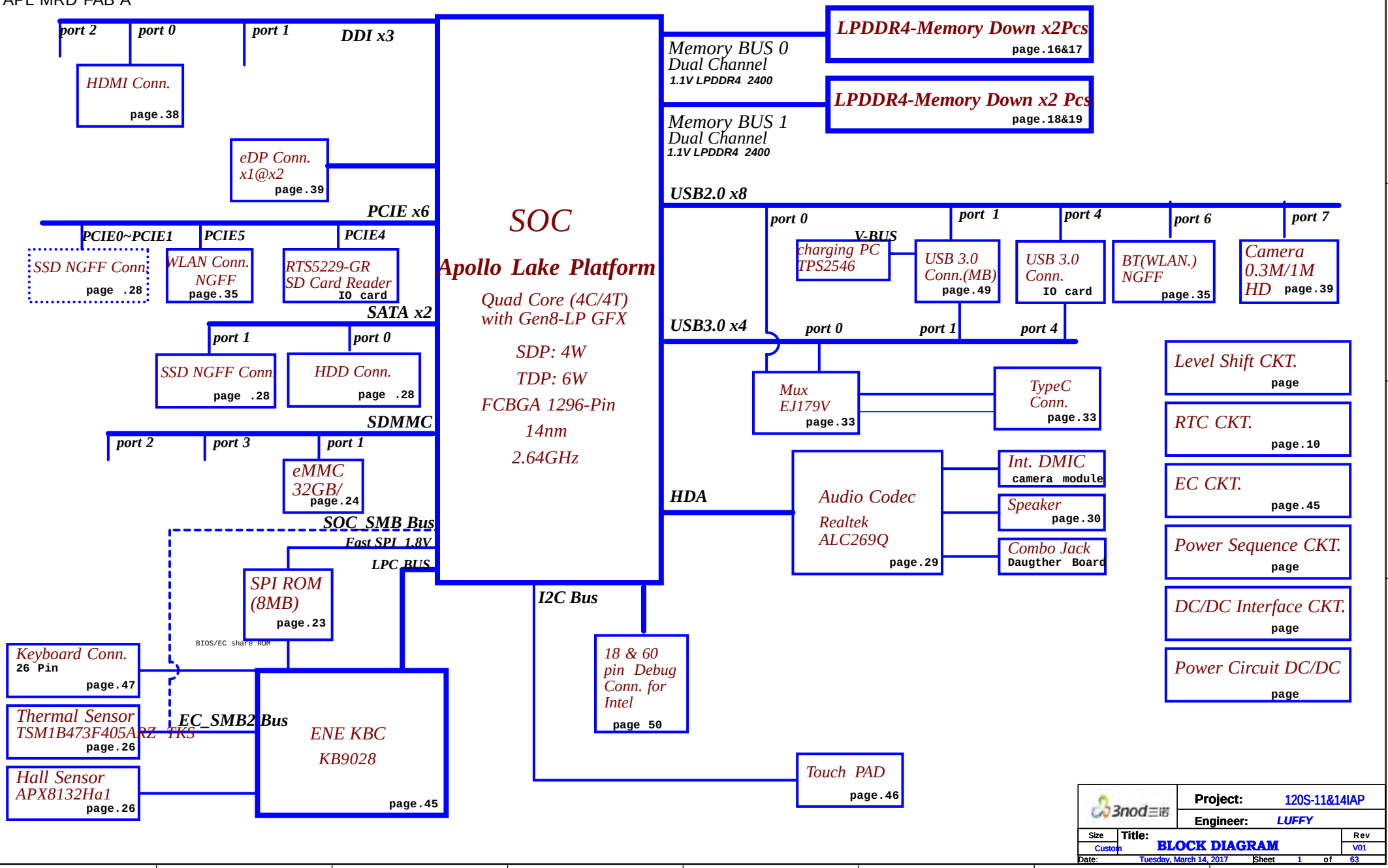
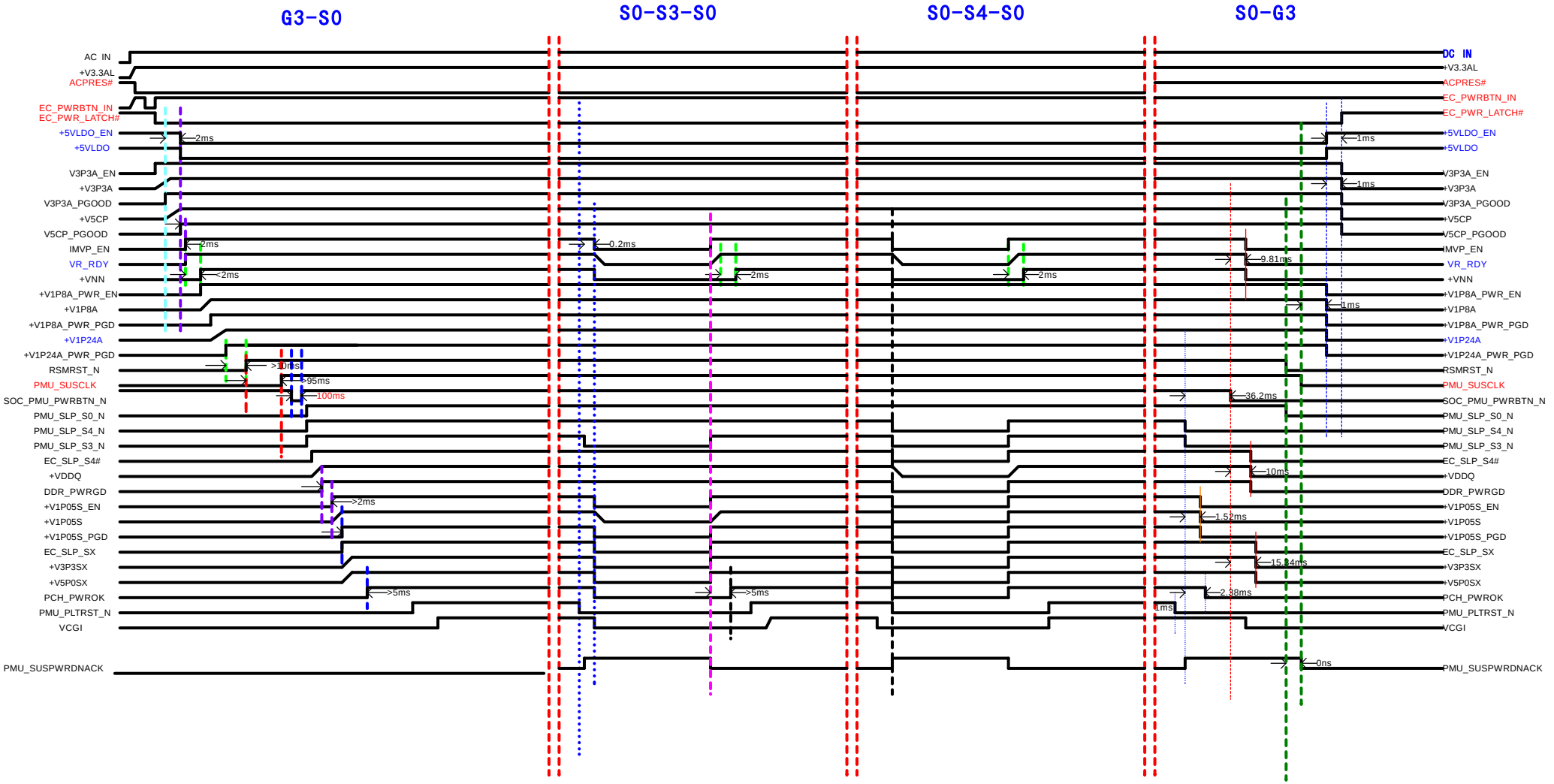
APL MRD FAB A



3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: BLOCK DIAGRAM	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 1 of 63	



INTERNAL ONLY

BPAGE DRAWING

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Fri May 27 06:47:24 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	Lear
Size: Custom	Title:	<POWER SEQUENCE>
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 2 of 63	

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BPAGE DRAWING

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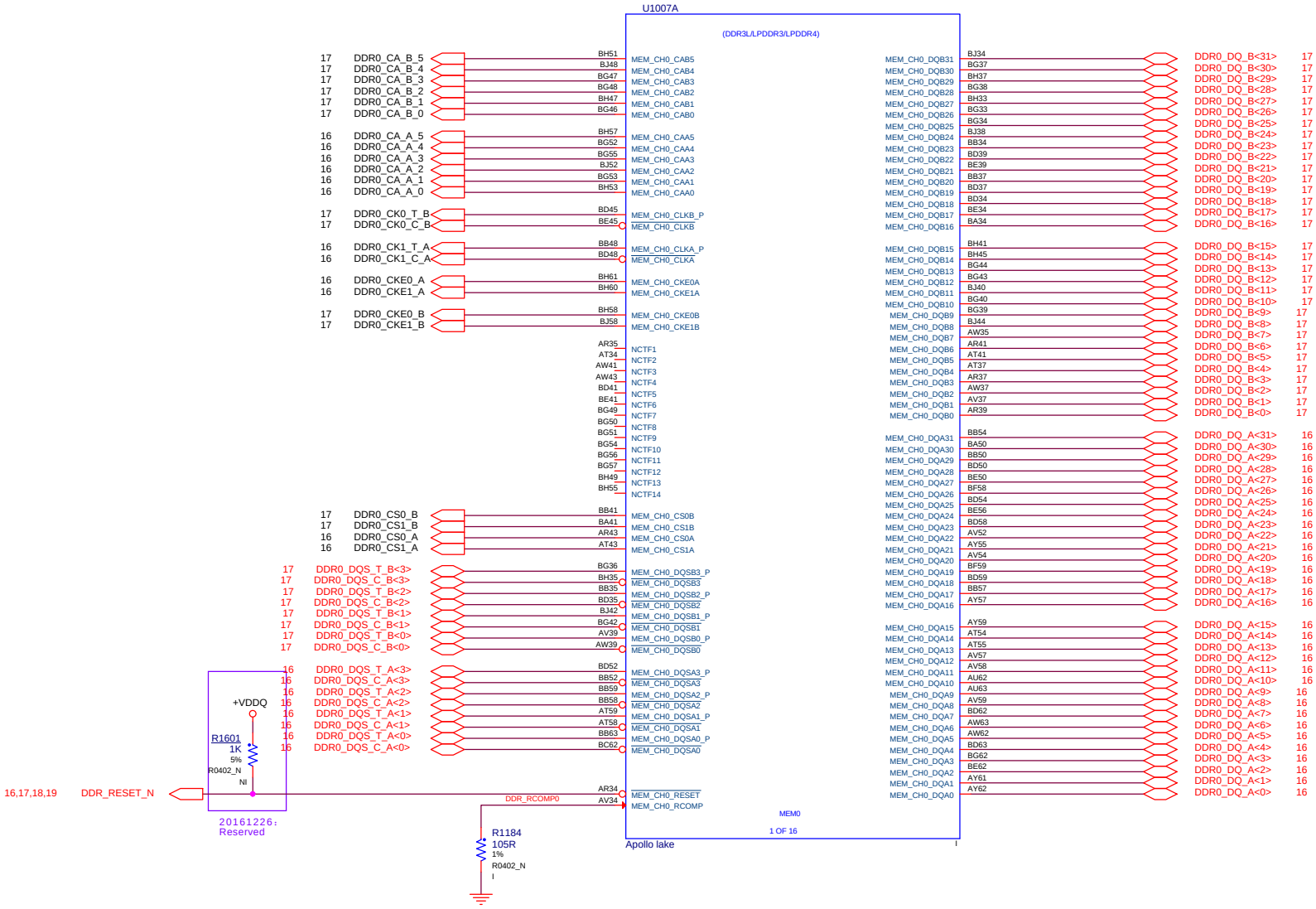
Fri May 27 06:47:10 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: TABLE OF CONTENTS	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 3 of 63	



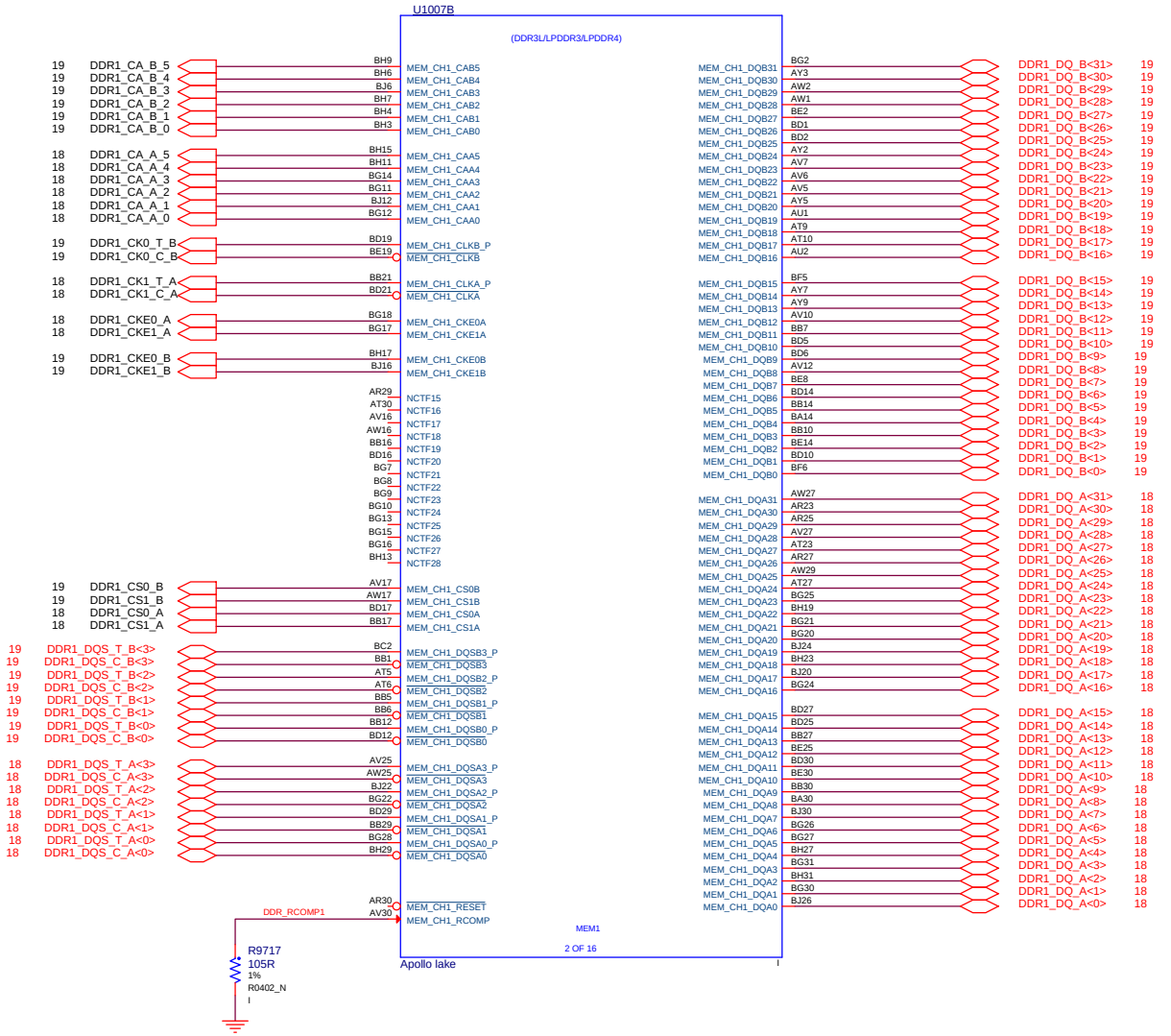
INTERNAL ONLY

BPAGE DRAWING

apl_ll.UN$20.205
Fri May 27 06:47:34 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	<APL SOC-LPDDR4 CH0>
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 4 of 63	

SOC: LPDDR4 CH1



BPAGE DRAWING

apl_lf.8A
Fri May 27 06:47:12 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: SOC-LDDR4 CH1	Rev: V01
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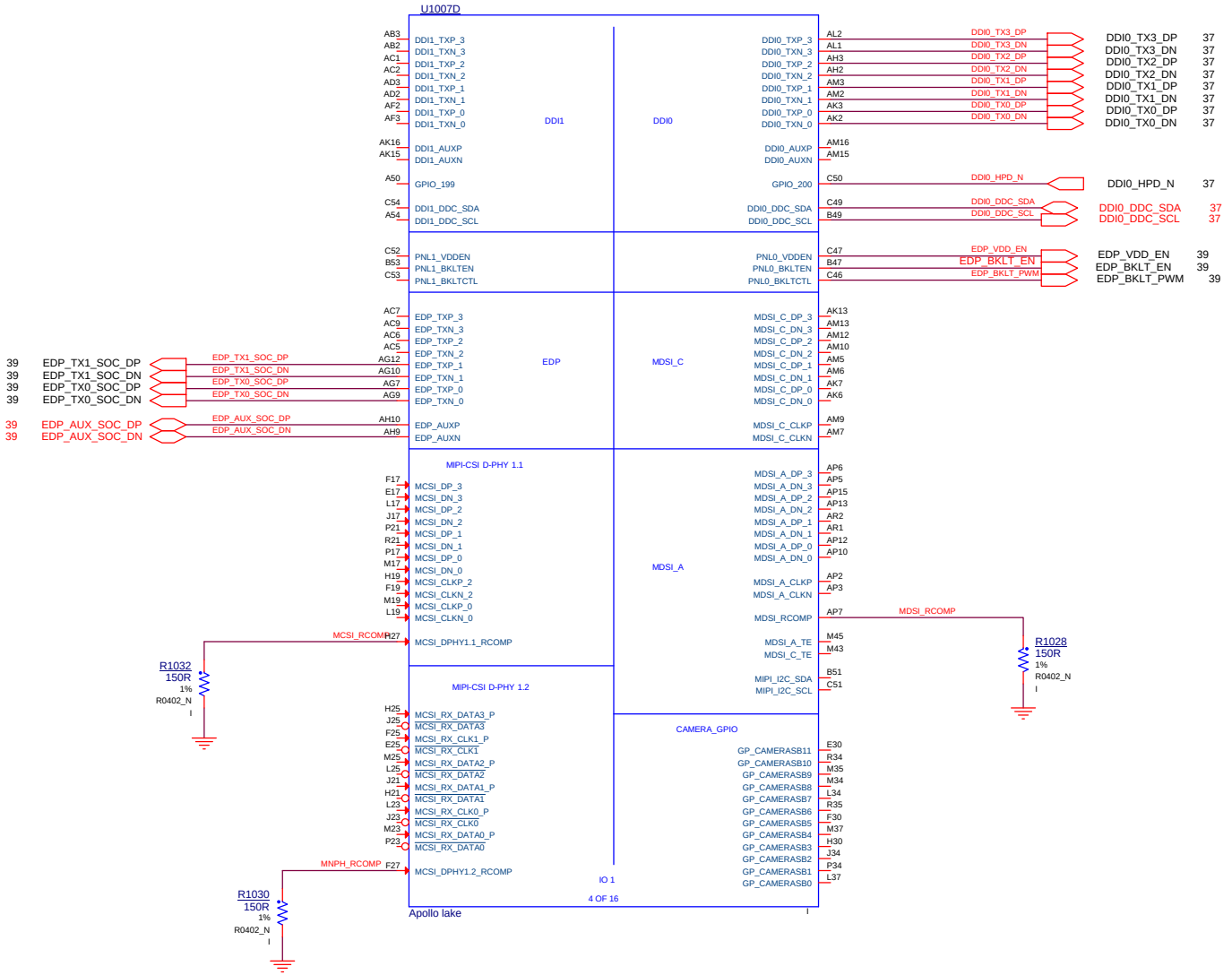
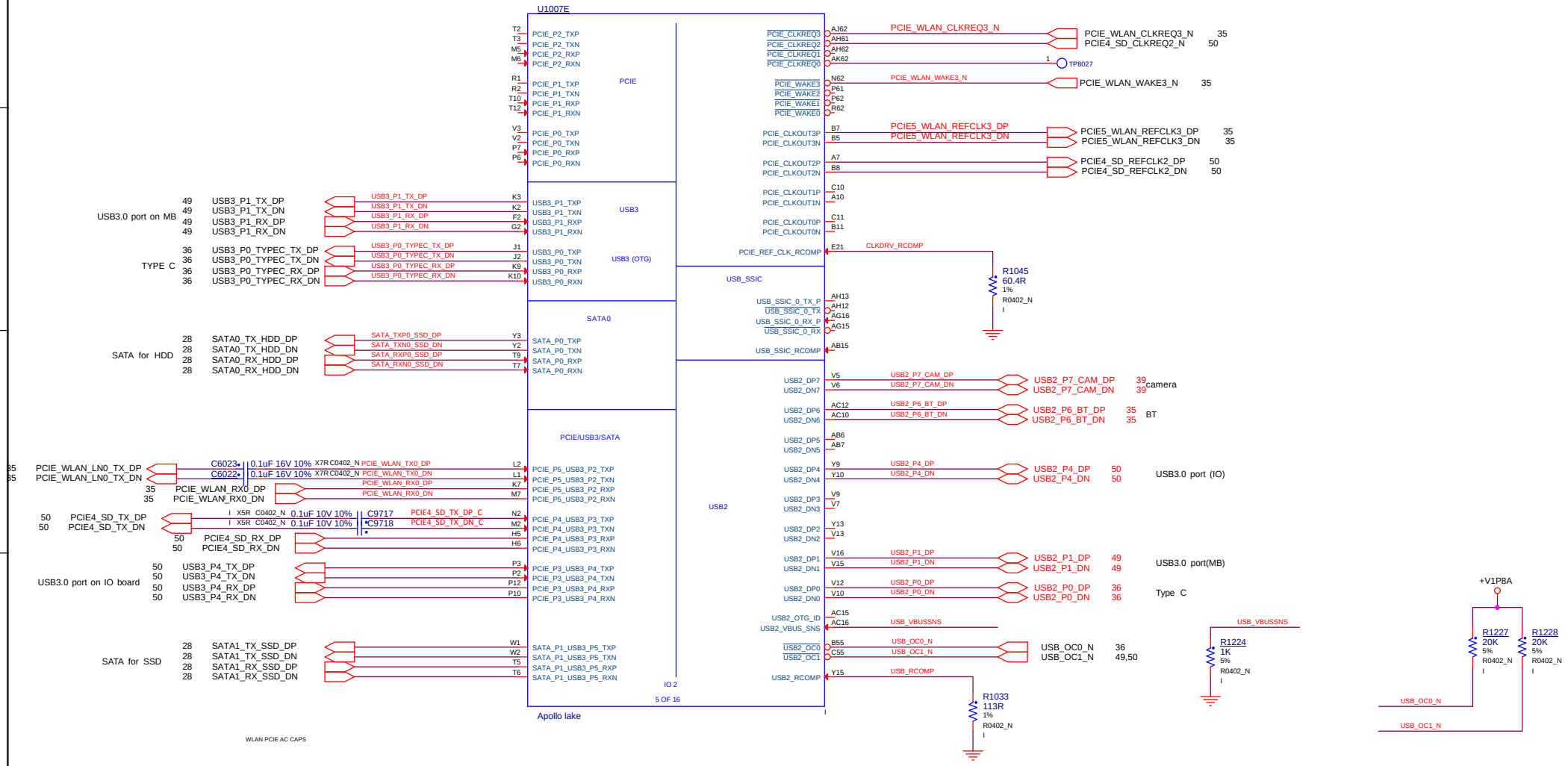


BPAGE DRAWING

apl_lf.GND

Fri May 27 06:47:12 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: SOC-DISPLAY	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 6 of 63	



Project:	120S-11&14IAP	
Engineer:	LUFFY	
Size: Custom	Title: SOC-PCIE&USB	Rev: V01
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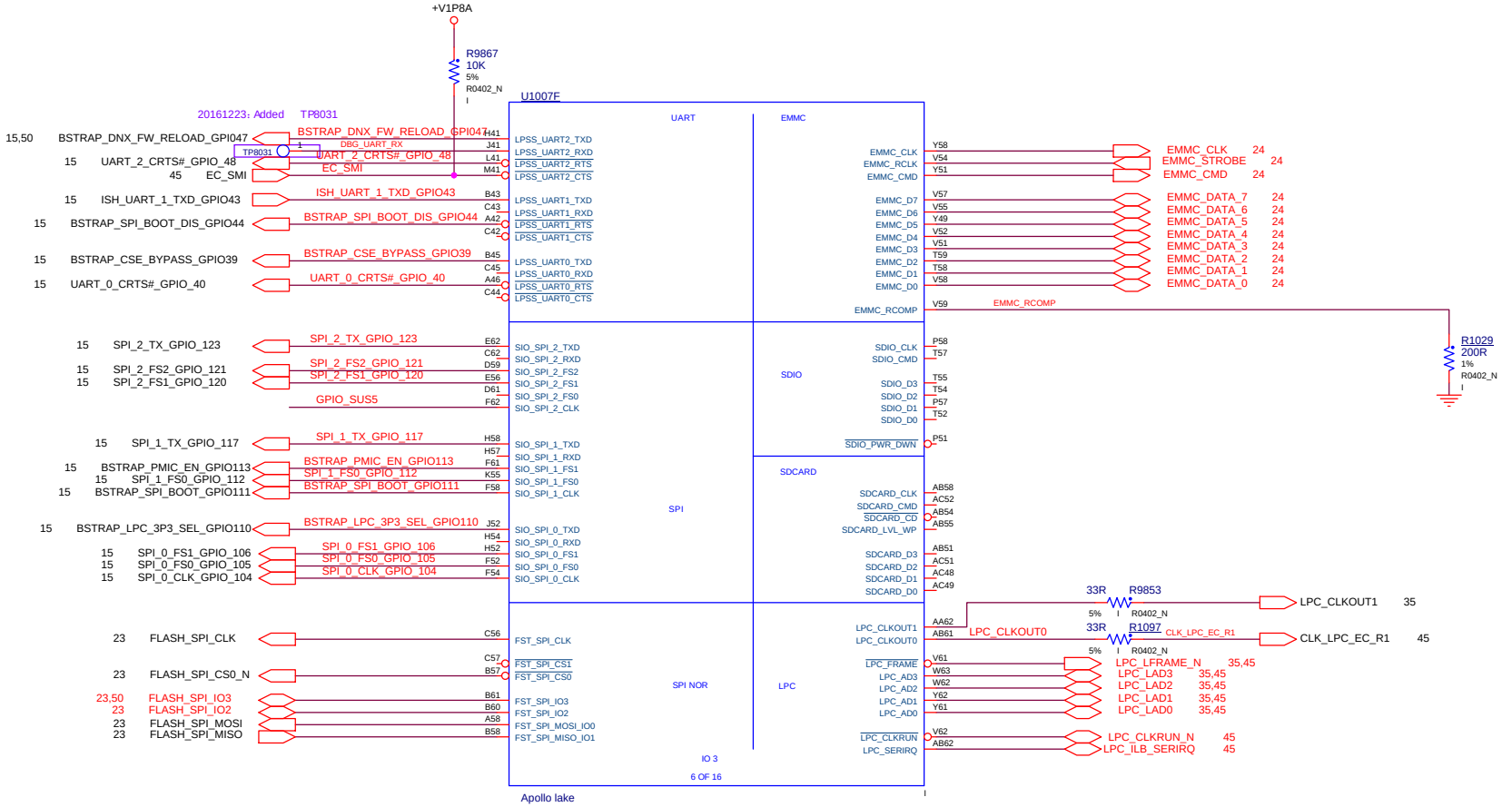
2016?12?Change to N1


+V1P8A
R9867
10K
5%
R0402_N
U1007F
UART
EMMC
SDIO
SDCARD
SPI
SPI NOR
LPC
IO 3
6 OF 16
Apollo lake
20161223: Added TP8031
15,50 BSTRAP_DNX_FW_RELOAD_GPIO47
BSTRAP_DNX_FW_RELOAD_GPIO47
TP8031
DBG_UART_RX
UART_2_CRTS#_GPIO_48
15 UART_2_CRTS#_GPIO_48
45 EC_SMI
EC_SMI
15 ISH_UART_1_TXD_GPIO43
ISH_UART_1_TXD_GPIO43
15 BSTRAP_SPI_BOOT_DIS_GPIO44
BSTRAP_SPI_BOOT_DIS_GPIO44
15 BSTRAP_CSE_BYPASS_GPIO39
BSTRAP_CSE_BYPASS_GPIO39
15 UART_0_CRTS#_GPIO_40
UART_0_CRTS#_GPIO_40
LPSS_UART2_TXD
LPSS_UART2_RXD
LPSS_UART2_RTS
LPSS_UART2_CTS
LPSS_UART1_TXD
LPSS_UART1_RXD
LPSS_UART1_RTS
LPSS_UART1_CTS
LPSS_UART0_TXD
LPSS_UART0_RXD
LPSS_UART0_RTS
LPSS_UART0_CTS
EMMC_CLK
EMMC_RCLK
EMMC_CMD
EMMC_D7
EMMC_D6
EMMC_D5
EMMC_D4
EMMC_D3
EMMC_D2
EMMC_D1
EMMC_D0
EMMC_RCOMP
EMMC_CLK 24
EMMC_STROBE 24
EMMC_CMD 24
EMMC_DATA_7 24
EMMC_DATA_6 24
EMMC_DATA_5 24
EMMC_DATA_4 24
EMMC_DATA_3 24
EMMC_DATA_2 24
EMMC_DATA_1 24
EMMC_DATA_0 24
R1029
200R
1%
R0402_N
15 SPI_2_TX_GPIO_123
15 SPI_2_FS2_GPIO_121
15 SPI_2_FS1_GPIO_120
GPIO_SUS5
SPI_2_TX_GPIO_123
SPI_2_FS2_GPIO_121
SPI_2_FS1_GPIO_120
SIO_SPI_2_TXD
SIO_SPI_2_RXD
SIO_SPI_2_FS2
SIO_SPI_2_FS1
SIO_SPI_2_FS0
SIO_SPI_2_CLK
SDIO_CLK
SDIO_CMD
SDIO_D3
SDIO_D2
SDIO_D1
SDIO_D0
SDIO_PWR_DWN
15 SPI_1_TX_GPIO_117
15 BSTRAP_PMIC_EN_GPIO113
15 SPI_1_FS0_GPIO_112
15 BSTRAP_SPI_BOOT_GPIO111
SPI_1_TX_GPIO_117
BSTRAP_PMIC_EN_GPIO113
SPI_1_FS0_GPIO_112
BSTRAP_SPI_BOOT_GPIO111
SIO_SPI_1_TXD
SIO_SPI_1_RXD
SIO_SPI_1_FS1
SIO_SPI_1_FS0
SIO_SPI_1_CLK
SDCARD_CLK
SDCARD_CMD
SDCARD_CD
SDCARD_LVL_WP
SDCARD_D3
SDCARD_D2
SDCARD_D1
SDCARD_D0
15 BSTRAP_LPC_3P3_SEL_GPIO110
BSTRAP_LPC_3P3_SEL_GPIO110
15 SPI_0_FS1_GPIO_106
15 SPI_0_FS0_GPIO_105
15 SPI_0_CLK_GPIO_104
SPI_0_FS1_GPIO_106
SPI_0_FS0_GPIO_105
SPI_0_CLK_GPIO_104
SIO_SPI_0_TXD
SIO_SPI_0_RXD
SIO_SPI_0_FS1
SIO_SPI_0_FS0
SIO_SPI_0_CLK
23 FLASH_SPI_CLK
23 FLASH_SPI_CS0_N
23,50 FLASH_SPI_IO3
23 FLASH_SPI_IO2
23 FLASH_SPI_MOSI
23 FLASH_SPI_MISO
FLASH_SPI_CLK
FLASH_SPI_CS0_N
FLASH_SPI_IO3
FLASH_SPI_IO2
FLASH_SPI_MOSI
FLASH_SPI_MISO
FST_SPI_CLK
FST_SPI_CS1
FST_SPI_CS0
FST_SPI_IO3
FST_SPI_IO2
FST_SPI_MOSI_IO0
FST_SPI_MISO_IO1
LPC_CLKOUT1
LPC_CLKOUT0
LPC_FRAME
LPC_AD3
LPC_AD2
LPC_AD1
LPC_AD0
LPC_CLKRUN
LPC_SERIRQ
33R R9853
LPC_CLKOUT1 35
LPC_CLKOUT0
33R R1097
CLK_LPC_EC_R1
CLK_LPC_EC_R1 45
LPC_LFRAME_N 35,45
LPC_LAD3 35,45
LPC_LAD2 35,45
LPC_LAD1 35,45
LPC_LAD0 35,45
LPC_CLKRUN_N 45
LPC_ILB_SERIRQ 45
+V1P8A
R9857
1K
5%
R0402_N
Q9513
2N7002KW 115mA 60V
sot_323_dgs
R9854
100R
5%
R0402_N
TXE _Reflash 45
GPIO_SUS5
R9856
10K
5%
R0402_N
R9855
100K
5%
R0402_N
20161220 :R9855 changed to 100K
20161220 :R9856 changed to I
GPIO_SUS5(20K PD)
Security Flash Descriptors
0 = Normal Operation
1 = Override
20161220 :Modified
CONN TBD
R1199 - EMMC BOOT STRAP
BPAGE DRAWING
apl_lf.GND
Fri May 27 06:47:12 2016
Project: 120S-11&14IAP
Engineer: LUFFY
Size: Custom
Title: SOC-EMMC,SPI,LPC
Rev: V01
Date: Tuesday, March 14, 2017
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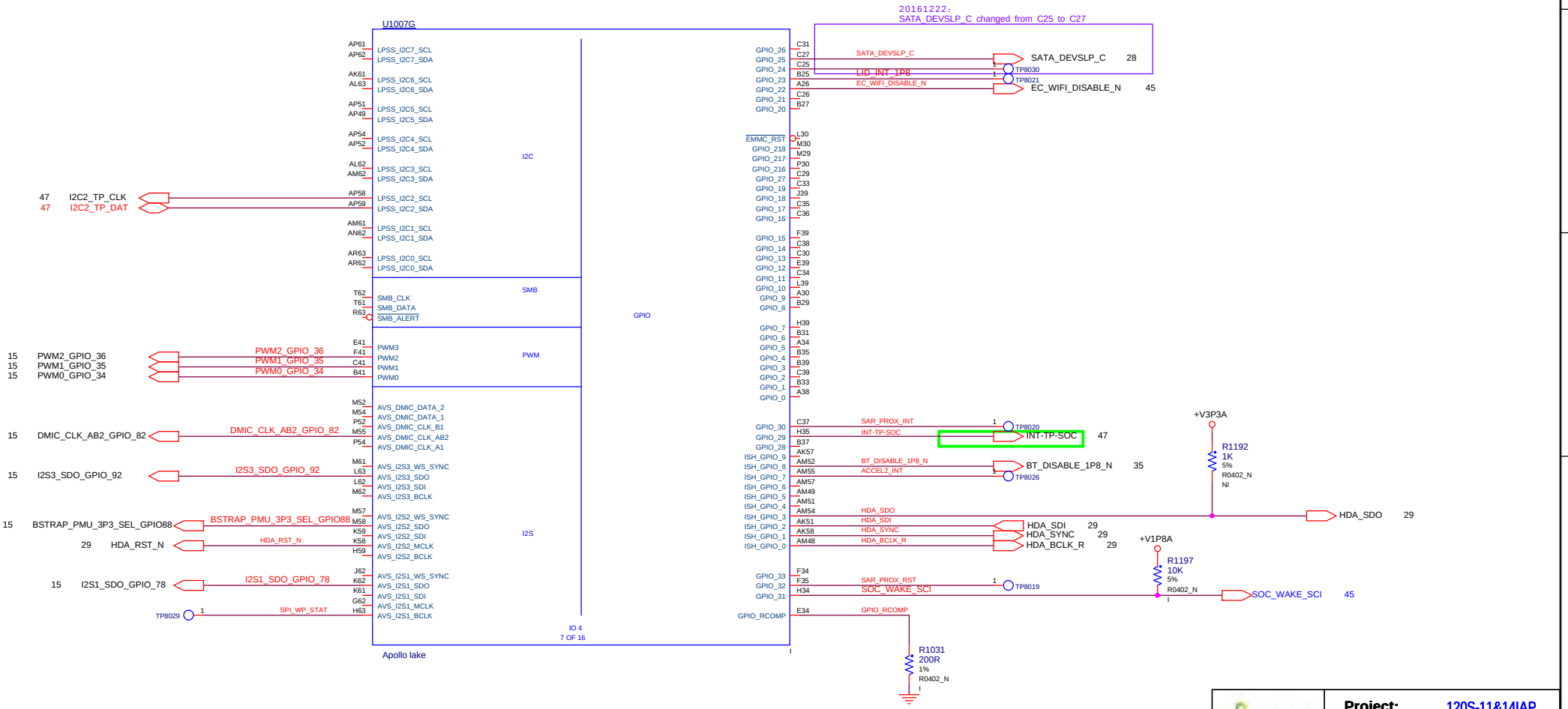

BPAGE DRAWING

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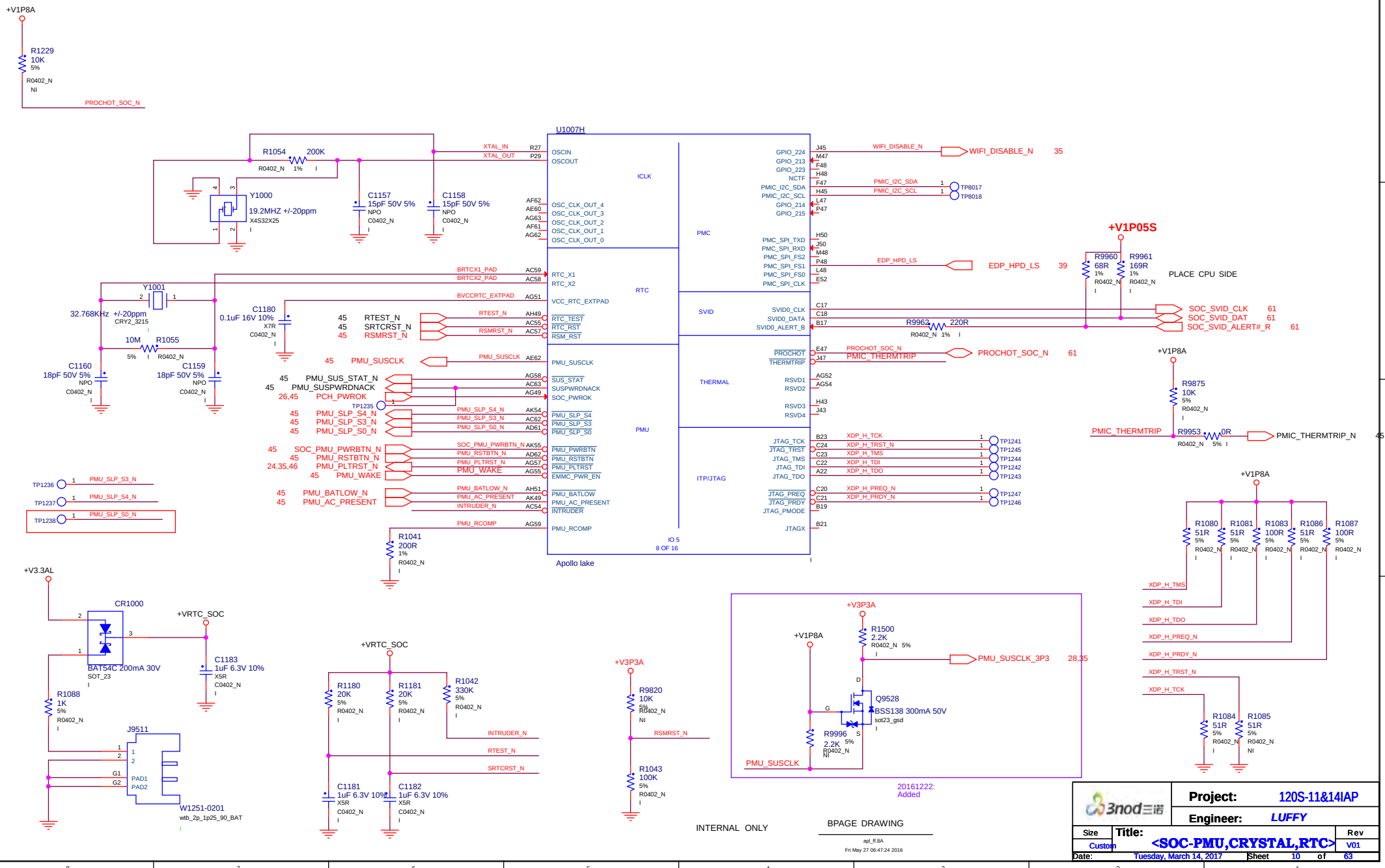
Fri May 27 06:47:14 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: SOC- I2C&HDA	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 9 of 63	


+V1P8A
R1229 10K 5% R0402_N NI
PROCHOT_SOC_N
U1007H
R1054 200K R0402_N 1%
Y1000 19.2MHZ +/-20ppm X4S32X25
C1157 15pF 50V 5% NPO C0402_N
C1158 15pF 50V 5% NPO C0402_N
XTAL_IN R27
XTAL_OUT P29
OSCIN
OSCOUT
ICLK
OSC_CLK_OUT_4 AF62
OSC_CLK_OUT_3 AE60
OSC_CLK_OUT_2 AG63
OSC_CLK_OUT_1 AF61
OSC_CLK_OUT_0 AG62
PMC
RTC
SVID
THERMAL
PMU
ITP/JTAG
GPIO_224 J45
GPIO_213 M47
GPIO_223 F48
NCTF H48
PMIC_I2C_SDA F47
PMIC_I2C_SCL H45
GPIO_214 L47
GPIO_215 P47
PMC_SPI_TXD H50
PMC_SPI_RXD J50
PMC_SPI_FS2 M48
PMC_SPI_FS1 P48
PMC_SPI_FS0 L48
PMC_SPI_CLK E52
WIFI_DISABLE_N
WIFI_DISABLE_N 35
PMIC_I2C_SDA
PMIC_I2C_SCL
TP8017
TP8018
EDP_HPD_LS
EDP_HPD_LS 39
+V1P05S
R9960 68R 1% R0402_N
R9961 169R 1% R0402_N
PLACE CPU SIDE
SVID0_CLK C17
SVID0_DATA C18
SVID0_ALERT_B B17
R9962 220R R0402_N 1%
SOC_SVID_CLK 61
SOC_SVID_DAT 61
SOC_SVID_ALERT#_R 61
PROCHOT E47
THERMTRIP J47
PROCHOT_SOC_N
PMIC_THERMTRIP
PROCHOT_SOC_N 61
RSVD1 AG52
RSVD2 AG54
RSVD3 H43
RSVD4 J43
+V1P8A
R9875 10K 5% R0402_N
PMIC_THERMTRIP
R9953 0R R0402_N 5%
PMIC_THERMTRIP_N 45
JTAG_TCK B23
JTAG_TRST C24
JTAG_TMS C23
JTAG_TDI C22
JTAG_TDO A22
JTAG_PREQ C20
JTAG_PRDY C21
JTAG_PMODE B19
JTAGX B21
XDP_H_TCK
XDP_H_TRST_N
XDP_H_TMS
XDP_H_TDO
XDP_H_PREQ_N
XDP_H_PRDY_N
TP1241
TP1245
TP1244
TP1242
TP1243
TP1247
TP1246
Y1001 32.768KHz +/-20ppm CRY2_3215
C1160 18pF 50V 5% NPO C0402_N
C1159 18pF 50V 5% NPO C0402_N
10M R1055 5% R0402_N
C1180 0.1uF 16V 10% X7R C0402_N
BRTCX1_PAD AC59
BRTCX2_PAD AC58
BVCCRTC_EXTPAD AG51
RTC_X1
RTC_X2
VCC_RTC_EXTPAD
RTC_TEST
RTC_RST
RSM_RST
45 RTEST_N
45 SRTCRST_N
45 RSMRST_N
RTEST_N AH49
AC55
RSMRST_N AC57
45 PMU_SUSCLK
PMU_SUSCLK AE62
45 PMU_SUS_STAT_N
45 PMU_SUSPWRDNACK
26,45 PCH_PWROK
SUS_STAT AG58
SUSPWRDNACK AC63
SOC_PWROK AG49
TP1235
45 PMU_SLP_S4_N
45 PMU_SLP_S3_N
45 PMU_SLP_S0_N
PMU_SLP_S4_N AK54
PMU_SLP_S3_N AC62
PMU_SLP_S0_N AD61
PMU_SLP_S4
PMU_SLP_S3
PMU_SLP_S0
45 SOC_PMU_PWRBTN_N
45 PMU_RSTBTN_N
24,35,46 PMU_PLTRST_N
45 PMU_WAKE
SOC_PMU_PWRBTN_N AK55
PMU_RSTBTN_N AD62
PMU_PLTRST_N AG57
PMU_WAKE AG55
PMU_PWRBTN
PMU_RSTBTN
PMU_PLTRST
EMMC_PWR_EN
45 PMU_BATLOW_N
45 PMU_AC_PRESENT
PMU_BATLOW_N AH51
PMU_AC_PRESENT AK49
INTRUDER_N AC54
PMU_BATLOW
PMU_AC_PRESENT
INTRUDER
PMU_RCOMP AG59
PMU_RCOMP
R1041 200R 1% R0402_N
IO 5
8 OF 16
Apollo lake
TP1236 PMU_SLP_S3_N
TP1237 PMU_SLP_S4_N
TP1238 PMU_SLP_S0_N
+V1P8A
R1080 51R 5% R0402_N
R1081 51R 5% R0402_N
R1083 100R 5% R0402_N
R1086 51R 5% R0402_N
R1087 100R 5% R0402_N
R1084 51R 5% R0402_N
R1085 51R 5% R0402_N NI
+V3.3AL
CR1000 BAT54C 200mA 30V SOT_23
+VRTC_SOC
C1183 1uF 6.3V 10% X5R C0402_N
R1088 1K 5% R0402_N
J9511 W1251-0201 wtb_2p_1p25_90_BAT
R1180 20K 5% R0402_N
R1181 20K 5% R0402_N
R1042 330K 5% R0402_N
INTRUDER_N
RTEST_N
SRTCRST_N
C1181 1uF 6.3V 10% X5R C0402_N
C1182 1uF 6.3V 10% X5R C0402_N
+V3P3A
R9820 10K 5% R0402_N NI
RSMRST_N
R1043 100K 5% R0402_N
+V3P3A
+V1P8A
R1500 2.2K R0402_N 5%
PMU_SUSCLK_3P3 28,35
Q9528 BSS138 300mA 50V sot23_gsd
R9996 2.2K 5% R0402_N NI
PMU_SUSCLK
20161222: Added
INTERNAL ONLY
BPAGE DRAWING
apl_ff.8A
Fri May 27 06:47:24 2016
3nod三诺
Project: 120S-11&14IAP
Engineer: LUFFY
Size Custom
Title: <SOC-PMU,CRYSTAL,RTC>
Rev V01
Date: Tuesday, March 14, 2017
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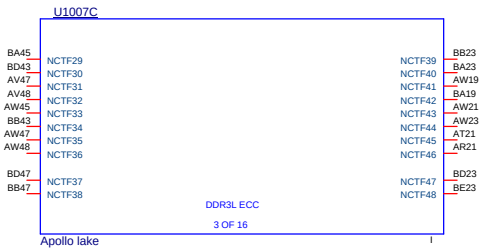

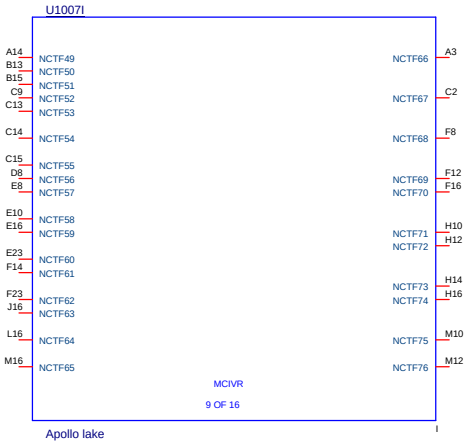

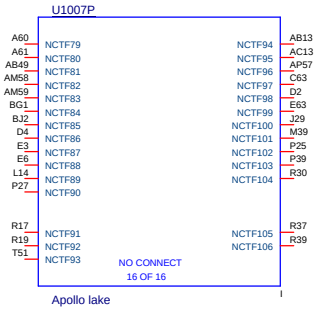

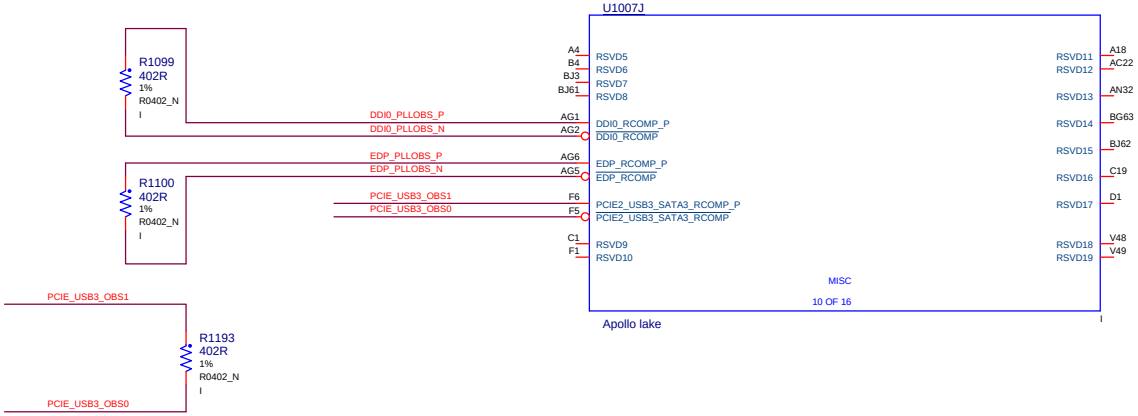

INTERNAL ONLY

BPAGE DRAWING

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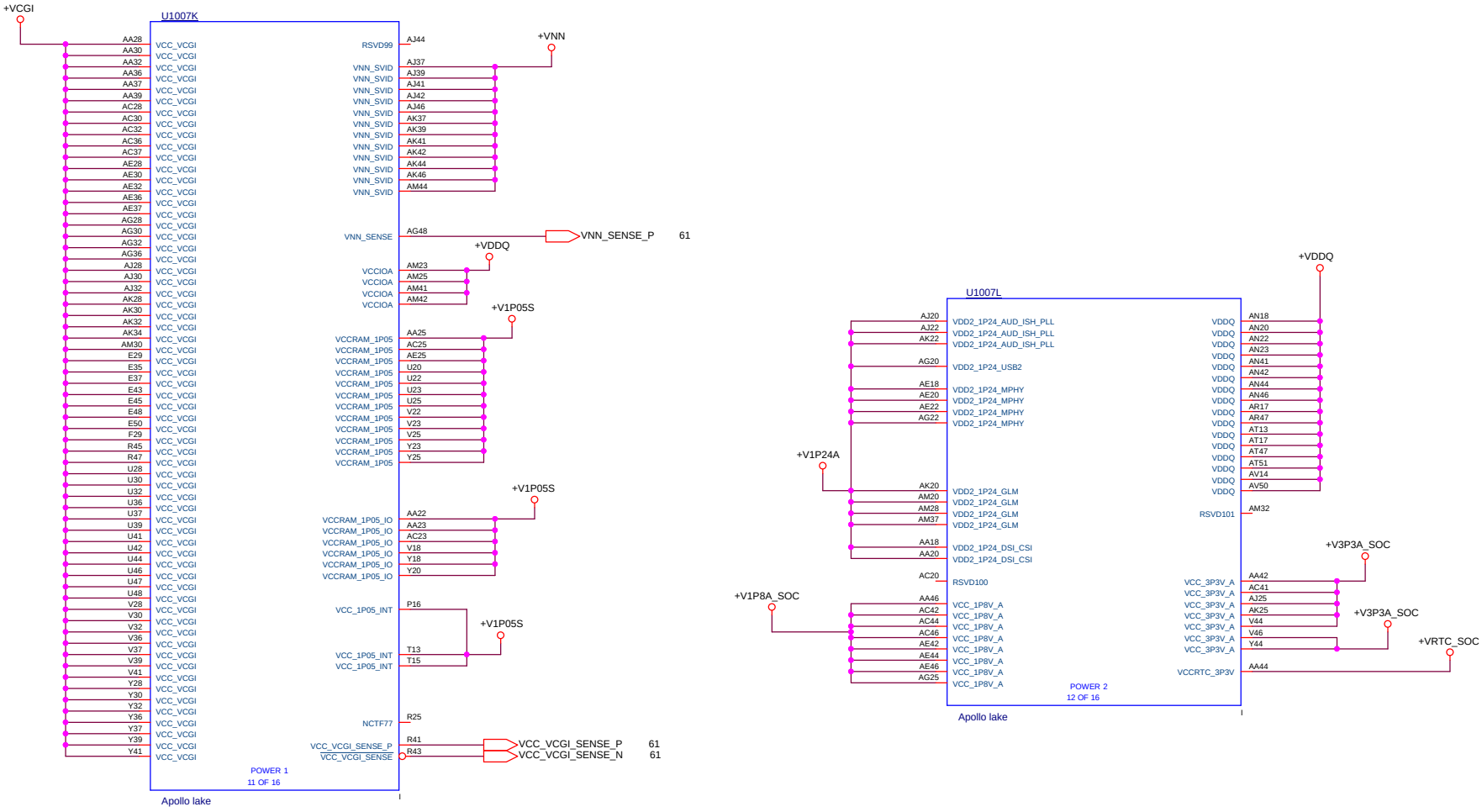
Fri May 27 06:47:24 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <SOC-MISC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 11 of 63	

SOC: POWER



BPAGE DRAWING

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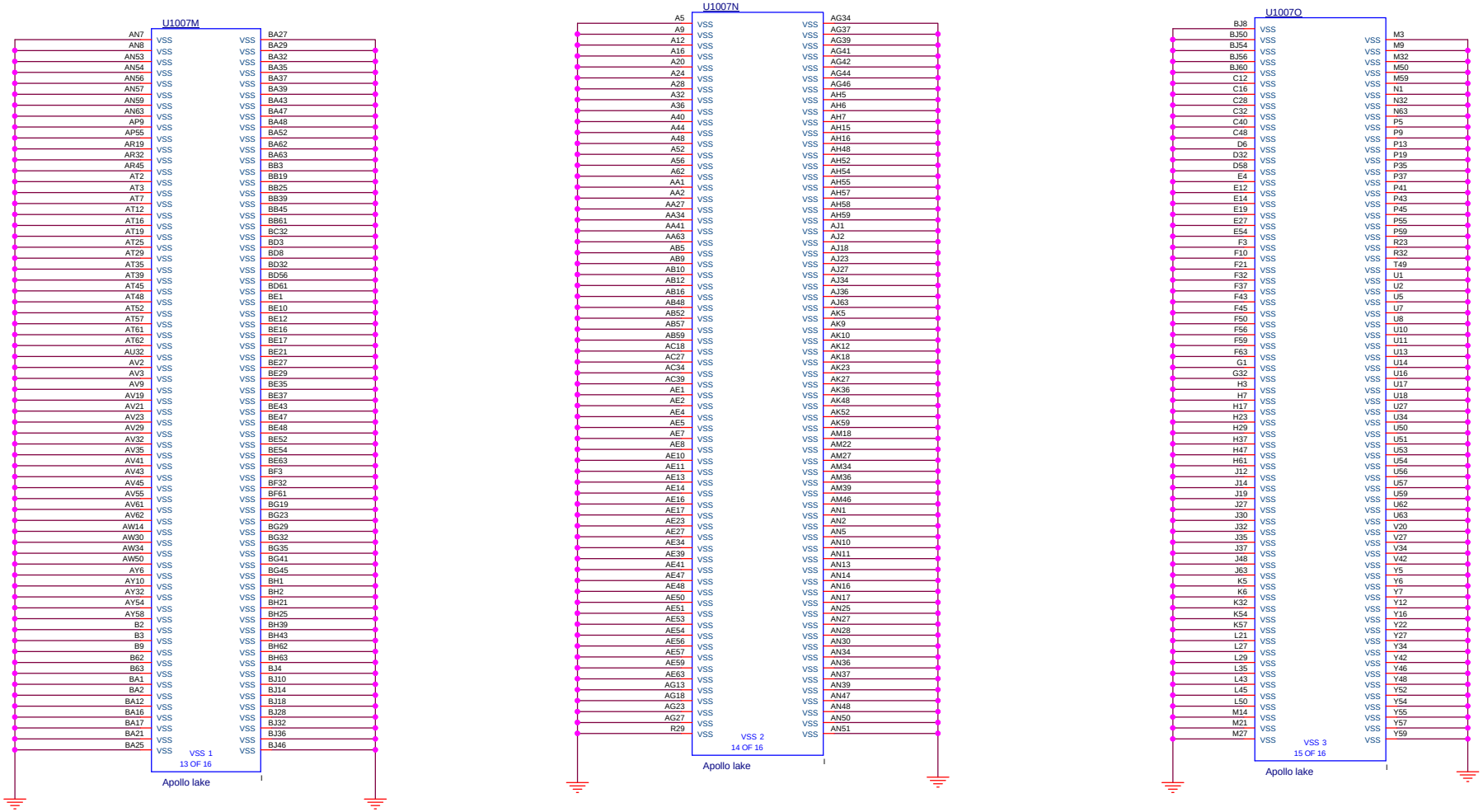
Fri May 27 06:47:14 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	SOC-POWER
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 12 of 63	

SOC: GND



BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:14 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: SOC-GND	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 13 of 63	

SOC: DECAPS

CAD NOTE:
PLACE IN BETWEEN SOC AND DRAM

+V1P8A_SOC — +V1P8A
NOBOM
JUMP_43X39
JUMP-SH1110

+V3P3A_SOC — +V3P3A
NOBOM
JUMP_43X39
JUMP-SH1111

+VDDQ
C1073 C1081 C1088 C1093 C1071 C1075 C1076 C1078
22uF 6.3V 20% X5R C0603_N

20161223"
Changed the footprint to 0603

+VDDQ (BSC)
C1241 1uF 6.3V 10% X5R C0402_N
C1242 1uF 6.3V 10% X5R C0402_N

+V1P8A_SOC (BSC)
C1132 C1135 C1138 C1140 1uF 6.3V 10% X5R C0402_N
C1143 22uF 6.3V 20% X5R C0603_N

+V3P3A_SOC (BSC)
C1144 C1145 C1146 C1215 1uF 6.3V 10% X5R C0402_N
C1147 22uF 6.3V 20% X5R C0603_N

+V1P24A (BSC)
C1108 C1110 C1112 C1116 C1119 C1123 C1127 C1131 1uF 6.3V 10% X5R C0402_N
C1109 C1111 C1113 C1118 C1126 C1130 C1134 C1137 22uF 6.3V 20% X5R C0603_N

+VNN (BSC)
C1235 C1086 C1092 C1097 1uF 6.3V 10% X5R C0402_N

+VNN
C1114 1uF 6.3V 10% X5R C0402_N

+VRTC_SOC
C1236 C1087 C1082 C1083 C1094 C1098 22uF 6.3V 20% X5R C0603_N
C1142 1uF 6.3V 10% X5R C0402_N

CAD NOTE: C1142 PLACE CLOSE TO PIN AA44

+V1P05S
C1117 C1121 C1125 C1129 1uF 6.3V 10% X5R C0402_N
C1133 C1136 C1139 22uF 6.3V 20% X5R C0603_N

BSC
C1115 C1120 C1124 C1128 1uF 6.3V 10% X5R C0402_N

+VCGI

BSC
C1067 C1069 C1074 C1079 C1085 C1091 C1096 C1100 C1102 C1104 C1105 C1214 1uF 6.3V 10% X5R C0402_N

C1068 22uF 6.3V 20% X5R C0603_N
MLCC
C1089 C1095 C1099 C1103 22uF 6.3V 20% X5R C0603_N

20170323 Deleted C1169

20170323 Deleted C1072,C1077,C1084

20170207 Changed to NI;
20170210 Deleted C1007/C1015

C1148 C1149 1uF 6.3V 10% X5R C0402_N

BPAGE DRAWING

apl_tl.8A
Fri May 27 06:47:16 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: SOC-(DECAP)	Rev: V01
Date: Thursday, March 23, 2017	Sheet 14 of 63	

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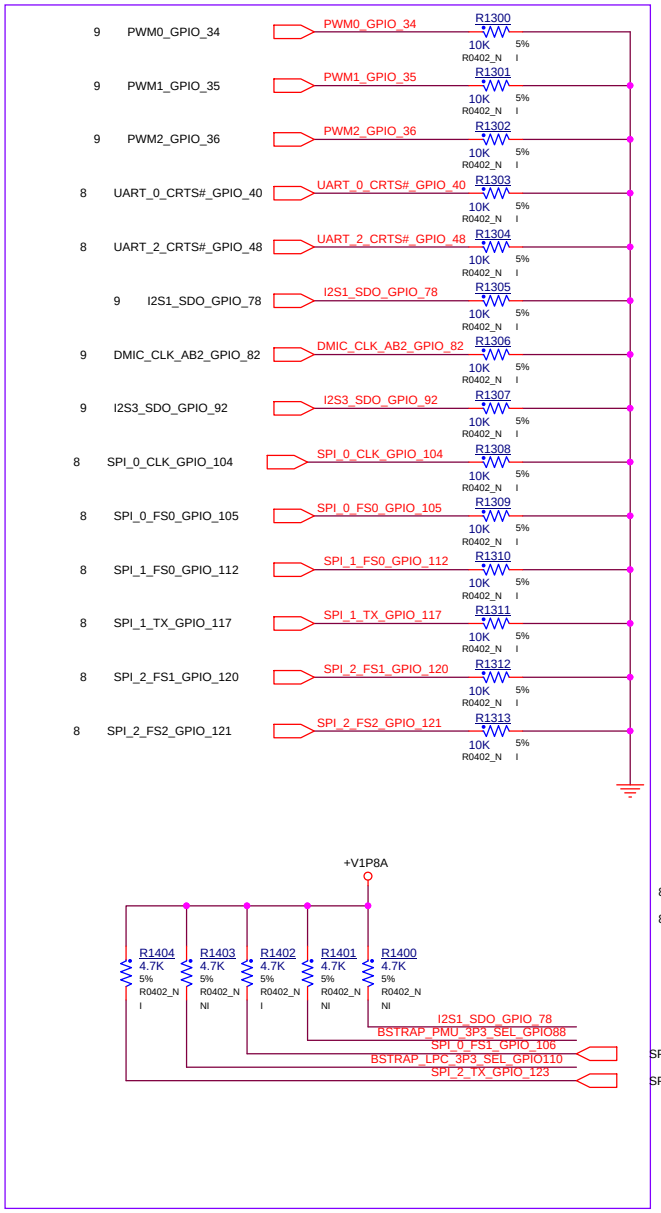
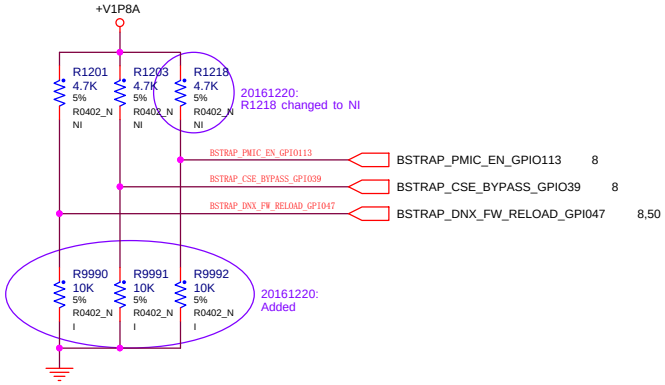
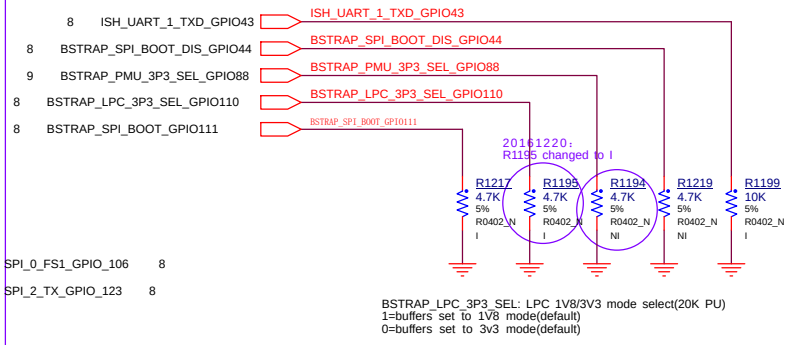


20161220:
Added





BSTRAP_LPC_3P3_SEL: LPC 1V8/3V3 mode select(20K PU)
1=buffers set to 1V8 mode(default)
0=buffers set to 3v3 mode(default)

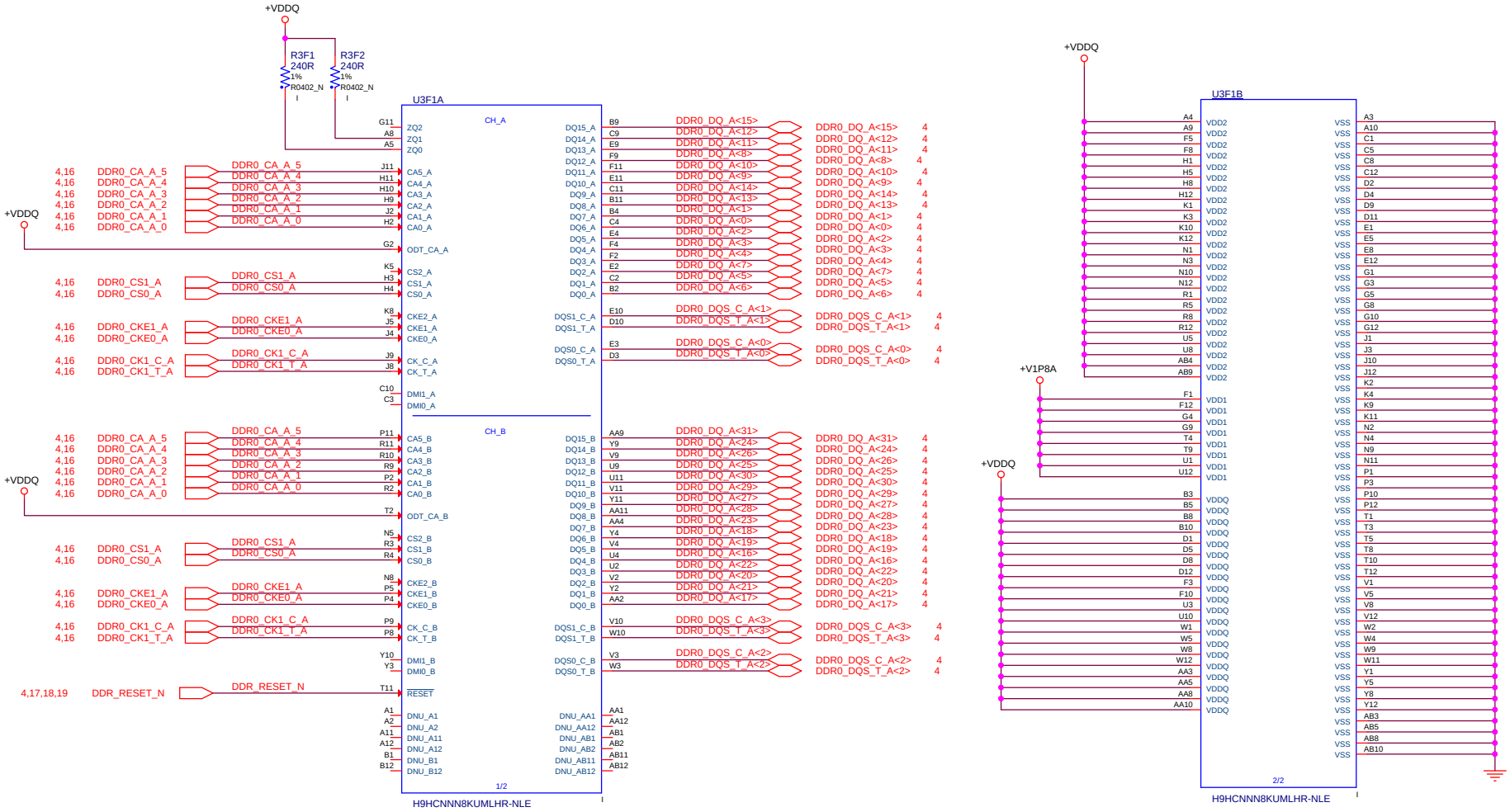
BXT-P GPIO	SOC Ball Name	BSTRAP	Default Internal PU/PD
GPIO34	PWM0	Delayed_vref_switch) 0= not delayed(Default) 1=delayed	PD
GPIO35	PWM1	Spare1 0= do not stall boot FSM(Default) 1=stall boot FSM	PD
GPIO36	PWM2	Spare2 0 =VDD2 IS 1.24V(Default) 1=VDD2 IS 1.35V	PD
GPIO39	LPASS_UART0_TXD	Eable CSE ROM bypass 0 = disable bypass (default) 1 = enable bypass	PD
GPIO40	RTC Clock Timer Bypass	RTC Clock Timer Bypass 0 =disable bypass (Default) 1 =enable bypass	PD
GPIO43	LPASS_UART1_TXD	Select eMMC boot source 0 =do now allow (Default) 1=allow	PU
GPIO44	LPASS_UART1_RTS_B	Select SPI boot source 0 =Disable 1=Enable(Default)	PU
GPIO47	LPASS_UART2_TXD	Force DNX FW Load 0 =Disable(Default) 1=Enable	PD
GPIO48	LPASS_UART2_RTS_B	LPC Boot strap 0 =Do not boot from LPC(Default) 1=Enable	PD
GPIO78	AVS_I2S1_SDO	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode (default)	PU
GPIO82	AVS_M_CLK_AB2	WC_PRESENT 0=non-Whiskey Cove(Default) 1=Whiskey Cove is connected	PD
GPIO88	AVS_I2S2_SD0	PMU (Power Management Unit) 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode (default)	PU
GPIO92	AVS_I2S3_SD0	SMBus No Re-Boot 0=Dsiable(Default) 1=Enable	PD
GPIO104	GP_SSP_0_CLK	(HVM Tester)XTAL startup 0=Dsiable(Default) 1=Enable	PD
GPIO105	GP_SSP_0_FS0	(HVM Tester)XTAL startup 0=Dsiable(Default) 1=Enable	PU
GPIO106	GP_SSP_0_FS1	Halts early boot for debug 0=Enable 1=Disable	PU
GPIO110	GP_SSP_0_TXD	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode (default)	PU
GPIO111	GP_SSP_1_CLK	SPI Boot BIOS strap 0=boot from SPI(Debug) 1=Do not boot from SPI (default)	PU
GPIO112	GP_SSP_1_FS0	Enable metal password auth 0=Disable 1=Enable	PD
GPIO113	GP_SSP_1_FS1	SVID diable 0=Enable SVID(Default) 1=Disbale SVID	PU
GPIO117	GP_SSP_1_TXD	Stall BOot FSM for debut 0=Do not stall boot FSM(Default) 1=stall boot FSM	PD
GPIO118	GP_SSP_2_CLK	Flash Descriptpr Override Pin-Strao status 0=Disable(Default) 1=Enable	PD
GPIO120	GP_SSP_2_FS1	Top swap pverride 0=Disable(Default) 1=Enable	PD
GPIO121	GP_SSP_2_FS2	Plled LOW when RSM_RST_N deasserts	PD
GPIO123	GP_SSP_2_TXD	Pulled HIGH when RSM_RST_N de-asserts	PU

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:16 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	SOC- (BOOT STRAP)
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 15 of 63	

CHANNEL 0 - MEMORY1/2

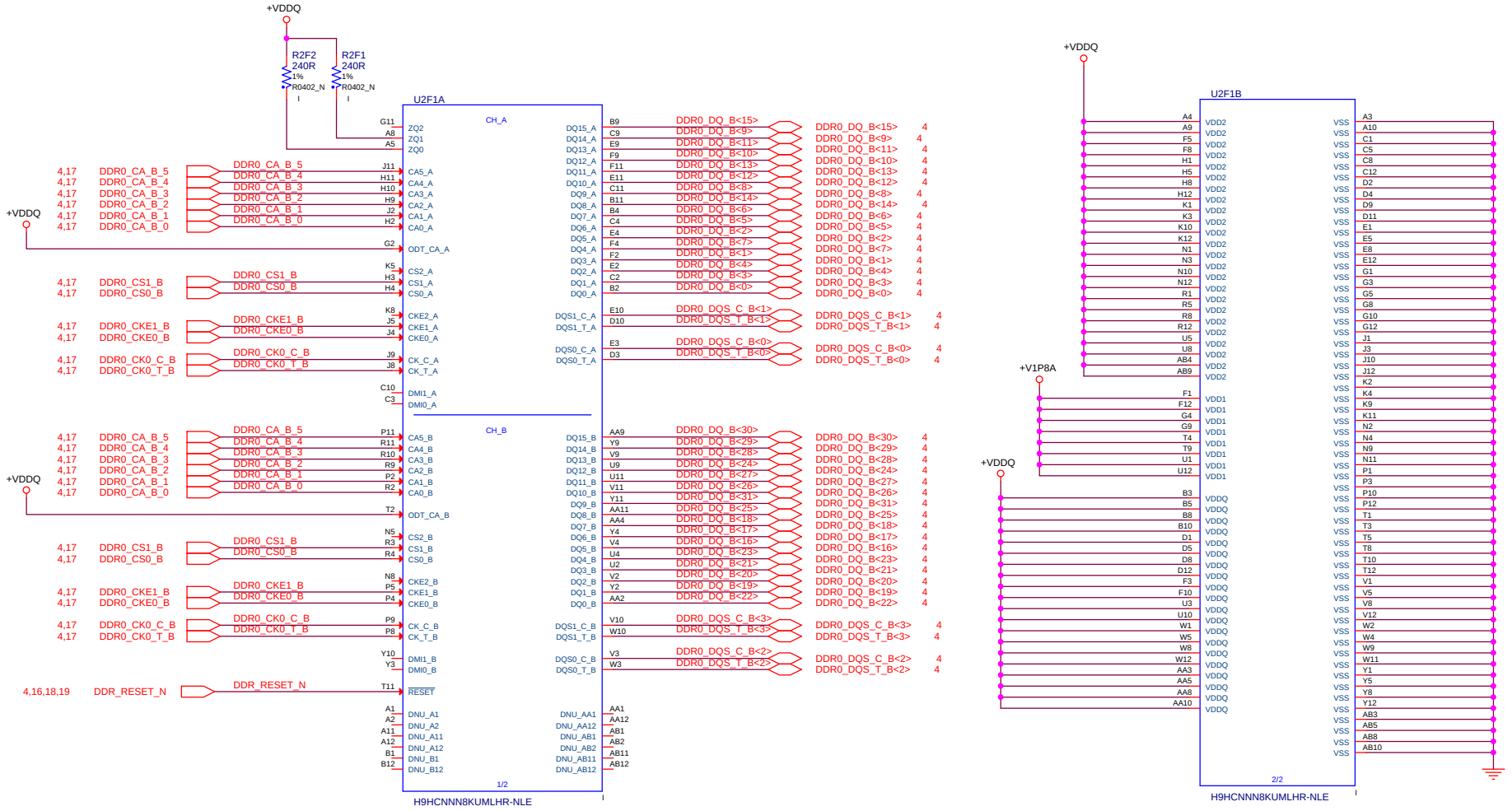


BPAGE DRAWING

apl_lf.GND
Fri May 27 06:47:16 2016

3nod三诺	Project:	120S-11&14IAP	
	Engineer:	LUFFY	
Size: Custom	Title:	MEM_LPDDR4 CH0-1 of 2	Rev: V01
Date: Tuesday, March 14, 2017	Sheet	16 of 63	

CHANNEL 0 - MEMORY2/2



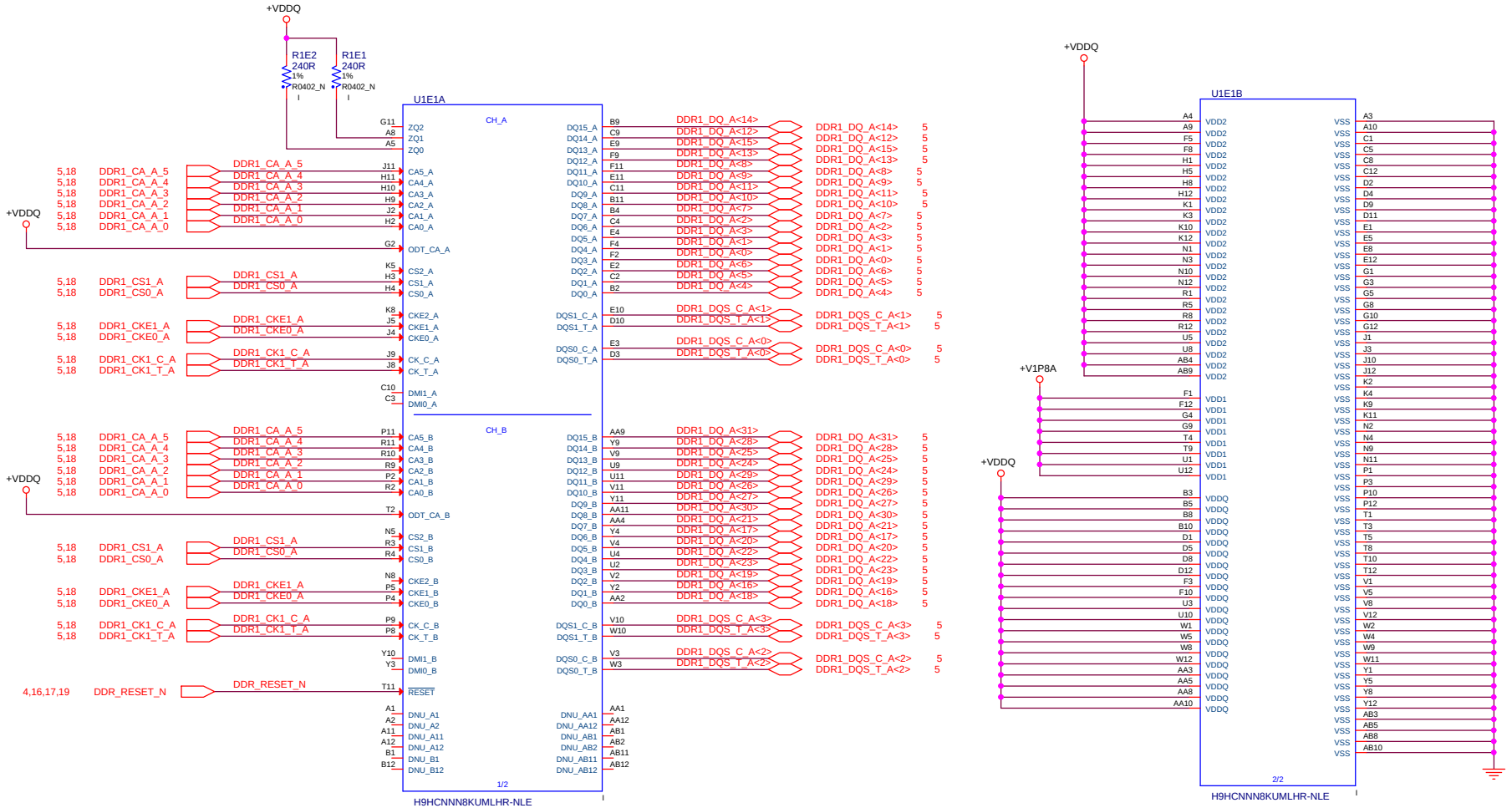
BPAGE DRAWING

apl_ff.GND

Fri May 27 06:47:16 2016

3nod三诺	Project:	120S-11&14IAP	
	Engineer:	LUFFY	
Size: Custom	Title:	MEM_LPDDR4 CH0-2 of 2	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 17 of 63		

CHANNEL 1 - MEMORY1/2



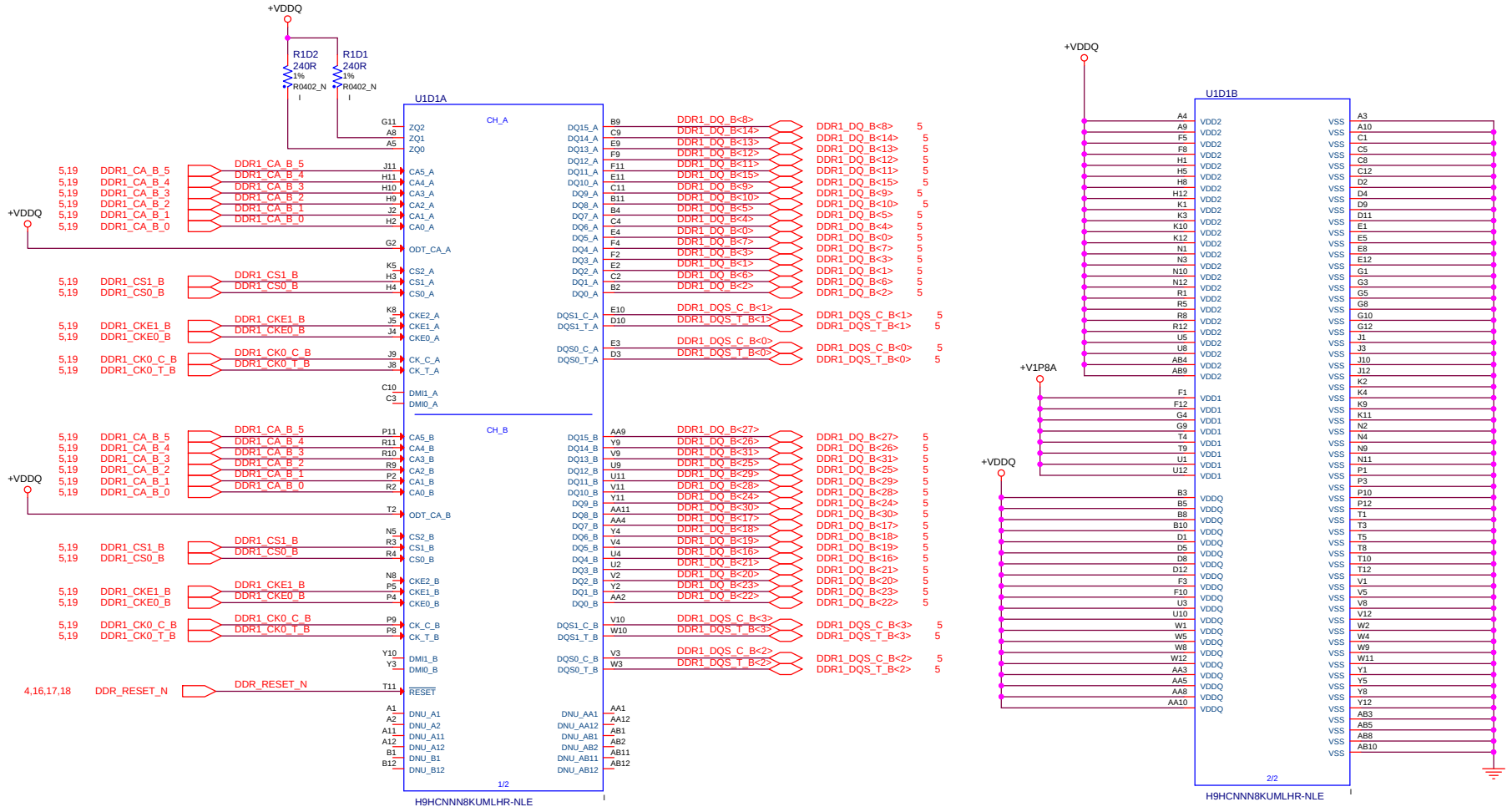
BPAGE DRAWING

apl_ff.GND

Fri May 27 06:47:18 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	MEM_LPDDR4 CH1-1 of 2
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 18 of 63	

CHANNEL 1 - MEMORY2/2



BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:18 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: MEM_LPDDR4 CH1-2of 2	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 19 of 63	

BPAGE DRAWING

apl_ff.+V1P8.18
Fri May 27 06:47:18 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: NC	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 20 of 63	

BPAGE DRAWING

apl_ff.+V1P8.18
Fri May 27 06:47:18 2016

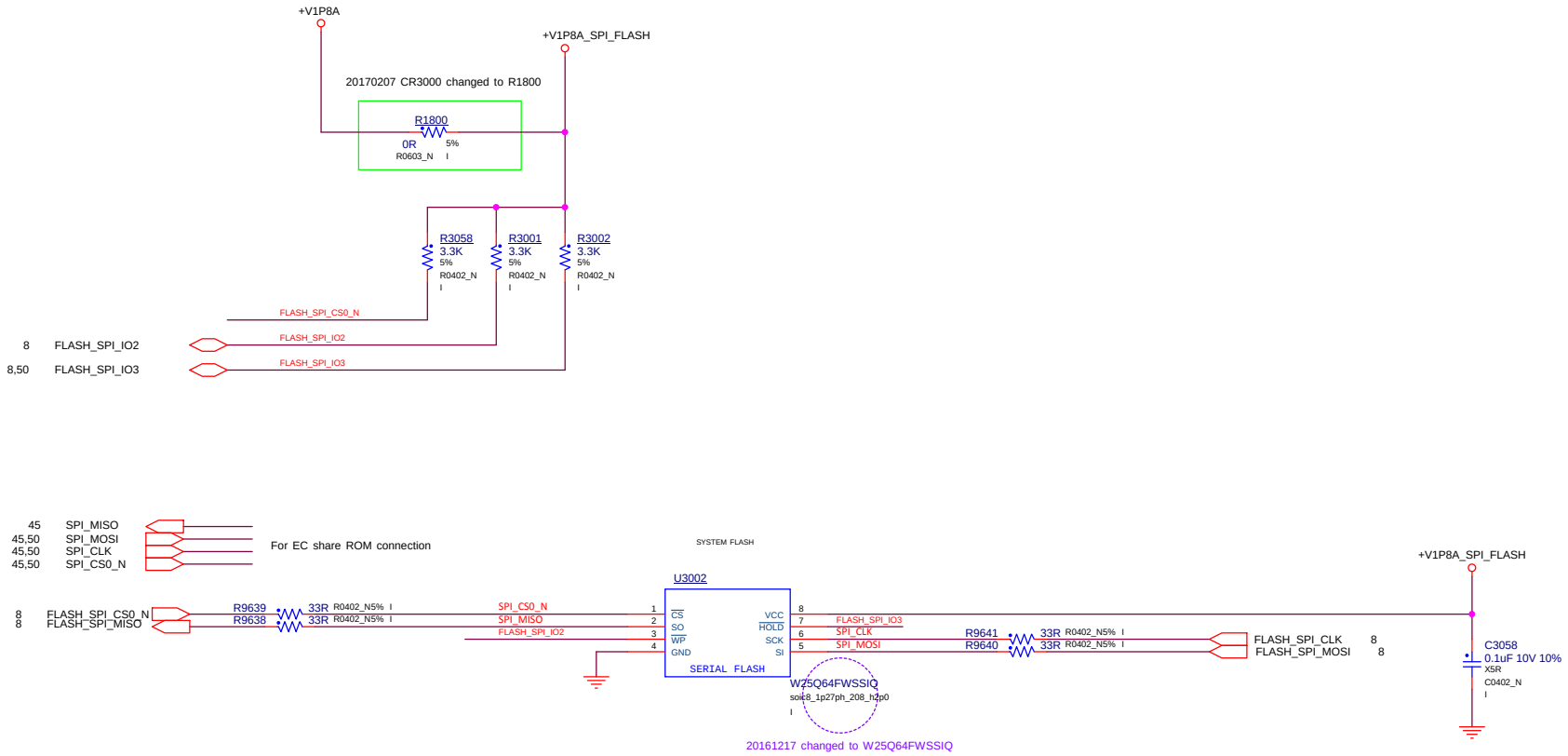
3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: NC	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 21 of 63	

BPAGE DRAWING

apl_ff.8A

Fri May 27 06:47:18 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: MEM_LPDDR4-DECAPS	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 22 of 63	



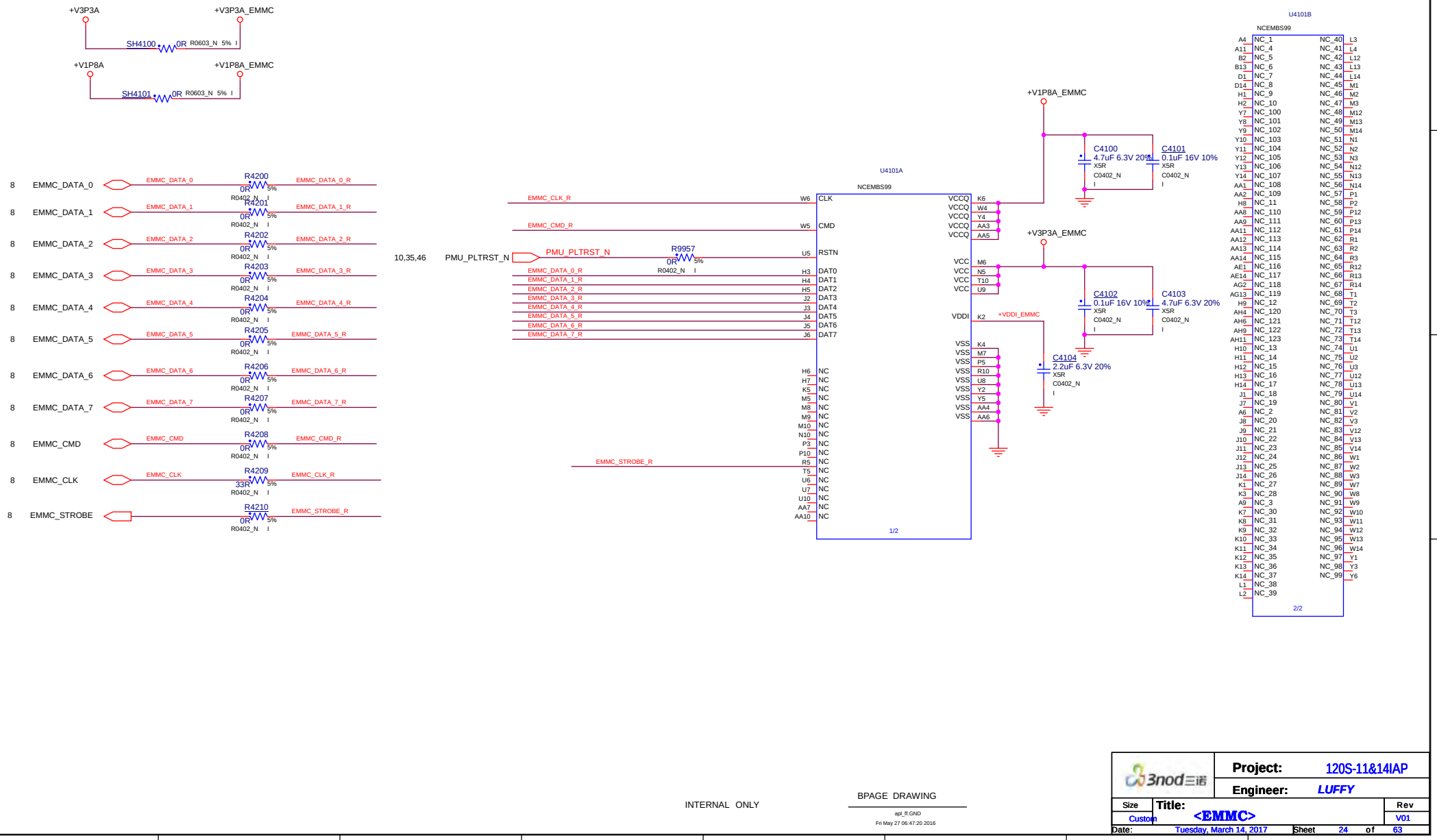
INTERNAL ONLY

BPAGE DRAWING

apl_ff.GND

Fri May 27 06:47:20 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <SYSTEM_FLASH>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 23 of 63	



3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <EMMC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 24 of 63	

INTERNAL ONLY

BPAGE DRAWING

apl_ff.s
Fri May 27 06:47:20 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 25 of 63	

SENSORS

+V3P3A — 1 — 2 — +V3P3A_SENSOR

NOBOM
JUMP_43X39
JUMP
SH8000

+V3.3AL — 1 — 2 — +V3.3AL_LID

NOBOM
JUMP_43X39
JUMP
SH9507

20170316 Added

CPU THERMAL SENSOR

+V3P3A_SENSOR
C2829
0.1uF 16V 10%
X7R
C0402

U2800
VCC, SCLK, DXP, SDATA, DXN, ALERT#, THERM#, GND
G788P81U
MSOP8_PH0P65_3X3_H1P1

+V3P3A_SENSOR
C2830 2200pF 50V 10% C0402 X7R
R2807 10.5K 1% R0402

H_THERMDA
H_THERMDC
CPU_THERM#

SML1_CLK
SML1_DATA
THERMAL_ALERT#

SML1_CLK 45
SML1_DATA 45
THERMAL_ALERT# 45

R2808 7.5K 1% R0402_N +V3P3A_SENSOR

+V3P3A_SHUTDOWN# +V3P3A_SHUTDOWN# 55
Q9526 2N7002 250mA 60V sot_23_dgs
R9993 330K 5% R0402_N PCH_PWROK 10,45
Q9527 2N7002 250mA 60V sot_23_dgs
THERMAL_ALERT#

20161220 :Added

Q2800
MMBT3904 200mA 40V
sot_23

Table 10. Remote temperature $\overline{\text{THERM}}$ limit

The default value is trapping after power up 100ms by different pull-up resistors of $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$ pin:

TEMPERATURE (°C)		$\overline{\text{THERM}}$				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

LID SENSOR

+V3.3AL_LID 20170316 Modified
LEVEL SHIFTER FOR SOC CONN TBD

R5556 20K 5% R0402_N
LID_INT_N
LID_INT_N 45
C2699 100pF 50V 5% NPO C0402_N

+V3.3AL_LID 20170316 Modified
C9698 0.1uF 16V 10% X5R C0402_N
U9505 VDD GND VOUT
LID_INT_N
APX8132Ha1 SOT23_3L_M

INTERNAL ONLY

BPAGE DRAWING
apl_ff.GND
Fri May 27 06:47:20 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <SENSORS>	Rev: V01
Date: Thursday, March 16, 2017	Sheet 26 of 63	

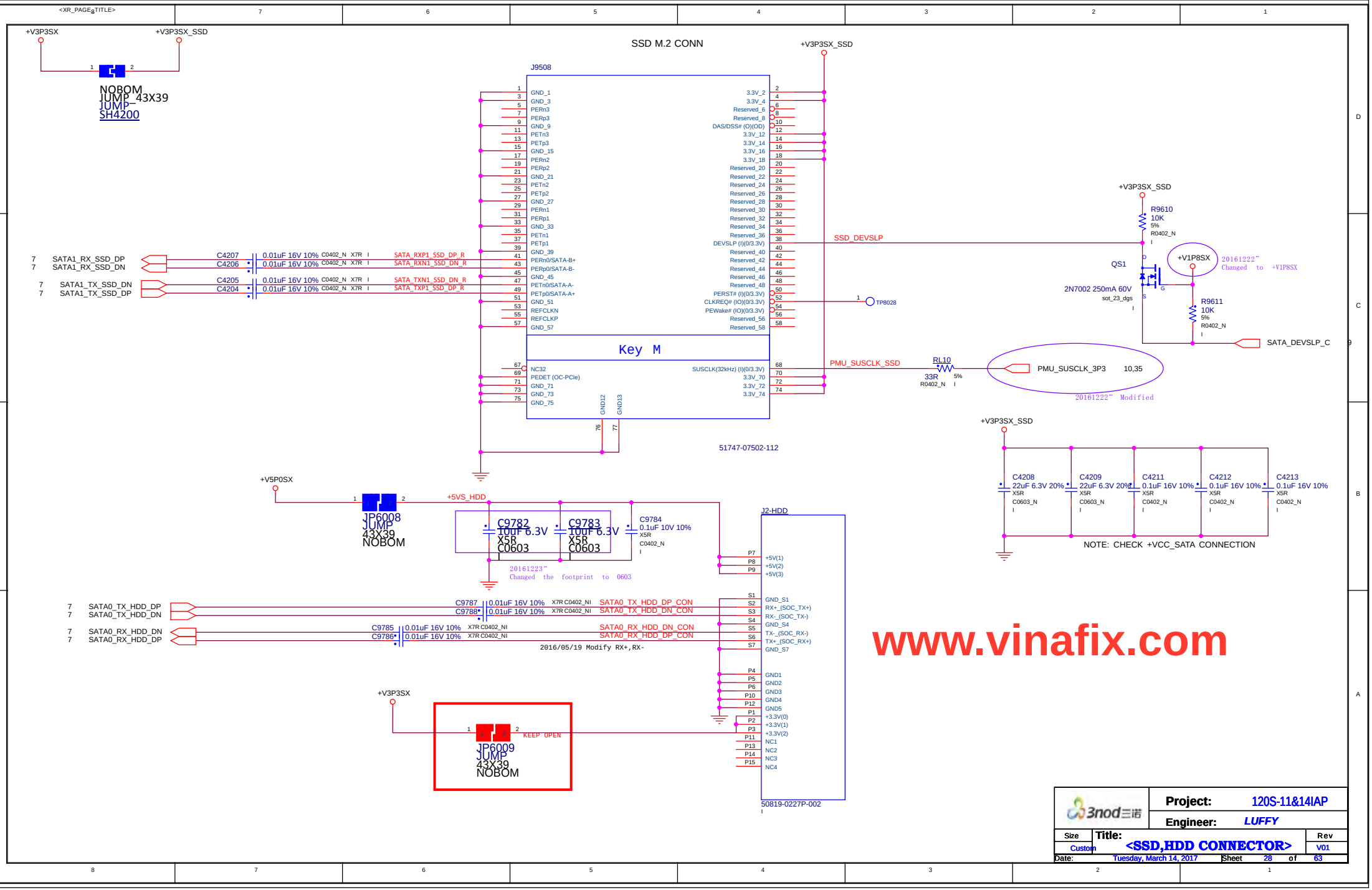
INTERNAL ONLY

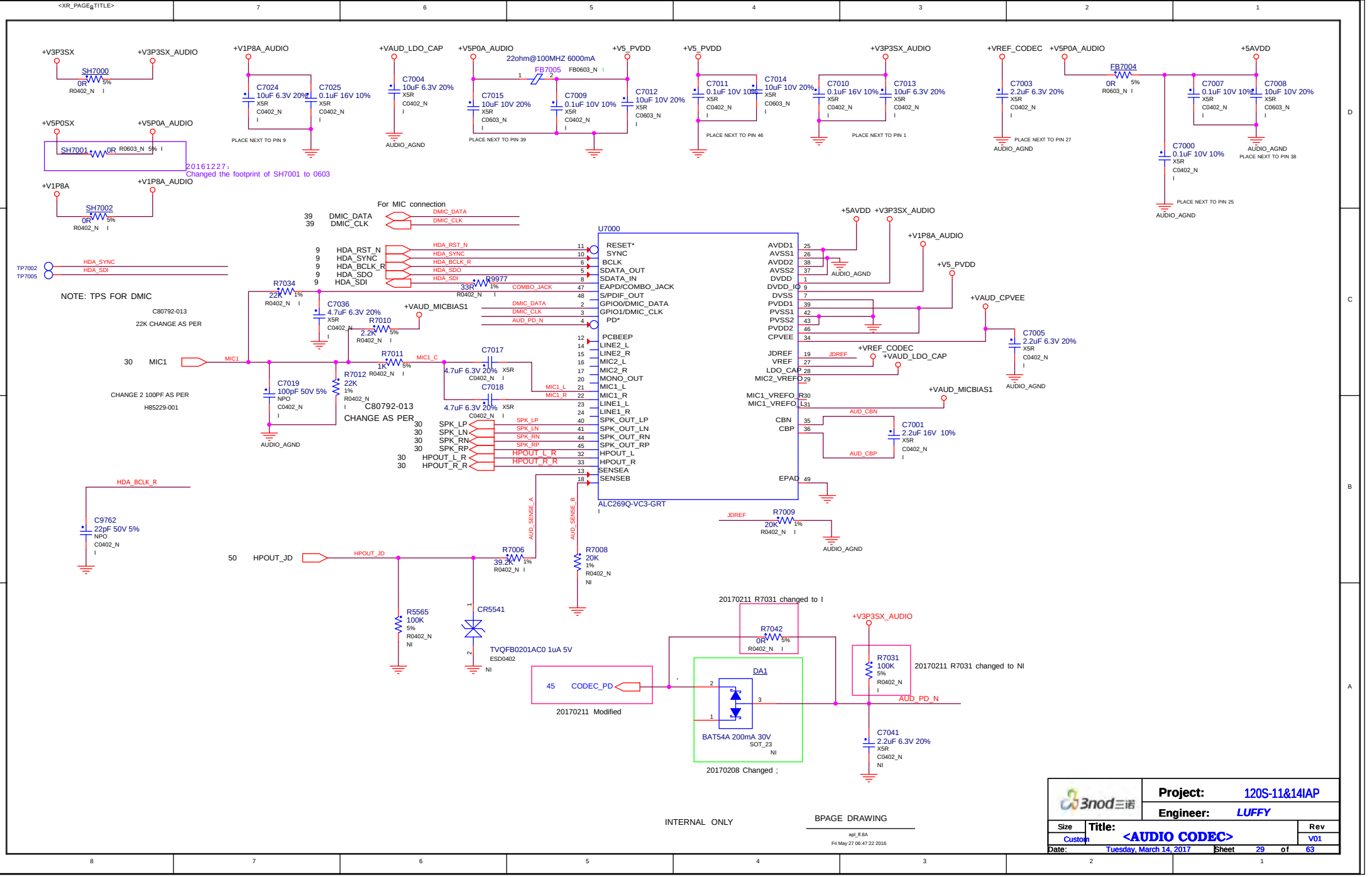
BPAGE DRAWING

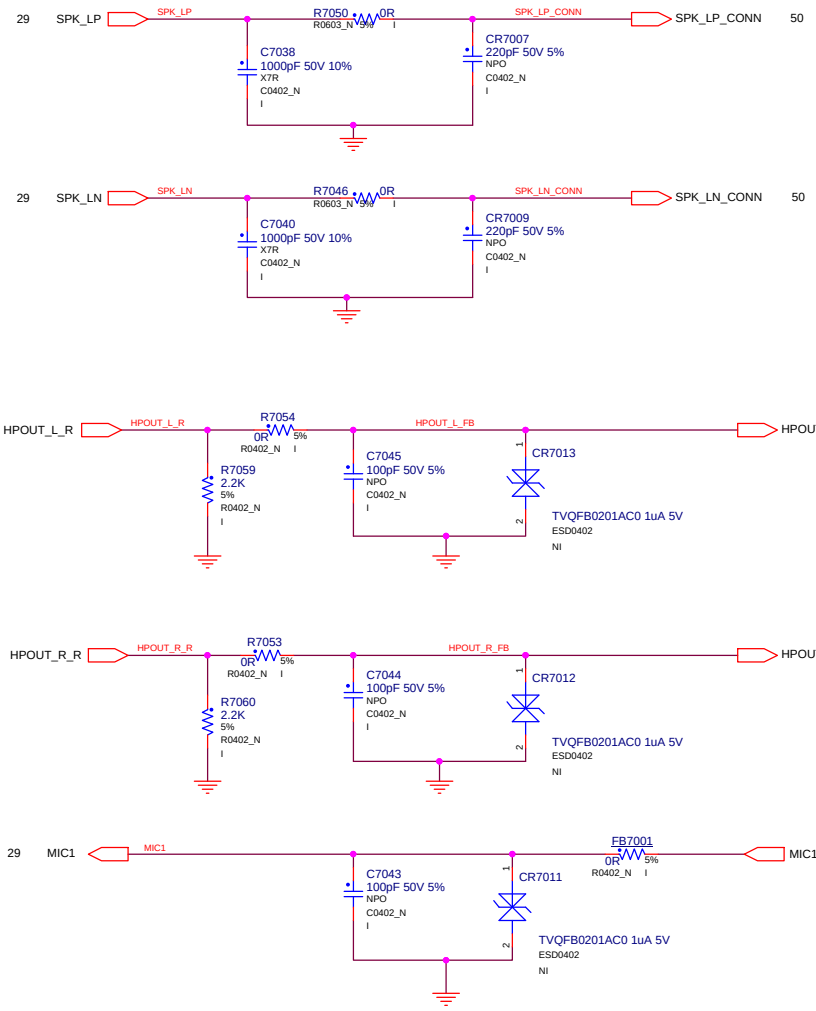
apl_ff.

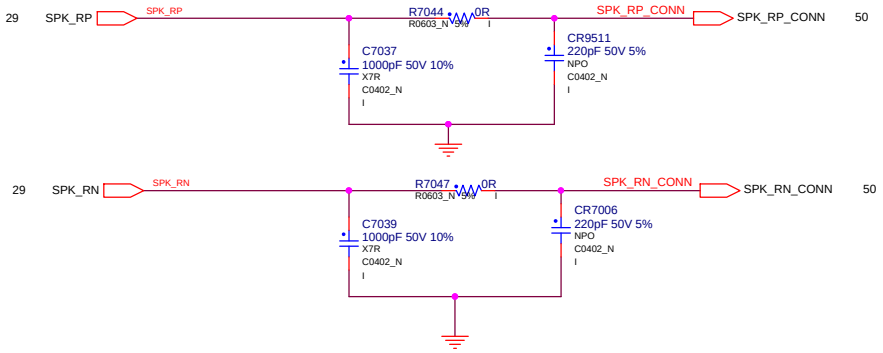
Fri May 27 06:47:22 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 27 of 63	


SSD M.2 CONN
J9508
Key M
51747-07502-112
+V3P3SX
+V3P3SX_SSD
NOBOM
JUMP_43X39
JUMP~
SH4200
SSD_DEVSLP
TP8028
R9610
10K
R0402_N
QS1
2N7002 250mA 60V
sot_23_dgs
+V1P8SX
20161222~
Changed to +V1P8SX
R9611
10K
SATA_DEVSLP_C
PMU_SUSCLK_SSD
RL10
33R
PMU_SUSCLK_3P3 10,35
20161222~ Modified
C4208 22uF 6.3V 20%
C4209 22uF 6.3V 20%
C4211 0.1uF 16V 10%
C4212 0.1uF 16V 10%
C4213 0.1uF 16V 10%
NOTE: CHECK +VCC_SATA CONNECTION
+V5P0SX
+5VS_HDD
JP6008
JUMP
43X39
NOBOM
C9782 10uF 6.3V X5R C0603
C9783 10uF 6.3V X5R C0603
C9784 0.1uF 10V 10%
20161223~
Changed the footprint to 0603
J2-HDD
SATA1_RX_SSD_DP
SATA1_RX_SSD_DN
SATA1_TX_SSD_DN
SATA1_TX_SSD_DP
C4207 0.01uF 16V 10%
C4206 0.01uF 16V 10%
C4205 0.01uF 16V 10%
C4204 0.01uF 16V 10%
SATA_RXP1_SSD_DP_R
SATA_RXN1_SSD_DN_R
SATA_TXN1_SSD_DN_R
SATA_TXP1_SSD_DP_R
SATA0_TX_HDD_DP
SATA0_TX_HDD_DN
SATA0_RX_HDD_DN
SATA0_RX_HDD_DP
C9787 0.01uF 16V 10%
C9788 0.01uF 16V 10%
C9785 0.01uF 16V 10%
C9786 0.01uF 16V 10%
SATA0_TX_HDD_DP_CON
SATA0_TX_HDD_DN_CON
SATA0_RX_HDD_DN_CON
SATA0_RX_HDD_DP_CON
2016/05/19 Modify RX+,RX-
+V3P3SX
JP6009
JUMP
43X39
NOBOM
KEEP OPEN
50819-0227P-002
www.vinafix.com
Project: 120S-11&14IAP
Engineer: LUFFY
Size: Custom
Title: <SSD,HDD CONNECTOR>
Rev: V01
Date: Tuesday, March 14, 2017
Sheet 28 of 63


+V3P3SX
+V3P3SX_AUDIO
SH7000
0R
R0402_N
+V1P8A_AUDIO
C7024
10uF 6.3V 20%
X5R
C0402_N
C7025
0.1uF 16V 10%
PLACE NEXT TO PIN 9
+VAUD_LDO_CAP
C7004
10uF 6.3V 20%
AUDIO_AGND
+V5P0A_AUDIO
22ohm@100MHZ 6000mA
FB7005
FB0603_N
C7015
10uF 10V 20%
C0603_N
C7009
0.1uF 10V 10%
PLACE NEXT TO PIN 39
+V5_PVDD
C7012
10uF 10V 20%
C7011
0.1uF 10V 10%
PLACE NEXT TO PIN 46
C7014
10uF 10V 20%
C7010
0.1uF 16V 10%
PLACE NEXT TO PIN 1
C7013
10uF 6.3V 20%
+VREF_CODEC
C7003
2.2uF 6.3V 20%
PLACE NEXT TO PIN 27
FB7004
+5AVDD
C7007
0.1uF 10V 10%
C7008
10uF 10V 20%
C7000
0.1uF 10V 10%
PLACE NEXT TO PIN 25
PLACE NEXT TO PIN 38
+V5P0SX
SH7001
R0603_N
20161227:
Changed the footprint of SH7001 to 0603
+V1P8A
SH7002
For MIC connection
DMIC_DATA
DMIC_CLK
U7000
RESET*
SYNC
BCLK
SDATA_OUT
SDATA_IN
EAPD/COMBO_JACK
S/PDIF_OUT
GPIO0/DMIC_DATA
GPIO1/DMIC_CLK
PD*
PCBEEP
LINE2_L
LINE2_R
MIC2_L
MIC2_R
MONO_OUT
MIC1_L
MIC1_R
LINE1_L
LINE1_R
SPK_OUT_LP
SPK_OUT_LN
SPK_OUT_RN
SPK_OUT_RP
HPOUT_L
HPOUT_R
SENSEA
SENSEB
ALC269Q-VC3-GRT
AVDD1
AVSS1
AVDD2
AVSS2
DVDD
DVDD_IO
DVSS
PVDD1
PVSS1
PVSS2
PVDD2
CPVEE
JDREF
VREF
LDO_CAP
MIC2_VREFO
MIC1_VREFO_R
MIC1_VREFO_L
CBN
CBP
EPAD
HDA_RST_N
HDA_SYNC
HDA_BCLK_R
HDA_SDO
HDA_SDI
R9977
33R
COMBO_JACK
TP7002
TP7005
NOTE: TPS FOR DMIC
C80792-013
22K CHANGE AS PER
R7034
22K
C7036
4.7uF 6.3V 20%
+VAUD_MICBIAS1
R7010
2.2K
MIC1
R7011
1K
MIC1_C
C7017
4.7uF 6.3V 20%
C7019
100pF 50V 5%
NPO
R7012
22K
CHANGE 2 100PF AS PER
H85229-001
C80792-013
CHANGE AS PER
C7018
SPK_LP
SPK_LN
SPK_RN
SPK_RP
HPOUT_L_R
HPOUT_R_R
AUDIO_AGND
+5AVDD
+V3P3SX_AUDIO
+V1P8A_AUDIO
+V5_PVDD
+VAUD_CPVEE
C7005
2.2uF 6.3V 20%
+VREF_CODEC
+VAUD_LDO_CAP
+VAUD_MICBIAS1
AUD_CBN
AUD_CBP
C7001
2.2uF 16V 10%
JDREF
R7009
20K
C9762
22pF 50V 5%
HPOUT_JD
R7006
39.2K
R7008
20K
AUD_SENSE_A
AUD_SENSE_B
R5565
100K
CR5541
TVQFB0201AC0 1uA 5V
ESD0402
20170211 R7031 changed to I
R7042
0R
R7031
100K
20170211 R7031 changed to NI
CODEC_PD
20170211 Modified
DA1
BAT54A 200mA 30V
SOT_23
AUD_PD_N
C7041
2.2uF 6.3V 20%
20170208 Changed ;
INTERNAL ONLY
BPAGE DRAWING
Project: 120S-11&14IAP
Engineer: LUFFY
Size: Custom
Title: <AUDIO CODEC>
Rev: V01
Date: Tuesday, March 14, 2017
Sheet 29 of 63



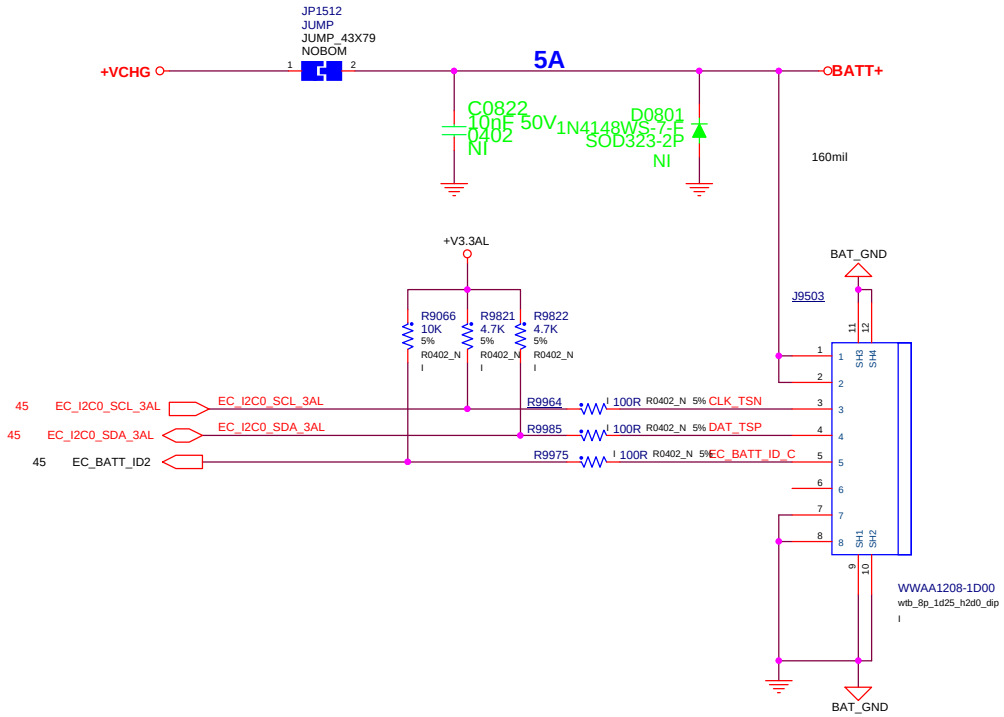


INTERNAL ONLY

BPAGE DRAWING

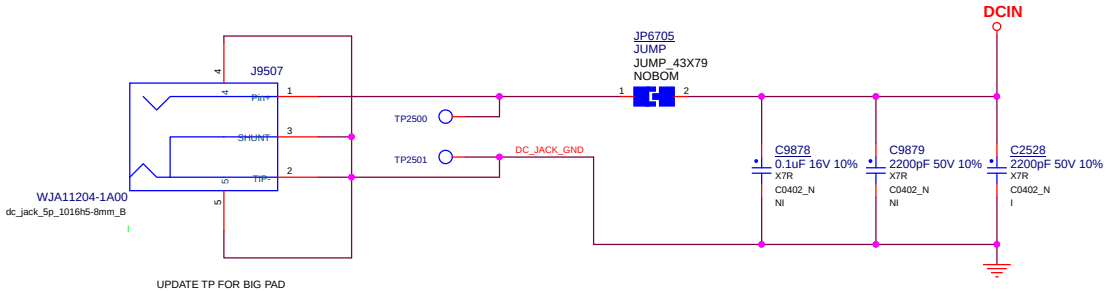
apl_ll.8A
Fri May 27 06:47:24 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <AUDIO_HEADSET AND SPEAKERS>	Rev
Date: Tuesday, March 14, 2017	Sheet 30 of 63	



20170205 Deleted reserved design for dummy battery

3nod三诺	Project:	120S-11&14IAP
	Engineer:	GGS
Size: Custom	Title:	<GAUGE&BATTERY CONN>
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 31 of 63	



UPDATE TP FOR BIG PAD

INTERNAL ONLY

BPAGE DRAWING

apl_ff.ADP_P.48
Fri May 27 06:47:24 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	GGS
Size: Custom	Title: <DC JACK>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 32 of 63	

INTERNAL ONLY

BPAGE DRAWING

apl_ff.8A

Fri May 27 06:47:24 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 33 of 63	

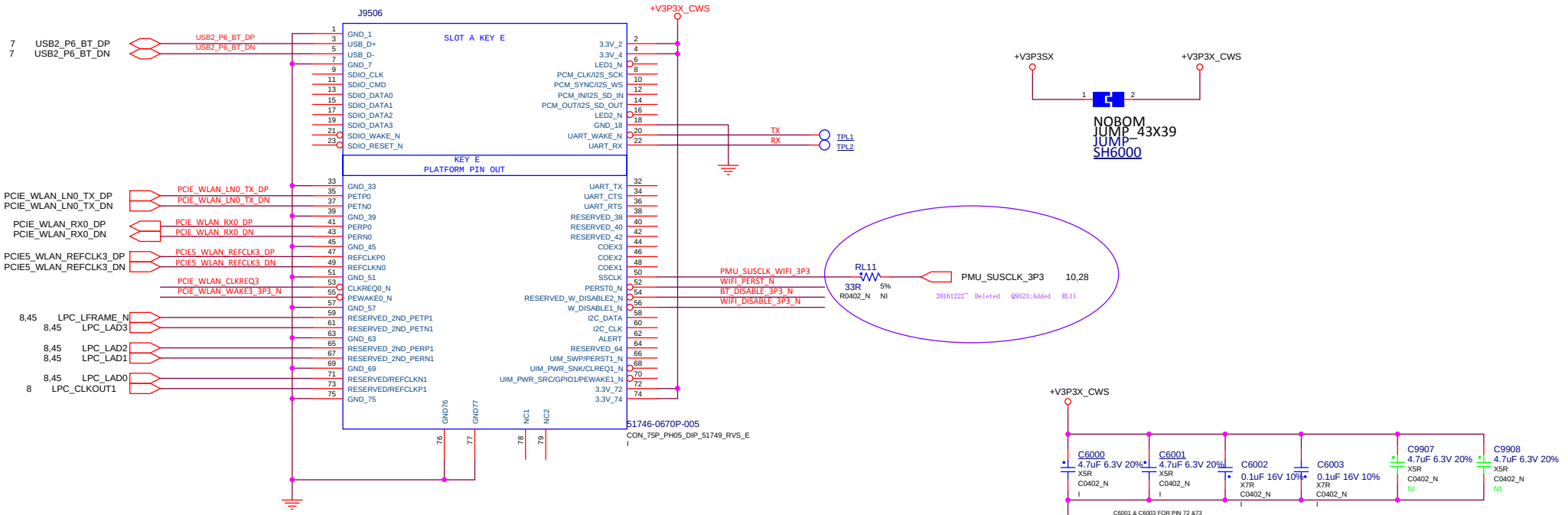
INTERNAL ONLY

BPAGE DRAWING

apl_ff.
Fri May 27 06:47:24 2016

TYPE-C PD CONTROLLER

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 34 of 63	



3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	<WIFI/BT M.2 CONN>
	Rev	V01
Date: Saturday, March 25, 2017	Sheet 35 of 63	

<XR_PAGE_TITLE>

+V5P0A_TYPEC_VIN

C9769 X5R C0603_N I — 10uF 10V 20%

C9768 X5R C0402_N I — 0.1uF 10V 10%

R9738 1K 5% R0402_N NI

CC_LINK

R9737 510K 5% R0402_N I

CC_LINK_R

C9770 2.2uF 16V 10% X5R C0603_N I

45 EC_ACDET

R9809 1K 5% R0402_N I

1.5A~3A/Stack Port

+VBUS_TYPEC

R9739 1K 5% R0402_N NI

20170314 Added C9901/C9903;C9772 changed to NI

C9771 22uF 6.3V 20% X5R C0603_N I

C9901 22uF 6.3V 20% X5R C0603_N I

C9903 22uF 6.3V 20% X5R C0603_N I

C9772 150uF 6.3V 20% CAP_3528_H1P9 NI

U9509 G517AL1TB1U I

IN OUT FLAG GND SET EN

USB_OC0_N 7

R9808 24K 1% R0402_N I

R9806 18K 1% R0402_N I

Q9508 2N7002W-7-F 115mA 60V sot_323_dgs I

DC ONLY : OCP SET TO 1.5A
AC IN: OCP SET TO 3A

TYPE_C_3P3V

C9764 0.1uF 10V 10% X5R C0402_N I

R9725 5.1K 1% R0402_N I

U9025 EJ179V

CU_MODE_0 CC2_Z_MODE HIGH_CURRENT MIDD_CURRENT CC_LINK EN_VCONN WHICH_LINK CC1

SR0_IN ZCC2_IN HC_EN MC_EN CC_EN VCONN_EN DIR_SET CC1_IN

EP SR1_IN ZCC1_IN REXT V33B TXN_1 TXP_1 TXN_0 TXP_0

VSSA1 TXP TXN VSSA2 V33A RXP RXN VSSA3

VSSA4 CC2_IN VCONN V33C RXN_1 RXP_1 RXN_0 RXP_0

SSTX2- SSTX2+ SSTX1- SSTX1+

TPL4 TPL5 TPL6 TPL7

C9765 0.1uF 10V 10% C0402_N I — USB3_P0_TYPEC_TX_DP 7

C9766 0.1uF 10V 10% C0402_N I — USB3_P0_TYPEC_TX_DN 7

USB3_P0_TYPEC_RX_DP 7

USB3_P0_TYPEC_RX_DN 7

C9767 0.1uF 10V 10% X5R C0402_N I

C9763 0.1uF 10V 10% X5R C0402_N I

TPL3

+V3P3A

R9724 0R 5% R0402_N I

+V5CP

+V5P0A_TYPEC_VIN

SH4570 JUMP JUMP_43X79 NOBOM

+V5P0A_TYPEC_VIN

R9723 0R 5% R0603_N I — VCONN

VCONN Disable(Default)
Reserved C9812 for VCONN enable

C9812 10uF 10V 20% X5R C0603_N NI

R9736 10K 5% R0402_N I — CU_MODE_0

R9718 10K 5% R0402_N I — CU_MODE_1

R9719 10K 5% R0402_N I — EN_VCONN

R9720 10K 5% R0402_N NI

R9721 10K 5% R0402_N I — CC1_Z_MODE

R9722 10K 5% R0402_N I — CC2_Z_MODE

20170314 Choke changed to NI;Resistor changed to I;

R9726 0R 5% R0402_N I

L9510 67ohm 320mA +-25% CO-CH_L4_PH0P8_H1_AB

SSTX2- A1 — SSTX2-_CONN

SSTX2+ B1 — SSTX2+_CONN

R9727 0R 5% R0402_N I NI

R9728 0R 5% R0402_N I

L9511 67ohm 320mA +-25% CO-CH_L4_PH0P8_H1_AB

SSTX1- A1 — SSTX1-_CONN

SSTX1+ B1 — SSTX1+_CONN

R9729 0R 5% R0402_N I NI

R9730 0R 5% R0402_N I

L9512 67ohm 320mA +-25% CO-CH_L4_PH0P8_H1_AB

SSRX2- A2 — SSRX2-_CONN

SSRX2+ B2 — SSRX2+_CONN

R9731 0R 5% R0402_N I NI

R9732 0R 5% R0402_N I

L9513 67ohm 320mA +-25% CO-CH_L4_PH0P8_H1_AB

SSRX1- A2 — SSRX1-_CONN

SSRX1+ B2 — SSRX1+_CONN

R9733 0R 5% R0402_N I NI

R9734 0R 5% R0402_N I

L9514 67ohm 320mA +-25% CO-CH_L4_PH0P8_H1_AB

7 USB2_P0_DN — DM_CON

7 USB2_P0_DP — DP_CON

R9735 0R 5% R0402_N I NI

SSRX2-_CONN SSRX2+_CONN SSRX1+_CONN SSRX1-_CONN

CR9514 NC NC NC NC I/O1 I/O2 I/O3 I/O4 GND GND

ESD5344D DFN10_PH0P5_ESD I

SSTX2+_CONN SSTX2-_CONN SSTX1-_CONN SSTX1+_CONN

CR9515 NC NC NC NC I/O1 I/O2 I/O3 I/O4 GND GND

ESD5344D DFN10_PH0P5_ESD I

CC2 CC1 DM_CON DP_CON

CR9519 NC NC NC NC I/O1 I/O2 I/O3 I/O4 GND GND

ESD5344D DFN10_PH0P5_ESD I

20170213:
CR9512/CR9513/CR9517/CR9518 modified to ESD5344D.

+VBUS_TYPEC

GND_10 GND_9 GND_8 GND_7 GND_6 GND_5

GND_12 GND_11

GND_2 SSRXp2 SSRXn2 VBUS_2 RFU1 Dn1 Dp1 CC1 VBUS_1 SSTXn1 SSTXp1 GND_1

GND_3 SSTXp2 SSTXn2 VBUS_3 CC2 Dp2 Dn2 RFU2 VBUS_4 SSRXn1 SSRXp1 GND_4

SSRX2+_CONN SSRX2-_CONN DM_CON DP_CON CC1 SSTX1-_CONN SSTX1+_CONN

SSTX2+_CONN SSTX2-_CONN CC2 DP_CON DM_CON SSRX1-_CONN SSRX1+_CONN

J9512 55933-0240Y-001 I

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	<TYPE C MUX&CONNECTOR>
		Rev: V01
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HDMI LEVEL SHIFTER

+V1P8A — NOBOM — +V1P8A_HDMI

JUMP_43X39

SH9500

JUMP

6	DDI0_TX0_DP	DDI0_TX0_DP	C9580 0.1uF 10V 10% C0402_N X5R	HDMI_TX2_CMC_DP	
6	DDI0_TX0_DN	DDI0_TX0_DN	C9581 0.1uF 10V 10% C0402_N X5R	HDMI_TX2_CMC_DN	
6	DDI0_TX1_DP	DDI0_TX1_DP	C9582 0.1uF 10V 10% C0402_N X5R	HDMI_TX1_CMC_DP	
6	DDI0_TX1_DN	DDI0_TX1_DN	C9583 0.1uF 10V 10% C0402_N X5R	HDMI_TX1_CMC_DN	
6	DDI0_TX2_DP	DDI0_TX2_DP	C9584 0.1uF 10V 10% C0402_N X5R	HDMI_TX0_CMC_DP	
6	DDI0_TX2_DN	DDI0_TX2_DN	C9585 0.1uF 10V 10% C0402_N X5R	HDMI_TX0_CMC_DN	
6	DDI0_TX3_DP	DDI0_TX3_DP	C9586 0.1uF 10V 10% C0402_N X5R	HDMI_CLK_CMC_DP	
6	DDI0_TX3_DN	DDI0_TX3_DN	C9587 0.1uF 10V 10% C0402_N X5R	HDMI_CLK_CMC_DN	

R9528 0R 5% R0402_N NI

L4S12X20U 90ohm 100mA +-20% — L9508

HDMI_TX2_CMC_DP → HDMI_TX2_CONN_DP → HDMI_TX2_CONN_DP 38

HDMI_TX2_CMC_DN → HDMI_TX2_CONN_DN → HDMI_TX2_CONN_DN 38

R9529 0R 5% R0402_N

R9530 0R 5% R0402_N NI

L4S12X20U 90ohm 100mA +-20% — L9509

HDMI_TX1_CMC_DP → HDMI_TX1_CONN_DP → HDMI_TX1_CONN_DP 38

HDMI_TX1_CMC_DN → HDMI_TX1_CONN_DN → HDMI_TX1_CONN_DN 38

R9531 0R 5% R0402_N

R9532 0R 5% R0402_N NI

L4S12X20U 90ohm 100mA +-20% — L9506

HDMI_TX0_CMC_DP → HDMI_TX0_CONN_DP → HDMI_TX0_CONN_DP 38

HDMI_TX0_CMC_DN → HDMI_TX0_CONN_DN → HDMI_TX0_CONN_DN 38

R9533 0R 5% R0402_N

R9534 0R 5% R0402_N NI

L4S12X20U 90ohm 100mA +-20% — L9507

HDMI_CLK_CMC_DP → HDMI_CLK_CONN_DP → HDMI_CLK_CONN_DP 38

HDMI_CLK_CMC_DN → HDMI_CLK_CONN_DN → HDMI_CLK_CONN_DN 38

R9535 0R 5% R0402_N

+V5P0SX_HDMI — CR9500 BAT54A 200mA 30V SOT_23

VHDMI_SCL — R9577 2.2K R0402_N 5%

VHDMI_SDA — R9580 2.2K R0402_N 5%

38 HDMI_DDC_SCL — HDMI_DDC_SDA 38

+V1P8A_HDMI — R9579 2.2K R0402_N 5%

+V1P8A_HDMI — R9581 2.2K R0402_N 5%

Q9501 BSS138 300mA 50V sot23_gsd

Q9503 BSS138 300mA 50V sot23_gsd

6 DDI0_DDC_SCL — DDI0_DDC_SCL

6 DDI0_DDC_SDA — DDI0_DDC_SDA

+V1P8A_HDMI — R9578 10K 5% R0402_N

DDI0_HPD_N → DDI0_HPD_N 6

Q9502 2N7002W-7-F 115mA 60V sot_323_dgs

HDMI_HPD → HDMI_HPD 38

R9576 100K 5% R0402_N

HDMI_PLS_FET — Q9504 2N7002W-7-F 115mA 60V sot_323_dgs

40,45 EC_SLP_SX — R9682 100K 5% R0402_N

FET HAS BEEN CHANGED PLEASE REVIEW

HDMI_TX2_CMC_DP / HDMI_TX2_CMC_DN

HDMI_TX1_CMC_DP / HDMI_TX1_CMC_DN

HDMI_TX0_CMC_DP / HDMI_TX0_CMC_DN

HDMI_CLK_CMC_DP / HDMI_CLK_CMC_DN

20161228:
Changed from 680R to 470R

R9520 470R 1% R0402_N — R9521 470R 1% R0402_N

R9522 470R 1% R0402_N — R9523 470R 1% R0402_N

R9524 470R 1% R0402_N — R9525 470R 1% R0402_N

R9526 470R 1% R0402_N — R9527 470R 1% R0402_N

HDMI_PLS_FET

BPAGE DRAWING

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Fri May 27 06:47:26 2016

3nod三诺	Project:	120S-11&14IAP	
	Engineer:	LUFFY	
Size: Custom	Title:	<HDMI LEVEL SHIFTER>	Rev: V01
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HDMI CONNECTOR

+V5P0SX — R9848 0R 5% R0603_N I — +V5P0SX_HDMI

J9500 — W-00-6229-1900A — CON_HDMI_19P_1001050-03111 I

Pin	Signal	Net
1	D2+	37 HDMI_TX2_CONN_DP
2	D2 Shield	
3	D2-	37 HDMI_TX2_CONN_DN
4	D1+	37 HDMI_TX1_CONN_DP
5	D1 Shield	
6	D1-	37 HDMI_TX1_CONN_DN
7	D0+	37 HDMI_TX0_CONN_DP
8	D0 Shield	
9	D0-	37 HDMI_TX0_CONN_DN
10	CK+	37 HDMI_CLK_CONN_DP
11	CK Shield	
12	CK-	37 HDMI_CLK_CONN_DN
13	CE Remote	
14	NC	
15	DDC CLK	37 HDMI_DDC_SCL
16	DDC DATA	37 HDMI_DDC_SDA
17	GND	
18	+5V	
19	HP DET	37 HDMI_HPD — R9877 0R 5% R0402_N I — HDMI_HPD_N
20	SHELL1	
21	SHELL2	
22	SHELL3	
23	SHELL4	

+V5P0SX_HDMI

CR9508 TVQFB0201AC0 1uA 5V ESD0402 NI

C9610 2.2uF 16V 10% X5R C0402_N I

C9880 10nF 50V 10% X7R C0402_N NI

C9881 10nF 50V 10% X7R C0402_N NI

C9813 1uF 25V 10% X5R C0603_N I

20170314 CR9505/CR9506 changed to NI

CR9506: HDMI_TX0_CONN_DP, HDMI_TX0_CONN_DN, HDMI_CLK_CONN_DN, HDMI_CLK_CONN_DP

CR9505: HDMI_TX1_CONN_DN, HDMI_TX1_CONN_DP, HDMI_TX2_CONN_DP, HDMI_TX2_CONN_DN

ESD5344D DFN10_PH0P5_ESD NI

HDMI_HPD_N — CR9502 AZ5725-01F.R7GR 1uA 5V ESD0402 I

HDMI_DDC_SCL — CR9503 AZ5725-01F.R7GR 1uA 5V ESD0402 I

HDMI_DDC_SDA — CR9504 AZ5725-01F.R7GR 1uA 5V ESD0402 I

BPAGE DRAWING

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Fri May 27 06:47:28 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	<HDMI CONN>
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EDP AC CAPS

EDP_TX1_SOC_DN — C8214 0.1uF 16V 10% X7R C0402_N — EDP_TX1_C_DN — L8200 — EDP_TX1_CONN_DN
EDP_TX1_SOC_DP — C8213 0.1uF 16V 10% X7R C0402_N — EDP_TX1_C_DP — L8200 — EDP_TX1_CONN_DP
R8203 0R 5% R0402_N NI
R8200 0R 5% R0402_N I
L4S12X20U 90ohm 100mA +-20%

EDP_TX0_SOC_DN — C8216 0.1uF 16V 10% X7R C0402_N — EDP_TX0_C_DN — L8201 — EDP_TX0_CONN_DN
EDP_TX0_SOC_DP — C8215 0.1uF 16V 10% X7R C0402_N — EDP_TX0_C_DP — L8201 — EDP_TX0_CONN_DP
R8201 0R 5% R0402_N NI
R8202 0R 5% R0402_N I
L4S12X20U 90ohm 100mA +-20%

EDP_AUX_SOC_DP — C8217 0.1uF 16V 10% X7R C0402_N — EDP_AUX_C_DP — L8205 — EDP_AUX_CONN_DP
EDP_AUX_SOC_DN — C8218 0.1uF 16V 10% X7R C0402_N — EDP_AUX_C_DN — L8205 — EDP_AUX_CONN_DN
R8218 0R 5% R0402_N NI
R8219 0R 5% R0402_N I
L4S12X20U 90ohm 100mA +-20%

+V3P3SX — R9979 100K 5% R0402_N I — EDP_AUX_CONN_DP
+V3P3SX — R9980 100K 5% R0402_N I — EDP_AUX_CONN_DN

+V1P8SX
+V3P3SX
20170210 changed

C9736 0.1uF 10V 10% X5R C0402_N I
C9735 0.1uF 10V 10% X5R C0402_N I

+V3P3SX — R9813 0R 5% R0603_N I
+V3P3A_CAM
C9734 1uF 10V 10% X5R C0402_N I
C9733 0.1uF 10V 10% X5R C0402_N I

U9508 FA8201OTR dfn14p_ph0p4_3x2_h0p8 I

6 EDP_BKLT_PWM
6 EDP_BKLT_EN
6 EDP_VDD_EN

EDP_BKLT_PWM_3P3
EDP_BKLT_EN_1
EDP_VDD_EN_3P3
R18 2.2K 5% R0402_N I
EDP_BKLT_EN_3P3

20170210 U9507 changed from G2129AE1U to FA8201OTR

+V3P3A
+V3P3_DISPLAY +V3P3_DISPLAY_CONN
NOBOM JUMP_43X39 SH8201 JUMP
C8207 22uF 6.3V 20% X5R C0603_N I
C9894 1uF 10V 10% X5R C0402_N NI
U8201 APL3512ABI-TRG SOT23_5 I
VIN VOUT EN GND SS
EDP_VDD_EN_3P3
TP8037
R8226 100K 5% R0402_N I
C9893 0.01uF 25V 10% X7R C0402_N NI

20170207 U8201 changed from WS4601E-5/TR to APL3512ABI-TRG

+VSYS
NOBOM JUMP_43X39 SH8203
C9909 10uF 25V 10% X5R C0805_N NI

SH9508 0R R0603_N 5% NI
+VBATA_BKLT_IN
Q8201 DMP3160L-7 -2.7A -30V sot23_gsd I
R8230 220K 5% R0402_N I
C8220 0.01uF 25V 10% X7R C0402_N I
C9882 0.1uF 25V 10% X5R C0402_N I
R8231 80.6K 1% R0402_N I

20170314 Added R1900
EDP_VDD_EN_3P3 — R1900 0R 5% R0402_N I — Q8200 2N7002KW 115mA 60V sot_323_dgs
R8238 100K 5% R0402_N I

20170205:
Changed from EDP_BKLT_EN to EDP_VDD_EN_3P3

+V1P8A
R8238 10K 5% R0402_N I
EDP_HPD_LS — EDP_HPD_LS 10
Q9505 2N7002W-7-F 115mA 60V sot_323_dgs I
EDP_HPD
R8237 100K 5% R0402_N I

ADD BL_EN_EC FOR CONTROL BL 20170115
BL_EN_EC — D5903 BAT54C 200mA 30V SOT_23
20170205 Added for reserve
R1700 0R 5% R0402_N NI EDP_VDD_EN_3P3

+VBATA_BKLT_IN
J9502 50406-04071-001 I
EDP_BKLT_PWM_3P3
EDP_BKLT_EN_3P3
DMIC_CLK_L
DMIC_DATA_L
MIC_POWER
EDP_HPD
EDP_AUX_CONN_DN
EDP_AUX_CONN_DP
EDP_TX0_CONN_DP
EDP_TX0_CONN_DN
EDP_TX1_CONN_DP
EDP_TX1_CONN_DN
USB2_P7_DN_CONN
USB2_P7_DP_CONN
+V3P3A_CAM
For camera

+V3P3_DISPLAY_CONN
C8200 10uF 6.3V 20% X5R C0402_N I
C8201 1uF 6.3V 10% X5R C0402_N I
R1602 0R 5% R0402_N I

29 DMIC_DATA — DMIC_DATA — FB7006 120 Ohm@100MHz 300mA +/-25% 0402 I — DMIC_DATA_L
29 DMIC_CLK — DMIC_CLK — FB7007 120 Ohm@100MHz 300mA +/-25% 0402 I — DMIC_CLK_L
C9719 15pF 50V 5% NPO C0402_N I
C9720 15pF 50V 5% NPO C0402_N I

7 USB2_P7_CAM_DN
7 USB2_P7_CAM_DP
R0402_N R9755 0R 5% I
L9516 90ohm 100mA +-20% L4S12X20U NI
R0402_N R9756 0R 5% I
USB2_P7_DN_CONN
USB2_P7_DP_CONN

INTERNAL ONLY

BPAGE DRAWING
apl_tl.UN557.57
Fri May 27 06:47:28 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <DISPLAY>	Rev: V01
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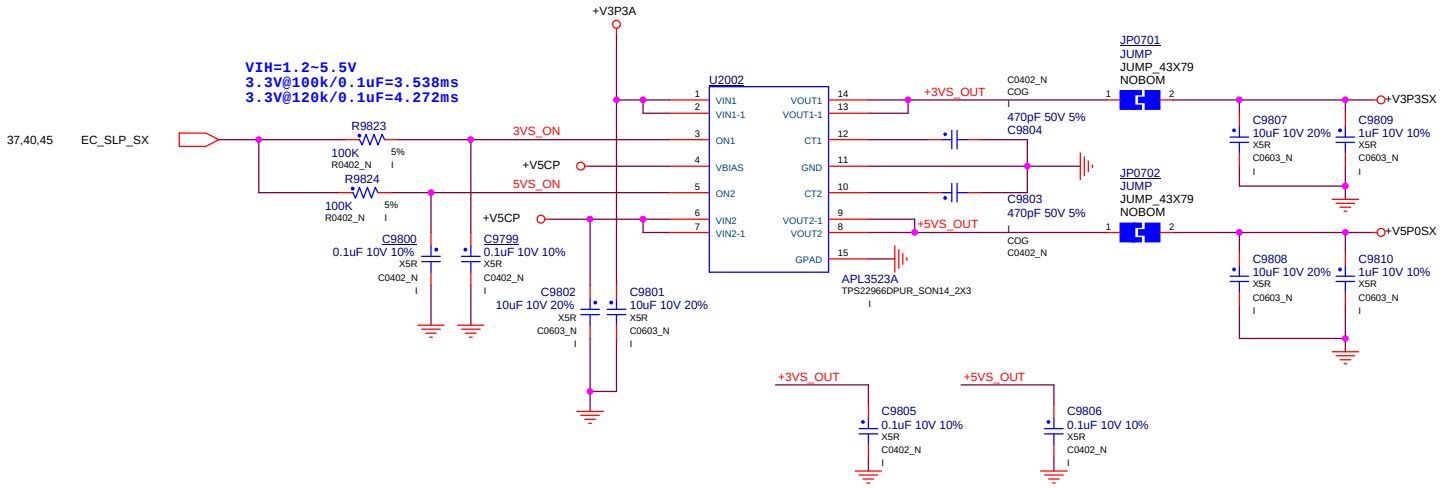

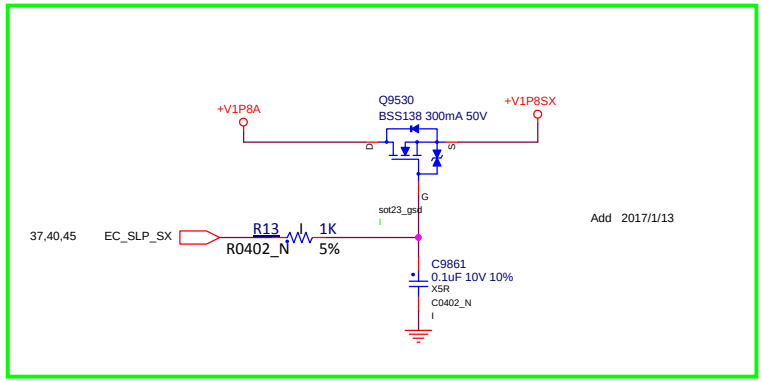

INTERNAL ONLY

BPAGE DRAWING

apl_lf.8A
Fri May 27 06:47:28 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: +V5P0A ,+V3P3SX,+V5P0SX	Rev: V01
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BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:28 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <NC>	Rev: V01
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apl_ff.UNS13.137
Fri May 27 06:47:30 2016

3nod三诺	Project:	120S-11&14IAP	
	Engineer:	LUFFY	
Size: Custom	Title: <NC>		Rev: V01
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BPAGE DRAWING

apl_8.8A
Fri May 27 06:47:30 2016

3nod三诺	Project:	120S-11&14IAP	
	Engineer:	LUFFY	
Size: Custom	Title: <NC>		Rev: V01
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BPAGE DRAWING

apl_ff.s
Fri May 27 06:47:30 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <NC>	Rev: V01
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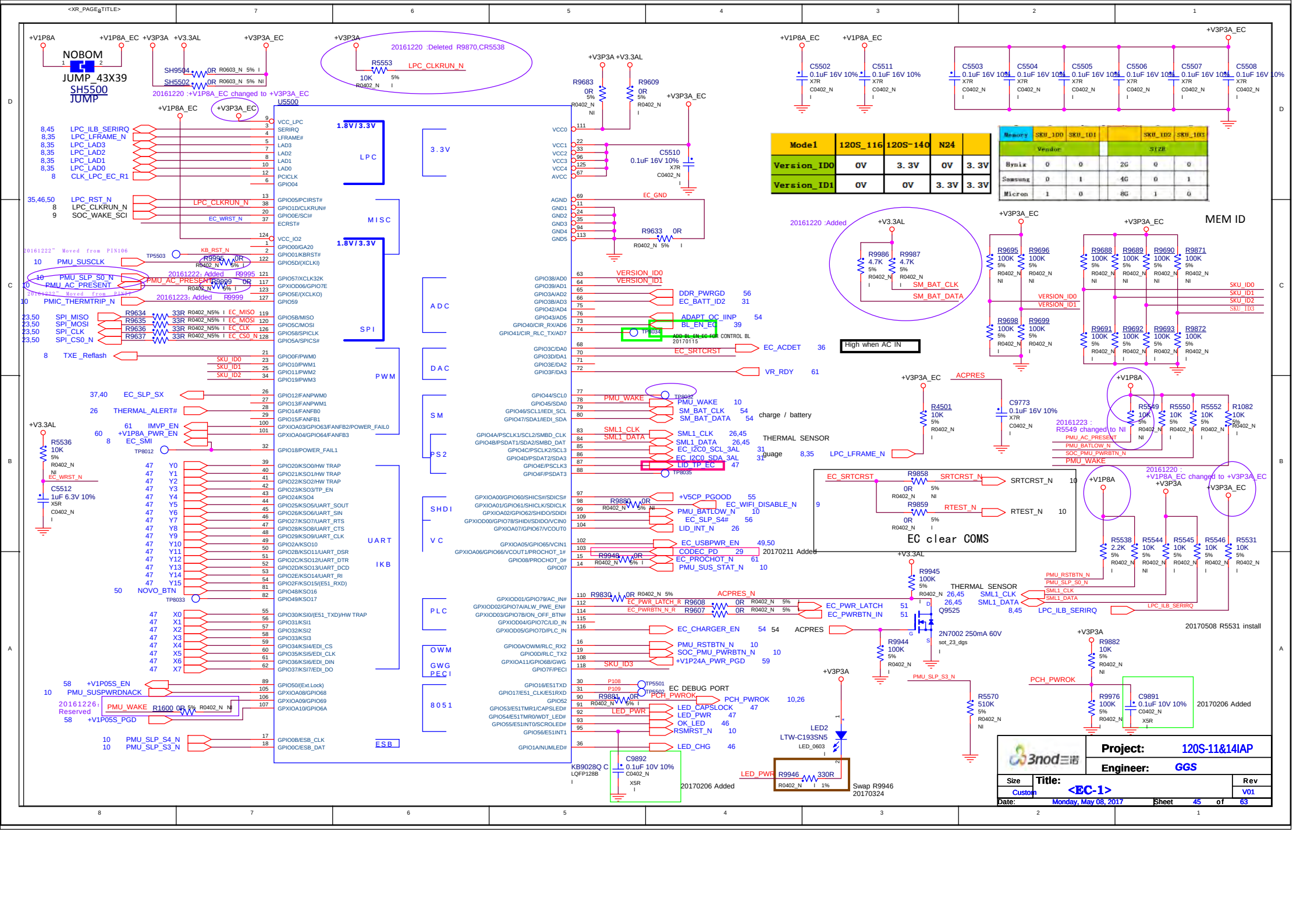
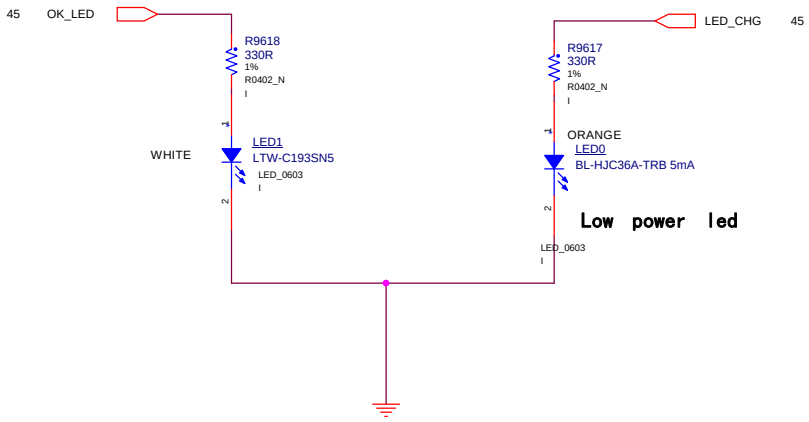
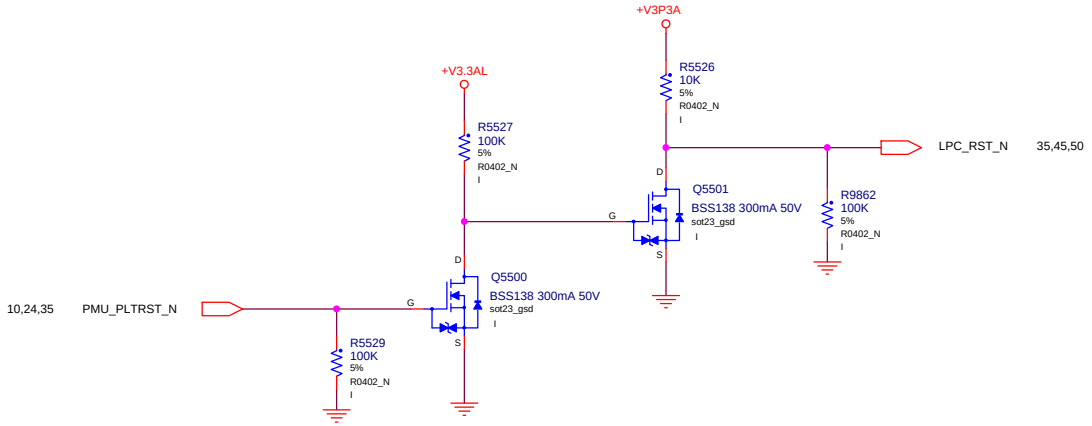

NOBOM
JUMP_43X39
SH5500
JUMP
20161220 :+V1P8A_EC changed to +V3P3A_EC
20161220 :Deleted R9870,CR5538
R5553
LPC_CLKRUN_N
U5500
1.8V/3.3V
LPC
3.3V
MISC
ADC
SPI
PWM
DAC
SM
PS2
SHDI
VC
UART
IKB
PLC
OWM
GWG
PECI
8051
ESB
LPC_ILB_SERIRQ
LPC_LFRAME_N
LPC_RST_N
LPC_CLKRUN_N
SOC_WAKE_SCI
EC_WRST_N
KB_RST_N
PMU_SUSCLK
PMU_SLP_S0_N
PMU_AC_PRESENT
PMIC_THERMTRIP_N
20161222: Added R9995
20161223: Added R9999
SPI_MISO
SPI_MOSI
SPI_CLK
SPI_CS0_N
EC_MISO
EC_MOSI
EC_CLK
EC_CS0_N
TXE _Reflash
SKU_ID0
SKU_ID1
SKU_ID2
EC_SLP_SX
THERMAL_ALERT#
IMVP_EN
+V1P8A_PWR_EN
EC_SMI
EC_WRST_N
C5512
1uF 6.3V 10%
NOVO_BTN
PMU_SUSPWRDNACK
20161226: Reserved
PMU_WAKE
R1600 0R
+V1P05S_EN
+V1P05S_PGD
PMU_SLP_S4_N
PMU_SLP_S3_N
VERSION_ID0
VERSION_ID1
DDR_PWRGD
EC_BATT_ID2
ADAPT_OC_IINP
BL_EN_EC
EC_SRTCRST
EC_ACDET
VR_RDY
PMU_WAKE
SM_BAT_CLK
SM_BAT_DATA
charge / battery
SML1_CLK
SML1_DATA
EC_I2C0_SCL_3AL
EC_I2C0_SDA_3AL
LID_TP_EC
THERMAL SENSOR
+V5CP_PGOOD
EC_WIFI_DISABLE_N
PMU_BATLOW_N
EC_SLP_S4#
LID_INT_N
EC_USBPWR_EN
CODEC_PD
EC_PROCHOT_N
PMU_SUS_STAT_N
20170211 Added
ACPRES_N
EC_PWR_LATCH_R
EC_PWRBTN_N_R
EC_CHARGER_EN
PMU_RSTBTN_N
SOC_PMU_PWRBTN_N
+V1P24A_PWR_PGD
SKU_ID3
EC DEBUG PORT
PCH_PWROK
LED_CAPSLOCK
LED_PWR
OK_LED
RSMRST_N
LED_CHG
KB9028Q C
LQFP128B
C9892
0.1uF 10V 10%
20170206 Added
Mode1
Version_ID0
Version_ID1
120S_116
120S-140
N24
MEM ID
Memory
Vendor
SIZE
Hynix
Samsung
Micron
20161220 :Added
High when AC IN
ACPRES
C9773
0.1uF 16V 10%
20161223 : R5549 changed to NI
20161220 : +V1P8A_EC changed to +V3P3A_EC
EC clear COMS
SRTCRST_N
RTEST_N
THERMAL SENSOR
2N7002 250mA 60V
sot_23_dgs
20170508 R5531 install
LED2
LTW-C193SN5
LED_0603
LED_PWR
R9946 330R
Swap R9946 20170324
20170206 Added
Project: 120S-11&14IAP
Engineer: GGS
Size: Custom
Title: <EC-1>
Rev: V01
Date: Monday, May 08, 2017
Sheet 45 of 63



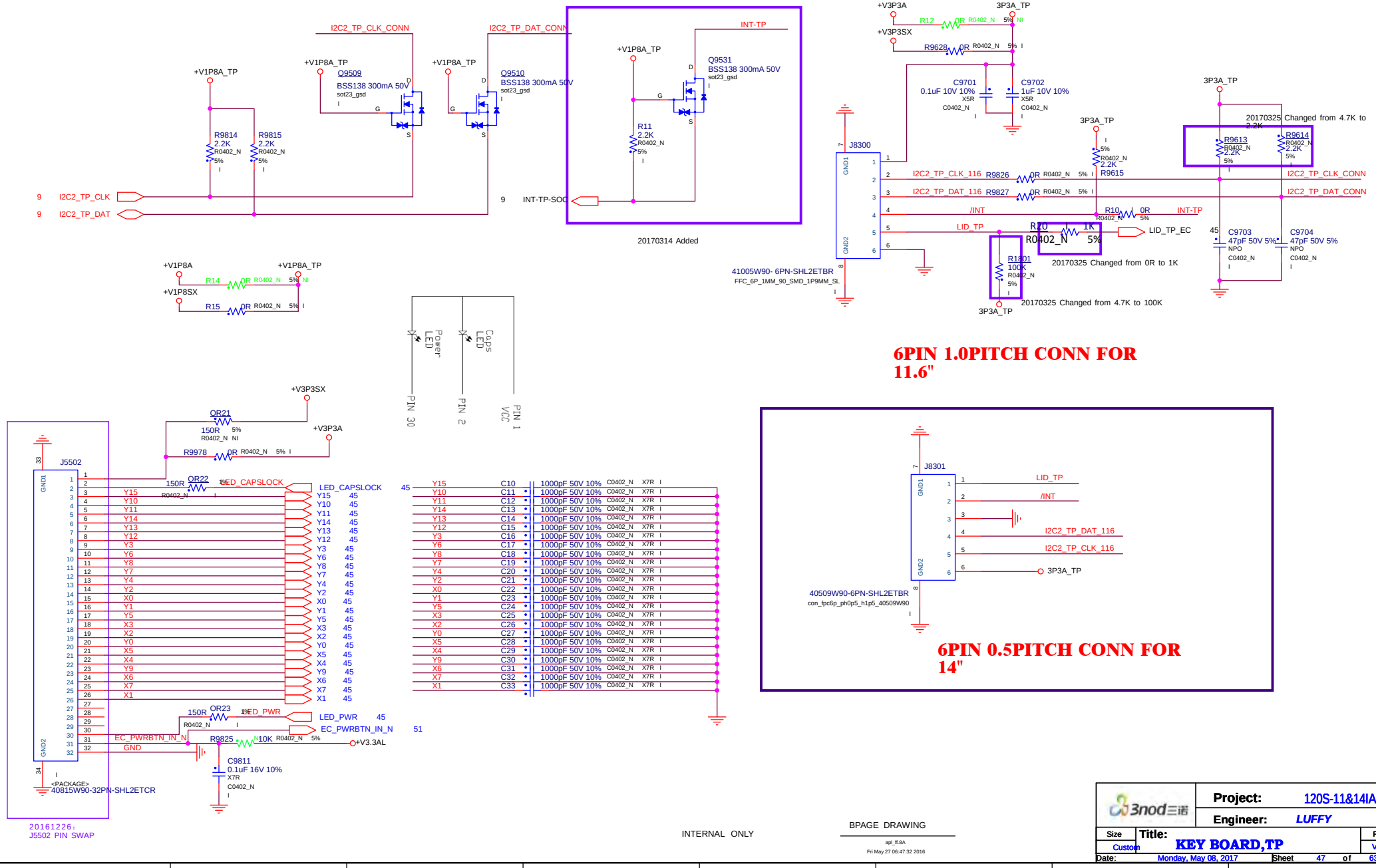


NOTE: CHECK RESET CONNECTION

BPAGE DRAWING

api_tf.UN$14.141
Fri May 27 06:47:32 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: LED AND BUTTON	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 46 of 63	


I2C2_TP_CLK_CONN
I2C2_TP_DAT_CONN
+V1P8A_TP
Q9509
BSS138 300mA 50V
Q9510
BSS138 300mA 50V
R9814 2.2K
R9815 2.2K
9 I2C2_TP_CLK
9 I2C2_TP_DAT
INT-TP
Q9531
BSS138 300mA 50V
R11 2.2K
9 INT-TP-SOC
20170314 Added
+V3P3A
3P3A_TP
+V3P3SX
R12 0R
R9628 0R
C9701 0.1uF 10V 10%
C9702 1uF 10V 10%
J8300
I2C2_TP_CLK_116
I2C2_TP_DAT_116
R9826 0R
R9827 0R
/INT
LID_TP
R10 0R
INT-TP
R20 1K
LID_TP_EC
R1801 100K
20170325 Changed from 0R to 1K
20170325 Changed from 4.7K to 100K
20170325 Changed from 4.7K to 2.2K
R9613
R9614
R9615
C9703 47pF 50V 5%
C9704 47pF 50V 5%
I2C2_TP_CLK_CONN
I2C2_TP_DAT_CONN
41005W90- 6PN-SHL2ETBR
FFC_6P_1MM_90_SMD_1P9MM_SL
6PIN 1.0PITCH CONN FOR 11.6"
+V1P8A
+V1P8SX
R14 0R
R15 0R
Power LED
Caps LED
PIN 30
PIN 2
PIN 1
+V3P3SX
+V3P3A
OR21 150R
R9978 0R
J5502
LED_CAPSLOCK
LED_PWR
EC_PWRBTN_IN_N
OR22 150R
OR23 150R
R9825 10K
C9811 0.1uF 16V 10%
+V3.3AL
GND
<PACKAGE>
40815W90-32PN-SHL2ETCR
20161226:
J5502 PIN SWAP
J8301
LID_TP
/INT
I2C2_TP_DAT_116
I2C2_TP_CLK_116
3P3A_TP
40509W90-6PN-SHL2ETBR
con_fpc6p_ph0p5_h1p5_40509W90
6PIN 0.5PITCH CONN FOR 14"
INTERNAL ONLY
BPAGE DRAWING
Project: 120S-11&14IAP
Engineer: LUFFY
Size: Custom
Title: KEY BOARD,TP
Rev: V01
Date: Monday, May 08, 2017
Sheet 47 of 63

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:32 2016

3nod三诺	Project:	120S-11&14IAP	
	Engineer:	LUFFY	
Size: Custom	Title: <NC>		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 48 of 63		

OCP SET TO 2A

NOBOM
JUMP_43X39
SH9506
JUMP

+V5CP

C2010
22uF 6.3V 20%
X5R
C0603_N

CC117
0.1uF 10V 10%
X5R
C0402_N

UB1
IN
OUT
GND
EN
OC
G524C1T11U
SY6288C20AAC_SOT23-5

+V5CP_USB3.0

45,50 EC_USBPWR_EN

TP8036

USB_OC1_N 7,50

20170207 Changed from G524D1T11U to G524C1T11U

20170206 Modified

USB2_P1_DP_CONN
USB2_P1_DN_CONN

CR9012
CR9013
AZ5725-01F.R7GR 1uA 5V
ESD0402

USB3_P1_TX_DP_CONN
USB3_P1_TX_DN_CONN
USB3_P1_RX_DP_CONN
USB3_P1_RX_DN_CONN

20170209 Modified

CR9006
ESD5344D
DFN10_PH0P5_ESD

7 USB3_P1_TX_DN
7 USB3_P1_TX_DP

C1271 0.1uF 10V 10%
C1270 0.1uF 10V 10%
C0402_N X5R

R9012 0R 5%
R9011 0R 5%
R0402_N

L9002
L4S12X20U
90ohm 100mA +-20%

C9902
C0603_N
X5R
22uF 6.3V 20%

C9791
150uF 6.3V 20%
CAP_3528_H1P9

C9900
22uF 6.3V 20%
X5R
C0603_N

C9006
0.1uF 10V 10%
X5R
C0402_N

C9007
22uF 6.3V 20%
X5R
C0603_N

20170314 Added C9900/C9902;C9791 changed to NI;C9007 changed to I

+V5CP_USB3.0

CR9005
TVQFB0201AC0 1uA 5V
ESD0402

7 USB3_P1_RX_DN
7 USB3_P1_RX_DP

R9745 0R 5%
R9746 0R 5%

L9515

7 USB2_P1_DN
7 USB2_P1_DP

R9007 0R 5%
R9006 0R 5%

L9003

J9504
W-90-USB3-H082
CON_USB30_9P_W-90-USB3-H082

VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+

20170206 changed

INTERNAL ONLY

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:32 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	USB CHANGER,USB3.0 CONN
		Rev: 1.01
Date: Tuesday, March 14, 2017	Sheet 49 of 63	

<XR_PAGE8TITLE>

SD CARD POWER SUPPLY

+V3P3SX → NOBOM JUMP_43X39 JUMP SH9503 → +V3.3S_SD
C9775 0.1uF 16V 10% X7R C0402_N

+V1P8SX
20161222" Changed to +V1P8SX
R9834 4.7K 5% R0402_N
RX2 10K 5% R0402_N
WLAN_EN
+V1P8SX
+V3.3S_SD
UX6 G2129TL1U SOT_363
VCCA VCCB GND OE A B
7 PCIE4_SD_CLKREQ2_N
SD_CLK_REQ#_LS
+V3.3S_SD
R9835 4.7K 5% R0402_N

+V5CP
G1 SH1 J9513 SH2 G2
con_fpc40p_ph0p5_h1p2_40553w90
40553W90-40PN-SHLOATCR
AUDIO_AGND

TO EC PIN34
7,49 USB_OC1_N
45,49 EC_USBPWR_EN
7 USB2_P4_DN
7 USB2_P4_DP
USB2_P4_DN
USB2_P4_DP
7 USB3_P4_TX_DN
7 USB3_P4_TX_DP
USB3_P4_TX_DN
USB3_P4_TX_DP
7 USB3_P4_RX_DN
7 USB3_P4_RX_DP
USB3_P4_RX_DN
USB3_P4_RX_DP
7 PCIE4_SD_RX_DN
7 PCIE4_SD_RX_DP
7 PCIE4_SD_REFCLK2_DN
7 PCIE4_SD_REFCLK2_DP
+V3.3S_SD
7 PCIE4_SD_TX_DN
7 PCIE4_SD_TX_DP
PCIE4_SD_TX_DN
PCIE4_SD_TX_DP
35,45,46 LPC_RST_N
SD_CLK_REQ#_LS
NOVO_BTN
30 HPOUT_L_CONN
30 HPOUT_R_CONN
29 HPOUT_JD
30 MIC1_CONN
HPOUT_JD
MIC1_CONN
30 SPK_RP_CONN
30 SPK_RN_CONN
SPK_RP_CONN
SPK_RN_CONN

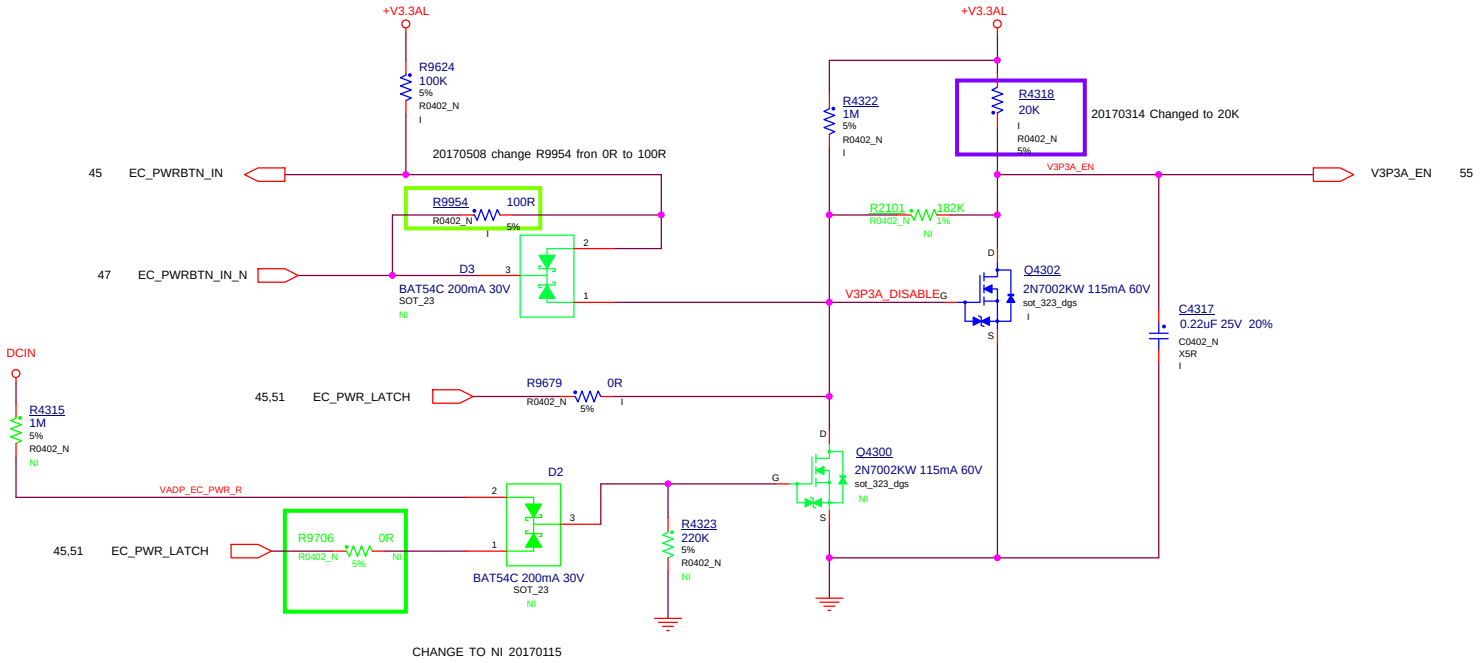
R9831 0R 5% R0603_N
R9832 0R 5% R0603_N
R9833 0R 5% R0603_N
AUDIO_AGND

+V3.3AL
R9 100K 5% R0402_N
NOVO_BTN
NOVO_BTN 45
TO EC PIN81

J7005 W1251-0201 wtb_2p_1p25_90_BAT
30 SPK_LP_CONN
30 SPK_LN_CONN
SPK_LP_CONN
SPK_LN_CONN
G1 G2 PAD1 PAD2

BPAGE DRAWING
apl_ff.s
Fri May 27 06:47:32 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	<IO&DEBUG CONN>
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 50 of 63	



CHANGE TO NI 20170115

BPAGE DRAWING

apl_ff.UN$20.203
Fri May 27 06:47:34 2016

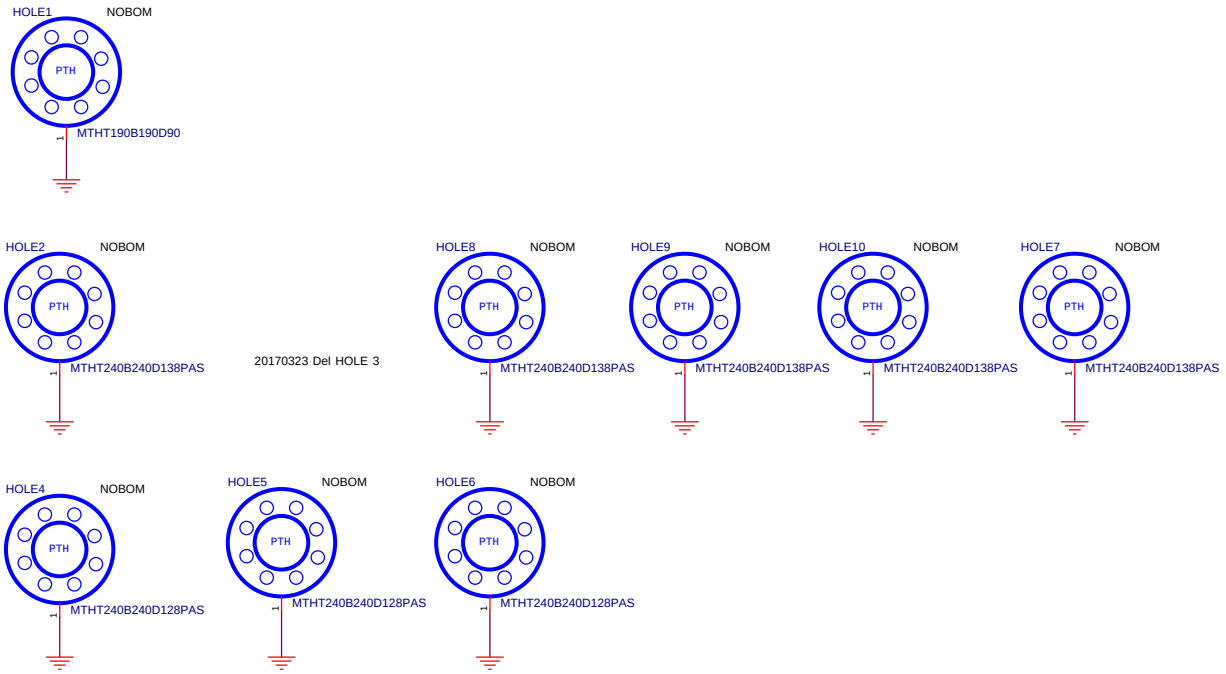
3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <MISC>	Rev: V01
Date: Monday, May 08, 2017	Sheet 51 of 63	

INTERNAL ONLY

BPAGE DRAWING

apl_ff.UN$20.205
Fri May 27 06:47:34 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 52 of 63	



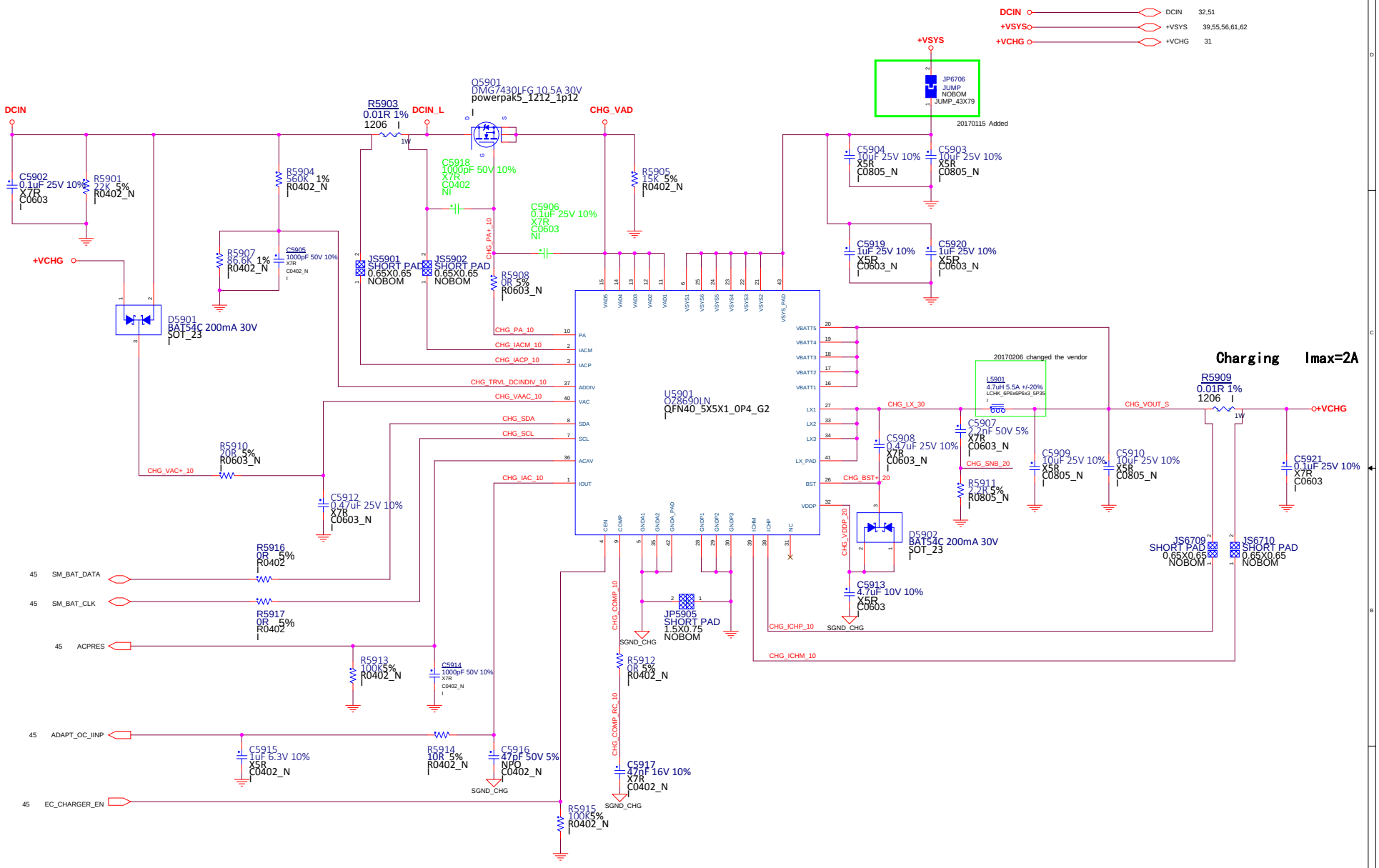
INTERNAL ONLY

BPAGE DRAWING

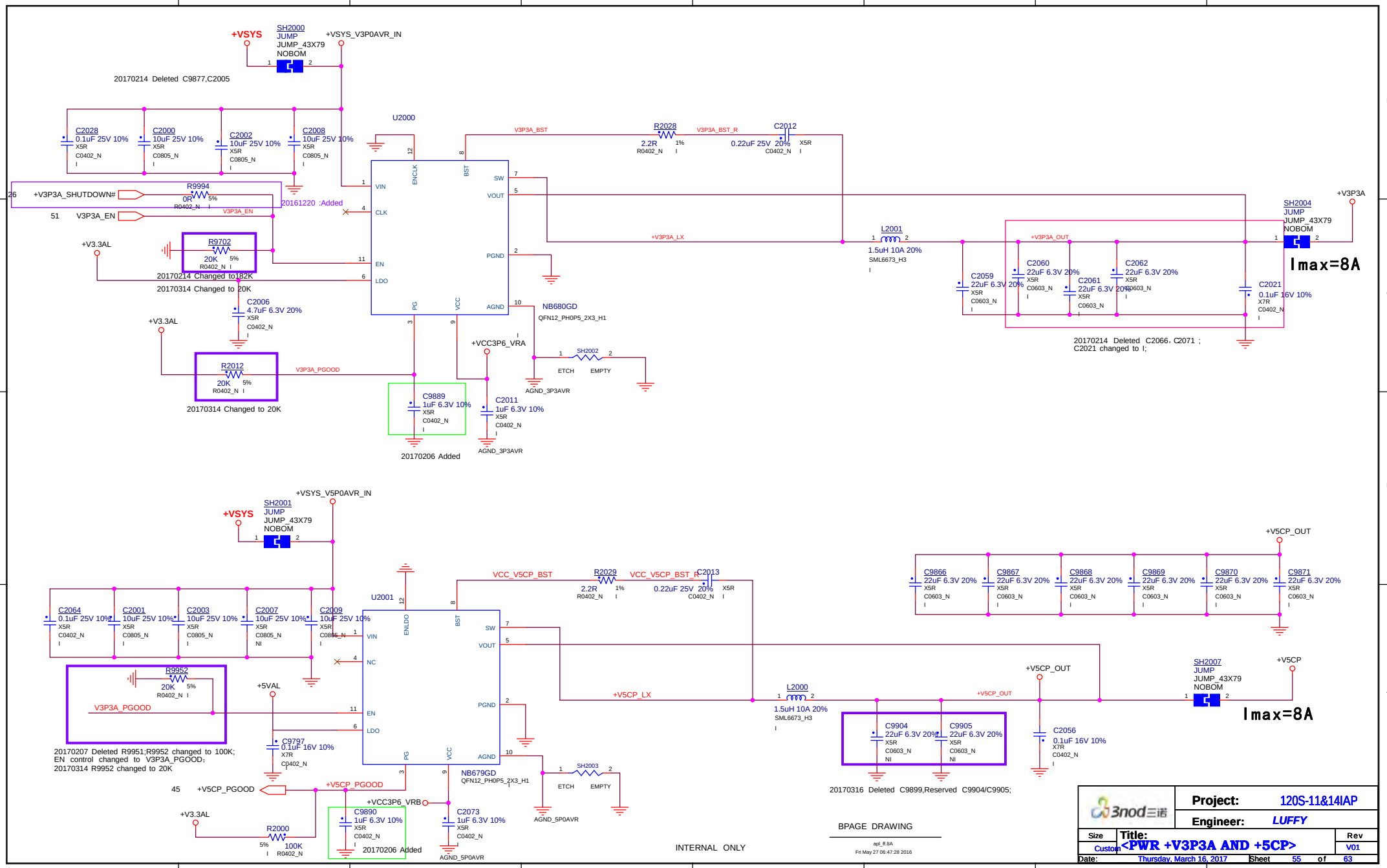
apl_ff.UN$20.205
Fri May 27 06:47:34 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <SCREW>	Rev: V01
Date: Friday, March 24, 2017	Sheet 53 of 63	

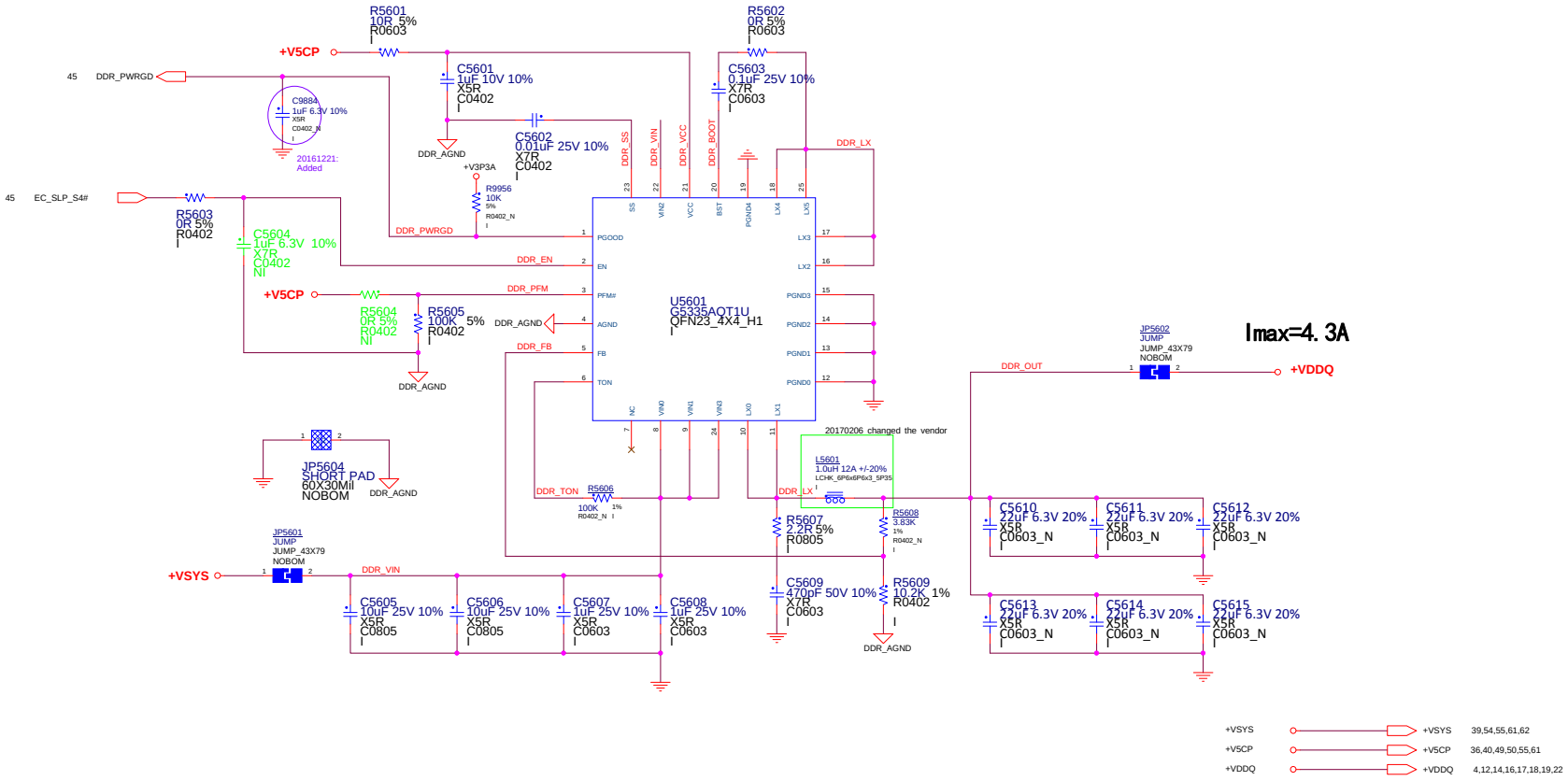
59: BATTERY CHARGER



3nod三诺	Project: 120S-11&14IAP		
	Engineer: Frank		
Size: Custom	Title: <BatteryCharger>		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 54 of 63		


+VSYS
SH2000
JUMP
JUMP_43X79
NOBOM
+VSYS_V3P0AVR_IN
20170214 Deleted C9877,C2005
U2000
C2028 0.1uF 25V 10% X5R C0402_N
C2000 10uF 25V 10% X5R C0805_N
C2002 10uF 25V 10% X5R C0805_N
C2008 10uF 25V 10% X5R C0805_N
R2028 2.2R 1% R0402_N
V3P3A_BST
V3P3A_BST_R
C2012 0.22uF 25V 20% X5R C0402_N
R9994 0R 5% R0402_N
+V3P3A_SHUTDOWN#
V3P3A_EN
20161220 :Added
R9702 20K 5% R0402_N
20170214 Changed to182K
20170314 Changed to 20K
+V3.3AL
C2006 4.7uF 6.3V 20% X5R C0402_N
VIN
ENCLK
BST
SW
VOUT
CLK
PGND
EN
LDO
PG
VCC
AGND
NB680GD
QFN12_PH0P5_2X3_H1
+V3P3A_LX
L2001 1.5uH 10A 20% SML6673_H3
+V3P3A_OUT
C2059 22uF 6.3V 20% X5R C0603_N
C2060 22uF 6.3V 20% X5R C0603_N
C2061 22uF 6.3V 20% X5R C0603_N
C2062 22uF 6.3V 20% X5R C0603_N
C2021 0.1uF 16V 10% X7R C0402_N
SH2004
JUMP
JUMP_43X79
NOBOM
+V3P3A
Imax=8A
20170214 Deleted C2066、C2071 ; C2021 changed to I;
+V3.3AL
R2012 20K 5% R0402_N
V3P3A_PGOOD
20170314 Changed to 20K
+VCC3P6_VRA
SH2002
ETCH
EMPTY
AGND_3P3AVR
C9889 1uF 6.3V 10% X5R C0402_N
C2011 1uF 6.3V 10% X5R C0402_N
20170206 Added
+VSYS_V5P0AVR_IN
SH2001
JUMP
JUMP_43X79
NOBOM
+VSYS
U2001
C2064 0.1uF 25V 10% X5R C0402_N
C2001 10uF 25V 10% X5R C0805_N
C2003 10uF 25V 10% X5R C0805_N
C2007 10uF 25V 10% X5R C0805_N NI
C2009 10uF 25V 10% X5R C0805_N
VCC_V5CP_BST
R2029 2.2R 1% R0402_N
VCC_V5CP_BST_R
C2013 0.22uF 25V 20% X5R C0402_N
ENLDO
BST
SW
VOUT
VIN
NC
PGND
EN
LDO
PG
VCC
AGND
NB679GD
QFN12_PH0P5_2X3_H1
+V5CP_LX
L2000 1.5uH 10A 20% SML6673_H3
+V5CP_OUT
C9866 22uF 6.3V 20% X5R C0603_N
C9867 22uF 6.3V 20% X5R C0603_N
C9868 22uF 6.3V 20% X5R C0603_N
C9869 22uF 6.3V 20% X5R C0603_N
C9870 22uF 6.3V 20% X5R C0603_N
C9871 22uF 6.3V 20% X5R C0603_N
C9904 22uF 6.3V 20% X5R C0603_N NI
C9905 22uF 6.3V 20% X5R C0603_N NI
C2056 0.1uF 16V 10% X7R C0402_N
SH2007
JUMP
JUMP_43X79
NOBOM
+V5CP
Imax=8A
R9952 20K 5% R0402_N
V3P3A_PGOOD
+5VAL
C9797 0.1uF 16V 10% X7R C0402_N
20170207 Deleted R9951;R9952 changed to 100K;
EN control changed to V3P3A_PGOOD;
20170314 R9952 changed to 20K
45 +V5CP_PGOOD
+V5CP_PGOOD
+VCC3P6_VRB
+V3.3AL
R2000 100K 5% R0402_N
C9890 1uF 6.3V 10% X5R C0402_N
C2073 1uF 6.3V 10% X5R C0402_N
20170206 Added
SH2003
ETCH
EMPTY
AGND_5P0AVR
20170316 Deleted C9899,Reserved C9904/C9905;
INTERNAL ONLY
BPAGE DRAWING
apl_lf.8A
Fri May 27 06:47:28 2016
3nod三诺
Project: 120S-11&14IAP
Engineer: LUFFY
Size: Custom
Title: <PWR +V3P3A AND +5CP>
Rev: V01
Date: Thursday, March 16, 2017
Sheet 55 of 63

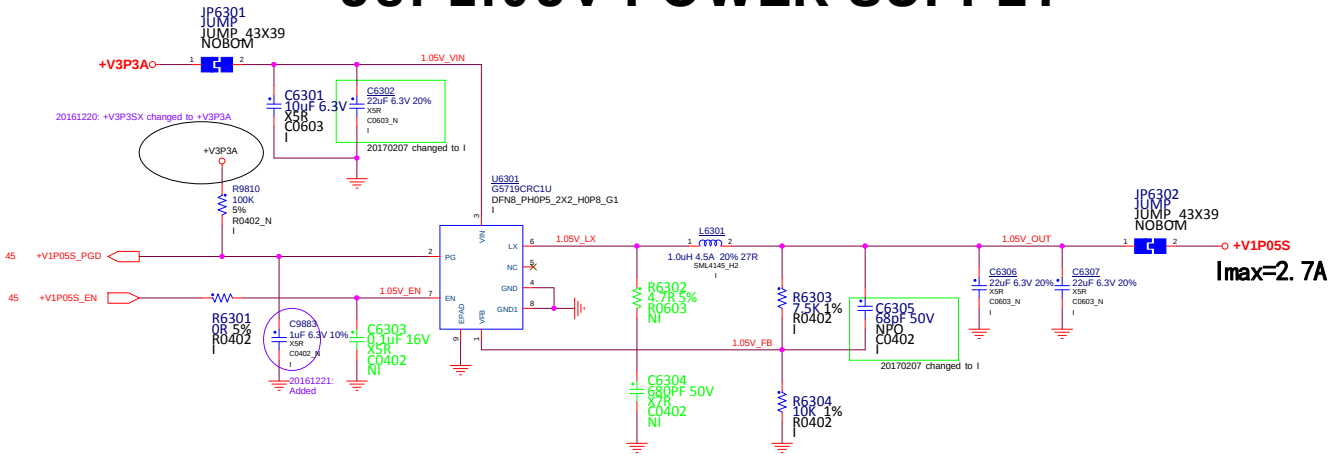
56: DDR POWER SUPPLY



3nod三诺	Project:	120S-11&14IAP
	Engineer:	Frank
Size: C	Title:	<DDR Power>
Rev: V01		
Date: Tuesday, March 14, 2017	Sheet 56 of 63	

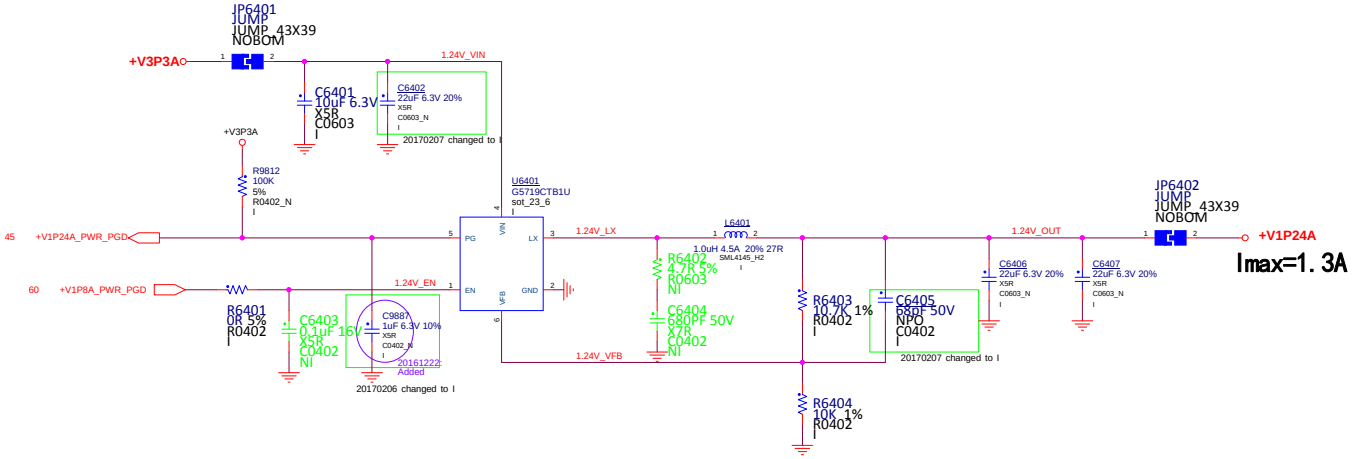
3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size: C	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 57 of 63	

58: 1.05V POWER SUPPLY



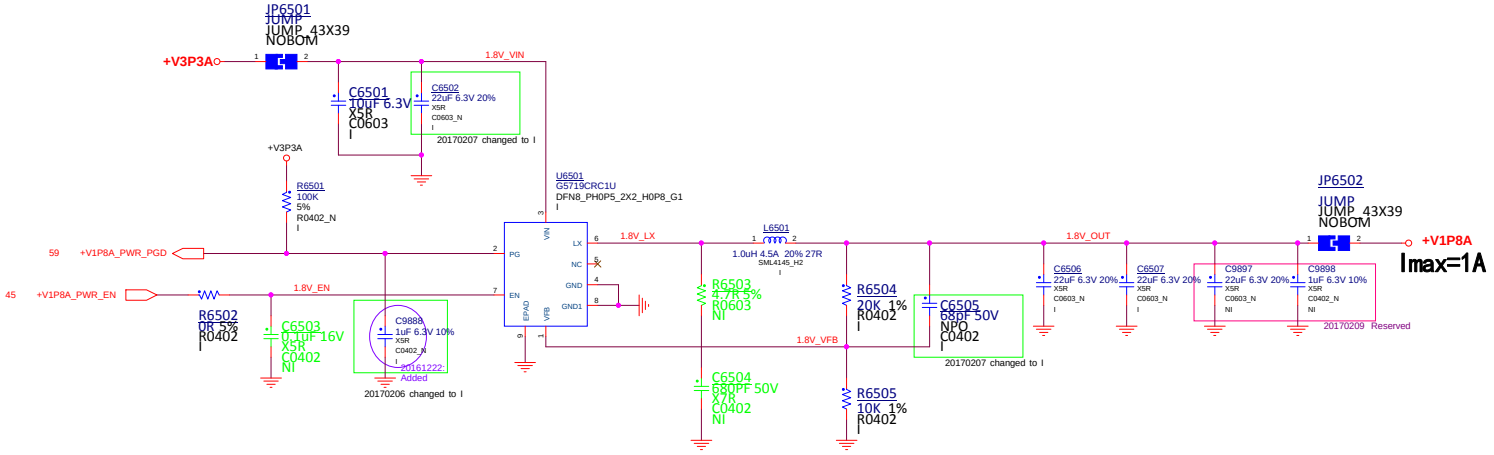
3nod三诺	Project:	120S-11&14IAP
	Engineer:	Frank
Size: C	Title:	<1.05V POWER SUPPLY>
Rev: V01		
Date: Tuesday, March 14, 2017	Sheet 58 of 63	

59: 1.24V POWER SUPPLY



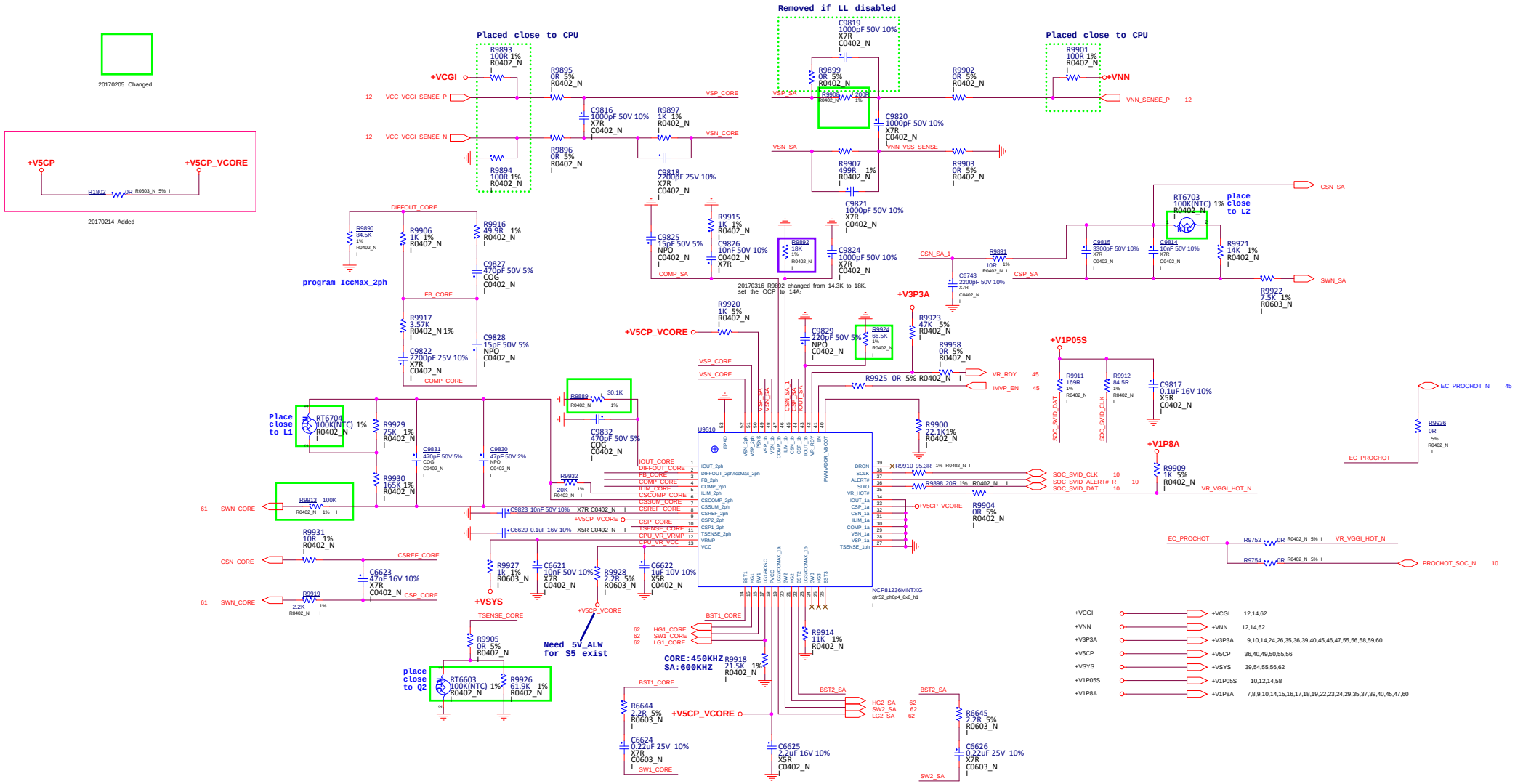
3nod三诺	Project:	120S-11&14IAP
	Engineer:	Frank
Size: C	Title:	<1.24V POWER SUPPLY>
Date: Tuesday, March 14, 2017	Sheet 59 of 63	Rev: V01

60: +1.8V POWER SUPPLY



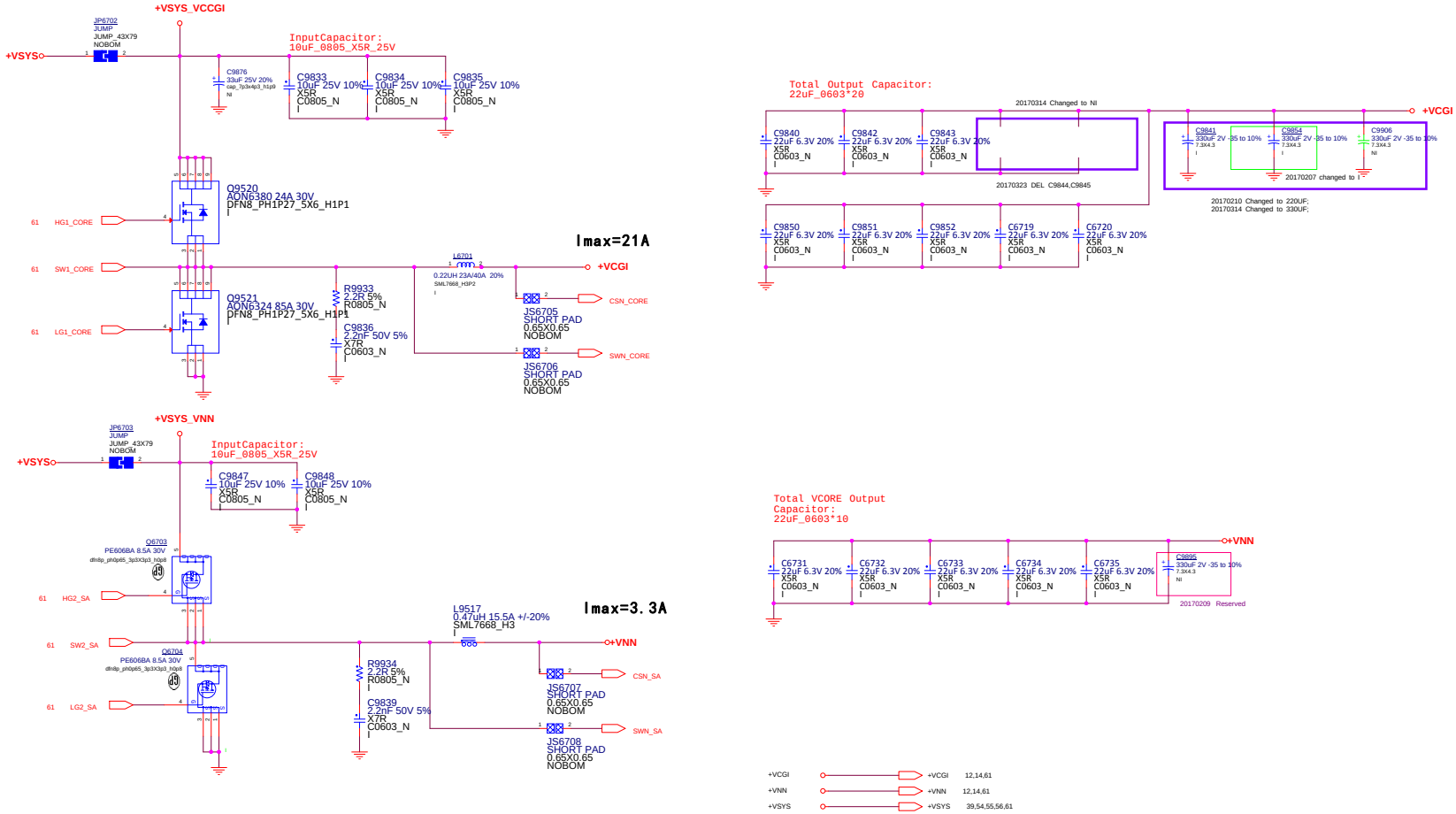
3nod三诺	Project:	120S-11&14IAP
	Engineer:	Frank
Size: C	Title:	<+1.8V_PRIM>
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 60 of 63	

CPU POWER SUPPLY



3nod三诺	Project: NA	
	Engineer: Frank	
Size: Custom	Title: <VCGI AND VNN_1>	Rev: V01
Date: Thursday, March 16, 2017	Sheet 61 of 63	

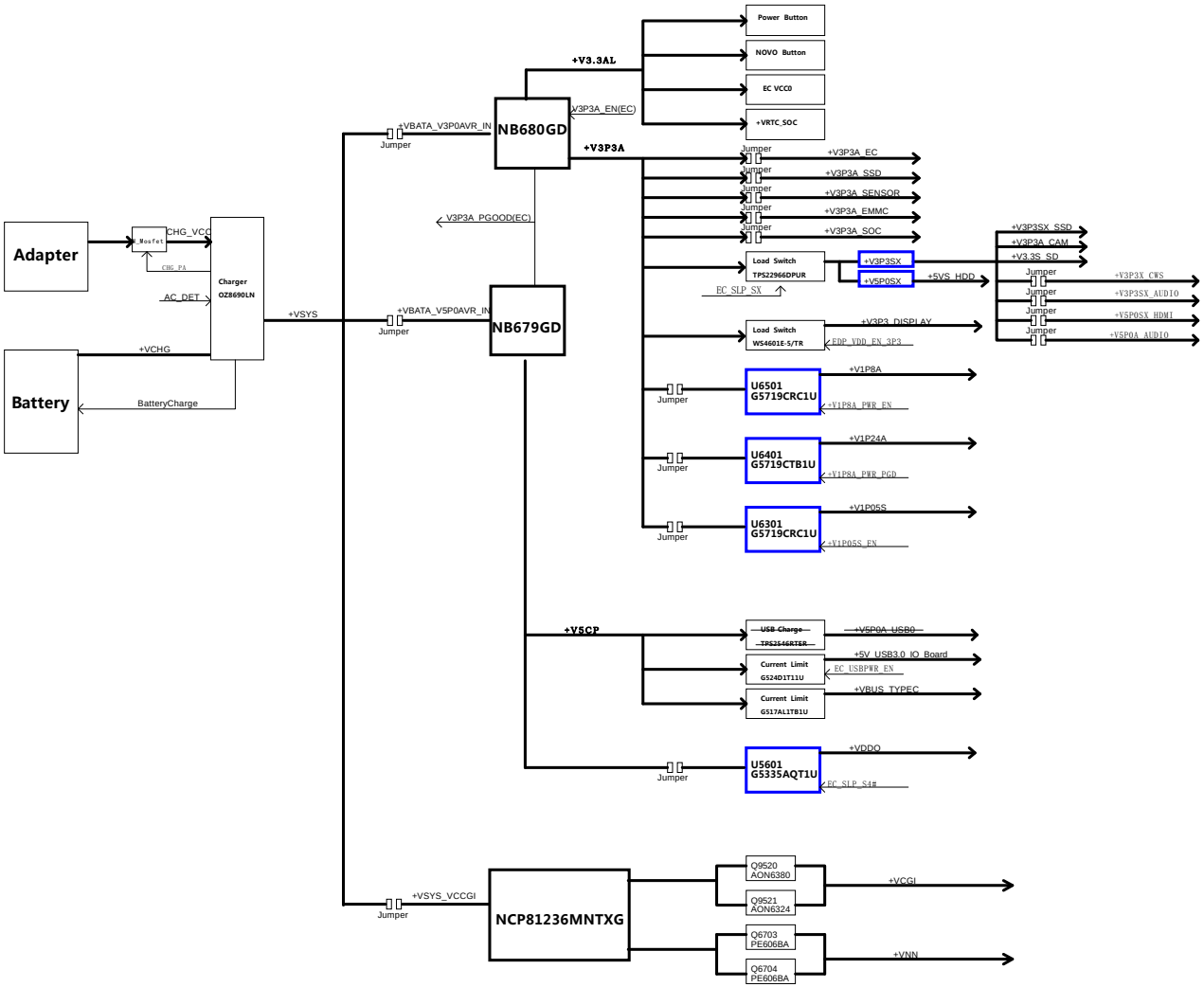
VCGI / VNN POWER SUPPLY



+VCGI	+VCGI	12,14,61	
+VNN	+VNN	12,14,61	
+VSYS	+VSYS	39,54,55,56,61	

3nod三诺	Project: NA	
	Engineer: Frank	
Size: Custom	Title: <VCGI AND VNN_2>	Rev: V01
Date: Thursday, March 23, 2017	Sheet 62 of 63	

Apollo Lake Platform Power Map



3nod三诺	Project:	120S-11&14IAP
	Engineer:	Frank
Size: C	Title:	<PWR BLOCK DIAGRAM>
Rev: V01		
Date: Tuesday, March 14, 2017	Sheet 63 of 63	