

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
07		355269	ENGINEERING RELEASED	12/10/04	?

M42/M42A MLB - GM - CS

10/16/2006 PVT

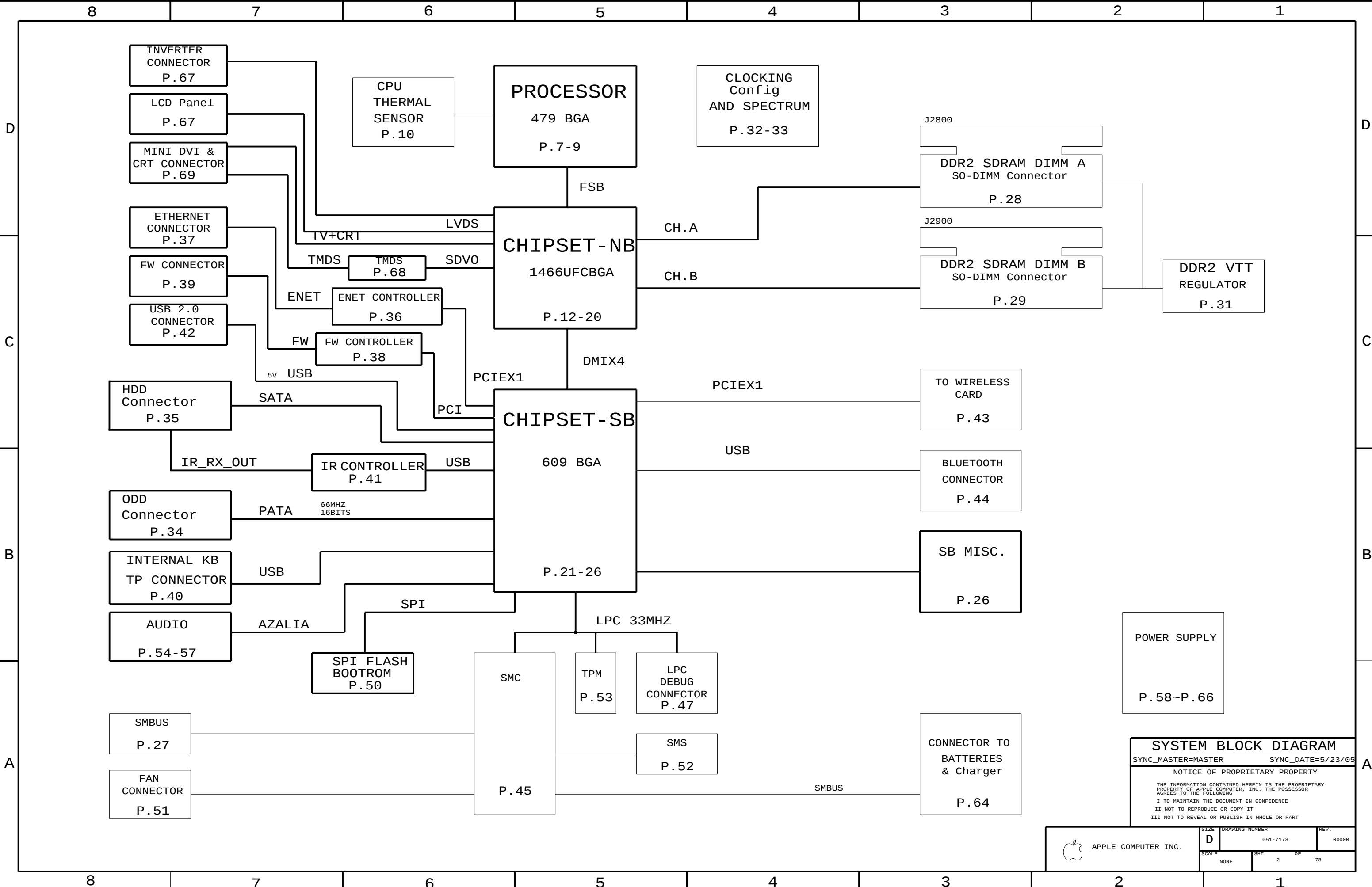
Page	Contents	M42-DRI	Sync	Date
1	Table of Contents	RX	N/A	N/A
2	SYSTEM BLOCK DIAGRAM	RX	MASTER	5/23/05
3	Power Block Diagram	MK	POWER	06/30/2005
4	CONFIGURATION OPTIONS	RX	SMC	07/18/2005
5	FUNC TEST 1 OF 2	RX	TP	07/25/2005
6	SIGNAL ALIAS /RESET	RX	ENET	08/19/2005
7	CPU 1 OF 2-FSB	RX	MASTER	05/03/2005
8	CPU 2 OF 2-PWR/GND	MK	MASTER	05/03/2005
9	CPU DECAPS & VID<>	MK	SMC	08/19/2005
10	CPU MISC1-TEMP SENSOR	ES	ENET	08/19/2005
11	CPU ITP700FLEX DEBUG	RX	MASTER	5/23/05
12	NB CPU Interface	MK	NB	07/25/2005
13	NB PEG / Video Interfaces	DK	NB	07/25/2005
14	NB Misc Interfaces	RX	NB	08/15/2005
15	NB DDR2 Interfaces	LT	NB	07/25/2005
16	NB Power 1	DK	NB	07/25/2005
17	NB Power 2	DK	NB	07/25/2005
18	NB Grounds	DK	NB	07/25/2005
19	NB (GM) Decoupling	DK	NB	06/22/2005
20	NB Config Straps	DK	NB	06/28/2005
21		RX	SB	08/05/2005
22		RX	ENET	11/16/2005
23		RX	ENET	11/28/2005
24		RX	SB	08/05/2005
25		RX	SB	06/28/2005
26	SB Misc	RX	NB	07/26/2005
27	M42 SMBUS CONNECTIONS	ES	ENET	08/30/2005
28	DDR2 SO-DIMM Connector A	LT	MEMORY	06/20/2005
29	DDR2 SO-DIMM Connector B	LT	MEMORY	06/20/2005
30	Memory Active Termination	LT	MEMORY	06/20/2005
31	Memory Vtt Supply	LT	(MASTER)	(MASTER)
32	CLOCKS	DK	CLOCK	06/03/2005
33	CLOCK TERMINATION	DK	CLOCK	06/06/2005
34	PATA CONNECTOR	ES	ENET	11/01/2005
35	SATA CONNECTOR	ES	ENET	11/14/2005
36	ETHERNET CONTROLLER	ES	ENET	12/06/2005
37	ETHERNET CONNECTOR	ES	ENET	11/14/2005
38	FIREWIRE CONTROLLER	ES	ENET	08/30/2005
39	FIREWIRE PORT	ES	ENET	11/16/2005
40	CONNECTOR MISC	ES	ENET	11/16/2005
41	IR CONTROLLER	ES	ENET	11/09/2005
42		ES	ENET	11/01/2005
43		ES	ENET	08/19/2005
44	BLUETOOTH INTERFACE	MK	ENET	08/29/2005
45	SMC	MK	SMC	08/18/2005
46	SMC SUPPORT	LD	SMC	08/23/2005
47	LPC+ Debug Connector	MK	NB	06/30/2005
48	CPU Current & Voltage Sense	ES	ENET	08/30/2005

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50	63	SPI BOOTROM	ES	MASTER	5/23/05
51	65	Fan	MK	ENET	11/10/2005
52	66	SMS	RX	SMC	08/23/2005
53	67	TPM	DK	SMC	07/18/2005
54	68	AUDIO0: CODEC	DK	M42AUDIO	08/05/2006
55	72	AUDIO0: SPEAKER AMP	DK	M42AUDIO	08/05/2006
56	73	AUDIO0: JACK	DK	M42AUDIO	08/05/2006
57	74	AUDIO0: JACK TRANSLATORS	MK	M42AUDIO	08/05/2006
58	75	IMVP6 CPU VCore Regulator	MK	POWER	07/13/2005
59	76	5V / 3.3V Power Supply	MK	POWER	07/13/2005
60	77	2.5V/1.2V Regulator	MK	ENET	12/06/2005
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62	79	1.5V / 1.05V Power Supply	MK	POWER	07/13/2005
63	80	S3/S0 FETS, G3H SUPPLY	MK	ENET	08/30/2005
64	81	Power Conn / Alias	MK	ENET	11/16/2005
65	82	DC-In & Battery Connectors	MK	POWER	07/13/2005
66	83	PBUS Supply/Battery Charger	ES	SMC	08/19/2005
67	94	INVERTER, LVDS, TMDS	DK	GRAPHIC	06/06/2005
68	95	EXTERNAL TMDS	DK	GRAPHIC	06/06/2005
69	98	MINI-DVI CONNECTOR		EUGENE	05/21/05
70	99	Cross Reference Page			
71	100	Cross Reference Page			
72	101	Cross Reference Page			
73	102	Cross Reference Page			
74	103	Cross Reference Page			
75	104	Cross Reference Page			
76	105	Cross Reference Page			
77	106	Cross Reference Page			
78	107	Cross Reference Page			

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-7173	1	SCHEM, M42, MLB	SCH	
820-1889	1	PCBF, M42, MLB	PCB	

DIMENSIONS ARE IN MILLIMETERS XX ± _____ X.XX ± _____ X.XXX ± _____ ANGLES ± _____ DO NOT SCALE DRAWING	METRIC				 Apple Computer Inc.	
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	DRAFTER			DESIGN CK		
	ENG APPD			MFG APPD		
QA APPD			DESIGNER			
RELEASE			SCALE		TITLE	
		NONE		SCHEM, MLB, M42		
 THIRD ANGLE PROJECTION	MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER 051-7173		
				REV. 00000		
				SHT 1	OF 78	



SYSTEM BLOCK DIAGRAM

SYNC_MASTER=MASTER

SYNC_DATE=5/23/05

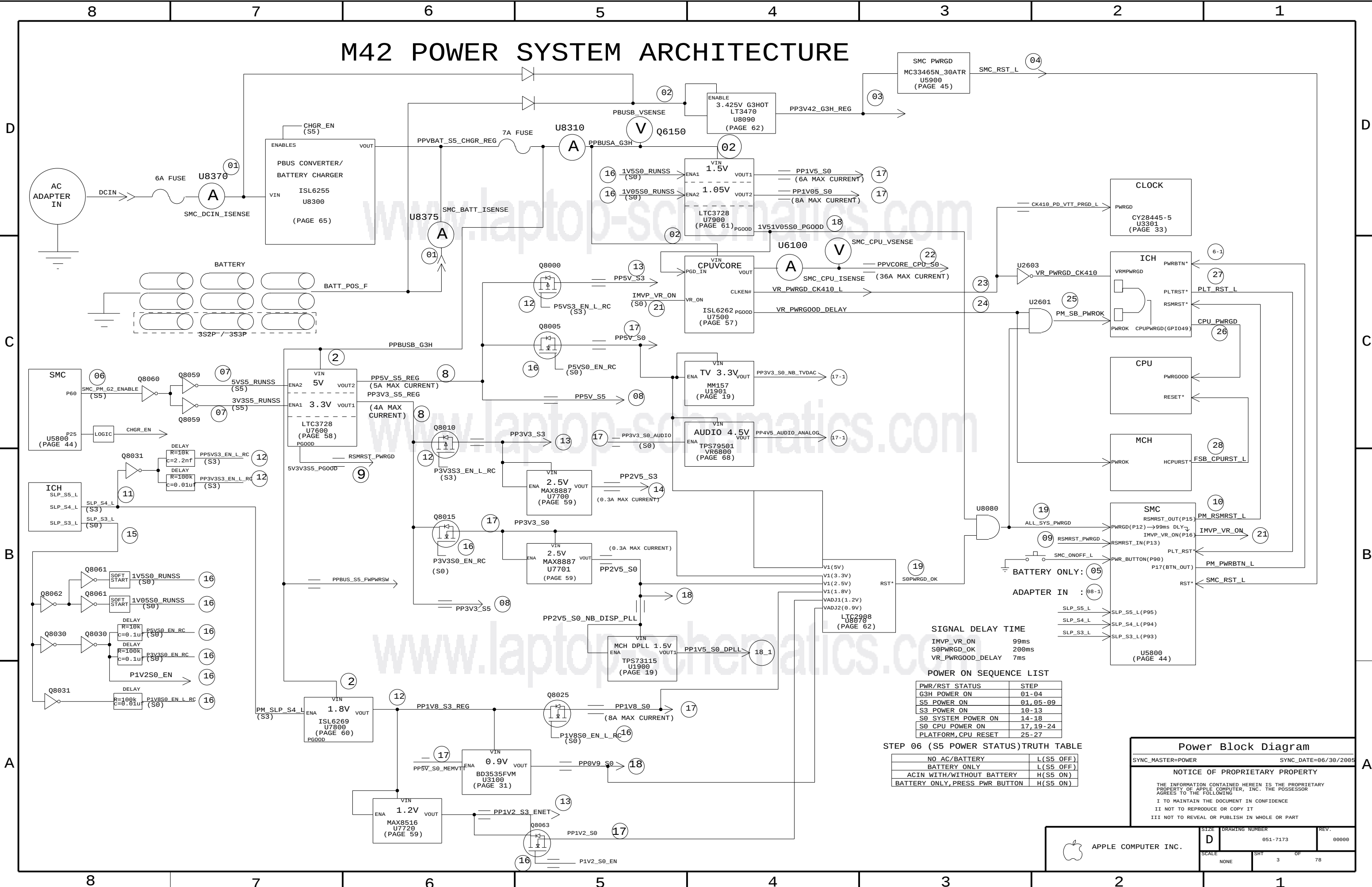
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SIGNAL DELAY TIME

IMVP_VR_ON	99ms
S0PWRGD_OK	200ms
VR_PWRGOOD_DELAY	7ms

POWER ON SEQUENCE LIST

PWR/RST STATUS	STEP
G3H POWER ON	01-04
S5 POWER ON	01,05-09
S3 POWER ON	10-13
S0 SYSTEM POWER ON	14-18
S0 CPU POWER ON	17,19-24
PLATFORM,CPU RESET	25-27

STEP 06 (S5 POWER STATUS) TRUTH TABLE

NO AC/BATTERY	L(S5 OFF)
BATTERY ONLY	L(S5 OFF)
ACIN WITH/WITHOUT BATTERY	H(S5 ON)
BATTERY ONLY,PRESS PWR BUTTON	H(S5 ON)

Power Block Diagram

SYNC_MASTER=POWER SYNC_DATE=06/30/2005

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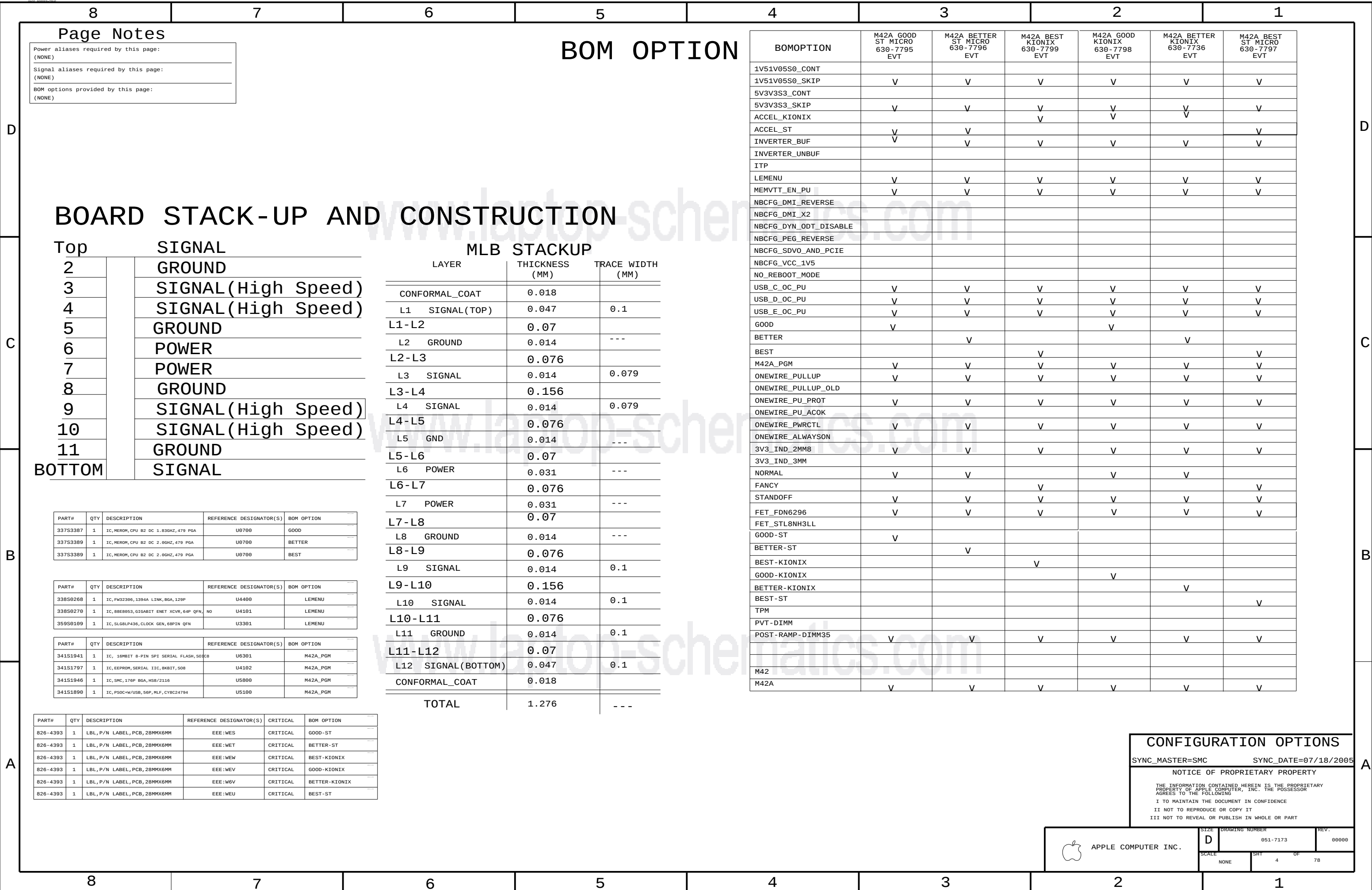


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SIZE: DRAWING NUMBER: REV.

D 051-7173 00000

SCALE: NONE SHY 3 OF 78



I140	TRUE	=PP5V_S0_LPC
I141	TRUE	LPC_AD<0>
I142	TRUE	LPC_AD<1>
I143	TRUE	LPC_FRAME_L
I144	TRUE	PM_CLKRUN_L
I145	TRUE	BOOT_LPC_SPI
I146	TRUE	SMC_TMS
I147	TRUE	DEBUG_RST_L
I148	TRUE	SMC_TRST_L
I149	TRUE	SMC_TDO
I150	TRUE	SMC_MD1
I151	TRUE	SMC_TX_L
I152	TRUE	FWH_INIT_L
I153	TRUE	PCI_CLK_PORTB
I154	TRUE	LPC_AD<2>
I155	TRUE	LPC_AD<3>
I156	TRUE	INT_SERIRQ
I157	TRUE	PM_SUS_STAT_L
I158	TRUE	SMC_TDI
I159	TRUE	SMC_TCK
I160	TRUE	SMC_RST_L
I161	TRUE	SMC_NMI
I162	TRUE	SMC_RX_L
I163	TRUE	SV_SET_UP

Other Func Test		
FUNC_TEST		
I164	TRUE	=PP1V05_S0_R
SMBus FUNC_TEST		
I182	TRUE	SMBUS_SMC_ML
I183	TRUE	SMBUS_SMC_ML
FIREWIRE FUNC_TEST		
I189	TRUE	PPFW_SWITCH
SLEEP_LED_FUNC_TEST		
I195	TRUE	SYS_LED_ANODE
SMC_FUNC_TEST		
I196	TRUE	SMC_LID
I197	TRUE	SMC_MANUAL_RST
I198	TRUE	SMC_CPU_VSENSE
Power Supply FUNC_TEST		
I199	TRUE	ALL_SYS_PWRGD
I200	TRUE	PPVCORE_CPU_S
I201	TRUE	PP1V05_S0
I202	TRUE	PP1V5_S0
I203	TRUE	PP1V8_S0
I204	TRUE	PP2V5_S0
I205	TRUE	PP3V3_S0
I206	TRUE	PP5V_S0
I207	TRUE	PP1V2_S3
I208	TRUE	PP1V8_S3
I209	TRUE	PP2V5_S3
I210	TRUE	PP3V3_S3

NO_TEST

CLOCK NO. TESTS

NO_TEST

NO_TESTNO TESTNO TESTNO_TEST

FUNC TEST

FUNC_TEST

FUNC TEST

Audio FUNC_TEST

Battery FUNC TESTUSB_FUNC_TESTDC-JACK_FUNC_TEST

Battery charger FUNC_TEST

INVERTER CONNECTOR FUNC_TESTEUNC TESTFIREWIRE_FUNC_TESTSMC_FUNC_TESTPower Supply FUNC_TESTNOTICE OF PROPRIETARY PROPERTY

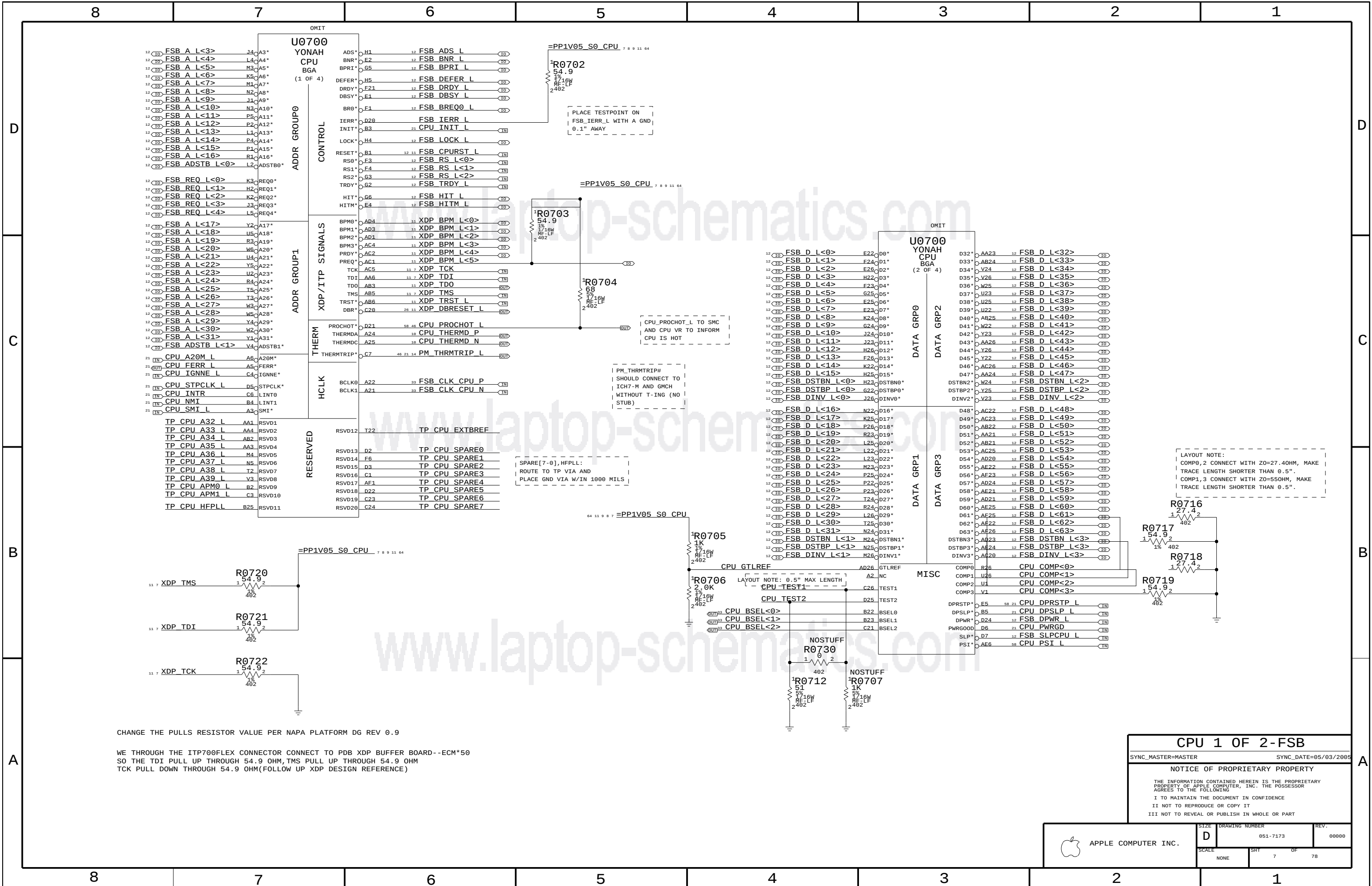
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SCALE	SHT	OF
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NONE	5	78
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CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB

SYNC_MASTER=MASTER

SYNC_DATE=05/03/2005

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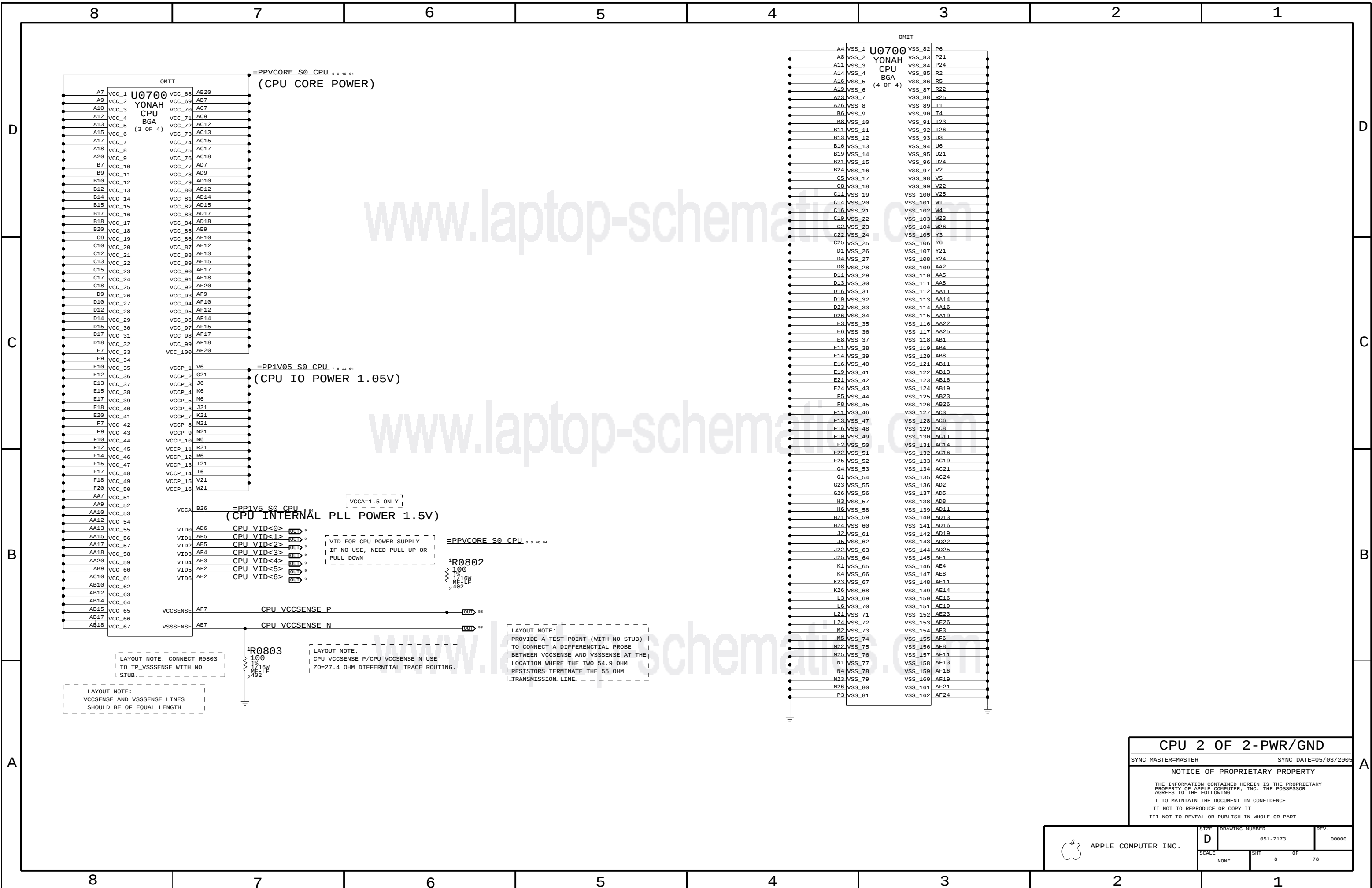
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SHT 7

OF 78



CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER

SYNC_DATE=05/03/2005

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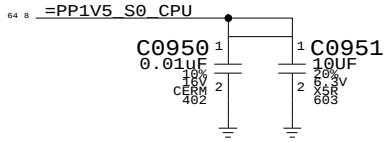
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REV.: 00000

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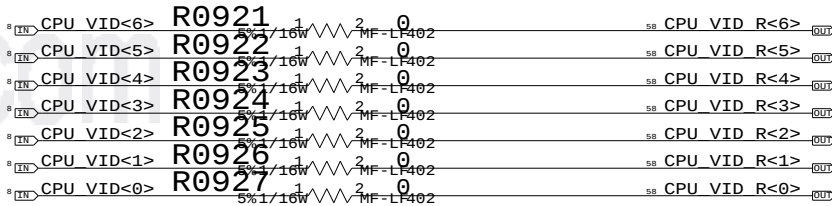
OF 78

VCCA DECOUPLING
(CPU INTERNAL PLL POWER 1.5V)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602	?	ALL	USE SAMSUNG AND MURATA ONLY

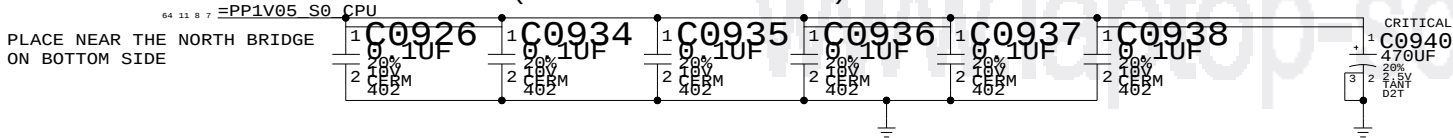
CPU CORE VID<> SETTINGS



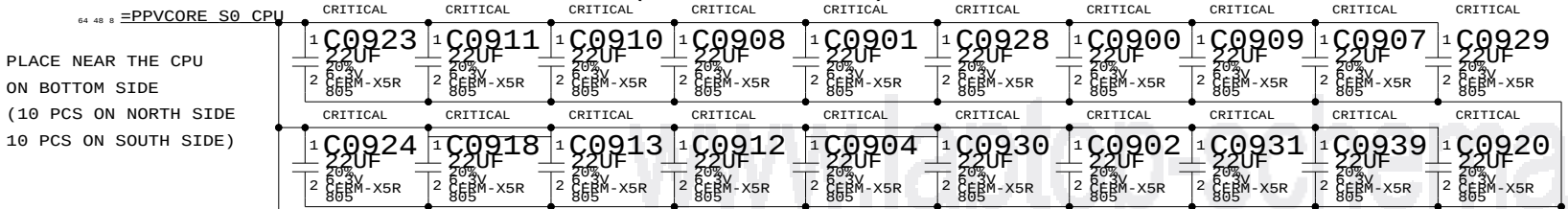
R0921-R0927 FOR CPU VOLTAGE MANUAL SETTING

VCCP CORE DECOUPLING
(CPU IO POWER 1.05V)

THIS 470UF FOR CPU, GMCH FSB BUS 1.05V

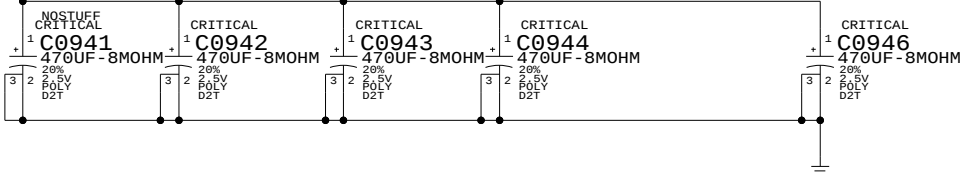


VCC CORE DECOUPLING
(CPU CORE POWER)



IF WE USE LOW ESL CAP, THEN WE CAN USE 20 PCS 22UF CAP

(2 PCS ON NORTH SIDE
2 PCS ON SOUTH SIDE)



	MIN	TYP	MAX
DUAL CORE SV CPU	VCCHFM 1.1625		1.30
	VCCLFM TBD		TBD
SINGLE CORE SV CPU	VCCHFM 1.1625		1.30
	VCCLFM TBD		TBD
DUAL CORE LV CPU	VCCHFM 1.0		1.1625
	VCCLFM TBD		TBD
ULV CPU	VCCHFM TBD		TBD
	VCCLFM TBD		TBD

UNIT: V

- # ALL PROCESSOR DEFAULT VCORE FOR INITIAL POWER UP IS 1.2V
- # TWO PROCESSORS AT THE SAME FREQUENCY MAY HAVE DIFFERENT SETTING WITH THE VID RANGE(VCORE VOLTAGE)!
- # REFER TO YONAH PROCESSOR EMTS REV 1.0
- # VCCHFM: VCORE AT HIGHEST FREQUENCY MODE
- # VCCLFM: VCORE AT LOWEST FREQUENCY MODE

CPU DECAPS & VID<>

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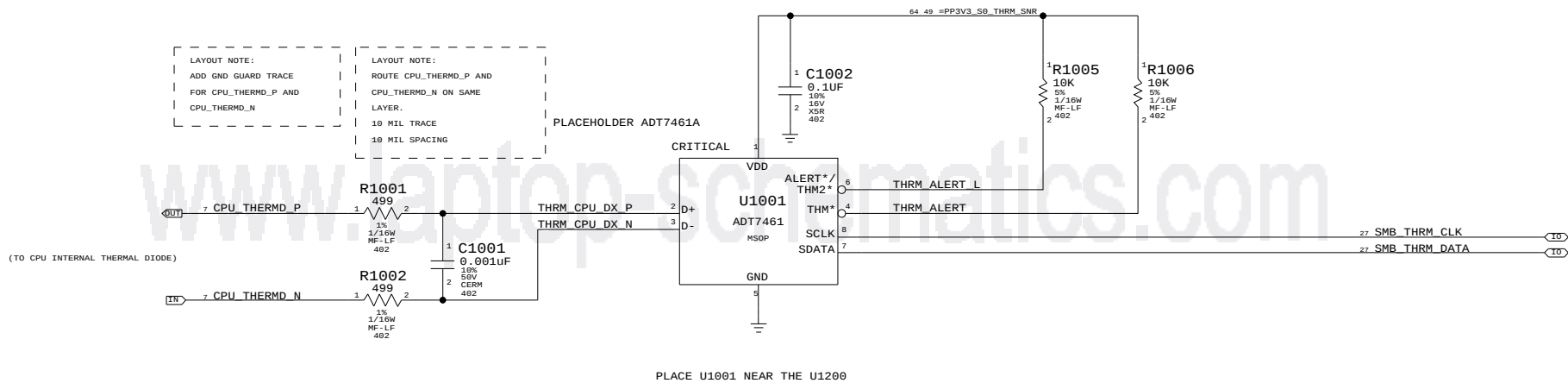


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NONE	9	78

www.laptop-schematics.com

CPU ZONE THERMAL SENSOR



CPU MISC1-TEMP SENSOR

SYNC_MASTER=ENET SYNC_DATE=08/19/2005

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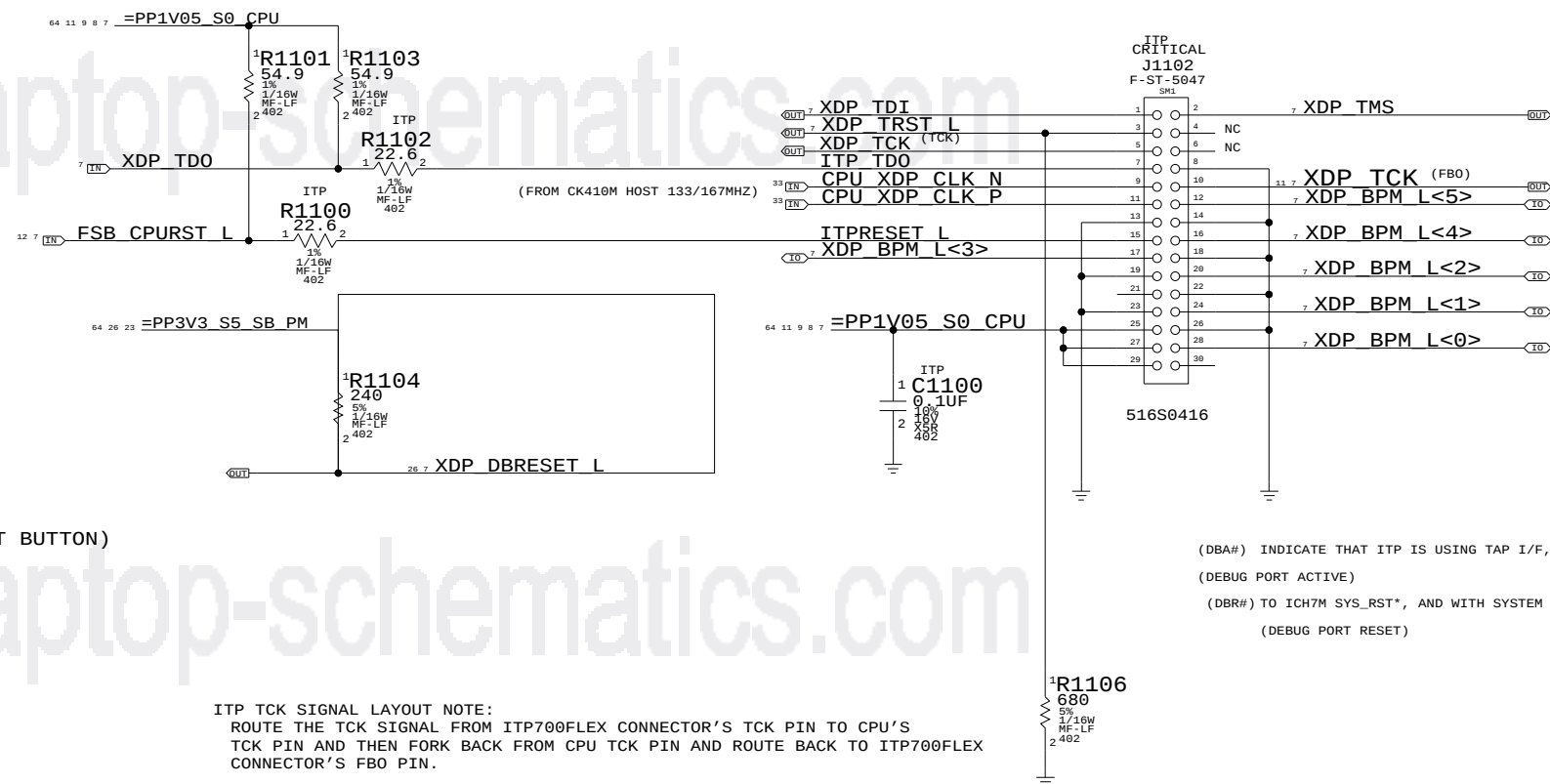
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NONE	10	78

CPU ITP700FLEX DEBUG SUPPORT



(AND WITH RESET BUTTON)

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S
TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX
CONNECTOR'S FBO PIN.

```
(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.
(DEBUG PORT ACTIVE)
(DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC
(DEBUG PORT RESET)
```

CPU ITP700FLEX DEBUG

SYNC_MASTER=MASTER	SYNC_DATE=5/23/05
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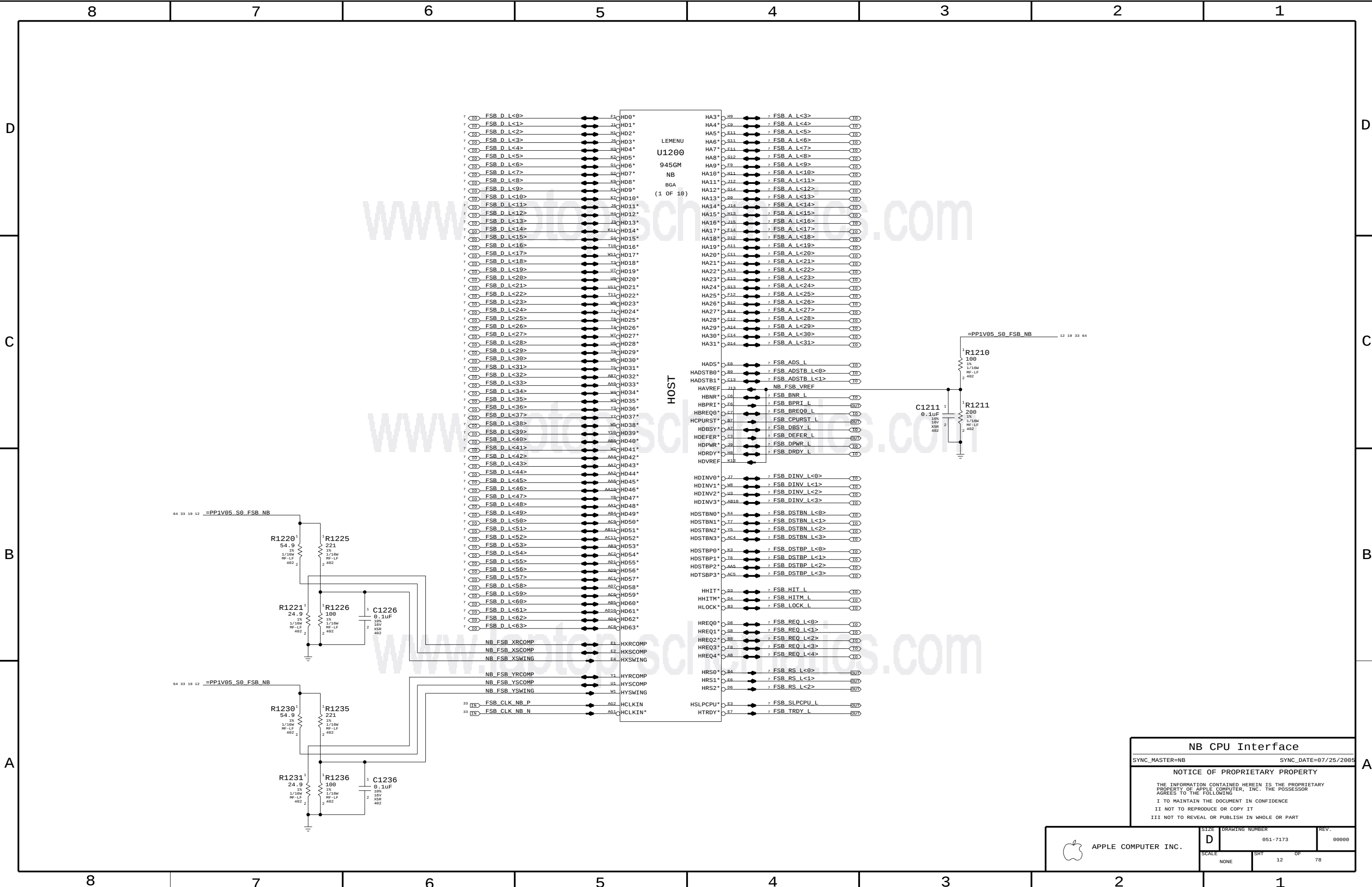
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NONE	11	78



NB CPU Interface

SYNC_MASTER=NB SYNC_DATE=07/25/2005

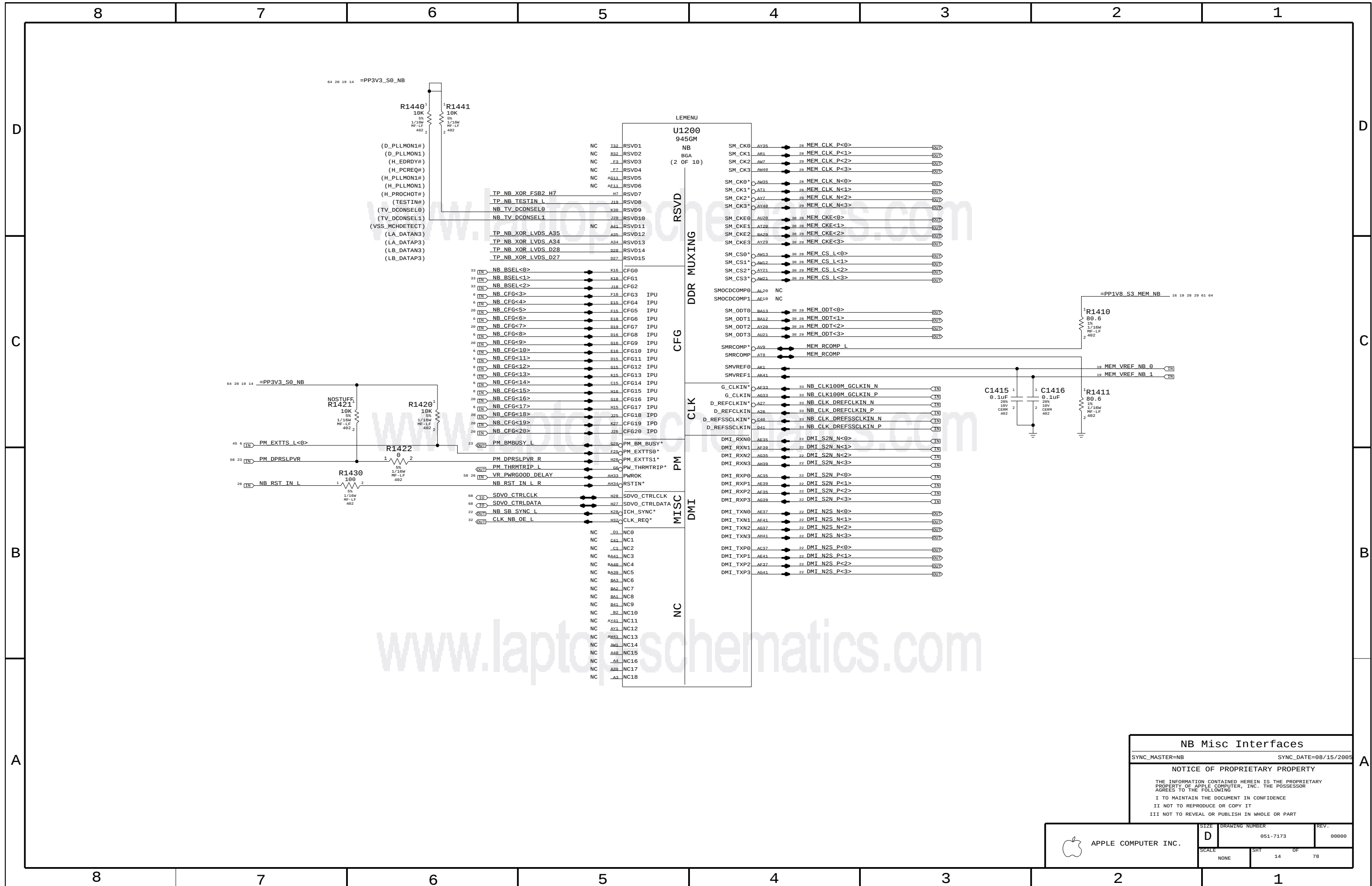
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NB Misc Interf

SYNC_MASTER=NB SYNC_DATE=08/15/2005

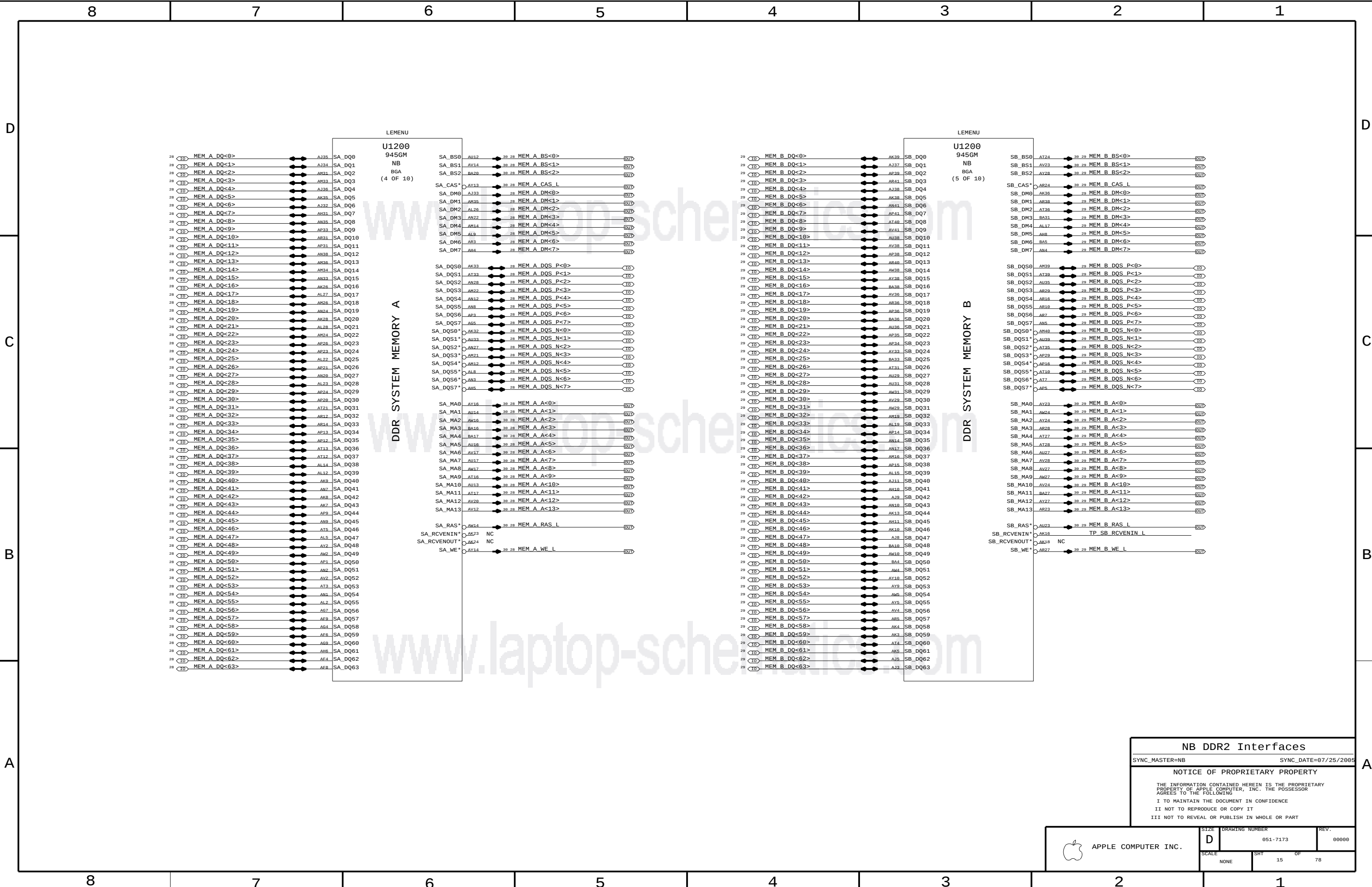
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NB DDR2 Interfaces

SYNC_MASTER=NB

SYNC_DATE=07/25/2005

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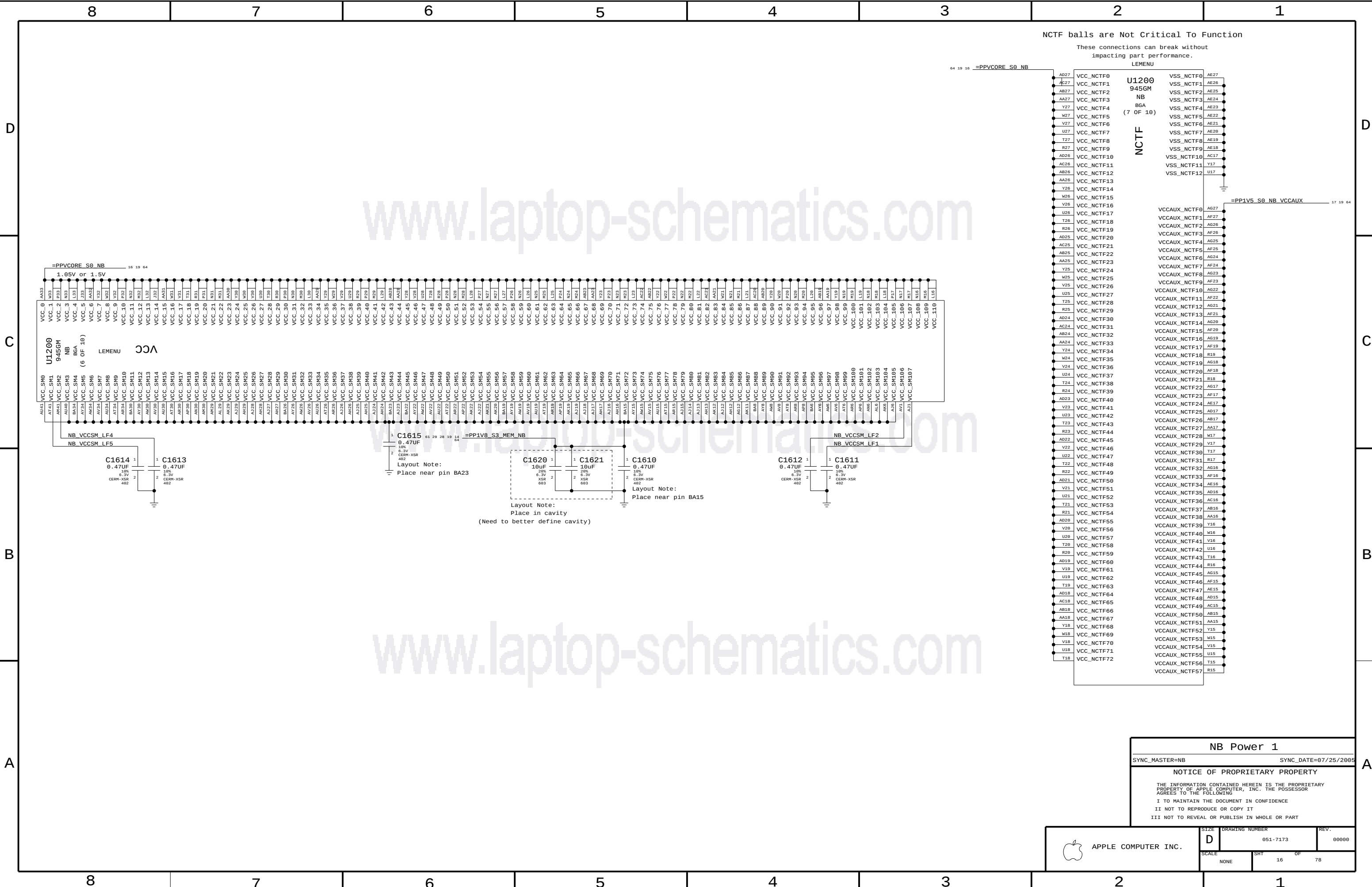
SCALE: NONE

DRAWING NUMBER: 051-7173

REV.: 00000

SHT: 15

OF: 78



APPLE COMPUTER INC.

SCALE: NONE

DRAWING NUMBER: 051-7173

REV: 00000

SIZE: D

SHT: 16 OF 78

NB Power 1

SYNC_MASTER=NB SYNC_DATE=07/25/2005

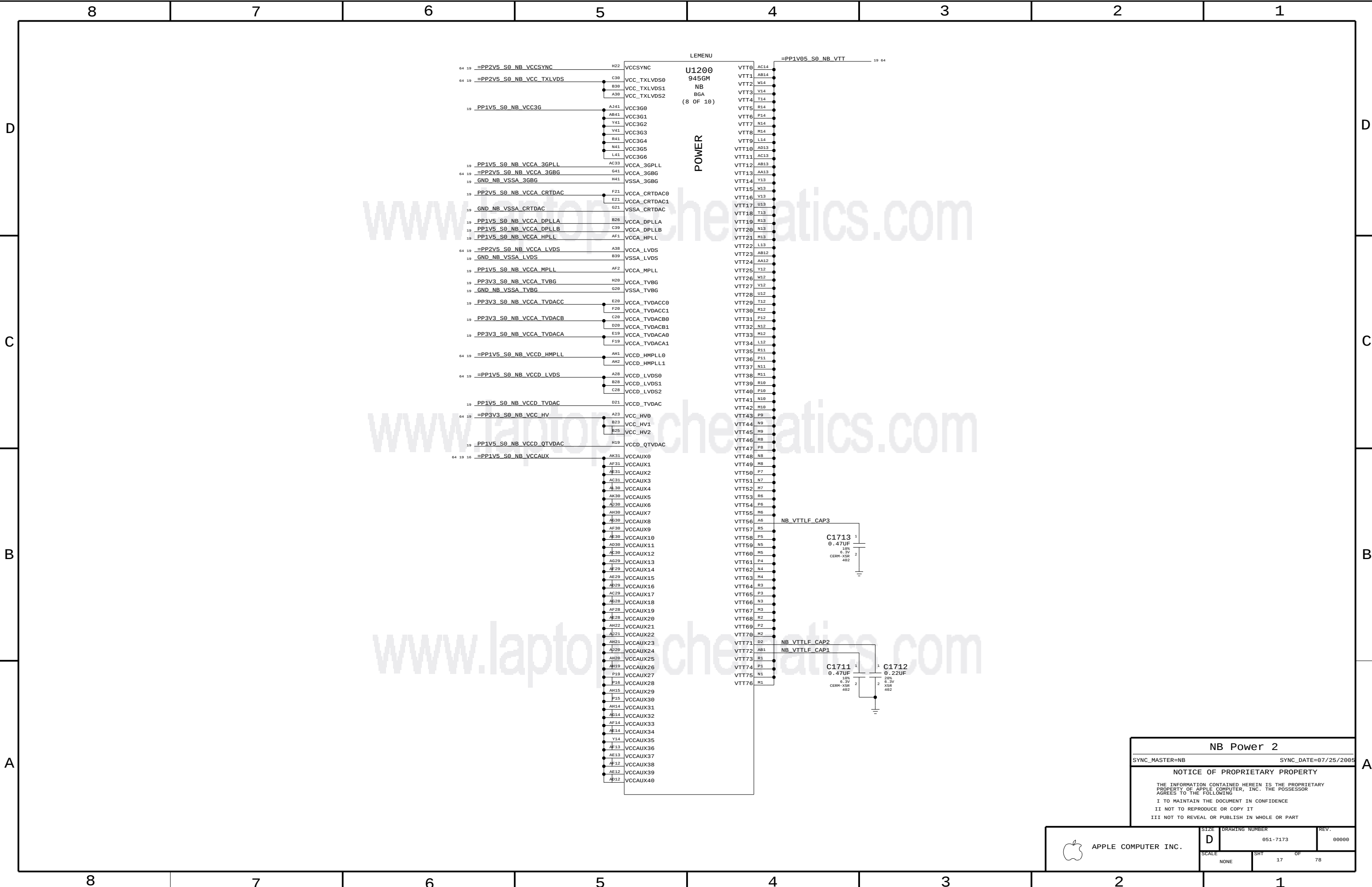
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NB Power 2

SYNC_MASTER=NB

SYNC_DATE=07/25/2005

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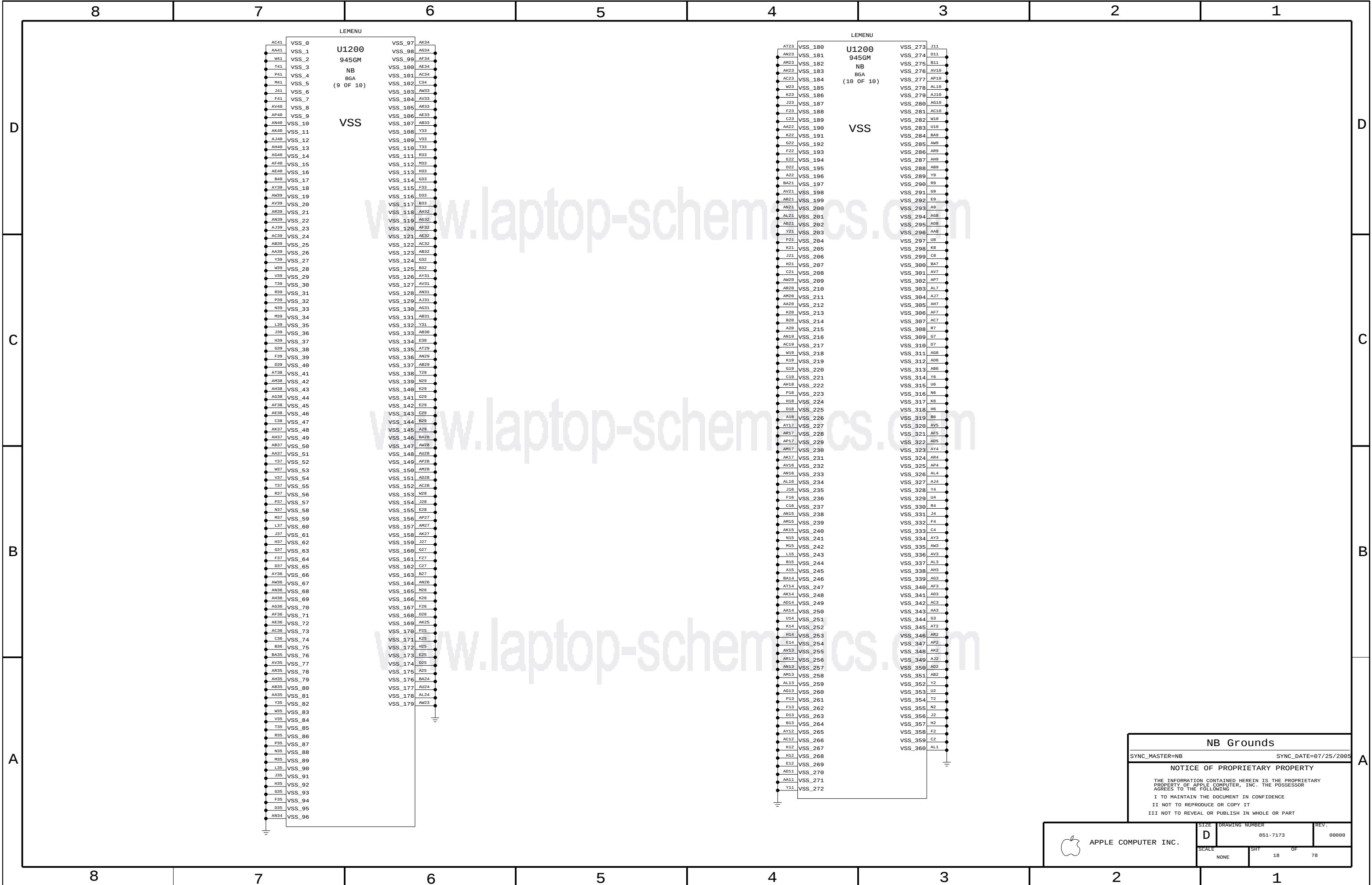
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	D	051-7173	00000
SCALE		SHT	
NONE		17 OF 78	



NB Grounds

SYNC_MASTER=NB SYNC_DATE=07/25/2005

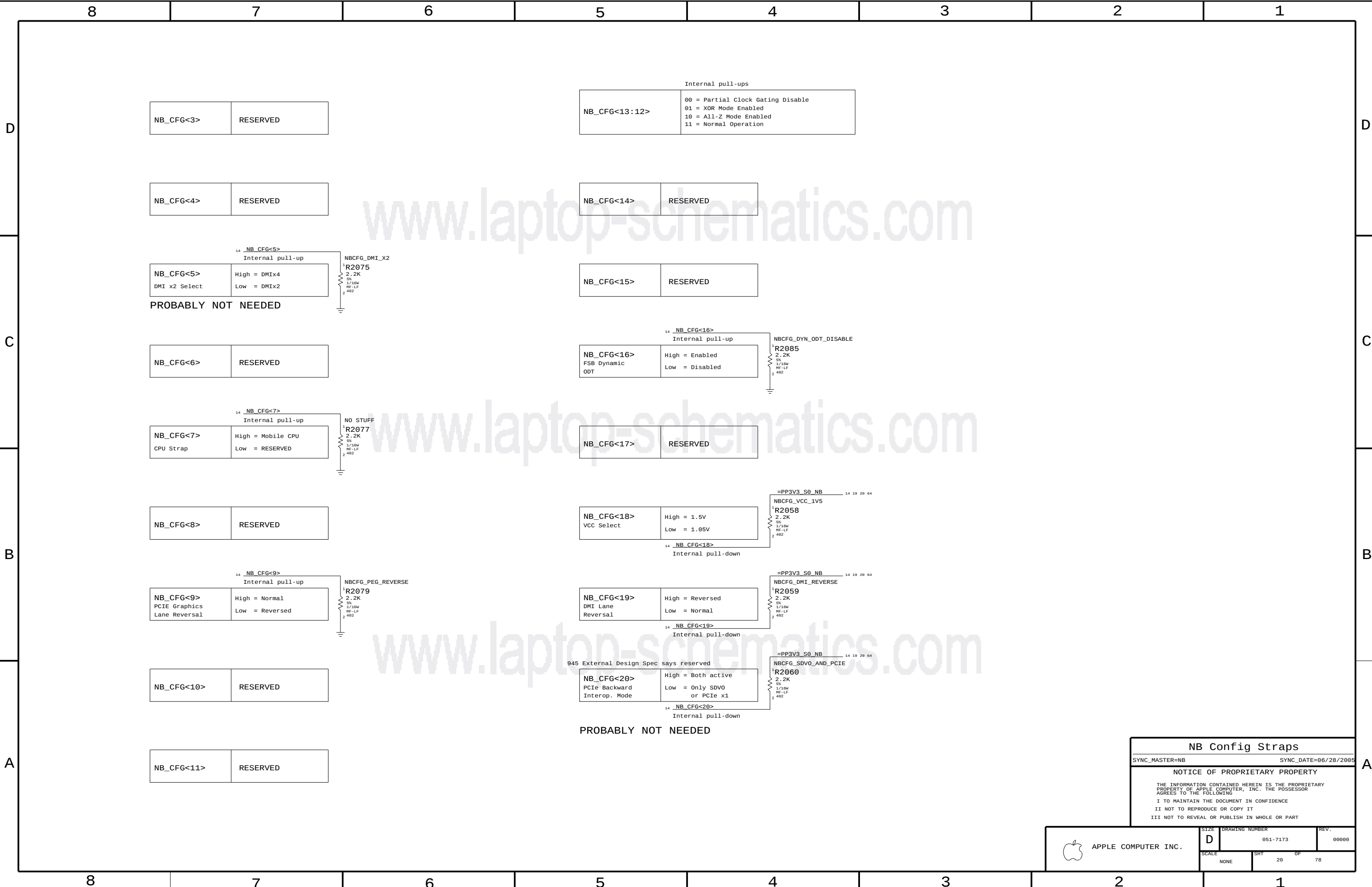
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NB Config Straps

SYNC_MASTER=NB

SYNC_DATE=06/28/2005

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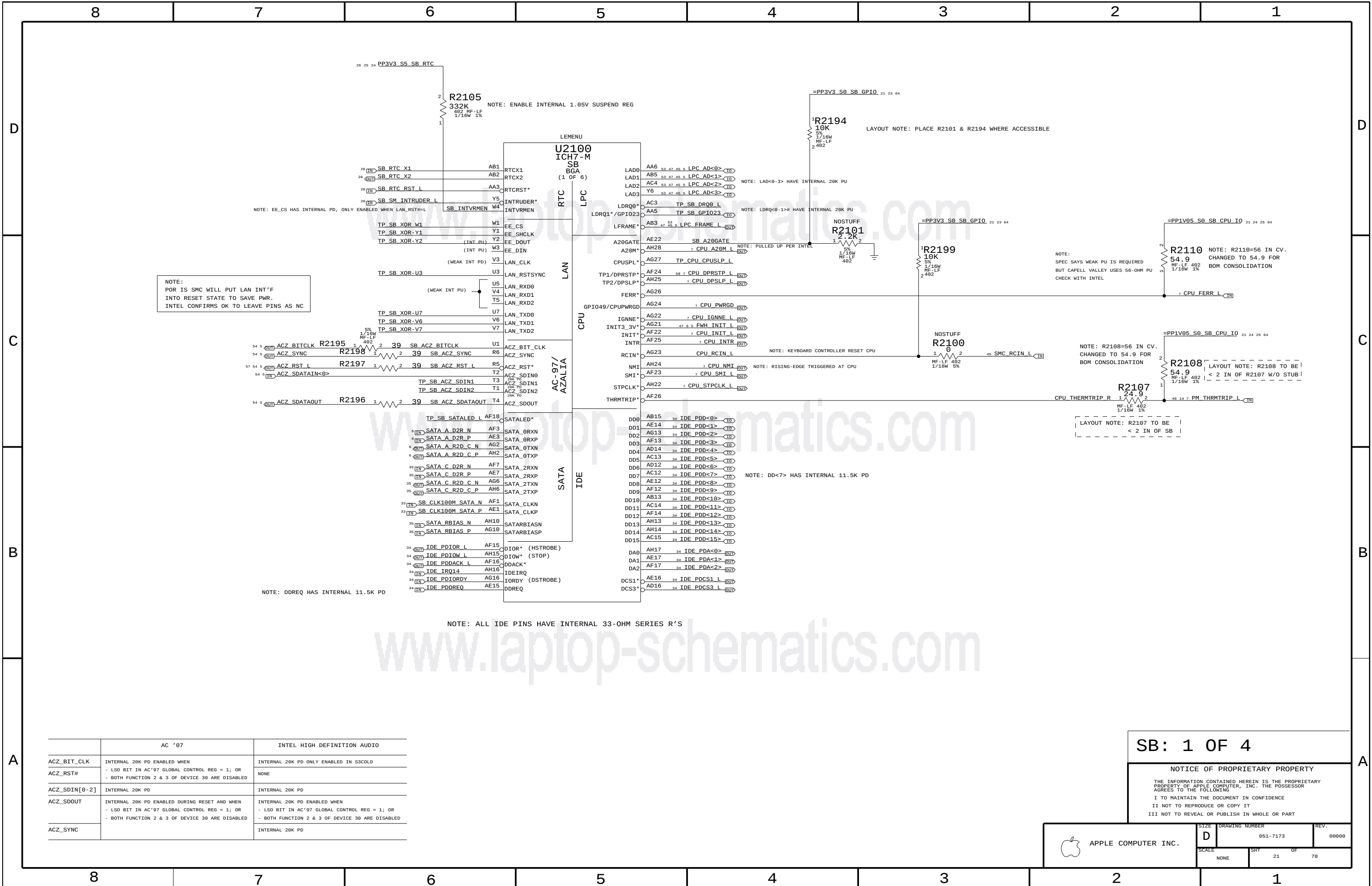
SIZE: D

DRAWING NUMBER: 051-7173

REV.: 00000

SHT: 20

OF: 78



	AC '97	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

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D

DRAWING NUMBER

051-7173

REV.

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SCALE

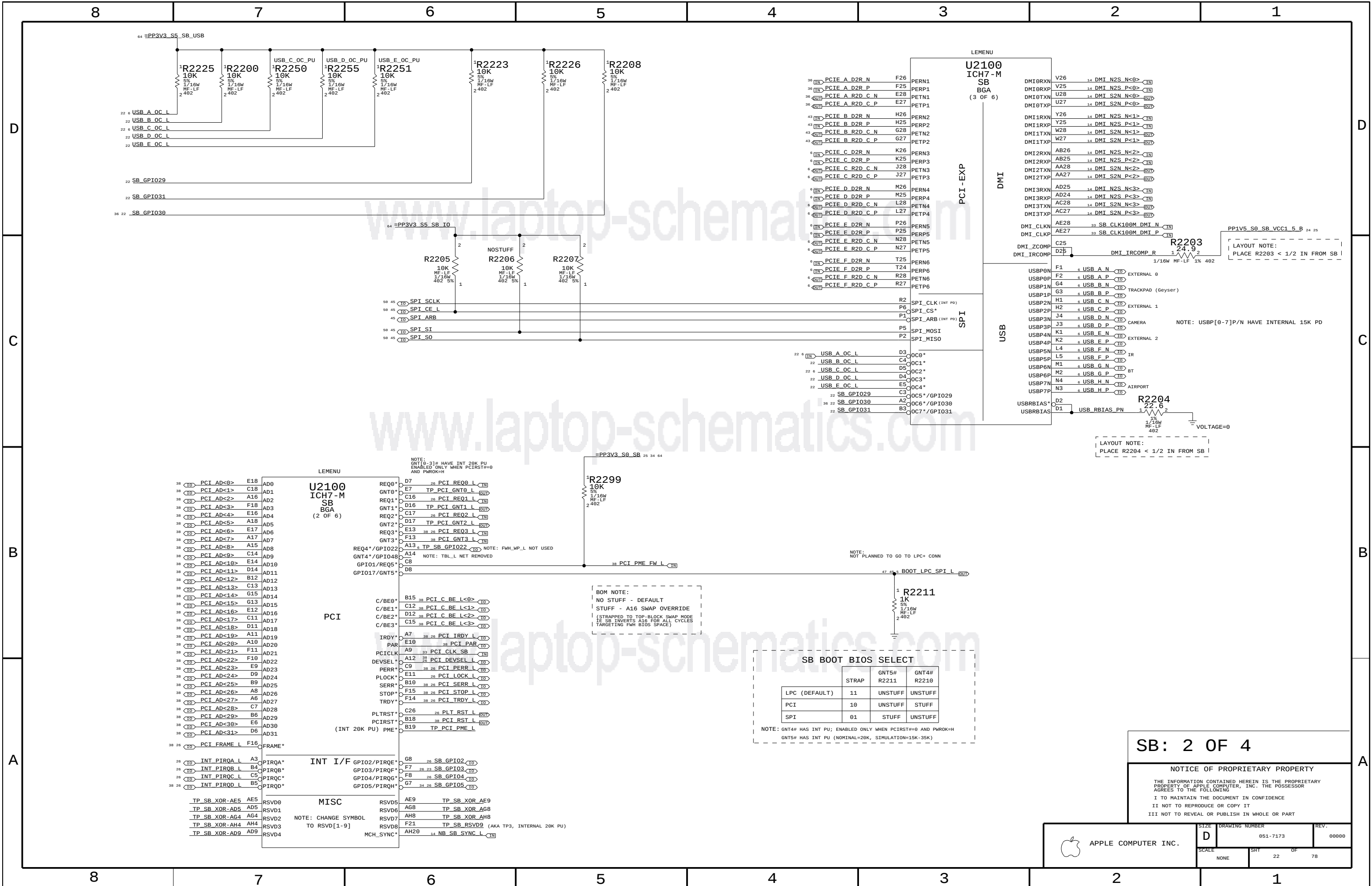
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SHT

21

OF

78



SB: 2 OF 4

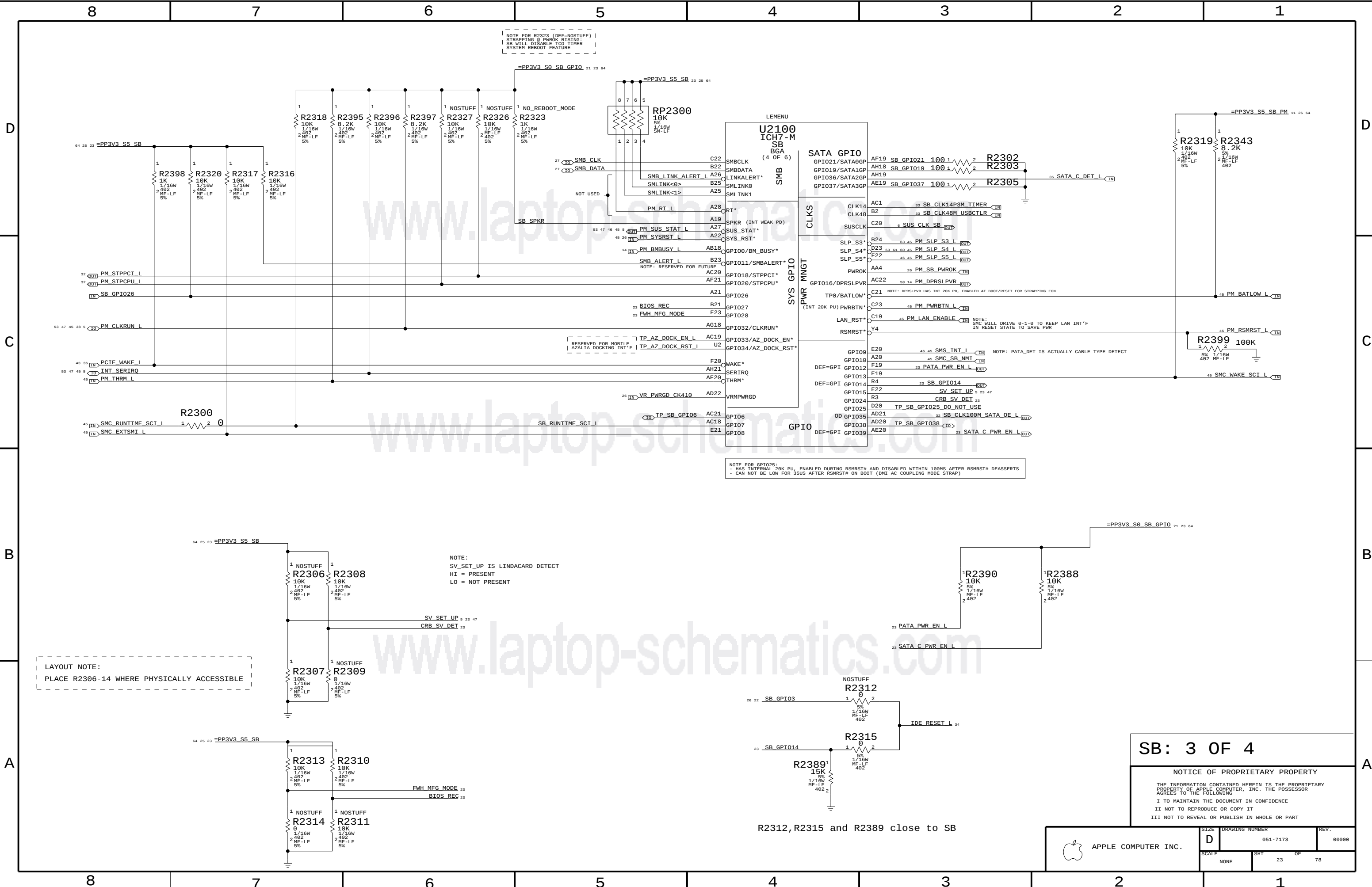
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SCALE	SHT	OF
NONE	22	78



NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DML AC COUPLING MODE STRAP)

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

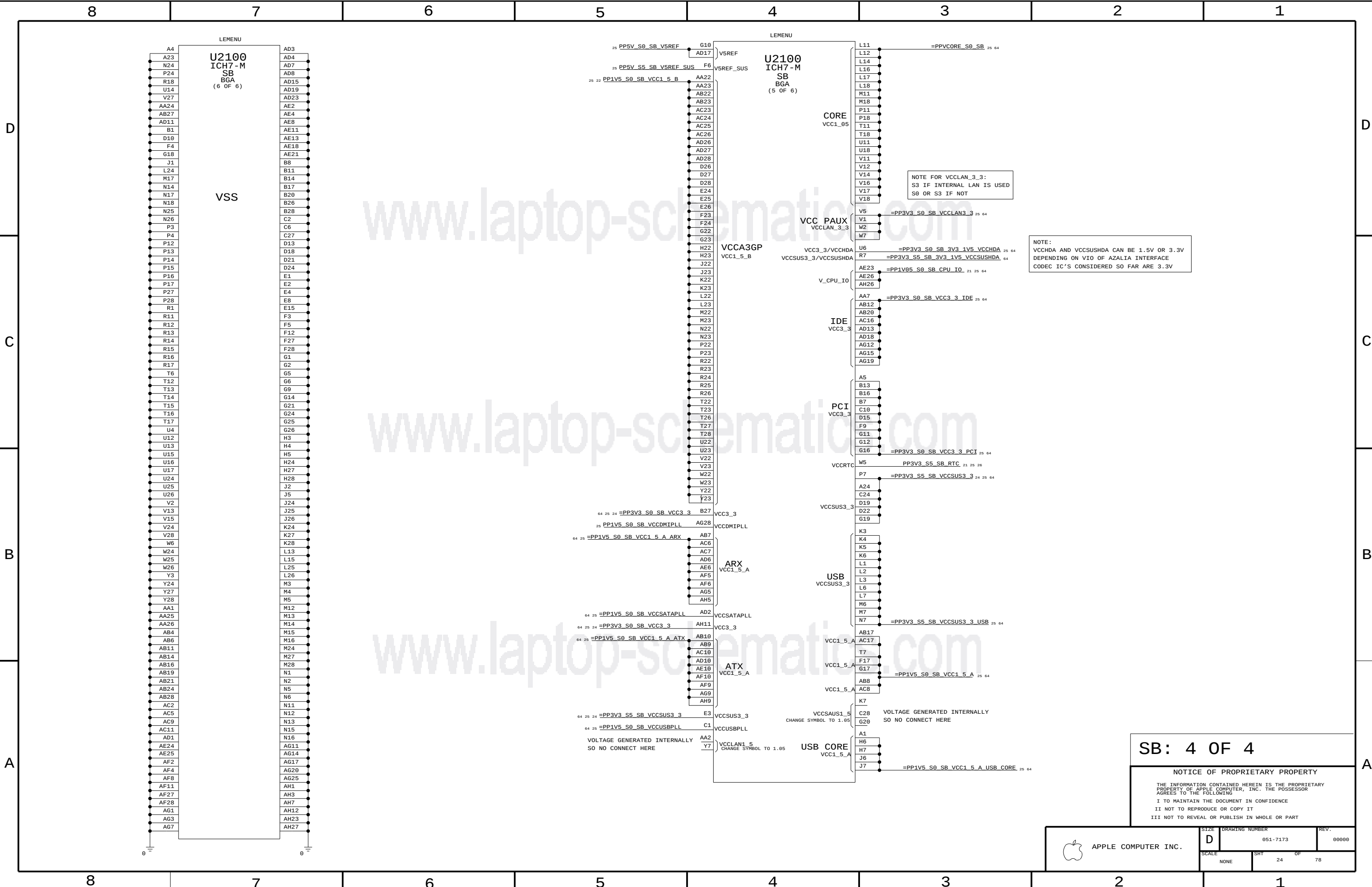
R2312, R2315 and R2389 close to SB

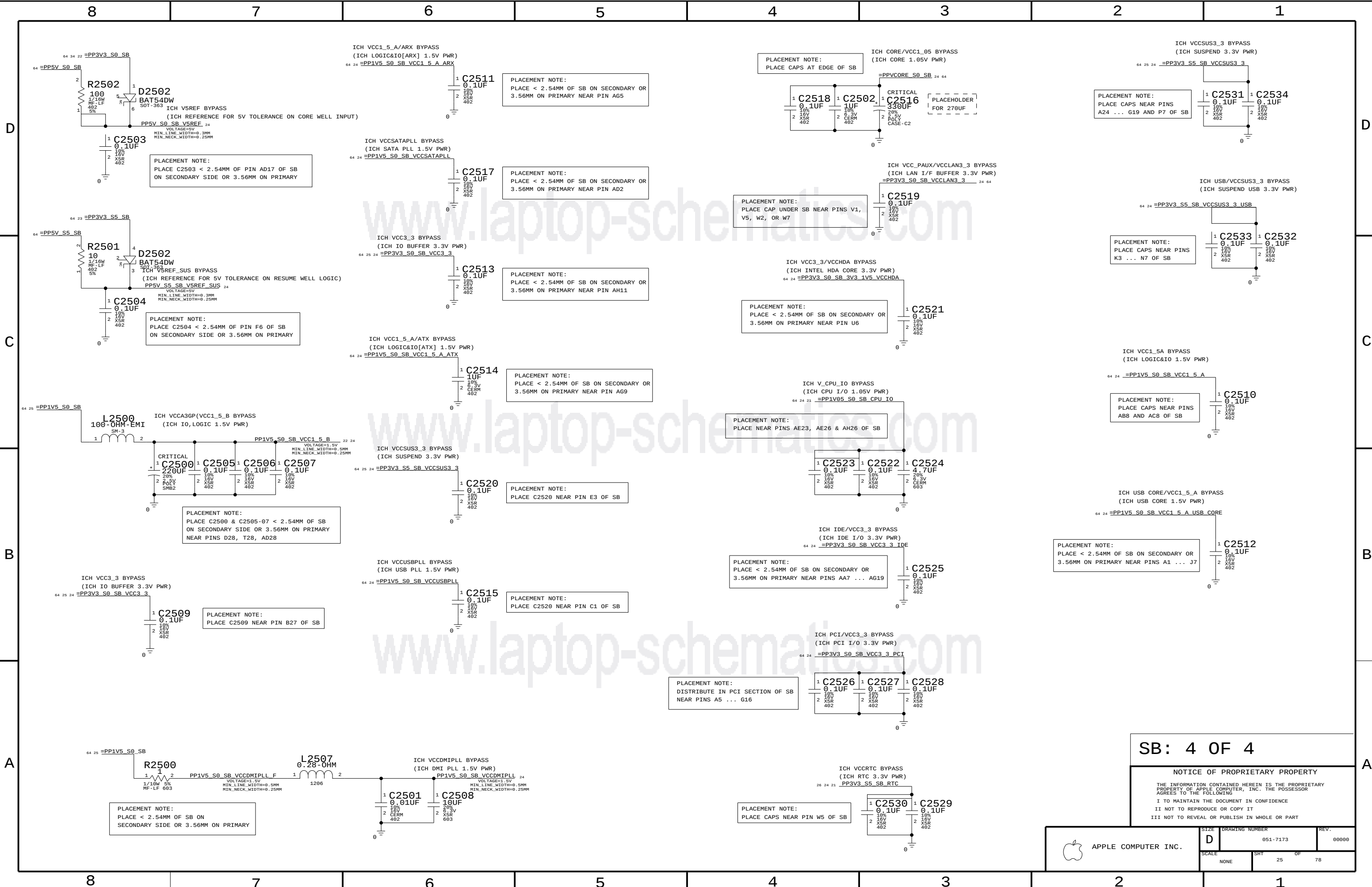
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	SHT	23	OF 78





SB: 4 OF 4

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHT	25	OF 78

D

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B

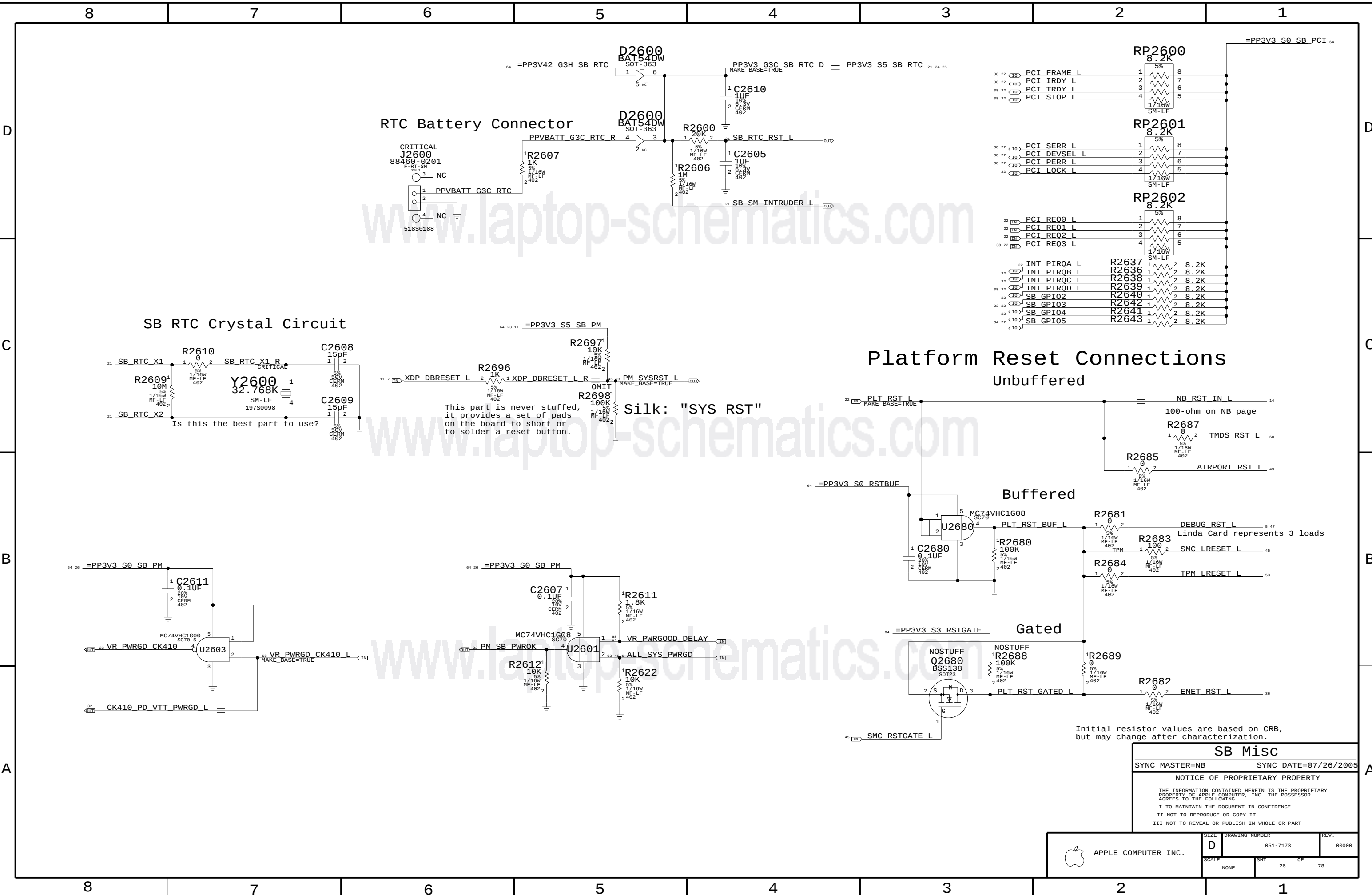
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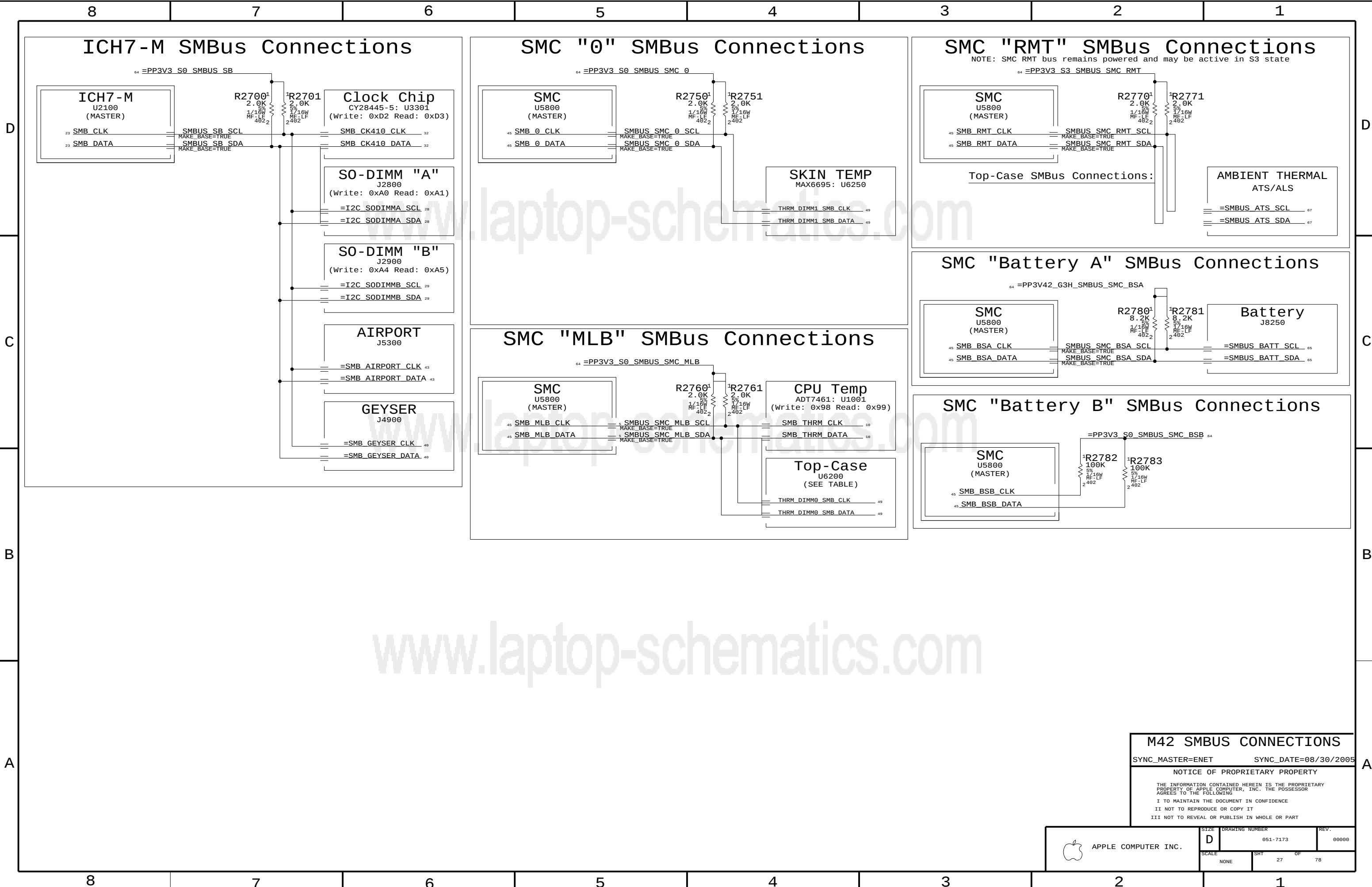
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B

A





M42 SMBUS CONNECTIONS

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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SIZE DRAWING NUMBER REV.

D

051-7173

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SCALE

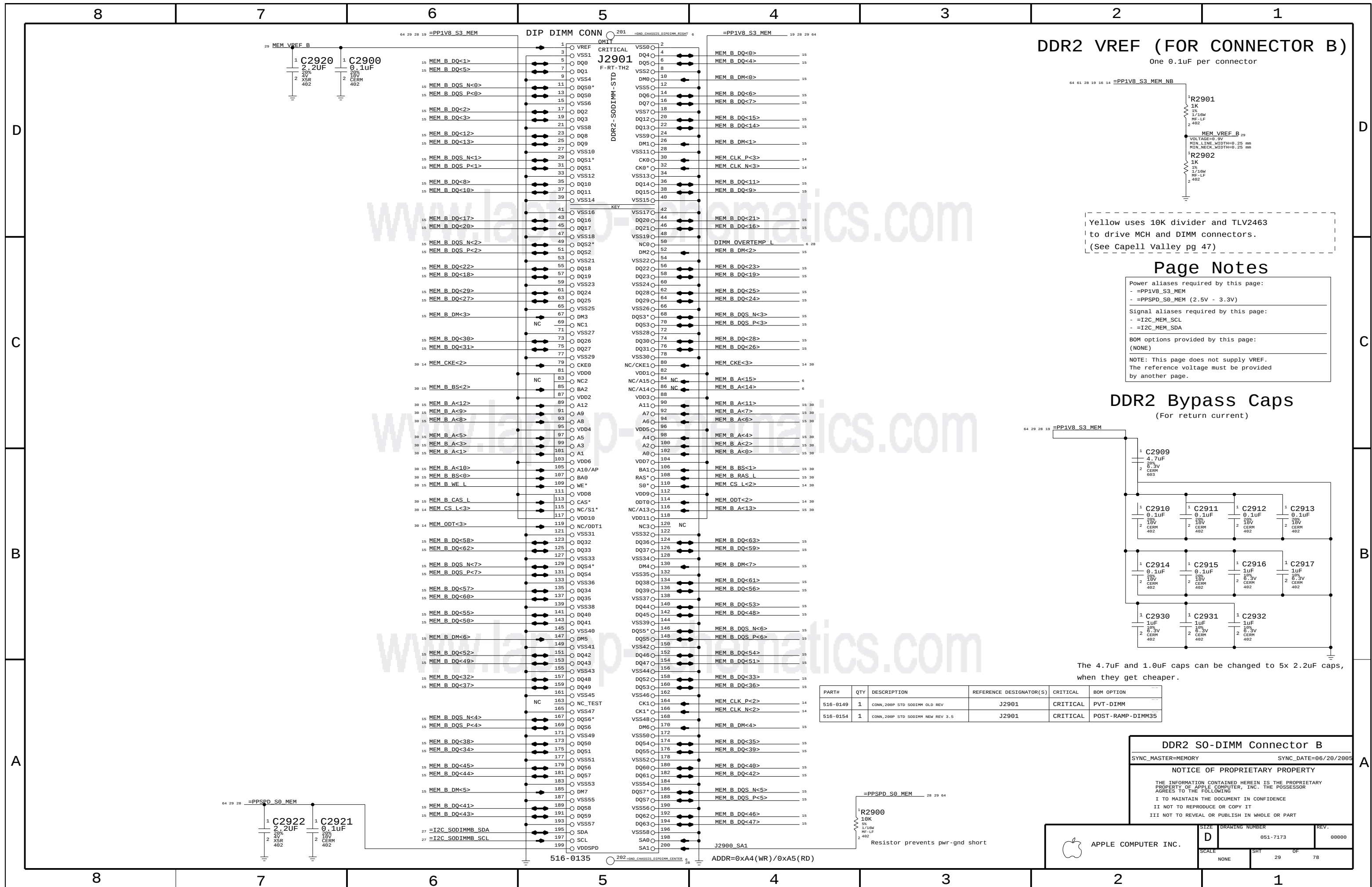
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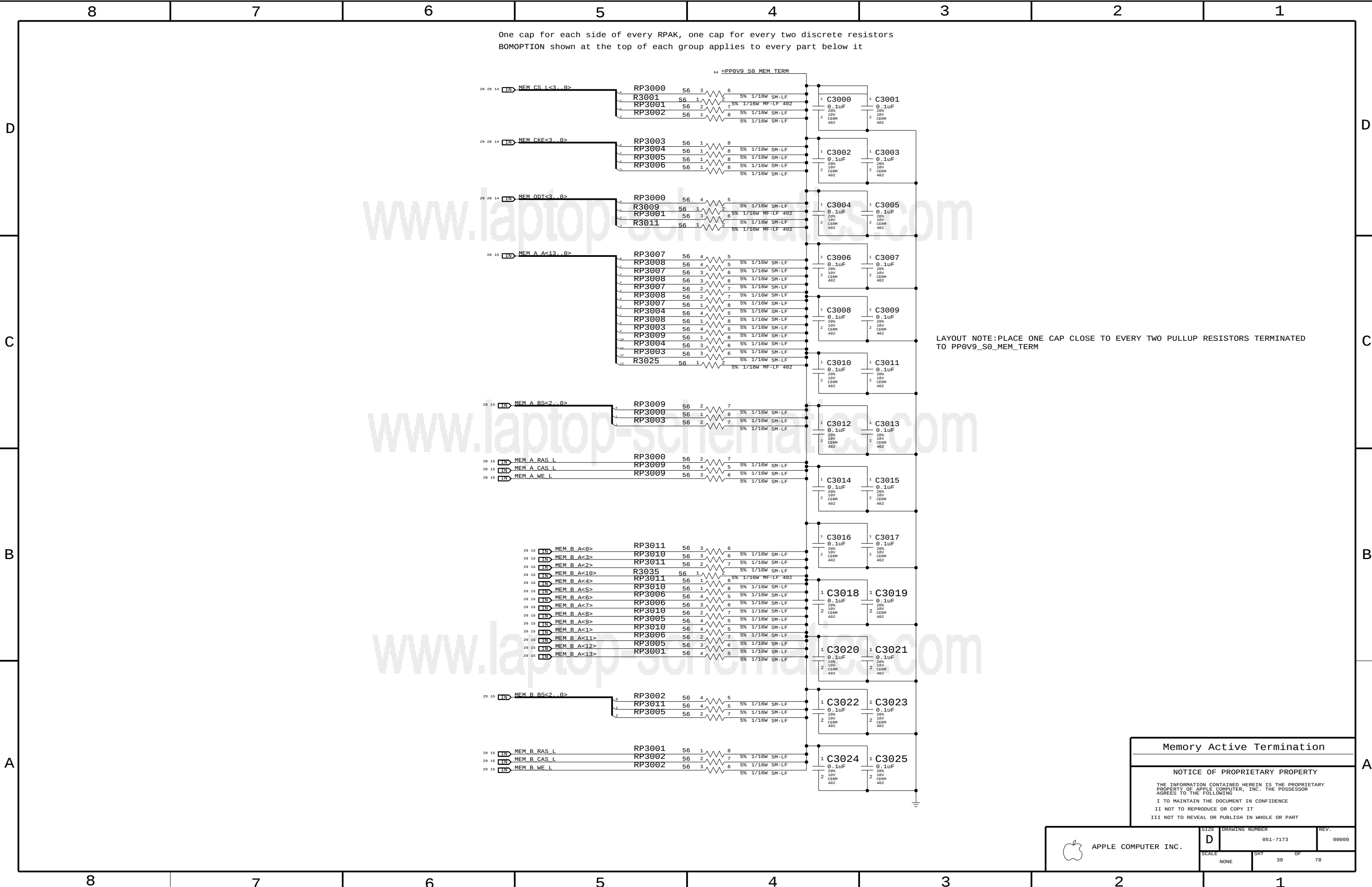
SHT

27

OF

78





Memory Active Termination

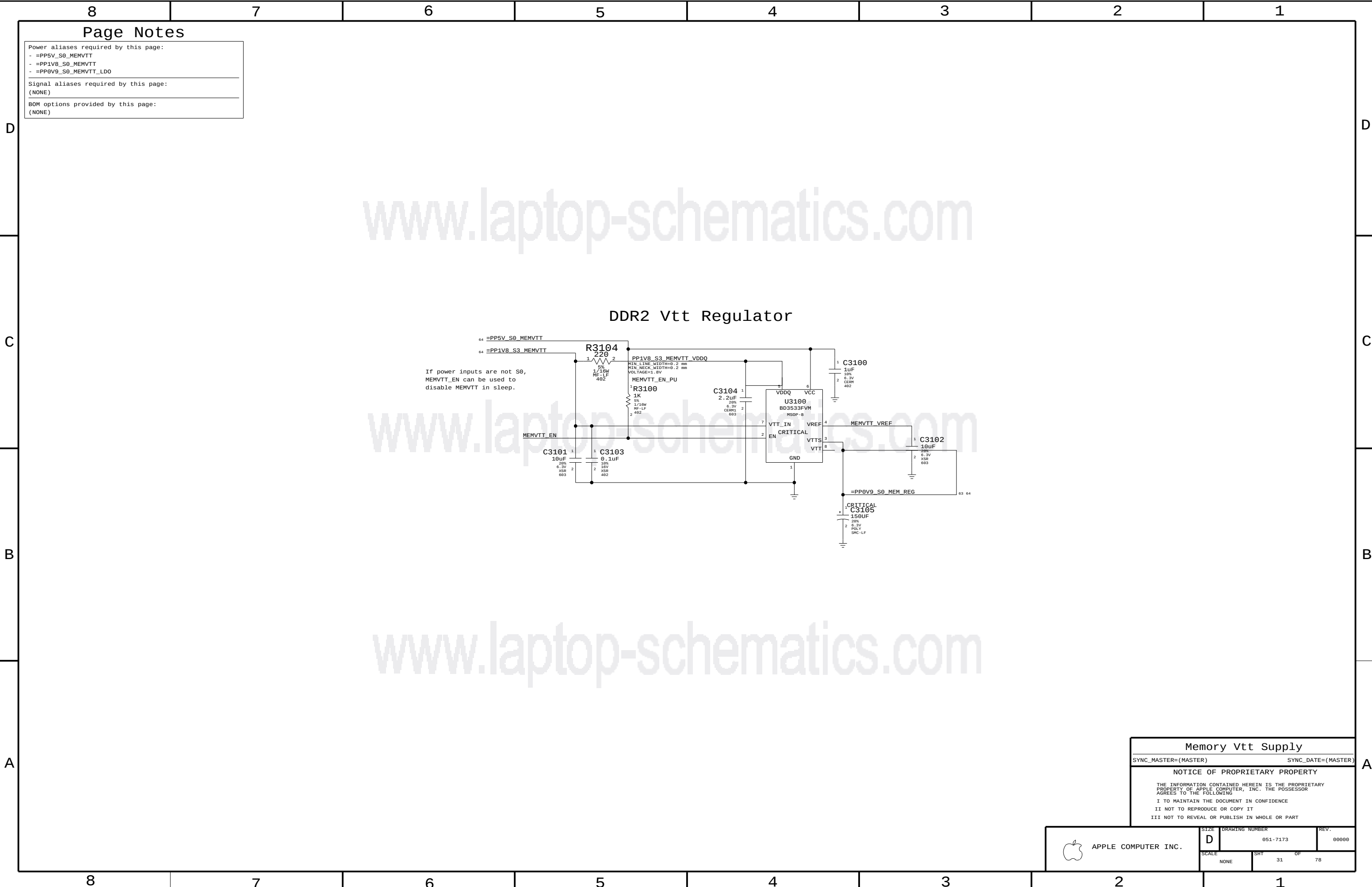
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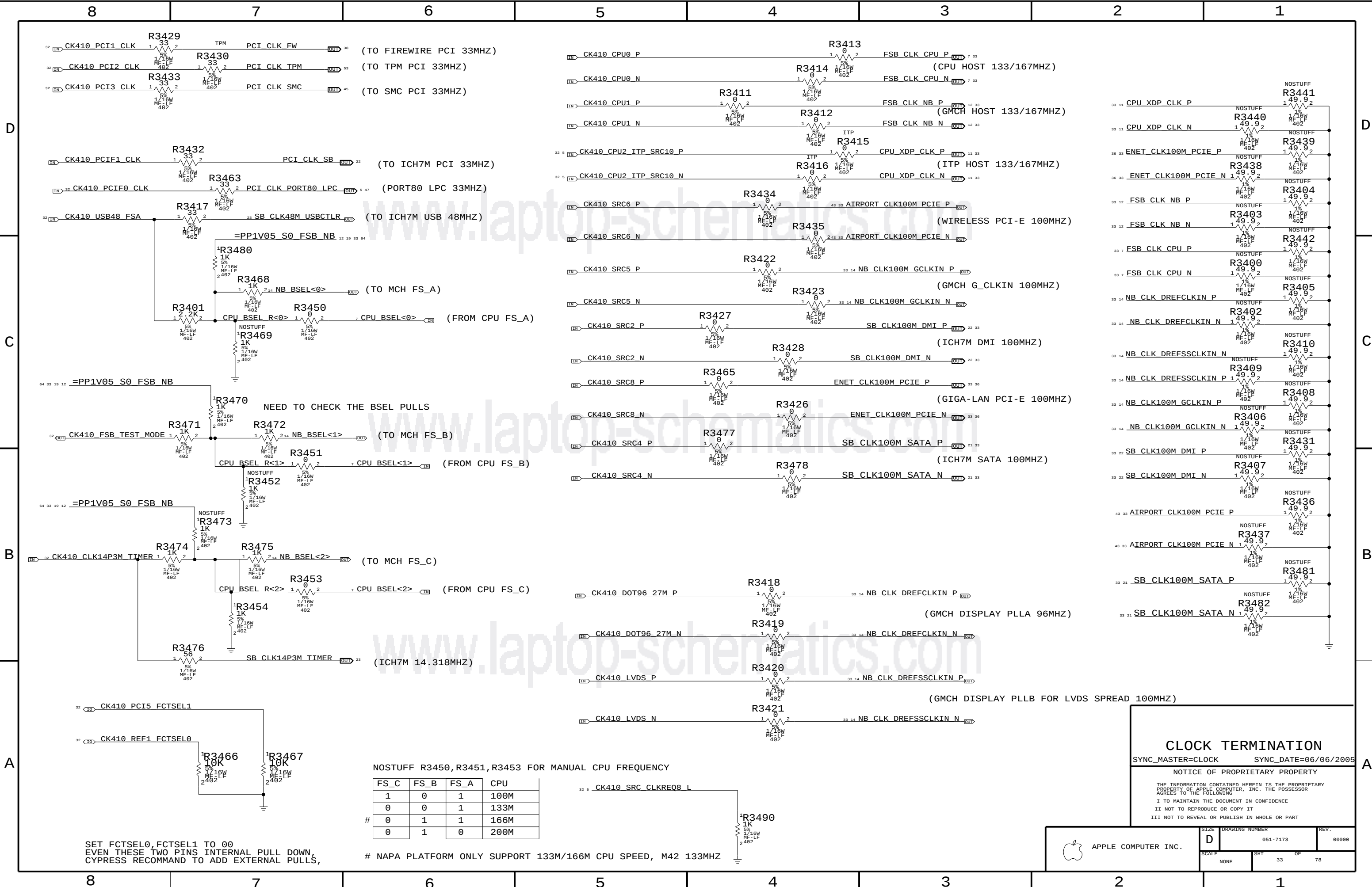
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NOSTUFF R3450, R3451, R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	1	0	1	100M
	0	0	1	133M
#	0	1	1	166M
	0	1	0	200M

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED, M42 133MHZ

SET FCTSEL0, FCTSEL1 TO 00
EVEN THESE TWO PINS INTERNAL PULL DOWN,
CYPRESS RECOMMEND TO ADD EXTERNAL PULLS,

CLOCK TERMINATION

SYNC_MASTER=CLOCK SYNC_DATE=06/06/2005

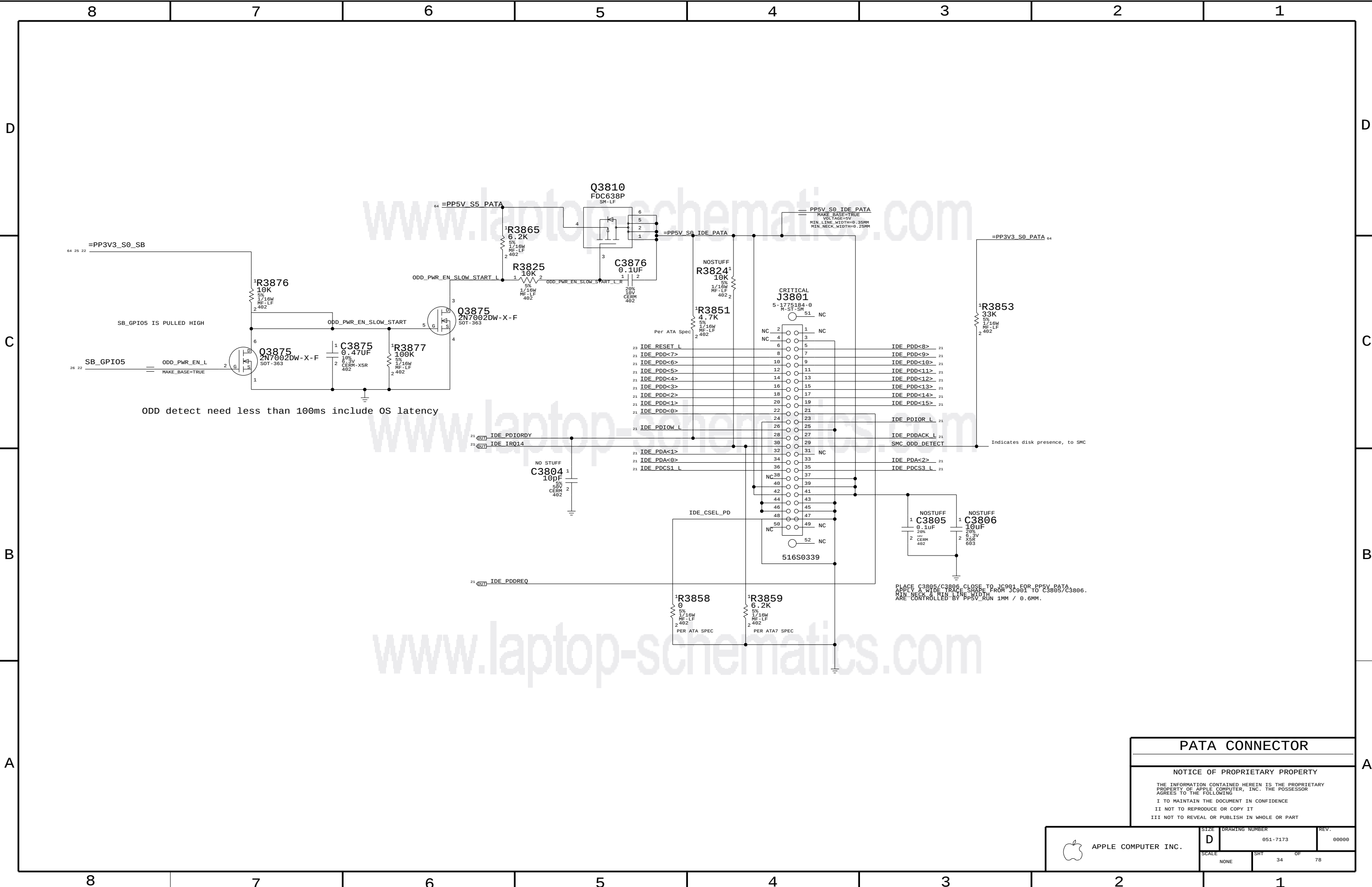
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D	051-7173	00000
SCALE	SHT	OF
NONE	33	78



PATA CONNECTOR

NOTICE OF PROPRIETARY PROPERTY

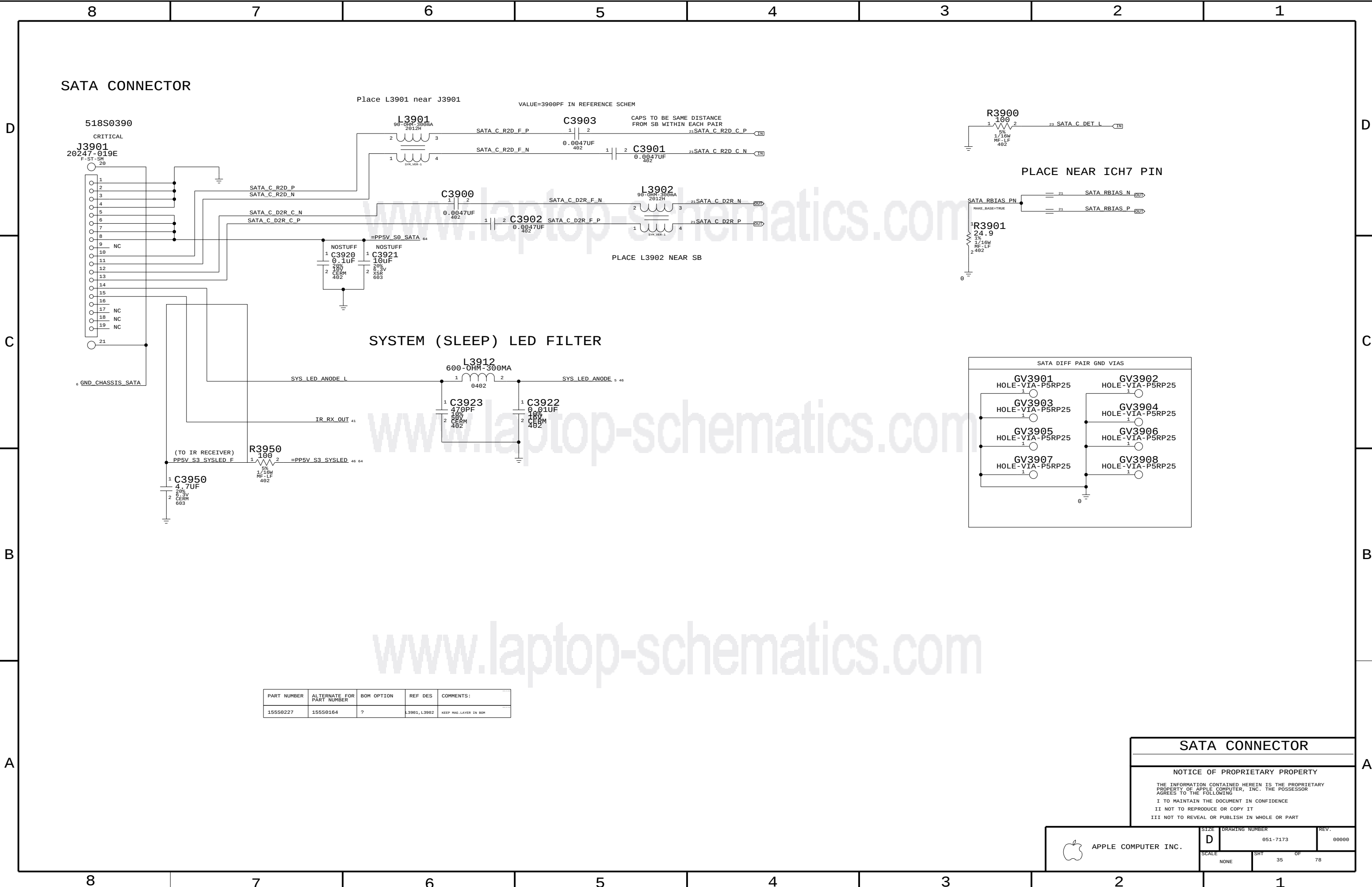
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SCALE		SHT	OF
NONE		34	78



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	L3901, L3902	KEEP MAG. LAYER IN BOM

SATA CONNECTOR

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APPLE COMPUTER INC.

SIZE D

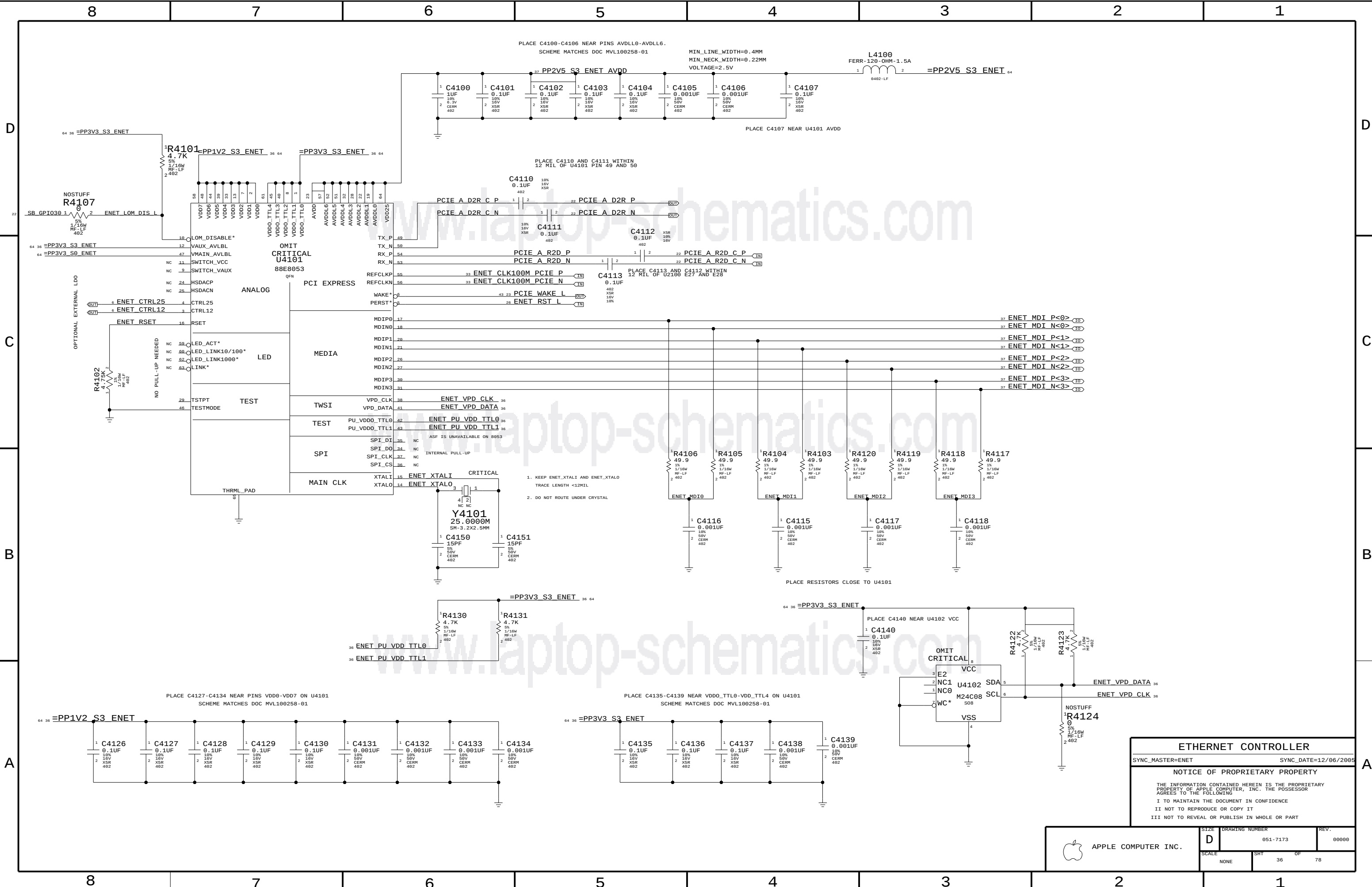
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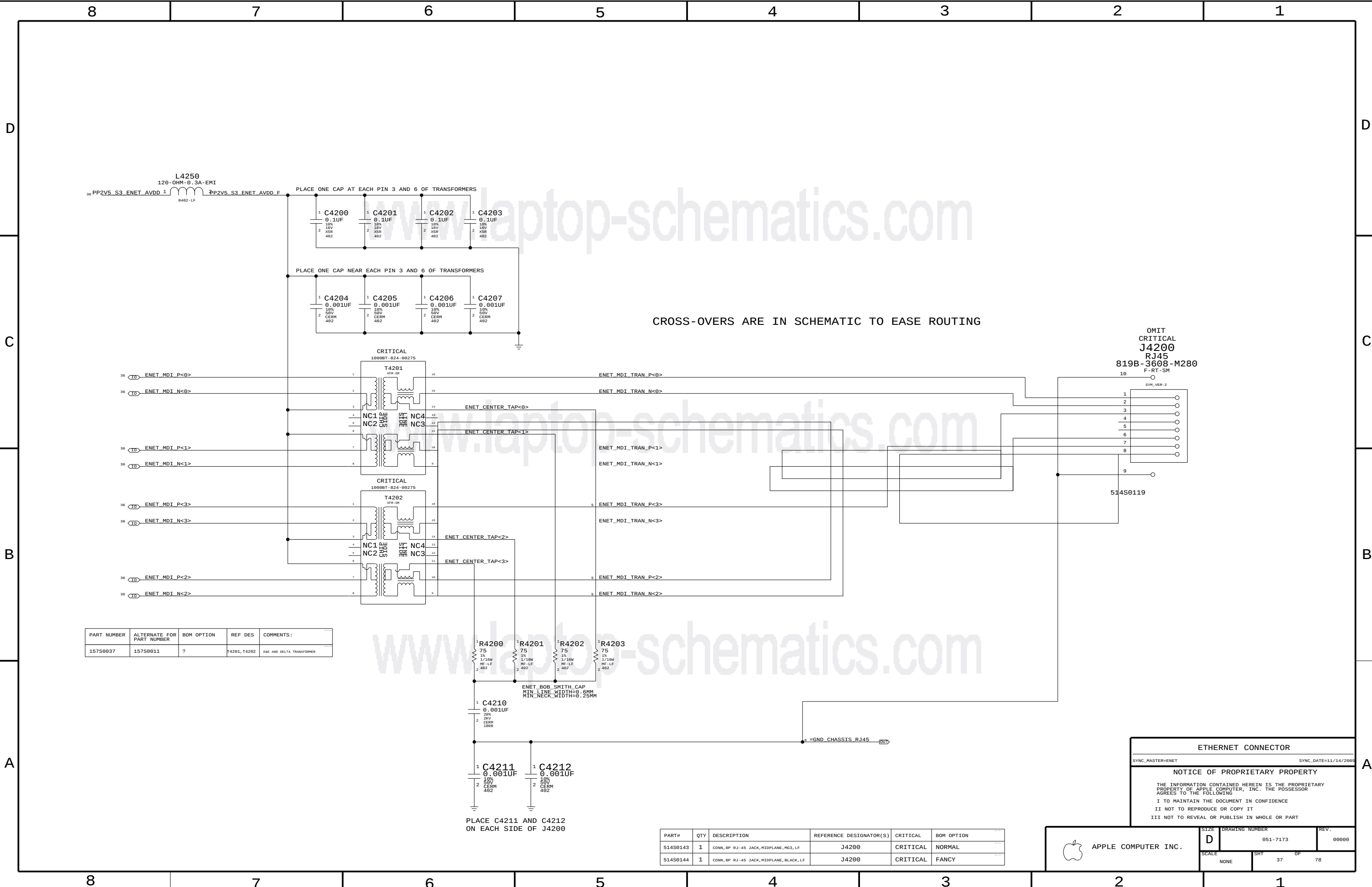
REV. 00000

SCALE NONE

SHT 35

OF 78





L4250
120-OHM-0.3A-EMI
PP2V5_S3_ENET_AVDD 1 6482-LF PP2V5_S3_ENET_AVDD_F

PLACE ONE CAP AT EACH PIN 3 AND 6 OF TRANSFORMERS

PLACE ONE CAP NEAR EACH PIN 3 AND 6 OF TRANSFORMERS

CROSS-OVERS ARE IN SCHEMATIC TO EASE ROUTING

OMIT
CRITICAL
J4200
RJ45
819B-3608-M280
F-RT-SM
10
STR_VER-2

514S0119

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0037	157S0011	?	T4201, T4202	SEE AND DELTA TRANSFORMER

ENET_BOB SMITH CAP
MIN LINE WIDTH=0.6MM
MIN NECK WIDTH=0.25MM

PLACE C4211 AND C4212
ON EACH SIDE OF J4200

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0143	1	CONN, BP RJ-45 JACK, MIDPLANE, M03, LF	J4200	CRITICAL	NORMAL
514S0144	1	CONN, BP RJ-45 JACK, MIDPLANE, BLACK, LF	J4200	CRITICAL	FANCY

ETHERNET CONNECTOR	
SYNC_MASTER=ENET	SYNC_DATE=11/14/2005
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SCALE		SHT	OF
NONE		37	78

PAGE NOTES

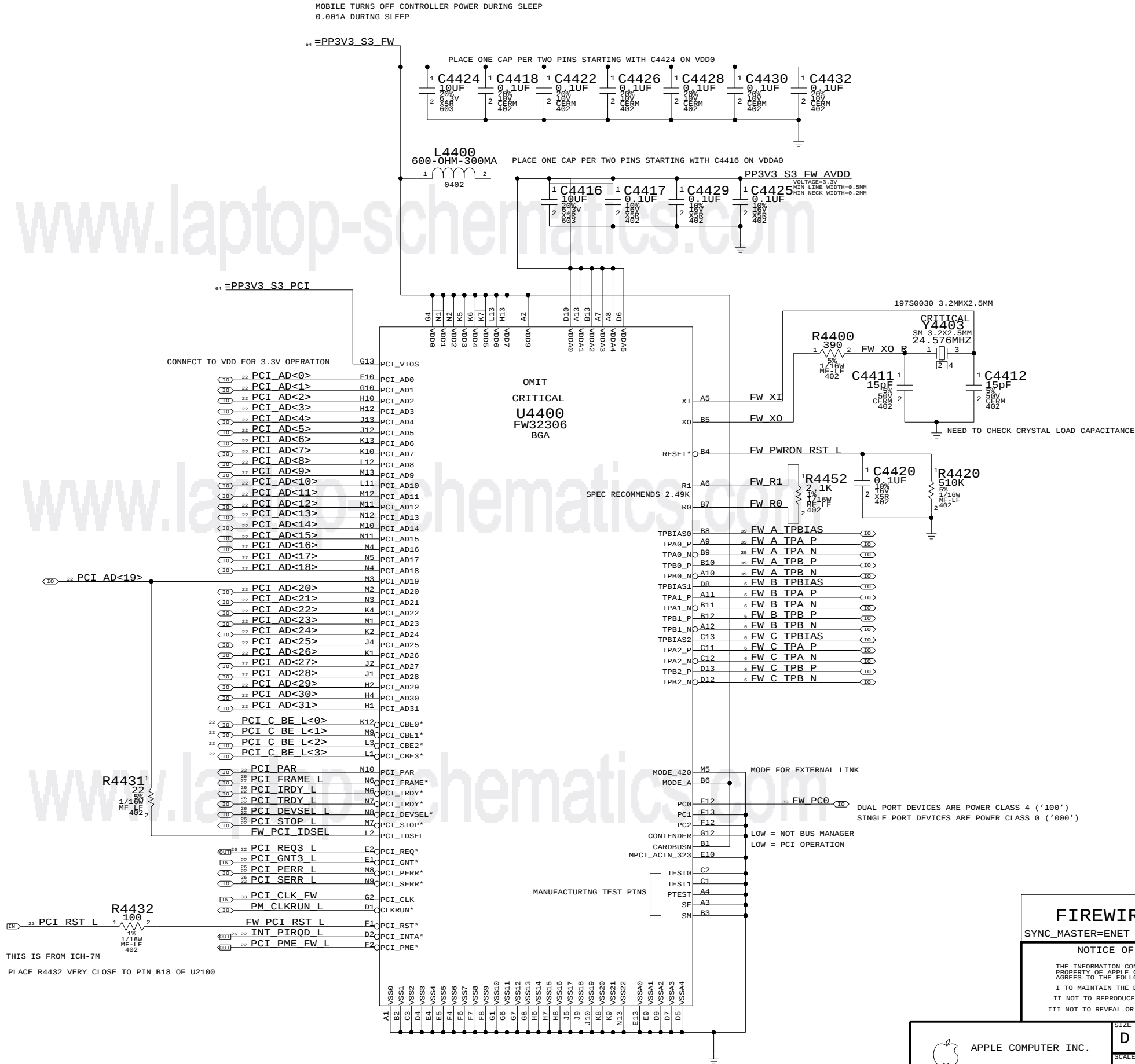
INPUT
=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT
PCI_AD<0..31>, PCI_C_BE_L<0..3>, PCI_FRAME_L, PCI_IRDY_L, PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT
PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/16/2005 - BGA VERSION OF FW32306 ADDED
6/21/2005 - CHANGED INT TO INT_PIRQD (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_STOP_L TO REQ3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - CHANGED FW_A_TPA_P/N TO REQ3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON REQ3 AND REMOVED CONNECTION TO PLY_RST_L
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRINGING OUT PCB CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND



FIREWIRE CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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D	051-7173	00000
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NONE	38	78

Page Notes

INPUT:
=PPBUS_FW - PORT POWER
=PP3V3_S5_FW - DIGITAL POWER
=GND_CHASSIS_FW_PORT0 - CHASSIS GROUND
=FWPWR_PWRON - ADDITIONAL POWER CONTROL

INPUT/OUTPUT:
FW_TPA0_P/N, FW_TPB0_P/N, FW_TPBIA0 - FIREWIRE DIFF PAIRS

OUTPUT:
FW_PC0 - POWER CLASS IDENTIFIER (SINGLE PORT - TIE LOW)

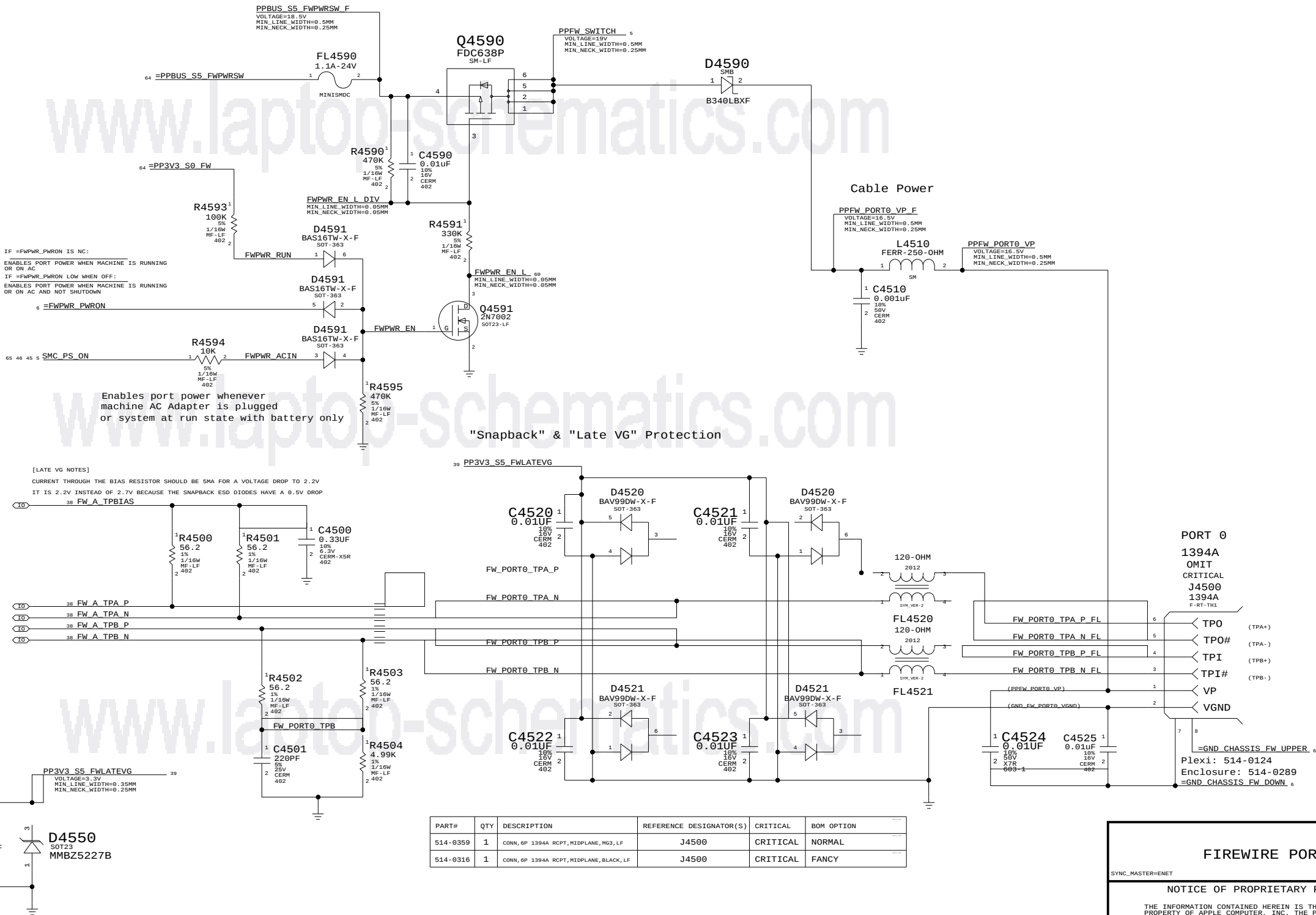
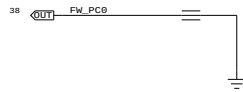
PAGE HISTORY

5/19/05 - INITIAL REVISION
6/22/05 - CHANGED DIFF PAIR NAMES TO MATCH REUSE
6/22/05 - REMOVED CONSTRAINTS BECAUSE USING ALLEGRO CONST MANAGER
6/22/05 - CONNECTED FW_PC0 FOR SINGLE PORT
7/26/05 - UPDATED LATE-VG POWER RAIL CIRCUIT FROM M1
7/26/05 - CHANGED CONNECTOR PORT NAMING TO PORT0
7/26/05 - SWITCHED TO 514-0124 FOR PRE-PROTO CONNECTOR
7/26/05 - REMOVED R4520 - IT HASN'T BEEN STUFFED FOR MANY PRODUCTS
7/26/05 - CHANGED FL4500 TO 1.1A VERSION
7/26/05 - REMOVED ETHERNET LOW-POWER MODE CIRCUIT
7/26/05 - UPDATED SIGNAL NAMES FOR FW PORT POWER ENABLE

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

PORT POWER CLASS

0 FOR SINGLE PORT
1 FOR DUAL PORT



FIREWIRE PORT

SYNC_MASTER=ENET

SYNC_DATE=11/16/2005

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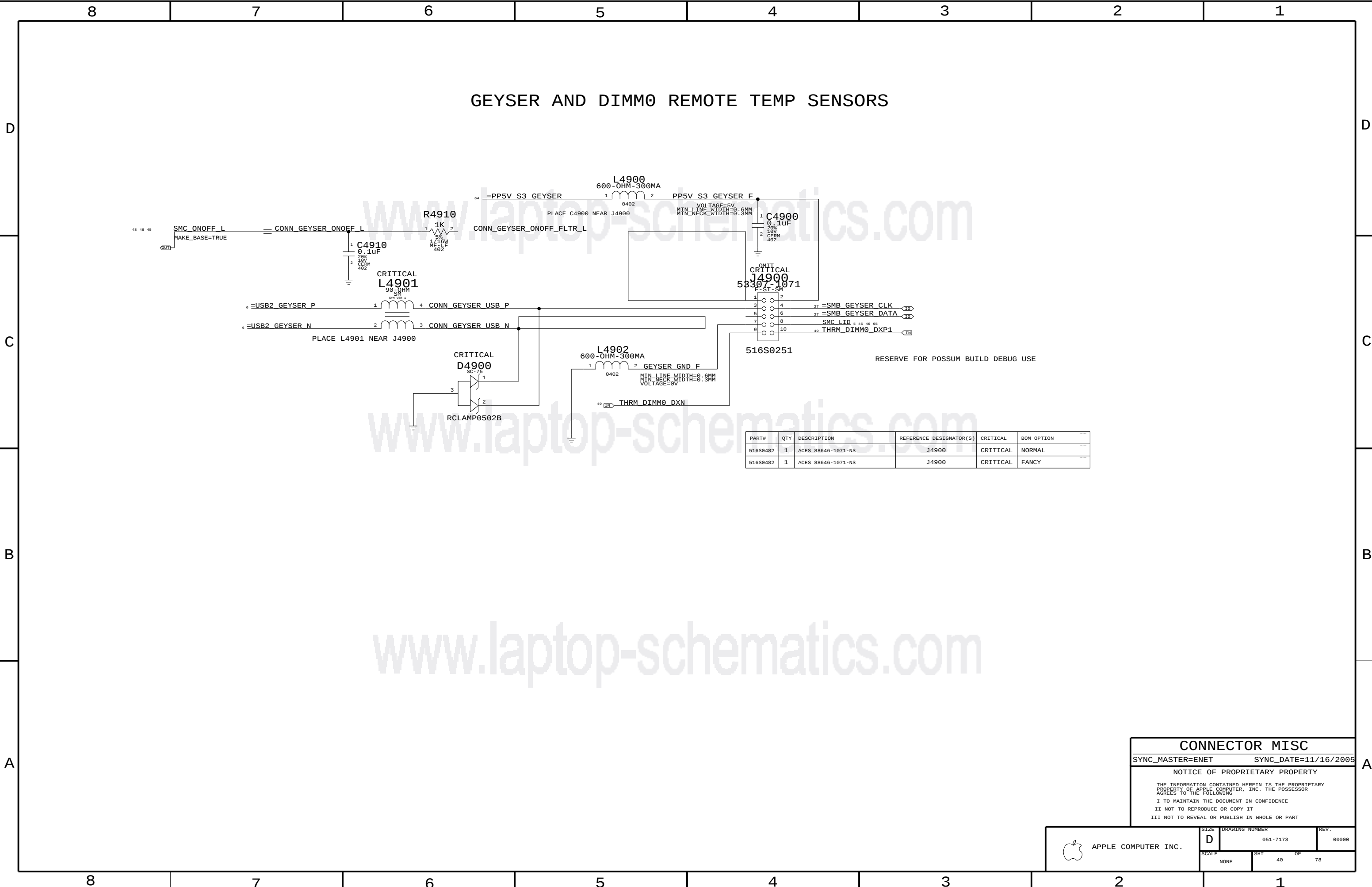
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SCALE: NONE

SHT: 39

OF: 78



CONNECTOR MISC

SYNC_MASTER=ENET SYNC_DATE=11/16/2005

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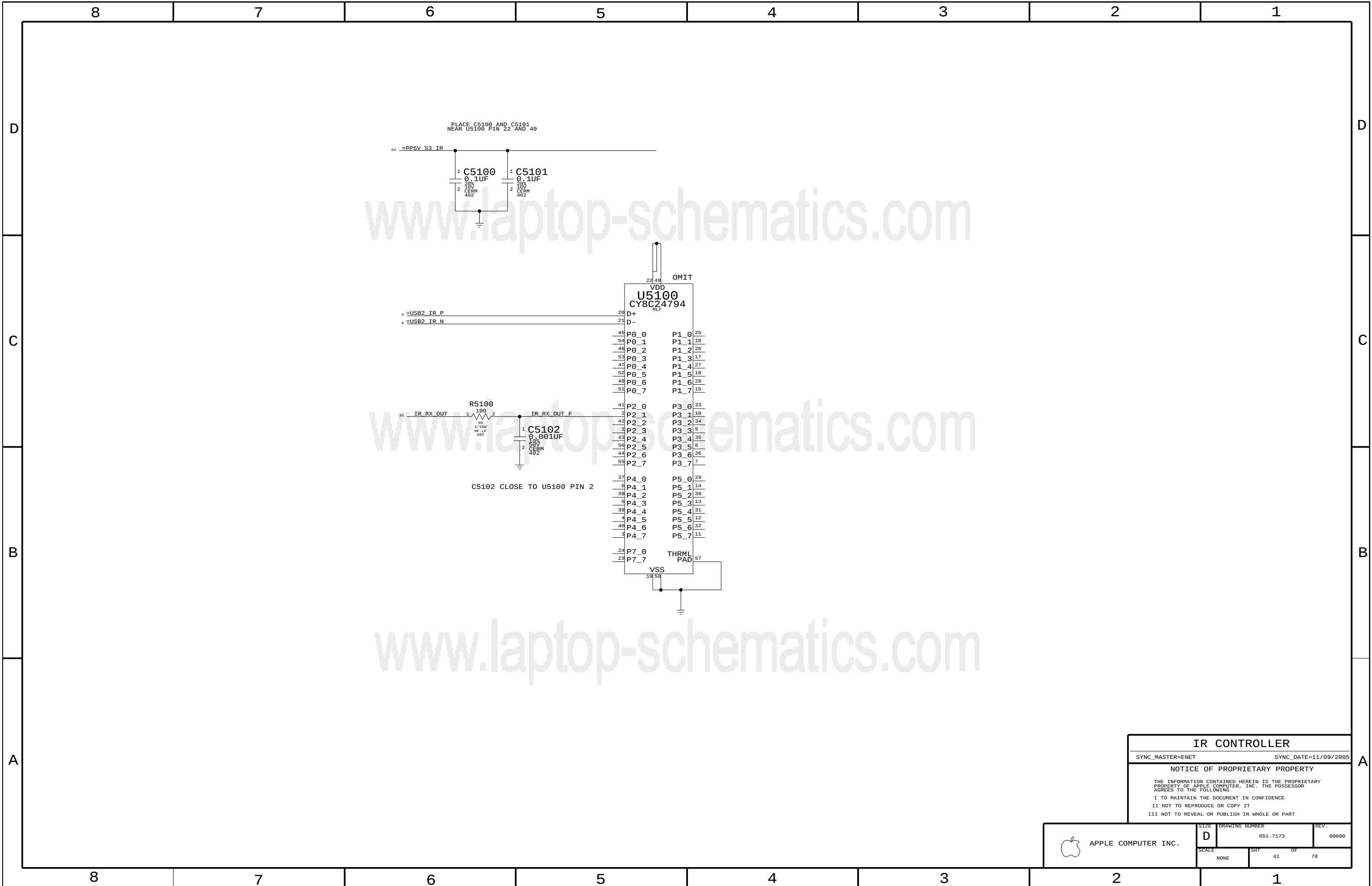
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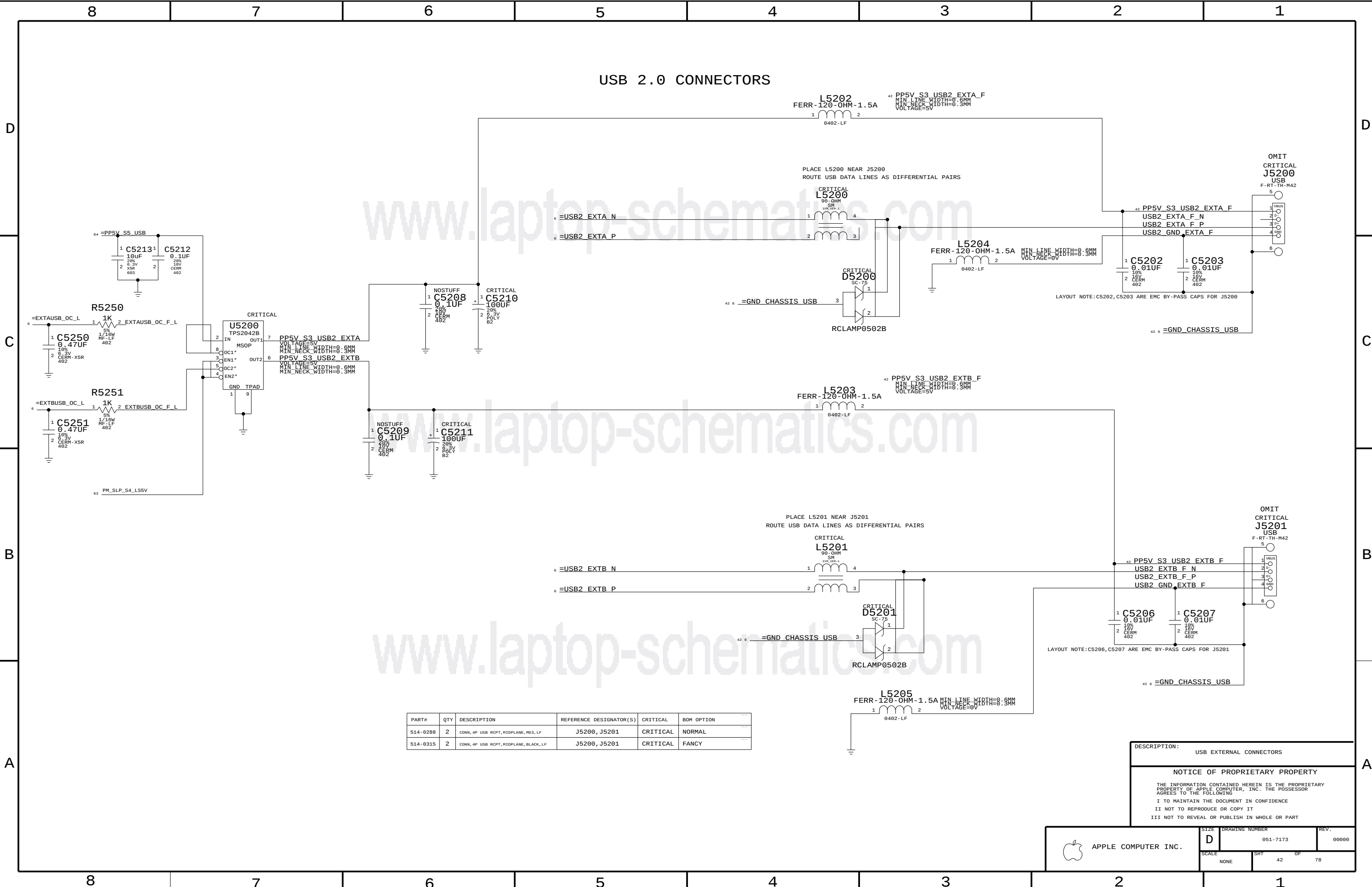
REV: 00000

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IR CONTROLLER		
SYNC_MASTER=ENET		SYNC_DATE=11/09/2005
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	D	051-7173	00000
SCALE	NONE	SHT	41 OF 78



USB 2.0 CONNECTORS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0288	2	CONN, 4P USB RCPT, MIDPLANE, MG3, LF	J5200, J5201	CRITICAL	NORMAL
514-0315	2	CONN, 4P USB RCPT, MIDPLANE, BLACK, LF	J5200, J5201	CRITICAL	FANCY

DESCRIPTION:
USB EXTERNAL CONNECTORS

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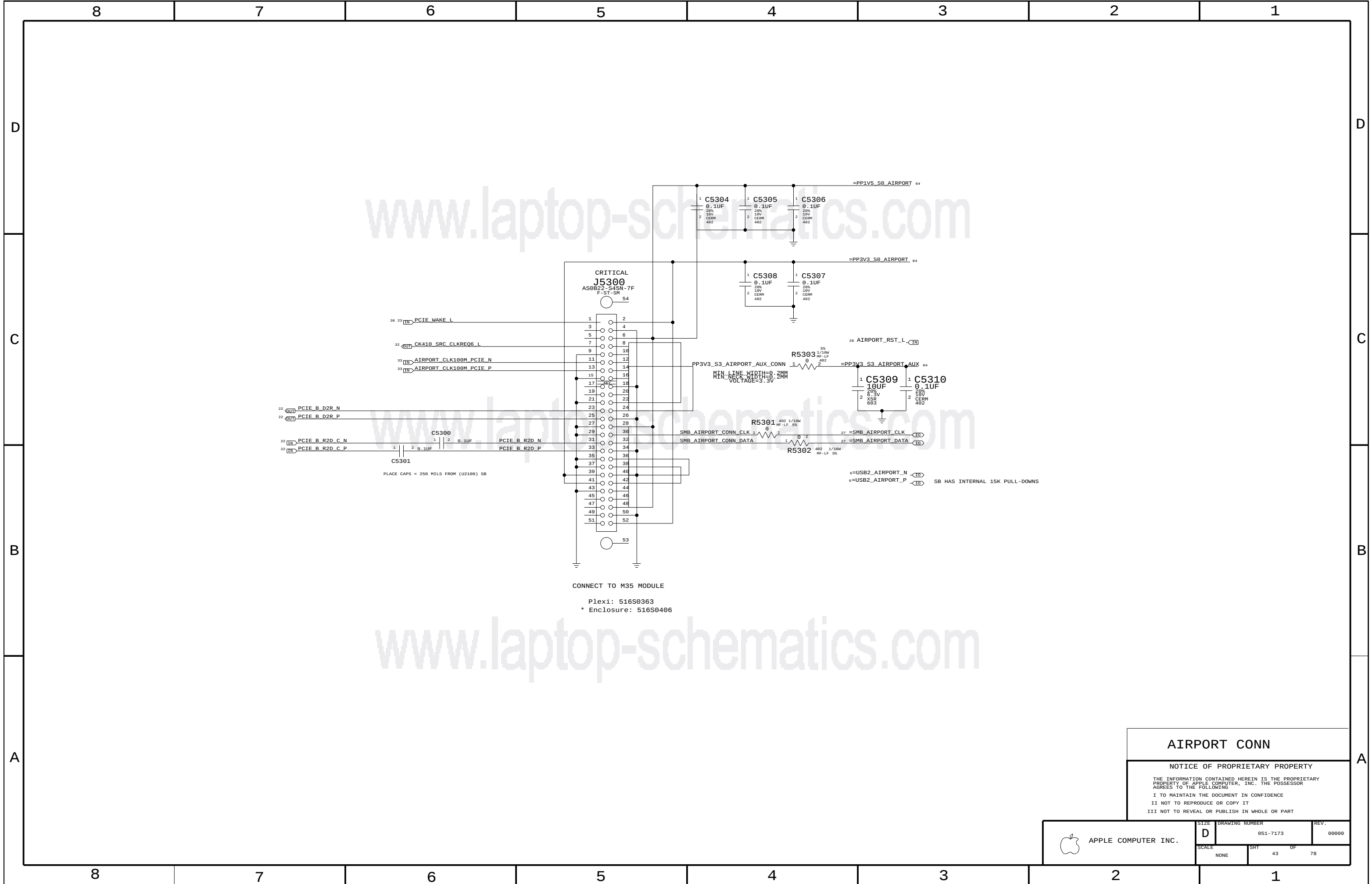
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	D	051-7173	00000
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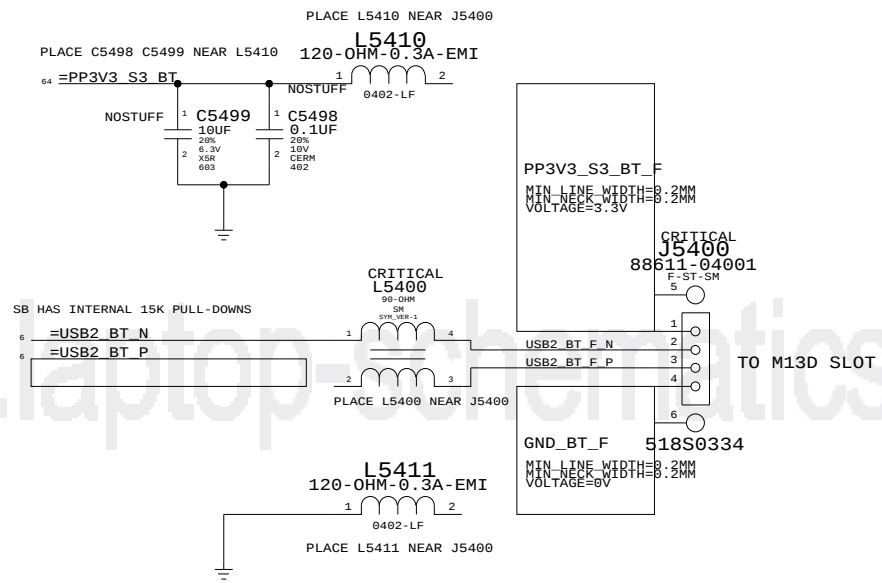
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D	051-7173	00000
SCALE	SHT	OF
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BLUETOOTH INTERFACE

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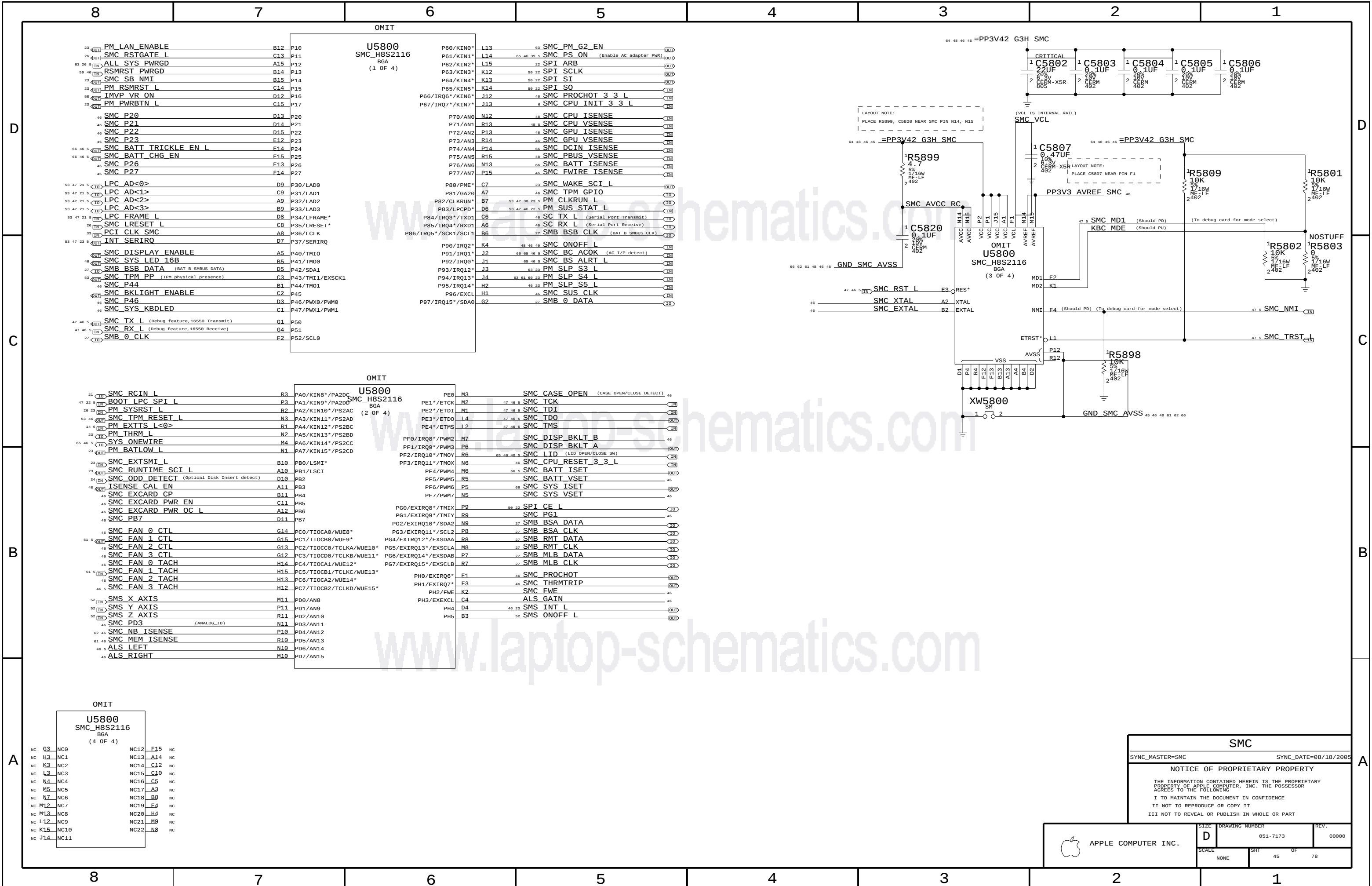
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SIZE D DRAWING NUMBER 051-7173 REV. 00000

SCALE NONE SHY 44 OF 78



SMC

SYNC_MASTER=SMC

SYNC_DATE=08/18/2005

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051-7173

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SCALE

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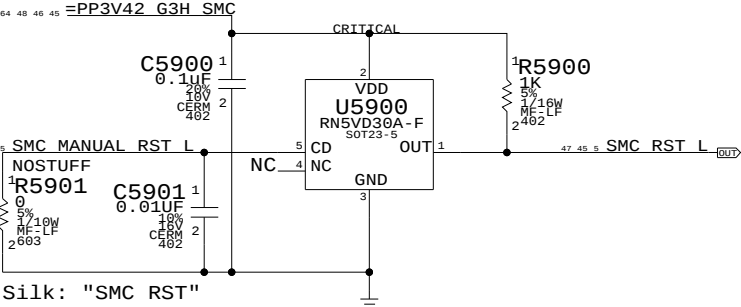
SHT

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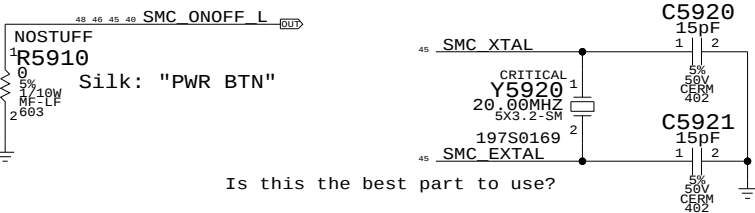
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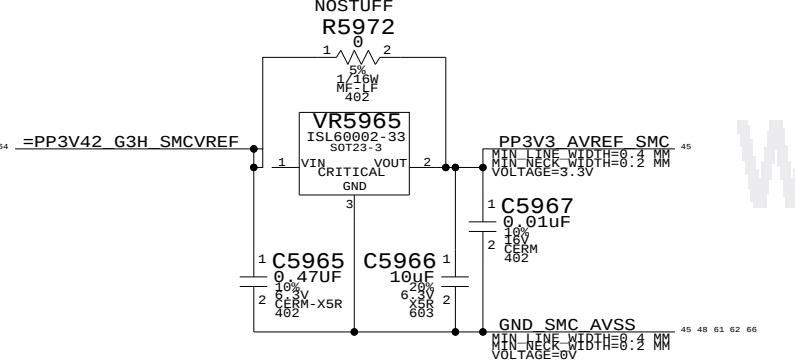
SMC Reset Button / Brownout Detect



Debug Power Button SMC Crystal Circuit

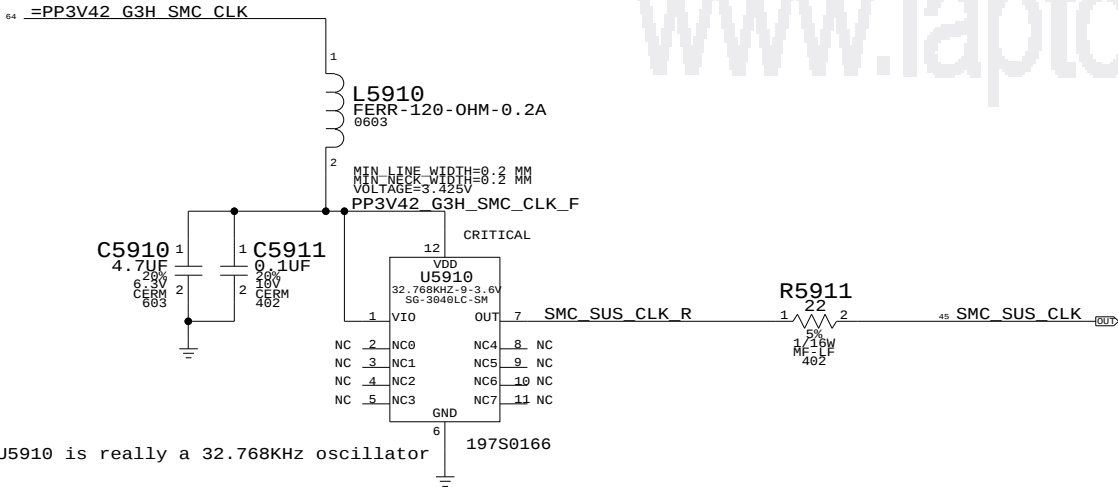


SMC AVREF Supply

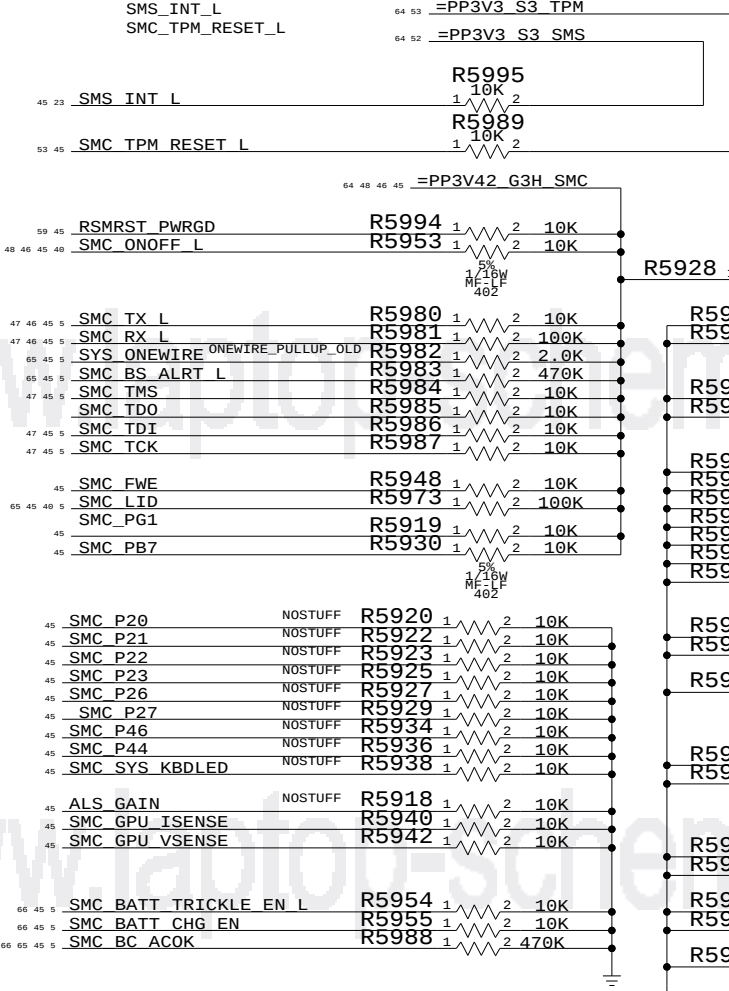


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1278	353S1381	?	VR5965	TI REF3133

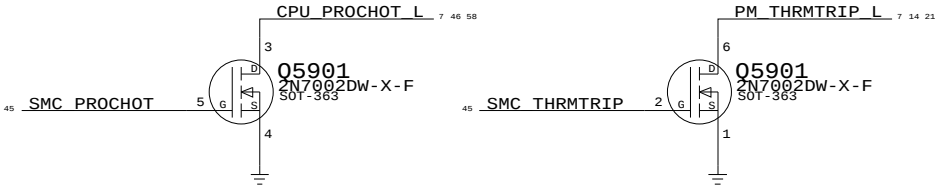
SMC G3HOT OSCILLATOR



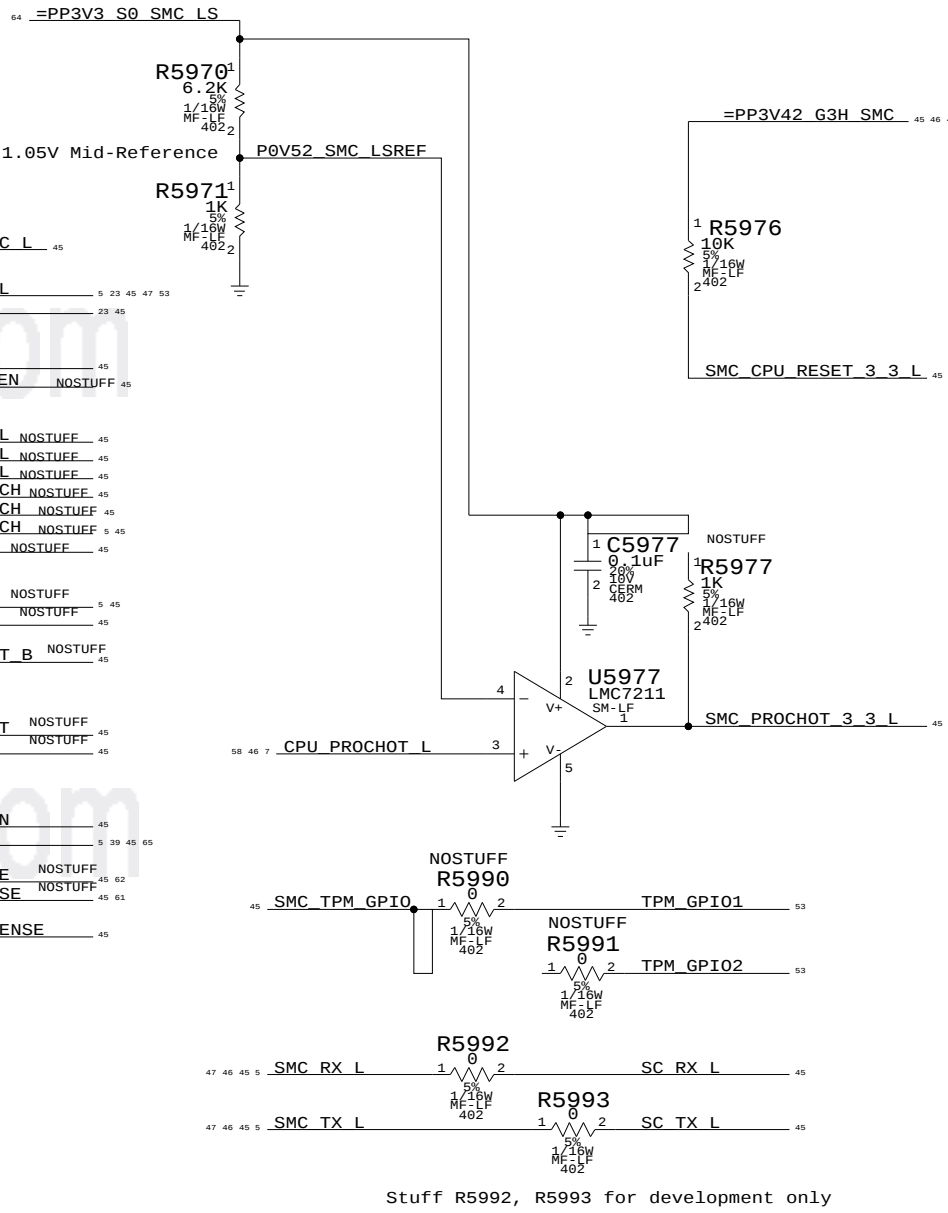
THESE NEED TO BE PULLED TO THE PROPER RAIL:



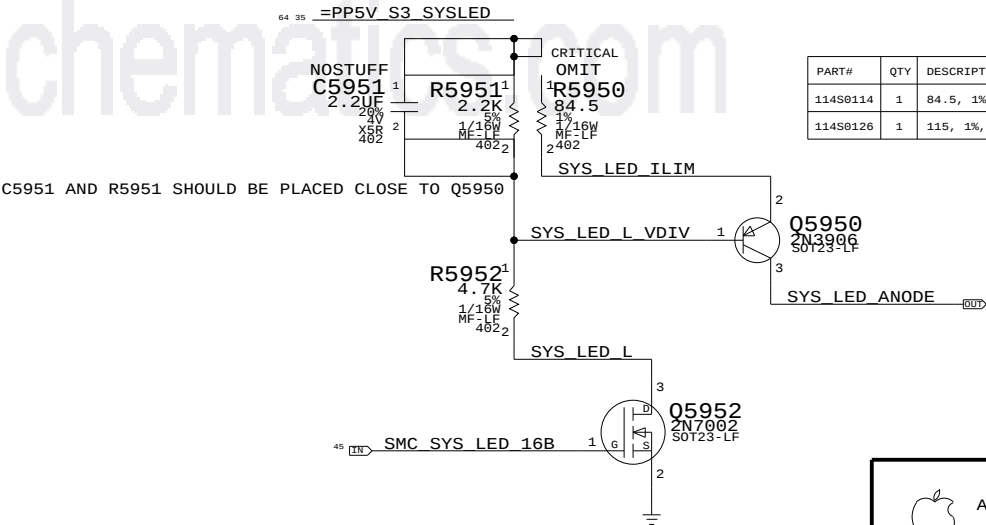
SMC 3.3V to 1.05V Level Shifting



SMC 1.05V to 3.3V Level Shifting



System (Sleep) LED Circuit



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0114	1	84.5, 1%, 1/16W, MF-LF, 402	R5950	NORMAL
114S0126	1	115, 1%, 1/16W, MF-LF, 402	R5950	FANCY

SMC SUPPORT

SYNC_MASTER=SMC SYNC_DATE=08/23/2005

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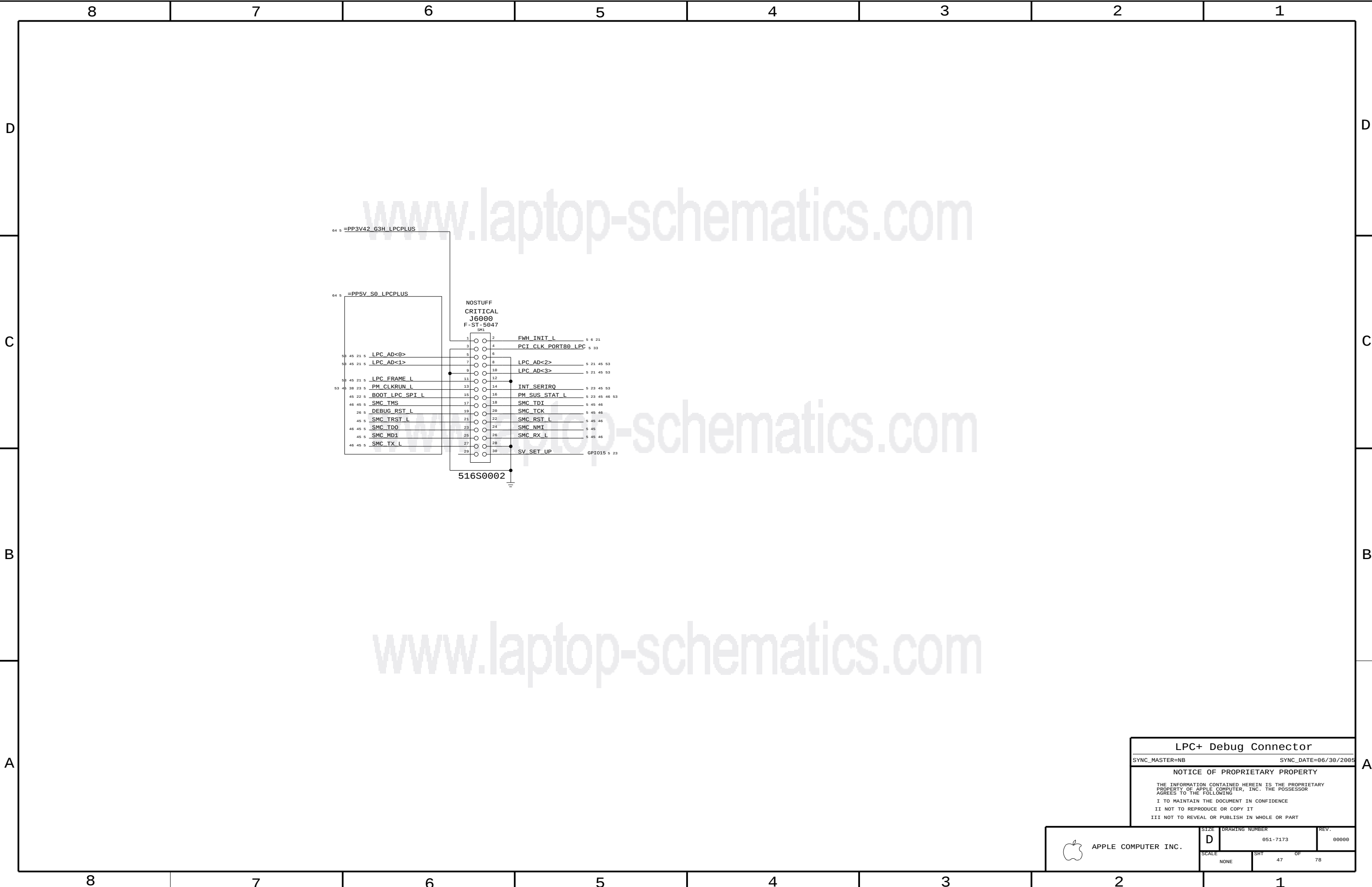
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APPLE COMPUTER INC.

D 051-7173 00000

SCALE SHY 46 OF 78



LPC+ Debug Connector

SYNC_MASTER=NB

SYNC_DATE=06/30/2005

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APPLE COMPUTER INC.

SCALE
NONE

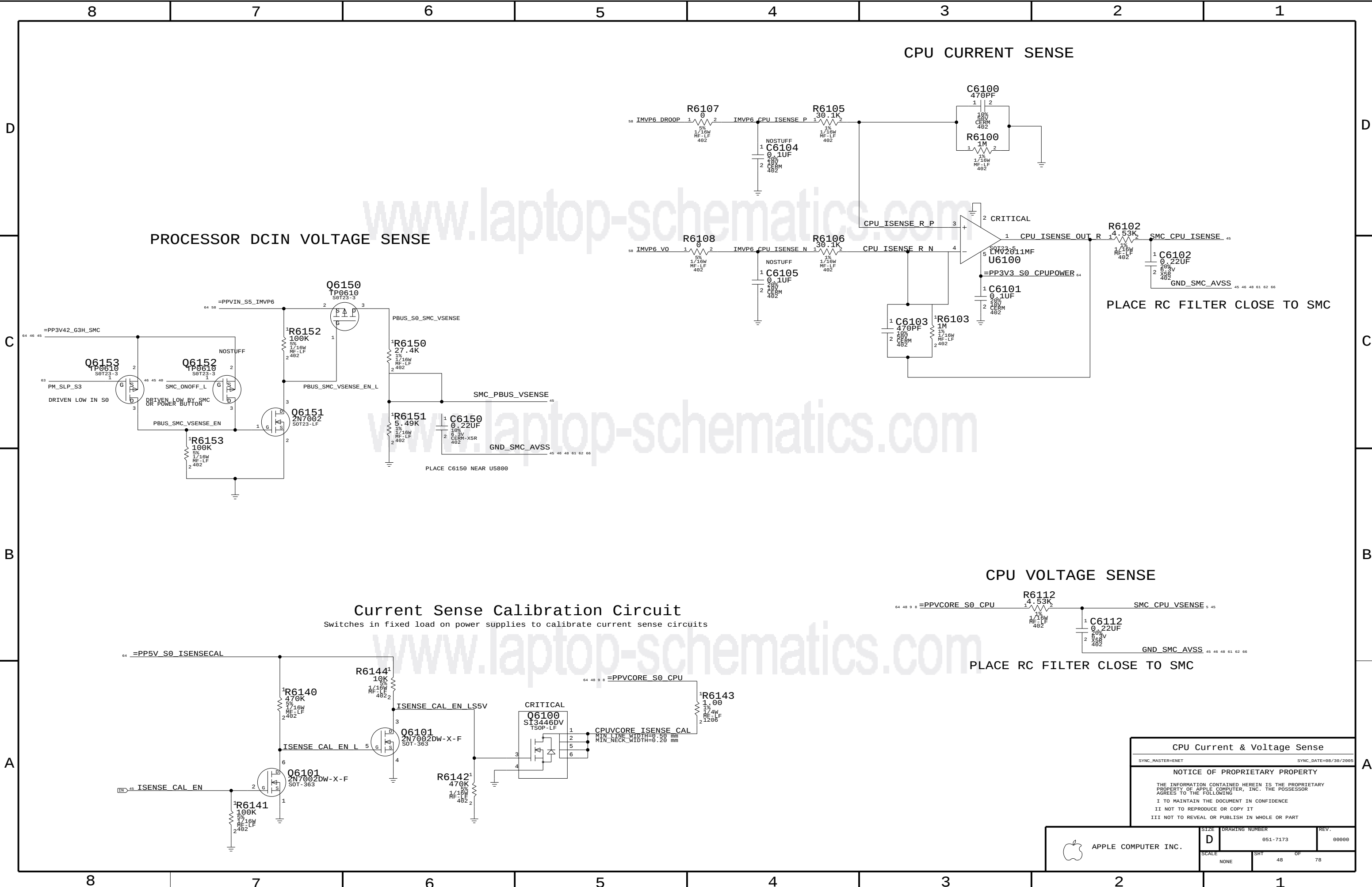
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051-7173

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OF
78



PROCESSOR DCIN VOLTAGE SENSE

CPU CURRENT SENSE

CPU VOLTAGE SENSE

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

CPU Current & Voltage Sense

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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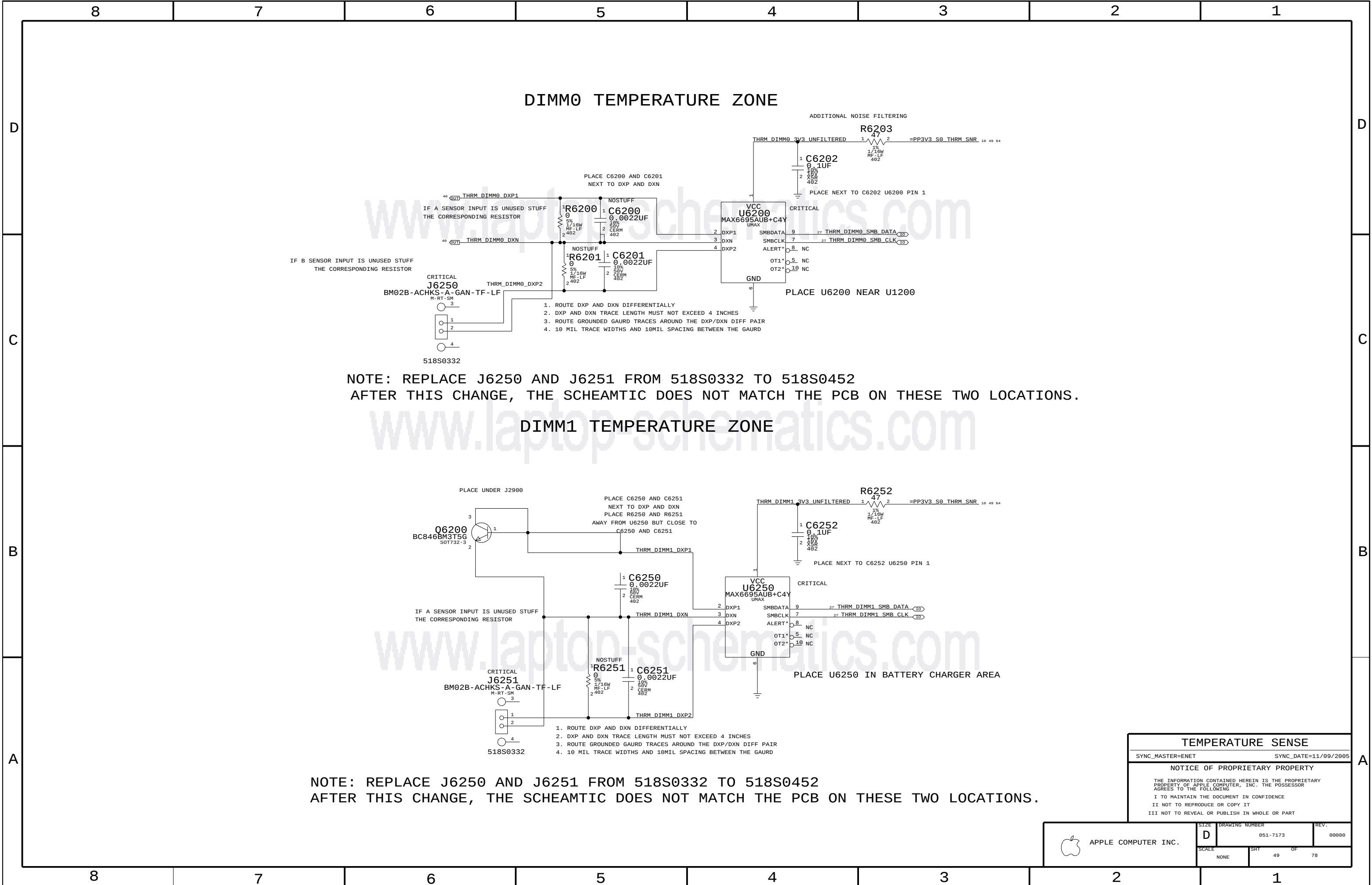


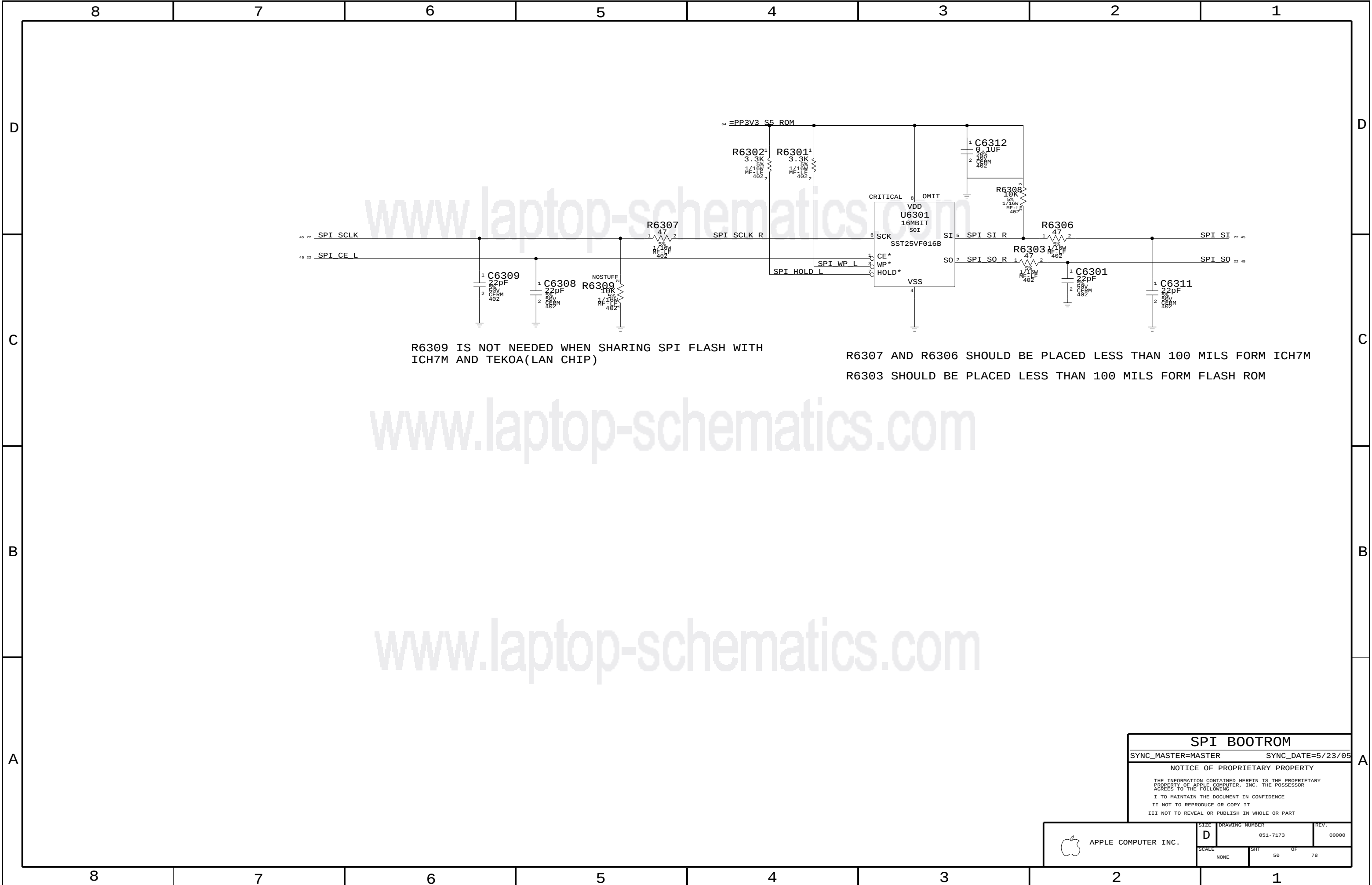
APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

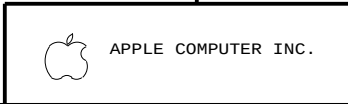
D 051-7173 00000

SCALE NONE SHY 48 OF 78





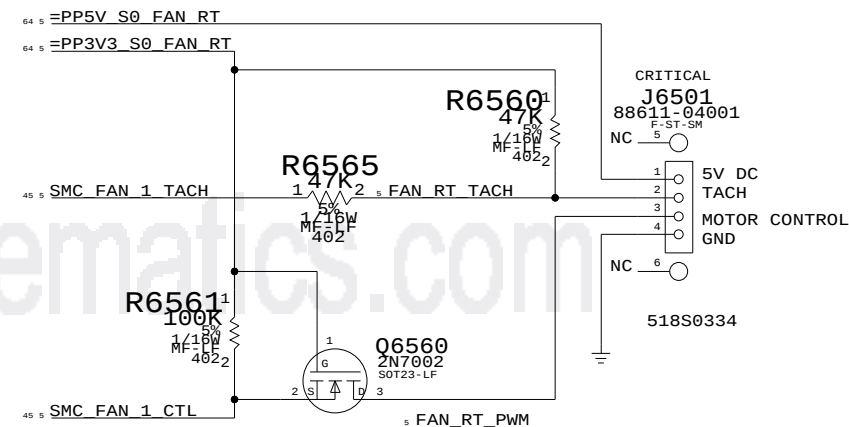
SPI BOOTROM		
SYNC_MASTER=MASTER		SYNC_DATE=5/23/05
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SCALE	SHT	OF
NONE	50	78



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Fan

SYNC_MASTER=ENET SYNC_DATE=11/10/2005

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SIZE	DRAWING NUMBER	REV.
D	051-7173	00000
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NONE	51	78

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PAGE NOTES

INPUT
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT
SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY
5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/28/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L

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Desired Orientation
(Placed on board bottom side)

Package Top

SMS_X_AXIS₄₅
SMS_Y_AXIS₄₅
SMS_Z_AXIS₄₅

Part# QTY DESCRIPTION REFERENCE DESIGNATOR(S) CRITICAL BOM OPTION
132S0131 3 0.033UF, 10%, 16V, 402 C6604, C6605, C6606 ACCEL_KIONIX
132S0042 3 0.01UF, 10%, 16V, 402 C6604, C6605, C6606 ACCEL_ST

SMC_ACC_SELFTEST-->is a test signal
0 -->Normal operation
1 -->Self test

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Desired Orientation
(Placed on board bottom side)

Package Top

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SMS
SYNC_MASTER=SMC SYNC_DATE=08/23/2005

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Desired Orientation
(Placed on board bottom side)

Package Top

+Y
+X
+Z (up)

SMS_X_AXIS₄₅
SMS_Y_AXIS₄₅
SMS_Z_AXIS₄₅

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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Desired Orientation
(Placed on board bottom side)

Package Top

+Z (up)
+X
+Y

SMS
SYNC_MASTER=SMC SYNC_DATE=08/23/2005

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DRAWING NUMBER: 051-7173 REV.: 00000

SCALE: NONE SHY: 0P OF: 78

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7/26/2005	CONNECTED PD PIN TO SMC'S SMS_ONOFF_L

The schematic shows two accelerometers: U6620 (KXM52-2050) and U6650 (LIS3L02AL). Both are connected to PP3V3_S3_SMS for VDD and have their GND pins connected to ground. The LIS3L02AL has its ST pin connected to PP3V3_S3_ST_ACCEL through a pull-up resistor R6621. The KXM52-2050 has its SELF TEST pin connected to ST ACCEL ON L through a pull-up resistor R6650. Its PARITY pin is connected to NC, and its THERML PAD pin is connected to ground. Output pins VOUTX, VOUTY, and VOUTZ are connected to the +X, +Y, and +Z axes respectively. Three decoupling capacitors C6604, C6605, and C6606 are shown with OMIT labels.

Desired Orientation (Placed on board bottom side)

Package Top
+Y
+X
+Z (up)

SMS_X_AXIS
SMS_Y_AXIS
SMS_Z_AXIS

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SMS
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D 051-7173 REV. 00000

SCALE NONE SHY OP 78

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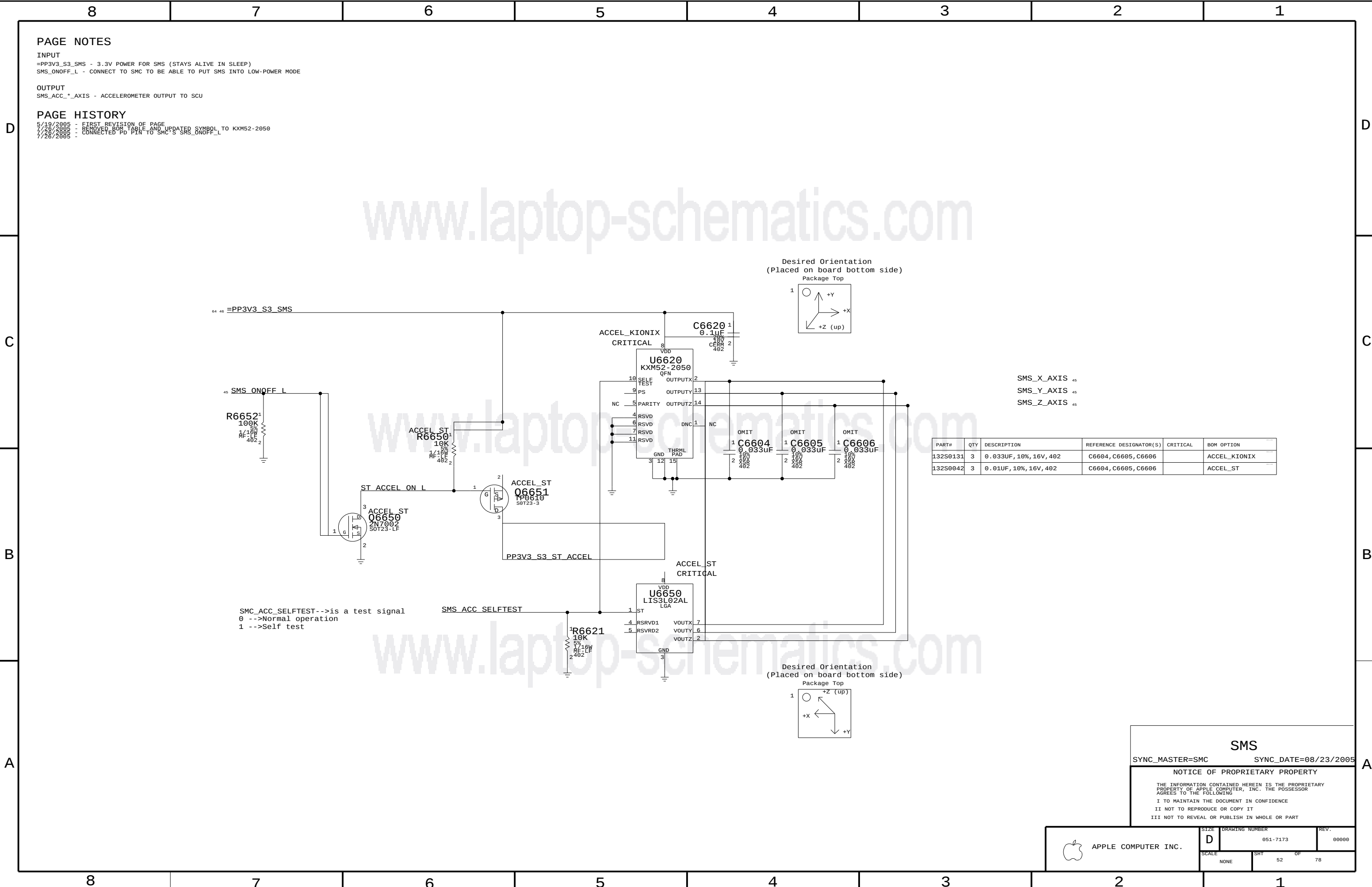
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SCALE: NONE SHY: 52 OF: 78

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The schematic shows two accelerometers: U6620 (KXM52-2050) and U6650 (LIS3L02AL). Both are connected to a common VDD supply derived from PP3V3_S3_SMS through resistors R6650 and R6652. They share a common ground connection via R6621. The outputs of both sensors are routed to the SCU as SMS_X_AXIS, SMS_Y_AXIS, and SMS_Z_AXIS.

Desired Orientation (Placed on board bottom side)

Package Top

- +Y
- +X
- +Z (up)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	0.033UF, 10%, 16V, 402	C6604, C6605, C6606		ACCEL_KIONIX
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SMS

SYNC_MASTER=SMC SYNC_DATE=08/23/2005

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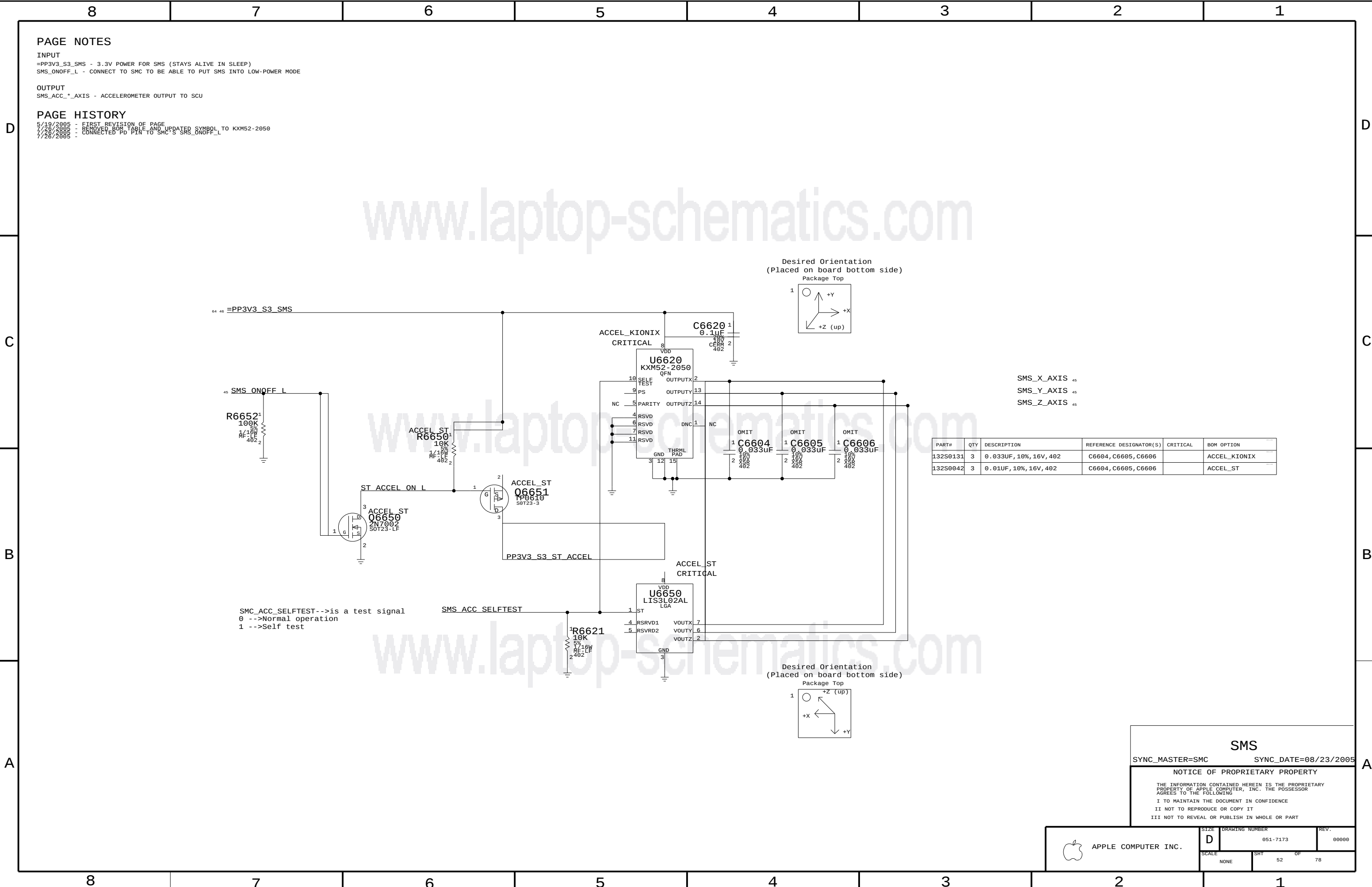
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SCALE: NONE SHEETS: 52 OF 78

[illegible][illegible]

87654321

D

B

A

C

PAGE NOTES

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Desired Orientation
(Placed on board bottom side)
Package Top

1

+Y

+X

+Z (up)

64 46 =PP3V3_S3_SMS

45 SMS_ONOFF_L

R6652¹

100K

1/16W

MF=LF

402

2

ACCEL_ST

R6650¹

10K

1/16W

MF=LF

402

2

ST ACCEL ON L

1

2

3

ACCEL_ST

Q6650

2N7002

SOT23-LF

1

6

2

ACCEL_ST

Q6651

TP0610

SOT23-3

1

2

3

PP3V3_S3_ST_ACCEL

SMC_ACC_SELFTEST-->is a test signal

0 -->Normal operation

1 -->Self test

SMS_ACC_SELFTEST

1R6621

10K

1/16W

MF=LF

402

2

ACCEL_KIONIX

CRITICAL

U6620

KXM52-2050

QFN

8 VDD

10 SELF TEST

9 PS

NC

5 PARITY

4 RSVD

6 RSVD

7 RSVD

11 RSVD

12 GND

15 THERML PAD

2 OUTPUTX

13 OUTPUTY

14 OUTPUTZ

1 NC

1 C6604

0.033uF

10% 16V 402

2

1 OMIT

1 C6605

0.033uF

10% 16V 402

2

1 OMIT

1 C6606

0.033uF

10% 16V 402

2

ACCEL_ST

CRITICAL

U6650

LIS3L02AL

LGA

8 VDD

1 ST

4 RSRVD1

5 RSRVD2

7 VOUTX

6 VOUTY

2 VOUTZ

3 GND

Desired Orientation
(Placed on board bottom side)
Package Top

1

+Z (up)

+X

+Y

SMS_X_AXIS 45

SMS_Y_AXIS 45

SMS_Z_AXIS 45

TABLE

PART#

QTY

DESCRIPTION

REFERENCE DESIGNATOR(S)

CRITICAL

BOM OPTION

132S0131

3

0.033uF, 10%, 16V, 402

C6604, C6605, C6606

ACCEL_KIONIX

132S0042

3

0.01uF, 10%, 16V, 402

C6604, C6605, C6606

ACCEL_ST

SMS

SYNC_MASTER=SMC

SYNC_DATE=08/23/2005

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D

SCALE

NONE

DRAWING NUMBER

051-7173

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52

78

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PAGE NOTES

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Desired Orientation
(Placed on board bottom side)

Package Top

1 +Y
+X
+Z (up)

SMS_X_AXIS 45
SMS_Y_AXIS 45
SMS_Z_AXIS 45

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Desired Orientation
(Placed on board bottom side)

Package Top

1 +Z (up)
+X
+Y

SMS
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SMS_X_AXIS
SMS_Y_AXIS
SMS_Z_AXIS

Desired Orientation
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Package Top

+Y
+X
+Z (up)

Part List:

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DESIGN INFORMATION:

- U6620: KXM52-2050 QFN
- U6650: LIS3L02AL LGA
- R6652: 100K 1% 1W MF-LF 402
- R6650: 10K 1% 1W MF-LF 402
- R6621: 10K 1% 1W MF-LF 402
- Q6651: TP0610 SOT23-3
- Q6650: 2N7002 SOT23-LF
- C6620: 0.1UF 16V CER-M 402
- C6604, C6605, C6606: 0.033UF or 0.01UF 10% 16V 402

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SYNC_MASTER=SMC SYNC_DATE=08/23/2005

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APPLE COMPUTER INC.

DRAWING NUMBER: 051-7173 REV.: 00000

SCALE: NONE SHY: OP 78

The figure displays a detailed schematic diagram for the SMS (Smart Motion Sensor) circuitry. It includes two accelerometers, U6620 (KXM52-2050 QFN) and U6650 (LIS3L02AL LGA), each with associated power regulation components like resistors R6652, R6650, R6621 and capacitors C6604, C6605, C6606. The diagram also shows control signals such as ST_ACCEL_ON_L, PP3V3_S3_ST_ACCEL, and SMS_ACC_SELFTEST. A parts table lists three capacitors (C6604, C6605, C6606) used for decoupling. Orientation diagrams indicate the desired placement of the chips on the board bottom side. Metadata at the bottom right identifies the drawing as D, created by Apple Computer Inc., dated 08/23/2005, with revision 00000.

PAGE NOTES

INPUT
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT
SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY
5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L

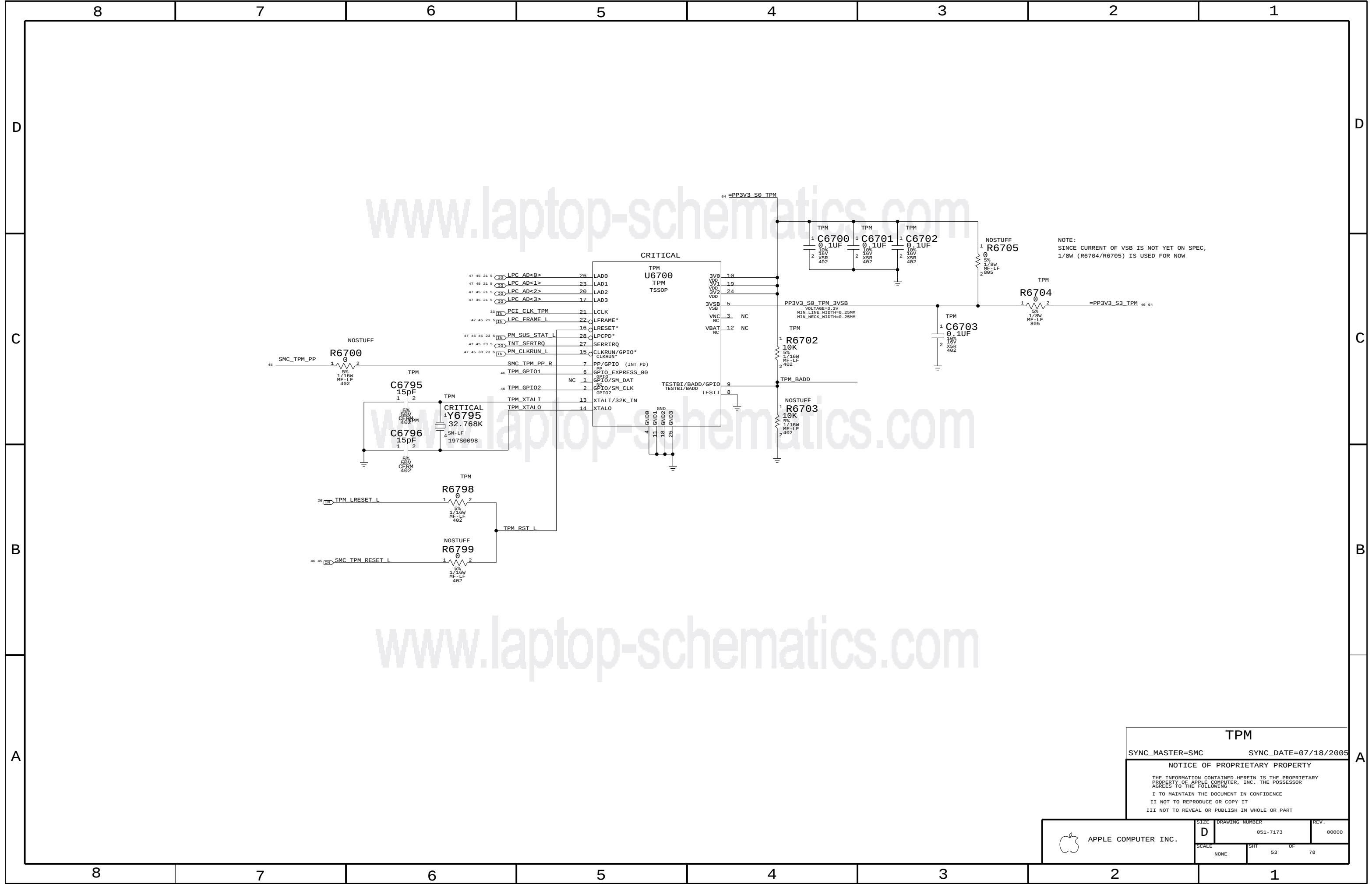
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	0.033UF, 10%, 16V, 402	C6604, C6605, C6606		ACCEL_KIONIX
132S0042	3	0.01UF, 10%, 16V, 402	C6604, C6605, C6606		ACCEL_ST

SMS
SYNC_MASTER=SMC SYNC_DATE=08/23/2005

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DRAWING NUMBER: D
SCALE: NONE
REV.: 06000



TPM

SYNC_MASTER=SMC SYNC_DATE=07/18/2005

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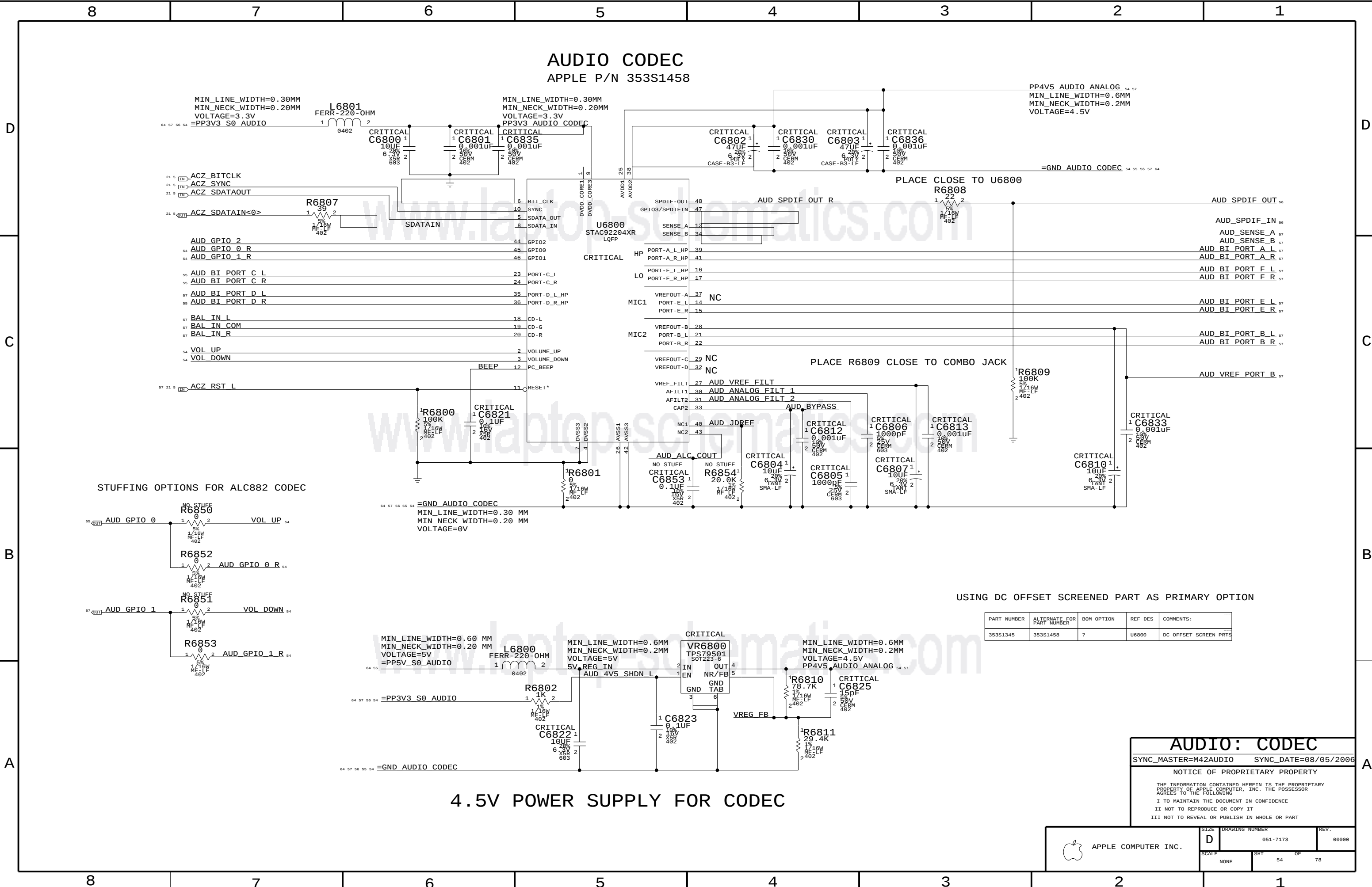
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	D	051-7173	00000
SCALE		SHT OF	
NONE		53 OF 78	



AUDIO CODEC
APPLE P/N 353S1458

PP4V5_AUDIO_ANALOG 54 57
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=4.5V

MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
PP3V3_S0_AUDIO

MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
PP3V3_AUDIO_CODEC

=GND_AUDIO_CODEC 54 55 56 57 64

PLACE CLOSE TO U6800

PLACE R6809 CLOSE TO COMBO JACK

STUFFING OPTIONS FOR ALC882 CODEC

USING DC OFFSET SCREENED PART AS PRIMARY OPTION

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1345	353S1458	?	U6800	DC OFFSET SCREEN PRTS

4.5V POWER SUPPLY FOR CODEC

AUDIO: CODEC

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

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SIZE DRAWING NUMBER

D

051-7173

REV.

00000

SCALE

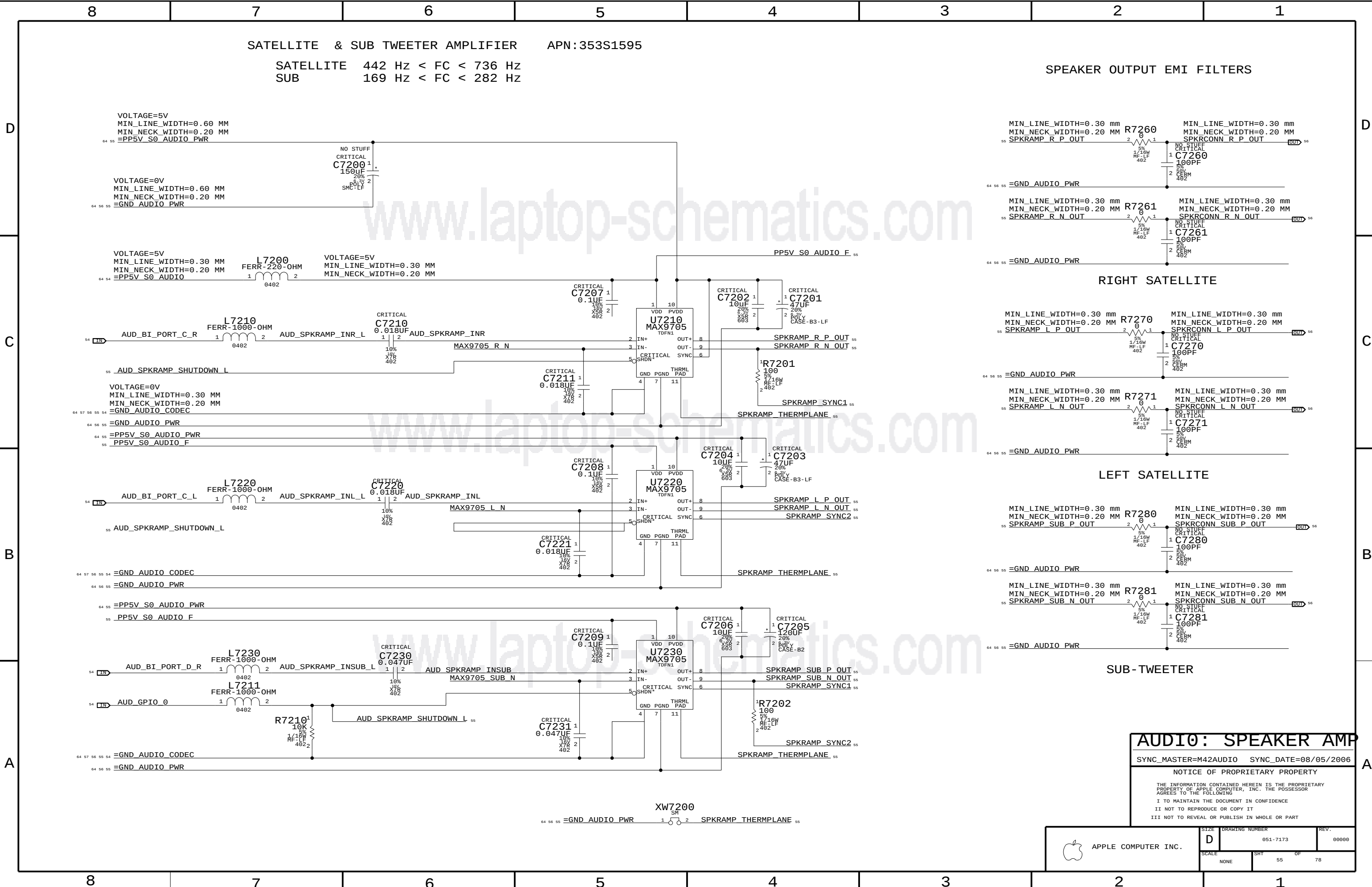
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SHT

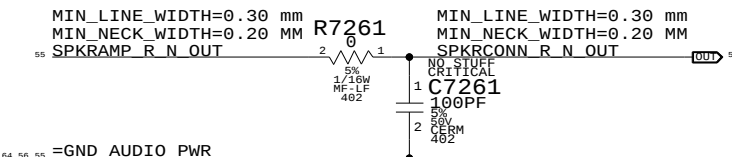
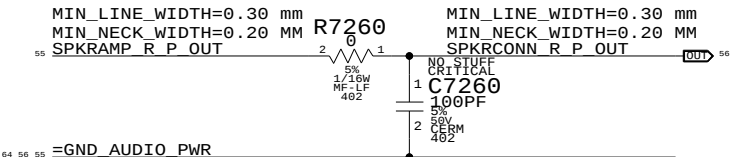
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OF

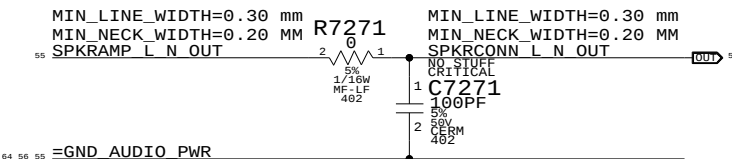
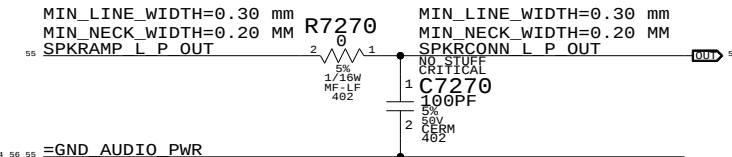
78



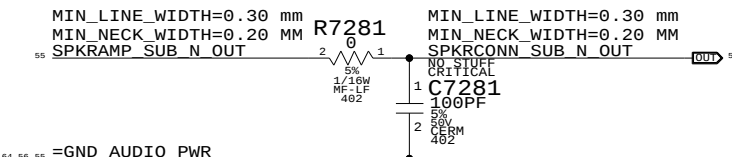
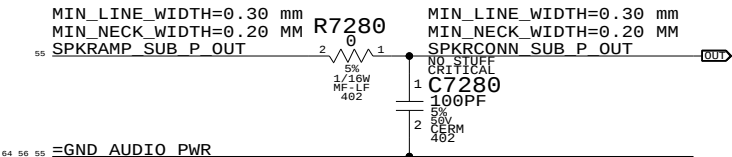
SPEAKER OUTPUT EMI FILTERS



RIGHT SATELLITE



LEFT SATELLITE



SUB-TWEETER

AUDIO0: SPEAKER AMP

SYNC_MASTER=M42AUDIO0 SYNC_DATE=08/05/2006

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	D	051-7173	00000
SCALE	NONE	SHT	55 OF 78

AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

MIC CONNECTOR

APN:514S0392

SPEAKER CONNECTOR

APN:518S0332

AUDIO SHIELD FILL

MIC EMI FILTER

AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0290	1	CONN, 3.5MM COMBO AUDIO OUT, RA, MG3, LF	J7300	CRITICAL	NORMAL
514-0291	1	CONN, 3.5MM COMBO AUDIO IN, RA, MG3, LF	J7350	CRITICAL	NORMAL
514-0317	1	CONN, 3.5MM COMBO AUDIO OUT, RA, BLACK, LF	J7300	CRITICAL	FANCY
514-0318	1	CONN, 3.5MM COMBO AUDIO IN, RA, BLACK, LF	J7350	CRITICAL	FANCY

AUDIO: JACK

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

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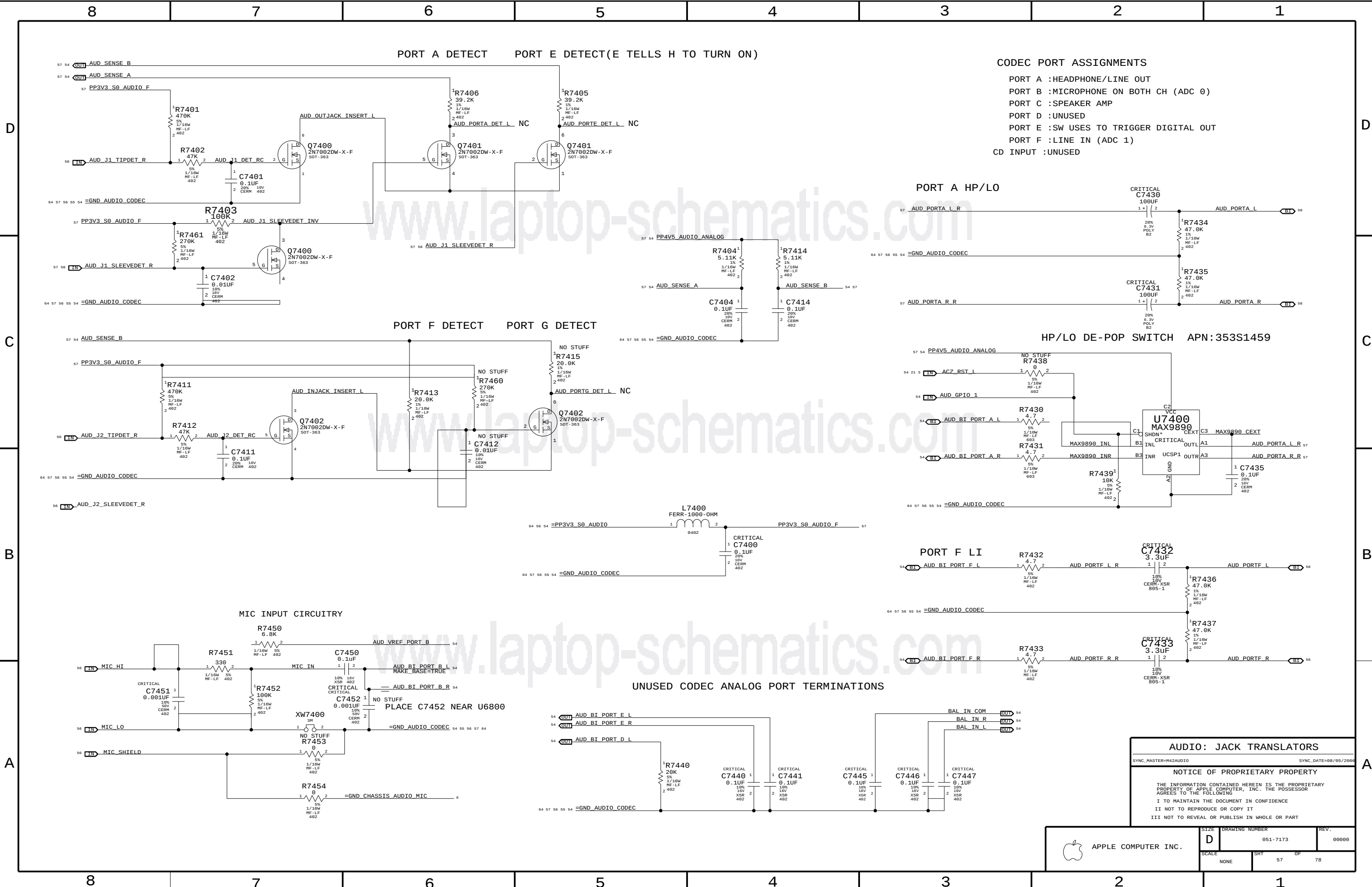


APPLE COMPUTER INC.

SIZE: DRAWING NUMBER: REV.

D 051-7173 00000

SCALE: NONE SHY 56 OF 78



CODEC PORT ASSIGNMENTS

PORT A :HEADPHONE/LINE OUT

PORT B :MICROPHONE ON BOTH CH (ADC 0)

PORT C :SPEAKER AMP

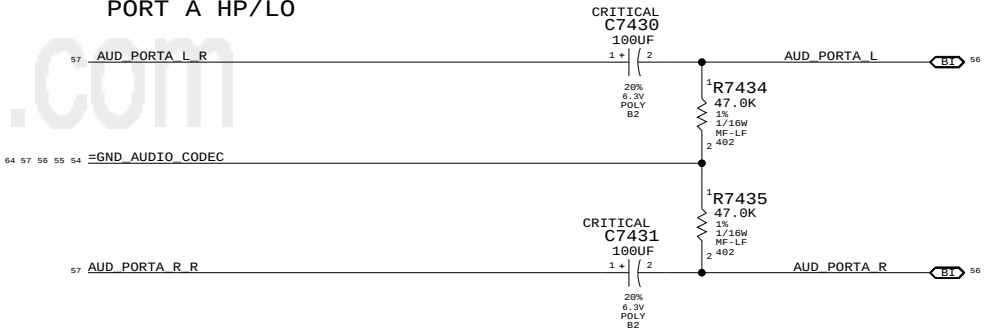
PORT D :UNUSED

PORT E :SW USES TO TRIGGER DIGITAL OUT

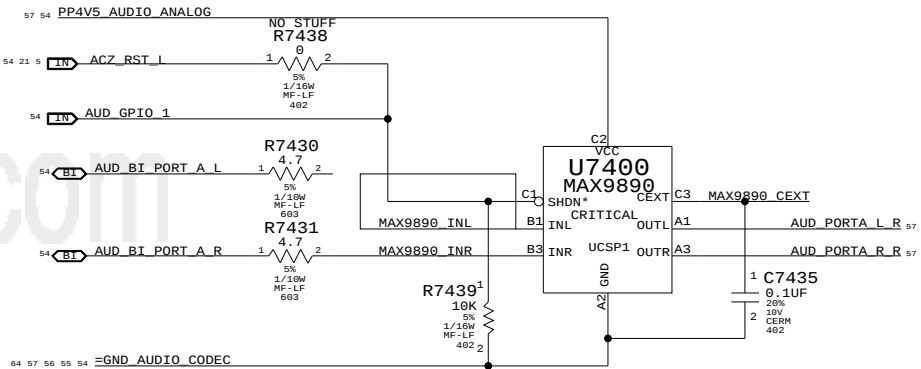
PORT F :LINE IN (ADC 1)

CD INPUT :UNUSED

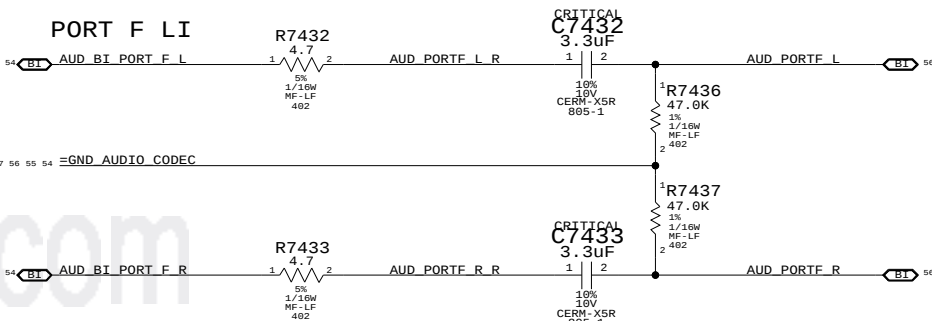
PORT A HP/LO



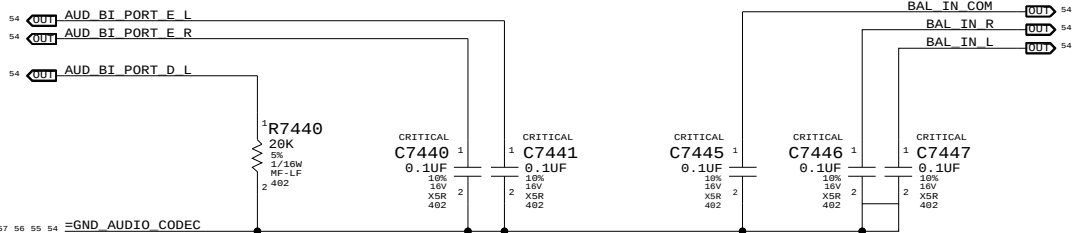
HP/LO DE-POP SWITCH APN:353S1459



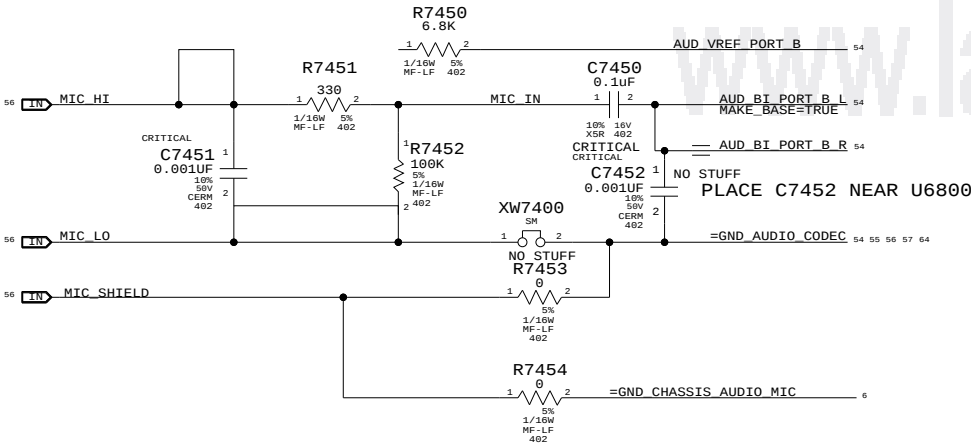
PORT F LI



UNUSED CODEC ANALOG PORT TERMINATIONS



MIC INPUT CIRCUITRY



AUDIO: JACK TRANSLATORS

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2008

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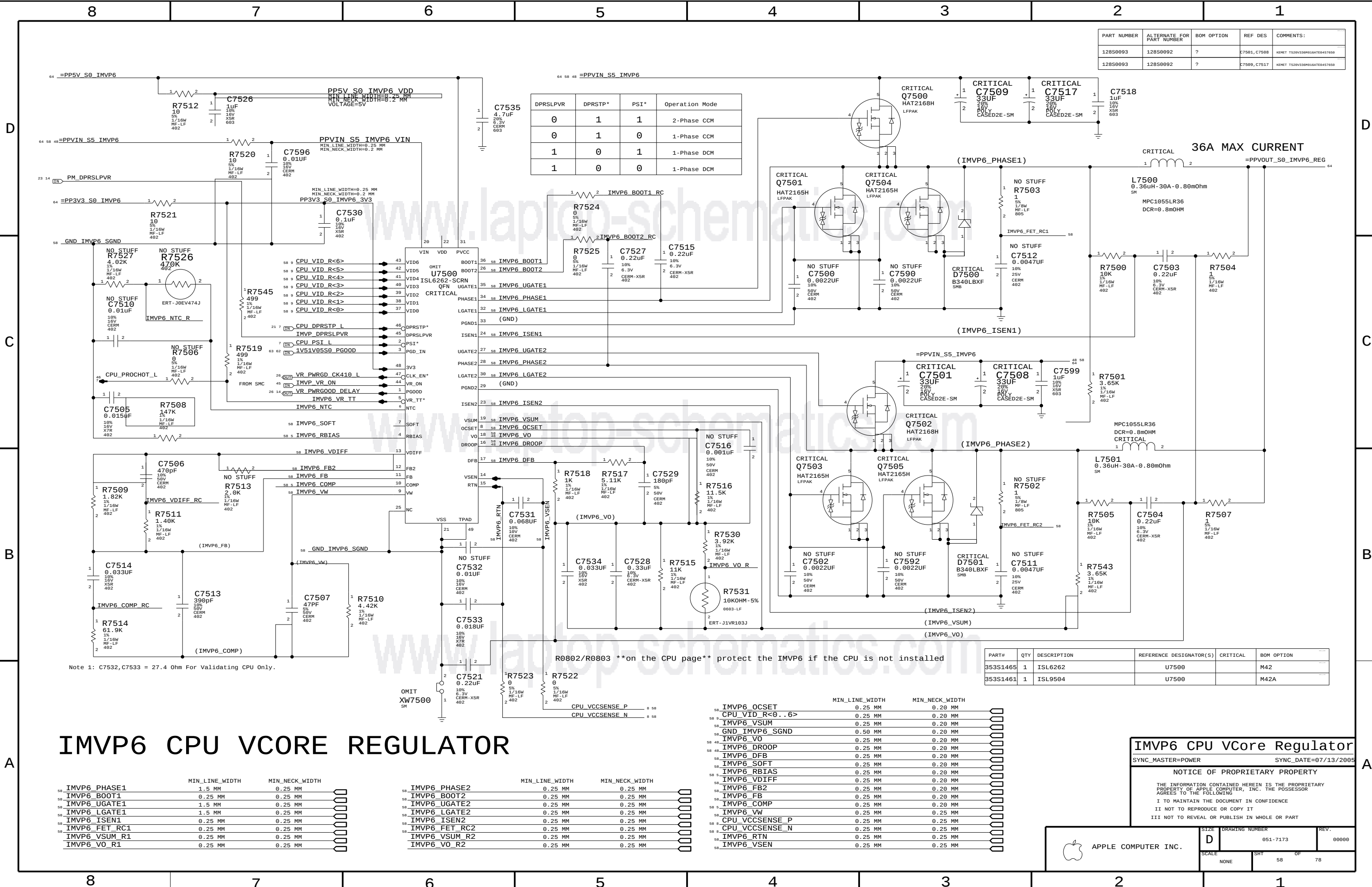
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SIZE	DRAWING NUMBER	REV.
D	051-7173	00000
SCALE	SHT	OF
NONE	57	78



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7501, C7508	KEKET 1520V330R0515ATE0457550
128S0093	128S0092	?	C7509, C7517	KEKET 1520V330R0515ATE0457550

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1465	1	ISL6262	U7500		M42
353S1461	1	ISL9504	U7500		M42A

IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
IMVP6_VO_R1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.25 MM	0.25 MM
IMVP6_VO_R2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
CPU_VID_R<0..6>	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DR00P	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P	0.25 MM	0.25 MM
CPU_VCCSENSE_N	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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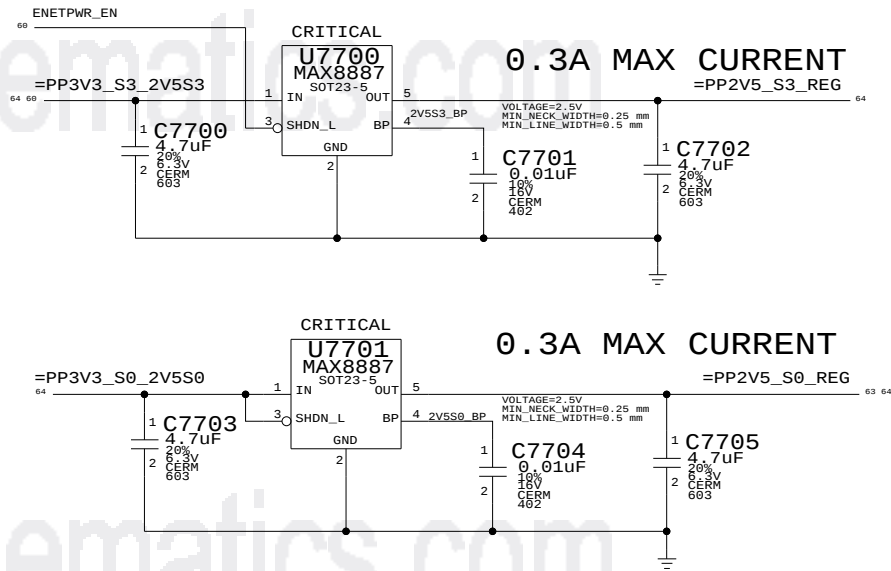
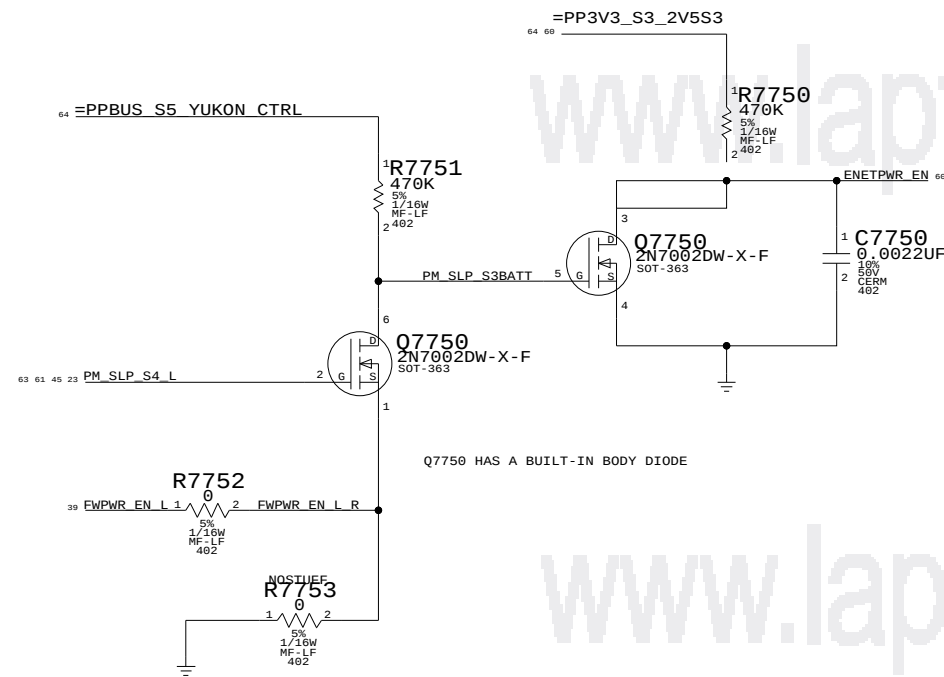


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SIZE	DRAWING NUMBER	REV.
D	051-7173	00000
SCALE	NONE	SHT 58 OF 78

YUKON POWER CONTROL

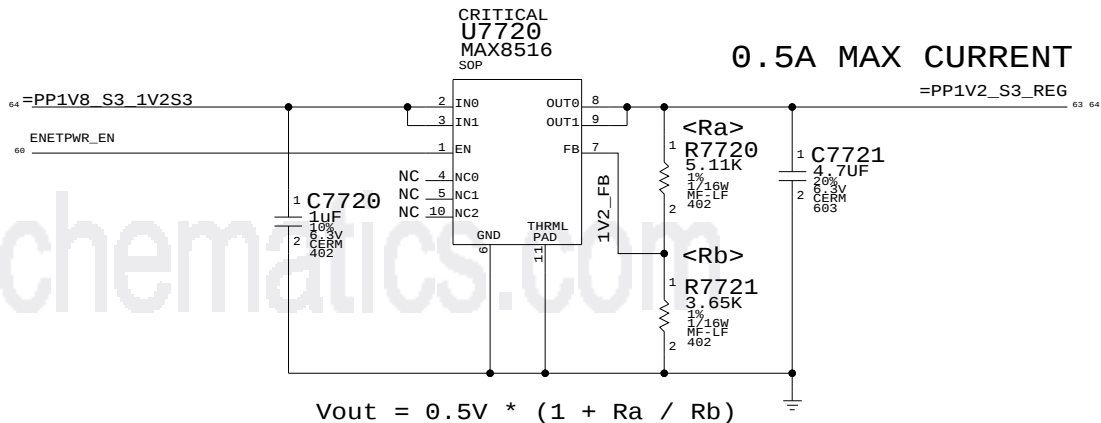
2.5V REGULATORS



1.2V REGULATOR

NAME	PM_SLP_S4_L	FWPWR_EN_L	PM_SLP_S3BATT	ENETPWR_EN
LOGIC	S3 S0	~S0 ~SMC_PS_ON		POWER YUKON
S3 ON BATTERY	TRUE (3.3V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S0 OR S3 ON AC	TRUE (3.3V)	FALSE (0V)	FALSE (0V)	TRUE (3.3V)
S5 ON AC	FALSE (0V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S5 ON BATT	FALSE (0V)	FALSE (0V)	TRUE (PBUS 12.6V)	FALSE (0V)

NOTE: IF CHANGE TO STUFFING R7753 THEN ENETPWR_EN IS BUFFERED PM_SLP_S4_L



$$V_{out} = 0.5V * (1 + R_a / R_b)$$

2.5V/1.2V Regulator

SYNC_MASTER=ENET SYNC_DATE=12/06/2005

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APPLE COMPUTER INC.

SIZE D

DRAWING NUMBER 051-7173

REV. 00000

SCALE NONE

SHT 60

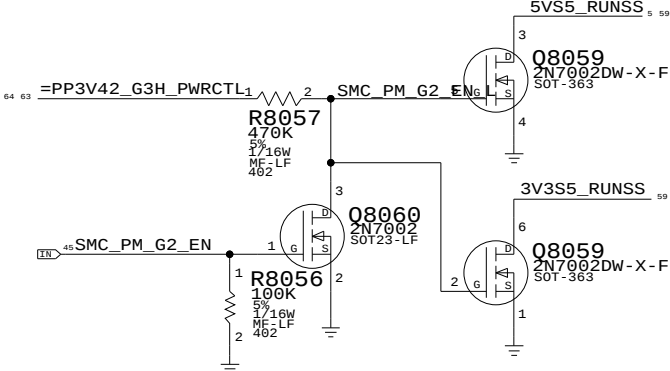
OF 78

POWER CONTROL SIGNALS

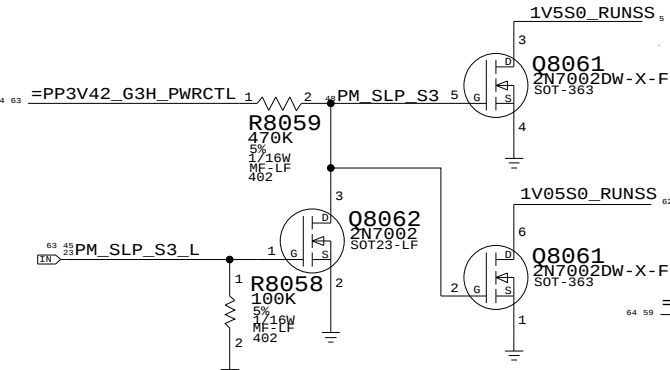
These rails are monitored by LTC2908

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

5V/3.3V S5 RUN/SS CONTROL



1.5V/1.05V S0 RUN/SS CONTROL



5V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	100 mA

3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	1 A

5V S0 FET

MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	3 A

3.3V S0 FET

MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	2 A

1.2V S0 FET

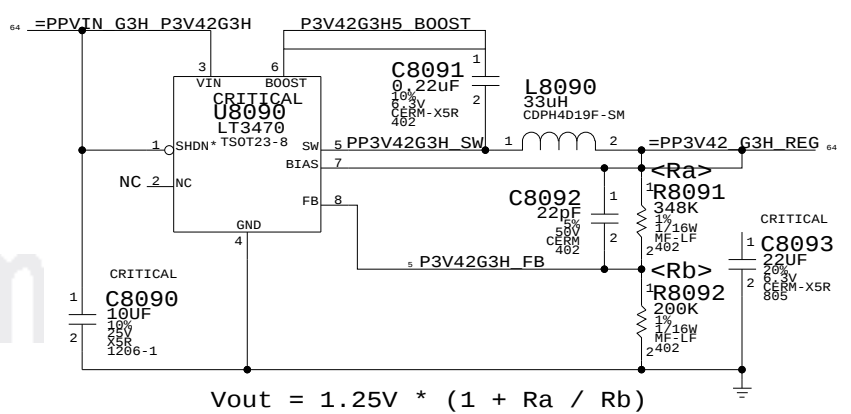
MOSFET	2N7002
CHANNEL	N-TYPE
RDS(ON)	13.5 Ohm
LOADING	Nothing

1.8V S0 FET

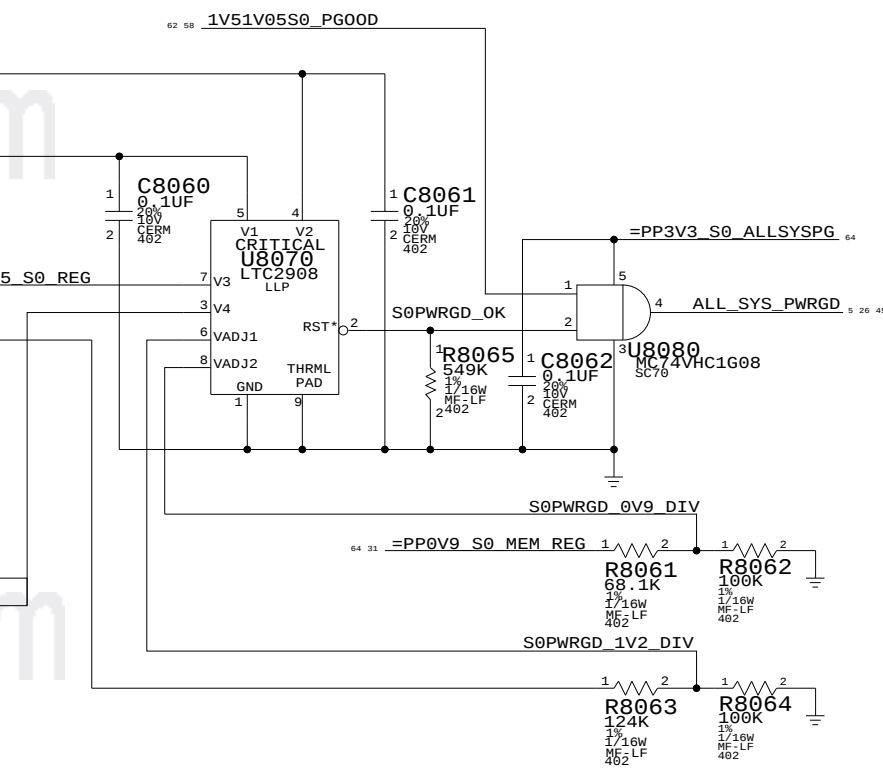
MOSFET	SI3447BDV
CHANNEL	P-TYPE
RDS(ON)	72 mOhm @1.8V
LOADING	320 mA

3.425V "G3Hot" SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



ALL SYSTEM PWRGD CIRCUIT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0445	2	FAIRCHILD FDM6296	Q8005, Q8015	FET_FDM6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	Q8005, Q8015	VISHAY SI7806ADN

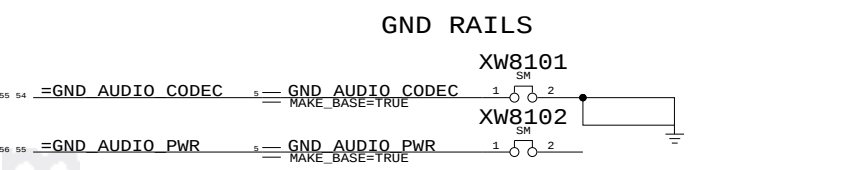
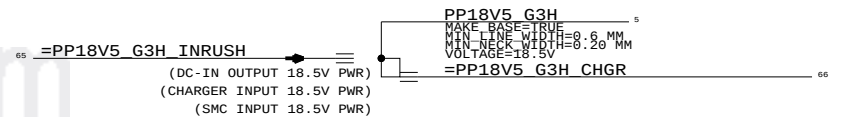
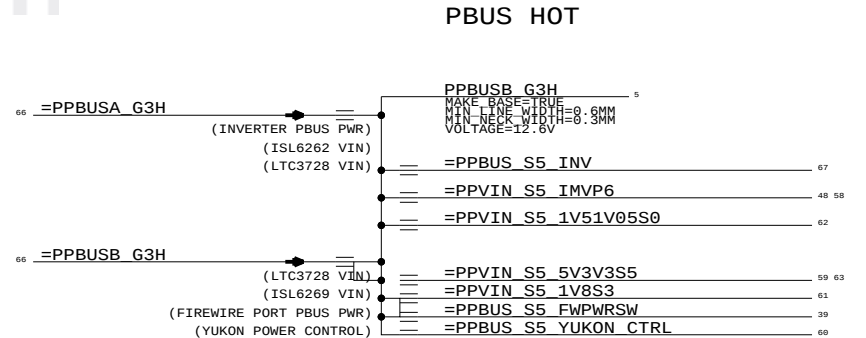
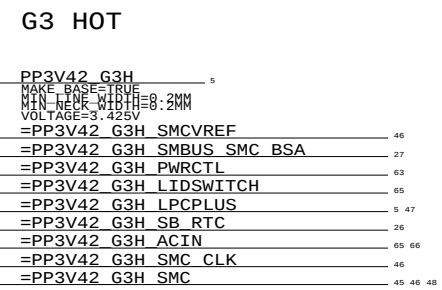
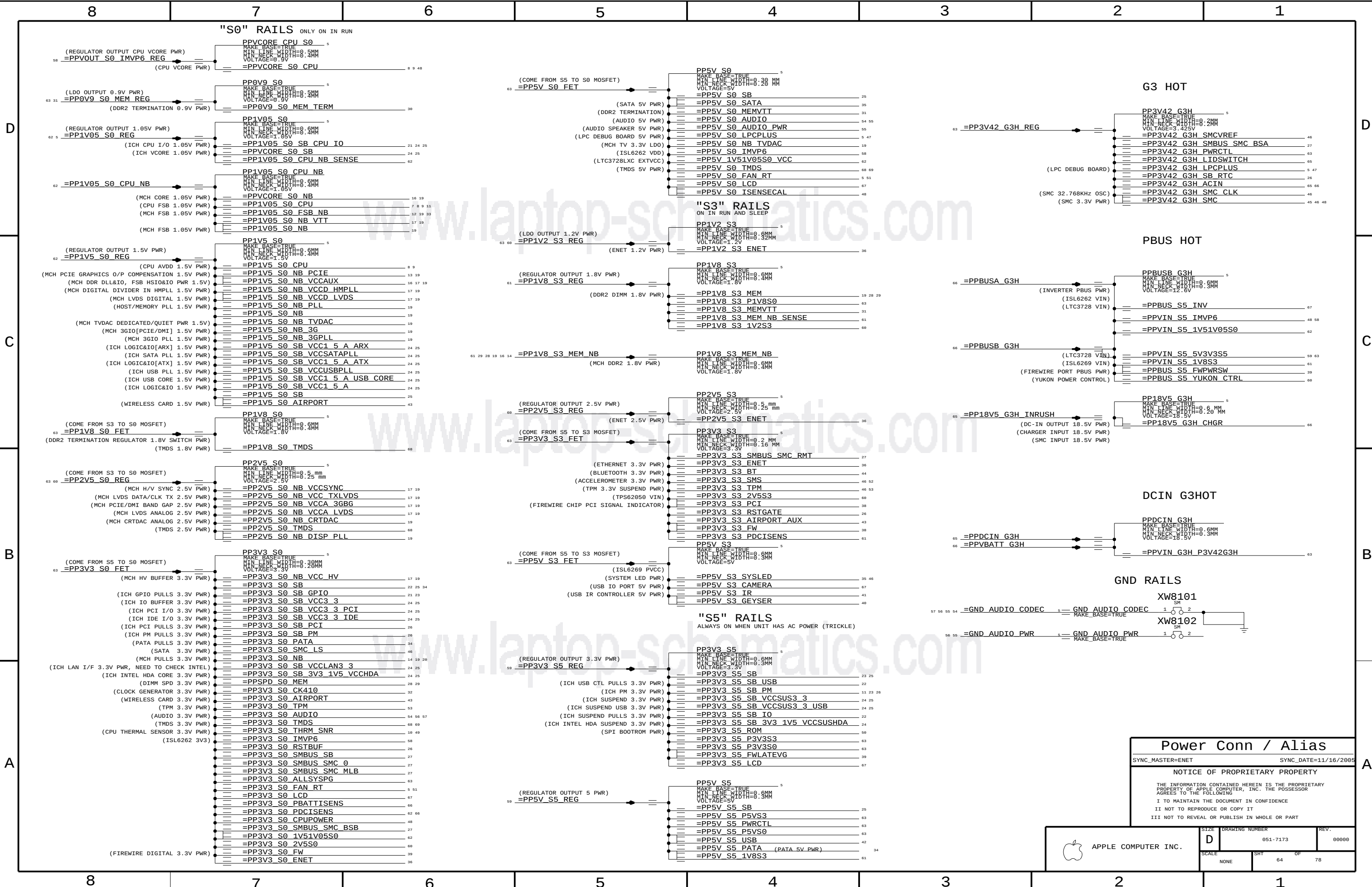
S3/S0 FETS, G3H SUPPLY

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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	D	051-7173	00000
SCALE	NONE	SHT	63 OF 78



Power Conn / Alias

SYNC_MASTER=ENET SYNC_DATE=11/16/2005

NOTICE OF PROPRIETARY PROPERTY

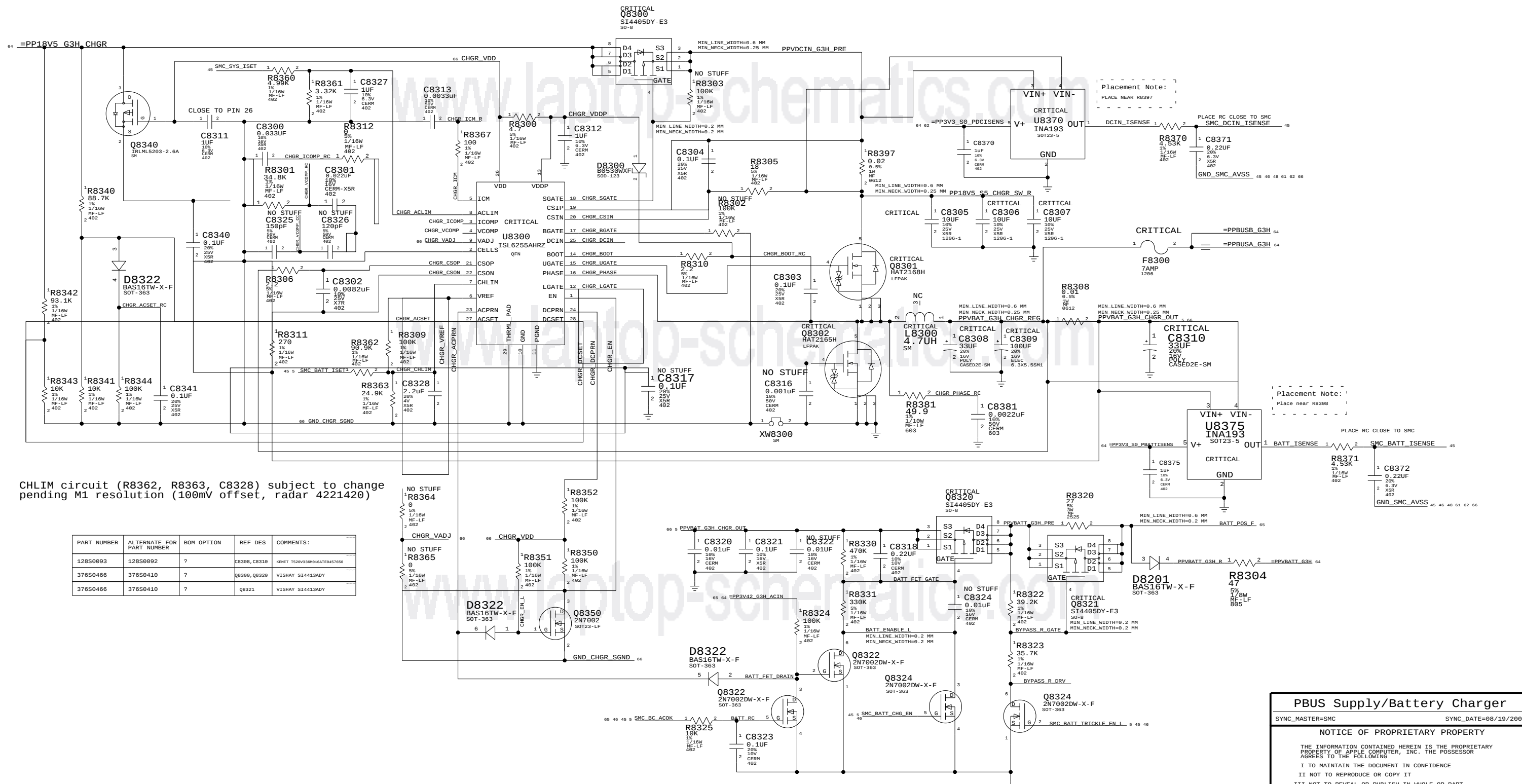
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PBUS SUPPLY / BATTERY CHARGER



CHLIM circuit (R8362, R8363, C8328) subject to change pending M1 resolution (100mV offset, radar 4221420)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
12850093	12850092	?	C8308, C8310	KEMET TS20V33M018ATE0457650
376S0466	376S0410	?	Q8300, Q8320	VISHAY SI4413ADY
376S0466	376S0410	?	Q8321	VISHAY SI4413ADY

PBUS Supply/Battery Charger

SYNC_MASTER=SMC

SYNC_DATE=08/19/2005

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SCALE

NONE

D

851-7173

00000

SCALE

SHT

66

OF

78

D

C

B

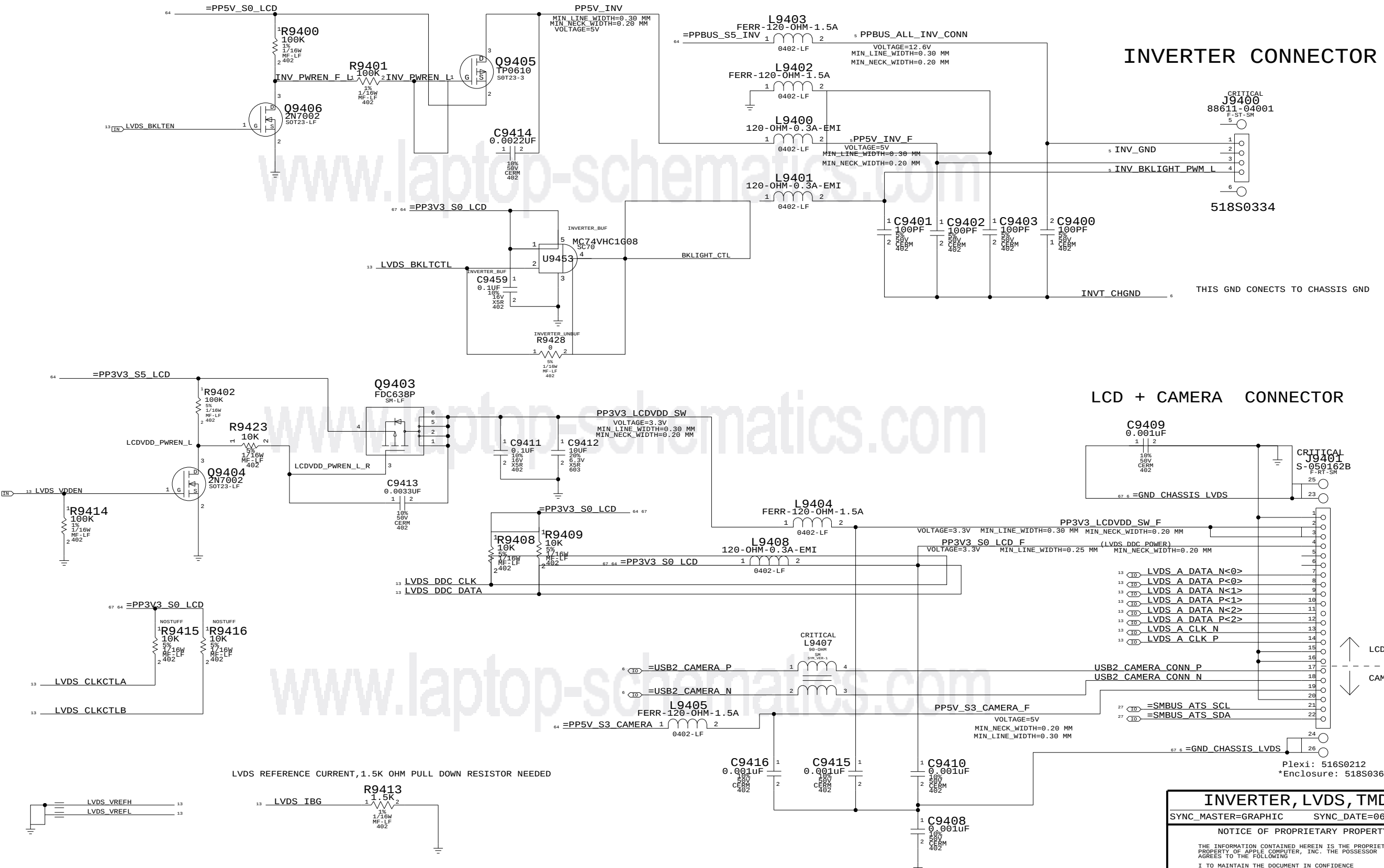
A

D

C

B

A



INVERTER, LVDS, TMDS

SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005

NOTICE OF PROPRIETARY PROPERTY

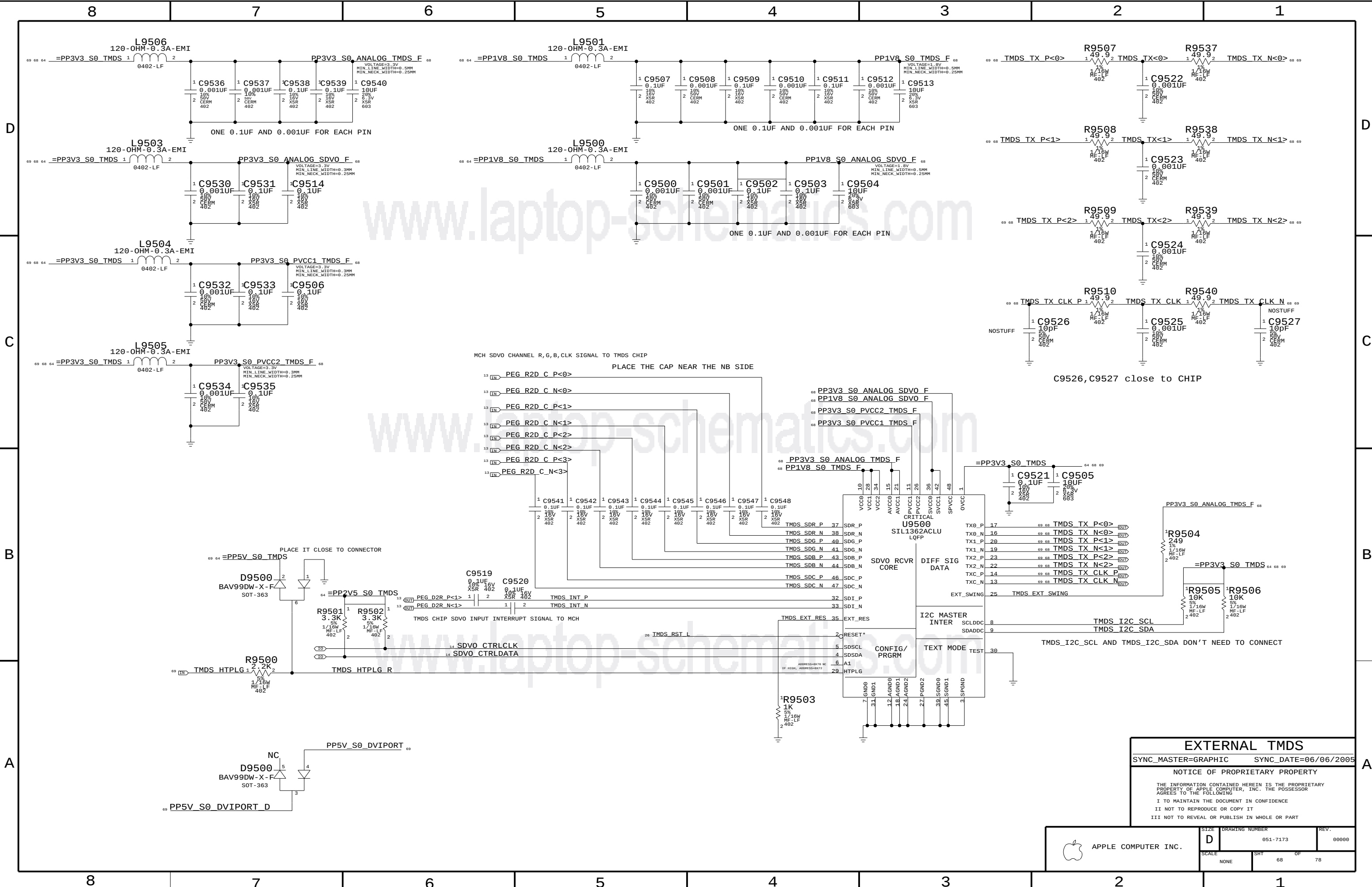
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NONE		67	78



EXTERNAL TMSD
SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	VIDEO, VIDEO, VIDEO	KEEP MAG LAYER IN BOM

Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

TMDS(MINI DVI) INTERFACE

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

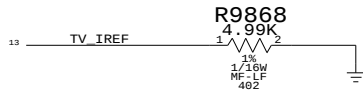
Isolation required for DVI power switch

DVI power DIODE on page 95 (D9500)

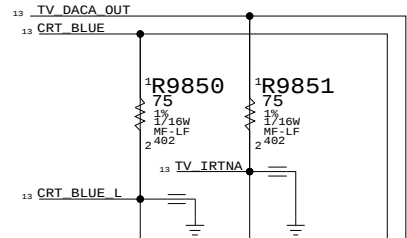
A 255 OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND



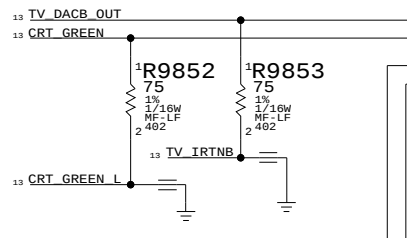
TV REFERENCE CURRENT, USES AN EXTERNAL RESISTOR OF 5K OHM 1% TO SET INTERNAL VOLTAGE LEVELS



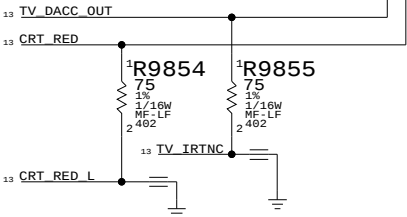
PLACE THE RESISTOR CLOSE TO GMCH



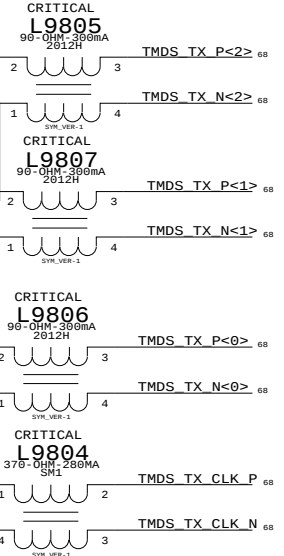
PLACE THE RESISTOR CLOSE TO GMCH



PLACE THE RESISTOR CLOSE TO GMCH



OMIT CRITICAL J9801 MINI-DVI RT-TH



MINI-DVI CONNECTOR

SYNC_MASTER=EUGENE SYNC_DATE=05/21/05

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0292	1	CONN, 32P MINI-DVI RCPT, RA, MG3, LF	J9801	CRITICAL	NORMAL
514-0319	1	CONN, 32P MINI-DVI RCPT, RA, BLACK, LF	J9801	CRITICAL	FANCY



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	00000
SCALE	SHT	OF
NONE	69	78

[illegible]

[illegible]

	8	7	6	5	4	3	2	1	
D	TP_NB_XOR_LVDS_D27 TP_NB_XOR_LVDS_D28 TP_PCI_GNT0_L TP_PCI_GNT1_L TP_PCI_GNT2_L TP_PCI_PME_L TP_SB_ACZ_SDIN1 TP_SB_ACZ_SDIN2 TP_SB_DRQ0_L TP_SB_GPI06 TP_SB_GPI022 TP_SB_GPI023 TP_SB_GPI025_DO_NOT_USE TP_SB_GPI038 TP_SB_RCVENIN_L TP_SB_RSVD9 TP_SB_SATALED_L TP_SB_XOR_A05 TP_SB_XOR_A09 TP_SB_XOR_AE5 TP_SB_XOR_AG4 TP_SB_XOR_AH4 TP_SB_XOR_U3 TP_SB_XOR_U7 TP_SB_XOR_V6 TP_SB_XOR_V7 TP_SB_XOR_Y1 TP_SB_XOR_Y2 TP_SB_XOR_AE9 TP_SB_XOR_AG8 TP_SB_XOR_AH8 TP_SB_XOR_W1 TP_USBN_F TP_USBP_F TV_DACA_OUT TV_DACB_OUT TV_DACC_OUT TV_IREF USB2_BT_F_N USB2_BT_F_P USB2_CAMERA_CONN_N USB2_CAMERA_CONN_P USB2_EXT_A_F_N USB2_EXT_A_F_P USB2_EXTB_F_N USB2_EXTB_F_P USB2_GND_EXT_A_F USB2_GND_EXTB_F USB_A_N USB_A_OC_L USB_A_P USB_B_N USB_B_OC_L USB_B_P USB_C_N USB_C_P USB_D_OC_L USB_E_N USB_E_OC_L USB_E_P USB_F_N USB_F_P USB_G_N USB_G_P USB_RBIAS_PN VGA_B VGA_G VGA_HSYNC VGA_R VGA_VSYNC VOL_DOWN VOL_UP VREG_FB VR_PWRGD_CK410 VR_PWRGOOD_DELAY XDP_BPM_L<8> XDP_BPM_L<1> XDP_BPM_L<2> XDP_BPM_L<3> XDP_BPM_L<4> XDP_BPM_L<5> XDP_DBRESET_L XDP_TCK XDP_TDI XDP_TDO	TP_NB_XOR_LVDS_D27 - @m42a_lib.M42A TP_NB_XOR_LVDS_D28 - @m42a_lib.M42A TP_PCI_GNT0_L - @m42a_lib.M42A TP_PCI_GNT1_L - @m42a_lib.M42A TP_PCI_GNT2_L - @m42a_lib.M42A TP_PCI_PME_L - @m42a_lib.M42A TP_SB_ACZ_SDIN1 - @m42a_lib.M42A TP_SB_ACZ_SDIN2 - @m42a_lib.M42A TP_SB_DRQ0_L - @m42a_lib.M42A TP_SB_GPI06 - @m42a_lib.M42A TP_SB_GPI022 - @m42a_lib.M42A =SB_GPI022 - @m42a_lib.M42A SB_GPI022 - @m42a_lib.M42A =SB_GPI022 - @m42a_lib.M42A TP_SB_GPI023 - @m42a_lib.M42A TP_SB_GPI025_DO_NOT_USE - @m42a_lib.M42A TP_SB_GPI038 - @m42a_lib.M42A TP_SB_RCVENIN_L - @m42a_lib.M42A TP_SB_RSVD9 - @m42a_lib.M42A TP_SB_SATALED_L - @m42a_lib.M42A TP_SB_XOR_A05 - @m42a_lib.M42A TP_SB_XOR_A09 - @m42a_lib.M42A TP_SB_XOR_AE5 - @m42a_lib.M42A TP_SB_XOR_AG4 - @m42a_lib.M42A TP_SB_XOR_AH4 - @m42a_lib.M42A TP_SB_XOR_U3 - @m42a_lib.M42A TP_SB_XOR_U7 - @m42a_lib.M42A TP_SB_XOR_V6 - @m42a_lib.M42A TP_SB_XOR_V7 - @m42a_lib.M42A TP_SB_XOR_Y1 - @m42a_lib.M42A TP_SB_XOR_Y2 - @m42a_lib.M42A TP_SB_XOR_AE9 - @m42a_lib.M42A TP_SB_XOR_AG8 - @m42a_lib.M42A TP_SB_XOR_AH8 - @m42a_lib.M42A TP_SB_XOR_W1 - @m42a_lib.M42A TP_USBN_F - @m42a_lib.M42A TP_USBP_F - @m42a_lib.M42A TV_DACA_OUT - @m42a_lib.M42A TV_DACB_OUT - @m42a_lib.M42A TV_DACC_OUT - @m42a_lib.M42A TV_IREF - @m42a_lib.M42A USB2_BT_F_N - @m42a_lib.M42A USB2_BT_F_P - @m42a_lib.M42A USB2_CAMERA_CONN_N - @m42a_lib.M42A USB2_CAMERA_CONN_P - @m42a_lib.M42A USB2_EXT_A_F_N - @m42a_lib.M42A USB2_EXT_A_F_P - @m42a_lib.M42A USB2_EXTB_F_N - @m42a_lib.M42A USB2_EXTB_F_P - @m42a_lib.M42A USB2_GND_EXT_A_F - @m42a_lib.M42A USB2_GND_EXTB_F - @m42a_lib.M42A USB_A_N - @m42a_lib.M42A =USB2_EXT_A_N - @m42a_lib.M42A USB2_EXT_A_N - @m42a_lib.M42A =USB2_EXT_A_N - @m42a_lib.M42A USB_A_OC_L - @m42a_lib.M42A =EXTAUSB_OC_L - @m42a_lib.M42A EXTAUSB_OC_L - @m42a_lib.M42A =EXTAUSB_OC_L - @m42a_lib.M42A USB_A_P - @m42a_lib.M42A =USB2_EXT_A_P - @m42a_lib.M42A USB2_EXT_A_P - @m42a_lib.M42A =USB2_EXT_A_P - @m42a_lib.M42A USB_B_N - @m42a_lib.M42A =USB2_GEYSER_N - @m42a_lib.M42A USB2_GEYSER_N - @m42a_lib.M42A =USB2_GEYSER_N - @m42a_lib.M42A USB_B_OC_L - @m42a_lib.M42A USB_B_P - @m42a_lib.M42A =USB2_GEYSER_P - @m42a_lib.M42A USB2_GEYSER_P - @m42a_lib.M42A =USB2_GEYSER_P - @m42a_lib.M42A USB_C_N - @m42a_lib.M42A =USB2_EXTB_N - @m42a_lib.M42A USB2_EXTB_N - @m42a_lib.M42A =USB2_EXTB_N - @m42a_lib.M42A USB_C_P - @m42a_lib.M42A =USB2_EXTB_P - @m42a_lib.M42A USB2_EXTB_P - @m42a_lib.M42A =USB2_EXTB_P - @m42a_lib.M42A USB_D_OC_L - @m42a_lib.M42A USB_E_N - @m42a_lib.M42A TP_USBN_E - @m42a_lib.M42A USB_E_OC_L - @m42a_lib.M42A USB_E_P - @m42a_lib.M42A TP_USBP_E - @m42a_lib.M42A USB_F_N - @m42a_lib.M42A =USB2_IR_N - @m42a_lib.M42A USB_IR_N - @m42a_lib.M42A =USB2_IR_N - @m42a_lib.M42A USB_F_P - @m42a_lib.M42A =USB2_IR_P - @m42a_lib.M42A USB_IR_P - @m42a_lib.M42A =USB2_IR_P - @m42a_lib.M42A USB_G_N - @m42a_lib.M42A =USB2_BT_N - @m42a_lib.M42A USB_BT_N - @m42a_lib.M42A =USB2_BT_N - @m42a_lib.M42A USB_G_P - @m42a_lib.M42A =USB2_BT_P - @m42a_lib.M42A USB_BT_P - @m42a_lib.M42A =USB2_BT_P - @m42a_lib.M42A USB_RBIAS_PN - @m42a_lib.M42A VGA_B - @m42a_lib.M42A VGA_G - @m42a_lib.M42A VGA_HSYNC - @m42a_lib.M42A VGA_R - @m42a_lib.M42A VGA_VSYNC - @m42a_lib.M42A VOL_DOWN - @m42a_lib.M42A VOL_UP - @m42a_lib.M42A VREG_FB - @m42a_lib.M42A VR_PWRGD_CK410 - @m42a_lib.M42A VR_PWRGOOD_DELAY - @m42a_lib.M42A XDP_BPM_L<8> - @m42a_lib.M42A XDP_BPM_L<1> - @m42a_lib.M42A XDP_BPM_L<2> - @m42a_lib.M42A XDP_BPM_L<3> - @m42a_lib.M42A XDP_BPM_L<4> - @m42a_lib.M42A XDP_BPM_L<5> - @m42a_lib.M42A XDP_DBRESET_L - @m42a_lib.M42A XDP_TCK - @m42a_lib.M42A XDP_TDI - @m42a_lib.M42A XDP_TDO - @m42a_lib.M42A	14C6 14C6 22B6 22B6 22B6 22A6 21C6 21C6 21D4 23C5 681 22B6 682 69A6 682 682 69A6 21D5 23C3 23C3 15B2 22A6 21C6 22A7 22A7 22A7 22A7 21C6 21C6 21C6 21C6 21C6 21C6 21C6 22A6 22A6 21C6 5C1 5C1 13C5 69B8 13C5 69A8 13C5 69A8 13C5 69C8 44C4 44B4 67A2 67B2 42C2 42C2 42B2 42B2 42C2 42B2 6C1 22C2 6C2 42C5 6C2 6C2 42C5 6C1 22C4 22D8 6C2 42C8 6C2 6C2 42C8 6C1 22C2 6C2 42C5 6C2 6C2 42C5 6C1 22C2 6C2 48C7 6C2 6C2 48C7 6C1 22C2 6C2 48C7 6C2 6C2 48C7 6C1 22C2 6C2 42B5 6C2 6C2 42B5 6C2 22C4 22D8 6C1 22C2 5C1 6C2 22C4 22D8 6C1 22C2 5C1 6C2 6C1 22C2 6C2 41C6 6C2 6C2 41C6 6C1 22C2 6C2 41C6 6C2 6C2 41C6 6C2 44C6 682 682 44C6 681 22C2 6C2 44C6 6C2 6C2 44C6 22C2 69B4 69B4 69B4 69C1 69A4 69B4 69C1 54B7 54C7 54B7 54C7 54A4 23C5 26A8 14B6 26B5 58C7 7C6 11B2 7C6 11B2 7C6 11B2 7C6 11B3 7C6 11B2 7C6 11B2 7C6 11B4 26C6 7A8 7C6 11B2 11B3 7B8 7C6 11B3 7C6 11B5		XDP_TMS XDP_TRST_L	XDP_TMS - @m42a_lib.M42A XDP_TRST_L - @m42a_lib.M42A	7B8 7C6 11B2 7C6 11B3		

