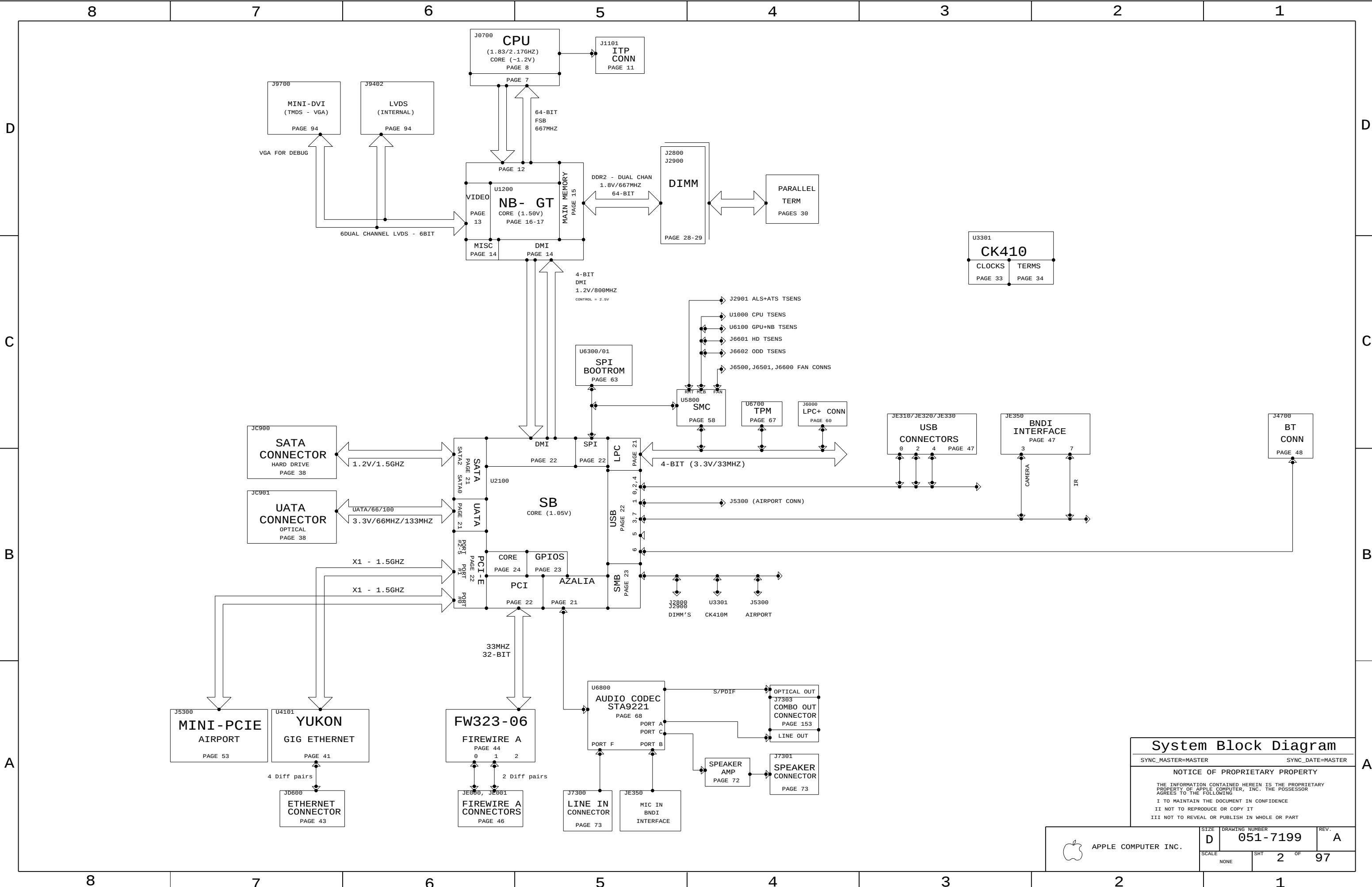


8		7		6		5		4		3		2		1					
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.														REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.																		DATE	DATE
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.																		07/26/06	06/22/04
IMAC 5,2 - - REV A																			
7/25/06																			
D	PDF	CSA	CONTENTS	SYNC	MASTER	DATE	PDF	CSA	CONTENTS	SYNC	MASTER	DATE							
	2	2	System Block Diagram		MASTER	MASTER	38	44	FW: FW323-06		MASTER	MASTER							
	3	3	Power Block Diagram		MASTER	MASTER	39	45	FW: DECAPS		MASTER	MASTER							
	4	4	Table Items		MASTER	MASTER	40	46	FIREWIRE CONNECTORS		MASTER	MASTER							
	5	5	FUNC TEST 1 OF 2		MASTER	MASTER	41	47	USB Device Interfaces		MASTER	MASTER							
C	6	6	Power Conn / Alias		MASTER	MASTER	42	53	AIRPORT CONN		MASTER	MASTER							
	7	7	CPU 1 OF 2-FSB		MASTER	MASTER	43	54	PCIE PORT ALIASES		MASTER	MASTER							
	8	8	CPU 2 OF 2-PWR/GND		MASTER	MASTER	44	58	SMC	M1		01/05/2006							
	9	9	CPU DECAPS & VID<>		MASTER	MASTER	45	59	SMC & TPM SUPPORT		(MASTER)	(MASTER)							
	10	10	CPU TEMP SENSOR		MASTER	MASTER	46	60	LPC+ CONN		M38	12/09/2005							
	11	11	CPU ITP700FLEX DEBUG		M38	01/05/2006	47	61	NB THERMAL		MASTER	MASTER							
	12	12	NB CPU Interface		M1	01/05/2006	48	63	SPI BOOTROM		M38	01/05/2006							
	13	13	NB PEG / Video Interfaces		M1	01/05/2006	49	65	Fan 0, 1 & System Temp		MASTER	MASTER							
	14	14	NB Misc Interfaces		MASTER	MASTER	50	66	Fan 2 & HD Temp		MASTER	MASTER							
	15	15	NB DDR2 Interfaces		M1	01/05/2006	51	67	TPM		M38	01/05/2006							
B	16	16	NB Power 1		MASTER	MASTER	52	68	AUDIO: CODEC		AUDIO	05/12/2006							
	17	17	NB Power 2		M40	01/05/2006	53	72	AUDIO: SPEAKER AMP		AUDIO	05/12/2006							
	18	18	NB Grounds		M1	01/05/2006	54	73	AUDIO: CONNECTORS		AUDIO	05/12/2006							
	19	19	NB (GM) Decoupling		(MASTER)	(MASTER)	55	74	AUDIO: POWER SUPPLIES		AUDIO	05/12/2006							
	20	20	NB Config Straps		M1	01/05/2006	56	75	IMVP6 CPU VCore Regulator		MASTER	MASTER							
	21	21	SB: 1 OF 4		M38	01/05/2006	57	76	CPU & SYSTEM SENSE CIRCUITS		(MASTER)	(MASTER)							
	22	22	SB: 2 OF 4		MASTER	MASTER	58	77	PWR GOOD		(MASTER)	(MASTER)							
	23	23	SB: 3 OF 4		MASTER	MASTER	59	78	3V DC/DC 2.5V		(MASTER)	(MASTER)							
	24	24	SB: 4 OF 4		M38	01/05/2006	60	79	1.8V & 1.2V VREG		MASTER	MASTER							
	25	25	SB:DECOUPLING		MASTER	MASTER	61	80	1.5V_S0 & 1.05V_S0 VREG		MASTER	MASTER							
A	26	26	SB: MISC		MASTER	MASTER	62	82	5V DC/DC		MASTER	MASTER							
	27	27	SB: SMB HUB AND ALIAS		MASTER	MASTER	63	83	S0 AND S3 FETS		MASTER	MASTER							
	28	28	DDR2 S0-DIMM Connector A		MASTER	MASTER	64	94	Internal Display Conns		MASTER	MASTER							
	29	29	DDR2 S0-DIMM Connector B		MASTER	MASTER	65	95	EXTERNAL TMDS		MASTER	MASTER							
	30	30	Memory Active Termination		MASTER	MASTER	66	96	TMDS/Inverter/ExtVGA		MASTER	MASTER							
	31	31	Memory Vtt Supply		MASTER	MASTER	67	97	External Display Conns		MASTER	MASTER							
	32	33	CLOCKS		MASTER	MASTER													
	33	34	CLOCKS: TERMINATIONS		MASTER	MASTER													
	34	38	Disk Connectors		MASTER	MASTER													
	35	41	ETHERNET CONTROLLER		MASTER	MASTER													
36	42	ETHERNET MISC		MASTER	MASTER														
37	43	ETHERNET CONNECTOR		MASTER	MASTER														
8		7		6		5		4		3		2		1					

DIMENSIONS ARE IN MILLIMETERS				METRIC				Apple Computer Inc.			
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 THIRD ANGLE PROJECTION				RELEASE				TITLE			
				SCALE				SCHEM VALLCO			
				MATERIAL/FINISH NOTED AS APPLICABLE				DRAWING NUMBER			
				SIZE D				051-7199			
								REV. A			
								SHT 1 OF 97			



System Block Diagram

SYNC_MASTER=MASTER

SYNC_DATE=MASTER

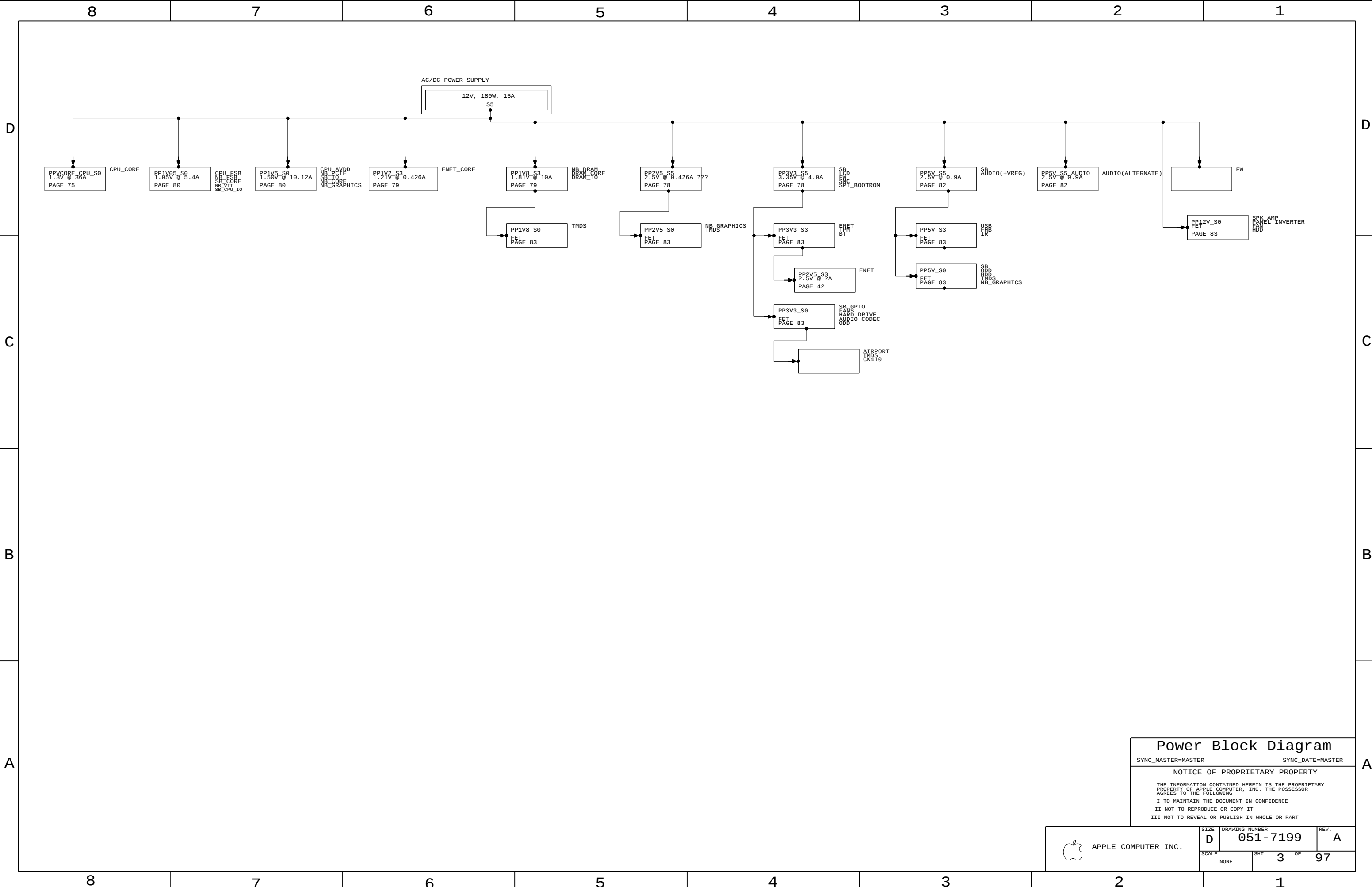
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Power Block Diagram

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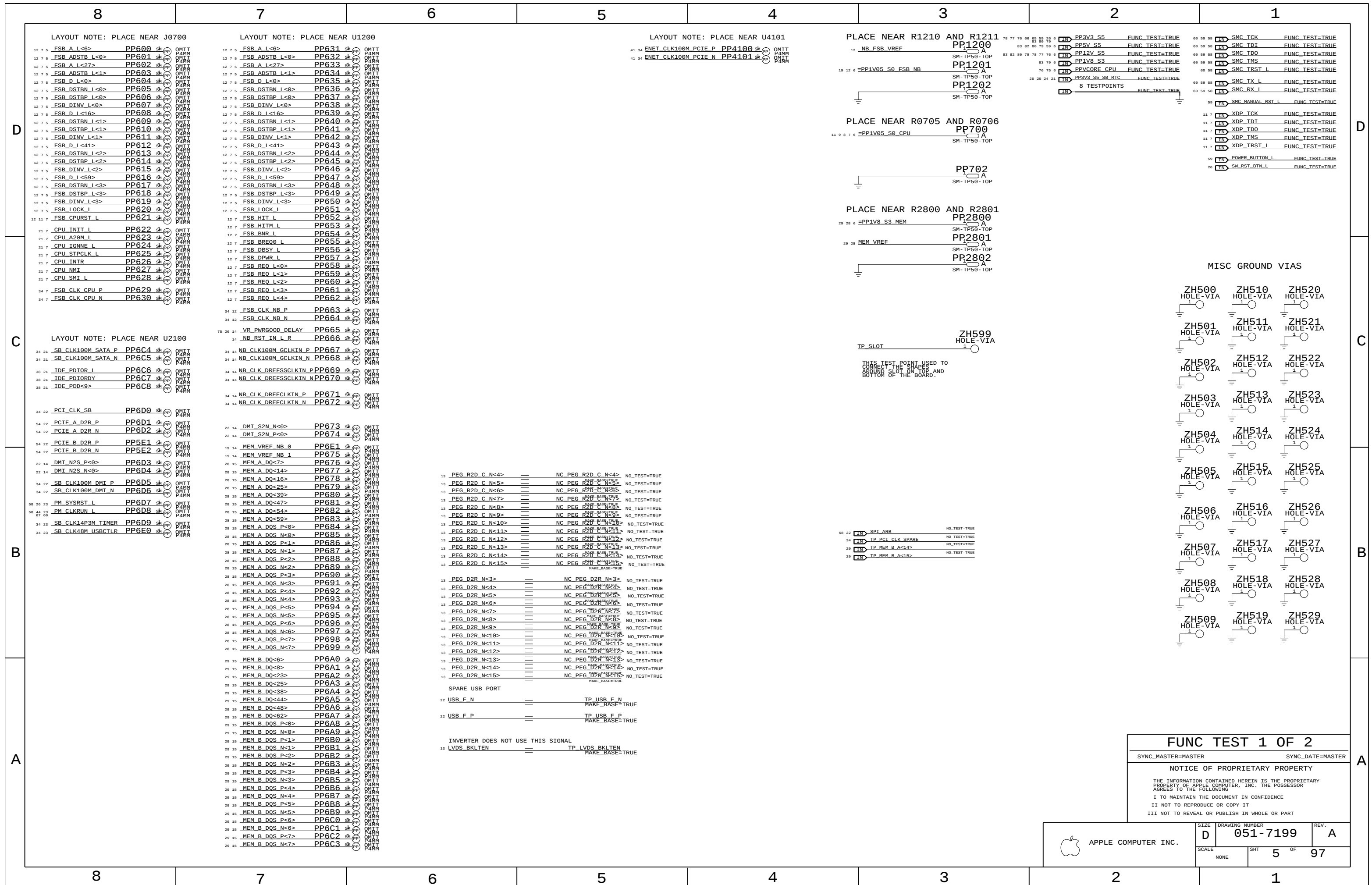
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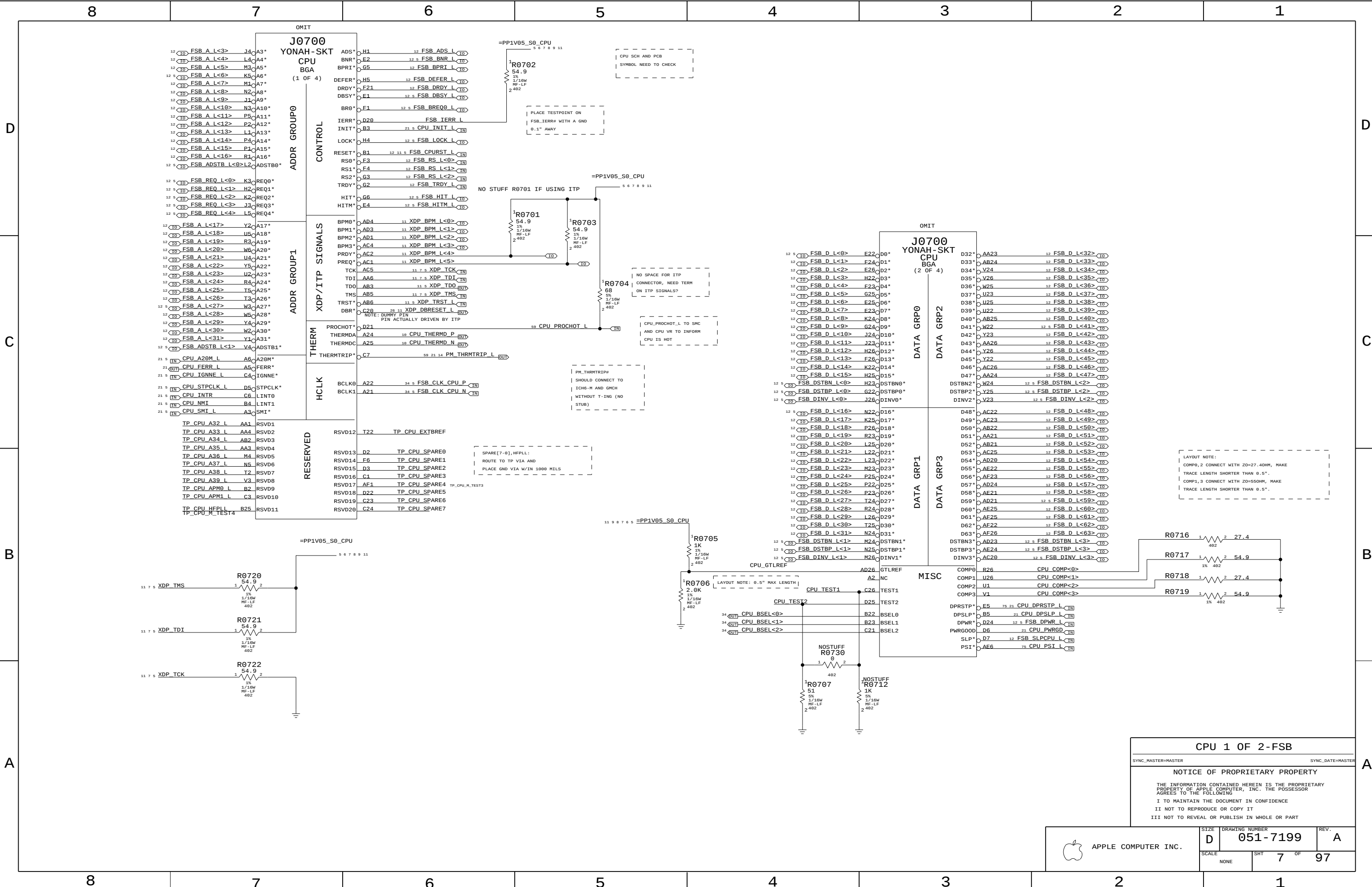
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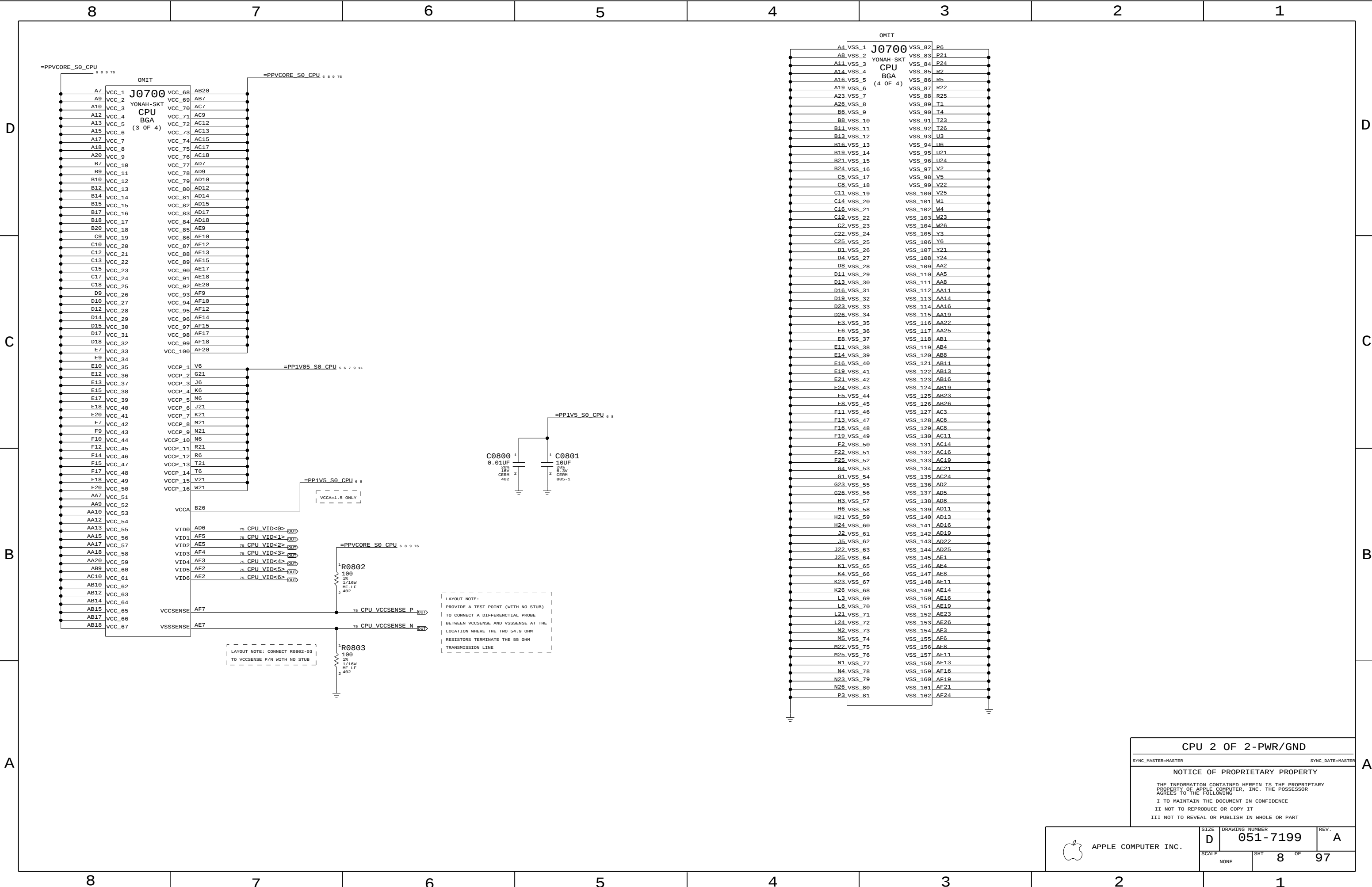
3

OF

97







CPU 2 OF 2 - PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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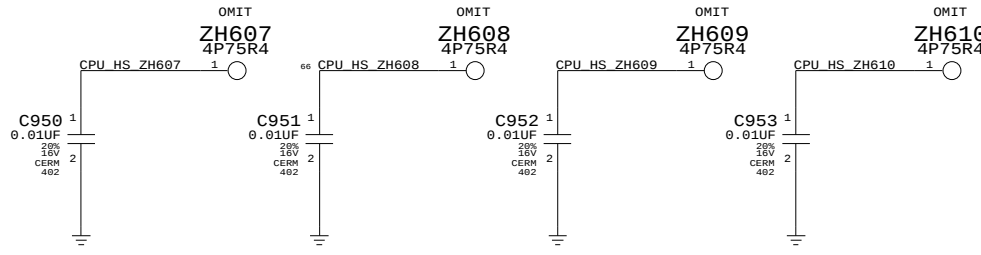
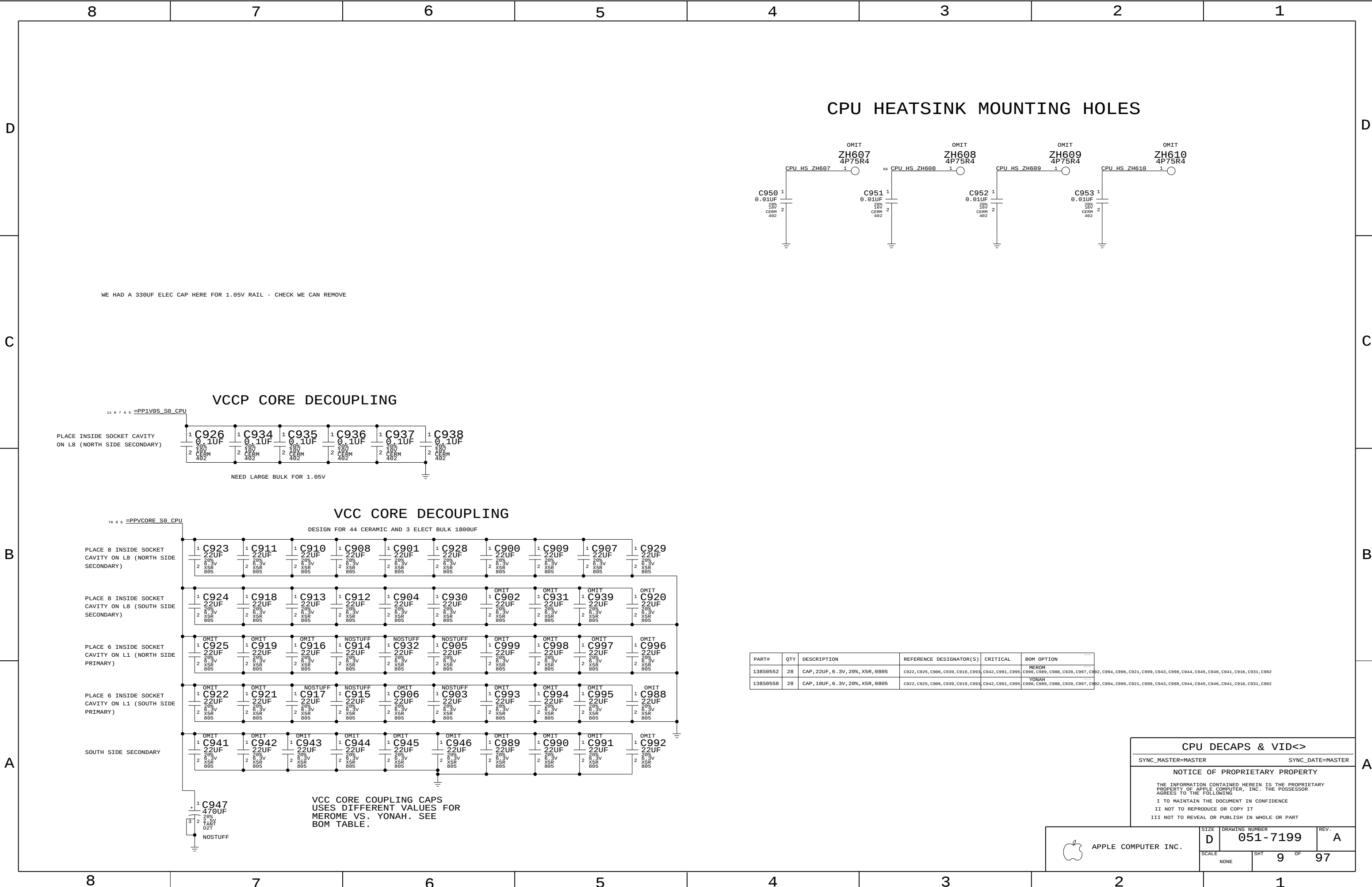
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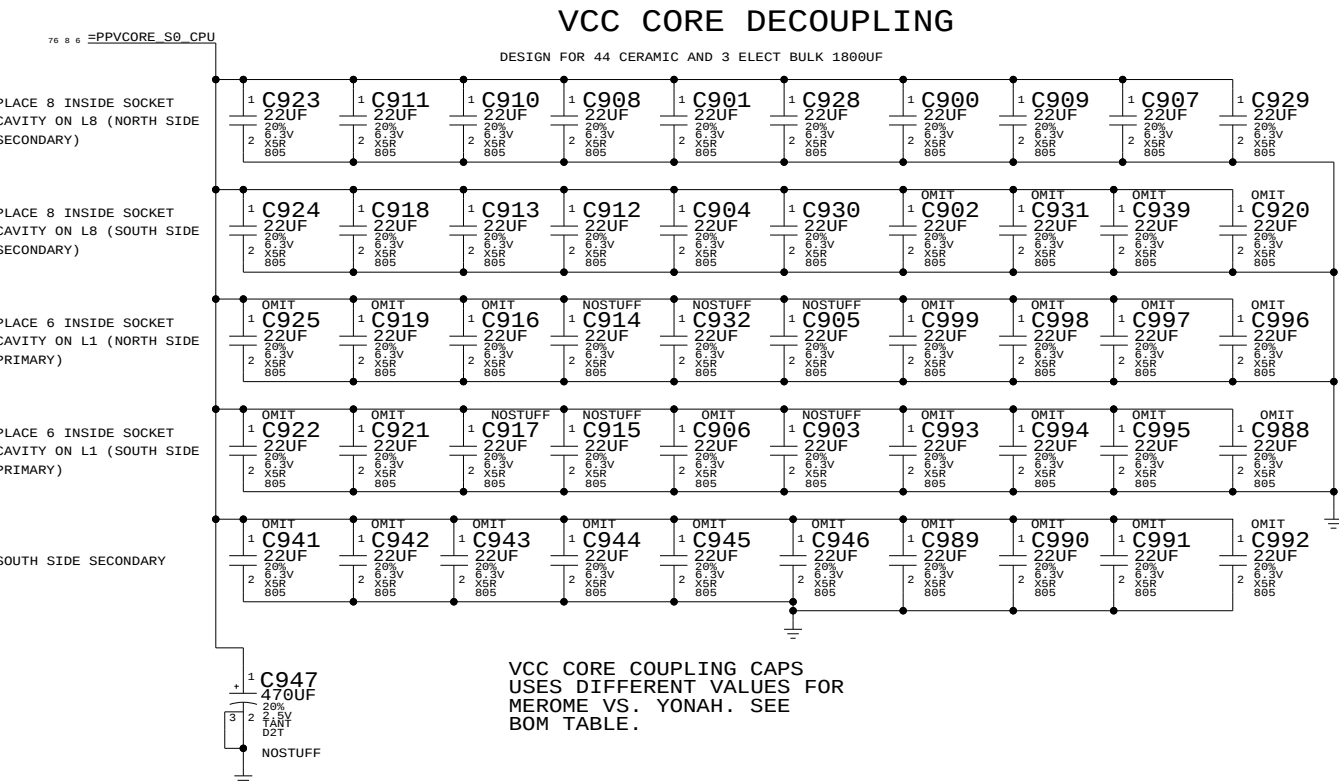
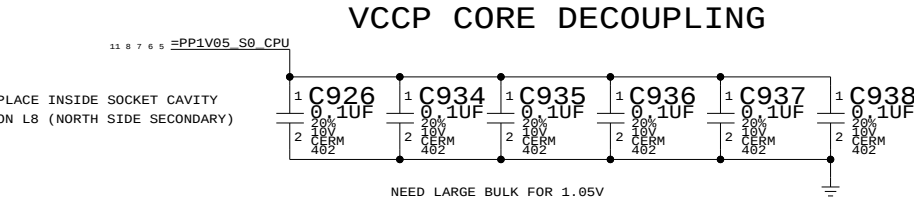
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	D	051-7199	A
SCALE		SHT	8 OF 97
NONE			



WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP, 22UF, 6.3V, 20%, X5R, 805	C922, C925, C906, C939, C919, C993, C942, C991, C995, C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902		MEROM
138S0558	28	CAP, 10UF, 6.3V, 20%, X5R, 805	C922, C925, C906, C939, C919, C993, C942, C991, C995, C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902		YONAH

CPU DECAPS & VID<>

SYNC_MASTER=MASTER SYNC_DATE=MASTER

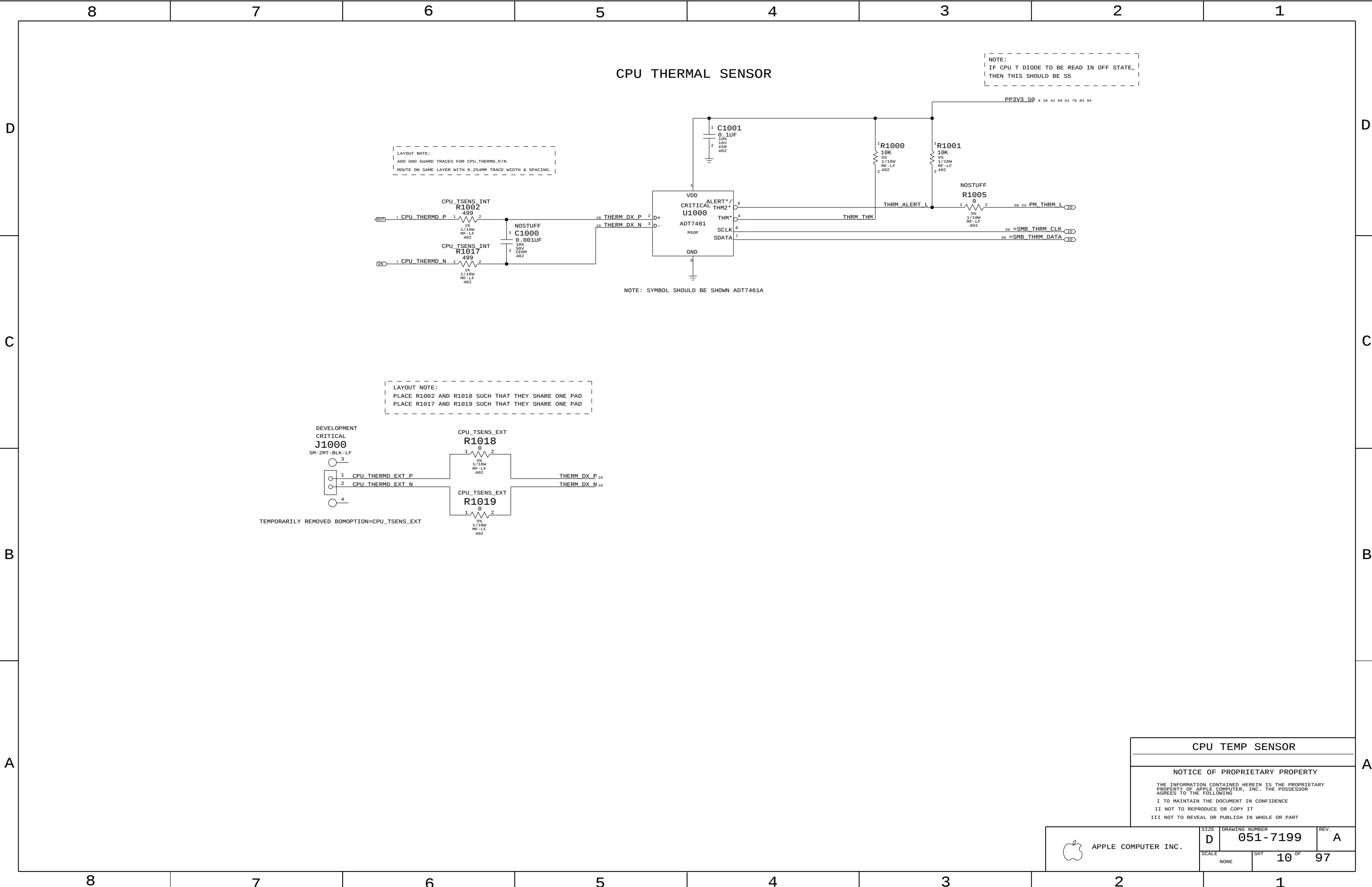
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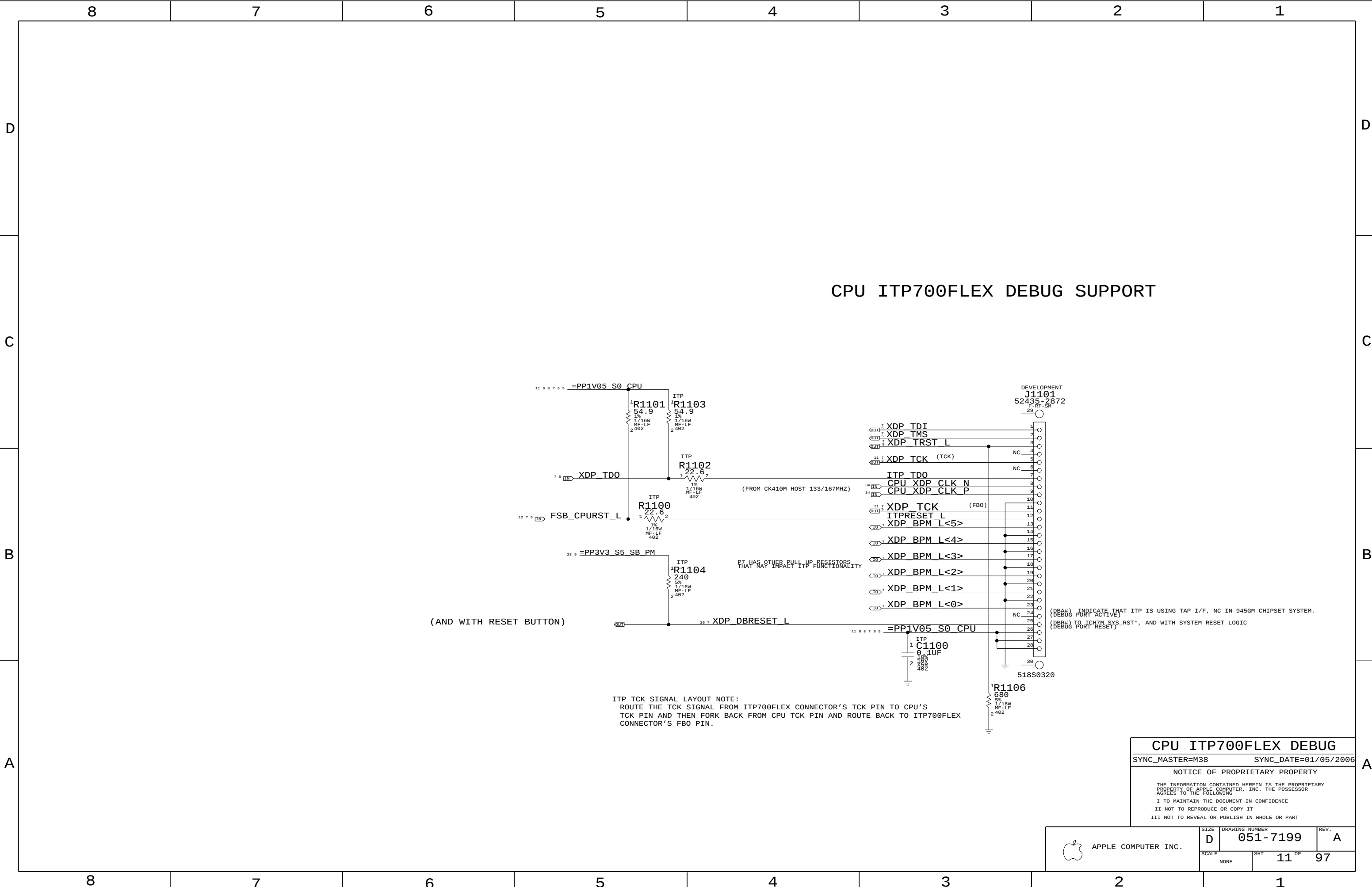
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CPU TEMP SENSOR		
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SCALE NONE	SHT 10 OF 97	



CPU ITP700FLEX DEBUG

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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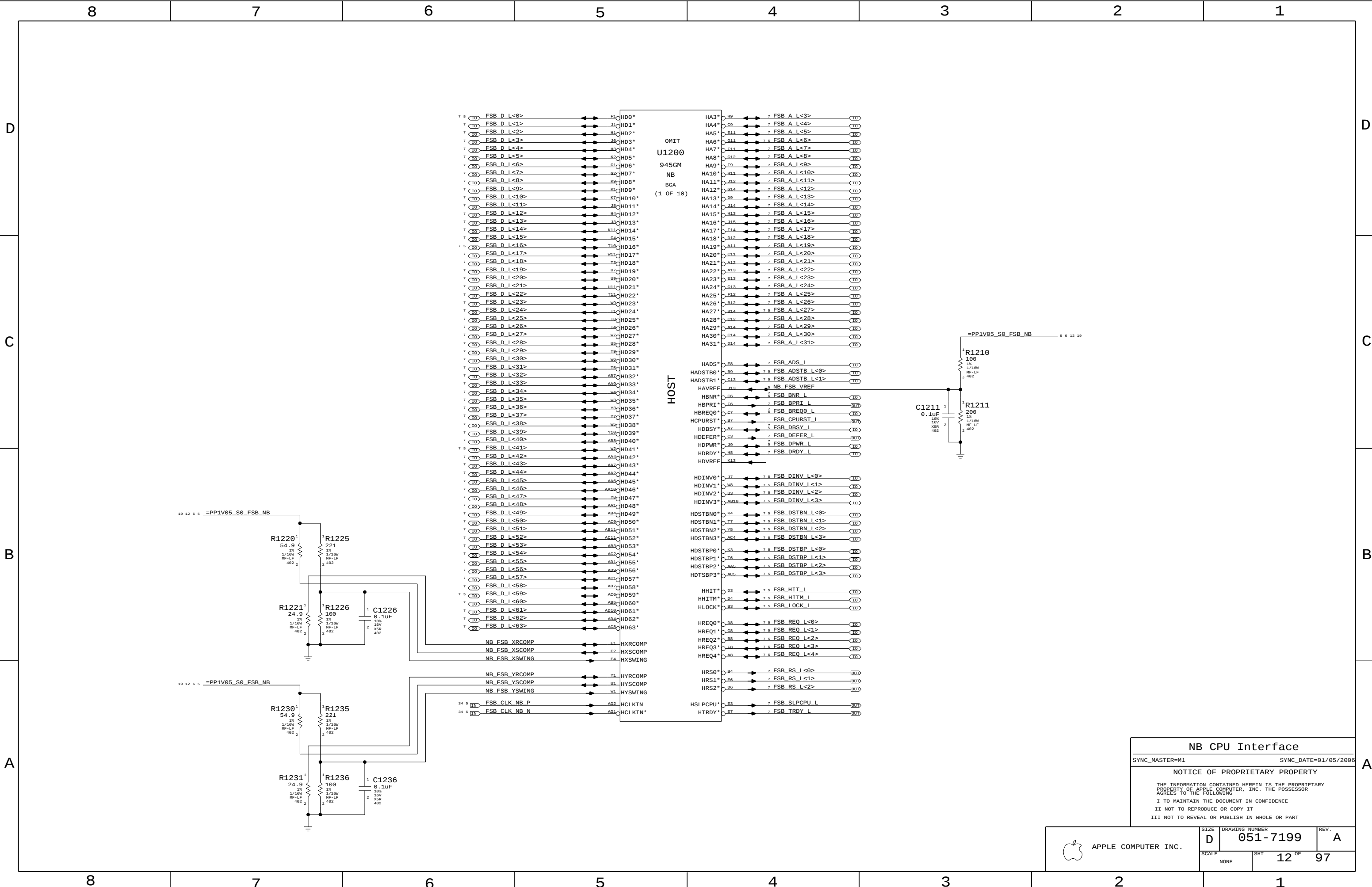
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	D	051-7199	A
SCALE		SHT	11 OF 97
NONE			



NB CPU Interface

SYNC_MASTER=M1

SYNC_DATE=01/05/2006

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SIZE

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DRAWING NUMBER

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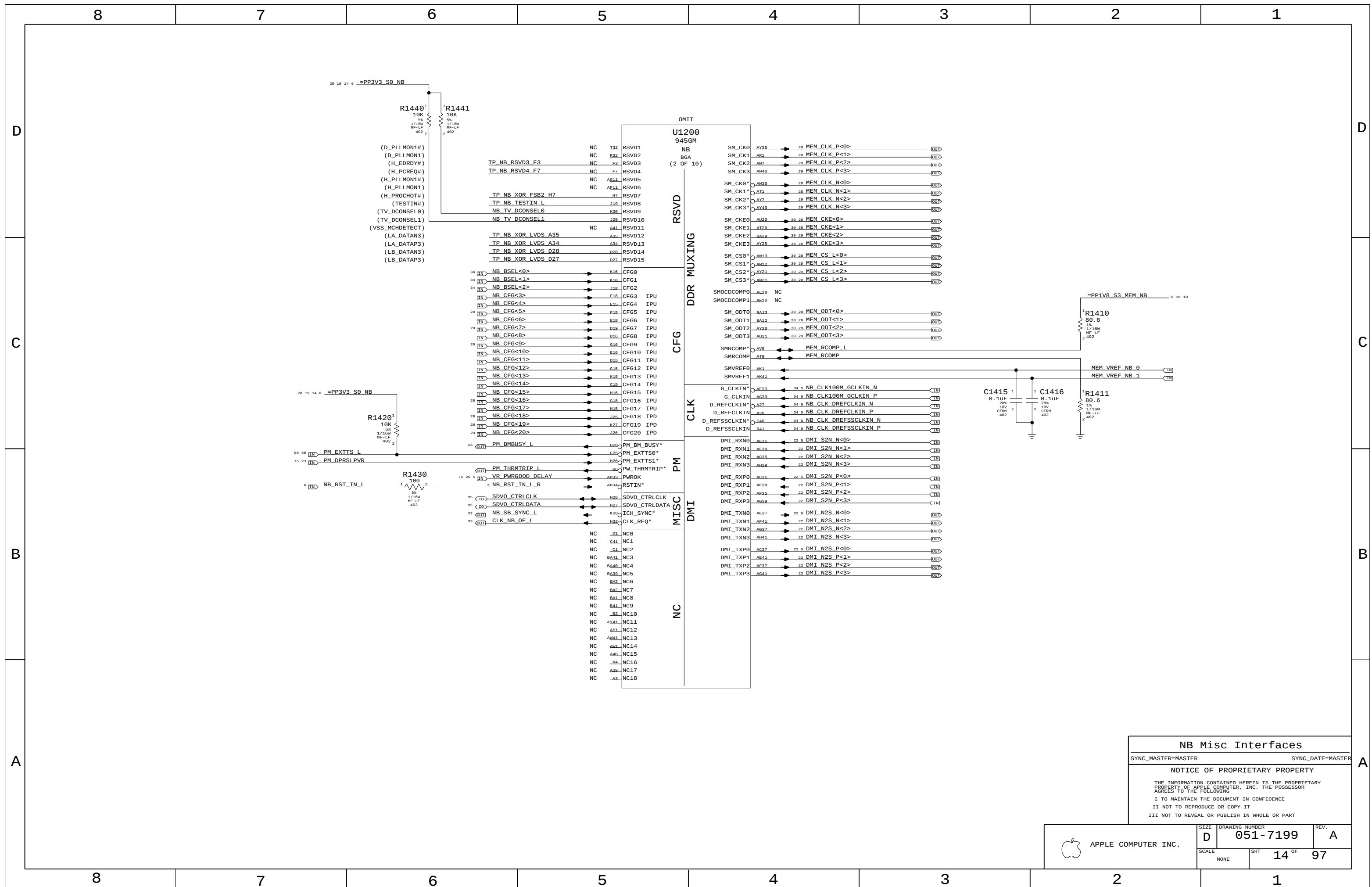
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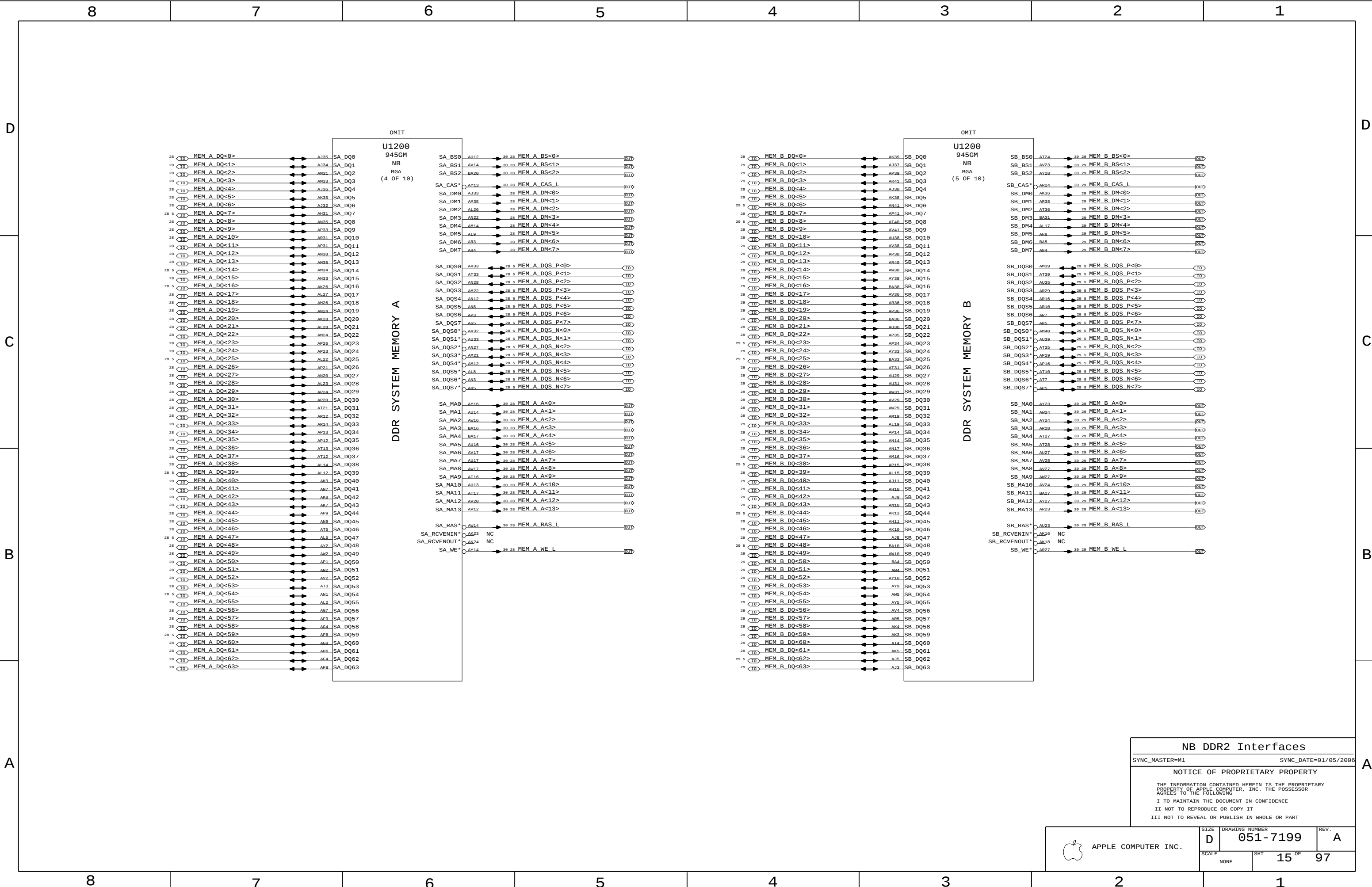
NONE

SHT

12 OF 97







NB DDR2 Interfaces

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

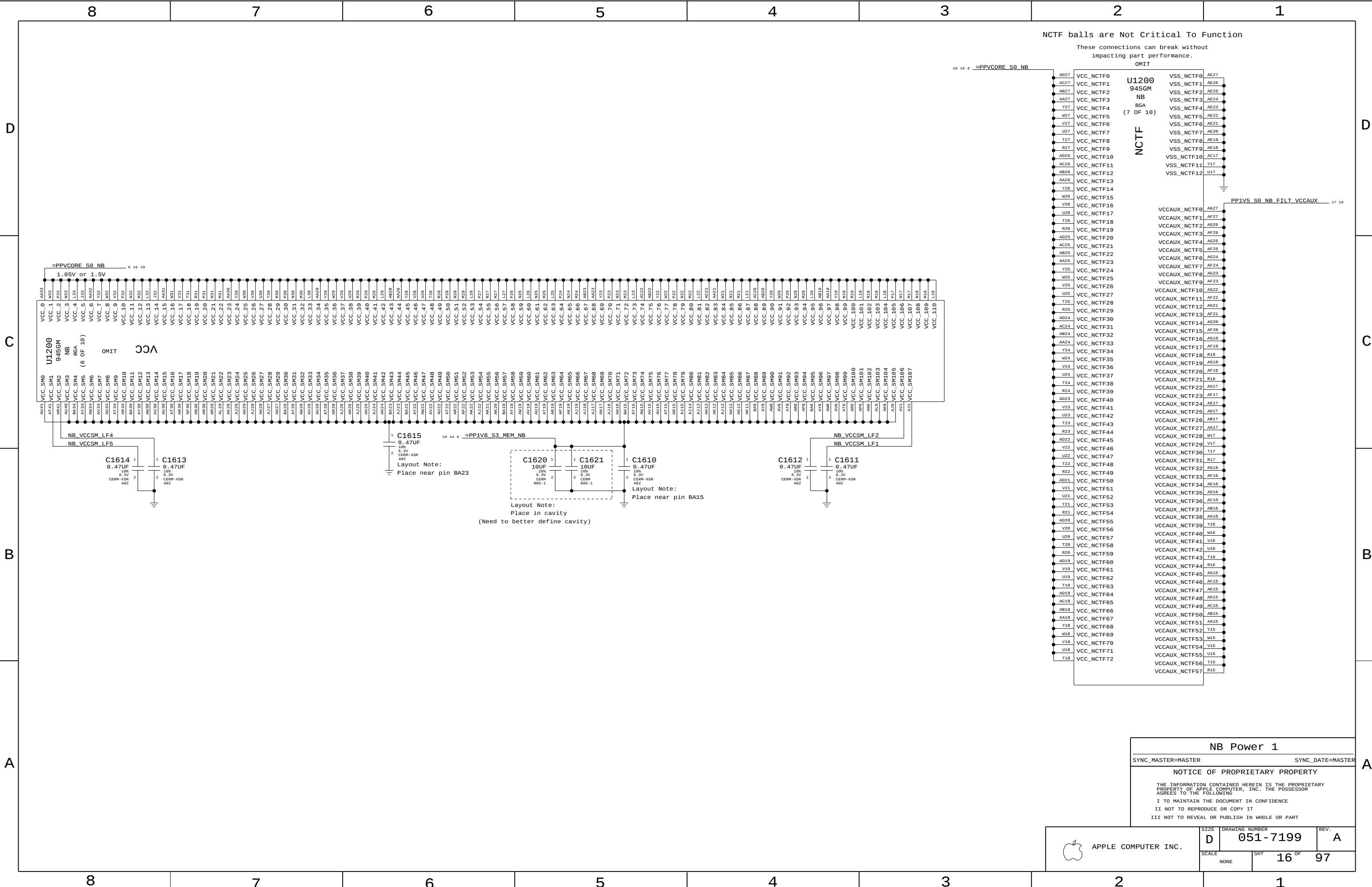
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NB Power 1

SYNC_MASTER=MASTER

SYNC_DATE=MASTER

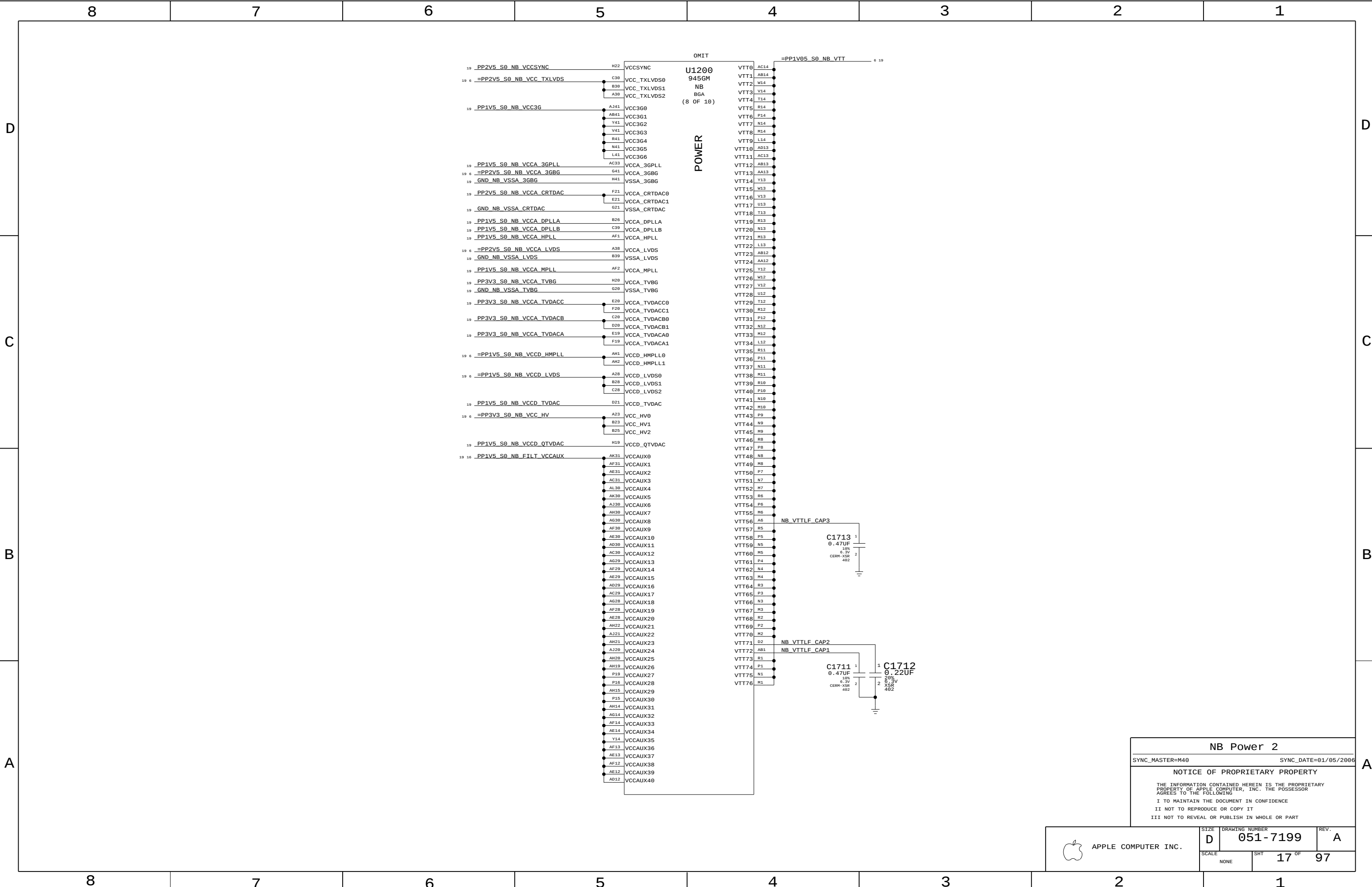
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NB Power 2

SYNC_MASTER=M40

SYNC_DATE=01/05/2006

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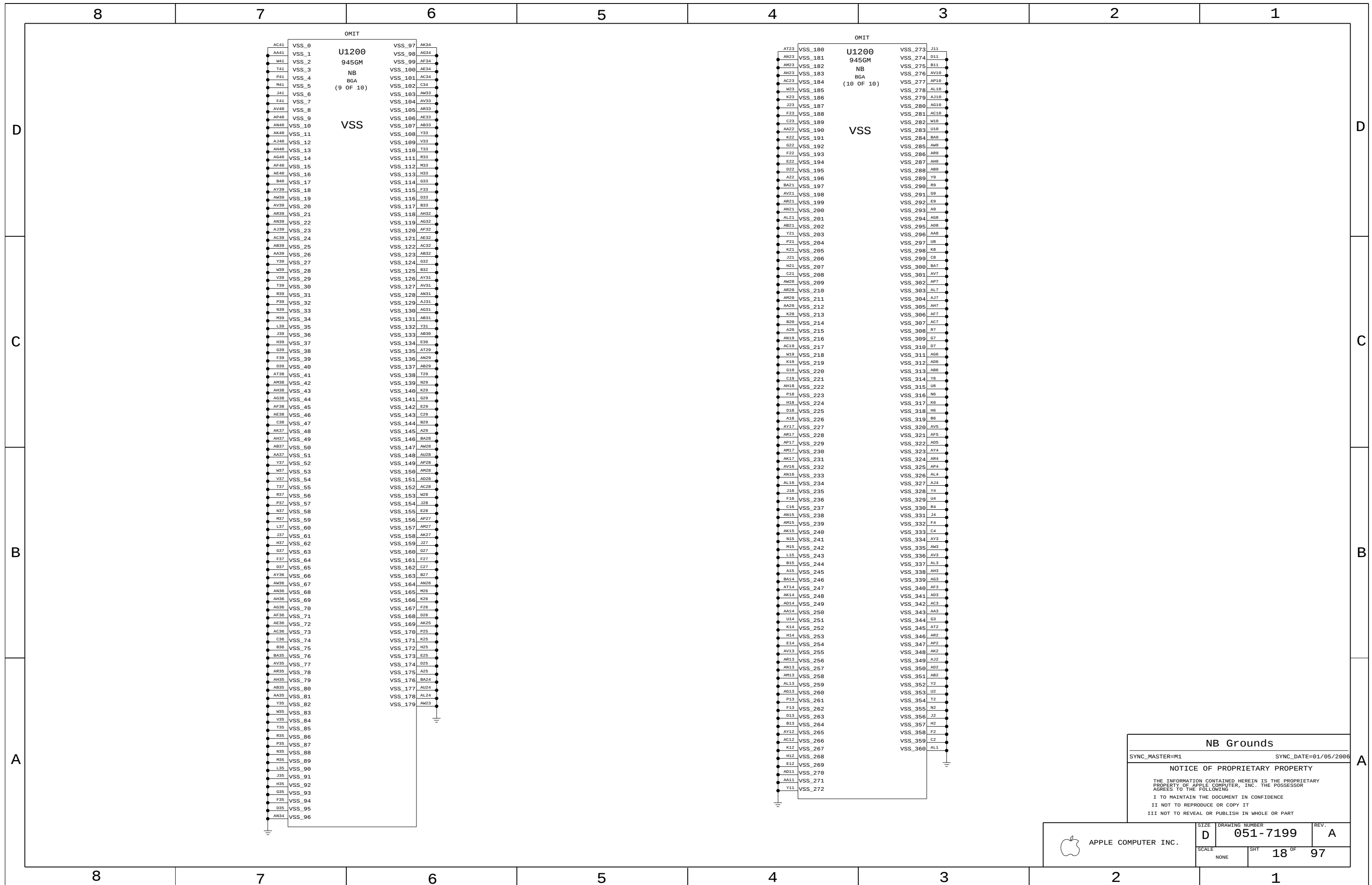
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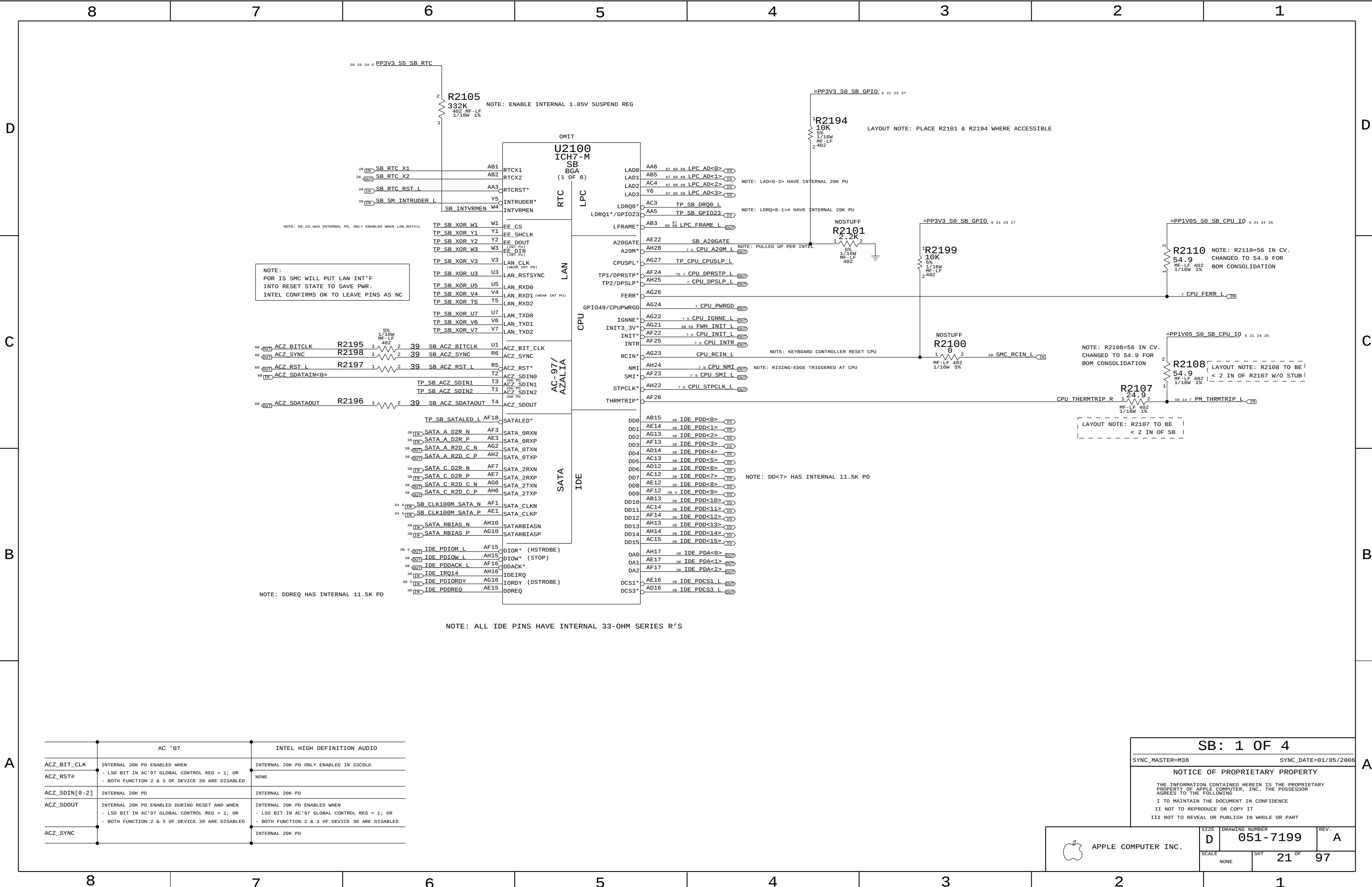
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	D	051-7199	A
SCALE		SHT	17 OF 97
NONE			





NOTE:
POR IS SMC WILL PUT LAN INT'F
INTO RESET STATE TO SAVE PWR.
INTEL CONFIRMS OK TO LEAVE PINS AS NC

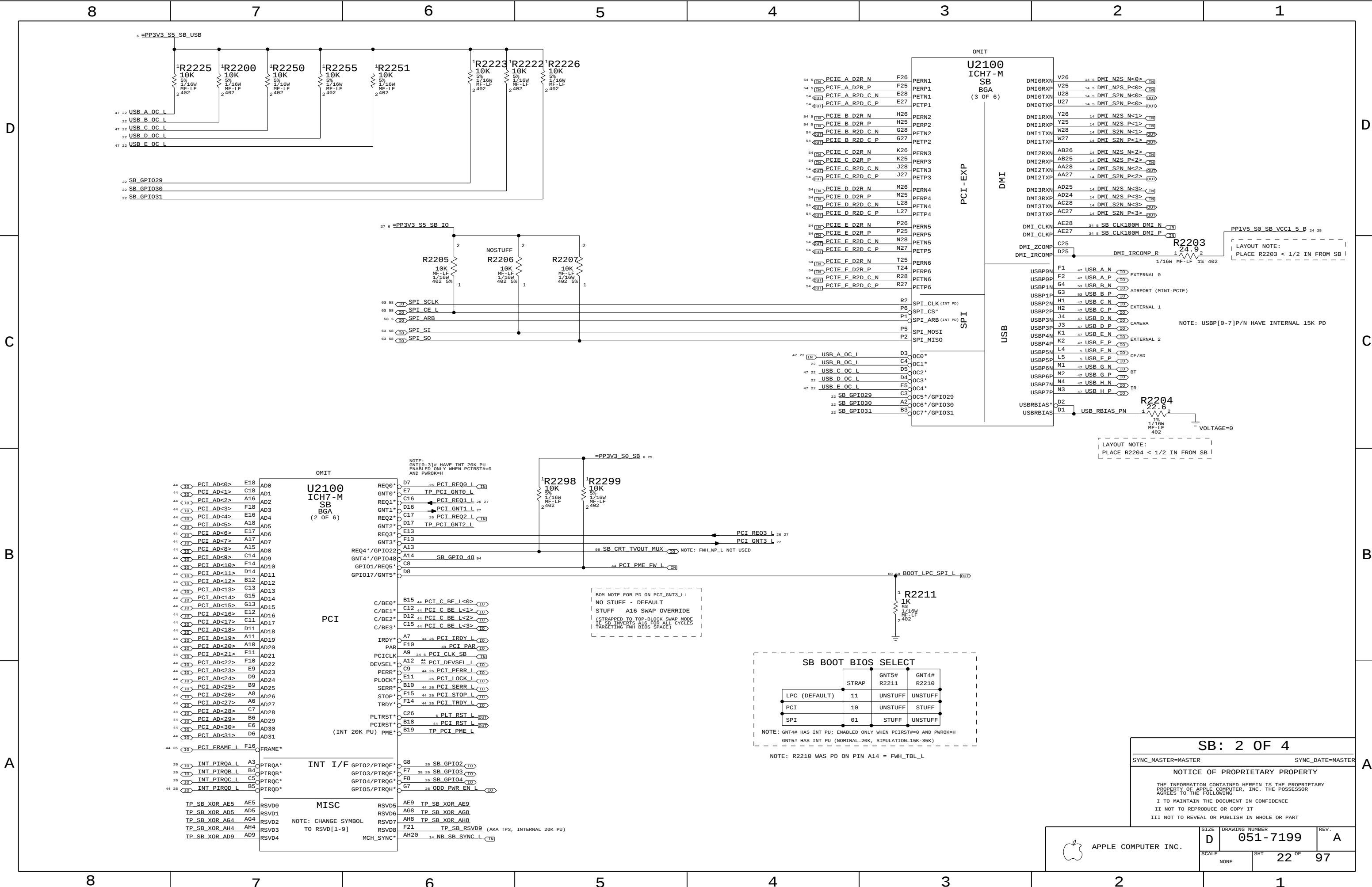
NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '97		INTEL HIGH DEFINITION AUDIO	
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD	NONE
ACZ_RST#			
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD	
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	
ACZ_SYNC		INTERNAL 20K PD	

SB: 1 OF 4		
SYNC_MASTER=M38		SYNC_DATE=01/05/2006
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHT 21 OF 97	



SB BOOT BIOS SELECT			
	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=29K, SIMULATION=15K-35K)
NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

SYNC_MASTER=MASTER

SYNC_DATE=MASTER

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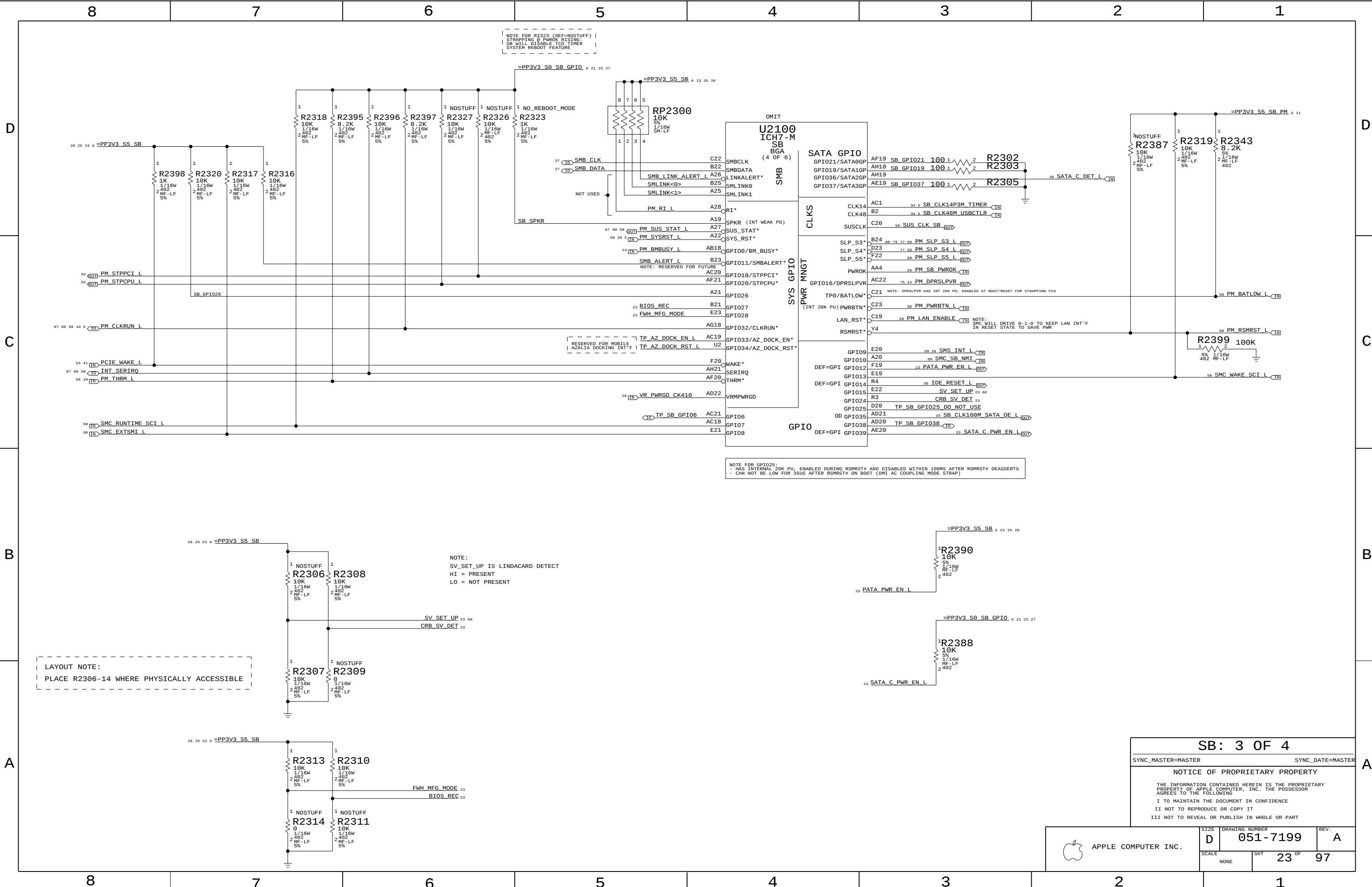
SCALE
NONE

D

DRAWING NUMBER
051-7199

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22 OF 97

REV.
A



NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (OWI AC COUPLING MODE STRAP)

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4

SYNC_MASTER=MASTER

SYNC_DATE=MASTER

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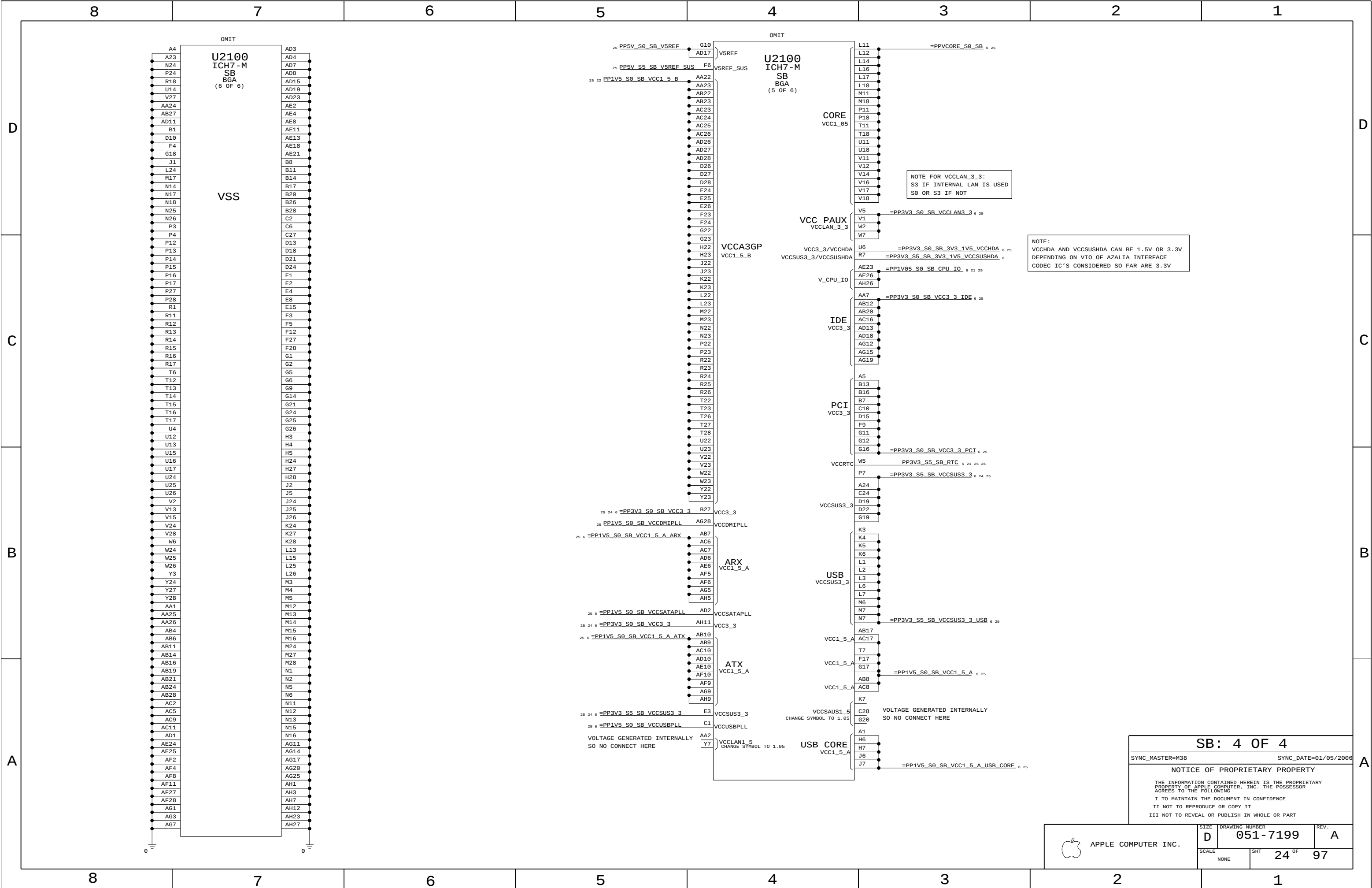
SIZE D

DRAWING NUMBER 051-7199

REV. A

SCALE NONE

SHT 23 OF 97



SB: 4 OF 4

SYNC_MASTER=M38

SYNC_DATE=01/05/2006

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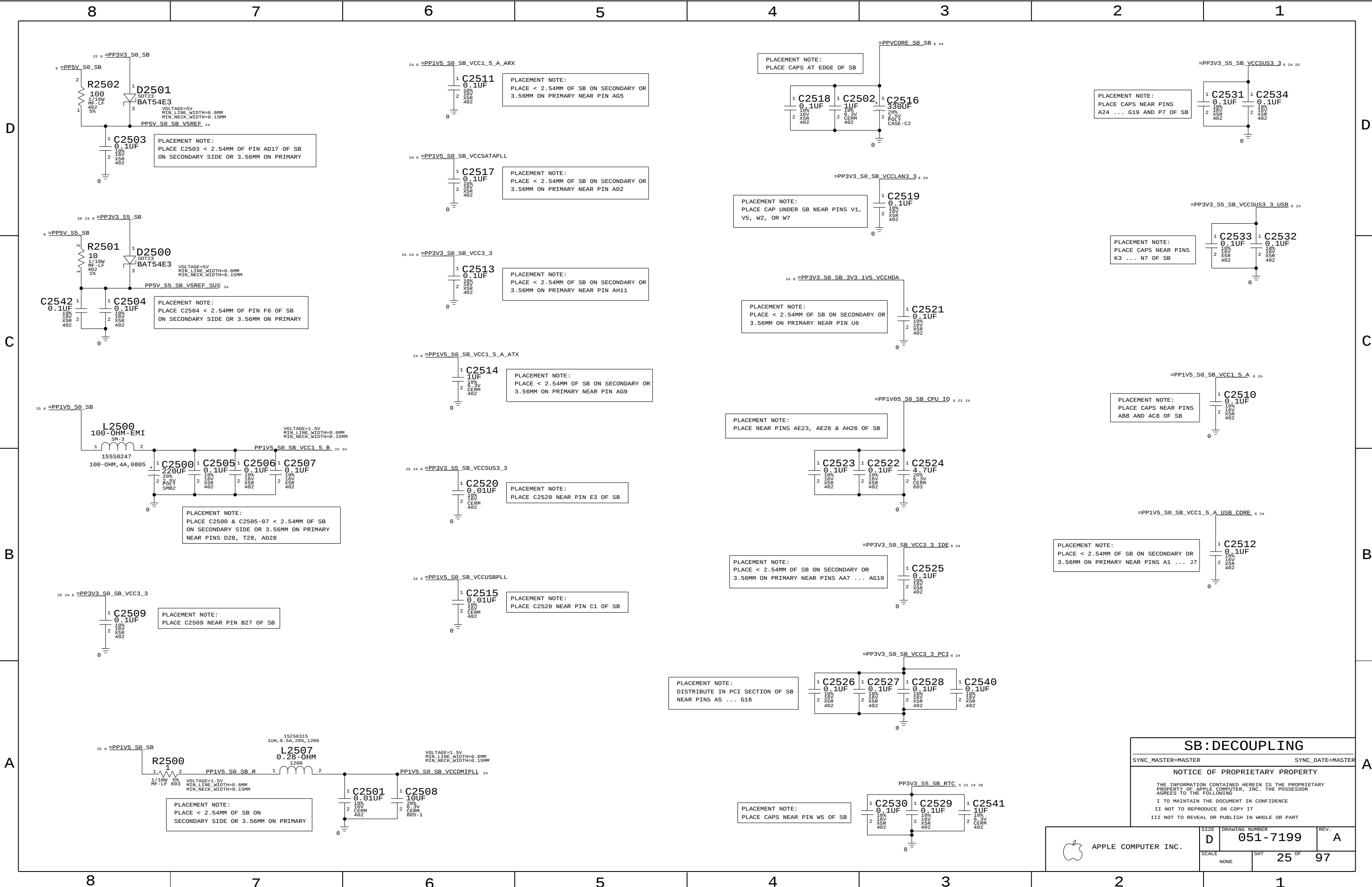
SCALE
NONE

SIZE
D

DRAWING NUMBER
051-7199

SHT
24 OF 97

REV.
A



SB: DECOUPLING

SYNC_MASTER=MASTER

SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

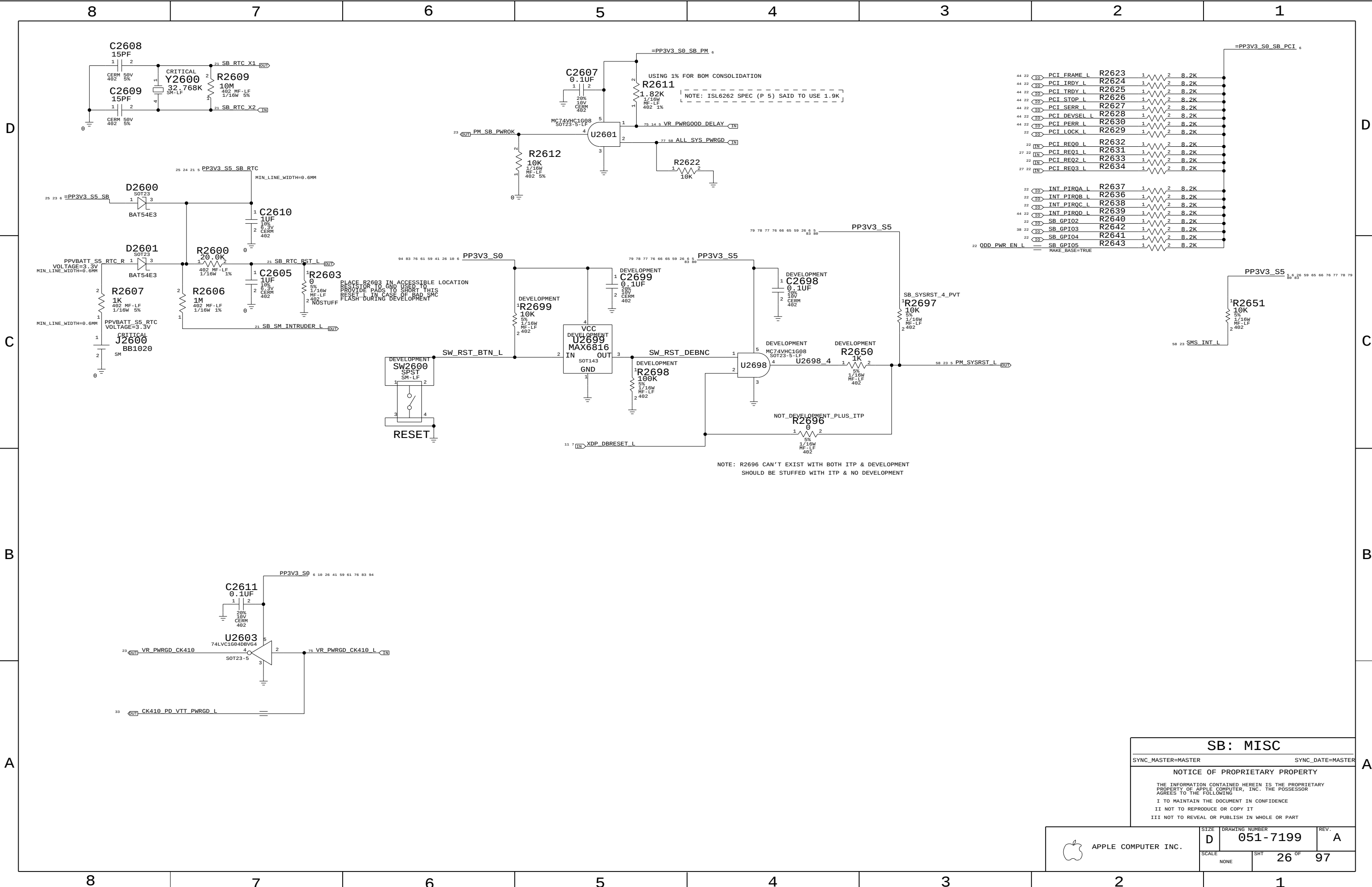
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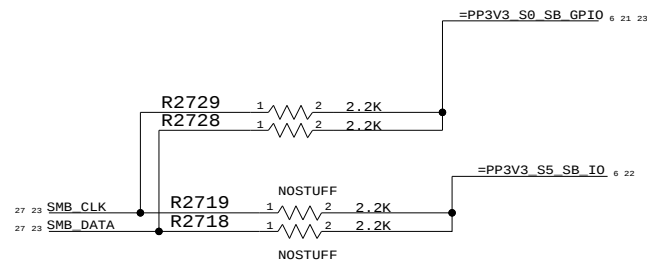
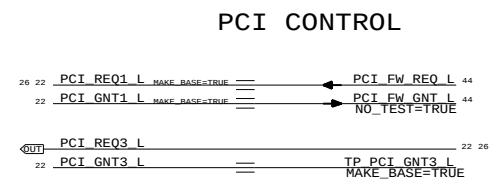
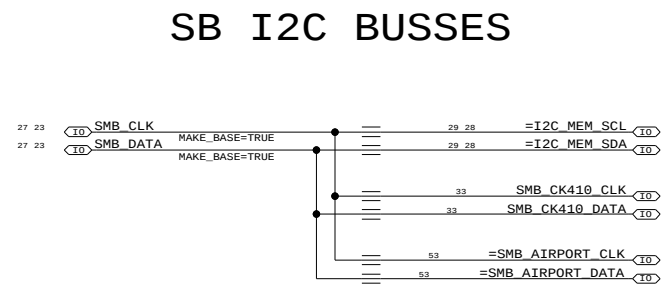
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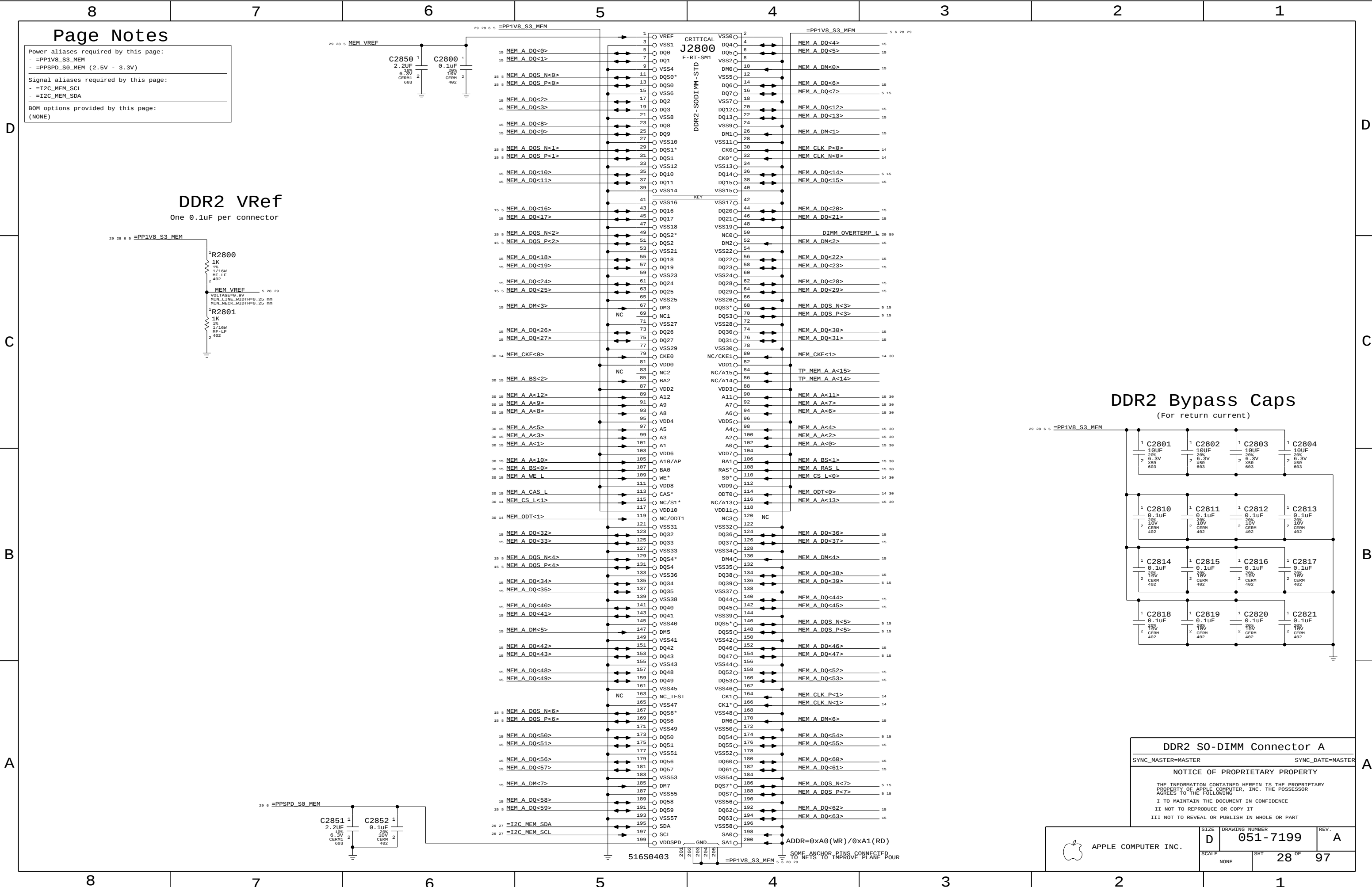
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE		SHT	25 OF 97
NONE			





SB: SMB HUB AND ALIAS	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
	SCALE	SHT	
	NONE	27 OF	97



Page Notes

Power aliases required by this page:

- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:

(NONE)

DDR2 VRef
One 0.1uF per connector

DDR2 Bypass Caps
(For return current)

DDR2 S0-DIMM Connector A

SYNC_MASTER=MASTER SYNC_DATE=MASTER

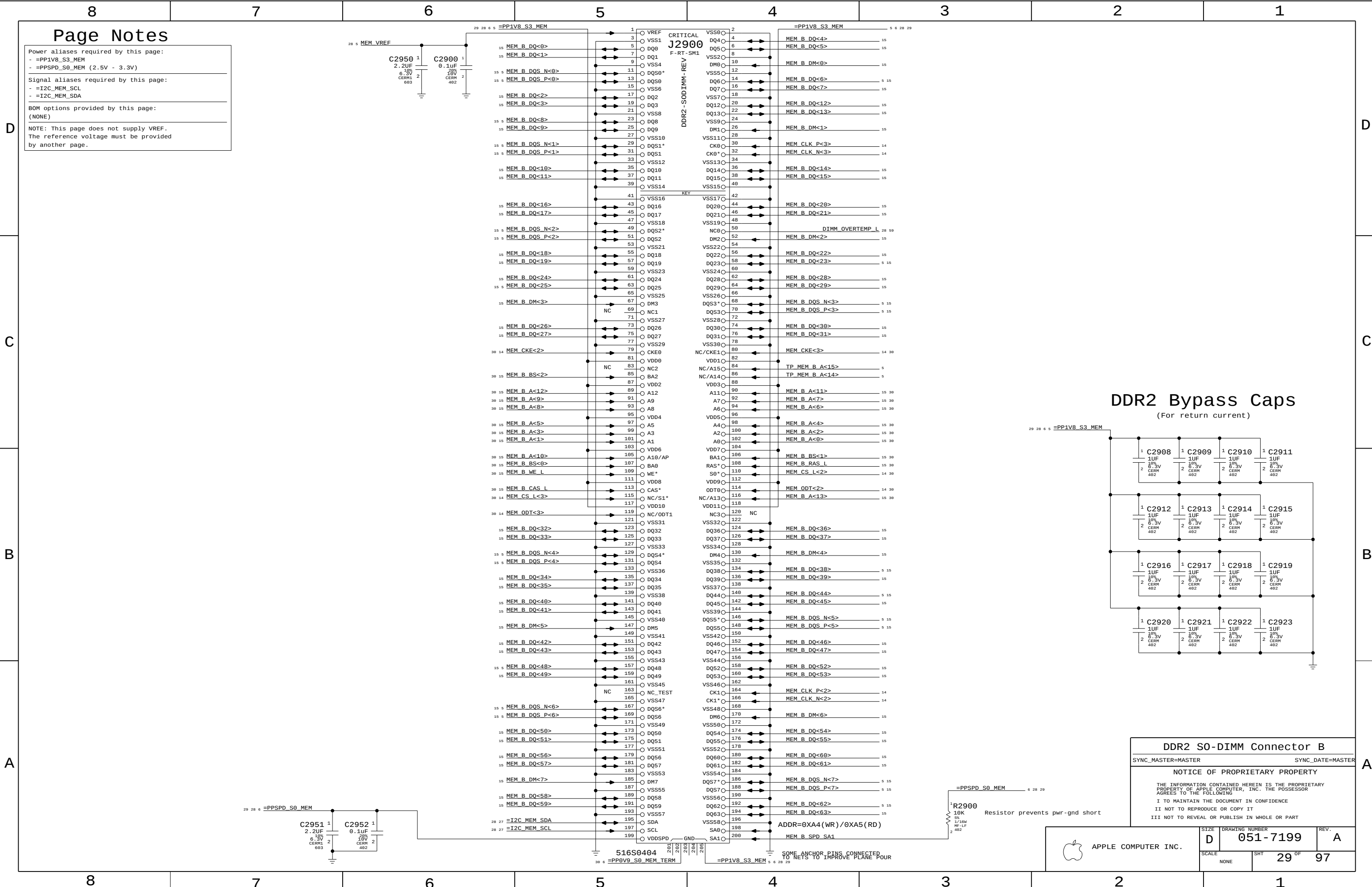
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Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

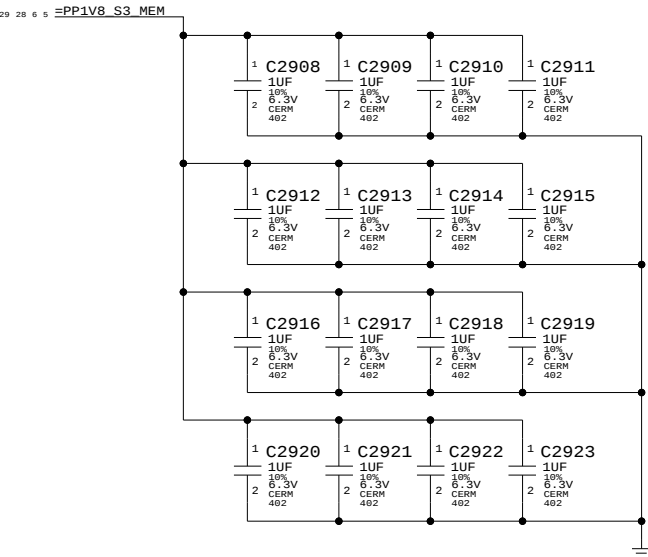
Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

DDR2 Bypass Caps

(For return current)



DDR2 S0-DIMM Connector B

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

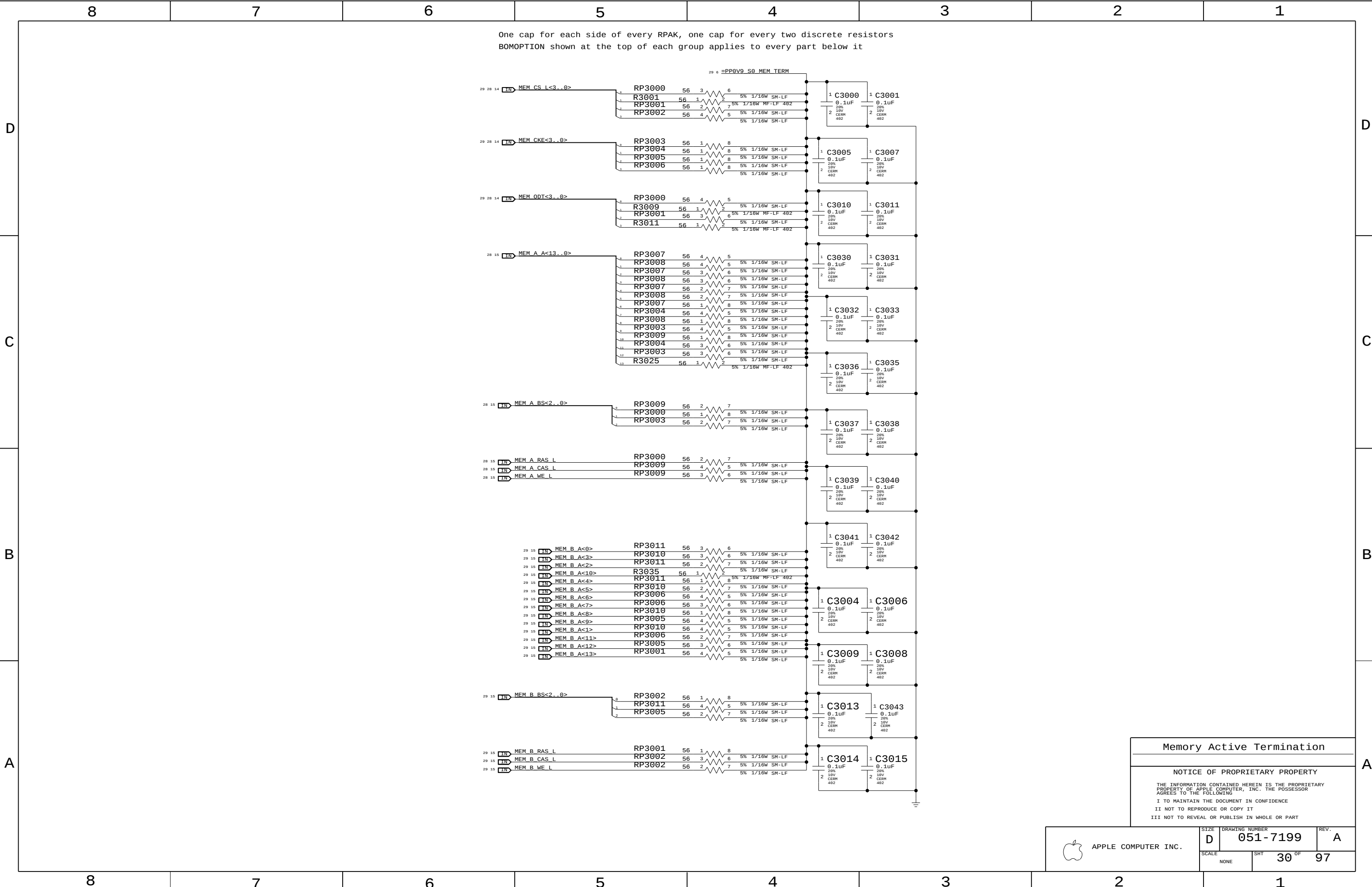
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHT 29 OF 97	



Memory Active Termination

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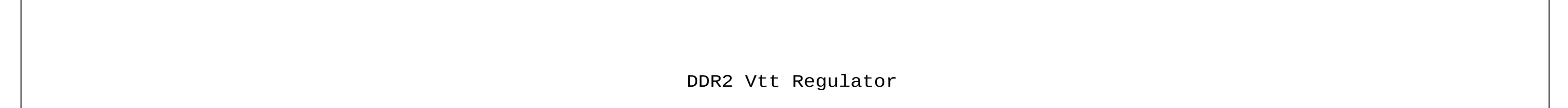
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE		SHT	30 OF 97
NONE			

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

(NONE)

(NONE)

[illegible]

If power inputs are not S0, MEMVTT_EN can be used to

SYNC_DATE=MASTER

disable MEMVlt in sleep.
 2Can 5V be so if 1V8 is 53? - - - - -

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II NOT TO REPRODUCE OR COPY IT

SIZE	DOAL-TAC NUMBER
------	-----------------



DRAWING NUMBER

051-7199

A

21⁰

NON

31

8	7	6	5	4	3	2	1
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6

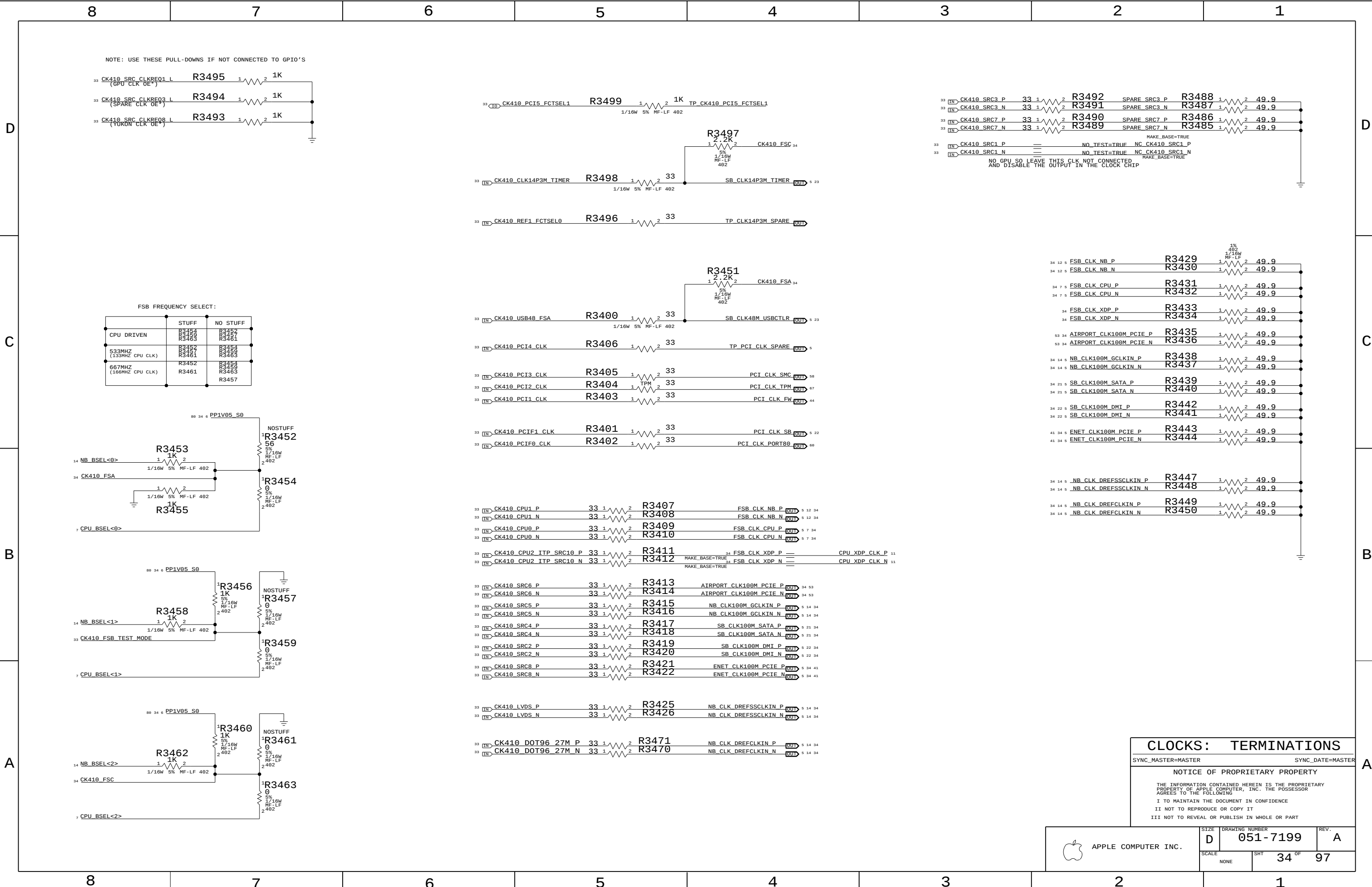
5

4

3

2

1



CLOCKS: TERMINATIONS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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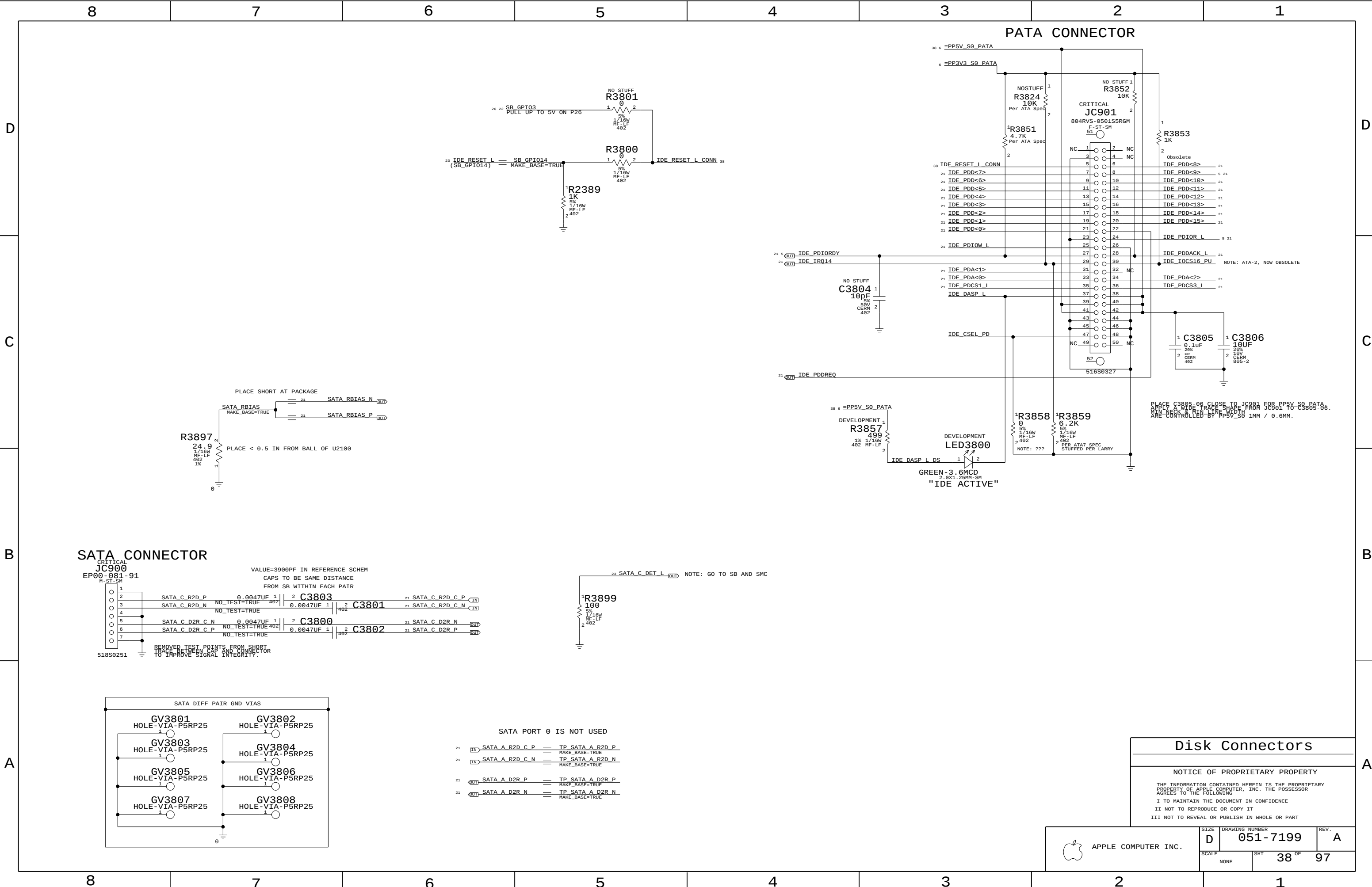
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



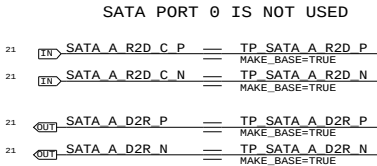
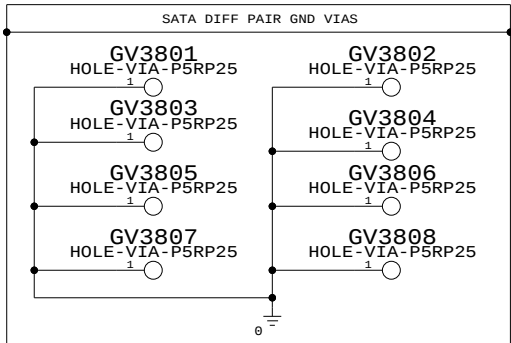
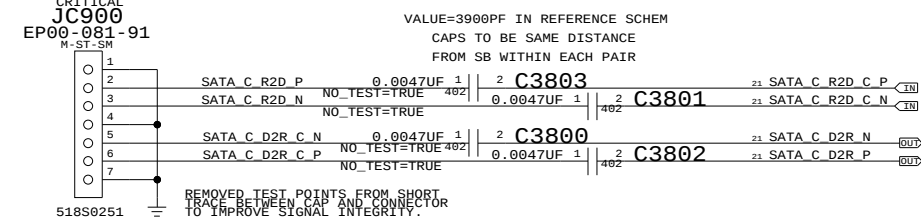
APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7199 REV. A

SCALE NONE SHT 34 OF 97



SATA CONNECTOR

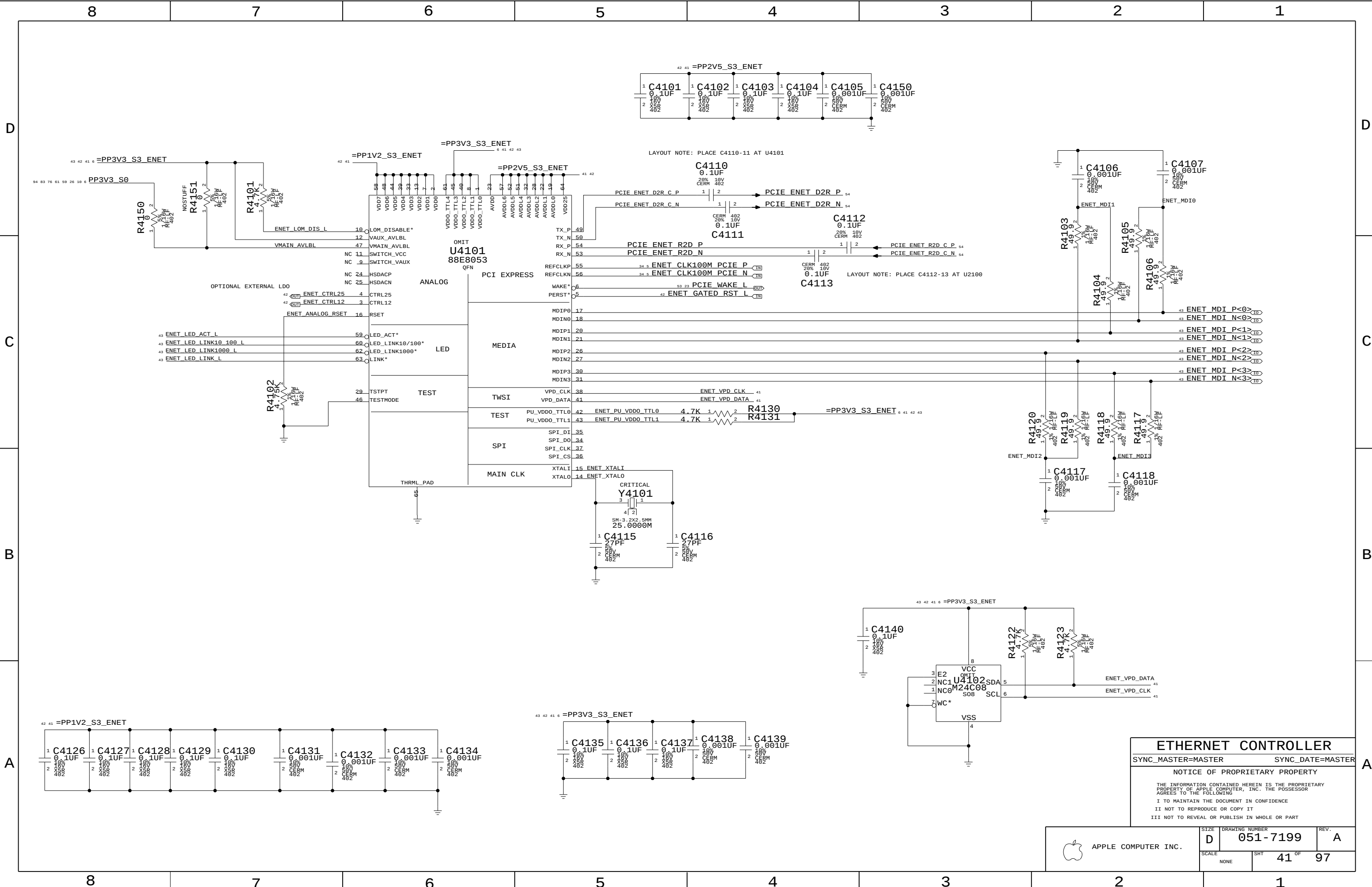


Disk Connectors

NOTICE OF PROPRIETARY PROPERTY

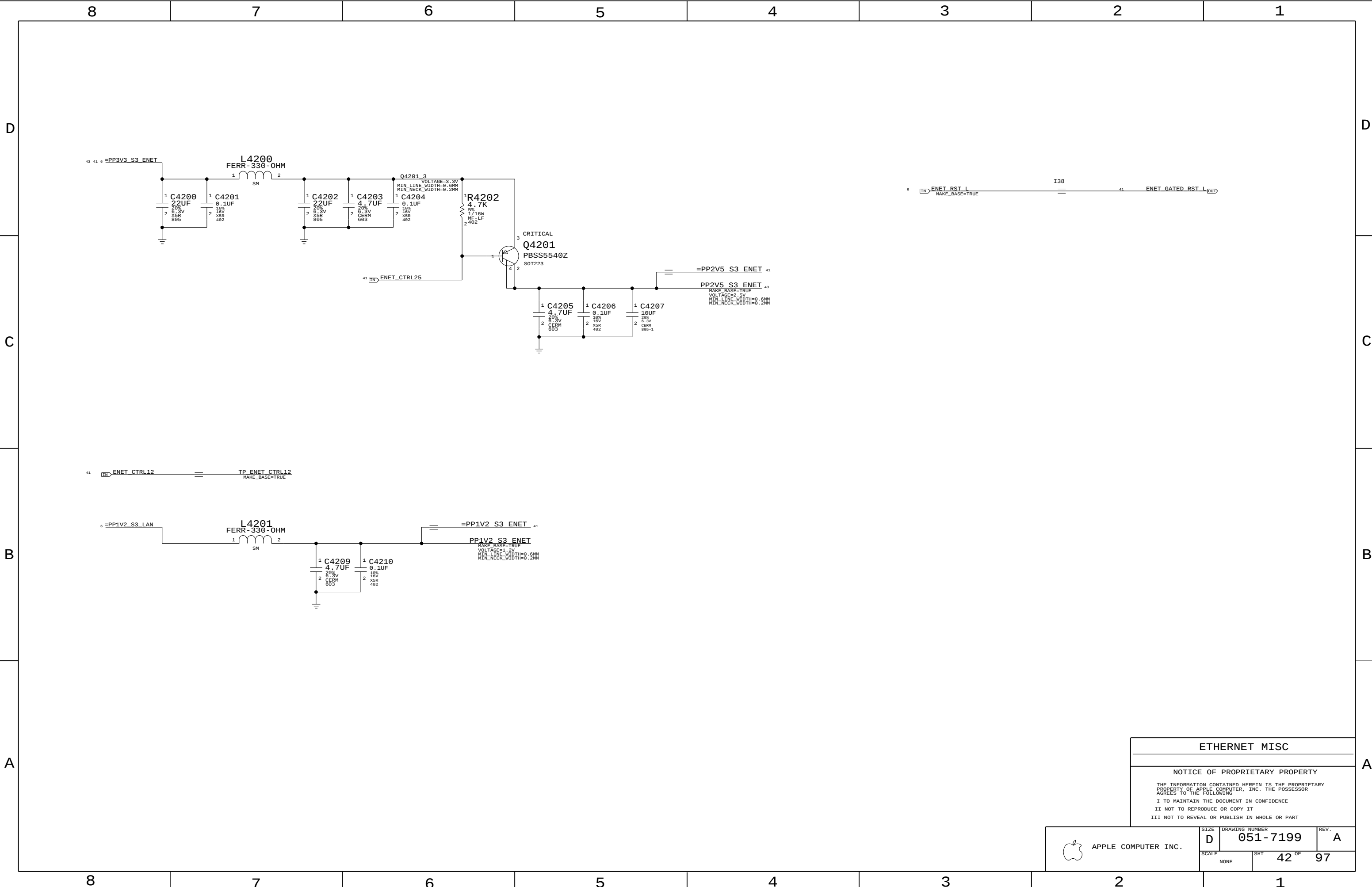
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHT 38 OF 97	



ETHERNET CONTROLLER
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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ETHERNET MISC

NOTICE OF PROPRIETARY PROPERTY

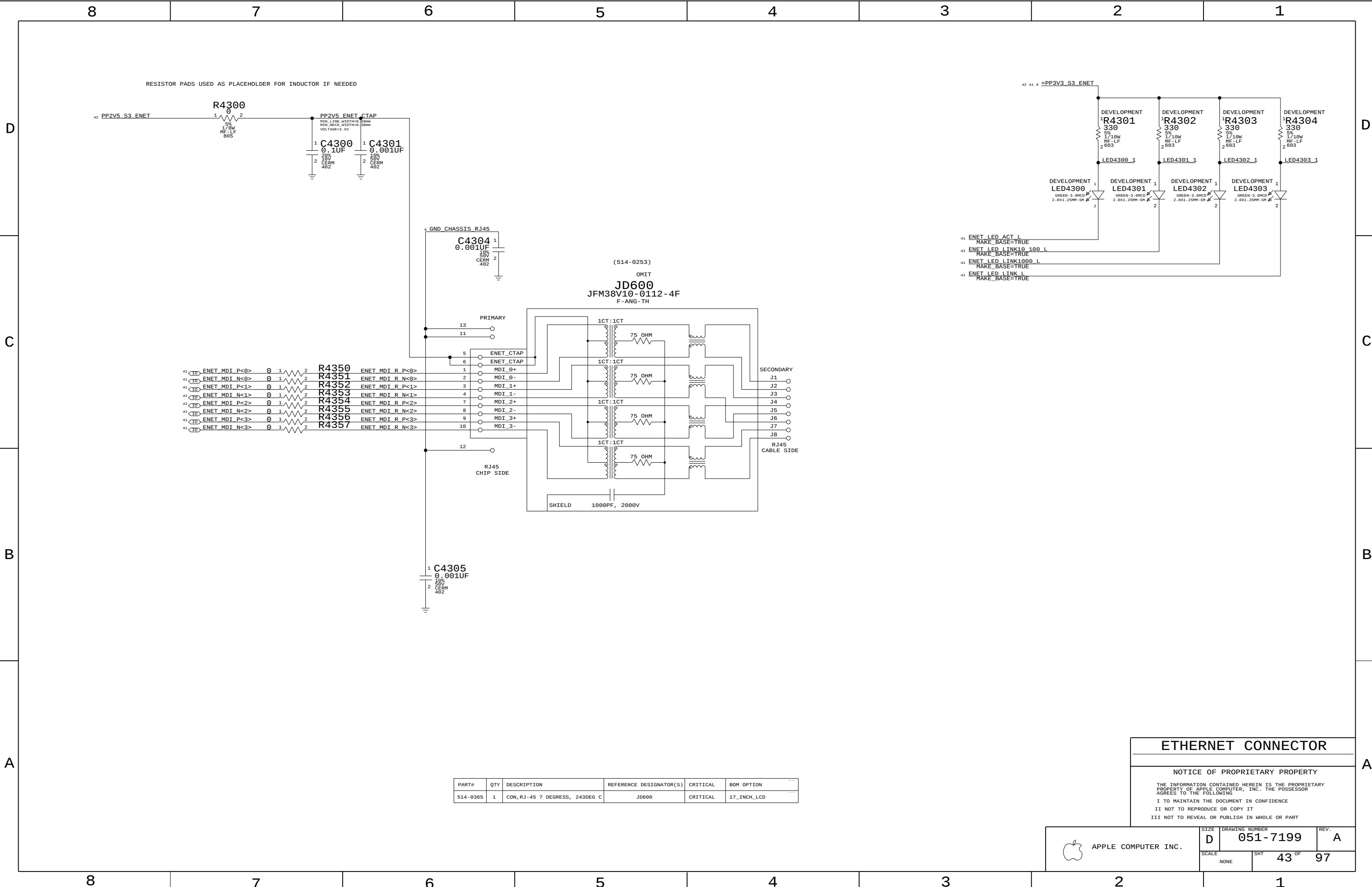
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE		SHT	42 OF 97
NONE			



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0365	1	CON,RJ-45 7 DEGRESS, 243DEG C	JD600	CRITICAL	17_INCH_LCD

ETHERNET CONNECTOR

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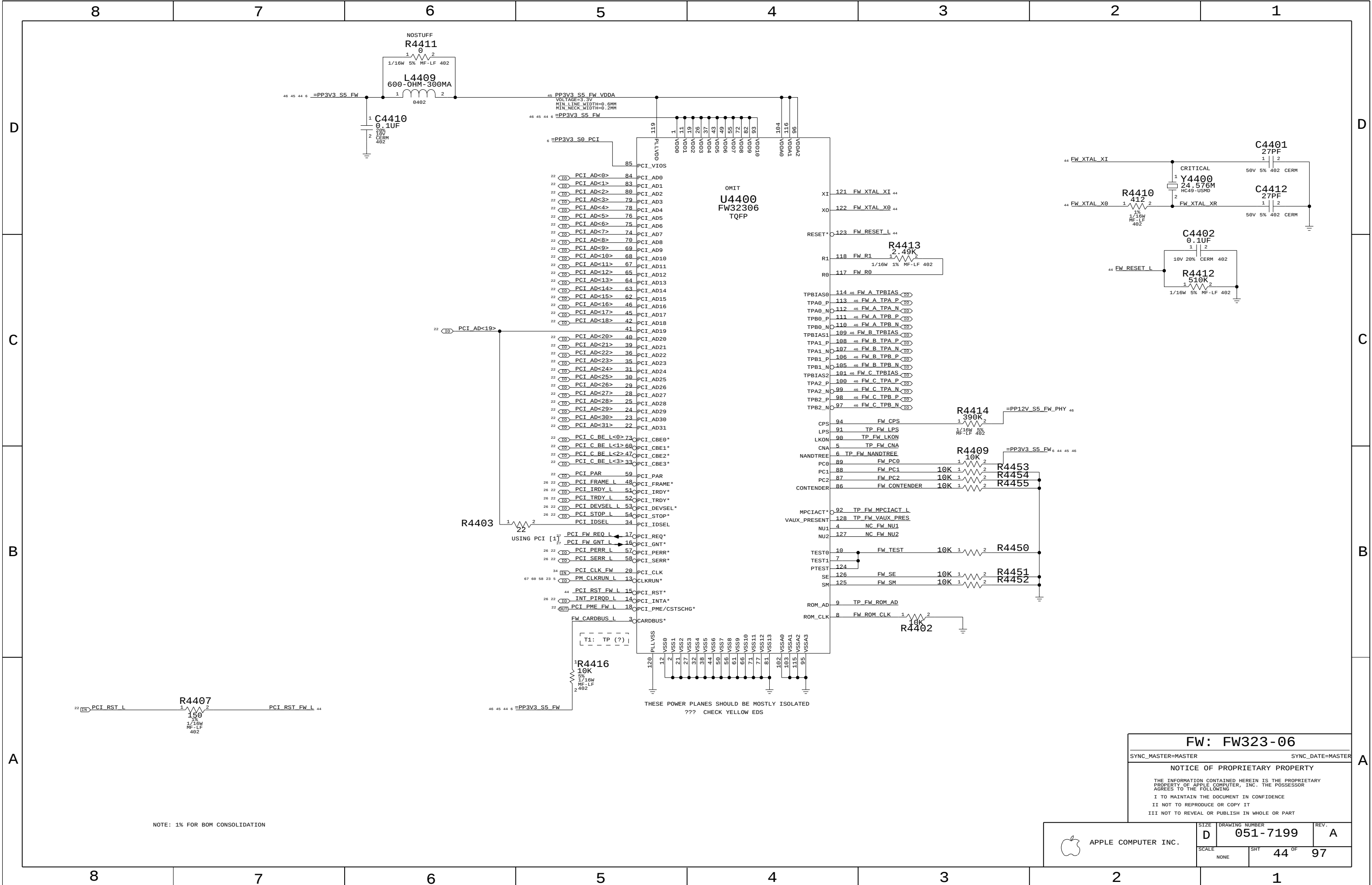
SIZE D

DRAWING NUMBER 051-7199

REV. A

SCALE NONE

SHT 43 OF 97



FW: FW323-06

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

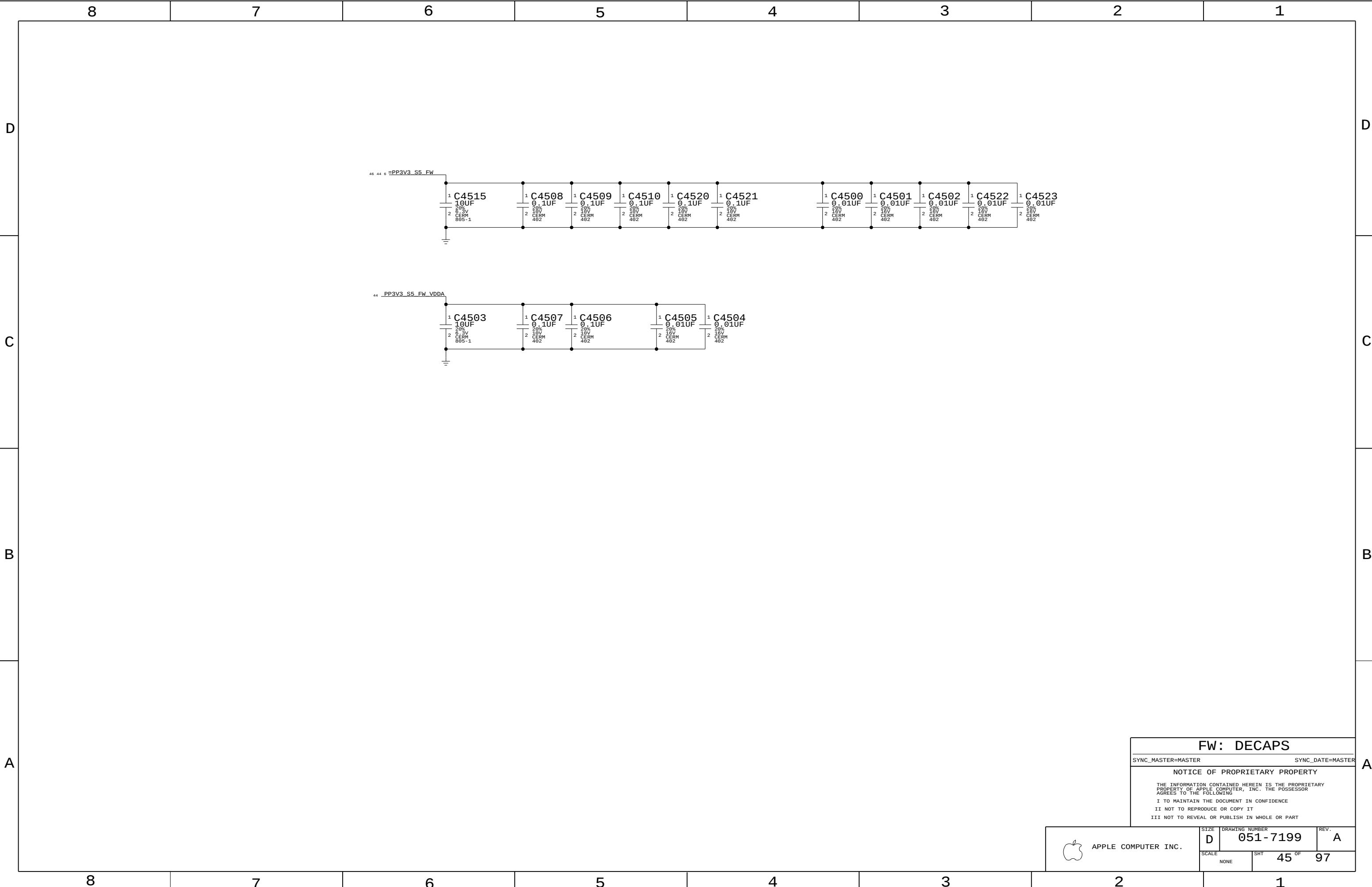
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE		SHT	44 OF 97
NONE			



FW: DECAPS

SYNC_MASTER=MASTER

SYNC_DATE=MASTER

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7199

REV.

A

SCALE

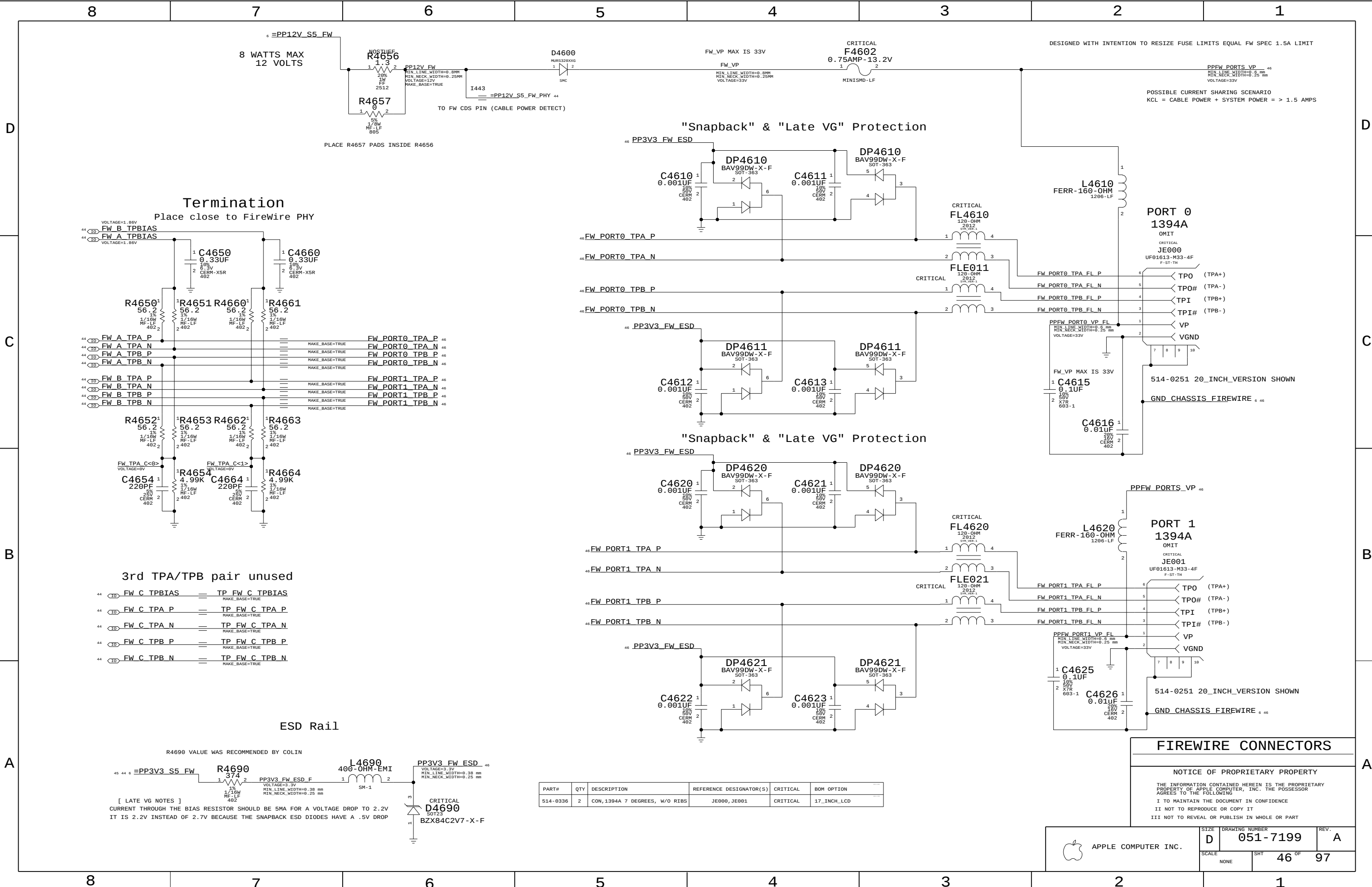
NONE

SHT

45

OF

97



Termination
Place close to FireWire PHY

"Snapback" & "Late VG" Protection

3rd TPA/TPB pair unused

"Snapback" & "Late VG" Protection

ESD Rail

FIREWIRE CONNECTORS

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON, 1394A 7 DEGREES, W/O RIBS	JE000, JE001	CRITICAL	17_INCH_LCD

 APPLE COMPUTER INC.

SIZE
D

DRAWING NUMBER
051-7199

REV.
A

SCALE
NONE

SHT
46 OF 97

External USB Ports

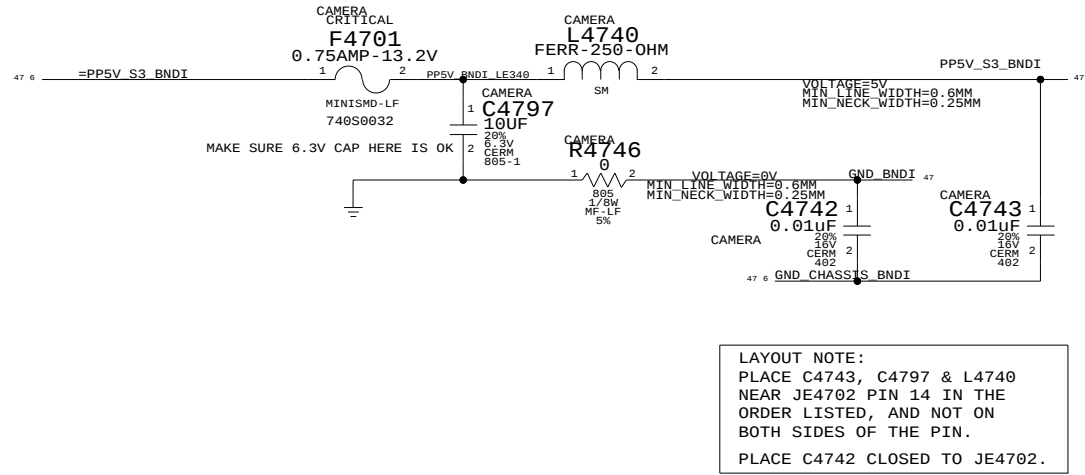
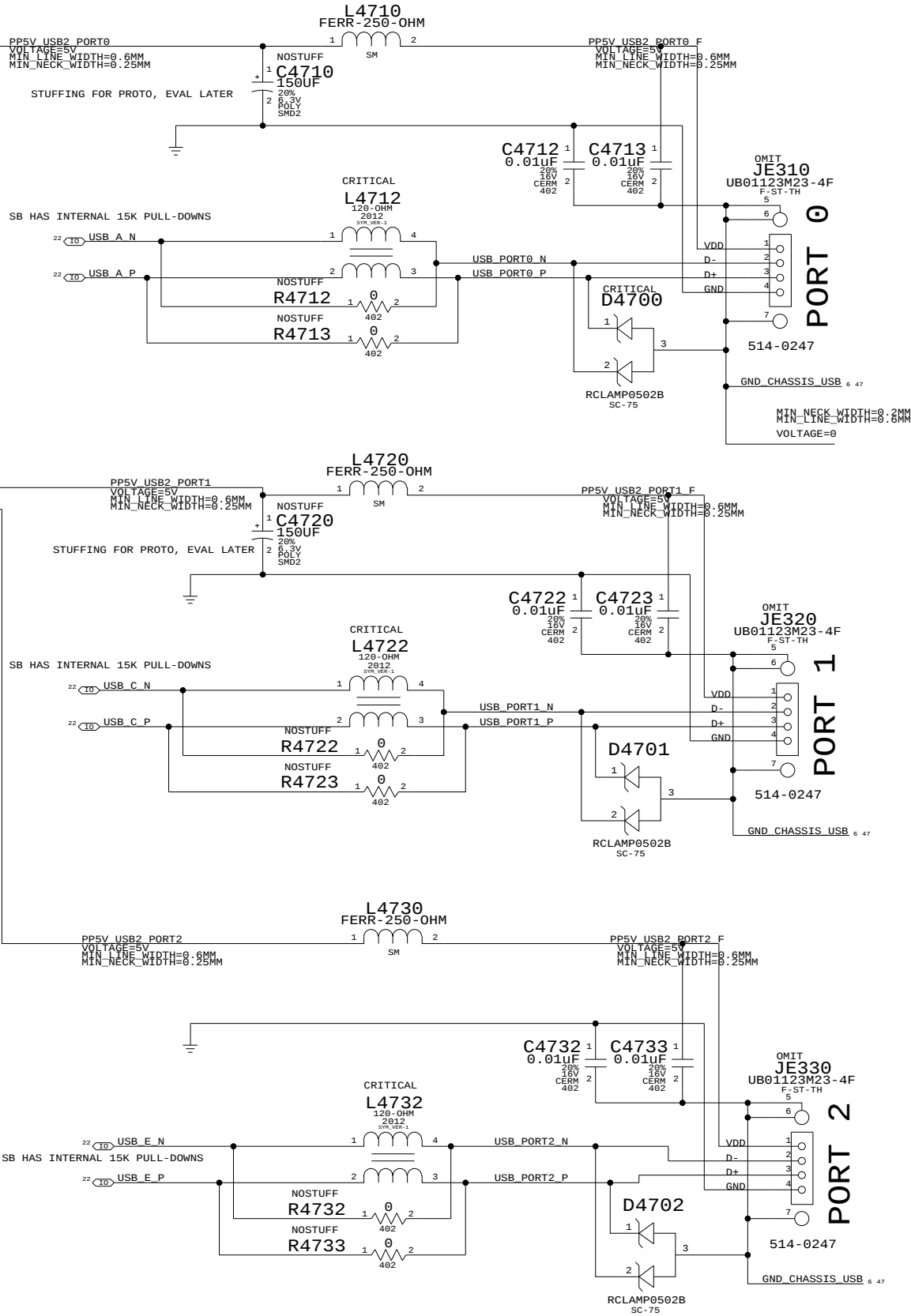
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C

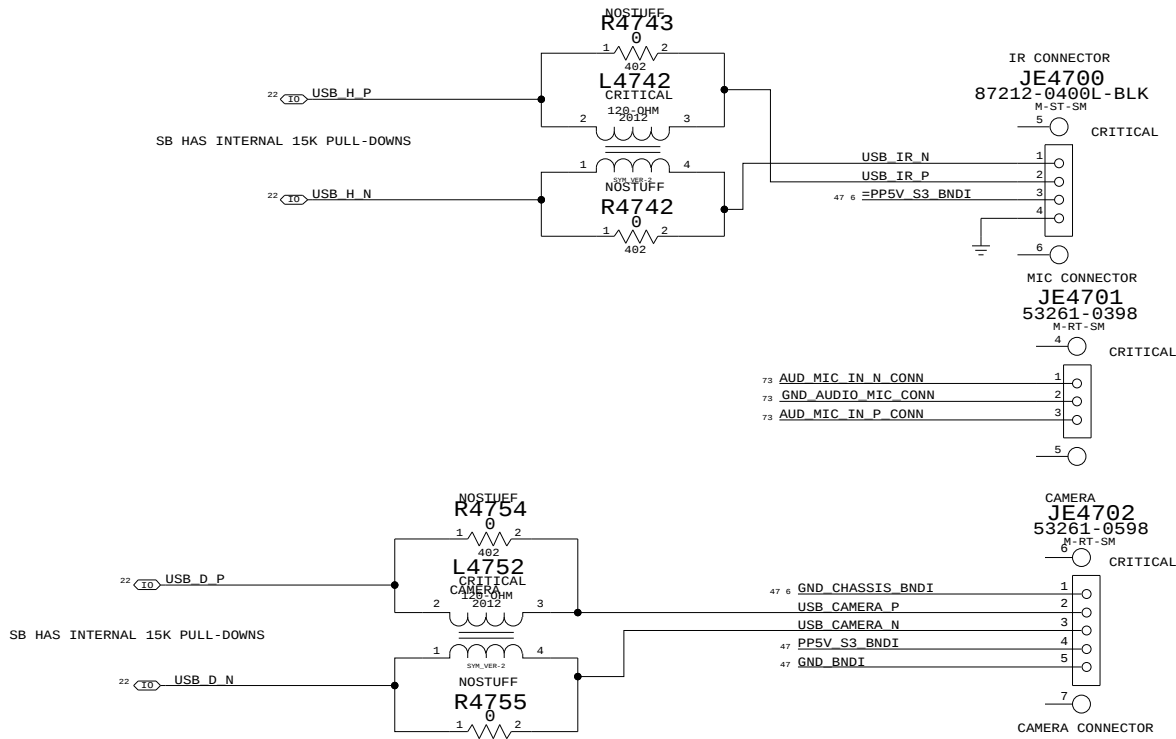
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A

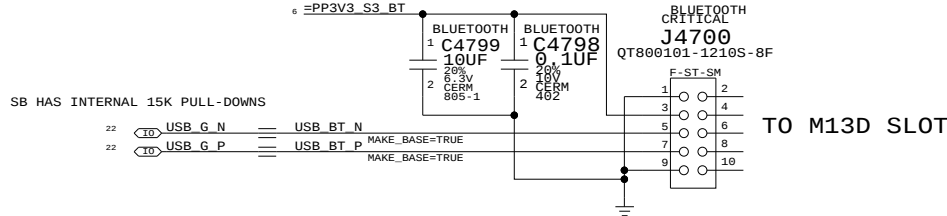
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE, 4P, UB1123-M50-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD



LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR JE4702 PIN 14 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.
PLACE C4742 CLOSED TO JE4702.



BLUETOOTH



NOTE: STANDOFFS FOR J4700
SDF4700
STD0FF-40D4.5H-1.35-TH
SDF4701
STD0FF-40D4.5H-1.35-TH

USB Device Interfaces

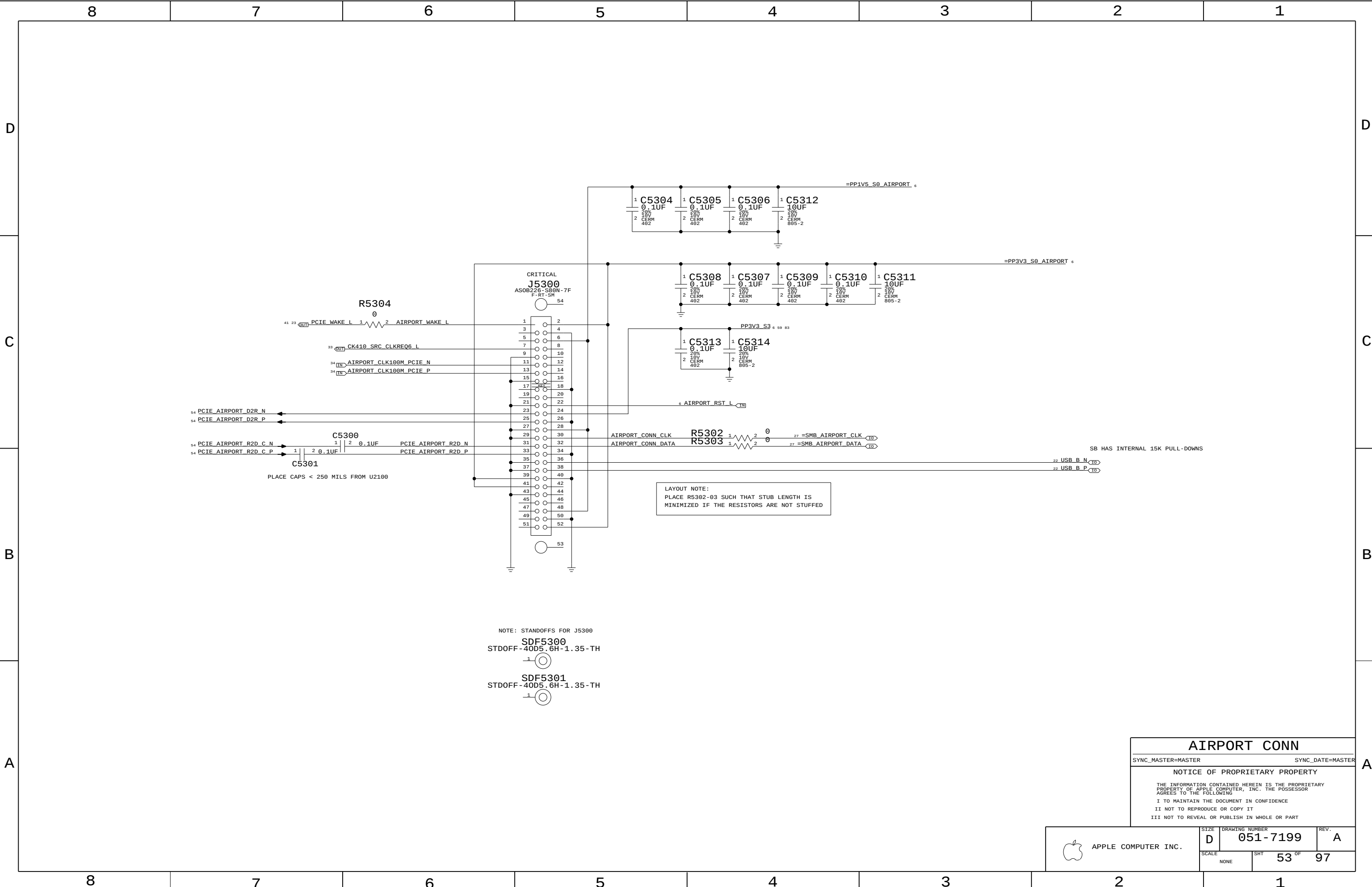
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SIZE	DRAWING NUMBER	REV.
D	051-7199	A
SCALE	SHT	OF
NONE	47	97



LAYOUT NOTE:
PLACE R5302-03 SUCH THAT STUB LENGTH IS
MINIMIZED IF THE RESISTORS ARE NOT STUFFED

NOTE: STANDOFFS FOR J5300
SDF5300
STDOFF-40D5.6H-1.35-TH
SDF5301
STDOFF-40D5.6H-1.35-TH

AIRPORT CONN

SYNC_MASTER=MASTER

SYNC_DATE=MASTER

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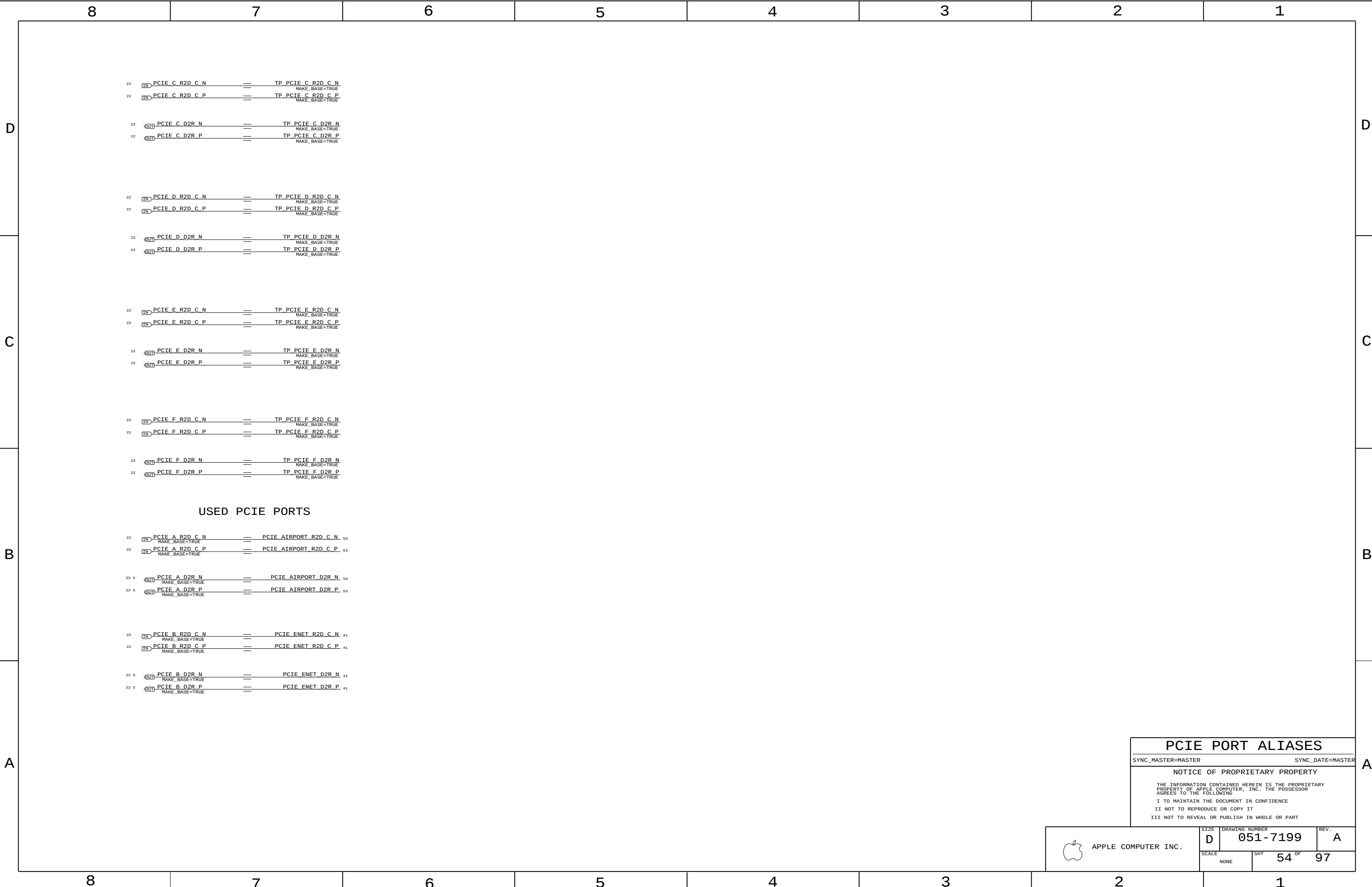
SIZE D

DRAWING NUMBER 051-7199

REV. A

SCALE NONE

SHT 53 OF 97



APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7199

REV.

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SCALE

NONE

SHT

54

OF

97

PCIE PORT ALIASES

SYNC_MASTER=MASTER

SYNC_DATE=MASTER

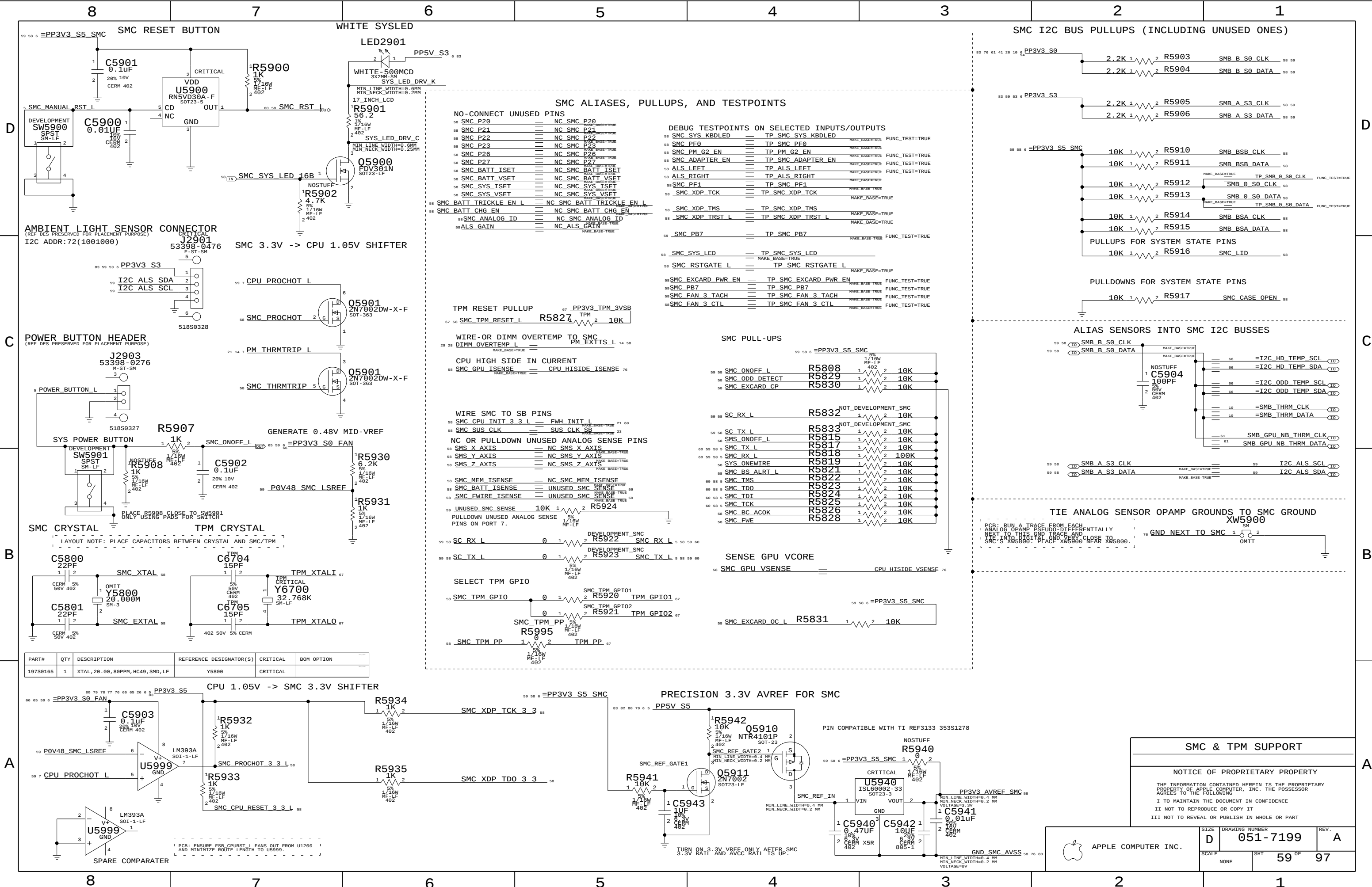
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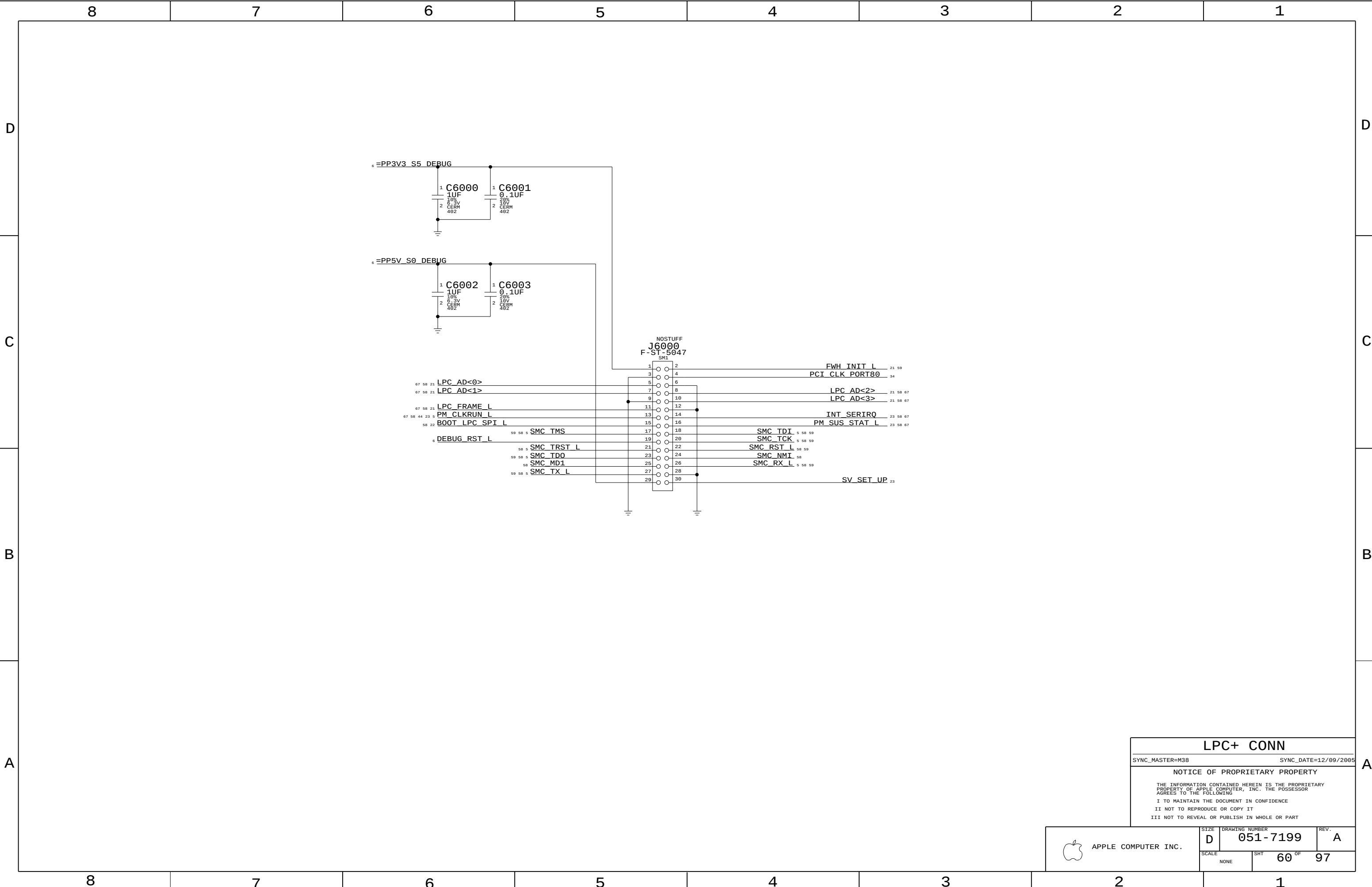
A

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LPC+ CONN

SYNC_MASTER=M38

SYNC_DATE=12/09/2005

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7199

REV.

A

SCALE

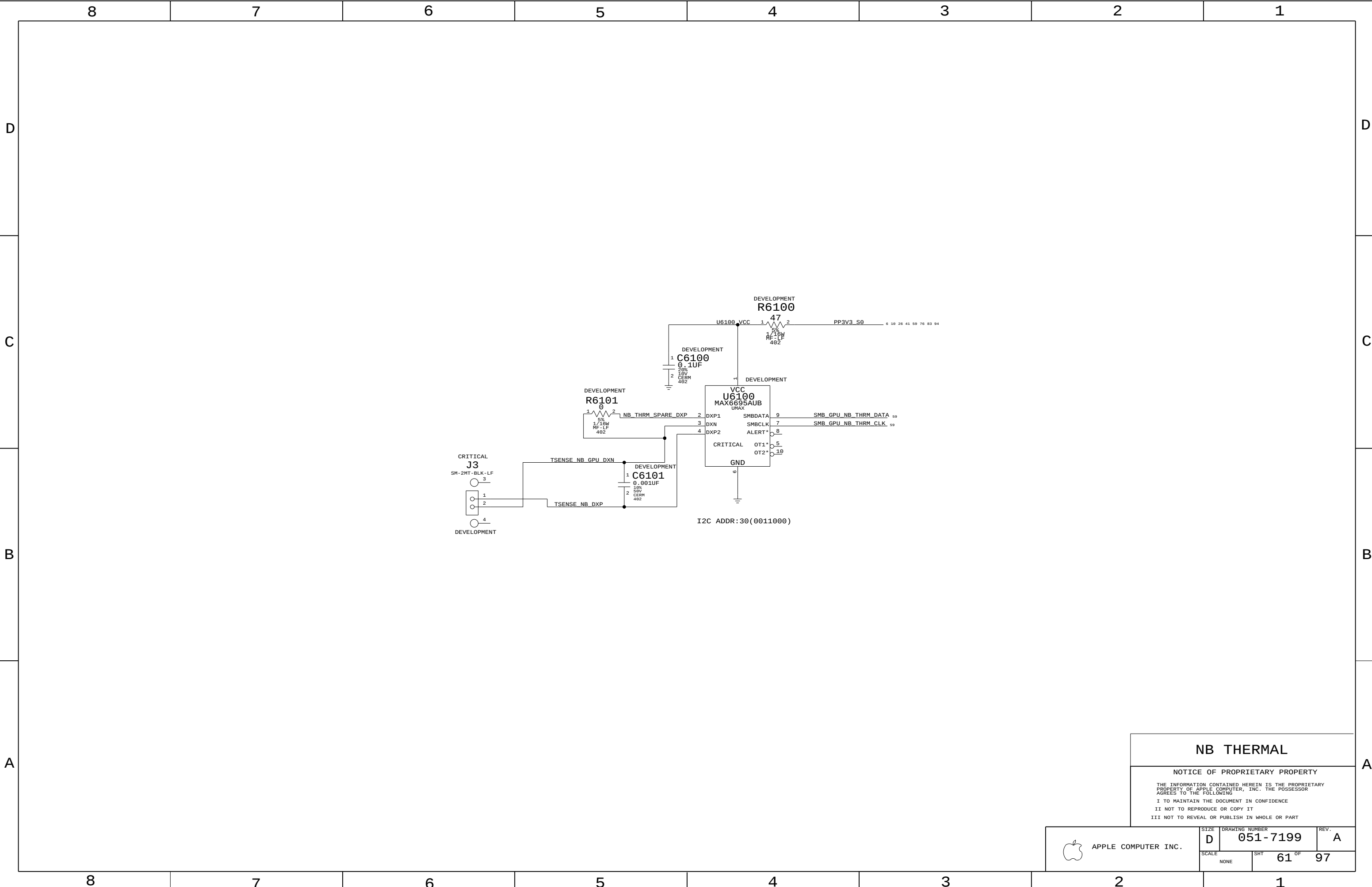
NONE

SHT

60

OF

97

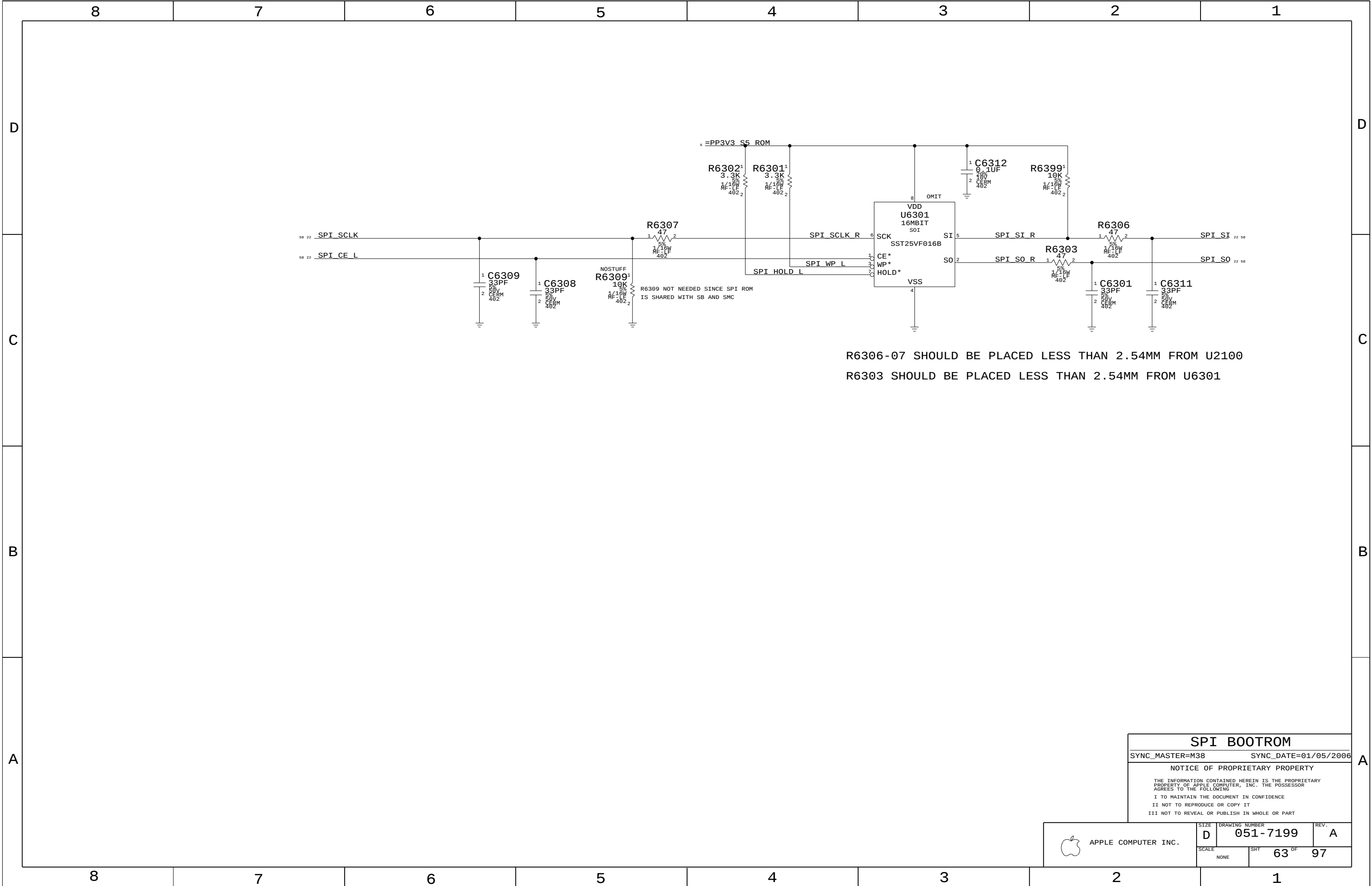


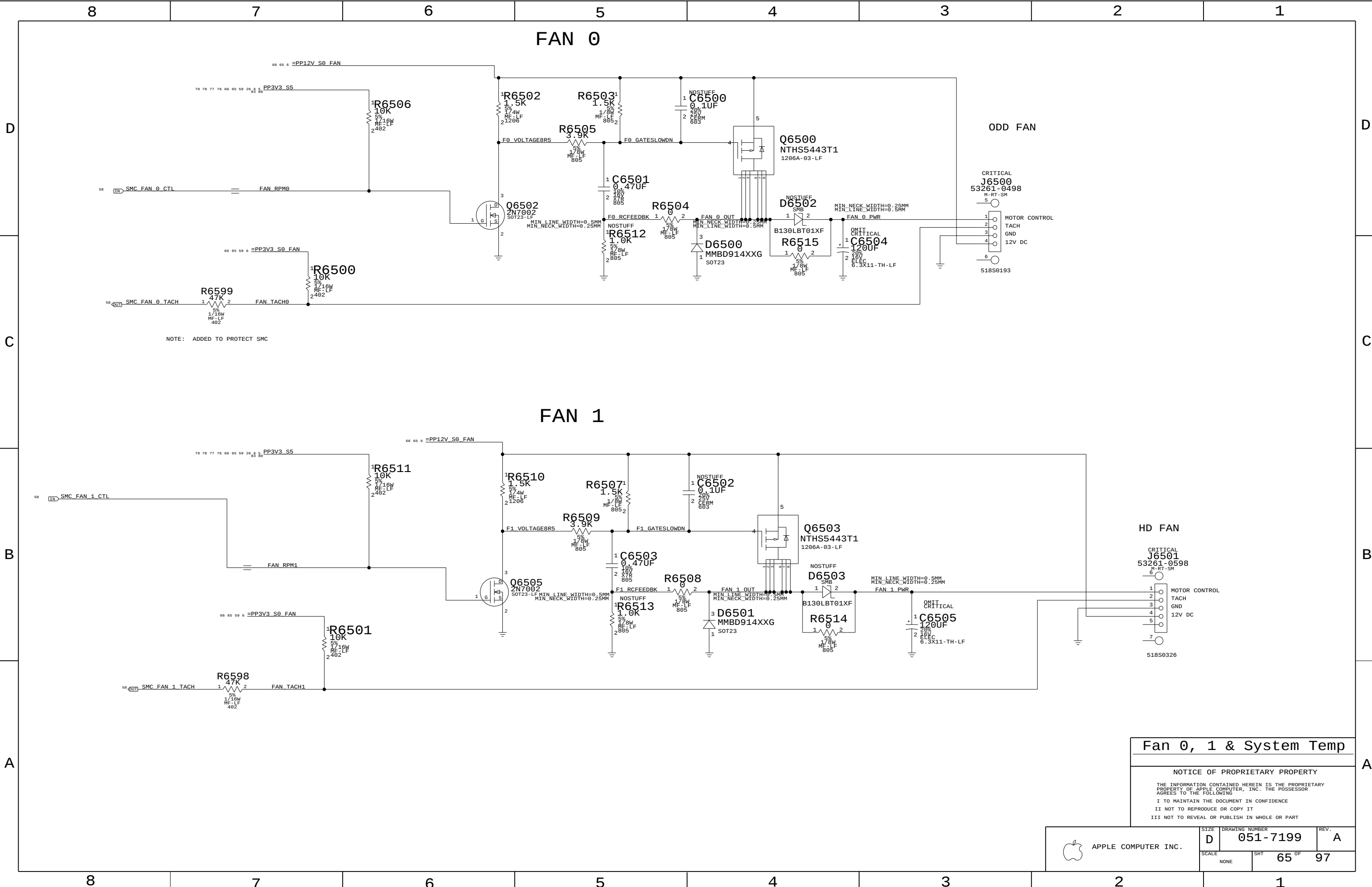
NB THERMAL

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHT 61	OF 97





FAN 0

FAN 1

Fan 0, 1 & System Temp

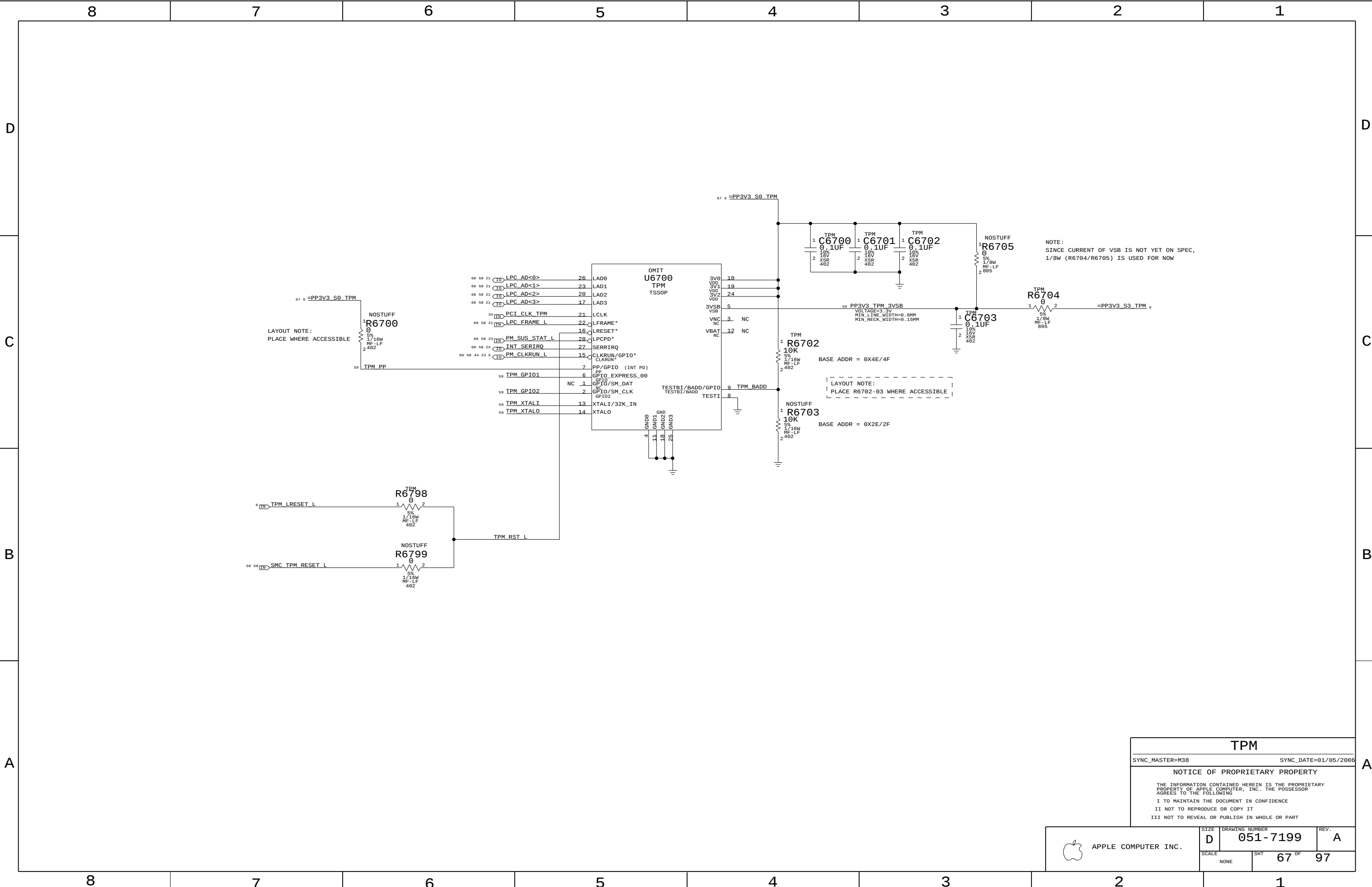
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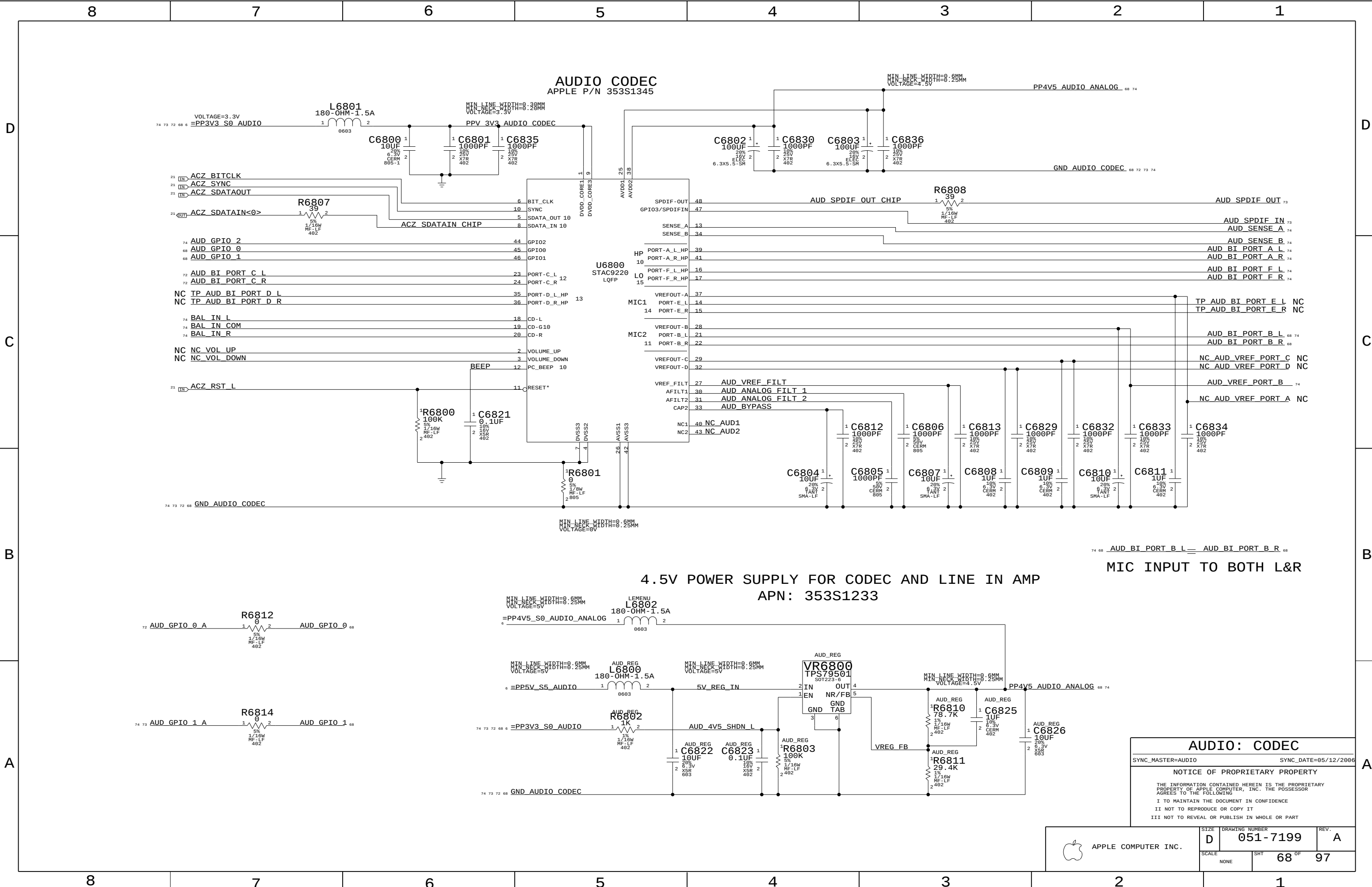
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7199	A
SCALE	SHT	OF
NONE	65	97



TPM		
SYNC_MASTER=M38		SYNC_DATE=01/05/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE		SHT	67 OF 97
NONE			



AUDIO: CODEC

SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

NOTICE OF PROPRIETARY PROPERTY

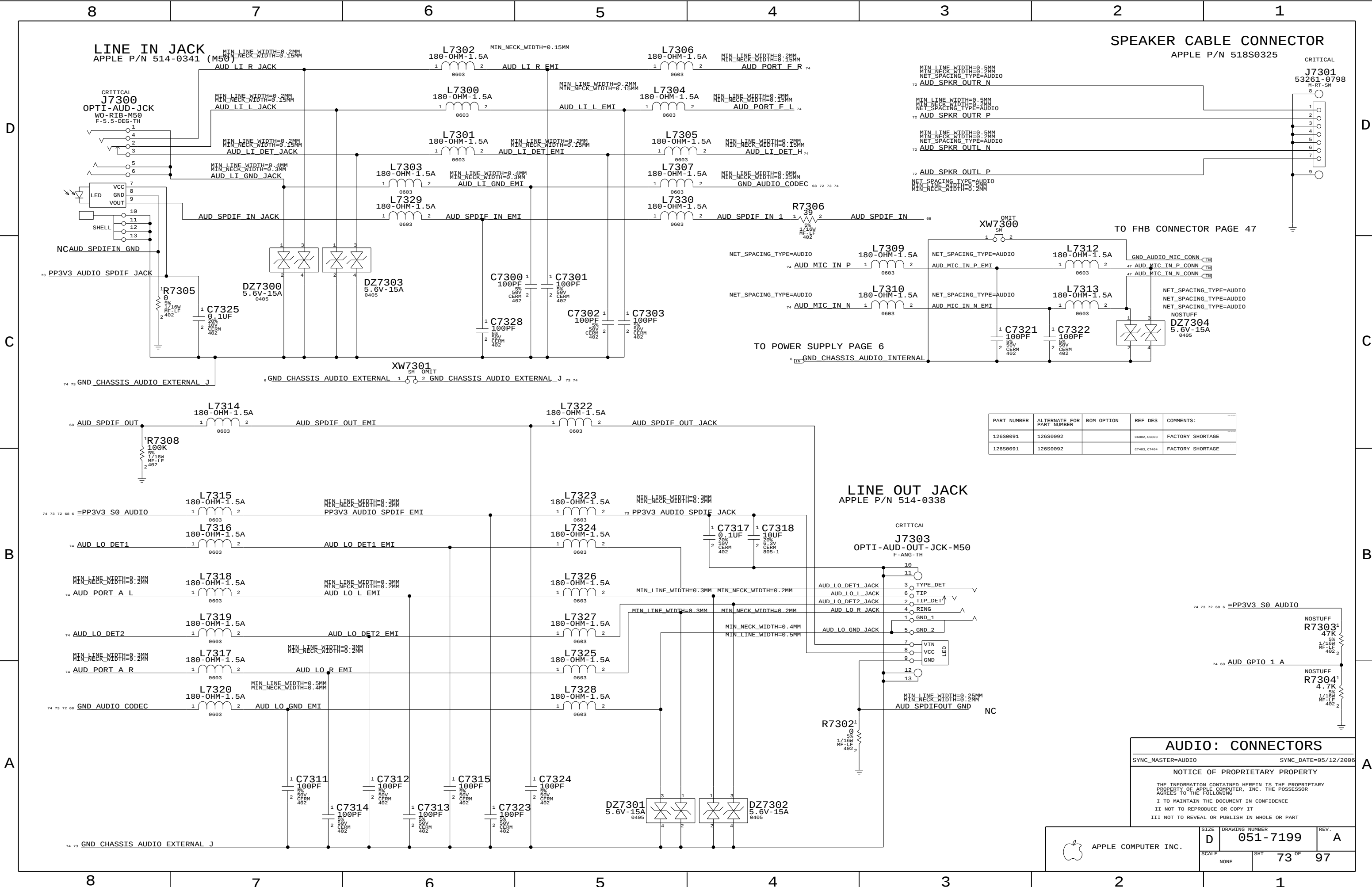
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE		SHT	68 OF 97
NONE			



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C8802, C8803	FACTORY SHORTAGE
126S0091	126S0092		C7493, C7494	FACTORY SHORTAGE

AUDIO: CONNECTORS

SYNC_MASTER=AUDIO

SYNC_DATE=05/12/2006

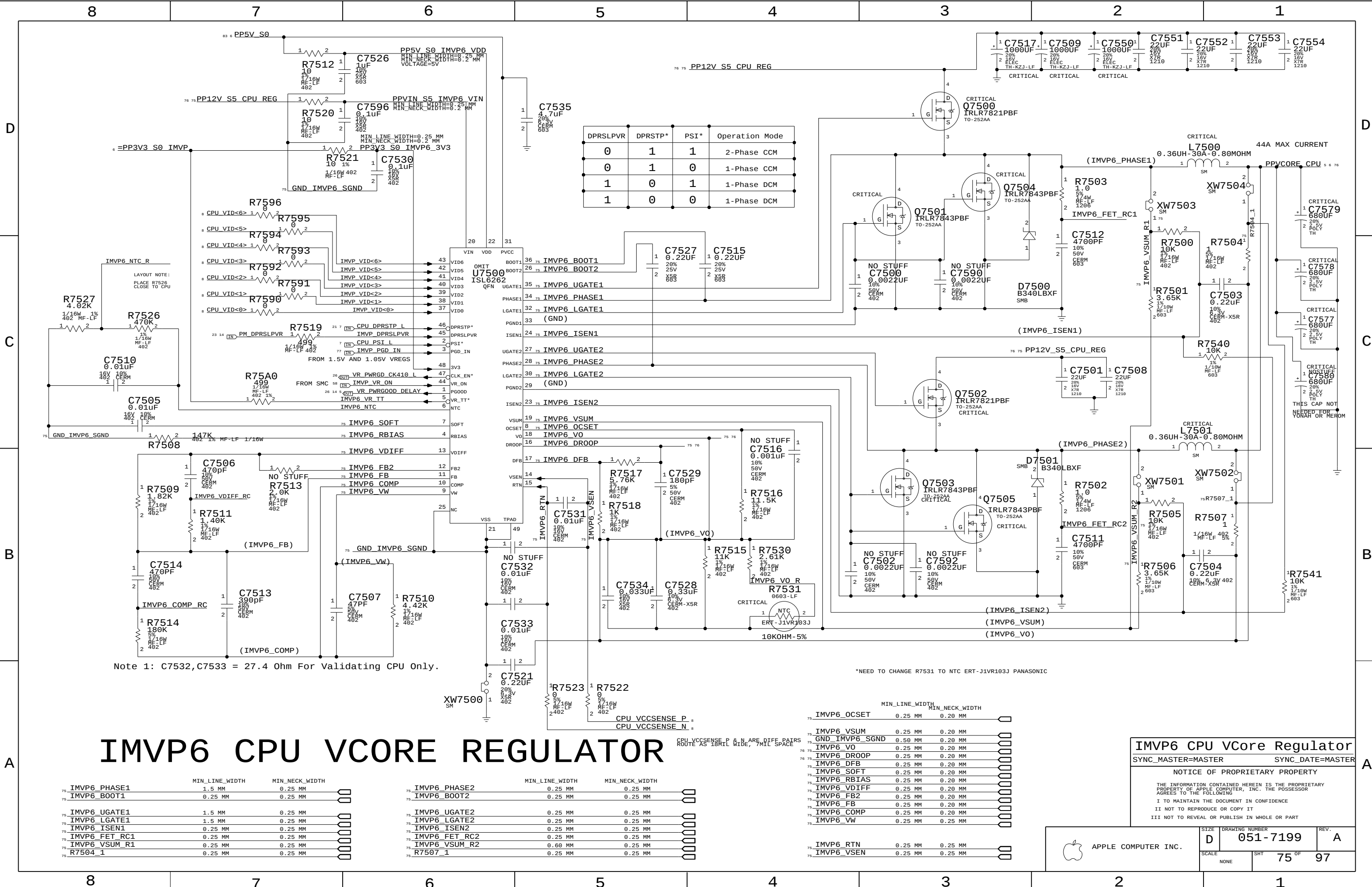
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IMVP6 CPU VCore REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_V0	0.25 MM	0.20 MM
IMVP6_DR00P	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTIN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

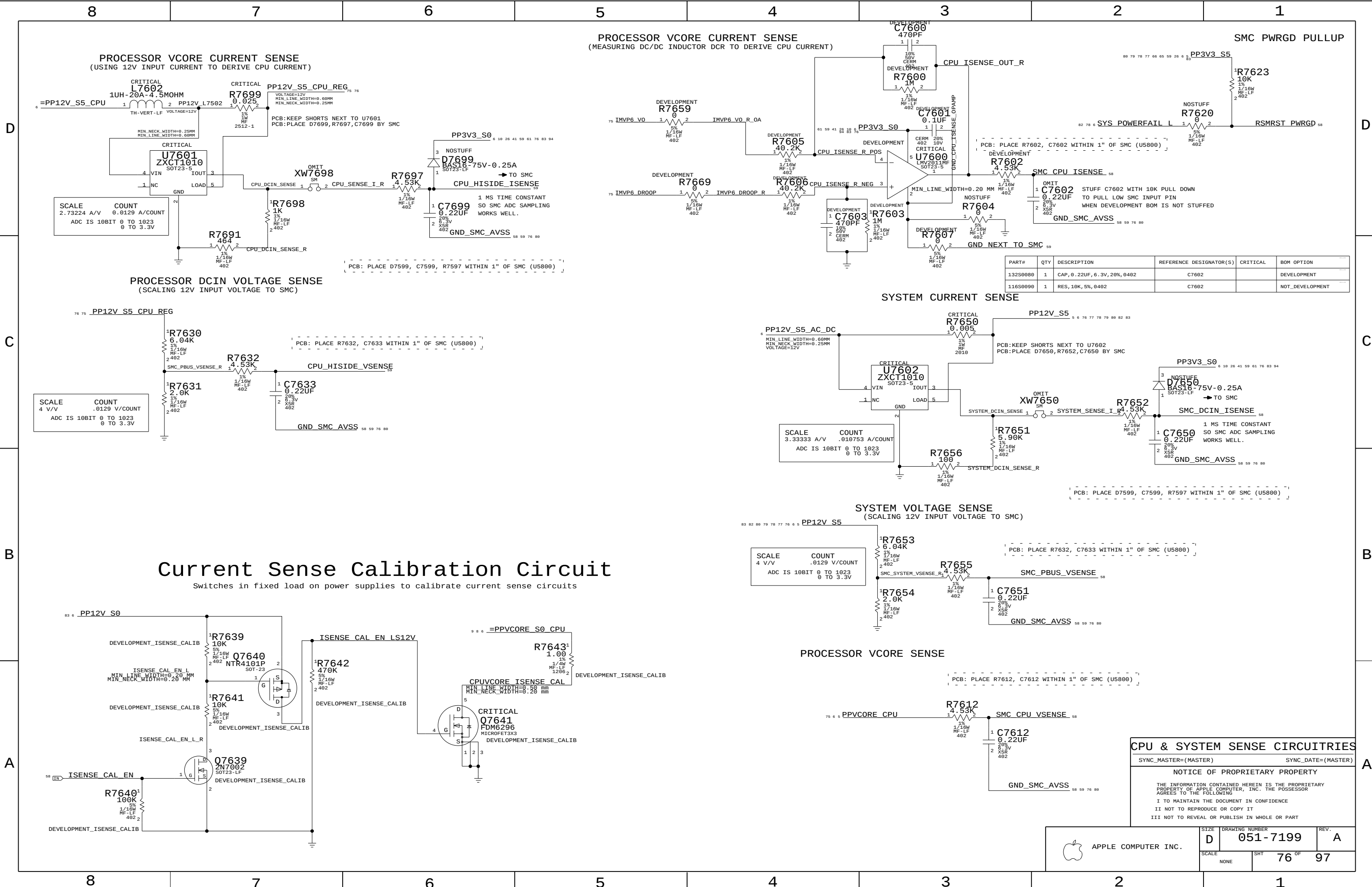
IMVP6 CPU VCore Regulator

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

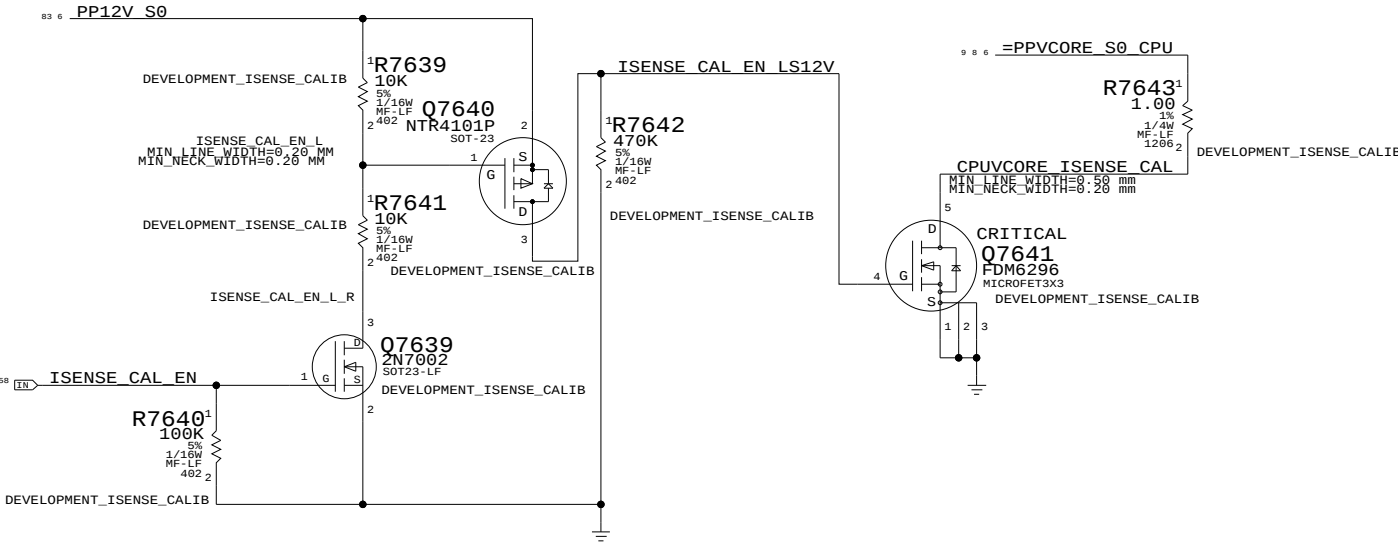
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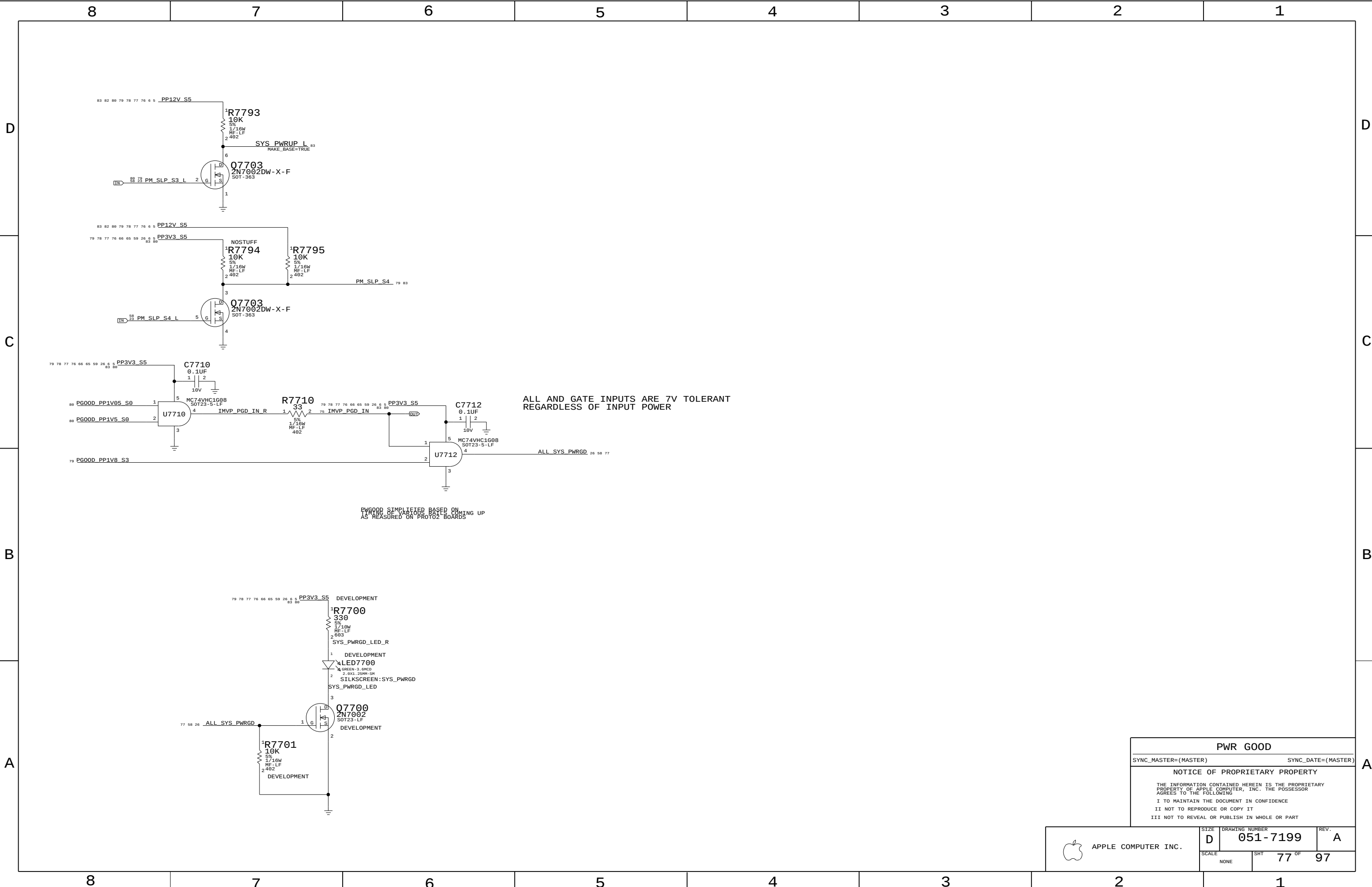
SIZE	D	DRAWING NUMBER	051-7199	REV.	A
SCALE	NONE	SHT	75 OF 97		



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits





PWR GOOD

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

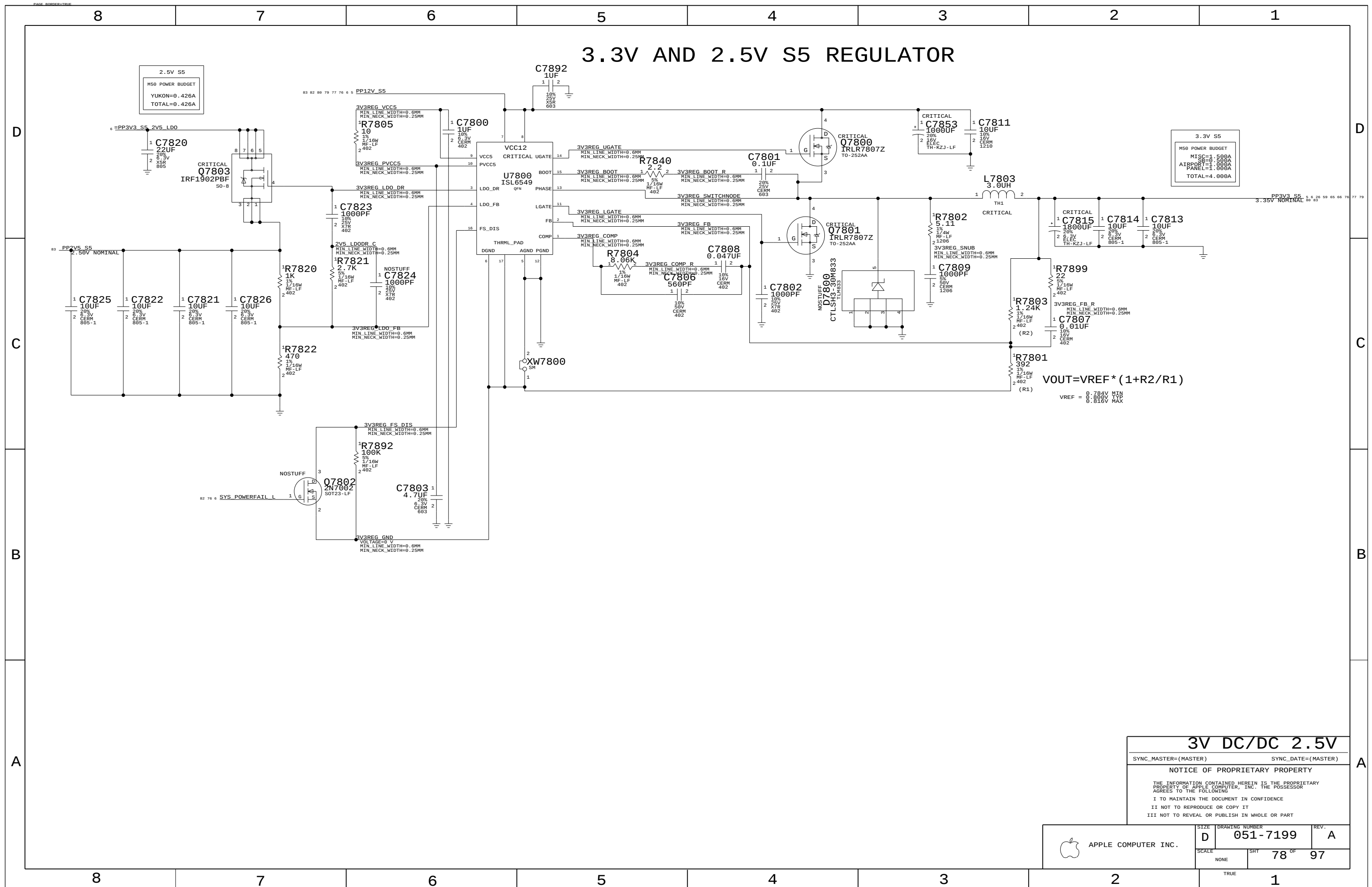
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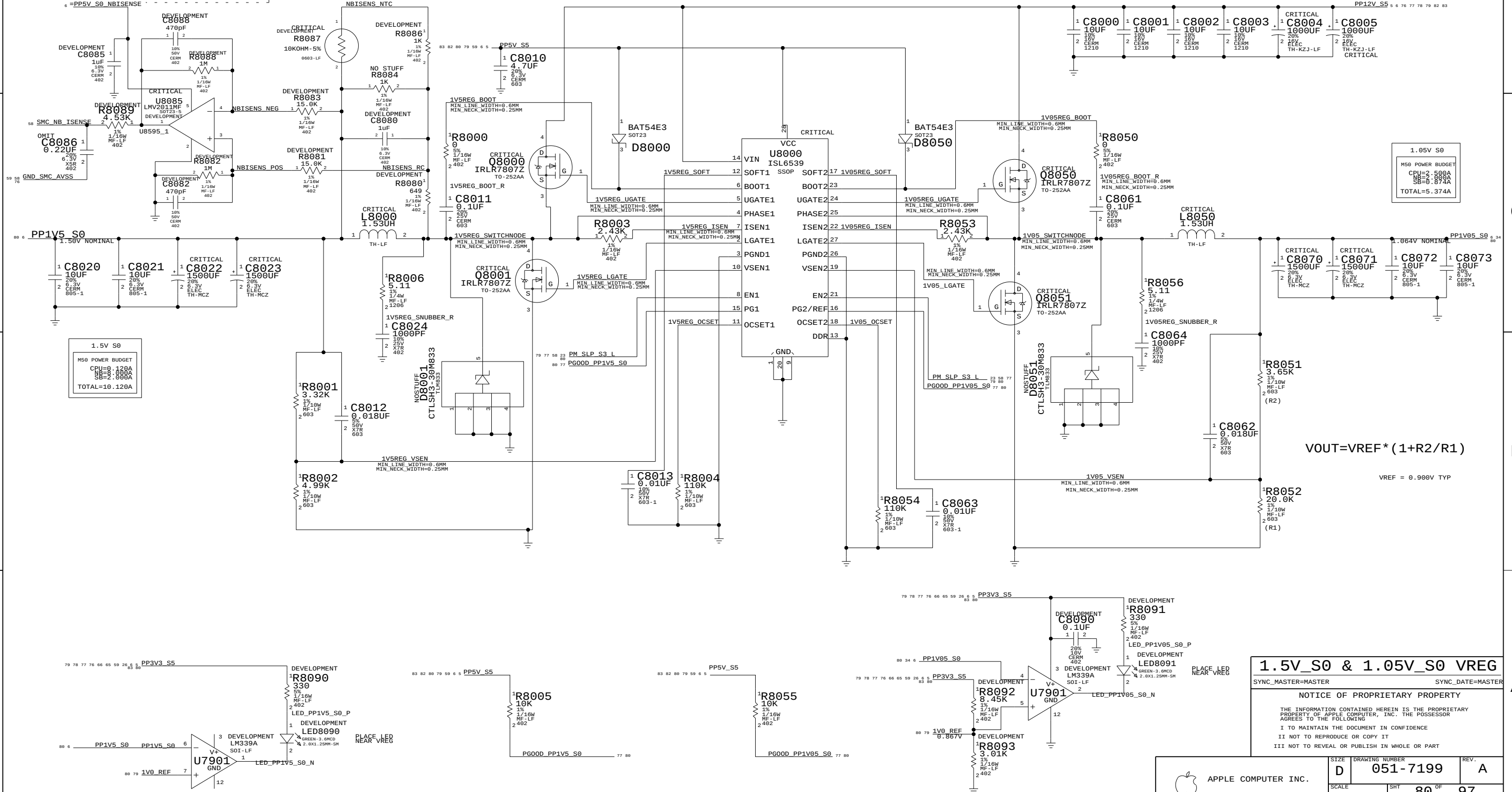
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE		SHT	77 OF 97
NONE			



1.5V S0 AND 1.05V S0 RAILS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP, 0.22UF, 6.3V, 20%, 0402	C8086		DEVELOPMENT
116S0090	1	RES, 10K, 5%, 0402	C8086		NOT_DEVELOPMENT

Placement Note:
KEEP C8080, R8080,
R8084 AND R8087
close to inductor



1.5V_S0 & 1.05V_S0 VREG

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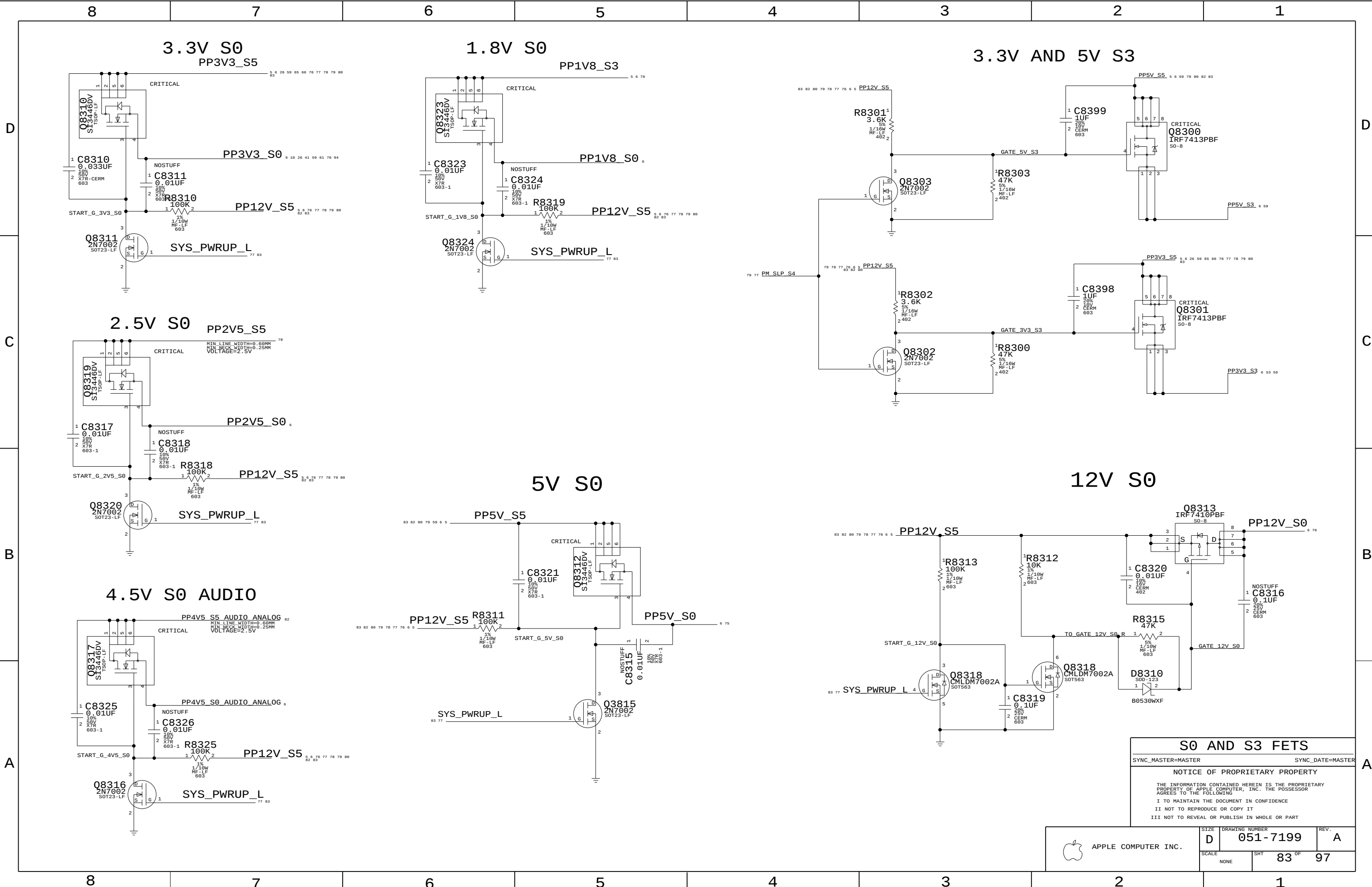
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S0 AND S3 FETS

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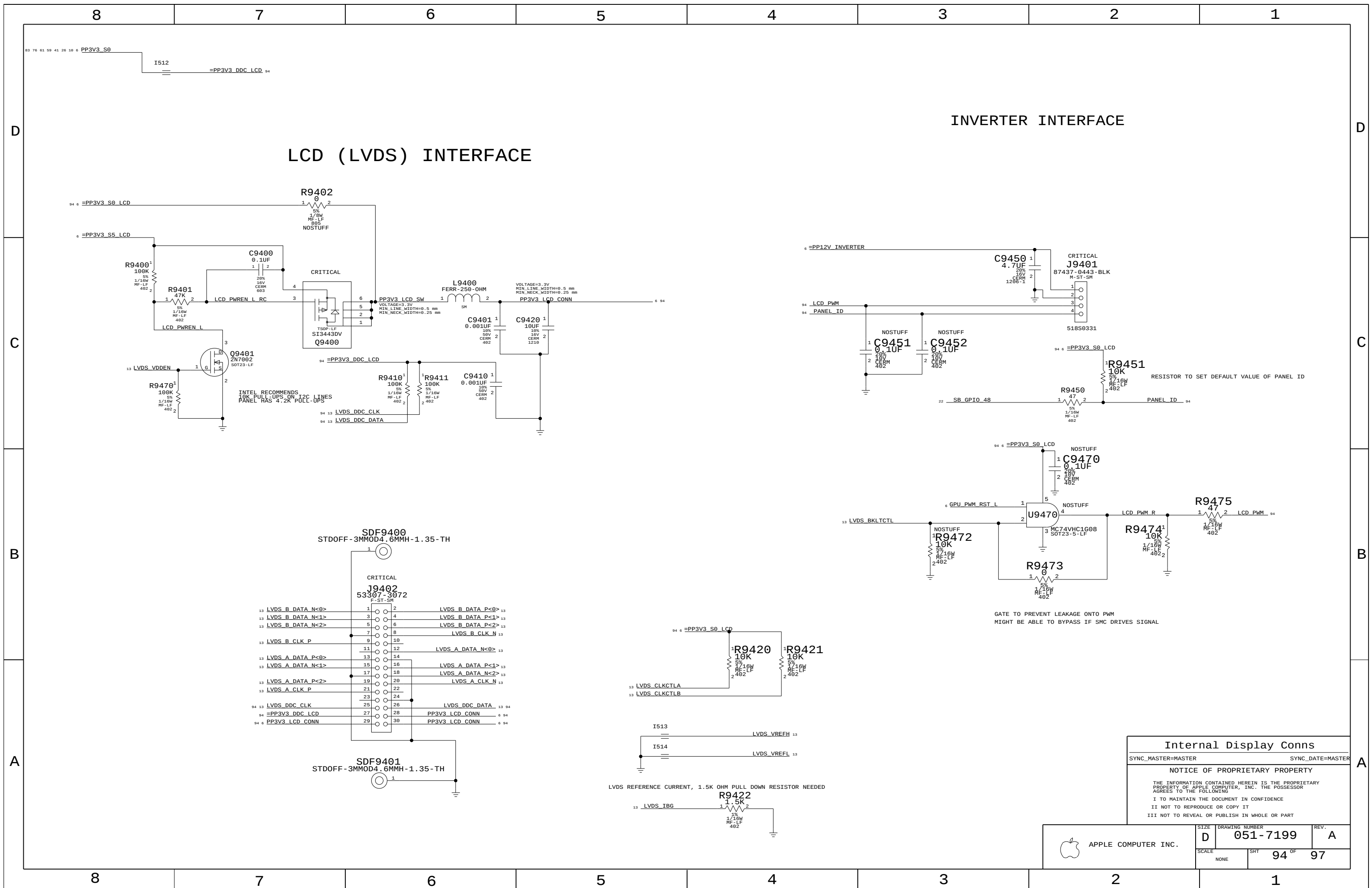
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8 7 6 5 4 3 2 1

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LCD (LVDS) INTERFACE

INVERTER INTERFACE

Internal Display Conns

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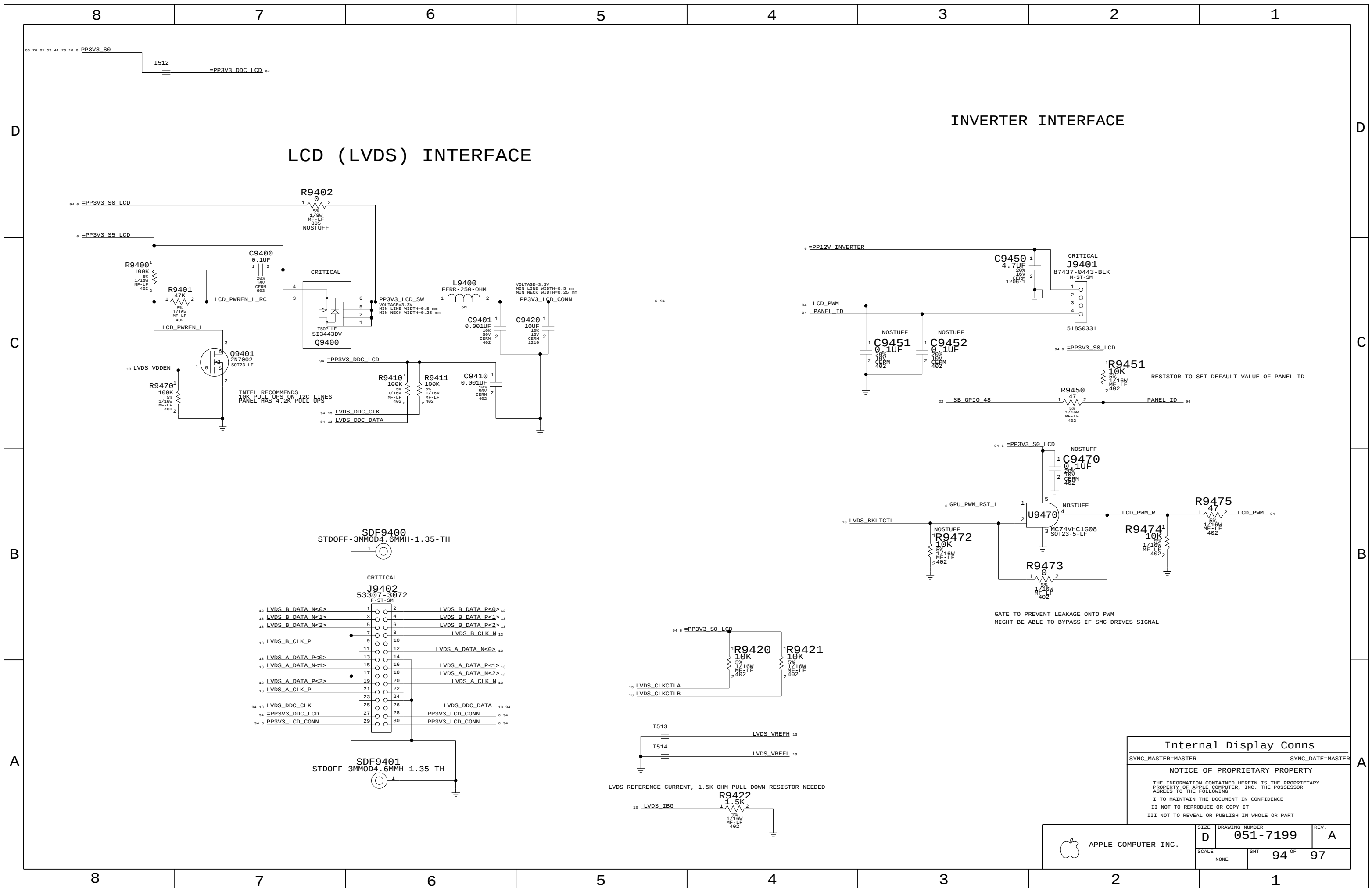
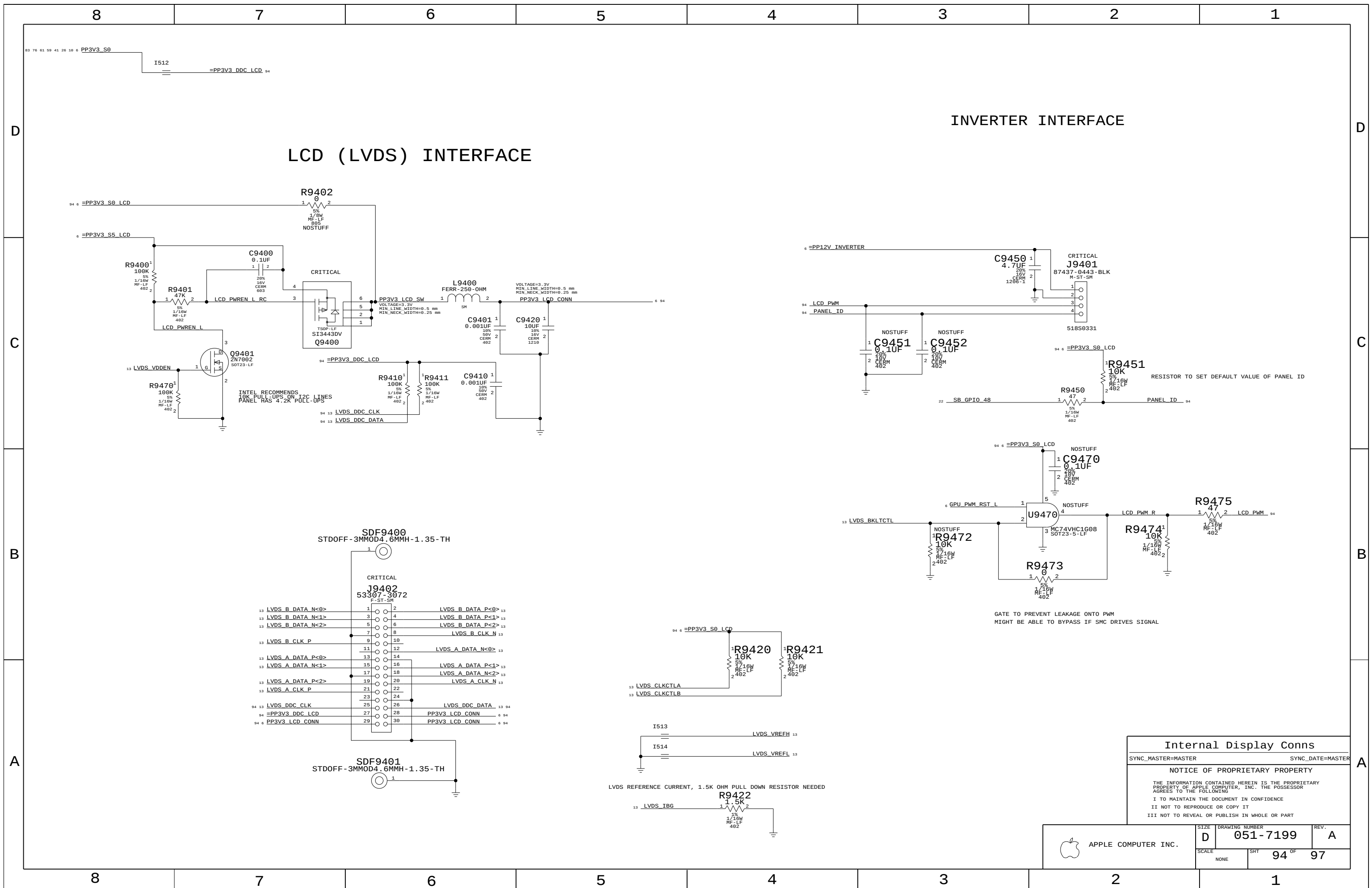
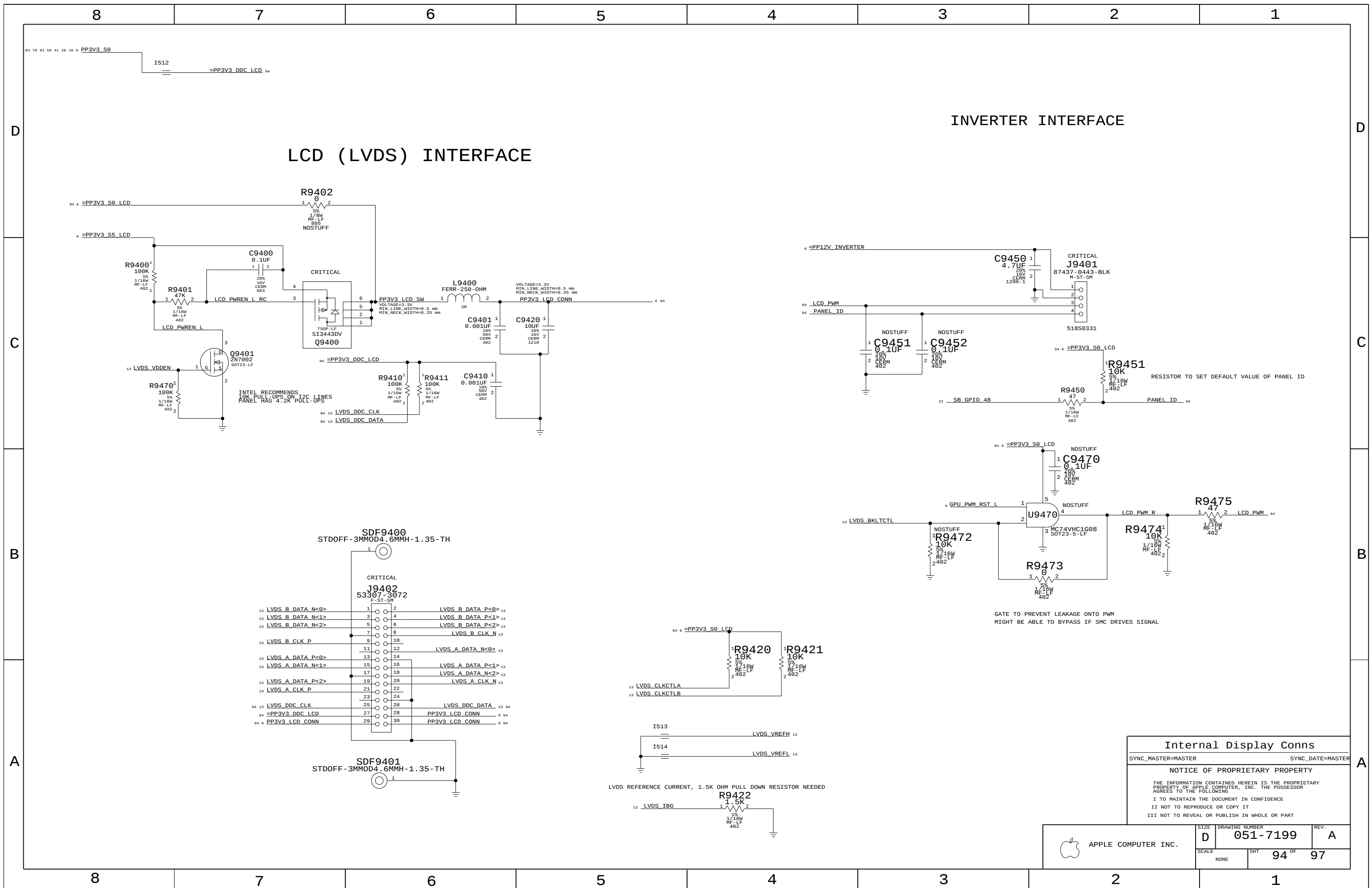
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LCD (LVDS) INTERFACE

INVERTER INTERFACE

Connector Pinout Table:

Signal	Pin	Signal	Pin
LVDS_B_DATA_N<0>	1	LVDS_B_DATA_P<0>	13
LVDS_B_DATA_N<1>	3	LVDS_B_DATA_P<1>	13
LVDS_B_DATA_N<2>	5	LVDS_B_DATA_P<2>	13
LVDS_B_CLK_P	7	LVDS_B_CLK_N	13
LVDS_A_DATA_P<0>	11	LVDS_A_DATA_N<0>	13
LVDS_A_DATA_N<1>	13	LVDS_A_DATA_P<1>	13
LVDS_A_DATA_P<2>	15	LVDS_A_DATA_N<2>	13
LVDS_A_CLK_P	17	LVDS_A_CLK_N	13
LVDS_DDC_CLK	19	LVDS_DDC_DATA	13
PP3V3_DDC_LCD	21	PP3V3_LCD_CONN	6
PP3V3_LCD_CONN	23	PP3V3_LCD_CONN	6

Internal Display Conns

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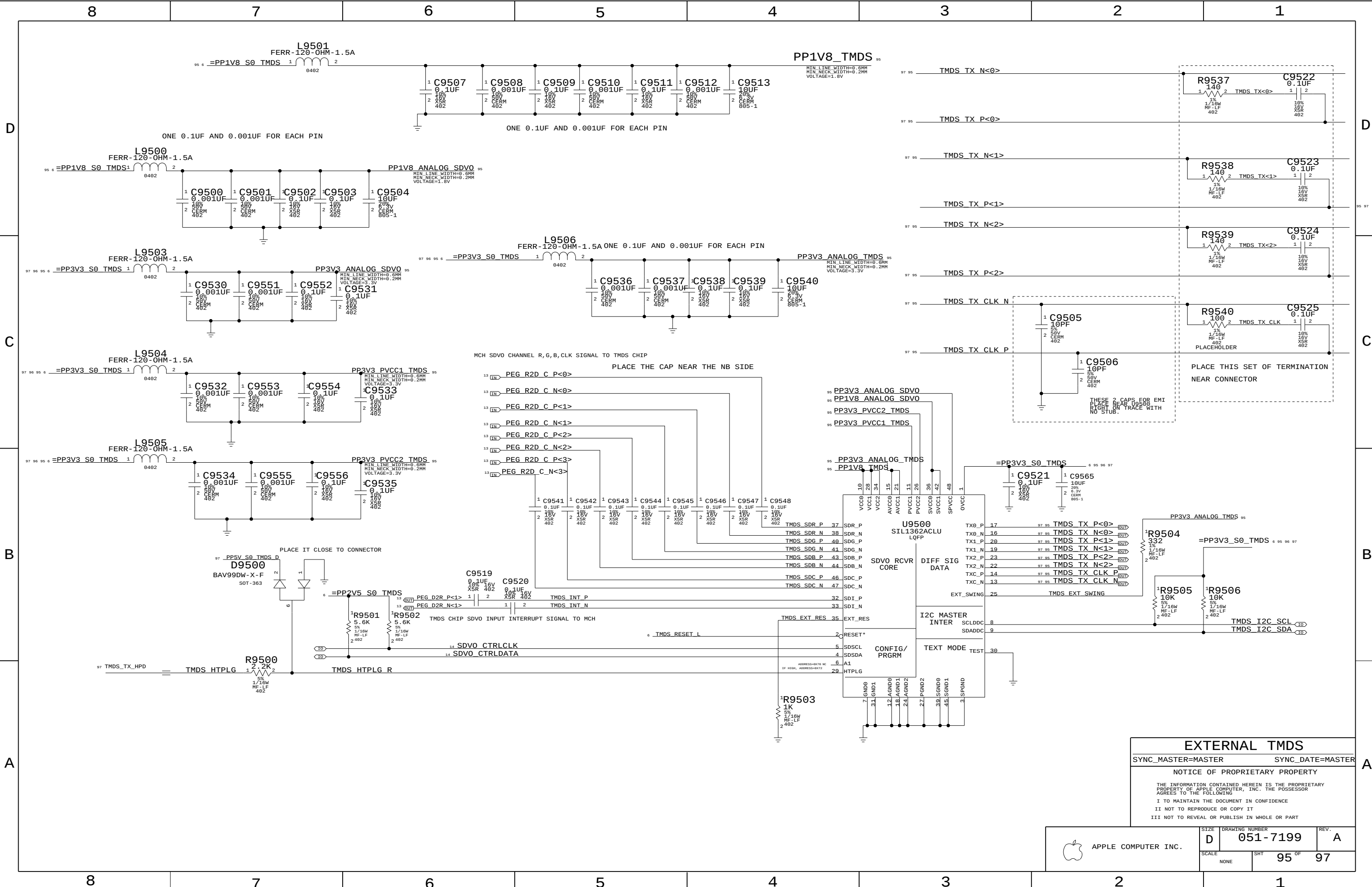
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EXTERNAL TMDs

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VGA SYNC BUFFERS

The schematic shows the connection of CRT and VGA sync signals. CRT_VSYNC_R and CRT_HSYNC_R are connected to 74LC125 buffers (U9670) through resistors R9600 and R9601. The outputs are connected to the TV_DACC_OUT and TV_DACB_OUT pins of U9620. The TV_DACC_OUT and TV_DACB_OUT pins are connected to the TV_DACC_OUT and TV_DACB_OUT pins of U9620. The TV_DACC_OUT and TV_DACB_OUT pins are connected to the TV_DACC_OUT and TV_DACB_OUT pins of U9620. The TV_DACC_OUT and TV_DACB_OUT pins are connected to the TV_DACC_OUT and TV_DACB_OUT pins of U9620.

PLACE RESISTORS AT NORTHBRIDGE

This section shows the connection of resistors R9690, R9691, R9692, R9693, R9694, R9695, R9697, R9698, and R9699 to the TV_DACC_OUT and TV_DACB_OUT pins of U9620. The resistors are connected to the TV_DACC_OUT and TV_DACB_OUT pins of U9620. The TV_DACC_OUT and TV_DACB_OUT pins are connected to the TV_DACC_OUT and TV_DACB_OUT pins of U9620. The TV_DACC_OUT and TV_DACB_OUT pins are connected to the TV_DACC_OUT and TV_DACB_OUT pins of U9620.

ANALOG FILTERING PLACE BY CONNECTOR

This section shows the connection of analog filters FL9600, FL9601, and FL9602 to the TV_DACC_OUT and TV_DACB_OUT pins of U9620. The filters are connected to the TV_DACC_OUT and TV_DACB_OUT pins of U9620. The TV_DACC_OUT and TV_DACB_OUT pins are connected to the TV_DACC_OUT and TV_DACB_OUT pins of U9620. The TV_DACC_OUT and TV_DACB_OUT pins are connected to the TV_DACC_OUT and TV_DACB_OUT pins of U9620.

TMSD/Inverter/ExtVGA

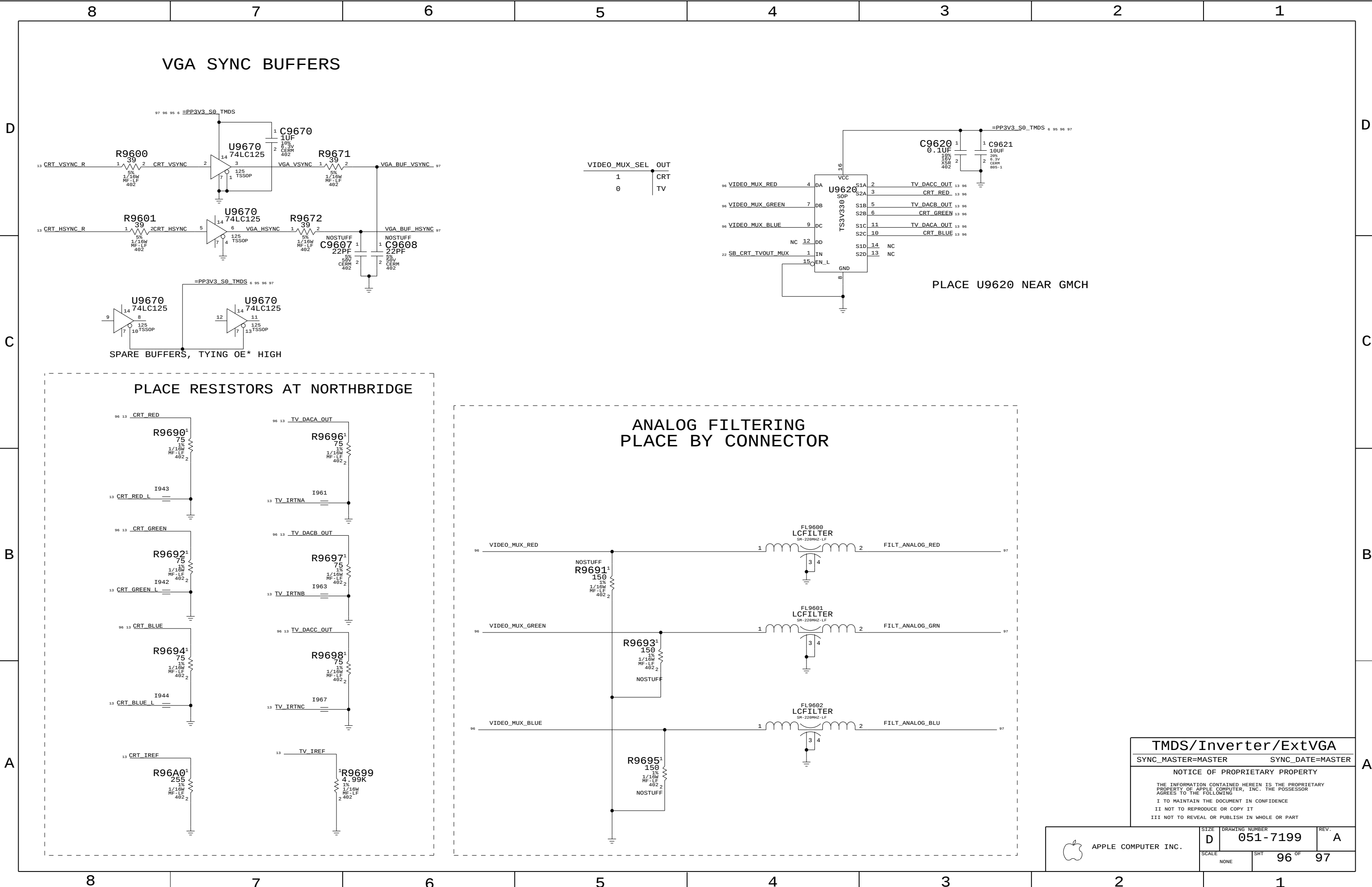
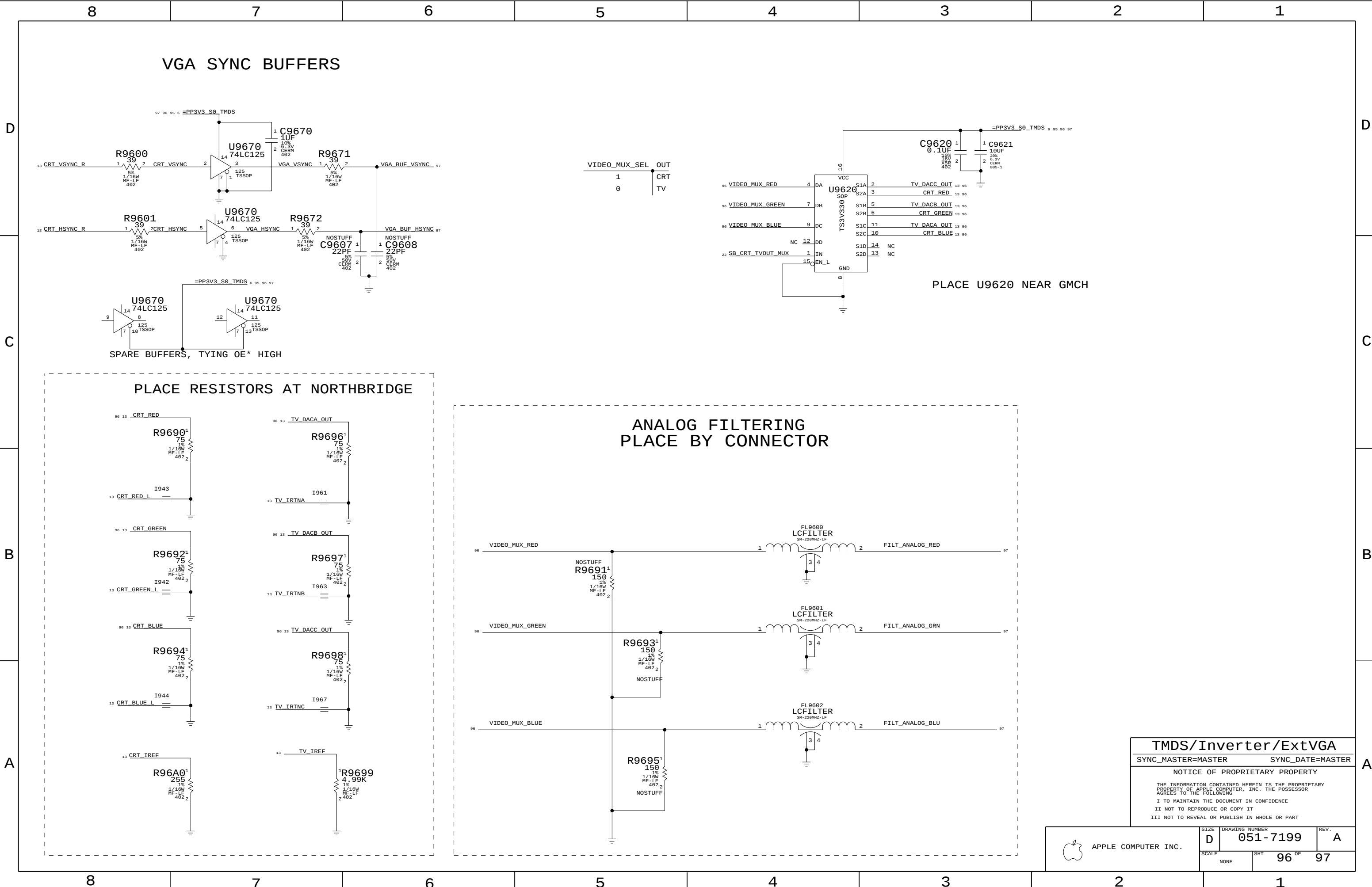
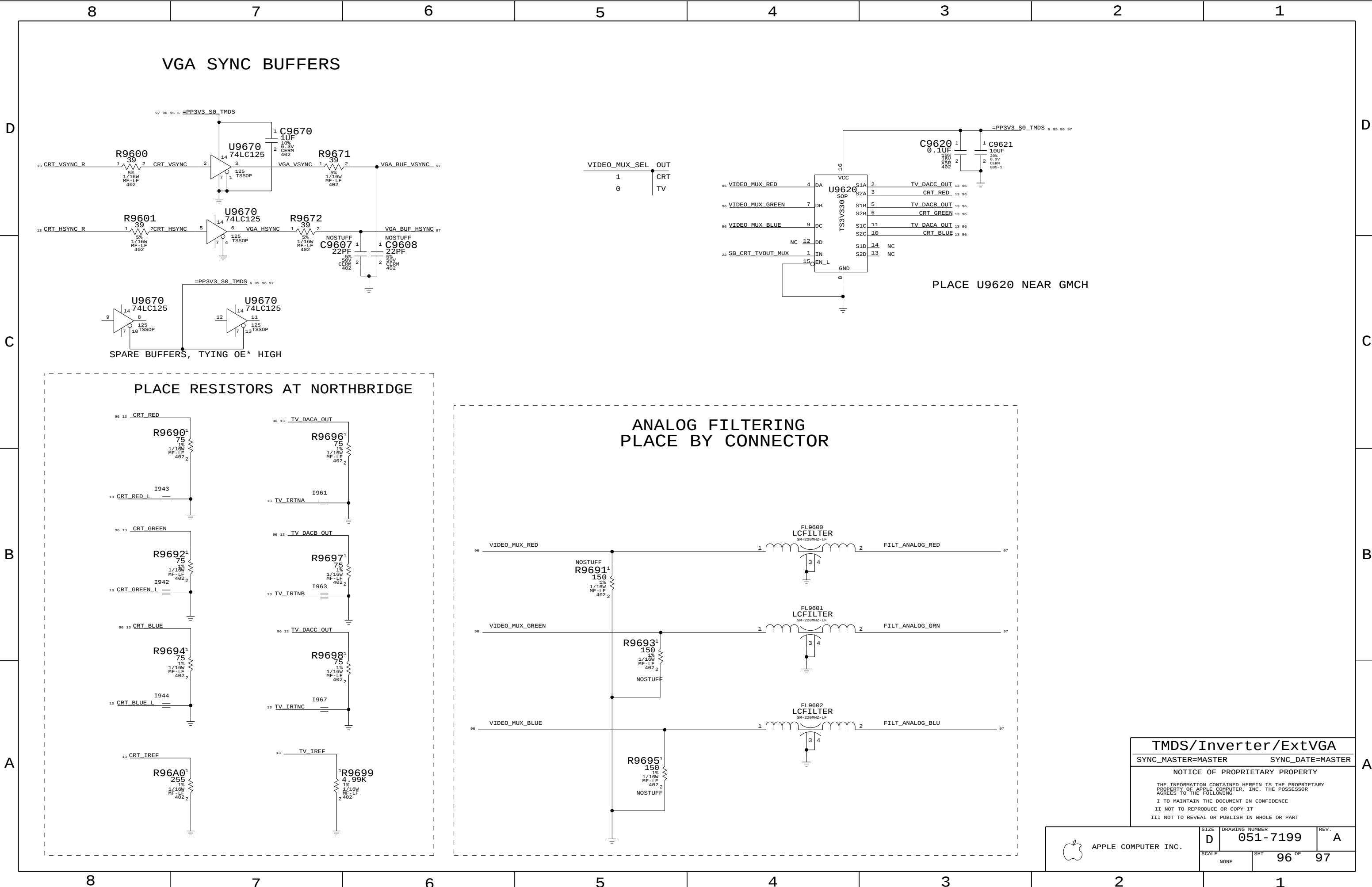
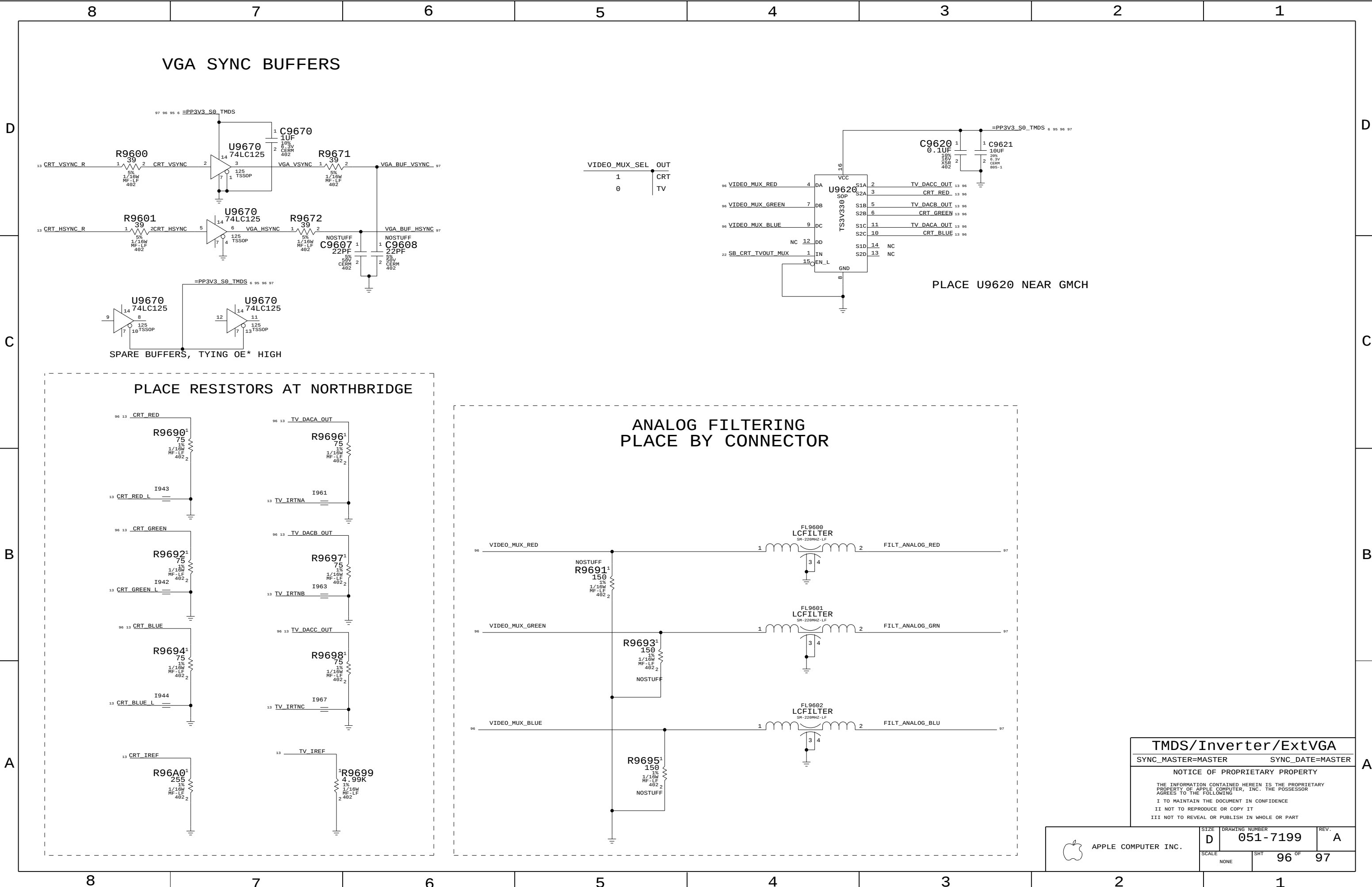
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[illegible][illegible]

VGA SYNC BUFFERS

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PLACE RESISTORS AT NORTHBRIDGE

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ANALOG FILTERING PLACE BY CONNECTOR

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TMSD/Inverter/ExtVGA

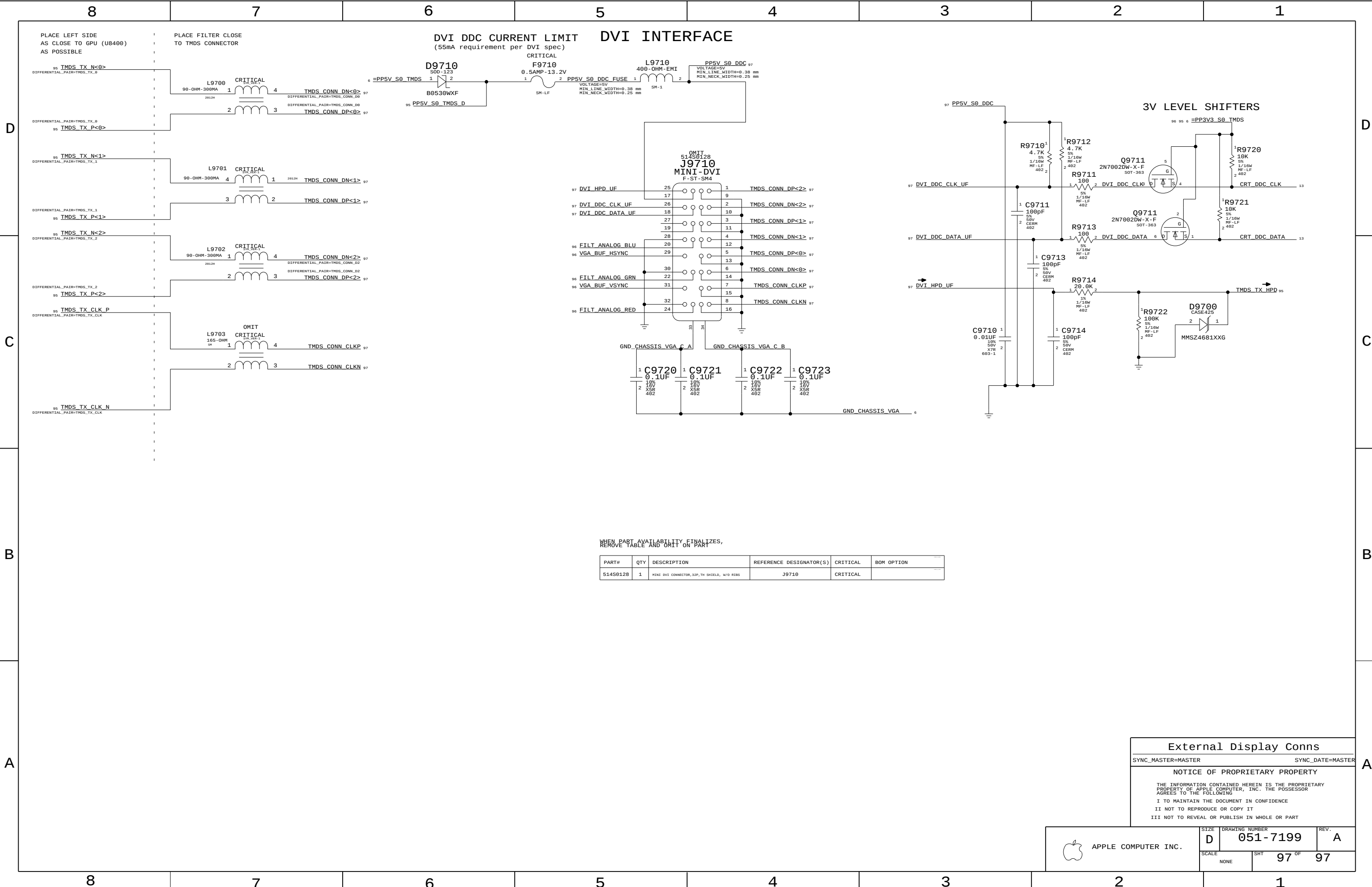
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WHEN PART AVAILABILITY FINALIZES,
REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0128	1	MINI DVI CONNECTOR, 32P, TH SHIELD, W/O RIBS	J9710	CRITICAL	

External Display Conns

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