1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SANTANA - M51 MLB

PVT REV A - 08/04/06

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
A		453469	PRODUCTION RELEASED	08/04/06	06/22/04

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8	8	CPU 2 OF 2-PWR/GND	M50_HENRY	08/04/2006
9	9	CPU DECAPS & VID<>	M51_HENRY	08/04/2006
10	10	ASIC TEMP SENSORS	M51_DAVE	(MASTER)
11	11	CPU ITP700FLEX DEBUG	M50_HENRY	08/04/2006
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16	16	NB Power 1	M51_HENRY	08/04/2006
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32	33	CLOCKS	M50_HENRY	08/04/2006
33	34	CLOCKS: TERMINATIONS	M51_HENRY	08/04/2006
34	38	Disk Connectors	M51_DOUG	08/04/2006
35	41	ETHERNET CONTROLLER	M50_DOUG	08/04/2006
36	42	ETHERNET MISC	M51_DOUG	08/04/2006
37	43	ETHERNET CONNECTOR	M51_DOUG	08/04/2006
38	44	FW: 1394B-LINK/PHY	M51_DOUG	08/04/2006
39	45	FW: 1394B MISC	M51_DOUG	08/04/2006
40	46	FIREWIRE CONNECTORS	M51_DOUG	08/04/2006
41	47	USB Device Interfaces	M51_DOUG	08/04/2006
42	53	AIRPORT CONN	M51_DOUG	08/04/2006
43	54	PCI-E CONNECTIONS	M51_DOUG	08/04/2006
44	58	SMC	M51_HENRY	08/04/2006
45	59	SMC & TPM SUPPORT	M51_HENRY	07/31/2006
46	60	LPC+ CONN	M51_HENRY	08/04/2006
47	63	SPI BOOTROM	M50_DOUG	08/04/2006
48	65	HD AND OD FAN	M51_HENRY	08/04/2006
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50	67	TPM	M51_HENRY	08/04/2006
51	68	AUDIO: CODEC	AUDIO	08/04/2006
52	69	AUDIO: LINE INPUT AMP	AUDIO	08/04/2006
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55	72	AUDIO: SPEAKER AMP	AUDIO	08/04/2006
56	73	AUDIO: CONNECTORS	AUDIO	08/04/2006
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58	75	IMVP6 CPU VCore Regulator	M51_PAUL	08/04/2006
59	76	CPU & SYSTEM SENSE	M51_DAVE	(MASTER)
60	77	PWR GOOD	M51_PAUL	08/04/2006
61	78	3V DC/DC 2.5V	M51_PAUL	08/04/2006
62	79	1.8V & 1.2V VREG	M51_PAUL	08/04/2006
63	80	1.5V_S0 & 1.05V_S0 VREG	M51_PAUL	08/04/2006
64	82	5V DC/DC	M51_PAUL	08/04/2006
65	83	S0 AND S3 FETS	M51_PAUL	08/04/2006
66	84	MXM PCI-E & PWR	M51_DAVE	(MASTER)
67	85	MXM I/O	M51_DAVE	(MASTER)
68	94	Internal Display Conns	M51_DAVE	(MASTER)
69	97	External Display Conns	M51_DAVE	(MASTER)

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7039	1	PCB,SCHEM,MLB,M51	SCH1		
820-1984	1	PCB,FAB,MLB,M51	MLB1		

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK
ENG APPD | MFG APPD
QA APPD | DESIGNER
RELEASE | SCALE NONE
MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D

Apple Computer Inc.

TITLE
SCHEM SANTANA

DRAWING NUMBER 051-7039 | REV. A

SHT 1 OF 97

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(1.83/2.17GHZ)
CORE (~1.2V)
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CAMERA

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5
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J5300 (AIRPORT CONN)

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3.3V/133MHZ

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PORT 3

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AZALIA
PCI
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SMB
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X1 - 1.5GHZ
X1 - 1.5GHZ

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U3301
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J5300
AIRPORT

33MHZ
32-BIT

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2 Diff pairs

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PORT C
PORT F
PORT B

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J7303
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LINE IN

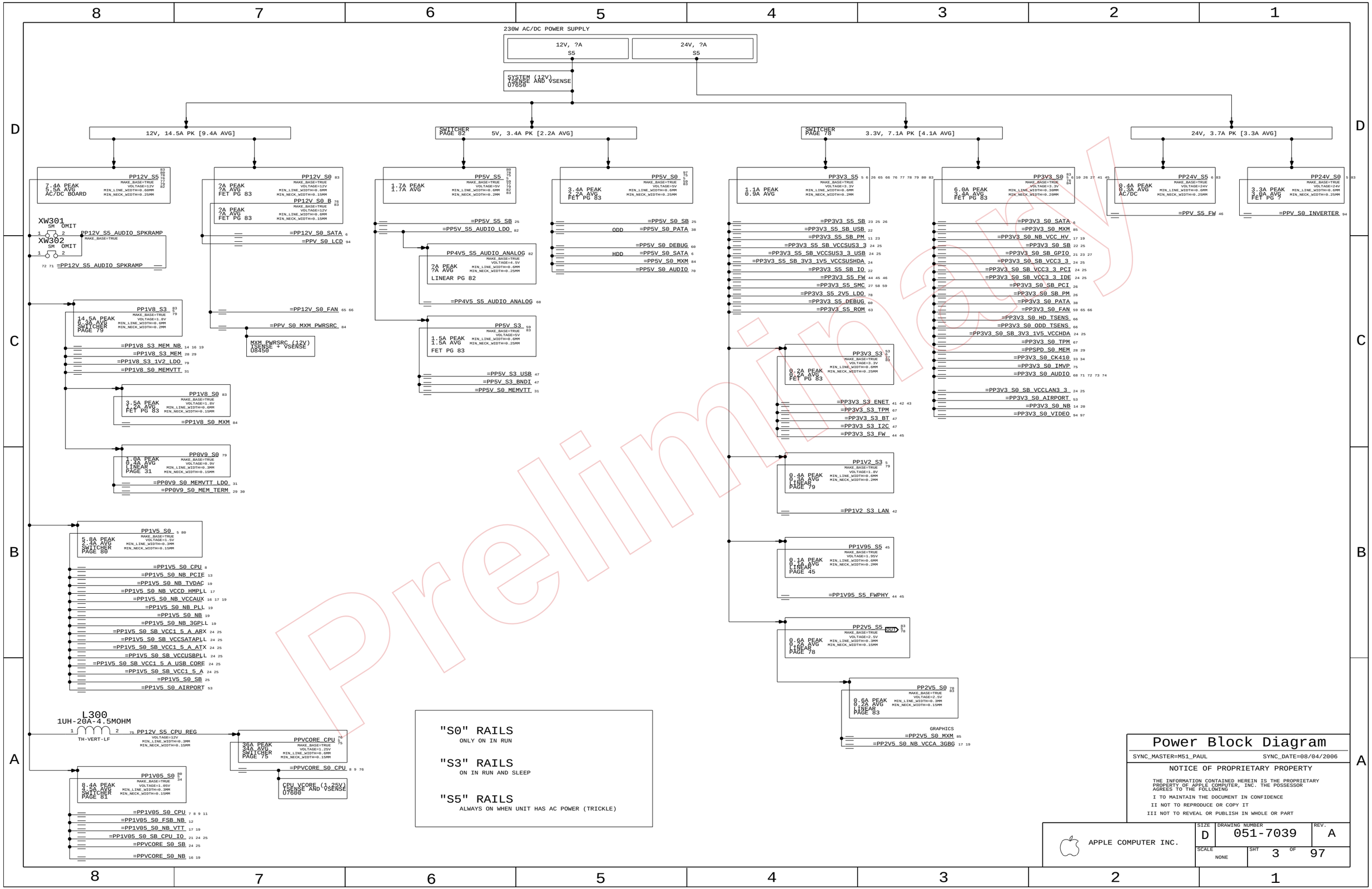
JE350
MIC IN
BNDI
INTERFACE

System Block Diagram

SYNC_MASTER=M51_PAUL
SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 2 OF 97	


230W AC/DC POWER SUPPLY
12V, ?A
S5
24V, ?A
S5
SYSTEM (12V)
ISENSE AND VSENSE
U7650
12V, 14.5A PK [9.4A AVG]
SWITCHER
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5V, 3.4A PK [2.2A AVG]
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24V, 3.7A PK [3.3A AVG]
PP12V_S5
7.4A PEAK
5.5A AVG
AC/DC BOARD
PP12V_S0
2A PEAK
2A AVG
FET PG 83
PP12V_S0_B
2A PEAK
2A AVG
FET PG 83
PP5V_S5
1.7A PEAK
1.7A AVG
PP5V_S0
3.4A PEAK
2.2A AVG
FET PG 83
PP3V3_S5
1.1A PEAK
0.9A AVG
PP3V3_S0
6.0A PEAK
3.4A AVG
FET PG 83
PP24V_S5
0.4A PEAK
0.3A AVG
AC/DC
PP24V_S0
3.3A PEAK
3.0A AVG
FET PG ?
XW301
SM OMIT
XW302
SM OMIT
PP12V_S5_AUDIO_SPKRAMP
=PP12V_S5_AUDIO_SPKRAMP
=PP12V_S0_SATA
=PPV_S0_LCD
=PP12V_S0_FAN
=PPV_S0_MXM_PWRSRC
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ISENSE + VSENSE
U8450
=PP5V_S5_SB
=PP5V_S5_AUDIO_LDO
PP4V5_S5_AUDIO_ANALOG
2A PEAK
2A AVG
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=PP4V5_S5_AUDIO_ANALOG
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1.5A PEAK
1.5A AVG
FET PG 83
=PP5V_S3_USB
=PP5V_S3_BNDI
=PP5V_S0_MEMVTT
=PP5V_S0_SB
=PP5V_S0_DEBUG
ODD =PP5V_S0_PATA
HDD =PP5V_S0_SATA
=PP5V_S0_MXM
=PP5V_S0_AUDIO
=PP3V3_S5_SB
=PP3V3_S5_SB_USB
=PP3V3_S5_SB_PM
=PP3V3_S5_SB_VCCSUS3_3
=PP3V3_S5_SB_VCCSUS3_3_USB
=PP3V3_S5_SB_3V3_1V5_VCCSUSHDA
=PP3V3_S5_SB_IO
=PP3V3_S5_FW
=PP3V3_S5_SMC
=PP3V3_S5_2V5_LDO
=PP3V3_S5_DEBUG
=PP3V3_S5_ROM
=PP3V3_S0_SATA
=PP3V3_S0_MXM
=PP3V3_S0_NB_VCC_HV
=PP3V3_S0_SB
=PP3V3_S0_SB_GPIO
=PP3V3_S0_SB_VCC3_3
=PP3V3_S0_SB_VCC3_3_PCI
=PP3V3_S0_SB_VCC3_3_IDE
=PP3V3_S0_SB_PCI
=PP3V3_S0_SB_PM
=PP3V3_S0_PATA
=PP3V3_S0_FAN
=PP3V3_S0_HD_TSENS
=PP3V3_S0_ODD_TSENS
=PP3V3_S0_SB_3V3_1V5_VCCHDA
=PP3V3_S0_TPM
=PPSPD_S0_MEM
=PP3V3_S0_CK410
=PP3V3_S0_IMVP
=PP3V3_S0_AUDIO
=PP3V3_S0_SB_VCCLAN3_3
=PP3V3_S0_AIRPORT
=PP3V3_S0_NB
=PP3V3_S0_VIDEO
=PPV_S5_FW
=PPV_S0_INVERTER
PP3V3_S3
0.2A PEAK
0.2A AVG
FET PG 83
=PP3V3_S3_ENET
=PP3V3_S3_TPM
=PP3V3_S3_BT
=PP3V3_S3_I2C
=PP3V3_S3_FW
PP1V2_S3
0.4A PEAK
0.3A AVG
LINEAR
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=PP1V2_S3_LAN
PP1V95_S5
0.1A PEAK
0.1A AVG
LINEAR
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=PP1V95_S5_FWPHY
PP2V5_S5
0.6A PEAK
0.2A AVG
LINEAR
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PP2V5_S0
0.6A PEAK
0.2A AVG
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=PP2V5_S0_MXM
=PP2V5_S0_NB_VCCA_3GBG
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=PP1V8_S3_MEM_NB
=PP1V8_S3_MEM
=PP1V8_S3_1V2_LDO
=PP1V8_S0_MEMVTT
PP1V8_S0
3.5A PEAK
1.2A AVG
FET PG 83
=PP1V8_S0_MXM
PP0V9_S0
1.0A PEAK
0.4A AVG
LINEAR
PAGE 31
=PP0V9_S0_MEMVTT_LDO
=PP0V9_S0_MEM_TERM
PP1V5_S0
5.8A PEAK
2.4A AVG
SWITCHER
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=PP1V5_S0_CPU
=PP1V5_S0_NB_PCIE
=PP1V5_S0_NB_TVDAC
=PP1V5_S0_NB_VCCD_HMPLL
=PP1V5_S0_NB_VCCAUX
=PP1V5_S0_NB_PLL
=PP1V5_S0_NB
=PP1V5_S0_NB_3GPLL
=PP1V5_S0_SB_VCC1_5_A_ARX
=PP1V5_S0_SB_VCCSATAPLL
=PP1V5_S0_SB_VCC1_5_A_ATX
=PP1V5_S0_SB_VCCUSBPLL
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
=PP1V5_S0_SB_VCC1_5_A
=PP1V5_S0_SB
=PP1V5_S0_AIRPORT
L300
1UH-20A-4.5MOHM
TH-VERT-LF
PP12V_S5_CPU_REG
PPVCORE_CPU
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34A AVG
SWITCHER
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=PPVCORE_S0_CPU
CPU VCORE (1.25V)
ISENSE AND VSENSE
U7600
PP1V05_S0
8.4A PEAK
4.5A AVG
SWITCHER
PAGE 81
=PP1V05_S0_CPU
=PP1V05_S0_FSB_NB
=PP1V05_S0_NB_VTT
=PP1V05_S0_SB_CPU_IO
=PPVCORE_S0_SB
=PPVCORE_S0_NB
"S0" RAILS
ONLY ON IN RUN
"S3" RAILS
ON IN RUN AND SLEEP
"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)
Power Block Diagram
SYNC_MASTER=M51_PAUL
SYNC_DATE=08/04/2006
NOTICE OF PROPRIETARY PROPERTY
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DRAWING NUMBER
051-7039
REV.
A
SCALE
NONE
SHT
3
OF
97

Production BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7512	PCBA,MLB,2.33GHz,M51	M51_COMMON,M51_BEST,EEE_V4K,PRODUCTION
630-7595	PCBA,MLB,2.16GHz,M51	M51_COMMON,M51_BETTER,EEE_VMD,PRODUCTION

Development BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
603-8960	PCBA,DEVBOM,M51	M51_DEVELOPMENT

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M51_COMMON	COMMON,M51_COMMON1,M51_COMMON2,ALTERNATE
M51_COMMON1	CPU_TSENS_EXT,GPU_TSENS_INT,GPU_TSENS_EXT,MXM_ROM,NBCFG_PEG_REVERSE
M51_COMMON2	SB_SYSRST_4_PVT,ITP,MEROM,AMB_TSENS,CPU_PWR_SENSE,MXM_PWR_SENSE
M51_DEVELOPMENT	DEVELOPMENT,M51_DEV1
M51_DEV1	CPU_TSENS_INT,SYS_PWR_SENSE

BarCode Label / EEE #'s

MEROM BOM OPTION DUE TO PAGE 76 SHARING W/ M50

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-6447	1	BAR CODE LABLE, MLB, M51	[EEE:VMD]	CRITICAL	EEE_VMD
825-6447	1	BAR CODE LABLE, MLB, M51	[EEE:V4K]	CRITICAL	EEE_V4K

CHIPSET, ROMS, ETC.

	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
	511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
	338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
	343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
	359S0117	1	IC,SLG84435,CLK GEN,68PIN QFN	U3301	CRITICAL	
	338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(335S0382)	341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
	341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	TPM
	353S1465	1	IC,CPU VREG,IMVP,TWO PHASE,SCREENED	U7500	CRITICAL	
	341S1892	1	IC,2K I2C EEPROM,MXM,M51	U8570	CRITICAL	MXM_ROM
(335S0384)	341T0019	1	IC,EFI BOOT ROM,M51	U6301	CRITICAL	
(338S0274)	341T0020	1	IC,SMC,M51	U5800	CRITICAL	

PROCESSORS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3392	1	MEROM 2.33GHZ, M51	CPU	CRITICAL	M51_BEST
337S3390	1	MEROM 2.16GHZ, M51	CPU	CRITICAL	M51_BETTER

Misc. Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	NOSTUFF
820-2038	1	IO ALIGNMENT BOARD, M51	PCB2	CRITICAL	
946-0743	1	IO ALIGNMENT BOARD ADHESIVE	ADH1	CRITICAL	
378S0193	1	LED,WHITE,740MCD,LF,3X2MM	LED5950	CRITICAL	

BATTERY IS INSTALLED AT FATP

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0086	126S0078		ALL	Sanyo alt for Nich.
126S0099	126S0073		ALL	Sanyo alt for Nich.
126S0068	126S0088		ALL	Sanyo alt for Nich.
124-0361	124-0339		ALL	SANYO ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0141	378S0140		ALL	GREEN LED ALT.
353S1461	353S1465		U7500	CPU VREG NEW REV
740S0044	740S0028		F9710	DVI DDC (LITTLEFUSE)

SENSOR STUFFING OPTIONS

MUST STUFF WHEN SYS_PWR_SENSE IS NOT STUFFED (I.E. WHEN DEVELOPMENT BOM IS NOT STUFFED)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
102S0699	1	RES,0-OHM,2010	R7650	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C7650	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C7650	PRODUCTION

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN MXM_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
107S0070	1	RES,0-OHM,2512	R8450	NOSTUFF
116S0090	1	RES,10K-OHM,5%,0402	C8458	NOSTUFF
116S0090	1	RES,10K-OHM,5%,0402	C8459	NOSTUFF

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN CPU_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0090	1	RES,10K-OHM,5%,0402	C7602	NOSTUFF
116S0090	1	RES,10K-OHM,5%,0402	C7612	NOSTUFF

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

BOM Config

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A

SCALE NONE SHT 4 OF 97

LAYOUT: PLACE CLOSE TO DESTINATION
* OPPOSITE END FROM CLOCK BUFFER

34 21 SB_CLK100M_SATA_P PP6C4 PP OMIT P4MM
34 21 SB_CLK100M_SATA_N PP6C5 PP OMIT P4MM

34 23 SB_CLK14P3M_TIMER PP6D9 PP OMIT P4MM
34 23 SB_CLK48M_USBCTLR PP6E0 PP OMIT P4MM

34 22 PCI_CLK_SB PP6D0 PP OMIT P4MM
44 34 PCI_CLK_FW PP626 PP OMIT P4MM
58 34 PCI_CLK_SMC PP627 PP OMIT P4MM

LAYOUT NOTE: PLACE NEAR SOUTHBRIDGE

38 21 IDE_PDIOR_L PP6C6 PP OMIT P4MM
38 21 IDE_PDIORDY PP6C7 PP OMIT P4MM
38 21 IDE_PDD<9> PP6C8 PP OMIT P4MM

54 22 PCIE_B_D2R_P PP600 PP OMIT P4MM
54 22 PCIE_B_D2R_N PP601 PP OMIT P4MM
22 14 DMI_N2S_P<0> PP6D3 PP OMIT P4MM
22 14 DMI_N2S_N<0> PP6D4 PP OMIT P4MM

67 60 58 21 5 LPC_FRAME_L PP6D8 PP OMIT P4MM

63 58 22 SPI_SO PP612 PP OMIT P4MM
63 58 22 SPI_SI PP613 PP OMIT P4MM

ALL I2C BUSSES (PLACE IN ACCESSIBLE LOCATION TOP SIDE)

27 SMBUS_SB_SCL PP604 PP OMIT P4MM
27 SMBUS_SB_SDA PP605 PP OMIT P4MM

27 SMBUS_SMC_A_S3_SCL PP610 PP OMIT P4MM
27 SMBUS_SMC_A_S3_SDA PP611 PP OMIT P4MM

FSB SIGNALS

12 11 7 FSB_CPURST_L PP621 PP OMIT P4MM

LAYOUT NOTE: PLACE NEAR NORTHBRIDGE

75 26 14 5 VR_PWRGOOD_DELAY PP665 PP OMIT P4MM
14 NB_RST_IN_L_R PP666 PP OMIT P4MM

22 14 DMI_S2N_N<0> PP673 PP OMIT P4MM
22 14 DMI_S2N_P<0> PP674 PP OMIT P4MM

19 14 MEM_VREF_NB_0 PP6E1 PP OMIT P4MM
19 14 MEM_VREF_NB_1 PP675 PP OMIT P4MM

I473
14 NB_CFG<17> — NC_NB_CFG<17> MAKE_BASE=TRUE
I474
14 NB_CFG<15> — NC_NB_CFG<15> MAKE_BASE=TRUE
I475
14 NB_CFG<14> — NC_NB_CFG<14> MAKE_BASE=TRUE
I476
14 NB_CFG<13> — NC_NB_CFG<13> MAKE_BASE=TRUE
I477
14 NB_CFG<12> — NC_NB_CFG<12> MAKE_BASE=TRUE
I478
14 NB_CFG<11> — NC_NB_CFG<11> MAKE_BASE=TRUE
I479
14 NB_CFG<10> — NC_NB_CFG<10> MAKE_BASE=TRUE
I481
14 NB_CFG<8> — NC_NB_CFG<8> MAKE_BASE=TRUE
I480
14 NB_CFG<6> — NC_NB_CFG<6> MAKE_BASE=TRUE
I482
14 NB_CFG<4> — NC_NB_CFG<4> MAKE_BASE=TRUE
I483
14 NB_CFG<3> — NC_NB_CFG<3> MAKE_BASE=TRUE

I513
22 PCI_GNT3_L — TP_PCI_GNT3_L MAKE_BASE=TRUE

SPARE USB PORT
22 USB_F_N — TP_USB_F_N MAKE_BASE=TRUE
22 USB_F_P — TP_USB_F_P MAKE_BASE=TRUE

INVERTER DOES NOT USE THIS SIGNAL
19 13 LVDS_BKLTEN — TP_LVDS_BKLTEN MAKE_BASE=TRUE

68 IN NC_AUD_BI_PORT_G_L NO_TEST=TRUE
59 IN NC_ALS_GAIN NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_C NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_D NO_TEST=TRUE
59 IN NC_SMC_BATT_CHG_EN NO_TEST=TRUE
59 IN NC_SMC_BATT_ISET NO_TEST=TRUE
59 IN NC_SMC_BATT_TRICKLE_EN_L NO_TEST=TRUE
59 IN NC_SMC_BATT_VSET NO_TEST=TRUE
59 IN NC_SMC_P20 NO_TEST=TRUE
59 IN NC_SMC_P21 NO_TEST=TRUE
59 IN NC_SMC_P22 NO_TEST=TRUE
59 IN NC_SMC_P23 NO_TEST=TRUE
59 IN NC_SMC_P26 NO_TEST=TRUE
59 IN NC_SMC_P27 NO_TEST=TRUE
59 IN NC_SMC_SYS_ISET NO_TEST=TRUE
59 IN NC_SMC_SYS_VSET NO_TEST=TRUE
59 IN NC_SMS_X_AXIS NO_TEST=TRUE
59 IN NC_SMS_Y_AXIS NO_TEST=TRUE
59 IN NC_SMS_Z_AXIS NO_TEST=TRUE

73 IN NC_J7302_3 NO_TEST=TRUE
73 IN NC_J7302_6 NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_R NO_TEST=TRUE
59 IN NC_SMC_MEM_ISENSE NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_R NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_B NO_TEST=TRUE

29 IN TP_MEM_B_A<15> NO_TEST=TRUE
29 IN TP_MEM_B_A<14> NO_TEST=TRUE

84 13 IN PEG_R2D_C_N<0> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<0> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<1> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<1> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<2> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<2> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<3> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<3> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<4> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<4> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<5> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<5> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<6> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<6> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<7> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<7> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<8> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<8> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<9> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<9> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<10> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<10> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<11> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<11> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<12> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<12> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<13> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<13> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<14> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<14> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<15> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<15> NO_TEST=TRUE

84 13 IN PEG_R2D_N<0> NO_TEST=TRUE
84 13 IN PEG_R2D_P<0> NO_TEST=TRUE
84 13 IN PEG_R2D_N<1> NO_TEST=TRUE
84 13 IN PEG_R2D_P<1> NO_TEST=TRUE
84 13 IN PEG_R2D_N<2> NO_TEST=TRUE
84 13 IN PEG_R2D_P<2> NO_TEST=TRUE
84 13 IN PEG_R2D_N<3> NO_TEST=TRUE
84 13 IN PEG_R2D_P<3> NO_TEST=TRUE
84 13 IN PEG_R2D_N<4> NO_TEST=TRUE
84 13 IN PEG_R2D_P<4> NO_TEST=TRUE
84 13 IN PEG_R2D_N<5> NO_TEST=TRUE
84 13 IN PEG_R2D_P<5> NO_TEST=TRUE
84 13 IN PEG_R2D_N<6> NO_TEST=TRUE
84 13 IN PEG_R2D_P<6> NO_TEST=TRUE
84 13 IN PEG_R2D_N<7> NO_TEST=TRUE
84 13 IN PEG_R2D_P<7> NO_TEST=TRUE
84 13 IN PEG_R2D_N<8> NO_TEST=TRUE
84 13 IN PEG_R2D_P<8> NO_TEST=TRUE
84 13 IN PEG_R2D_N<9> NO_TEST=TRUE
84 13 IN PEG_R2D_P<9> NO_TEST=TRUE
84 13 IN PEG_R2D_N<10> NO_TEST=TRUE
84 13 IN PEG_R2D_P<10> NO_TEST=TRUE
84 13 IN PEG_R2D_N<11> NO_TEST=TRUE
84 13 IN PEG_R2D_P<11> NO_TEST=TRUE
84 13 IN PEG_R2D_N<12> NO_TEST=TRUE
84 13 IN PEG_R2D_P<12> NO_TEST=TRUE
84 13 IN PEG_R2D_N<13> NO_TEST=TRUE
84 13 IN PEG_R2D_P<13> NO_TEST=TRUE
84 13 IN PEG_R2D_N<14> NO_TEST=TRUE
84 13 IN PEG_R2D_P<14> NO_TEST=TRUE
84 13 IN PEG_R2D_N<15> NO_TEST=TRUE
84 13 IN PEG_R2D_P<15> NO_TEST=TRUE

84 13 IN PEG_D2R_N<0> NO_TEST=TRUE
84 13 IN PEG_D2R_P<0> NO_TEST=TRUE
84 13 IN PEG_D2R_N<1> NO_TEST=TRUE
84 13 IN PEG_D2R_P<1> NO_TEST=TRUE
84 13 IN PEG_D2R_N<2> NO_TEST=TRUE
84 13 IN PEG_D2R_P<2> NO_TEST=TRUE
84 13 IN PEG_D2R_N<3> NO_TEST=TRUE
84 13 IN PEG_D2R_P<3> NO_TEST=TRUE
84 13 IN PEG_D2R_N<4> NO_TEST=TRUE
84 13 IN PEG_D2R_P<4> NO_TEST=TRUE
84 13 IN PEG_D2R_N<5> NO_TEST=TRUE
84 13 IN PEG_D2R_P<5> NO_TEST=TRUE
84 13 IN PEG_D2R_N<6> NO_TEST=TRUE
84 13 IN PEG_D2R_P<6> NO_TEST=TRUE
84 13 IN PEG_D2R_N<7> NO_TEST=TRUE
84 13 IN PEG_D2R_P<7> NO_TEST=TRUE
84 13 IN PEG_D2R_N<8> NO_TEST=TRUE
84 13 IN PEG_D2R_P<8> NO_TEST=TRUE
84 13 IN PEG_D2R_N<9> NO_TEST=TRUE
84 13 IN PEG_D2R_P<9> NO_TEST=TRUE
84 13 IN PEG_D2R_N<10> NO_TEST=TRUE
84 13 IN PEG_D2R_P<10> NO_TEST=TRUE
84 13 IN PEG_D2R_N<11> NO_TEST=TRUE
84 13 IN PEG_D2R_P<11> NO_TEST=TRUE
84 13 IN PEG_D2R_N<12> NO_TEST=TRUE
84 13 IN PEG_D2R_P<12> NO_TEST=TRUE
84 13 IN PEG_D2R_N<13> NO_TEST=TRUE
84 13 IN PEG_D2R_P<13> NO_TEST=TRUE
84 13 IN PEG_D2R_N<14> NO_TEST=TRUE
84 13 IN PEG_D2R_P<14> NO_TEST=TRUE
84 13 IN PEG_D2R_N<15> NO_TEST=TRUE
84 13 IN PEG_D2R_P<15> NO_TEST=TRUE

76 75 3 IN PPVCORE_CPU FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 5 3 3 IN PP3V3_S5 FUNC_TEST=TRUE
83 78 3 IN PP2V5_S5 FUNC_TEST=TRUE
83 79 3 IN PP1V8_S3 FUNC_TEST=TRUE
79 3 IN PP1V2_S3 FUNC_TEST=TRUE
80 3 IN PP1V5_S0 FUNC_TEST=TRUE
80 34 3 IN PP1V05_S0 FUNC_TEST=TRUE
83 82 80 79 78 77 75 59 5 3 IN PP5V_S5 FUNC_TEST=TRUE
97 83 75 59 3 IN PP5V_S0 FUNC_TEST=TRUE
83 82 80 79 78 77 75 59 5 3 IN PP5V_S5 FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 5 3 3 IN PP3V3_S5 FUNC_TEST=TRUE
84 83 76 45 41 27 26 10 6 3 IN PP3V3_S0 FUNC_TEST=TRUE
83 3 IN PP24V_S0 FUNC_TEST=TRUE

11 7 IN XDP_BPM_L<3> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<2> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<1> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<0> FUNC_TEST=TRUE
26 11 7 IN XDP_DBRESET_L FUNC_TEST=TRUE
26 5 IN SW_RST_BTN_L FUNC_TEST=TRUE
59 5 IN POWER_BUTTON_L FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<0> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<1> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<2> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<3> FUNC_TEST=TRUE
67 60 58 21 5 IN LPC_FRAME_L FUNC_TEST=TRUE
67 60 58 23 IN PM_CLKRUN_L FUNC_TEST=TRUE
60 58 22 IN BOOT_LPC_SPI_L FUNC_TEST=TRUE
60 6 IN DEBUG_RST_L FUNC_TEST=TRUE
60 6 IN FWH_INIT_L FUNC_TEST=TRUE
60 59 21 IN PCI_CLK_PORT80 FUNC_TEST=TRUE
60 34 IN INT_SERIRQ FUNC_TEST=TRUE
67 60 58 23 IN PM_SUS_STAT_L FUNC_TEST=TRUE
67 60 58 23 IN SMC_MD1 FUNC_TEST=TRUE
60 58 IN SMC_RST_L FUNC_TEST=TRUE
60 59 58 IN SMC_NMI FUNC_TEST=TRUE
60 58 IN SV_SET_UP FUNC_TEST=TRUE
60 23 IN ISENSE_CAL_EN FUNC_TEST=TRUE
76 58 IN INV_ENABLE_BL FUNC_TEST=TRUE
94 85 IN LCD_PWM FUNC_TEST=TRUE
94 IN CPU_VID<0> FUNC_TEST=TRUE
75 8 IN CPU_VID<1> FUNC_TEST=TRUE
75 8 IN CPU_VID<2> FUNC_TEST=TRUE
75 8 IN CPU_VID<3> FUNC_TEST=TRUE
75 8 IN CPU_VID<4> FUNC_TEST=TRUE
75 8 IN CPU_VID<5> FUNC_TEST=TRUE
75 8 IN CPU_VID<6> FUNC_TEST=TRUE
75 23 14 IN PM_DPRSLPVR FUNC_TEST=TRUE
75 21 7 IN CPU_DPRSTP_L FUNC_TEST=TRUE
75 26 14 5 IN VR_PWRGOOD_DELAY FUNC_TEST=TRUE
26 23 IN VR_PWRGD_CK410 FUNC_TEST=TRUE
84 77 58 26 IN ALL_SYS_PWRGD FUNC_TEST=TRUE
77 58 23 IN PM_SLP_S4_L FUNC_TEST=TRUE
80 79 77 58 23 IN PM_SLP_S3_L FUNC_TEST=TRUE

60 59 58 IN SMC_TCK FUNC_TEST=TRUE
60 59 58 IN SMC_TDI FUNC_TEST=TRUE
60 59 58 IN SMC_TDO FUNC_TEST=TRUE
60 59 58 IN SMC_TMS FUNC_TEST=TRUE
60 58 IN SMC_TRST_L FUNC_TEST=TRUE
60 59 58 IN SMC_TX_L FUNC_TEST=TRUE
60 59 58 IN SMC_RX_L FUNC_TEST=TRUE
59 IN SMC_MANUAL_RST_L FUNC_TEST=TRUE
11 7 IN XDP_TCK FUNC_TEST=TRUE
11 7 IN XDP_TDI FUNC_TEST=TRUE
11 7 IN XDP_TDO FUNC_TEST=TRUE
11 7 IN XDP_TMS FUNC_TEST=TRUE
11 7 IN XDP_TRST_L FUNC_TEST=TRUE
59 5 IN POWER_BUTTON_L FUNC_TEST=TRUE
26 5 IN SW_RST_BTN_L FUNC_TEST=TRUE
10 IN NB_TSENS_HS_DXP FUNC_TEST=TRUE
10 IN NB_TSENS_HS_DXN FUNC_TEST=TRUE
34 11 IN CPU_XDP_CLK_N FUNC_TEST=TRUE
34 11 IN CPU_XDP_CLK_P FUNC_TEST=TRUE
11 IN ITPRESET_L FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<5> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<4> FUNC_TEST=TRUE

MISC GROUND VIAS

ZH500 HOLE-VIA 1
ZH510 HOLE-VIA 1
ZH520 HOLE-VIA 1
ZH501 HOLE-VIA 1
ZH511 HOLE-VIA 1
ZH521 HOLE-VIA 1
ZH502 HOLE-VIA 1
ZH512 HOLE-VIA 1
ZH522 HOLE-VIA 1
ZH503 HOLE-VIA 1
ZH513 HOLE-VIA 1
ZH523 HOLE-VIA 1
ZH504 HOLE-VIA 1
ZH514 HOLE-VIA 1
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ZH505 HOLE-VIA 1
ZH515 HOLE-VIA 1
ZH525 HOLE-VIA 1
ZH506 HOLE-VIA 1
ZH516 HOLE-VIA 1
ZH526 HOLE-VIA 1
ZH507 HOLE-VIA 1
ZH517 HOLE-VIA 1
ZH527 HOLE-VIA 1
ZH508 HOLE-VIA 1
ZH518 HOLE-VIA 1
ZH528 HOLE-VIA 1
ZH509 HOLE-VIA 1
ZH519 HOLE-VIA 1
ZH529 HOLE-VIA 1

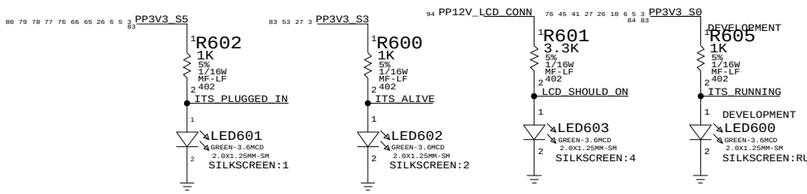
FUNC TEST 1 OF 2

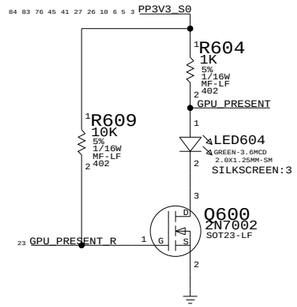
SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

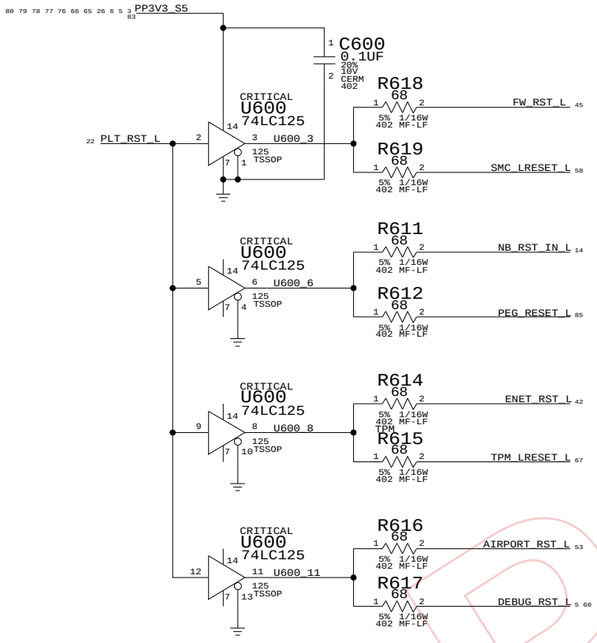
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 5 OF 97	

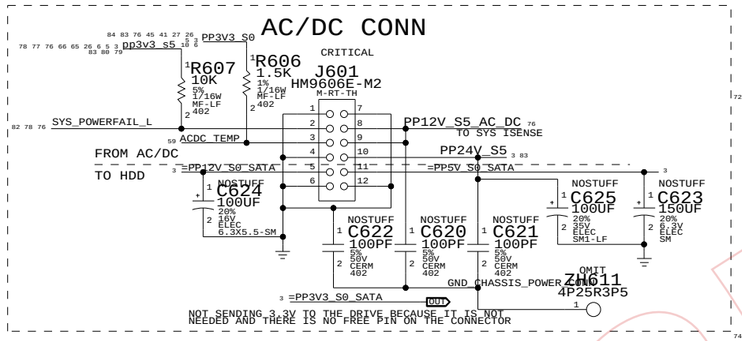
SYSTEM STATUS



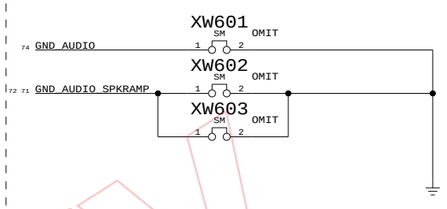




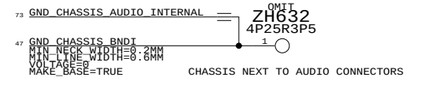
AC/DC CONN

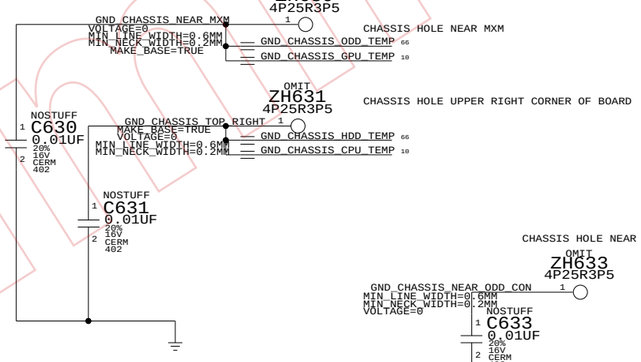


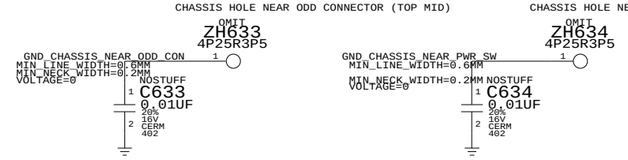
GND RAILS



CHASSIS GND

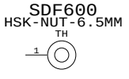


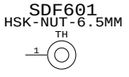




HEATSINK BACKER PLATE STANDOFFS

LOCATED NORTH OF CPU



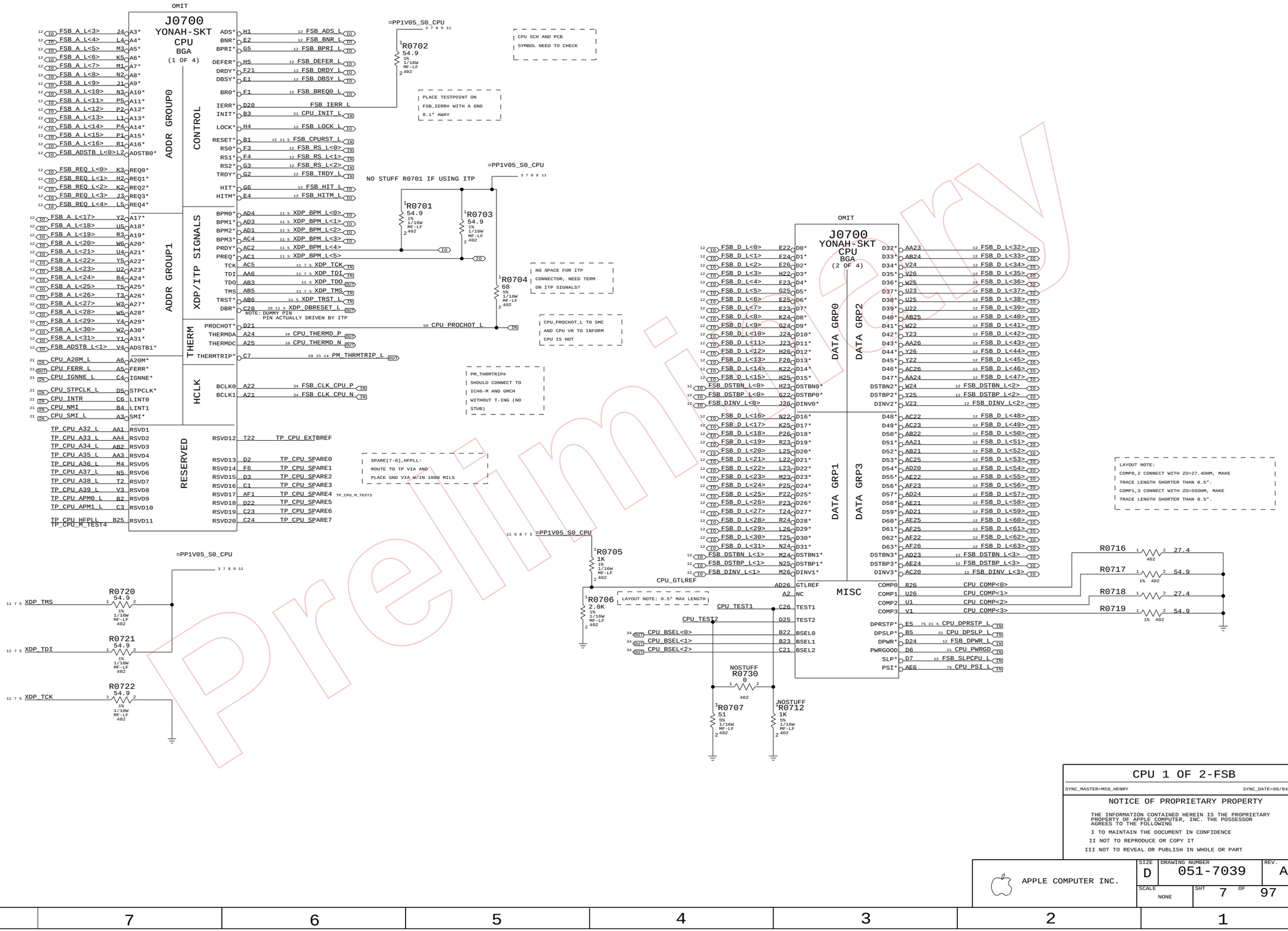


POWER CONN / MISC

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 6 OF 97	


OMIT
J0700
YONAH-SKT
CPU
BGA
(1 OF 4)
ADDR GROUP0
ADDR GROUP1
CONTROL
XDP/ITP SIGNALS
THERM
HCLK
RESERVED
FSB_A_L<3> J4 A3*
FSB_A_L<4> L4 A4*
FSB_A_L<5> M3 A5*
FSB_A_L<6> K5 A6*
FSB_A_L<7> M1 A7*
FSB_A_L<8> N2 A8*
FSB_A_L<9> J1 A9*
FSB_A_L<10> N3 A10*
FSB_A_L<11> P5 A11*
FSB_A_L<12> P2 A12*
FSB_A_L<13> L1 A13*
FSB_A_L<14> P4 A14*
FSB_A_L<15> P1 A15*
FSB_A_L<16> R1 A16*
FSB_ADSTB_L<0> L2 ADSTB0*
FSB_REQ_L<0> K3 REQ0*
FSB_REQ_L<1> H2 REQ1*
FSB_REQ_L<2> K2 REQ2*
FSB_REQ_L<3> J3 REQ3*
FSB_REQ_L<4> L5 REQ4*
FSB_A_L<17> Y2 A17*
FSB_A_L<18> U5 A18*
FSB_A_L<19> R3 A19*
FSB_A_L<20> W6 A20*
FSB_A_L<21> U4 A21*
FSB_A_L<22> Y5 A22*
FSB_A_L<23> U2 A23*
FSB_A_L<24> R4 A24*
FSB_A_L<25> T5 A25*
FSB_A_L<26> T3 A26*
FSB_A_L<27> W3 A27*
FSB_A_L<28> W5 A28*
FSB_A_L<29> Y4 A29*
FSB_A_L<30> W2 A30*
FSB_A_L<31> Y1 A31*
FSB_ADSTB_L<1> V4 ADSTB1*
CPU_A20M_L A6 A20M*
CPU_FERR_L A5 FERR*
CPU_IGNNE_L C4 IGNNE*
CPU_STPCLK_L D5 STPCLK*
CPU_INTR C6 LINT0
CPU_NMI B4 LINT1
CPU_SMI_L A3 SMI*
TP_CPU_A32_L AA1 RSVD1
TP_CPU_A33_L AA4 RSVD2
TP_CPU_A34_L AB2 RSVD3
TP_CPU_A35_L AA3 RSVD4
TP_CPU_A36_L M4 RSVD5
TP_CPU_A37_L N5 RSVD6
TP_CPU_A38_L T2 RSVD7
TP_CPU_A39_L V3 RSVD8
TP_CPU_APM0_L B2 RSVD9
TP_CPU_APM1_L C3 RSVD10
TP_CPU_HFPLL B25 RSVD11
TP_CPU_M_TEST4
ADS* H1 FSB_ADS_L
BNR* E2 FSB_BNR_L
BPRI* G5 FSB_BPRI_L
DEFER* H5 FSB_DEFER_L
DRDY* F21 FSB_DRDY_L
DBSY* E1 FSB_DBSY_L
BR0* F1 FSB_BREQ0_L
IERR* D20 FSB_IERR_L
INIT* B3 CPU_INIT_L
LOCK* H4 FSB_LOCK_L
RESET* B1 FSB_CPURST_L
RS0* F3 FSB_RS_L<0>
RS1* F4 FSB_RS_L<1>
RS2* G3 FSB_RS_L<2>
TRDY* G2 FSB_TRDY_L
HIT* G6 FSB_HIT_L
HITM* E4 FSB_HITM_L
BPM0* AD4 XDP_BPM_L<0>
BPM1* AD3 XDP_BPM_L<1>
BPM2* AD1 XDP_BPM_L<2>
BPM3* AC4 XDP_BPM_L<3>
PRDY* AC2 XDP_BPM_L<4>
PREQ* AC1 XDP_BPM_L<5>
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST* AB6 XDP_TRST_L
DBR* C20 XDP_DBRESET_L
NOTE: DUMMY PIN
PIN ACTUALLY DRIVEN BY ITP
PROCHOT* D21 CPU_PROCHOT_L
THERMDA A24 CPU_THERMD_P
THERMDC A25 CPU_THERMD_N
THERMTRIP* C7 PM_THRMTRIP_L
BCLK0 A22 FSB_CLK_CPU_P
BCLK1 A21 FSB_CLK_CPU_N
RSVD12 T22 TP_CPU_EXTBREF
RSVD13 D2 TP_CPU_SPARE0
RSVD14 F6 TP_CPU_SPARE1
RSVD15 D3 TP_CPU_SPARE2
RSVD16 C1 TP_CPU_SPARE3
RSVD17 AF1 TP_CPU_SPARE4
RSVD18 D22 TP_CPU_SPARE5
RSVD19 C23 TP_CPU_SPARE6
RSVD20 C24 TP_CPU_SPARE7
TP_CPU_M_TEST3
=PP1V05_S0_CPU
R0702 54.9 1% 1/16W MF-LF 402
CPU SCH AND PCB SYMBOL NEED TO CHECK
PLACE TESTPOINT ON FSB_IERR# WITH A GND 0.1" AWAY
NO STUFF R0701 IF USING ITP
R0701 54.9 1% 1/16W MF-LF 402
R0703 54.9 1% 1/16W MF-LF 402
R0704 68 5% 1/16W MF-LF 402
NO SPACE FOR ITP CONNECTOR, NEED TERM ON ITP SIGNALS?
CPU_PROCHOT_L TO SMC AND CPU VR TO INFORM CPU IS HOT
PM_THRMTRIP# SHOULD CONNECT TO ICH6-M AND GMCH WITHOUT T-ING (NO STUB)
SPARE[7-0],HFPLL: ROUTE TO TP VIA AND PLACE GND VIA W/IN 1000 MILS
R0720 54.9 1% 1/16W MF-LF 402
R0721 54.9 1% 1/16W MF-LF 402
R0722 54.9 1% 1/16W MF-LF 402
R0705 1K 1% 1/16W MF-LF 402
R0706 2.0K 1% 1/16W MF-LF 402
LAYOUT NOTE: 0.5" MAX LENGTH
CPU_GTLREF
CPU_TEST1
CPU_TEST2
CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>
NOSTUFF R0730 0 402
R0707 51 5% 1/16W MF-LF 402
NOSTUFF R0712 1K 5% 1/16W MF-LF 402
OMIT
J0700
YONAH-SKT
CPU
BGA
(2 OF 4)
DATA GRP0
DATA GRP1
DATA GRP2
DATA GRP3
MISC
FSB_D_L<0> E22 D0*
FSB_D_L<1> F24 D1*
FSB_D_L<2> E26 D2*
FSB_D_L<3> H22 D3*
FSB_D_L<4> F23 D4*
FSB_D_L<5> G25 D5*
FSB_D_L<6> E25 D6*
FSB_D_L<7> E23 D7*
FSB_D_L<8> K24 D8*
FSB_D_L<9> G24 D9*
FSB_D_L<10> J24 D10*
FSB_D_L<11> J23 D11*
FSB_D_L<12> H26 D12*
FSB_D_L<13> F26 D13*
FSB_D_L<14> K22 D14*
FSB_D_L<15> H25 D15*
FSB_DSTBN_L<0> H23 DSTBN0*
FSB_DSTBP_L<0> G22 DSTBP0*
FSB_DINV_L<0> J26 DINV0*
FSB_D_L<16> N22 D16*
FSB_D_L<17> K25 D17*
FSB_D_L<18> P26 D18*
FSB_D_L<19> R23 D19*
FSB_D_L<20> L25 D20*
FSB_D_L<21> L22 D21*
FSB_D_L<22> L23 D22*
FSB_D_L<23> M23 D23*
FSB_D_L<24> P25 D24*
FSB_D_L<25> P22 D25*
FSB_D_L<26> P23 D26*
FSB_D_L<27> T24 D27*
FSB_D_L<28> R24 D28*
FSB_D_L<29> L26 D29*
FSB_D_L<30> T25 D30*
FSB_D_L<31> N24 D31*
FSB_DSTBN_L<1> M24 DSTBN1*
FSB_DSTBP_L<1> N25 DSTBP1*
FSB_DINV_L<1> M26 DINV1*
AD26 GTLREF
A2 NC
C26 TEST1
D25 TEST2
B22 BSEL0
B23 BSEL1
C21 BSEL2
D32* AA23 FSB_D_L<32>
D33* AB24 FSB_D_L<33>
D34* V24 FSB_D_L<34>
D35* V26 FSB_D_L<35>
D36* W25 FSB_D_L<36>
D37* U23 FSB_D_L<37>
D38* U25 FSB_D_L<38>
D39* U22 FSB_D_L<39>
D40* AB25 FSB_D_L<40>
D41* W22 FSB_D_L<41>
D42* Y23 FSB_D_L<42>
D43* AA26 FSB_D_L<43>
D44* Y26 FSB_D_L<44>
D45* Y22 FSB_D_L<45>
D46* AC26 FSB_D_L<46>
D47* AA24 FSB_D_L<47>
DSTBN2* W24 FSB_DSTBN_L<2>
DSTBP2* Y25 FSB_DSTBP_L<2>
DINV2* V23 FSB_DINV_L<2>
D48* AC22 FSB_D_L<48>
D49* AC23 FSB_D_L<49>
D50* AB22 FSB_D_L<50>
D51* AA21 FSB_D_L<51>
D52* AB21 FSB_D_L<52>
D53* AC25 FSB_D_L<53>
D54* AD20 FSB_D_L<54>
D55* AE22 FSB_D_L<55>
D56* AF23 FSB_D_L<56>
D57* AD24 FSB_D_L<57>
D58* AE21 FSB_D_L<58>
D59* AD21 FSB_D_L<59>
D60* AE25 FSB_D_L<60>
D61* AF25 FSB_D_L<61>
D62* AF22 FSB_D_L<62>
D63* AF26 FSB_D_L<63>
DSTBN3* AD23 FSB_DSTBN_L<3>
DSTBP3* AE24 FSB_DSTBP_L<3>
DINV3* AC20 FSB_DINV_L<3>
COMP0 R26 CPU_COMP<0>
COMP1 U26 CPU_COMP<1>
COMP2 U1 CPU_COMP<2>
COMP3 V1 CPU_COMP<3>
DPRSTP* E5 CPU_DPRSTP_L
DPSLP* B5 CPU_DPSLP_L
DPWR* D24 FSB_DPWR_L
PWRGOOD D6 CPU_PWRGD
SLP* D7 FSB_SLPCPU_L
PSI* AE6 CPU_PSI_L
R0716 27.4 402
R0717 54.9 1% 402
R0718 27.4 402
R0719 54.9 1% 402
LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
CPU 1 OF 2-FSB
SYNC_MASTER=M58_HENRY
SYNC_DATE=08/04/2006
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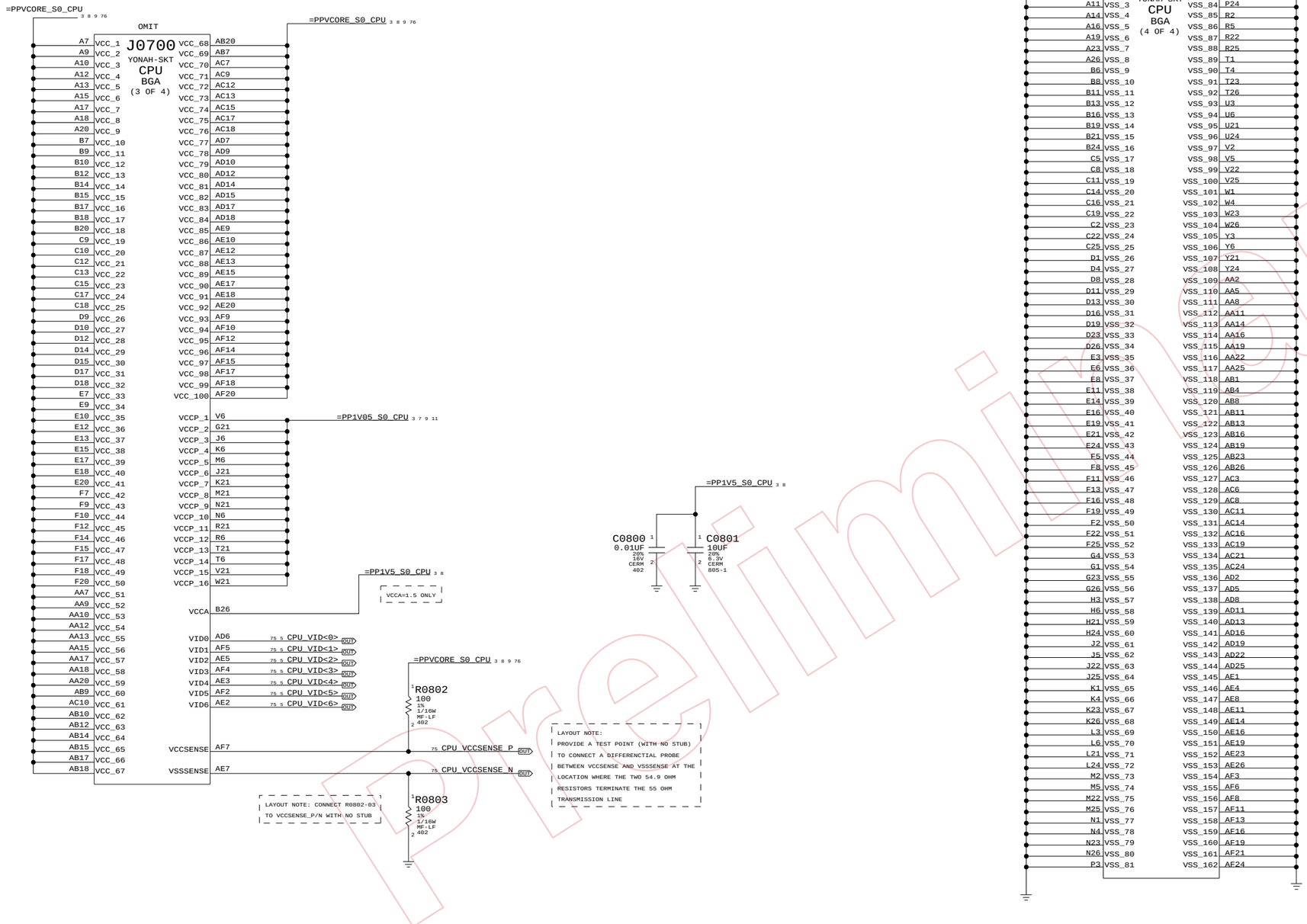
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7039
REV. A
SCALE NONE
SHT 7 OF 97



CPU 2 OF 2-PWR/GND

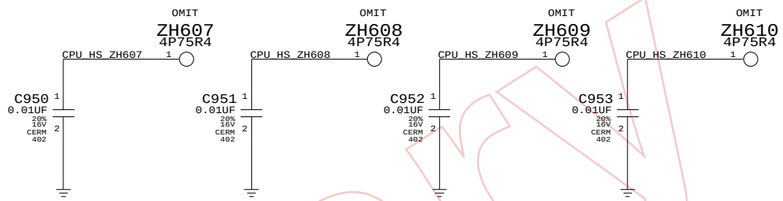
SYNC_MASTER=M59_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A

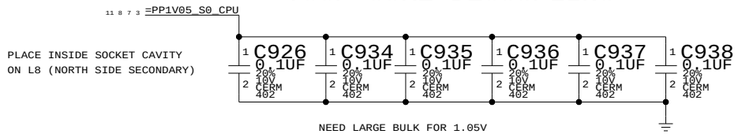
SCALE	SHT	OF
NONE	8	97

CPU HEATSINK MOUNTING HOLES

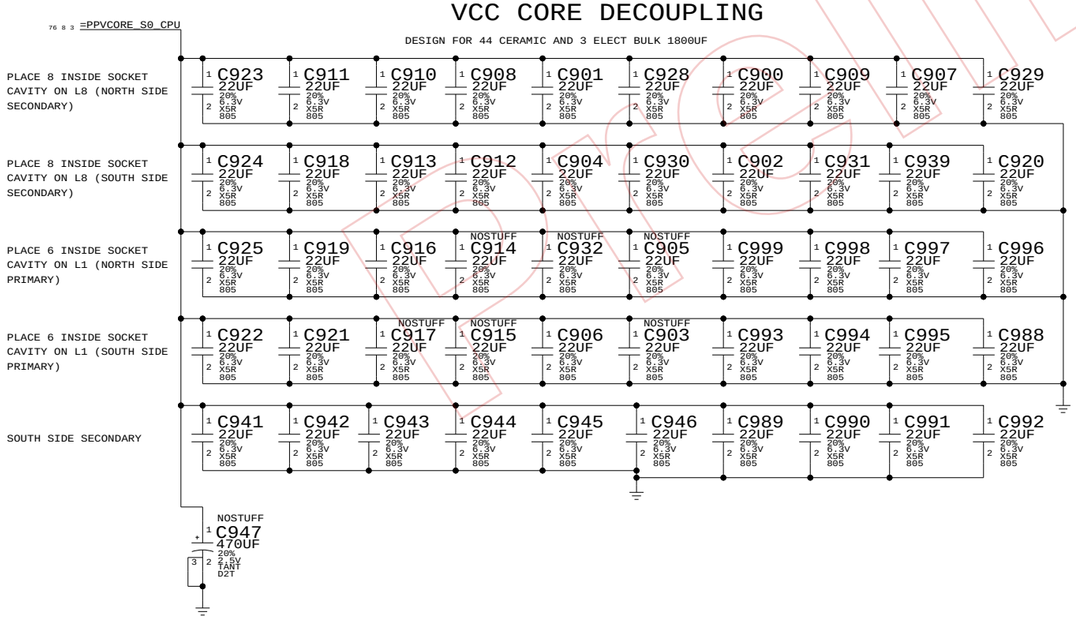


WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



VCC CORE DECOUPLING



CPU DECAPS & VID<>

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

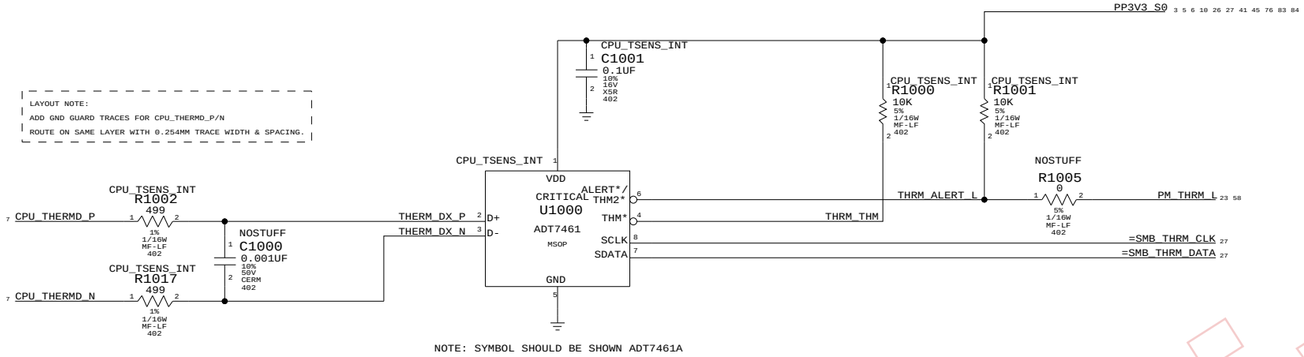
SIZE	DRAWING NUMBER	REV.
D	051-7039	A

SCALE	SHT	OF
NONE	9	97

CPU INTERNAL DIODE THERMAL SENSOR

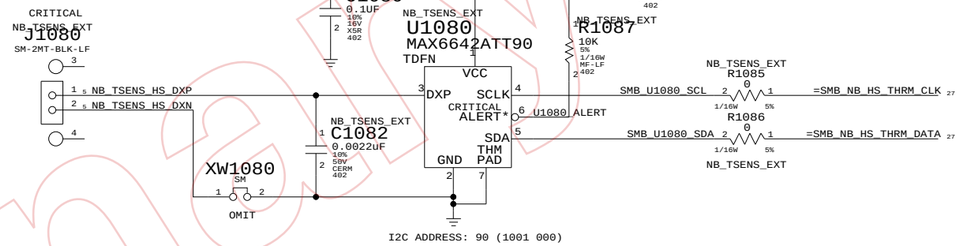
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACES FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



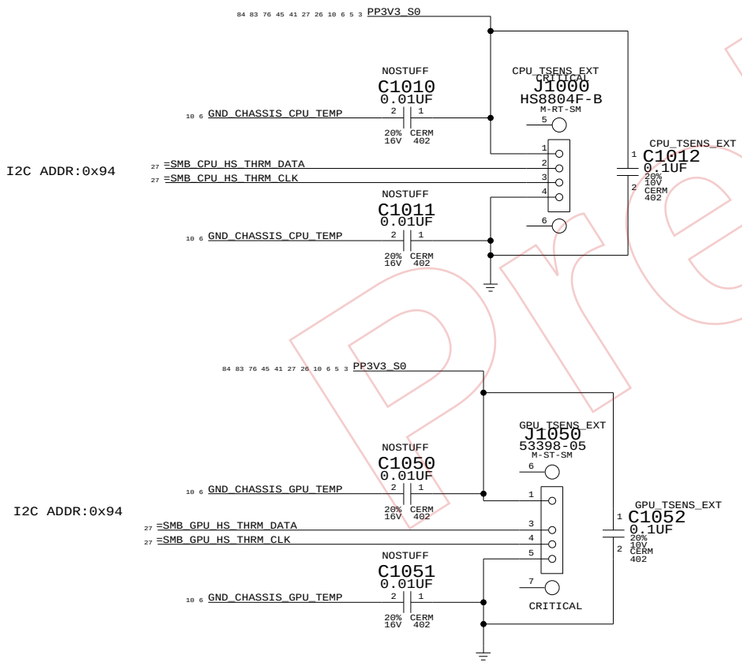
NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

NB HEATSINK TEMPERATURE SENSE

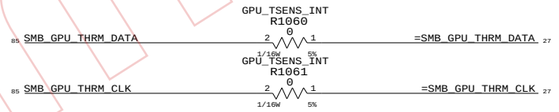


I2C ADDRESS: 90 (1001 000)

CPU AND GPU REMOTE HEATSINK THERMAL SENSORS

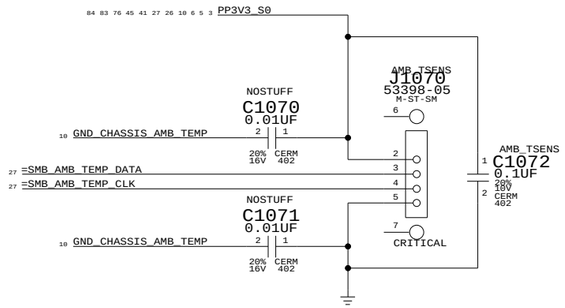


MXM CARD TEMPERATURE SENSOR (GPU INTERNAL DIODE)



NOTE: I2C ADDR:98(1001 100) ON NVIDIA CARD
MAY NOT BE CONSISTENT WITH OTHER CARDS

AMBIENT TEMPERATURE (CPU FAN INTAKE) SENSOR



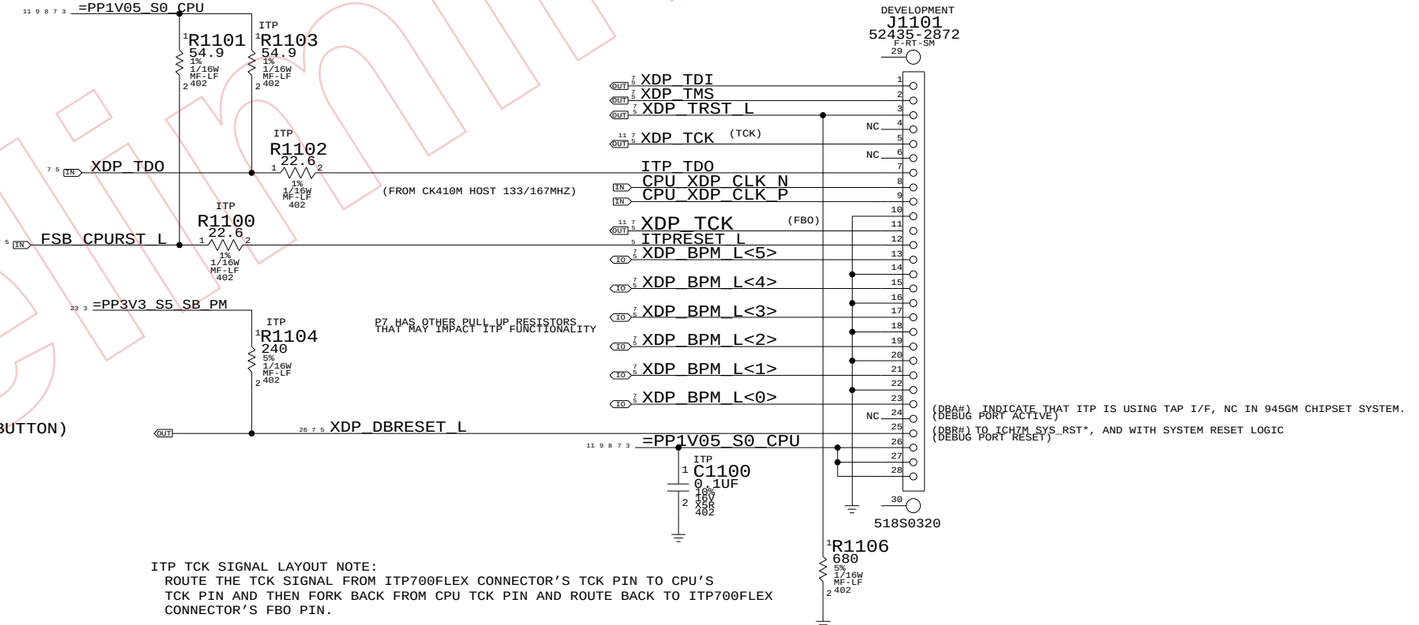
ASIC TEMP SENSORS

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 10 OF 97	

CPU ITP700FLEX DEBUG SUPPORT



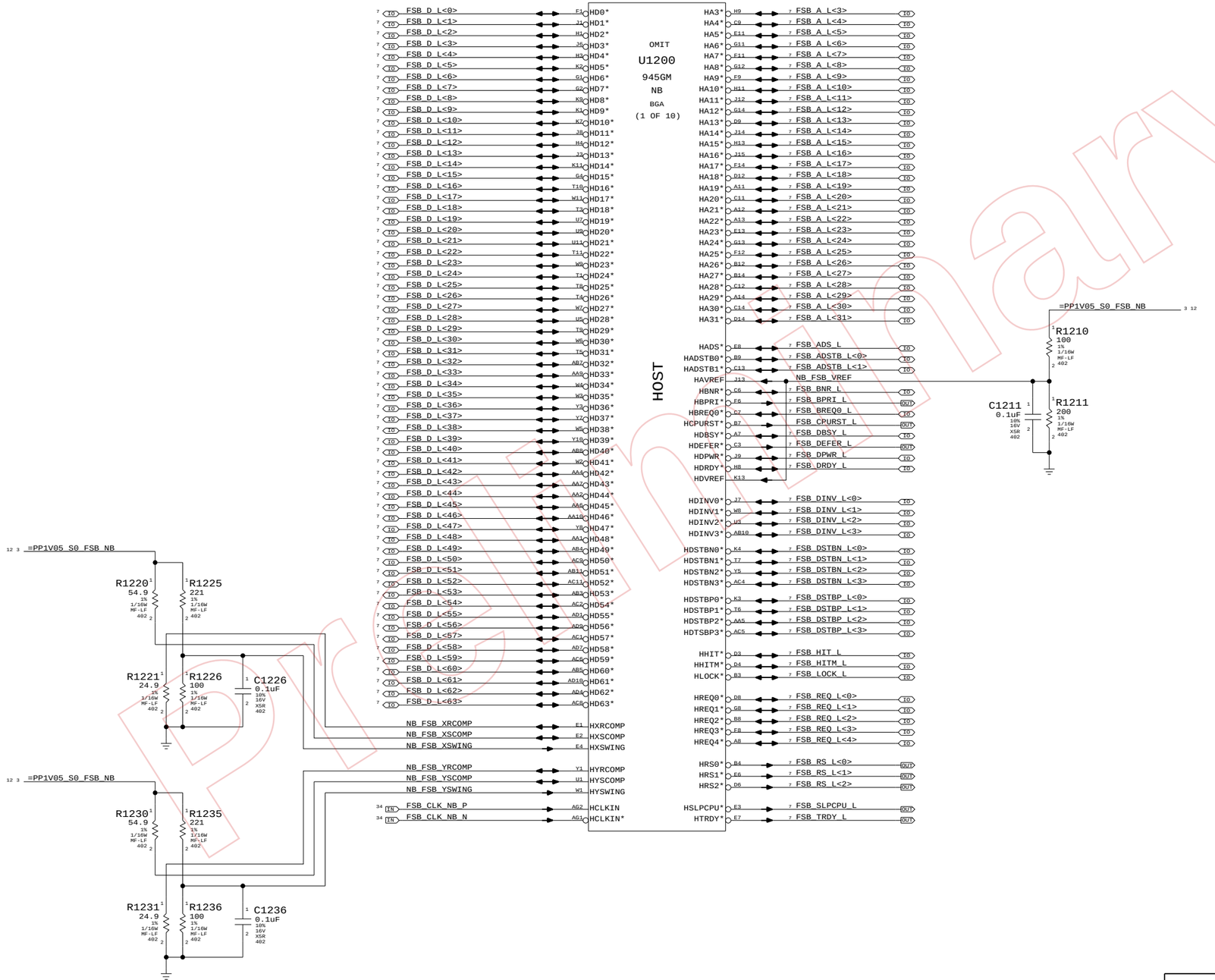
ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 11 OF 97	



NB CPU Interface

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 12 OF 97	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

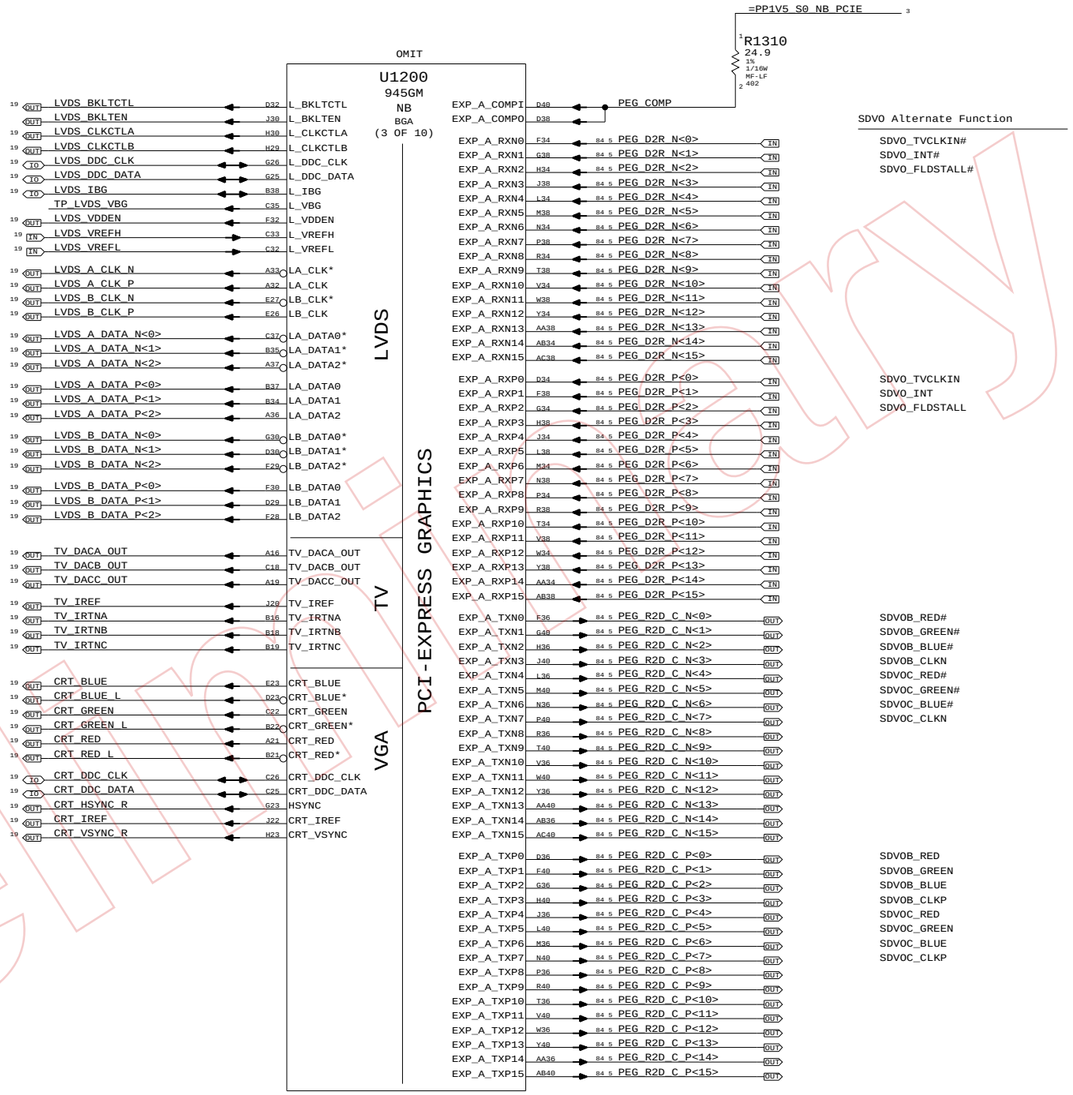
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

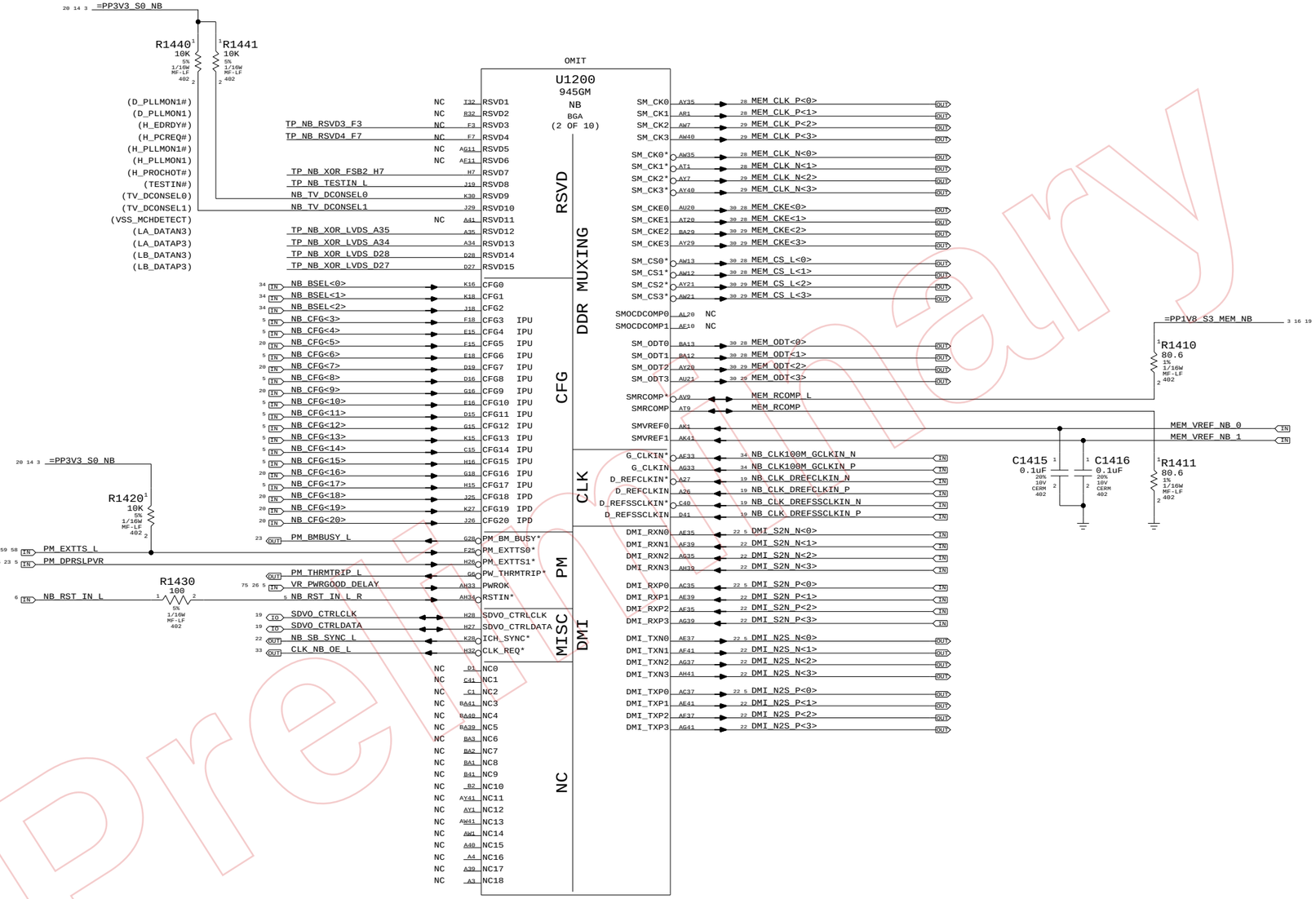


NB PEG / Video Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 13 OF 97	

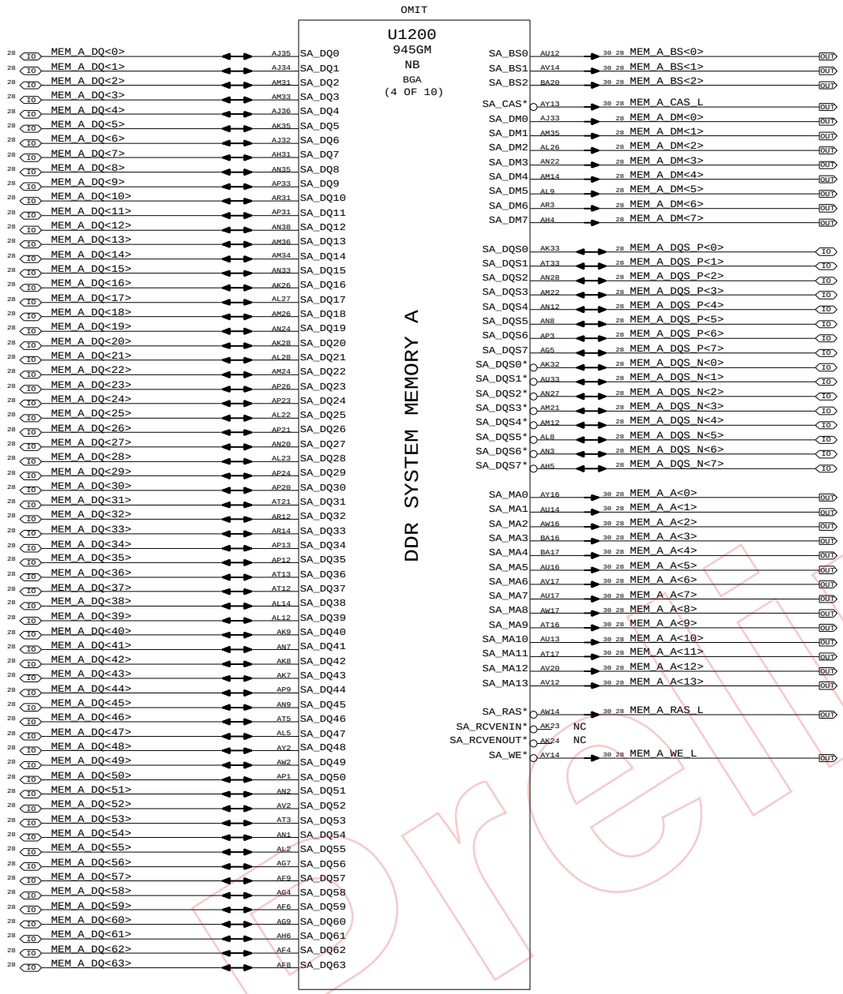


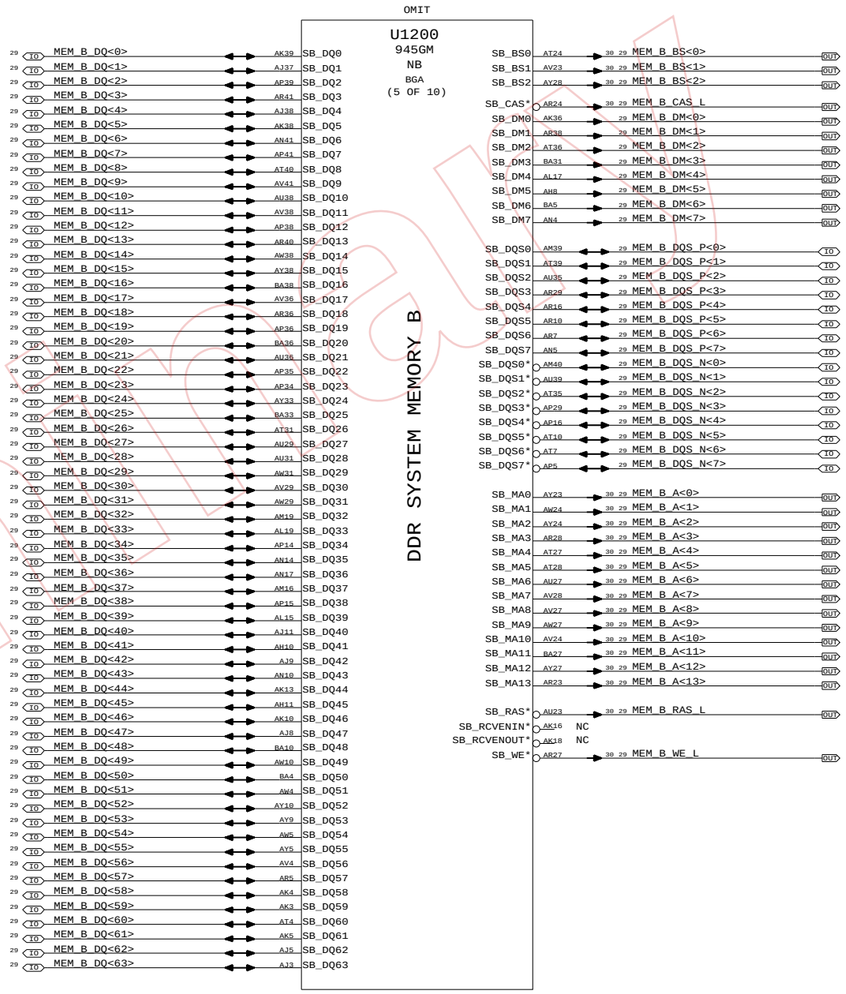
NB Misc Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 14 OF 97	





NB DDR2 Interfaces

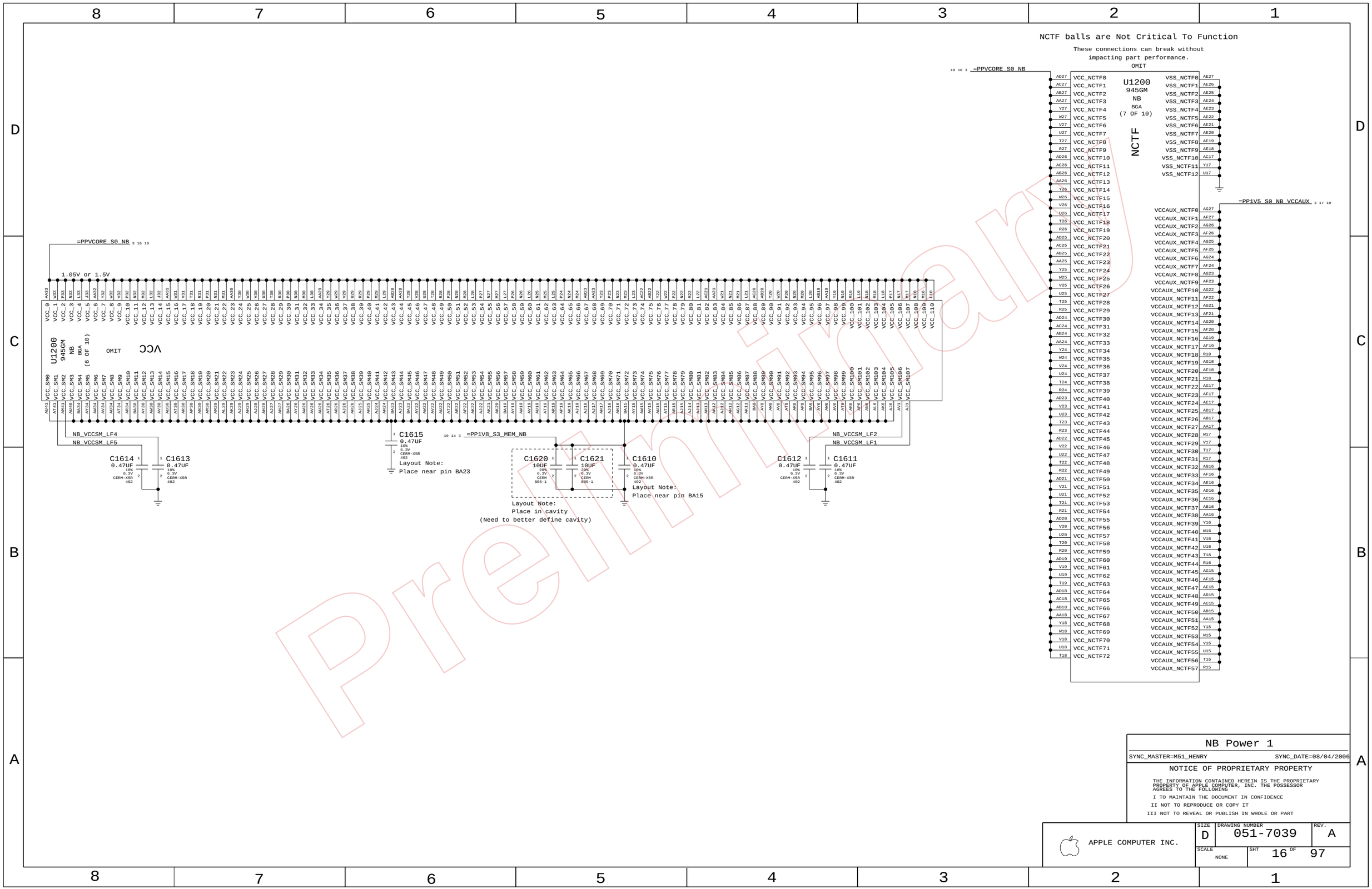
SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A

SCALE: NONE

SHT 15 OF 97



NB Power 1

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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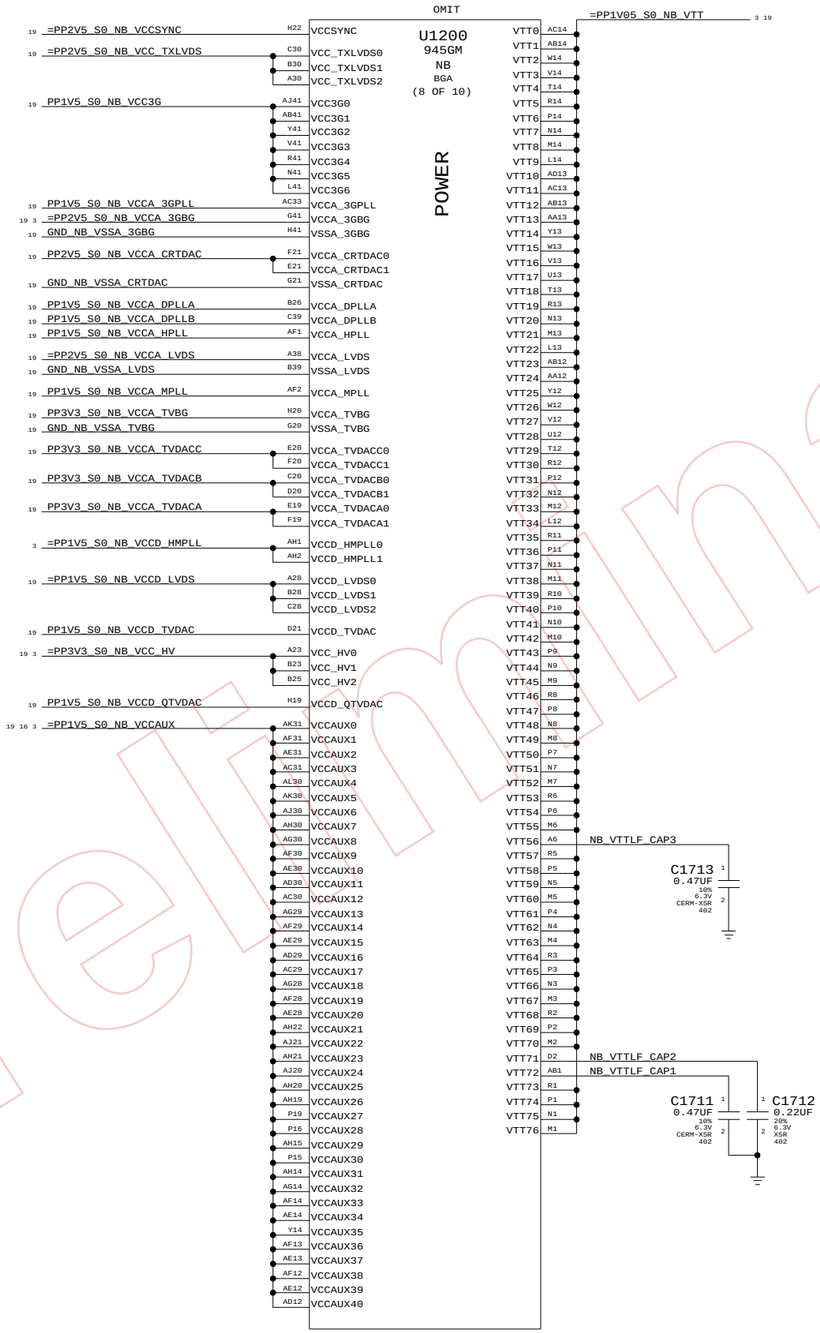
SIZE	DRAWING NUMBER	REV.
D	051-7039	A

SCALE NONE SHT 16 OF 97

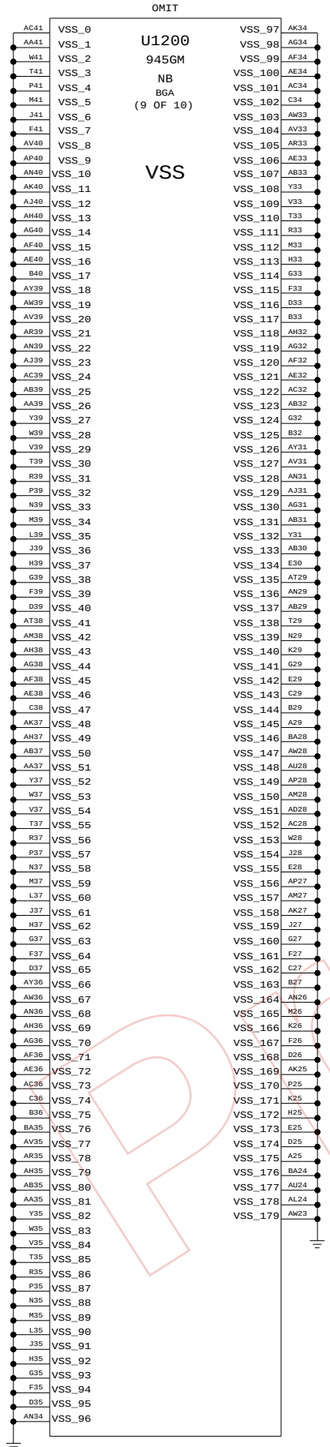


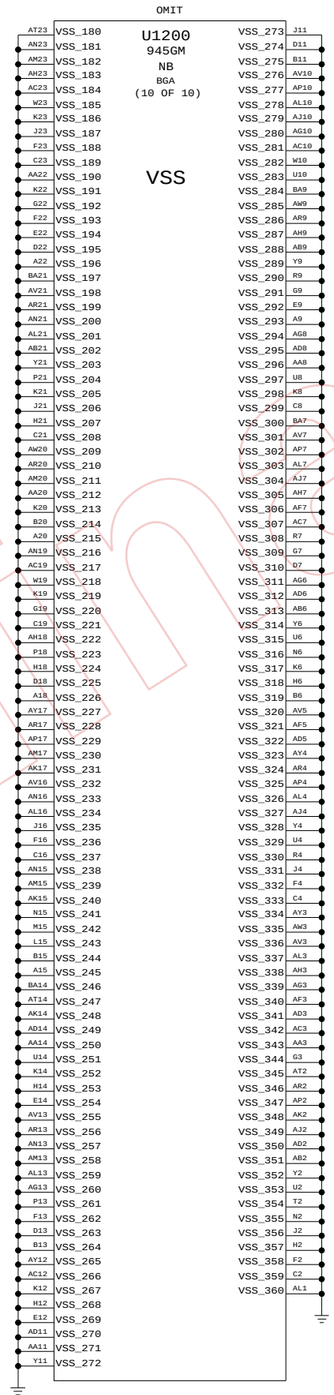
NB Power 2

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 17 OF 97	



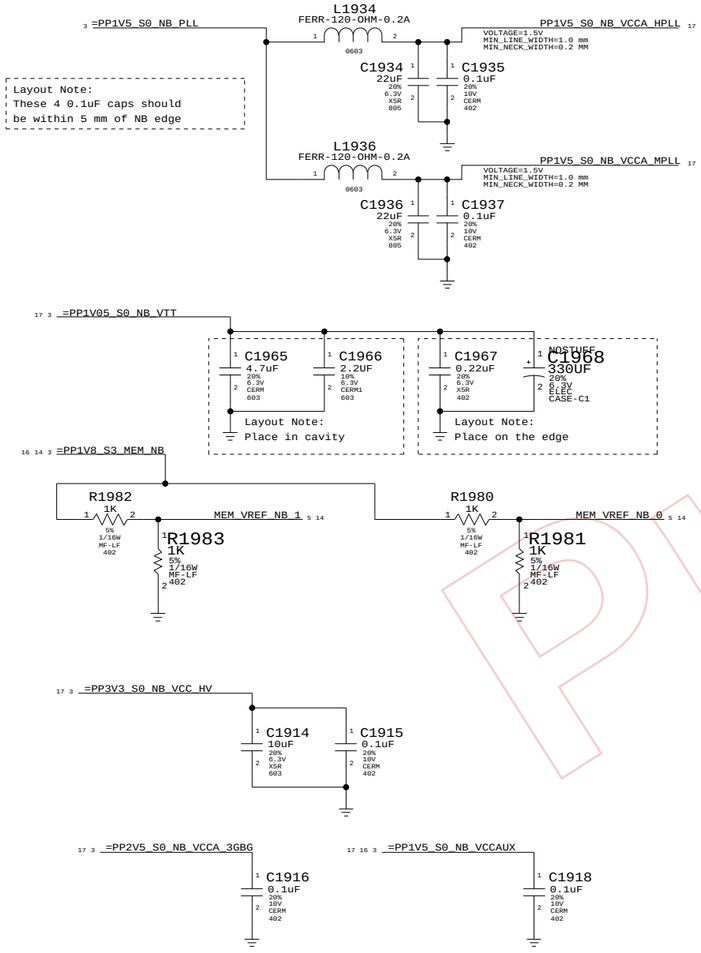


NB Grounds

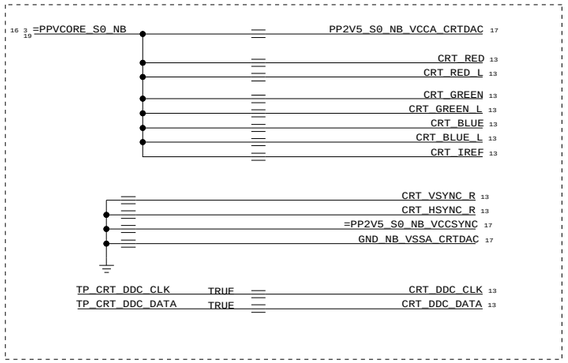
SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

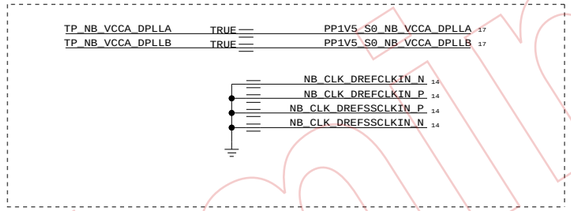
SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 18 OF 97	



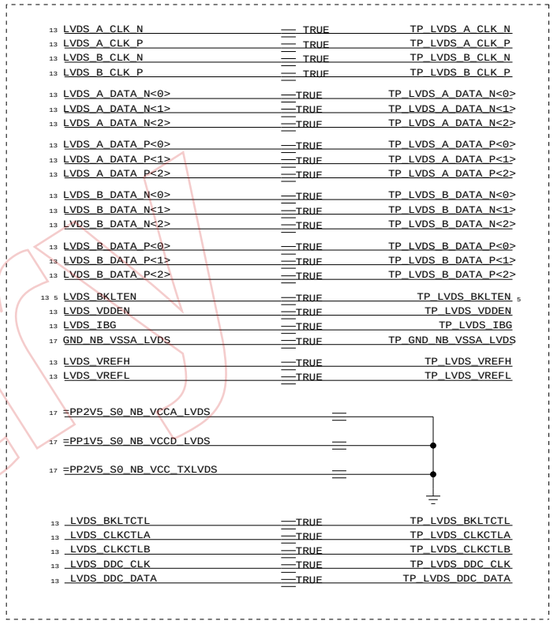
TVOUT DISABLE



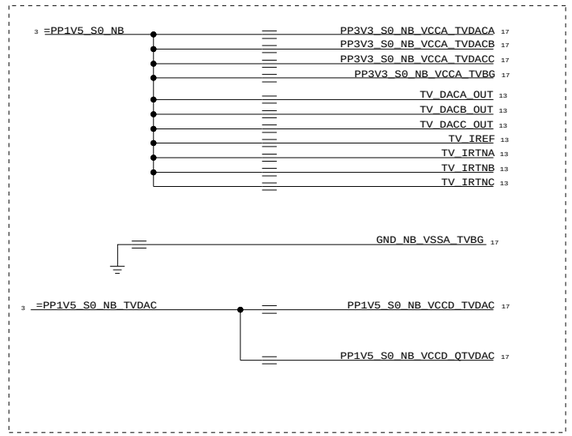
DISPLAY DISABLE

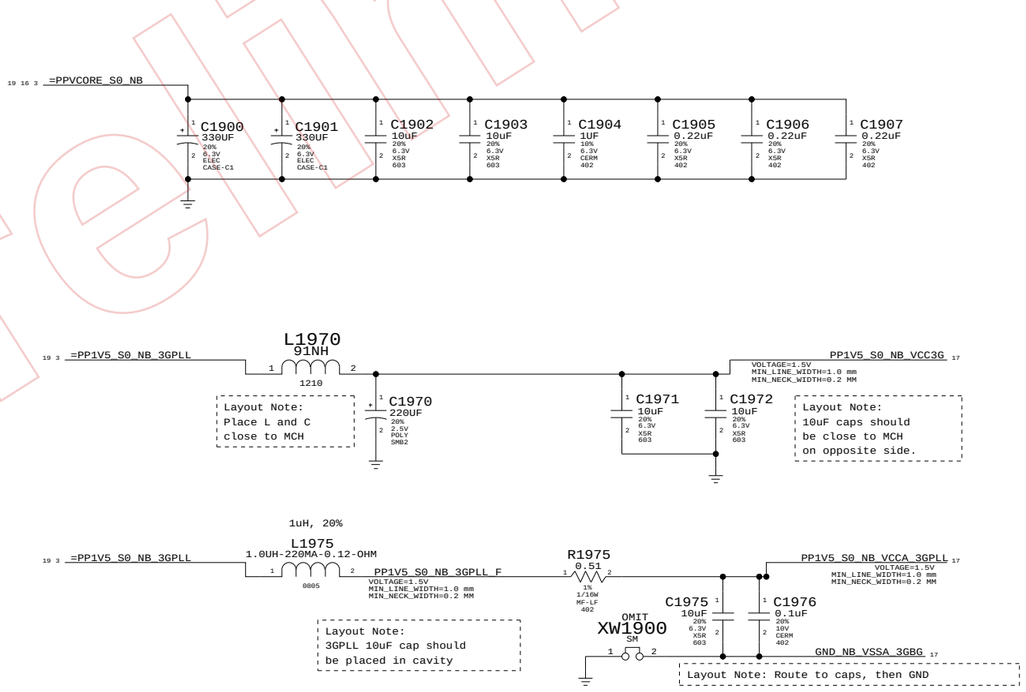


LVDS DISABLE



TVOUT DISABLE





NB (GM) Decoupling

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 19 OF 97	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075 2.2K 5% 1/16W MF-LF 402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077 2.2K 5% 1/16W MF-LF 402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079 2.2K 5% 1/16W MF-LF 402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085 2.2K 5% 1/16W MF-LF 402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 3 14 20
NBCFG_VCC_1V5
R2058 2.2K 5% 1/16W MF-LF 402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 3 14 20
NBCFG_DMI_REVERSE
R2059 2.2K 5% 1/16W MF-LF 402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 3 14 20
NBCFG_SDVO_AND_PCIE
R2060 2.2K 5% 1/16W MF-LF 402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

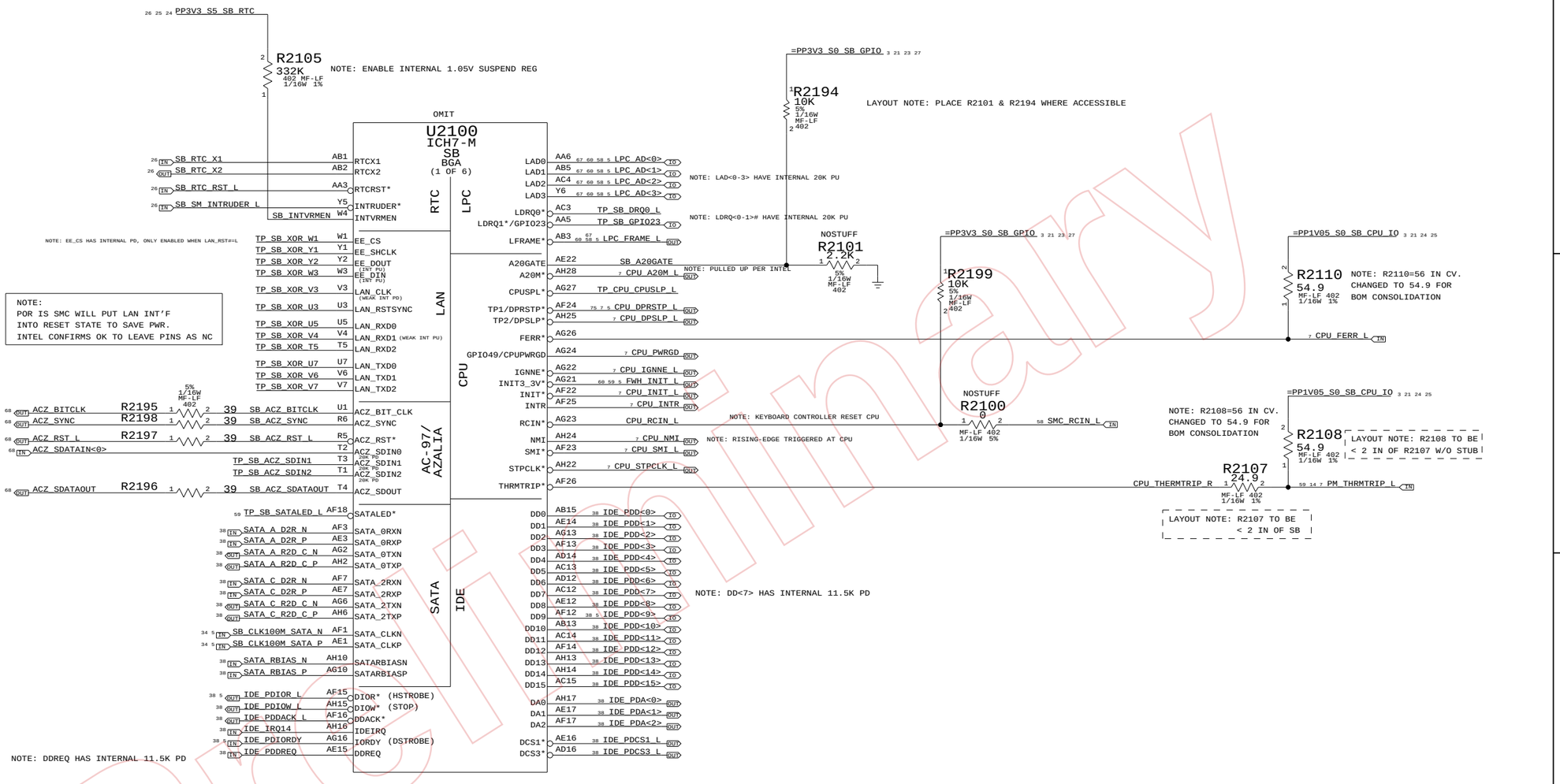
NB Config Straps

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A

SCALE	SHT
NONE	20 OF 97



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

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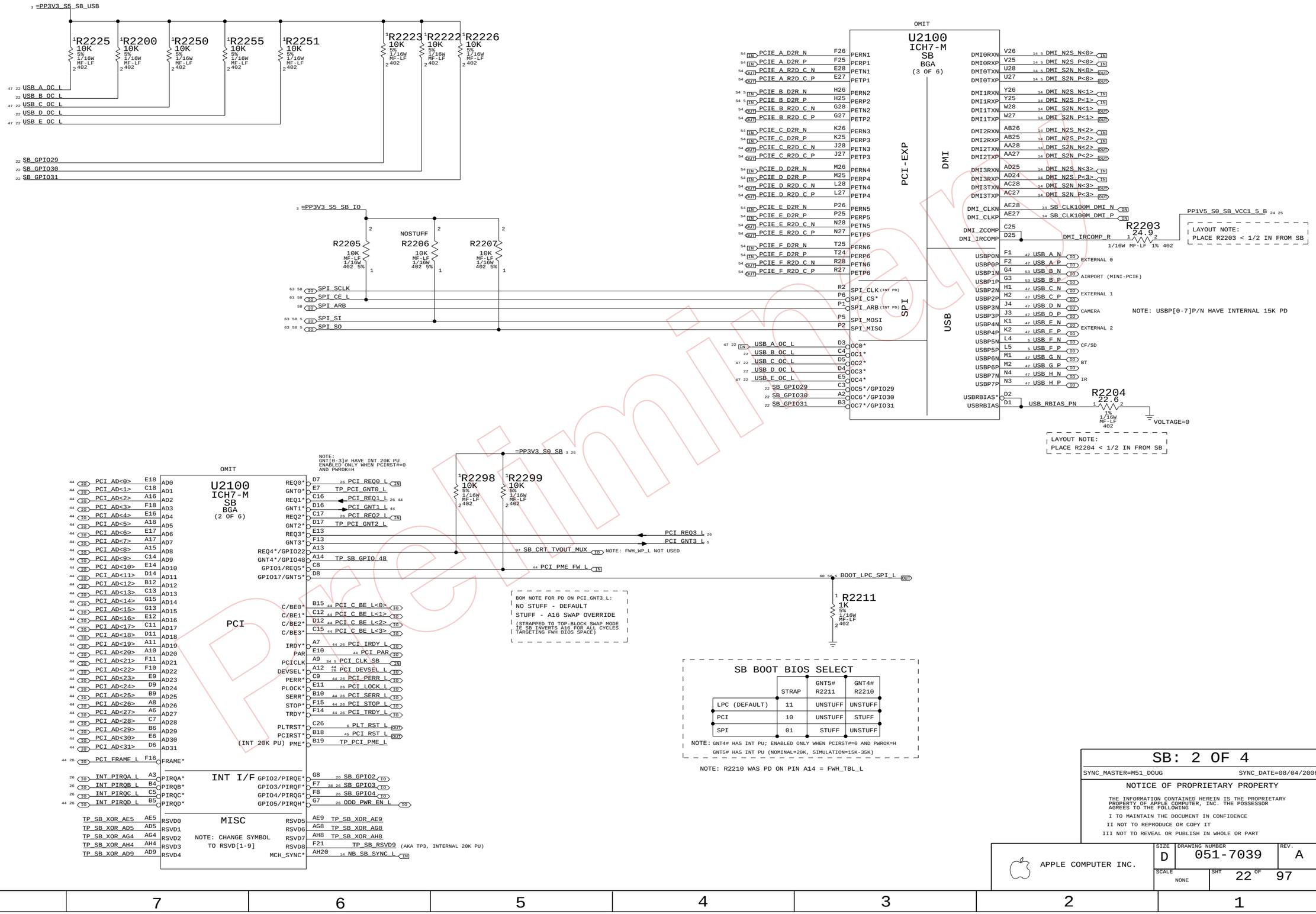
SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 21 OF 97	


=PP3V3_S5_SB_USB
R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2223 10K 5% 1/16W MF-LF 402
R2222 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO30
SB_GPIO31
=PP3V3_S5_SB_IO
R2205 10K MF-LF 1/16W 402 5%
NOSTUFF
R2206 10K MF-LF 1/16W 402 5%
R2207 10K MF-LF 1/16W 402 5%
SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO
OMIT
U2100
ICH7-M
SB
BGA
(3 OF 6)
PCI-EXP
DMI
SPI
USB
PCIE_A_D2R_N
PCIE_A_D2R_P
PCIE_A_R2D_C_N
PCIE_A_R2D_C_P
PCIE_B_D2R_N
PCIE_B_D2R_P
PCIE_B_R2D_C_N
PCIE_B_R2D_C_P
PCIE_C_D2R_N
PCIE_C_D2R_P
PCIE_C_R2D_C_N
PCIE_C_R2D_C_P
PCIE_D_D2R_N
PCIE_D_D2R_P
PCIE_D_R2D_C_N
PCIE_D_R2D_C_P
PCIE_E_D2R_N
PCIE_E_D2R_P
PCIE_E_R2D_C_N
PCIE_E_R2D_C_P
PCIE_F_D2R_N
PCIE_F_D2R_P
PCIE_F_R2D_C_N
PCIE_F_R2D_C_P
SPI_CLK
SPI_CS*
SPI_ARB
SPI_MOSI
SPI_MISO
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO30
SB_GPIO31
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
DMI_IRCOMP_R
R2203 24.9 1/16W MF-LF 1% 402
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE: PLACE R2203 < 1/2 IN FROM SB
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBRBIAS*
USBRBIAS
EXTERNAL 0
AIRPORT (MINI-PCIE)
EXTERNAL 1
CAMERA
EXTERNAL 2
CF/SD
BT
IR
NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD
R2204 22.6 1% 1/16W MF-LF 402
USB_RBIAS_PN
VOLTAGE=0
LAYOUT NOTE: PLACE R2204 < 1/2 IN FROM SB
NOTE: GNT[0-3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
OMIT
U2100
ICH7-M
SB
BGA
(2 OF 6)
PCI
INT I/F
MISC
PCI_AD<0>
PCI_AD<1>
PCI_AD<2>
PCI_AD<3>
PCI_AD<4>
PCI_AD<5>
PCI_AD<6>
PCI_AD<7>
PCI_AD<8>
PCI_AD<9>
PCI_AD<10>
PCI_AD<11>
PCI_AD<12>
PCI_AD<13>
PCI_AD<14>
PCI_AD<15>
PCI_AD<16>
PCI_AD<17>
PCI_AD<18>
PCI_AD<19>
PCI_AD<20>
PCI_AD<21>
PCI_AD<22>
PCI_AD<23>
PCI_AD<24>
PCI_AD<25>
PCI_AD<26>
PCI_AD<27>
PCI_AD<28>
PCI_AD<29>
PCI_AD<30>
PCI_AD<31>
PCI_FRAME_L
INT_PIRQA_L
INT_PIRQB_L
INT_PIRQC_L
INT_PIRQD_L
TP_SB_XOR_AE5
TP_SB_XOR_AD5
TP_SB_XOR_AG4
TP_SB_XOR_AH4
TP_SB_XOR_AD9
NOTE: CHANGE SYMBOL TO RSVD[1-9]
REQ0*
GNT0*
REQ1*
GNT1*
REQ2*
GNT2*
REQ3*
GNT3*
REQ4*/GPIO22
GNT4*/GPIO48
GPIO1/REQ5*
GPIO17/GNT5*
C/BE0*
C/BE1*
C/BE2*
C/BE3*
IRDY*
PAR
PCICLK
DEVSEL*
PERR*
PLOCK*
SERR*
STOP*
TRDY*
PLTRST*
PCIRST*
(INT 20K PU) PME*
GPIO2/PIRQE*
GPIO3/PIRQF*
GPIO4/PIRQG*
GPIO5/PIRQH*
RSVD5
RSVD6
RSVD7
RSVD8
MCH_SYNC*
TP_PCI_GNT0_L
TP_PCI_GNT1_L
TP_PCI_GNT2_L
TP_SB_GPIO_48
TP_PCI_PME_L
PCI_REQ0_L
PCI_REQ1_L
PCI_REQ2_L
PCI_REQ3_L
PCI_GNT3_L
SB_CRT_TVOUT_MUX
NOTE: FWH_WP_L NOT USED
PCI_PME_FW_L
PCI_C_BE_L<0>
PCI_C_BE_L<1>
PCI_C_BE_L<2>
PCI_C_BE_L<3>
PCI_IRDY_L
PCI_PAR
PCI_CLK_SB
PCI_DEVSEL_L
PCI_PERR_L
PCI_LOCK_L
PCI_SERR_L
PCI_STOP_L
PCI_TRDY_L
PLT_RST_L
PCI_RST_L
SB_GPIO2
SB_GPIO3
SB_GPIO4
ODD_PWR_EN_L
TP_SB_XOR_AE9
TP_SB_XOR_AG8
TP_SB_XOR_AH8
TP_SB_RSVD9 (AKA TP3, INTERNAL 20K PU)
NB_SB_SYNC_L
=PP3V3_S0_SB
R2298 10K 5% 1/16W MF-LF 402
R2299 10K 5% 1/16W MF-LF 402
BOOT_LPC_SPI_L
R2211 1K 5% 1/10W MF-LF 402
BOM NOTE FOR PD ON PCI_GNT3_L:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IE SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)
SB BOOT BIOS SELECT
STRAP
GNT5# R2211
GNT4# R2210
LPC (DEFAULT) 11 UNSTUFF UNSTUFF
PCI 10 UNSTUFF STUFF
SPI 01 STUFF UNSTUFF
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L
SB: 2 OF 4
SYNC_MASTER=M51_DOUG
SYNC_DATE=08/04/2006
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SIZE D
DRAWING NUMBER 051-7039
REV. A
SCALE NONE
SHT 22 OF 97

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 3 21 23 27

=PP3V3_S5_SB 3 23 25 26

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2323 NO_REBOOT_MODE 1K 1/16W 402 MF-LF 5%

RP2300 10K 5% 1/16W SM-LF

26 25 23 3 =PP3V3_S5_SB

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

27 TO SMB_CLK — C22 SMBCLK
27 TO SMB_DATA — B22 SMBDATA
SMB_LINK_ALERT_L — A26 LINKALERT*
SMLINK<0> — B25 SMLINK0
SMLINK<1> — A25 SMLINK1
NOT USED
PM_RI_L — A28 RI*
SB_SPKR — A19 SPKR (INT WEAK PD)
67 60 58 5 OUT PM_SUS_STAT_L — A27 SUS_STAT*
58 26 IN PM_SYSRST_L — A22 SYS_RST*
14 IN PM_BMBUSY_L — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE

SYS GPIO / PWR MNGT

33 OUT PM_STPPCI_L — AC20 GPIO18/STPPCI*
34 OUT PM_STPCPU_L — AF21 GPIO20/STPCPU*
SB_GPIO26 — A21 GPIO26
23 BIOS_REC — B21 GPIO27
23 FWH_MFG_MODE — E23 GPIO28
67 60 58 5 TO PM_CLKRUN_L — AG18 GPIO32/CLKRUN*
TP_AZ_DOCK_EN_L — AC19 GPIO33/AZ_DOCK_EN*
RESERVED FOR MOBILE AZALIA DOCKING INT'F
TP_AZ_DOCK_RST_L — U2 GPIO34/AZ_DOCK_RST*
53 41 IN PCIE_WAKE_L — F20 WAKE*
67 60 58 5 TO INT_SERIRQ — AH21 SERIRQ
58 10 IN PM_THRM_L — AF20 THRM*
26 5 IN VR_PWRGD_CK410 — AD22 VRMPWRGD
6 GPU_PRESENT_R — AC21 GPIO6
58 IN SMC_RUNTIME_SCI_L — AC18 GPIO7
58 IN SMC_EXTSMI_L — E21 GPIO8

GPIO

SATA GPIO

GPIO21/SATA0GP — AF19 SB_GPIO21 — 100 — R2302
GPIO19/SATA1GP — AH18 SB_GPIO19 — 100 — R2303
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19 SB_GPIO37 — 100 — R2305
38 SATA_C_DET_L IN

CLKS

CLK14 — AC1 — 34 5 SB_CLK14P3M_TIMER IN
CLK48 — B2 — 34 5 SB_CLK48M_USBCTLR IN
SUSCLK — C20 — 59 SUS_CLK_SB OUT

SLP_S3* — B24 — 79 77 58 5 PM_SLP_S3_L OUT
SLP_S4* — D23 — 77 58 5 PM_SLP_S4_L OUT
SLP_S5* — F22 — 58 PM_SLP_S5_L OUT
PWROK — AA4 — 26 PM_SB_PWROK IN
AC22 — 75 14 5 PM_DPRSLPVR OUT
GPIO16/DPRSLPVR
TP0/BATLOW* — C21 — NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN* — C23 — 58 PM_PWRBTN_L IN
LAN_RST* — C19 — 58 PM_LAN_ENABLE IN — NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* — Y4

GPIO9 — E20 — 58 26 SMS_INT_L IN
GPIO10 — A20 — 58 SMC_SB_NMI IN
DEF=GPI GPIO12 — F19 — 23 PATA_PWR_EN_L OUT
GPIO13 — E19
DEF=GPI GPIO14 — R4 — 38 IDE_RESET_L OUT
GPIO15 — E22 — SV_SET_UP 5 23 60
GPIO24 — R3 — TP_SB_GPIO24
GPIO25 — D20 — TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 — 33 SB_CLK100M_SATA_OE_L OUT
GPIO38 — AD20 — TP_SB_GPIO38 TO
DEF=GPI GPIO39 — AE20 — 23 SATA_C_PWR_EN_L OUT

=PP3V3_S5_SB_PM 3 11

R2387 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

58 PM_BATLOW_L IN
58 PM_RSMRST_L IN
58 SMC_WAKE_SCI_L IN

R2399 100K 5% 1/16W 402 MF-LF

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

26 25 23 3 =PP3V3_S5_SB

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 10K 1/16W 402 MF-LF 5%

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

SV_SET_UP 5 23 60
EFI_OK_R

26 25 23 3 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE 23
BIOS_REC 23

=PP3V3_S5_SB 3 23 25 26

R2390 10K 5% 1/16W MF-LF 402

23 PATA_PWR_EN_L

=PP3V3_S0_SB_GPIO 3 21 23 27

R2388 10K 5% 1/16W MF-LF 402

23 SATA_C_PWR_EN_L

SB: 3 OF 4

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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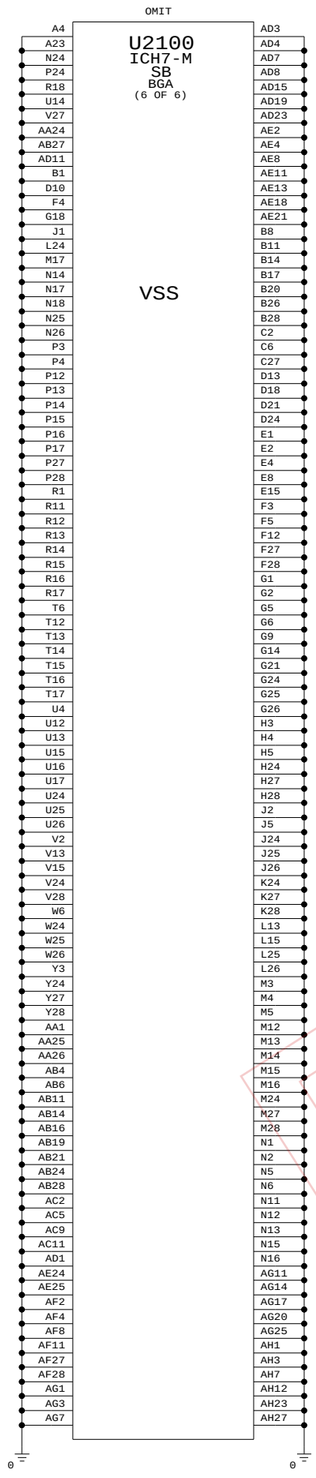
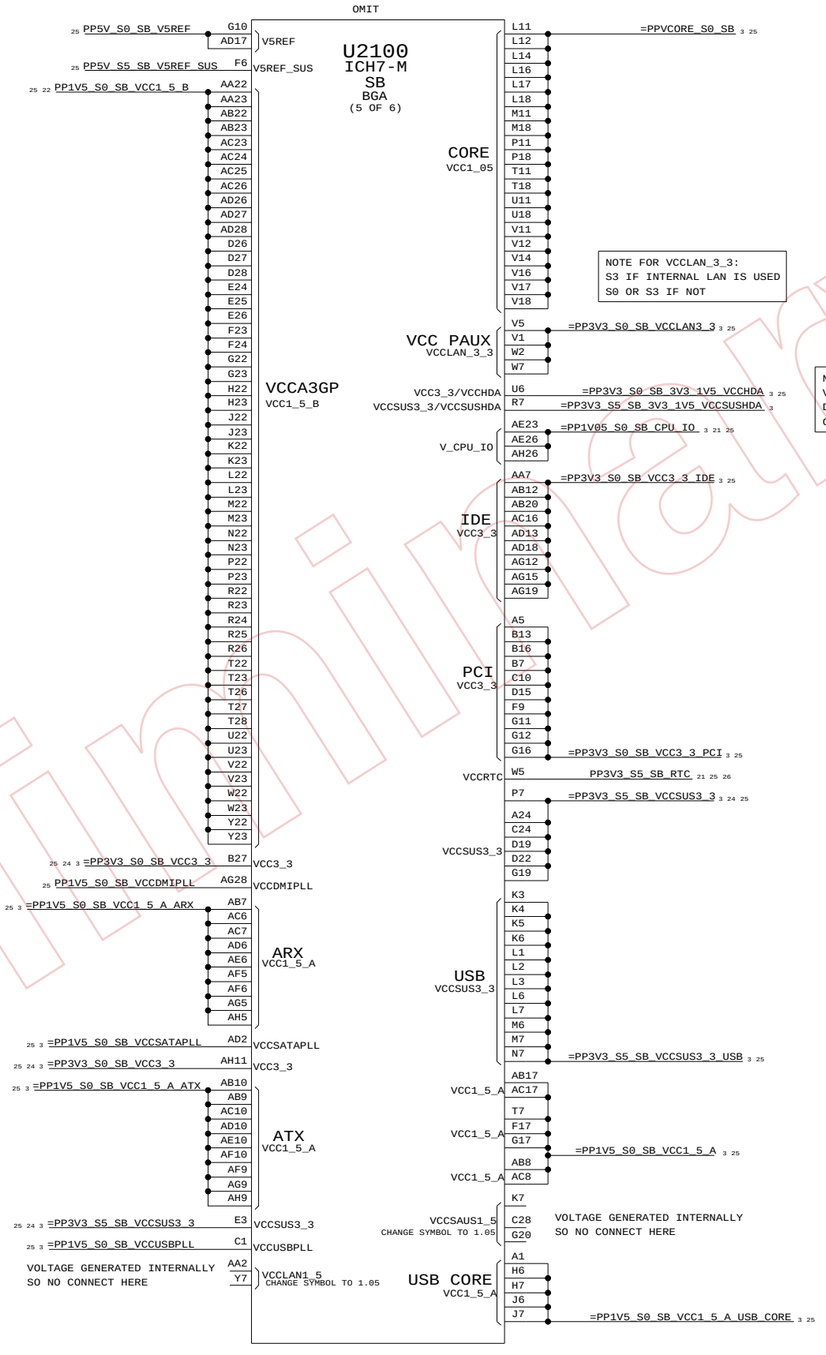
SIZE	DRAWING NUMBER	REV.
D	051-7039	A

SCALE	SHT
NONE	23 OF 97





SB: 4 OF 4

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

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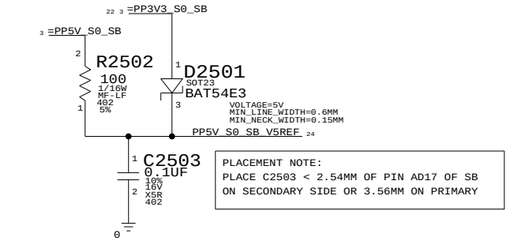
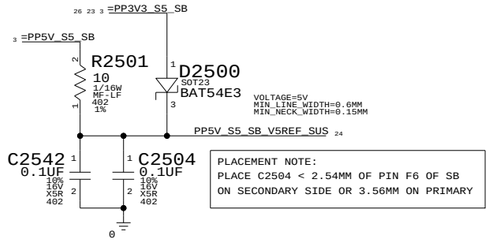
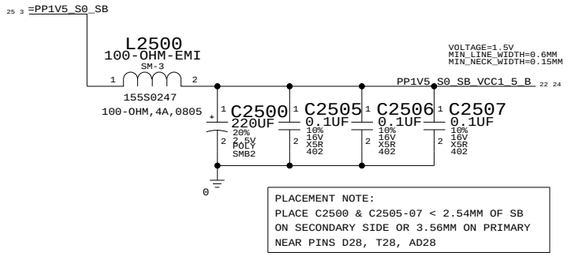
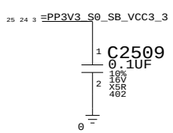
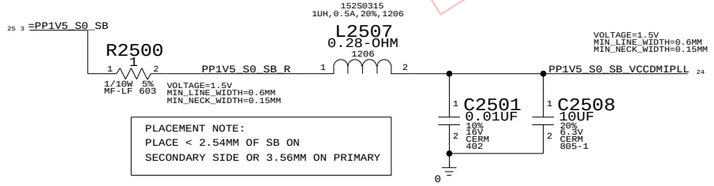
SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 24 OF 97	

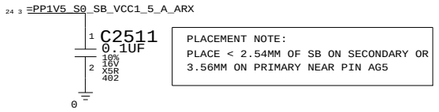


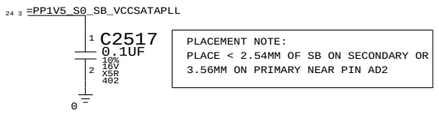


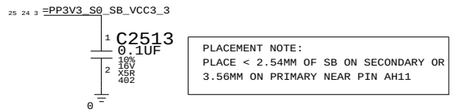


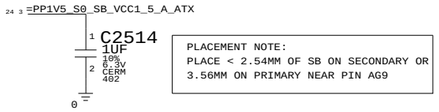


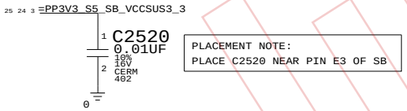


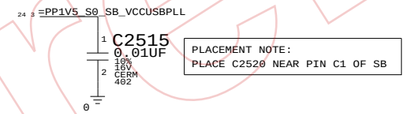


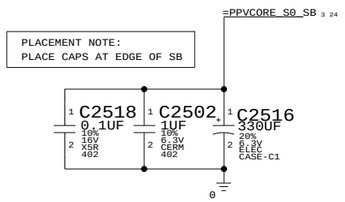


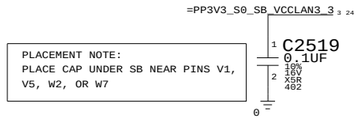


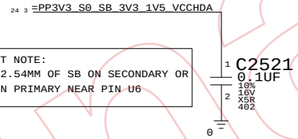


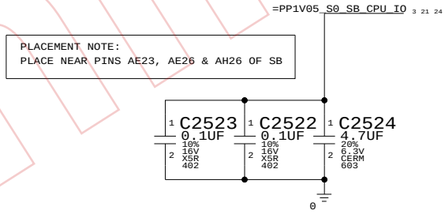


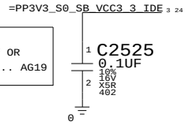


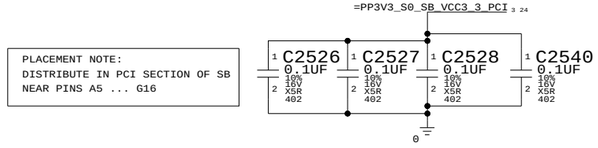


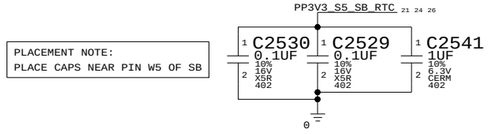


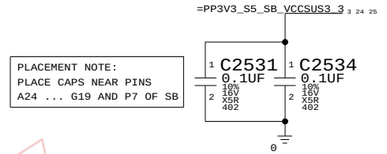


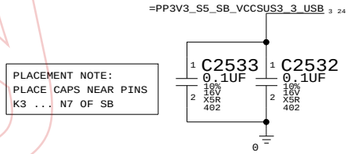


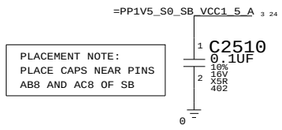


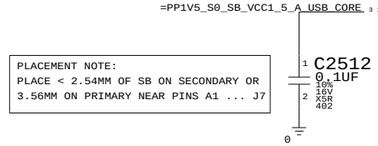












SB:DECOUPLING

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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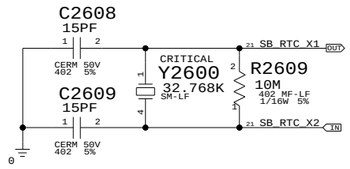

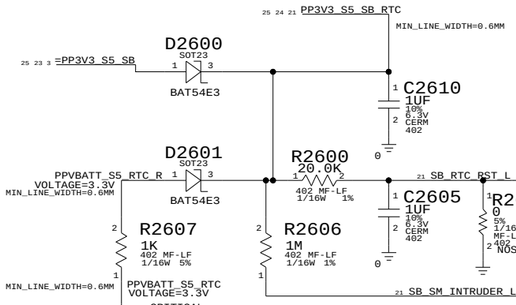

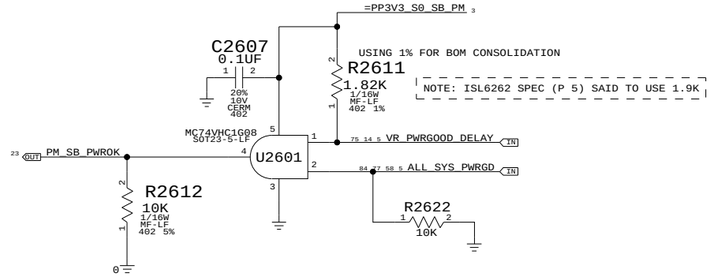

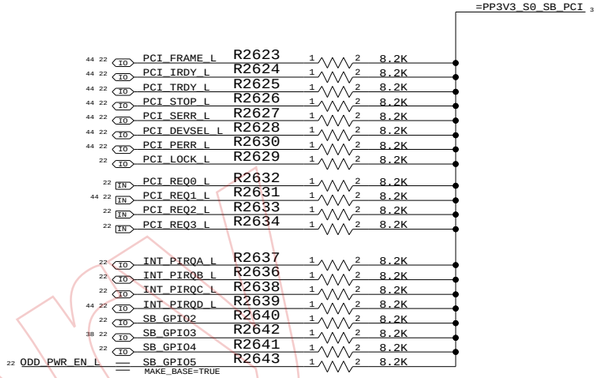

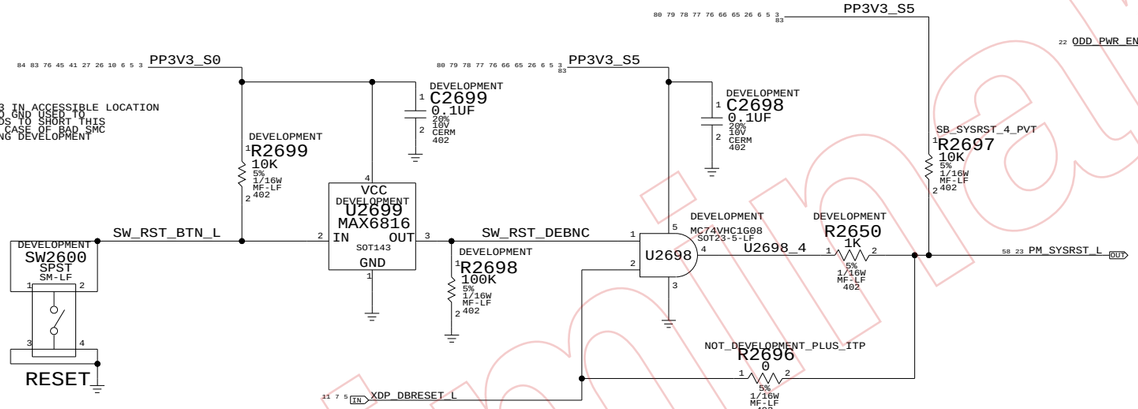

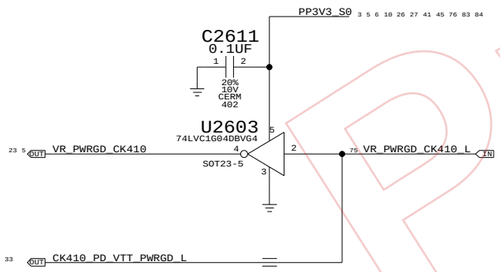

SB: MISC

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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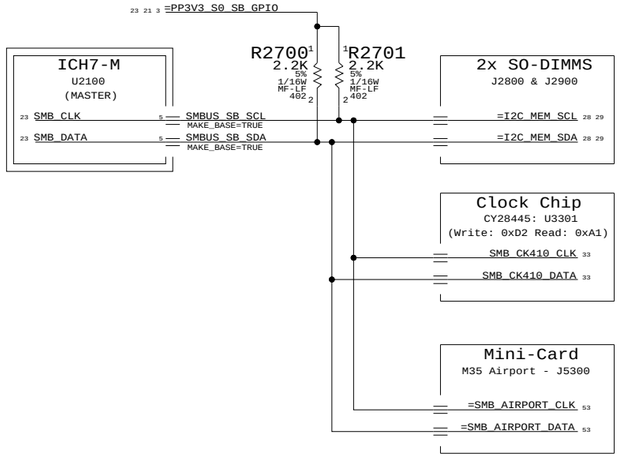
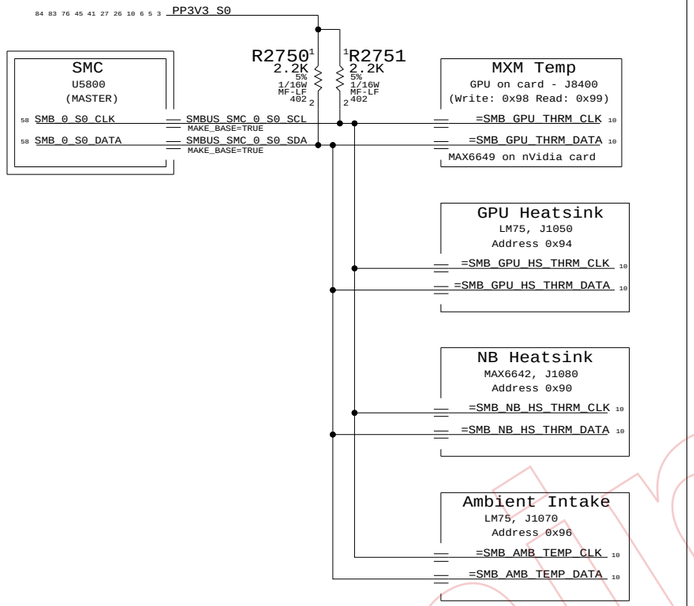
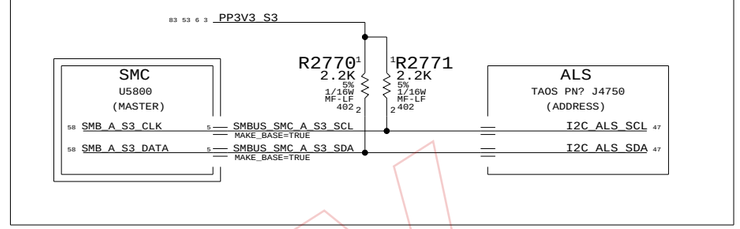
ICH7-M SMBus Connections



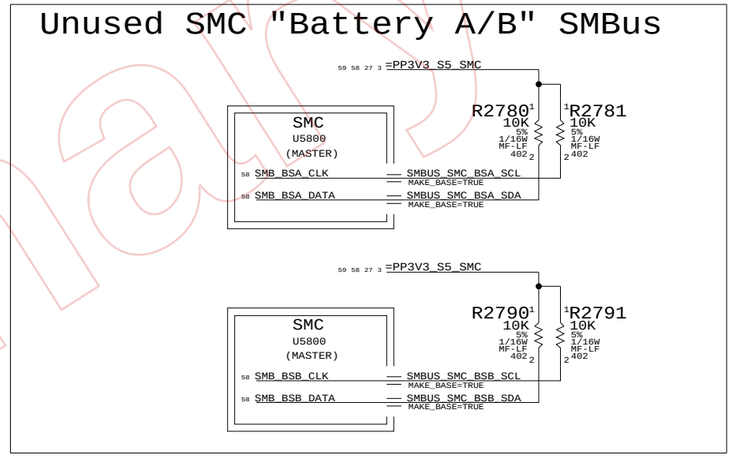
SMC "0" SMBus Connections



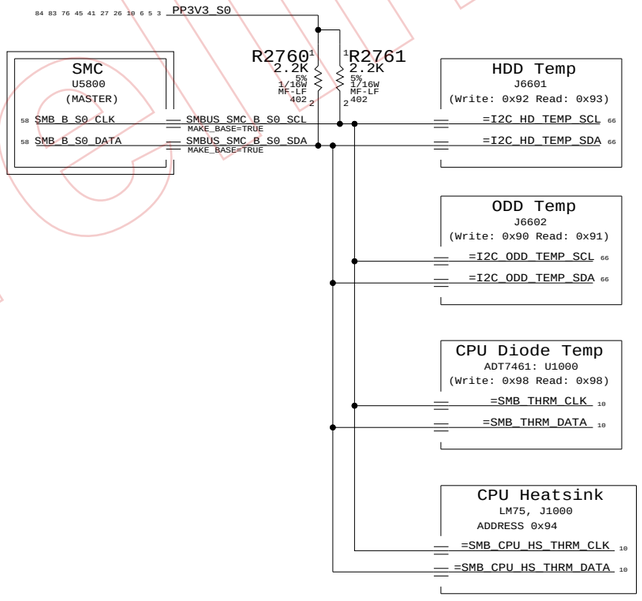
SMC "A" SMBus Connections



Unused SMC "Battery A/B" SMBus



SMC "B" SMBus Connections



M51 SMBus Connections

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
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Page Notes

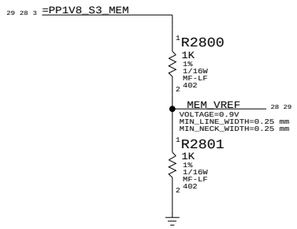
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

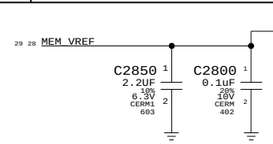
Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

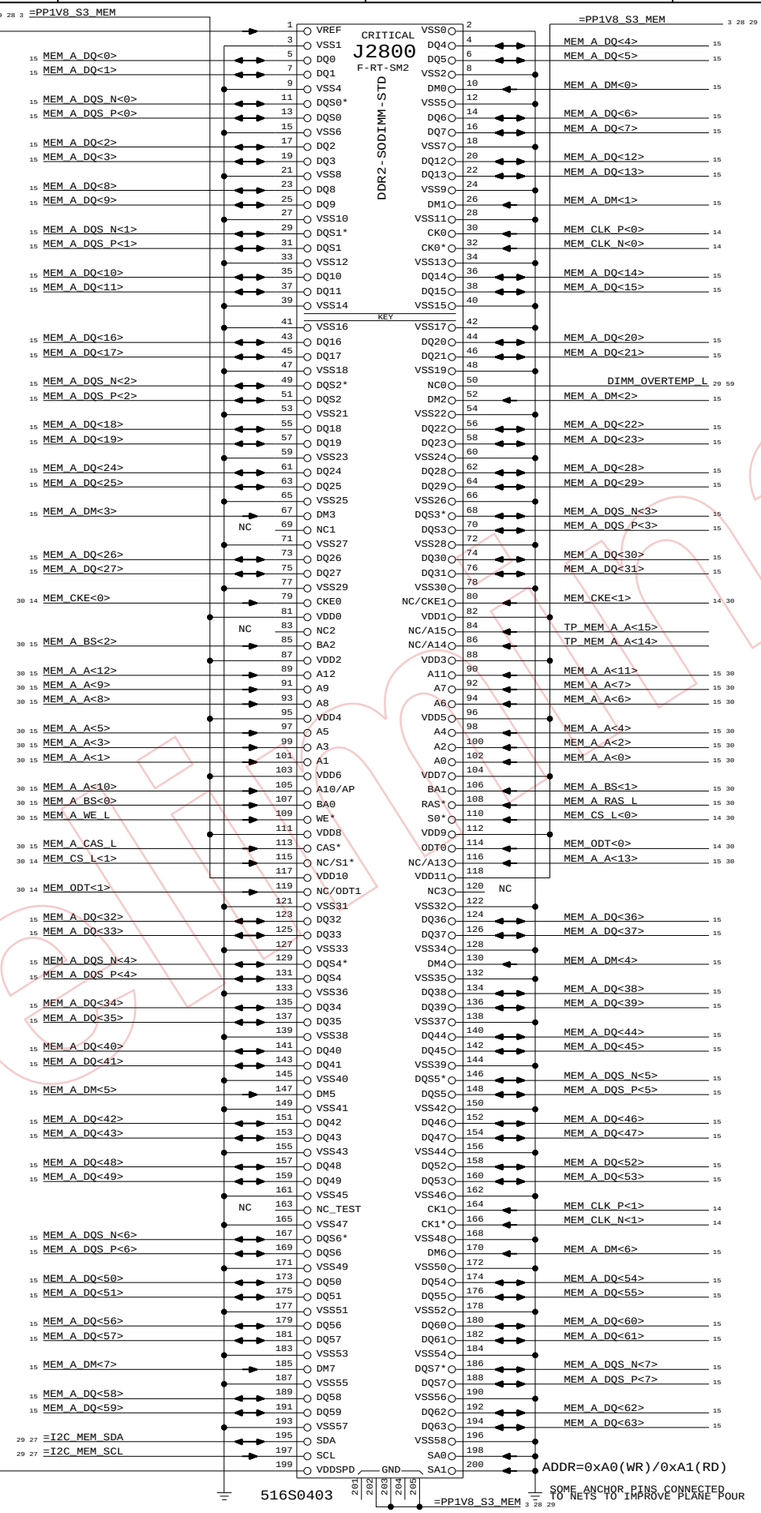
BOM options provided by this page:
(NONE)

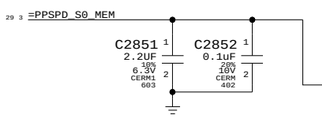
DDR2 VRef

One 0.1uF per connector



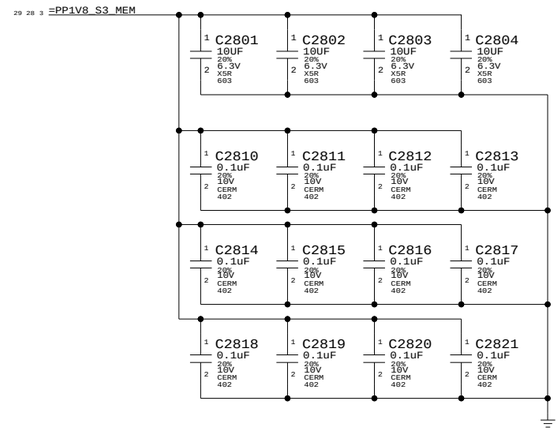






DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
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Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

28 MEM_VREF

C2950 2.2UF 10% 6.3V CERM1 603 — C2900 0.1uF 20% 10V CERM 402

29 28 3 =PP1V8_S3_MEM

CRITICAL
J2900
F-RT-SM2
DDR2-SODIMM-REV

	VREF	1	2	VSS0			
	VSS1	3	4	DQ4	15	MEM_B_DQ<4>	15
15	MEM_B_DQ<0>	5	6	DQ5	15	MEM_B_DQ<5>	15
15	MEM_B_DQ<1>	7	8	VSS2			
	VSS4	9	10	DM0	15	MEM_B_DM<0>	15
15	MEM_B_DQS_N<0>	11	12	VSS5			
15	MEM_B_DQS_P<0>	13	14	DQ6	15	MEM_B_DQ<6>	15
	VSS6	15	16	DQ7	15	MEM_B_DQ<7>	15
15	MEM_B_DQ<2>	17	18	VSS7			
15	MEM_B_DQ<3>	19	20	DQ12	15	MEM_B_DQ<12>	15
	VSS8	21	22	DQ13	15	MEM_B_DQ<13>	15
15	MEM_B_DQ<8>	23	24	VSS9			
15	MEM_B_DQ<9>	25	26	DM1	15	MEM_B_DM<1>	15
	VSS10	27	28	VSS11			
15	MEM_B_DQS_N<1>	29	30	CK0	14	MEM_CLK_P<3>	14
15	MEM_B_DQS_P<1>	31	32	CK0*	14	MEM_CLK_N<3>	14
	VSS12	33	34	VSS13			
15	MEM_B_DQ<10>	35	36	DQ14	15	MEM_B_DQ<14>	15
15	MEM_B_DQ<11>	37	38	DQ15	15	MEM_B_DQ<15>	15
	VSS14	39	40	VSS15			
	KEY						
	VSS16	41	42	VSS17			
15	MEM_B_DQ<16>	43	44	DQ20	15	MEM_B_DQ<20>	15
15	MEM_B_DQ<17>	45	46	DQ21	15	MEM_B_DQ<21>	15
	VSS18	47	48	VSS19			
15	MEM_B_DQS_N<2>	49	50	NC0	28 59	DIMM_OVERTEMP_L	
15	MEM_B_DQS_P<2>	51	52	DM2	15	MEM_B_DM<2>	15
	VSS21	53	54	VSS22			
15	MEM_B_DQ<18>	55	56	DQ22	15	MEM_B_DQ<22>	15
15	MEM_B_DQ<19>	57	58	DQ23	15	MEM_B_DQ<23>	15
	VSS23	59	60	VSS24			
15	MEM_B_DQ<24>	61	62	DQ28	15	MEM_B_DQ<28>	15
15	MEM_B_DQ<25>	63	64	DQ29	15	MEM_B_DQ<29>	15
	VSS25	65	66	VSS26			
15	MEM_B_DM<3>	67	68	DQS3*	15	MEM_B_DQS_N<3>	15
NC		69	70	DQS3	15	MEM_B_DQS_P<3>	15
	NC1	71	72	VSS28			
	VSS27	73	74	DQ30	15	MEM_B_DQ<30>	15
15	MEM_B_DQ<26>	75	76	DQ31	15	MEM_B_DQ<31>	15
15	MEM_B_DQ<27>	77	78	VSS30			
	VSS29	79	80	NC/CKE1	14 30	MEM_CKE<3>	14 30
30 14	MEM_CKE<2>	81	82	VDD1			
	VDD0	83	84	NC/A15	5	TP_MEM_B_A<15>	5
NC		85	86	NC/A14	5	TP_MEM_B_A<14>	5
	NC2	87	88	VDD3			
30 15	MEM_B_BS<2>	89	90	A11	15 30	MEM_B_A<11>	15 30
	VDD2	91	92	A7	15 30	MEM_B_A<7>	15 30
30 15	MEM_B_A<12>	93	94	A6	15 30	MEM_B_A<6>	15 30
30 15	MEM_B_A<9>	95	96	VDD5			
30 15	MEM_B_A<8>	97	98	A4	15 30	MEM_B_A<4>	15 30
	VDD4	99	100	A2	15 30	MEM_B_A<2>	15 30
30 15	MEM_B_A<5>	101	102	A0	15 30	MEM_B_A<0>	15 30
30 15	MEM_B_A<3>	103	104	VDD7			
30 15	MEM_B_A<1>	105	106	BA1	15 30	MEM_B_BS<1>	15 30
	VDD6	107	108	RAS*	15 30	MEM_B_RAS_L	15 30
30 15	MEM_B_A<10>	109	110	S0*	14 30	MEM_CS_L<2>	14 30
30 15	MEM_B_BS<0>	111	112	VDD9			
30 15	MEM_B_WE_L	113	114	ODT0	14 30	MEM_ODT<2>	14 30
	VDD8	115	116	NC/A13	15 30	MEM_B_A<13>	15 30
30 15	MEM_B_CAS_L	117	118	VDD11			
30 14	MEM_CS_L<3>	119	120	NC3	NC		
	VDD10	121	122	VSS32			
30 14	MEM_ODT<3>	123	124	DQ36	15	MEM_B_DQ<36>	15
	NC/ODT1	125	126	DQ37	15	MEM_B_DQ<37>	15
	VSS31	127	128	VSS34			
15	MEM_B_DQ<32>	129	130	DM4	15	MEM_B_DM<4>	15
15	MEM_B_DQ<33>	131	132	VSS35			
	VSS33	133	134	DQ38	15	MEM_B_DQ<38>	15
15	MEM_B_DQS_N<4>	135	136	DQ39	15	MEM_B_DQ<39>	15
15	MEM_B_DQS_P<4>	137	138	VSS37			
	VSS36	139	140	DQ44	15	MEM_B_DQ<44>	15
15	MEM_B_DQ<34>	141	142	DQ45	15	MEM_B_DQ<45>	15
15	MEM_B_DQ<35>	143	144	VSS39			
	VSS38	145	146	DQS5*	15	MEM_B_DQS_N<5>	15
15	MEM_B_DQ<40>	147	148	DQS5	15	MEM_B_DQS_P<5>	15
15	MEM_B_DQ<41>	149	150	VSS42			
	VSS40	151	152	DQ46	15	MEM_B_DQ<46>	15
15	MEM_B_DM<5>	153	154	DQ47	15	MEM_B_DQ<47>	15
	VSS41	155	156	VSS44			
15	MEM_B_DQ<42>	157	158	DQ52	15	MEM_B_DQ<52>	15
15	MEM_B_DQ<43>	159	160	DQ53	15	MEM_B_DQ<53>	15
	VSS43	161	162	VSS46			
15	MEM_B_DQ<48>	163	164	CK1	14	MEM_CLK_P<2>	14
15	MEM_B_DQ<49>	165	166	CK1*	14	MEM_CLK_N<2>	14
	VSS45	167	168	VSS48			
NC		169	170	DM6	15	MEM_B_DM<6>	15
	NC_TEST	171	172	VSS50			
	VSS47	173	174	DQ54	15	MEM_B_DQ<54>	15
15	MEM_B_DQS_N<6>	175	176	DQ55	15	MEM_B_DQ<55>	15
15	MEM_B_DQS_P<6>	177	178	VSS52			
	DQS6*	179	180	DQ60	15	MEM_B_DQ<60>	15
	DQS6	181	182	DQ61	15	MEM_B_DQ<61>	15
	VSS49	183	184	VSS54			
15	MEM_B_DQ<50>	185	186	DQS7*	15	MEM_B_DQS_N<7>	15
15	MEM_B_DQ<51>	187	188	DQS7	15	MEM_B_DQS_P<7>	15
	VSS51	189	190	VSS56			
15	MEM_B_DQ<56>	191	192	DQ62	15	MEM_B_DQ<62>	15
15	MEM_B_DQ<57>	193	194	DQ63	15	MEM_B_DQ<63>	15
	VSS53	195	196	VSS58			
15	MEM_B_DM<7>	197	198	SA0		ADDR=0XA4(WR)/0XA5(RD)	
	VSS55	199	200	SA1		MEM_B_SPD_SA1	
15	MEM_B_DQ<58>	201	202	GND			
15	MEM_B_DQ<59>	203	204	GND			
	VSS57	205	206	GND			
28 27	=I2C_MEM_SDA						
28 27	=I2C_MEM_SCL						
	VDDSPD						

516S0404

30 3 =PP0V9_S0_MEM_TERM

SOME ANCHOR PINS CONNECTED TO NETS TO IMPROVE PLANE POUR

=PP1V8_S3_MEM 3 28 29

29 28 3 =PPSPD_S0_MEM

C2951 2.2UF 10% 6.3V CERM1 603 — C2952 0.1uF 20% 16V CERM 402

=PPSPD_S0_MEM 3 28 29

R2900 10K 5% 1/16W MF-LF 402 — Resistor prevents pwr-gnd short

DDR2 Bypass Caps

(For return current)

29 28 3 =PP1V8_S3_MEM

C2908 C2909 C2910 C2911
C2912 C2913 C2914 C2915
C2916 C2917 C2918 C2919
C2920 C2921 C2922 C2923

1UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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APPLE COMPUTER INC.

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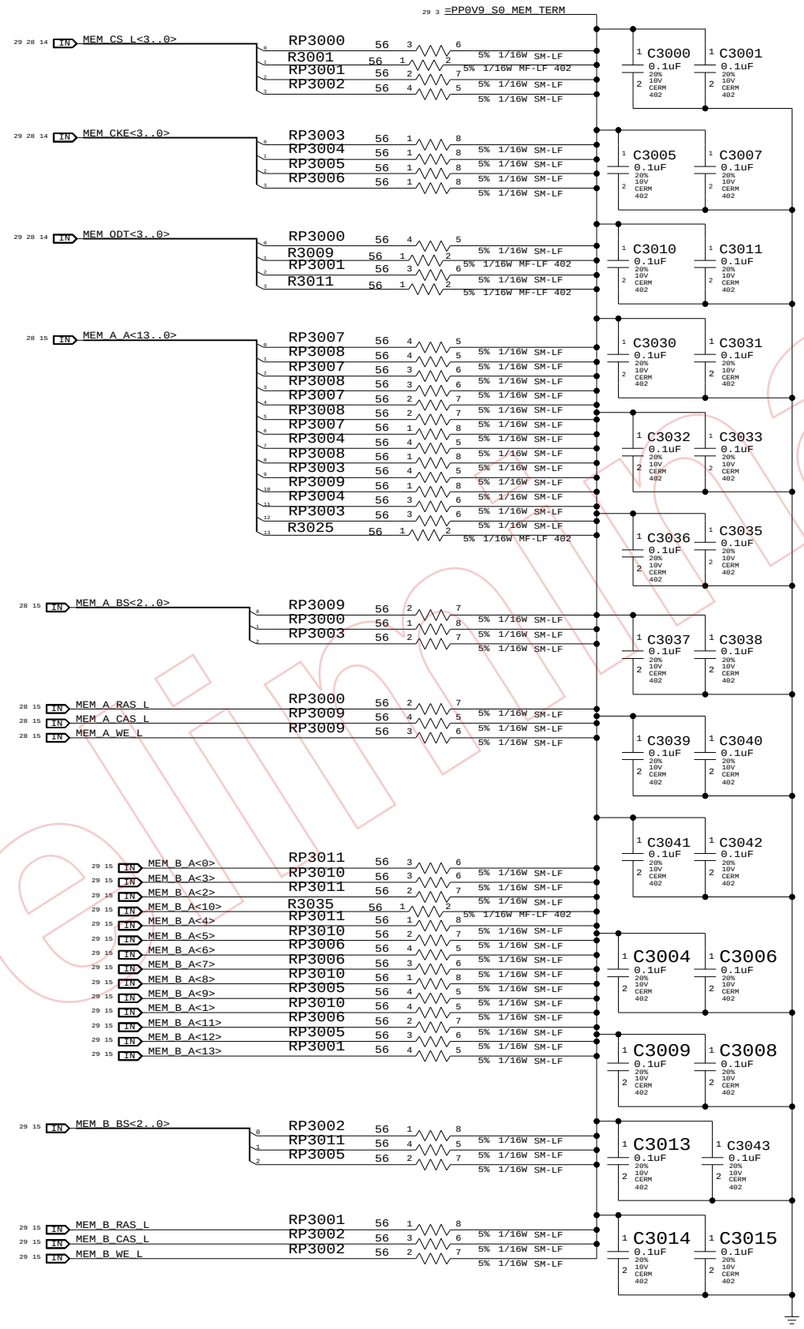
One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 30 OF 97	

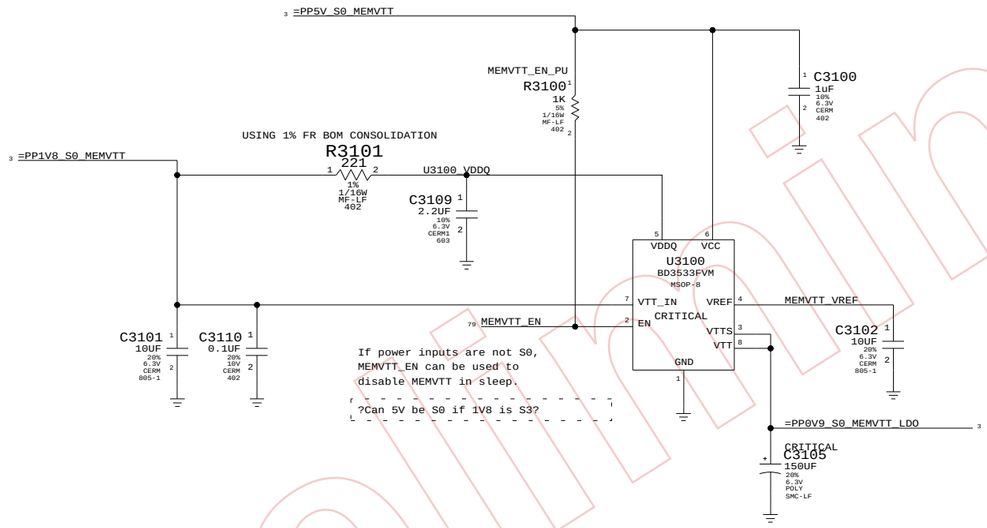
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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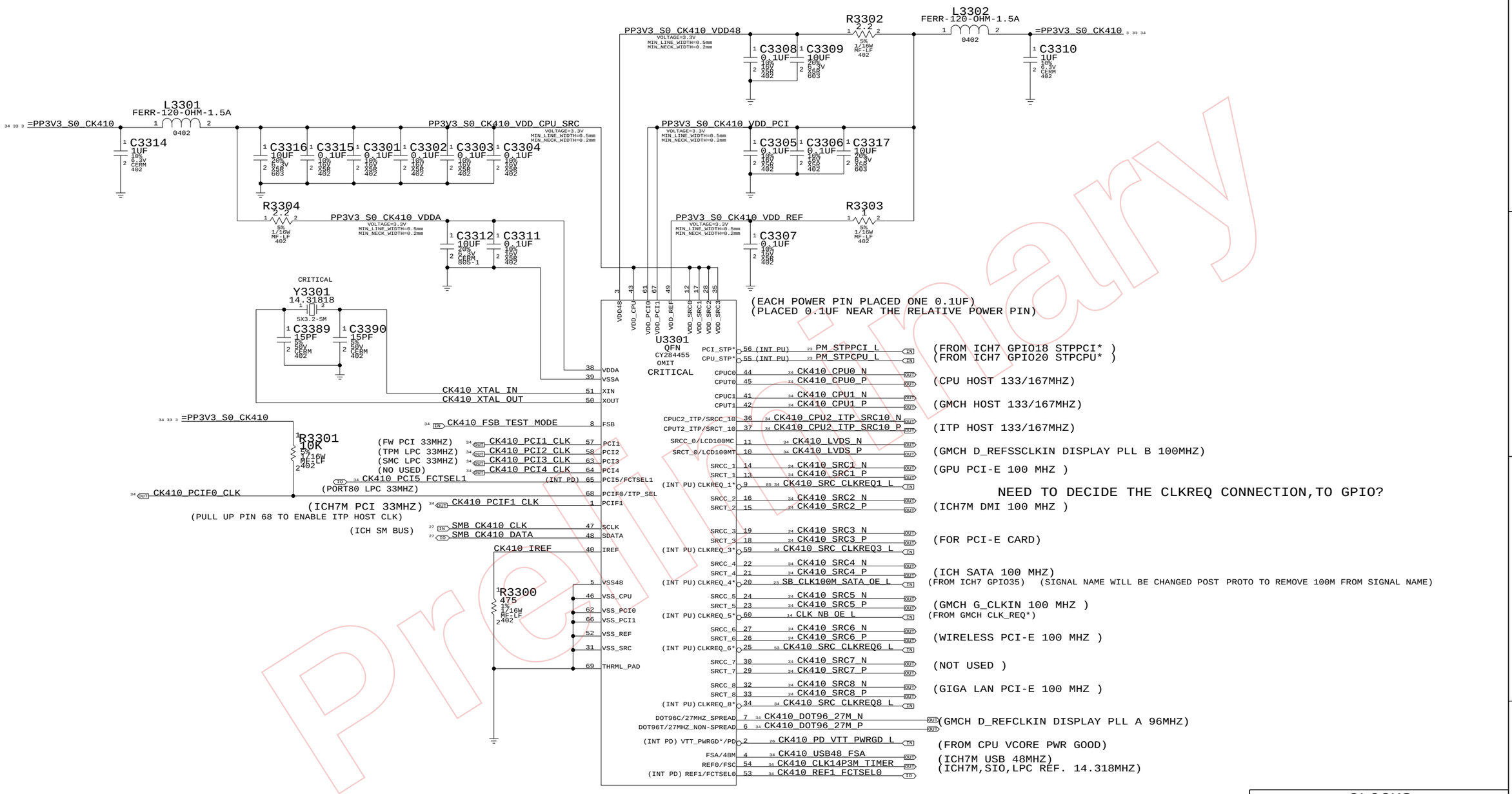
D	051-7039	A

SCALE: NONE SHT 31 OF 97



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A

SCALE NONE SHT 33 OF 97

FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3459 R3463	R3452 R3457 R3461
533MHZ (133MHZ CPU CLK)	R3452 R3457 R3461	R3454 R3459 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3454 R3459 R3463 R3457

80 34 5 3 PP1V05_S0

NOSTUFF R3452 56 5% 1/16W MF-LF 402

R3453 1K 1/16W 5% MF-LF 402

14 NB_BSEL<0>

34 CK410_FSA

R3454 0 5% 1/16W MF-LF 402

R3455 1K 1/16W 5% MF-LF 402

7 CPU_BSEL<0>

80 34 5 3 PP1V05_S0

R3456 1K 5% 1/16W MF-LF 402

NOSTUFF R3457 0 5% 1/16W MF-LF 402

R3458 1K 1/16W 5% MF-LF 402

14 NB_BSEL<1>

33 CK410_FSB_TEST_MODE

R3459 0 5% 1/16W MF-LF 402

7 CPU_BSEL<1>

80 34 5 3 PP1V05_S0

R3460 1K 5% 1/16W MF-LF 402

NOSTUFF R3461 0 5% 1/16W MF-LF 402

R3462 1K 1/16W 5% MF-LF 402

14 NB_BSEL<2>

34 CK410_FSC

R3463 0 5% 1/16W MF-LF 402

7 CPU_BSEL<2>

=PP3V3_S0_CK410 3 33

33 CK410_PCI5_FCTSEL1 R3499 1K 1/16W 5% MF-LF 402

R3497 2.2K 5% 1/16W MF-LF 402 CK410_FSC 34

33 CK410_CLK14P3M_TIMER R3498 33 1/16W 5% MF-LF 402 SB_CLK14P3M_TIMER 5 23

33 CK410_REF1_FCTSEL0 R3496 33 TP_CLK14P3M_SPARE

R3451 2.2K 5% 1/16W MF-LF 402 CK410_FSA 34

33 CK410_USB48_FSA R3400 33 1/16W 5% MF-LF 402 SB_CLK48M_USBCTLR 5 23

33 CK410_PCI4_CLK R3406 33 TP_PCI_CLK_SPARE

32 CK410_PCI3_CLK R3405 33 PCI_CLK_SMC 5 58

32 CK410_PCI2_CLK R3404 33 NOSTUFF PCI_CLK_TPM 67

33 CK410_PCI1_CLK R3403 33 PCI_CLK_FW 5 44

32 CK410_PCIF1_CLK R3401 33 PCI_CLK_SB 5 22

32 CK410_PCIF0_CLK R3402 33 PCI_CLK_PORT80 5 60

TPM CLOCK IS TURNED OFF IN SW AND RESISTOR NOSTUFF

33 CK410_SRC3_P 33 R3492 SPARE_SRC3_P R3488 49.9

33 CK410_SRC3_N 33 R3491 SPARE_SRC3_N R3487 49.9

33 CK410_SRC7_P 33 R3490 SPARE_SRC7_P R3486 49.9

33 CK410_SRC7_N 33 R3489 SPARE_SRC7_N R3485 49.9

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

85 33 CK410_SRC_CLKREQ1_L (GPU CLK OE*) R3495 NOSTUFF 1K

33 CK410_SRC_CLKREQ3_L (SPARE CLK OE*) R3494 1K

33 CK410_SRC_CLKREQ8_L (YUKON CLK OE*) R3493 1K

NOTE: CLKREQ1 SHOULD BE DRIVEN OR PULLED DOWN BY MXM GRAPHICS CARD.

33 CK410_CPU1_P 33 R3407 12 FSB_CLK_NB_P R3429 1% 402 1/16W MF-LF 49.9

33 CK410_CPU1_N 33 R3408 12 FSB_CLK_NB_N R3430 49.9

33 CK410_CPU0_P 33 R3409 7 FSB_CLK_CPU_P R3431 49.9

33 CK410_CPU0_N 33 R3410 7 FSB_CLK_CPU_N R3432 49.9

33 CK410_CPU2_ITP_SRC10_P 33 R3411 11 5 CPU_XDP_CLK_P MAKE_BASE=TRUE FSB_CLK_XDP_P R3433 49.9

33 CK410_CPU2_ITP_SRC10_N 33 R3412 11 5 CPU_XDP_CLK_N FSB_CLK_XDP_N MAKE_BASE=TRUE R3434 49.9

33 CK410_SRC6_P 33 R3413 53 AIRPORT_CLK100M_PCIE_P R3435 49.9

33 CK410_SRC6_N 33 R3414 53 AIRPORT_CLK100M_PCIE_N R3436 49.9

33 CK410_SRC5_P 33 R3415 14 NB_CLK100M_GCLKIN_P R3438 49.9

33 CK410_SRC5_N 33 R3416 14 NB_CLK100M_GCLKIN_N R3437 49.9

33 CK410_SRC4_P 33 R3417 21 5 SB_CLK100M_SATA_P R3439 49.9

33 CK410_SRC4_N 33 R3418 21 5 SB_CLK100M_SATA_N R3440 49.9

33 CK410_SRC2_P 33 R3419 22 SB_CLK100M_DMI_P R3442 49.9

33 CK410_SRC2_N 33 R3420 22 SB_CLK100M_DMI_N R3441 49.9

33 CK410_SRC8_P 33 R3421 41 ENET_CLK100M_PCIE_P R3443 49.9

33 CK410_SRC8_N 33 R3422 41 ENET_CLK100M_PCIE_N R3444 49.9

33 CK410_SRC1_P 33 R3423 85 GPU_CLK100M_PCIE_P R3446 49.9

33 CK410_SRC1_N 33 R3424 85 GPU_CLK100M_PCIE_N R3445 49.9

33 CK410_LVDS_P MAKE_BASE=TRUE TP_CK410_LVDS_P

33 CK410_LVDS_N MAKE_BASE=TRUE TP_CK410_LVDS_N

33 CK410_DOT96_27M_N MAKE_BASE=TRUE TP_CK410_27M_SPREAD

33 CK410_DOT96_27M_P MAKE_BASE=TRUE TP_CK410_27M_NONSPREAD

CLOCKS: TERMINATIONS

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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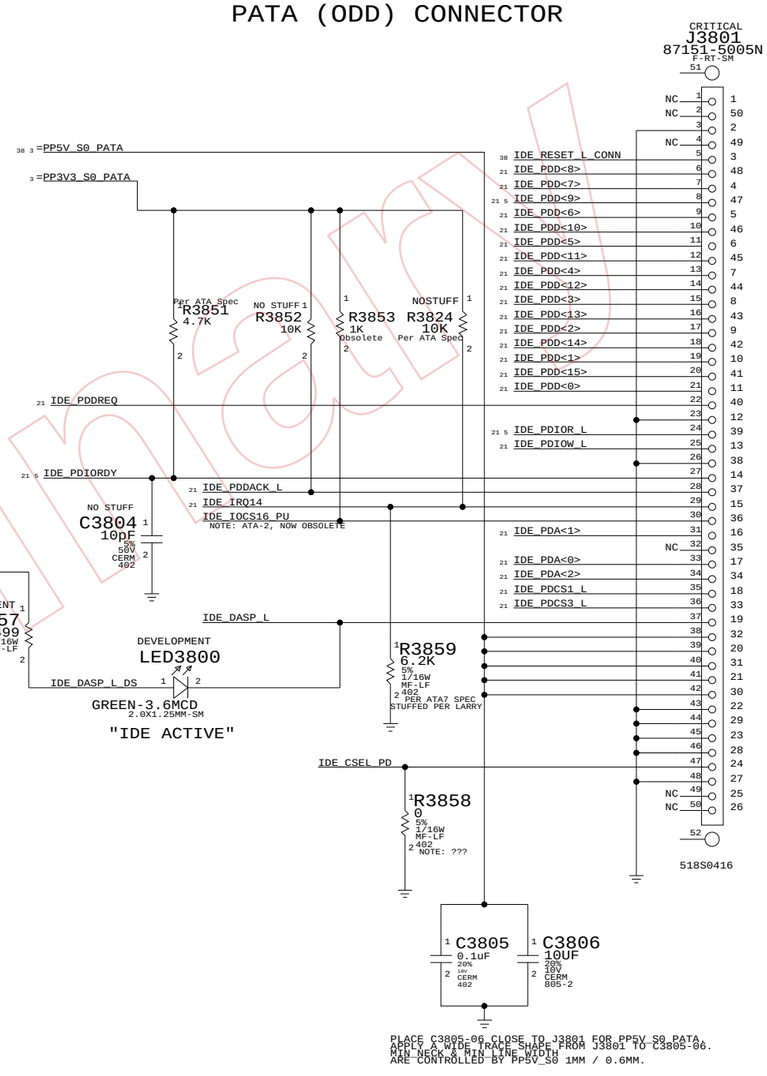
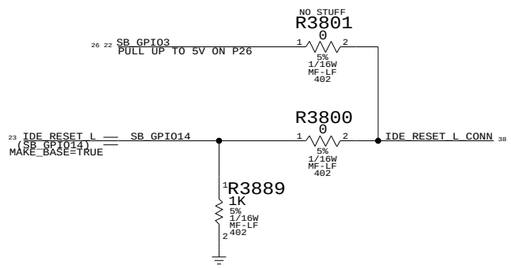
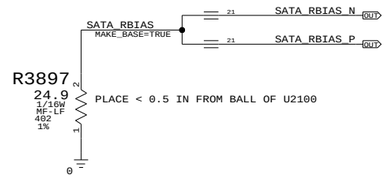
SCALE: NONE	SHT 34 OF 97	

PATA (ODD) CONNECTOR

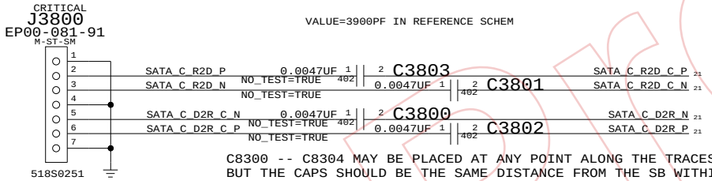


PLACE C3805-06 CLOSE TO J3801 FOR PP5V_S0_PATA.
APPLY A WIDE TRACE SHAPE FROM J3801 TO C3805-06.
MIN NECK & MIN LINE WIDTH
ARE CONTROLLED BY PP5V_S0 1MM / 0.6MM.

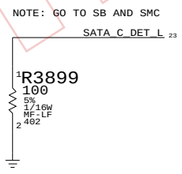


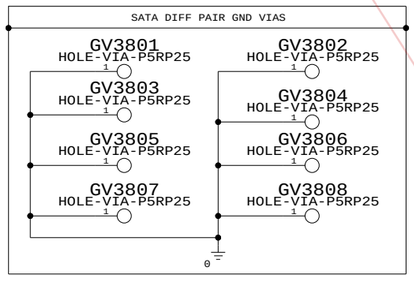


SATA CONNECTOR

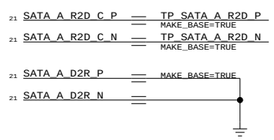


C8300 -- C8304 MAY BE PLACED AT ANY POINT ALONG THE TRACES
BUT THE CAPS SHOULD BE THE SAME DISTANCE FROM THE SB WITHIN EACH PAIR





SATA PORT 0 IS NOT USED



Disk Connectors

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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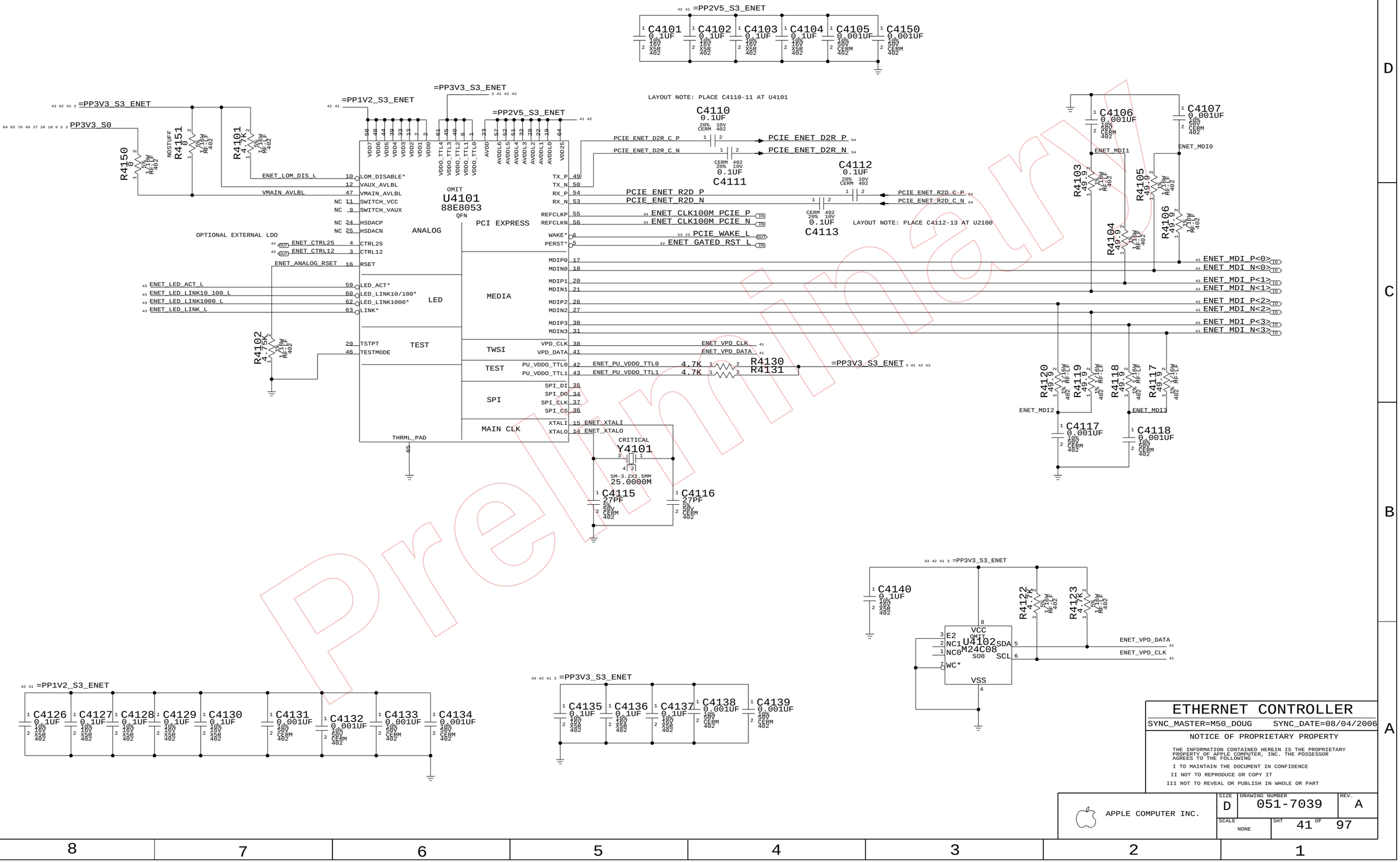
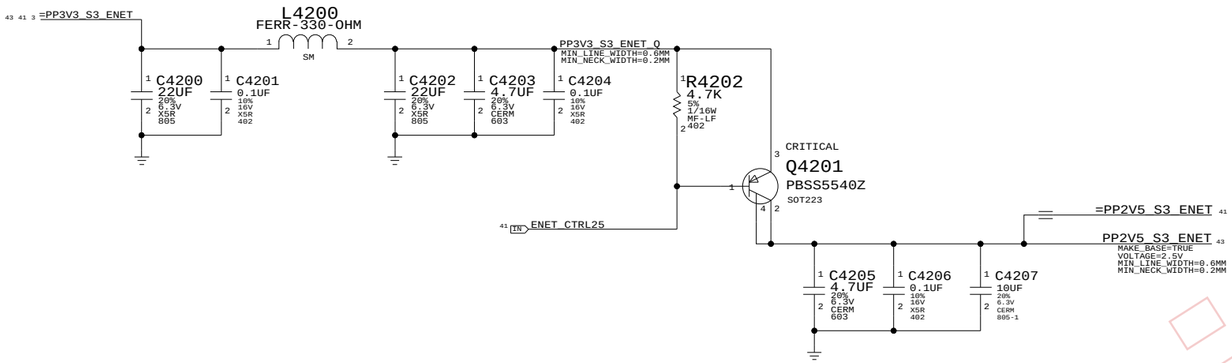
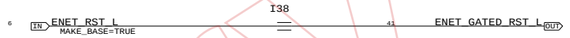
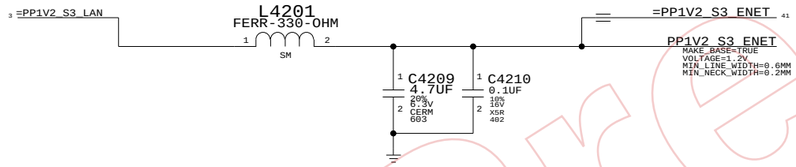
SCALE: NONE	SHT 38 OF 97	









ETHERNET MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED

42 PP2V5_S3_ENET — R4300 0 5% 1/8W MF-LF 805 — PP2V5_ENET_CTAP (MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.10mm, VOLTAGE=2.5V)

C4300 0.1UF 20% 10V CERM 402

C4301 0.001UF 10% 50V CERM 402

6 GND_CHASSIS_RJ45

C4304 0.001UF 10% 50V CERM 402

CRITICAL (514-0331)
J4300
RJ45-M51
F-ANG-TH

PRIMARY

13
11
5 ENET_CTAP
6 ENET_CTAP
1 MDI_0+
2 MDI_0-
3 MDI_1+
4 MDI_1-
7 MDI_2+
8 MDI_2-
9 MDI_3+
10 MDI_3-
12

1CT:1CT — 75 OHM (x4)

SECONDARY
J1
J2
J3
J4
J5
J6
J7
J8

RJ45 CABLE SIDE

RJ45 CHIP SIDE

SHIELD 1000PF, 2000V

41 ENET_MDI_P<0>
41 ENET_MDI_N<0>
41 ENET_MDI_P<1>
41 ENET_MDI_N<1>
41 ENET_MDI_P<2>
41 ENET_MDI_N<2>
41 ENET_MDI_P<3>
41 ENET_MDI_N<3>

MARVELL DOES NOT REQUIRE/RECOMMEND ANY SERIES TERMINATIONS HERE

C4305 0.001UF 10% 50V CERM 402

42 41 3 =PP3V3_S3_ENET

DEVELOPMENT R4301 330 5% 1/10W MF-LF 603 — LED4300_1
DEVELOPMENT R4302 330 5% 1/10W MF-LF 603 — LED4301_1
DEVELOPMENT R4303 330 5% 1/10W MF-LF 603 — LED4302_1
DEVELOPMENT R4304 330 5% 1/10W MF-LF 603 — LED4303_1

DEVELOPMENT LED4300 GREEN-3.0MCD 2.0X1.25MM-SM
DEVELOPMENT LED4301 GREEN-3.0MCD 2.0X1.25MM-SM
DEVELOPMENT LED4302 GREEN-3.0MCD 2.0X1.25MM-SM
DEVELOPMENT LED4303 GREEN-3.0MCD 2.0X1.25MM-SM

41 ENET_LED_ACT_L MAKE_BASE=TRUE
41 ENET_LED_LINK10_100_L MAKE_BASE=TRUE
41 ENET_LED_LINK1000_L MAKE_BASE=TRUE
41 ENET_LED_LINK_L MAKE_BASE=TRUE

ETHERNET CONNECTOR

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE

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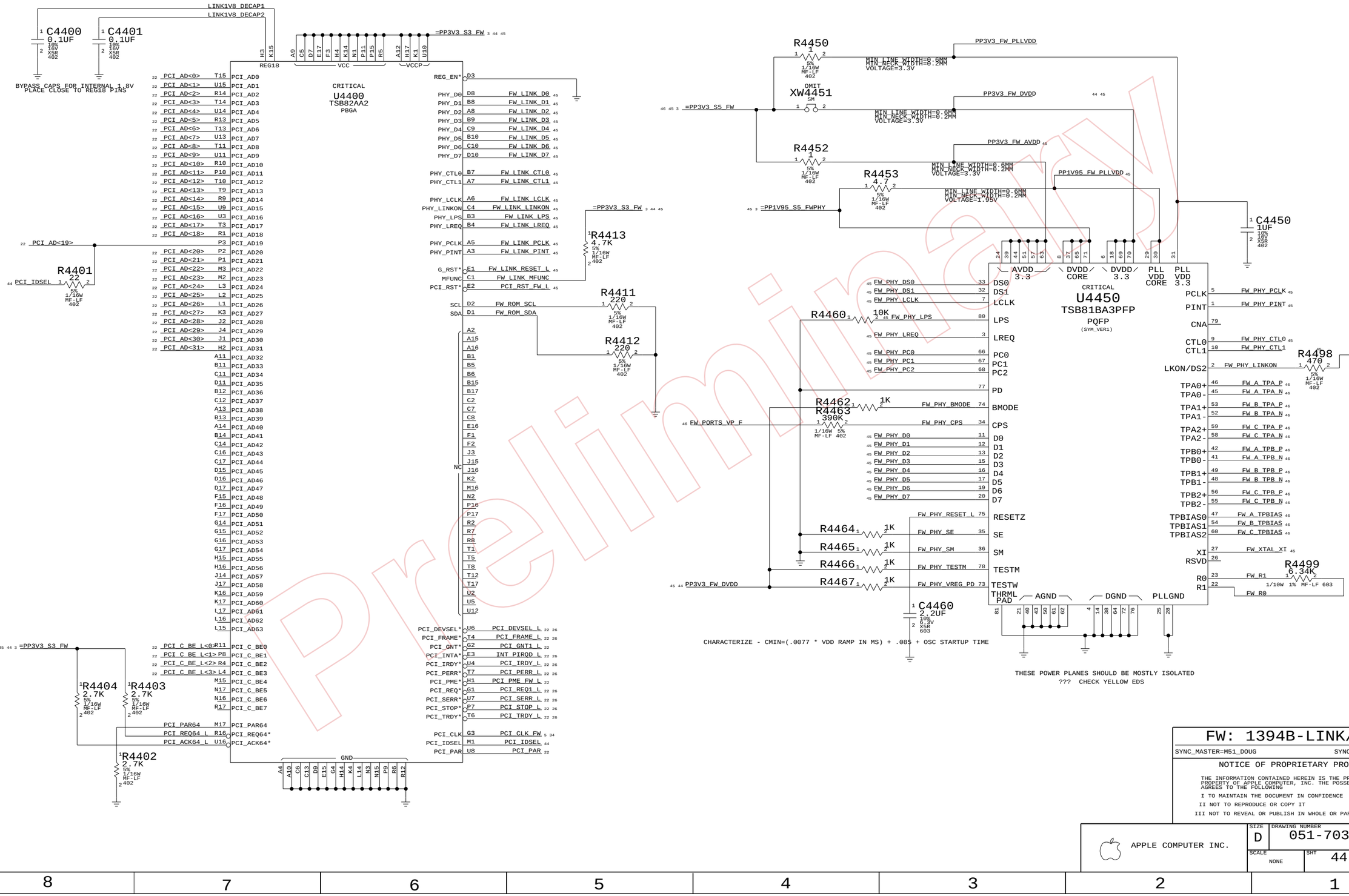
LINK1V8_DECAP1
LINK1V8_DECAP2
C4400 0.1UF 10% 10V X5R 402
C4401 0.1UF 10% 10V X5R 402
BYPASS CAPS FOR INTERNAL 1.8V
PLACE CLOSE TO REG18 PINS
REG18
=PP3V3_S3_FW
VCC
VCCP
CRITICAL
U4400
TSB82AA2
PBGA
PCI_AD<0> T15 PCI_AD0
PCI_AD<1> U15 PCI_AD1
PCI_AD<2> R14 PCI_AD2
PCI_AD<3> T14 PCI_AD3
PCI_AD<4> U14 PCI_AD4
PCI_AD<5> R13 PCI_AD5
PCI_AD<6> T13 PCI_AD6
PCI_AD<7> U13 PCI_AD7
PCI_AD<8> T11 PCI_AD8
PCI_AD<9> U11 PCI_AD9
PCI_AD<10> R10 PCI_AD10
PCI_AD<11> P10 PCI_AD11
PCI_AD<12> T10 PCI_AD12
PCI_AD<13> T9 PCI_AD13
PCI_AD<14> R9 PCI_AD14
PCI_AD<15> U9 PCI_AD15
PCI_AD<16> U3 PCI_AD16
PCI_AD<17> T3 PCI_AD17
PCI_AD<18> R1 PCI_AD18
PCI_AD<19> P3 PCI_AD19
PCI_AD<20> P2 PCI_AD20
PCI_AD<21> P1 PCI_AD21
PCI_AD<22> M3 PCI_AD22
PCI_AD<23> M2 PCI_AD23
PCI_AD<24> L3 PCI_AD24
PCI_AD<25> L2 PCI_AD25
PCI_AD<26> L1 PCI_AD26
PCI_AD<27> K3 PCI_AD27
PCI_AD<28> J2 PCI_AD28
PCI_AD<29> J4 PCI_AD29
PCI_AD<30> J1 PCI_AD30
PCI_AD<31> H2 PCI_AD31
A11 PCI_AD32
B11 PCI_AD33
C11 PCI_AD34
D11 PCI_AD35
B12 PCI_AD36
C12 PCI_AD37
A13 PCI_AD38
B13 PCI_AD39
A14 PCI_AD40
B14 PCI_AD41
C14 PCI_AD42
C16 PCI_AD43
C17 PCI_AD44
D15 PCI_AD45
D16 PCI_AD46
D17 PCI_AD47
F15 PCI_AD48
F16 PCI_AD49
F17 PCI_AD50
G14 PCI_AD51
G15 PCI_AD52
G16 PCI_AD53
G17 PCI_AD54
H15 PCI_AD55
H16 PCI_AD56
J14 PCI_AD57
J17 PCI_AD58
K16 PCI_AD59
K17 PCI_AD60
L17 PCI_AD61
L16 PCI_AD62
L15 PCI_AD63
R4401 22 5% 1/16W MF-LF 402
PCI_IDSEL
REG_EN*
PHY_D0 FW_LINK_D0
PHY_D1 FW_LINK_D1
PHY_D2 FW_LINK_D2
PHY_D3 FW_LINK_D3
PHY_D4 FW_LINK_D4
PHY_D5 FW_LINK_D5
PHY_D6 FW_LINK_D6
PHY_D7 FW_LINK_D7
PHY_CTL0 FW_LINK_CTL0
PHY_CTL1 FW_LINK_CTL1
PHY_LCLK FW_LINK_LCLK
PHY_LINKON FW_LINK_LINKON
PHY_LPS FW_LINK_LPS
PHY_LREQ FW_LINK_LREQ
PHY_PCLK FW_LINK_PCLK
PHY_PINT FW_LINK_PINT
G_RST* FW_LINK_RESET_L
MFUNC FW_LINK_MFUNC
PCI_RST* PCI_RST_FW_L
R4413 4.7K 5% 1/16W MF-LF 402
R4411 220 5% 1/16W MF-LF 402
R4412 220 5% 1/16W MF-LF 402
SCL FW_ROM_SCL
SDA FW_ROM_SDA
NC
PCI_C_BE<0> R11 PCI_C_BE0
PCI_C_BE<1> P8 PCI_C_BE1
PCI_C_BE<2> R4 PCI_C_BE2
PCI_C_BE<3> L4 PCI_C_BE3
M15 PCI_C_BE4
N17 PCI_C_BE5
N16 PCI_C_BE6
R17 PCI_C_BE7
PCI_PAR64 M17 PCI_PAR64
PCI_REQ64_L R16 PCI_REQ64*
PCI_ACK64_L U16 PCI_ACK64*
PCI_DEVSEL* U6 PCI_DEVSEL_L
PCI_FRAME* T4 PCI_FRAME_L
PCI_GNT* G2 PCI_GNT1_L
PCI_INTA* E3 INT_PIRQD_L
PCI_IRDY* U4 PCI_IRDY_L
PCI_PERR* T7 PCI_PERR_L
PCI_PME* H1 PCI_PME_FW_L
PCI_REQ* G1 PCI_REQ1_L
PCI_SERR* U7 PCI_SERR_L
PCI_STOP* P7 PCI_STOP_L
PCI_TRDY* T6 PCI_TRDY_L
PCI_CLK G3 PCI_CLK_FW
PCI_IDSEL M1 PCI_IDSEL
PCI_PAR U8 PCI_PAR
R4404 2.7K 5% 1/16W MF-LF 402
R4403 2.7K 5% 1/16W MF-LF 402
R4402 2.7K 5% 1/16W MF-LF 402
=PP3V3_S3_FW
GND
R4450 1 5% 1/10W MF-LF 402
PP3V3_FW_PLLVDD
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
OMIT
XW4451
SM
=PP3V3_S5_FW
PP3V3_FW_DVDD
R4452 1 5% 1/10W MF-LF 402
PP3V3_FW_AVDD
R4453 4.7 5% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.95V
PP1V95_FW_PLLVDD
=PP1V95_S5_FWPHY
C4450 1UF 10% 10V X5R 402
AVDD 3.3
DVDD CORE
DVDD 3.3
PLL VDD CORE 3.3
PLL VDD 3.3
CRITICAL
U4450
TSB81BA3PFP
PQFP
(SYM_VER1)
DS0 FW_PHY_DS0
DS1 FW_PHY_DS1
LCLK FW_PHY_LCLK
LPS FW_PHY_LPS
LREQ FW_PHY_LREQ
PC0 FW_PHY_PC0
PC1 FW_PHY_PC1
PC2 FW_PHY_PC2
PD
BMODE FW_PHY_BMODE
CPS FW_PHY_CPS
D0 FW_PHY_D0
D1 FW_PHY_D1
D2 FW_PHY_D2
D3 FW_PHY_D3
D4 FW_PHY_D4
D5 FW_PHY_D5
D6 FW_PHY_D6
D7 FW_PHY_D7
RESETZ FW_PHY_RESET_L
SE FW_PHY_SE
SM FW_PHY_SM
TESTM FW_PHY_TESTM
TESTW FW_PHY_VREG_PD
THRML PAD
AGND
DGND
PLLGND
PCLK FW_PHY_PCLK
PINT FW_PHY_PINT
CNA
CTL0 FW_PHY_CTL0
CTL1 FW_PHY_CTL1
LKON/DS2 FW_PHY_LINKON
TPA0+ FW_A_TPA_P
TPA0- FW_A_TPA_N
TPA1+ FW_B_TPA_P
TPA1- FW_B_TPA_N
TPA2+ FW_C_TPA_P
TPA2- FW_C_TPA_N
TPB0+ FW_A_TPB_P
TPB0- FW_A_TPB_N
TPB1+ FW_B_TPB_P
TPB1- FW_B_TPB_N
TPB2+ FW_C_TPB_P
TPB2- FW_C_TPB_N
TPBIAS0 FW_A_TPBIAS
TPBIAS1 FW_B_TPBIAS
TPBIAS2 FW_C_TPBIAS
XI FW_XTAL_XI
RSVD
R0 FW_R1
R1 FW_R0
R4460 10K FW_PHY_LPS
R4462 1K FW_PHY_BMODE
R4463 390K 1/16W 5% MF-LF 402
FW_PORTS_VP_F
R4464 1K FW_PHY_SE
R4465 1K FW_PHY_SM
R4466 1K FW_PHY_TESTM
R4467 1K FW_PHY_VREG_PD
PP3V3_FW_DVDD
C4460 2.2UF 10% 6.3V X5R 603
R4498 470 5% 1/10W MF-LF 402
PP3V3_FW_DVDD
R4499 6.34K 1/10W 1% MF-LF 603
CHARACTERIZE - CMIN=(.0077 * VDD RAMP IN MS) + .085 + OSC STARTUP TIME
THESE POWER PLANES SHOULD BE MOSTLY ISOLATED
??? CHECK YELLOW EDS
FW: 1394B-LINK/PHY
SYNC_MASTER=M51_DOUG
SYNC_DATE=08/04/2006
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APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7039
REV. A
SCALE NONE
SHT 44 OF 97

1394 PHY DATA/STROBE AND POWER CLASS OPTIONS

45 44 PP3V3_FW_DVDD

NOSTUFF R4550 1K 5% 1/16W MF-LF 402
NOSTUFF R4551 1K 5% 1/16W MF-LF 402
R4570 1K 5% 1/16W MF-LF 402
NOSTUFF R4571 1K 5% 1/16W MF-LF 402
NOSTUFF R4572 1K 5% 1/16W MF-LF 402

44 FW_PHY_DS0
44 FW_PHY_DS1
44 FW_PHY_PC0
44 FW_PHY_PC1
44 FW_PHY_PC2

NOSTUFF R4560 1K 5% 1/16W MF-LF 402
NOSTUFF R4561 1K 5% 1/16W MF-LF 402
NOSTUFF R4580 1K 5% 1/16W MF-LF 402
NOSTUFF R4581 1K 5% 1/16W MF-LF 402
NOSTUFF R4582 1K 5% 1/16W MF-LF 402

1394 PHY 1.95V REGULATOR

46 44 3 =PP3V3_S5_FW

CRITICAL
U4501 LT1762EMS8 MSOP
IN 8
OUT 1
NC 7
NC 6
SHDN* 5
SENSE/ADJ* 2
BYP 3
GND
353S1403

C4500 2.2UF 10% 6.3V X5R 603
C4503 0.01UF 20% 16V CERM 402
R4500 16.2K 1% 1/16W MF-LF 402
R4501 27.4K 1% 1/16W MF-LF 402
C4501 10UF 20% 6.3V X5R 603

V_ADJ
V_BYP
PP1V95_S5 3

VOUT = 1.22V * (1 + R4500 / R4501) + (Iadj * R4500)
Iadj = 30nA @ 25 deg C
VOUT = 1.946V

1394 PHY CRYSTAL OSCILLATOR

FIXME!!! CHARACTERIZE TO SEE IF THIS BRINGS US CLOSE ENOUGH TO 1.8V - 4.7 CHOSEN FOR BOM CONSOLIDATION

PP1V8X_FW_XTAL
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.95V

45 44 PP1V95_FW_PLLVDD
R4502 4.7 5% 1/16W MF-LF 402

NOSTUFF R4503 100K 5% 1/16W MF-LF 402
C4502 0.22UF 20% 6.3V X5R 402
CRITICAL
G4500 98P3040MHZ SM
VCC
FW_OSC_EN
TRI-ST/NC
OUT
GND
197S0179
FW_XTAL_XI 44

LINK DECOUPLING

45 44 3 =PP3V3_S3_FW

C4550 C4551 C4552 C4553 C4554 C4555 C4556 C4557 C4558 C4559 C4560 C4561
1UF 10% 6.3V CERM 402

NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4400

1394 LINK POWER ON RESET AND PCI RESET

22 PCI_RST_L — R4595 150 1% 1/16W MF-LF 402 — PCI_RST_FW_L 44

NOTE: 1% FOR BOM CONSOLIDATION(APPLIED TO M50)
NOTE: R SHOULD BE CHOSEN TO PREVENT OVERSHOOT

=PP3V3_S3_FW
R4591 10K 5% 1/16W MF-LF 402
R4590 10K 5% 1/16W MF-LF 402
58 SMC_RSTGATE_L — SMC_RSTGATE_RC_L
Q4500 2N7002DW-X-F SOT-363
FW_LINK_RESET_L 44
C4590 0.001UF 10% 50V CERM 402
FW_PLT_RST_L
NOSTUFF C4591 0.001UF 10% 50V CERM 402
84 83 76 41 27 26 10 6 5 3 PP3V3_S0
R4592 100K 5% 1/16W MF-LF 402
Q4510 2N7002DW-X-F SOT-363
PLT_RST_FW
Q4510 2N7002DW-X-F SOT-363
6 FW_RST_L

PHY DECOUPLING

44 3 =PP1V95_S5_FWPHY
C4510 C4511 C4512 C4513 1UF 10% 6.3V CERM 402

45 44 PP3V3_FW_DVDD
C4520 C4521 C4522 C4523 1UF 10% 6.3V CERM 402

45 44 PP1V95_FW_PLLVDD
C4530 C4531 1UF 10% 6.3V CERM 402

44 PP3V3_FW_AVDD
C4540 C4541 C4542 C4543 C4544 C4545 1UF 10% 6.3V CERM 402

NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4450

44 FW_LINK_D0 — MAKE_BASE=TRUE — FW_PHY_D0 44
44 FW_LINK_D1 — MAKE_BASE=TRUE — FW_PHY_D1 44
44 FW_LINK_D2 — MAKE_BASE=TRUE — FW_PHY_D2 44
44 FW_LINK_D3 — MAKE_BASE=TRUE — FW_PHY_D3 44
44 FW_LINK_D4 — MAKE_BASE=TRUE — FW_PHY_D4 44
44 FW_LINK_D5 — MAKE_BASE=TRUE — FW_PHY_D5 44
44 FW_LINK_D6 — MAKE_BASE=TRUE — FW_PHY_D6 44
44 FW_LINK_D7 — MAKE_BASE=TRUE — FW_PHY_D7 44
44 FW_LINK_CTL0 — MAKE_BASE=TRUE — FW_PHY_CTL0 44
44 FW_LINK_CTL1 — MAKE_BASE=TRUE — FW_PHY_CTL1 44
44 FW_LINK_LCLK — MAKE_BASE=TRUE — FW_PHY_LCLK 44
44 FW_LINK_LPS — MAKE_BASE=TRUE — FW_PHY_LPS 44
44 FW_LINK_LREQ — MAKE_BASE=TRUE — FW_PHY_LREQ 44
44 FW_LINK_PCLK — MAKE_BASE=TRUE — FW_PHY_PCLK 44

R4520 1K
44 FW_LINK_LINKON — FW_PHY_LINKON 44
NOTE: 1K IS PER TI SPEC TO BALANCE OUT THE 470 PULLUP ON DS2

44 FW_LINK_PINT — MAKE_BASE=TRUE — FW_PHY_PINT 44

NORMALLY TERMINATIONS WOULD GO HERE...
SIMULATIONS SHOW THAT THERMINATIONS WERE NOT NEEDED FOR M51
CONSTRAIN NETS TO 200-250PS IF NO TERM-Rs...

FW: 1394B MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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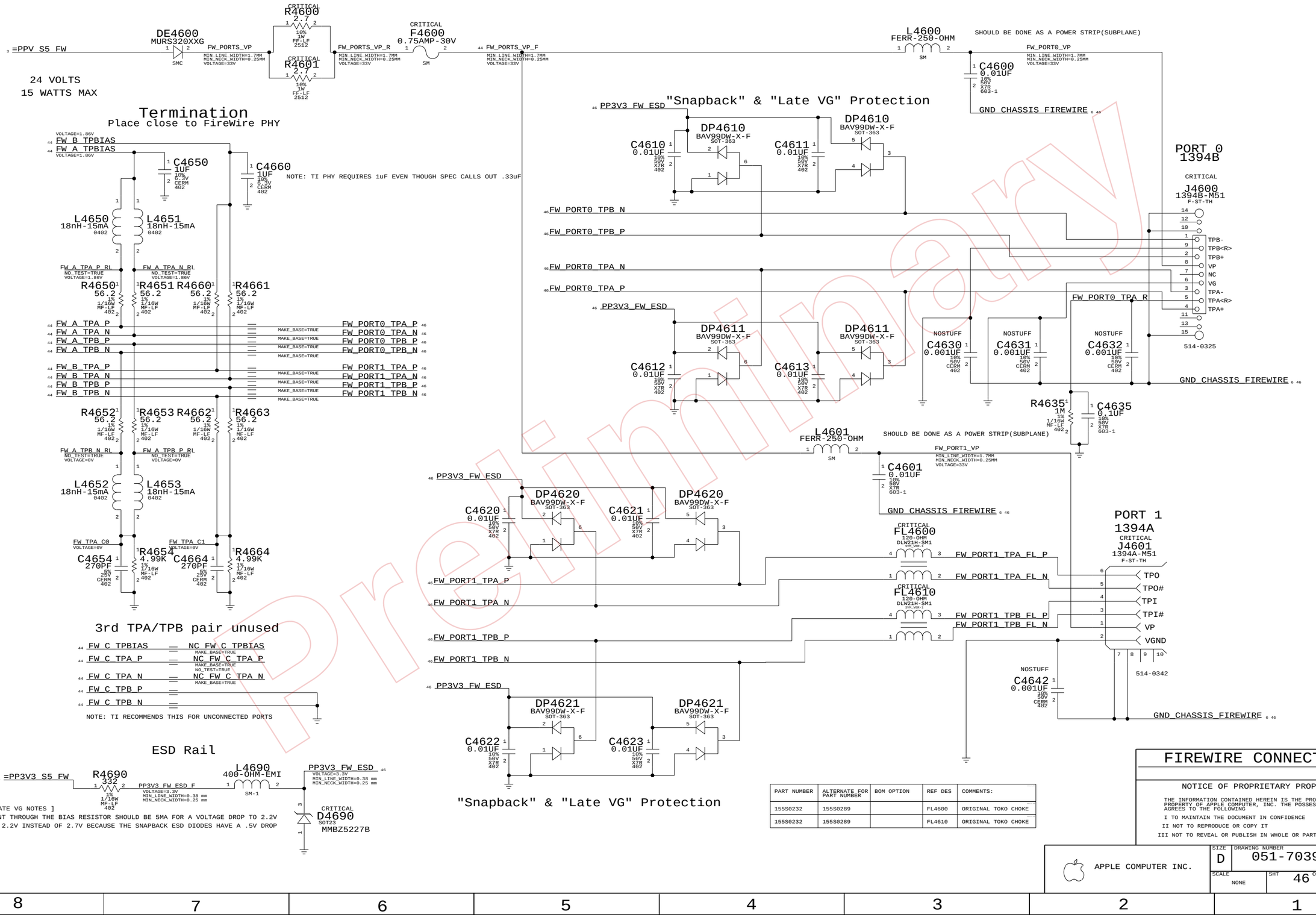
SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 45 OF 97	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		FL4600	ORIGINAL TOKO CHOKE
155S0232	155S0289		FL4610	ORIGINAL TOKO CHOKE

FIREWIRE CONNECTORS

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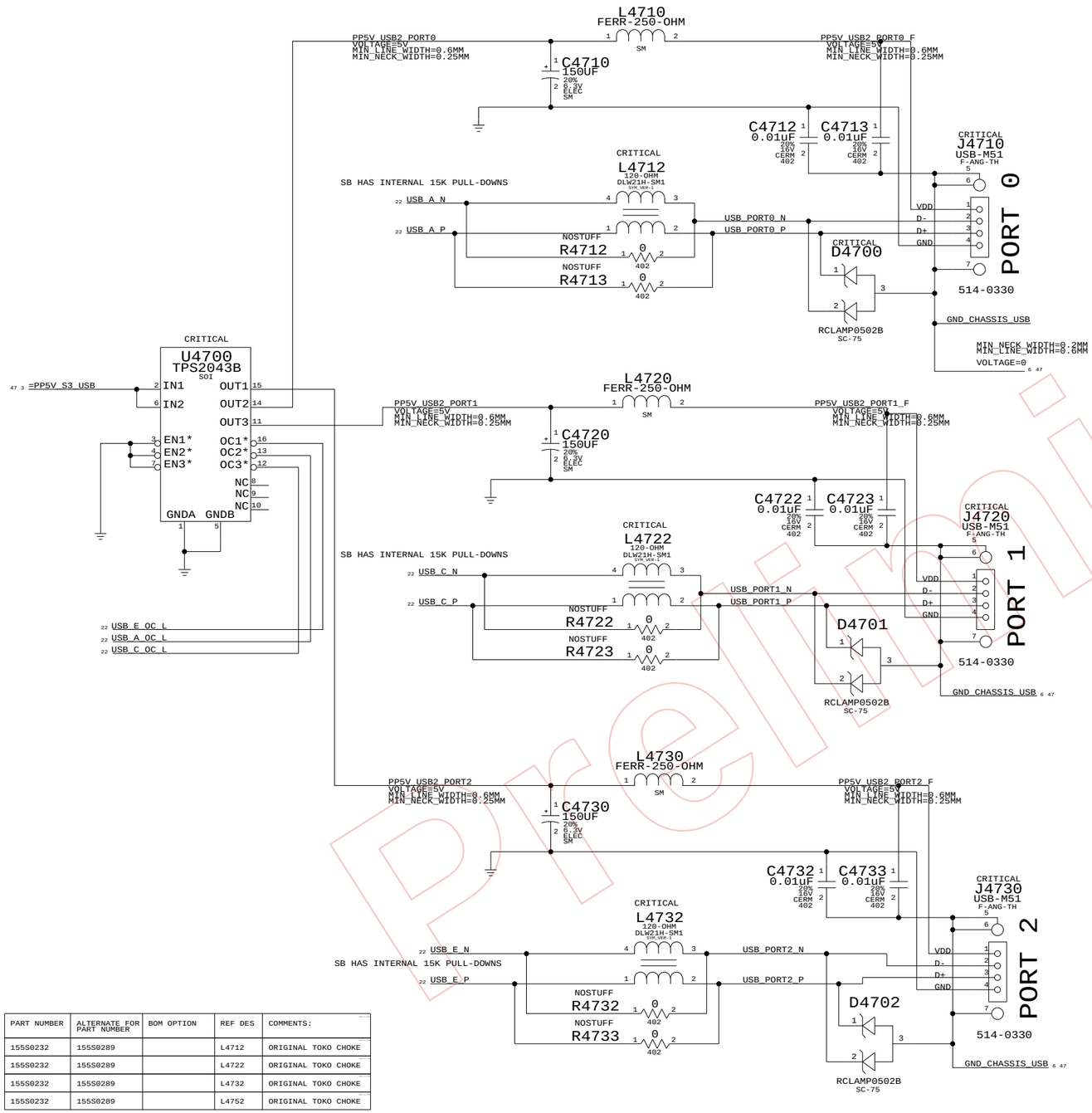
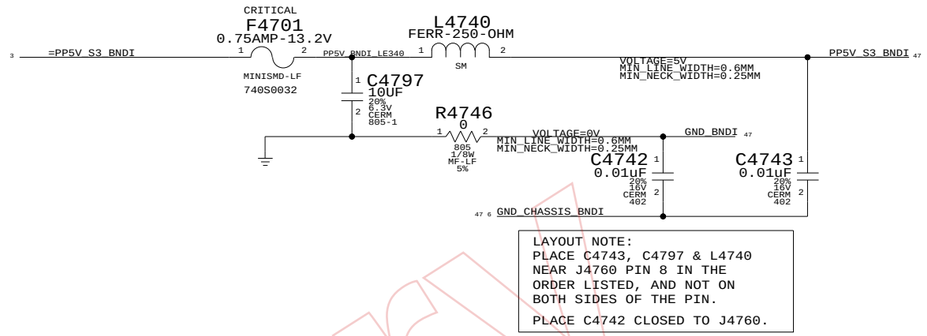
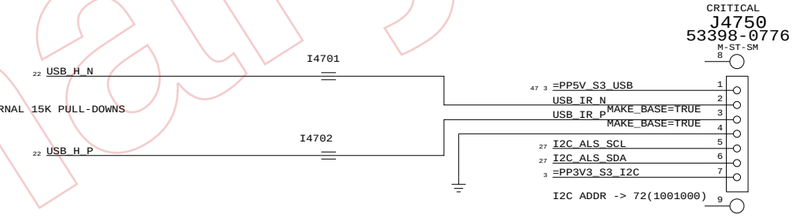
External USB Ports



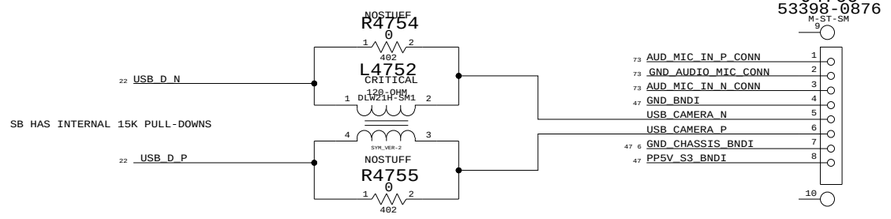
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		L4712	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4722	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4732	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4752	ORIGINAL TOKO CHOKE



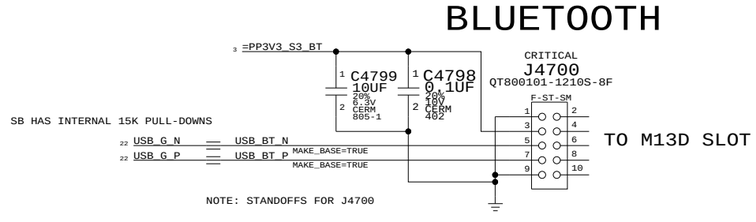
IR RECEIVER & ALS



CAMERA & MIC



BLUETOOTH



USB Device Interfaces

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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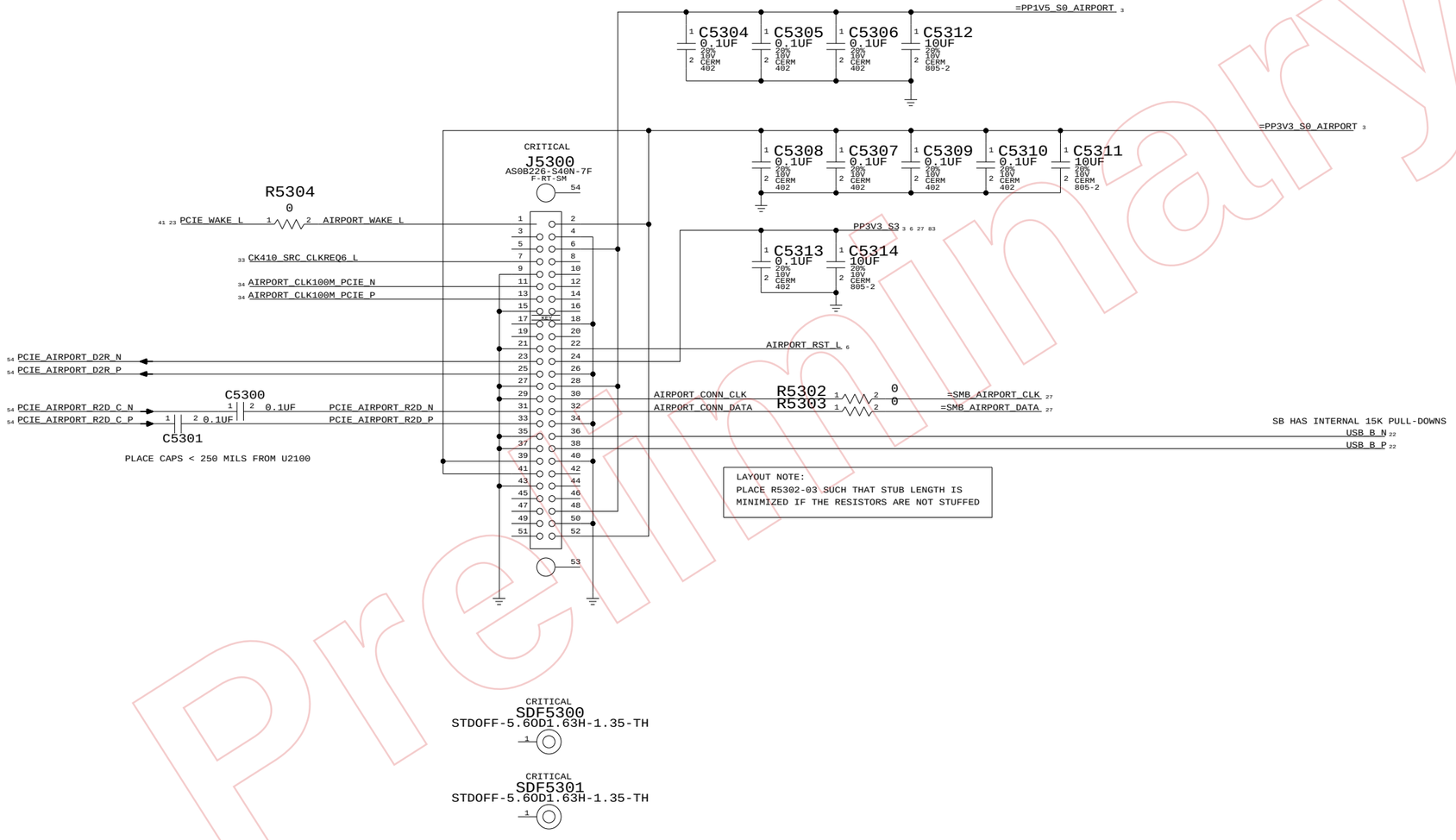
SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 47 OF 97	



AIRPORT CONN

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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SCALE: NONE	SHT 53 OF 97	

PCI-E X1 PORT "A" = ETHERNET (YUKON)

22 PCIE_A_R2D_C_N — PCIE_ENET_R2D_C_N 41
MAKE_BASE=TRUE
22 PCIE_A_R2D_C_P — PCIE_ENET_R2D_C_P 41
MAKE_BASE=TRUE

22 PCIE_A_D2R_N — PCIE_ENET_D2R_N 41
MAKE_BASE=TRUE
22 PCIE_A_D2R_P — PCIE_ENET_D2R_P 41
MAKE_BASE=TRUE

PCI-E X1 PORT "B" = MINI CARD (AIRPORT)

22 PCIE_B_R2D_C_N — PCIE_AIRPORT_R2D_C_N 53
MAKE_BASE=TRUE
22 PCIE_B_R2D_C_P — PCIE_AIRPORT_R2D_C_P 53
MAKE_BASE=TRUE

22 5 PCIE_B_D2R_N — PCIE_AIRPORT_D2R_N 53
MAKE_BASE=TRUE
22 5 PCIE_B_D2R_P — PCIE_AIRPORT_D2R_P 53
MAKE_BASE=TRUE

PCI-E X1 PORTS C, D, E, F = UNUSED

22 PCIE_C_R2D_C_N — TP_PCIE_C_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_C_R2D_C_P — TP_PCIE_C_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_C_D2R_N — TP_PCIE_C_D2R_N
MAKE_BASE=TRUE
22 PCIE_C_D2R_P — TP_PCIE_C_D2R_P
MAKE_BASE=TRUE

22 PCIE_D_R2D_C_N — TP_PCIE_D_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_D_R2D_C_P — TP_PCIE_D_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_D_D2R_N — TP_PCIE_D_D2R_N
MAKE_BASE=TRUE
22 PCIE_D_D2R_P — TP_PCIE_D_D2R_P
MAKE_BASE=TRUE

22 PCIE_E_R2D_C_N — TP_PCIE_E_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_E_R2D_C_P — TP_PCIE_E_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_E_D2R_N — TP_PCIE_E_D2R_N
MAKE_BASE=TRUE
22 PCIE_E_D2R_P — TP_PCIE_E_D2R_P
MAKE_BASE=TRUE

22 PCIE_F_R2D_C_N — TP_PCIE_F_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_F_R2D_C_P — TP_PCIE_F_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_F_D2R_N — TP_PCIE_F_D2R_N
MAKE_BASE=TRUE
22 PCIE_F_D2R_P — TP_PCIE_F_D2R_P
MAKE_BASE=TRUE

PCI-E CONNECTIONS

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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D	051-7039	A
SCALE: NONE	SHT 54 OF 97	

UNUSED PINS HAVE THE FORMAT
SMC_XXX WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

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23 OUT	PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	59	SMC_PM_G2_EN OUT
45 OUT	SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	59	SMC_ADAPTER_EN OUT
84 77 26 5 IN	ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	22	SPI_ARB IN
76 IN	RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	63 22	SPI_SCLK IN
23 OUT	SMC_SB_NMI	B15	P14	P64/KIN4*	K13	63 22 5	SPI_SI OUT
23 OUT	PM_RSMRST_L	C14	P15	P65/KIN5*	K14	63 22 5	SPI_SO IN
75 OUT	IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	59	SMC_PROCHOT_3_3_L IN
23 OUT	PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	59	SMC_CPU_INIT_3_3_L IN
59	SMC_P20	D13	P20	P70/AN0	N12	76	SMC_CPU_ISENSE IN
59	SMC_P21	D14	P21	P71/AN1	R13	76	SMC_CPU_VSENSE IN
59	SMC_P22	D15	P22	P72/AN2	P13	84	SMC_GPU_ISENSE IN
59	SMC_P23	E12	P23	P73/AN3	R14	84	SMC_GPU_VSENSE IN
59 OUT	SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	76	SMC_DCIN_ISENSE IN
59 OUT	SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	76	SMC_PBUS_VSENSE IN
59	SMC_P26	E13	P26	P76/AN6	N13	59	SMC_BATT_ISENSE IN
59	SMC_P27	F14	P27	P77/AN7	P15	59	SMC_FWIRE_ISENSE IN
67 60 21 5 IO	LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	23	SMC_WAKE_SCI_L IN
67 60 21 5 IO	LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	59	SMC_TPM_GPIO OUT
67 60 21 5 IO	LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	67 60 23 5	PM_CLKRUN_L IO
67 60 21 5 IO	LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	67 60 23 5	PM_SUS_STAT_L IN
67 60 21 5 IN	LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	59	SC_TX_L OUT
6 IN	SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	59	SC_RX_L IN
34 5 IN	PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	27	SMB_BSB_CLK IO
67 60 23 5 OUT	INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	59	SMC_ONOFF_L IN
59 OUT	SMC_XDP_TMS	A5	P40/TMI0	P91/IRQ1*	J2	59	SMC_BC_ACOK IN
59 OUT	SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	59	SMC_BS_ALRT_L IN
27 IO	SMB_BSB_DATA	D5	P42/SDA1	P93/IRQ12*	J3	80 79 77 23 5	PM_SLP_S3_L IN
59 OUT	SMC_TPM_PP	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	77 23 5	PM_SLP_S4_L IN
59 OUT	SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	23	PM_SLP_S5_L IN
59 OUT	SMC_XDP_TCK	C2	P45	P96/EXCL	H1	59	SMC_SUS_CLK IN
59 OUT	SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	27	SMB_0_S0_DATA IO
59 OUT	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1				
60 59 5 OUT	SMC_TX_L	G1	P50				
60 59 5 IN	SMC_RX_L	G4	P51				
27 IO	SMB_0_S0_CLK	F2	P52/SCL0				

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21 OUT	SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3	59	SMC_CASE_OPEN IN
60 22 5 IN	BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	60 59 5	SMC_TCK IN
26 23 IN	PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	60 59 5	SMC_TDI IN
67 59 OUT	SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	60 59 5	SMC_TDO OUT
59 14 IN	PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	60 59 5	SMC_TMS IN
23 10 IO	PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7		SMC_PF0 59
59 IO	SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6		SMC_PF1 59
23 OUT	PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	59	SMC_LID IN
23 IN	SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	59	SMC_CPU_RESET_3_3_L IN
23 OUT	SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	59	SMC_BATT_ISET OUT
50 IN	SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	59	SMC_BATT_VSET OUT
76 5 OUT	ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	59	SMC_SYS_ISET OUT
59 IN	SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	59	SMC_SYS_VSET OUT
59 OUT	SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	63 22	SPI_CE_L IO
55 IN	SMC_EXCARD_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	59	SMC_XDP_TCK_3_3 IN
59 IN	SMC_XDP_TDO_3_3	D11	PB7	PG2/EXIRQ10*/SDA2	N9	27	SMB_BSA_DATA IO
65 OUT	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	27	SMB_BSA_CLK IO
65 OUT	SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	27	SMB_A_S3_DATA IO
66 OUT	SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	27	SMB_A_S3_CLK IO
59 OUT	SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	27	SMB_B_S0_DATA IO
65 IN	SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	27	SMB_B_S0_CLK IO
65 IN	SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	59	SMC_PROCHOT OUT
66 IN	SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	59	SMC_THRMTRIP OUT
59 IN	SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	59	SMC_FWE IN
59 IN	SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	59	ALS_GAIN OUT
59 IN	SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	26 23	SMS_INT_L OUT
59 IN	SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	59	SMS_ONOFF_L OUT
59 IN	SMC_ANALOG_ID	N11	PD3/AN11				
59 IN	SMC_NB_ISENSE	P10	PD4/AN12				
59 IN	SMC_MEM_ISENSE	R10	PD5/AN13				
59 IN	ALS_LEFT	N10	PD6/AN14				
59 IN	ALS_RIGHT	M10	PD7/AN15				

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G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

59 58 27 3 =PP3V3_S5_SMC

C5802 22UF 20% 6.3V X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
VCL IS INTERNAL RAIL
C5807 0.47UF 10% 6.3V CERM-X5R 402

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

59 58 27 3 =PP3V3_S5_SMC
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
C5820 0.1UF 20% 10V CERM 402
84 76 59 58 GND_SMC_AVSS

PP3V3_AVREF_SMC 59
59 58 27 3 =PP3V3_S5_SMC

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U5800
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AVCC1 N14
AVCC2 N15
VCC1 P2
VCC2 P1
VCC3 J15
VCC4 A1
VCC5 F1
AVREF M14
AVREF M15

60 59 5 IN SMC_RST_L → RES* E3
59 SMC_XTAL → XTAL A2
59 SMC_EXTAL → EXTAL B2

MD1 F2 → SMC_MD1 5 60
MD2 K1 → KBC_MDE
NMI F4 → SMC_NMI IN
ETRST* L1 → SMC_TRST_L IN

VSS: D1 F4 R4 F12 F13 B13 A13 A4 B4 D2
AVSS P12 R12

R5809 10K 5% 1/16W MF-LF 2402
R5801 10K 5% 1/16W MF-LF 2402
NOSTUFF
R5898 10K 5% 1/16W MF-LF 2402
R5803 0 5% 1/16W MF-LF 2402
R5802 10K 5% 1/16W MF-LF 2402

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XW5800
SM
GND_SMC_AVSS 58 59 76 84

SMC

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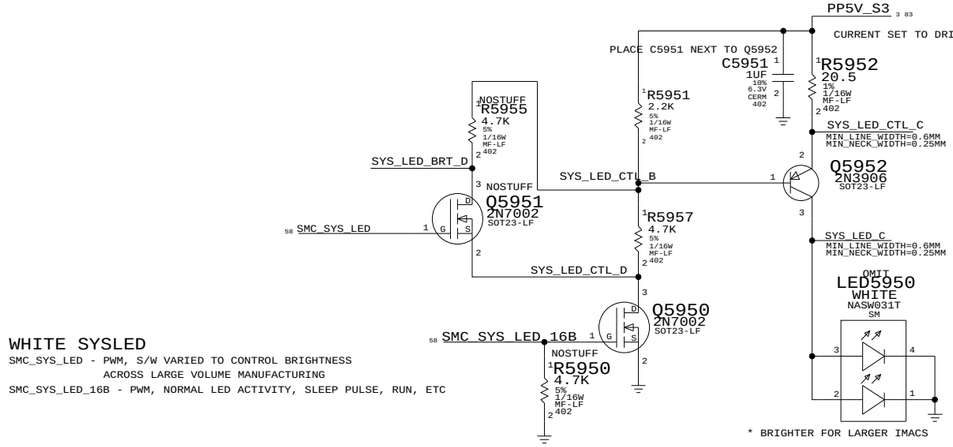
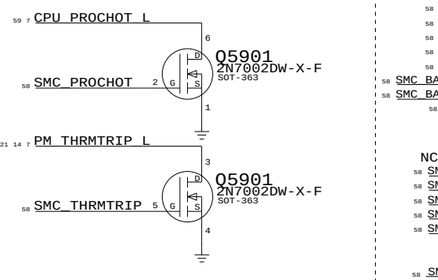
SCALE: NONE	SHT 58 OF 97	



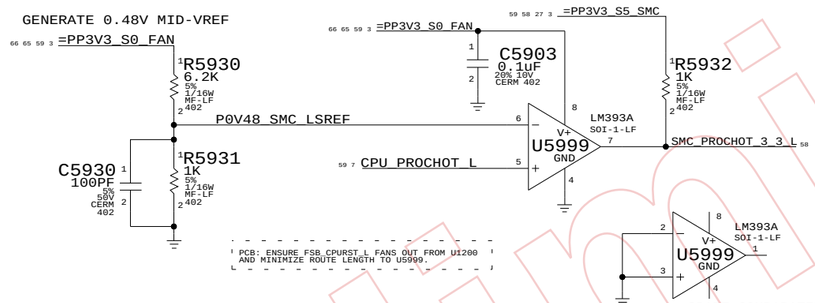
WHITE SYSLED

SMC_SYS_LED - PWM, S/W VARIED TO CONTROL BRIGHTNESS
ACROSS LARGE VOLUME MANUFACTURING
SMC_SYS_LED_16B - PWM, NORMAL LED ACTIVITY, SLEEP PULSE, RUN, ETC

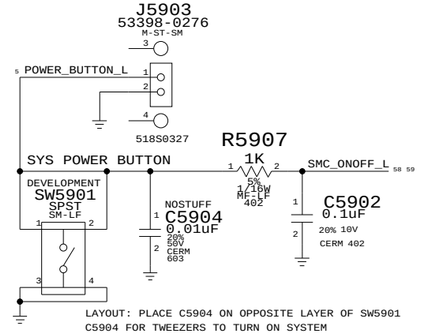
SMC 3.3V -> CPU 1.05V SHIFTER



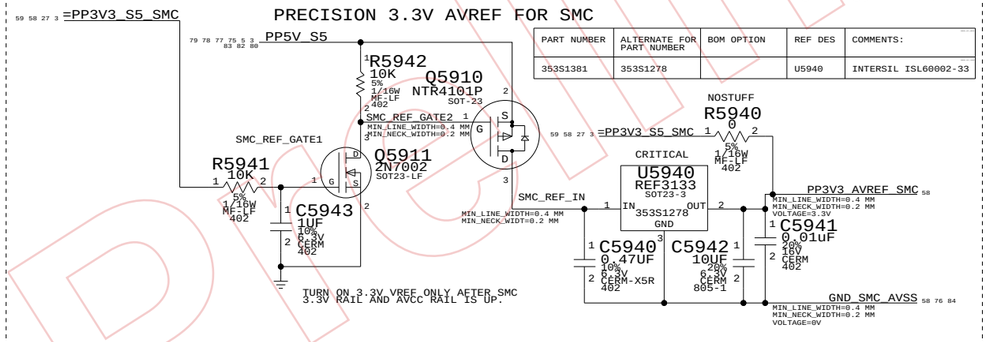
CPU 1.05V -> SMC 3.3V SHIFTER



POWER BUTTON HEADER

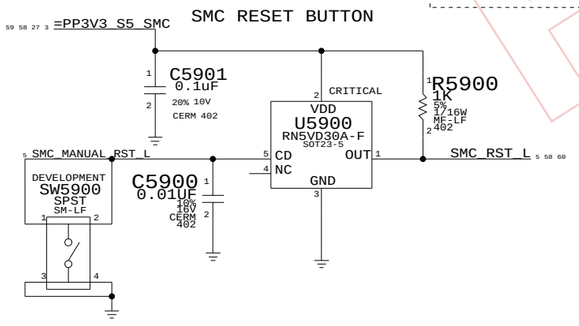


PRECISION 3.3V AVREF FOR SMC

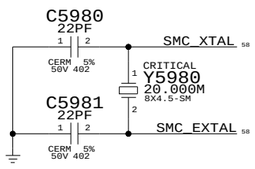


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		U5940	INTERSIL ISL60002-33

SMC RESET BUTTON

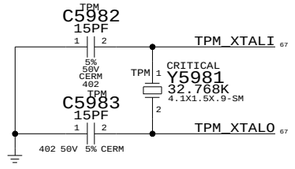


SMC CRYSTAL



TPM CRYSTAL

LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM



SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS

SMC_P20	NC_SMC_P20	MAKE_BASE=TRUE
SMC_P21	NC_SMC_P21	MAKE_BASE=TRUE
SMC_P22	NC_SMC_P22	MAKE_BASE=TRUE
SMC_P23	NC_SMC_P23	MAKE_BASE=TRUE
SMC_P26	NC_SMC_P26	MAKE_BASE=TRUE
SMC_P27	NC_SMC_P27	MAKE_BASE=TRUE
SMC_BATT_ISET	NC_SMC_BATT_ISET	MAKE_BASE=TRUE
SMC_BATT_VSET	NC_SMC_BATT_VSET	MAKE_BASE=TRUE
SMC_SYS_ISET	NC_SMC_SYS_ISET	MAKE_BASE=TRUE
SMC_SYS_VSET	NC_SMC_SYS_VSET	MAKE_BASE=TRUE
SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	MAKE_BASE=TRUE
SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN	MAKE_BASE=TRUE
ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE

DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS

SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE, FUNC_TEST=TRUE
SMC_PF0	TP_SMC_PF0	MAKE_BASE=TRUE
SMC_PM_G2_EN	TP_SMC_PM_G2_EN	MAKE_BASE=TRUE, FUNC_TEST=TRUE
SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN	MAKE_BASE=TRUE, FUNC_TEST=TRUE
ALS_LEFT	TP_ALS_LEFT	MAKE_BASE=TRUE, FUNC_TEST=TRUE
ALS_RIGHT	TP_ALS_RIGHT	MAKE_BASE=TRUE
SMC_PF1	TP_SMC_PF1	MAKE_BASE=TRUE
SMC_XDP_TCK	TP_SMC_XDP_TCK	MAKE_BASE=TRUE
SMC_XDP_TRST_L	TP_SMC_XDP_TRST_L	MAKE_BASE=TRUE
SMC_PB7	TP_SMC_PB7	MAKE_BASE=TRUE, FUNC_TEST=TRUE

NC OR PULLDOWN UNUSED ANALOG SENSE PINS

SMS_X_AXIS	NC_SMS_X_AXIS
SMS_Y_AXIS	NC_SMS_Y_AXIS
SMS_Z_AXIS	NC_SMS_Z_AXIS
SMC_NB_ISENSE	NC_SMC_NB_ISENSE
SMC_MEM_ISENSE	NC_SMC_MEM_ISENSE

SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE, FUNC_TEST=TRUE
SMC_PB7	TP_SMC_PB7	MAKE_BASE=TRUE, FUNC_TEST=TRUE
SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH	MAKE_BASE=TRUE, FUNC_TEST=TRUE
SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL	MAKE_BASE=TRUE, FUNC_TEST=TRUE

SMC_FWIRE_ISENSE	UNUSED_SMC_SENSE
SMC_BATT_ISENSE	UNUSED_SMC_SENSE

UNUSED_SMC_SENSE — 10K — R5924
PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7.

SMC PULL-UPS & PULL-DOWNS

=PP3V3_S5_SMC

SMC_ONOFF_L	R5808	10K
SMC_ODD_DETECT	R5829	10K
SC_RX_L	R5832	10K
SC_TX_L	R5833	10K
SMS_ONOFF_L	R5815	10K
SMC_TX_L	R5817	10K
SMC_RX_L	R5818	100K
SYS_ONEWIRE	R5819	10K
SMC_BS_ALRT_L	R5821	10K
SMC_TMS	R5822	10K
SMC_TDO	R5823	10K
SMC_TDI	R5824	10K
SMC_TCK	R5825	10K
SMC_BC_ACOK	R5826	10K
SMC_FWE	R5828	10K
SMC_LID	R5916	10K
SMC_EXCARD_OC_L	R5831	10K
SMC_XDP_TCK_3_3	R5934	1K
SMC_CPU_RESET_3_3_L	R5933	1K
SMC_EXCARD_CP	R5830	10K
SMC_CASE_OPEN	R5917	10K

TPM RESET PULLUP

SMC_TPM_RESET_L — R5827 — 10K — PP3V3_TPM_3VSB

WIRE-OR DIMM OVERTEMP TO SMC

DIMM_OVERTEMP_L — PM_EXTTS_L

WIRE SMC TO SB PINS

SMC_CPU_INIT_3_3_L	FWH_INIT_L	MAKE_BASE=TRUE
SMC_SUS_CLK	SUS_CLK_SB	MAKE_BASE=TRUE
SC_RX_L — 0 — R5922	SMC_RX_L	
SC_TX_L — 0 — R5923	SMC_TX_L	

POWER SUPPLY TEMP SENSE

SMC_ANALOG_ID — ACDC_TEMP (MAKE_BASE=TRUE)

SELECT TPM GPIO

SMC_TPM_GPIO — 0 — R5920 — SMC_TPM_GPIO1 — TPM_GPIO1
SMC_TPM_GPIO — 0 — R5921 — SMC_TPM_GPIO2 — TPM_GPIO2

HDD ACTIVITY MONITOR

PP5V_S0
M51: FOLLOWED M50, NOT CONNECTING TO SMC, AND TERMINATING
TP_SB_SATALED_L — PU_HDD_ACTIVITY_LED — R5960 — 10K
MAKE_BASE=TRUE

SMC_TPM_PP

SMC_TPM_PP — R5995 0 — TPM_PP

TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND

PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY INPUT TO THIS END. PLACE AND LAY OUT INTO DIGITAL GND VIA CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.
XW5900 (SM) — GND_NEXT_TO_SMC — OMIT

M51 SPECIFIC: GPU MONITORING SIGNALS

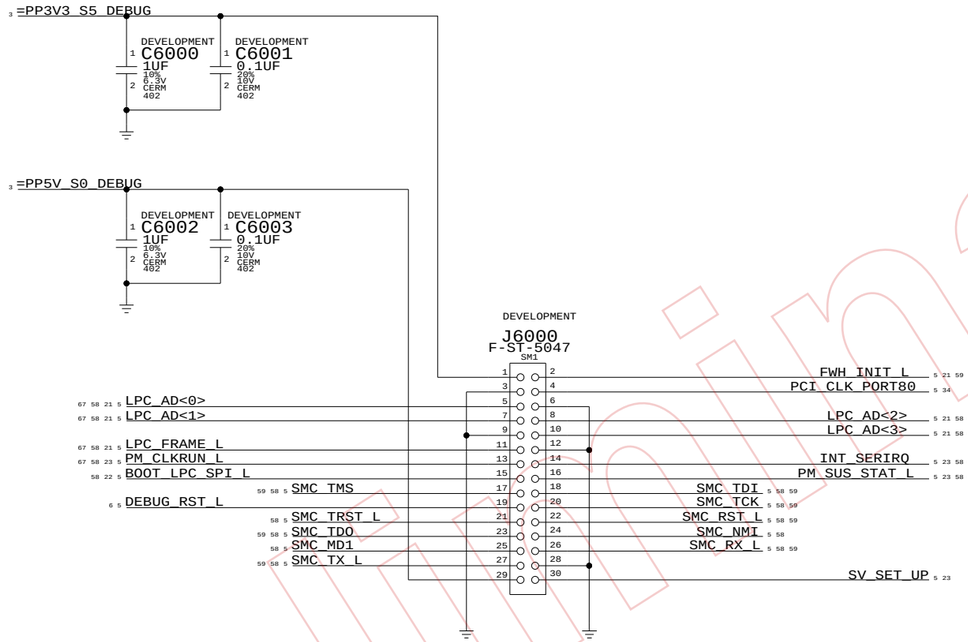
SMC_XDP_TMS (I327)	MXM_AC_BATT_L	MAKE_BASE=TRUE
SMC_XDP_TDO_3_3 (I328)	GPU_OVERTEMP_L	MAKE_BASE=TRUE

SMC & TPM SUPPORT

SYNC_MASTER=M51_HENRY — SYNC_DATE=07/31/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 59 OF 97	



LPC+ CONN

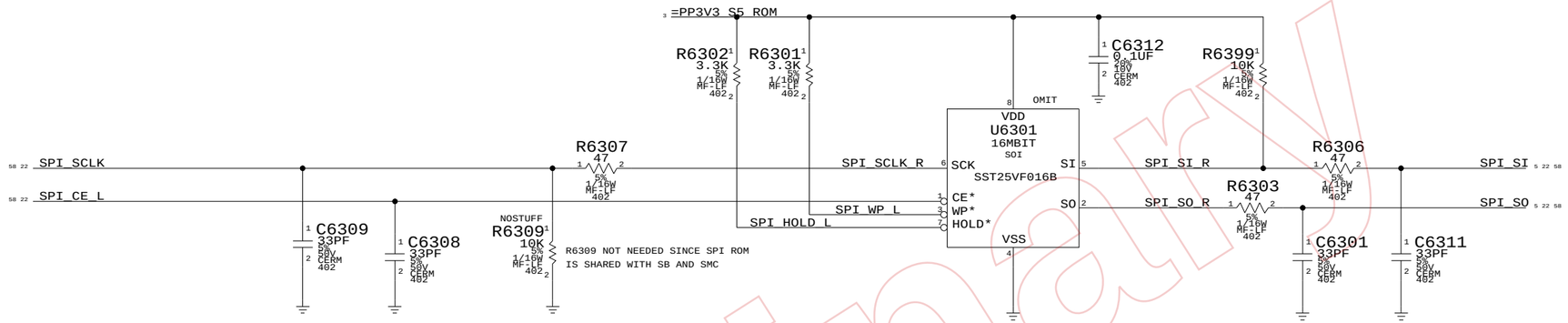
SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A

SCALE: NONE

SHT 60 OF 97



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100

R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM

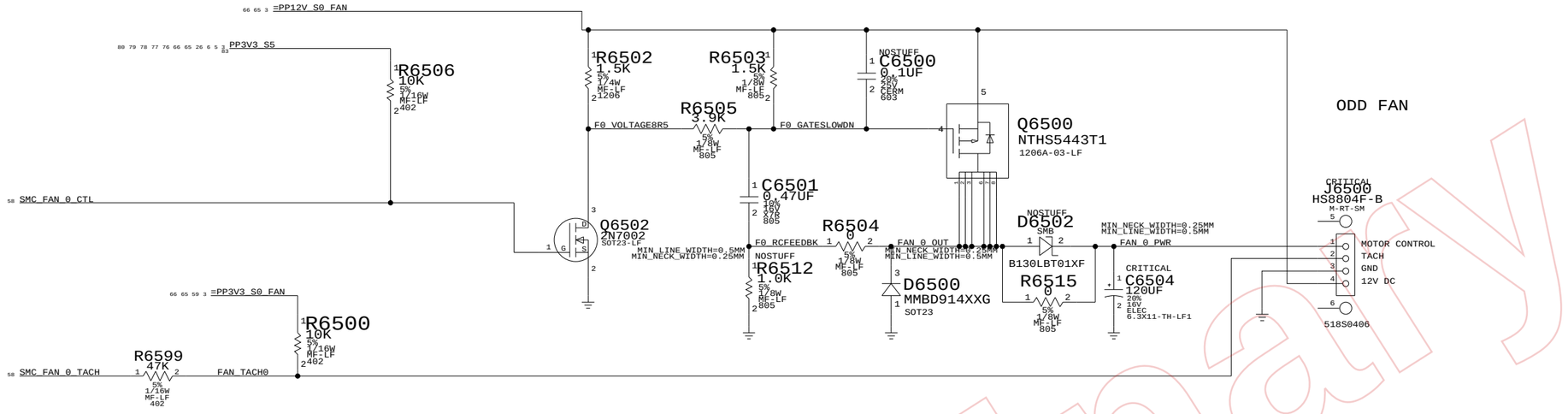
SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A

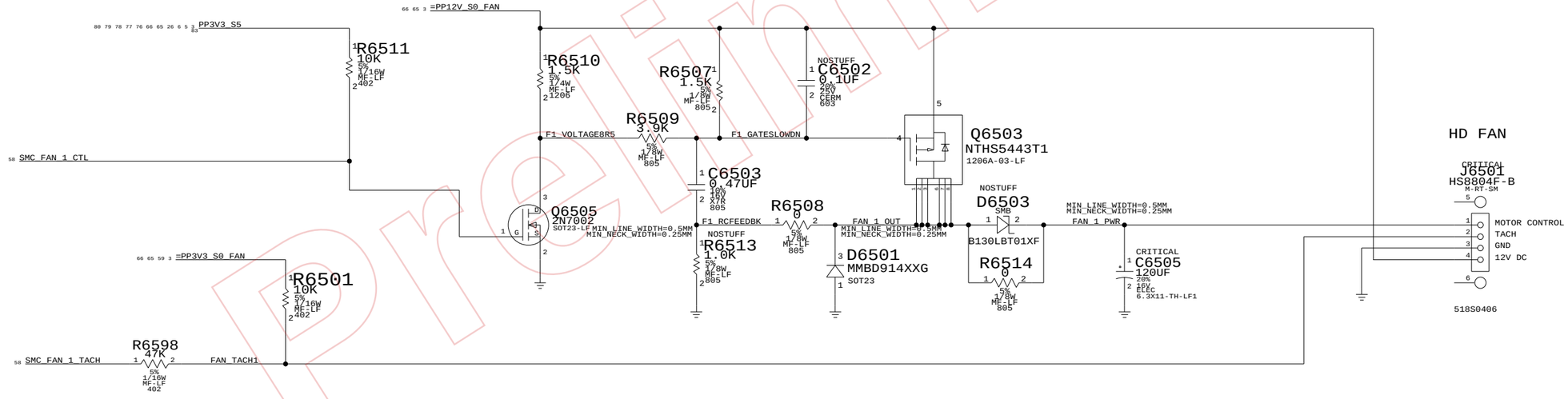
SCALE	SHT
NONE	63 OF 97

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



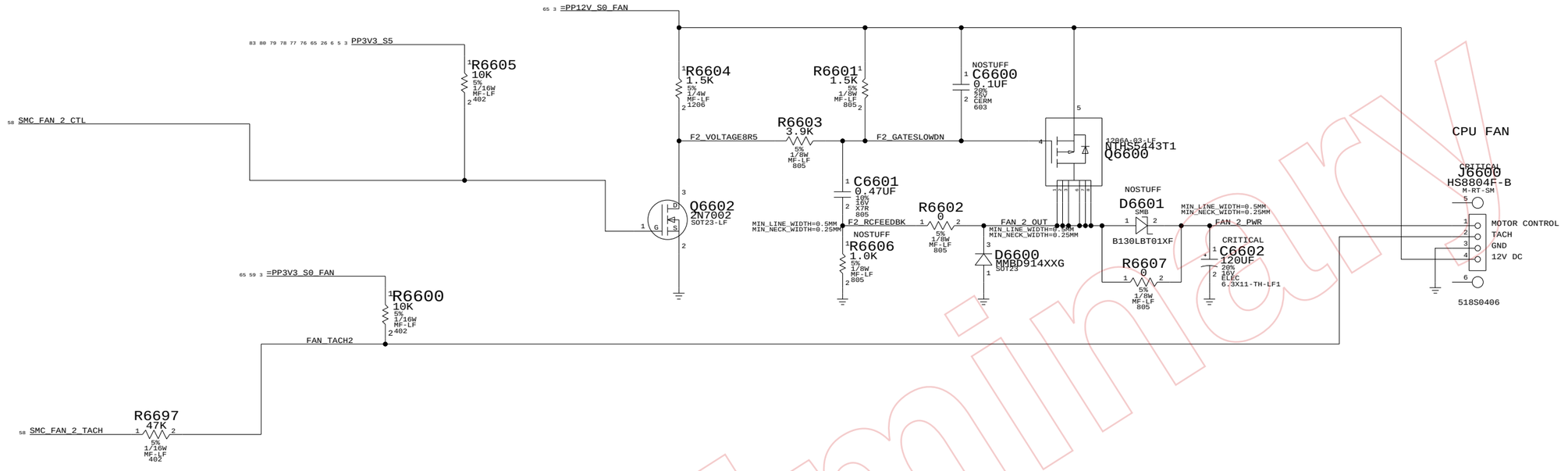
HD AND OD FAN

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

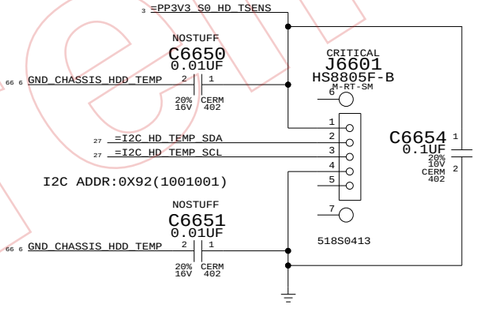
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 65 OF 97	

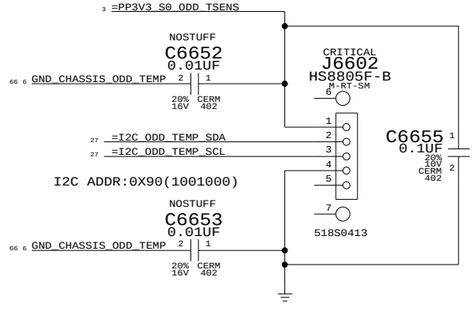
FAN 2



HD TEMP SENSOR



ODD TEMP SENSOR

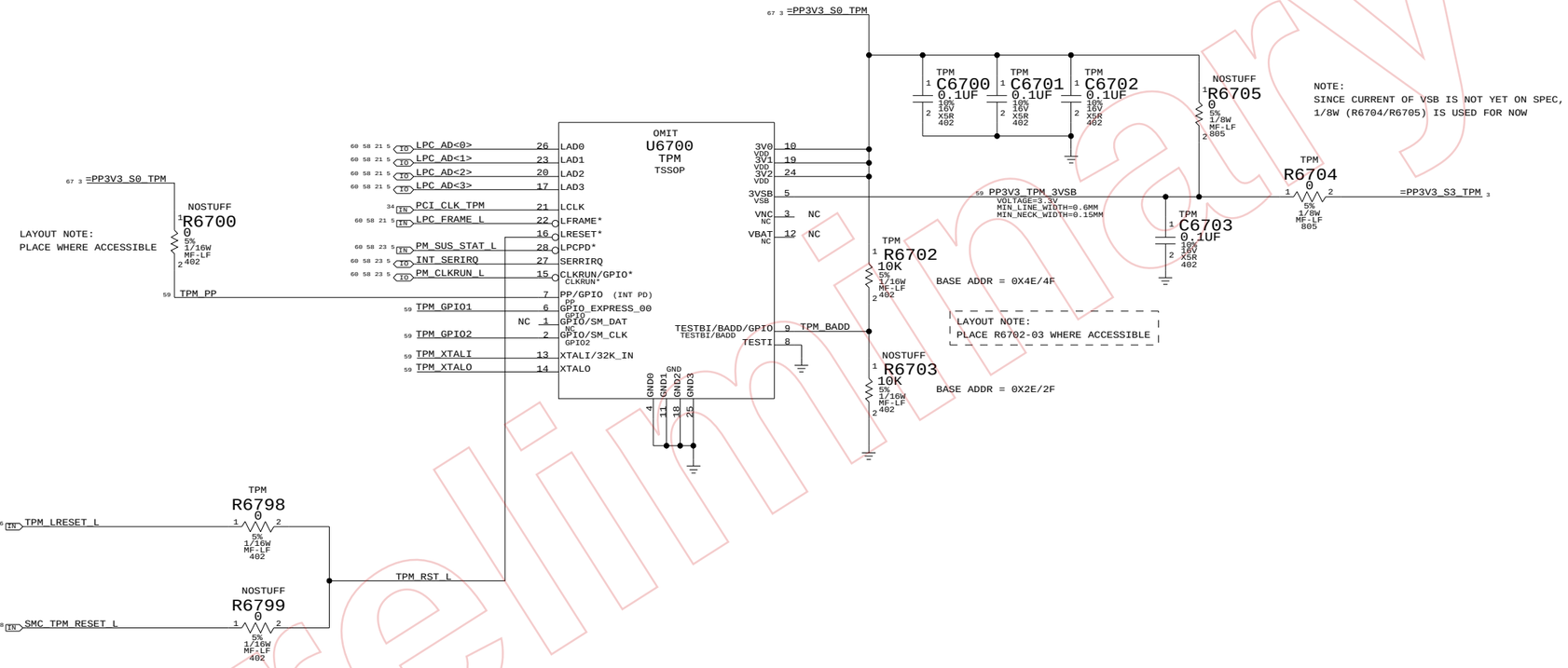


CPU FAN, HD & OD TEMP

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 66 OF 97	



TPM

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

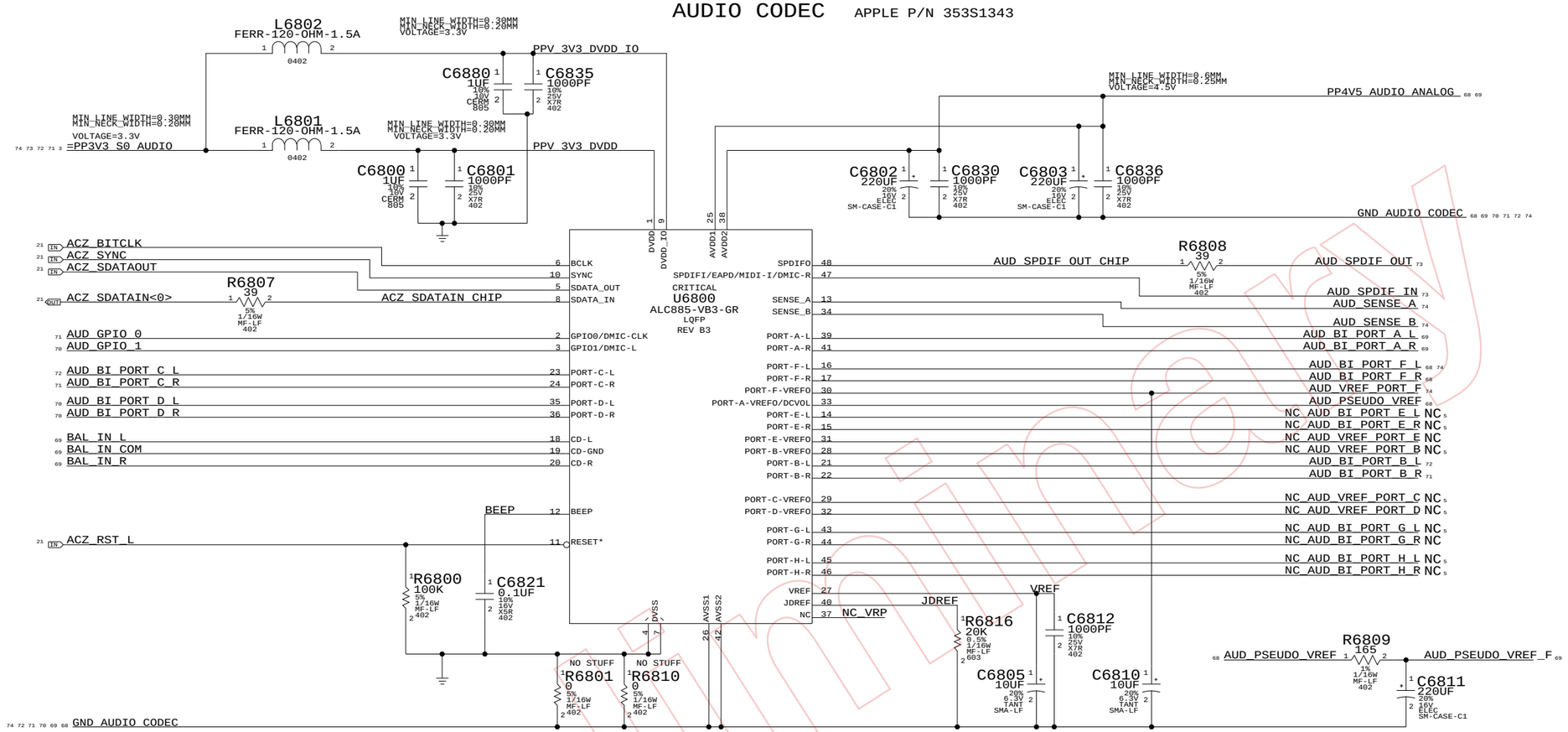
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A

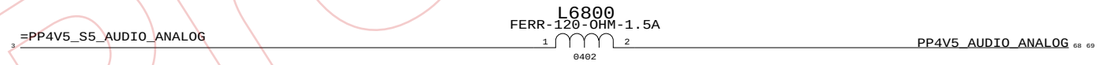
SCALE	SHT
NONE	67 OF 97

AUDIO CODEC

APPLE P/N 353S1343



4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP



AUD_BI_PORT_F_L ═ AUD_BI_PORT_F_R

MIC INPUT TO BOTH L&R

AUDIO: CODEC

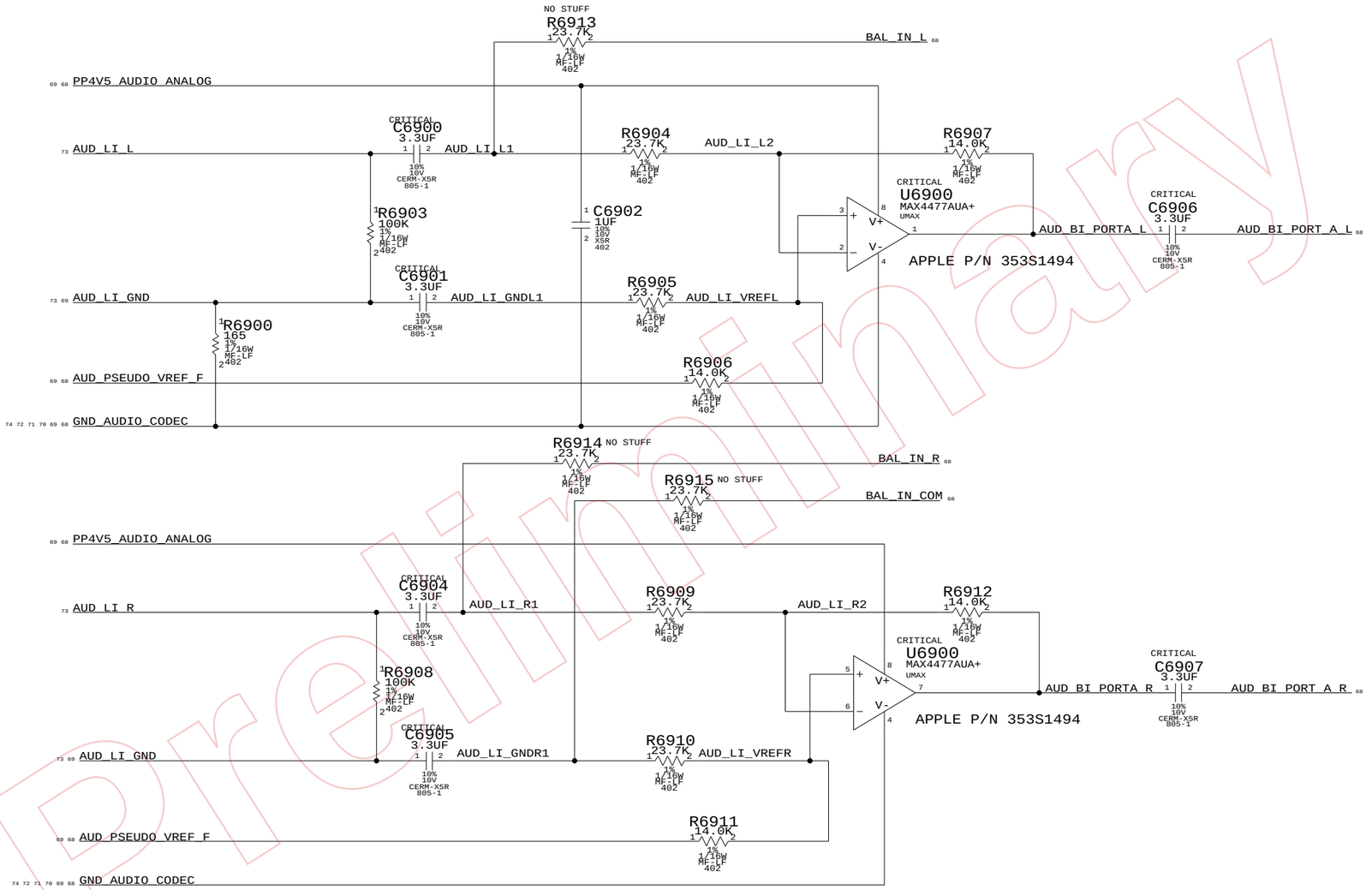
SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 68 OF 97	

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.59



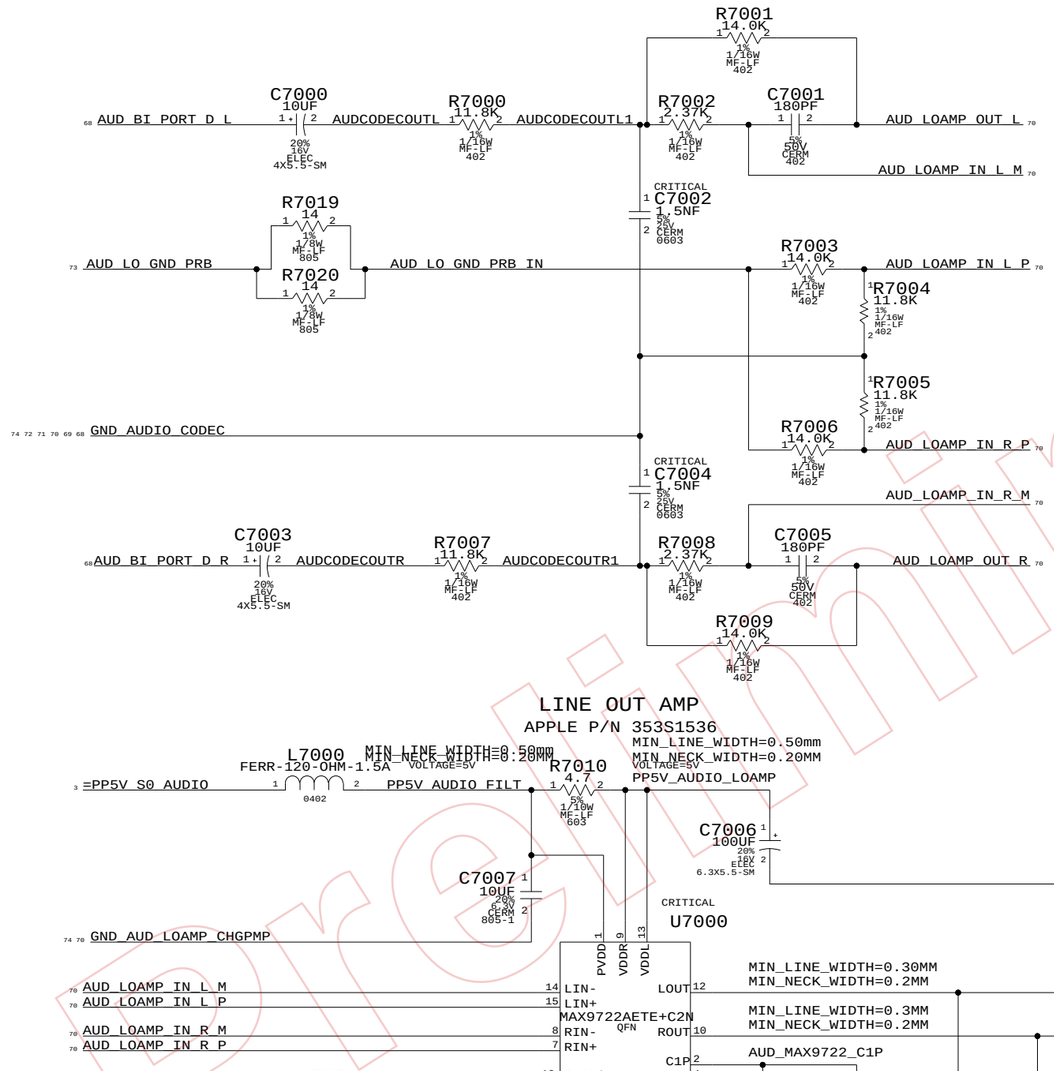
AUDIO: LINE INPUT AMP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 69 OF 97	

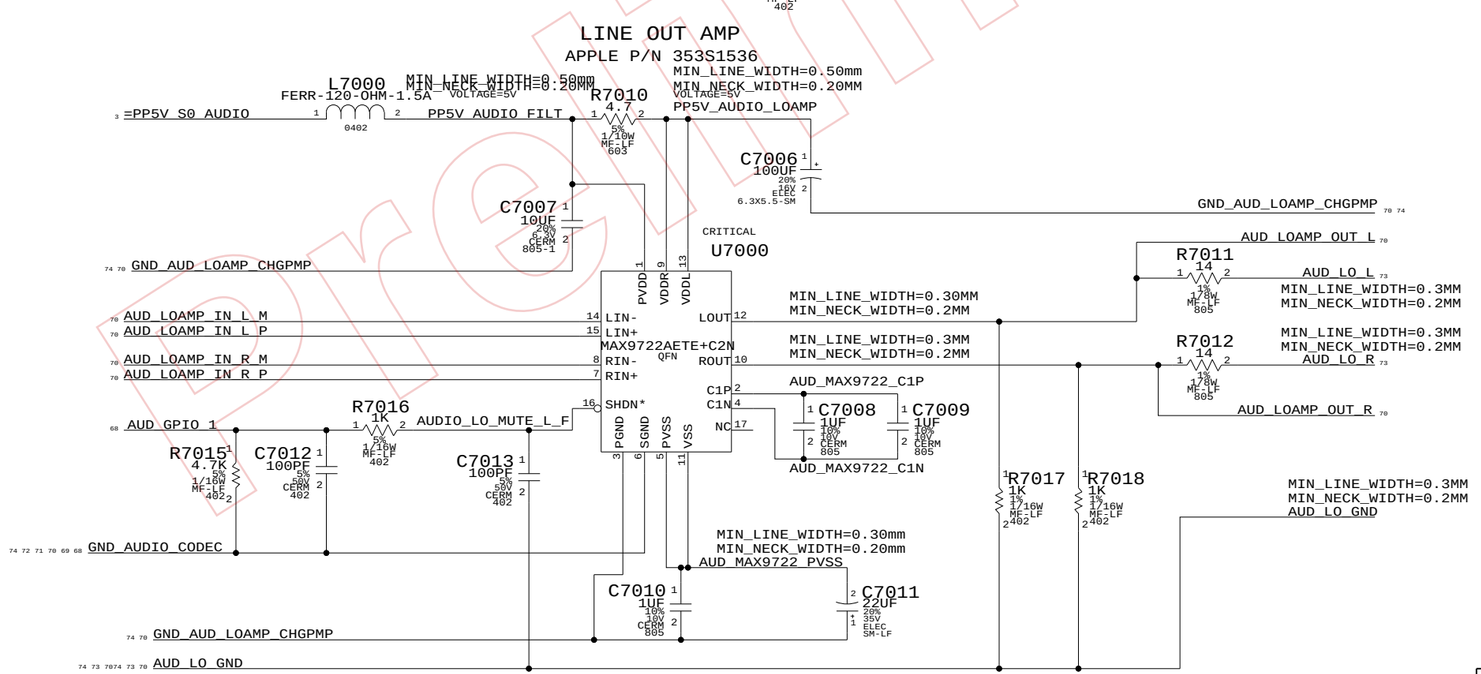
LINE OUT LOW-PASS FILTER

Fc = 37 KHZ, Av = -1.18



LINE OUT AMP

APPLE P/N 353S1536



AUDIO: COMBO OUT AMP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 70 OF 97	

DRAWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING

SPEAKER AMP
APPLE P/N 353S1156

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=12V

PP12V_AUD_SPKRAMP_PLANE

=PP12V_S5_AUDIO_SPKRAMP

R7170 0.005 1% 1/4W MF-LF 1206

L7122 FERR-250-OHM SM-1

L7100 FERR-250-OHM SM-1

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=3.0MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=12V
12V_S5_SPKRAMP

C7117 470UF 20% 25V ELEC 10X10-SM
C7100 470UF 20% 25V ELEC 10X10-SM
C7101 10UF 10% 16V X5R-CERM 1210
C7118 0.1UF 10% 16V CERM 603

GND_AUDIO_SPKRAMP_PLANE

C7102 1UF 10% 16V X7R 805
C7119 0.1UF 20% 16V CERM 603
C7103 10UF 10% 16V X5R-CERM 1210

GND_AUDIO_SPKRAMP_PLANE

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.2MM
AUD_MAX9714_CHOLD

AUD_BI_PORT_C_R

L7105 1000-OHM-200MA 0603
C7104 0.47UF 10% 16V X7R 805
AUDSAMPINLN
C7115 100PF 5% 50V CERM 402

L7106 1000-OHM-200MA 0603
C7105 0.47UF 10% 16V X7R 805
AUDSAMPINLP

GND_AUDIO_CODEC

L7107 1000-OHM-200MA 0603
C7106 0.47UF 10% 16V X7R 805
AUDSAMPINRP
C7116 100PF 5% 50V CERM 402

AUD_BI_PORT_B_R

L7108 1000-OHM-200MA 0603
C7107 0.47UF 10% 16V X7R 805
AUDSAMPINRN

=PP3V3_S0_AUDIO

R7114 47K 5% 1/10W MF-LF 402

AUD_SAMP_SHDN_L

AUD_SPKRAMP_MUTE

R7115 47K 5% 1/10W MF-LF 402

=PP3V3_S0_AUDIO

R7113 47K 5% 1/16W MF-LF 402

AUD_GPIO_0

AUD_SPKRAMP_MUTE_L

Q7100 2N7002DW-X-F SOT-363

R7112 4.7K 5% 1/16W MF-LF 402

C7120 100PF 5% 50V CERM 402

C7121 100PF 5% 50V CERM 402

GND_AUDIO_CODEC

GND_AUDIO_SPKRAMP_PLANE

GND_AUDIO_CODEC

C7190 100PF 5% 50V CERM 402

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
SPKRAMP_SS

Q7100 2N7002DW-X-F SOT-363

C7114 1UF 10% 25V X5R 603

C7109 0.47UF 10% 16V X7R 805

NOSTUFF
R7119 0 5% 1/16W MF-LF 402

CRITICAL
U7100
MAX9714
QFN-LF

VDD
CHOLD
INL-
INL+
INR+
INR-
G1
G2
FS1
FS2
SHDN*
NC
REG
AGND PAD
THM
PGND
OUTL+
OUTL+
OUTL-
OUTL-
C1+
C1-
OUTR+
OUTR+
OUTR-
OUTR-
SS

AUD_SAMP_INL_N
AUD_SAMP_INL_P
AUD_SAMP_INR_P
AUD_SAMP_INR_N
AUD_SAMP_G1
AUD_SAMP_G2
AUD_SAMP_FS1
AUD_SAMP_FS2
AUD_SAMP_SHDN_L
AUD_MAX9714_VREG

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUDSAMPOUTLP

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUDSAMPOUTLN

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUDSAMPCPP

C7108 0.1UF 10% 50V X7R 603-1

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUDSAMPCPN

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUDSAMPOUTRP

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUDSAMPOUTRN

L7101 180-OHM-1.5A 0603-LF
L7102 180-OHM-1.5A 0603-LF
L7103 180-OHM-1.5A 0603-LF
L7104 180-OHM-1.5A 0603-LF

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUD_SPKR_OUTCR_P

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUD_SPKR_OUTCR_N

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUD_SPKR_OUTBR_P

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUD_SPKR_OUTBR_N

C7110 1000PF 10% 25V X7R 402
C7111 1000PF 10% 25V X7R 402
C7112 1000PF 10% 25V X7R 402
C7113 1000PF 10% 25V X7R 402

XW7102 SM OMIT
XW7101 SM OMIT

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=3.0MM
MIN_NECK_WIDTH=0.2MM

GND_AUDIO_SPKRAMP

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

GND_AUDIO_SPKRAMP_PLANE

GAIN SETTINGS: +16DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

=PP3V3_S0_AUDIO

RP7100 47K 5% 1/16W SM-LF

AUD_SAMP_FS2
AUD_SAMP_FS1
AUD_SAMP_G2
AUD_SAMP_G1

NOSTUFF
R7118 0 5% 1/16W MF-LF 402

NOSTUFF
R7108 0 5% 1/16W MF-LF 402

GND_AUDIO_SPKRAMP_PLANE

AUDIO: SPEAKER AMP_1

SYNC_MASTER=AUDIO
SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 71 OF 97	

DRAWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING

SPEAKER AMP
APPLE P/N 353S1156

=PP12V_S5_AUDIO_SPKRAMP
R7270 0.005 1% 1/4W MF-LF 1206
12V_S5_SPKRAMP1
L7222 FERR-250-OHM SM-1
L7200 FERR-250-OHM SM-1
PP12V_AUD_SPKRAMP1_PLANE
C7217 470UF 20% 25V ELEC 10X10-SM
C7200 470UF 20% 25V ELEC 10X10-SM
C7201 10UF 10% 16V X5R-CERM 1210
C7218 0.1UF 20% 16V CERM 603
C7202 1UF 10% 16V X7R 805
C7219 0.1UF 20% 16V CERM 603
C7203 10UF 10% 16V X5R-CERM 1210
GND_AUDIO_SPKRAMP1_PLANE

AUD_BI_PORT_C_L
L7205 1000-OHM-200MA 0603
C7204 0.47UF 10% 16V X7R 805
AUDSAMPINLN1
C7215 100PF 5% 50V CERM 402
AUD_SAMP1_INL_N
AUD_SAMP1_INL_P

GND_AUDIO_CODEC
L7206 1000-OHM-200MA 0603
C7205 0.47UF 10% 16V X7R 805
AUDSAMPINLP1

L7207 1000-OHM-200MA 0603
C7206 0.47UF 10% 16V X7R 805
AUDSAMPINRP1
C7216 100PF 5% 50V CERM 402
AUD_SAMP1_INR_P
AUD_SAMP1_INR_N

AUD_BI_PORT_B_L
L7208 1000-OHM-200MA 0603
C7207 0.47UF 10% 16V X7R 805
AUDSAMPINRN1

=PP3V3_S0_AUDIO
R7214 47K 5% 1/16W MF-LF 402
C7290 100PF 5% 50V CERM 402
GND_AUDIO_SPKRAMP1_PLANE

SPKRAMP1_SS
AUD_SPKRAMP_MUTE
Q7200 2N7002 SOT23-LF
GND_AUDIO_SPKRAMP1_PLANE

GND_AUDIO_CODEC

CRITICAL
U7200 MAX9714 QFN-LF
VDD
INL- INL+ INR+ INR- G1 G2 FS1 FS2 SHDN* NC REG
AUD_SAMP1_G1
AUD_SAMP1_G2
AUD_SAMP1_FS1
AUD_SAMP1_FS2
AUD_SAMP1_SHDN_L
AUD_MAX9714_VREG1
MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.15MM
THM PAD AGND PGND
MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.15MM
C7214 1UF 10% 25V X5R 603
C7209 0.47UF 10% 16V X7R 805
NOSTUFF R7219 0 5% 1/16W MF-LF 402

CHOLD OUTL+ OUTL+ OUTL- OUTL- C1+ C1- OUTR+ OUTR+ OUTR- OUTR- SS
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
AUD_MAX9714_CHOLD1
C7208 0.1UF 10% 50V X7R 603-1
MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.15MM
AUDSAMPCPP1
AUDSAMPCPN1

NET_SPACING_TYPE=AUDIO MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM
AUDSAMPOUTLP1
AUDSAMPOUTLN1
AUDSAMPOUTRP1
AUDSAMPOUTRN1
NET_SPACING_TYPE=AUDIO MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

L7201 180-OHM-1.5A 0603-LF
L7202 180-OHM-1.5A 0603-LF
L7203 180-OHM-1.5A 0603-LF
L7204 180-OHM-1.5A 0603-LF
AUD_SPKR_OUTCL_P
AUD_SPKR_OUTCL_N
AUD_SPKR_OUTBL_P
AUD_SPKR_OUTBL_N

C7210 1000PF 10% 25V X7R 402
C7211 1000PF 10% 25V X7R 402
C7212 1000PF 10% 25V X7R 402
C7213 1000PF 10% 25V X7R 402

XW7202 SM OMIT
XW7201 SM OMIT
NET_SPACING_TYPE=AUDIO MIN_LINE_WIDTH=3.0MM MIN_NECK_WIDTH=0.2MM
GND_AUDIO_SPKRAMP

GND_AUDIO_SPKRAMP1_PLANE

GAIN SETTINGS: +16DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

=PP3V3_S0_AUDIO
RP7200 47K 5% 1/16W SM-LF
AUD_SAMP1_FS2
AUD_SAMP1_FS1
AUD_SAMP1_G2
AUD_SAMP1_G1
NOSTUFF R7218 0 5% 1/16W MF-LF 402
NOSTUFF R7208 0 5% 1/16W MF-LF 402
GND_AUDIO_SPKRAMP1_PLANE

AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 72 OF 97	

COMBO IN JACK
APPLE P/N 514-0328

NC_AUD_LI_TYPE_JACK NC

CRITICAL
J7300
OPTI-AUD-IN-JCK-M51
F-ANG-TH

AUD_LI_L_JACK — L7300 180-OHM-1.5A 0603-LF — AUD_LI_L_EMI — L7304 180-OHM-1.5A 0603-LF — AUD_LI_L 69
AUD_LI_DET_JACK — L7301 180-OHM-1.5A 0603-LF — AUD_LI_DET_EMI — L7305 180-OHM-1.5A 0603-LF — AUD_LI_DET_H 74
AUD_LI_R_JACK — L7302 180-OHM-1.5A 0603-LF — AUD_LI_R_EMI — L7306 180-OHM-1.5A 0603-LF — AUD_LI_R 69
AUD_LI_GND_JACK — L7303 180-OHM-1.5A 0603-LF — AUD_LI_GND_EMI — L7307 180-OHM-1.5A 0603-LF — AUD_LI_GND 69

MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.3MM

TYPE_DET 6
TIP 2
TIP_DET 3
RING 4
GND_1 1
GND_2 5

OPTICAL RECEIVER: VCC 7 (73 PP3V3_AUDIO_SPDIF_JACK), GND 8, VOUT 9 — AUD_SPDIFIN_JACK

R7306 39 5% 1/16W MF-LF 402 — AUD_SPDIF_IN 68

DZ7300 14V-15A 0405
DZ7303 14V-15A 0405

C7300 100PF 5% 50V CERM 402
C7302 100PF 5% 50V CERM 402
C7301 100PF 5% 50V CERM 402
C7303 100PF 5% 50V CERM 402

73 AUD_SPDIF_GND
NC
C7326 0.1UF 20% 10V CERM 402
R7305 0 5% 1/16W MF-LF 402

74 73 6 GND_CHASSIS_AUDIO_EXTERNAL

XW7300 SM

NET_SPACING_TYPE=AUDIO
74 AUD_MIC_IN_P — L7309 180-OHM-1.5A 0603-LF — AUD_MIC_IN_P_EMI — L7312 180-OHM-1.5A 0603-LF — GND_AUDIO_MIC_CONN (IN) / 47 AUD_MIC_IN_P_CONN (IN)
74 AUD_MIC_IN_N — L7310 180-OHM-1.5A 0603-LF — AUD_MIC_IN_N_EMI — L7313 180-OHM-1.5A 0603-LF — 47 AUD_MIC_IN_N_CONN (IN)

C7321 100PF 5% 50V CERM 402
C7322 100PF 5% 50V CERM 402

NET_SPACING_TYPE=AUDIO
NET_SPACING_TYPE=AUDIO
NET_SPACING_TYPE=AUDIO
NOSTUFF
DZ7304 14V-15A 0405

TO FHB CONNECTOR PAGE 47

TO POWER SUPPLY PAGE 6

6 (IN) GND_CHASSIS_AUDIO_INTERNAL

SPEAKER CABLE CONNECTORS
APPLE P/N 518-0193
APPLE P/N 518-0255

PROPERTIES FOR ALL SPKR NETS
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=AUDIO

CRITICAL
J7301
87833-0431
M-RT-TH

72 AUD_SPKR_OUTBL_P — 1 — 2 — AUD_SPKR_OUTBL_N 72
72 AUD_SPKR_OUTCL_N — 3 — 4 — AUD_SPKR_OUTCL_P 72

PROPERTIES FOR ALL SPKR NETS
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=AUDIO

CRITICAL
J7302
87833-0631
M-RT-TH

71 AUD_SPKR_OUTBR_P — 1 — 2 — AUD_SPKR_OUTBR_N 71
5 NC_J7302_3 — 3 — 4 — NC_J7302_6 5
71 AUD_SPKR_OUTCR_N — 5 — 6 — AUD_SPKR_OUTCR_P 71

LINE OUT JACK
APPLE P/N 514-0329

68 AUD_SPDIF_OUT — L7314 180-OHM-1.5A 0603-LF — AUD_SPDIF_OUT_JACK
74 72 71 68 3 =PP3V3_S0_AUDIO — L7315 180-OHM-1.5A 0603-LF — PP3V3_AUDIO_SPDIF_EMI — L7323 180-OHM-1.5A 0603-LF — 73 PP3V3_AUDIO_SPDIF_JACK
74 AUD_LO_DET1 — L7316 180-OHM-1.5A 0603 — AUD_LO_DET1_EMI — L7324 180-OHM-1.5A 0603-LF
70 AUD_LO_L — L7318 180-OHM-1.5A 0603-LF — AUD_LO_L_EMI — L7326 180-OHM-1.5A 0603-LF
74 AUD_LO_DET2 — L7319 180-OHM-1.5A 0603-LF — AUD_LO_DET2_EMI — L7327 180-OHM-1.5A 0603-LF
70 AUD_LO_R — L7317 180-OHM-1.5A 0603-LF — AUD_LO_R_EMI — L7325 180-OHM-1.5A 0603-LF
70 AUD_LO_GND_PRB — L7320 180-OHM-1.5A 0603-LF — AUD_LO_GND_EMI — L7328 180-OHM-1.5A 0603-LF
74 70 AUD_LO_GND — L7380 180-OHM-1.5A 0603-LF — GND_AUDIO_CODEC_EMI1 — L7381 180-OHM-1.5A 0603-LF

MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.3MM

C7317 0.1UF 20% 10V CERM 402
C7318 1UF 10% 10V CERM 805

CRITICAL
J7303
OPTI-AUD-OUT-JCK-M51
F-ANG-TH

AUD_LO_DET1_JACK — TYPE_DET
AUD_LO_L_JACK — TIP
AUD_LO_DET2_JACK — TIP_DET
AUD_LO_R_JACK — RING
GND_1
AUD_LO_GND_JACK — GND_2
VIN, VCC, GND — LED

MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.2MM
AUD_SPDIF_GND — NC 73

R7302 0 5% 1/16W MF-LF 402

C7311 100PF 5% 50V CERM 402
C7312 100PF 5% 50V CERM 402
C7315 100PF 5% 50V CERM 402
C7380 100PF 5% 50V CERM 402
C7314 100PF 5% 50V CERM 402
C7313 100PF 5% 50V CERM 402
C7323 100PF 5% 50V CERM 402

DZ7301 14V-15A 0405
DZ7302 14V-15A 0405

74 73 6 GND_CHASSIS_AUDIO_EXTERNAL

AUDIO: CONNECTORS

SYNC_MASTER=AUDIO — SYNC_DATE=08/04/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A

SCALE: NONE — SHT 73 OF 97

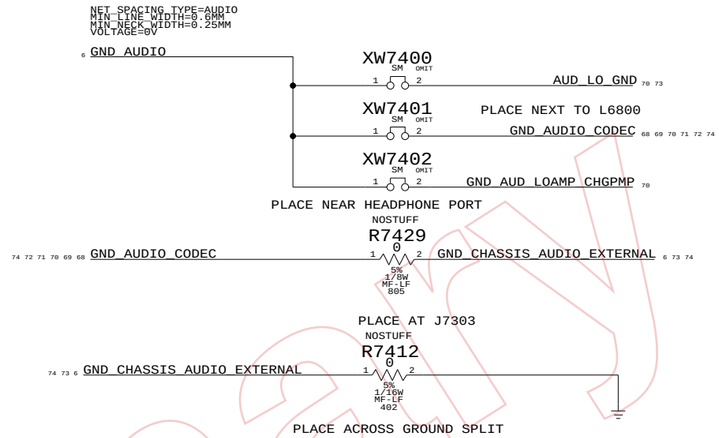
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	DAC	PIN COMPLEX	MUTE CONTROL
LINE OUT	0X0C	0X02	0X14(D)	GPIO 1
SPKR AMP	0X0D	0X03	0X18(B)	GPIO 0
SPKR AMP1	0X0F	0X05	0X1A(C)	GPIO 0
SPDIFOUT		CONVERTER=0X06	PIN=0X1E	
		DETECT DELEGATE PIN 0X16H		

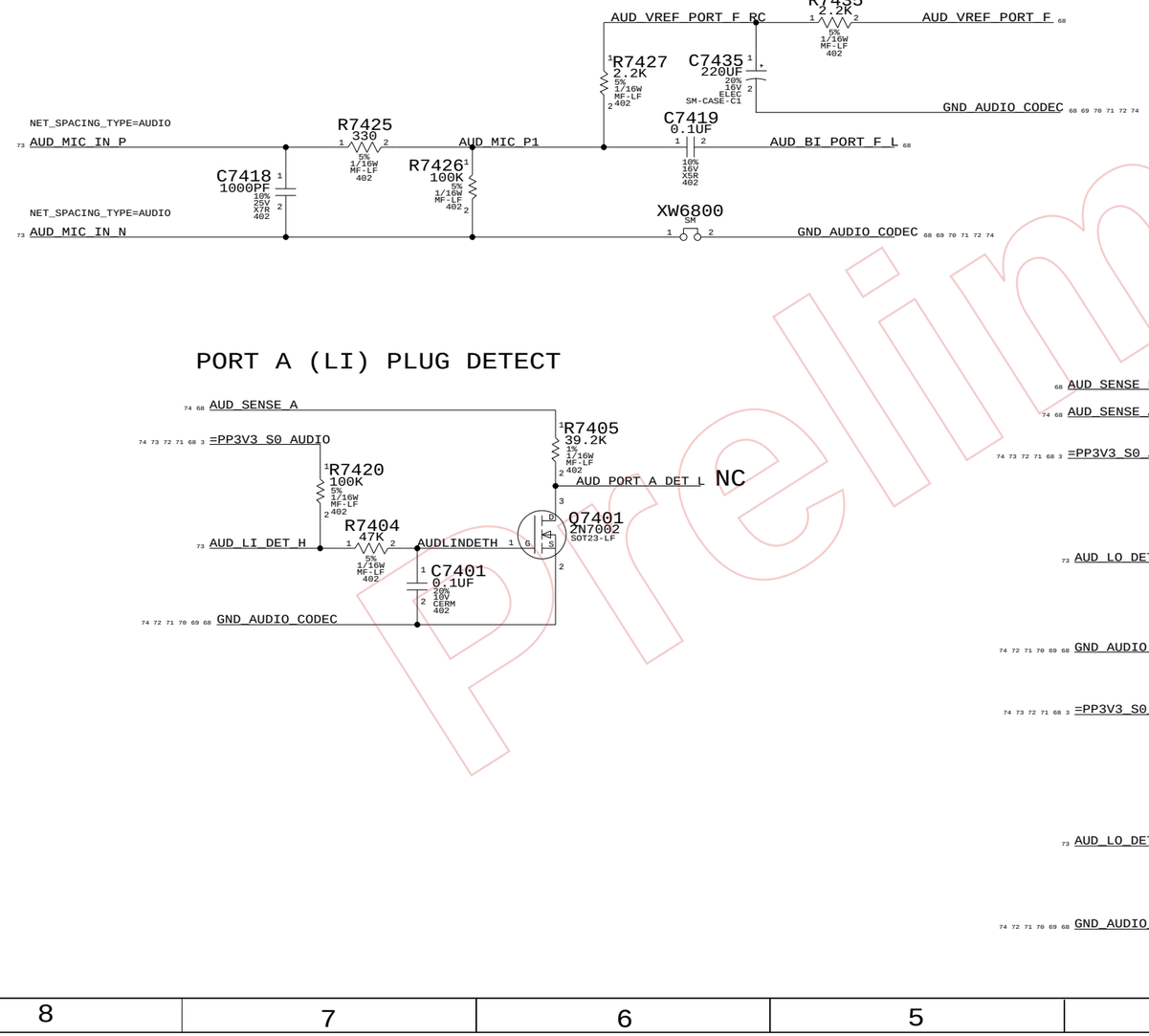
CODEC INPUT SIGNAL PATHS

FUNCTION	ADC	MIXER	PORT	VREF
MIC INPUT	0X07	0X24	0X19(F)	80%
LINE INPUT	0X08	0X23	0X15(A)	50%
SPDIFIN	CONVERTER=0X0A		PIN=0X1F	

AUDIO GROUND RETURNS

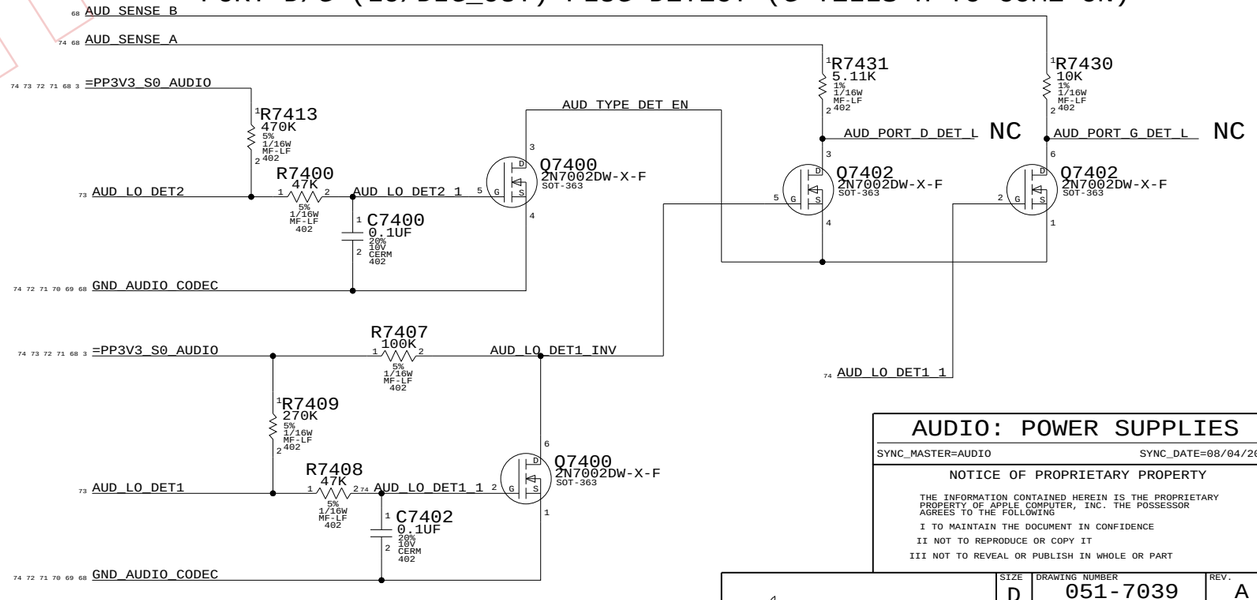


MICROPHONE IMPEDANCE MATCHING CIRCUIT



PORT A (LI) PLUG DETECT

PORT D/G (LO/DIG_OUT) PLUG DETECT (G TELLS H TO COME ON)



AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 74 OF 97	

IMVP6 CPU VCORE REGULATOR

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

CPU_VCCSENSE_P & N ARE DIFF PAIRS ROUTE AS 18MIL WIDE, 7MIL SPACE

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 75 OF 97	

PROCESSOR VCORE SENSE

PCB: PLACE R7612, C7612 WITHIN 1" OF SMC (U5800)

75 5 3 PPVCORE_CPU — R7612 4.53K 1% 1/16W MF-LF 402 (CPU_PWR_SENSE) — SMC_CPU_VSENSE 58

C7612 0.22UF 20% 6.3V X5R 402 (CPU_PWR_SENSE) — GND_SMC_AVSS 58 59 76 84

PROCESSOR VCORE CURRENT SENSE

(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

C7600 470PF 10% 50V CERM 402 (CPU_PWR_SENSE) — CPU_ISENSE_OUT_R

R7609 1M 1% 1/16W MF-LF 402 (CPU_PWR_SENSE)

C7601 0.1UF CERM 20% 402 10V CRITICAL (CPU_PWR_SENSE) — PP3V3_S0 84 83 76 45 41 27 26 10 6 5 3

U7600 LMV2011MF SOT23-5 (CPU_PWR_SENSE) — GND_CPU_ISENSE_OPAMP

75 IMVP6_VO — R7659 0 5% 1/16W MF-LF 402 (CPU_PWR_SENSE) — IMVP6_VO_R_OA

R7605 40.2K 1% 1/16W MF-LF 402 (CPU_PWR_SENSE) — CPU_ISENSE_R_POS

75 IMVP6_DROOP — R7669 0 5% 1/16W MF-LF 402 (CPU_PWR_SENSE) — IMVP6_DROOP_R

R7606 40.2K 1% 1/16W MF-LF 402 (CPU_PWR_SENSE) — CPU_ISENSE_R_NEG

MIN_LINE_WIDTH=0.20 MM

C7603 470PF 10% 50V CERM 402 (CPU_PWR_SENSE)

R7603 1M 1% 1/16W MF-LF 402 (CPU_PWR_SENSE)

NOSTUFF R7604 0 5% 1/16W MF-LF 402

R7607 0 5% 1/16W MF-LF 402 (CPU_PWR_SENSE) — GND_NEXT_TO_SMC 59

PCB: PLACE R7602, C7602 WITHIN 1" OF SMC (U5800)

R7602 4.53K 1% 1/16W MF-LF 402 (CPU_PWR_SENSE) — SMC_CPU_ISENSE 58

C7602 0.22UF 20% 6.3V X5R 402 (CPU_PWR_SENSE) — GND_SMC_AVSS 58 59 76 84

CPU CURRENT SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits

83 3 PP12V_S0_B

R7639 10K 5% 1/16W MF-LF 402 (CPU_PWR_SENSE)

Q7640 NTR4101P SOT-23 (CPU_PWR_SENSE)

ISENSE_CAL_EN_L — MIN_LINE_WIDTH=0.20 MM, MIN_NECK_WIDTH=0.20 MM

R7641 10K 5% 1/16W MF-LF 402 (CPU_PWR_SENSE)

ISENSE_CAL_EN_L_R

Q7639 2N7002 SOT23-LF (CPU_PWR_SENSE)

58 5 ISENSE_CAL_EN — R7640 100K 5% 1/16W MF-LF 402 (CPU_PWR_SENSE)

ISENSE_CAL_EN_LS12V

R7642 470K 5% 1/16W MF-LF 402 (CPU_PWR_SENSE)

9 8 3 =PPVCORE_S0_CPU

R7643 1.00 1% 1/4W MF-LF 1206 (CPU_PWR_SENSE)

CPUVCORE_ISENSE_CAL — MIN_LINE_WIDTH=0.50 mm, MIN_NECK_WIDTH=0.20 mm

CRITICAL Q7641 FDC796N SUPERSOT-6 (CPU_PWR_SENSE)

SMC PWRGD PULLUP

83 80 79 78 77 66 65 26 6 5 3 PP3V3_S5

R7623 10K 1% 1/16W MF-LF 402

NOSTUFF R7620 0 5% 1/16W MF-LF 402

82 78 6 SYS_POWERFAIL_L — RSMRST_PWRGD 58

SYSTEM CURRENT SENSE

PP12V_S5_AC_DC — MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V

CRITICAL R7650 0.005 1% 1W MF 2010 (SYS_PWR_SENSE)

PP12V_S5 3 76 77 78 79 80 82 83

PCB:KEEP SHORTS NEXT TO U7602

PCB:PLACE D7650,R7652,C7650 BY SMC

U7602 ZXCT1010 SOT23-5 (SYS_PWR_SENSE) — VIN, IOUT 3, NC, LOAD 5, GND 2

OMIT XW7650 SM — SYSTEM_DCIN_SENSE — SYSTEM_SENSE_I_R

R7651 5.90K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE)

R7656 100 1% 1/16W MF-LF 402 (SYS_PWR_SENSE) — SYSTEM_SENSE_SET

R7652 4.53K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE) — SMC_DCIN_ISENSE 58

C7650 0.22UF 20% 6.3V X5R 402 (SYS_PWR_SENSE) — GND_SMC_AVSS 58 59 76 84

PP3V3_S0 3 5 6 10 26 27 41 45 76 83 84

NOSTUFF D7650 BAS16-75V-0.25A SOT23-LF → TO SMC

1 MS TIME CONSTANT SO SMC ADC SAMPLING WORKS WELL.

SCALE	COUNT
3.33333 A/V	.010753 A/COUNT
ADC IS 10BIT 0 TO 1023	0 TO 3.3V

PCB: PLACE D7599, C7599, R7597 WITHIN 1" OF SMC (U5800)

SYSTEM VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)

83 82 80 79 78 77 76 3 PP12V_S5

R7653 6.04K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE)

R7654 2.0K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE)

SMC_SYSTEM_VSENSE_R

R7655 4.53K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE) — SMC_PBUS_VSENSE 58

C7651 0.22UF 20% 6.3V X5R 402 (SYS_PWR_SENSE) — GND_SMC_AVSS 58 59 76 84

SCALE	COUNT
4 V/V	.0129 V/COUNT
ADC IS 10BIT 0 TO 1023	0 TO 3.3V

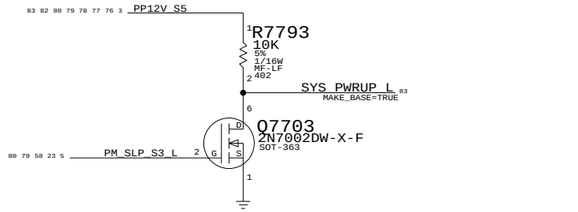
PCB: PLACE R7655, C7651 WITHIN 1" OF SMC (U5800)

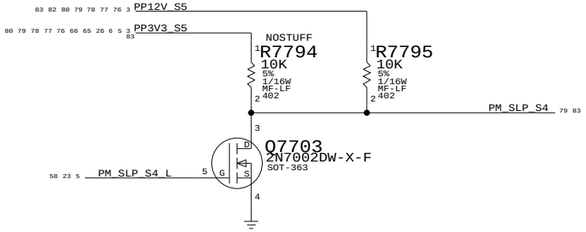
CPU & SYSTEM SENSE

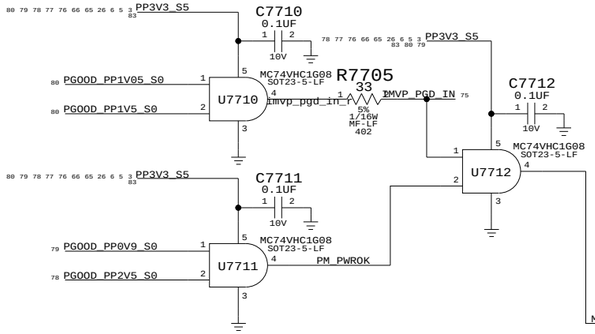
SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 76 OF 97	

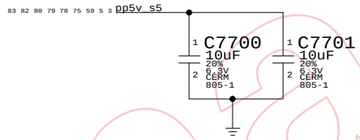


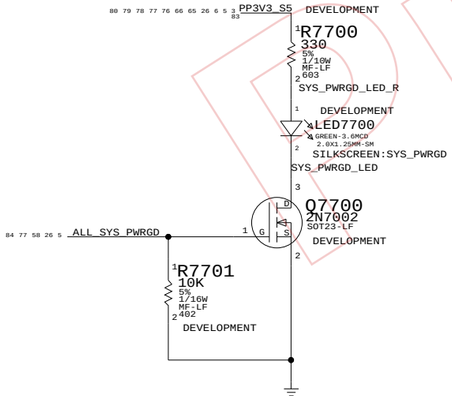




ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

two additional caps to increase ripple margin
put here to stay in sync with M50 on page 82





PWR GOOD

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A

SCALE	SHT
NONE	77 OF 97

3.3V AND 2.5V S5 REGULATOR

2.5V S5
POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

3.3V S5
POWER BUDGET
MISC=1.500A
SB=0.500A
AIRPORT=1.000A
PANEL=1.000A
TOTAL=4.000A

=PP3V3_S5_2V5_LDO
C7820 22UF 20% 6.3V X5R 805
CRITICAL Q7803 IRF1902PBF SO-8

PP12V_S5
C7892 1UF 10% 25V X5R 603
C7800 1UF 10% 6.3V CERM 402

3V3REG_VCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7805 10 1% 1/16W MF-LF 402
3V3REG_PVCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_LDO_DR MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7823 1000PF 10% 25V X7R 402

U7800 ISL6549 QFN
VCC12 CRITICAL
VCC5
PVCC5
LDO_DR
LDO_FB
FS_DIS
THRML_PAD
DGND AGND PGND
UGATE BOOT PHASE LGATE FB COMP

3V3REG_UGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7840 2.2 5% 1/16W MF-LF 402
3V3REG_BOOT MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_BOOT_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7801 0.1UF 20% 25V CERM 603
3V3REG_SWITCHNODE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_LGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_COMP MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7804 8.06K 1% 1/16W MF-LF 402
C7808 0.047UF 10% 16V CERM 402
3V3REG_COMP_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7806 560PF 10% 50V CERM 402

CRITICAL Q7800 IRLR7807Z TO-252AA
CRITICAL Q7801 IRLR7807Z TO-252AA
CRITICAL C7853 1000UF 20% 16V ELEC TH-KZJ-LF
C7811 10UF 10% 16V X5R-CERM 1210

L7803 3.0UH TH1 CRITICAL
PP3V3_S5 3.35V NOMINAL
R7802 5.11 1% 1/4W MF-LF 1206
3V3REG_SNUB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7809 1000PF 5% 50V CERM 1206
D7800 CTLSH3-30M833 TLM833
nostuff
C7802 1000PF 10% 25V X7R 402

CRITICAL C7815 1800UF 20% 6.3V ELEC TH-KZJ-LF
C7814 10UF 20% 6.3V CERM 805-1
C7813 10UF 20% 6.3V CERM 805-1

PP2V5_S5 2.50V NOMINAL
C7825 10UF 20% 6.3V CERM 805-1
C7822 10UF 20% 6.3V CERM 805-1
C7821 10UF 20% 6.3V CERM 805-1
C7826 10UF 20% 6.3V CERM 805-1
R7820 1K 1% 1/16W MF-LF 402
R7821 2.7K 5% 1/16W MF-LF 402
C7824 1000PF 10% 25V X7R 402
2V5_LDODR_C nostuff MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_LDO_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7822 470 1% 1/16W MF-LF 402

XW7800 SM

R7899 22 5% 1/16W MF-LF 402
3V3REG_FB_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7807 0.01UF 10% 16V CERM 402
R7803 1.24K 1% 1/16W MF-LF 402 (R2)
R7801 392 1% 1/16W MF-LF 402 (R1)

5% OK ON R7801?
VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN
0.800V TYP
0.816V MAX

3V3REG_FS_DIS MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7892 100K 5% 1/16W MF-LF 402
NOSTUFF
Q7802 2N7002 SOT23-LF
SYS_POWERFAIL_L
C7803 4.7UF 20% 6.3V CERM 603
3V3REG_GND VOLTAGE=0 V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

PP5V_S5
PP3V3_S5
R7811 2.49K 1% 1/16W MF-LF 402
C7880 0.1UF 20% 10V CERM 402
R7810 10K 1% 1/16W MF-LF 402
2V2_REF 2.219V
U7810 LM339A SOI-LF
PGOOD_PP2V5_S0
PP2V5_S0
R7812 5.11K 1% 1/16W MF-LF 402

PP2V5_S0
U7810 LM339A SOI-LF
SPARE COMPARATOR

3V DC/DC 2.5V

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7039
REV. A
SCALE NONE
SHT 78 OF 97
TRUE

1.8V AND 1.2V S3 REGULATOR

1.2V S3
POWER BUDGET
PEAK=0.4A
AVE=0.3A

=PP1V8_S3_1V2_LDO
C7920 22UF 20% 6.3V X5R 805
CRITICAL Q7903 IRF1902PBF SO-8

C7992 1UF 10% 25V X5R 603
PP12V_S5

VCC12 U7900 ISL6549 QFN
CRITICAL
VCC5 PVCC5 LDO_DR LDO_FB FS_DIS THRML_PAD DGND AGND PGND
UGATE BOOT PHASE LGATE FB COMP

C7900 1UF 10% 6.3V CERM 402
1V8REG_DDR_VCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7905 10 1% 1/16W MF-LF 402
1V8REG_DDR_PVCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_LDO_DR MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7923 1000PF 10% 25V X7R 402
1V2_LDODR_C nostuff MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7921 2.7K 5% 1/16W MF-LF 402
C7924 1000PF 10% 25V X7R 402
1V8REG_DDR_LDO_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

PP1V2_S3 1.21V NOMINAL
C7925 10UF 20% 6.3V CERM 805-1
C7922 10UF 20% 6.3V CERM 805-1
C7921 10UF 20% 6.3V CERM 805-1
C7926 10UF 20% 6.3V CERM 805-1
R7920 1K 1% 1/16W MF-LF 402
R7922 1.96K 1% 1/16W MF-LF 402

1V8REG_DDR_UGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7940 2.2 5% 1/16W MF-LF 402
1V8REG_DDR_BOOT MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_BOOT_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7901 0.1UF 20% 25V CERM 603
1V8REG_DDR_SWITCHNODE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_LGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_COMP MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7904 8.06K 1% 1/16W MF-LF 402
C7908 0.047UF
1V8REG_DDR_COMP_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7906 560PF 10% 50V CERM 402

Q7900 IRLR7807Z TO-252AA
Q7901 IRLR7807Z TO-252AA
D7900 CTLSH3-30M833 TLM833
nostuff
C7902 1000PF 10% 25V X7R 402

L7903 1.53UH TH-LF CRITICAL
C7953 680UF 20% 16V ELEC TH-MCZ
C7954 680UF 20% 16V ELEC TH-MCZ
C7911 10UF 10% 16V X5R-CERM 1210
C7912 10UF 10% 16V X5R-CERM 1210
C7956 1500UF 20% 6.3V ELEC TH-MCZ
C7957 1500UF 20% 6.3V ELEC TH-MCZ
C7913 10UF 20% 6.3V CERM 805-1
C7958 1UF 10% 6.3V CERM 402
C7959 1UF 10% 6.3V CERM 402
C7960 1UF 10% 6.3V CERM 402
PP1V8_S3 1.81V NOMINAL

1.8V S3
M51
POWER BUDGET
PEAK=14.5A
TOTAL=6.3A

R7902 5.11 1% 1/4W MF-LF 1206
1V8REG_DDR_SNUB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7909 1000PF 5% 50V CERM 1206

R7999 22 5% 1/16W MF-LF 402
R7903 1.24K 1% 1/16W MF-LF 402 (R2)
1V8REG_DDR_FB_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7907 0.01UF 10% 16V CERM 402
R7901 953 1% 1/16W MF-LF 402 (R1)

VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN
0.800V TYP
0.816V MAX

XW7900 SM

1V8REG_DDR_FS_DIS MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7992 100K 5% 1/16W MF-LF 402
Q7902 2N7002 SOT23-LF
PM_SLP_S4
C7903 4.7UF 20% 6.3V CERM 603
1V8REG_DDR_GND VOLTAGE=0 V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

PM_SLP_S3_L — MEMVTT_EN

PP5V_S5
PP3V3_S5
R7911 5.49K 1% 1/16W MF-LF 402
R7910 10K 1% 1/16W MF-LF 402
1V2_REF 1.21V
U7810 LM339A SOI-LF GND V+
PGOOD_PP1V8_S3
R7912 2.7K 5% 1/16W MF-LF 402

PP5V_S5
PP3V3_S5
R7914 8.45K 1% 1/16W MF-LF 402
R7913 10K 1% 1/16W MF-LF 402
0V7_REF 0.723V
U7810 LM339A SOI-LF GND V+
PP0V9_S0
PGOOD_PP0V9_S0
R7915 2.37K 1% 1/16W MF-LF 402

PP3V3_S5
R7906 330 5% 1/16W MF-LF 402
DEVELOPMENT
LED_PP1V8_S3_P
DEVELOPMENT LED7900 GREEN-3.6MCD 2.0X1.25MM-SM
PLACE_LED NEAR VREG
PP1V8_S3
1V0_REF
U7901 DEVELOPMENT LM339A SOI-LF GND V+
LED_PP1V8_S3_N

1.8V & 1.2V VREG

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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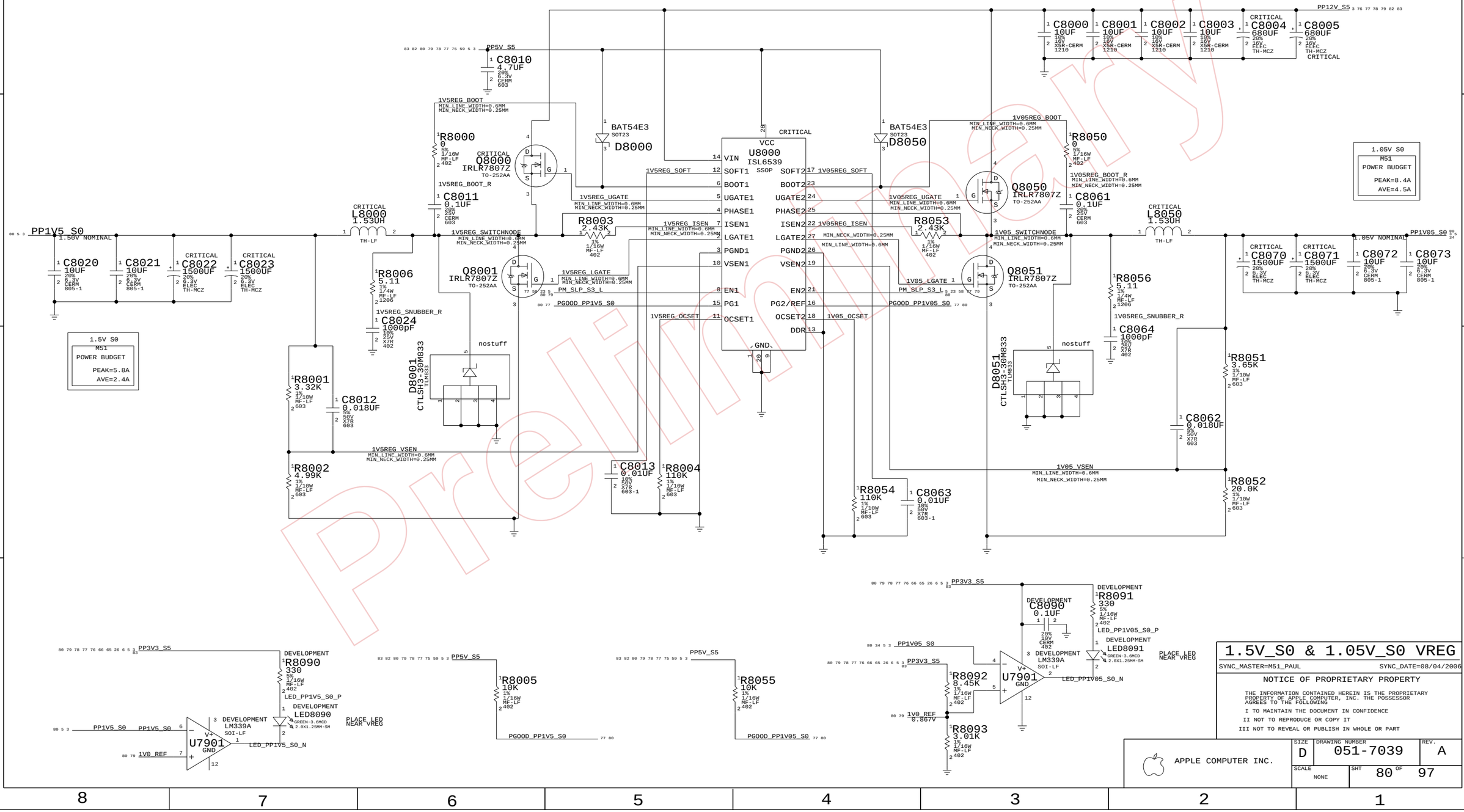
D	051-7039	A
SCALE: NONE	SHT 79 OF 97	

1.5V S0 AND 1.05V S0 RAILS



1.5V_S0 & 1.05V_S0 VREG		
SYNC_MASTER=M51_PAUL	SYNC_DATE=08/04/2006	

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	A
	SCALE: NONE	SHT 80 OF 97	

5V S5 AND 5V AUDIO S5 REGULATOR

=PP5V_S5_AUDIO_LDO
C8220 22UF 20% 6.3V X5R 805
CRITICAL Q8203 IRF1902PBF SO-8
5V AUDIO S5 — M50 POWER BUDGET: AUDIO=?A TOTAL=?A
PP4V5_S5_AUDIO_ANALOG 4.50V NOMINAL
C8225 10UF 20% 6.3V CERM 805-1
C8222 10UF 20% 6.3V CERM 805-1
C8221 10UF 20% 6.3V CERM 805-1
C8226 10UF 20% 6.3V CERM 805-1
R8220 1K 1% 1/16W MF-LF 402
R8222 221 1% 1/16W MF-LF 402
C8223 1000PF 10% 25V X7R 402
R8221 2.7K 5% 1/16W MF-LF 402
NOSTUFF C8224 1000PF 10% 25V X7R 402
5V_AUDIO_LDODR_C MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_LDO_DR MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_LDO_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

PP12V_S5
C8292 1UF 10% 25V X5R 603
C8200 1UF 10% 6.3V CERM 402
5VREG_VCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8205 10 1% 1/10W MF-LF 402
5VREG_PVCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

U8200 ISL6549 QFN
VCC12
VCC5
PVCC5 CRITICAL
LDO_DR
LDO_FB
FS_DIS
THRML_PAD
DGND AGND PGND
UGATE
BOOT
PHASE
LGATE
FB
COMP

5VREG_UGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_BOOT MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8240 2.2 5% 1/16W MF-LF 402
5VREG_BOOT_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8201 0.1UF 20% 25V CERM 603
5VREG_SWITCHNODE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_LGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_COMP MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8204 8.06K 1% 1/16W MF-LF 402
5VREG_COMP_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8206 470PF 10% 50V CERM 402
C8208 0.047UF 10% 16V CERM 402
C8202 1000PF 10% 25V X7R 402

CRITICAL Q8200 IRLR7807Z TO-252AA
CRITICAL Q8201 IRLR7807Z TO-252AA
NOSTUFF D8200 CTLSH3-30M833 TLM833
CRITICAL C8253 1000UF 20% 16V ELEC TH-KZJ-LF
C8211 10UF 20% 16V X5R-CERM 1210
L8203 3.0UH TH1 CRITICAL
5V S5 — M50 POWER BUDGET: MISC=1.500A USB=1.500A AUDIO=1.000A ODD=1.000A TOTAL=5.000A
PP5V_S5 5.10V NOMINAL
R8202 5.11 1% 1/4W MF-LF 1206
5VREG_SNUB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8209 1000PF 5% 50V CERM 1206
CRITICAL C8215 1800UF 20% 6.3V ELEC TH-KZJ-LF
C8214 10UF 20% 6.3V CERM 805-1
C8213 10UF 20% 6.3V CERM 805-1
R8299 22 5% 1/16W MF-LF 402
R8203 1.24K 1% 1/16W MF-LF 402 (R2)
5VREG_FB_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8207 0.01UF 10% 16V CERM 402
R8201 232 1% 1/16W MF-LF 402 (R1)

VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN, 0.800V TYP, 0.816V MAX

XW8200 SM

5VREG_FS_DIS MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8292 100K 5% 1/10W MF-LF 402
NOSTUFF Q8202 2N7002 SOT23-LF
SYS_POWERFAIL_L
C8203 4.7UF 20% 6.3V CERM 603
5VREG_GND VOLTAGE=0 V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

POWER SUPPLY 3.3V/5V MAIN SWITCH

5V DC/DC

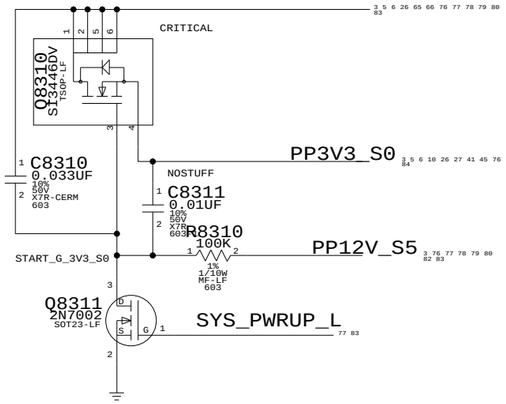
SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

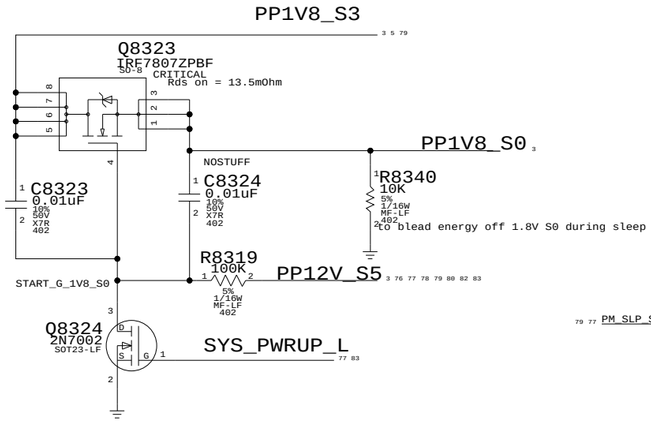
SIZE	DRAWING NUMBER	REV.
D	051-7039	A

SCALE: NONE SHT 82 OF 97

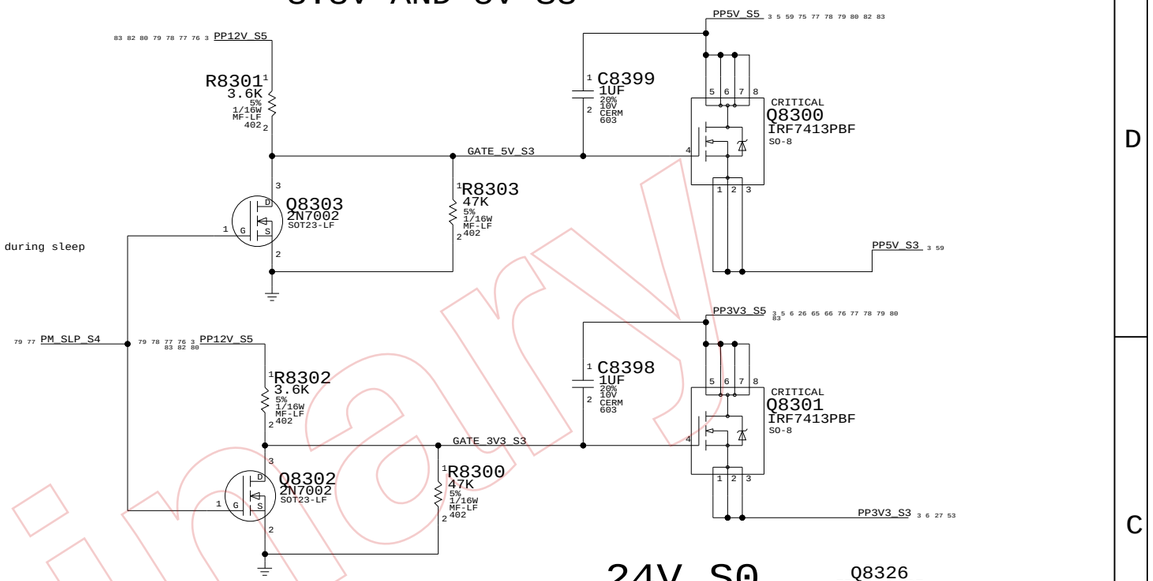
3.3V S0



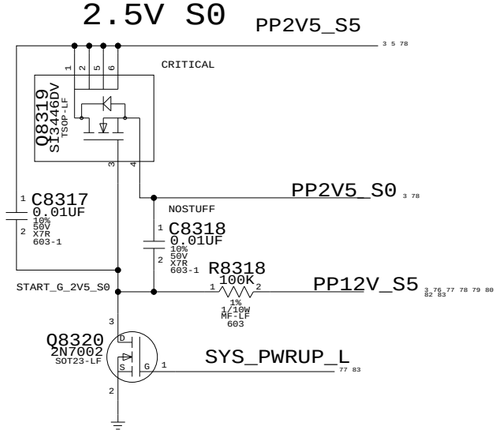
1.8V S0



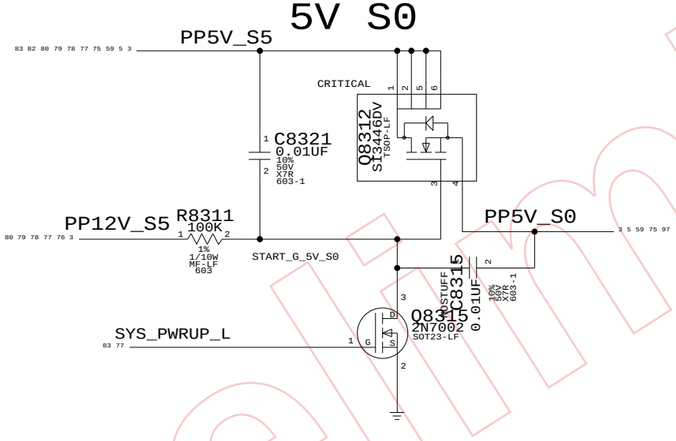
3.3V AND 5V S3



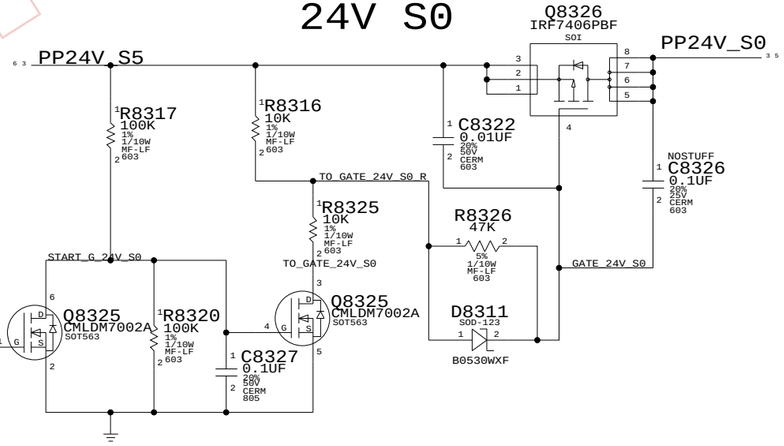
2.5V S0



5V S0

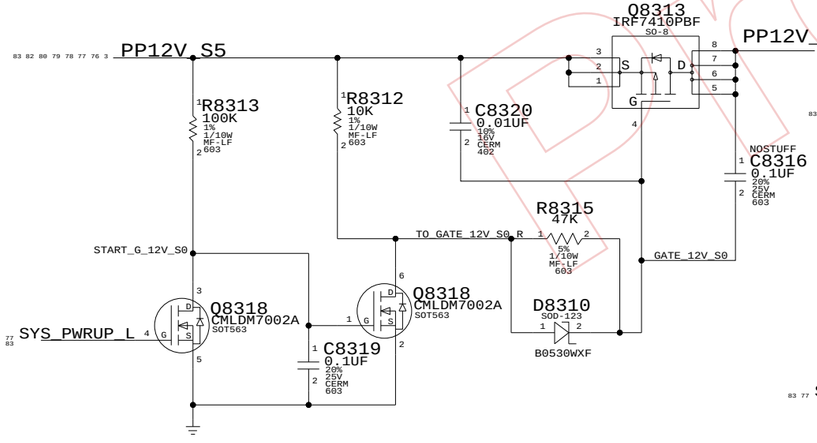


24V S0

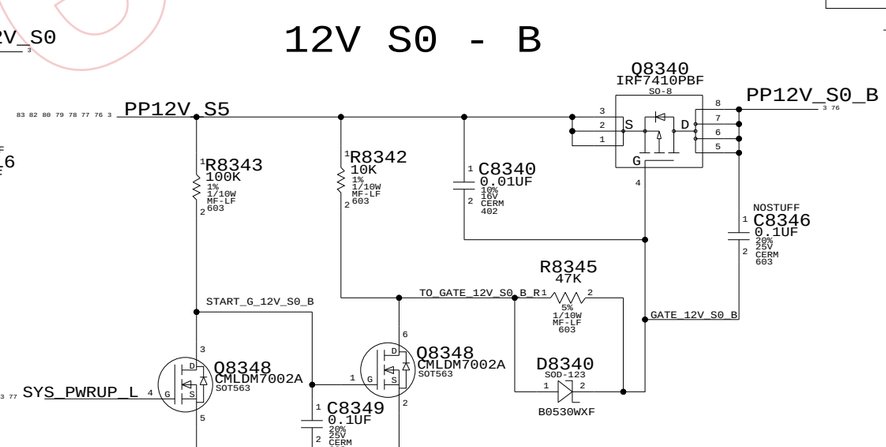


12V S0

Split 12V S0 is for better power plane structure
12VS0 - B will connect to MXM, Audio, Fans



12V S0 - B



S0 AND S3 FETS

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 83 OF 97	

Page Notes

Power aliases required by this page:
- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

M51: FIX ON CARD ALLOWS US TO NOT STUFF MOST OF THE 1.8V DECOUPLING, WITH NO DROOP OR NOISE

MXM PWRSRC (GPU CORE) CURRENT SENSE

=PPV_S0_MXM_PWRSRC → CRITICAL R8450 0.025 1% 1W MF 2512-1 → PPV_S0_MXM_PWRSRC

PCB:KEEP SHORTS NEXT TO U8450
PCB:PLACE D8450,R8452,C8458 BY SMC

MXM_PWR_SENSE
CRITICAL U8450 ZXCT1010 SOT23-5
VIN, IOUT, NC, LOAD, GND

PP3V3_S0 → D8450 BAS16-75V-0.25A SOT23-LF (NOSTUFF) → TO SMC

XW8450 SM (OMIT)
MXM_PWRSRC_SENSE → MXM_SENSE_I_R

MXM_PWR_SENSE R8452 4.53K 1% 1/16W MF-LF 402 → SMC_GPU_ISENSE

MXM_PWR_SENSE R8451 3.01K 1% 1/16W MF-LF 402

MXM_PWR_SENSE C8458 0.22UF 20% 6.3V X5R 402 → GND_SMC_AVSS
1 MS TIME CONSTANT SO SMC ADC SAMPLING WORKS WELL.

SCALE	COUNT
1.33333 A/V	.004296875 A/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

MXM PWRSRC VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

PPV_S0_MXM_PWRSRC

MXM_PWR_SENSE R8453 6.04K 1% 1/16W MF-LF 402

MXM_PWR_SENSE R8454 2.0K 1% 1/16W MF-LF 402

SMC_MXM_VSENSE_R

MXM_PWR_SENSE R8455 4.53K 1% 1/16W MF-LF 402 → SMC_GPU_VSENSE

PCB: PLACE R8455, C8459 WITHIN 1" OF SMC (U5800)

MXM_PWR_SENSE C8459 0.22UF 20% 6.3V X5R 402 → GND_SMC_AVSS

SCALE	COUNT
4 V/V	.0129 V/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

=PP1V8_S0_MXM

C8401 22UF 20% 6.3V X5R 805
C8402 22UF (NOSTUFF) 20% 6.3V X5R 805
C8403 22UF (NOSTUFF) 20% 6.3V X5R 805

=PP5V_S0_MXM

ALL_SYS_PWRGD

PLACE CAPS NEAR NB

PRSNT2_L: RESERVED FOR FUTURE USE

CRITICAL
J8400 B33@102-0123 F-RT-SM (1 OF 2)

PPV_S0_MXM_PWRSRC (VOLTAGE=12V MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.25MM)

C8400 22UF 20% 35V ELEC SM-LF

KEY

2	1V8RUN0	PWR_SRC0	1				
4	1V8RUN1	PWR_SRC1	3				
6	1V8RUN2	PWR_SRC2	5				
8	1V8RUN3	PWR_SRC3	7				
10	1V8RUN4	PWR_SRC4	9				
12	1V8RUN5	PWR_SRC5	11				
14	1V8RUN6	PWR_SRC6	13				
16	RUNPWROK	PWR_SRC7	15				
18	5VRUN	GND0	17				
20	GND20	GND1	19				
22	GND21	GND2	21				
24	GND22	GND3	23				
38	PRSNT2_L	PEX_RX15_L	37	PEG_D2R_P<0>			
40	PEX_TX15_L	PEX_RX15	39	PEG_D2R_N<0>			
42	PEX_TX15	GND4	41				
44	GND23	PEX_RX14_L	43	PEG_D2R_P<1>			
46	PEX_TX14_L	PEX_RX14	45	PEG_D2R_N<1>			
48	PEX_TX14	GND5	47				
50	GND24	PEX_RX13_L	49	PEG_D2R_P<2>			
52	PEX_TX13_L	PEX_RX13	51	PEG_D2R_N<2>			
54	PEX_TX13	GND6	53				
56	GND25	PEX_RX12_L	55	PEG_D2R_P<3>			
58	PEX_TX12_L	PEX_RX12	57	PEG_D2R_N<3>			
60	PEX_TX12	GND7	59				
62	GND26	PEX_RX11_L	61	PEG_D2R_P<4>			
64	PEX_TX11_L	PEX_RX11	63	PEG_D2R_N<4>			
66	PEX_TX11	GND8	65				
68	GND27	PEX_RX10_L	67	PEG_D2R_P<5>			
70	PEX_TX10_L	PEX_RX10	69	PEG_D2R_N<5>			
72	PEX_TX10	GND9	71				
74	GND28	PEX_RX9_L	73	PEG_D2R_P<6>			
76	PEX_TX9_L	PEX_RX9	75	PEG_D2R_N<6>			
78	PEX_TX9	GND10	77				
80	GND29	PEX_RX8_L	79	PEG_D2R_P<7>			
82	PEX_TX8_L	PEX_RX8	81	PEG_D2R_N<7>			
84	PEX_TX8	GND11	83				
86	GND30	PEX_RX7_L	85	PEG_D2R_P<8>			
88	PEX_TX7_L	PEX_RX7	87	PEG_D2R_N<8>			
90	PEX_TX7	GND12	89				
92	GND31	PEX_RX6_L	91	PEG_D2R_P<9>			
94	PEX_TX6_L	PEX_RX6	93	PEG_D2R_N<9>			
96	PEX_TX6	GND13	95				
98	GND32	PEX_RX5_L	97	PEG_D2R_P<10>			
100	PEX_TX5_L	PEX_RX5	99	PEG_D2R_N<10>			
102	PEX_TX5	GND14	101				
104	GND33	PEX_RX4_L	103	PEG_D2R_P<11>			
106	PEX_TX4_L	PEX_RX4	105	PEG_D2R_N<11>			
108	PEX_TX4	GND15	107				
110	GND34	PEX_RX3_L	109	PEG_D2R_P<12>			
112	PEX_TX3_L	PEX_RX3	111	PEG_D2R_N<12>			
114	PEX_TX3	GND16	113				
116	GND35	PEX_RX2_L	115	PEG_D2R_P<13>			
118	PEX_TX2_L	PEX_RX2	117	PEG_D2R_N<13>			
120	PEX_TX2	GND17	119				
122	GND36	PEX_RX1_L	121	PEG_D2R_P<14>			
124	PEX_TX1_L	PEX_RX1	123	PEG_D2R_N<14>			
126	PEX_TX1	GND18	125				
128	GND37	PEX_RX0_L	127	PEG_D2R_P<15>			
130	PEX_TX0_L	PEX_RX0	129	PEG_D2R_N<15>			
132	PEX_TX0	GND19	131				

PEG_R2D_C_P<0>	C8420	0.1uF	16V 10% X5R 402	PEG_R2D_P<15>
PEG_R2D_C_N<0>	C8421	0.1uF		PEG_R2D_N<15>
PEG_R2D_C_P<1>	C8422	0.1uF		PEG_R2D_P<14>
PEG_R2D_C_N<1>	C8423	0.1uF		PEG_R2D_N<14>
PEG_R2D_C_P<2>	C8424	0.1uF		PEG_R2D_P<13>
PEG_R2D_C_N<2>	C8425	0.1uF		PEG_R2D_N<13>
PEG_R2D_C_P<3>	C8426	0.1uF		PEG_R2D_P<12>
PEG_R2D_C_N<3>	C8427	0.1uF		PEG_R2D_N<12>
PEG_R2D_C_P<4>	C8428	0.1uF		PEG_R2D_P<11>
PEG_R2D_C_N<4>	C8429	0.1uF		PEG_R2D_N<11>
PEG_R2D_C_P<5>	C8430	0.1uF		PEG_R2D_P<10>
PEG_R2D_C_N<5>	C8431	0.1uF		PEG_R2D_N<10>
PEG_R2D_C_P<6>	C8432	0.1uF		PEG_R2D_P<9>
PEG_R2D_C_N<6>	C8433	0.1uF		PEG_R2D_N<9>
PEG_R2D_C_P<7>	C8434	0.1uF		PEG_R2D_P<8>
PEG_R2D_C_N<7>	C8435	0.1uF		PEG_R2D_N<8>
PEG_R2D_C_P<8>	C8436	0.1uF		PEG_R2D_P<7>
PEG_R2D_C_N<8>	C8437	0.1uF		PEG_R2D_N<7>
PEG_R2D_C_P<9>	C8438	0.1uF		PEG_R2D_P<6>
PEG_R2D_C_N<9>	C8439	0.1uF		PEG_R2D_N<6>
PEG_R2D_C_P<10>	C8440	0.1uF		PEG_R2D_P<5>
PEG_R2D_C_N<10>	C8441	0.1uF		PEG_R2D_N<5>
PEG_R2D_C_P<11>	C8442	0.1uF		PEG_R2D_P<4>
PEG_R2D_C_N<11>	C8443	0.1uF		PEG_R2D_N<4>
PEG_R2D_C_P<12>	C8444	0.1uF		PEG_R2D_P<3>
PEG_R2D_C_N<12>	C8445	0.1uF		PEG_R2D_N<3>
PEG_R2D_C_P<13>	C8446	0.1uF		PEG_R2D_P<2>
PEG_R2D_C_N<13>	C8447	0.1uF		PEG_R2D_N<2>
PEG_R2D_C_P<14>	C8448	0.1uF		PEG_R2D_P<1>
PEG_R2D_C_N<14>	C8449	0.1uF		PEG_R2D_N<1>
PEG_R2D_C_P<15>	C8450	0.1uF		PEG_R2D_P<0>
PEG_R2D_C_N<15>	C8451	0.1uF		PEG_R2D_N<0>

MXM PCI-E & PWR

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A

SCALE: NONE SHT 84 OF 97

Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

Signal aliases required by this page:
- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

BOM options provided by this page:
(NONE)

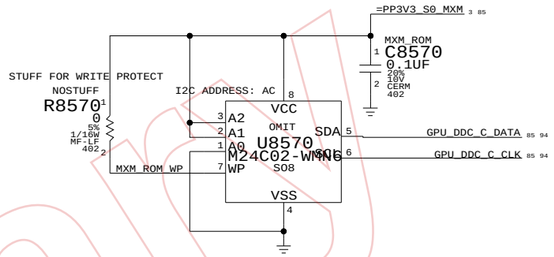
MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

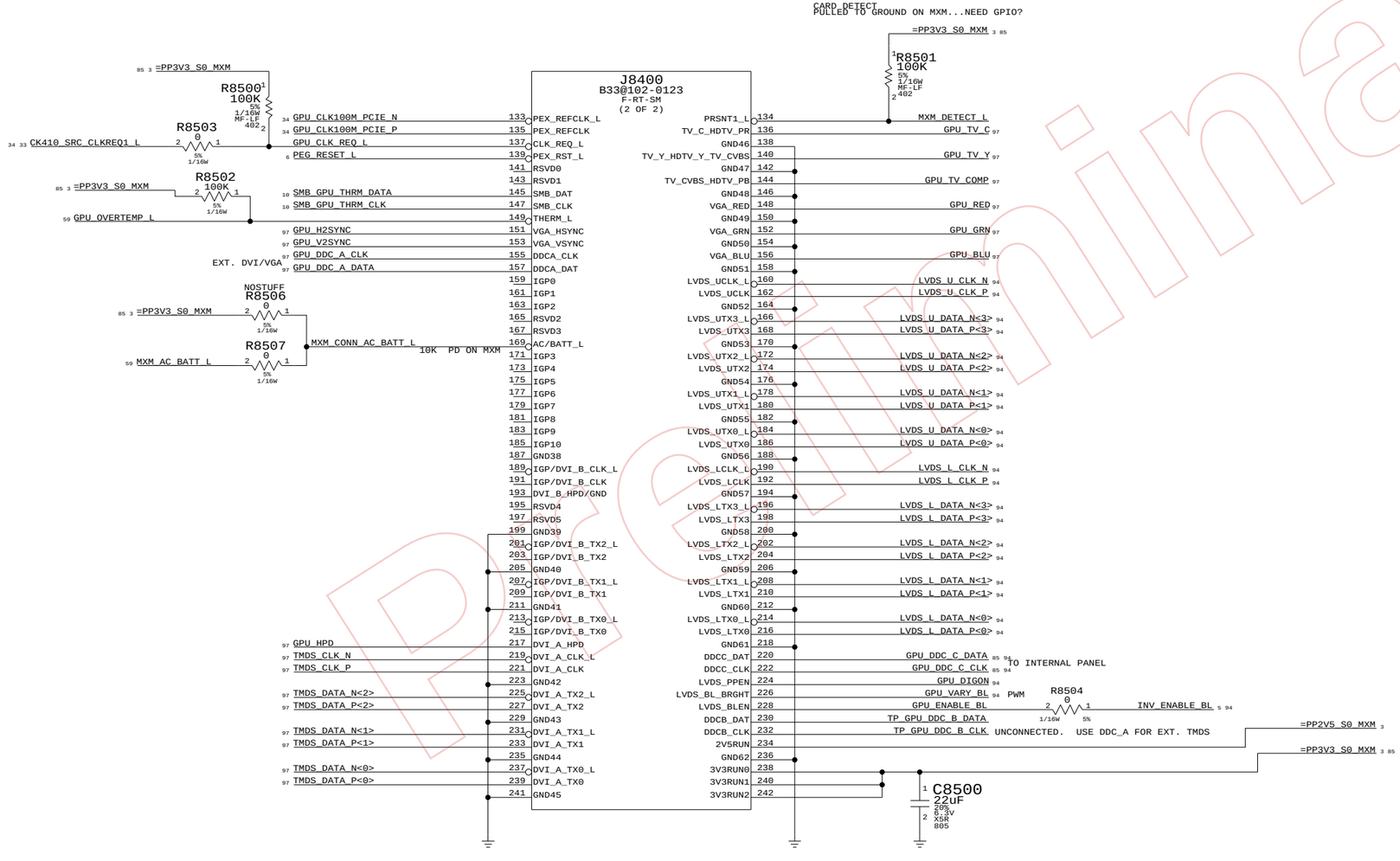
VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



CARD DETECT
PULLED TO GROUND ON MXM...NEED GPIO?



MXM I/O

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 85 OF 97	

Page Notes

Power aliases required by this page:
- =PP12V_LCD
- =PP24V_INVERTER
- =PP3V3_S0_VIDEO

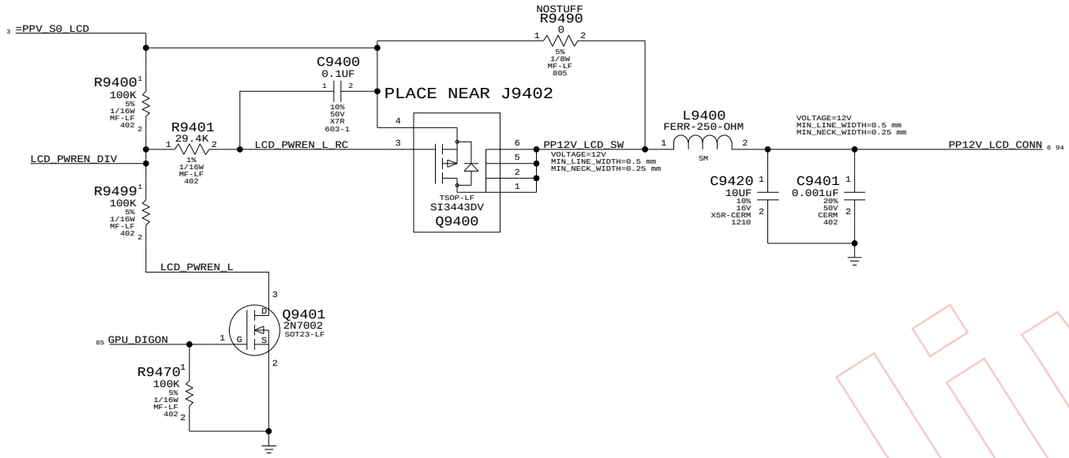
Signal aliases required by this page:
(NONE)

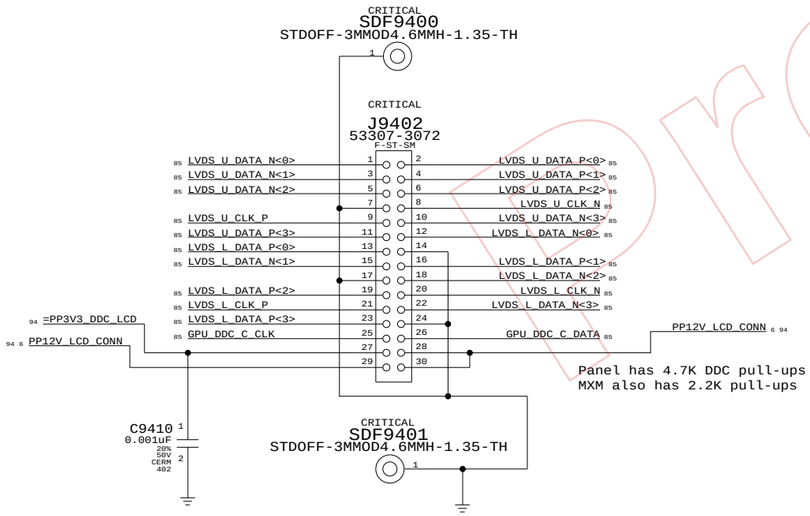
BOM options provided by this page:
(NONE)

97 94 3 =PP3V3_S0_VIDEO ═══ =PP3V3_DDC_LCD 94

LCD (LVDS) INTERFACE

PANEL POWER SEQUENCING

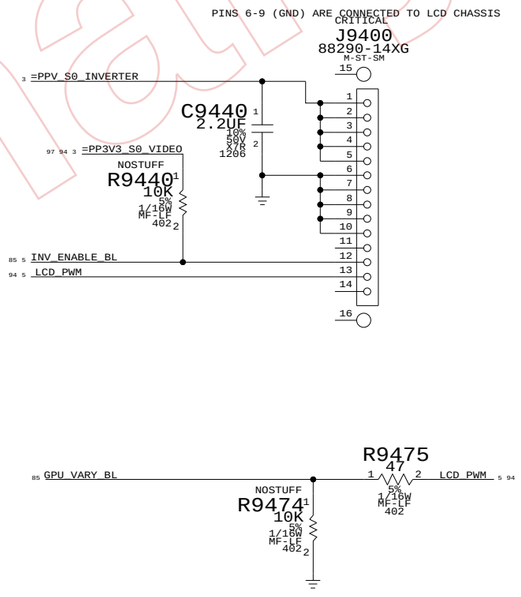




Panel has 4.7K DDC pull-ups
MXM also has 2.2K pull-ups

INVERTER INTERFACE

PINS 6-9 (GND) ARE CONNECTED TO LCD CHASSIS



Internal Display Conns

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A

SCALE	SHT
NONE	94 OF 97

DVI INTERFACE

TMDS TERMINATION, IF ANY, IS ON MXM CARD

PLACE FILTER CLOSE TO MINI-DVI CONNECTOR

TMDS_DATA_N<0> — NOSTUFF R9700 0 — L9700 90-OHM-SM CRITICAL — R9790 49.9 1% 1/16W MF-LF 402 — R9791 49.9 1% 1/16W MF-LF 402 — TMDS_CONN_DN<0>
TMDS_DATA_P<0> — NOSTUFF R9702 0 — TMDS_CONN_DP<0>
TMDS_DATA_N<1> — NOSTUFF R9703 0 — L9701 90-OHM-SM CRITICAL — R9792 49.9 1% 1/16W MF-LF 402 — R9793 49.9 1% 1/16W MF-LF 402 — TMDS_CONN_DN<1>
TMDS_DATA_P<1> — NOSTUFF R9705 0 — TMDS_CONN_DP<1>
TMDS_DATA_N<2> — NOSTUFF R9704 0 — L9702 90-OHM-SM CRITICAL — R9794 49.9 1% 1/16W MF-LF 402 — R9795 49.9 1% 1/16W MF-LF 402 — TMDS_CONN_DN<2>
TMDS_DATA_P<2> — NOSTUFF R9709 0 — TMDS_CONN_DP<2>
=PP3V3_S0_VIDEO 3 94 97

TMDS_CLK_N — NOSTUFF R9708 0 — L9703 90-OHM-SM CRITICAL — TMDS_CONN_CLKN
TMDS_CONN_CLKP
TMDS_CLK_P — NOSTUFF R9715 0

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

PP5V_S0 — D9710 SOD-123 B0530WXF — PP5V_S0_DDC_DIODE (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm) — CRITICAL F9710 0.5AMP-13.2V SM-LF — PP5V_S0_DDC_FUSE (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm) — L9710 400-OHM-EMI SM-1 — PP5V_S0_DDC (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

CRITICAL J9710 MINI-DVI-M51 F-ST-SM

DVI_HPD_UF	25	1	TMDS_CONN_DP<2>
	17	9	
DVI_DDC_CLK_UF	26	2	TMDS_CONN_DN<2>
DVI_DDC_DATA_UF	18	10	
	27	3	TMDS_CONN_DP<1>
	19	11	
	28	4	TMDS_CONN_DN<1>
VGA_BLU	20	12	
VGA_HSYNC	29	5	TMDS_CONN_DP<0>
		13	
	30	6	TMDS_CONN_DN<0>
VGA_GRN	22	14	
VGA_VSYNC	31	7	TMDS_CONN_CLKP
		15	
	32	8	TMDS_CONN_CLKN
VGA_RED	24	16	
	33	34	

DVI_CHASSIS 33 — C9720 0.1UF 10% 16V X5R 402 — C9721 0.1UF 10% 16V X5R 402 — GND_CHASSIS_DVI 6

PLACE CLOSE TO MINI-DVI CONNECTOR
3V LEVEL SHIFTERS

PP5V_S0_DDC — R9710 4.7K 5% 1/16W MF-LF 402 — R9712 4.7K 5% 1/16W MF-LF 402

DVI_DDC_CLK_UF — R9711 100 5% 1/16W MF-LF 402 — C9711 100pF 5% 50V CERM 402 — Q9711 2N7002DW-X-F SOT-363 — DVI_DDC_CLK — R9720 10K 5% 1/16W MF-LF 402 — GPU_DDC_A_CLK
DVI_DDC_DATA_UF — R9713 100 5% 1/16W MF-LF 402 — C9713 100pF 5% 50V CERM 402 — Q9711 2N7002DW-X-F SOT-363 — DVI_DDC_DATA — R9721 10K 5% 1/16W MF-LF 402 — GPU_DDC_A_DATA
DVI_HPD_UF — R9714 0 5% 1/16W MF-LF 402 — GPU_HPD

C9710 0.01uF 20% 50V CERM 603 — C9714 100pF 5% 50V CERM 402

NOSTUFF R9722 100K 5% 1/16W MF-LF 402 — NOSTUFF D9700 CASE425 MMSZ4681XXG

Note: this clamp is supposed to be on the MXM card

ANALOG FILTERING

PLACE CLOSE TO CONNECTOR

=PP3V3_S0_VIDEO — C9730 0.1UF 20% 10V CERM 402 — C9731 10uF 20% 6.3V CERM 805-1

U9730 SOP TS3V330 CRITICAL

GPU_TV_C	S1A	DA	VIDEO_MUX_RED
GPU_RED	S2A		
GPU_TV_Y	S1B	DB	VIDEO_MUX_GRN
GPU_GRN	S2B		
GPU_TV_COMP	S1C	DC	VIDEO_MUX_BLU
GPU_BLU	S2C		
NC	S1D	DD	NC
NC	S2D	IN	SB_CRT_TVOUT_MUX
		EN_L	
	VCC	GND	

R9740 150 1% 1/16W MF-LF 402 — NOSTUFF C9743 10PF 5% 50V CERM 402 — OMIT L9740 27NH 0402 — C9740 10PF 5% 50V CERM 402 — VGA_BLU
R9741 150 1% 1/16W MF-LF 402 — NOSTUFF C9744 10PF 5% 50V CERM 402 — OMIT L9741 27NH 0402 — C9741 10PF 5% 50V CERM 402 — VGA_GRN
R9742 150 1% 1/16W MF-LF 402 — NOSTUFF C9745 10PF 5% 50V CERM 402 — OMIT L9742 27NH 0402 — C9742 10PF 5% 50V CERM 402 — VGA_RED

PLACE R9760 & R9761 CLOSE TO DVI CONNECTOR

=PP3V3_S0_VIDEO — C9760 0.1UF 20% 10V CERM 402

GPU_V2SYNC — U9760 74LC125 125 TSSOP — GPU_VSYNC_BUF — R9760 33 5% 1/16W MF-LF 402 — VGA_VSYNC_R — OMIT L9760 27NH 0402 — VGA_VSYNC
GPU_H2SYNC — U9760 74LC125 125 TSSOP — GPU_HSYNC_BUF — R9761 33 5% 1/16W MF-LF 402 — VGA_HSYNC_R — OMIT L9761 27NH 0402 — VGA_HSYNC

C9762 10PF 5% 50V CERM 402 — C9763 10PF 5% 50V CERM 402

DISABLE UNUSED BUFFERS

U9760 74LC125 125 TSSOP — U9760 74LC125 125 TSSOP

=PP3V3_S0_VIDEO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0469	5	27NH,402,INDUCTOR,MAGLAYERS	L9740,L9741,L9742,L9760,L9761	

External Display Conns

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	A
SCALE: NONE	SHT 97 OF 97	