1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB-PRQ,M59

02/12/2007

BOM Update for Post Ramp Qualifications

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
B		486797	PRODUCTION RELEASED	02/12/07	

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7270	1	SCHEM,MLB-PRQ,M59	SCH	CRITICAL	
820-2054	1	PCBF,MLB,M59	PCB	CRITICAL	

DRAWING
TITLE=M59_MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 12 10:35:04 2007

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

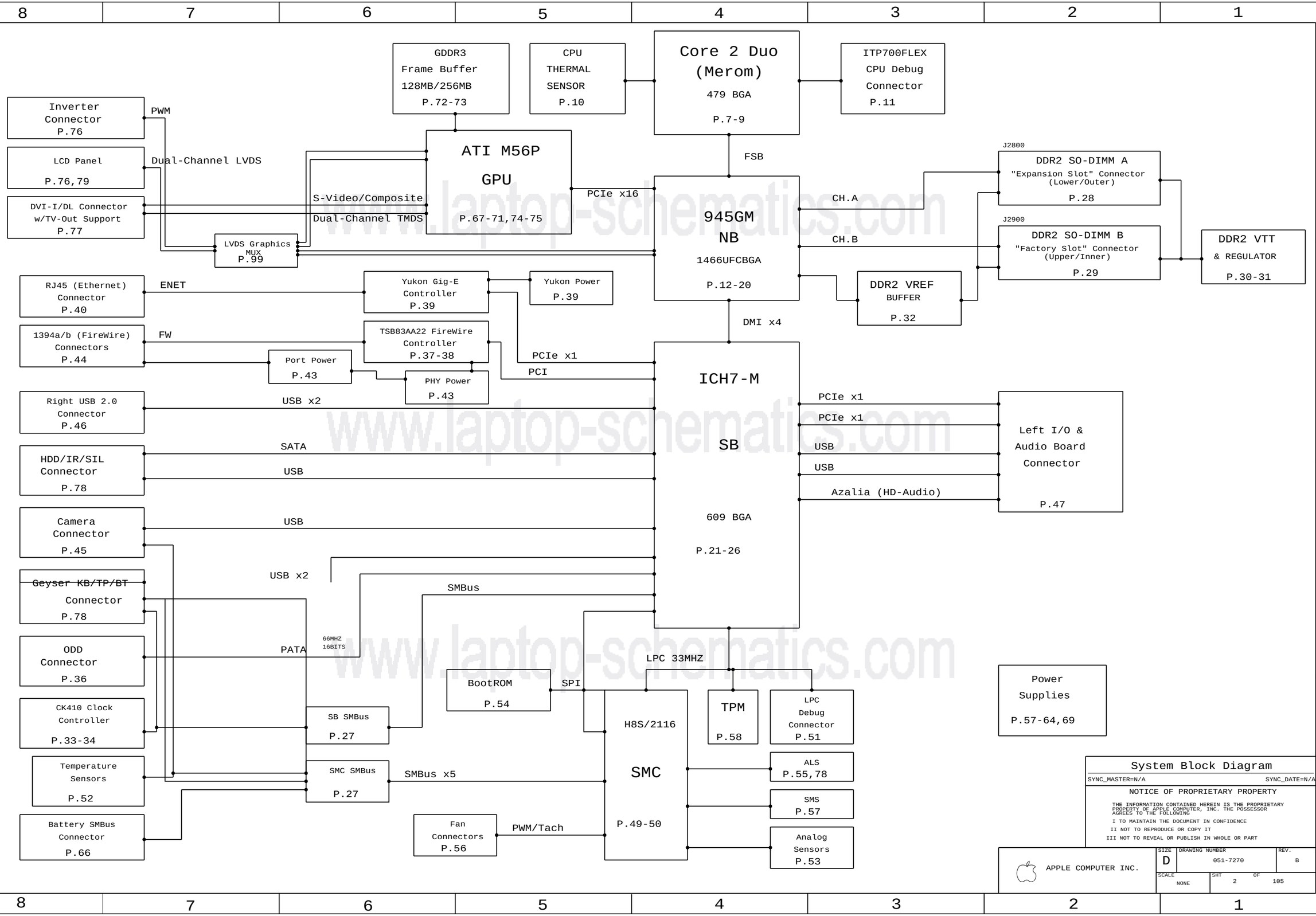
SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB-PRQ,M59

DRAWING NUMBER 051-7270 REV. B

SHT 1 OF 105



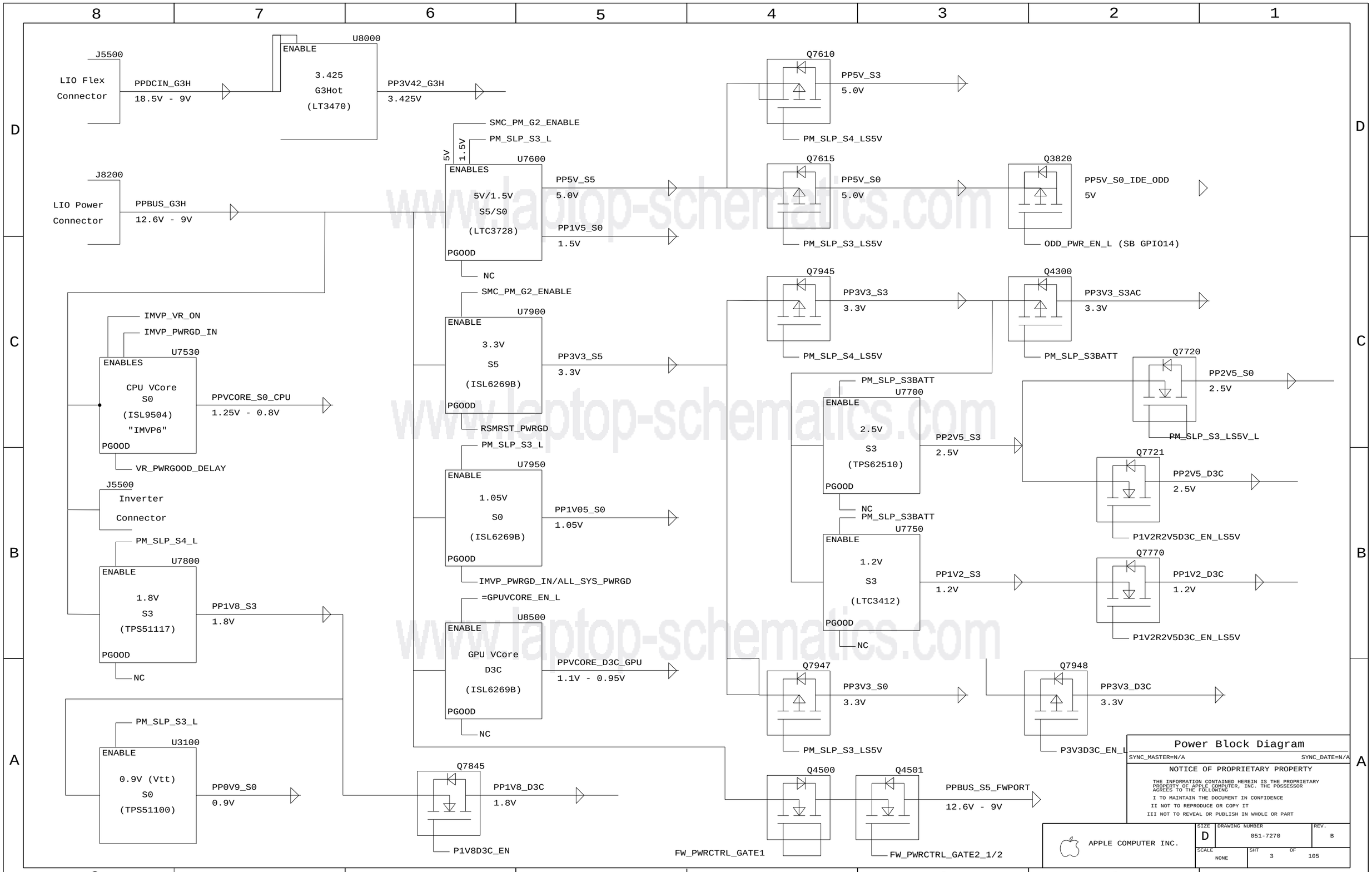
System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE	SHT	OF
NONE	2	105



Original Production BOMs (SS VRAM, All SS/MU Caps)

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7849	PCBA,2.16,128VR-SS,SAM-CAP,M59,MBP15	EEE_WTE,M59_COMMON,CPU_2_16GHZ,VRAM_SAM128,CAP22UF_ALLSAM,ODD_NONLOCK_CONN
630-7919	PCBA,2.16,128VR-SS,MUR-CAP,M59,MBP15	EEE_X34,M59_COMMON,CPU_2_16GHZ,VRAM_SAM128,CAP22UF_ALLMURA,ODD_NONLOCK_CONN
630-7851	PCBA,2.33,256VR-SS,SAM-CAP,M59,MBP15	EEE_WTG,M59_COMMON,CPU_2_33GHZ,VRAM_SAM256,CAP22UF_ALLSAM,ODD_NONLOCK_CONN
630-7920	PCBA,2.33,256VR-SS,MUR-CAP,M59,MBP15	EEE_X35,M59_COMMON,CPU_2_33GHZ,VRAM_SAM256,CAP22UF_ALLMURA,ODD_NONLOCK_CONN

Mixed Cap BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7964	PCBA,2.16,128VR-SS,SAM_TYO-CAP,M59,MBP15	EEE_XAC,M59_COMMON,CPU_2_16GHZ,VRAM_SAM128,CAP22UF_MIXSAM,ODD_NONLOCK_CONN
630-7965	PCBA,2.16,128VR-SS,MUR_TYO-CAP,M59,MBP15	EEE_XAD,M59_COMMON,CPU_2_16GHZ,VRAM_SAM128,CAP22UF_MIXMURA,ODD_NONLOCK_CONN
630-7966	PCBA,2.33,256VR-SS,SAM_TYO-CAP,M59,MBP15	EEE_XAE,M59_COMMON,CPU_2_33GHZ,VRAM_SAM256,CAP22UF_MIXSAM,ODD_NONLOCK_CONN
630-7967	PCBA,2.33,256VR-SS,MUR_TYO-CAP,M59,MBP15	EEE_XAF,M59_COMMON,CPU_2_33GHZ,VRAM_SAM256,CAP22UF_MIXMURA,ODD_NONLOCK_CONN

Qimonda (Infineon) VRAM BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7982	PCBA,2.16,128VR-QM,SS-CAP,M59,MBP15	EEE_XBU,M59_COMMON,CPU_2_16GHZ,VRAM_INF128,CAP22UF_ALLSAM,ODD_NONLOCK_CONN
630-7983	PCBA,2.16,128VR-QM,MU-CAP,M59,MBP15	EEE_XBV,M59_COMMON,CPU_2_16GHZ,VRAM_INF128,CAP22UF_ALLMURA,ODD_NONLOCK_CONN
630-7984	PCBA,2.33,256VR-QM,SS-CAP,M59,MBP15	EEE_XBW,M59_COMMON,CPU_2_33GHZ,VRAM_INF256,CAP22UF_ALLSAM,ODD_NONLOCK_CONN
630-7985	PCBA,2.33,256VR-QM,MU-CAP,M59,MBP15	EEE_XBX,M59_COMMON,CPU_2_33GHZ,VRAM_INF256,CAP22UF_ALLMURA,ODD_NONLOCK_CONN
630-7986	PCBA,2.16,128VR-QM,SS_TY-CAP,M59,MBP15	EEE_XBY,M59_COMMON,CPU_2_16GHZ,VRAM_INF128,CAP22UF_MIXSAM,ODD_NONLOCK_CONN
630-7987	PCBA,2.16,128VR-QM,MU_TY-CAP,M59,MBP15	EEE_XBZ,M59_COMMON,CPU_2_16GHZ,VRAM_INF128,CAP22UF_MIXMURA,ODD_NONLOCK_CONN
630-7988	PCBA,2.33,256VR-QM,SS_TY-CAP,M59,MBP15	EEE_XC0,M59_COMMON,CPU_2_33GHZ,VRAM_INF256,CAP22UF_MIXSAM,ODD_NONLOCK_CONN
630-7989	PCBA,2.33,256VR-QM,MU_TY-CAP,M59,MBP15	EEE_XC1,M59_COMMON,CPU_2_33GHZ,VRAM_INF256,CAP22UF_MIXMURA,ODD_NONLOCK_CONN

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:WTE]	CRITICAL	EEE_WTE
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:WTG]	CRITICAL	EEE_WTG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:X34]	CRITICAL	EEE_X34
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:X35]	CRITICAL	EEE_X35
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XAC]	CRITICAL	EEE_XAC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XAD]	CRITICAL	EEE_XAD
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XAE]	CRITICAL	EEE_XAE
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XAF]	CRITICAL	EEE_XAF
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XBU]	CRITICAL	EEE_XBU
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XBV]	CRITICAL	EEE_XBV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XBW]	CRITICAL	EEE_XBW
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XBX]	CRITICAL	EEE_XBX
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XBY]	CRITICAL	EEE_XBY
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XBZ]	CRITICAL	EEE_XBZ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XC0]	CRITICAL	EEE_XC0
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XC1]	CRITICAL	EEE_XC1

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M59_COMMON	ALTERNATE,COMMON,M59_COMMON1,M59_COMMON2,M59_COMMON3
M59_COMMON1	BOOTROM_FINAL,ENET_LOWPWR_EN,ENETPWR_S3AC,GPU_BB_CTL,D3CPGOOD_3V3
M59_COMMON2	ITP,KBDLED_HAS,LPCPLUS,LVDS_PD,MEMVREF_S3
M59_COMMON3	MEMVTT_EN_PU,RTUSB_ESD,SMC_PRGRM,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
VRAM_INF128	GPU_MEM_NOT_SAM,VRAM_128_INFINEON
VRAM_SAM128	VRAM_128_SAMSUNG
VRAM_INF256	GPU_MEM_256M,GPU_MEM_NOT_SAM,VRAM_256_INFINEON
VRAM_SAM256	GPU_MEM_256M,VRAM_256_SAMSUNG
M59_TPM	TPM
CAP22UF_ALLSAM	CAP22UF_SAM,CAP22UF_SAM_CRIT
CAP22UF_ALLMURA	CAP22UF_MURA,CAP22UF_MURA_CRIT
CAP22UF_MIXSAM	CAP22UF_TAIYO,CAP22UF_SAM_CRIT
CAP22UF_MIXMURA	CAP22UF_TAIYO,CAP22UF_MURA_CRIT

extra TPM options:
SMC_TPM_GPIO2 SMC_TPM_GPIO1 SMC_TPM_PP

see page 85 (csa page 105)
for option definitions

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX
333S0376	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_INFINEON
333S0377	4	IC,SGRAM,GDDR3,16MX32,600MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_INFINEON
337S3391	1	IC,MDC,B2,PRQ,2.16G,34W,667M,4M,479BGA	U0700	CRITICAL	CPU_2_16GHZ
337S3393	1	IC,MDC,B2,PRQ,2.33G,34W,667M,4M,479BGA	U0700	CRITICAL	CPU_2_33GHZ
341S1922	1	IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M59	U6301	CRITICAL	BOOTROM_DEVEL
341S2006	1	IC,EFI,BOOTROM FINAL (LOCKED),M59	U6301	CRITICAL	BOOTROM_FINAL
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1929	1	IC,PRGRM,SMC (NEW),M59	U5800	CRITICAL	SMC_PRGRM
338S0269	1	IC,945GM,NORTHBRIDGE	U1200	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0368	1	IC,ATI,M56L-LLP,GRPHXCRTL,LF 880BGA	U8400	CRITICAL	
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	TPM
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
343S0385	1	IC,ICH7M,BGA	U2100	CRITICAL	
353S1461	1	IC,ISL9504,SYNC REG CTRL,QFN48	U7530	CRITICAL	
359S0109	1	LOW POWER CLOCK SYNTHESIZER, 68PIN	U3301	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060		ALL	330uF,2V,9MOHM,D2
128S0095	128S0060		ALL	330uF,2V,6MOHM,D2
128S0081	128S0061		ALL	150uF,6.3V,25MOHM,C2
376S0448	376S0445		ALL	517806ADN for FDM6296
353S1465	353S1461		ALL	Screened ISL6262 for ISL9504
152S0287	152S0435		ALL	Alternates for Coilcraft MSS5131
128S0093	128S0092		ALL	33uF,16V,D2
157S0030	157S0011		ALL	TDK Ethernet XFMR for E&E
353S1381	353S1278		ALL	ISL60002 for REF3133 SMC AVREF Supply

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE	SHT	OF
NONE	4	105

Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	59C7
TRUE		IMVP6_COMP	59B7
TRUE		P5VS5_RUNSS	60C5 64A6
TRUE		P1V5S0_RUNSS	5B7 60C4 64C6
TRUE		P1V2S3_RT	61B6
TRUE		P1V2S3_RUNSS	41C4 61B7
TRUE		P3V3S5_COMP	5B7 63C6
TRUE		P3V3S5_FSET	5B7 63D6
TRUE		P1V05S0_COMP	5C7 63A7
TRUE		P1V05S0_FSET	5B7 63B7
TRUE		P3V42G3H_FB	64C3
TRUE		GPUVCORE_COMP	68C7
TRUE		GPUVCORE_FSET	68C7
TRUE		GPUBBP_ADJ	68B7
TRUE		GPUBBN_FB	68A3
TRUE		GPUVCORE_FB	68C7
TRUE		GPUVCORE_FB_RC	68C3
TRUE		GPUVCORE_ISEN	68C5
TRUE		GPUVCORE_LG	68C5
TRUE		GPUVCORE_PHASE	68C5
TRUE		GPUVCORE_UG	68D5
TRUE		IMVP6_COMP_RC	59B8
TRUE		IMVP6_DFB	59B6
TRUE		IMVP6_FB	59B7
TRUE		IMVP6_OCSET	59C6
TRUE		IMVP6_VDIFF	59C7
TRUE		IMVP6_VDIFF_RC	59B8
TRUE		P1V05S0_BOOT	63B5
TRUE		P1V05S0_BOOT_R	63B5
TRUE		P1V05S0_COMP	5D7 63A7
TRUE		P1V05S0_COMP_R	63A7
TRUE		P1V05S0_FB	63A7
TRUE		P1V05S0_FB_RC	63A3
TRUE		P1V05S0_FSET	5D7 63B7
TRUE		P1V05S0_ISEN	63A5
TRUE		P1V05S0_LG	63A5
TRUE		P1V05S0_PHASE	63B5
TRUE		P1V05S0_UG	63B5
TRUE		P1V5S0_RUNSS	5D7 60C4 64C6
TRUE		P3V3S5_BOOT	63D4
TRUE		P3V3S5_BOOT_R	63D4
TRUE		P3V3S5_COMP	5D7 63C6
TRUE		P3V3S5_COMP_R	63C6
TRUE		P3V3S5_FB	63C6
TRUE		P3V3S5_FB_RC	63C2
TRUE		P3V3S5_FSET	5D7 63D6
TRUE		P3V3S5_ISEN	63C4
TRUE		P3V3S5_LG	63C4
TRUE		P3V3S5_UG	63D4
TRUE		CK410_XTAL_IN	33C6

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7C8 7D8 12C4 12D4 84D6
TRUE		FSB_ADS_L	7D6 12C4 84D6
TRUE	TRUE	FSB_ADSTB_L<1..0>	7C8 7D8 12C4 84C6
TRUE		FSB_BNR_L	7D6 12C4 84D6
TRUE		FSB_BREQ0_L	7D6 12C4 84D6
TRUE		FSB_D_L<63..0>	7B3 7B4 7C3 7C4 12B6 12C6 12D6 84D6
TRUE		FSB_DBSY_L	7D6 12B4 84D6
TRUE	TRUE	FSB_DINV_L<3..0>	7B3 7B4 7C3 7C4 12B4 84D6
TRUE		FSB_DRDY_L	7D6 12B4 84D6
TRUE	TRUE	FSB_DSTBN_L<3..0>	7B3 7B4 7C3 7C4 12B4 84D6
TRUE	TRUE	FSB_DSTBP_L<3..0>	7B3 7B4 7C3 7C4 12B4 84D6
TRUE		FSB_HIT_L	7D6 12B4 84D6
TRUE		FSB_HITM_L	7D6 12B4 84D6
TRUE		FSB_LOCK_L	7D6 12B4 84D6
TRUE		FSB_REQ_L<4..0>	7D8 12A4 12B4 84D6

Fan Connectors

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	56C7 65A1
TRUE	FAN_LT_PWM	56B6
TRUE	FAN_LT_TACH	56B6
TRUE	FAN_RT_PWM	56B3
TRUE	FAN_RT_TACH	56B3

LPC+ Debug Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	51C4 65D3
TRUE	=PP5V_S0_LPCPLUS	51C4 65A1
TRUE	LPC_AD<0>	21D4 49D7 51C4 58C6
TRUE	LPC_AD<1>	21D4 49D7 51C4 58C6
TRUE	LPC_FRAME_L	21C5 49C7 51C4 58C6
TRUE	PM_CLKRUN_L	23C8 49C5 51C4 58C6
TRUE	BOOT_LPC_SPI_L	22B3 49C7 51B4
TRUE	SMC_TMS	49B5 50B2 51B4
TRUE	DEBUG_RST_L	26B1 51B4
TRUE	SMC_TRST_L	49C1 51B4
TRUE	SMC_TDO	49B5 50B2 51B4
TRUE	SMC_MD1	49C1 51B4
TRUE	SMC_TX_L	46B5 49C7 50B2 50B3 51B4
TRUE	FWH_INIT_L	21C4 50D3 51C5
TRUE	PCI_CLK_PORT80_LPC	34D6 51C5
TRUE	LPC_AD<2>	21D4 49C7 51C5 58C6
TRUE	LPC_AD<3>	21D4 49C7 51C5 58C6
TRUE	INT_SERIRQ	23C8 49C7 51C5 58C6
TRUE	PM_SUS_STAT_L	23C5 49C5 50A2 51B5 58C6
TRUE	SMC_TDI	49B5 50B2 51B5
TRUE	SMC_TCK	49C5 50B2 51B5
TRUE	SMC_RST_L	49C3 50D6 51B5
TRUE	SMC_NMI	49C1 51B5
TRUE	SMC_RX_L	46B5 49C7 50B2 50B3 51B5
TRUE	SV_SET_UP	23B6 23C3 51B5

Left ALS Connector

FUNC_TEST

TRUE	=PP3V3_S3_LTALS	65C3 78C5
TRUE	ALS_GAIN	6D5 49B5 78C6
TRUE	LTALS_OUT	55C7 78C6
TRUE	GND	

Thermal Diode Connectors

FUNC_TEST

TRUE	HSTHMSNS_DX_P	52C5
TRUE	HSTHMSNS_DX_N	52C5
TRUE	RSFSTHMSNS_D_P	52D5
TRUE	RSFSTHMSNS_D_N	52C5

Other Func Test Points

FUNC_TEST

TRUE	=PP1V05_S0_REG	53A4 63A2 65D8
TRUE	PM_SYSRST_L	23C5 26C5 49B7
TRUE	SMC_ONOFF_L	49C5 50B2 50C6 78C2

Current Sense Calibration

FUNC_TEST

TRUE	ISENSE_CAL_EN	49B7 53A8
TRUE	=PP5V_S0_ISENSECAL	53A8 65A1
TRUE	=PP1V8_S3_REG	62C1 65B8
TRUE	=PP1V5_S0_REG	60C1 65C8
TRUE	PPVCORE_S0_GPU	
TRUE	PPVCORE_S0_CPU	65D1
TRUE	GND	

2 TPs per

8 TPs, 2 with each of above TP pairs

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	49C5 50B2 66B5
TRUE	=SMBUS_BATT_SCL	27C1 66B5
TRUE	=SMBUS_BATT_SDA	27C1 66B5
TRUE	GND_BATT	66B5

Left I/O Data Connector

FUNC_TEST

TRUE	=PP1V5_S0_LIO	47D6 65C6
TRUE	=PPDCIN_G3H_LIO	47C6 65A8
TRUE	=PP5V_S5_LIO	47C6 65B1
TRUE	=PP3V42_G3H_LIO	47D6 65D3
TRUE	PP5V_S0_AUDIO_PWR	47D4
TRUE	PP5V_S0_AUDIO	47C4
TRUE	GND_AUDIO_PWR	47A4
TRUE	GND_AUDIO	47A4
TRUE	ACZ_SDATAIN<0>	21C7 47B6 84B4
TRUE	ACZ_SDATAOUT	21C7 47B6 84B4
TRUE	ACZ_BITCLK	21C7 47B6 84B4
TRUE	ACZ_RST_L	21C7 47B3 84B4
TRUE	EXCARD_OC_L	6C3 47C6 50B3
TRUE	LTUSB_OC_L	6D3 47C6
TRUE	LIO_BATT_ISENSE	47C6 53C3
TRUE	SMC_SYS_ISET	47C6 49B5
TRUE	SMC_BATT_ISET	47B6 49B5
TRUE	SMC_BATT_CHG_EN	47C6 49D7 50A2
TRUE	SMC_BC_ACOK	47B6 49C5 50A2
TRUE	SMC_ADAPTER_EN	43B7 47C6 49D5 50A2
TRUE	LIO_P3V3S0_EN_L	47B6 64C6
TRUE	LIO_DCIN_ISENSE	47B6 53C5
TRUE	LIO_P3V3S3_EN	47B6 64A6
TRUE	SMC_BATT_TRICKLE_EN_L	47B6 49D7 50A2
TRUE	SYS_ONEWIRE	47C6 49B7 50B2
TRUE	MINI_CLKREQ_L	34A3 47C6
TRUE	SMC_EXCARD_CP	47B6 49B7 50A2
TRUE	EXCARD_CLKREQ_L	34A3 47C6
TRUE	SMC_EXCARD_PWR_EN	47B6 49B7
TRUE	LIO_PLT_RESET_L	26C1 47C6
TRUE	ACZ_SYNC	21C7 47B6 84B4
TRUE	=USB2_LT_N	6D3 47C3
TRUE	=USB2_LT_P	6D3 47C3
TRUE	=USB2_EXCARD_N	6C3 47C3
TRUE	=USB2_EXCARD_P	6C3 47C3
TRUE	=PCIE_EXCARD_R2D_N	47B3 48C6
TRUE	=PCIE_EXCARD_R2D_P	47B3 48C6
TRUE	=PCIE_EXCARD_D2R_N	47B3 48B6
TRUE	=PCIE_EXCARD_D2R_P	47B3 48C6
TRUE	PCIE_CLK100M_EXCARD_P	34C3 47B3
TRUE	PCIE_CLK100M_EXCARD_N	34B3 47B3
TRUE	=PCIE_MINI_R2D_N	47B3 48C6
TRUE	=PCIE_MINI_R2D_P	47B3 48C6
TRUE	=PCIE_MINI_D2R_N	47C3 48C6
TRUE	=PCIE_MINI_D2R_P	47C3 48C6
TRUE	PCIE_CLK100M_MINI_P	34D4 47C3
TRUE	PCIE_CLK100M_MINI_N	34D4 47C3
TRUE	=SMBUS_LIO_SMC_SCL	27D1 47C3
TRUE	=SMBUS_LIO_SMC_SDA	27D1 47C3
TRUE	=SMBUS_LIO_SB_SCL	27B6 47C3
TRUE	=SMBUS_LIO_SB_SDA	27B6 47C3
TRUE	PCIE_WAKE_L	23C8 39C6 47C3

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUS_G3H_LIO_CONN	65C3 66C4
TRUE	GND	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14B4 22D2
TRUE	DMI_N2S_N<1..0>	14B4 22D2
TRUE	SB_CLK100M_SATA_P	21B6 34C3
TRUE	SB_CLK100M_SATA_N	21B6 34C3

Camera Connector

FUNC_TEST

TRUE	=PP5V_S3_CAMERA	45C3 65B1
	=USB2_CAMERA_N	6C3 45C3
	=USB2_CAMERA_P	6D3 45B3

Inverter Connector

FUNC_TEST

TRUE	GND_CHASSIS_INVERTER	6A8
TRUE	PPBUS_S0_INVERTER	76B5
TRUE	GND_INVERTER	76A5
TRUE	INVERTER_PWM	76A5
TRUE	PP5V_INVERTER_SW	76B5

RTC Battery Connector

FUNC_TEST

TRUE	PPVBATT_G3C_RTC	26D6
TRUE	GND	

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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SCALE NONE | SHT 5 OF 105

NC_CPU_A32_L = TP_CPU_A32_L 7C8
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_A33_L = TP_CPU_A33_L 7B8
NC_CPU_A34_L = TP_CPU_A34_L 7B8
NC_CPU_A35_L = TP_CPU_A35_L 7B8
NC_CPU_A36_L = TP_CPU_A36_L 7B8
NC_CPU_A37_L = TP_CPU_A37_L 7B8
NC_CPU_A38_L = TP_CPU_A38_L 7B8
NC_CPU_A39_L = TP_CPU_A39_L 7B8
NC_CPU_APM0_L = TP_CPU_APM0_L 7B8
NC_CPU_APM1_L = TP_CPU_APM1_L 7B8
NC_CPU_EXTBREF = TP_CPU_EXTBREF 7B6
NC_CPU_HFPLL = TP_CPU_HFPLL 7B8
NC_CPU_SPARE0 = TP_CPU_SPARE0 7B6
NC_CPU_SPARE1 = TP_CPU_SPARE1 7B6
NC_CPU_SPARE2 = TP_CPU_SPARE2 7B6
NC_CPU_SPARE4 = TP_CPU_SPARE4 7B6

NC_MEM_A_A<15..14> = MEM_A_A<15..14> 28C3
NC_MEM_B_A<15..14> = MEM_B_A<15..14> 29C3
TP_NB_CFG<4..3> = NB_CFG<4..3> 14C6
TP_NB_CFG<6> = NB_CFG<6> 14C6
TP_NB_CFG<8> = NB_CFG<8> 14C6
TP_NB_CFG<11..10> = NB_CFG<11..10> 14C6
TP_NB_CFG<15..14> = NB_CFG<15..14> 14C6
TP_NB_CFG<17> = NB_CFG<17> 14C6
MAKE_BASE=TRUE

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> = NB_CFG<13..12> 14C6

TP_SB_SUS_CLK = SUS_CLK_SB 23C3

NC_SB_XOR_T5 = TP_SB_XOR_T5 21C6
NC_SB_XOR_U5 = TP_SB_XOR_U5 21C6
NC_SB_XOR_V3 = TP_SB_XOR_V3 21C6
NC_SB_XOR_V4 = TP_SB_XOR_V4 21C6
NC_SB_XOR_W3 = TP_SB_XOR_W3 21C6

FireWire Aliases

42C4 =PP3V3_FWPHY_REG — PP3V3_FWPHY
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
MAKE_BASE=TRUE
→ =PP3V3_FWPHY 38D7 44B8
→ =PP3V3_FWPHY_CORE 42C4
→ =PP3V3_FWLATEVG 44A8
→ =PP3V3_FWLATEVG_ACTIVE 43A7

42C1 =PP1V95_FWPHY_CORE_LDO — PP1V95_FWPHY
VOLTAGE=1.95V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
MAKE_BASE=TRUE
→ =PP1V95_FWPHY 38D5
→ =PP1V8_FWPHY_OSC 38B2

49D7 6D4 SMC_RSTGATE_L — =SMC_FWRSTGATE_L 37A8
MAKE_BASE=TRUE

37C6 22A7 PCI_AD<19> — =FW_PCI_IDSEL 37B7
MAKE_BASE=TRUE

22B6 PCI_GNT3_L — =FW_PCI_GNT_L 37D3
MAKE_BASE=TRUE

26D2 22B6 PCI_REQ3_L — =FW_PCI_REQ_L 37D3
MAKE_BASE=TRUE

Chassis GNDs

GND_CHASSIS_RTUSB
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
→ =GND_CHASSIS_RTUSB 46B2
→ =GND_CHASSIS_FW_PORT2L 44A1
→ =GND_CHASSIS_FW_EMI_R 44A3

GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
C0600 1 0.01UF 10% 50V X7R 402 2
→ =GND_CHASSIS_DVI2 77A5
→ =GND_CHASSIS_DVI4 77A3

GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
1 R0601 0 5% 1/16W MF-LF 402 2
→ =GND_CHASSIS_DVI1 77B5
→ =GND_CHASSIS_DVI3 77A2
→ =GND_CHASSIS_DVI5 77A2

GND_CHASSIS_ENET
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
→ =GND_CHASSIS_ENET 40B2
→ =GND_CHASSIS_FW_PORT1 44C1
→ =GND_CHASSIS_FW_PORT2U 44A1

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602 HOLE-VIA-P5RP25 1
C0602 1 0.01UF 10% 50V X7R 402 2

GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
→ =GND_CHASSIS_LCD1 76D2
→ =GND_CHASSIS_LCD2 76D3
→ =GND_CHASSIS_LCD3 76C3
→ =GND_CHASSIS_LCD4 76B2

SH0600 OG-503040 SMLD-SM-LF
1 2 3
5A6 GND_CHASSIS_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
→ =GND_CHASSIS_INVERTER 76A6
→ =GND_CHASSIS_CAMERA 45B5 45C5

TP_SMC_RSTGATE_L = SMC_RSTGATE_L 6B7 49D7
MAKE_BASE=TRUE

78C6 49B5 5B2 ALS_GAIN = =RTALS_GAIN 55C4
MAKE_BASE=TRUE

NC_ENET_CTRL12 = ENET_CTRL12 39C8
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_ENET_CTRL25 = ENET_CTRL25 39C8
MAKE_BASE=TRUE
NO_TEST=TRUE

Ethernet Power Management Support

ENET_LOWPWR_EN
R0600 0 5% 1/16W MF-LF 402
22D8 22C4 SB_GPIO30 — 1 — 2 — 39B8 ENET_LOWPWR_EN
EN — OUT

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOWPWR_EN" are mutually-exclusive.

Inverter PWM Reset Alias

26C1 MS9_INVERTER_PLT_RST_L = =INVERTER_PWM_PLT_RST_L 76A8

Thermal Module Holes

Add 2 blind vias per hole per side to GND

Top CPU TM Hole
Top GPU Right TM Hole
Left CPU TM Hole
Right CPU TM Hole
Bottom Left GPU TM Hole

RAM door (Torx) holes

ZT0630 HOLE-VIA-P5RP25 1 GND_CHASSIS_RAMDOOR_HOLE_0
C0630 1 0.01UF 10% 50V X7R 402 2

ZT0631 HOLE-VIA-P5RP25 1 GND_CHASSIS_RAMDOOR_HOLE_1
C0631 1 0.01UF 10% 50V X7R 402 2

Frame holes

ZT0615 HOLE-VIA-P5RP25 1 GND_CHASSIS_RIGHT_FAN_HOLE
ZT0614 HOLE-VIA-P5RP25 1 GND_CHASSIS_RIGHT_FAN_NOTCH
ZT0613 HOLE-VIA-P5RP25 1 GND_CHASSIS_DIMM_NOTCH
ZT0612 HOLE-VIA-P5RP25 1 GND_CHASSIS_LIOFLEX_HOLE
ZT0611 HOLE-VIA-P5RP25 1 GND_CHASSIS_BATTCONN_HOLE
ZT0610 HOLE-VIA-P5RP25 1 GND_CHASSIS_LNDACARD_HOLE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

C0610 1 0.01UF 10% 50V X7R 402 2
C0611 1 0.01UF 10% 50V X7R 402 2
C0612 1 0.01UF 10% 50V X7R 402 2
C0613 1 0.01UF 10% 50V X7R 402 2
C0614 1 0.01UF 10% 50V X7R 402 2
C0615 1 0.01UF 10% 50V X7R 402 2

USB Port "A" (Debug Port) = Right USB 2.0 Port

46B5 =USB2_RT_P — USB2_RT_P — USB_A_P 22C2
46B5 =USB2_RT_N — USB2_RT_N — USB_A_N 22C2
46C5 =RTUSB_OC_L — RTUSB_OC_L — USB_A_OC_L 22C4 22D8
MAKE_BASE=TRUE

USB Port "B" = Trackpad (Geyser)

78C3 =USB_TRACKPAD_P — USB_TRACKPAD_P — USB_B_P 22C2
78C3 =USB_TRACKPAD_N — USB_TRACKPAD_N — USB_B_N 22C2
UNUSED_USB_B_OC_L — USB_B_OC_L 22C4 22D8
MAKE_BASE=TRUE

USB Port "C" = Left USB 2.0 Port

47C3 5B1 =USB2_LT_P — USB2_LT_P — USB_C_P 22C2
47C3 5B1 =USB2_LT_N — USB2_LT_N — USB_C_N 22C2
47C6 5C1 LTUSB_OC_L — USB_C_OC_L 22C4 22D8
MAKE_BASE=TRUE

USB Port "D" = Camera

45B3 5A4 =USB2_CAMERA_P — USB2_CAMERA_P — USB_D_P 22C2
45C3 5A4 =USB2_CAMERA_N — USB2_CAMERA_N — USB_D_N 22C2
UNUSED_USB_D_OC_L — USB_D_OC_L 22C4 22D8
MAKE_BASE=TRUE

USB Port "E" = ExpressCard

47C3 5B1 =USB2_EXCARD_P — USB2_EXCARD_P — USB_E_P 22C2
47C3 5B1 =USB2_EXCARD_N — USB2_EXCARD_N — USB_E_N 22C2
50B3 47C6 5C1 EXCARD_OC_L — USB_E_OC_L 22C4 22D8
MAKE_BASE=TRUE

USB Port "F" = IR Receiver

78B4 =USB_IR_P — USB_IR_P — USB_F_P 22C2
78B4 =USB_IR_N — USB_IR_N — USB_F_N 22C2
MAKE_BASE=TRUE

USB Port "G" = Bluetooth (M13L)

78C2 =USB_BT_P — USB_BT_P — USB_G_P 22C2
78C2 =USB_BT_N — USB_BT_N — USB_G_N 22C2
MAKE_BASE=TRUE

USB Port "H" = Reserved

22C2 6C1 TP_USB_H_P — TP_USB_H_P 6C2 22C2
22C2 6C1 TP_USB_H_N — TP_USB_H_N 6C2 22C2
MAKE_BASE=TRUE

LVDS pulldown aliases

79B8 =LVDS_PD_U_CLK_N — LVDS_U_CLK_CONN_N 76B2 76D7 79C1
79B8 =LVDS_PD_U_CLK_P — LVDS_U_CLK_CONN_P 76B2 76D7 79C1
79C8 =LVDS_PD_U_DATA_P<0> — LVDS_U_DATA_CONN_P<0> 76C2 76D7 79D1
79C8 =LVDS_PD_U_DATA_N<0> — LVDS_U_DATA_CONN_N<0> 76C2 76D7 79D1
79B8 =LVDS_PD_U_DATA_P<1> — LVDS_U_DATA_CONN_P<1> 76C2 76D7 79C1
79B8 =LVDS_PD_U_DATA_N<1> — LVDS_U_DATA_CONN_N<1> 76C2 76D7 79C1
79B8 =LVDS_PD_U_DATA_P<2> — LVDS_U_DATA_CONN_P<2> 76B2 76D7 79C1
79B8 =LVDS_PD_U_DATA_N<2> — LVDS_U_DATA_CONN_N<2> 76C2 76D7 79D1
79C8 =LVDS_PD_L_CLK_N — LVDS_L_CLK_CONN_N 76C2 76D7 79C1
79C8 =LVDS_PD_L_CLK_P — LVDS_L_CLK_CONN_P 76C2 76D7 79C1
79D8 =LVDS_PD_L_DATA_P<0> — LVDS_L_DATA_CONN_P<0> 76C2 76D7 79C1
79D8 =LVDS_PD_L_DATA_N<0> — LVDS_L_DATA_CONN_N<0> 76C2 76D7 79C1
79D8 =LVDS_PD_L_DATA_P<1> — LVDS_L_DATA_CONN_P<1> 76C2 76D7 79C1
79C8 =LVDS_PD_L_DATA_N<1> — LVDS_L_DATA_CONN_N<1> 76C2 76D7 79C1
79C8 =LVDS_PD_L_DATA_P<2> — LVDS_L_DATA_CONN_P<2> 76C2 76D7 79C1
79C8 =LVDS_PD_L_DATA_N<2> — LVDS_L_DATA_CONN_N<2> 76C2 76D7 79C1
MAKE_BASE=TRUE

Signal Aliases/Misc Comps

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-7270 | REV. B
SCALE NONE | SHT 6 OF 105

OMIT

U0700
YONAH-BST1
CPU
BGA
(1 OF 4)

ADDR GROUP0
FSB_A_L<3>
FSB_A_L<4>
FSB_A_L<5>
FSB_A_L<6>
FSB_A_L<7>
FSB_A_L<8>
FSB_A_L<9>
FSB_A_L<10>
FSB_A_L<11>
FSB_A_L<12>
FSB_A_L<13>
FSB_A_L<14>
FSB_A_L<15>
FSB_A_L<16>
FSB_ADSTB_L<0>
FSB_REQ_L<0>
FSB_REQ_L<1>
FSB_REQ_L<2>
FSB_REQ_L<3>
FSB_REQ_L<4>

ADDR GROUP1
FSB_A_L<17>
FSB_A_L<18>
FSB_A_L<19>
FSB_A_L<20>
FSB_A_L<21>
FSB_A_L<22>
FSB_A_L<23>
FSB_A_L<24>
FSB_A_L<25>
FSB_A_L<26>
FSB_A_L<27>
FSB_A_L<28>
FSB_A_L<29>
FSB_A_L<30>
FSB_A_L<31>
FSB_ADSTB_L<1>

CONTROL
FSB_ADS_L
FSB_BNR_L
FSB_BPRI_L
FSB_DEFER_L
FSB_DRDY_L
FSB_DBSY_L
FSB_BREQ0_L
FSB_IERR_L
CPU_INIT_L
FSB_LOCK_L
FSB_CPURST_L
FSB_RS_L<0>
FSB_RS_L<1>
FSB_RS_L<2>
FSB_TRDY_L
FSB_HIT_L
FSB_HITM_L

XDP/ITP SIGNALS
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST_L
XDP_DBRESET_L

THERM
CPU_PROCHOT_L
CPU_THERMD_P
CPU_THERMD_N
PM_THRMTRIP_L

HCLK
FSB_CLK_CPU_P
FSB_CLK_CPU_N

RESERVED
TP_CPU_A32_L
TP_CPU_A33_L
TP_CPU_A34_L
TP_CPU_A35_L
TP_CPU_A36_L
TP_CPU_A37_L
TP_CPU_A38_L
TP_CPU_A39_L
TP_CPU_APM0_L
TP_CPU_APM1_L
TP_CPU_HFPLL
TP_CPU_EXTBREF
TP_CPU_SPARE0
TP_CPU_SPARE1
TP_CPU_SPARE2
TP_CPU_SPARE3
TP_CPU_SPARE4
TP_CPU_SPARE5
TP_CPU_SPARE6
TP_CPU_SPARE7

CPU_A20M_L
CPU_FERR_L
CPU_IGNNE_L
CPU_STPCLK_L
CPU_INTR
CPU_NMI
CPU_SMI_L

=PP1V05_S0_CPU 7B5 7B6 7D5 8C7 9B7 11B3 11C5 65D6

R0702 54.9 1% 1/16W MF-LF 402
R0703 54.9 1% 1/16W MF-LF 402
R0704 68 5% 1/16W MF-LF 402

PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY

CPU_PROCHOT_L TO SMC AND CPU VR TO INFORM CPU IS HOT

PM_THRMTRIP# SHOULD CONNECT TO ICH7-M AND GMCH WITHOUT T-ING (NO STUB)

SPARE[7-0],HFPLL: ROUTE TO TP VIA AND PLACE GND VIA W/IN 1000 MILS

OMIT

U0700
YONAH-BST1
CPU
BGA
(2 OF 4)

DATA GRP0
FSB_D_L<0>
FSB_D_L<1>
FSB_D_L<2>
FSB_D_L<3>
FSB_D_L<4>
FSB_D_L<5>
FSB_D_L<6>
FSB_D_L<7>
FSB_D_L<8>
FSB_D_L<9>
FSB_D_L<10>
FSB_D_L<11>
FSB_D_L<12>
FSB_D_L<13>
FSB_D_L<14>
FSB_D_L<15>
FSB_DSTBN_L<0>
FSB_DSTBP_L<0>
FSB_DINV_L<0>

DATA GRP1
FSB_D_L<16>
FSB_D_L<17>
FSB_D_L<18>
FSB_D_L<19>
FSB_D_L<20>
FSB_D_L<21>
FSB_D_L<22>
FSB_D_L<23>
FSB_D_L<24>
FSB_D_L<25>
FSB_D_L<26>
FSB_D_L<27>
FSB_D_L<28>
FSB_D_L<29>
FSB_D_L<30>
FSB_D_L<31>
FSB_DSTBN_L<1>
FSB_DSTBP_L<1>
FSB_DINV_L<1>

DATA GRP2
FSB_D_L<32>
FSB_D_L<33>
FSB_D_L<34>
FSB_D_L<35>
FSB_D_L<36>
FSB_D_L<37>
FSB_D_L<38>
FSB_D_L<39>
FSB_D_L<40>
FSB_D_L<41>
FSB_D_L<42>
FSB_D_L<43>
FSB_D_L<44>
FSB_D_L<45>
FSB_D_L<46>
FSB_D_L<47>
FSB_DSTBN_L<2>
FSB_DSTBP_L<2>
FSB_DINV_L<2>

DATA GRP3
FSB_D_L<48>
FSB_D_L<49>
FSB_D_L<50>
FSB_D_L<51>
FSB_D_L<52>
FSB_D_L<53>
FSB_D_L<54>
FSB_D_L<55>
FSB_D_L<56>
FSB_D_L<57>
FSB_D_L<58>
FSB_D_L<59>
FSB_D_L<60>
FSB_D_L<61>
FSB_D_L<62>
FSB_D_L<63>
FSB_DSTBN_L<3>
FSB_DSTBP_L<3>
FSB_DINV_L<3>

MISC
CPU_COMP<0>
CPU_COMP<1>
CPU_COMP<2>
CPU_COMP<3>
CPU_DPRSTP_L
CPU_DPSLP_L
FSB_DPWR_L
CPU_PWRGOOD
FSB_SLPCPU_L
CPU_PSI_L

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".

R0716 27.4 1% 1/16W MF-LF 402
R0717 54.9 1% 1/16W MF-LF 402
R0718 27.4 1% 1/16W MF-LF 402
R0719 54.9 1% 1/16W MF-LF 402

=PP1V05_S0_CPU 65D6 11C5 11B3 9B7 8C7 7D5 7B6

R0705 1K 1% 1/16W MF-LF 402
CPU_GTLREF
R0706 2.0K 1% 1/16W MF-LF 402

LAYOUT NOTE: 0.5" MAX LENGTH
CPU_TEST1
CPU_TEST2

CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>

NOSTUFF R0730 0 402
R0712 51 5% 1/16W MF-LF 402
NOSTUFF R0707 1K 5% 1/16W MF-LF 402

=PP1V05_S0_CPU 7B5 7D5 8C7 9B7 11B3 11C5 65D6

R0720 54.9 1% 402 XDP_TMS
R0721 54.9 1% 402 XDP_TDI
R0722 54.9 1% 402 XDP_TCK

CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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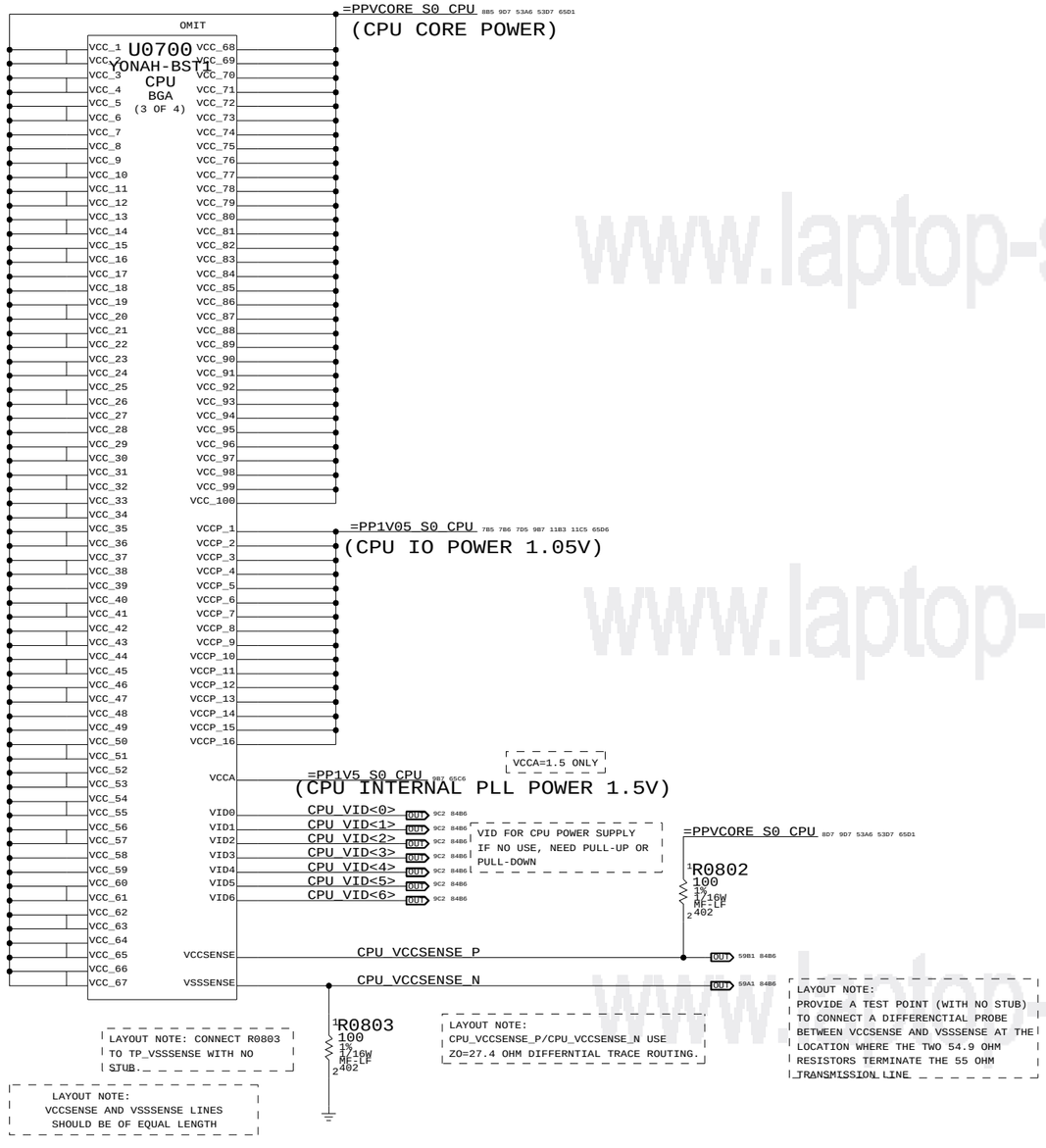
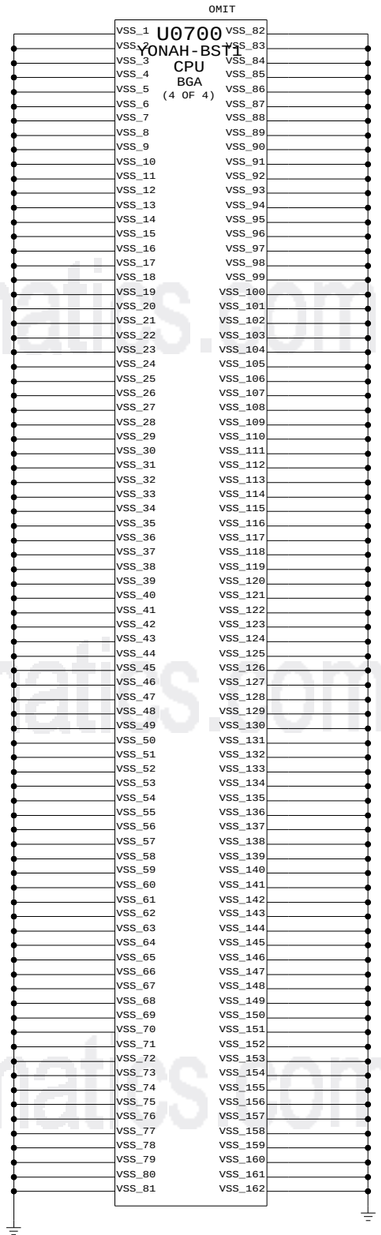
SCALE: NONE	SHT 7 OF 105	





CPU 2 OF 2-PWR/GND

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 8 OF 105	

CPU VCORE HF AND BULK DECOUPLING

65D1 53D7 53A6 8D7 8B5 =PPVCORE_S0_CPU

4x 330uF. 20x 22uF 0805

OMIT C0900 22UF 20% 6.3V CERM 805	OMIT C0901 22UF 20% 6.3V CERM 805	OMIT C0902 22UF 20% 6.3V CERM 805	OMIT C0903 22UF 20% 6.3V CERM 805	OMIT C0904 22UF 20% 6.3V CERM 805	OMIT C0905 22UF 20% 6.3V CERM 805	OMIT C0906 22UF 20% 6.3V CERM 805	OMIT C0907 22UF 20% 6.3V CERM 805	OMIT C0908 22UF 20% 6.3V CERM 805	OMIT C0909 22UF 20% 6.3V CERM 805
OMIT C0910 22UF 20% 6.3V CERM 805	OMIT C0911 22UF 20% 6.3V CERM 805	OMIT C0912 22UF 20% 6.3V CERM 805	OMIT C0913 22UF 20% 6.3V CERM 805	OMIT C0914 22UF 20% 6.3V CERM 805	OMIT C0915 22UF 20% 6.3V CERM 805	OMIT C0916 22UF 20% 6.3V CERM 805	OMIT C0917 22UF 20% 6.3V CERM 805	OMIT C0918 22UF 20% 6.3V CERM 805	OMIT C0919 22UF 20% 6.3V CERM 805
CRITICAL C0950 330UF 20% 2.5V POLY D2T	CRITICAL C0952 330UF 20% 2.5V POLY D2T	CRITICAL C0953 330UF 20% 2.5V POLY D2T	CRITICAL C0954 330UF 20% 2.5V POLY D2T						

CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production

RP0990

0

5%

8486 8B7	CPU_VID<0>	1	8	IMVP6_VID<0> 59C7
8486 8B7	CPU_VID<1>	2	7	IMVP6_VID<1> 59C7
8486 8B7	CPU_VID<2>	3	6	IMVP6_VID<2> 59C7
8486 8B7	CPU_VID<3>	4	5	IMVP6_VID<3> 59C7

1/16W
SM-LF

RP0991

0

5%

8486 8B7	CPU_VID<4>	1	8	IMVP6_VID<4> 59C7
8486 8B7	CPU_VID<5>	2	7	IMVP6_VID<5> 59C7
8486 8B7	CPU_VID<6>	3	6	IMVP6_VID<6> 59C7
NC		4	5	NC

1/16W
SM-LF

VCCA (CPU AVdd) Decoupling

65C6 8B7 =PP1V5_S0_CPU

1x 10uF, 1x 0.01uF

C0980 10uF 20% 6.3V X5R 603	C0981 0.01UF 20% 16V CERM 402

VCCP (CPU I/O) Decoupling

65D6 11C5 11B3 8C7 7D5 7B6 7B5 =PP1V05_S0_CPU

1x 470uF, 6x 0.1uF 0402

C0935 470uF 20% 2.5V TANT D2T CRITICAL	C0936 0.1UF 20% 10V CERM 402	C0937 0.1UF 20% 10V CERM 402	C0938 0.1UF 20% 10V CERM 402	C0939 0.1UF 20% 10V CERM 402	C0940 0.1UF 20% 10V CERM 402	C0941 0.1UF 20% 10V CERM 402

NOTE: This cap is shared between CPU and NB

CPU Decoupling & VID

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 9 OF 105	

CPU ZONE THERMAL SENSOR

LAYOUT NOTE:
ADD GND GUARD TRACE
FOR CPU_THERMD_P AND
CPU_THERMD_N

LAYOUT NOTE:
ROUTE CPU_THERMD_P AND
CPU_THERMD_N ON SAME
LAYER.
10 MIL TRACE
10 MIL SPACING

(TO CPU INTERNAL THERMAL DIODE)
(TC0D)

7C6 OUT CPU_THERMD_P
R1001 499 1% 1/16W MF-LF 402
7C6 IN CPU_THERMD_N
R1002 499 1% 1/16W MF-LF 402
C1001 0.001UF 10% 50V CERM 402

65B3 =PP3V3_S0_THRM_SNR
C1002 0.1UF 10% 16V X5R 402
R1006 10K 5% 1/16W MF-LF 402
R1005 10K 5% 1/16W MF-LF 402

U1001 TMP401 MSOP CRITICAL
VDD
GND
D+
D-
ALERT*/THM2*
THM*
SCLK
SDATA

THRM_CPU_DX_P
THRM_CPU_DX_N
THERM_ALERT_L
THERM_ALERT
27D1 SMB_THRM_CLK TO
27D1 SMB_THRM_DATA TO

PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 10 OF 105	

CPU ITP700FLEX DEBUG SUPPORT

Note: This connection to 1V5_S0 is to steal this mounting pad to add to the 1.5V S0 shape and to provide better feeding of the 1.5V NB rail through its current sense resistor

65C6 =PP1V5_S0_ITPMOUNT

65D6 11B3 9B7 8C7 7D5 7B6 7B5 =PP1V05_S0_CPU

ITP R1101 54.9 1% 1/16W MF-LF 402

ITP R1103 54.9 1% 1/16W MF-LF 402

ITP R1102 22.6 1% 1/16W MF-LF 402

7C6 IN XDP_TDO

ITP R1100 22.6 1% 1/16W MF-LF 402

84D6 12C4 7D6 IN FSB_CPURST_L

65D3 26C5 23D1 =PP3V3_S5_SB_PM

R1104 240 5% 1/16W MF-LF 402

(AND WITH RESET BUTTON)

OUT 26C6 7C6 XDP_DBRESET_L

ITPCONN CRITICAL J1101 52435-2872 F-RT-SM

1	7C6 7B8 OUT	XDP_TDI	
2	7C6 7B8 OUT	XDP_TMS	
3	7C6 OUT	XDP_TRST_L	
4	NC		
5	11B3 7C6 7A8 OUT	XDP_TCK	(TCK)
6	NC		
7		ITP_TDO	
8	84C6 34D3 IN	CPU_XDP_CLK_N	(FROM CK410M HOST 133/167MHZ)
9	84C6 34D3 IN	CPU_XDP_CLK_P	
10			
11	11B3 7C6 7A8 OUT	XDP_TCK	(FBO)
12	84C6 IN	ITPRESET_L	
13	84C6 7C6 IO	XDP_BPM_L<5>	
14			
15	84C6 7C6 IO	XDP_BPM_L<4>	
16			
17	84C6 7C6 IO	XDP_BPM_L<3>	
18			
19	84C6 7C6 IO	XDP_BPM_L<2>	
20			
21	84C6 7C6 IO	XDP_BPM_L<1>	
22			
23	84C6 7C6 IO	XDP_BPM_L<0>	
24	NC		
25			
26	65D6 11C5 9B7 8C7 7D5 7B6 7B5	=PP1V05_S0_CPU	
27			
28			
30			

518S0320

C1100 0.1UF 10% 16V X5R 402

R1106 680 5% 1/16W MF-LF 402

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM. (DEBUG PORT ACTIVE)

(DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC (DEBUG PORT RESET)

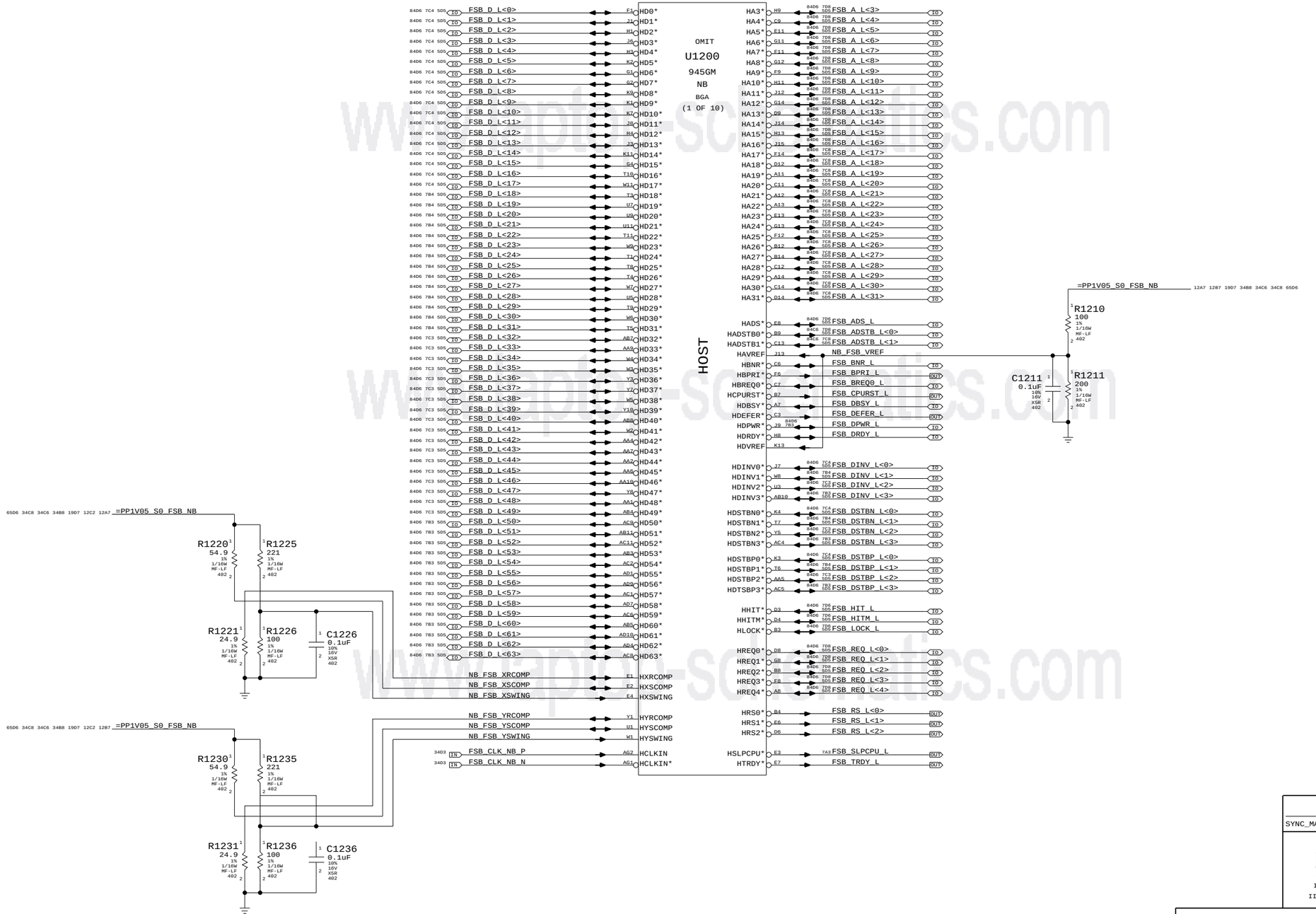
ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 11 OF 105	



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 12 OF 105	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

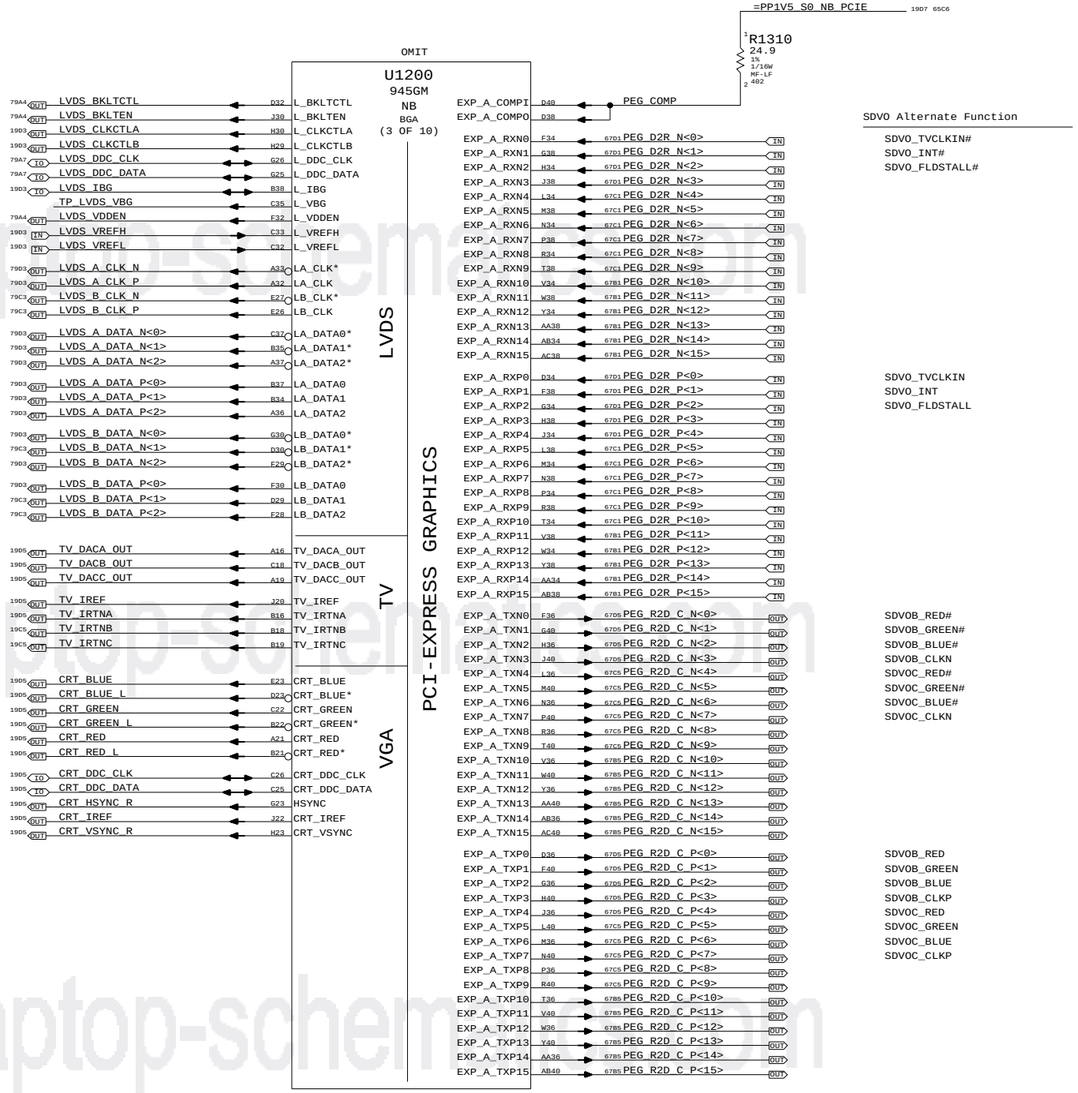
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

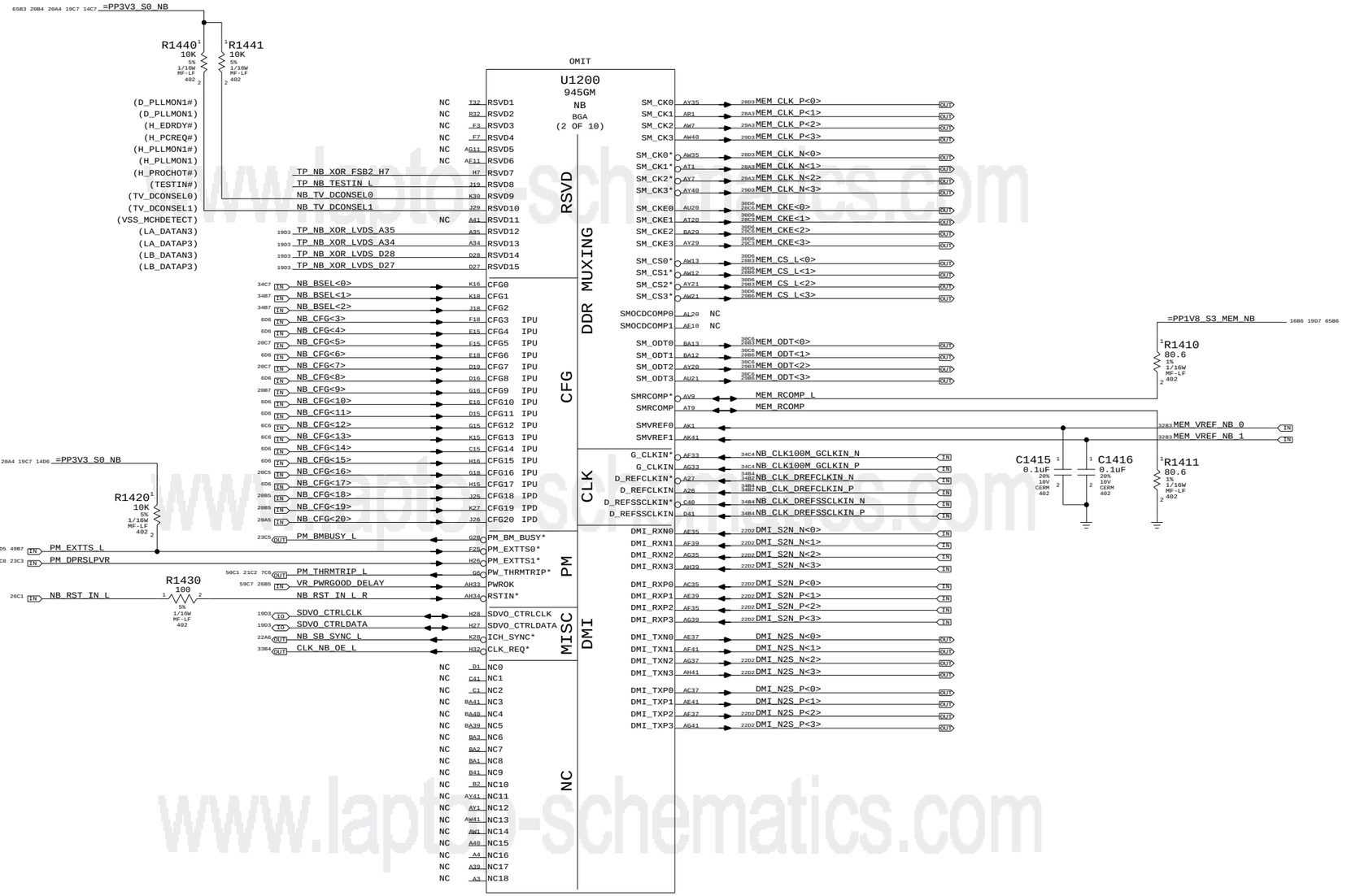


NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 13 OF 105	

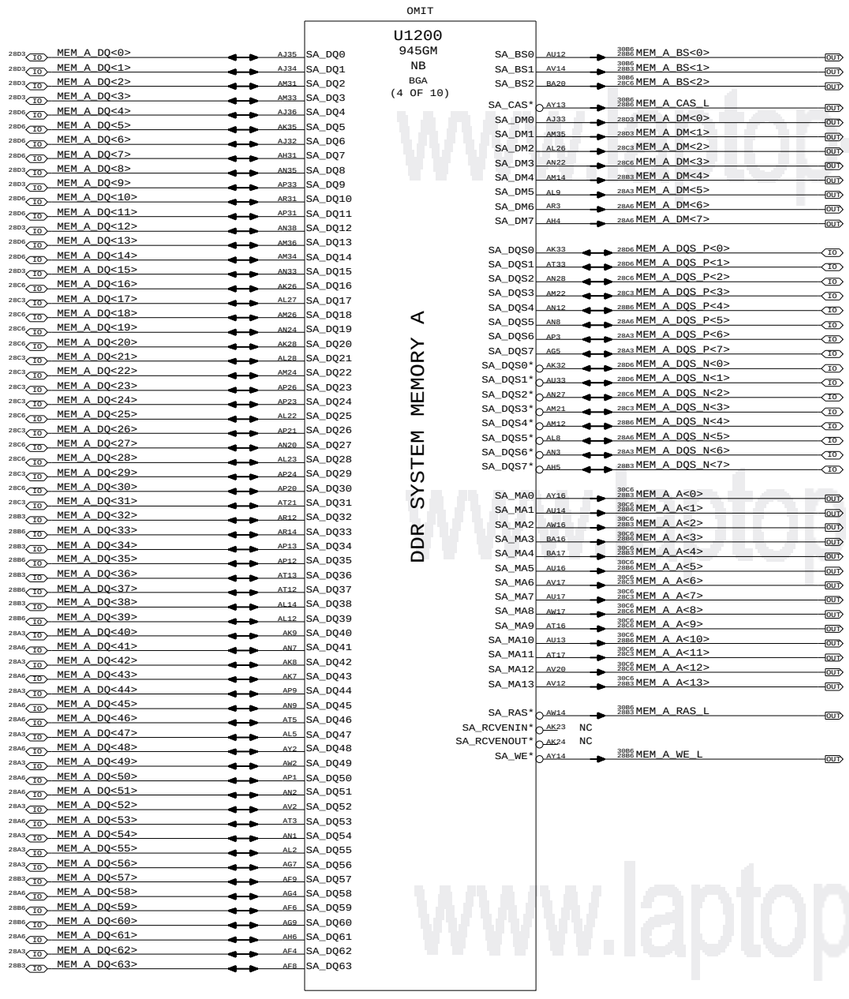


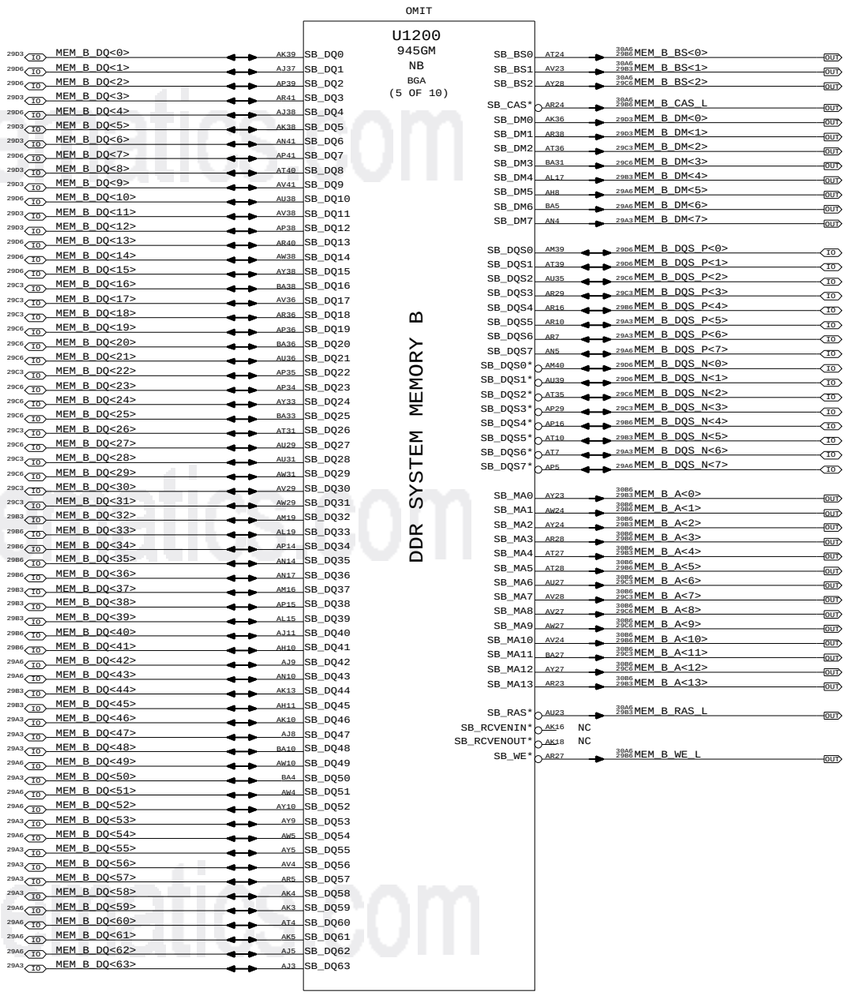
NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 14 OF 105	





NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 15 OF 105	

1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.5V, Internal Graphics: 5500mA Max

=PPVCORE_S0_NB 16D3 19C8 19D2 19D7 65D6
1.05V or 1.5V

U1200
945GM
NB
BGA
(6 OF 10)
OMIT
VCC

1.8V Max Current

Speed	1 Channel	2 Channel
400MTs	1300mA	2400mA
533MTs	1500mA	2800mA
667MTs	1700mA	3200mA

NB_VCCSM_LF4
NB_VCCSM_LF5

C1614 0.47UF 10% 6.3V CERM-X5R 402
C1613 0.47UF 10% 6.3V CERM-X5R 402

C1615 0.47UF 10% 6.3V CERM-X5R 402 65B6 19D7 14C2 =PP1V8_S3_MEM_NB
Layout Note: Place near pin BA23

C1620 10uF 20% 6.3V X5R 603
C1621 10uF 20% 6.3V X5R 603
Layout Note: Place in cavity

C1610 0.47UF 10% 6.3V CERM-X5R 402
Layout Note: Place near pin BA15

NB_VCCSM_LF2
NB_VCCSM_LF1

C1612 0.47UF 10% 6.3V CERM-X5R 402
C1611 0.47UF 10% 6.3V CERM-X5R 402

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

65D6 19D7 19D2 19C8 16C8 =PPVCORE_S0_NB

OMIT

U1200
945GM
NB
BGA
(7 OF 10)
NCTF

=PP1V5_S0_NB_VCCAUX 17B6 19C4 19D7 65B6

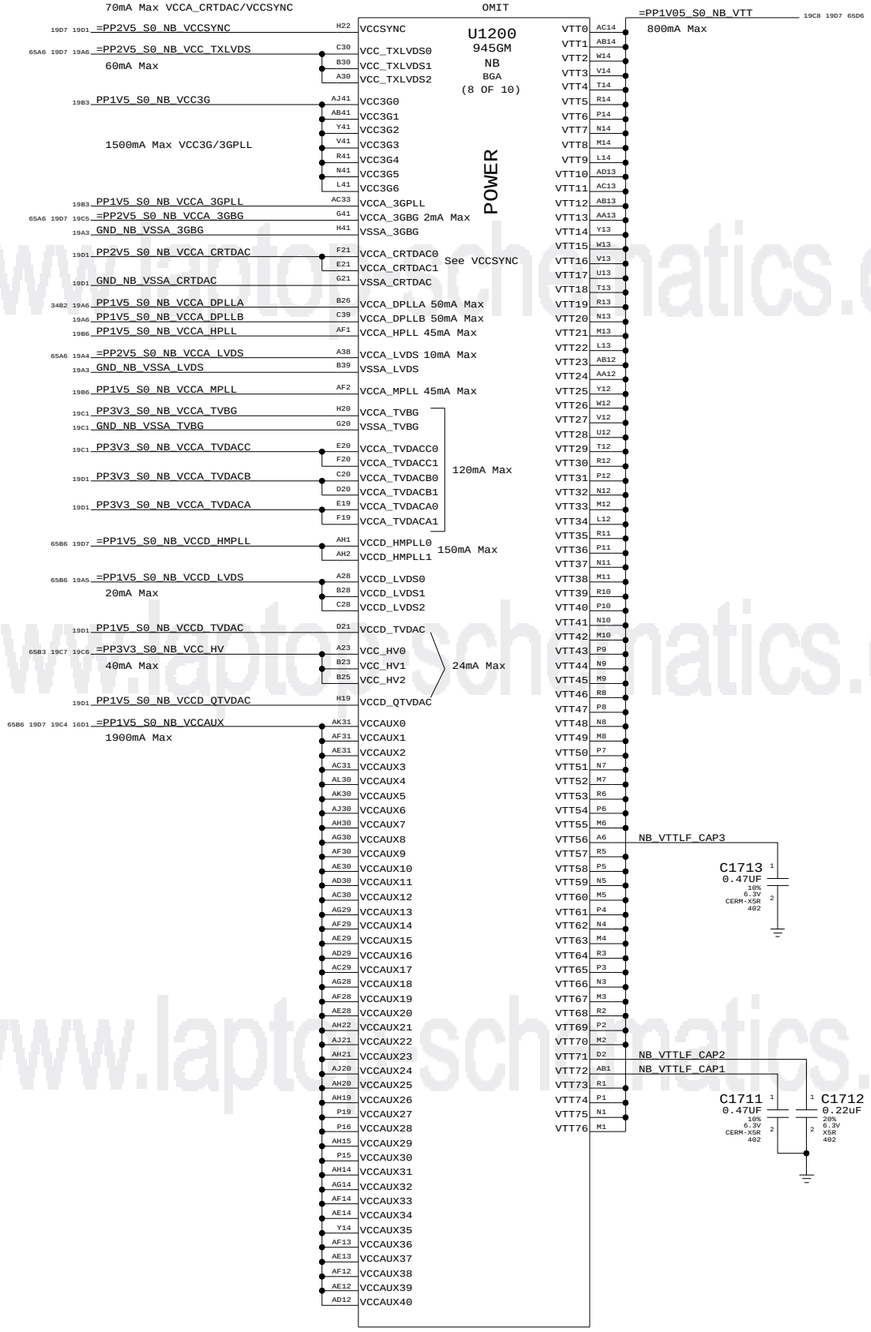
NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE	SHT	OF
NONE	16	105

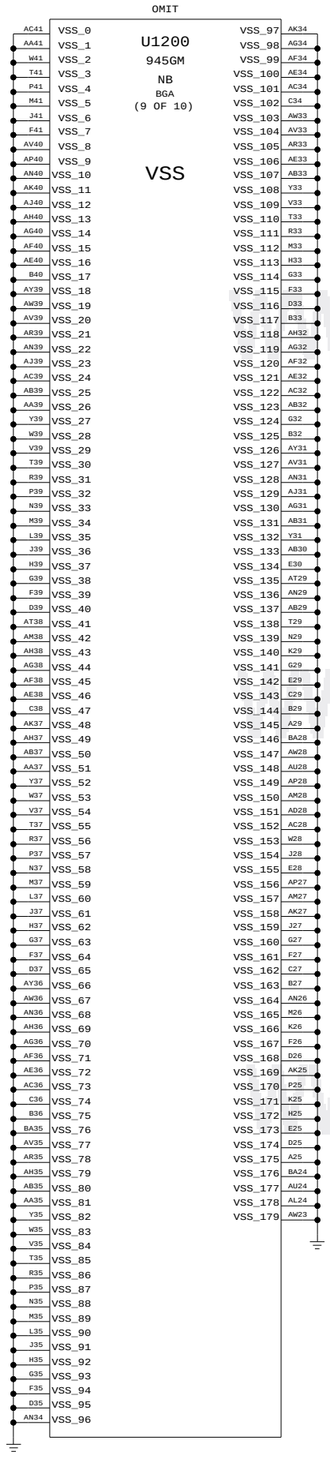


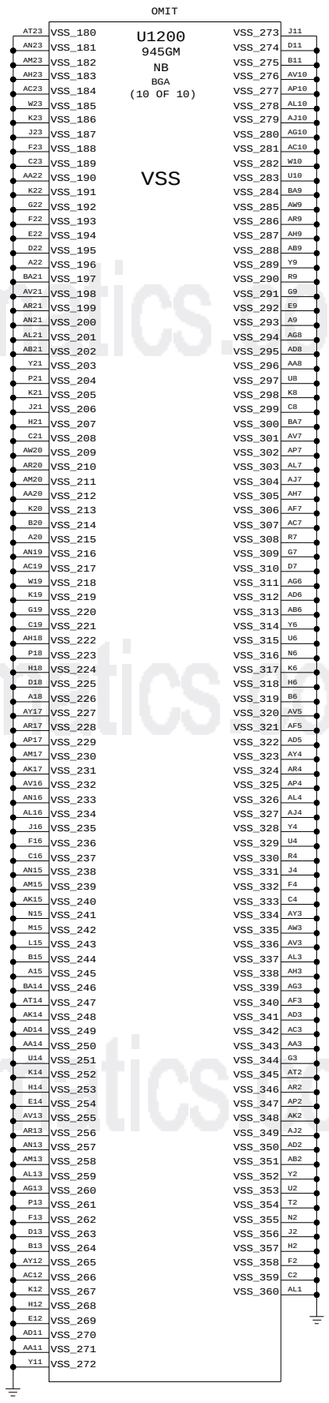
NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 17 OF 105	





NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 18 OF 105	

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	=PPVCORE_S0_NB	16C8 16D2 19C8 19D2 65D6	1500mA Max
	=PP1V05_S0_FSB_NB	12A7 12B2 12C2 14B8 34C6 34C8 65D5	10mA Max?
	=PP1V05_S0_NB_VTT	17D3 19C8 65D6	800mA Max
	=PP1V05_S0_NB_CRT	19D6 65D6	?mA Max
3674mA Max	=PP1V5_S0_NB	60A7 65C6 65C8	?mA Max
	=PP1V5_S0_NB_3G	19B5 65C6	1500mA Max
	=PP1V5_S0_NB_3GPLL	19B5 65C6	
	=PP1V5_S0_NB_PCIE	13D2 65C6	?mA Max
	=PP1V5_S0_NB_PLL	19B8 65B6	100mA Max
	=PP1V5_S0_NB_TVDAC	19D2 65B6 19D6	24mA Max
	=PP1V5_S0_NB_VCCD_HMPLL	17C6 65B6	150mA Max
	=PP1V5_S0_NB_VCCAUX	16D1 17B6 19C8 65B6	1900mA Max
3200mA Max	=PP1V8_S3_MEM_NB	14C2 16B6 65B6	3200mA Max
132mA Max	=PP2V5_S0_NB_VCCSYNC	17D6 19D1	70mA Max
	=PP2V5_S0_NB_VCC_TXLVDS	17D6 19A6	60mA Max
	=PP2V5_S0_NB_VCCA_3GBG	17D6 19C5 65A6	2mA Max
40mA Max?	=PP3V3_S0_NB	14C7 14D6 20A4 20B4 65B3	?mA Max
	=PP3V3_S0_NB_VCC_HV	17C6 19C6 65B3	40mA Max

65D6 19D7 =PP1V05_S0_NB_CRT

CRT_RED 13B5
CRT_GREEN 13B5
CRT_BLUE 13B5
CRT_RED_L 13B5
CRT_GREEN_L 13B5
CRT_BLUE_L 13B5
CRT_IREF 13B5
CRT_HSYNC_R 13B5
CRT_VSYNC_R 13B5

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK 13B5
TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA 13B5

65B6 19D7 19D2 =PP1V5_S0_NB_TVDAC

TV_DACA_OUT 13C5
TV_DACB_OUT 13C5
TV_DACC_OUT 13C5
TV_IREF 13C5
TV_IRTNA 13C5
TV_IRTNB 13C5
TV_IRTNC 13C5

TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA 13D5
TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB 13D5
NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34 14C6
NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35 14C6
NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27 14C6
NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28 14C6
TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK 14B6
TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA 14B6

LVDS_IBG 13D5

R1990 1.5K 1% 1/16W MF-LF 402 (1 — 2)

LVDS_VREFH 13D5
LVDS_VREFL 13D5

65D6 19D7 19C8 16D3 16C8 =PPVCORE_S0_NB

65B6 19D7 19D6 =PP1V5_S0_NB_TVDAC

(MCH CRTDAC ANALOG 2.5V PWR)
PP2V5_S0_NB_VCCA_CRTDAC 17D6
GND_NB_VSSA_CRTDAC 17D6

(MCH H/V SYNC 2.5V PWR)
=PP2V5_S0_NB_VCCSYNC 17D6 19D7

(MCH TVDAC DEDICATED PWR 1.5V)
PP1V5_S0_NB_VCCD_TVDAC 17C6

(MCH TVDAC DIGITAL QUIET 1.5V PWR)
PP1V5_S0_NB_VCCD_QTVDAC 17B6

(MCH TV OUT CHANNEL A 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACA 17C6

(MCH TV OUT CHANNEL B 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACB 17C6

(MCH TV OUT CHANNEL C 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACC 17C6

(MCH TV DAC BAND GAP 3.3V PWR)
PP3V3_S0_NB_VCCA_TVBG 17C6

GND_NB_VSSA_TVBG 17C6

65D6 16D7 16C8 19D7 16D2 =PPVCORE_S0_NB
1500mA Max

GMCH CORE PWR 1.05V BYPASS
CRITICAL
C1900 470uF 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1uF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

65D6 19D7 17D3 =PP1V05_S0_NB_VTT
800mA Max

MCH VTT BYPASS
(MCH FSB 1.05V PWR)
(SHARE C0940 470UF)
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603
Layout Note: Place in cavity
C1967 0.22uF 20% 6.3V X5R 402
Layout Note: Place on the edge

65B3 19C7 17C6 =PP3V3_S0_NB_VCC_HV
40mA Max

MCH VCC_HV BYPASS
(MCH HV BUFFER 3.3V PWR)
C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

65A6 19D7 17D6 =PP2V5_S0_NB_VCCA_3GBG
2mA Max

MCH VCCA_3GBG BYPASS
(MCH PCIE/DMI BAND GAP 2.5V PWR)
C1916 0.1uF 20% 10V CERM 402

65B6 19D7 17B6 16D1 =PP1V5_S0_NB_VCCAUX
1900mA Max

GMCH VCCAUX FILTER
(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)
C1918 0.1uF 20% 10V CERM 402

65B6 19D7 19C6 =PP1V5_S0_NB_PLL
100mA Max

L1934 FERR-120-OHM-0.2A 0603
GMCH VCCA_HPLL FILTER
(HOST PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_HPLL 17C6
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
45mA Max
C1934 22UF 20% 6.3V CERM 805 OMIT
C1935 0.1uF 20% 10V CERM 402

L1936 FERR-120-OHM-0.2A 0603
GMCH VCCA_MPLL FILTER
(MCH MEMORY PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_MPLL 17C6
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
45mA Max
C1936 22UF 20% 6.3V CERM 805 OMIT
C1937 0.1uF 20% 10V CERM 402

65A6 =PP2V5_S0_NB_DPLL

CRITICAL
U1900 TPS73115 SOT23-5
IN EN NR/FB OUT GND
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
PP1V5_S0_NB_DPLL
TPS73115_NR
C1950 1uF 10% 6.3V CERM 402
C1951 0.01uF 10% 16V CERM 402
C1952 10uF 20% 6.3V X5R 603

NO STUFF
R1953 0 5% 1/16W MF-LF 402
GMCH VCCA_DPLLA FILTER
(CRT/TVOUT PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_DPLLA 17C6 34B2
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
50MA MAX

R1954 0 5% 1/16W MF-LF 402
GMCH VCCA_DPLLB FILTER
(LVDS PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_DPLLB 17C6 65A6 19D7 17D6
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
50MA MAX

C1953 0.1uF 20% 10V CERM 402 NO STUFF
C1954 0.1uF 20% 10V CERM 402

65B6 17C6 =PP2V5_S0_NB_VCC_TXLVDS
60MA MAX

MCH VCC_TXLVDS BYPASS
(MCH LVDS TRANSMITTER 2.5V PWR)
C1990 4.7UF 20% 6.3V CERM 603
C1991 0.1uF 20% 10V CERM 402

65B6 17C6 =PP1V5_S0_NB_VCCD_LVDS
20MA MAX

MCH VCCD_LVDS BYPASS
(MCH LVDS DIGITAL 1.5V PWR)
C1992 10uF 20% 6.3V X5R 603
C1993 0.1uF 20% 10V CERM 402

65A6 17C6 =PP2V5_S0_NB_VCCA_LVDS
10MA MAX

MCH VCCA_LVDS BYPASS
(MCH LVDS ANALOG 2.5V PWR)
C1994 0.01UF 20% 16V CERM 402
C1995 0.1uF 20% 10V CERM 402
GND_NB_VSSA_LVDS 17C6
Layout Note: Route to caps, then GND

65C6 19D7 =PP1V5_S0_NB_3G
1500mA Max

L1970 91nH 1210
Layout Note: Place L and C close to MCH
C1970 220UF 20% 2.5V POLY CASE-B2

GMCH VCC3G FILTER
(PCI-E/DMI ANALOG 1.5V PWR)
PP1V5_S0_NB_VCC3G 17D6
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.

65C6 19D7 =PP1V5_S0_NB_3GPLL
1500mA Max

L1975 1.0UH-220MA-0.12-OHM 0805
PP1V5_S0_NB_3GPLL_F
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=1.5V
R1975 0.51 1% 1/16W MF-LF 402

GMCH VCCA_3GPLL FILTER
(3GIO PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_3GPLL 17D6
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402
GND_NB_VSSA_3GBG 17D6
Layout Note: 3GPLL 10uF cap should be placed in cavity
Layout Note: Route to caps, then GND

1500mA Max

NB (GM) Decoupling

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 19 OF 105	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14C6 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14C6 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14C6 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14C6 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4 65B3
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14C6 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4 65B3
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14C6 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14C7 14D6 19C7 20B4 65B3
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14B6 NB_CFG<20>
Internal pull-down

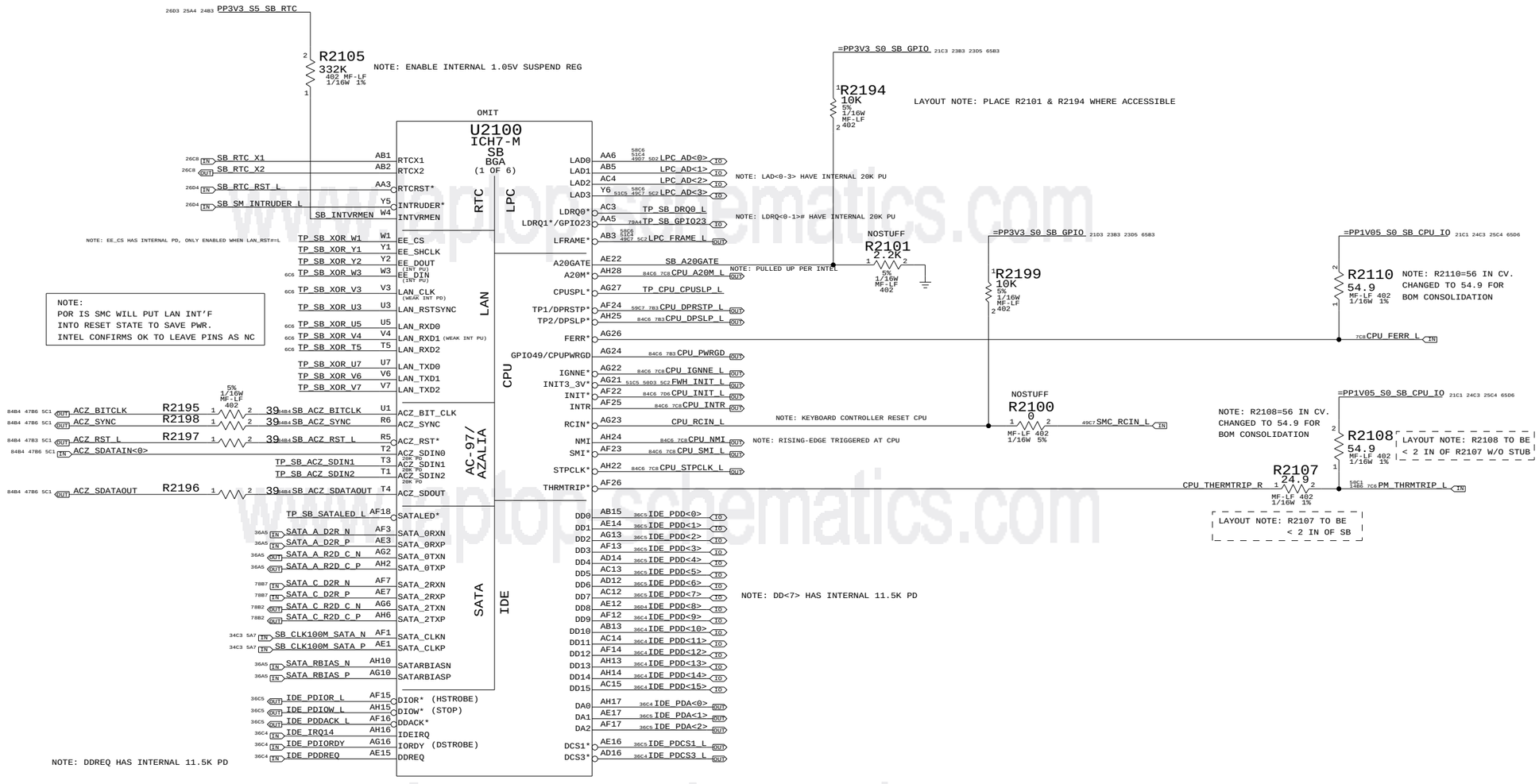
PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 20 OF 105	



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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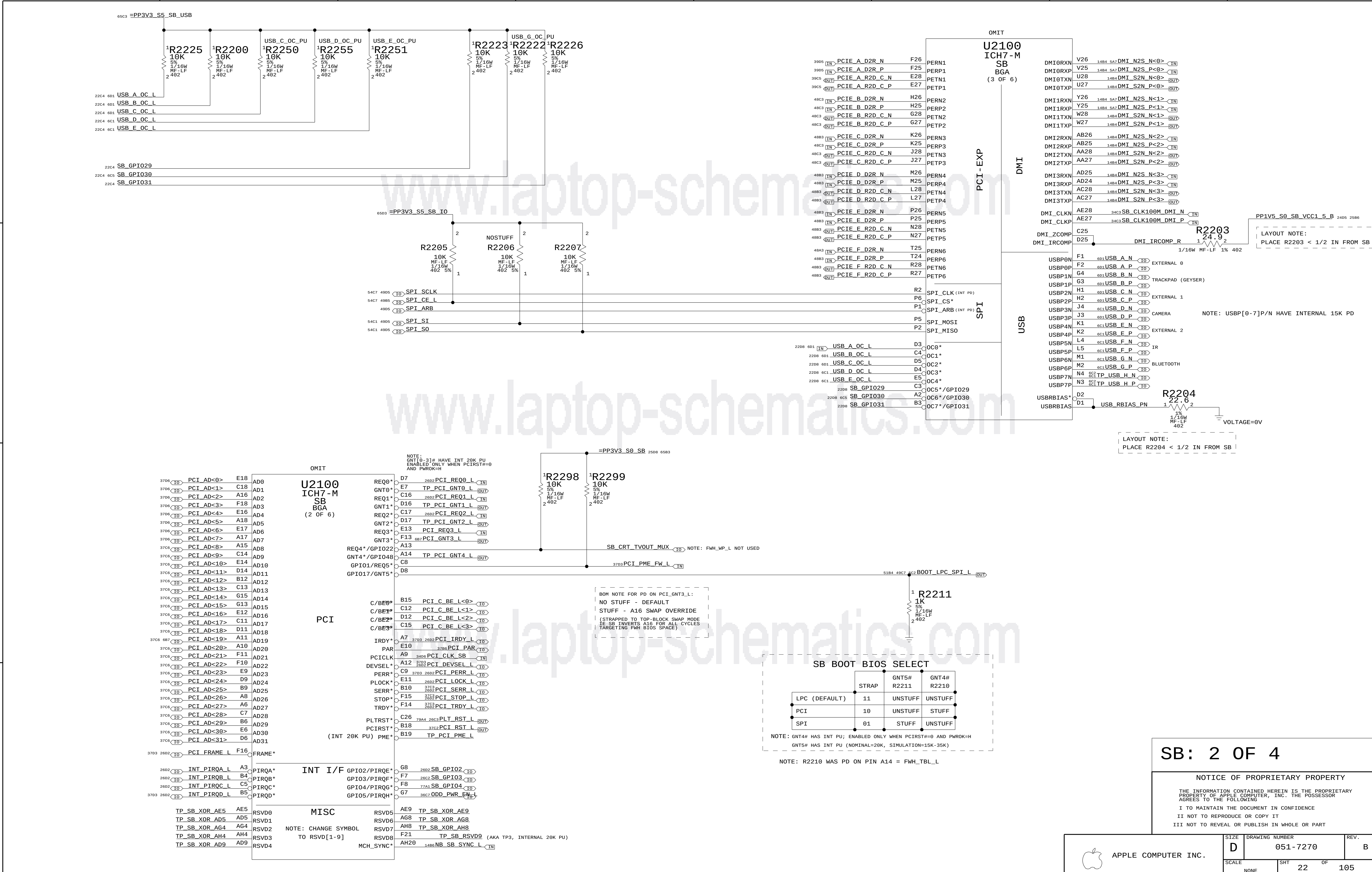
SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 21 OF 105	



SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7270	REV. B
	SCALE NONE	SHT 22 OF 105	

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21C3 21D3 23B3 65B3

=PP3V3_S5_SB 23A7 23B7 23D8 25C8 65D3

65D3 25C8 23D4 23B7 23A7 =PP3V3_S5_SB

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2323 NO_REBOOT_MODE 1K 1/16W 402 MF-LF 5%

RP2300 10K 5% 1/16W SM-LF

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

27D8 TO SMB_CLK — C22 SMBCLK
27D8 TO SMB_DATA — B22 SMBDATA
SMB_LINK_ALERT_L — A26 LINKALERT*
SMLINK<0> — B25 SMLINK0
NOT USED — SMLINK<1> — A25 SMLINK1
PM_RI_L — A28 RI*

SB_SPKR — A19 SPKR (INT WEAK PD)
58C6 51B5 50A2 49C5 5C2 OUT PM_SUS_STAT_L — A27 SUS_STAT*
49B7 26C5 58Z IN PM_SYSRST_L — A22 SYS_RST*
14B6 IN PM_BMBUSY_L — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE

SYS GPIO

33C4 OUT PM_STPPCI_L — AC20 GPIO18/STPPCI*
33C4 OUT PM_STPCPU_L — AF21 GPIO20/STPCPU*
SB_GPIO26 — A21 GPIO26
23A6 BIOS_REC — B21 GPIO27
23A6 FWH_MFG_MODE — E23 GPIO28
58C6 51C4 49C5 5C2 TO PM_CLKRUN_L — AG18 GPIO32/CLKRUN*
26A4 TP_GPU_D3COLD_RST_L — AC19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L — U2 GPIO34/AZ_DOCK_RST*
47C3 39C6 58L IN PCIE_WAKE_L — F20 WAKE*
58C6 51C5 49C7 5C2 TO INT_SERIRQ — AH21 SERIRQ
49B7 IN PM_THRM_L — AF20 THRM*
26B8 IN VR_PWRGD_CK410 — AD22 VRMPWRGD
TO TP_SB_GPIO6 — AC21 GPIO6
49B7 IN SMC_RUNTIME_SCI_L — AC18 GPIO7
49B7 IN SMC_EXTSMI_L — E21 GPIO8

PWR MNGT

SATA GPIO

GPIO21/SATA0GP — AF19 SB_GPIO21 — 100 — R2302
GPIO19/SATA1GP — AH18 SB_GPIO19 — 100 — R2303
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19 SB_GPIO37 — 100 — R2305
36B5 SATA_C_DET_L IN

CLKS

CLK14 — AC1 34A6 SB_CLK14P3M_TIMER IN
CLK48 — B2 34C7 SB_CLK48M_USBCTLR IN
SUSCLK — C20 6C6 SUS_CLK_SB OUT

SLP_S3* — B24 64C8 49C5 43B7 42A8 PM_SLP_S3_L OUT
SLP_S4* — D23 49C5 64B8 41B6 PM_SLP_S4_L OUT
SLP_S5* — F22 50A2 49C5 PM_SLP_S5_L OUT
PWROK — AA4 26A6 PM_SB_PWROK IN
GPIO16/DPRSLPVR — AC22 59C8 64C9 14B7 PM_DPRSLPVR OUT
TP0/BATLOW* — C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN* — C23 49D7 PM_PWRBTN_L IN
LAN_RST* — C19 49D7 PM_LAN_ENABLE IN — NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* — Y4

GPIO

GPIO9 — E20 50B2 49B5 SMS_INT_L IN
GPIO10 — A20 49D7 SMC_SB_NMI IN
DEF=GPI GPIO12 — F19 48A3 LAN_ENERGY_DET IN
GPIO13 — E19
DEF=GPI GPIO14 — R4 36D5 IDE_RESET_L OUT
GPIO15 — E22 SV_SET_UP 5C2 23B6 51B5
GPIO24 — R3 CRB_SV_DET 23B6
GPIO25 — D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 33B4 SB_CLK100M_SATA_OE_L OUT
GPIO38 — AD20 TP_SB_GPIO38 TO
DEF=GPI GPIO39 — AE20 23A3 SATA_C_PWR_EN_L OUT

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB_PM 11B5 26C5 65D3

R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

49D7 PM_BATLOW_L IN
49D7 PM_RSMRST_L IN
R2399 100K 5% 1/16W 402 MF-LF
49D5 SMC_WAKE_SCI_L IN

65D3 25C8 23D8 23D4 23A7 =PP3V3_S5_SB

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 MF-LF 5%

SV_SET_UP 5C2 23C3 51B5
CRB_SV_DET 23C3

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

=PP3V3_S0_SB_GPIO 21C3 21D3 23D5 65B3

R2388 10K 5% 1/16W MF-LF 402
23B3 SATA_C_PWR_EN_L

65D3 25C8 23D8 23D4 23B7 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE 23C5
BIOS_REC 23C5

SB: 3 OF 4
SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

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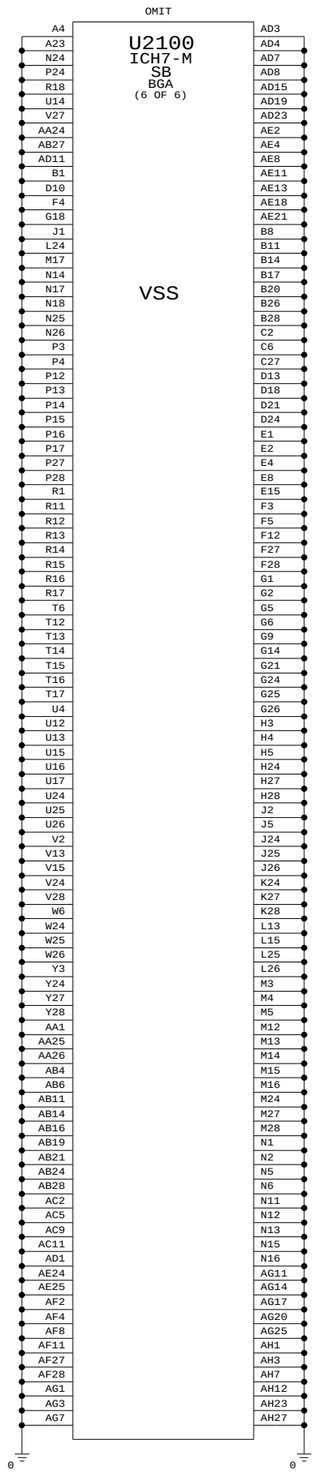
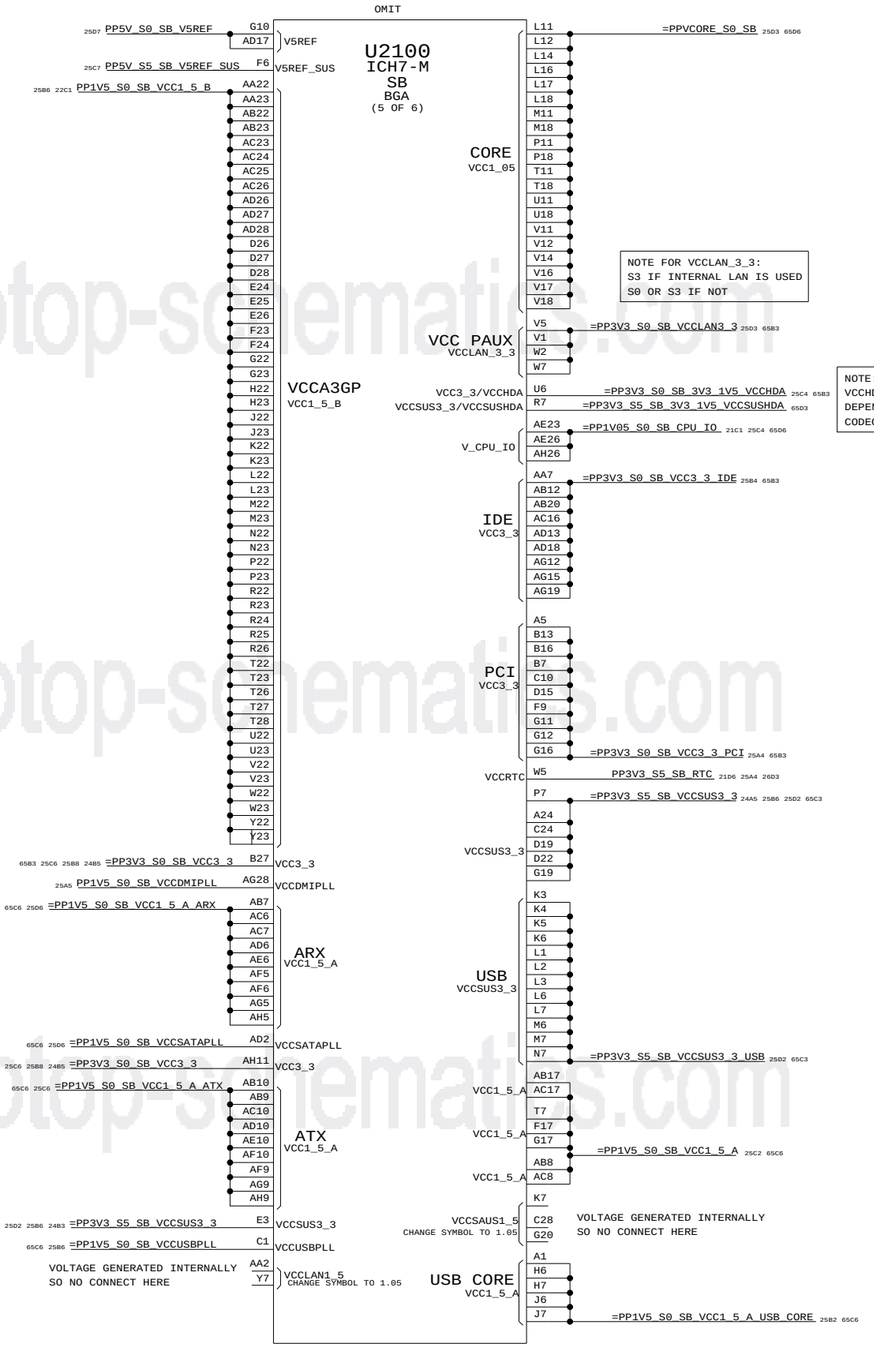
D	051-7270	B
SCALE: NONE	SHT 23 OF 105	





SB: 4 OF 4

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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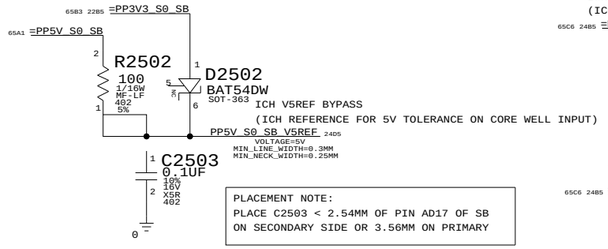
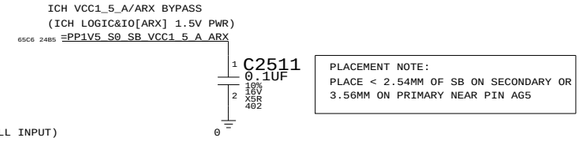
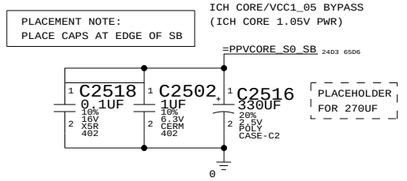
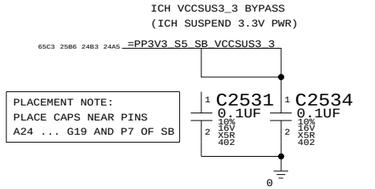
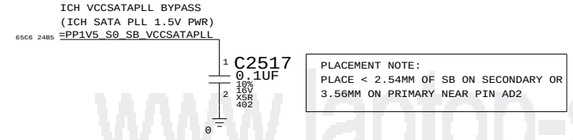
SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 24 OF 105	

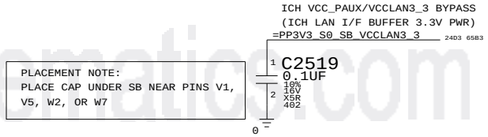


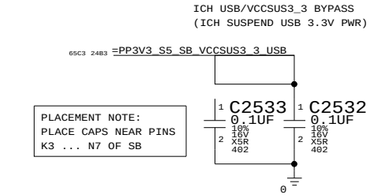


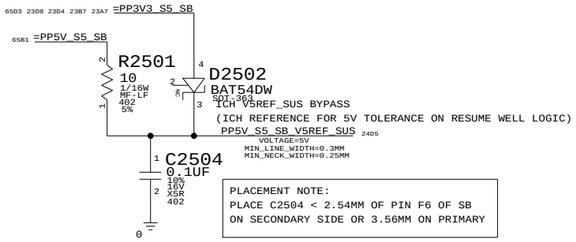


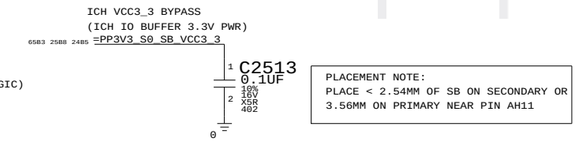


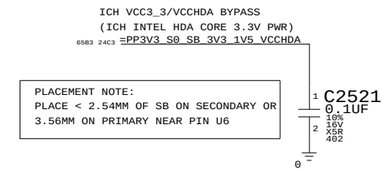


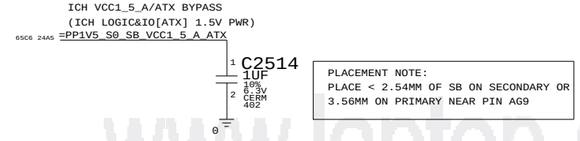


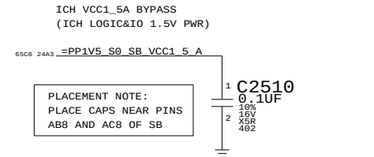


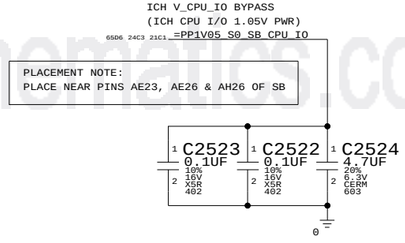


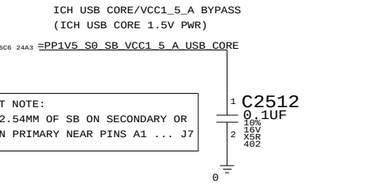


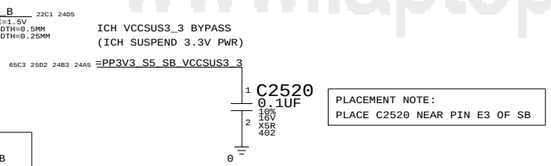


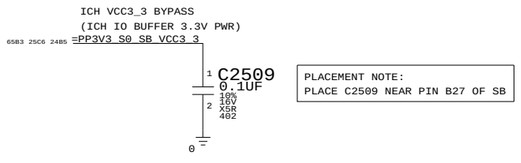


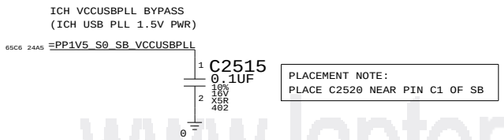


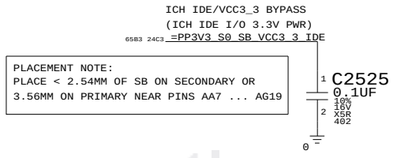


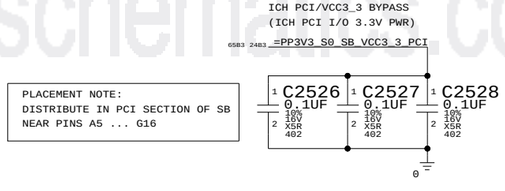


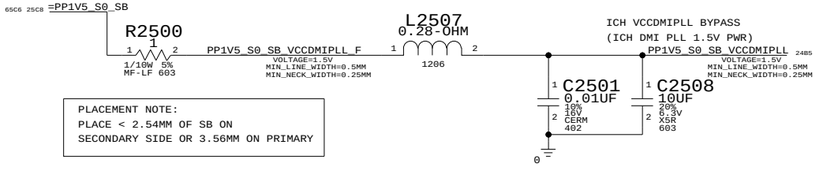


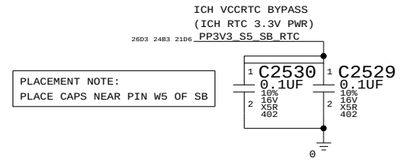












SB: 4 OF 4

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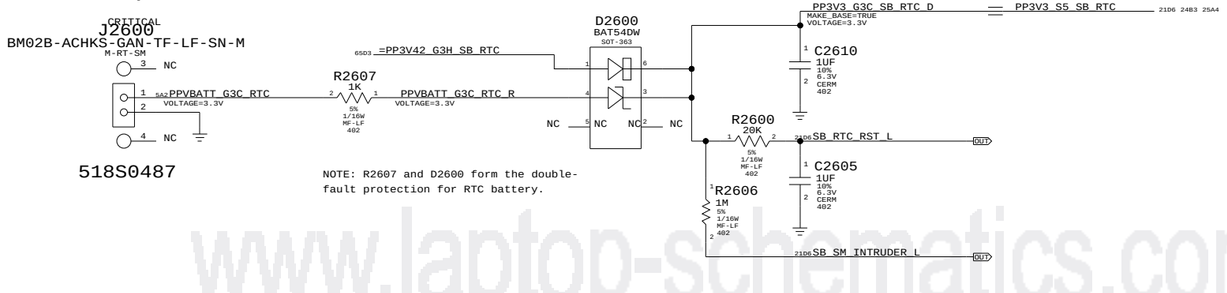
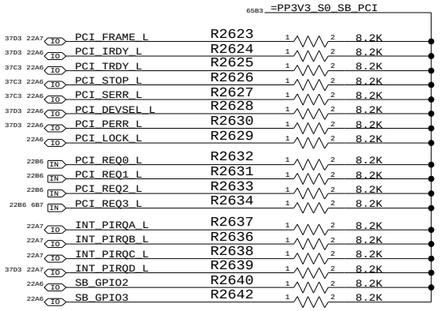
SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 25 OF 105	

RTC Battery Connector

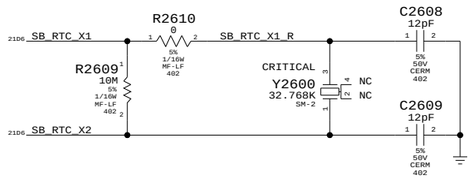


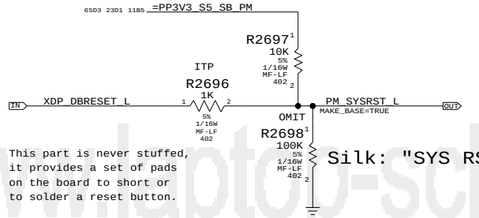
NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



Pullup on SB_GPIO4 removed as it now defaults low for use as DVI_HPD in muxed graphics solution.

SB RTC Crystal Circuit



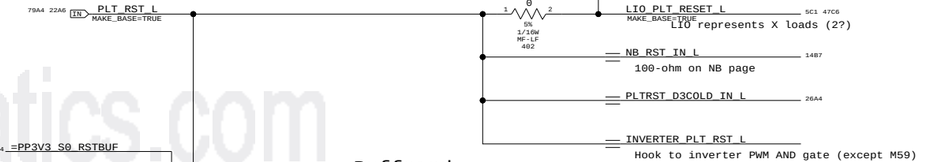


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

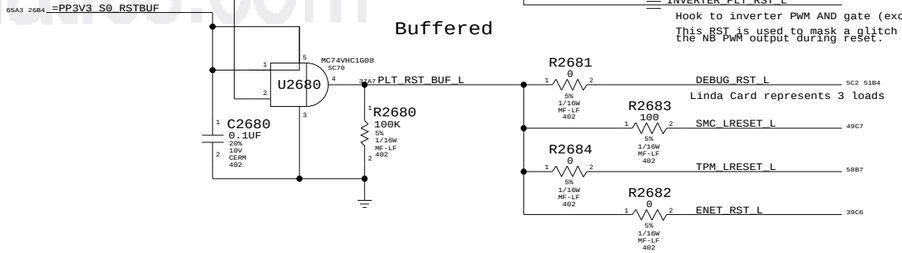
Silk: "SYS RST"

Platform Reset Connections

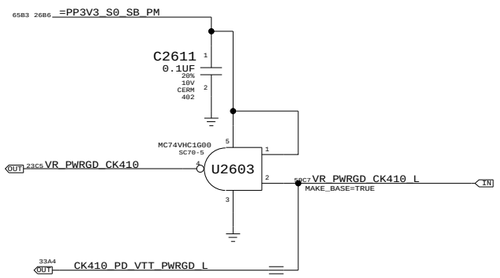
Unbuffered



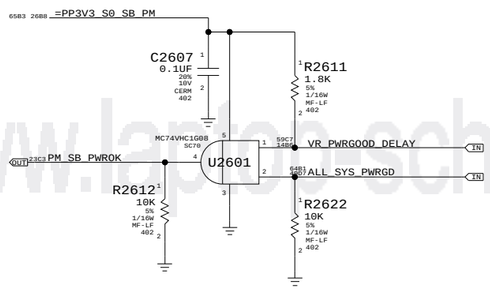
Buffered



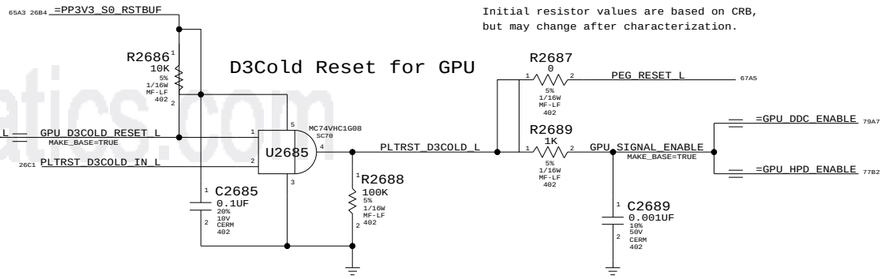
Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter



D3Cold Reset for GPU



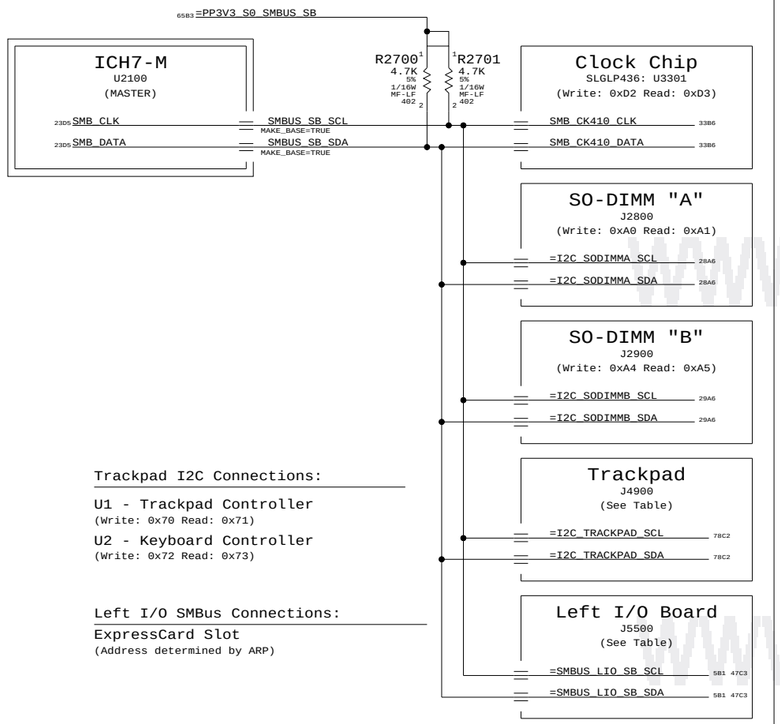
SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 26 OF 105	

ICH7-M SMBus Connections



Trackpad I2C Connections:

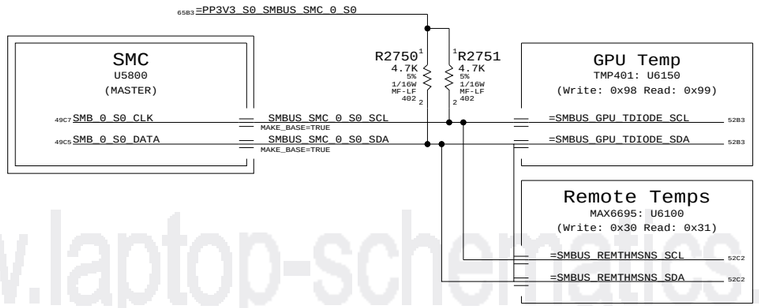
U1 - Trackpad Controller
(Write: 0x70 Read: 0x71)

U2 - Keyboard Controller
(Write: 0x72 Read: 0x73)

Left I/O SMBus Connections:

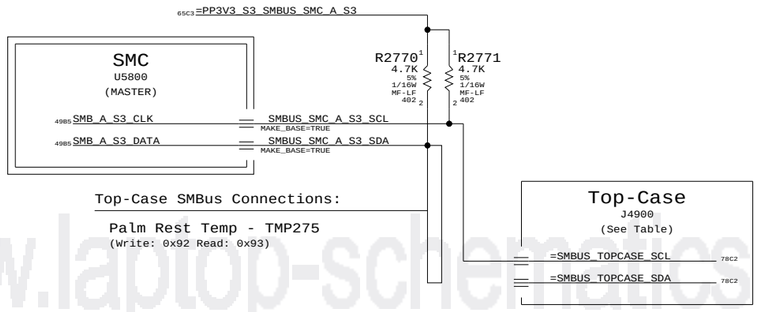
ExpressCard Slot
(Address determined by ARP)

SMC "0" SMBus Connections



SMC "A" SMBus Connections

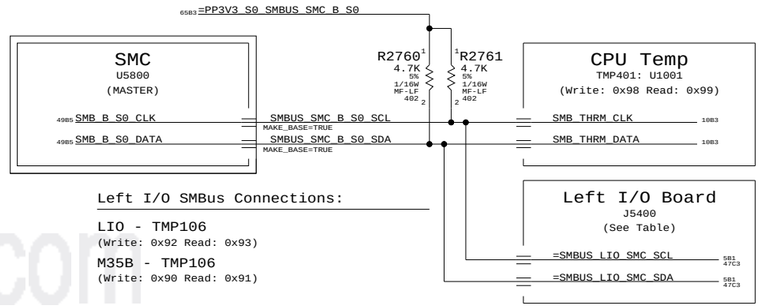
NOTE: SMC RMT bus remains powered and may be active in S3 state



Top-Case SMBus Connections:

Palm Rest Temp - TMP275
(Write: 0x92 Read: 0x93)

SMC "B" SMBus Connections

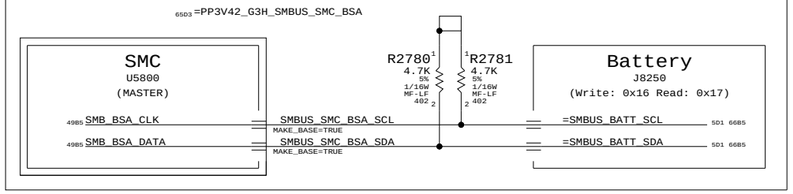


Left I/O SMBus Connections:

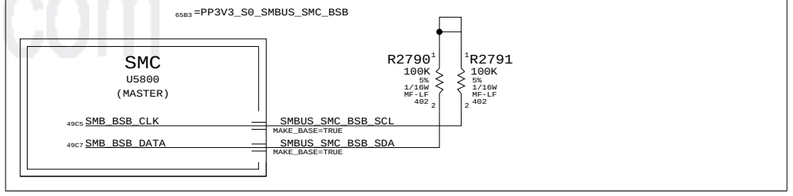
LIO - TMP106
(Write: 0x92 Read: 0x93)

M35B - TMP106
(Write: 0x90 Read: 0x91)

SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE	SHT	OF
NONE	27	105

Page Notes

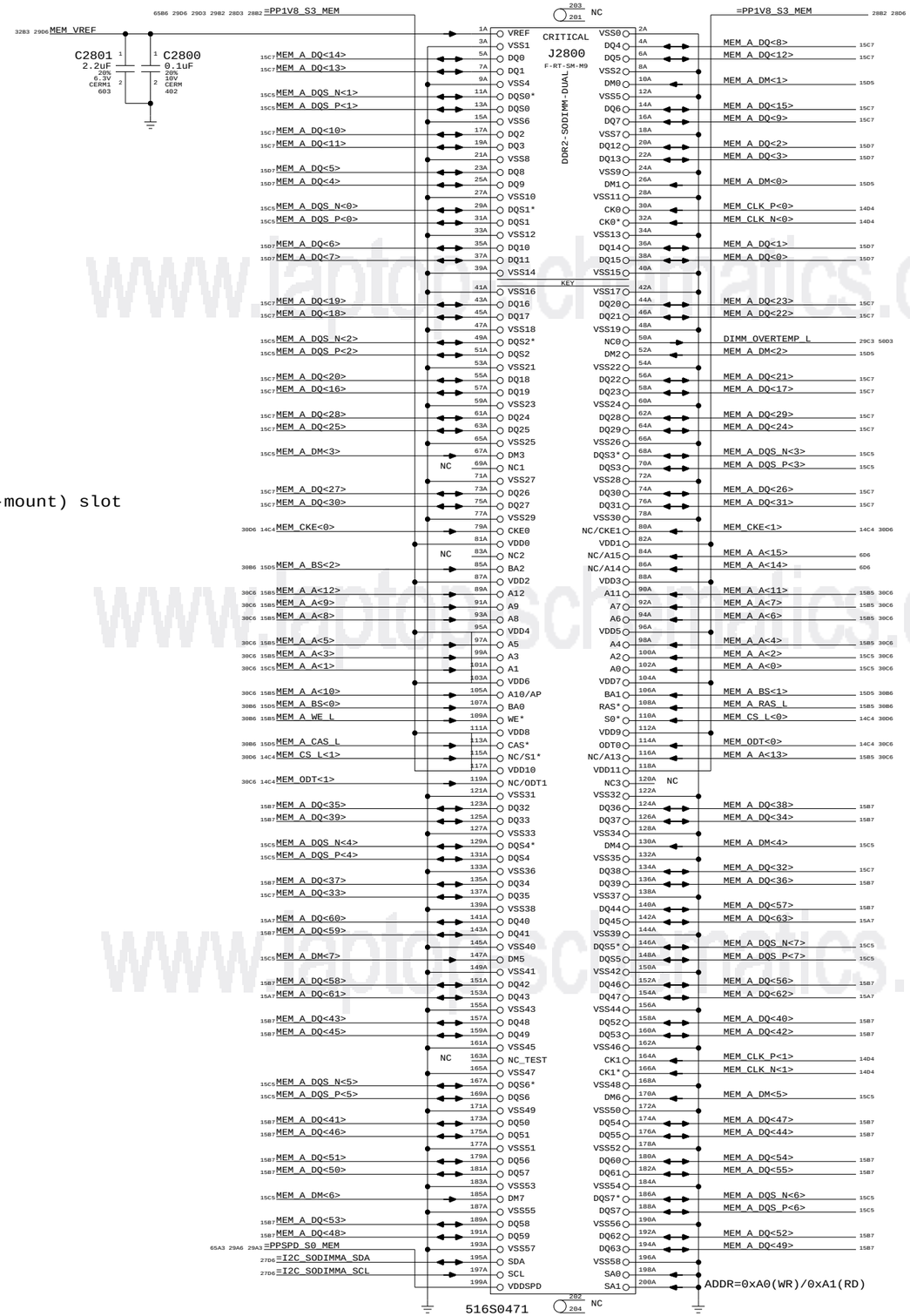
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

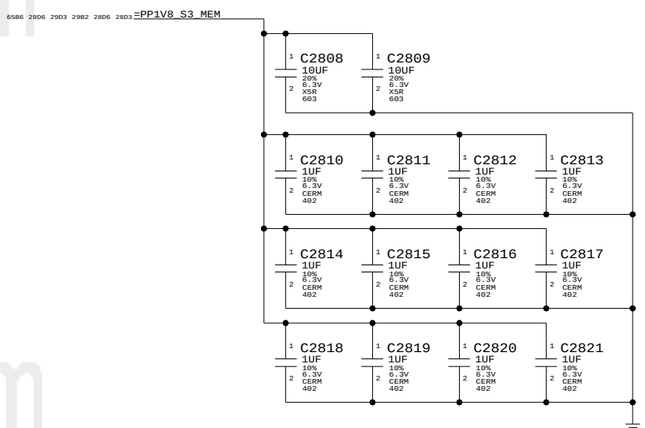
NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Expansion" (surface-mount) slot



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 28 OF 105	

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Factory" (thru-hole) slot

65B6 29D3 29B2 28D6 28D3 28B2 =PP1V8_S3_MEM

32B3 28D6 MEM_VREF

C2901 2.2uF 20% 6.3V CERM1 603

C2900 0.1uF 20% 10V CERM 402

DDR2-SODIMM-DUAL

CRITICAL
J2900
F-RT-TH1

		1B	VREF		201	NC	
		3B	VSS1		2B	VSS0	
15C4	MEM_B_DQ<15>	5B	DQ0		4B	DQ4	MEM_B_DQ<9> 15C4
15C4	MEM_B_DQ<14>	7B	DQ1		6B	DQ5	MEM_B_DQ<11> 15C4
		9B	VSS4		8B	VSS2	
15C2	MEM_B_DQS_N<1>	11B	DQS0*		10B	DM0	MEM_B_DM<1> 15D2
15C2	MEM_B_DQS_P<1>	13B	DQS0		12B	VSS5	
		15B	VSS6		14B	DQ6	MEM_B_DQ<12> 15C4
15C4	MEM_B_DQ<10>	17B	DQ2		16B	DQ7	MEM_B_DQ<8> 15C4
15C4	MEM_B_DQ<13>	19B	DQ3		18B	VSS7	
		21B	VSS8		20B	DQ12	MEM_B_DQ<3> 15D4
15D4	MEM_B_DQ<7>	23B	DQ8		22B	DQ13	MEM_B_DQ<6> 15D4
15D4	MEM_B_DQ<2>	25B	DQ9		24B	VSS9	
		27B	VSS10		26B	DM1	MEM_B_DM<0> 15D2
15C2	MEM_B_DQS_N<0>	29B	DQS1*		28B	VSS11	
15C2	MEM_B_DQS_P<0>	31B	DQS1		30B	CK0	MEM_CLK_P<3> 14D4
		33B	VSS12		32B	CK0*	MEM_CLK_N<3> 14D4
15D4	MEM_B_DQ<1>	35B	DQ10		34B	VSS13	
15D4	MEM_B_DQ<4>	37B	DQ11		36B	DQ14	MEM_B_DQ<0> 15D4
		39B	VSS14		38B	DQ15	MEM_B_DQ<5> 15D4
			KEY		40B	VSS15	
		41B	VSS16		42B	VSS17	
15C4	MEM_B_DQ<21>	43B	DQ16		44B	DQ20	MEM_B_DQ<22> 15C4
15C4	MEM_B_DQ<19>	45B	DQ17		46B	DQ21	MEM_B_DQ<18> 15C4
		47B	VSS18		48B	VSS19	
15C2	MEM_B_DQS_N<2>	49B	DQS2*		50B	NC0	DIMM_OVERTEMP_L 28C3 50D3
15C2	MEM_B_DQS_P<2>	51B	DQS2		52B	DM2	MEM_B_DM<2> 15D2
		53B	VSS21		54B	VSS22	
15C4	MEM_B_DQ<20>	55B	DQ18		56B	DQ22	MEM_B_DQ<17> 15C4
15C4	MEM_B_DQ<23>	57B	DQ19		58B	DQ23	MEM_B_DQ<16> 15C4
		59B	VSS23		60B	VSS24	
15C4	MEM_B_DQ<29>	61B	DQ24		62B	DQ28	MEM_B_DQ<26> 15C4
15C4	MEM_B_DQ<24>	63B	DQ25		64B	DQ29	MEM_B_DQ<28> 15C4
		65B	VSS25		66B	VSS26	
15C2	MEM_B_DM<3>	67B	DM3		68B	DQS3*	MEM_B_DQS_N<3> 15C2
	NC	69B	NC1		70B	DQS3	MEM_B_DQS_P<3> 15C2
		71B	VSS27		72B	VSS28	
15C4	MEM_B_DQ<27>	73B	DQ26		74B	DQ30	MEM_B_DQ<31> 15C4
15C4	MEM_B_DQ<25>	75B	DQ27		76B	DQ31	MEM_B_DQ<30> 15C4
		77B	VSS29		78B	VSS30	
30D6 14C4	MEM_CKE<2>	79B	CKE0		80B	NC/CKE1	MEM_CKE<3> 14C4 30D6
		81B	VDD0		82B	VDD1	
	NC	83B	NC2		84B	NC/A15	MEM_B_A<15> 6D6
30A6 15D2	MEM_B_BS<2>	85B	BA2		86B	NC/A14	MEM_B_A<14> 6D6
		87B	VDD2		88B	VDD3	
30B6 15B2	MEM_B_A<12>	89B	A12		90B	A11	MEM_B_A<11> 15B2 30B6
30B6 15B2	MEM_B_A<9>	91B	A9		92B	A7	MEM_B_A<7> 15B2 30B6
30B6 15B2	MEM_B_A<8>	93B	A8		94B	A6	MEM_B_A<6> 15B2 30B6
		95B	VDD4		96B	VDD5	
30B6 15B2	MEM_B_A<5>	97B	A5		98B	A4	MEM_B_A<4> 15B2 30B6
30B6 15B2	MEM_B_A<3>	99B	A3		100B	A2	MEM_B_A<2> 15C2 30B6
30B6 15C2	MEM_B_A<1>	101B	A1		102B	A0	MEM_B_A<0> 15C2 30B6
		103B	VDD6		104B	VDD7	
30B6 15B2	MEM_B_A<10>	105B	A10/AP		106B	BA1	MEM_B_BS<1> 15D2 30A6
30A6 15D2	MEM_B_BS<0>	107B	BA0		108B	RAS*	MEM_B_RAS_L 15B2 30A6
30A6 15B2	MEM_B_WE_L	109B	WE*		110B	S0*	MEM_CS_L<2> 14C4 30D6
		111B	VDD8		112B	VDD9	
30A6 15D2	MEM_B_CAS_L	113B	CAS*		114B	ODT0	MEM_ODT<2> 14C4 30C6
30D6 14C4	MEM_CS_L<3>	115B	NC/S1*		116B	NC/A13	MEM_B_A<13> 15B2 30B6
		117B	VDD10		118B	VDD11	
30C6 14C4	MEM_ODT<3>	119B	NC/ODT1		120B	NC3	NC
		121B	VSS31		122B	VSS32	
15B4	MEM_B_DQ<36>	123B	DQ32		124B	DQ36	MEM_B_DQ<32> 15C4
15C4	MEM_B_DQ<33>	125B	DQ33		126B	DQ37	MEM_B_DQ<37> 15B4
		127B	VSS33		128B	VSS34	
15C2	MEM_B_DQS_N<4>	129B	DQS4*		130B	DM4	MEM_B_DM<4> 15C2
15C2	MEM_B_DQS_P<4>	131B	DQS4		132B	VSS35	
		133B	VSS36		134B	DQ38	MEM_B_DQ<38> 15B4
15B4	MEM_B_DQ<34>	135B	DQ34		136B	DQ39	MEM_B_DQ<39> 15B4
15B4	MEM_B_DQ<35>	137B	DQ35		138B	VSS37	
		139B	VSS38		140B	DQ44	MEM_B_DQ<44> 15B4
15B4	MEM_B_DQ<40>	141B	DQ40		142B	DQ45	MEM_B_DQ<45> 15B4
15B4	MEM_B_DQ<41>	143B	DQ41		144B	VSS39	
		145B	VSS40		146B	DQS5*	MEM_B_DQS_N<5> 15C2
15C2	MEM_B_DM<5>	147B	DM5		148B	DQS5	MEM_B_DQS_P<5> 15C2
		149B	VSS41		150B	VSS42	
15B4	MEM_B_DQ<42>	151B	DQ42		152B	DQ46	MEM_B_DQ<46> 15B4
15B4	MEM_B_DQ<43>	153B	DQ43		154B	DQ47	MEM_B_DQ<47> 15B4
		155B	VSS43		156B	VSS44	
15A4	MEM_B_DQ<62>	157B	DQ48		158B	DQ52	MEM_B_DQ<58> 15B4
15B4	MEM_B_DQ<59>	159B	DQ49		160B	DQ53	MEM_B_DQ<63> 15A4
		161B	VSS45		162B	VSS46	
	NC	163B	NC_TEST		164B	CK1	MEM_CLK_P<2> 14D4
		165B	VSS47		166B	CK1*	MEM_CLK_N<2> 14D4
15C2	MEM_B_DQS_N<7>	167B	DQS6*		168B	VSS48	
15C2	MEM_B_DQS_P<7>	169B	DQS6		170B	DM6	MEM_B_DM<7> 15C2
		171B	VSS49		172B	VSS50	
15A4	MEM_B_DQ<60>	173B	DQ50		174B	DQ54	MEM_B_DQ<56> 15B4
15A4	MEM_B_DQ<61>	175B	DQ51		176B	DQ55	MEM_B_DQ<57> 15B4
		177B	VSS51		178B	VSS52	
15B4	MEM_B_DQ<54>	179B	DQ56		180B	DQ60	MEM_B_DQ<55> 15B4
15B4	MEM_B_DQ<51>	181B	DQ57		182B	DQ61	MEM_B_DQ<50> 15B4
		183B	VSS53		184B	VSS54	
15C2	MEM_B_DM<6>	185B	DM7		186B	DQS7*	MEM_B_DQS_N<6> 15C2
		187B	VSS55		188B	DQS7	MEM_B_DQS_P<6> 15C2
15B4	MEM_B_DQ<52>	189B	DQ58		190B	VSS56	
15B4	MEM_B_DQ<49>	191B	DQ59		192B	DQ62	MEM_B_DQ<53> 15B4
65A3 29A3 28A6	=PPSPD_S0_MEM	193B	VSS57		194B	DQ63	MEM_B_DQ<48> 15B4
27C6	=I2C_SODIMMB_SDA	195B	SDA		196B	VSS58	Resistor prevents pwr-gnd short
27C6	=I2C_SODIMMB_SCL	197B	SCL		198B	SA0	
		199B	VDDSPD		200B	SA1	SODIMM_A_SA1
			516-0140		202	NC	ADDR=0xA4(WR)/0xA5(RD)

=PPSPD_S0_MEM 28A6 29A6 65A3

R2900 10K 5% 1/16W MF-LF 402

DDR2 Bypass Caps

(For return current)

65B6 29D6 29D3 28D6 28D3 28B2 =PP1V8_S3_MEM

C2908	10UF	20%	5.3V XSR 603
C2909	10UF	20%	5.3V XSR 603
C2910	1UF	10%	6.3V CERM 402
C2911	0.1uF	20%	10V CERM 402
C2912	1UF	10%	6.3V CERM 402
C2913	1UF	10%	6.3V CERM 402
C2914	1UF	10%	6.3V CERM 402
C2915	1UF	10%	6.3V CERM 402
C2916	1UF	10%	6.3V CERM 402
C2917	0.1uF	20%	10V CERM 402
C2918	0.1uF	20%	10V CERM 402
C2919	0.1uF	20%	10V CERM 402
C2920	0.1uF	20%	10V CERM 402
C2921	0.1uF	20%	10V CERM 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

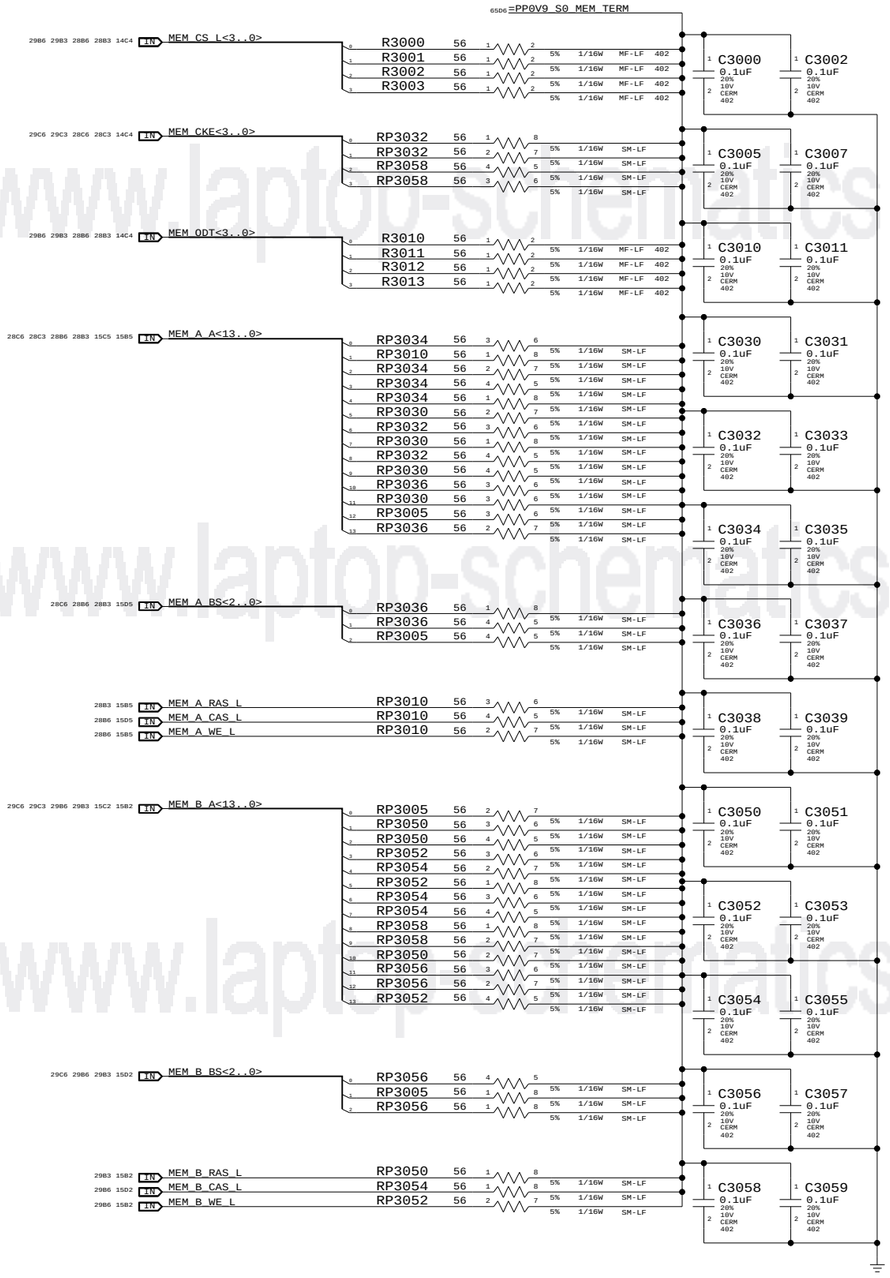
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE	SHT	OF
NONE	29	105

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7270	B
	SCALE NONE	SHT 30 OF 105	

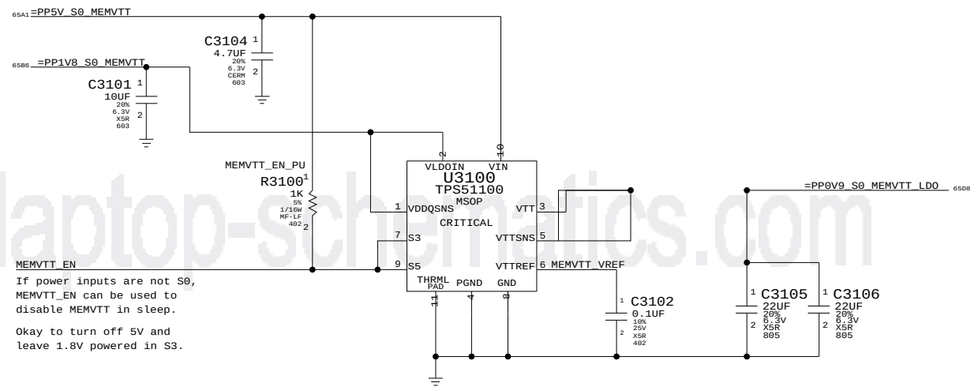
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



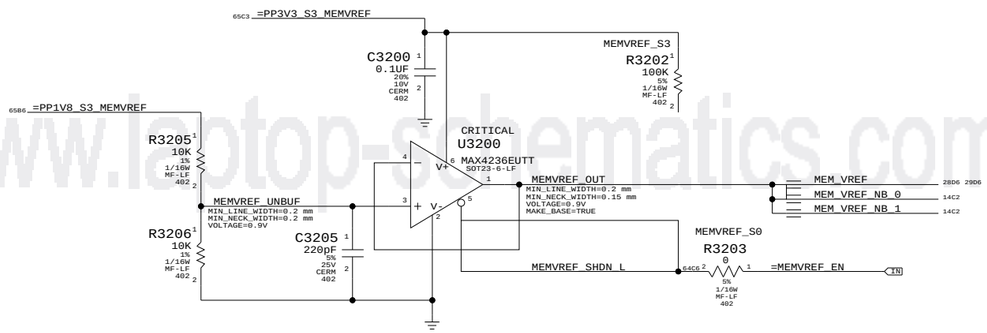
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE	SHT	OF
NONE	31	105



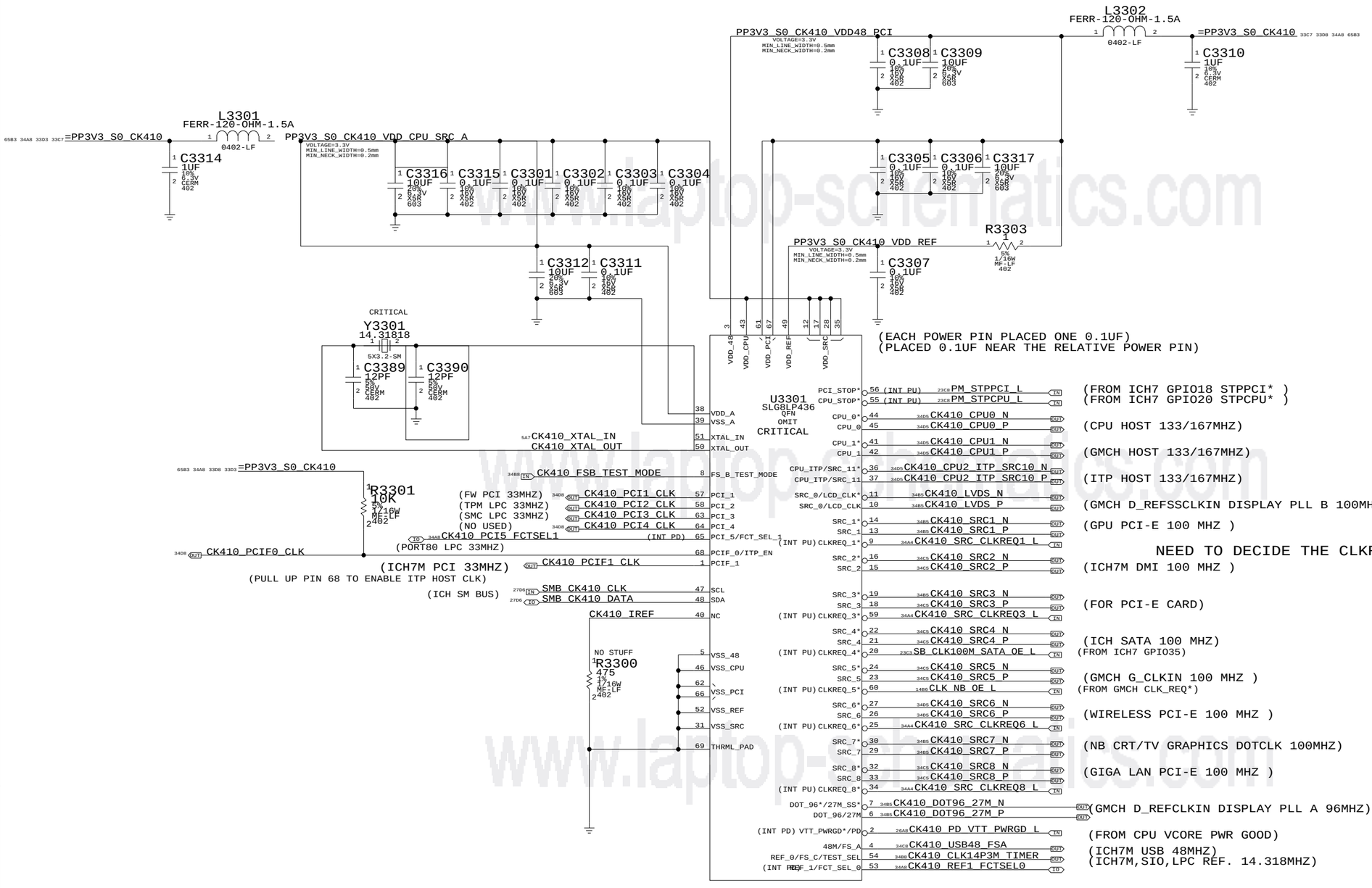
DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE	SHT	OF
NONE	32	105



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

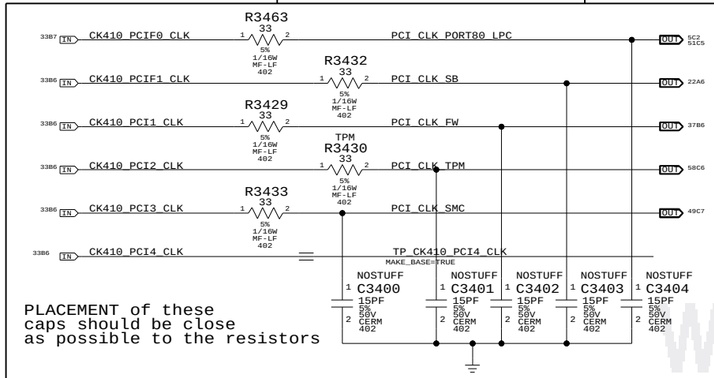
CLOCKS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

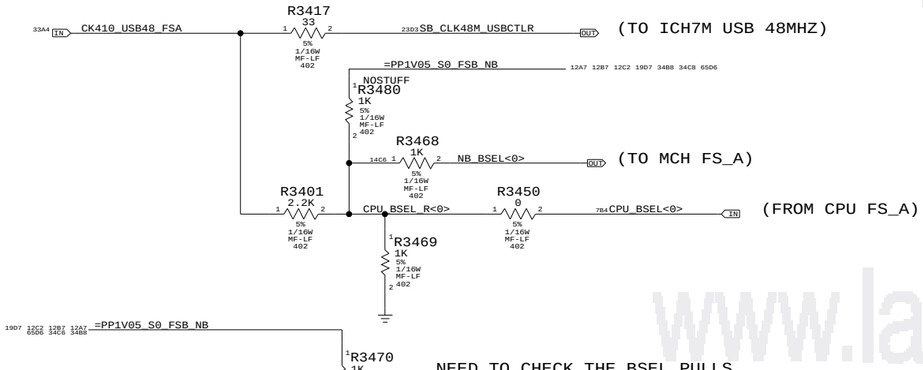
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE NONE SHT 33 OF 105



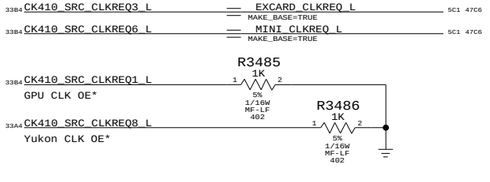
PLACEMENT of these caps should be close as possible to the resistors



NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

FS_C	FS_B	FS_A	CPU
0	0	0	266M
# 0	0	1	133M
# 0	1	0	166M
0	1	1	200M
1	0	0	100M
1	0	1	333M
1	1	0	400M
1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED



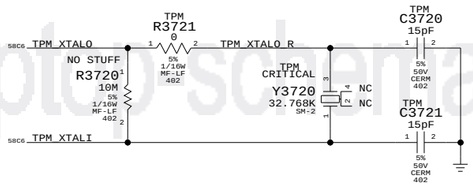
Clock Termination

SYNC_MASTER=M59_MG SYNC_DATE=05/07/2006

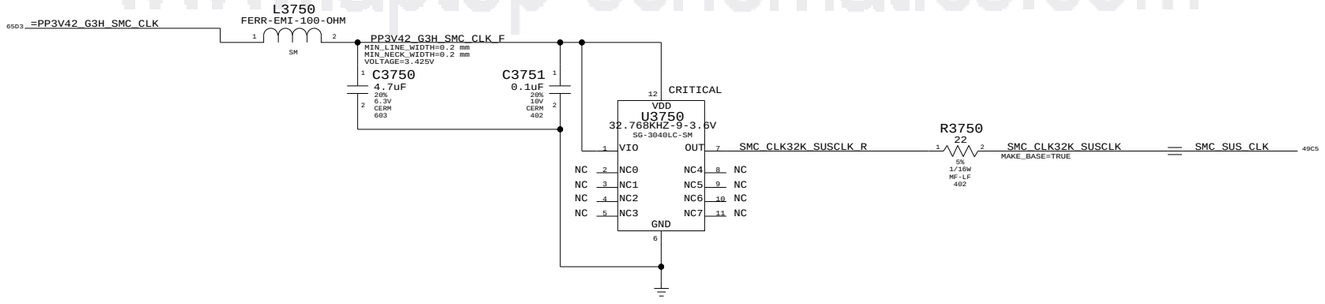
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 34 OF 105	

TPM Crystal Circuit



SMC G3Hot Oscillator



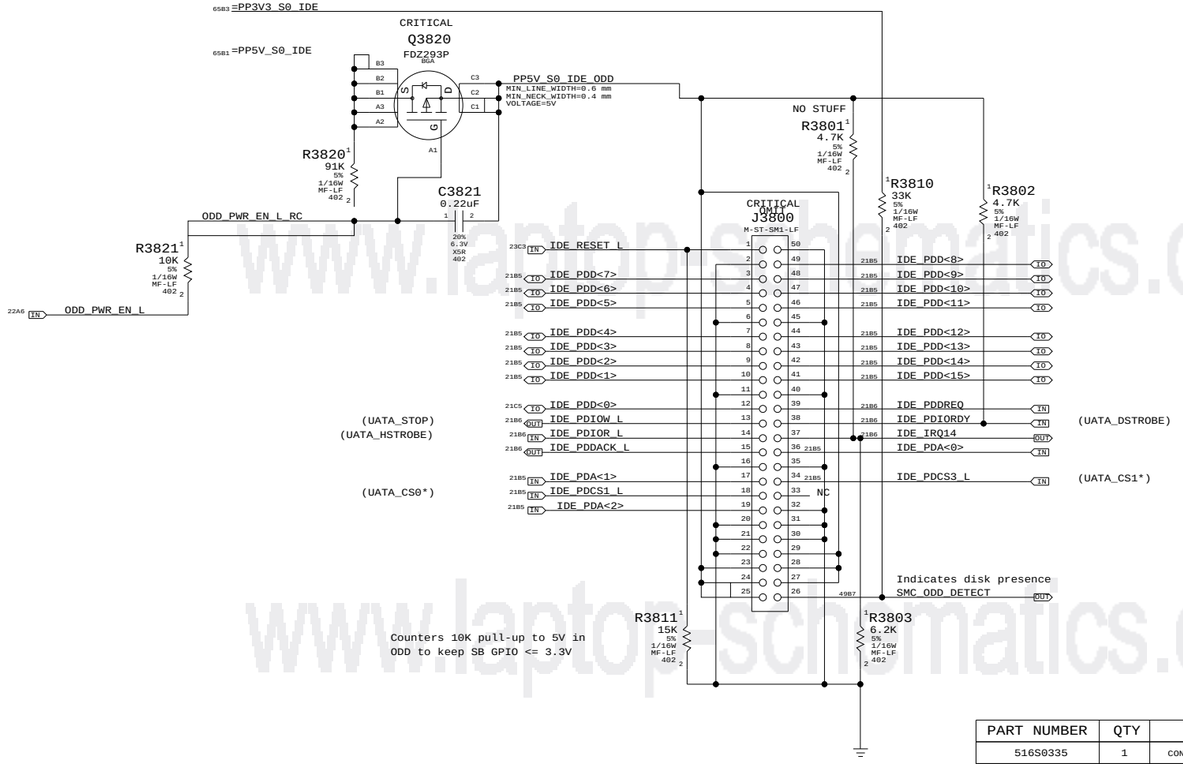
Mobile Clocking

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

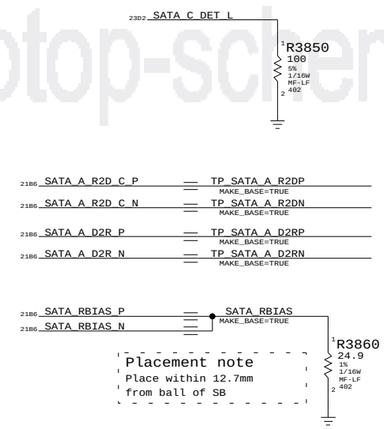
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 37 OF 105	

IDE (ODD) Connector



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
516S0335	1	CONN,PLUG,0.5MM PITCH,1.5MM STK,50P	J3800	CRITICAL	ODD_NONLOCK_CONN
516S0557	1	CONN,PLUG,0.5MM PITCH,1.5MM STK,50P,LOCK	J3800	CRITICAL	ODD_LOCK_CONN

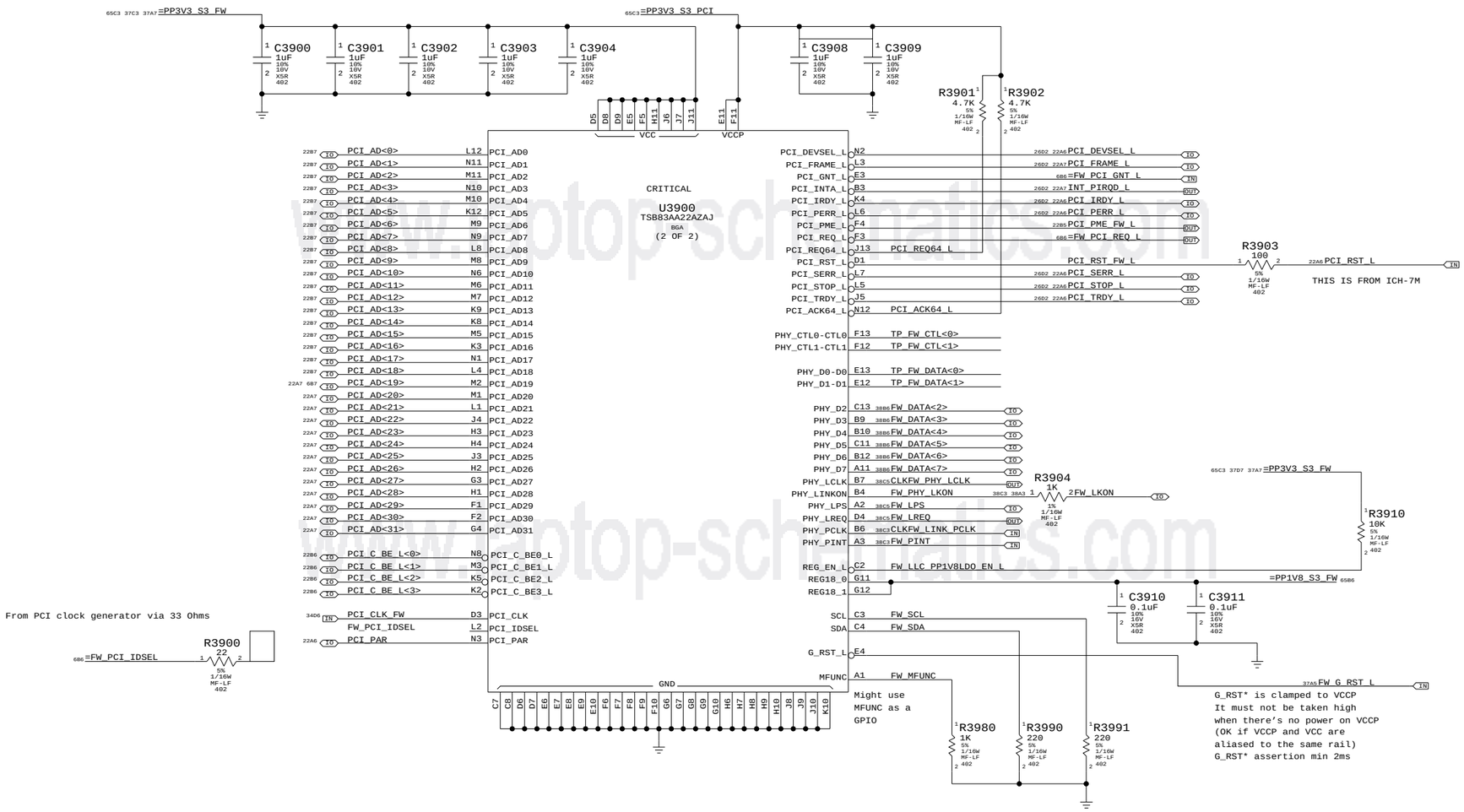


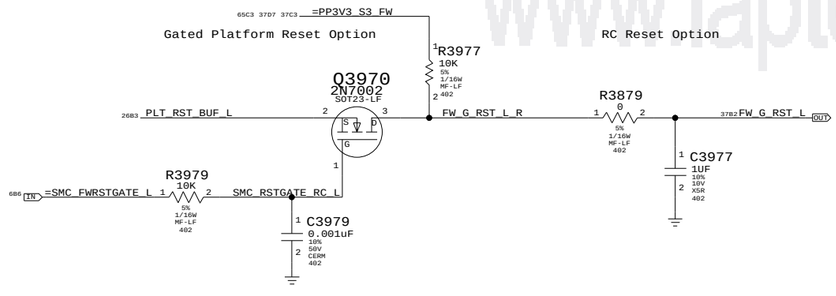
PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 38 OF 105	



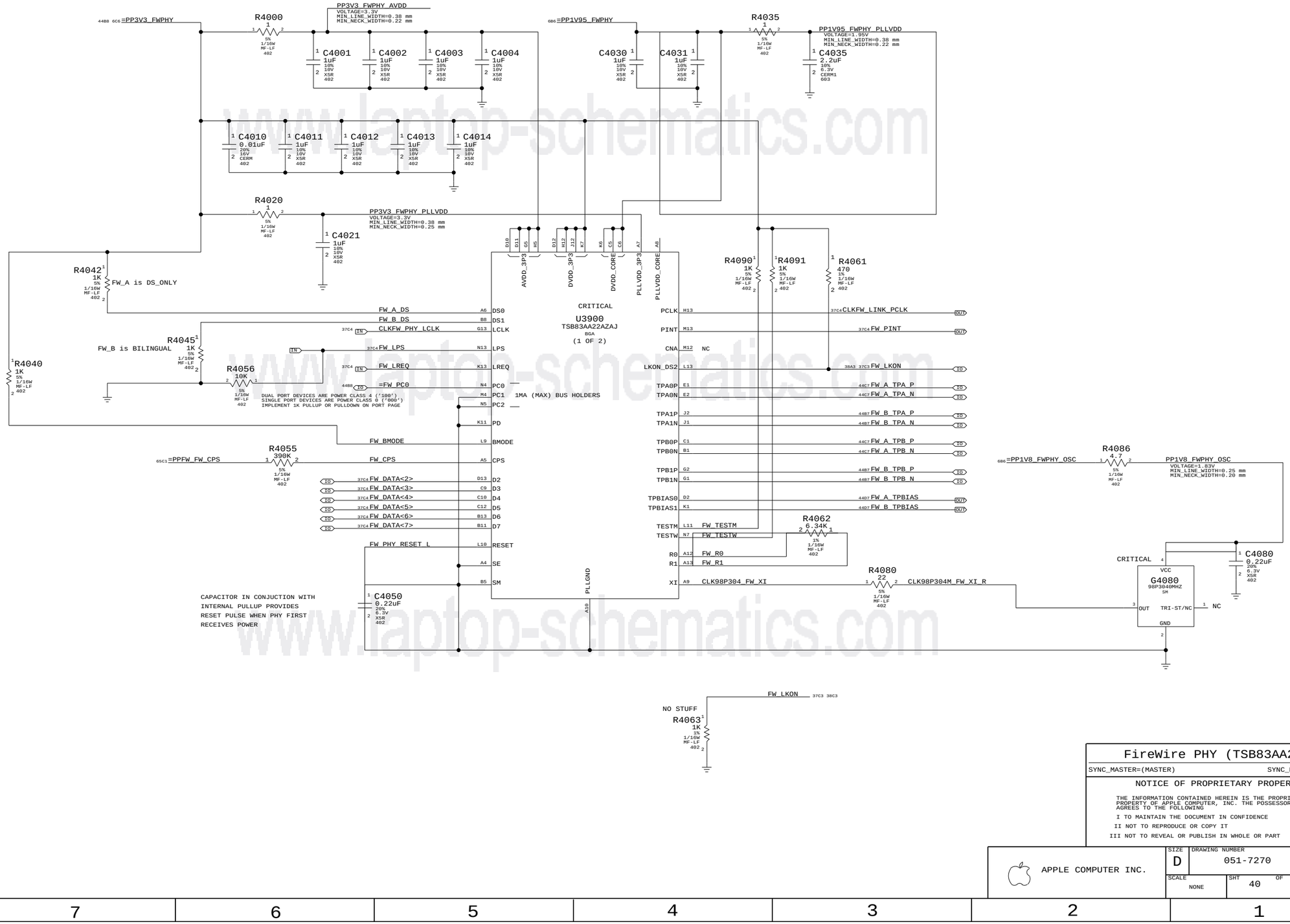


FireWire Link (TSB83AA22)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 39 OF 105	


=PP3V3_FWPHY
R4000
PP3V3_FWPHY_AVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.22 mm
C4001 1uF
C4002 1uF
C4003 1uF
C4004 1uF
=PP1V95_FWPHY
R4035
PP1V95_FWPHY_PLLVDD
VOLTAGE=1.95V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.22 mm
C4030 1uF
C4031 1uF
C4035 2.2uF
C4010 0.01uF
C4011 1uF
C4012 1uF
C4013 1uF
C4014 1uF
R4020
PP3V3_FWPHY_PLLVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
C4021 1uF
R4042 1K
FW_A is DS_ONLY
R4040 1K
R4045 1K
FW_B is BILINGUAL
R4056 10K
DUAL PORT DEVICES ARE POWER CLASS 4 ('100')
SINGLE PORT DEVICES ARE POWER CLASS 0 ('000')
IMPLEMENT 1K PULLUP OR PULLDOWN ON PORT PAGE
AVDD_3P3
DVDD_3P3
DVDD_CORE
PLLVDD_3P3
PLLVDD_CORE
R4090 1K
R4091 1K
R4061 470
CRITICAL
U3900
TSB83AA22AZAJ
BGA
(1 OF 2)
FW_A_DS
FW_B_DS
CLKFW_PHY_LCLK
FW_LPS
FW_LREQ
=FW_PC0
1MA (MAX) BUS HOLDERS
FW_BMODE
R4055 390K
=PPFW_FW_CPS
FW_CPS
FW_DATA<2>
FW_DATA<3>
FW_DATA<4>
FW_DATA<5>
FW_DATA<6>
FW_DATA<7>
FW_PHY_RESET_L
CAPACITOR IN CONJUCTION WITH
INTERNAL PULLUP PROVIDES
RESET PULSE WHEN PHY FIRST
RECEIVES POWER
C4050 0.22uF
PLLGND
PCLK
PINT
CNA NC
LKON_DS2
TPA0P
TPA0N
TPA1P
TPA1N
TPB0P
TPB0N
TPB1P
TPB1N
TPBIAS0
TPBIAS1
TESTM
TESTW
R0
R1
XI
CLKFW_LINK_PCLK
FW_PINT
FW_LKON
FW_A_TPA_P
FW_A_TPA_N
FW_B_TPA_P
FW_B_TPA_N
FW_A_TPB_P
FW_A_TPB_N
FW_B_TPB_P
FW_B_TPB_N
FW_A_TPBIAS
FW_B_TPBIAS
FW_TESTM
FW_TESTW
R4062 6.34K
FW_R0
FW_R1
R4080 22
CLK98P304_FW_XI
CLK98P304M_FW_XI_R
=PP1V8_FWPHY_OSC
R4086 4.7
PP1V8_FWPHY_OSC
VOLTAGE=1.83V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.20 mm
CRITICAL
G4080
98P3040MHZ
C4080 0.22uF
NO STUFF
R4063 1K
FW_LKON
FireWire PHY (TSB83AA22)
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7270
REV. B
SCALE NONE
SHT 40 OF 105

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

39D5 PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402-LF

=PP2V5_S3_ENET 65B6

PLACE C4107 NEAR U4101 AVDD

=PP3V3_S3_ENET 39D5 39A3 39B4 39B8 65D1
=PP1V2_S3_ENET 39A8 65D6
=PP3V3_S3_ENET 39D8 65D1 39A5 39B4 39B5 39B8

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402

PCIE_A_D2R_C_P 22D4 PCIE_A_D2R_P OUT
PCIE_A_D2R_C_N 22D4 PCIE_A_D2R_N OUT

C4112 0.1UF X5R 10% 16V 402
C4113 0.1UF 402 X5R 16V 10%

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

PCIE_A_R2D_P 22D4 PCIE_A_R2D_C_P IN
PCIE_A_R2D_N 22D4 PCIE_A_R2D_C_N IN

OMIT
CRITICAL
U4101
88E8053
QFN

VDD7	58		
VDD6	48		
VDD5	44		
VDD4	39		
VDD3	33		
VDD2	13		
VDD1	7		
VDD0	2		
VDDO_TTL4	61		
VDDO_TTL3	46		
VDDO_TTL2	40		
VDDO_TTL1	8		
VDDO_TTL0	1		
AVDD	23		
AVDDL6	57		
AVDDL5	52		
AVDDL4	51		
AVDDL3	32		
AVDDL2	28		
AVDDL1	22		
AVDDL0	19		
VDD25	64		
		TX_P	49
		TX_N	50
		RX_P	54
		RX_N	53
		REFCLKP	55
		REFCLKN	56
		WAKE*	6
		PERST*	5
		MDIP0	17
		MDIN0	18
		MDIP1	20
		MDIN1	21
		MDIP2	26
		MDIN2	27
		MDIP3	30
		MDIN3	31
		VPD_CLK	38
		VPD_DATA	41
		PU_VDDO_TTL0	42
		PU_VDDO_TTL1	43
		SPI_DI	35
		SPI_DO	34
		SPI_CLK	37
		SPI_CS	36
		XTALI	15
		XTALO	14
THRML_PAD	0		

PCI EXPRESS
ANALOG
MEDIA
LED
TEST
TWSI
SPI
MAIN CLK

39B7 ENET_LOM_DIS_L → LOM_DISABLE* 10
VAUX_AVLBL 12
64C6 =ENET_VMAIN_AVLBL → VMAIN_AVLBL 47
NC SWITCH_VCC 11
NC SWITCH_VAUX 9
NC HSDACP 24
NC HSDACN 25
OPTIONAL EXTERNAL LDO
6D4 ENET_CTRL25 → CTRL25 4
6D4 ENET_CTRL12 → CTRL12 3
ENET_RSET → RSET 16
R4102 4.87K 1% 1/16W MF-LF 402
NO PULL-UP NEEDED
NC LED_ACT* 59
NC LED_LINK10/100* 60
NC LED_LINK1000* 62
NC LINK* 63
TSTPT 29
TESTMODE 46

34C3 ENET_CLK100M_PCIE_P IN
34C3 ENET_CLK100M_PCIE_N IN
47C3 23C8 5B1 PCIE_WAKE_L OUT
26B1 ENET_RST_L IN

40D4 ENET_MDI_P<0> IO
40C4 40B7 ENET_MDI_N<0> IO
40C4 ENET_MDI_P<1> IO
40C4 40A7 ENET_MDI_N<1> IO
40C4 ENET_MDI_P<2> IO
40C4 ENET_MDI_N<2> IO
40C4 ENET_MDI_P<3> IO
40B4 ENET_MDI_N<3> IO

ENET_VPD_CLK 39A2
ENET_VPD_DATA 39A2
ENET_PU_VDD_TTL0 39A6
ENET_PU_VDD_TTL1 39A6

ASF IS UNAVAILABLE ON 80S3

INTERNAL PULL-UP

CRITICAL
ENET_XTALI
Y4101 SM-3.2X2.5MM 25.0000M
C4150 27pF 5% 50V CERM 402
C4151 27pF 5% 50V CERM 402

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

R4106 49.9 1% 1/16W MF-LF 402
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402
R4117 49.9 1% 1/16W MF-LF 402

ENET_MDI0 VOLTAGE=1.234V
ENET_MDI1 VOLTAGE=1.234V
ENET_MDI2 VOLTAGE=1.234V
ENET_MDI3 VOLTAGE=1.234V

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

Setting attribute VOLTAGE
to arbitrary value
to help constraint manager
find correct topolgy

PLACE RESISTORS CLOSE TO U4101

65D1 39D8 39D6 39B5 39B4 39A5 =PP3V3_S3_ENET
R4101 4.7K 5% 1/16W MF-LF 402
ENET_LOM_DIS_L 39C8
Q4100 2N7002 SOT23-LF
6C4 ENET_LOWPWR_EN
R4132 100K 5% 1/16W MF-LF 402

=PP3V3_S3_ENET 39A5 39B4 39B8 39D6 39D8 65D1
R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402
39C6 ENET_PU_VDD_TTL0
39B6 ENET_PU_VDD_TTL1

65D1 39D8 39D6 39B8 39B5 39A5 =PP3V3_S3_ENET
PLACE C4140 NEAR U4102 VCC
C4140 0.1UF 10% 16V X5R 402
OMIT
CRITICAL
U4102 M24C08 SO8
VCC
E2
NC1
NC0
WC*
SDA
SCL
VSS
R4122 10K 5% 1/16W MF-LF 402
R4123 10K 5% 1/16W MF-LF 402
ENET_VPD_DATA 39C6
ENET_VPD_CLK 39C6

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

65D6 39D7 =PP1V2_S3_ENET
C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

65D1 39D8 39D6 39B8 39B5 39B4 =PP3V3_S3_ENET
C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 41 OF 105	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0> 40D3
	ENETCONN	ENET_100D	ENETCONN_N<0> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<1> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<1> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<2> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<2> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<3> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<3> 40B3

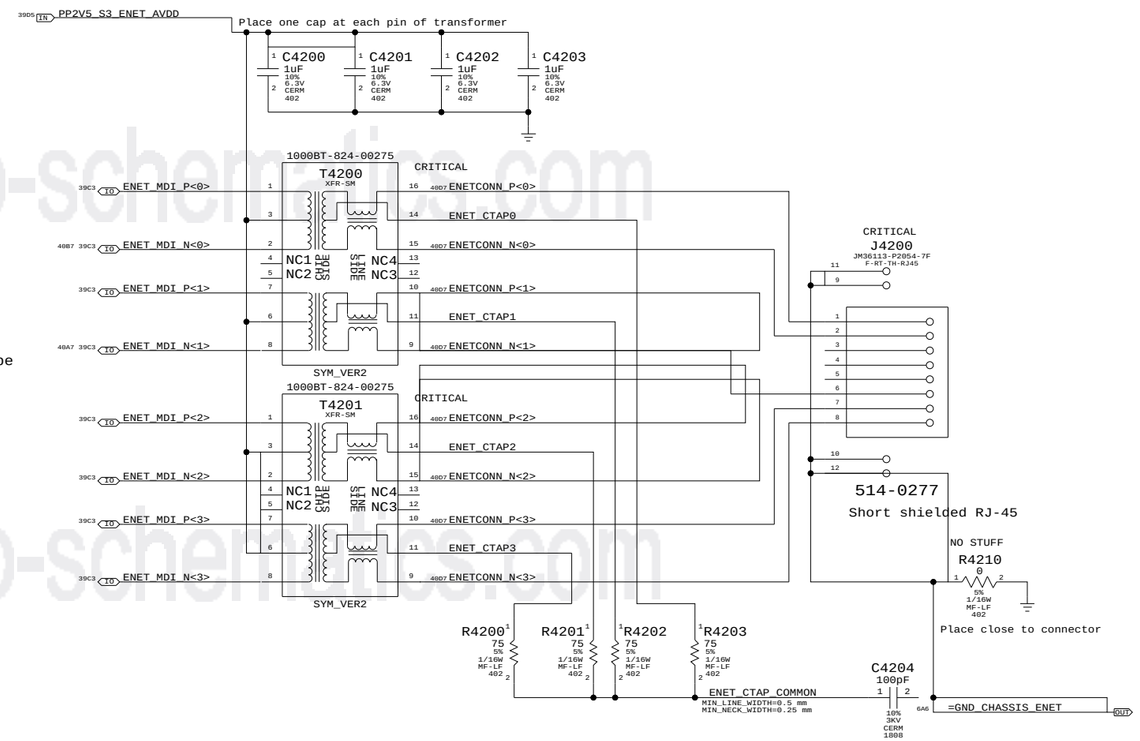
Page Notes

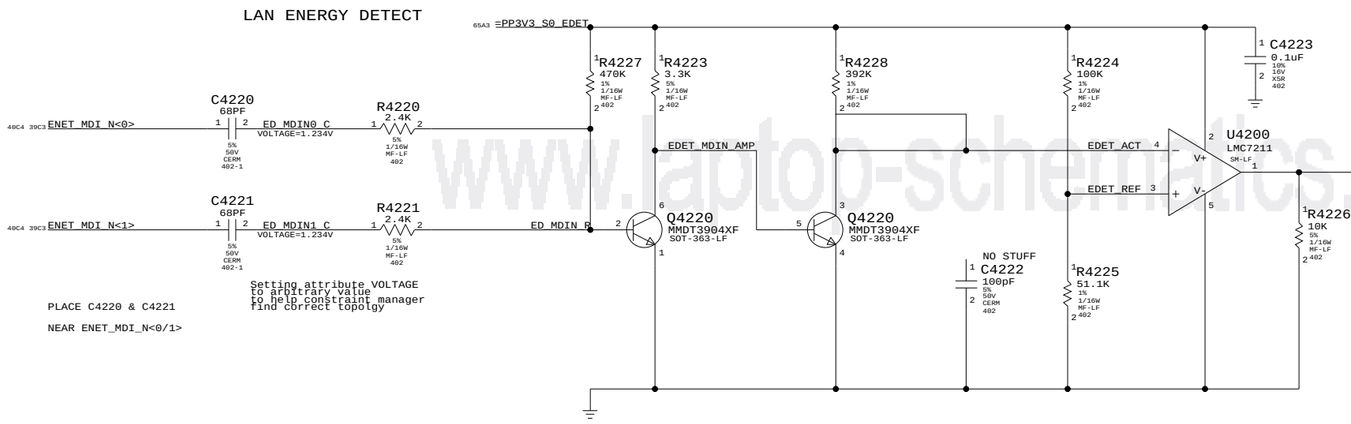
Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board





Ethernet Connector

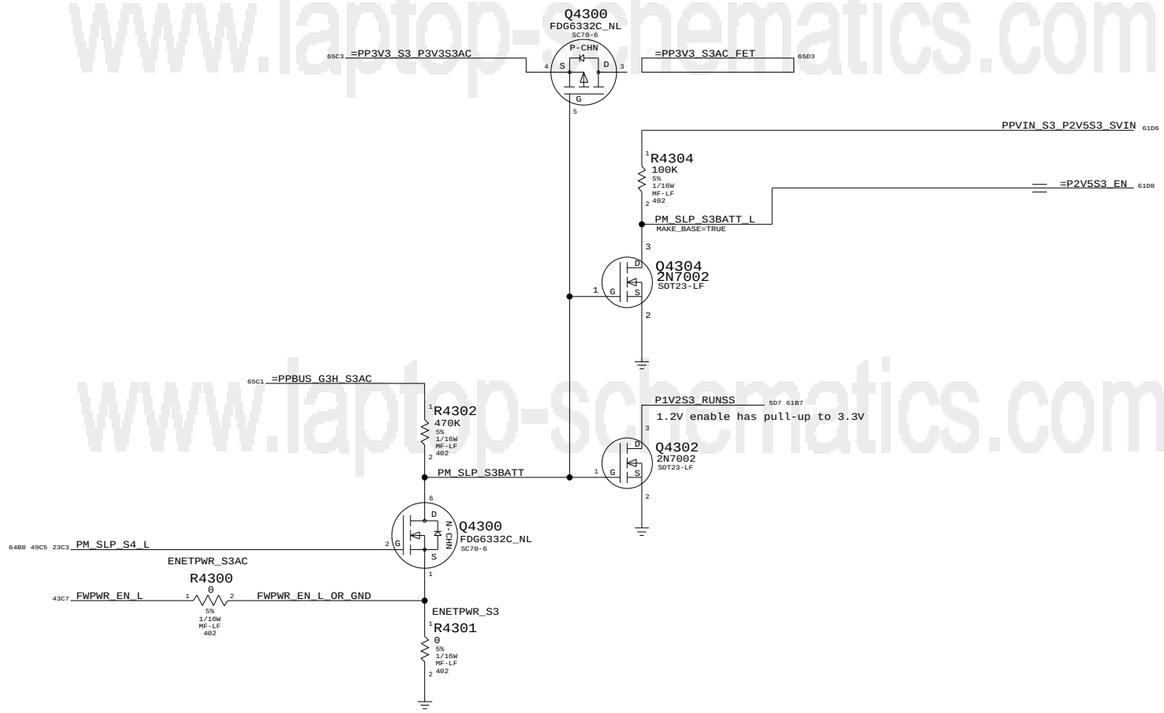
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 42 OF 105	

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

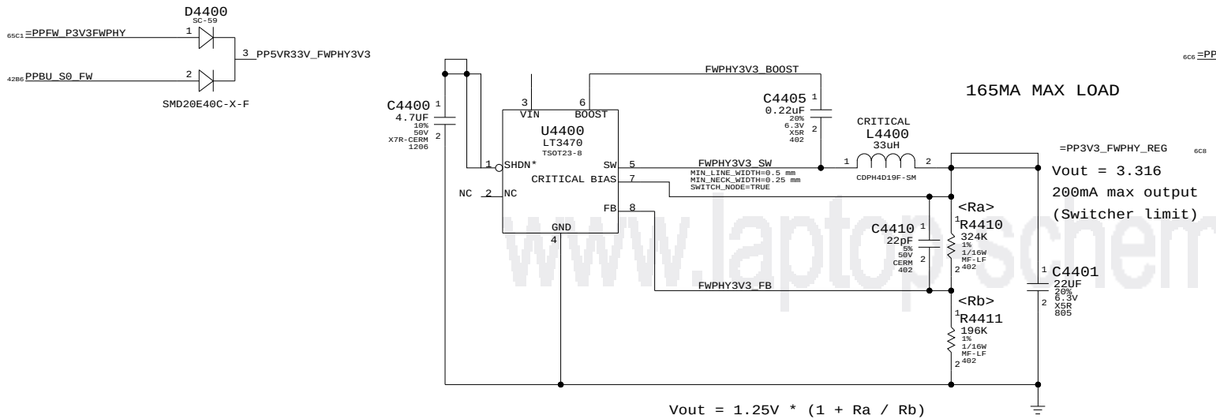
Yukon Power Control

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

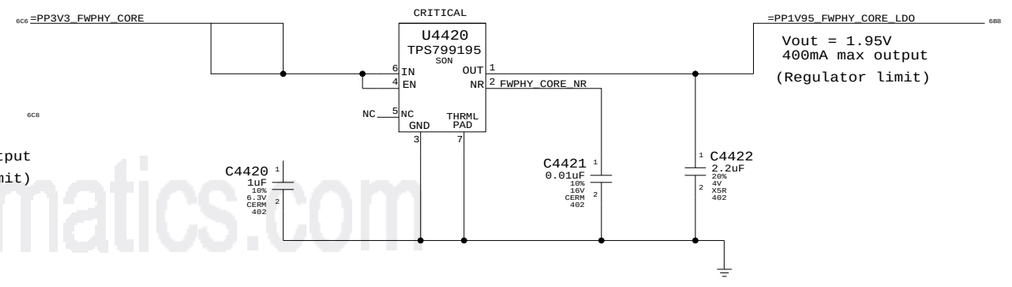
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 43 OF 105	

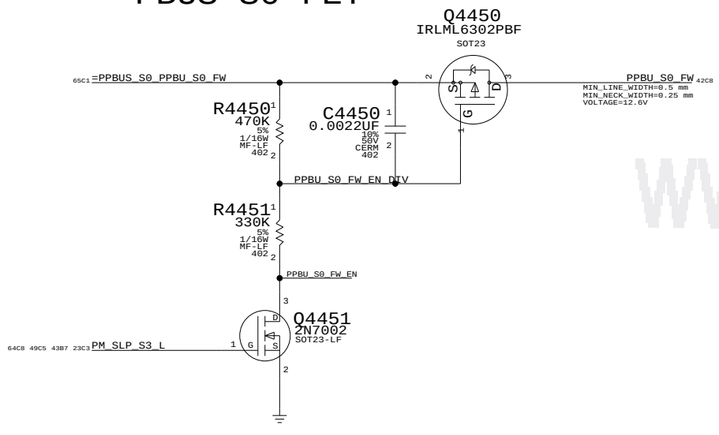
3.3V Supply for FWPHY



1.95V Supply for FW PHY



PBUS S0 FET



FW PHY Power Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE	SHT	OF
NONE	44	105

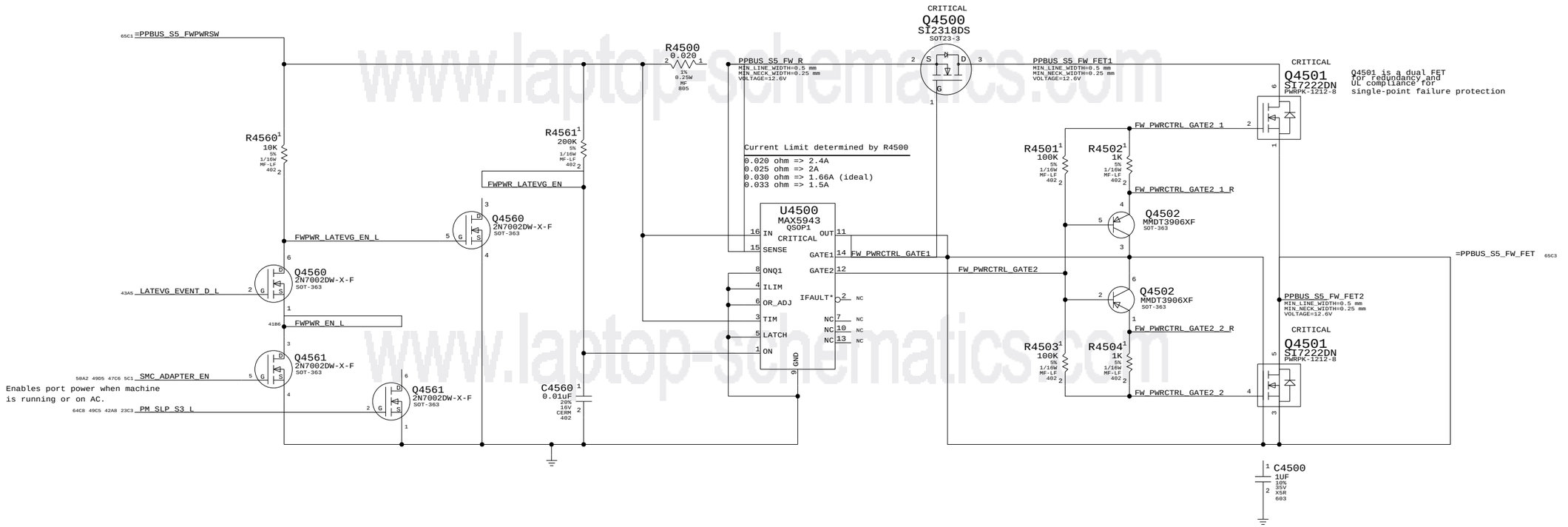
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

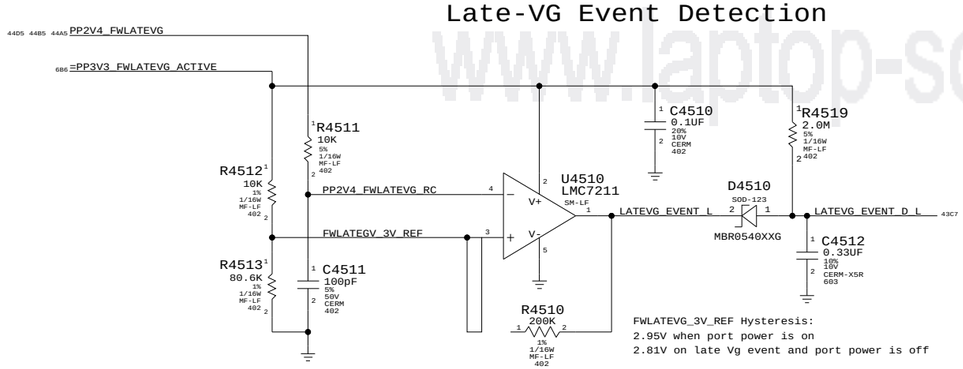
Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Current Limit/Active Late-VG Protection



Late-VG Event Detection



FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 45 OF 105	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
PROVIDED	FW	FW_110D	FW_PORT1_TPA_P	44B5 44C5
	FW	FW_110D	FW_PORT1_TPA_N	44B5 44C5
BY	FW	FW_110D	FW_PORT1_TPB_P	44B5 44C5
	FW	FW_110D	FW_PORT1_TPB_N	44B5 44C5
PHY	FW	FW_110D	FW_PORT2_TPA_FL_P	44B2
	FW	FW_110D	FW_PORT2_TPA_FL_N	44B2
PAGE	FW	FW_110D	FW_PORT2_TPB_FL_P	44B2
	FW	FW_110D	FW_PORT2_TPB_FL_N	44B2

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

Place close to FireWire PHY

38B3 FW_B_TPBIAS
38B3 FW_A_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4650 1uF 10% 6.3V CERM 402
C4660 1uF 10% 6.3V CERM 402

Setting attribute VOLTAGE to arbitrary value to help constraint manager find correct topolgy

VOLTAGE=1.234V

OMIT L4660 0 5% 1/16W MF-LF 402
OMIT L4661 0 5% 1/16W MF-LF 402

FW_B_TPA_L_P VOLTAGE=1.234V
FW_B_TPA_L_N VOLTAGE=1.234V

R4650 56.2 1% 1/16W MF-LF 402
R4651 56.2 1% 1/16W MF-LF 402
R4660 56.2 1% 1/16W MF-LF 402
R4661 56.2 1% 1/16W MF-LF 402

38B3 FW_A_TPA_P — FW_PORT2_TPA_P MAKE_BASE=TRUE 44B4
38B3 FW_A_TPA_N — FW_PORT2_TPA_N MAKE_BASE=TRUE 44B4
38B3 FW_A_TPB_P — FW_PORT2_TPB_P MAKE_BASE=TRUE 44B4
38B3 FW_A_TPB_N — FW_PORT2_TPB_N MAKE_BASE=TRUE 44B4
38B3 FW_B_TPA_P — FW_PORT1_TPA_P MAKE_BASE=TRUE 44C5 44D7
38B3 FW_B_TPA_N — FW_PORT1_TPA_N MAKE_BASE=TRUE 44C5 44D7
38B3 FW_B_TPB_P — FW_PORT1_TPB_P MAKE_BASE=TRUE 44C5 44D7
38B3 FW_B_TPB_N — FW_PORT1_TPB_N MAKE_BASE=TRUE 44C5 44D7 44D5 44A5 43B7

38D7 6C6 =PP3V3_FWPHY

38B5 =FW_PC0 — FW_PC0

R4652 56.2 1% 1/16W MF-LF 402
R4653 56.2 1% 1/16W MF-LF 402
R4662 56.2 1% 1/16W MF-LF 402
R4663 56.2 1% 1/16W MF-LF 402

FW_B_TPB_L_N VOLTAGE=1.234V
FW_B_TPB_L_P VOLTAGE=1.234V

OMIT L4662 0 5% 1/16W MF-LF 402
OMIT L4663 0 5% 1/16W MF-LF 402

FW_PORT2_TPB_C VOLTAGE=1.234V
FW_PORT1_TPB_C VOLTAGE=1.234V

C4654 220pF 5% 25V CERM 402
C4664 220pF 5% 25V CERM 402

R4654 4.99K 1% 1/16W MF-LF 402
R4664 4.99K 1% 1/16W MF-LF 402

Note: The peaking inductors were changed to resistors to allow placement in an area restricted by DFM rules for only Rs and Cs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S0414	4	IND,18nH-15mA,0402	L4660,L4661,L4662,L4663	CRITICAL	

Late-VG Protection Power

6C6 =PP3V3_FWLATEVG

R4690 332 1% 1/16W MF-LF 402

PP2V4_FWLATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V 43B7 44B5 44D5

C4691 0.01UF 10% 50V X7R 402

CRITICAL D4690 MMBZ5227B SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4690 should be 390 Ohms max for a 3.3V rail

"Snapback" & "Late VG" Protection

44B5 44A5 43B7 PP2V4_FWLATEVG

DP4620 BAV99DW-X-F SOT-363
DP4621 BAV99DW-X-F SOT-363

C4620 0.01uF 10% 50V X7R 402
C4621 0.01uF 10% 50V X7R 402
C4622 0.01uF 10% 50V X7R 402
C4623 0.01uF 10% 50V X7R 402

44D7 44B5 FW_PORT1_TPB_N
44D7 44B5 FW_PORT1_TPB_P
44D7 44B5 FW_PORT1_TPA_N
44D7 44B5 FW_PORT1_TPA_P

Cable Power

65C1 =PPFW_PORT1_VP

L4620 FERR-250-OHM SM

C4624 0.001uF 20% 50V CERM 402

PPFW_PORT1_VP MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

Note:Trace PPFW_PORT1_VP should handle up to 5A

PORT 1 BILINGUAL

CRITICAL J4620 1394B-UG31903 F-RT-SM1

(FW_PORT1_BREF)
(PPFW_PORT1_VP)
(GND_FW_PORT1_VG)
FW_PORT1_AREF

TPB- TPB<R> TPB+ VP NC VG TPA- TPA<R> TPA+ — OUTPUT / INPUT

514S0133

C4629 0.1uF 10% 50V X7R 603-1
Place C4629 close to pin 5 of connector
R4629 1M 5% 1/16W MF-LF 402

C4625 0.01uF 20% 50V CERM 603
NO STUFF C4627 0.01uF 20% 16V CERM 402
C4626 0.01uF 20% 16V CERM 402

=GND_CHASSIS_FW_PORT1 6A6

"Snapback" & "Late VG" Protection

44C5 FW_PORT2_TPA_P
44C5 FW_PORT2_TPA_N
44C5 FW_PORT2_TPB_P
44C5 FW_PORT2_TPB_N

DP4630 BAV99DW-X-F SOT-363
DP4631 BAV99DW-X-F SOT-363

C4630 0.01uF 10% 50V X7R 402
C4631 0.01uF 10% 50V X7R 402
C4632 0.01uF 10% 50V X7R 402
C4633 0.01uF 10% 50V X7R 402

FL4630 1210-45R1 90-OHM-100MA CRITICAL
FL4631 1210-45R1 90-OHM-100MA CRITICAL

44D7 FW_PORT2_TPA_FL_P
44D7 FW_PORT2_TPA_FL_N
44D7 FW_PORT2_TPB_FL_P
44D7 FW_PORT2_TPB_FL_N

Cable Power

65C1 =PPFW_PORT2_VP

L4630 FERR-250-OHM SM

C4634 0.001uF 20% 50V CERM 402

PPFW_PORT2_VP MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

PORT 2 1394A

CRITICAL J4630 1394A F-RT-TH-LF

(PPFW_PORT2_VP)
(GND_FW_PORT2_VG)

TPO (TPA+) TPO# (TPA-) TPI (TPB+) TPI# (TPB-) VP VGND

514-0255

C4635 0.01uF 20% 50V CERM 603
C4636 0.01uF 20% 16V CERM 402

=GND_CHASSIS_FW_PORT2L 6B6
=GND_CHASSIS_FW_PORT2U 6A6

R4699 0 5% 1/16W MF-LF 402 =GND_CHASSIS_FW_EMI_R 6B6

FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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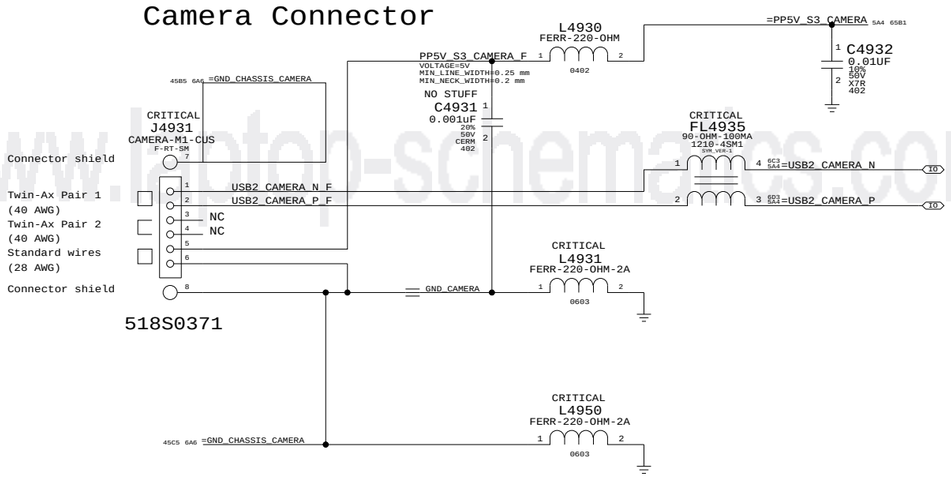
SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 46 OF 105	

Camera Connector



Camera Connector

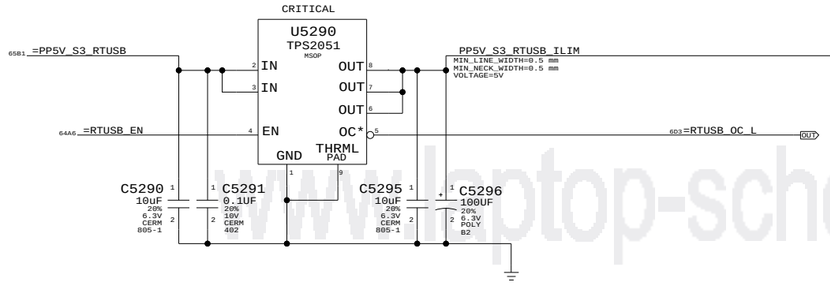
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

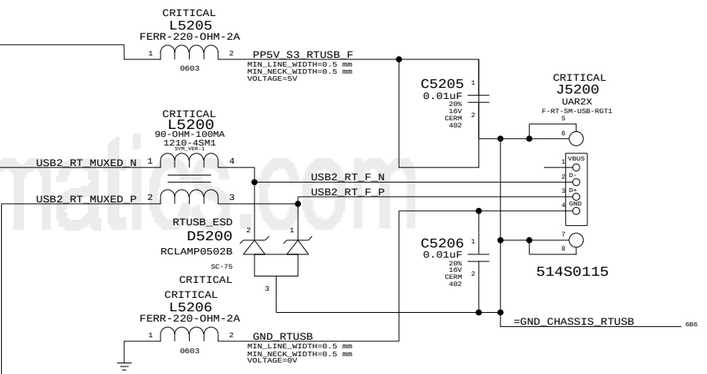
SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE	SHT	OF
NONE	49	105

Port Power Switch

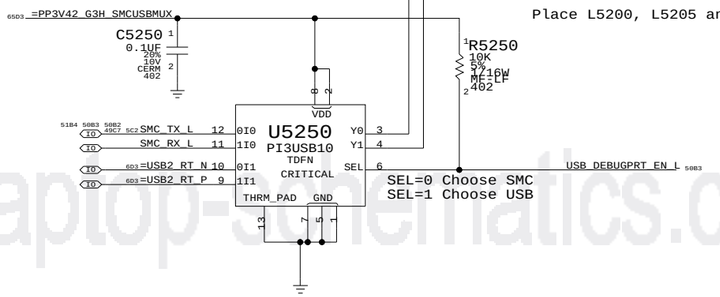


Right USB Port



Place L5200, L5205 and L5206 across moat

USB/SMC Debug Mux



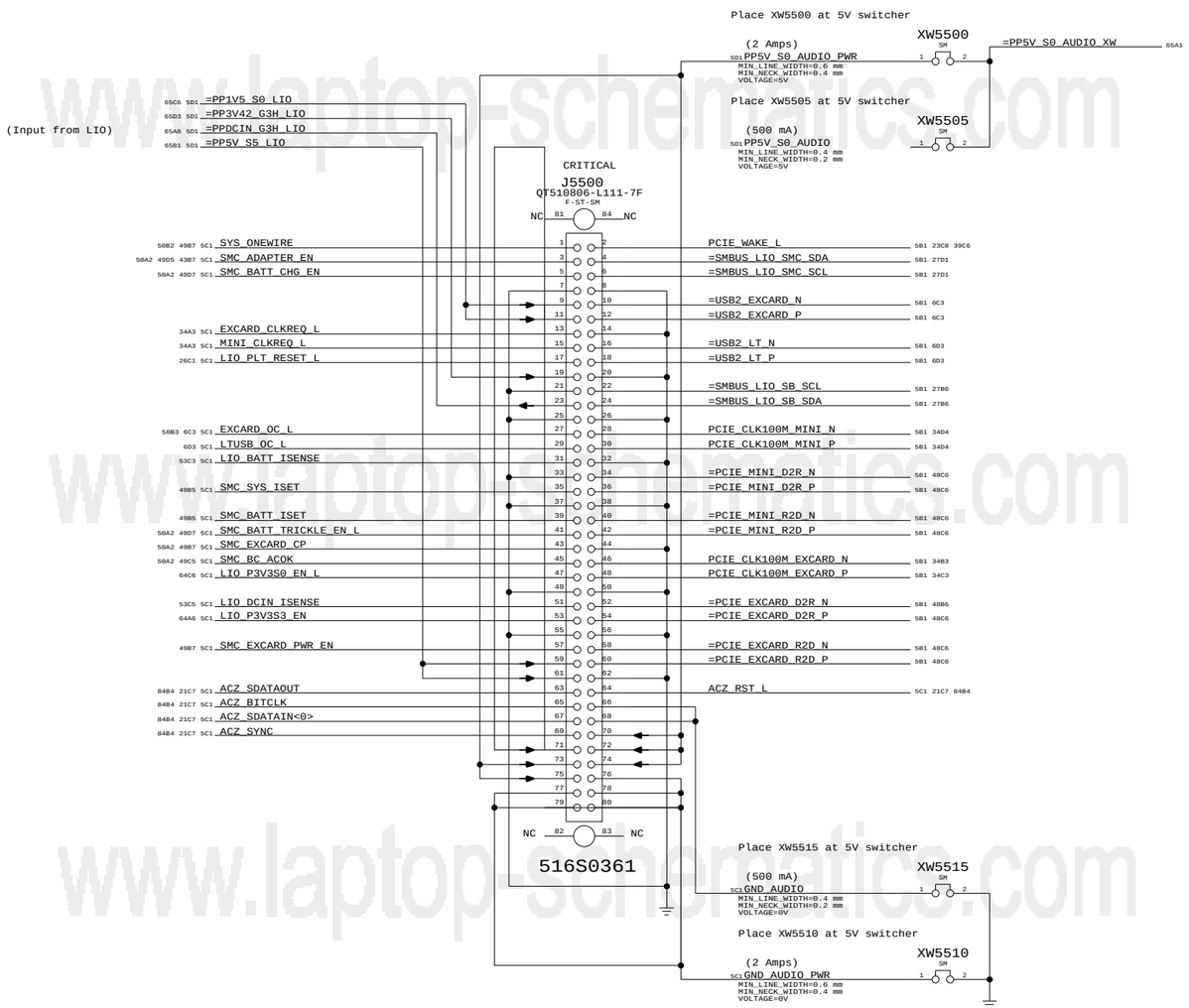
External USB Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 52 OF 105	

Left I/O Board Connector



Left I/O Board Connector

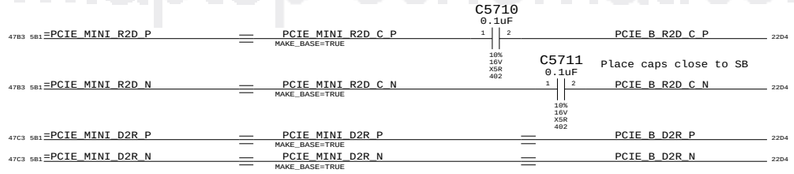
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

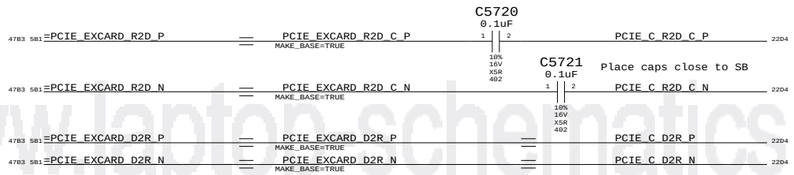
SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 55 OF 105	

PCI-E x1 Port "A" = Ethernet (Yukon)

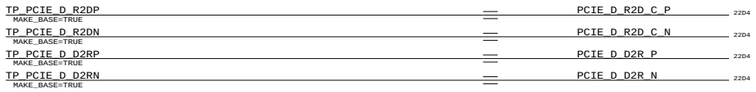
PCI-E x1 Port "B" = PCI-E Mini Card



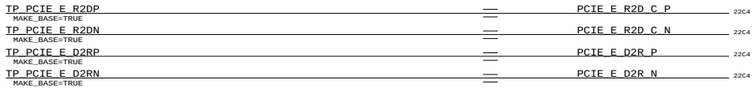
PCI-E x1 Port "C" = ExpressCard



PCI-E x1 Port "D" = Unused



PCI-E x1 Port "E" = Unused



PCI-E x1 Port "F" = Unused

PCI-E Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 57 OF 105	

UNUSED PINS HAVE THE FORMAT
SMC_XXX WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE	OUT	B12	P10	P60/KIN0*	L13	SMC_PM_G2_EN
SMC_RSTGATE_L	OUT	C13	P11	P61/KIN1*	L14	SMC_ADAPTER_EN
ALL_SYS_PWRGD	IN	A15	P12	P62/KIN2*	L15	SPI_ARB
RSMRST_PWRGD	IN	B14	P13	P63/KIN3*	K12	SPI_SCLK
SMC_SB_NMI	OUT	B15	P14	P64/KIN4*	K13	SPI_SI
PM_RSMRST_L	OUT	C14	P15	P65/KIN5*	K14	SPI_SO
IMVP_VR_ON	OUT	D12	P16	P66/IRQ6*/KIN6*	J12	SMC_PROCHOT_3_3_L
PM_PWRBTN_L	OUT	C15	P17	P67/IRQ7*/KIN7*	J13	SMC_CPU_INIT_3_3_L
SMC_P20		D13	P20	P70/AN0	N12	SMC_CPU_ISENSE
SMC_P21		D14	P21	P71/AN1	R13	SMC_CPU_VSENSE
SMC_P22		D15	P22	P72/AN2	P13	SMC_GPU_ISENSE
SMC_P23		E12	P23	P73/AN3	R14	SMC_GPU_VSENSE
SMC_BATT_TRICKLE_EN_L	OUT	E14	P24	P74/AN4	P14	SMC_DCIN_ISENSE
SMC_BATT_CHG_EN	OUT	E15	P25	P75/AN5	R15	SMC_PBUS_VSENSE
SMC_P26		E13	P26	P76/AN6	N13	SMC_BATT_ISENSE
SMC_P27		F14	P27	P77/AN7	P15	SMC_NB1V5_ISENSE
LPC_AD<0>	IO	D9	P30/LAD0	P80/PME*	C7	SMC_WAKE_SCI_L
LPC_AD<1>	IO	C9	P31/LAD1	P81/GA20	A7	SMC_TPM_GPIO
LPC_AD<2>	IO	A9	P32/LAD2	P82/CLKRUN*	B7	PM_CLKRUN_L
LPC_AD<3>	IO	B9	P33/LAD3	P83/LPCPD*	D6	PM_SUS_STAT_L
LPC_FRAME_L	IN	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	SC_TX_L
SMC_LRESET_L	IN	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	SC_RX_L
PCI_CLK_SMC	IN	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	SMB_BSB_CLK
INT_SERIRQ	OUT	D7	P37/SERIRQ	P90/IRQ2*	K4	SMC_ONOFF_L
SMC_XDP_TMS		A5	P40/TMI0	P91/IRQ1*	J2	SMC_BC_ACOK
SMC_SYS_LED_16B	OUT	B5	P41/TMO0	P92/IRQ0*	J1	SMC_BS_ALRT_L
SMB_BSB_DATA	IO	D5	P42/SDA1	P93/IRQ12*	J3	PM_SLP_S3_L
SMC_TPM_PP	OUT	C3	P43/TMI1/EXSCKX	P94/IRQ13*	J4	PM_SLP_S4_L
SMC_XDP_TRST_L	OUT	B1	P44/TMO1	P95/IRQ14*	H2	PM_SLP_S5_L
SMC_XDP_TCK	OUT	C2	P45	P96/EXCL	H1	SMC_SUS_CLK
SMC_SYS_LED	OUT	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	SMB_0_S0_DATA
SMC_SYS_KBDLED	OUT	C1	P47/PWX1/PWM1			
SMC_TX_L	OUT	G1	P50			
SMC_RX_L	IN	G4	P51			
SMB_0_S0_CLK	IO	F2	P52/SCL0			

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	OUT	R3	PA0/KIN8*/PA2DC	PE0	M3	SMC_CASE_OPEN
BOOT_LPC_SPI_L	IN	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	SMC_TCK
PM_SYSRST_L	IN	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	SMC_TDI
SMC_USB_DEBUG_MUX	OUT	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	SMC_TDO
PM_EXTTS_L	IN	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	SMC_TMS
PM_THRM_L	IO	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7	SMC_PF0
SYS_ONEWIRE	IO	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6	SMC_PF1
PM_BATLOW_L	OUT	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	SMC_LID
SMC_EXTSMI_L	IN	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	SMC_CPU_RESET_3_3_L
SMC_RUNTIME_SCI_L	OUT	A10	PB1/LSCI	PF4/PWM4	M6	SMC_BATT_ISET
SMC_ODD_DETECT	IN	D10	PB2	PF5/PWM5	R5	SMC_BATT_VSET
ISENSE_CAL_EN	OUT	A11	PB3	PF6/PWM6	P5	SMC_SYS_ISET
SMC_EXCARD_CP	IN	B11	PB4	PF7/PWM7	N5	SMC_SYS_VSET
SMC_EXCARD_PWR_EN	OUT	C11	PB5	PG0/EXIRQ8*/TMIX	P9	SPI_CE_L
SMC_EXCARD_OC_L	IN	A12	PB6	PG1/EXIRQ9*/TMIY	R9	SMC_XDP_TCK_3_3
SMC_XDP_TDO_3_3	OUT	D11	PB7	PG2/EXIRQ10*/SDA2	N9	SMB_BSA_DATA
SMC_FAN_0_CTL	OUT	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	SMB_BSA_CLK
SMC_FAN_1_CTL	OUT	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	SMB_A_S3_DATA
SMC_FAN_2_CTL	OUT	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	SMB_A_S3_CLK
SMC_FAN_3_CTL	OUT	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	SMB_B_S0_DATA
SMC_FAN_0_TACH	IN	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	SMB_B_S0_CLK
SMC_FAN_1_TACH	IN	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	SMC_PROCHOT
SMC_FAN_2_TACH	IN	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	SMC_THRMTRIP
SMC_FAN_3_TACH	IN	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	SMC_FWE
SMS_X_AXIS	IN	M11	PD0/AN8	PH3/EXEXCL	C4	ALS_GAIN
SMS_Y_AXIS	IN	P11	PD1/AN9	PH4	D4	SMS_INT_L
SMS_Z_AXIS	IN	R11	PD2/AN10	PH5	B3	SMS_ONOFF_L
SMC_ANALOG_ID	IN	N11	PD3/AN11			
SMC_NB_ISENSE	IN	P10	PD4/AN12			
SMC_MEM_ISENSE	IN	R10	PD5/AN13			
ALS_LEFT	IN	N10	PD6/AN14			
ALS_RIGHT	IN	M10	PD7/AN15			

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

=PP3V3_S5_SMC
OMIT
C5802 22UF 20% 6.3V CERM 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
VCL IS INTERNAL RAIL
C5807 0.47UF 10% 6.3V CERM-X5R 402

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

=PP3V3_S5_SMC
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.35 MM
MIN_NECK_WIDTH=0.20 MM
C5820 0.1UF 20% 10V CERM 402
GND_SMC_AVSS

PP3V3_AVREF_SMC
=PP3V3_S5_SMC

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

SMC_RST_L
SMC_XTAL
SMC_EXTAL
KBC_MDE
SMC_NMI
SMC_TRST_L
NOSTUFF
R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
R5898 10K 5% 1/16W MF-LF 402
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402

XW5800
SM
GND_SMC_AVSS

SMC

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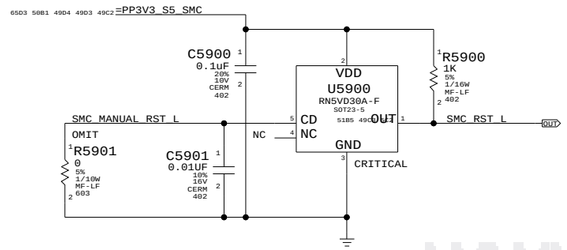
APPLE COMPUTER INC.

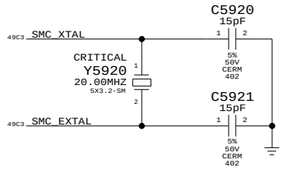
SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 58 OF 105	

SMC Reset Button / Brownout Detect

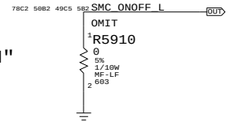


Silk: "SMC RST"

SMC Crystal Circuit

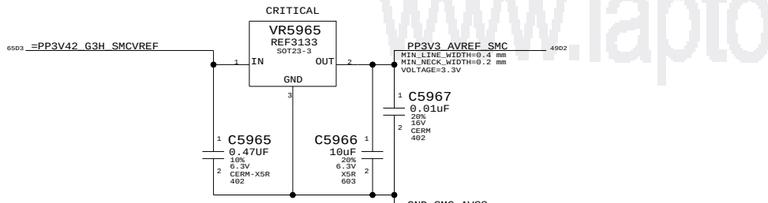


Debug Power Button

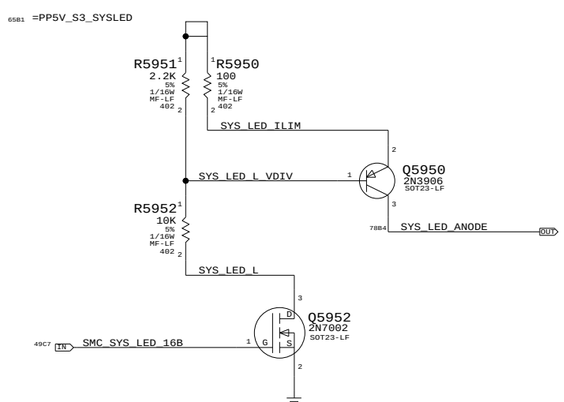


Silk: "PWR BTN"

SMC AVREF Supply

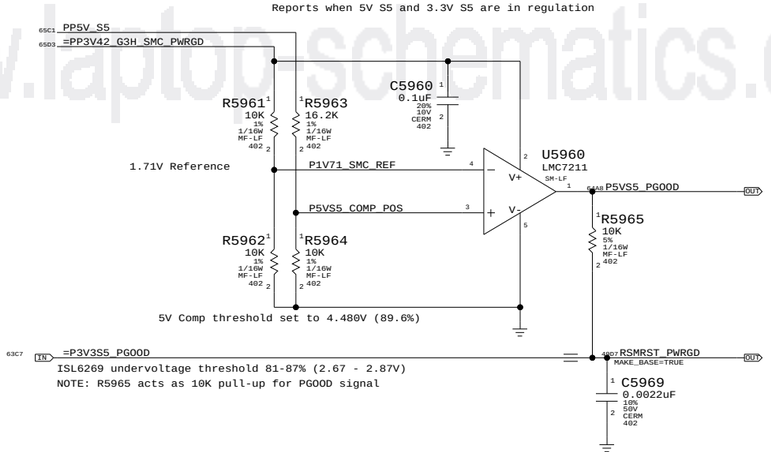


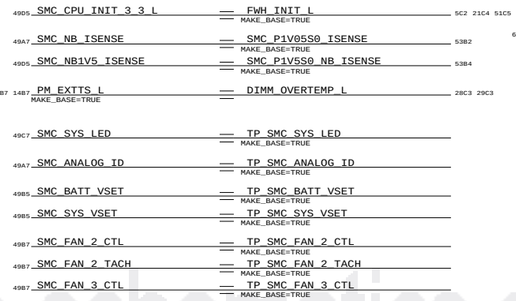
System (Sleep) LED Circuit

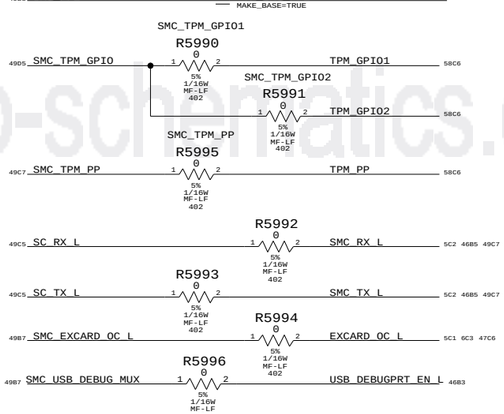


SMC PWRGD Circuit

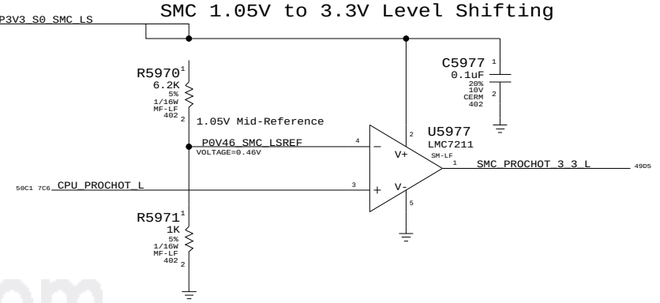
Reports when 5V S5 and 3.3V S5 are in regulation



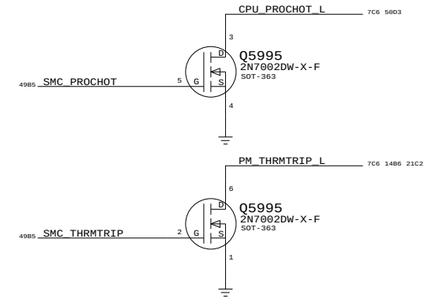




SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting



SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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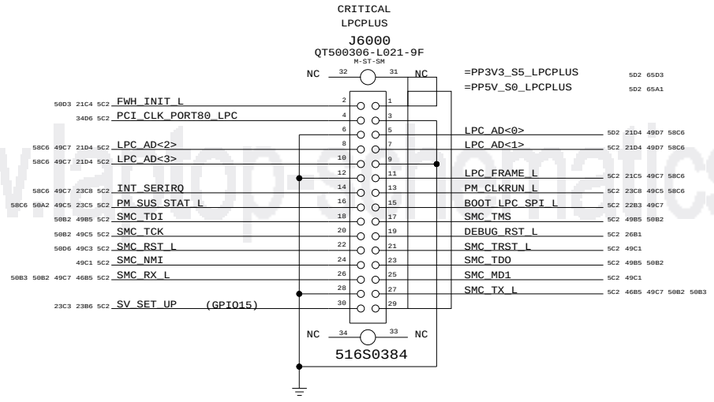
SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 59 OF 105	



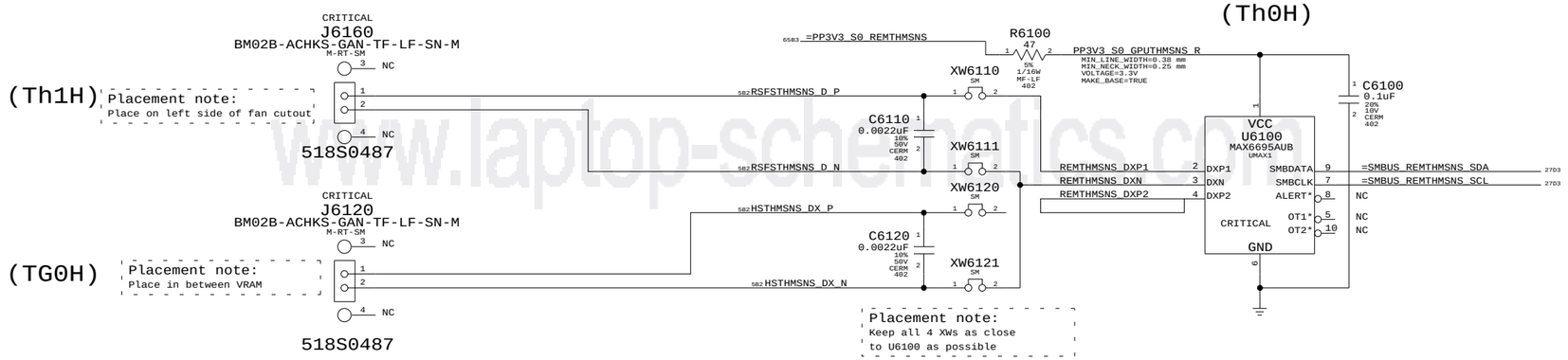
LPC+ Debug Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

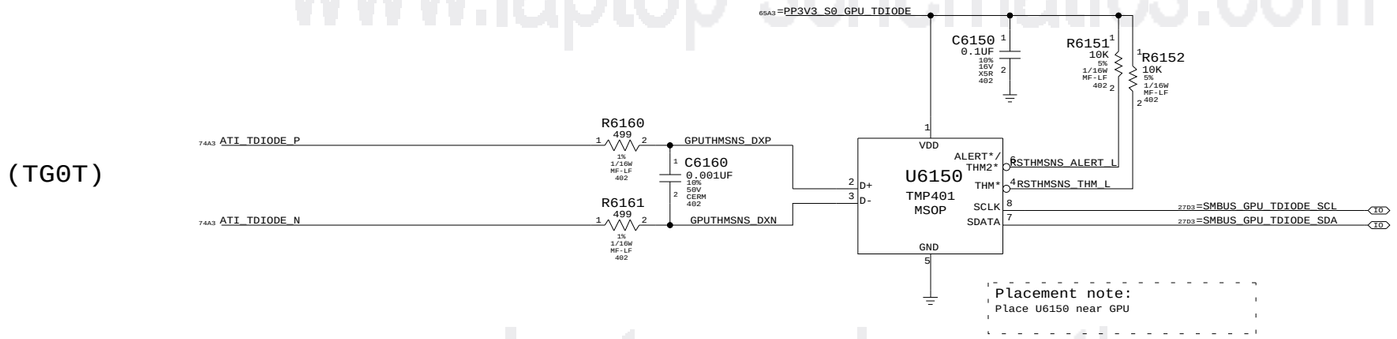
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 60 OF 105	

GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



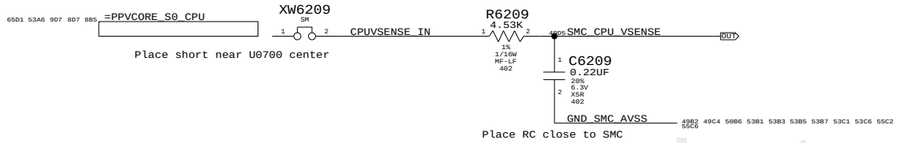
Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 61 OF 105	

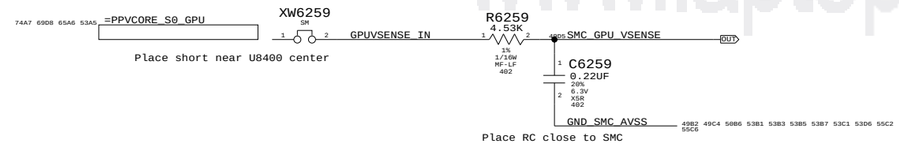
CPU Voltage Sense / Filter



Place short near U0700 center

Place RC close to SMC

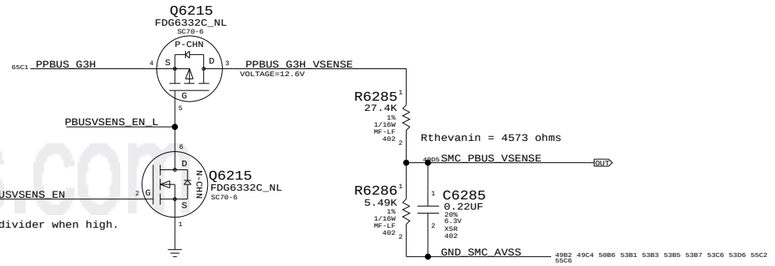
GPU Voltage Sense / Filter



Place short near U8400 center

Place RC close to SMC

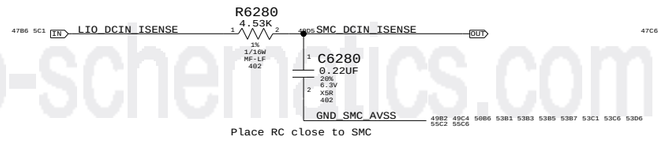
PBUS Voltage Sense Enable & Filter



Enables PBUS VSense divider when high.

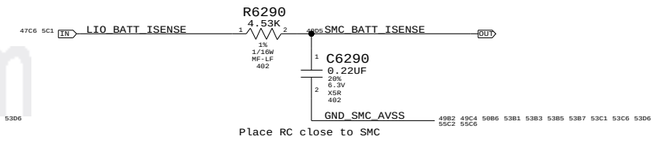
Place RC close to SMC

DCIN Current Sense Filter



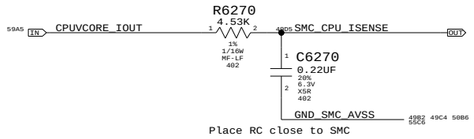
Place RC close to SMC

Battery Current Sense Filter



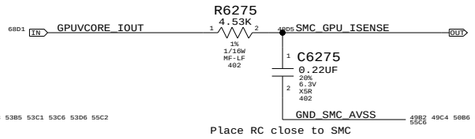
Place RC close to SMC

CPU Current Sense Filter



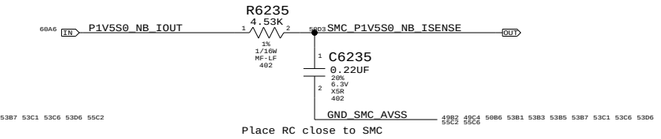
Place RC close to SMC

GPU Current Sense Filter



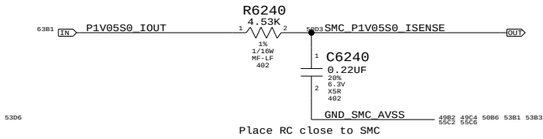
Place RC close to SMC

1.5V S0 (NB) Current Sense Filter



Place RC close to SMC

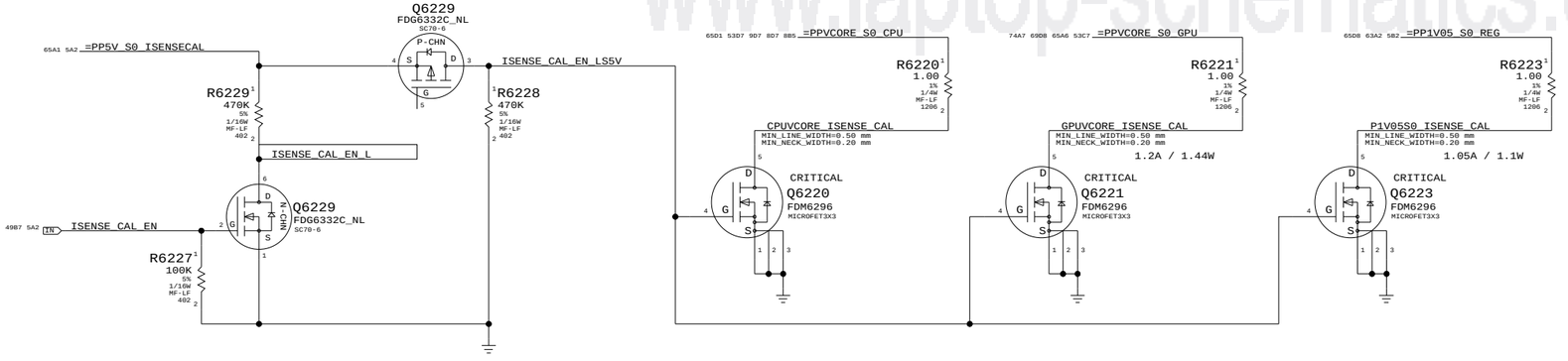
1.05V S0 (NB) Current Sense Filter



Place RC close to SMC

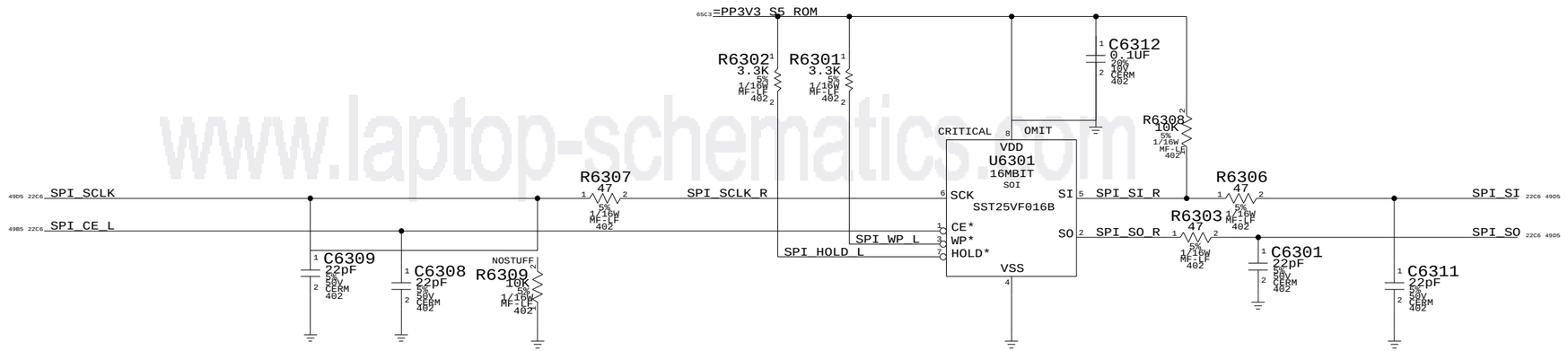
Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 62 OF 105	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

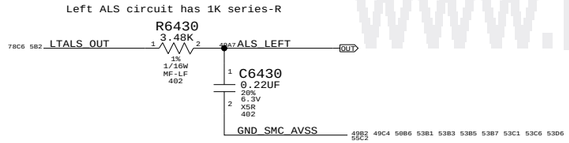
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

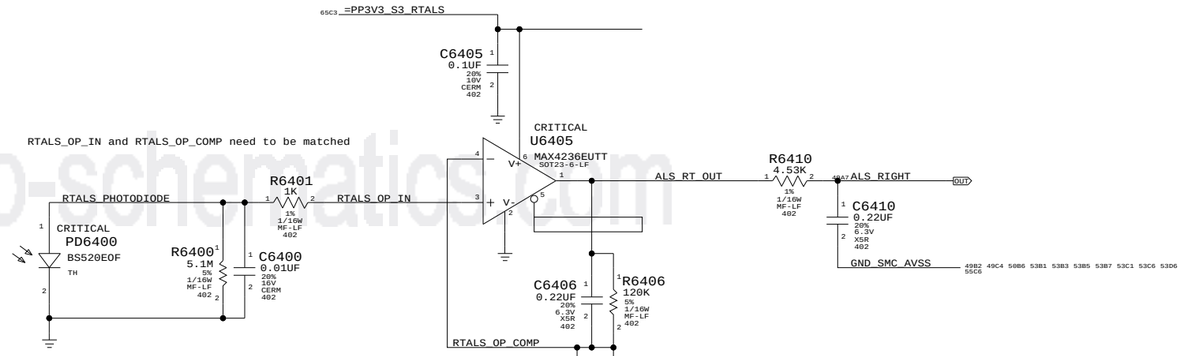
SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE	SHT	OF
NONE	63	105

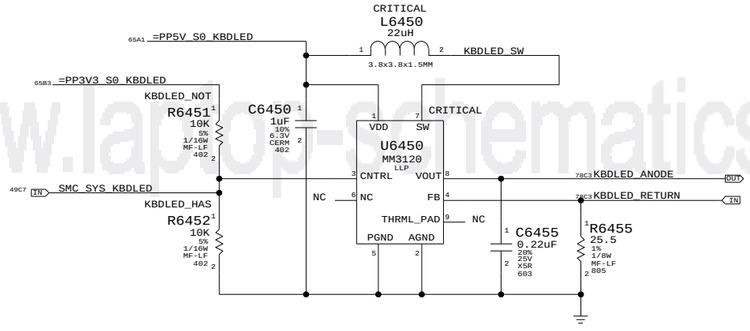
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



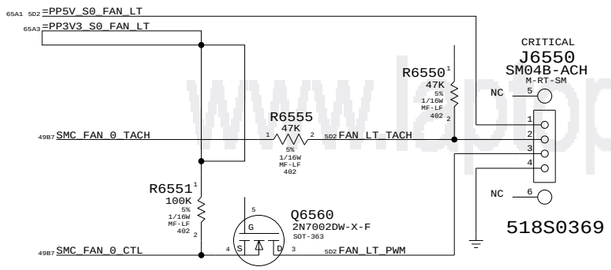
ALS Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

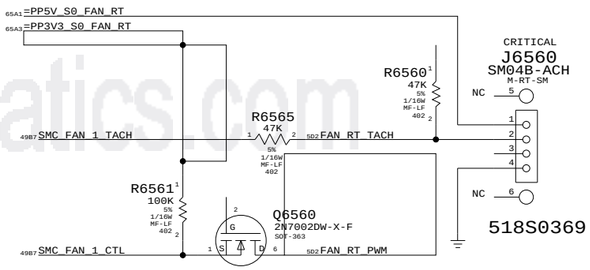
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 64 OF 105	

Left Fan



Right Fan



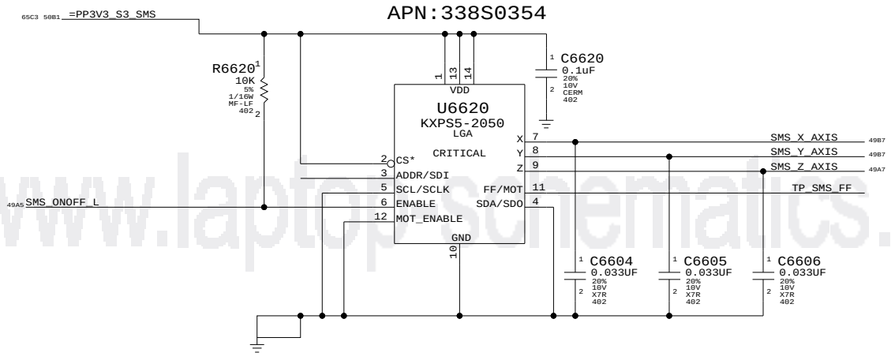
Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

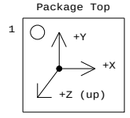
SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 65 OF 105	

APN:338S0354



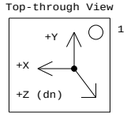
Desired orientation when
placed on board top-side:

Package Top



Desired orientation when
placed on board bottom-side:

Top-through View



M59 placement: Bottom-side

Sudden Motion Sensor (SMS)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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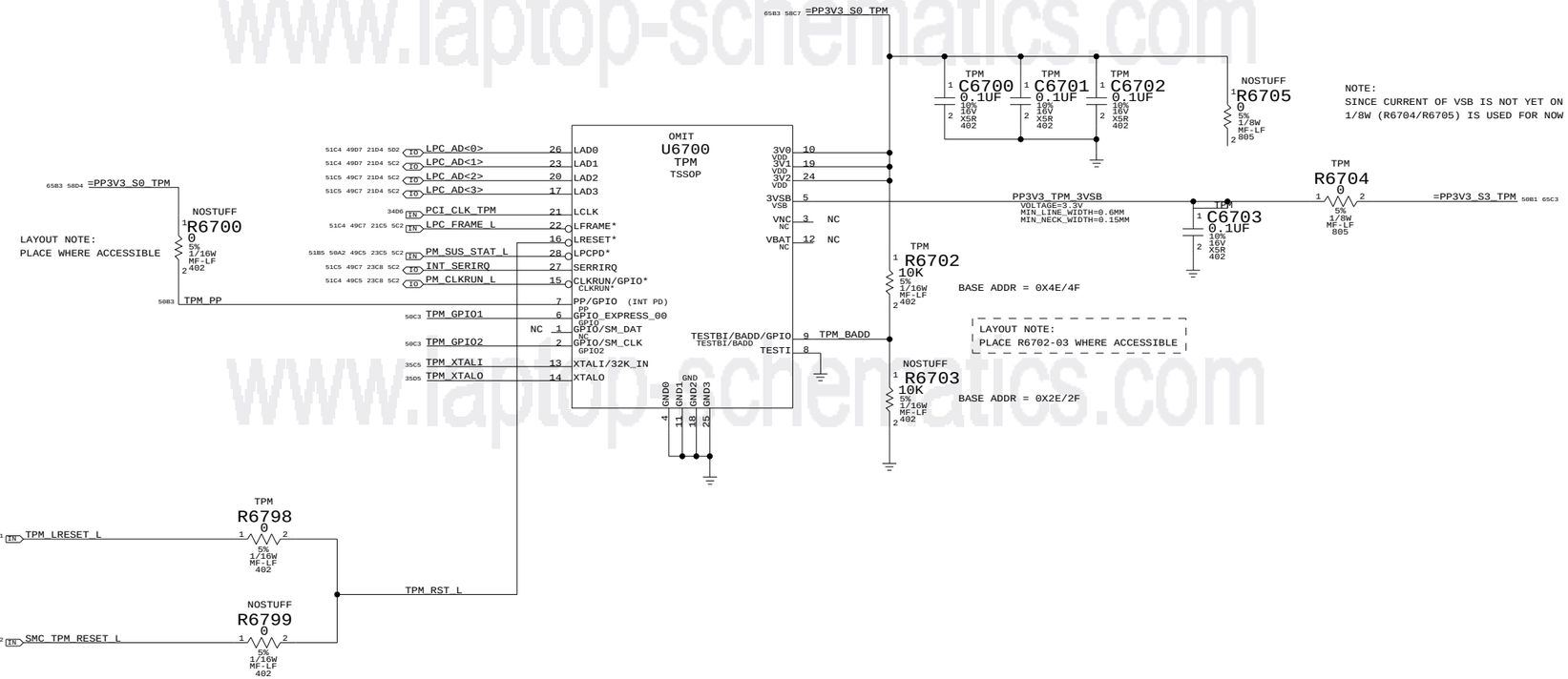
SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE: NONE

SHT 66 OF 105



TPM

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE	SHT	OF
NONE	67	105

DPRSLPVR	DPRSTP*	PSI*	Operation Mode	
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

Vout = Variable
36A max output
(Inductors limit)

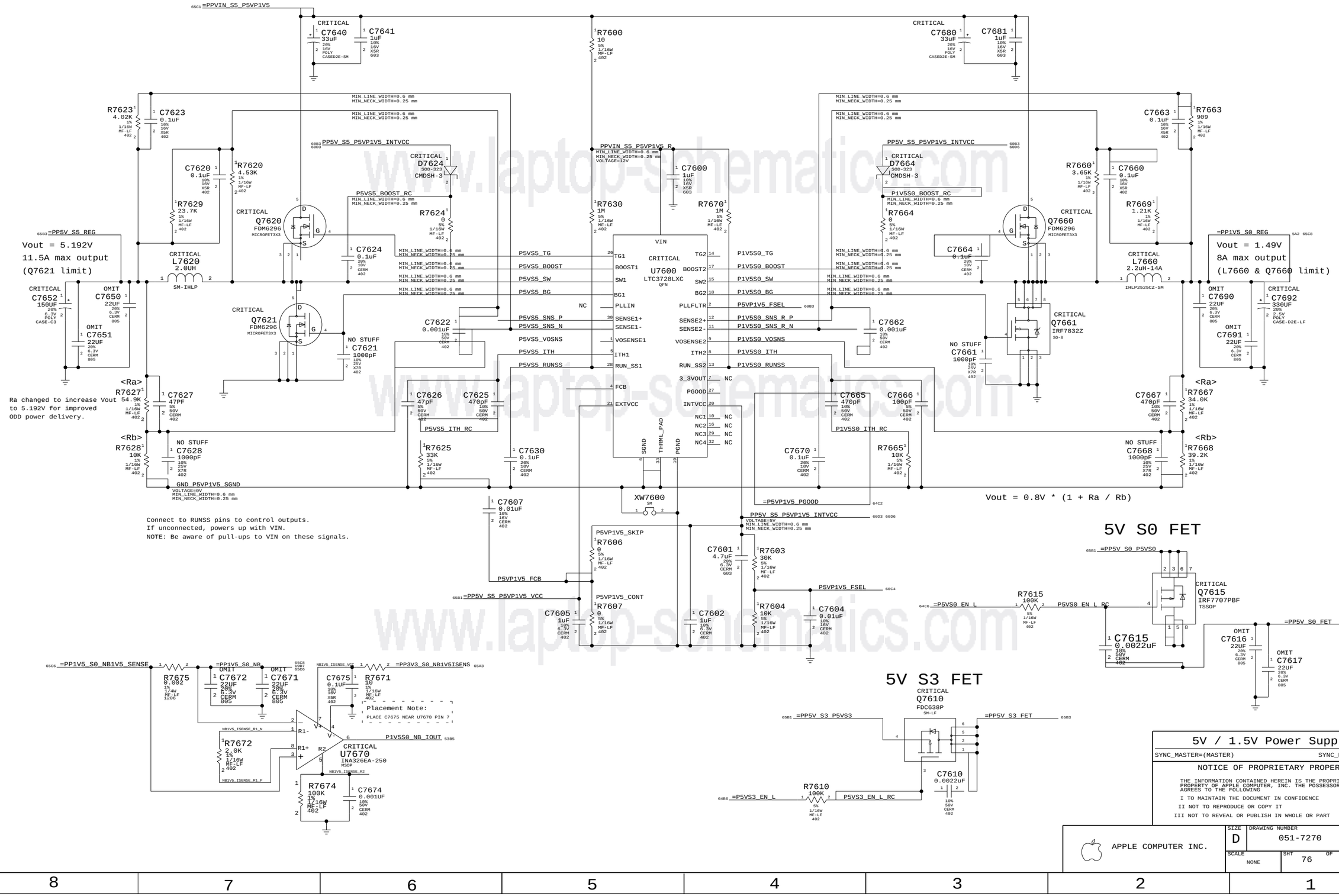
Vout = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kdroop) + Vamp_offset
Gain = Rc / (Ra + Rb)
Voffset worst-case ~2.3mV (+/- ~1A offset)
Vout @ 36A = 2.44V-2.60V

IMVP6 CPU VCore Regulator

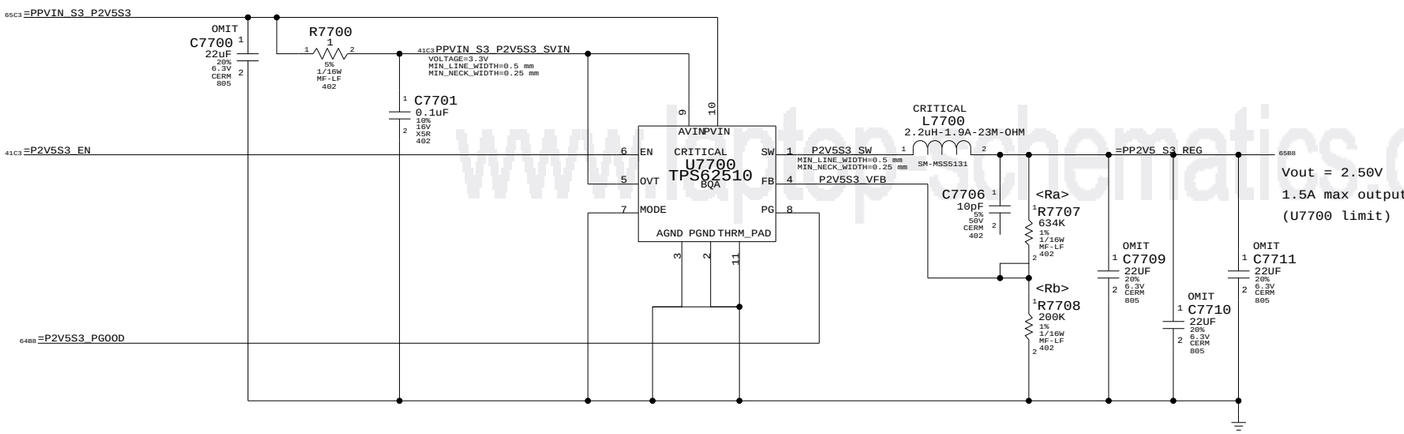
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE	SHT	OF
NONE	75	105



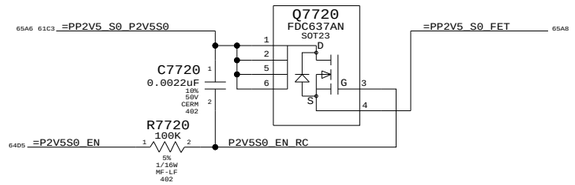
2.5V S3 Regulator



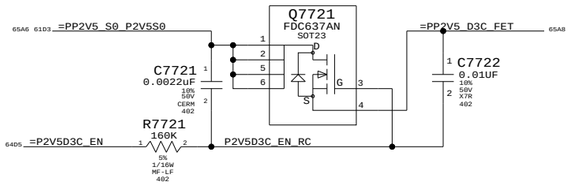
Vout = 2.50V
1.5A max output
(U7700 limit)

Vout = 0.6V * (1 + Ra / Rb)

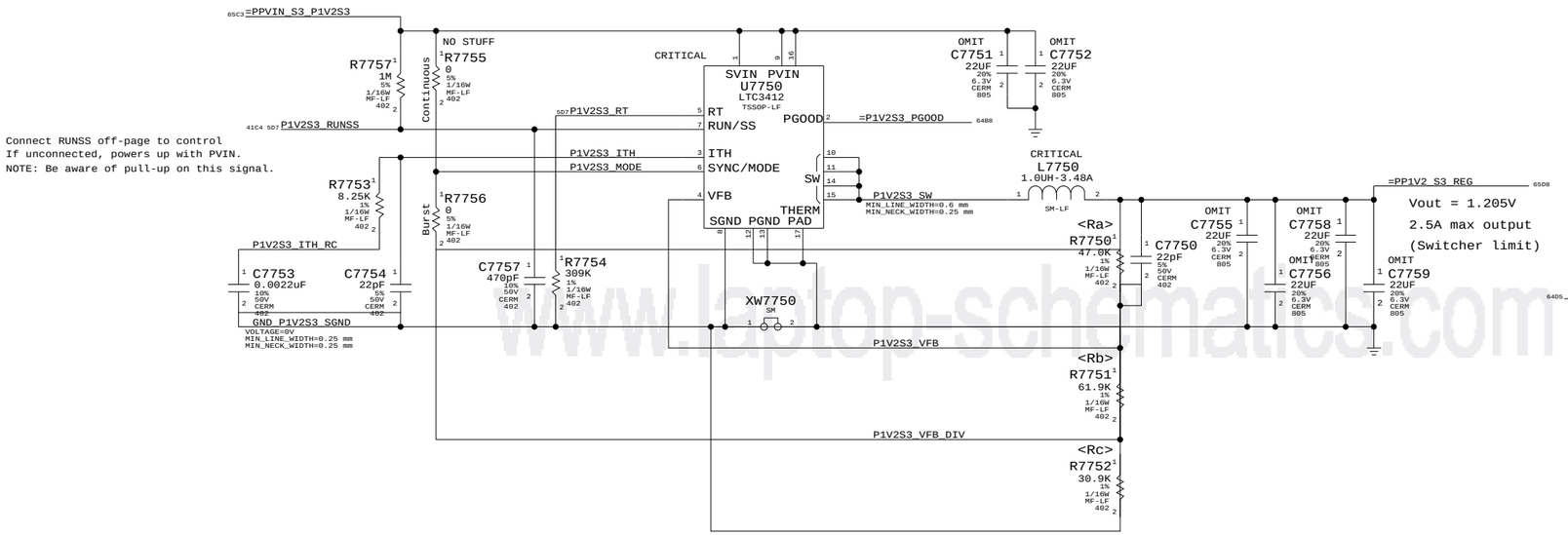
2.5V S0 FET



2.5V D3Cold FET



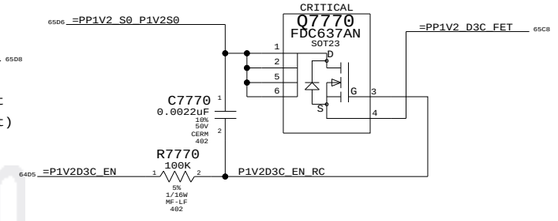
1.2V S3 Regulator



Vout = 1.205V
2.5A max output
(Switcher limit)

Vout = 0.8V * (1 + Ra / (Rb + Rc))

1.2V D3Cold FET

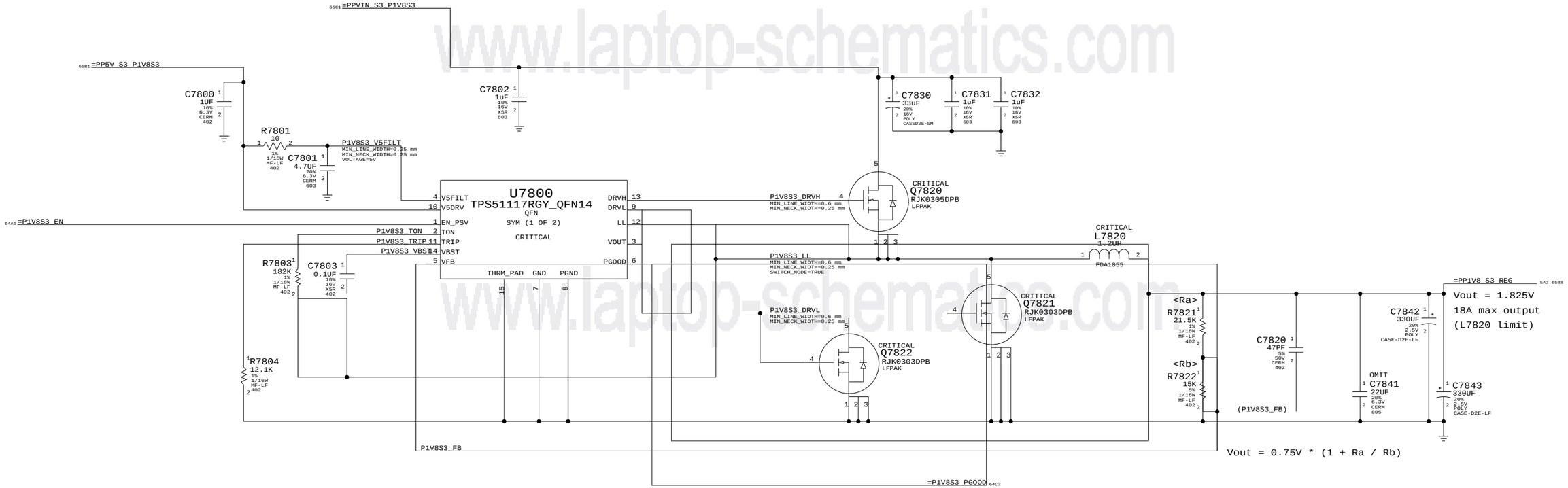


2.5V & 1.2V Regulators

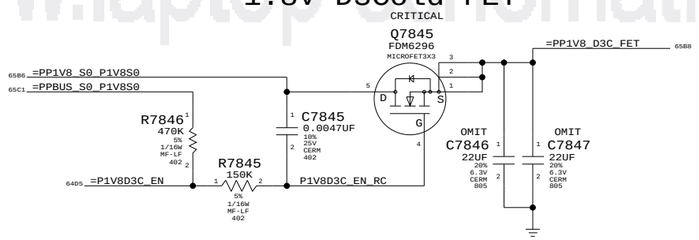
SYNC_MASTER=M59_MG SYNC_DATE=05/07/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 77 OF 105	



1.8V D3Cold FET

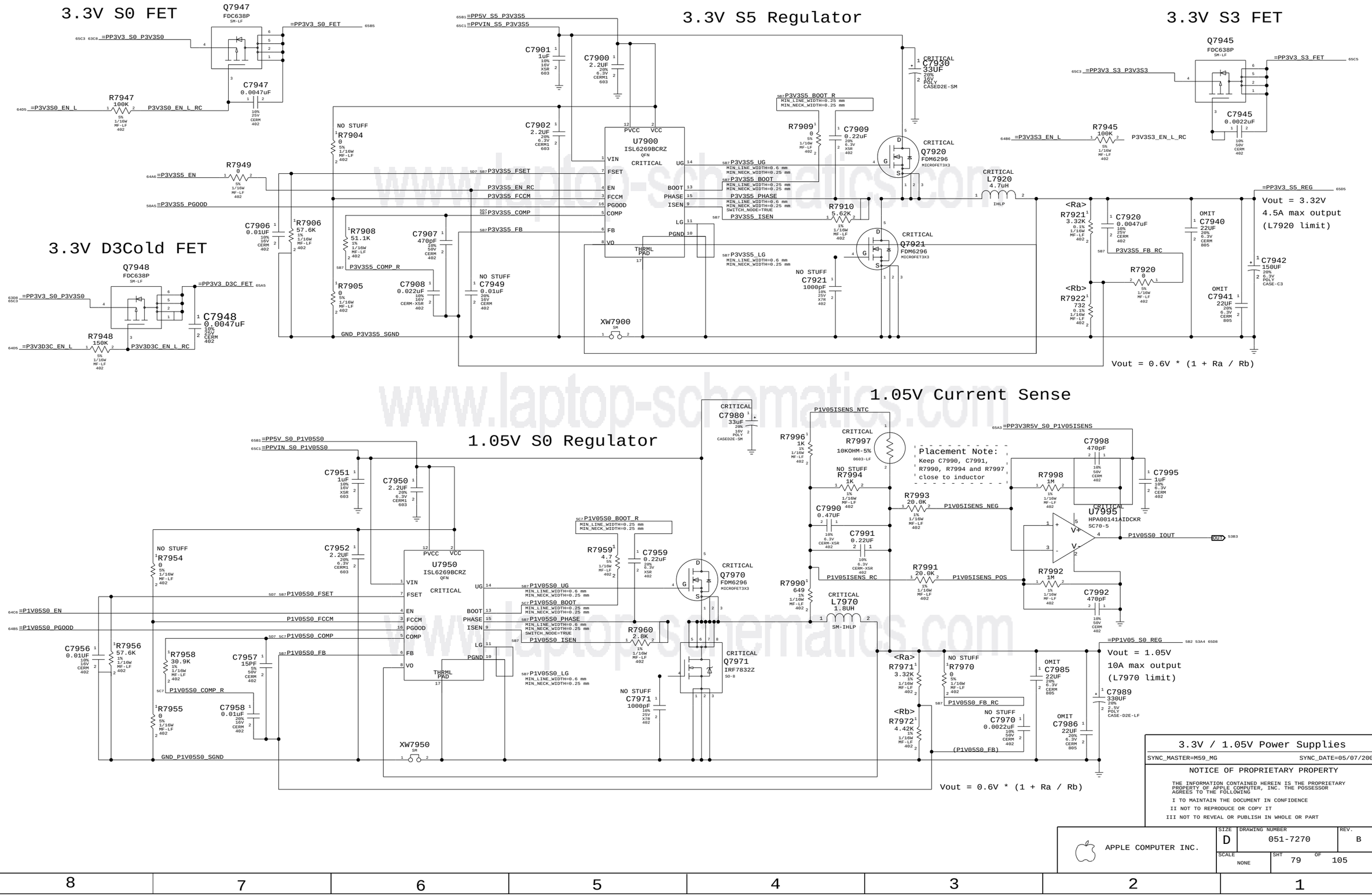


1.8V Supply

SYNC_MASTER=M59_MG SYNC_DATE=05/07/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 78 OF 105	



Power Control Signals

65B1 64B8 =PP5V_S5_PWRCTL

R8050 10K 5% 1/16W MF-LF 402
R8051 10K 5% 1/16W MF-LF 402
R8052 10K 5% 1/16W MF-LF 402
R8068 10K 5% 1/16W MF-LF 402
R8069 10K 5% 1/16W MF-LF 402

GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up.

68C8 IN =GPUVCORE_PGOOD

Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.

P1V2R2V5D3C_EN_LS5V
MAKE_BASE=TRUE

P3V3D3C_EN_L
MAKE_BASE=TRUE

P1V8D3C_EN
MAKE_BASE=TRUE

=P2V5D3C_EN 61C3
=P1V2D3C_EN 61B3
=P3V3D3C_EN_L 63C8
=P1V8D3C_EN 62A6

1.8V Enable has pull-up to PBUS

Q8055 2N7002DW-X-F SOT-363
Q8056 2N7002DW-X-F SOT-363
Q8050 2N7002DW-X-F SOT-363
Q8058 2N7002DW-X-F SOT-363
Q8058 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V_L
MAKE_BASE=TRUE

P3V3S0_EN_L
MAKE_BASE=TRUE

=P2V5S0_EN 61D3
=P3V3S0_EN_L 63D8

PM_SLP_S3_LS5V
MAKE_BASE=TRUE

=P5VS0_EN_L 60B3
LIO_P3V3S0_EN_L 5C1 47B6
P1V5S0_RUNSS 5B7 5D7 60C4

1.5V Enable has pull-up to PBUS

65D3 64A8 =PP3V42_G3H_PWRCTL

Q8050 2N7002DW-X-F SOT-363
R8054 100K 5% 1/16W MF-LF 402
Q8057 2N7002DW-X-F SOT-363
Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3

42A8 23C3 49C5 IN PM_SLP_S3_L

R8056 100K 5% 1/16W MF-LF 402

(PM_SLP_S3_L)
MAKE_BASE=TRUE

=P1V05S0_EN 63B8
=ENET_VMAIN_AVLBL 39C8
=MEMVREF_EN 32B3
=PBUSVSENS_EN 53C3

65C3 =PP3V3_S3_PWRCTL

C8081 0.1uF 20% 10V CERM 402

65A3 =PP3V3_S0_PWRCTL

R8053 10K 5% 1/16W MF-LF 402
R8081 10K 5% 1/16W MF-LF 402

PM_SLP_S3_L_GPUVCORE_EN

C8053 0.047UF 10% 10V CERM 402

TP_SB_GPIO38 SB_GPUVCORE_DISABLE_L
MAKE_BASE=TRUE

U8081 MC74VHC1G08 SC70

GPUVCORE_EN
MAKE_BASE=TRUE

=GPUVCORE_EN 68C8

61C8 IN =P2V5S3_PGOOD
61B5 IN =P1V2S3_PGOOD
TP_P2V5S3_P1V2S3_PGOOD
MAKE_BASE=TRUE

This signal was used as an option previously to test for 2v5 and 1v2 S3 valid for GPUVCORE_EN. But was disconnected for C8053 placement.

The SB can turn off the GPUVcore (and by extension all D3Cold rails) by driving GPIO38 low.

65B1 64D8 =PP5V_S5_PWRCTL

R8055 10K 5% 1/16W MF-LF 402

PM_SLP_S4_LS5V
MAKE_BASE=TRUE

=P3V3S3_EN_L 63D3
=P5VS3_EN_L 60A4

Q8055 2N7002DW-X-F SOT-363

41B6 23C3 49C5 IN PM_SLP_S4_L

R8057 100K 5% 1/16W MF-LF 402

2.5V S3 and 1.2V S3 supplies are controlled by ethernet power control circuit.

(PM_SLP_S4_L)
MAKE_BASE=TRUE

=P1V8S3_EN 62C8
=RTUSB_EN 46C7
LIO_P3V3S3_EN 5C1 47B6

65D3 64C8 =PP3V42_G3H_PWRCTL

50A4 IN P5VS5_PGOOD

(P5VS5_PGOOD)
MAKE_BASE=TRUE

=P3V3S5_EN 63D7

P5VS5_RUNSS 5D7 60C5

5V Enable has pull-up to PBUS

R8059 470K 5% 1/16W MF-LF 402

SMC_PM_G2_EN_L

Q8059 2N7002DW-X-F SOT-363
Q8059 2N7002DW-X-F SOT-363

49D5 IN SMC_PM_G2_EN

R8058 100K 5% 1/16W MF-LF 402

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

65A6 =PPVIN_G3H_P3V42G3H

C8000 10UF 10% 25V X5R 1206-1

P3V42G3H5_BOOST

U8000 LT3470 TSOT23-8
VIN BOOST SHDN* SW BIAS NC NC CRITICAL FB GND

C8005 0.22uF 20% 6.3V X5R 402

CRITICAL L8010 33uH CDPH4D19F-SM

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

=PP3V42_G3H_REG 65D5

Vout = 3.425
200mA max output
(Switcher limit)

C8010 22pF 5% 50V CERM 402

<Ra> R8010 348K 1% 1/16W MF-LF 402
<Rb> R8011 200K 1% 1/16W MF-LF 402

5D7 P3V42G3H_FB

OMIT C8015 22UF 20% 6.3V CERM 805

Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

65C3 =PP3V3_S5_P1V5PG
65C6 PP1V5_S0

R8061 27.4K 1% 1/16W MF-LF 402
R8063 4.99K 1% 1/16W MF-LF 402

0.89V Reference

P1V0_P1V5PG_REF
P1V5S0_COMP_POS

R8062 10K 1% 1/16W MF-LF 402
R8064 10K 1% 1/16W MF-LF 402

C8060 0.1uF 20% 10V CERM 402

U8060 LMC7211 SM-LF
V+ V- P1V5S0_PGOOD

R8065 10K 5% 1/16W MF-LF 402

1.5V Comp threshold set to 1.32V (88%)

IMVP_PWRGD_IN OUT 59C7

63B8 IN =P1V05S0_PGOOD

P1V5P1V05S0_PGOOD
MAKE_BASE=TRUE

ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)
NOTE: R8065 acts as 10K pull-up for PGOOD signal

Unused PGOOD Signals

60B3 =P5VP1V5_PGOOD — TP_P5V_P1V5_PGOOD MAKE_BASE=TRUE
62B4 =P1V8S3_PGOOD — TP_P1V8S3_PGOOD MAKE_BASE=TRUE

Other S0 Rails PWRGD Circuit

Does not include D3C rails for GPU!!

65C3 PP3V3_S0
65B1 PP5V_S0
65A6 PP2V5_S0
65D6 PP0V9_S0

R8074 68.1K 1% 1/16W MF-LF 402
R8072 365K 1% 1/16W MF-LF 402
R8070 845K 1% 1/16W MF-LF 402

C8070 0.1uF 20% 10V CERM 402

CRITICAL
U8070 LTC2903 TSOT-23
V1 V2 V3 V4 GND RST*

S0PGOOD_5V_DIV
S0PGOOD_2V5_DIV
S0PGOOD_0V9_DIV

S0PGOOD_PWROK 79A4 79D5

R8076 10K 5% 1/16W MF-LF 402

R8075 100K 1% 1/16W MF-LF 402 — C8075 0.1UF 20% 10V CERM 402
R8073 100K 1% 1/16W MF-LF 402 — C8073 0.1UF 20% 10V CERM 402
R8071 100K 1% 1/16W MF-LF 402 — C8071 0.1UF 20% 10V CERM 402

LTC2903 guaranteed threshold is 93.5% (3.055V, 4.725V, 2.325V, 0.840V)

=PP3V3_S0_ALLSYSPG 65A3 79D5

U8080 MC74VHC1G08 SC70
79A2 PGOOD_MUXED_S0_OR_S0D3C
ALL_SYS_PWRGD OUT 26A5 49D7

C8080 0.1UF 20% 10V CERM 402

3.3V G3Hot Supply & Power Control

SYNC_MASTER=M59_MG SYNC_DATE=08/01/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE NONE SHT 80 OF 105

"S3AC" rail is ON in S3 on AC, OFF in S3 on battery

PP0V9_S0
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
31C2 =PP0V9_S0_MEMVTT_LDO
=PP0V9_S0_MEM_TERM 64B5 30D5

PP1V05_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
63A2 53A4 5B2 =PP1V05_S0_REG
=PP1V05_S0_CPU 7B5 7B6 7D5 8C7 9B7 11B3 11C5
=PP1V05_S0_FSB_NB 12A7 12B7 12C2 19D7 34B8 34C6 34C8
=PP1V05_S0_NB_CRT 19D6 19D7
=PP1V05_S0_NB_VTT 17D3 19C8 19D7
=PP1V05_S0_SB_CPU_IO 21C1 24C3 25C4
=PPVCORE_S0_NB 16C8 16D3 19C8 19D2 19D7
=PPVCORE_S0_SB 24D3 25D3

PP1V2_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.22 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
61B3 =PP1V2_S3_REG
=PP1V2_S3_ENET 39A8 39D7
=PP1V2_S0_P1V2S0 61B3

PP1V2_D3C
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
79D7
61B1 =PP1V2_D3C_FET
=PP1V2_S0_GPU_VDDPLL 74B8
=PP1V2_S0_PCIE_GPU 67A1
=PP1V2_S0_PCIE_GPU_PVDD 67C7
=PP1V2_S0_PCIE_GPU_VDDR 67C7

PP1V5_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0
MAKE_BASE=TRUE
64C5
60C1 5A2 =PP1V5_S0_REG
=PP1V5_S0_CPU 8B7 9B7
=PP1V5_S0_NB1V5_SENSE 60A8
=PP1V5_S0_SB 25A8 25C8
=PP1V5_S0_SB_VCC1_5_A 24A3 25C2
=PP1V5_S0_SB_VCC1_5_A_ARX 24B5 25D6
=PP1V5_S0_SB_VCC1_5_A_ATX 24A5 25C6
=PP1V5_S0_SB_VCC1_5_A_USB_CORE 24A3 25B2
=PP1V5_S0_SB_VCCSATAPLL 24B5 25D6
=PP1V5_S0_SB_VCCUSBPLL 24A5 25B6
=PP1V5_S0_LIO 5D1 47D6
=PP1V5_S0_ITPMOUNT 11C4

PP1V5_S0_NB
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0
MAKE_BASE=TRUE
65C6 68A7 19D7 =PP1V5_S0_NB
=PP1V5_S0_NB 19D7 68A7 65C8
=PP1V5_S0_NB_3G 19B5 19D7
=PP1V5_S0_NB_3GPLL 19B5 19D7
=PP1V5_S0_NB_PCIE 13D2 19D7
=PP1V5_S0_NB_PLL 19B8 19D7
=PP1V5_S0_NB_VCCD_LVDS 17C6 19A5
=PP1V5_S0_NB_TVDAC 19D2 19D6 19D7
=PP1V5_S0_NB_VCCAUX 16D1 17B6 19C4 19D7
=PP1V5_S0_NB_VCCD_HMPLL 17C6 19D7

PP1V8_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
62C1 5A2 =PP1V8_S3_REG
=PP1V8_S3_MEM 28B2 28D3 28D6 29B2 29D3 29D6
=PP1V8_S3_MEM_NB 14C2 16B6 19D7
=PP1V8_S3_MEMVREF 32C6
=PP1V8_S0_MEMVTT 31C5
=PP1V8_S0_P1V8S0 62A6
=PP1V8_S3_FW 37B2

PP1V8_D3C
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
79D7
62A4 =PP1V8_D3C_FET
=PP1V8R2V0_S0_FB_GPU 69B8 70A5 70A8 70B5 70B8
=PP1V8_S0_FB_VDD 72D5 72D8 73D5 73D8
=PP1V8_S0_FB_VDDQ 72D5 72D8 73D5 73D8

PP2V5_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V
MAKE_BASE=TRUE
61D4 =PP2V5_S3_REG
=PP2V5_S3_ENET 39D3
=PP2V5_S0_P2V5S0 61C3 61D3

PP2V5_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V
MAKE_BASE=TRUE
64B5
61D1 =PP2V5_S0_FET
=PP2V5_S0_NB_VCCA_3GBG 17D6 19C5 19D7
=PP2V5_S0_NB_VCC_TXLVDS 17D6 19A6 19D7
=PP2V5_S0_NB_VCCA_LVDS 17C6 19A4
=PP2V5_S0_NB_DPLL 19A8
=PP2V5_S0_LVDS_MUX 79C5 79D3

PP2V5_D3C
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0
MAKE_BASE=TRUE
79D7
61C1 =PP2V5_D3C_FET
=PP2V5_S0_GPU 75C8
=PP2V5_S0_GPU_PVDD 74A8
=PP2V5_S0_GPU_VDD25 74C6
=PP2V5_S0_GPU_VDDC_CT 74C6

PPVCORE_D3C_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
68C1 =PPVCORE_S0_GPU_REG
=PPVCORE_S0_GPU 53A5 53C7 69D8 74A7
=PPVCORE_S0_GPU_BBP 68B7

PPDCIN_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE
47C6 5D1 =PPDCIN_G3H_LIO
=PPVIN_G3H_P3V42G3H 64D5

GND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

PP3V42_G3H
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.425V
MAKE_BASE=TRUE
64D2 =PP3V42_G3H_REG
=PP3V42_G3H_SMCVREF 50B7
=PP3V42_G3H_SMBUS_SMC_BSA 27C3
=PP3V42_G3H_PWRCTL 64A8 64C8
=PP3V42_G3H_SB_RTC 26D6
=PP3V42_G3H_SMC_PWRGD 50B5
=PP3V42_G3H_SMC_CLK 35B7
=PP3V42_G3H_LIO 5D1 47D6
=PP3V42_G3H_LIDSWITCH 78D3
=PP3V3_S5_SMC 49C2 49D3 49D4 50B1 50D7
=PP3V3_S5_LPCPLUS 5D2 51C4
=PP3V42_G3H_SMCUSBMUX 46B5

PP3V3_S5
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
63D1 =PP3V3_S5_REG
=PP3V3_S5_SB 23A7 23B7 23D4 23D8 25C8
=PP3V3_S5_SB_3V3_1V5_VCCSUSHDA 24C3
=PP3V3_S5_SB_IO 22C6
=PP3V3_S5_SB_PM 11B5 23D1 26C5
=PP3V3_S5_SB_USB 22D8
=PP3V3_S5_SB_VCCSUS3_3 24A5 24B3 25B6 25D2
=PP3V3_S5_SB_VCCSUS3_3_USB 24B3 25D2
=PP3V3_S5_ROM 54D4
=PP3V3_S5_P1V5PG 64C5
=PP3V3_S3_P3V3S3 63D2
=PPVIN_S3_P2V5S3 61D8
=PP3V3_S0_LCD 76D5
=PP3V3_S0_P3V3S0 63C8 63D8

PP3V3_S3
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
63D1 =PP3V3_S3_FET
=PP3V3_S3_P3V3S3AC 41C5
=PP3V3_S3_RTALS 55D4
=PP3V3_S3_SMBUS_SMC_A_S3 27C5
=PP3V3_S3_TPM 50B1 58C2
=PP3V3_S3_SMS 50B1 57C6
=PP3V3_S3_TOPCASE 78D3
=PP3V3_S3_LTALS 58Z 78C5
=PP3V3_S3_MEMVREF 32C5
=PP3V3_S3_FW 37A7 37C3 37D7
=PP3V3_S3_PCI 37D5
=PPVIN_S3_P1V2S3 61B7
=PP3V3_S3_PWRCTL 64C6

PP3V3_S0
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
64B5
63D6 =PP3V3_S0_FET
=PP3V3_S0_DDC_LCD 76D3
=PP3V3_S0_CK410 33C7 33D3 33D8 34A8
=PP3V3_S0_IDE 36D6
=PP3V3_S0_IMVP6 59D8
=PP3V3_S0_INVERTER 76A8
=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4
=PP3V3_S0_NB_VCC_HV 17C6 19C6 19C7
=PP3V3_S0_SB 22B5 25D8
=PP3V3_S0_SB_3V3_1V5_VCCHDA 24C3 25C4
=PP3V3_S0_SB_GPIO 21C3 21D3 23B3 23D5
=PP3V3_S0_SB_PCI 26D1
=PP3V3_S0_SB_PM 26B6 26B8
=PP3V3_S0_SB_VCC3_3 24B5 25B8 25C6
=PP3V3_S0_SB_VCC3_3_IDE 24C3 25B4
=PP3V3_S0_SB_VCC3_3_PCI 24B3 25A4
=PP3V3_S0_SB_VCCLAN3_3 24D3 25D3
=PP3V3_S0_TPM 58C7 58D4
=PP3V3_S0_KBDLED 55B6
=PP3V3_S0_THRM_SNR 10C5
=PP3V3_S0_REMTHMSNS 52D4
=PP3V3_S0_SMBUS_SB 27D8
=PP3V3_S0_SMBUS_SMC_0_S0 27D5
=PP3V3_S0_SMBUS_SMC_B_S0 27D3
=PP3V3_S0_SMBUS_SMC_BSB 27C3
=PP3V3_S0_RSTBUF 26B4
=PP3V3_S0_SMC_LS 50D3
=PP3V3_S0_ALLSYSPG 64B1 79D5
=PP3V3_S0_FAN_LT 56C7
=PP3V3_S0_FAN_RT 56C4
=PP3V3R5V_S0_CPUISENS 59A5
=PP3V3R5V_S0_GPUISENS 68D2
=PP3V3R5V_S0_P1V05ISENS 63B3
=PPSPD_S0_MEM 28A6 29A3 29A6
=PP3V3_S0_EDET 40B6
=PP3V3_S0_LVDS_MUX 79A4 79B3 79C6
=PP3V3_S0_NB1V5ISENS 60A6
=PP3V3_S0_GPU_TDIODE 52B5
=PP3V3_S0_PWRCTL 64B6

PP3V3_D3C
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
79D7
63C7 =PP3V3_D3C_FET
=PP3V3_S0_GPU 68C4 74D2
=PP3V3_S0_GPUBBP 68B8
=PP3V3_S0_GPUBBN 68A4
=PP3V3_S0_GPU_VDDR3 74C6
=PP3V3_D3C_GPU_GPIOS 71D6
=PP1V8R3V3_S0_GPU_VDDR4 74B7
=PP1V8R3V3_S0_GPU_VDDR5 74B7
=PP3V3_D3C_DDC_DVI 77B2
=PP3V3_D3C_VGASYNC 77D5
=PP3V3_D3C_GPU_LVDS_DDC 79A7
=PP3V3_D3C_GPU 71B2

PP3V3_S3AC
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.22 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
41C4 =PP3V3_S3AC_FET
=PP3V3_S3_ENET 39A5 39B4 39B5 39B8 39D6 39D8

PNBB_S0_GPU
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=-0.7V
MAKE_BASE=TRUE
68A2 =PNVOUT_S0_GPUBBN_REG
=PNBB_S0_GPU 69D2

PPBB_S0_GPU
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.9V
MAKE_BASE=TRUE
68B5 =PPVOUT_S0_GPUBBP_LDO
=PPBB_S0_GPU 69D6

PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V
MAKE_BASE=TRUE
5A2
59D1 =PPVOUT_S0_IMVP6_REG
=PPVCORE_S0_CPU 8B5 8D7 9D7 53A6 53D7

PPBUS_G3H
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
53D3
66C4 5A1 =PPBUS_G3H_LIO_CONN
=PPBUS_G3H_S3AC 41C6
=PPVIN_S5_P5VP1V5 60D7
=PPVIN_S0_IMVP6 59D4 59D7
=PPVIN_S5_P3V3S5 63D6
=PPBUS_S5_FWPWRSW 43D7
=PPVIN_S3_P1V8S3 62D7
=PPVIN_S0_P1V05S0 63B7
=PPVIN_S0_GPUVCORE 68D7
=PPBUS_S0_INVERTER 76B7
=PPBUS_S0_P1V8S0 62A6
=PPBUS_S0_PPBU_S0_FW 42B8

PPBUS_S5_FW_FET
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=33V
MAKE_BASE=TRUE
43C1 =PPBUS_S5_FW_FET
=PPFW_PORT1_VP 44D3
=PPFW_PORT2_VP 44B3
=PPFW_FW_CPS 38B7
=PPFW_P3V3FWPHY 42C8

PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
50B5
60C8 =PP5V_S5_REG
=PP5V_S5_SB 25C8
=PP5V_S5_P3V3S5 63D6
=PP5V_S5_P5VP1V5_VCC 60B6
=PP5V_S5_LIO 5D1 47C6
=PP5V_S5_PWRCTL 64B8 64D8
=PP5V_S3_P5VS3 60A4
=PP5V_S3_P1V8S3 62C8
=PP5V_S3_RTUSB 46C7
=PP5V_S0_P5VS0 60B2
=PP5V_S0_GPUVCORE 68D7
=PP5V_S0_P1V05S0 63B7

PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
60A2 =PP5V_S3_FET
=PP5V_S3_SYSLED 50B8
=PP5V_S3_CAMERA 5A4 45C3
=PP5V_S3_IR 78B5
=PP5V_S3_TOPCASE 78D3

PP5V_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
64B5
60B1 =PP5V_S0_FET
=PP5V_S0_DVI_DDC 77B5
=PP5V_S0_IDE 36D6
=PP5V_S0_HDD 78B5
=PP5V_S0_IMVP6 59D7
=PP5V_S0_INVERTER 76B8
=PP5V_S0_MEMVTT 31C5
=PP5V_S0_SB 25D8
=PP5V_S0_FAN_LT 5D2 56C7
=PP5V_S0_FAN_RT 56C4
=PP5V_S0_KBDLED 55B5
=PP5V_S0_GPUBBCTL 68A6
=PP5V_S0_LPCPLUS 5D2 51C4
=PP5V_S0_AUDIO_XW 47D3
=PP5V_S0_ISENSECAL 5A2 53A8
=PP5V_S0_SB_HPD 77A1

Power Aliases

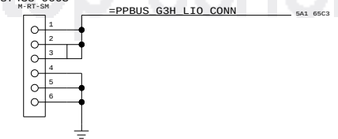
SYNC_MASTER=M59_MG SYNC_DATE=05/07/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 81 OF 105	

Left I/O Power Connector

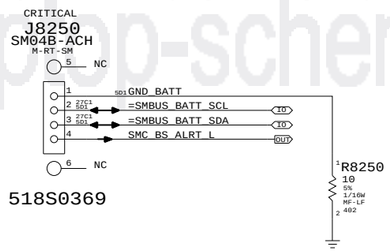
CRITICAL
J8200
87438-0663
M-RT-SM



518S0458

Battery Connector (Digital Signals)

CRITICAL
J8250
SM04B-ACH
M-RT-SM



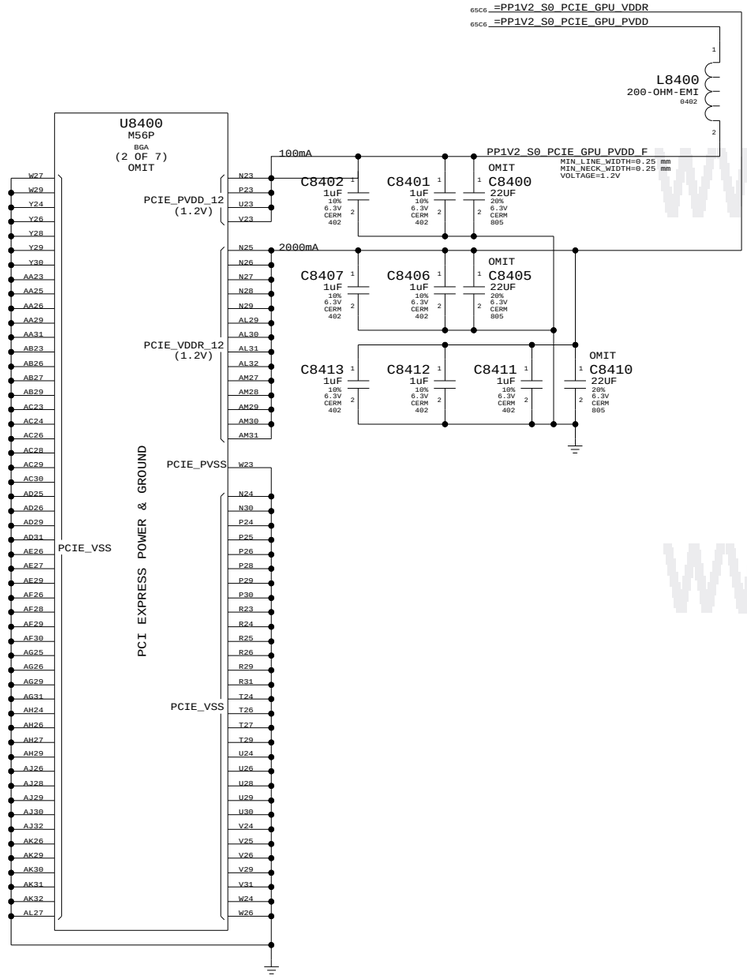
518S0369

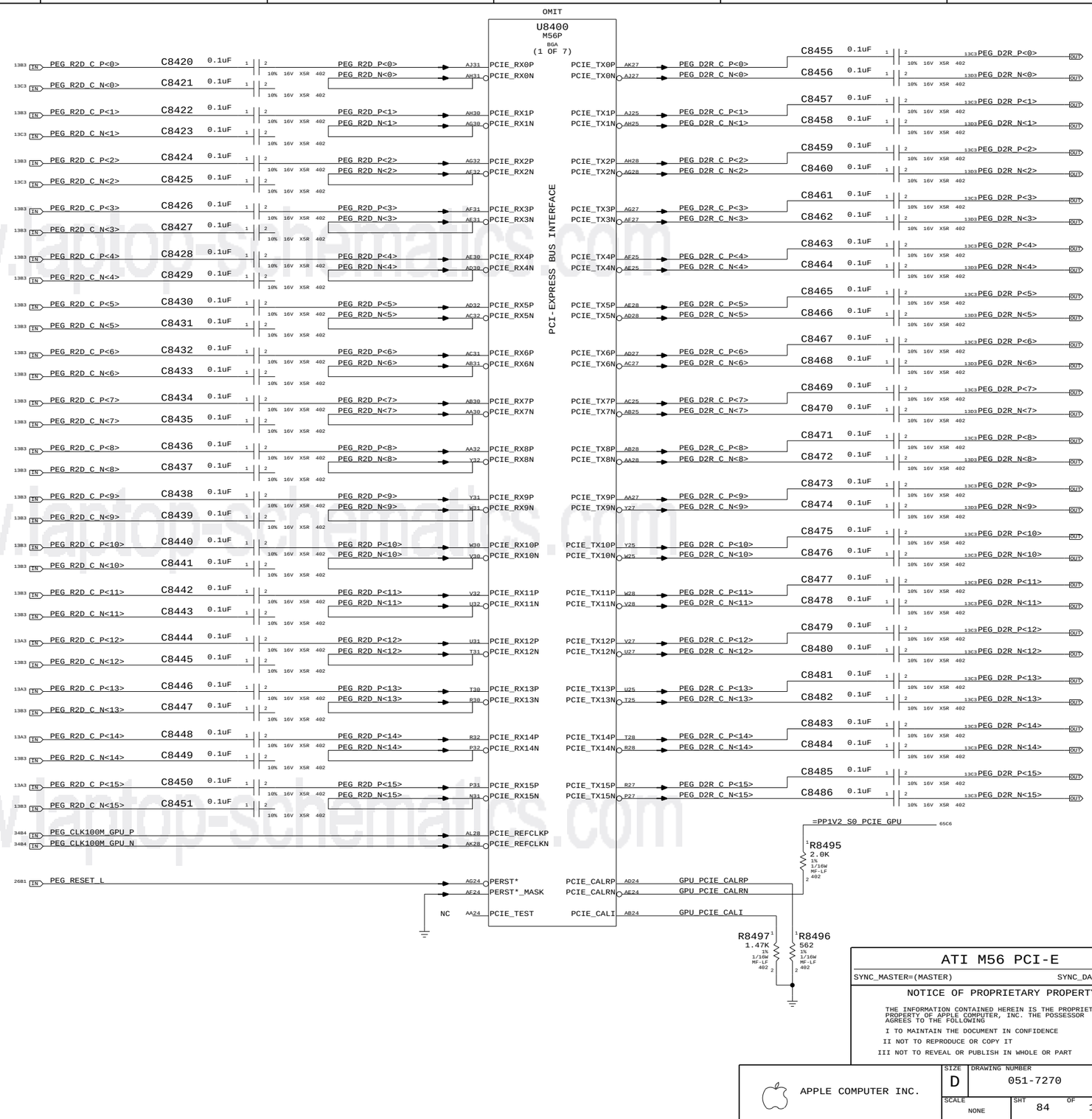
PBus-In,Batt. & 3G Pwr Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 82 OF 105	





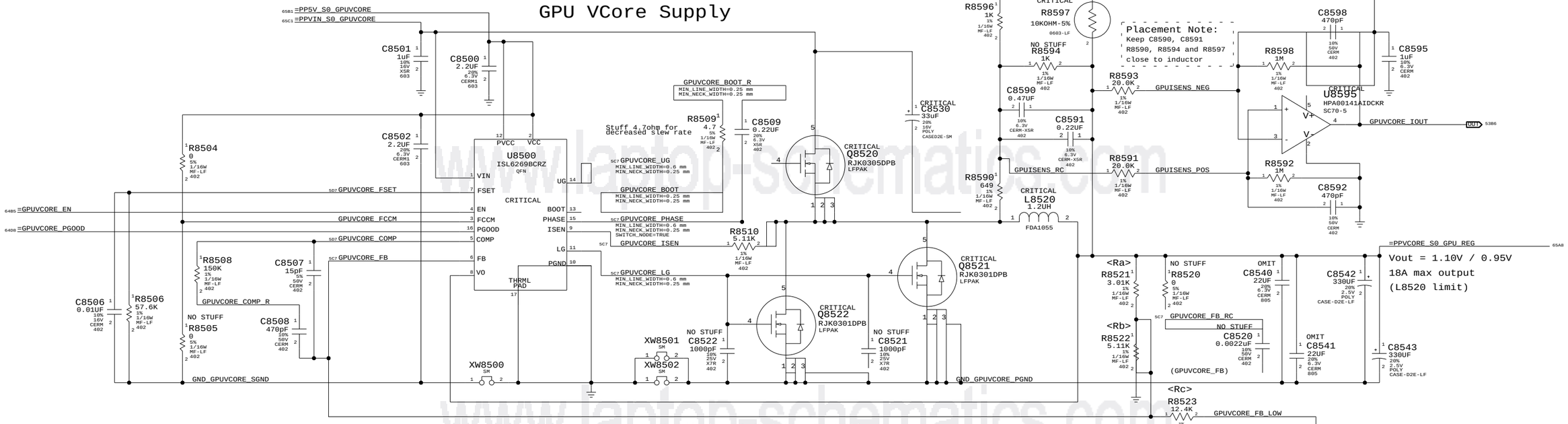
ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 84 OF 105	

GPU VCore Supply

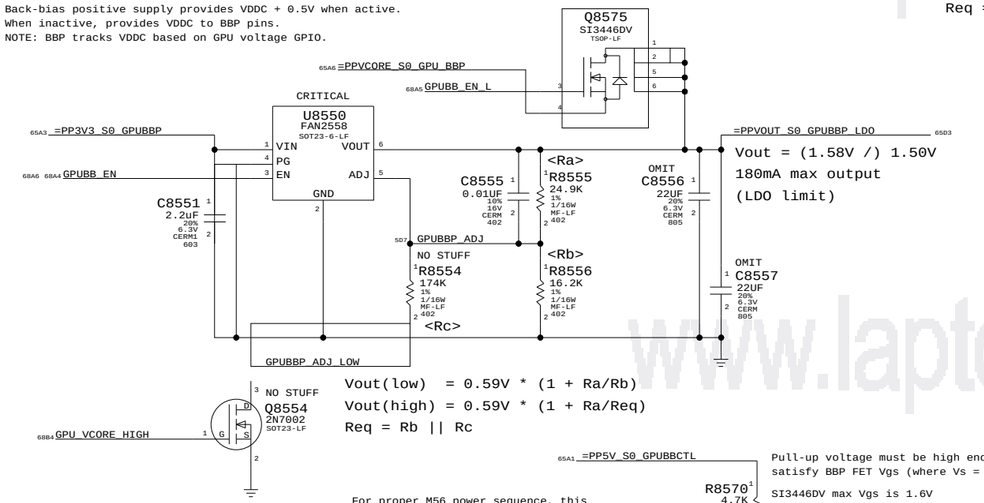


GPU VCore Current Sense

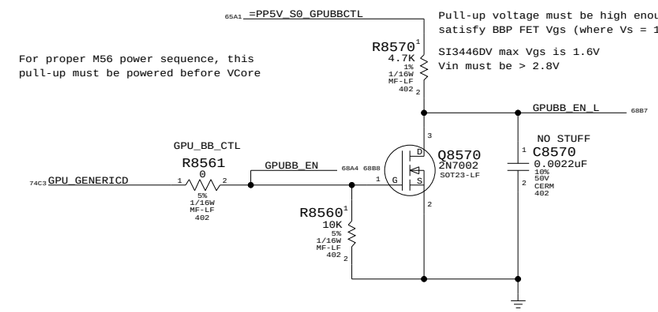
Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.



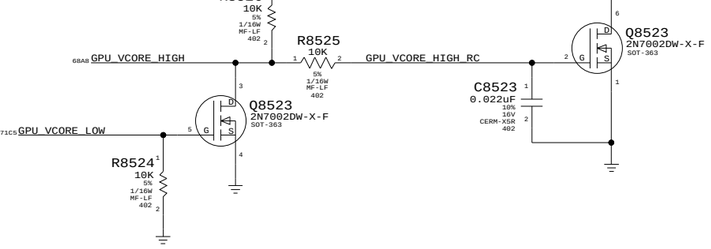
Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc



Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)

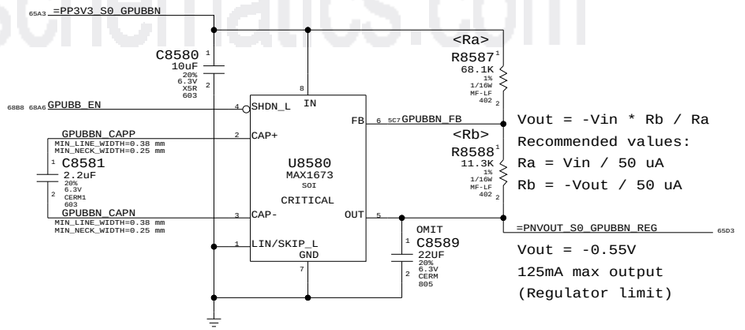
SI3446DV max Vgs is 1.6V
Vin must be > 2.8V

For proper M56 power sequence, this pull-up must be powered before VCore



Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active.
When inactive, provides VSS to BBN pins.



Vout = -Vin * Rb / Ra
Recommended values:
Ra = Vin / 50 uA
Rb = -Vout / 50 uA

Vout = -0.55V
125mA max output
(Regulator limit)

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

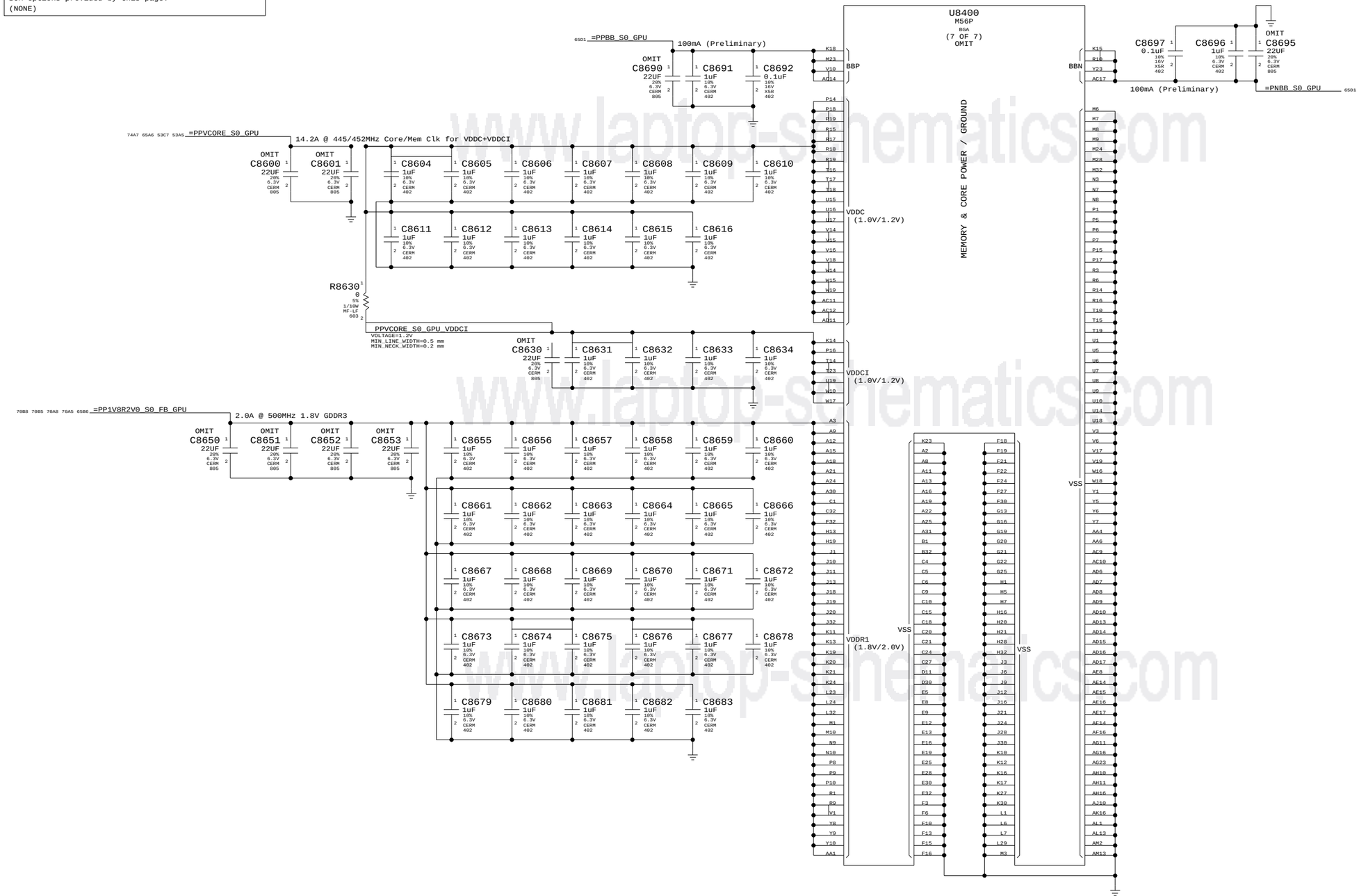
SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 85 OF 105	

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 86 OF 105	

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8400
M56P
BGA
(3 OF 7)

MEMORY INTERFACE A

FB_A_DQ<0>	M31	DQA_0	D26	MAA_0	FB_A_MA<0>
FB_A_DQ<1>	M30	DQA_1	F28	MAA_1	FB_A_MA<1>
FB_A_DQ<2>	L31	DQA_2	D28	MAA_2	FB_A_MA<2>
FB_A_DQ<3>	L30	DQA_3	D25	MAA_3	FB_A_MA<3>
FB_A_DQ<4>	H30	DQA_4	E24	MAA_4	FB_A_MA<4>
FB_A_DQ<5>	G31	DQA_5	E26	MAA_5	FB_A_MA<5>
FB_A_DQ<6>	G30	DQA_6	D27	MAA_6	FB_A_MA<6>
FB_A_DQ<7>	F31	DQA_7	F25	MAA_7	FB_A_MA<7>
FB_A_DQ<8>	M27	DQA_8	C26	MAA_8	FB_A_MA<8>
FB_A_DQ<9>	M29	DQA_9	B26	MAA_9	FB_A_MA<9>
FB_A_DQ<10>	L28	DQA_10	D29	MAA_10	FB_A_MA<10>
FB_A_DQ<11>	L27	DQA_11	B27	MAA_11	FB_A_MA<11>
FB_A_DQ<12>	J27	DQA_12	E27	MAA_12	TP_FB_A_MA12
FB_A_DQ<13>	H29	DQA_13	E29	MAA_13	FB_A_BA<2>
FB_A_DQ<14>	G29	DQA_14	B25	MAA_14	FB_A_BA<0>
FB_A_DQ<15>	G27	DQA_15	C25	MAA_15	FB_A_BA<1>
FB_A_DQ<16>	M26	DQA_16			
FB_A_DQ<17>	L26	DQA_17	H31	DQMA_0	FB_A_DQM_L<0>
FB_A_DQ<18>	M25	DQA_18	J29	DQMA_1	FB_A_DQM_L<1>
FB_A_DQ<19>	L25	DQA_19	J26	DQMA_2	FB_A_DQM_L<2>
FB_A_DQ<20>	J25	DQA_20	G23	DQMA_3	FB_A_DQM_L<3>
FB_A_DQ<21>	G28	DQA_21	E21	DQMA_4	FB_A_DQM_L<4>
FB_A_DQ<22>	H27	DQA_22	B15	DQMA_5	FB_A_DQM_L<5>
FB_A_DQ<23>	H26	DQA_23	D14	DQMA_6	FB_A_DQM_L<6>
FB_A_DQ<24>	F26	DQA_24	J17	DQMA_7	FB_A_DQM_L<7>
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FB_A_DQ<26>	H25	DQA_26	J31	QSA_0	FB_A_RDQS<0>
FB_A_DQ<27>	H24	DQA_27	K29	QSA_1	FB_A_RDQS<1>
FB_A_DQ<28>	H23	DQA_28	K25	QSA_2	FB_A_RDQS<2>
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FB_A_DQ<30>	J23	DQA_30	D20	QSA_4	FB_A_RDQS<4>
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FB_A_DQ<33>	D22	DQA_33	H15	QSA_7	FB_A_RDQS<7>
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FB_A_DQ<35>	E22	DQA_35	K31	QSA_0*	FB_A_WDQS<0>
FB_A_DQ<36>	E20	DQA_36	K28	QSA_1*	FB_A_WDQS<1>
FB_A_DQ<37>	F20	DQA_37	K26	QSA_2*	FB_A_WDQS<2>
FB_A_DQ<38>	D19	DQA_38	G24	QSA_3*	FB_A_WDQS<3>
FB_A_DQ<39>	D18	DQA_39	D21	QSA_4*	FB_A_WDQS<4>
FB_A_DQ<40>	B19	DQA_40	C16	QSA_5*	FB_A_WDQS<5>
FB_A_DQ<41>	B18	DQA_41	D15	QSA_6*	FB_A_WDQS<6>
FB_A_DQ<42>	C17	DQA_42	J15	QSA_7*	FB_A_WDQS<7>
FB_A_DQ<43>	B17	DQA_43			
FB_A_DQ<44>	C14	DQA_44	D31	CLKA0	FB_A_CLK_P<0>
FB_A_DQ<45>	B14	DQA_45	E31	CLKA0*	FB_A_CLK_N<0>
FB_A_DQ<46>	C13	DQA_46	B29	CSA0_0*	FB_A_CS_L<0>
FB_A_DQ<47>	B13	DQA_47	C28	CSA0_1*	NC
FB_A_DQ<48>	D17	DQA_48			
FB_A_DQ<49>	E18	DQA_49	B30	CKEA0	FB_A_CKE<0>
FB_A_DQ<50>	E17	DQA_50	B28	RASA0*	FB_A_RAS_L<0>
FB_A_DQ<51>	F17	DQA_51	C29	CASA0*	FB_A_CAS_L<0>
FB_A_DQ<52>	E15	DQA_52	B31	WEA0*	FB_A_WE_L<0>
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FB_A_DQ<54>	F14	DQA_54			
FB_A_DQ<55>	D13	DQA_55	B20	CLKA1	FB_A_CLK_P<1>
FB_A_DQ<56>	H18	DQA_56	C19	CLKA1*	FB_A_CLK_N<1>
FB_A_DQ<57>	H17	DQA_57	B23	CSA1_0*	FB_A_CS_L<1>
FB_A_DQ<58>	G18	DQA_58	C23	CSA1_1*	NC
FB_A_DQ<59>	G17	DQA_59			
FB_A_DQ<60>	G15	DQA_60	C22	CKEA1	FB_A_CKE<1>
FB_A_DQ<61>	G14	DQA_61	B24	RASA1*	FB_A_RAS_L<1>
FB_A_DQ<62>	H14	DQA_62	B22	CASA1*	FB_A_CAS_L<1>
FB_A_DQ<63>	J14	DQA_63	B21	WEA1*	FB_A_WE_L<1>
			D24	ODTA1	TP_FB_A_ODT<1>

=PP1V8R2V0_S0_FB_GPU

R8710 40.2 1% 1/16W MF-LF 402
R8712 40.2 1% 1/16W MF-LF 402
R8711 100 1% 1/16W MF-LF 402
C8711 0.1uF 10% 16V X5R 402
R8713 100 1% 1/16W MF-LF 402
C8713 0.1uF 10% 16V X5R 402

GPU_MVREFD0 → MVREFD_0
GPU_MVREFS0 → MVREFS_0
VDDRH0 (1.8V/2.0V)
VSSRH0

=PP1V8R2V0_S0_FB_GPU
L8715 FERR-220-OHM 0402
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
PP1V8R2V0_S0_GPU_VDDRH0
C8715 1uF 10% 6.3V CERM 402
C8716 1uF 10% 6.3V CERM 402
XW8715 SM
GND_GPU_VSSRH0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

OMIT
U8400
M56P
BGA
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MEMORY INTERFACE B

FB_B_DQ<0>	B12	DQB_0	G4	MAB_0	FB_B_MA<0>
FB_B_DQ<1>	C12	DQB_1	E6	MAB_1	FB_B_MA<1>
FB_B_DQ<2>	B11	DQB_2	E4	MAB_2	FB_B_MA<2>
FB_B_DQ<3>	C11	DQB_3	H4	MAB_3	FB_B_MA<3>
FB_B_DQ<4>	C8	DQB_4	J5	MAB_4	FB_B_MA<4>
FB_B_DQ<5>	B7	DQB_5	G5	MAB_5	FB_B_MA<5>
FB_B_DQ<6>	C7	DQB_6	F4	MAB_6	FB_B_MA<6>
FB_B_DQ<7>	B6	DQB_7	H6	MAB_7	FB_B_MA<7>
FB_B_DQ<8>	F12	DQB_8	G3	MAB_8	FB_B_MA<8>
FB_B_DQ<9>	D12	DQB_9	G2	MAB_9	FB_B_MA<9>
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FB_B_DQ<12>	F9	DQB_12	F5	MAB_12	TP_FB_B_MA12
FB_B_DQ<13>	D8	DQB_13	D5	MAB_13	FB_B_BA<2>
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FB_B_DQ<16>	G12	DQB_16			
FB_B_DQ<17>	G11	DQB_17	B8	DQMB_0	FB_B_DQM_L<0>
FB_B_DQ<18>	H12	DQB_18	D9	DQMB_1	FB_B_DQM_L<1>
FB_B_DQ<19>	H11	DQB_19	G9	DQMB_2	FB_B_DQM_L<2>
FB_B_DQ<20>	H9	DQB_20	K7	DQMB_3	FB_B_DQM_L<3>
FB_B_DQ<21>	E7	DQB_21	M5	DQMB_4	FB_B_DQM_L<4>
FB_B_DQ<22>	F8	DQB_22	V2	DQMB_5	FB_B_DQM_L<5>
FB_B_DQ<23>	G8	DQB_23	W4	DQMB_6	FB_B_DQM_L<6>
FB_B_DQ<24>	G6	DQB_24	T9	DQMB_7	FB_B_DQM_L<7>
FB_B_DQ<25>	G7	DQB_25			
FB_B_DQ<26>	H8	DQB_26	B9	QSB_0	FB_B_RDQS<0>
FB_B_DQ<27>	J8	DQB_27	D10	QSB_1	FB_B_RDQS<1>
FB_B_DQ<28>	K8	DQB_28	H10	QSB_2	FB_B_RDQS<2>
FB_B_DQ<29>	L8	DQB_29	K6	QSB_3	FB_B_RDQS<3>
FB_B_DQ<30>	K9	DQB_30	N4	QSB_4	FB_B_RDQS<4>
FB_B_DQ<31>	L9	DQB_31	U2	QSB_5	FB_B_RDQS<5>
FB_B_DQ<32>	K5	DQB_32	U4	QSB_6	FB_B_RDQS<6>
FB_B_DQ<33>	L4	DQB_33	V8	QSB_7	FB_B_RDQS<7>
FB_B_DQ<34>	K4	DQB_34			
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FB_B_DQ<36>	N5	DQB_36	E10	QSB_1*	FB_B_WDQS<1>
FB_B_DQ<37>	N6	DQB_37	G10	QSB_2*	FB_B_WDQS<2>
FB_B_DQ<38>	P4	DQB_38	J7	QSB_3*	FB_B_WDQS<3>
FB_B_DQ<39>	R4	DQB_39	M4	QSB_4*	FB_B_WDQS<4>
FB_B_DQ<40>	P2	DQB_40	U3	QSB_5*	FB_B_WDQS<5>
FB_B_DQ<41>	R2	DQB_41	V4	QSB_6*	FB_B_WDQS<6>
FB_B_DQ<42>	T3	DQB_42	V9	QSB_7*	FB_B_WDQS<7>
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FB_B_DQ<45>	W2	DQB_45	B5	CLKB0*	FB_B_CLK_N<0>
FB_B_DQ<46>	Y3	DQB_46	D2	CSB0_0*	FB_B_CS_L<0>
FB_B_DQ<47>	Y2	DQB_47	E3	CSB0_1*	NC
FB_B_DQ<48>	T4	DQB_48			
FB_B_DQ<49>	R5	DQB_49	C2	CKEB0	FB_B_CKE<0>
FB_B_DQ<50>	T5	DQB_50	E2	RASB0*	FB_B_RAS_L<0>
FB_B_DQ<51>	T6	DQB_51	D3	CASB0*	FB_B_CAS_L<0>
FB_B_DQ<52>	V5	DQB_52	B2	WEB0*	FB_B_WE_L<0>
FB_B_DQ<53>	W5	DQB_53	D6	ODTB0	TP_FB_B_ODT<0>
FB_B_DQ<54>	W6	DQB_54			
FB_B_DQ<55>	Y4	DQB_55	N2	CLKB1	FB_B_CLK_P<1>
FB_B_DQ<56>	R8	DQB_56	P3	CLKB1*	FB_B_CLK_N<1>
FB_B_DQ<57>	T8	DQB_57	K2	CSB1_0*	FB_B_CS_L<1>
FB_B_DQ<58>	R7	DQB_58	K3	CSB1_1*	NC
FB_B_DQ<59>	T7	DQB_59			
FB_B_DQ<60>	V7	DQB_60	L3	CKEB1	FB_B_CKE<1>
FB_B_DQ<61>	W7	DQB_61	J2	RASB1*	FB_B_RAS_L<1>
FB_B_DQ<62>	W8	DQB_62	L2	CASB1*	FB_B_CAS_L<1>
FB_B_DQ<63>	W9	DQB_63	M2	WEB1*	FB_B_WE_L<1>
			J4	ODTB1	TP_FB_B_ODT<1>

GPU_MVREFD1 → MVREFD_1
GPU_MVREFS1 → MVREFS_1
PP1V8R2V0_S0_GPU_VDDRH1 → VDDRH1 (1.8V/2.0V)
VSSRH1

GPU_TEST_MCLK → TEST_MCLK
GPU_TEST_YCLK → TEST_YCLK
GPU_MEMTEST → MEMTEST
DRAM_RST → FB_DRAM_RST

=PP1V8R2V0_S0_FB_GPU
R8720 40.2 1% 1/16W MF-LF 402
R8722 40.2 1% 1/16W MF-LF 402
R8721 100 1% 1/16W MF-LF 402
C8721 0.1uF 10% 16V X5R 402
R8723 100 1% 1/16W MF-LF 402
C8723 0.1uF 10% 16V X5R 402

=PP1V8R2V0_S0_FB_GPU
L8725 FERR-220-OHM 0402
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
C8725 1uF 10% 6.3V CERM 402
C8726 1uF 10% 6.3V CERM 402
XW8725 SM
GND_GPU_VSSRH1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

R8731 4.7K 5% 1/16W MF-LF 402
R8730 4.7K 5% 1/16W MF-LF 402
R8732 243 1% 1/16W MF-LF 402
R8733 4.7K 5% 1/16W MF-LF 402

ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 87 OF 105	

	Serial ROM	TestBus	Misc	Straps
GPU_GPIO_0	IPD	TESTIN[0]		TX_PWRS_ENb
GPU_GPIO_1	IPD	TESTIN[1]		TX_DEEMPH_EN
GPU_GPIO_2	VDD_VCL	TESTIN[2]		Reserved
GPU_GPIO_3		TESTIN[3]		Reserved
GPU_GPIO_4	IPD	TESTIN[4]		DEBUG_ACCESS
GPU_GPIO_5		TESTIN[5]		Reserved
GPU_GPIO_6		TESTIN[6]		Reserved
GPU_GPIO_7	ENA_BL	TESTIN[7]		
GPU_GPIO_8	ROMSO	TESTWR		Reserved
GPU_GPIO_9	IPD ROMSI			ROMIDCFG[3]
GPU_GPIO_10	ROMSCK	TESTOUT[8]		
GPU_GPIO_11	IPD	TESTOUT[9]		ROMIDCFG[0]
GPU_GPIO_12	IPD	TESTOUT[10]		ROMIDCFG[1]
GPU_GPIO_13	IPD	TESTOUT[11]		ROMIDCFG[2]
GPU_GPIO_14		TESTIN[8]		
GPU_GPIO_15		TESTIN[9]	PWRCNTL	
GPU_GPIO_16			SS_IN	
GPU_GPIO_17			Thm Mon Int	

GPU_GPIO_18 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_18
GPU_GPIO_19 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_19
GPU_GPIO_20 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_20
GPU_GPIO_21 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_21
GPU_GPIO_22 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_22
GPU_GPIO_23 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_23
GPU_GPIO_24 — MAKE_BASE=TRUE, NO_TEST=TRUE
GPU_GPIO_25 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_25
GPU_GPIO_26 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_26
GPU_GPIO_27 — MAKE_BASE=TRUE, NO_TEST=TRUE
GPU_GPIO_28 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_28
GPU_GPIO_29 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_29
GPU_GPIO_30 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_30
GPU_GPIO_31 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_31
GPU_GPIO_32 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_32
GPU_GPIO_33 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_33
GPU_GPIO_34 — MAKE_BASE=TRUE, NO_TEST=TRUE — NC_GPU_GPIO_34

=PP3V3_D3C_GPU_GPIOS

ROMCFGID[3..0]

0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

R8800	10K	
GPU_DEEPMH_EN R8801	10K	
NO STUFF R8802	10K	
NO STUFF R8803	10K	
NO STUFF R8804	10K	
R8805	10K	
NO STUFF R8806	10K	
NO STUFF R8808	10K	
NO STUFF R8809	10K	
GPU_MEM_64M R8813	10K	
GPU_MEM_256M R8812	10K	
NO STUFF R8811	10K	
GPU_MEM_256M R8824	10K	
GPU_MEM_NOT_SAM R8827	10K	

All: 5% 1/16W MF-LF 402

GPU_BLON — MAKE_BASE=TRUE — 79A4

TP_GPU_GPIO_10 — MAKE_BASE=TRUE — Required for debug access
Required for debug access
Required for debug access
Required for debug access

NC_GPU_GPIO_14 — MAKE_BASE=TRUE, NO_TEST=TRUE
GPU_VCORE_LOW — MAKE_BASE=TRUE — 68B4
GPU_CLK27MSS_IN — MAKE_BASE=TRUE — 34B2 34B4
NC_GPU_GPIO_17 — MAKE_BASE=TRUE, NO_TEST=TRUE

GPU_MEM_256M — MAKE_BASE=TRUE
GPU_MEMID — MAKE_BASE=TRUE

Renamed signals

34B4 34B2 GPU_CLK27M — MAKE_BASE=TRUE — GPU_XTALIN 74A5

Unused signals

NC_GPU_XTALOUT	MAKE_BASE=TRUE, NO_TEST=TRUE	GPU_XTALOUT 74A5
NC_ATI_ROMCS_L	MAKE_BASE=TRUE, NO_TEST=TRUE	TP_ATI_ROMCS_L 74A3
NC_FB_A_MA12	MAKE_BASE=TRUE, NO_TEST=TRUE	TP_FB_A_MA12 70D5
NC_FB_B_MA12	MAKE_BASE=TRUE, NO_TEST=TRUE	TP_FB_B_MA12 70D1
NC_GPU_GENERICA	MAKE_BASE=TRUE, NO_TEST=TRUE	GPU_GENERICA 74C3
NC_GPU_GENERICB	MAKE_BASE=TRUE, NO_TEST=TRUE	GPU_GENERICB 74C3
NC_GPU_GENERICC	MAKE_BASE=TRUE, NO_TEST=TRUE	GPU_GENERICC 74C3
NC_GPU_VGA_R	MAKE_BASE=TRUE, NO_TEST=TRUE	GPU_VGA_R 75C3
NC_GPU_VGA_G	MAKE_BASE=TRUE, NO_TEST=TRUE	GPU_VGA_G 75C3
NC_GPU_VGA_B	MAKE_BASE=TRUE, NO_TEST=TRUE	GPU_VGA_B 75C3
TP_GPU_VGA_HSYNC	MAKE_BASE=TRUE	GPU_VGA_HSYNC 75B3
TP_GPU_VGA_VSYNC	MAKE_BASE=TRUE	GPU_VGA_VSYNC 75B3
NC_GPU_TV_Y	MAKE_BASE=TRUE, NO_TEST=TRUE	GPU_TV_Y 75B3
NC_GPU_TV_C	MAKE_BASE=TRUE, NO_TEST=TRUE	GPU_TV_C 75B3
NC_GPU_TV_COMP	MAKE_BASE=TRUE, NO_TEST=TRUE	GPU_TV_COMP 75B3
NC_LVDS_U_DATAP<3>	MAKE_BASE=TRUE, NO_TEST=TRUE	LVDS_U_DATA_P<3> 75B3
NC_LVDS_U_DATAN<3>	MAKE_BASE=TRUE, NO_TEST=TRUE	LVDS_U_DATA_N<3> 75B3
NC_LVDS_L_DATAP<3>	MAKE_BASE=TRUE, NO_TEST=TRUE	LVDS_L_DATA_P<3> 75A3
NC_LVDS_L_DATAN<3>	MAKE_BASE=TRUE, NO_TEST=TRUE	LVDS_L_DATA_N<3> 75A3
NC_ATI_DVPCLK	MAKE_BASE=TRUE, NO_TEST=TRUE	ATI_DVPCLK 74C3
NC_ATI_DVPCNTL<2..0>	MAKE_BASE=TRUE, NO_TEST=TRUE	ATI_DVPCNTL<2..0> 74B3 74C3
NC_ATI_DVPDATA<15..0>	MAKE_BASE=TRUE, NO_TEST=TRUE	ATI_DVPDATA<15..0> 74B3

Required for debug access

TP_ATI_DVPDATA<23..16> — MAKE_BASE=TRUE — ATI_DVPDATA<23..16> 74A3 74B3

Also required: GPIO10 - GPIO13

65A3 =PP3V3_D3C_GPU

R8890 4.7K 5% 1/16W MF-LF 402
R8891 4.7K 5% 1/16W MF-LF 402

75A3 GPU_DDC_B_CLK
75A3 GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
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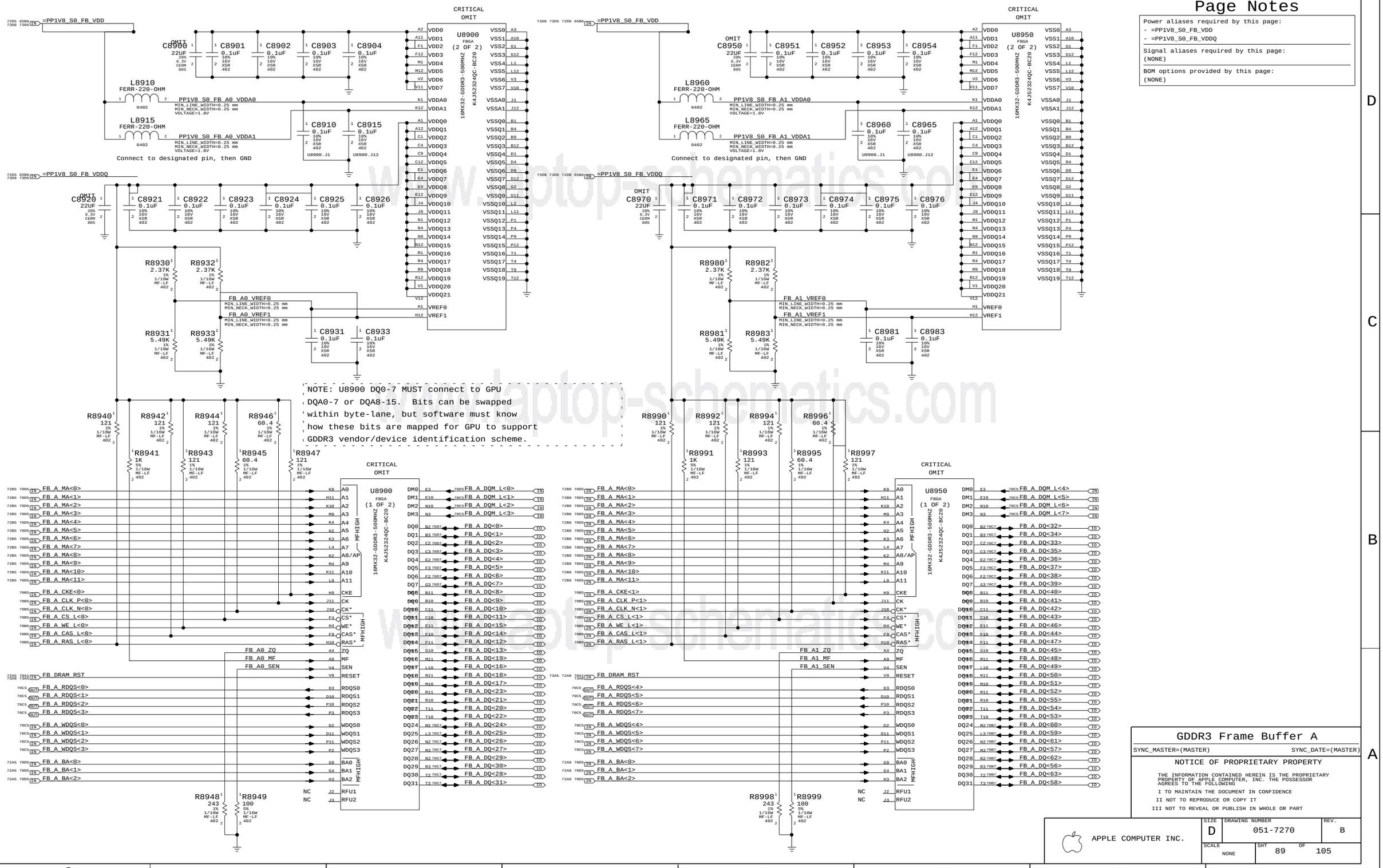

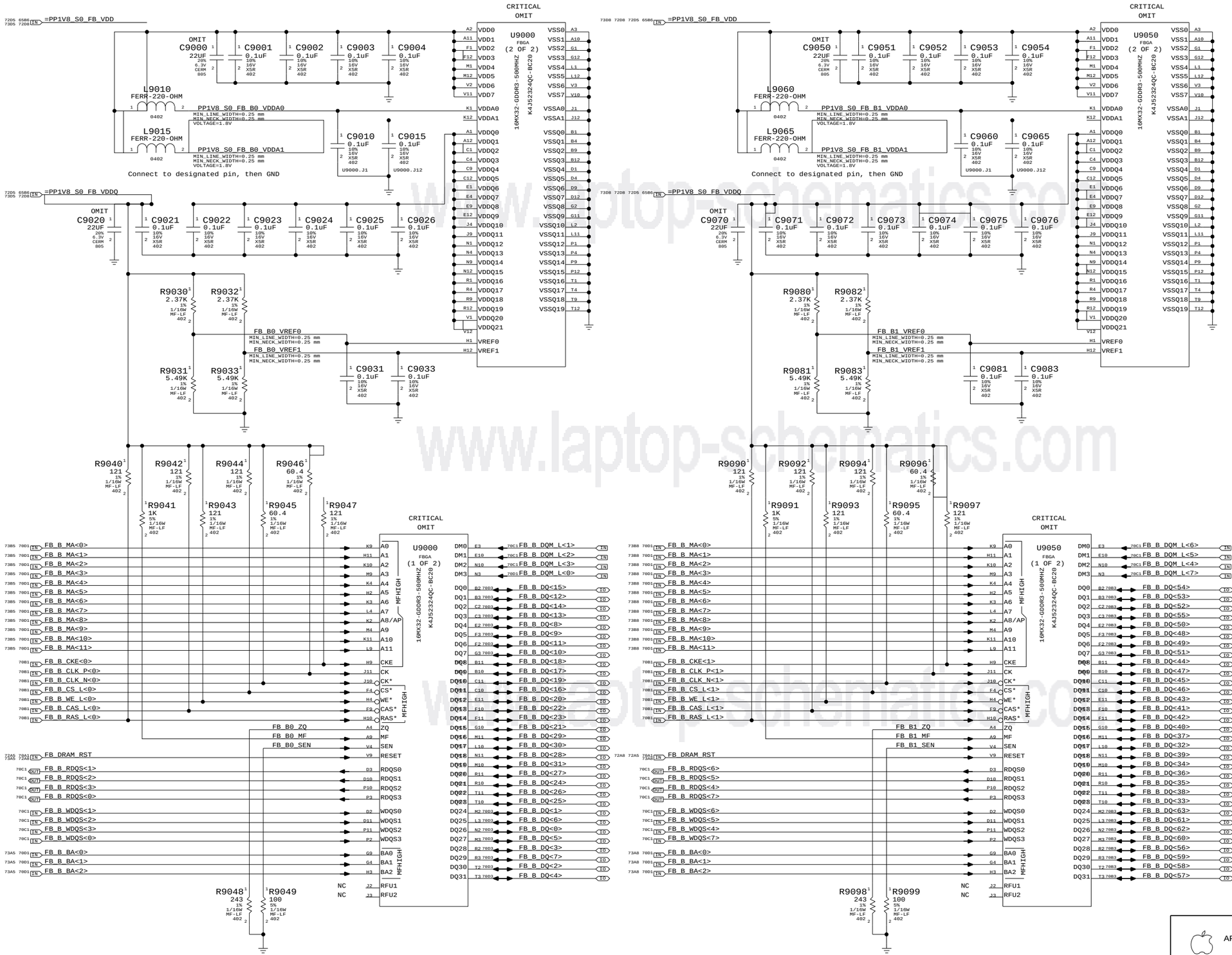

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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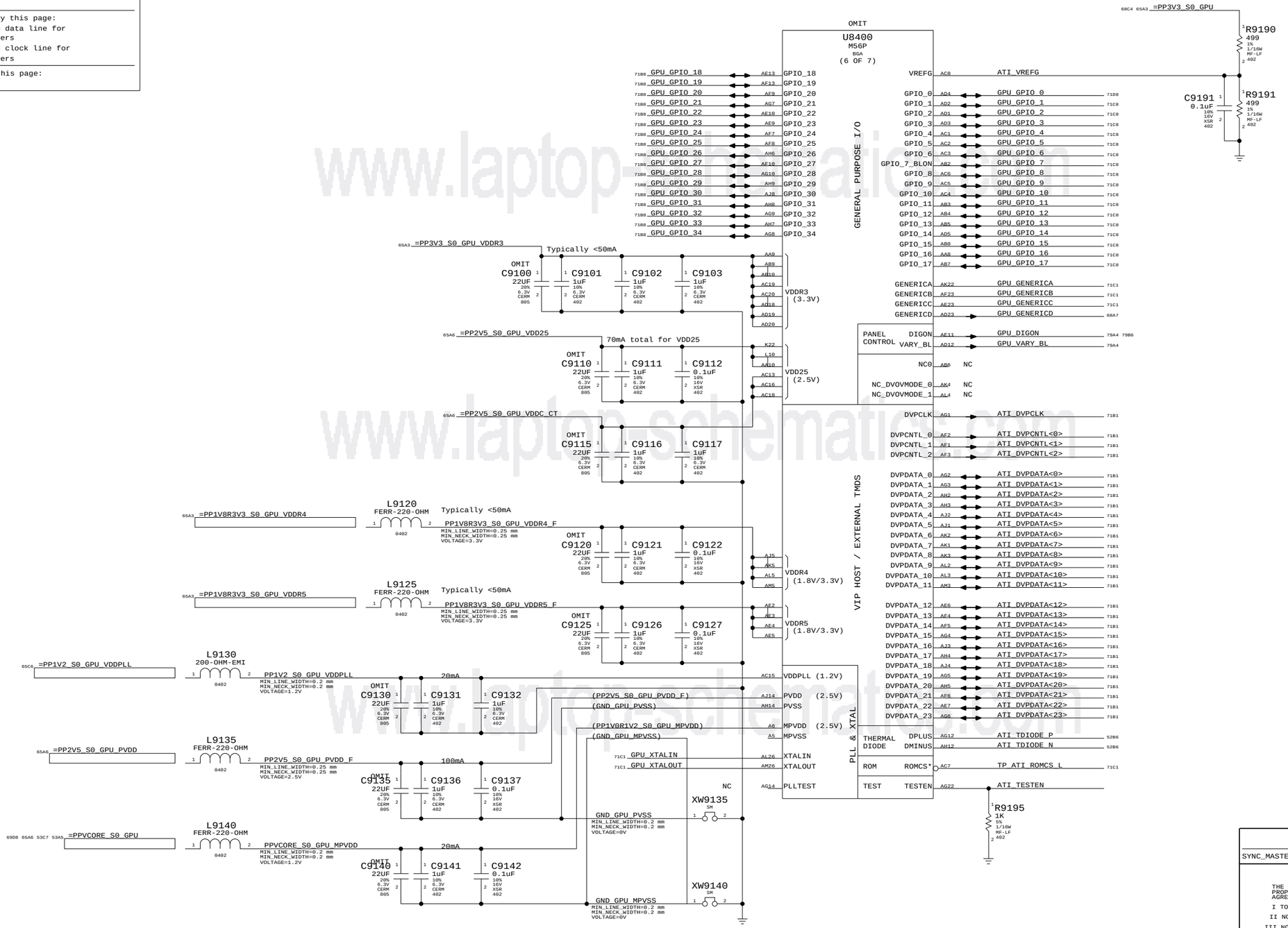
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 91 OF 105	

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

65A6 =PP2V5_S0_GPU

Sum of peak currents on this page: 605mA

L9300 FERR-220-OHM 0402 — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
OMIT C9300 22UF 20% 6.3V CERM 805
C9301 1uF 10% 6.3V CERM 402
C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 150mA peak
OMIT C9305 22UF 20% 6.3V CERM 805
C9306 1uF 10% 6.3V CERM 402
C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 65mA peak
OMIT C9310 22UF 20% 6.3V CERM 805
C9311 1uF 10% 6.3V CERM 402
C9312 0.1uF 10% 16V X5R 402

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
OMIT C9315 22UF 20% 6.3V CERM 805
C9316 1uF 10% 6.3V CERM 402
C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 130mA peak
OMIT C9320 22UF 20% 6.3V CERM 805
C9321 1uF 10% 6.3V CERM 402
C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
OMIT C9325 22UF 20% 6.3V CERM 805
C9326 1uF 10% 6.3V CERM 402
C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
OMIT C9330 22UF 20% 6.3V CERM 805
C9331 1uF 10% 6.3V CERM 402
C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 200mA peak
OMIT C9340 22UF 20% 6.3V CERM 805
OMIT C9345 22UF 20% 6.3V CERM 805
C9341 1uF 10% 6.3V CERM 402
C9342 0.1uF 10% 16V X5R 402
C9346 0.1uF 10% 16V X5R 402
C9347 0.1uF 10% 16V X5R 402

ATI_RSET 75A8 — R9350 499 1% 1/10W MF-LF 402
ATI_R2SET 75B5 — R9351 715 1% 1/10W MF-LF 402

OMIT U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
- AM8 TPVDD (2.5V)
- AL8 TPVSS
- AJ6, AK6, AL6, AM6 TXVDDR (2.5V)
- AJ7, AK7, AK8, AL7, AM7 TXVSSR
- AL25, AM25 AVDD (2.5V)
- AJ24, AK25 AVSS
- AK23 AVSSQ
- AM23 VDD1DI (2.5V)
- AL23 VSS1DI

DAC (CRT)
- 75A8 ATI_RSET → AL22 RSET
- AL16, AM16 A2VDD (2.5V)
- AL17, AM17 A2VSS
- NC AL14 NC_A2VDDQ
- AK13 A2VSSQ
- AJ16 VDD2DI (2.5V)
- AJ17 VSS2DI

DAC2 (TV/CRT2)
- 75A8 ATI_R2SET → AK14 R2SET

LVDS
- AE19 LPVDD (2.5V)
- AE18 LPVSS
- AC21, AC22, AD21, AD22, AE20, AE21, AE22, AE19, AF17, AF18 LVDDR (2.5V)
- AE29, AF21, AF22, AG17, AG19, AH17, AH19, AJ19, AK17 LVSSR

MONITOR IDENTIFICATION
- 77A1 GPU_HPD → AE11 HPD1

TXCP	AM9	TMDS_CLK_P	OUT
TXCM	AL9	TMDS_CLK_N	OUT
TX0P	AL10	TMDS_DATA_P<0>	OUT
TX0M	AK10	TMDS_DATA_N<0>	OUT
TX1P	AM11	TMDS_DATA_P<1>	OUT
TX1M	AL11	TMDS_DATA_N<1>	OUT
TX2P	AM12	TMDS_DATA_P<2>	OUT
TX2M	AL12	TMDS_DATA_N<2>	OUT
TX3P	AJ9	TMDS_DATA_P<3>	OUT
TX3M	AK9	TMDS_DATA_N<3>	OUT
TX4P	AJ11	TMDS_DATA_P<4>	OUT
TX4M	AK11	TMDS_DATA_N<4>	OUT
TX5P	AJ12	TMDS_DATA_P<5>	OUT
TX5M	AK12	TMDS_DATA_N<5>	OUT
R	AK24	GPU_VGA_R	OUT
G	AM24	GPU_VGA_G	OUT
B	AL24	GPU_VGA_B	OUT
HSYNC	AJ23	GPU_VGA_HSYNC	OUT
VSYNC	AJ22	GPU_VGA_VSYNC	OUT
R2	AK15	GPU_R2	OUT
G2	AM15	GPU_G2	OUT
B2	AL15	GPU_B2	OUT
H2SYNC	AE15	GPU_H2SYNC	OUT
V2SYNC	AG15	GPU_V2SYNC	OUT
Y	AJ15	GPU_TV_Y	OUT
C	AJ13	GPU_TV_C	OUT
COMP	AH15	GPU_TV_COMP	OUT
TXCLK_UP	AJ21	LVDS_U_CLK_P	OUT
TXCLK_UN	AK21	LVDS_U_CLK_N	OUT
TXOUT_U0P	AG18	LVDS_U_DATA_P<0>	OUT
TXOUT_U0N	AH18	LVDS_U_DATA_N<0>	OUT
TXOUT_U1P	AK20	LVDS_U_DATA_P<1>	OUT
TXOUT_U1N	AJ20	LVDS_U_DATA_N<1>	OUT
TXOUT_U2P	AG20	LVDS_U_DATA_P<2>	OUT
TXOUT_U2N	AH20	LVDS_U_DATA_N<2>	OUT
TXOUT_U3P	AH21	LVDS_U_DATA_P<3>	OUT
TXOUT_U3N	AG21	LVDS_U_DATA_N<3>	OUT
TXCLK_LP	AM18	LVDS_L_CLK_P	OUT
TXCLK_LN	AL18	LVDS_L_CLK_N	OUT
TXOUT_L0P	AL19	LVDS_L_DATA_P<0>	OUT
TXOUT_L0N	AK19	LVDS_L_DATA_N<0>	OUT
TXOUT_L1P	AM20	LVDS_L_DATA_P<1>	OUT
TXOUT_L1N	AL20	LVDS_L_DATA_N<1>	OUT
TXOUT_L2P	AM21	LVDS_L_DATA_P<2>	OUT
TXOUT_L2N	AL21	LVDS_L_DATA_N<2>	OUT
TXOUT_L3P	AJ18	LVDS_L_DATA_P<3>	OUT
TXOUT_L3N	AK18	LVDS_L_DATA_N<3>	OUT
DDC1CLK	AH23	GPU_DDC_A_CLK	IO
DDC1DATA	AH22	GPU_DDC_A_DATA	IO
DDC2CLK	AG13	GPU_DDC_B_CLK	IO
DDC2DATA	AH13	GPU_DDC_B_DATA	IO
DDC3CLK	AE12	GPU_DDC_C_CLK	IO
DDC3DATA	AE12	GPU_DDC_C_DATA	IO

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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D	051-7270	B
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LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
	VGA	VGA	GPU_R2	75B3 77C3
	VGA	VGA	GPU_G2	75B3 77C3
	VGA	VGA	GPU_B2	75B3 77C3
	LVDS	LVDS	LVDS_U_CLK_P	75B3 79C3
	LVDS	LVDS	LVDS_U_CLK_N	75B3 79C3
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	75B3 79B3 79C3
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	75B3 79C3
	LVDS	LVDS	LVDS_L_CLK_P	75A3 79C3
	LVDS	LVDS	LVDS_L_CLK_N	75A3 79C3
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	75A3 79C3
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	75A3 79C3
	LVDS	LVDS	LVDS_U_CLK_CONN_P	6B1 76B2 79C1
	LVDS	LVDS	LVDS_U_CLK_CONN_N	6B1 76B2 79C1
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>	6B1 76B2 76C2 79C1 79D1
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>	6B1 76C2 79C1 79D1
	LVDS	LVDS	LVDS_L_CLK_CONN_P	6B1 76C2 79C1
	LVDS	LVDS	LVDS_L_CLK_CONN_N	6B1 76C2 79C1
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>	6A1 6B1 76C2 79C1
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>	6A1 76C2 79C1
	TMDS	TMDS	TMDS_CLK_P	75C3 77B8 84B4
	TMDS	TMDS	TMDS_CLK_N	75C3 77C8 84B4
	TMDS	TMDS	TMDS_DATA_P<5..3>	75C3 77A8 77B8 84A4
	TMDS	TMDS	TMDS_DATA_N<5..3>	75C3 77A8 77B8 84A4
	TMDS	TMDS	TMDS_DATA_P<2..0>	75C3 77C8 77D8 84A4
	TMDS	TMDS	TMDS_DATA_N<2..0>	75C3 77C8 77D8 84A4

65C3 =PP3V3_S0_LCD

R9400 100K 5% 1/10W MF-LF 402

C9400 0.0022uF 10% 50V CERM 402

R9401 100K 5% 1/16W MF-LF 402

LCD_PWREN_L_RC

LCD_PWREN_L

Q9400 SI3443DV TSOP-LF

86 PP3V3_LCD_SW MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=3.3V

L9400 FERR-250-OHM SM

C9401 0.001uF 20% 50V CERM 402

6A6 =GND_CHASSIS_LCD2

6A6 =GND_CHASSIS_LCD1

CRITICAL J9400 MSC-RB30-5-FA F-RT-SM

C9420 0.001uF 20% 50V CERM 402

79A2 LVDS_PANEL_EN

Q9401 2N7002 SOT23-LF

R9494 100K 5% 1/16W MF-LF 402

65B3 =PP3V3_S0_DDC_LCD

100K pull-ups are for no-panel case (development). Panel has 2K pull-ups

R9410 100K 5% 1/16W MF-LF 402

R9411 100K 5% 1/16W MF-LF 402

PP3V3_LCD_CONN MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=3.3V

NC

79A5 LVDS_CONN_DDC_CLK

79A5 LVDS_CONN_DDC_DATA

C9410 0.001uF 20% 50V CERM 402

6A6 =GND_CHASSIS_LCD3

79C1 76D7 6A1 LVDS_L_DATA_CONN_N<0>

79C1 76D7 6B1 LVDS_L_DATA_CONN_P<0>

79C1 76D7 6A1 LVDS_L_DATA_CONN_N<1>

79C1 76D7 6A1 LVDS_L_DATA_CONN_P<1>

79C1 76D7 6A1 LVDS_L_DATA_CONN_N<2>

79C1 76D7 6A1 LVDS_L_DATA_CONN_P<2>

79C1 76D7 6B1 LVDS_L_CLK_CONN_N

79C1 76D7 6B1 LVDS_L_CLK_CONN_P

79D1 76D7 6B1 LVDS_U_DATA_CONN_N<0>

79D1 76D7 6B1 LVDS_U_DATA_CONN_P<0>

79C1 76D7 6B1 LVDS_U_DATA_CONN_N<1>

79C1 76D7 6B1 LVDS_U_DATA_CONN_P<1>

79D1 76D7 6B1 LVDS_U_DATA_CONN_N<2>

79C1 76D7 6B1 LVDS_U_DATA_CONN_P<2>

79C1 76D7 6B1 LVDS_U_CLK_CONN_N

79C1 76D7 6B1 LVDS_U_CLK_CONN_P

C9421 0.001uF 20% 50V CERM 402

518S0289

6A6 =GND_CHASSIS_LCD4

INVERTER INTERFACE

65C1 =PPBUS_S0_INVERTER

CRITICAL L9450 FERR-220-OHM-2A 0603

5A4 PPBUS_S0_INVERTER MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=12.8V

C9450 0.001uF 20% 50V CERM 402

65A1 =PP5V_S0_INVERTER

Q9450 FDG6332C_NL SC70-6 P-CHN

R9450 100K 5% 1/16W MF-LF 402

PP5V_INVERTER_SW_F MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V

L9452 400-OHM-EMI SM-1

C9451 10UF 20% 6.3V XSR 603

FP_PWR_EN_L

5A4 PP5V_INVERTER_SW MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V

CRITICAL J9450 SM04B-ACH M-RT-SM

NC

NC

518S0369

79A2 INVERTER_BKLTON

Q9450 FDG6332C_NL SC70-6 N-CHN

R9489 100K 5% 1/16W MF-LF 402

C9452 0.001uF 20% 50V CERM 402

L9454 400-OHM-EMI SM-1

5A3 INVERTER_PWM

5A4 GND_INVERTER

C9454 0.001uF 20% 50V CERM 402

CRITICAL L9455 FERR-220-OHM-2A 0603

6A6 =GND_CHASSIS_INVERTER

65B3 =PP3V3_S0_INVERTER

6C4 =INVERTER_PWM_PLT_RST_L

79A2 INVERTER_PWM_UNBUF

U9453 MC74VHC1G08 SC70

INVERTER_PWM_F

INVERTER EXPECTS ACTIVE HIGH PWM SIGNAL

C9453 0.1uF 20% 10V CERM 402

Internal Display Connectors

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

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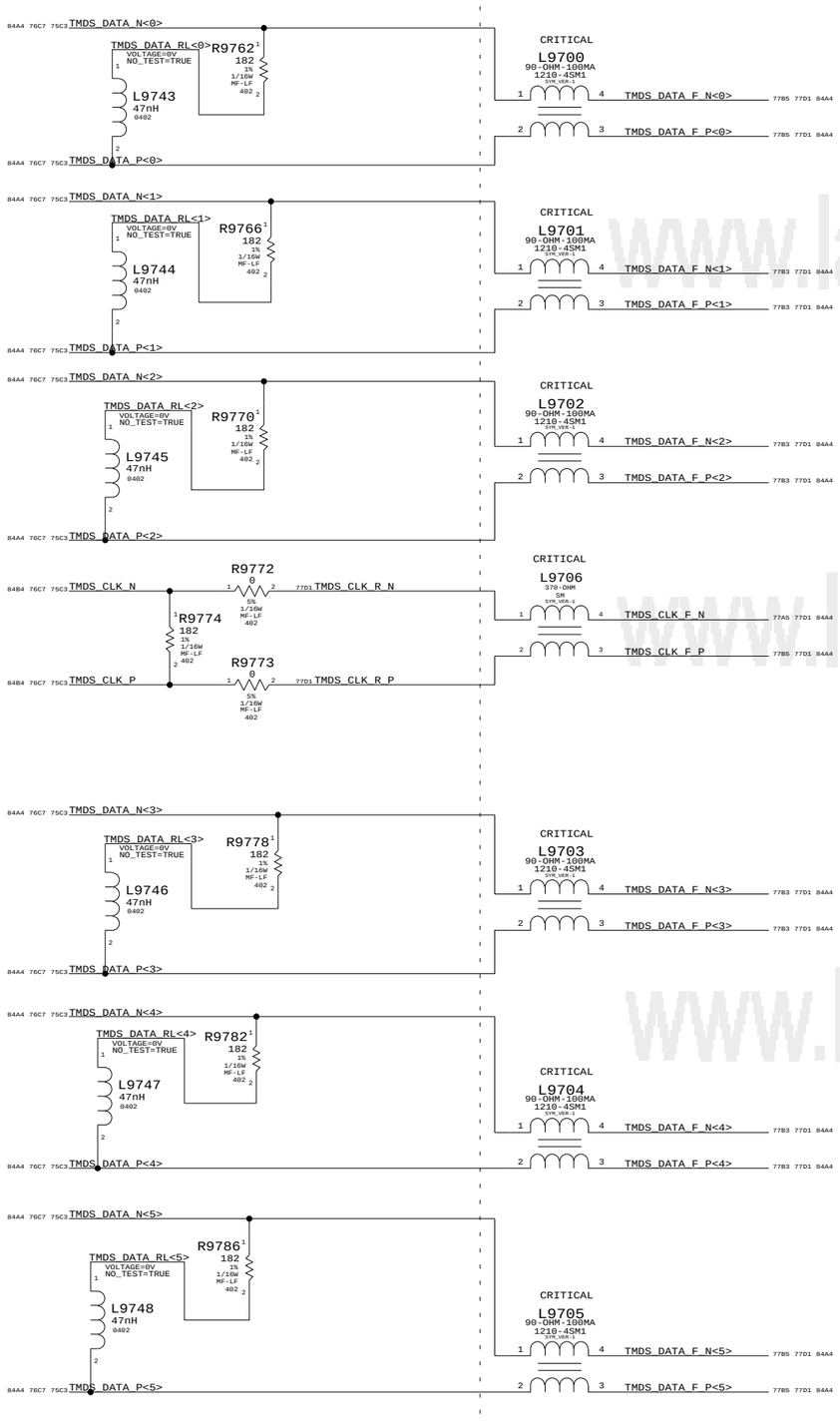
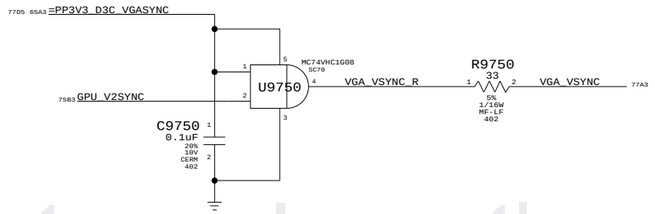
D	051-7270	B
SCALE: NONE	SHT 94 OF 105	

TMDS Filtering

Place termination components close to GPU, common mode chokes near connector.

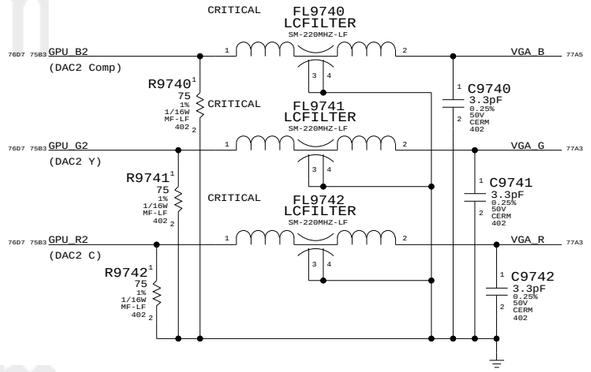


VGA SYNC BUFFERS



ANALOG FILTERING

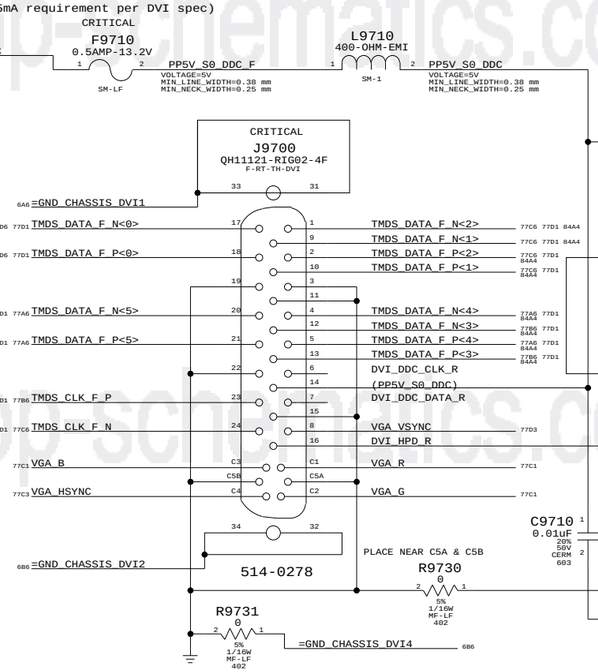
PLACE CLOSE TO CONNECTOR



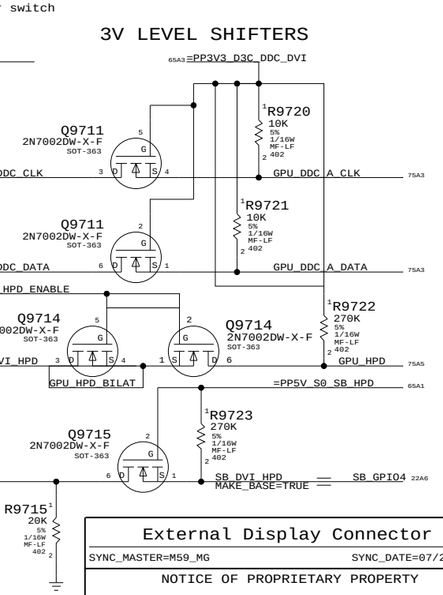
DVI INTERFACE

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)



3V LEVEL SHIFTERS



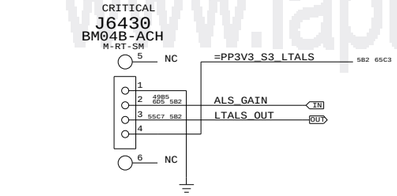
NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	
TMDS	TMDS	TMDS_CLK_R_P	77B7
TMDS	TMDS	TMDS_CLK_R_N	77C7
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	77B5 77B6 84A4
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	77A5 77C6 84A4
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..0>	77A6 77B3 77B5 77B6 77C6 77D6 84A4
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..0>	77A6 77B3 77B5 77B6 77C6 77D6 84A4

External Display Connector

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7270	B
	SCALE: NONE	SHT 97 OF 105	

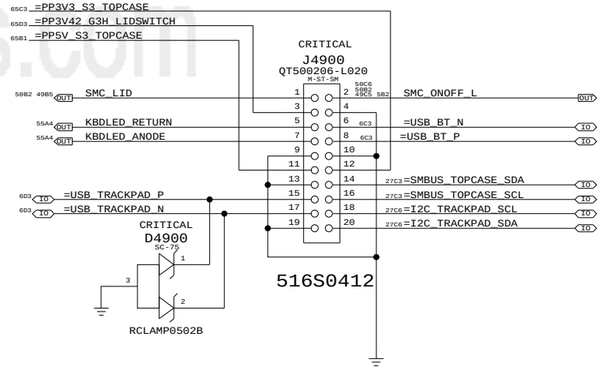
Left ALS Connector



518S0469

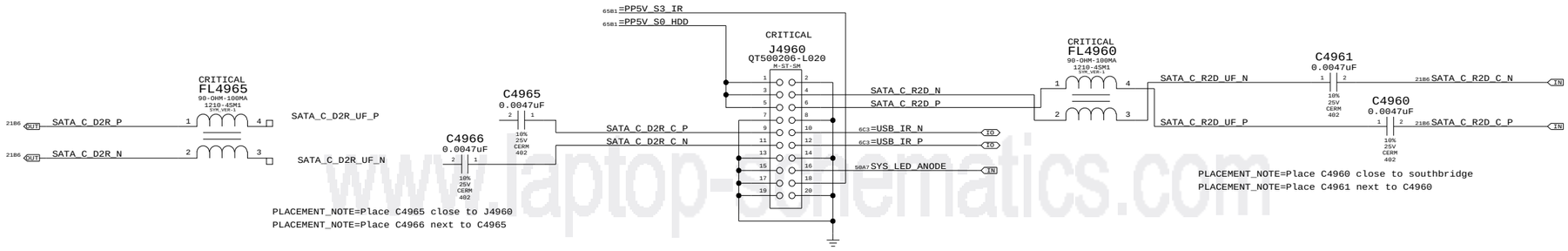
white colored version of 518S0369

Top-Case Connector



516S0412

SATA HDD & IR & SIL Flex Connector



PLACEMENT_NOTE=Place C4965 close to J4960

PLACEMENT_NOTE=Place C4966 next to C4965

PLACEMENT_NOTE=Place C4960 close to southbridge

PLACEMENT_NOTE=Place C4961 next to C4960

516S0412

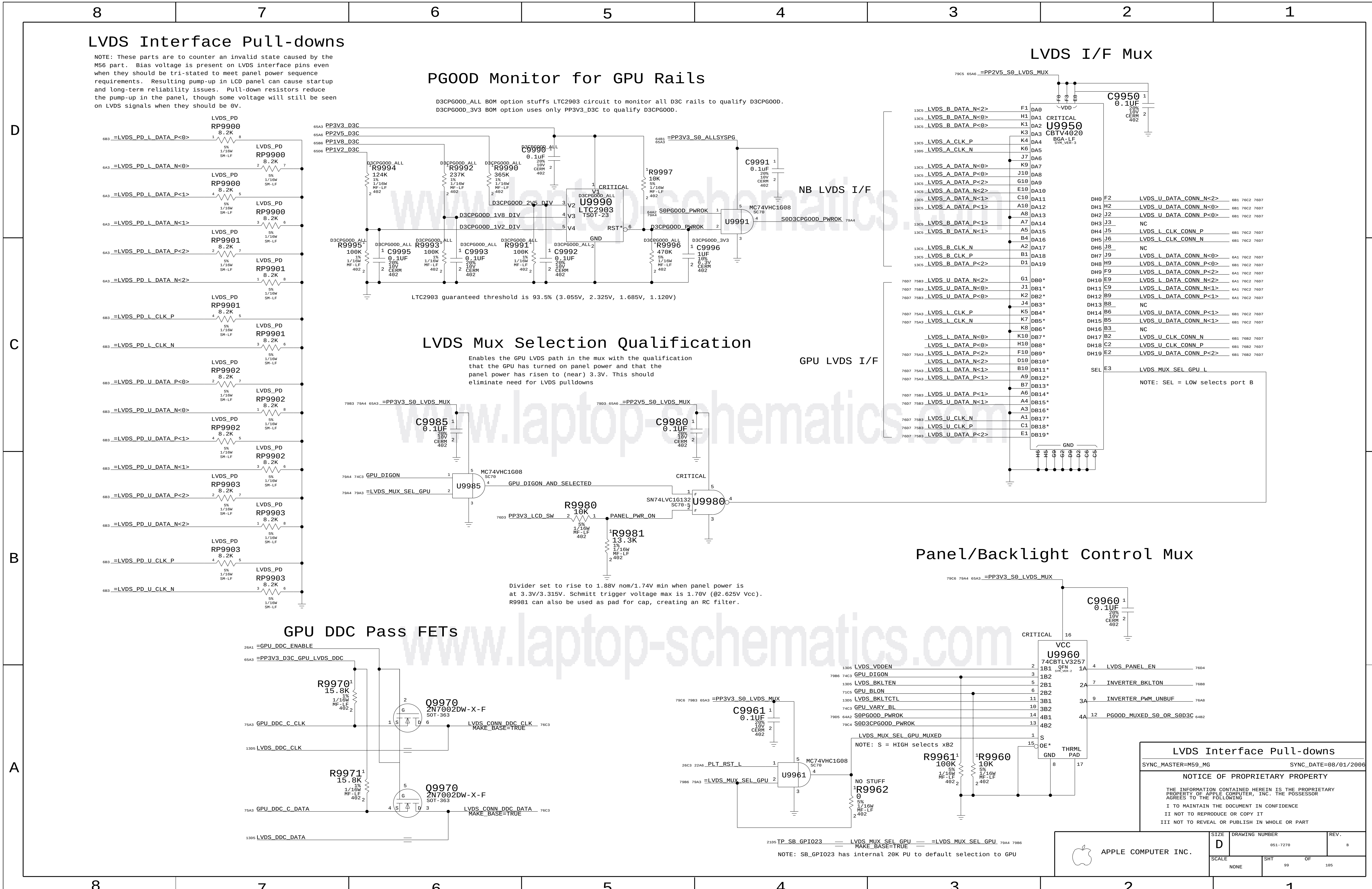
NOTE: _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

M59 Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 98 OF 105	



LVDS Interface Pull-downs
NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.
PGOOD Monitor for GPU Rails
D3CPGOOD_ALL BOM option stuffs LTC2903 circuit to monitor all D3C rails to qualify D3CPGOOD.
D3CPGOOD_3V3 BOM option uses only PP3V3_D3C to qualify D3CPGOOD.
LTC2903 guaranteed threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)
NB LVDS I/F
LVDS I/F Mux
GPU LVDS I/F
NOTE: SEL = LOW selects port B
LVDS Mux Selection Qualification
Enables the GPU LVDS path in the mux with the qualification that the GPU has turned on panel power and that the panel power has risen to (near) 3.3V. This should eliminate need for LVDS pulldowns
Divider set to rise to 1.88V nom/1.74V min when panel power is at 3.3V/3.315V. Schmitt trigger voltage max is 1.70V (@2.625V Vcc). R9981 can also be used as pad for cap, creating an RC filter.
Panel/Backlight Control Mux
NOTE: S = HIGH selects xB2
GPU DDC Pass FETs
NOTE: SB_GPIO23 has internal 20K PU to default selection to GPU
LVDS Interface Pull-downs
SYNC_MASTER=M59_MG
SYNC_DATE=08/01/2006
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APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7270
REV. 8
SCALE NONE
SHT 99 OF 105

Date	- Radar # - Description

DMS Release #01000

2006/05/26 - 4508681 - Release for Proto

DMS Release #04000

2006/06/30 - 4566939 - Release for EVT

DMS Release #07000

2006/08/07 - 4607952 - Release for DVT

DMS Release #0A000

2006/09/19 - 4726575 - Release for PVT

DMS Release #0C000

2006/09/27 - 4726575 - Release for PVT

B

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE	SHT	OF
NONE	100	105

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	
FSB_ADDR2ADDR	*	=2:1_SPACING	
FSB_ADSTB	*	=3:1_SPACING	
FSB_ADDR2ADSTB	*	=3:1_SPACING	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	
FSB_DATA2DATA	*	=2:1_SPACING	
FSB_DSTB	*	=3:1_SPACING	
FSB_DATA2DSTB	*	=3:1_SPACING	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	
CPU_COMP	*	25 MIL	
CPU_GTLREF	*	25 MIL	
CPU_ITP	*	=2:1_SPACING	
CPU_VCCSENSE	*	25 MIL	

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	
MEM_CTRL2CTRL	*	=2:1_SPACING	
MEM_CTRL2MEM	*	=3:1_SPACING	
MEM_CMD2CMD	*	=1.5:1_SPACING	
MEM_CMD2MEM	*	=3:1_SPACING	
MEM_DATA2DATA	*	=1.5:1_SPACING	
MEM_DATA2MEM	*	=3:1_SPACING	
MEM_DQS2MEM	*	=3:1_SPACING	
MEM_2OTHER	*	25 MIL	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	
DMI	*	20 MIL	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	
SATA	*	20 MIL	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	
USB2_2CLK	*	25 MIL	

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	
SPI	*	=1.8:1_SPACING	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	
CLK_PCIE	*	20 MIL	
CLK_MED	*	20 MIL	
CLK_SLOW	*	10 MIL	

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE	SHT	OF
NONE	101	105

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_3SS_TO_5SS	*	Y	=3S_OHM_SE	=5S_OHM_SE	=3S_5S_OHM_SE	=STANDARD	=STANDARD
FB_4QS	*	Y	=4Q_OHM_SE	=4Q_OHM_SE	=4Q_OHM_SE	=STANDARD	=STANDARD
FB_5SS	*	Y	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	
FB_CLK	*	=2.5:1_SPACING	
FB_DATA	*	=2.5:1_SPACING	

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	=3:1_SPACING	
TMDS	*	=3:1_SPACING	
VGA	*	15 MIL	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS_PAIR2PAIR	*	25 MIL	
TMDS_PAIR2PAIR	*	25 MIL	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET	*	=3:1_SPACING	
FW	*	=3:1_SPACING	

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5SS	*	Y	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	

More System Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE NONE SHT 102 OF 105

M59 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	
STANDARD	*	=DEFAULT	
BGA_P1MM	*	=DEFAULT	
BGA_P2MM	*	=DEFAULT	
BGA_P3MM	*	=DEFAULT	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	
1.8:1_SPACING	*	0.18 MM	
2:1_SPACING	*	0.2 MM	
2.5:1_SPACING	*	0.25 MM	
3:1_SPACING	*	0.3 MM	
4:1_SPACING	*	0.4 MM	

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2,ISL11	0.1 MM	
1.8:1_SPACING	ISL2,ISL11	0.1 MM	
2:1_SPACING	ISL2,ISL11	0.1 MM	
2.5:1_SPACING	ISL2,ISL11	0.1 MM	
3:1_SPACING	ISL2,ISL11	0.1 MM	
4:1_SPACING	ISL2,ISL11	0.1 MM	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2,ISL11	0.1 MM	
CLK_PCIE	ISL2,ISL11	0.1 MM	
CLK_MED	ISL2,ISL11	0.1 MM	
CLK_SLOW	ISL2,ISL11	0.1 MM	
CPU_COMP	ISL2,ISL11	0.1 MM	
CPU_GTLREF	ISL2,ISL11	0.1 MM	
CPU_VCCSENSE	ISL2,ISL11	0.1 MM	
DMI	ISL2,ISL11	0.1 MM	
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	
MEM_2OTHER	ISL2,ISL11	0.1 MM	
PCIE	ISL2,ISL11	0.1 MM	
SATA	ISL2,ISL11	0.1 MM	
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	
VGA	ISL2,ISL11	0.1 MM	

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_5SS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_4SS OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_7OD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_8SD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M59 Spacing & Physical Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B

SCALE NONE SHT 103 OF 105

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5D5 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BNR_L	5D5 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5D5 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7B3 12B4
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HIT_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HITM_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7D6 11B5 12C4
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5D5 7B3 7B4 7C3 7C4 12B6 12C6 12D6
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5D5 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5D5 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5D5 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5D5 7C8 7D8 12C4 12D4
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5D5 7D8 12A4 12B4
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5D5 7C8 7D8 12C4
	CPU_55S		FSB_IERR_L	7D6
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7B3 21C4
	CPU_55S		CPU_INTR	7C8 21C4
	CPU_55S		CPU_NMI	7C8 21C4
	CPU_55S		CPU_A20M_L	7C8 21C4
	CPU_55S		CPU_DPSLP_L	7B3 21C4
	CPU_55S		CPU_IGNNE_L	7C8 21C4
	CPU_55S		CPU_INIT_L	7D6 21C4
	CPU_55S		CPU_SMI_L	7C8 21C4
	CPU_55S		CPU_STPCLK_L	7C8 21C4
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	14B7 23C3 59C8
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	59C7
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7B4
	CPU_55S	CPU_COMP	CPU_COMP<3>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7B3
	CPU_55S	CPU_COMP	CPU_COMP<1>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7B3
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7C6 11B3
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11B3 34D3
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11B3 34D3
	CPU_55S	CPU_ITP	ITPRESET_L	11B3
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 84B6
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 84B6
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8B6 59B1
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8B6 59A1
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	59A3
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	59A3

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21C6	
AUDIO_55S	AUDIO	ACZ_BITCLK	5C1 21C7 47B6	
AUDIO_55S	AUDIO	SB_ACZ_SYNC	21C6	
AUDIO_55S	AUDIO	ACZ_SYNC	5C1 21C7 47B6	
AUDIO_55S	AUDIO	SB_ACZ_RST_L	21C6	
AUDIO_55S	AUDIO	ACZ_RST_L	5C1 21C7 47B3	
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5C1 21C7 47B6	
AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21C6	
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5C1 21C7 47B6	

TMDS	TMDS	TMDS_CLK_P	75C3 76C7 77B8	
TMDS	TMDS	TMDS_CLK_N	75C3 76C7 77C8	
TMDS	TMDS	TMDS_DATA_P<5..3>	75C3 76C7 77A8 77B8	
TMDS	TMDS	TMDS_DATA_N<5..3>	75C3 76C7 77A8 77B8	
TMDS	TMDS	TMDS_DATA_P<2..0>	75C3 76C7 77C8 77D8	
TMDS	TMDS	TMDS_DATA_N<2..0>	75C3 76C7 77C8 77D8	
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	77B5 77B6 77D1	
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	77A5 77C6 77D1	
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	77A6 77B3 77B5 77B6 77D1	
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	77A6 77B3 77B5 77B6 77D1	
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	77B3 77B5 77C6 77D1 77D6	
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	77B3 77B5 77C6 77D1 77D6	

M59 Net Properties

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 104 OF 105	

Low Acoustic Noise 22uF Ceramic Capacitor options

Samsung

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
138S0602	20	CAP,CER,22UF,20%,6.3V,X5R,0805		CRITICAL	CAP22UF_SAM_CRIT	CPU_VCORE
138S0602	2	CAP,CER,22UF,20%,6.3V,X5R,0805	C1934,C1936	CRITICAL	CAP22UF_SAM	PP1V5_30_NB_VCCA_PLL
138S0602	1	CAP,CER,22UF,20%,6.3V,X5R,0805	C5802	CRITICAL	CAP22UF_SAM	3V42_G3H
138S0602	8	CAP,CER,22UF,20%,6.3V,X5R,0805	C7616,C7617,C7650,C7651,C7671,C7672,C7696,C7696	CRITICAL	CAP22UF_SAM	5V_S0,5V_S5,1V5_NB,1V5_S0
138S0602	6	CAP,CER,22UF,20%,6.3V,X5R,0805	C7706,C7706,C7716,C7711,C7761,C7762	CRITICAL	CAP22UF_SAM	3V3_S5 (2V5_INPUT),2V5_S3,3V3_S3 (1V2_INPUT)
138S0602	4	CAP,CER,22UF,20%,6.3V,X5R,0805	C7716,C7706,C7706,C7706	CRITICAL	CAP22UF_SAM_CRIT	1V2_S3
138S0602	1	CAP,CER,22UF,20%,6.3V,X5R,0805	C7841	CRITICAL	CAP22UF_SAM	1V8_S3
138S0602	2	CAP,CER,22UF,20%,6.3V,X5R,0805	C7846,C7847	CRITICAL	CAP22UF_SAM	1V8_D3C
138S0602	2	CAP,CER,22UF,20%,6.3V,X5R,0805	C7940,C7941	CRITICAL	CAP22UF_SAM	3V3_S5
138S0602	2	CAP,CER,22UF,20%,6.3V,X5R,0805	C7985,C7986	CRITICAL	CAP22UF_SAM	1V05_S0
138S0602	1	CAP,CER,22UF,20%,6.3V,X5R,0805	C8015	CRITICAL	CAP22UF_SAM	3V42_G3H
138S0602	3	CAP,CER,22UF,20%,6.3V,X5R,0805	C8400,C8405,C8410	CRITICAL	CAP22UF_SAM_CRIT	GPU PCIE
138S0602	5	CAP,CER,22UF,20%,6.3V,X5R,0805	C8540,C8541,C8556,C8557,C8589	CRITICAL	CAP22UF_SAM_CRIT	GPU_VCORE,GPU_BB
138S0602	9	CAP,CER,22UF,20%,6.3V,X5R,0805	C8600,C8601,C8630,C8654,C8661,C8662,C8665,C8695,C8695	CRITICAL	CAP22UF_SAM_CRIT	GPU_CORE
138S0602	4	CAP,CER,22UF,20%,6.3V,X5R,0805	C8900,C8920,C8950,C8970	CRITICAL	CAP22UF_SAM_CRIT	VRAM_A
138S0602	4	CAP,CER,22UF,20%,6.3V,X5R,0805	C9000,C9020,C9050,C9070	CRITICAL	CAP22UF_SAM_CRIT	VRAM_B
138S0602	8	CAP,CER,22UF,20%,6.3V,X5R,0805	C9100,C9110,C9115,C9120,C9125,C9130,C9135,C9140	CRITICAL	CAP22UF_SAM	GPU_MISC
138S0602	9	CAP,CER,22UF,20%,6.3V,X5R,0805	C9300,C9305,C9310,C9315,C9320,C9325,C9330,C9340,C9345	CRITICAL	CAP22UF_SAM	GPU_VIDEO

Murata

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
138S0603	20	CAP,CER,22UF,20%,6.3V,X5R,0805		CRITICAL	CAP22UF_MURA_CRIT	CPU_VCORE
138S0603	2	CAP,CER,22UF,20%,6.3V,X5R,0805	C1934,C1936	CRITICAL	CAP22UF_MURA	PP1V5_30_NB_VCCA_PLL
138S0603	1	CAP,CER,22UF,20%,6.3V,X5R,0805	C5802	CRITICAL	CAP22UF_MURA	3V42_G3H
138S0603	8	CAP,CER,22UF,20%,6.3V,X5R,0805	C7616,C7617,C7650,C7651,C7671,C7672,C7696,C7696	CRITICAL	CAP22UF_MURA	5V_S0,5V_S5,1V5_NB,1V5_S0
138S0603	6	CAP,CER,22UF,20%,6.3V,X5R,0805	C7706,C7706,C7716,C7711,C7761,C7762	CRITICAL	CAP22UF_MURA	3V3_S5 (2V5_INPUT),2V5_S3,3V3_S3 (1V2_INPUT)
138S0603	4	CAP,CER,22UF,20%,6.3V,X5R,0805	C7716,C7706,C7706,C7706	CRITICAL	CAP22UF_MURA_CRIT	1V2_S3
138S0603	1	CAP,CER,22UF,20%,6.3V,X5R,0805	C7841	CRITICAL	CAP22UF_MURA	1V8_S3
138S0603	2	CAP,CER,22UF,20%,6.3V,X5R,0805	C7846,C7847	CRITICAL	CAP22UF_MURA	1V8_D3C
138S0603	2	CAP,CER,22UF,20%,6.3V,X5R,0805	C7940,C7941	CRITICAL	CAP22UF_MURA	3V3_S5
138S0603	2	CAP,CER,22UF,20%,6.3V,X5R,0805	C7985,C7986	CRITICAL	CAP22UF_MURA	1V05_S0
138S0603	1	CAP,CER,22UF,20%,6.3V,X5R,0805	C8015	CRITICAL	CAP22UF_MURA	3V42_G3H
138S0603	3	CAP,CER,22UF,20%,6.3V,X5R,0805	C8400,C8405,C8410	CRITICAL	CAP22UF_MURA_CRIT	GPU PCIE
138S0603	5	CAP,CER,22UF,20%,6.3V,X5R,0805	C8540,C8541,C8556,C8557,C8589	CRITICAL	CAP22UF_MURA_CRIT	GPU_VCORE,GPU_BB
138S0603	9	CAP,CER,22UF,20%,6.3V,X5R,0805	C8600,C8601,C8630,C8654,C8661,C8662,C8665,C8695,C8695	CRITICAL	CAP22UF_MURA_CRIT	GPU_CORE
138S0603	4	CAP,CER,22UF,20%,6.3V,X5R,0805	C8900,C8920,C8950,C8970	CRITICAL	CAP22UF_MURA_CRIT	VRAM_A
138S0603	4	CAP,CER,22UF,20%,6.3V,X5R,0805	C9000,C9020,C9050,C9070	CRITICAL	CAP22UF_MURA_CRIT	VRAM_B
138S0603	8	CAP,CER,22UF,20%,6.3V,X5R,0805	C9100,C9110,C9115,C9120,C9125,C9130,C9135,C9140	CRITICAL	CAP22UF_MURA	GPU_MISC
138S0603	9	CAP,CER,22UF,20%,6.3V,X5R,0805	C9300,C9305,C9310,C9315,C9320,C9325,C9330,C9340,C9345	CRITICAL	CAP22UF_MURA	GPU_VIDEO

Taiyo - non critical locations only

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
138S0606	2	CAP,CER,22UF,20%,6.3V,X5R,0805	C1934,C1936	CRITICAL	CAP22UF_TAIYO	PP1V5_30_NB_VCCA_PLL
138S0606	1	CAP,CER,22UF,20%,6.3V,X5R,0805	C5802	CRITICAL	CAP22UF_TAIYO	3V42_G3H
138S0606	8	CAP,CER,22UF,20%,6.3V,X5R,0805	C7616,C7617,C7650,C7651,C7671,C7672,C7696,C7696	CRITICAL	CAP22UF_TAIYO	5V_S0,5V_S5,1V5_NB,1V5_S0
138S0606	6	CAP,CER,22UF,20%,6.3V,X5R,0805	C7706,C7706,C7716,C7711,C7761,C7762	CRITICAL	CAP22UF_TAIYO	3V3_S5 (2V5_INPUT),2V5_S3,3V3_S3 (1V2_INPUT)
138S0606	1	CAP,CER,22UF,20%,6.3V,X5R,0805	C7841	CRITICAL	CAP22UF_TAIYO	1V8_S3
138S0606	2	CAP,CER,22UF,20%,6.3V,X5R,0805	C7846,C7847	CRITICAL	CAP22UF_TAIYO	1V8_D3C
138S0606	2	CAP,CER,22UF,20%,6.3V,X5R,0805	C7940,C7941	CRITICAL	CAP22UF_TAIYO	3V3_S5
138S0606	2	CAP,CER,22UF,20%,6.3V,X5R,0805	C7985,C7986	CRITICAL	CAP22UF_TAIYO	1V05_S0
138S0606	1	CAP,CER,22UF,20%,6.3V,X5R,0805	C8015	CRITICAL	CAP22UF_TAIYO	3V42_G3H
138S0606	8	CAP,CER,22UF,20%,6.3V,X5R,0805	C9100,C9110,C9115,C9120,C9125,C9130,C9135,C9140	CRITICAL	CAP22UF_TAIYO	GPU_MISC
138S0606	9	CAP,CER,22UF,20%,6.3V,X5R,0805	C9300,C9305,C9310,C9315,C9320,C9325,C9330,C9340,C9345	CRITICAL	CAP22UF_TAIYO	GPU_VIDEO

The vendors for 22uF ceramic capacitors are controlled on this page.
The main BOMs must choose a vendor for critical and non-critical locations.

BOM options for crit. loc.	BOM options for non-crit. loc.
CAP22UF_SAM_CRIT	CAP22UF_SAM
CAP22UF_MURA_CRIT	CAP22UF_MURA
	CAP22UF_TAIYO

Note: all caps have CRITICAL BOM options regardless of location.

22uF Capacitor BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7270	B
SCALE: NONE	SHT 105 OF 105	