1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,M1

05/16/2006

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
A		439877	PRODUCTION RELEASED	05/16/06	

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7155	1	SCHEM,MLB,M1	SCH	CRITICAL	
820-2056	1	PCBF,MLB,M1	PCB	CRITICAL	

DRAWING
TITLE=M1_MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue May 16 11:30:38 2006

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK
ENG APPD | MFG APPD
QA APPD | DESIGNER
RELEASE | SCALE: NONE

MATERIAL/FINISH NOTED AS APPLICABLE

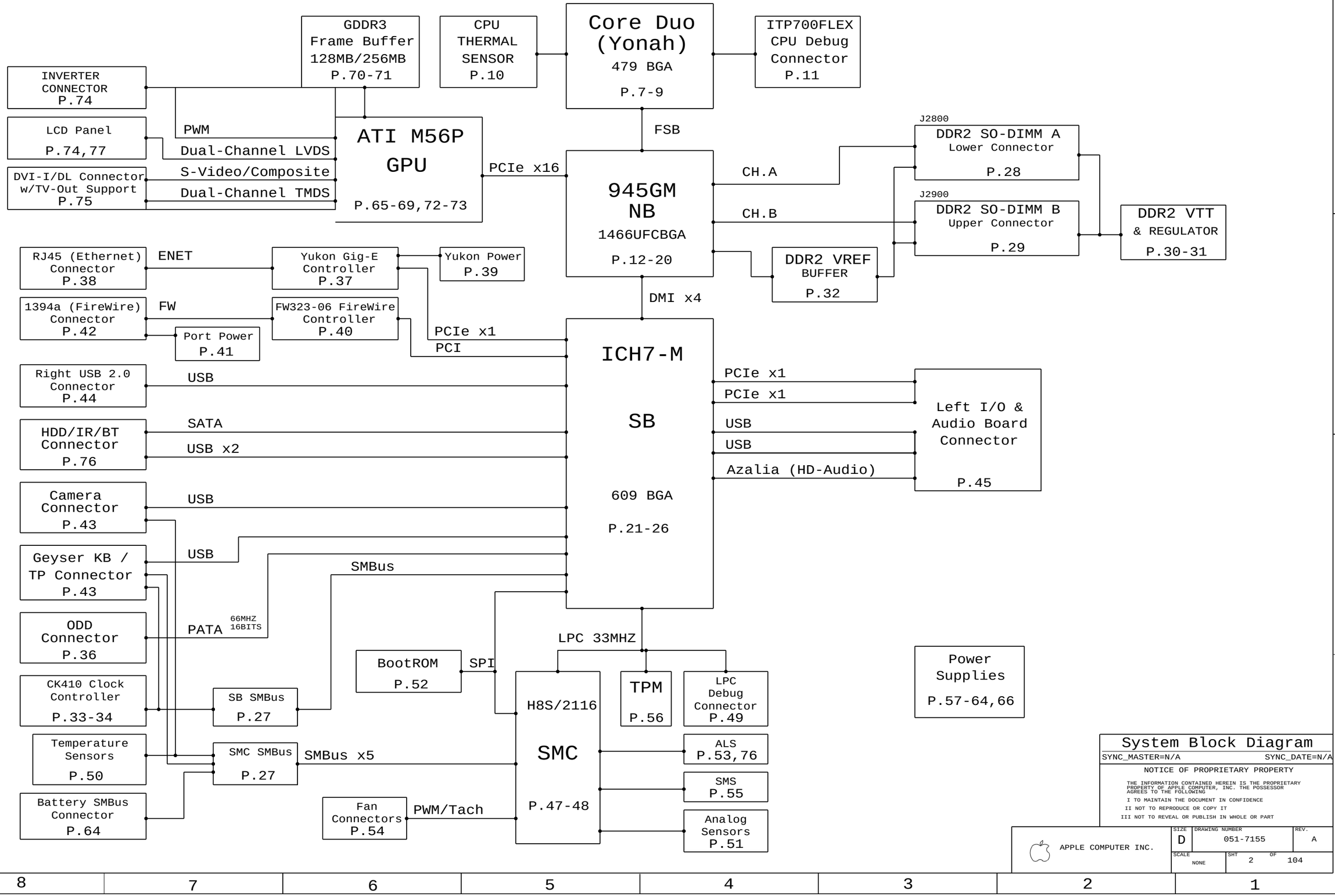
SIZE: D

Apple Computer Inc.

TITLE: SCHEM,MLB,M1

DRAWING NUMBER: 051-7155 | REV.: A

SHT 1 OF 104


GDDR3
Frame Buffer
128MB/256MB
P.70-71
CPU
THERMAL
SENSOR
P.10
Core Duo
(Yonah)
479 BGA
P.7-9
ITP700FLEX
CPU Debug
Connector
P.11
INVERTER
CONNECTOR
P.74
LCD Panel
P.74,77
DVI-I/DL Connector
w/TV-Out Support
P.75
PWM
Dual-Channel LVDS
S-Video/Composite
Dual-Channel TMDS
ATI M56P
GPU
P.65-69,72-73
PCIe x16
FSB
945GM
NB
1466UFCBGA
P.12-20
J2800
DDR2 SO-DIMM A
Lower Connector
P.28
J2900
DDR2 SO-DIMM B
Upper Connector
P.29
CH.A
CH.B
DDR2 VTT
& REGULATOR
P.30-31
DDR2 VREF
BUFFER
P.32
RJ45 (Ethernet)
Connector
P.38
ENET
Yukon Gig-E
Controller
P.37
Yukon Power
P.39
1394a (FireWire)
Connector
P.42
FW
FW323-06 FireWire
Controller
P.40
Port Power
P.41
PCIe x1
PCI
DMI x4
ICH7-M
SB
609 BGA
P.21-26
PCIe x1
PCIe x1
USB
USB
Azalia (HD-Audio)
Left I/O &
Audio Board
Connector
P.45
Right USB 2.0
Connector
P.44
USB
HDD/IR/BT
Connector
P.76
SATA
USB x2
Camera
Connector
P.43
USB
Geyser KB /
TP Connector
P.43
USB
SMBus
ODD
Connector
P.36
PATA
66MHZ
16BITS
LPC 33MHZ
BootROM
P.52
SPI
H8S/2116
SMC
P.47-48
TPM
P.56
LPC
Debug
Connector
P.49
Power
Supplies
P.57-64,66
CK410 Clock
Controller
P.33-34
SB SMBus
P.27
Temperature
Sensors
P.50
SMC SMBus
P.27
SMBus x5
Battery SMBus
Connector
P.64
Fan
Connectors
P.54
PWM/Tach
ALS
P.53,76
SMS
P.55
Analog
Sensors
P.51
System Block Diagram
SYNC_MASTER=N/A
SYNC_DATE=N/A
NOTICE OF PROPRIETARY PROPERTY
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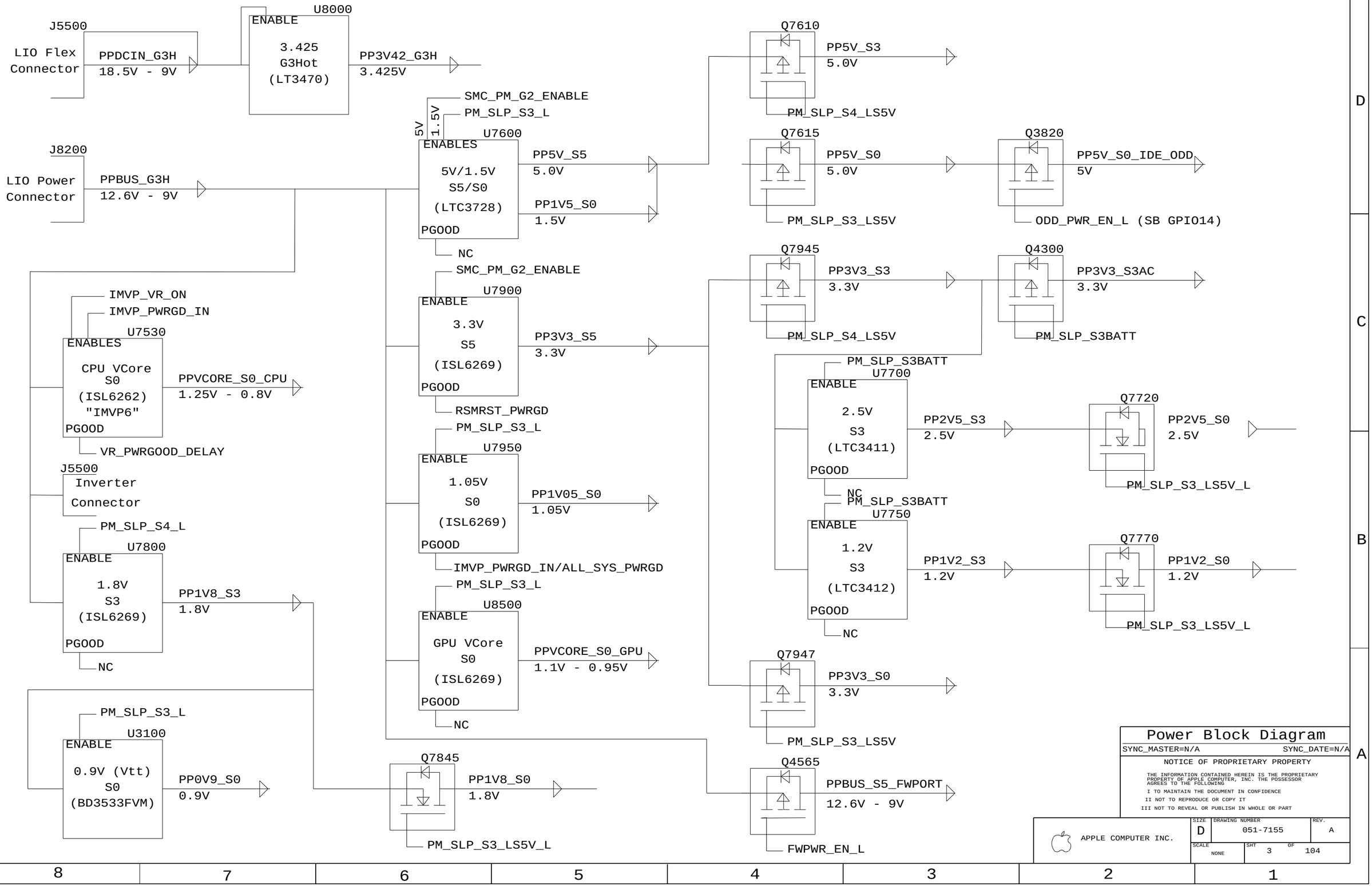
J5500
LIO Flex Connector
PPDCIN_G3H
18.5V - 9V
U8000
ENABLE
3.425 G3Hot (LT3470)
PP3V42_G3H
3.425V
J8200
LIO Power Connector
PPBUS_G3H
12.6V - 9V
SMC_PM_G2_ENABLE
PM_SLP_S3_L
5V
1.5V
U7600
ENABLES
5V/1.5V S5/S0 (LTC3728)
PGOOD
PP5V_S5
5.0V
PP1V5_S0
1.5V
NC
Q7610
PP5V_S3
5.0V
PM_SLP_S4_LS5V
Q7615
PP5V_S0
5.0V
PM_SLP_S3_LS5V
Q3820
PP5V_S0_IDE_ODD
5V
ODD_PWR_EN_L (SB GPIO14)
IMVP_VR_ON
IMVP_PWRGD_IN
U7530
ENABLES
CPU VCore S0 (ISL6262) "IMVP6"
PGOOD
PPVCORE_S0_CPU
1.25V - 0.8V
VR_PWRGOOD_DELAY
SMC_PM_G2_ENABLE
U7900
ENABLE
3.3V S5 (ISL6269)
PGOOD
PP3V3_S5
3.3V
RSMRST_PWRGD
PM_SLP_S3_L
U7950
ENABLE
1.05V S0 (ISL6269)
PGOOD
PP1V05_S0
1.05V
IMVP_PWRGD_IN/ALL_SYS_PWRGD
PM_SLP_S3_L
U8500
ENABLE
GPU VCore S0 (ISL6269)
PGOOD
PPVCORE_S0_GPU
1.1V - 0.95V
NC
Q7945
PP3V3_S3
3.3V
PM_SLP_S4_LS5V
Q4300
PP3V3_S3AC
3.3V
PM_SLP_S3BATT
PM_SLP_S3BATT
U7700
ENABLE
2.5V S3 (LTC3411)
PGOOD
PP2V5_S3
2.5V
Q7720
PP2V5_S0
2.5V
PM_SLP_S3_LS5V_L
NC
PM_SLP_S3BATT
U7750
ENABLE
1.2V S3 (LTC3412)
PGOOD
PP1V2_S3
1.2V
Q7770
PP1V2_S0
1.2V
PM_SLP_S3_LS5V_L
NC
J5500
Inverter Connector
PM_SLP_S4_L
U7800
ENABLE
1.8V S3 (ISL6269)
PGOOD
PP1V8_S3
1.8V
NC
PM_SLP_S3_L
U3100
ENABLE
0.9V (Vtt) S0 (BD3533FVM)
PP0V9_S0
0.9V
Q7845
PP1V8_S0
1.8V
PM_SLP_S3_LS5V_L
Q7947
PP3V3_S0
3.3V
PM_SLP_S3_LS5V
Q4565
PPBUS_S5_FWPORT
12.6V - 9V
FWPWR_EN_L
Power Block Diagram
SYNC_MASTER=N/A
SYNC_DATE=N/A
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"Better" BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7684	PCBA,2.0GHZ,128VRAM,M1-CAP_MBP15	EEE_VWP,M1_COMMON,CPU_2_0GHZ,VRAM_SAM128

"Best" BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7685	PCBA,2.16GHZ,256VRAM,M1-CAP_MBP15	EEE_VWQ,M1_COMMON,CPU_2_16GHZ,VRAM_SAM256

Service BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7704	PCBA,1.83GHZ,128VRAM,M1-CAP_MBP15	EEE_W36,M1_COMMON,CPU_1_83GHZ,VRAM_SAM128
630-7705	PCBA,2.0GHZ,256VRAM,M1-CAP_MBP15	EEE_W37,M1_COMMON,CPU_2_0GHZ,VRAM_SAM256

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M1_COMMON	ALTERNATE,COMMON,M1_COMMON1,M1_COMMON2,M1_COMMON3
M1_COMMON1	ATI_REV_B26,BOOTROM_DEVEL,ENET_LOM_DISABLE,ENETPWR_S3AC,GPU_BB_CTL,GPUTHM_A_GPU
M1_COMMON2	HSTHMSNS_HAS,ITP,INVERTER_BUF,KBDLED_HAS,LPCPLUS,LVDS_PD,MEMVREF_S3
M1_COMMON3	MEMVTT_EN_PU,RTUSB_ESD,SMC_PRGRM,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
VRAM_HY128	GPU_MEM_HYNIX,VRAM_128_HYNIX
VRAM_SAM128	VRAM_128_SAMSUNG
VRAM_HY256	GPU_MEM_256M,GPU_MEM_HYNIX,VRAM_256_HYNIX
VRAM_SAM256	GPU_MEM_256M,VRAM_256_SAMSUNG

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:VWP]	CRITICAL	EEE_VWP	M1,2.0GHZ,128VRAM
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:VWQ]	CRITICAL	EEE_VWQ	M1,2.16GHZ,256VRAM
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:W36]	CRITICAL	EEE_W36	M1,1.83GHZ,128VRAM
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:W37]	CRITICAL	EEE_W37	M1,2.0GHZ,256VRAM

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX
337S3282	1	IC,YDC,CO,1.83G,31W,667M,2M,479BGA	U0700	CRITICAL	CPU_1_83GHZ
337S3267	1	IC,YDC,CO,2.0G,31W,667M,2M,479BGA	U0700	CRITICAL	CPU_2_0GHZ
337S3268	1	IC,YDC,CO,2.16G,31W,667M,2M,479BGA	U0700	CRITICAL	CPU_2_16GHZ
341S1873	1	IC,EFI,BOOTROM DEVELOPMENT (NEW),M1	U6301	CRITICAL	BOOTROM_DEVEL
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1875	1	IC,PRGRM,SMC (NEW),M1	U5800	CRITICAL	SMC_PRGRM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0268	1	IC,FW32306,1394A LINK,BGA,129P	U4400	CRITICAL	
338S0269	1	IC,945GM,NORTHBRIDGE	U1200	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0309	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	ATI_REV_B24
338S0315	1	IC,ATI,M56-LP,B26,GRPHXCRTL,LF 880BGA	U8400	CRITICAL	ATI_REV_B26
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
343S0385	1	IC,ICH7M,BGA	U2100	CRITICAL	
353S1465	1	IC,ISL6262,SYNC REG CTRL,SCREENED,QFN48	U7530	CRITICAL	
359S0101	1	IC,CY28445-5,CLOCK GEN,68PIN QFN	U3301	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060		ALL	330uF,2V,9MOHM,D2
128S0095	128S0060		ALL	330uF,2V,6MOHM,D2
128S0081	128S0061		ALL	150uF,6.3V,25MOHM,C2
376S0448	376S0445		ALL	Si7806ADN for FDM6296
128S0093	128S0092		ALL	Kemet is alt to Sanyo

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

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Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	57
TRUE		IMVP6_COMP	57
TRUE		P5VS5_RUNSS	58 62
TRUE		P1V5S0_RUNSS	58 62
TRUE		P2V5S3_MODE	59
TRUE		P2V5S3_SHDNRT	59
TRUE		P1V2S3_RT	59
TRUE		P1V2S3_RUNSS	39 59
TRUE		P1V8S3_COMP	60
TRUE		P1V8S3_FSET	60
TRUE		P3V3S5_COMP	61
TRUE		P3V3S5_FSET	61
TRUE		P1V05S0_COMP	61
TRUE		P1V05S0_FSET	61
TRUE		P3V42G3H_FB	62
TRUE		GPUVCORE_COMP	66
TRUE		GPUVCORE_FSET	66
TRUE		GPUBBP_ADJ	66

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7 12 82
TRUE		FSB_ADS_L	7 12 82
TRUE	TRUE	FSB_ADSTB_L<1..0>	7 12 82
TRUE		FSB_BNR_L	7 12 82
TRUE		FSB_BREQ0_L	7 12 82
TRUE		FSB_D_L<63..0>	7 12 82
TRUE		FSB_DBSY_L	7 12 82
TRUE	TRUE	FSB_DINV_L<3..0>	7 12 82
TRUE		FSB_DRDY_L	7 12 82
TRUE	TRUE	FSB_DSTBN_L<3..0>	7 12 82
TRUE	TRUE	FSB_DSTBP_L<3..0>	7 12 82
TRUE		FSB_HIT_L	7 12 82
TRUE		FSB_HITM_L	7 12 82
TRUE		FSB_LOCK_L	7 12 82
TRUE		FSB_REQ_L<4..0>	7 12 82

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14 22
TRUE	DMI_N2S_N<1..0>	14 22
TRUE	SB_CLK100M_SATA_P	21 34
TRUE	SB_CLK100M_SATA_N	21 34

FUNC_TEST property removed since these test points are not on the proper side for Functional Test points.

Fan Connectors

FUNC_TEST		
	=PP5V_S0_FAN_LT	54 63
	FAN_LT_PWM	54
	FAN_LT_TACH	54
	FAN_RT_PWM	54
	FAN_RT_TACH	54

LPC+ Debug Connector

FUNC_TEST		
TRUE	=PP3V3_S5_LPCPLUS	49 63
TRUE	=PP5V_S0_LPCPLUS	49 63
TRUE	LPC_AD<0>	21 47 49 56
TRUE	LPC_AD<1>	21 47 49 56
TRUE	LPC_FRAME_L	21 47 49 56
TRUE	PM_CLKRUN_L	23 40 47 49 56
TRUE	BOOT_LPC_SPI_L	22 47 49
TRUE	SMC_TMS	47 48 49
TRUE	DEBUG_RST_L	26 49
TRUE	SMC_TRST_L	47 49
TRUE	SMC_TDO	47 48 49
TRUE	SMC_MD1	47 49
TRUE	SMC_TX_L	47 48 49
TRUE	FWH_INIT_L	21 48 49
TRUE	PCI_CLK_PORT80_LPC	34 49
TRUE	LPC_AD<2>	21 47 49 56
TRUE	LPC_AD<3>	21 47 49 56
TRUE	INT_SERIRQ	23 47 49 56
TRUE	PM_SUS_STAT_L	23 47 48 49 56
TRUE	SMC_TDI	47 48 49
TRUE	SMC_TCK	47 48 49
TRUE	SMC_RST_L	47 48 49
TRUE	SMC_NMI	47 49
TRUE	SMC_RX_L	47 48 49
TRUE	SV_SET_UP	23 49

Left ALS Connector

FUNC_TEST		
TRUE	=PP3V3_S3_LTALS	63 76
TRUE	ALS_GAIN	6 47 76
TRUE	LTALS_OUT	53 76
TRUE	GND	

Camera Connector

FUNC_TEST		
TRUE	=PP5V_S3_CAMERA	43 63
TRUE	=USB2_CAMERA_N	6 43
TRUE	=USB2_CAMERA_P	6 43
TRUE	=SMBUS_ATS_SDA	27 43
TRUE	=SMBUS_ATS_SCL	27 43
TRUE	GND	

Thermal Diode Connectors

FUNC_TEST		
TRUE	HSTHMSNS_DX_P	50
TRUE	HSTHMSNS_DX_N	50
TRUE	RSFSTHMSNS_D_P	50
TRUE	RSFSTHMSNS_D_N	50

Other Func Test Points

FUNC_TEST		
TRUE	=PP1V05_S0_REG	51 61 63
TRUE	PM_SYSRST_L	23 26 47
TRUE	SMC_ONOFF_L	43 47 48 51

Current Sense Calibration

FUNC_TEST		
TRUE	ISENSE_CAL_EN	
TRUE	=PP5V_S0_ISENSECAL	
TRUE	=PP1V8_S3_REG	51 60 63
TRUE	=PP1V5_S0_REG	58 63
TRUE	PPVCORE_S0_GPU	63
TRUE	PPVCORE_S0_CPU	63
TRUE	GND	

2 TPs per

8 TPs, 2 with each of above TP pairs

Battery Digital Connector

FUNC_TEST		
TRUE	SMC_BS_ALRT_L	47 48 64
TRUE	=SMBUS_BATT_SCL	27 64
TRUE	=SMBUS_BATT_SDA	27 64
TRUE	GND_BATT	64

Left I/O Data Connector

FUNC_TEST		
TRUE	=PP1V5_S0_LIO	45 63
TRUE	=PPDCIN_G3H_LIO	45 63
TRUE	=PP5V_S5_LIO	45 63
TRUE	=PP3V42_G3H_LIO	45 63
TRUE	PP5V_S0_AUDIO_PWR	45
TRUE	PP5V_S0_AUDIO	45
TRUE	GND_AUDIO_PWR	45
TRUE	GND_AUDIO	45
TRUE	ACZ_SDATAIN<0>	21 45 82
TRUE	ACZ_SDATAOUT	21 45 82
TRUE	ACZ_BITCLK	21 45 82
TRUE	ACZ_RST_L	21 45 82
TRUE	EXCARD_OC_L	6 45 48
TRUE	LTUSB_OC_L	6 45
TRUE	LIO_BATT_ISENSE	45 51
TRUE	SMC_SYS_ISET	45 47
TRUE	SMC_BATT_ISET	45 47
TRUE	SMC_BATT_CHG_EN	45 47 48
TRUE	SMC_BC_ACOK	45 47 48
TRUE	SMC_ADAPTER_EN	41 45 47 48
TRUE	LIO_P3V3S0_EN_L	45 62
TRUE	LIO_DCIN_ISENSE	45 51
TRUE	LIO_P3V3S3_EN	45 62
TRUE	SMC_BATT_TRICKLE_EN_L	45 47 48
TRUE	SYS_ONEWIRE	45 47 48
TRUE	MINI_CLKREQ_L	34 45
TRUE	SMC_EXCARD_CP	45 47 48
TRUE	EXCARD_CLKREQ_L	34 45
TRUE	SMC_EXCARD_PWR_EN	45 47
TRUE	LIO_PLT_RESET_L	26 45
TRUE	ACZ_SYNC	21 45 82
TRUE	=USB2_LT_N	6 45
TRUE	=USB2_LT_P	6 45
TRUE	=USB2_EXCARD_N	6 45
TRUE	=USB2_EXCARD_P	6 45
TRUE	=PCIE_EXCARD_R2D_N	45 46
TRUE	=PCIE_EXCARD_R2D_P	45 46
TRUE	=PCIE_EXCARD_D2R_N	45 46
TRUE	=PCIE_EXCARD_D2R_P	45 46
TRUE	PCIE_CLK100M_EXCARD_P	34 45
TRUE	PCIE_CLK100M_EXCARD_N	34 45
TRUE	=PCIE_MINI_R2D_N	45 46
TRUE	=PCIE_MINI_R2D_P	45 46
TRUE	=PCIE_MINI_D2R_N	45 46
TRUE	=PCIE_MINI_D2R_P	45 46
TRUE	PCIE_CLK100M_MINI_P	34 45
TRUE	PCIE_CLK100M_MINI_N	34 45
TRUE	=SMBUS_LIO_SMC_SCL	27 45
TRUE	=SMBUS_LIO_SMC_SDA	27 45
TRUE	=SMBUS_LIO_SB_SCL	27 45
TRUE	=SMBUS_LIO_SB_SDA	27 45
TRUE	PCIE_WAKE_L	23 37 45

Left I/O Power Connector

FUNC_TEST		
TRUE	=PPBUS_G3H_LIO_CONN	63 64
TRUE	GND	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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NC_CPU_A32_L — TP_CPU_A32_L (7)
NC_CPU_A33_L — TP_CPU_A33_L (7)
NC_CPU_A34_L — TP_CPU_A34_L (7)
NC_CPU_A35_L — TP_CPU_A35_L (7)
NC_CPU_A36_L — TP_CPU_A36_L (7)
NC_CPU_A37_L — TP_CPU_A37_L (7)
NC_CPU_A38_L — TP_CPU_A38_L (7)
NC_CPU_A39_L — TP_CPU_A39_L (7)
NC_CPU_APM0_L — TP_CPU_APM0_L (7)
NC_CPU_APM1_L — TP_CPU_APM1_L (7)
NC_CPU_EXTBREF — TP_CPU_EXTBREF (7)
NC_CPU_HFPLL — TP_CPU_HFPLL (7)
NC_CPU_SPARE0 — TP_CPU_SPARE0 (7)
NC_CPU_SPARE1 — TP_CPU_SPARE1 (7)
NC_CPU_SPARE2 — TP_CPU_SPARE2 (7)
NC_CPU_SPARE4 — TP_CPU_SPARE4 (7)

NC_MEM_A_A<15..14> — MEM_A_A<15..14> (28)
NC_MEM_B_A<15..14> — MEM_B_A<15..14> (29)
TP_NB_CFG<4..3> — NB_CFG<4..3> (14)
TP_NB_CFG<6> — NB_CFG<6> (14)
TP_NB_CFG<8> — NB_CFG<8> (14)
TP_NB_CFG<11..10> — NB_CFG<11..10> (14)
TP_NB_CFG<15..14> — NB_CFG<15..14> (14)
TP_NB_CFG<17> — NB_CFG<17> (14)

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> — NB_CFG<13..12> (14)

TP_SB_SUS_CLK — SUS_CLK_SB (23)

NC_SB_XOR_T5 — TP_SB_XOR_T5 (21)
NC_SB_XOR_U5 — TP_SB_XOR_U5 (21)
NC_SB_XOR_V3 — TP_SB_XOR_V3 (21)
NC_SB_XOR_V4 — TP_SB_XOR_V4 (21)
NC_SB_XOR_W3 — TP_SB_XOR_W3 (21)

TP_SMC_RSTGATE_L — SMC_RSTGATE_L (47)
ALS_GAIN (76 47 5) — =RTALS_GAIN (53)

NC_ENET_CTRL12 — ENET_CTRL12 (37)
NC_ENET_CTRL25 — ENET_CTRL25 (37)

Ethernet Power Management Support

ENET_LOM_DISABLE
R0600
0
5%
1/16W
MF-LF
402

SB_GPIO30 (22) — 1 — 2 — ENET_LOM_DIS_L (37)

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOM_DISABLE" are mutually-exclusive.

USB Port "A" (Debug Port) = Right USB 2.0 Port

=USB2_RT_P (44) — USB2_RT_P — USB_A_P (22)
=USB2_RT_N (44) — USB2_RT_N — USB_A_N (22)
=RTUSB_OC_L (44) — RTUSB_OC_L — USB_A_OC_L (22)

USB Port "B" = Trackpad (Geyser)

=USB_TRACKPAD_P (43) — USB_TRACKPAD_P — USB_B_P (22)
=USB_TRACKPAD_N (43) — USB_TRACKPAD_N — USB_B_N (22)
UNUSED_USB_B_OC_L — USB_B_OC_L (22)

USB Port "C" = Left USB 2.0 Port

=USB2_LT_P (45 5) — USB2_LT_P — USB_C_P (22)
=USB2_LT_N (45 5) — USB2_LT_N — USB_C_N (22)
LTUSB_OC_L — USB_C_OC_L (22)

USB Port "D" = Camera

=USB2_CAMERA_P (43 5) — USB2_CAMERA_P — USB_D_P (22)
=USB2_CAMERA_N (43 5) — USB2_CAMERA_N — USB_D_N (22)
UNUSED_USB_D_OC_L — USB_D_OC_L (22)

USB Port "E" = ExpressCard

=USB2_EXCARD_P (45 5) — USB2_EXCARD_P — USB_E_P (22)
=USB2_EXCARD_N (45 5) — USB2_EXCARD_N — USB_E_N (22)
EXCARD_OC_L (48 45 5) — USB_E_OC_L (22)

USB Port "F" = IR Receiver

=USB_IR_P (76) — USB_IR_P — USB_F_P (22)
=USB_IR_N (76) — USB_IR_N — USB_F_N (22)

USB Port "G" = Bluetooth (M13P)

=USB_BT_P (76) — USB_BT_P — USB_G_P (22)
=USB_BT_N (76) — USB_BT_N — USB_G_N (22)

USB Port "H" = Reserved (PCI-E Mini Card)

TP_USB2_HP — USB_H_P (22)
TP_USB2_HN — USB_H_N (22)

Trace deleted to make room for other diffpairs over RAM connector.

Chassis connection to be made at the mounting hole northwest of the DVI connector

ZT0600
HOLE-VIA-P5RP25
1 — GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_DVI_TOP — =GND_CHASSIS_DVI2 (75)
GND_CHASSIS_DVI_TOP — =GND_CHASSIS_DVI4 (75)

Chassis connection to be made at the mounting hole southwest of the USB connector

ZT0601
HOLE-VIA-P5RP25
1 — GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_DVI_BOT — =GND_CHASSIS_DVI1 (75)
GND_CHASSIS_DVI_BOT — =GND_CHASSIS_DVI3 (75)
GND_CHASSIS_DVI_BOT — =GND_CHASSIS_DVI5 (75)
GND_CHASSIS_DVI_BOT — =GND_CHASSIS_ENET (38)
GND_CHASSIS_DVI_BOT — =GND_CHASSIS_FW_EMI (42)
GND_CHASSIS_DVI_BOT — =GND_CHASSIS_FW_PORT1 (42)
GND_CHASSIS_DVI_BOT — =GND_CHASSIS_RTUSB (44)

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602
HOLE-VIA-P5RP25
1 — GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_LVDS — =GND_CHASSIS_LCD1 (74)
GND_CHASSIS_LVDS — =GND_CHASSIS_LCD2 (74)
GND_CHASSIS_LVDS — =GND_CHASSIS_LCD3 (74)
GND_CHASSIS_LVDS — =GND_CHASSIS_LCD4 (74)

SH0600
OG-503040
SHLD-SM-LF
1, 2, 3 — GND_CHASSIS_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_INVERTER — =GND_CHASSIS_INVERTER (74)

Signal Aliases

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7155 | REV. A

SCALE NONE | SHT 6 OF 104

OMIT

U0700
YONAH
CPU
BGA
(1 OF 4)

ADDR GROUP0
CONTROL
ADDR GROUP1
XDP/ITP SIGNALS
THERM
HCLK
RESERVED

FSB_A_L<3> J4 A3*
FSB_A_L<4> L4 A4*
FSB_A_L<5> M3 A5*
FSB_A_L<6> K5 A6*
FSB_A_L<7> M1 A7*
FSB_A_L<8> N2 A8*
FSB_A_L<9> J1 A9*
FSB_A_L<10> N3 A10*
FSB_A_L<11> P5 A11*
FSB_A_L<12> P2 A12*
FSB_A_L<13> L1 A13*
FSB_A_L<14> P4 A14*
FSB_A_L<15> P1 A15*
FSB_A_L<16> R1 A16*
FSB_ADSTB_L<0> U2 ADSTB0*

FSB_REQ_L<0> K3 REQ0*
FSB_REQ_L<1> H2 REQ1*
FSB_REQ_L<2> K2 REQ2*
FSB_REQ_L<3> J3 REQ3*
FSB_REQ_L<4> L5 REQ4*

FSB_A_L<17> Y2 A17*
FSB_A_L<18> U5 A18*
FSB_A_L<19> R3 A19*
FSB_A_L<20> W6 A20*
FSB_A_L<21> U4 A21*
FSB_A_L<22> Y5 A22*
FSB_A_L<23> U2 A23*
FSB_A_L<24> R4 A24*
FSB_A_L<25> T5 A25*
FSB_A_L<26> T3 A26*
FSB_A_L<27> W3 A27*
FSB_A_L<28> W5 A28*
FSB_A_L<29> Y4 A29*
FSB_A_L<30> W2 A30*
FSB_A_L<31> Y1 A31*
FSB_ADSTB_L<1> AD1 ADSTB1*

CPU_A20M_L A6 A20M*
CPU_FERR_L A5 FERR*
CPU_IGNNE_L C4 IGNNE*
CPU_STPCLK_L D5 STPCLK*
CPU_INTR C6 LINT0
CPU_NMI B4 LINT1
CPU_SMI_L A3 SMI*

TP_CPU_A32_L AA1 RSVD1
TP_CPU_A33_L AA4 RSVD2
TP_CPU_A34_L AB2 RSVD3
TP_CPU_A35_L AA3 RSVD4
TP_CPU_A36_L M4 RSVD5
TP_CPU_A37_L N5 RSVD6
TP_CPU_A38_L T2 RSVD7
TP_CPU_A39_L V3 RSVD8
TP_CPU_APM0_L B2 RSVD9
TP_CPU_APM1_L C3 RSVD10
TP_CPU_HFPLL L25 RSVD11

ADS* H1 FSB_ADS_L
BNR* E2 FSB_BNR_L
BPRI* G5 FSB_BPRI_L
DEFER* H5 FSB_DEFER_L
DRDY* F21 FSB_DRDY_L
DBSY* E1 FSB_DBSY_L
BR0* F1 FSB_BREQ0_L
IERR* D20 FSB_IERR_L
INIT* B3 CPU_INIT_L
LOCK* H4 FSB_LOCK_L
RESET* B1 FSB_CPURST_L
RS0* F3 FSB_RS_L<0>
RS1* F4 FSB_RS_L<1>
RS2* G3 FSB_RS_L<2>
TRDY* G2 FSB_TRDY_L
HIT* G6 FSB_HIT_L
HITM* E4 FSB_HITM_L

BPM0* AD4 XDP_BPM_L<0>
BPM1* AD3 XDP_BPM_L<1>
BPM2* AD1 XDP_BPM_L<2>
BPM3* AC4 XDP_BPM_L<3>
PRDY* AC2 XDP_BPM_L<4>
PREQ* AC1 XDP_BPM_L<5>
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST* AB6 XDP_TRST_L
DBR* C20 XDP_DBRESET_L

PROCHOT* D21 CPU_PROCHOT_L
THERMDA A24 CPU_THERMD_P
THERMDC A25 CPU_THERMD_N
THERMTRIP* C7 PM_THRMTRIP_L

BCLK0 A22 FSB_CLK_CPU_P
BCLK1 A21 FSB_CLK_CPU_N

RSVD12 T22 TP_CPU_EXTBREF
RSVD13 D2 TP_CPU_SPARE0
RSVD14 F6 TP_CPU_SPARE1
RSVD15 D3 TP_CPU_SPARE2
RSVD16 C1 TP_CPU_SPARE3
RSVD17 AF1 TP_CPU_SPARE4
RSVD18 D22 TP_CPU_SPARE5
RSVD19 C23 TP_CPU_SPARE6
RSVD20 C24 TP_CPU_SPARE7

SPARE[7-0],HFPLL:
ROUTE TO TP VIA AND
PLACE GND VIA W/IN 1000 MILS

=PP1V05_S0_CPU

R0702 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY

R0703 54.9 1% 1/16W MF-LF 402

R0704 68 5% 1/16W MF-LF 402
CPU_PROCHOT_L TO SMC AND CPU VR TO INFORM CPU IS HOT

PM_THRMTRIP# SHOULD CONNECT TO ICH7-M AND GMCH WITHOUT T-ING (NO STUB)

R0705 1K 1% 1/16W MF-LF 402

R0706 2.0K 1% 1/16W MF-LF 402
LAYOUT NOTE: 0.5" MAX LENGTH

CPU_GTLREF
CPU_TEST1
CPU_TEST2
CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>

NOSTUFF R0730 0 402
R0712 5K 5% 1/16W MF-LF 402
NOSTUFF R0707 1K 5% 1/16W MF-LF 402

OMIT

U0700
YONAH
CPU
BGA
(2 OF 4)

DATA GRP0
DATA GRP2
DATA GRP1
DATA GRP3
MISC

FSB_D_L<0> E22 D0*
FSB_D_L<1> F24 D1*
FSB_D_L<2> E26 D2*
FSB_D_L<3> H22 D3*
FSB_D_L<4> F23 D4*
FSB_D_L<5> G25 D5*
FSB_D_L<6> E25 D6*
FSB_D_L<7> E23 D7*
FSB_D_L<8> K24 D8*
FSB_D_L<9> G24 D9*
FSB_D_L<10> J24 D10*
FSB_D_L<11> J23 D11*
FSB_D_L<12> H26 D12*
FSB_D_L<13> F26 D13*
FSB_D_L<14> K22 D14*
FSB_D_L<15> H25 D15*
FSB_DSTBN_L<0> K26 DSTBN0*
FSB_DSTBP_L<0> L24 DSTBP0*
FSB_DINV_L<0> G26 DINV0*

FSB_D_L<16> N22 D16*
FSB_D_L<17> K25 D17*
FSB_D_L<18> P26 D18*
FSB_D_L<19> R23 D19*
FSB_D_L<20> L25 D20*
FSB_D_L<21> L22 D21*
FSB_D_L<22> L23 D22*
FSB_D_L<23> M23 D23*
FSB_D_L<24> P25 D24*
FSB_D_L<25> P22 D25*
FSB_D_L<26> P23 D26*
FSB_D_L<27> T24 D27*
FSB_D_L<28> R24 D28*
FSB_D_L<29> L26 D29*
FSB_D_L<30> T25 D30*
FSB_D_L<31> N24 D31*
FSB_DSTBN_L<1> M24 DSTBN1*
FSB_DSTBP_L<1> N25 DSTBP1*
FSB_DINV_L<1> U26 DINV1*

GTLREF AD26
NC A2
TEST1 C26
TEST2 D25
BSEL0 B22
BSEL1 B23
BSEL2 C21

COMP0 R26 CPU_COMP<0>
COMP1 U26 CPU_COMP<1>
COMP2 U1 CPU_COMP<2>
COMP3 V1 CPU_COMP<3>
DPRSTP* E5 CPU_DPRSTP_L
DPSLP* B5 CPU_DPSLP_L
DPWR* D24 FSB_DPWR_L
PWRGOOD D6 CPU_PWRGD
SLP* D7 FSB_SLPCPU_L
PSI* AE6 CPU_PSI_L

D32* AA23 FSB_D_L<32>
D33* AB24 FSB_D_L<33>
D34* V24 FSB_D_L<34>
D35* V26 FSB_D_L<35>
D36* W25 FSB_D_L<36>
D37* U23 FSB_D_L<37>
D38* U25 FSB_D_L<38>
D39* U22 FSB_D_L<39>
D40* AB25 FSB_D_L<40>
D41* W22 FSB_D_L<41>
D42* Y23 FSB_D_L<42>
D43* AA26 FSB_D_L<43>
D44* Y26 FSB_D_L<44>
D45* Y22 FSB_D_L<45>
D46* AC26 FSB_D_L<46>
D47* AA24 FSB_D_L<47>
DSTBN2* W24 FSB_DSTBN_L<2>
DSTBP2* Y25 FSB_DSTBP_L<2>
DINV2* V23 FSB_DINV_L<2>

D48* AC22 FSB_D_L<48>
D49* AC23 FSB_D_L<49>
D50* AB22 FSB_D_L<50>
D51* AA21 FSB_D_L<51>
D52* AB21 FSB_D_L<52>
D53* AC25 FSB_D_L<53>
D54* AD20 FSB_D_L<54>
D55* AE22 FSB_D_L<55>
D56* AF23 FSB_D_L<56>
D57* AD24 FSB_D_L<57>
D58* AE21 FSB_D_L<58>
D59* AD21 FSB_D_L<59>
D60* AE25 FSB_D_L<60>
D61* AF25 FSB_D_L<61>
D62* AF22 FSB_D_L<62>
D63* AF26 FSB_D_L<63>
DSTBN3* AD23 FSB_DSTBN_L<3>
DSTBP3* AE24 FSB_DSTBP_L<3>
DINV3* AC20 FSB_DINV_L<3>

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".

R0716 27.4 1% 1/16W MF-LF 402
R0717 54.9 1% 1/16W MF-LF 402
R0718 27.4 1% 1/16W MF-LF 402
R0719 54.9 1% 1/16W MF-LF 402

=PP1V05_S0_CPU

R0720 54.9 1% 1/16W MF-LF 402 XDP_TMS
R0721 54.9 1% 1/16W MF-LF 402 XDP_TDI
R0722 54.9 1% 1/16W MF-LF 402 XDP_TCK

CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

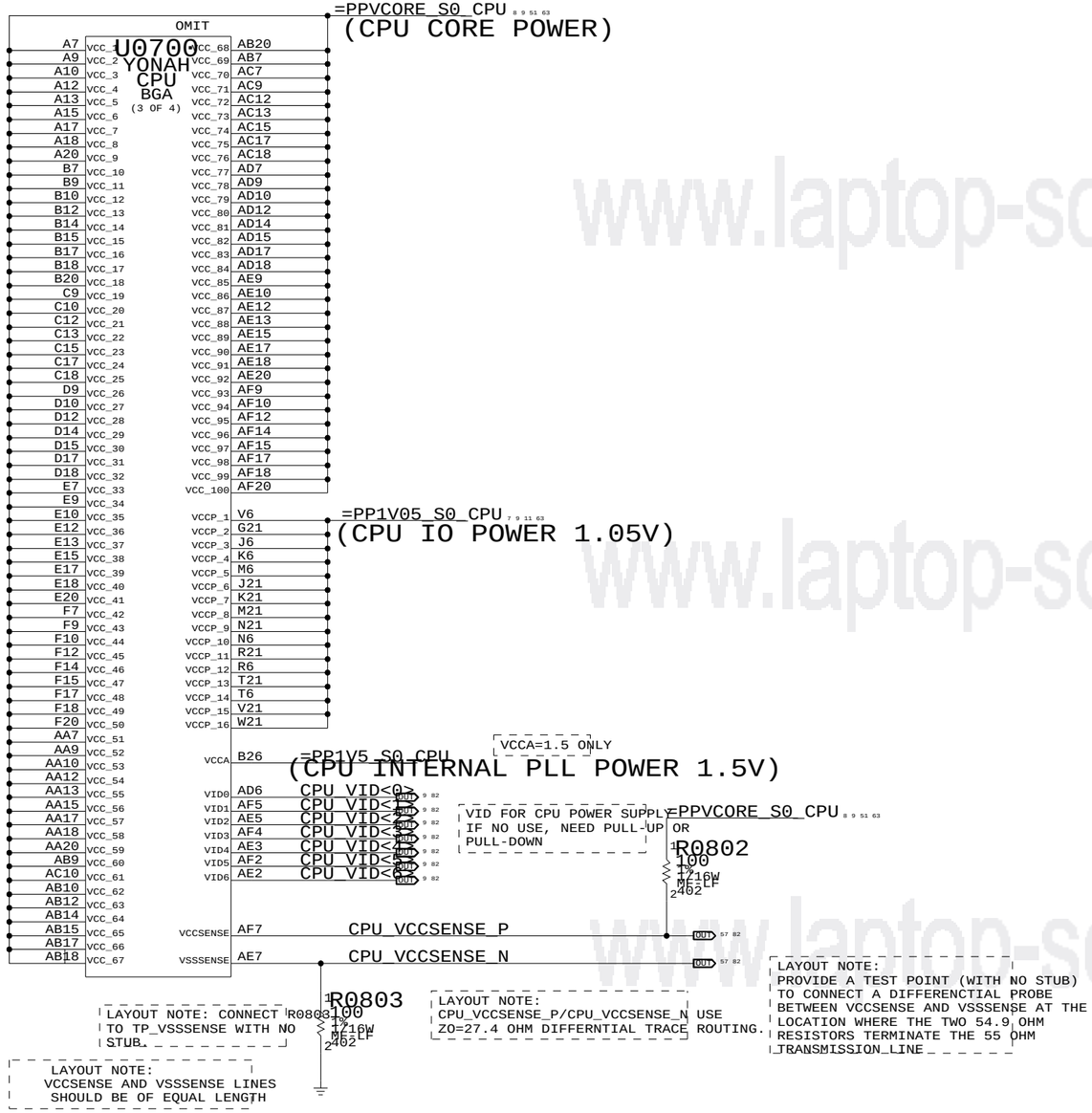
WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

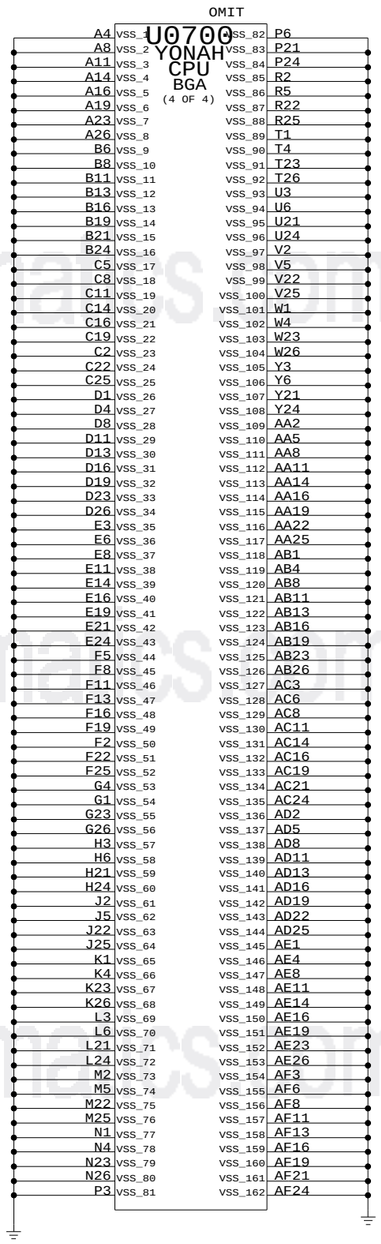
CPU 1 OF 2-FSB

SYNC_MASTER=M42 SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 7 OF 104	





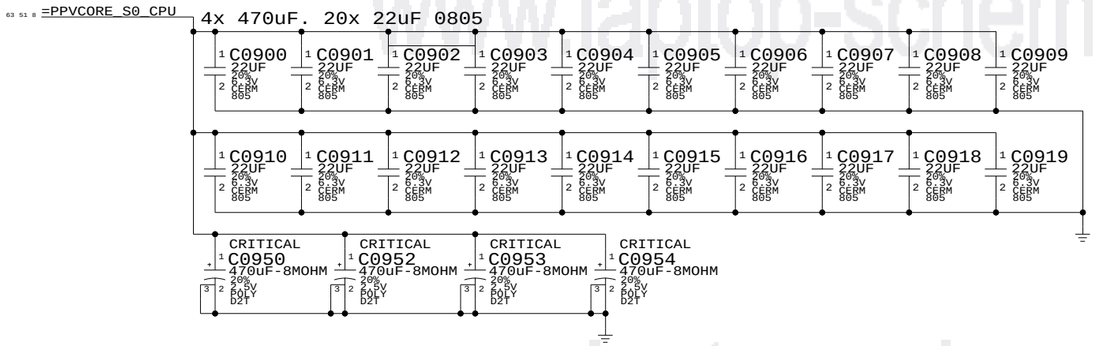
CPU 2 OF 2-PWR/GND

SYNC_MASTER=M42 SYNC_DATE=11/16/2005

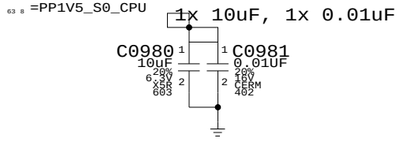
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 8 OF 104	

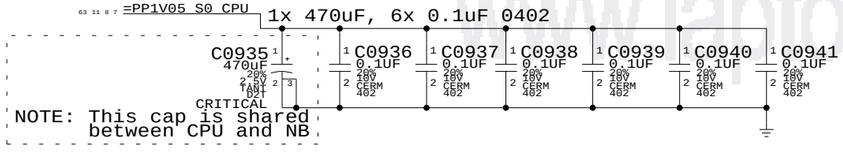
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

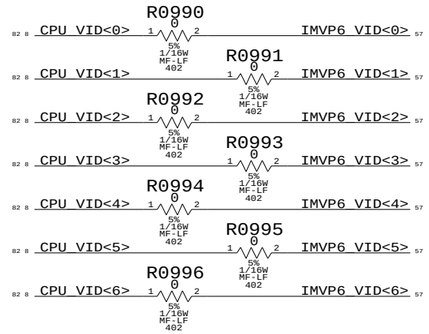


VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



CPU Decoupling & VID

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 9 OF 104	

CPU ZONE THERMAL SENSOR

LAYOUT NOTE:
ADD GND GUARD TRACE
FOR CPU_THERMD_P AND
CPU_THERMD_N

LAYOUT NOTE:
ROUTE CPU_THERMD_P AND
CPU_THERMD_N ON SAME
LAYER.
10 MIL TRACE
10 MIL SPACING

PLACEHOLDER ADT7461A
CRITICAL

63 =PP3V3_S0_THRM_SNR

C1002
0.1UF
16V
X5R
402

R1005
10K
5%
1/16W
MF-LF
402

R1006
10K
5%
1/16W
MF-LF
402

U1001
ADT7461
MSOP

VDD
GND
ALERT*/THM2*
THM*
SCLK
SDATA

THRM_ALERT_L
THRM_ALERT

27 SMB_THRM_CLK
27 SMB_THRM_DATA

R1001
499
1%
1/10W
MF-LF
402

R1002
499
1%
1/10W
MF-LF
402

C1001
0.001uF
10%
50V
CERM
402

OUT CPU_THERMD_P
IN CPU_THERMD_N

50 THRM_CPU_DX_P
50 THRM_CPU_DX_N

D+
D-

(TO CPU INTERNAL THERMAL DIODE)

PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

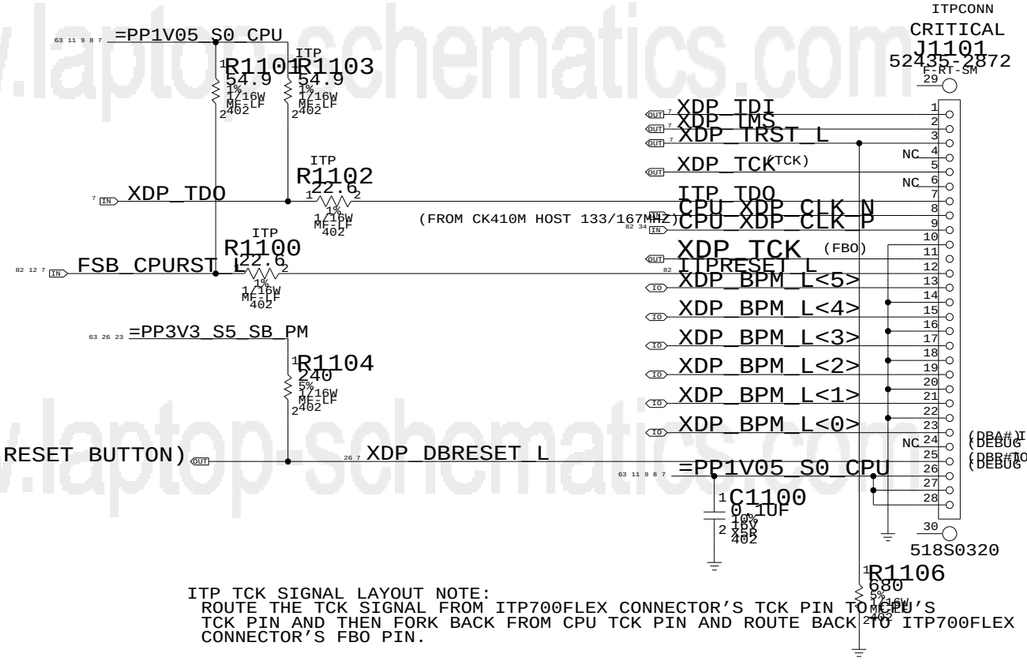
SYNC_MASTER=M42 SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE	SHT	OF
NONE	10	104

CPU ITP700FLEX DEBUG SUPPORT



(DBA#)INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.
(DEBUG PORT ACTIVE)
(DBR#)TO TCH7M_SYS_RST*, AND WITH SYSTEM RESET LOGIC
(DEBUG PORT RESET)

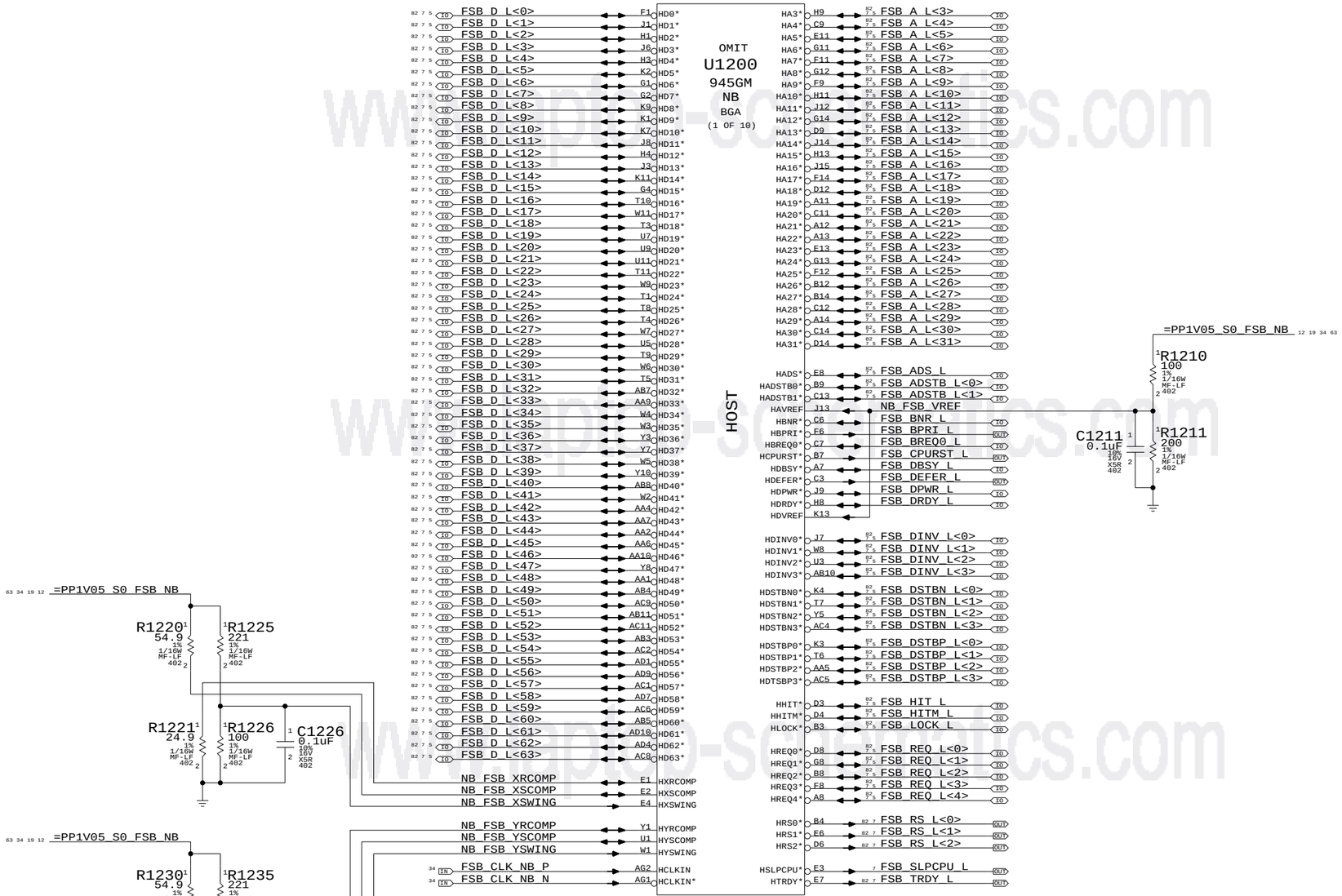
ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M52 SYNC_DATE=10/12/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 11 OF 104	



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE	SHT	OF
NONE	12	104

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

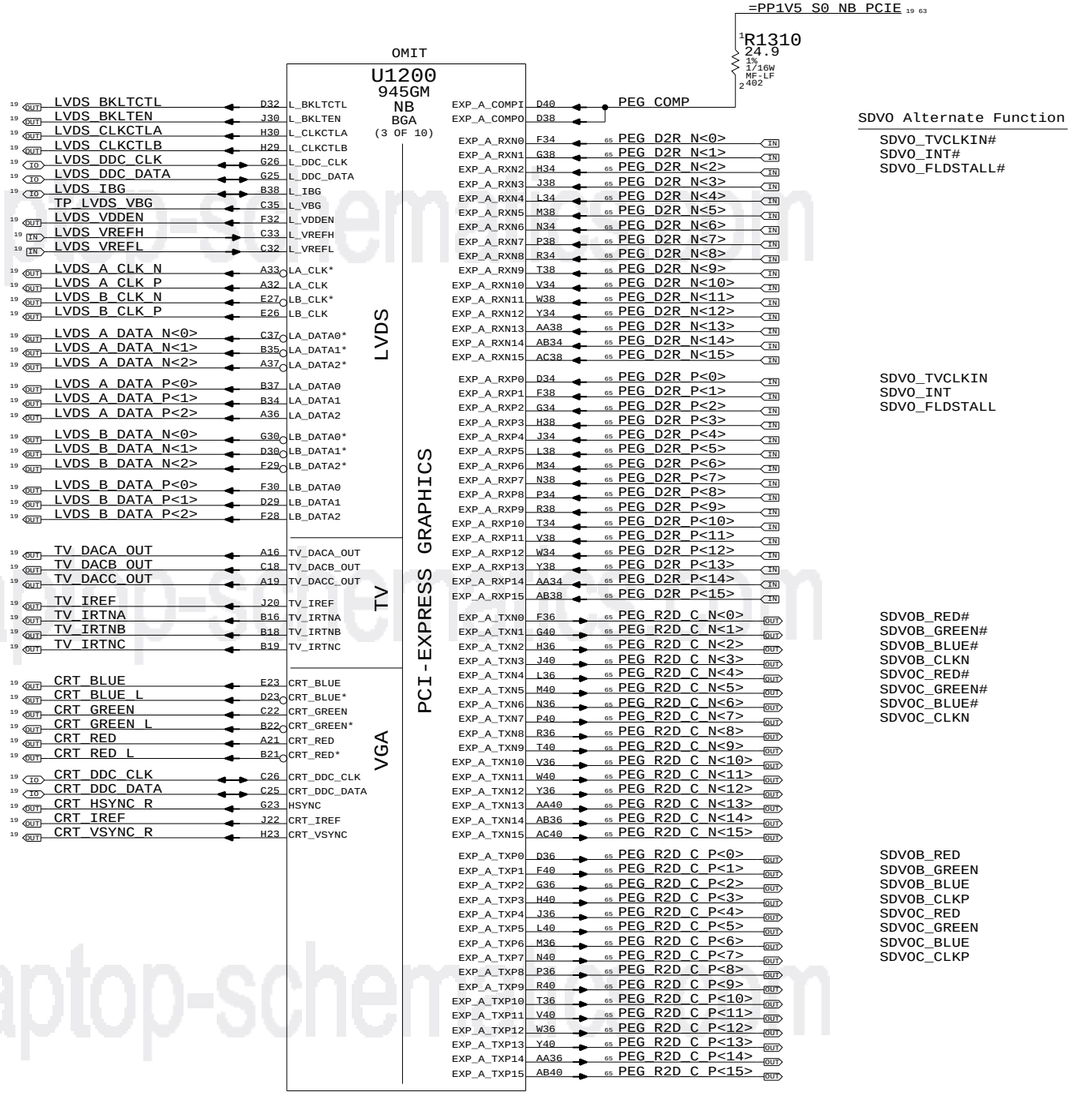
Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



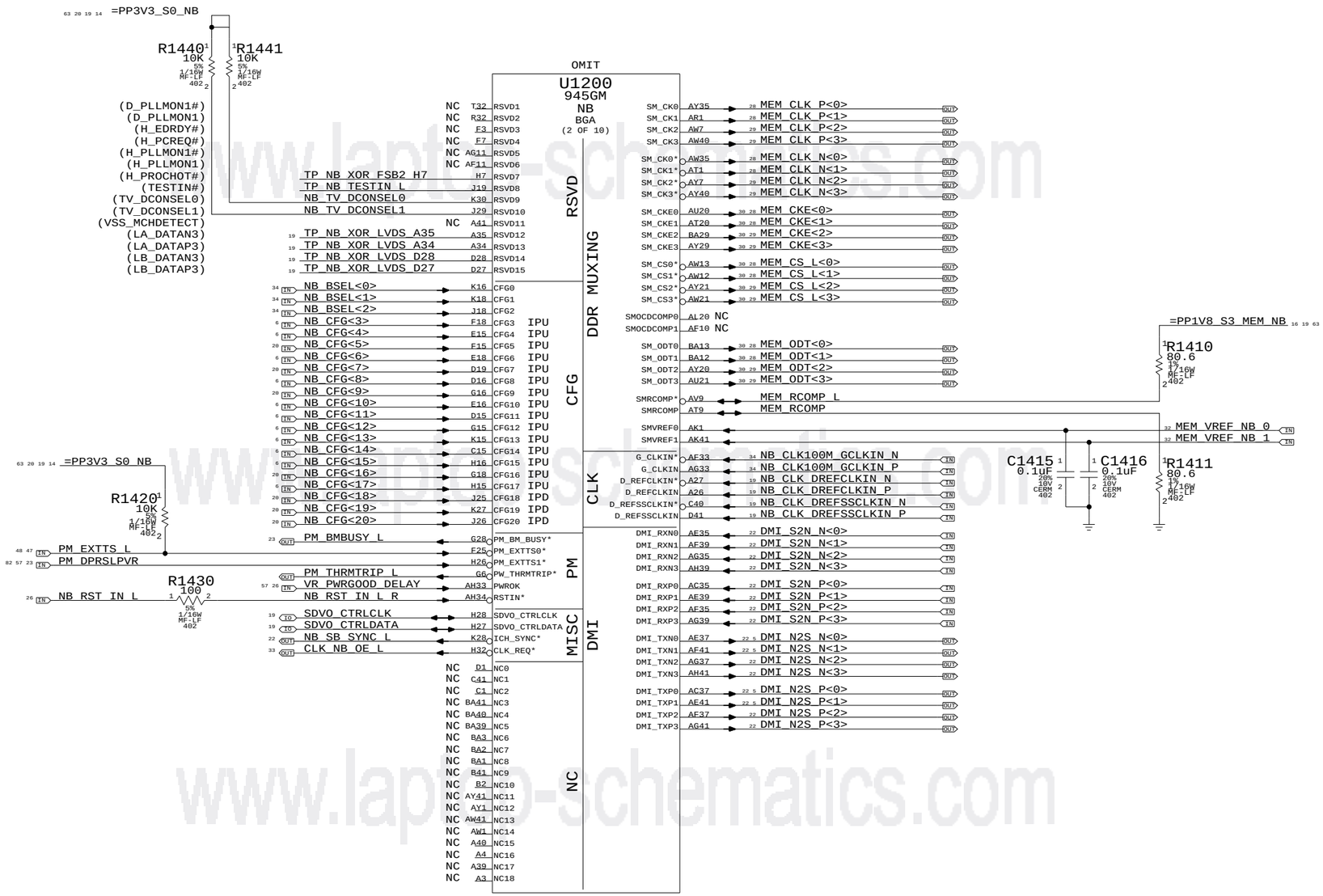
NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE NONE SHT 13 OF 104

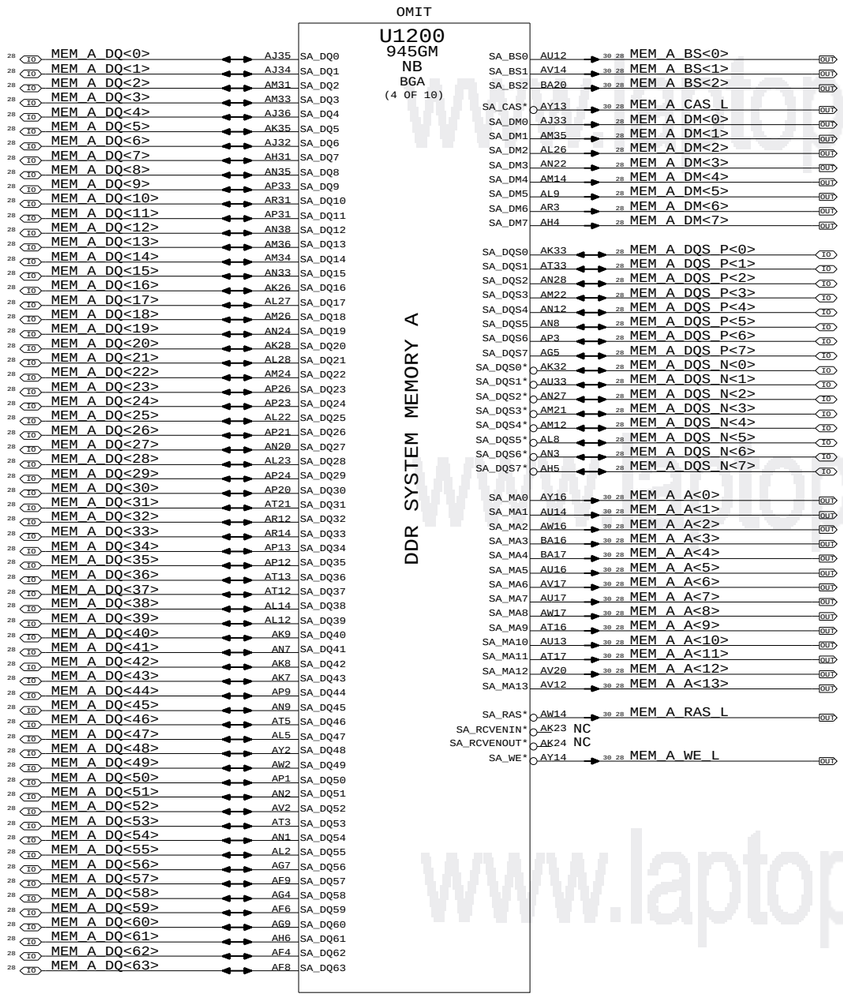


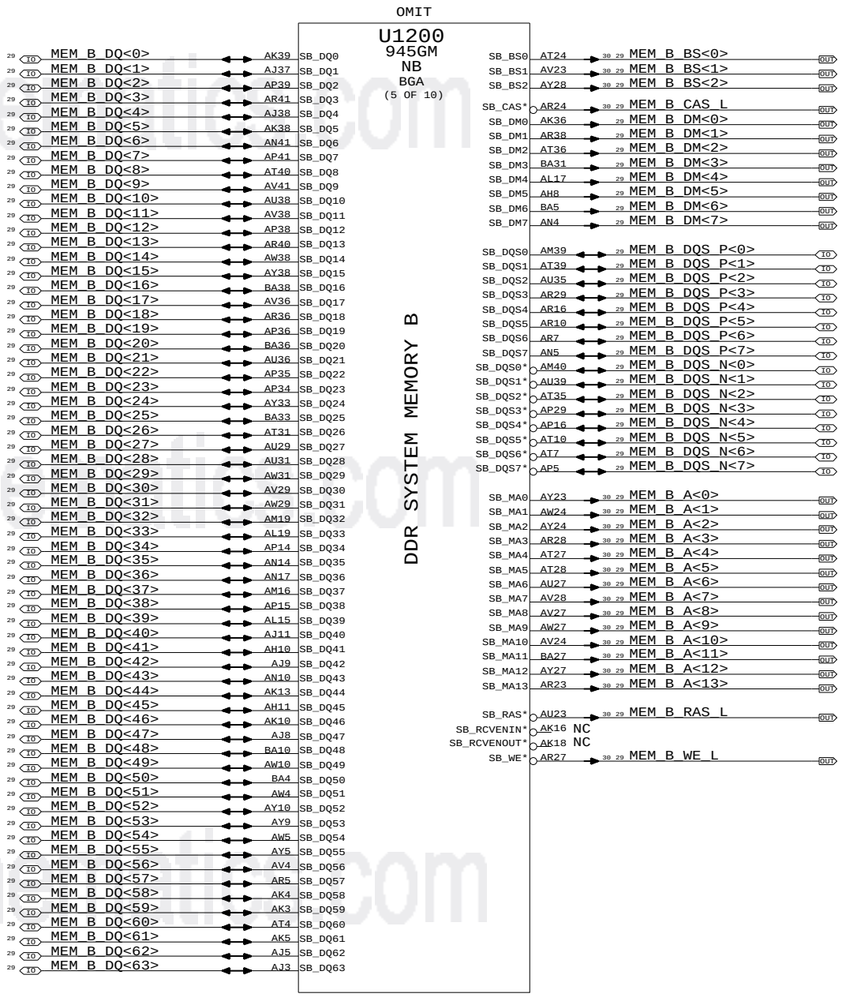
NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 14 OF 104	





NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE: NONE

SHT 15 OF 104

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

=PPVCORE_S0_NB 63 19 16

OMIT

U1200 945GM NB BGA (7 OF 10) NCTF

AD27	VCC_NCTF0	VSS_NCTF0	AE27
AC27	VCC_NCTF1	VSS_NCTF1	AE26
AB27	VCC_NCTF2	VSS_NCTF2	AE25
AA27	VCC_NCTF3	VSS_NCTF3	AE24
Y27	VCC_NCTF4	VSS_NCTF4	AE23
W27	VCC_NCTF5	VSS_NCTF5	AE22
V27	VCC_NCTF6	VSS_NCTF6	AE21
U27	VCC_NCTF7	VSS_NCTF7	AE20
T27	VCC_NCTF8	VSS_NCTF8	AE19
R27	VCC_NCTF9	VSS_NCTF9	AE18
AD26	VCC_NCTF10	VSS_NCTF10	AC17
AC26	VCC_NCTF11	VSS_NCTF11	Y17
AB26	VCC_NCTF12	VSS_NCTF12	U17
AA26	VCC_NCTF13		
Y26	VCC_NCTF14		
W26	VCC_NCTF15		
V26	VCC_NCTF16		
U26	VCC_NCTF17		
T26	VCC_NCTF18		
R26	VCC_NCTF19		
AD25	VCC_NCTF20		
AC25	VCC_NCTF21		
AB25	VCC_NCTF22		
AA25	VCC_NCTF23		
Y25	VCC_NCTF24		
W25	VCC_NCTF25		
V25	VCC_NCTF26		
U25	VCC_NCTF27		
T25	VCC_NCTF28		
R25	VCC_NCTF29		
AD24	VCC_NCTF30		
AC24	VCC_NCTF31		
AB24	VCC_NCTF32		
AA24	VCC_NCTF33		
Y24	VCC_NCTF34		
W24	VCC_NCTF35		
V24	VCC_NCTF36		
U24	VCC_NCTF37		
T24	VCC_NCTF38		
R24	VCC_NCTF39		
AD23	VCC_NCTF40		
V23	VCC_NCTF41		
U23	VCC_NCTF42		
T23	VCC_NCTF43		
R23	VCC_NCTF44		
AD22	VCC_NCTF45		
V22	VCC_NCTF46		
U22	VCC_NCTF47		
T22	VCC_NCTF48		
R22	VCC_NCTF49		
AD21	VCC_NCTF50		
V21	VCC_NCTF51		
U21	VCC_NCTF52		
T21	VCC_NCTF53		
R21	VCC_NCTF54		
AD20	VCC_NCTF55		
V20	VCC_NCTF56		
U20	VCC_NCTF57		
T20	VCC_NCTF58		
R20	VCC_NCTF59		
AD19	VCC_NCTF60		
V19	VCC_NCTF61		
U19	VCC_NCTF62		
T19	VCC_NCTF63		
AD18	VCC_NCTF64		
AC18	VCC_NCTF65		
AB18	VCC_NCTF66		
AA18	VCC_NCTF67		
Y18	VCC_NCTF68		
W18	VCC_NCTF69		
V18	VCC_NCTF70		
U18	VCC_NCTF71		
T18	VCC_NCTF72		

=PP1V5_S0_NB_VCCAUX 17 19 63

		VCCAUX_NCTF0	AG27
		VCCAUX_NCTF1	AF27
		VCCAUX_NCTF2	AG26
		VCCAUX_NCTF3	AF26
		VCCAUX_NCTF4	AG25
		VCCAUX_NCTF5	AF25
		VCCAUX_NCTF6	AG24
		VCCAUX_NCTF7	AF24
		VCCAUX_NCTF8	AG23
		VCCAUX_NCTF9	AF23
		VCCAUX_NCTF10	AG22
		VCCAUX_NCTF11	AF22
		VCCAUX_NCTF12	AG21
		VCCAUX_NCTF13	AF21
		VCCAUX_NCTF14	AG20
		VCCAUX_NCTF15	AF20
		VCCAUX_NCTF16	AG19
		VCCAUX_NCTF17	AF19
		VCCAUX_NCTF18	R19
		VCCAUX_NCTF19	AG18
		VCCAUX_NCTF20	AF18
		VCCAUX_NCTF21	R18
		VCCAUX_NCTF22	AG17
		VCCAUX_NCTF23	AF17
		VCCAUX_NCTF24	AE17
		VCCAUX_NCTF25	AD17
		VCCAUX_NCTF26	AB17
		VCCAUX_NCTF27	AA17
		VCCAUX_NCTF28	W17
		VCCAUX_NCTF29	V17
		VCCAUX_NCTF30	T17
		VCCAUX_NCTF31	R17
		VCCAUX_NCTF32	AG16
		VCCAUX_NCTF33	AF16
		VCCAUX_NCTF34	AE16
		VCCAUX_NCTF35	AD16
		VCCAUX_NCTF36	AC16
		VCCAUX_NCTF37	AB16
		VCCAUX_NCTF38	AA16
		VCCAUX_NCTF39	Y16
		VCCAUX_NCTF40	W16
		VCCAUX_NCTF41	V16
		VCCAUX_NCTF42	U16
		VCCAUX_NCTF43	T16
		VCCAUX_NCTF44	R16
		VCCAUX_NCTF45	AG15
		VCCAUX_NCTF46	AF15
		VCCAUX_NCTF47	AE15
		VCCAUX_NCTF48	AD15
		VCCAUX_NCTF49	AC15
		VCCAUX_NCTF50	AB15
		VCCAUX_NCTF51	AA15
		VCCAUX_NCTF52	Y15
		VCCAUX_NCTF53	W15
		VCCAUX_NCTF54	V15
		VCCAUX_NCTF55	U15
		VCCAUX_NCTF56	T15
		VCCAUX_NCTF57	R15

=PPVCORE_S0_NB 16 19 63

1.05V or 1.5V

1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.5V, Internal Graphics: 5500mA Max

U1200 945GM NB BGA (6 OF 10) VCC

OMIT

AA33	VCC_0	VCC_55	AA29
W33	VCC_1	VCC_56	Y29
P33	VCC_2	VCC_57	W29
N33	VCC_3	VCC_58	V29
L33	VCC_4	VCC_59	U29
J33	VCC_5	VCC_60	R29
AA32	VCC_6	VCC_61	P29
Y32	VCC_7	VCC_62	N29
W32	VCC_8	VCC_63	L29
V32	VCC_9	VCC_64	J29
P32	VCC_10	VCC_65	AB28
N32	VCC_11	VCC_66	AA28
M32	VCC_12	VCC_67	AB23
L32	VCC_13	VCC_68	AA23
J32	VCC_14	VCC_69	Y23
AA31	VCC_15	VCC_70	W23
W31	VCC_16	VCC_71	P23
V31	VCC_17	VCC_72	N23
T31	VCC_18	VCC_73	L23
R31	VCC_19	VCC_74	AC22
P31	VCC_20	VCC_75	AB22
N31	VCC_21	VCC_76	Y22
M31	VCC_22	VCC_77	W22
AA30	VCC_23	VCC_78	P22
Y30	VCC_24	VCC_79	N22
W30	VCC_25	VCC_80	M22
V30	VCC_26	VCC_81	L22
U30	VCC_27	VCC_82	AC21
T30	VCC_28	VCC_83	AA21
R30	VCC_29	VCC_84	W21
P30	VCC_30	VCC_85	N21
N30	VCC_31	VCC_86	M21
M30	VCC_32	VCC_87	L21
L30	VCC_33	VCC_88	AC20
AA29	VCC_34	VCC_89	AB20
Y29	VCC_35	VCC_90	Y20
W29	VCC_36	VCC_91	W20
V29	VCC_37	VCC_92	P20
U29	VCC_38	VCC_93	N20
P29	VCC_39	VCC_94	L20
N29	VCC_40	VCC_95	AB19
M29	VCC_41	VCC_96	AA19
L29	VCC_42	VCC_97	T19
J29	VCC_43	VCC_98	N19
AB28	VCC_44	VCC_99	M19
AA28	VCC_45	VCC_100	L19
Y28	VCC_46	VCC_101	N18
V28	VCC_47	VCC_102	M18
U28	VCC_48	VCC_103	L18
T28	VCC_49	VCC_104	P17
R28	VCC_50	VCC_105	N17
P28	VCC_51	VCC_106	M17
N28	VCC_52	VCC_107	N16
M28	VCC_53	VCC_108	M16
L28	VCC_54	VCC_109	L16
P27		VCC_110	
N27			
M27			
L27			
P26			
N26			
L26			
M25			
L25			
P24			
N24			
M24			
AB23			
AA23			
Y23			
W23			
N23			
L23			
AC22			
AB22			
Y22			
W22			
P22			
N22			
M22			
L22			
AC21			
AA21			
W21			
N21			
M21			
L21			
AC20			
AB20			
Y20			
W20			
P20			
N20			
M20			
L20			
AB19			
T19			
N19			
M19			
L19			
N18			
M18			
L18			
P17			
N17			
M17			
N16			
M16			
L16			

1.8V Max Current

Speed	1 Channel	2 Channel
400MTs	1300mA	2400mA
533MTs	1500mA	2800mA
667MTs	1700mA	3200mA

AU41	VCC_SM0	AP33	VCC_SM42
AT41	VCC_SM1	AP32	VCC_SM43
AM41	VCC_SM2	AP31	VCC_SM44
AJ40	VCC_SM3	AP30	VCC_SM45
BK34	VCC_SM4	AP29	VCC_SM46
AK34	VCC_SM5	AP28	VCC_SM47
AJ34	VCC_SM6	AP27	VCC_SM48
AH34	VCC_SM7	AP26	VCC_SM49
AG34	VCC_SM8	AP25	VCC_SM50
AE34	VCC_SM9	AP24	VCC_SM51
AK34	VCC_SM10	AP23	VCC_SM52
BL30	VCC_SM11	AP22	VCC_SM53
AY30	VCC_SM12	AP21	VCC_SM54
AW30	VCC_SM13	AP20	VCC_SM55
AV30	VCC_SM14	AP19	VCC_SM56
AU30	VCC_SM15	AP18	VCC_SM57
AT30	VCC_SM16	AP17	VCC_SM58
AR30	VCC_SM17	AP16	VCC_SM59
AP30	VCC_SM18	AP15	VCC_SM60
AN30	VCC_SM19	AP14	VCC_SM61
AM30	VCC_SM20	AP13	VCC_SM62
AM29	VCC_SM21	AP12	VCC_SM63
AL29	VCC_SM22	AP11	VCC_SM64
AK29	VCC_SM23	AP10	VCC_SM65
AJ29	VCC_SM24	AP9	VCC_SM66
AH29	VCC_SM25	AP8	VCC_SM67
AJ28	VCC_SM26	AP7	VCC_SM68
AH28	VCC_SM27	AP6	VCC_SM69
AJ27	VCC_SM28	AP5	VCC_SM70
AH27	VCC_SM29	AP4	VCC_SM71
BA26	VCC_SM30	AP3	VCC_SM72
AY26	VCC_SM31	AP2	VCC_SM73
AW26	VCC_SM32	AP1	VCC_SM74
AV26	VCC_SM33	AN1	VCC_SM75
AU26	VCC_SM34	AM1	VCC_SM76
AT26	VCC_SM35	AL1	VCC_SM77
AR26	VCC_SM36	AK1	VCC_SM78
AJ26	VCC_SM37	AJ1	VCC_SM79
AH26	VCC_SM38	AH1	VCC_SM80
AJ25	VCC_SM39	AG1	VCC_SM81
AH25	VCC_SM40	AF1	VCC_SM82
AJ24	VCC_SM41	AE1	VCC_SM83
AH24	VCC_SM42	AD1	VCC_SM84
BA23	VCC_SM43	AC1	VCC_SM85
AJ23	VCC_SM44	AB1	VCC_SM86
BA22	VCC_SM45	AA1	VCC_SM87
AY22	VCC_SM46	Y1	VCC_SM88
AW22	VCC_SM47	W1	VCC_SM89
AV22	VCC_SM48	V1	VCC_SM90
AU22	VCC_SM49	U1	VCC_SM91
AT22	VCC_SM50	T1	VCC_SM92
AR22	VCC_SM51	R1	VCC_SM93
AP22	VCC_SM52	P1	VCC_SM94
AK22	VCC_SM53	N1	VCC_SM95
AJ22	VCC_SM54	M1	VCC_SM96
AK21	VCC_SM55	L1	VCC_SM97
AK20	VCC_SM56	K1	VCC_SM98
BA19	VCC_SM57	J1	VCC_SM99
AY19	VCC_SM58	H1	VCC_SM100
AW19	VCC_SM59	G1	VCC_SM101
AV19	VCC_SM60	F1	VCC_SM102
AU19	VCC_SM61	E1	VCC_SM103
AT19	VCC_SM62	D1	VCC_SM104
AR19	VCC_SM63	BK1	VCC_SM105
AP19	VCC_SM64	BJ1	VCC_SM106
AK19	VCC_SM65	BH1	VCC_SM107
AJ19	VCC_SM66		
AH19	VCC_SM67		
AJ17	VCC_SM68		
AH17	VCC_SM69		
AJ16	VCC_SM70		
AH16	VCC_SM71		
BA15	VCC_SM72		
AY15	VCC_SM73		
AW15	VCC_SM74		
AV15	VCC_SM75		
AU15	VCC_SM76		
AT15	VCC_SM77		
AR15	VCC_SM78		
AJ15	VCC_SM79		
AJ14	VCC_SM80		
AJ13	VCC_SM81		
AH13	VCC_SM82		
AK12	VCC_SM83		
AJ12	VCC_SM84		
AH12	VCC_SM85		
AG12	VCC_SM86		
AK11	VCC_SM87		
AJ11	VCC_SM88		
AY8	VCC_SM89		
AW8	VCC_SM90		
AV8	VCC_SM91		
AT8	VCC_SM92		
AR8	VCC_SM93		
AP8	VCC_SM94		
BA6	VCC_SM95		
AY6	VCC_SM96		
AV6	VCC_SM97		
AT6	VCC_SM98		
AR6	VCC_SM99		
AP6	VCC_SM100		
AL6	VCC_SM101		
AK6	VCC_SM102		
AJ6	VCC_SM103		
AV1	VCC_SM104		
AJ1	VCC_SM105		
	VCC_SM106		
	VCC_SM107		

NB_VCCSM_LF4
NB_VCCSM_LF5

C1614 0.47uF 20% 6.3V CERM-X5R 402

C1613 0.47uF 20% 6.3V CERM-X5R 402

C1615 0.47uF 20% 6.3V CERM-X5R 402
63 19 14 =PP1V8_S3_MEM_NB
Layout Note: Place near pin BA23

C1620 10uF 20% 6.3V X5R 603

C1621 10uF 20% 6.3V X5R 603

Layout Note: Place in cavity

C1610 0.47uF 20% 6.3V CERM-X5R 402
Layout Note: Place near pin BA15

NB_VCCSM_LF2
NB_VCCSM_LF1

C1612 0.47uF 20% 6.3V CERM-X5R 402

C1611 0.47uF 20% 6.3V CERM-X5R 402

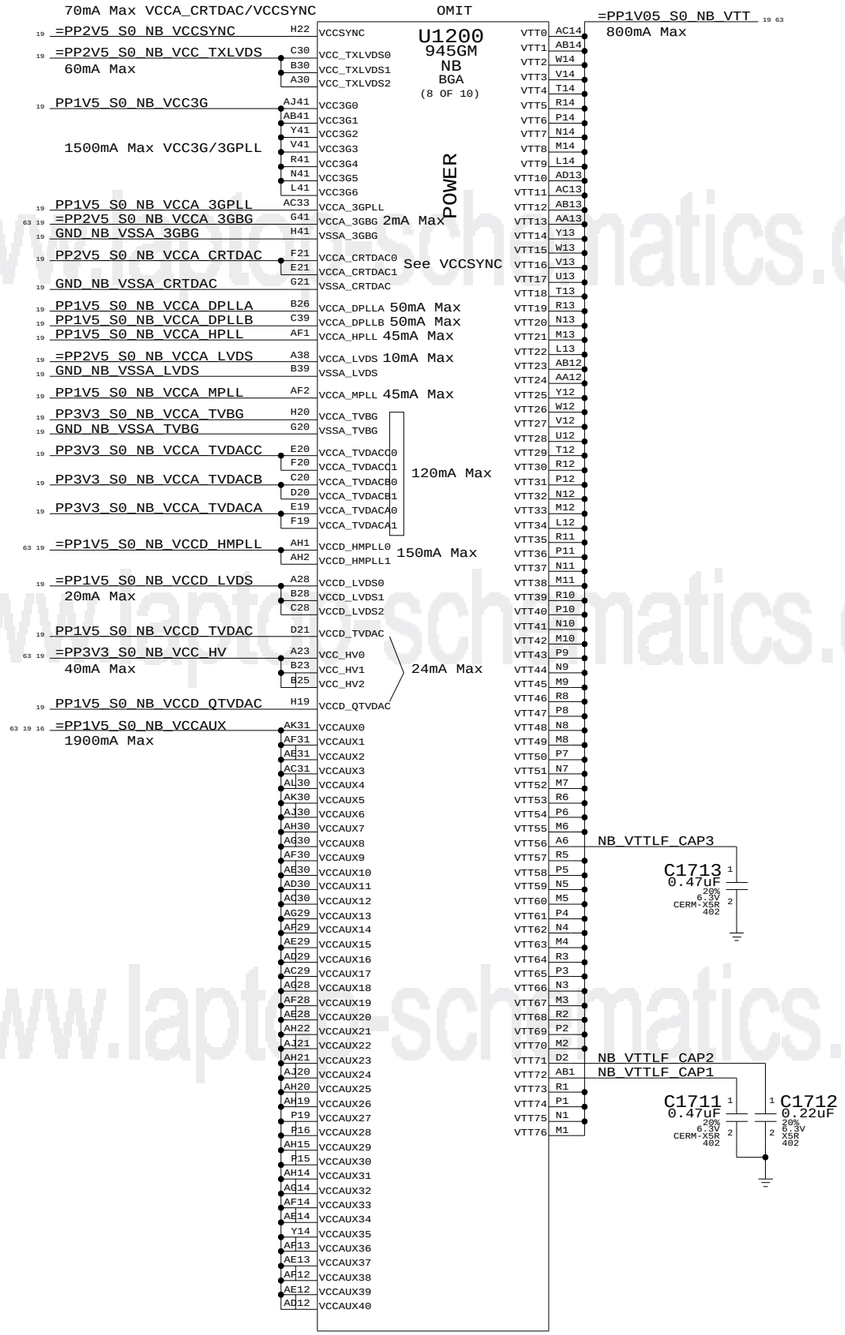
NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE	SHT	OF
NONE	16	104



NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 17 OF 104	

OMIT

U1200
945GM
NB
BGA
(9 OF 10)

VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

OMIT

U1200
945GM
NB
BGA
(10 OF 10)

VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE	SHT	OF
NONE	18	104

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	IN	=PPVCORE_S0_NB	1500mA Max
	IN	=PP1V05_S0_FSB_NB	10mA Max?
	IN	=PP1V05_S0_NB_VTT	800mA Max
	IN	=PP1V05_S0_NB_CRT	?mA Max
3674mA Max	IN	=PP1V5_S0_NB	?mA Max
	IN	=PP1V5_S0_NB_3G	1500mA Max
	IN	=PP1V5_S0_NB_3GPLL	
	IN	=PP1V5_S0_NB_PCIE	?mA Max
	IN	=PP1V5_S0_NB_PLL	100mA Max
	IN	=PP1V5_S0_NB_TVDAC	24mA Max
	IN	=PP1V5_S0_NB_VCCD_HMPLL	150mA Max
	IN	=PP1V5_S0_NB_VCCAUX	1900mA Max
3200mA Max	IN	=PP1V8_S3_MEM_NB	3200mA Max
	IN	=PP2V5_S0_NB_VCCSYNC	70mA Max
132mA Max	IN	=PP2V5_S0_NB_VCC_TXLVDS	60mA Max
	IN	=PP2V5_S0_NB_VCCA_3GBG	2mA Max
	IN	=PP3V3_S0_NB	?mA Max
40mA Max?	IN	=PP3V3_S0_NB_VCC_HV	40mA Max

63 19 =PP1V05_S0_NB_CRT

- CRT_RED — 13
- CRT_GREEN — 13
- CRT_BLUE — 13
- CRT_RED_L — 13
- CRT_GREEN_L — 13
- CRT_BLUE_L — 13
- CRT_IREF — 13
- CRT_HSYNC_R — 13
- CRT_VSYNC_R — 13

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK — 13

TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA — 13

63 19 =PP1V5_S0_NB_TVDAC

- TV_DACA_OUT — 13
- TV_DACB_OUT — 13
- TV_DACC_OUT — 13
- TV_IREF — 13
- TV_IRTNA — 13
- TV_IRTNB — 13
- TV_IRTNC — 13

- TP_LVDS_BKLTCTL (MAKE_BASE=TRUE) — LVDS_BKLTCTL — 13
- TP_LVDS_BKLTEN (MAKE_BASE=TRUE) — LVDS_BKLTEN — 13
- TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA — 13
- TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB — 13
- TP_LVDS_DDC_CLK (MAKE_BASE=TRUE) — LVDS_DDC_CLK — 13
- TP_LVDS_DDC_DATA (MAKE_BASE=TRUE) — LVDS_DDC_DATA — 13
- NC_LVDS_IBG (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_IBG — 13
- TP_LVDS_VDDEN (MAKE_BASE=TRUE) — LVDS_VDDEN — 13
- NC_LVDS_VREFH (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_VREFH — 13
- TP_LVDS_VREFL (MAKE_BASE=TRUE) — LVDS_VREFL — 13
- NC_LVDS_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_P — 13
- NC_LVDS_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_N — 13
- NC_LVDS_A_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_P<2..0> — 13
- NC_LVDS_A_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_N<2..0> — 13
- NC_LVDS_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_P — 13
- NC_LVDS_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_N — 13
- NC_LVDS_B_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_P<2..0> — 13
- NC_LVDS_B_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_N<2..0> — 13
- NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34 — 14
- NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35 — 14
- NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27 — 14
- NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28 — 14
- TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK — 14
- TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA — 14

(MCH LVDS DATA/CLK TX 2.5V PWR)
=PP2V5_S0_NB_VCC_TXLVDS — 17 19

(MCH LVDS DIGITAL 1.5V PWR)
=PP1V5_S0_NB_VCCD_LVDS — 17

(MCH LVDS ANALOG 2.5V PWR)
=PP2V5_S0_NB_VCCA_LVDS — 17

NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE) — GND_NB_VSSA_LVDS — 17

63 19 16 =PPVCORE_S0_NB

(MCH CRTDAC ANALOG 2.5V PWR)
PP2V5_S0_NB_VCCA_CRTDAC — 17

GND_NB_VSSA_CRTDAC — 17

(MCH H/V SYNC 2.5V PWR)
=PP2V5_S0_NB_VCCSYNC — 17 19

63 19 =PP1V5_S0_NB_TVDAC

(MCH TVDAC DEDICATED PWR 1.5V)
PP1V5_S0_NB_VCCD_TVDAC — 17

(MCH TVDAC DIGITAL QUIET 1.5V PWR)
PP1V5_S0_NB_VCCD_QTVDAC — 17

(MCH TV OUT CHANNEL A 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACA — 17

(MCH TV OUT CHANNEL B 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACB — 17

(MCH TV OUT CHANNEL C 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACC — 17

(MCH TV DAC BAND GAP 3.3V PWR)
PP3V3_S0_NB_VCCA_TVBG — 17

GND_NB_VSSA_TVBG — 17

(MCH DISPLAY A PLL 1.5V PWR)
TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLA — 17

(MCH DISPLAY B PLL 1.5V PWR)
TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLB — 17

- NB_CLK_DREFCLKIN_P — 14
- NB_CLK_DREFCLKIN_N — 14
- NB_CLK_DREFSSCLKIN_P — 14
- NB_CLK_DREFSSCLKIN_N — 14

63 19 16 =PPVCORE_S0_NB
1500mA Max

GMCH CORE PWR 1.05V BYPASS

CRITICAL
C1900 470uF 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1uF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

MCH VTT BYPASS
(MCH FSB 1.05V PWR)

63 19 17 =PP1V05_S0_NB_VTT
800mA Max

(SHARE C0940 470UF)

C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603

Layout Note: Place in cavity

C1967 0.22uF 20% 6.3V X5R 402

Layout Note: Place on the edge

MCH VCC_HV BYPASS
(MCH HV BUFFER 3.3V PWR)

63 19 17 =PP3V3_S0_NB_VCC_HV
40mA Max

C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 10% 16V CERM 402

MCH VCCA_3GBG BYPASS
(MCH PCIE/DMI BAND GAP 2.5V PWR)

63 19 17 =PP2V5_S0_NB_VCCA_3GBG
2mA Max

C1916 0.1uF 20% 16V CERM 402

GMCH VCCAUX FILTER
(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

63 19 17 16 =PP1V5_S0_NB_VCCAUX
1900mA Max

C1918 0.1uF 20% 16V CERM 402

63 19 =PP1V5_S0_NB_PLL
100mA Max

L1934 FERR-120-OHM-0.2A 0603

GMCH VCCA_HPLL FILTER
(HOST PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_HPLL — 17
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
45mA Max

C1934 22UF 20% 6.3V CERM 805
C1935 0.1uF 20% 10V CERM 402

L1936 FERR-120-OHM-0.2A 0603

GMCH VCCA_MPLL FILTER
(MCH MEMORY PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_MPLL — 17
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
45mA Max

C1936 22UF 20% 6.3V CERM 805
C1937 0.1uF 20% 10V CERM 402

63 19 =PP1V5_S0_NB_3G
1500mA Max

L1970 91nH 1210

Layout Note: Place L and C close to MCH

C1970 220UF 20% 2.5V POLY SMB2

GMCH VCC3G FILTER
(PCI-E/DMI ANALOG 1.5V PWR)
PP1V5_S0_NB_VCC3G — 17
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603

Layout Note: 10uF caps should be close to MCH on opposite side.

1500mA Max

63 19 =PP1V5_S0_NB_3GPLL
1500mA Max

L1975 1.0UH-220MA-0.12-OHM 0805

PP1V5_S0_NB_3GPLL_F
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=1.5V

R1975 0.51 1% 1/16W MF-LF 402

GMCH VCCA_3GPLL FILTER
(3GIO PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_3GPLL — 17
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

C1975 10UF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402

Layout Note: 3GPLL 10uF cap should be placed in cavity

GND_NB_VSSA_3GBG — 17

Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 19 OF 104	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14 19 20 63
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14 19 20 63
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14 19 20 63
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

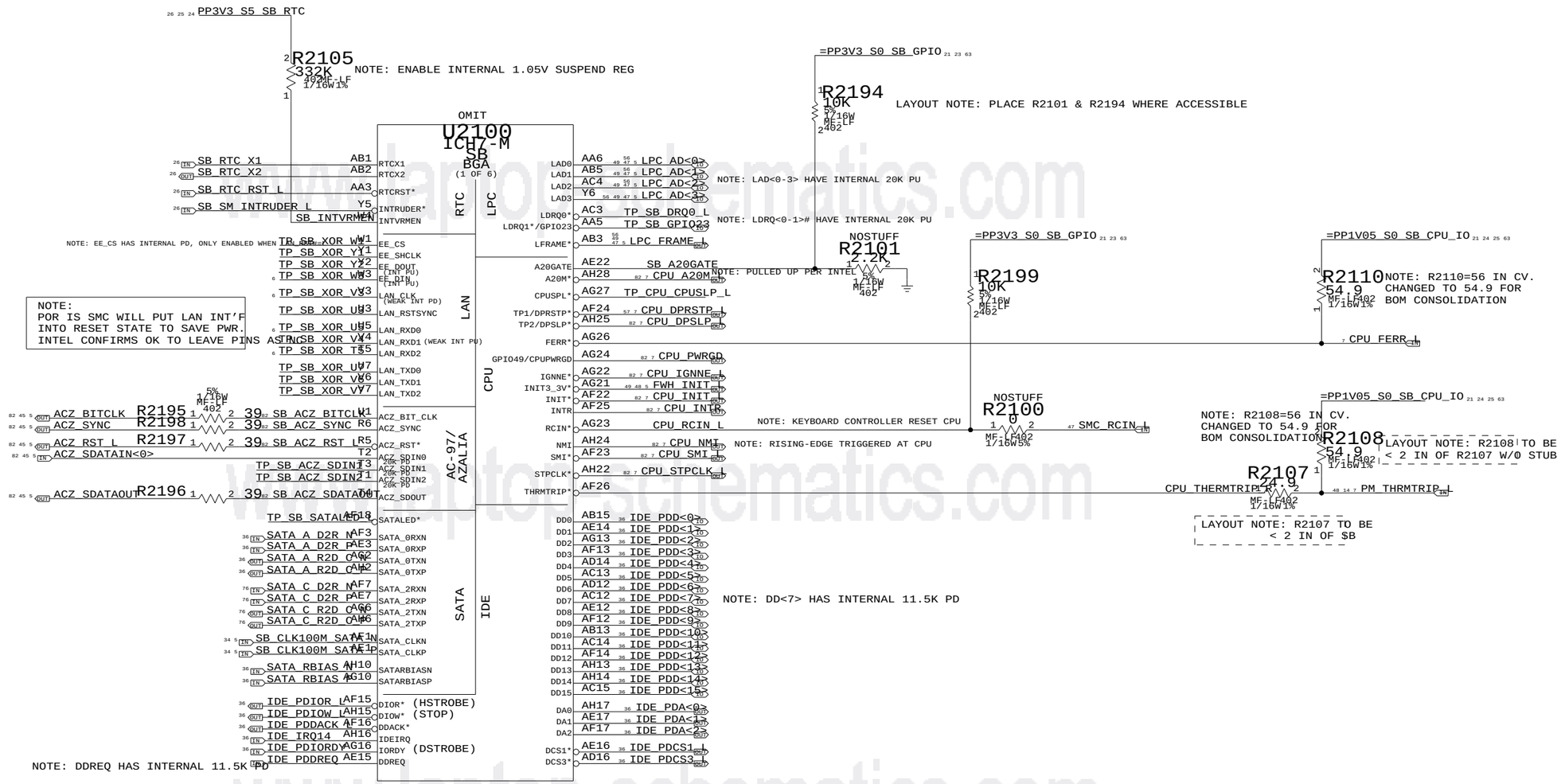
PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 20 OF 104	



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 21 OF 104	

=PP3V3_S5_SB_USB

R2225 10K 5% 1/16W MF-LF 2402 — USB_A_OC_L
R2200 10K 5% 1/16W MF-LF 2402 — USB_B_OC_L
R2250 10K 5% 1/16W MF-LF 2402 — USB_C_OC_L (USB_C_OC_PU)
R2255 10K 5% 1/16W MF-LF 2402 — USB_D_OC_L (USB_D_OC_PU)
R2251 10K 5% 1/16W MF-LF 2402 — USB_E_OC_L (USB_E_OC_PU)
R2227 10K 5% 1/16W MF-LF 2402 — SB_GPIO29
R2228 10K 5% 1/16W MF-LF 2402 — SB_GPIO30
R2226 10K 5% 1/16W MF-LF 2402 — SB_GPIO31 (USB_G_OC_PU)

=PP3V3_S5_SB_IO

R2205 10K 5% 1/16W MF-LF 402
R2206 10K 5% 1/16W MF-LF 402 (NOSTUFF)
R2207 10K 5% 1/16W MF-LF 402

SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO

OMIT

U2100
ICH7-M
SB
BGA
(3 OF 6)

PCI-EXP

PCIE_A_D2R_N	F26 PERN1
PCIE_A_D2R_P	F25 PERP1
PCIE_A_R2D_C_N	G28 PETN1
PCIE_A_R2D_C_P	G27 PETP1
PCIE_B_D2R_N	H26 PERN2
PCIE_B_D2R_P	H25 PERP2
PCIE_B_R2D_C_N	G28 PETN2
PCIE_B_R2D_C_P	G27 PETP2
PCIE_C_D2R_N	K26 PERN3
PCIE_C_D2R_P	K25 PERP3
PCIE_C_R2D_C_N	J28 PETN3
PCIE_C_R2D_C_P	J27 PETP3
PCIE_D_D2R_N	M26 PERN4
PCIE_D_D2R_P	M25 PERP4
PCIE_D_R2D_C_N	L28 PETN4
PCIE_D_R2D_C_P	L27 PETP4
PCIE_E_D2R_N	P26 PERN5
PCIE_E_D2R_P	P25 PERP5
PCIE_E_R2D_C_N	N28 PETN5
PCIE_E_R2D_C_P	N27 PETP5
PCIE_F_D2R_N	T25 PERN6
PCIE_F_D2R_P	T24 PERP6
PCIE_F_R2D_C_N	R28 PETN6
PCIE_F_R2D_C_P	R27 PETP6

SPI

R2	SPI_CLK (INT PD)
P6	SPI_CS*
P1	SPI_ARB (INT PU)
P5	SPI_MOSI
P2	SPI_MISO

USB

D3	USB_A_OC_L → OC0*
C4	USB_B_OC_L → OC1*
D5	USB_C_OC_L → OC2*
D4	USB_D_OC_L → OC3*
E5	USB_E_OC_L → OC4*
C3	SB_GPIO29 → OC5*/GPIO29
A2	SB_GPIO30 → OC6*/GPIO30
B3	SB_GPIO31 → OC7*/GPIO31

DMI

V26	DMI0RXN — DMI_N2S_N<0>
V25	DMI0RXP — DMI_N2S_P<0>
U28	DMI0TXN — DMI_S2N_N<0>
U27	DMI0TXP — DMI_S2N_P<0>
Y26	DMI1RXN — DMI_N2S_N<1>
Y25	DMI1RXP — DMI_N2S_P<1>
W28	DMI1TXN — DMI_S2N_N<1>
W27	DMI1TXP — DMI_S2N_P<1>
AB26	DMI2RXN — DMI_N2S_N<2>
AB25	DMI2RXP — DMI_N2S_P<2>
AA28	DMI2TXN — DMI_S2N_N<2>
AA27	DMI2TXP — DMI_S2N_P<2>
AD25	DMI3RXN — DMI_N2S_N<3>
AD24	DMI3RXP — DMI_N2S_P<3>
AC28	DMI3TXN — DMI_S2N_N<3>
AC27	DMI3TXP — DMI_S2N_P<3>
AE28	DMI_CLKN — SB_CLK100M_DMI_N
AE27	DMI_CLKP — SB_CLK100M_DMI_P
C25	DMI_ZCOMP
D25	DMI_IRCOMP — R2203 24.9 1/16W MF-LF 1% 402

PP1V5_S0_SB_VCC1_5_B

LAYOUT NOTE:
PLACE R2203 < 1/2 IN FROM SB

USB

F1	USBP0N — USB_A_N
F2	USBP0P — USB_A_P — EXTERNAL 0
G4	USBP1N — USB_B_N
G3	USBP1P — USB_B_P — AIRPORT (MINI-PCIE)
H1	USBP2N — USB_C_N
H2	USBP2P — USB_C_P — EXTERNAL 1
J4	USBP3N — USB_D_N
J3	USBP3P — USB_D_P — CAMERA
K1	USBP4N — USB_E_N
K2	USBP4P — USB_E_P — EXTERNAL 2
L4	USBP5N — USB_F_N
L5	USBP5P — USB_F_P — CF/SD
M1	USBP6N — USB_G_N
M2	USBP6P — USB_G_P — BT
N4	USBP7N — USB_H_N
N3	USBP7P — USB_H_P — IR
D2	USBRBIAS*
D1	USBRBIAS — USB_RBIAS_PN — R2204 22.6 1/16W MF-LF 1% 402 — VOLTAGE=0V

NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD

LAYOUT NOTE:
PLACE R2204 < 1/2 IN FROM SB

=PP3V3_S0_SB

R2298 10K 5% 1/16W MF-LF 2402
R2299 10K 5% 1/16W MF-LF 2402

NOTE: GNT1#, GNT3# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H

PCI

PCI_AD<0>	E18 AD0
PCI_AD<1>	C18 AD1
PCI_AD<2>	A16 AD2
PCI_AD<3>	F18 AD3
PCI_AD<4>	E16 AD4
PCI_AD<5>	A18 AD5
PCI_AD<6>	E17 AD6
PCI_AD<7>	A17 AD7
PCI_AD<8>	A15 AD8
PCI_AD<9>	C14 AD9
PCI_AD<10>	E14 AD10
PCI_AD<11>	D14 AD11
PCI_AD<12>	B12 AD12
PCI_AD<13>	C13 AD13
PCI_AD<14>	B13 AD14
PCI_AD<15>	C12 AD15
PCI_AD<16>	E12 AD16
PCI_AD<17>	C11 AD17
PCI_AD<18>	D11 AD18
PCI_AD<19>	A11 AD19
PCI_AD<20>	A10 AD20
PCI_AD<21>	F11 AD21
PCI_AD<22>	F10 AD22
PCI_AD<23>	E9 AD23
PCI_AD<24>	D9 AD24
PCI_AD<25>	B9 AD25
PCI_AD<26>	A8 AD26
PCI_AD<27>	A6 AD27
PCI_AD<28>	C7 AD28
PCI_AD<29>	B6 AD29
PCI_AD<30>	E6 AD30
PCI_AD<31>	D6 AD31
PCI_FRAME_L	F16 FRAME*
	C/BE0* B15 PCI_C_BE_L<0>
	C/BE1* C12 PCI_C_BE_L<1>
	C/BE2* D12 PCI_C_BE_L<2>
	C/BE3* C15 PCI_C_BE_L<3>
	IRDY* A7 PCI_IRDY
	PAR E10 PCI_PAR
	PCICLK A9 PCI_CLK_SB
	DEVSEL* A12 PCI_DEVSEL_L
	PERR* C9 PCI_PERR
	PLOCK* E11 PCI_LOCK
	SERR* B10 PCI_SERR
	STOP* F15 PCI_STOP
	TRDY* F14 PCI_TRDY
	PLTRST* C26 PLT_RST
	PCIRST* B18 PCI_RST
	REQ0* D7 PCI_REQ0_L
	GNT0* E7 TP_PCI_GNT0
	REQ1* C16 PCI_REQ1
	GNT1* D16 TP_PCI_GNT1
	REQ2* C17 PCI_REQ2
	GNT2* D17 TP_PCI_GNT2
	REQ3* E13 PCI_REQ3_L
	GNT3* F13 PCI_GNT3_L
	REQ4*/GPIO22 A13
	GNT4*/GPIO48 A14 TP_PCI_GNT4_L
	GPIO1/REQ5* C8
	GPIO17/GNT5* D8
	(INT 20K PU) B19 TP_PCI_PME_L

INT I/F

INT_PIRQA_L	A3 PIRQA*
INT_PIRQB_L	B4 PIRQB*
INT_PIRQC_L	C5 PIRQC*
INT_PIRQD_L	B5 PIRQD*
	G8 GPIO2/PIRQE* — SB_GPIO2
	F7 GPIO3/PIRQF* — SB_GPIO3
	F8 GPIO4/PIRQG* — SB_GPIO4
	G7 GPIO5/PIRQH* — ODD_PWR_EN_L

MISC

NOTE: CHANGE SYMBOL TO RSVD[1-9]

TP_SB_XOR_AE5	AE5 RSVD0
TP_SB_XOR_AD5	AD5 RSVD1
TP_SB_XOR_AG4	AG4 RSVD2
TP_SB_XOR_AH4	AH4 RSVD3
TP_SB_XOR_AG9	AG9 RSVD4
	AE9 RSVD5 — TP_SB_XOR_AE9
	AG8 RSVD6 — TP_SB_XOR_AG8
	AH8 RSVD7 — TP_SB_XOR_AH8
	F21 RSVD8 — TP_SB_RSVD8 (PU TP3, INTERNAL 20K PU)
	AH20 MCH_SYNC* — NB_SB_SYNC_L

SB_CRT_TVOUT_MUX (NOTE: FWH_WP_L NOT USED)
PCI_PME_FW_L
BOOT_LPC_SPI_L

R2211 1K 5% 1/16W MF-LF 402

BOM NOTE FOR PD ON PCI_GNT3_L:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IF SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)

SB BOOT BIOS SELECT

STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT) 11	UNSTUFF	UNSTUFF
PCI 10	UNSTUFF	STUFF
SPI 01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

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NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21 23 63

=PP3V3_S5_SB 23 25 63

NO_REBOOT_MODE

RP2300 10K 5% 1/16W 5M-LF

R2318 10K 1/16W 402 2MF-LF 5%
R2395 8.2K 1/16W 402 2MF-LF 5%
R2396 10K 1/16W 402 2MF-LF 5%
R2397 8.2K 1/16W 402 2MF-LF 5%
R2327 10K 1/16W 402 2MF-LF 5%
R2326 10K 1/16W 402 2MF-LF 5%
R2323 1K 1/16W 402 2MF-LF 5%

=PP3V3_S5_SB 63 25 23

R2398 1K 1/16W 402 2MF-LF 5%
R2320 10K 1/16W 402 2MF-LF 5%
R2317 10K 1/16W 402 2MF-LF 5%
R2316 10K 1/16W 402 2MF-LF 5%

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SMB_CLK 27 TO
SMB_DATA 27 TO
SMB_LINK_ALERT_L
SMLINK<0>
SMLINK<1>
NOT USED
PM_RI_L
SB_SPKR
PM_SUS_STAT_L 56 49 48 47 5 OUT
PM_SYSRST_L 47 26 5 IN
PM_BMBUSY_L 14 IN
SMB_ALERT_L
NOTE: RESERVED FOR FUTURE
PM_STPPCI_L 33 OUT
PM_STPCPU_L 33 OUT
SB_GPIO26
BIOS_REC 23
FWH_MFG_MODE 23
PM_CLKRUN_L 56 49 47 40 5 TO
RESERVED FOR MOBILE AZALIA DOCKING INTF
TP_AZ_DOCK_EN
TP_AZ_DOCK_RST
PCIE_WAKE_L 45 37 5 IN
INT_SERIRQ 56 49 47 5 TO
PM_THRM_L 47 IN
VR_PWRGD_CK410 26 IN
TP_SB_GPIO6 TO
SMC_RUNTIME_SCI_L 47 IN
SMC_EXTSMI_L 47 IN

SMB:
C22 SMBCLK
B22 SMBDATA
A16 SMLINKALERT*
B25 SMLINK0
A25 SMLINK1
A28 RI*
A19 SPKR (INT WEAK PD)
A27 SUS_STAT*
A22 SYS_RST*
AB18 GPIO0/BM_BUSY*
B23 GPIO11/SMBALERT*
AC20 GPIO18/STPPCI*
AF21 GPIO20/STPCPU*
A21 GPIO26
B21 GPIO27
E23 GPIO28
AG18 GPIO32/CLKRUN*
AC19 GPIO33/AZ_DOCK_EN*
U2 GPIO34/AZ_DOCK_RST*
F20 WAKE*
AH21 SERIRQ
AF20 THRM*
AD22 VRMPWRGD
AG21 GPIO6
AC18 GPIO7
E21 GPIO8

SATA GPIO:
AF19 SB_GPIO21 100 1% 1/16W 2 R2302
AH18 SB_GPIO19 100 1% 1/16W 2 R2303
AH19
AE19 SB_GPIO36 100 1% 1/16W 2 R2305
SATA_C_DET_L 36 IN

CLKS:
AC1 CLK14 — SB_CLK14P3M_TIMER 34 IN
B2 CLK48 — SB_CLK48M_USBCTLR 34 IN
C20 SUSCLK — SUS_CLK_SB 8 OUT

PWR MNGT:
B24 SLP_S3* — PM_SLP_S3_L 62 47 41 OUT
D23 SLP_S4* — PM_SLP_S4_L 62 47 39 OUT
F22 SLP_S5* — PM_SLP_S5_L 48 47 OUT
AA4 PWROK — PM_SB_PWROK 26 IN
AC22 GPIO16/DPRSLPVR — PM_DPRSLPVR 82 57 14 OUT
C21 TP0/BATLOW* — PM_BATLOW_L 47 IN
(INT 20K PU) PWRBTN* — C23 PM_PWRBTN_L 47 IN
LAN_RST* — C19 PM_LAN_ENABLE 47 IN
RSMRST* — Y4 PM_RSMRST_L 47 IN

NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR

GPIO:
E20 GPIO9 — SMS_INT_L 48 47 IN
A20 GPIO10 — SMC_SB_NMI 47 IN
F19 GPIO12 — PATA_PWR_EN_L 23 OUT (DEF=GPI)
E19 GPIO13
R4 GPIO14 — IDE_RESET_L 36 OUT (DEF=GPI)
E22 GPIO15 — SV_SET_UP 5 23 49
R3 GPIO24 — CRB_SV_DET 23
D20 GPIO25 — TP_SB_GPIO25_DO_NOT_USE
AD21 OD GPIO35 — SB_CLK100M_SATA_OE_L 33 OUT
AD20 GPIO38 — TP_SB_GPIO38 NC
AE20 GPIO39 — SATA_C_PWR_EN_L 23 OUT (DEF=GPI)

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB_PM 11 26 63

R2319 10K 1/16W 402 2MF-LF 5%
R2343 8.2K 1/16W 402 2MF-LF 5%

R2399 100K 5% 1/16W 402 2MF-LF

SMC_WAKE_SCI_L 47 IN

=PP3V3_S5_SB 63 25 23

R2306 10K 1/16W 402 2MF-LF 5% NOSTUFF
R2308 10K 1/16W 402 2MF-LF 5%

SV_SET_UP 5 23 49
CRB_SV_DET 23

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

R2307 10K 1/16W 402 2MF-LF 5%
R2309 0 1/16W 402 2MF-LF 5% NOSTUFF

=PP3V3_S5_SB 63 25 23

R2313 10K 1/16W 402 2MF-LF 5%
R2310 10K 1/16W 402 2MF-LF 5%

FWH_MFG_MODE 23
BIOS_REC 23

R2314 0 1/16W 402 2MF-LF 5% NOSTUFF
R2311 10K 1/16W 402 2MF-LF 5% NOSTUFF

=PP3V3_S5_SB 23 25 63

R2390 10K 5% 1/16W 2MF-LF 2402

PATA_PWR_EN_L 23

=PP3V3_S0_SB_GPIO 21 23 63

R2388 10K 5% 1/16W 2MF-LF 2402

SATA_C_PWR_EN_L 23

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VSS

A4	A23	N24	P24
R18	U14	V27	AA24
AB27	AD11	B1	D10
F4	G18	J1	L24
M17	N14	N17	N18
N25	N26	P3	P4
P12	P13	P14	P15
P16	P17	P27	P28
R1	R11	R12	R13
R14	R15	R16	R17
T6	T12	T13	T14
T15	T16	T17	U4
U12	U13	U15	U16
U17	U24	U25	U26
V2	V13	V15	V24
V28	W6	W24	W25
W26	Y3	Y24	Y27
Y28	AA1	AA25	AA26
AB4	AB6	AB11	AB14
AB16	AB19	AB21	AB24
AB28	AC2	AC5	AC9
AC11	AD1	AE24	AE25
AF2	AF4	AF8	AF11
AF27	AF28	AG1	AG3
AG7	AD3	AD4	AD7
AD8	AD15	AD19	AD23
AE2	AE4	AE8	AE11
AE13	AE18	AE21	B8
B11	B14	B17	B20
B26	B28	C2	C6
C27	D13	D18	D21
D24	E1	E2	E4
E8	E15	F3	F5
F12	F27	F28	G1
G2	G5	G6	G9
G14	G21	G24	G25
G26	H3	H4	H5
H24	H27	H28	J2
J5	J24	J25	J26
K24	K27	K28	L13
L15	L25	L26	M3
M4	M5	M12	M13
M14	M15	M16	M24
M27	M28	N1	N2
N5	N6	N11	N12
N13	N15	N16	AG11
AG14	AG17	AG20	AG25
AH1	AH3	AH7	AH12
AH23	AH27		

0 0

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25 PP5V_S0_SB_V5REF
V5REF

25 PP5V_S5_SB_V5REF_SUS
V5REF_SUS

25 22 PP1V5_S0_SB_VCC1_5_A

VCCA3GP
VCC1_5_B

AA22	AA23	AB22	AB23
AC23	AC24	AC25	AC26
AD26	AD27	AD28	D26
D27	D28	E24	E25
E26	F23	F24	G22
G23	H22	H23	J22
J23	K22	K23	L22
L23	M22	M23	N22
N23	P22	P23	R22
R23	R24	R25	R26
T22	T23	T26	T27
T28	U22	U23	V22
V23	W22	W23	Y22
Y23			

63 25 24 =PP3V3_S0_SB_VCC3_3
VCC3_3

25 PP1V5_S0_SB_VCCDMIPLL
VCCDMIPLL

63 25 =PP1V5_S0_SB_VCC1_5_A_ARX
ARX
VCC1_5_A

AC6	AC7	AD6	AE6
AF5	AF6	AG5	AH5

63 25 =PP1V5_S0_SB_VCCSATAPLL
VCCSATAPLL

63 25 24 =PP3V3_S0_SB_VCC3_3
VCC3_3

63 25 =PP1V5_S0_SB_VCC1_5_A_ATX
ATX
VCC1_5_A

AB9	AC10	AD10	AE10
AF10	AF9	AG9	AH9

63 25 24 =PP3V3_S5_SB_VCCSUS3_3
VCCSUS3_3

63 25 =PP1V5_S0_SB_VCCUSBPLL
VCCUSBPLL

VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE

AH11	AB10	E3	C1
A2	Y7		

VCCLAN1_5
CHANGE SYMBOL TO 1.0V

CORE
VCC1_05

=PPVCORE_S0_SB 25 63

L11	L12	L14	L16
L17	L18	M11	M18
P11	P18	T11	T18
U11	U18	V11	V12
V14	V16	V17	V18

NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

VCC_PAUX
VCCLAN_3_3

=PP3V3_S0_SB_VCCLAN3_3 25 63

V5	V1	W2	W7

VCC3_3/VCCHDA
VCCSUS3_3/VCCSUSHDA

U6 =PP3V3_S0_SB_3V3_1V5_VCCHDA
R7 =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA

NOTE:
VCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

AE23 =PP1V05_S0_SB_CPU_IO 21 25 63
V_CPU_IO
AE26
AH26

AA7 =PP3V3_S0_SB_VCC3_3_IDE 25 63
IDE
VCC3_3

AB12	AB20	AC16	AD13
AD18	AG12	AG15	AG19

A5
PCI
VCC3_3

B13	B16	B7	C10
D15	F9	G11	G12

G16 =PP3V3_S0_SB_VCC3_3_PCI 25 63

VCCRTC
W5 PP3V3_S5_SB_RTC 21 25 26

P7 =PP3V3_S5_SB_VCCSUS3_3 24 25 63
VCCSUS3_3

A24	C24	D19	D22
G19			

USB
VCCSUS3_3

K3	K4	K5	K6
L1	L2	L3	L6
L7	M6	M7	N7

N7 =PP3V3_S5_SB_VCCSUS3_3_USB 25 63

AB17	AC17	T7	F17

VCC1_5_A
G17 =PP1V5_S0_SB_VCC1_5_A 25 63
VCC1_5_A
AB8
VCC1_5_A
AC8

K7
VCCSAUS1_5
CHANGE SYMBOL TO 1.0V
C28 VOLTAGE GENERATED INTERNALLY
G20 SO NO CONNECT HERE

A1
USB CORE
VCC1_5_A

H6	H7	J6	J7

J7 =PP1V5_S0_SB_VCC1_5_A_USB_CORE

SB: 4 OF 4

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

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SCALE NONE

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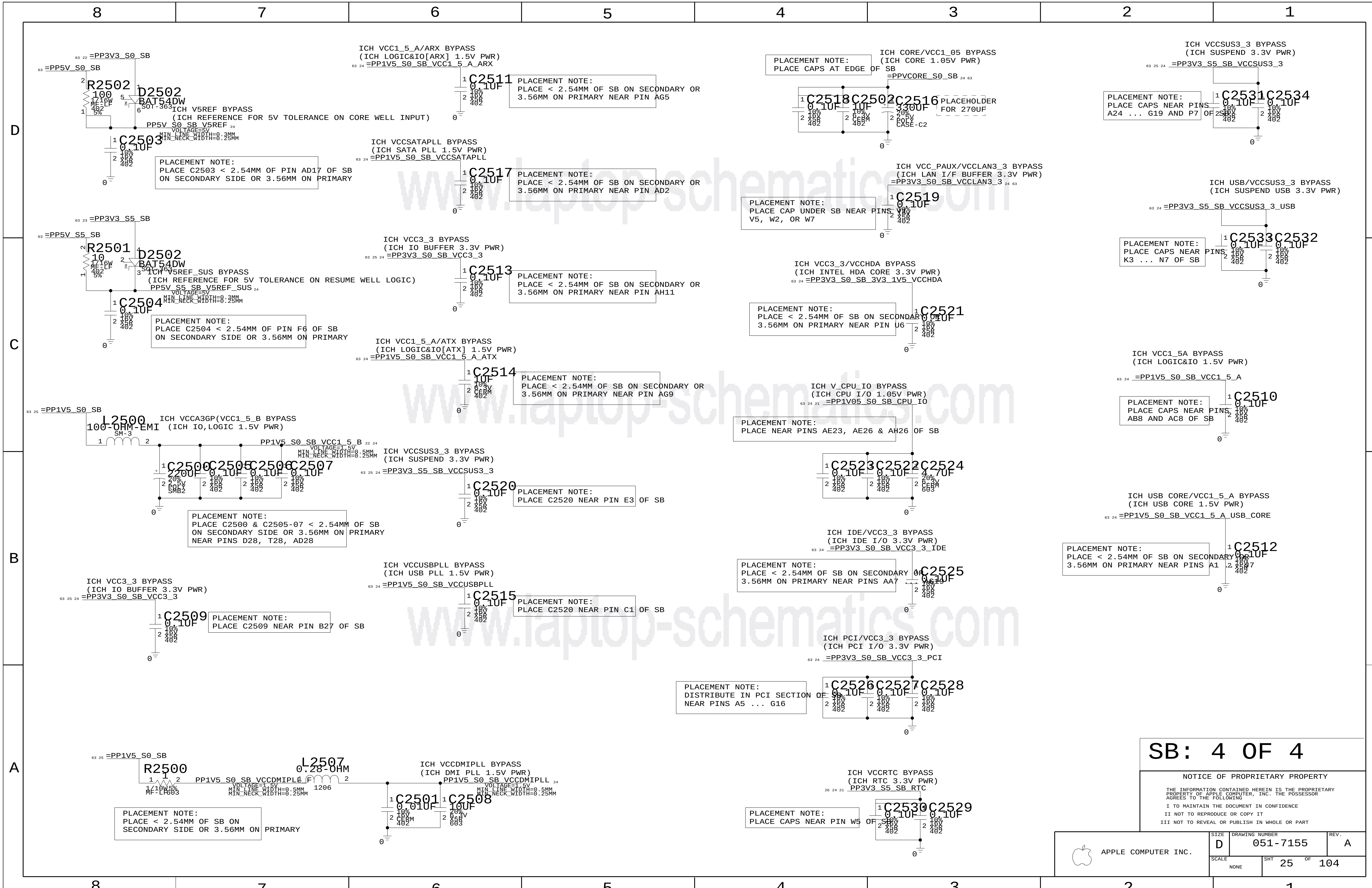

ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ARX
C2511
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG5
=PP3V3_S0_SB
=PP5V_S0_SB
R2502
100
D2502
BAT54DW
SOT-363
ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
PP5V_S0_SB_V5REF
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2503
0.1UF
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
=PP1V5_S0_SB_VCCSATAPLL
C2517
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AD2
=PP3V3_S5_SB
=PP5V_S5_SB
R2501
10
D2502
BAT54DW
ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
PP5V_S5_SB_V5REF_SUS
C2504
0.1UF
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCC3_3
C2513
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ATX
C2514
1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG9
=PP1V5_S0_SB
L2500
100-OHM-EMI
SM-3
ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
PP1V5_S0_SB_VCC1_5_B
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2500 220UF
C2505 0.1UF
C2506 0.1UF
C2507 0.1UF
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3
C2520
0.1UF
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCC3_3
C2509
0.1UF
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
=PP1V5_S0_SB_VCCUSBPLL
C2515
0.1UF
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB
=PP1V5_S0_SB
R2500
L2507
0.28-OHM
PP1V5_S0_SB_VCCDMIPLL
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
PP1V5_S0_SB_VCCDMIPLL
C2501 0.01UF
C2508 10UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
=PPVCORE_S0_SB
C2518 0.1UF
C2502 1UF
C2516 330UF
PLACEHOLDER
FOR 270UF
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCCLAN3_3
C2519
0.1UF
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS V6,
V5, W2, OR W7
ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
=PP3V3_S0_SB_3V3_1V5_VCCHDA
C2521
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
=PP1V05_S0_SB_CPU_IO
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB
C2523 0.1UF
C2522 0.1UF
C2524 4.7UF
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_IDE
C2525
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7 ... AG19
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_PCI
C2526 0.1UF
C2527 0.1UF
C2528 0.1UF
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
PP3V3_S5_SB_RTC
C2530 0.1UF
C2529 0.1UF
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3
C2531 0.1UF
C2534 0.1UF
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF SB
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3_USB
C2533 0.1UF
C2532 0.1UF
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB
ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A
C2510
0.1UF
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
C2512
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1 ... F17
SB: 4 OF 4
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II NOT TO REPRODUCE OR COPY IT
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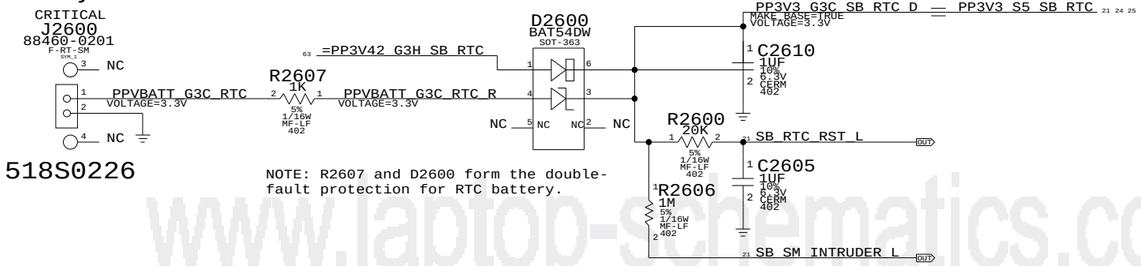
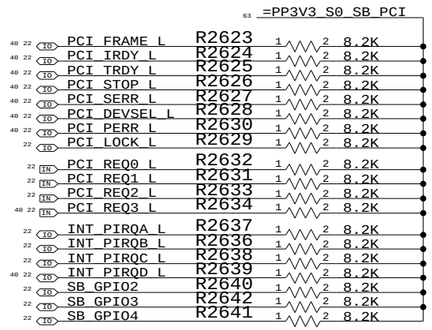
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7155
REV. A
SCALE NONE
SHT 25 OF 104

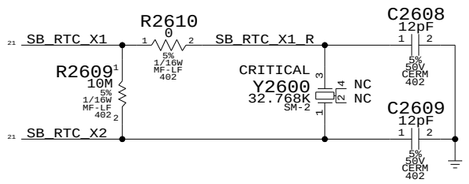
RTC Battery Connector



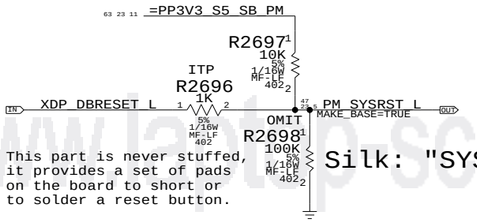
NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



SB RTC Crystal Circuit



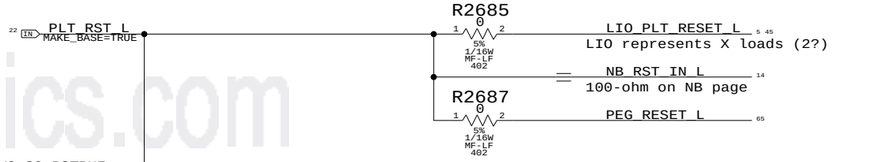
Platform Reset Connections



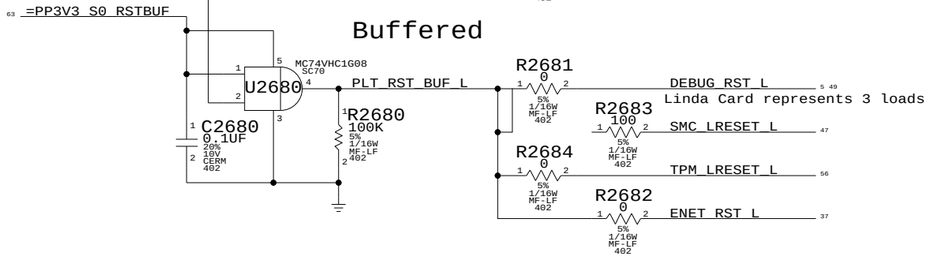
This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"

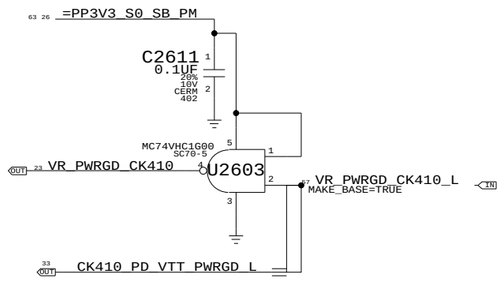
Unbuffered



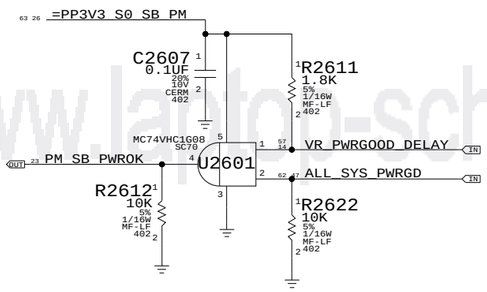
Buffered



Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter



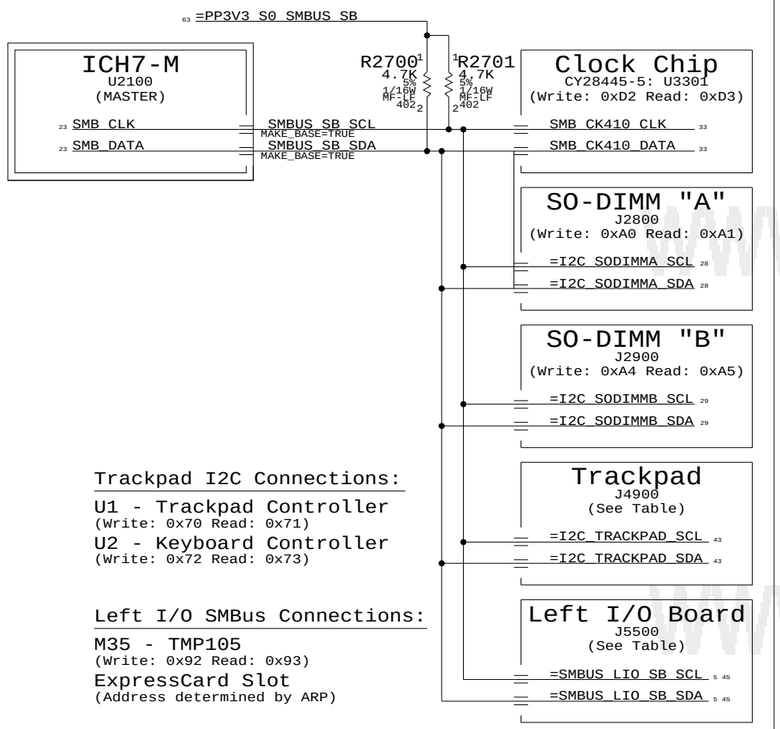
SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

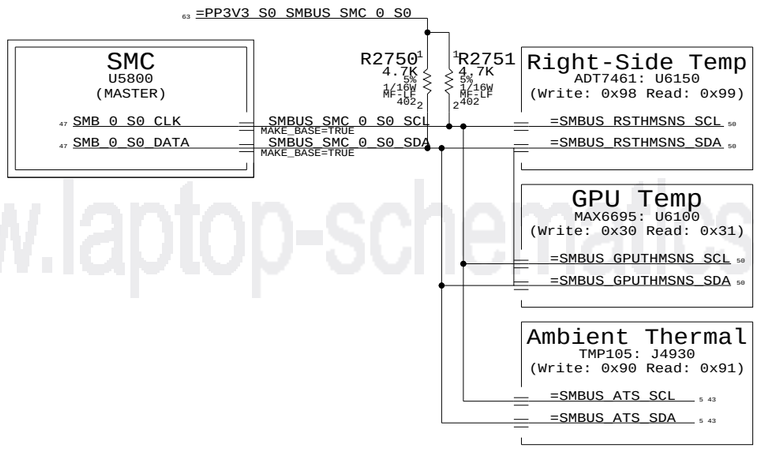
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 26 OF 104	

ICH7-M SMBus Connections

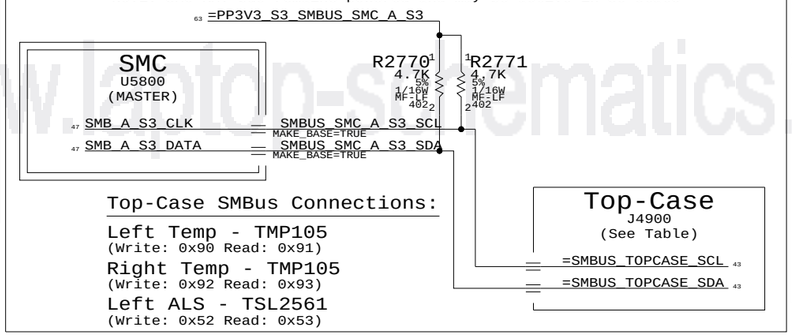


SMC "0" SMBus Connections

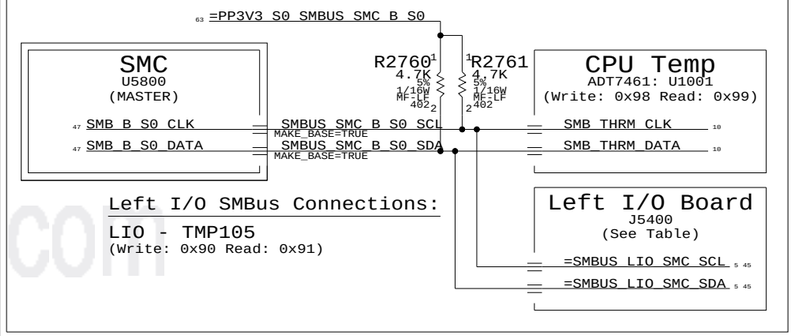


SMC "A" SMBus Connections

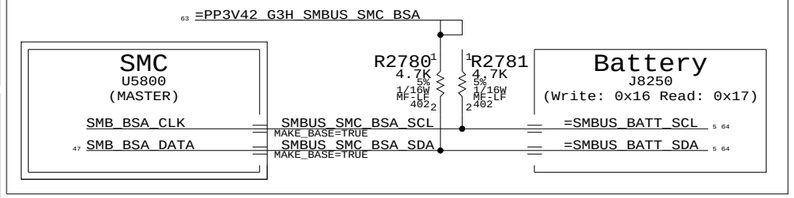
NOTE: SMC RMT bus remains powered and may be active in S3 state



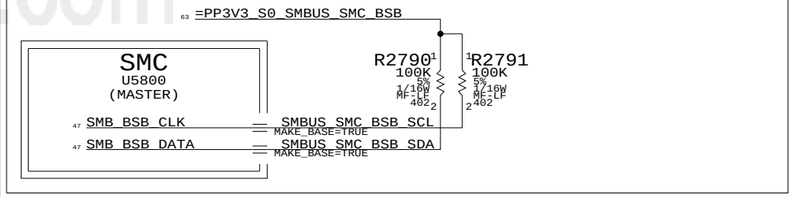
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE	SHT	OF
NONE	27	104

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Lower" (surface-mount) slot

32 29 MEM_VREF

C2801 2.2uF 20% 6.3V CERM 603

C2800 0.1uF 20% 10V CERM 402

63 29 28 =PP1V8_S3_MEM

203 NC

201

CRITICAL J2800 F-RT-SM

DDR2-SODIMM-DUAL

	1A	VREF		2A	VSS0		
	3A	VSS1		4A	DQ4	15	MEM_A_DQ<8>
15	MEM_A_DQ<14>	5A	DQ0	6A	DQ5	15	MEM_A_DQ<12>
15	MEM_A_DQ<13>	7A	DQ1	8A	VSS2		
	9A	VSS4		10A	DM0	15	MEM_A_DM<1>
15	MEM_A_DQS_N<1>	11A	DQS0*	12A	VSS5		
15	MEM_A_DQS_P<1>	13A	DQS0	14A	DQ6	15	MEM_A_DQ<15>
	15A	VSS6		16A	DQ7	15	MEM_A_DQ<9>
15	MEM_A_DQ<10>	17A	DQ2	18A	VSS7		
15	MEM_A_DQ<11>	19A	DQ3	20A	DQ12	15	MEM_A_DQ<2>
	21A	VSS8		22A	DQ13	15	MEM_A_DQ<3>
15	MEM_A_DQ<5>	23A	DQ8	24A	VSS9		
15	MEM_A_DQ<4>	25A	DQ9	26A	DM1	15	MEM_A_DM<0>
	27A	VSS10		28A	VSS11		
15	MEM_A_DQS_N<0>	29A	DQS1*	30A	CK0	14	MEM_CLK_P<0>
15	MEM_A_DQS_P<0>	31A	DQS1	32A	CK0*	14	MEM_CLK_N<0>
	33A	VSS12		34A	VSS13		
15	MEM_A_DQ<6>	35A	DQ10	36A	DQ14	15	MEM_A_DQ<1>
15	MEM_A_DQ<7>	37A	DQ11	38A	DQ15	15	MEM_A_DQ<0>
	39A	VSS14	KEY	40A	VSS15		
	41A	VSS16		42A	VSS17		
15	MEM_A_DQ<19>	43A	DQ16	44A	DQ20	15	MEM_A_DQ<23>
15	MEM_A_DQ<18>	45A	DQ17	46A	DQ21	15	MEM_A_DQ<22>
	47A	VSS18		48A	VSS19		
15	MEM_A_DQS_N<2>	49A	DQS2*	50A	NC0	29 48	DIMM_OVERTEMP_L
15	MEM_A_DQS_P<2>	51A	DQS2	52A	DM2	15	MEM_A_DM<2>
	53A	VSS21		54A	VSS22		
15	MEM_A_DQ<20>	55A	DQ18	56A	DQ22	15	MEM_A_DQ<21>
15	MEM_A_DQ<16>	57A	DQ19	58A	DQ23	15	MEM_A_DQ<17>
	59A	VSS23		60A	VSS24		
15	MEM_A_DQ<28>	61A	DQ24	62A	DQ28	15	MEM_A_DQ<29>
15	MEM_A_DQ<25>	63A	DQ25	64A	DQ29	15	MEM_A_DQ<24>
	65A	VSS25		66A	VSS26		
15	MEM_A_DM<3>	67A	DM3	68A	DQS3*	15	MEM_A_DQS_N<3>
	NC	69A	NC1	70A	DQS3	15	MEM_A_DQS_P<3>
	71A	VSS27		72A	VSS28		
15	MEM_A_DQ<27>	73A	DQ26	74A	DQ30	15	MEM_A_DQ<26>
15	MEM_A_DQ<30>	75A	DQ27	76A	DQ31	15	MEM_A_DQ<31>
	77A	VSS29		78A	VSS30		
30 14	MEM_CKE<0>	79A	CKE0	80A	NC/CKE1	14 30	MEM_CKE<1>
	81A	VDD0		82A	VDD1		
	NC	83A	NC2	84A	NC/A15	6	MEM_A_A<15>
30 15	MEM_A_BS<2>	85A	BA2	86A	NC/A14	6	MEM_A_A<14>
	87A	VDD2		88A	VDD3		
30 15	MEM_A_A<12>	89A	A12	90A	A11	15 30	MEM_A_A<11>
30 15	MEM_A_A<9>	91A	A9	92A	A7	15 30	MEM_A_A<7>
30 15	MEM_A_A<8>	93A	A8	94A	A6	15 30	MEM_A_A<6>
	95A	VDD4		96A	VDD5		
30 15	MEM_A_A<5>	97A	A5	98A	A4	15 30	MEM_A_A<4>
30 15	MEM_A_A<3>	99A	A3	100A	A2	15 30	MEM_A_A<2>
30 15	MEM_A_A<1>	101A	A1	102A	A0	15 30	MEM_A_A<0>
	103A	VDD6		104A	VDD7		
30 15	MEM_A_A<10>	105A	A10/AP	106A	BA1	15 30	MEM_A_BS<1>
30 15	MEM_A_BS<0>	107A	BA0	108A	RAS*	15 30	MEM_A_RAS_L
30 15	MEM_A_WE_L	109A	WE*	110A	S0*	14 30	MEM_CS_L<0>
	111A	VDD8		112A	VDD9		
30 15	MEM_A_CAS_L	113A	CAS*	114A	ODT0	14 30	MEM_ODT<0>
30 14	MEM_CS_L<1>	115A	NC/S1*	116A	NC/A13	15 30	MEM_A_A<13>
	117A	VDD10		118A	VDD11		
30 14	MEM_ODT<1>	119A	NC/ODT1	120A	NC3		NC
	121A	VSS31		122A	VSS32		
15	MEM_A_DQ<35>	123A	DQ32	124A	DQ36	15	MEM_A_DQ<38>
15	MEM_A_DQ<39>	125A	DQ33	126A	DQ37	15	MEM_A_DQ<34>
	127A	VSS33		128A	VSS34		
15	MEM_A_DQS_N<4>	129A	DQS4*	130A	DM4	15	MEM_A_DM<4>
15	MEM_A_DQS_P<4>	131A	DQS4	132A	VSS35		
	133A	VSS36		134A	DQ38	15	MEM_A_DQ<32>
15	MEM_A_DQ<37>	135A	DQ34	136A	DQ39	15	MEM_A_DQ<36>
15	MEM_A_DQ<33>	137A	DQ35	138A	VSS37		
	139A	VSS38		140A	DQ44	15	MEM_A_DQ<57>
15	MEM_A_DQ<60>	141A	DQ40	142A	DQ45	15	MEM_A_DQ<63>
15	MEM_A_DQ<59>	143A	DQ41	144A	VSS39		
	145A	VSS40		146A	DQS5*	15	MEM_A_DQS_N<7>
15	MEM_A_DM<7>	147A	DM5	148A	DQS5	15	MEM_A_DQS_P<7>
	149A	VSS41		150A	VSS42		
15	MEM_A_DQ<58>	151A	DQ42	152A	DQ46	15	MEM_A_DQ<56>
15	MEM_A_DQ<61>	153A	DQ43	154A	DQ47	15	MEM_A_DQ<62>
	155A	VSS43		156A	VSS44		
15	MEM_A_DQ<43>	157A	DQ48	158A	DQ52	15	MEM_A_DQ<40>
15	MEM_A_DQ<45>	159A	DQ49	160A	DQ53	15	MEM_A_DQ<42>
	161A	VSS45		162A	VSS46		
	NC	163A	NC_TEST	164A	CK1	14	MEM_CLK_P<1>
	165A	VSS47		166A	CK1*	14	MEM_CLK_N<1>
15	MEM_A_DQS_N<5>	167A	DQS6*	168A	VSS48		
15	MEM_A_DQS_P<5>	169A	DQS6	170A	DM6	15	MEM_A_DM<5>
	171A	VSS49		172A	VSS50		
15	MEM_A_DQ<41>	173A	DQ50	174A	DQ54	15	MEM_A_DQ<47>
15	MEM_A_DQ<46>	175A	DQ51	176A	DQ55	15	MEM_A_DQ<44>
	177A	VSS51		178A	VSS52		
15	MEM_A_DQ<51>	179A	DQ56	180A	DQ60	15	MEM_A_DQ<54>
15	MEM_A_DQ<50>	181A	DQ57	182A	DQ61	15	MEM_A_DQ<55>
	183A	VSS53		184A	VSS54		
15	MEM_A_DM<6>	185A	DM7	186A	DQS7*	15	MEM_A_DQS_N<6>
	187A	VSS55		188A	DQS7	15	MEM_A_DQS_P<6>
15	MEM_A_DQ<53>	189A	DQ58	190A	VSS56		
15	MEM_A_DQ<48>	191A	DQ59	192A	DQ62	15	MEM_A_DQ<52>
63 29	=PPSPD_S0_MEM	193A	VSS57	194A	DQ63	15	MEM_A_DQ<49>
27	=I2C_SODIMMA_SDA	195A	SDA	196A	VSS58		
27	=I2C_SODIMMA_SCL	197A	SCL	198A	SA0		ADDR=0xA0(WR)/0xA1(RD)
		199A	VDDSPD	200A	SA1		

202 NC

204

516S0382

=PP1V8_S3_MEM 28 29 63

DDR2 Bypass Caps

(For return current)

63 29 28 =PP1V8_S3_MEM

C2808 10UF 20% 6.3V X5R 603

C2809 10UF 20% 6.3V X5R 603

C2810 0.1UF 20% 10V CERM 402

C2811 0.1UF 20% 10V CERM 402

C2812 0.1UF 20% 10V CERM 402

C2813 0.1UF 20% 10V CERM 402

C2814 0.1UF 20% 10V CERM 402

C2815 0.1UF 20% 10V CERM 402

C2816 0.1UF 20% 10V CERM 402

C2817 0.1UF 20% 10V CERM 402

C2818 0.1UF 20% 10V CERM 402

C2819 0.1UF 20% 10V CERM 402

C2820 0.1UF 20% 10V CERM 402

C2821 0.1UF 20% 10V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE	SHT 28 OF 104	
NONE		

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Upper" (thru-hole) slot

MEM_VREF

C2901 2.2uF 20% 6.3V CERM 603

C2900 0.1uF 20% 10V CERM 402

=PP1V8_S3_MEM

NC

CRITICAL
J2900
F-RT-TH1
DDR2-SODIMM-DUAL

	1B	VREF		2B	VSS0		
	3B	VSS1		4B	DQ4	MEM_B_DQ<9>	15
15 MEM_B_DQ<15>	5B	DQ0		6B	DQ5	MEM_B_DQ<11>	15
15 MEM_B_DQ<14>	7B	DQ1		8B	VSS2		
	9B	VSS4		10B	DM0	MEM_B_DM<1>	15
15 MEM_B_DQS_N<1>	11B	DQS0*		12B	VSS5		
15 MEM_B_DQS_P<1>	13B	DQS0		14B	DQ6	MEM_B_DQ<12>	15
	15B	VSS6		16B	DQ7	MEM_B_DQ<8>	15
15 MEM_B_DQ<10>	17B	DQ2		18B	VSS7		
15 MEM_B_DQ<13>	19B	DQ3		20B	DQ12	MEM_B_DQ<3>	15
	21B	VSS8		22B	DQ13	MEM_B_DQ<6>	15
15 MEM_B_DQ<7>	23B	DQ8		24B	VSS9		
15 MEM_B_DQ<2>	25B	DQ9		26B	DM1	MEM_B_DM<0>	15
	27B	VSS10		28B	VSS11		
15 MEM_B_DQS_N<0>	29B	DQS1*		30B	CK0	MEM_CLK_P<3>	14
15 MEM_B_DQS_P<0>	31B	DQS1		32B	CK0*	MEM_CLK_N<3>	14
	33B	VSS12		34B	VSS13		
15 MEM_B_DQ<1>	35B	DQ10		36B	DQ14	MEM_B_DQ<0>	15
15 MEM_B_DQ<4>	37B	DQ11		38B	DQ15	MEM_B_DQ<5>	15
	39B	VSS14	KEY	40B	VSS15		
	41B	VSS16		42B	VSS17		
15 MEM_B_DQ<21>	43B	DQ16		44B	DQ20	MEM_B_DQ<22>	15
15 MEM_B_DQ<19>	45B	DQ17		46B	DQ21	MEM_B_DQ<18>	15
	47B	VSS18		48B	VSS19		
15 MEM_B_DQS_N<2>	49B	DQS2*		50B	NC0	DIMM_OVERTEMP_L	28 48
15 MEM_B_DQS_P<2>	51B	DQS2		52B	DM2	MEM_B_DM<2>	15
	53B	VSS21		54B	VSS22		
15 MEM_B_DQ<20>	55B	DQ18		56B	DQ22	MEM_B_DQ<17>	15
15 MEM_B_DQ<23>	57B	DQ19		58B	DQ23	MEM_B_DQ<16>	15
	59B	VSS23		60B	VSS24		
15 MEM_B_DQ<29>	61B	DQ24		62B	DQ28	MEM_B_DQ<26>	15
15 MEM_B_DQ<24>	63B	DQ25		64B	DQ29	MEM_B_DQ<28>	15
	65B	VSS25		66B	VSS26		
15 MEM_B_DM<3>	67B	DM3		68B	DQS3*	MEM_B_DQS_N<3>	15
NC	69B	NC1		70B	DQS3	MEM_B_DQS_P<3>	15
	71B	VSS27		72B	VSS28		
15 MEM_B_DQ<27>	73B	DQ26		74B	DQ30	MEM_B_DQ<31>	15
15 MEM_B_DQ<25>	75B	DQ27		76B	DQ31	MEM_B_DQ<30>	15
	77B	VSS29		78B	VSS30		
30 14 MEM_CKE<2>	79B	CKE0		80B	NC/CKE1	MEM_CKE<3>	14 30
	81B	VDD0		82B	VDD1		
NC	83B	NC2		84B	NC/A15	MEM_B_A<15>	6
30 15 MEM_B_BS<2>	85B	BA2		86B	NC/A14	MEM_B_A<14>	6
	87B	VDD2		88B	VDD3		
30 15 MEM_B_A<12>	89B	A12		90B	A11	MEM_B_A<11>	15 30
30 15 MEM_B_A<9>	91B	A9		92B	A7	MEM_B_A<7>	15 30
30 15 MEM_B_A<8>	93B	A8		94B	A6	MEM_B_A<6>	15 30
	95B	VDD4		96B	VDD5		
30 15 MEM_B_A<5>	97B	A5		98B	A4	MEM_B_A<4>	15 30
30 15 MEM_B_A<3>	99B	A3		100B	A2	MEM_B_A<2>	15 30
30 15 MEM_B_A<1>	101B	A1		102B	A0	MEM_B_A<0>	15 30
	103B	VDD6		104B	VDD7		
30 15 MEM_B_A<10>	105B	A10/AP		106B	BA1	MEM_B_BS<1>	15 30
30 15 MEM_B_BS<0>	107B	BA0		108B	RAS*	MEM_B_RAS_L	15 30
30 15 MEM_B_WE_L	109B	WE*		110B	S0*	MEM_CS_L<2>	14 30
	111B	VDD8		112B	VDD9		
30 15 MEM_B_CAS_L	113B	CAS*		114B	ODT0	MEM_ODT<2>	14 30
30 14 MEM_CS_L<3>	115B	NC/S1*		116B	NC/A13	MEM_B_A<13>	15 30
	117B	VDD10		118B	VDD11		
30 14 MEM_ODT<3>	119B	NC/ODT1		120B	NC3	NC	
	121B	VSS31		122B	VSS32		
15 MEM_B_DQ<36>	123B	DQ32		124B	DQ36	MEM_B_DQ<32>	15
15 MEM_B_DQ<33>	125B	DQ33		126B	DQ37	MEM_B_DQ<37>	15
	127B	VSS33		128B	VSS34		
15 MEM_B_DQS_N<4>	129B	DQS4*		130B	DM4	MEM_B_DM<4>	15
15 MEM_B_DQS_P<4>	131B	DQS4		132B	VSS35		
	133B	VSS36		134B	DQ38	MEM_B_DQ<38>	15
15 MEM_B_DQ<34>	135B	DQ34		136B	DQ39	MEM_B_DQ<39>	15
15 MEM_B_DQ<35>	137B	DQ35		138B	VSS37		
	139B	VSS38		140B	DQ44	MEM_B_DQ<44>	15
15 MEM_B_DQ<40>	141B	DQ40		142B	DQ45	MEM_B_DQ<45>	15
15 MEM_B_DQ<41>	143B	DQ41		144B	VSS39		
	145B	VSS40		146B	DQS5*	MEM_B_DQS_N<5>	15
15 MEM_B_DM<5>	147B	DM5		148B	DQS5	MEM_B_DQS_P<5>	15
	149B	VSS41		150B	VSS42		
15 MEM_B_DQ<42>	151B	DQ42		152B	DQ46	MEM_B_DQ<46>	15
15 MEM_B_DQ<43>	153B	DQ43		154B	DQ47	MEM_B_DQ<47>	15
	155B	VSS43		156B	VSS44		
15 MEM_B_DQ<62>	157B	DQ48		158B	DQ52	MEM_B_DQ<58>	15
15 MEM_B_DQ<59>	159B	DQ49		160B	DQ53	MEM_B_DQ<63>	15
	161B	VSS45		162B	VSS46		
NC	163B	NC_TEST		164B	CK1	MEM_CLK_P<2>	14
	165B	VSS47		166B	CK1*	MEM_CLK_N<2>	14
15 MEM_B_DQS_N<7>	167B	DQS6*		168B	VSS48		
15 MEM_B_DQS_P<7>	169B	DQS6		170B	DM6	MEM_B_DM<7>	15
	171B	VSS49		172B	VSS50		
15 MEM_B_DQ<60>	173B	DQ50		174B	DQ54	MEM_B_DQ<56>	15
15 MEM_B_DQ<61>	175B	DQ51		176B	DQ55	MEM_B_DQ<57>	15
	177B	VSS51		178B	VSS52		
15 MEM_B_DQ<54>	179B	DQ56		180B	DQ60	MEM_B_DQ<55>	15
15 MEM_B_DQ<51>	181B	DQ57		182B	DQ61	MEM_B_DQ<50>	15
	183B	VSS53		184B	VSS54		
15 MEM_B_DM<6>	185B	DM7		186B	DQS7*	MEM_B_DQS_N<6>	15
	187B	VSS55		188B	DQS7	MEM_B_DQS_P<6>	15
15 MEM_B_DQ<52>	189B	DQ58		190B	VSS56		
15 MEM_B_DQ<49>	191B	DQ59		192B	DQ62	MEM_B_DQ<53>	15
63 29 28 =PPSPD_S0_MEM	193B	VSS57		194B	DQ63	MEM_B_DQ<48>	15
27 =I2C_SODIMMB_SDA	195B	SDA		196B	VSS58		
27 =I2C_SODIMMB_SCL	197B	SCL		198B	SA0		
	199B	VDDSPD		200B	SA1		

516-0140 202NC

=PPSPD_S0_MEM 28 29 63

R2900 10K 5% 1/10W MF-LF 402

Resistor prevents pwr-gnd short

SODIMM_A_SA1
ADDR=0xA4(WR)/0xA5(RD)

DDR2 Bypass Caps

(For return current)

=PP1V8_S3_MEM

C2908 10UF 20% 6.3V X5R 603

C2909 10UF 20% 6.3V X5R 603

C2910 0.1uF 20% 10V CERM 402

C2911 0.1uF 20% 10V CERM 402

C2912 0.1uF 20% 10V CERM 402

C2913 0.1uF 20% 10V CERM 402

C2914 0.1uF 20% 10V CERM 402

C2915 0.1uF 20% 10V CERM 402

C2916 0.1uF 20% 10V CERM 402

C2917 0.1uF 20% 10V CERM 402

C2918 0.1uF 20% 10V CERM 402

C2919 0.1uF 20% 10V CERM 402

C2920 0.1uF 20% 10V CERM 402

C2921 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

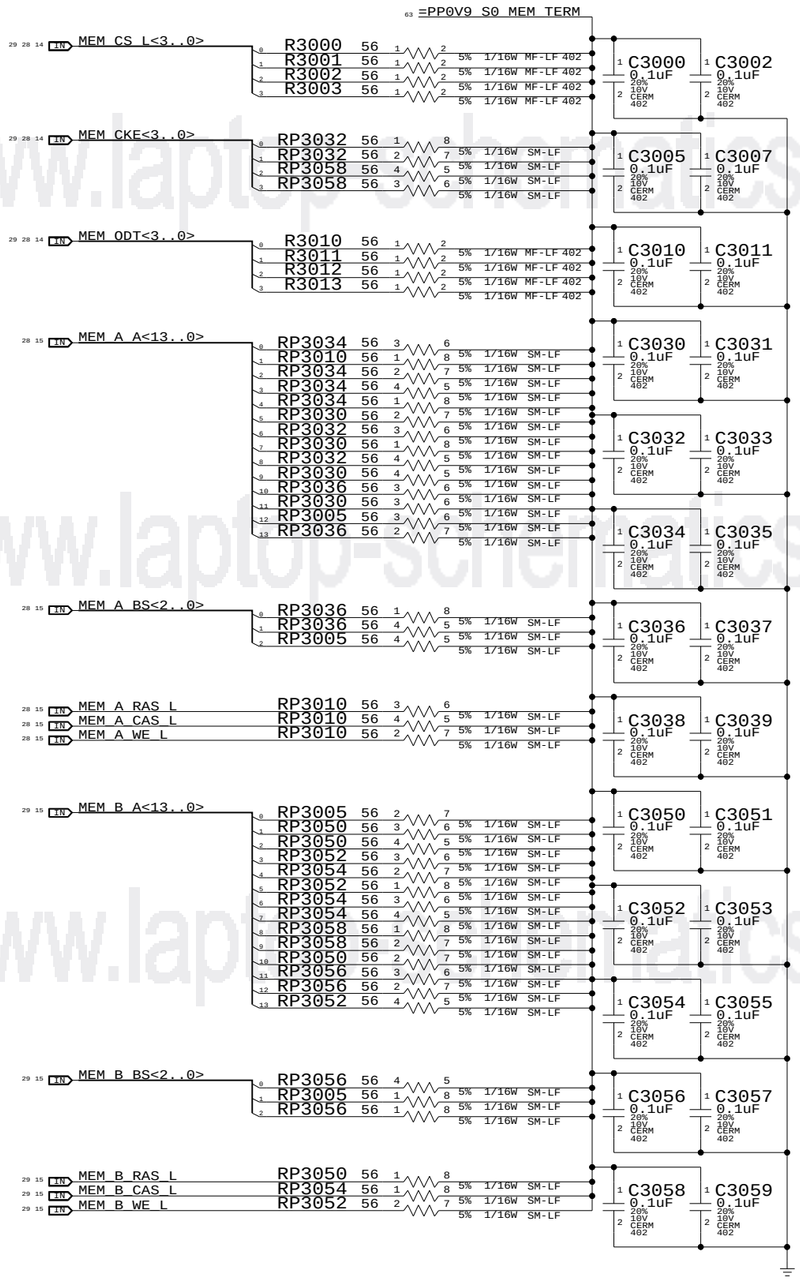
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 29 OF 104	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7155 | REV. A

SCALE NONE | SHT 30 OF 104

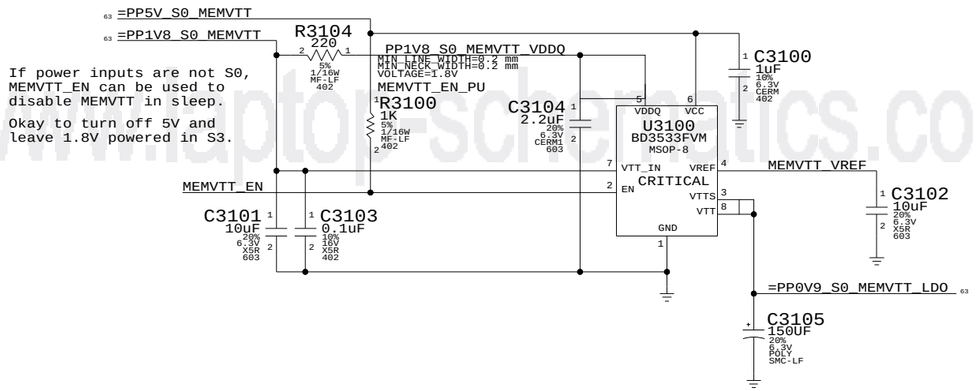
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



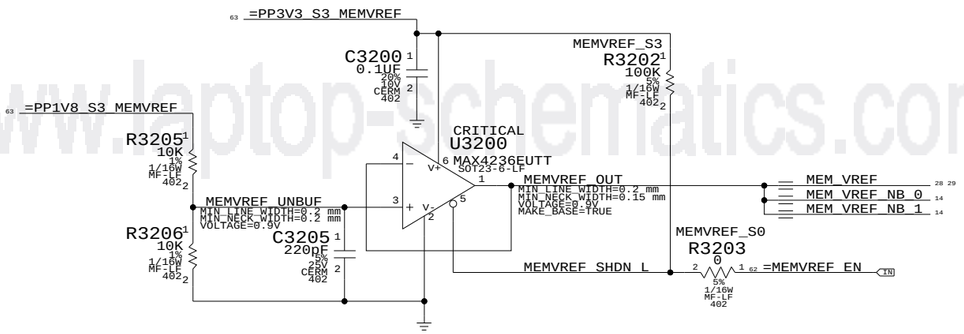
If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

Okay to turn off 5V and leave 1.8V powered in S3.

Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7155	A
	SCALE: NONE	SHT 31 OF 104	



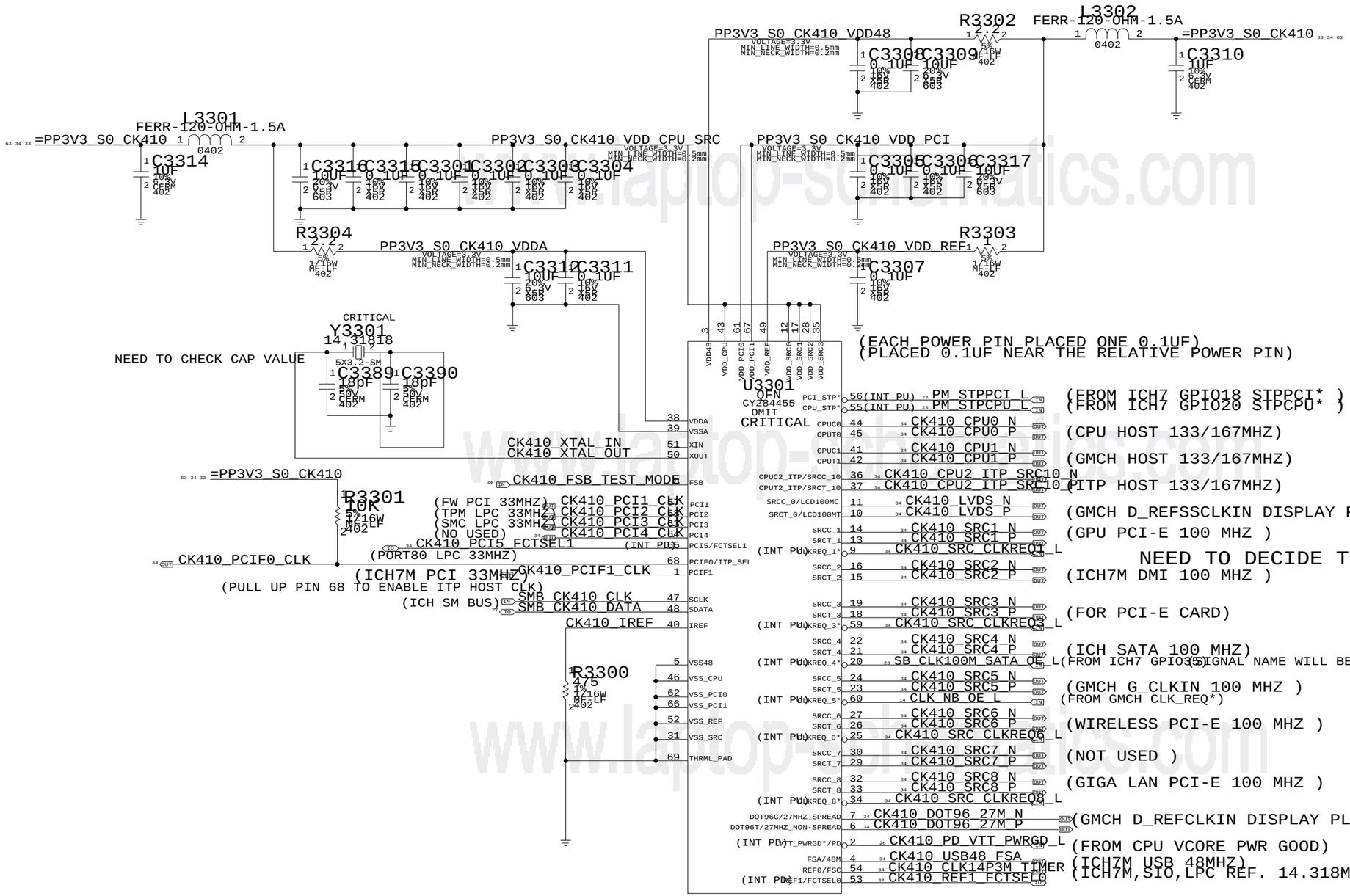
DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE	SHT	OF
NONE	32	104



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SS	T100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	SPREAD	SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF	LOW	BD	SRCT0	SRCC0

CLOCKS

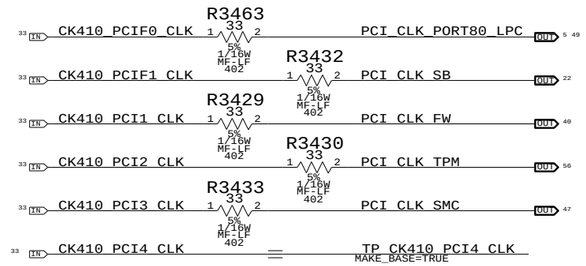
SYNC_MASTER=MBZ SYNC_DATE=10/12/2005

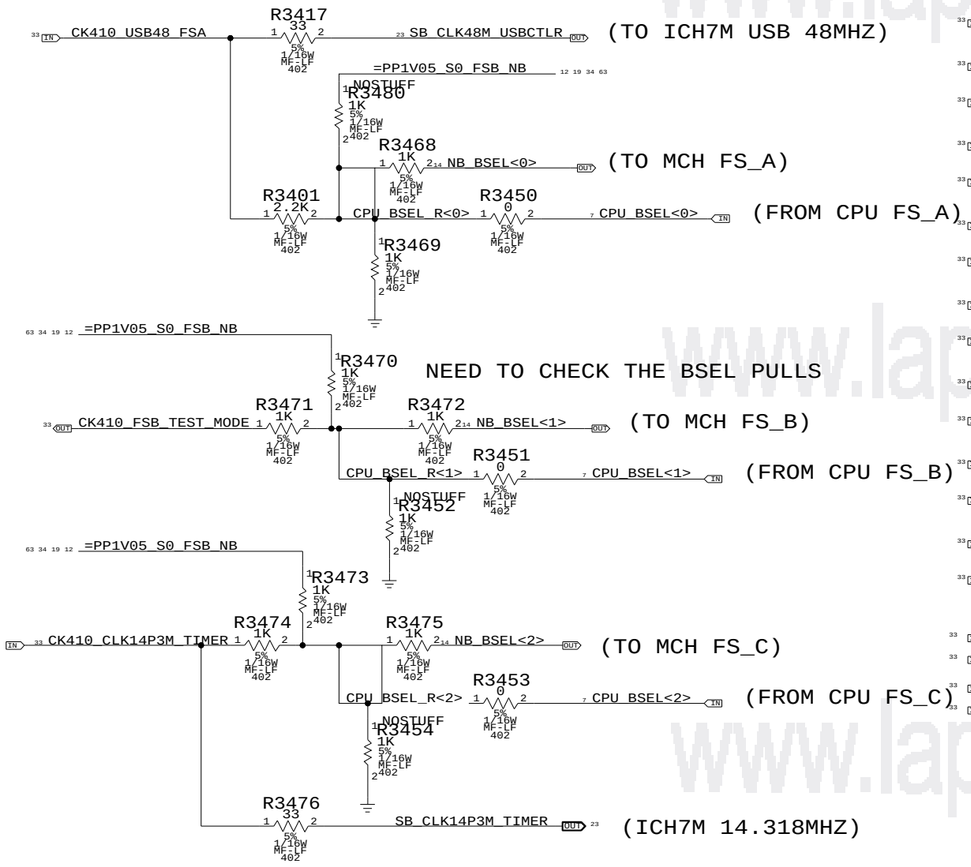
APPLE COMPUTER INC.

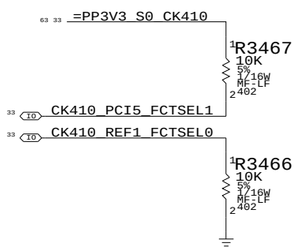
SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE: NONE

SHT 33 OF 104



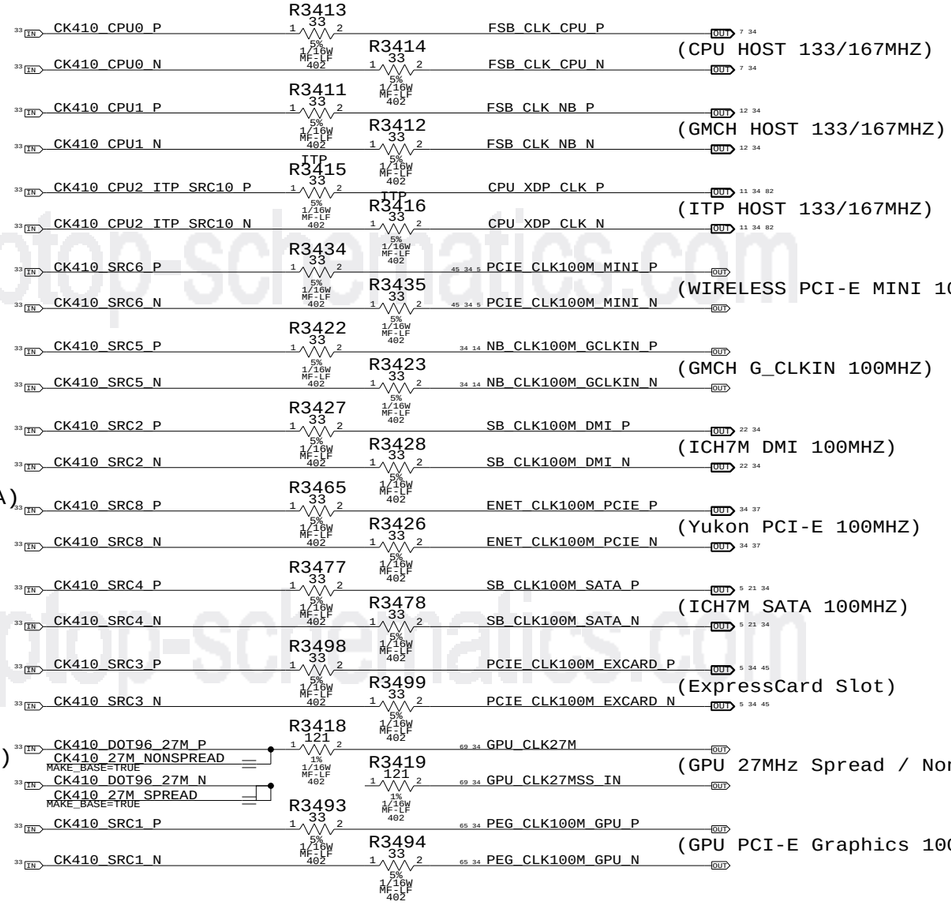


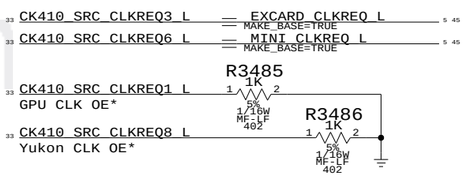


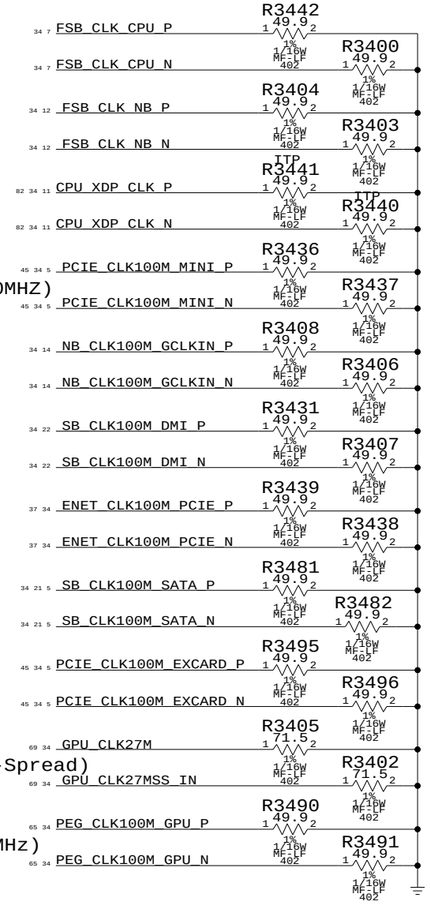
NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

FS_C	FS_B	FS_A	CPU
0	0	0	266M
# 0	0	1	133M
# 0	1	0	166M
0	1	1	200M
1	0	0	100M
1	0	1	333M
1	1	0	400M
1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED







Clock Termination

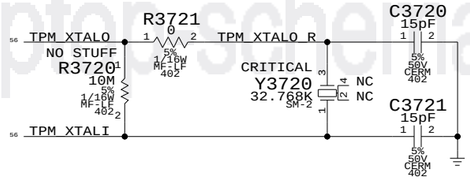
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

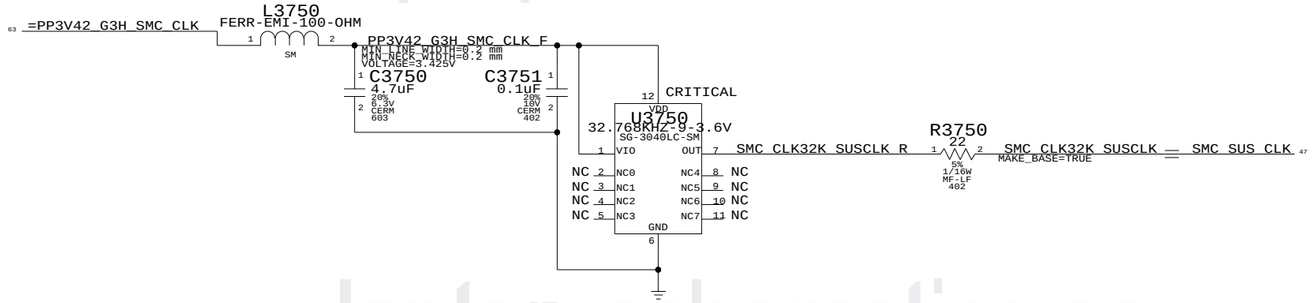
SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE	SHT	OF
NONE	34	104

TPM Crystal Circuit



SMC G3Hot Oscillator



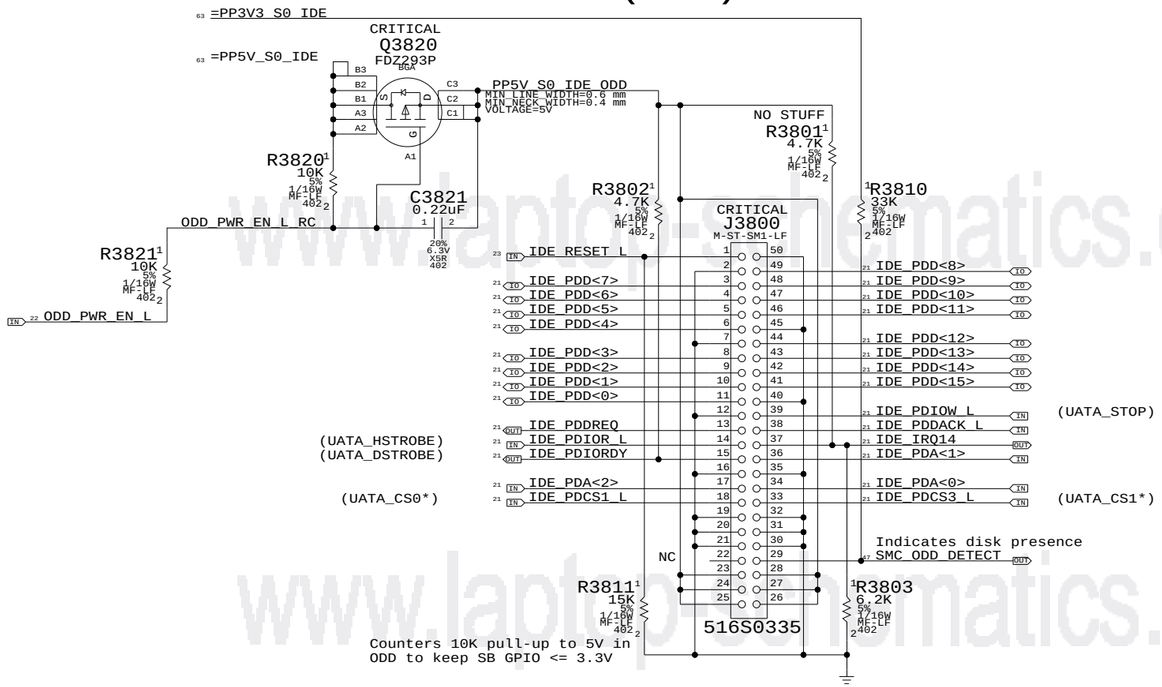
Mobile Clocking

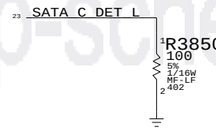
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

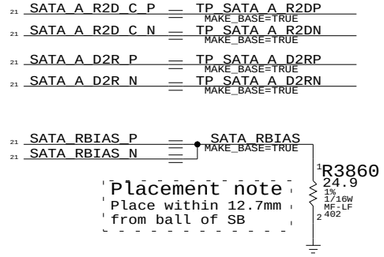
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 37 OF 104	

IDE (ODD) Connector







PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE	SHT	OF
NONE	38	104

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01 MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402 =PP2V5_S3_ENET

PLACE C4107 NEAR U4101 AVDD

=PP3V3_S3_ENET
=PP1V2_S3_ENET
=PP3V3_S3_ENET

R4101 4.7K 5% 1/16W MF-LF 402

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402
C4112 0.1UF 10% 16V X5R 402

PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
PCIE_A_D2R_P
PCIE_A_D2R_N
PCIE_A_R2D_P
PCIE_A_R2D_N
PCIE_A_R2D_C_P
PCIE_A_R2D_C_N

C4113 0.1UF 10% 16V X5R 402
PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

ENET_CLK100M_PCIE_P
ENET_CLK100M_PCIE_N
PCIE_WAKE_L
ENET_RST_L

ENET_LOM_DIS_L
=ENET_VMAIN_AVLBL
ENET_CTRL25
ENET_CTRL12
ENET_RSET

OPTIONAL EXTERNAL LDO
NO PULL-UP NEEDED

R4102 4.87K 1% 1/16W MF-LF 402

OMIT
CRITICAL
U4101
88E8053
QFN

ANALOG
PCI EXPRESS
LED
MEDIA
TEST
TWSI
SPI
MAIN CLK

ENET_VPD_CLK
ENET_VPD_DATA
ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1

ASF IS UNAVAILABLE ON 8053
INTERNAL PULL-UP

CRITICAL
ENET_XTALI
ENET_XTALO
Y4101 SM-3.2X2.5MM 25.0000M
C4150 27pF 5% 50V CERM 402
C4151 27pF 5% 50V CERM 402

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

R4106 49.9 1% 1/16W MF-LF 402 ENET_MDI0
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402 ENET_MDI1
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402 ENET_MDI2
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402 ENET_MDI3
R4117 49.9 1% 1/16W MF-LF 402

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

PLACE RESISTORS CLOSE TO U4101

=PP3V3_S3_ENET
R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402
ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1

=PP3V3_S3_ENET
PLACE C4140 NEAR U4102 VCC
C4140 0.1UF 10% 16V X5R 402

OMIT
CRITICAL
U4102 M24C08 SO8
VCC E2 NC1 NC0 WC* VSS SDA SCL

R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402

ENET_VPD_DATA
ENET_VPD_CLK

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

=PP1V2_S3_ENET
C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

=PP3V3_S3_ENET
C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=M42 SYNC_DATE=10/12/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE: NONE SHT 41 OF 104

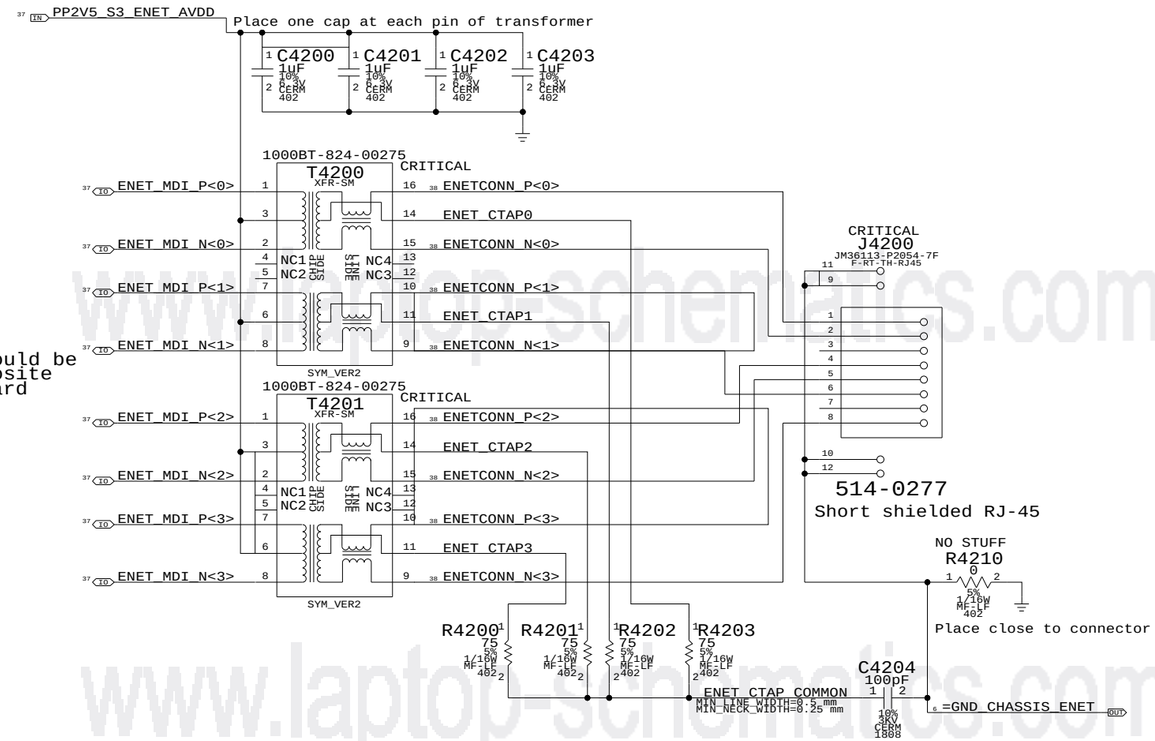
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0> 38
	ENETCONN	ENET_100D	ENETCONN_N<0> 38
	ENETCONN	ENET_100D	ENETCONN_P<1> 38
	ENETCONN	ENET_100D	ENETCONN_N<1> 38
	ENETCONN	ENET_100D	ENETCONN_P<2> 38
	ENETCONN	ENET_100D	ENETCONN_N<2> 38
	ENETCONN	ENET_100D	ENETCONN_P<3> 38
	ENETCONN	ENET_100D	ENETCONN_N<3> 38

Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Transformers should be mirrored on opposite sides of the board

Ethernet Connector

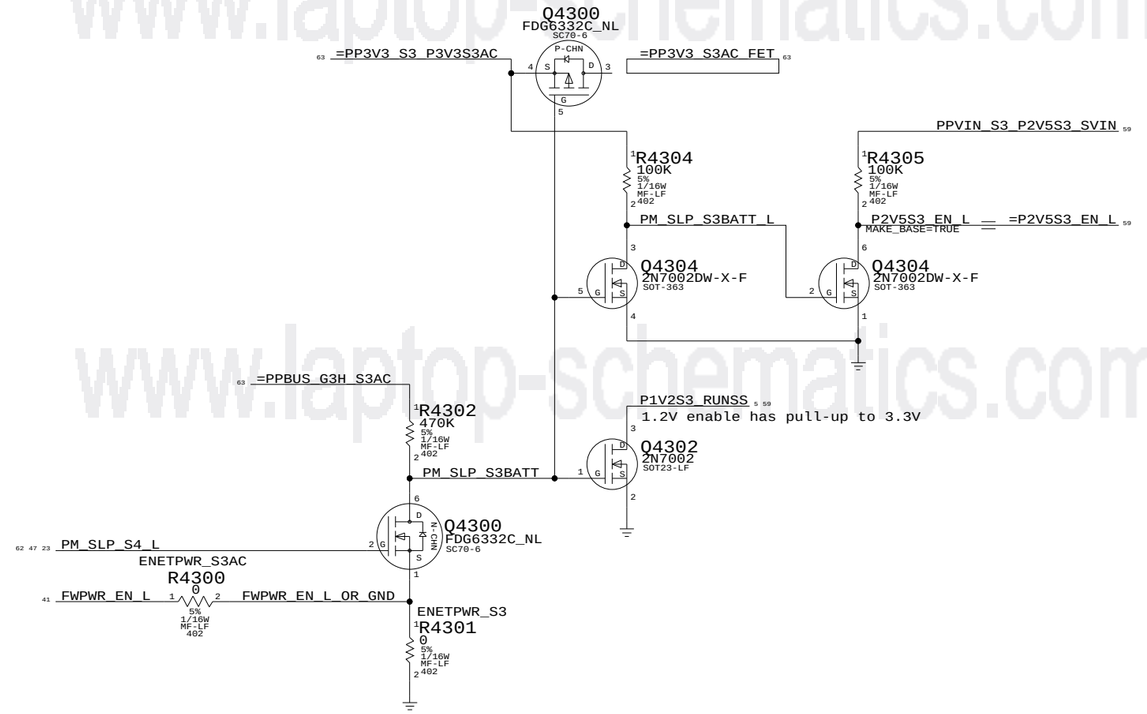
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 42 OF 104	

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	3.3V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE	SHT	OF
NONE	43	104

PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW23506 ADDED
6/21/2005 - CHANGED INT*_IO_INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_IO TO ADIO (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT IO_REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST, AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_FW DIFF_PAIR_NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

0.001A DURING SLEEP

=PP3V3_S3_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4424 ON VDD0

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 20% 16V X5R CERM 402
C4422 0.1UF 20% 16V X5R CERM 402
C4426 0.1UF 20% 16V X5R CERM 402
C4428 0.1UF 20% 16V X5R CERM 402
C4430 0.1UF 20% 16V X5R CERM 402
C4432 0.1UF 20% 16V X5R CERM 402

L4400
600-OHM-300MA
0402

PLACE ONE CAP PER TWO PINS STARTING WITH C4416 ON VDDA0

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 10% 16V X5R 402
C4429 0.1UF 10% 16V X5R 402
C4425 0.1UF 10% 16V X5R 402

PP3V3_S3_FW_AVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

GND_FW_VSSA
VOLTAGE=0V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

=PP3V3_S3_PCI

CONNECT TO VDD FOR 3.3V OPERATION

VDD0 G4, VDD1 N1, VDD2 N2, VDD3 K5, VDD4 K6, VDD5 K7, VDD6 L13, VDD7 H13, VDD9 A2
VDDA0 D10, VDDA1 A13, VDDA2 B13, VDDA3 A7, VDDA4 A8, VDDA5 D6

PCI_VIOS F10

PCI_AD<0> F10 PCI_AD0
PCI_AD<1> G10 PCI_AD1
PCI_AD<2> H10 PCI_AD2
PCI_AD<3> H12 PCI_AD3
PCI_AD<4> J13 PCI_AD4
PCI_AD<5> J12 PCI_AD5
PCI_AD<6> K13 PCI_AD6
PCI_AD<7> K10 PCI_AD7
PCI_AD<8> L12 PCI_AD8
PCI_AD<9> M13 PCI_AD9
PCI_AD<10> L11 PCI_AD10
PCI_AD<11> M12 PCI_AD11
PCI_AD<12> M11 PCI_AD12
PCI_AD<13> N12 PCI_AD13
PCI_AD<14> M10 PCI_AD14
PCI_AD<15> N11 PCI_AD15
PCI_AD<16> M4 PCI_AD16
PCI_AD<17> N5 PCI_AD17
PCI_AD<18> N4 PCI_AD18
PCI_AD<19> M3 PCI_AD19
PCI_AD<20> M2 PCI_AD20
PCI_AD<21> N3 PCI_AD21
PCI_AD<22> K4 PCI_AD22
PCI_AD<23> M1 PCI_AD23
PCI_AD<24> K2 PCI_AD24
PCI_AD<25> J4 PCI_AD25
PCI_AD<26> K1 PCI_AD26
PCI_AD<27> J2 PCI_AD27
PCI_AD<28> J1 PCI_AD28
PCI_AD<29> H2 PCI_AD29
PCI_AD<30> H4 PCI_AD30
PCI_AD<31> H1 PCI_AD31

PCI_C_BE_L<0> K12 PCI_CBE0*
PCI_C_BE_L<1> M9 PCI_CBE1*
PCI_C_BE_L<2> L3 PCI_CBE2*
PCI_C_BE_L<3> L1 PCI_CBE3*

PCI_PAR N10 PCI_PAR
PCI_FRAME_L N6 PCI_FRAME*
PCI_IRDY_L M6 PCI_IRDY*
PCI_TRDY_L N7 PCI_TRDY*
PCI_DEVSEL_L N8 PCI_DEVSEL*
PCI_STOP_L M7 PCI_STOP*
FW_PCI_IDSEL L2 PCI_IDSEL

R4431 22 5% 1/16W MF-LF 402

PCI_REQ3_L E2 PCI_REQ*
PCI_GNT3_L E1 PCI_GNT*
PCI_PERR_L M8 PCI_PERR*
PCI_SERR_L N9 PCI_SERR*

PCI_CLK_FW G2 PCI_CLK
PM_CLKRUN_L D1 CLKRUN*

R4432 100 5% 1/16W MF-LF 402
THIS IS FROM ICH-7M
PCI_RST_L
FW_PCI_RST_L F1 PCI_RST*

INT_PIRQD_L D2 PCI_INTA*
PCI_PME_FW_L F2 PCI_PME*

CRITICAL
U4400
FW32306
BGA
OMIT

VSS0 A1, VSS1 B2, VSS2 C3, VSS3 D4, VSS4 E4, VSS5 E5, VSS6 F4, VSS7 F6, VSS8 F7, VSS9 F8, VSS10 G1, VSS11 G6, VSS12 G7, VSS13 G8, VSS14 H6, VSS15 H7, VSS16 H8, VSS17 J5, VSS18 J9, VSS19 J10, VSS20 K8, VSS21 K9, VSS22 N13
VSSA0 E13, VSSA1 E9, VSSA2 D9, VSSA3 D7, VSSA4 D5

XW4400 SM

GND_FW_VSSA

197S0178 3.2MMX2.5MM CRITICAL
Y4403 SM-3.2X2.5MM 24.576MHZ

R4400 300 5% 1/16W MF-LF 402
FW_XO_R

C4411 22PF 5% 50V CERM 402
C4412 22PF 5% 50V CERM 402

NEED TO CHECK CRYSTAL LOAD CAPACITANCE

XI A5 FW_XI
XO B5 FW_XO

RESET* B4 FW_PWRON_RST_L

R4452 2.49K 1% 1/16W MF-LF 402
C4420 0.1UF 10% 16V X5R 402
R4420 510K 5% 1/16W MF-LF 402

SPEC RECOMMENDS 2.49K

R1 A6 FW_R1
R0 B7 FW_R0

TPBIAS0 B8 FW_A_TPBIAS
TPA0_P A9 FW_A_TPA_P
TPA0_N B9 FW_A_TPA_N
TPB0_P B10 FW_A_TPB_P
TPB0_N A10 FW_A_TPB_N
TPBIAS1 D8 FW_B_TPBIAS
TPA1_P A11 FW_B_TPA_P
TPA1_N B11 FW_B_TPA_N
TPB1_P B12 FW_B_TPB_P
TPB1_N A12 FW_B_TPB_N
TPBIAS2 C13 FW_C_TPBIAS
TPA2_P C11 FW_C_TPA_P
TPA2_N C12 FW_C_TPA_N
TPB2_P D13 FW_C_TPB_P
TPB2_N D12 FW_C_TPB_N

MODE_420 M5
MODE_A B6
MODE FOR EXTERNAL LINK

PC0 E12 FW_PC0
DUAL PORT DEVICES ARE POWER CLASS 4 (’100’)
SINGLE PORT DEVICES ARE POWER CLASS 0 (’000’)

PC1 F13
PC2 F12
CONTENDER G12
LOW = NOT BUS MANAGER
CARDBUSN B1
LOW = PCI OPERATION
MPCI_ACTN_323 E10

MANUFACTURING TEST PINS

TEST0 C2
TEST1 C1
TEST2 A4
SE A3
SM B3

FIREWIRE CONTROLLER

SYNC_MASTER=(M42) SYNC_DATE=08/29/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 44 OF 104	

Page Notes

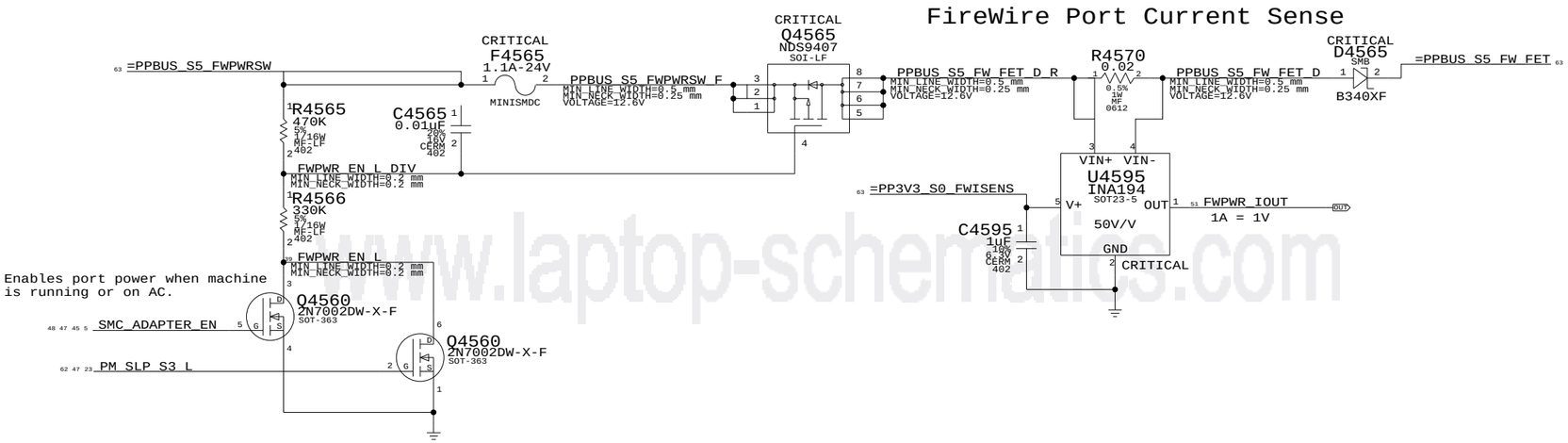
Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Port Power Switch

FireWire Port Current Sense



FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE: NONE

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY	FW	FW_110D	FW_PORT1_TPA_FL_P 42
	FW	FW_110D	FW_PORT1_TPA_FL_N 42
PHY	FW	FW_110D	FW_PORT1_TPB_FL_P 42
PAGE	FW	FW_110D	FW_PORT1_TPB_FL_N 42

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

Place close to FireWire PHY

40 FW_A_TPBIAS
C4650 0.33uF 10% 6.3V CERM-X5R 402
R4650 56.2 1% 1/16W MF-LF 402
R4651 56.2 1% 1/16W MF-LF 402
40 FW_A_TPA_P — FW_PORT1_TPA_P 42 (MAKE_BASE=TRUE)
40 FW_A_TPA_N — FW_PORT1_TPA_N 42 (MAKE_BASE=TRUE)
40 FW_A_TPB_P — FW_PORT1_TPB_P 42 (MAKE_BASE=TRUE)
40 FW_A_TPB_N — FW_PORT1_TPB_N 42 (MAKE_BASE=TRUE)
R4652 56.2 1% 1/16W MF-LF 402
R4653 56.2 1% 1/16W MF-LF 402
FW_TPA0_C
C4654 220pF 5% 25V CERM 402
R4654 4.99K 1% 1/16W MF-LF 402

2nd TPA/TPB pair unused

40 FW_B_TPBIAS — NC_FW_B_TPBIAS (MAKE_BASE=TRUE, NO_TEST=YES)
40 FW_B_TPA_P — NC_FW_B_TPAP (MAKE_BASE=TRUE, NO_TEST=YES)
40 FW_B_TPA_N — NC_FW_B_TPAN (MAKE_BASE=TRUE, NO_TEST=YES)
40 FW_B_TPB_P — NC_FW_B_TPBP (MAKE_BASE=TRUE, NO_TEST=YES)
40 FW_B_TPB_N — NC_FW_B_TPBN (MAKE_BASE=TRUE, NO_TEST=YES)

3rd TPA/TPB pair unused

40 FW_C_TPBIAS — NC_FW_C_TPBIAS (MAKE_BASE=TRUE, NO_TEST=YES)
40 FW_C_TPA_P — NC_FW_C_TPAP (MAKE_BASE=TRUE, NO_TEST=YES)
40 FW_C_TPA_N — NC_FW_C_TPAN (MAKE_BASE=TRUE, NO_TEST=YES)
40 FW_C_TPB_P — NC_FW_C_TPBP (MAKE_BASE=TRUE, NO_TEST=YES)
40 FW_C_TPB_N — NC_FW_C_TPBN (MAKE_BASE=TRUE, NO_TEST=YES)

FW Power Class Strap

Single-port system sets PC=0

FW_PC0 — 40

Late-VG Protection Power

63 =PP3V3_S5_FWLATEVG
R4690 330 5% 1/16W MF-LF 402
PP3V3_S5_FWLATEVG_R (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=3.3V)
L4690 400-OHM-EMI SM-1
PP3V3_S5_FWLATEVG_R_F 42 (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=3.3V)
C4691 0.1uF 10% 10V CERM 402
C4692 0.001uF 10% 50V CERM 402
D4690 CRITICAL MMBZ5227B SOT23

Cable Power

63 =PPFW_PORT1
L4620 FERR-250-OHM SM
PPFW_PORT1_VP (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=33V)
C4624 0.001uF 20% 50V CERM 402

"Snapback" & "Late VG" Protection

42 PP3V3_S5_FWLATEVG_R_F
DP4620 BAV99DW-X-F SOT-363
C4620 0.001uF 20% 50V CERM 402
C4621 0.001uF 20% 50V CERM 402
42 FW_PORT1_TPA_P
42 FW_PORT1_TPA_N
42 FW_PORT1_TPB_P
42 FW_PORT1_TPB_N
DP4621 BAV99DW-X-F SOT-363
C4622 0.001uF 20% 50V CERM 402
C4623 0.001uF 20% 50V CERM 402
SM1 260-OHM-330MA FL4620 CRITICAL
SM1 260-OHM-330MA FL4621 CRITICAL
42 FW_PORT1_TPA_FL_P
42 FW_PORT1_TPA_FL_N
42 FW_PORT1_TPB_FL_P
42 FW_PORT1_TPB_FL_N
(PPFW_PORT1_VP)
(GND_FW_PORT1_VG)
C4625 0.01uF 10% 16V CERM 603
C4626 0.01uF 20% 16V CERM 402

PORT 1 1394A

CRITICAL
J4620 1394A F-RT-TH-LF
6 TPO (TPA+)
5 TPO# (TPA-)
4 TPI (TPB+)
3 TPI# (TPB-)
1 VP
2 VGND
7 8 9 10
514-0255
=GND_CHASSIS_FW_PORT1 6

R4699 0 5% 1/16W MF-LF 402
=GND_CHASSIS_FW_EMI 6

FireWire Ports

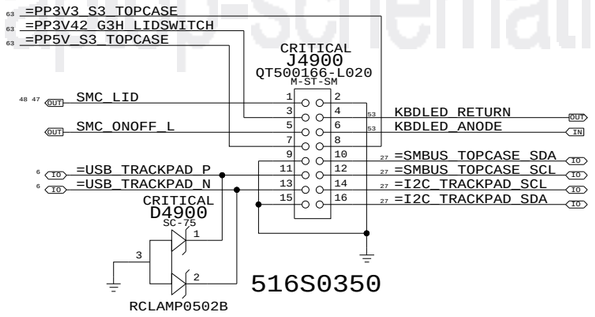
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

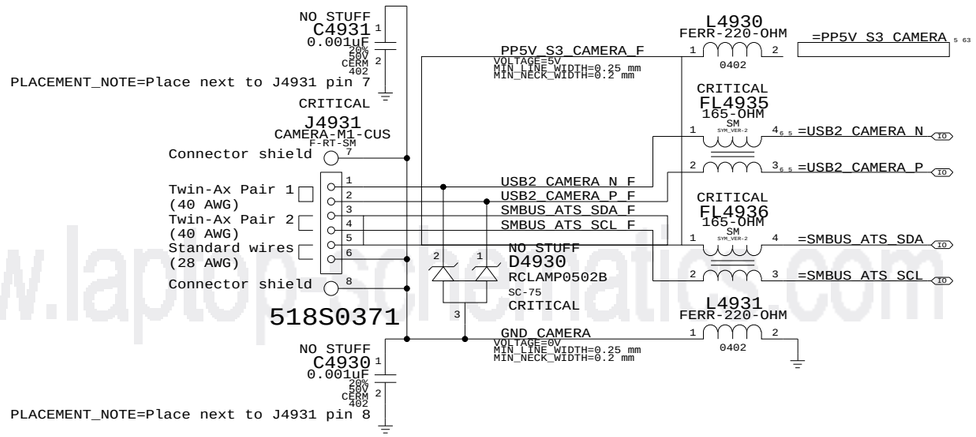
SIZE D | DRAWING NUMBER 051-7155 | REV. A

SCALE NONE | SHT 46 OF 104

Top-Case Connector



Camera Connector



Internal USB Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

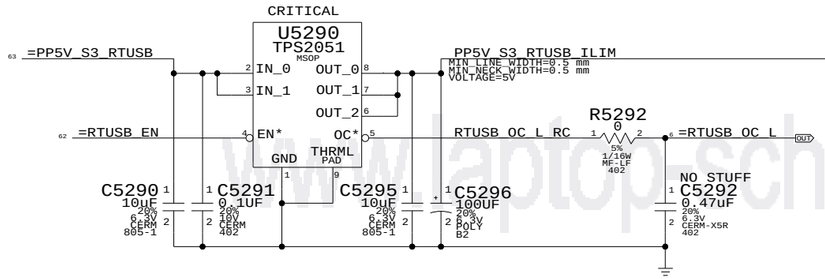
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

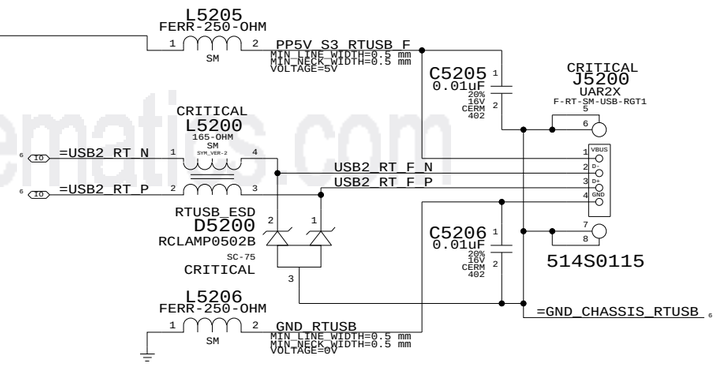
SCALE: NONE

SHT 49 OF 104

Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

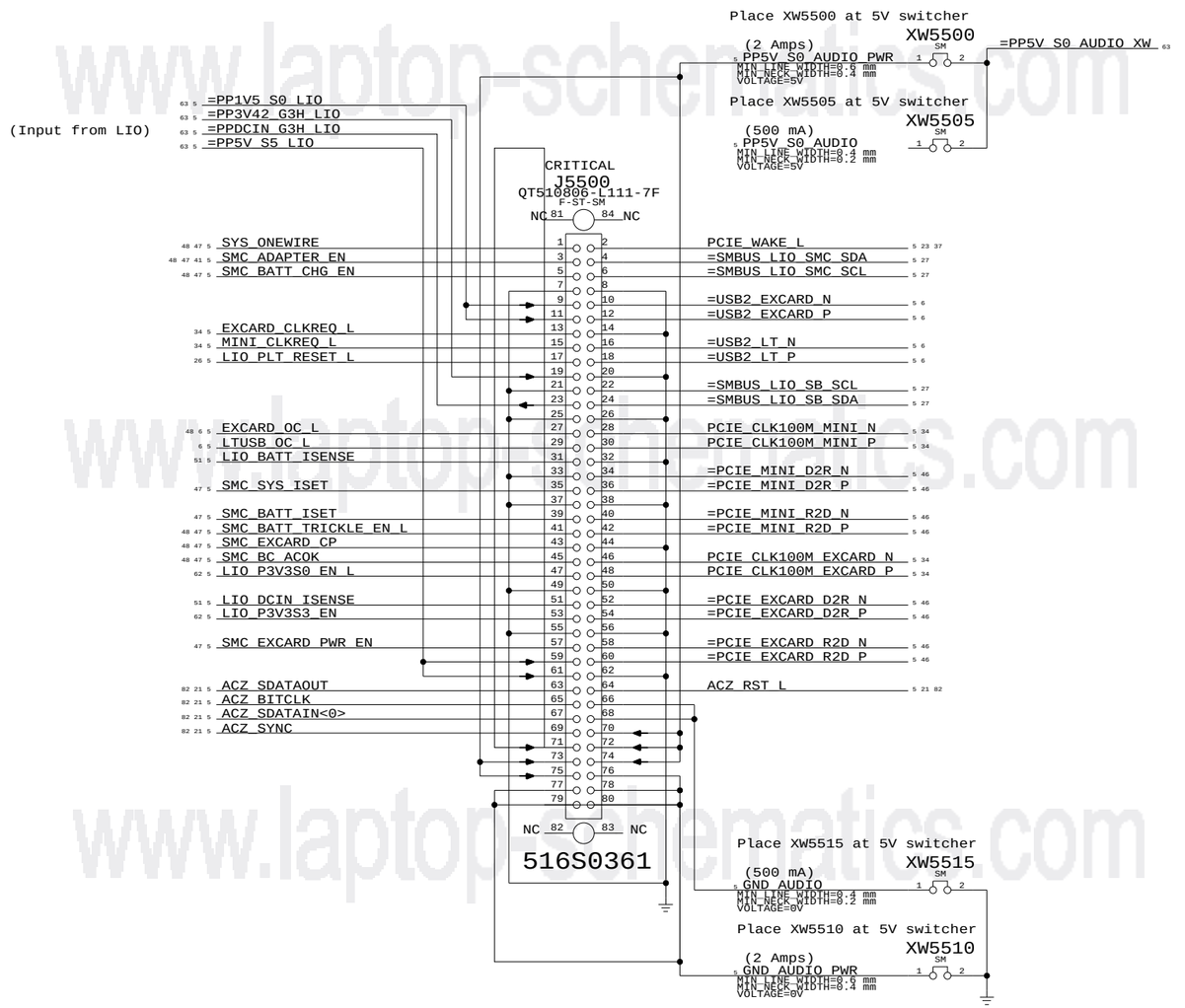
External USB Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 52 OF 104	

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 55 OF 104	

PCI-E x1 Port "A" = Ethernet (Yukon)

PCI-E x1 Port "B" = PCI-E Mini Card

C5710 0.1uF 10% 16V X5R 402

C5711 0.1uF 10% 16V X5R 402 Place caps close to SB

=PCIE_MINI_R2D_P	PCIE_MINI_R2D_C_P	MAKE_BASE=TRUE	PCIE_B_R2D_C_P	22
=PCIE_MINI_R2D_N	PCIE_MINI_R2D_C_N	MAKE_BASE=TRUE	PCIE_B_R2D_C_N	22
=PCIE_MINI_D2R_P	PCIE_MINI_D2R_P	MAKE_BASE=TRUE	PCIE_B_D2R_P	22
=PCIE_MINI_D2R_N	PCIE_MINI_D2R_N	MAKE_BASE=TRUE	PCIE_B_D2R_N	22

PCI-E x1 Port "C" = ExpressCard

C5720 0.1uF 10% 16V X5R 402

C5721 0.1uF 10% 16V X5R 402 Place caps close to SB

=PCIE_EXCARD_R2D_P	PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE	PCIE_C_R2D_C_P	22
=PCIE_EXCARD_R2D_N	PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE	PCIE_C_R2D_C_N	22
=PCIE_EXCARD_D2R_P	PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE	PCIE_C_D2R_P	22
=PCIE_EXCARD_D2R_N	PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE	PCIE_C_D2R_N	22

PCI-E x1 Port "D" = Unused

TP_PCIE_D_R2DP	MAKE_BASE=TRUE	PCIE_D_R2D_C_P	22
TP_PCIE_D_R2DN	MAKE_BASE=TRUE	PCIE_D_R2D_C_N	22
TP_PCIE_D_D2RP	MAKE_BASE=TRUE	PCIE_D_D2R_P	22
TP_PCIE_D_D2RN	MAKE_BASE=TRUE	PCIE_D_D2R_N	22

PCI-E x1 Port "E" = Unused

TP_PCIE_E_R2DP	MAKE_BASE=TRUE	PCIE_E_R2D_C_P	22
TP_PCIE_E_R2DN	MAKE_BASE=TRUE	PCIE_E_R2D_C_N	22
TP_PCIE_E_D2RP	MAKE_BASE=TRUE	PCIE_E_D2R_P	22
TP_PCIE_E_D2RN	MAKE_BASE=TRUE	PCIE_E_D2R_N	22

PCI-E x1 Port "F" = Unused

TP_PCIE_F_R2DP	MAKE_BASE=TRUE	PCIE_F_R2D_C_P	22
TP_PCIE_F_R2DN	MAKE_BASE=TRUE	PCIE_F_R2D_C_N	22
TP_PCIE_F_D2RP	MAKE_BASE=TRUE	PCIE_F_D2R_P	22
TP_PCIE_F_D2RN	MAKE_BASE=TRUE	PCIE_F_D2R_N	22

PCI-E Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 57 OF 104	

UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	62	SMC_PM_G2_EN	
SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	48 45 41 5	SMC_ADAPTER_EN	
ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	22	SPI_ARB	
RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	52 22	SPI_SCLK	
SMC_SB_NMI	B15	P14	P64/KIN4*	K13	52 22	SPI_SI	
PM_RSMRST_L	C14	P15	P65/KIN5*	K14	52 22	SPI_SO	
IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	48	SMC_PROCHOT_3_3_L	
PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	48	SMC_CPU_INIT_3_3_L	
SMC_P20	D13	P20	P70/AN0	N12	51	SMC_CPU_ISENSE	
SMC_P21	D14	P21	P71/AN1	R13	51	SMC_CPU_VSENSE	
SMC_P22	D15	P22	P72/AN2	P13	51	SMC_GPU_ISENSE	
SMC_P23	E12	P23	P73/AN3	R14	51	SMC_GPU_VSENSE	
SMC_BATT_TRICKLE_EN	E14	P24	P74/AN4	P14	51	SMC_DCIN_ISENSE	
SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	51	SMC_PBUS_VSENSE	
SMC_P26	E13	P26	P76/AN6	N13	51	SMC_BATT_ISENSE	
SMC_P27	F14	P27	P77/AN7	P15	51	SMC_FWIRE_ISENSE	
LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	23	SMC_WAKE_SCI_L	
LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	48	SMC_TPM_GPIO	
LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	56 49 40 23 5	PM_CLKRUN_L	
LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	56 49 48 23 5	PM_SUS_STAT_L	
LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	48	SC_TX_L	
SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	48	SC_RX_L	
PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	27	SMB_BSB_CLK	
INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	51 48 43 5	SMC_ONOFF_L	
SMC_XDP_TMS	A5	P40/TMI0	P91/IRQ1*	J2	48 45 5	SMC_BC_ACOK	
SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	64 48 5	SMC_BS_ALRT_L	
SMB_BSB_DATA	D5	P42/SDA1	P93/IRQ12*	J3	62 41 23	PM_SLP_S3_L	
SMC_TPM_PP	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	62 39 23	PM_SLP_S4_L	
SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	48 23	PM_SLP_S5_L	
SMC_XDP_TCK	C2	P45	P96/EXCL	H1	35	SMC_SUS_CLK	
SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	27	SMB_0_S0_DATA	
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1					
SMC_TX_L	G1	P50					
SMC_RX_L	G4	P51					
SMB_0_S0_CLK	F2	P52/SCL0					

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3	48	SMC_CASE_OPEN	
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	49 48 5	SMC_TCK	
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	49 48 5	SMC_TDI	
SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	49 48 5	SMC_TDO	
PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	49 48 5	SMC_TMS	
PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7		SMC_PF0	48
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6		SMC_PF1	48
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	48 43	SMC_LID	
SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	48	SMC_CPU_RESET_3_3_L	
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	45 5	SMC_BATT_ISET	
SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	48	SMC_BATT_VSET	
ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	45 5	SMC_SYS_ISET	
SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	48	SMC_SYS_VSET	
SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	52 22	SPI_CE_L	
SMC_EXCARD_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	48	SMC_XDP_TCK_3_3	
SMC_XDP_TDO_3_3	D11	PB7	PG2/EXIRQ10*/SDA2	N9	27	SMB_BSA_DATA	
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	27	SMB_BSA_CLK	
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	27	SMB_A_S3_DATA	
SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	27	SMB_A_S3_CLK	
SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	27	SMB_B_S0_DATA	
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	27	SMB_B_S0_CLK	
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	48	SMC_PROCHOT	
SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	48	SMC_THRMTRIP	
SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	48	SMC_FWE	
SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	76 6 5	ALS_GAIN	
SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	48 23	SMS_INT_L	
SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	55	SMS_ONOFF_L	
SMC_ANALOG_ID	N11	PD3/AN11					
SMC_NB_ISENSE	P10	PD4/AN12					
SMC_MEM_ISENSE	R10	PD5/AN13					
ALS_LEFT	N10	PD6/AN14					
ALS_RIGHT	M10	PD7/AN15					

OMIT
U5800
SMC_H8S2116
BGA
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G3	NC0	NC12	E15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

63 48 47 =PP3V3_S5_SMC

C5802 22UF 20% 6.3V CERM 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL

C5807 0.47UF 20% 6.3V CERM-X5R 402

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

VCL IS INTERNAL RAIL

63 48 47 =PP3V3_S5_SMC

R5899 4.7 5% 1/10W MF 402

PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.25
MIN_NECK_WIDTH=0.28

C5820 0.1UF 20% 10V CERM 402

PP3V3_AVREF_SMC 48

63 48 47 =PP3V3_S5_SMC

R5809 10K 5% 1/16W MF 402
R5801 10K 5% 1/16W MF 402

53 51 48 47 GND_SMC_AVSS

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

AVCC	N15	VCL	M14
AVCC	N15	VCL	M15
VCC	P2	VCL	F1
VCC	P1	A1	
VCC	J15		
AVREF	M14		
AVREF	M15		

49 48 5 SMC_RST_L — RES* E3
48 SMC_XTAL — XTAL A2
48 SMC_EXTAL — EXTAL B2

MD1 E2 — SMC_MD1 5 49
MD2 K1 — KBC_MDE
NMI F4 — SMC_NMI
ETRST* L1 — SMC_TRST_L
AVSS P12
AVSS R12

VSS: D1 P4 R4 F12 F13 B13 A13 A4 B4 D2

R5898 10K 5% 1/16W MF 402
R5803 10K 5% 1/16W MF 402
R5802 10K 5% 1/16W MF 402
NOSTUFF

XW5800 SM 1 2

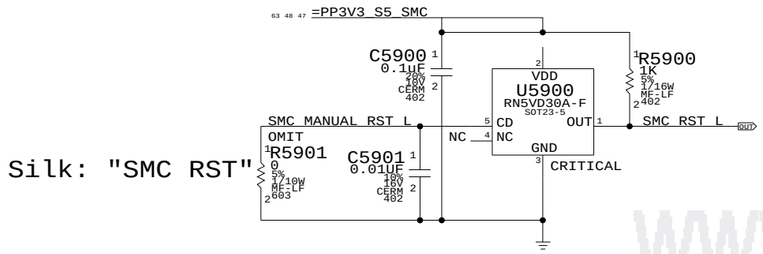
GND_SMC_AVSS 47 48 51 53

SMC

APPLE COMPUTER INC.

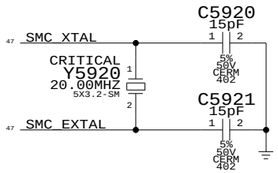
SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 58 OF 104	

SMC Reset Button / Brownout Detect

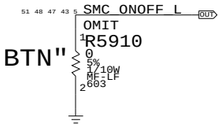


Silk: "SMC RST"

SMC Crystal Circuit

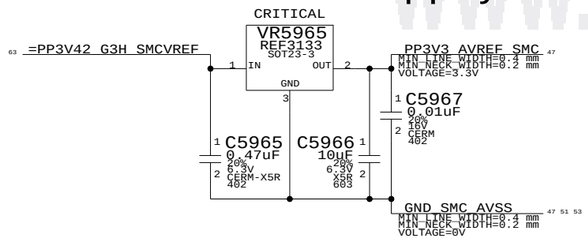


Debug Power Button

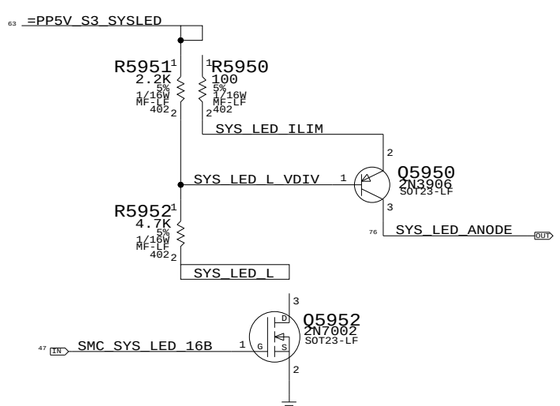


Silk: "PWR BTN"

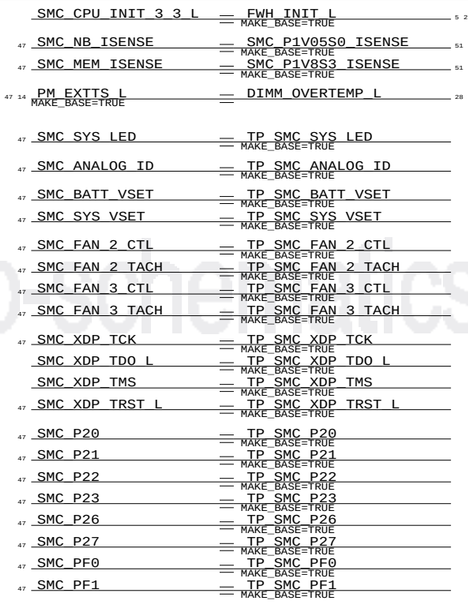
SMC AVREF Supply



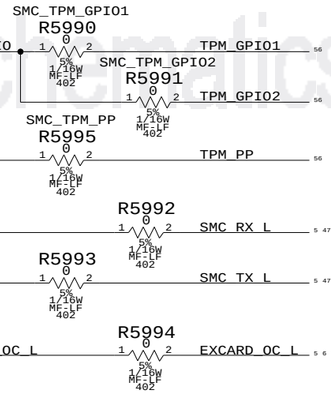
System (Sleep) LED Circuit



SMC_CPU_INIT_3_3_L

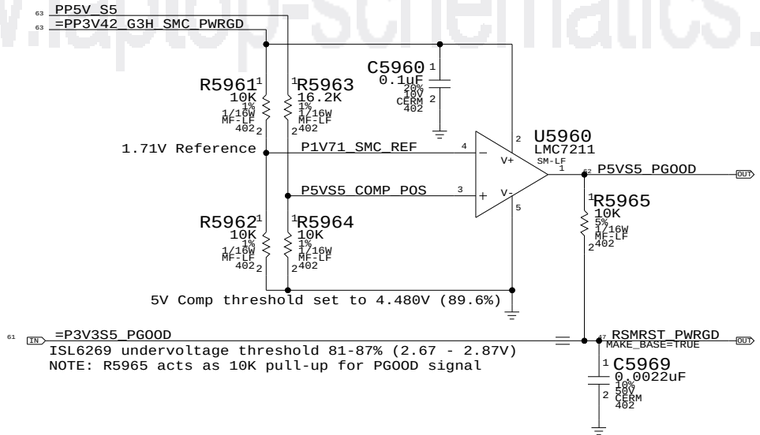


SMC_TPM_GPIO

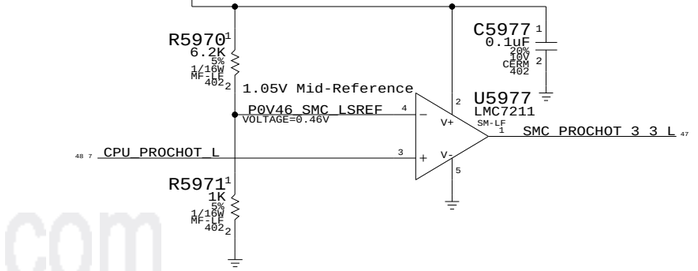


SMC PWRGD Circuit

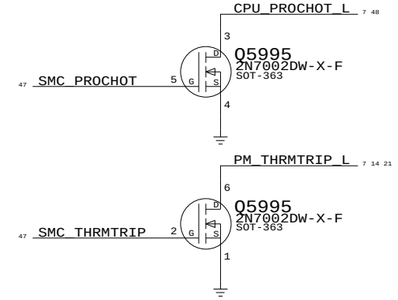
Reports when 5V S5 and 3.3V S5 are in regulation



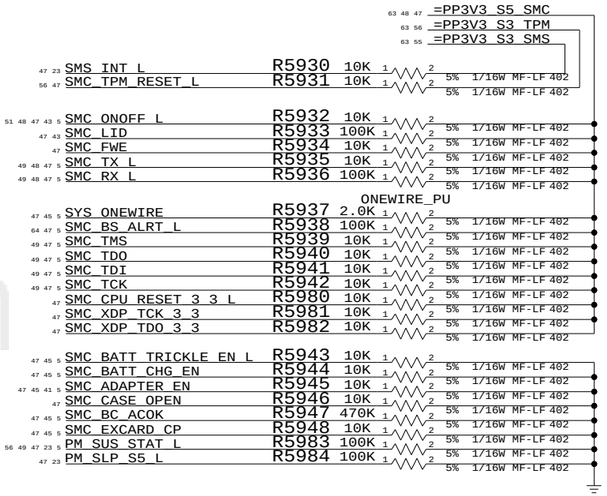
SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting



SMC_PM_G2_EN

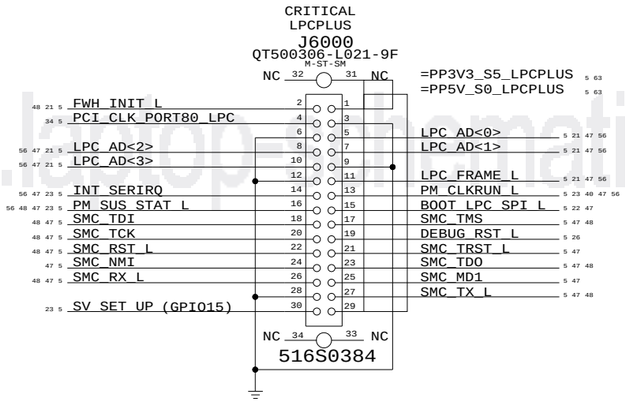


SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 59 OF 104	



LPC+ Debug Connector

SYNC_MASTER=M42 SYNC_DATE=07/20/2005

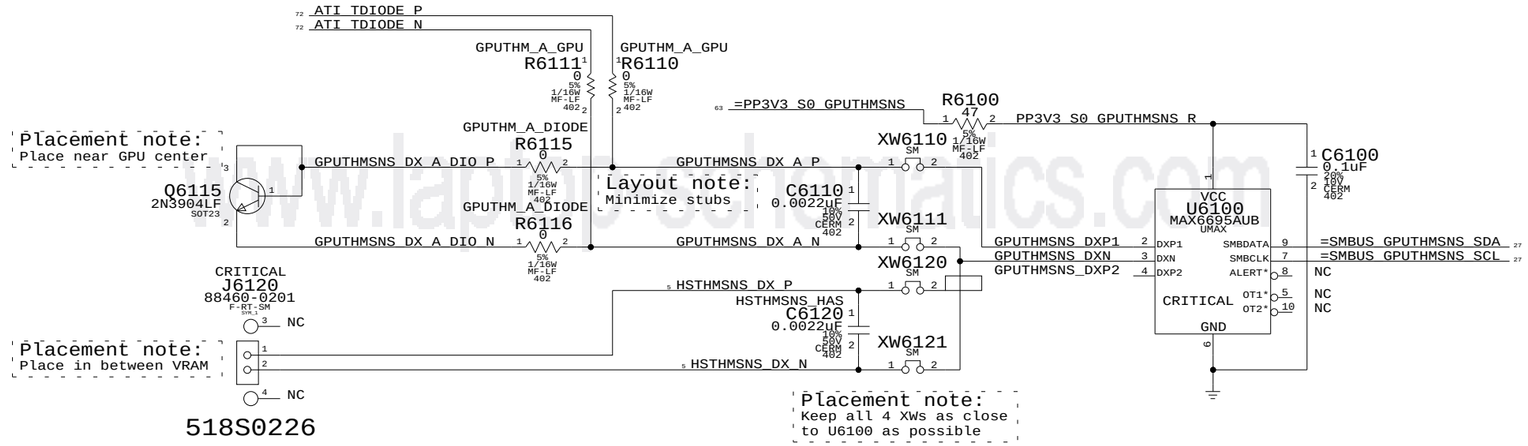
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE: NONE

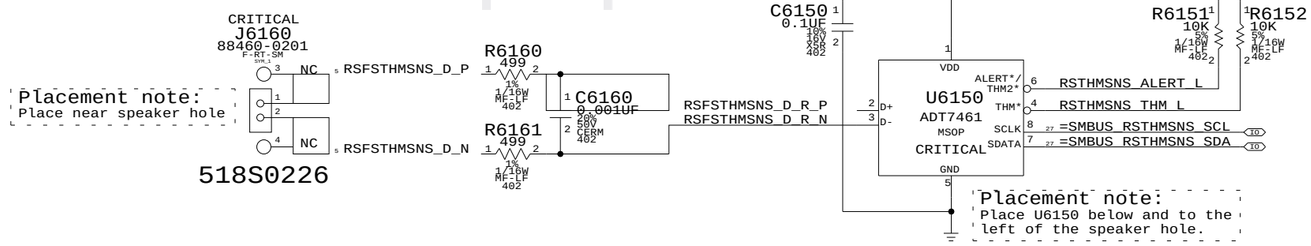
SHT 60 OF 104

GPU / Heat Pipe Thermal Sensor

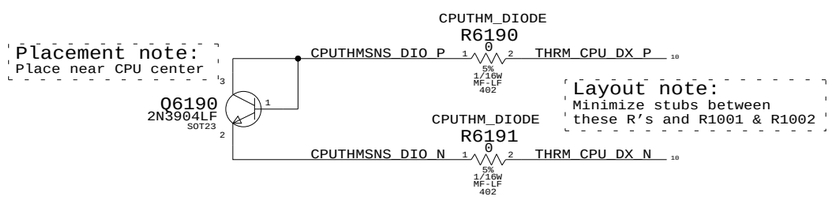


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

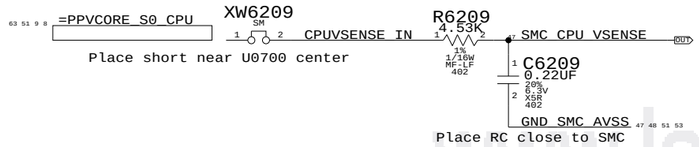
Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

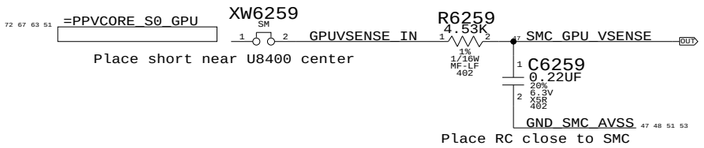
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 61 OF 104	

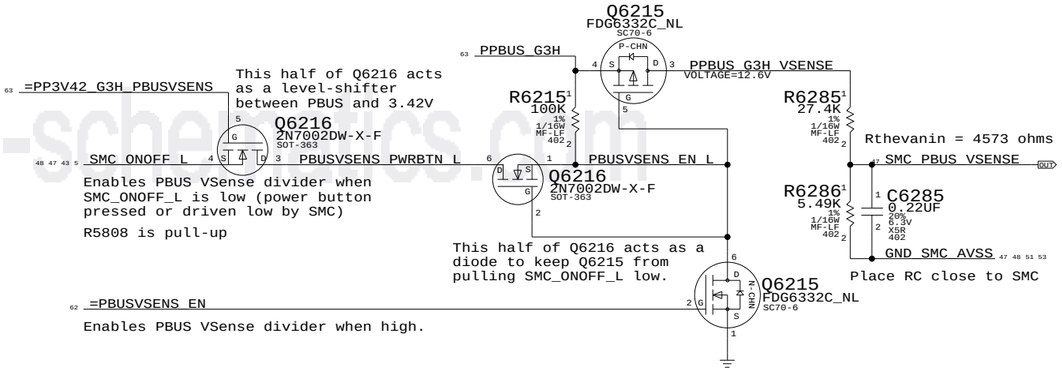
CPU Voltage Sense / Filter



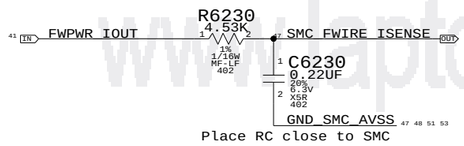
GPU Voltage Sense / Filter



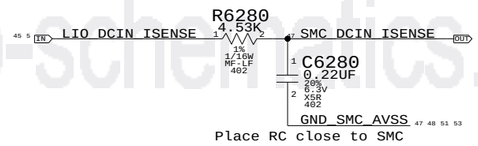
PBUS Voltage Sense Enable & Filter



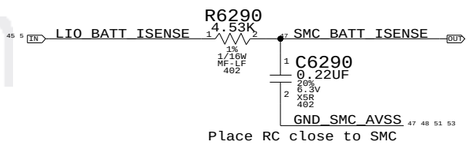
FireWire Current Sense Filter



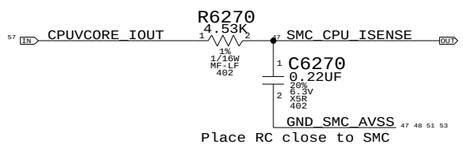
DCIN Current Sense Filter



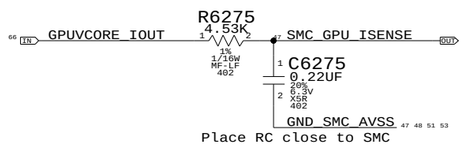
Battery Current Sense Filter



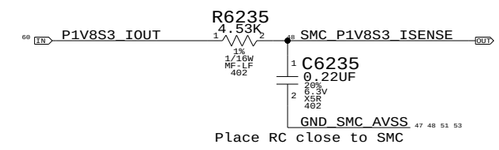
CPU Current Sense Filter



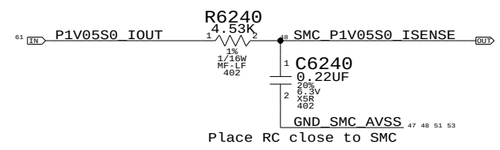
GPU Current Sense Filter



1.8V S3 (Memory) Current Sense Filter

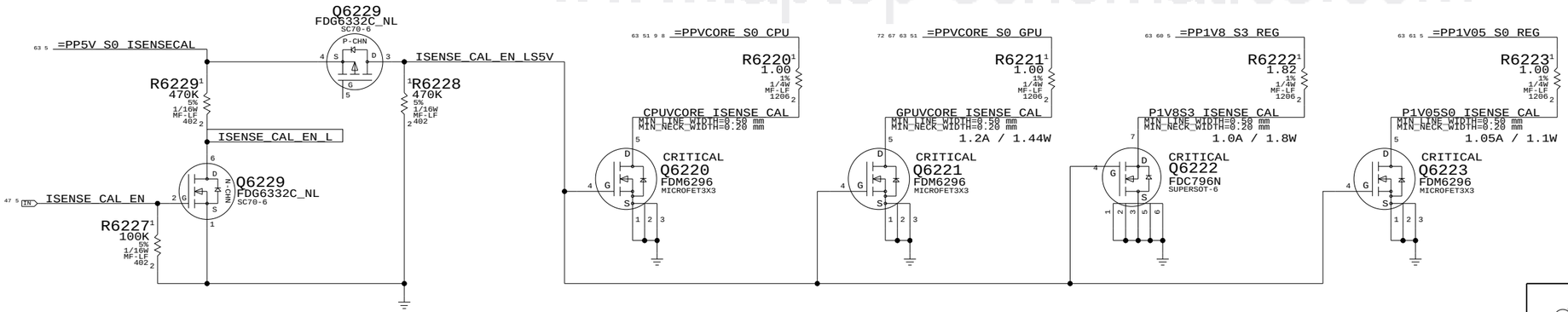


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing			
SYNC_MASTER=M1_MLB	SYNC_DATE=01/05/2006		
NOTICE OF PROPRIETARY PROPERTY			
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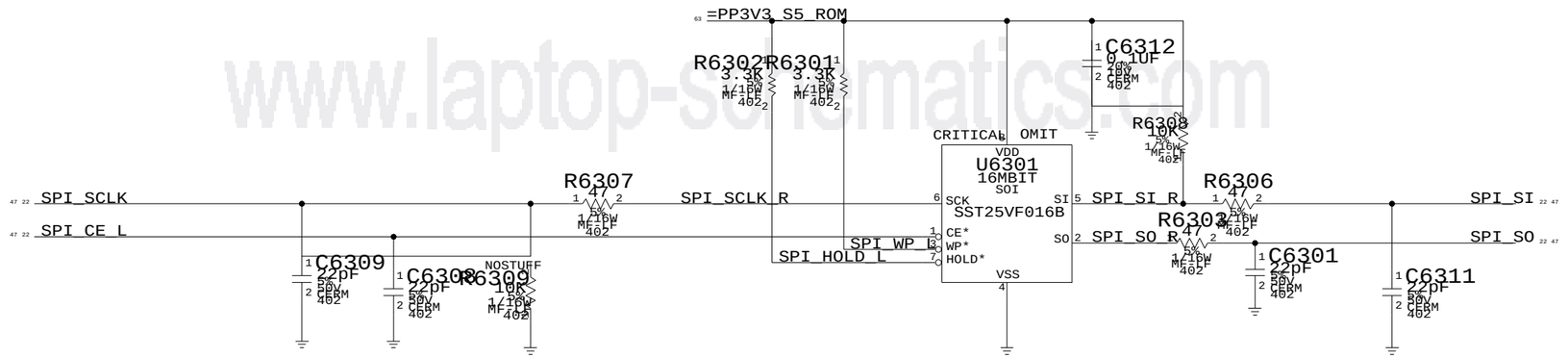
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7155	REV. A
	SCALE NONE	SHT 62 OF 104	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

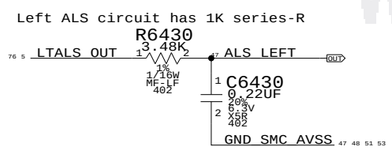
SYNC_MASTER=M37 SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

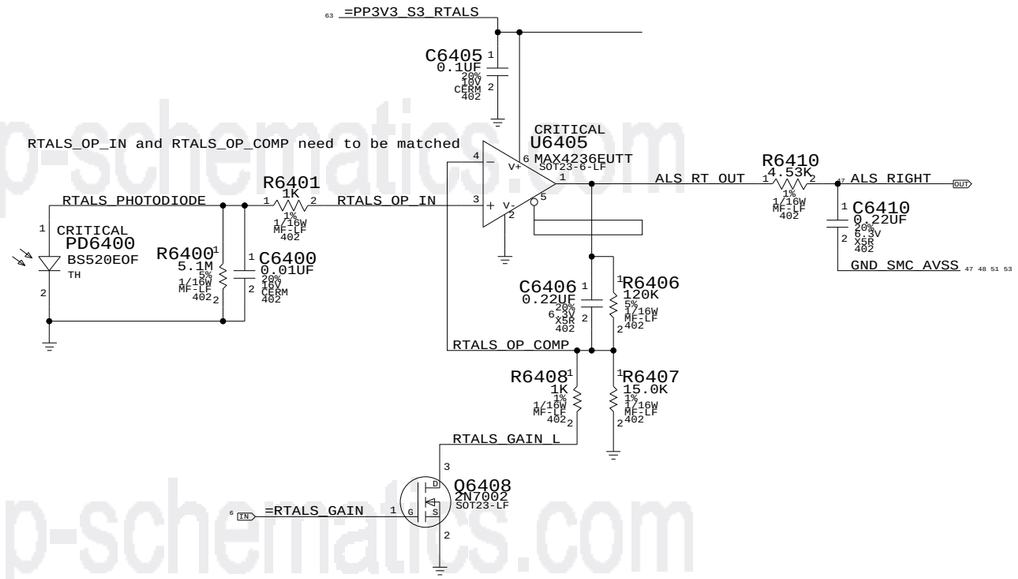
SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE	SHT	OF
NONE	63	104

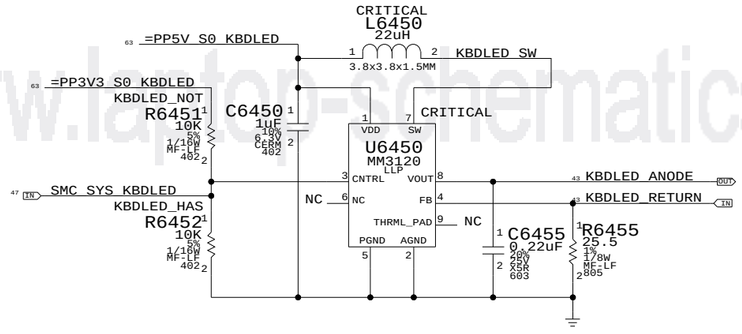
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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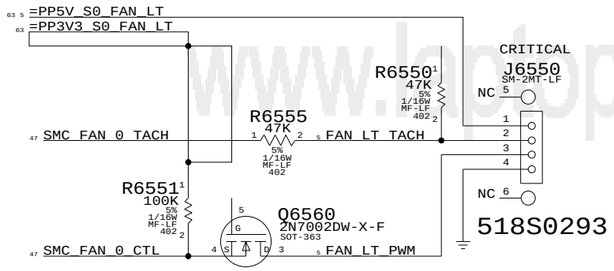
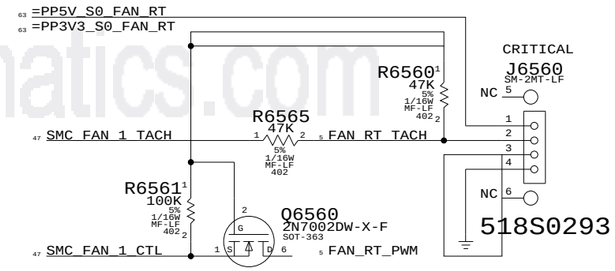
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 64 OF 104	

Left Fan



Right Fan

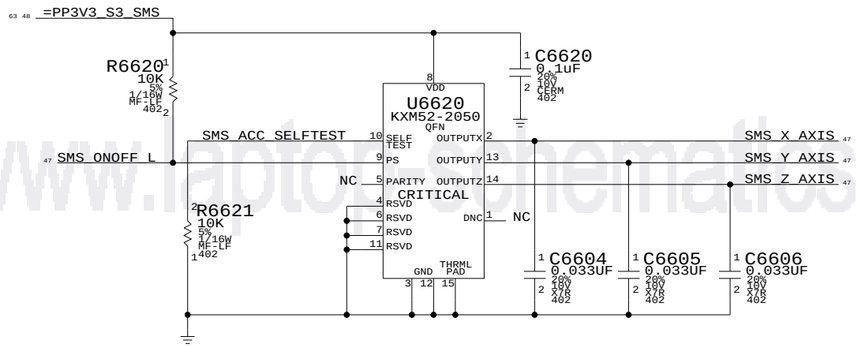


Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

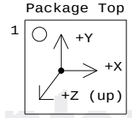
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 65 OF 104	



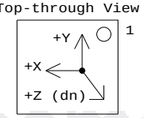
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



M1 placement: Bottom-side

Sudden Motion Sensor (SMS)

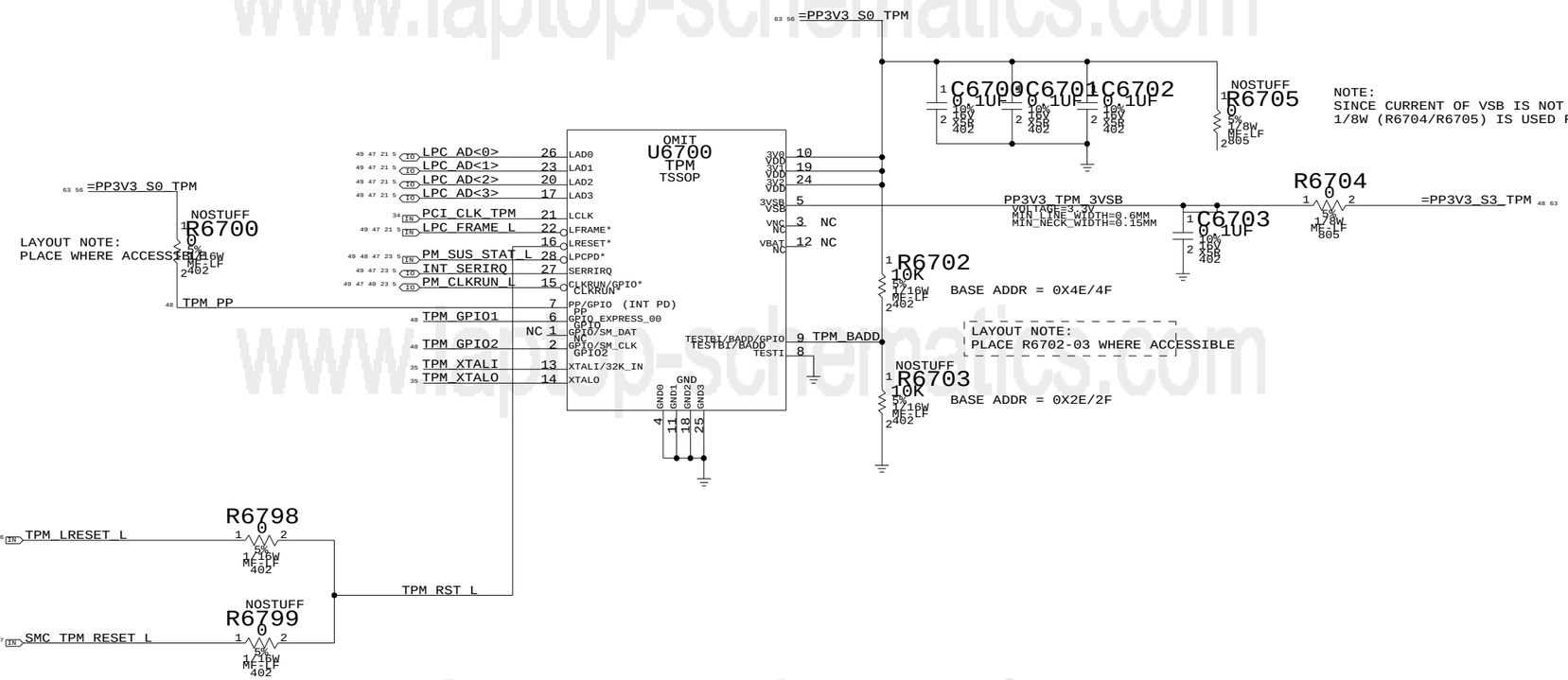
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE: NONE

SHT 66 OF 104



TPM

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE	SHT	OF
NONE	67	104

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

These caps for Q7500

These caps for Q7550

Vout = Variable
36A max output
(Inductors limit)

OMIT
U7530
ISL6262
QFN

Vout = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kddroop) + Vamp_offset
Gain = Rc / (Ra + Rb)
Voffset worst-case ~2.3mV (+/- ~1A offset)
Vout @ 36A = 2.44V-2.60V

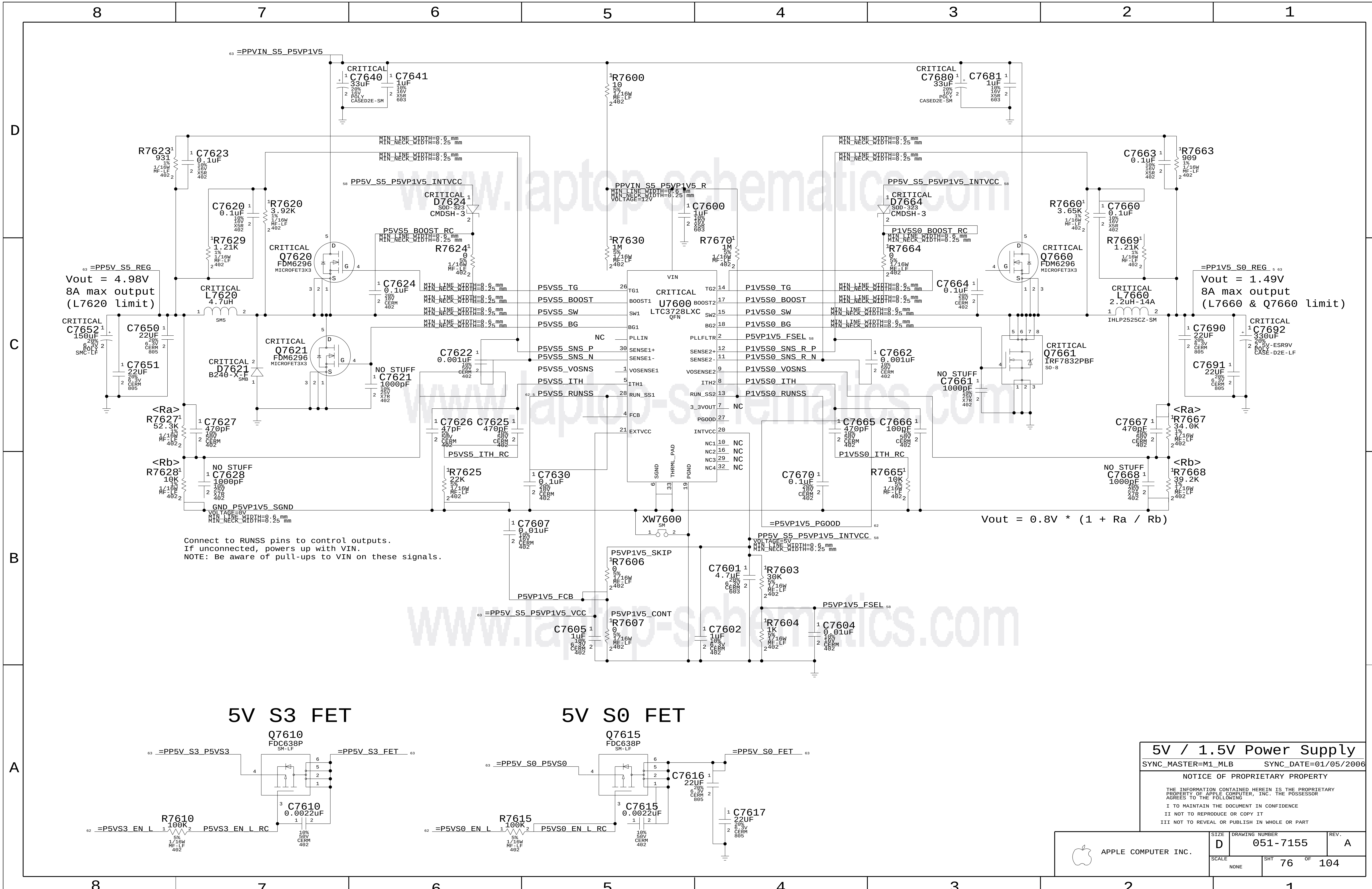
CPU VCore Current Sense

IMVP6 CPU VCore Regulator

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 75 OF 104	



=PPVIN_S5_P5VP1V5
CRITICAL C7640 33uF
C7641 1uF
R7600 10
CRITICAL C7680 33uF
C7681 1uF
R7623 931
C7623 0.1uF
C7620 0.1uF
R7620 3.92K
R7629 1.21K
PP5V_S5_P5VP1V5_INTVCC
CRITICAL D7624 CMDSH-3
P5VS5_BOOST_RC
R7624 0
CRITICAL Q7620 FDM6296
=PP5V_S5_REG
Vout = 4.98V
8A max output
(L7620 limit)
CRITICAL L7620 4.7uH
CRITICAL C7652 150uF
C7650 22UF
C7651 22UF
CRITICAL D7621 B240-X-F
CRITICAL Q7621 FDM6296
C7624 0.1uF
NO STUFF C7621 1000pF
C7622 0.001uF
PPVIN_S5_P5VP1V5_R
VOLTAGE=12V
C7600 1uF
R7630 1M
R7670 1M
CRITICAL U7600 LTC3728LXC
P5VS5_TG
P5VS5_BOOST
P5VS5_SW
P5VS5_BG
P5VS5_SNS_P
P5VS5_SNS_N
P5VS5_VOSNS
P5VS5_ITH
P5VS5_RUNSS
P1V5S0_TG
P1V5S0_BOOST
P1V5S0_SW
P1V5S0_BG
P5VP1V5_FSEL
P1V5S0_SNS_R_P
P1V5S0_SNS_R_N
P1V5S0_VOSNS
P1V5S0_ITH
P1V5S0_RUNSS
PP5V_S5_P5VP1V5_INTVCC
CRITICAL D7664 CMDSH-3
P1V5S0_BOOST_RC
R7664 0
C7663 0.1uF
R7663 909
R7660 3.65K
C7660 0.1uF
R7669 1.21K
CRITICAL Q7660 FDM6296
C7664 0.1uF
=PP1V5_S0_REG
Vout = 1.49V
8A max output
(L7660 & Q7660 limit)
CRITICAL L7660 2.2uH-14A
CRITICAL Q7661 IRF7832PBF
C7662 0.001uF
NO STUFF C7661 1000pF
C7690 22UF
CRITICAL C7692 330uF
C7691 22UF
<Ra> R7627 52.3K
C7627 470pF
<Rb> R7628 10K
NO STUFF C7628 1000pF
C7626 47pF
C7625 470pF
P5VS5_ITH_RC
R7625 22K
C7630 0.1uF
GND_P5VP1V5_SGND
VOLTAGE=0V
XW7600
C7665 470pF
C7666 100pF
P1V5S0_ITH_RC
C7670 0.1uF
R7665 10K
C7667 470pF
<Ra> R7667 34.0K
<Rb> R7668 39.2K
NO STUFF C7668 1000pF
=P5VP1V5_PGOOD
Vout = 0.8V * (1 + Ra / Rb)
C7607 0.01uF
Connect to RUNSS pins to control outputs.
If unconnected, powers up with VIN.
NOTE: Be aware of pull-ups to VIN on these signals.
P5VP1V5_SKIP
R7606 0
P5VP1V5_FCB
=PP5V_S5_P5VP1V5_VCC
P5VP1V5_CONT
R7607 0
C7605 1uF
C7601 4.7uF
R7603 30K
P5VP1V5_FSEL
R7604 1K
C7602 1uF
C7604 0.01uF
5V S3 FET
Q7610 FDC638P
=PP5V_S3_P5VS3
=PP5V_S3_FET
C7610 0.0022uF
R7610 100K
=P5VS3_EN_L
P5VS3_EN_L_RC
5V S0 FET
Q7615 FDC638P
=PP5V_S0_P5VS0
=PP5V_S0_FET
C7616 22UF
C7617 22UF
C7615 0.0022uF
R7615 100K
=P5VS0_EN_L
P5VS0_EN_L_RC

5V / 1.5V Power Supply

SYNC_MASTER=M1_MLB SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

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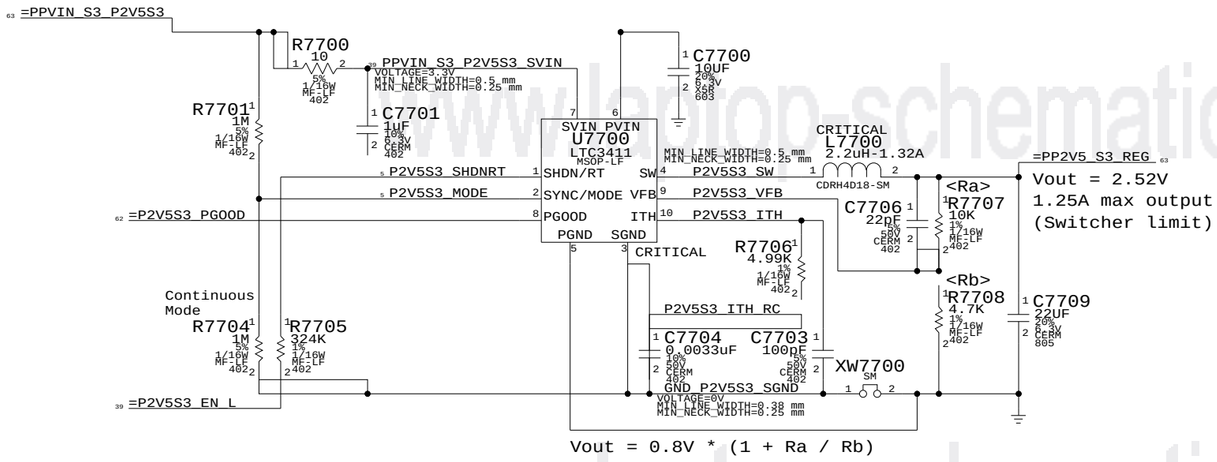
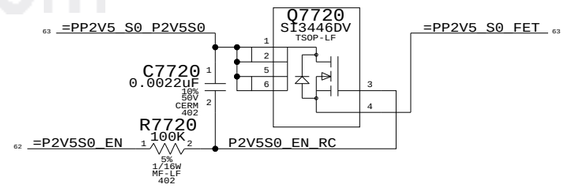
D	051-7155	A
SCALE NONE	SHT 76 OF 104	

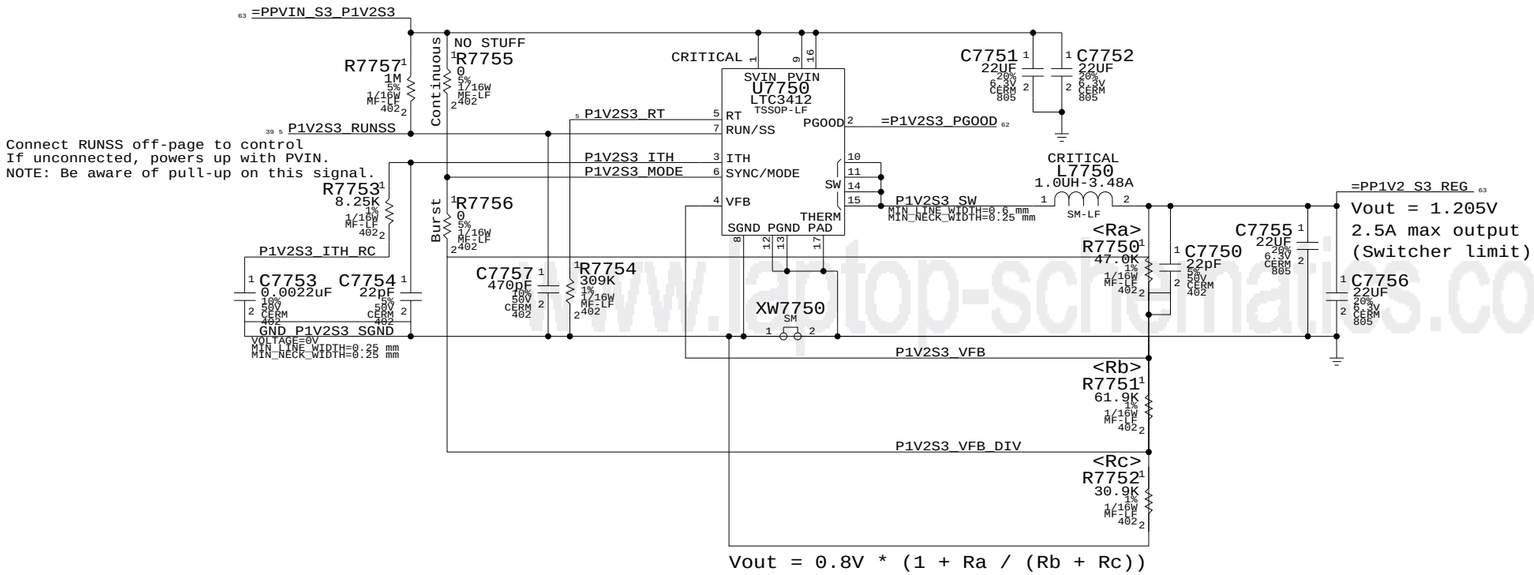
2.5V S3 Regulator



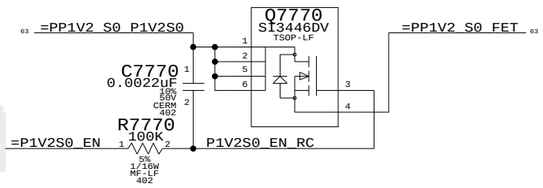
2.5V S0 FET



1.2V S3 Regulator



1.2V S0 FET



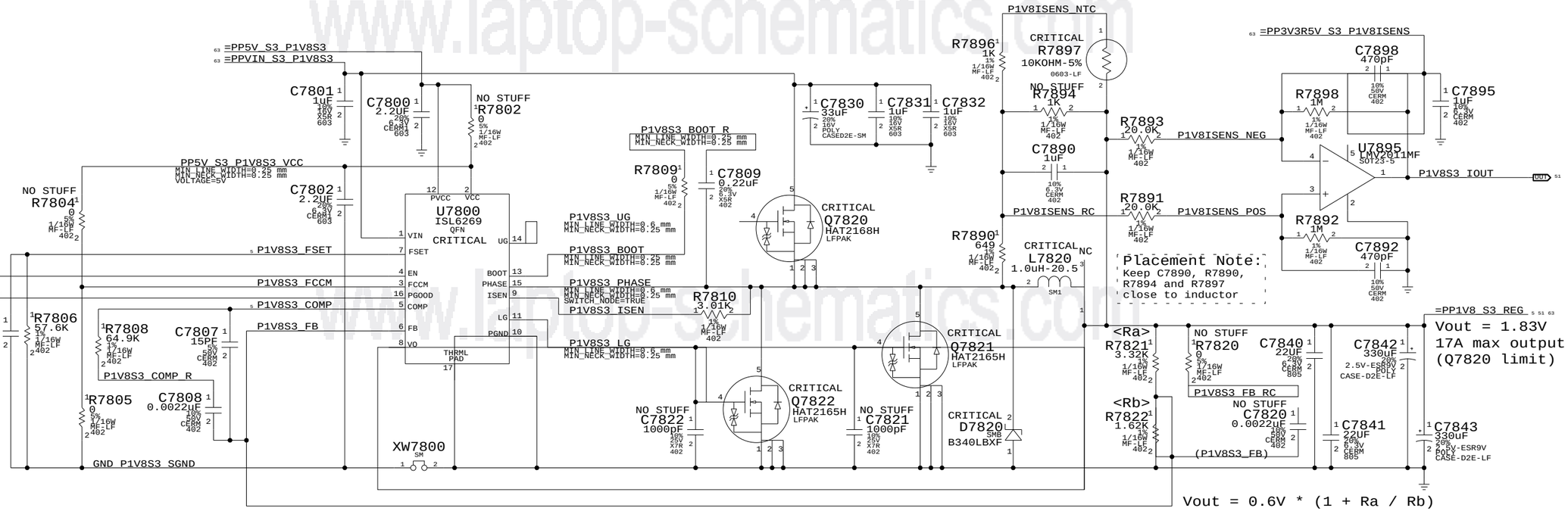
2.5V & 1.2V Regulators

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

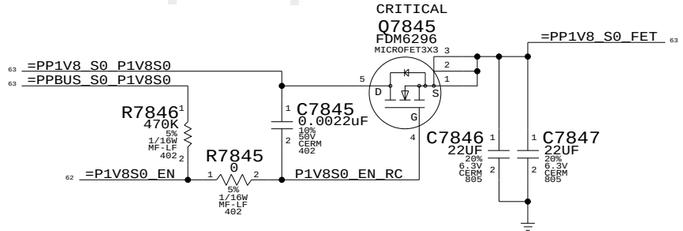
SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 77 OF 104	

1.8V S3 Current Sense



Vout = 0.6V * (1 + Ra / Rb)

1.8V S0 FET

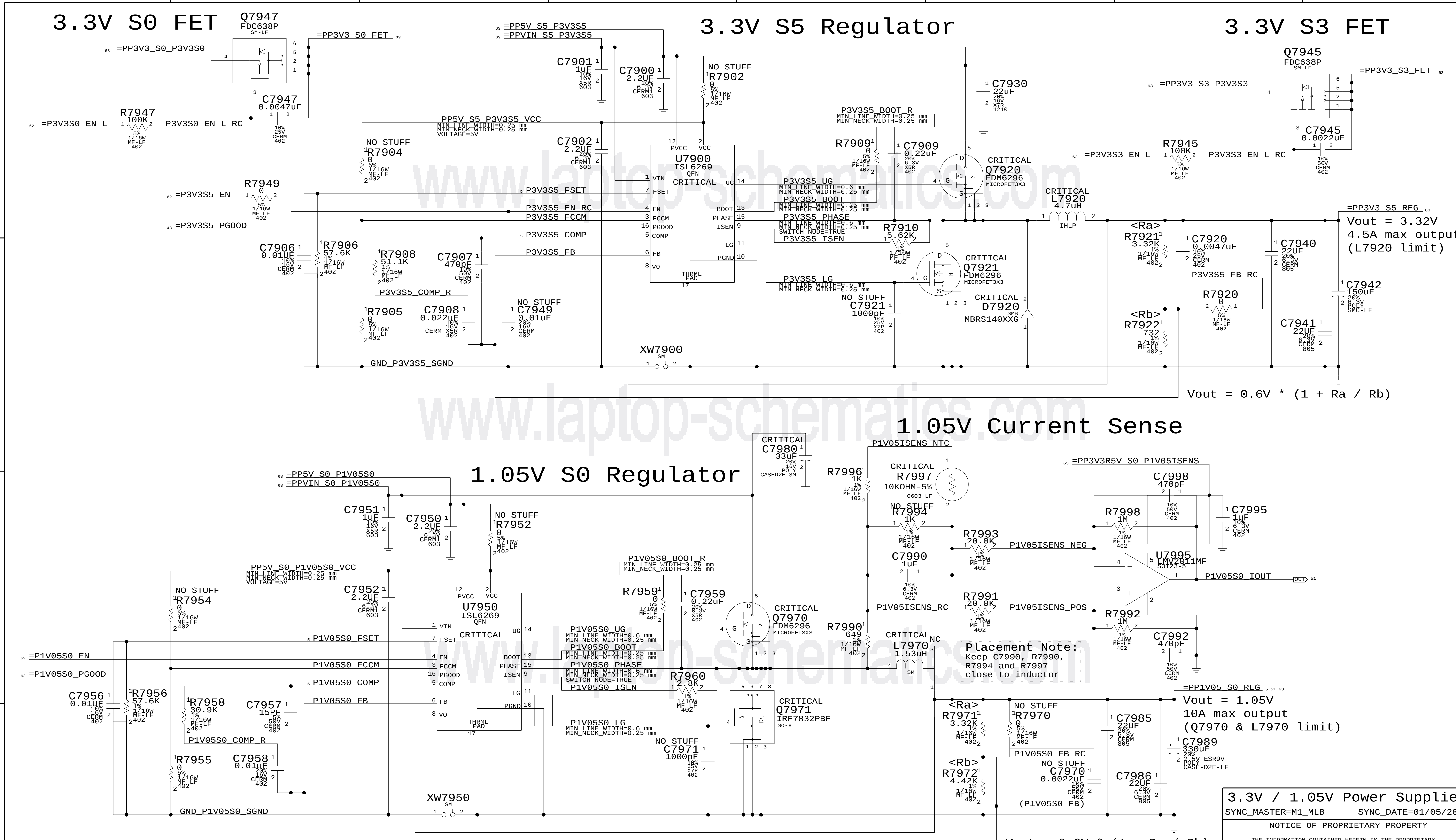


1.8V Supply

SYNC_MASTER=M1_MLB SYNC_DATE=01/05/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 78 OF 104	



3.3V / 1.05V Power Supplies

SYNC_MASTER=M1_MLB SYNC_DATE=01/05/2006

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7155 | REV. A

SCALE NONE | SHT 79 OF 104

Power Control Signals

=PP5V_S5_PWRCTL

R8050 10K 5% 1/10W MF-LF 402
R8051 10K 5% 1/10W MF-LF 402
R8052 10K 5% 1/10W MF-LF 402

GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up.

=GPUVCORE_PGOOD

Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.

PM_SLP_S3_LS5V_L → =P2V5S0_EN, =P1V2S0_EN
P3V3S0_EN_L → =P3V3S0_EN_L
P1V8S0_EN → =P1V8S0_EN

1.8V Enable has pull-up to PBUS

Q8055 2N7002DW-X-F SOT-363
Q8056 2N7002DW-X-F SOT-363
Q8050 2N7002DW-X-F SOT-363

=PP3V42_G3H_PWRCTL

PM_SLP_S3_LS5V → =P5VS0_EN_L, LIO_P3V3S0_EN_L

Q8050 2N7002DW-X-F SOT-363
R8054 100K 5% 1/10W MF-LF 402

P1V5S0_RUNSS

1.5V Enable has pull-up to PBUS

Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3

Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3_L
R8056 100K 5% 1/10W MF-LF 402

(PM_SLP_S3_L) → =P1V05S0_EN, =ENET_VMAIN_AVLBL, =MEMVREF_EN, =PBUSVSENS_EN

=P2V5S3_PGOOD
=P1V2S3_PGOOD

NO STUFF
R8060 0 5% 1/10W MF-LF 402

P2V5S3_P1V2S3_PGOOD → GPUVCORE_EN → =GPUVCORE_EN

R8053 10K 5% 1/10W MF-LF 402

Ensure 1.2V and 2.5V S3 supplies are up before enabling GPU VCore to support removing ethernet power in battery sleep.

=PP5V_S5_PWRCTL

R8055 10K 5% 1/10W MF-LF 402

PM_SLP_S4_LS5V → =P3V3S3_EN_L, =P5VS3_EN_L

Q8055 2N7002DW-X-F SOT-363

PM_SLP_S4_L
R8057 100K 5% 1/10W MF-LF 402

2.5V S3 and 1.2V S3 supplies are controlled by ethernet power control circuit.

(PM_SLP_S4_L) → =P1V8S3_EN, =RTUSB_EN, LIO_P3V3S3_EN

=PP3V42_G3H_PWRCTL

P5VS5_PGOOD
(P5VS5_PGOOD) → =P3V3S5_EN

R8059 470K 5% 1/10W MF-LF 402

P5VS5_RUNSS

5V Enable has pull-up to PBUS

SMC_PM_G2_EN_L

Q8059 2N7002DW-X-F SOT-363
Q8059 2N7002DW-X-F SOT-363

SMC_PM_G2_EN
R8058 100K 5% 1/10W MF-LF 402

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

=PPVIN_G3H_P3V42G3H

C8000 10uF 20% 25V X5R 1206

U8000 LT3470 TSOT23-8
VIN, BOOST, SHDN*, SW, BIAS, NC, NC CRITICAL, FB, GND

P3V42G3H5_BOOST
C8005 0.22uF 20% 6.3V X5R 402

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

CRITICAL
L8010 33uH CDPH4D19F-SM

=PP3V42_G3H_REG

Vout = 3.425
200mA max output
(Switcher limit)

C8010 22pF 5% 50V CERM 402

<Ra> R8010 348K 1% 1/16W MF-LF 402
<Rb> R8011 200K 1% 1/16W MF-LF 402

C8015 22UF 20% 6.3V CERM 805

P3V42G3H_FB

Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

=PP3V3_S5_P1V5PG
PP1V5_S0

0.89V Reference

R8061 27.4K 1% 1/10W MF-LF 402
R8063 4.99K 1% 1/16W MF-LF 402
R8062 10K 1% 1/10W MF-LF 402
R8064 10K 1% 1/16W MF-LF 402

C8060 0.1uF 20% 10V CERM 402

U8060 LMC7211 SM-LF
P1V0_P1V5PG_REF
P1V5S0_COMP_POS
P1V5S0_PGOOD

R8065 10K 5% 1/10W MF-LF 402

1.5V Comp threshold set to 1.32V (88%)

IMVP_PWRGD_IN

=P1V05S0_PGOOD
P1V5P1V05S0_PGOOD

ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)
NOTE: R8065 acts as 10K pull-up for PGOOD signal

Unused PGOOD Signals

=P5VP1V5_PGOOD — TP_P5V_P1V5_PGOOD
=P1V8S3_PGOOD — TP_P1V8S3_PGOOD

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation

PP5V_S0
PP3V3_S0
PP2V5_S0
PP1V8_S0
PP1V2_S0
PP0V9_S0

C8070 0.1uF 20% 10V CERM 402
C8071 0.1uF 20% 10V CERM 402

U8070 LTC2908 LLP
V1, V2, V3, V4 CRITICAL, VADJ1, VADJ2, GND, RST*, THRML PAD

R8074 68.1K 1% 1/10W MF-LF 402
R8072 124K 1% 1/16W MF-LF 402
R8075 100K 1% 1/10W MF-LF 402
R8073 100K 1% 1/16W MF-LF 402

S0PGOOD_1V2_DIV
S0PGOOD_0V9_DIV

S0PGOOD_PWROK

R8076 549K 1% 1/16W MF-LF 402

LTC2908 sources 6uA at 5.0V
R8076 serves as pull-down and 3.3V level-shifter.

LTC2908 threshold is 95% (4.75V, 3.135V, 2.375V, 1.71V, 1.14V, 0.86V)

=PP3V3_S0_ALLSYSPG

U8080 MC74VHC1G08 SC70
ALL_SYS_PWRGD

C8080 0.1uF 20% 10V CERM 402

3.3V G3Hot Supply & Power Control

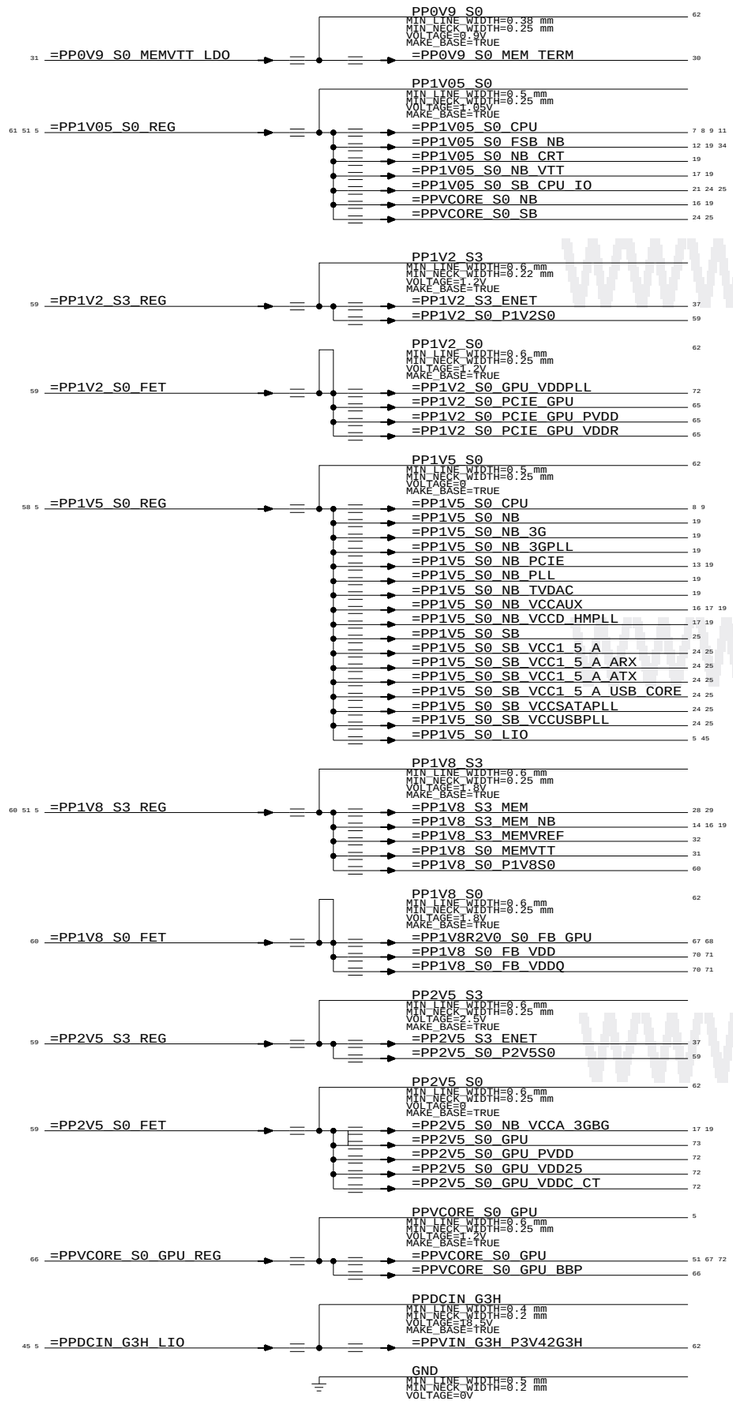
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

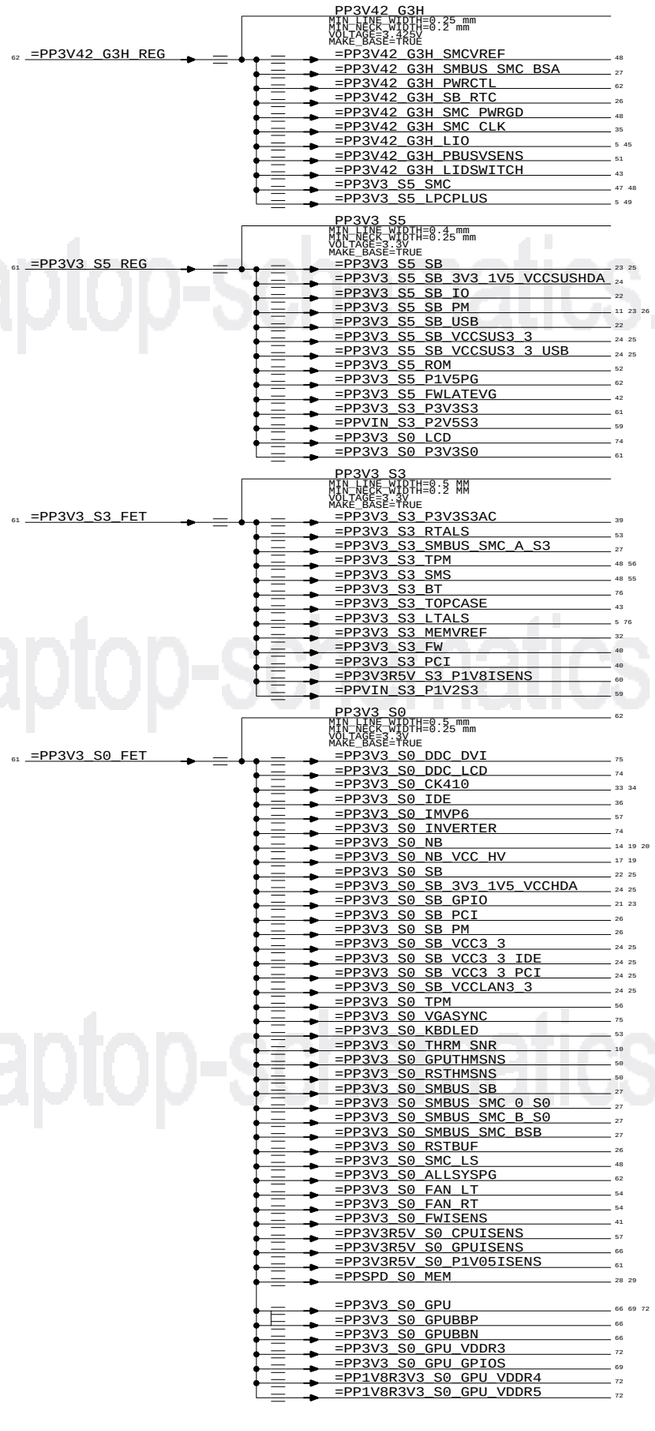
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

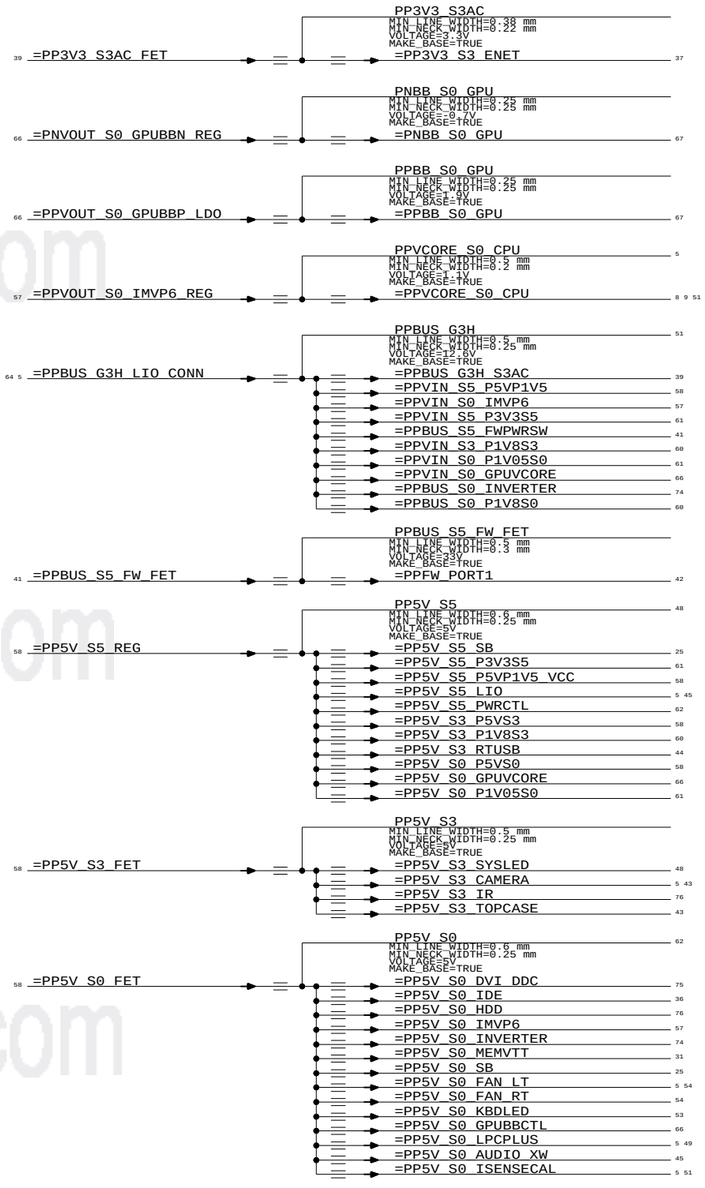
SCALE: NONE

SHT 80 OF 104





"S3AC" rail is ON in S3 on AC, OFF in S3 on battery



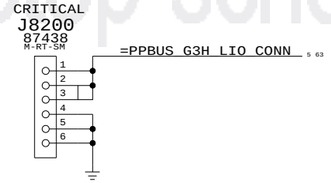
Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

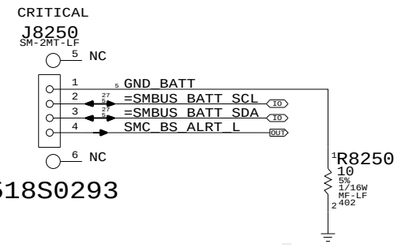
SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 81 OF 104	

Left I/O Power Connector



518S0368

Battery Connector (Digital Signals)



518S0293

PBus-In & Battery Connectors

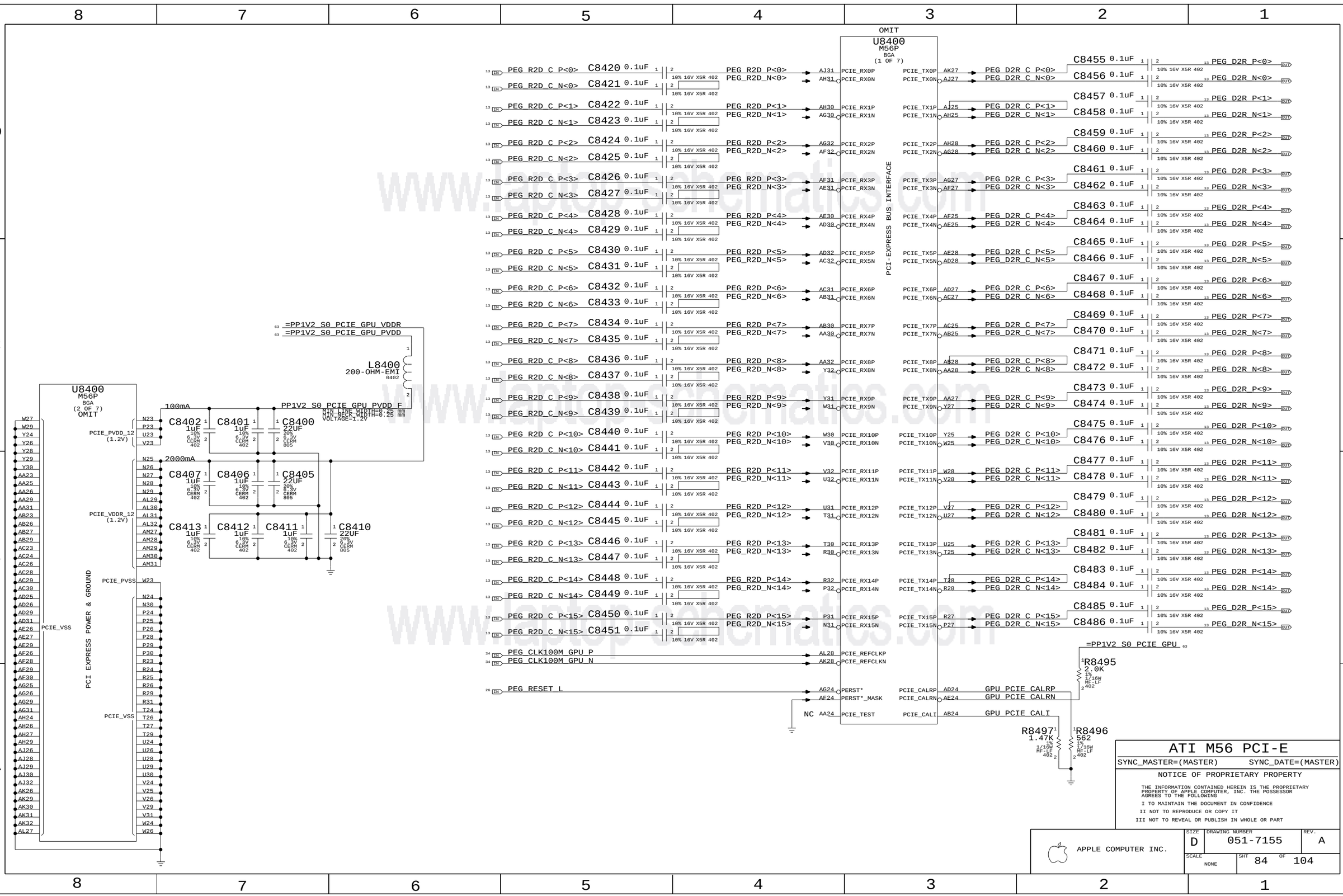
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE NONE

SHT 82 OF 104



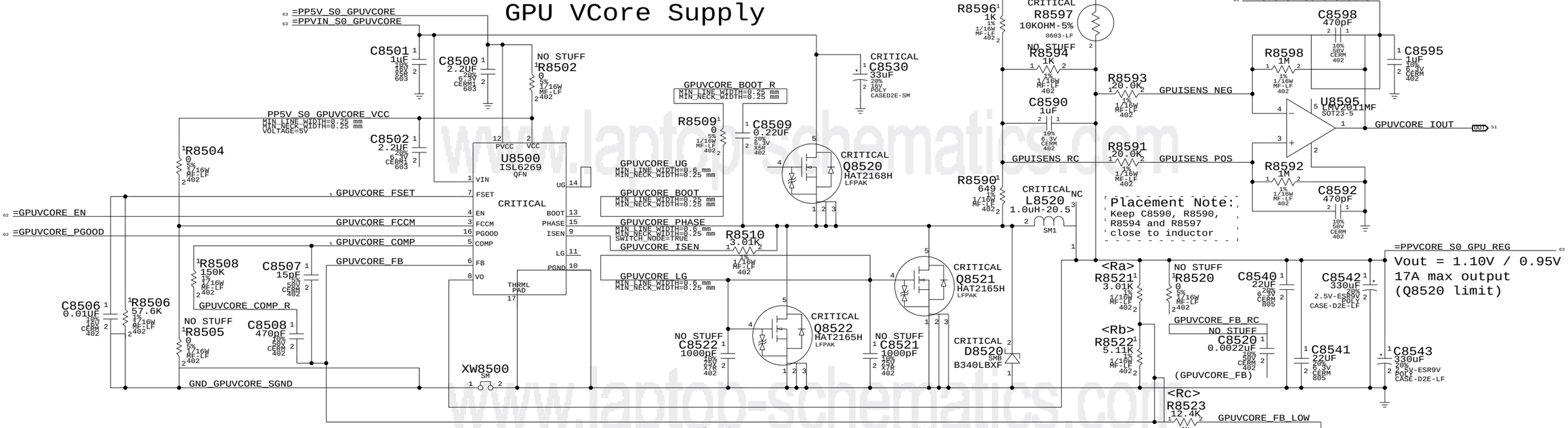
ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 84 OF 104	

GPU VCore Supply

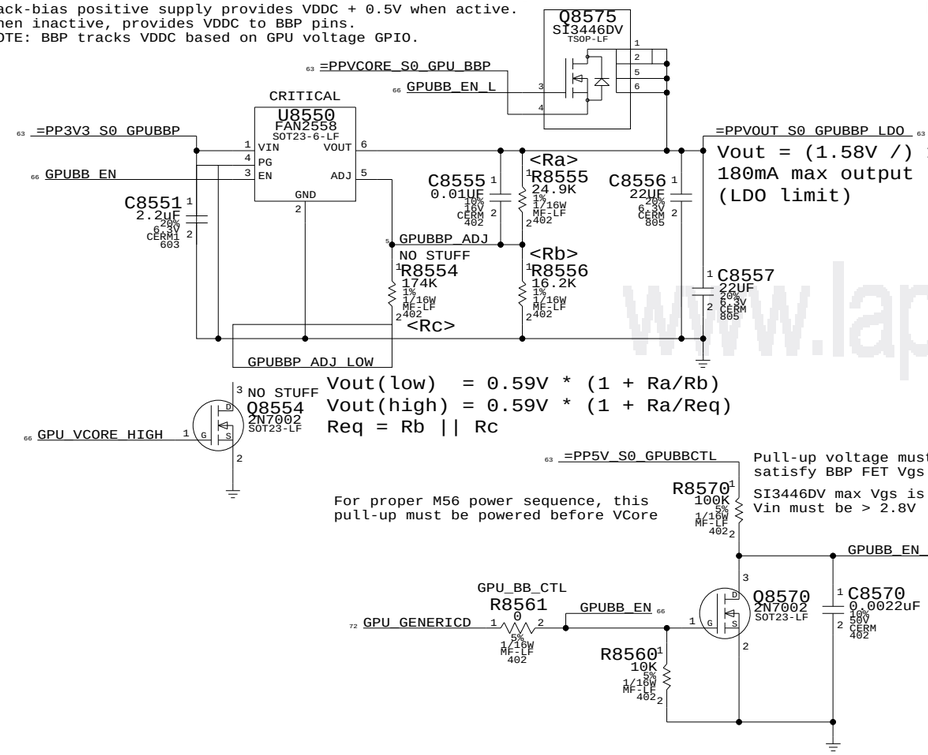


Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

GPU VCore Current Sense

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.



=PP5V_S0_GPUBBCTL

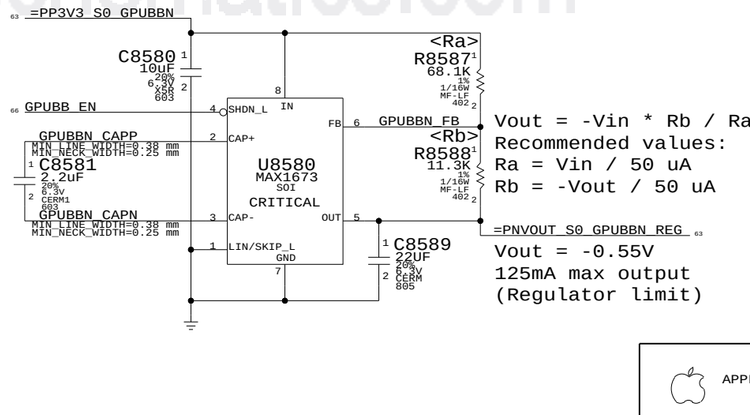
Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)

SI3446DV max Vgs is 1.6V
Vin must be > 2.8V

For proper M56 power sequence, this pull-up must be powered before VCore

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active.
When inactive, provides VSS to BBN pins.



GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

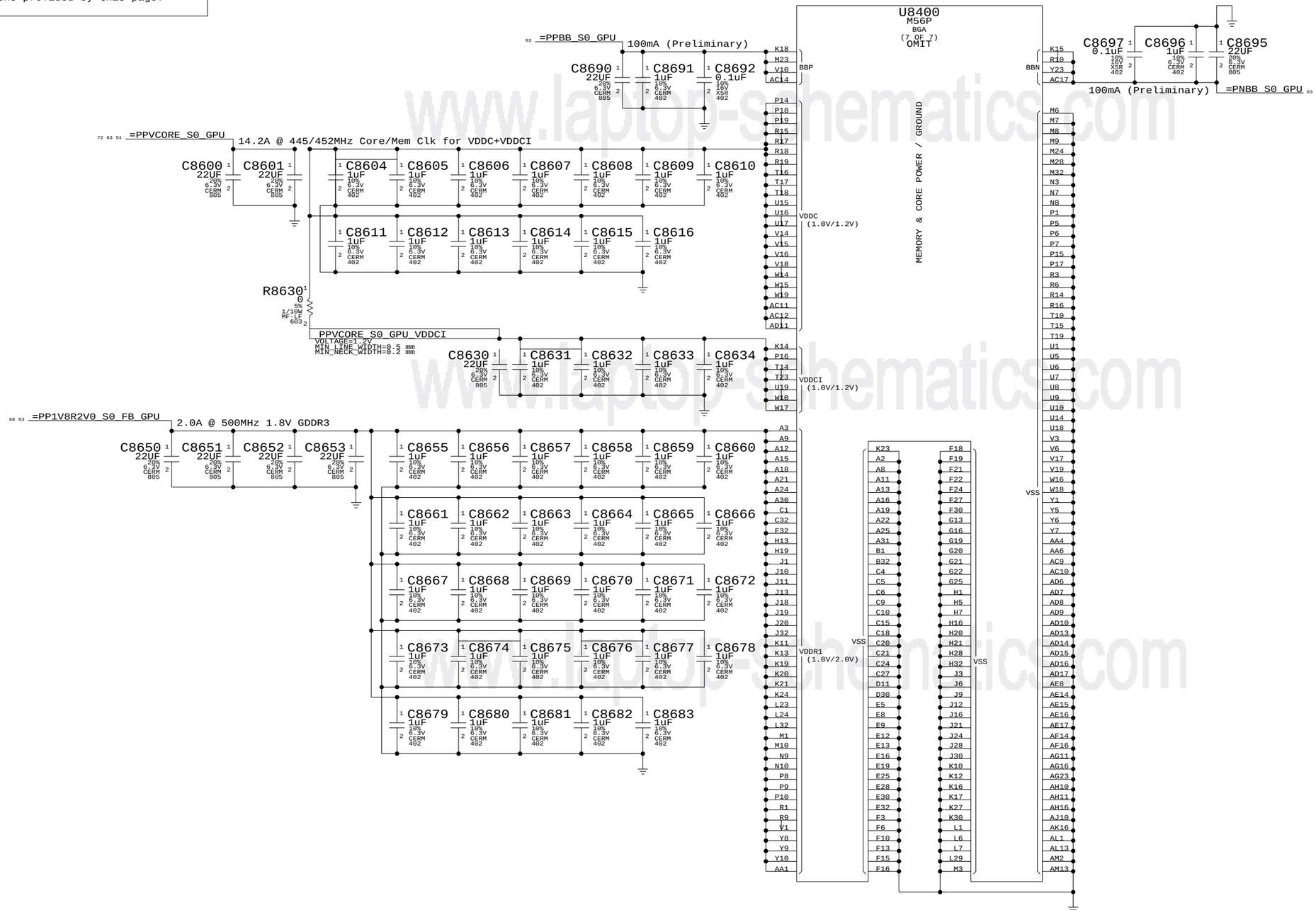
SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 85 OF 104	

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

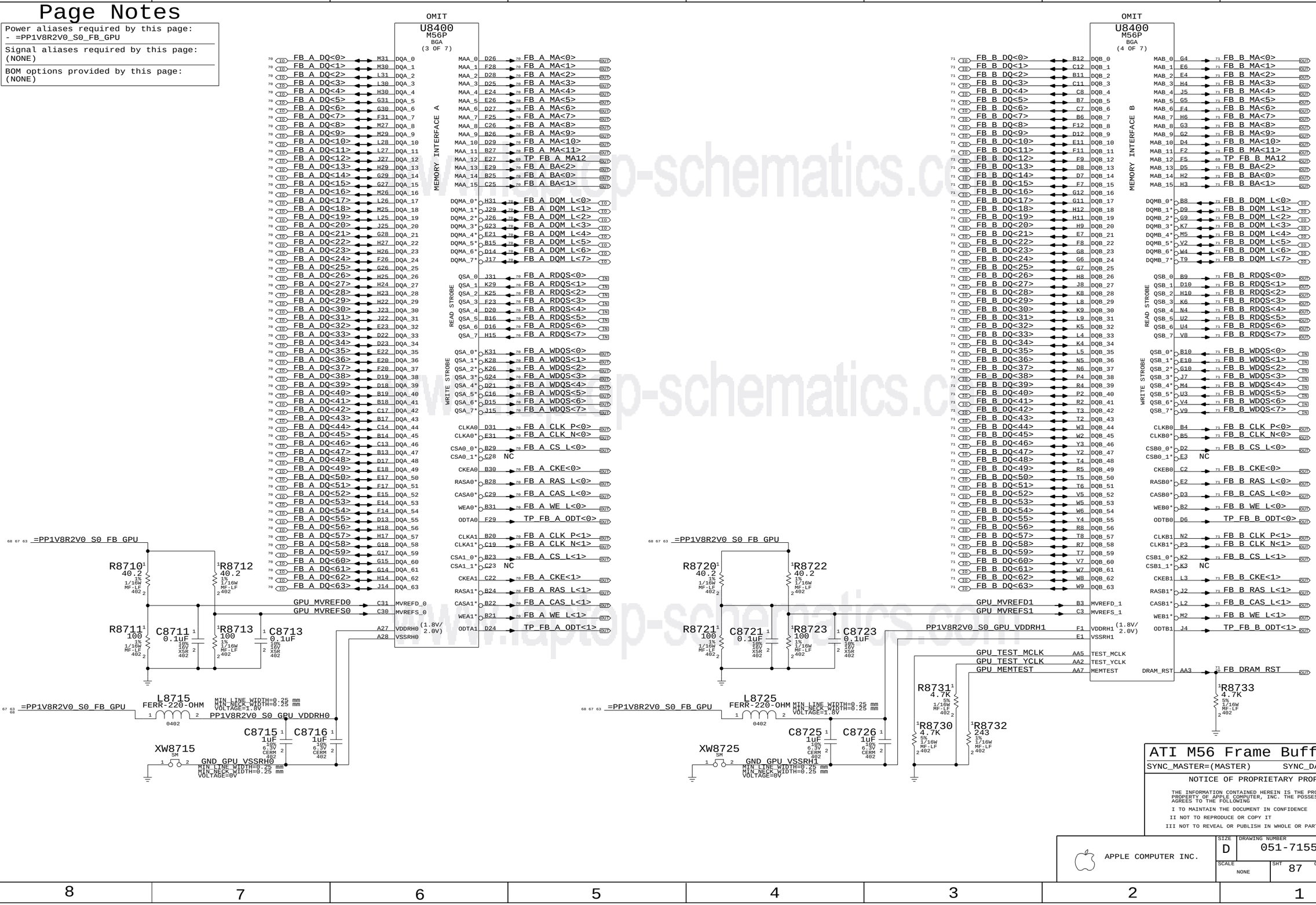
SCALE	SHT	OF
NONE	86	104

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE: NONE

SHT 87 OF 104

ROMCFGID[3..0]
0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

63 =PP3V3_S0_GPU_GPIOS

R8800 10K 5% 1/16W MF-LF 402
R8802 NO STUFF 10K 5% 1/16W MF-LF 402
R8804 NO STUFF 10K 5% 1/16W MF-LF 402
R8806 NO STUFF 10K 5% 1/16W MF-LF 402
R8809 NO STUFF 10K 5% 1/16W MF-LF 402
R8812 GPU_MEM_256M 10K 5% 1/16W MF-LF 402
R8824 GPU_MEM_256M 10K 5% 1/16W MF-LF 402

R8801 GPU_DEEPMH_EN 10K 5% 1/16W MF-LF 402
R8803 NO STUFF 10K 5% 1/16W MF-LF 402
R8805 10K 5% 1/16W MF-LF 402
R8808 NO STUFF 10K 5% 1/16W MF-LF 402
R8813 GPU_MEM_64M 10K 5% 1/16W MF-LF 402
R8811 NO STUFF 10K 5% 1/16W MF-LF 402
R8827 GPU_MEM_HYNIX 10K 5% 1/16W MF-LF 402

		Serial ROM	TestBus	Misc	Straps	
72	GPU_GPIO_0	IPD	TESTIN[0]		TX_PWRS_ENb	
72	GPU_GPIO_1	IPD	TESTIN[1]		TX_DEEMPH_EN	
72	GPU_GPIO_2	VDD_VCL	TESTIN[2]		Reserved	
72	GPU_GPIO_3		TESTIN[3]		Reserved	
72	GPU_GPIO_4	IPD	TESTIN[4]		DEBUG_ACCESS	
72	GPU_GPIO_5		TESTIN[5]		Reserved	
72	GPU_GPIO_6		TESTIN[6]		Reserved	
72	GPU_GPIO_7	ENA_BL	TESTIN[7]			= GPU_BLON (74) MAKE_BASE=TRUE
72	GPU_GPIO_8	ROMSO	TESTWR		Reserved	
72	GPU_GPIO_9	IPD ROMSI			ROMIDCFG[3]	
72	GPU_GPIO_10	ROMSCK	TESTOUT[8]			= TP_GPU_GPIO_10 MAKE_BASE=TRUE
72	GPU_GPIO_11	IPD	TESTOUT[9]		ROMIDCFG[0]	Required for debug access
72	GPU_GPIO_12	IPD	TESTOUT[10]		ROMIDCFG[1]	Required for debug access
72	GPU_GPIO_13	IPD	TESTOUT[11]		ROMIDCFG[2]	Required for debug access
72	GPU_GPIO_14		TESTIN[8]			Required for debug access
72	GPU_GPIO_15		TESTIN[9]	PWRCNTL		= NC_GPU_GPIO_14 MAKE_BASE=TRUE NO_TEST=TRUE
72	GPU_GPIO_16			SS_IN		= GPU_VCORE_LOW (66) MAKE_BASE=TRUE
72	GPU_GPIO_17			Thm Mon Int		= GPU_CLK27MSS_IN (34) MAKE_BASE=TRUE
						= NC_GPU_GPIO_17 MAKE_BASE=TRUE NO_TEST=TRUE

72 GPU_GPIO_18 = NC_GPU_GPIO_18 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_19 = NC_GPU_GPIO_19 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_20 = NC_GPU_GPIO_20 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_21 = NC_GPU_GPIO_21 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_22 = NC_GPU_GPIO_22 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_23 = NC_GPU_GPIO_23 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_24 = GPU_MEM_256M MAKE_BASE=TRUE
72 GPU_GPIO_25 = NC_GPU_GPIO_25 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_26 = NC_GPU_GPIO_26 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_27 = GPU_MEMID MAKE_BASE=TRUE
72 GPU_GPIO_28 = NC_GPU_GPIO_28 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_29 = NC_GPU_GPIO_29 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_30 = NC_GPU_GPIO_30 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_31 = NC_GPU_GPIO_31 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_32 = NC_GPU_GPIO_32 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_33 = NC_GPU_GPIO_33 MAKE_BASE=TRUE NO_TEST=TRUE
72 GPU_GPIO_34 = NC_GPU_GPIO_34 MAKE_BASE=TRUE NO_TEST=TRUE

Renamed signals

34 GPU_CLK27M = GPU_XTALIN (72) MAKE_BASE=TRUE

Unused signals

NC_GPU_XTALOUT = GPU_XTALOUT (72) MAKE_BASE=TRUE NO_TEST=TRUE
NC_ATI_ROMCS_L = TP_ATI_ROMCS_L (72) MAKE_BASE=TRUE NO_TEST=TRUE
NC_FB_A_MA12 = TP_FB_A_MA12 (68) MAKE_BASE=TRUE NO_TEST=TRUE
NC_FB_B_MA12 = TP_FB_B_MA12 (68) MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICA = GPU_GENERICA (72) MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICB = GPU_GENERICB (72) MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICC = GPU_GENERICC (72) MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_VGA_R = GPU_VGA_R (73) MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_VGA_G = GPU_VGA_G (73) MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_VGA_B = GPU_VGA_B (73) MAKE_BASE=TRUE NO_TEST=TRUE
TP_GPU_VGA_HSYNC = GPU_VGA_HSYNC (73) MAKE_BASE=TRUE
TP_GPU_VGA_VSYNC = GPU_VGA_VSYNC (73) MAKE_BASE=TRUE
NC_GPU_TV_Y = GPU_TV_Y (73) MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_TV_C = GPU_TV_C (73) MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_TV_COMP = GPU_TV_COMP (73) MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_U_DATAP<3> = LVDS_U_DATA_P<3> (73) MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_U_DATAN<3> = LVDS_U_DATA_N<3> (73) MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_L_DATAP<3> = LVDS_L_DATA_P<3> (73) MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_L_DATAN<3> = LVDS_L_DATA_N<3> (73) MAKE_BASE=TRUE NO_TEST=TRUE
NC_ATI_DVPCLK = ATI_DVPCLK (72) MAKE_BASE=TRUE NO_TEST=TRUE
NC_ATI_DVPCNTL<2..0> = ATI_DVPCNTL<2..0> (72) MAKE_BASE=TRUE NO_TEST=TRUE
NC_ATI_DVPDATA<15..0> = ATI_DVPDATA<15..0> (72) MAKE_BASE=TRUE NO_TEST=TRUE

Required for debug access

TP_ATI_DVPDATA<23..16> = ATI_DVPDATA<23..16> (72) MAKE_BASE=TRUE

Also required: GPIO10 - GPIO13

72 66 63 =PP3V3_S0_GPU

R9390 4.7K 5% 1/16W MF-LF 402
R9391 4.7K 5% 1/16W MF-LF 402

73 GPU_DDC_B_CLK
73 GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_S0_FB_VDD

=PP1V8_S0_FB_VDDQ

C8900 C8901 C8902 C8903 C8904 — 22UF 20% 6.3V CERM 805; 0.1UF 10% 16V X5R 402

L8910 FERR-220-OHM 0402 — PP1V8_S0_FB_A0_VDDA0 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

L8915 FERR-220-OHM 0402 — PP1V8_S0_FB_A0_VDDA1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

Connect to designated pin, then GND

C8910 C8915 — 0.1UF 10% 16V X5R 402 — U8900.J1 U8900.J12

C8920 — 22UF 20% 6.3V CERM 805

C8921 C8922 C8923 C8924 C8925 C8926 — 0.1UF 10% 16V X5R 402

R8930 R8932 — 2.37K 1% 1/10W MF-LF 402

FB_A0_VREF0 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

FB_A0_VREF1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

R8931 R8933 — 5.49K 1% 1/10W MF-LF 402

C8931 C8933 — 0.1UF 10% 16V X5R 402

R8940 R8942 R8944 R8946 — 121 1% 1/10W MF-LF 402; 60.4 1% 1/10W MF-LF 402

R8941 — 1K 5% 1/10W MF-LF 402

R8943 — 121 1% 1/10W MF-LF 402

R8945 — 60.4 1% 1/10W MF-LF 402

R8947 — 121 1% 1/10W MF-LF 402

NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.

CRITICAL OMIT

U8900 FBGA (2 OF 2) 16MX32-GDDR3-500MHZ K4J52324QC-BC20

FB_A_MA<0> FB_A_MA<1> FB_A_MA<2> FB_A_MA<3> FB_A_MA<4> FB_A_MA<5> FB_A_MA<6> FB_A_MA<7> FB_A_MA<8> FB_A_MA<9> FB_A_MA<10> FB_A_MA<11>

FB_A_CKE<0> FB_A_CLK_P<0> FB_A_CLK_N<0> FB_A_CS_L<0> FB_A_WE_L<0> FB_A_CAS_L<0> FB_A_RAS_L<0>

FB_A0_ZQ FB_A0_MF FB_A0_SEN

FB_DRAM_RST

FB_A_RDQS<0> FB_A_RDQS<1> FB_A_RDQS<2> FB_A_RDQS<3>

FB_A_WDQS<0> FB_A_WDQS<1> FB_A_WDQS<2> FB_A_WDQS<3>

FB_A_BA<0> FB_A_BA<1> FB_A_BA<2>

R8948 — 243 1% 1/10W MF-LF 402

R8949 — 100 5% 1/10W MF-LF 402

NC J2 RFU1
NC J3 RFU2

FB_A_DQM_L<0> FB_A_DQM_L<1> FB_A_DQM_L<2> FB_A_DQM_L<3>

FB_A_DQ<0> FB_A_DQ<1> FB_A_DQ<2> FB_A_DQ<3> FB_A_DQ<4> FB_A_DQ<5> FB_A_DQ<6> FB_A_DQ<7> FB_A_DQ<8> FB_A_DQ<9> FB_A_DQ<10> FB_A_DQ<11> FB_A_DQ<15> FB_A_DQ<14> FB_A_DQ<12> FB_A_DQ<13> FB_A_DQ<19> FB_A_DQ<16> FB_A_DQ<18> FB_A_DQ<17> FB_A_DQ<23> FB_A_DQ<21> FB_A_DQ<20> FB_A_DQ<22> FB_A_DQ<24> FB_A_DQ<25> FB_A_DQ<26> FB_A_DQ<27> FB_A_DQ<29> FB_A_DQ<30> FB_A_DQ<28> FB_A_DQ<31>

C8950 C8951 C8952 C8953 C8954 — 22UF 20% 6.3V CERM 805; 0.1UF 10% 16V X5R 402

L8960 FERR-220-OHM 0402 — PP1V8_S0_FB_A1_VDDA0 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

L8965 FERR-220-OHM 0402 — PP1V8_S0_FB_A1_VDDA1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

Connect to designated pin, then GND

C8960 C8965 — 0.1UF 10% 16V X5R 402 — U8900.J1 U8900.J12

C8970 — 22UF 20% 6.3V CERM 805

C8971 C8972 C8973 C8974 C8975 C8976 — 0.1UF 10% 16V X5R 402

R8980 R8982 — 2.37K 1% 1/10W MF-LF 402

FB_A1_VREF0 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

FB_A1_VREF1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

R8981 R8983 — 5.49K 1% 1/10W MF-LF 402

C8981 C8983 — 0.1UF 10% 16V X5R 402

R8990 R8992 R8994 R8996 — 121 1% 1/10W MF-LF 402; 60.4 1% 1/10W MF-LF 402

R8991 — 1K 5% 1/10W MF-LF 402

R8993 — 121 1% 1/10W MF-LF 402

R8995 — 60.4 1% 1/10W MF-LF 402

R8997 — 121 1% 1/10W MF-LF 402

CRITICAL OMIT

U8950 FBGA (1 OF 2) 16MX32-GDDR3-500MHZ K4J52324QC-BC20

FB_A_MA<0> FB_A_MA<1> FB_A_MA<2> FB_A_MA<3> FB_A_MA<4> FB_A_MA<5> FB_A_MA<6> FB_A_MA<7> FB_A_MA<8> FB_A_MA<9> FB_A_MA<10> FB_A_MA<11>

FB_A_CKE<1> FB_A_CLK_P<1> FB_A_CLK_N<1> FB_A_CS_L<1> FB_A_WE_L<1> FB_A_CAS_L<1> FB_A_RAS_L<1>

FB_A1_ZQ FB_A1_MF FB_A1_SEN

FB_DRAM_RST

FB_A_RDQS<4> FB_A_RDQS<5> FB_A_RDQS<6> FB_A_RDQS<7>

FB_A_WDQS<4> FB_A_WDQS<5> FB_A_WDQS<6> FB_A_WDQS<7>

FB_A_BA<0> FB_A_BA<1> FB_A_BA<2>

R8998 — 243 1% 1/10W MF-LF 402

R8999 — 100 5% 1/10W MF-LF 402

NC J2 RFU1
NC J3 RFU2

FB_A_DQM_L<4> FB_A_DQM_L<5> FB_A_DQM_L<6> FB_A_DQM_L<7>

FB_A_DQ<32> FB_A_DQ<34> FB_A_DQ<33> FB_A_DQ<35> FB_A_DQ<36> FB_A_DQ<37> FB_A_DQ<38> FB_A_DQ<39> FB_A_DQ<40> FB_A_DQ<41> FB_A_DQ<42> FB_A_DQ<43> FB_A_DQ<46> FB_A_DQ<44> FB_A_DQ<47> FB_A_DQ<45> FB_A_DQ<48> FB_A_DQ<49> FB_A_DQ<50> FB_A_DQ<51> FB_A_DQ<52> FB_A_DQ<55> FB_A_DQ<54> FB_A_DQ<53> FB_A_DQ<60> FB_A_DQ<59> FB_A_DQ<61> FB_A_DQ<57> FB_A_DQ<62> FB_A_DQ<56> FB_A_DQ<63> FB_A_DQ<58>

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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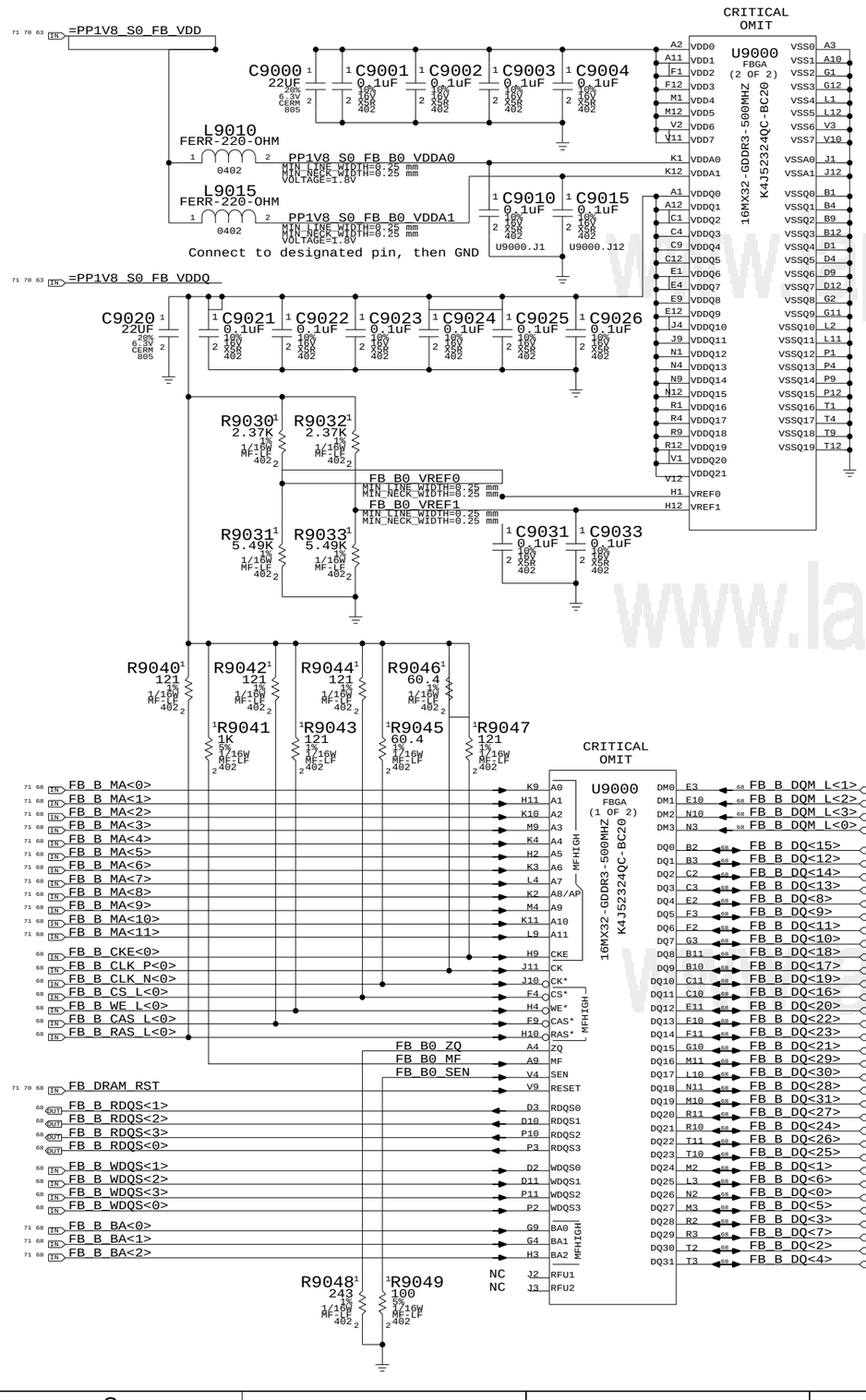
D	051-7155	A
SCALE: NONE	SHT 89 OF 104	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

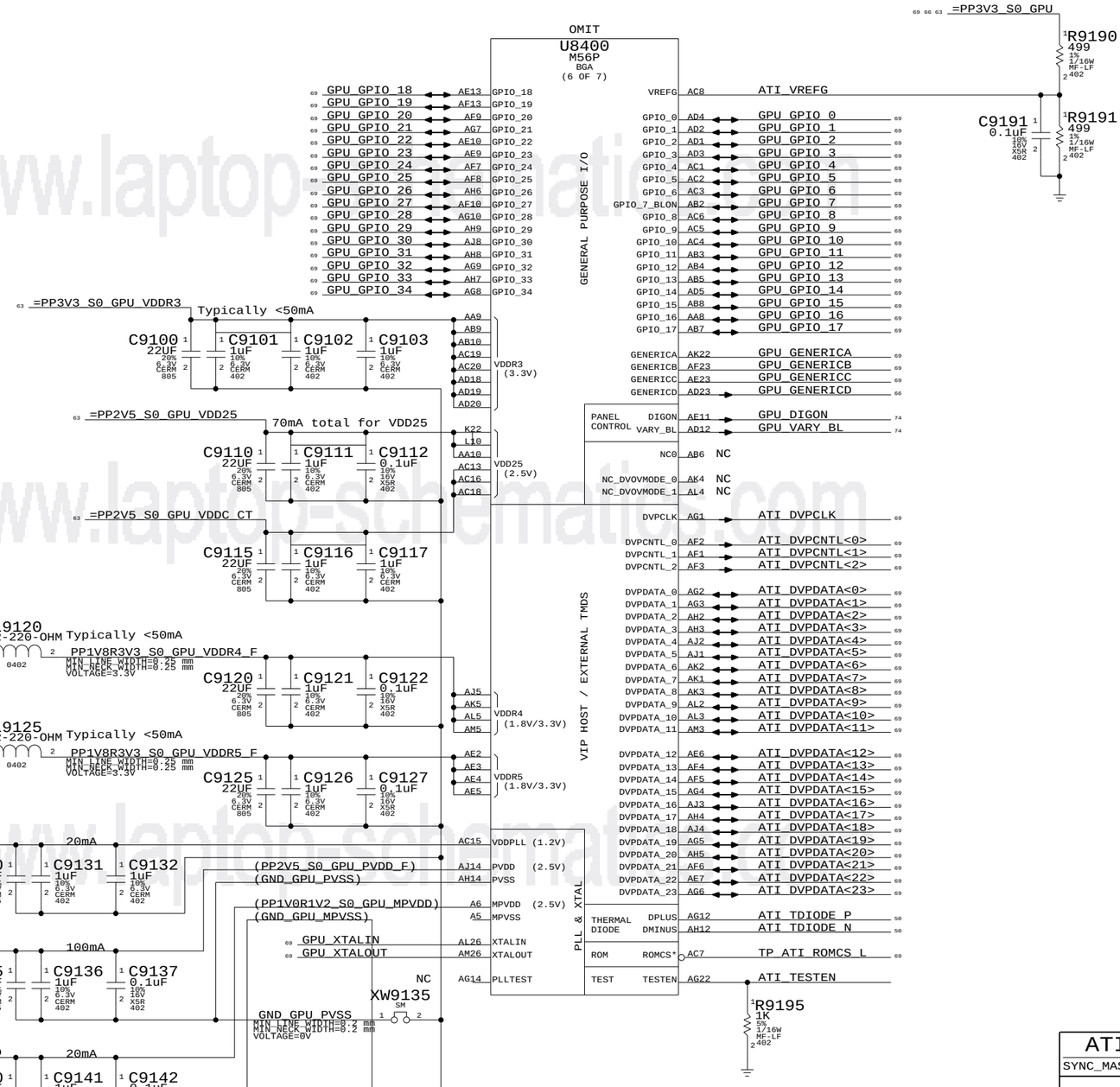
SIZE	DRAWING NUMBER	REV.
D	051-7155	A
SCALE: NONE	SHT 90 OF 104	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7155	A
	SCALE NONE	SHT 91 OF 104	

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

63 =PP2V5_S0_GPU

Sum of peak currents on this page: 605mA

L9300 FERR-220-OHM 0402 — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9300 SM — GND_GPU_TPVSS — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V
C9300 22UF 20% 6.3V CERM 805; C9301 1uF 10% 6.3V CERM 402; C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 150mA peak
XW9305 SM — GND_GPU_TXVSSR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9305 22UF 20% 6.3V CERM 805; C9306 1uF 10% 6.3V CERM 402; C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 65mA peak
XW9310 SM — GND_GPU_AVSSN — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9310 22UF 20% 6.3V CERM 805; C9311 1uF 10% 6.3V CERM 402; C9312 0.1uF 10% 16V X5R 402

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9314 SM — GND_GPU_AVSSQ — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9315 22UF 20% 6.3V CERM 805; C9316 1uF 10% 6.3V CERM 402; C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 130mA peak
XW9320 SM — GND_GPU_A2VSSN — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9320 22UF 20% 6.3V CERM 805; C9321 1uF 10% 6.3V CERM 402; C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V
XW9324 SM — GND_GPU_A2VSSQ — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V — 20mA peak
C9325 22UF 20% 6.3V CERM 805; C9326 1uF 10% 6.3V CERM 402; C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9330 SM — GND_GPU_LPVSS — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V
C9330 22UF 20% 6.3V CERM 805; C9331 1uF 10% 6.3V CERM 402; C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 200mA peak
XW9345 SM — GND_GPU_LVSSR — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9340 22UF 20% 6.3V CERM 805; C9345 22UF 20% 6.3V CERM 805; C9341 1uF 10% 6.3V CERM 402; C9342 0.1uF 10% 16V X5R 402; C9346 0.1uF 10% 16V X5R 402; C9347 0.1uF 10% 16V X5R 402

ATI_RSET 73
ATI_R2SET 73
R9350 499 1% 1/16W MF-LF 402
R9351 715 1% 1/16W MF-LF 402

OMIT
U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
AM8 TPVDD (2.5V)
AL8 TPVSS
AJ6, AK6, AL6, AM6 TXVDDR (2.5V)
AJ7, AK7, AK8, AL7, AM7 TXVSSR

DAC (CRT)
AL25, AM25 AVDD (2.5V)
AJ24, AK25 AVSS
AK23 AVSSQ
AM23 VDD1DI (2.5V)
AL23 VSS1DI
AL22 RSET ← ATI_RSET

DAC2 (TV/CRT2)
AL16, AM16 A2VDD (2.5V)
AL17, AM17 A2VSS
NC AL14 NC_A2VDDQ
AK13 A2VSSQ
AJ16 VDD2DI (2.5V)
AJ17 VSS2DI
AK14 R2SET ← ATI_R2SET

LVDS
AE19 LPVDD (2.5V)
AE18 LPVSS
AC21, AC22, AD21, AD22, AE20, AE21, AE22, AF19, AF20 LVDDR (2.5V)
AF17, AF18, AF21, AF22, AG17, AG19, AH17, AH19, AJ19, AK17 LVSSR

MONITOR IDENTIFICATION
AF11 HPD1 ← GPU_HPD 75 IN

TMDS outputs:
TXCP AM9 — GPU_TMDS_CLK_P
TXCM AL9 — GPU_TMDS_CLK_N
TX0P AL10 — GPU_TMDS_DATA_P<0>
TX0M AK10 — GPU_TMDS_DATA_N<0>
TX1P AM11 — GPU_TMDS_DATA_P<1>
TX1M AL11 — GPU_TMDS_DATA_N<1>
TX2P AM12 — GPU_TMDS_DATA_P<2>
TX2M AL12 — GPU_TMDS_DATA_N<2>
TX3P AJ9 — GPU_TMDS_DATA_P<3>
TX3M AK9 — GPU_TMDS_DATA_N<3>
TX4P AJ11 — GPU_TMDS_DATA_P<4>
TX4M AK11 — GPU_TMDS_DATA_N<4>
TX5P AJ12 — GPU_TMDS_DATA_P<5>
TX5M AK12 — GPU_TMDS_DATA_N<5>

VGA outputs:
R AK24 — GPU_VGA_R
G AM24 — GPU_VGA_G
B AL24 — GPU_VGA_B
HSYNC AJ23 — GPU_VGA_HSYNC
VSYNC AJ22 — GPU_VGA_VSYNC

TV outputs:
R2 AK15 — GPU_R2
G2 AM15 — GPU_G2
B2 AL15 — GPU_B2
H2SYNC AE15 — GPU_H2SYNC
V2SYNC AG15 — GPU_V2SYNC
Y AJ15 — GPU_TV_Y
C AJ13 — GPU_TV_C
COMP AH15 — GPU_TV_COMP

LVDS outputs:
TXCLK_UP AJ21 — GPU_LVDS_U_CLK_P
TXCLK_UN AK21 — GPU_LVDS_U_CLK_N
TXOUT_U0P AG18 — GPU_LVDS_U_DATA_P<0>
TXOUT_U0N AH18 — GPU_LVDS_U_DATA_N<0>
TXOUT_U1P AK20 — GPU_LVDS_U_DATA_P<1>
TXOUT_U1N AJ20 — GPU_LVDS_U_DATA_N<1>
TXOUT_U2P AG20 — GPU_LVDS_U_DATA_P<2>
TXOUT_U2N AH20 — GPU_LVDS_U_DATA_N<2>
TXOUT_U3P AH21 — GPU_LVDS_U_DATA_P<3>
TXOUT_U3N AG21 — GPU_LVDS_U_DATA_N<3>
TXCLK_LP AM18 — GPU_LVDS_L_CLK_P
TXCLK_LN AL18 — GPU_LVDS_L_CLK_N
TXOUT_L0P AL19 — GPU_LVDS_L_DATA_P<0>
TXOUT_L0N AK19 — GPU_LVDS_L_DATA_N<0>
TXOUT_L1P AM20 — GPU_LVDS_L_DATA_P<1>
TXOUT_L1N AL20 — GPU_LVDS_L_DATA_N<1>
TXOUT_L2P AM21 — GPU_LVDS_L_DATA_P<2>
TXOUT_L2N AL21 — GPU_LVDS_L_DATA_N<2>
TXOUT_L3P AJ18 — GPU_LVDS_L_DATA_P<3>
TXOUT_L3N AK18 — GPU_LVDS_L_DATA_N<3>

DDC outputs:
DDC1CLK AH23 — GPU_DDC_A_CLK
DDC1DATA AH22 — GPU_DDC_A_DATA
DDC2CLK AG13 — GPU_DDC_B_CLK
DDC2DATA AH13 — GPU_DDC_B_DATA
DDC3CLK AF12 — GPU_DDC_C_CLK
DDC3DATA AE12 — GPU_DDC_C_DATA

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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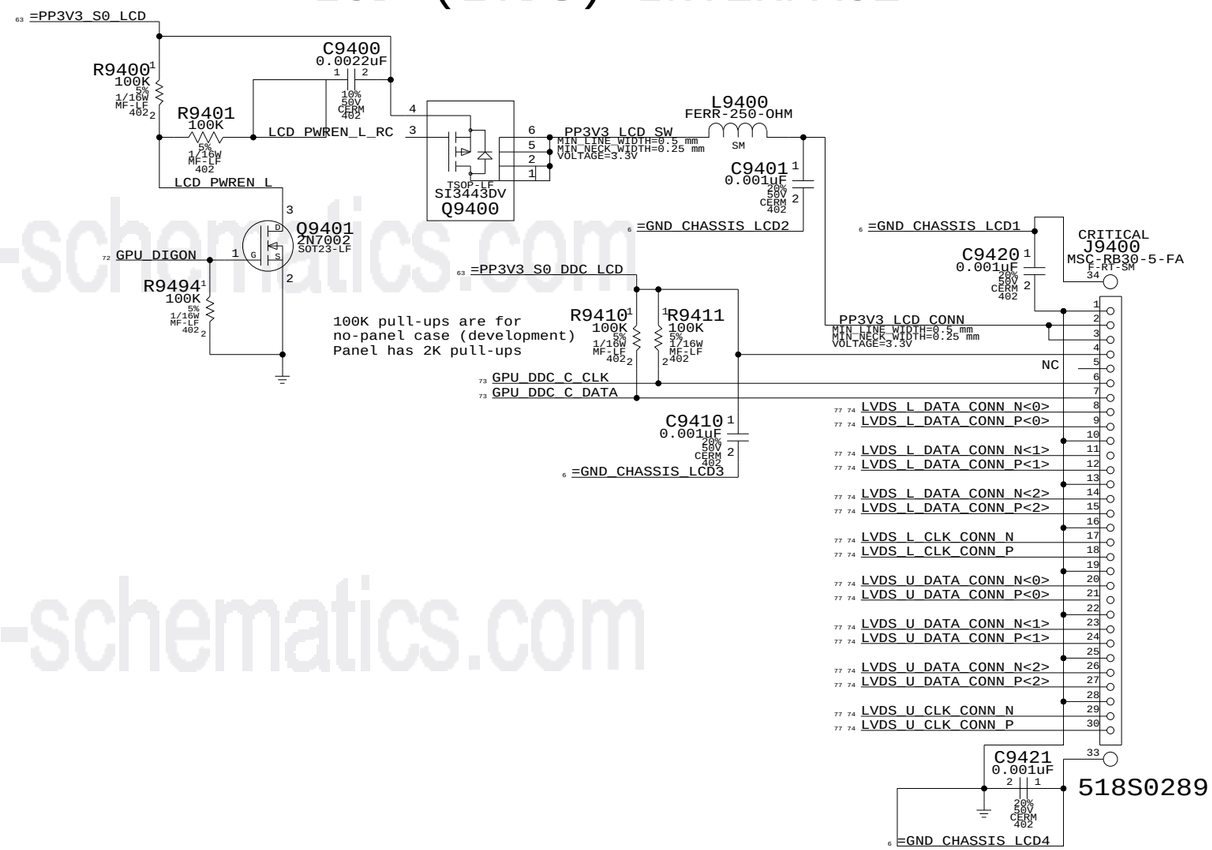
D	051-7155	A

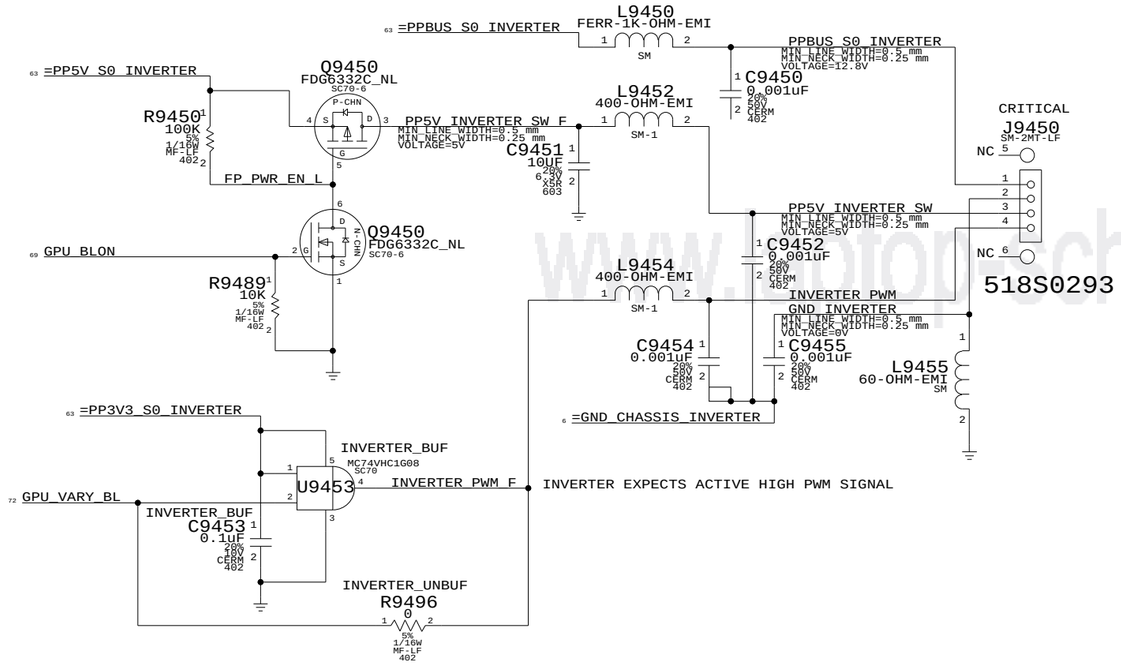
SCALE: NONE SHT 93 OF 104

LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
	VGA	VGA	GPU_R2	73 75
	VGA	VGA	GPU_G2	73 75
	VGA	VGA	GPU_B2	73 75
	LVDS	LVDS	LVDS_U_CLK_P	73 77
	LVDS	LVDS	LVDS_U_CLK_N	73 77
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	73 77
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	73 77
	LVDS	LVDS	LVDS_L_CLK_P	73 77
	LVDS	LVDS	LVDS_L_CLK_N	73 77
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	73 77
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	73 77
	LVDS	LVDS	LVDS_U_CLK_CONN_P	74 77
	LVDS	LVDS	LVDS_U_CLK_CONN_N	74 77
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>	74 77
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>	74 77
	LVDS	LVDS	LVDS_L_CLK_CONN_P	74 77
	LVDS	LVDS	LVDS_L_CLK_CONN_N	74 77
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>	74 77
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>	74 77
	TMDS	TMDS	TMDS_CLK_P	73 75 82
	TMDS	TMDS	TMDS_CLK_N	73 75 82
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 75 82
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 75 82
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 75 82
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 75 82



INVERTER INTERFACE



Internal Display Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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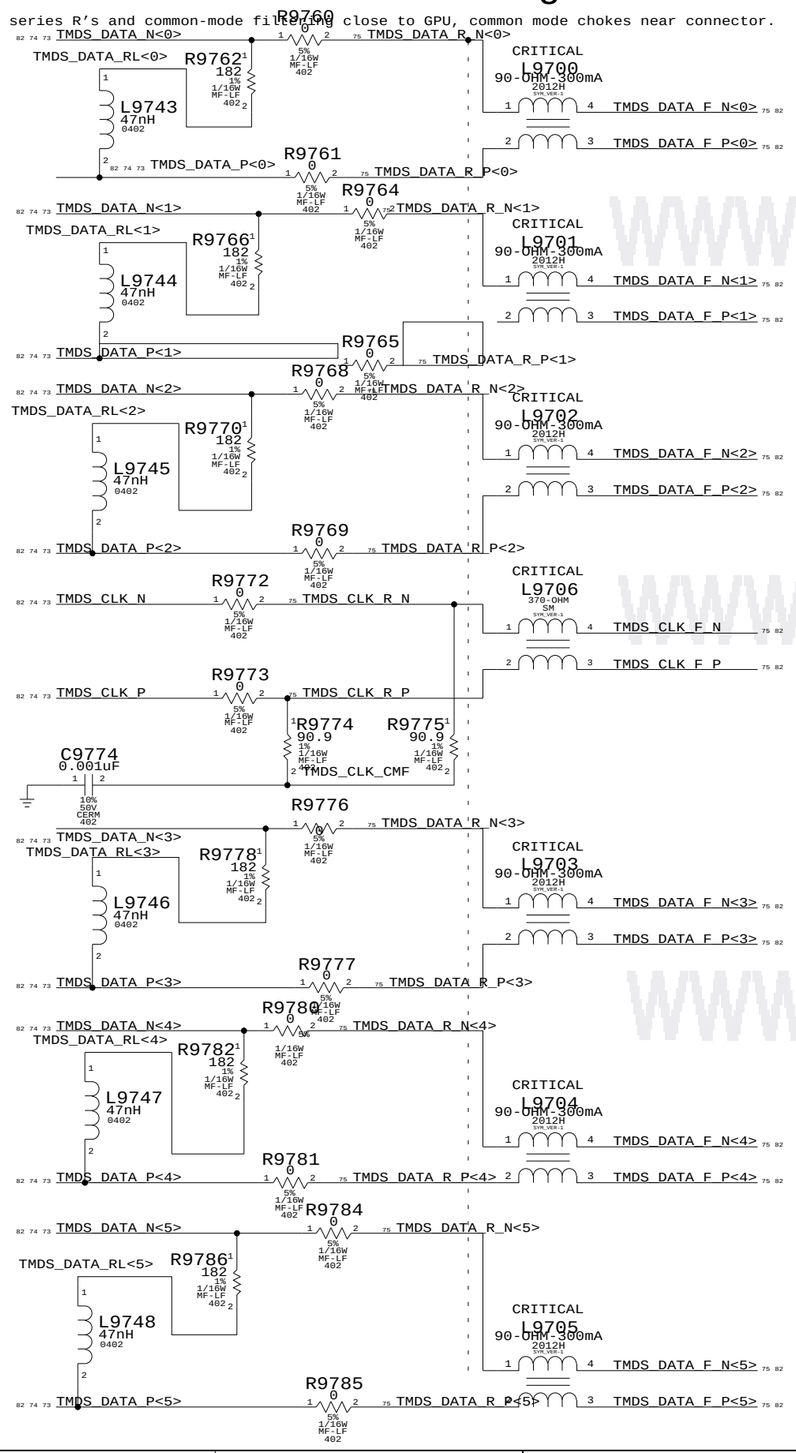
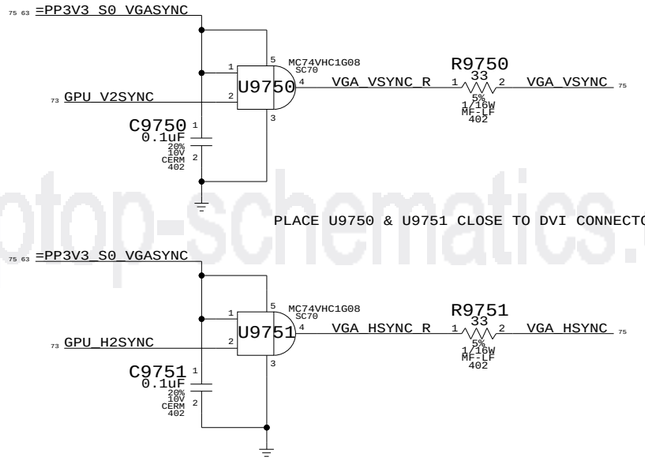
SCALE: NONE	SHT 94 OF 104	

TMDS Filtering

Place series R's and common-mode filtering close to GPU, common mode chokes near connector.



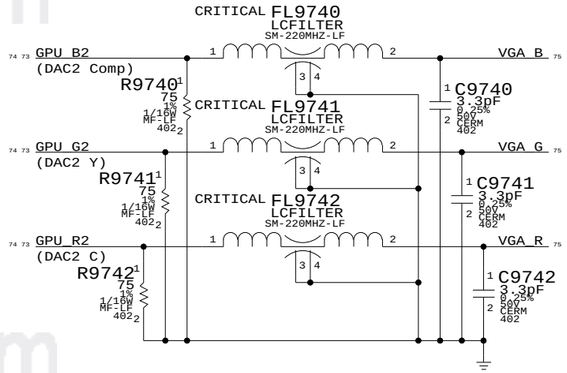
VGA SYNC BUFFERS



NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL
	TMDS	TMDS
	TMDS	TMDS
	TMDS	TMDS
	TMDS	TMDS
	TMDSCONN	TMDSCONN
	TMDSCONN	TMDSCONN
	TMDSCONN	TMDSCONN
	TMDSCONN	TMDSCONN

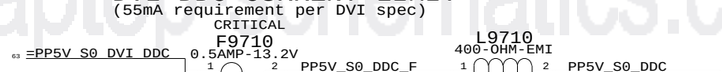
TMDS_CLK_R_P
TMDS_CLK_R_N
TMDS_DATA_R_P<5..0>
TMDS_DATA_R_N<5..0>
TMDS_CLK_F_P
TMDS_CLK_F_N
TMDS_DATA_F_P<5..0>
TMDS_DATA_F_N<5..0>

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR



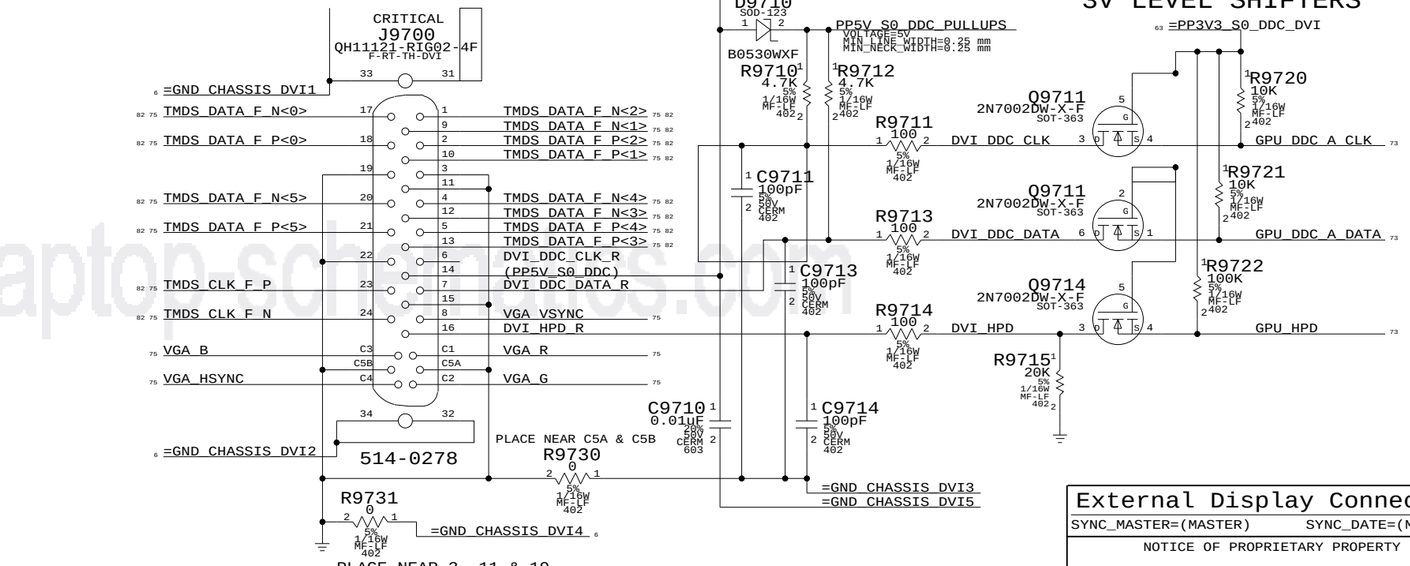
DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)



Isolation required for DVI power switch

3V LEVEL SHIFTERS



External Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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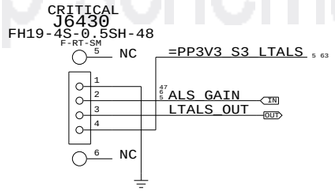
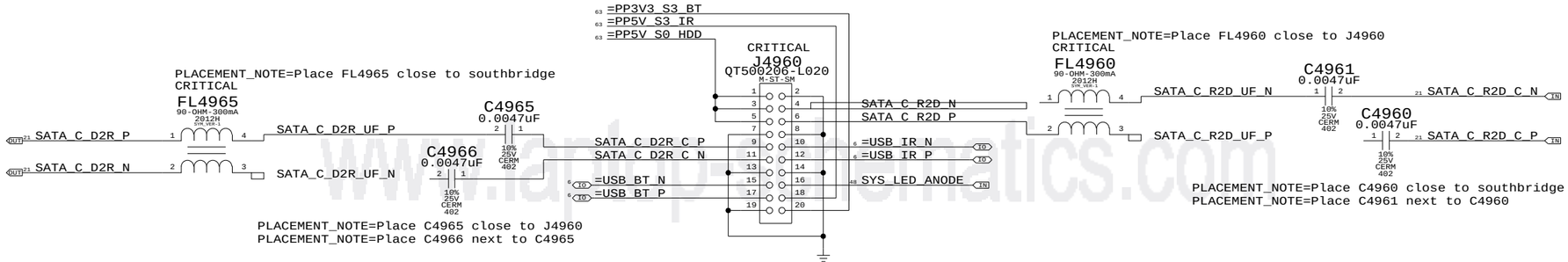
SCALE: NONE	SHT 97 OF 104	

Left ALS Connector



518S0395

Bluetooth (M13P), IR & SATA HDD Flex Connector



516S0412

NOTE: _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

M1 Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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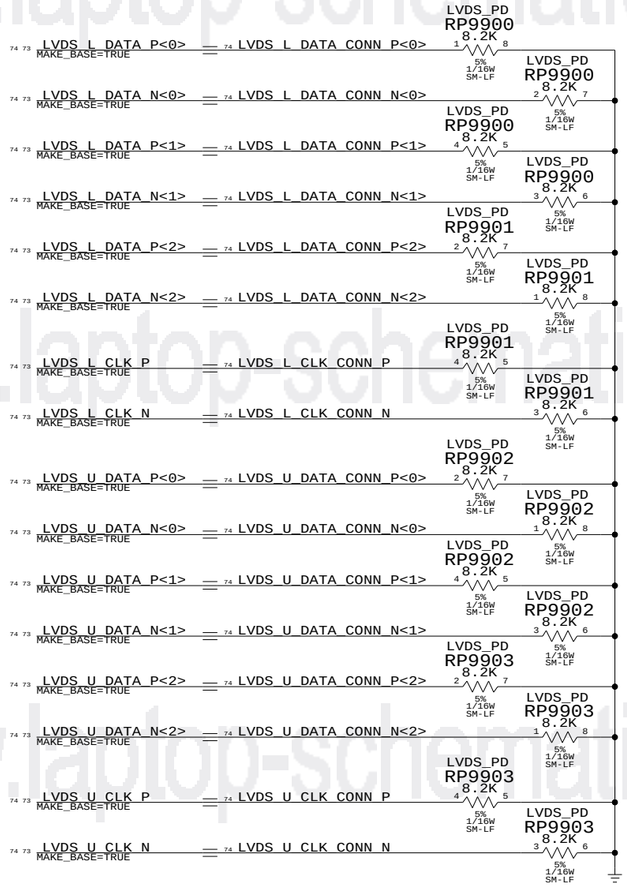
LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



LVDS Interface Pull-downs

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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D	051-7155	A
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Date - Radar # - Description

DMS Release #03000 (RFA #394758)

2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part.
2005/08/12 - 4231030 - Changed pinout of J4960, added placement notes.

Changes from Proto Branch (DMS Release #04000):

2005/08/27 - 4230219 - Changed Y3301 to non-obsoleted part.
2005/08/27 - 4235208 - Changed value of R7707 to fix 2.5V S3 supply.
2005/08/27 - 4235213 - Changed R8305, R8310, R8315 to slow down FET RCs.
2005/08/27 - 4235401 - Moved a few pins at LIO BTB connector.
2005/08/27 - 4227325 - Removed S0 option for camera, now S3-only.
2005/08/27 - 4227369 - Removed SMC options for display/backlight, now GPU-only.
2005/08/27 - 4225433 - Changed PBUS voltage sense circuit.
2005/08/28 - 4217535 - Added Left ALS FFC connector.
2005/08/28 - 4232563 - Changed analog video from Y/C/Comp to G2/R2/B2.
2005/08/28 - 4235203 - Changed BOM settings to stuff R2251.
2005/08/28 - 4217524 - Added LEFT ALS connector (J6430).
2005/08/28 - 4217535 - OMITs and tables to change 4-pin WTB connector parts.
2005/08/28 - 4221973 - Added pull-up for SB GPIO22 (REQ4#).
2005/08/28 - 4225369 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5.
2005/08/28 - 4225433 - Changed PBUS Voltage Sense circuit.
2005/08/28 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3.
2005/08/28 - 4235179 - OMIT and table to change 8-pin DC-In connector to 6-pin.
2005/08/28 - 4235179 - Changed PBUS net names to merge PBUS A & PBUS B.
2005/08/28 - 4232715 - Added FireWire ISense resistor, changed INA193 to INA194.
2005/08/28 - 4235217 - Added RC on Q3820 gate to slow down ODD FET turn-on.
2005/08/28 - 4225369 - OMITs and tables for staged LeMenu BOM approach.
2005/08/28 - 4227323 - Repinned Top-Case Flex connector.

DMS Checkin #04001

2005/08/29 - 4235179 - Changed J8200 to proper 6-pin part.
2005/08/29 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs.
2005/08/29 - 4217524 - Changed R6430 from 4.5K to 3.5K.
2005/08/29 - 4237119 - Changed LIO 5V S3 to 5V S5.
2005/08/29 - 4225369 - Changed 3.3V S5 sequence to follow 5V S5 PGOOD.
2005/08/29 - 4227336 - Changed Y5920 to 197S0169.
2005/08/29 - 4227309 - Resolved sync issues with M38 (SB page 21).
2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22).
2005/08/29 - 4227312 - Resolved sync issues with M38 (SB page 23).
2005/08/29 - 4227322 - Sync page 44 with M42 to fix FW power net S-states.
2005/08/29 - 4227332 - Resolved sync issues with M38 (SMC page 58).
2005/08/29 - 4227335 - Changed U5900 to resolve ROHS issue.

DMS Checkin #04002

2005/08/30 - 4225433 - Fixed voltage divider values in PBUS VSense circuit.
2005/08/30 - 4217535 - Removed BOM tables and OMITs for new 4-pin WTB connector.
2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint.
2005/08/31 - 4227328 - Added ESD protection diode on right USB port.
2005/08/31 - 4223808 - Various power supply R/C updates, plus some R/C adds.
2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K.
2005/08/31 - 4237025 - Added R8824 and R8827 for GPU memory configuration straps.

DMS Checkin #04003

2005/08/31 - 4240157 - Corrected pinout at SATA/BT conn (J4960) to match flex.
2005/08/31 - 4240150 - Swapped PCIE Mini Card R2D/D2R connections at J5500.
2005/08/31 - 4232563 - Corrected net properties on R2/G2/B2 nets.
2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.
2005/08/31 - 4240300 - Changed C6455 to a smaller part for cost & MCO.
2005/08/31 - 4240486 - Power line width & neck reductions at PCB request.
2005/08/31 - 4240257 - Swapped some top & bottom EMC connections at DVI connector.

DMS Checkin #04004

2005/08/31 - 4227328 - Changed EMI caps from 50V to 16V to fid in ESD protection.

DMS Checkin #04005

2005/09/02 - 4241087 - Fixed pinout of USB D+/D- at camera connector to match FHB.
2005/09/02 - 4243269 - Inverted GPU VCore control, adjusted supply R values.
2005/09/02 - 4244019 - Moved GPU-related power alias from PP3V3_S0 to PP3V3_S0_GPU.
2005/09/02 - 4240486 - Adjusted line/neck widths, changed J4931 to 518S0371.

DMS Checkin #04006

2005/09/03 - 4232534 - Fixed documentation of battery address on I2C page.
2005/09/03 - 4244484 - Changed P1V5S0_RUNSS circuit to work properly in G3Hot.
2005/09/03 - 4244539 - Added GPUVCORE_PGOOD to 1.2V, 1.8V, & 2.5V S0 sequence.
2005/09/03 - 4227315 - Changed SMBus pull-ups to 4.7K.
2005/09/03 - 4232534 - Added notes for power supplies and connectors.

DMS Checkin #04007

2005/09/06 - 4240486 - Removed NO_TEST property from GPU HSYNC and VSYNC.
2005/09/06 - 4246683 - Removed NO STUFF option from R8805 per ATI request.
2005/09/06 - 4232534 - Fixed label BOM tables to call out proper EEE #'s.

DMS Release #05000-07000 (Proto 2 releases)

2005/09/08 - 4247941 - Net property & name changes to support PCB/ICT requests.
2005/09/08 - 4248911 - Sync with M38 & M42.
2005/09/08 - 4214493 - Combined RTC coin cell diodes into dual-diode package.
2005/09/08 - 4229560 - First implementation of Physical Security Guidelines.
2005/09/16 - 4256660 - Updated FUNC_TEST property for merged PBUS.
2005/09/16 - 4229560 - Changed FW PCI REQ/GNT pair for Physical Security.
2005/09/19 - 4247941 - GND line/neck/voltage properties updated per PCB request.
2005/09/19 - 4235898 - Moved signal alias to improve schematic reuse.
2005/09/20 - 4214847 - Updated L1970 (old part no longer exists in library).
2005/09/21 - 4227306 - Changed CPU VCore caps to proper production part number.
2005/09/21 - 4234952 - Replaced FDG6324L parts with FDG6332C for cost & supply.
2005/09/26 - 4239505 - Updated J4200 (old part no longer exists in library).
2005/09/26 - 4274915 - Thermal sensor BOM updates from Proto 2 MLB branch.
2005/09/26 - 4274915 - U6301 part number updated to M1 development BootROM.

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DMS Checkin #07001

2005/09/28 - 4221965 - Added 2.2uF caps on SO-DIMM VREF pins.
2005/09/28 - 4278828 - Adjusted P5VS5_PGOOD R's, added cap on PM_RSMRST_L.
2005/09/29 - 4232826 - Swapped Vtt RPAK functions to free up unnecessary part.
2005/09/30 - 4261313 - Added placeholder connector for IR FFC connector.
2005/09/30 - 4282162 - Changed GPU BBN supply to MAX1673.
2005/09/30 - 4248911 - Sync with M38 & M42.
2005/09/30 - 4282349 - Added CRITICAL flags to parts identified in scrub.
2005/09/30 - 4274915 - C1001 stuffing change from Proto 2 MLB branch.

DMS Checkin #07002

2005/10/04 - 4256409 - Changed fan CTL series R's to 2N7002 level-shifter.
2005/10/04 - 4261313 - Deleted placeholder connector, grew HDD connector for IR.
2005/10/04 - 4281394 - BOM option change to stuff right USB ESD protection part.
2005/10/06 - 4227330 - Added ESD protection on top-case USB port.
2005/10/07 - 4286888 - BOM restructuring per EVT build plan.
2005/10/07 - 4292633 - Changed IMVP6 10K NTC from 10% to 5% part.
2005/10/07 - 4248911 - Sync with M38 & M42.

DMS Checkin #07003

2005/10/08 - 4214493 - Simplified FireWire port power circuit for BOM consolidation.
2005/10/08 - 4293072 - Various BOM / connection changes at IMVP6 (CPU VCore).
2005/10/08 - 4286729 - Changed value of TPM Xtal caps.
2005/10/08 - 4290735 - Swapped trackpad & PCIe Mini Card USB connections.
2005/10/09 - 4235898 - Part moves & refdes changes to support sync with M9.
2005/10/09 - 4214494 - Changed GPU VCore supply enable to use 1.2V/2.5V S3 PGOODs.
2005/10/09 - 4272237 - Changed 2.5V S0 FET RC to 100K to slow down turn-on.

DMS Checkin #07004

2005/10/10 - 4232826 - Swapped Vtt RPAK functions to optimize layout.
2005/10/10 - 4247941 - Net property updates found via back-annotation.

DMS Checkin #07005

2005/10/10 - 4229560 - Removed Physical Security circuitry.
2005/10/10 - 4214493 - Cost reductions to GPU power supply circuitry.
2005/10/10 - 4214847 - Changed 0-ohm resistor to solder jumper.
2005/10/10 - 4248911 - Sync with M38 & M42.
2005/10/10 - 4295280 - Changed sleep LED connection per new SMC ERS.

DMS Checkin #07006

2005/10/11 - 4261313 - Updated SATA connector pinout to match latest flex.
2005/10/11 - 4227308 - Deleted unnecessary MCH TVDAC filtering.
2005/10/11 - 4229560 - Changed SB GNT3#/GNT4# back to test points.
2005/10/12 - 4248911 - Sync with M38 & M42.
2005/10/12 - 4298899 - Changed stuffing option to disable PLT_RST gating.
2005/10/12 - 4297684 - Split FW323 VSSA from VSS to reduce noise.
2005/10/12 - 4223808 - Power supply changes per vendor feedback.
2005/10/12 - 4227320 - Updated SB pin name for GPIO 5 (ODD_PWR_EN_L).
2005/10/12 - 4244539 - Retasked FET to control 3.3V S0 FET from GPU VCore PGOOD.
2005/10/12 - 4247941 - Added properties to resolve a PCB constraint issue.
2005/10/12 - 4214493 - Consolidated 0.22uF caps in design.
2005/10/12 - 4298905 - Changed ethernet VMAIN_AVLBL connection.
2005/10/12 - 4298943 - Replaced last remaining non-RoHS compliant connector.
2005/10/12 - 4214494 - Implemented circuit to power down ethernet in S3 on battery.

DMS Checkin #07007

2005/10/13 - 4247941 - Swapped pins at trackpad ESD protection diode.

DMS Checkin #07008

2005/10/13 - 4247941 - Unswapped pins at trackpad ESD protection diode.

DMS Checkin #07009

2005/10/13 - 4247941 - Removed NO_TEST properties from CPU FSB strobe signals.
2005/10/13 - 4247941 - Spacing/Physical rule updates to match latest board database.
2005/10/14 - 4247941 - Restored NO_TEST properties, added EXPOSED_VIA properties.
2005/10/17 - 4292633 - Changed remaining 10K NTCs to new 5% part.
2005/10/17 - 4304248 - Updated GPU VCore / BBP voltages for B13/B24 support.

DMS Release #08000-11000 (EVT releases)

2005/10/20 - 4310267 - Synced 4 pages from mlb_evt branch back to trunk.
2005/10/21 - 4310267 - Synced 3 pages from mlb_evt branch back to trunk.
2005/10/21 - 4235898 - Synced 2 pages from m9/mlb.
2005/10/26 - 4310267 - Synced 4 pages from mlb_evt branch back to trunk.
2005/11/03 - 4310267 - Synced 6 pages from mlb_evt branch back to trunk.
2005/11/15 - 4310267 - Synced 5 pages from mlb_evt branch back to trunk.
2005/11/15 - 4298899 - Removed unused platform reset gate.
2005/11/15 - 4322537 - Updated thru-hole SO-DIMM connector part number.
2005/11/16 - 4345498 - Updated Ethernet & FireWire crystal part numbers.
2005/11/16 - 4235898 - Aliased connection to ALS_GAIN to support M9 request.
2005/11/16 - 4235898 - Changed Yukon power rail neck widths per M9 request.
2005/11/16 - 4227333 - Updated SMC net names per ERS v1.2.1.
2005/11/16 - 4345921 - FUNC_TEST updates per test team request.
2005/11/16 - 4346006 - Updated J5500 pinout to match updated LIO board pinout.
2005/11/16 - 4343202 - Changed USB overcurrent switch to TPS2051B, added OC* RC.
2005/11/16 - 4346184 - Inserted common-mode chokes on SATA R2D/D2R pairs.

DMS Checkin #11001

2005/11/16 - 4235898 - Sync with M38 & M42.
(11.1.0) 2005/11/16 - 4298899 - Fixed ethernet reset net name on page 26.
(11.2.0) 2005/11/16 - 4227333 - Fixed single-pin nets caused by SMC net name updates.
2005/11/18 - 4235898 - Changed R4210 package size per M9 request.
(11.3.0) 2005/11/18 - 4235898 - Changed C9710 GND connection per M9 request.
2005/11/19 - 4346184 - Fixed location of SATA R2D common-mode choke.
2005/11/19 - 4347717 - Changed SMS self-test pull-up to pull-down.
2005/11/19 - 4350840 - Simplified TMDS filtering to allow movement of filter.
2005/11/19 - 4229560 - Changed FW chip back to REQ/GNT3.
2005/11/19 - 4350849 - Added option to connect SB_GPIO30 to ENET_LOM_DIS_L.
2005/11/19 - 4340256 - Changed topcase flex trackpad power from 3.3V to 5V.
(11.4.0) 2005/11/19 - 4292165 - Refreshed schematic symbol for U3750 (library update).

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DMS Checkin #11002

2005/11/21 - 4351196 - Added 1K pull-down on IDE_RESET_L.
(11.5.0) 2005/11/21 - 4343202 - Changed RC value and net name for USB OC.
2005/11/22 - 4350840 - Swapped TMDS termination components for placement.
(11.6.0) 2005/11/22 - 4352020 - Changed 2.5V S3 supply inductor & compensation values.
(11.7.0) 2005/11/28 - 4347845 - Added pull-down resistors on LVDS interface.
2005/11/30 - 4227340 - Removed CPU VCore current sense input RC.
2005/11/30 - 4331670 - Added CRITICAL flags to some more parts.
2005/11/30 - 4343864 - Added EMI/ESD parts at camera connector.
2005/11/30 - 4351181 - Changed ITP connector BOM option.
2005/11/30 - 4351196 - Changed IDE_RESET_L pull-down from 1K to 15K.
2005/11/30 - 4358831 - Added pull-downs on two SB-to-SMC signals.
2005/12/01 - 4362404 - Changed TMDS diff term from 100-ohm to 180-ohm.
2005/12/01 - 4352020 - Changed 2.5V supply inductor to RoHS-compliant part.
2005/12/01 - 4227340 - Changed supply for 1.8V S3 current sense amp.
2005/12/01 - 4362566 - Restructured BOM for thick/thin PCB versions.
2005/12/01 - 4347845 - RPAK pinswaps to LVDS pull-downs for PCB layout.

DMS Checkin #11003

2005/12/02 - 4256256 - Added BOMOPTION to R8801 to allow per-project control.
2005/12/02 - 4363848 - Removed M56 GPU die rev B13 support from BOM.
2005/12/02 - 4363870 - Removed M1a support from BOM.
2005/12/02 - 4217524 - Updated part number for J6430.

DMS Release #12000-13000 (DVT releases)

2005/12/07 - 4375840 - Synced 4 pages from mlb_dvt branch back to trunk.
2005/12/12 - 4235898 - Changes to LVDS net names to support mux option.
2005/12/12 - 4362451 - Added MAKE_BASE=TRUE to SMC 32KHz SUSCLK net.
2006/01/03 - 4375840 - Synced 1 page from mlb_dvt branch back to trunk.
2006/01/03 - 4290282 - Removed BOM table, changed L9455 to 155S0002.
2006/01/03 - 4347845 - Changed LVDS pull-downs from 10K to 8.2K.
2006/01/03 - 4391436 - Swapped N/P signal names on one portion of SATA_R2D.
2006/01/03 - 4362451 - Changed SCH/PCB/BOM part descriptions for Rev A.
2006/01/03 - 4362451 - Removed power jumpers and 0-ohm resistor.
2006/01/05 - 4362566 - Removed 920- number for thin PCB option.
2006/01/05 - 4394079 - Added BOMOPTION to SYS_ONEWIRE pull-up.
2006/01/05 - 4362451 - Removed power jumpers and 0-ohm resistor.
2006/01/05 - 4362451 - Restructured BOM tables to eliminate LeMenu.
2006/01/06 - 4402184 - Changed R7540 value for IMVP6 load-line improvement.
2006/01/06 - 4362451 - Added System Block Diagram, updated Power Diagram.
2006/01/06 - 4362451 - Changed BOM options for production SMC, BootROM.

DMS Release #A000 (Production Release)

2006/01/09 - 4403346 - Schem P/N changed from 051-6941 to 051-7076.
2006/01/09 - 4403360 - Changed all FDC796N parts to FDM6296.
2006/01/12 - 4403360 - Changed C6222 from FDM6296 back to FDC796N.
2006/01/13 - 4403346 - Updated to newer 630- and EEE #'s.

DMS Release #01000-03000 (Post-PVT Qual Build Releases)

2006/02/07 - 4403346 - Synced 18 pages from mlb_mosfet_qual branch to trunk.
2006/02/10 - 4437189 - Changed R7757 to 1Mohm & R7770 to 100K.
(3.1.0) 2006/02/10 - 4403360 - Changed R7910 from 3.01k to 5.62k.
(3.2.0) 2006/02/13 - 4431947 - Removed NO STUFF option from C3309.
(3.3.0) 2006/02/13 - 4403346 - Changed BOM structure for 3 CPU speeds.
2006/02/14 - 4403346 - Updated part numbers for BootROM and SMC.

(A.0.0) ## DMS Release #A000 (Production Release)

2006/02/17 - 4449123 - Changed C7537: 4.7nF -> 47pF, R7537: 3.57K -> 4.42K.

(B.0.0) ## DMS Release #B000 (BOM Update)

2006/03/01 - 4457745 - Added 128S0094 & 128S0095 as alternates for 128S0060.
2006/03/01 - 4457745 - Added 128S0081 as alternate for 128S0061.

(C.0.0) ## DMS Release #C000 (BOM Update for EE Qual Build)

2006/03/20 - 4485021 - Changed R7542 from 9.31K to 11.5K for CPU VCore OCP.

(D.0.0) ## DMS Release #D000 (BOM Update)

2006/03/31 - 4498859 - Updated BOM table for screened ISL6262.

(E.0.0) ## DMS Release #E000 (BOM Update)

2006/03/31 - 4436716 - Added BOM table for ATI rev B26.
2006/04/05 - 4502903 - Reset BOM part numbers & EEE codes for B26 change.

(F.0.0) ## DMS Release #F000 (New EEE/BOM Release)

2006/04/10 - 4508528 - Replace PwrSupply MLCCs with POSCAPs for noise red.
2006/04/17 - 4517184 - New BOM/EEE numbers for new configs
2006/04/17 - 4517438 - Add 47nH 1.30hm inductors across TMDS data lines

(1.0.0) ## DMS Release #1000 (New Board and BOM Release)

2006/04/25 - 4517184 - New BOM/EEE numbers for new configs

(2.0.0) ## DMS Release #2000 (New Board and BOM Release)

(3.0.0) ## DMS Release #A000 (Production Release)

A

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE NONE SHT 100 OF 104

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	
FSB_ADDR2ADDR	*	=2:1_SPACING	
FSB_ADSTB	*	=3:1_SPACING	
FSB_ADDR2ADSTB	*	=3:1_SPACING	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	
FSB_DATA2DATA	*	=2:1_SPACING	
FSB_DSTB	*	=3:1_SPACING	
FSB_DATA2DSTB	*	=3:1_SPACING	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	
CPU_COMP	*	25 MIL	
CPU_GTLREF	*	25 MIL	
CPU_ITP	*	=2:1_SPACING	
CPU_VCCSENSE	*	25 MIL	

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	
MEM_CTRL2CTRL	*	=2:1_SPACING	
MEM_CTRL2MEM	*	=3:1_SPACING	
MEM_CMD2CMD	*	=1.5:1_SPACING	
MEM_CMD2MEM	*	=3:1_SPACING	
MEM_DATA2DATA	*	=1.5:1_SPACING	
MEM_DATA2MEM	*	=3:1_SPACING	
MEM_DQS2MEM	*	=3:1_SPACING	
MEM_2OTHER	*	25 MIL	

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	
DMI	*	20 MIL	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	
SATA	*	20 MIL	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	
USB2_2CLK	*	25 MIL	

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	
SPI	*	=1.8:1_SPACING	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	
CLK_PCIE	*	20 MIL	
CLK_MED	*	20 MIL	
CLK_SLOW	*	10 MIL	

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE	SHT	OF
NONE	101	104

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	
FB_CLK	*	=2.5:1_SPACING	
FB_DATA	*	=2.5:1_SPACING	

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	=3:1_SPACING	
TMDS	*	=3:1_SPACING	
VGA	*	15 MIL	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS_PAIR2PAIR	*	25 MIL	
TMDS_PAIR2PAIR	*	25 MIL	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET	*	=3:1_SPACING	
FW	*	=3:1_SPACING	

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	

More System Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE: NONE

SHT 102 OF 104

M1 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	
STANDARD	*	=DEFAULT	
BGA_P1MM	*	=DEFAULT	
BGA_P2MM	*	=DEFAULT	
BGA_P3MM	*	=DEFAULT	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	
1.8:1_SPACING	*	0.18 MM	
2:1_SPACING	*	0.2 MM	
2.5:1_SPACING	*	0.25 MM	
3:1_SPACING	*	0.3 MM	
4:1_SPACING	*	0.4 MM	

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2,ISL11	0.1 MM	
1.8:1_SPACING	ISL2,ISL11	0.1 MM	
2:1_SPACING	ISL2,ISL11	0.1 MM	
2.5:1_SPACING	ISL2,ISL11	0.1 MM	
3:1_SPACING	ISL2,ISL11	0.1 MM	
4:1_SPACING	ISL2,ISL11	0.1 MM	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2,ISL11	0.1 MM	
CLK_PCIE	ISL2,ISL11	0.1 MM	
CLK_MED	ISL2,ISL11	0.1 MM	
CLK_SLOW	ISL2,ISL11	0.1 MM	
CPU_COMP	ISL2,ISL11	0.1 MM	
CPU_GTLREF	ISL2,ISL11	0.1 MM	
CPU_VCCSENSE	ISL2,ISL11	0.1 MM	
DMI	ISL2,ISL11	0.1 MM	
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	
MEM_2OTHER	ISL2,ISL11	0.1 MM	
PCIE	ISL2,ISL11	0.1 MM	
SATA	ISL2,ISL11	0.1 MM	
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	
VGA	ISL2,ISL11	0.1 MM	

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M1 Spacing & Physical Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE NONE SHT 103 OF 104

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 11 12
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	7 21
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	14 23 57
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	57
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 82
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 82
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 57
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 57
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	57
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	57

MEM_CLK	MEM_70D
MEM_CTRL	MEM_45S
MEM_CMD	MEM_55S
MEM_DATA	MEM_55S
MEM_DQS	MEM_85D
FB_CLK	FB_75D
FB_ADCTRL	FB_35S_TO_55S
FB_ADCTRL	FB_55S
FB_DATA	FB_40S
LVDS	LVDS_100D
TMDS	TMDS_100D
VGA	VGA_75S
PCIE	PCIE_100D
DMI	DMI_100D
SATA	SATA_100D
IDE	IDE_55S
USB2	USB2_90D
ENET	ENET_100D
FW	FW_110D
SMB	SMB_55S
SPI	SPI_55S
CLK_FSB	CLK_FSB_100D
CLK_PCIE	CLK_PCIE_100D
CLK_MED	CLK_MED_55S
CLK_SLOW	CLK_SLOW_55S

	AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
	AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 45
	AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
	AUDIO_55S	AUDIO	ACZ_SYNC	5 21 45
	AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
	AUDIO_55S	AUDIO	ACZ_RST_L	5 21 45
	AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 45
	AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
	AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 45

	TMDS	TMDS	TMDS_CLK_P	73 74 75
	TMDS	TMDS	TMDS_CLK_N	73 74 75
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 74 75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P	75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	75

M1 Net Properties

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7155	A

SCALE	SHT	OF
NONE	104	104