1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

SCHEM,TRUCKEE,M57

DVT2

8/16/2006

PAGE (.CSA)		CONTENTS	SYNC DATE
1	1	Table of Contents	N/A N/A
2	2	System Block Diagram	(MASTER)
3	3	Power Block Diagram	(MASTER)
4	4	BOM CONFIGURATION	(MASTER)
5	5	Functional / ICT Test	(MASTER)
6	6	Signal Aliases	(MASTER)
7	7	CPU 1 OF 2-FSB	M59_MLB 08/08/2006
8	8	CPU 2 OF 2-PWR/GND	M59_MLB 08/08/2006
9	9	CPU Decoupling & VID	M59_MLB 08/08/2006
10	10	CPU MISC1-TEMP SENSOR	M59_MLB 08/08/2006
11	11	CPU ITP700FLEX DEBUG	(MASTER)
12	12	NB CPU Interface	M59_MLB 08/08/2006
13	13	NB PEG / Video Interfaces	M59_MLB 08/08/2006
14	14	NB Misc Interfaces	M59_MLB 08/08/2006
15	15	NB DDR2 Interfaces	M59_MLB 08/08/2006
16	16	NB Power 1	M59_MLB 08/08/2006
17	17	NB Power 2	M59_MLB 08/08/2006
18	18	NB Grounds	M59_MLB 08/08/2006
19	19	NB (GM) Decoupling	M57_MLB_MG 08/08/2006
20	20	NB Config Straps	M59_MLB 08/08/2006
21	21	SB: 1 OF 4	M59_MLB 08/08/2006
22	22	SB: 2 of 4	M59_MLB 08/08/2006
23	23	SB: 3 OF 4	M57_MLB_MG 08/08/2006
24	24	SB: 4 OF 4	M59_MLB 08/08/2006
25	25	SB Decoupling	M59_MLB 08/08/2006
26	26	SB Misc	(MASTER)
27	27	M57 SMBUS CONNECTIONS	(MASTER)
28	28	DDR2 SO-DIMM Connector A	M59_MLB 08/08/2006
29	29	DDR2 SO-DIMM Connector B	M59_MLB 08/08/2006
30	30	Memory Active Termination	(MASTER)
31	31	Memory Vtt Supply	M59_MLB 08/08/2006
32	32	DDR2 VRef	M59_MLB 08/08/2006
33	33	CLOCKS	M59_MLB 08/08/2006
34	34	Clock Termination	M59_MLB 08/08/2006
35	37	Mobile Clocking	M59_MLB 08/08/2006
36	38	PATA Connector	(MASTER)
37	39	FireWire Link (TSB83AA22)	M59_MLB 08/08/2006
38	40	FireWire PHY (TSB83AA22)	M59_MLB 08/08/2006
39	41	ETHERNET CONTROLLER	M59_MLB 08/08/2006
40	42	Ethernet Connector	M59_MLB 08/08/2006
41	43	Yukon Power Control	M59_MLB 08/08/2006
42	44	FW PHY Power Supply	M59_MLB 08/08/2006
43	45	FireWire Port Power	(MASTER)
44	46	FireWire Ports	M59_MLB 06/27/2006
45	49	Camera Connector	M59_MLB 08/08/2006
46	50	Internal USB Hub	(MASTER)
47	52	External USB Connector	M59_MLB 08/08/2006
48	55	Left I/O Board Connector	(MASTER)
49	56	Current & Thermal Sensors	(MASTER)
50	57	PCI-E Connections	(MASTER)
51	58	SMC	M59_MLB 08/08/2006
52	59	SMC Support	M59_MLB 08/08/2006
53	60	LPC+ Debug Connector	(MASTER)
54	61	Thermal Sensors	M59_MLB 08/08/2006
55	62	Current & Voltage Sensing	M59_MLB 08/08/2006
56	63	SPI BOOTROM	M59_MLB 08/08/2006
57	64	ALS Support	(MASTER)
58	65	Fan Connectors	(MASTER)
59	66	Sudden Motion Sensor (SMS)	M59_MLB 08/08/2006
60	67	TPM	M59_MLB 08/08/2006
61	75	IMVP6 CPU VCore Regulator	M59_MLB 08/08/2006
62	76	5V / 1.5V Power Supply	M59_MLB 08/08/2006
63	77	2.5V & 1.2V Regulators	M59_MLB 08/08/2006
64	78	1.8V Supply	(MASTER)
65	79	3.3V / 1.05V Power Supplies	M59_MLB 08/08/2006
66	80	3.3V G3Hot Supply & Power Control	M57_MLB_MG 08/08/2006
67	81	Power Aliases	(MASTER)
68	82	DC-In & Battery Connectors	(MASTER)
69	83	PBus Supply & Batt. Charger	M59_LIO 08/08/2006
70	84	ATI M56 PCI-E	(MASTER)
71	85	GPU (M56) Core Supplies	(MASTER)
72	86	ATI M56 Core Power	(MASTER)
73	87	ATI M56 Frame Buffer I/F	(MASTER)
74	88	GPU Straps	M57_MLB_MG 08/08/2006
75	89	GDDR3 Frame Buffer A	(MASTER)
76	90	GDDR3 Frame Buffer B	(MASTER)
77	91	ATI M56 GPIO/DVO/Misc	(MASTER)
78	93	ATI M56 Video Interfaces	(MASTER)
79	94	Internal Display Connectors	M57_MLB_MG 08/08/2006
80	97	External Display Connector	M57_MLB_MG 08/08/2006
81	98	M57 SPECIFIC CONNECTORS	(MASTER)
82	99	LVDS Interface Pull-downs	M57_MLB_MG 08/08/2006
83	100	Revision History	(MASTER)
84	101	Napa Platform Constraints	(MASTER)
85	102	More System Constraints	(MASTER)
86	103	M9 Spacing & Physical Constraints	(MASTER)
87	104	M57 NET PROPERTIES	(MASTER)

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7164	1	SCHEM,TRUCKEE,M57	SCH	CRITICAL	
820-2059	1	PCBF,TRUCKEE,M57	PCB	CRITICAL	

DRAWING
TITLE=TRUCKEE
ABBREV=DRAWING
LAST_MODIFIED=Wed Aug 16 19:10:01 2006

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

NOTICE OF PROPRIETARY PROPERTY

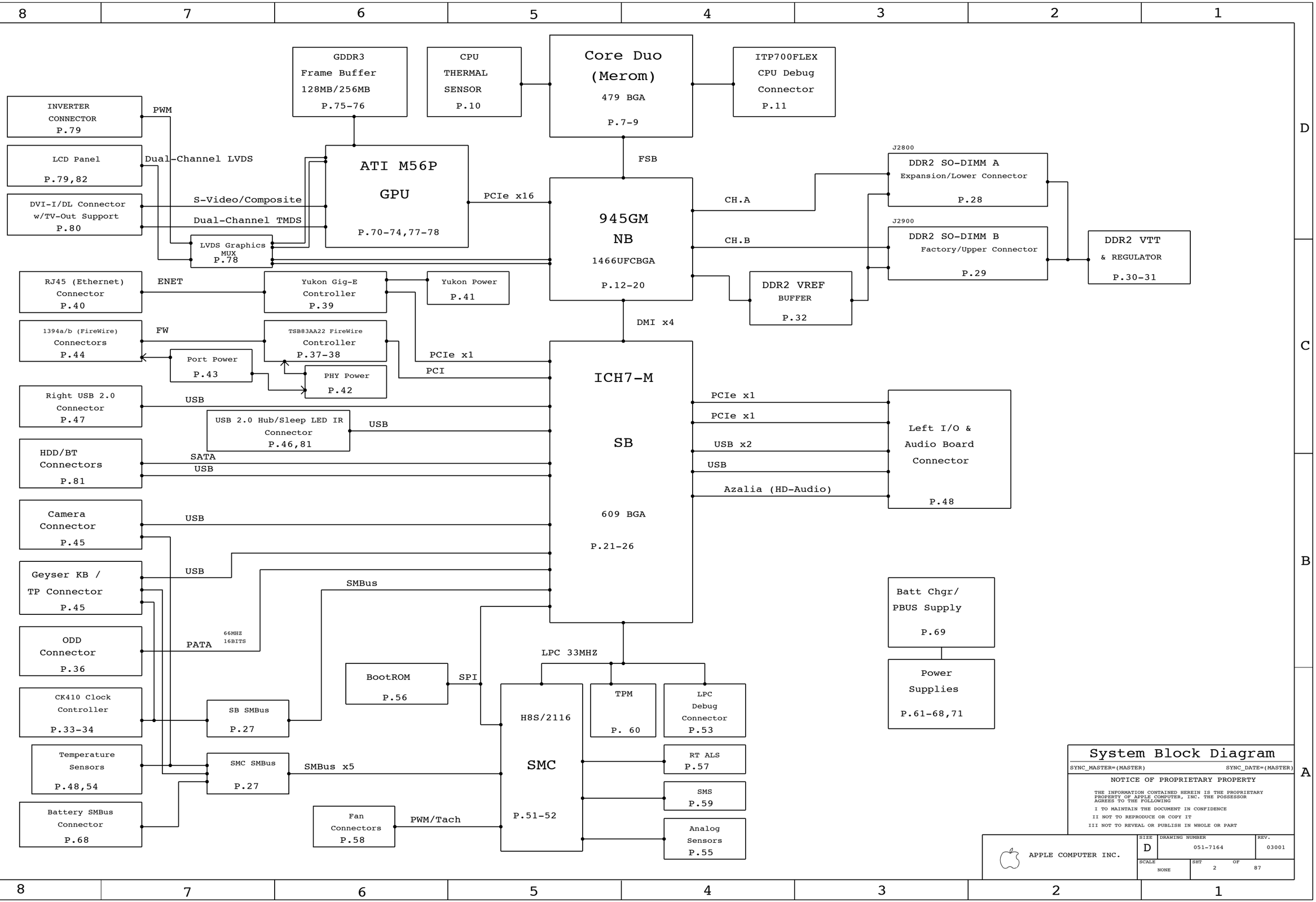
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

TITLE
SCHEM.TRUCKEE,M57

DRAWING NUMBER 051-7164 REV. 03001

SHT 1 OF 87



System Block Diagram

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

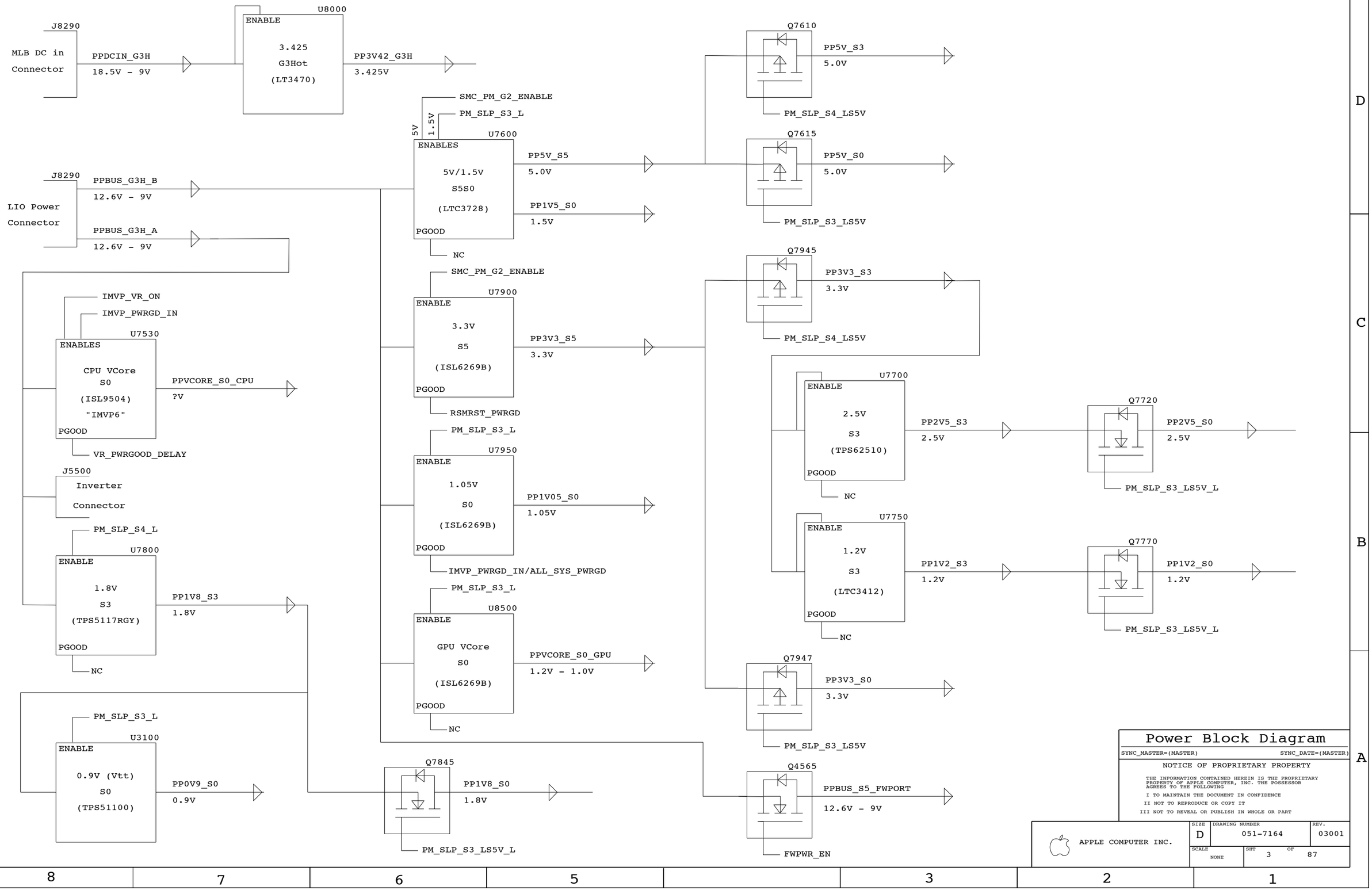
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	2	87


J8290
MLB DC in Connector
PPDCIN_G3H
18.5V - 9V
U8000
ENABLE
3.425 G3Hot (LT3470)
PP3V42_G3H
3.425V
J8290
LIO Power Connector
PPBUS_G3H_B
12.6V - 9V
PPBUS_G3H_A
12.6V - 9V
SMC_PM_G2_ENABLE
PM_SLP_S3_L
5V
1.5V
U7600
ENABLES
5V/1.5V S5S0 (LTC3728)
PGOOD
PP5V_S5
5.0V
PP1V5_S0
1.5V
NC
Q7610
PP5V_S3
5.0V
PM_SLP_S4_LS5V
Q7615
PP5V_S0
5.0V
PM_SLP_S3_LS5V
SMC_PM_G2_ENABLE
U7900
ENABLE
3.3V S5 (ISL6269B)
PGOOD
PP3V3_S5
3.3V
RSMRST_PWRGD
PM_SLP_S3_L
U7950
ENABLE
1.05V S0 (ISL6269B)
PGOOD
PP1V05_S0
1.05V
IMVP_PWRGD_IN/ALL_SYS_PWRGD
PM_SLP_S3_L
U8500
ENABLE
GPU VCore S0 (ISL6269B)
PGOOD
PPVCORE_S0_GPU
1.2V - 1.0V
NC
Q7945
PP3V3_S3
3.3V
PM_SLP_S4_LS5V
U7700
ENABLE
2.5V S3 (TPS62510)
PGOOD
PP2V5_S3
2.5V
NC
Q7720
PP2V5_S0
2.5V
PM_SLP_S3_LS5V_L
U7750
ENABLE
1.2V S3 (LTC3412)
PGOOD
PP1V2_S3
1.2V
NC
Q7770
PP1V2_S0
1.2V
PM_SLP_S3_LS5V_L
IMVP_VR_ON
IMVP_PWRGD_IN
U7530
ENABLES
CPU VCore S0 (ISL9504) "IMVP6"
PGOOD
PPVCORE_S0_CPU
?V
VR_PWRGOOD_DELAY
J5500
Inverter Connector
PM_SLP_S4_L
U7800
ENABLE
1.8V S3 (TPS5117RGY)
PGOOD
PP1V8_S3
1.8V
NC
PM_SLP_S3_L
U3100
ENABLE
0.9V (Vtt) S0 (TPS51100)
PP0V9_S0
0.9V
Q7845
PP1V8_S0
1.8V
PM_SLP_S3_LS5V_L
Q7947
PP3V3_S0
3.3V
PM_SLP_S3_LS5V
Q4565
PPBUS_S5_FWPORT
12.6V - 9V
FWPWR_EN
Power Block Diagram
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7164
REV. 03001
SCALE NONE
SHT 3 OF 87

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7813	TRUCKEE,2.16GHZ,B2,256VRAM,INF,M57	VRAM_256INF,M57_COMMON,CPU_2_16GHZ_B2,EEE_WJJ
630-7812	TRUCKEE,2.16GHZ,B2,256VRAM,SAM,M57	VRAM_256SAM,M57_COMMON,CPU_2_16GHZ_B2,EEE_WJH

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7815	TRUCKEE,2.33GHZ,B2,256VRAM,INF,M57	VRAM_256INF,M57_COMMON,CPU_2_33GHZ_B2,EEE_WJL
630-7814	TRUCKEE,2.33GHZ,B2,256VRAM,SAM,M57	VRAM_256SAM,M57_COMMON,CPU_2_33GHZ_B2,EEE_WJK

BOM GROUP	BOM OPTIONS
VRAM_128SAM	VRAM_128_SAMSUNG
VRAM_256SAM	GPU_MEM_256M,VRAM_256_SAMSUNG
VRAM_128INF	GPU_MEM_NOT_SAM,VRAM_128_INFINEON
VRAM_256INF	GPU_MEM_NOT_SAM,GPU_MEM_256M,VRAM_256_INFINEON

BOM GROUP	BOM OPTIONS
M57_COMMON	ALTERNATE,COMMON,M57_COMMON1,M57_COMMON2,M57_COMMON3,M57_COMMON4,M57_DEBUG,ISL6255A,M57_NO_3G
M57_COMMON1	ENET_LOWPWR_EN,ENETPWR_S3AC,GPU_BB_CTL
M57_COMMON2	KBDLED_HAS,MEMVREF_S3,MEMVTT_EN_PU,RTUSB_ESD,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
M57_COMMON3	LVDS_PD,FW_PORT_FAULT_PU
M57_COMMON4	BOOTROM_DEVEL,SMC_PRGRM
M57_DEBUG	ITP,ITPCONN,LPCPLUS
M57_TPM	TPM
M57_3G	3G
M57_NO_3G	NO_3G

BAR CODE LABELS / EEE #'S

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:W9J]	CRITICAL	EEE_WJJ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:W3A]	CRITICAL	EEE_WJH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:W3A]	CRITICAL	EEE_WJK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:WDV]	CRITICAL	EEE_WJL

MODULE PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0368	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX
333S0376	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_INFINEON
333S0377	4	IC,SGRAM,GDDR3,16MX32,600MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_INFINEON

ALTERNATE PARTS

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680448	37680445		ALL	SI7806ADN for FDM6296
12880083	12880073		C2516	1.86 MAX ALT TO 1.9 MAX
12880093	12880092		ALL	KEMET IS ALT TO SANYO
12880094	12880060		ALL	330UF,2V,9MOHM,D2
12880095	12880060		ALL	330UF,2V,6MOHM,D2
12880081	12880061		ALL	150UF,6.3V,25MOHM,C2
353B1465	353B1461		ALL	Screened ISL6262 for ISL9504
15280287	15280435		ALL	Alternates for Coilcraft MSS5131
15780030	15780111		ALL	Alternates for E&E Magnetics, TOK

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1931	1	IC,PRGRM,SMC(NEW),M57	U5800	CRITICAL	SMC_PRGRM
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6301	CRITICAL	BOOTROM_BLANK
341S1924	1	IC, BOOTROM, DEVELOPMENT, UNLOCKED ,M57	U6301	CRITICAL	BOOTROM_DEVEL
341S1925	1	IC, BOOTROM, FINAL, LOCKED, M57	U6301	CRITICAL	BOOTROM_FINAL
353S1461	1	IC,ISL9504,SYNC REG CTL,QFN 48	U7530	CRITICAL	
359S0109	1	IC,LOW POWER CLOCK SYNTHESIZER,68PIN	U3301	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	TPM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3391	1	IC,MDC,B2,PRQ,2.16GHZ,34W,667M,4M,479 BGA	U0700	CRITICAL	CPU_2_16GHZ_B2
337S3393	1	IC,MDC,B2,PRQ,2.33GHZ,34W,667M,4M,479 BGA	U0700	CRITICAL	CPU_2_33GHZ_B2
338S0269	1	IC,945GM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,ICH7M,BGA	U2100	CRITICAL	

Extra TPM options:
SMC_TPM_GPIO2
SMC_TPM_GPIO1
SMC_TPM_PP

BOM CONFIGURATION

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7164 | REV. 03001

SCALE NONE | SHT 4 OF 87

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	61C7
TRUE		P5VS5_RUNSS	62C5 66A6
TRUE		P1V5S0_RUNSS	62C4 66C6
TRUE		P2V5S3_MODE	
TRUE		P2V5S3_SHDNRT	
TRUE		P1V2S3_RT	63B6
TRUE		P1V2S3_RUNSS	41C4 63B7
TRUE		P1V8S3_COMP	
TRUE		P1V8S3_FSET	
TRUE		P3V3S5_COMP	65C6
TRUE		P3V3S5_FSET	65D6
TRUE		P1V05S0_COMP	65A7
TRUE		P1V05S0_FSET	65B7
TRUE		P3V42G3H_FB	64C3
TRUE		GPUVCORE_COMP	71C7
TRUE		GPUVCORE_FSET	71C7
TRUE		GPUBBP_ADJ	71B7

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7C8 7D8 12C4 12D4 87D6
TRUE		FSB_ADS_L	7D6 12C4 87D6
TRUE	TRUE	FSB_ADSTB_L<1..0>	7C8 7D8 12C4 87C6
TRUE		FSB_BNR_L	7D6 12C4 87D6
TRUE		FSB_BREQ0_L	7D6 12C4 87D6
TRUE		FSB_D_L<63..0>	7B3 7B4 7C3 7C4 12B6 12C6 12D6 87D6
TRUE		FSB_DBSY_L	7D6 12B4 87D6
TRUE	TRUE	FSB_DINV_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE		FSB_DRDY_L	7D6 12B4 87D6
TRUE	TRUE	FSB_DSTBN_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE	TRUE	FSB_DSTBP_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE		FSB_HIT_L	7D6 12B4 87D6
TRUE		FSB_HITM_L	7D6 12B4 87D6
TRUE		FSB_LOCK_L	7D6 12B4 87D6
TRUE		FSB_REQ_L<4..0>	7D8 12A4 12B4 87D6

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA			
TRUE		DMI_N2S_P<1..0>	14B4 22D2
TRUE		DMI_N2S_N<1..0>	14B4 22D2
TRUE		SB_CLK100M_SATA_P	21B6 33B4 34C3 34C5
TRUE		SB_CLK100M_SATA_N	21B6 33B4 34C3 34C5
TP70	TRUE	USB_BT_P	6C1 6C2 6C3 22C2 81A4
TP80	TRUE	USB_BT_N	6C1 6C2 6C3 22C2 81A4

Misc NO_TESTs

NO_TEST	EXPOSED_VIA		
TP85	TRUE	USB2_CAMERA_P_F	45B5
TP86	TRUE	USB2_CAMERA_N_F	45B5
TP8	TRUE	TP_FW_CTL<0>	37C3

Functional Test Points

Power Nets

FUNC_TEST		
TP39	TRUE	PP0V9_S0
TP38	TRUE	PP1V05_S0
TP37	TRUE	PP1V2_D3C
TP36	TRUE	PP1V2_S3
TP44	TRUE	PP1V5_S0
TP45	TRUE	PP1V5_S0_NB
TP46	TRUE	PP1V8_S3
TP47	TRUE	PP1V8_D3C
TP76	TRUE	PP2V5_S0
TP47	TRUE	PP2V5_D3C
TP48	TRUE	PP3V3_S0
TP49	TRUE	PP3V3_S3
TP50	TRUE	PP3V3_S5
TP51	TRUE	PP5V_S0
TP52	TRUE	PP5V_S3
TP53	TRUE	PP5V_S5
TP54	TRUE	PPBUS_G3H
TP55	TRUE	GND

Request for at least 10 GND TPs

Characterization TPs

FUNC_TEST		
TP58	TRUE	IMVP_VR_ON
TP60	TRUE	IMVP_DPRSLPVR
TP59	TRUE	PM_SLP_S3_L
TP61	TRUE	PM_SLP_S3BATT
TP62	TRUE	PM_SLP_S4_L
TP63	TRUE	PM_SLP_S5_L
TP64	TRUE	P1V5P1V05S0_PGOOD
TP65	TRUE	CPU_DPRSTP_L
TP66	TRUE	IMVP6_VID<6..0>
TP67	TRUE	FSB_CLK_CPU_N
TP68	TRUE	FSB_CLK_CPU_P
TP69	TRUE	PLT_RST_L
TP70	TRUE	PLT_RST_L
TP71	TRUE	PEG_RESET_L
TP72	TRUE	SMC_LRESET_L
TP73	TRUE	TPM_LRESET_L
TP74	TRUE	CPU_STPCLK_L
TP75	TRUE	FSB_CLK_NB_P
TP76	TRUE	FSB_CLK_NB_N
TP77	TRUE	CLK_NB_OE_L
TP78	TRUE	NB_CLK100M_GCLKIN_P
TP79	TRUE	NB_CLK100M_GCLKIN_N
TP80	TRUE	NB_CLK_DREFCLKIN_P
TP81	TRUE	NB_CLK_DREFCLKIN_N
TP82	TRUE	NB_CLK_DREFSSCLKIN_P
TP83	TRUE	NB_CLK_DREFSSCLKIN_N
TP84	TRUE	CPU_THERMTRIP_R
TP85	TRUE	TP_SB_SUS_CLK

MAC-1 TPs

FUNC_TEST		
TP27	TRUE	CPU_PWRGD
TP28	TRUE	TP_CPU_CPUSLP_L
TP29	TRUE	PM_DPRSLPVR
TP30	TRUE	CPU_DPSLP_L
TP31	TRUE	PM_LAN_ENABLE
TP32	TRUE	PCI_RST_L
TP33	TRUE	PM_RSMRST_L
TP35	TRUE	PM_SB_PWROK
TP34	TRUE	SB_RTC_RST_L
TP16	TRUE	PM_STPCPU_L
TP17	TRUE	PM_STPPCI_L
TP18	TRUE	VR_PWRGD_CK410
TP19	TRUE	VR_PWRGOOD_DELAY
TP40	TRUE	FSB_CPURST_L
TP41	TRUE	FSB_SLPCPU_L
TP42	TRUE	FSB_DPWR_L
TP43	TRUE	NB_SB_SYNC_L
TP44	TRUE	PP2V5_S0_GPU_TPVDD
TP45	TRUE	PP2V5_S0_GPU_TXVDDR
TP46	TRUE	PP2V5_S0_GPU_AVDD
TP47	TRUE	PP2V5_S0_GPU_A2VDD
TP48	TRUE	PP2V5_S0_GPU_LPVDD
TP49	TRUE	PP2V5_S0_GPU_LVDDR
TP49	TRUE	PP3V3_S0
TP51	TRUE	PP3V3_S0_CK410_VDD48
TP53	TRUE	PP3V3_S0_CK410_VDD_PCI
TP54	TRUE	PP3V3_S0_CK410_VDD_REF
TP55	TRUE	PP3V3_S0_CK410_VDD_CPU_SRC
TP56	TRUE	PP3V3_S0_CK410_VDDA
TP57	TRUE	PP3V3_FWPHY
TP57	TRUE	PP3V3_FWPHY_AVDD
TP58	TRUE	PP3V3_FWPHY_PLLVDD
TP59	TRUE	PP1V95_FWPHY
TP60	TRUE	PP1V95_FWPHY_PLLVDD
TP61	TRUE	PP1V2_S3
TP62	TRUE	PP3V3_S3AC
TP63	TRUE	PP2V5_S3
TP64	TRUE	PP2V5_S3_ENET_AVDD

Fan Connectors

FUNC_TEST		
TP87	TRUE	PP5V_S0
TP88	TRUE	FAN_LT_PWM
TP89	TRUE	FAN_LT_TACH
TP90	TRUE	FAN_RT_PWM
TP91	TRUE	FAN_RT_TACH

LPC+ Debug Connector

FUNC_TEST		
TP92	TRUE	PP3V42_G3H
TP93	TRUE	PP5V_S0
TP94	TRUE	LPC_AD<0>
TP95	TRUE	LPC_AD<1>
TP96	TRUE	LPC_FRAME_L
TP97	TRUE	PM_CLKRUN_L
TP98	TRUE	BOOT_LPC_SPI_L
TP99	TRUE	SMC_TMS
TP100	TRUE	DEBUG_RST_L
TP101	TRUE	SMC_TRST_L
TP102	TRUE	SMC_TDO
TP103	TRUE	SMC_MD1
TP104	TRUE	SMC_TX_L
TP105	TRUE	FWH_INIT_L
TP106	TRUE	PCI_CLK_PORT80_LPC
TP107	TRUE	LPC_AD<2>
TP108	TRUE	LPC_AD<3>
TP109	TRUE	INT_SERIRQ
TP110	TRUE	PM_SUS_STAT_L
TP111	TRUE	SMC_TDI
TP112	TRUE	SMC_TCK
TP113	TRUE	SMC_RST_L
TP114	TRUE	SMC_NMI
TP115	TRUE	SMC_RX_L
TP116	TRUE	SV_SET_UP

Resistor Calibration

FUNC_TEST		
TP141	TRUE	PP5V_S0_ISENSECAL
TP141	TRUE	PP1V8_S3
TP140	TRUE	PP1V05_S0
TP139	TRUE	PPVCORE_S0_CPU
TP138	TRUE	PPVCORE_D3C_GPU
TP143	TRUE	ISENSE_CAL_EN
TP144	TRUE	GND

Request for at least 2 GND TPs per resistor

Camera Connector

FUNC_TEST		
TP168	TRUE	PP5V_S3
TP162	TRUE	USB2_CAMERA_N
TP163	TRUE	USB2_CAMERA_P
TP260	TRUE	PP5V_S3_CAMERA_F

Inverter Connector

TP274	TRUE	GND_CHASSIS_INVERTER
TP275	TRUE	PPBUS_S0_INVERTER
TP277	TRUE	PP5V_INVERTER_SW
TP276	TRUE	INVERTER_PWM
TP278	TRUE	GND_CHASSIS_INVERTER

Thermal Sensors

FUNC_TEST		
TP172	TRUE	HSTHMSNS_DX_P
TP174	TRUE	HSTHMSNS_DX_N
TP172	TRUE	RSFSTHMSNS_D_P
TP175	TRUE	RSFSTHMSNS_D_N

SMC TPs

FUNC_TEST		
TP177	TRUE	PM_SYSRST_L
TP176	TRUE	SMC_ONOFF_L

Battery Connector

FUNC_TEST		
TP180	TRUE	BATT_POS
TP181	TRUE	BATT_NEG

Left I/O Data Connector

FUNC_TEST		
TP182	TRUE	ALS_GAIN
TP183	TRUE	LTALS_OUT
TP184	TRUE	ACZ_SDATAIN<0>
TP185	TRUE	ACZ_SDATAOUT
TP186	TRUE	ACZ_BITCLK
TP187	TRUE	ACZ_RST_L
TP188	TRUE	EXCARD_OC_L
TP189	TRUE	LTUSB_OC_L
TP190	TRUE	LT2USB_OC_L
TP191	TRUE	PM_SLP_S3_LS5V
TP192	TRUE	PM_SLP_S4_L
TP193	TRUE	SYS_ONEWIRE
TP194	TRUE	MINI_CLKREQ_L
TP195	TRUE	SMC_EXCARD_CP
TP196	TRUE	EXCARD_CLKREQ_L
TP197	TRUE	SMC_EXCARD_PWR_EN
TP198	TRUE	LIO_PLT_RESET_L
TP199	TRUE	ACZ_SYNC
TP200	TRUE	USB2_LT_N
TP201	TRUE	USB2_LT_P
TP202	TRUE	USB2_EXCARD_N
TP203	TRUE	USB2_EXCARD_P
TP204	TRUE	PCIE_EXCARD_R2D_C_N
TP205	TRUE	PCIE_EXCARD_R2D_C_P
TP206	TRUE	PCIE_EXCARD_D2R_N
TP207	TRUE	PCIE_EXCARD_D2R_P
TP208	TRUE	PCIE_CLK100M_EXCARD_P
TP209	TRUE	PCIE_CLK100M_EXCARD_N
TP210	TRUE	USB2_LT2_N
TP211	TRUE	USB2_LT2_P
TP212	TRUE	PCIE_MINI_R2D_C_N
TP213	TRUE	PCIE_MINI_R2D_C_P
TP214	TRUE	PCIE_MINI_D2R_N
TP215	TRUE	PCIE_MINI_D2R_P
TP216	TRUE	PCIE_CLK100M_MINI_P
TP217	TRUE	PCIE_CLK100M_MINI_N
TP218	TRUE	SMBUS_SB_SCL
TP219	TRUE	SMBUS_SB_SDA
TP220	TRUE	PCIE_WAKE_L
TP221	TRUE	SMC_BC_ACOK
TP222	TRUE	SMBUS_SMC_A_S3_SCL
TP223	TRUE	SMBUS_SMC_A_S3_SDA

Left I/O Power Connector

FUNC_TEST		
TP224	TRUE	PP18V5_DCIN
TP225	TRUE	PPBUS_G3H
	TRUE	GND

Request for at least 10 GND test points

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7164 | REV. 03001

SCALE NONE | SHT 5 OF 87

NC_CPU_A32_L
NC_CPU_A33_L
NC_CPU_A34_L
NC_CPU_A35_L
NC_CPU_A36_L
NC_CPU_A37_L
NC_CPU_A38_L
NC_CPU_A39_L
NC_CPU_APM0_L
NC_CPU_APM1_L
NC_CPU_EXTBREF
NC_CPU_HFPLL
NC_CPU_SPARE0
NC_CPU_SPARE1
NC_CPU_SPARE2
NC_CPU_SPARE4
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_MEM_A_A<15..14>
NC_MEM_B_A<15..14>
MEM_A_A<15..14>
MEM_B_A<15..14>
MAKE_BASE=TRUE
NO_TEST=TRUE

TP_NB_CFG<4..3>
TP_NB_CFG<6>
TP_NB_CFG<8>
TP_NB_CFG<11..10>
TP_NB_CFG<15..14>
TP_NB_CFG<17>
NB_CFG<4..3>
NB_CFG<6>
NB_CFG<8>
NB_CFG<11..10>
NB_CFG<15..14>
NB_CFG<17>
MAKE_BASE=TRUE

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12>
NB_CFG<13..12>

TP_SB_SUS_CLK
MAKE_BASE=TRUE

Inverter PWM Reset Alias

PLT_RST_L

R0600

ALS_GAIN — 1 — R0600 0 5% 1/16W MF-LF 402 — 2 — RTALS_GAIN
MAKE_BASE=TRUE

NC_ENET_CTRL12
NC_ENET_CTRL25
MAKE_BASE=TRUE
NO_TEST=TRUE

Ethernet Powr Management Support

ENET_LOWPWR_EN

R0690 0 5% 1/16W MF-LF 402

SB_GPIO30 — ENET_LOWPWR_EN

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOWPWR_EN" are mutually-exclusive.

FireWire Aliases

PPFW_PORTA_VP_UF
PPFW_PORTB_VP_UF
MAKE_BASE=TRUE

PP3V3_FWPHY
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.20 mm
MAKE_BASE=TRUE

PP1V95_FWPHY
VOLTAGE=1.95V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
MAKE_BASE=TRUE

SMC_RSTGATE_L
PCI_AD<19>
PCI_GNT3_L
PCI_REQ3_L
MAKE_BASE=TRUE

=FW_PCI_IDSEL

USB Port "A" (Debug Port) = Right USB 2.0 Port

USB2_RT_P
USB2_RT_N
RTUSB_OC_L
MAKE_BASE=TRUE

USB Port "B" = Trackpad (Geyser)

USB_TRACKPAD_P
USB_TRACKPAD_N
UNUSED_USB_B_OC_L
MAKE_BASE=TRUE

USB Port "C" = Left USB 2.0 Port

USB2_LT_P
USB2_LT_N
LTUSB_OC_L
MAKE_BASE=TRUE

USB Port "D" = Camera

USB2_CAMERA_P
USB2_CAMERA_N
UNUSED_USB_D_OC_L
MAKE_BASE=TRUE

USB Port "E" = ExpressCard

USB2_EXCARD_P
USB2_EXCARD_N
EXCARD_OC_L
MAKE_BASE=TRUE

USB Port "F" = USB 1.1 Hub

USB_HUB_P
USB_HUB_N
MAKE_BASE=TRUE

USB Port "G" = Bluetooth (M13P)

USB_BT_P
USB_BT_N
MAKE_BASE=TRUE

USB Port "H" = 2nd Left USB 2.0 Port

USB2_LT2_P
USB2_LT2_N
LT2USB_OC_L
MAKE_BASE=TRUE

TP_USB2_3G_P
TP_USB2_3G_N
MAKE_BASE=TRUE

LVDS Pull Down Aliases

=LVDS_PD_L_CLK_N
=LVDS_PD_L_CLK_P
LVDS_L_DATA_P<1>
LVDS_L_DATA_N<1>
LVDS_L_DATA_P<0>
LVDS_L_DATA_N<0>
LVDS_L_CLK_N
LVDS_L_CLK_P
=LVDS_PD_L_DATA_P<2>
=LVDS_PD_L_DATA_N<2>
=LVDS_PD_U_CLK_N
=LVDS_PD_U_CLK_P
LVDS_U_DATA_N<1>
LVDS_U_DATA_P<0>
LVDS_U_DATA_P<1>
=LVDS_PD_U_DATA_P<1>
=LVDS_PD_U_DATA_N<1>
LVDS_U_CLK_N
LVDS_U_CLK_P
MAKE_BASE=TRUE

Base net is PM_SLP_S3_LS5V

PM_SLP_S4_L

Base net is PM_SLP_S4_L

PM_SLP_S3_LS5V

Chassis connection to be made at the fan cutout near the right ALS. Not stuffed at Proto.

NO STUFF
SH0601 EMI-SPRING 00-5024208
GND_CHASSIS_FANFRAME
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
NO STUFF R0601 0 5% 1/16W MF-LF 402

Chassis connection to be made at the mounting hole northwest of the DVI connector. Plated hole.

ZT0600 195R106
GND_CHASSIS_DVI_TOP
C0600 0.01UF 10% 50V X7R 402
GND_CHASSIS_DVI_TOP
GND

Chassis connection to be made on FW shell

ZT0603 HOLE-VIA-P5RP25
GND_CHASSIS_DVI_BOT
NO STUFF R0602 0 5% 1/16W MF-LF 402
GND_CHASSIS_DVI_BOT

ZT0604 HOLE-VIA-P5RP25
GND_CHASSIS_ENET
GND_CHASSIS_ENET
GND_CHASSIS_ENET

Chassis connection to be made at the mounting hole southwest of the USB connector. Plated hole.

ZT0601 195R106
GND_CHASSIS_USB
GND_CHASSIS_USB
GND_CHASSIS_USB

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602 HOLE-VIA-P5RP25
GND_CHASSIS_LVDS
C0602 0.01UF 10% 50V X7R 402
GND_CHASSIS_LVDS

SH0600 OG-503040 SHLD-SM-LF
GND_CHASSIS_INVERTER
GND_CHASSIS_INVERTER
GND_CHASSIS_INVERTER
GND_CHASSIS_INVERTER LEFT CLUTCH BARREL CABLING

Thermal Module Holes

Add one through via per hole to GND or 2 blind vias per side per hole to GND

Top CPU TM Hole
Top GPU Right TM Hole
Left CPU TM Hole
Right CPU TM Hole
Lower Left GPU TM Hole

Frame holes

ZT0612 HOLE-VIA-P5RP25 GND_CHASSIS_LIOFLEX_HOLE
C0612 0.01UF 10% 50V X7R 402
C0613 0.01UF 10% 50V X7R 402

ZT0613 HOLE-VIA-P5RP25 GND_CHASSIS_ODD_HOLE
C0610 0.01UF 10% 50V X7R 402
C0611 0.01UF 10% 50V X7R 402

ZT0611 HOLE-VIA-P5RP25 GND_CHASSIS_BATTCONN_HOLE
GND_CHASSIS_BATTCONN_HOLE
C0619 0.01UF 10% 50V X7R 402
C0614 0.01UF 10% 50V X7R 402

ZT0610 HOLE-VIA-P5RP25 GND_CHASSIS_LNDACARD_HOLE
C0615 0.01UF 10% 50V X7R 402
C0616 0.01UF 10% 50V X7R 402

ZT0614 HOLE-VIA-P5RP25 GND_CHASSIS_LEFT_DIMM_HOLE
C0617 0.01UF 10% 50V X7R 402
C0618 0.01UF 10% 50V X7R 402

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

Signal Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

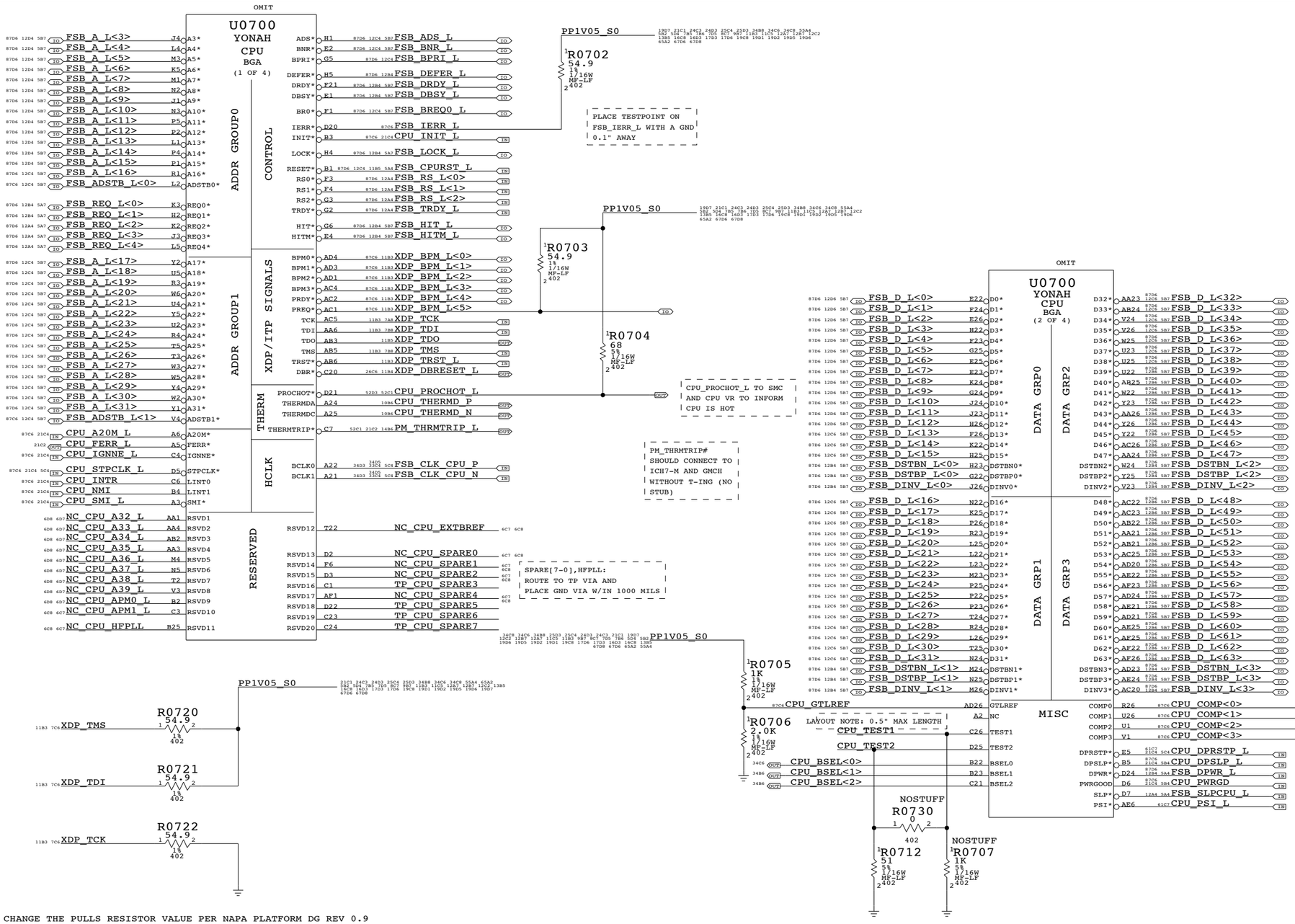
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 6 OF 87	



CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

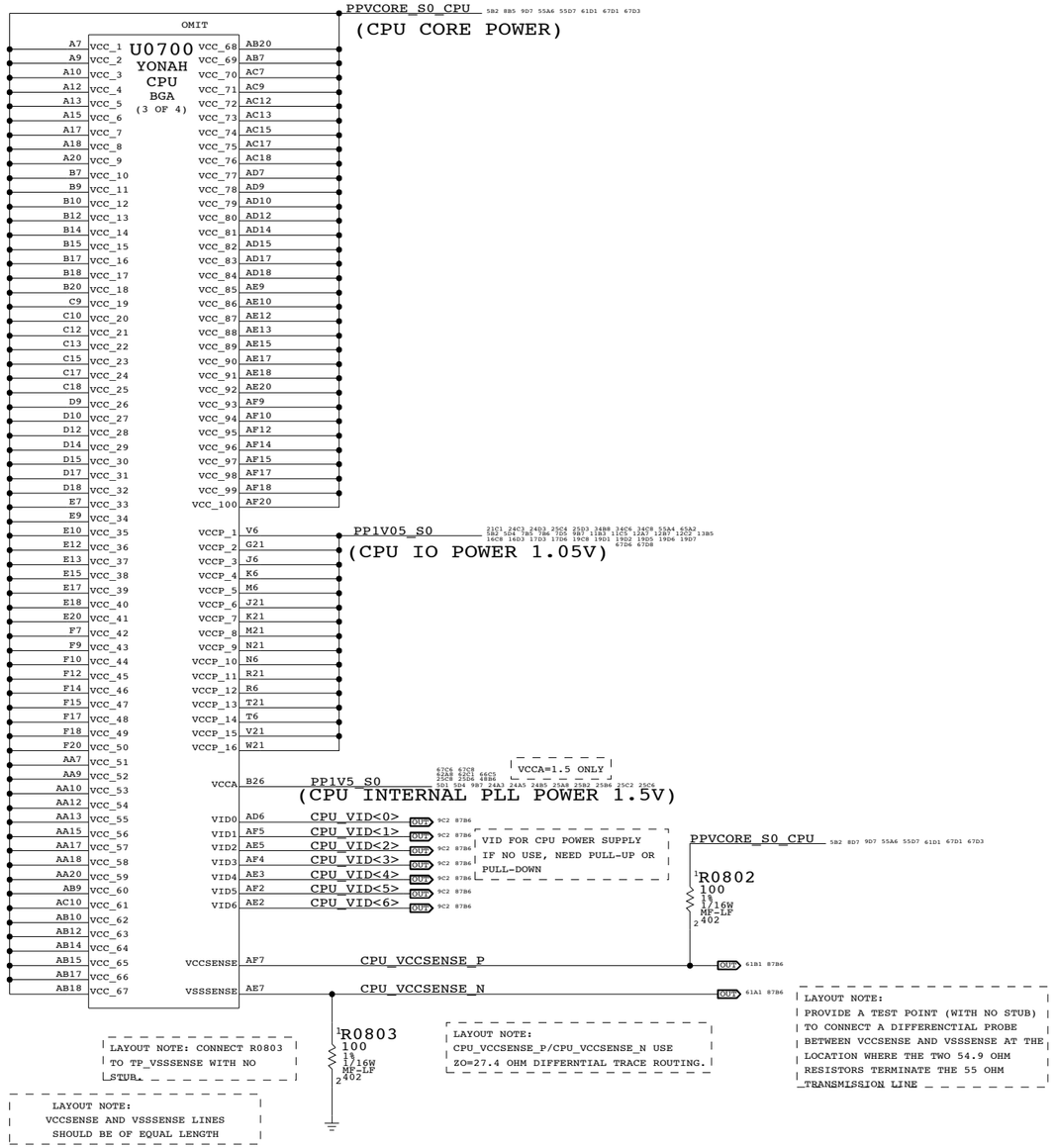
II NOT TO REPRODUCE OR COPY IT

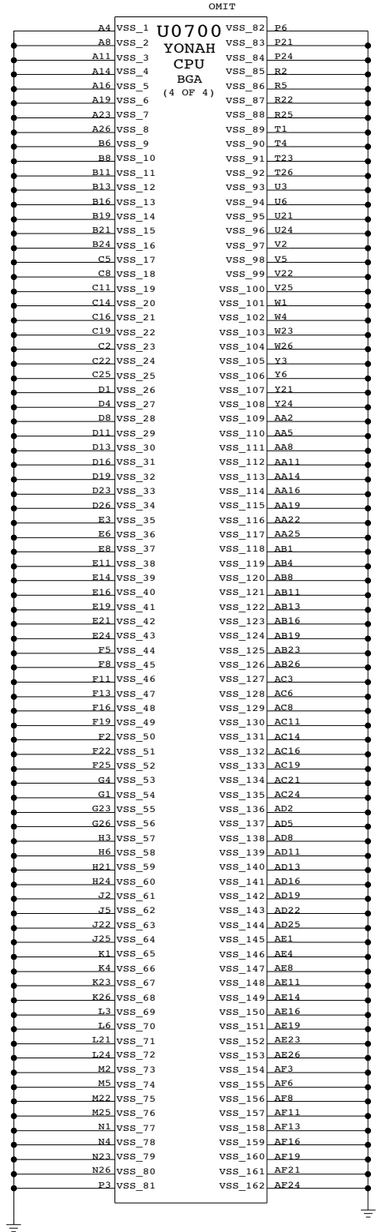
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	7	87





CPU 2 OF 2-PWR/GND

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

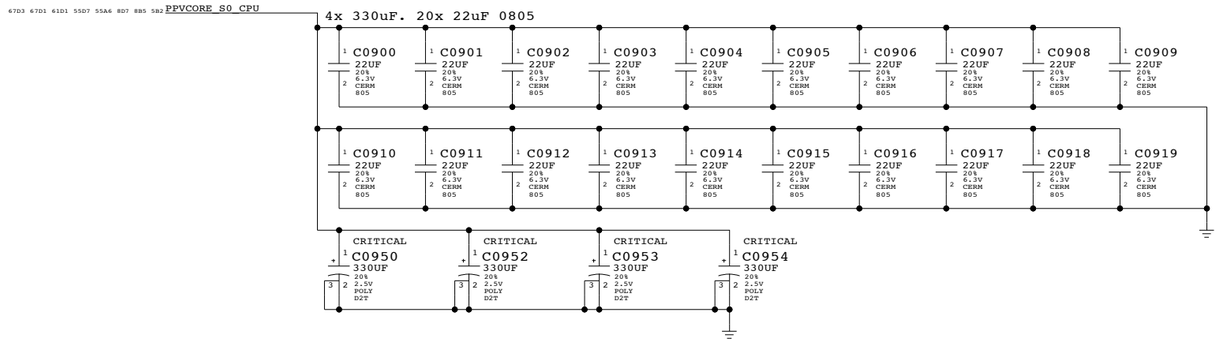
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

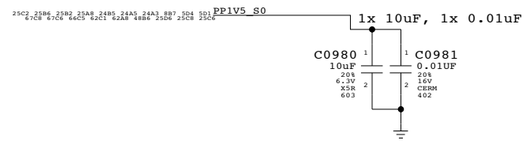
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 8 OF 87	

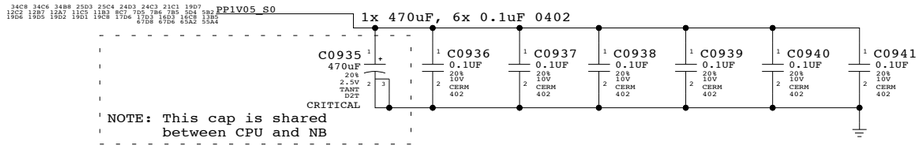
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

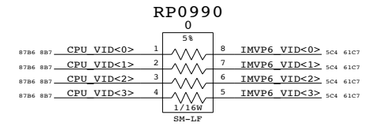


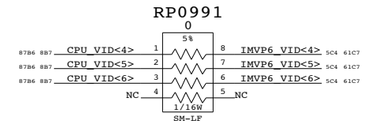
VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production





CPU Decoupling & VID

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

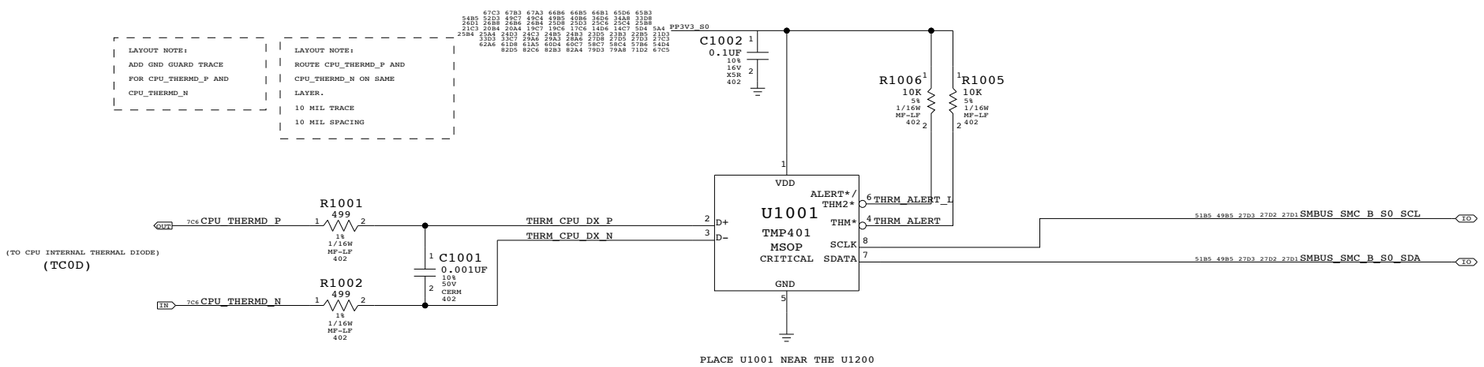
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	9	87

CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

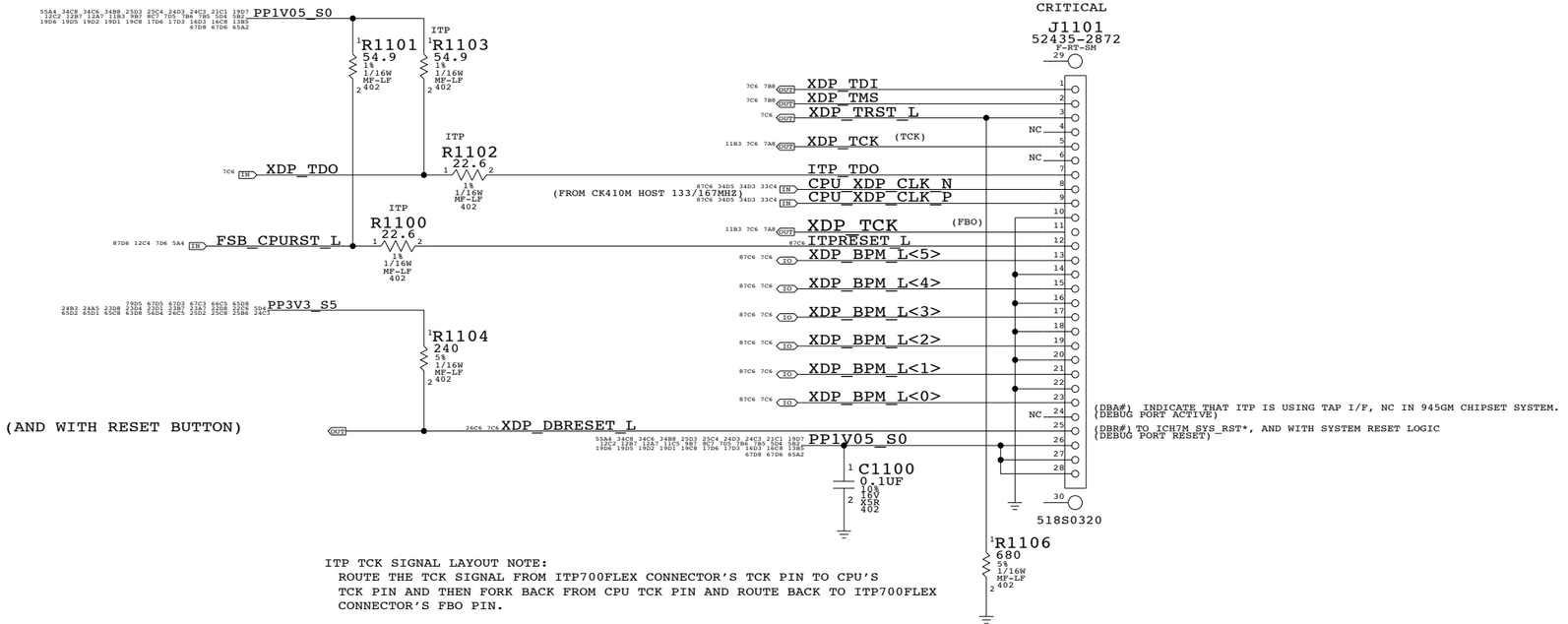
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	10	87

CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM. (DEBUG PORT ACTIVE)

(DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC (DEBUG PORT RESET)

CPU ITP700FLEX DEBUG

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

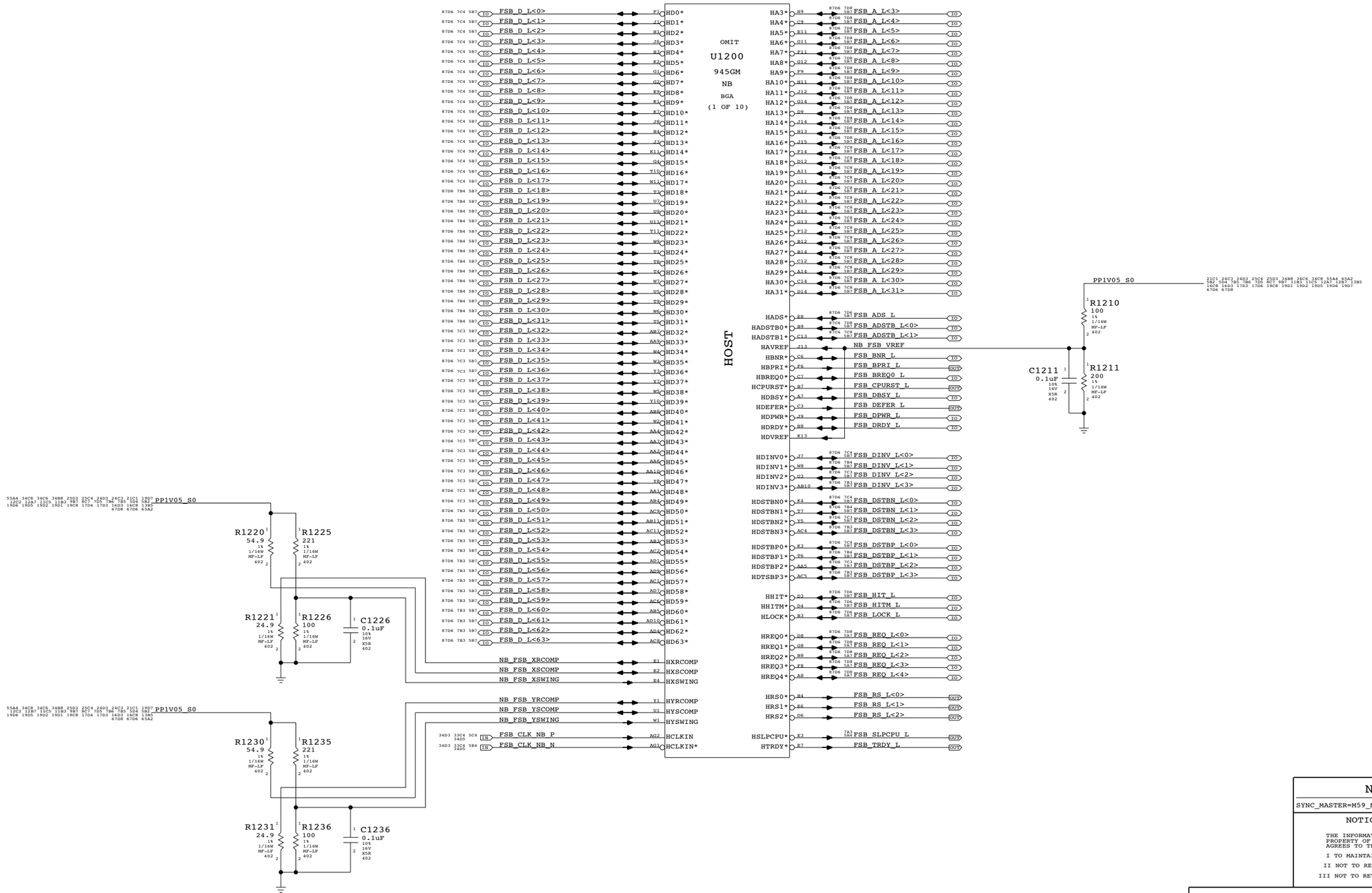
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 11 OF 87	



NB CPU Interface

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	12	87

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

NB PEG / Video Interfaces

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

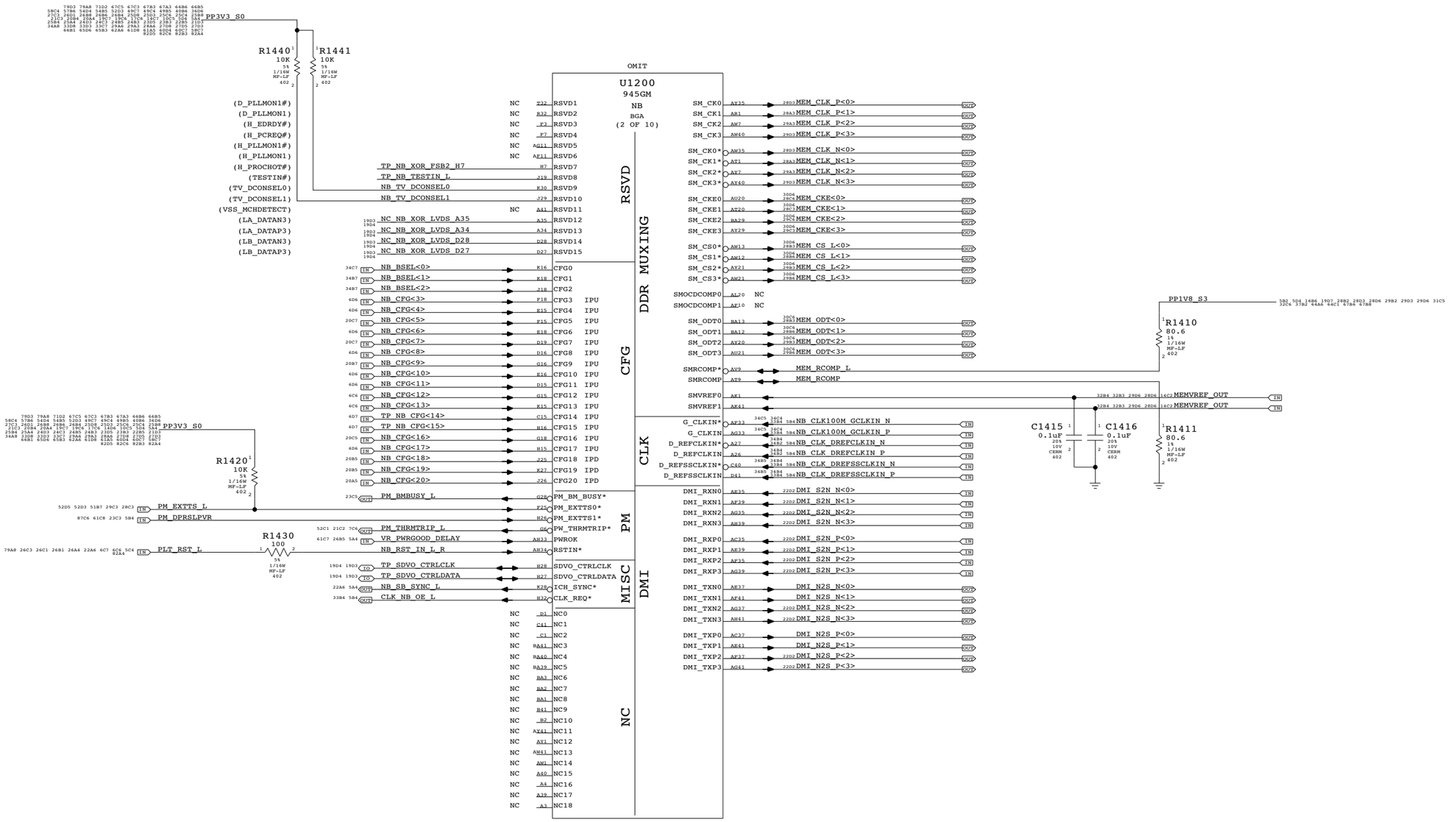
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 13 OF 87	



NB Misc Interfaces

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

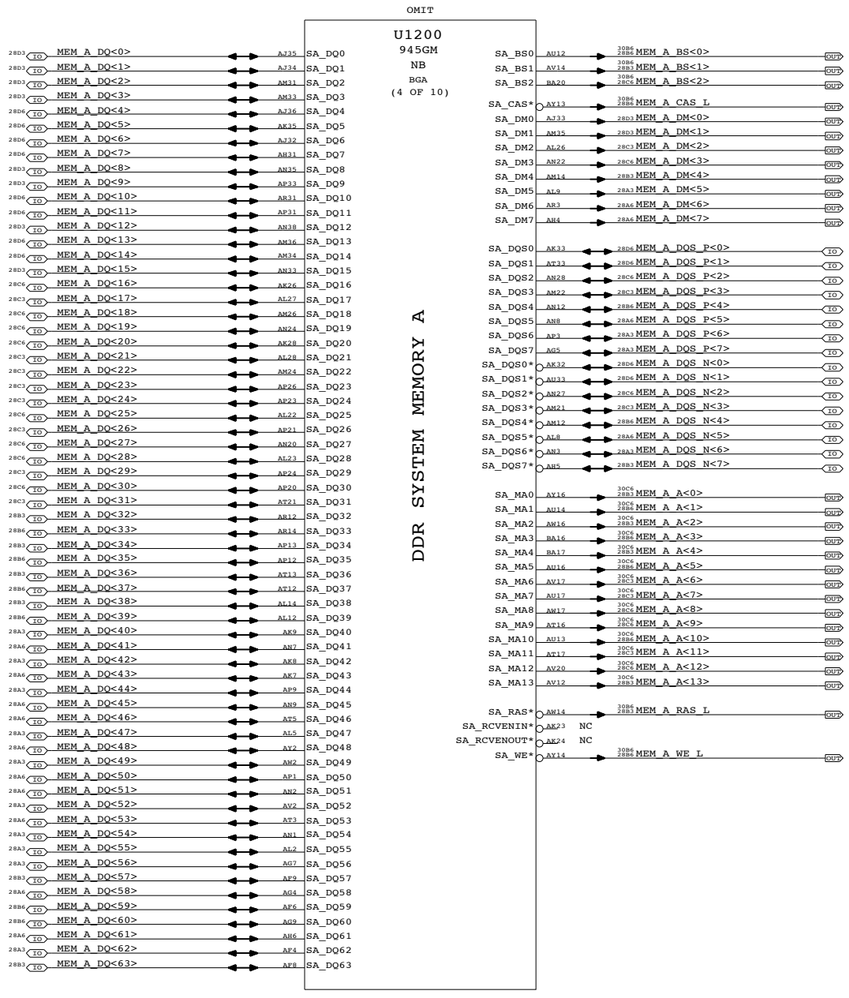
II NOT TO REPRODUCE OR COPY IT

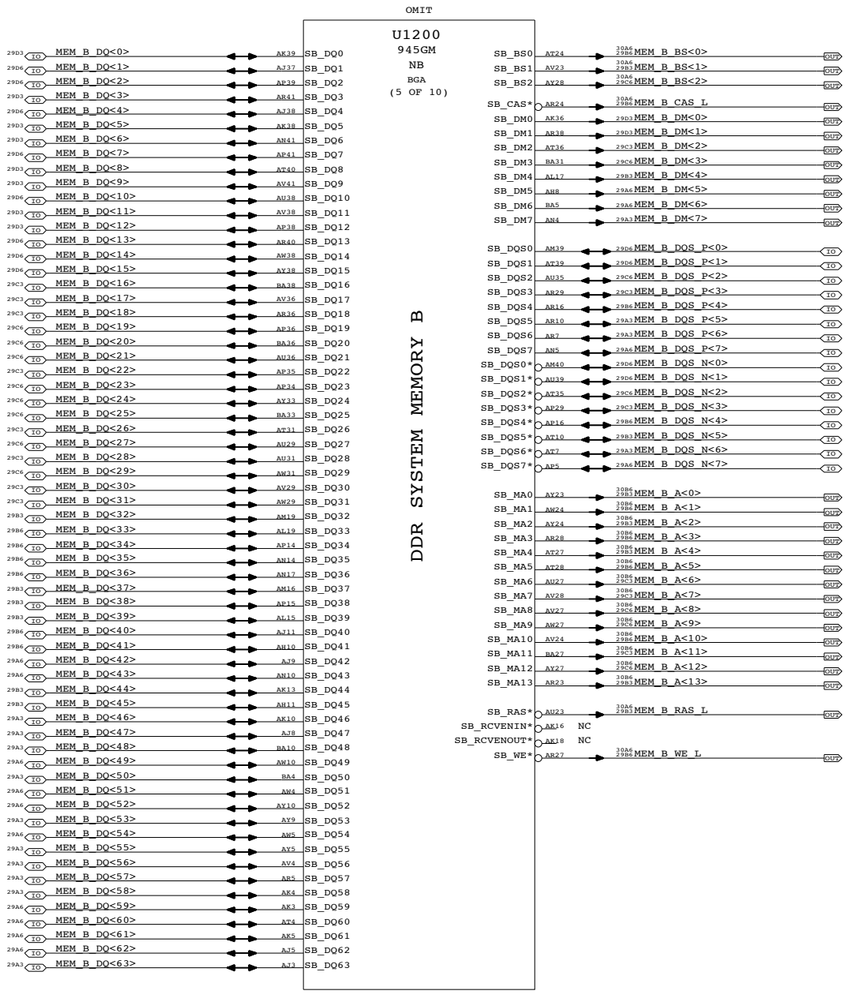
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 14 OF 87





NB DDR2 Interfaces

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

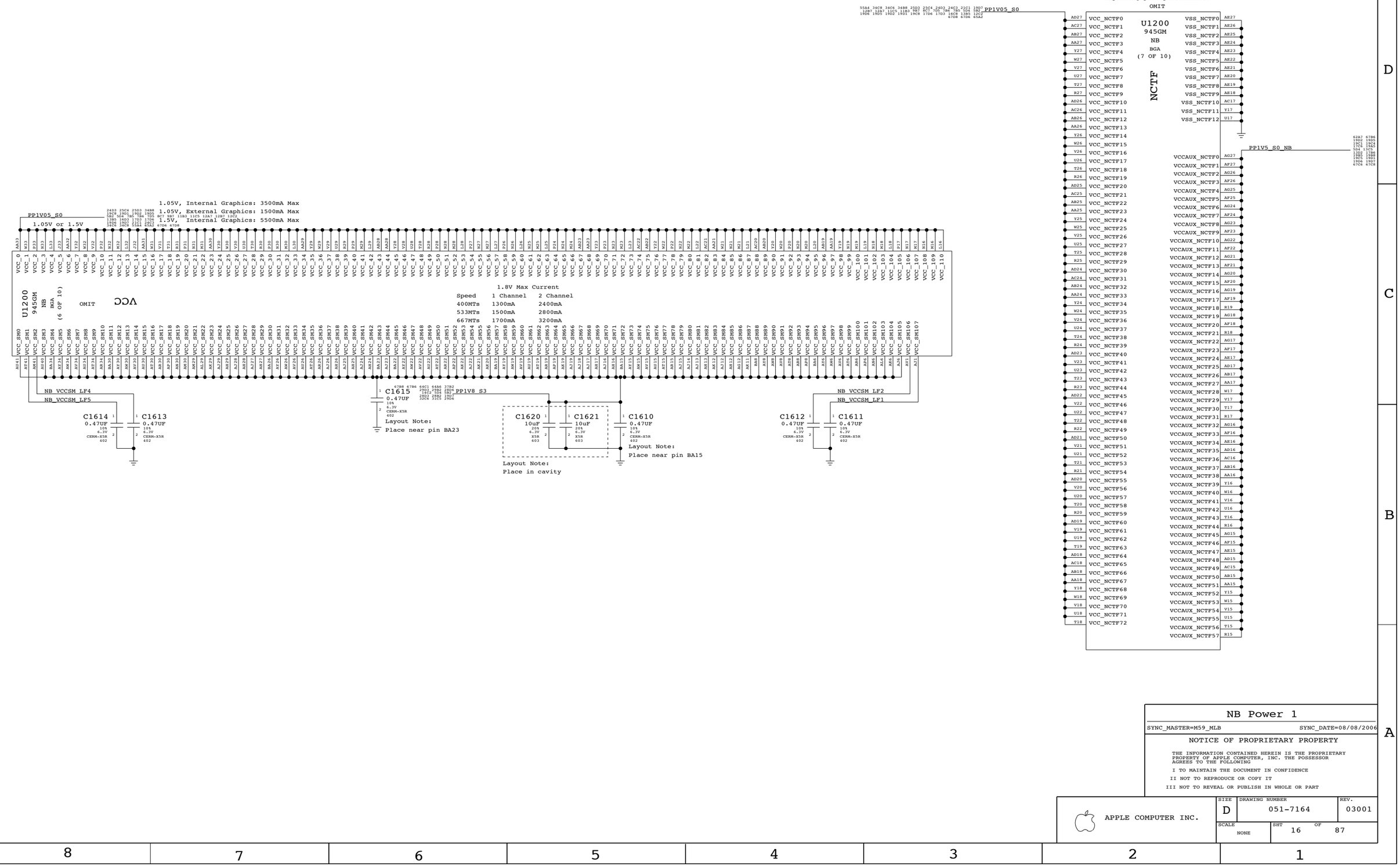
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	15	87



NB Power 1

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

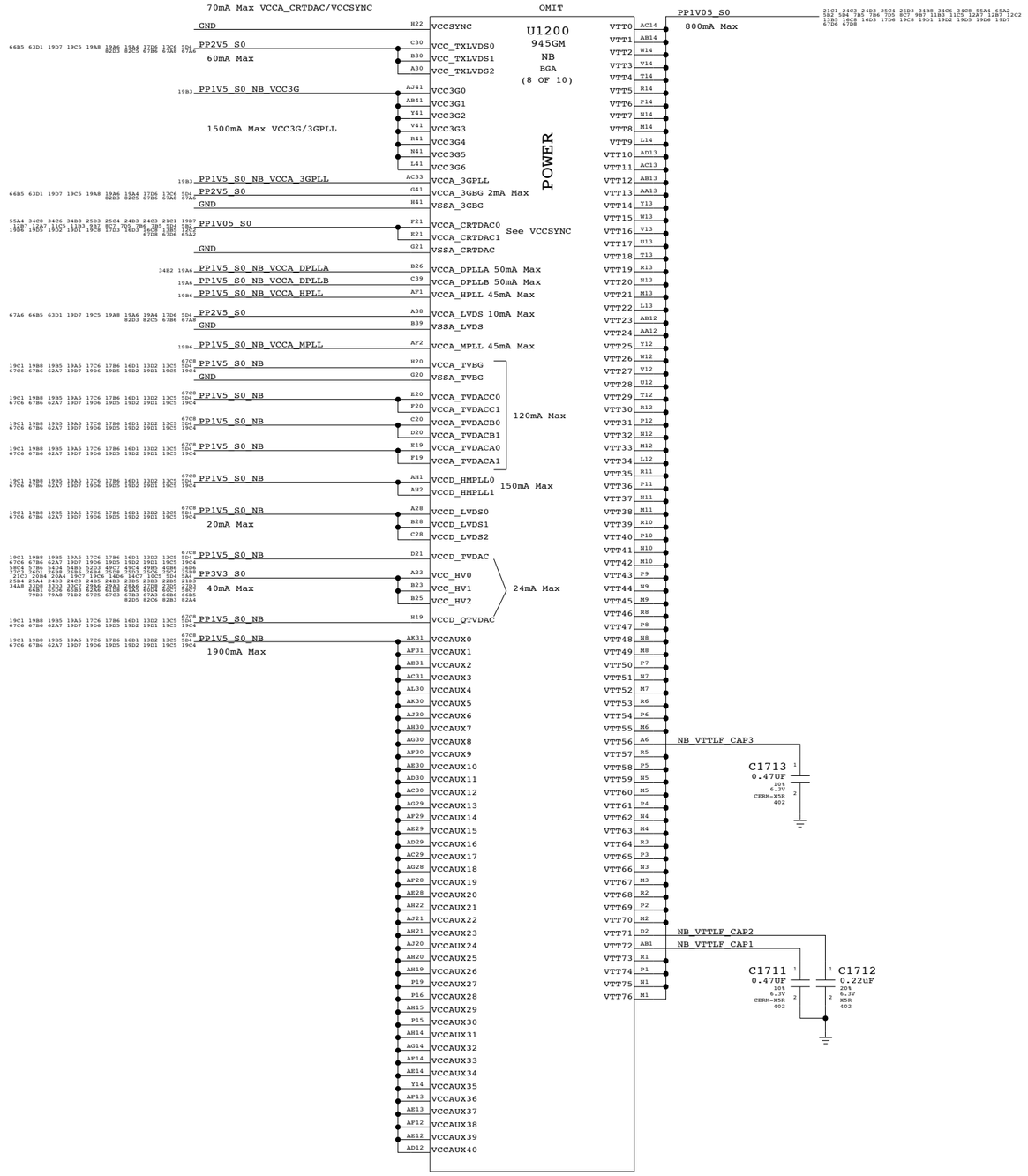
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	16	87



NB Power 2

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

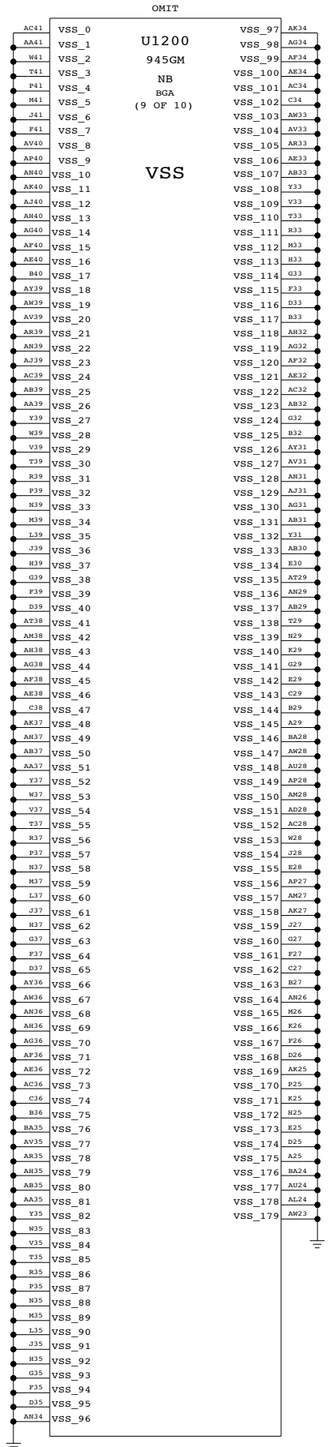
II NOT TO REPRODUCE OR COPY IT

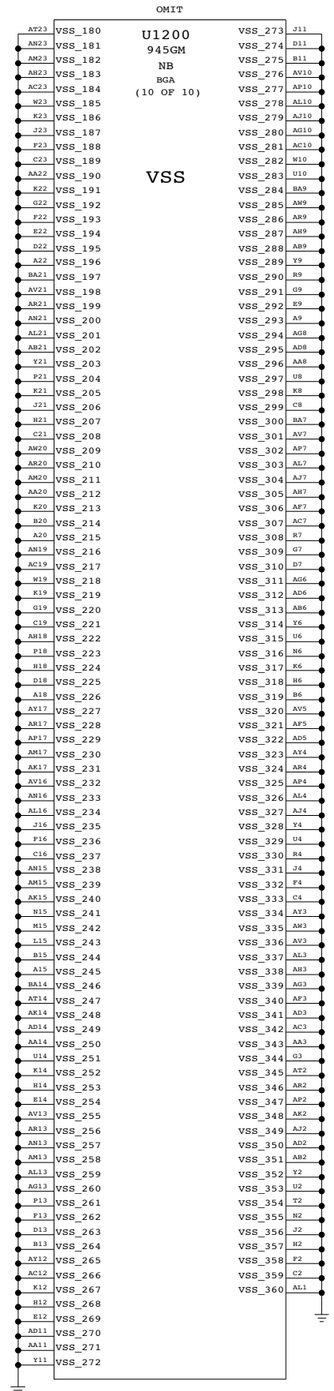
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	17	87





NB Grounds

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	18	87

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?
3674mA Max
3200mA Max
132mA Max
40mA Max?

PP1V05_S0 — 10mA Max?
PP1V05_S0 — 800mA Max
PP1V05_S0_NB — 7mA Max
PP1V05_S0_NB — 1500mA Max
PP1V05_S0_NB — 100mA Max
PP1V05_S0_NB — 7mA Max
PP1V05_S0_NB — 150mA Max
PP1V05_S0_NB — 1900mA Max
PP1V8_S3 — 3200mA Max
GND
PP2V5_S0 — 70mA Max
PP2V5_S0 — 60mA Max
2mA Max
PP3V3_S0 — 7mA Max
PP3V3_S0 — 40mA Max

PP1V05_S0 → PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, GND, GND

PP1V05_S0 → TP_LVDS_CLKCTLA, TP_LVDS_CLKCTLB, NC_NB_XOR_LVDS_A34, NC_NB_XOR_LVDS_A35, NC_NB_XOR_LVDS_D27, NC_NB_XOR_LVDS_D28, TP_SDVO_CTRLCLK, TP_SDVO_CTRLDATA (MAKE_BASE=TRUE; NO_TEST=TRUE)

PP1V05_S0 → (MCH CRTDAC ANALOG 2.5V PWR) PP1V05_S0, GND

(MCH H/V SYNC 2.5V PWR) GND

PP1V5_S0_NB → (MCH TVDAC DEDICATED PWR 1.5V) PP1V5_S0_NB; (MCH TVDAC DIGITAL QUIET 1.5V PWR) PP1V5_S0_NB; (MCH TV OUT CHANNEL A 3.3V PWR) PP1V5_S0_NB; (MCH TV OUT CHANNEL B 3.3V PWR) PP1V5_S0_NB; (MCH TV OUT CHANNEL C 3.3V PWR) PP1V5_S0_NB; (MCH TV DAC BAND GAP 3.3V PWR) PP1V5_S0_NB; GND

TP_CRT_DDC_CLK — MAKE_BASE=TRUE — 13B5 19D6
TP_CRT_DDC_DATA — MAKE_BASE=TRUE — 13B5 19D6

LVDS_IBG — 13D5
R1990 1.5K 1% 1/16W MF-LF 402 — GND, GND

PP1V5_S0_NB → PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB

GMCH CORE PWR 1.05V BYPASS

PP1V05_S0 — 1500mA Max

CRITICAL
C1900 470uF 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1uF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

MCH VTT BYPASS (MCH FSB 1.05V PWR)

PP1V05_S0 — 800mA Max

C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603
Layout Note: Place in cavity

C1967 0.22uF 20% 6.3V X5R 402
Layout Note: Place on the edge

MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR)

PP3V3_S0 — 40mA Max

C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)

PP2V5_S0 — 2mA Max

C1916 0.1uF 20% 10V CERM 402

GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

PP1V5_S0_NB — 1900mA Max

C1918 0.1uF 20% 10V CERM 402

GMCH VCCA_HPLL FILTER (HOST PLL 1.5V PWR)

PP1V5_S0_NB — 100mA Max
L1934 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_HPLL — MIN_LINE_WIDTH=0.38 mm; MIN_NECK_WIDTH=0.25 mm; VOLTAGE=1.5V — 45mA Max
C1934 22UF 20% 6.3V CERM 805
C1935 0.1uF 20% 10V CERM 402

GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR)

L1936 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_MPLL — MIN_LINE_WIDTH=0.38 mm; MIN_NECK_WIDTH=0.25 mm; VOLTAGE=1.5V — 45mA Max
C1936 22UF 20% 6.3V CERM 805
C1937 0.1uF 20% 10V CERM 402

1500mA Max

L1970 91nH 1210
Layout Note: Place L and C close to MCH
C1970 220UF 20% 2.5V POLY CASE-B2
C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.

GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR)
PP1V5_S0_NB_VCC3G — MIN_LINE_WIDTH=0.5 mm; MIN_NECK_WIDTH=0.25 mm; VOLTAGE=1.5V

L1975 1.0UH-220MA-0.12-OHM 0805
PP1V5_S0_NB_3GPLL_F — MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.4 mm; VOLTAGE=1.5V
R1975 0.51 1% 1/16W MF-LF 402
C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402
Layout Note: 3GPLL 10uF cap should be placed in cavity
Layout Note: Route to caps, then GND

GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_3GPLL — MIN_LINE_WIDTH=0.5 mm; MIN_NECK_WIDTH=0.25 mm; VOLTAGE=1.5V

1500mA Max

GMCH VCCA_DPLLA FILTER (CRT/TVOUT PLL 1.5V PWR)

NO STUFF R1953 0 5% 1/16W MF-LF 402
PP1V5_S0_NB_VCCA_DPLLA — MIN_LINE_WIDTH=0.38 mm; MIN_NECK_WIDTH=0.25 mm; VOLTAGE=1.5V — 50MA MAX

GMCH VCCA_DPLLB FILTER (LVDS PLL 1.5V PWR)

PP2V5_S0 — 70mA Max
CRITICAL
U1900 TPS73115 SOT23-5
IN OUT — PP1V5_S0_NB_DPLL — MIN_LINE_WIDTH=0.38 mm; MIN_NECK_WIDTH=0.25 mm; VOLTAGE=1.5V
EN NR/FB — TPS73115_NR
GND
C1950 1uF 10% 6.3V CERM 402
C1951 0.01uF 10% 16V CERM 402
C1952 10uF 20% 6.3V X5R 603
NO STUFF R1954 0 5% 1/16W MF-LF 402
C1953 0.1uF 20% 10V CERM 402
C1954 0.1uF 20% 10V CERM 402
PP1V5_S0_NB_VCCA_DPLLB — MIN_LINE_WIDTH=0.38 mm; MIN_NECK_WIDTH=0.25 mm; VOLTAGE=1.5V — 50MA MAX

MCH VCC_TXLVDS BYPASS (MCH LVDS TRANSMITTER 2.5V PWR)

PP2V5_S0 — 60MA MAX
C1990 4.7uF 20% 6.3V CERM 603
C1991 0.1uF 20% 10V CERM 402

MCH VCCD_LVDS BYPASS (MCH LVDS DIGITAL 1.5V PWR)

PP1V5_S0_NB — 20MA MAX
C1992 10uF 20% 6.3V X5R 603
C1993 0.1uF 20% 10V CERM 402

MCH VCCA_LVDS BYPASS (MCH LVDS ANALOG 2.5V PWR)

PP2V5_S0 — 10MA MAX
C1994 0.01UF 20% 16V CERM 402
C1995 0.1uF 20% 10V CERM 402
GND
Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 19 OF 87	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14C6 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14C6 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14C6 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14C6 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

PP3V3_S0
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14C6 NB_CFG<18>
Internal pull-down

PP3V3_S0
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14C6 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

PP3V3_S0
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14B6 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

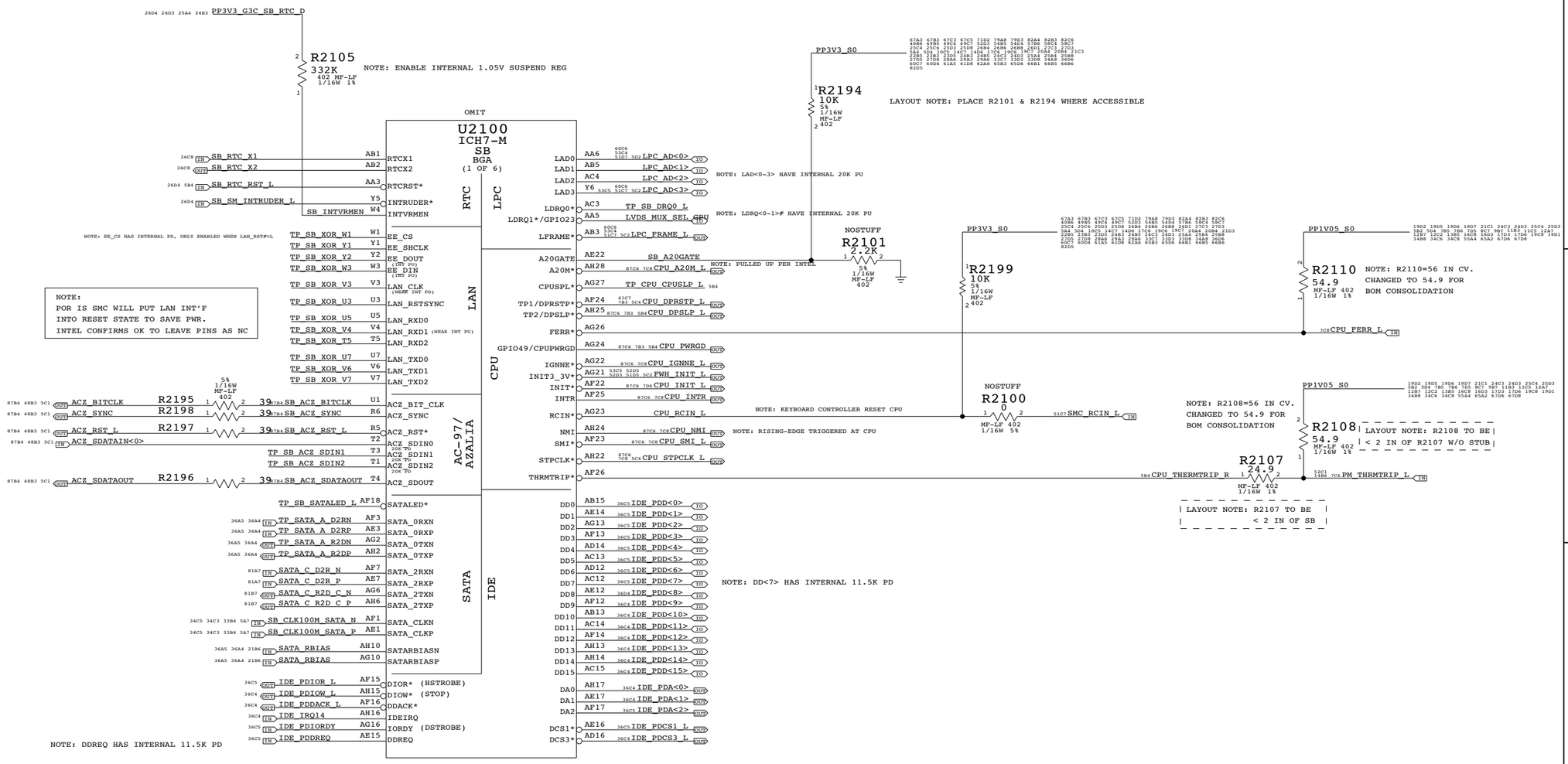
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 20 OF 87	



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

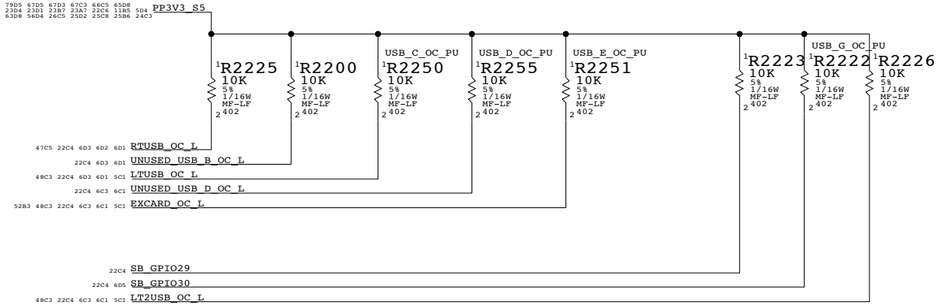
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

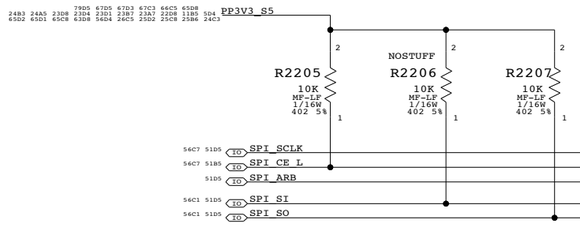
II NOT TO REPRODUCE OR COPY IT

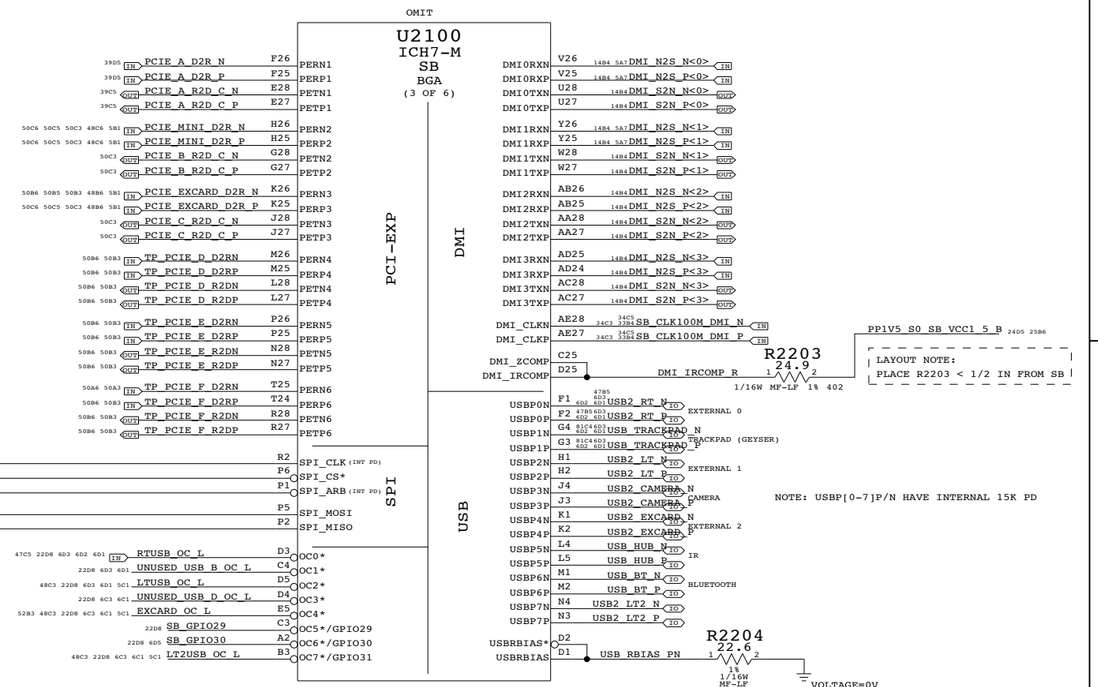
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

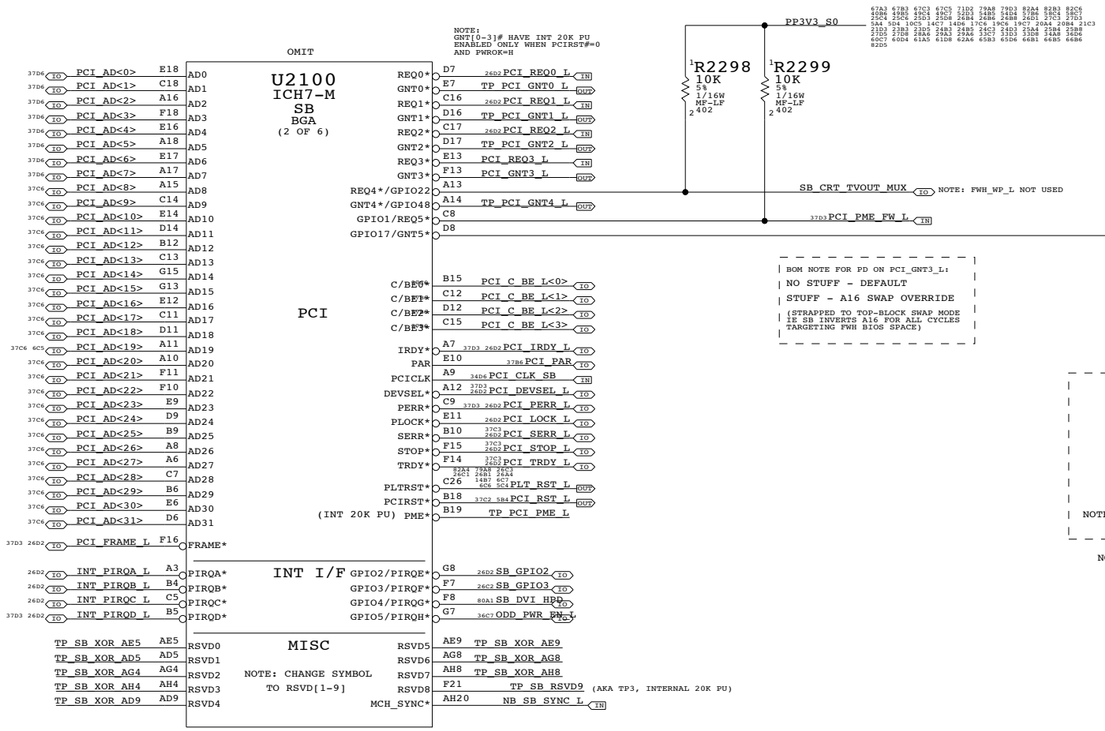
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 21 OF 87	









SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	22	87

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING 8 PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

PP3V3_S0

PP3V3_S5

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 10K 1/16W 402 MF-LF 5% NOSTUFF
R2326 10K 1/16W 402 MF-LF 5% NOSTUFF
R2323 1K 1/16W 402 MF-LF 5% NO_REBOOT_MODE

RP2300 10K 5% 1/16W SM-LF

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB
- SMBCLK C22
- SMBDATA B22
- LINKALERT* A26
- SMLINK0 B25
- SMLINK1 A25
- RI* A28
- SPKR (INT WEAK PD) A19
- SUS_STAT* A27
- SYS_RST* A22

SYS GPIO / PWR MNGT
- GPIO0/BM_BUSY* AB18
- GPIO11/SMBALERT* B23
- GPIO18/STPPCI* AC20
- GPIO20/STPCPU* AF21
- GPIO26 A21
- GPIO27 B21
- GPIO28 E23
- GPIO32/CLKRUN* AG18
- GPIO33/AZ_DOCK_EN* AC19
- GPIO34/AZ_DOCK_RST* U2
- WAKE* F20
- SERIRQ AH21
- THRM* AF20
- VRMPWRGD AD22
- GPIO6 AC21
- GPIO7 AC18
- GPIO8 E21

SMBUS_SB_SCL
SMBUS_SB_SDA
SMB_LINK_ALERT_L
SMLINK<0>
SMLINK<1>
NOT USED
PM_RI_L
SB_SPKR
PM_SUS_STAT_L
PM_SYSRST_L
PM_BMBUSY_L
SMB_ALERT_L
NOTE: RESERVED FOR FUTURE
PM_STPPCI_L
PM_STPCPU_L
SB_GPIO26
BIOS_REC
FWH_MFG_MODE
PM_CLKRUN_L
GPU_D3COLD_RESET_L
TP_AZ_DOCK_RST_L
PCIE_WAKE_L
INT_SERIRQ
PM_THRM_L
VR_PWRGD_CK410
TP_SB_GPIO6
SMC_RUNTIME_SCI_L
SMC_EXTSMI_L

SATA GPIO
- GPIO21/SATA0GP AF19 — SB_GPIO21 — 100 — R2302
- GPIO19/SATA1GP AH18 — SB_GPIO19 — 100 — R2303
- GPIO36/SATA2GP AH19
- GPIO37/SATA3GP AE19 — SB_GPIO37 — 100 — R2305

SATA_C_DET_L

CLKS
- CLK14 AC1 — SB_CLK14P3M_TIMER
- CLK48 B2 — SB_CLK48M_USBCTLR
- SUSCLK C20 — TP_SB_SUS_CLK

SLP_S3* B24 — PM_SLP_S3_L
SLP_S4* D23 — PM_SLP_S4_L
SLP_S5* F22 — PM_SLP_S5_L
PWROK AA4 — PM_SB_PWROK
GPIO16/DPRSLPVR AC22 — PM_DPRSLPVR
TP0/BATLOW* C21 — NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN* C23 — PM_PWRBTN_L
LAN_RST* C19 — PM_LAN_ENABLE — NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* Y4

GPIO
- GPIO9 E20 — SMS_INT_L
- GPIO10 A20 — SMC_SB_NMI
- DEF=GPI GPIO12 F19 — LAN_ENERGY_DET
- GPIO13 E19
- DEF=GPI GPIO14 R4 — IDE_RESET_L
- GPIO15 E22 — SV_SET_UP
- GPIO24 R3 — CRB_SV_DET
- GPIO25 D20 — TP_SB_GPIO25_DO_NOT_USE
- OD GPIO35 AD21 — SB_CLK100M_SATA_OE_L
- GPIO36 AD20 — SB_GPUVCORE_DISABLE_L
- DEF=GPI GPIO39 AE20 — SATA_C_PWR_EN_L

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 350S AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

PP3V3_S5

R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

PM_BATLOW_L
PM_RSMRST_L
R2399 100K 5% 1/16W 402 MF-LF
SMC_WAKE_SCI_L

PP3V3_S5

R2306 10K 1/16W 402 MF-LF 5% NOSTUFF
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 0 1/16W 402 MF-LF 5% NOSTUFF

SV_SET_UP
CRB_SV_DET

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

PP3V3_S5

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 0 1/16W 402 MF-LF 5% NOSTUFF
R2311 10K 1/16W 402 MF-LF 5% NOSTUFF

FWH_MFG_MODE
BIOS_REC

PP3V3_S0

R2388 10K 5% 1/16W MF-LF 402

SATA_C_PWR_EN_L

SB: 3 OF 4

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	23	87

OMIT

U2100
ICH7-M
SB
BGA
(6 OF 6)

VSS

A4			AD3
A23			AD4
N24			AD7
P24			AD8
R18			AD15
U14			AD19
V27			AD23
AA24			AE2
AB27			AE4
AD11			AE8
B1			AE11
D10			AE13
F4			AE18
G18			AE21
J1			B8
L24			B11
M17			B14
N14			B17
N17			B20
N18			B26
N25			B28
N26			C2
P3			C6
P4			C27
P12			D13
P13			D18
P14			D21
P15			D24
P16			E1
P17			E2
P27			E4
P28			E8
R1			E15
R11			F3
R12			F5
R13			F12
R14			F27
R15			F28
R16			G1
R17			G2
T6			G5
T12			G6
T13			G9
T14			G14
T15			G21
T16			G24
T17			G25
U4			G26
U12			H3
U13			H4
U15			H5
U16			H24
U17			H27
U24			H28
U25			J2
U26			J5
V2			J24
V13			J25
V15			J26
V24			K24
V28			K27
W6			K28
W24			L13
W25			L15
W26			L25
Y3			L26
Y24			M3
Y27			M4
Y28			M5
AA1			M12
AA25			M13
AA26			M14
AB4			M15
AB6			M16
AB11			M24
AB14			M27
AB16			M28
AB19			N1
AB21			N2
AB24			N5
AB28			N6
AC2			N11
AC5			N12
AC9			N13
AC11			N15
AD1			N16
AE24			AG11
AE25			AG14
AF2			AG17
AF4			AG20
AF8			AG25
AF11			AH1
AF27			AH3
AF28			AH7
AG1			AH12
AG3			AH23
AG7			AH27

0 0

OMIT

U2100
ICH7-M
SB
BGA
(5 OF 6)

25D7 PP5V_S0_SB_V5REF	G10		
	AD17	V5REF	
25C7 PP5V_S5_SB_V5REF_SUS	F6	V5REF_SUS	
25B6 22C1 PP1V5_S0_SB_VCC1_5_B	AA22		
	AA23		
	AB22		
	AB23		
	AC23		
	AC24		
	AC25		
	AC26		
	AD26		
	AD27		
	AD28		
	D26		
	D27		
	D28		
	E24		
	E25		
	E26		
	F23		
	F24		
	G22		
	G23		
	H22	VCCA3GP	
	H23	VCC1_5_B	
	J22		
	J23		
	K22		
	K23		
	L22		
	L23		
	M22		
	M23		
	N22		
	N23		
	P22		
	P23		
	R22		
	R23		
	R24		
	R25		
	R26		
	T22		
	T23		
	T26		
	T27		
	T28		
	U22		
	U23		
	V22		
	V23		
	W22		
	W23		
	Y22		
	Y23		
52D5 82C6 82B3 82A4 79D3 66B6 66B5 66B1 49C4 49B5 40B6 36D6 34A8 33D8 33D3 25C8 25B8 25A4 25A3 24B5 24A5 24A3 23D7 23D3 23C3 22D3 21C3 24D1 60D4 60C7 58C7 58C4 57B6 54D4 54B5 52D3 49C7 49C4 49B5 40B6 36D6 34A8 33D8 33D3 25C8 25B8 25A4 25A3 24B5 24A5 24A3 23D7 23D3 23C3 22D3 21C3 24D1 79A8 71D2 67C5 67C3 67B3 67A3			
25A5 PP1V5_S0_SB_VCCDMIPLL	AG28	VCCDMIPLL	
25B6 25B2 25A8 24B5 24A5 24A3 9B7 8B7 5D4 5D1 67C8 67C6 66C5 62C1 62A8 48B6 25D6 25C8 25C6 25C2 PP1V5_S0	AB7		
	AC6		
	AC7		
	AD6	ARX	
	AE6	VCC1_5_A	
	AF5		
	AF6		
	AG5		
	AH5		
67C8 67C6 66C5 62C1 62A8 48B6 25D6 25C6 25C2 25B6 25B2 25A8 24B5 24A5 24A3 9B7 8B7 5D4 5D1 PP1V5_S0	AD2	VCCSATAPLL	
52D3 49C7 49C4 49B5 40B6 36D6 34A8 33D8 33D3 25C8 25B8 25B6 25A4 25A3 24B5 24A5 24A3 23D7 23D3 23C3 22D3 21C3 24D1 67B3 53C7 39A4 29A3 28A8 27D8 27D3 27C3 24D1 82D5 61A5 60D4 60C7 58C7 58C4 57B6 54D4 54B5 PP3V3_S0	AH11	VCC3_3	
67C8 67C6 66C5 62C1 62A8 48B6 25D6 25C8 25C6 25C2 25B6 25B2 25A8 24B5 24A5 24A3 9B7 8B7 5D4 5D1 PP1V5_S0	AB10		
	AB9		
	AC10		
	AD10	ATX	
	AE10	VCC1_5_A	
	AF10		
	AF9		
	AG9		
	AH9		
79D5 67D5 67D3 67C3 66C5 65D8 24B3 23D8 23D4 23C7 23B5 23A5 22C5 22B3 5D4 24A3 65D2 65D1 65C8 63D8 54B4 25C5 25D2 25C8 25B6 24C3 PP3V3_S5	E3	VCCSUS3_3	
25B6 25B2 25A8 24B5 24A5 24A3 9B7 8B7 5D4 5D1 67C8 67C6 66C5 62C1 62A8 48B6 25D6 25C8 25C6 25C2 PP1V5_S0	C1	VCCUSBPLL	
VOLTAGE GENERATED INTERNALLY SO NO CONNECT HERE	AA2		
	Y7	VCCLAN1_5 CHANGE SYMBOL TO 1.05	

	L11		
PP1V05_S0	L12		
	L14		
	L16		
	L17		
	L18		
	M11		
	M18		
	P11	CORE	
	P18	VCC1_05	
	T11		
	T18		
	U11		
	U18		
	V11		
	V12		
	V14		
	V16		
	V17		
	V18		
PP3V3_S0	V5		
	V1	VCC_PAUX	
	W2	VCCLAN_3_3	
	W7		
PP3V3_S0	U6	VCC3_3/VCCHDA	
PP3V3_S5	R7	VCCSUS3_3/VCCSUSHDA	
PP1V05_S0	AE23		
	AE26	V_CPU_IO	
	AH26		
PP3V3_S0	AA7		
	AB12		
	AB20		
	AC16	IDE	
	AD13	VCC3_3	
	AD18		
	AG12		
	AG15		
	AG19		
	A5		
	B13		
	B16		
	B7	PCI	
	C10	VCC3_3	
	D15		
	F9		
	G11		
	G12		
PP3V3_S0	G16		
PP3V3_G3C_SB_RTC_D	W5	VCCRTC	
PP3V3_S5	P7		
	A24		
	C24		
	D19	VCCSUS3_3	
	D22		
	G19		
	K3		
	K4		
	K5		
	K6	USB	
	L1	VCCSUS3_3	
	L2		
	L3		
	L6		
	L7		
	M6		
	M7		
PP3V3_S5	N7		
	AB17		
	AC17	VCC1_5_A	
	T7		
	F17	VCC1_5_A	
PP1V5_S0	G17		
	AB8		
	AC8	VCC1_5_A	
	K7		
VOLTAGE GENERATED INTERNALLY SO NO CONNECT HERE	C28	VCCSAUS1_5 CHANGE SYMBOL TO 1.05	
	G20		
	A1		
	H6		
	H7	USB CORE	
	J6	VCC1_5_A	
PP1V5_S0	J7		

NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

NOTE:
VCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

SB: 4 OF 4

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 24 OF 87	

ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
PP1V5_S0
C2511 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AG5

PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB

ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
PP1V05_S0
C2518 0.1UF 10% 16V X5R 402
C2502 1UF 10% 6.3V CERM 402
C2516 330UF 20% 2.5V POLY CASE-C2
PLACEHOLDER FOR 270UF

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PP3V3_S5
C2531 0.1UF 10% 16V X5R 402
C2534 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PINS A24 ... G19 AND P7 OF SB

R2502 100 1/16W MF-LF 402 5%
PP3V3_S0
PP5V_S0
D2502 BAT54DW SOT-363
ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
PP5V_S0_SB_V5REF
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2503 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB ON SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
PP1V5_S0
C2517 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AD2

ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
PP3V3_S0
C2519 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS V1, V5, W2, OR W7

ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
PP3V3_S5
C2533 0.1UF 10% 16V X5R 402
C2532 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PINS K3 ... N7 OF SB

R2501 10 1/16W MF-LF 402 5%
PP3V3_S5
PP5V_S5
D2502 BAT54DW SOT-363
ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
PP5V_S5_SB_V5REF_SUS
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2504 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB ON SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PP3V3_S0
C2513 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AH11

ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
PP3V3_S0
C2521 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN U6

ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
PP1V5_S0
C2514 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AG9

ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
PP1V5_S0
C2510 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PINS AB8 AND AC8 OF SB

L2500 100-OHM-EMI SM-3
ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
PP1V5_S0_SB_VCC1_5_B
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2500 220UF 20% 2.5V POLY CASE-B2
C2505 0.1UF 10% 16V X5R 402
C2506 0.1UF 10% 16V X5R 402
C2507 0.1UF 10% 16V X5R 402
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PP3V3_S5
C2520 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB ON SECONDARY SIDE OR 3.56MM ON PRIMARY NEAR PINS D28, T28, AD28

ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
PP1V05_S0
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB
C2523 0.1UF 10% 16V X5R 402
C2522 0.1UF 10% 16V X5R 402
C2524 4.7UF 20% 6.3V CERM 603

ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
PP1V5_S0
C2512 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PINS A1 ... J7

ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
PP3V3_S0
C2525 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PINS AA7 ... AG19

ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
PP1V5_S0
C2515 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB

ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PP3V3_S0
C2509 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB

ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
PP3V3_S0
C2526 0.1UF 10% 16V X5R 402
C2527 0.1UF 10% 16V X5R 402
C2528 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB NEAR PINS A5 ... G16

ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
PP3V3_G3C_SB_RTC_D
C2530 0.1UF 10% 16V X5R 402
C2529 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB

R2500 1/10W 5% MF-LF 603
PP1V5_S0
PP1V5_S0_SB_VCCDMIPLL_F
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
L2507 0.28-OHM 1206
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
PP1V5_S0_SB_VCCDMIPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2501 0.01UF 10% 16V CERM 402
C2508 10UF 20% 6.3V X5R 603
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY SIDE OR 3.56MM ON PRIMARY

SB: 4 OF 4

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

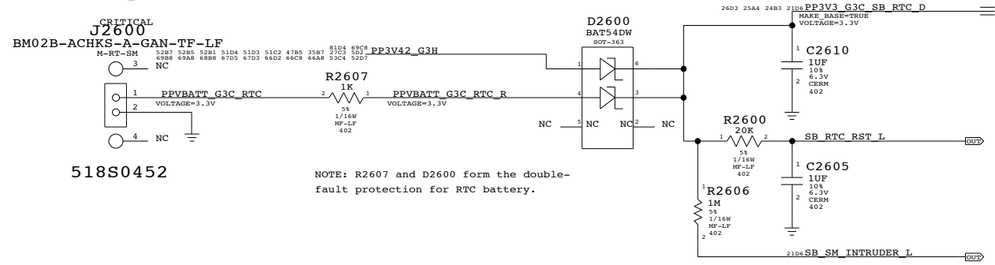
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

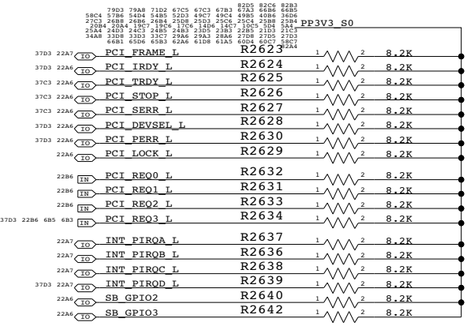
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 25 OF 87	

RTC Battery Connector



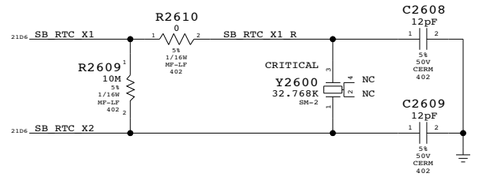
518S0452

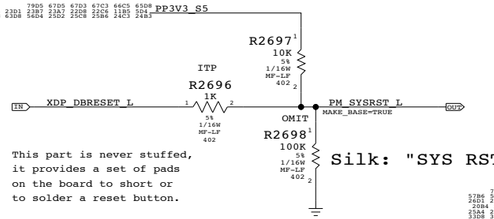
NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



Pullup on SB_GPIO4 removed as it now defaults low for use as DVI_HPD in muxed graphics solution.

SB RTC Crystal Circuit



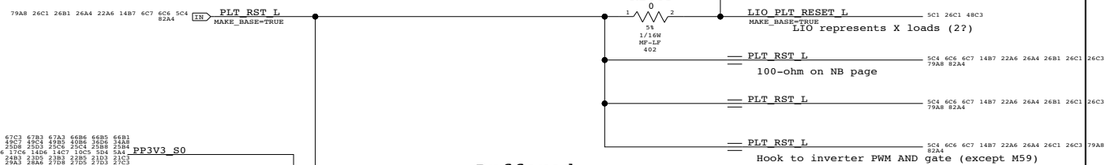


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

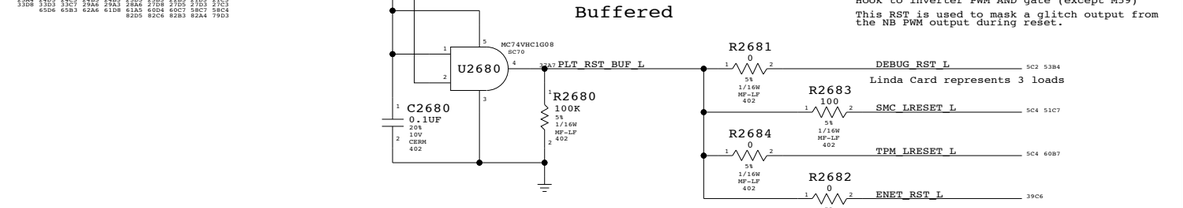
Silk: "SYS RST"

Platform Reset Connections

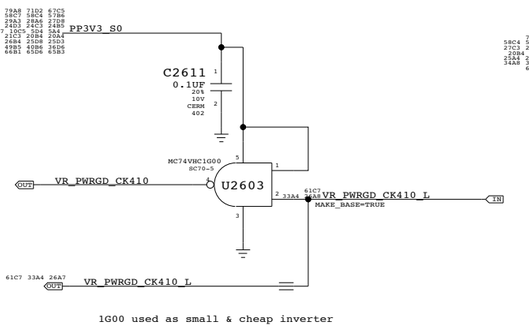
Unbuffered



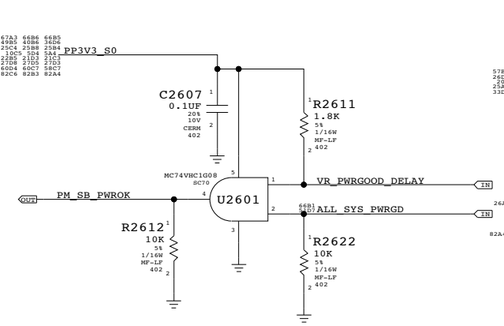
Buffered

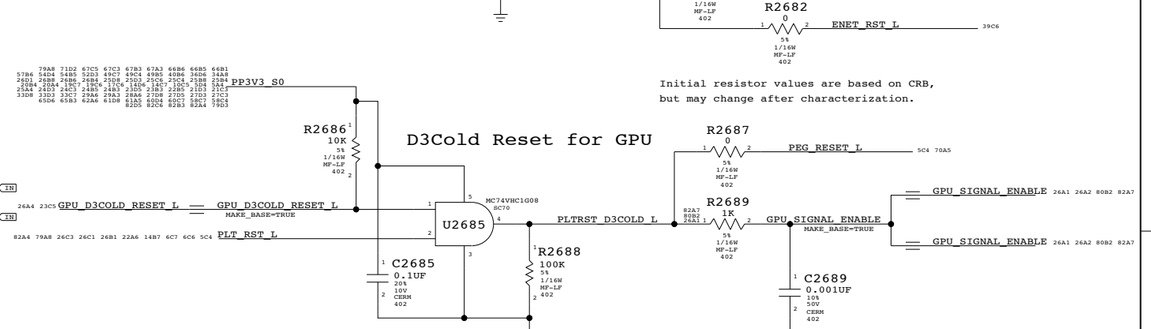


Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter





SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

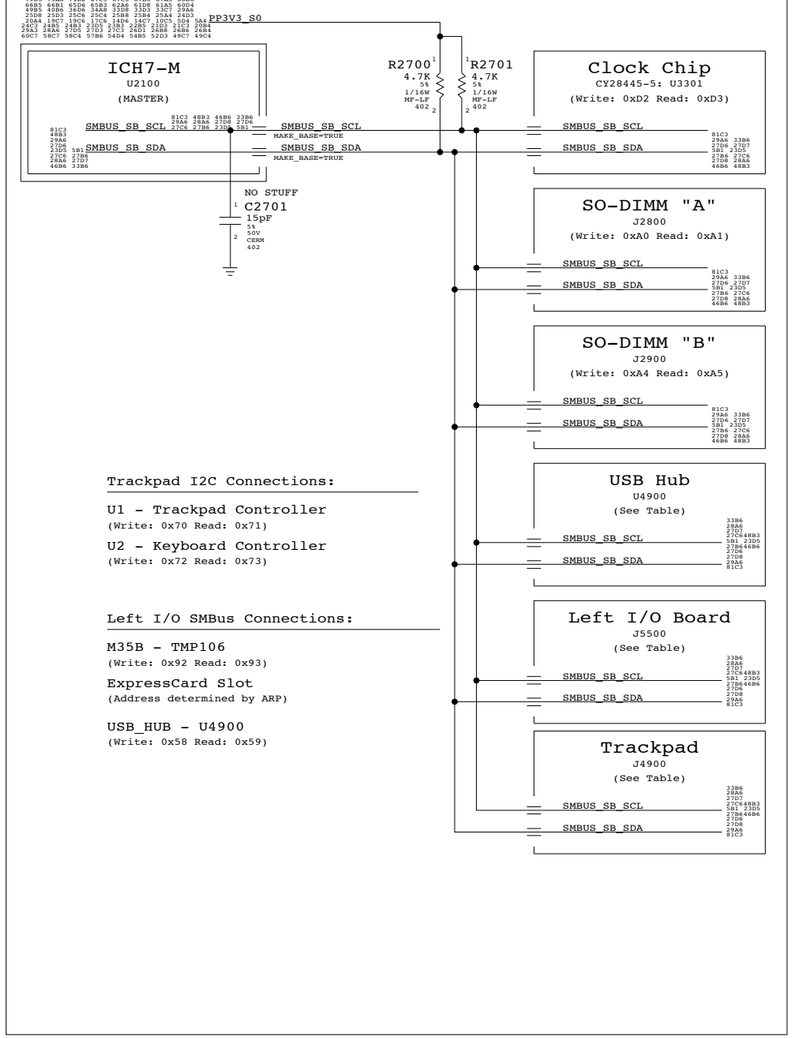
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	26	87

ICH7-M SMBus Connections



Trackpad I2C Connections:

U1 - Trackpad Controller
(Write: 0x70 Read: 0x71)

U2 - Keyboard Controller
(Write: 0x72 Read: 0x73)

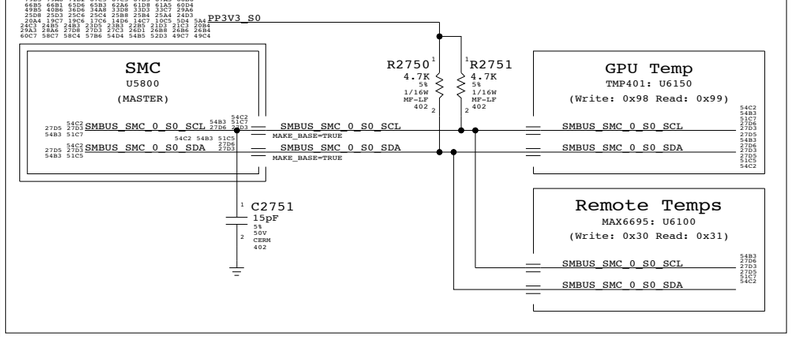
Left I/O SMBus Connections:

M35B - TMP106
(Write: 0x92 Read: 0x93)

ExpressCard Slot
(Address determined by ARP)

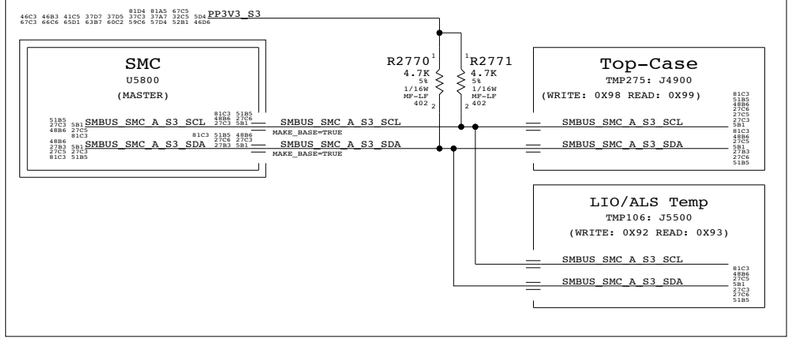
USB_HUB - U4900
(Write: 0x58 Read: 0x59)

SMC "0" SMBus Connections

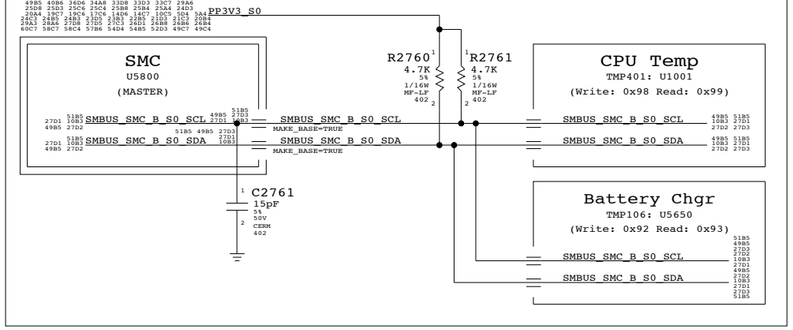


SMC "A" SMBus Connections

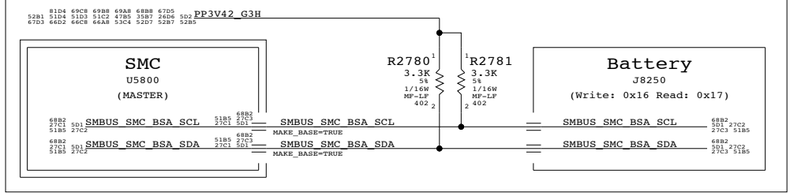
NOTE: SMC RMT bus remains powered and may be active in S3 state



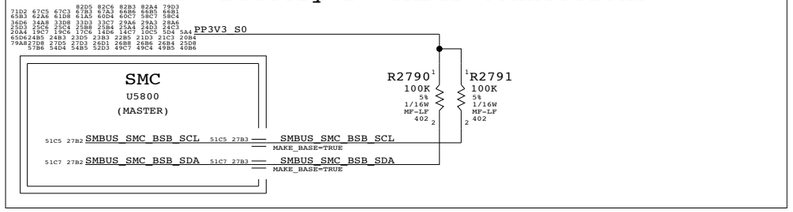
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M57 SMBUS CONNECTIONS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 27 OF 87

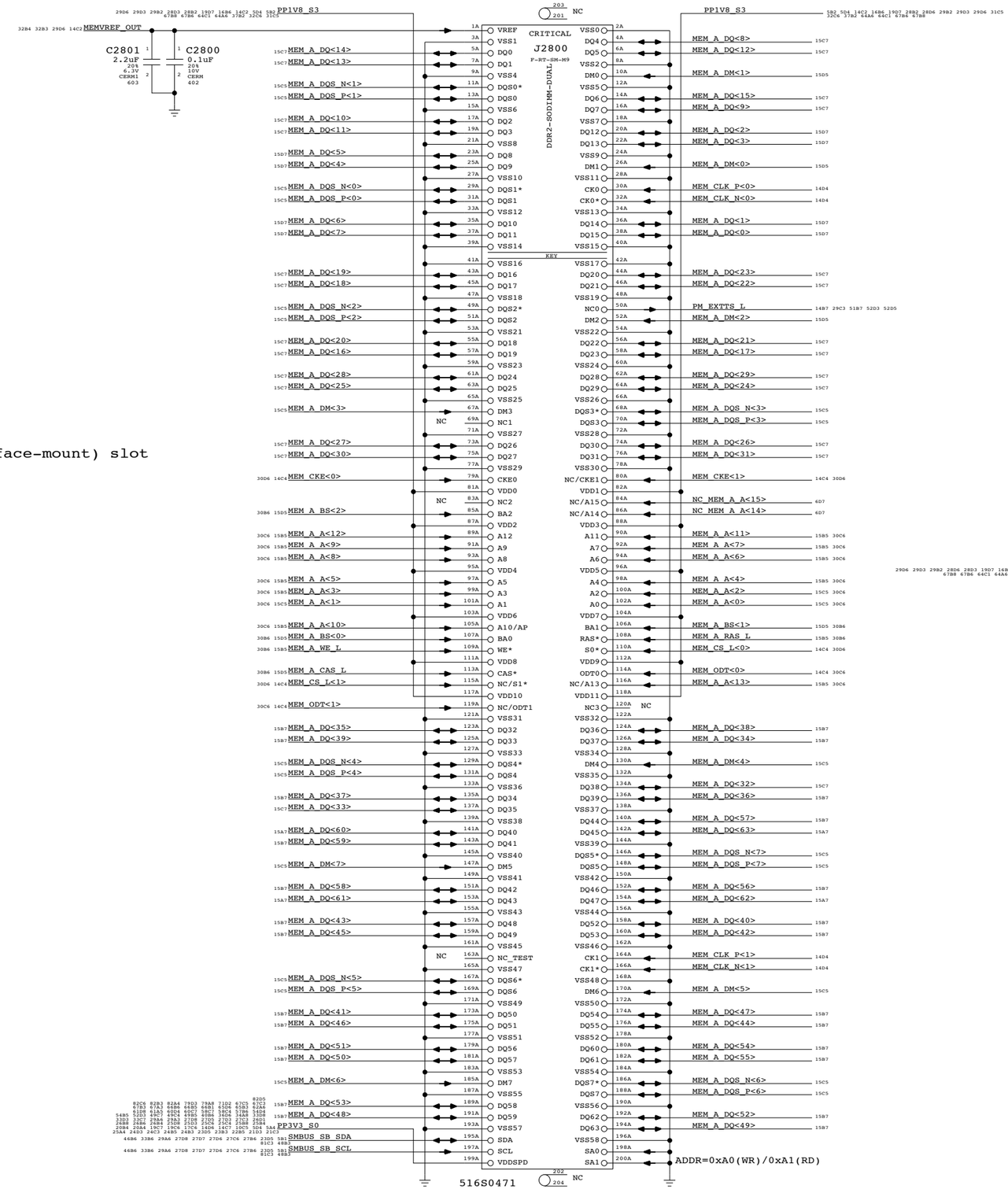
Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

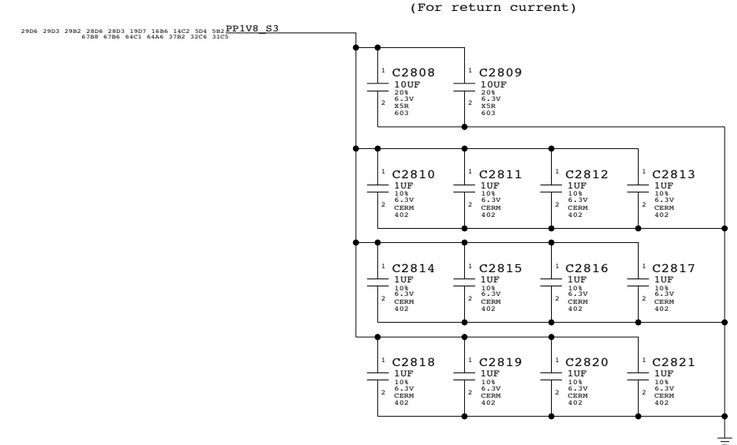
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE NONE SHT 28 OF 87

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Factory" (thru-hole) slot

MEMVREF_OUT

C2901 2.2uF 20% 6.3V CERM1 603

C2900 0.1uF 20% 10V CERM 402

PP1V8_S3

CRITICAL
J2900
F-RT-TH1
DDR2-SODIMM-DUAL

	1	VREF		2	VSS0		
	3	VSS1		4	DQ4	MEM_B_DQ<9>	15C4
MEM_B_DQ<15>	5	DQ0		6	DQ5	MEM_B_DQ<11>	15C4
MEM_B_DQ<14>	7	DQ1		8	VSS2		
	9	VSS4		10	DM0	MEM_B_DM<1>	15D2
MEM_B_DQS_N<1>	11	DQS0*		12	VSS5		
MEM_B_DQS_P<1>	13	DQS0		14	DQ6	MEM_B_DQ<12>	15C4
	15	VSS6		16	DQ7	MEM_B_DQ<8>	15C4
MEM_B_DQ<10>	17	DQ2		18	VSS7		
MEM_B_DQ<13>	19	DQ3		20	DQ12	MEM_B_DQ<3>	15D4
	21	VSS8		22	DQ13	MEM_B_DQ<6>	15D4
MEM_B_DQ<7>	23	DQ8		24	VSS9		
MEM_B_DQ<2>	25	DQ9		26	DM1	MEM_B_DM<0>	15D2
	27	VSS10		28	VSS11		
MEM_B_DQS_N<0>	29	DQS1*		30	CK0	MEM_CLK_P<3>	14D4
MEM_B_DQS_P<0>	31	DQS1		32	CK0*	MEM_CLK_N<3>	14D4
	33	VSS12		34	VSS13		
MEM_B_DQ<1>	35	DQ10		36	DQ14	MEM_B_DQ<0>	15D4
MEM_B_DQ<4>	37	DQ11		38	DQ15	MEM_B_DQ<5>	15D4
	39	VSS14		40	VSS15		
		KEY					
	41	VSS16		42	VSS17		
MEM_B_DQ<21>	43	DQ16		44	DQ20	MEM_B_DQ<22>	15C4
MEM_B_DQ<19>	45	DQ17		46	DQ21	MEM_B_DQ<18>	15C4
	47	VSS18		48	VSS19		
MEM_B_DQS_N<2>	49	DQS2*		50	NC0	PM_EXTTS_L	14B7 28C3 51B7 52D3 52D5
MEM_B_DQS_P<2>	51	DQS2		52	DM2	MEM_B_DM<2>	15D2
	53	VSS21		54	VSS22		
MEM_B_DQ<20>	55	DQ18		56	DQ22	MEM_B_DQ<17>	15C4
MEM_B_DQ<23>	57	DQ19		58	DQ23	MEM_B_DQ<16>	15C4
	59	VSS23		60	VSS24		
MEM_B_DQ<29>	61	DQ24		62	DQ28	MEM_B_DQ<26>	15C4
MEM_B_DQ<24>	63	DQ25		64	DQ29	MEM_B_DQ<28>	15C4
	65	VSS25		66	VSS26		
MEM_B_DM<3>	67	DM3		68	DQS3*	MEM_B_DQS_N<3>	15C2
NC	69	NC1		70	DQS3	MEM_B_DQS_P<3>	15C2
	71	VSS27		72	VSS28		
MEM_B_DQ<27>	73	DQ26		74	DQ30	MEM_B_DQ<31>	15C4
MEM_B_DQ<25>	75	DQ27		76	DQ31	MEM_B_DQ<30>	15C4
	77	VSS29		78	VSS30		
MEM_CKE<2>	79	CKE0		80	NC/CKE1	MEM_CKE<3>	14C4 30D6
	81	VDD0		82	VDD1		
NC	83	NC2		84	NC/A15	NC_MEM_B_A<15>	6D7
MEM_B_BS<2>	85	BA2		86	NC/A14	NC_MEM_B_A<14>	6D7
	87	VDD2		88	VDD3		
MEM_B_A<12>	89	A12		90	A11	MEM_B_A<11>	15B2 30B6
MEM_B_A<9>	91	A9		92	A7	MEM_B_A<7>	15B2 30B6
MEM_B_A<8>	93	A8		94	A6	MEM_B_A<6>	15B2 30B6
	95	VDD4		96	VDD5		
MEM_B_A<5>	97	A5		98	A4	MEM_B_A<4>	15B2 30B6
MEM_B_A<3>	99	A3		100	A2	MEM_B_A<2>	15C2 30B6
MEM_B_A<1>	101	A1		102	A0	MEM_B_A<0>	15C2 30B6
	103	VDD6		104	VDD7		
MEM_B_A<10>	105	A10/AP		106	BA1	MEM_B_BS<1>	15D2 30A6
MEM_B_BS<0>	107	BA0		108	RAS*	MEM_B_RAS_L	15B2 30A6
MEM_B_WE_L	109	WE*		110	S0*	MEM_CS_L<2>	14C4 30D6
	111	VDD8		112	VDD9		
MEM_B_CAS_L	113	CAS*		114	ODT0	MEM_ODT<2>	14C4 30C6
MEM_CS_L<3>	115	NC/S1*		116	NC/A13	MEM_B_A<13>	15B2 30B6
	117	VDD10		118	VDD11		
MEM_ODT<3>	119	NC/ODT1		120	NC3	NC	
	121	VSS31		122	VSS32		
MEM_B_DQ<36>	123	DQ32		124	DQ36	MEM_B_DQ<32>	15C4
MEM_B_DQ<33>	125	DQ33		126	DQ37	MEM_B_DQ<37>	15B4
	127	VSS33		128	VSS34		
MEM_B_DQS_N<4>	129	DQS4*		130	DM4	MEM_B_DM<4>	15C2
MEM_B_DQS_P<4>	131	DQS4		132	VSS35		
	133	VSS36		134	DQ38	MEM_B_DQ<38>	15B4
MEM_B_DQ<34>	135	DQ34		136	DQ39	MEM_B_DQ<39>	15B4
MEM_B_DQ<35>	137	DQ35		138	VSS37		
	139	VSS38		140	DQ44	MEM_B_DQ<44>	15B4
MEM_B_DQ<40>	141	DQ40		142	DQ45	MEM_B_DQ<45>	15B4
MEM_B_DQ<41>	143	DQ41		144	VSS39		
	145	VSS40		146	DQS5*	MEM_B_DQS_N<5>	15C2
MEM_B_DM<5>	147	DM5		148	DQS5	MEM_B_DQS_P<5>	15C2
	149	VSS41		150	VSS42		
MEM_B_DQ<42>	151	DQ42		152	DQ46	MEM_B_DQ<46>	15B4
MEM_B_DQ<43>	153	DQ43		154	DQ47	MEM_B_DQ<47>	15B4
	155	VSS43		156	VSS44		
MEM_B_DQ<62>	157	DQ48		158	DQ52	MEM_B_DQ<58>	15B4
MEM_B_DQ<59>	159	DQ49		160	DQ53	MEM_B_DQ<63>	15A4
	161	VSS45		162	VSS46		
NC	163	NC_TEST		164	CK1	MEM_CLK_P<2>	14D4
	165	VSS47		166	CK1*	MEM_CLK_N<2>	14D4
MEM_B_DQS_N<7>	167	DQS6*		168	VSS48		
MEM_B_DQS_P<7>	169	DQS6		170	DM6	MEM_B_DM<7>	15C2
	171	VSS49		172	VSS50		
MEM_B_DQ<60>	173	DQ50		174	DQ54	MEM_B_DQ<56>	15B4
MEM_B_DQ<61>	175	DQ51		176	DQ55	MEM_B_DQ<57>	15B4
	177	VSS51		178	VSS52		
MEM_B_DQ<54>	179	DQ56		180	DQ60	MEM_B_DQ<55>	15B4
MEM_B_DQ<51>	181	DQ57		182	DQ61	MEM_B_DQ<50>	15B4
	183	VSS53		184	VSS54		
MEM_B_DM<6>	185	DM7		186	DQS7*	MEM_B_DQS_N<6>	15C2
	187	VSS55		188	DQS7	MEM_B_DQS_P<6>	15C2
MEM_B_DQ<52>	189	DQ58		190	VSS56		
MEM_B_DQ<49>	191	DQ59		192	DQ62	MEM_B_DQ<53>	15B4
	193	VSS57		194	DQ63	MEM_B_DQ<48>	15B4
SMBUS_SB_SDA	195	SDA		196	VSS58	Resistor prevents pwr-gnd short	
SMBUS_SB_SCL	197	SCL		198	SA0		
	199	VDDSPD		200	SA1	SODIMM_A_SA1	

PP3V3_S0

ADDR=0xA4(WR)/0xA5(RD)

516-0140

201 NC

202 NC

DDR2 Bypass Caps

(For return current)

PP1V8_S3

C2908	10UF	20% 6.3V X5R	603
C2909	10UF	20% 6.3V X5R	603
C2910	1UF	10% 6.3V CERM	402
C2911	0.1uF	20% 10V CERM	402
C2912	1UF	10% 6.3V CERM	402
C2913	1UF	10% 6.3V CERM	402
C2914	1UF	10% 6.3V CERM	402
C2915	1UF	10% 6.3V CERM	402
C2916	1UF	10% 6.3V CERM	402
C2917	0.1uF	20% 10V CERM	402
C2918	0.1uF	20% 10V CERM	402
C2919	0.1uF	20% 10V CERM	402
C2920	0.1uF	20% 10V CERM	402
C2921	0.1uF	20% 10V CERM	402

PP3V3_S0

R2900 10K 5% 1/16W MF-LF 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

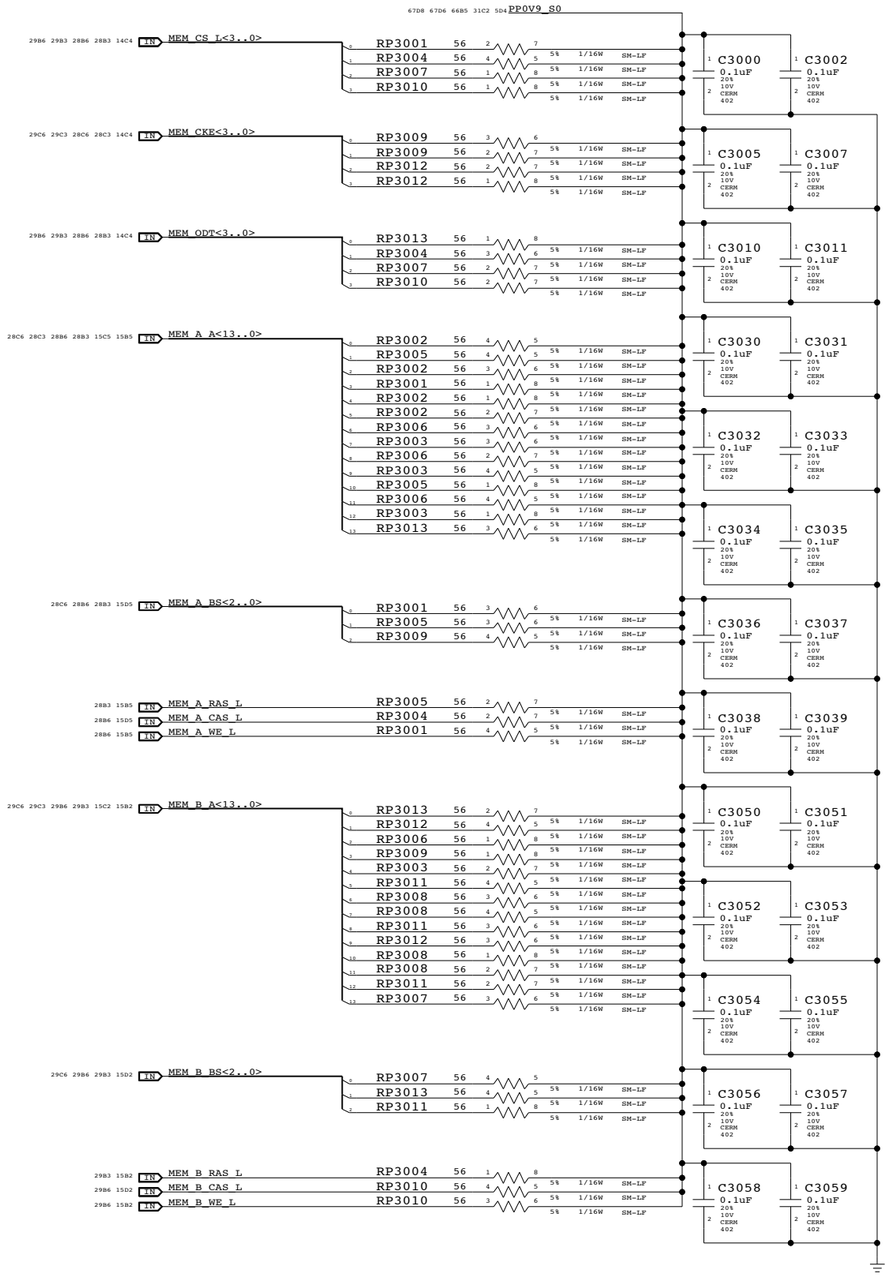
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 29 OF 87	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	30	87

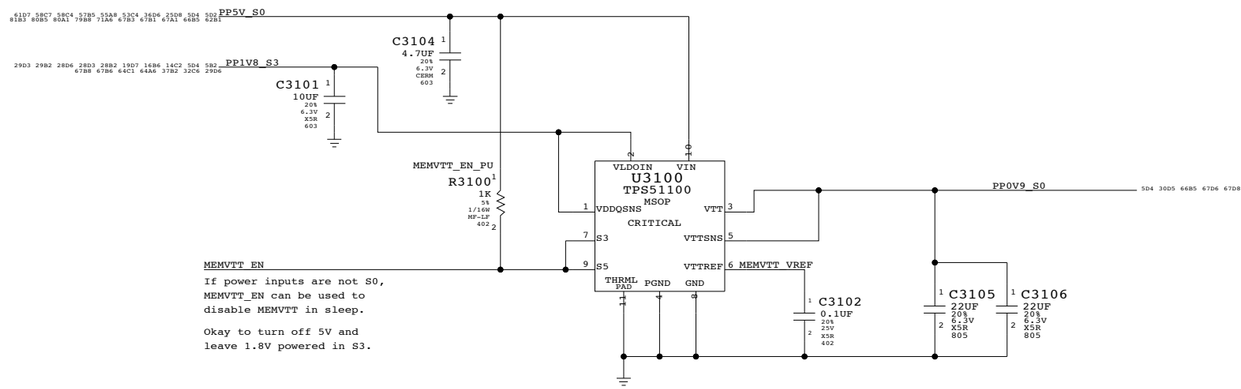
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

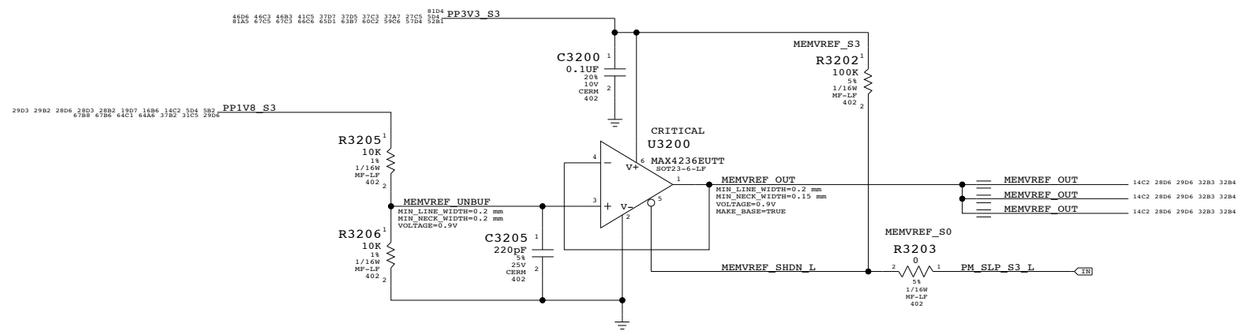
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	31	87



DDR2 VRef

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

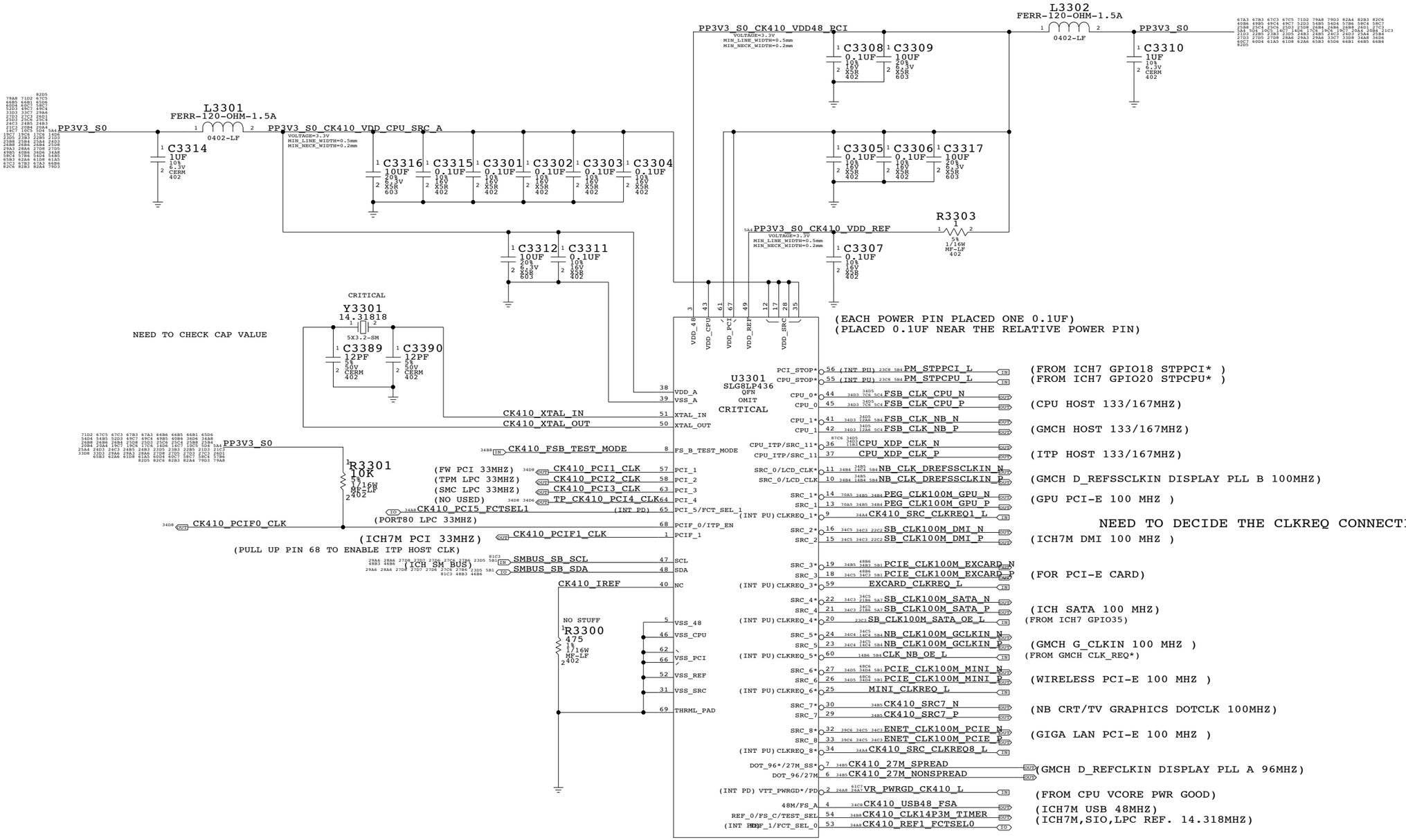
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE

SHT 32 OF 87



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

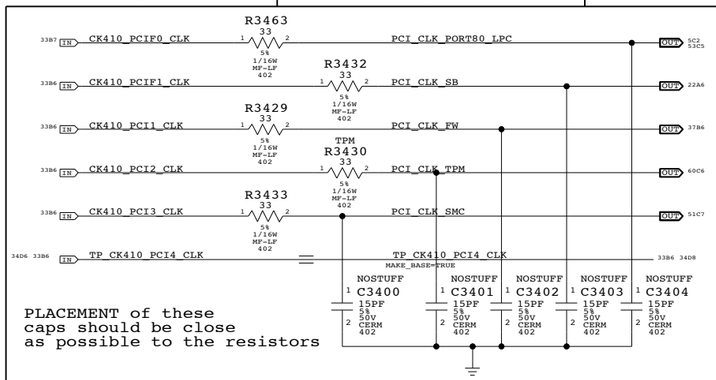
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

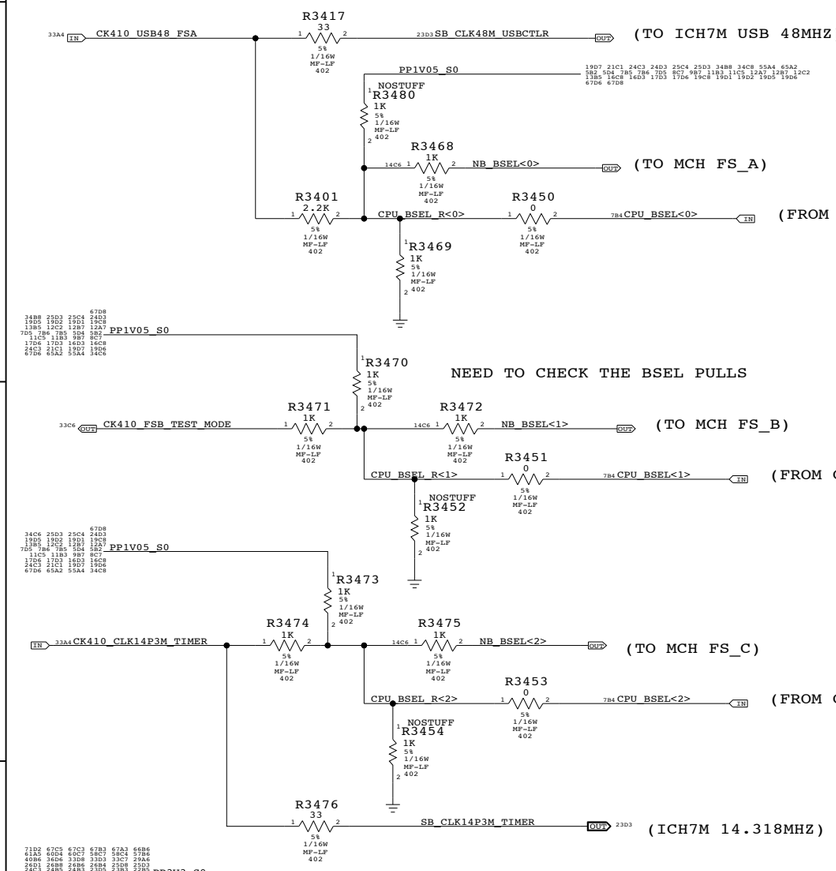
II NOT TO REPRODUCE OR COPY IT

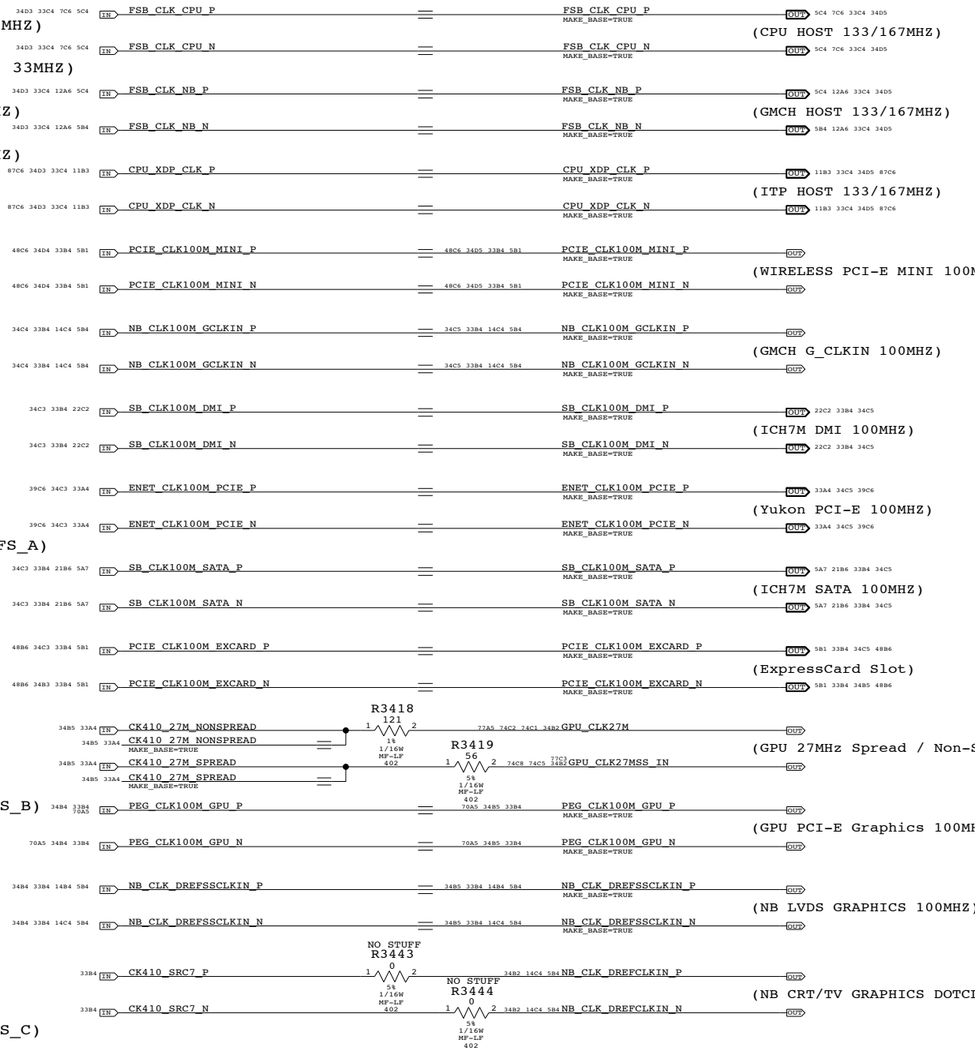
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

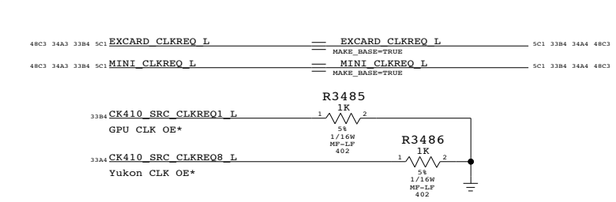
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 33 OF 87	









NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

FS_C	FS_B	FS_A	CPU
0	0	0	266M
# 0	0	1	133M
# 0	1	0	166M
0	1	1	200M
1	0	0	100M
1	0	1	333M
1	1	0	400M
1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED

Clock Termination

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

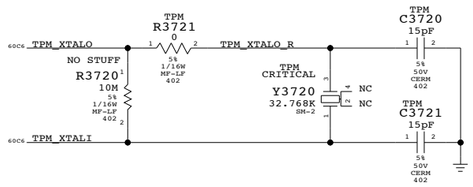
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

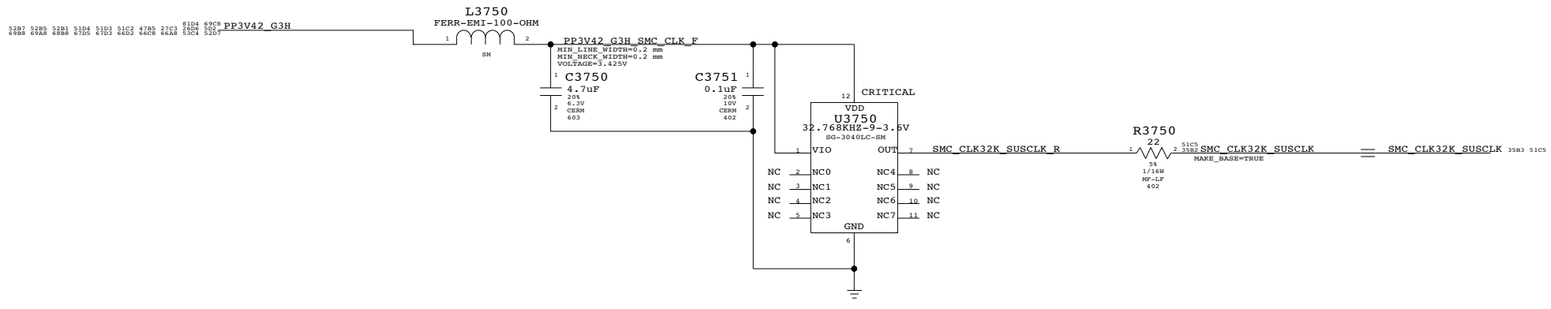
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 34 OF 87	

TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

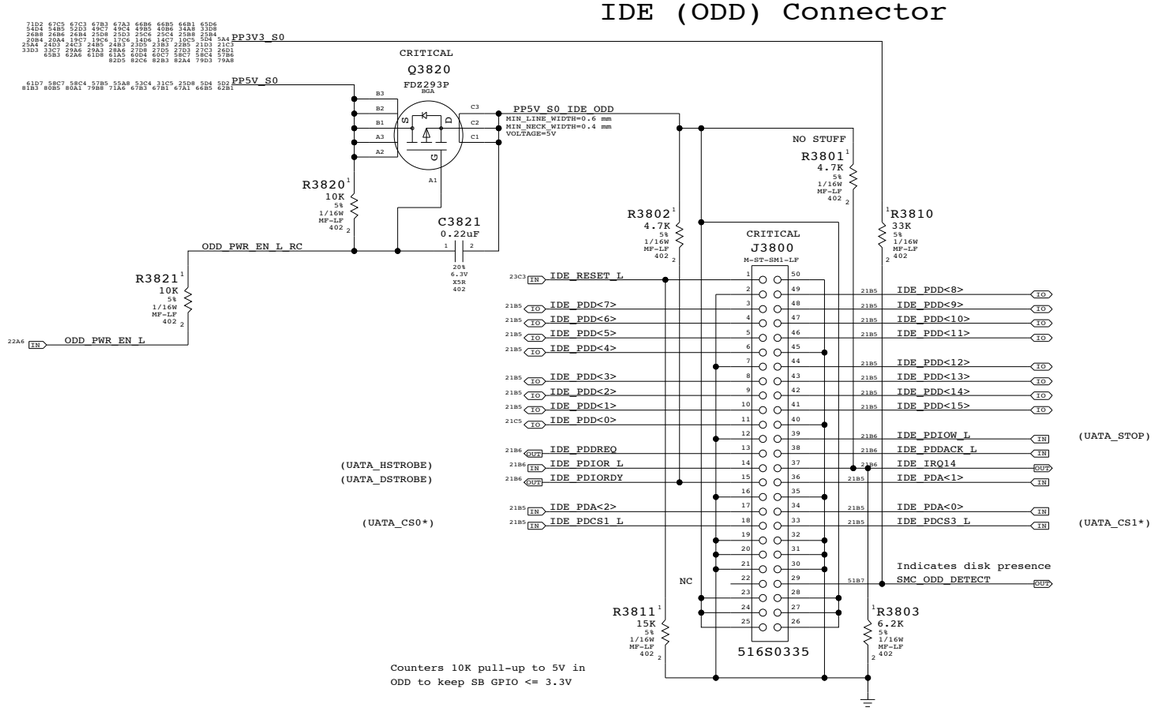
II NOT TO REPRODUCE OR COPY IT

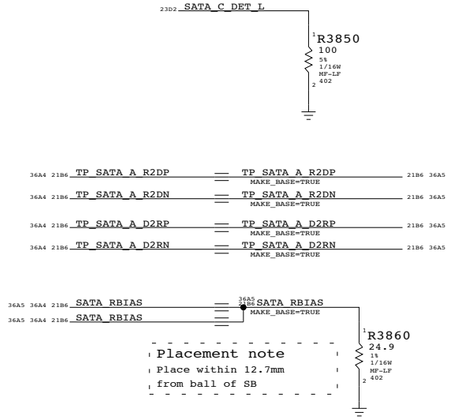
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 35 OF 87	

IDE (ODD) Connector





PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

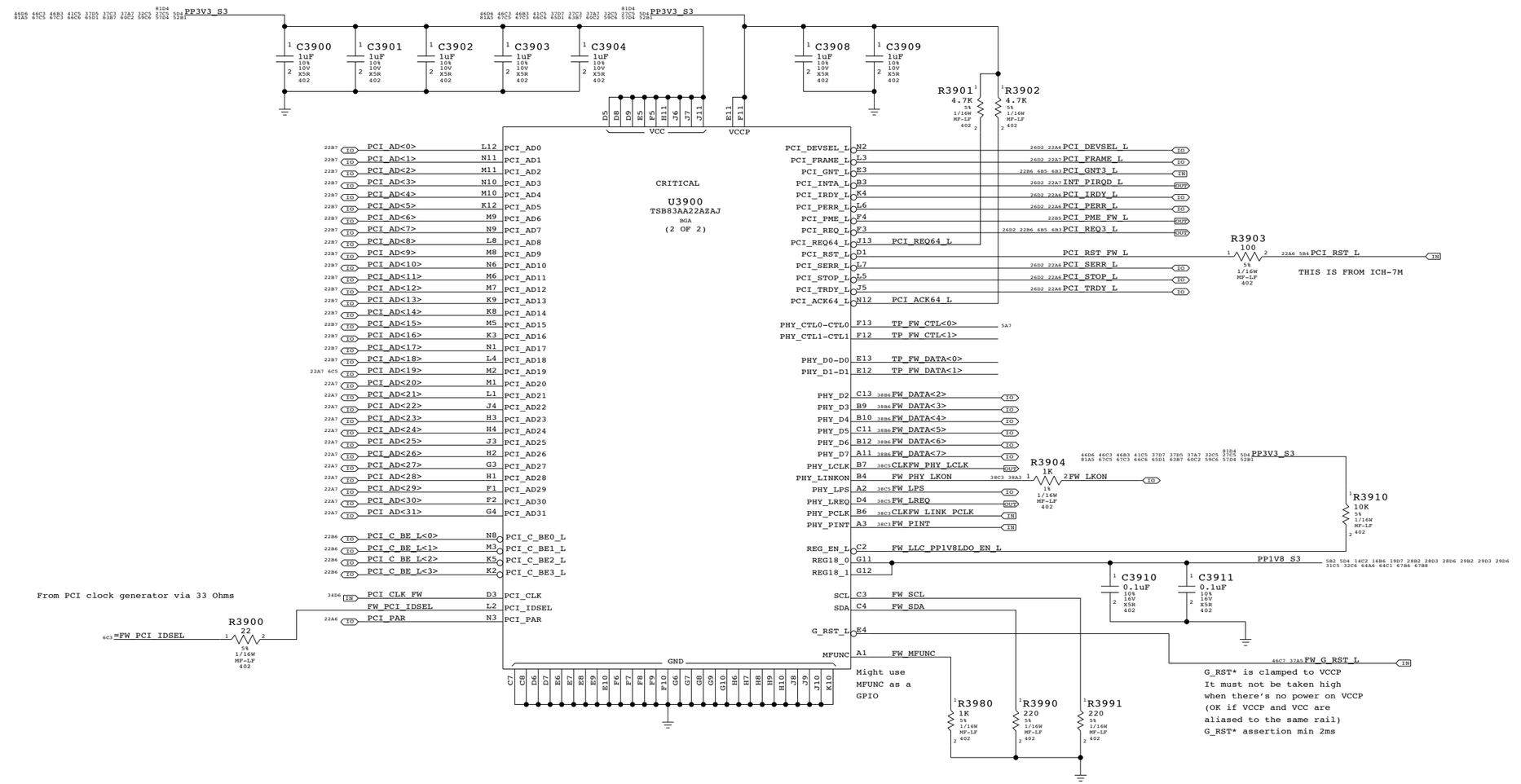
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 36 OF 87	



FireWire Link (TSB83AA22)

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

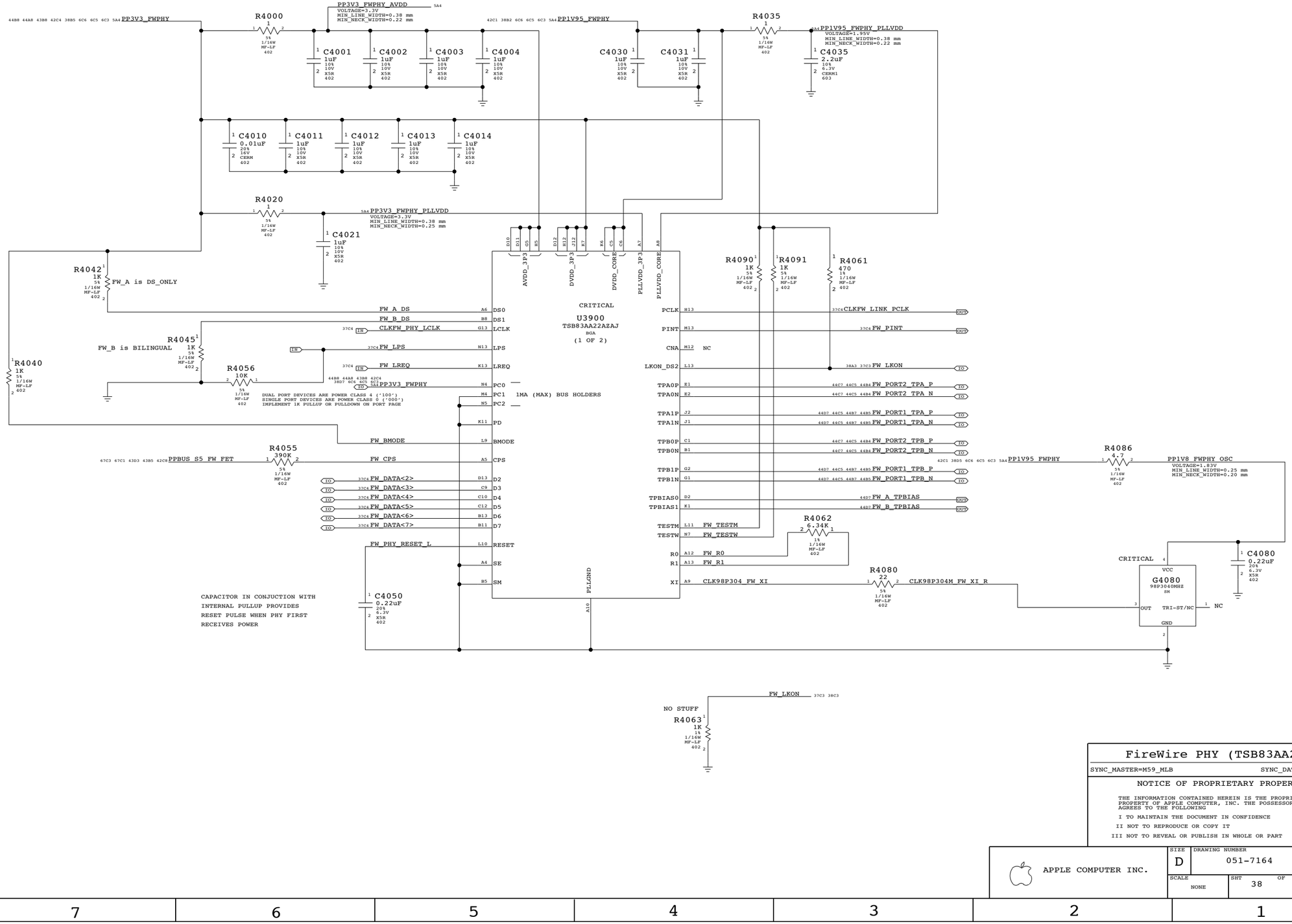
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 37 OF 87	



FireWire PHY (TSB83AA22)

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

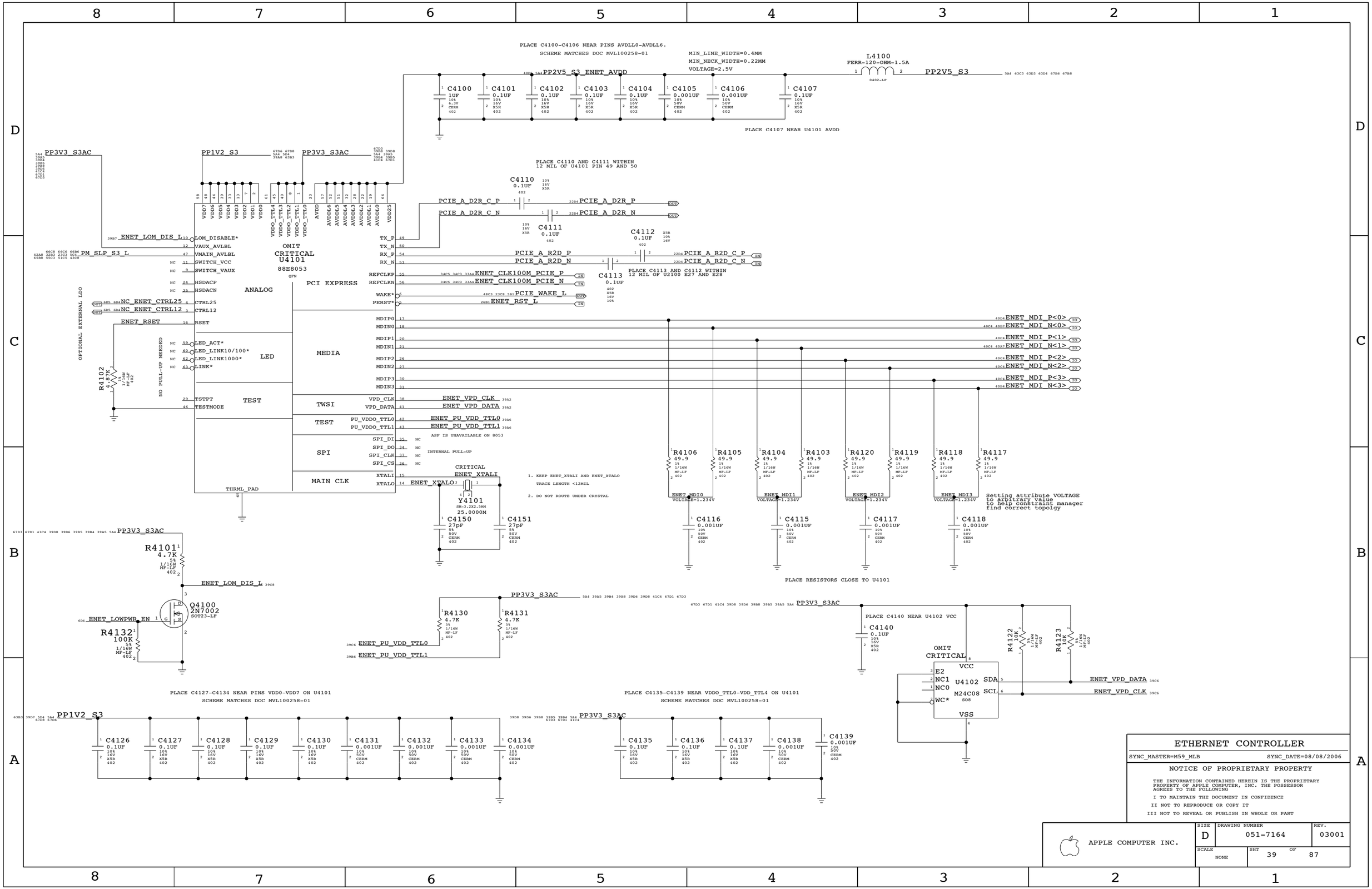
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 38 OF 87	



ETHERNET CONTROLLER

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 39 OF 87	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0> 40D3
	ENETCONN	ENET_100D	ENETCONN_N<0> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<1> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<1> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<2> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<2> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<3> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<3> 40B3

Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

39D5 5A4 PP2V5_S3_ENET_AVDD

Place one cap at each pin of transformer

C4200 1uF 10% 6.3V CERM 402
C4201 1uF 10% 6.3V CERM 402
C4202 1uF 10% 6.3V CERM 402
C4203 1uF 10% 6.3V CERM 402

Transformers should be mirrored on opposite sides of the board

T4200 1000BT-824-00275 XFR-SM CRITICAL
T4201 1000BT-824-00275 XFR-SM CRITICAL
SYM_VER2

39C3 ENET_MDI_P<0>
40B7 39C3 ENET_MDI_N<0>
39C3 ENET_MDI_P<1>
40A7 39C3 ENET_MDI_N<1>
39C3 ENET_MDI_P<2>
39C3 ENET_MDI_N<2>
39C3 ENET_MDI_P<3>
39C3 ENET_MDI_N<3>

NC1 NC2 CHAS SIDE NC4 NC3 LINE SIDE

40D7 ENETCONN_P<0>
40D7 ENETCONN_N<0>
40D7 ENETCONN_P<1>
40D7 ENETCONN_N<1>
40D7 ENETCONN_P<2>
40D7 ENETCONN_N<2>
40D7 ENETCONN_P<3>
40D7 ENETCONN_N<3>

ENET_CTAP0
ENET_CTAP1
ENET_CTAP2
ENET_CTAP3

CRITICAL
J4200 JM36113-P2054-7F F-RT2-TH-RJ45
514-0277 Short shielded RJ-45

NO STUFF
R4210 0 5% 1/16W MF-LF 402
Place close to connector

R4200 R4201 R4202 R4203 75 5% 1/16W MF-LF 402

ENET_CTAP_COMMON
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

C4204 100pF 10% 16V X5R CERM 1808
GND_CHASSIS_ENET 40F7

LAN ENERGY DETECT

PP3V3_S0

R4227 470K 1% 1/16W MF-LF 402
R4223 3.3K 5% 1/16W MF-LF 402
R4228 392K 1% 1/16W MF-LF 402
R4224 100K 1% 1/16W MF-LF 402
C4223 0.1uF 10% 10V X5R 402

C4220 68PF 5% 50V CERM 402-1
R4220 2.4K 5% 1/16W MF-LF 402
40C4 39C3 ENET_MDI_N<0>
ED_MDIN0_C VOLTAGE=1.234V

C4221 68PF 5% 50V CERM 402-1
R4221 2.4K 5% 1/16W MF-LF 402
40C4 39C3 ENET_MDI_N<1>
ED_MDIN1_C VOLTAGE=1.234V

EDET_MDIN_AMP
ED_MDIN_R

Q4220 MMDT3904XF SOT-363-LF

NO STUFF
C4222 100pF 5% 50V CERM 402

R4225 51.1K 1% 1/16W MF-LF 402

U4200 LMC7211 SM-LF
EDET_ACT
EDET_REF
V+ V-
LAN_ENERGY_DET 23C3

R4226 10K 5% 1/16W MF-LF 402

Setting attribute VOLTAGE to arbitrary value to help constraint manager find correct topolgy

PLACE C4220 & C4221
NEAR ENET_MDI_N<0/1>

Ethernet Connector

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

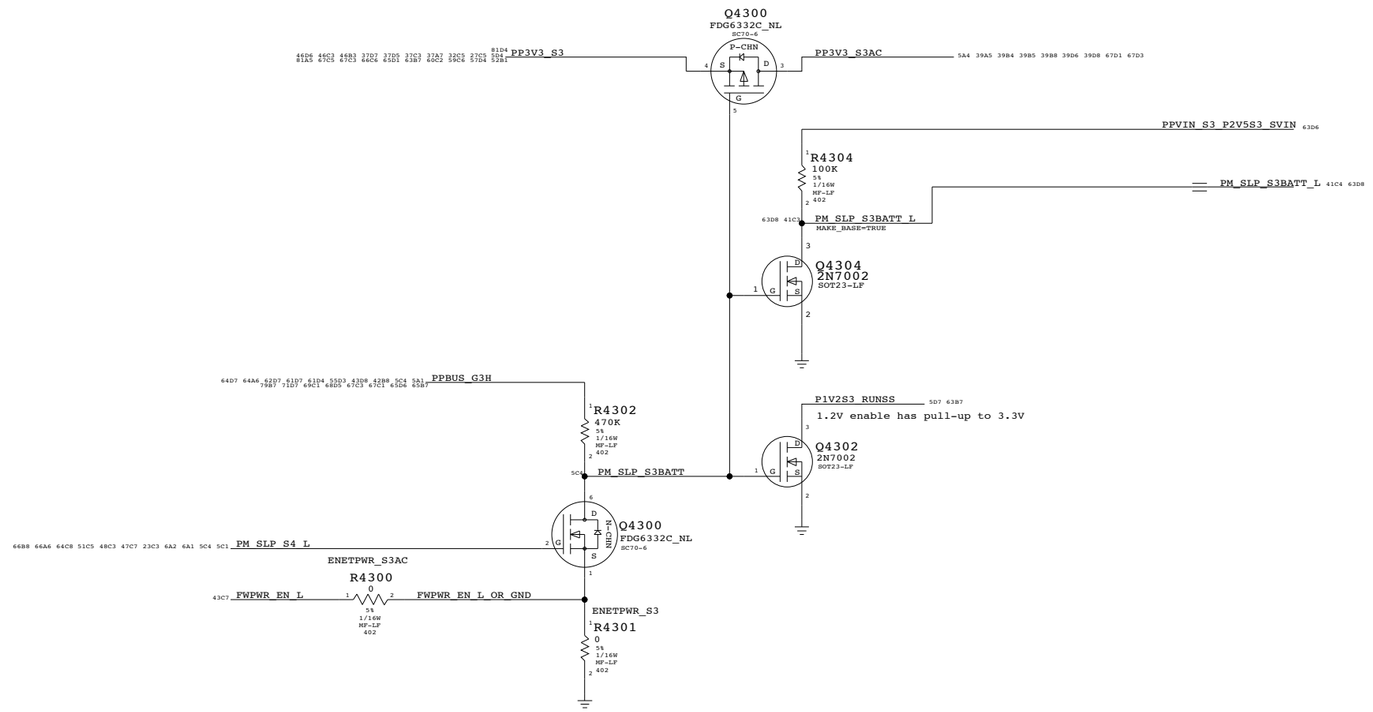
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 40 OF 87	

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

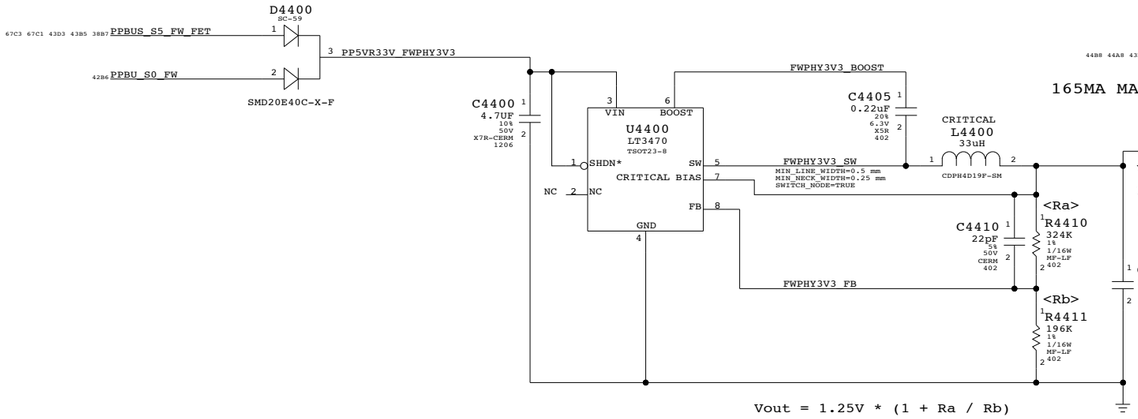
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

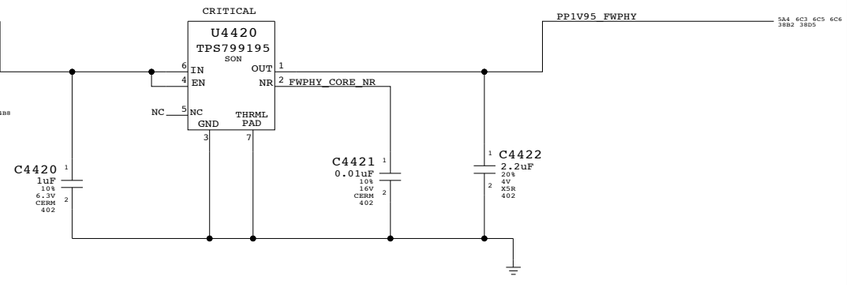
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 41 OF 87	

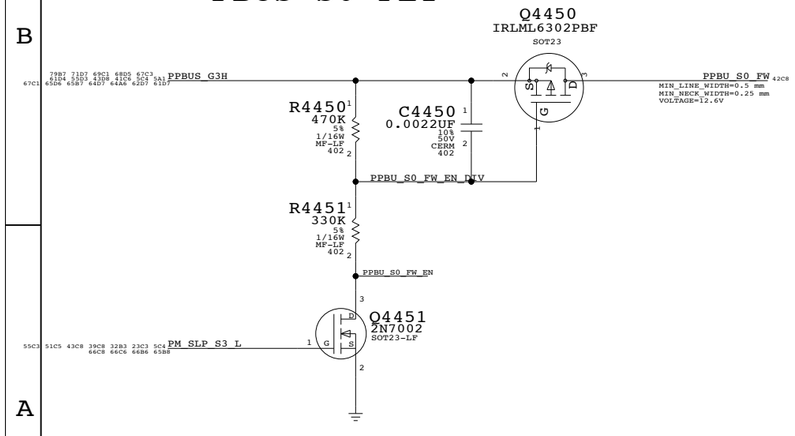
3.3V Supply for FWPHY



1.95V Supply for FW PHY



PBUS S0 FET



FW PHY Power Supply

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 42 OF 87	

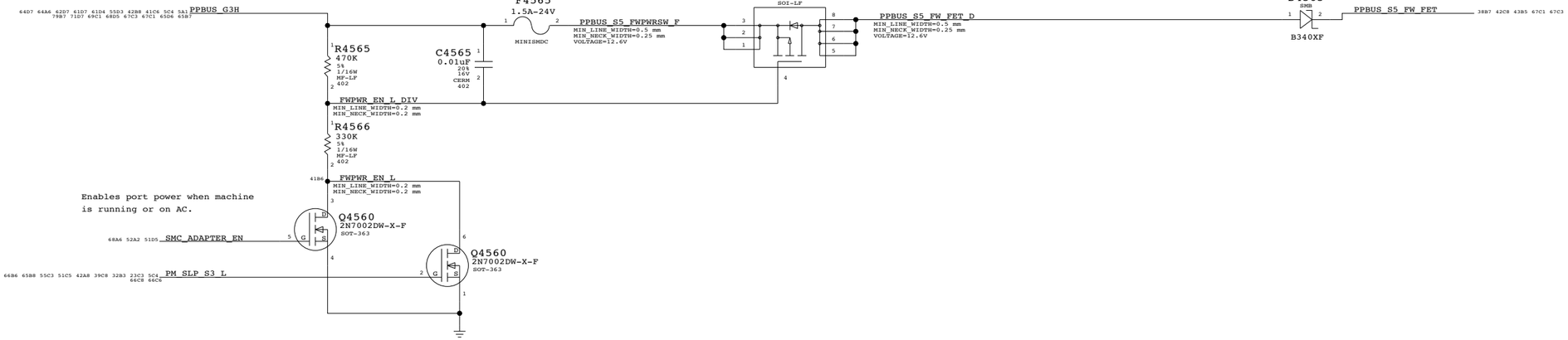
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

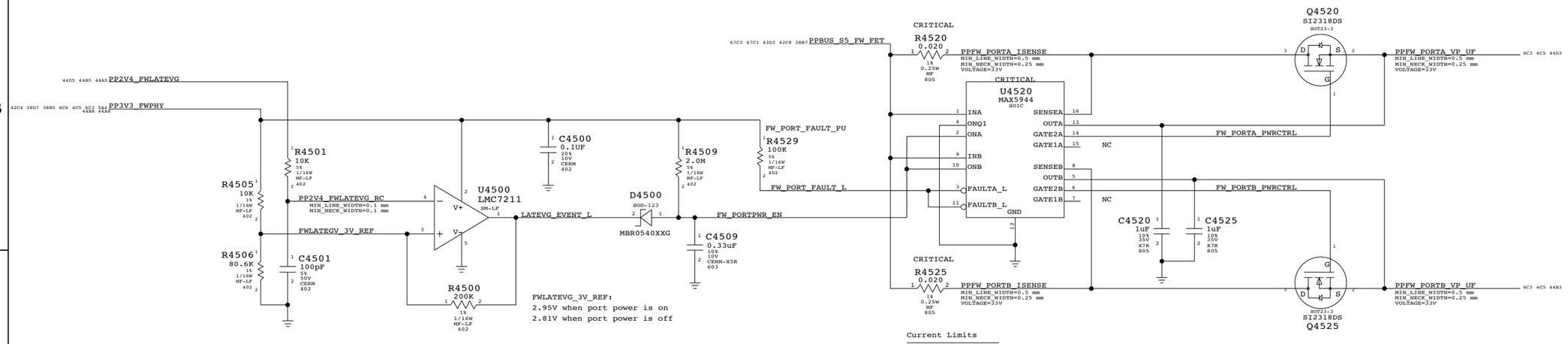
BOM options provided by this page:
(NONE)

Port Power Switch



Current Limit/Active Late-VG Protection

Late-VG Event Detection



Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 43 OF 87	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
PROVIDED	FW	FW_110ΩD	FW_PORT1_TPA_P	38B3 44B5 44B7 44C5
	FW	FW_110ΩD	FW_PORT1_TPA_N	38B3 44B5 44B7 44C5
	FW	FW_110ΩD	FW_PORT1_TPB_P	38B3 44B5 44B7 44C5
BY	FW	FW_110ΩD	FW_PORT1_TPB_N	38B3 44B5 44B7 44C5
	FW	FW_110ΩD	FW_PORT2_TPA_FL_P	44B2
PHY	FW	FW_110ΩD	FW_PORT2_TPA_FL_N	44B2
	FW	FW_110ΩD	FW_PORT2_TPB_FL_P	44B2
PAGE	FW	FW_110ΩD	FW_PORT2_TPB_FL_N	44B2

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Termination

Place close to FireWire PHY

TI PHYs require 1uF even though FW spec calls out 0.33uF

Setting attribute VOLTAGE to arbitrary value to help constraint manager find correct topolgy

Note: The peaking inductors were changed to resistors to allow placement in an area restricted by DFM rules for only Rs and Cs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S0414	4	IND,18nH-15mA,0402	L4660,L4661,L4662,L4663	CRITICAL	

Late-VG Protection Power

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4690 should be 390 Ohms max for a 3.3V rail

ESD and late-VG rail for snap-back diodes (Common to all ports)

Cable Power

"Snapback" & "Late VG" Protection

Note:Trace PPFW_PORT1_VP should handle up to 5A

PORT 1
BILINGUAL

Place C4629 close to pin 5 of connector

Cable Power

"Snapback" & "Late VG" Protection

PORT 2
1394A

FireWire Ports	
SYNC_MASTER=M59_MLB	SYNC_DATE=06/27/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

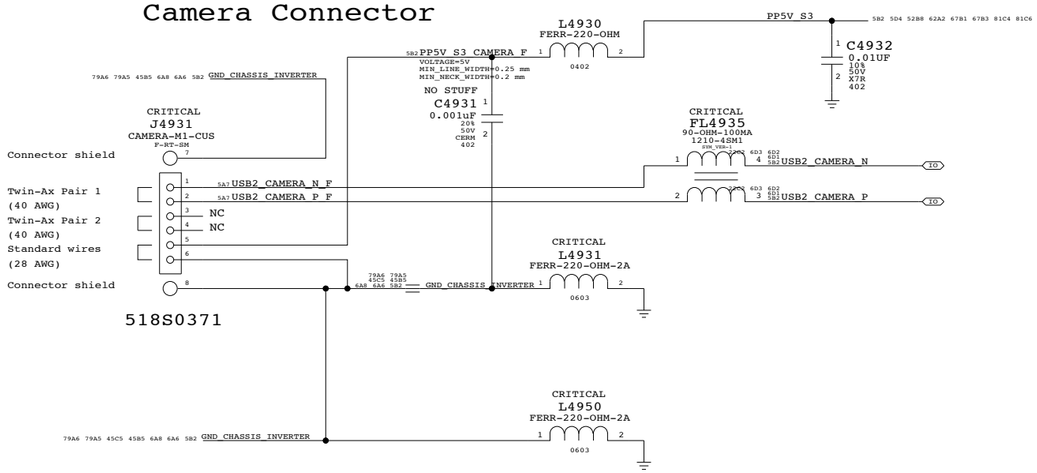
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 44 OF 87	

Camera Connector



Camera Connector

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

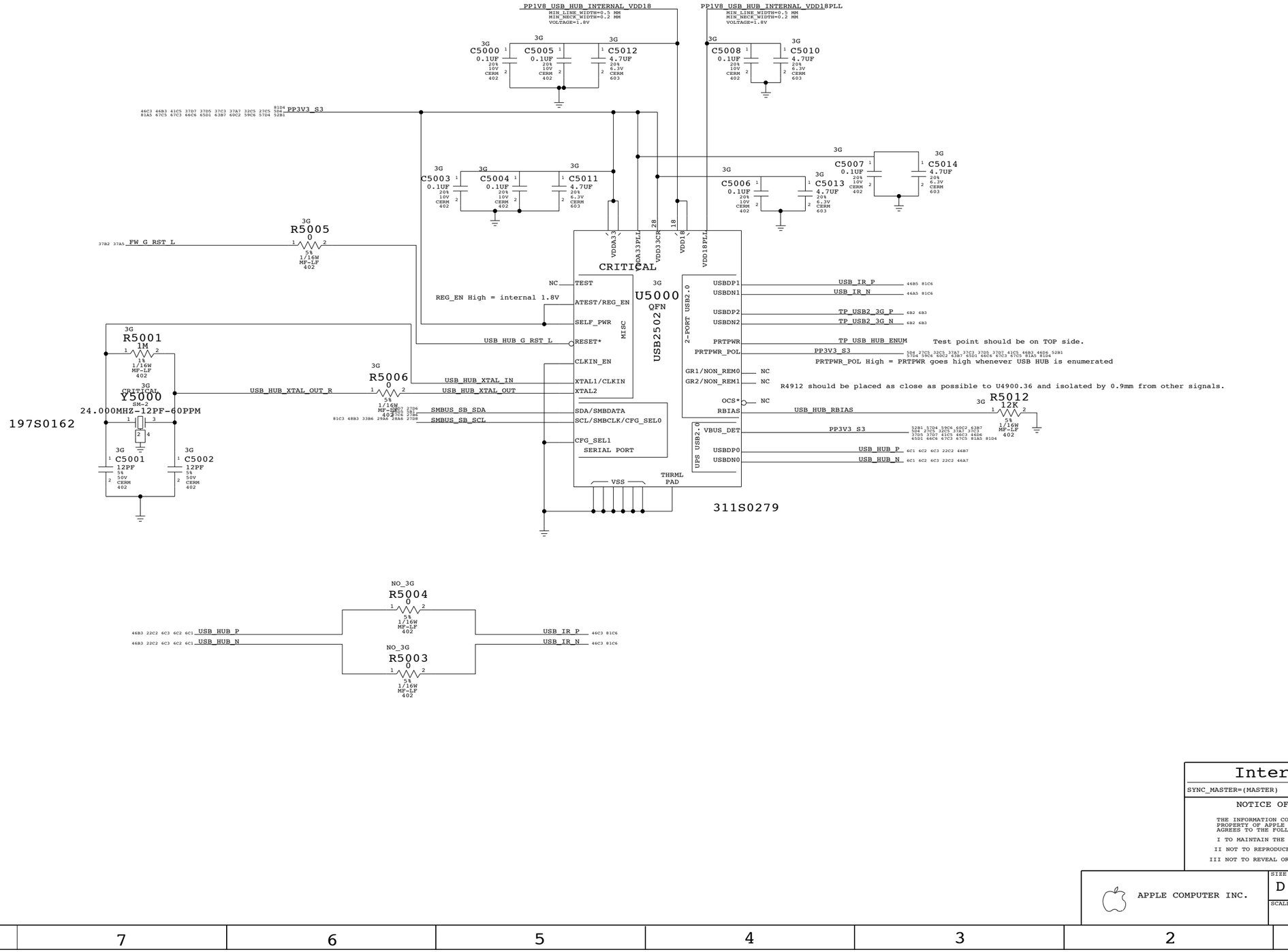
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	45	87



Internal USB Hub

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

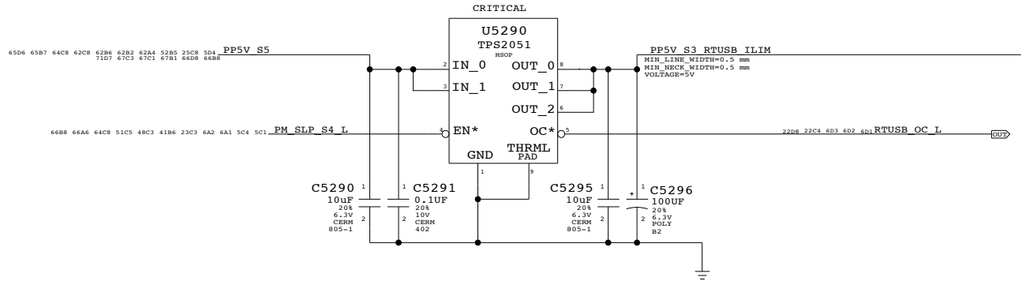
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

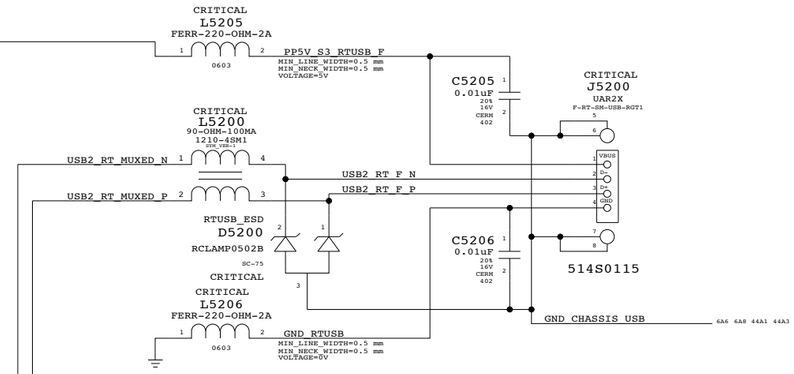
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	46	87

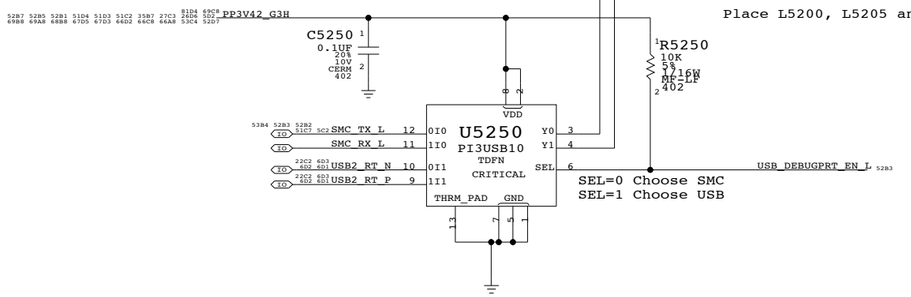
Port Power Switch



Right USB Port



USB/SMC Debug Mux



Place L5200, L5205 and L5206 across moat

External USB Connector

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

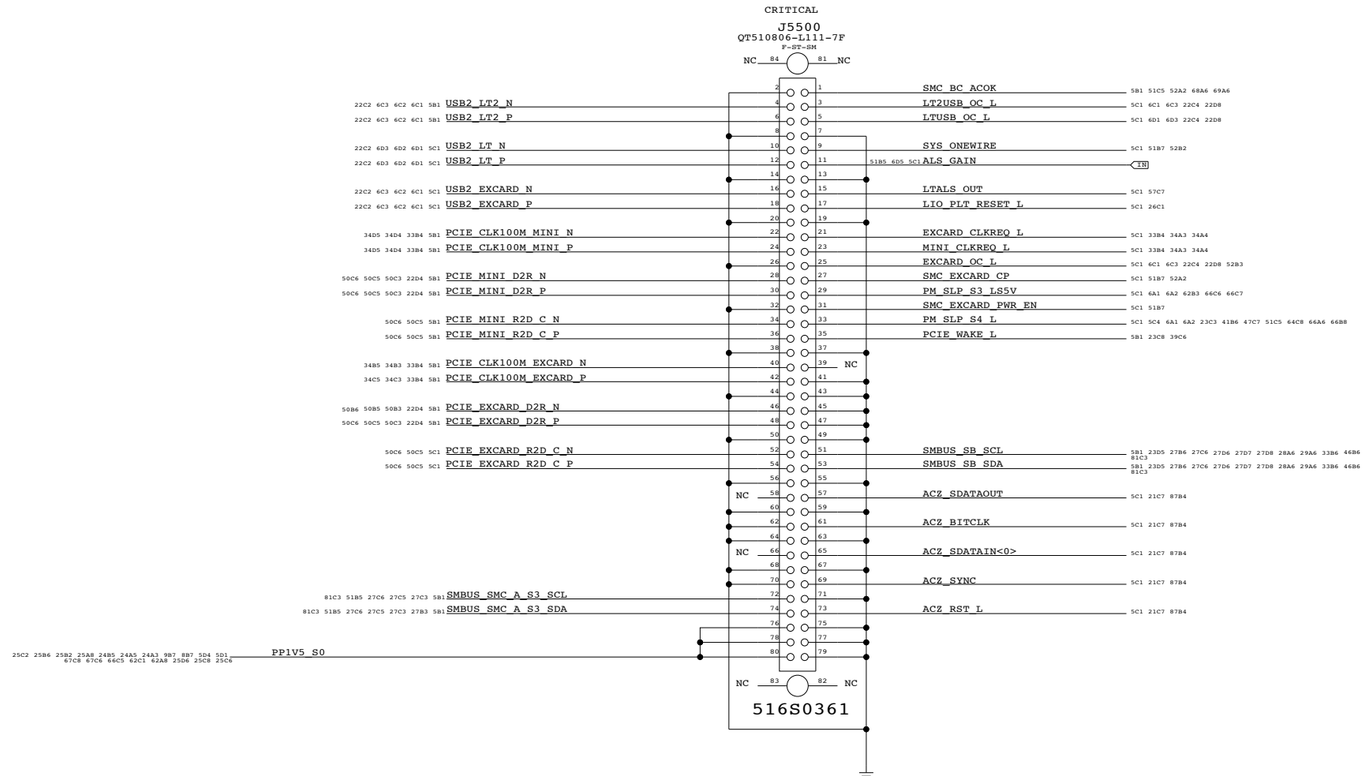
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 47 OF 87	

Left I/O Board Connector



Left I/O Board Connector		
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

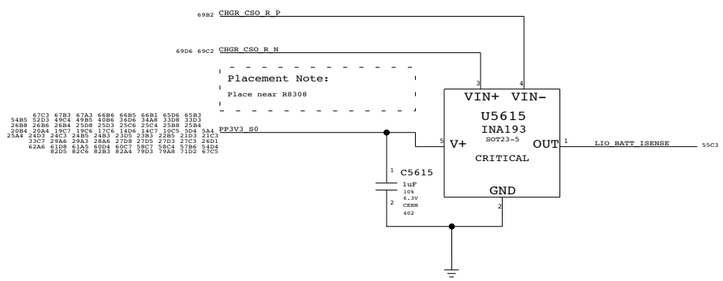
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

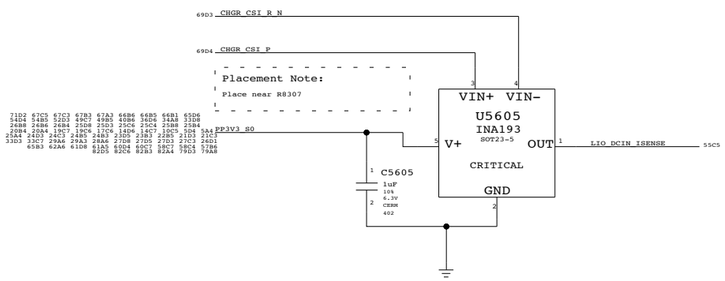
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	03001
	SCALE: NONE	SHT 48 OF 87	

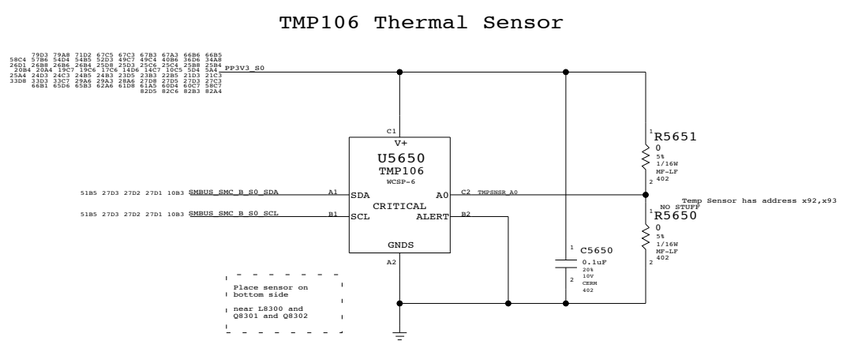
Battery Current Sense



DCIn Current Sense



TMP106 Thermal Sensor



Current & Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 49 OF 87	

PCI-E x1 Port "A" = Ethernet (Yukon)

PCI-E x1 Port "B" = PCI-E Mini Card

C5710 0.1uF

C5711 0.1uF

Place caps close to SB

50C5 48C6 5B1	PCIE_MINI_R2D_C_P	PCIE_MINI_R2D_C_P	PCIE_B_R2D_C_P	22D4	
50C5 48C6 5B1	PCIE_MINI_R2D_C_N	PCIE_MINI_R2D_C_N	PCIE_B_R2D_C_N	22D4	
50C5 50C3 48C6 22D4 5B1	PCIE_MINI_D2R_P	PCIE_MINI_D2R_P	PCIE_MINI_D2R_P	5B1 22D4 48C6 50C5 50C6	
50C5 50C3 48C6 22D4 5B1	PCIE_MINI_D2R_N	PCIE_MINI_D2R_N	PCIE_MINI_D2R_N	5B1 22D4 48C6 50C5 50C6	

PCI-E x1 Port "C" = ExpressCard

C5720 0.1uF

C5721 0.1uF

Place caps close to SB

50C5 48B6 5C1	PCIE_EXCARD_R2D_C_P	PCIE_EXCARD_R2D_C_P	PCIE_C_R2D_C_P	22D4	
50C5 48B6 5C1	PCIE_EXCARD_R2D_C_N	PCIE_EXCARD_R2D_C_N	PCIE_C_R2D_C_N	22D4	
50C5 50C3 48B6 22D4 5B1	PCIE_EXCARD_D2R_P	PCIE_EXCARD_D2R_P	PCIE_EXCARD_D2R_P	5B1 22D4 48B6 50C5 50C6	
50B5 50B3 48B6 22D4 5B1	PCIE_EXCARD_D2R_N	PCIE_EXCARD_D2R_N	PCIE_EXCARD_D2R_N	5B1 22D4 48B6 50B5 50B6	

PCI-E x1 Port "D" = Unused

50B3 22D4	TP_PCIE_D_R2DP	TP_PCIE_D_R2DP	22D4 50B6
50B3 22D4	TP_PCIE_D_R2DN	TP_PCIE_D_R2DN	22D4 50B6
50B3 22D4	TP_PCIE_D_D2RP	TP_PCIE_D_D2RP	22D4 50B6
50B3 22D4	TP_PCIE_D_D2RN	TP_PCIE_D_D2RN	22D4 50B6

PCI-E x1 Port "E" = Unused

50B3 22C4	TP_PCIE_E_R2DP	TP_PCIE_E_R2DP	22C4 50B6
50B3 22C4	TP_PCIE_E_R2DN	TP_PCIE_E_R2DN	22C4 50B6
50B3 22C4	TP_PCIE_E_D2RP	TP_PCIE_E_D2RP	22C4 50B6
50B3 22C4	TP_PCIE_E_D2RN	TP_PCIE_E_D2RN	22C4 50B6

PCI-E x1 Port "F" = Unused

50B3 22C4	TP_PCIE_F_R2DP	TP_PCIE_F_R2DP	22C4 50B6
50B3 22C4	TP_PCIE_F_R2DN	TP_PCIE_F_R2DN	22C4 50B6
50B3 22C4	TP_PCIE_F_D2RP	TP_PCIE_F_D2RP	22C4 50B6
50A3 22C4	TP_PCIE_F_D2RN	TP_PCIE_F_D2RN	22C4 50A6

PCI-E Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 50 OF 87

UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE_XXX_IS_THE_PORT_NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE	B12	P10	
SMC_RSTGATE_L	C13	P11	
ALL_SYS_PWRGD	A15	P12	
RSMRST_PWRGD	B14	P13	
SMC_SB_NMI	B15	P14	
PM_RSMRST_L	C14	P15	
IMVP_VR_ON	D12	P16	
PM_PWRBTN_L	C15	P17	
TP_SMC_P20	D13	P20	
TP_SMC_P21	D14	P21	
TP_SMC_P22	D15	P22	
TP_SMC_P23	E12	P23	
SMC_BATT_TRICKLE_EN_L	E14	P24	
SMC_BATT_CHG_EN	E15	P25	
TP_SMC_P26	E13	P26	
TP_SMC_P27	F14	P27	
LPC_AD<0>	D9	P30/LAD0	
LPC_AD<1>	C9	P31/LAD1	
LPC_AD<2>	A9	P32/LAD2	
LPC_AD<3>	B9	P33/LAD3	
LPC_FRAME_L	D8	P34/LFRAME*	
SMC_LRESET_L	C8	P35/LRESET*	
PCI_CLK_SMC	A8	P36/LCLK	
INT_SERIRQ	D7	P37/SERIRQ	
TP_SMC_XDP_TMS	A5	P40/TMI0	
SMC_SYS_LED_16B	B5	P41/TMO0	
SMBUS_SMC_BSB_SDA	D5	P42/SDA1	
SMC_TPM_PP	C3	P43/TMI1/EXSCK1	
TP_SMC_XDP_TRST_L	B1	P44/TMO1	
TP_SMC_XDP_TCK	C2	P45	
TP_SMC_SYS_LED	D3	P46/PWX0/PWM0	
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1	
SMC_TX_L	G1	P50	
SMC_RX_L	G4	P51	
SMBUS_SMC_0_S0_SCL	F2	P52/SCL0	

P60/KIN0*	L13		SMC_PM_G2_EN
P61/KIN1*	L14		SMC_ADAPTER_EN
P62/KIN2*	L15		SPI_ARB
P63/KIN3*	K12		SPI_SCLK
P64/KIN4*	K13		SPI_SI
P65/KIN5*	K14		SPI_SO
P66/IRQ6*/KIN6*	J12		SMC_PROCHOT_3_3_L
P67/IRQ7*/KIN7*	J13		FWH_INIT_L
P70/AN0	N12		SMC_CPU_ISENSE
P71/AN1	R13		SMC_CPU_VSENSE
P72/AN2	P13		SMC_GPU_ISENSE
P73/AN3	R14		SMC_GPU_VSENSE
P74/AN4	P14		SMC_DCIN_ISENSE
P75/AN5	R15		SMC_PBUS_VSENSE
P76/AN6	N13		SMC_BATT_ISENSE
P77/AN7	P15		SMC_P1V5S0_NB_ISENSE
P80/PME*	C7		SMC_WAKE_SCI_L
P81/GA20	A7		SMC_TPM_GPIO
P82/CLKRUN*	B7		PM_CLKRUN_L
P83/LPCPD*	D6		PM_SUS_STAT_L
P84/IRQ3*/TXD1	C6		SC_TX_L
P85/IRQ4*/RXD1	A6		SC_RX_L
P86/IRQ5*/SCK1/SCL1	B6		SMBUS_SMC_BSB_SCL
P90/IRQ2*	K4		SMC_ONOFF_L
P91/IRQ1*	J2		SMC_BC_ACOK
P92/IRQ0*	J1		SMC_BS_ALRT_L
P93/IRQ12*	J3		PM_SLP_S3_L
P94/IRQ13*	J4		PM_SLP_S4_L
P95/IRQ14*	H2		PM_SLP_S5_L
P96/EXCL	H1		SMC_CLK32K_SUSCLK
P97/IRQ15*/SDA0	G2		SMBUS_SMC_0_S0_SDA

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	
SMC_USB_DEBUG_MUX	N3	PA3/KIN11*/PS2AD	
PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	
PM_THRM_L	N2	PA5/KIN13*/PS2BD	
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	
SMC_EXTSMI_L	B10	PB0/LSMI*	
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	
SMC_ODD_DETECT	D10	PB2	
ISENSE_CAL_EN	A11	PB3	
SMC_EXCARD_CP	B11	PB4	
SMC_EXCARD_PWR_EN	C11	PB5	
SMC_EXCARD_OC_L	A12	PB6	
SMC_XDP_TDO_3_3	D11	PB7	
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	
TP_SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	
TP_SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	
TP_SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	
TP_SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	
SMS_X_AXIS	M11	PD0/AN8	
SMS_Y_AXIS	P11	PD1/AN9	
SMS_Z_AXIS	R11	PD2/AN10	
TP_SMC_ANALOG_ID	N11	PD3/AN11	
SMC_P1V05S0_ISENSE	P10	PD4/AN12	
SMC_MEM_ISENSE	R10	PD5/AN13	
ALS_LEFT	N10	PD6/AN14	
ALS_RIGHT	M10	PD7/AN15	

PE0	M3		SMC_CASE_OPEN
PE1*/ETCK	M2		SMC_TCK
PE2*/ETDI	M1		SMC_TDI
PE3*/ETDO	L4		SMC_TDO
PE4*/ETMS	L2		SMC_TMS
PF0/IRQ8*/PWM2	M7		TP_SMC_PF0
PF1/IRQ9*/PWM3	P6		TP_SMC_PF1
PF2/IRQ10*/TMOY	R6		SMC_LID
PF3/IRQ11*/TMOX	N6		SMC_CPU_RESET_3_3_L
PF4/PWM4	M6		SMC_BATT_ISET
PF5/PWM5	R5		TP_SMC_BATT_VSET
PF6/PWM6	P5		SMC_SYS_ISET
PF7/PWM7	N5		TP_SMC_SYS_VSET
PG0/EXIRQ8*/TMIX	P9		SPI_CE_L
PG1/EXIRQ9*/TMIY	R9		SMC_XDP_TCK_3_3
PG2/EXIRQ10*/SDA2	N9		SMBUS_SMC_BSA_SDA
PG3/EXIRQ11*/SCL2	P8		SMBUS_SMC_BSA_SCL
PG4/EXIRQ12*/EXSDAA	R8		SMBUS_SMC_A_S3_SDA
PG5/EXIRQ13*/EXSCLA	M8		SMBUS_SMC_A_S3_SCL
PG6/EXIRQ14*/EXSDAB	P7		SMBUS_SMC_B_S0_SDA
PG7/EXIRQ15*/EXSCLB	R7		SMBUS_SMC_B_S0_SCL
PH0/EXIRQ6*	E1		SMC_PROCHOT
PH1/EXIRQ7*	F3		SMC_THRMTRIP
PH2/FWE	K2		SMC_FWE
PH3/EXEXCL	C4		ALS_GAIN
PH4	D4		SMS_INT_L
PH5	B3		SMS_ONOFF_L

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

PP3V42_G3H

C5802 22UF 20% 6.3V CERM 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 10% 6.3V CERM-X5R 402
VCL IS INTERNAL RAIL

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

PP3V42_G3H
R5899 4.7 5% 1/16W MF-LF 402
PP3V3_AVCC_SMC
C5820 0.1UF 20% 10V CERM 402
GND_SMC_AVSS

PP3V3_AVREF_SMC
PP3V42_G3H

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
KBC_MDE
SMC_MD1
SMC_NMI
SMC_TRST_L
NOSTUFF
R5898 10K 5% 1/16W MF-LF 402
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402

SMC_RST_L
SMC_XTAL
SMC_EXTAL

XW5800
SM
GND_SMC_AVSS

SMC

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

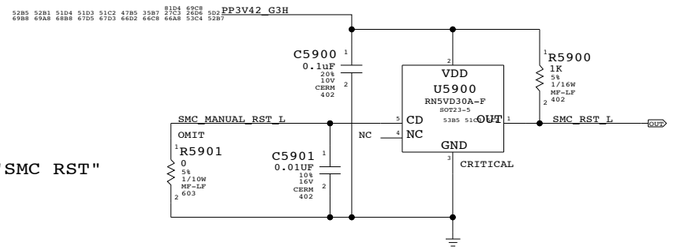
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

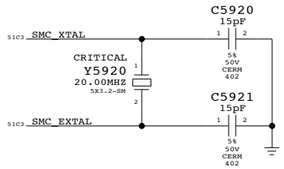
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 51 OF 87	

SMC Reset Button / Brownout Detect

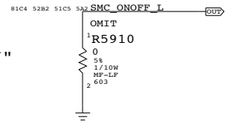


Silk: "SMC RST"

SMC Crystal Circuit

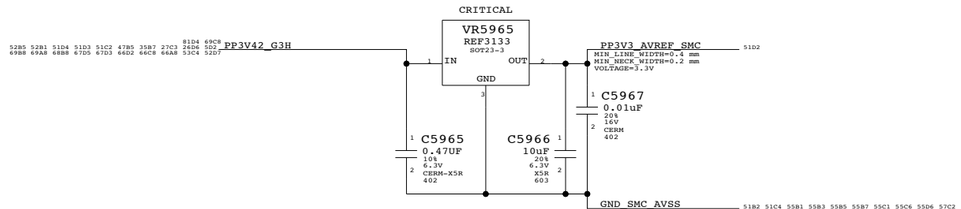


Debug Power Button

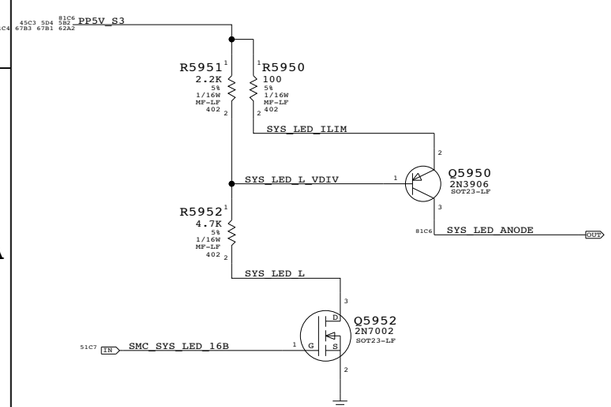


Silk: "PWR BTN"

SMC AVREF Supply

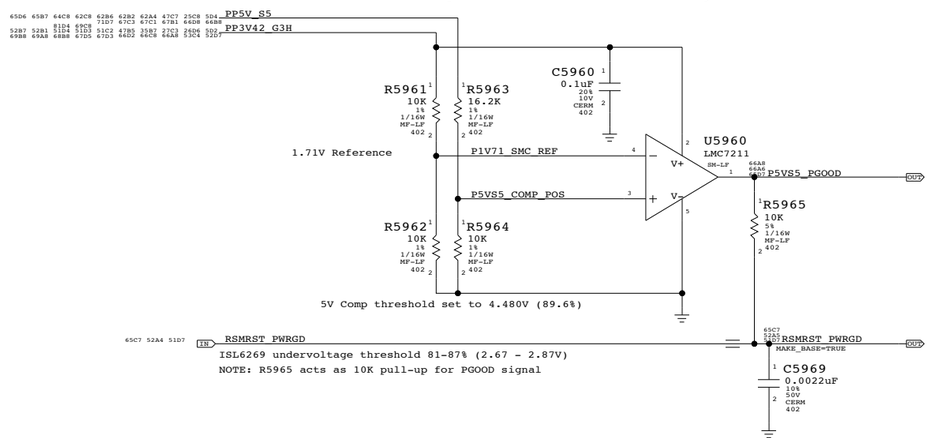


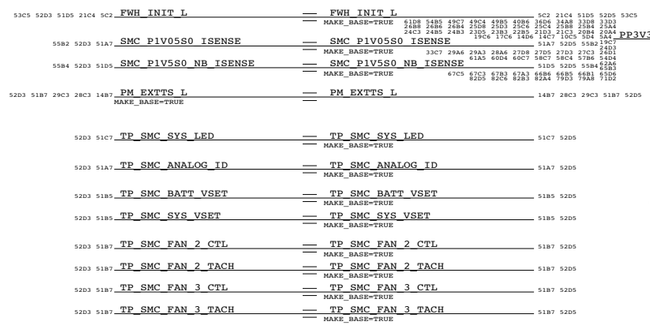
System (Sleep) LED Circuit

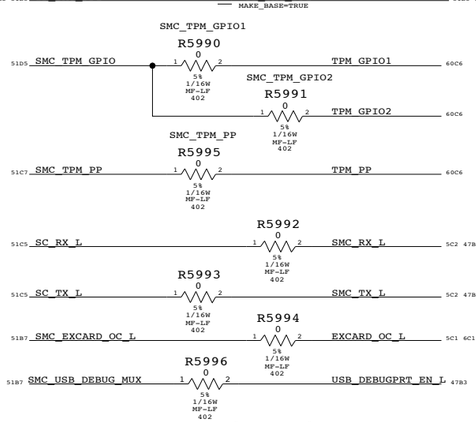


SMC PWRGD Circuit

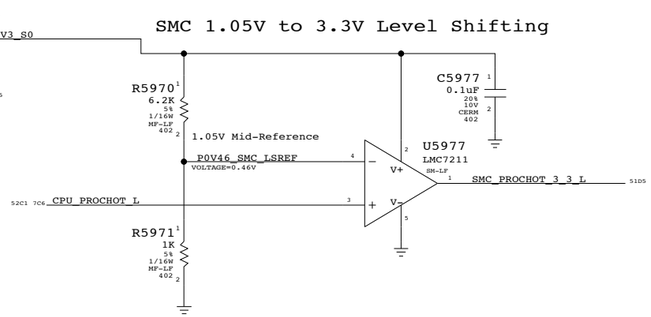
Reports when 5V S5 and 3.3V S5 are in regulation



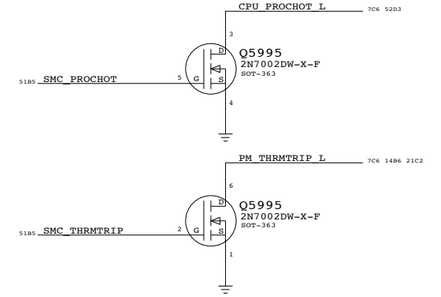


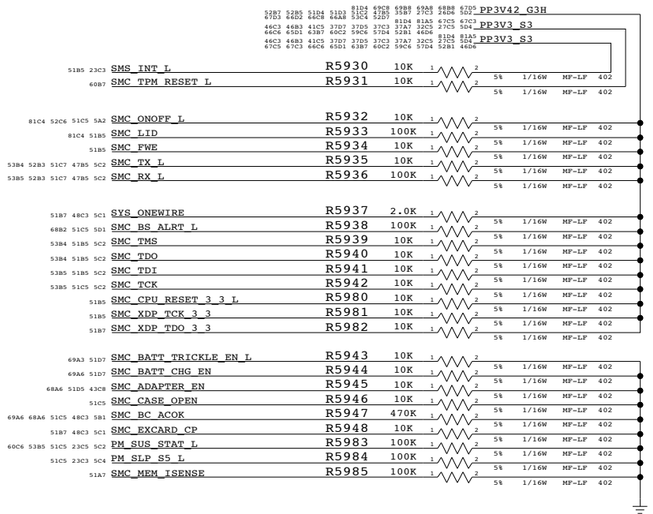


SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting





SMC Support

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

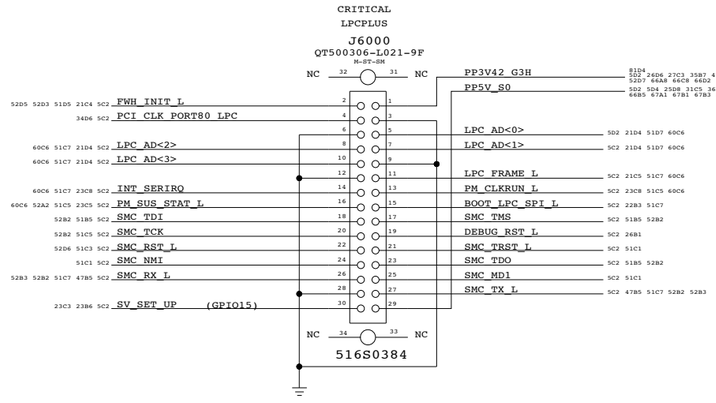
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 52 OF 87	



LPC+ Debug Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

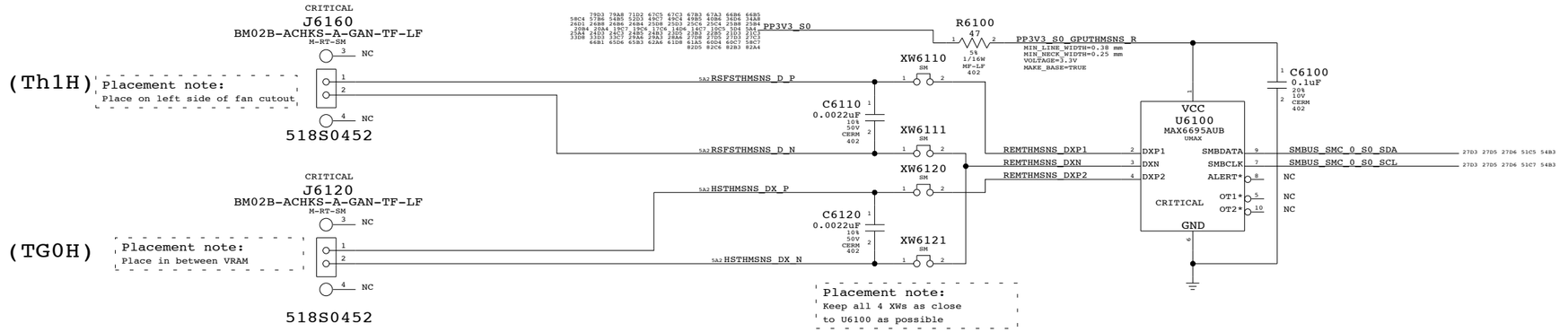
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

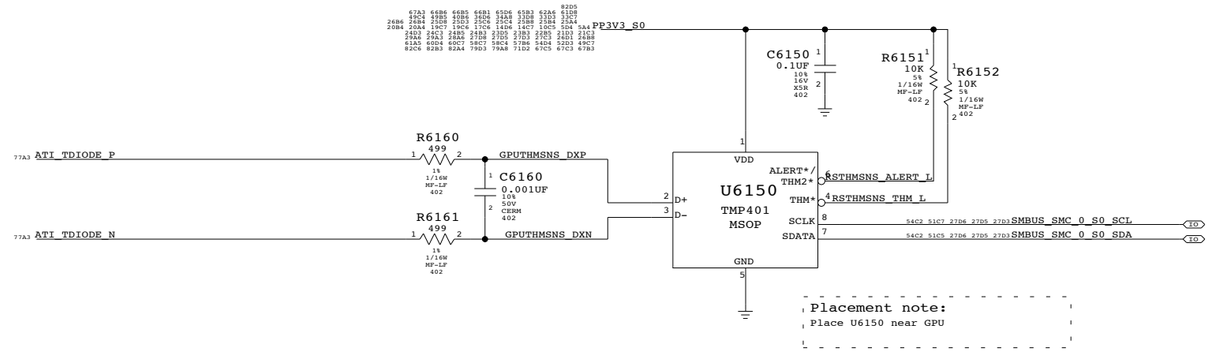
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 53 OF 87	

GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



Thermal Sensors

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

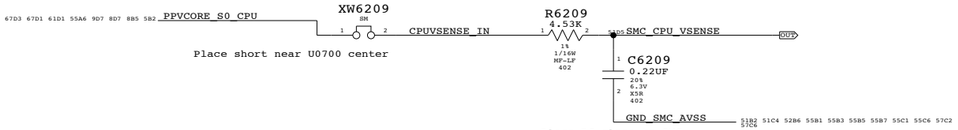
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

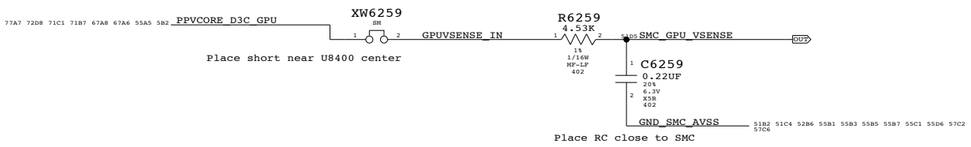
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	54	87

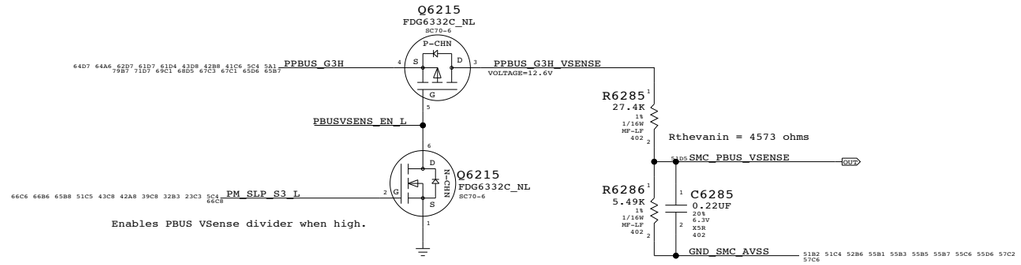
CPU Voltage Sense / Filter



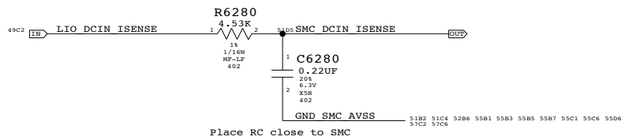
GPU Voltage Sense / Filter



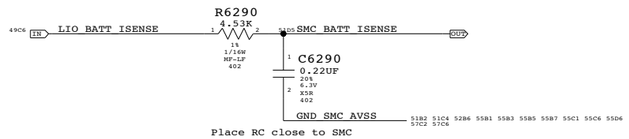
PBUS Voltage Sense Enable & Filter



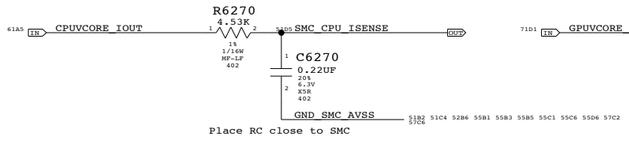
DCIN Current Sense Filter



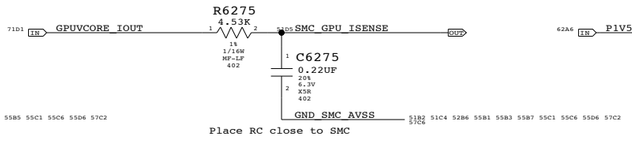
Battery Current Sense Filter



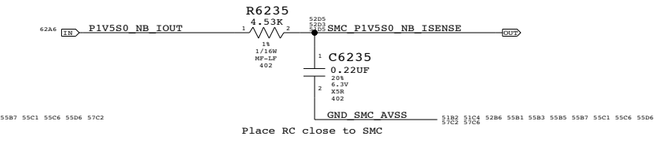
CPU Current Sense Filter



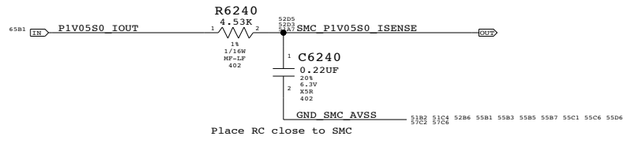
GPU Current Sense Filter



1.5V S0 (NB) Current Sense Filter

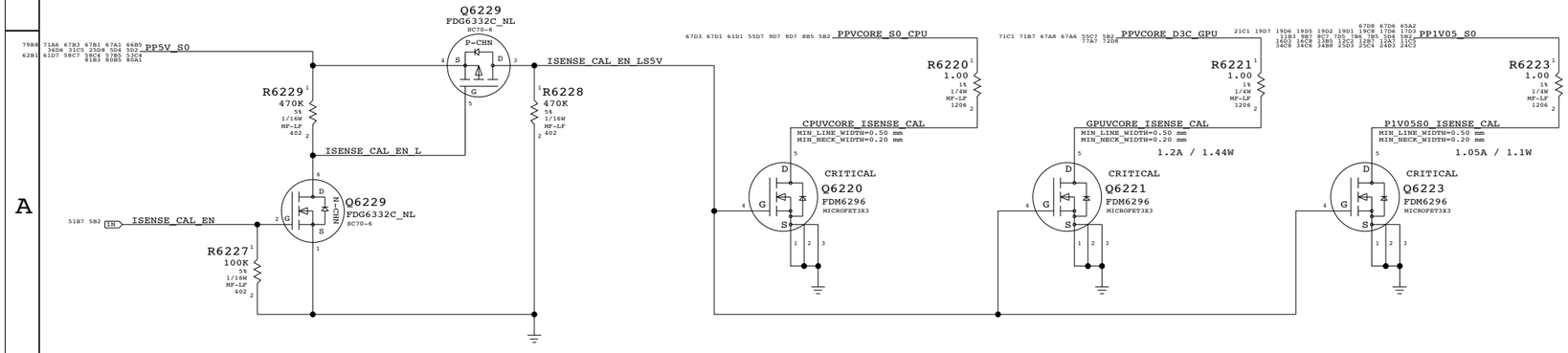


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

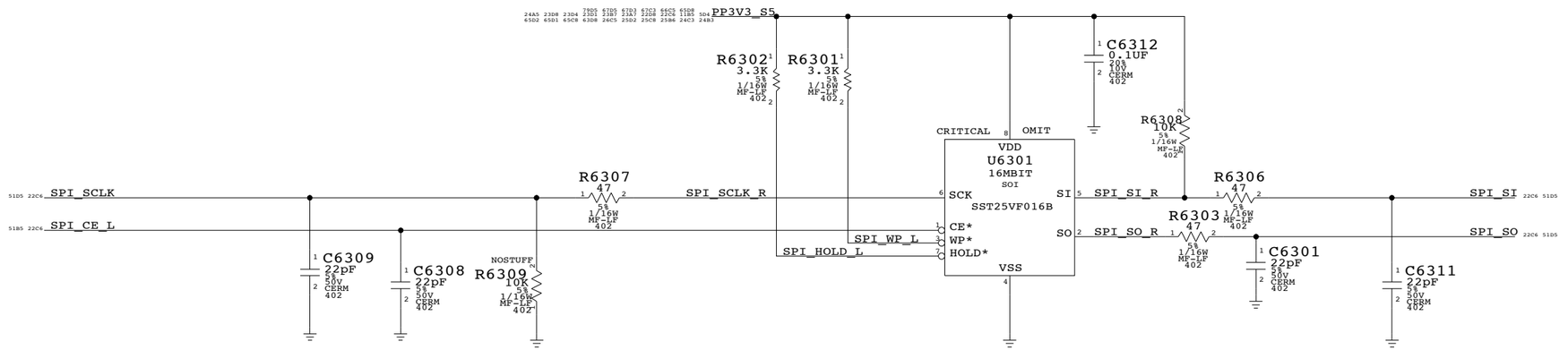
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 55 OF 87	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

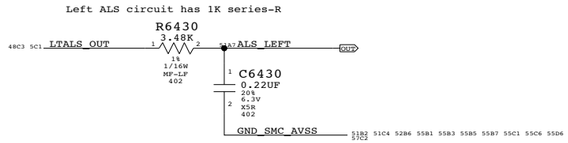
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

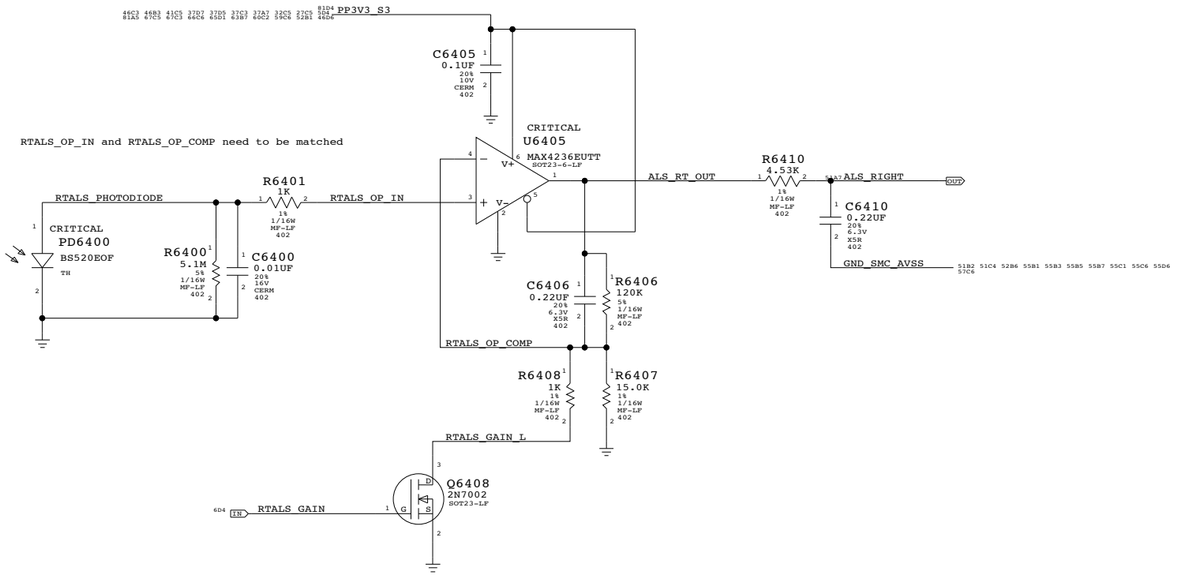
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	56	87

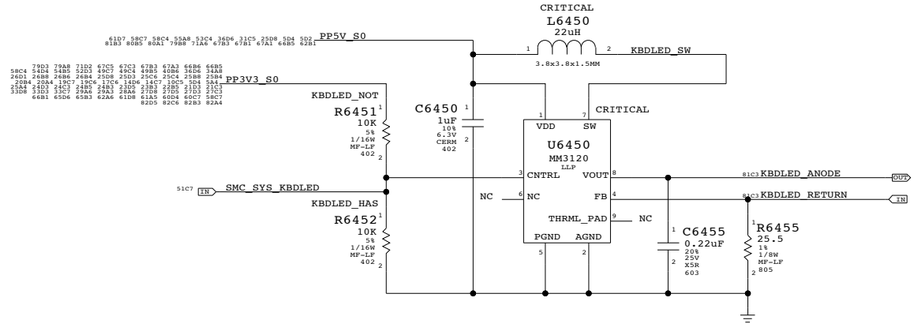
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

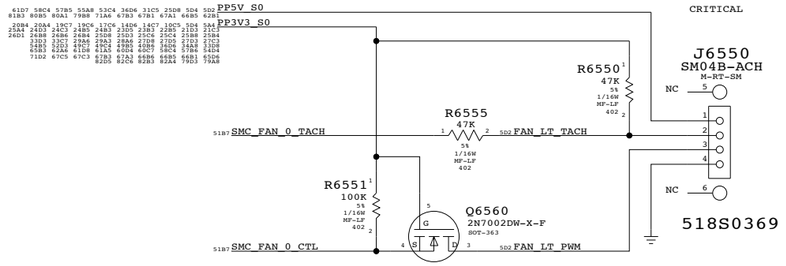
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

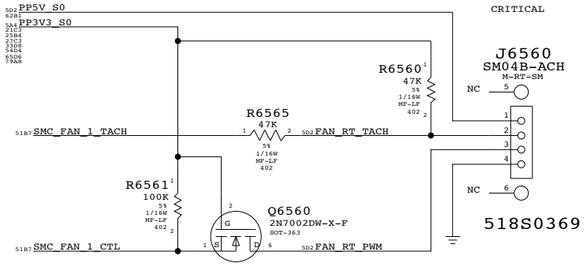
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	57	87

Left Fan



Right Fan



Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

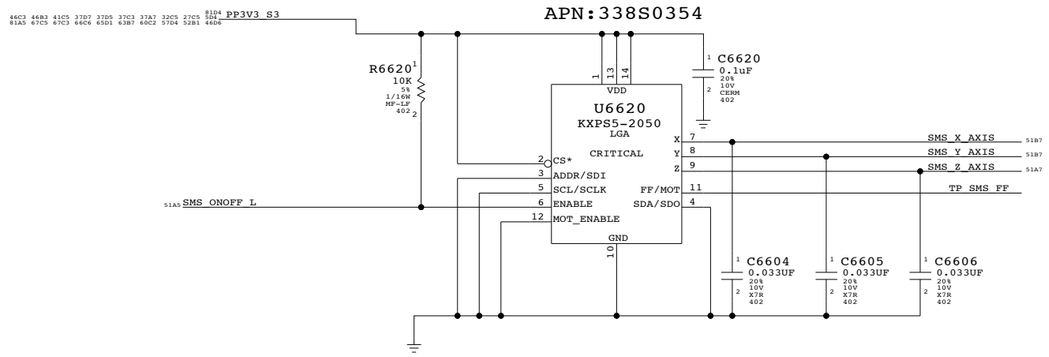
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

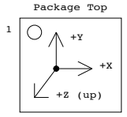
SCALE	SHT	OF
NONE	58	87

APN:338S0354



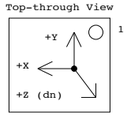
Desired orientation when
placed on board top-side:

Package Top



Desired orientation when
placed on board bottom-side:

Top-through View



M59 placement: Bottom-side

Sudden Motion Sensor (SMS)

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

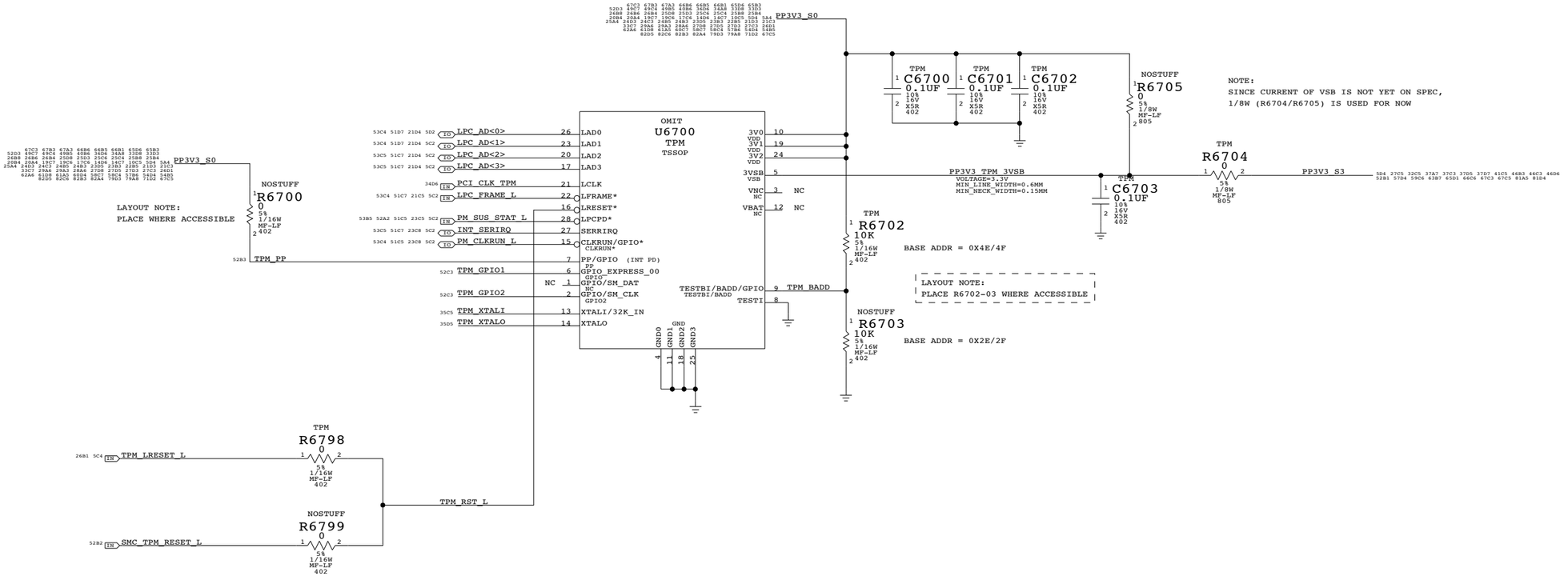
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE

SHT 59 OF 87



TPM		
SYNC_MASTER=M59_MLB	SYNC_DATE=08/08/2006	

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	03001
	SCALE: NONE	SHT 60 OF 87	

DPRSLPVR	DPRSTP*	PSI*	Operation Mode	
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

These caps for Q7500

These caps for Q7550

Vout = Variable
36A max output
(Inductors limit)

U7530 ISL9504CRZ QFN

Vout = Gain * ((2.1 mV/A * Iload) + Voffset)

Voffset = (Vdrp_offset * Kdroop) + Vamp_offset

Gain = Rc / (Ra + Rb)

Voffset worst-case -2.3mV (+/- ~1A offset)

Vout @ 36A = 2.44V-2.60V

CPU VCore Current Sense

IMVP6 CPU VCore Regulator

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

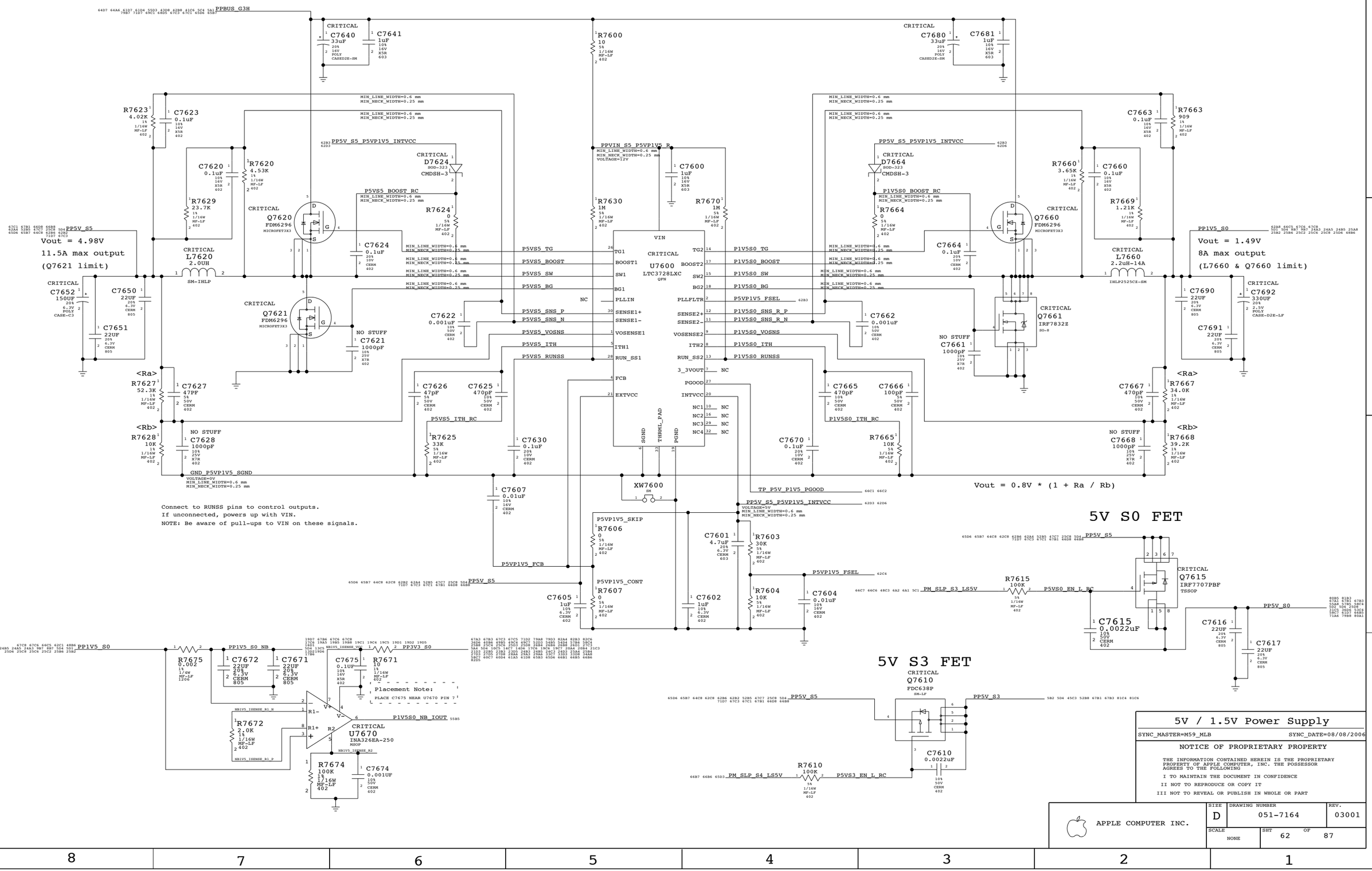
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 61 OF 87	



5V / 1.5V Power Supply

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

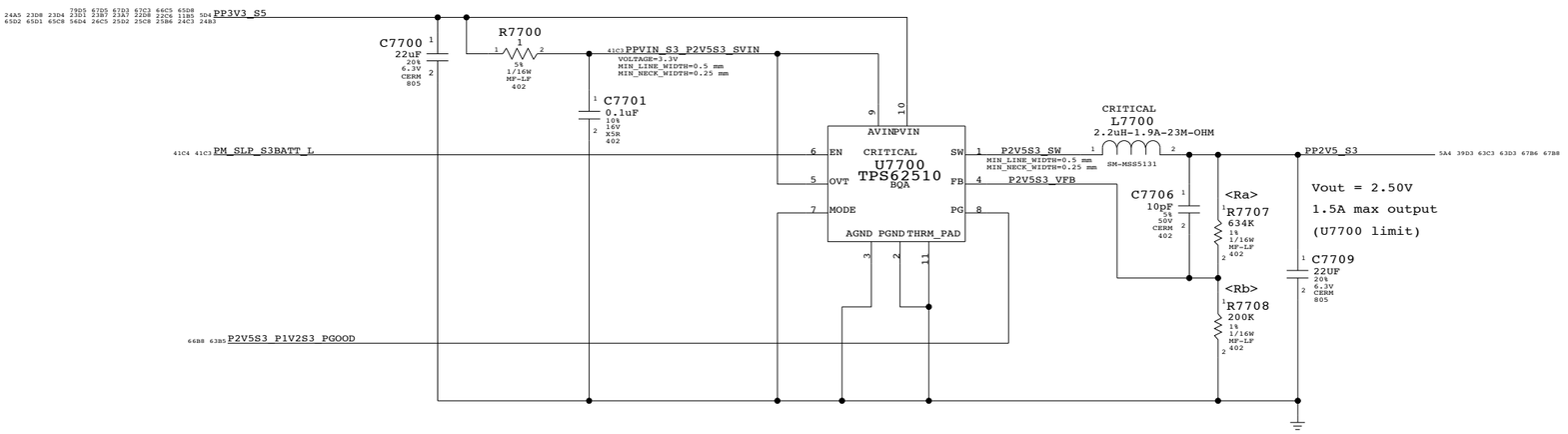
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

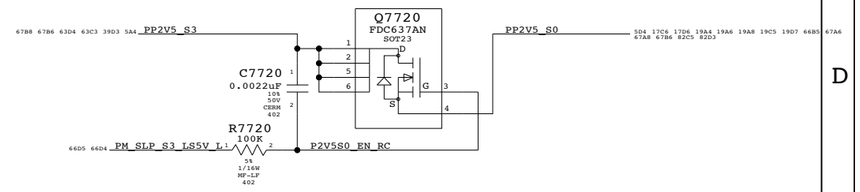
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 62 OF 87	

2.5V S3 Regulator

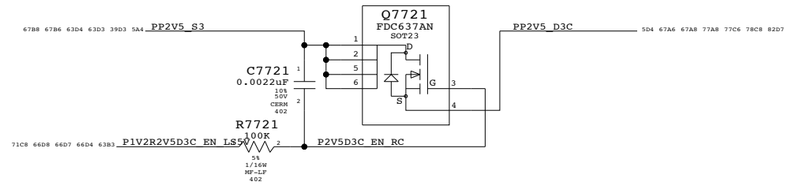


Vout = 0.6V * (1 + Ra / Rb)

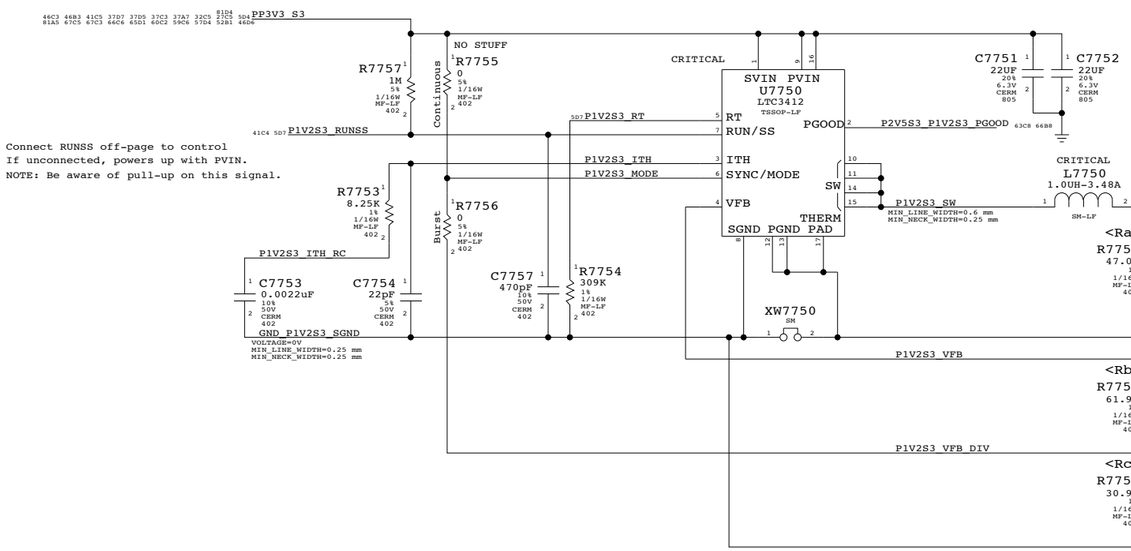
2.5V S0 FET



2.5V D3Cold FET

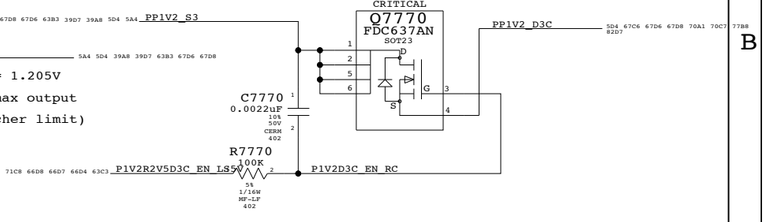


1.2V S3 Regulator



Vout = 0.8V * (1 + Ra / (Rb + Rc))

1.2V D3Cold FET



2.5V & 1.2V Regulators

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

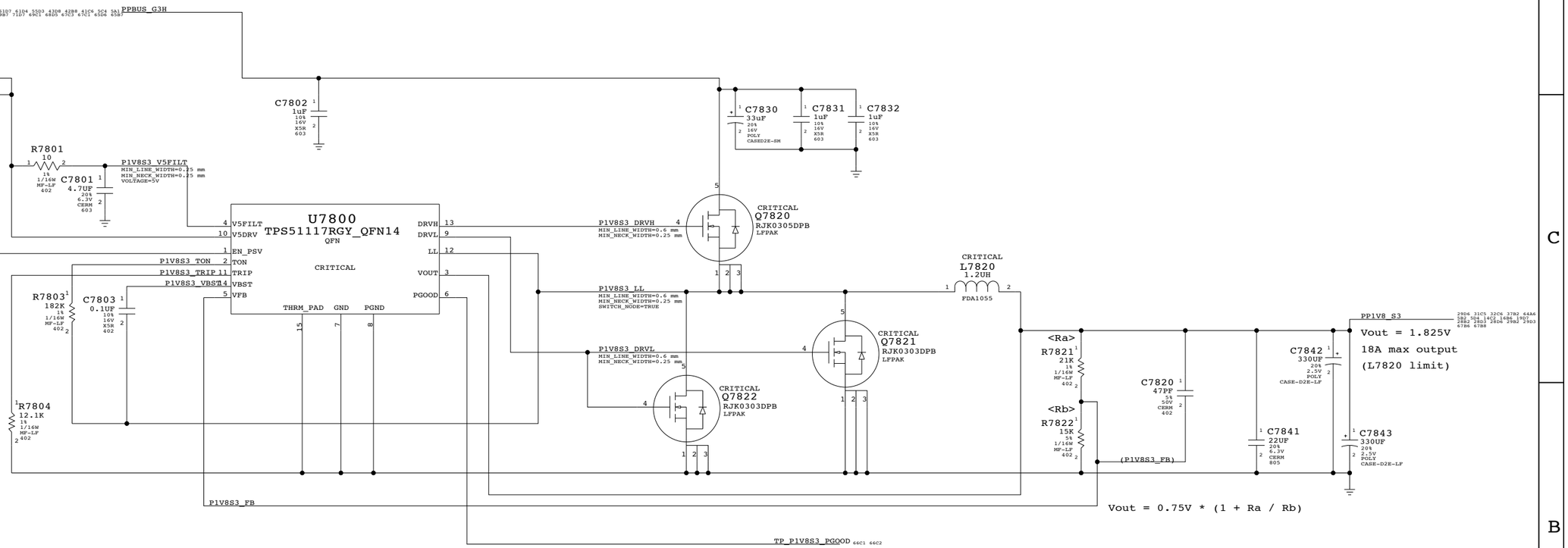
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

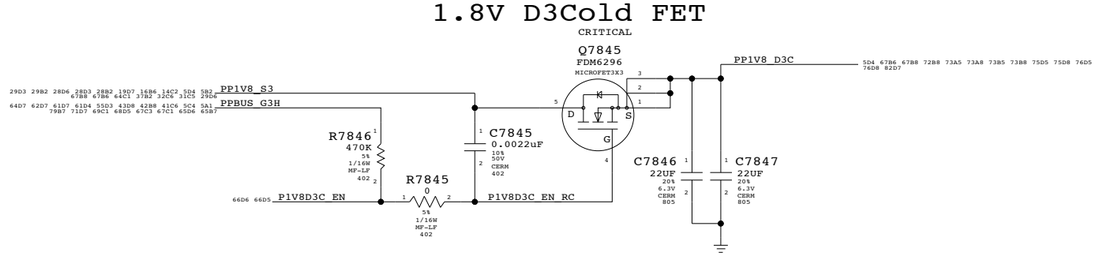
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	63	87



1.8V D3Cold FET



1.8V Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT: 64	OF: 87

3.3V S0 FET

Q7947
FDC638P
SM-LF

PP3V3_S5 → Q7947 pin 4
PP3V3_S0 ← Q7947 pin 6

R7947 100K 5% 1/16W MF-LF 402
66D5 P3V3S0_EN_L → R7947 pin 1
R7947 pin 2 → P3V3S0_EN_L_RC

C7947 0.0047uF 10% 25V CERM 402
C7947 pin 1 → Q7947 pin 3
C7947 pin 2 → GND_P3V3S5_SGND

3.3V D3Cold FET

Q7948
FDC638P
SM-LF

PP3V3_S5 → Q7948 pin 4
PP3V3_D3C ← Q7948 pin 6

C7948 0.0047uF 10% 25V CERM 402
C7948 pin 1 → Q7948 pin 3
C7948 pin 2 → GND_P3V3S5_SGND

R7948 100K 5% 1/16W MF-LF 402
66D5 66D7 P3V3D3C_EN_L → R7948 pin 1
R7948 pin 2 → P3V3D3C_EN_L_RC

3.3V S5 Regulator

PP5V_S5
PPBUS_G3H

C7901 1uF 10% 16V X5R 603
C7900 2.2UF 20% 6.3V CERM1 603
C7902 2.2UF 20% 6.3V CERM1 603

NO STUFF
R7904 0 5% 1/16W MF-LF 402

R7949 0 5% 1/16W MF-LF 402
66A8 66A6 52A4 P5VS5_PGOOD → R7949 pin 1
52A5 52A4 51D7 RSMRST_PWRGD → R7949 pin 2

C7906 0.01UF 10% 16V CERM 402
R7906 57.6K 1% 1/16W MF-LF 402

R7908 51.1K 1% 1/16W MF-LF 402
C7907 470pF 10% 50V CERM 402
P3V3S5_COMP_R

R7905 0 5% 1/16W MF-LF 402
C7908 0.022uF 10% 16V CERM-X5R 402
NO STUFF
C7949 0.01uF 20% 16V CERM 402

GND_P3V3S5_SGND

U7900
ISL6269BCRZ
QFN
CRITICAL

1	VIN	UG	14
7	FSET	BOOT	13
4	EN	PHASE	15
3	FCCM	ISEN	9
16	PGOOD	LG	11
5	COMP	PGND	10
6	FB		
8	VO		
12	PVCC		
2	VCC		
17	THRML PAD		

5D7 P3V3S5_FSET
P3V3S5_EN_RC
P3V3S5_FCCM
5D7 P3V3S5_COMP
P3V3S5_FB

P3V3S5_BOOT_R
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

R7909 0 5% 1/16W MF-LF 402
C7909 0.22uF 20% 6.3V X5R 402

P3V3S5_UG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
P3V3S5_BOOT
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
P3V3S5_PHASE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
P3V3S5_ISEN
P3V3S5_LG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

R7910 5.62K 1% 1/16W MF-LF 402

CRITICAL
Q7920
FDM6296
MICROFET3X3

CRITICAL
Q7921
FDM6296
MICROFET3X3

NO STUFF
C7921 1000pF 10% 25V X7R 402

XW7900 8M

CRITICAL
C7930 33UF 20% 16V POLY CASED2E-SM

3.3V S3 FET

Q7945
FDC638P
SM-LF

PP3V3_S5 → Q7945 pin 4
PP3V3_S3 ← Q7945 pin 6

C7945 0.0022uF 10% 50V CERM 402
C7945 pin 1 → Q7945 pin 3
C7945 pin 2 → GND_P3V3S5_SGND

R7945 100K 5% 1/16W MF-LF 402
66B7 66B6 62A4 PM_SLP_S4_LS5V → R7945 pin 1
R7945 pin 2 → P3V3S3_EN_L_RC

CRITICAL
L7920 4.7uH
IHLP

<Ra> R7921 3.32K 0.1% 1/16W MF-LF 402
<Rb> R7922 732 0.1% 1/16W MF-LF 402

C7920 0.0047uF 10% 25V CERM 402
P3V3S5_FB_RC
R7920 0 5% 1/16W MF-LF 402

C7940 22UF 20% 6.3V CERM 805
C7941 22UF 20% 6.3V CERM 805
C7942 150UF 20% 6.3V POLY CASE-C3

PP3V3_S5
Vout = 3.32V
4.5A max output
(L7920 limit)

Vout = 0.6V * (1 + Ra / Rb)

1.05V S0 Regulator

PP5V_S5
PPBUS_G3H

C7951 1uF 10% 16V X5R 603
C7950 2.2UF 20% 6.3V CERM1 603
C7952 2.2UF 20% 6.3V CERM1 603

CRITICAL
C7980 33uF 20% 16V POLY CASE2E-SM

NO STUFF
R7954 0 5% 1/16W MF-LF 402

P1V05S0_BOOT_R
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

R7959 4.7 5% 1/16W MF-LF 402
C7959 0.22uF 20% 6.3V X5R 402

CRITICAL
U7950
ISL6269BCRZ
QFN
CRITICAL

1	VIN	UG	14
7	FSET	BOOT	13
4	EN	PHASE	15
3	FCCM	ISEN	9
16	PGOOD	LG	11
5	COMP	PGND	10
6	FB		
8	VO		
12	PVCC		
2	VCC		
17	THRML PAD		

55C3 51C5 PM_SLP_S3_L
66B2 61C7 5C4 64B5 64B3 P1V5P1V05S0_PGOOD
5D7 P1V05S0_FSET
P1V05S0_FCCM
5D7 P1V05S0_COMP
P1V05S0_FB

P1V05S0_UG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
P1V05S0_BOOT
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
P1V05S0_PHASE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
P1V05S0_ISEN
P1V05S0_LG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

R7960 2.8K 1% 1/16W MF-LF 402

CRITICAL
Q7970
FDM6296
MICROFET3X3

CRITICAL
Q7971
IRF7832Z
SO-8

NO STUFF
C7971 1000pF 10% 25V X7R 402

C7956 0.01UF 10% 16V CERM 402
R7956 57.6K 1% 1/16W MF-LF 402

R7958 30.9K 1% 1/16W MF-LF 402
C7957 15PF 5% 50V CERM 402
P1V05S0_COMP_R

R7955 0 5% 1/16W MF-LF 402
C7958 0.01uF 20% 16V CERM 402

XW7950 8M

GND_P1V05S0_SGND

1.05V Current Sense

P1V05ISENS_NTC

R7996 1K 1% 1/16W MF-LF 402

CRITICAL
R7997 10KOHM-5% 0603-LF

NO STUFF
R7994 1K 1% 1/16W MF-LF 402

Placement Note:
Keep C7990, C7991, R7990, R7994 and R7997 close to inductor

R7993 20.0K 1% 1/16W MF-LF 402
P1V05ISENS_NEG

C7990 0.47UF 10% 6.3V CERM-X5R 402
C7991 0.22UF 10% 6.3V CERM-X5R 402

R7991 20.0K 1% 1/16W MF-LF 402
P1V05ISENS_RC
P1V05ISENS_POS

R7990 649 1% 1/16W MF-LF 402

CRITICAL
L7970 1.8UH
SM-IHLP

CRITICAL
U7995
HPA00141AIDCKR
SC70-5

R7998 1M 1% 1/16W MF-LF 402
C7998 470pF 10% 50V CERM 402
C7995 1uF 10% 6.3V CERM 402

R7992 1M 1% 1/16W MF-LF 402
C7992 470pF 10% 50V CERM 402

P1V05S0_IOUT → OUT 55B3

<Ra> R7971 3.32K 1% 1/16W MF-LF 402
<Rb> R7972 4.42K 1% 1/16W MF-LF 402

NO STUFF
R7970 0 5% 1/16W MF-LF 402
P1V05S0_FB_RC
(P1V05S0_FB)

NO STUFF
C7970 0.0022uF 10% 50V CERM 402

C7985 22UF 20% 6.3V CERM 805
C7986 22UF 20% 6.3V CERM 805
C7989 330UF 20% 2.5V POLY CASE-D2E-LF

PP1V05_S0
Vout = 1.05V
10A max output
(L7970 limit)

Vout = 0.6V * (1 + Ra / Rb)

3.3V / 1.05V Power Supplies

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 65 OF 87	

Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

PP5V_S5

R8050 10K 5% 1/16W MF-LF 402

R8051 10K 5% 1/16W MF-LF 402

R8052 10K 5% 1/16W MF-LF 402

GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up.

R8068 10K 5% 1/16W MF-LF 402

R8069 10K 5% 1/16W MF-LF 402

P1V2R2V5D3C_EN_LS5V

Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.

P1V2R2V5D3C_EN_LS5V (MAKE_BASE=TRUE)

P3V3D3C_EN_L (MAKE_BASE=TRUE)

P1V8D3C_EN (MAKE_BASE=TRUE)

Q8055 2N7002DW-X-F SOT-363

Q8056 2N7002DW-X-F SOT-363

1.8V Enable has pull-up to PBUS

PM_SLP_S3_LS5V_L (MAKE_BASE=TRUE)

P3V3S0_EN_L (MAKE_BASE=TRUE)

Q8050 2N7002DW-X-F SOT-363

Q8058 2N7002DW-X-F SOT-363

Q8058 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V (MAKE_BASE=TRUE)

PM_SLP_S3_LS5V

PM_SLP_S3_LS5V

P1V5S0_RUNSS

1.5V Enable has pull-up to PBUS

PP3V42_G3H

Q8050 2N7002DW-X-F SOT-363

R8054 100K 5% 1/16W MF-LF 402

Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3

PM_SLP_S3_L

R8056 100K 5% 1/16W MF-LF 402

(PM_SLP_S3_L) MAKE_BASE=TRUE

PP3V3_S3

PM_SLP_S3_L

PM_SLP_S3_L

PM_SLP_S3_L

PM_SLP_S3_L

PP3V3_S0

R8053 10K 5% 1/16W MF-LF 402

R8081 10K 5% 1/16W MF-LF 402

C8081 0.1uF 20% 10V CERM 402

MC74VHC1G08 SC70 U8081

PM_SLP_S3_L_GPUVCORE_EN

GPUVCORE_EN

GPUVCORE_EN

P2V5S3_P1V2S3_PGOOD

P2V5S3_P1V2S3_PGOOD

Ensure 1.2V and 2.5V S3 supplies are up before enabling GPU VCore to support removing ethernet power in battery sleep.

R8060 NO STUFF 0 5% 1/16W MF-LF 402

P2V5S3_P1V2S3_PGOOD (MAKE_BASE=TRUE)

SB_GPUVCORE_DISABLE_L (MAKE_BASE=TRUE)

The SB can turn off the GPUVcore (and by extension all D3Cold rails) by driving GPIO38 low.

PP5V_S5

R8055 10K 5% 1/16W MF-LF 402

PM_SLP_S4_LS5V (MAKE_BASE=TRUE)

PM_SLP_S4_LS5V

PM_SLP_S4_LS5V

Q8055 2N7002DW-X-F SOT-363

PM_SLP_S4_L

R8057 100K 5% 1/16W MF-LF 402

2.5V S3 and 1.2V S3 supplies are controlled by ethernet power control circuit.

(PM_SLP_S4_L) MAKE_BASE=TRUE

PM_SLP_S4_L

PM_SLP_S4_L

PM_SLP_S4_L

PP3V42_G3H

P5VS5_PGOOD

(P5VS5_PGOOD) MAKE_BASE=TRUE

P5VS5_PGOOD

P5VS5_RUNSS

5V Enable has pull-up to PBUS

R8059 470K 5% 1/16W MF-LF 402

Q8059 2N7002DW-X-F SOT-363

SMC_PM_G2_EN_L

Q8059 2N7002DW-X-F SOT-363

SMC_PM_G2_EN

R8058 100K 5% 1/16W MF-LF 402

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

PPDCIN_G3H

C8000 10UF 10% 25V X5R 1206-1

U8000 LT3470 TSOT23-8

VIN BOOST SHDN* SW BIAS NC NC CRITICAL FB GND

P3V42G3H5_BOOST

C8005 0.22uF 20% 6.3V X5R 402

CRITICAL L8010 33uH CDPH4D19F-SM

P3V42G3H_SW

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

C8010 22pF 5% 50V CERM 402

<Ra> R8010 348K 1% 1/16W MF-LF 402

<Rb> R8011 200K 1% 1/16W MF-LF 402

P3V42G3H_FB

PP3V42_G3H

Vout = 3.425
200mA max output
(Switcher limit)

C8015 22UF 20% 6.3V CERM 805

Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

PP3V3_S5

PP1V5_S0

R8061 27.4K 1% 1/16W MF-LF 402

R8063 4.99K 1% 1/16W MF-LF 402

0.89V Reference

P1V0_P1V5PG_REF

P1V5S0_COMP_POS

R8062 10K 1% 1/16W MF-LF 402

R8064 10K 1% 1/16W MF-LF 402

C8060 0.1uF 20% 10V CERM 402

U8060 LMC7211 SM-LF

P1V5S0_PGOOD

R8065 10K 5% 1/16W MF-LF 402

1.5V Comp threshold set to 1.32V (88%)

P1V5P1V05S0_PGOOD

P1V5P1V05S0_PGOOD

P1V5P1V05S0_PGOOD (MAKE_BASE=TRUE)

ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)
NOTE: R8065 acts as 10K pull-up for PGOOD signal

Unused PGOOD Signals

TP_P5V_P1V5_PGOOD — TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE)

TP_P1V8S3_PGOOD — TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)

Other S0 Rails PWRGD Circuit

Does not include D3C rails for GPU!!

PP3V3_S0

PP5V_S0

PP2V5_S0

PPOV9_S0

R8074 68.1K 1% 1/16W MF-LF 402

R8072 365K 1% 1/16W MF-LF 402

R8070 845K 1% 1/16W MF-LF 402

C8070 0.1uF 20% 10V CERM 402

U8070 LTC2903 TSOT-23

S0PGOOD_5V_DIV

S0PGOOD_2V5_DIV

S0PGOOD_0V9_DIV

S0PGOOD_PWROK

R8076 10K 5% 1/16W MF-LF 402

R8075 100K 1% 1/16W MF-LF 402

C8075 0.1UF 20% 10V CERM 402

R8073 100K 1% 1/16W MF-LF 402

C8073 0.1UF 20% 10V CERM 402

R8071 100K 1% 1/16W MF-LF 402

C8071 0.1UF 20% 10V CERM 402

LTC2903 guaranteed threshold is 93.5% (3.055V, 4.725V, 2.325V, 0.840V)

PP3V3_S0

MC74VHC1G08 SC70 U8080

ALL_SYS_PWRGD

PGOOD_MUXED_S0_OR_S0D3C

C8080 0.1UF 20% 10V CERM 402

3.3V G3Hot Supply & Power Control

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 66 OF 87	

"S3AC" rail is ON in S3 on AC, OFF in S3 on battery

Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

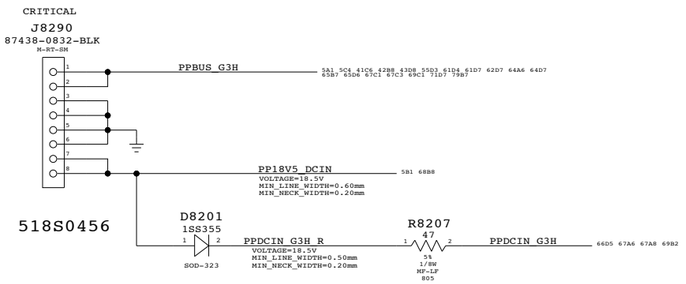
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

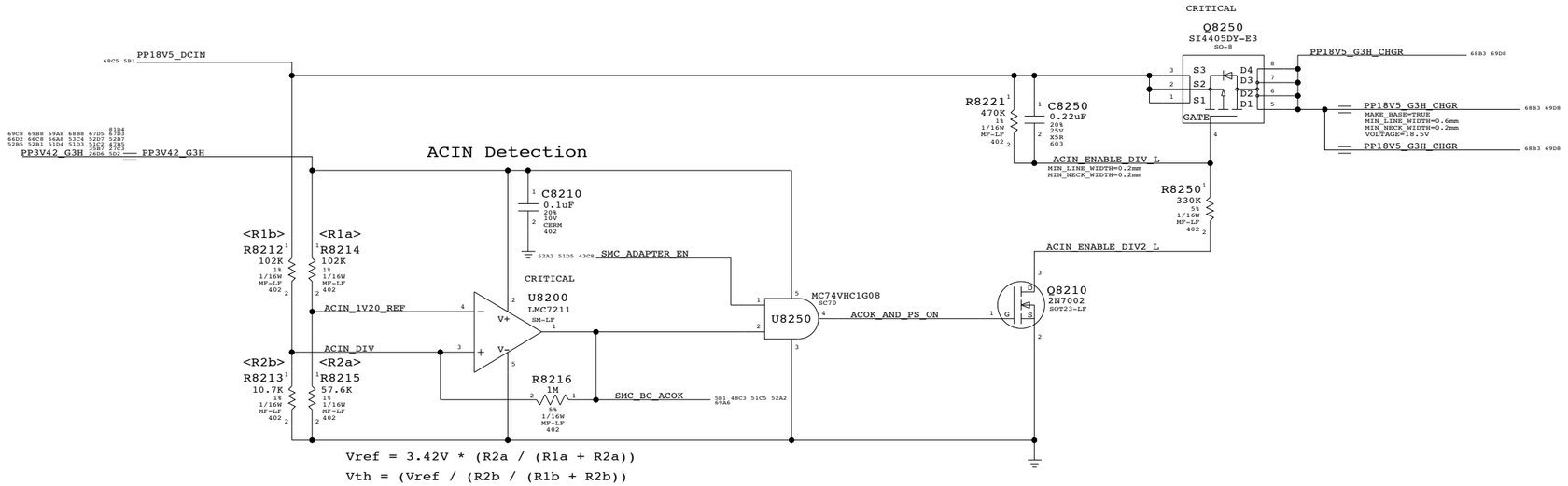
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 67 OF 87	

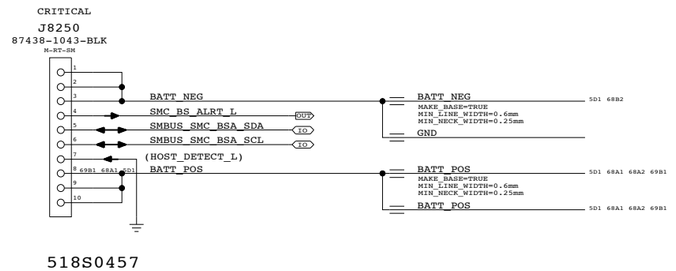
DC-In Connector



Inrush Limiter



Battery Connector



DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	68	87

PBus Supply & Battery Charger

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1510	1	ISL6257H,BATT CHGR,28P,QFN,LF	U8300	CRITICAL	ISL6257H
116S0004	1	0 OHM,5%,1/16W,0402,SMD,LF	R8304		ISL6257H

VOLTAGE FOLLOWER GUARANTEES CURRENT LIMIT CIRCUITS ARE PROVIDED WITH SUFFICIENT CURRENT WITHOUT SINKING CURRENT FROM VREF.

Battery Charge FET

Adapter Input Current Limit

As shown, Isys =-4.6A max

Battery Charge Current Limit

As shown, Ichg = 3.9A max

PBus Supply & Batt. Charger

SYNC_MASTER=M59_LIO SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

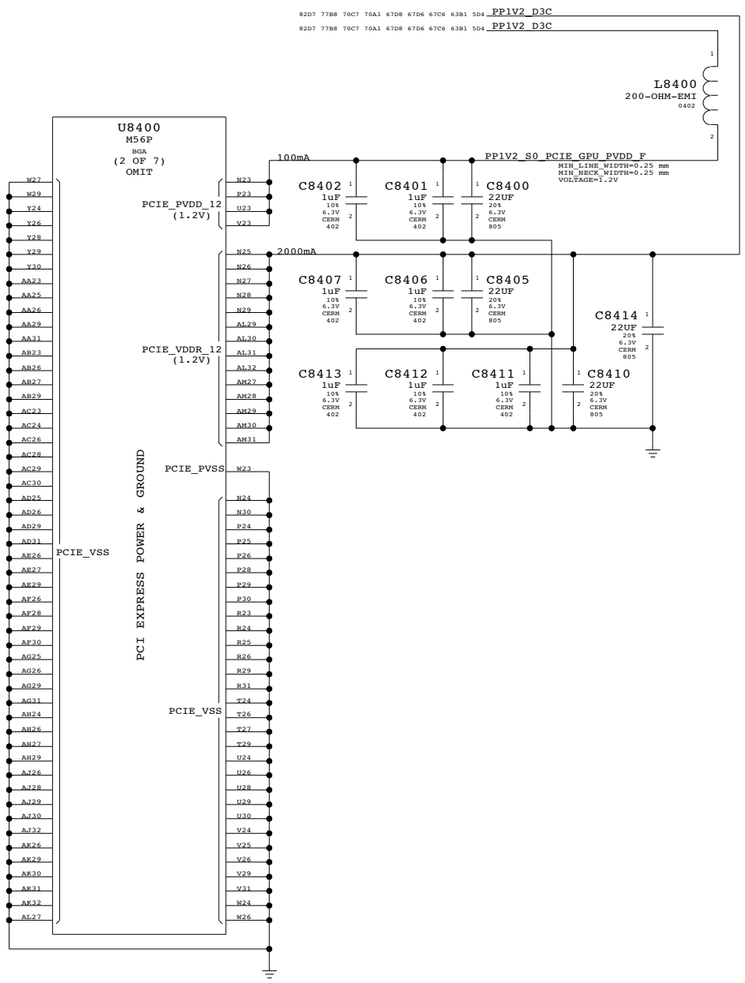
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

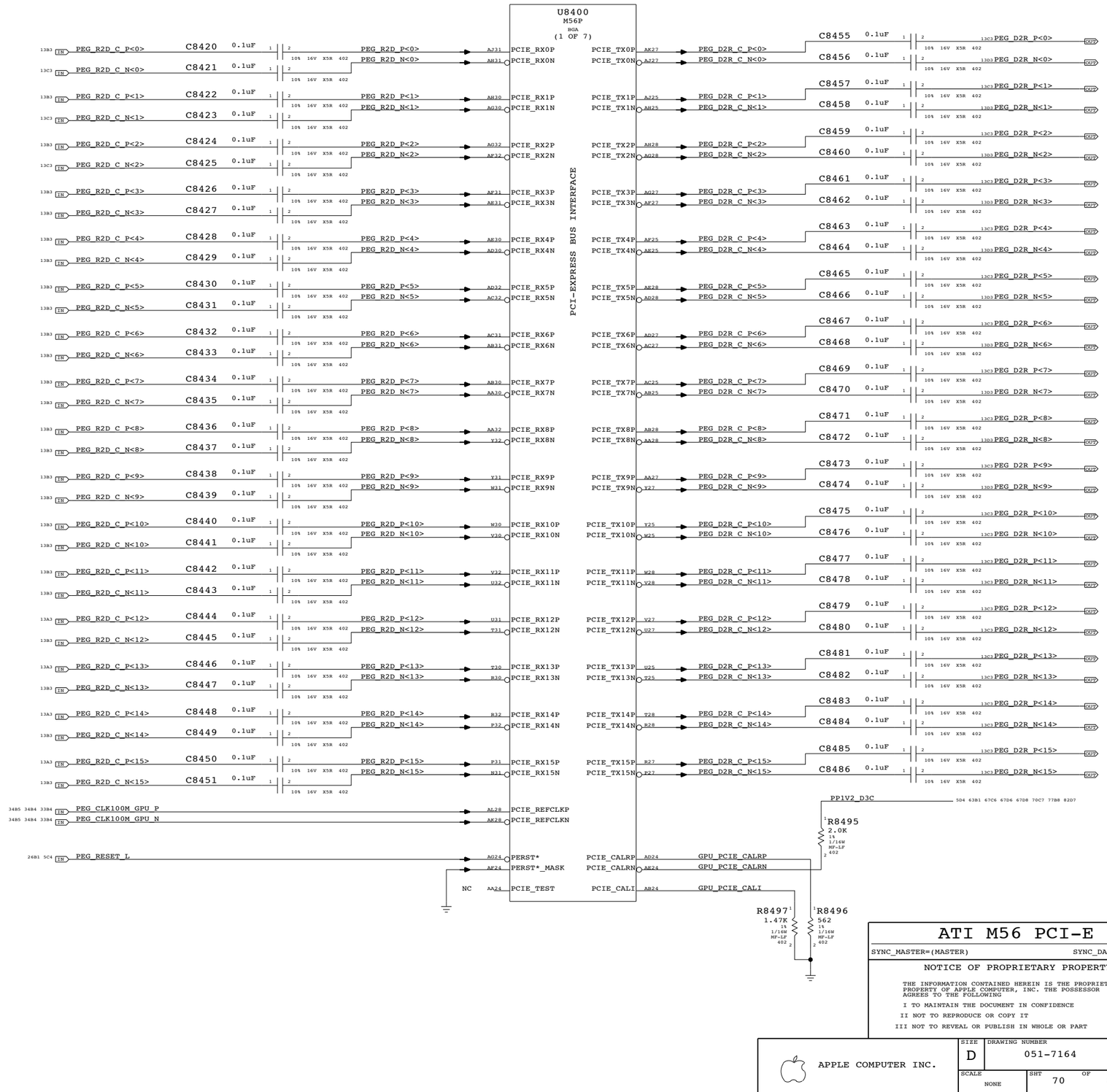
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 69 OF 87	





ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

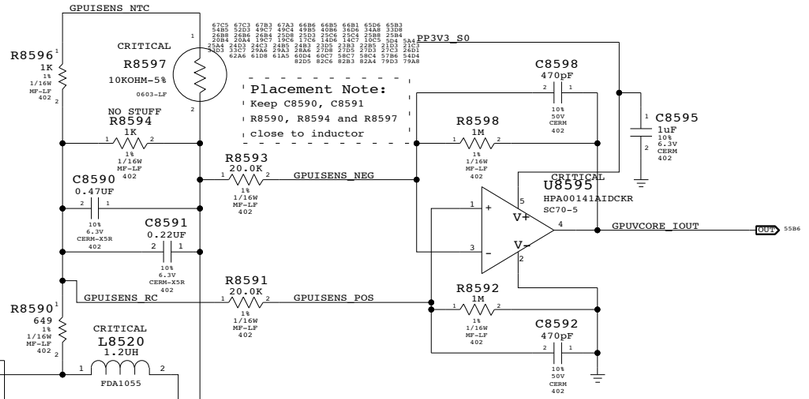
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

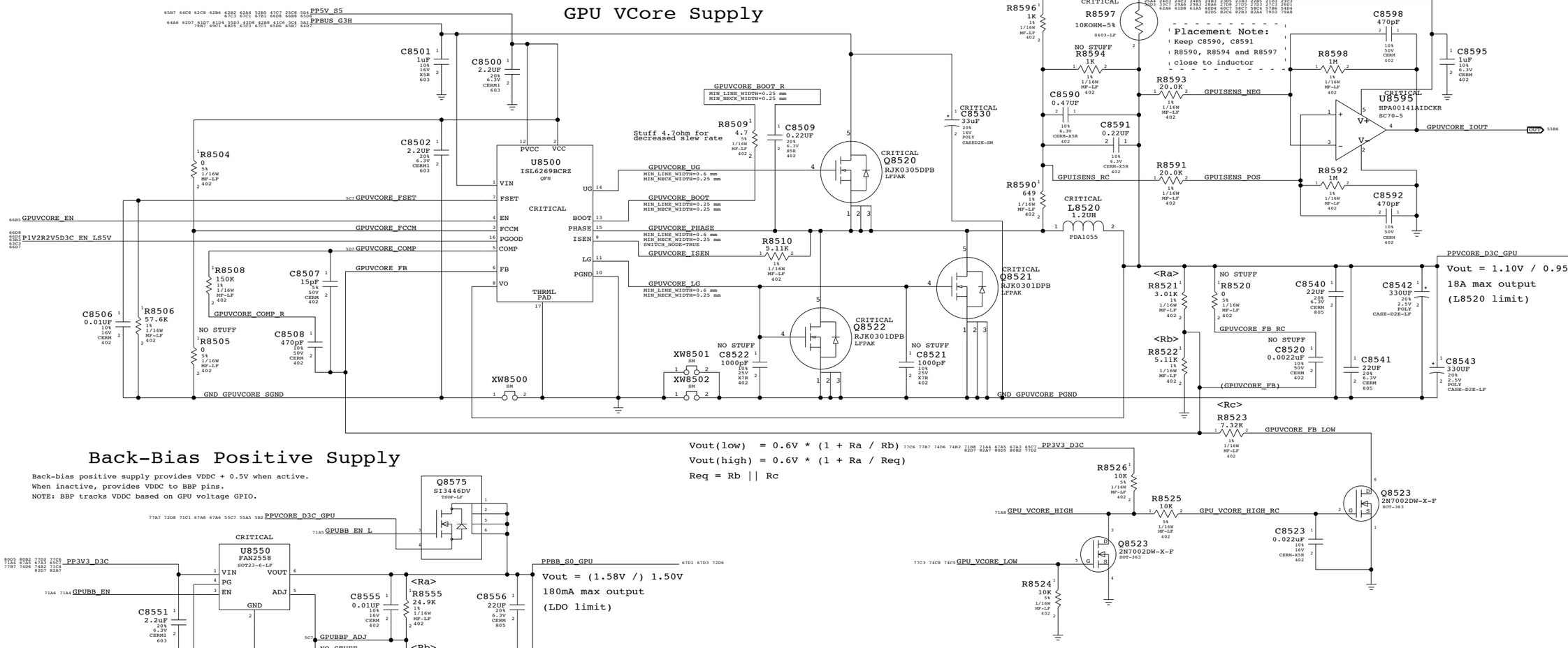
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 70 OF 87	

GPU VCore Current Sense



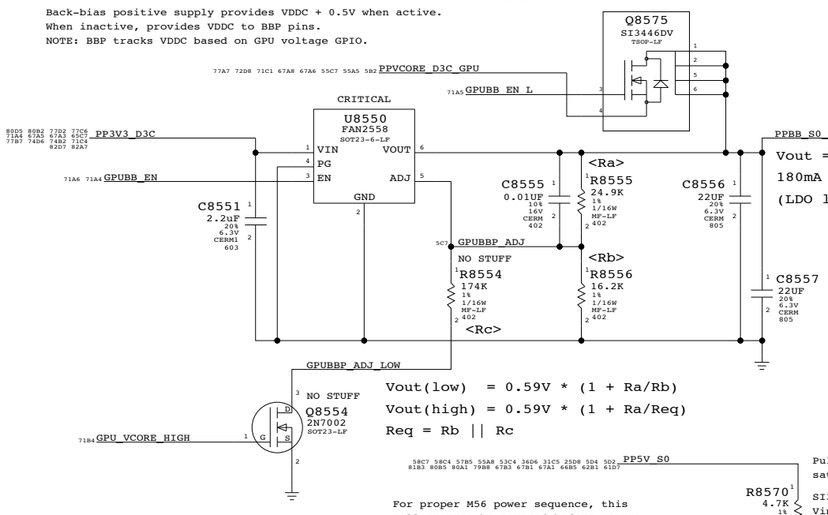
GPU VCore Supply



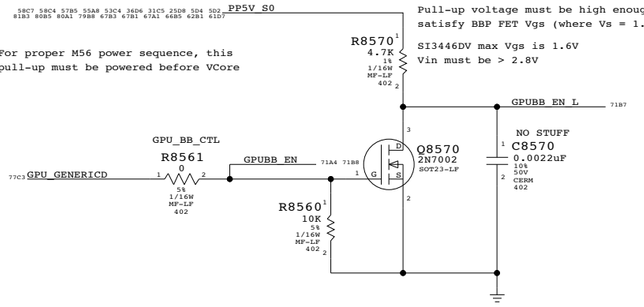
Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.



Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc

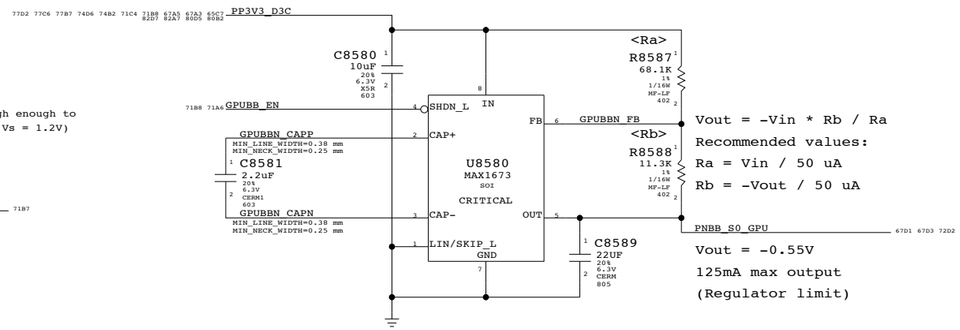


Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
SI3446DV max Vgs is 1.6V
Vin must be > 2.8V

For proper M56 power sequence, this pull-up must be powered before VCore

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active.
When inactive, provides VSS to BBN pins.



Vout = -Vin * Rb / Ra
Recommended values:
Ra = Vin / 50 uA
Rb = -Vout / 50 uA

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

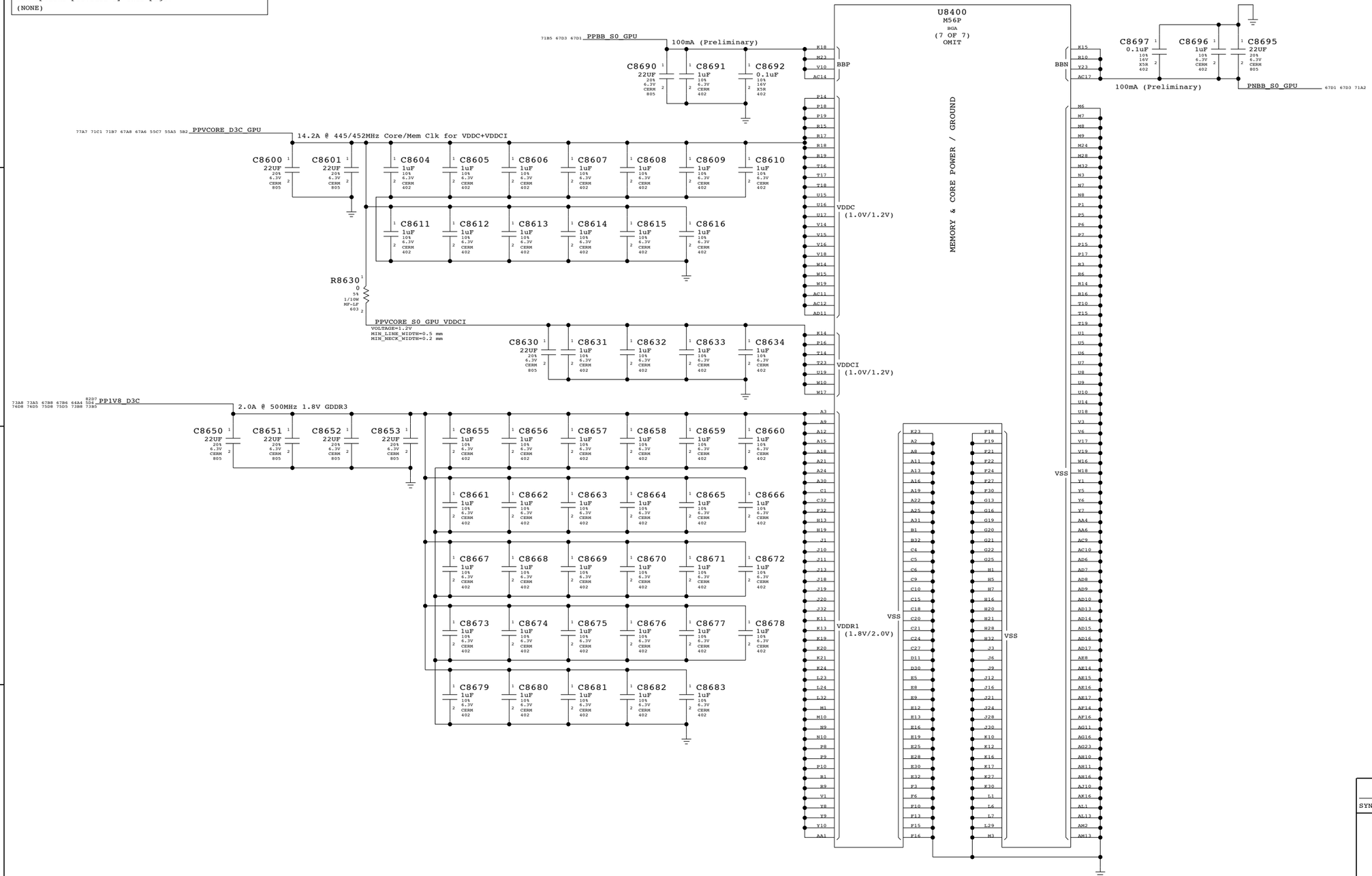
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 71 OF 87	

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

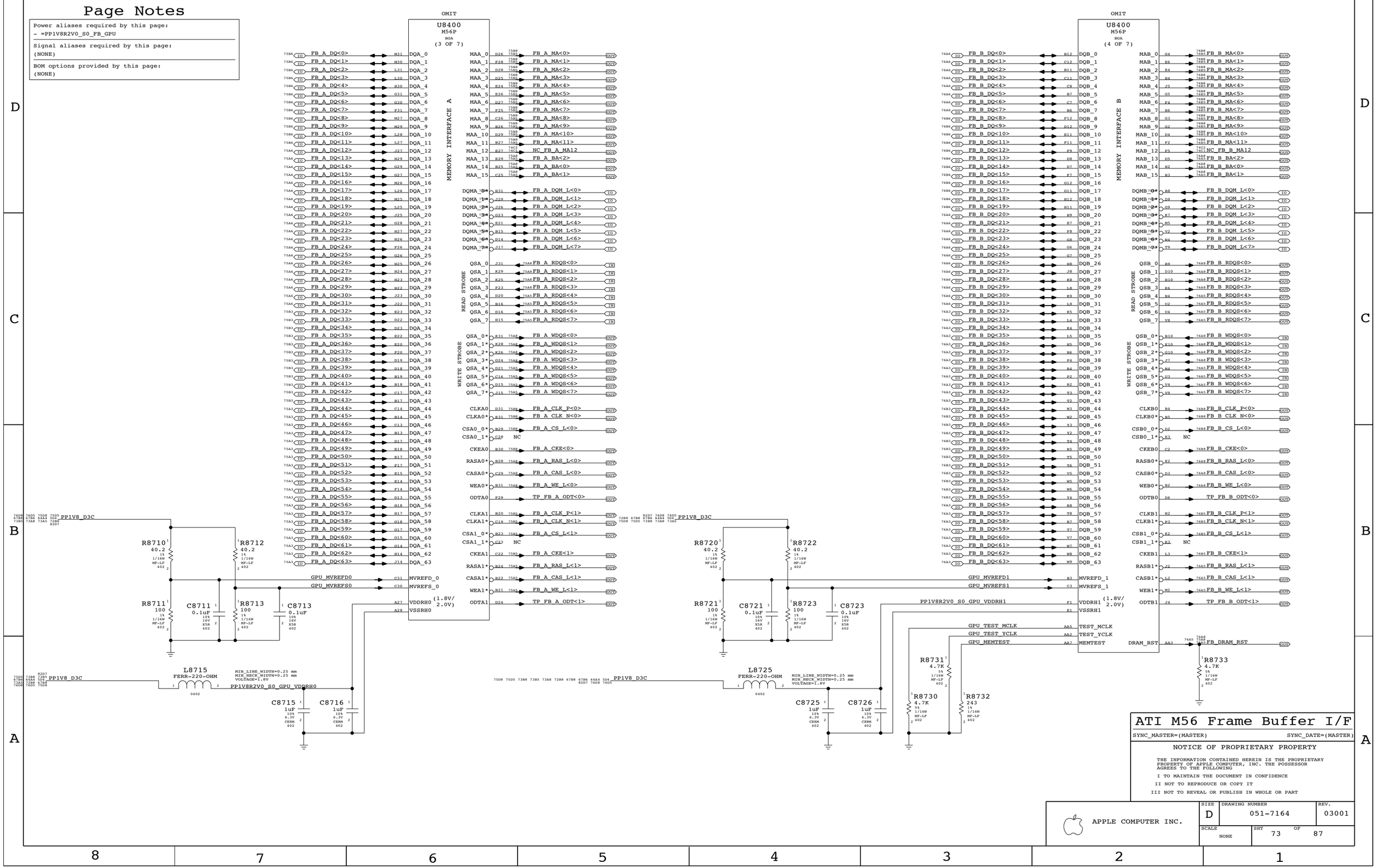
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 72 OF 87	

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 73 OF 87	

ROMCFGID[3..0]

0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

77D2 77C6 77B7 74B2 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 PP3V3_D3C

R8800 10K 5% 1/16W MF-LF 402

GPU_DEEPMH_EN
R8801 10K 5% 1/16W MF-LF 402

NO STUFF
R8802 10K 5% 1/16W MF-LF 402

NO STUFF
R8803 10K 5% 1/16W MF-LF 402

NO STUFF
R8804 10K 5% 1/16W MF-LF 402

NO STUFF
R8805 10K 5% 1/16W MF-LF 402

NO STUFF
R8806 10K 5% 1/16W MF-LF 402

NO STUFF
R8808 10K 5% 1/16W MF-LF 402

NO STUFF
R8809 10K 5% 1/16W MF-LF 402

GPU_MEM_64M
R8813 10K 5% 1/16W MF-LF 402

GPU_MEM_256M
R8811 10K 5% 1/16W MF-LF 402

GPU_MEM_256M
R8812 10K 5% 1/16W MF-LF 402

GPU_MEM_256M
R8824 10K 5% 1/16W MF-LF 402

GPU_MEM_NOT_SAM
R8827 10K 5% 1/16W MF-LF 402

		Serial ROM	TestBus	Misc	Straps
77D3 GPU_GPIO_0	IPD		TESTIN[0]		TX_PWRS_ENb
77D3 GPU_GPIO_1	IPD		TESTIN[1]		TX_DEEMPH_EN
77D3 GPU_GPIO_2		VDD_VCL	TESTIN[2]		Reserved
77D3 GPU_GPIO_3			TESTIN[3]		Reserved
77D3 GPU_GPIO_4	IPD		TESTIN[4]		DEBUG_ACCESS
77D3 GPU_GPIO_5			TESTIN[5]		Reserved
77D3 GPU_GPIO_6			TESTIN[6]		Reserved
82A4 77D3 74C5 GPU_BLON		ENA_BL	TESTIN[7]		
77D3 GPU_GPIO_8		ROMSO	TESTWR		Reserved
77C3 GPU_GPIO_9	IPD	ROMSI			ROMIDCFG[3]
77C3 74C5 TP_GPU_GPIO_10		ROMSCK	TESTOUT[8]		
77C3 GPU_GPIO_11	IPD		TESTOUT[9]		ROMIDCFG[0]
77C3 GPU_GPIO_12	IPD		TESTOUT[10]		ROMIDCFG[1]
77C3 GPU_GPIO_13	IPD		TESTOUT[11]		ROMIDCFG[2]
77C3 74C5 NC_GPU_GPIO_14			TESTIN[8]		
77C3 74C5 71B4 GPU_VCORE_LOW			TESTIN[9]	PWRCNTL	
77C3 74C5 34B4 34B2 GPU_CLK27MSS_IN				SS_IN	
77C3 74C5 NC_GPU_GPIO_17				Thm Mon Int	

GPU_BLON — MAKE_BASE=TRUE — 74C8 77D3 82A4

TP_GPU_GPIO_10 — MAKE_BASE=TRUE — 74C8 77C3 — Required for debug access

Required for debug access

Required for debug access

Required for debug access

NC_GPU_GPIO_14 — MAKE_BASE=TRUE — NO_TEST=TRUE — 74C8 77C3

GPU_VCORE_LOW — MAKE_BASE=TRUE — 71B4 74C8 77C3

GPU_CLK27MSS_IN — MAKE_BASE=TRUE — 34B2 34B4 74C8 77C3

NC_GPU_GPIO_17 — MAKE_BASE=TRUE — NO_TEST=TRUE — 74C8 77C3

77D5 74B7 NC_GPU_GPIO_18 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_18 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_19 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_19 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_20 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_20 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_21 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_21 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_22 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_22 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_23 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_23 — 74B8 77D5
77D5 74B6 GPU_MEM_256M — MAKE_BASE=TRUE NO_TEST=TRUE — 77D5 74B8 GPU_MEM_256M — MAKE_BASE=TRUE
77D5 74B7 NC_GPU_GPIO_25 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_25 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_26 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_26 — 74B8 77D5
77D5 74B6 GPU_MEMID — MAKE_BASE=TRUE NO_TEST=TRUE — 77D5 74B8 GPU_MEMID — MAKE_BASE=TRUE
77D5 74B7 NC_GPU_GPIO_28 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_28 — 74B8 77D5
77C5 74B7 NC_GPU_GPIO_29 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_29 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_30 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_30 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_31 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_31 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_32 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_32 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_33 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_33 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_34 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_34 — 74B8 77C5

Renamed signals

77A5 74C1 34B4 34B2 GPU_CLK27M — MAKE_BASE=TRUE — GPU_CLK27M — 34B2 34B4 74C2 77A5

Unused signals

77A5 74C1 NC_GPU_XTALOUT — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_XTALOUT — 74C2 77A5
77A3 74C1 NC_ATI_ROMCS_L — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_ATI_ROMCS_L — 74C2 77A3
74C1 73D5 NC_FB_A_MA12 — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_FB_A_MA12 — 73D5 74C2
74C1 73D1 NC_FB_B_MA12 — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_FB_B_MA12 — 73D1 74C2
77C3 74C1 NC_GPU_GENERICA — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_GENERICA — 74C2 77C3
77C3 74C1 NC_GPU_GENERICB — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_GENERICB — 74C2 77C3
77C3 74C1 NC_GPU_GENERICC — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_GENERICC — 74C2 77C3
78C3 74C1 NC_GPU_VGA_R — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_VGA_R — 74C2 78C3
78C3 74C1 NC_GPU_VGA_G — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_VGA_G — 74C2 78C3
78C3 74C1 NC_GPU_VGA_B — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_VGA_B — 74C2 78C3
78B3 74C1 TP_GPU_VGA_HSYNC — MAKE_BASE=TRUE — NO_TEST=TRUE — TP_GPU_VGA_HSYNC — 74C2 78B3
78B3 74C1 TP_GPU_VGA_VSYNC — MAKE_BASE=TRUE — NO_TEST=TRUE — TP_GPU_VGA_VSYNC — 74C2 78B3
78B3 74C1 NC_GPU_TV_Y — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_TV_Y — 74C2 78B3
78B3 74B1 NC_GPU_TV_C — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_TV_C — 74B2 78B3
78B3 74B1 NC_GPU_TV_COMP — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_TV_COMP — 74B2 78B3
78B3 74B1 NC_LVDS_U_DATAP<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_LVDS_U_DATAP<3> — 74B2 78B3
78B3 74B1 NC_LVDS_U_DATAN<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_LVDS_U_DATAN<3> — 74B2 78B3
78A3 74B1 NC_LVDS_L_DATAP<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_LVDS_L_DATAP<3> — 74B2 78A3
78A3 74B1 NC_LVDS_L_DATAN<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_LVDS_L_DATAN<3> — 74B2 78A3
77C3 74B1 NC_ATI_DVPCLK — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_ATI_DVPCLK — 74B2 77C3
77C3 77B3 NC_ATI_DVPCNTL<2..0> — MAKE_BASE=TRUE — NO_TEST=TRUE — ATI_DVPCNTL<2..0>
77B3 NC_ATI_DVPDATA<15..0> — MAKE_BASE=TRUE — NO_TEST=TRUE — ATI_DVPDATA<15..0>

Required for debug access

77B3 77A3 TP_ATI_DVPDATA<23..16> — MAKE_BASE=TRUE — ATI_DVPDATA<23..16>

Also required: GPIO10 - GPIO13

77D2 77C6 77B7 74D6 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 PP3V3_D3C

R8890 4.7K 5% 1/16W MF-LF 402

R8891 4.7K 5% 1/16W MF-LF 402

78A3 GPU_DDC_B_CLK
78A3 GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

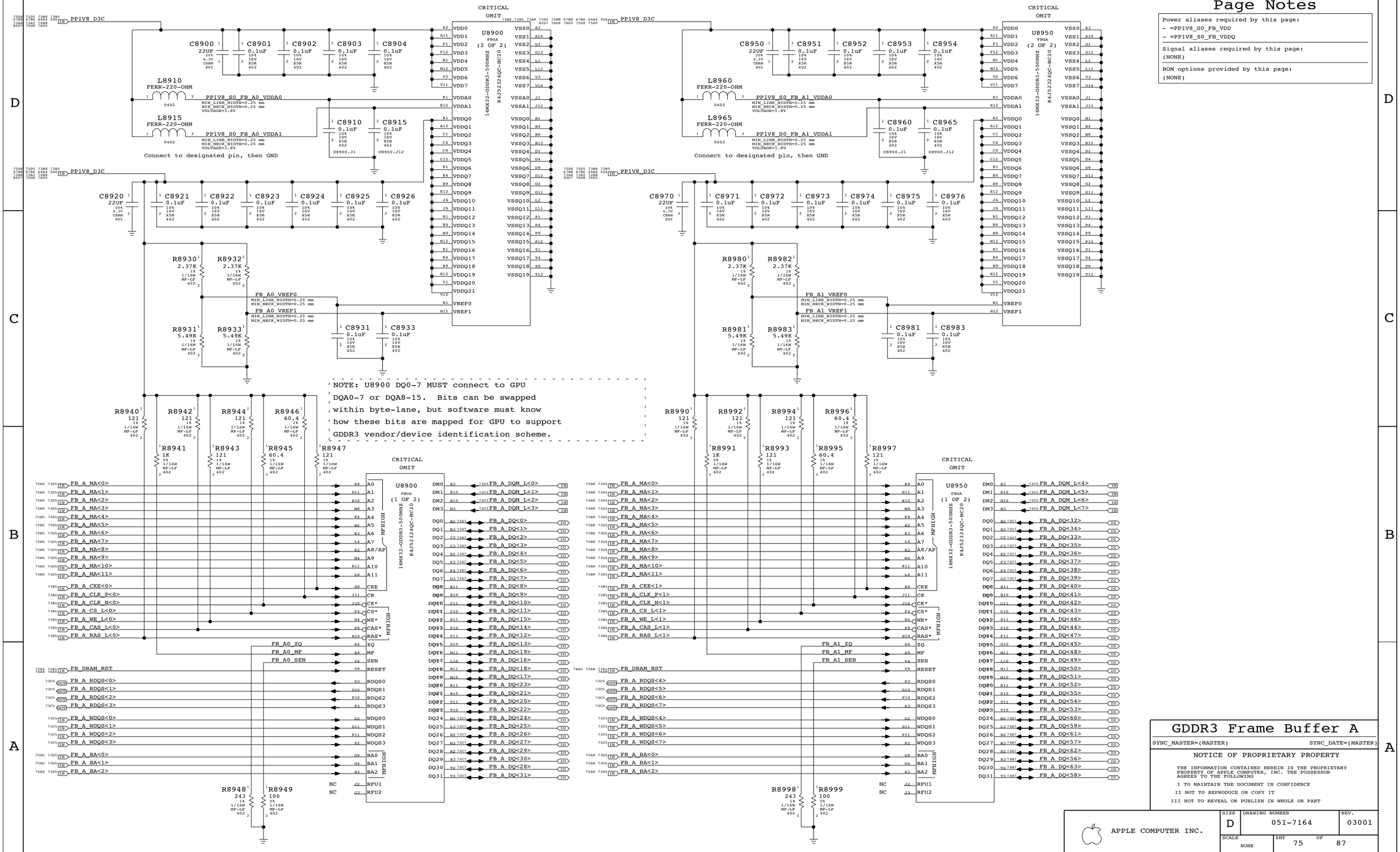
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 74 OF 87	



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

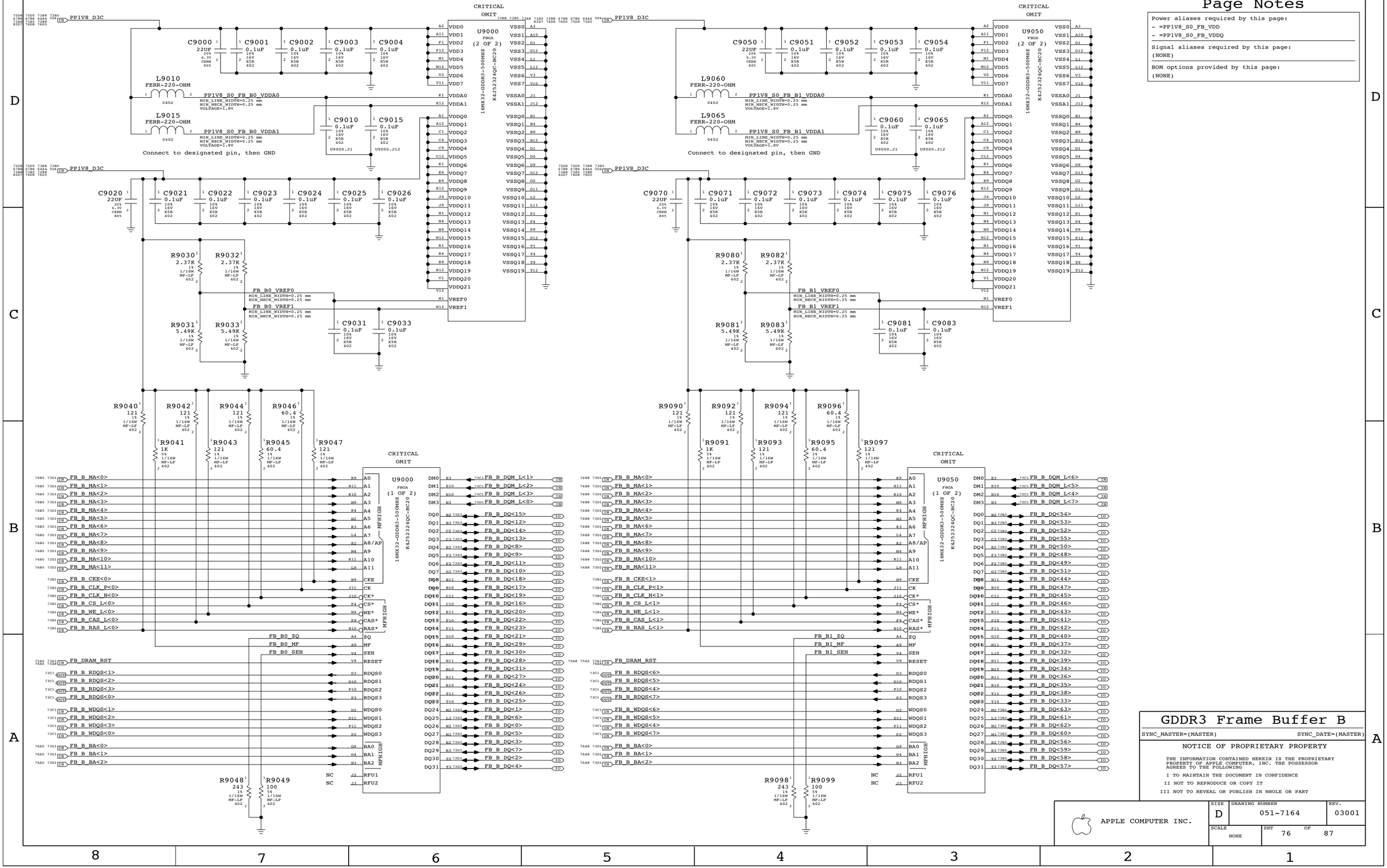
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	75	87


CRITICAL
OMIT
U9000
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20
U9050
(1 OF 2)
PP1V8_D3C
C9000 22UF 20% 6.3V CERM 805
C9001 0.1uF 10% 16V X5R 402
C9002 0.1uF 10% 16V X5R 402
C9003 0.1uF 10% 16V X5R 402
C9004 0.1uF 10% 16V X5R 402
L9010 FERR-220-OHM 0402
L9015 FERR-220-OHM 0402
PP1V8_S0_FB_B0_VDDA0
PP1V8_S0_FB_B0_VDDA1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
Connect to designated pin, then GND
C9010 0.1uF 10% 16V X5R 402
C9015 0.1uF 10% 16V X5R 402
C9020 22UF 20% 6.3V CERM 805
C9021 0.1uF 10% 16V X5R 402
C9022 0.1uF 10% 16V X5R 402
C9023 0.1uF 10% 16V X5R 402
C9024 0.1uF 10% 16V X5R 402
C9025 0.1uF 10% 16V X5R 402
C9026 0.1uF 10% 16V X5R 402
R9030 2.37K 1% 1/16W MF-LF 402
R9032 2.37K 1% 1/16W MF-LF 402
R9031 5.49K 1% 1/16W MF-LF 402
R9033 5.49K 1% 1/16W MF-LF 402
FB_B0_VREF0
FB_B0_VREF1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
C9031 0.1uF 10% 16V X5R 402
C9033 0.1uF 10% 16V X5R 402
R9040 121 1% 1/16W MF-LF 402
R9042 121 1% 1/16W MF-LF 402
R9044 121 1% 1/16W MF-LF 402
R9046 60.4 1% 1/16W MF-LF 402
R9041 1K 5% 1/16W MF-LF 402
R9043 121 1% 1/16W MF-LF 402
R9045 60.4 1% 1/16W MF-LF 402
R9047 121 1% 1/16W MF-LF 402
R9048 243 1% 1/16W MF-LF 402
R9049 100 1% 1/16W MF-LF 402
MFHIGH
MFHIGH_HDT
FB_B_MA<0>
FB_B_MA<1>
FB_B_MA<2>
FB_B_MA<3>
FB_B_MA<4>
FB_B_MA<5>
FB_B_MA<6>
FB_B_MA<7>
FB_B_MA<8>
FB_B_MA<9>
FB_B_MA<10>
FB_B_MA<11>
FB_B_CKE<0>
FB_B_CLK_P<0>
FB_B_CLK_N<0>
FB_B_CS_L<0>
FB_B_WE_L<0>
FB_B_CAS_L<0>
FB_B_RAS_L<0>
FB_B0_ZQ
FB_B0_MF
FB_B0_SEN
FB_DRAM_RST
FB_B_RDQS<1>
FB_B_RDQS<2>
FB_B_RDQS<3>
FB_B_RDQS<0>
FB_B_WDQS<1>
FB_B_WDQS<2>
FB_B_WDQS<3>
FB_B_WDQS<0>
FB_B_BA<0>
FB_B_BA<1>
FB_B_BA<2>
FB_B_DQM_L<1>
FB_B_DQM_L<2>
FB_B_DQM_L<3>
FB_B_DQM_L<0>
FB_B_DQ<15>
FB_B_DQ<12>
FB_B_DQ<14>
FB_B_DQ<13>
FB_B_DQ<8>
FB_B_DQ<9>
FB_B_DQ<11>
FB_B_DQ<10>
FB_B_DQ<18>
FB_B_DQ<17>
FB_B_DQ<19>
FB_B_DQ<16>
FB_B_DQ<20>
FB_B_DQ<22>
FB_B_DQ<23>
FB_B_DQ<21>
FB_B_DQ<29>
FB_B_DQ<30>
FB_B_DQ<28>
FB_B_DQ<31>
FB_B_DQ<27>
FB_B_DQ<24>
FB_B_DQ<26>
FB_B_DQ<25>
FB_B_DQ<1>
FB_B_DQ<6>
FB_B_DQ<0>
FB_B_DQ<5>
FB_B_DQ<3>
FB_B_DQ<7>
FB_B_DQ<2>
FB_B_DQ<4>
C9050 22UF 20% 6.3V CERM 805
C9051 0.1uF 10% 16V X5R 402
C9052 0.1uF 10% 16V X5R 402
C9053 0.1uF 10% 16V X5R 402
C9054 0.1uF 10% 16V X5R 402
L9060 FERR-220-OHM 0402
L9065 FERR-220-OHM 0402
PP1V8_S0_FB_B1_VDDA0
PP1V8_S0_FB_B1_VDDA1
C9060 0.1uF 10% 16V X5R 402
C9065 0.1uF 10% 16V X5R 402
C9070 22UF 20% 6.3V CERM 805
C9071 0.1uF 10% 16V X5R 402
C9072 0.1uF 10% 16V X5R 402
C9073 0.1uF 10% 16V X5R 402
C9074 0.1uF 10% 16V X5R 402
C9075 0.1uF 10% 16V X5R 402
C9076 0.1uF 10% 16V X5R 402
R9080 2.37K 1% 1/16W MF-LF 402
R9082 2.37K 1% 1/16W MF-LF 402
R9081 5.49K 1% 1/16W MF-LF 402
R9083 5.49K 1% 1/16W MF-LF 402
FB_B1_VREF0
FB_B1_VREF1
C9081 0.1uF 10% 16V X5R 402
C9083 0.1uF 10% 16V X5R 402
R9090 121 1% 1/16W MF-LF 402
R9092 121 1% 1/16W MF-LF 402
R9094 121 1% 1/16W MF-LF 402
R9096 60.4 1% 1/16W MF-LF 402
R9091 1K 5% 1/16W MF-LF 402
R9093 121 1% 1/16W MF-LF 402
R9095 60.4 1% 1/16W MF-LF 402
R9097 121 1% 1/16W MF-LF 402
R9098 243 1% 1/16W MF-LF 402
R9099 100 1% 1/16W MF-LF 402
FB_B1_ZQ
FB_B1_MF
FB_B1_SEN
Page Notes
Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
GDDR3 Frame Buffer B
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7164
REV. 03001
SCALE NONE
SHT 76 OF 87

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)

OMIT

U8400
M56P
BGA
(6 OF 7)

GENERAL PURPOSE I/O

NC_GPU_GPIO_18	AE13	GPIO_18	
NC_GPU_GPIO_19	AF13	GPIO_19	
NC_GPU_GPIO_20	AF9	GPIO_20	
NC_GPU_GPIO_21	AG7	GPIO_21	
NC_GPU_GPIO_22	AE10	GPIO_22	
NC_GPU_GPIO_23	AE9	GPIO_23	
GPU_MEM_256M	AF7	GPIO_24	
NC_GPU_GPIO_25	AF8	GPIO_25	
NC_GPU_GPIO_26	AH6	GPIO_26	
GPU_MEMID	AF10	GPIO_27	
NC_GPU_GPIO_28	AG10	GPIO_28	
NC_GPU_GPIO_29	AH9	GPIO_29	
NC_GPU_GPIO_30	AJ8	GPIO_30	
NC_GPU_GPIO_31	AH8	GPIO_31	
NC_GPU_GPIO_32	AG9	GPIO_32	
NC_GPU_GPIO_33	AH7	GPIO_33	
NC_GPU_GPIO_34	AG8	GPIO_34	

VREFG	AC8	ATI_VREFG	
GPIO_0	AD4	GPU_GPIO_0	74D8
GPIO_1	AD2	GPU_GPIO_1	74C8
GPIO_2	AD1	GPU_GPIO_2	74C8
GPIO_3	AD3	GPU_GPIO_3	74C8
GPIO_4	AC1	GPU_GPIO_4	74C8
GPIO_5	AC2	GPU_GPIO_5	74C8
GPIO_6	AC3	GPU_GPIO_6	74C8
GPIO_7_BLON	AB2	GPU_BLON	74C5 74C8 82A4
GPIO_8	AC6	GPU_GPIO_8	74C8
GPIO_9	AC5	GPU_GPIO_9	74C8
GPIO_10	AC4	TP_GPU_GPIO_10	74C5 74C8
GPIO_11	AB3	GPU_GPIO_11	74C8
GPIO_12	AB4	GPU_GPIO_12	74C8
GPIO_13	AB5	GPU_GPIO_13	74C8
GPIO_14	AD5	NC_GPU_GPIO_14	74C5 74C8
GPIO_15	AB8	GPU_VCORE_LOW	71B4 74C5 74C8
GPIO_16	AA8	GPU_CLK27MSS_IN	34B2 34B4 74C5 74C8
GPIO_17	AB7	NC_GPU_GPIO_17	74C5 74C8

GENERICA	AK22	NC_GPU_GENERICA	74C1 74C2
GENERICB	AF23	NC_GPU_GENERICB	74C1 74C2
GENERICC	AE23	NC_GPU_GENERICC	74C1 74C2
GENERICD	AD23	GPU_GENERICD	71A7

PANEL CONTROL

DIGON	AE11	GPU_DIGON	82A4 82B6
VARY_BL	AD12	GPU_VARY_BL	82A4

NC0	AB6	NC	
NC_DVOVMODE_0	AK4	NC	
NC_DVOVMODE_1	AL4	NC	

VIP HOST / EXTERNAL TMDS

DVPCLK	AG1	NC_ATI_DVPCLK	74B1 74B2
DVPCNTL_0	AF2	NC_ATI_DVPCNTL<0>	74B2
DVPCNTL_1	AF1	NC_ATI_DVPCNTL<1>	74B2
DVPCNTL_2	AF3	NC_ATI_DVPCNTL<2>	74B2
DVPDATA_0	AG2	NC_ATI_DVPDATA<0>	74B2
DVPDATA_1	AG3	NC_ATI_DVPDATA<1>	74B2
DVPDATA_2	AH2	NC_ATI_DVPDATA<2>	74B2
DVPDATA_3	AH3	NC_ATI_DVPDATA<3>	74B2
DVPDATA_4	AJ2	NC_ATI_DVPDATA<4>	74B2
DVPDATA_5	AJ1	NC_ATI_DVPDATA<5>	74B2
DVPDATA_6	AK2	NC_ATI_DVPDATA<6>	74B2
DVPDATA_7	AK1	NC_ATI_DVPDATA<7>	74B2
DVPDATA_8	AK3	NC_ATI_DVPDATA<8>	74B2
DVPDATA_9	AL2	NC_ATI_DVPDATA<9>	74B2
DVPDATA_10	AL3	NC_ATI_DVPDATA<10>	74B2
DVPDATA_11	AM1	NC_ATI_DVPDATA<11>	74B2
DVPDATA_12	AR6	NC_ATI_DVPDATA<12>	74B2
DVPDATA_13	AP4	NC_ATI_DVPDATA<13>	74B2
DVPDATA_14	AP5	NC_ATI_DVPDATA<14>	74B2
DVPDATA_15	AG4	NC_ATI_DVPDATA<15>	74B2
DVPDATA_16	AJ3	TP_ATI_DVPDATA<16>	74B2
DVPDATA_17	AH4	TP_ATI_DVPDATA<17>	74B2
DVPDATA_18	AJ4	TP_ATI_DVPDATA<18>	74B2
DVPDATA_19	AG5	TP_ATI_DVPDATA<19>	74B2
DVPDATA_20	AH5	TP_ATI_DVPDATA<20>	74B2
DVPDATA_21	AP6	TP_ATI_DVPDATA<21>	74B2
DVPDATA_22	AE7	TP_ATI_DVPDATA<22>	74B2
DVPDATA_23	AG6	TP_ATI_DVPDATA<23>	74B2

PLL & XTAL

THERMAL DIODE DPLUS	AG12	ATI_TDIODE_P	54B6
THERMAL DIODE DMINUS	AH12	ATI_TDIODE_N	54B6
ROM ROMCS*	AC7	NC_ATI_ROMCS_L	74C1 74C2
TEST TESTEN	AG22	ATI_TESTEN	
	AM26	XTALOUT	74C2 74C1 NC_GPU_XTALOUT
	AL26	XTALIN	74C1 34B4 34B2 74C2 GPU_CLK27M
NC	AG14	PLLTEST	

77C6 77B7 74D6 74B2 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 PP3V3_D3C

R9190 499 1% 1/16W MF-LF 402

C9191 0.1uF 10% 16V X5R 402

R9191 499 1% 1/16W MF-LF 402

77D2 77B7 74D6 74B2 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 PP3V3_D3C

Typically <50mA

C9100 22UF 20% 6.3V CERM 805

C9101 C9102 C9103 1uF 10% 6.3V CERM 402

VDDR3 (3.3V)

82D7 78C8 77C6 77A8 67A8 67A6 63C1 5D4 PP2V5_D3C

70mA total for VDD25

C9110 22UF 20% 6.3V CERM 805

C9111 1uF 10% 6.3V CERM 402

C9112 0.1uF 10% 16V X5R 402

VDD25 (2.5V)

82D7 78C8 77C6 77A8 67A8 67A6 63C1 5D4 PP2V5_D3C

C9115 22UF 20% 6.3V CERM 805

C9116 C9117 1uF 10% 6.3V CERM 402

77C6 77B7 74D6 74B2 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 77D2 PP3V3_D3C

L9120 FERR-220-OHM 0402

Typically <50mA

PP1V8R3V3_S0_GPU_VDDR4_F

MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

C9120 22UF 20% 6.3V CERM 805

C9121 1uF 10% 6.3V CERM 402

C9122 0.1uF 10% 16V X5R 402

VDDR4 (1.8V/3.3V)

77C6 77B7 74D6 74B2 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 77D2 PP3V3_D3C

L9125 FERR-220-OHM 0402

Typically <50mA

PP1V8R3V3_S0_GPU_VDDR5_F

MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

C9125 22UF 20% 6.3V CERM 805

C9126 1uF 10% 6.3V CERM 402

C9127 0.1uF 10% 16V X5R 402

VDDR5 (1.8V/3.3V)

82D7 70C7 70A1 67D8 67D6 67C6 63B1 5D4 PP1V2_D3C

L9130 200-OHM-EMI 0402

PP1V2_S0_GPU_VDDPLL

MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

20mA

C9130 22UF 20% 6.3V CERM 805

C9131 C9132 1uF 10% 6.3V CERM 402

(PP2V5_S0_GPU_PVDD_F)

(PP1V0R1V2_S0_GPU_MPVDD)

82D7 78C8 77C6 67A8 67A6 63C1 5D4 PP2V5_D3C

L9135 FERR-220-OHM 0402

PP2V5_S0_GPU_PVDD_F

MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V

100mA

C9135 22UF 20% 6.3V CERM 805

C9136 1uF 10% 6.3V CERM 402

C9137 0.1uF 10% 16V X5R 402

72D8 71C1 71B7 67A8 67A6 55C7 55A5 5B2 PPVCORE_D3C_GPU

L9140 FERR-220-OHM 0402

PPVCORE_S0_GPU_MPVDD

MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

20mA

C9140 22UF 20% 6.3V CERM 805

C9141 C9142 1uF 10% 6.3V CERM 402

R9195 1K 5% 1/16W MF-LF 402

ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	77	87

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents on this page: 605mA

PP2V5_D3C

L9300 FERR-220-OHM 0402 — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9300 22UF 20% 6.3V CERM 805; C9301 1uF 10% 6.3V CERM 402; C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 150mA peak
C9305 22UF 20% 6.3V CERM 805; C9306 1uF 10% 6.3V CERM 402; C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 65mA peak
C9310 22UF 20% 6.3V CERM 805; C9311 1uF 10% 6.3V CERM 402; C9312 0.1uF 10% 16V X5R 402

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9315 22UF 20% 6.3V CERM 805; C9316 1uF 10% 6.3V CERM 402; C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 130mA peak
C9320 22UF 20% 6.3V CERM 805; C9321 1uF 10% 6.3V CERM 402; C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9325 22UF 20% 6.3V CERM 805; C9326 1uF 10% 6.3V CERM 402; C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9330 22UF 20% 6.3V CERM 805; C9331 1uF 10% 6.3V CERM 402; C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 200mA peak
C9340 22UF 20% 6.3V CERM 805; C9345 22UF 20% 6.3V CERM 805; C9341 1uF 10% 6.3V CERM 402; C9342 0.1uF 10% 16V X5R 402; C9346 0.1uF 10% 16V X5R 402; C9347 0.1uF 10% 16V X5R 402

OMIT

U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
- TPVDD (2.5V) — AM8
- TPVSS — AL8
- TXVDDR (2.5V) — AJ6, AK6, AL6, AM6
- TXVSSR — AJ7, AK7, AK8, AL7, AM7

DAC (CRT)
- AVDD (2.5V) — AL25, AM25
- AVSS — AJ24, AK25
- AVSSQ — AK23
- VDD1DI (2.5V) — AM23
- VSS1DI — AL23
- RSET — AL22 (78A8 ATI_RSET)

DAC2 (TV/CRT2)
- A2VDD (2.5V) — AL16, AM16
- A2VSS — AL17, AM17
- NC_A2VDDQ — NC, AL14
- A2VSSQ — AK13
- VDD2DI (2.5V) — AJ16
- VSS2DI — AJ17
- R2SET — AK14 (78A8 ATI_R2SET)

LVDS
- LPVDD (2.5V) — AK19
- LPVSS — AK18
- LVDDR (2.5V) — AC21, AC22, AD21, AD22, AE20, AE21, AE22, AF19, AF20
- LVSSR — AF17, AF18, AF21, AF22, AG17, AG19, AH17, AH19, AJ19, AK17

MONITOR IDENTIFICATION
- GPU_HPD (80A2, I/O) — AF11 HPD1

TMDS
- TXCP AM9 — TMDS_CLK_P
- TXCM AL9 — TMDS_CLK_N
- TX0P AL10 — TMDS_DATA_P<0>
- TX0M AK10 — TMDS_DATA_N<0>
- TX1P AM11 — TMDS_DATA_P<1>
- TX1M AL11 — TMDS_DATA_N<1>
- TX2P AM12 — TMDS_DATA_P<2>
- TX2M AL12 — TMDS_DATA_N<2>
- TX3P AJ9 — TMDS_DATA_P<3>
- TX3M AK9 — TMDS_DATA_N<3>
- TX4P AJ11 — TMDS_DATA_P<4>
- TX4M AK11 — TMDS_DATA_N<4>
- TX5P AJ12 — TMDS_DATA_P<5>
- TX5M AK12 — TMDS_DATA_N<5>

VGA
- R AK24 — NC_GPU_VGA_R
- G AM24 — NC_GPU_VGA_G
- B AL24 — NC_GPU_VGA_B
- HSYNC AJ23 — TP_GPU_VGA_HSYNC
- VSYNC AJ22 — TP_GPU_VGA_VSYNC
- R2 AK15 — GPU_R2
- G2 AM15 — GPU_G2
- B2 AL15 — GPU_B2
- H2SYNC AF15 — GPU_H2SYNC
- V2SYNC AG15 — GPU_V2SYNC

Composite/S-Video
- Y AJ15 — NC_GPU_TV_Y
- C AJ13 — NC_GPU_TV_C
- COMP AM15 — NC_GPU_TV_COMP

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

LVDS
- TXCLK_UP AJ21 — LVDS_U_CLK_P
- TXCLK_UN AK21 — LVDS_U_CLK_N
- TXOUT_U0P AG18 — LVDS_U_DATA_P<0>
- TXOUT_U0N AH18 — LVDS_U_DATA_N<0>
- TXOUT_U1P AK20 — LVDS_U_DATA_P<1>
- TXOUT_U1N AJ20 — LVDS_U_DATA_N<1>
- TXOUT_U2P AG20 — LVDS_U_DATA_P<2>
- TXOUT_U2N AH20 — LVDS_U_DATA_N<2>
- TXOUT_U3P AH21 — NC_LVDS_U_DATAP<3>
- TXOUT_U3N AG21 — NC_LVDS_U_DATAN<3>
- TXCLK_LP AM18 — LVDS_L_CLK_P
- TXCLK_LN AL18 — LVDS_L_CLK_N
- TXOUT_L0P AL19 — LVDS_L_DATA_P<0>
- TXOUT_L0N AK19 — LVDS_L_DATA_N<0>
- TXOUT_L1P AM20 — LVDS_L_DATA_P<1>
- TXOUT_L1N AL20 — LVDS_L_DATA_N<1>
- TXOUT_L2P AM21 — LVDS_L_DATA_P<2>
- TXOUT_L2N AL21 — LVDS_L_DATA_N<2>
- TXOUT_L3P AJ18 — NC_LVDS_L_DATAP<3>
- TXOUT_L3N AK18 — NC_LVDS_L_DATAN<3>

MONITOR IDENTIFICATION
- DDC1CLK AH23 — GPU_DDC_A_CLK
- DDC1DATA AH22 — GPU_DDC_A_DATA
- DDC2CLK AG13 — GPU_DDC_B_CLK
- DDC2DATA AH13 — GPU_DDC_B_DATA
- DDC3CLK AF12 — GPU_DDC_C_CLK
- DDC3DATA AE12 — GPU_DDC_C_DATA

ATI_RSET (78B5) — R9350 499 1% 1/16W MF-LF 402
ATI_R2SET (78B5) — R9351 715 1% 1/16W MF-LF 402

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 78 OF 87	

LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
	VGA	VGA	GPU_R2
	VGA	VGA	GPU_G2
	VGA	VGA	GPU_B2
	LVDS	LVDS	LVDS_U_CLK_P
	LVDS	LVDS	LVDS_U_CLK_N
	LVDS	LVDS	LVDS_U_DATA_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_P
	LVDS	LVDS	LVDS_L_CLK_N
	LVDS	LVDS	LVDS_L_DATA_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_N<2..0>
	LVDS	LVDS	LVDS_U_CLK_CONN_P
	LVDS	LVDS	LVDS_U_CLK_CONN_N
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_CONN_P
	LVDS	LVDS	LVDS_L_CLK_CONN_N
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>
	TMDS	TMDS	TMDS_CLK_P
	TMDS	TMDS	TMDS_CLK_N
	TMDS	TMDS	TMDS_DATA_P<5..3>
	TMDS	TMDS	TMDS_DATA_N<5..3>
	TMDS	TMDS	TMDS_DATA_P<2..0>
	TMDS	TMDS	TMDS_DATA_N<2..0>

PP3V3_S5

R9400 100K 5% 1/16W MF-LF 402

C9400 0.0022uF 10% 50V CERM 402

R9401 100K 5% 1/16W MF-LF 402

LCD_PWREN_L_RC

Q9400 SI3443DV TSOP-LF

PP3V3_LCD_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

L9400 FERR-250-OHM SM

C9401 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

LCD_PWREN_L

Q9401 2N7002 SOT23-LF

LVDS_PANEL_EN

R9494 100K 5% 1/16W MF-LF 402

PP3V3_S0

100K pull-ups are for no-panel case (development). Panel has 2K pull-ups

R9410 100K 5% 1/16W MF-LF 402

R9411 100K 5% 1/16W MF-LF 402

LVDS_CONN_DDC_CLK

LVDS_CONN_DDC_DATA

C9410 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

CRITICAL
J9400 MSC-RB30-5-FA F-RT-SM

C9420 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

PP3V3_LCD_CONN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

NC

LVDS_L_DATA_CONN_N<0>
LVDS_L_DATA_CONN_P<0>
LVDS_L_DATA_CONN_N<1>
LVDS_L_DATA_CONN_P<1>
LVDS_L_DATA_CONN_N<2>
LVDS_L_DATA_CONN_P<2>
LVDS_L_CLK_CONN_N
LVDS_L_CLK_CONN_P
LVDS_U_DATA_CONN_N<0>
LVDS_U_DATA_CONN_P<0>
LVDS_U_DATA_CONN_N<1>
LVDS_U_DATA_CONN_P<1>
LVDS_U_DATA_CONN_N<2>
LVDS_U_DATA_CONN_P<2>
LVDS_U_CLK_CONN_N
LVDS_U_CLK_CONN_P

C9421 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

518S0289

INVERTER INTERFACE

CRITICAL
L9450 FERR-220-OHM-2A 0603

PPBUS_G3H

PPBUS_S0_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.8V

C9450 0.001uF 20% 50V CERM 402

Q9450 FDG6332C_NL SC70-6 P-CHN

PP5V_S0

R9450 100K 5% 1/16W MF-LF 402

PP5V_INVERTER_SW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

L9452 400-OHM-EMI SM-1

C9451 10UF 20% 6.3V X5R 603

FP_PWR_EN_L

Q9450 FDG6332C_NL SC70-6 N-CHN

INVERTER_BKLTON

R9489 100K 5% 1/16W MF-LF 402

PP5V_INVERTER_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

C9452 0.001uF 20% 50V CERM 402

INVERTER_PWM

GND_CHASSIS_INVERTER

CRITICAL
J9450 SM04B-ACH M-RT-SM

NC

518S0369

L9454 400-OHM-EMI SM-1

C9454 0.001uF 20% 50V CERM 402

GND_CHASSIS_INVERTER

CRITICAL
L9455 FERR-220-OHM-2A 0603

PP3V3_S0

PLT_RST_L

INVERTER_PWM_UNBUF

U9453 MC74VHC1G08 SC70

INVERTER_PWM_F

INVERTER EXPECTS ACTIVE HIGH PWM SIGNAL

C9453 0.1uF 20% 10V CERM 402

Internal Display Connectors	
SYNC_MASTER=M57_MLB_MG	SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 79 OF 87	

TMDS Filtering

Place termination components close to GPU, common mode chokes near connector.

TMDS_DATA_N<0> — TMDS_DATA_RL<0> (VOLTAGE=0V, NO_TEST=TRUE) — L9743 47nH 0402 — R9762 182 1% 1/16W MF-LF 402 — TMDS_DATA_P<0>

TMDS_DATA_N<1> — TMDS_DATA_RL<1> (VOLTAGE=0V, NO_TEST=TRUE) — L9744 47nH 0402 — R9766 182 1% 1/16W MF-LF 402 — TMDS_DATA_P<1>

TMDS_DATA_N<2> — TMDS_DATA_RL<2> (VOLTAGE=0V, NO_TEST=TRUE) — L9745 47nH 0402 — R9770 182 1% 1/16W MF-LF 402 — TMDS_DATA_P<2>

TMDS_CLK_N — R9772 0 5% 1/16W MF-LF 402 — TMDS_CLK_R_N
TMDS_CLK_P — R9774 182 1% 1/16W MF-LF 402 — R9773 0 5% 1/16W MF-LF 402 — TMDS_CLK_R_P

TMDS_DATA_N<3> — TMDS_DATA_RL<3> (VOLTAGE=0V, NO_TEST=TRUE) — L9746 47nH 0402 — R9778 182 1% 1/16W MF-LF 402 — TMDS_DATA_P<3>

TMDS_DATA_N<4> — TMDS_DATA_RL<4> (VOLTAGE=0V, NO_TEST=TRUE) — L9747 47nH 0402 — R9782 182 1% 1/16W MF-LF 402 — TMDS_DATA_P<4>

TMDS_DATA_N<5> — TMDS_DATA_RL<5> (VOLTAGE=0V, NO_TEST=TRUE) — L9748 47nH 0402 — R9786 182 1% 1/16W MF-LF 402 — TMDS_DATA_P<5>

CRITICAL
L9700 90-OHM-100MA 1210-4SM1 (SYM_VER=1)
TMDS_DATA_F_N<0> — TMDS_DATA_F_P<0>

CRITICAL
L9701 90-OHM-100MA 1210-4SM1 (SYM_VER=1)
TMDS_DATA_F_N<1> — TMDS_DATA_F_P<1>

CRITICAL
L9702 90-OHM-100MA 1210-4SM1 (SYM_VER=1)
TMDS_DATA_F_N<2> — TMDS_DATA_F_P<2>

CRITICAL
L9706 370-OHM 6M (SYM_VER=1)
TMDS_CLK_F_N — TMDS_CLK_F_P

CRITICAL
L9703 90-OHM-100MA 1210-4SM1 (SYM_VER=1)
TMDS_DATA_F_N<3> — TMDS_DATA_F_P<3>

CRITICAL
L9704 90-OHM-100MA 1210-4SM1 (SYM_VER=1)
TMDS_DATA_F_N<4> — TMDS_DATA_F_P<4>

CRITICAL
L9705 90-OHM-100MA 1210-4SM1 (SYM_VER=1)
TMDS_DATA_F_N<5> — TMDS_DATA_F_P<5>

VGA SYNC BUFFERS

PP3V3_D3C — C9750 0.1uF 20% 10V CERM 402 — U9750 MC74VHC1G08 SC70
GPU_V2SYNC — U9750 — VGA_VSYNC_R — R9750 33 5% 1/16W MF-LF 402 — VGA_VSYNC

PLACE U9750 & U9751 CLOSE TO DVI CONNECTOR

PP3V3_D3C — C9751 0.1uF 20% 10V CERM 402 — U9751 MC74VHC1G08 SC70
GPU_H2SYNC — U9751 — VGA_HSYNC_R — R9751 33 5% 1/16W MF-LF 402 — VGA_HSYNC

DVI INTERFACE

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

CRITICAL
F9710 0.5AMP-13.2V SM-LF
PP5V_S0 — F9710 — PP5V_S0_DDC_F — L9710 400-OHM-EMI SM-1 — PP5V_S0_DDC
VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm

CRITICAL
J9700 QH11121-RIG02-4F F-RT-TH-DVI

GND_CHASSIS_DVI_BOT	33	31	
TMDS_DATA_F_N<0>	17	1	TMDS_DATA_F_N<2>
	9		TMDS_DATA_F_N<1>
TMDS_DATA_F_P<0>	18	2	TMDS_DATA_F_P<2>
	10		TMDS_DATA_F_P<1>
	19	3	
TMDS_DATA_F_N<5>	20	11	TMDS_DATA_F_N<4>
		12	TMDS_DATA_F_N<3>
TMDS_DATA_F_P<5>	21	4	TMDS_DATA_F_P<4>
		13	TMDS_DATA_F_P<3>
	22	6	DVI_DDC_CLK_R
		14	(PP5V_S0_DDC)
TMDS_CLK_F_P	23	7	DVI_DDC_DATA_R
	15		
TMDS_CLK_F_N	24	8	VGA_VSYNC
		16	DVI_HPD_R
VGA_B	C3	C1	VGA_R
	C5B	C5A	
VGA_HSYNC	C4	C2	VGA_G
	34	32	
GND_CHASSIS_DVI_TOP	514-0278		

PLACE NEAR C5A & C5B
R9730 0 5% 1/16W MF-LF 402 — GND_CHASSIS_DVI_BOT — GND
C9710 0.01uF 20% 50V CERM 603
C9714 100pF 5% 50V CERM 402

R9731 0 5% 1/16W MF-LF 402 — GND_CHASSIS_DVI_TOP
PLACE NEAR 3, 11 & 19

Isolation required for DVI power switch

D9710 SOD-123 B0530WXF
PP5V_S0_DDC_PULLUPS (VOLTAGE=5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm)
R9710 4.7K 5% 1/16W MF-LF 402 — PP3V3_D3C
R9712 4.7K 5% 1/16W MF-LF 402 — PP3V3_D3C
C9711 100pF 5% 50V CERM 402 — GND

3V LEVEL SHIFTERS

R9711 100 5% 1/16W MF-LF 402 — DVI_DDC_CLK — Q9711 2N7002DW-X-F SOT-363 — R9720 10K 5% 1/16W MF-LF 402 — GPU_DDC_A_CLK
R9713 100 5% 1/16W MF-LF 402 — DVI_DDC_DATA — Q9711 2N7002DW-X-F SOT-363 — R9721 10K 5% 1/16W MF-LF 402 — GPU_DDC_A_DATA
C9713 100pF 5% 50V CERM 402
R9714 100 5% 1/16W MF-LF 402 — DVI_HPD — Q9714 2N7002DW-X-F SOT-363 — R9722 270K 5% 1/16W MF-LF 402 — GPU_HPD_R
GPU_SIGNAL_ENABLE — Q9714 2N7002DW-X-F SOT-363 — GPU_HPD_BILAT
PP5V_S0 — R9723 270K 5% 1/16W MF-LF 402 — Q9715 2N7002DW-X-F SOT-363 — SB_DVI_HPD
MAKE_BASE=TRUE
R9715 20K 5% 1/16W MF-LF 402 — GND_CHASSIS_DVI_BOT
R9724 0 5% 1/16W MF-LF 402 — GPU_HPD_R — GPU_HPD

ANALOG FILTERING

PLACE CLOSE TO CONNECTOR

CRITICAL
FL9740 LCFILTER SM-220MHZ-LF
GPU_B2 (DAC2 Comp) — R9740 75 1% 1/16W MF-LF 402 — VGA_B — C9740 3.3pF 0.25% 50V CERM 402

CRITICAL
FL9741 LCFILTER SM-220MHZ-LF
GPU_G2 (DAC2 Y) — R9741 75 1% 1/16W MF-LF 402 — VGA_G — C9741 3.3pF 0.25% 50V CERM 402

CRITICAL
FL9742 LCFILTER SM-220MHZ-LF
GPU_R2 (DAC2 C) — R9742 75 1% 1/16W MF-LF 402 — VGA_R — C9742 3.3pF 0.25% 50V CERM 402

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	
	TMDS	TMDS	TMDS_CLK_R_P
	TMDS	TMDS	TMDS_CLK_R_N
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..0>
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..0>

External Display Connector

SYNC_MASTER=M57_MLB_MG — SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

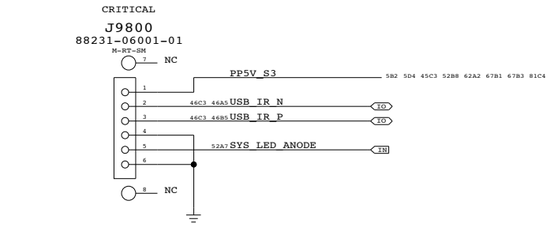
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

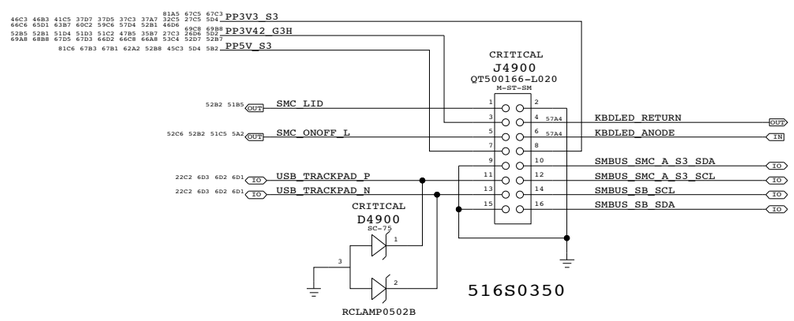
SCALE: NONE — SHT 80 OF 87

IR & Sleep LED Connector



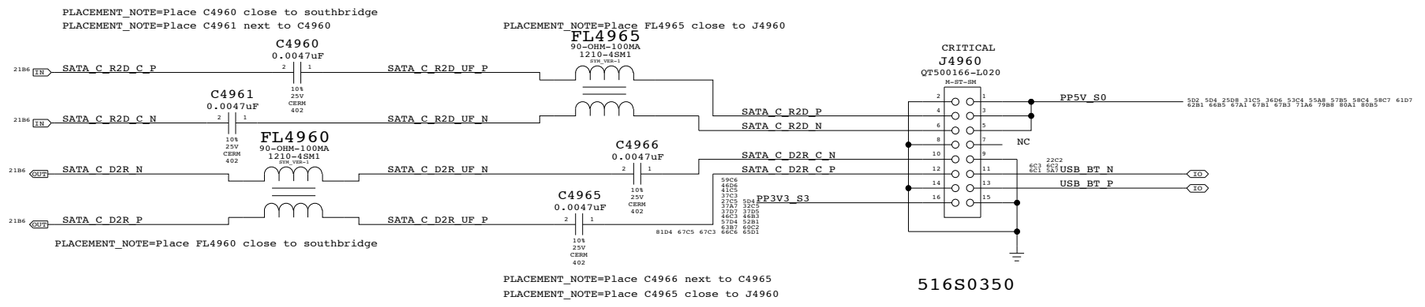
518S0474

Top-Case Connector



516S0350

Bluetooth (M13P) & SATA HDD Flex Connector



516S0350

M57 SPECIFIC CONNECTORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	81	87

LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.

LVDS_L_DATA_P<0>
LVDS_L_DATA_N<0>
LVDS_L_CLK_N
LVDS_L_CLK_P
=LVDS_PD_L_DATA_P<2>
=LVDS_PD_L_DATA_N<2>
=LVDS_PD_L_CLK_P
=LVDS_PD_L_CLK_N
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
=LVDS_PD_U_DATA_P<1>
=LVDS_PD_U_DATA_N<1>
LVDS_U_CLK_N
LVDS_U_CLK_P
=LVDS_PD_U_CLK_P
=LVDS_PD_U_CLK_N

All: LVDS_PD RP9900 / RP9901 / RP9902 / RP9903, 8.2K, 5% 1/16W 8M-LF

PGOOD Monitor for GPU Rails

PP3V3_D3C
PP2V5_D3C
PP1V8_D3C
PP1V2_D3C

R9994 124K 1% 1/16W MF-LF 402
R9992 237K 1% 1/16W MF-LF 402
R9990 365K 1% 1/16W MF-LF 402
R9997 10K 5% 1/16W MF-LF 402

C9990 0.1uF 20% 10V CERM 402
C9991 0.1uF 20% 10V CERM 402

U9990 LTC2903 TSOT-23 (CRITICAL)
V1, V2: D3CPGOOD_2V5_DIV
V3: D3CPGOOD_1V8_DIV
V4: D3CPGOOD_1V2_DIV
RST*: D3CPGOOD_PWROK
GND

R9995 100K 1% 1/16W MF-LF 402 — C9995 0.1UF 20% 10V CERM 402
R9993 100K 1% 1/16W MF-LF 402 — C9993 0.1UF 20% 10V CERM 402
R9991 100K 1% 1/16W MF-LF 402 — C9992 0.1UF 20% 10V CERM 402
R9996 470K 5% 1/16W MF-LF 402

U9991 MC74VHC1G08 SC70
S0PGOOD_PWROK → S0D3CPGOOD_PWROK

LTC2903 guaranteed threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

LVDS Mux Selection Qualification

Enables the GPU LVDS path in the mux with the qualification that the GPU has turned on panel power and that the panel power has risen to (near) 3.3V. This should eliminate need for LVDS pulldowns

PP3V3_S0 → C9985 0.1UF 20% 10V CERM 402
PP2V5_S0 → C9980 0.1UF 20% 10V CERM 402

U9985 MC74VHC1G08 SC70
GPU_DIGON
LVDS_MUX_SEL_GPU
GPU_DIGON_AND_SELECTED

U9980 SN74LVC1G132 SC70-5 (CRITICAL)

R9980 10K 5% 1/16W MF-LF 402 — PP3V3_LCD_SW, PANEL_PWR_ON
R9981 13.3K 1% 1/16W MF-LF 402

Divider set to rise to 1.88V nom/1.74V min when panel power is at 3.3V/3.315V. Schmitt trigger voltage max is 1.70V (@2.625V Vcc). R9981 can also be used as pad for cap, creating an RC filter.

GPU DDC Pass FETs

GPU_SIGNAL_ENABLE
PP3V3_D3C

R9970 15.8K 1% 1/16W MF-LF 402 — Q9970 2N7002DW-X-F SOT-363
GPU_DDC_C_CLK → LVDS_CONN_DDC_CLK (MAKE_BASE=TRUE)
LVDS_CONN_DDC_CLK

R9971 15.8K 1% 1/16W MF-LF 402 — Q9970 2N7002DW-X-F SOT-363
GPU_DDC_C_DATA → LVDS_CONN_DDC_DATA (MAKE_BASE=TRUE)
LVDS_CONN_DDC_DATA

LVDS I/F Mux

PP2V5_S0 → C9950 0.1UF 20% 10V CERM 402

U9950 CBTV4020 BGA-LF (CRITICAL)

NB LVDS I/F:
LVDS_B_DATA_N<2>
LVDS_B_DATA_N<0>
LVDS_B_DATA_P<0>
LVDS_A_CLK_P
LVDS_A_CLK_N
LVDS_A_DATA_N<0>
LVDS_A_DATA_P<0>
LVDS_A_DATA_P<2>
LVDS_A_DATA_N<2>
LVDS_A_DATA_N<1>
LVDS_A_DATA_P<1>
LVDS_B_DATA_P<1>
LVDS_B_DATA_N<1>
LVDS_B_CLK_N
LVDS_B_CLK_P
LVDS_B_DATA_P<2>

GPU LVDS I/F:
LVDS_U_DATA_N<2>
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
LVDS_L_CLK_P
LVDS_L_CLK_N
LVDS_L_DATA_N<0>
LVDS_L_DATA_P<0>
LVDS_L_DATA_P<2>
LVDS_L_DATA_N<2>
LVDS_L_DATA_N<1>
LVDS_L_DATA_P<1>
LVDS_U_DATA_P<1>
LVDS_U_DATA_N<1>
LVDS_U_CLK_N
LVDS_U_CLK_P
LVDS_U_DATA_P<2>

LVDS_U_DATA_CONN_N<2>
LVDS_U_DATA_CONN_N<0>
LVDS_U_DATA_CONN_P<0>
NC
LVDS_L_CLK_CONN_P
LVDS_L_CLK_CONN_N
NC
LVDS_L_DATA_CONN_N<0>
LVDS_L_DATA_CONN_P<0>
LVDS_L_DATA_CONN_P<2>
LVDS_L_DATA_CONN_N<2>
LVDS_L_DATA_CONN_N<1>
LVDS_L_DATA_CONN_P<1>
NC
LVDS_U_DATA_CONN_P<1>
LVDS_U_DATA_CONN_N<1>
NC
LVDS_U_CLK_CONN_N
LVDS_U_CLK_CONN_P
LVDS_U_DATA_CONN_P<2>

SEL: LVDS_MUX_SEL_GPU_L
NOTE: SEL = LOW selects port B

Panel/Backlight Control Mux

PP3V3_S0 → C9960 0.1UF 20% 10V CERM 402

U9960 74CBTLV3257 QFN (CRITICAL)
VCC, GND, THRML PAD

LVDS_VDDEN
GPU_DIGON
LVDS_BKLTEN
GPU_BLON
LVDS_BKLTCTL
GPU_VARY_BL
S0PGOOD_PWROK
S0D3CPGOOD_PWROK
LVDS_MUX_SEL_GPU_MUXED
NOTE: S = HIGH selects xB2

LVDS_PANEL_EN
INVERTER_BKLTON
INVERTER_PWM_UNBUF
PGOOD_MUXED_S0_OR_S0D3C

R9961 100K 5% 1/16W MF-LF 402
R9960 10K 5% 1/16W MF-LF 402

PP3V3_S0 → C9961 0.1UF 20% 10V CERM 402

U9961 MC74VHC1G08 SC70
PLT_RST_L
LVDS_MUX_SEL_GPU
NO STUFF R9962 0 5% 1/16W MF-LF 402

LVDS_MUX_SEL_GPU — LVDS_MUX_SEL_GPU (MAKE_BASE=TRUE) — LVDS_MUX_SEL_GPU

NOTE: SB_GPIO23 has internal 20K PU to default selection to GPU

LVDS Interface Pull-downs

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 82 OF 87	

Revision History

Revision History

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	83	87

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	?
USB2_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	84	87

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	?
FB_CLK	*	=2.5:1_SPACING	?
FB_DATA	*	=2.5:1_SPACING	?

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	=3:1_SPACING	?
TMDS	*	=3:1_SPACING	?
VGA	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS_PAIR2PAIR	*	25 MIL	?
TMDS_PAIR2PAIR	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET	*	=3:1_SPACING	?
FW	*	=3:1_SPACING	?

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

More System Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	85	87

M9 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2,ISL11	0.1 MM	?
1.8:1_SPACING	ISL2,ISL11	0.1 MM	?
2:1_SPACING	ISL2,ISL11	0.1 MM	?
2.5:1_SPACING	ISL2,ISL11	0.1 MM	?
3:1_SPACING	ISL2,ISL11	0.1 MM	?
4:1_SPACING	ISL2,ISL11	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2,ISL11	0.1 MM	?
CLK_PCIE	ISL2,ISL11	0.1 MM	?
CLK_MED	ISL2,ISL11	0.1 MM	?
CLK_SLOW	ISL2,ISL11	0.1 MM	?
CPU_COMP	ISL2,ISL11	0.1 MM	?
CPU_GTLREF	ISL2,ISL11	0.1 MM	?
CPU_VCCSENSE	ISL2,ISL11	0.1 MM	?
DMI	ISL2,ISL11	0.1 MM	?
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
MEM_2OTHER	ISL2,ISL11	0.1 MM	?
PCIE	ISL2,ISL11	0.1 MM	?
SATA	ISL2,ISL11	0.1 MM	?
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
VGA	ISL2,ISL11	0.1 MM	?

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	? OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_5S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M9 Spacing & Physical Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 86 OF 87	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BNR_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DPWR_L	5A4 7B3 12B4
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HIT_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HITM_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5A7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_CPURST_L	5A4 7D6 11B5 12C4
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5B7 7B3 7B4 7C3 7C4 12B6 12C6 12D6
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5B7 7C8 7D8 12C4 12D4
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5A7 7D8 12A4 12B4
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5B7 7C8 7D8 12C4
	CPU_55S		FSB_IERR_L	7D6
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	5B4 7B3 21C4
	CPU_55S		CPU_INTR	7C8 21C4
	CPU_55S		CPU_NMI	7C8 21C4
	CPU_55S		CPU_A20M_L	7C8 21C4
	CPU_55S		CPU_DPSLP_L	5B4 7B3 21C4
	CPU_55S		CPU_IGNNE_L	7C8 21C4
	CPU_55S		CPU_INIT_L	7D6 21C4
	CPU_55S		CPU_SMI_L	7C8 21C4
	CPU_55S		CPU_STPCLK_L	5C4 7C8 21C4
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	5B4 14B7 23C3 61C8
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	5C4 61C7
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7B4
	CPU_55S	CPU_COMP	CPU_COMP<3>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7B3
	CPU_55S	CPU_COMP	CPU_COMP<1>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7B3
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7C6 11B3
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11B3 33C4 34D3 34D5
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11B3 33C4 34D3 34D5
	CPU_55S	CPU_ITP	ITPRESET_L	11B3
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 87B6
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 87B6
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8B6 61B1
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8B6 61A1
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	61A3
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	61A3

MEM_CLK	MEM_76D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21C6
AUDIO_55S	AUDIO	ACZ_BITCLK	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_SYNC	21C6
AUDIO_55S	AUDIO	ACZ_SYNC	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_RST_L	21C6
AUDIO_55S	AUDIO	ACZ_RST_L	5C1 21C7 48B3
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21C6
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5C1 21C7 48B3

TMDS	TMDS	TMDS_CLK_P	78C3 79C7 80B8
TMDS	TMDS	TMDS_CLK_N	78C3 79C7 80C8
TMDS	TMDS	TMDS_DATA_P<5..3>	78C3 79C7 80A8 80B8
TMDS	TMDS	TMDS_DATA_N<5..3>	78C3 79C7 80A8 80B8
TMDS	TMDS	TMDS_DATA_P<2..0>	78C3 79C7 80C8 80D8
TMDS	TMDS	TMDS_DATA_N<2..0>	78C3 79C7 80C8 80D8
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	80A5 80C6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	80A6 80B3 80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	80A6 80B3 80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	80B3 80B5 80C6 80D1 80D6
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	80B3 80B5 80C6 80D1 80D6

M57 NET PROPERTIES

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	87	87