1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,MBP15

10/24/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
B		541444	PRODUCTION RELEASED	10/25/07	

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7492	1	SCHEM,MLB,MBP15	SCH	CRITICAL	
820-2101	1	PCBF,MLB,MBP15	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Wed Oct 24 16:56:10 2007

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

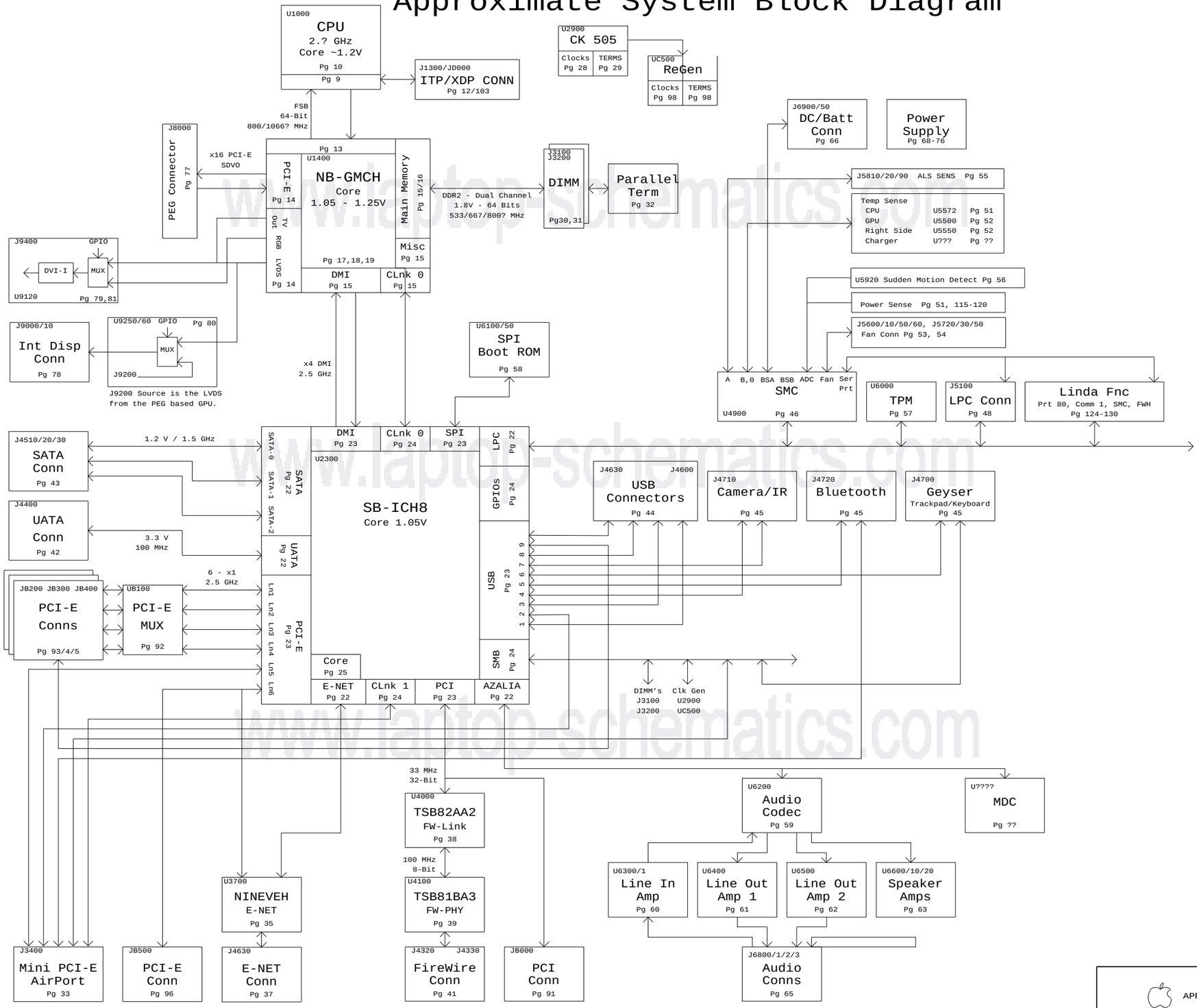
APPLE INC.

TITLE
SCHEM,MLB,MBP15

DRAWING NUMBER 051-7492 REV. B

SHT 1 OF 109

Approximate System Block Diagram



System Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 2 OF 109	

Power Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE	SHT	OF
NONE	3	109

Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	4	109

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9166	PCBA,G0,2.2GHZ,128SAM-VRAM,MBP15	M75_COMMON,EEE_ZF2,CPU_2_2GHZ,FB_128_SAMSUNG
630-9172	PCBA,G0,2.4GHZ,256SAM-VRAM,MBP15	M75_COMMON,EEE_ZF5,CPU_2_4GHZ,FB_256_SAMSUNG
630-9167	PCBA,G0,2.2GHZ,128HY-VRAM,MBP15	M75_COMMON,EEE_ZF3,CPU_2_2GHZ,FB_128_HYNIX
630-9171	PCBA,G0,2.4GHZ,256HY-VRAM,MBP15	M75_COMMON,EEE_ZF4,CPU_2_4GHZ,FB_256_HYNIX
630-9175	PCBA,G0,2.6GHZ,256SAM-VRAM,MBP15	M75_COMMON,EEE_ZF8,CPU_2_6GHZ,FB_256_SAMSUNG
630-9176	PCBA,G0,2.6GHZ,256HY-VRAM,MBP15	M75_COMMON,EEE_ZF9,CPU_2_6GHZ,FB_256_HYNIX

M75 BOM Groups

BOM GROUP	BOM OPTIONS
M75_COMMON	ALTERNATE,COMMON,M75_COMMON1,M75_COMMON2,M75_DEBUG,M75_PROGPARTS
M75_COMMON1	EXTGPU_RST_HW,ISL9504B,LVDS_SEL_RESUME,ONEWIRE_PU
M75_COMMON2	P1V8S3_1V825,SLG2AP101,SMS_MOT_DIS,YUKON_ULTRA,VGA_TERM_CONN
M75_DEBUG	SMC_DEBUG_NO,XDP,LPCPLUS
M75_PROGPARTS	BOOTROM_PROG,SMC_PROG

BOM GROUP	BOM OPTIONS
FB_128_SAMSUNG	VRAM_128,VRAM_SAMSUNG,VRAM_128_SAMSUNG
FB_128_HYNIX	VRAM_128,VRAM_HYNIX,VRAM_128_HYNIX
FB_256_SAMSUNG	VRAM_256,VRAM_SAMSUNG,VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM_256,VRAM_HYNIX,VRAM_256_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZF2]	CRITICAL	EEE_ZF2
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZF5]	CRITICAL	EEE_ZF5
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZF3]	CRITICAL	EEE_ZF3
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZF4]	CRITICAL	EEE_ZF4
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZF8]	CRITICAL	EEE_ZF8
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZF9]	CRITICAL	EEE_ZF9

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3502	1	IC,MDC,SR,G0,PRQ,2.2G,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_2GHZ
337S3503	1	IC,MDC,SR,G0,PRQ,2.4G,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3527	1	IC,MDC,SR,G0,PRQ,2.6G,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_6GHZ
338S0388	1	IC,GPU,NV G84M,BGA	U8000	CRITICAL	
338S0432	1	IC,NB,CRESTLINE,GM,C0,PRQ,965PM	U1400	CRITICAL	
338S0434	1	IC,SB,ICH8M,B1,PRQ,BGA	U2300	CRITICAL	
353S1461	1	IC,ISL9504,SYNC REG CTRL,2PHAS,QFN48,LF	U7100	CRITICAL	ISL9504A
353S1651	1	IC,ISL9504B,2PH IMVP6 REG,PMON,QFN48	U7100	CRITICAL	ISL9504B
359S0127	1	IC,68 PIN,CK505,LOW POWER CLOCK GENER	U2900	CRITICAL	SLG8LP537
359S0130	1	IC,SLG2AP101,LW PWR CLCK GEN,CK505,QFN68	U2900	CRITICAL	SLG2AP101
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2259	1	IC,SMC,V1.16F10,M75A	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2243	1	IC,EFI ROM,DEVELOPMENT,M75A/M76A	U6100	CRITICAL	BOOTROM_PROG

333S0404	4	IC,SGRAM,GDDR3,8Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_128_SAMSUNG
333S0409	4	IC,SGRAM,GDDR3,8Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_128_HYNIX
333S0382	4	IC,SGRAM,GDDR3,16Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0401	4	IC,SGRAM,GDDR3,16Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	E&E alt to TDK/BI-Tech magnetics
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE NONE SHT 5 OF 109

PROTO

See Perforce change notes for updates before Proto Release
12/22/06 -- Released for Proto (Schem Rev 08, PCB Rev 01)

EVT

8.1.0:
01/05/07 -- Clock Termination: Removed NO STUFF property from R3067
01/05/07 -- GPU FB: Corrected FB CLK termination (added cap and removed connection to VDDQ)
8.2.0:
01/08/07 -- GPU FB: Added VREF support for unterminated memory mode (added FETs and pulldown Rs)
9.0.0:
01/09/07 -- Temp Sensors: NO STUFFed C5520 (circuit should have only 1 cap)
01/12/07 -- Power Aliases: Moved Ethernet to PP3V3_S3 from S5 (layout improvements)
01/12/07 -- Power Supplies: Minor power supply feedback connection changes from M76
9.1.0:
01/17/07 -- Power Aliases: Moved LCD panel FET to PP3V3_S5 from S0
01/17/07 -- SMBus: Changed R5260 & R5261 from 4.7K to 3.3K
01/17/07 -- Sync with T9 noME (6.1.4) to pull in WOL_EN and Wake-on-Wireless support
01/17/07 -- Power FETs: Corrected BOM values for 5V/3.3V S3/S0 FETs
01/17/07 -- Power Sequencing: Added RC delay on PP1V8_S3 switcher enable
01/17/07 -- Testpoints: Removed FUNC_TEST from NB_RESET_L and FSB_DPWR_L per PCB request
01/17/07 -- BOM: Consolidated 3 caps on page 59 from 132S0120 to 132S0131
01/17/07 -- BOM: Added Hynix BOM configurations
9.2.0:
01/17/07 -- Power Aliases: Deleted alias that accidentally eliminated filtering on PP1V5_S0_SB_VCC1_5_B
01/18/07 -- Clock Termination: Changed series termination on all single ended clocks to 33 ohms
01/18/07 -- IMVP: Updated BOMOPTIONs and values for ISL9504B
01/18/07 -- Testpoints: Added NO_TEST property to LVDS_L_DATA_N<1>, _N<2>, _P<2> due to lack of layout space for TP
01/18/07 -- ODD Conn: Reconnected ODD power FET gate control circuitry to properly implement soft start (added one cap)
9.3.0:
01/19/07 -- SB Decoupling: Removed filtering for PP1V5_S0_SB_VCCGLANPLL to enable PP1V5_S0 corrections at SB
01/19/07 -- Ethernet Conn: Changed resistor short reference designators from R392x to RX392x
01/19/07 -- Clock Termination: Changed R3050 and R3055 to bypass discrete muxes for pending change to SLG2AP101
01/19/07 -- Power Sequencing: Added C7859 to create RC delay for 1.5 and 1.05V S0 rails
01/19/07 -- Power Sequencing: Changed power rail for U7850 to PP3V3_S5 to eliminate a leakage path
9.4.0:
01/19/07 -- GPU GPIOs: Added 2 TPs on GPIOs to make G-state externally visible
01/19/07 -- SB GPIOs: Changed SB_GPIO42 to WOW_EN and changed pullup to pulldown (T9_noME change 40787)
9.5.0:
01/22/07 -- LIO Conn: Removed unnecessary aliases as T9 reference design now matches M75 (T9_noME change 40998)
01/22/07 -- Clocks: Changed U2900 to SLG2AP101 as primary clock chip (T9_noME change 40975)
01/22/07 -- Clock Termination: Added R3051 for Silego 537/101 compatibility
01/22/07 -- BOM: Added BOMOPTIONs for SLG2AP101 (primary) and SLG8LP537 (backup)
01/22/07 -- BOM: Selected P1V8S3_1V825 BOMOPTION to lift voltage at FB memories
10.0.0:
01/23/07 -- BOM: Changed C3860/61 to 22pF from 27 pF based on -R characterization (T9_noME change 41248)
01/23/07 -- BOM: Changed FB memories to new Samsung and Hynix APNs (also added new BOMOPTIONs to GPU straps)
01/23/07 -- Released for EVT (Schem Rev 10, PCB Rev 02)

EVT_SE

10.1.0:
01/24/07 -- PATA Conn: Added pass FET Q4430 to allow PCIREQ3 (ODD reset GPIO) to pullup to S0
01/24/07 -- PATA Conn: Changed =PP5V_S0_ODDPWREN to =PP3V3_S0_ODDPWREN for minor power savings
01/24/07 -- Power Aliases: Updated PP3V3_S0 aliases to support above changes
10.2.0:
01/25/07 -- PATA Conn: Replaced PCIREQ pass FET with OD buffer to correct a corner case during PLTRST
01/25/07 -- Power Aliases: Updated PP5V_S0 aliases to support above changes
11.0.0:
01/25/07 -- BOM: Updated gain of PP1V25_ENET current sense amplifier to 165 (R5432 to 165K)
01/25/07 -- BOM: Updated all Intel APNs to use QS parts
01/25/07 -- Released for EVT (Schem Rev 11, PCB Rev 03)
12.0.0:
02/19/07 -- GPU Reset: Changed C2885 to 0.047uF to reduce reset delay on powerup
02/19/07 -- GPU PGOOD: Changed C9595 to 330pF to reduce PGOOD delay on powerup
02/19/07 -- Power Sequencing: NO STUFFed U7885 to remove GPU PGOOD from PWROK chain
02/19/07 -- Power Sequencing Rework: Short pins 2 and 4 of U7885 to complete PWROK chain
02/19/07 -- Released post-EVT to document what was built (Schem Rev 12)

DVT

12.1.0:
02/20/07 -- GPU FB: Changed cal resistors per Nvidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm)
02/20/07 -- GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -> 1.02K, R8432/82, R8532/82 -> 2.21K)
02/21/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435)
02/21/07 -- Power Sequencing: Removed U7885/C7885 to take GFX_PGOOD out of PWR_OK chain (rdar://4974927)
02/26/07 -- GPU Vcore: NO STUFFed all PWRCTL related components (feature not to be supported)
02/26/07 -- GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V (rdar://5021453)
02/26/07 -- SB GPIOs: Sync'd page25.csa to T9_MLB to get pullup updates
02/26/07 -- Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors - rdar://5025773)
12.2.0:
02/27/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on) (rdar://4993378)
02/28/07 -- Power Aliases: Moving PP1V8_GPU FET source to PP1V8_S3 rather than PP1V8_S3_ISNS to improve power delivery to GPU (rdar://5021462)
12.3.0:
02/28/07 -- Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating)
02/28/07 -- NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109)
02/28/07 -- Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109)
03/01/07 -- Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF)
03/01/07 -- NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines
12.4.0:
03/01/07 -- LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882)
03/01/07 -- NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272)
12.5.0:
03/02/07 -- Power/Signal Aliases: Added XW0900 to PP5V_S5 to enable layout improvements
12.6.0:
03/06/07 -- Power FETs: Changed Q7080 to RJK0301 which provides much lower Rds(on)
03/06/07 -- FireWire Ports: Changed D4260 to PDS340 for lower height
12.7.0:
03/06/07 -- FireWire Ports: Changed D4260 to PDS540 for higher current capacity
03/06/07 -- Ethernet Connector: Removed RX shorts on Ethernet MDI lines per EMC request
03/06/07 -- SB GPIOs: Changed R2514 from pulldown to pullup to correct auto power-on issue (Linda card detect GPIO)
03/06/07 -- DDR2 Regulator: Changed FB resistors to 0.1% to raise guaranteed lowest output voltage

DVT (cont'd)

12.8.0:
03/08/07 -- Thermal Sensors: Added R5515/R5516 in case low pass filter is needed for EMC1033
13.0.0:
03/12/07 -- Power Control: Corrected alias connections for 5V/3V3 S5 enable signals
13.1.0:
03/13/07 -- BOM Options: Removed HDCP BOM option from stuffing list (feature removed)
03/14/07 -- Constraints: Constrained WWAN_SIM signals to 50 ohms
03/14/07 -- Thermal Sensors/Aliases: Changed mounting pads of Th2H sensor connector to left clutch chassis gnd
13.2.0:
03/16/07 -- Thermal Sensors: Replaced EMC1033 with second EMC1043 for improved noise filtering
03/16/07 -- NB GFX: LVDS_VREFL/VREFH changed to single pin nets to prevent LVDS glitches per Intel
03/16/07 -- Yukon Power Control: Crystal caps changed to 18pF (rdar://4946795 and rdar://4945362)
13.3.0:
03/16/07 -- Thermal Sensors: Moved remote sensor U5500 to SMC SMBus "A" and S3 power rail to clear I2C addr clash
13.4.0:
03/19/07 -- Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail
03/19/07 -- Power Control: Added U7858 to level shift PM_G2_EN from 3.42V to 5V
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, removed VBST 0-ohm series R (rdar://5070179)
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, increased cap size to 0603/0805 on VBST caps (rdar://5070179)
13.5.0:
03/19/07 -- Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3, EN5) together as part of PM_G2_EN
14.0.0:
03/20/07 -- GPU Vcore: Updated setpoints for GPU Vcore based upon Nvidia Vmin (i.e. 1.05V,1.05V,1.05V,1.125V)
03/20/07 -- FB: Changed FB VREF caps to 2x0.0047uF as required in Nvidia PUN 02736-001-v07 (which requests 1x0.01uF)
15.0.0:
03/30/07 -- SIL: Changed R5031 to 2.21K and R5032 to 9.53K to raise SIL current approx 15% (lightpipe dimmed by 20%)
03/30/07 -- Power Supply: Changed 1.05V power supply current limit to 10A from 8A (R7455 to 5.62k -- rdar://5095642)
04/03/07 -- Power Supply: Changed numerous 10K Rs to 100K for Energy Star compliance (rdar://5102118)
04/03/07 -- GPU FB: Changed FB clock termination to 242 ohms (2x121) per Nvidia PUN
04/03/07 -- CPU Vcore: Changed R7117,C7134 and R7115,R7130 for calibration improvements (rdar://5085959)
04/03/07 -- Released for DVT (BOM update)
16.0.0:
04/17/07 -- Power Sequencing: NO STUFFED U7858 and stuffed R7860 to allow SMC to drive S5 enable pins directly
04/17/07 -- Released for DVT (As-Built)

PVT

16.1.0:
04/18/07 -- GPU Misc: Added R8735-37 to implement PCI DEVID 0x407 in hardware
16.2.0:
04/18/07 -- Power FETs: Changed Q7095 to FDM6296 and pulled up to PBUS for better PP1V25_S0 FET Rds(on)
04/18/07 -- Modules: Updated Intel chipset to PRQ parts
16.3.0:
04/20/07 -- Power FETs: Changed R7097 to 220K to maintain EnergyStar compliance with FET gate pulled to PBUS
04/20/07 -- Power FETs: Changed C7095/C7083 to 16V for proper rating of parts tied to PBUS
04/20/07 -- CPU VCore: Changed C7196 to 16V to eliminate a BOM item
17.0.0:
04/20/07 -- No changes. Weekly BOM release.
A.0.0:
04/24/07 -- SB Decoupling: Changed L2700 from 155S0152 to 155S0333 for AVL updates
04/24/07 -- SMC Support: Changed R5031 to 2.37K, R5032 to 9.09K to meet SIL brightness targets
04/24/07 -- Released for PVT
B.0.0:
05/08/07 -- SB Decoupling: Changed C2703 to 158S0578 per Intel recommendations (rdar://5185100)
05/08/07 -- GPU Straps: Stuffed R8728 to put GPU PEG I/F into mobile mode (rdar://5188253)

M75A PROTO

See Perforce change notes for updates before Proto Release
08/16/07 -- Released for Proto (Branched from M75, updated CPU part numbers)

B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 6 OF 109	

Functional Test Points

Fan Connectors

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	8 52
TRUE	FAN_LT_PWM	52
TRUE	FAN_LT_TACH	52
TRUE	FAN_RT_PWM	52
TRUE	FAN_RT_TACH	52

LPC+ Debug Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	8 47
TRUE	=PP5V_S0_LPCPLUS	8 47
TRUE	LPC_AD<0>	23 45 47
TRUE	LPC_AD<1>	23 45 47
TRUE	LPC_FRAME_L	23 45 47
TRUE	PM_CLKRUN_L	25 45 47
TRUE	BOOT_LPC_SPI_L	24 47
TRUE	SMC_TMS	45 46 47
TRUE	DEBUG_RESET_L	28 47
TRUE	SMC_TRST_L	45 47
TRUE	SMC_TDO	45 46 47
TRUE	SMC_MD1	45 47
TRUE	SMC_TX_L	43 45 46 47
TRUE	FWH_INIT_L	47
TRUE	PCI_CLK33M_LPCPLUS	30 47 84
TRUE	LPC_AD<2>	23 45 47
TRUE	LPC_AD<3>	23 45 47
TRUE	INT_SERIRQ	25 45 47
TRUE	PM_SUS_STAT_L	25 45 46 47
TRUE	SMC_TDI	45 46 47
TRUE	SMC_TCK	45 46 47
TRUE	SMC_RESET_L	45 46 47
TRUE	SMC_NMI	45 47
TRUE	SMC_RX_L	43 45 46 47
TRUE	LINDACARD_GPIO	25 47

Left ALS Connector

FUNC_TEST

TRUE	=PP3V3_S3_LTALS	8 78
TRUE	ALS_GAIN	45 53 78
TRUE	LTALS_OUT	53 78
TRUE	GND	

Thermal Diode Connectors

FUNC_TEST

TEST	TRUE	HSTHMSNS_D_P	51 87
TEST	TRUE	HSTHMSNS_D_N	51
	TRUE	RSFSTHMSNS_D_P	51 87
	TRUE	RSFSTHMSNS_D_N	51
		CPUTHMSNS_D2_P	51 87
		CPUTHMSNS_D2_N	51

CPUTHMSNS can not be supported due to layout constraints

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	45 46 56
TRUE	=SMBUS_BATT_SCL	48 56
TRUE	=SMBUS_BATT_SDA	48 56
TRUE	GND_BATT	56

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUS_G3H_LIO_CONN	8 56
TRUE	GND	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

RTC Battery Connector

FUNC_TEST

TRUE	PPVBATT_G3_RTC	28
TRUE	GND	

Current Sense Calibration

FUNC_TEST

TRUE	ISENSE_CAL_EN	45 49
TRUE	=PP5V_S0_ISENSECAL	8 49
TRUE	=PPVCORE_S0_NBGFX_REG	8 59
TRUE	=PPVCORE_S0_CPU_REG	8 49 58
TRUE	=PPVCORE_GPU_REG	8 49 74
TRUE	GND	

2 TPs per

6 TPs, 2 with each of above TP pairs

Left Clutch Barrel Connector

FUNC_TEST

TRUE	=PP5V_S3_CAMERA	8 44
TRUE	USB_CAMERA_N	24 44 82
TRUE	USB_CAMERA_P	24 44 82
TRUE	=PP5V_S3_WWAN	8 44
TRUE	USB_WWAN_N	44
TRUE	USB_WWAN_P	44

Other Func Test Points

FUNC_TEST

TRUE	PM_SYSRST_L	25 28 45
TRUE	SMC_ONOFF_L	45 46 78

System Validation TPs

FUNC_TEST

TRUE	CPU_PWRGD	10 13 23 79
TRUE	CPU_DPSLP_L	7 10 23 79
TRUE	PM_DPRSLPVR	16 25 58 79
TRUE	CPU_DPSLP_L	7 10 23 79
TRUE	PM_LAN_ENABLE	25 45
TRUE	PCI_RST_L	24 28
TRUE	PM_RSMRST_L	25 45
TRUE	PM_SB_PWROK	9 25 28
TRUE	SB_RTC_RST_L	23 28
TRUE	PM_STPCPU_L	25 29 30
TRUE	PM_STPPCI_L	25 29 30
TRUE	VR_PWRGD_CLKEN	25 28
TRUE	VR_PWRGOOD_DELAY	9 16 28 58
TRUE	FSB_CPURST_L	10 13 14 79
TRUE	FSB_CPUSLP_L	10 14 79
	FSB_DPWR_L	10 14 79
TRUE	NB_SB_SYNC_L	16 25

FUNC_TEST

TRUE	IMVP_VR_ON	45 58
TRUE	IMVP_DPRSLPVR	58 79
TRUE	PM_SLP_S3_L	25 36 40 45 65
TRUE	PM_S4_STATE_L	25 45 65
TRUE	PM_SLP_S5_L	25 45 46
TRUE	PM_ENET_EN	36 65
TRUE	P1V5P1V05S0_PGOOD	65
TRUE	CPU_DPRSTP_L	10 16 23 58 79
TRUE	IMVP6_VID<6..0>	12 58 79
TRUE	PLT_RST_L	24 28 77
	NB_RESET_L	16 28
TRUE	GPU_RESET_L	28 66
TRUE	SMC_LRESET_L	28 45
TRUE	CPU_STPCLK_L	10 23 79
TRUE	FSB_CLK_NB_P	14 30 84
TRUE	FSB_CLK_NB_N	14 30 84
TRUE	NB_CLKREQ_L	16 29
TRUE	NB_CLK100M_PCIE_P	16 30 84
TRUE	NB_CLK100M_PCIE_N	16 30 84
TRUE	NB_CLK96M_DOT_P	84
TRUE	NB_CLK96M_DOT_N	84
TRUE	NB_CLK100M_DPLLSS_P	22 30 84
TRUE	NB_CLK100M_DPLLSS_N	22 30 84
TRUE	CPU_THERMTRIP_R	23

ICT Test Points

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	10 14 79
TRUE	FSB_ADS_L	10 14 79
TRUE	FSB_ADSTB_L<1..0>	10 14 79
TRUE	FSB_BNR_L	10 14 79
TRUE	FSB_BREQ0_L	10 14 79
TRUE	FSB_D_L<63..0>	10 14 79
TRUE	FSB_DBSY_L	10 14 79
TRUE	FSB_DINV_L<3..0>	10 14 79
TRUE	FSB_DRDY_L	10 14 79
TRUE	FSB_DSTB_L_N<3..0>	10 14 79
TRUE	FSB_DSTB_L_P<3..0>	10 14 79
TRUE	FSB_HIT_L	10 14 79
TRUE	FSB_HITM_L	10 14 79
TRUE	FSB_LOCK_L	10 14 79
TRUE	FSB_REQ_L<4..0>	10 14 79

GPU NO_TESTs

NO_TEST

LVDS	TRUE	LVDS_L_DATA_N<1>	73 77 86
LVDS	TRUE	LVDS_L_DATA_N<2>	73 77 86
LVDS	TRUE	LVDS_L_DATA_P<2>	73 77 86

NB NO_TESTs

NO_TEST

	TRUE	NC_NB_NC<1..16>	TP_NB_NC<1..16> 16

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 7 OF 109	

"G3Hot" (Always-Present) Rails

=PPBUS_G3H_LIO_CONN
PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPBUS_S5_FWPWRSW
=PPBUS_S5_P1V8GPUFET
=PPBUS_S5_P1V25S0FET
=PPVIN_S5_CPU_IMVP_VIN
=PPVIN_S5_CPU_IMVP
=PPVIN_S5_P5VP3V3
=PPVIN_S5_P5VS5
=PPVIN_S5_P3V3S5
=PPVIN_ENET_P1V25ENET
=PPVIN_S3_P1V8S3
=PPVIN_S0_P1V5S0
=PPVIN_S0_GFXIMVP6
=PPVIN_S0_P1V05S0
=PPVIN_GPU_GPUVCORE

=PPDCIN_G3H_LIO_CONN
PPDCIN_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PPVIN_G3H_P3V42G3H

=PP3V42_G3H_REG
PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PP3V42_G3H_SB_RTC
=PP3V42_G3H_LIO
=PP3V42_G3H_SMCUSBMUX
=PP3V42_G3H_SMBUS_SMC_BSA
=PP3V42_G3H_LIDSWITCH
=PP3V3_S5_SMC
=PP3V3_S5_LPCPLUS
=PPVIN_S5_SMCVREF
=PP3V42_G3H_PWRCTL

5V Rails

=PP5V_S5_REG
PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S5_SB
=PP5V_S5_P1V8GPUFET
=PP5V_S5_P1V8S0FET
=PP5V_S5_P1V25GPUFET
=PP5V_S5_P1V25S0FETXW
=PP5V_S5_P1V25ENET
=PP5V_S5_P1V05S0
=PP5V_S5_P1V8DDRREG
=PP5V_S5_P1V5S0
=PP5V_S5_PWRCTL
=PP5V_S5_GPUVCORE
=PP5V_S3_RTUSB
=PP5V_S3_P5VS3FET
=PP5V_S0_P5VS0FET

=PP5V_S3_FET
PP5V_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_SYSLED
=PP5V_S3_CAMERA
=PP5V_S3_WWAN
=PP5V_S3_IR
=PP5V_S3_TOPCASE
=PP5V_S0_KBDLED
=PP5V_S0_ISENSECAL

=PP5V_S0_FET
PP5V_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_SB
=PP5V_S0_ODD
=PP5V_S0_LPCPLUS
=PP5V_S0_FAN_LT
=PP5V_S0_FAN_RT
=PP5V_S0_CPU_IMVP
=PP5V_S0_GFXIMVP6
=PP5V_S0_DVI_DDC
=PP5V_S0_SB_HPD
=PP5V_S0_HDD
=PP5V_S0_ODDPWREN
=PP5V_S0_PCIREQFIX

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU

=PPVCORE_S0_NBGFX_REG
PPVCORE_S0_NB_GFX
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_NB_GFX
=PPVCORE_S0_NBGFX_VSEN

3.3V-2.5V Rails

=PP3V3_S5_REG
PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_SB_PM
=PP3V3_S5_SB_CLINK
=PP3V3_S5_SB
=PP3V3_S5_SB_CLINK1
=PP3V3_S5_SB_GPIO
=PP3V3_S5_SB_3V3_VCCSUSHDA
=PP3V3_S5_SB_VCCSUS3_3
=PP3V3_S5_SB_VCCSUS3_3_USB
=PP3V3_S5_S5PWRGD
=PP3V3_S5_SMBUS_SB_ME
=PP3V3_S5_ROM
=PP3V3_S5_P1V5P1V05PG
=PP3V3_S3_P3V3S3FET
=PP3V3_S0_LCD
=PP3V3_S0_P3V3S0FET
=PP3V3_GPU_P3V3GPUFET
=PP3V3_S5_PWRCTL

=PP3V3_S3_FET
PP3V3_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_P3V3ENETFET
=PP3V3_S3_FW
=PP3V3_S3_PCI
=PP3V3_S3_SMBUS_SMC_A_S3
=PP3V3_S3_RTALS
=PP3V3_S3_SMS
=PP3V3_S3_SMBUS_SMC_MGMT
=PP3V3_S3_P1V25ISNS
=PP3V3_S3_P1V8ISNS
=PP3V3_S3_LTALS
=PP3V3_S3_TOPCASE
=PP3V3_S3_REMTHMSNS

=PP3V3_S0_FET
PP3V3_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_NB_VCCHV
=PP3V3_S0_NB_VCCA_PEG_BG
=PP3V3_S0_NB_FOLLOW
=PP3V3_S0_SB_GPIO
=PP3V3_S0_SB_PCI
=PP3V3_S0_SB_VCC3_3_IDE
=PP3V3_S0_SB_VCC3_3_PCI
=PP3V3R1V5_S0_SB_VCCHDA
=PP3V3_S0_SB_VCC3_3_DMI
=PP3V3_S0_SB_VCC3_3_VCCPCORE
=PP3V3_S0_SB_VCCGLAN3_3
=PP3V3_S0_SB_VCC3_3_SATA
=PP3V3_S0_SB
=PP3V3_S0_SB_PM
=PP3V3_S0_RSTBUF
=PP3V3_S0_CK505
=PP3V3_S0_IDE
=PP3V3_S0_SMC
=PP3V3_S0_LPCPLUS
=PP3V3_S0_SMBUS_SB
=PP3V3_S0_SMBUS_SMC_B_S0
=PP3V3_S0_CPUCOREISNS
=PP3V3_S0_NBGFXCOREISNS
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_GPUTHMSNS
=PP3V3_S0_FAN_LT
=PP3V3_S0_FAN_RT
=PP3V3_S0_IMVP
=PP3V3_S0_GFXIMVP6
=PP3V3_S0_NBCOREISNS
=PP3V3_S0_ALLSYSPG
=PP3V3_S0_DDC_LCD
=PP3V3_S0_LVDS_MUX
=PP3V3R5V_GPU_GPUISENS
=PP3V3_S0_XDP
=PP3V3_S0M_CK505
=PP3V3_S0_GPUCLKGATE
=PPSPD_S0M_MEM_A
=PPSPD_S0M_MEM_B
=PP3V3_S0MWOL_SB_CLINK0
=PP3V3_S0MWOL_SB_VCCCL3_3
=PP3V3_S0MWOL_SB_VCCLAN3_3
=PP3V3_S0_PWRCTL

=PP1V25_ENET_ISNS
PP1V25_ENET_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PP1V25_S0_P1V25S0FET
=PP1V25_GPU_P1V25GPUFET

1.8V-0.9V Rails

=PP1V8_S3_REG
PP1V8_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_S3_FW
=PP1V8_S3M_MEM_A
=PP1V8_S3M_MEM_B
=PP1V8_S3_ISNS_R
=PP1V8_GPU_P1V8GPUFET

=PP1V8_S3_ISNS
PP1V8_S3_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_S3M_NB_VCC
=PP1V8_S3M_MEM_NB
=PP1V8_S0_P1V8S0FET

=PP1V8_S0_FET
MAX I = 0.36A
PP1V8_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_S0_NB_LVDS
=PPVIN_S0_NB_DPLL

=PP1V5_S0_REG
MAX I = ?.??A
PP1V5_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU
=PP1V5_S0_NB_TVDAC
=PP1V5_S0_SB
=PP1V5_S0_SB_VCC1_5_A_ARX
=PP1V5_S0_SB_VCC1_5_A_ATX
=PP1V5_S0_SB_VCC1_5_A
=PP1V5_S0_SB_VCCUSBPLL
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
=PP1V5_S0_LIO

=PP1V25_S0_FET
PP1V25_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PP1V25_S0M_NB_PLL
=PP1V25_S0M_NB_VCC
=PP1V25_S0M_NB_VCCA
=PP1V25_S0_NB_VCCDMI
=PP1V25_S0_NB_PLL
=PP1V25_S0_NB_VCC
=PP1V25_S0_SB_DMI

=PP1V05_S0_REG
PP1V05_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0M_NB_VCCAXM
=PP1V05_S0_CPU
=PP1V05_S0_NB_FOLLOW
=PP1V05_S0_NB_PCIE
=PP1V05_S0_SB_CPU_IO
=PP1V05_S0_SMC_LS
=PP1V25R1V05_S0_FSB_NB
=PP1V25R1V05_S0_NB_VTT
=PPVCORE_S0_NBCOREISNS
=PPVCORE_S0_NB_FOLLOW
=PPVCORE_S0_SB

=PPVCORE_S0_NB_R
PPVCORE_S0_NB_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PPVCORE_S0_NB

=PP0V9_S3_VTTR_BUF
PP0V9_S3_MEM_VREF
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V9_S3M_MEM_NBVREFA
=PP0V9_S3M_MEM_NBVREFB
=PP0V9_S3M_MEM_DIMMVREFA
=PP0V9_S3M_MEM_DIMMVREFB

=PP0V9_S0_VTT_LDO
PP0V9_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V9_S0M_MEM_TERM

"ENET" Rails

=PP3V3_ENET_FET
PP3V3_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_PHY
=PP3V3_ENET_AVDDLDO

=PPVOUT_ENET_AVDDLDO
PP1V9_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.9V
MAKE_BASE=TRUE
=PP1V8R2V5_ENET_PHY

=PP1V25_ENET_REG
PP1V25_ENET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PP1V2_ENET_PHY
=PP1V25_ENET_ISNS_R

=YUKON_EC_PP2V5_ENET
Yukon EC will not be supported

"FW" (FireWire) Rails

PPBUS_FW_FWPWRSW_F
MAKE_BASE=TRUE
=PPBU_S0_P3V3FW

=PPBUS_S5_FW_FET
PPVP_FW
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PPVP_FW_SUMNODE
=PPVP_FW_CPS
=PPVP_FW_P3V3FW

PPVP_FW_PORTA_UF
MAKE_BASE=TRUE
=PPVP_FW_PORT0

PPVP_FW_PORTB_UF
MAKE_BASE=TRUE
=PPVP_FW_PORT1

=PP3V3_FW_REG
PP3V3_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_FW_PHY
=PP3V3_FW_LATEVG_ACTIVE
=PP3V3_FW_LATEVG
=PPVIN_FW_P1V95FW

=PP1V95_FW_LDO
PP1V95_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.95V
MAKE_BASE=TRUE
=PP1V95_FW_PHY
=PP1V8_FW_PHYOSC

"GPU" Rails

=PP3V3_GPU_FET
PP3V3_GPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_VDD33
=PP3V3_GPU_MIO
=PP3V3_GPU_DAC
=PP3V3_GPU_DVI
=PP3V3_GPU_LVDS_DDC
=PP3V3_GPU_VGASYNC
=PP3V3_GPU_TMDS
=PP3V3_GPU_VIDEOMUX
=PP2V5_GPU_LTC2900
=PP3V3_GPU_SMBUS_SMC_0_S0
=PP3V3_GPU_PWRCTL
=PP3V3_GPU_VCORELOGIC
=PP3V3_GPU_HDCP

=PP3V3_GPU_TMDS_FET
PP3V3_GPU_TMDS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_TMDSBIAS
=PP3V3_GPU_IFPCD_IOVDD

=PP1V8_GPU_FET
PP1V8_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_GPU_FB_VDD
=PP1V8_GPU_FB_VDDQ
=PP1V8_GPU_FBVDDQ
=PP1V8_GPU_FBIO
=PP1V8_GPU_IFPX

=PP1V25_GPU_FET
PP1V25_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PP1V2_GPU_PEX_IOVDDQ
=PP1V2_GPU_PEX_IOVDD
=PP1V2_GPU_PEX_PLLXVDD
=PP1V2_GPU_PLLVDD
=PP1V2_GPU_H_PLLVDD
=PP1V2_GPU_VID_PLLVDD
=PP1V2_GPU_FBPLLAVDD
=PP1V2_GPU_VCOREPWRCTL

=PPVCORE_GPU_REG
PPVCORE_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
=PPVCORE_GPU

Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE D | DRAWING NUMBER 051-7492 | REV. B

SCALE NONE | SHT 8 OF 109

Thermal Module Holes

Top CPU TM Notch
Add 2 buried vias to GND

ZT0970 5P75R2P7 — Left CPU TM Hole
ZT0975 5P75R2P7 — Right CPU TM Hole
ZT0980 5P75R2P7 — Bottom Left GPU TM Hole
ZT0985 5P75R2P7 — Top GPU Right TM Hole

RAM Door (Torx) Holes

ZT0930 3P7R3P2 — GND_CHASSIS_RAMDOOR_HOLE_0
ZT0935 3P7R3P2 — GND_CHASSIS_RAMDOOR_HOLE_1

Frame Holes

ZT0920 3P2R2P7 — GND_CHASSIS_LVDS_HOLE
ZT0940 3P7R3P2 — GND_CHASSIS_RIGHT_FAN_HOLE

Board Edge Notches (Can't be PTH)

ZT0945 HOLE-VIA-P5RP25 — GND_CHASSIS_RIGHT_FAN_NOTCH
ZT0950 HOLE-VIA-P5RP25 — GND_CHASSIS_DIMM_NOTCH

ZT0955 3P2R2P7 — GND_CHASSIS_LIOFLEX_HOLE
ZT0965 3P2R2P7 — GND_CHASSIS_LINDACARD_HOLE

Tooling Holes (Can't be PTH)

ZT0960 HOLE-VIA-P5RP25 — GND_CHASSIS_BATTCONN_HOLE
ZT0990 HOLE-VIA-P5RP25 — GND_CHASSIS_DVI_HOLE

Chassis GNDs

GND_CHASSIS_DVI_TOP — =GND_CHASSIS_DVI_TOP (76)
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_DVI_BOT — =GND_CHASSIS_DVI_BOT (76)
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

OMIT
R0910 1 2 402 SHORT
NONE
NONE
NONE

GND_CHASSIS_ENET
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.21 mm
VOLTAGE=0V
MAKE_BASE=TRUE
— =GND_CHASSIS_ENET (37)
— =GND_CHASSIS_FW_PORT1 (41)
— =GND_CHASSIS_FW_PORT0U (41)

GND_CHASSIS_RTUSB
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
— =GND_CHASSIS_FW_PORT0L (41)
— =GND_CHASSIS_RTUSB (43)

SH0925 0G-503040 SHLD-SM-LF
1 GND_CHASSIS_LEFTCLUTCH
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
2
3
— =GND_CHASSIS_LEFTCLUTCH (44)
— =GND_CHASSIS_J5590 (51)

PM_SB_PWROK (28 25 7) — =SB_CLINK_MPWROK (25)
MAKE_BASE=TRUE
VR_PWRGOOD_DELAY (58 28 16 7) — =NB_CLINK_MPWROK (16)
MAKE_BASE=TRUE

SMC_SMS_INT (54) — =SMC_SMS_INT (45)
MAKE_BASE=TRUE

PEG_CLK100M_GPU_P (66 30) — PEG_CLK100M_P (84)
MAKE_BASE=TRUE
PEG_CLK100M_GPU_N (66 30) — PEG_CLK100M_N (84)
MAKE_BASE=TRUE

PM_ALL_NBGFX_PGOOD (77) — GFXIMVP6_PGOOD (59)
MAKE_BASE=TRUE
GFX_VR_EN (59) — =GFX_VR_EN (16)
MAKE_BASE=TRUE
GFXIMVP6_VID<4..0> (59) — GFX_VID<4..0> (16)
MAKE_BASE=TRUE

TP_MEM_A_A<15> — MEM_A_A<15> (31)
MAKE_BASE=TRUE
TP_MEM_B_A<15> — MEM_B_A<15> (32)
MAKE_BASE=TRUE

TP_USB_EXTCP — USB_EXTC_P (24 82)
MAKE_BASE=TRUE
TP_USB_EXTCN — USB_EXTC_N (24 82)
MAKE_BASE=TRUE

XW0900 SM
(8) =PP5V_S5_P1V25S0FETXW — 1 2 — PP5V_S5_P1V25S0FET — =PP5V_S5_P1V25S0FET (57)
MIN_LINE_WIDTH=0.1 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=5V
MAKE_BASE=TRUE
NO_TEST=TRUE

Digital Ground

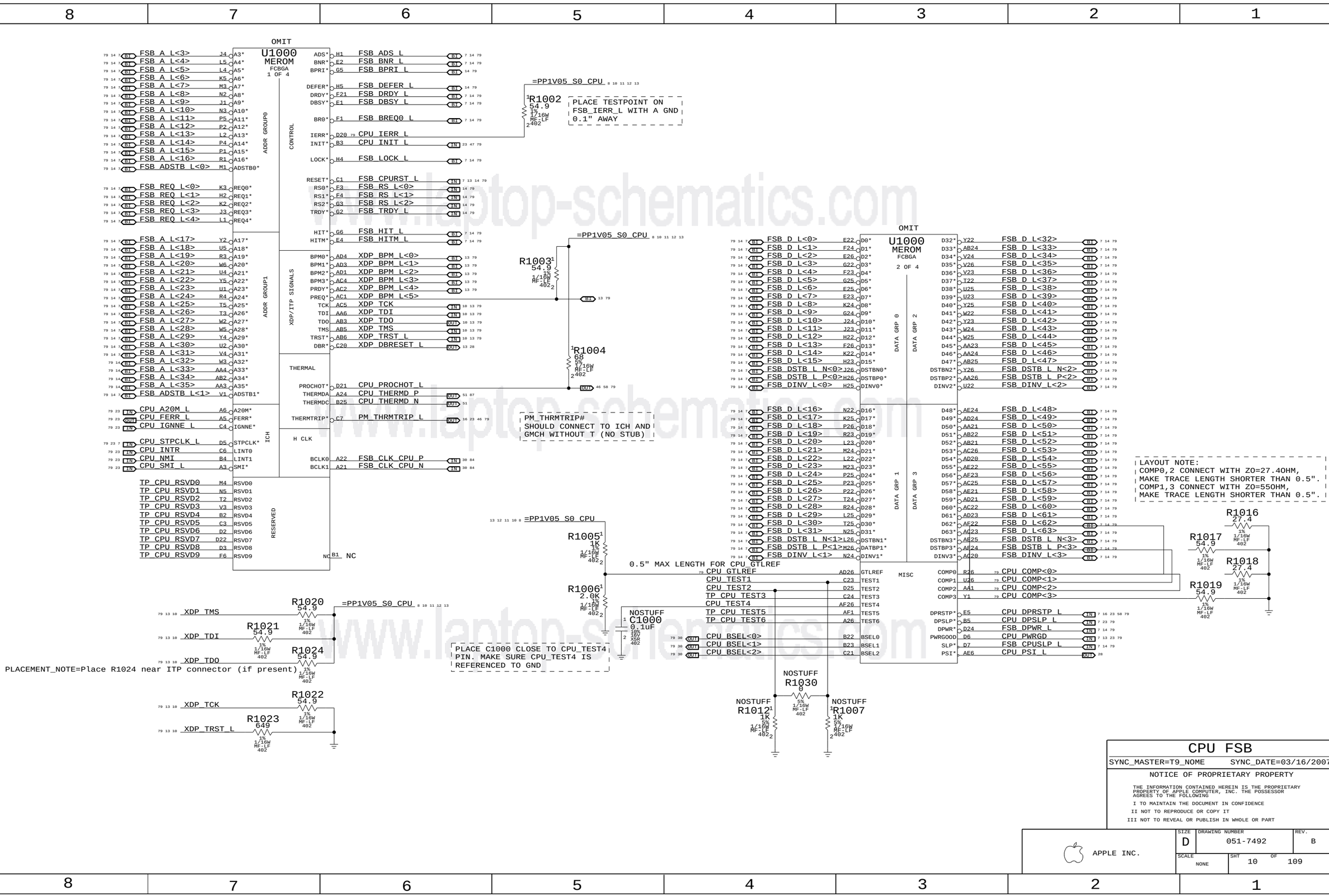
GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

Signal Aliases

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 9 OF 109	



CPU FSB

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 10 OF 109	

(CPU CORE POWER)
=PPVCORE_S0_CPU 8 11 12 49

Standard Voltage:	Low Voltage:	Ultra Low Voltage:
44.0 A (Design Target)	23.0 A (Design Target)	17.0 A (Design Target)
41.0 A (HFM)	21.0 A (HFM)	TBD A (HFM)
30.4 A (LFM)	18.7 A (LFM)	TBD A (LFM)
25.5 A (SuperLFM)	TBD A (SuperLFM)	
27.4 A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant LFM)
27.4 A (Sleep HFM)	TBD A (Sleep HFM)	TBD A (Sleep HFM)
16.8 A (Sleep SuperLFM)	TBD A (Sleep SuperLFM)	TBD A (Sleep LFM)
25.0 A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)	TBD A (Deep Sleep SuperLFM)	TBD A (Deep Sleep LFM)
11.5 A (Deeper Sleep)	TBD A (Deeper Sleep)	TBD A (Deeper Sleep)
9.4 A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)

OMIT
U1000
MEROM
FCBGA
3 OF 4

VCC: A7 A9 A10 A12 A13 A15 A17 A18 A20 B7 B9 B10 B12 B14 B15 B17 B18 B20 C9 C10 C12 C13 C15 C17 C18 D9 D10 D12 D14 D15 D17 D18 E7 E9 E10 E12 E13 E15 E17 E18 E20 F7 F9 F10 F12 F14 F15 F17 F18 F20 AA7 AA9 AA10 AA12 AA13 AA15 AA17 AA18 AA20 AB9 AC10 AB10 AB12 AB14 AB15 AB17 AB18

VCC: AB20 AB7 AC7 AC9 AC12 AC13 AC15 AC17 AC18 AD7 AD9 AD10 AD12 AD14 AD15 AD17 AD18 AE9 AE10 AE12 AE13 AE15 AE17 AE18 AE20 AF9 AF10 AF12 AF14 AF15 AF17 AF18 AF20

(CPU IO POWER 1.05V)
=PP1V05_S0_CPU 8 10 12 13

4500 mA (before VCC stable)
2500 mA (after VCC stable)

VCCP: G21 V6 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21

(CPU INTERNAL PLL POWER 1.5V)
=PP1V5_S0_CPU 8 12

130 mA

VCCA: B26 C26

VID0	AD6	CPU_VID<0>	OUT 12 79
VID1	AF5	CPU_VID<1>	OUT 12 79
VID2	AE5	CPU_VID<2>	OUT 12 79
VID3	AF4	CPU_VID<3>	OUT 12 79
VID4	AE3	CPU_VID<4>	OUT 12 79
VID5	AF3	CPU_VID<5>	OUT 12 79
VID6	AE2	CPU_VID<6>	OUT 12 79
VCCSENSE	AF7	CPU_VCCSENSE_P	OUT 58 79
VSSSENSE	AE7	CPU_VCCSENSE_N	OUT 58 79

=PPVCORE_S0_CPU 8 11 12 49

R1100
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

OMIT
U1000
MEROM
FCBGA
4 OF 4

VSS: A4 A8 A11 A14 A16 A19 A23 AF2 B6 B8 B11 B13 B16 B19 B21 B24 C5 C8 C11 C14 C16 C19 C2 C22 C25 D1 D4 D8 D11 D13 D16 D19 D23 D26 E3 E6 E8 E11 E14 E16 E19 E21 E24 F5 F8 F11 F13 F16 F19 F2 F22 F25 G4 G1 G23 G26 H3 H6 H21 H24 J2 J5 J22 J25 K1 K4 K23 K26 L3 L6 L21 L24 M2 M5 M22 M25 N1 N4 N23 N26 P3

VSS: P6 P21 P24 R2 R5 R22 R25 T1 T4 T23 T26 U3 U6 U21 U24 V2 V5 V22 V25 W1 W4 W23 W26 Y3 Y6 Y21 Y24 AA2 AA5 AA8 AA11 AA14 AA16 AA19 AA22 AA25 AB1 AB4 AB8 AB11 AB13 AB16 AB19 AB23 AB26 AC3 AC6 AC8 AC11 AC14 AC16 AC19 AC21 AC24 AD2 AD5 AD8 AD11 AD13 AD16 AD19 AD22 AD25 AE1 AE4 AE8 AE11 AE14 AE16 AE19 AE23 AE26 A2 AF6 AF8 AF11 AF13 AF16 AF19 AF21 A25 AF25

CPU Power & Ground

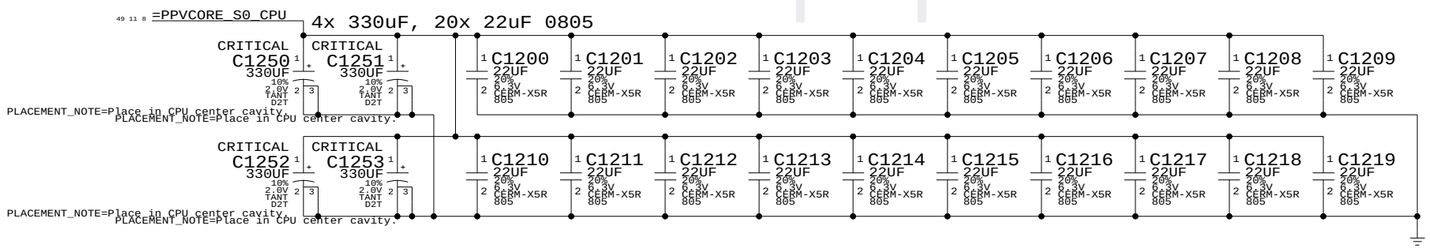
SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

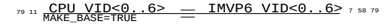
SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 11 OF 109	

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

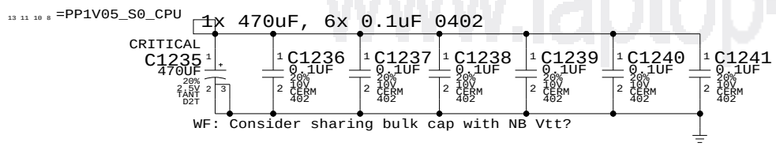
CPU VCORE HF AND BULK DECOUPLING



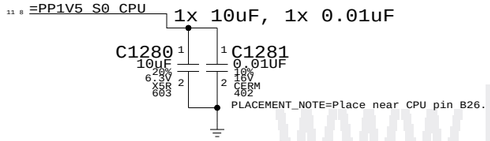
CPU VCORE VID CONNECTIONS



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

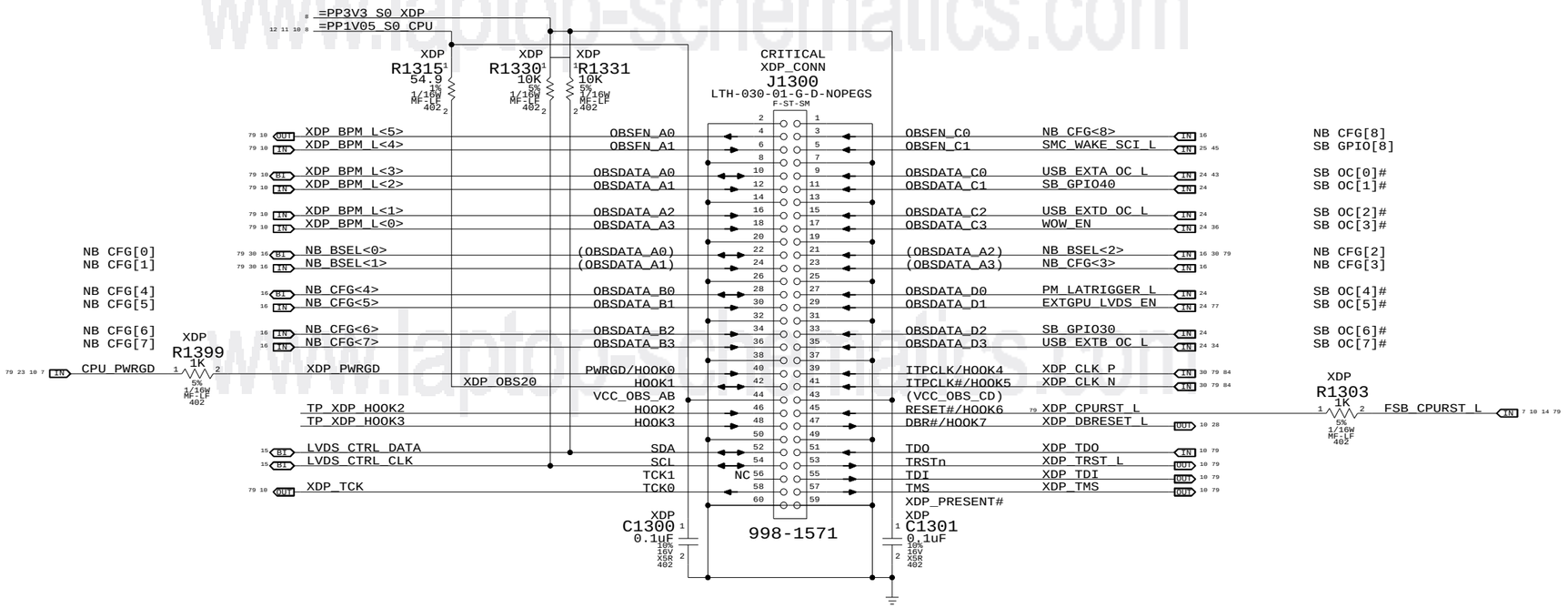
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 12 OF 109	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

SYNC_MASTER=T9_NOME SYNC_DATE=12/12/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	13	109

OMIT

U1400
CRESTLINE
FCBGA
(1 OF 10)
HOST

FSB_D_L<0>	E2	H_D0*		H_A3*	J13	FSB_A_L<3>	
FSB_D_L<1>	G2	H_D1*		H_A4*	B11	FSB_A_L<4>	
FSB_D_L<2>	G7	H_D2*		H_A5*	C11	FSB_A_L<5>	
FSB_D_L<3>	M6	H_D3*		H_A6*	M11	FSB_A_L<6>	
FSB_D_L<4>	H7	H_D4*		H_A7*	C15	FSB_A_L<7>	
FSB_D_L<5>	H3	H_D5*		H_A8*	F16	FSB_A_L<8>	
FSB_D_L<6>	G4	H_D6*		H_A9*	L13	FSB_A_L<9>	
FSB_D_L<7>	F3	H_D7*		H_A10*	G17	FSB_A_L<10>	
FSB_D_L<8>	N8	H_D8*		H_A11*	C14	FSB_A_L<11>	
FSB_D_L<9>	H2	H_D9*		H_A12*	K16	FSB_A_L<12>	
FSB_D_L<10>	M10	H_D10*		H_A13*	B13	FSB_A_L<13>	
FSB_D_L<11>	N12	H_D11*		H_A14*	L16	FSB_A_L<14>	
FSB_D_L<12>	N9	H_D12*		H_A15*	J17	FSB_A_L<15>	
FSB_D_L<13>	H5	H_D13*		H_A16*	B14	FSB_A_L<16>	
FSB_D_L<14>	P13	H_D14*		H_A17*	K19	FSB_A_L<17>	
FSB_D_L<15>	K9	H_D15*		H_A18*	P15	FSB_A_L<18>	
FSB_D_L<16>	M2	H_D16*		H_A19*	R17	FSB_A_L<19>	
FSB_D_L<17>	W10	H_D17*		H_A20*	B16	FSB_A_L<20>	
FSB_D_L<18>	Y8	H_D18*		H_A21*	H20	FSB_A_L<21>	
FSB_D_L<19>	V4	H_D19*		H_A22*	L19	FSB_A_L<22>	
FSB_D_L<20>	M3	H_D20*		H_A23*	D17	FSB_A_L<23>	
FSB_D_L<21>	J1	H_D21*		H_A24*	M17	FSB_A_L<24>	
FSB_D_L<22>	N5	H_D22*		H_A25*	N16	FSB_A_L<25>	
FSB_D_L<23>	N3	H_D23*		H_A26*	J19	FSB_A_L<26>	
FSB_D_L<24>	W6	H_D24*		H_A27*	B18	FSB_A_L<27>	
FSB_D_L<25>	W9	H_D25*		H_A28*	E19	FSB_A_L<28>	
FSB_D_L<26>	N2	H_D26*		H_A29*	B17	FSB_A_L<29>	
FSB_D_L<27>	Y7	H_D27*		H_A30*	B15	FSB_A_L<30>	
FSB_D_L<28>	Y9	H_D28*		H_A31*	E17	FSB_A_L<31>	
FSB_D_L<29>	P4	H_D29*		H_A32*	C18	FSB_A_L<32>	
FSB_D_L<30>	W3	H_D30*		H_A33*	A19	FSB_A_L<33>	
FSB_D_L<31>	N1	H_D31*		H_A34*	B19	FSB_A_L<34>	
FSB_D_L<32>	AD12	H_D32*		H_A35*	N19	FSB_A_L<35>	
FSB_D_L<33>	AE3	H_D33*					
FSB_D_L<34>	AD9	H_D34*		H_ADS*	G12	FSB_ADS_L	
FSB_D_L<35>	AC9	H_D35*		H_ADSTB0*	H17	FSB_ADSTB_L<0>	
FSB_D_L<36>	AC7	H_D36*		H_ADSTB1*	G20	FSB_ADSTB_L<1>	
FSB_D_L<37>	AC14	H_D37*		H_BNR*	C8	FSB_BNR_L	
FSB_D_L<38>	AD11	H_D38*		H_BPRI*	E8	FSB_BPRI_L	
FSB_D_L<39>	AC11	H_D39*		H_BREQ*	F12	FSB_BREQ0_L	
FSB_D_L<40>	AB2	H_D40*		H_DEFER*	D6	FSB_DEFER_L	
FSB_D_L<41>	AD7	H_D41*		H_DBSY*	C10	FSB_DBSY_L	
FSB_D_L<42>	AB1	H_D42*		HPLL_CLK	AM5	FSB_CLK_NB_P	
FSB_D_L<43>	Y3	H_D43*		HPLL_CLK*	AM7	FSB_CLK_NB_N	
FSB_D_L<44>	AC6	H_D44*		H_DPWR*	H8	FSB_DPWR_L	
FSB_D_L<45>	AE2	H_D45*		H_DRDY*	K7	FSB_DRDY_L	
FSB_D_L<46>	AC5	H_D46*		H_HIT*	E4	FSB_HIT_L	
FSB_D_L<47>	AG3	H_D47*		H_HITM*	C6	FSB_HITM_L	
FSB_D_L<48>	AJ3	H_D48*		H_LOCK*	G10	FSB_LOCK_L	
FSB_D_L<49>	AH8	H_D49*		H_TRDY*	B7	FSB_TRDY_L	
FSB_D_L<50>	AJ14	H_D50*					
FSB_D_L<51>	AE9	H_D51*					
FSB_D_L<52>	AE11	H_D52*					
FSB_D_L<53>	AH12	H_D53*					
FSB_D_L<54>	AJ5	H_D54*					
FSB_D_L<55>	AH5	H_D55*					
FSB_D_L<56>	AJ6	H_D56*					
FSB_D_L<57>	AE7	H_D57*					
FSB_D_L<58>	AJ7	H_D58*					
FSB_D_L<59>	AJ2	H_D59*					
FSB_D_L<60>	AE5	H_D60*					
FSB_D_L<61>	AJ3	H_D61*					
FSB_D_L<62>	AH2	H_D62*					
FSB_D_L<63>	AH13	H_D63*					

H_DINV0*	K5	FSB_DINV_L<0>	
H_DINV1*	L2	FSB_DINV_L<1>	
H_DINV2*	AD13	FSB_DINV_L<2>	
H_DINV3*	AE13	FSB_DINV_L<3>	
H_DSTBN0*	M7	FSB_DSTB_L_N<0>	
H_DSTBN1*	K3	FSB_DSTB_L_N<1>	
H_DSTBN2*	AD2	FSB_DSTB_L_N<2>	
H_DSTBN3*	AH11	FSB_DSTB_L_N<3>	
H_DSTBP0*	L7	FSB_DSTB_L_P<0>	
H_DSTBP1*	K2	FSB_DSTB_L_P<1>	
H_DSTBP2*	AC2	FSB_DSTB_L_P<2>	
H_DSTBP3*	AJ10	FSB_DSTB_L_P<3>	
H_REQ0*	M14	FSB_REQ_L<0>	
H_REQ1*	E13	FSB_REQ_L<1>	
H_REQ2*	A11	FSB_REQ_L<2>	
H_REQ3*	H13	FSB_REQ_L<3>	
H_REQ4*	B12	FSB_REQ_L<4>	
H_RS0*	E12	FSB_RS_L<0>	
H_RS1*	D7	FSB_RS_L<1>	
H_RS2*	D8	FSB_RS_L<2>	

NB_FSB_SWING	B3	H_SWING	
NB_FSB_RCOMP	C2	H_RCOMP	
NB_FSB_SCOMP	W1	H_SCOMP	
NB_FSB_SCOMP_L	W2	H_SCOMP*	
FSB_CPURST_L	B6	H_CPURST*	
FSB_CPUSLP_L	E5	H_CPUSLP*	
NB_FSB_VREF	B9	H_AVREF	
	A9	H_DVREF	

=PP1V25R1V05_S0_FSB_NB

R1421 54.9 1% 1/16W MF-LF 402
R1420 54.9 1% 1/16W MF-LF 402
R1410 221 1% 1/16W MF-LF 402
R1425 1K 1% 1/16W MF-LF 402
R1426 2.0K 1% 1/16W MF-LF 402
C1425 0.1uF 10% 10V X5R 402
R1415 24.9 1% 1/16W MF-LF 402
R1411 100 1% 1/16W MF-LF 402
C1410 0.1uF 10% 10V X5R 402

NB CPU Interface

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 14 OF 109	

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

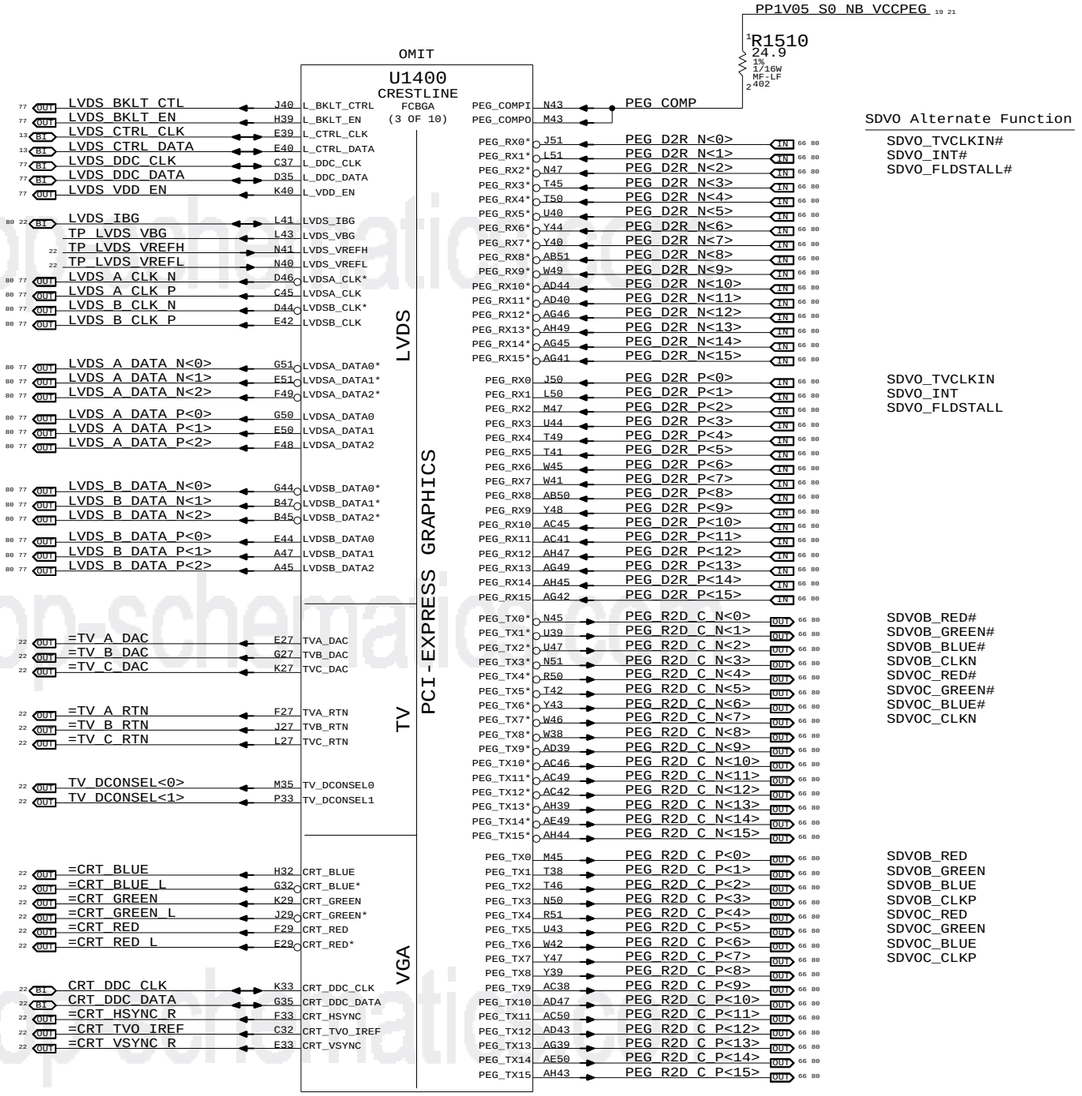
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 15 OF 109	

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

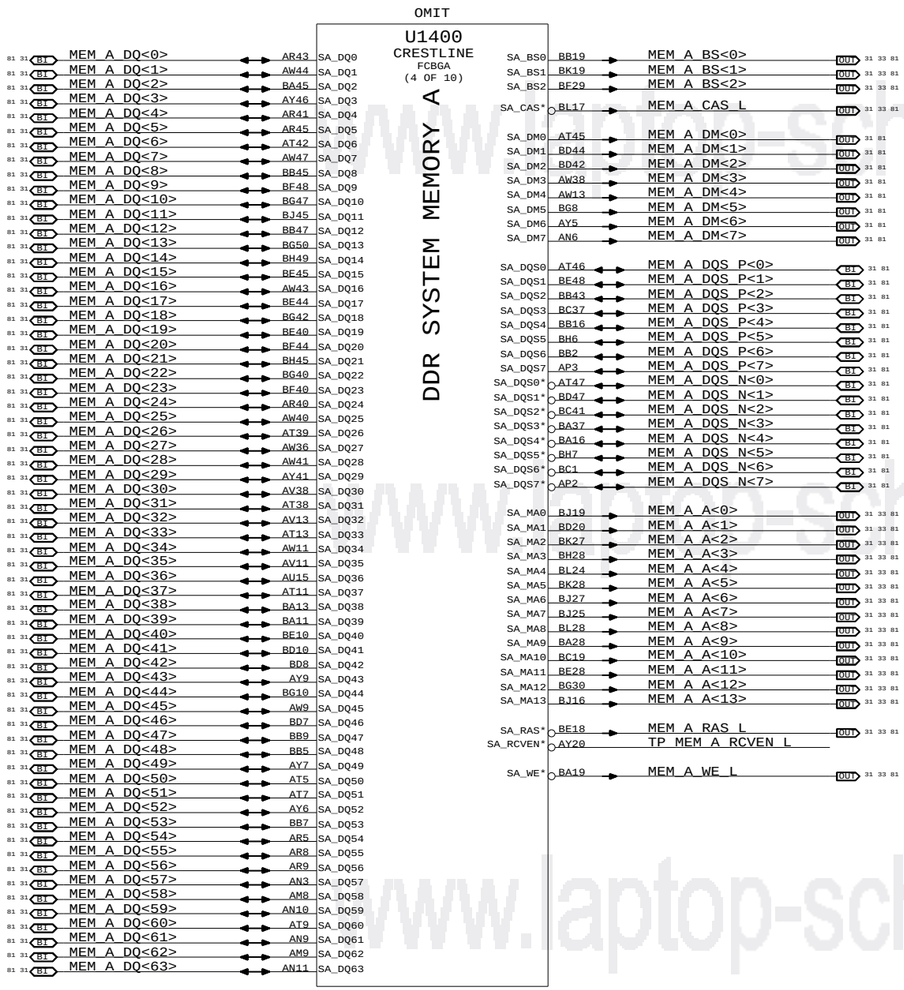
NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

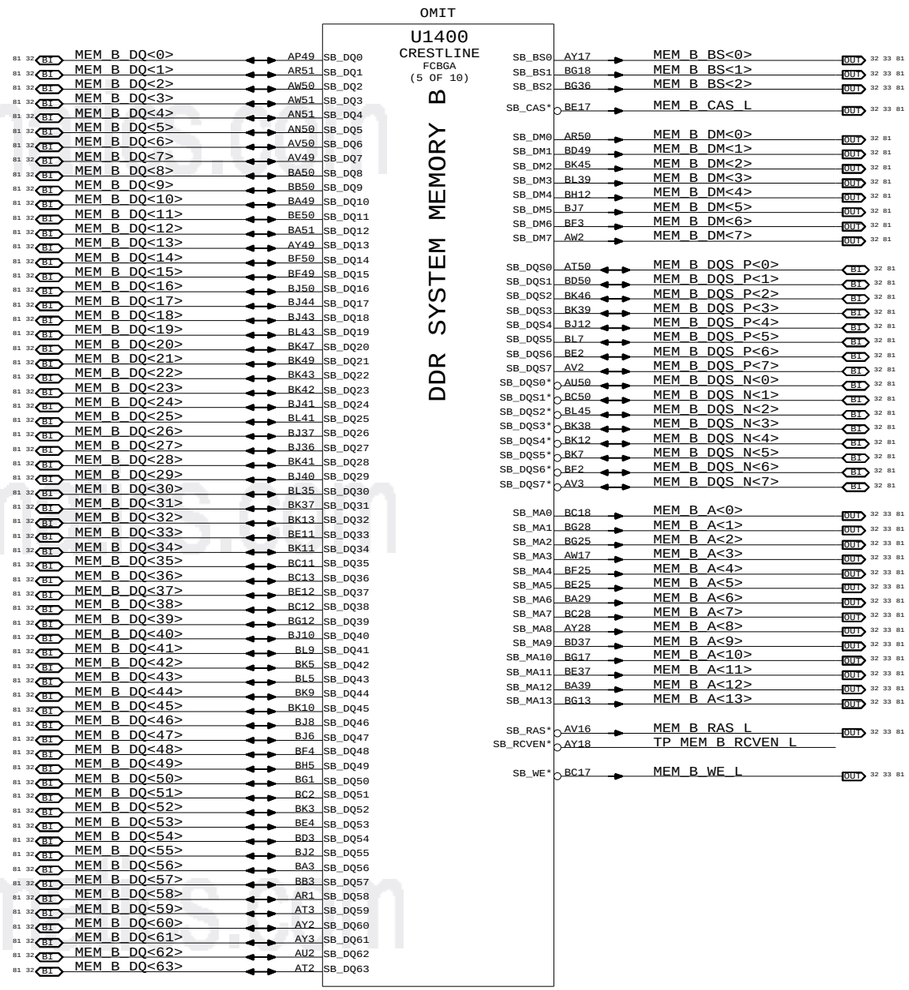
NB Misc Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 16 OF 109	



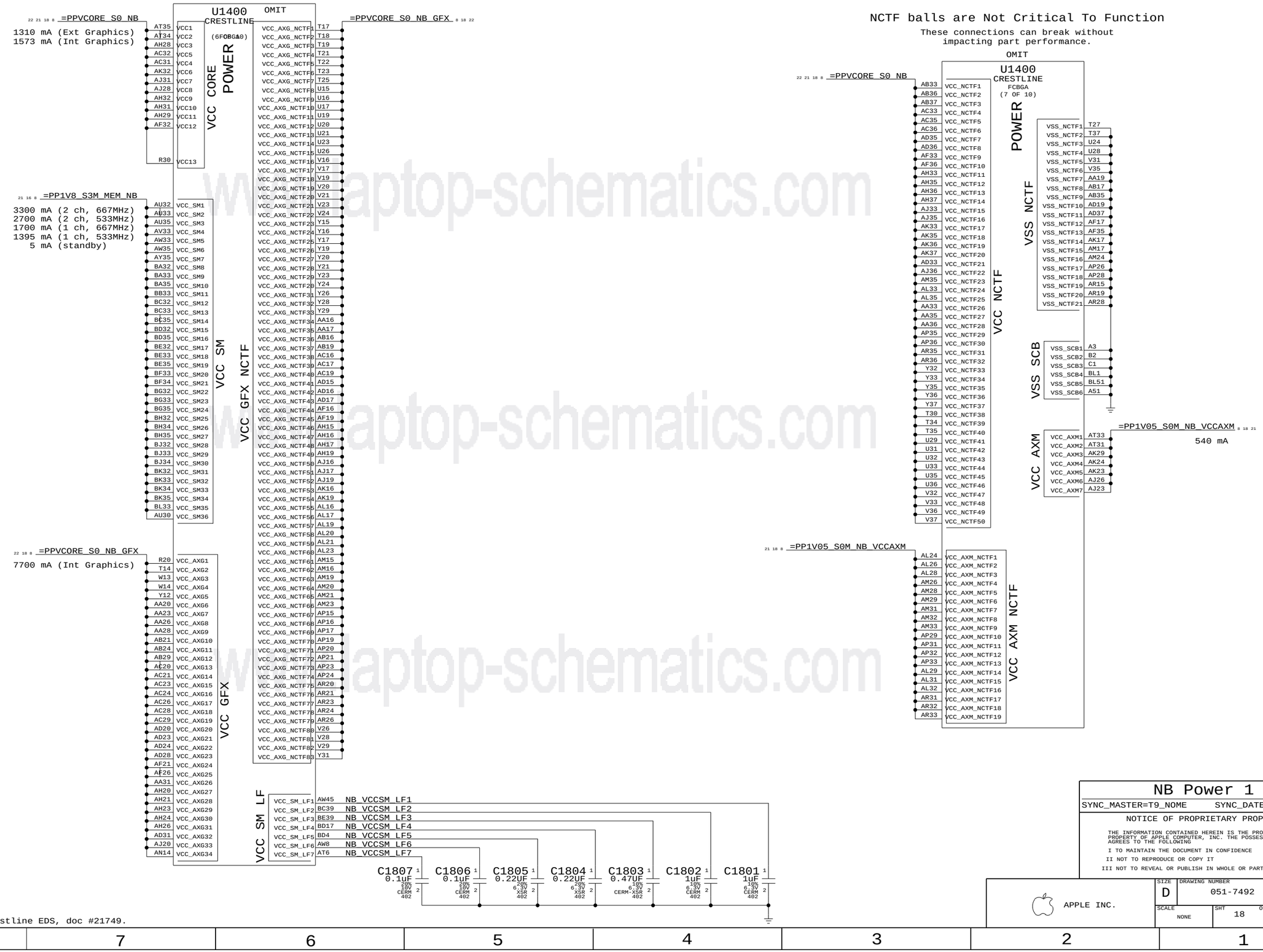


NB DDR2 Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 17 OF 109	

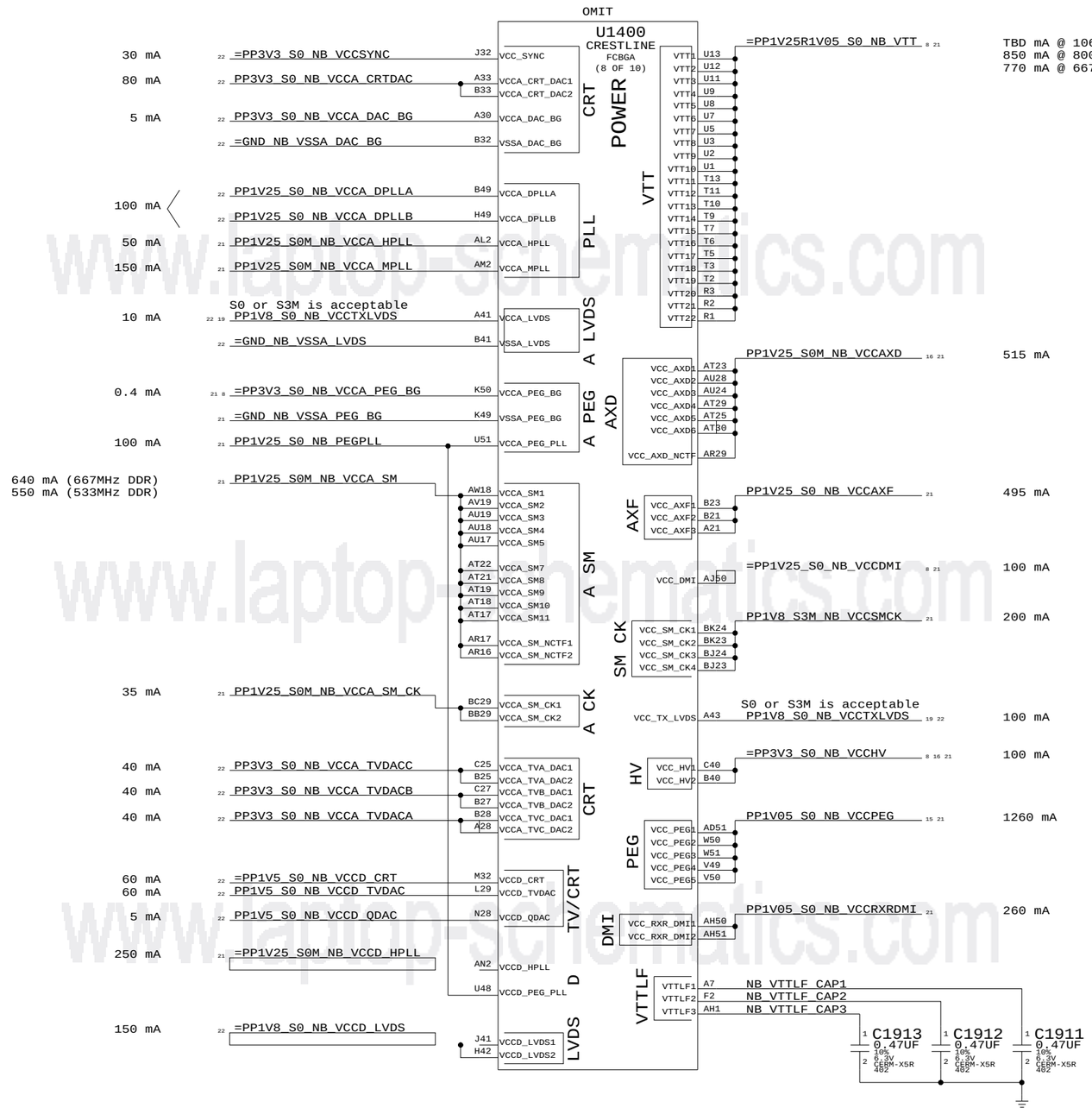


NB Power 1

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 18 OF 109	



Current numbers from Crestline EDS, doc #21749.

NB Power 2

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 19 OF 109	

OMIT

U1400
CRESTLINE
FCBGA
(9 OF 10)
VSS

A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AY10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B38
AD26	VSS21	VSS120	B43
AD29	VSS22	VSS121	B46
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BB12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BG19
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BJ11
AN43	VSS72	VSS171	BJ13
AN5	VSS73	VSS172	BJ38
AN7	VSS74	VSS173	BJ4
AP4	VSS75	VSS174	BJ42
AP48	VSS76	VSS175	BJ46
AP50	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C36
AW16	VSS99	VSS198	C41

OMIT

U1400
CRESTLINE
FCBGA
(10 OF 10)
VSS

C46	VSS199	VSS287	W11
C50	VSS200	VSS288	W39
C7	VSS201	VSS289	W43
D13	VSS202	VSS290	W47
D24	VSS203	VSS291	W5
D3	VSS204	VSS292	W7
D32	VSS205	VSS293	Y13
D39	VSS206	VSS294	Y2
D45	VSS207	VSS295	Y41
D49	VSS208	VSS296	Y45
E10	VSS209	VSS297	Y49
E16	VSS210	VSS298	Y5
E24	VSS211	VSS299	Y50
E28	VSS212	VSS300	Y11
E32	VSS213	VSS301	P29
E47	VSS214		
F19	VSS215		
F36	VSS216	TDE_SENSE VSS302	T29
F4	VSS217		
F40	VSS218		
F50	VSS219	TDE_FORCE VSS303	T31
G1	VSS220		
G13	VSS221		
G16	VSS222	TDB_FORCE VSS304	T33
G19	VSS223		
G24	VSS224		
G28	VSS225	TDB_SENSE VSS305	R28
G29	VSS226		
G33	VSS227		
G42	VSS228		
G45	VSS229	VSS306	AA32
G48	VSS230	VSS307	AB32
G8	VSS231	VSS308	AD32
H24	VSS232	VSS309	AF28
H28	VSS233	VSS310	AF29
H4	VSS234	VSS311	AT27
H45	VSS235	VSS312	AV25
J11	VSS236	VSS313	H50
J16	VSS237		
J2	VSS238		
J24	VSS239		
J28	VSS240		
J33	VSS241		
J35	VSS242		
J39	VSS243		
K12	VSS245		
K47	VSS246		
K8	VSS247		
L1	VSS248		
L17	VSS249		
L20	VSS250		
L24	VSS251		
L28	VSS252		
L3	VSS253		
L33	VSS254		
L49	VSS255		
M28	VSS256		
M42	VSS257		
M46	VSS258		
M49	VSS259		
M5	VSS260		
M50	VSS261		
M9	VSS262		
N11	VSS263		
N14	VSS264		
N17	VSS265		
N29	VSS266		
N32	VSS267		
N36	VSS268		
N39	VSS269		
N44	VSS270		
N49	VSS271		
N7	VSS272		
P19	VSS273		
P2	VSS274		
P23	VSS275		
P3	VSS276		
P50	VSS277		
R49	VSS278		
T39	VSS279		
T43	VSS280		
T47	VSS281		
U41	VSS282		
U45	VSS283		
U50	VSS284		
V2	VSS285		
V3	VSS286		

Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

TDE_SENSE T29 =NB_TDE_SENSE S1

NOTE: TDE = _P

TDE_FORCE T31 =NB_TDE_FORCE S1

TDB_FORCE T33 =NB_TDB_FORCE S1

NOTE: TDB = _N

TDB_SENSE R28 =NB_TDB_SENSE S1

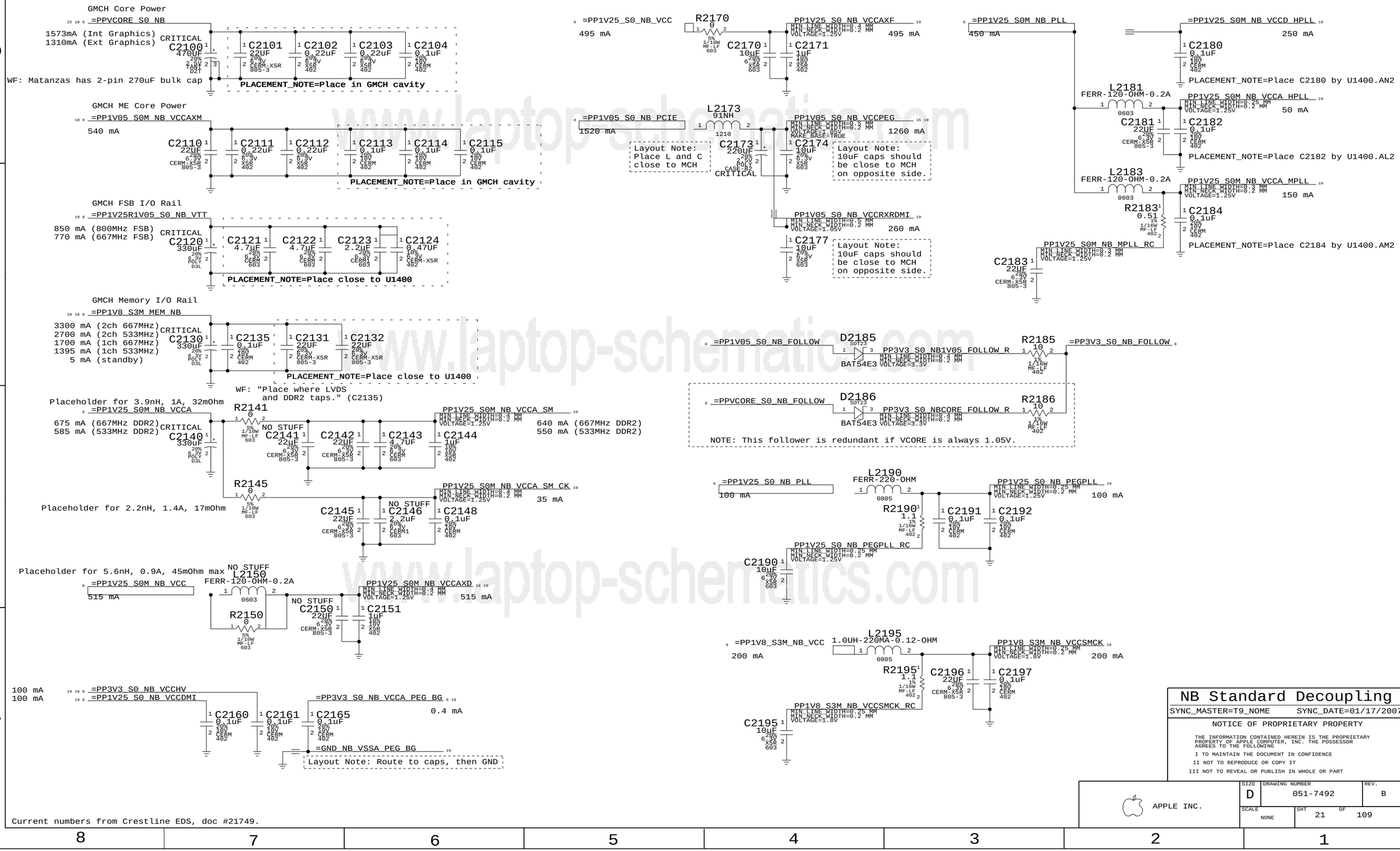
NB Grounds

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	20	109


GMCH Core Power
=PPVCORE_S0_NB
1573mA (Int Graphics)
1310mA (Ext Graphics)
CRITICAL
C2100 470uF
C2101 22UF
C2102 0.22uF
C2103 0.22uF
C2104 0.1uF
WF: Matanzas has 2-pin 270uF bulk cap
PLACEMENT_NOTE=Place in GMCH cavity
GMCH ME Core Power
=PP1V05_S0M_NB_VCCAXM
540 mA
C2110 22UF
C2111 0.22uF
C2112 0.22uF
C2113 0.1uF
C2114 0.1uF
C2115 0.1uF
PLACEMENT_NOTE=Place in GMCH cavity
GMCH FSB I/O Rail
=PP1V25R1V05_S0_NB_VTT
850 mA (800MHz FSB)
770 mA (667MHz FSB)
CRITICAL
C2120 330uF
C2121 4.7uF
C2122 4.7uF
C2123 2.2uF
C2124 0.47UF
PLACEMENT_NOTE=Place close to U1400
GMCH Memory I/O Rail
=PP1V8_S3M_MEM_NB
3300 mA (2ch 667MHz)
2700 mA (2ch 533MHz)
1700 mA (1ch 667MHz)
1395 mA (1ch 533MHz)
5 mA (standby)
CRITICAL
C2130 330uF
C2135 0.1uF
C2131 22UF
C2132 22UF
PLACEMENT_NOTE=Place close to U1400
WF: "Place where LVDS
and DDR2 taps." (C2135)
Placeholder for 3.9nH, 1A, 32mOhm
=PP1V25_S0M_NB_VCCA
675 mA (667MHz DDR2)
585 mA (533MHz DDR2)
R2141 0
CRITICAL
C2140 330uF
NO STUFF
C2141 22UF
C2142 22UF
C2143 4.7UF
C2144 1uF
PP1V25_S0M_NB_VCCA_SM
640 mA (667MHz DDR2)
550 mA (533MHz DDR2)
Placeholder for 2.2nH, 1.4A, 17mOhm
R2145 0
C2145 22UF
NO STUFF
C2146 2.2uF
C2148 0.1uF
PP1V25_S0M_NB_VCCA_SM_CK
35 mA
Placeholder for 5.6nH, 0.9A, 45mOhm max
=PP1V25_S0M_NB_VCC
515 mA
NO STUFF
L2150 FERR-120-OHM-0.2A
R2150 0
NO STUFF
C2150 22UF
C2151 1uF
PP1V25_S0M_NB_VCCAXD
515 mA
100 mA =PP3V3_S0_NB_VCCHV
100 mA =PP1V25_S0_NB_VCCDMI
C2160 0.1uF
C2161 0.1uF
=PP3V3_S0_NB_VCCA_PEG_BG
0.4 mA
C2165 0.1uF
=GND_NB_VSSA_PEG_BG
Layout Note: Route to caps, then GND
Current numbers from Crestline EDS, doc #21749.
=PP1V25_S0_NB_VCC
495 mA
R2170 0
PP1V25_S0_NB_VCCAXF
495 mA
C2170 10uF
C2171 1uF
=PP1V25_S0_NB_PCIE
1520 mA
L2173 91NH
PP1V05_S0_NB_VCCPEG
1260 mA
Layout Note:
Place L and C
close to MCH
C2173 220UF
C2174 10uF
Layout Note:
10uF caps should
be close to MCH
on opposite side.
PP1V05_S0_NB_VCCRXRDMI
260 mA
C2177 10uF
Layout Note:
10uF caps should
be close to MCH
on opposite side.
=PP1V25_S0M_NB_PLL
450 mA
=PP1V25_S0M_NB_VCCD_HPLL
250 mA
C2180 0.1uF
PLACEMENT_NOTE=Place C2180 by U1400.AN2
L2181 FERR-120-OHM-0.2A
PP1V25_S0M_NB_VCCA_HPLL
50 mA
C2181 22UF
C2182 0.1uF
PLACEMENT_NOTE=Place C2182 by U1400.AL2
L2183 FERR-120-OHM-0.2A
PP1V25_S0M_NB_VCCA_MPLL
150 mA
R2183 0.51
C2184 0.1uF
PLACEMENT_NOTE=Place C2184 by U1400.AM2
PP1V25_S0M_NB_MPLL_RC
C2183 22UF
=PP1V05_S0_NB_FOLLOW
D2185 BAT54E3
PP3V3_S0_NB1V05_FOLLOW_R
R2185 10
=PP3V3_S0_NB_FOLLOW
=PPVCORE_S0_NB_FOLLOW
D2186 BAT54E3
PP3V3_S0_NBCORE_FOLLOW_R
R2186 10
NOTE: This follower is redundant if VCORE is always 1.05V.
=PP1V25_S0_NB_PLL
100 mA
L2190 FERR-220-OHM
PP1V25_S0_NB_PEGPLL
100 mA
R2190 1.1
C2191 0.1uF
C2192 0.1uF
PP1V25_S0_NB_PEGPLL_RC
C2190 10uF
=PP1V8_S3M_NB_VCC
200 mA
L2195 1.0UH-220MA-0.12-OHM
PP1V8_S3M_NB_VCCSMCK
200 mA
R2195 1.1
C2196 22UF
C2197 0.1uF
PP1V8_S3M_NB_VCCSMCK_RC
C2195 10uF
NB Standard Decoupling
SYNC_MASTER=T9_NOME
SYNC_DATE=01/17/2007
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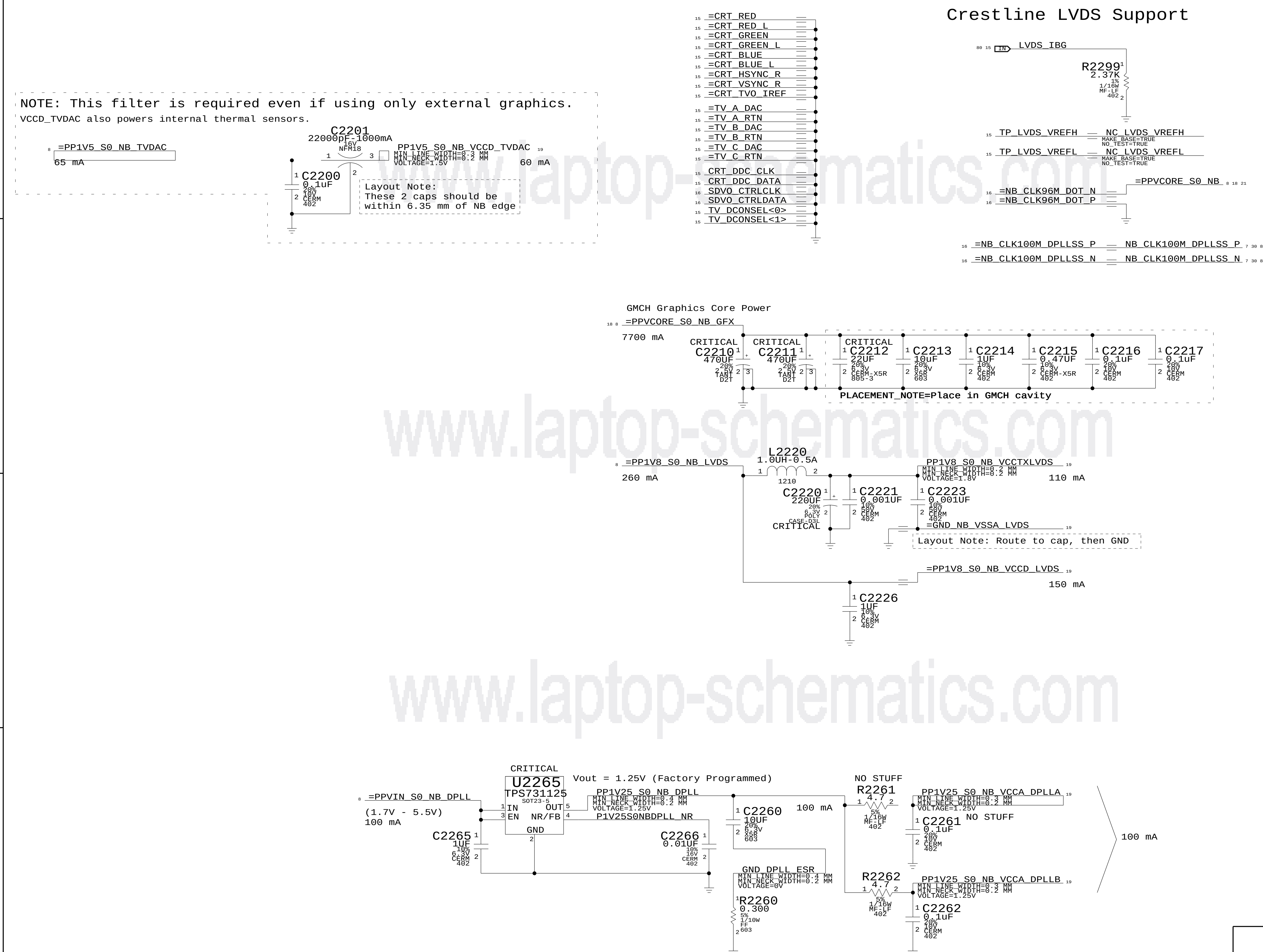
APPLE INC.
SIZE D
DRAWING NUMBER 051-7492
REV. B
SCALE NONE
SHT 21 OF 109



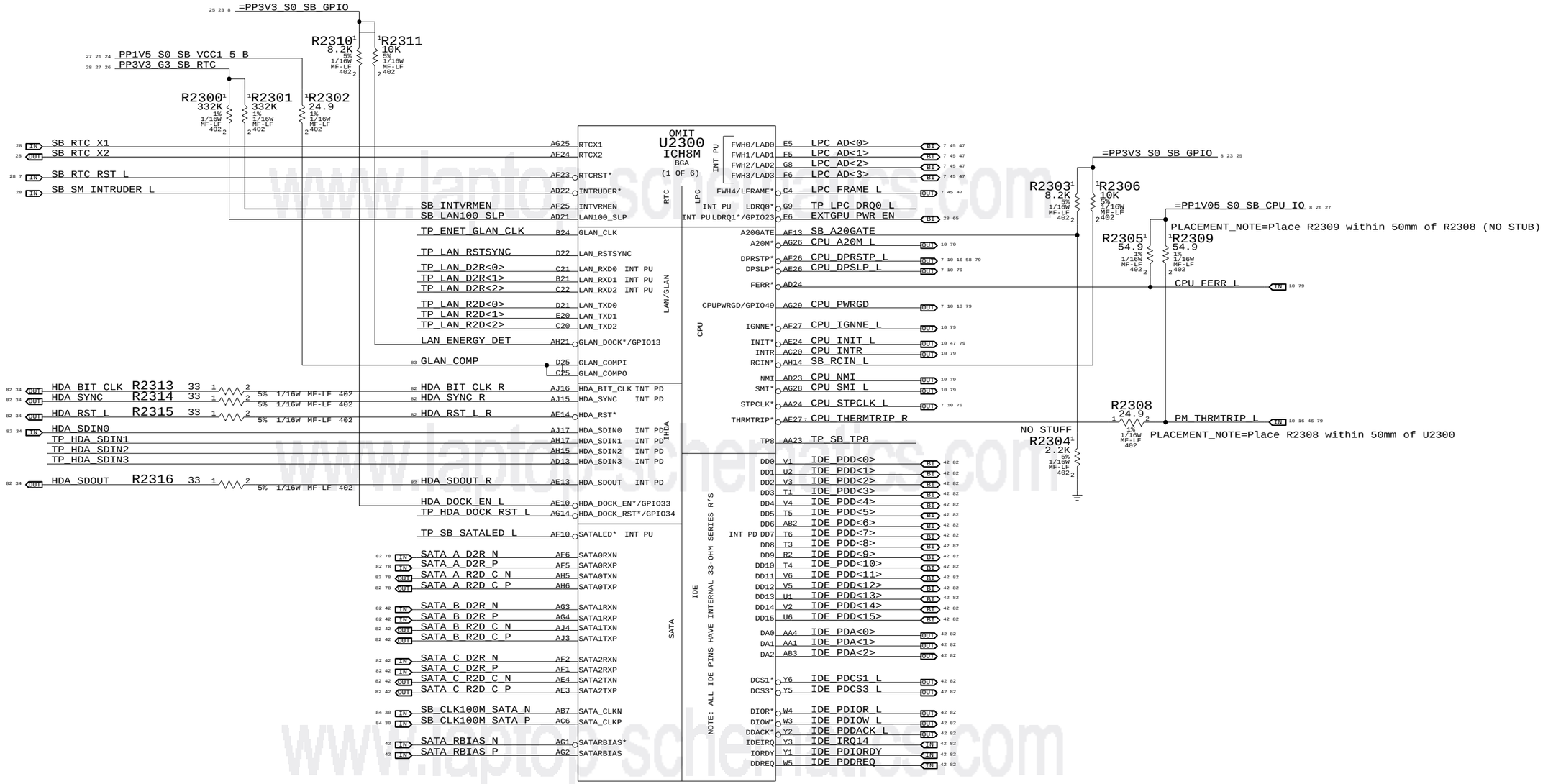
Current numbers from Crestline EDS Addendum, doc #20127.

NB Graphics Decoupling

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE NONE	SHT 22	OF 109



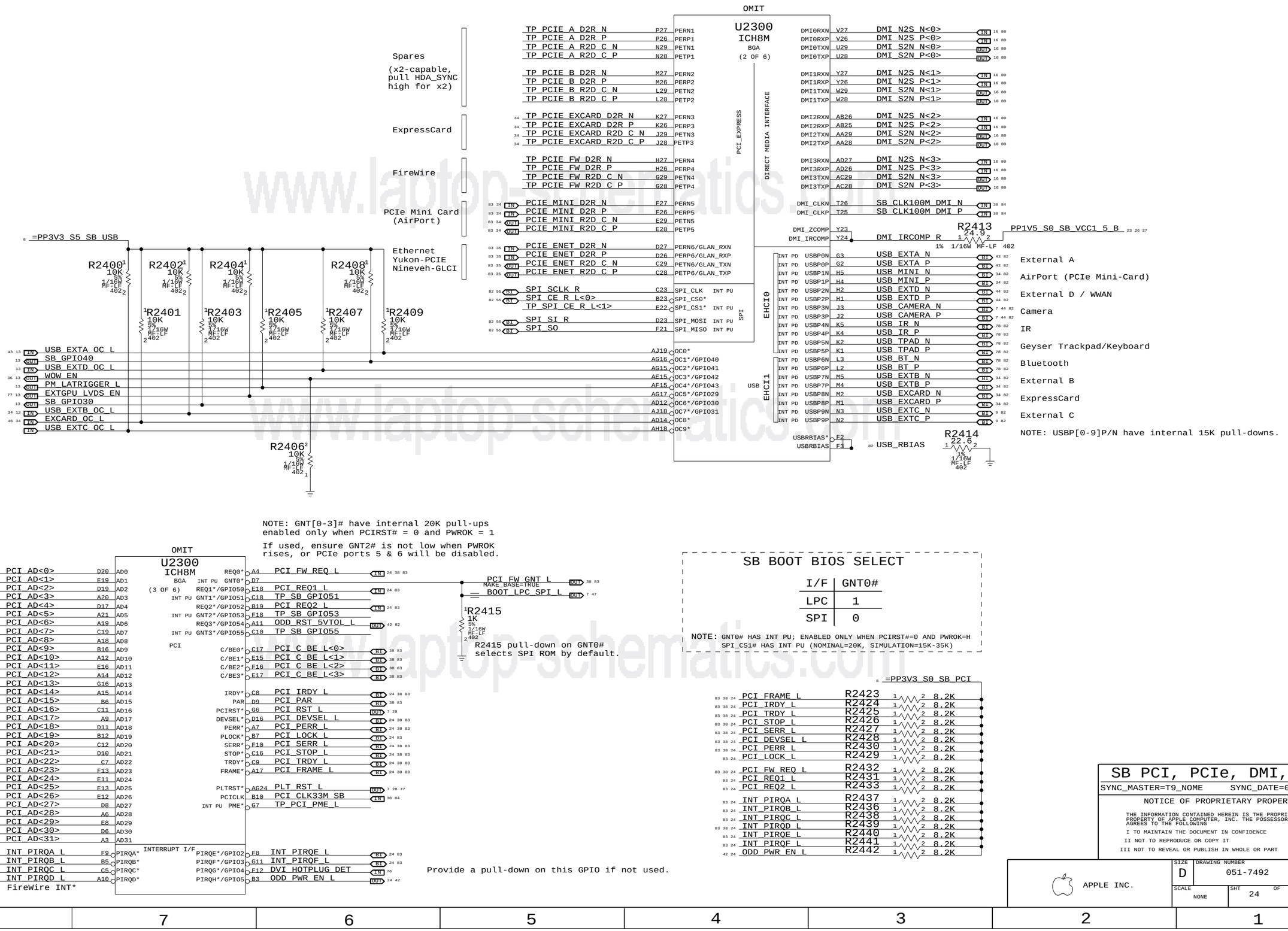
	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 23 OF 109	



=PP3V3_S0_SB_GPIO
=PP3V3_S5_SB_GPIO

R2500 1K 5% 1/16W MF-LF 402
R2551 8.2K 5% 1/16W MF-LF 402
R2553 8.2K 5% 1/16W MF-LF 402
R2504 10K 5% 1/16W MF-LF 402
R2506 10K 5% 1/16W MF-LF 402
R2510 1K 5% 1/16W MF-LF 402
NO_REBOOT_MODE

R2502 10K 5% 1/16W MF-LF 402
R2550 10K 5% 1/16W MF-LF 402
R2552 10K 5% 1/16W MF-LF 402
R2547 10K 5% 1/16W MF-LF 402
R2505 8.2K 5% 1/16W MF-LF 402
R2507 8.2K 5% 1/16W MF-LF 402

R2532 10K 5% 1/16W MF-LF 402
R2535 10K 5% 1/16W MF-LF 402
R2533 10K 5% 1/16W MF-LF 402
R2534 10K 5% 1/16W MF-LF 402

OMIT
U2300
ICH8M
BGA
(4 OF 6)

SMB_CLK — AJ26 SMBCLK
SMB_DATA — AD19 SMBDATA
TP_CLINK_WLAN_RESET_L — AG21 LINKALERT*
SMB_ME_CLK — AC17 SMLINK0
SMB_ME_DATA — AE19 SMLINK1
PM_RI_L — AF17 RI*
PM_SUS_STAT_L — F4 SUS_STAT*/LPCPD*
PM_SYSRST_L — AD15 SYS_RESET*
PM_BMBUSY_L — AG12 BMBUSY*/GPIO0
LINDACARD_GPIO — AG22 SMBALERT*/GPIO11
AE20 STP_PCI*/GPIO15
AG18 STP_CPU*/GPIO25
AH11 CLKRUN*/GPIO32
AE17 WAKE*
AF12 SERIRQ
PM_THRM_L — AC13 THRM*
VR_PWRGD_CLKEN — AJ20 VRMPWRGD
TP_SB_TP7 — AJ22 TP7
PCI_PME_FW_L — AJ8 TACH1/GPIO1
SB_GPIO6 — AJ9 TACH2/GPIO6
AH9 TACH3/GPIO7
AE16 GPIO8
LAN_PHYPC — AC19 GPIO12
EXTGPU_RST_L — AG8 TACH0/GPIO17
SB_GPIO18 — AH12 GPIO18
TP_SB_GPIO20 — AE11 GPIO20 INT PD
SB_SCLOCK — AG10 SCLOCK/GPIO22
SATA_B_PWR_EN_L — AH25 QRT_STATE0/GPIO27
FWH_MFG_MODE — AD16 QRT_STATE1/GPIO28
SB_SATA_CLKREQ_L — AG13 SATACLKREQ*/GPIO35
SB_SLOAD — AF9 SLOAD/GPIO38
SB_SDATAOUT<0> — AJ11 SDATAOUT0/GPIO39
SB_SDATAOUT<1> — AD10 SDATAOUT1/GPIO48
SB_SPKR — AD9 SPKR INT PD
NB_SB_SYNC_L — AJ13 MCH_SYNC*
TP_SB_TP3 — AJ21 TP3 INT PU

SMB
SATA GPIO
CLOCKS
SYS GPIO
POWER MGT
GPIO
CONTROLLER LINK
MISC

SATA0GP/GPIO21 — AJ12 — RSVD_EXTGPU_LVDS_EN
SATA1GP/GPIO19 — AJ10 — SATA_B_DET_L
SATA2GP/GPIO36 — AF11 — SB_GPIO36
SATA3GP/GPIO37 — AG11 — SB_CRT_TVOUT_MUX_L
CLK14 — AG9 — SB_CLK14P3M_TIMER
CLK48 — G5 — SB_CLK48M_USBCTLR
SUSCLK — D3 — SUS_CLK_SB
SLP_S3* — AG23 — PM_SLP_S3_L
SLP_S4* — AF21 — TP_PM_SLP_S4_L
SLP_S5* — AD18 — PM_SLP_S5_L
S4_STATE*/GPIO26 — AH27 — PM_S4_STATE_L
PWROK — AE23 — PM_SB_PWROK
DPRSLPVR/GPIO16 — AJ14 — PM_DPRSLPVR
BATLOW* — AE21 — PM_BATLOW_L
INT PU PWRBTN* — C2 — PM_PWRBTN_L
LAN_RST* — AH20 — PM_LAN_ENABLE
RSMRST* — AG27 — PM_RSMRST_L
CK_PWRGD — E1 — CLK_PWRGD
CLPWROK — E3 — See note below =SB_CLINK_MPWROK
SLP_M* — AJ25 — TP_PM_SLP_M_L
CL_CLK0 — F23 — CLINK_NB_CLK
CL_CLK1 — AE18 — TP_CLINK_WLAN_CLK
CL_DATA0 — F22 — CLINK_NB_DATA
CL_DATA1 — AF19 — TP_CLINK_WLAN_DATA
CL_VREF0 — D24 — SB_CLINK_VREF0
CL_VREF1 — AH23 — SB_CLINK_VREF1
INT PU CL_RST* — AJ23 — CLINK_NB_RESET_L
MEM_LED/GPIO24 — AJ27 — ARB_DETECT_L
ME_EC_ALERT/GPIO10 — AJ24 — SB_GPIO10_CL1
EC_ME_ALERT/GPIO14 — AF22 — SB_GPIO14_CL2
WOL_EN/GPIO9 — AG19 — WOL_EN

NOTE: DPRSLPVR HAS INT 20K PD ENABLED AT BOOT/RESET FOR STRAPPING FUNCTION

PM_LAN_ENABLE must remain deasseted until VccCL3_3, VccLAN3_3 and VccLAN1_05 have been up for at least 1ms.

R2524 100K 5% 1/16W MF-LF 402
R2525 10K 5% 1/16W MF-LF 402

=PP3V3_S0MWOL_SB_CLINK0
R2526 3.24K 1% 1/16W MF-LF 402
C2500 0.1uF 10% 16V X5R 402
R2527 453 1% 1/16W MF-LF 402

=PP3V3_S5_SB_CLINK1
R2528 32.4K 1% 1/16W MF-LF 402
C2501 0.1uF 10% 16V X5R 402
R2529 4.53K 1% 1/16W MF-LF 402

R2523 100K 5% 1/16W MF-LF 402

Test access required for XOR chain testing.

NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

=PP3V3_S5_SB
R2511 10K 5% 1/16W MF-LF 402
R2515 10K 5% 1/16W MF-LF 402
R2514 100K 5% 1/16W MF-LF 402
LINDACARD_GPIO
ARB_DETECT_L
FWH_MFG_MODE
NOSTUFF R2512 0 5% 1/16W MF-LF 402
ARB_ONLY R2516 0 5% 1/16W MF-LF 402

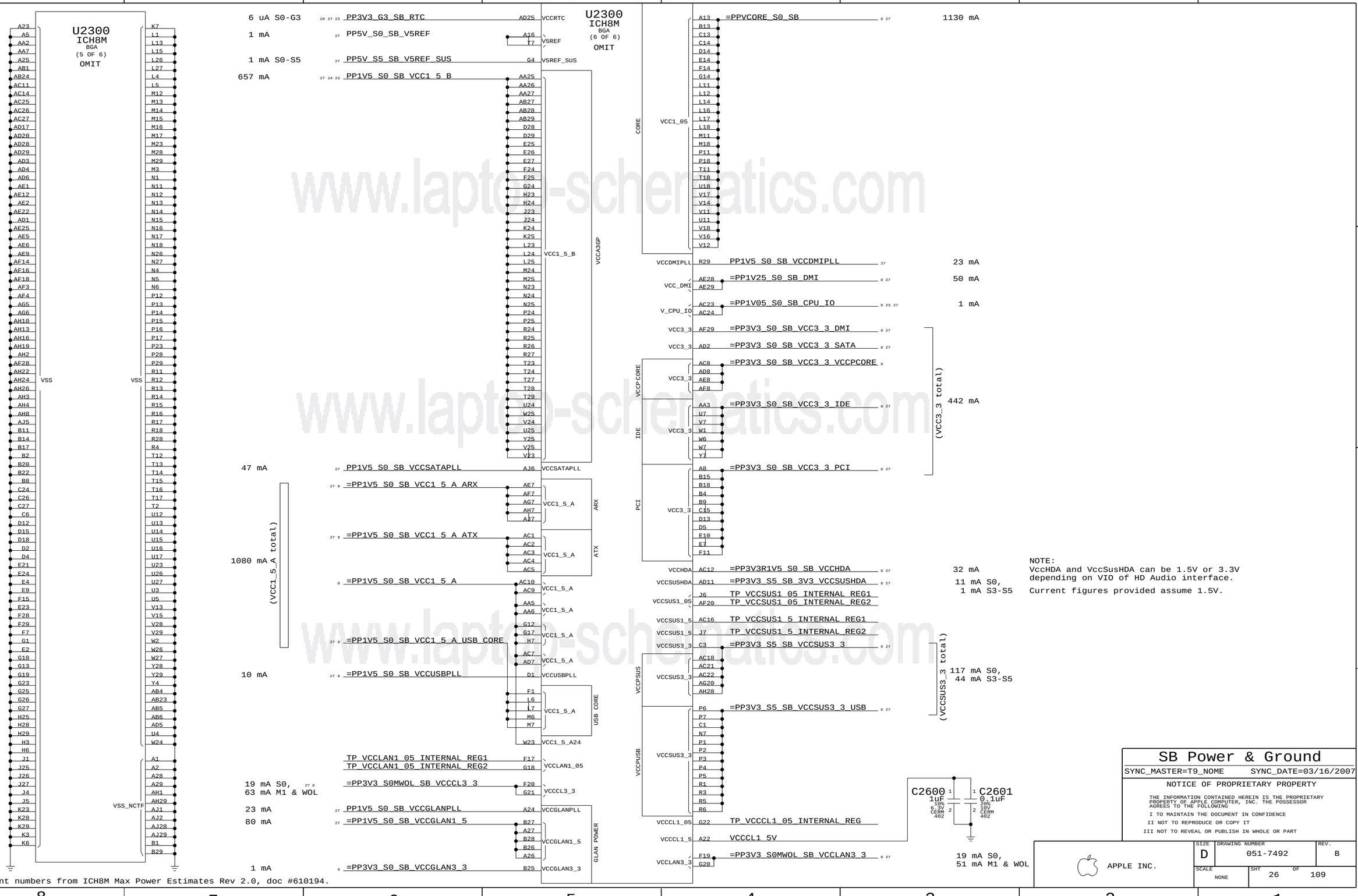
SATA_B_PWR_EN_L — R2530 10K 1% 1/16W MF-LF 402 — =PP3V3_S0_SB_GPIO
PCI_PME_FW_L — R2531 10K 1% 1/16W MF-LF 402
SB_GPIO6 — R2596 10K 1% 1/16W MF-LF 402
EXTGPU_RST_L — R2597 10K 1% 1/16W MF-LF 402
PM_RI_L — R2536 10K 1% 1/16W MF-LF 402 — =PP3V3_S5_SB
PM_BATLOW_L — R2544 8.2K 5% 1/16W MF-LF 402
LAN_PHYPC — R2545 10K 1% 1/16W MF-LF 402
SB_GPIO10_CL1 — R2598 10K 1% 1/16W MF-LF 402
SB_GPIO14_CL2 — R2546 10K 1% 1/16W MF-LF 402

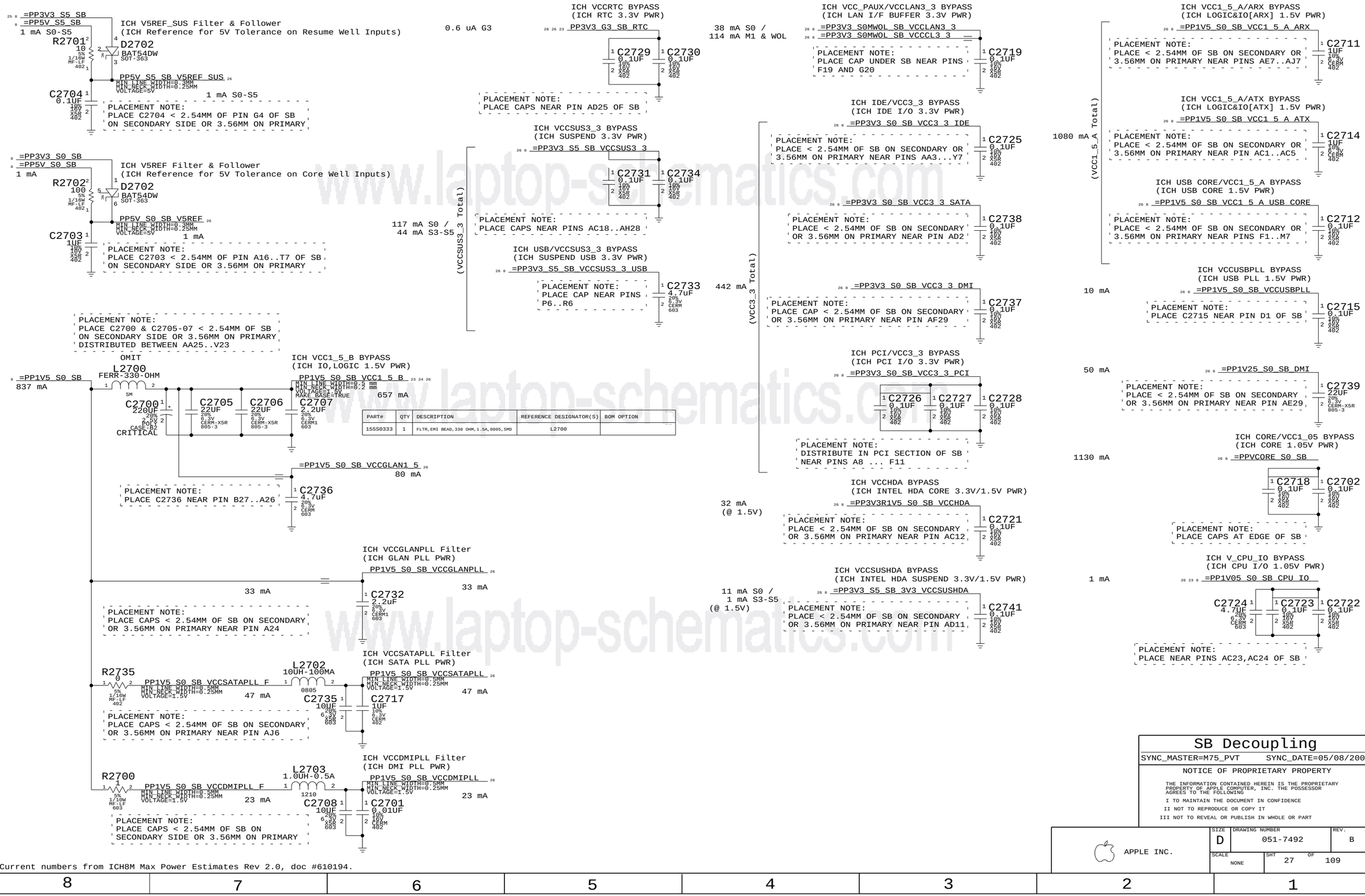
SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 25 OF 109	




ICH V5REF_SUS Filter & Follower
(ICH Reference for 5V Tolerance on Resume Well Inputs)
=PP3V3_S5_SB
=PP5V_S5_SB
1 mA S0-S5
R2701 10 5% 1/16W MF-LF 402
D2702 BAT54DW SOT-363
PP5V_S5_SB_V5REF_SUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
C2704 0.1UF 10% 16V X5R 402
1 mA S0-S5
PLACEMENT NOTE:
PLACE C2704 < 2.54MM OF PIN G4 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH V5REF Filter & Follower
(ICH Reference for 5V Tolerance on Core Well Inputs)
=PP3V3_S0_SB
=PP5V_S0_SB
1 mA
R2702 100 5% 1/16W MF-LF 402
D2702 BAT54DW SOT-363
PP5V_S0_SB_V5REF
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
C2703 1UF 10% 16V X5R 402
1 mA
PLACEMENT NOTE:
PLACE C2703 < 2.54MM OF PIN A16..T7 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
PLACEMENT NOTE:
PLACE C2700 & C2705-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
DISTRIBUTED BETWEEN AA25..V23
OMIT
L2700 FERR-330-OHM SM
=PP1V5_S0_SB
837 mA
C2700 220UF 20% 6.3V CASE-D2 CRITICAL
C2705 22UF 20% 6.3V CERM-X5R 805-3
C2706 22UF 20% 6.3V CERM-X5R 805-3
ICH VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
PP1V5_S0_SB_VCC1_5_B
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
657 mA
C2707 2.2UF 20% 6.3V CERM 603
PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION
155S0333 | 1 | FLTR,EMI BEAD,330 OHM,1.5A,0805,SMD | L2700
=PP1V5_S0_SB_VCCGLAN1_5
80 mA
C2736 4.7UF 20% 6.3V CERM 603
PLACEMENT NOTE:
PLACE C2736 NEAR PIN B27..A26
ICH VCCGLANPLL Filter
(ICH GLAN PLL PWR)
PP1V5_S0_SB_VCCGLANPLL
33 mA
33 mA
C2732 2.2UF 20% 6.3V CERM1 603
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN A24
ICH VCCSATAPLL Filter
(ICH SATA PLL PWR)
R2735 0 5% 1/10W MF-LF 402
PP1V5_S0_SB_VCCSATAPLL_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
47 mA
L2702 10UH-100MA 0805
PP1V5_S0_SB_VCCSATAPLL
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
47 mA
C2735 10UF 20% 6.3V X5R 603
C2717 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AJ6
ICH VCCDMIPLL Filter
(ICH DMI PLL PWR)
R2700 1 5% 1/10W MF-LF 603
PP1V5_S0_SB_VCCDMIPLL_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
23 mA
L2703 1.0UH-0.5A 1210
PP1V5_S0_SB_VCCDMIPLL
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
23 mA
C2708 10UF 20% 6.3V X5R 603
C2701 0.01UF 10% 16V CERM 402
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
0.6 uA G3
PP3V3_G3_SB_RTC
C2729 0.1UF 10% 16V X5R 402
C2730 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PIN AD25 OF SB
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3
(VCCSUS3_3 Total)
117 mA S0 /
44 mA S3-S5
C2731 0.1UF 10% 16V X5R 402
C2734 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PINS AC18..AH28
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3_USB
PLACEMENT NOTE:
PLACE CAP NEAR PINS
P6..R6
C2733 4.7UF 20% 6.3V CERM 603
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
38 mA S0 /
114 mA M1 & WOL
=PP3V3_S0MWOL_SB_VCCLAN3_3
=PP3V3_S0MWOL_SB_VCCCL3_3
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS
F19 AND G20
C2719 0.1UF 10% 16V X5R 402
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_IDE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA3...Y7
C2725 0.1UF 10% 16V X5R 402
(VCC3_3 Total)
442 mA
=PP3V3_S0_SB_VCC3_3_SATA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD2
C2738 1UF 10% 16V X5R 402
=PP3V3_S0_SB_VCC3_3_DMI
PLACEMENT NOTE:
PLACE CAP < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AF29
C2737 0.1UF 10% 16V X5R 402
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_PCI
C2726 0.1UF 10% 16V X5R 402
C2727 0.1UF 10% 16V X5R 402
C2728 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A8 ... F11
ICH VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V/1.5V PWR)
32 mA
(@ 1.5V)
=PP3V3R1V5_S0_SB_VCCHDA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AC12
C2721 0.1UF 10% 16V X5R 402
ICH VCCSUSHDA BYPASS
(ICH INTEL HDA SUSPEND 3.3V/1.5V PWR)
11 mA S0 /
1 mA S3-S5
(@ 1.5V)
=PP3V3_S5_SB_3V3_VCCSUSHDA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD11
C2741 0.1UF 10% 16V X5R 402
ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ARX
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AE7..AJ7
C2711 1UF 10% 6.3V CERM 402
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ATX
1080 mA
(VCC1_5_A Total)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AC1..AC5
C2714 1UF 10% 6.3V CERM 402
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS F1..M7
C2712 0.1UF 10% 16V X5R 402
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
10 mA
=PP1V5_S0_SB_VCCUSBPLL
PLACEMENT NOTE:
PLACE C2715 NEAR PIN D1 OF SB
C2715 0.1UF 10% 16V X5R 402
=PP1V25_S0_SB_DMI
50 mA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AE29
C2739 22UF 20% 6.3V CERM-X5R 805-3
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
1130 mA
=PPVCORE_S0_SB
C2718 0.1UF 10% 16V X5R 402
C2702 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
1 mA
=PP1V05_S0_SB_CPU_IO
C2724 4.7UF 20% 6.3V CERM 603
C2723 0.1UF 10% 16V X5R 402
C2722 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE NEAR PINS AC23,AC24 OF SB
Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.
SB Decoupling
SYNC_MASTER=M75_PVT SYNC_DATE=05/08/2007
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DRAWING NUMBER 051-7492
REV. B
SCALE NONE
SHT 27 OF 109
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RTC Power Sources

Coin-Cell Connector

CRITICAL
J2800
BM02B-ACHKS-GAN-TF-LF-SN-M
M-RT-SM
518S0487

PPVBATT_G3_RTC
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R2800 1K 5% 1/10W MF-LF 402

PPVBATT_G3_RTC_R
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

D2805
BAT54DW
SOT-363
NC NC NC

=PP3V42_G3H_SB_RTC

PP3V3_G3_SB_RTC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R2806 20K 5% 1/10W MF-LF 402

SB_RTC_RST_L

C2806 1UF 10% 6.3V CERM 402

R2805 1M 5% 1/10W MF-LF 402

C2805 1UF 10% 6.3V CERM 402

SB_SM_INTRUDER_L

NOTE: R2800 and D2805 form the double-fault protection for RTC battery.

Platform Reset Connections

Unbuffered

PLT_RST_L
MAKE_BASE=TRUE

R2860 100 5% 1/16W MF-LF 402 — NB_RESET_L
R2861 0 5% 1/16W MF-LF 402 — FW_PLT_RST_L
R2862 100 5% 1/16W MF-LF 402 — SMC_LRESET_L
R2863 0 5% 1/16W MF-LF 402 — DEBUG_RESET_L
R2864 100 5% 1/16W MF-LF 402 — LIO_PLT_RST_L
R2865 0 5% 1/16W MF-LF 402 — ENET_RESET_L
LCDBKLT_PLT_RST_L

SB RTC Crystal

SB_RTC_X1
R2810 0 5% 1/16W MF-LF 402
SB_RTC_X1_R
C2810 12pF 5% 50V CERM 402
R2811 10M 5% 1/16W MF-LF 402
CRITICAL
Y2810 32.768K SM-2 NC NC
C2811 12pF 5% 50V CERM 402
SB_RTC_X2

System Reset "Button"

=PP3V3_S5_SB_PM
R2825 10K 5% 1/16W MF-LF 402
ITP&XDP
R2826 1K 5% 1/10W MF-LF 402
XDP_DBRESET_L
PM_SYSRST_L
OMIT
R2820 0 5% 1/10W MF-LF 603

SILK_PART=SYS_RST
This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Muxed GFX GPU Reset Support

=PP3V3_S0_RSTBUF
C2883 0.1UF 20% 10V CERM 402
CRITICAL
U2883 74LVC2G132 US8
U2883 74LVC2G132 US8 CRITICAL
PM_ALL_GPU_PGOOD
R2885 10K 5% 1/10W MF-LF 402
GPU_PGOOD_RC
RST_L_AND_GPU_PGOOD_L
R2886 24.3K 1% 1/10W MF-LF 402
C2885 0.047UF 10% 10V CERM 402

ON POWER UP:
This delay ensures that GPU clocks run before GPU is released from reset (RC should reach schmitt trigger threshold at approx .8 ms nominal w/ 1K pullup on PM_ALL_GPU_PGOOD)

RST_L_AND_GPU_PGOOD
=PP3V3_S0_RSTBUF
EXTGPU_RST_SW
R2880 0 5% 1/10W MF-LF 402
EXTGPU_RST_L
EXTGPU_RST_QUAL_L
U2880 MC74VHC1G08 SC70
GPU_RESET_R_L
R2881 0 5% 1/10W MF-LF 402
GPU_RESET_L
C2880 0.1UF 10% 10V CERM 402
R2882 1K 5% 1/10W MF-LF 402
GPU_IOENABLE_RC
MAKE_BASE=TRUE
=GPU_DDC_ENABLE
=GPU_HPD_ENABLE
C2882 0.001UF 10% 10V CERM 402
EXTGPU_RST_HW
R2887 0 5% 1/10W MF-LF 402
EXTGPU_PWR_EN

GPU_IOENABLE_RC is used to isolate certain GPU signals from the rest of the system. RC prevents glitch that would otherwise be injected into isolated signals due to sharp reset edge and isolating FET Cgs.

ON POWER DOWN:
This ensures that GPU is put into reset while chip is still powered and clocks are still running.

VRMPWRGD Inverter

=PP3V3_S0_SB_PM
C2830 0.1UF 20% 10V CERM 402
U2830 MC74VHC1G00 SC70-5
VR_PWRGD_CLKEN_L
VR_PWRGD_CLKEN

PWROK Circuit

=PP3V3_S0_SB_PM
C2840 0.1UF 20% 10V CERM 402
U2840 MC74VHC1G08 SC70
VR_PWRGOOD_DELAY
ALL_SYS_PWRGD
PM_SB_PWROK
R2840 10K 5% 1/16W MF-LF 402
R2841 10K 5% 1/10W MF-LF 402

PCI Reset Connections

PCI_RST_L
R2890 100 5% 1/16W MF-LF 402
PCI_FW_RST_L

CPU VCore ForcePSI

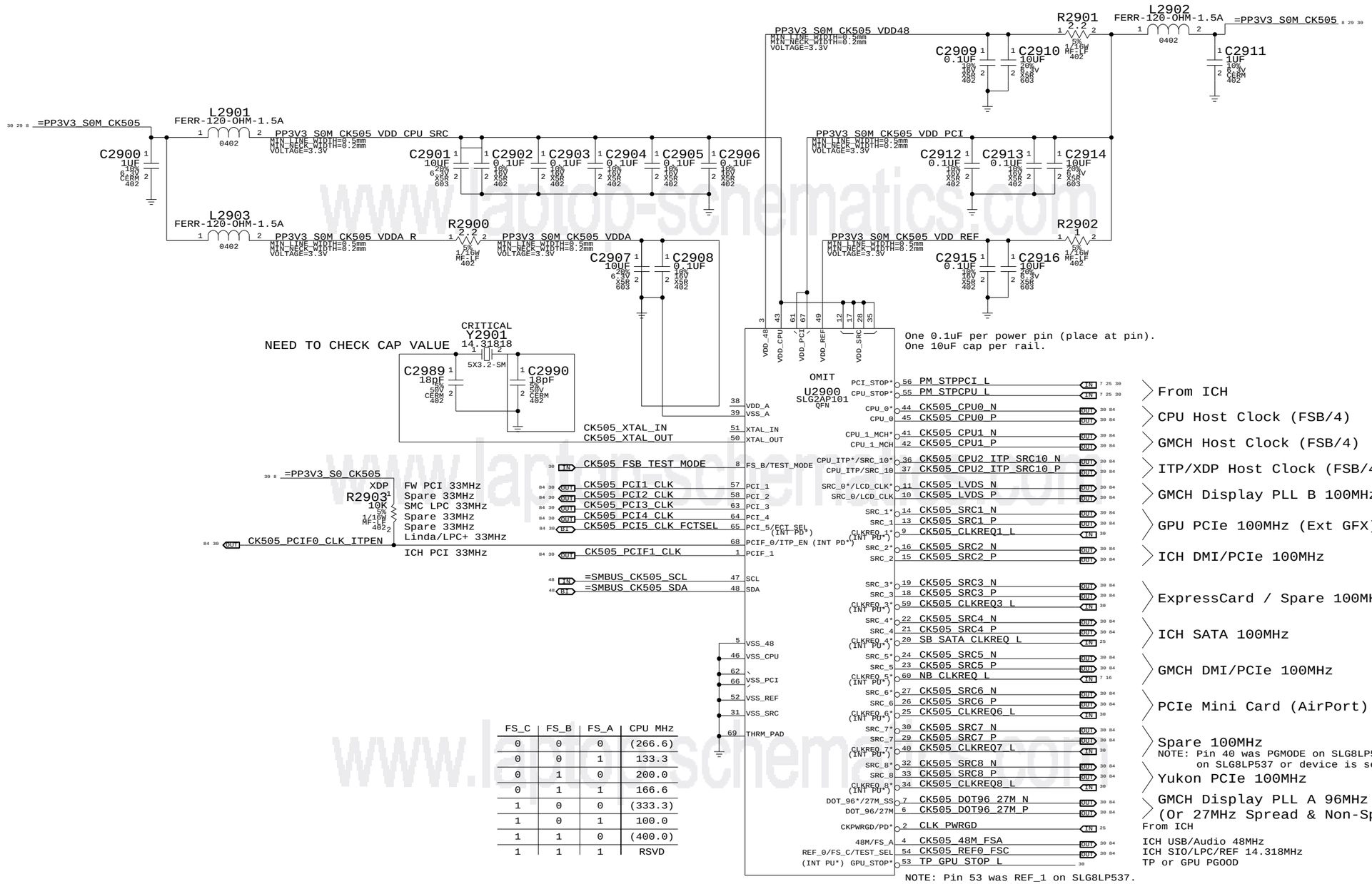
CPU_PSI_L
MAKE_BASE=TRUE
IMVP6_PSI_L

SB Misc

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/24/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 28 OF 109	



FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

Clock (CK505)

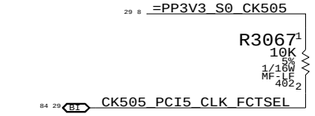
SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

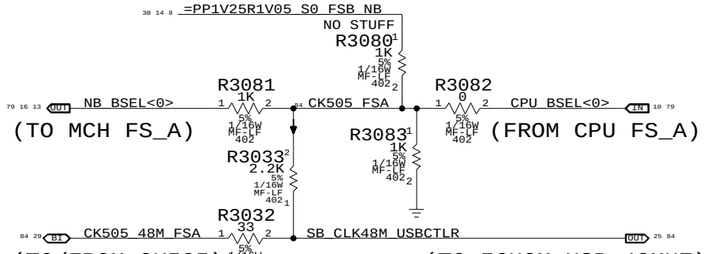
SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 29 OF 109	

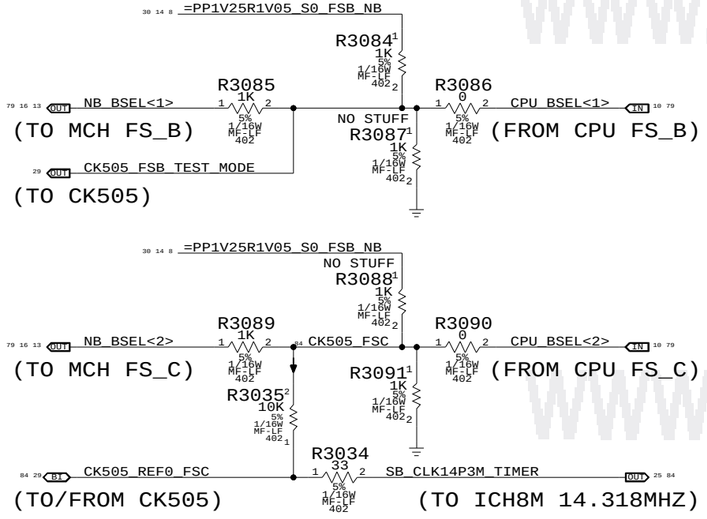
CK505 Configuration Straps

FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)





FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

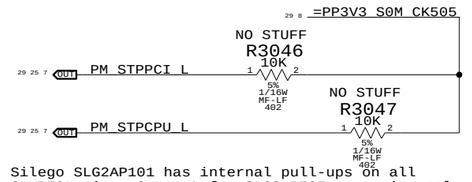
CLK Termination

(Note: HOST/SRC/GFX clock termination removed. Silego SL8GLP536 or equiv. support only)

CK505_CPU0_P	FSB_CLK_CPU_P	(CPU HOST 167/200MHZ)
CK505_CPU0_N	FSB_CLK_CPU_N	
CK505_CPU1_P	FSB_CLK_NB_P	(GMCH HOST 167/200MHZ)
CK505_CPU1_N	FSB_CLK_NB_N	
CK505_CPU2_ITP_SRC10_P	XDP_CLK_P	(ITP HOST 167/200MHZ)
CK505_CPU2_ITP_SRC10_N	XDP_CLK_N	
CK505_LVDS_P	NB_CLK100M_DPLLSS_P	(Int Gfx LVDS 100MHz)
CK505_LVDS_N	NB_CLK100M_DPLLSS_N	
CK505_SRC1_P	PEG_CLK100M_GPU_P	(GPU PCIe 100MHz)
CK505_SRC1_N	PEG_CLK100M_GPU_N	
CK505_SRC2_P	SB_CLK100M_DMI_P	(ICH8M DMI 100MHZ)
CK505_SRC2_N	SB_CLK100M_DMI_N	
CK505_SRC3_P	PCIE_CLK100M_EXCARD_P	(ExpressCard 100MHz)
CK505_SRC3_N	PCIE_CLK100M_EXCARD_N	
CK505_SRC4_P	SB_CLK100M_SATA_P	(ICH8M SATA 100MHZ)
CK505_SRC4_N	SB_CLK100M_SATA_N	
CK505_SRC5_P	NB_CLK100M_PCIE_P	(GMCH PEG/DMI 100MHZ)
CK505_SRC5_N	NB_CLK100M_PCIE_N	
CK505_SRC6_P	PCIE_CLK100M_MINI_P	(WIRELESS PCIe MINI 100MHZ)
CK505_SRC6_N	PCIE_CLK100M_MINI_N	
CK505_SRC7_P	TP_PCIE_CLK100M_SRC7P	(FW 100MHz)
CK505_SRC7_N	TP_PCIE_CLK100M_SRC7N	
CK505_SRC8_P	PCIE_CLK100M_ENET_P	(ENET 100MHZ)
CK505_SRC8_N	PCIE_CLK100M_ENET_N	

CK505_DOT96_27M_P	R3024 33 → GPU_CLK27M	(Ext GFX 27MHz)
CK505_CLK27M		
CK505_DOT96_27M_N	R3025 33 → GPU_CLK27M_SS	(Ext GFX Spread 27MHz)
CK505_CLK27M_SS		
CK505_PCIF0_CLK_ITPEN	R3026 33 → PCI_CLK33M_LPCPLUS	(LINDA/LPC+ LPC 33MHZ)
CK505_PCIF1_CLK	R3027 33 → PCI_CLK33M_SB	(ICH8M PCI 33MHZ)
CK505_PCI1_CLK	R3028 33 → PCI_CLK33M_FW	(FIREWIRE PCI 33MHZ)
CK505_PCI3_CLK	R3030 33 → PCI_CLK33M_SMC	(SMC PCI 33MHZ)

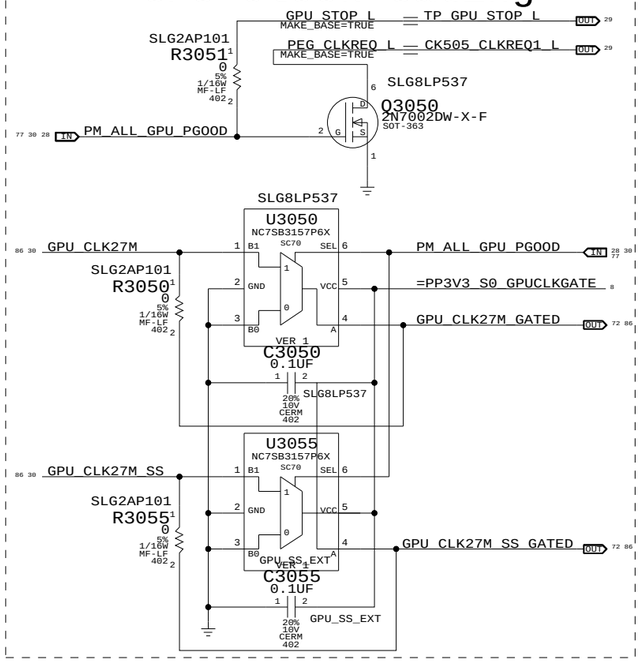
CLKREQ Controls



Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).

EXCARD_CLKREQ_L	CK505_CLKREQ3_L	
MINI_CLKREQ_L	CK505_CLKREQ6_L	
=ENET_CLKREQ_L	ENET_CLKREQ_L	CK505_CLKREQ8_L
TP_CK505_CLKREQ7_L	CK505_CLKREQ7_L	

GPU Clock Gating



Unused Clocks

CK505_PCI2_CLK	TP_CK505_PCI2_CLK	(Reserved for TPM PCI 33MHZ)
CK505_PCI4_CLK	TP_CK505_PCI4_CLK	(Spare 33MHZ)

Clock Termination

SYNC_MASTER=(MASTER) SYNC_DATE=08/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 30 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

"Factory" (thru-hole) slot

=PP0V9_S3M_MEM_DIMMVREFA

C3101 2.2uF 20% 6.3V CERM 603

C3100 0.1uF 20% 10V CERM 402

=PP1V8_S3M_MEM_A

CRITICAL
J3100
F-RT-TH1
DDR2-SODIMM-DUAL

		1B	VREF	VSS0	2B		
		3B	VSS1	DQ4	4B	MEM_A_DQ<9>	17 81
81 17	MEM_A_DQ<14>	5B	DQ0	DQ5	6B	MEM_A_DQ<15>	17 81
81 17	MEM_A_DQ<13>	7B	DQ1	VSS2	8B		
		9B	VSS4	DM0	10B	MEM_A_DM<1>	17 81
81 17	MEM_A_DQS_N<1>	11B	DQS0*	VSS5	12B		
81 17	MEM_A_DQS_P<1>	13B	DQS0	DQ6	14B	MEM_A_DQ<8>	17 81
		15B	VSS6	DQ7	16B	MEM_A_DQ<12>	17 81
81 17	MEM_A_DQ<10>	17B	DQ2	VSS7	18B		
81 17	MEM_A_DQ<11>	19B	DQ3	DQ12	20B	MEM_A_DQ<2>	17 81
		21B	VSS8	DQ13	22B	MEM_A_DQ<3>	17 81
81 17	MEM_A_DQ<7>	23B	DQ8	VSS9	24B		
81 17	MEM_A_DQ<0>	25B	DQ9	DM1	26B	MEM_A_DM<0>	17 81
		27B	VSS10	VSS11	28B		
81 17	MEM_A_DQS_N<0>	29B	DQS1*	CK0	30B	MEM_CLK_P<0>	16 81
81 17	MEM_A_DQS_P<0>	31B	DQS1	CK0*	32B	MEM_CLK_N<0>	16 81
		33B	VSS12	VSS13	34B		
81 17	MEM_A_DQ<6>	35B	DQ10	DQ14	36B	MEM_A_DQ<1>	17 81
81 17	MEM_A_DQ<4>	37B	DQ11	DQ15	38B	MEM_A_DQ<5>	17 81
		39B	VSS14	VSS15	40B		
				KEY			
		41B	VSS16	VSS17	42B		
81 17	MEM_A_DQ<17>	43B	DQ16	DQ20	44B	MEM_A_DQ<18>	17 81
81 17	MEM_A_DQ<21>	45B	DQ17	DQ21	46B	MEM_A_DQ<20>	17 81
		47B	VSS18	VSS19	48B		
81 17	MEM_A_DQS_N<2>	49B	DQS2*	NC0	50B	PM_EXTTS_L<0>	16 45
81 17	MEM_A_DQS_P<2>	51B	DQS2	DM2	52B	MEM_A_DM<2>	17 81
		53B	VSS21	VSS22	54B		
81 17	MEM_A_DQ<23>	55B	DQ18	DQ22	56B	MEM_A_DQ<22>	17 81
81 17	MEM_A_DQ<16>	57B	DQ19	DQ23	58B	MEM_A_DQ<19>	17 81
		59B	VSS23	VSS24	60B		
81 17	MEM_A_DQ<31>	61B	DQ24	DQ28	62B	MEM_A_DQ<26>	17 81
81 17	MEM_A_DQ<27>	63B	DQ25	DQ29	64B	MEM_A_DQ<24>	17 81
		65B	VSS25	VSS26	66B		
81 17	MEM_A_DM<3>	67B	DM3	DQS3*	68B	MEM_A_DQS_N<3>	17 81
	NC	69B	NC1	DQS3	70B	MEM_A_DQS_P<3>	17 81
		71B	VSS27	VSS28	72B		
81 17	MEM_A_DQ<30>	73B	DQ26	DQ30	74B	MEM_A_DQ<25>	17 81
81 17	MEM_A_DQ<28>	75B	DQ27	DQ31	76B	MEM_A_DQ<29>	17 81
		77B	VSS29	VSS30	78B		
81 33 16	MEM_CKE<0>	79B	CKE0	NC/CKE1	80B	MEM_CKE<1>	16 33 81
		81B	VDD0	VDD1	82B		
	NC	83B	NC2	NC/A15	84B	MEM_A_A<15>	9
81 33 17	MEM_A_BS<2>	85B	BA2	NC/A14	86B	MEM_A_A<14>	16 33 81
		87B	VDD2	VDD3	88B		
81 33 17	MEM_A_A<12>	89B	A12	A11	90B	MEM_A_A<11>	17 33 81
81 33 17	MEM_A_A<9>	91B	A9	A7	92B	MEM_A_A<7>	17 33 81
81 33 17	MEM_A_A<8>	93B	A8	A6	94B	MEM_A_A<6>	17 33 81
		95B	VDD4	VDD5	96B		
81 33 17	MEM_A_A<5>	97B	A5	A4	98B	MEM_A_A<4>	17 33 81
81 33 17	MEM_A_A<3>	99B	A3	A2	100B	MEM_A_A<2>	17 33 81
81 33 17	MEM_A_A<1>	101B	A1	A0	102B	MEM_A_A<0>	17 33 81
		103B	VDD6	VDD7	104B		
81 33 17	MEM_A_A<10>	105B	A10/AP	BA1	106B	MEM_A_BS<1>	17 33 81
81 33 17	MEM_A_BS<0>	107B	BA0	RAS*	108B	MEM_A_RAS_L	17 33 81
81 33 17	MEM_A_WE_L	109B	WE*	S0*	110B	MEM_CS_L<0>	16 33 81
		111B	VDD8	VDD9	112B		
81 33 17	MEM_A_CAS_L	113B	CAS*	ODT0	114B	MEM_ODT<0>	16 33 81
81 33 16	MEM_CS_L<1>	115B	NC/S1*	NC/A13	116B	MEM_A_A<13>	17 33 81
		117B	VDD10	VDD11	118B		
81 33 16	MEM_ODT<1>	119B	NC/ODT1	NC3	120B	NC	
		121B	VSS31	VSS32	122B		
81 17	MEM_A_DQ<36>	123B	DQ32	DQ36	124B	MEM_A_DQ<35>	17 81
81 17	MEM_A_DQ<38>	125B	DQ33	DQ37	126B	MEM_A_DQ<39>	17 81
		127B	VSS33	VSS34	128B		
81 17	MEM_A_DQS_N<4>	129B	DQS4*	DM4	130B	MEM_A_DM<4>	17 81
81 17	MEM_A_DQS_P<4>	131B	DQS4	VSS35	132B		
		133B	VSS36	DQ38	134B	MEM_A_DQ<33>	17 81
81 17	MEM_A_DQ<37>	135B	DQ34	DQ39	136B	MEM_A_DQ<32>	17 81
81 17	MEM_A_DQ<34>	137B	DQ35	VSS37	138B		
		139B	VSS38	DQ44	140B	MEM_A_DQ<63>	17 81
81 17	MEM_A_DQ<56>	141B	DQ40	DQ45	142B	MEM_A_DQ<62>	17 81
81 17	MEM_A_DQ<59>	143B	DQ41	VSS39	144B		
		145B	VSS40	DQS5*	146B	MEM_A_DQS_N<7>	17 81
81 17	MEM_A_DM<7>	147B	DM5	DQS5	148B	MEM_A_DQS_P<7>	17 81
		149B	VSS41	VSS42	150B		
81 17	MEM_A_DQ<58>	151B	DQ42	DQ46	152B	MEM_A_DQ<57>	17 81
81 17	MEM_A_DQ<60>	153B	DQ43	DQ47	154B	MEM_A_DQ<61>	17 81
		155B	VSS43	VSS44	156B		
81 17	MEM_A_DQ<51>	157B	DQ48	DQ52	158B	MEM_A_DQ<55>	17 81
81 17	MEM_A_DQ<54>	159B	DQ49	DQ53	160B	MEM_A_DQ<50>	17 81
		161B	VSS45	VSS46	162B		
	NC	163B	NC_TEST	CK1	164B	MEM_CLK_P<1>	16 81
		165B	VSS47	CK1*	166B	MEM_CLK_N<1>	16 81
81 17	MEM_A_DQS_N<6>	167B	DQS6*	VSS48	168B		
81 17	MEM_A_DQS_P<6>	169B	DQS6	DM6	170B	MEM_A_DM<6>	17 81
		171B	VSS49	VSS50	172B		
81 17	MEM_A_DQ<48>	173B	DQ50	DQ54	174B	MEM_A_DQ<49>	17 81
81 17	MEM_A_DQ<53>	175B	DQ51	DQ55	176B	MEM_A_DQ<52>	17 81
		177B	VSS51	VSS52	178B		
81 17	MEM_A_DQ<43>	179B	DQ56	DQ60	180B	MEM_A_DQ<45>	17 81
81 17	MEM_A_DQ<42>	181B	DQ57	DQ61	182B	MEM_A_DQ<40>	17 81
		183B	VSS53	VSS54	184B		
81 17	MEM_A_DM<5>	185B	DM7	DQS7*	186B	MEM_A_DQS_N<5>	17 81
		187B	VSS55	DQS7	188B	MEM_A_DQS_P<5>	17 81
81 17	MEM_A_DQ<46>	189B	DQ58	VSS56	190B		
81 17	MEM_A_DQ<41>	191B	DQ59	DQ62	192B	MEM_A_DQ<44>	17 81
8	=PPSPD_S0M_MEM_A	193B	VSS57	DQ63	194B	MEM_A_DQ<47>	17 81
48	=I2C_SODIMMA_SDA	195B	SDA	VSS58	196B		
48	=I2C_SODIMMA_SCL	197B	SCL	SA0	198B		
		199B	VDDSPD	SA1	200B	ADDR=0xA0(WR)/0xA1(RD)	

516-0140

DDR2 Bypass Caps
(For return current)

=PP1V8_S3M_MEM_A

C3108 10UF 20% 6.3V CERM 603
C3109 10UF 20% 6.3V CERM 603
C3110 1UF 10% 6.3V CERM 402
C3111 1UF 10% 6.3V CERM 402
C3112 1UF 10% 6.3V CERM 402
C3113 1UF 10% 6.3V CERM 402
C3114 1UF 10% 6.3V CERM 402
C3115 1UF 10% 6.3V CERM 402
C3116 1UF 10% 6.3V CERM 402
C3117 1UF 10% 6.3V CERM 402
C3118 1UF 10% 6.3V CERM 402
C3119 1UF 10% 6.3V CERM 402
C3120 1UF 10% 6.3V CERM 402
C3121 1UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 31 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

=PP0V9_S3M_MEM_DIMMVREFB

C3201 2.2uF 20% 6.3V CERM 603

C3200 0.1uF 20% 10V CERM 402

"Expansion" (surface-mount) slot

=PP1V8_S3M_MEM_B

CRITICAL
J3200
F-RT-SM-M9
DDR2-SODIMM-DUAL

		1A	VREF	VSS0	2A		
		3A	VSS1	DQ4	4A	MEM_B_DQ<9>	17 81
81 17	MEM_B_DQ<15>	5A	DQ0	DQ5	6A	MEM_B_DQ<11>	17 81
81 17	MEM_B_DQ<14>	7A	DQ1	VSS2	8A		
		9A	VSS4	DM0	10A	MEM_B_DM<1>	17 81
81 17	MEM_B_DQS_N<1>	11A	DQS0*	VSS5	12A		
81 17	MEM_B_DQS_P<1>	13A	DQS0	DQ6	14A	MEM_B_DQ<12>	17 81
		15A	VSS6	DQ7	16A	MEM_B_DQ<8>	17 81
81 17	MEM_B_DQ<10>	17A	DQ2	VSS7	18A		
81 17	MEM_B_DQ<13>	19A	DQ3	DQ12	20A	MEM_B_DQ<3>	17 81
		21A	VSS8	DQ13	22A	MEM_B_DQ<6>	17 81
81 17	MEM_B_DQ<7>	23A	DQ8	VSS9	24A		
81 17	MEM_B_DQ<2>	25A	DQ9	DM1	26A	MEM_B_DM<0>	17 81
		27A	VSS10	VSS11	28A		
81 17	MEM_B_DQS_N<0>	29A	DQS1*	CK0	30A	MEM_CLK_P<4>	16 81
81 17	MEM_B_DQS_P<0>	31A	DQS1	CK0*	32A	MEM_CLK_N<4>	16 81
		33A	VSS12	VSS13	34A		
81 17	MEM_B_DQ<1>	35A	DQ10	DQ14	36A	MEM_B_DQ<0>	17 81
81 17	MEM_B_DQ<4>	37A	DQ11	DQ15	38A	MEM_B_DQ<5>	17 81
		39A	VSS14	VSS15	40A		
				KEY			
		41A	VSS16	VSS17	42A		
81 17	MEM_B_DQ<21>	43A	DQ16	DQ20	44A	MEM_B_DQ<22>	17 81
81 17	MEM_B_DQ<19>	45A	DQ17	DQ21	46A	MEM_B_DQ<18>	17 81
		47A	VSS18	VSS19	48A		
81 17	MEM_B_DQS_N<2>	49A	DQS2*	NC0	50A	PM_EXTTS_L<1>	16 45
81 17	MEM_B_DQS_P<2>	51A	DQS2	DM2	52A	MEM_B_DM<2>	17 81
		53A	VSS21	VSS22	54A		
81 17	MEM_B_DQ<20>	55A	DQ18	DQ22	56A	MEM_B_DQ<17>	17 81
81 17	MEM_B_DQ<23>	57A	DQ19	DQ23	58A	MEM_B_DQ<16>	17 81
		59A	VSS23	VSS24	60A		
81 17	MEM_B_DQ<29>	61A	DQ24	DQ28	62A	MEM_B_DQ<26>	17 81
81 17	MEM_B_DQ<24>	63A	DQ25	DQ29	64A	MEM_B_DQ<28>	17 81
		65A	VSS25	VSS26	66A		
81 17	MEM_B_DM<3>	67A	DM3	DQS3*	68A	MEM_B_DQS_N<3>	17 81
	NC	69A	NC1	DQS3	70A	MEM_B_DQS_P<3>	17 81
		71A	VSS27	VSS28	72A		
81 17	MEM_B_DQ<27>	73A	DQ26	DQ30	74A	MEM_B_DQ<31>	17 81
81 17	MEM_B_DQ<25>	75A	DQ27	DQ31	76A	MEM_B_DQ<30>	17 81
		77A	VSS29	VSS30	78A		
81 33 16	MEM_CKE<3>	79A	CKE0	NC/CKE1	80A	MEM_CKE<4>	16 33 81
		81A	VDD0	VDD1	82A		
	NC	83A	NC2	NC/A15	84A	MEM_B_A<15>	9
81 33 17	MEM_B_BS<2>	85A	BA2	NC/A14	86A	MEM_B_A<14>	16 33 81
		87A	VDD2	VDD3	88A		
81 33 17	MEM_B_A<12>	89A	A12	A11	90A	MEM_B_A<11>	17 33 81
81 33 17	MEM_B_A<9>	91A	A9	A7	92A	MEM_B_A<7>	17 33 81
81 33 17	MEM_B_A<8>	93A	A8	A6	94A	MEM_B_A<6>	17 33 81
		95A	VDD4	VDD5	96A		
81 33 17	MEM_B_A<5>	97A	A5	A4	98A	MEM_B_A<4>	17 33 81
81 33 17	MEM_B_A<3>	99A	A3	A2	100A	MEM_B_A<2>	17 33 81
81 33 17	MEM_B_A<1>	101A	A1	A0	102A	MEM_B_A<0>	17 33 81
		103A	VDD6	VDD7	104A		
81 33 17	MEM_B_A<10>	105A	A10/AP	BA1	106A	MEM_B_BS<1>	17 33 81
81 33 17	MEM_B_BS<0>	107A	BA0	RAS*	108A	MEM_B_RAS_L	17 33 81
81 33 17	MEM_B_WE_L	109A	WE*	S0*	110A	MEM_CS_L<2>	16 33 81
		111A	VDD8	VDD9	112A		
81 33 17	MEM_B_CAS_L	113A	CAS*	ODT0	114A	MEM_ODT<2>	16 33 81
81 33 16	MEM_CS_L<3>	115A	NC/S1*	NC/A13	116A	MEM_B_A<13>	17 33 81
		117A	VDD10	VDD11	118A		
81 33 16	MEM_ODT<3>	119A	NC/ODT1	NC3	120A	NC	
		121A	VSS31	VSS32	122A		
81 17	MEM_B_DQ<36>	123A	DQ32	DQ36	124A	MEM_B_DQ<32>	17 81
81 17	MEM_B_DQ<33>	125A	DQ33	DQ37	126A	MEM_B_DQ<37>	17 81
		127A	VSS33	VSS34	128A		
81 17	MEM_B_DQS_N<4>	129A	DQS4*	DM4	130A	MEM_B_DM<4>	17 81
81 17	MEM_B_DQS_P<4>	131A	DQS4	VSS35	132A		
		133A	VSS36	DQ38	134A	MEM_B_DQ<38>	17 81
81 17	MEM_B_DQ<34>	135A	DQ34	DQ39	136A	MEM_B_DQ<39>	17 81
81 17	MEM_B_DQ<35>	137A	DQ35	VSS37	138A		
		139A	VSS38	DQ44	140A	MEM_B_DQ<56>	17 81
81 17	MEM_B_DQ<57>	141A	DQ40	DQ45	142A	MEM_B_DQ<59>	17 81
81 17	MEM_B_DQ<60>	143A	DQ41	VSS39	144A		
		145A	VSS40	DQS5*	146A	MEM_B_DQS_N<7>	17 81
81 17	MEM_B_DM<7>	147A	DM5	DQS5	148A	MEM_B_DQS_P<7>	17 81
		149A	VSS41	VSS42	150A		
81 17	MEM_B_DQ<61>	151A	DQ42	DQ46	152A	MEM_B_DQ<63>	17 81
81 17	MEM_B_DQ<62>	153A	DQ43	DQ47	154A	MEM_B_DQ<58>	17 81
		155A	VSS43	VSS44	156A		
81 17	MEM_B_DQ<48>	157A	DQ48	DQ52	158A	MEM_B_DQ<54>	17 81
81 17	MEM_B_DQ<51>	159A	DQ49	DQ53	160A	MEM_B_DQ<53>	17 81
		161A	VSS45	VSS46	162A		
	NC	163A	NC_TEST	CK1	164A	MEM_CLK_P<3>	16 81
		165A	VSS47	CK1*	166A	MEM_CLK_N<3>	16 81
81 17	MEM_B_DQS_N<6>	167A	DQS6*	VSS48	168A		
81 17	MEM_B_DQS_P<6>	169A	DQS6	DM6	170A	MEM_B_DM<6>	17 81
		171A	VSS49	VSS50	172A		
81 17	MEM_B_DQ<50>	173A	DQ50	DQ54	174A	MEM_B_DQ<52>	17 81
81 17	MEM_B_DQ<55>	175A	DQ51	DQ55	176A	MEM_B_DQ<49>	17 81
		177A	VSS51	VSS52	178A		
81 17	MEM_B_DQ<40>	179A	DQ56	DQ60	180A	MEM_B_DQ<46>	17 81
81 17	MEM_B_DQ<47>	181A	DQ57	DQ61	182A	MEM_B_DQ<43>	17 81
		183A	VSS53	VSS54	184A		
81 17	MEM_B_DM<5>	185A	DM7	DQS7*	186A	MEM_B_DQS_N<5>	17 81
		187A	VSS55	DQS7	188A	MEM_B_DQS_P<5>	17 81
81 17	MEM_B_DQ<42>	189A	DQ58	VSS56	190A		
81 17	MEM_B_DQ<45>	191A	DQ59	DQ62	192A	MEM_B_DQ<41>	17 81
32 8	=PPSPD_S0M_MEM_B	193A	VSS57	DQ63	194A	MEM_B_DQ<44>	17 81
48	=I2C_SODIMMB_SDA	195A	SDA	VSS58	196A		
48	=I2C_SODIMMB_SCL	197A	SCL	SA0	198A		
		199A	VDDSPD	SA1	200A	SODIMM_B_SA1	

202 204 516S0471

203 201

ADDR=0xA4(WR)/0xA5(RD)

=PPSPD_S0M_MEM_B 8 32

R3200 10K 5% 1/16W MF-LF 402

Resistor prevents pwr-gnd short

DDR2 Bypass Caps

(For return current)

=PP1V8_S3M_MEM_B 87 32 8

C3208 10UF 20% 6.3V X5R 603

C3209 10UF 20% 6.3V X5R 603

C3210 1UF 10% 6.3V CERM 402

C3211 0.1UF 20% 10V CERM 402

C3212 1UF 10% 6.3V CERM 402

C3213 1UF 10% 6.3V CERM 402

C3214 1UF 10% 6.3V CERM 402

C3215 1UF 10% 6.3V CERM 402

C3216 1UF 10% 6.3V CERM 402

C3217 0.1UF 20% 10V CERM 402

C3218 0.1UF 20% 10V CERM 402

C3219 0.1UF 20% 10V CERM 402

C3220 0.1UF 20% 10V CERM 402

C3221 0.1UF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

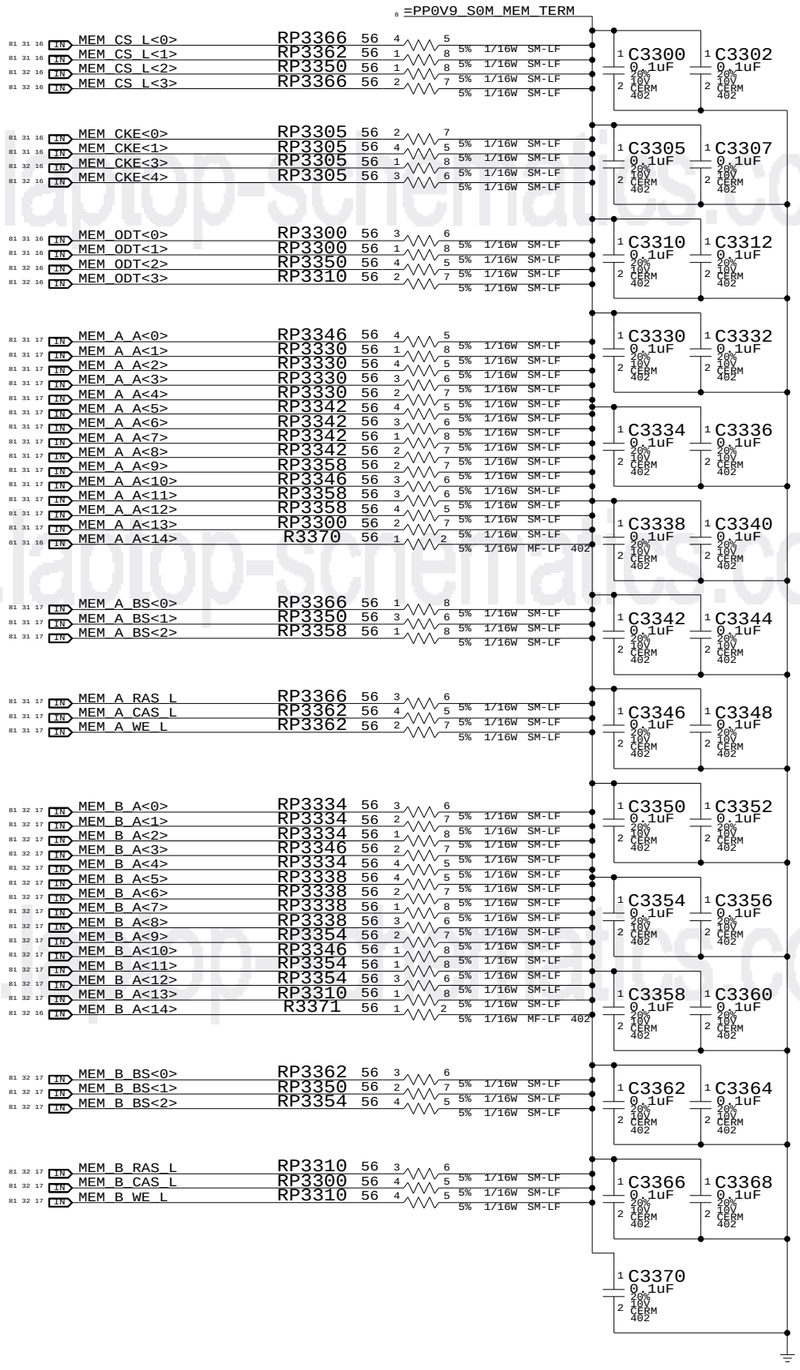
SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 32 OF 109	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

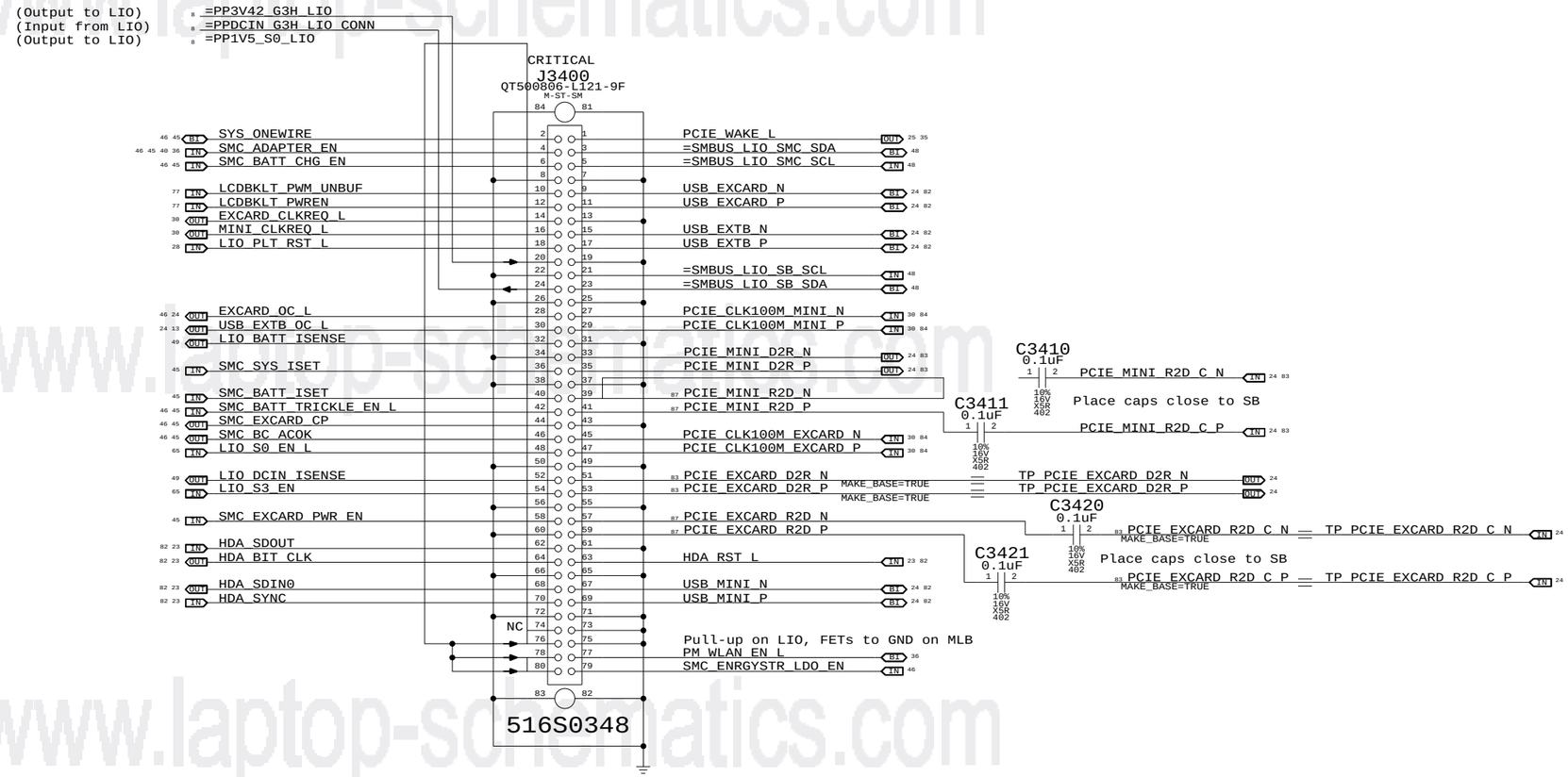
SYNC_MASTER=(T9_NOME) SYNC_DATE=11/14/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	33	109

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 34 OF 109	

Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

=PP1V2_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	171 mA	No link:	130 mA
10 Mbps:	179 mA	10 Mbps:	130 mA
100 Mbps:	203 mA	100 Mbps:	150 mA
1000 Mbps:	426 mA	1000 Mbps:	290 mA

C3700 4.7UF 20% 6.3V CERM 603; C3701–C3708 0.1UF 10% 16V X5R 402 (C3707, C3708: 0.001UF 10% 50V CERM 402)

=PP3V3_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	4 mA	No link:	60 mA
10 Mbps:	4 mA	10 Mbps:	70 mA
100 Mbps:	4 mA	100 Mbps:	70 mA
1000 Mbps:	4 mA	1000 Mbps:	80 mA

C3710 4.7UF 20% 6.3V CERM 603; C3711–C3715 0.1UF 10% 16V X5R 402 (C3714, C3715: 0.001UF 10% 50V CERM 402)

=PP1V8R2V5_ENET_PHY — L3720 FERR-120-OHM-1.5A 0402 — PP1V8R2V5_ENET_PHY_AVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

Yukon EC (2.5V)		Yukon Ultra (1.8V)	
No link:	82 mA	No link:	0 mA
10 Mbps:	108 mA	10 Mbps:	30 mA
100 Mbps:	126 mA	100 Mbps:	40 mA
1000 Mbps:	218 mA	1000 Mbps:	150 mA

(EC:2.5V)

C3720 4.7UF 20% 6.3V CERM 603; C3721–C3724 0.1UF 10% 16V X5R 402 (C3724: 0.001UF 10% 50V CERM 402)

=YUKON_EC_PP2V5_ENET
Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
Yukon Ultra: Alias to GND

PCIE_ENET_D2R_P
PCIE_ENET_D2R_N
PCIE_ENET_R2D_C_P — C3730 0.1UF 10% 16V X5R 402 — PLACEMENT_NOTE=Place C3730 close to southbridge.
PCIE_ENET_R2D_C_N — C3731 0.1UF 10% 16V X5R 402 — PLACEMENT_NOTE=Place C3731 close to southbridge.
C3735 0.1UF 10% 16V X5R 402
C3736 0.1UF 10% 16V X5R 402
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
Yukon EC: Pin 42 should be NC (or TP) net.
=ENET_CLKREQ_L
PCIE_WAKE_L
ENET_RESET_L
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

R3740 R3741 R3742 R3743 R3744 R3745 R3746 R3747: 49.9 1% 1/16W MF-LF 402; SIGNAL_MODEL=EMPTY
ENET_MDI0 — C3740 0.001UF 10% 50V CERM 402
ENET_MDI1 — C3742 0.001UF 10% 50V CERM 402
ENET_MDI2 — C3744 0.001UF 10% 50V CERM 402
ENET_MDI3 — C3746 0.001UF 10% 50V CERM 402

ENET_CLK25M_XTALI
ENET_CLK25M_XTALO

U3700 88E8058 QFN — CRITICAL — OMIT

Pin	Signal
32, 51, 52, 57, 64	NC
19, 22, 23, 28	AVDD0–AVDD3 (EC:AVDD 2.5V)
1, 40, 45, 61	VDDO_TTL0–VDDO_TTL3
8	AVDDH
2, 7, 13, 33, 39, 44, 48, 58	VDD0–VDD7
49	TX_P ← PCIE_ENET_D2R_C_P
50	TX_N ← PCIE_ENET_D2R_C_N
54	RX_P ← PCIE_ENET_R2D_P
53	RX_N ← PCIE_ENET_R2D_N
55	REFCLKP ← PCIE_CLK100M_ENET_P
56	REFCLKN ← PCIE_CLK100M_ENET_N
42	CLKREQ* EC:NO CONNECT ← =ENET_CLKREQ_L
6	WAKE* ← PCIE_WAKE_L
5	PERST* ← ENET_RESET_L
17	MDIP0 ↔ ENET_MDI_P<0>
18	MDIN0 ↔ ENET_MDI_N<0>
20	MDIP1 ↔ ENET_MDI_P<1>
21	MDIN1 ↔ ENET_MDI_N<1>
26	MDIP2 ↔ ENET_MDI_P<2>
27	MDIN2 ↔ ENET_MDI_N<2>
30	MDIP3 ↔ ENET_MDI_P<3>
31	MDIN3 ↔ ENET_MDI_N<3>
15	XTALI ← ENET_CLK25M_XTALI
14	XTALO → ENET_CLK25M_XTALO
65	THRML_PAD

PCI EXPRESS; ANALOG; LED; SPI; MEDIA; TWSI; TEST/RSVD; MAIN CLK

Pin	Signal
10	LOM_DISABLE* ← ENET_LOM_DIS_L
12	VAUX_AVLBL
9	SWITCH_VAUX NC
47	VMAIN_AVLBL ← =ENET_VMAIN_AVLBL
11	SWITCH_VCC NC
4	EC:CTRL25 CTRL18 → TP_YUKON_CTRL18
3	CTRL12 → TP_YUKON_CTRL12
16	RSET ← YUKON_RSET
59	LED_ACT* NC
60	LED_LINK10/100* NC
62	LED_LINK1000* NC
63	LED_DUPLEX* NC
34	(IPU) SPI_DO NC
35	(IPU) SPI_DI NC
37	(IPU) SPI_CLK NC
36	(IPU) SPI_CS NC
38	(IPU) VPD_CLK ↔ YUKON_VPD_CLK
41	(IPU) VPD_DATA ↔ YUKON_VPD_DATA
46	(IPD) TESTMODE
24	RSVD_24 NC
25	RSVD_25 NC
29	RSVD_29 NC
43	RSVD_43 NC

R3760 4.7K 5% 1/10W MF-LF 402
Must be high in S0 state (can use PP3V3_S0 as input)
YUKON_ULTRA R3765 4.99K 1% 1/16W MF-LF 402

VPD ROM — U3780 M24C08 SO8 — CRITICAL
C3780 0.1UF 10% 16V X5R 402
R3780 4.7K 5% 1/10W MF-LF 402
R3781 4.7K 5% 1/16W MF-LF 402
E2, NC1, NC0, WC*, VCC, VSS, SDA, SCL

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONs to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

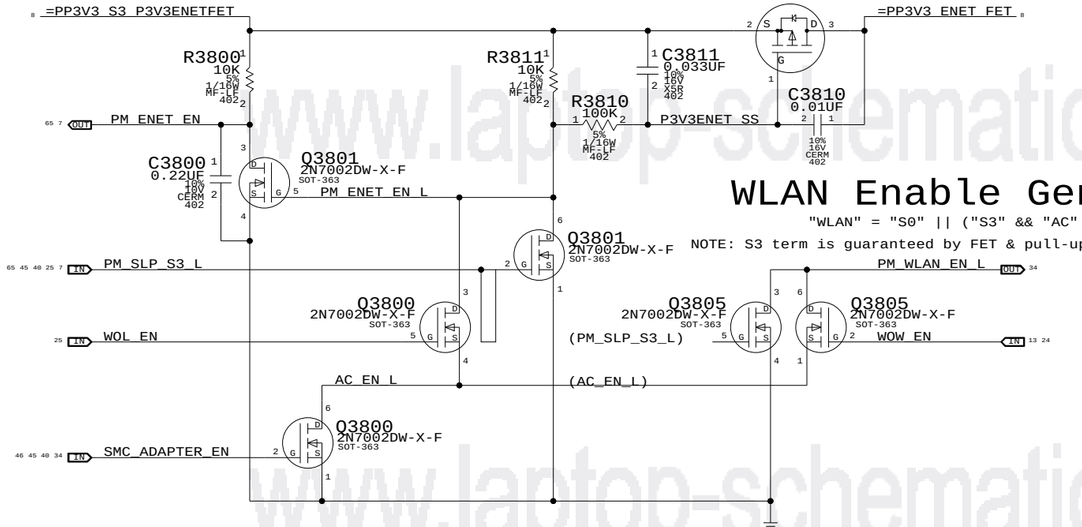
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 37 OF 109	

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.



3.3V ENET FET

WLAN Enable Generation

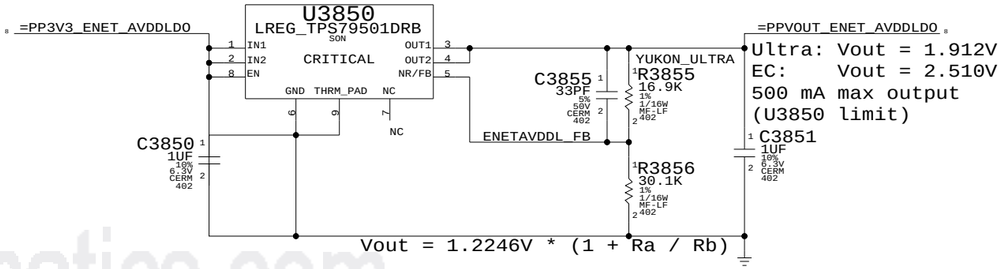
"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")

NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

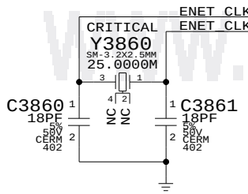
Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



Yukon Crystal



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

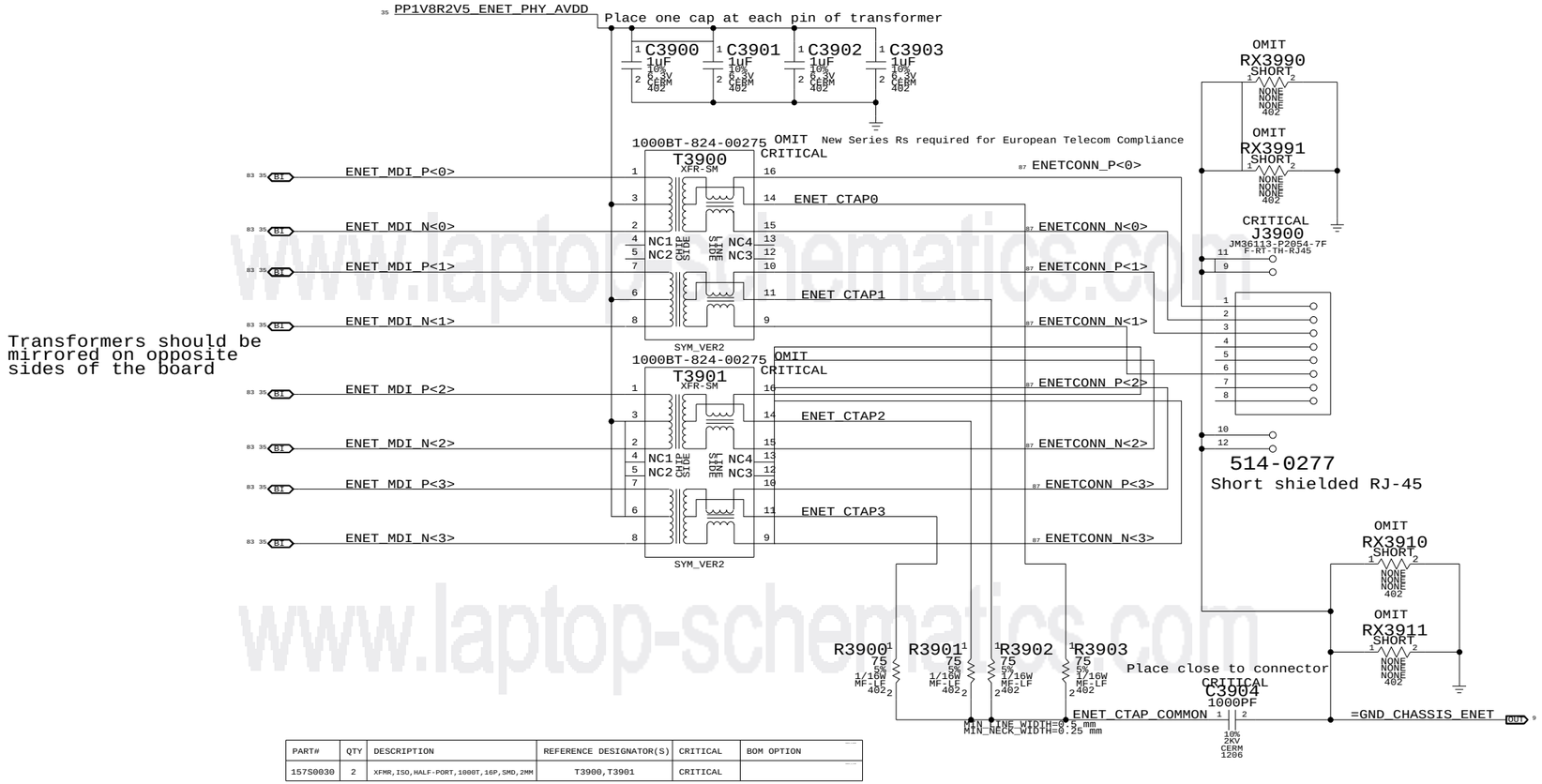
SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 38 OF 109	

Page Notes

Power aliases required by this page:
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Transformers should be mirrored on opposite sides of the board

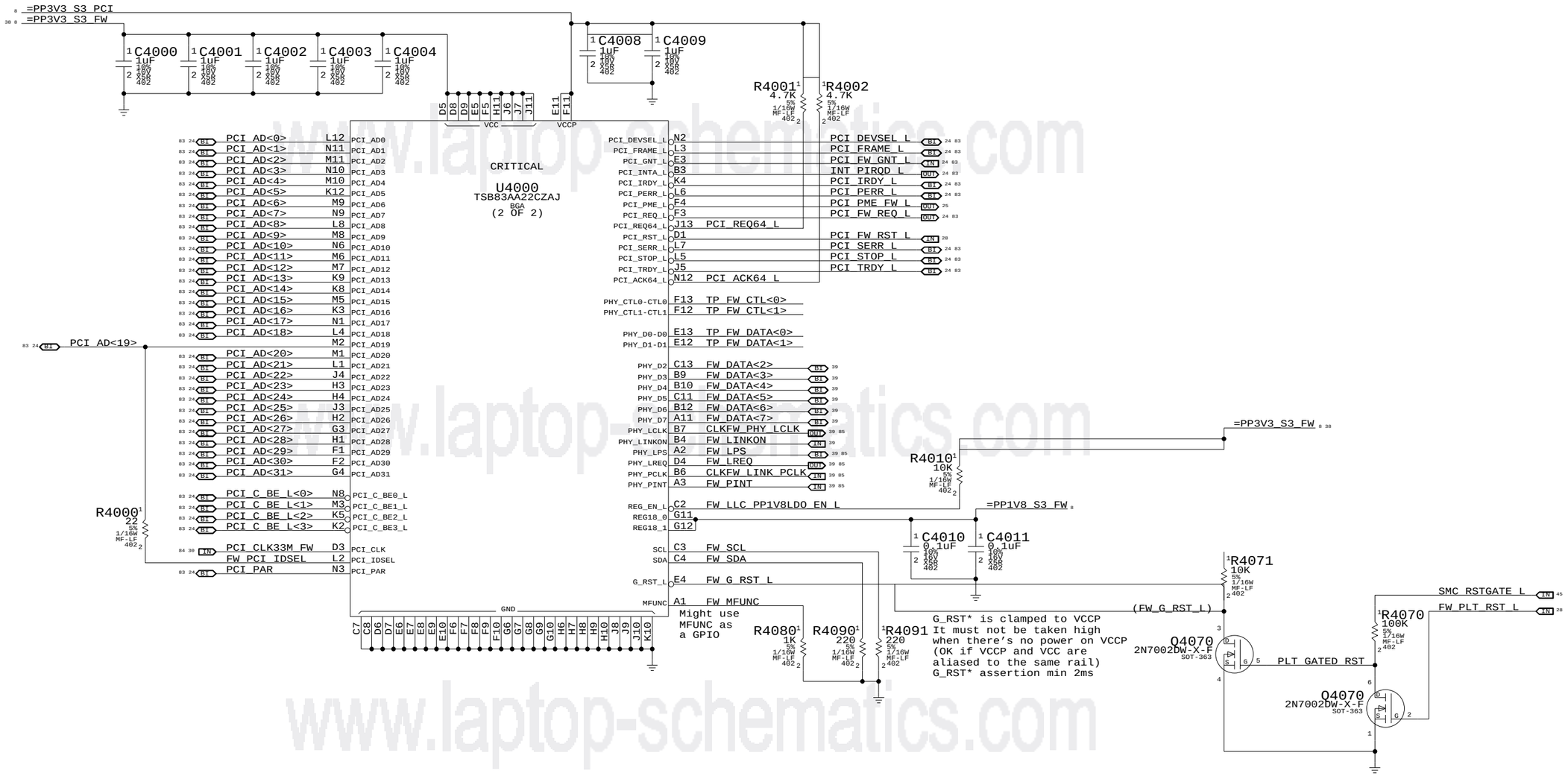
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
157S0030	2	XFMR,ISO,HALF-PORT,1000T,16P,SMD,2MM	T3900,T3901	CRITICAL	

Ethernet Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 39 OF 109	

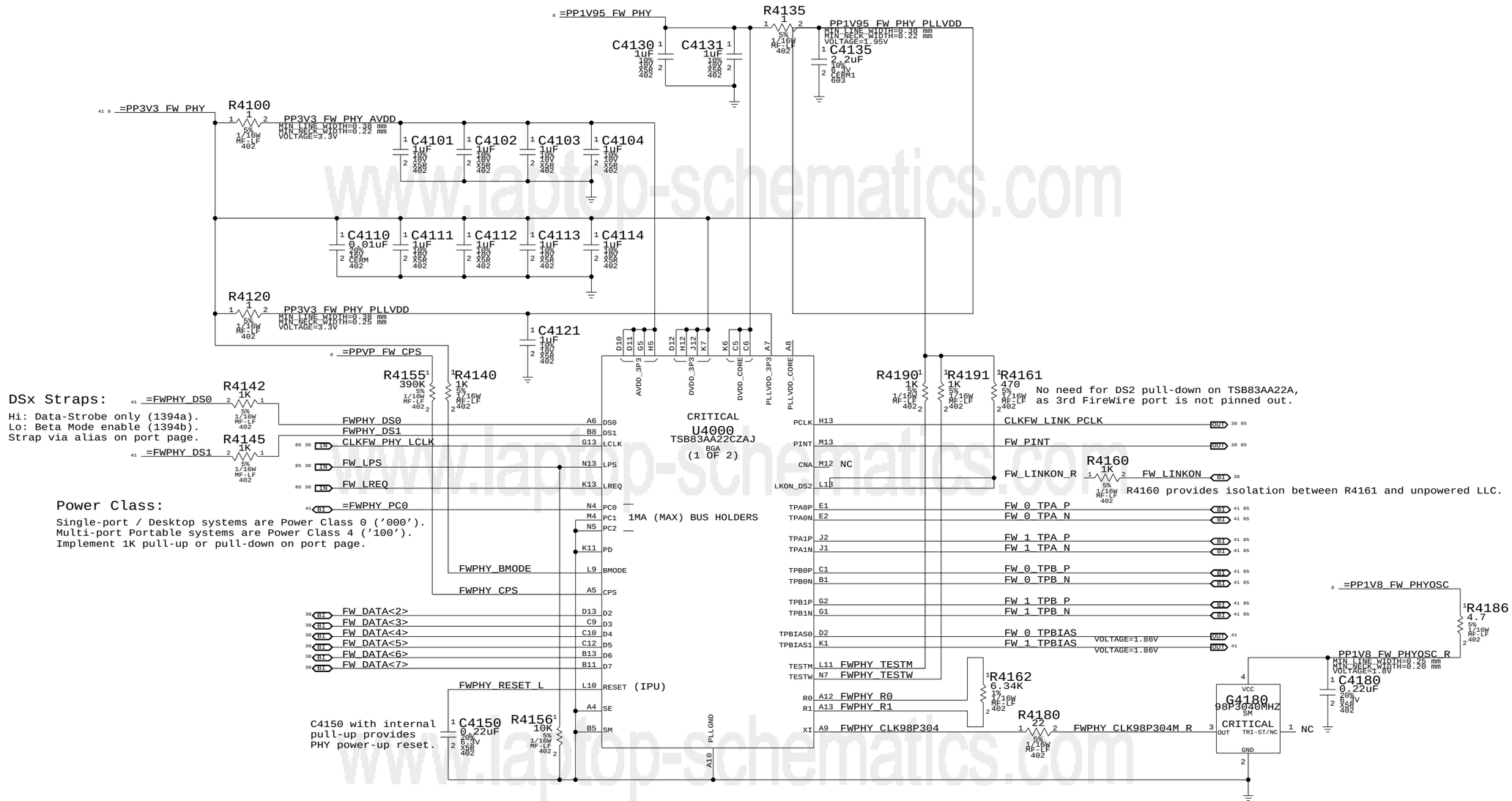


FireWire Link (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 40 OF 109	



FireWire PHY (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 41 OF 109	

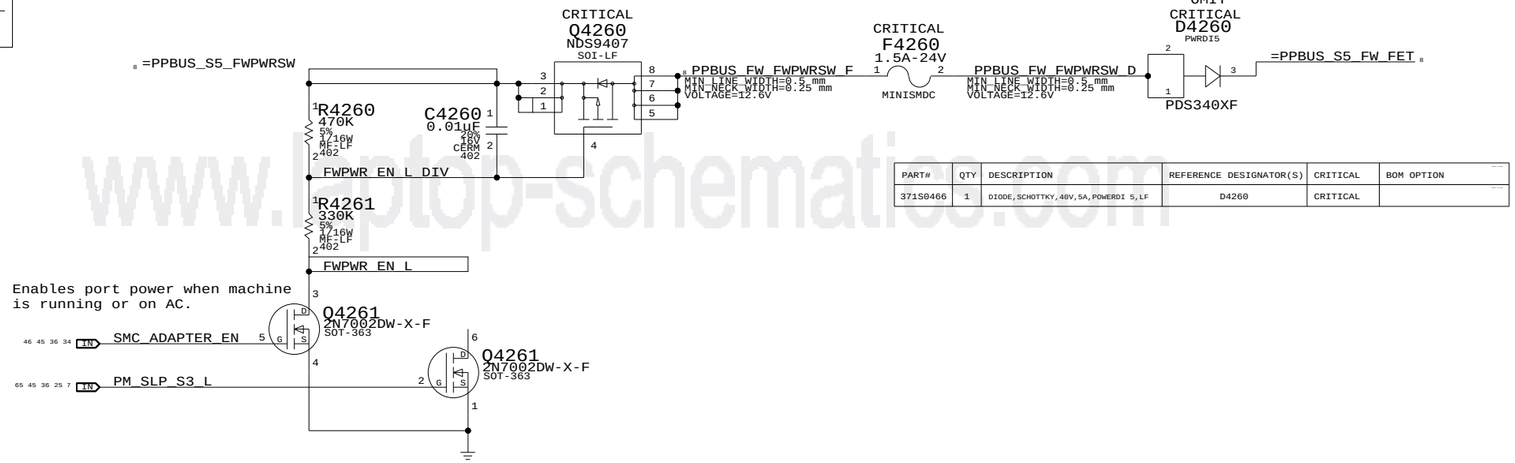
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

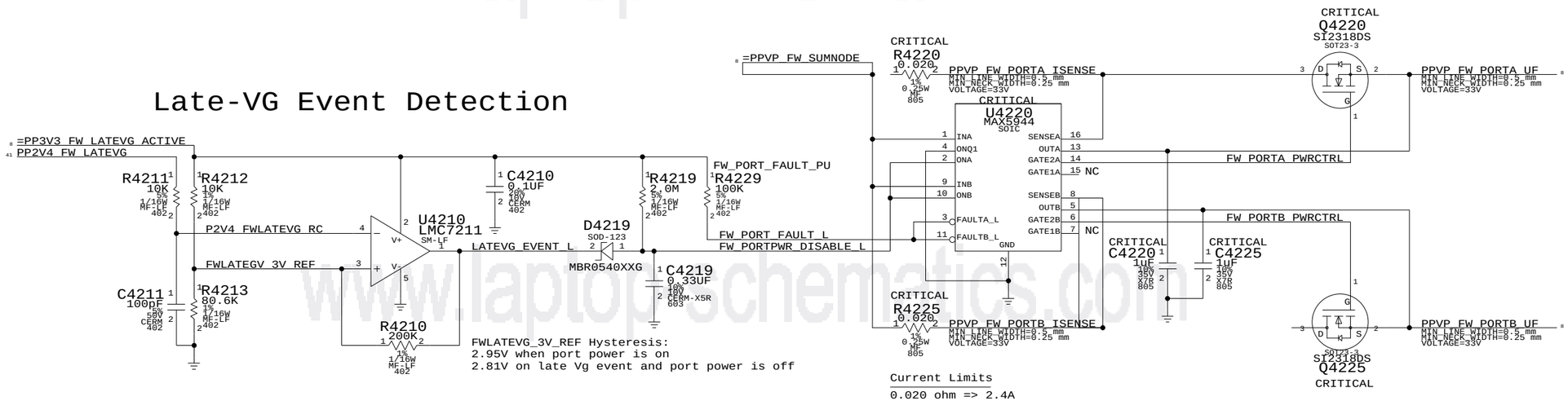
BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
371S0466	1	DIODE,SCHOTTKY,40V,5A,POWERDI 5,LF	D4260	CRITICAL	

Current Limit/Active Late-VG Protection



Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

Late-VG Event Detection

FireWire Port Power

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE	SHT 42 OF 109	
NONE		

Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT0
- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG
- =GND_CHASSIS_FW_PORT0L
- =GND_CHASSIS_FW_PORT0U
- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:
- 2-port Portable Power Class (4)
- Port "0" Data-Strobe only (1394A)
- Port "1" Bilingual (1394B)

39 8 =PP3V3_FW_PHY
39 =FWPHY_PC0
39 =FWPHY_DS0
39 =FWPHY_DS1

Termination

Place close to FireWire PHY

39 FW_1_TPBIAS
39 FW_0_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4350 1uF 10% 6.3V CERM 402
C4360 1uF 10% 6.3V CERM 402

CRITICAL L4360 18NH-250MA 0402 FW_B_TPA_L_P
CRITICAL L4361 18NH-250MA 0402 FW_B_TPA_L_N

R4350 56.2 1% 1/16W MF-LF 402
R4351 56.2 1% 1/16W MF-LF 402
R4360 56.2 1% 1/16W MF-LF 402
R4361 56.2 1% 1/16W MF-LF 402

85 39 FW_0_TPA_P — FW_PORT0_TPA_P 41 MAKE_BASE=TRUE
85 39 FW_0_TPA_N — FW_PORT0_TPA_N 41 MAKE_BASE=TRUE
85 39 FW_0_TPB_P — FW_PORT0_TPB_P 41 MAKE_BASE=TRUE
85 39 FW_0_TPB_N — FW_PORT0_TPB_N 41 MAKE_BASE=TRUE
85 39 FW_1_TPA_P — FW_PORT1_TPA_P 41 MAKE_BASE=TRUE
85 39 FW_1_TPA_N — FW_PORT1_TPA_N 41 MAKE_BASE=TRUE
85 39 FW_1_TPB_P — FW_PORT1_TPB_P 41 MAKE_BASE=TRUE
85 39 FW_1_TPB_N — FW_PORT1_TPB_N 41 MAKE_BASE=TRUE

SIGNAL_MODEL=EMPTY
R4352 56.2 1% 1/16W MF-LF 402
R4353 56.2 1% 1/16W MF-LF 402
R4362 56.2 1% 1/16W MF-LF 402
R4363 56.2 1% 1/16W MF-LF 402

FW_B_TPB_L_N
FW_B_TPB_L_P

CRITICAL L4362 18NH-250MA 0402 SIGNAL_MODEL=EMPTY FW_PORT1_TPB_C
CRITICAL L4363 18NH-250MA 0402 SIGNAL_MODEL=EMPTY

FW_PORT0_TPB_C

C4354 220pF 5% 25V CERM 402
R4354 4.99K 1% 1/16W MF-LF 402
C4364 220pF 5% 25V CERM 402
R4364 4.99K 1% 1/16W MF-LF 402

Late-VG Protection Power

8 =PP3V3_FW_LATEVG
R4390 332 1% 1/16W MF-LF 402
PP2V4_FW_LATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V 40 41
CRITICAL D4390 MMBZ5227B SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

Cable Power

CRITICAL Note: Trace PPVP_FW_PORT0 must handle up to 5A

"Snapback" & "Late VG" Protection

8 =PPVP_FW_PORT0
CRITICAL L4300 FERR-250-OHM SM
PPVP_FW_PORT0 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V
C4304 0.001uF 20% 50V CERM 402

41 40 PP2V4_FW_LATEVG

DP4300 BAV99DW-X-F SOT-363
C4300 0.01uF 10% 50V X7R 402
C4301 0.01uF 10% 50V X7R 402

41 FW_PORT0_TPA_P
41 FW_PORT0_TPA_N
41 FW_PORT0_TPB_P
41 FW_PORT0_TPB_N

CRITICAL FL4300 90-OHM-100MA 1210-4SM1
CRITICAL FL4301 90-OHM-100MA 1210-4SM1

87 FW_PORT0_TPA_FL_P
87 FW_PORT0_TPA_FL_N
87 FW_PORT0_TPB_FL_P
87 FW_PORT0_TPB_FL_N

(PPFW_PORT0_VP)
(GND_FW_PORT0_VG)

DP4301 BAV99DW-X-F SOT-363
C4302 0.01uF 10% 50V X7R 402
C4303 0.01uF 10% 50V X7R 402

C4305 0.01uF 20% 50V CERM 603

41 9 =GND_CHASSIS_FW_PORT0L
OMIT CX4300 SHORT NONE NONE NONE 402
OMIT CX4301 SHORT NONE NONE NONE 402

PORT 0
1394A

CRITICAL J4300 1394A F-RT-TH-LF
6 TPO (TPA+)
5 TPO# (TPA-)
4 TPI (TPB+)
3 TPI# (TPB-)
1 VP
2 VGND
7 8 9 10
514-0255

=GND_CHASSIS_FW_PORT0L
=GND_CHASSIS_FW_PORT0U
OMIT CX4302 SHORT NONE NONE NONE 402
OMIT CX4303 SHORT NONE NONE NONE 402

Cable Power

CRITICAL Note: Trace PPVP_FW_PORT1 must handle up to 5A

"Snapback" & "Late VG" Protection

8 =PPVP_FW_PORT1
CRITICAL L4310 FERR-250-OHM SM
PPVP_FW_PORT1 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V
C4314 0.001uF 20% 50V CERM 402

41 40 PP2V4_FW_LATEVG

DP4310 BAV99DW-X-F SOT-363
C4311 0.01uF 10% 50V X7R 402
C4310 0.01uF 10% 50V X7R 402

41 FW_PORT1_TPB_N
41 FW_PORT1_TPB_P
41 FW_PORT1_TPA_N
41 FW_PORT1_TPA_P

DP4311 BAV99DW-X-F SOT-363
C4312 0.01uF 10% 50V X7R 402
C4313 0.01uF 10% 50V X7R 402

C4319 0.1uF 10% 50V X7R 603-1
R4319 1M 5% 1/16W MF-LF 402

NO STUFF
C4317 0.01uF 20% 16V CERM 402
C4315 0.01uF 20% 50V CERM 603

(FW_PORT1_BREF)
(PPVP_FW_PORT1)
(GND_FW_PORT1_VG)
FW_PORT1_AREF

41 9 =GND_CHASSIS_FW_PORT1
OMIT CX4304 SHORT NONE NONE NONE 402
OMIT CX4305 SHORT NONE NONE NONE 402

PORT 1
BILINGUAL

CRITICAL J4310 1394B-UG31903 F-RT-SM1
10
1 TPB- 9 TPB<R> OUTPUT
2 TPB+ 8 VP
NC 7 NC
6 VG 3 TPA- 5 TPA<R> INPUT 4 TPA+
11
514S0133

=GND_CHASSIS_FW_PORT1
OMIT CX4306 SHORT NONE NONE NONE 402
OMIT CX4307 SHORT NONE NONE NONE 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

FireWire Ports

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 43 OF 109	

IDE (ODD) Connector

=PP3V3_S0_IDE

CRITICAL
Q4420
FDC606P
SOT-6

PP5V_ODD
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=5V

=PP5V_S0_ODD

R4420 10K 5% 1/16W MF-LF 402

C4422 0.068UF 10% 10V CERM 402

C4421 0.01UF 10% 16V CERM 402

R4421 47K 5% 1/16W MF-LF 402

P5VODD_SS

R4402 4.7K 5% 1/16W MF-LF 402

=PP5V_S0_ODDPWREN

R4422 100K 5% 1/16W MF-LF 402

R4410 33K 5% 1/16W MF-LF 402

P5VODD_EN_L

ODD_PWR_EN

Q4421
2N7002DW-X-F
SOT-363

Q4421
2N7002DW-X-F
SOT-363

24 IN ODD_PWR_EN_L

(UATA_STOP)
(UATA_HSTROBE)

(UATA_CS0*)

(ODD has internal 100K pull-up to 5V)

CRITICAL
J4400
M-ST-SM1-LF

42 ODD_RST_BUF_L

82 23 BI	IDE_PDD<7>	IDE_PDD<8>	BI 23 82
82 23 BI	IDE_PDD<6>	IDE_PDD<9>	BI 23 82
82 23 BI	IDE_PDD<5>	IDE_PDD<10>	BI 23 82
		IDE_PDD<11>	BI 23 82
82 23 BI	IDE_PDD<4>	IDE_PDD<12>	BI 23 82
82 23 BI	IDE_PDD<3>	IDE_PDD<13>	BI 23 82
82 23 BI	IDE_PDD<2>	IDE_PDD<14>	BI 23 82
82 23 BI	IDE_PDD<1>	IDE_PDD<15>	BI 23 82
82 23 BI	IDE_PDD<0>	IDE_PDDREQ	IN 23 82 (SB has internal pulldown 5.7k-23.5k)
82 23 OUT	IDE_PDIOW_L	IDE_PDIORDY	IN 23 82 (UATA_DSTROBE)
82 23 IN	IDE_PDIOR_L	IDE_IRQ14	OUT 23 82
82 23 OUT	IDE_PDDACK_L	IDE_PDA<0>	IN 23 82
82 23 IN	IDE_PDA<1>	IDE_PDCS3_L	IN 23 82 (UATA_CS1*)
82 23 IN	IDE_PDCS1_L	NC	
82 23 IN	IDE_PDA<2>		

Indicates disk presence
SMC_ODD_DETECT OUT 45

516S0335

R4403 6.2K 5% 1/16W MF-LF 402

=PP5V_S0_PCIREQFIX

R4430 100K 5% 1/16W MF-LF 402

MC74VHC1G09 SC70
U4430

82 24 IN ODD_RST_5VTOL_L

ODD_RST_BUF_L 42

Unused SATA Ports

82 23 IN	SATA_B_R2D_C_P	TP_SATA_B_R2DP MAKE_BASE=TRUE
82 23 IN	SATA_B_R2D_C_N	TP_SATA_B_R2DN MAKE_BASE=TRUE
82 23 OUT	SATA_B_D2R_P	TP_SATA_B_D2RP MAKE_BASE=TRUE
82 23 OUT	SATA_B_D2R_N	TP_SATA_B_D2RN MAKE_BASE=TRUE
82 22 IN	SATA_C_R2D_C_P	TP_SATA_C_R2DP MAKE_BASE=TRUE
82 23 IN	SATA_C_R2D_C_N	TP_SATA_C_R2DN MAKE_BASE=TRUE
82 23 OUT	SATA_C_D2R_P	TP_SATA_C_D2RP MAKE_BASE=TRUE
82 23 OUT	SATA_C_D2R_N	TP_SATA_C_D2RN MAKE_BASE=TRUE

23 BI SATA_RBIAS_P
23 BI SATA_RBIAS_N
SATA_RBIAS MAKE_BASE=TRUE

R4460 24.9 1% 1/16W MF-LF 402

Placement note
Place within 12.7mm
from ball of SB

PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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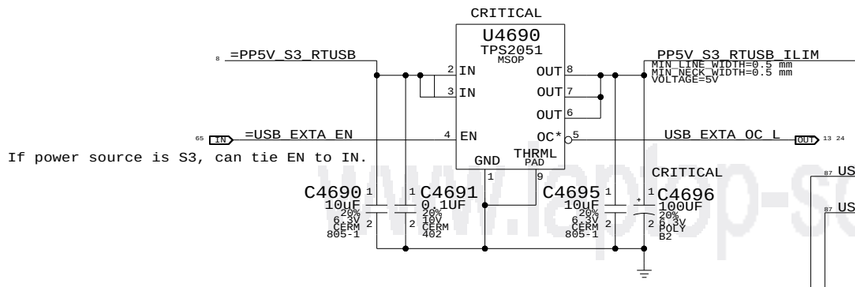
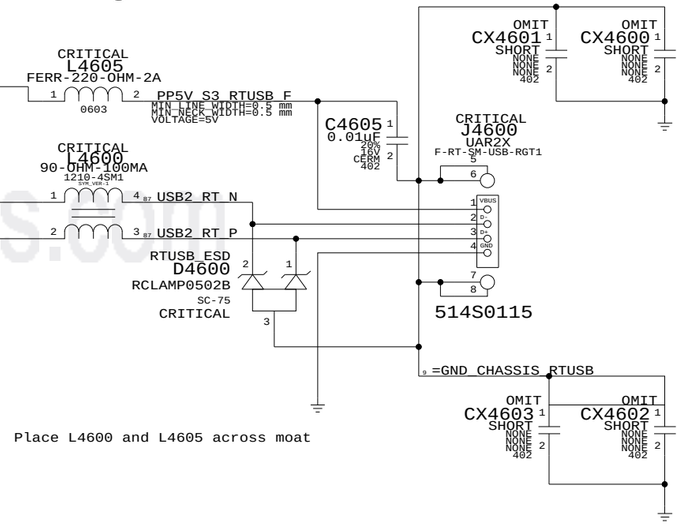
SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 44 OF 109	

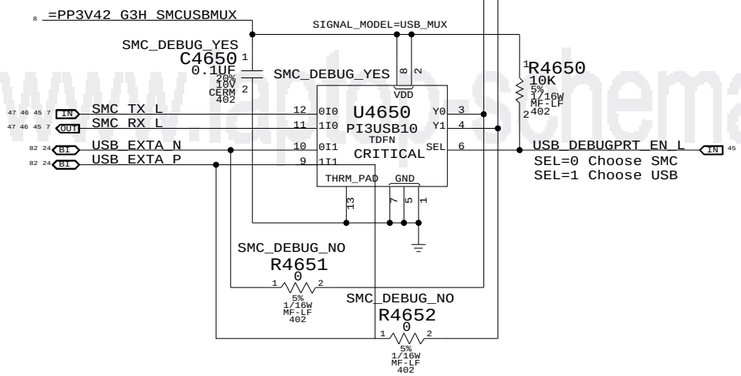
Port Power Switch



Right USB Port



USB/SMC Debug Mux



External USB Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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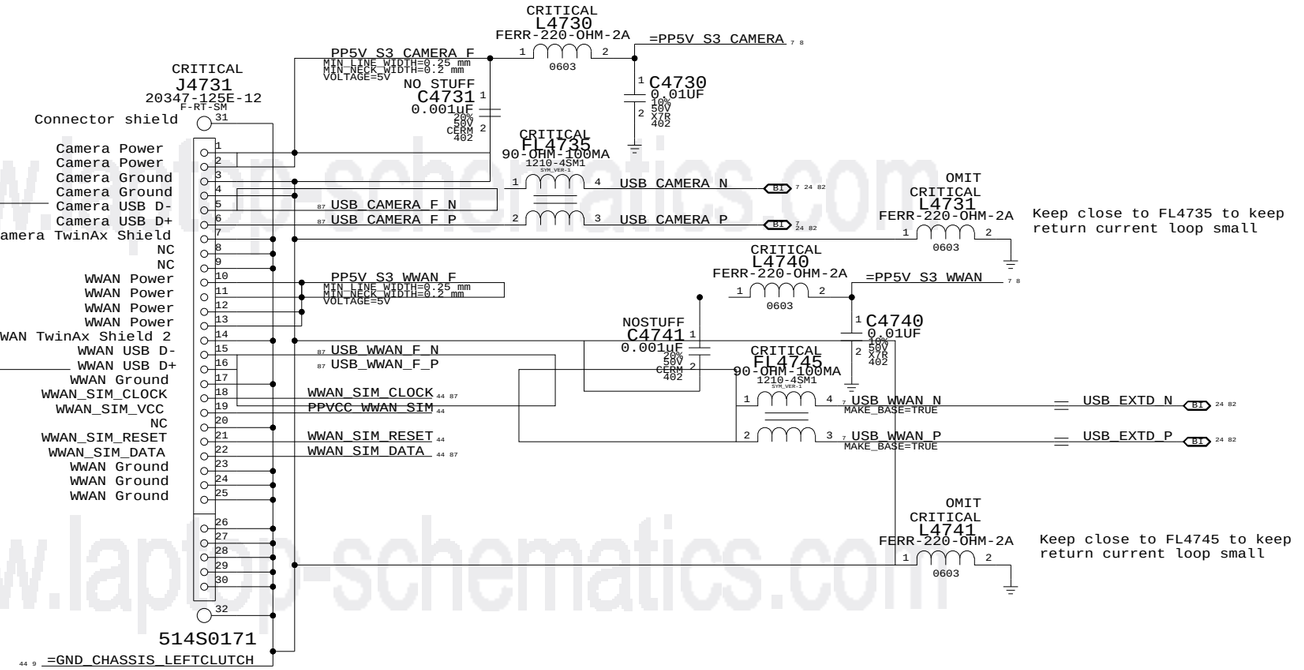
APPLE INC.

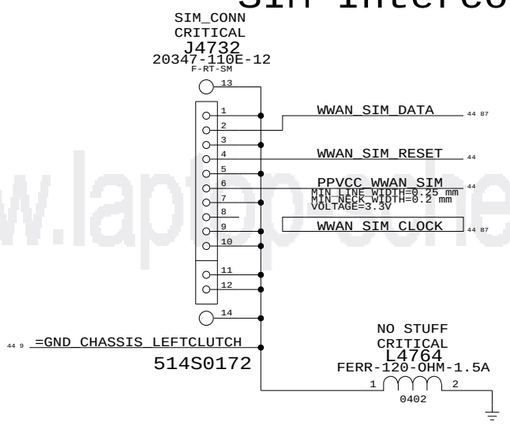
SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 46 OF 109	

Left Clutch Barrel Interconnect



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
113S0022	2	RES,MF,1/10W,0OHM,5,0603,SM,LF	L4731,L4741	CRITICAL	

SIM Interconnect



Left Clutch Barrel Interconnect

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 47 OF 109	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

OMIT
U4900
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE		B12	P10	P60/KIN0*	L13	SMC_PM_G2_EN	
SMC_RSTGATE_L		C13	P11	P61/KIN1*	L14	SMC_ADAPTER_EN	
ALL_SYS_PWRGD		A15	P12	P62/KIN2*	L15	SMC_P62	
RSMRST_PWRGD		B14	P13	P63/KIN3*	K12	SMC_P63	
SMC_P14		B15	P14	P64/KIN4*	K13	SMC_P64	
PM_RSMRST_L		C14	P15	P65/KIN5*	K14	PM_LAN_PWRGD	
IMVP_VR_ON		D12	P16	P66/IRQ6*/KIN6*	J12	SMC_PROCHOT_3_3_L	
PM_PWRBTN_L		C15	P17	P67/IRQ7*/KIN7*	J13	SMC_P67	
SMC_P20		D13	P20	P70/AN0	N12	SMC_CPU_ISENSE	
SMC_P21		D14	P21	P71/AN1	R13	SMC_CPU_VSENSE	
SMC_P22		D15	P22	P72/AN2	P13	SMC_GPU_ISENSE	
SMC_P23		E12	P23	P73/AN3	R14	SMC_GPU_VSENSE	
SMC_BATT_TRICKLE_EN_L		E14	P24	P74/AN4	P14	SMC_DCIN_ISENSE	
SMC_BATT_CHG_EN		E15	P25	P75/AN5	R15	SMC_PBUS_VSENSE	
SMC_P26		E13	P26	P76/AN6	N13	SMC_BATT_ISENSE	
SMC_P27		F14	P27	P77/AN7	P15	SMC_NB_1V25_ISENSE	
LPC_AD<0>		D9	P30/LAD0	P80/PME*	C7	SMC_WAKE_SCI_L	
LPC_AD<1>		C9	P31/LAD1	P81/GA20	A7	SMC_P81	
LPC_AD<2>		A9	P32/LAD2	P82/CLKRUN*	B7	PM_CLKRUN_L	
LPC_AD<3>		B9	P33/LAD3	P83/LPCPD*	D6	PM_SUS_STAT_L	
LPC_FRAME_L		D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	SMC_TX_L	
SMC_LRESET_L		C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	SMC_RX_L	
PCI_CLK33M_SMC		A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	(OC) SMB_MGMT_CLK	
INT_SERIRQ		D7	P37/SERIRQ	P90/IRQ2*	K4	SMC_ONOFF_L	
SMC_GFX_THROTTLE_L		A5	P40/TMI0	P91/IRQ1*	J2	SMC_BC_ACOK	
SMC_SYS_LED		B5	P41/TMO0	P92/IRQ0*	J1	SMC_BS_ALRT_L	
SMB_MGMT_DATA	(OC)	D5	P42/SDA1	P93/IRQ12*	J3	PM_SLP_S3_L	
SMC_P43		C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	PM_S4_STATE_L	
SMC_P44		B1	P44/TMO1	P95/IRQ14*	H2	PM_SLP_S5_L	
SMC_P45		C2	P45	P96/EXCL	H1	SMC_SUS_CLK	
SMC_P46		D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	(OC) SMB_0_S0_DATA	
SMC_SYS_KBDLED		C1	P47/PWX1/PWM1				
SMC_TX_L		G1	P50				
SMC_RX_L		G4	P51				
SMB_0_S0_CLK	(OC)	F2	P52/SCL0				

OMIT
U4900
SMC_H8S2116
BGA
(2 OF 4)

(DEBUG_SW_1)	SMC_PA0		R3	PA0/KIN8*/PA2DC	PE0	M3	SMC_CASE_OPEN
(DEBUG_SW_2)	SMC_PA1		P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	SMC_TCK
	PM_SYSRST_L	(OC)	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	SMC_TDI
	USB_DEBUGPRT_EN_L	(OC)	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	SMC_TDO
	PM_EXTTS_L<0>	(OC)	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	SMC_TMS
	PM_EXTTS_L<1>	(OC)	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7	SMC_PF0
	SYS_ONEWIRE	(OC)	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6	SMC_PF1
	PM_BATLOW_L	(OC)	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	SMC_LID
(DEBUG_SW_3)	SMC_PB0		B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	SMC_PF3
	SMC_RUNTIME_SCI_L		A10	PB1/LSCI	PF4/PWM4	M6	SMC_BATT_ISET
	SMC_ODD_DETECT		D10	PB2	PF5/PWM5	R5	SMC_BATT_VSET
	ISENSE_CAL_EN		A11	PB3	PF6/PWM6	P5	SMC_SYS_ISET
	SMC_EXCARD_CP		B11	PB4	PF7/PWM7	N5	SMC_SYS_VSET
	SMC_EXCARD_PWR_EN		C11	PB5	PG0/EXIRQ8*/TMIX	P9	SMC_PG0
	SMC_EXCARD_OC_L		A12	PB6	PG1/EXIRQ9*/TMIY	R9	=SMC_SMS_INT
	SMC_GFX_OVERTEMP_L		D11	PB7	PG2/EXIRQ10*/SDA2	N9	(OC) SMB_BSA_DATA
	SMC_FAN_0_CTL		G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	(OC) SMB_BSA_CLK
	SMC_FAN_1_CTL		G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	(OC) SMB_A_S3_DATA
	SMC_FAN_2_CTL		G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	(OC) SMB_A_S3_CLK
	SMC_FAN_3_CTL		G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	(OC) SMB_B_S0_DATA
	SMC_FAN_0_TACH		H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	(OC) SMB_B_S0_CLK
	SMC_FAN_1_TACH		H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	SMC_PROCHOT
	SMC_FAN_2_TACH		H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	SMC_THRMTRIP
	SMC_FAN_3_TACH		H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	SMC_FWE
	SMS_X_AXIS		M11	PD0/AN8	PH3/EXEXCL	C4	ALS_GAIN
	SMS_Y_AXIS		P11	PD1/AN9	PH4	D4	SMC_PH4
	SMS_Z_AXIS		R11	PD2/AN10	PH5	B3	SMS_ONOFF_L
	SMC_ANALOG_ID		N11	PD3/AN11			
	SMC_NB_CORE_ISENSE		P10	PD4/AN12			
	SMC_NB_1V8_ISENSE		R10	PD5/AN13			
	ALS_LEFT		N10	PD6/AN14			
	ALS_RIGHT		M10	PD7/AN15			

PP3V3_S5_AVREF_SMC
=PP3V3_S5_SMC

C4902 22UF 20% 6.3V CERM-25M 805-3
C4903 0.1UF 20% 10V CERM 402
C4904 0.1UF 20% 10V CERM 402
C4905 0.1UF 20% 10V CERM 402
C4906 0.1UF 20% 10V CERM 402

R4999 4.7 5% 1/10W MF-LF 402
PP3V3_S5_SMC_AVCC
MIN_LINE_WIDTH=0.28 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
C4920 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place R4999 close to U4900 pins N14,N15
PLACEMENT_NOTE=Place C4920 close to U4900 pins N14,N15

PLACEMENT_NOTE=Place C4907 close to U4900 pin F1
SMC_VCL
C4907 0.47UF 10% 6.3V CERM-X5R 402

OMIT
U4900
SMC_H8S2116
BGA
(3 OF 4)

SMC_RESET_L	E3	RES*	
SMC_XTAL	A2	XTAL	
SMC_EXTAL	B2	EXTAL	
	N14	AVCC	
	N15	AVCC	
	P2	VCC	
	P1	VCC	
	J15	VCC	
	A1	VCC	
	F1	VCL	
	M14	AVREF	
	M15	AVREF	
	MD1	F2	SMC_MD1
	MD2	K1	SMC_KBC_MDE
	NMI	F4	SMC_NMI
	ETRST*	L1	SMC_TRST_L
	AVSS	P12	
		R12	
	VSS	D1 P4 R4 F12 F13 B13 A13 A4 B4 D2	

R4909 10K 5% 1/10W MF-LF 402
R4901 10K 5% 1/10W MF-LF 402
R4902 10K 5% 1/10W MF-LF 402
R4998 10K 5% 1/10W MF-LF 402
R4903 0 5% 1/10W MF-LF 402
NO STUFF

XW4900 SM

GND_SMC_AVSS

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

OMIT
U4900
SMC_H8S2116
BGA
(4 OF 4)

NC	G3	NC0	
NC	H3	NC1	
NC	K3	NC2	
NC	L3	NC3	
NC	N4	NC4	
NC	M5	NC5	
NC	N7	NC6	
NC	M12	NC7	
NC	M13	NC8	
NC	L12	NC9	
NC	K15	NC10	
NC	J14	NC11	
		NC12	F15 NC
		NC13	A14 NC
		NC14	C12 NC
		NC15	C10 NC
		NC16	C5 NC
		NC17	A3 NC
		NC18	B8 NC
		NC19	E4 NC
		NC20	H4 NC
		NC21	M9 NC
		NC22	N8 NC

SMC
SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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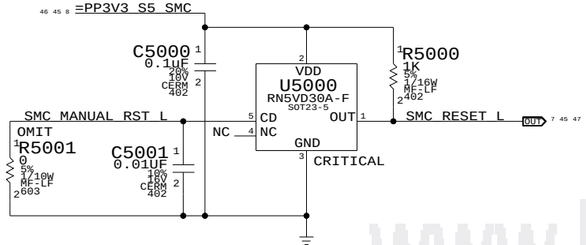
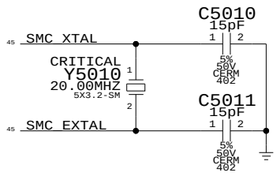
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 49 OF 109	

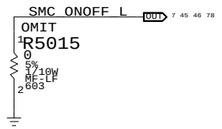
SMC Reset "Button" / Brownout Detect



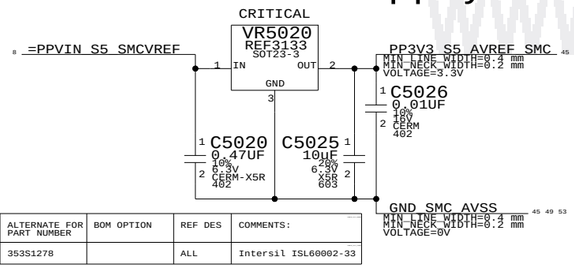
SMC Crystal Circuit



Debug Power "Button"

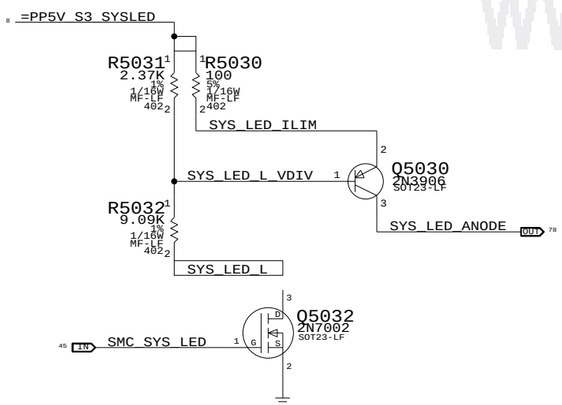


SMC AVREF Supply

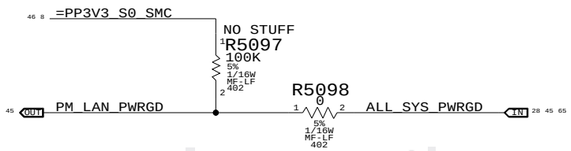


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

System (Sleep) LED Circuit

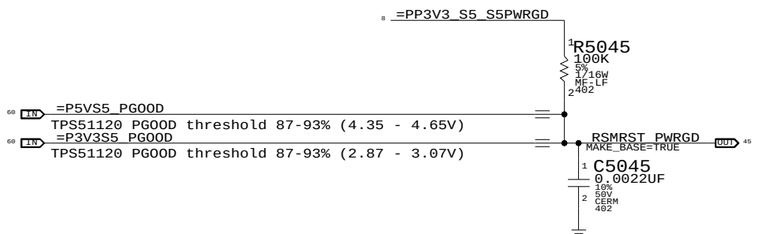


LAN PWRGD Circuit

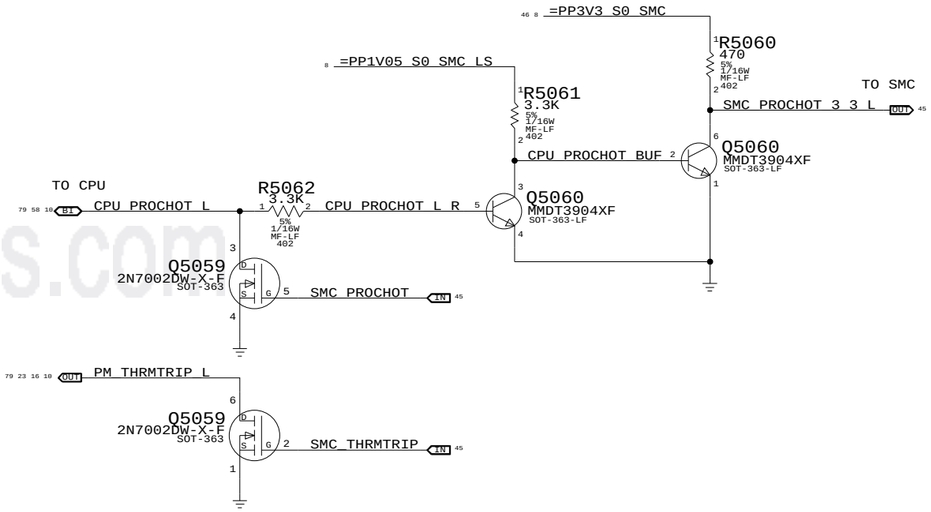


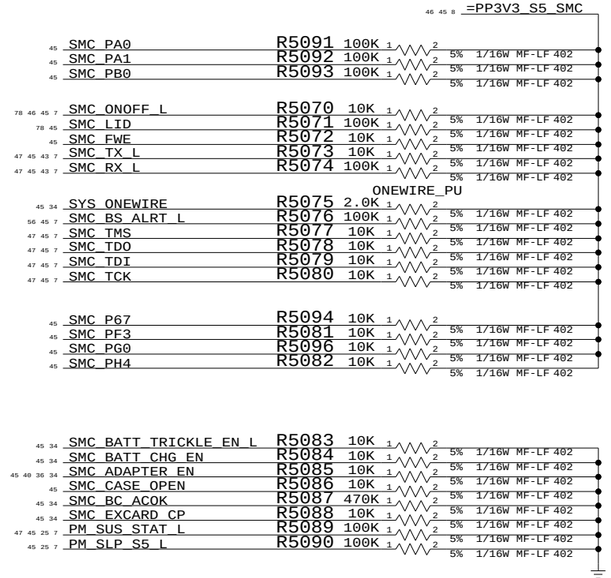
S5 Rail PWRGD Circuit

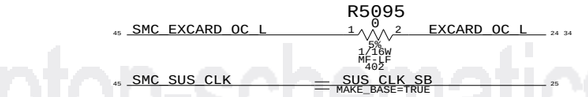
Reports when 5V S5 and 3.3V S5 are in regulation



SMC FSB to 3.3V Level Shifting







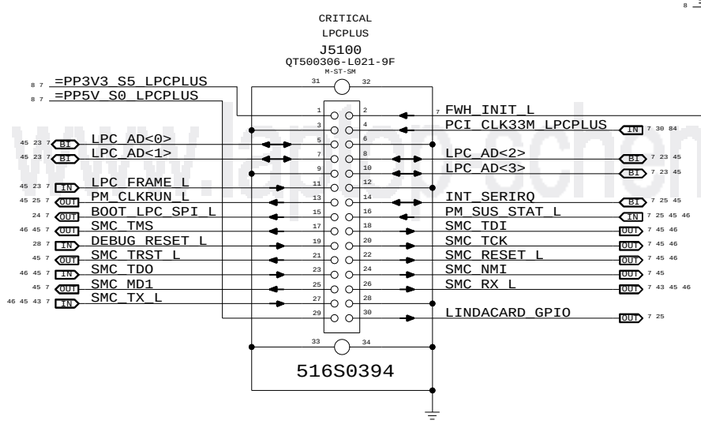
SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

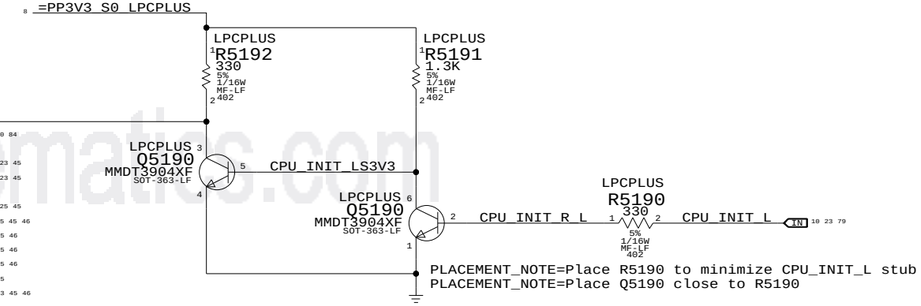
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 50 OF 109	

LPC+ Connector



FWH_INIT_L Generation



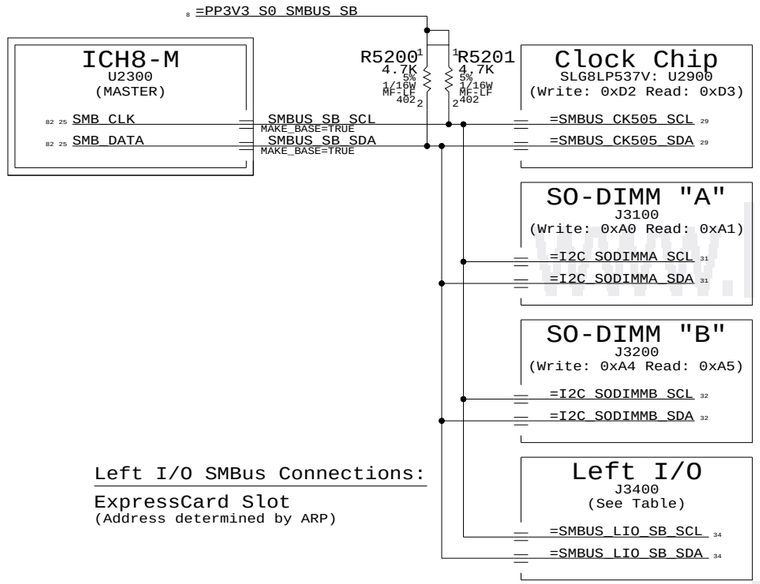
LPC+ Debug Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

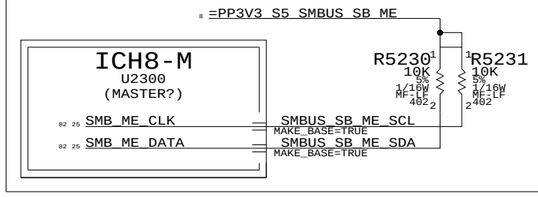
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 51 OF 109	

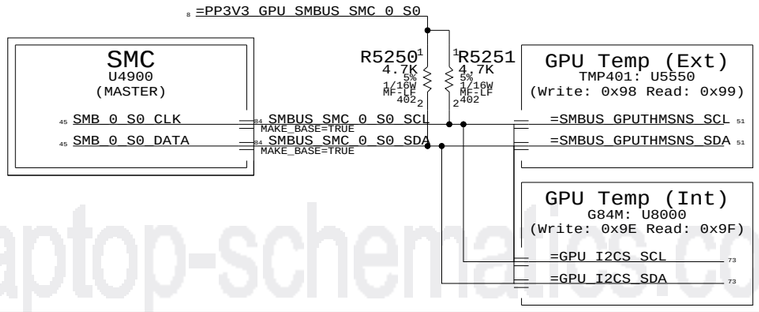
ICH8-M SMBus Connections



ICH8-M ME SMBus Connections

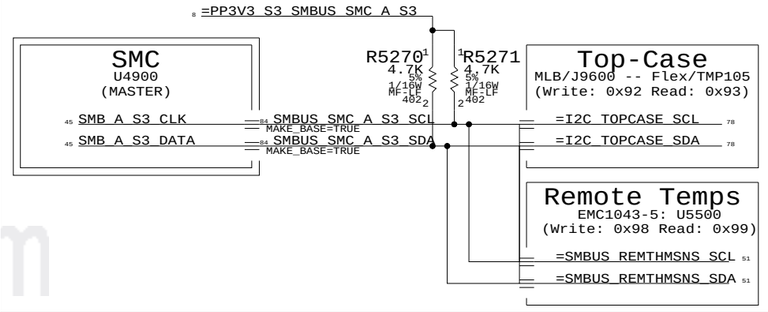


SMC "0" SMBus Connections

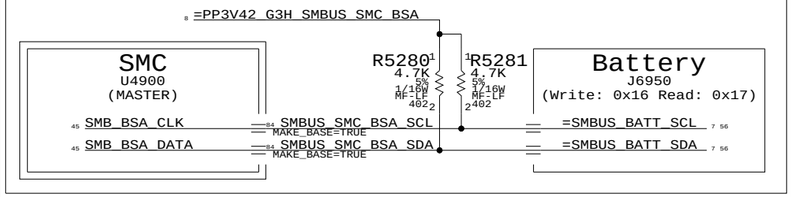


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

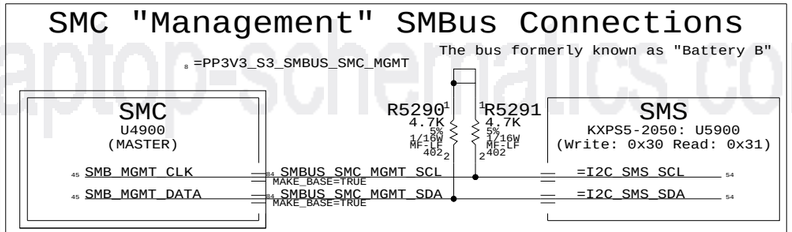


SMC "Battery A" SMBus Connections

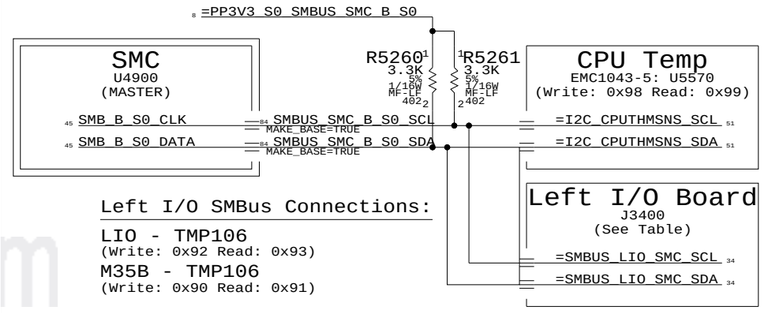


SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



SMC "B" SMBus Connections



SMBus Connections

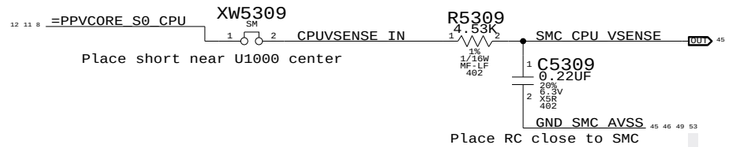
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

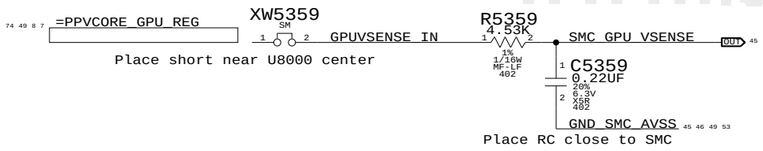
SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	52	109

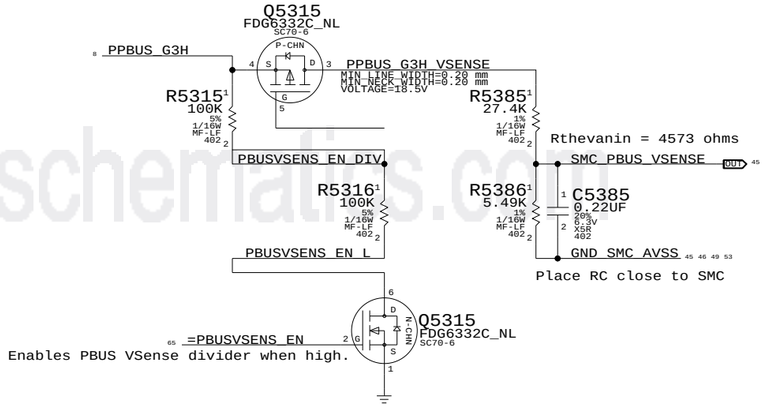
CPU Voltage Sense / Filter



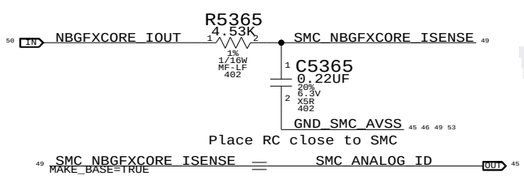
GPU Voltage Sense / Filter



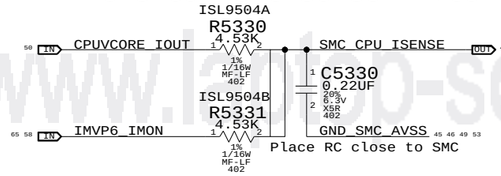
PBUS Voltage Sense & Filter



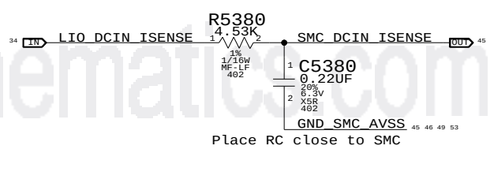
NB GFX Current Sense Filter



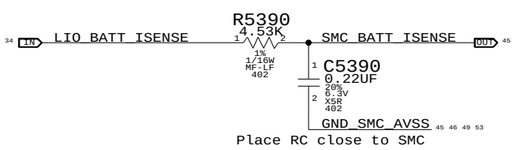
CPU Current Sense Filter



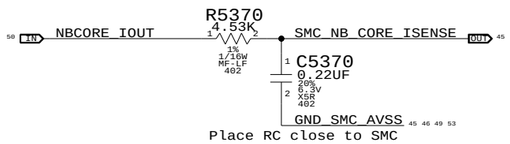
DCIN Current Sense Filter



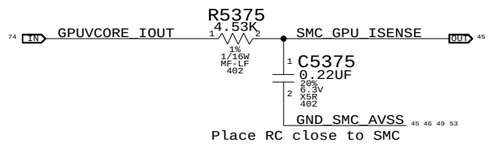
Battery (PBUS) Current Sense Filter



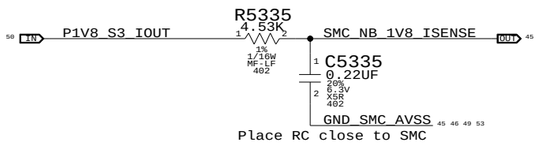
NB Core Current Sense Filter



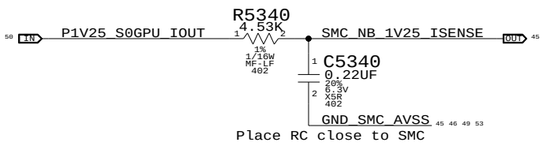
GPU Current Sense Filter



NB 1.8V Current Sense Filter

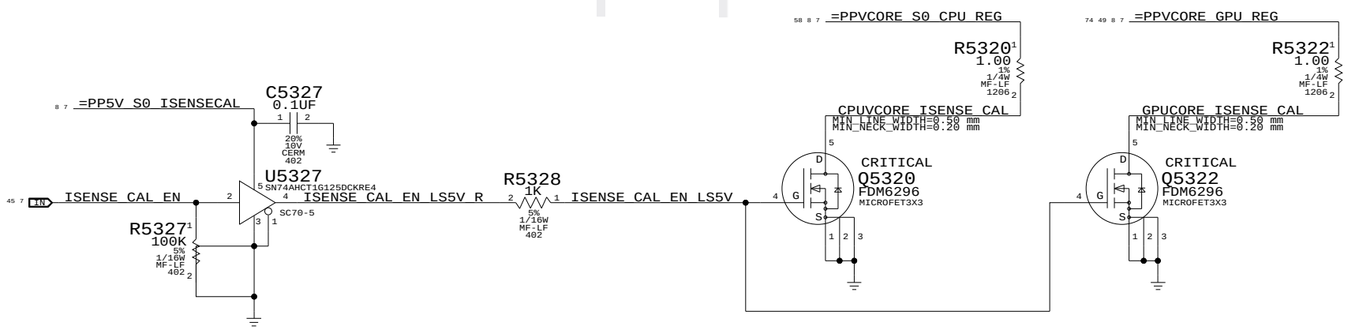


S0/GPU 1.25V Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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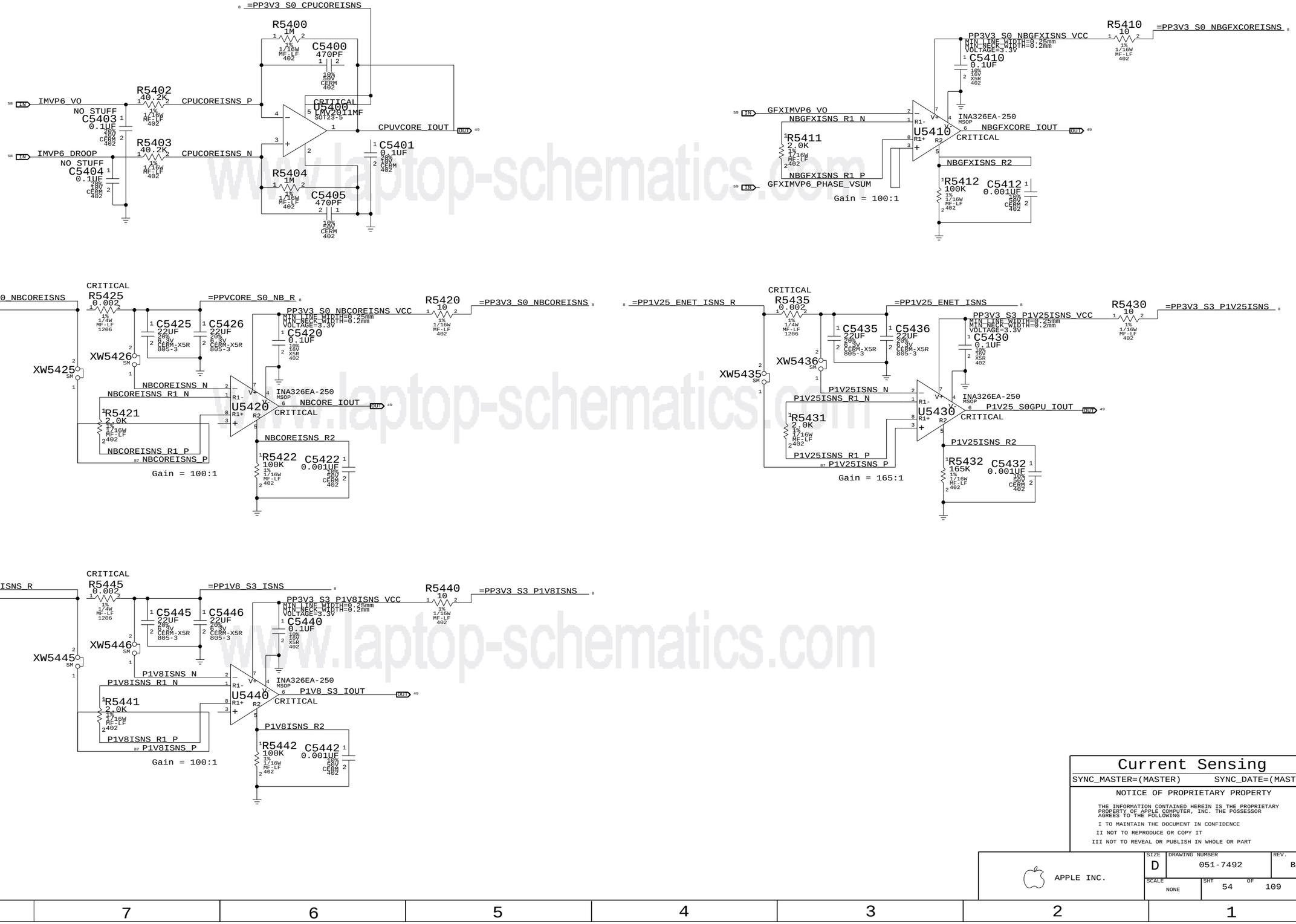
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 53 OF 109	



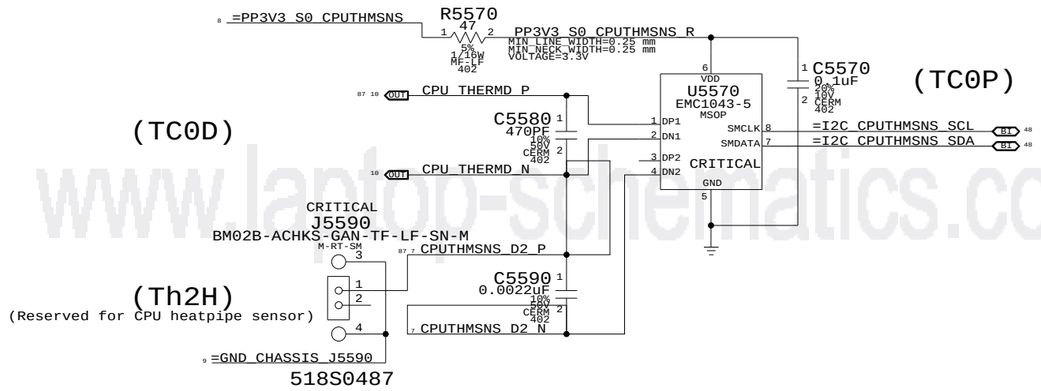
Current Sensing

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

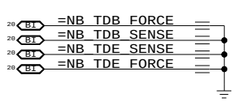
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 54 OF 109	

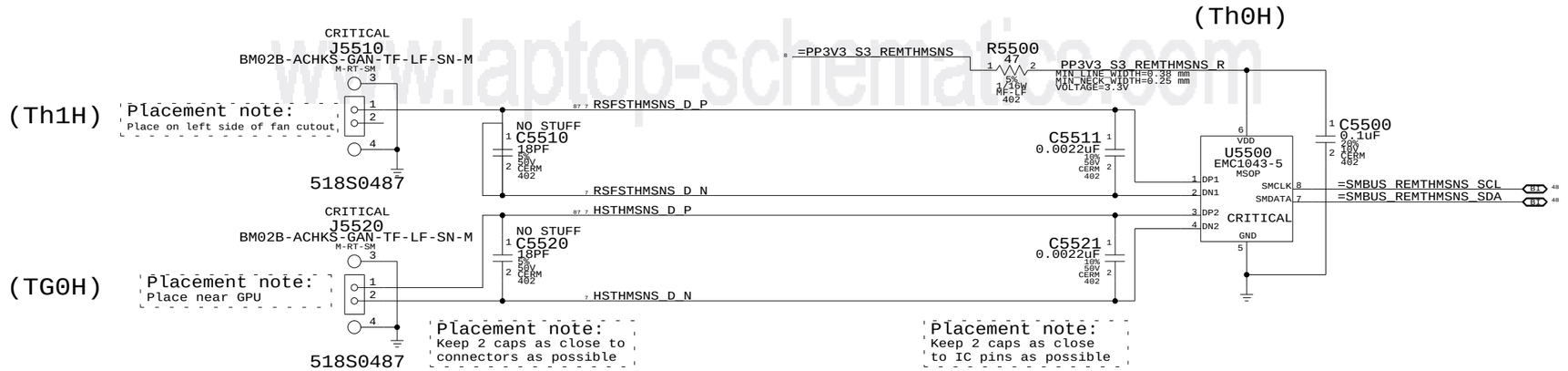
CPU T-Diode Thermal Sensor



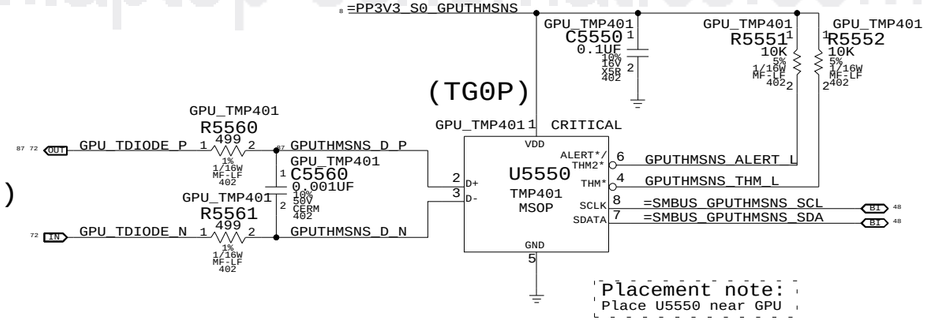
NB Thermal Diodes Not Used



GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



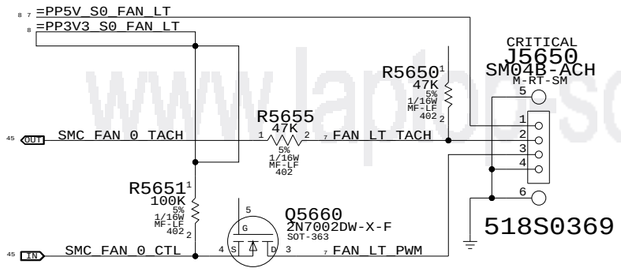
Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

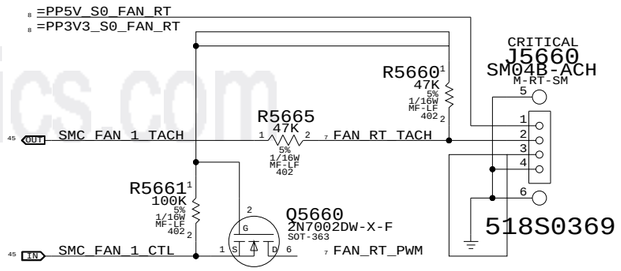
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 55 OF 109	

Left Fan



Right Fan



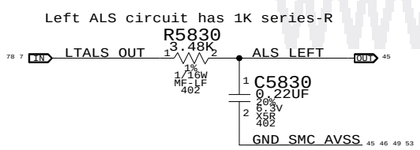
Fan Connectors

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

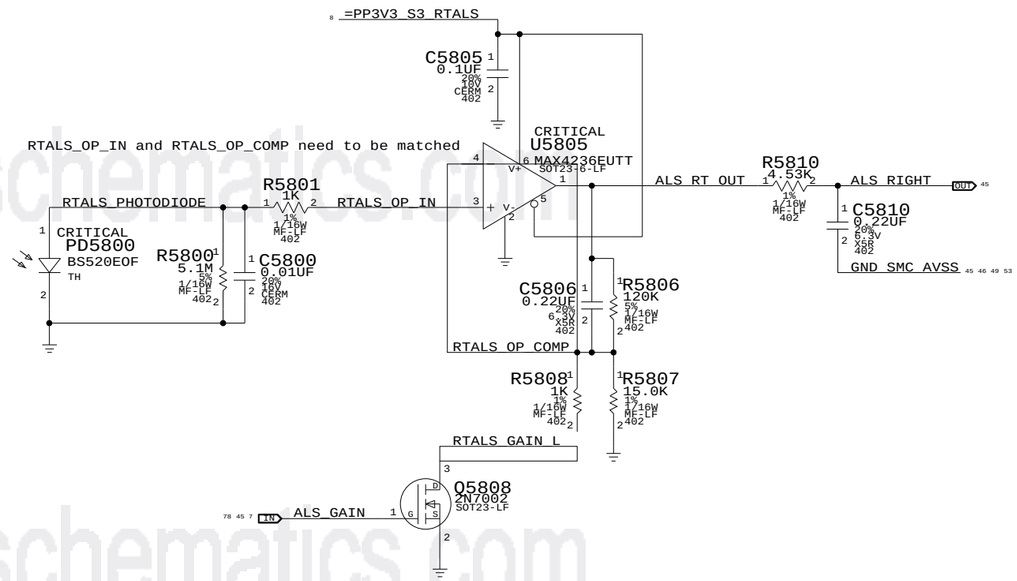
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 56 OF 109	

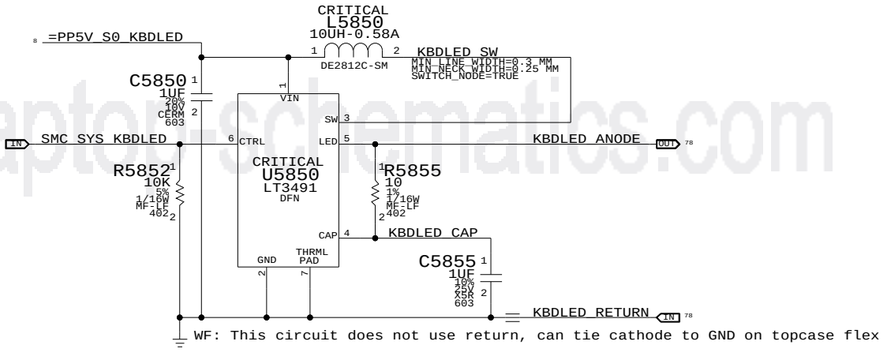
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



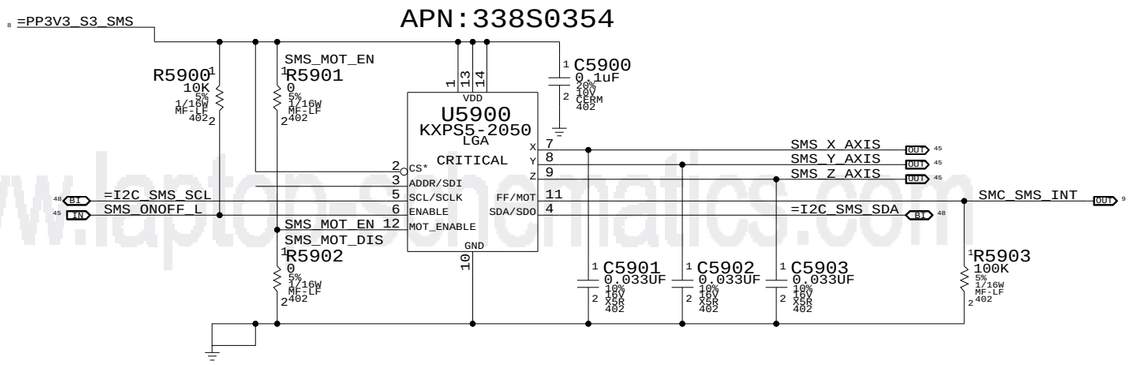
ALS Support

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 58 OF 109	

APN:338S0354

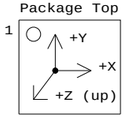


I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

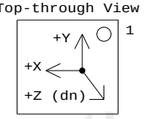
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



Sudden Motion Sensor (SMS)

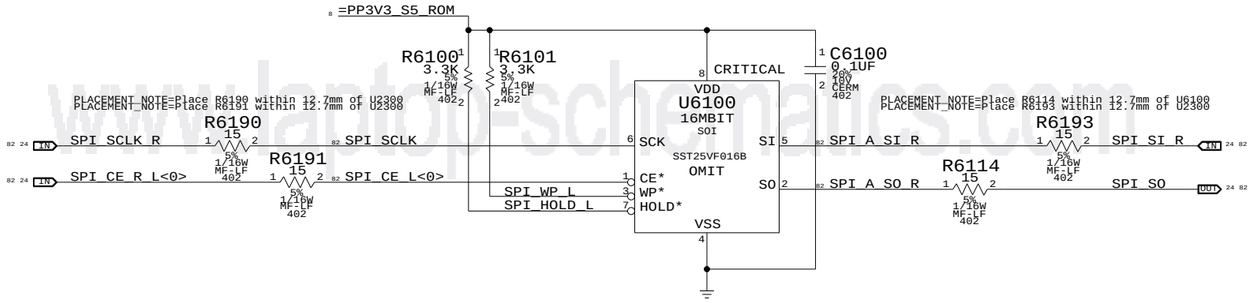
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE: NONE

SHT 59 OF 109



SPI BootROM

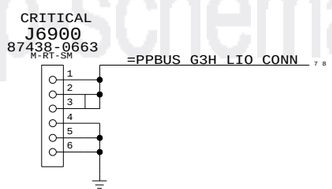
SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

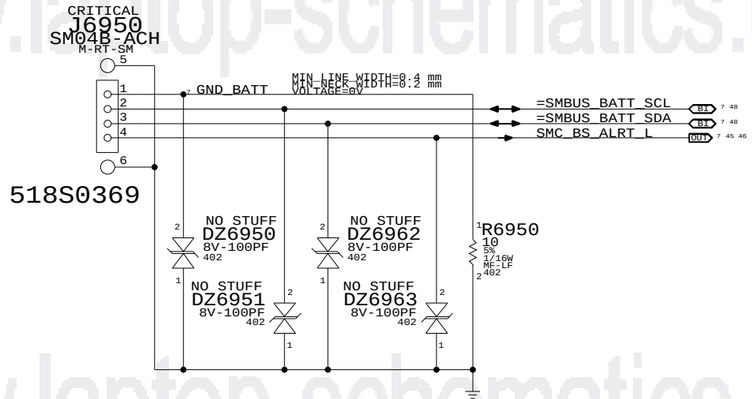
SCALE	SHT	OF
NONE	61	109

Left I/O Power Connector



518S0458

Battery Connector (Digital Signals)



518S0369

PBus-In & Battery Connectors

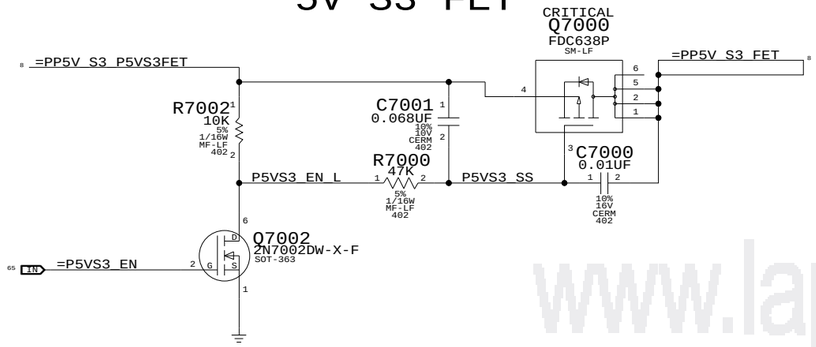
SYNC_MASTER=(M59_SYNC) SYNC_DATE=09/09/2006

APPLE INC.

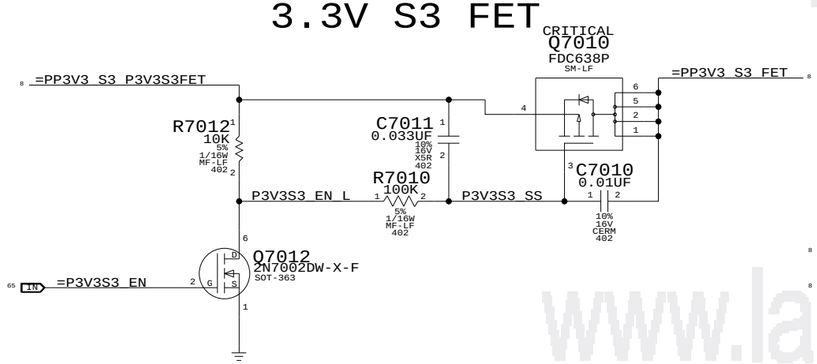
SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	69	109

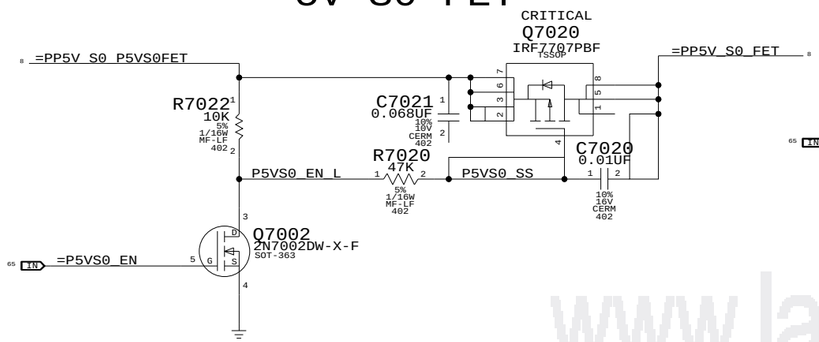
5V S3 FET



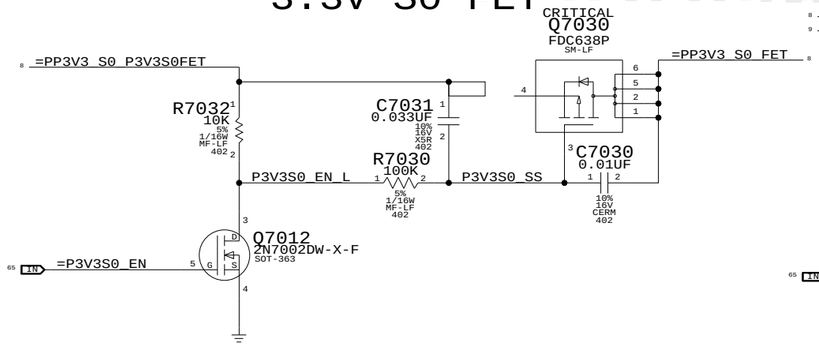
3.3V S3 FET



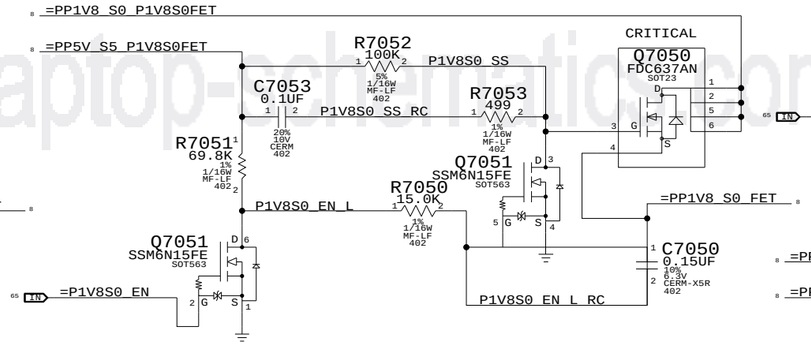
5V S0 FET



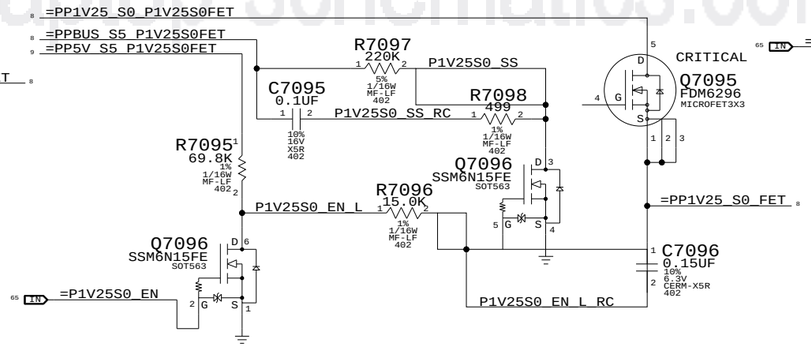
3.3V S0 FET



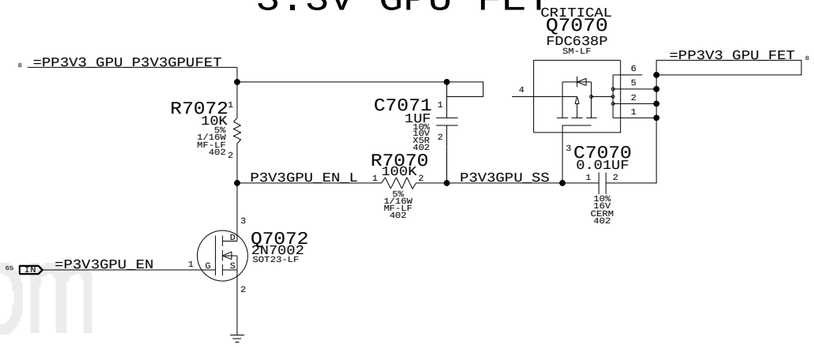
1.8V S0 FET



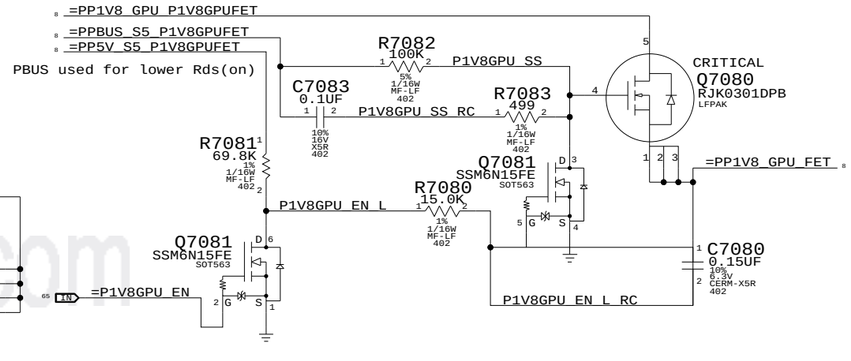
1.25V S0 FET



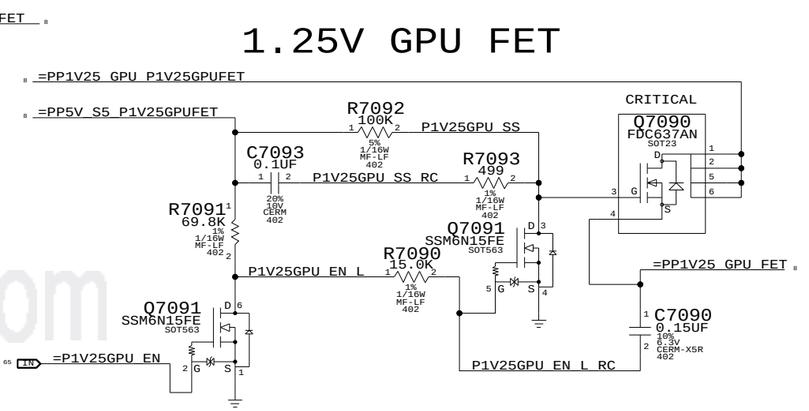
3.3V GPU FET



1.8V GPU FET



1.25V GPU FET

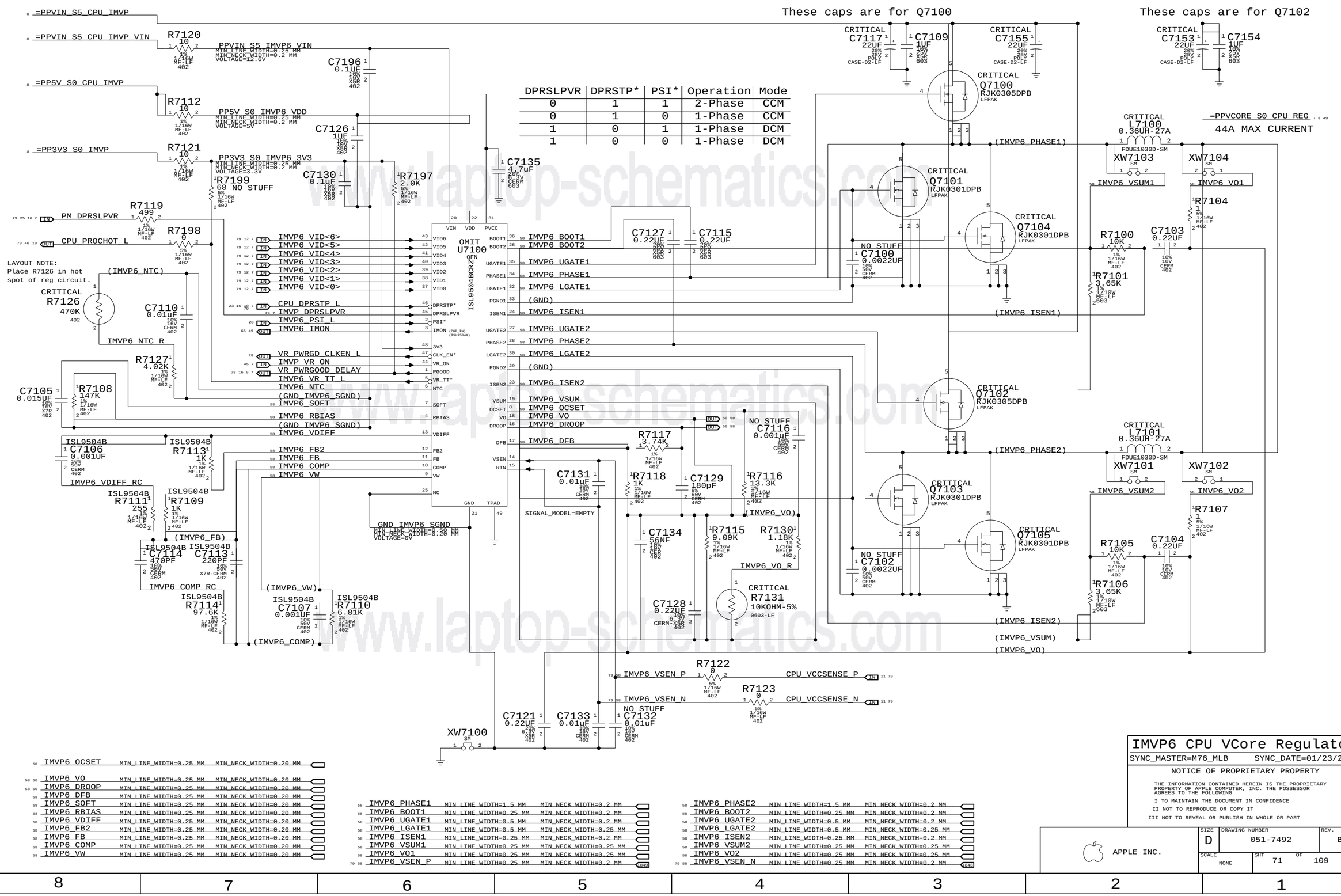


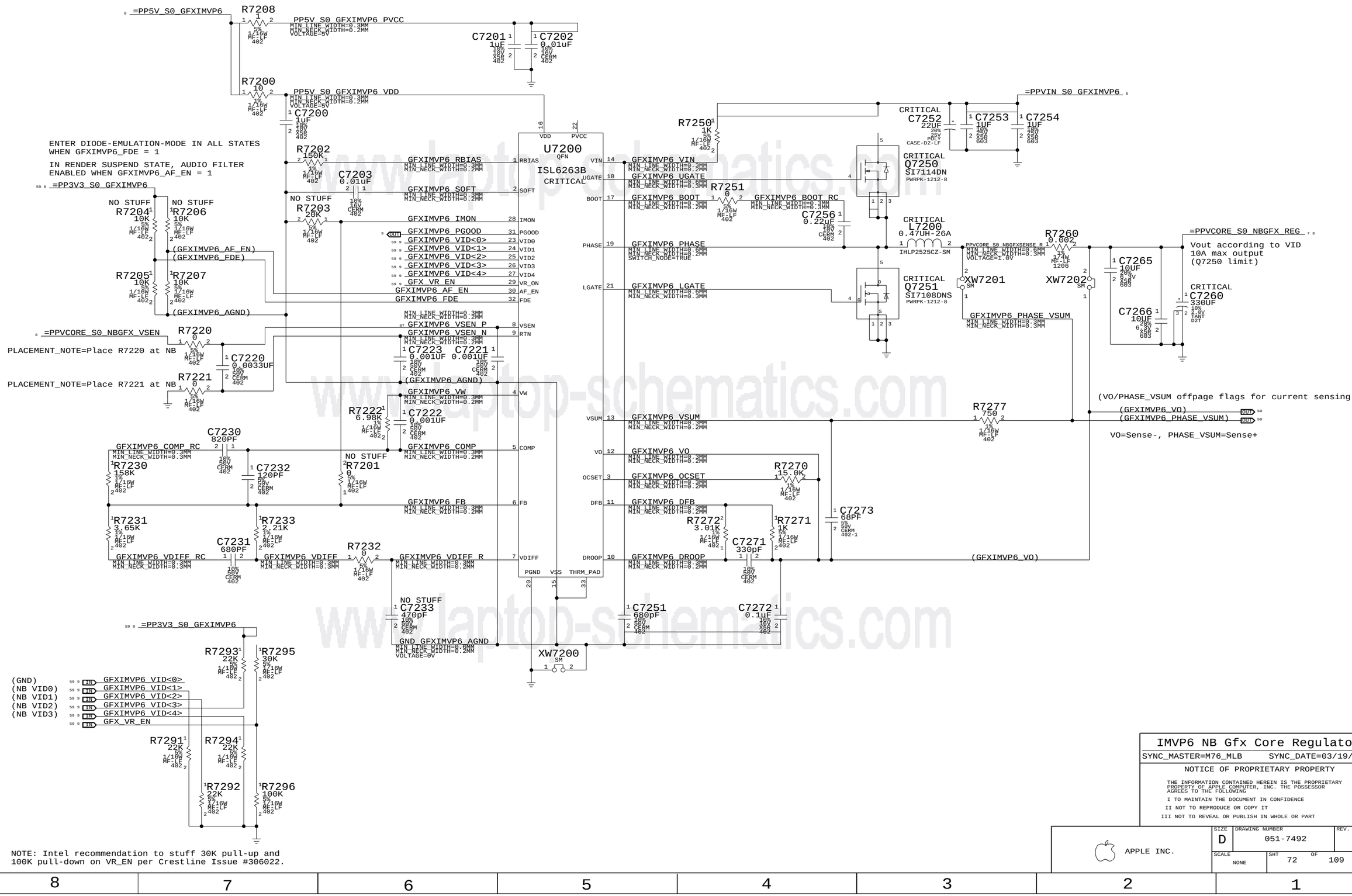
Power FETs

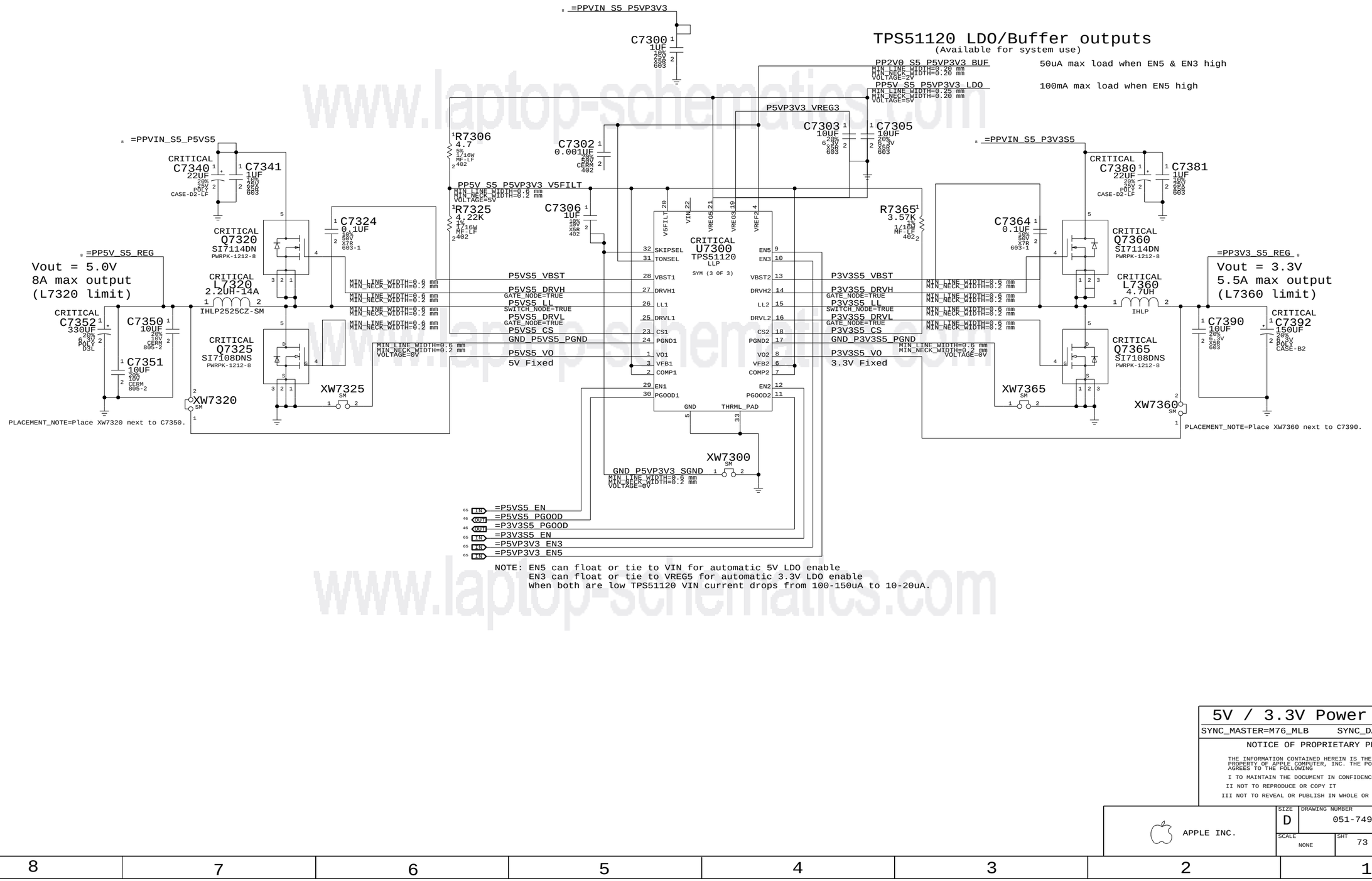
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 70 OF 109	





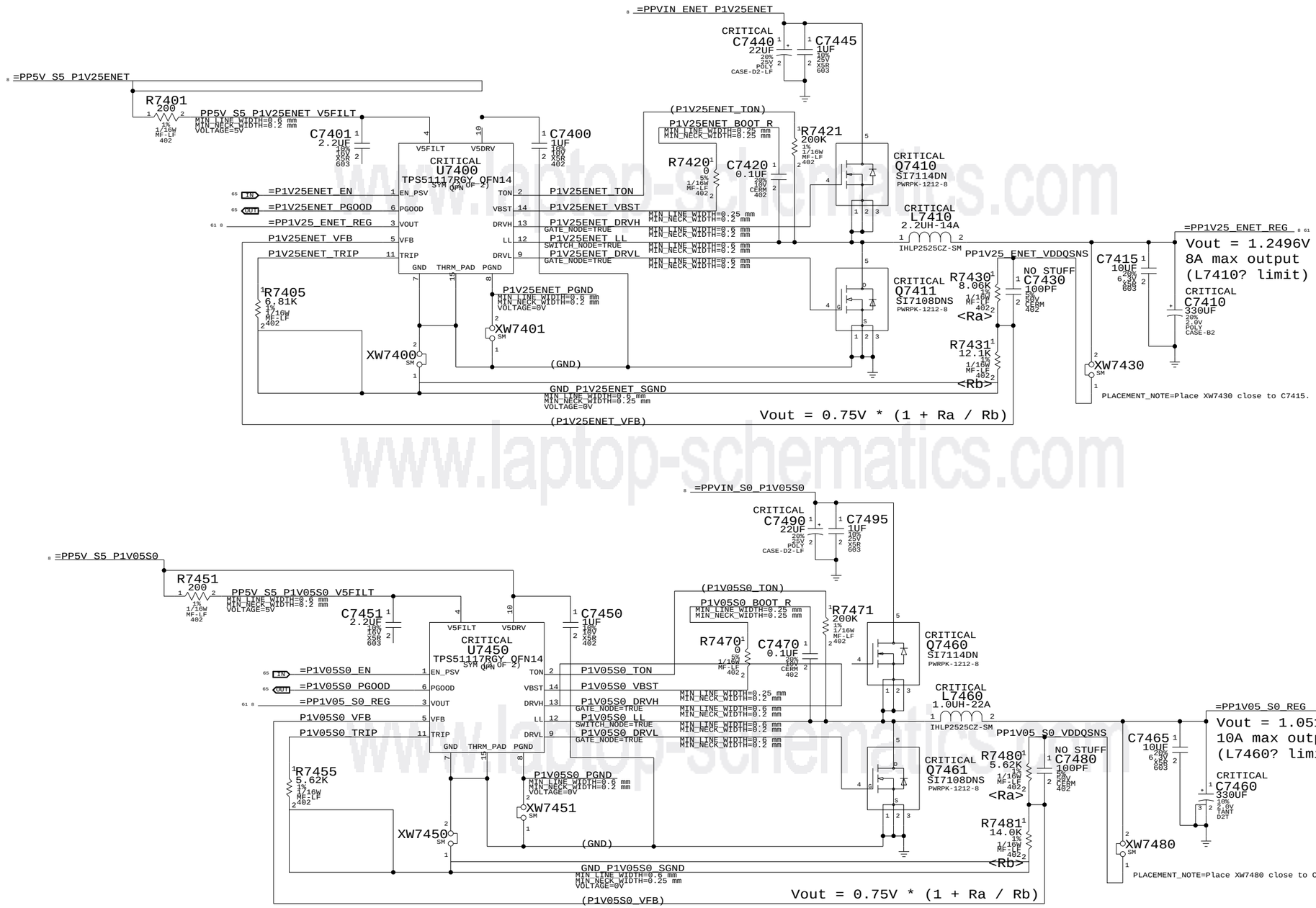


5V / 3.3V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 73 OF 109	

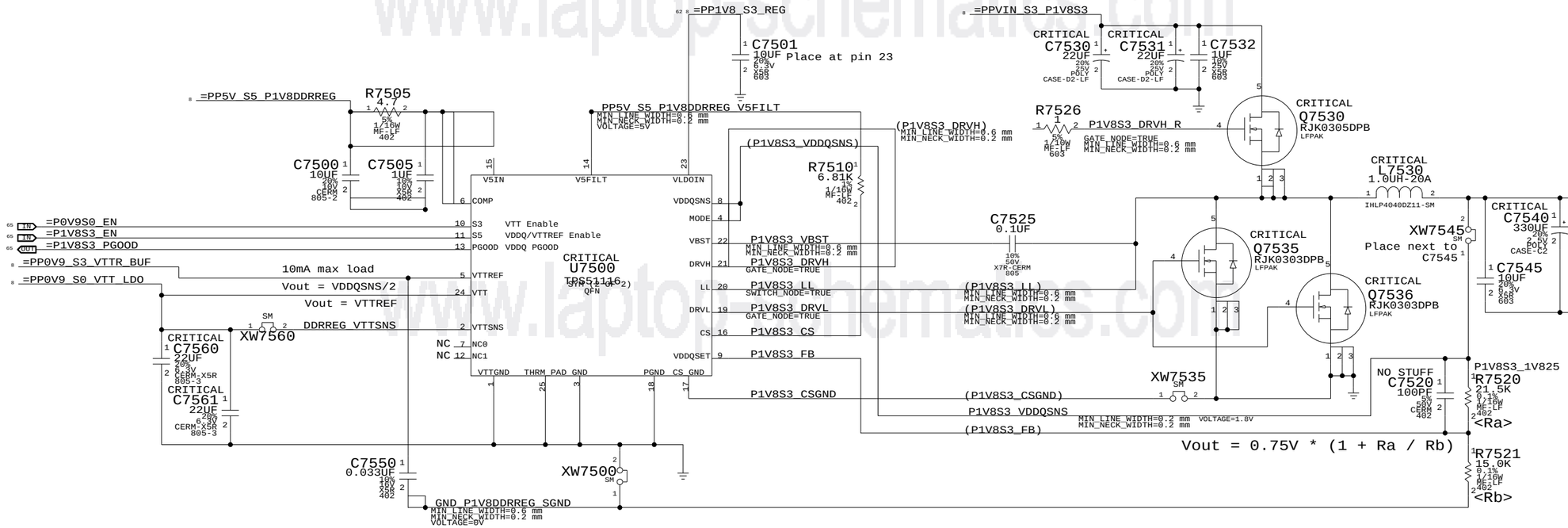


1.25V / 1.05V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE	SHT	OF
NONE	74	109



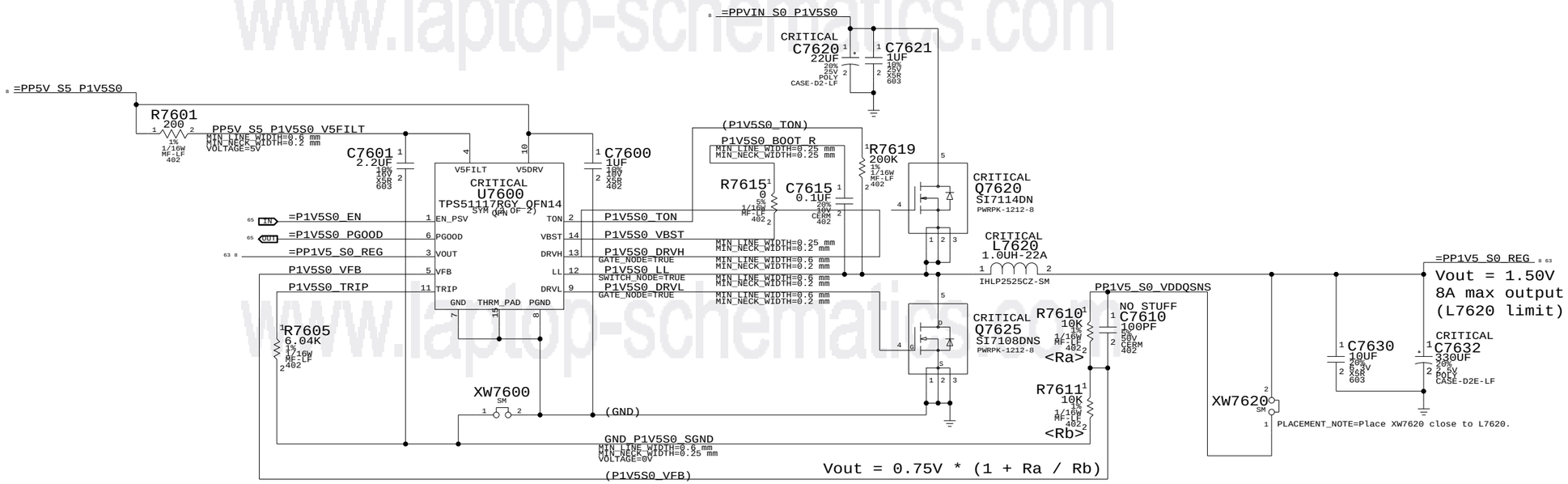
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S0192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V8

1.8V DDR2 Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 75 OF 109	



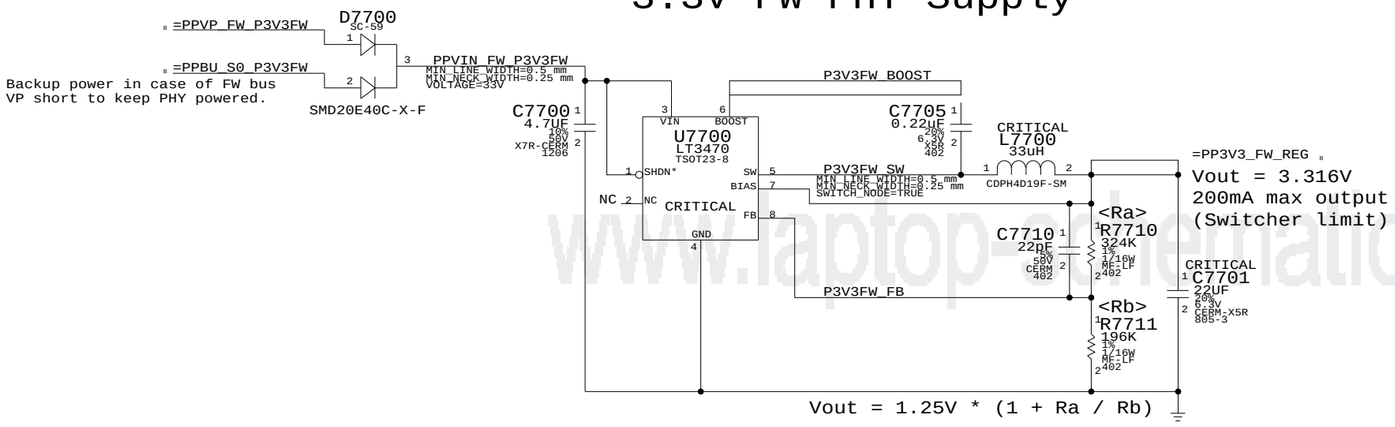
1.5V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

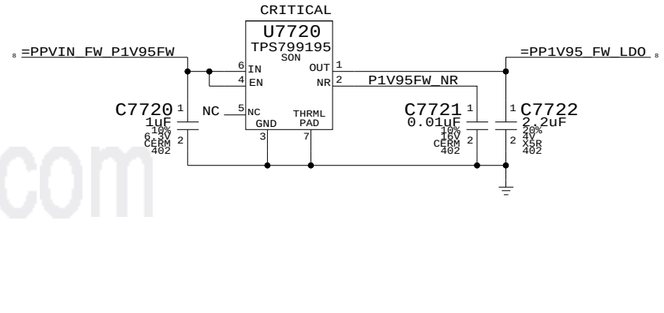
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 76 OF 109	

3.3V FW PHY Supply



1.95V FW PHY Supply



FW PHY Power Supplies

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 77 OF 109	

Power Control Signals

=PP5V_S5_PWRCTL

=PP3V3_GPU_PWRCTL

R7850 10K 5% 1/16W MF-LF 402

R7851 100K 5% 1/16W MF-LF 402

R7852 100K 5% 1/16W MF-LF 402

R7854 10K 5% 1/16W MF-LF 402

G84M GPU requires rails to come up in the following order:
1) 1.2V
2) 3.3V
3) Vcore
4) 1.8V

=GPUVCORE_PGOOD

Need to ensure that TPS51117 PGOOD does not deassert while GPU VIDs are changing GPU core voltage.

PM_GPUP1V8FET_EN — MAKE_BASE=TRUE — =P1V8GPU_EN

PM_GPUVCORE_EN — MAKE_BASE=TRUE — =GPUVCORE_EN

Q7850 2N7002DW-X-F SOT-363

Q7851 2N7002DW-X-F SOT-363

PVCOREGPU_EN_L

Q7851 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V — MAKE_BASE=TRUE — LIO_S0_EN_L

Q7850 2N7002DW-X-F SOT-363

PM_SLP_S3_L

R7856 100K 5% 1/16W MF-LF 402

(PM_SLP_S3_L) — MAKE_BASE=TRUE

=P5VS0_EN
=P3V3S0_EN
=P1V8S0_EN
=P1V25S0_EN
=P0V9S0_EN
=PBUSVSENS_EN
=ENET_VMAIN_AVLBL
=PM_SLP_S3_DELAY_L

R7853 10K 5% 1/16W MF-LF 402

EXTGPU_PWR_EN — (EXTGPU_PWR_EN) MAKE_BASE=TRUE

=PVCOREGPU_EN
=P3V3GPU_EN
=P1V25GPU_EN

SB GPIO has ability to force all GPU rails off
R7853 acts as pull-up for open-drain GPIO.

NO STUFF
C7853 0.047UF 10% 16V CERM 402

Fast wake glitch filter. Should not be necessary to stuff if GPU supplies and PGOOD revalidate before 99ms SMC timer expires.

PP1V2_GPU needs to ramp first via RC control

PM_ENET_EN — (PM_ENET_EN) MAKE_BASE=TRUE

=P3V3ENET_EN
=P1V25ENET_EN

PM_S4_STATE_L — (PM_S4_STATE_L) MAKE_BASE=TRUE

=P3V3S3_EN
=P5VS3_EN
=USB_EXTA_EN
LIO_S3_EN

R7857 10K 5% 1/16W MF-LF 402

R7855 10K 5% 1/16W MF-LF 402

P1V8S3_EN — MAKE_BASE=TRUE — =P1V8S3_EN

C7855 0.47UF 10% 6.3V CERM-X5R 402

=PP3V42_G3H_PWRCTL

NO STUFF

U7858 MC74VHC1G09 SC70

SMC_PM_G2_EN

PM_G2_EN — MAKE_BASE=TRUE

=P5VS5_EN
=P3V3S5_EN
=P5VP3V3_EN5
=P5VP3V3_EN3

R7858 100K 5% 1/16W MF-LF 402

R7860 0 5% 1/16W MF-LF 402

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

=PPVIN_G3H_P3V42G3H

P3V42G3H5_BOOST

C7800 10UF 10% 16V CERM 1206-1

U7800 LT3470 TSOT23-8

VIN BOOST SHDN* SW BIAS NC FB GND

NC CRITICAL

C7805 0.22UF 20% 50V X5R 402

CRITICAL L7810 33uH CDPH4D19F-SM

P3V42G3H_SW — MIN_LINE_WIDTH=0.5 mm — MIN_NECK_WIDTH=0.25 mm — SWITCH_NODE=TRUE

=PP3V42_G3H_REG

Vout = 3.425
200mA max output
(Switcher limit)

C7810 22pF 5% 50V CERM 402

<Ra> R7810 348K 1% 1/16W MF-LF 402

<Rb> R7811 200K 1% 1/16W MF-LF 402

P3V42G3H_FB

C7815 22UF 20% 6.3V CERM-X5R 805-3

Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

=PP3V3_S0_PWRCTL

=PP3V3_S5_PWRCTL

U7850 MC74VHC1G09 SC70

PM_SLP_S3_DELAY_L — MAKE_BASE=TRUE

R7859 10K 5% 1/16W MF-LF 402

=P1V5S0_EN
=P1V05S0_EN

NO STUFF
C7859 0.047UF 10% 16V CERM 402

Unused PGOOD Signals

=P1V25ENET_PGOOD — TP_P1V25ENET_PGOOD — MAKE_BASE=TRUE

=P1V8S3_PGOOD — TP_P1V8S3_PGOOD — MAKE_BASE=TRUE

IMVP6_IMON — To CPU IMVP6

=PP3V3_S5_P1V5P1V05PG

ISL9504A

R7865 100K 5% 1/16W MF-LF 402

R7866 0 5% 1/16W MF-LF 402

=PP3V3_S0_ALLSYSPG

C7880 0.1UF 20% 16V CERM 402

=P1V5S0_PGOOD
TPS51117 PGOOD threshold 92.5-97.5% (1.36 - 1.46V)

=P1V05S0_PGOOD
TPS51117 PGOOD threshold 92.5-97.5% (0.98 - 1.02V)

P1V5P1V05S0_PGOOD — MAKE_BASE=TRUE

U7880 MC74VHC1G08 SC70

ALL_SYS_PWRGD

NOTE: 0.9V/2.5V is not checked!

Other S0 Rails PWRGD Circuit

Does not include GFX rails

PP5V_S0
PP3V3_S0
PP1V8_S0
PP1V25_S0

R7873 124K 1% 1/16W MF-LF 402

C7872 0.1UF 20% 10V CERM 402

C7871 0.1UF 20% 10V CERM 402

C7870 0.1UF 20% 10V CERM 402

R7875 10K 5% 1/16W MF-LF 402

U7870 LTC2900 DFN

V1 V2 V3 V4 VREF VPG PBR* RST* CRT GND THRM_PAD

CRITICAL

NC

S0PGOOD_P1V2_DIV

S0PGOOD_VREF

S0PGOOD_VPG

S0PGOOD_CRT

S0PGOOD_PWROK

R7874 100K 1% 1/16W MF-LF 402

R7870 9.53K 1% 1/16W MF-LF 402

R7871 93.1K 1% 1/16W MF-LF 402

C7873 0.1UF 20% 10V CERM 402

C7875 0.047UF 10% 16V CERM 402

Trst = 4.6ms/nF
Trst = 216ms

LTC2900 typical threshold is 93.5% (4.675V, 3.086V, 1.685V, 1.120V)

3.425V G3Hot Supply & Power Control		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	
NOTICE OF PROPRIETARY PROPERTY		

APPLE INC.

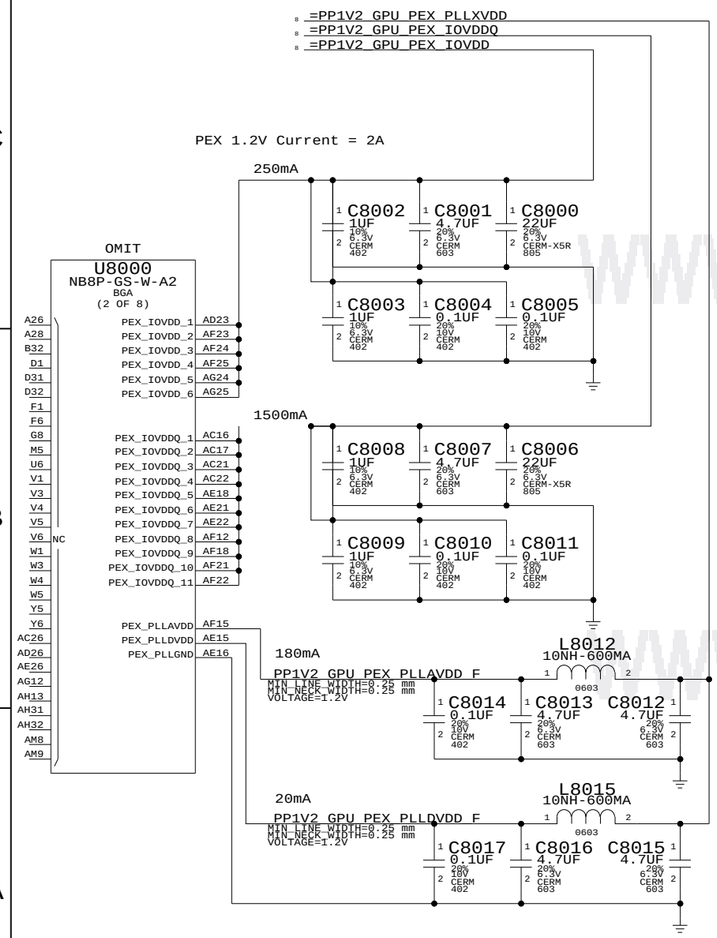
SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 78 OF 109	

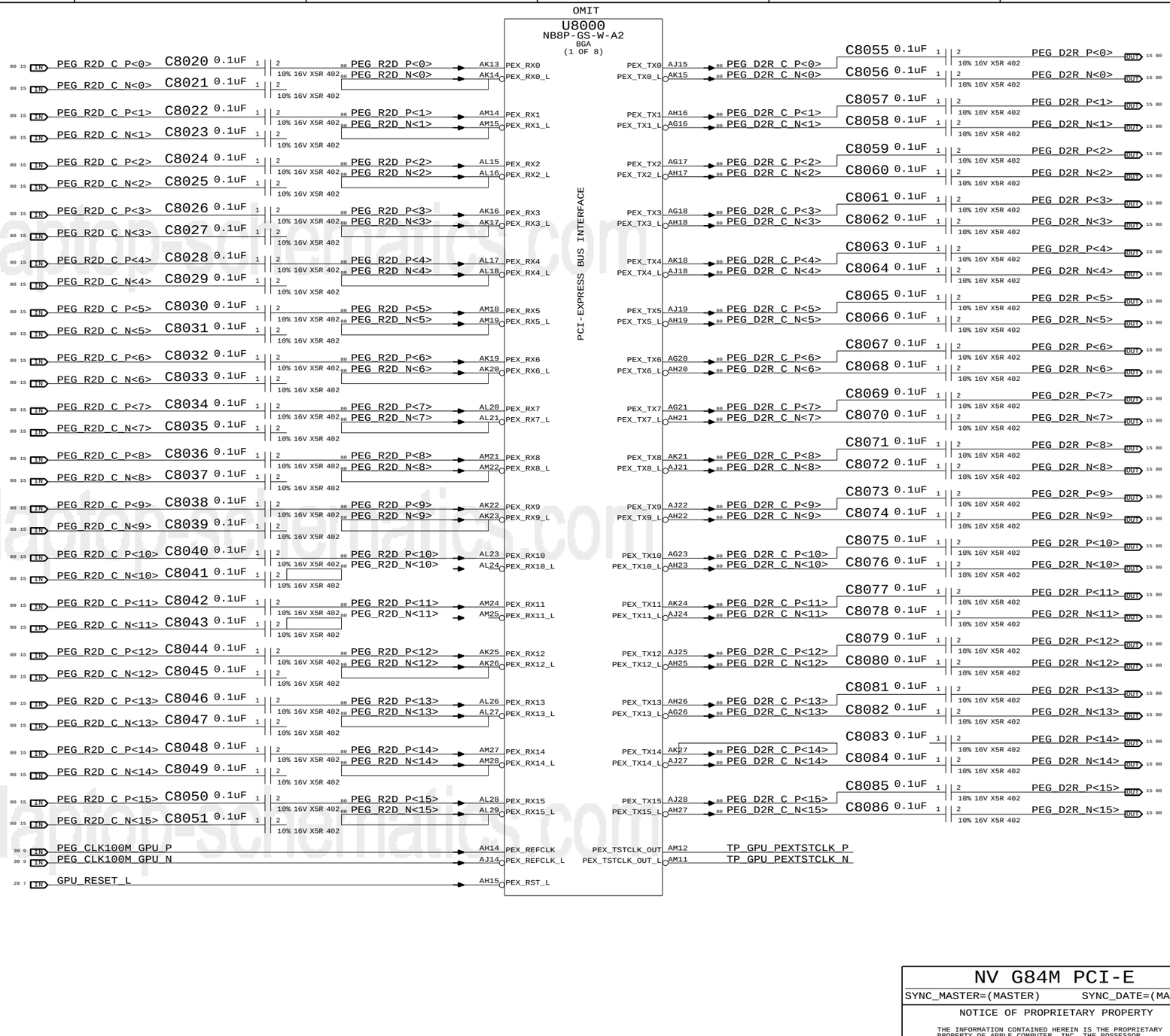
Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





NV G84M PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	80	109

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 1UF 20% 6.3V CERM 402
C8101 1UF 20% 6.3V CERM 402
C8102 1UF 20% 6.3V CERM 402
C8103 0.1UF 20% 10V CERM 402
C8104 0.1UF 20% 10V CERM 402
C8105 0.1UF 20% 10V CERM 402
C8106 0.1UF 20% 10V CERM 402
C8107 0.1UF 20% 10V CERM 402
C8108 0.1UF 20% 10V CERM 402
C8109 0.1UF 20% 10V CERM 402
C8110 0.1UF 20% 10V CERM 402
C8111 0.1UF 20% 10V CERM 402
C8112 0.1UF 20% 10V CERM 402
C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
C8115 0.1UF 20% 10V CERM 402
C8116 0.1UF 20% 10V CERM 402
C8117 0.1UF 20% 10V CERM 402
C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

OMIT
U8000
NB8P-GS-W-A2
BGA
(7 OF 8)

K16 K17 N13 N14 N16 N17 N19 P13 P14 P16 P17 P19 R16 R17 T13 T14 T15 T18 T19 U13 U14 U15 U18 U19 V16 V17 W13 W14 W16 W17 W19 Y13 Y14 Y16 Y17 Y19 Y20 → VDD

P20 T20 T23 U20 U23 W20 → VDD_LP

=PP1V8_GPU_FBVDDQ

A12 A18 A21 A24 A27 A3 A30 A6 A9 AA32 AD32 AG32 AK32 C32 F32 J32 M32 R32 → FBVDD

???A @ ???MHz 1.8V GDDR3

AA25 AA26 AB25 AB26 G11 G12 G15 G18 G21 G22 H11 H12 H15 H18 H21 H22 L25 L26 M25 M26 R25 R26 V25 V26 → FBVDDQ

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603
C8156 0.1UF 20% 10V CERM 402
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402
C8162 0.1UF 20% 10V CERM 402
C8163 0.1UF 20% 10V CERM 402
C8164 0.1UF 20% 10V CERM 402
C8165 0.1UF 20% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402
C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

AA23 AB23 H16 H17 J10 J23 J24 J9 K11 K12 K21 K22 K24 K9 L23 M23 T25 U25 → NC

FBVTT

TP_GPU_VDD_SENSE N20 → VDD_SENSE
TP_GPU_GND_SENSE M21 → GND_SENSE

OMIT
U8000
NB8P-GS-W-A2
BGA
(8 OF 8)

AE17 AE27 AE6 AF11 AF26 AF29 AF4 AF7 AG10 AG11 AB27 AB6 AC10 AC23 AC29 AC4 AD16 AD17 AD2 AD31 AA12 AA2 AA21 AA31 AG13 AG14 AG15 AG19 AG2 AG22 AG31 AG8 AH24 AJ10 AJ13 AJ16 AJ17 AJ20 AJ23 AJ26 AJ29 AJ4 AJ7 AK2 AK28 AK31 AL10 AL11 AL14 AL19 AL22 AL25 AL3 AL6 AL9 AM10 AM13 AM16 AM17 AM20 AM23 AM26 AM29 B12 B15 B18 B21 B24 B27 B3 B30 B6 B9 C2 C31 D10 D13 → GND

D16 D17 D20 D23 D26 D29 D4 D7 F11 F14 F19 F2 F22 F25 F31 F8 G26 G29 G4 G7 H27 H6 J16 J17 J2 J31 K10 K23 K29 K4 L27 L6 M12 M2 M31 N15 N18 N29 N4 P15 P18 P27 P6 R13 R14 R15 R18 R19 R2 R20 R31 T16 T17 T24 T29 T4 U16 U17 U24 U29 U8 V13 V14 V15 V18 V19 V2 V20 V31 W15 W18 W27 W6 Y15 Y18 Y29 Y4 → GND

NV G84M Core/FB Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	81	109

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8000
NB8P-GS-W-A2
BGA
(3 OF 8)

MEMORY INTERFACE A

FB_A_DQ<0> N27 FBAD0
FB_A_DQ<1> M27 FBAD1
FB_A_DQ<2> N28 FBAD2
FB_A_DQ<3> L29 FBAD3
FB_A_DQ<4> K27 FBAD4
FB_A_DQ<5> K28 FBAD5
FB_A_DQ<6> J29 FBAD6
FB_A_DQ<7> J28 FBAD7
FB_A_DQ<8> P30 FBAD8
FB_A_DQ<9> N31 FBAD9
FB_A_DQ<10> N30 FBAD10
FB_A_DQ<11> N32 FBAD11
FB_A_DQ<12> L31 FBAD12
FB_A_DQ<13> L30 FBAD13
FB_A_DQ<14> J30 FBAD14
FB_A_DQ<15> L32 FBAD15
FB_A_DQ<16> H30 FBAD16
FB_A_DQ<17> K30 FBAD17
FB_A_DQ<18> H31 FBAD18
FB_A_DQ<19> F30 FBAD19
FB_A_DQ<20> H32 FBAD20
FB_A_DQ<21> E31 FBAD21
FB_A_DQ<22> D30 FBAD22
FB_A_DQ<23> E30 FBAD23
FB_A_DQ<24> H28 FBAD24
FB_A_DQ<25> H29 FBAD25
FB_A_DQ<26> E29 FBAD26
FB_A_DQ<27> J27 FBAD27
FB_A_DQ<28> F27 FBAD28
FB_A_DQ<29> E27 FBAD29
FB_A_DQ<30> E28 FBAD30
FB_A_DQ<31> F28 FBAD31
FB_A_DQ<32> AD29 FBAD32
FB_A_DQ<33> AE29 FBAD33
FB_A_DQ<34> AD28 FBAD34
FB_A_DQ<35> AC28 FBAD35
FB_A_DQ<36> AB29 FBAD36
FB_A_DQ<37> AA30 FBAD37
FB_A_DQ<38> Y28 FBAD38
FB_A_DQ<39> AB30 FBAD39
FB_A_DQ<40> AM30 FBAD40
FB_A_DQ<41> AF30 FBAD41
FB_A_DQ<42> AJ31 FBAD42
FB_A_DQ<43> AJ30 FBAD43
FB_A_DQ<44> AJ32 FBAD44
FB_A_DQ<45> AK29 FBAD45
FB_A_DQ<46> AM31 FBAD46
FB_A_DQ<47> AL30 FBAD47
FB_A_DQ<48> AE32 FBAD48
FB_A_DQ<49> AE30 FBAD49
FB_A_DQ<50> AE31 FBAD50
FB_A_DQ<51> AD30 FBAD51
FB_A_DQ<52> AC31 FBAD52
FB_A_DQ<53> AC32 FBAD53
FB_A_DQ<54> AB32 FBAD54
FB_A_DQ<55> AB31 FBAD55
FB_A_DQ<56> AG27 FBAD56
FB_A_DQ<57> AF28 FBAD57
FB_A_DQ<58> AH28 FBAD58
FB_A_DQ<59> AG28 FBAD59
FB_A_DQ<60> AG29 FBAD60
FB_A_DQ<61> AD27 FBAD61
FB_A_DQ<62> AF27 FBAD62
FB_A_DQ<63> AE28 FBAD63

FBA_CMD0 P32 FB_A_LMA<4>
FBA_CMD1 U27 FB_A_RAS_L
FBA_CMD2 P31 FB_A_LMA<5>
FBA_CMD3 U30 FB_A_BA<1>
FBA_CMD4 Y31 FB_A_UMA<2>
FBA_CMD5 W32 FB_A_UMA<4>
FBA_CMD6 W31 FB_A_UMA<3>
FBA_CMD7 T32 FB_A_BA<2>
FBA_CMD8 V27 FB_A_CS0_L
FBA_CMD9 T28 FB_A_MA<11>
FBA_CMD10 T31 FB_A_CAS_L
FBA_CMD11 U32 FB_A_WE_L
FBA_CMD12 W29 FB_A_BA<0>
FBA_CMD13 W30 FB_A_UMA<5>
FBA_CMD14 T27 TP_FB_A_MA12
FBA_CMD15 V28 FB_A_DRAM_RST
FBA_CMD16 V30 FB_A_MA<7>
FBA_CMD17 U31 FB_A_MA<10>
FBA_CMD18 R27 FB_A_CKE
FBA_CMD19 V29 FB_A_MA<0>
FBA_CMD20 T30 FB_A_MA<9>
FBA_CMD21 W28 FB_A_MA<6>
FBA_CMD22 R29 FB_A_LMA<2>
FBA_CMD23 R30 FB_A_MA<8>
FBA_CMD24 P29 FB_A_LMA<3>
FBA_CMD25 U28 FB_A_MA<1>
FBA_CMD26 Y32 TP_FB_A_MA13
FBA_CMD27 Y30 TP_FBA_CMD27
FBA_CMD28 V32 TP_FBA_CMD28

FBA_CLK0 P28 FB_A_CLK_P<0>
FBA_CLK0_L R28 FB_A_CLK_N<0>
FBA_CLK1 Y27 FB_A_CLK_P<1>
FBA_CLK1_L AA27 FB_A_CLK_N<1>

FBADQM0 M29 FB_A_DQM_L<0>
FBADQM1 M30 FB_A_DQM_L<1>
FBADQM2 G30 FB_A_DQM_L<2>
FBADQM3 F29 FB_A_DQM_L<3>
FBADQM4 AA29 FB_A_DQM_L<4>
FBADQM5 AK30 FB_A_DQM_L<5>
FBADQM6 AC30 FB_A_DQM_L<6>
FBADQM7 AG30 FB_A_DQM_L<7>

READ STROBE
FBADQS_RN0 M28 FB_A_RDQS<0>
FBADQS_RN1 K32 FB_A_RDQS<1>
FBADQS_RN2 G31 FB_A_RDQS<2>
FBADQS_RN3 G27 FB_A_RDQS<3>
FBADQS_RN4 AA28 FB_A_RDQS<4>
FBADQS_RN5 AL31 FB_A_RDQS<5>
FBADQS_RN6 AF31 FB_A_RDQS<6>
FBADQS_RN7 AH29 FB_A_RDQS<7>

WRITE STROBE
FBADQS_WP0 L28 FB_A_WDQS<0>
FBADQS_WP1 K31 FB_A_WDQS<1>
FBADQS_WP2 G32 FB_A_WDQS<2>
FBADQS_WP3 G28 FB_A_WDQS<3>
FBADQS_WP4 AB28 FB_A_WDQS<4>
FBADQS_WP5 AL32 FB_A_WDQS<5>
FBADQS_WP6 AF32 FB_A_WDQS<6>
FBADQS_WP7 AH30 FB_A_WDQS<7>

FBA_DEBUG AC27 TP_FBA_DEBUG

FBA_PLLAVDD G25
FBA_PLLGND G24

FBCAL_PD_VDDQ K26 FBCAL_PD_VDDQ
FBCAL_PU_GND H26 FBCAL_PU_GND

R8200 10K 5% 1/16W MF-LF 402
R8201 10K 5% 1/16W MF-LF 402
R8290 45.3 1% 1/16W MF-LF 402
R8291 24.9 1% 1/16W MF-LF 402

PP1V2_GPU_FBA_PLL_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V

=PP1V2_GPU_FBPLLAVDD
L8200 FERR-220-OHM 0402
C8201 0.1UF 20% 10V CERM 402
C8200 4.7UF 20% 6.3V CERM 603

=PP1V8_GPU_FBIO

OMIT
U8000
NB8P-GS-W-A2
BGA
(4 OF 8)

MEMORY INTERFACE B

FB_B_DQ<0> B7 FBCD0
FB_B_DQ<1> A7 FBCD1
FB_B_DQ<2> C7 FBCD2
FB_B_DQ<3> A2 FBCD3
FB_B_DQ<4> B2 FBCD4
FB_B_DQ<5> C4 FBCD5
FB_B_DQ<6> A5 FBCD6
FB_B_DQ<7> B5 FBCD7
FB_B_DQ<8> F9 FBCD8
FB_B_DQ<9> F10 FBCD9
FB_B_DQ<10> D12 FBCD10
FB_B_DQ<11> D9 FBCD11
FB_B_DQ<12> E12 FBCD12
FB_B_DQ<13> D11 FBCD13
FB_B_DQ<14> E8 FBCD14
FB_B_DQ<15> D8 FBCD15
FB_B_DQ<16> E7 FBCD16
FB_B_DQ<17> F7 FBCD17
FB_B_DQ<18> D6 FBCD18
FB_B_DQ<19> D5 FBCD19
FB_B_DQ<20> D3 FBCD20
FB_B_DQ<21> E4 FBCD21
FB_B_DQ<22> C3 FBCD22
FB_B_DQ<23> B4 FBCD23
FB_B_DQ<24> C10 FBCD24
FB_B_DQ<25> B10 FBCD25
FB_B_DQ<26> C8 FBCD26
FB_B_DQ<27> A10 FBCD27
FB_B_DQ<28> C11 FBCD28
FB_B_DQ<29> C12 FBCD29
FB_B_DQ<30> A11 FBCD30
FB_B_DQ<31> B11 FBCD31
FB_B_DQ<32> B28 FBCD32
FB_B_DQ<33> C27 FBCD33
FB_B_DQ<34> C26 FBCD34
FB_B_DQ<35> B26 FBCD35
FB_B_DQ<36> C30 FBCD36
FB_B_DQ<37> B31 FBCD37
FB_B_DQ<38> C29 FBCD38
FB_B_DQ<39> A31 FBCD39
FB_B_DQ<40> D28 FBCD40
FB_B_DQ<41> D27 FBCD41
FB_B_DQ<42> F26 FBCD42
FB_B_DQ<43> D24 FBCD43
FB_B_DQ<44> E23 FBCD44
FB_B_DQ<45> E26 FBCD45
FB_B_DQ<46> E24 FBCD46
FB_B_DQ<47> F23 FBCD47
FB_B_DQ<48> B23 FBCD48
FB_B_DQ<49> A23 FBCD49
FB_B_DQ<50> C25 FBCD50
FB_B_DQ<51> C23 FBCD51
FB_B_DQ<52> A22 FBCD52
FB_B_DQ<53> C22 FBCD53
FB_B_DQ<54> C21 FBCD54
FB_B_DQ<55> B22 FBCD55
FB_B_DQ<56> E22 FBCD56
FB_B_DQ<57> D22 FBCD57
FB_B_DQ<58> D21 FBCD58
FB_B_DQ<59> E21 FBCD59
FB_B_DQ<60> E18 FBCD60
FB_B_DQ<61> D19 FBCD61
FB_B_DQ<62> D18 FBCD62
FB_B_DQ<63> E19 FBCD63

FBC_CMD0 C13 FB_B_LMA<4>
FBC_CMD1 A16 FB_B_RAS_L
FBC_CMD2 A13 FB_B_LMA<5>
FBC_CMD3 B17 FB_B_BA<1>
FBC_CMD4 B20 FB_B_UMA<2>
FBC_CMD5 A19 FB_B_UMA<4>
FBC_CMD6 B19 FB_B_UMA<3>
FBC_CMD7 B14 FB_B_BA<2>
FBC_CMD8 E16 FB_B_CS0_L
FBC_CMD9 A14 FB_B_MA<11>
FBC_CMD10 C15 FB_B_CAS_L
FBC_CMD11 B16 FB_B_WE_L
FBC_CMD12 F17 FB_B_BA<0>
FBC_CMD13 C19 FB_B_UMA<5>
FBC_CMD14 D15 TP_FB_B_MA12
FBC_CMD15 C17 FB_B_DRAM_RST
FBC_CMD16 A17 FB_B_MA<7>
FBC_CMD17 C16 FB_B_MA<10>
FBC_CMD18 D14 FB_B_CKE
FBC_CMD19 F16 FB_B_MA<0>
FBC_CMD20 C14 FB_B_MA<9>
FBC_CMD21 C18 FB_B_MA<6>
FBC_CMD22 E14 FB_B_LMA<2>
FBC_CMD23 B13 FB_B_MA<8>
FBC_CMD24 E15 FB_B_LMA<3>
FBC_CMD25 F15 FB_B_MA<1>
FBC_CMD26 A20 TP_FB_B_MA13
FBC_CMD27 C20 TP_FBC_CMD27
FBC_CMD28 A15 TP_FBC_CMD28

FBC_CLK0 E13 FB_B_CLK_P<0>
FBC_CLK0_L F13 FB_B_CLK_N<0>
FBC_CLK1 F18 FB_B_CLK_P<1>
FBC_CLK1_L E17 FB_B_CLK_N<1>

FBCDQM0 A4 FB_B_DQM_L<0>
FBCDQM1 E11 FB_B_DQM_L<1>
FBCDQM2 F5 FB_B_DQM_L<2>
FBCDQM3 C9 FB_B_DQM_L<3>
FBCDQM4 C28 FB_B_DQM_L<4>
FBCDQM5 F24 FB_B_DQM_L<5>
FBCDQM6 C24 FB_B_DQM_L<6>
FBCDQM7 E20 FB_B_DQM_L<7>

READ STROBE
FBCDQS_RN0 C6 FB_B_RDQS<0>
FBCDQS_RN1 E9 FB_B_RDQS<1>
FBCDQS_RN2 E6 FB_B_RDQS<2>
FBCDQS_RN3 A8 FB_B_RDQS<3>
FBCDQS_RN4 B29 FB_B_RDQS<4>
FBCDQS_RN5 E25 FB_B_RDQS<5>
FBCDQS_RN6 A25 FB_B_RDQS<6>
FBCDQS_RN7 F21 FB_B_RDQS<7>

WRITE STROBE
FBCDQS_WP0 C5 FB_B_WDQS<0>
FBCDQS_WP1 E10 FB_B_WDQS<1>
FBCDQS_WP2 E5 FB_B_WDQS<2>
FBCDQS_WP3 B8 FB_B_WDQS<3>
FBCDQS_WP4 A29 FB_B_WDQS<4>
FBCDQS_WP5 D25 FB_B_WDQS<5>
FBCDQS_WP6 B25 FB_B_WDQS<6>
FBCDQS_WP7 F20 FB_B_WDQS<7>

FBC_DEBUG F12 TP_FBC_DEBUG

NC G10 FBC_PLLAVDD
NC G9 FBC_PLLGND

FBCAL_TERM_GND J26 FBCAL_TERM GND
FB_VREF E32 GPU_FB_VREF

R8250 10K 5% 1/16W MF-LF 402
R8251 10K 5% 1/16W MF-LF 402
R8292 40.2 1% 1/16W MF-LF 402

=PP1V8_GPU_FBIO
R8295 1.07K 1% 1/16W MF-LF 402
C8296 0.1uF 10% 10V X5R 402
R8297 1.02K 1% 1/16W MF-LF 402
R8296 2.49K 1% 1/16W MF-LF 402

GPU_FB_VREF_UNTERM_L
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

Q8295 2N7002DW-X-F SOT-363
FB_VREF_UNTERM

NV G84M Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE INC.

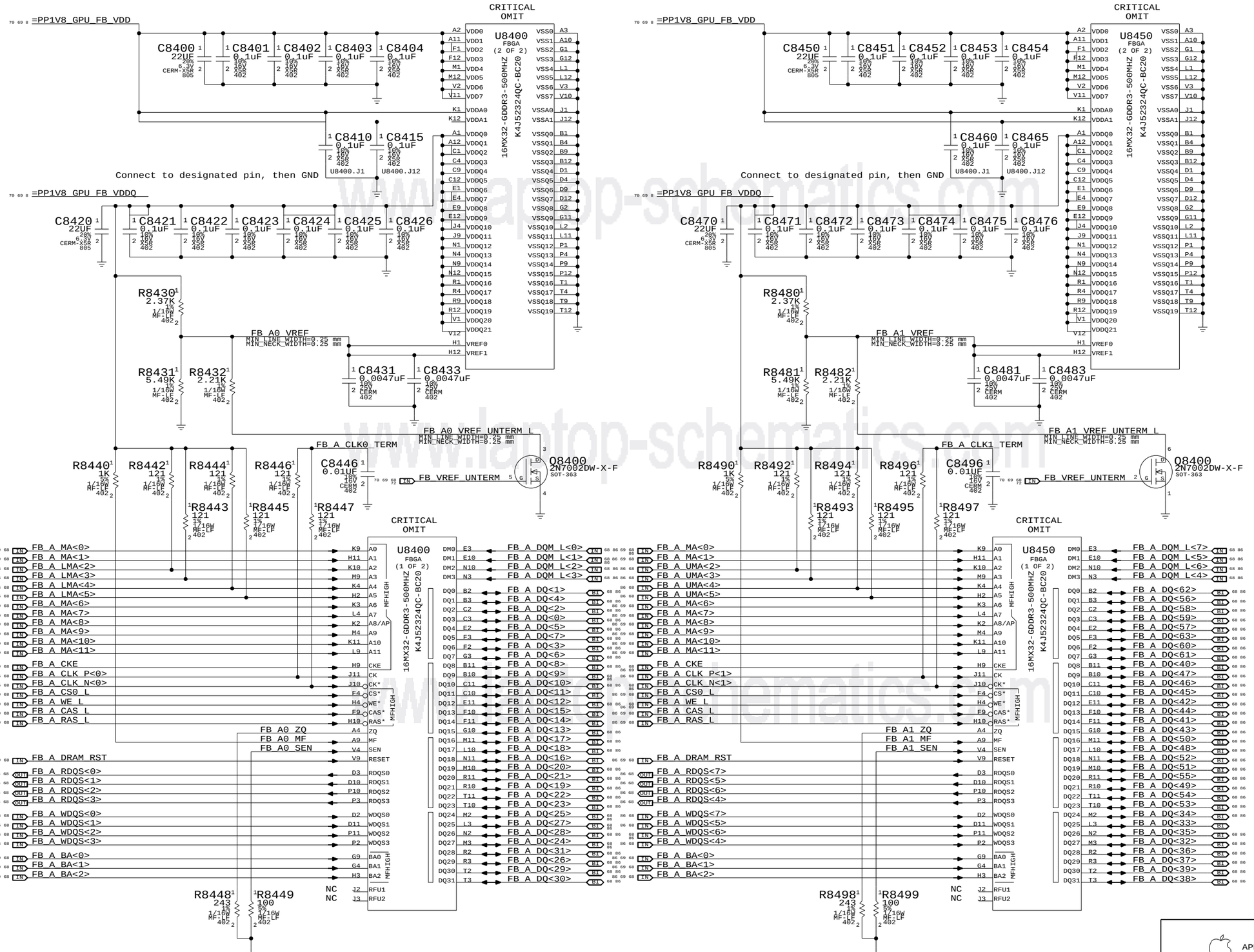
SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 82 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 84 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_GPU_FB_VDD

=PP1V8_GPU_FB_VDDQ

Connect to designated pin, then GND

CRITICAL
OMIT

U8500
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

U8550
FBGA
(1 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

C8500 C8501 C8502 C8503 C8504 C8510 C8515
C8520 C8521 C8522 C8523 C8524 C8525 C8526
C8530 C8531 C8533
C8540 C8542 C8544 C8546 C8543 C8545 C8547 C8548 C8549
C8550 C8551 C8552 C8553 C8554 C8560 C8565
C8570 C8571 C8572 C8573 C8574 C8575 C8576
C8580 C8581 C8582 C8583
C8590 C8592 C8594 C8596 C8593 C8595 C8597 C8598 C8599

FB_B0_VREF
FB_B1_VREF
FB_B_CLK0_TERM
FB_B_CLK1_TERM
FB_B0_VREF_UNTERM_L
FB_B1_VREF_UNTERM_L
FB_VREF_UNTERM

Q8500
2N7002DW-X-F
SOT-363

FB_B0_ZQ
FB_B0_MF
FB_B0_SEN
FB_B1_ZQ
FB_B1_MF
FB_B1_SEN

FB_B_MA<0>
FB_B_MA<1>
FB_B_LMA<2>
FB_B_LMA<3>
FB_B_LMA<4>
FB_B_LMA<5>
FB_B_MA<6>
FB_B_MA<7>
FB_B_MA<8>
FB_B_MA<9>
FB_B_MA<10>
FB_B_MA<11>
FB_B_CKE
FB_B_CLK_P<0>
FB_B_CLK_N<0>
FB_B_CS0_L
FB_B_WE_L
FB_B_CAS_L
FB_B_RAS_L
FB_B_DRAM_RST
FB_B_RDQS<2>
FB_B_RDQS<1>
FB_B_RDQS<3>
FB_B_RDQS<0>
FB_B_WDQS<2>
FB_B_WDQS<1>
FB_B_WDQS<3>
FB_B_WDQS<0>
FB_B_BA<0>
FB_B_BA<1>
FB_B_BA<2>

FB_B_DQM_L<2>
FB_B_DQM_L<1>
FB_B_DQM_L<3>
FB_B_DQM_L<0>
FB_B_DQ<18>
FB_B_DQ<17>
FB_B_DQ<19>
FB_B_DQ<16>
FB_B_DQ<21>
FB_B_DQ<23>
FB_B_DQ<20>
FB_B_DQ<22>
FB_B_DQ<8>
FB_B_DQ<12>
FB_B_DQ<9>
FB_B_DQ<10>
FB_B_DQ<13>
FB_B_DQ<14>
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FB_B_DQ<1>
FB_B_DQ<6>
FB_B_DQ<0>
FB_B_DQ<7>
FB_B_DQ<4>
FB_B_DQ<5>
FB_B_DQ<3>

FB_B_MA<0>
FB_B_MA<1>
FB_B_UMA<2>
FB_B_UMA<3>
FB_B_UMA<4>
FB_B_UMA<5>
FB_B_MA<6>
FB_B_MA<7>
FB_B_MA<8>
FB_B_MA<9>
FB_B_MA<10>
FB_B_MA<11>
FB_B_CKE
FB_B_CLK_P<1>
FB_B_CLK_N<1>
FB_B_CS0_L
FB_B_WE_L
FB_B_CAS_L
FB_B_RAS_L
FB_B_DRAM_RST
FB_B_RDQS<6>
FB_B_RDQS<5>
FB_B_RDQS<4>
FB_B_RDQS<7>
FB_B_WDQS<6>
FB_B_WDQS<5>
FB_B_WDQS<4>
FB_B_WDQS<7>
FB_B_BA<0>
FB_B_BA<1>
FB_B_BA<2>

FB_B_DQM_L<6>
FB_B_DQM_L<5>
FB_B_DQM_L<4>
FB_B_DQM_L<7>
FB_B_DQ<49>
FB_B_DQ<50>
FB_B_DQ<48>
FB_B_DQ<51>
FB_B_DQ<52>
FB_B_DQ<55>
FB_B_DQ<54>
FB_B_DQ<53>
FB_B_DQ<40>
FB_B_DQ<42>
FB_B_DQ<41>
FB_B_DQ<45>
FB_B_DQ<43>
FB_B_DQ<46>
FB_B_DQ<47>
FB_B_DQ<44>
FB_B_DQ<36>
FB_B_DQ<39>
FB_B_DQ<37>
FB_B_DQ<38>
FB_B_DQ<34>
FB_B_DQ<32>
FB_B_DQ<35>
FB_B_DQ<33>
FB_B_DQ<63>
FB_B_DQ<58>
FB_B_DQ<61>
FB_B_DQ<59>
FB_B_DQ<62>
FB_B_DQ<56>
FB_B_DQ<60>
FB_B_DQ<57>

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	85	109

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8000
NB8P-GS-W-A2
BGA
(6 OF 8)

=PP3V3_GPU_VDD33 Typically <??mA

C8600 0.47UF 10% 6.3V CERM-X5R 402
C8601 0.47UF 10% 6.3V CERM-X5R 402
C8602 0.47UF 10% 6.3V CERM-X5R 402

AC11 VDD33_1
AC12 VDD33_2
AC24 VDD33_3
AD24 VDD33_4
AE11 VDD33_5
AE12 VDD33_6
H7 VDD33_7
J7 VDD33_8
K7 VDD33_9
L10 VDD33_10
L7 VDD33_11
L8 VDD33_12
M10 VDD33_13

GPIO0 K3 GPU_GPIO_0
GPIO1 H1 GPU_GPIO_1
GPIO2 K5 GPU_GPIO_2
GPIO3 G5 GPU_GPIO_3
GPIO4 E2 GPU_GPIO_4
GPIO5 J5 GPU_GPIO_5
GPIO6 G6 GPU_GPIO_6
GPIO7 K6 GPU_GPIO_7
GPIO8 E1 GPU_GPIO_8
GPIO9 D2 GPU_GPIO_9
GPIO10 H5 GPU_GPIO_10
GPIO11 F4 GPU_GPIO_11
GPIO12 E3 GPU_GPIO_12
GPIO13 U3 GPU_GPIO_13
GPIO14 U4 GPU_GPIO_14

GPU_ROM_CS_L AA4 ROMCS_L
GPU_ROM_SCLK AA7 ROM_SCLK
GPU_ROM_SI W2 ROM_SI
GPU_ROM_SO AA6 ROM_SO

R8695 100K 5% 1/16W MF-LF 402
R8696 10K 5% 1/16W MF-LF 402

GPU_TESTMODE_PD H2 TESTMODE
GPU_SWAPRDY_A M6 SWAPRDY_A

SPDIF J6 GPU_SPDIF
STEREO T3 GPU_STEREO
BUFRST_L F3 TP_GPU_BUFRST_L

JTAG_TCK AJ11 TP_GPU_JTAG_TCK
JTAG_TDI AK12 TP_GPU_JTAG_TDI
JTAG_TDO AL12 TP_GPU_JTAG_TDO
JTAG_TMS AK11 TP_GPU_JTAG_TMS
(IPD) JTAG_TRST_L AL13 TP_GPU_JTAG_TRST_L

=PP3V3_GPU_MIO

C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402

M7 MIOA_VDDQ_1
M8 MIOA_VDDQ_2
R8 MIOA_VDDQ_3
T8 MIOA_VDDQ_4
U9 MIOA_VDDQ_5
AA8 MIOB_VDDQ_1
AB7 MIOB_VDDQ_2
AB8 MIOB_VDDQ_3
AC6 MIOB_VDDQ_4
AC7 MIOB_VDDQ_5

MIOA_CLKOUT R4 GPU_MIOA_CLKOUT_P
MIOA_CLKOUT_L P4 GPU_MIOA_CLKOUT_N
MIOA_CTL3 P3 GPU_MIOA_CTL3
MIOA_DE P1 GPU_MIOA_DE
MIOAD0 P2 GPU_MIOA_D<0>
MIOAD1 N2 GPU_MIOA_D<1>
MIOAD2 N1 GPU_MIOA_D<2>
MIOAD3 N3 GPU_MIOA_D<3>
MIOAD4 M1 GPU_MIOA_D<4>
MIOAD5 M3 GPU_MIOA_D<5>
MIOAD6 P5 GPU_MIOA_D<6>
MIOAD7 N6 GPU_MIOA_D<7>
MIOAD8 N5 GPU_MIOA_D<8>
MIOAD9 M4 GPU_MIOA_D<9>
MIOAD10 L4 GPU_MIOA_D<10>
MIOAD11 L5 GPU_MIOA_D<11>
MIOA_HSYNC R3 GPU_MIOA_HSYNC
MIOA_VSYNC R1 GPU_MIOA_VSYNC

=PP3V3_GPU_MIO

R8620 49.9 1% 1/10W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402

GPU_MIOA_PD_VDDQ
GPU_MIOB_PD_VDDQ
GPU_MIOA_PU_GND
GPU_MIOB_PU_GND

R8622 49.9 1% 1/10W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402

R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
R8619 10K 5% 1/16W MF-LF 402

C8617 0.1uF 10% 16V X5R 402
C8619 0.1uF 10% 16V X5R 402

GPU_MIOA_VREF L2 MIOA_VREF
GPU_MIOB_VREF Y2 MIOB_VREF

GPU_MIOA_PD_VDDQ L1 MIOACAL_PD_VDDQ
GPU_MIOA_PU_GND L3 MIOACAL_PU_GND

GPU_MIOB_PD_VDDQ Y1 MIOBCAL_PD_VDDQ
GPU_MIOB_PU_GND Y3 MIOBCAL_PU_GND

MIOB_CLKIN AE4 GPU_MIOB_CLKIN
MIOB_CLKOUT AD4 GPU_MIOB_CLKOUT_P
MIOB_CLKOUT_L AD5 GPU_MIOB_CLKOUT_N
MIOB_CTL3 AD3 GPU_MIOB_CTL3
MIOB_DE AD1 GPU_MIOB_DE
MIOBD0 AC3 GPU_MIOB_D<0>
MIOBD1 AC1 GPU_MIOB_D<1>
MIOBD2 AC2 GPU_MIOB_D<2>
MIOBD3 AB2 GPU_MIOB_D<3>
MIOBD4 AB1 GPU_MIOB_D<4>
MIOBD5 AA1 GPU_MIOB_D<5>
MIOBD6 AB3 GPU_MIOB_D<6>
MIOBD7 AA3 GPU_MIOB_D<7>
MIOBD8 AC5 GPU_MIOB_D<8>
MIOBD9 AB5 GPU_MIOB_D<9>
MIOBD10 AB4 GPU_MIOB_D<10>
MIOBD11 AA5 GPU_MIOB_D<11>
MIOB_HSYNC AF3 GPU_MIOB_HSYNC
MIOB_VSYNC AE3 GPU_MIOB_VSYNC

=PP1V2_GPU_PLLVDD

L8630 FERR-220-OHM 0402
PP1V2_GPU_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V 40mA

C8633 4.7UF 20% 6.3V CERM 603
C8630 4.7UF 20% 6.3V CERM 603
C8631 0.1uF 10% 16V X5R 402

T9 PLLVDD
U10 PLLGND
G23 H_PLLVDD
T10 VID_PLLVDD

=PP1V2_GPU_H_PLLVDD

L8635 FERR-220-OHM 0402
PP1V2_GPU_H_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V 40mA

C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 0.1uF 10% 16V X5R 402

GPU_XTALIN U1 XTALIN
GPU_XTALOUT U2 XTALOUT
GPU_XTALOUTBUFF T2 XTALOUTBUFF
GPU_XTALSSIN T1 XTALSSIN

=PP1V2_GPU_VID_PLLVDD

L8640 FERR-220-OHM 0402
PP1V2_GPU_VID_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V 40mA

C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 0.1uF 10% 16V X5R 402

THERMDP K1 GPU_THERMD_P
THERMDN J1 GPU_THERMD_N

NV G84M GPIO/MIO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 86 OF 109	

GPIOs

	Native Func		
GPU_GPIO_0	HPD0	GPU_HPD	IN 76
GPU_GPIO_1	HPD1	NC_GPU_GPIO_1	
GPU_GPIO_2	LCD0_BL_PWM	GPU_BL_PWM	OUT 77
GPU_GPIO_3	LCD0_VDD	GPU_PANEL_EN	OUT 77
GPU_GPIO_4	LCD0_BL_EN	GPU_BKLT_EN	OUT 77
GPU_GPIO_5	VID0	GPU_VCORE_VID0	OUT 74
GPU_GPIO_6	VID1	GPU_VCORE_VID1	OUT 74
GPU_GPIO_7	MEM_VID	GPU_VGA_EN_L	72
GPU_GPIO_8	THERM	NC_GPU_GPIO_8	
GPU_GPIO_9	FAN_PWM	TP_GPU_GSTATE<0>	
GPU_GPIO_10	MEM_VREF	FB_VREF_UNTERM	OUT 68 69 70
GPU_GPIO_11	SLI_SYNC	GPU_VCORE_VID2	OUT 74
GPU_GPIO_12	AC_DET	TP_GPU_GSTATE<1>	
GPU_GPIO_13	PWR_CTL0	GPU_VCORE_PWRCTL0	OUT 74
GPU_GPIO_14	PWR_CTL1	GPU_VCORE_PWRCTL1	OUT 74

Config Straps

72 71 8 =PP3V3_GPU_MIO

	VRAM_SAMSUNG		VRAM_128	NO STUFF		NO STUFF	NO STUFF	NO STUFF	NO STUFF
	R8720[1]	R8722[1]	R8724[1]	R8726[1]	R8728[1]	R8729[1]	R8730[1]	R8731[1]	R8732[1]
	10K	10K	10K	10K	1K	1K	1K	1K	1K
	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402

Supported straps:

RAMCFG0	71 GPU_MIOB_D<0>								
RAMCFG1	71 GPU_MIOB_D<1>								
RAMCFG2	71 GPU_MIOB_D<8>								
RAMCFG3	71 GPU_MIOB_D<9>								
3GIO_PADCFG0	71 GPU_MIOA_D<6>								
3GIO_PADCFG1	71 GPU_MIOA_D<8>								
3GIO_PADCFG2	71 GPU_MIOA_D<9>								
3GIO_PADCFG3	71 GPU_MIOB_HSYNC								
PEX_PLL_EN_TERM	71 GPU_MIOA_D<0>								
SUBVENDOR (BIOS ROM PRESENT)	71 GPU_MIOA_D<1>								
PCI_DEVID<2..0>									

	VRAM_HYNIX	NO STUFF	VRAM_256		
	R8721[1]	R8723[1]	R8725[1]	R8727[1]	R8733[1]
	10K	10K	10K	10K	1K
	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402

72 71 8 =PP3V3_GPU_MIO

R8735[1]	R8736[1]	R8737[1]	
1K	1K	1K	
5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	5% 1/16W MF-LF 402	
PCI_DEVID2	71 GPU_MIOB_D<3>		
PCI_DEVID1	71 GPU_MIOB_D<5>		
PCI_DEVID0	71 GPU_MIOB_D<4>		

Straps not supported:

USER<3..0>	MIOA_D<5..2>
SLOT_CLOCK_CFG	MIOA_HSYNC
PCI_IOBAR	MIOB_D<7>
BAR2_SIZE	MIOB_DE
ROMTYPE<1..0>	MIOB_VSYNC, MIOB_D<10>
PCI_DEVID<4..3>	MIOB_CTL3, MIOB_D<11>

Analog Video Mux

8 =PP3V3_GPU_VIDEOMUX

C8700 0.1UF 1 2 20% 10V CERM 402

CRITICAL OMIT

U8700 QFN TS3V330 VCC 16

86 73 IN GPU_VGA_R	R8740[1] 150 1% 1/10W MF-LF 402	R8741[1] 150 1% 1/10W MF-LF 402	R8742[1] 150 1% 1/10W MF-LF 402	Place Rs near GPU
86 73 IN GPU_VGA_G				
86 73 IN GPU_VGA_B				
86 73 IN GPU_TV_C	R8743[1] 150 1% 1/10W MF-LF 402	R8744[1] 150 1% 1/10W MF-LF 402	R8745[1] 150 1% 1/10W MF-LF 402	Place Rs near GPU
86 73 IN GPU_TV_Y				
86 73 IN GPU_TV_COMP				

S1A 2	DA 4	GPU_TV_C_VGA_R	OUT 76 86
S2A 3	DB 7	GPU_TV_Y_VGA_G	OUT 76 86
S1B 5	DC 9	GPU_TV_COMP_VGA_B	OUT 76 86
S2B 6	DD 12	NC	
S1C 11	IN 1	GPU_VGA_EN_L	72
S2C 10	EN_L 15		
S1D 14			
S2D 13			
THRML PAD 17	GND 8		

R8700 10K 5% 1/16W MF-LF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1718	1	IC,TS3V340,QUAD VIDEO SW,QFN16	U8700	CRITICAL	

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1579	353S1718		ALL (U8700)	TS3V330 alt to TS3V340

Renamed signals

86 30 GPU_CLK27M_GATED	MAKE_BASE=TRUE	GPU_XTALIN 71
86 30 GPU_CLK27M_SS_GATED	MAKE_BASE=TRUE	GPU_XTALSSIN 71 72
87 51 GPU_TDIODE_P	MAKE_BASE=TRUE	GPU_THERMD_P 71
51 GPU_TDIODE_N	MAKE_BASE=TRUE	GPU_THERMD_N 71
76 GPU_DVI_DDC_CLK	MAKE_BASE=TRUE	GPU_I2CB_SCL 73
76 GPU_DVI_DDC_DATA	MAKE_BASE=TRUE	GPU_I2CB_SDA 73
77 GPU_PANEL_DDC_CLK	MAKE_BASE=TRUE	GPU_I2CC_SCL 73
77 GPU_PANEL_DDC_DATA	MAKE_BASE=TRUE	GPU_I2CC_SDA 73

Unused I2C Buses

NC_GPU_I2CA_SCL	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_I2CA_SCL 73
NC_GPU_I2CA_SDA	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_I2CA_SDA 73

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

HDCP Support

8 =PP3V3_GPU_HDCP

HDCP R8770[1] 10K 5% 1/16W MF-LF 402

HDCP C8770 0.1UF 1 2 20% 10V CERM 402

HDCP CRITICAL

U8770 AT88SC080C SO1

73 BI GPU_I2CH_SCL	SCL 6	NC 7	
73 BI GPU_I2CH_SDA	SDA 5		
	NC 3		
	NC 2	NC 1	
	GND 4		

HDCP R8771[1] 10K 5% 1/16W MF-LF 402 NC

TMDS Backdrive Protection

CRITICAL Q8790 SI2305DS SOT-23

8 =PP3V3_GPU_TMDS — 3 D, G, S 2 — =PP3V3_GPU_TMDS_FET 8

[1]R8790 10K 5% 1/16W MF-LF 402

GPU_TMDS_PWREN_L

Q8925 2N7002DW-X-F SOT-363

74 65 IN =GPUVCORE_EN

R8791[1] 100K 5% 1/10W MF-LF 402

Unused signals

NC_GPU_XTALOUT	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_XTALOUT 71
NC_GPU_SPDIF	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_SPDIF 71
NC_GPU_STEREO	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_STEREO 71
NC_FB_A_MA12	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FB_A_MA12 68
NC_FB_B_MA12	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FB_B_MA12 68
NC_FB_A_MA13	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FB_A_MA13 68
NC_FB_B_MA13	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FB_B_MA13 68
NC_FBA_CMD27	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FBA_CMD27 68
NC_FBC_CMD27	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FBC_CMD27 68
NC_FBA_CMD28	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FBA_CMD28 68
NC_FBC_CMD28	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FBC_CMD28 68
NC_GPU_ROM_CS_L	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_ROM_CS_L 71
NC_GPU_ROM_SCLK	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_ROM_SCLK 71
NC_GPU_ROM_SI	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_ROM_SI 71
NC_GPU_ROM_SO	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_ROM_SO 71
NC_GPU_CSYNC	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_CSYNC 73
NC_GPU_R2	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_R2 73
NC_GPU_G2	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_G2 73
NC_GPU_B2	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_B2 73
NC_GPU_H2SYNC	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_H2SYNC 73
NC_GPU_V2SYNC	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_V2SYNC 73
NC_LVDS_U_DATAP<3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_U_DATA_P<3> 73 86
NC_LVDS_U_DATAN<3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_U_DATA_N<3> 73 86
NC_LVDS_L_DATAP<3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_L_DATA_P<3> 73 86
NC_LVDS_L_DATAN<3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_L_DATA_N<3> 73 86
TP_GPU_MIOA_CLKOUT_P	MAKE_BASE=TRUE	GPU_MIOA_CLKOUT_P 71
TP_GPU_MIOA_CLKOUT_N	MAKE_BASE=TRUE	GPU_MIOA_CLKOUT_N 71
TP_GPU_MIOA_CTL3	MAKE_BASE=TRUE	GPU_MIOA_CTL3 71
TP_GPU_MIOA_DE	MAKE_BASE=TRUE	GPU_MIOA_DE 71
TP_GPU_MIOA_D<5..2>	MAKE_BASE=TRUE	GPU_MIOA_D<5..2> 71
TP_GPU_MIOA_D<7>	MAKE_BASE=TRUE	GPU_MIOA_D<7> 71
TP_GPU_MIOA_D<11..10>	MAKE_BASE=TRUE	GPU_MIOA_D<11..10> 71
TP_GPU_MIOA_HSYNC	MAKE_BASE=TRUE	GPU_MIOA_HSYNC 71
TP_GPU_MIOA_VSYNC	MAKE_BASE=TRUE	GPU_MIOA_VSYNC 71
TP_GPU_MIOB_CLKIN	MAKE_BASE=TRUE	GPU_MIOB_CLKIN 71
TP_GPU_MIOB_CLKOUT_P	MAKE_BASE=TRUE	GPU_MIOB_CLKOUT_P 71
TP_GPU_MIOB_CLKOUT_N	MAKE_BASE=TRUE	GPU_MIOB_CLKOUT_N 71
TP_GPU_MIOB_DE	MAKE_BASE=TRUE	GPU_MIOB_DE 71
TP_GPU_MIOB_CTL3	MAKE_BASE=TRUE	GPU_MIOB_CTL3 71
TP_GPU_MIOB_D<2>	MAKE_BASE=TRUE	GPU_MIOB_D<2> 71
TP_GPU_MIOB_D<7..6>	MAKE_BASE=TRUE	GPU_MIOB_D<7..6> 71
TP_GPU_MIOB_D<11..10>	MAKE_BASE=TRUE	GPU_MIOB_D<11..10> 71
TP_GPU_MIOB_VSYNC	MAKE_BASE=TRUE	GPU_MIOB_VSYNC 71
NC_GPU_IFPD_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_IFPD_CLK_P 73
NC_GPU_IFPD_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_IFPD_CLK_N 73

Unused Clocks

72 71 GPU_XTALSSIN
71 GPU_XTALOUTBUFF

R8780[1] 10K 5% 1/16W MF-LF 402

GPU_SS_INT R8781[1] 10K 5% 1/16W MF-LF 402

GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 87 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

=PP1V8_GPU_IFPX

L8800 FERR-220-OHM 0402
20mA peak per diff pair
160mA peak for all pairs
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402 — Place at AF9
C8803 0.1UF 20% 10V CERM 402 — Place at AF8

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

L8805 FERR-220-OHM 0402
40mA peak
C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPAB_VPROBE
GPU_IFPAB_RSET

=PP3V3_GPU_IFPCD_IOVDD

L8810 FERR-220-OHM 0402
20mA peak per diff pair
200mA peak for all pairs
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402 — Place at AD6
C8813 0.1UF 20% 10V CERM 402 — Place at AE7

PP3V3_GPU_IFPCD_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

L8815 FERR-220-OHM 0402
40mA peak
C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPCD_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPCD_VPROBE
GPU_IFPCD_RSET

Sum of peak currents: 390mA

=PP3V3_GPU_DAC

L8820 FERR-220-OHM 0402
120mA peak
C8820 4.7UF 20% 6.3V CERM 603
C8821 0.1UF 20% 10V CERM 402

PP3V3_GPU_DACA_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

GPU_DACA_VREF
GPU_DACA_RSET

L8830 FERR-220-OHM 0402
150mA peak
C8830 4.7UF 20% 6.3V CERM 603
C8831 0.1UF 20% 10V CERM 402

PP3V3_GPU_DACB_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

GPU_DACB_VREF
GPU_DACB_RSET

NO STUFF
L8840 FERR-220-OHM 0402
120mA peak
NO STUFF C8840 4.7UF 20% 6.3V CERM 603
C8841 0.1UF 20% 10V CERM 402
C8845 4.7UF 20% 6.3V CERM 603

PP3V3_GPU_DACC_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

GPU_DACC_VREF
GPU_DACC_RSET

GPU_I2CC_SCL
GPU_I2CC_SDA
GPU_I2CH_SCL
GPU_I2CH_SDA
=GPU_I2CS_SCL
=GPU_I2CS_SDA

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

OMIT
U8000 NB8P-GS-W-A2 BGA (5 OF 8)

AF9	IFPA_IOVDD	IFPA_TXC AK9	LVDS_L_CLK_P
AF8	IFPB_IOVDD	IFPA_TXC_L AJ9	LVDS_L_CLK_N
		IFPA_TXD0 AH6	LVDS_L_DATA_P<0>
		IFPA_TXD0_L AJ6	LVDS_L_DATA_N<0>
		IFPA_TXD1 AH8	LVDS_L_DATA_P<1>
		IFPA_TXD1_L AH7	LVDS_L_DATA_N<1>
		IFPA_TXD2 AJ8	LVDS_L_DATA_P<2>
		IFPA_TXD2_L AK8	LVDS_L_DATA_N<2>
		IFPA_TXD3 AJ5	LVDS_L_DATA_P<3>
		IFPA_TXD3_L AH5	LVDS_L_DATA_N<3>
AC9	IFPAB_PLLVDD		
AD9	IFPAB_PLLGND		
AM4	IFPAB_VPROBE		
AL5	IFPAB_RSET		
		IFPB_TXC AK4	LVDS_U_CLK_P
		IFPB_TXC_L AL4	LVDS_U_CLK_N
		IFPB_TXD4 AM6	LVDS_U_DATA_P<0>
		IFPB_TXD4_L AM5	LVDS_U_DATA_N<0>
		IFPB_TXD5 AM7	LVDS_U_DATA_P<1>
		IFPB_TXD5_L AL7	LVDS_U_DATA_N<1>
		IFPB_TXD6 AK6	LVDS_U_DATA_P<2>
		IFPB_TXD6_L AK5	LVDS_U_DATA_N<2>
		IFPB_TXD7 AK7	LVDS_U_DATA_P<3>
		IFPB_TXD7_L AL8	LVDS_U_DATA_N<3>
AD6	IFPC_IOVDD	IFPC_TXC AM2	TMDS_CLK_P
AE7	IFPD_IOVDD	IFPC_TXC_L AM3	TMDS_CLK_N
		IFPC_TXD0 AE2	TMDS_DATA_P<0>
		IFPC_TXD0_L AE1	TMDS_DATA_N<0>
		IFPC_TXD1 AF1	TMDS_DATA_P<1>
		IFPC_TXD1_L AF2	TMDS_DATA_N<1>
		IFPC_TXD2 AG1	TMDS_DATA_P<2>
		IFPC_TXD2_L AH1	TMDS_DATA_N<2>
		IFPD_TXC AG3	GPU_IFPD_CLK_P
		IFPD_TXC_L AH2	GPU_IFPD_CLK_N
		IFPD_TXD4 AK1	TMDS_DATA_P<3>
		IFPD_TXD4_L AJ1	TMDS_DATA_N<3>
		IFPD_TXD5 AL2	TMDS_DATA_P<4>
		IFPD_TXD5_L AL1	TMDS_DATA_N<4>
		IFPD_TXD6 AJ2	TMDS_DATA_P<5>
		IFPD_TXD6_L AJ3	TMDS_DATA_N<5>
AA10	IFPCD_PLLVDD		
AB10	IFPCD_PLLGND		
AK3	IFPCD_VPROBE		
AH3	IFPCD_RSET		
AD10	DACA_VDD	DACA_RED AH11	GPU_VGA_R
AG9	DACA_IDUMP	DACA_GREEN AJ12	GPU_VGA_G
AH10	DACA_VREF	DACA_BLUE AH12	GPU_VGA_B
AH9	DACA_RSET	DACA_HSYNC AF10	GPU_VGA_HSYNC
		DACA_VSYNC AK10	GPU_VGA_VSYNC
V8	DACB_VDD	DACB_RED R6	GPU_TV_C
V7	DACB_IDUMP	DACB_GREEN T5	GPU_TV_Y
R5	DACB_VREF	DACB_BLUE T6	GPU_TV_COMP
R7	DACB_RSET	DACB_CSYNC U5	GPU_CSYNC
AD7	DACC_VDD	DACC_RED AF6	GPU_R2
AG4	DACC_IDUMP	DACC_GREEN AG6	GPU_G2
AH4	DACC_VREF	DACC_BLUE AE5	GPU_B2
AF5	DACC_RSET	DACC_HSYNC AG7	GPU_H2SYNC
		DACC_VSYNC AG5	GPU_V2SYNC
G2	I2CC_SCL	I2CA_SCL K2	GPU_I2CA_SCL
G1	I2CC_SDA	I2CA_SDA J3	GPU_I2CA_SDA
G3	I2CH_SCL	I2CB_SCL H4	GPU_I2CB_SCL
H3	I2CH_SDA	I2CB_SDA J4	GPU_I2CB_SDA
C1	I2CS_SCL		
B1	I2CS_SDA		

Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb

GPU_IFPAB_RSET
GPU_IFPCD_RSET
GPU_DACA_RSET
GPU_DACB_RSET
GPU_DACC_RSET
NO STUFF R8850 1K 1% 1/16W ME-LF 402
NO STUFF R8851 1K 1% 1/16W ME-LF 402
R8852 124 1% 1/16W ME-LF 402
R8853 124 1% 1/16W ME-LF 402
R8854 124 1% 1/16W ME-LF 402

GPU_DACA_VREF
GPU_DACB_VREF
GPU_DACC_VREF
C8852 0.1UF 20% 10V CERM 402
C8853 0.1UF 20% 10V CERM 402
C8854 0.1UF 20% 10V CERM 402

GPU_IFPAB_VPROBE
GPU_IFPCD_VPROBE
NO STUFF C8855 0.01UF 20% 16V CERM 402
NO STUFF C8856 0.01UF 20% 16V CERM 402

NV G84M Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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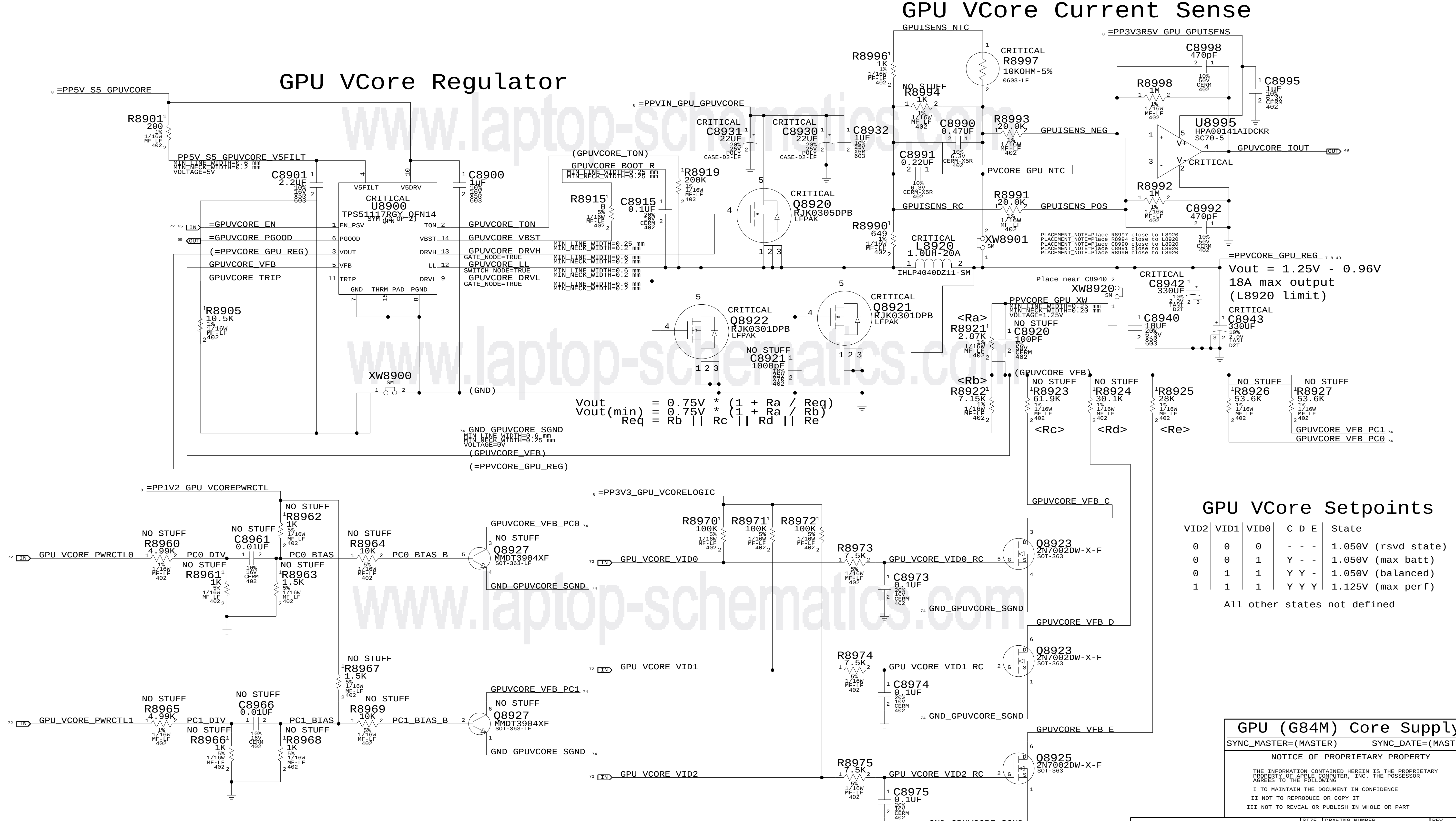
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 88 OF 109	

GPU VCore Regulator

GPU VCore Current Sense



GPU VCore Setpoints

VID2	VID1	VID0	C D E	State
0	0	0	- - -	1.050V (rsvd state)
0	0	1	Y - -	1.050V (max batt)
0	1	1	Y Y -	1.050V (balanced)
1	1	1	Y Y Y	1.125V (max perf)

All other states not defined

GPU (G84M) Core Supply

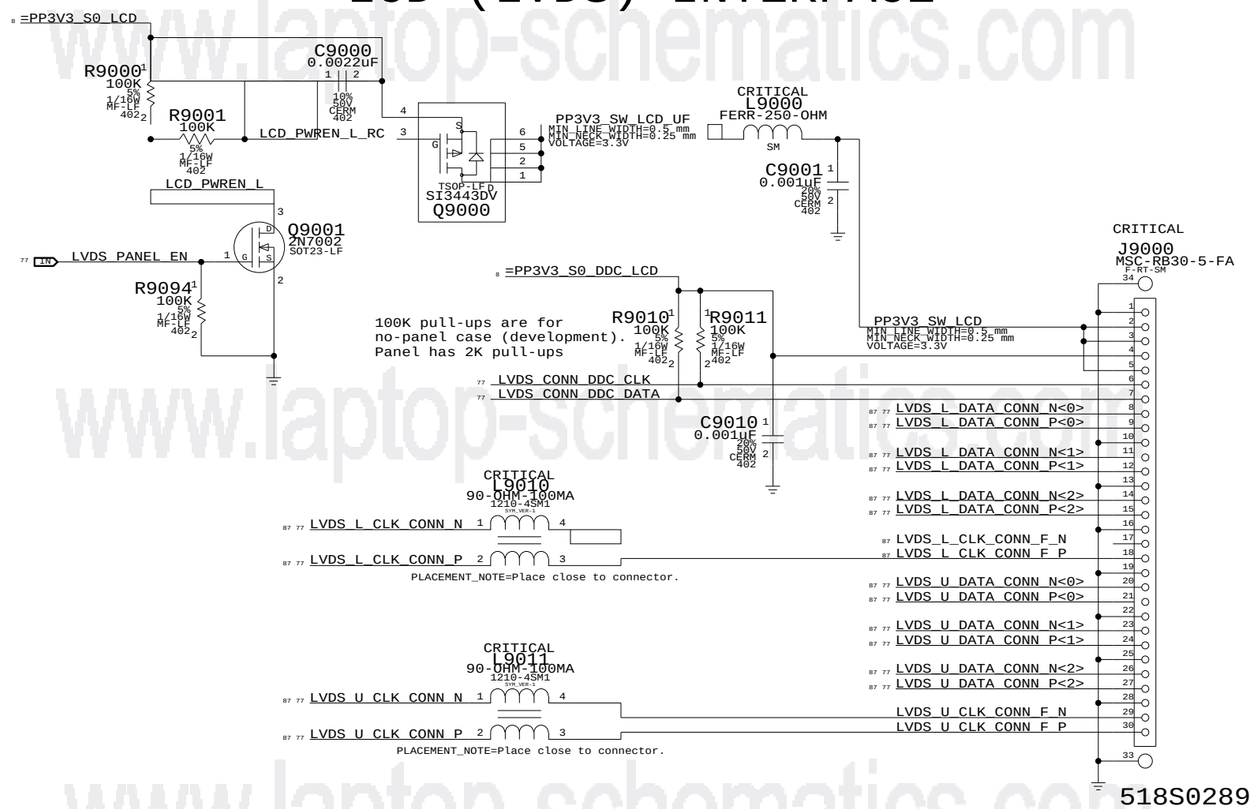
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE D | DRAWING NUMBER 051-7492 | REV. B

SCALE NONE | SHT 89 OF 109

LCD (LVDS) INTERFACE



LVDS Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7492	B
	SCALE: NONE	SHT 90 OF 109	

TMDS Filtering

(Place close to GPU) (Place close to connector)

TMDS_DATA_N<0> → TMDS_DATA_F_N<0>
TMDS_DATA_P<0> → TMDS_DATA_F_P<0>
TMDS_DATA_N<1> → TMDS_DATA_F_N<1>
TMDS_DATA_P<1> → TMDS_DATA_F_P<1>
TMDS_DATA_N<2> → TMDS_DATA_F_N<2>
TMDS_DATA_P<2> → TMDS_DATA_F_P<2>
TMDS_CLK_N → TMDS_CLK_F_N
TMDS_CLK_P → TMDS_CLK_F_P
TMDS_DATA_N<3> → TMDS_DATA_F_N<3>
TMDS_DATA_P<3> → TMDS_DATA_F_P<3>
TMDS_DATA_N<4> → TMDS_DATA_F_N<4>
TMDS_DATA_P<4> → TMDS_DATA_F_P<4>
TMDS_DATA_N<5> → TMDS_DATA_F_N<5>
TMDS_DATA_P<5> → TMDS_DATA_F_P<5>

=PP3V3_GPU_TMDSBIAS

NO STUFF C9462 0.01UF 10% 16V CERM 402
NO STUFF C9466 0.01UF 10% 16V CERM 402
NO STUFF C9470 0.01UF 10% 16V CERM 402
NO STUFF C9474 0.01UF 10% 16V CERM 402
NO STUFF C9478 0.01UF 10% 16V CERM 402
NO STUFF C9482 0.01UF 10% 16V CERM 402
NO STUFF C9486 0.01UF 10% 16V CERM 402

NO STUFF R9462 49.9 1% 1/16W MF-LF 402
NO STUFF R9463 49.9 1% 1/16W MF-LF 402
NO STUFF R9466 49.9 1% 1/16W MF-LF 402
NO STUFF R9467 49.9 1% 1/16W MF-LF 402
NO STUFF R9470 49.9 1% 1/16W MF-LF 402
NO STUFF R9471 49.9 1% 1/16W MF-LF 402
R9472 0 5% 1/16W MF-LF 402
NO STUFF R9474 49.9 1% 1/16W MF-LF 402
NO STUFF R9475 49.9 1% 1/16W MF-LF 402
R9473 0 5% 1/16W MF-LF 402
NO STUFF R9478 49.9 1% 1/16W MF-LF 402
NO STUFF R9479 49.9 1% 1/16W MF-LF 402
NO STUFF R9482 49.9 1% 1/16W MF-LF 402
NO STUFF R9483 49.9 1% 1/16W MF-LF 402
NO STUFF R9486 49.9 1% 1/16W MF-LF 402
NO STUFF R9487 49.9 1% 1/16W MF-LF 402

SIGNAL_MODEL=EMPTY TMDS_DATA_R0
SIGNAL_MODEL=EMPTY TMDS_DATA_R1
SIGNAL_MODEL=EMPTY TMDS_DATA_R2
SIGNAL_MODEL=EMPTY TMDS_DATA_R3
SIGNAL_MODEL=EMPTY TMDS_DATA_R4
SIGNAL_MODEL=EMPTY TMDS_DATA_R5
SIGNAL_MODEL=EMPTY TMDS_CLK_CMF

CRITICAL L9460 90-OHM-100MA 1210-4SM1 SYM_VER_1
CRITICAL L9464 90-OHM-100MA 1210-4SM1 SYM_VER_1
CRITICAL L9468 90-OHM-100MA 1210-4SM1 SYM_VER_1
CRITICAL L9472 370-OHM SM SYM_VER_1
CRITICAL L9476 90-OHM-100MA 1210-4SM1 SYM_VER_1
CRITICAL L9480 90-OHM-100MA 1210-4SM1 SYM_VER_1
CRITICAL L9484 90-OHM-100MA 1210-4SM1 SYM_VER_1

PLACEMENT_NOTE=Place close to connector.

VGA SYNC Buffers

=PP3V3_GPU_VGASYNC

GPU_VGA_VSYNC → U9450 MC74VHC1G08 SC70 → VGA_VSYNC_R → R9450 33 5% 1/16W MF-LF 402 → VGA_VSYNC

GPU_VGA_HSYNC → U9451 MC74VHC1G08 SC70 → VGA_HSYNC_R → R9451 33 5% 1/16W MF-LF 402 → VGA_HSYNC

C9450 0.1UF 10% 16V CERM 402
C9451 0.1UF 10% 16V CERM 402

PLACEMENT_NOTE=Place close to connector.

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

GPU_TV_COMP_VGA_B → VGA_TERM_FILTER R9440 150 1% 1/16W MF-LF 402 → VGA_B (DACB TV COMP)
GPU_TV_Y_VGA_G → VGA_TERM_FILTER R9441 150 1% 1/16W MF-LF 402 → VGA_G (DACB TV Y)
GPU_TV_C_VGA_R → VGA_TERM_FILTER R9442 150 1% 1/16W MF-LF 402 → VGA_R (DACB TV C)

CRITICAL FL9440 210MHZ MEA2010P-SM

C9440 3.3PF 0.25PF 50V CERM 402
C9441 3.3PF 0.25PF 50V CERM 402
C9442 3.3PF 0.25PF 50V CERM 402

DVI INTERFACE

DVI DDC Current Limit
(55mA requirement per DVI spec)

=PP5V_S0_DVI_DDC → CRITICAL F9410 0.5AMP-13.2V SM-LF → PP5V_S0_DDC_F (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V) → CRITICAL L9410 400-OHM-EMI SM-1 → PP5V_S0_DDC (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)

Isolation required for DVI->ADC Adapter

D9410 SOD-123 B0530WXF
PP5V_S0_DDC_PULLUPS (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)

=GND_CHASSIS_DVI_BOT → CRITICAL J9400 QH11121-RIG02-4F F-RT-TH-DVI

514-0278

TMDS_DATA_F_N<0> 17
TMDS_DATA_F_P<0> 18
TMDS_DATA_F_N<5> 20
TMDS_DATA_F_P<5> 21
TMDS_CLK_F_P 23
TMDS_CLK_F_N 24
VGA_B C3
VGA_HSYNC C4
C5B
C5A
C1 VGA_R
C2 VGA_G
34
32
1 TMDS_DATA_F_N<2>
9 TMDS_DATA_F_N<1>
2 TMDS_DATA_F_P<2>
10 TMDS_DATA_F_P<1>
19
11
4 TMDS_DATA_F_N<4>
12 TMDS_DATA_F_N<3>
5 TMDS_DATA_F_P<4>
13 TMDS_DATA_F_P<3>
6 DVI_DDC_CLK_R
14 (PP5V_S0_DDC)
7 DVI_DDC_DATA_R
15
8 VGA_VSYNC
16 DVI_HPD_R

VGA_TERM_CONN R9445 150 1% 1/16W MF-LF 402
VGA_TERM_CONN R9443 150 1% 1/16W MF-LF 402
VGA_TERM_CONN R9444 150 1% 1/16W MF-LF 402
C9410 0.01UF 10% 50V CERM 603

OMIT CX9490 SHORT NONE NONE 402
OMIT CX9491 SHORT NONE NONE 402
OMIT CX9492 SHORT NONE NONE 402
OMIT CX9493 SHORT NONE NONE 402
OMIT CX9400 SHORT NONE NONE 402
OMIT CX9401 SHORT NONE NONE 402
OMIT CX9402 SHORT NONE NONE 402
OMIT CX9403 SHORT NONE NONE 402

=GND_CHASSIS_DVI_TOP
=GND_CHASSIS_DVI_BOT

C9411 100PF 5% 50V CERM 402
C9413 100PF 5% 50V CERM 402
C9414 100PF 5% 50V CERM 402

R9410 4.7K 5% 1/16W MF-LF 402
R9412 4.7K 5% 1/16W MF-LF 402
R9411 100 5% 1/16W MF-LF 402
R9413 100 5% 1/16W MF-LF 402
R9414 100 5% 1/16W MF-LF 402

DVI_DDC_CLK
DVI_DDC_DATA
DVI_HPD

GPU Isolation / Level-Shift

=PP3V3_GPU_DVI

Q9411 2N7002DW-X-F SOT-363
Q9414 2N7002DW-X-F SOT-363
Q9415 2N7002DW-X-F SOT-363

R9420 10K 5% 1/16W MF-LF 402
R9421 10K 5% 1/16W MF-LF 402
R9422 270K 5% 1/16W MF-LF 402
R9423 270K 5% 1/16W MF-LF 402
R9415 20K 5% 1/16W MF-LF 402

GPU_DVI_DDC_CLK (OUT)
GPU_DVI_DDC_DATA (OUT)
GPU_HPD_BILAT
=GPU_HPD_ENABLE (IN)
GPU_HPD (OUT)
=PP5V_S0_SB_HPD
DVI_HOTPLUG_DET (OUT)

DVI Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7492	B
	SCALE: NONE	SHT 94 OF 109	

PGOOD Monitor for GPU Rails

LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit

Alias to 3.3V if not used->

PP3V3_GPU
=PP2V5_GPU_LTC2900
PP1V8_GPU
PP1V25_GPU

R9593 124K 1% 1/16W MF-LF 402
C9592 0.1UF 20% 10V CERM 402
C9591 0.1UF 20% 10V CERM 402
C9590 0.1UF 20% 10V CERM 402
R9595 1K 5% 1/16W MF-LF 402

U9590 CRITICAL
LTC2900 DFN
V1 V2 V3 V4 VREF VPG GND THRM_PAD
PBR* RST* CRT

GPU_PGOOD_P1V2_DIV
GPU_PGOOD_VREF
GPU_PGOOD_VPG
NC
PM_ALL_GPU_PGOOD
GPU_PGOOD_CRT

R9594 100K 1% 1/16W MF-LF 402
R9590 28K 1% 1/16W MF-LF 402
R9591 71.5K 1% 1/16W MF-LF 402
C9593 0.1UF 20% 10V CERM 402
C9595 330PF 10% 50V CERM 402
R9596 470K 5% 1/16W MF-LF 402

Trst = 4.6ms/nF
Trst = 1.5ms

LTC2900 typical threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

Fast wake condition is worst case. ICHx can create an S3 duration of 1 RTC clock (32 us). If mux select is on core well and AND-gate is implemented, glitch filter or <99ms PGOOD assertion time is required for PGOODs to be valid at end of 99 ms SMC timer. If mux select on resume well, then observed PGOOD will not change during S3 transitions and ICHx will honor whatever PGOOD delays are provided.

Mux Select Conditioning

=PP3V3_S0_LVDS_MUX
PP2V5_S0_LVDS_MUX

R9544 10K 5% 1/16W MF-LF 402
R9545 10K 5% 1/16W MF-LF 402

LVDS_SEL_RESUME
R9541 0 5% 1/16W MF-LF 402
LVDSDATAMUX_SEL_GPU_L

EXTGPU_LVDS_EN
RSVD_EXTGPU_LVDS_EN
LVDS_SEL_CORE
R9542 0 5% 1/16W MF-LF 402
Q9540 2N7002DW-X-F SOT-363
EXTGPU_LVDS_SEL

LVDS_SEL_RESUME
R9543 0 5% 1/16W MF-LF 402
EXTGPU_LVDS_EN33_L
LVDSCTRLMUX_SEL_GPU_L

Q9540 2N7002DW-X-F SOT-363
LVDS_SEL_CORE
R9563 0 5% 1/16W MF-LF 402

=PP3V3_S0_LVDS_MUX
LVDS_SEL_CORE
C9561 0.1UF 20% 10V CERM 402

LVDS_SEL_CORE
MC74VHC1G00 SC70-5
U9561
PLT_RST_L
EXTGPU_LVDS_EN_QUAL

NOTE: NAND-gate required if EXTGPU_LVDS_EN GPIO is on SB core well. Keeps PGOOD looking at non-GPU rails until GPIO switches back to default state and GPU power rails have come up and are valid (which should be before platform reset deasserts). Could be eliminated if GPIO moved to resume well.

LVDS I/F Mux

PP2V5_S0_LVDS_MUX
C9550 0.1UF 20% 10V CERM 402

U9550 CRITICAL
CBTV4020 BGA-LF
FB F3 E8 VDD

NB LVDS I/F

LVDS_B_DATA_N<2> LVDS_B_DATA_N<0> LVDS_B_DATA_P<0>
LVDS_A_CLK_P LVDS_A_CLK_N
LVDS_A_DATA_N<0> LVDS_A_DATA_P<0> LVDS_A_DATA_P<2> LVDS_A_DATA_N<2> LVDS_A_DATA_N<1> LVDS_A_DATA_P<1>
LVDS_B_DATA_P<1> LVDS_B_DATA_N<1>
LVDS_B_CLK_N LVDS_B_CLK_P
LVDS_B_DATA_P<2>

GPU LVDS I/F

LVDS_U_DATA_N<2> LVDS_U_DATA_N<0> LVDS_U_DATA_P<0>
LVDS_L_CLK_P LVDS_L_CLK_N
LVDS_L_DATA_N<0> LVDS_L_DATA_P<0> LVDS_L_DATA_P<2> LVDS_L_DATA_N<2> LVDS_L_DATA_N<1> LVDS_L_DATA_P<1>
LVDS_U_DATA_P<1> LVDS_U_DATA_N<1>
LVDS_U_CLK_N LVDS_U_CLK_P
LVDS_U_DATA_P<2>

GND

LVDS_U_DATA_CONN_N<2> LVDS_U_DATA_CONN_N<0> LVDS_U_DATA_CONN_P<0>
NC
LVDS_L_CLK_CONN_P LVDS_L_CLK_CONN_N
NC
LVDS_L_DATA_CONN_N<0> LVDS_L_DATA_CONN_P<0> LVDS_L_DATA_CONN_P<2> LVDS_L_DATA_CONN_N<2> LVDS_L_DATA_CONN_N<1> LVDS_L_DATA_CONN_P<1>
NC
LVDS_L_DATA_CONN_P<1> LVDS_L_DATA_CONN_N<1>
NC
LVDS_U_CLK_CONN_N LVDS_U_CLK_CONN_P LVDS_U_DATA_CONN_P<2>

SEL LVDSDATAMUX_SEL_GPU_L
NOTE: SEL = LOW selects port B

LVDS Data Mux Power Supply

=PP3V3_S0_LVDS_MUX
R9555 10K 1% 1/16W MF-LF 402
R9556 31.6K 1% 1/16W MF-LF 402
P2V5_S0_VREF
C9556 0.1UF 20% 10V CERM 402
U9555 CRITICAL MAX4236EUTT SOT23-6-LF
C9555 0.1UF 20% 10V CERM 402
PP2V5_S0_LVDS_MUX
MIN_LINE_WIDTH=0.26 mm
MIN_NECK_WIDTH=0.10 mm
VOLTAGE=2.5V

GPU DDC Pass FETs

=GPU_DDC_ENABLE
=PP3V3_GPU_LVDS_DDC

R9570 15.8K 1% 1/16W MF-LF 402
(Ext. GFX) GPU_PANEL_DDC_CLK
Q9570 2N7002DW-X-F SOT-363
LVDS_CONN_DDC_CLK
MAKE_BASE=TRUE
LVDS_DDC_CLK (Int. GFX)

R9571 15.8K 1% 1/16W MF-LF 402
(Ext. GFX) GPU_PANEL_DDC_DATA
Q9570 2N7002DW-X-F SOT-363
LVDS_CONN_DDC_DATA
MAKE_BASE=TRUE
LVDS_DDC_DATA (Int. GFX)

Panel/Backlight Control Mux

=PP3V3_S0_LVDS_MUX

R9562 10K 5% 1/16W MF-LF 402
C9560 0.1UF 20% 10V CERM 402
CRITICAL
U9560 74CBTLV3257 QFN
VCC GND THRML PAD
HI=xB2 LO=xB1 OE*

GPU_PANEL_EN
LVDS_VDD_EN
GPU_BKLT_EN
LVDS_BKLT_EN
GPU_BL_PWM
LVDS_BKLT_CTL
PM_ALL_GPU_PGOOD
PM_ALL_NBGFX_PGOOD
LVDSCTRLMUX_SEL_GPU_L

R9561 100K 5% 1/16W MF-LF 402
R9560 10K 5% 1/16W MF-LF 402

LVDS_PANEL_EN
LCDBKLT_PWREN
LCDBKLT_PWM_UNBUF
TP_PM_ALL_GFX_PGOOD

NOTE: New H/W and S/W challenge since NB gfx might be powered off if using external GPU. S/W will have to guarantee that the "other" device is ready before a switch can occur. If mux select GPIO is still on a core well, this could mean powering up IG supply will be necessary before going to sleep to keep PGOODs valid.

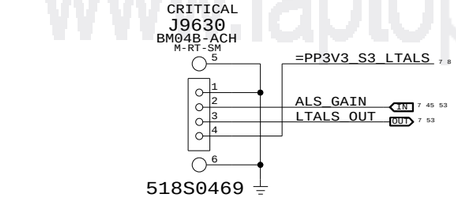
LVDS Interface Mux

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

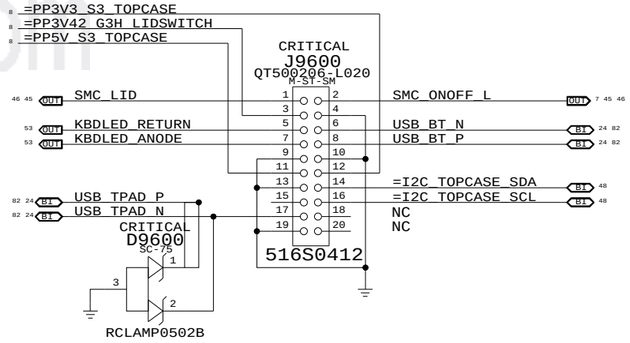
SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 95 OF 109	

Left ALS Connector

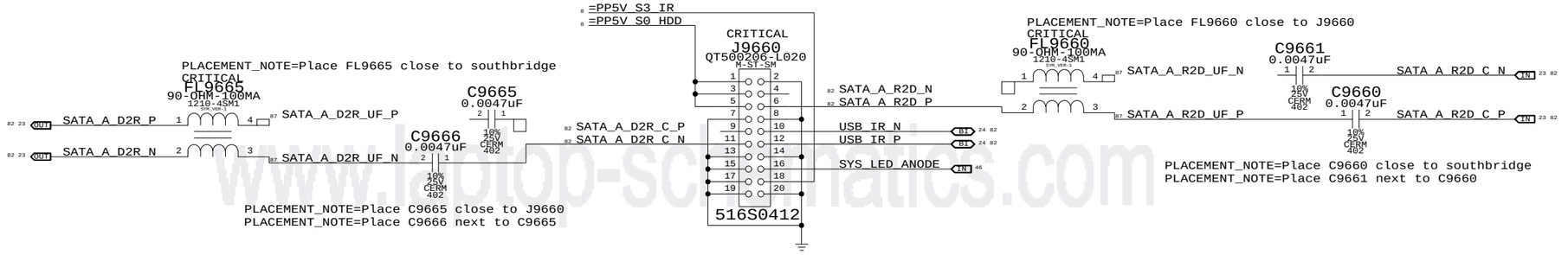


White colored version of 518S0369

Top-Case Connector



SATA HDD & IR & SIL Flex Connector



NOTE: SATA _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

Project Specific Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 96 OF 109	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	10
CPU_FERR_L	CPU_55S		CPU_FERR_L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	10 46 58
CPU_PWRGD	CPU_55S		CPU_PWRGD	7 10 13 23
CPU_FROM_SB	CPU_55S		CPU_INTR	10 23
CPU_FROM_SB	CPU_55S		CPU_NMI	10 23
CPU_FROM_SB	CPU_55S		CPU_A20M_L	10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	7 10 23
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	10 23 47
CPU_FROM_SB	CPU_55S		CPU_SMI_L	10 23
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	7 10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	7 16 25 58
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	7 58
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	7 10 16 23 58
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 84
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 84
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	13
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	7 12 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 58
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	58
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	58

CPU/FSB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE NONE SHT 100 OF 109

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
LVDS	*	20 MIL	?	
CRT	*	25 MIL	?	DG Says 40 mil spacing minimum
CRT_2CRT	*	20 MIL	?	
CRT_SYNC	*	25 MIL	?	DG Says 30 mil spacing minimum
CRT_SYNC2SYNC	*	20 MIL	?	
TVDAC	*	25 MIL	?	DG Says 40 mil spacing minimum
TVDAC_2TVDAC	*	20 MIL	?	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.

CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG_R2D_P<15..0>	66
	PCIE_100D	PCIE	PEG_R2D_N<15..0>	66
	PCIE_100D	PCIE	PEG_R2D_C_P<15..0>	15 66
	PCIE_100D	PCIE	PEG_R2D_C_N<15..0>	15 66
PEG_D2R	PCIE_100D	PCIE	PEG_D2R_P<15..0>	15 66
	PCIE_100D	PCIE	PEG_D2R_N<15..0>	15 66
	PCIE_100D	PCIE	PEG_D2R_C_P<15..0>	66
	PCIE_100D	PCIE	PEG_D2R_C_N<15..0>	66
DMI_N2S	DMI_100D	DMI	DMI_N2S_P<3..0>	16 24
	DMI_100D	DMI	DMI_N2S_N<3..0>	16 24
DMI_S2N	DMI_100D	DMI	DMI_S2N_P<3..0>	16 24
	DMI_100D	DMI	DMI_S2N_N<3..0>	16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	15 77
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	15 77
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_N<3>	
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	15 77
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	15 77
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_P<3>	
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_N<3>	
LVDS_IBG		LVDS	LVDS_IBG	15 22
CRT_TVO_IREF		CRT	CRT_TVO_IREF	
CRT_RED	CRT_50S	CRT	CRT_RED	
CRT_GREEN	CRT_50S	CRT	CRT_GREEN	
CRT_BLUE	CRT_50S	CRT	CRT_BLUE	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R	
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC	
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC	
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC	

NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	101	109

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK_N<2..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK_N<5..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	17 32

Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 102 OF 109	

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L	23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ	23 42
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L	24 42
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	23 78
	SATA_100D	SATA	SATA_A_R2D_C_N	23 78
	SATA_100D	SATA	SATA_A_R2D_P	78
	SATA_100D	SATA	SATA_A_R2D_N	78
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P	23 78
	SATA_100D	SATA	SATA_A_D2R_N	23 78
	SATA_100D	SATA	SATA_A_D2R_C_P	78
	SATA_100D	SATA	SATA_A_D2R_C_N	78
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D_C_P	23 42
	SATA_100D	SATA	SATA_B_R2D_C_N	23 42
	SATA_100D	SATA	SATA_B_R2D_P	
	SATA_100D	SATA	SATA_B_R2D_N	
SATA_B_D2R	SATA_100D	SATA	SATA_B_D2R_P	23 42
	SATA_100D	SATA	SATA_B_D2R_N	23 42
	SATA_100D	SATA	SATA_B_D2R_C_P	
	SATA_100D	SATA	SATA_B_D2R_C_N	
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D_C_P	23 42
	SATA_100D	SATA	SATA_C_R2D_C_N	23 42
	SATA_100D	SATA	SATA_C_R2D_P	
	SATA_100D	SATA	SATA_C_R2D_N	
SATA_C_D2R	SATA_100D	SATA	SATA_C_D2R_P	23 42
	SATA_100D	SATA	SATA_C_D2R_N	23 42
	SATA_100D	SATA	SATA_C_D2R_C_P	
	SATA_100D	SATA	SATA_C_D2R_C_N	
SATA_RBIAS	SATA_55S		SATA_RBIAS	42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	23 34
	HDA_55S	HDA	HDA_BIT_CLK_R	23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	23 34
	HDA_55S	HDA	HDA_SYNC_R	23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	23 34
	HDA_55S	HDA	HDA_RST_L_R	23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	23 34
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	23 34
	HDA_55S	HDA	HDA_SDOUT_R	23
USB_EXTA	USB_90D	USB	USB_EXTA_P	24 43
	USB_90D	USB	USB_EXTA_N	24 43
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	24 34
	USB_90D	USB	USB_MINI_N	24 34
USB_EXTD	USB_90D	USB	USB_EXTD_P	24 44
	USB_90D	USB	USB_EXTD_N	24 44
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7 24 44
	USB_90D	USB	USB_CAMERA_N	7 24 44
USB_BT	USB_90D	USB	USB_BT_P	24 78
	USB_90D	USB	USB_BT_N	24 78
USB_TPAD	USB_90D	USB	USB_TPAD_P	24 78
	USB_90D	USB	USB_TPAD_N	24 78
USB_IR	USB_90D	USB	USB_IR_P	24 78
	USB_90D	USB	USB_IR_N	24 78
USB_EXTB	USB_90D	USB	USB_EXTB_P	24 34
	USB_90D	USB	USB_EXTB_N	24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	24 34
	USB_90D	USB	USB_EXCARD_N	24 34
USB_EXTC	USB_90D	USB	USB_EXTC_P	9 24
	USB_90D	USB	USB_EXTC_N	9 24
USB_RBIAS	USB_60S		USB_RBIAS	24
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK	25 48
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA	25 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK	25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA	25 48
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	24 55
	SPI_55S	SPI	SPI_SCLK	55
	SPI_55S	SPI	SPI_A_SCLK_R	
	SPI_55S	SPI	SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	24 55
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	55
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	24 55
	SPI_55S	SPI	SPI_A_SO_R	55
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_I0	SPI_55S	SPI	SPI_CE_R_L<0>	24 55
	SPI_55S	SPI	SPI_CE_L<0>	55
SPI_CE_I1	SPI_55S	SPI	SPI_CE_R_L<1>	
	SPI_55S	SPI	SPI_CE_L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE NONE SHT 103 OF 109

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCI_AD	PCI_55S	PCI	PCI_AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI_AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI_AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI_AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI_PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	24 38
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI_LOCK_L	24
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI_FW_REQ_L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI_FW_GNT_L	24 38
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	24
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_REQ2_L	PCI_55S	PCI	PCI_REQ2_L	24
PCI_GNT2_L	PCI_55S	PCI	PCI_GNT2_L	
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	24 38
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L	24
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE_A_R2D_C_P	
	PCIE_100D	PCIE	PCIE_A_R2D_C_N	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE_A_D2R_P	
	PCIE_100D	PCIE	PCIE_A_D2R_N	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_B_R2D_C_P	
	PCIE_100D	PCIE	PCIE_B_R2D_C_N	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_B_D2R_P	
	PCIE_100D	PCIE	PCIE_B_D2R_N	
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_P	34
	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_N	34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE_EXCARD_D2R_P	34
	PCIE_100D	PCIE	PCIE_EXCARD_D2R_N	34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_100D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE_FW_D2R_P	
	PCIE_100D	PCIE	PCIE_FW_D2R_N	
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE_MINI_R2D_C_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_R2D_C_N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE_MINI_D2R_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_D2R_N	24 34
GLAN_COMP			GLAN_COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE_ENET_R2D_C_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_C_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_P	35
	PCIE_100D	PCIE	PCIE_ENET_R2D_N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE_ENET_D2R_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_P	35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<0>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<1>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<2>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3>	35 37

SB Constraints (2 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	104	109

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	29 30
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	29 30
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	29 30
CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	29 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 79
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 79
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 47
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	30 38
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	30 45
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	7
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	7
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	7 22 30
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	7 22 30
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	9
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	9
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	30 34
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	30 34
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 30
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	30 34
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	30 34
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	30 35
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	30 35

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	48
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	48
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	48
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	48
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	48
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	48
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	48
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	48
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48

Clock & SMC Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE: NONE	SHT 105 OF 109	

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_D_CTL	FW_55S	FW	FW_LINK<7..0>	
FW_D_CTL	FW_55S	FW	FW_CTL<1..0>	
FW_LCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_LCLK	
	CLK_MED_55S	CLK_MED	CLKFW_PHY_LCLK	38 39
FW_PCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_PCLK	38 39
	CLK_MED_55S	CLK_MED	CLKFW_PHY_PCLK	
FW_LKON	FW_55S	FW	FW_LKON	
	FW_55S	FW	FW_LKON_R	
FW_LPS	FW_55S	FW	FW_LPS	38 39
FW_LREQ	FW_55S	FW	FW_LREQ	38 39
FW_PINT	FW_55S	FW	FW_PINT	38 39
FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R	
	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI	
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_P	39 41
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_N	39 41
FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_P	39 41
FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_N	39 41
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_P	39 41
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_N	39 41
FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_P	39 41
FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_N	39 41

Port 2 Not Used

FireWire Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	106	109

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R50SE	*	=50_OHM_SE	=40_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_MA<1..0>
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_MA<11..6>
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_BA<2..0>
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_RAS_L
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_CAS_L
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_WE_L
FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_A_CKE
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_CS0_L
FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_A_DRAM_RST
FB_A_CMD	GDDR3_50SE	GDDR3_CMD	FB_A_LMA<5..2>
FB_B_CMD	GDDR3_50SE	GDDR3_CMD	FB_A_UMA<5..2>
FB_A_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<0>
FB_A_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<1>
FB_A_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<2>
FB_A_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<3>
FB_A_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<0>
FB_A_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<1>
FB_A_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<2>
FB_A_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<3>
FB_A_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<7..0>
FB_A_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<15..8>
FB_A_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<23..16>
FB_A_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<31..24>
FB_A_DQM0	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<0>
FB_A_DQM1	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<1>
FB_A_DQM2	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<2>
FB_A_DQM3	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<3>
FB_B_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<4>
FB_B_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<5>
FB_B_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<6>
FB_B_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<7>
FB_B_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<4>
FB_B_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<5>
FB_B_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<6>
FB_B_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<7>
FB_B_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<39..32>
FB_B_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<47..40>
FB_B_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<55..48>
FB_B_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<63..56>
FB_B_DQM0	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<4>
FB_B_DQM1	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<5>
FB_B_DQM2	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<6>
FB_B_DQM3	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<7>

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_MA<1..0>
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_MA<11..6>
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_BA<2..0>
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_RAS_L
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_CAS_L
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_WE_L
FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_B_CKE
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_CS0_L
FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_B_DRAM_RST
FB_C_CMD	GDDR3_50SE	GDDR3_CMD	FB_B_LMA<5..2>
FB_D_CMD	GDDR3_50SE	GDDR3_CMD	FB_B_UMA<5..2>
FB_C_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<0>
FB_C_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<1>
FB_C_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<2>
FB_C_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<3>
FB_C_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<0>
FB_C_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<1>
FB_C_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<2>
FB_C_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<3>
FB_C_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<7..0>
FB_C_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<15..8>
FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<23..16>
FB_C_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<31..24>
FB_C_DQM0	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<0>
FB_C_DQM1	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<1>
FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<2>
FB_C_DQM3	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<3>
FB_D_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<4>
FB_D_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<5>
FB_D_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<6>
FB_D_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<7>
FB_D_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<4>
FB_D_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<5>
FB_D_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<6>
FB_D_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<7>
FB_D_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<39..32>
FB_D_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<47..40>
FB_D_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<55..48>
FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<63..56>
FB_D_DQM0	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<4>
FB_D_DQM1	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<5>
FB_D_DQM2	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<6>
FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<7>

G84M Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_GATED
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS_GATED
	LVDS_100D	LVDS	LVDS_L_CLK_P
	LVDS_100D	LVDS	LVDS_L_CLK_N
	LVDS_100D	LVDS	LVDS_L_DATA_P<3..0>
	LVDS_100D	LVDS	LVDS_L_DATA_N<3..0>
	LVDS_100D	LVDS	LVDS_U_CLK_P
	LVDS_100D	LVDS	LVDS_U_CLK_N
	LVDS_100D	LVDS	LVDS_U_DATA_P<3..0>
	LVDS_100D	LVDS	LVDS_U_DATA_N<3..0>
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_N
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<5..0>
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_N<5..0>
VGA_R_TV_C	VGA_50S	VGA	GPU_TV_C_VGA_R
VGA_G_TV_Y	VGA_50S	VGA	GPU_TV_Y_VGA_G
VGA_B_TV_COMP	VGA_50S	VGA	GPU_TV_COMP_VGA_B
	VGA_50S	VGA	GPU_VGA_R
	VGA_50S	VGA	GPU_VGA_G
	VGA_50S	VGA	GPU_VGA_B
	VGA_50S	VGA	GPU_TV_C
	VGA_50S	VGA	GPU_TV_Y
	VGA_50S	VGA	GPU_TV_COMP
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_HSYNC
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_VSYNC

GPU (G84M) Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	107	109

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
DMI	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	ENET_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	FW_POWER	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*			0.100 MM	2.54 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	ISL10			0.100 MM	2.54 MM		
MEM_85D	ISL4,ISL10			0.100 MM	2.54 MM		

Graphics Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
TMDS_100D	BGA	100_DIFF_BGA

SIM Card Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
WWAN_SIM	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
WWAN_SIM	*	=2:1_SPACING	?

M75 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_P	34
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_N	34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_P	34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_N	34
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3..0>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3..0>	
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
	FW_110D	FW_TP	FW_PORT0_TPA_FL_P	41
	FW_110D	FW_TP	FW_PORT0_TPA_FL_N	41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_P	41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_N	41
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_P	78
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_N	78
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_P	78
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_N	78
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	43
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	43
(USB_EXTA)	USB_90D	USB	USB2_RT_P	43
(USB_EXTA)	USB_90D	USB	USB2_RT_N	43
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_P	44
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_N	44
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_P	44
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_P	59
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	NBCOREISNS_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8ISNS_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V25ISNS_P	50
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 72
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	HSTHMSNS_D_P	7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	REMTHMSNS_DX_P	
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	RSFSTHMSNS_D_P	7 51
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_P	75
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_N	75
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_P	75 77
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_N	75 77
	LVDS_100D	LVDS	LVDS_L_DATA_CONN_P<3..0>	75 77
	LVDS_100D	LVDS	LVDS_L_DATA_CONN_N<3..0>	75 77
	LVDS_100D	LVDS	LVDS_U_CLK_CONN_P	75 77
	LVDS_100D	LVDS	LVDS_U_CLK_CONN_N	75 77
	LVDS_100D	LVDS	LVDS_U_DATA_CONN_P<3..0>	75 77
	LVDS_100D	LVDS	LVDS_U_DATA_CONN_N<3..0>	75 77
	TMDS_100D	TMDS	TMDS_CLK_R_P	76
	TMDS_100D	TMDS	TMDS_CLK_R_N	76
	TMDS_100D	TMDS	TMDS_CLK_F_P	76
	TMDS_100D	TMDS	TMDS_CLK_F_N	76
	TMDS_100D	TMDS	TMDS_DATA_F_P<5..0>	76
	TMDS_100D	TMDS	TMDS_DATA_F_N<5..0>	76
(VGA_R_TV_Y)	VGA_50S	VGA	VGA_R	76
(VGA_G_TV_C)	VGA_50S	VGA	VGA_G	76
(VGA_B_TV_COMP)	VGA_50S	VGA	VGA_B	76
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC_R	76
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC_R	76
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC	76
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC	76
		PP1V8_MEM	=PP1V8_S3M_MEM_A	8 31
		PP1V8_MEM	=PP1V8_S3M_MEM_B	8 32
		GND	GND	
		SB_POWER	PP3V3_S5	8
		SB_POWER	PP3V3_S0	8 65
		SB_POWER	PP1V5_S0	8
	WWAN_SIM	WWAN_SIM	WWAN_SIM_CLOCK	44
	WWAN_SIM	WWAN_SIM	WWAN_SIM_DATA	44

Project Specific Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B
SCALE	SHT	OF
NONE	108	109

M75 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	ISL2,ISL11	Y	0.250 MM	0.076 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.125 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7492	B

SCALE	SHT	OF
NONE	109	109