1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MBP 15" MLB

12/07/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7413	1	SCHEM,TAUPO,M87	SCH	CRITICAL	
820-2249	1	PCBF,TAUPO,M87	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Wed Dec 12 10:44:22 2007

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

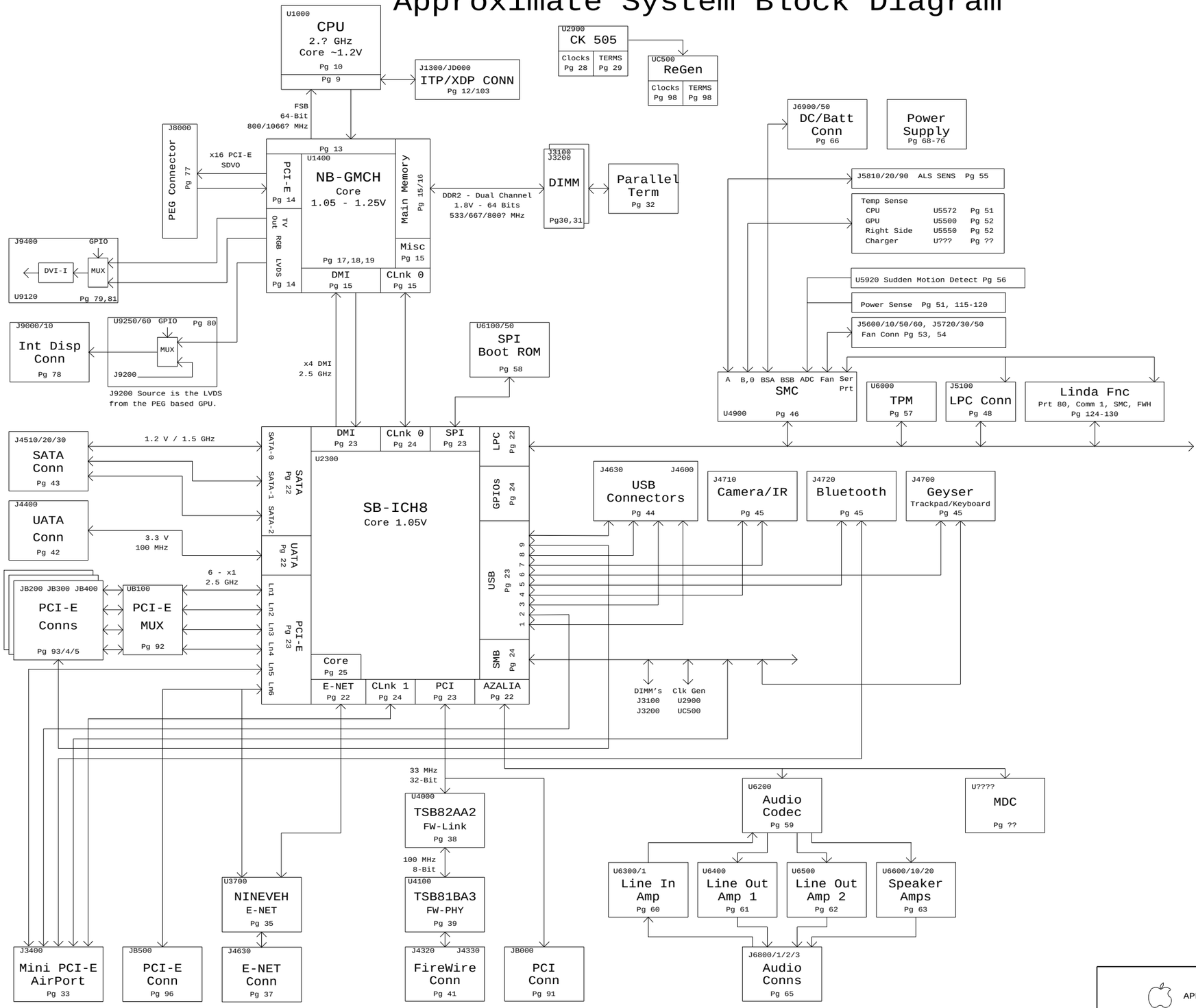
SIZE D

APPLE INC.

TITLE
SCHEM,TAUPO,M87

DRAWING NUMBER 051-7413
REV 16.0.0
SHT 1 OF 89

Approximate System Block Diagram



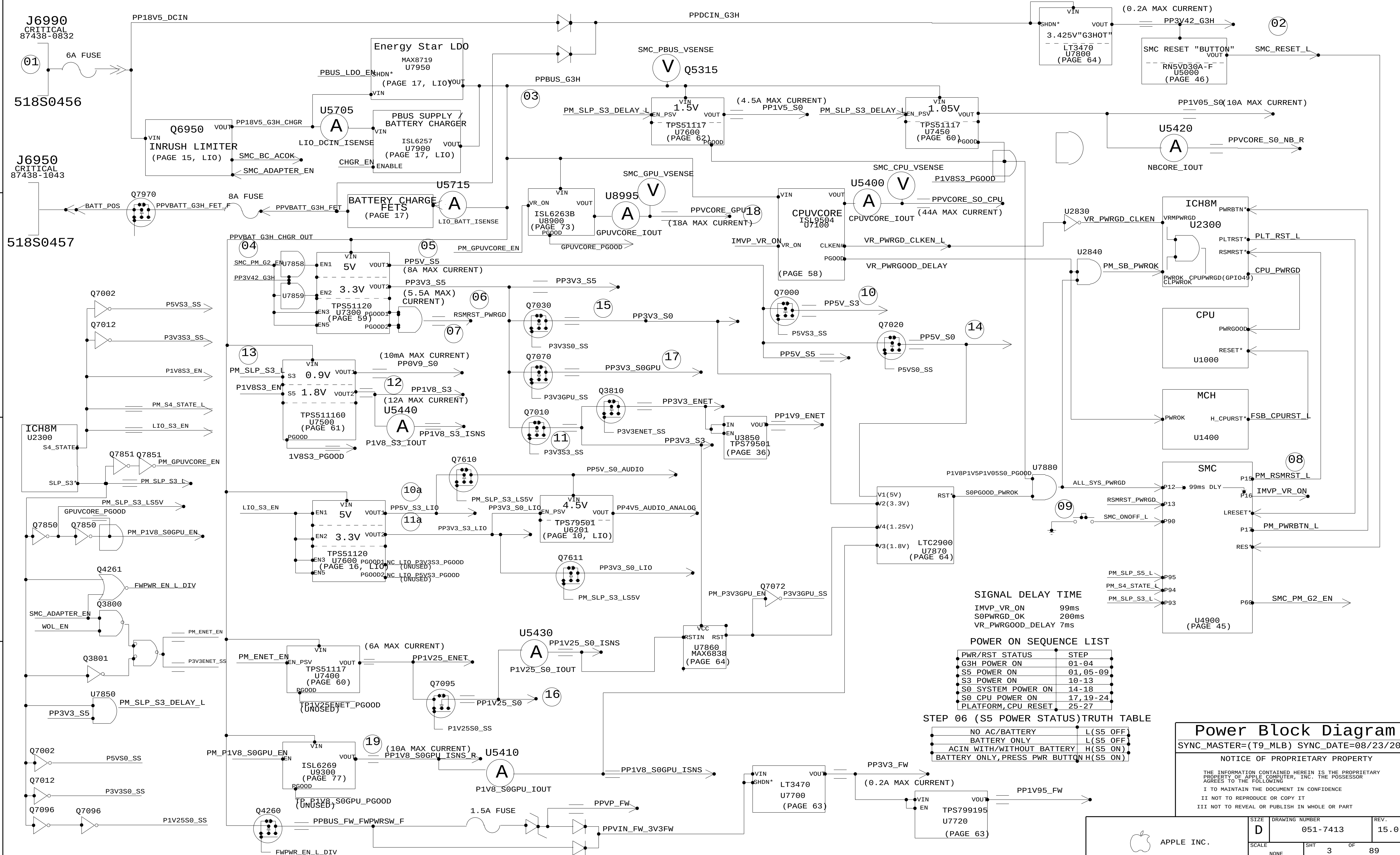
System Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 2 OF 89	

M87 POWER SYSTEM ARCHITECTURE



SIGNAL DELAY TIME

IMVP_VR_ON	99ms
S0PWRGD_OK	200ms
VR_PWRGOOD_DELAY	7ms

POWER ON SEQUENCE LIST

PWR/RST STATUS	STEP
G3H POWER ON	01-04
S5 POWER ON	01,05-09
S3 POWER ON	10-13
S0 SYSTEM POWER ON	14-18
S0 CPU POWER ON	17,19-24
PLATFORM,CPU RESET	25-27

STEP 06 (S5 POWER STATUS)TRUTH TABLE

NO AC/BATTERY	L(S5 OFF)
BATTERY ONLY	L(S5 OFF)
ACIN WITH/WITHOUT BATTERY	H(S5 ON)
BATTERY ONLY,PRESS PWR BUTTON	H(S5 ON)

Power Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

APPLE INC.

SIZE D | DRAWING NUMBER 051-7413 | REV. 15.0.0

SCALE NONE

Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 4 OF 89	

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9089	PCBA,2.5GHZ,512SAM_VRAM,M87	M87_COMMON,EEE_Z3G,CPU_2_5GHZ,FB_512_SAMSUNG
630-9091	PCBA,2.6GHZ,512SAM_VRAM,M87	M87_COMMON,EEE_Z3J,CPU_2_6GHZ,FB_512_SAMSUNG
630-9088	PCBA,2.5GHZ,512HY_VRAM,M87	M87_COMMON,EEE_Z3F,CPU_2_5GHZ,FB_512_HYNIX
630-9090	PCBA,2.6GHZ,512HY_VRAM,M87	M87_COMMON,EEE_Z3H,CPU_2_6GHZ,FB_512_HYNIX
630-9213	PCBA,2.4GHZ,256SAM_VRAM,M87	M87_COMMON,EEE_ZUP,CPU_2_4GHZ,FB_256_SAMSUNG
630-9238	PCBA,2.4GHZ,256HY_VRAM,M87	M87_COMMON,EEE_043,CPU_2_4GHZ,FB_256_HYNIX
630-9286	PCBA,2.4GHZFUSED,256SAM_VRAM,M87	M87_COMMON,EEE_0U2,CPU_2_4GHZFUSED,FB_256_SAMSUNG
630-9287	PCBA,2.4GHZFUSED,256HY_VRAM,M87	M87_COMMON,EEE_0U3,CPU_2_4GHZFUSED,FB_256_HYNIX

M87 BOM Groups

BOM GROUP	BOM OPTIONS
M87_COMMON	ALTERNATE,COMMON,M87_COMMON1,M87_COMMON2,M87_PROGPARTS
M87_COMMON1	ISL9504B,ONEWIRE_PU,LPCPLUS,SMC_DEBUG_NO
M87_COMMON2	GPUVID_1P13V,P1V8S3_1V8,SMS_MOT_DIS,YUKON_ULTRA,VGA_TERM_CONN
M87_DEBUG	SMC_DEBUG_YES,XDP,XDP_CONN
M87_PROGPARTS	BOOTROM_PROG,SMC_PROG

BOM GROUP	BOM OPTIONS
FB_512_SAMSUNG	VRAM8,VRAM_16M,VRAM_SAMSUNG,VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM8,VRAM_16M,VRAM_HYNIX,VRAM_512_HYNIX
FB_256_SAMSUNG	VRAM4,VRAM_16M,VRAM_SAMSUNG,VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4,VRAM_16M,VRAM_HYNIX,VRAM_256_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z3F]	CRITICAL	EEE_Z3F
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z3G]	CRITICAL	EEE_Z3G
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z3H]	CRITICAL	EEE_Z3H
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z3J]	CRITICAL	EEE_Z3J
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUP]	CRITICAL	EEE_ZUP
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:043]	CRITICAL	EEE_043
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUP]	CRITICAL	EEE_0U2
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:043]	CRITICAL	EEE_0U3

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3560	1	IC,PDC,SR,QS,C0,2.5G,35W,800FSB,6M,BGA	U1000	CRITICAL	CPU_2_5GHZ
337S3559	1	IC,PDC,SR,QS,C0,2.6G,35W,800FSB,6M,BGA	U1000	CRITICAL	CPU_2_6GHZ
338S0509	1	IC,GPU,NV G84M,BGA,LOW LEAK	U8000	CRITICAL	
338S0432	1	IC,NB,CRESTLINE,GM,C0,PRQ,965PM	U1400	CRITICAL	
338S0434	1	IC,SB,ICH8M,B1,PRQ,BGA	U2300	CRITICAL	
353S1651	1	IC,ISL9504B,2PH IMVP6 REG,PMON,QFN48	U7100	CRITICAL	ISL9504B
359S0130	1	IC,SLG2AP101,LW PWR CLCK GEN,CK505,QFN68	U2900	CRITICAL	
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2193	1	IC,SMC,DEVELOPMENT,M75	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2192	1	IC,EFI ROM,DEVELOPMENT,M75	U6100	CRITICAL	BOOTROM_PROG
337S3561	1	IC,PDC,SR,ES2,L0,2.4G,35W,800FSB,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3576	1	IC,PDC,SR,QS,C0,2.4G,35W,800FSB,3M,BGA	U1000	CRITICAL	CPU_2_4GHZFUSED

333S0423	8	IC,SGRAM,GDDR3,16Mx32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550,U9100,U9150,U9200,U9250	CRITICAL	VRAM_512_SAMSUNG
333S0424	8	IC,SGRAM,GDDR3,16Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550,U9100,U9150,U9200,U9250	CRITICAL	VRAM_512_HYNIX
333S0423	4	IC,SGRAM,GDDR3,16Mx32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0424	4	IC,SGRAM,GDDR3,16Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	E&E alt to TDK/BI-Tech magnetics
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung
353S1681	353S1294		ALL	LMV2011,OPAMP. GBW
152S0684	152S0368		ALL	Maglayers alt to Dale/Vishay
152S0683	152S0276		ALL	Maglayers alt to Dale/Vishay
104S0023	104S0018		ALL	Cyntec alt to sense resistor
104S0024	104S0017		ALL	Panasonic alt to FW resistor

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	5	89

PROTO

```
0.1.0:
04/26/07 -- Design branched from 051-7225-A
04/26/07 -- Clock Termination: Removed support for SLG8LP537 device (GPU_CLK_27M/27MSS muxes, etc)
04/26/07 -- Clock Termination: Added S0-powered AND gate between GPU_PGOOD and SLG2AP101 enable pin to eliminate leakage path (rdar://5086613)
04/26/07 -- SB Misc: Removed EXTGPU_RST_L support for reseting the GPU (hardware control only)
04/26/07 -- Power Control: Removed U7858 and R7860. Tied SMC_PM_G2_EN/PM_G2_EN directly to S5 regulators
04/26/07 -- SB Decoupling: Replaced L2700 with 155S0333 for AVL updates
04/26/07 -- FW Port Power: Replaced D4260 with proper symbol (instead of table)
04/30/07 -- FW Port Power: Updated U4210 to 353S1744 for AVL updates
05/01/07 -- Current Sensors: Changed R5425/35/45 to RES_SENSE symbol which implements kelvin sensing without the need for XW shorts
0.1.2:
05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)
05/08/07 -- GPU Straps: Stuffed R8728 to put GPU PEG I/F into mobile mode (rdar://5188253)
0.2.0:
05/10/07 -- Thermal Sensors: Added SIGNAL_MODEL=EMPTY properties to thermal sense diff pairs (rdar://5192397)
05/10/07 -- Current Sensors: Added SIGNAL_MODEL=EMPTY properties to current sense diff pairs (rdar://5192397)
0.3.0:
05/14/07 -- Power Control: Added U7858,U7859 to properly enable/disable S5 regulators (rdar://TBD)
05/14/07 -- 5V/3.3V Regulators: Added C7307,C7308 to allow soft-start control of S5 regulators (rdar://TBD)
0.4.0:
05/22/07 -- Power Control: Added C7858 to decouple U7858/59
05/22/07 -- GPU Vcore: Removed Power Control circuitry
05/22/07 -- GPU Straps: Added R8734 to get PCIDEVID3 pullup
0.5.0:
06/06/07 -- GPU FB: Reassigned CS1/BA2 for future memory expansion
06/06/07 -- GPU FB: Changed 22uF, 0805 caps to 10uF, 0603 for future memory expansion
06/06/07 -- GPU FB: Reworked/added FB device Vrefs (with smaller FETs) for future memory expansion
06/06/07 -- Left Clutch I/C: Removed SIM I/F connector
0.6.0:
06/07/07 -- GPU Straps: U8700 changed to TS3V340 only
06/18/07 -- GPU FB: Added support for 1Gb density ICs (added MA<12> and CS1)
06/18/07 -- Left Clutch I/C: Added alternate camera connections (CCP2 I/F)
06/18/07 -- DFM: Added NC nets to allow copper on BGA corner balls (CPU and GPU)
06/19/07 -- GPU FB: Added 4 more 16Mx32 VRAM devices
06/20/07 -- Muxed Gfx: Began removing support for this feature
0.7.0:
06/25/07 -- GPU VCORE: U8900 Changed to IMVP6
06/25/07 -- FB REGULATOR: Added U9300
06/25/07 -- Muxed Gfx: Removed LVDS/BKLT muxes and support
06/25/07 -- Power Fet: Removed 1V8 and 1V25 Fets
06/25/07 -- Current Sense: Removed U5410 NBGfx Sense
06/25/07 -- Regulators: Changed Q7320,Q7360,Q7410,Q7460,Q7620 to SI7110N
0.8.0:
06/27/07 -- Power Fet: Removed 1v8 S0 Fet, cleaned up aliasing
0.9.0:
06/27/07 -- Current Sense: Added 1v8 FB current sense
06/27/07 -- GPU VCORE: Added additional High side Input Cap
0.10.0:
06/27/07 -- MUX Gfx: Delete GPU PGOOD Monitor
0.11.0:
06/27/07 -- Aliasing:Cleanup
06/27/07 -- BOM: Changed BOM option table for M87
0.12.0:
07/02/07 -- Power CTL:Added 1.25 PGOOD/3V3 GPU EN,Moved 1V8_S3 to pgood chain
07/02/07 -- LCC: Added Camera/MIC pins
07/02/07 -- DVI: Removed SB Hotplug Detect support(muxed gfx)
0.13.0:
07/05/07 -- Aliasing: Moved pages back in sync with T9, aliasing now on separate page
07/05/07 -- Regulators: Changed L7100,L7101 to 4mm 152S0433
1.2.0:
08/02/07 -- USB: Change to active enable USB ports
08/02/07 -- Regulators: Changed U8900 to use VID instead of Feedback resistors
```

EVT

```
4.1.0:
08/09/07 -- Current Sense: Change Q5322 TO FDN337 to accommodate TH1H
08/09/07 -- Ethernet: Change T3900,T3901 to 157S0053
5.1.0:
08/13/07 -- Regulators: Change GPUVCORE VID pullup/pulldowns to 2.2K
```

DVT

```
10.0.0:
09/21/07 -- BOM OPTION: Add 2.4Ghz 256MB VRAM Config, change 2.5Ghz Conifgs to 512MB VRAM
```

Revision History

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 6 OF 89	

Functional Test Points

Fan Connectors

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	8 52
TRUE	FAN_LT_PWM	52
TRUE	FAN_LT_TACH	52
TRUE	FAN_RT_PWM	52
TRUE	FAN_RT_TACH	52

LPC+ Debug Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	8 47
TRUE	=PP5V_S0_LPCPLUS	8 47
TRUE	LPC_AD<0>	23 45 47
TRUE	LPC_AD<1>	23 45 47
TRUE	LPC_FRAME_L	23 45 47
TRUE	PM_CLKRUN_L	25 45 47
TRUE	BOOT_LPC_SPI_L	24 47
TRUE	SMC_TMS	45 46 47
TRUE	DEBUG_RESET_L	28 47
TRUE	SMC_TRST_L	45 47
TRUE	SMC_TDO	45 46 47
TRUE	SMC_MD1	45 47
TRUE	SMC_TX_L	43 45 46 47
TRUE	FWH_INIT_L	47
TRUE	PCI_CLK33M_LPCPLUS	30 47 85
TRUE	LPC_AD<2>	23 45 47
TRUE	LPC_AD<3>	23 45 47
TRUE	INT_SERIRQ	25 45 47
TRUE	PM_SUS_STAT_L	25 45 46 47
TRUE	SMC_TDI	45 46 47
TRUE	SMC_TCK	45 46 47
TRUE	SMC_RESET_L	45 46 47
TRUE	SMC_NMI	45 47
TRUE	SMC_RX_L	43 45 46 47
TRUE	LINDACARD_GPIO	25 47

Left ALS Connector

FUNC_TEST

TRUE	=PP3V3_S3_LTALS	8 79
TRUE	ALS_GAIN	45 53 79
TRUE	LTALS_OUT	53 79
TRUE	GND	

Thermal Diode Connectors

FUNC_TEST

TRUE	HSTHMSNS_D_P	51 88
TRUE	HSTHMSNS_D_N	51 88
TRUE	RSFSTHMSNS_D_P	51 88
TRUE	RSFSTHMSNS_D_N	51 88
	CPUTHMSNS_D2_P	51 88
	CPUTHMSNS_D2_N	51 88

CPUTHMSNS can not be supported due to layout constraints

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	45 46 56
TRUE	=SMBUS_BATT_SCL	48 56
TRUE	=SMBUS_BATT_SDA	48 56
TRUE	GND_BATT	56

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUS_G3H_LIO_CONN	8 56
TRUE	GND	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

RTC Battery Connector

FUNC_TEST

TRUE	PPVBATT_G3_RTC	28
TRUE	GND	

Current Sense Calibration

FUNC_TEST

TRUE	ISENSE_CAL_EN	45 49
TRUE	=PP5V_S0_ISENSECAL	8 49
TRUE	=PPVCORE_S0_CPU_REG	8 49 58
TRUE	=PPVCORE_GPU_REG	8 49 73
TRUE	GND	

2 TPs per

6 TPs, 2 with each of above TP pairs

Left Clutch Barrel Connector

FUNC_TEST

TRUE	=PP5V_S3_CAMERA	8 44
TRUE	USB_CAMERA_N	24 44 83
TRUE	USB_CAMERA_P	24 44 83
TRUE	=PP5V_S3_WWAN	8

Other Func Test Points

FUNC_TEST

TRUE	PM_SYSRST_L	25 28 45
TRUE	SMC_ONOFF_L	45 46 79

TRUE	CPU_THERMTRIP_R	23

System Validation TPs

FUNC_TEST

TRUE	CPU_PWRGD	10 13 23 80
TRUE	CPU_DPSLP_L	7 10 23 80
TRUE	PM_DPRSLPVR	16 25 58 80
TRUE	CPU_DPSLP_L	7 10 23 80
TRUE	PM_LAN_ENABLE	25 45
TRUE	PCI_RST_L	24 28
TRUE	PM_RSMRST_L	25 45
TRUE	PM_SB_PWROK	9 25 28
TRUE	SB_RTC_RST_L	23 28
TRUE	PM_STPCPU_L	25 29 30
TRUE	PM_STPPCI_L	25 29 30
TRUE	VR_PWRGD_CLKEN	25 28
TRUE	VR_PWRGOOD_DELAY	9 16 28 58
TRUE	FSB_CPURST_L	10 13 14 80
TRUE	FSB_CPUSLP_L	10 14 80
TRUE	FSB_DPWR_L	10 14 80
TRUE	NB_SB_SYNC_L	16 25

FUNC_TEST

TRUE	IMVP_VR_ON	45 58
TRUE	IMVP_DPRSLPVR	58 80
TRUE	PM_SLP_S3_L	25 36 40 45 64
TRUE	PM_S4_STATE_L	25 45 64
TRUE	PM_SLP_S5_L	25 45 46
TRUE	PM_ENET_EN	36 64
TRUE	P1V8P1V5P1V05S0_PGOOD	64
TRUE	CPU_DPRSTP_L	10 16 23 58 80
TRUE	IMVP6_VID<6..0>	12 58 80
TRUE	PLT_RST_L	24 28
	NB_RESET_L	16 28
TRUE	GPU_RESET_L	28 65
TRUE	SMC_LRESET_L	28 45
TRUE	CPU_STPCLK_L	10 23 80
TRUE	FSB_CLK_NB_P	14 30 85
TRUE	FSB_CLK_NB_N	14 30 85
TRUE	NB_CLKREQ_L	16 29
TRUE	NB_CLK100M_PCIE_P	16 30 85
TRUE	NB_CLK100M_PCIE_N	16 30 85

ICT Test Points

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	10 14 80
TRUE	FSB_ADS_L	10 14 80
TRUE	FSB_ADSTB_L<1..0>	10 14 80
TRUE	FSB_BNR_L	10 14 80
TRUE	FSB_BREQ0_L	10 14 80
TRUE	FSB_D_L<63..0>	10 14 80
TRUE	FSB_DBSY_L	10 14 80
TRUE	FSB_DINV_L<3..0>	10 14 80
TRUE	FSB_DRDY_L	10 14 80
TRUE	FSB_DSTB_L_N<3..0>	10 14 80
TRUE	FSB_DSTB_L_P<3..0>	10 14 80
TRUE	FSB_HIT_L	10 14 80
TRUE	FSB_HITM_L	10 14 80
TRUE	FSB_LOCK_L	10 14 80
TRUE	FSB_REQ_L<4..0>	10 14 80

GPU NO_TESTs

NB NO_TESTs

NO_TEST

TRUE	NC_NB_NC<1..16>	TP_NB_NC<1..16> 16

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 7 OF 89	

"G3Hot" (Always-Present) Rails

=PPBUS_G3H_LIO_CONN — PPBUS_G3H (56 7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
- =PPBUS_S5_FWPWRSW (40)
- =PPBUS_S5_P1V25S0FET (57)
- =PPVIN_S5_CPU_IMVP_VIN (58)
- =PPVIN_S5_CPU_IMVP (58)
- =PPVIN_S5_P5VP3V3 (59)
- =PPVIN_S5_P5VS5 (59)
- =PPVIN_S5_P3V3S5 (59)
- =PPVIN_ENET_P1V25ENET (60)
- =PPVIN_S3_P1V8S3 (61)
- =PPVIN_S0_P1V5S0 (62)
- =PPVIN_S0_P1V8FB (77)
- =PPVIN_S0_P1V05S0 (60)
- =PPVIN_GPU_GPUVCORE (73)

=PPDCIN_G3H_LIO_CONN (34) — PPDCIN_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPVIN_G3H_P3V42G3H (64)

=PP3V42_G3H_REG (64) — PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V42_G3H_SB_RTC (28)
- =PP3V42_G3H_LIO (34)
- =PP3V42_G3H_SMCUSBMUX (43)
- =PP3V42_G3H_SMBUS_SMC_BSA (48)
- =PP3V42_G3H_LIDSWITCH (79)
- =PP3V3_S5_SMC (45 46)
- =PP3V3_S5_LPCPLUS (7 47)
- =PPVIN_S5_SMCVREF (46)
- =PP3V42_G3H_PWRCTL (64)

5V Rails

=PP5V_S5_REG (59) — PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S5_SB (27)
- =PP5V_S5_P1V8FB (77)
- =PP5V_S5_P1V25S0FET (57)
- =PP5V_S5_P1V25ENET (60)
- =PP5V_S5_P1V05S0 (60)
- =PP5V_S5_P1V8DDRREG (61)
- =PP5V_S5_PWRCTL (64)
- =PP5V_S5_GPUVCORE (73)
- =PP5V_S3_RTUSB (43)
- =PP5V_S3_P5VS3FET (57)
- =PP5V_S0_P5VS0FET (57)

=PP5V_S3_FET (57) — PP5V_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S3_SYSLED (46)
- =PP5V_S3_CAMERA (7 44)
- =PP5V_S3_WWAN (7)
- =PP5V_S3_IR (79)
- =PP5V_S3_TOPCASE (79)
- =PP5V_S0_KBDLED (53)
- =PP5V_S0_ISENSECAL (7 49)
- =PP5V_S5_P1V5S0 (62)

=PP5V_S0_FET (57) — PP5V_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_SB (27)
- =PP5V_S0_ODD (42)
- =PP5V_S0_LPCPLUS (7 47)
- =PP5V_S0_FAN_LT (7 52)
- =PP5V_S0_FAN_RT (52)
- =PP5V_S0_CPU_IMVP (58)
- =PP5V_S0_DVI_DDC (78)
- =PP5V_S0_HDD (79)
- =PP5V_S0_ODDPWREN (42)
- =PP5V_S0_PCIREQFIX (42)
- =PP5V_S0_MIC

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG (58 49 7) — PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU (11 12 49)

=PPVCORE_S0_NB_GFX (18)

3.3V-2.5V Rails

=PP3V3_S5_REG (59) — PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S5_SB_PM (28)
- =PP3V3_S5_SB_CLINK (24)
- =PP3V3_S5_SB (25 27)
- =PP3V3_S5_SB_CLINK1 (25)
- =PP3V3_S5_SB_GPIO (25)
- =PP3V3_S5_SB_3V3_VCCSUSHDA (26 27)
- =PP3V3_S5_SB_VCCSUS3_3 (26 27)
- =PP3V3_S5_SB_VCCSUS3_3_USB (26 27)
- =PP3V3_S5_S5PWRGD (46)
- =PP3V3_S5_SMBUS_SB_ME (48)
- =PP3V3_S5_ROM (55)
- =PP3V3_S5_P1V5P1V05PG (64)
- =PP3V3_S3_P3V3S3FET (57)
- =PP3V3_S0_LCD (74)
- =PP3V3_S0_P3V3S0FET (57)
- =PP3V3_GPU_P3V3GPUFET (57)
- =PP3V3_S5_PWRCTL (64)

=PP3V3_S3_FET (57) — PP3V3_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S3_P3V3ENETFET (36)
- =PP3V3_S3_FW (38)
- =PP3V3_S3_PCI (38)
- =PP3V3_S3_SMBUS_SMC_A_S3 (48)
- =PP3V3_S3_RTALS (53)
- =PP3V3_S3_SMS (54)
- =PP3V3_S3_SMBUS_SMC_MGMT (48)
- =PP3V3_S3_P1V8ISNS (50)
- =PP3V3_S3_LTALS (7 79)
- =PP3V3_S3_TOPCASE (79)
- =PP3V3_S3_REMTHMSNS (51)
- =PP3V3_S3_PWRCTL (64)

=PP3V3_S0_FET (57) — PP3V3_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S0_NB_VCCHV (16 19 21)
- =PP3V3_S0_NB_VCCA_PEG_BG (19 21)
- =PP3V3_S0_NB_FOLLOW (21)
- =PP3V3_S0_SB_GPIO (23 25)
- =PP3V3_S0_SB_PCI (24)
- =PP3V3_S0_SB_VCC3_3_IDE (26 27)
- =PP3V3_S0_SB_VCC3_3_PCI (26 27)
- =PP3V3R1V5_S0_SB_VCCHDA (26 27)
- =PP3V3_S0_SB_VCC3_3_DMI (26 27)
- =PP3V3_S0_SB_VCC3_3_VCCPCORE (26)
- =PP3V3_S0_SB_VCCGLAN3_3 (26)
- =PP3V3_S0_SB_VCC3_3_SATA (26 27)
- =PP3V3_S0_SB (27)
- =PP3V3_S0_SB_PM (28)
- =PP3V3_S0_RSTBUF (28)
- =PP3V3_S0_CK505 (29 30)
- =PP3V3_S0_IDE (42)
- =PP3V3_S0_SMC (46)
- =PP3V3_S0_LPCPLUS (47)
- =PP3V3_S0_SMBUS_SB (48)
- =PP3V3_S0_SMBUS_SMC_B_S0 (48)
- =PP3V3_S0_CPUCOREISNS (50)
- =PP3V3_S0_GPU1V8ISNS (50)
- =PP3V3_S0_CPUTHMSNS (51)
- =PP3V3_S0_GPUTHMSNS (51)
- =PP3V3_S0_FAN_LT (52)
- =PP3V3_S0_FAN_RT (52)
- =PP3V3_S0_IMVP (58)
- =PP3V3_S0_NBCOREISNS (50)
- =PP3V3_S0_ALLSYSPG (64)
- =PP3V3_S0_DDC_LCD (74)
- =PP3V3R5V_GPU_GPUISENS (50)
- =PP3V3_S0_XDP (13)
- =PP3V3_S0M_CK505 (29 30)
- =PPSPD_S0M_MEM_A (31)
- =PPSPD_S0M_MEM_B (32)
- =PP3V3_S0MWOL_SB_CLINK0 (25)
- =PP3V3_S0MWOL_SB_VCCCL3_3 (26 27)
- =PP3V3_S0MWOL_SB_VCCLAN3_3 (26 27)
- =PP3V3_S0_PWRCTL (64)
- =PP3V3_S0_CCP2
- =PP3V3_S0_P1V25ISNS (50)

=PP1V25_S0_FET (57) — PP1V25_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V25_S0_ISNS_R (50)

1.8V-0.9V Rails

=PP1V8_S3_REG (61) — PP1V8_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S3_FW (38)
- =PP1V8_S3M_MEM_A (31 88)
- =PP1V8_S3M_MEM_B (32 88)
- =PP1V8_S3_ISNS_R (50)

=PP1V8_S3_ISNS (50) — PP1V8_S3_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S3M_NB_VCC (21)
- =PP1V8_S3M_MEM_NB (16 18 21)

=PP1V5_S0_REG (62) — PP1V5_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
MAX I = ?.??A
- =PP1V5_S0_CPU (11 12)
- =PP1V5_S0_NB_TVDAC (22)
- =PP1V5_S0_SB (27)
- =PP1V5_S0_SB_VCC1_5_A_ARX (26 27)
- =PP1V5_S0_SB_VCC1_5_A_ATX (26 27)
- =PP1V5_S0_SB_VCC1_5_A (26)
- =PP1V5_S0_SB_VCCUSBPLL (26 27)
- =PP1V5_S0_SB_VCC1_5_A_USB_CORE (26 27)
- =PP1V5_S0_LIO (34)

=PP1V25_S0_ISNS (50) — PP1V25_S0_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V25_S0M_NB_PLL (21)
- =PP1V25_S0M_NB_VCC (21)
- =PP1V25_S0M_NB_VCCA (21)
- =PP1V25_S0_NB_VCCDMI (19 21)
- =PP1V25_S0_NB_PLL (21)
- =PP1V25_S0_NB_VCC (21)
- =PP1V25_S0_SB_DMI (26 27)
- =PP1V2_GPU_PEX_IOVDDQ (65)
- =PP1V2_GPU_PEX_IOVDD (65)
- =PP1V2_GPU_PEX_PLLXVDD (65)
- =PP1V2_GPU_PLLVDD (70)
- =PP1V2_GPU_H_PLLVDD (70)
- =PP1V2_GPU_VID_PLLVDD (70)
- =PP1V2_GPU_FBPLLAVDD (67)

=PP1V05_S0_REG (60) — PP1V05_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0M_NB_VCCAXM (18 21)
- =PP1V05_S0_CPU (10 11 12 13)
- =PP1V05_S0_NB_FOLLOW (21)
- =PP1V05_S0_NB_PCIE (21)
- =PP1V05_S0_SB_CPU_IO (23 26 27)
- =PP1V05_S0_SMC_LS (46)
- =PP1V25R1V05_S0_FSB_NB (14 30)
- =PP1V25R1V05_S0_NB_VTT (19 21)
- =PPVCORE_S0_NBCOREISNS (50)
- =PPVCORE_S0_NB_FOLLOW (21)
- =PPVCORE_S0_SB (26 27 73 49 7)

=PPVCORE_S0_NB_R (50) — PPVCORE_S0_NB_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PPVCORE_S0_NB (18 21)

=PP0V9_S3_VTTR_BUF (61) — PP0V9_S3_MEM_VREF
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PP0V9_S3M_MEM_NBVREFA (16)
- =PP0V9_S3M_MEM_NBVREFB (16)
- =PP0V9_S3M_MEM_DIMMVREFA (31)
- =PP0V9_S3M_MEM_DIMMVREFB (32)

=PP0V9_S0_VTT_LDO (61) — PP0V9_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PP0V9_S0M_MEM_TERM (33)

"ENET" Rails

=PP3V3_ENET_FET (36) — PP3V3_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_ENET_PHY (35)
- =PP3V3_ENET_AVDDLDO (36)

=PPVOUT_ENET_AVDDLDO (36) — PP1V9_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.9V
MAKE_BASE=TRUE
- =PP1V8R2V5_ENET_PHY (35)

=PP1V25_ENET_REG (60) — PP1V25_ENET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V2_ENET_PHY (35)
- =PP1V25_S0_P1V25S0FET (57)

=YUKON_EC_PP2V5_ENET (35)
Yukon EC will not be supported

"FW" (FireWire) Rails

=PPBUS_FW_FWPWRSW_F (40) — =PPBU_S0_P3V3FW (63)
MAKE_BASE=TRUE

=PPBUS_S5_FW_FET (40) — PPVP_FW
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=8V
MAKE_BASE=TRUE
- =PPVP_FW_SUMNODE (40)
- =PPVP_FW_CPS (39)
- =PPVP_FW_P3V3FW (63)

PPVP_FW_PORTA_UF (40) — =PPVP_FW_PORT0 (41)
MAKE_BASE=TRUE

PPVP_FW_PORTB_UF (40) — =PPVP_FW_PORT1 (41)
MAKE_BASE=TRUE

=PP3V3_FW_REG (63) — PP3V3_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_FW_PHY (39 41)
- =PP3V3_FW_LATEVG_ACTIVE (40)
- =PP3V3_FW_LATEVG (41)
- =PPVIN_FW_P1V95FW (63)

=PP1V95_FW_LDO (63) — PP1V95_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.95V
MAKE_BASE=TRUE
- =PP1V95_FW_PHY (39)
- =PP1V8_FW_PHYOSC (39)

"GPU" Rails

=PP3V3_S0GPU_FET (57) — PP3V3_S0GPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_GPU_VDD33 (70)
- =PP3V3_GPU_MIO (70 71)
- =PP3V3_GPU_DAC (72)
- =PP3V3_GPU_DVI (78)
- =PP3V3_GPU_VGASYNC (78)
- =PP3V3_GPU_TMDS (71)
- =PP3V3_GPU_VIDEOMUX (71)
- =PP3V3_GPU_SMBUS_SMC_0_S0 (48)
- =PP3V3_GPU_PWRCTL (64)
- =PP3V3_GPU_VCORELOGIC (73)
- =PP3V3_GPU_HDCP (71)

=PP3V3_S0GPU_TMDS_FET (71) — PP3V3_S0GPU_TMDS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_GPU_TMDSBIAS (78)
- =PP3V3_GPU_IFPCD_IOVDD (72)

=PP1V8_S0GPU_ISNS (50) — PP1V8_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_GPU_FB_VDD (68 69 75 76)
- =PP1V8_GPU_FB_VDDQ (68 69 75 76)
- =PP1V8_GPU_FBVDDQ (66)
- =PP1V8_GPU_FBIO (67)
- =PP1V8_GPU_IFPX (72)

=PPVCORE_GPU_REG (73 49 7) — PPVCORE_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
- =PPVCORE_GPU (66)

=PP1V8_S0GPU_REG (77) — PP1V8_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S0GPU_ISNS_R (50)

Power Aliases

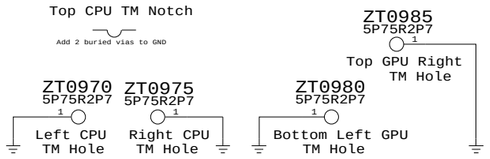
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	8	89

Thermal Module Holes



RAM Door (Torx) Holes

ZT0930
3P7R3P2
GND_CHASSIS_RAMDOOR_HOLE_0

ZT0935
3P7R3P2
GND_CHASSIS_RAMDOOR_HOLE_1

Frame Holes

ZT0920
3P2R2P7
GND_CHASSIS_LVDS_HOLE

ZT0940
3P7R3P2
GND_CHASSIS_RIGHT_FAN_HOLE

Board Edge Notches
(Can't be PTH)

ZT0945
HOLE-VIA-P5RP25
GND_CHASSIS_RIGHT_FAN_NOTCH

ZT0950
HOLE-VIA-P5RP25
GND_CHASSIS_DIMM_NOTCH

ZT0955
3P2R2P7
GND_CHASSIS_LIOFLEX_HOLE

ZT0965
3P2R2P7
GND_CHASSIS_LINDACARD_HOLE

Tooling Holes
(Can't be PTH)

ZT0960
HOLE-VIA-P5RP25
GND_CHASSIS_BATTCONN_HOLE

ZT0990
HOLE-VIA-P5RP25
GND_CHASSIS_DVI_HOLE

SH0925
0G-503040
SHLD-SM-LF

EXTGPU_PWR_EN — TP_EXTGPU_PWR_EN (MAKE_BASE=TRUE)
TP_USB_EXTDP — USB_EXTD_P (MAKE_BASE=TRUE) 24 83
TP_USB_EXTDN — USB_EXTD_N (MAKE_BASE=TRUE) 24 83

28 25 7 PM_SB_PWROK — =SB_CLINK_MPWROK (MAKE_BASE=TRUE) 25
58 28 16 7 VR_PWRGOOD_DELAY — =NB_CLINK_MPWROK (MAKE_BASE=TRUE) 16

54 SMC_SMS_INT — =SMC_SMS_INT (MAKE_BASE=TRUE) 45

65 30 PEG_CLK100M_GPU_P — PEG_CLK100M_P (MAKE_BASE=TRUE) 85
65 30 PEG_CLK100M_GPU_N — PEG_CLK100M_N (MAKE_BASE=TRUE) 85

TP_MEM_A_A<15> — MEM_A_A<15> (MAKE_BASE=TRUE) 31
TP_MEM_B_A<15> — MEM_B_A<15> (MAKE_BASE=TRUE) 32
TP_USB_EXTCP — USB_EXTC_P (MAKE_BASE=TRUE) 24 83
TP_USB_EXTCN — USB_EXTC_N (MAKE_BASE=TRUE) 24 83

84 24 INT_PIRQE_L — IPHS_SW_INT (MAKE_BASE=TRUE) 34
25 SB_SLOAD — IPHS_SW_BIAS_EN_L (MAKE_BASE=TRUE) 34

Digital Ground

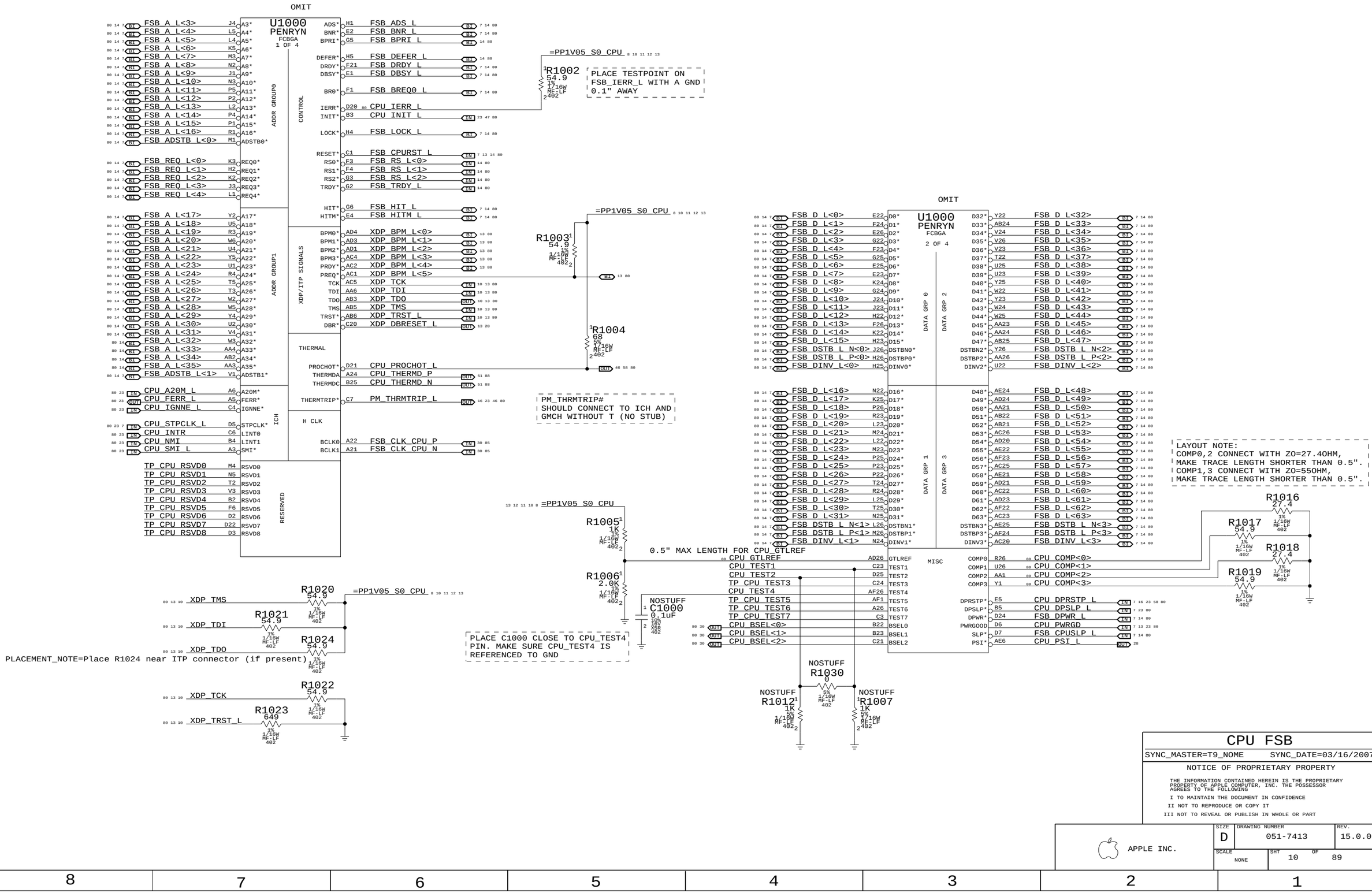
GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

Signal Aliases

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 9 OF 89	



CPU FSB

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 10 OF 89	

(CPU CORE POWER)
=PPVCORE_S0_CPU 8 11 12 49

Standard Voltage:	Low Voltage:	Ultra Low Voltage:
44.0 A (Design Target)	23.0 A (Design Target)	17.0 A (Design Target)
41.0 A (HFM)	21.0 A (HFM)	TBD A (HFM)
30.4 A (LFM)	18.7 A (LFM)	TBD A (LFM)
25.5 A (SuperLFM)	TBD A (SuperLFM)	
27.4 A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant LFM)
27.4 A (Sleep HFM)	TBD A (Sleep HFM)	TBD A (Sleep HFM)
16.8 A (Sleep SuperLFM)	TBD A (Sleep SuperLFM)	TBD A (Sleep LFM)
25.0 A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)	TBD A (Deep Sleep SuperLFM)	TBD A (Deep Sleep LFM)
11.5 A (Deeper Sleep)	TBD A (Deeper Sleep)	TBD A (Deeper Sleep)
9.4 A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)

OMIT
U1000
PENRYN
FCBGA
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VCC: A7 A9 A10 A12 A13 A15 A17 A18 A20 B7 B9 B10 B12 B14 B15 B17 B18 B20 C9 C10 C12 C13 C15 C17 C18 D9 D10 D12 D14 D15 D17 D18 E7 E9 E10 E12 E13 E15 E17 E18 E20 F7 F9 F10 F12 F14 F15 F17 F18 F20 AA7 AA9 AA10 AA12 AA13 AA15 AA17 AA18 AA20 AB9 AC10 AB10 AB12 AB14 AB15 AB17 AB18

VCC: AB20 AB7 AC7 AC9 AC12 AC13 AC15 AC17 AC18 AD7 AD9 AD10 AD12 AD14 AD15 AD17 AD18 AE9 AE10 AE12 AE13 AE15 AE17 AE18 AE20 AF9 AF10 AF12 AF14 AF15 AF17 AF18 AF20

(CPU IO POWER 1.05V)
=PP1V05_S0_CPU 8 10 12 13

4500 mA (before VCC stable)
2500 mA (after VCC stable)

VCCP: G21 V6 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21

(CPU INTERNAL PLL POWER 1.5V)
=PP1V5_S0_CPU 8 12

130 mA

VCCA: B26 C26

VID0	AD6	CPU_VID<0>	OUT 12 80
VID1	AF5	CPU_VID<1>	OUT 12 80
VID2	AE5	CPU_VID<2>	OUT 12 80
VID3	AF4	CPU_VID<3>	OUT 12 80
VID4	AE3	CPU_VID<4>	OUT 12 80
VID5	AF3	CPU_VID<5>	OUT 12 80
VID6	AE2	CPU_VID<6>	OUT 12 80

=PPVCORE_S0_CPU 8 11 12 49

R1100
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

VCCSENSE	AF7	CPU_VCCSENSE_P	OUT 58 80
VSSSENSE	AE7	CPU_VCCSENSE_N	OUT 58 80

R1101
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

OMIT
U1000
PENRYN
FCBGA
4 OF 4

VSS: A4 A8 A11 A14 A16 A19 A23 AF2 B6 B8 B11 B13 B16 B19 B21 B24 C5 C8 C11 C14 C16 C19 C2 C22 C25 D1 D4 D8 D11 D13 D16 D19 D23 D26 E3 E6 E8 E11 E14 E16 E19 E21 E24 F5 F8 F11 F13 F16 F19 F2 F22 F25 G4 G1 G23 G26 H3 H6 H21 H24 J2 J5 J22 J25 K1 K4 K23 K26 L3 L6 L21 L24 M2 M5 M22 M25 N1 N4 N23 N26 P3 B1

VSS: P6 P21 P24 R2 R5 R22 R25 T1 T4 T23 T26 U3 U6 U21 U24 V2 V5 V22 V25 W1 W4 W23 W26 Y3 Y6 Y21 Y24 AA2 AA5 AA8 AA11 AA14 AA16 AA19 AA22 AA25 AB1 AB4 AB8 AB11 AB13 AB16 AB19 AB23 AB26 AC3 AC6 AC8 AC11 AC14 AC16 AC19 AC21 AC24 AD2 AD5 AD8 AD11 AD13 AD16 AD19 AD22 AD25 AE1 AE4 AE8 AE11 AE14 AE16 AE19 AE23 AE26 A2 AF6 AF8 AF11 AF13 AF16 AF19 AF21 A25 AF25

CPU Power & Ground

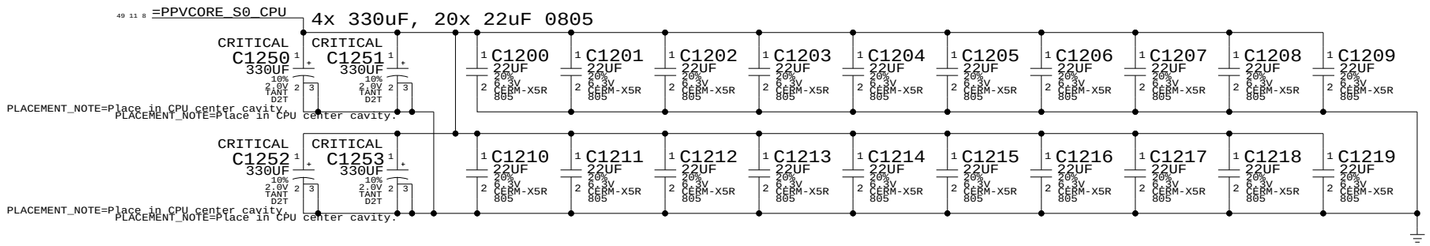
SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

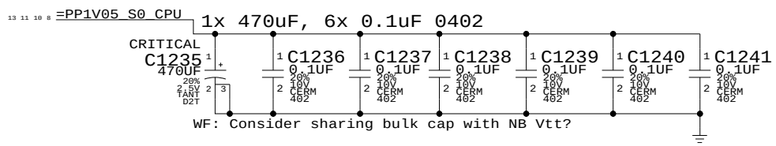
SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 11 OF 89	

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

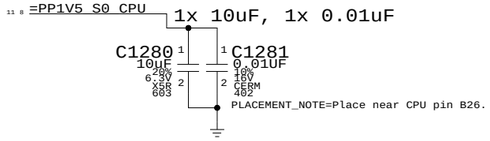
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU VCORE VID CONNECTIONS

80 11 CPU_VID<0..6> ═══ IMVP6_VID<0..6> 7 58 80

MAKE_BASE=TRUE

CPU Decoupling & VID

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

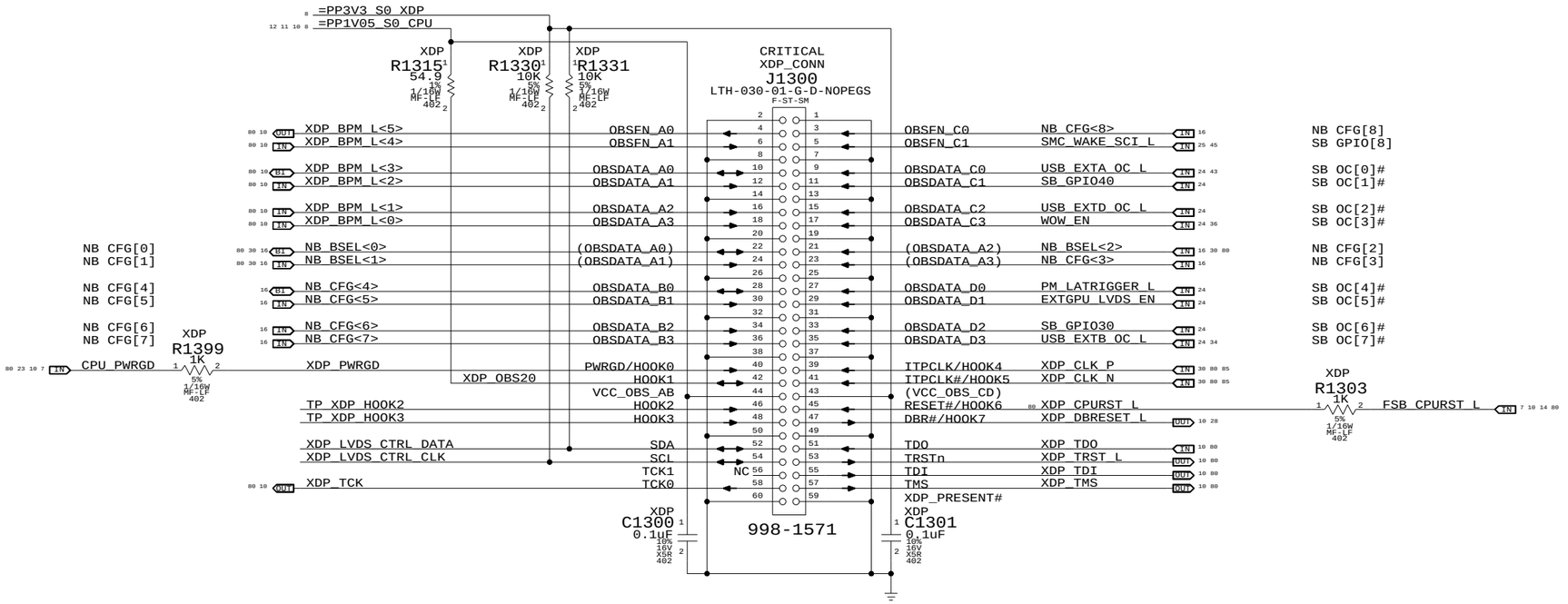
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 12 OF 89	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

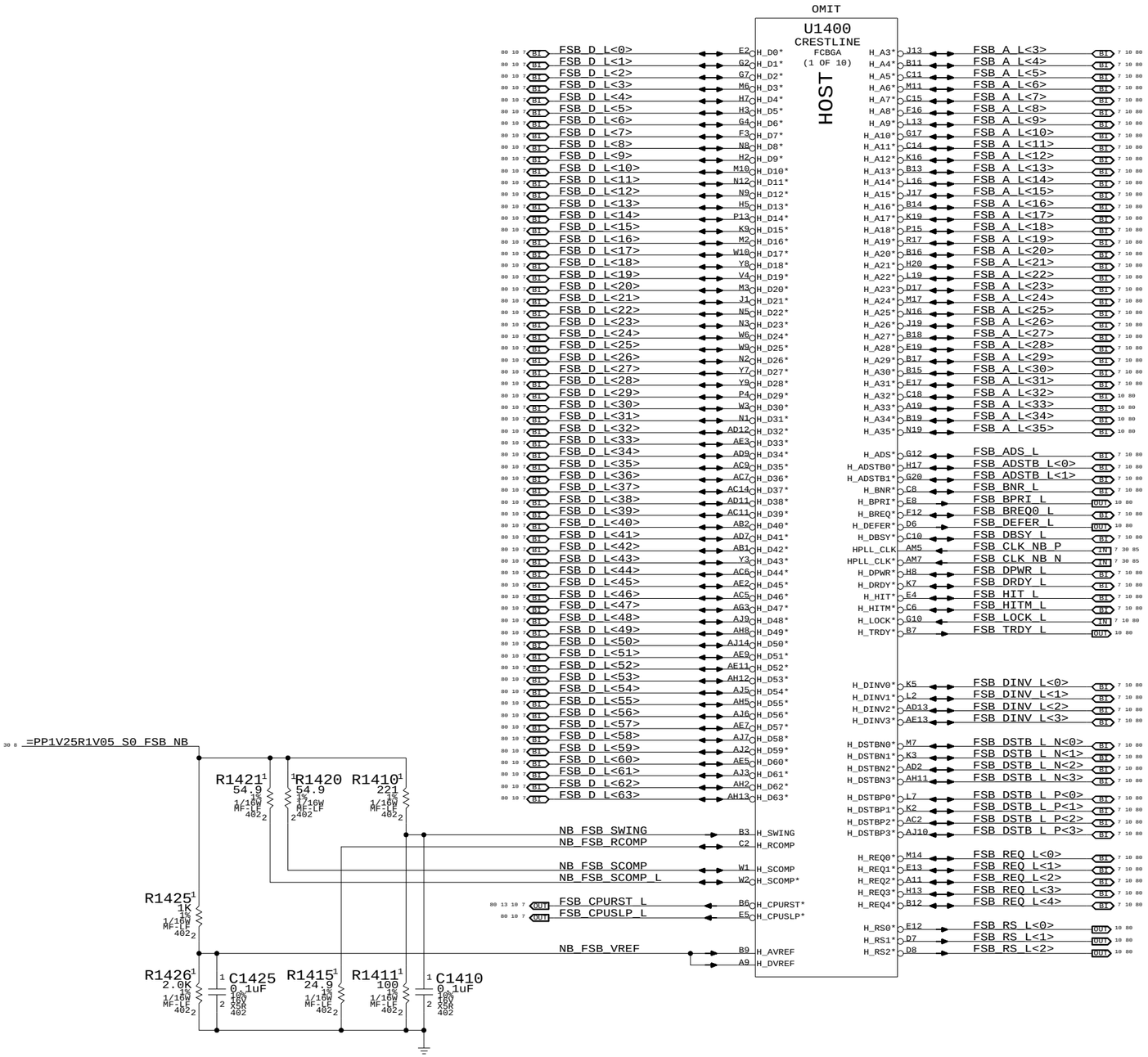
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

SYNC_MASTER=T9_NOME SYNC_DATE=12/12/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 13 OF 89	



NB CPU Interface

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 14 OF 89	

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND.
All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

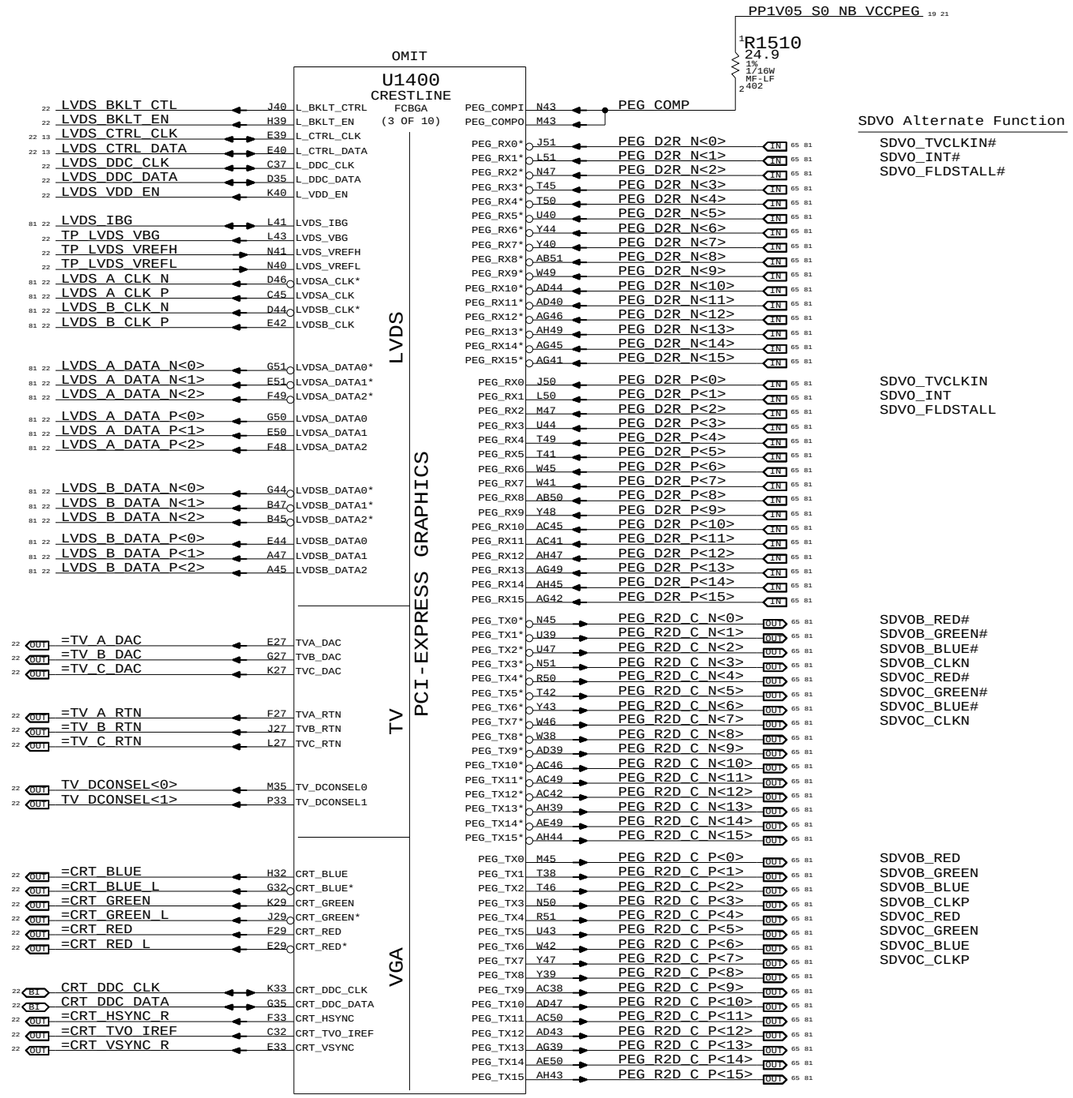
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 15 OF 89	

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB_CFG<5> 13 16
NBCFG_DMI_X2
R1655 3.9K 5% 1/16W MF-LF 402

NB_CFG<9> 16
NBCFG_PEG_REVERSE
R1659 3.9K 5% 1/16W MF-LF 402

NB_CFG<16> 16
NBCFG_DYN_ODT_DISABLE
R1666 3.9K 5% 1/16W MF-LF 402

=PP3V3_S0_NB_VCCHV 8 16 19 21
NBCFG_DMI_REVERSE
R1669 3.9K 5% 1/16W MF-LF 402
NB_CFG<19> 16

=PP3V3_S0_NB_VCCHV 8 16 19 21
NBCFG_SDVO_AND_PCIE
R1670 3.9K 5% 1/16W MF-LF 402
NB_CFG<20> 16

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

21 19 16 8 =PP3V3_S0_NB_VCCHV
R1630 10K 5% 1/16W MF-LF 402
R1631 10K 5% 1/16W MF-LF 402
45 31 IN PM_EXTTS_L<0>
45 32 IN PM_EXTTS_L<1>

OMIT

U1400
CRESTLINE
FCBGA
(2 OF 10)

TP_NB_RSVD<1>	P36	RSVD1		
TP_NB_RSVD<2>	P37	RSVD2		
TP_NB_RSVD<3>	R35	RSVD3		
TP_NB_RSVD<4>	N35	RSVD4		
TP_NB_RSVD<5>	AR12	RSVD5		
TP_NB_RSVD<6>	AR13	RSVD6		
TP_NB_RSVD<7>	AM12	RSVD7		
TP_NB_RSVD<8>	AN13	RSVD8		
TP_NB_RSVD<9>	J12	RSVD9		
TP_NB_RSVD<10>	AR37	RSVD10		
TP_NB_RSVD<11>	AM36	RSVD11		
TP_NB_RSVD<12>	AL36	RSVD12		
TP_NB_RSVD<13>	AM37	RSVD13		
TP_NB_RSVD<14>	D20	RSVD14		
TP_NB_RSVD<20>	H10	RSVD20		
TP_NB_RSVD<21>	B51	RSVD21		
TP_NB_RSVD<22>	BJ20	RSVD22		
TP_NB_RSVD<23>	BK22	RSVD23		
TP_NB_RSVD<24>	BF19	RSVD24		
TP_NB_RSVD<25>	BH20	RSVD25		
TP_NB_RSVD<26>	BK18	RSVD26		
TP_NB_RSVD<27>	BJ18	RSVD27		
TP_MEM_CLKP2	BF23	SM_CK2		
TP_MEM_CLKN2	BG23	SM_CK2*		
TP_MEM_CLKP5	BC23	SM_CK5		
TP_MEM_CLKN5	BD24	SM_CK5*		
82 33 31 OUT MEM_A_A<14>	BJ29	SA_MA14		
82 33 32 OUT MEM_B_A<14>	BE24	SB_MA14		
TP_NB_RSVD<34>	BH39	RSVD34		
TP_NB_RSVD<35>	AW20	RSVD35		
TP_NB_RSVD<36>	BK20	RSVD36		
TP_LVDS_A_DATAN3	C48	RSVD37		
TP_LVDS_A_DATAP3	D47	RSVD38		
TP_LVDS_B_DATAN3	B44	RSVD39		
TP_LVDS_B_DATAP3	C44	RSVD40		
TP_NB_RSVD<41>	A35	RSVD41		
TP_NB_RSVD<42>	B37	RSVD42		
TP_NB_RSVD<43>	B36	RSVD43		
TP_NB_RSVD<44>	B34	RSVD44		
TP_NB_RSVD<45>	C34	RSVD45		
80 30 13 IN NB_BSEL<0>	P27	CFG0		
80 30 13 IN NB_BSEL<1>	N27	CFG1		
80 30 13 IN NB_BSEL<2>	N24	CFG2		
13 OUT NB_CFG<3>	C21	CFG3	IPU	
13 B1 NB_CFG<4>	C23	CFG4	IPU	
16 13 B1 NB_CFG<5>	F23	CFG5	IPU	
13 OUT NB_CFG<6>	N23	CFG6	IPU	
13 OUT NB_CFG<7>	G23	CFG7	IPU	
13 OUT NB_CFG<8>	J20	CFG8	IPU	
16 NB_CFG<9>	C20	CFG9	IPU	
TP_NB_CFG<10>	R24	CFG10	IPU	
TP_NB_CFG<11>	L23	CFG11	IPU	
TP_NB_CFG<12>	J23	CFG12	IPU	
TP_NB_CFG<13>	E23	CFG13	IPU	
TP_NB_CFG<14>	E20	CFG14	IPU	
TP_NB_CFG<15>	K23	CFG15	IPU	
16 NB_CFG<16>	M20	CFG16	IPU	
TP_NB_CFG<17>	M24	CFG17	IPU	
TP_NB_CFG<18>	L32	CFG18	IPD	
16 NB_CFG<19>	N33	CFG19	IPD	
16 NB_CFG<20>	L35	CFG20	IPD	
25 OUT PM_BMBUSY_L	G41	PM_BM_BUSY*		
80 58 23 10 7 IN CPU_DPRSTP_L	L39	PM_DPRSTP*		
	L36	PM_EXT_TS0*		
	J36	PM_EXT_TS1*		
58 28 9 7 IN VR_PWRGOOD_DELAY	AW49	PWROK		
28 7 IN NB_RESET_L	AV20	RSTIN*		
80 46 23 10 OUT PM_THRMTRIP_L	N20	THERMTRIP*		
80 58 25 7 IN PM_DPRSLPVR	G36	DPRSLPVR		
7 TP_NB_NC<1>	BJ51	NC1		
7 TP_NB_NC<2>	BK51	NC2		
7 TP_NB_NC<3>	BK50	NC3		
7 TP_NB_NC<4>	BL50	NC4		
7 TP_NB_NC<5>	BL49	NC5		
7 TP_NB_NC<6>	BL3	NC6		
7 TP_NB_NC<7>	BL2	NC7		
7 TP_NB_NC<8>	BK1	NC8		
7 TP_NB_NC<9>	BJ1	NC9		
7 TP_NB_NC<10>	E1	NC10		
7 TP_NB_NC<11>	A5	NC11		
7 TP_NB_NC<12>	C51	NC12		
7 TP_NB_NC<13>	B50	NC13		
7 TP_NB_NC<14>	A50	NC14		
7 TP_NB_NC<15>	A49	NC15		
7 TP_NB_NC<16>	BK2	NC16		

RSVD | DDR MUXING | CFG | DMI | PM | GRAPHICS VID | CLK | ME | NC | MISC

SM_CK0	AV29	MEM_CLK_P<0>	OUT 31 82
SM_CK1	BB23	MEM_CLK_P<1>	OUT 31 82
SM_CK3	BA25	MEM_CLK_P<3>	OUT 32 82
SM_CK4	AV23	MEM_CLK_P<4>	OUT 32 82
SM_CK0*	AW30	MEM_CLK_N<0>	OUT 31 82
SM_CK1*	BA23	MEM_CLK_N<1>	OUT 31 82
SM_CK3*	AW25	MEM_CLK_N<3>	OUT 32 82
SM_CK4*	AW23	MEM_CLK_N<4>	OUT 32 82
SM_CKE0	BE29	MEM_CKE<0>	OUT 31 33 82
SM_CKE1	AY32	MEM_CKE<1>	OUT 31 33 82
SM_CKE3	BD39	MEM_CKE<3>	OUT 32 33 82
SM_CKE4	BG37	MEM_CKE<4>	OUT 32 33 82
SM_CS0*	BG20	MEM_CS_L<0>	OUT 31 33 82
SM_CS1*	BK16	MEM_CS_L<1>	OUT 31 33 82
SM_CS2*	BG16	MEM_CS_L<2>	OUT 32 33 82
SM_CS3*	BE13	MEM_CS_L<3>	OUT 32 33 82
SM_ODT0	BH18	MEM_ODT<0>	OUT 31 33 82
SM_ODT1	BJ15	MEM_ODT<1>	OUT 31 33 82
SM_ODT2	BJ14	MEM_ODT<2>	OUT 32 33 82
SM_ODT3	BE16	MEM_ODT<3>	OUT 32 33 82
SM_RCOMP	BL15	MEM_RCOMP	
SM_RCOMP*	BK14	MEM_RCOMP_L	
SM_RCOMP_VOH	BK31	MEM_RCOMP_VOH	
SM_RCOMP_VOL	BL31	MEM_RCOMP_VOL	
SM_VREF0	AR49	=PP0V9_S3M_MEM_NBVREFA	IN 8
SM_VREF1	AW4	=PP0V9_S3M_MEM_NBVREFB	IN 8
DPLL_REF_CLK	B42	=NB_CLK96M_DOT_P	IN 22
DPLL_REF_CLK*	C42	=NB_CLK96M_DOT_N	IN 22
DPLL_REF_SSCLK	H48	=NB_CLK100M_DPLLSS_P	IN 22
DPLL_REF_SSCLK*	H47	=NB_CLK100M_DPLLSS_N	IN 22
PEG_CLK	K44	NB_CLK100M_PCIE_P	IN 7 30 85
PEG_CLK*	K45	NB_CLK100M_PCIE_N	IN 7 30 85
		Clk used for PEG and DMI	
DMI_RXN0	AN47	DMI_S2N_N<0>	IN 24 81
DMI_RXN1	AJ38	DMI_S2N_N<1>	IN 24 81
DMI_RXN2	AN42	DMI_S2N_N<2>	IN 24 81
DMI_RXN3	AN46	DMI_S2N_N<3>	IN 24 81
DMI_RXP0	AM47	DMI_S2N_P<0>	IN 24 81
DMI_RXP1	AJ39	DMI_S2N_P<1>	IN 24 81
DMI_RXP2	AN41	DMI_S2N_P<2>	IN 24 81
DMI_RXP3	AN45	DMI_S2N_P<3>	IN 24 81
DMI_TXN0	AJ46	DMI_N2S_N<0>	OUT 24 81
DMI_TXN1	AJ41	DMI_N2S_N<1>	OUT 24 81
DMI_TXN2	AM40	DMI_N2S_N<2>	OUT 24 81
DMI_TXN3	AM44	DMI_N2S_N<3>	OUT 24 81
DMI_TXP0	AJ47	DMI_N2S_P<0>	OUT 24 81
DMI_TXP1	AJ42	DMI_N2S_P<1>	OUT 24 81
DMI_TXP2	AM39	DMI_N2S_P<2>	OUT 24 81
DMI_TXP3	AM43	DMI_N2S_P<3>	OUT 24 81
GFX_VID0	E35	GFX_VID<0>	OUT
GFX_VID1	A39	GFX_VID<1>	OUT 22
GFX_VID2	C38	GFX_VID<2>	OUT 22
GFX_VID3	B39	GFX_VID<3>	OUT 22
GFX_VR_EN	E36	GFX_VID<4>	OUT 22
		=GFX_VR_EN	OUT 22
CL_CLK	AM49	CLINK_NB_CLK	B1 25 84
CL_DATA	AK50	CLINK_NB_DATA	B1 25 84
CL_PWROK	AT43	=NB_CLINK_MPWROK	IN 9
CL_RST*	AN49	CLINK_NB_RESET_L	OUT 25 84
CL_VREF	AM50	84 NB_CLINK_VREF	
SDVO_CTRL_CLK	H35	SDVO_CTRLCLK	B1 22
SDVO_CTRL_DATA	K36	SDVO_CTRLDATA	B1 22
CLKREQ*	G39	NB_CLKREQ_L	OUT 7 29
ICH_SYNC*	G40	NB_SB_SYNC_L	OUT 7 25
TEST1	A37	NB_TEST1	
TEST2	R32	NB_TEST2	

21 18 8 =PP1V8_S3M_MEM_NB
R1610 20 5% 1/10W MF-LF 402
R1620 1K 1% 1/16W MF-LF 402
C1623 0.01UF 10% 16V CERM 402
C1622 2.2UF 20% 6.3V CERM1 603
R1622 3.01K 1% 1/16W MF-LF 402
R1611 20 5% 1/10W MF-LF 402
C1625 0.01UF 10% 16V CERM 402
C1624 2.2UF 20% 6.3V CERM1 603
R1624 1K 1% 1/10W MF-LF 402
C1615 0.1UF 20% 10V CERM 402
C1616 0.1UF 20% 10V CERM 402

PP1V25_S0M_NB_VCCAXD 19 21
R1640 1K 1% 1/16W MF-LF 402
C1640 0.1uF 20% 10V CERM 402
R1641 392 1% 1/16W MF-LF 402

R1691 20K 5% 1/16W MF-LF 402
R1690 0 5% 1/16W MF-LF 402

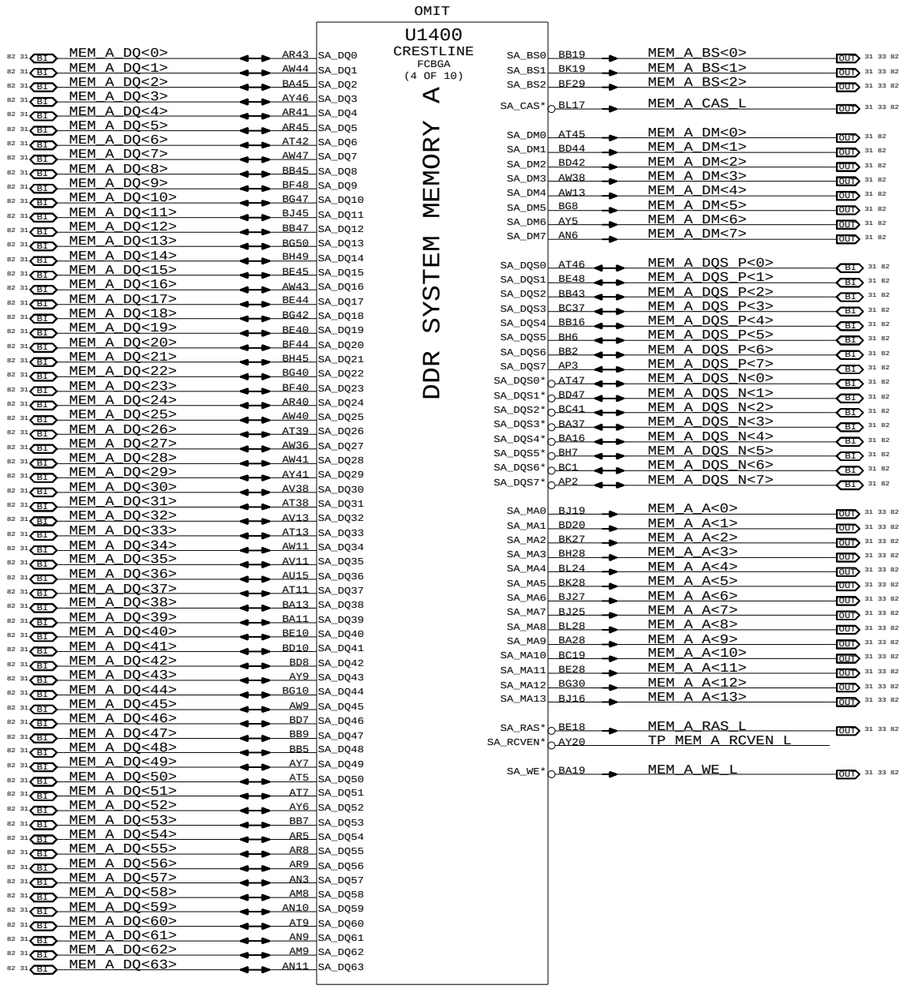
NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

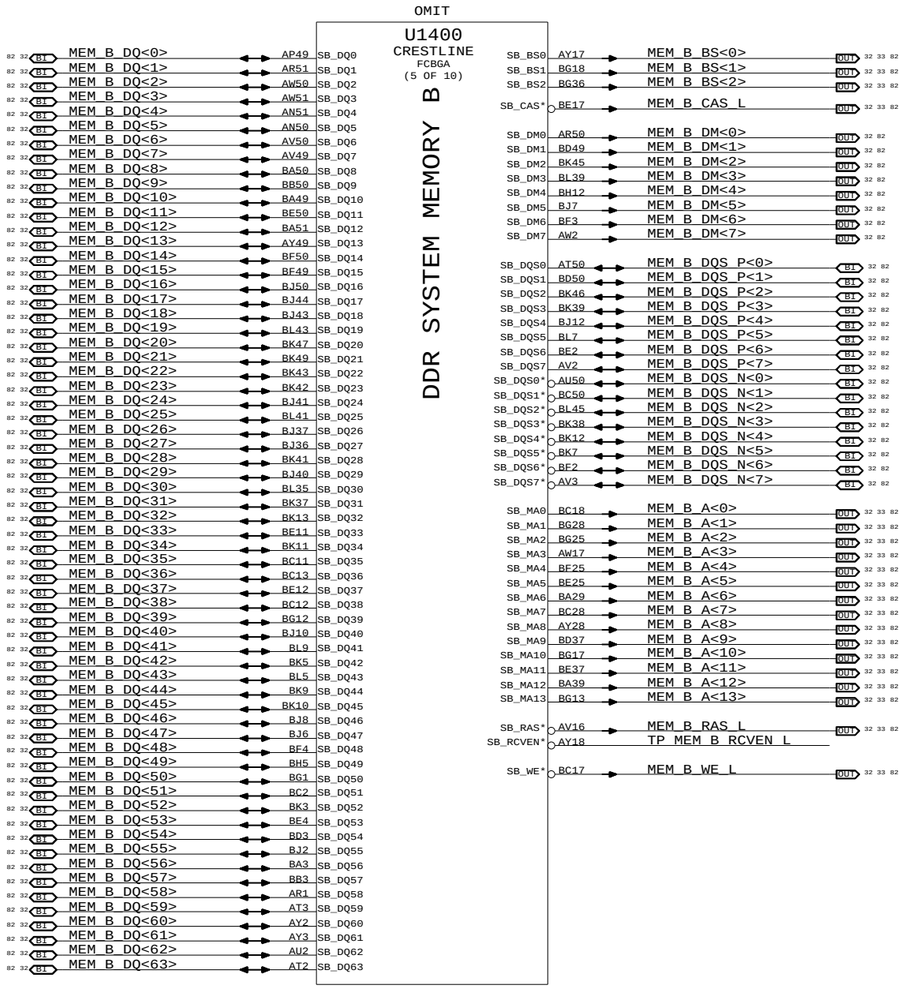
NB Misc Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 16 OF 89	





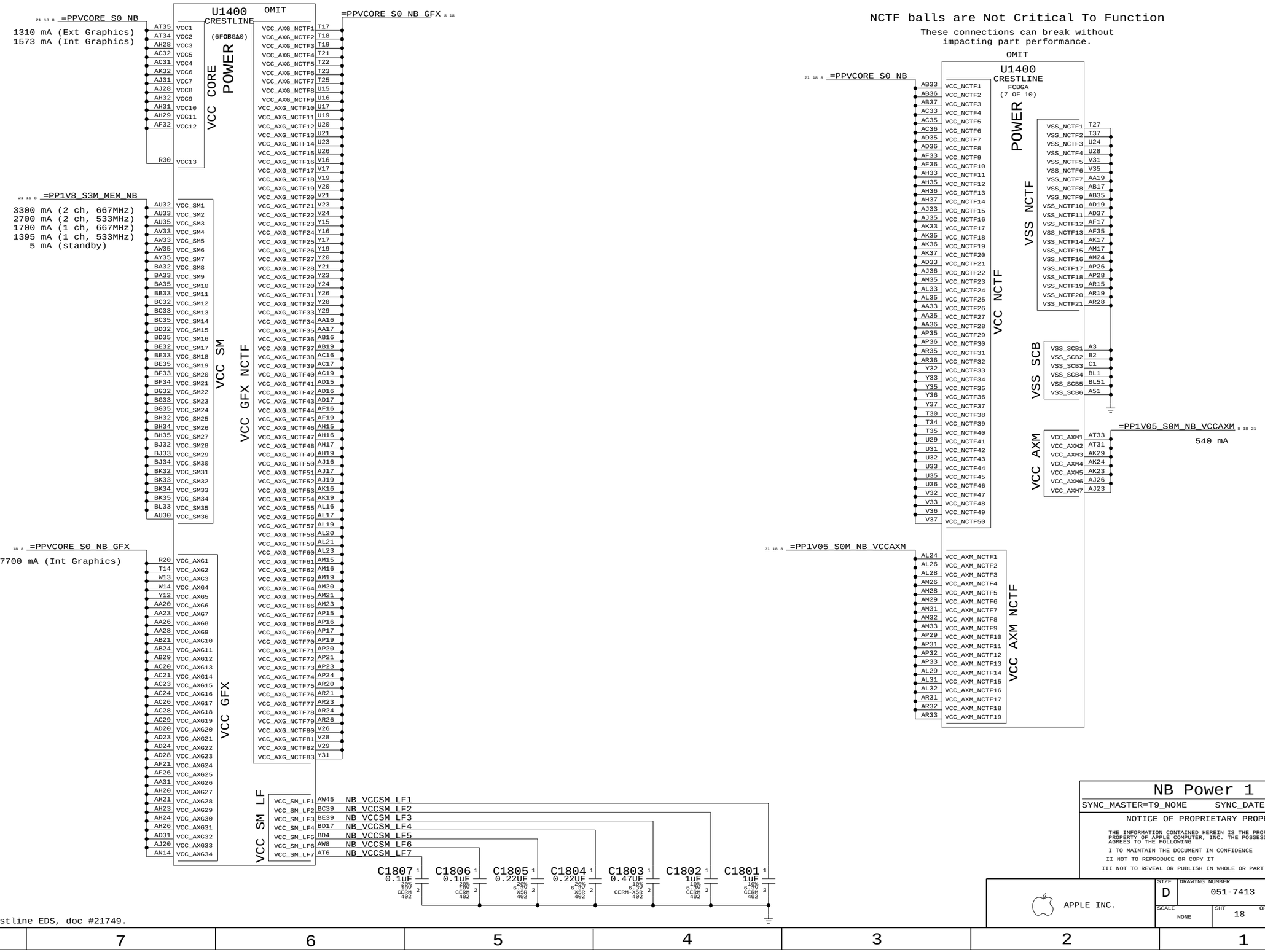
NB DDR2 Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	17	89


U1400
CRESTLINE
(6 OF 10)
FCBGA
OMIT
=PPVCORE_S0_NB
1310 mA (Ext Graphics)
1573 mA (Int Graphics)
VCC CORE POWER
AT35 VCC1
AT34 VCC2
AH28 VCC3
AC32 VCC5
AC31 VCC4
AK32 VCC6
AJ31 VCC7
AJ28 VCC8
AH32 VCC9
AH31 VCC10
AH29 VCC11
AF32 VCC12
R30 VCC13
=PPVCORE_S0_NB_GFX
VCC_AXG_NCTF1 T17
VCC_AXG_NCTF2 T18
VCC_AXG_NCTF3 T19
VCC_AXG_NCTF4 T21
VCC_AXG_NCTF5 T22
VCC_AXG_NCTF6 T23
VCC_AXG_NCTF7 T25
VCC_AXG_NCTF8 U15
VCC_AXG_NCTF9 U16
VCC_AXG_NCTF10 U17
VCC_AXG_NCTF11 U19
VCC_AXG_NCTF12 U20
VCC_AXG_NCTF13 U21
VCC_AXG_NCTF14 U23
VCC_AXG_NCTF15 U26
VCC_AXG_NCTF16 V16
VCC_AXG_NCTF17 V17
VCC_AXG_NCTF18 V19
VCC_AXG_NCTF19 V20
VCC_AXG_NCTF20 V21
VCC_AXG_NCTF21 V23
VCC_AXG_NCTF22 V24
VCC_AXG_NCTF23 Y15
VCC_AXG_NCTF24 Y16
VCC_AXG_NCTF25 Y17
VCC_AXG_NCTF26 Y19
VCC_AXG_NCTF27 Y20
VCC_AXG_NCTF28 Y21
VCC_AXG_NCTF29 Y23
VCC_AXG_NCTF30 Y24
VCC_AXG_NCTF31 Y26
VCC_AXG_NCTF32 Y28
VCC_AXG_NCTF33 Y29
VCC_AXG_NCTF34 AA16
VCC_AXG_NCTF35 AA17
VCC_AXG_NCTF36 AB16
VCC_AXG_NCTF37 AB19
VCC_AXG_NCTF38 AC16
VCC_AXG_NCTF39 AC17
VCC_AXG_NCTF40 AC19
VCC_AXG_NCTF41 AD15
VCC_AXG_NCTF42 AD16
VCC_AXG_NCTF43 AD17
VCC_AXG_NCTF44 AF16
VCC_AXG_NCTF45 AF19
VCC_AXG_NCTF46 AH15
VCC_AXG_NCTF47 AH16
VCC_AXG_NCTF48 AH17
VCC_AXG_NCTF49 AH19
VCC_AXG_NCTF50 AJ16
VCC_AXG_NCTF51 AJ17
VCC_AXG_NCTF52 AJ19
VCC_AXG_NCTF53 AK16
VCC_AXG_NCTF54 AK19
VCC_AXG_NCTF55 AL16
VCC_AXG_NCTF56 AL17
VCC_AXG_NCTF57 AL19
VCC_AXG_NCTF58 AL20
VCC_AXG_NCTF59 AL21
VCC_AXG_NCTF60 AL23
VCC_AXG_NCTF61 AM15
VCC_AXG_NCTF62 AM16
VCC_AXG_NCTF63 AM19
VCC_AXG_NCTF64 AM20
VCC_AXG_NCTF65 AM21
VCC_AXG_NCTF66 AM23
VCC_AXG_NCTF67 AP15
VCC_AXG_NCTF68 AP16
VCC_AXG_NCTF69 AP17
VCC_AXG_NCTF70 AP19
VCC_AXG_NCTF71 AP20
VCC_AXG_NCTF72 AP21
VCC_AXG_NCTF73 AP23
VCC_AXG_NCTF74 AP24
VCC_AXG_NCTF75 AR20
VCC_AXG_NCTF76 AR21
VCC_AXG_NCTF77 AR23
VCC_AXG_NCTF78 AR24
VCC_AXG_NCTF79 AR26
VCC_AXG_NCTF80 V26
VCC_AXG_NCTF81 V28
VCC_AXG_NCTF82 V29
VCC_AXG_NCTF83 Y31
VCC GFX NCTF
=PP1V8_S3M_MEM_NB
3300 mA (2 ch, 667MHz)
2700 mA (2 ch, 533MHz)
1700 mA (1 ch, 667MHz)
1395 mA (1 ch, 533MHz)
5 mA (standby)
AU32 VCC_SM1
AU33 VCC_SM2
AU35 VCC_SM3
AV33 VCC_SM4
AW33 VCC_SM5
AW35 VCC_SM6
AY35 VCC_SM7
BA32 VCC_SM8
BA33 VCC_SM9
BA35 VCC_SM10
BB33 VCC_SM11
BC32 VCC_SM12
BC33 VCC_SM13
BC35 VCC_SM14
BD32 VCC_SM15
BD35 VCC_SM16
BE32 VCC_SM17
BE33 VCC_SM18
BE35 VCC_SM19
BF33 VCC_SM20
BF34 VCC_SM21
BG32 VCC_SM22
BG33 VCC_SM23
BG35 VCC_SM24
BH32 VCC_SM25
BH34 VCC_SM26
BH35 VCC_SM27
BJ32 VCC_SM28
BJ33 VCC_SM29
BJ34 VCC_SM30
BK32 VCC_SM31
BK33 VCC_SM32
BK34 VCC_SM33
BK35 VCC_SM34
BL33 VCC_SM35
AU30 VCC_SM36
VCC SM
=PPVCORE_S0_NB_GFX
7700 mA (Int Graphics)
R20 VCC_AXG1
T14 VCC_AXG2
W13 VCC_AXG3
W14 VCC_AXG4
Y12 VCC_AXG5
AA20 VCC_AXG6
AA23 VCC_AXG7
AA26 VCC_AXG8
AA28 VCC_AXG9
AB21 VCC_AXG10
AB24 VCC_AXG11
AB29 VCC_AXG12
AC20 VCC_AXG13
AC21 VCC_AXG14
AC23 VCC_AXG15
AC24 VCC_AXG16
AC26 VCC_AXG17
AC28 VCC_AXG18
AC29 VCC_AXG19
AD20 VCC_AXG20
AD23 VCC_AXG21
AD24 VCC_AXG22
AD28 VCC_AXG23
AF21 VCC_AXG24
AF26 VCC_AXG25
AA31 VCC_AXG26
AH20 VCC_AXG27
AH21 VCC_AXG28
AH23 VCC_AXG29
AH24 VCC_AXG30
AH26 VCC_AXG31
AD31 VCC_AXG32
AJ20 VCC_AXG33
AN14 VCC_AXG34
VCC GFX
VCC_SM_LF1 AW45 NB_VCCSM_LF1
VCC_SM_LF2 BC39 NB_VCCSM_LF2
VCC_SM_LF3 BE39 NB_VCCSM_LF3
VCC_SM_LF4 BD17 NB_VCCSM_LF4
VCC_SM_LF5 BD4 NB_VCCSM_LF5
VCC_SM_LF6 AW8 NB_VCCSM_LF6
VCC_SM_LF7 AT6 NB_VCCSM_LF7
VCC SM LF
C1807 0.1uF 20% 16V CERM 402
C1806 0.1uF 20% 16V CERM 402
C1805 0.22UF 20% 6.3V X5R 402
C1804 0.22UF 20% 6.3V X5R 402
C1803 0.47UF 10% 6.3V CERM-X5R 402
C1802 1uF 10% 6.3V CERM 402
C1801 1uF 10% 6.3V CERM 402
NCTF balls are Not Critical To Function
These connections can break without impacting part performance.
OMIT
U1400
CRESTLINE
FCBGA
(7 OF 10)
=PPVCORE_S0_NB
AB33 VCC_NCTF1
AB36 VCC_NCTF2
AB37 VCC_NCTF3
AC33 VCC_NCTF4
AC35 VCC_NCTF5
AC36 VCC_NCTF6
AD35 VCC_NCTF7
AD36 VCC_NCTF8
AF33 VCC_NCTF9
AF36 VCC_NCTF10
AH33 VCC_NCTF11
AH35 VCC_NCTF12
AH36 VCC_NCTF13
AH37 VCC_NCTF14
AJ33 VCC_NCTF15
AJ35 VCC_NCTF16
AK33 VCC_NCTF17
AK35 VCC_NCTF18
AK36 VCC_NCTF19
AK37 VCC_NCTF20
AD33 VCC_NCTF21
AJ36 VCC_NCTF22
AM35 VCC_NCTF23
AL33 VCC_NCTF24
AL35 VCC_NCTF25
AA33 VCC_NCTF26
AA35 VCC_NCTF27
AA36 VCC_NCTF28
AP35 VCC_NCTF29
AP36 VCC_NCTF30
AR35 VCC_NCTF31
AR36 VCC_NCTF32
Y32 VCC_NCTF33
Y33 VCC_NCTF34
Y35 VCC_NCTF35
Y36 VCC_NCTF36
Y37 VCC_NCTF37
T30 VCC_NCTF38
T34 VCC_NCTF39
T35 VCC_NCTF40
U29 VCC_NCTF41
U31 VCC_NCTF42
U32 VCC_NCTF43
U33 VCC_NCTF44
U35 VCC_NCTF45
U36 VCC_NCTF46
V32 VCC_NCTF47
V33 VCC_NCTF48
V36 VCC_NCTF49
V37 VCC_NCTF50
VCC NCTF
VSS_NCTF1 T27
VSS_NCTF2 T37
VSS_NCTF3 U24
VSS_NCTF4 U28
VSS_NCTF5 V31
VSS_NCTF6 V35
VSS_NCTF7 AA19
VSS_NCTF8 AB17
VSS_NCTF9 AB35
VSS_NCTF10 AD19
VSS_NCTF11 AD37
VSS_NCTF12 AF17
VSS_NCTF13 AF35
VSS_NCTF14 AK17
VSS_NCTF15 AM17
VSS_NCTF16 AM24
VSS_NCTF17 AP26
VSS_NCTF18 AP28
VSS_NCTF19 AR15
VSS_NCTF20 AR19
VSS_NCTF21 AR28
VSS NCTF
VSS_SCB1 A3
VSS_SCB2 B2
VSS_SCB3 C1
VSS_SCB4 BL1
VSS_SCB5 BL51
VSS_SCB6 A51
VSS SCB
=PP1V05_S0M_NB_VCCAXM
540 mA
VCC_AXM1 AT33
VCC_AXM2 AT31
VCC_AXM3 AK29
VCC_AXM4 AK24
VCC_AXM5 AK23
VCC_AXM6 AJ26
VCC_AXM7 AJ23
VCC AXM
=PP1V05_S0M_NB_VCCAXM
AL24 VCC_AXM_NCTF1
AL26 VCC_AXM_NCTF2
AL28 VCC_AXM_NCTF3
AM26 VCC_AXM_NCTF4
AM28 VCC_AXM_NCTF5
AM29 VCC_AXM_NCTF6
AM31 VCC_AXM_NCTF7
AM32 VCC_AXM_NCTF8
AM33 VCC_AXM_NCTF9
AP29 VCC_AXM_NCTF10
AP31 VCC_AXM_NCTF11
AP32 VCC_AXM_NCTF12
AP33 VCC_AXM_NCTF13
AL29 VCC_AXM_NCTF14
AL31 VCC_AXM_NCTF15
AL32 VCC_AXM_NCTF16
AR31 VCC_AXM_NCTF17
AR32 VCC_AXM_NCTF18
AR33 VCC_AXM_NCTF19
VCC AXM NCTF
NB Power 1
SYNC_MASTER=T9_NOME
SYNC_DATE=03/16/2007
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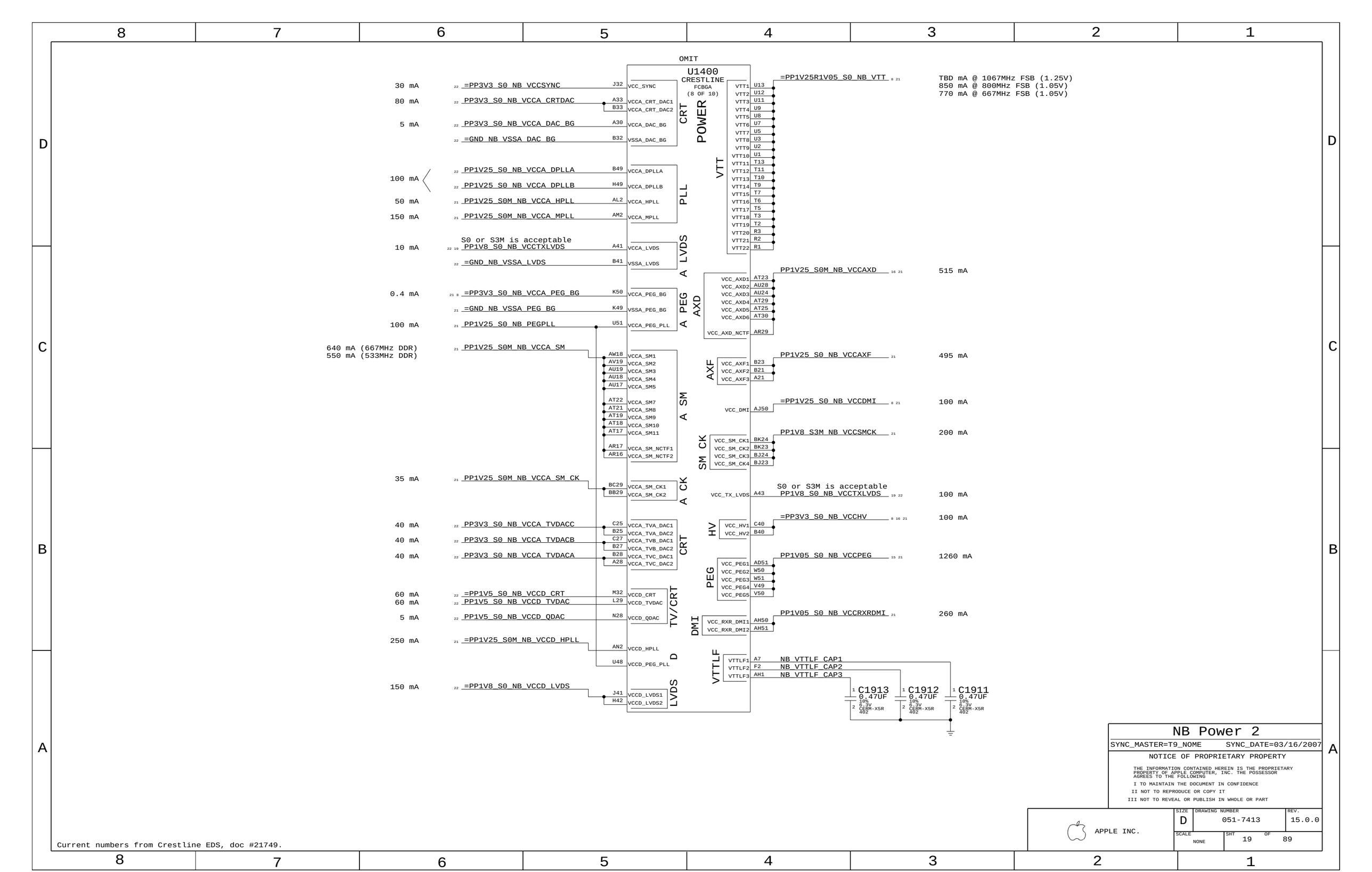
APPLE INC.
SIZE D
DRAWING NUMBER 051-7413
REV. 15.0.0
SCALE NONE
SHT 18 OF 89
Current numbers from Crestline EDS, doc #21749.



Current numbers from Crestline EDS, doc #21749.

NB Power 2

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	19	89

OMIT

U1400
CRESTLINE
FCBGA
(9 OF 10)
VSS

A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AY10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B38
AD26	VSS21	VSS120	B43
AD29	VSS22	VSS121	B46
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BB12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BG19
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BJ11
AN43	VSS72	VSS171	BJ13
AN5	VSS73	VSS172	BJ38
AN7	VSS74	VSS173	BJ4
AP4	VSS75	VSS174	BJ42
AP48	VSS76	VSS175	BJ46
AP50	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C36
AW16	VSS99	VSS198	C41

OMIT

U1400
CRESTLINE
FCBGA
(10 OF 10)
VSS

C46	VSS199	VSS287	W11
C50	VSS200	VSS288	W39
C7	VSS201	VSS289	W43
D13	VSS202	VSS290	W47
D24	VSS203	VSS291	W5
D3	VSS204	VSS292	W7
D32	VSS205	VSS293	Y13
D39	VSS206	VSS294	Y2
D45	VSS207	VSS295	Y41
D49	VSS208	VSS296	Y45
E10	VSS209	VSS297	Y49
E16	VSS210	VSS298	Y5
E24	VSS211	VSS299	Y50
E28	VSS212	VSS300	Y11
E32	VSS213	VSS301	P29
E47	VSS214		
F19	VSS215		
F36	VSS216	TDE_SENSE VSS302	T29
F4	VSS217		
F40	VSS218		
F50	VSS219	TDE_FORCE VSS303	T31
G1	VSS220		
G13	VSS221		
G16	VSS222	TDB_FORCE VSS304	T33
G19	VSS223		
G24	VSS224		
G28	VSS225	TDB_SENSE VSS305	R28
G29	VSS226		
G33	VSS227		
G42	VSS228		
G45	VSS229	VSS306	AA32
G48	VSS230	VSS307	AB32
G8	VSS231	VSS308	AD32
H24	VSS232	VSS309	AF28
H28	VSS233	VSS310	AF29
H4	VSS234	VSS311	AT27
H45	VSS235	VSS312	AV25
J11	VSS236	VSS313	H50
J16	VSS237		
J2	VSS238		
J24	VSS239		
J28	VSS240		
J33	VSS241		
J35	VSS242		
J39	VSS243		
K12	VSS245		
K47	VSS246		
K8	VSS247		
L1	VSS248		
L17	VSS249		
L20	VSS250		
L24	VSS251		
L28	VSS252		
L3	VSS253		
L33	VSS254		
L49	VSS255		
M28	VSS256		
M42	VSS257		
M46	VSS258		
M49	VSS259		
M5	VSS260		
M50	VSS261		
M9	VSS262		
N11	VSS263		
N14	VSS264		
N17	VSS265		
N29	VSS266		
N32	VSS267		
N36	VSS268		
N39	VSS269		
N44	VSS270		
N49	VSS271		
N7	VSS272		
P19	VSS273		
P2	VSS274		
P23	VSS275		
P3	VSS276		
P50	VSS277		
R49	VSS278		
T39	VSS279		
T43	VSS280		
T47	VSS281		
U41	VSS282		
U45	VSS283		
U50	VSS284		
V2	VSS285		
V3	VSS286		

Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

TDE_SENSE T29 =NB_TDE_SENSE 51

NOTE: TDE = _P

TDE_FORCE T31 =NB_TDE_FORCE 51

TDB_FORCE T33 =NB_TDB_FORCE 51

NOTE: TDB = _N

TDB_SENSE R28 =NB_TDB_SENSE 51

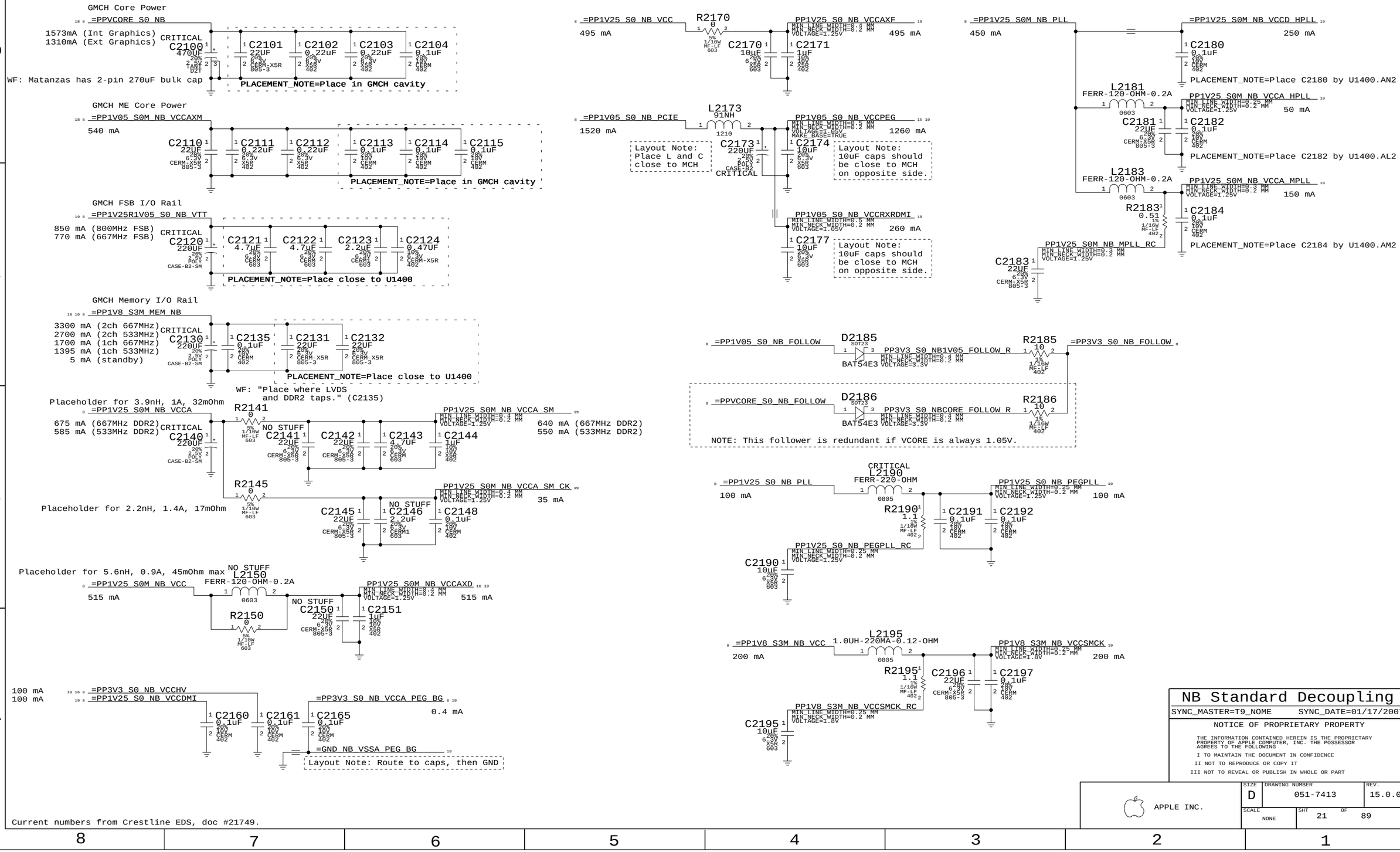
NB Grounds

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	20	89


GMCH Core Power
=PPVCORE_S0_NB
1573mA (Int Graphics)
1310mA (Ext Graphics)
CRITICAL
C2100 470UF 20% 2.5V POLY CASE-B2-SM
C2101 22UF 20% 6.3V CERM-X5R 805-3
C2102 0.22uF 20% 6.3V CERM 402
C2103 0.22uF 20% 6.3V CERM 402
C2104 0.1uF 20% 10V CERM 402
WF: Matanzas has 2-pin 270uF bulk cap
PLACEMENT_NOTE=Place in GMCH cavity
GMCH ME Core Power
=PP1V05_S0M_NB_VCCAXM
540 mA
C2110 22UF 20% 6.3V CERM-X5R 805-3
C2111 0.22uF 20% 6.3V CERM 402
C2112 0.22uF 20% 6.3V CERM 402
C2113 0.1uF 20% 10V CERM 402
C2114 0.1uF 20% 10V CERM 402
C2115 0.1uF 20% 10V CERM 402
PLACEMENT_NOTE=Place in GMCH cavity
GMCH FSB I/O Rail
=PP1V25R1V05_S0_NB_VTT
850 mA (800MHz FSB)
770 mA (667MHz FSB)
CRITICAL
C2120 220UF 20% 2.5V POLY CASE-B2-SM
C2121 4.7uF 20% 6.3V CERM 603
C2122 4.7uF 20% 6.3V CERM 603
C2123 2.2uF 20% 6.3V CERM 603
C2124 0.47UF 10% 6.3V CERM-X5R 402
PLACEMENT_NOTE=Place close to U1400
GMCH Memory I/O Rail
=PP1V8_S3M_MEM_NB
3300 mA (2ch 667MHz)
2700 mA (2ch 533MHz)
1700 mA (1ch 667MHz)
1395 mA (1ch 533MHz)
5 mA (standby)
CRITICAL
C2130 220UF 20% 2.5V POLY CASE-B2-SM
C2135 0.1uF 20% 10V CERM 402
C2131 22UF 20% 6.3V CERM-X5R 805-3
C2132 22UF 20% 6.3V CERM-X5R 805-3
PLACEMENT_NOTE=Place close to U1400
WF: "Place where LVDS and DDR2 taps." (C2135)
Placeholder for 3.9nH, 1A, 32mOhm
=PP1V25_S0M_NB_VCCA
675 mA (667MHz DDR2)
585 mA (533MHz DDR2)
CRITICAL
C2140 220UF 20% 2.5V POLY CASE-B2-SM
R2141 0 5% 1/10W MF-LF 603
NO STUFF
C2141 22UF 20% 6.3V CERM-X5R 805-3
C2142 22UF 20% 6.3V CERM-X5R 805-3
C2143 4.7UF 20% 6.3V CERM 603
C2144 1UF 10% 10V X5R 402
PP1V25_S0M_NB_VCCA_SM
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
640 mA (667MHz DDR2)
550 mA (533MHz DDR2)
R2145 0 5% 1/10W MF-LF 603
Placeholder for 2.2nH, 1.4A, 17mOhm
C2145 22UF 20% 6.3V CERM-X5R 805-3
NO STUFF
C2146 2.2uF 20% 6.3V CERM1 603
C2148 0.1uF 20% 10V CERM 402
PP1V25_S0M_NB_VCCA_SM_CK
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
35 mA
Placeholder for 5.6nH, 0.9A, 45mOhm max
=PP1V25_S0M_NB_VCC
515 mA
NO STUFF
L2150 FERR-120-OHM-0.2A 0603
R2150 0 5% 1/10W MF-LF 603
NO STUFF
C2150 22UF 20% 6.3V CERM-X5R 805-3
C2151 1uF 10% 10V X5R 402
PP1V25_S0M_NB_VCCAXD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
515 mA
100 mA
100 mA
=PP3V3_S0_NB_VCCHV
=PP1V25_S0_NB_VCCDMI
C2160 0.1uF 20% 10V CERM 402
C2161 0.1uF 20% 10V CERM 402
=PP3V3_S0_NB_VCCA_PEG_BG
C2165 0.1uF 20% 10V CERM 402
0.4 mA
=GND_NB_VSSA_PEG_BG
Layout Note: Route to caps, then GND
=PP1V25_S0_NB_VCC
495 mA
R2170 0 5% 1/10W MF-LF 603
C2170 10uF 20% 6.3V X5R 603
C2171 1uF 10% 10V X5R 402
PP1V25_S0_NB_VCCAXF
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
495 mA
=PP1V05_S0_NB_PCIE
1520 mA
L2173 91NH 1210
C2173 220UF 20% 2.5V POLY CASE-B2 CRITICAL
Layout Note: Place L and C close to MCH
C2174 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.
PP1V05_S0_NB_VCCPEG
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
1260 mA
PP1V05_S0_NB_VCCRXRDMI
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
260 mA
C2177 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.
=PP1V25_S0M_NB_PLL
450 mA
=PP1V25_S0M_NB_VCCD_HPLL
250 mA
C2180 0.1uF 20% 10V CERM 402
PLACEMENT_NOTE=Place C2180 by U1400.AN2
L2181 FERR-120-OHM-0.2A 0603
PP1V25_S0M_NB_VCCA_HPLL
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
50 mA
C2181 22UF 20% 6.3V CERM-X5R 805-3
C2182 0.1uF 20% 10V CERM 402
PLACEMENT_NOTE=Place C2182 by U1400.AL2
L2183 FERR-120-OHM-0.2A 0603
PP1V25_S0M_NB_VCCA_MPLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
150 mA
R2183 0.51 1% 1/10W MF-LF 402
C2184 0.1uF 20% 10V CERM 402
PLACEMENT_NOTE=Place C2184 by U1400.AM2
PP1V25_S0M_NB_MPLL_RC
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
C2183 22UF 20% 6.3V CERM-X5R 805-3
=PP1V05_S0_NB_FOLLOW
D2185 SOT23 BAT54E
PP3V3_S0_NB1V05_FOLLOW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
R2185 10 1% 1/16W MF-LF 402
=PP3V3_S0_NB_FOLLOW
=PPVCORE_S0_NB_FOLLOW
D2186 SOT23 BAT54E
PP3V3_S0_NBCORE_FOLLOW_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
R2186 10 1% 1/16W MF-LF 402
NOTE: This follower is redundant if VCORE is always 1.05V.
=PP1V25_S0_NB_PLL
100 mA
CRITICAL
L2190 FERR-220-OHM 0805
R2190 1.1 1% 1/16W MF-LF 402
C2191 0.1uF 20% 10V CERM 402
C2192 0.1uF 20% 10V CERM 402
PP1V25_S0_NB_PEGPLL
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
100 mA
PP1V25_S0_NB_PEGPLL_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
C2190 10uF 20% 6.3V X5R 603
=PP1V8_S3M_NB_VCC
200 mA
L2195 1.0UH-220MA-0.12-OHM 0805
R2195 1.1 1% 1/16W MF-LF 402
C2196 22UF 20% 6.3V CERM-X5R 805-3
C2197 0.1uF 20% 10V CERM 402
PP1V8_S3M_NB_VCCSMCK
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
200 mA
PP1V8_S3M_NB_VCCSMCK_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
C2195 10uF 20% 6.3V X5R 603
NB Standard Decoupling
SYNC_MASTER=T9_NOME
SYNC_DATE=01/17/2007
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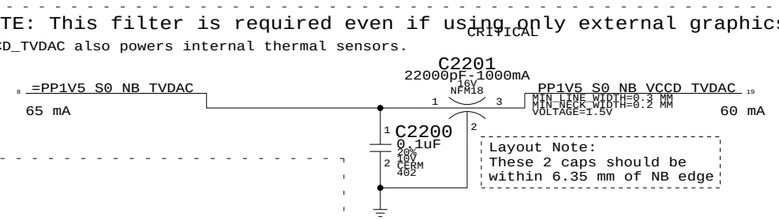
SIZE D
DRAWING NUMBER 051-7413
REV. 15.0.0
SCALE NONE
SHT 21 OF 89
Current numbers from Crestline EDS, doc #21749.

Crestline LVDS Strapping

NOTE: This filter is required even if using only external graphics.
VCCD_TVDAC also powers internal thermal sensors.



15 LVDS_DDC_CLK
15 LVDS_DDC_DATA
15 13 LVDS_CTRL_CLK
15 13 LVDS_CTRL_DATA
15 =CRT_RED
15 =CRT_RED_L
15 =CRT_GREEN
15 =CRT_GREEN_L
15 =CRT_BLUE
15 =CRT_BLUE_L
15 =CRT_HSYNC_R
15 =CRT_VSYNC_R
15 =CRT_TVO_IREF
15 =TV_A_DAC
15 =TV_A_RTN
15 =TV_B_DAC
15 =TV_B_RTN
15 =TV_C_DAC
15 =TV_C_RTN
15 CRT_DDC_CLK
15 CRT_DDC_DATA
16 SDVO_CTRLCLK
16 SDVO_CTRLDATA
15 TV_DCONSEL<0>
15 TV_DCONSEL<1>
16 =NB_CLK96M_DOT_N
16 =NB_CLK96M_DOT_P
16 =NB_CLK100M_DPLLSS_P
16 =NB_CLK100M_DPLLSS_N

=GND_NB_VSSA_LVDS 19
PP1V8_S0_NB_VCCTXLVDS 19
PP1V25_S0_NB_VCCA_DPLLB 19
PP1V25_S0_NB_VCCA_DPLLA 19
=PP1V8_S0_NB_VCCD_LVDS 19
=PP1V5_S0_NB_VCCD_CRT 19
PP3V3_S0_NB_VCCA_CRTDAC 19
=PP3V3_S0_NB_VCCSYNC 19
PP1V5_S0_NB_VCCD_QDAC 19
PP3V3_S0_NB_VCCA_DAC_BG 19
=GND_NB_VSSA_DAC_BG 19
PP3V3_S0_NB_VCCA_TVDACA 19
PP3V3_S0_NB_VCCA_TVDACB 19
PP3V3_S0_NB_VCCA_TVDACC 19

15 LVDS_BKLT_CTL — NC_LVDS_BKLT_CTL
15 LVDS_BKLT_EN — NC_LVDS_BKLT_EN
15 LVDS_VDD_EN — NC_LVDS_VDD_EN
81 15 LVDS_IBG — NC_LVDS_IBG
15 TP_LVDS_VBG — NC_LVDS_VBG
81 15 LVDS_A_CLK_N — NC_LVDS_A_CLKN
81 15 LVDS_A_CLK_P — NC_LVDS_A_CLKP
81 15 LVDS_B_CLK_N — NC_LVDS_B_CLKN
81 15 LVDS_B_CLK_P — NC_LVDS_B_CLKP
81 15 LVDS_A_DATA_N<0> — NC_LVDS_A_DATAN<0>
81 15 LVDS_A_DATA_N<1> — NC_LVDS_A_DATAN<1>
81 15 LVDS_A_DATA_N<2> — NC_LVDS_A_DATAN<2>
81 15 LVDS_A_DATA_P<0> — NC_LVDS_A_DATAP<0>
81 15 LVDS_A_DATA_P<1> — NC_LVDS_A_DATAP<1>
81 15 LVDS_A_DATA_P<2> — NC_LVDS_A_DATAP<2>
81 15 LVDS_B_DATA_N<0> — NC_LVDS_B_DATAN<0>
81 15 LVDS_B_DATA_N<1> — NC_LVDS_B_DATAN<1>
81 15 LVDS_B_DATA_N<2> — NC_LVDS_B_DATAN<2>
81 15 LVDS_B_DATA_P<0> — NC_LVDS_B_DATAP<0>
81 15 LVDS_B_DATA_P<1> — NC_LVDS_B_DATAP<1>
81 15 LVDS_B_DATA_P<2> — NC_LVDS_B_DATAP<2>
15 TP_LVDS_VREFH — NC_LVDS_VREFH
15 TP_LVDS_VREFL — NC_LVDS_VREFL
16 GFX_VID<1> — TP_GFX_VID<1>
16 GFX_VID<2> — TP_GFX_VID<2>
16 GFX_VID<3> — TP_GFX_VID<3>
16 GFX_VID<4> — TP_GFX_VID<4>
16 =GFX_VR_EN — TP_GFX_VR_EN

MAKE_BASE=TRUE NO_TEST=TRUE

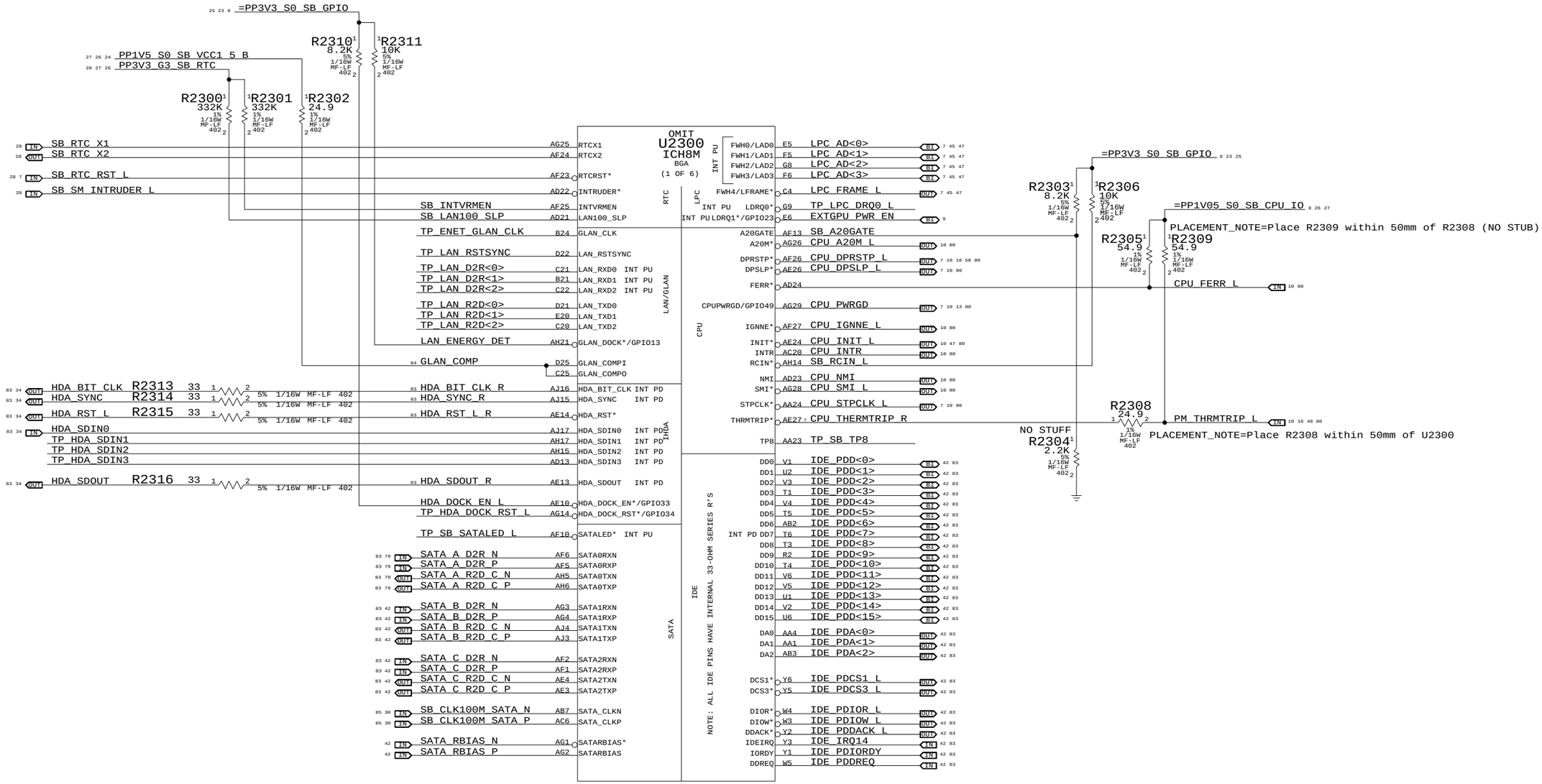
Current numbers from Crestline EDS Addendum, doc #20127.

NB Graphics Decoupling

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 22 OF 89	



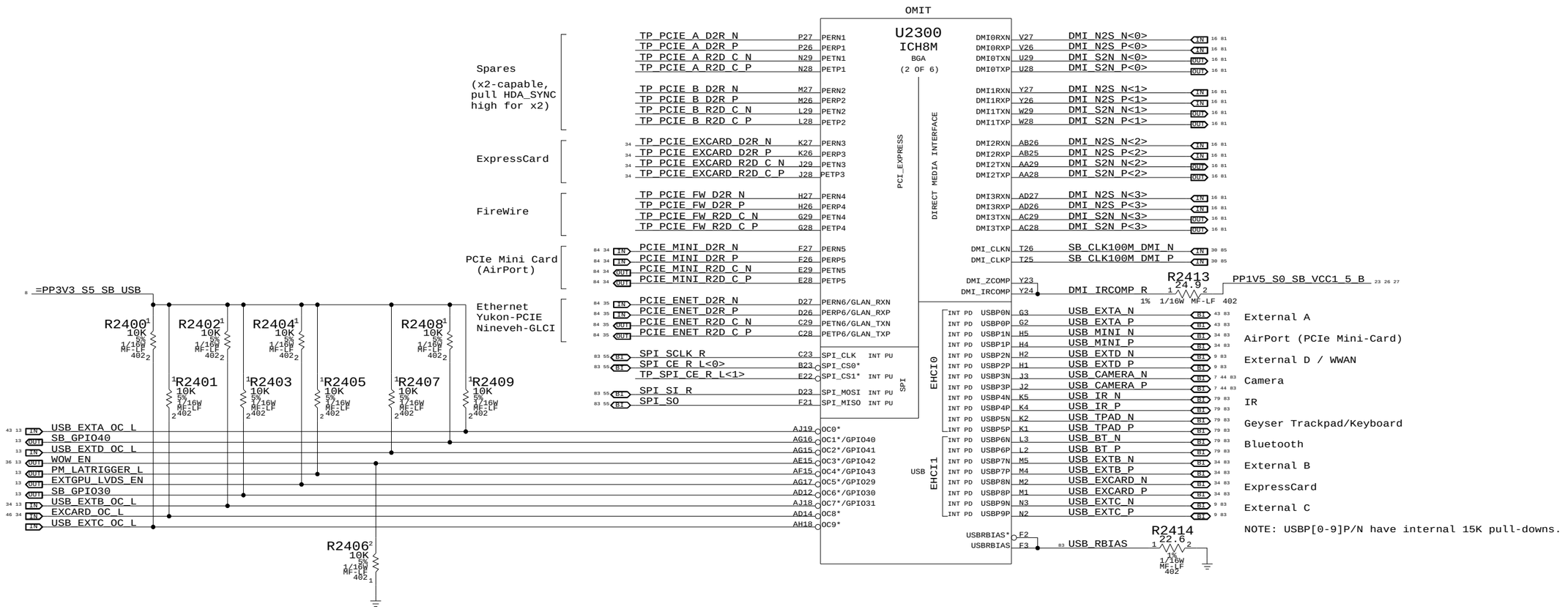
	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 23 OF 89	


OMIT
U2300
ICH8M
BGA
(2 OF 6)
PCI_EXPRESS
DIRECT MEDIA INTERFACE
SPI
EHCI0
EHCI1
USB
Spares
(x2-capable, pull HDA_SYNC high for x2)
ExpressCard
FireWire
PCIe Mini Card (AirPort)
Ethernet Yukon-PCIE Nineveh-GLCI
TP_PCIE_A_D2R_N
TP_PCIE_A_D2R_P
TP_PCIE_A_R2D_C_N
TP_PCIE_A_R2D_C_P
TP_PCIE_B_D2R_N
TP_PCIE_B_D2R_P
TP_PCIE_B_R2D_C_N
TP_PCIE_B_R2D_C_P
TP_PCIE_EXCARD_D2R_N
TP_PCIE_EXCARD_D2R_P
TP_PCIE_EXCARD_R2D_C_N
TP_PCIE_EXCARD_R2D_C_P
TP_PCIE_FW_D2R_N
TP_PCIE_FW_D2R_P
TP_PCIE_FW_R2D_C_N
TP_PCIE_FW_R2D_C_P
PCIE_MINI_D2R_N
PCIE_MINI_D2R_P
PCIE_MINI_R2D_C_N
PCIE_MINI_R2D_C_P
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
SPI_SCLK_R
SPI_CE_R_L<0>
TP_SPI_CE_R_L<1>
SPI_SI_R
SPI_SO
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_N2S_N<0>
DMI_N2S_P<0>
DMI_S2N_N<0>
DMI_S2N_P<0>
DMI_N2S_N<1>
DMI_N2S_P<1>
DMI_S2N_N<1>
DMI_S2N_P<1>
DMI_N2S_N<2>
DMI_N2S_P<2>
DMI_S2N_N<2>
DMI_S2N_P<2>
DMI_N2S_N<3>
DMI_N2S_P<3>
DMI_S2N_N<3>
DMI_S2N_P<3>
DMI_CLKN
DMI_CLKP
SB_CLK100M_DMI_N
SB_CLK100M_DMI_P
DMI_ZCOMP
DMI_IRCOMP
DMI_IRCOMP_R
R2413
24.9
1% 1/16W MF-LF 402
PP1V5_S0_SB_VCC1_5_B
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USB_EXTA_N
USB_EXTA_P
USB_MINI_N
USB_MINI_P
USB_EXTD_N
USB_EXTD_P
USB_CAMERA_N
USB_CAMERA_P
USB_IR_N
USB_IR_P
USB_TPAD_N
USB_TPAD_P
USB_BT_N
USB_BT_P
USB_EXTB_N
USB_EXTB_P
USB_EXCARD_N
USB_EXCARD_P
USB_EXTC_N
USB_EXTC_P
USBRBIAS*
USBRBIAS
USB_RBIAS
R2414
22.6
1%
1/16W
MF-LF
402
External A
AirPort (PCIe Mini-Card)
External D / WWAN
Camera
IR
Geyser Trackpad/Keyboard
Bluetooth
External B
ExpressCard
External C
NOTE: USBP[0-9]P/N have internal 15K pull-downs.
=PP3V3_S5_SB_USB
R2400 10K
R2402 10K
R2404 10K
R2408 10K
R2401 10K
R2403 10K
R2405 10K
R2407 10K
R2409 10K
5% 1/10W MF-LF 402
USB_EXTA_OC_L
SB_GPIO40
USB_EXTD_OC_L
WOW_EN
PM_LATRIGGER_L
EXTGPU_LVDS_EN
SB_GPIO30
USB_EXTB_OC_L
EXCARD_OC_L
USB_EXTC_OC_L
OC0*
OC1*/GPIO40
OC2*/GPIO41
OC3*/GPIO42
OC4*/GPIO43
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
OC8*
OC9*
R2406 10K
NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1
If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.
INTERRUPT I/F
PCI
PCI_AD<0>
PCI_AD<1>
PCI_AD<2>
PCI_AD<3>
PCI_AD<4>
PCI_AD<5>
PCI_AD<6>
PCI_AD<7>
PCI_AD<8>
PCI_AD<9>
PCI_AD<10>
PCI_AD<11>
PCI_AD<12>
PCI_AD<13>
PCI_AD<14>
PCI_AD<15>
PCI_AD<16>
PCI_AD<17>
PCI_AD<18>
PCI_AD<19>
PCI_AD<20>
PCI_AD<21>
PCI_AD<22>
PCI_AD<23>
PCI_AD<24>
PCI_AD<25>
PCI_AD<26>
PCI_AD<27>
PCI_AD<28>
PCI_AD<29>
PCI_AD<30>
PCI_AD<31>
INT_PIRQA_L
INT_PIRQB_L
INT_PIRQC_L
INT_PIRQD_L
FireWire INT*
PCI_FW_REQ_L
PCI_REQ1_L
TP_SB_GPIO51
PCI_REQ2_L
TP_SB_GPIO53
ODD_RST_5VTOL_L
TP_SB_GPIO55
PCI_C_BE_L<0>
PCI_C_BE_L<1>
PCI_C_BE_L<2>
PCI_C_BE_L<3>
PCI_IRDY_L
PCI_PAR
PCI_RST_L
PCI_DEVSEL_L
PCI_PERR_L
PCI_LOCK_L
PCI_SERR_L
PCI_STOP_L
PCI_TRDY_L
PCI_FRAME_L
PLT_RST_L
PCI_CLK33M_SB
TP_PCI_PME_L
INT_PIRQE_L
INT_PIRQF_L
DVI_HOTPLUG_DET
ODD_PWR_EN_L
PCI_FW_GNT_L
MAKE_BASE=TRUE
BOOT_LPC_SPI_L
R2415
1K
5% 1/16W MF-LF 402
R2415 pull-down on GNT0# selects SPI ROM by default.
SB BOOT BIOS SELECT
I/F | GNT0#
LPC | 1
SPI | 0
NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
=PP3V3_S0_SB_PCI
R2423 8.2K
R2424 8.2K
R2425 8.2K
R2426 8.2K
R2427 8.2K
R2428 8.2K
R2430 8.2K
R2429 8.2K
R2432 8.2K
R2431 8.2K
R2433 8.2K
R2437 8.2K
R2436 8.2K
R2438 8.2K
R2439 8.2K
R2440 100K
R2441 8.2K
R2442 8.2K
SB PCI, PCIe, DMI, USB
SYNC_MASTER=T9_NOME
SYNC_DATE=03/16/2007
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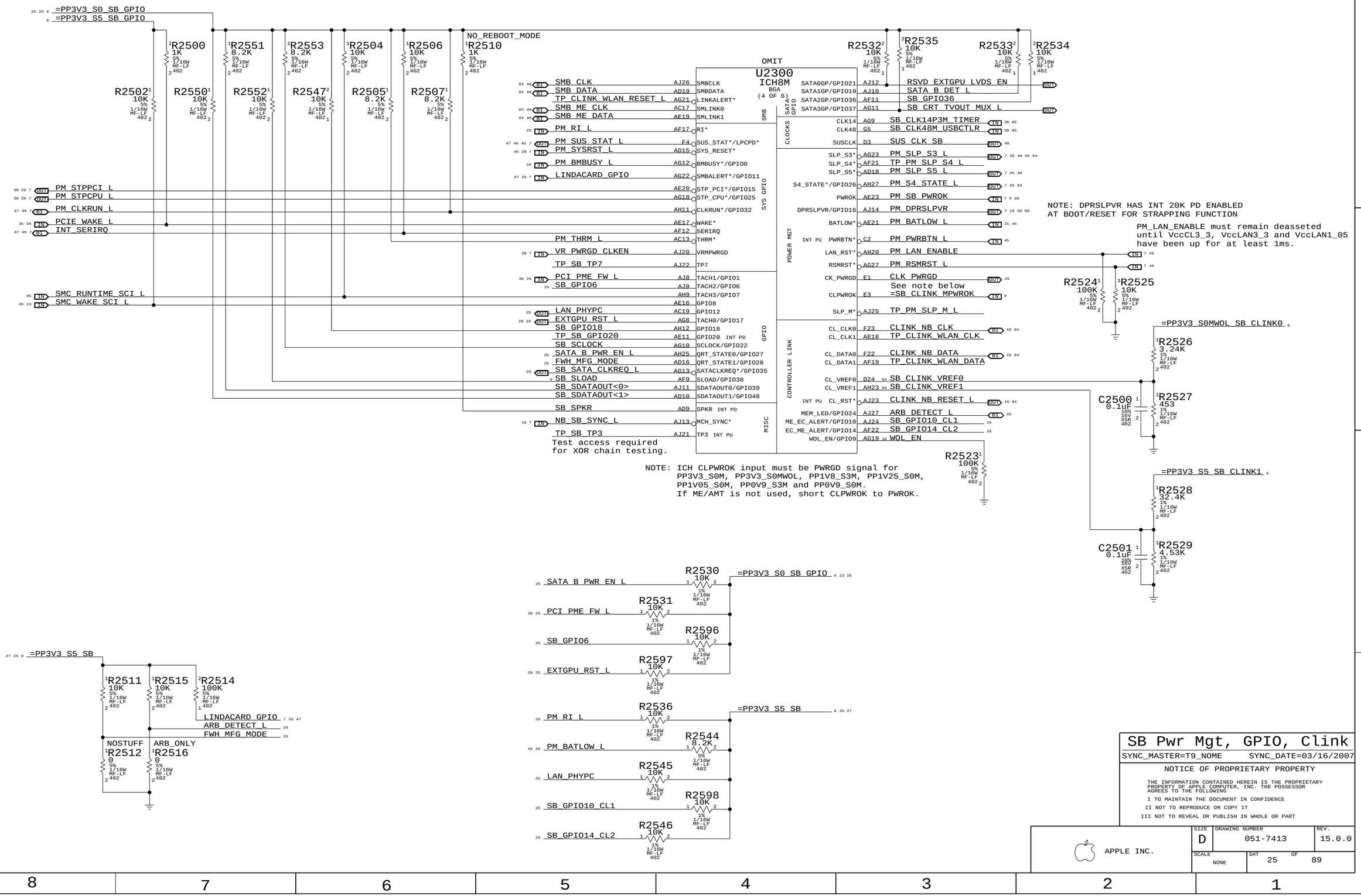
REV. 15.0.0
SCALE NONE
SHT 24 OF 89



SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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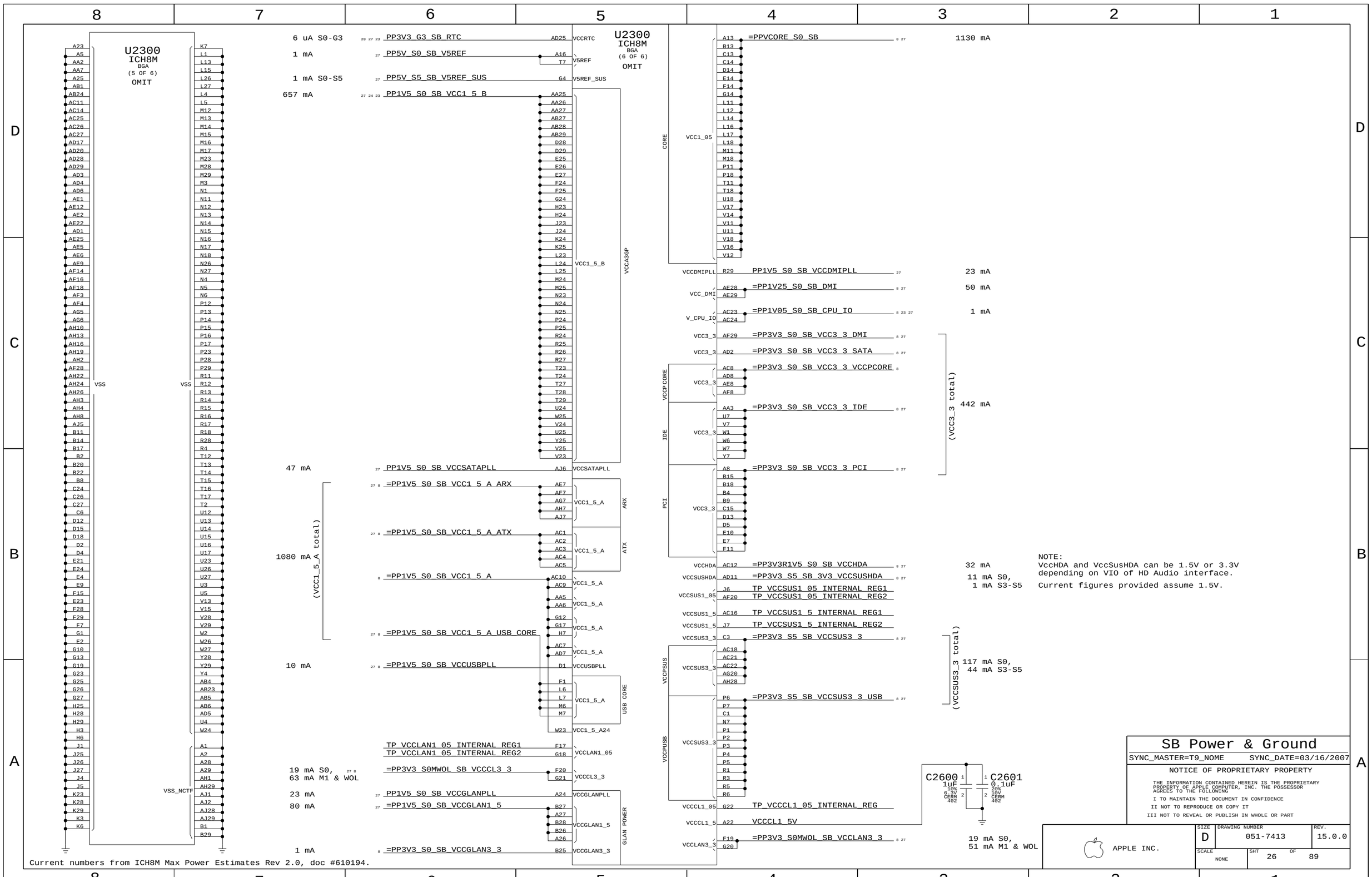
SCALE: NONE	SHT 25 OF 89	


U2300
ICH8M
BGA
(5 OF 6)
OMIT
VSS
VSS_NCTF
U2300
ICH8M
BGA
(6 OF 6)
OMIT
6 uA S0-G3
PP3V3_G3_SB_RTC
VCCRTC
1 mA
PP5V_S0_SB_V5REF
V5REF
V5REF_SUS
1 mA S0-S5
PP5V_S5_SB_V5REF_SUS
657 mA
PP1V5_S0_SB_VCC1_5_B
VCC1_5_B
VCCA3GP
47 mA
PP1V5_S0_SB_VCCSATAPLL
VCCSATAPLL
=PP1V5_S0_SB_VCC1_5_A_ARX
=PP1V5_S0_SB_VCC1_5_A_ATX
=PP1V5_S0_SB_VCC1_5_A
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
(VCC1_5_A total)
1080 mA
VCC1_5_A
ARX
ATX
USB CORE
10 mA
=PP1V5_S0_SB_VCCUSBPLL
VCCUSBPLL
W23
VCC1_5_A24
TP_VCCLAN1_05_INTERNAL_REG1
TP_VCCLAN1_05_INTERNAL_REG2
VCCLAN1_05
19 mA S0,
63 mA M1 & WOL
=PP3V3_S0MWOL_SB_VCCCL3_3
VCCCL3_3
23 mA
PP1V5_S0_SB_VCCGLANPLL
VCCGLANPLL
80 mA
=PP1V5_S0_SB_VCCGLAN1_5
VCCGLAN1_5
GLAN POWER
1 mA
=PP3V3_S0_SB_VCCGLAN3_3
VCCGLAN3_3
=PPVCORE_S0_SB
1130 mA
CORE
VCC1_05
VCCDMIPLL
PP1V5_S0_SB_VCCDMIPLL
23 mA
VCC_DMI
=PP1V25_S0_SB_DMI
50 mA
V_CPU_IO
=PP1V05_S0_SB_CPU_IO
1 mA
VCC3_3
=PP3V3_S0_SB_VCC3_3_DMI
=PP3V3_S0_SB_VCC3_3_SATA
=PP3V3_S0_SB_VCC3_3_VCCPCORE
VCCP CORE
=PP3V3_S0_SB_VCC3_3_IDE
IDE
=PP3V3_S0_SB_VCC3_3_PCI
PCI
(VCC3_3 total)
442 mA
VCCHDA
=PP3V3R1V5_S0_SB_VCCHDA
32 mA
VCCSUSHDA
=PP3V3_S5_SB_3V3_VCCSUSHDA
11 mA S0,
1 mA S3-S5
TP_VCCSUS1_05_INTERNAL_REG1
VCCSUS1_05
TP_VCCSUS1_05_INTERNAL_REG2
VCCSUS1_5
TP_VCCSUS1_5_INTERNAL_REG1
TP_VCCSUS1_5_INTERNAL_REG2
VCCSUS3_3
=PP3V3_S5_SB_VCCSUS3_3
VCCPSUS
=PP3V3_S5_SB_VCCSUS3_3_USB
VCCPUSB
(VCCSUS3_3 total)
117 mA S0,
44 mA S3-S5
TP_VCCCL1_05_INTERNAL_REG
VCCCL1_05
VCCCL1_5
VCCCL1_5V
=PP3V3_S0MWOL_SB_VCCLAN3_3
19 mA S0,
51 mA M1 & WOL
C2600
1uF
10%
6.3V
CERM
402
C2601
0.1uF
20%
10V
CERM
402
NOTE:
VccHDA and VccSusHDA can be 1.5V or 3.3V
depending on VIO of HD Audio interface.
Current figures provided assume 1.5V.
Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.
SB Power & Ground
SYNC_MASTER=T9_NOME
SYNC_DATE=03/16/2007
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DRAWING NUMBER 051-7413
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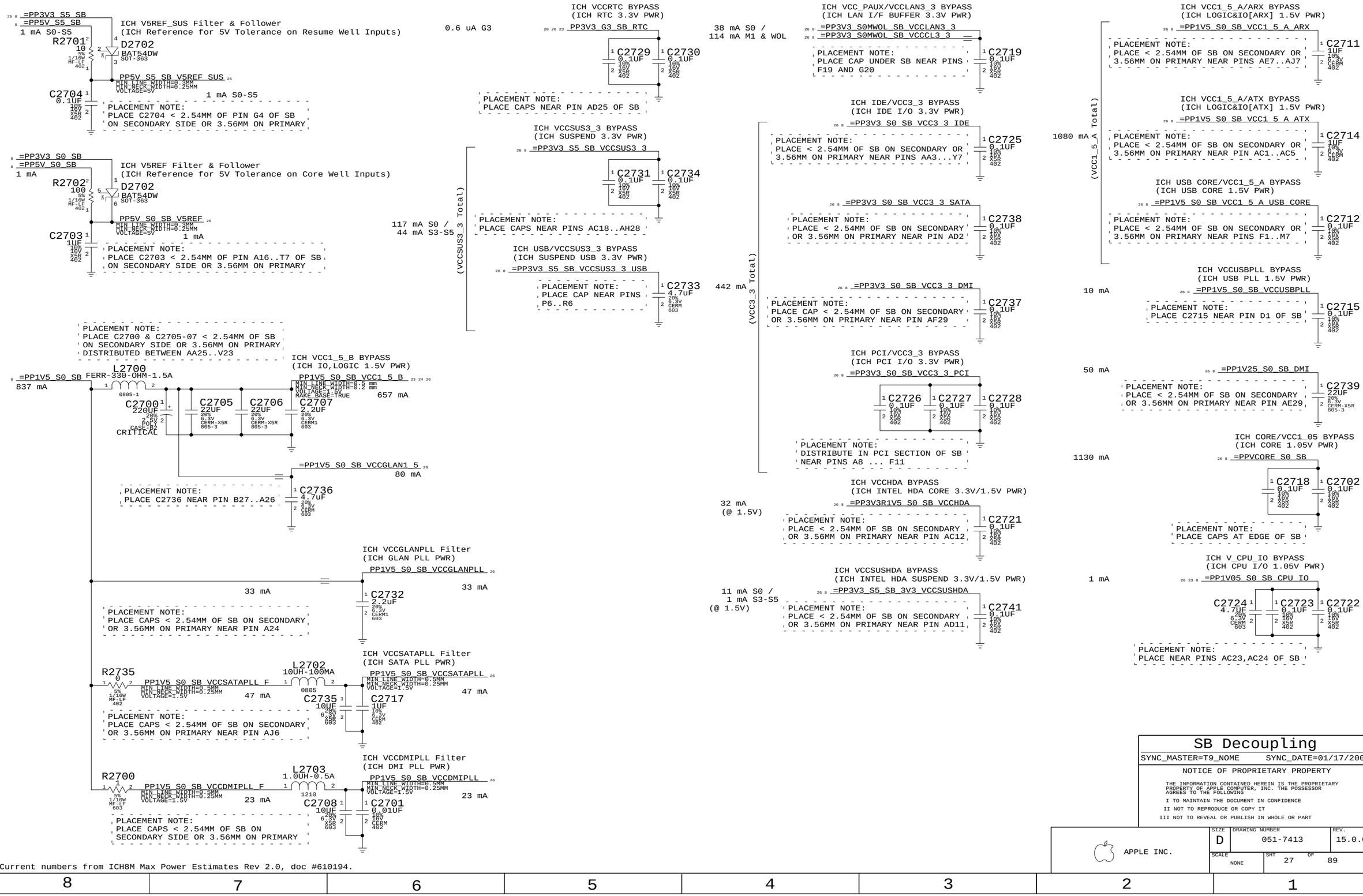
SHT 26 OF 89


=PP3V3_S5_SB
=PP5V_S5_SB
1 mA S0-S5
ICH V5REF_SUS Filter & Follower
(ICH Reference for 5V Tolerance on Resume Well Inputs)
R2701 10 5% 1/16W MF-LF 402
D2702 BAT54DW SOT-363
PP5V_S5_SB_V5REF_SUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
C2704 0.1UF 10% 16V X5R 402
1 mA S0-S5
PLACEMENT NOTE:
PLACE C2704 < 2.54MM OF PIN G4 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
=PP3V3_S0_SB
=PP5V_S0_SB
1 mA
ICH V5REF Filter & Follower
(ICH Reference for 5V Tolerance on Core Well Inputs)
R2702 100 5% 1/16W MF-LF 402
D2702 BAT54DW SOT-363
PP5V_S0_SB_V5REF
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
C2703 1UF 10% 16V X5R 402
1 mA
PLACEMENT NOTE:
PLACE C2703 < 2.54MM OF PIN A16..T7 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
PLACEMENT NOTE:
PLACE C2700 & C2705-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
DISTRIBUTED BETWEEN AA25..V23
ICH VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
=PP1V5_S0_SB
837 mA
L2700 FERR-330-OHM-1.5A 0805-1
PP1V5_S0_SB_VCC1_5_B
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
657 mA
C2700 220UF 20% 6.3V 6DV CASE-D2 CRITICAL
C2705 22UF 20% 6.3V CERM-X5R 805-3
C2706 22UF 20% 6.3V CERM-X5R 805-3
C2707 2.2UF 20% 6.3V CERM1 603
=PP1V5_S0_SB_VCCGLAN1_5
80 mA
PLACEMENT NOTE:
PLACE C2736 NEAR PIN B27..A26
C2736 4.7UF 20% 6.3V CERM 603
ICH VCCGLANPLL Filter
(ICH GLAN PLL PWR)
PP1V5_S0_SB_VCCGLANPLL
33 mA
33 mA
C2732 2.2UF 20% 6.3V CERM1 603
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN A24
ICH VCCSATAPLL Filter
(ICH SATA PLL PWR)
R2735 0 5% 1/10W MF-LF 402
L2702 10UH-100MA 0805
PP1V5_S0_SB_VCCSATAPLL_F
PP1V5_S0_SB_VCCSATAPLL
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
47 mA
47 mA
C2735 10UF 20% 6.3V X5R 603
C2717 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AJ6
ICH VCCDMIPLL Filter
(ICH DMI PLL PWR)
R2700 1 5% 1/10W MF-LF 603
L2703 1.0UH-0.5A 1210
PP1V5_S0_SB_VCCDMIPLL_F
PP1V5_S0_SB_VCCDMIPLL
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
23 mA
23 mA
C2708 10UF 20% 6.3V X5R 603
C2701 0.01UF 10% 16V CERM 402
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
0.6 uA G3
PP3V3_G3_SB_RTC
C2729 0.1UF 10% 16V X5R 402
C2730 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PIN AD25 OF SB
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
(VCCSUS3_3 Total)
117 mA S0 /
44 mA S3-S5
=PP3V3_S5_SB_VCCSUS3_3
C2731 0.1UF 10% 16V X5R 402
C2734 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PINS AC18..AH28
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3_USB
PLACEMENT NOTE:
PLACE CAP NEAR PINS
P6..R6
C2733 4.7UF 20% 6.3V CERM 603
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
38 mA S0 /
114 mA M1 & WOL
=PP3V3_S0MW0L_SB_VCCLAN3_3
=PP3V3_S0MW0L_SB_VCCCL3_3
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS
F19 AND G20
C2719 0.1UF 10% 16V X5R 402
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
(VCC3_3 Total)
442 mA
=PP3V3_S0_SB_VCC3_3_IDE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA3...Y7
C2725 0.1UF 10% 16V X5R 402
=PP3V3_S0_SB_VCC3_3_SATA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD2
C2738 0.1UF 10% 16V X5R 402
=PP3V3_S0_SB_VCC3_3_DMI
PLACEMENT NOTE:
PLACE CAP < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AF29
C2737 0.1UF 10% 16V X5R 402
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_PCI
C2726 0.1UF 10% 16V X5R 402
C2727 0.1UF 10% 16V X5R 402
C2728 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A8 ... F11
ICH VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V/1.5V PWR)
32 mA
(@ 1.5V)
=PP3V3R1V5_S0_SB_VCCHDA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AC12
C2721 0.1UF 10% 16V X5R 402
ICH VCCSUSHDA BYPASS
(ICH INTEL HDA SUSPEND 3.3V/1.5V PWR)
11 mA S0 /
1 mA S3-S5
(@ 1.5V)
=PP3V3_S5_SB_3V3_VCCSUSHDA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD11
C2741 0.1UF 10% 16V X5R 402
ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
(VCC1_5_A Total)
1080 mA
=PP1V5_S0_SB_VCC1_5_A_ARX
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AE7..AJ7
C2711 1UF 10% 6.3V CERM 402
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ATX
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AC1..AC5
C2714 1UF 10% 6.3V CERM 402
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS F1..M7
C2712 0.1UF 10% 16V X5R 402
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
10 mA
=PP1V5_S0_SB_VCCUSBPLL
PLACEMENT NOTE:
PLACE C2715 NEAR PIN D1 OF SB
C2715 0.1UF 10% 16V X5R 402
50 mA
=PP1V25_S0_SB_DMI
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AE29
C2739 22UF 20% 6.3V CERM-X5R 805-3
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
1130 mA
=PPVCORE_S0_SB
C2718 0.1UF 10% 16V X5R 402
C2702 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
1 mA
=PP1V05_S0_SB_CPU_IO
C2724 4.7UF 20% 6.3V CERM 603
C2723 0.1UF 10% 16V X5R 402
C2722 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE NEAR PINS AC23,AC24 OF SB
SB Decoupling
SYNC_MASTER=T9_NOME
SYNC_DATE=01/17/2007
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APPLE INC.
SIZE D
DRAWING NUMBER 051-7413
REV. 15.0.0
SCALE NONE
SHT 27 OF 89

RTC Power Sources

Coin-Cell Connector

CRITICAL
J2800
BM02B-ACHKS-GAN-TF-LF-SN-M
M-RT-SM
518S0487

PPVBATT_G3_RTC
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R2800 1K 5% 1/10W MF-LF 402

PPVBATT_G3_RTC_R
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

=PP3V42_G3H_SB_RTC

D2805
BAT54DW
SOT-363
NC NC NC

PP3V3_G3_SB_RTC
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R2806 20K 5% 1/10W MF-LF 402

SB_RTC_RST_L (OUT)

R2805 1M 5% 1/10W MF-LF 402

C2806 1UF 10% 6.3V CERM 402

C2805 1UF 10% 6.3V CERM 402

SB_SM_INTRUDER_L (OUT)

NOTE: R2800 and D2805 form the double-fault protection for RTC battery.

Platform Reset Connections

Unbuffered

PLT_RST_L (IN)
MAKE_BASE=TRUE

R2860 100 5% 1/16W MF-LF 402 — NB_RESET_L (OUT)

R2861 0 5% 1/16W MF-LF 402 — FW_PLT_RST_L (OUT)

R2862 100 5% 1/16W MF-LF 402 — SMC_LRESET_L (OUT)

R2863 0 5% 1/16W MF-LF 402 — DEBUG_RESET_L (OUT)

R2864 100 5% 1/16W MF-LF 402 — LIO_PLT_RST_L (OUT)

R2865 0 5% 1/16W MF-LF 402 — ENET_RESET_L (OUT)

SB RTC Crystal

SB_RTC_X1

R2810 0 5% 1/16W MF-LF 402

SB_RTC_X1_R

C2810 12PF 5% 50V CERM 402

R2811 10M 5% 1/16W MF-LF 402

CRITICAL
Y2810
32.768K
SM-2
NC NC

C2811 12PF 5% 50V CERM 402

SB_RTC_X2

System Reset "Button"

=PP3V3_S5_SB_PM

R2825 10K 5% 1/16W MF-LF 402

ITP&XDP
R2826 1K 5% 1/16W MF-LF 402

XDP_DBRESET_L (IN) — PM_SYSRST_L (OUT)

OMIT
R2820 0 5% 1/10W MF-LF 603

SILK_PART=SYS_RST
This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

VRMPWRGD Inverter

=PP3V3_S0_SB_PM

C2830 0.1UF 20% 10V CERM 402

MC74VHC1G00 SC70-5
U2830

VR_PWRGD_CLKEN_L (IN)

VR_PWRGD_CLKEN (OUT)

PWROK Circuit

=PP3V3_S0_SB_PM

C2840 0.1UF 20% 10V CERM 402

MC74VHC1G08 SC70
U2840

VR_PWRGOOD_DELAY (IN)

ALL_SYS_PWRGD (IN)

PM_SB_PWROK (OUT)

R2841 10K 5% 1/10W MF-LF 402

R2840 10K 5% 1/16W MF-LF 402

PCI Reset Connections

PCI_RST_L (IN)

R2890 100 5% 1/16W MF-LF 402 — PCI_FW_RST_L (OUT)

CPU VCore ForcePSI

CPU_PSI_L (IN) — IMVP6_PSI_L (OUT)
MAKE_BASE=TRUE

=PP3V3_S0_RSTBUF

MC74VHC1G08 SC70
U2880

EXTGPU_RST_L (IN)

GPU_RESET_R_L

R2881 0 5% 1/16W MF-LF 402

GPU_RESET_L (OUT)

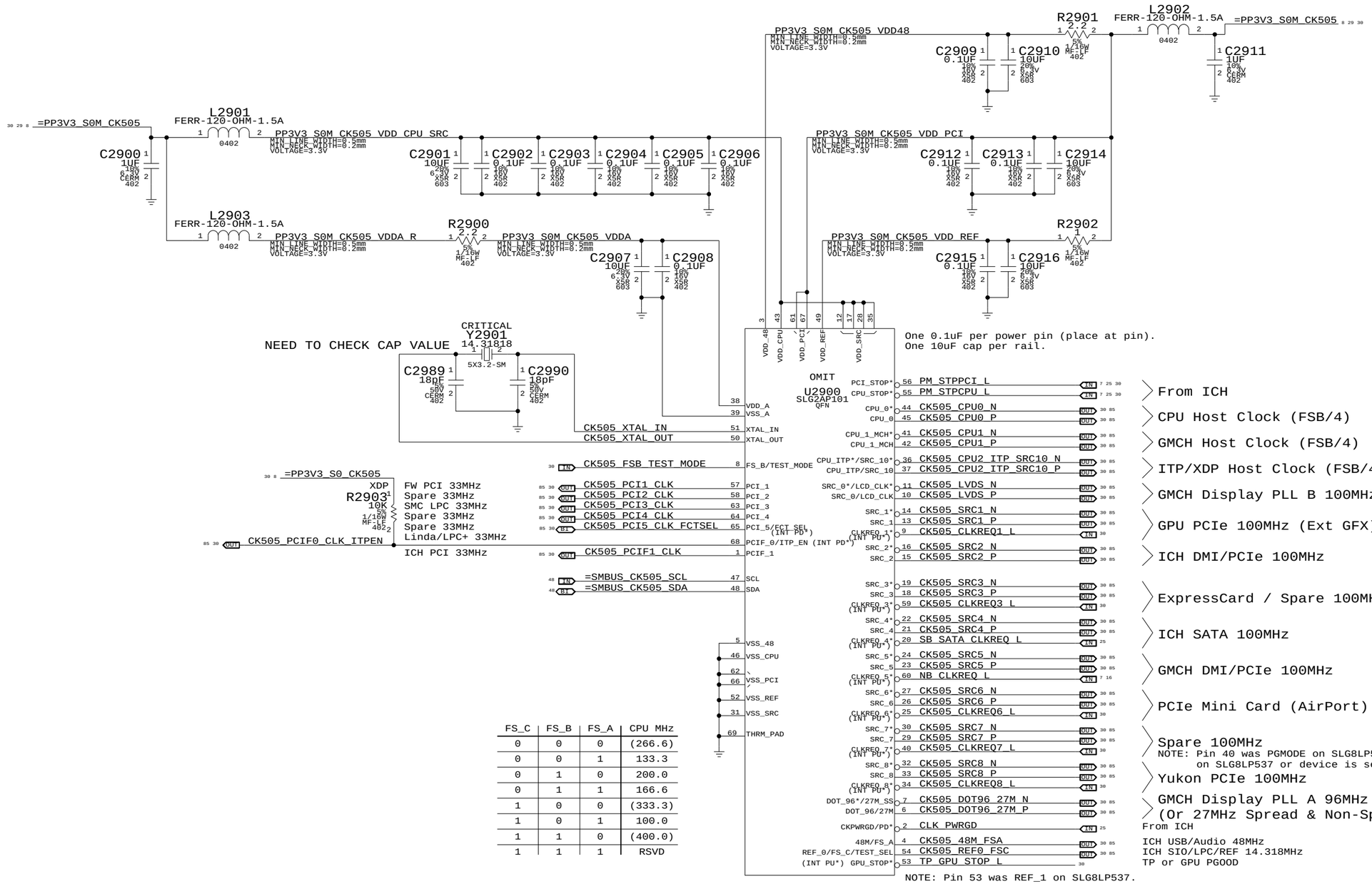
C2880 0.1UF 20% 10V CERM 402

SB Misc

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/24/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 28 OF 89	



FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

Clock (CK505)

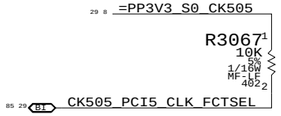
SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

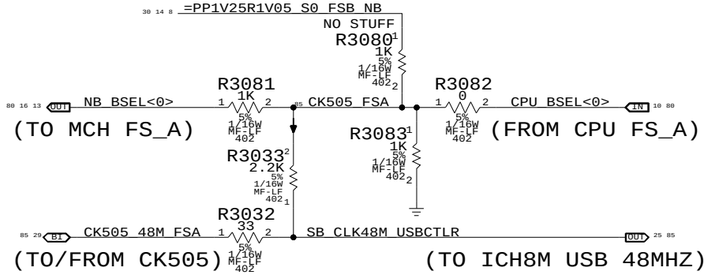
SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 29 OF 89	

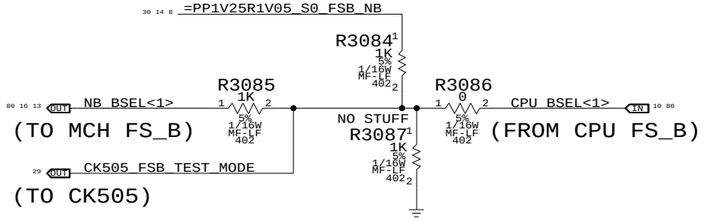
CK505 Configuration Straps

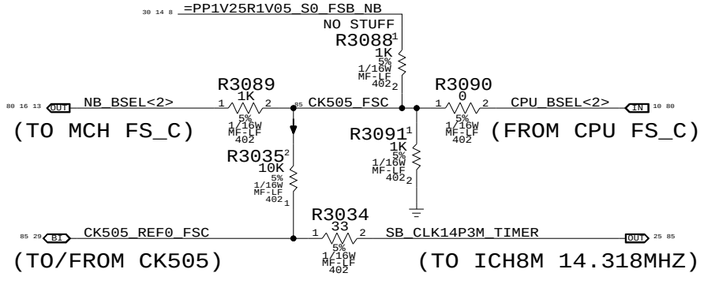
FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)







FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

CLK Termination

(Note: HOST/SRC/GFX clock termination removed. Silego SL8GLP536 or equiv. support only)

85 29 IN CK505_CPU0_P = FSB_CLK_CPU_P OUT 10 85 (MAKE_BASE=TRUE)
85 29 IN CK505_CPU0_N = FSB_CLK_CPU_N OUT 10 85 (MAKE_BASE=TRUE)
(CPU HOST 167/200MHZ)

85 29 IN CK505_CPU1_P = FSB_CLK_NB_P OUT 7 14 85 (MAKE_BASE=TRUE)
85 29 IN CK505_CPU1_N = FSB_CLK_NB_N OUT 7 14 85 (MAKE_BASE=TRUE)
(GMCH HOST 167/200MHZ)

85 29 IN CK505_CPU2_ITP_SRC10_P = XDP_CLK_P OUT 13 80 85 (MAKE_BASE=TRUE)
85 29 IN CK505_CPU2_ITP_SRC10_N = XDP_CLK_N OUT 13 80 85 (MAKE_BASE=TRUE)
(ITP HOST 167/200MHZ)

85 29 IN CK505_LVDS_P = TP_NB_CLK100M_DPLLSS_P (MAKE_BASE=TRUE)
85 29 IN CK505_LVDS_N = TP_NB_CLK100M_DPLLSS_N (MAKE_BASE=TRUE)
(Int Gfx LVDS 100MHz)

85 29 IN CK505_SRC1_P = PEG_CLK100M_GPU_P OUT 9 65 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC1_N = PEG_CLK100M_GPU_N OUT 9 65 (MAKE_BASE=TRUE)
(GPU PCIe 100MHz)

85 29 IN CK505_SRC2_P = SB_CLK100M_DMI_P OUT 24 85 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC2_N = SB_CLK100M_DMI_N OUT 24 85 (MAKE_BASE=TRUE)
(ICH8M DMI 100MHZ)

85 29 IN CK505_SRC3_P = PCIE_CLK100M_EXCARD_P OUT 34 85 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC3_N = PCIE_CLK100M_EXCARD_N OUT 34 85 (MAKE_BASE=TRUE)
(ExpressCard 100MHz)

85 29 IN CK505_SRC4_P = SB_CLK100M_SATA_P OUT 23 85 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC4_N = SB_CLK100M_SATA_N OUT 23 85 (MAKE_BASE=TRUE)
(ICH8M SATA 100MHZ)

85 29 IN CK505_SRC5_P = NB_CLK100M_PCIE_P OUT 7 16 85 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC5_N = NB_CLK100M_PCIE_N OUT 7 16 85 (MAKE_BASE=TRUE)
(GMCH PEG/DMI 100MHZ)

85 29 IN CK505_SRC6_P = PCIE_CLK100M_MINI_P OUT 34 85 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC6_N = PCIE_CLK100M_MINI_N OUT 34 85 (MAKE_BASE=TRUE)
(WIRELESS PCIe MINI 100MHZ)

85 29 IN CK505_SRC7_P = TP_PCIE_CLK100M_SRC7P (MAKE_BASE=TRUE)
85 29 IN CK505_SRC7_N = TP_PCIE_CLK100M_SRC7N (MAKE_BASE=TRUE)
(FW 100MHz)

85 29 IN CK505_SRC8_P = PCIE_CLK100M_ENET_P OUT 35 85 (MAKE_BASE=TRUE)
85 29 IN CK505_SRC8_N = PCIE_CLK100M_ENET_N OUT 35 85 (MAKE_BASE=TRUE)
(ENET 100MHZ)

85 29 IN CK505_DOT96_27M_P — CK505_CLK27M (MAKE_BASE=TRUE) — R3024 33 5% 1/16W MF-LF 402 — GPU_CLK27M OUT 71 87
(Ext GFX 27MHz)

85 29 IN CK505_DOT96_27M_N — CK505_CLK27M_SS (MAKE_BASE=TRUE) — R3025 33 5% 1/16W MF-LF 402 — GPU_CLK27M_SS OUT 71 87
(Ext GFX Spread 27MHz)

85 29 IN CK505_PCIF0_CLK_ITPEN — R3026 33 5% 1/16W MF-LF 402 — PCI_CLK33M_LPCPLUS OUT 7 47 85
(LINDA/LPC+ LPC 33MHZ)

85 29 IN CK505_PCIF1_CLK — R3027 33 5% 1/16W MF-LF 402 — PCI_CLK33M_SB OUT 24 85
(ICH8M PCI 33MHZ)

85 29 IN CK505_PCI1_CLK — R3028 33 5% 1/16W MF-LF 402 — PCI_CLK33M_FW OUT 38 85
(FIREWIRE PCI 33MHZ)

85 29 IN CK505_PCI3_CLK — R3030 33 5% 1/16W MF-LF 402 — PCI_CLK33M_SMC OUT 45 85
(SMC PCI 33MHZ)

CLKREQ Controls

29 8 =PP3V3_S0M_CK505
NO STUFF
R3046
10K
5%
1/16W
MF-LF
402
29 25 7 OUT PM_STPPCI_L
NO STUFF
R3047
10K
5%
1/16W
MF-LF
402
29 25 7 OUT PM_STPCPU_L

Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).

34 IN EXCARD_CLKREQ_L (MAKE_BASE=TRUE) = CK505_CLKREQ3_L OUT 29
34 IN MINI_CLKREQ_L (MAKE_BASE=TRUE) = CK505_CLKREQ6_L OUT 29
35 IN =ENET_CLKREQ_L = ENET_CLKREQ_L (MAKE_BASE=TRUE) = CK505_CLKREQ8_L OUT 29
TP_CK505_CLKREQ7_L (MAKE_BASE=TRUE) = CK505_CLKREQ7_L OUT 29
TP_CK505_CLKREQ1_L (MAKE_BASE=TRUE) = CK505_CLKREQ1_L OUT 29

GPU Clock Gating

64 S0PGOOD_PWROK (MAKE_BASE=TRUE) = TP_GPU_STOP_L OUT 29

Unused Clocks

85 29 IN CK505_PCI2_CLK = TP_CK505_PCI2_CLK (MAKE_BASE=TRUE)
(Reserved for TPM PCI 33MHZ)
85 29 IN CK505_PCI4_CLK = TP_CK505_PCI4_CLK (MAKE_BASE=TRUE)
(Spare 33MHZ)

Clock Termination

SYNC_MASTER=(MASTER) SYNC_DATE=08/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE NONE SHT 30 OF 89

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

"Factory" (thru-hole) slot

=PP0V9_S3M_MEM_DIMMVREFA

C3101 2.2uF 20% 6.3V CERM 603

C3100 0.1uF 20% 10V CERM 402

=PP1V8_S3M_MEM_A

CRITICAL
J3100
F-RT-TH1
DDR2-SODIMM-DUAL

	1B	VREF		201	VSS0	2B	
	3B	VSS1			DQ4	4B	MEM_A_DQ<9>
MEM_A_DQ<14>	5B	DQ0			DQ5	6B	MEM_A_DQ<15>
MEM_A_DQ<13>	7B	DQ1			VSS2	8B	
	9B	VSS4			DM0	10B	MEM_A_DM<1>
MEM_A_DQS_N<1>	11B	DQS0*			VSS5	12B	
MEM_A_DQS_P<1>	13B	DQS0			DQ6	14B	MEM_A_DQ<8>
	15B	VSS6			DQ7	16B	MEM_A_DQ<12>
MEM_A_DQ<10>	17B	DQ2			VSS7	18B	
MEM_A_DQ<11>	19B	DQ3			DQ12	20B	MEM_A_DQ<2>
	21B	VSS8			DQ13	22B	MEM_A_DQ<3>
MEM_A_DQ<7>	23B	DQ8			VSS9	24B	
MEM_A_DQ<0>	25B	DQ9			DM1	26B	MEM_A_DM<0>
	27B	VSS10			VSS11	28B	
MEM_A_DQS_N<0>	29B	DQS1*			CK0	30B	MEM_CLK_P<0>
MEM_A_DQS_P<0>	31B	DQS1			CK0*	32B	MEM_CLK_N<0>
	33B	VSS12			VSS13	34B	
MEM_A_DQ<6>	35B	DQ10			DQ14	36B	MEM_A_DQ<1>
MEM_A_DQ<4>	37B	DQ11			DQ15	38B	MEM_A_DQ<5>
	39B	VSS14			VSS15	40B	
		KEY					
	41B	VSS16			VSS17	42B	
MEM_A_DQ<17>	43B	DQ16			DQ20	44B	MEM_A_DQ<18>
MEM_A_DQ<21>	45B	DQ17			DQ21	46B	MEM_A_DQ<20>
	47B	VSS18			VSS19	48B	
MEM_A_DQS_N<2>	49B	DQS2*			NC0	50B	PM_EXTTS_L<0>
MEM_A_DQS_P<2>	51B	DQS2			DM2	52B	MEM_A_DM<2>
	53B	VSS21			VSS22	54B	
MEM_A_DQ<23>	55B	DQ18			DQ22	56B	MEM_A_DQ<22>
MEM_A_DQ<16>	57B	DQ19			DQ23	58B	MEM_A_DQ<19>
	59B	VSS23			VSS24	60B	
MEM_A_DQ<31>	61B	DQ24			DQ28	62B	MEM_A_DQ<26>
MEM_A_DQ<27>	63B	DQ25			DQ29	64B	MEM_A_DQ<24>
	65B	VSS25			VSS26	66B	
MEM_A_DM<3>	67B	DM3			DQS3*	68B	MEM_A_DQS_N<3>
NC	69B	NC1			DQS3	70B	MEM_A_DQS_P<3>
	71B	VSS27			VSS28	72B	
MEM_A_DQ<30>	73B	DQ26			DQ30	74B	MEM_A_DQ<25>
MEM_A_DQ<28>	75B	DQ27			DQ31	76B	MEM_A_DQ<29>
	77B	VSS29			VSS30	78B	
MEM_CKE<0>	79B	CKE0			NC/CKE1	80B	MEM_CKE<1>
	81B	VDD0			VDD1	82B	
NC	83B	NC2			NC/A15	84B	MEM_A_A<15>
MEM_A_BS<2>	85B	BA2			NC/A14	86B	MEM_A_A<14>
	87B	VDD2			VDD3	88B	
MEM_A_A<12>	89B	A12			A11	90B	MEM_A_A<11>
MEM_A_A<9>	91B	A9			A7	92B	MEM_A_A<7>
MEM_A_A<8>	93B	A8			A6	94B	MEM_A_A<6>
	95B	VDD4			VDD5	96B	
MEM_A_A<5>	97B	A5			A4	98B	MEM_A_A<4>
MEM_A_A<3>	99B	A3			A2	100B	MEM_A_A<2>
MEM_A_A<1>	101B	A1			A0	102B	MEM_A_A<0>
	103B	VDD6			VDD7	104B	
MEM_A_A<10>	105B	A10/AP			BA1	106B	MEM_A_BS<1>
MEM_A_BS<0>	107B	BA0			RAS*	108B	MEM_A_RAS_L
MEM_A_WE_L	109B	WE*			S0*	110B	MEM_CS_L<0>
	111B	VDD8			VDD9	112B	
MEM_A_CAS_L	113B	CAS*			ODT0	114B	MEM_ODT<0>
MEM_CS_L<1>	115B	NC/S1*			NC/A13	116B	MEM_A_A<13>
	117B	VDD10			VDD11	118B	
MEM_ODT<1>	119B	NC/ODT1			NC3	120B	NC
	121B	VSS31			VSS32	122B	
MEM_A_DQ<36>	123B	DQ32			DQ36	124B	MEM_A_DQ<35>
MEM_A_DQ<38>	125B	DQ33			DQ37	126B	MEM_A_DQ<39>
	127B	VSS33			VSS34	128B	
MEM_A_DQS_N<4>	129B	DQS4*			DM4	130B	MEM_A_DM<4>
MEM_A_DQS_P<4>	131B	DQS4			VSS35	132B	
	133B	VSS36			DQ38	134B	MEM_A_DQ<33>
MEM_A_DQ<37>	135B	DQ34			DQ39	136B	MEM_A_DQ<32>
MEM_A_DQ<34>	137B	DQ35			VSS37	138B	
	139B	VSS38			DQ44	140B	MEM_A_DQ<63>
MEM_A_DQ<56>	141B	DQ40			DQ45	142B	MEM_A_DQ<62>
MEM_A_DQ<59>	143B	DQ41			VSS39	144B	
	145B	VSS40			DQS5*	146B	MEM_A_DQS_N<7>
MEM_A_DM<7>	147B	DM5			DQS5	148B	MEM_A_DQS_P<7>
	149B	VSS41			VSS42	150B	
MEM_A_DQ<58>	151B	DQ42			DQ46	152B	MEM_A_DQ<57>
MEM_A_DQ<60>	153B	DQ43			DQ47	154B	MEM_A_DQ<61>
	155B	VSS43			VSS44	156B	
MEM_A_DQ<51>	157B	DQ48			DQ52	158B	MEM_A_DQ<55>
MEM_A_DQ<54>	159B	DQ49			DQ53	160B	MEM_A_DQ<50>
	161B	VSS45			VSS46	162B	
NC	163B	NC_TEST			CK1	164B	MEM_CLK_P<1>
	165B	VSS47			CK1*	166B	MEM_CLK_N<1>
MEM_A_DQS_N<6>	167B	DQS6*			VSS48	168B	
MEM_A_DQS_P<6>	169B	DQS6			DM6	170B	MEM_A_DM<6>
	171B	VSS49			VSS50	172B	
MEM_A_DQ<48>	173B	DQ50			DQ54	174B	MEM_A_DQ<49>
MEM_A_DQ<53>	175B	DQ51			DQ55	176B	MEM_A_DQ<52>
	177B	VSS51			VSS52	178B	
MEM_A_DQ<43>	179B	DQ56			DQ60	180B	MEM_A_DQ<45>
MEM_A_DQ<42>	181B	DQ57			DQ61	182B	MEM_A_DQ<40>
	183B	VSS53			VSS54	184B	
MEM_A_DM<5>	185B	DM7			DQS7*	186B	MEM_A_DQS_N<5>
	187B	VSS55			DQS7	188B	MEM_A_DQS_P<5>
MEM_A_DQ<46>	189B	DQ58			VSS56	190B	
MEM_A_DQ<41>	191B	DQ59			DQ62	192B	MEM_A_DQ<44>
=PPSPD_S0M_MEM_A	193B	VSS57			DQ63	194B	MEM_A_DQ<47>
=I2C_SODIMMA_SDA	195B	SDA			VSS58	196B	
=I2C_SODIMMA_SCL	197B	SCL			SA0	198B	
	199B	VDDSPD			SA1	200B	ADDR=0xA0(WR)/0xA1(RD)

516-0140 202

DDR2 Bypass Caps

(For return current)

=PP1V8_S3M_MEM_A

C3108 10UF 20% 6.3V X5R 603

C3109 10UF 20% 6.3V X5R 603

C3110 1UF 10% 6.3V CERM 402

C3111 1UF 10% 6.3V CERM 402

C3112 1UF 10% 6.3V CERM 402

C3113 1UF 10% 6.3V CERM 402

C3114 1UF 10% 6.3V CERM 402

C3115 1UF 10% 6.3V CERM 402

C3116 1UF 10% 6.3V CERM 402

C3117 1UF 10% 6.3V CERM 402

C3118 1UF 10% 6.3V CERM 402

C3119 1UF 10% 6.3V CERM 402

C3120 1UF 10% 6.3V CERM 402

C3121 1UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 31 OF 89	

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

=PP0V9_S3M_MEM_DIMMVREFB

C3201 2.2uF 20% 6.3V CERM 603

C3200 0.1uF 20% 10V CERM 402

"Expansion" (surface-mount) slot

=PP1V8_S3M_MEM_B

CRITICAL
J3200
F-RT-SM-M9
DDR2-SODIMM-DUAL

	1A	VREF			2A	VSS0	
	3A	VSS1			4A	DQ4	MEM_B_DQ<9>
MEM_B_DQ<15>	5A	DQ0			6A	DQ5	MEM_B_DQ<11>
MEM_B_DQ<14>	7A	DQ1			8A	VSS2	
	9A	VSS4			10A	DM0	MEM_B_DM<1>
MEM_B_DQS_N<1>	11A	DQS0*			12A	VSS5	
MEM_B_DQS_P<1>	13A	DQS0			14A	DQ6	MEM_B_DQ<12>
	15A	VSS6			16A	DQ7	MEM_B_DQ<8>
MEM_B_DQ<10>	17A	DQ2			18A	VSS7	
MEM_B_DQ<13>	19A	DQ3			20A	DQ12	MEM_B_DQ<3>
	21A	VSS8			22A	DQ13	MEM_B_DQ<6>
MEM_B_DQ<7>	23A	DQ8			24A	VSS9	
MEM_B_DQ<2>	25A	DQ9			26A	DM1	MEM_B_DM<0>
	27A	VSS10			28A	VSS11	
MEM_B_DQS_N<0>	29A	DQS1*			30A	CK0	MEM_CLK_P<4>
MEM_B_DQS_P<0>	31A	DQS1			32A	CK0*	MEM_CLK_N<4>
	33A	VSS12			34A	VSS13	
MEM_B_DQ<1>	35A	DQ10			36A	DQ14	MEM_B_DQ<0>
MEM_B_DQ<4>	37A	DQ11			38A	DQ15	MEM_B_DQ<5>
	39A	VSS14	KEY		40A	VSS15	
	41A	VSS16			42A	VSS17	
MEM_B_DQ<21>	43A	DQ16			44A	DQ20	MEM_B_DQ<22>
MEM_B_DQ<19>	45A	DQ17			46A	DQ21	MEM_B_DQ<18>
	47A	VSS18			48A	VSS19	
MEM_B_DQS_N<2>	49A	DQS2*			50A	NC0	PM_EXTTS_L<1>
MEM_B_DQS_P<2>	51A	DQS2			52A	DM2	MEM_B_DM<2>
	53A	VSS21			54A	VSS22	
MEM_B_DQ<20>	55A	DQ18			56A	DQ22	MEM_B_DQ<17>
MEM_B_DQ<23>	57A	DQ19			58A	DQ23	MEM_B_DQ<16>
	59A	VSS23			60A	VSS24	
MEM_B_DQ<29>	61A	DQ24			62A	DQ28	MEM_B_DQ<26>
MEM_B_DQ<24>	63A	DQ25			64A	DQ29	MEM_B_DQ<28>
	65A	VSS25			66A	VSS26	
MEM_B_DM<3>	67A	DM3			68A	DQS3*	MEM_B_DQS_N<3>
NC	69A	NC1			70A	DQS3	MEM_B_DQS_P<3>
	71A	VSS27			72A	VSS28	
MEM_B_DQ<27>	73A	DQ26			74A	DQ30	MEM_B_DQ<31>
MEM_B_DQ<25>	75A	DQ27			76A	DQ31	MEM_B_DQ<30>
	77A	VSS29			78A	VSS30	
MEM_CKE<3>	79A	CKE0			80A	NC/CKE1	MEM_CKE<4>
	81A	VDD0			82A	VDD1	
NC	83A	NC2			84A	NC/A15	MEM_B_A<15>
MEM_B_BS<2>	85A	BA2			86A	NC/A14	MEM_B_A<14>
	87A	VDD2			88A	VDD3	
MEM_B_A<12>	89A	A12			90A	A11	MEM_B_A<11>
MEM_B_A<9>	91A	A9			92A	A7	MEM_B_A<7>
MEM_B_A<8>	93A	A8			94A	A6	MEM_B_A<6>
	95A	VDD4			96A	VDD5	
MEM_B_A<5>	97A	A5			98A	A4	MEM_B_A<4>
MEM_B_A<3>	99A	A3			100A	A2	MEM_B_A<2>
MEM_B_A<1>	101A	A1			102A	A0	MEM_B_A<0>
	103A	VDD6			104A	VDD7	
MEM_B_A<10>	105A	A10/AP			106A	BA1	MEM_B_BS<1>
MEM_B_BS<0>	107A	BA0			108A	RAS*	MEM_B_RAS_L
MEM_B_WE_L	109A	WE*			110A	S0*	MEM_CS_L<2>
	111A	VDD8			112A	VDD9	
MEM_B_CAS_L	113A	CAS*			114A	ODT0	MEM_ODT<2>
MEM_CS_L<3>	115A	NC/S1*			116A	NC/A13	MEM_B_A<13>
	117A	VDD10			118A	VDD11	
MEM_ODT<3>	119A	NC/ODT1			120A	NC3	NC
	121A	VSS31			122A	VSS32	
MEM_B_DQ<36>	123A	DQ32			124A	DQ36	MEM_B_DQ<32>
MEM_B_DQ<33>	125A	DQ33			126A	DQ37	MEM_B_DQ<37>
	127A	VSS33			128A	VSS34	
MEM_B_DQS_N<4>	129A	DQS4*			130A	DM4	MEM_B_DM<4>
MEM_B_DQS_P<4>	131A	DQS4			132A	VSS35	
	133A	VSS36			134A	DQ38	MEM_B_DQ<38>
MEM_B_DQ<34>	135A	DQ34			136A	DQ39	MEM_B_DQ<39>
MEM_B_DQ<35>	137A	DQ35			138A	VSS37	
	139A	VSS38			140A	DQ44	MEM_B_DQ<56>
MEM_B_DQ<57>	141A	DQ40			142A	DQ45	MEM_B_DQ<59>
MEM_B_DQ<60>	143A	DQ41			144A	VSS39	
	145A	VSS40			146A	DQS5*	MEM_B_DQS_N<7>
MEM_B_DM<7>	147A	DM5			148A	DQS5	MEM_B_DQS_P<7>
	149A	VSS41			150A	VSS42	
MEM_B_DQ<61>	151A	DQ42			152A	DQ46	MEM_B_DQ<63>
MEM_B_DQ<62>	153A	DQ43			154A	DQ47	MEM_B_DQ<58>
	155A	VSS43			156A	VSS44	
MEM_B_DQ<48>	157A	DQ48			158A	DQ52	MEM_B_DQ<54>
MEM_B_DQ<51>	159A	DQ49			160A	DQ53	MEM_B_DQ<53>
	161A	VSS45			162A	VSS46	
NC	163A	NC_TEST			164A	CK1	MEM_CLK_P<3>
	165A	VSS47			166A	CK1*	MEM_CLK_N<3>
MEM_B_DQS_N<6>	167A	DQS6*			168A	VSS48	
MEM_B_DQS_P<6>	169A	DQS6			170A	DM6	MEM_B_DM<6>
	171A	VSS49			172A	VSS50	
MEM_B_DQ<50>	173A	DQ50			174A	DQ54	MEM_B_DQ<52>
MEM_B_DQ<55>	175A	DQ51			176A	DQ55	MEM_B_DQ<49>
	177A	VSS51			178A	VSS52	
MEM_B_DQ<40>	179A	DQ56			180A	DQ60	MEM_B_DQ<46>
MEM_B_DQ<47>	181A	DQ57			182A	DQ61	MEM_B_DQ<43>
	183A	VSS53			184A	VSS54	
MEM_B_DM<5>	185A	DM7			186A	DQS7*	MEM_B_DQS_N<5>
	187A	VSS55			188A	DQS7	MEM_B_DQS_P<5>
MEM_B_DQ<42>	189A	DQ58			190A	VSS56	
MEM_B_DQ<45>	191A	DQ59			192A	DQ62	MEM_B_DQ<41>
=PPSPD_S0M_MEM_B	193A	VSS57			194A	DQ63	MEM_B_DQ<44>
=I2C_SODIMMB_SDA	195A	SDA			196A	VSS58	
=I2C_SODIMMB_SCL	197A	SCL			198A	SA0	
	199A	VDDSPD			200A	SA1	

203 201 202 204

516S0471

Resistor prevents pwr-gnd short

SODIMM_B_SA1

ADDR=0xA4(WR)/0xA5(RD)

=PPSPD_S0M_MEM_B

R3200 10K 5% 1/16W MF-LF 402

DDR2 Bypass Caps

(For return current)

=PP1V8_S3M_MEM_B

C3208 10UF 20% 6.3V X5R 603

C3209 10UF 20% 6.3V X5R 603

C3210 1UF 10% 6.3V CERM 402

C3211 0.1UF 20% 10V CERM 402

C3212 1UF 10% 6.3V CERM 402

C3213 1UF 10% 6.3V CERM 402

C3214 1UF 10% 6.3V CERM 402

C3215 1UF 10% 6.3V CERM 402

C3216 1UF 10% 6.3V CERM 402

C3217 0.1UF 20% 10V CERM 402

C3218 0.1UF 20% 10V CERM 402

C3219 0.1UF 20% 10V CERM 402

C3220 0.1UF 20% 10V CERM 402

C3221 0.1UF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

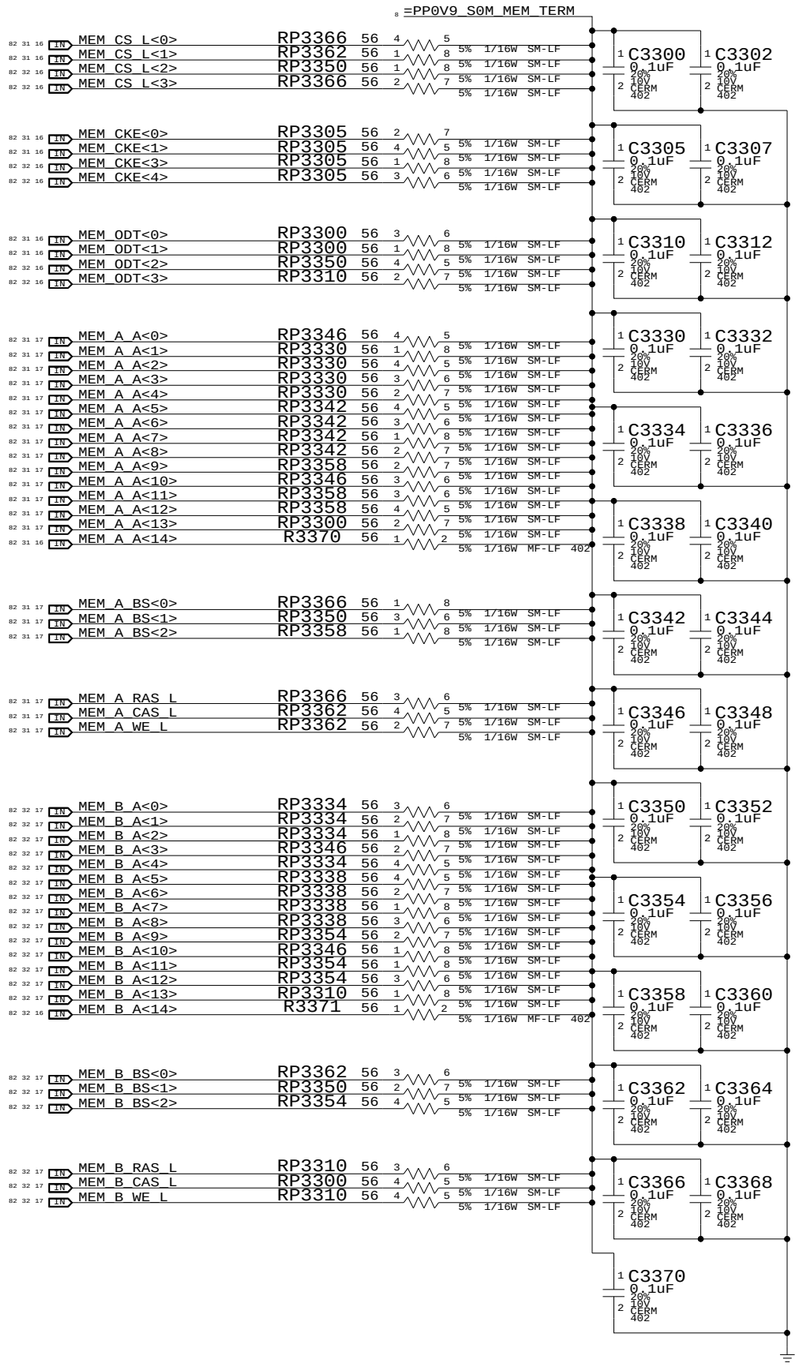
SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 32 OF 89	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

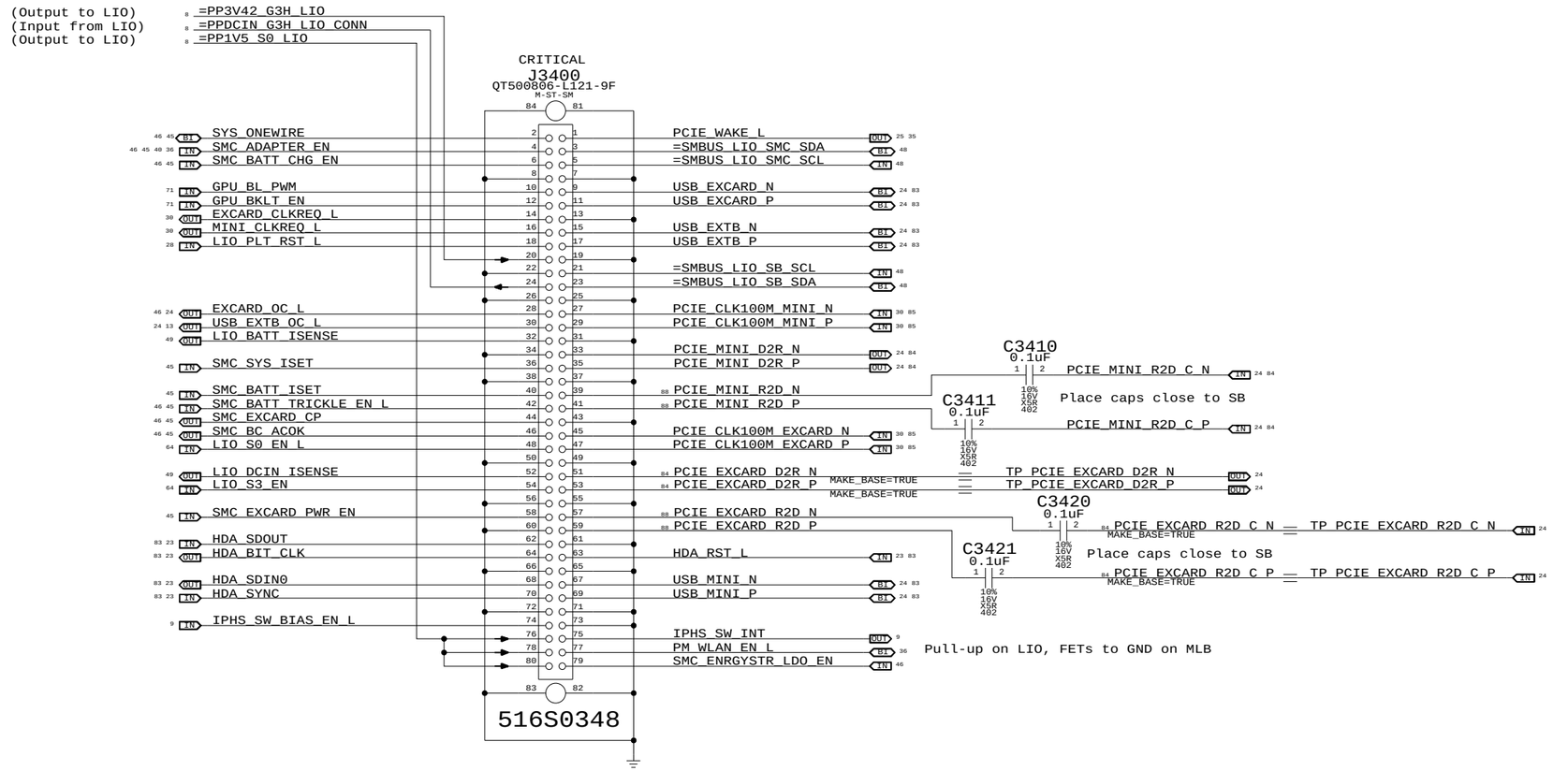
SYNC_MASTER=(T9_NOME) SYNC_DATE=11/14/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	33	89

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 34 OF 89	

Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

=PP1V2_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	171 mA	No link:	130 mA
10 Mbps:	179 mA	10 Mbps:	130 mA
100 Mbps:	203 mA	100 Mbps:	150 mA
1000 Mbps:	426 mA	1000 Mbps:	290 mA

C3700 4.7UF 20% 6.3V CERM 603; C3701 0.1UF 10% 16V X5R 402; C3702 0.1UF 10% 16V X5R 402; C3703 0.1UF 10% 16V X5R 402; C3704 0.1UF 10% 16V X5R 402; C3705 0.1UF 10% 16V X5R 402; C3706 0.001UF 10% 50V CERM 402; C3707 0.001UF 10% 50V CERM 402; C3708 0.001UF 10% 50V CERM 402

=PP3V3_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	4 mA	No link:	60 mA
10 Mbps:	4 mA	10 Mbps:	70 mA
100 Mbps:	4 mA	100 Mbps:	70 mA
1000 Mbps:	4 mA	1000 Mbps:	80 mA

C3710 4.7UF 20% 6.3V CERM 603; C3711 0.1UF 10% 16V X5R 402; C3712 0.1UF 10% 16V X5R 402; C3713 0.1UF 10% 16V X5R 402; C3714 0.001UF 10% 50V CERM 402; C3715 0.001UF 10% 50V CERM 402

=PP1V8R2V5_ENET_PHY L3720 FERR-120-OHM-1.5A 0402 PP1V8R2V5_ENET_PHY_AVDD
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

Yukon EC (2.5V)		Yukon Ultra (1.8V)	
No link:	82 mA	No link:	0 mA
10 Mbps:	108 mA	10 Mbps:	30 mA
100 Mbps:	126 mA	100 Mbps:	40 mA
1000 Mbps:	218 mA	1000 Mbps:	150 mA

(EC:2.5V)

C3720 4.7UF 20% 6.3V CERM 603; C3721 0.1UF 10% 16V X5R 402; C3722 0.1UF 10% 16V X5R 402; C3723 0.1UF 10% 16V X5R 402; C3724 0.001UF 10% 50V CERM 402

=YUKON_EC_PP2V5_ENET
Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
Yukon Ultra: Alias to GND

PCIE_ENET_D2R_P (OUT) — C3735 0.1uF 10% 16V X5R 402 — PCIE_ENET_D2R_C_P
PCIE_ENET_D2R_N (OUT) — C3736 0.1uF 10% 16V X5R 402 — PCIE_ENET_D2R_C_N
PLACEMENT_NOTE=Place C3730 close to southbridge.
PCIE_ENET_R2D_C_P (IN) — C3730 0.1uF 10% 16V X5R 402 — PCIE_ENET_R2D_P
PCIE_ENET_R2D_C_N (IN) — C3731 0.1uF 10% 16V X5R 402 — PCIE_ENET_R2D_N
PLACEMENT_NOTE=Place C3731 close to southbridge.
PCIE_CLK100M_ENET_P (IN)
PCIE_CLK100M_ENET_N (IN)
=ENET_CLKREQ_L (OUT) — Yukon EC: Pin 42 should be NC (or TP) net.
PCIE_WAKE_L (OUT)
ENET_RESET_L (IN)
ENET_MDI_P<0> (BI)
ENET_MDI_N<0> (BI)
ENET_MDI_P<1> (BI)
ENET_MDI_N<1> (BI)
ENET_MDI_P<2> (BI)
ENET_MDI_N<2> (BI)
ENET_MDI_P<3> (BI)
ENET_MDI_N<3> (BI)

SIGNAL_MODEL=EMPTY
R3740 49.9 1% 1/16W MF-LF 402; R3741 49.9 1% 1/16W MF-LF 402 — ENET_MDI0 — C3740 0.001UF 10% 50V CERM 402
R3742 49.9 1% 1/16W MF-LF 402; R3743 49.9 1% 1/16W MF-LF 402 — ENET_MDI1 — C3742 0.001UF 10% 50V CERM 402
R3744 49.9 1% 1/16W MF-LF 402; R3745 49.9 1% 1/16W MF-LF 402 — ENET_MDI2 — C3744 0.001UF 10% 50V CERM 402
R3746 49.9 1% 1/16W MF-LF 402; R3747 49.9 1% 1/16W MF-LF 402 — ENET_MDI3 — C3746 0.001UF 10% 50V CERM 402

ENET_CLK25M_XTALI (IN)
ENET_CLK25M_XTALO (OUT)

U3700 88E8058 QFN — CRITICAL — OMIT

NC_32	32		
NC_51	51		
NC_52	52		
NC_57	57		
NC_64	64		
AVDD0	19		
AVDD1	22		
AVDD2	23		
AVDD3	28		
		EC:AVDD 2.5V	
VDDO_TTL0	1		
VDDO_TTL1	40		
VDDO_TTL2	45		
VDDO_TTL3	61		
AVDDH	8		
VDD0	2		
VDD1	7		
VDD2	13		
VDD3	33		
VDD4	39		
VDD5	44		
VDD6	48		
VDD7	58		
TX_P	49	PCIE_ENET_D2R_C_P	
TX_N	50	PCIE_ENET_D2R_C_N	
RX_P	54	PCIE_ENET_R2D_P	
RX_N	53	PCIE_ENET_R2D_N	
REFCLKP	55		
REFCLKN	56		
CLKREQ*	42		EC:NO CONNECT
WAKE*	6		
PERST*	5		
MDIP0	17		
MDIN0	18		
MDIP1	20		
MDIN1	21		
MDIP2	26		
MDIN2	27		
MDIP3	30		
MDIN3	31		
XTALI	15		
XTALO	14		
THRML_PAD	65		

PCI EXPRESS

ANALOG
- LOM_DISABLE* 10 — ENET_LOM_DIS_L
- VAUX_AVLBL 12
- SWITCH_VAUX 9 — NC
- VMAIN_AVLBL 47 — Must be high in S0 state (can use PP3V3_S0 as input) =ENET_VMAIN_AVLBL (IN 64)
- SWITCH_VCC 11 — NC
- EC:CTRL25 CTRL18 4 — TP_YUKON_CTRL18 (OUT)
- CTRL12 3 — TP_YUKON_CTRL12 (OUT)
- RSET 16 — YUKON_RSET

R3760 4.7K 5% 1/10W MF-LF 402

YUKON_ULTRA
R3765 4.99K 1% 1/16W MF-LF 402

LED
- LED_ACT* 59 — NC
- LED_LINK10/100* 60 — NC
- LED_LINK1000* 62 — NC
- LED_DUPLEX* 63 — NC

SPI
- (IPU) SPI_DO 34 — NC
- (IPU) SPI_DI 35 — NC
- (IPU) SPI_CLK 37 — NC
- (IPU) SPI_CS 36 — NC

MEDIA

TWSI
- (IPU) VPD_CLK 38 — YUKON_VPD_CLK
- (IPU) VPD_DATA 41 — YUKON_VPD_DATA

TEST/RSVD
- (IPD) TESTMODE 46
- RSVD_24 24 — NC
- RSVD_25 25 — NC
- RSVD_29 29 — NC
- RSVD_43 43 — NC

MAIN CLK

VPD ROM
C3780 0.1UF 10% 16V X5R 402
R3780 4.7K 5% 1/10W MF-LF 402
R3781 4.7K 5% 1/10W MF-LF 402
U3780 M24C08 SO8 — CRITICAL
VCC 8; E2 3; NC NC1 2; NC NC0 1; WC* 7; SDA 5; SCL 6; VSS 4

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONs to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 35 OF 89	

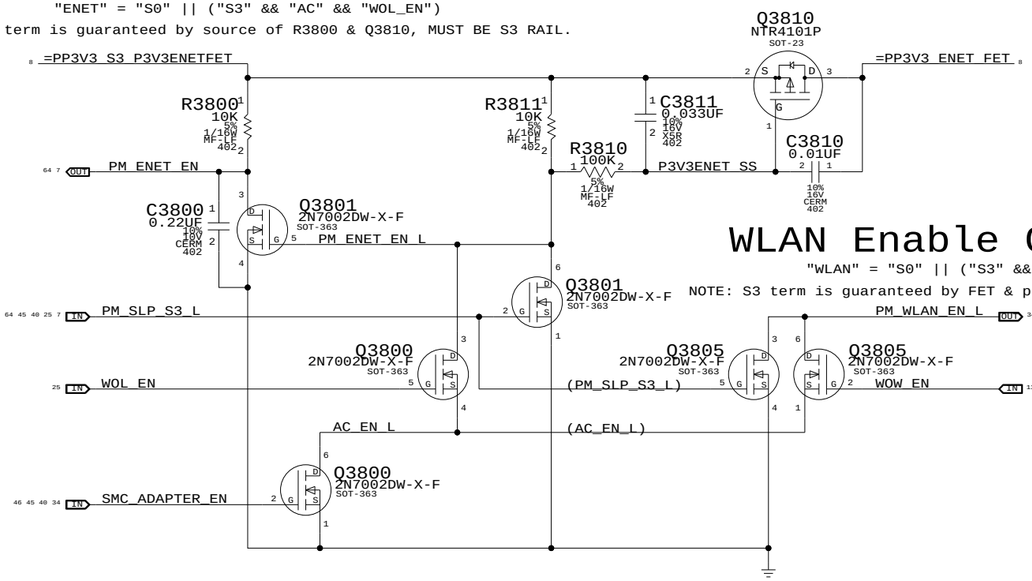
ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

3.3V ENET FET

CRITICAL



WLAN Enable Generation

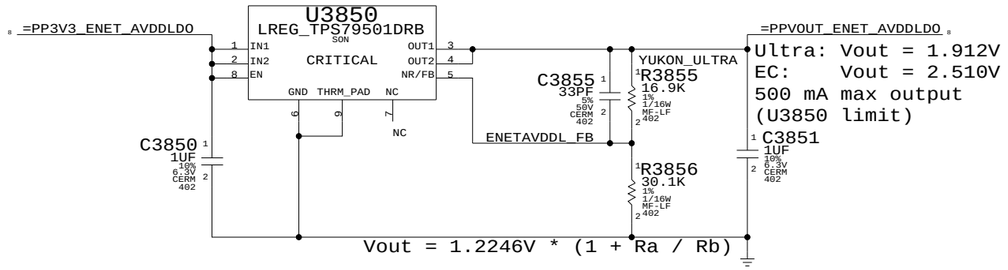
"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")

NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

Yukon AVDDL LDO

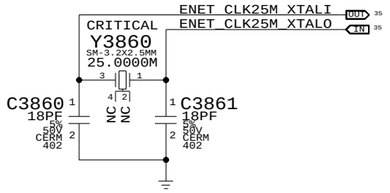
1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

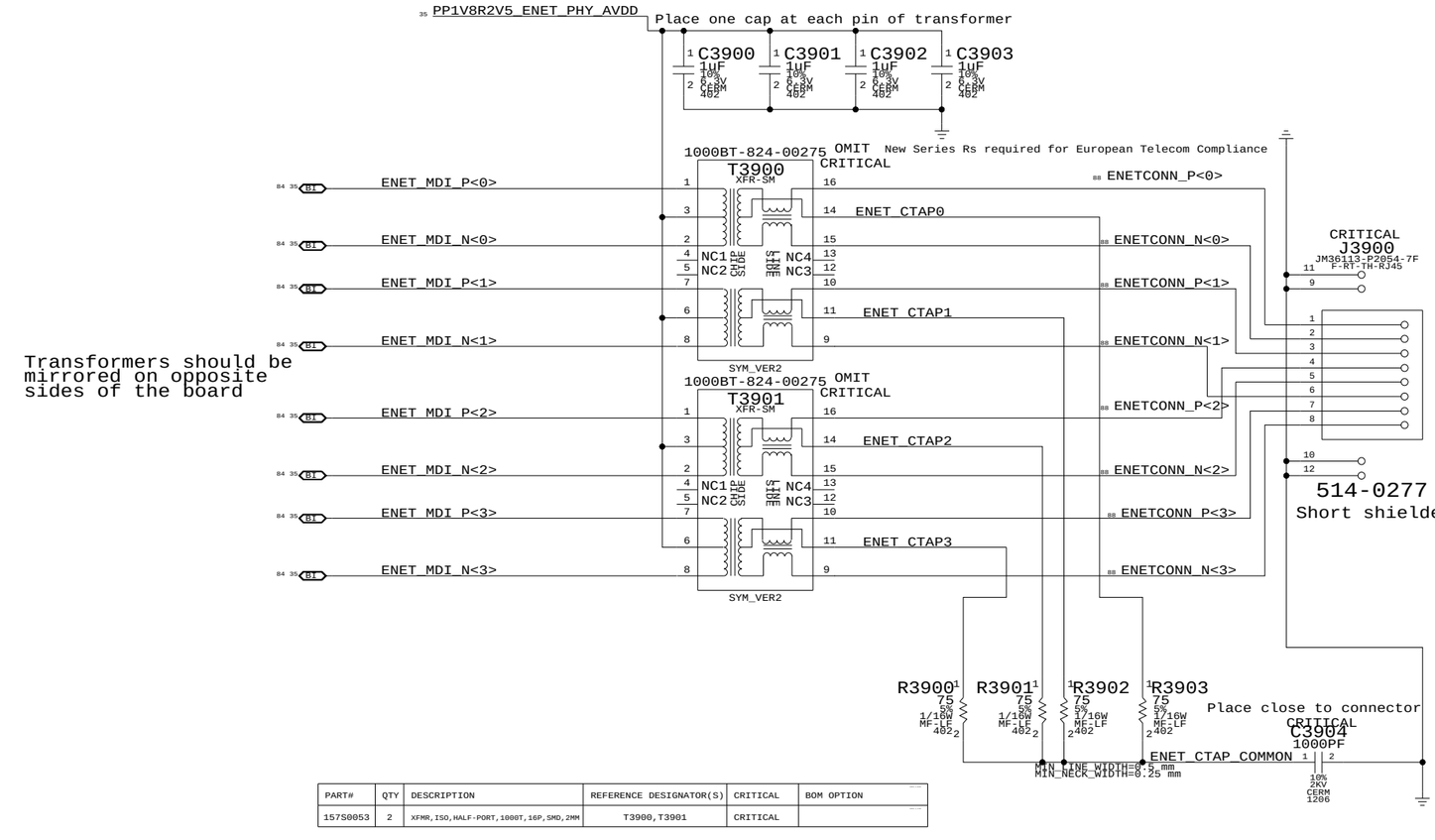
SCALE	SHT	OF
NONE	36	89

Page Notes

Power aliases required by this page:
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
157S0053	2	XFMR,ISO,HALF-PORT,1000T,16P,SMD,2MM	T3900,T3901	CRITICAL	

Ethernet Connector

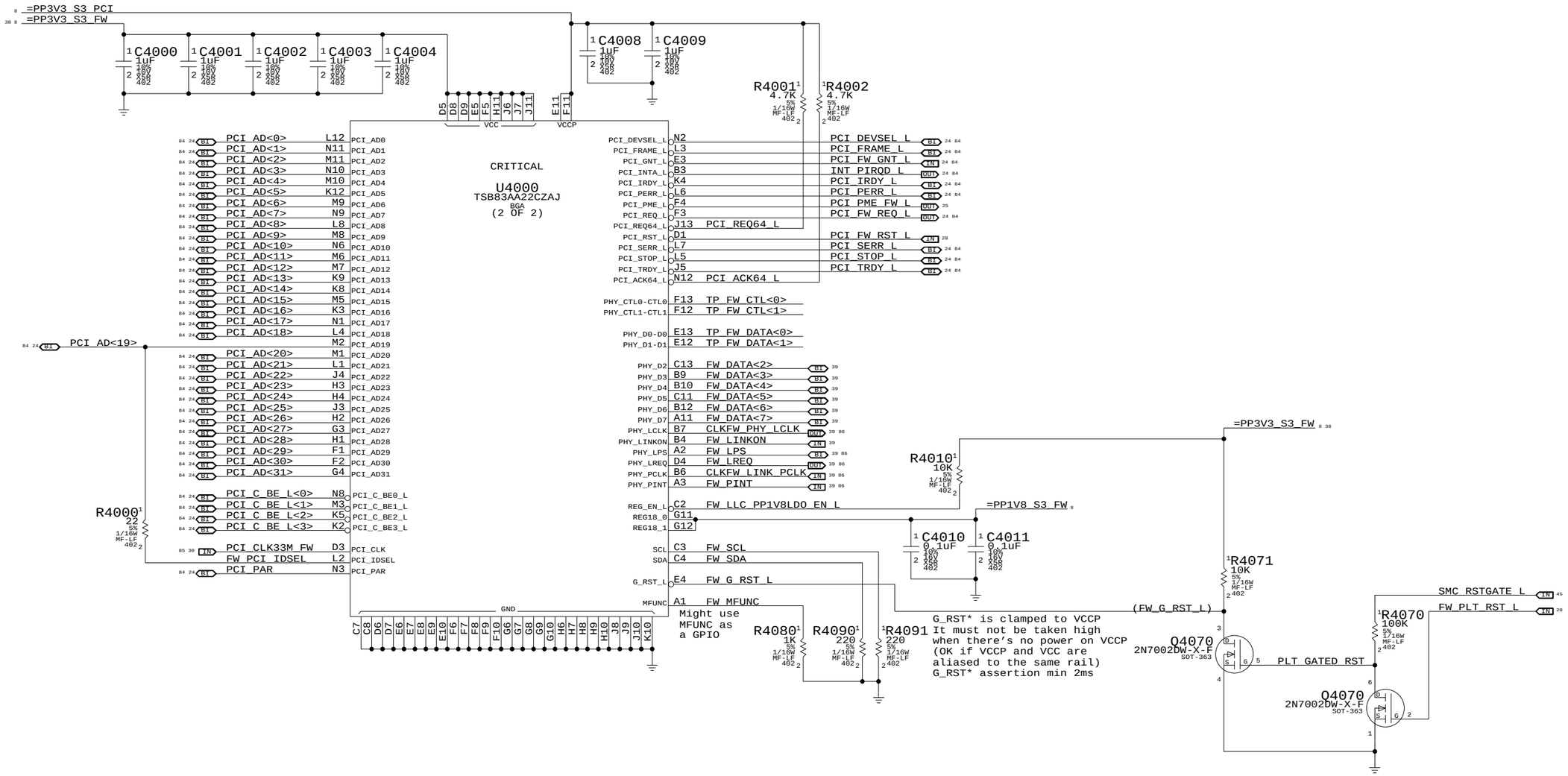
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE: NONE

SHT 37 OF 89



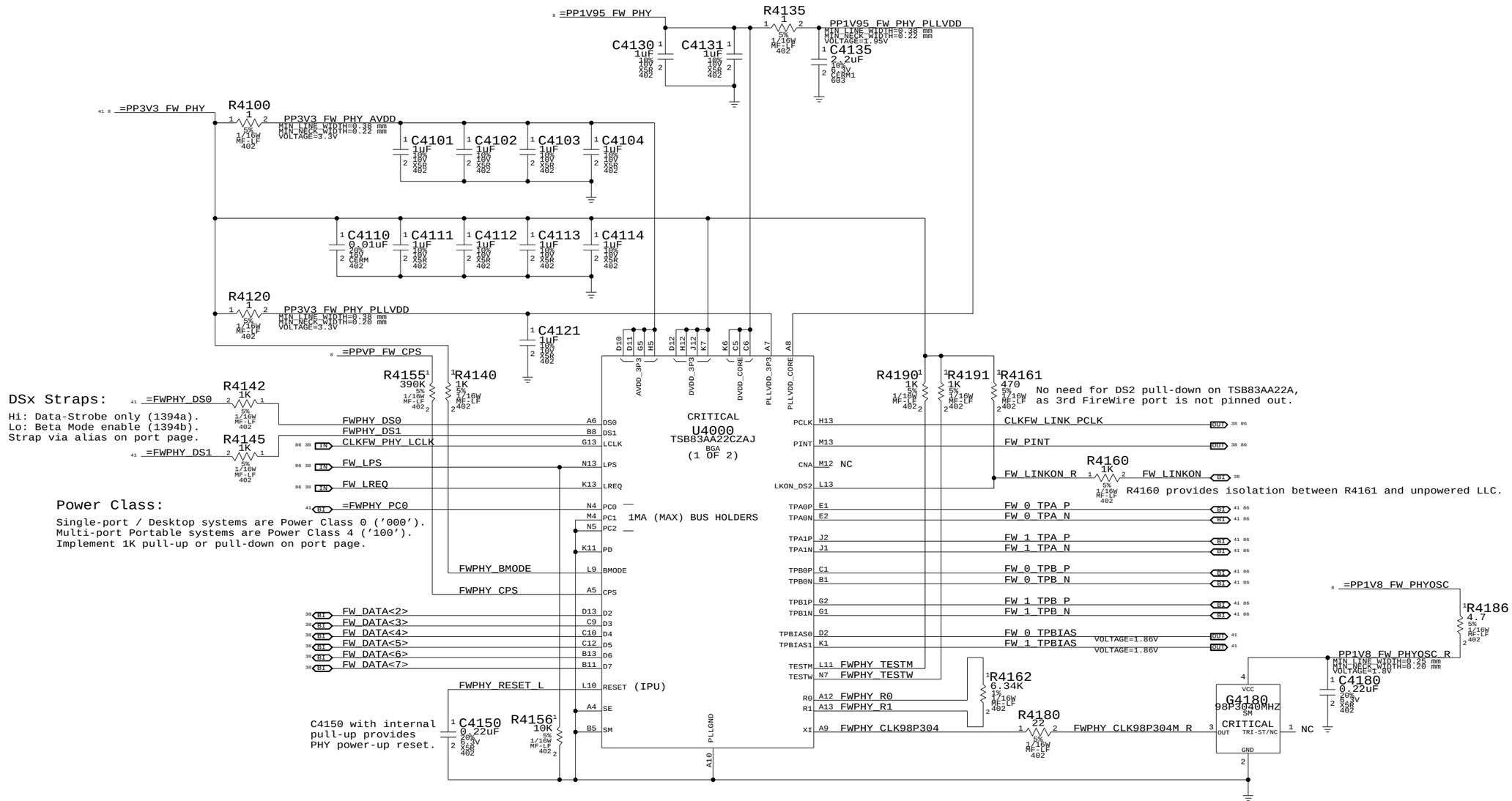
FireWire Link (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 38 OF 89	



FireWire PHY (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 39 OF 89	

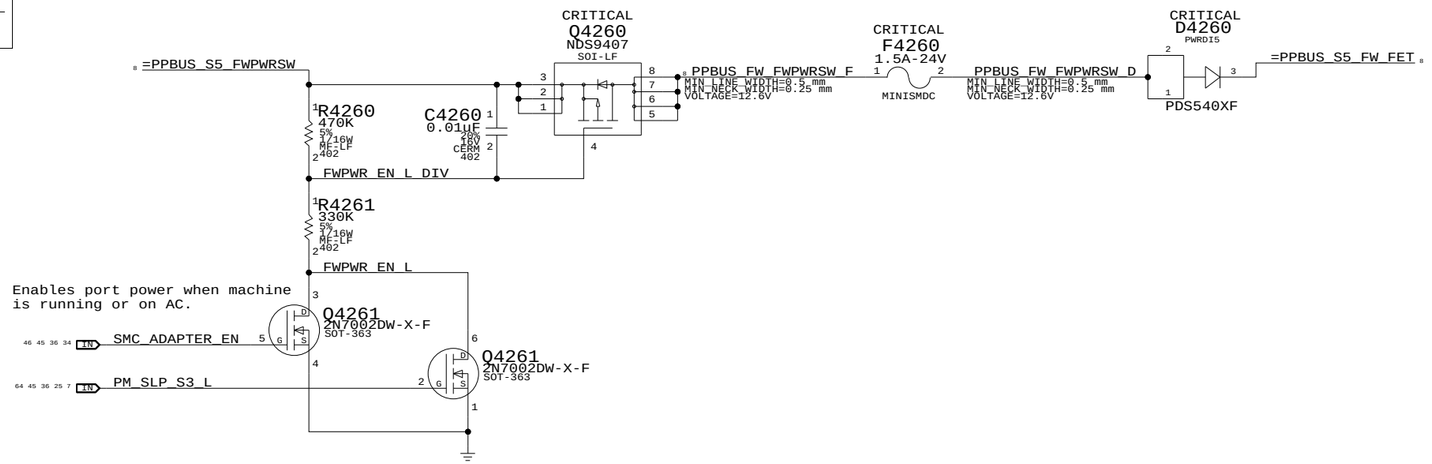
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

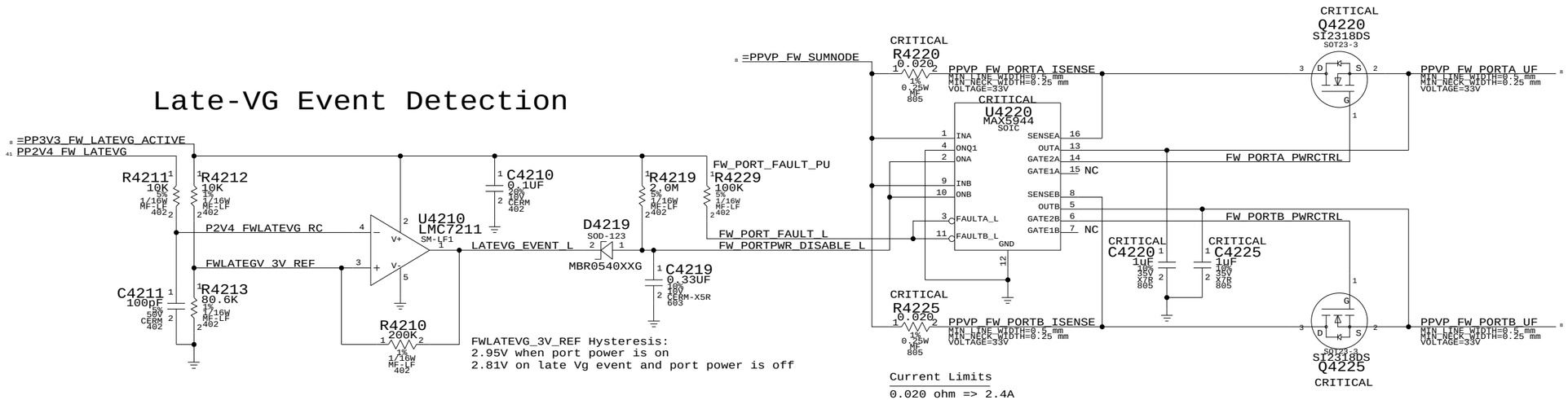
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Current Limit/Active Late-VG Protection



FWLATEVG_3V_REF Hysteresis:
2.95V when port power is on
2.81V on late Vg event and port power is off

Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

Late-VG Event Detection

FireWire Port Power

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	40	89

Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT0
- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG
- =GND_CHASSIS_FW_PORT0L
- =GND_CHASSIS_FW_PORT0U
- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:
- 2-port Portable Power Class (4)
- Port "0" Data-Strobe only (1394A)
- Port "1" Bilingual (1394B)

39 8 =PP3V3_FW_PHY
39 =FWPHY_PC0
39 =FWPHY_DS0
39 =FWPHY_DS1

Termination

Place close to FireWire PHY

TI PHYs require 1uF even though FW spec calls out 0.33uF

39 FW_1_TPBIAS
39 FW_0_TPBIAS
C4350 1uF 10% 6.3V CERM 402
C4360 1uF 10% 6.3V CERM 402
CRITICAL L4360 18NH-250MA 0402
CRITICAL L4361 18NH-250MA 0402
FW_B_TPA_L_P
FW_B_TPA_L_N
R4350 56.2 1% 1/16W MF-LF 402
R4351 56.2 1% 1/16W MF-LF 402
R4360 56.2 1% 1/16W MF-LF 402
R4361 56.2 1% 1/16W MF-LF 402

86 39 FW_0_TPA_P — FW_PORT0_TPA_P 41 MAKE_BASE=TRUE
86 39 FW_0_TPA_N — FW_PORT0_TPA_N 41 MAKE_BASE=TRUE
86 39 FW_0_TPB_P — FW_PORT0_TPB_P 41 MAKE_BASE=TRUE
86 39 FW_0_TPB_N — FW_PORT0_TPB_N 41 MAKE_BASE=TRUE
86 39 FW_1_TPA_P — FW_PORT1_TPA_P 41 MAKE_BASE=TRUE
86 39 FW_1_TPA_N — FW_PORT1_TPA_N 41 MAKE_BASE=TRUE
86 39 FW_1_TPB_P — FW_PORT1_TPB_P 41 MAKE_BASE=TRUE
86 39 FW_1_TPB_N — FW_PORT1_TPB_N 41 MAKE_BASE=TRUE

SIGNAL_MODEL=EMPTY
R4352 56.2 1% 1/16W MF-LF 402
R4353 56.2 1% 1/16W MF-LF 402
R4362 56.2 1% 1/16W MF-LF 402
R4363 56.2 1% 1/16W MF-LF 402
FW_B_TPB_L_N
FW_B_TPB_L_P
CRITICAL L4362 18NH-250MA 0402
CRITICAL L4363 18NH-250MA 0402
SIGNAL_MODEL=EMPTY
FW_PORT0_TPB_C
FW_PORT1_TPB_C
C4354 220pF 5% 25V CERM 402
R4354 4.99K 1% 1/16W MF-LF 402
C4364 220pF 5% 25V CERM 402
R4364 4.99K 1% 1/16W MF-LF 402

Late-VG Protection Power

8 =PP3V3_FW_LATEVG
R4390 332 1% 1/16W MF-LF 402
PP2V4_FW_LATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V 40 41
CRITICAL D4390 MMBZ5227B SOT23

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

ESD and late-VG rail for snap-back diodes (Common to all ports)

Cable Power

8 =PPVP_FW_PORT0
CRITICAL L4300 FERR-250-OHM SM
PPVP_FW_PORT0 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V
C4304 0.01UF 10% 50V X7R 402

Note: Trace PPVP_FW_PORT0 must handle up to 5A

"Snapback" & "Late VG" Protection

41 40 PP2V4_FW_LATEVG
DP4300 BAV99DW-X-F SOT-363
C4300 0.01uF 10% 50V X7R 402
C4301 0.01uF 10% 50V X7R 402

41 FW_PORT0_TPA_P
41 FW_PORT0_TPA_N
41 FW_PORT0_TPB_P
41 FW_PORT0_TPB_N

DP4301 BAV99DW-X-F SOT-363
C4302 0.01uF 10% 50V X7R 402
C4303 0.01uF 10% 50V X7R 402

CRITICAL FL4300 90-OHM-100MA 1210-4SM1
CRITICAL FL4301 90-OHM-100MA 1210-4SM1

88 FW_PORT0_TPA_FL_P
88 FW_PORT0_TPA_FL_N
88 FW_PORT0_TPB_FL_P
88 FW_PORT0_TPB_FL_N
(GND_FW_PORT0_VG)

PORT 0
1394A
CRITICAL J4300 1394A F-RT-TH-LF
6 TPO (TPA+)
5 TPO# (TPA-)
4 TPI (TPB+)
3 TPI# (TPB-)
1 VP
2 VGND
7 8 9 10
514-0255

Cable Power

8 =PPVP_FW_PORT1
CRITICAL L4310 FERR-250-OHM SM
PPVP_FW_PORT1 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V
C4314 0.01UF 10% 50V X7R 402

Note: Trace PPVP_FW_PORT1 must handle up to 5A

"Snapback" & "Late VG" Protection

41 40 PP2V4_FW_LATEVG
DP4310 BAV99DW-X-F SOT-363
C4311 0.01uF 10% 50V X7R 402
C4310 0.01uF 10% 50V X7R 402

41 FW_PORT1_TPB_N
41 FW_PORT1_TPB_P
41 FW_PORT1_TPA_N
41 FW_PORT1_TPA_P

DP4311 BAV99DW-X-F SOT-363
C4312 0.01uF 10% 50V X7R 402
C4313 0.01uF 10% 50V X7R 402

C4319 0.1uF 10% 50V X7R 603-1
R4319 1M 5% 1/16W MF-LF 402

(FW_PORT1_BREF)
(GND_FW_PORT1_VG)
FW_PORT1_AREF

PORT 1
BILINGUAL
CRITICAL J4310 1394B-UG31903 F-RT-SM1
1 TPB- OUTPUT
9 TPB<R> OUTPUT
2 TPB+ OUTPUT
8 VP
NC 7 NC
6 VG
3 TPA- INPUT
5 TPA<R> INPUT
4 TPA+ INPUT
10 11
514S0133

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

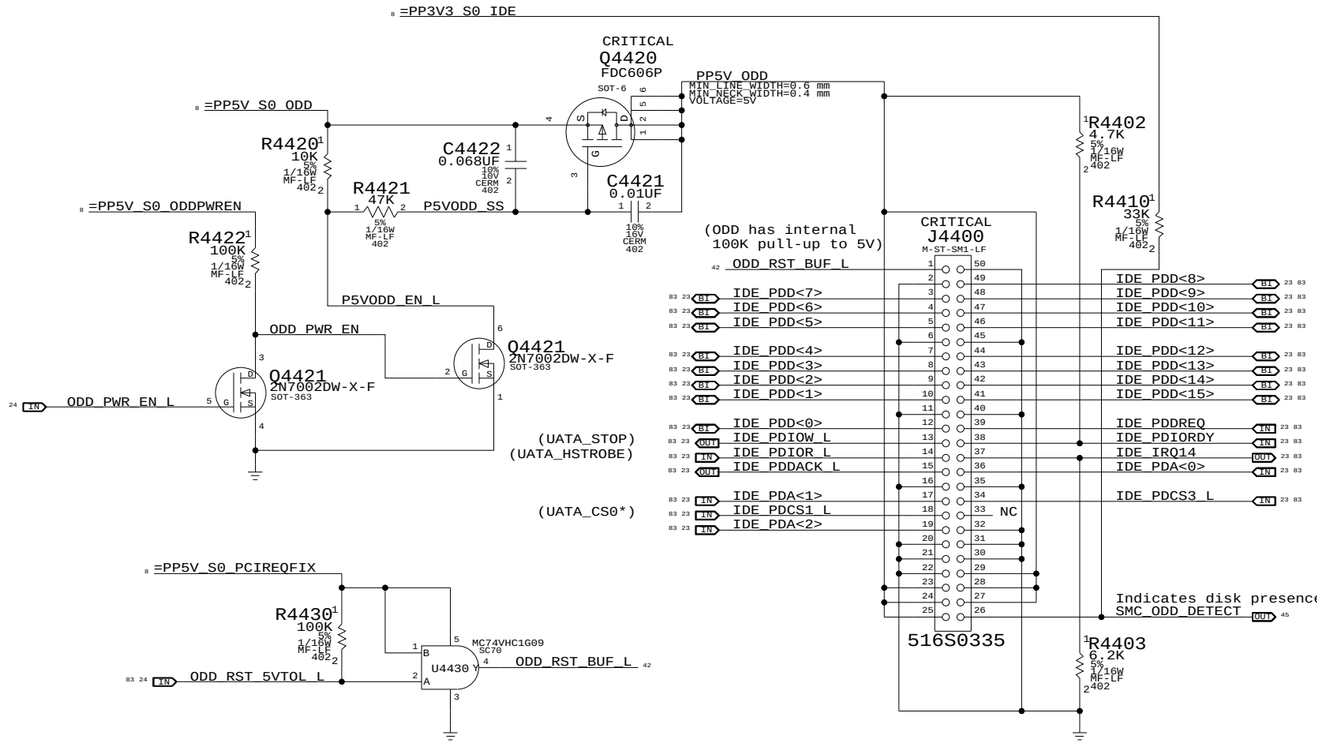
FireWire Ports

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

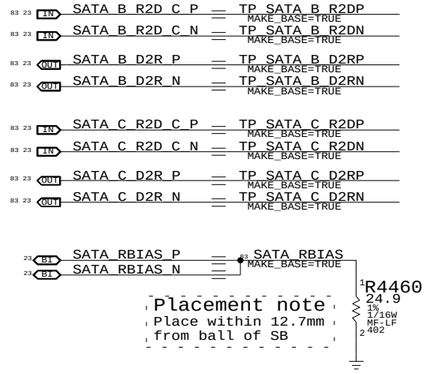
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 41 OF 89	

IDE (ODD) Connector



Unused SATA Ports



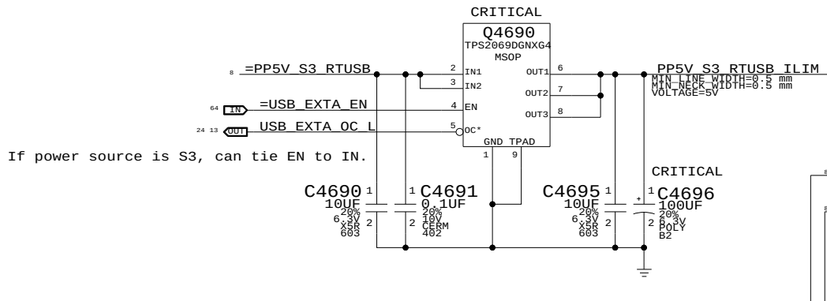
PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

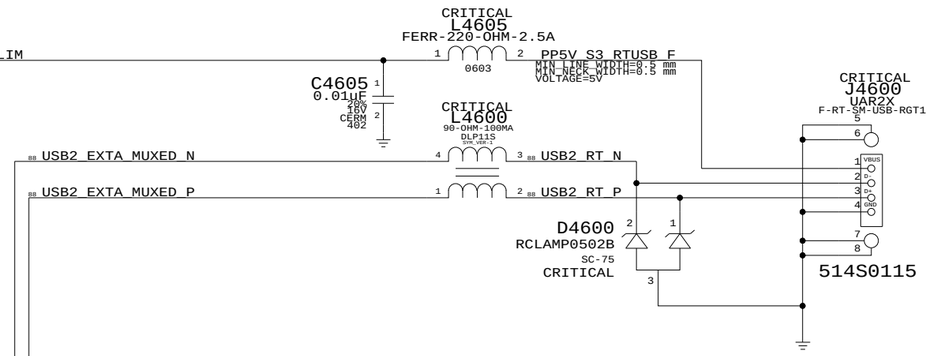
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 42 OF 89	

Port Power Switch

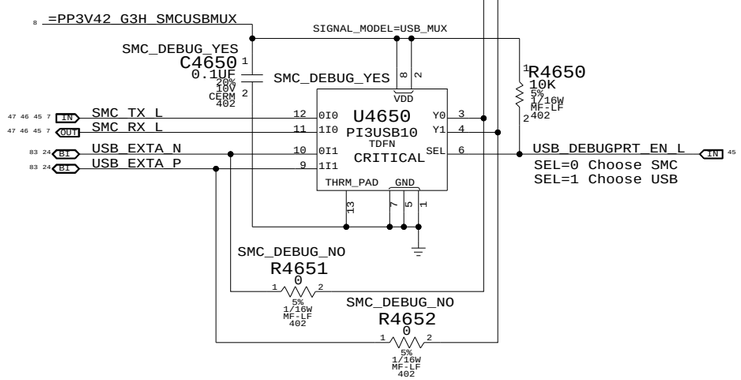


Right USB Port



Place L4600 and L4605 at connector pin

USB/SMC Debug Mux



External USB Connector

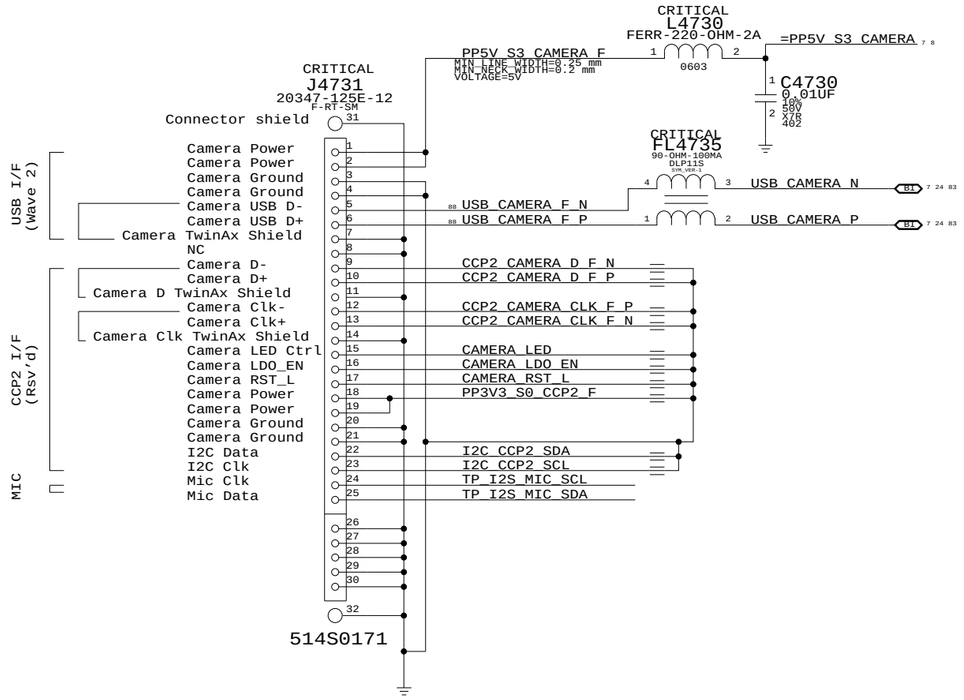
SYNC_MASTER=M88 SYNC_DATE=08/02/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	43	89

Left Clutch Barrel Interconnect



Left Clutch Barrel Interconnect

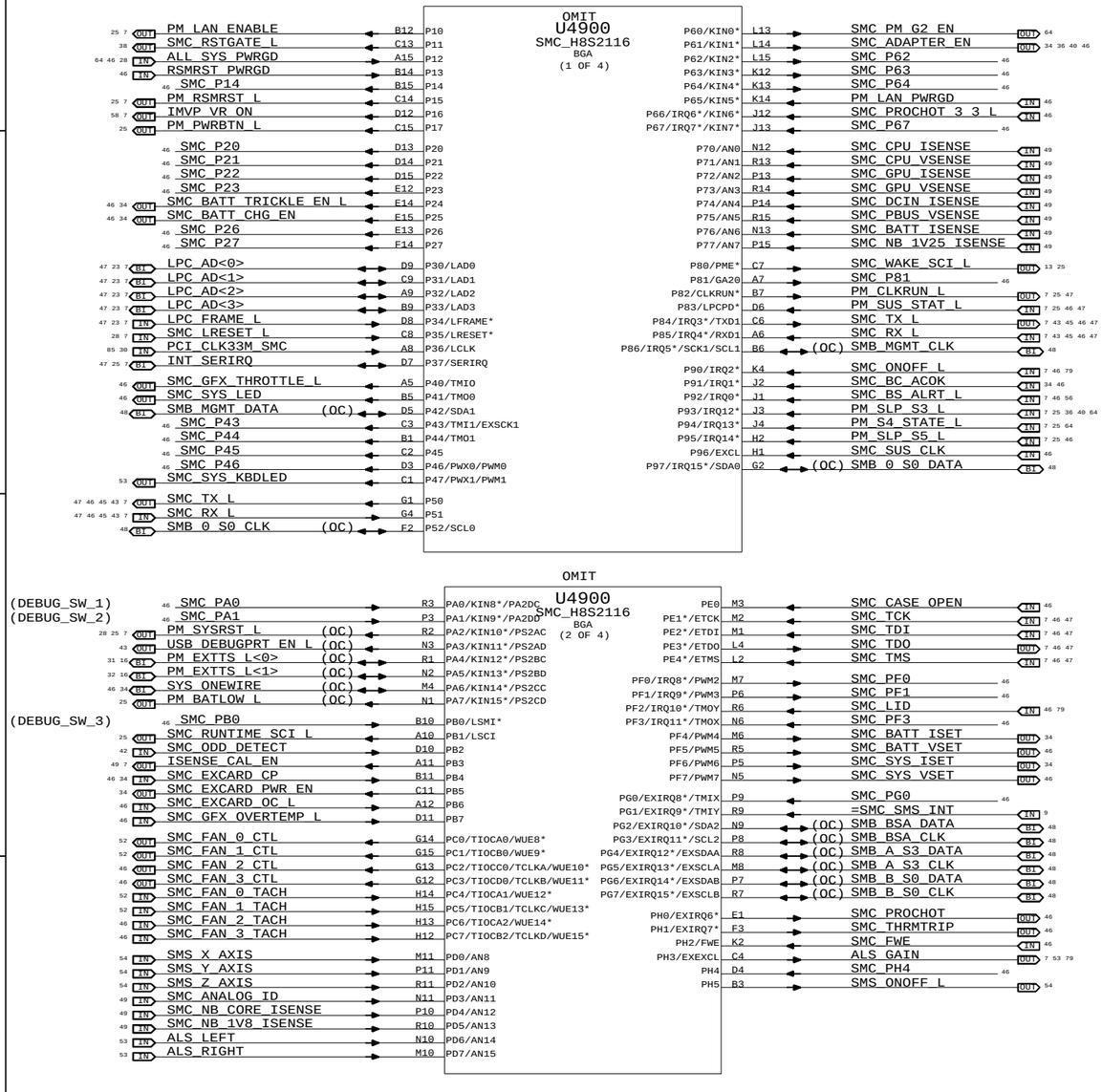
SYNC_MASTER=M87 SYNC_DATE=07/16/2007

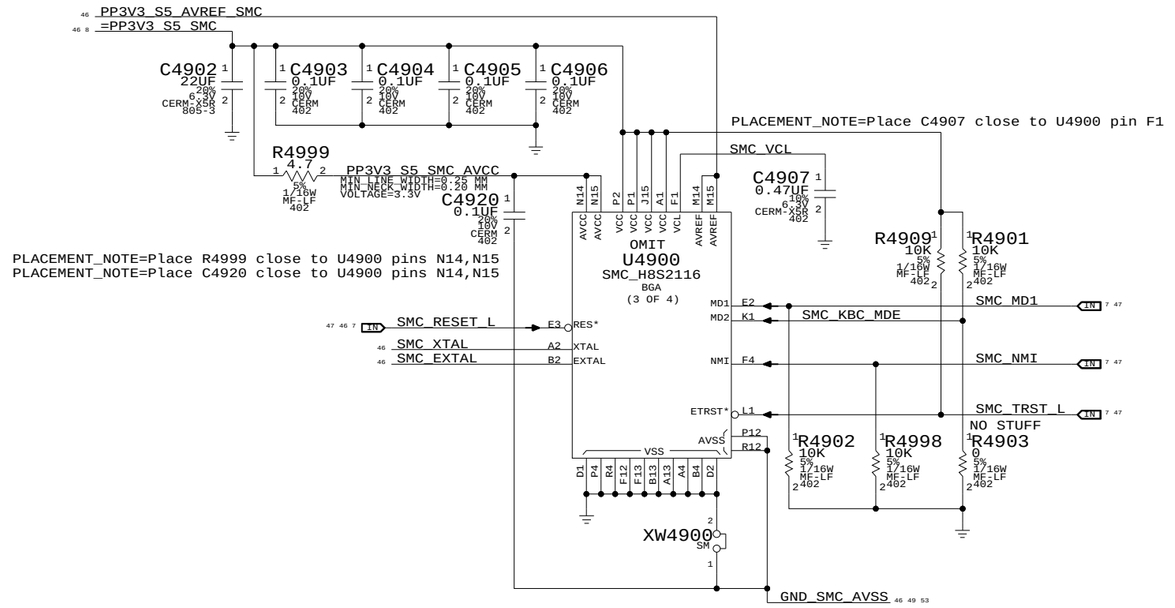
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

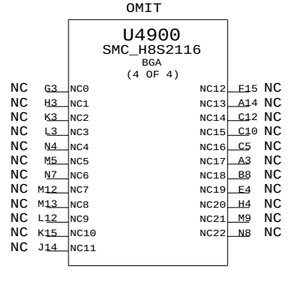
SCALE	SHT	OF
NONE	44	89

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



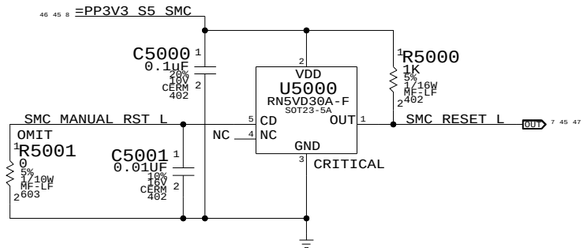
SMC

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

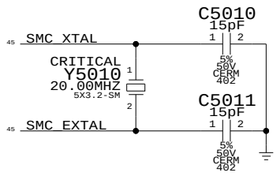
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 45 OF 89	

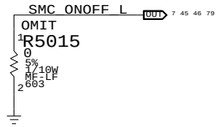
SMC Reset "Button" / Brownout Detect



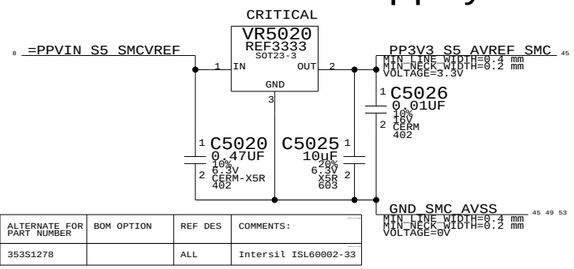
SMC Crystal Circuit



Debug Power "Button"

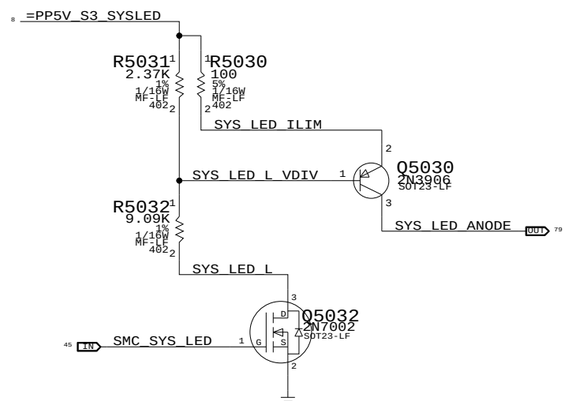


SMC AVREF Supply

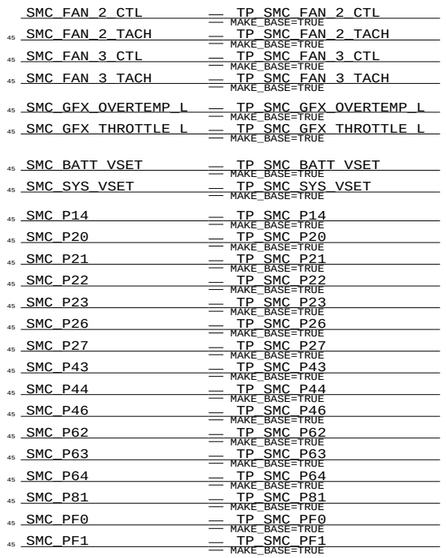


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

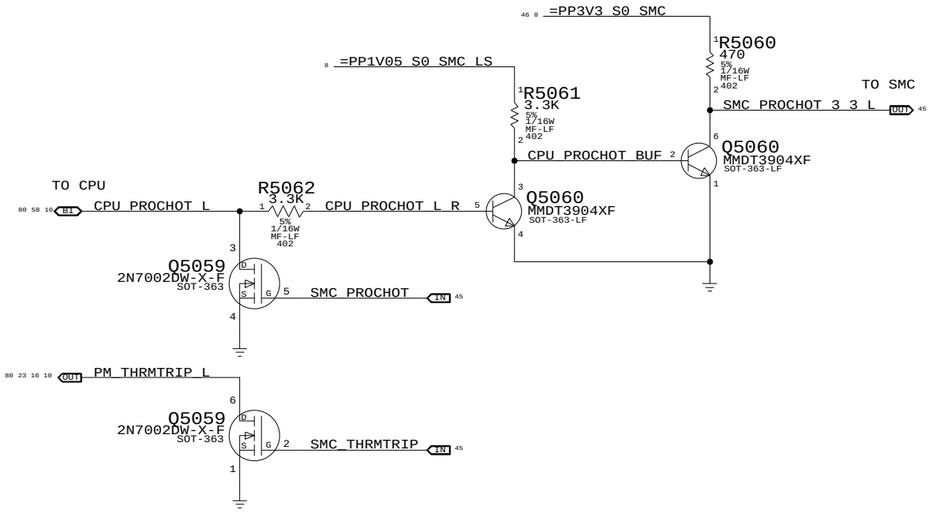
System (Sleep) LED Circuit



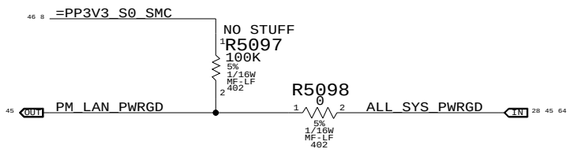
SMC FAN / GFX / Power Signals



SMC FSB to 3.3V Level Shifting

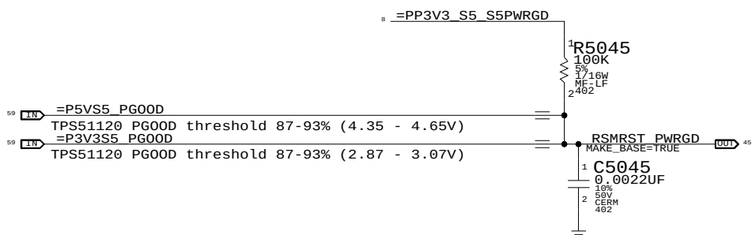


LAN PWRGD Circuit



S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



R5095

SMC Support

SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

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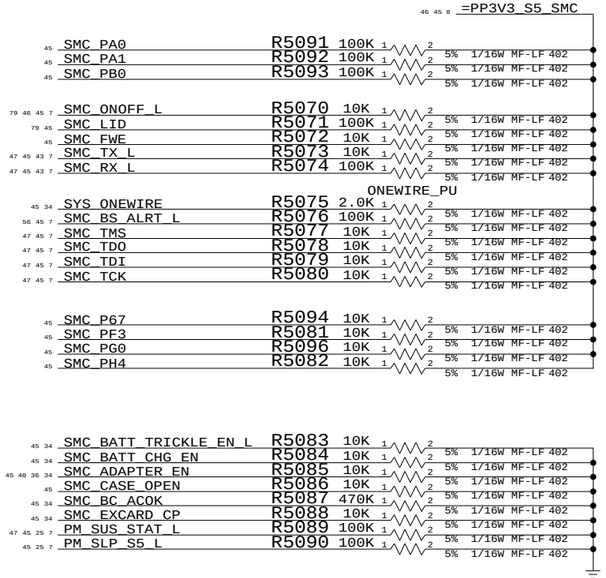
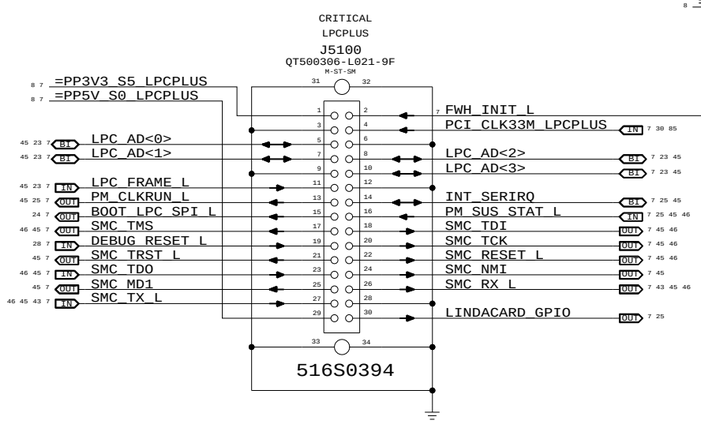
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 46 OF 89	

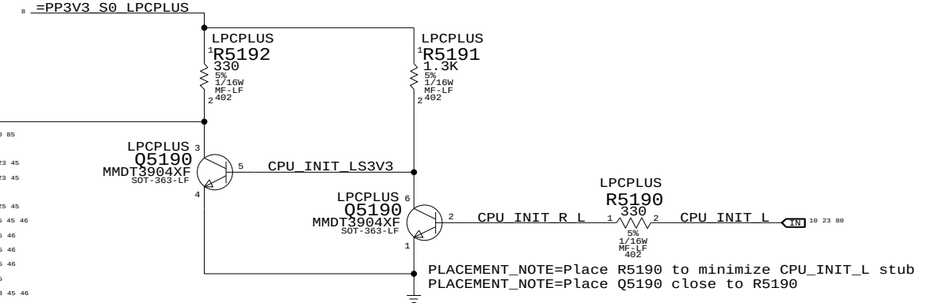
SMC Pull-ups



LPC+ Connector



FWH_INIT_L Generation



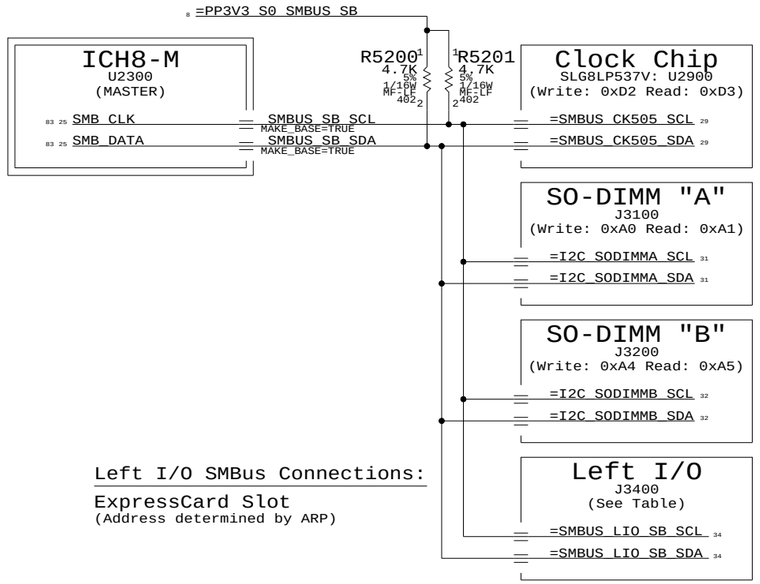
LPC+ Debug Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

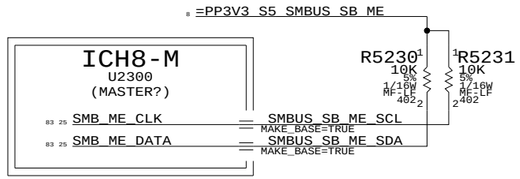
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 47 OF 89	

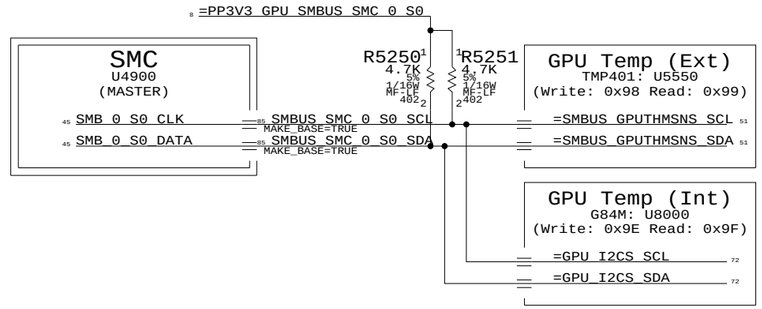
ICH8-M SMBus Connections



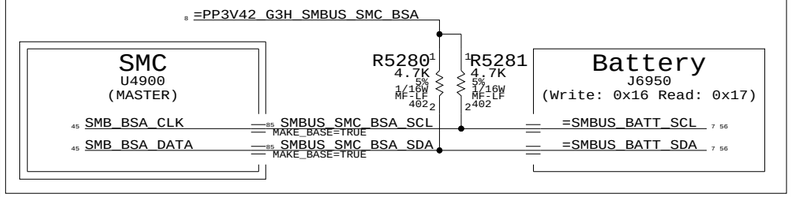
ICH8-M ME SMBus Connections



SMC "0" SMBus Connections

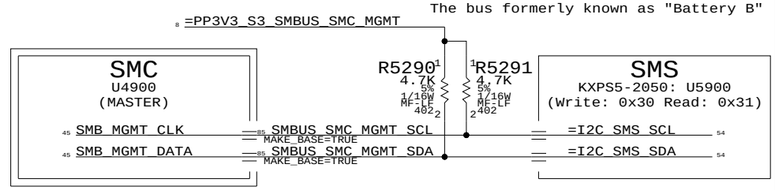


SMC "Battery A" SMBus Connections



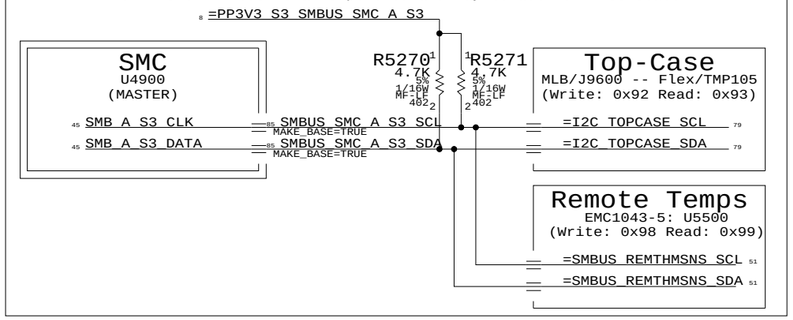
SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

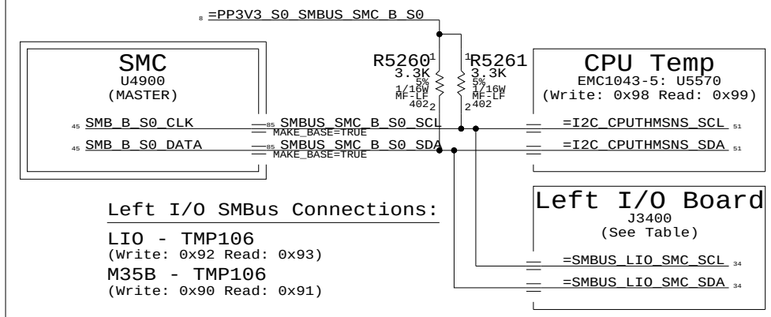


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "B" SMBus Connections



SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

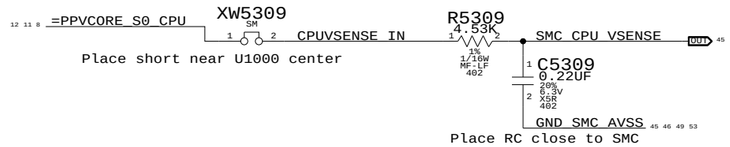
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

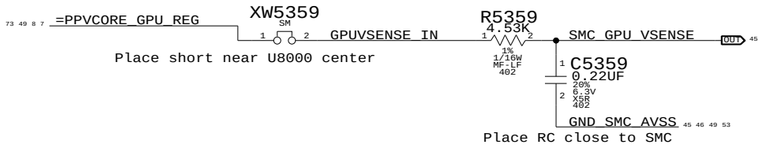
SCALE: NONE

SHT 48 OF 89

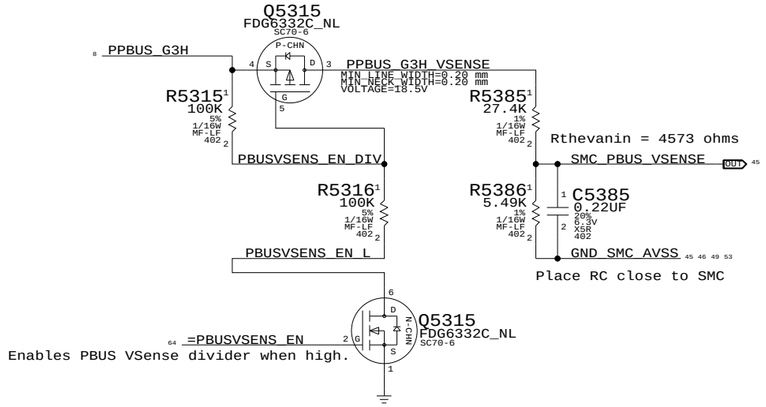
CPU Voltage Sense / Filter



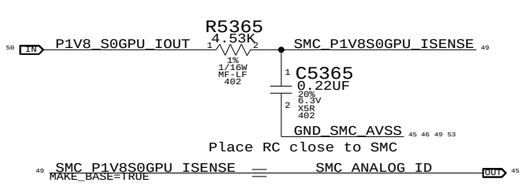
GPU Voltage Sense / Filter



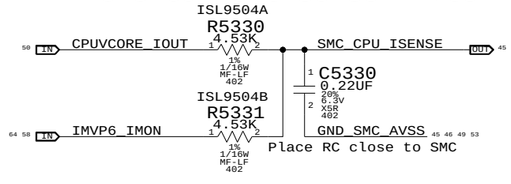
PBUS Voltage Sense & Filter



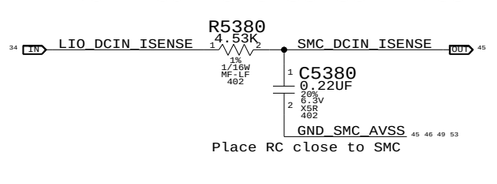
1.8V FB Current Sense Filter



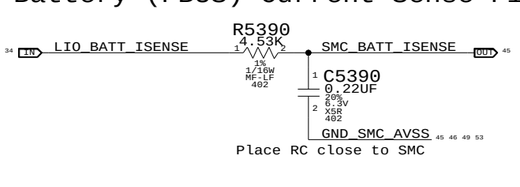
CPU Current Sense Filter



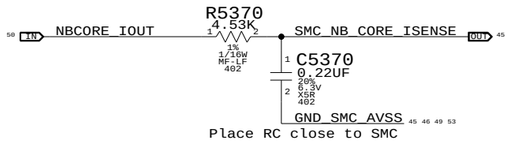
DCIN Current Sense Filter



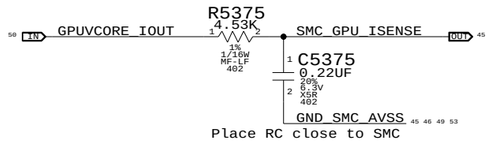
Battery (PBUS) Current Sense Filter



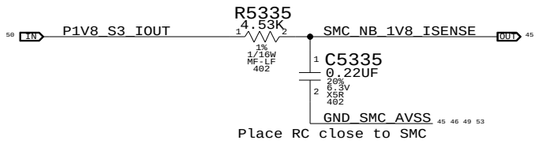
NB Core Current Sense Filter



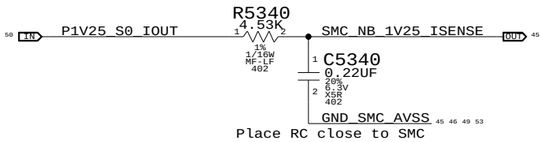
GPU Current Sense Filter



NB 1.8V Current Sense Filter

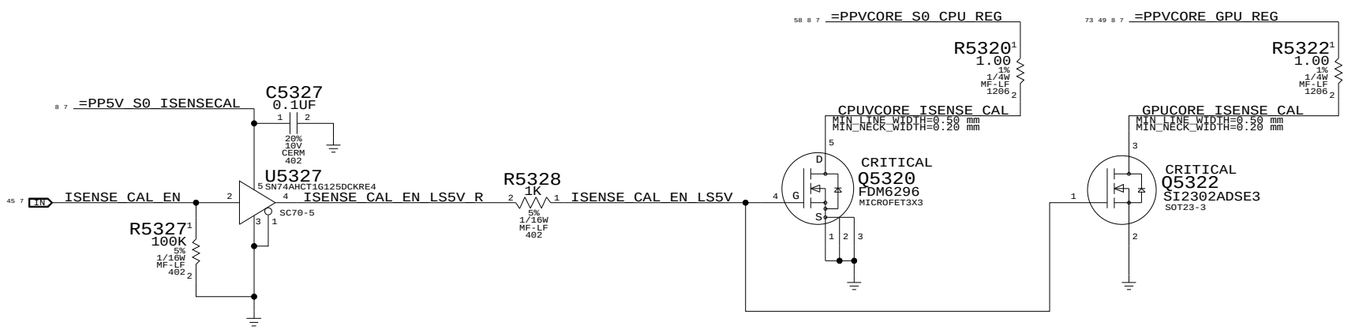


S0/GPU 1.25V Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



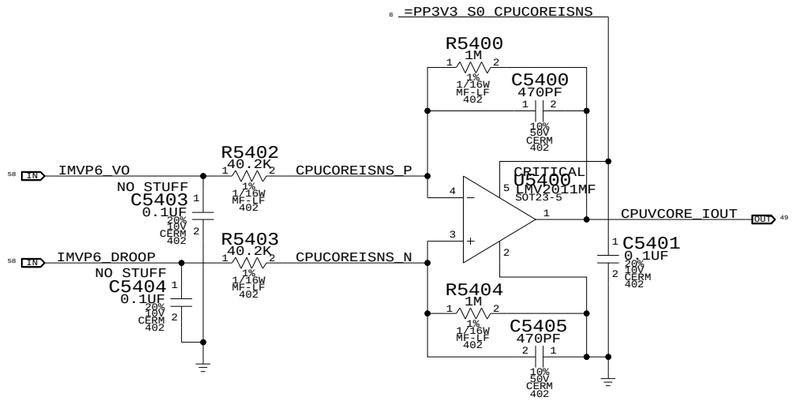
Current & Voltage Sensing

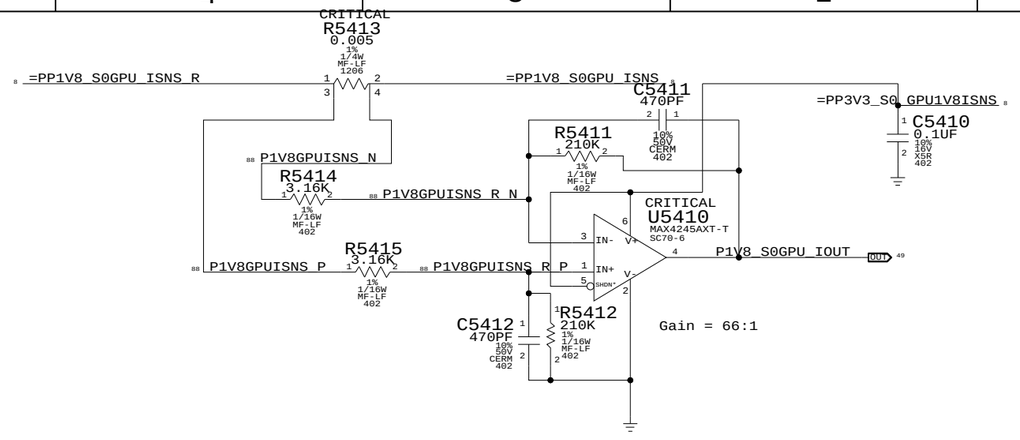
SYNC_MASTER=M87_MLB SYNC_DATE=05/22/2007

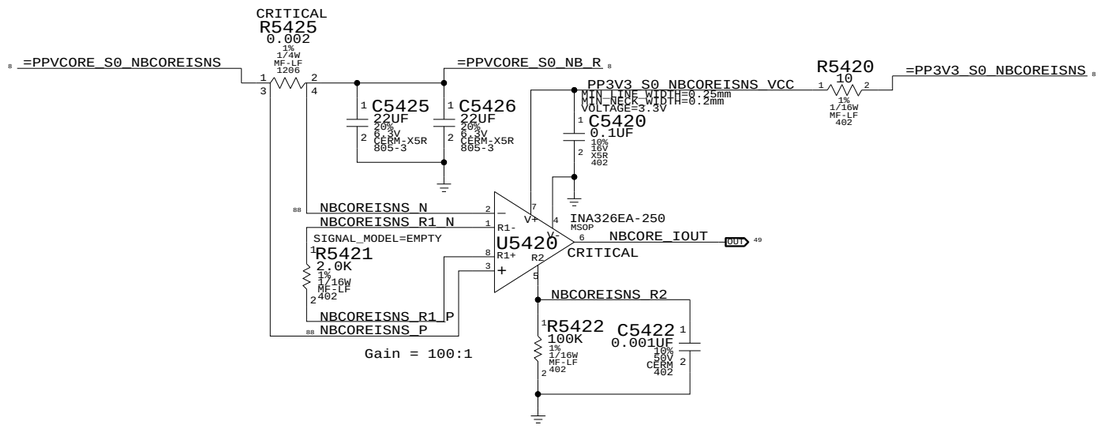
APPLE INC.

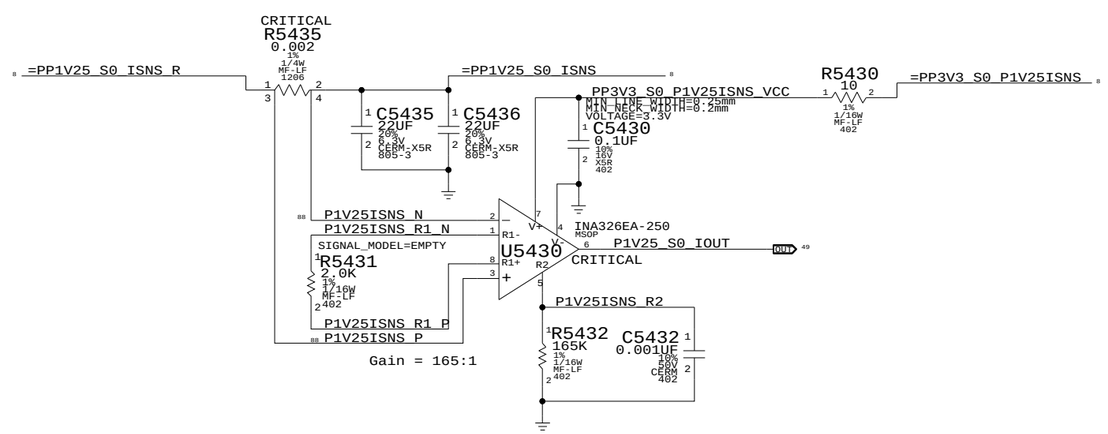
SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 49 OF 89	

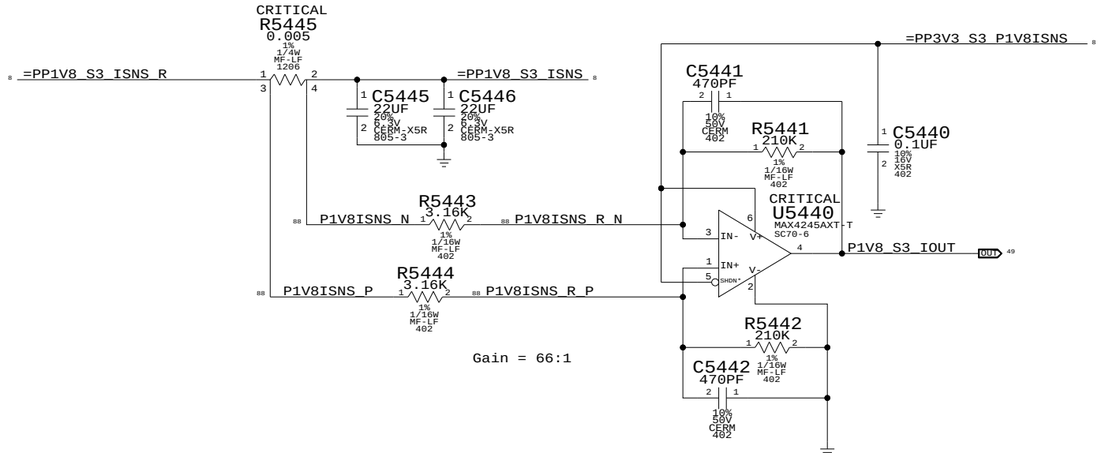
GPU VCore Current Sense

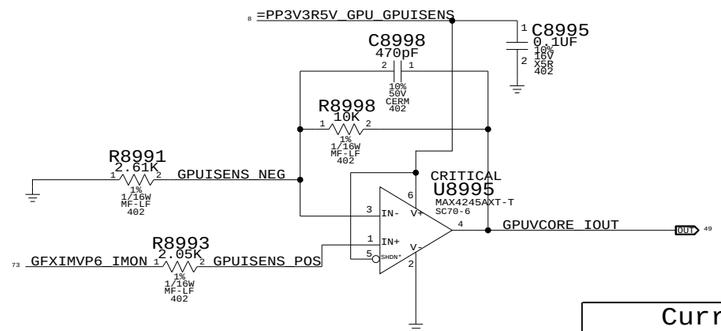












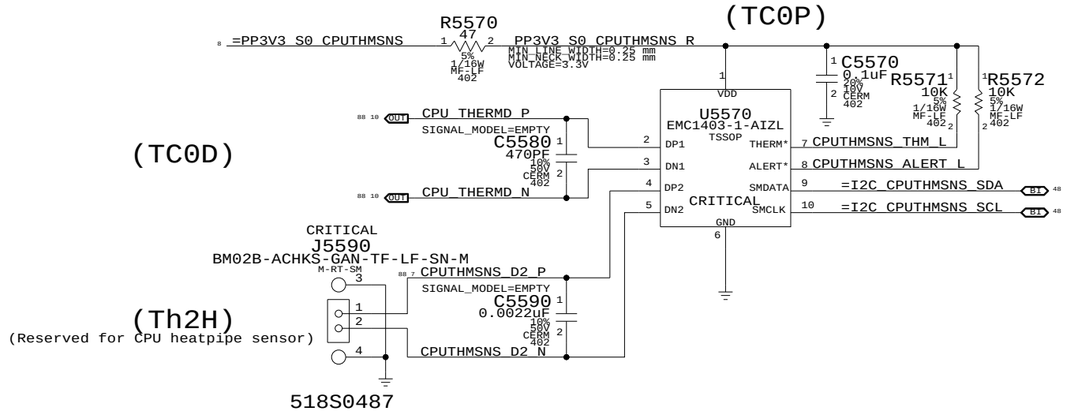
Current Sensing

SYNC_MASTER=M87_MLB SYNC_DATE=05/22/2007

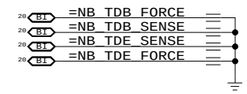
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 50 OF 89	

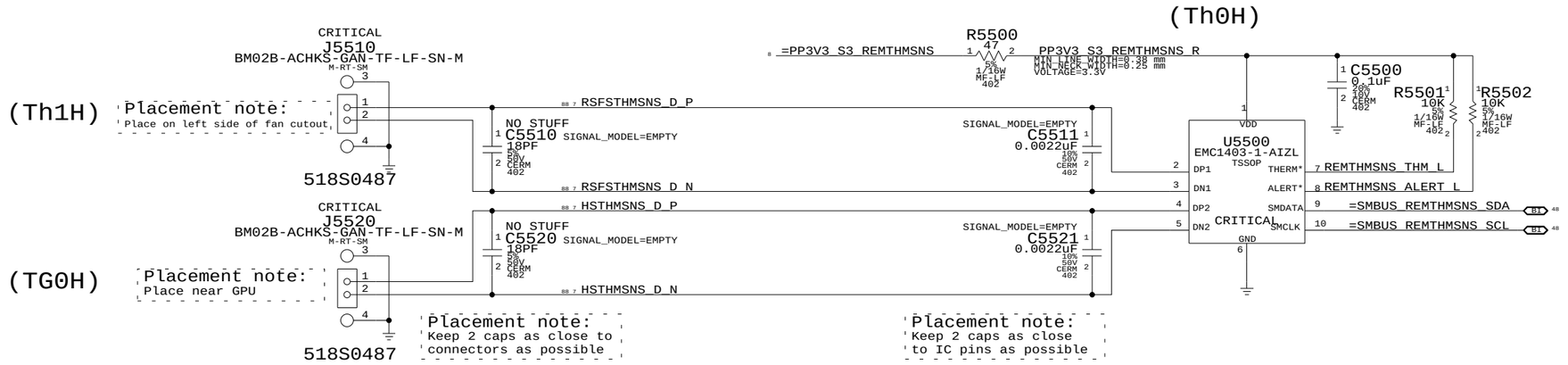
CPU T-Diode Thermal Sensor



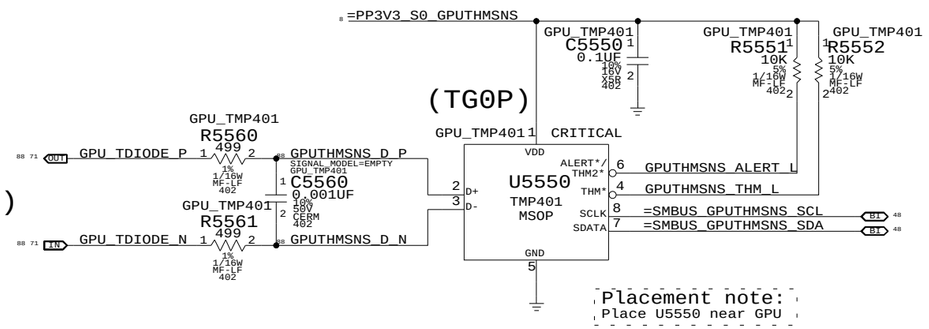
NB Thermal Diodes Not Used



GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



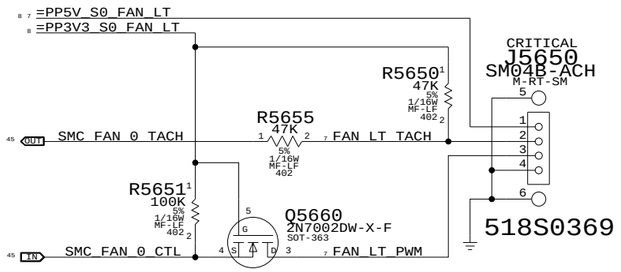
Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

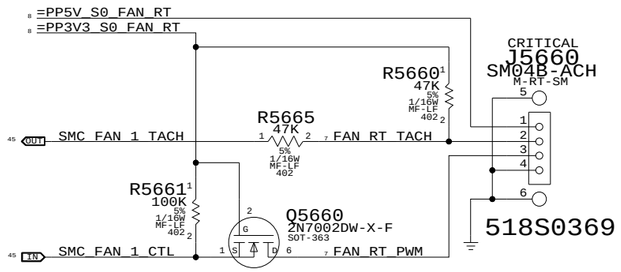
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 51 OF 89	

Left Fan



Right Fan



Fan Connectors

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

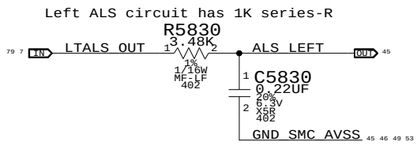
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

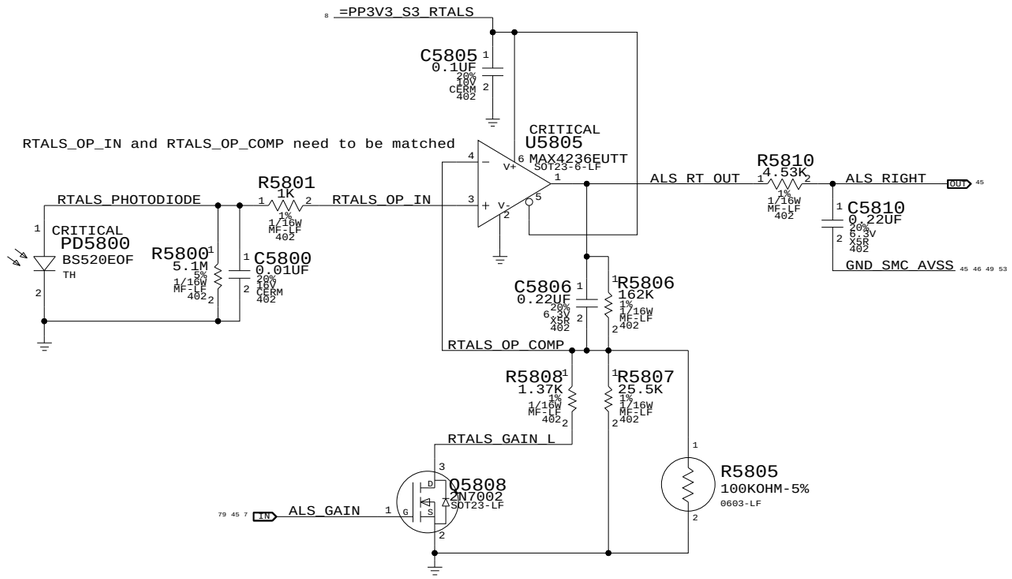
SCALE	SHT	OF
NONE	52	89

Left ALS Filter

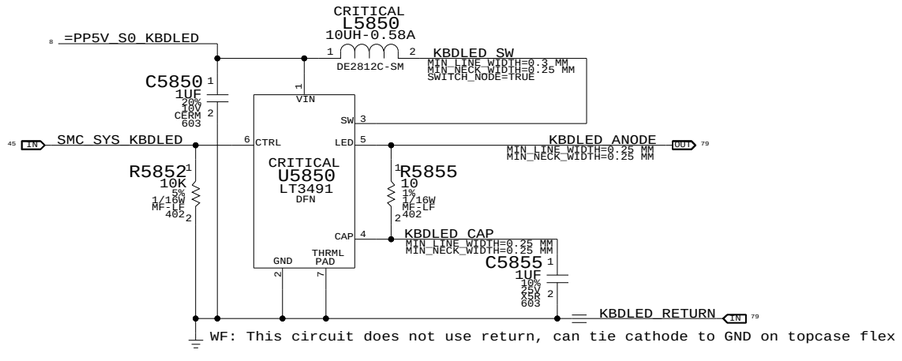
Left ALS circuit has 1K series-R



Right ALS Circuit



Keyboard LED Driver

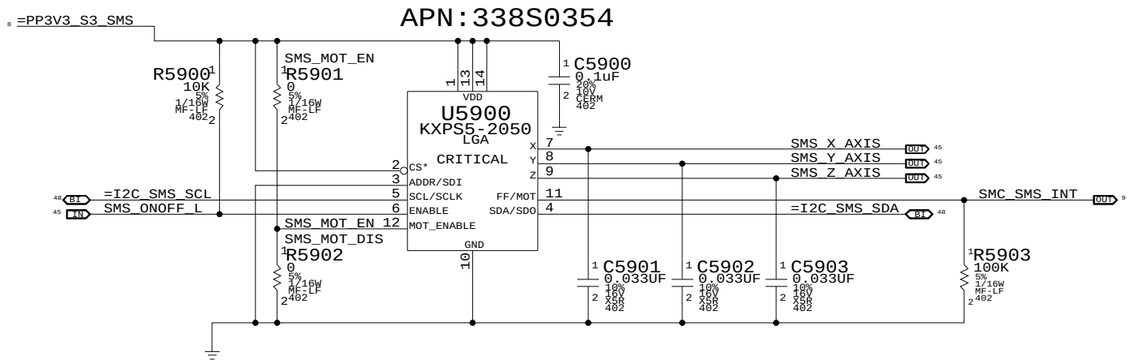


ALS Support

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 53 OF 89	

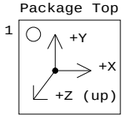


I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

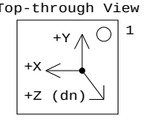
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



Sudden Motion Sensor (SMS)

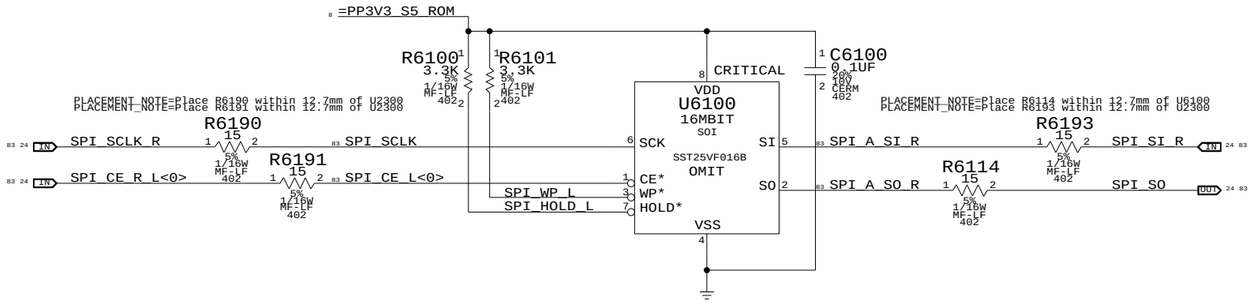
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE: NONE

SHT 54 OF 89



SPI BootROM

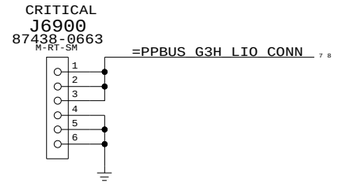
SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

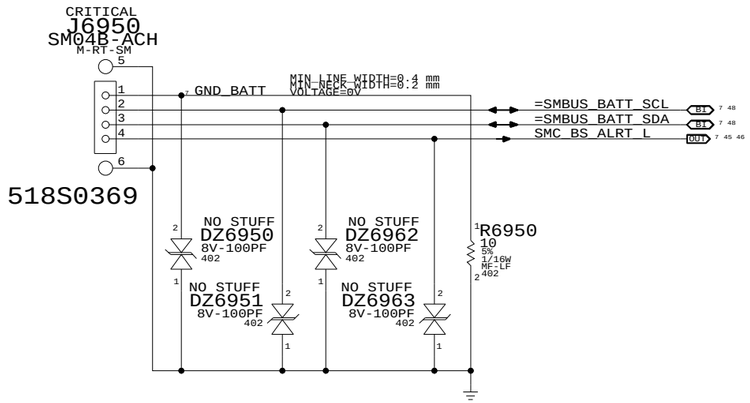
SCALE	SHT	OF
NONE	55	89

Left I/O Power Connector



518S0458

Battery Connector (Digital Signals)



518S0369

PBus-In & Battery Connectors

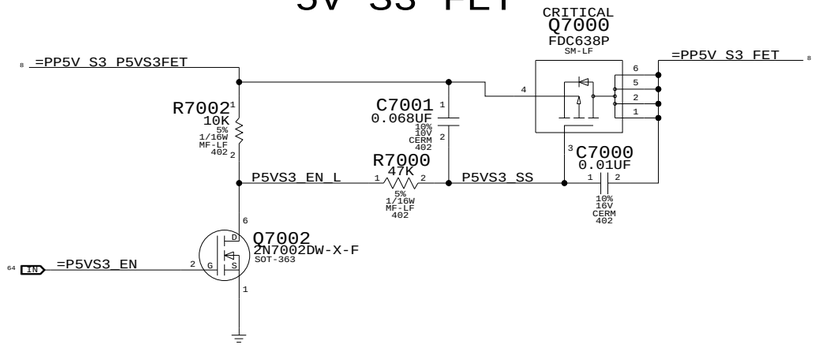
SYNC_MASTER=(M59_SYNC) SYNC_DATE=09/09/2006

APPLE INC.

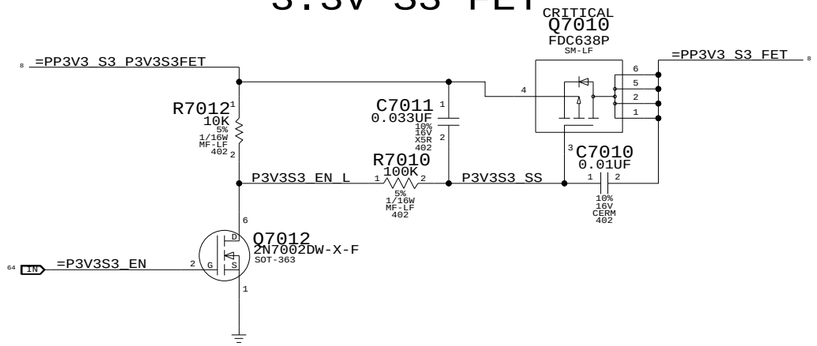
SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	56	89

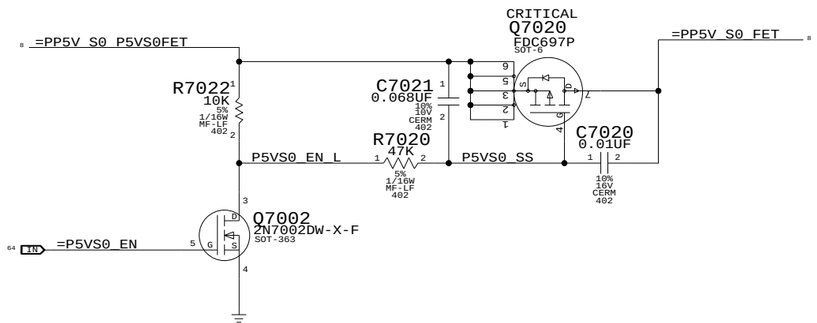
5V S3 FET



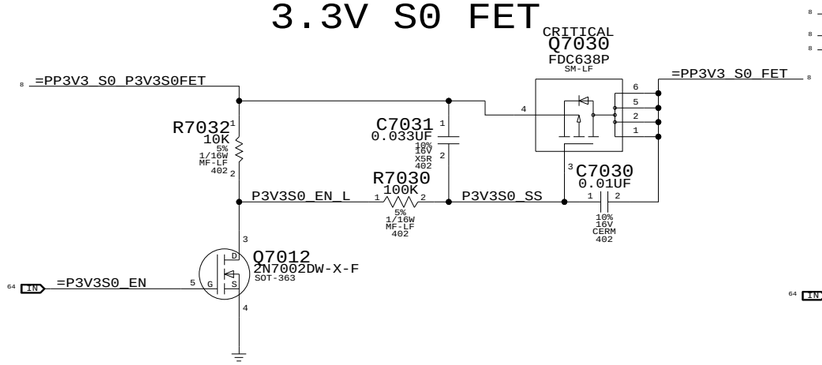
3.3V S3 FET



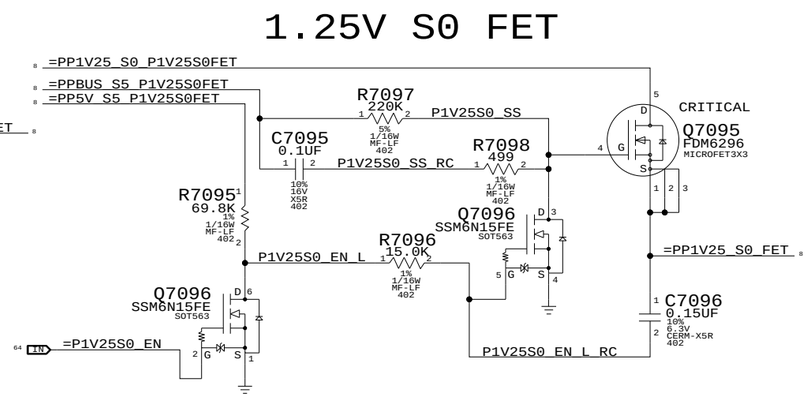
5V S0 FET



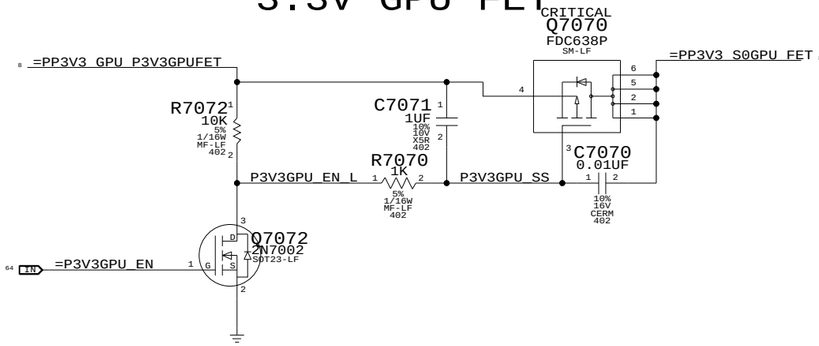
3.3V S0 FET



1.25V S0 FET



3.3V GPU FET



Power FETs

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	57	89

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

These caps are for Q7100

These caps are for Q7102

Place R7131 Between L7100,L7101 and CPU

LAYOUT NOTE:
Place R7126 in hot spot of reg circuit.

IMVP6_VSEN_P	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_BOOT1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_UGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_LGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_ISEN1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_VSUM1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_VO1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_VSEN_P	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM

IMVP6_PHASE2	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_BOOT2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_UGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_LGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_ISEN2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_VSUM2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_VO2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_VSEN_N	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM

IMVP6_OCSET	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_VO	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_DROOP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_DFB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_SOFT	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_RBIAS	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_VDIFF	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_FB2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_FB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_COMP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_VW	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=M76_MLB SYNC_DATE=01/23/2007

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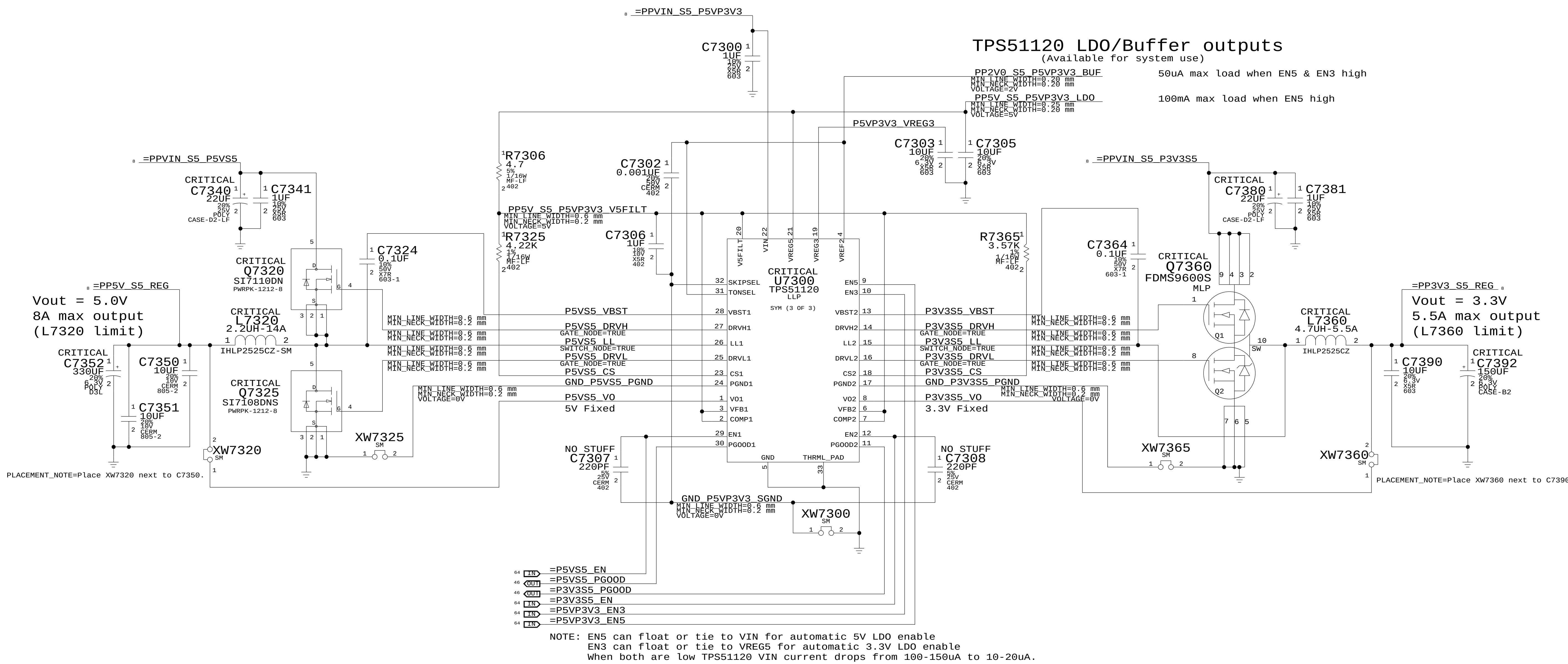
SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 58 OF 89	



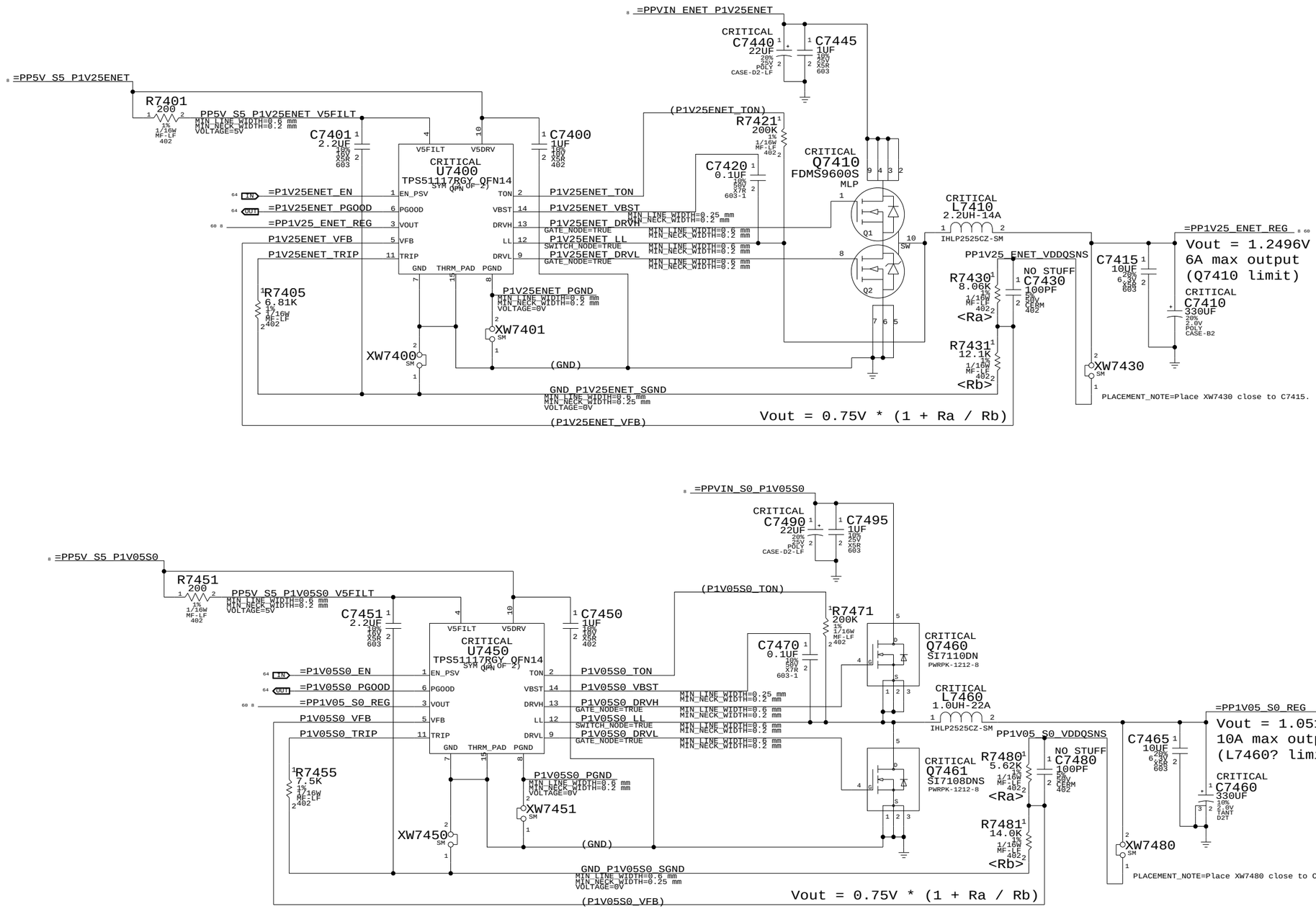
5V / 3.3V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE NONE	SHT 59 OF 89	

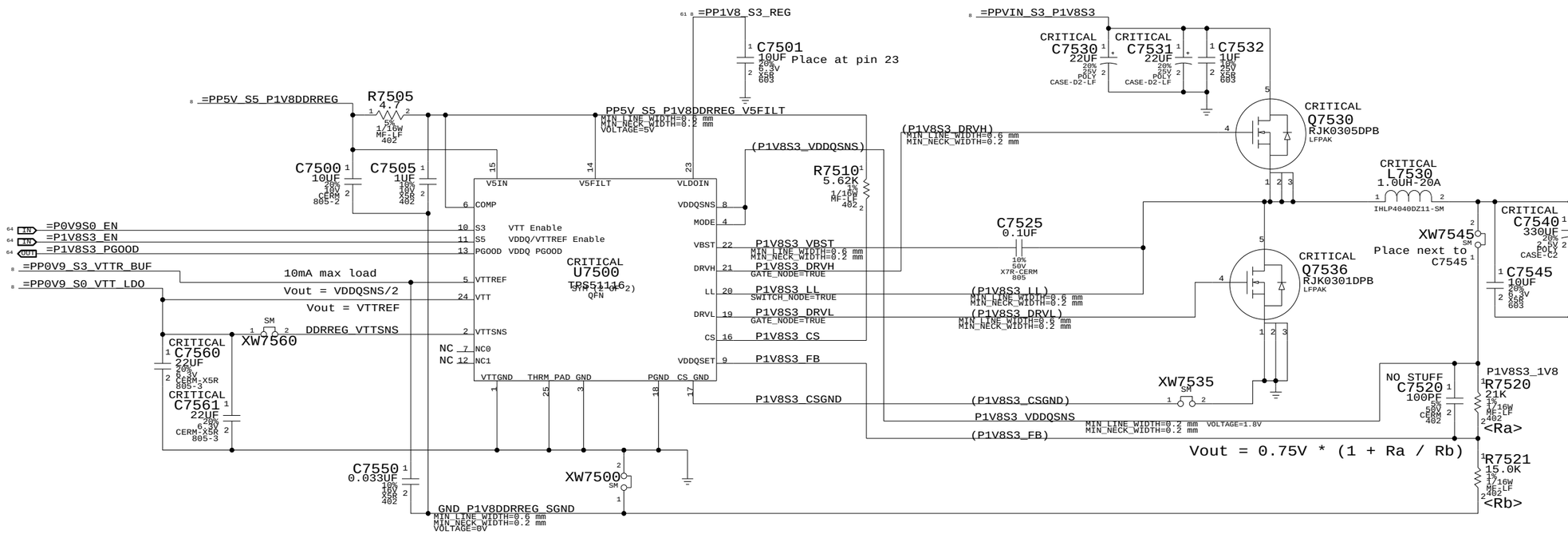


1.25V / 1.05V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 60 OF 89	



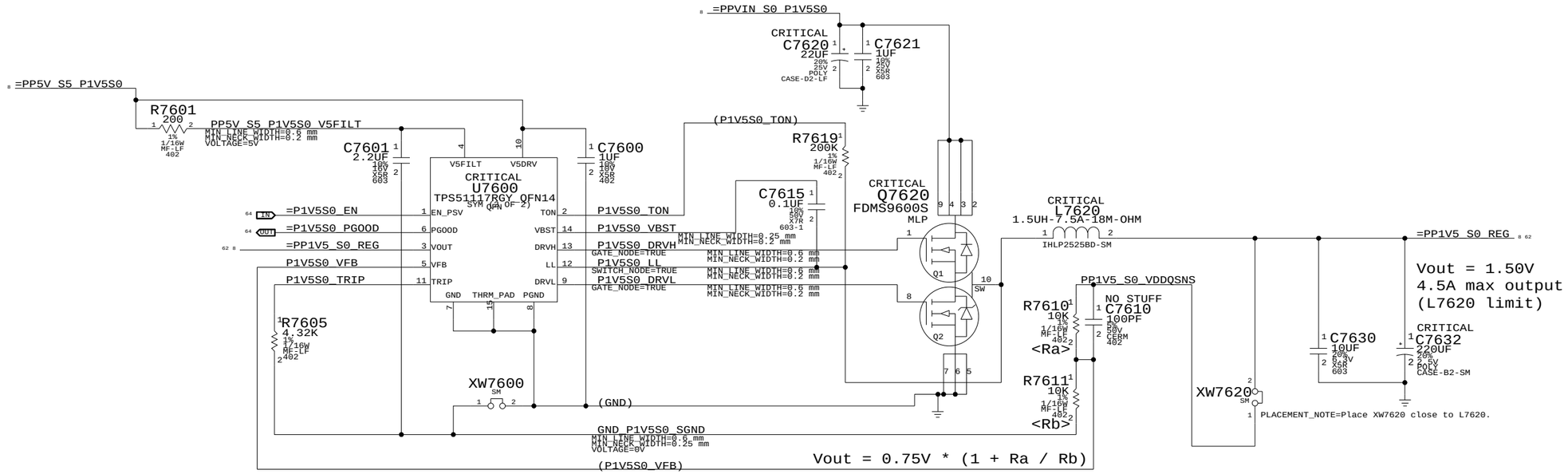
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0346	1	RES,MTL FILM,21.5K,1%,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V825

1.8V DDR2 Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 61 OF 89	



1.5V Power Supply

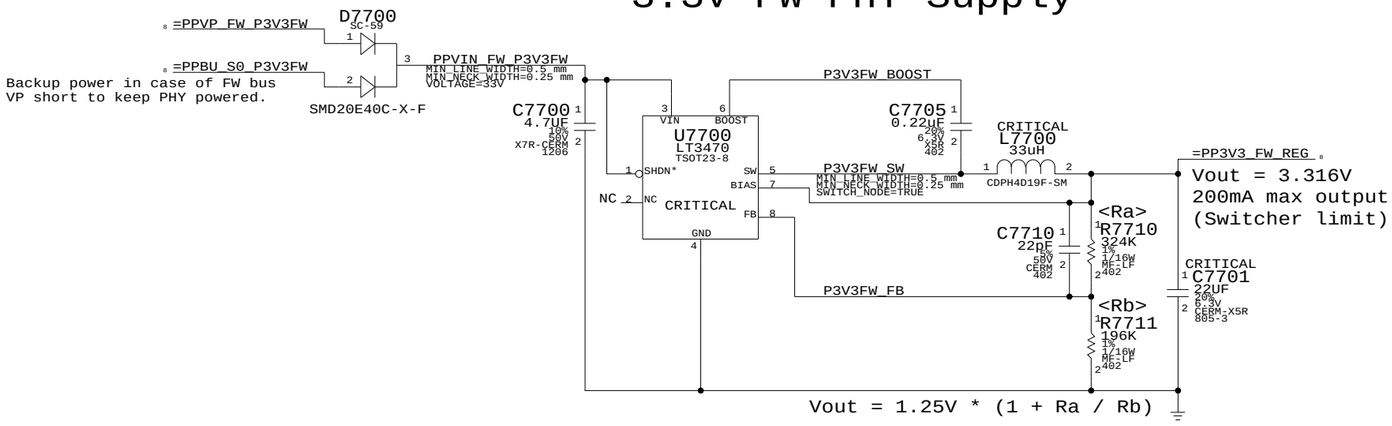
SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

NOTICE OF PROPRIETARY PROPERTY

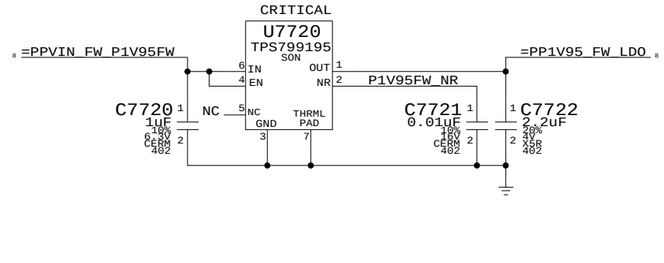
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 62 OF 89	

3.3V FW PHY Supply



1.95V FW PHY Supply



FW PHY Power Supplies

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	63	89

Power Control Signals

=PP5V_S5_PWRCTL

=PP3V3_GPU_PWRCTL

G84M GPU requires rails to come up in the following order:
1) 1.2V
2) 3.3V
3) Vcore
4) 1.8V

R7850 10K 5% 1/16W MF-LF 402

R7851 10K 5% 1/16W MF-LF 402

R7852 100K 5% 1/16W MF-LF 402

R7854 10K 5% 1/16W MF-LF 402

=GPUVCORE_PGOOD

Need to ensure that TPS51117 PGOOD does not deassert while GPU VIDs are changing GPU core voltage.

Q7850 2N7002DW-X-F SOT-363

Q7851 2N7002DW-X-F SOT-363

Q7851 2N7002DW-X-F SOT-363

PM_P1V8_S0GPU_EN (MAKE_BASE=TRUE) = =P1V8_S0GPU_EN

PM_GPUVCORE_EN (MAKE_BASE=TRUE) = =GPUVCORE_EN

PVCOREGPU_EN_L

C7851 0.1UF 20% 10V CERM 402

PM_SLP_S3_LS5V (MAKE_BASE=TRUE) = LIO_S0_EN_L

Q7850 2N7002DW-X-F SOT-363

PM_SLP_S3_L

(PM_SLP_S3_L) MAKE_BASE=TRUE

=PVCOREGPU_EN
=P5VS0_EN
=P3V3S0_EN
=P1V25S0_EN
=P0V9S0_EN
=PBUSVSENS_EN
=ENET_VMAIN_AVLBL
=PM_SLP_S3_DELAY_L

R7856 100K 5% 1/16W MF-LF 402

=PP3V3_S0_PWRCTL

=PP3V3_S5_PWRCTL

U7850 MC74VHC1G09 SC70

PM_SLP_S3_DELAY_L (MAKE_BASE=TRUE)

R7859 10K 5% 1/16W MF-LF 402

NO STUFF C7859 0.047UF 10% 16V CERM 402

=P1V5S0_EN

=P1V05S0_EN

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

=PPVIN_G3H_P3V42G3H

P3V42G3H5_BOOST

C7800 10UF 10% 16V CERM 1206-1

U7800 LT3470 TSOT23-8

SHDN*

NC CRITICAL

GND

C7805 0.22UF 20% 50V X5R 402

CRITICAL L7810 33UH CDPH4D19F-SM

P3V42G3H_SW (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, SWITCH_NODE=TRUE)

=PP3V42_G3H_REG

Vout = 3.425
200mA max output
(Switcher limit)

C7810 22pF 5% 50V CERM 402

<Ra> R7810 348K 1% 1/16W MF-LF 402

<Rb> R7811 200K 1% 1/16W MF-LF 402

C7815 22UF 20% 6.3V CERM-X5R 805-3

P3V42G3H_FB

Vout = 1.25V * (1 + Ra / Rb)

Unused PGOOD Signals

=P1V25ENET_PGOOD = TP_P1V25ENET_PGOOD (MAKE_BASE=TRUE)

=P1V8_S0GPU_PGOOD = TP_P1V8_S0GPU_PGOOD (MAKE_BASE=TRUE)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

PP1V25_S0_ISNS

=PP3V3_S3_PWRCTL

MAX6838 threshold is 93.5% @ 1.120V

R7860 154K 1% 1/16W MF-LF 402

U7860 MAX6838XSD0 SC70-4 (VCC, RESET-IN, RESET+, GND)

S0PGOOD_1V2_DIV

R7861 100K 1% 1/16W MF-LF 402

C7860 0.0047UF 10% 16V CERM 402

R7862 100K 5% 1/16W MF-LF 402

PM_P3V3GPU_EN (MAKE_BASE=TRUE) = =P3V3GPU_EN

=P1V25_PWRGD

IMVP6_IMON

To CPU IMVP6

ISL9504A

R7866 0 5% 1/16W MF-LF 402

=PP3V3_S0_ALLSYSPG

C7880 0.1UF 20% 16V CERM 402

=PP3V3_S5_P1V5P1V05PG

R7865 100K 5% 1/16W MF-LF 402

=P1V5S0_PGOOD

TPS51117 PGOOD threshold 92.5-97.5% (1.36 - 1.46V)

=P1V05S0_PGOOD

TPS51117 PGOOD threshold 92.5-97.5% (0.98 - 1.02V)

=P1V8S3_PGOOD

P1V8P1V5P1V05S0_PGOOD (MAKE_BASE=TRUE)

U7880 MC74VHC1G08 SC70

ALL_SYS_PWRGD

PM_ENET_EN

(PM_ENET_EN) MAKE_BASE=TRUE = =P1V25ENET_EN

PM_S4_STATE_L

(PM_S4_STATE_L) MAKE_BASE=TRUE

=P3V3S3_EN
=P5VS3_EN
=USB_EXTA_EN
LIO_S3_EN

R7857 10K 5% 1/16W MF-LF 402

R7855 10K 5% 1/16W MF-LF 402

P1V8S3_EN (MAKE_BASE=TRUE) = =P1V8S3_EN

C7855 0.47UF 10% 6.3V CERM-X5R 402

NOTE: 0.9V is not checked!

Other S0 Rails PWRGD Circuit

PP3V3GPU_EN IS A PROXY FOR 1.2V

PP5V_S0

PP3V3_S0

PP1V8_S0GPU_ISNS

=P1V25_PWRGD

C7872 0.1UF 20% 10V CERM 402

C7871 0.1UF 20% 10V CERM 402

C7870 0.1UF 20% 10V CERM 402

R7875 10K 5% 1/16W MF-LF 402

U7870 LTC2900 DFN (V1, V2, V3, V4, VREF, VPG, PBR*, RST*, GND, THRM_PAD)

NC

S0PGOOD_VREF

R7870 9.53K 1% 1/16W MF-LF 402

S0PGOOD_VPG

R7871 93.1K 1% 1/16W MF-LF 402

S0PGOOD_PWROK

S0PGOOD_CRT

C7875 0.047UF 10% 16V CERM 402

Trst = 4.6ms/nF
Trst = 216ms

LTC2900 typical threshold is 93.5% (4.675V, 3.086V, 1.685V,1.120V)

3.425V G3Hot Supply & Power Control	
SYNC_MASTER=M88	SYNC_DATE=08/02/2007

APPLE INC.

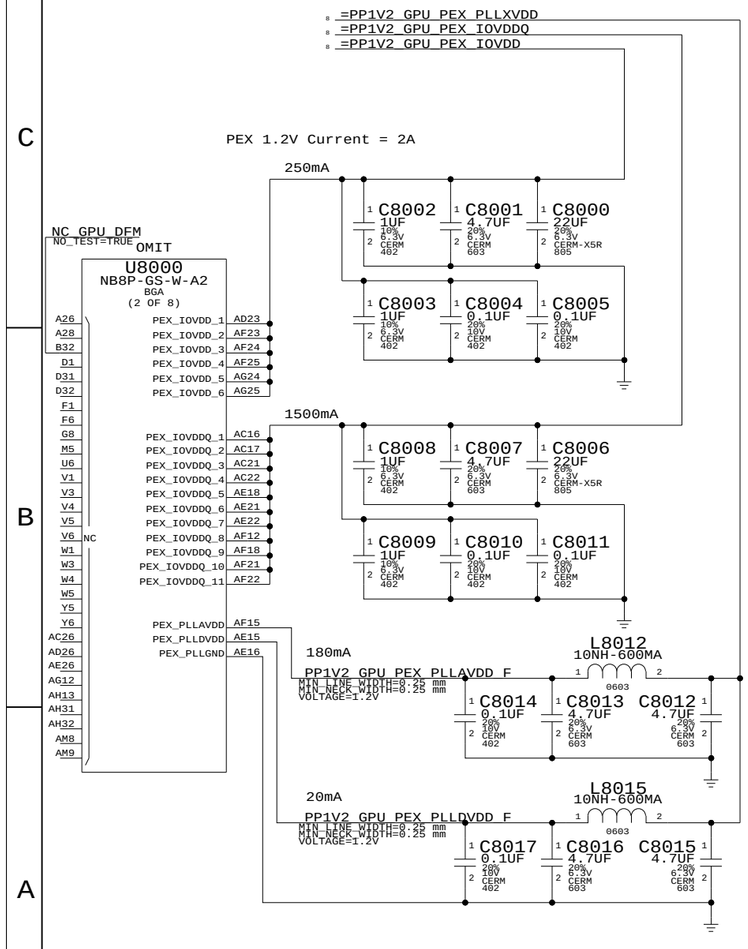
SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 64 OF 89	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



OMIT
U8000
NB8P-GS-W-A2
BGA
(1 OF 8)

PCI-EXPRESS BUS INTERFACE

PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AK13	PEX_RX0	PEX_TX0	AJ15	PEG_D2R_C_P<0>	C8055 0.1uF	PEG_D2R_P<0>
PEG_R2D_C_N<0>	C8021 0.1uF	PEG_R2D_N<0>	AK14	PEX_RX0_L	PEX_TX0_L	AK15	PEG_D2R_C_N<0>	C8056 0.1uF	PEG_D2R_N<0>
PEG_R2D_C_P<1>	C8022 0.1uF	PEG_R2D_P<1>	AM14	PEX_RX1	PEX_TX1	AH16	PEG_D2R_C_P<1>	C8057 0.1uF	PEG_D2R_P<1>
PEG_R2D_C_N<1>	C8023 0.1uF	PEG_R2D_N<1>	AM15	PEX_RX1_L	PEX_TX1_L	AG16	PEG_D2R_C_N<1>	C8058 0.1uF	PEG_D2R_N<1>
PEG_R2D_C_P<2>	C8024 0.1uF	PEG_R2D_P<2>	AL15	PEX_RX2	PEX_TX2	AG17	PEG_D2R_C_P<2>	C8059 0.1uF	PEG_D2R_P<2>
PEG_R2D_C_N<2>	C8025 0.1uF	PEG_R2D_N<2>	AL16	PEX_RX2_L	PEX_TX2_L	AH17	PEG_D2R_C_N<2>	C8060 0.1uF	PEG_D2R_N<2>
PEG_R2D_C_P<3>	C8026 0.1uF	PEG_R2D_P<3>	AK16	PEX_RX3	PEX_TX3	AG18	PEG_D2R_C_P<3>	C8061 0.1uF	PEG_D2R_P<3>
PEG_R2D_C_N<3>	C8027 0.1uF	PEG_R2D_N<3>	AK17	PEX_RX3_L	PEX_TX3_L	AH18	PEG_D2R_C_N<3>	C8062 0.1uF	PEG_D2R_N<3>
PEG_R2D_C_P<4>	C8028 0.1uF	PEG_R2D_P<4>	AL17	PEX_RX4	PEX_TX4	AK18	PEG_D2R_C_P<4>	C8063 0.1uF	PEG_D2R_P<4>
PEG_R2D_C_N<4>	C8029 0.1uF	PEG_R2D_N<4>	AL18	PEX_RX4_L	PEX_TX4_L	AJ18	PEG_D2R_C_N<4>	C8064 0.1uF	PEG_D2R_N<4>
PEG_R2D_C_P<5>	C8030 0.1uF	PEG_R2D_P<5>	AM18	PEX_RX5	PEX_TX5	AJ19	PEG_D2R_C_P<5>	C8065 0.1uF	PEG_D2R_P<5>
PEG_R2D_C_N<5>	C8031 0.1uF	PEG_R2D_N<5>	AM19	PEX_RX5_L	PEX_TX5_L	AH19	PEG_D2R_C_N<5>	C8066 0.1uF	PEG_D2R_N<5>
PEG_R2D_C_P<6>	C8032 0.1uF	PEG_R2D_P<6>	AK19	PEX_RX6	PEX_TX6	AG20	PEG_D2R_C_P<6>	C8067 0.1uF	PEG_D2R_P<6>
PEG_R2D_C_N<6>	C8033 0.1uF	PEG_R2D_N<6>	AK20	PEX_RX6_L	PEX_TX6_L	AH20	PEG_D2R_C_N<6>	C8068 0.1uF	PEG_D2R_N<6>
PEG_R2D_C_P<7>	C8034 0.1uF	PEG_R2D_P<7>	AL20	PEX_RX7	PEX_TX7	AG21	PEG_D2R_C_P<7>	C8069 0.1uF	PEG_D2R_P<7>
PEG_R2D_C_N<7>	C8035 0.1uF	PEG_R2D_N<7>	AL21	PEX_RX7_L	PEX_TX7_L	AH21	PEG_D2R_C_N<7>	C8070 0.1uF	PEG_D2R_N<7>
PEG_R2D_C_P<8>	C8036 0.1uF	PEG_R2D_P<8>	AM21	PEX_RX8	PEX_TX8	AK21	PEG_D2R_C_P<8>	C8071 0.1uF	PEG_D2R_P<8>
PEG_R2D_C_N<8>	C8037 0.1uF	PEG_R2D_N<8>	AM22	PEX_RX8_L	PEX_TX8_L	AJ21	PEG_D2R_C_N<8>	C8072 0.1uF	PEG_D2R_N<8>
PEG_R2D_C_P<9>	C8038 0.1uF	PEG_R2D_P<9>	AK22	PEX_RX9	PEX_TX9	AJ22	PEG_D2R_C_P<9>	C8073 0.1uF	PEG_D2R_P<9>
PEG_R2D_C_N<9>	C8039 0.1uF	PEG_R2D_N<9>	AK23	PEX_RX9_L	PEX_TX9_L	AH22	PEG_D2R_C_N<9>	C8074 0.1uF	PEG_D2R_N<9>
PEG_R2D_C_P<10>	C8040 0.1uF	PEG_R2D_P<10>	AL23	PEX_RX10	PEX_TX10	AG23	PEG_D2R_C_P<10>	C8075 0.1uF	PEG_D2R_P<10>
PEG_R2D_C_N<10>	C8041 0.1uF	PEG_R2D_N<10>	AL24	PEX_RX10_L	PEX_TX10_L	AH23	PEG_D2R_C_N<10>	C8076 0.1uF	PEG_D2R_N<10>
PEG_R2D_C_P<11>	C8042 0.1uF	PEG_R2D_P<11>	AM24	PEX_RX11	PEX_TX11	AK24	PEG_D2R_C_P<11>	C8077 0.1uF	PEG_D2R_P<11>
PEG_R2D_C_N<11>	C8043 0.1uF	PEG_R2D_N<11>	AM25	PEX_RX11_L	PEX_TX11_L	AJ24	PEG_D2R_C_N<11>	C8078 0.1uF	PEG_D2R_N<11>
PEG_R2D_C_P<12>	C8044 0.1uF	PEG_R2D_P<12>	AK25	PEX_RX12	PEX_TX12	AJ25	PEG_D2R_C_P<12>	C8079 0.1uF	PEG_D2R_P<12>
PEG_R2D_C_N<12>	C8045 0.1uF	PEG_R2D_N<12>	AK26	PEX_RX12_L	PEX_TX12_L	AH25	PEG_D2R_C_N<12>	C8080 0.1uF	PEG_D2R_N<12>
PEG_R2D_C_P<13>	C8046 0.1uF	PEG_R2D_P<13>	AL26	PEX_RX13	PEX_TX13	AH26	PEG_D2R_C_P<13>	C8081 0.1uF	PEG_D2R_P<13>
PEG_R2D_C_N<13>	C8047 0.1uF	PEG_R2D_N<13>	AL27	PEX_RX13_L	PEX_TX13_L	AG26	PEG_D2R_C_N<13>	C8082 0.1uF	PEG_D2R_N<13>
PEG_R2D_C_P<14>	C8048 0.1uF	PEG_R2D_P<14>	AM27	PEX_RX14	PEX_TX14	AK27	PEG_D2R_C_P<14>	C8083 0.1uF	PEG_D2R_P<14>
PEG_R2D_C_N<14>	C8049 0.1uF	PEG_R2D_N<14>	AM28	PEX_RX14_L	PEX_TX14_L	AJ27	PEG_D2R_C_N<14>	C8084 0.1uF	PEG_D2R_N<14>
PEG_R2D_C_P<15>	C8050 0.1uF	PEG_R2D_P<15>	AL28	PEX_RX15	PEX_TX15	AJ28	PEG_D2R_C_P<15>	C8085 0.1uF	PEG_D2R_P<15>
PEG_R2D_C_N<15>	C8051 0.1uF	PEG_R2D_N<15>	AL29	PEX_RX15_L	PEX_TX15_L	AH27	PEG_D2R_C_N<15>	C8086 0.1uF	PEG_D2R_N<15>
PEG_CLK100M_GPU_P			AH14	PEX_REFCLK	PEX_TSTCLK_OUT	AM12	TP_GPU_PEXTSTCLK_P		
PEG_CLK100M_GPU_N			AJ14	PEX_REFCLK_L	PEX_TSTCLK_OUT_L	AM11	TP_GPU_PEXTSTCLK_N		
GPU_RESET_L			AH15	PEX_RST_L					

All 0.1uF capacitors: 10% 16V X5R 402

NV G84M PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	65	89

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 1UF 20% 10V 6.3V CERM 402
C8101 1UF 20% 10V 6.3V CERM 402
C8102 1UF 20% 10V 6.3V CERM 402
C8103 0.1UF 20% 10V CERM 402
C8104 0.1UF 20% 10V CERM 402
C8105 0.1UF 20% 10V CERM 402
C8106 0.1UF 20% 10V CERM 402
C8107 0.1UF 20% 10V CERM 402
C8108 0.1UF 20% 10V CERM 402
C8109 0.1UF 20% 10V CERM 402
C8110 0.1UF 20% 10V CERM 402
C8111 0.1UF 20% 10V CERM 402
C8112 0.1UF 20% 10V CERM 402
C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
C8115 0.1UF 20% 10V CERM 402
C8116 0.1UF 20% 10V CERM 402
C8117 0.1UF 20% 10V CERM 402
C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

OMIT
U8000
NB8P-GS-W-A2
BGA
(7 OF 8)

K16 K17 N13 N14 N16 N17 N19 P13 P14 P16 P17 P19 R16 R17 T13 T14 T15 T18 T19 U13 U14 U15 U18 U19 V16 V17 W13 W14 W16 W17 W19 Y13 Y14 Y16 Y17 Y19 Y20 → VDD

P20 T20 T23 U20 U23 W20 → VDD_LP

TP_GPU_VDD_SENSE N20 → VDD_SENSE
TP_GPU_GND_SENSE M21 → GND_SENSE

A12 A18 A21 A24 A27 A3 A30 A6 A9 AA32 AD32 AG32 AK32 C32 F32 J32 M32 R32 → FBVDD

AA25 AA26 AB25 AB26 G11 G12 G15 G18 G21 G22 H11 H12 H15 H18 H21 H22 L25 L26 M25 M26 R25 R26 V25 V26 → FBVDDQ

AA23 AB23 H16 H17 J10 J23 J24 J9 K11 K12 K21 K22 K24 K9 L23 M23 T25 U25 → NC

=PP1V8_GPU_FBVDDQ

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603
C8156 0.1UF 20% 10V CERM 402
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402
C8162 0.1UF 20% 10V CERM 402
C8163 0.1UF 20% 10V CERM 402
C8164 0.1UF 20% 10V CERM 402
C8165 0.1UF 20% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402
C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

OMIT
U8000
NB8P-GS-W-A2
BGA
(8 OF 8)

AE17 AE27 AE6 AF11 AF26 AF29 AF4 AF7 AG10 AG11 AB27 AB6 AC10 AC23 AC29 AC4 AD16 AD17 AD2 AD31 AA12 AA2 AA21 AA31 AG13 AG14 AG15 AG19 AG2 AG22 AG31 AG8 AH24 AJ10 AJ13 AJ16 AJ17 AJ20 AJ23 AJ26 AJ29 AJ4 AJ7 AK2 AK28 AK31 AL10 AL11 AL14 AL19 AL22 AL25 AL3 AL6 AL9 AM10 AM13 AM16 AM17 AM20 AM23 AM26 AM29 B12 B15 B18 B21 B24 B27 B3 B30 B6 B9 C2 C31 D10 D13 → GND

D16 D17 D20 D23 D26 D29 D4 D7 F11 F14 F19 F2 F22 F25 F31 F8 G26 G29 G4 G7 H27 H6 J16 J17 J2 J31 K10 K23 K29 K4 L27 L6 M12 M2 M31 N15 N18 N29 N4 P15 P18 P27 P6 R13 R14 R15 R18 R19 R2 R20 R31 T16 T17 T24 T29 T4 U16 U17 U24 U29 U8 V13 V14 V15 V18 V19 V2 V20 V31 W15 W18 W27 W6 Y15 Y18 Y29 Y4 → GND

NV G84M Core/FB Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 66 OF 89	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8000
NB8P-GS-W-A2
BGA
(3 OF 8)

MEMORY INTERFACE A

FB_A_DQ<0> N27 FBAD0
FB_A_DQ<1> M27 FBAD1
FB_A_DQ<2> N28 FBAD2
FB_A_DQ<3> L29 FBAD3
FB_A_DQ<4> K27 FBAD4
FB_A_DQ<5> K28 FBAD5
FB_A_DQ<6> J29 FBAD6
FB_A_DQ<7> J28 FBAD7
FB_A_DQ<8> P30 FBAD8
FB_A_DQ<9> N31 FBAD9
FB_A_DQ<10> N30 FBAD10
FB_A_DQ<11> N32 FBAD11
FB_A_DQ<12> L31 FBAD12
FB_A_DQ<13> L30 FBAD13
FB_A_DQ<14> J30 FBAD14
FB_A_DQ<15> L32 FBAD15
FB_A_DQ<16> H30 FBAD16
FB_A_DQ<17> K30 FBAD17
FB_A_DQ<18> H31 FBAD18
FB_A_DQ<19> F30 FBAD19
FB_A_DQ<20> H32 FBAD20
FB_A_DQ<21> E31 FBAD21
FB_A_DQ<22> D30 FBAD22
FB_A_DQ<23> E30 FBAD23
FB_A_DQ<24> H28 FBAD24
FB_A_DQ<25> H29 FBAD25
FB_A_DQ<26> E29 FBAD26
FB_A_DQ<27> J27 FBAD27
FB_A_DQ<28> F27 FBAD28
FB_A_DQ<29> E27 FBAD29
FB_A_DQ<30> E28 FBAD30
FB_A_DQ<31> F28 FBAD31
FB_A_DQ<32> AD29 FBAD32
FB_A_DQ<33> AE29 FBAD33
FB_A_DQ<34> AD28 FBAD34
FB_A_DQ<35> AC28 FBAD35
FB_A_DQ<36> AB29 FBAD36
FB_A_DQ<37> AA30 FBAD37
FB_A_DQ<38> Y28 FBAD38
FB_A_DQ<39> AB30 FBAD39
FB_A_DQ<40> AM30 FBAD40
FB_A_DQ<41> AF30 FBAD41
FB_A_DQ<42> AJ31 FBAD42
FB_A_DQ<43> AJ30 FBAD43
FB_A_DQ<44> AJ32 FBAD44
FB_A_DQ<45> AK29 FBAD45
FB_A_DQ<46> AM31 FBAD46
FB_A_DQ<47> AL30 FBAD47
FB_A_DQ<48> AE32 FBAD48
FB_A_DQ<49> AE30 FBAD49
FB_A_DQ<50> AE31 FBAD50
FB_A_DQ<51> AD30 FBAD51
FB_A_DQ<52> AC31 FBAD52
FB_A_DQ<53> AC32 FBAD53
FB_A_DQ<54> AB32 FBAD54
FB_A_DQ<55> AB31 FBAD55
FB_A_DQ<56> AG27 FBAD56
FB_A_DQ<57> AF28 FBAD57
FB_A_DQ<58> AH28 FBAD58
FB_A_DQ<59> AG28 FBAD59
FB_A_DQ<60> AG29 FBAD60
FB_A_DQ<61> AD27 FBAD61
FB_A_DQ<62> AF27 FBAD62
FB_A_DQ<63> AE28 FBAD63

FBA_CMD0 P32 FB_A_LMA<4>
FBA_CMD1 U27 FB_A_RAS_L
FBA_CMD2 P31 FB_A_LMA<5>
FBA_CMD3 U30 FB_A_BA<1>
FBA_CMD4 Y31 FB_A_UMA<2>
FBA_CMD5 W32 FB_A_UMA<4>
FBA_CMD6 W31 FB_A_UMA<3>
FBA_CMD7 T32 FB_A_CS1_L
FBA_CMD8 V27 FB_A_CS0_L
FBA_CMD9 T28 FB_A_MA<11>
FBA_CMD10 T31 FB_A_CAS_L
FBA_CMD11 U32 FB_A_WE_L
FBA_CMD12 W29 FB_A_BA<0>
FBA_CMD13 W30 FB_A_UMA<5>
FBA_CMD14 T27 FB_A_MA<12>
FBA_CMD15 V28 FB_A_DRAM_RST
FBA_CMD16 V30 FB_A_MA<7>
FBA_CMD17 U31 FB_A_MA<10>
FBA_CMD18 R27 FB_A_CKE
FBA_CMD19 V29 FB_A_MA<0>
FBA_CMD20 T30 FB_A_MA<9>
FBA_CMD21 W28 FB_A_MA<6>
FBA_CMD22 R29 FB_A_LMA<2>
FBA_CMD23 R30 FB_A_MA<8>
FBA_CMD24 P29 FB_A_LMA<3>
FBA_CMD25 U28 FB_A_MA<1>
FBA_CMD26 Y32 FB_A_MA<13>
FBA_CMD27 Y30 FB_A_BA<2>
FBA_CMD28 V32 TP_FBA_CMD28

FBA_CLK0 P28 FB_A_CLK_P<0>
FBA_CLK0_L R28 FB_A_CLK_N<0>
FBA_CLK1 Y27 FB_A_CLK_P<1>
FBA_CLK1_L AA27 FB_A_CLK_N<1>

FBADQM0 M29 FB_A_DQM_L<0>
FBADQM1 M30 FB_A_DQM_L<1>
FBADQM2 G30 FB_A_DQM_L<2>
FBADQM3 F29 FB_A_DQM_L<3>
FBADQM4 AA29 FB_A_DQM_L<4>
FBADQM5 AK30 FB_A_DQM_L<5>
FBADQM6 AC30 FB_A_DQM_L<6>
FBADQM7 AG30 FB_A_DQM_L<7>

READ STROBE
FBADQS_RN0 M28 FB_A_RDQS<0>
FBADQS_RN1 K32 FB_A_RDQS<1>
FBADQS_RN2 G31 FB_A_RDQS<2>
FBADQS_RN3 G27 FB_A_RDQS<3>
FBADQS_RN4 AA28 FB_A_RDQS<4>
FBADQS_RN5 AL31 FB_A_RDQS<5>
FBADQS_RN6 AF31 FB_A_RDQS<6>
FBADQS_RN7 AH29 FB_A_RDQS<7>

WRITE STROBE
FBADQS_WP0 L28 FB_A_WDQS<0>
FBADQS_WP1 K31 FB_A_WDQS<1>
FBADQS_WP2 G32 FB_A_WDQS<2>
FBADQS_WP3 G28 FB_A_WDQS<3>
FBADQS_WP4 AB28 FB_A_WDQS<4>
FBADQS_WP5 AL32 FB_A_WDQS<5>
FBADQS_WP6 AF32 FB_A_WDQS<6>
FBADQS_WP7 AH30 FB_A_WDQS<7>

=PP1V8_GPU_FBIO
FBA_DEBUG AC27 TP_FBA_DEBUG

PP1V2_GPU_FBA_PLL_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V
FBA_PLLAVDD G25
FBA_PLLGND G24

FBCAL_PD_VDDQ K26
FBCAL_PU_GND H26

R8200 10K 5% 1/16W MF-LF 402
R8201 10K 5% 1/16W MF-LF 402
R8290 45.3 1% 1/16W MF-LF 402
R8291 24.9 1% 1/16W MF-LF 402

=PP1V2_GPU_FBPLLAVDD
L8200 FERR-220-OHM 0402
C8201 0.1UF 20% 10V CERM 402
C8200 4.7UF 20% 6.3V CERM 603

OMIT
U8000
NB8P-GS-W-A2
BGA
(4 OF 8)

MEMORY INTERFACE B

FB_B_DQ<0> B7 FBCD0
FB_B_DQ<1> A7 FBCD1
FB_B_DQ<2> C7 FBCD2
FB_B_DQ<3> A2 FBCD3
FB_B_DQ<4> B2 FBCD4
FB_B_DQ<5> C4 FBCD5
FB_B_DQ<6> A5 FBCD6
FB_B_DQ<7> B5 FBCD7
FB_B_DQ<8> F9 FBCD8
FB_B_DQ<9> F10 FBCD9
FB_B_DQ<10> D12 FBCD10
FB_B_DQ<11> D9 FBCD11
FB_B_DQ<12> E12 FBCD12
FB_B_DQ<13> D11 FBCD13
FB_B_DQ<14> E8 FBCD14
FB_B_DQ<15> D8 FBCD15
FB_B_DQ<16> E7 FBCD16
FB_B_DQ<17> F7 FBCD17
FB_B_DQ<18> D6 FBCD18
FB_B_DQ<19> D5 FBCD19
FB_B_DQ<20> D3 FBCD20
FB_B_DQ<21> E4 FBCD21
FB_B_DQ<22> C3 FBCD22
FB_B_DQ<23> B4 FBCD23
FB_B_DQ<24> C10 FBCD24
FB_B_DQ<25> B10 FBCD25
FB_B_DQ<26> C8 FBCD26
FB_B_DQ<27> A10 FBCD27
FB_B_DQ<28> C11 FBCD28
FB_B_DQ<29> C12 FBCD29
FB_B_DQ<30> A11 FBCD30
FB_B_DQ<31> B11 FBCD31
FB_B_DQ<32> B28 FBCD32
FB_B_DQ<33> C27 FBCD33
FB_B_DQ<34> C26 FBCD34
FB_B_DQ<35> B26 FBCD35
FB_B_DQ<36> C30 FBCD36
FB_B_DQ<37> B31 FBCD37
FB_B_DQ<38> C29 FBCD38
FB_B_DQ<39> A31 FBCD39
FB_B_DQ<40> D28 FBCD40
FB_B_DQ<41> D27 FBCD41
FB_B_DQ<42> F26 FBCD42
FB_B_DQ<43> D24 FBCD43
FB_B_DQ<44> E23 FBCD44
FB_B_DQ<45> E26 FBCD45
FB_B_DQ<46> E24 FBCD46
FB_B_DQ<47> F23 FBCD47
FB_B_DQ<48> B23 FBCD48
FB_B_DQ<49> A23 FBCD49
FB_B_DQ<50> C25 FBCD50
FB_B_DQ<51> C23 FBCD51
FB_B_DQ<52> A22 FBCD52
FB_B_DQ<53> C22 FBCD53
FB_B_DQ<54> C21 FBCD54
FB_B_DQ<55> B22 FBCD55
FB_B_DQ<56> E22 FBCD56
FB_B_DQ<57> D22 FBCD57
FB_B_DQ<58> D21 FBCD58
FB_B_DQ<59> E21 FBCD59
FB_B_DQ<60> E18 FBCD60
FB_B_DQ<61> D19 FBCD61
FB_B_DQ<62> D18 FBCD62
FB_B_DQ<63> E19 FBCD63

NC G10 FBC_PLLAVDD
NC G9 FBC_PLLGND

FBC_CMD0 C13 FB_B_LMA<4>
FBC_CMD1 A16 FB_B_RAS_L
FBC_CMD2 A13 FB_B_LMA<5>
FBC_CMD3 B17 FB_B_BA<1>
FBC_CMD4 B20 FB_B_UMA<2>
FBC_CMD5 A19 FB_B_UMA<4>
FBC_CMD6 B19 FB_B_UMA<3>
FBC_CMD7 B14 FB_B_CS1_L
FBC_CMD8 E16 FB_B_CS0_L
FBC_CMD9 A14 FB_B_MA<11>
FBC_CMD10 C15 FB_B_CAS_L
FBC_CMD11 B16 FB_B_WE_L
FBC_CMD12 F17 FB_B_BA<0>
FBC_CMD13 C19 FB_B_UMA<5>
FBC_CMD14 D15 FB_B_MA<12>
FBC_CMD15 C17 FB_B_DRAM_RST
FBC_CMD16 A17 FB_B_MA<7>
FBC_CMD17 C16 FB_B_MA<10>
FBC_CMD18 D14 FB_B_CKE
FBC_CMD19 F16 FB_B_MA<0>
FBC_CMD20 C14 FB_B_MA<9>
FBC_CMD21 C18 FB_B_MA<6>
FBC_CMD22 E14 FB_B_LMA<2>
FBC_CMD23 B13 FB_B_MA<8>
FBC_CMD24 E15 FB_B_LMA<3>
FBC_CMD25 F15 FB_B_MA<1>
FBC_CMD26 A20 FB_B_MA<13>
FBC_CMD27 C20 FB_B_BA<2>
FBC_CMD28 A15 TP_FBC_CMD28

FBC_CLK0 E13 FB_B_CLK_P<0>
FBC_CLK0_L F13 FB_B_CLK_N<0>
FBC_CLK1 F18 FB_B_CLK_P<1>
FBC_CLK1_L E17 FB_B_CLK_N<1>

FBCDQM0 A4 FB_B_DQM_L<0>
FBCDQM1 E11 FB_B_DQM_L<1>
FBCDQM2 F5 FB_B_DQM_L<2>
FBCDQM3 C9 FB_B_DQM_L<3>
FBCDQM4 C28 FB_B_DQM_L<4>
FBCDQM5 F24 FB_B_DQM_L<5>
FBCDQM6 C24 FB_B_DQM_L<6>
FBCDQM7 E20 FB_B_DQM_L<7>

READ STROBE
FBCDQS_RN0 C6 FB_B_RDQS<0>
FBCDQS_RN1 E9 FB_B_RDQS<1>
FBCDQS_RN2 E6 FB_B_RDQS<2>
FBCDQS_RN3 A8 FB_B_RDQS<3>
FBCDQS_RN4 B29 FB_B_RDQS<4>
FBCDQS_RN5 E25 FB_B_RDQS<5>
FBCDQS_RN6 A25 FB_B_RDQS<6>
FBCDQS_RN7 F21 FB_B_RDQS<7>

WRITE STROBE
FBCDQS_WP0 C5 FB_B_WDQS<0>
FBCDQS_WP1 E10 FB_B_WDQS<1>
FBCDQS_WP2 E5 FB_B_WDQS<2>
FBCDQS_WP3 B8 FB_B_WDQS<3>
FBCDQS_WP4 A29 FB_B_WDQS<4>
FBCDQS_WP5 D25 FB_B_WDQS<5>
FBCDQS_WP6 B25 FB_B_WDQS<6>
FBCDQS_WP7 F20 FB_B_WDQS<7>

FBC_DEBUG F12 TP_FBC_DEBUG

FBCAL_TERM_GND J26 FBCAL_TERM_GND
FB_VREF E32 GPU_FB_VREF

R8250 10K 5% 1/16W MF-LF 402
R8251 10K 5% 1/16W MF-LF 402
R8292 40.2 1% 1/16W MF-LF 402

=PP1V8_GPU_FBIO
R8295 1.07K 1% 1/16W MF-LF 402
C8296 0.1UF 10% 16V X5R 402
R8297 1.02K 1% 1/16W MF-LF 402
R8296 2.49K 1% 1/16W MF-LF 402

GPU_FB_VREF_UNTERM_L
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

Q8295 SSM6N15FE SOT563
FB_VREF_UNTERM

NV G84M Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 67 OF 89	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_GPU_FB_VDD

=PP1V8_GPU_FB_VDDQ

CRITICAL
OMIT

U8400
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

U8450
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

C8400 10UF 20% 6.3V X5R 603
C8401 C8402 C8403 C8404 0.1UF 10% 16V X5R 402
C8410 C8415 0.1UF 10% 16V X5R 402
Connect to designated pin, then GND
U8400.J1
U8400.J12

C8450 10UF 20% 6.3V X5R 603
C8451 C8452 C8453 C8454 0.1UF 10% 16V X5R 402
C8460 C8465 0.1UF 10% 16V X5R 402
Connect to designated pin, then GND
U8400.J1
U8400.J12

C8420 10UF 20% 6.3V X5R 603
C8421 C8422 C8423 C8424 C8425 C8426 0.1UF 10% 16V X5R 402

C8470 10UF 20% 6.3V X5R 603
C8471 C8472 C8473 C8474 C8475 C8476 0.1UF 10% 16V X5R 402

R8430 2.37K 1% 1/16W MF-LF 402
R8433 2.37K 1% 1/16W MF-LF 402
FB_A0_VREF
FB_A2_VREF
R8431 5.49K 1% 1/16W MF-LF 402
R8432 2.21K 1% 1/16W MF-LF 402
C8431 0.01UF 10% 16V CERM 402
R8434 5.49K 1% 1/16W MF-LF 402
R8435 2.21K 1% 1/16W MF-LF 402
C8432 0.01UF 10% 16V CERM 402
FB_A2_VREF_UNTERM_L
FB_A0_VREF_UNTERM_L

R8480 2.37K 1% 1/16W MF-LF 402
R8483 2.37K 1% 1/16W MF-LF 402
FB_A1_VREF
FB_A3_VREF
R8481 5.49K 1% 1/16W MF-LF 402
R8482 2.21K 1% 1/16W MF-LF 402
C8481 0.01UF 10% 16V CERM 402
R8484 5.49K 1% 1/16W MF-LF 402
R8485 2.21K 1% 1/16W MF-LF 402
C8482 0.01UF 10% 16V CERM 402
FB_A3_VREF_UNTERM_L
FB_A1_VREF_UNTERM_L

FB_A_CLK0_TERM
VOLTAGE=0.9V
R8440 1K 5% 1/16W MF-LF 402
VRAM4 R8442 121 1% 1/16W MF-LF 402
VRAM4 R8444 121 1% 1/16W MF-LF 402
VRAM4 R8443 121 1% 1/16W MF-LF 402
R8446 121 1% 1/16W MF-LF 402
VRAM4 R8445 121 1% 1/16W MF-LF 402
VRAM4 R8447 121 1% 1/16W MF-LF 402
C8446 0.01UF 10% 16V CERM 402
FB_VREF_UNTERM
Q8400 SSM6N15FE SOT563

FB_A_CLK1_TERM
VOLTAGE=0.9V
R8490 1K 5% 1/16W MF-LF 402
VRAM4 R8492 121 1% 1/16W MF-LF 402
VRAM4 R8494 121 1% 1/16W MF-LF 402
VRAM4 R8493 121 1% 1/16W MF-LF 402
R8496 121 1% 1/16W MF-LF 402
VRAM4 R8495 121 1% 1/16W MF-LF 402
VRAM4 R8497 121 1% 1/16W MF-LF 402
C8496 0.01UF 10% 16V CERM 402
FB_VREF_UNTERM
Q8450 SSM6N15FE SOT563

FB_A_MA<0>
FB_A_MA<1>
FB_A_LMA<2>
FB_A_LMA<3>
FB_A_LMA<4>
FB_A_LMA<5>
FB_A_MA<6>
FB_A_MA<7>
FB_A_MA<8>
FB_A_MA<9>
FB_A_MA<10>
FB_A_MA<11>
FB_A_CKE
FB_A_CLK_P<0>
FB_A_CLK_N<0>
FB_A_CS0_L
FB_A_WE_L
FB_A_CAS_L
FB_A_RAS_L
MFHIGH
MFHIGH
FB_A0_ZQ
FB_A0_MF
FB_A0_SEN
FB_A_DRAM_RST
FB_A_RDQS<0>
FB_A_RDQS<1>
FB_A_RDQS<2>
FB_A_RDQS<3>
FB_A_WDQS<0>
FB_A_WDQS<1>
FB_A_WDQS<2>
FB_A_WDQS<3>
FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>
FB_A_MA<12>
FB_A_CS1_L
(For 32Mx32 support)
R8448 243 1% 1/16W MF-LF 402
R8449 100 5% 1/16W MF-LF 402

FB_A_DQM_L<0>
FB_A_DQM_L<1>
FB_A_DQM_L<2>
FB_A_DQM_L<3>
FB_A_DQ<0>
FB_A_DQ<1>
FB_A_DQ<2>
FB_A_DQ<3>
FB_A_DQ<4>
FB_A_DQ<5>
FB_A_DQ<6>
FB_A_DQ<7>
FB_A_DQ<8>
FB_A_DQ<9>
FB_A_DQ<10>
FB_A_DQ<11>
FB_A_DQ<12>
FB_A_DQ<13>
FB_A_DQ<14>
FB_A_DQ<15>
FB_A_DQ<16>
FB_A_DQ<17>
FB_A_DQ<18>
FB_A_DQ<19>
FB_A_DQ<20>
FB_A_DQ<21>
FB_A_DQ<22>
FB_A_DQ<23>
FB_A_DQ<24>
FB_A_DQ<25>
FB_A_DQ<26>
FB_A_DQ<27>
FB_A_DQ<28>
FB_A_DQ<29>
FB_A_DQ<30>
FB_A_DQ<31>

FB_A_MA<0>
FB_A_MA<1>
FB_A_UMA<2>
FB_A_UMA<3>
FB_A_UMA<4>
FB_A_UMA<5>
FB_A_MA<6>
FB_A_MA<7>
FB_A_MA<8>
FB_A_MA<9>
FB_A_MA<10>
FB_A_MA<11>
FB_A_CKE
FB_A_CLK_P<1>
FB_A_CLK_N<1>
FB_A_CS0_L
FB_A_WE_L
FB_A_CAS_L
FB_A_RAS_L
MFHIGH
MFHIGH
FB_A1_ZQ
FB_A1_MF
FB_A1_SEN
FB_A_DRAM_RST
FB_A_RDQS<7>
FB_A_RDQS<5>
FB_A_RDQS<6>
FB_A_RDQS<4>
FB_A_WDQS<7>
FB_A_WDQS<5>
FB_A_WDQS<6>
FB_A_WDQS<4>
FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>
FB_A_MA<12>
FB_A_CS1_L
(For 32Mx32 support)
R8498 243 1% 1/16W MF-LF 402
R8499 100 5% 1/16W MF-LF 402

FB_A_DQM_L<7>
FB_A_DQM_L<5>
FB_A_DQM_L<6>
FB_A_DQM_L<4>
FB_A_DQ<62>
FB_A_DQ<56>
FB_A_DQ<58>
FB_A_DQ<59>
FB_A_DQ<57>
FB_A_DQ<63>
FB_A_DQ<60>
FB_A_DQ<61>
FB_A_DQ<40>
FB_A_DQ<47>
FB_A_DQ<46>
FB_A_DQ<45>
FB_A_DQ<42>
FB_A_DQ<44>
FB_A_DQ<41>
FB_A_DQ<43>
FB_A_DQ<50>
FB_A_DQ<48>
FB_A_DQ<52>
FB_A_DQ<51>
FB_A_DQ<55>
FB_A_DQ<49>
FB_A_DQ<54>
FB_A_DQ<53>
FB_A_DQ<34>
FB_A_DQ<33>
FB_A_DQ<35>
FB_A_DQ<32>
FB_A_DQ<36>
FB_A_DQ<37>
FB_A_DQ<39>
FB_A_DQ<38>

GDDR3 Frame Buffer A (Top)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

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Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_GPU_FB_VDD

=PP1V8_GPU_FB_VDDQ

Connect to designated pin, then GND

CRITICAL
OMIT

U8500
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

U8550
FBGA
(1 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

FB_B_CLK0_TERM
FB_B_CLK1_TERM
VOLTAGE=0.9V

FB_VREF_UNTERM

FB_B0_VREF
FB_B1_VREF
FB_B2_VREF
FB_B3_VREF

FB_B2_VREF_UNTERM_L
FB_B0_VREF_UNTERM_L
FB_B3_VREF_UNTERM_L
FB_B1_VREF_UNTERM_L

FB_B0_ZQ
FB_B0_MF
FB_B0_SEN
FB_B1_ZQ
FB_B1_MF
FB_B1_SEN

(For 32Mx32 support)

GDDR3 Frame Buffer B (Top)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

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D	051-7413	15.0.0
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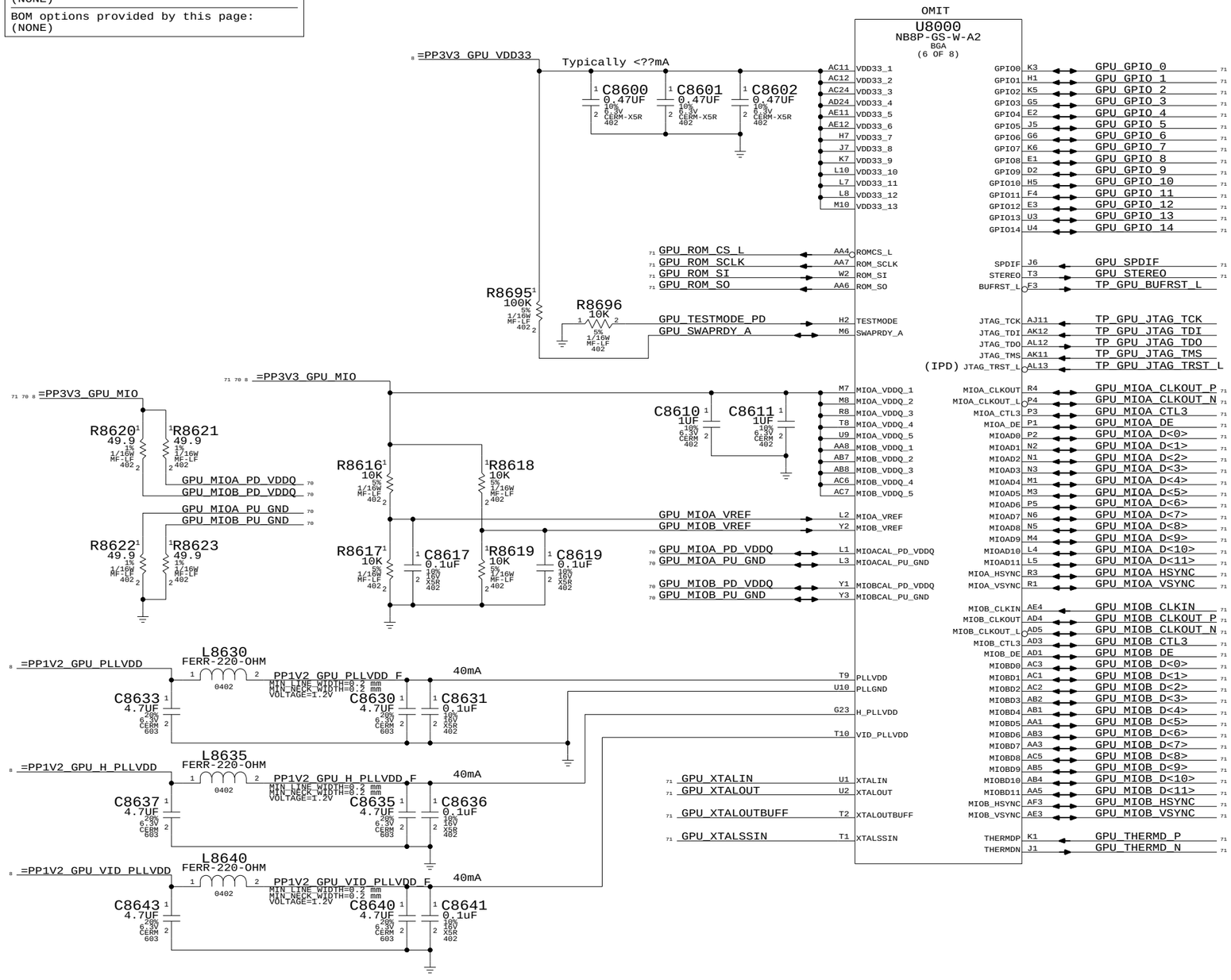
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M GPIO/MIO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

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GPIOs

	Native Func			
GPU_GPIO_0	HPD0	=	GPU_HPD	IN 78
GPU_GPIO_1	HPD1	=	NC_GPU_GPIO_1	
GPU_GPIO_2	LCD0_BL_PWM	=	GPU_BL_PWM	OUT 34
GPU_GPIO_3	LCD0_VDD	=	GPU_PANEL_EN	OUT 74
GPU_GPIO_4	LCD0_BL_EN	=	GPU_BKLT_EN	OUT 34
GPU_GPIO_5	VID0	=	TP_GPU_GSTATE<0>	
GPU_GPIO_6	VID1	=	TP_GPU_GSTATE<1>	
GPU_GPIO_7	MEM_VID	=	GPU_VGA_EN_L	71
GPU_GPIO_8	THERM	=	NC_GPU_GPIO_8	
GPU_GPIO_9	FAN_PWM	=	NC_GPU_GPIO_9	
GPU_GPIO_10	MEM_VREF	=	FB_VREF_UNTERM	OUT 67 68 69
GPU_GPIO_11	SLI_SYNC	=	GPU_VCORE_VID0	OUT 73
GPU_GPIO_12	AC_DET	=	GPU_VCORE_VID1	OUT 73
GPU_GPIO_13	PWR_CTL0	=	GPU_VCORE_VID2	OUT 73
GPU_GPIO_14	PWR_CTL1	=	GPU_VCORE_VID3	OUT 73

Config Straps

=PP3V3_GPU_MIO

VRAM_SAMSUNG	VRAM_8M	VRAM8	NO STUFF	NO STUFF	NO STUFF	NO STUFF		
R8720 10K	R8722 10K	R8724 10K	R8726 10K	R8728 2.2K	R8729 2.2K	R8730 2.2K	R8731 2.2K	R8732 2.2K

Supported straps:

RAMCFG0	GPU_MIOB_D<0>
RAMCFG1	GPU_MIOB_D<1>
RAMCFG2	GPU_MIOB_D<8>
RAMCFG3	GPU_MIOB_D<9>
3GIO_PADCFG0	GPU_MIOA_D<6>
3GIO_PADCFG1	GPU_MIOA_D<8>
3GIO_PADCFG2	GPU_MIOA_D<9>
3GIO_PADCFG3	GPU_MIOB_HSYNC
PEX_PLL_EN_TERM	GPU_MIOA_D<0>
SUBVENDOR (BIOS ROM PRESENT)	GPU_MIOA_D<1>
PCI_DEVID<3..0>	

VRAM_HYNIX	NO STUFF	VRAM_16M	VRAM4	
R8721 10K	R8723 10K	R8725 10K	R8727 10K	R8733 2.2K

Straps not supported:

USER<3..0>	MIOA_D<5..2>
ROMTYPE<1..0>	MIOB_VSYNC, MIOB_D<10>
SLOT_CLOCK_CFG	MIOA_HSYNC
PCI_IOBAR	MIOB_D<7>
BAR2_SIZE	MIOB_DE
PCI_DEVID<4>	MIOB_CTL3

PCI_DEVID3, PCI_DEVID2, PCI_DEVID1, PCI_DEVID0

=PP3V3_GPU_MIO

NO STUFF			
R8734 2.2K	R8735 2.2K	R8736 2.2K	R8737 2.2K

GPU_MIOB_D<11>, GPU_MIOB_D<3>, GPU_MIOB_D<5>, GPU_MIOB_D<4>

Analog Video Mux

=PP3V3_GPU_VIDEOMUX

C8700 0.1UF 20% 10V CERM 402

CRITICAL U8700 TS3V340 QFN 16

GPU_VGA_R	S1A	DA	GPU_TV_C_VGA_R
GPU_VGA_G	S2A	DB	GPU_TV_Y_VGA_G
GPU_VGA_B	S1B	DC	GPU_TV_COMP_VGA_B
	S2B	DD	NC
GPU_TV_C	S1C	IN	GPU_VGA_EN_L
GPU_TV_Y	S2C	EN_L	GND
GPU_TV_COMP	S1D	THRML PAD	GND
	S2D	VCC	

Place Rs near GPU: R8740 150 1%, R8741 150 1%, R8742 150 1%

Place Rs near GPU: R8743 150 1%, R8744 150 1%, R8745 150 1%

R8700 10K 5% 1/16W MF-LF 402

Renamed signals

GPU_CLK27M	=	GPU_XTALIN
GPU_CLK27M_SS	=	GPU_XTALSSIN
GPU_TDIODE_P	=	GPU_THERMD_P
GPU_TDIODE_N	=	GPU_THERMD_N
GPU_DVI_DDC_CLK	=	GPU_I2CB_SCL
GPU_DVI_DDC_DATA	=	GPU_I2CB_SDA
GPU_PANEL_DDC_CLK	=	GPU_I2CC_SCL
GPU_PANEL_DDC_DATA	=	GPU_I2CC_SDA
GPU_VDD_SENSE	=	TP_GPU_VDD_SENSE
GPU_GND_SENSE	=	TP_GPU_GND_SENSE

Unused I2C Buses

NC_GPU_I2CA_SCL	=	GPU_I2CA_SCL
NC_GPU_I2CA_SDA	=	GPU_I2CA_SDA

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

HDCP Support

=PP3V3_GPU_HDCP

HDCP R8770 10K 5% 1/16W MF-LF 402

HDCP C8770 0.1UF 20% 10V CERM 402

CRITICAL HDCP U8770 190-00001-0001 SOI

GPU_I2CH_SCL, GPU_I2CH_SDA

HDCP R8771 10K 5% 1/16W MF-LF 402

TMDS Backdrive Protection

CRITICAL Q8790 SI2305DS SOT-23

=PP3V3_GPU_TMDS, =PP3V3_S0GPU_TMDS_FET

R8790 10K 5% 1/16W MF-LF 402

GPU_TMDS_PWREN_L

Q8791 SSM6N15FE SOT563

=GPUVCORE_EN

R8791 100K 5% 1/16W MF-LF 402

Unused signals

NC_GPU_XTALOUT	=	GPU_XTALOUT
NC_GPU_SPDIF	=	GPU_SPDIF
NC_GPU_STEREO	=	GPU_STEREO
NC_FBA_MA<13>	=	FB_A_MA<13>
NC_FBB_MA<13>	=	FB_B_MA<13>
NC_FBA_CMD28	=	TP_FBA_CMD28
NC_FBC_CMD28	=	TP_FBC_CMD28
NC_GPU_ROM_CS_L	=	GPU_ROM_CS_L
NC_GPU_ROM_SCLK	=	GPU_ROM_SCLK
NC_GPU_ROM_SI	=	GPU_ROM_SI
NC_GPU_ROM_SO	=	GPU_ROM_SO
NC_GPU_CSYNC	=	GPU_CSYNC
NC_GPU_R2	=	GPU_R2
NC_GPU_G2	=	GPU_G2
NC_GPU_B2	=	GPU_B2
NC_GPU_H2SYNC	=	GPU_H2SYNC
NC_GPU_V2SYNC	=	GPU_V2SYNC
NC_LVDS_U_DATAP<3>	=	LVDS_U_DATA_P<3>
NC_LVDS_U_DATAN<3>	=	LVDS_U_DATA_N<3>
NC_LVDS_L_DATAP<3>	=	LVDS_L_DATA_P<3>
NC_LVDS_L_DATAN<3>	=	LVDS_L_DATA_N<3>
TP_GPU_MIOA_CLKOUT_P	=	GPU_MIOA_CLKOUT_P
TP_GPU_MIOA_CLKOUT_N	=	GPU_MIOA_CLKOUT_N
TP_GPU_MIOA_CTL3	=	GPU_MIOA_CTL3
TP_GPU_MIOA_DE	=	GPU_MIOA_DE
TP_GPU_MIOA_D<5..2>	=	GPU_MIOA_D<5..2>
TP_GPU_MIOA_D<7>	=	GPU_MIOA_D<7>
TP_GPU_MIOA_D<11..10>	=	GPU_MIOA_D<11..10>
TP_GPU_MIOA_HSYNC	=	GPU_MIOA_HSYNC
TP_GPU_MIOA_VSYNC	=	GPU_MIOA_VSYNC
TP_GPU_MIOB_CLKIN	=	GPU_MIOB_CLKIN
TP_GPU_MIOB_CLKOUT_P	=	GPU_MIOB_CLKOUT_P
TP_GPU_MIOB_CLKOUT_N	=	GPU_MIOB_CLKOUT_N
TP_GPU_MIOB_CTL3	=	GPU_MIOB_CTL3
TP_GPU_MIOB_DE	=	GPU_MIOB_DE
TP_GPU_MIOB_D<2>	=	GPU_MIOB_D<2>
TP_GPU_MIOB_D<7..6>	=	GPU_MIOB_D<7..6>
TP_GPU_MIOB_D<10>	=	GPU_MIOB_D<10>
TP_GPU_MIOB_VSYNC	=	GPU_MIOB_VSYNC
NC_GPU_IFPD_CLK_P	=	GPU_IFPD_CLK_P
NC_GPU_IFPD_CLK_N	=	GPU_IFPD_CLK_N

Unused Clocks

GPU_XTALSSIN, GPU_XTALOUTBUFF

R8780 10K 5% 1/16W MF-LF 402

GPU_SS_INT

R8781 10K 5% 1/16W MF-LF 402

GPU Straps

SYNC_MASTER=M88 SYNC_DATE=08/02/2007

APPLE INC.

SIZE D | DRAWING NUMBER 051-7413 | REV. 15.0.0

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Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

=PP1V8_GPU_IFPX

L8800 FERR-220-OHM 0402
20mA peak per diff pair
160mA peak for all pairs
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402
Place at AF9 Place at AF8

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

L8805 FERR-220-OHM 0402
40mA peak
C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

72 GPU_IFPAB_VPROBE
72 GPU_IFPAB_RSET

=PP3V3_GPU_IFPCD_IOVDD

L8810 FERR-220-OHM 0402
20mA peak per diff pair
200mA peak for all pairs
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402
Place at AD6 Place at AE7

PP3V3_GPU_IFPCD_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

L8815 FERR-220-OHM 0402
40mA peak
C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPCD_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

72 GPU_IFPCD_VPROBE
72 GPU_IFPCD_RSET

Sum of peak currents: 390mA

=PP3V3_GPU_DAC

L8820 FERR-220-OHM 0402
120mA peak
C8820 4.7UF 20% 6.3V CERM 603
C8821 0.1UF 20% 10V CERM 402

PP3V3_GPU_DACA_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

72 GPU_DACA_VREF
72 GPU_DACA_RSET

L8830 FERR-220-OHM 0402
150mA peak
C8830 4.7UF 20% 6.3V CERM 603
C8831 0.1UF 20% 10V CERM 402

PP3V3_GPU_DACB_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

72 GPU_DACB_VREF
72 GPU_DACB_RSET

NO STUFF
L8840 FERR-220-OHM 0402
120mA peak
C8845 4.7UF 20% 6.3V CERM 603
NO STUFF
C8840 4.7UF 20% 6.3V CERM 603
C8841 0.1UF 20% 10V CERM 402

PP3V3_GPU_DACC_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

72 GPU_DACC_VREF
72 GPU_DACC_RSET

71 GPU_I2CC_SCL
71 GPU_I2CC_SDA
71 GPU_I2CH_SCL
71 GPU_I2CH_SDA
=GPU_I2CS_SCL
=GPU_I2CS_SDA

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

OMIT
U8000 NB8P-GS-W-A2 BGA (5 OF 8)

AF9	IFPA_IOVDD	IFPA_TXC	AK9
AF8	IFPB_IOVDD	IFPA_TXC_L	AJ9
AC9	IFPAB_PLLVDD	IFPA_TXD0	AH6
AD9	IFPAB_PLLGND	IFPA_TXD0_L	AJ6
AM4	IFPAB_VPROBE	IFPA_TXD1	AH8
AL5	IFPAB_RSET	IFPA_TXD1_L	AH7
		IFPA_TXD2	AJ8
		IFPA_TXD2_L	AK8
		IFPA_TXD3	AJ5
		IFPA_TXD3_L	AH5
		IFPB_TXC	AK4
		IFPB_TXC_L	AL4
		IFPB_TXD4	AM6
		IFPB_TXD4_L	AM5
		IFPB_TXD5	AM7
		IFPB_TXD5_L	AL7
		IFPB_TXD6	AK6
		IFPB_TXD6_L	AK5
		IFPB_TXD7	AK7
		IFPB_TXD7_L	AL8
AD6	IFPC_IOVDD	IFPC_TXC	AM2
AE7	IFPD_IOVDD	IFPC_TXC_L	AM3
AA10	IFPCD_PLLVDD	IFPC_TXD0	AE2
AB10	IFPCD_PLLGND	IFPC_TXD0_L	AE1
AK3	IFPCD_VPROBE	IFPC_TXD1	AF1
AH3	IFPCD_RSET	IFPC_TXD1_L	AF2
		IFPC_TXD2	AG1
		IFPC_TXD2_L	AH1
		IFPD_TXC	AG3
		IFPD_TXC_L	AH2
		IFPD_TXD4	AK1
		IFPD_TXD4_L	AJ1
		IFPD_TXD5	AL2
		IFPD_TXD5_L	AL1
		IFPD_TXD6	AJ2
		IFPD_TXD6_L	AJ3
AD10	DACA_VDD	DACA_RED	AH11
AG9	DACA_IDUMP	DACA_GREEN	AJ12
AH10	DACA_VREF	DACA_BLUE	AH12
AH9	DACA_RSET	DACA_HSYNC	AF10
		DACA_VSYNC	AK10
V8	DACB_VDD	DACB_RED	R6
V7	DACB_IDUMP	DACB_GREEN	T5
R5	DACB_VREF	DACB_BLUE	T6
R7	DACB_RSET	DACB_CSYNC	U5
AD7	DACC_VDD	DACC_RED	AF6
AG4	DACC_IDUMP	DACC_GREEN	AG6
AH4	DACC_VREF	DACC_BLUE	AE5
AF5	DACC_RSET	DACC_HSYNC	AG7
		DACC_VSYNC	AG5
G2	I2CC_SCL	I2CA_SCL	K2
G1	I2CC_SDA	I2CA_SDA	J3
G3	I2CH_SCL	I2CB_SCL	H4
H3	I2CH_SDA	I2CB_SDA	J4
C1	I2CS_SCL		
B1	I2CS_SDA		

LVDS_L_CLK_P	IFPA_TXC
LVDS_L_CLK_N	IFPA_TXC_L
LVDS_L_DATA_P<0>	IFPA_TXD0
LVDS_L_DATA_N<0>	IFPA_TXD0_L
LVDS_L_DATA_P<1>	IFPA_TXD1
LVDS_L_DATA_N<1>	IFPA_TXD1_L
LVDS_L_DATA_P<2>	IFPA_TXD2
LVDS_L_DATA_N<2>	IFPA_TXD2_L
LVDS_L_DATA_P<3>	IFPA_TXD3
LVDS_L_DATA_N<3>	IFPA_TXD3_L
LVDS_U_CLK_P	IFPB_TXC
LVDS_U_CLK_N	IFPB_TXC_L
LVDS_U_DATA_P<0>	IFPB_TXD4
LVDS_U_DATA_N<0>	IFPB_TXD4_L
LVDS_U_DATA_P<1>	IFPB_TXD5
LVDS_U_DATA_N<1>	IFPB_TXD5_L
LVDS_U_DATA_P<2>	IFPB_TXD6
LVDS_U_DATA_N<2>	IFPB_TXD6_L
LVDS_U_DATA_P<3>	IFPB_TXD7
LVDS_U_DATA_N<3>	IFPB_TXD7_L
TMDS_CLK_P	IFPC_TXC
TMDS_CLK_N	IFPC_TXC_L
TMDS_DATA_P<0>	IFPC_TXD0
TMDS_DATA_N<0>	IFPC_TXD0_L
TMDS_DATA_P<1>	IFPC_TXD1
TMDS_DATA_N<1>	IFPC_TXD1_L
TMDS_DATA_P<2>	IFPC_TXD2
TMDS_DATA_N<2>	IFPC_TXD2_L
GPU_IFPD_CLK_P	IFPD_TXC
GPU_IFPD_CLK_N	IFPD_TXC_L
TMDS_DATA_P<3>	IFPD_TXD4
TMDS_DATA_N<3>	IFPD_TXD4_L
TMDS_DATA_P<4>	IFPD_TXD5
TMDS_DATA_N<4>	IFPD_TXD5_L
TMDS_DATA_P<5>	IFPD_TXD6
TMDS_DATA_N<5>	IFPD_TXD6_L
GPU_VGA_R	DACA_RED
GPU_VGA_G	DACA_GREEN
GPU_VGA_B	DACA_BLUE
GPU_VGA_HSYNC	DACA_HSYNC
GPU_VGA_VSYNC	DACA_VSYNC
GPU_TV_C	DACB_RED
GPU_TV_Y	DACB_GREEN
GPU_TV_COMP	DACB_BLUE
GPU_CSYNC	DACB_CSYNC
GPU_R2	DACC_RED
GPU_G2	DACC_GREEN
GPU_B2	DACC_BLUE
GPU_H2SYNC	DACC_HSYNC
GPU_V2SYNC	DACC_VSYNC
GPU_I2CA_SCL	I2CA_SCL
GPU_I2CA_SDA	I2CA_SDA
GPU_I2CB_SCL	I2CB_SCL
GPU_I2CB_SDA	I2CB_SDA

Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb

GPU_IFPAB_RSET 72
GPU_IFPCD_RSET 72
GPU_DACA_RSET 72
GPU_DACB_RSET 72
GPU_DACC_RSET 72

NO STUFF R8850 1K 1% 1/16W ME-LF 402
NO STUFF R8851 1K 1% 1/16W ME-LF 402
R8852 124 1% 1/16W ME-LF 402
R8853 124 1% 1/16W ME-LF 402
R8854 124 1% 1/16W ME-LF 402

GPU_DACA_VREF 72
GPU_DACB_VREF 72
GPU_DACC_VREF 72

C8852 0.1UF 20% 16V CERM 402
C8853 0.1UF 20% 16V CERM 402
C8854 0.1UF 20% 16V CERM 402

GPU_IFPAB_VPROBE 72
GPU_IFPCD_VPROBE 72

NO STUFF C8855 0.01UF 20% 16V CERM 402
NO STUFF C8856 0.01UF 20% 16V CERM 402

NV G84M Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

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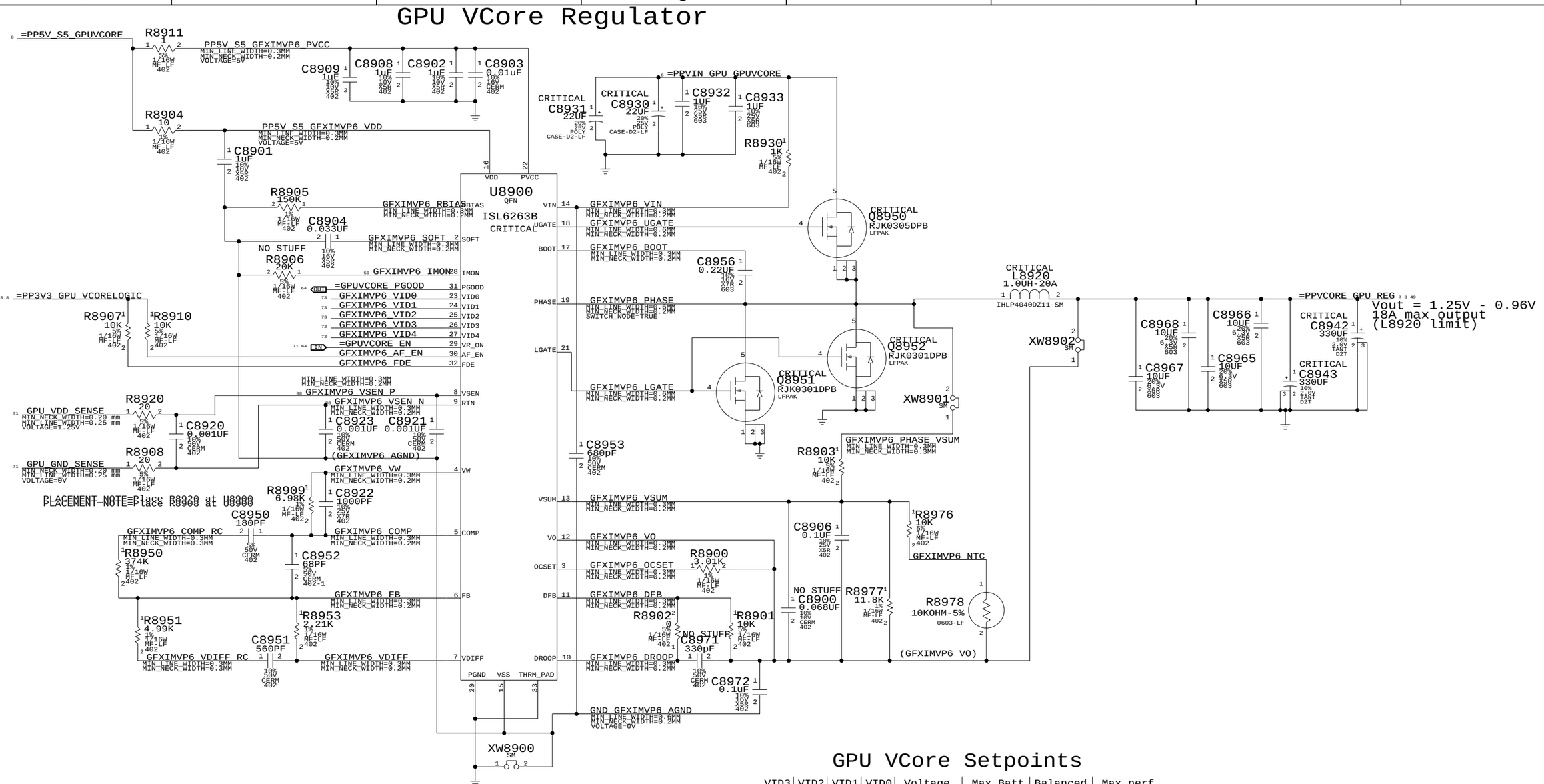
SCALE: NONE	SHT 72 OF 89	

GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	0	1	1.05575V	M87,M88	M87	-
0	1	1	0	1.13300V	-	M88	M87
0	0	1	0	1.23600V	-	-	M88

Other VID states may not be valid

M87/M88 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P26V	GPUVID3_0,GPUVID2_0,GPUVID1_1,GPUVID0_0
GPUVID_1P13V	GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_0
GPUVID_1P05V	GPUVID3_1,GPUVID2_0,GPUVID1_0,GPUVID0_1

GPU (G84M) Core Supply

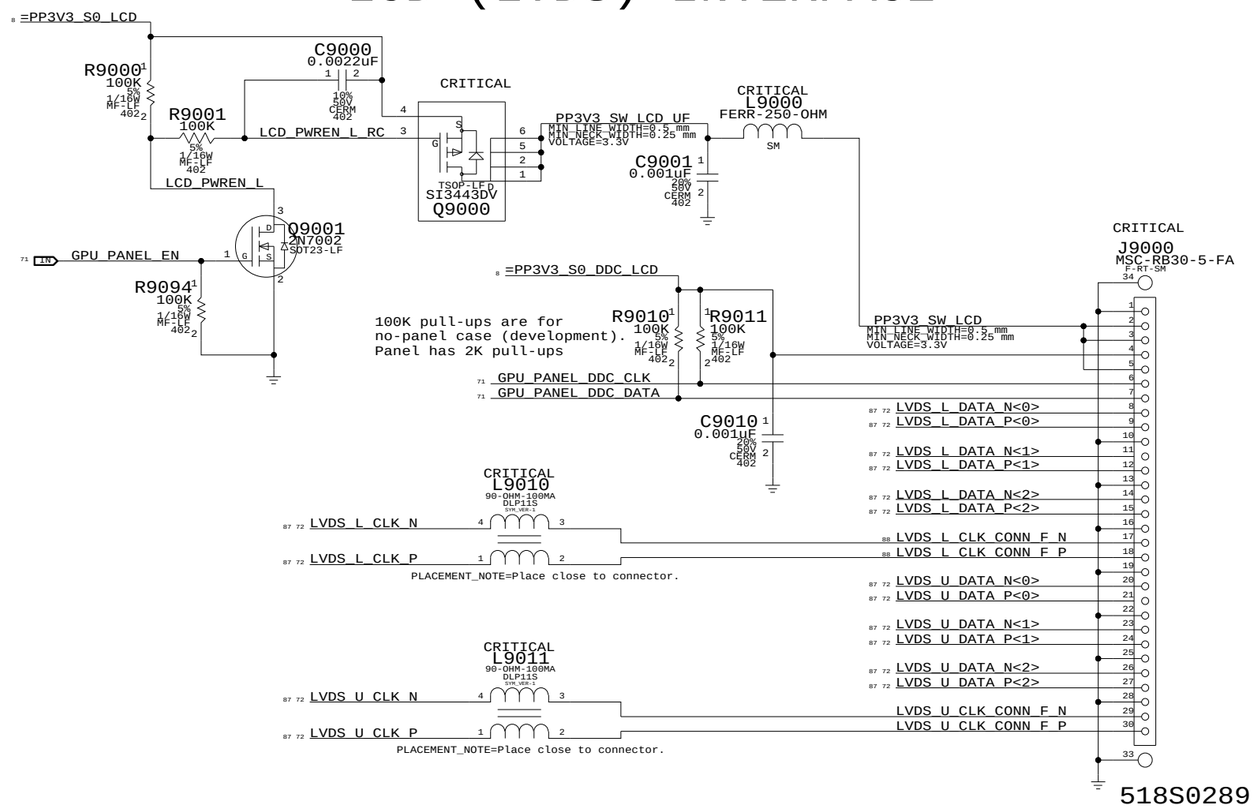
SYNC_MASTER=M88 SYNC_DATE=08/02/2007

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 73	OF 89

LCD (LVDS) INTERFACE



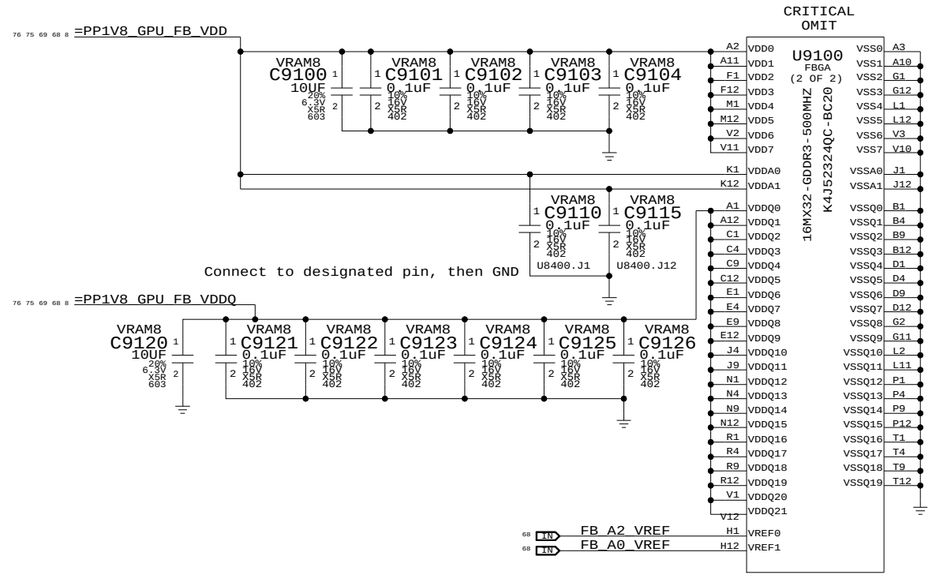
LVDS Display Connector

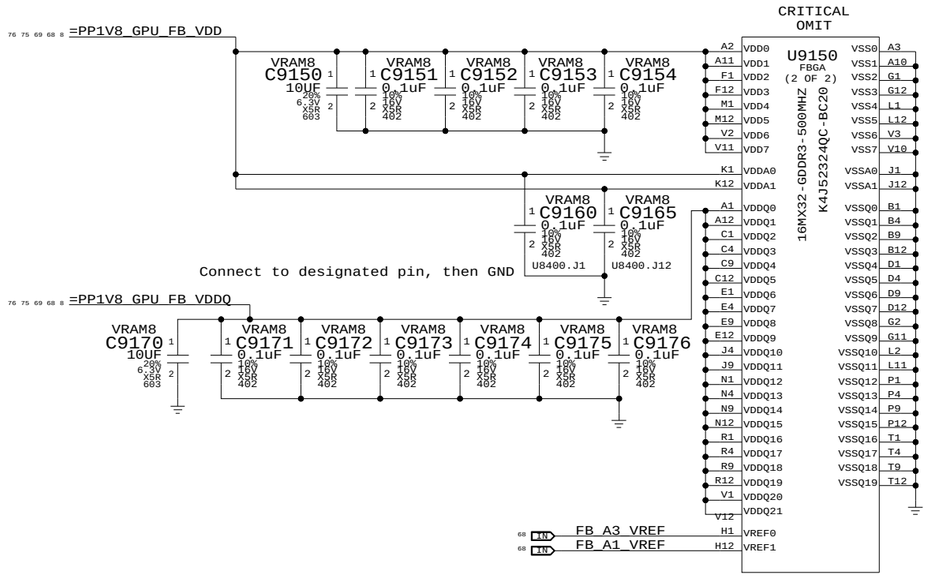
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

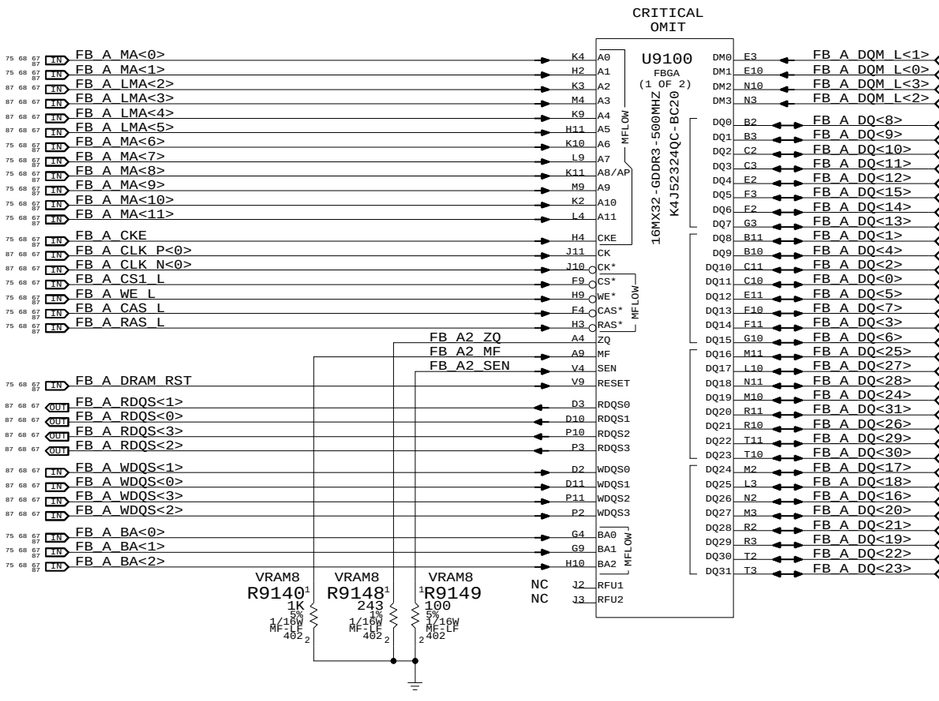
APPLE INC.

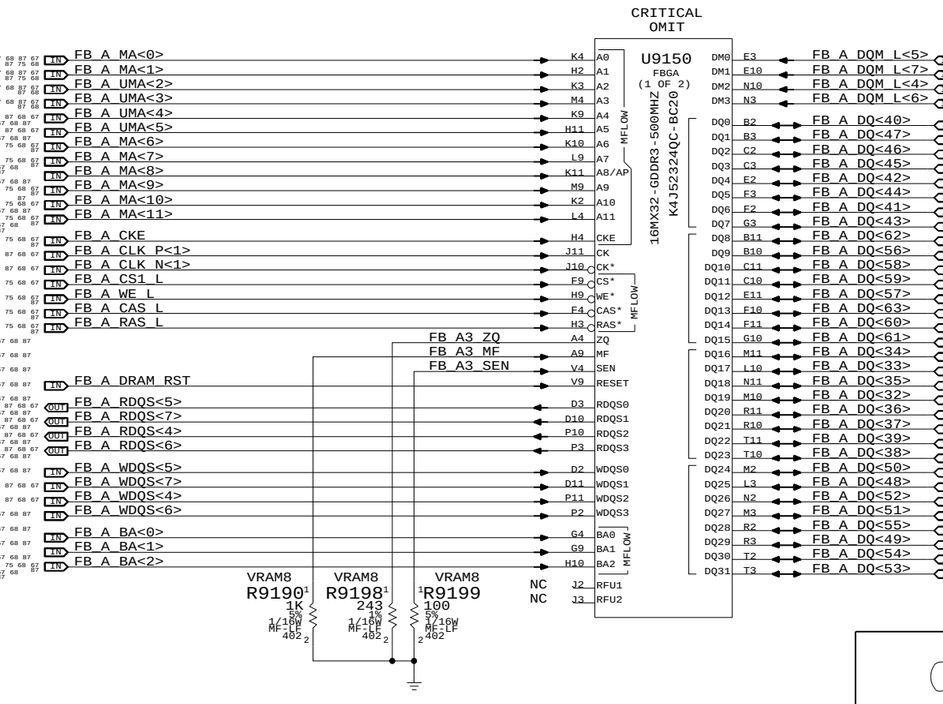
SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	74	89









Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

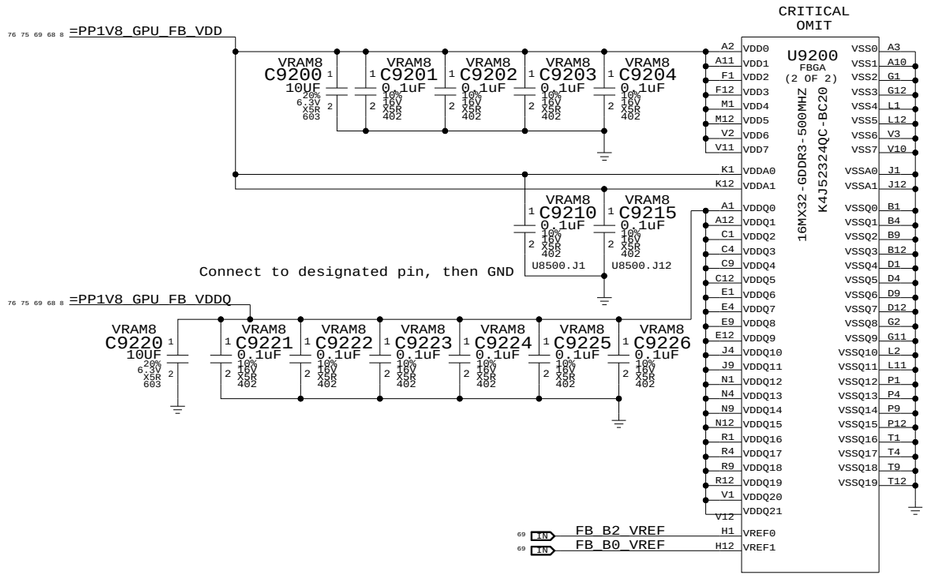
BOM options provided by this page:
(NONE)

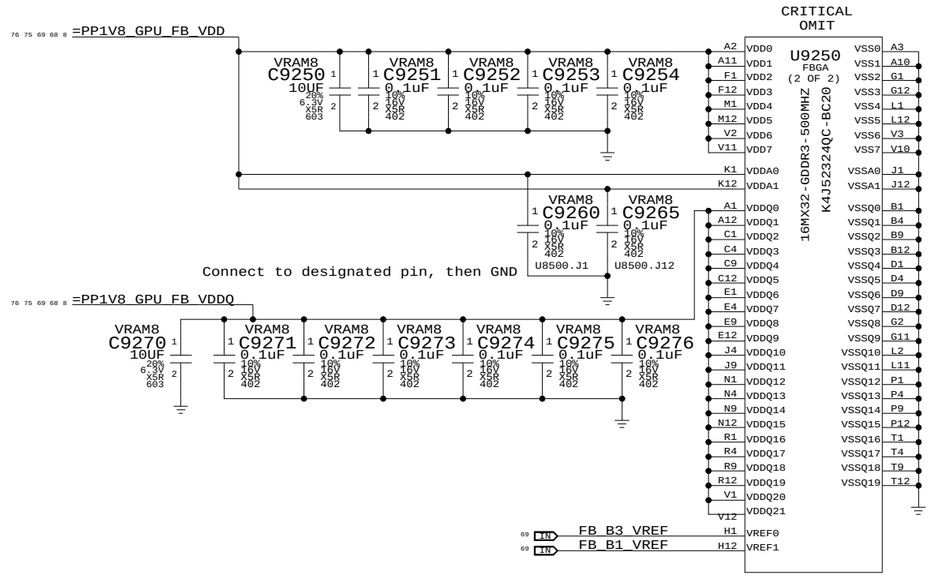
GDDR3 Frame Buffer A (Bot)

SYNC_MASTER=M88_MLB_VRAMSORT SYNC_DATE=06/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 75 OF 89	



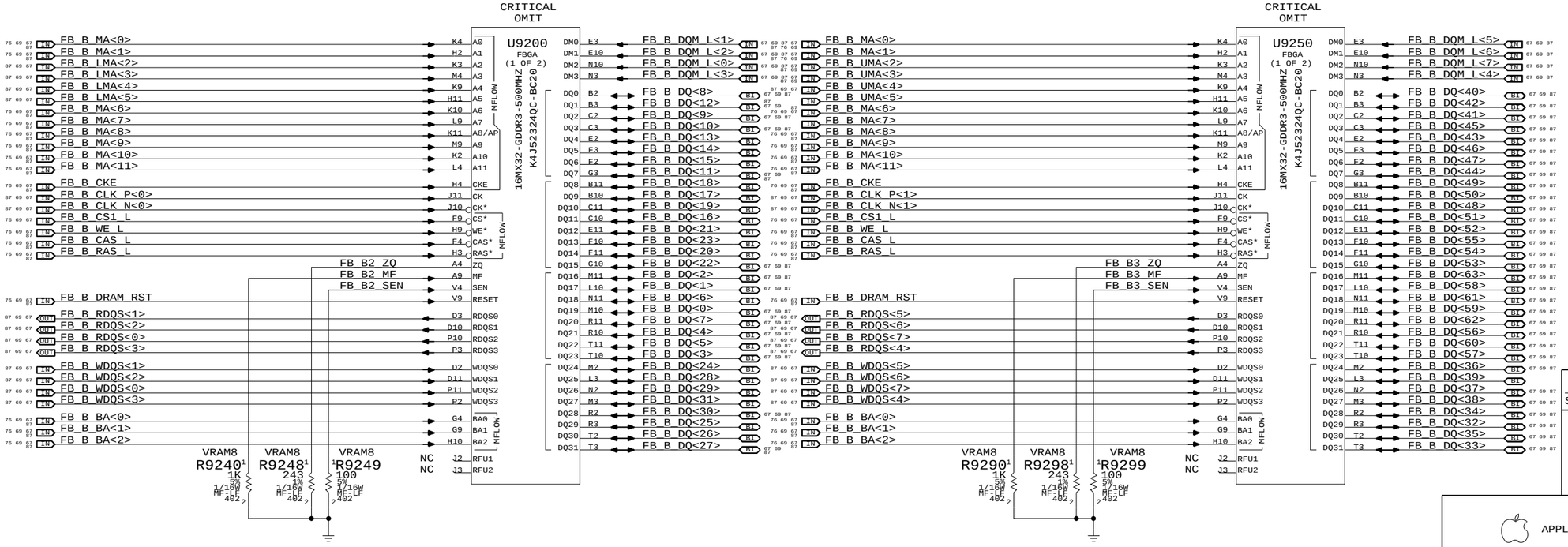


Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



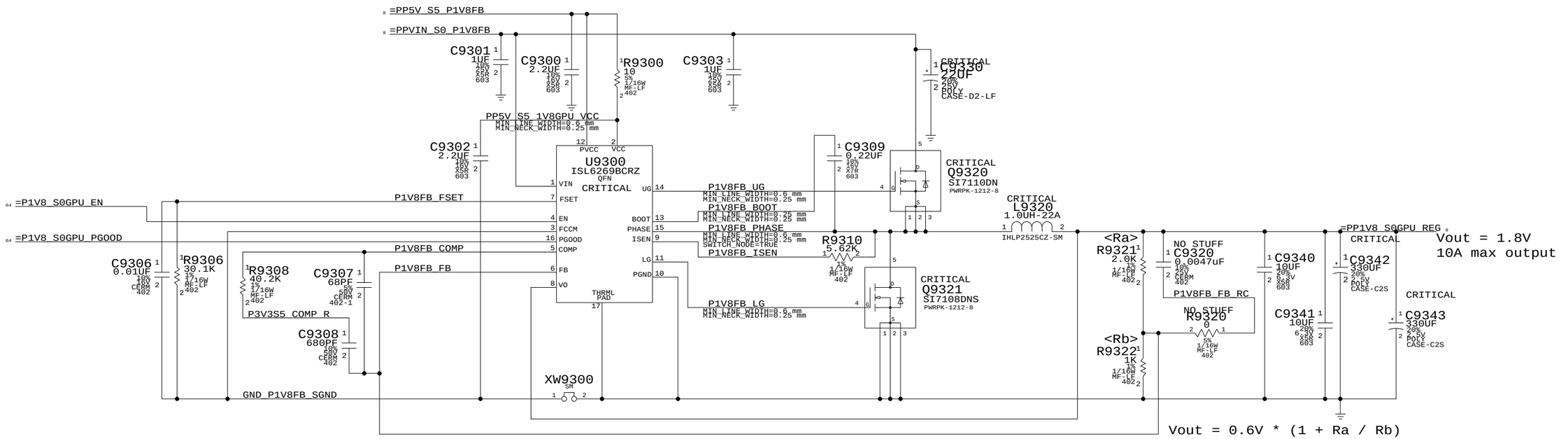
GDDR3 Frame Buffer B (Bot)

SYNC_MASTER=M88_MLB_VRAMSUB SYNC_DATE=06/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 76 OF 89	

1.8V Frame Buffer Regulator



1.8V FB Power Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 77 OF 89	

TMDS Filtering

(Place close to GPU) (Place close to connector)

TMDS_DATA_N<0> — NO STUFF R9462 49.9 1% 1/16W MF-LF 402 — SIGNAL_MODEL=EMPTY TMDS_DATA_R0 — NO STUFF R9463 49.9 1% 1/16W MF-LF 402 — TMDS_DATA_P<0>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9462 0.01UF 10% 16V CERM 402
CRITICAL L9460 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<0> / TMDS_DATA_F_P<0>
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<1> — NO STUFF R9466 49.9 1% 1/16W MF-LF 402 — SIGNAL_MODEL=EMPTY TMDS_DATA_R1 — NO STUFF R9467 49.9 1% 1/16W MF-LF 402 — TMDS_DATA_P<1>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9466 0.01UF 10% 16V CERM 402
CRITICAL L9464 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<1> / TMDS_DATA_F_P<1>
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<2> — NO STUFF R9470 49.9 1% 1/16W MF-LF 402 — SIGNAL_MODEL=EMPTY TMDS_DATA_R2 — NO STUFF R9471 49.9 1% 1/16W MF-LF 402 — TMDS_DATA_P<2>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9470 0.01UF 10% 16V CERM 402
CRITICAL L9468 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<2> / TMDS_DATA_F_P<2>
PLACEMENT_NOTE=Place close to connector.

TMDS_CLK_N — R9472 0 5% 1/16W MF-LF 402 — TMDS_CLK_R_N — CRITICAL L9472 370-OHM SM — TMDS_CLK_F_N / TMDS_CLK_F_P
=PP3V3_GPU_TMDSBIAS — NO STUFF C9474 0.01UF 10% 16V CERM 402 — NO STUFF R9474 49.9 1% 1/16W MF-LF 402 — SIGNAL_MODEL=EMPTY TMDS_CLK_CMF — NO STUFF R9475 49.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to connector.
TMDS_CLK_P — R9473 0 5% 1/16W MF-LF 402 — TMDS_CLK_R_P

TMDS_DATA_N<3> — NO STUFF R9478 49.9 1% 1/16W MF-LF 402 — SIGNAL_MODEL=EMPTY TMDS_DATA_R3 — NO STUFF R9479 49.9 1% 1/16W MF-LF 402 — TMDS_DATA_P<3>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9478 0.01UF 10% 16V CERM 402
CRITICAL L9476 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<3> / TMDS_DATA_F_P<3>
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<4> — NO STUFF R9482 49.9 1% 1/16W MF-LF 402 — SIGNAL_MODEL=EMPTY TMDS_DATA_R4 — NO STUFF R9483 49.9 1% 1/16W MF-LF 402 — TMDS_DATA_P<4>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9482 0.01UF 10% 16V CERM 402
CRITICAL L9480 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<4> / TMDS_DATA_F_P<4>
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<5> — NO STUFF R9486 49.9 1% 1/16W MF-LF 402 — SIGNAL_MODEL=EMPTY TMDS_DATA_R5 — NO STUFF R9487 49.9 1% 1/16W MF-LF 402 — TMDS_DATA_P<5>
=PP3V3_GPU_TMDSBIAS — NO STUFF C9486 0.01UF 10% 16V CERM 402
CRITICAL L9484 90-OHM-100MA 1210-4SM1 — TMDS_DATA_F_N<5> / TMDS_DATA_F_P<5>
PLACEMENT_NOTE=Place close to connector.

VGA SYNC Buffers

=PP3V3_GPU_VGASYNC — C9450 0.1UF 20% 25V CERM 402 — GPU_VGA_VSYNC — U9450 MC74VHC1G08 SC70 — PLACEMENT_NOTE=Place close to connector. — VGA_VSYNC_R — R9450 33 5% 1/16W MF-LF 402 — VGA_VSYNC

=PP3V3_GPU_VGASYNC — C9451 0.1UF 20% 25V CERM 402 — GPU_VGA_HSYNC — U9451 MC74VHC1G08 SC70 — PLACEMENT_NOTE=Place close to connector. — VGA_HSYNC_R — R9451 33 5% 1/16W MF-LF 402 — VGA_HSYNC

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

GPU_TV_COMP_VGA_B — VGA_TERM_FILTER R9440 150 1% 1/16W MF-LF 402 — CRITICAL FL9440 210MHZ MEA2010P-SM — C9440 3.3pF 0.25pF 50V CERM 402 — VGA_B (DACB TV COMP)
GPU_TV_Y_VGA_G — VGA_TERM_FILTER R9441 150 1% 1/16W MF-LF 402 — C9441 3.3pF 0.25pF 50V CERM 402 — VGA_G (DACB TV Y)
GPU_TV_C_VGA_R — VGA_TERM_FILTER R9442 150 1% 1/16W MF-LF 402 — C9442 3.3pF 0.25pF 50V CERM 402 — VGA_R (DACB TV C)

DVI INTERFACE

DVI DDC Current Limit

(55mA requirement per DVI spec)

=PP5V_S0_DVI_DDC — CRITICAL F9410 0.5AMP-13.2V SM-LF — PP5V_S0_DDC_F (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V) — CRITICAL L9410 400-OHM-EMI SM-1 — PP5V_S0_DDC (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)
C9410 0.01UF 20% 50V CERM 603
CRITICAL J9400 QH11121-RIG02-4F F-RT-TH-DVI

TMDS_DATA_F_N<0> — TMDS_DATA_F_N<2>
TMDS_DATA_F_N<1>
TMDS_DATA_F_P<0> — TMDS_DATA_F_P<2>
TMDS_DATA_F_P<1>
TMDS_DATA_F_N<5> — TMDS_DATA_F_N<4>
TMDS_DATA_F_N<3>
TMDS_DATA_F_P<5> — TMDS_DATA_F_P<4>
TMDS_DATA_F_P<3>
DVI_DDC_CLK_R — (PP5V_S0_DDC)
TMDS_CLK_F_P — DVI_DDC_DATA_R
TMDS_CLK_F_N — VGA_VSYNC
DVI_HPD_R
VGA_B — VGA_R
VGA_HSYNC — VGA_G

VGA_TERM_CONN R9445 150 1% 1/16W MF-LF 402
VGA_TERM_CONN R9443 150 1% 1/16W MF-LF 402
VGA_TERM_CONN R9444 150 1% 1/16W MF-LF 402

514-0278

Isolation required for DVI->ADC Adapter

PP5V_S0_DDC_PULLUPS (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V) — D9410 SOD-123 B0530WXF

R9410 4.7K 5% 1/16W MF-LF 402 — R9412 4.7K 5% 1/16W MF-LF 402
R9411 100 5% 1/16W MF-LF 402 — DVI_DDC_CLK
C9411 100pF 5% 50V CERM 402
R9413 100 5% 1/16W MF-LF 402 — DVI_DDC_DATA
C9413 100pF 5% 50V CERM 402
R9414 100 5% 1/16W MF-LF 402 — DVI_HPD
C9414 100pF 5% 50V CERM 402
R9415 20K 5% 1/16W MF-LF 402

GPU Isolation / Level-Shift

=PP3V3_GPU_DVI

Q9411 2N7002DW-X-F SOT-363 — R9420 10K 5% 1/16W MF-LF 402 — GPU_DVI_DDC_CLK
Q9411 2N7002DW-X-F SOT-363 — R9421 10K 5% 1/16W MF-LF 402 — GPU_DVI_DDC_DATA
Q9414 2N7002DW-X-F SOT-363 — R9422 100K 5% 1/16W MF-LF 402 — GPU_HPD

DVI_HOTPLUG_DET — R9416 10K 5% 1/16W MF-LF 402

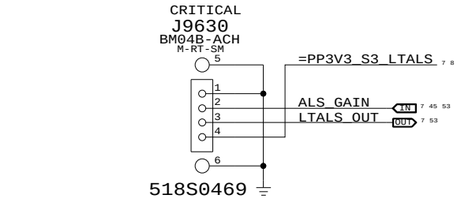
DVI Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

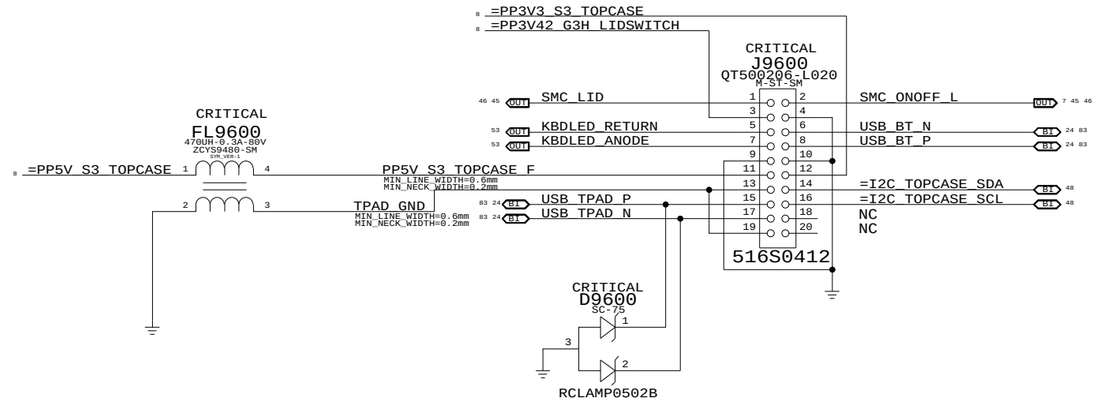
SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 78 OF 89	

Left ALS Connector

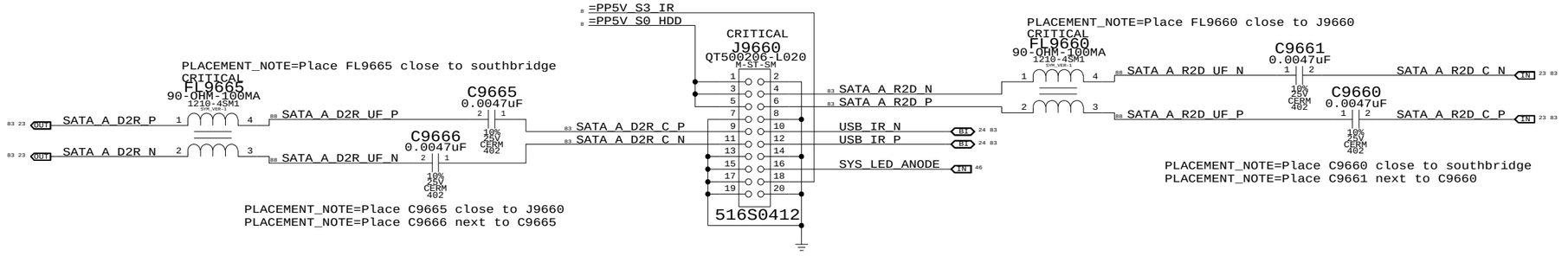


White colored version of 518S0369

Top-Case Connector



SATA HDD & IR & SIL Flex Connector



NOTE: SATA _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

Project Specific Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 79 OF 89	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	10
CPU_FERR_L	CPU_55S		CPU_FERR_L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	10 46 58
CPU_PWRGD	CPU_55S		CPU_PWRGD	7 10 13 23
CPU_FROM_SB	CPU_55S		CPU_INTR	10 23
CPU_FROM_SB	CPU_55S		CPU_NMI	10 23
CPU_FROM_SB	CPU_55S		CPU_A20M_L	10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	7 10 23
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	10 23 47
CPU_FROM_SB	CPU_55S		CPU_SMI_L	10 23
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	7 10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	7 16 25 58
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	7 58
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	7 10 16 23 58
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 85
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 85
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	13
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	7 12 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 58
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	58
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	58

CPU/FSB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 80 OF 89	

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
LVDS	*	20 MIL	?	
CRT	*	25 MIL	?	DG Says 40 mil spacing minimum
CRT_2CRT	*	20 MIL	?	
CRT_SYNC	*	25 MIL	?	DG Says 30 mil spacing minimum
CRT_SYNC2SYNC	*	20 MIL	?	
TVDAC	*	25 MIL	?	DG Says 40 mil spacing minimum
TVDAC_2TVDAC	*	20 MIL	?	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.

CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG_R2D_P<15..0>	65
	PCIE_100D	PCIE	PEG_R2D_N<15..0>	65
	PCIE_100D	PCIE	PEG_R2D_C_P<15..0>	15 65
	PCIE_100D	PCIE	PEG_R2D_C_N<15..0>	15 65
PEG_D2R	PCIE_100D	PCIE	PEG_D2R_P<15..0>	15 65
	PCIE_100D	PCIE	PEG_D2R_N<15..0>	15 65
	PCIE_100D	PCIE	PEG_D2R_C_P<15..0>	65
	PCIE_100D	PCIE	PEG_D2R_C_N<15..0>	65
DMI_N2S	DMI_100D	DMI	DMI_N2S_P<3..0>	16 24
	DMI_100D	DMI	DMI_N2S_N<3..0>	16 24
DMI_S2N	DMI_100D	DMI	DMI_S2N_P<3..0>	16 24
	DMI_100D	DMI	DMI_S2N_N<3..0>	16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	15 22
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	15 22
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_N<3>	
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	15 22
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	15 22
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_P<3>	
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_N<3>	
LVDS_IBG		LVDS	LVDS_IBG	15 22
CRT_TVO_IREF		CRT	CRT_TVO_IREF	
CRT_RED	CRT_50S	CRT	CRT_RED	
CRT_GREEN	CRT_50S	CRT	CRT_GREEN	
CRT_BLUE	CRT_50S	CRT	CRT_BLUE	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R	
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC	
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC	
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC	

NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 81 OF 89	

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK_N<2..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK_N<5..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	17 32

Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 82 OF 89	

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L	23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ	23 42
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L	24 42
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	23 79
	SATA_100D	SATA	SATA_A_R2D_C_N	23 79
	SATA_100D	SATA	SATA_A_R2D_P	79
	SATA_100D	SATA	SATA_A_R2D_N	79
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P	23 79
	SATA_100D	SATA	SATA_A_D2R_N	23 79
	SATA_100D	SATA	SATA_A_D2R_C_P	79
	SATA_100D	SATA	SATA_A_D2R_C_N	79
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D_C_P	23 42
	SATA_100D	SATA	SATA_B_R2D_C_N	23 42
	SATA_100D	SATA	SATA_B_R2D_P	
	SATA_100D	SATA	SATA_B_R2D_N	
SATA_B_D2R	SATA_100D	SATA	SATA_B_D2R_P	23 42
	SATA_100D	SATA	SATA_B_D2R_N	23 42
	SATA_100D	SATA	SATA_B_D2R_C_P	
	SATA_100D	SATA	SATA_B_D2R_C_N	
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D_C_P	23 42
	SATA_100D	SATA	SATA_C_R2D_C_N	23 42
	SATA_100D	SATA	SATA_C_R2D_P	
	SATA_100D	SATA	SATA_C_R2D_N	
SATA_C_D2R	SATA_100D	SATA	SATA_C_D2R_P	23 42
	SATA_100D	SATA	SATA_C_D2R_N	23 42
	SATA_100D	SATA	SATA_C_D2R_C_P	
	SATA_100D	SATA	SATA_C_D2R_C_N	
SATA_RBIAS	SATA_55S		SATA_RBIAS	42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	23 34
	HDA_55S	HDA	HDA_BIT_CLK_R	23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	23 34
	HDA_55S	HDA	HDA_SYNC_R	23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	23 34
	HDA_55S	HDA	HDA_RST_L_R	23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	23 34
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	23 34
	HDA_55S	HDA	HDA_SDOUT_R	23
USB_EXTA	USB_90D	USB	USB_EXTA_P	24 43
	USB_90D	USB	USB_EXTA_N	24 43
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	24 34
	USB_90D	USB	USB_MINI_N	24 34
USB_EXTD	USB_90D	USB	USB_EXTD_P	9 24
	USB_90D	USB	USB_EXTD_N	9 24
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7 24 44
	USB_90D	USB	USB_CAMERA_N	7 24 44
USB_BT	USB_90D	USB	USB_BT_P	24 79
	USB_90D	USB	USB_BT_N	24 79
USB_TPAD	USB_90D	USB	USB_TPAD_P	24 79
	USB_90D	USB	USB_TPAD_N	24 79
USB_IR	USB_90D	USB	USB_IR_P	24 79
	USB_90D	USB	USB_IR_N	24 79
USB_EXTB	USB_90D	USB	USB_EXTB_P	24 34
	USB_90D	USB	USB_EXTB_N	24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	24 34
	USB_90D	USB	USB_EXCARD_N	24 34
USB_EXTC	USB_90D	USB	USB_EXTC_P	9 24
	USB_90D	USB	USB_EXTC_N	9 24
USB_RBIAS	USB_60S		USB_RBIAS	24
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK	25 48
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA	25 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK	25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA	25 48
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	24 55
	SPI_55S	SPI	SPI_SCLK	55
	SPI_55S	SPI	SPI_A_SCLK_R	
	SPI_55S	SPI	SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	24 55
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	55
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	24 55
	SPI_55S	SPI	SPI_A_SO_R	55
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_I0	SPI_55S	SPI	SPI_CE_R_L<0>	24 55
	SPI_55S	SPI	SPI_CE_L<0>	55
SPI_CE_I1	SPI_55S	SPI	SPI_CE_R_L<1>	
	SPI_55S	SPI	SPI_CE_L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCI_AD	PCI_55S	PCI	PCI_AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI_AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI_AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI_AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI_PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	24 38
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI_LOCK_L	24
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI_FW_REQ_L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI_FW_GNT_L	24 38
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	24
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_REQ2_L	PCI_55S	PCI	PCI_REQ2_L	24
PCI_GNT2_L	PCI_55S	PCI	PCI_GNT2_L	
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	24 38
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L	9 24
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE_A_R2D_C_P	
	PCIE_100D	PCIE	PCIE_A_R2D_C_N	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE_A_D2R_P	
	PCIE_100D	PCIE	PCIE_A_D2R_N	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_B_R2D_C_P	
	PCIE_100D	PCIE	PCIE_B_R2D_C_N	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_B_D2R_P	
	PCIE_100D	PCIE	PCIE_B_D2R_N	
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_P	34
	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_N	34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE_EXCARD_D2R_P	34
	PCIE_100D	PCIE	PCIE_EXCARD_D2R_N	34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_100D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE_FW_D2R_P	
	PCIE_100D	PCIE	PCIE_FW_D2R_N	
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE_MINI_R2D_C_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_R2D_C_N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE_MINI_D2R_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_D2R_N	24 34
GLAN_COMP			GLAN_COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE_ENET_R2D_C_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_C_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_P	35
	PCIE_100D	PCIE	PCIE_ENET_R2D_N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE_ENET_D2R_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_P	35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<0>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<1>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<2>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3>	35 37

SB Constraints (2 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	84	89

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	29 30
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	29 30
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	29 30
CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	29 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 80
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 80
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 47
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	30 38
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	30 45
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_DOT96)	CRT_50S	GND	NB_CLK96M_DOT_P	
(CK505_DOT96)	CRT_50S	GND	NB_CLK96M_DOT_N	
(CK505_LVDS)	CRT_50S	GND	NB_CLK100M_DPLLSS_P	
(CK505_LVDS)	CRT_50S	GND	NB_CLK100M_DPLLSS_N	
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	9
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	9
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	30 34
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	30 34
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 30
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	30 34
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	30 34
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	30 35
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	30 35

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	48
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	48
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	48
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	48
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	48
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	48
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	48
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	48
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48

Clock & SMC Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 85 OF 89	

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
FW_D_CTL	FW_55S	FW	FW_LINK<7..0>	
FW_D_CTL	FW_55S	FW	FW_CTL<1..0>	
FW_LCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_LCLK	
	CLK_MED_55S	CLK_MED	CLKFW_PHY_LCLK	38 39
FW_PCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_PCLK	38 39
	CLK_MED_55S	CLK_MED	CLKFW_PHY_PCLK	
FW_LKON	FW_55S	FW	FW_LKON	
	FW_55S	FW	FW_LKON_R	
FW_LPS	FW_55S	FW	FW_LPS	38 39
FW_LREQ	FW_55S	FW	FW_LREQ	38 39
FW_PINT	FW_55S	FW	FW_PINT	38 39
FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R	
	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI	
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_P	39 41
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_N	39 41
FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_P	39 41
FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_N	39 41
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_P	39 41
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_N	39 41
FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_P	39 41
FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_N	39 41

Port 2 Not Used

FireWire Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0

SCALE	SHT	OF
NONE	86	89

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	=55_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_46SE	*	=46_OHM_SE	=46_OHM_SE	=46_OHM_SE	=46_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<11..6>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CKE
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS0_L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST
FB_A_CMD	GDDR3_46SE	GDDR3_CMD	FB_A_LMA<5..2>
FB_B_CMD	GDDR3_46SE	GDDR3_CMD	FB_A_UMA<5..2>
FB_A_WDQS0	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<0>
FB_A_WDQS1	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<1>
FB_A_WDQS2	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<2>
FB_A_WDQS3	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<3>
FB_A_RDQS0	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<0>
FB_A_RDQS1	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<1>
FB_A_RDQS2	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<2>
FB_A_RDQS3	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<3>
FB_A_DQ_BYTE0	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<7..0>
FB_A_DQ_BYTE1	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<15..8>
FB_A_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<23..16>
FB_A_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<31..24>
FB_A_DQM0	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<0>
FB_A_DQM1	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<1>
FB_A_DQM2	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<2>
FB_A_DQM3	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<3>
FB_B_WDQS0	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<4>
FB_B_WDQS1	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<5>
FB_B_WDQS2	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<6>
FB_B_WDQS3	GDDR3_46SE	GDDR3_DQS	FB_A_WDQS<7>
FB_B_RDQS0	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<4>
FB_B_RDQS1	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<5>
FB_B_RDQS2	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<6>
FB_B_RDQS3	GDDR3_46SE	GDDR3_DQS	FB_A_RDQS<7>
FB_B_DQ_BYTE0	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<39..32>
FB_B_DQ_BYTE1	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<47..40>
FB_B_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<55..48>
FB_B_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB_A_DQ<63..56>
FB_B_DQM0	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<4>
FB_B_DQM1	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<5>
FB_B_DQM2	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<6>
FB_B_DQM3	GDDR3_46SE	GDDR3_DATA	FB_A_DQM_L<7>

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<11..6>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CKE
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS0_L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST
FB_C_CMD	GDDR3_46SE	GDDR3_CMD	FB_B_LMA<5..2>
FB_D_CMD	GDDR3_46SE	GDDR3_CMD	FB_B_UMA<5..2>
FB_C_WDQS0	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<0>
FB_C_WDQS1	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<1>
FB_C_WDQS2	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<2>
FB_C_WDQS3	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<3>
FB_C_RDQS0	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<0>
FB_C_RDQS1	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<1>
FB_C_RDQS2	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<2>
FB_C_RDQS3	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<3>
FB_C_DQ_BYTE0	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<7..0>
FB_C_DQ_BYTE1	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<15..8>
FB_C_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<23..16>
FB_C_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<31..24>
FB_C_DQM0	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<0>
FB_C_DQM1	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<1>
FB_C_DQM2	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<2>
FB_C_DQM3	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<3>
FB_D_WDQS0	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<4>
FB_D_WDQS1	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<5>
FB_D_WDQS2	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<6>
FB_D_WDQS3	GDDR3_46SE	GDDR3_DQS	FB_B_WDQS<7>
FB_D_RDQS0	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<4>
FB_D_RDQS1	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<5>
FB_D_RDQS2	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<6>
FB_D_RDQS3	GDDR3_46SE	GDDR3_DQS	FB_B_RDQS<7>
FB_D_DQ_BYTE0	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<39..32>
FB_D_DQ_BYTE1	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<47..40>
FB_D_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<55..48>
FB_D_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB_B_DQ<63..56>
FB_D_DQM0	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<4>
FB_D_DQM1	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<5>
FB_D_DQM2	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<6>
FB_D_DQM3	GDDR3_46SE	GDDR3_DATA	FB_B_DQM_L<7>

G84M Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS
LVDS_L_CLK	LVDS_100D	LVDS	LVDS_L_CLK_P
	LVDS_100D	LVDS	LVDS_L_CLK_N
LVDS_L_DATA	LVDS_100D	LVDS	LVDS_L_DATA_P<2..0>
	LVDS_100D	LVDS	LVDS_L_DATA_N<2..0>
I127	LVDS_100D	LVDS	LVDS_L_DATA_P<3>
I126	LVDS_100D	LVDS	LVDS_L_DATA_N<3>
LVDS_U_CLK	LVDS_100D	LVDS	LVDS_U_CLK_P
	LVDS_100D	LVDS	LVDS_U_CLK_N
LVDS_U_DATA	LVDS_100D	LVDS	LVDS_U_DATA_P<2..0>
	LVDS_100D	LVDS	LVDS_U_DATA_N<2..0>
I128	LVDS_100D	LVDS	LVDS_U_DATA_P<3>
I129	LVDS_100D	LVDS	LVDS_U_DATA_N<3>
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_N
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<5..0>
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_N<5..0>
VGA_R_TV_C	VGA_50S	VGA	GPU_TV_C_VGA_R
VGA_G_TV_Y	VGA_50S	VGA	GPU_TV_Y_VGA_G
VGA_B_TV_COMP	VGA_50S	VGA	GPU_TV_COMP_VGA_B
	VGA_50S	VGA	GPU_VGA_R
	VGA_50S	VGA	GPU_VGA_G
	VGA_50S	VGA	GPU_VGA_B
	VGA_50S	VGA	GPU_TV_C
	VGA_50S	VGA	GPU_TV_Y
	VGA_50S	VGA	GPU_TV_COMP
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_HSYNC
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_VSYNC

GPU (G84M) Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE: NONE	SHT 87 OF 89	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
DMI	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	ENET_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	FW_POWER	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*			0.100 MM	2.54 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	ISL10			0.100 MM	2.54 MM		
MEM_85D	ISL4,ISL10			0.100 MM	2.54 MM		

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
TMDS_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

M87 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_P	34
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_N	34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_P	34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_N	34
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3..0>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3..0>	
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
	FW_110D	FW_TP	FW_PORT0_TPA_FL_P	41
	FW_110D	FW_TP	FW_PORT0_TPA_FL_N	41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_P	41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_N	41
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_P	79
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_N	79
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_P	79
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_N	79
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	43
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	43
(USB_EXTA)	USB_90D	USB	USB2_RT_P	43
(USB_EXTA)	USB_90D	USB	USB2_RT_N	43
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_P	
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_N	
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_P	44
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_P	73
	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_N	73
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	NBCOREISNS_P	50
	SENSE_1TO1_55S	SENSE	NBCOREISNS_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8ISNS_P	50
	SENSE_1TO1_55S	SENSE	P1V8ISNS_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V25ISNS_P	50
	SENSE_1TO1_55S	SENSE	P1V25ISNS_N	50
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	7 51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 51
	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 71
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	51 71
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	HSTHMSNS_D_P	7 51
	THERM_1TO1_55S	THERM	HSTHMSNS_D_N	7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	RSFSTHMSNS_D_P	7 51
	THERM_1TO1_55S	THERM	RSFSTHMSNS_D_N	7 51
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_P	74
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_N	74
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8ISNS_R_P	50
	SENSE_1TO1_55S	SENSE	P1V8ISNS_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_P	50
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_N	50
	TMDS_100D	TMDS	TMDS_CLK_R_P	78
	TMDS_100D	TMDS	TMDS_CLK_R_N	78
	TMDS_100D	TMDS	TMDS_CLK_F_P	78
	TMDS_100D	TMDS	TMDS_CLK_F_N	78
	TMDS_100D	TMDS	TMDS_DATA_F_P<5..0>	78
	TMDS_100D	TMDS	TMDS_DATA_F_N<5..0>	78
(VGA_R_TV_Y)	VGA_50S	VGA	VGA_R	78
(VGA_G_TV_C)	VGA_50S	VGA	VGA_G	78
(VGA_B_TV_COMP)	VGA_50S	VGA	VGA_B	78
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC_R	78
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC_R	78
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC	78
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC	78
		PP1V8_MEM	=PP1V8_S3M_MEM_A	8 31
		PP1V8_MEM	=PP1V8_S3M_MEM_B	8 32
		GND	GND	
		ENET_POWER		
		SB_POWER	PP3V3_S5	8
		SB_POWER	PP3V3_S0	8 64
		SB_POWER	PP1V5_S0	8
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_P	50
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_N	50
		FW_POWER		

Project Specific Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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M75 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	ISL2,ISL11	Y	0.250 MM	0.076 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.125 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
46_OHM_SE	TOP,BOTTOM	Y	0.126 MM	0.126 MM			
46_OHM_SE	*	Y	0.100 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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