1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
G		599886	PRODUCTION RELEASED	06/06/08	

SCHEMATIC,MLB,"Gloxter"

6/6/2008

Page (.csa)		Contents	Sync	Date
1	1	Table of Contents	N/A	N/A
2	2	System Block Diagram	(MASTER)	(MASTER)
3	3	Power Block Diagram	(MASTER)	(MASTER)
4	4	Power Block Diagram	N/A	N/A
5	5	BOM Configuration	N/A	N/A
6	6	Revision History	N/A	N/A
7	7	Functional / ICT Test	MASTER	MASTER
8	8	Power Aliases	(MASTER)	(MASTER)
9	9	Signal Aliases	MASTER	MASTER
10	10	CPU FSB	M87_MLB	08/28/2007
11	11	CPU Power & Ground	M87_MLB	08/28/2007
12	12	CPU Decoupling & VID	M87_MLB	08/28/2007
13	13	eXtended Debug Port (XDP)	T9_NOME	01/22/2007
14	14	NB CPU Interface	T9_NOME	01/25/2007
15	15	NB PEG / Video Interfaces	T9_NOME	03/19/2007
16	16	NB Misc Interfaces	T9_NOME	01/25/2007
17	17	NB DDR2 Interfaces	T9_NOME	01/25/2007
18	18	NB Power 1	T9_NOME	01/25/2007
19	19	NB Power 2	T9_NOME	01/25/2007
20	20	NB Grounds	T9_NOME	01/25/2007
21	21	NB Standard Decoupling	MASTER	MASTER
22	22	NB Graphics Decoupling	M87_MLB	08/28/2007
23	23	SB Enet, Disk, FSB, LPC	T9_NOME	01/25/2007
24	24	SB PCI, PCIe, DMI, USB	M87_MLB	08/28/2007
25	25	SB Pwr Mgt, GPIO, Clink	M87_MLB	08/28/2007
26	26	SB Power & Ground	T9_NOME	01/25/2007
27	27	SB Decoupling	MASTER	MASTER
28	28	SB Misc	M87_MLB	08/28/2007
29	29	Clock (CK505)	T9_NOME	01/25/2007
30	30	Clock Termination	M87_MLB	08/28/2007
31	31	DDR2 SO-DIMM Connector A	M87_MLB	08/28/2007
32	32	DDR2 SO-DIMM Connector B	M87_MLB	08/28/2007
33	33	Memory Active Termination	(MASTER)	(MASTER)
34	34	Left I/O Board Connector	(MASTER)	(MASTER)
35	37	Ethernet (Yukon)	T9_NOME	01/25/2007
36	38	Yukon Power Control	T9_NOME	03/19/2007
37	39	Ethernet Connector	M87_MLB	08/28/2007
38	40	FireWire Link (TSB83AA22)	M87_MLB	08/28/2007
39	41	FireWire PHY (TSB83AA22)	M87_MLB	08/28/2007
40	42	FireWire Port Power	M87_MLB	08/28/2007
41	43	FireWire Ports	M87_MLB	08/28/2007
42	44	PATA Connector	MASTER	MASTER
43	46	External USB Connector	MASTER	MASTER
44	47	Left Clutch Barrel Interconnect	M87_MLB	08/28/2007
45	49	SMC	M87_MLB	08/28/2007
46	50	SMC Support	M87_MLB	10/15/2007
47	51	LPC+ Debug Connector	M87_MLB	08/28/2007
48	52	SMBus Connections	(MASTER)	(MASTER)
49	53	Current & Voltage Sensing	M87_MLB	08/28/2007
50	54	Current Sensing	MASTER	MASTER
51	55	Thermal Sensors	M87_MLB	08/28/2007
52	56	Fan Connectors	M87_MLB	08/28/2007
53	57	Current & Thermal Sensors	M87_LIO	11/06/2007
54	58	ALS Support	M87_MLB	08/28/2007
55	59	Sudden Motion Sensor (SMS)	M87_MLB	08/28/2007
56	61	SPI BootROM	T9_NOME	01/25/2007
57	69	DC-In & Battery Connectors	(MASTER)	(MASTER)
58	70	Power FETs	M87_MLB	08/28/2007
59	71	IMVP6 CPU VCore Regulator	MASTER	MASTER
60	73	5V / 3.3V Power Supply	MASTER	MASTER
61	74	1.25V / 1.05V Power Supply	M87_MLB	08/28/2007
62	75	1.8V DDR2 Supply	M87_MLB	08/28/2007
63	76	1.5V Power Supply	MASTER	MASTER
64	77	FW PHY Power Supplies	M87_MLB	08/28/2007
65	78	3.425V G3Hot Supply & Power Control	M87_MLB	09/26/2007
66	79	PBus Supply & Batt. Charger	MASTER	MASTER
67	80	NV G84M PCI-E	M87_MLB	08/28/2007
68	81	NV G84M Core/FB Power	M87_MLB	08/28/2007
69	82	NV G84M Frame Buffer I/F	M87_MLB	08/28/2007
70	84	GDDR3 Frame Buffer A (Top)	M87_MLB	08/28/2007
71	85	GDDR3 Frame Buffer B (Top)	M87_MLB	08/28/2007
72	86	NV G84M GPIO/MIO/Misc	M87_MLB	08/28/2007
73	87	GPU Straps	M87_MLB	08/28/2007
74	88	NV G84M Video Interfaces	M87_MLB	08/28/2007
75	89	GPU (G84M) Core Supply	M87_MLB	09/26/2007
76	90	LVDS Display Connector	MASTER	MASTER
77	91	GDDR3 Frame Buffer A (Bot)	M87_MLB	08/28/2007
78	92	GDDR3 Frame Buffer B (Bot)	M87_MLB	08/28/2007
79	93	1.8V FB Power Supply	MASTER	MASTER
80	94	DVI Display Connector	MASTER	MASTER
81	96	Project Specific Connectors	(MASTER)	(MASTER)
82	98	LCD Backlight Support	M87_LIO	12/06/2007
83	100	CPU/FSB Constraints	T9_NOME	01/25/2007
84	101	NB Constraints	T9_NOME	01/25/2007
85	102	Memory Constraints	T9_NOME	01/25/2007
86	103	SB Constraints (1 of 2)	T9_NOME	01/25/2007
87	104	SB Constraints (2 of 2)	T9_NOME	01/25/2007
88	105	Clock & SMC Constraints	M87_MLB	08/28/2007
89	106	FireWire Constraints	T9_NOME	01/25/2007
90	107	GPU (G84M) Constraints	M87_MLB	10/02/2007
91	108	Project Specific Constraints	M87_MLB	08/28/2007
92	109	PCB Rule Definitions	M87_MLB	10/03/2007

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Jun 6 19:18:03 2008

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

APPLE INC.

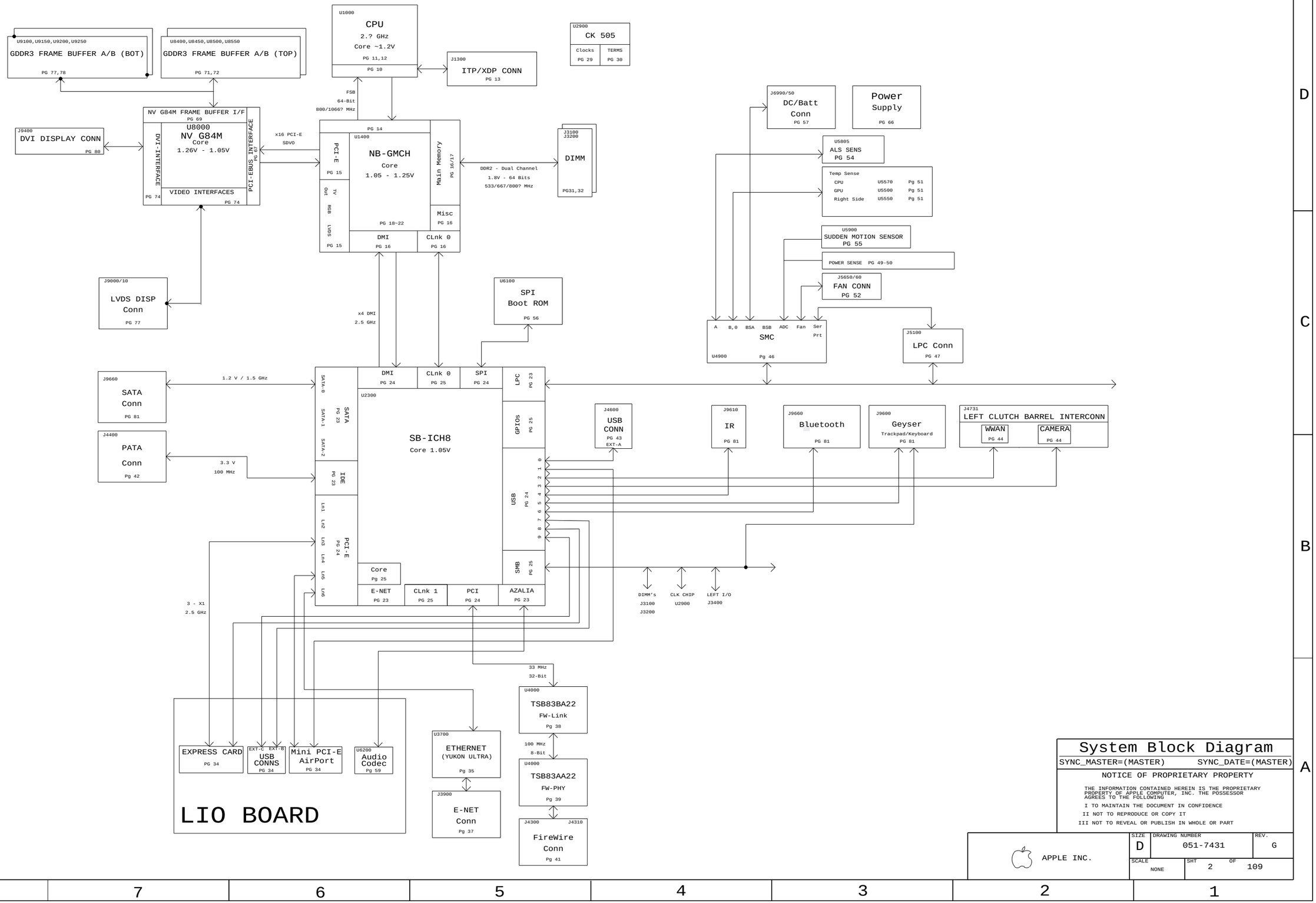
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

TITLE
SCHEM,MLB,MBP17

DRAWING NUMBER 051-7431
REV. G
SHT 1 OF 109


U9100,U9150,U9200,U9250
GDDR3 FRAME BUFFER A/B (BOT)
PG 77,78
U8400,U8450,U8500,U8550
GDDR3 FRAME BUFFER A/B (TOP)
PG 71,72
U1000
CPU
2.? GHz
Core ~1.2V
PG 11,12
PG 10
J1300
ITP/XDP CONN
PG 13
U2900
CK 505
Clocks
PG 29
TERMS
PG 30
FSB
64-Bit
800/1066? MHz
NV G84M FRAME BUFFER I/F
PG 69
U8000
NV G84M
Core
1.26V - 1.05V
DVI-INTERFACE
PCI-EBUS INTERFACE
PG 67
VIDEO INTERFACES
PG 74
J9400
DVI DISPLAY CONN
PG 80
x16 PCI-E
SDVO
PG 14
U1400
NB-GMCH
Core
1.05 - 1.25V
PG 18-22
PCI-E
PG 15
TV Out
RGB
LVDS
PG 15
Main Memory
PG 16/17
Misc
PG 16
DMI
PG 16
CLnk 0
PG 16
DDR2 - Dual Channel
1.8V - 64 Bits
533/667/800? MHz
J3100
J3200
DIMM
PG31,32
J9000/10
LVDS DISP
Conn
PG 77
x4 DMI
2.5 GHz
U6100
SPI
Boot ROM
PG 56
J9990/50
DC/Batt
Conn
PG 57
Power
Supply
PG 66
U5805
ALS SENS
PG 54
Temp Sense
CPU U5570 Pg 51
GPU U5500 Pg 51
Right Side U5550 Pg 51
U5900
SUDDEN MOTION SENSOR
PG 55
POWER SENSE PG 49-50
J5650/60
FAN CONN
PG 52
A
B,0
BSA
BSB
ADC
Fan
Ser Prt
SMC
U4900
Pg 46
J5100
LPC Conn
PG 47
J9660
SATA
Conn
PG 81
1.2 V / 1.5 GHz
SATA-0
SATA-1
SATA-2
SATA
PG 23
DMI
PG 24
CLnk 0
PG 25
SPI
PG 24
LPC
PG 23
U2300
SB-ICH8
Core 1.05V
GPIOs
PG 25
USB
PG 24
J4600
USB
CONN
PG 43
EXT-A
J9610
IR
PG 81
J9660
Bluetooth
PG 81
J9600
Geyser
Trackpad/Keyboard
PG 81
J4731
LEFT CLUTCH BARREL INTERCONN
WWAN
PG 44
CAMERA
PG 44
J4400
PATA
Conn
Pg 42
3.3 V
100 MHz
IDE
PG 23
PCI-E
PG 24
SMB
PG 25
Core
Pg 25
E-NET
PG 23
CLnk 1
PG 25
PCI
PG 24
AZALIA
PG 23
DIMM's
J3100
J3200
CLK CHIP
U2900
LEFT I/O
J3400
3 - X1
2.5 GHz
33 MHz
32-Bit
U4000
TSB83BA22
FW-Link
Pg 38
100 MHz
8-Bit
U4000
TSB83AA22
FW-PHY
Pg 39
J4300
J4310
FireWire
Conn
Pg 41
U3700
ETHERNET
(YUKON ULTRA)
Pg 35
J3900
E-NET
Conn
Pg 37
EXPRESS CARD
PG 34
EXT-C
EXT-B
USB
CONNS
PG 34
Mini PCI-E
AirPort
PG 34
U6200
Audio
Codec
Pg 59
LIO BOARD
System Block Diagram
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE
D
DRAWING NUMBER
051-7431
REV.
G
SCALE
NONE
SHT
2
OF
109

"Gloxter" POWER SYSTEM ARCHITECTURE

J6990
CRITICAL
87438-0832
PP18V5_DCIN
518S0456

J6950
CRITICAL
87438-1043
518S0457

PPDCIN_G3H

Energy Star LDO
MAX8719
U7950
(PAGE 66)
PBUS_LDO_EN
SHDN*
VIN
VOUT

Q6950
INRUSH LIMITER
(PAGE 57)
VIN
VOUT
PP18V5_G3H_CHGR
SMC_BC_ACOK
SMC_ADAPTER_EN

U5705
A
LIO_DCIN_ISENSE

PBUS SUPPLY / BATTERY CHARGER
ISL6257
U7900
(PAGE 66)
CHGR_EN
ENABLES

Q7970
BATT_POS
PPVBATT_G3H_FET_F
8A FUSE
PPVBATT_G3H_FET

BATTERY CHARGE FET
(PAGE 66)

U5715
A
LIO_BATT_ISENSE

PPVBAT_G3H_CHGR_OUT

SMC_PBUS_VSENSE
V
Q5315
PPBUS_G3H

1.5V
TPS51117
U7600
(PAGE 63)
PM_SLP_S3_DELAY_L
EN_PSV
PGOOD
(4.5A MAX CURRENT)
PP1V5_S0

1.05V
TPS51117
U7450
(PAGE 61)
PM_SLP_S3_DELAY_L
EN_PSV
PGOOD
PP1V05_S0(10A MAX CURRENT)

U5420
A
NBCORE_IOUT
PPVCORE_S0_NB_R

P1V8S3_PGOOD

SMC_CPU_VSENSE
V
U5400
A
CPUVCORE_IOUT
PPVCORE_SO_CPU
(44A MAX CURRENT)

CPUVCORE
ISL9504
U7100
(PAGE 59)
IMVP_VR_ON
VR_ON
CLKEN#
PGOOD
VR_PWRGD_CLKEN_L
VR_PWRGOOD_DELAY

SMC_GPU_VSENSE
V
U5495
A
GPUVCORE_IOUT
PPVCORE_GPU
(18A MAX CURRENT)

ISL6263B
U8900
(PAGE 75)
PM_GPUVCORE_EN
EN_PSV
PGOOD
GPUVCORE_PGOOD

U2830
VR_PWRGD_CLKEN

U2840
PM_SB_PWROK

ICH8M
U2300
VRMPWRGD
PWRBTN*
PLTRST*
RSMRST*
PWROK
CLPWROK
CPUPWRGD(GPIO49)
27
PLT_RST_L
26
CPU_PWRGD

CPU
U1000
PWRGOOD
RESET*

MCH
U1400
PWROK
HCPURST
28
FSB_CPURST_L

SMC
U4900
(PAGE 45)
10
RSMRST_OUT(P15)
PM_RSMRST_L
PWRGD(P12)
99ms DLY
IMVP_VR_ON(P16)
IMVP_VR_ON
RSMRST_IN(P13)
PLT_RST*
SMC_ONOFF_L
PWR_BUTTON(P90)
BATTERY ONLY: 05
P17(BTN_OUT)
PM_PWRBTN_L
ADAPTER IN : 08-1
RST*
PM_SLP_S5_L
PM_SLP_S5_L(P95)
PM_S4_STATE_L
PM_SLP_S4_L(P94)
PM_SLP_S3_L
PM_SLP_S3_L(P93)

U7880
P1V8P1V5P1V05S0_PGOOD
ALL_SYS_PWRGD
S0PGOOD_PWROK

LT3470
U7800
(PAGE 65)
VIN
SHDN*
VOUT
3.425V"G3HOT"
(0.2A MAX CURRENT)
PP3V42_G3H

SMC RESET "BUTTON"
RN5VD30A-F
U5000
(PAGE 46)
SMC_RESET_L

LTC2900
U7870
(PAGE 66)
1(5V)
2(3.3V)
4(1.25V)
3(1.8V)
RST*

Q7002
DELAY
R=47K
C=68NF
P5VS3_SS

Q7012
DELAY
R=100K
C=33NF
P3V3S3_SS

DELAY
R=10K
C=0.47UF
P1V8S3_EN

PM_S4_STATE_L

ICH8M
U2300
S4_STATE*

Q7851 Q7851
PM_GPUVCORE_EN
SLP_S3*
PM_SLP_S3_L

PM_SLP_S3_LS5V

GPUVCORE_PGOOD

Q7850 Q7850
PM_P1V8_S0GPU_EN

Q4261
FWPWR_EN_L_DIV

SMC_ADAPTER_EN
WOL_EN
Q3800
Q3801
PM_ENET_EN

Q3801
DELAY
R=100K
C=33NF
P3V3ENET_SS

U7850
PM_SLP_S3_DELAY_L
PP3V3_S5

Q7002
DELAY
R=47K
C=68NF
P5VS0_SS

Q7012
DELAY
R=100K
C=33NF
P3V3S0_SS

Q7096 Q7096
DELAY
R=100K
C=1UF
P1V25S0_SS

U7858
U7859
SMC_PM_G2_EN
PP3V42_G3H
5V
3.3V
TPS51120
U7300
(PAGE 60)
EN1
EN2
VOUT1
VOUT2
PGOOD
PP5V_S5
(8A MAX CURRENT)
PP3V3_S5
(5.5A MAX) CURRENT)
RSMRST_PWRGD

0.9V
1.8V
TPS511160
U7500
(PAGE 62)
PM_SLP_S3_L
S3_VTT_EN
P1V8S3_EN
S5_EN
PGOOD
PP0V9_S0
(10mA MAX CURRENT)
PP1V8_S3
(12A MAX CURRENT)
U5440
A
P1V8_S3_IOUT
PP1V8_S3_ISNS
1V8S3_PGOOD

PM_ENET_EN
TPS51117
U7400
(PAGE 61)
(6A MAX CURRENT)
PP1V25_ENET
PP1V25ENET_PGOOD
(UNUSED)

Q7095
PP1V25_S0
P1V25S0_SS

U5430
A
P1V25_S0_IOUT
PP1V25_S0_ISNS

U7860
MAX6838
(PAGE 65)
VCC
RSTIN
RST

Q7072
PM_P3V3GPU_EN
DELAY
R=100K
C=1UF
P3V3GPU_SS

ISL6269
U9300
(PAGE 79)
PM_P1V8_S0GPU_EN
EN
VOUT
PGOOD
(10A MAX CURRENT)
PP1V8_S0GPU
U5410
A
P1V8_S0GPU_IOUT
PP1V8_S0GPU_ISNS
PP_P1V8_S0GPU_PGOOD
(UNUSED)

Q4260
PPBUS_FW_FWPWRSW_F
FWPWR_EN_L_DIV
1.5A FUSE
PPVP_FW
PPVIN_FW_3V3FW

Q7000
PP5V_S3
P5VS3_SS

Q7030
PP3V3_S0
P3V3S0_SS

Q7020
PP5V_S0
P5VS0_SS
PP5V_S5

Q7070
PP3V3_GPU
P3V3GPU_SS

Q3810
PP3V3_ENET
P3V3ENET_SS

U3850
TPS79501
(PAGE 36)
IN
EN
VOUT
PP1V9_ENET

Q7010
PP3V3_S3
P3V3S3_SS

LT3470
U7700
(PAGE 64)
VIN
SHDN*
VOUT
PP3V3_FW (0.2A MAX CURRENT)
27.11UF

TPS799195
U7720
(PAGE 64)
VIN
EN
VOUT
PP1V95_FW
4.2UF

SIGNAL DELAY TIME

IMVP_VR_ON	99ms
S0PWRGD_OK	200ms
VR_PWRGOOD_DELAY	7ms

POWER ON SEQUENCE LIST

PWR/RST STATUS	STEP
G3H POWER ON	01-04
S5 POWER ON	01,05-09
S3 POWER ON	10-13
S0 SYSTEM POWER ON	14-18
S0 CPU POWER ON	17,19-24
PLATFORM,CPU RESET	25-27

STEP 06 (S5 POWER STATUS)TRUTH TABLE

NO AC/BATTERY	L(S5 OFF)
BATTERY ONLY	L(S5 OFF)
ACIN WITH/WITHOUT BATTERY	H(S5 ON)
BATTERY ONLY,PRESS PWR BUTTON	H(S5 ON)

Power Block Diagram

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 3 OF 109	

Schematic / PCB #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7431	1	SCHEM,MLB,MBP17	SCH	CRITICAL	
820-2262	1	PCBF,MLB,MBP17	PCB	CRITICAL	

Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 4 OF 109	

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9470	PCBA,2.6GHZ,512VRAM-HY,M88	M88_COMMON,CPU_2_6GHZ,FB_512_HYNIX,EEE_229
630-9471	PCBA,2.6GHZ,512VRAM-SAM,M88	M88_COMMON,CPU_2_6GHZ,FB_512_SAMSUNG,EEE_22A
630-9472	PCBA,2.5GHZ,512VRAM-HY,M88	M88_COMMON,CPU_2_5GHZ,FB_512_HYNIX,EEE_22B
630-9473	PCBA,2.5GHZ,512VRAM-SAM,M88	M88_COMMON,CPU_2_5GHZ,FB_512_SAMSUNG,EEE_22C

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9451	PCBA,2.6GHZ_STT,512VRAM-HY,M88	M88_COMMON,CPU_2_6GHZ_STT,FB_512_HYNIX,EEE_22Y
630-9446	PCBA,2.6GHZ_STT,512VRAM-SAM,M88	M88_COMMON,CPU_2_6GHZ_STT,FB_512_SAMSUNG,EEE_22X
630-9450	PCBA,2.5GHZ_STT,512VRAM-HY,M88	M88_COMMON,CPU_2_5GHZ_STT,FB_512_HYNIX,EEE_22W
630-9445	PCBA,2.5GHZ_STT,512VRAM-SAM,M88	M88_COMMON,CPU_2_5GHZ_STT,FB_512_SAMSUNG,EEE_22V

BOM Groups

BOM GROUP	BOM OPTIONS
M88_COMMON	COMMON,ALTERNATE,M88_COMMON1,M88_COMMON2,M88_DEBUG,M88_PROGPARTS
M88_COMMON1	BKLT_5V_PWR,ISL9504B,ONEWIRE_PU,GPUVID_1P23V
M88_COMMON2	P1V8S3_1V8,SMS_MOT_DIS,YUKON_ULTRA,VGA_TERM_CONN
M88_DEBUG	SMC_DEBUG_NO,XDP,LPCPLUS
M88_PROGPARTS	BOOTROM_PROG,SMC_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4,VRAM_16M,VRAM_SAMSUNG,VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4,VRAM_16M,VRAM_HYNIX,VRAM_256_HYNIX
FB_512_SAMSUNG	VRAM8,VRAM_16M,VRAM_SAMSUNG,VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM8,VRAM_16M,VRAM_HYNIX,VRAM_512_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:229]	CRITICAL	EEE_229
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:22A]	CRITICAL	EEE_22A
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:22B]	CRITICAL	EEE_22B
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:22C]	CRITICAL	EEE_22C

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:22V]	CRITICAL	EEE_22V
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:22W]	CRITICAL	EEE_22W
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:22X]	CRITICAL	EEE_22X
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:22Y]	CRITICAL	EEE_22Y

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3559	1	IC,PDC,SR,PRQ,2.6G,35W,800FSB,6M,BGA	U1000	CRITICAL	CPU_2_6GHZ
337S3560	1	IC,PDC,SR,PRQ,2.5G,35W,800FSB,6M,BGA	U1000	CRITICAL	CPU_2_5GHZ
337S3601	1	IC,PDC,SLAZA,PRQ,2.6G,35W,800FSB,6M,STT,BGA	U1000	CRITICAL	CPU_2_6GHZ_STT
337S3603	1	IC,PDC,SLAZB,PRQ,2.5G,35W,800FSB,6M,STT,BGA	U1000	CRITICAL	CPU_2_5GHZ_STT
338S0509	1	IC,GPU,NV,G84M,BGA	U8000	CRITICAL	
338S0432	1	IC,NB,CRESTLINE,GM,C0,PRQ,ROHS-SPECIAL,965PM	U1400	CRITICAL	
338S0615	1	IC,SB,ICH8M,B2,PRQ,SLB9A	U2300	CRITICAL	
353S1651	1	IC,ISL9504B,2PH IMVP6 REG,PMON,QFN48	U7100	CRITICAL	ISL9504B
359S0130	1	IC,SLG2AP101,LW PWR CLK GEN,CK505,QFN68	U2900	CRITICAL	
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	

338S0274	1	IC,SMC,HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2194	1	IC,SMC,DEVELOPMENT,M88	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2192	1	IC,EFI ROM,DEVELOPMENT,M87	U6100	CRITICAL	BOOTROM_PROG

333S0423	4	IC,SGRAM,GDDR3,16MX32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0423	8	IC,SGRAM,GDDR3,16MX32,800MHZ,136 FBGA	U8100,U8150,U8200,U8250,U8300,U8350,U8400,U8450	CRITICAL	VRAM_512_SAMSUNG
333S0424	4	IC,SGRAM,GDDR3,16MX32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
333S0424	8	IC,SGRAM,GDDR3,16MX32,900MHZ,136 FBGA	U8100,U8150,U8200,U8250,U8300,U8350,U8400,U8450	CRITICAL	VRAM_512_HYNIX

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	E&E alt to TDK/BiTech magnetics
138S0603	138S0602		ALL	Murata alt to Samnung 22uF acoustic caps
353S1681	353S1294		ALL	TI alternate to National
376S0543	376S0466		ALL	AOS alternate to Siliconix SI4413
152S0683	152S0276		ALL	Mag Layers alternate to Dale/Vishay
104S0024	104S0017		ALL	Panasonic alternate to Cyntec
128S0083	128S0165		ALL	alternate to halogen free Sanyo 330uF 2V tant
128S0113	128S0160		ALL	alternate to Halogen free Sanyo 220uF 2k mohm tant
128S0122	128S0157		ALL	alternate to Halogen free Sanyo 220uF 1k mohm tant
128S0057	128S0147		ALL	alternate to Halogen free Sanyo 100uF tant
128S0056	128S0175		ALL	alternate to Halogen free Sanyo 330uF 6V tant
376S0448	376S0445		ALL	SiI7000ADB for FSM6206

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE	SHT	OF
NONE	5	109

Proto:

See earlier schematics for info about releases 0.0.1 - 4.0.0

EVT:

5.0.0:
08/03/07 -- Page 5: Removed Q4690 BOM table entry. BOM table is on CSA pg. 46
6.0.0 & 5.1.0:
08/10/07 -- Synced to M87 MLB label 4.3.0
08/10/07 -- Page 3: Revised power block diagram.
08/10/07 -- Page 10-12: Updated U1000 CPU part number to reflect latest Penryn pin-out.
08/10/07 -- Page 37: T3900,T3901 magnetics changed to 157S0053.
08/10/07 -- Page 65: Changed L7810 3.425V G3 Hot inductor to 152S0301. R7070 changed from 100K to 10K.
6.1.0:
08/14/07 -- Synced to M87 MLB label 5.1.0
08/14/07 -- Page 49: Changed Q5322 to SOT23 part same as M87.
08/14/07 -- Page 75: Changed GPU VID pull up/downs to 2.2K ohms.
6.2.0:
08/16/07 -- Removed Rev B Silego clock chip as alternate.
08/16/07 -- Page 51: Temp Sensors: Changed U5500 and U5570 to EMC1043-1 APN 353S1947.
7.0.0:
08/17/07 -- Page 48: Changed SMBus SMC "A" pull ups R5270 and R5271 to 3.3K to improve rise time on SCL..
7.1.0:
08/22/07 -- Page. 9,34: Added GPIOs to support iPhone headset. ICH8 GPIO 22 IPHS_SW_BIAS_EN_L routes to JJ3400.63
08/22/07 -- Page. 9,34: Removed R3410 and R3411. ICH8 GPIO 2 IPHS_SW_INT routes to JJ3400.65
08/22/07 -- Synced M87 MLB label 6.2.0
08/22/07 -- Page 51: Temp sensors: Added R5501,R5502,R5571,R5572 pull ups on U5500 and U5570.
08/22/07 -- Page 61: R7455 changed to 7.5K to change max load current margin on PP1V05.
08/22/07 -- Page 90: Changed frame buffer net physical type to GDDR3_50SE.
08/22/07 -- Synced M87 LIO label 1.5.0
08/22/07 -- Page 66: U7901 voltage follower changed from OPA333 to OPA705.
08/22/07 -- Page 82: Changed L9891,L9893,L9894 to 155S0220
7.2.0:
08/23/07 -- Page 5: Changed CPU parts to ES2, B1 for EVT
08/23/07 -- Page 9: IPHS_SW_BIAS_EN_L now connected to SB_SLOAD (GPIO 38).
08/23/07 -- Synced M87 MLB label 6.5.0
08/23/07 -- Page 50: Current Sensors: Changed U5410 and U5440 to MAX4245 Changed R5413 and R5443 to 0.005 ohm resistors.
08/23/07 -- Page 91: Added diff pair properties to new current sensor pairs.
08/23/07 -- Synced M87 LIO label 1.7.0
08/23/07 -- Page 66: Changed U7901 to MAX4245. Changed F7902 to 740S0055.
08/23/07 -- Page 82: Add BOMOPTION OMIT to RX9892.
8.0.0:
08/24/07 -- Page 25: Added NO STUFF to R2552 (was pull up on SB GPIO38 which is now used on IPHS).
08/24/07 -- Page 59: CPU Vcore supply changes per characterization. Changed L7100 and L7101 to 152S0624. Changed C7134 to 0.01uF 132S0042.
8.1.0:
08/24/07 -- Synced M87 MLB label 8.2.0
Page 5,75: Changed BOM option to GPUVID_1P23V
Page 73: Changed R5491 and R5493 to 6.81K to allow full resolution of GPUVCORE current sense
Page 50: Adding C5411,C5412,C5441,C5442 feedback caps for current sense op amps
Page 66: Changed R7920 to halogen free 107S0110.
8.2.0:
08/29/07 -- Synced m87_mlb CSA pgs. Major release label name : m87_mlb_051-7413_8.2.0
08/29/07 -- Changed net physical and net spacing to CRT_50S on these signals NB_CLK100M_DPLSS_P/N NB_CLK96M_DOT_P/N
8.3.0:
08/29/07 -- Changed the following filters to 155S0371 for supply issues: pg. 43 L4600 pg. 44 FL4735 pg. 76 L9010,L9011
08/29/07 -- pg. 80 L9460,L9464,L9468,L9476,L9480,L9484
8.4.0:
08/30/07 -- Changed the orientation on these filters to match layout: pg. 43 L4600 pg. 76 L9010,L9011
9.0.0:
08/30/07 -- RFA 529050 EVT Release of Schematic BOM and PCBF
9.1.0: BOM Changes only
09/04/07 -- Page 5: Added alternate sources for these parts:
09/04/07 -- 152S0683 is the Mag layers alternate for Dale/Vishay inductors.

09/04/07 -- 128S0164 is the Kemet alternate to Sanyo caps
09/04/07 -- 104S0023 is the Panasonic alternate to Cyntec resistors
09/04/07 -- Page 50: Changed R5425 and R5435 to 104S0023.
10.0.0:
09/06/07 -- HF capacitor substitution, with halogen parts as alternates. pg. 5 Alternates BOM table updates.
11.0.0:
09/11/07 -- Page 57: Removed NO STUFF from DZ6960 (377S0044), ESD diode on BATT_POS per Chris.
09/11/07 -- Page 5: Removed alternate to 128S0164 Kemet 220uF tantalum cap at C7540 and C7541.
09/11/07 -- Added BOM variants and EEE codes for 2.5GHz:
09/11/07 -- 630-9225: ZVW PCBA,2.5GHZ,512VRAM-HY,M88
09/11/07 -- 630-9228: ZVX PCBA,2.5GHZ,512VRAM-SAM,M88
09/11/07 -- Page 62: Removed OMIT property and BOM option table to make C7540 and C7541 only 128S0073.
09/11/07 -- Page 82: LCD Backlight Added OMIT properties and BOM option table to change these beads to 155S0220: L9891,L9893,L9894

DVT:

11.1.0:
09/12/07 -- Page 66: Swapped U7901 pins 1 and 3 signals (positive and negative inputs).
11.2.0:
09/26/07 -- Synced M*& MLB label 10.2.0
09/26/07 -- Page 50 & 75: GPUVCORE: Current sense to use IMVP6 IMON + Non-inverting Opamp removed R8992,C8992
09/26/07 -- Page 65: Changed C7860 to 0.0047uF (radar://5468257
12.0.0:
09/28/07 -- Removed BOM tables and OMIT BOM options from HF capacitor substitution, with halogen parts as alternates.
09/28/07 -- Synced M87 MLB label 10.3.0
09/28/07 -- Page 50: updating GPUVcore current sense resistor values for gain of 4.83
12.0.0:
10/01/07 -- Synced M87 LIO label 9.0.0 Added R9810
10/01/07 -- Synced M87 LIO label 7.0.0
10/01/07 -- <rdar://problem/5493576> M87/M88 MLB/LED: LED driver current mirror can not be disabled + power sequencing issue
<rdar://problem/5510696> TASK: M87 LIO changes to support LED board
10/01/07 -- Page 5: Added 376S0448 as alternate for 376S0445.
13.0.0:
10/05/07 -- Page 5: Removed HDCP ROM. Removed U8770, R8770,R871, C8770.
10/05/07 -- Page 75: GPU Vcore supply: Changed L8920 from 152S0525 to 152S0697.Dale 0.9uH 27A inductor has smaller pad size than Vishay IHLP4040.
13.1.0:
10/09/07 -- Synced m87_MLB label Change 72968 Page 5: Changed Module parts for new Penryn APNs.
10/09/07 -- Page 93: <rdar://problem/5525486> M87/88 1V8 FB DC converter transient response improve/BOM change
10/09/07 -- R9308 change to 40.2k, 0402, 1%; C9308 change to 680pF, 0402, 10V, 10% C9307 change to 68pF, 0402, 10V, 10%

DVT (cont):

14.0.0:
10/12/07 -- Page 81: Added FL9600 155S0372 to multi-touch trackpad power and GND.
10/12/07 -- Synced M87_MLB label: 12.1.0
10/12/07 -- Page 46: Changed to new Sleep LED circuit Deleted, Q5032,R5032,R5030 Added, C5030 Changed Q5030 to new LED Driver IC
10/12/07 -- Synced M*&_LIO label: 10.0.0
10/12/07 -- Changed R9807 to 5.1k Changed C9807 to 0.1uF Changed R9809 to 200k
14.1.0:
10/19/07 -- Synced M87_MLB label: 12.2.0 Page 50: Named unnamed net on Q5030.
10/19/07 -- Page 69: NO STUFF battery positive terminal varistor DZ6960
14.5.0:
10/24/07 -- Page 43: Changed L4605 ferrite bead to 155S0329 for lower DCR.
10/24/07 -- Page 57: Changed DZ6960-DZ6963 to 377S0068. These are NO STUFFs.
10/24/07 -- Page 90: Graphics constraints Changed all GDDR3_46SE constraints back to GDDR3_50SE.
16.0.0:
11/01/07 -- Page 53: Changed U5750 TMP102 to RevE part 353S2039 with old part 353S1807 as alternate.
11/01/07 -- Page 59: CPU Vcore power supply change C7134 to 0.022uF 132S0102 per Dayu
17.0.0:
11/06/07 -- Page 25: Removed NO STUFF BOM option from R2552, pull up on SB GPIO38.
11/06/07 -- Synced M87_LIO label 14.0.0 pg. 82 Changed C9805 to 2.2uF for LED power sequencing.

PVT:

18.0.0:
12/10/07 -- Page 98: Changed R9808 to 200K, R9809 to 100K, C9802 to 0.033uF, C9807 to 0.33uF to improve Q9806 Vgs and sequencing
18.1.0:
12/12/07 -- Page 5: Updated CPUs to PRQ parts, removed XDP_CONN and GPU_TMP401 bom options and changed to SMC_DEBUG_NO for PVT
12/12/07 -- Page 50: Removed ST SIL driver and returned to EVT's BJT-driven current source
12/12/07 -- Page 98: Changed C9805 to actual 2.2uF part (removed table entry)
18.2.0:
12/13/07 -- Page 13: NO STUFFed R1330/R1331 since the LVDS_CTRL_DATA/CLK lines are grounded
18.3.0:
12/16/07 -- Page 54: Added C8992/R8992 to provide differential sense option
A.0.0:
12/18/07 -- Release as Rev A (Rev A NOT BUILT!!!)
A.1.0:
12/19/07 -- Fixed grounded I2C bus on mini-XDP connector
C.0.0:
02/01/08 -- Changed R9805, R9810 to 100K to fix panel enable timing issue
D.0.0:
02/17/08 -- Backed out C.0.0 change (changed R9805, R9810 to back 51.1K).

E.0.0:
02/17/08 -- All new 630s to properly implement the D.0.0 changes
F.0.0:
02/26/08 -- Added new 630s to control new CPUs that are screened for therm trip
02/26/08 -- Removed 128S0115 as alternate to 128S0150
F.0.0:
06/06/08 -- Changed ICH8M from B1 to B2 part (APN: 338S0615)

www.laptop-schematics.com

G

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 6 OF 109	

Functional Test Points

Fan Connectors

FUNC_TEST

I498	TRUE	=PP5V_S0_FAN_LT	8 52
I497	TRUE	FAN_LT_PWM	52
I496	TRUE	FAN_LT_TACH	52
I495	TRUE	FAN_RT_PWM	52
I494	TRUE	FAN_RT_TACH	52

LPC+ Debug Connector

FUNC_TEST

I490	TRUE	=PP3V3_S5_LPCPLUS	8 47
I491	TRUE	=PP5V_S0_LPCPLUS	8 47
I492	TRUE	LPC_AD<0>	23 45 47
I493	TRUE	LPC_AD<1>	23 45 47
I422	TRUE	LPC_FRAME_L	23 45 47
I423	TRUE	PM_CLKRUN_L	25 45 47
I492	TRUE	BOOT_LPC_SPI_L	24 47
I421	TRUE	SMC_TMS	45 46 47
I420	TRUE	DEBUG_RESET_L	28 47
I419	TRUE	SMC_TRST_L	45 47
I418	TRUE	SMC_TDO	45 46 47
I417	TRUE	SMC_MD1	45 47
I416	TRUE	SMC_TX_L	43 45 46 47
I415	TRUE	FWH_INIT_L	47
I414	TRUE	PCI_CLK33M_LPCPLUS	30 47 88
I413	TRUE	LPC_AD<2>	23 45 47
I412	TRUE	LPC_AD<3>	23 45 47
I411	TRUE	INT_SERIRQ	25 45 47
I410	TRUE	PM_SUS_STAT_L	25 45 46 47
I409	TRUE	SMC_TDI	45 46 47
I408	TRUE	SMC_TCK	45 46 47
I407	TRUE	SMC_RESET_L	45 46 47
I406	TRUE	SMC_NMI	45 47
I405	TRUE	SMC_RX_L	43 45 46 47
I403	TRUE	LINDACARD_GPIO	25 47

Left ALS

FUNC_TEST

I448	TRUE	ALS_GAIN	34 45 54
I447	TRUE	LTALS_OUT	34 54
	TRUE	GND	

Thermal Diode Connectors

FUNC_TEST

I568	TRUE	HSTHMSNS_D_P	51 91
I567	TRUE	HSTHMSNS_D_N	51 91
I443	TRUE	RSFSTHMSNS_D_P	51 91
I442	TRUE	RSFSTHMSNS_D_N	51 91
I520	TRUE	CPUTHMSNS_D2_P	51 91
I521	TRUE	CPUTHMSNS_D2_N	51 91

Battery Digital Connector

FUNC_TEST

I606	TRUE	SMC_BS_ALRT_L	45 46 57
I607	TRUE	=SMBUS_BATT_SCL	48 57
I608	TRUE	=SMBUS_BATT_SDA	48 57
I641	TRUE	=BATT_POS	57 66
I636	TRUE	=BATT_NEG	57 66
	TRUE	GND (HOST_DETECT_L)	

Left I/O Power Connector

FUNC_TEST

I629	TRUE	PP18V5_DCIN	57	Request for 2 test points
I430	TRUE	=PPBUS_G3H_LIO_CONN	8 57	Request for 3 test points
	TRUE	GND		

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

RTC Battery Connector

FUNC_TEST

I634	TRUE	PPVBATT_G3_RTC	28
	TRUE	GND	

Current Sense Calibration

FUNC_TEST

I431	TRUE	ISENSE_CAL_EN	45 49
I430	TRUE	=PP5V_S0_ISENSECAL	8 49
I427	TRUE	=PPVCORE_S0_CPU_REG	8 49 59
I426	TRUE	=PPVCORE_GPU_REG	8 49 75
	TRUE	GND	

2 TPs per

6 TPs, 2 with each of above TP pairs

Backlight Connector

FUNC_TEST

I632	TRUE	BKLT_PWR	81 82
I632	TRUE	BKLT_GND	81 82
I638	TRUE	BKLT_P5V_EN	81 82
I638	TRUE	BKLT_PWM	81 82
	TRUE	GND	

Left Clutch Barrel Connector

FUNC_TEST

I636	TRUE	PP5V_S3_CAMERA_F	44
I614	TRUE	USB_CAMERA_F_N	44 91
I616	TRUE	USB_CAMERA_F_P	44 91

IR & Sleep LED Connector

FUNC_TEST

I630	TRUE	=PP5V_S3_IR	8 81
I640	TRUE	USB_IR_N	24 81 86
I642	TRUE	USB_IR_P	24 81 86
I644	TRUE	SYS_LED_ANODE	46 81
	TRUE	GND	

Other Func Test Points

FUNC_TEST

I433	TRUE	PM_SYSRST_L	25 28 45
I432	TRUE	SMC_ONOFF_L	45 46 81

System Validation TPs

FUNC_TEST

	TRUE	CPU_PWRGD	10 13 23 83
	TRUE	CPU_DPSLP_L	7 10 23 83
	TRUE	PM_DPRSLPVR	16 25 59 83
	TRUE	CPU_DPSLP_L	7 10 23 83
	TRUE	PM_LAN_ENABLE	25 45
	TRUE	PCI_RST_L	24 28
	TRUE	PM_RSMRST_L	25 45
	TRUE	PM_SB_PWROK	9 25 28
	TRUE	SB_RTC_RST_L	23 28
	TRUE	PM_STPCPU_L	25 29 30
	TRUE	PM_STPPCI_L	25 29 30
	TRUE	VR_PWRGD_CLKEN	25 28
	TRUE	VR_PWRGOOD_DELAY	9 16 28 59
	TRUE	FSB_CPURST_L	10 13 14 83
	TRUE	FSB_CPUSLP_L	10 14 83
	TRUE	FSB_DPWR_L	10 14 83
	TRUE	NB_SB_SYNC_L	16 25
I561	TRUE	PM_BMBUSY_L	16 25

FUNC_TEST

	TRUE	IMVP_VR_ON	45 59
	TRUE	IMVP_DPRSLPVR	59 83
	TRUE	PM_SLP_S3_L	25 36 40 45 65
	TRUE	PM_S4_STATE_L	25 45 65
	TRUE	PM_SLP_S5_L	25 45 46
	TRUE	PM_ENET_EN	36 65
	TRUE	P1V8P1V5P1V05S0_PGOOD	65
	TRUE	CPU_DPRSTP_L	10 16 23 59 83
	TRUE	IMVP6_VID<6..0>	12 59 83
	TRUE	FSB_CLK_CPU_N	10 30 88
	TRUE	FSB_CLK_CPU_P	10 30 88
	TRUE	PLT_RST_L	9 24 28
	TRUE	NB_RESET_L	16 28
	TRUE	GPU_RESET_L	28 67
	TRUE	SMC_LRESET_L	28 45
	TRUE	CPU_STPCLK_L	10 23 83
	TRUE	FSB_CLK_NB_P	14 30 88
	TRUE	FSB_CLK_NB_N	14 30 88
	TRUE	NB_CLKREQ_L	16 29
	TRUE	NB_CLK100M_PCIE_P	16 30 88
	TRUE	NB_CLK100M_PCIE_N	16 30 88
	TRUE	CPU_THERMTRIP_R	23

ICT Test Points

CPU FSB NO_TESTs

MAKE BASE — NO_TEST

I638	TRUE	FSB_A_L<31..3>	10 14 83
I557	TRUE	FSB_ADS_L	10 14 83
I556	TRUE	FSB_ADSTB_L<1..0>	10 14 83
I555	TRUE	FSB_BNR_L	10 14 83
I554	TRUE	FSB_BREQ0_L	10 14 83
I552	TRUE	FSB_D_L<63..0>	10 14 83
I553	TRUE	FSB_DBSY_L	10 14 83
I636	TRUE	FSB_DINV_L<3..0>	10 14 83
I551	TRUE	FSB_DRDY_L	10 14 83
I640	TRUE	FSB_DSTB_L_N<3..0>	10 14 83
I647	TRUE	FSB_DSTB_L_P<3..0>	10 14 83
I648	TRUE	FSB_HIT_L	10 14 83
I649	TRUE	FSB_HITM_L	10 14 83
I634	TRUE	FSB_LOCK_L	10 14 83
I646	TRUE	FSB_REQ_L<4..0>	10 14 83
I672	TRUE	NC_CPU_RSVD5 — TP_CPU_RSVD5	10

NB NO_TESTs

MAKE BASE — NO_TEST

I655	TRUE	NC_NB_NC<1..16>	TP_NB_NC<1..16>	16
I566	TRUE	NC_NB_RSVD<26..27>	TP_NB_RSVD<26..27>	16
I670	TRUE	NC_NB_RSVD<24>	TP_NB_RSVD<24>	16

www.laptop-schematics.com

Functional / ICT Test

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 7 OF 109	

www.laptop-schematics.com

"G3Hot" (Always-Present) Rails

=PPVBAT_G3H_CHGR_REG → PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
- =PPBUS_S5_FWPWRSW 40
- =PPVIN_S5_CPU_IMVP_VIN 59
- =PPVIN_S5_CPU_IMVP 59
- =PPVIN_S5_P5VP3V3 60
- =PPVIN_S5_P5VS5 60
- =PPVIN_S5_P3V3S5 60
- =PPVIN_ENET_P1V25ENET 61
- =PPVIN_S3_P1V8S3 62
- =PPVIN_S0_P1V5S0 63
- =PPBUS_S0_LCDBKLT 82
- =PPVIN_S0_P1V8FB 79
- =PPVIN_S0_P1V05S0 61
- =PPVIN_GPU_GPUVCORE 75
- =PPBUS_G3H_LIO_CONN 7 57
- =PPBUS_S5_P1V25S0FET 58

=PPDCIN_G3H → PPDCIN_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPVIN_G3H_P3V42G3H 65
- =PPVBATT_G3H_LIO_CONN 66

=PP3V42_G3H_REG → PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V42_G3H_SB_RTC 28
- =PP3V42_G3H_ACIN 57 66
- =PP3V42_G3H_SMCUSBMUX 43
- =PP3V42_G3H_SMBUS_SMC_BSA 48
- =PP3V42_G3H_LIDSWITCH 81
- =PP3V3_S5_SMC 45 46
- =PP3V3_S5_LPCPLUS 7 47
- =PPVIN_S5_SMCVREF 46
- =PP3V42_G3H_PWRCTL 65

5V Rails

=PP5V_S5_REG → PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S5_SB 27
- =PP5V_S5_P1V8FB 79
- =PP5V_S5_P1V25S0FET 58
- =PP5V_S5_P1V25ENET 61
- =PP5V_S5_P1V05S0 61
- =PP5V_S5_P1V8DDRREG 62
- =PP5V_S5_P1V5S0 63
- =PP5V_S5_PWRCTL 65
- =PP5V_S5_GPUVCORE 75
- =PP5V_S3_RTUSB 43
- =PP5V_S3_P5VS3FET 58
- =PP5V_S0_P5VS0FET 58
- =PP5V_S0_ODD 42

=PP5V_S3_FET → PP5V_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S3_SYSLED 46
- =PP5V_S3_CAMERA 44
- =PP5V_S3_IR 7 81
- =PP5V_S3_TOPCASE 81

=PP5V_S0_FET → PP5V_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_SB 27
- =PP5V_S0_ODDPWREN 42
- =PP5V_S0_LPCPLUS 7 47
- =PP5V_S0_ISENSECAL 7 49
- =PP5V_S0_FAN_LT 7 52
- =PP5V_S0_FAN_RT 52
- =PP5V_S0_KBDLED 54
- =PP5V_S0_CPU_IMVP 59
- =PP5V_S0_LCDBKLT 82
- =PP5V_S0_DVI_DDC 80
- =PP5V_S0_HDD 81
- =PP5V_S0_PCIREQFIX 42

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG → PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU 11 12 49
- =PPVCORE_S0_NB_GFX 18

3.3V-2.5V Rails

=PP3V3_S5_REG → PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V3_S5_SB_PM 28
- =PP3V3_S5_SB_USB 24
- =PP3V3_S5_SB 25 27
- =PP3V3_S5_SB_CLINK1 25
- =PP3V3_S5_SB_GPIO 25
- =PP3V3_S5_SB_3V3_VCCSUSHDA 26 27
- =PP3V3_S5_SB_VCCSUS3_3 26 27
- =PP3V3_S5_SB_VCCSUS3_3_USB 26 27
- =PP3V3_S5_S5PWRGD 46
- =PP3V3_S5_SMBUS_SB_ME 48
- =PP3V3_S5_ROM 56
- =PP3V3_S5_P1V5P1V05PG 65
- =PP3V3_S5_PWRCTL 65
- =PP3V3_S3_P3V3S3FET 58
- =PP3V3_S0_P3V3S0FET 58
- =PP3V3_S0_LCD 76
- =PP3V3_GPU_P3V3GPUFET 58

=PP3V3_S3_FET → PP3V3_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S3_P3V3ENETFET 36
- =PP3V3_S3_FW 38
- =PP3V3_S3_PCI 38
- =PP3V3_S3_SMBUS_SMC_A_S3 48
- =PP3V3_S3_RTALS 54
- =PP3V3_S3_SMS 55
- =PP3V3_S3_BT 81
- =PP3V3_S3_TOPCASE 81
- =PP3V3_S3_SMBUS_SMC_MGMT 48
- =PP3V3_S3_P1V8ISNS 50
- =PP3V3_S3_REMTHMSNS 51
- =PP3V3_S3_PWRCTL 65

=PP3V3_S0_FET → PP3V3_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S0_NB_VCCHV 16 19 21
- =PP3V3_S0_NB_VCCA_PEG_BG 19 21
- =PP3V3_S0_NB_FOLLOW 21
- =PP3V3_S0_SB_GPIO 23 25
- =PP3V3_S0_SB_PCI 24
- =PP3V3_S0_SB_VCC3_3_IDE 26 27
- =PP3V3_S0_SB_VCC3_3_PCI 26 27
- =PP3V3R1V5_S0_SB_VCCHDA 26 27
- =PP3V3_S0_SB_VCC3_3_DMI 26 27
- =PP3V3_S0_SB_VCC3_3_VCCPCORE 26
- =PP3V3_S0_SB_VCCGLAN3_3 26
- =PP3V3_S0_SB_VCC3_3_SATA 26 27
- =PP3V3_S0_SB 27
- =PP3V3_S0_SB_PM 28
- =PP3V3_S0_RSTBUF 28
- =PP3V3_S0_CK505 29 30
- =PP3V3_S0_IDE 42
- =PP3V3_S0_SMC 46
- =PP3V3_S0_LPCPLUS 47
- =PP3V3_S0_SMBUS_SB 48
- =PP3V3_S0_SMBUS_SMC_B_S0 48
- =PP3V3_S0_CPUCOREISNS 50
- =PP3V3_S0_GPU1V8ISNS 50
- =PP3V3_S0_P1V25ISNS 50
- =PP3V3_S0_CPUTHMSNS 51
- =PP3V3_S0_GPUTHMSNS 51
- =PP3V3_S0_FAN_LT 52
- =PP3V3_S0_FAN_RT 52
- =PP3V3_S0_IMVP 59
- =PP3V3_S0_NBCOREISNS 50
- =PP3V3_S0_ALLSYSPG 65
- =PP3V3R5V_GPU_GPUISENS 50
- =PP3V3_S0_XDP 13
- =PP3V3_S0M_CK505 29 30
- =PPSPD_S0M_MEM_A 31
- =PPSPD_S0M_MEM_B 32
- =PP3V3_S0MWOL_SB_CLINK0 25
- =PP3V3_S0MWOL_SB_VCCCL3_3 26 27
- =PP3V3_S0MWOL_SB_VCCLAN3_3 26 27
- =PP3V3_S0_PBATTISENS 53
- =PP3V3_S0_PDCISENS 53
- =PP3V3_S0_TMPSNSR 53
- =PP3V3_S0_PWRCTL 65
- =PP3V3_S0_LCDBKLT 82

=PP1V25_S0_FET → PP1V25_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V25_S0_ISNS_R 50

1.8V-0.9V Rails

=PP1V8_S3_REG → PP1V8_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S3_FW 38
- =PP1V8_S3M_MEM_A 31 91
- =PP1V8_S3M_MEM_B 32 91
- =PP1V8_S3_ISNS_R 50

=PP1V8_S3_ISNS → PP1V8_S3_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S3M_MEM_NB 16 18 21
- =PP1V8_S3M_NB_VCC 21

=PP1V5_S0_REG → PP1V5_S0
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
MAX I = ?.??A
- =PP1V5_S0_CPU 11 12
- =PP1V5_S0_NB_TVDAC 22
- =PP1V5_S0_SB 27
- =PP1V5_S0_SB_VCC1_5_A_ARX 26 27
- =PP1V5_S0_SB_VCC1_5_A_ATX 26 27
- =PP1V5_S0_SB_VCC1_5_A 26
- =PP1V5_S0_SB_VCCUSBPLL 26 27
- =PP1V5_S0_SB_VCC1_5_A_USB_CORE 26 27
- =PP1V5_S0_LIO 34

=PP1V25_S0_ISNS → PP1V25_S0_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V25_S0M_NB_PLL 21
- =PP1V25_S0M_NB_VCC 21
- =PP1V25_S0M_NB_VCCA 21
- =PP1V25_S0_NB_VCCDMI 19 21
- =PP1V25_S0_NB_PLL 21
- =PP1V25_S0_NB_VCC 21
- =PP1V25_S0_SB_DMI 26 27
- =PP1V2_GPU_PEX_IOVDDQ 67
- =PP1V2_GPU_PEX_IOVDD 67
- =PP1V2_GPU_PEX_PLLXVDD 67
- =PP1V2_GPU_PLLVDD 72
- =PP1V2_GPU_H_PLLVDD 72
- =PP1V2_GPU_VID_PLLVDD 72
- =PP1V2_GPU_FBPLLAVDD 69

=PP1V05_S0_REG → PP1V05_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0M_NB_VCCAXM 18 21
- =PP1V05_S0_CPU 10 11 12 13
- =PP1V05_S0_NB_FOLLOW 21
- =PP1V05_S0_NB_PCIE 21
- =PP1V05_S0_SB_CPU_IO 23 26 27
- =PP1V05_S0_SMC_LS 46
- =PP1V25R1V05_S0_FSB_NB 14 30
- =PP1V25R1V05_S0_NB_VTT 19 21
- =PPVCORE_S0_NBCOREISNS 50
- =PPVCORE_S0_NB_FOLLOW 21
- =PPVCORE_S0_SB 26 27

=PPVCORE_S0_NB_R → PPVCORE_S0_NB_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PPVCORE_S0_NB 18 21

=PP0V9_S3_VTTR_BUF → PP0V9_S3_MEM_VREF
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PP0V9_S3M_MEM_NBVREFA 16
- =PP0V9_S3M_MEM_NBVREFB 16
- =PP0V9_S3M_MEM_DIMMVREFA 31
- =PP0V9_S3M_MEM_DIMMVREFB 32

=PP0V9_S0_VTT_LDO → PP0V9_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PP0V9_S0M_MEM_TERM 33

"ENET" Rails

=PP3V3_ENET_FET → PP3V3_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_ENET_PHY 35
- =PP3V3_ENET_AVDDLDO 36

=PPVOUT_ENET_AVDDLDO → PP1V9_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.9V
MAKE_BASE=TRUE
- =PP1V8R2V5_ENET_PHY 35

=YUKON_EC_PP2V5_ENET
Yukon EC will not be supported

=PP1V25_ENET_REG → PP1V25_ENET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PP1V2_ENET_PHY 35
- =PP1V25_S0_P1V25S0FET 58

"FW" (FireWire) Rails

=PPBUS_FW_FWPWRSW_F → =PPBU_S0_P3V3FW 64
MAKE_BASE=TRUE

=PPBUS_S5_FW_FET → PPVP_FW
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PPVP_FW_SUMNODE 40
- =PPVP_FW_CPS 39
- =PPVP_FW_P3V3FW 64

PPVP_FW_PORTA_UF → =PPVP_FW_PORT0 41
MAKE_BASE=TRUE

PPVP_FW_PORTB_UF → =PPVP_FW_PORT1 41
MAKE_BASE=TRUE

=PP3V3_FW_REG → PP3V3_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_FW_PHY 39 41
- =PP3V3_FW_LATEVG_ACTIVE 40
- =PP3V3_FW_LATEVG 41
- =PPVIN_FW_P1V95FW 64

=PP1V95_FW_LDO → PP1V95_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.95V
MAKE_BASE=TRUE
- =PP1V95_FW_PHY 39
- =PP1V8_FW_PHYOSC 39

"GPU" Rails

=PP3V3_S0GPU_FET → PP3V3_S0GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_GPU_VDD33 72
- =PP3V3_GPU_MIO 72 73
- =PP3V3_GPU_DAC 74
- =PP3V3_GPU_DVI 80
- =PP3V3_S0_DDC_LCD 76
- =PP3V3_GPU_VGASYNC 80
- =PP3V3_GPU_TMDS 73
- =PP3V3_GPU_VIDEOMUX 73
- =PP3V3_GPU_SMBUS_SMC_0_S0 48
- =PP3V3_GPU_PWRCTL 65
- =PP3V3_GPU_VCORELOGIC 75
- =PP3V3_GPU_HDCP 73

=PP3V3_S0GPU_TMDS_FET → PP3V3_S0GPU_TMDS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_GPU_TMDSBIAS 80
- =PP3V3_GPU_IFPCD_IOVDD 74

=PP1V8_S0GPU_REG → PP1V8_S0GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S0GPU_ISNS_R 50

=PP1V8_S0GPU_ISNS → PP1V8_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_GPU_FB_VDD 70 71 77 78
- =PP1V8_GPU_FB_VDDQ 70 71 77 78
- =PP1V8_GPU_FBVDDQ 68
- =PP1V8_GPU_FBIO 69
- =PP1V8_GPU_IFPX 74

=PPVCORE_GPU_REG → PPVCORE_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
- =PPVCORE_GPU 68

Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 8 OF 109	

www.laptop-schematics.com

TP_USB_EXTDN — USB_EXTD_N (BI) 24 86
MAKE_BASE=TRUE

TP_USB_EXTDP — USB_EXTD_P (BI) 24 86
MAKE_BASE=TRUE

28 25 7 PM_SB_PWROK — =SB_CLINK_MPWROK 25
MAKE_BASE=TRUE

59 28 16 7 VR_PWRGOOD_DELAY — =NB_CLINK_MPWROK 16
MAKE_BASE=TRUE

67 30 PEG_CLK100M_GPU_P — PEG_CLK100M_P 88
MAKE_BASE=TRUE

67 30 PEG_CLK100M_GPU_N — PEG_CLK100M_N 88
MAKE_BASE=TRUE

55 SMC_SMS_INT — =SMC_SMS_INT 45
MAKE_BASE=TRUE

TP_EXTGPU_PWR_EN — EXTGPU_PWR_EN 23
MAKE_BASE=TRUE

25 SB_SLOAD — IPHS_SW_BIAS_EN_L 34
MAKE_BASE=TRUE

24 INT_PIRQE_L — IPHS_SW_INT 34
MAKE_BASE=TRUE

46 SMC_ENRGYSTR_LDO_EN — PBUS_LDO_EN 66

TP_MEM_A_A<15> — MEM_A_A<15> 31
MAKE_BASE=TRUE

TP_MEM_B_A<15> — MEM_B_A<15> 32
MAKE_BASE=TRUE

28 24 7 PLT_RST_L — =BKLT_PLT_RST_L 82

73 GPU_BL_PWM — =BKLT_PWM 82

73 GPU_BKLT_EN — =BKLT_EN 82

Thermal Module Holes

All holes are plated through holes with two exceptions:

GND_CHASSIS_RIGHT_FAN_NOTCH (to the left of small well on lower board edge near USB)
GND_CHASSIS_BATTCONN_HOLE (to the left of DIMM cutout near board edge)

Top CPU TM "Hole"
Add 8 blind vias per side to GND

ZT0970 195R106 — Left CPU TM Hole
ZT0975 195R106 — Right CPU TM Hole
ZT0980 195R106 — Bottom Left GPU TM Hole
Top Right GPU TM Hole
ZT0985 195R106

Chassis GNDs

ZT0901 195R106 — GND_CHASSIS_RBIO
ZT0900 195R106 — GND_CHASSIS_RTIO

Digital Ground

GND
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V

RAM door (Torx) holes

ZT0930 235R126 — GND_CHASSIS_RAMDOOR_HOLE_0
ZT0935 235R126 — GND_CHASSIS_RAMDOOR_HOLE_1
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V

Frame holes

GND_CHASSIS_RIGHT_FAN_HOLE
GND_CHASSIS_RIGHT_FAN_NOTCH
GND_CHASSIS_DIMM_NOTCH
ZT0955 195R106 — GND_CHASSIS_LIOFLEX_HOLE
GND_CHASSIS_BATTCONN_HOLE
ZT0965 195R106 — GND_CHASSIS_LNDACARD_HOLE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V

Chassis connection to be made at the mounting hole east of the LVDS connector

GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V
MAKE_BASE=TRUE

=GND_CHASSIS_BKLT
GND_CHASSIS_BACKLIGHT

SH0925 OG-503040 SHLD-SM-LF (1, 2, 3)

Signal Aliases

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

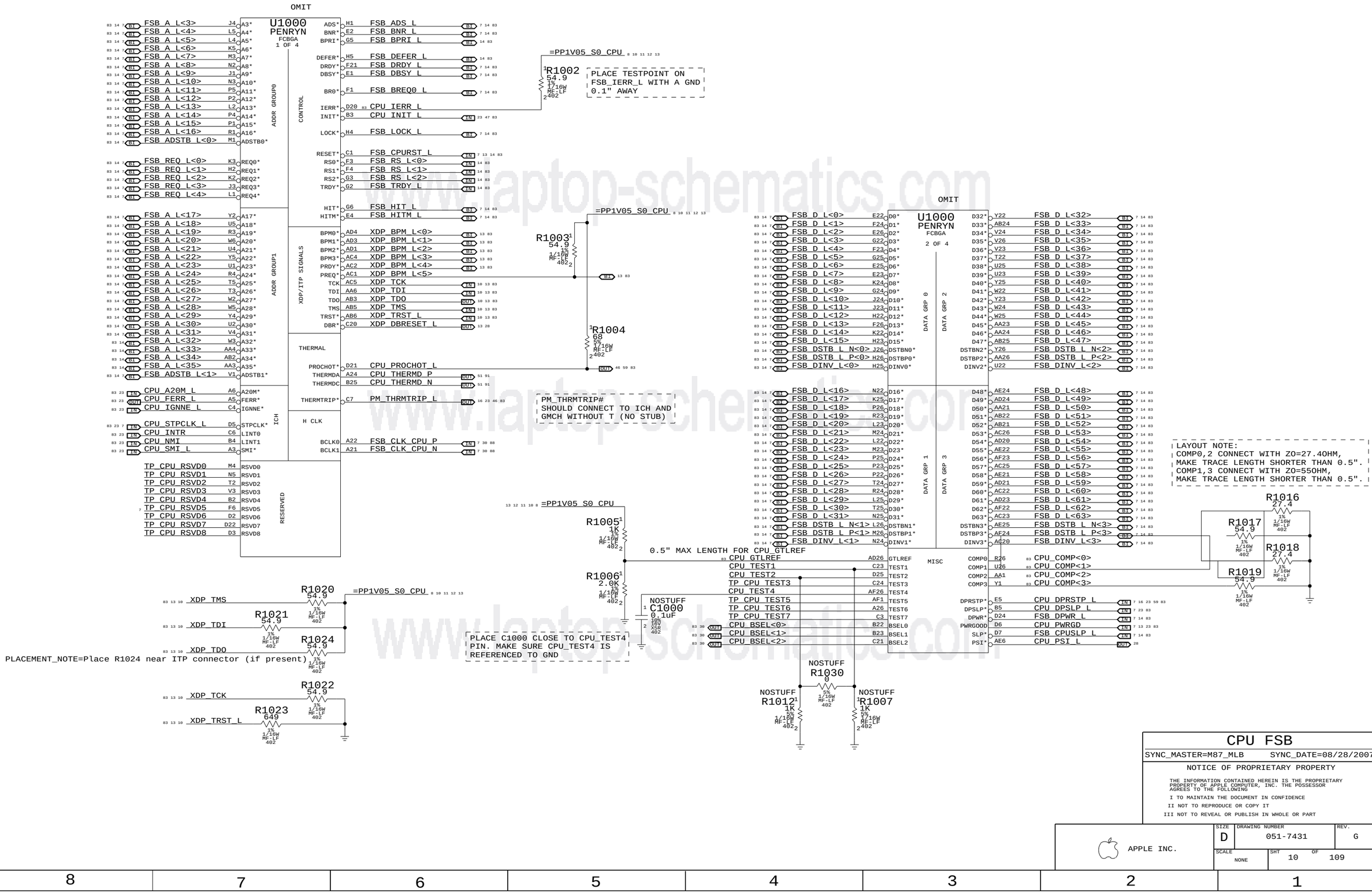
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE	SHT	OF
NONE	9	109



www.laptop-schematics.com

CPU FSB

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 10 OF 109	

(CPU CORE POWER)
=PPVCORE_S0_CPU 8 11 12 49

Standard Voltage:	Low Voltage:	Ultra Low Voltage:
44.0 A (Design Target)	23.0 A (Design Target)	17.0 A (Design Target)
41.0 A (HFM)	21.0 A (HFM)	TBD A (HFM)
30.4 A (LFM)	18.7 A (LFM)	TBD A (LFM)
25.5 A (SuperLFM)	TBD A (SuperLFM)	
27.4 A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant LFM)
27.4 A (Sleep HFM)	TBD A (Sleep HFM)	TBD A (Sleep HFM)
16.8 A (Sleep SuperLFM)	TBD A (Sleep SuperLFM)	TBD A (Sleep LFM)
25.0 A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)	TBD A (Deep Sleep SuperLFM)	TBD A (Deep Sleep LFM)
11.5 A (Deeper Sleep)	TBD A (Deeper Sleep)	TBD A (Deeper Sleep)
9.4 A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)

OMIT
U1000
PENRYN
FCBGA
3 OF 4

VCC: A7 A9 A10 A12 A13 A15 A17 A18 A20 B7 B9 B10 B12 B14 B15 B17 B18 B20 C9 C10 C12 C13 C15 C17 C18 D9 D10 D12 D14 D15 D17 D18 E7 E9 E10 E12 E13 E15 E17 E18 E20 F7 F9 F10 F12 F14 F15 F17 F18 F20 AA7 AA9 AA10 AA12 AA13 AA15 AA17 AA18 AA20 AB9 AC10 AB10 AB12 AB14 AB15 AB17 AB18

VCC: AB20 AB7 AC7 AC9 AC12 AC13 AC15 AC17 AC18 AD7 AD9 AD10 AD12 AD14 AD15 AD17 AD18 AE9 AE10 AE12 AE13 AE15 AE17 AE18 AE20 AF9 AF10 AF12 AF14 AF15 AF17 AF18 AF20

(CPU IO POWER 1.05V)
=PP1V05_S0_CPU 8 10 12 13

4500 mA (before VCC stable)
2500 mA (after VCC stable)

VCCP: G21 V6 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21

(CPU INTERNAL PLL POWER 1.5V)
=PP1V5_S0_CPU 8 12

130 mA

VCCA: B26 C26

VID0	AD6	CPU_VID<0>	OUT 12 83
VID1	AF5	CPU_VID<1>	OUT 12 83
VID2	AE5	CPU_VID<2>	OUT 12 83
VID3	AF4	CPU_VID<3>	OUT 12 83
VID4	AE3	CPU_VID<4>	OUT 12 83
VID5	AF3	CPU_VID<5>	OUT 12 83
VID6	AE2	CPU_VID<6>	OUT 12 83
VCCSENSE	AF7	CPU_VCCSENSE_P	OUT 59 83
VSSSENSE	AE7	CPU_VCCSENSE_N	OUT 59 83

=PPVCORE_S0_CPU 8 11 12 49

R1100
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

OMIT
U1000
PENRYN
FCBGA
4 OF 4

VSS: A4 A8 A11 A14 A16 A19 A23 AF2 B6 B8 B11 B13 B16 B19 B21 B24 C5 C8 C11 C14 C16 C19 C2 C22 C25 D1 D4 D8 D11 D13 D16 D19 D23 D26 E3 E6 E8 E11 E14 E16 E19 E21 E24 F5 F8 F11 F13 F16 F19 F2 F22 F25 G4 G1 G23 G26 H3 H6 H21 H24 J2 J5 J22 J25 K1 K4 K23 K26 L3 L6 L21 L24 M2 M5 M22 M25 N1 N4 N23 N26 P3 B1

VSS: P6 P21 P24 R2 R5 R22 R25 T1 T4 T23 T26 U3 U6 U21 U24 V2 V5 V22 V25 W1 W4 W23 W26 Y3 Y6 Y21 Y24 AA2 AA5 AA8 AA11 AA14 AA16 AA19 AA22 AA25 AB1 AB4 AB8 AB11 AB13 AB16 AB19 AB23 AB26 AC3 AC6 AC8 AC11 AC14 AC16 AC19 AC21 AC24 AD2 AD5 AD8 AD11 AD13 AD16 AD19 AD22 AD25 AE1 AE4 AE8 AE11 AE14 AE16 AE19 AE23 AE26 A2 AF6 AF8 AF11 AF13 AF16 AF19 AF21 A25 AF25

www.laptop-schematics.com

CPU Power & Ground

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

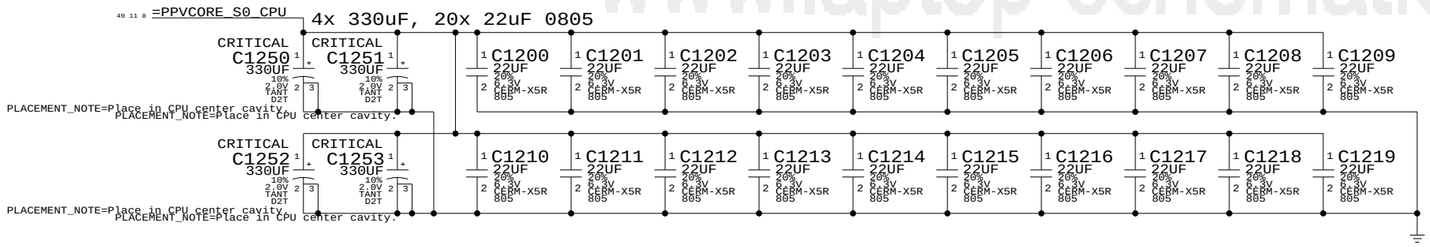
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

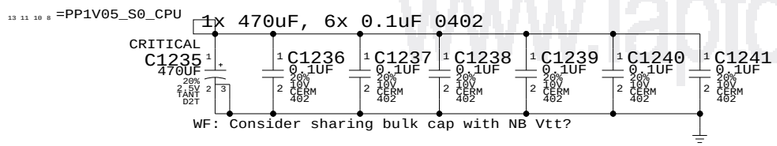
SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 11 OF 109	

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

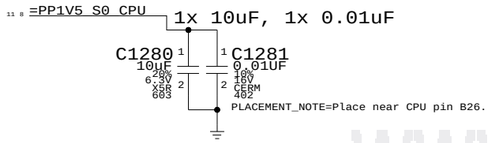
CPU VCORE HF AND BULK DECOUPLING



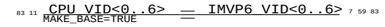
VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU VCORE VID CONNECTIONS



www.laptop-schematics.com

CPU Decoupling & VID

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

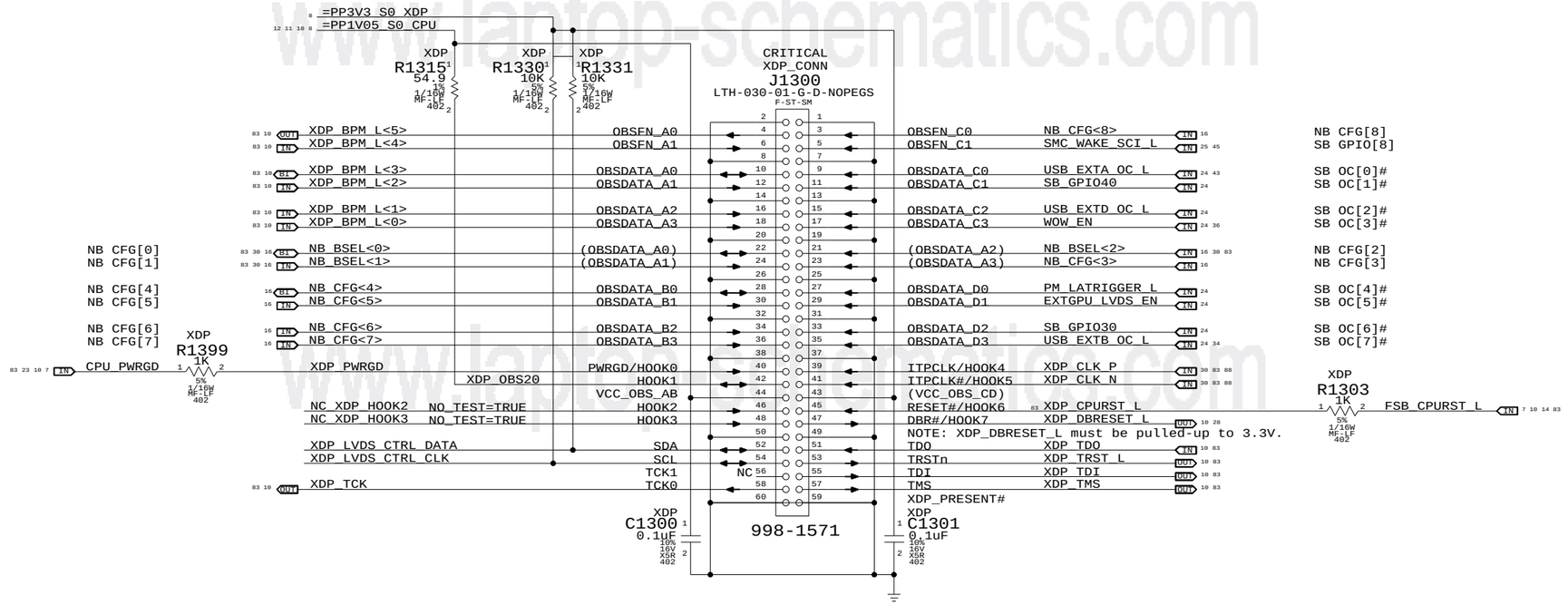
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 12 OF 109	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

www.laptop-schematics.com

eXtended Debug Port (XDP)

SYNC_MASTER=T9_NOME SYNC_DATE=01/22/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

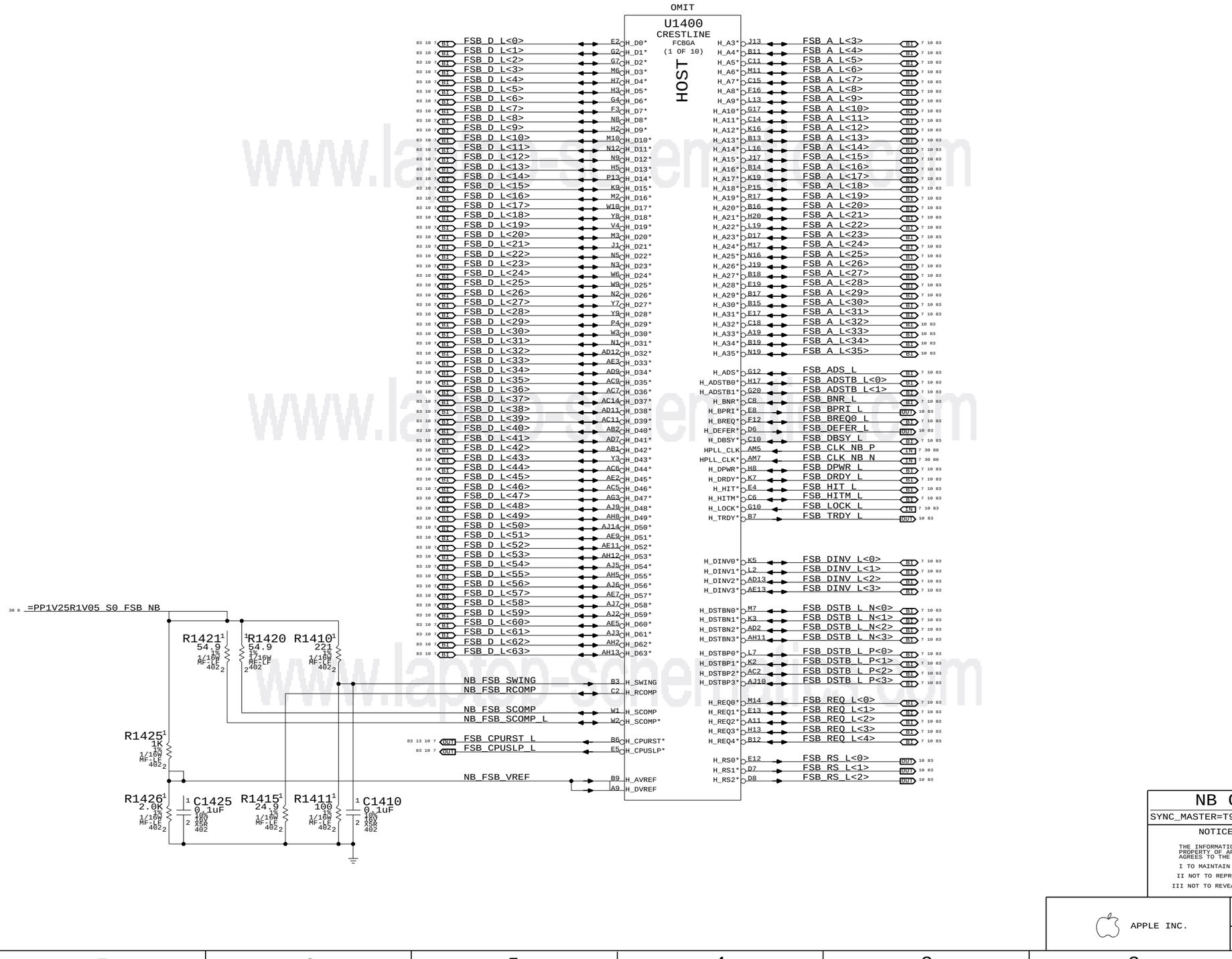
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 13 OF 109	



www.laptop-schematics.com

NB CPU Interface

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 14 OF 109	

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

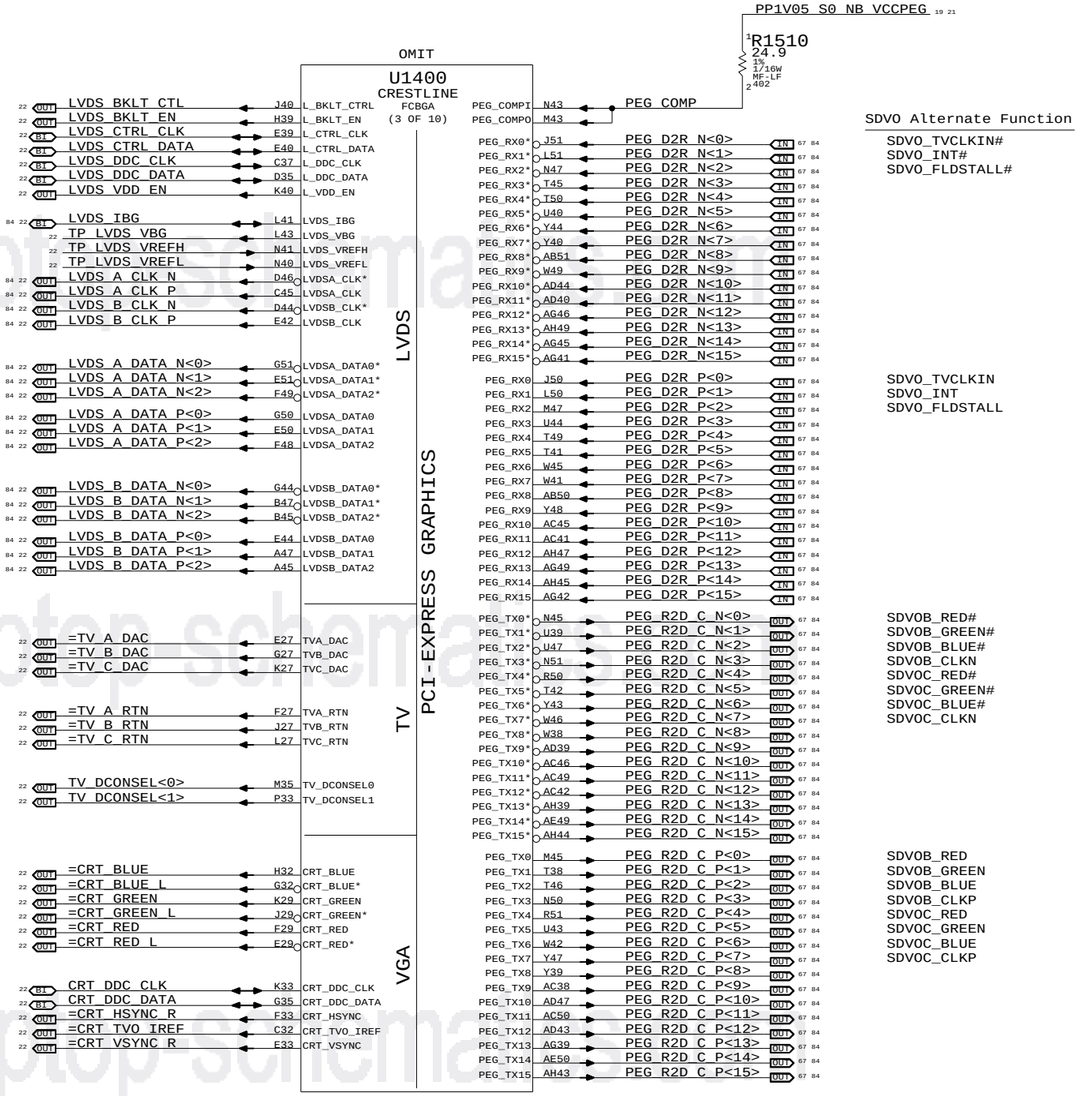
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



www.laptop-schematics.com

NB PEG / Video Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 15 OF 109	

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB_CFG<5> 13 16
NBCFG_DMI_X2
R1655 3.9K 5% 1/16W MF-LF 402

NB_CFG<9> 16
NBCFG_PEG_REVERSE
R1659 3.9K 5% 1/16W MF-LF 402

NB_CFG<16> 16
NBCFG_DYN_ODT_DISABLE
R1666 3.9K 5% 1/16W MF-LF 402

=PP3V3_S0_NB_VCCHV 8 16 19 21
NBCFG_DMI_REVERSE
R1669 3.9K 5% 1/16W MF-LF 402
NB_CFG<19> 16

=PP3V3_S0_NB_VCCHV 8 16 19 21
NBCFG_SDVO_AND_PCIE
R1670 3.9K 5% 1/16W MF-LF 402
NB_CFG<20> 16

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

21 19 16 8 =PP3V3_S0_NB_VCCHV
R1630 10K 5% 1/16W MF-LF 402
R1631 10K 5% 1/16W MF-LF 402

45 31 IN PM_EXTTS_L<0>
45 32 IN PM_EXTTS_L<1>

OMIT

U1400
CRESTLINE
FCBGA
(2 OF 10)

TP_NB_RSVD<1>	P36	RSVD1		
TP_NB_RSVD<2>	P37	RSVD2		
TP_NB_RSVD<3>	R35	RSVD3		
TP_NB_RSVD<4>	N35	RSVD4		
TP_NB_RSVD<5>	AR12	RSVD5		
TP_NB_RSVD<6>	AR13	RSVD6		
TP_NB_RSVD<7>	AM12	RSVD7		
TP_NB_RSVD<8>	AN13	RSVD8		
TP_NB_RSVD<9>	J12	RSVD9		
TP_NB_RSVD<10>	AR37	RSVD10		
TP_NB_RSVD<11>	AM36	RSVD11		
TP_NB_RSVD<12>	AL36	RSVD12		
TP_NB_RSVD<13>	AM37	RSVD13		
TP_NB_RSVD<14>	D20	RSVD14		
TP_NB_RSVD<20>	H10	RSVD20		
TP_NB_RSVD<21>	B51	RSVD21		
TP_NB_RSVD<22>	BJ20	RSVD22		
TP_NB_RSVD<23>	BK22	RSVD23		
7 TP_NB_RSVD<24>	BF19	RSVD24		
TP_NB_RSVD<25>	BH20	RSVD25		
7 TP_NB_RSVD<26>	BK18	RSVD26		
7 TP_NB_RSVD<27>	BJ18	RSVD27		
TP_MEM_CLKP2	BF23	SM_CK2		
TP_MEM_CLKN2	BG23	SM_CK2*		
TP_MEM_CLKP5	BC23	SM_CK5		
TP_MEM_CLKN5	BD24	SM_CK5*		
85 33 31 OUT MEM_A_A<14>	BJ29	SA_MA14		
85 33 32 OUT MEM_B_A<14>	BE24	SB_MA14		
TP_NB_RSVD<34>	BH39	RSVD34		
TP_NB_RSVD<35>	AW20	RSVD35		
TP_NB_RSVD<36>	BK20	RSVD36		
TP_LVDS_A_DATAN3	C48	RSVD37		
TP_LVDS_A_DATAP3	D47	RSVD38		
TP_LVDS_B_DATAN3	B44	RSVD39		
TP_LVDS_B_DATAP3	C44	RSVD40		
TP_NB_RSVD<41>	A35	RSVD41		
TP_NB_RSVD<42>	B37	RSVD42		
TP_NB_RSVD<43>	B36	RSVD43		
TP_NB_RSVD<44>	B34	RSVD44		
TP_NB_RSVD<45>	C34	RSVD45		
83 30 13 IN NB_BSEL<0>	P27	CFG0		
83 30 13 IN NB_BSEL<1>	N27	CFG1		
83 30 13 IN NB_BSEL<2>	N24	CFG2		
13 OUT NB_CFG<3>	C21	CFG3	IPU	
13 B1 NB_CFG<4>	C23	CFG4	IPU	
16 13 B1 NB_CFG<5>	F23	CFG5	IPU	
13 OUT NB_CFG<6>	N23	CFG6	IPU	
13 OUT NB_CFG<7>	G23	CFG7	IPU	
13 OUT NB_CFG<8>	J20	CFG8	IPU	
16 NB_CFG<9>	C20	CFG9	IPU	
TP_NB_CFG<10>	R24	CFG10	IPU	
TP_NB_CFG<11>	L23	CFG11	IPU	
TP_NB_CFG<12>	J23	CFG12	IPU	
TP_NB_CFG<13>	E23	CFG13	IPU	
TP_NB_CFG<14>	E20	CFG14	IPU	
TP_NB_CFG<15>	K23	CFG15	IPU	
16 NB_CFG<16>	M20	CFG16	IPU	
TP_NB_CFG<17>	M24	CFG17	IPU	
TP_NB_CFG<18>	L32	CFG18	IPD	
16 NB_CFG<19>	N33	CFG19	IPD	
16 NB_CFG<20>	L35	CFG20	IPD	
25 7 OUT PM_BMBUSY_L	G41	PM_BM_BUSY*		
83 59 23 10 7 IN CPU_DPRSTP_L	L39	PM_DPRSTP*		
	L36	PM_EXT_TS0*		
	J36	PM_EXT_TS1*		
59 28 9 7 IN VR_PWRGOOD_DELAY	AW49	PWROK		
28 7 IN NB_RESET_L	AV20	RSTIN*		
83 46 23 10 OUT PM_THRMTRIP_L	N20	THERMTRIP*		
83 59 25 7 IN PM_DPRSLPVR	G36	DPRSLPVR		
7 TP_NB_NC<1>	BJ51	NC1		
7 TP_NB_NC<2>	BK51	NC2		
7 TP_NB_NC<3>	BK50	NC3		
7 TP_NB_NC<4>	BL50	NC4		
7 TP_NB_NC<5>	BL49	NC5		
7 TP_NB_NC<6>	BL3	NC6		
7 TP_NB_NC<7>	BL2	NC7		
7 TP_NB_NC<8>	BK1	NC8		
7 TP_NB_NC<9>	BJ1	NC9		
7 TP_NB_NC<10>	E1	NC10		
7 TP_NB_NC<11>	A5	NC11		
7 TP_NB_NC<12>	C51	NC12		
7 TP_NB_NC<13>	B50	NC13		
7 TP_NB_NC<14>	A50	NC14		
7 TP_NB_NC<15>	A49	NC15		
7 TP_NB_NC<16>	BK2	NC16		

RSVD
DDR MUXING
CFG
DMI
PM
GRAPHICS VID
ME
NC
CLK
MISC

SM_CK0	AV29	MEM_CLK_P<0>	OUT 31 85
SM_CK1	BB23	MEM_CLK_P<1>	OUT 31 85
SM_CK3	BA25	MEM_CLK_P<3>	OUT 32 85
SM_CK4	AV23	MEM_CLK_P<4>	OUT 32 85
SM_CK0*	AW30	MEM_CLK_N<0>	OUT 31 85
SM_CK1*	BA23	MEM_CLK_N<1>	OUT 31 85
SM_CK3*	AW25	MEM_CLK_N<3>	OUT 32 85
SM_CK4*	AW23	MEM_CLK_N<4>	OUT 32 85
SM_CKE0	BE29	MEM_CKE<0>	OUT 31 33 85
SM_CKE1	AY32	MEM_CKE<1>	OUT 31 33 85
SM_CKE3	BD39	MEM_CKE<3>	OUT 32 33 85
SM_CKE4	BG37	MEM_CKE<4>	OUT 32 33 85
SM_CS0*	BG20	MEM_CS_L<0>	OUT 31 33 85
SM_CS1*	BK16	MEM_CS_L<1>	OUT 31 33 85
SM_CS2*	BG16	MEM_CS_L<2>	OUT 32 33 85
SM_CS3*	BE13	MEM_CS_L<3>	OUT 32 33 85
SM_ODT0	BH18	MEM_ODT<0>	OUT 31 33 85
SM_ODT1	BJ15	MEM_ODT<1>	OUT 31 33 85
SM_ODT2	BJ14	MEM_ODT<2>	OUT 32 33 85
SM_ODT3	BE16	MEM_ODT<3>	OUT 32 33 85
SM_RCOMP	BL15	MEM_RCOMP	
SM_RCOMP*	BK14	MEM_RCOMP_L	
SM_RCOMP_VOH	BK31	MEM_RCOMP_VOH	
SM_RCOMP_VOL	BL31	MEM_RCOMP_VOL	
SM_VREF0	AR49	=PP0V9_S3M_MEM_NBVREFA	IN 8
SM_VREF1	AW4	=PP0V9_S3M_MEM_NBVREFB	IN 8
DPLL_REF_CLK	B42	=NB_CLK96M_DOT_P	IN 22
DPLL_REF_CLK*	C42	=NB_CLK96M_DOT_N	IN 22
DPLL_REF_SSCLK	H48	=NB_CLK100M_DPLLSS_P	IN 22
DPLL_REF_SSCLK*	H47	=NB_CLK100M_DPLLSS_N	IN 22
PEG_CLK	K44	NB_CLK100M_PCIE_P	IN 7 30 88
PEG_CLK*	K45	NB_CLK100M_PCIE_N	IN 7 30 88
		Clk used for PEG and DMI	
DMI_RXN0	AN47	DMI_S2N_N<0>	IN 24 84
DMI_RXN1	AJ38	DMI_S2N_N<1>	IN 24 84
DMI_RXN2	AN42	DMI_S2N_N<2>	IN 24 84
DMI_RXN3	AN46	DMI_S2N_N<3>	IN 24 84
DMI_RXP0	AM47	DMI_S2N_P<0>	IN 24 84
DMI_RXP1	AJ39	DMI_S2N_P<1>	IN 24 84
DMI_RXP2	AN41	DMI_S2N_P<2>	IN 24 84
DMI_RXP3	AN45	DMI_S2N_P<3>	IN 24 84
DMI_TXN0	AJ46	DMI_N2S_N<0>	OUT 24 84
DMI_TXN1	AJ41	DMI_N2S_N<1>	OUT 24 84
DMI_TXN2	AM40	DMI_N2S_N<2>	OUT 24 84
DMI_TXN3	AM44	DMI_N2S_N<3>	OUT 24 84
DMI_TXP0	AJ47	DMI_N2S_P<0>	OUT 24 84
DMI_TXP1	AJ42	DMI_N2S_P<1>	OUT 24 84
DMI_TXP2	AM39	DMI_N2S_P<2>	OUT 24 84
DMI_TXP3	AM43	DMI_N2S_P<3>	OUT 24 84
GFX_VID0	E35	GFX_VID<0>	OUT 22
GFX_VID1	A39	GFX_VID<1>	OUT 22
GFX_VID2	C38	GFX_VID<2>	OUT 22
GFX_VID3	B39	GFX_VID<3>	OUT 22
GFX_VR_EN	E36	GFX_VID<4>	OUT 22
		=GFX_VR_EN	OUT 22
CL_CLK	AM49	CLINK_NB_CLK	B1 25 87
CL_DATA	AK50	CLINK_NB_DATA	B1 25 87
CL_PWROK	AT43	=NB_CLINK_MPWROK	IN 9
CL_RST*	AN49	CLINK_NB_RESET_L	OUT 25 87
CL_VREF	AM50	NB_CLINK_VREF	87
SDVO_CTRL_CLK	H35	SDVO_CTRLCLK	B1 22
SDVO_CTRL_DATA	K36	SDVO_CTRLDATA	B1 22
CLKREQ*	G39	NB_CLKREQ_L	OUT 7 29
ICH_SYNC*	G40	NB_SB_SYNC_L	OUT 7 25
TEST1	A37	NB_TEST1	
TEST2	R32	NB_TEST2	

21 18 8 =PP1V8_S3M_MEM_NB
R1610 20 1% 1/10W MF-LF 402
R1620 1K 1% 1/16W MF-LF 402
C1623 0.01UF 10% 16V CERM 402
C1622 2.2UF 20% 6.3V CERM1 603
R1622 3.01K 1% 1/16W MF-LF 402
R1611 20 1% 1/10W MF-LF 402
C1625 0.01UF 10% 16V CERM 402
C1624 2.2UF 20% 6.3V CERM1 603
R1624 1K 1% 1/10W MF-LF 402
C1615 0.1UF 20% 10V CERM 402
C1616 0.1UF 20% 10V CERM 402

PP1V25_S0M_NB_VCCAXD 19 21
R1640 1K 1% 1/16W MF-LF 402
C1640 0.1uF 20% 10V CERM 402
R1641 392 1% 1/16W MF-LF 402

R1691 20K 5% 1/16W MF-LF 402
R1690 0 5% 1/16W MF-LF 402

NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

NB Misc Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

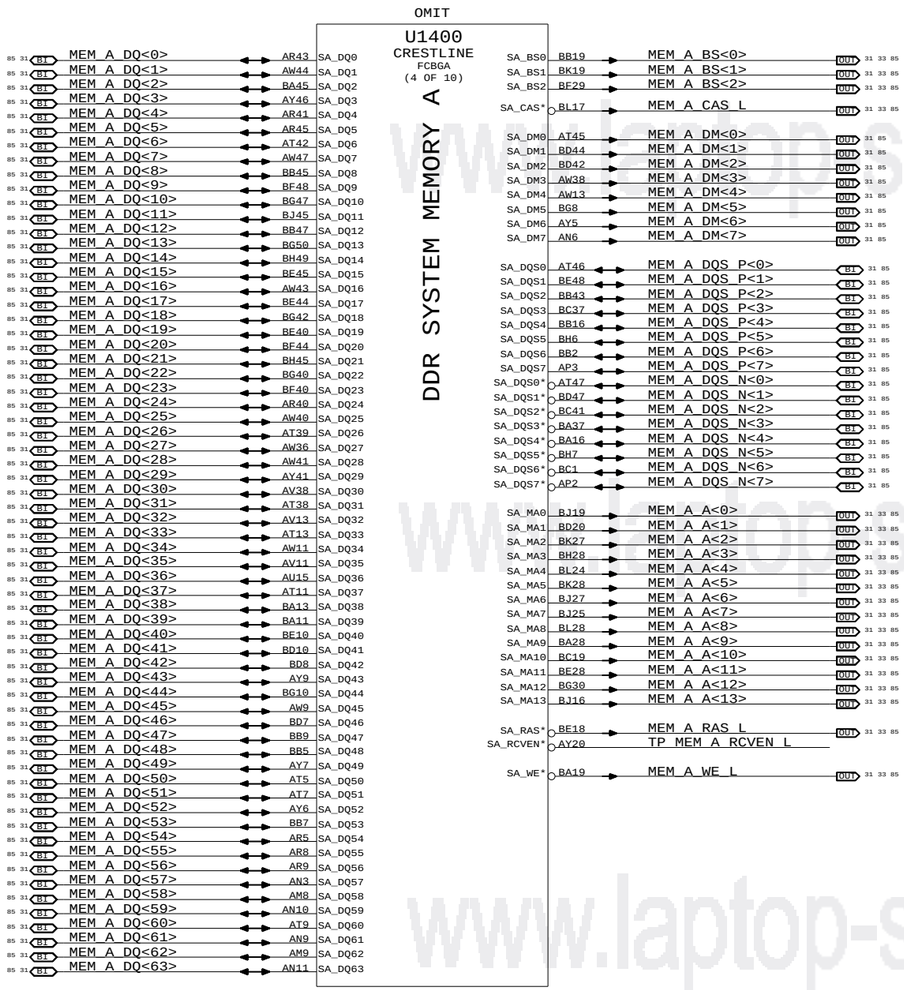
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

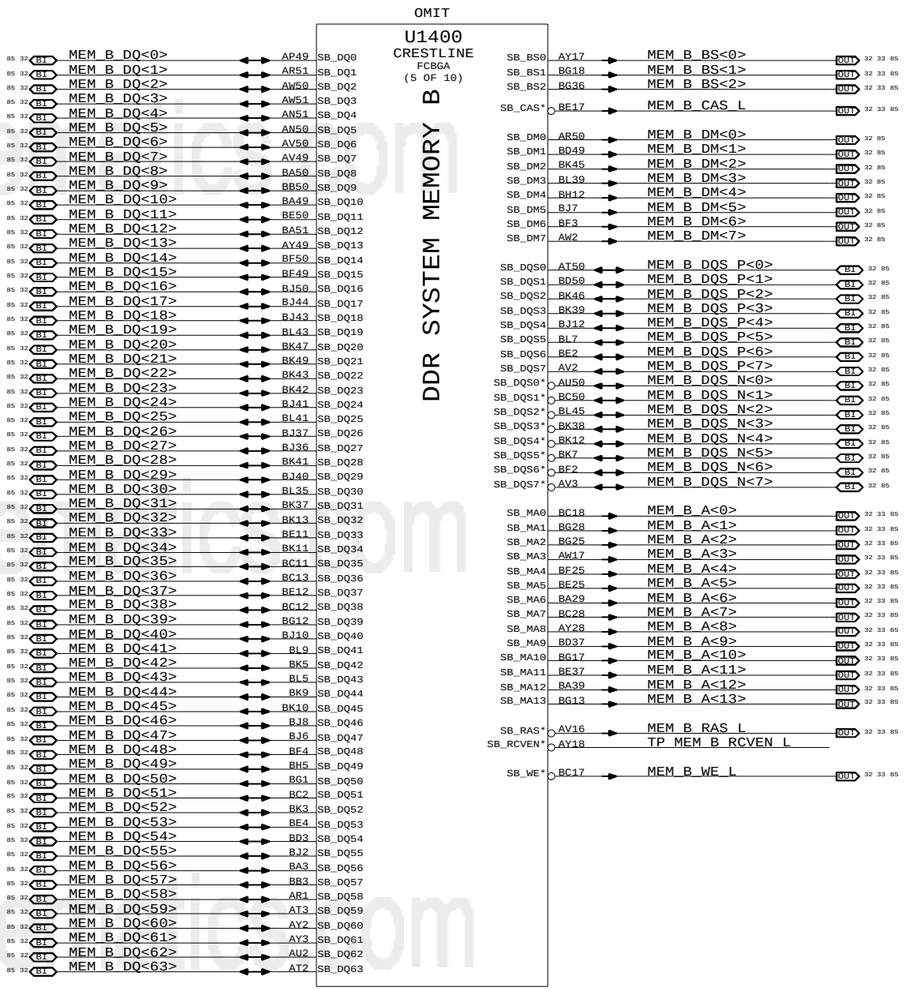
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 16 OF 109	

www.apple-schematics.com





www.laptop-schematic.com

NB DDR2 Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

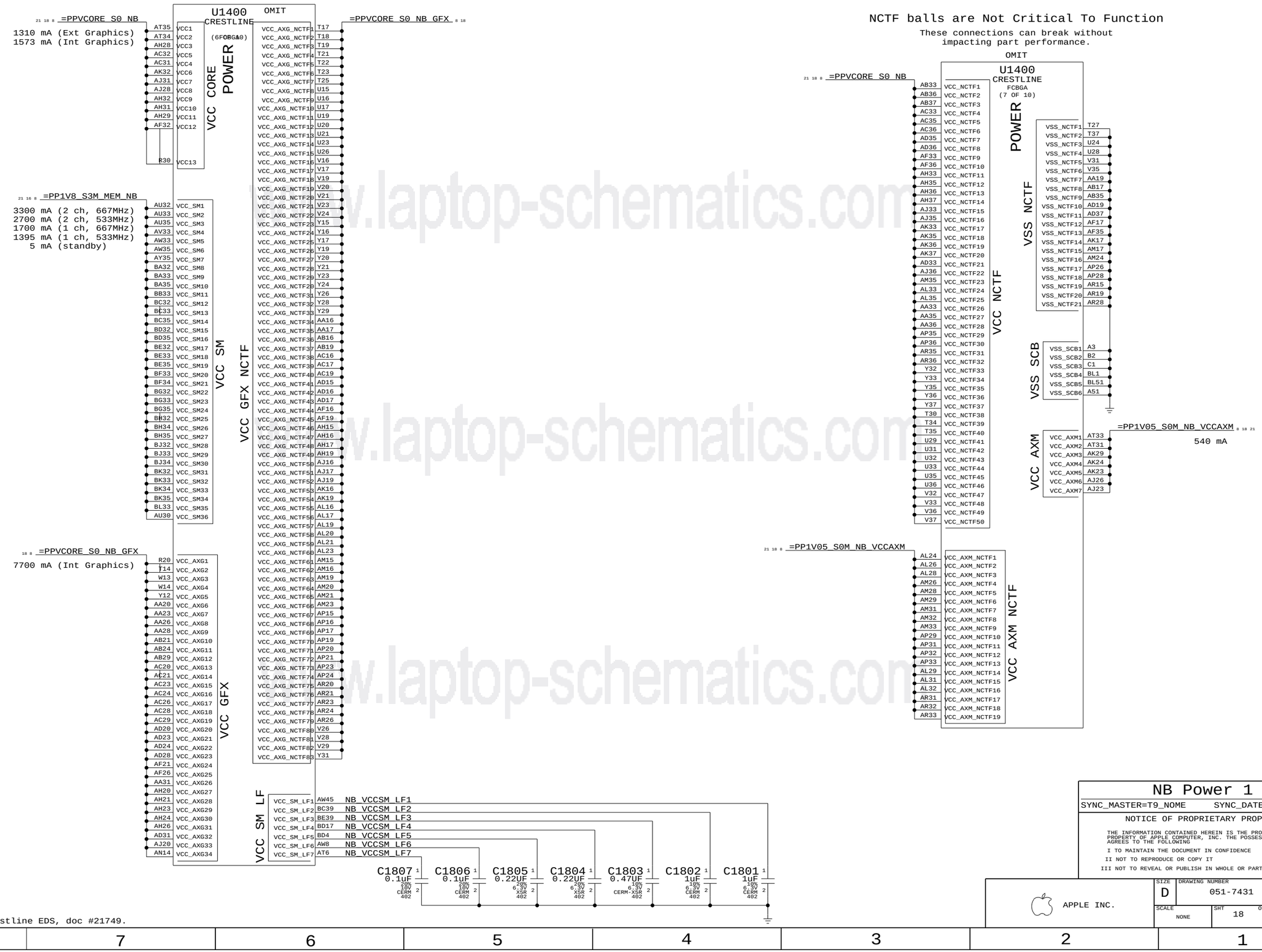
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

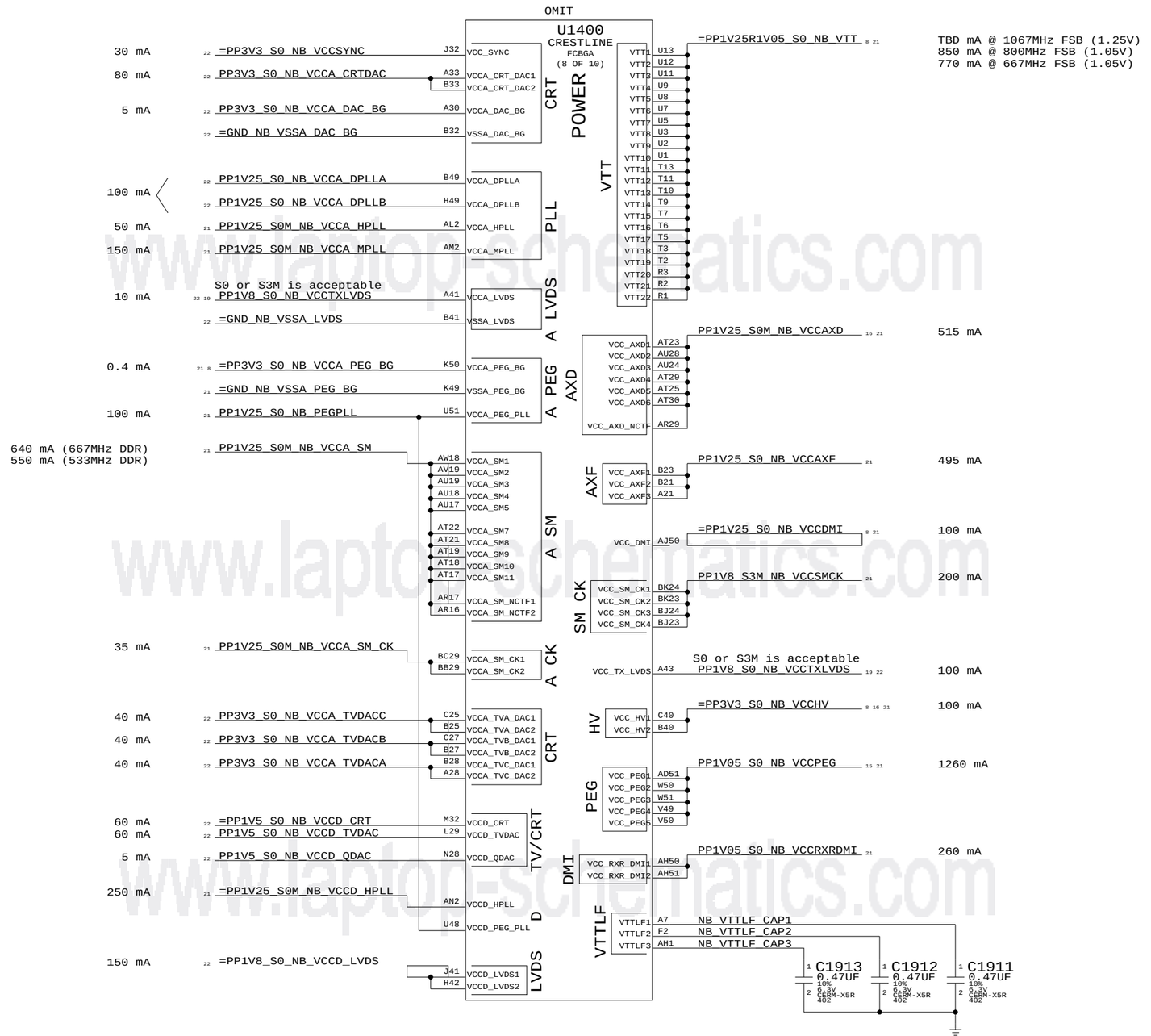
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 17 OF 109	


U1400
CRESTLINE
(6 OF 10)
FCBGA
OMIT
=PPVCORE_S0_NB
1310 mA (Ext Graphics)
1573 mA (Int Graphics)
VCC CORE POWER
=PP1V8_S3M_MEM_NB
3300 mA (2 ch, 667MHz)
2700 mA (2 ch, 533MHz)
1700 mA (1 ch, 667MHz)
1395 mA (1 ch, 533MHz)
5 mA (standby)
VCC SM
=PPVCORE_S0_NB_GFX
VCC GFX NCTF
=PPVCORE_S0_NB_GFX
7700 mA (Int Graphics)
VCC GFX
VCC SM LF
NB_VCCSM_LF1
NB_VCCSM_LF2
NB_VCCSM_LF3
NB_VCCSM_LF4
NB_VCCSM_LF5
NB_VCCSM_LF6
NB_VCCSM_LF7
C1807 0.1uF 20% 16V CERM 402
C1806 0.1uF 20% 16V CERM 402
C1805 0.22UF 20% 6.3V X5R 402
C1804 0.22UF 20% 6.3V X5R 402
C1803 0.47UF 10% 6.3V CERM-X5R 402
C1802 1uF 10% 6.3V CERM 402
C1801 1uF 10% 6.3V CERM 402
NCTF balls are Not Critical To Function
These connections can break without impacting part performance.
OMIT
U1400
CRESTLINE
FCBGA
(7 OF 10)
=PPVCORE_S0_NB
VCC NCTF
VSS NCTF POWER
VSS SCB
=PP1V05_S0M_NB_VCCAXM
540 mA
VCC AXM
=PP1V05_S0M_NB_VCCAXM
VCC AXM NCTF
Current numbers from Crestline EDS, doc #21749.
NB Power 1
SYNC_MASTER=T9_NOME
SYNC_DATE=01/25/2007
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE D
DRAWING NUMBER 051-7431
REV. G
SCALE NONE
SHT 18 OF 109



www.laptopschematics.com

Current numbers from Crestline EDS, doc #21749.

NB Power 2

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 19 OF 109	

OMIT

U1400
CRESTLINE
FCBGA
(9 OF 10)
VSS

A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AY10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B38
AD26	VSS21	VSS120	B43
AD29	VSS22	VSS121	B46
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BB12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BG19
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BJ11
AN43	VSS72	VSS171	BJ13
AN5	VSS73	VSS172	BJ38
AN7	VSS74	VSS173	BJ4
AP4	VSS75	VSS174	BJ42
AP48	VSS76	VSS175	BJ46
AP50	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C36
AW16	VSS99	VSS198	C41

OMIT

U1400
CRESTLINE
FCBGA
(10 OF 10)
VSS

C46	VSS199	VSS287	W11
C50	VSS200	VSS288	W39
C7	VSS201	VSS289	W43
D13	VSS202	VSS290	W47
D24	VSS203	VSS291	W5
D3	VSS204	VSS292	W7
D32	VSS205	VSS293	Y13
D39	VSS206	VSS294	Y2
D45	VSS207	VSS295	Y41
D49	VSS208	VSS296	Y45
E10	VSS209	VSS297	Y49
E16	VSS210	VSS298	Y5
E24	VSS211	VSS299	Y50
E28	VSS212	VSS300	Y11
E32	VSS213	VSS301	P29
E47	VSS214		
F19	VSS215		
F36	VSS216	TDE_SENSE VSS302	T29
F4	VSS217		
F40	VSS218	TDE_FORCE VSS303	T31
F50	VSS219		
G1	VSS220	TDB_FORCE VSS304	T33
G13	VSS221		
G16	VSS222	TDB_SENSE VSS305	R28
G19	VSS223		
G24	VSS224		
G28	VSS225	VSS306	AA32
G29	VSS226	VSS307	AB32
G33	VSS227	VSS308	AD32
G42	VSS228	VSS309	AF28
G45	VSS229	VSS310	AF29
G48	VSS230	VSS311	AT27
G8	VSS231	VSS312	AV25
H24	VSS232	VSS313	H50
H28	VSS233		
H4	VSS234		
H45	VSS235		
J11	VSS236		
J16	VSS237		
J2	VSS238		
J24	VSS239		
J28	VSS240		
J33	VSS241		
J35	VSS242		
J39	VSS243		
K12	VSS245		
K47	VSS246		
K8	VSS247		
L1	VSS248		
L17	VSS249		
L20	VSS250		
L24	VSS251		
L28	VSS252		
L3	VSS253		
L33	VSS254		
L49	VSS255		
M28	VSS256		
M42	VSS257		
M46	VSS258		
M49	VSS259		
M5	VSS260		
M50	VSS261		
M9	VSS262		
N11	VSS263		
N14	VSS264		
N17	VSS265		
N29	VSS266		
N32	VSS267		
N36	VSS268		
N39	VSS269		
N44	VSS270		
N49	VSS271		
N7	VSS272		
P19	VSS273		
P2	VSS274		
P23	VSS275		
P3	VSS276		
P50	VSS277		
R49	VSS278		
T39	VSS279		
T43	VSS280		
T47	VSS281		
U41	VSS282		
U45	VSS283		
U50	VSS284		
V2	VSS285		
V3	VSS286		

Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

TDE_SENSE T29 =NB_TDE_SENSE S1

NOTE: TDE = _P

TDE_FORCE T31 =NB_TDE_FORCE S1

TDB_FORCE T33 =NB_TDB_FORCE S1

NOTE: TDB = _N

TDB_SENSE R28 =NB_TDB_SENSE S1

NB Grounds

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 20 OF 109	

www.laptop-schematics.com

www.laptop-schematics.com

GMCH Core Power

=PPVCORE_S0_NB

1573mA (Int Graphics)
1310mA (Ext Graphics)

CRITICAL
C2100 470UF 20% 2.5V POLY CASE-D2T-SM
C2101 22UF 20% 6.3V CERM-X5R 805-3
C2102 0.22UF 20% 6.3V CERM 402
C2103 0.22UF 20% 6.3V CERM 402
C2104 0.1UF 20% 10V CERM 402

WF: Matanzas has 2-pin 270uF bulk cap

PLACEMENT_NOTE=Place in GMCH cavity

GMCH ME Core Power

=PP1V05_S0M_NB_VCCAXM

540 mA

C2110 22UF 20% 6.3V CERM-X5R 805-3
C2111 0.22UF 20% 6.3V CERM 402
C2112 0.22UF 20% 6.3V CERM 402
C2113 0.1UF 20% 10V CERM 402
C2114 0.1UF 20% 10V CERM 402
C2115 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place in GMCH cavity

GMCH FSB I/O Rail

=PP1V25R1V05_S0_NB_VTT

850 mA (800MHz FSB)
770 mA (667MHz FSB)

CRITICAL
C2120 220UF 20% 2.5V POLY CASE-B2-SM-HF
C2121 4.7UF 20% 6.3V CERM 603
C2122 4.7UF 20% 6.3V CERM 603
C2123 2.2UF 20% 6.3V CERM 603
C2124 0.47UF 10% 6.3V CERM-X5R 402

PLACEMENT_NOTE=Place close to U1400

GMCH Memory I/O Rail

=PP1V8_S3M_MEM_NB

3300 mA (2ch 667MHz)
2700 mA (2ch 533MHz)
1700 mA (1ch 667MHz)
1395 mA (1ch 533MHz)
5 mA (standby)

CRITICAL
C2130 330UF 20% 2.5V POLY CASE-C2S-HF
C2135 0.1UF 20% 10V CERM 402
C2131 22UF 20% 6.3V CERM-X5R 805-3
C2132 22UF 20% 6.3V CERM-X5R 805-3

PLACEMENT_NOTE=Place close to U1400

WF: "Place where LVDS and DDR2 taps." (C2135)

Placeholder for 3.9nH, 1A, 32mOhm

=PP1V25_S0M_NB_VCCA

675 mA (667MHz DDR2)
585 mA (533MHz DDR2)

R2141 0 5% 1/10W MF-LF 603
CRITICAL
C2140 220UF 20% 2.5V POLY CASE-B2-SM-HF
NO STUFF
C2141 22UF 20% 6.3V CERM-X5R 805-3
C2142 22UF 20% 6.3V CERM-X5R 805-3
C2143 4.7UF 20% 6.3V CERM 603
C2144 1UF 10% 10V X5R 402

PP1V25_S0M_NB_VCCA_SM
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

640 mA (667MHz DDR2)
550 mA (533MHz DDR2)

Placeholder for 2.2nH, 1.4A, 17mOhm

R2145 0 5% 1/10W MF-LF 603
NO STUFF
C2145 22UF 20% 6.3V CERM-X5R 805-3
C2146 2.2UF 20% 6.3V CERM1 603
C2148 0.1UF 20% 10V CERM 402

PP1V25_S0M_NB_VCCA_SM_CK
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

35 mA

Placeholder for 5.6nH, 0.9A, 45mOhm max

=PP1V25_S0M_NB_VCC

515 mA

NO STUFF
L2150 FERR-120-OHM-0.2A 0603
R2150 0 5% 1/10W MF-LF 603
NO STUFF
C2150 22UF 20% 6.3V CERM-X5R 805-3
C2151 1UF 10% 10V X5R 402

PP1V25_S0M_NB_VCCAXD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

515 mA

100 mA =PP3V3_S0_NB_VCCHV
100 mA =PP1V25_S0_NB_VCCDMI

C2160 0.1UF 20% 10V CERM 402
C2161 0.1UF 20% 10V CERM 402

=PP3V3_S0_NB_VCCA_PEG_BG

C2165 0.1UF 20% 10V CERM 402

0.4 mA

=GND_NB_VSSA_PEG_BG

Layout Note: Route to caps, then GND

=PP1V25_S0_NB_VCC

495 mA

R2170 0 5% 1/10W MF-LF 603
C2170 10UF 20% 6.3V POLY 603
C2171 1UF 10% 10V X5R 402

PP1V25_S0_NB_VCCAXF
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

495 mA

=PP1V05_S0_NB_PCIE

1520 mA

L2173 91NH 1210
C2173 220UF 20% 2.5V POLY CASE-B2-SM-HF CRITICAL
C2174 10UF 20% 6.3V X5R 603

PP1V05_S0_NB_VCCPEG
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

1260 mA

Layout Note: Place L and C close to MCH

Layout Note: 10uF caps should be close to MCH on opposite side.

PP1V05_S0_NB_VCCRXRDMI
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

260 mA

C2177 10UF 20% 6.3V X5R 603

Layout Note: 10uF caps should be close to MCH on opposite side.

=PP1V25_S0M_NB_PLL

450 mA

=PP1V25_S0M_NB_VCCD_HPLL

250 mA

C2180 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place C2180 by U1400.AN2

L2181 FERR-120-OHM-0.2A 0603

PP1V25_S0M_NB_VCCA_HPLL
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

50 mA

C2181 22UF 20% 6.3V CERM-X5R 805-3
C2182 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place C2182 by U1400.AL2

L2183 FERR-120-OHM-0.2A 0603

PP1V25_S0M_NB_VCCA_MPLL
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

150 mA

R2183 0.51 1% 1/10W MF-LF 402
C2184 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place C2184 by U1400.AM2

PP1V25_S0M_NB_MPLL_RC
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

C2183 22UF 20% 6.3V CERM-X5R 805-3

=PP1V05_S0_NB_FOLLOW

D2185 SOT23 BAT54E3
PP3V3_S0_NB1V05_FOLLOW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

R2185 10 1% 1/16W MF-LF 402

=PP3V3_S0_NB_FOLLOW

=PPVCORE_S0_NB_FOLLOW

D2186 SOT23 BAT54E3
PP3V3_S0_NBCORE_FOLLOW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

R2186 10 1% 1/16W MF-LF 402

NOTE: This follower is redundant if VCORE is always 1.05V.

CRITICAL

=PP1V25_S0_NB_PLL

100 mA

L2190 FERR-220-OHM 0805
R2190 1.1 1% 1/16W MF-LF 402
C2190 10UF 20% 6.3V X5R 603
C2191 0.1UF 20% 10V CERM 402
C2192 0.1UF 20% 10V CERM 402

PP1V25_S0_NB_PEGPLL
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

100 mA

PP1V25_S0_NB_PEGPLL_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

=PP1V8_S3M_NB_VCC

200 mA

L2195 1.0UH-220MA-0.12-OHM 0805
R2195 1.1 1% 1/16W MF-LF 402
C2195 10UF 20% 6.3V X5R 603
C2196 22UF 20% 6.3V CERM-X5R 805-3
C2197 0.1UF 20% 10V CERM 402

PP1V8_S3M_NB_VCCSMCK
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

200 mA

PP1V8_S3M_NB_VCCSMCK_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

NB Standard Decoupling

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 21 OF 109	

Current numbers from Crestline EDS, doc #21749.

Crestline LVDS Strapping

NOTE: This filter is required even if using only external graphics.
VCCD_TVDAC also powers internal thermal sensors.

8 =PP1V5_S0_NB_TVDAC
65 mA

CRITICAL
C2201
22000pF-1000mA
10V
NFM18
PP1V5_S0_NB_VCCD_TVDAC 19
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
60 mA

C2200
0.1uF
10V
CERM
402

Layout Note:
These 2 caps should be
within 6.35 mm of NB edge

15 LVDS_DDC_CLK
15 LVDS_DDC_DATA
15 LVDS_CTRL_CLK
15 LVDS_CTRL_DATA
15 =CRT_RED
15 =CRT_RED_L
15 =CRT_GREEN
15 =CRT_GREEN_L
15 =CRT_BLUE
15 =CRT_BLUE_L
15 =CRT_HSYNC_R
15 =CRT_VSYNC_R
15 =CRT_TVO_IREF
15 =TV_A_DAC
15 =TV_A_RTN
15 =TV_B_DAC
15 =TV_B_RTN
15 =TV_C_DAC
15 =TV_C_RTN
15 CRT_DDC_CLK
15 CRT_DDC_DATA
16 SDVO_CTRLCLK
16 SDVO_CTRLDATA
15 TV_DCONSEL<0>
15 TV_DCONSEL<1>
16 =NB_CLK96M_DOT_N
16 =NB_CLK96M_DOT_P
16 =NB_CLK100M_DPLLSS_P
16 =NB_CLK100M_DPLLSS_N

=GND_NB_VSSA_LVDS 19
PP1V8_S0_NB_VCCTXLVDS 19
PP1V25_S0_NB_VCCA_DPLLB 19
PP1V25_S0_NB_VCCA_DPLLA 19
=PP1V8_S0_NB_VCCD_LVDS 19
=PP1V5_S0_NB_VCCD_CRT 19
PP3V3_S0_NB_VCCA_CRTDAC 19
=PP3V3_S0_NB_VCCSYNC 19
PP1V5_S0_NB_VCCD_QDAC 19
PP3V3_S0_NB_VCCA_DAC_BG 19
=GND_NB_VSSA_DAC_BG 19
PP3V3_S0_NB_VCCA_TVDACA 19
PP3V3_S0_NB_VCCA_TVDACB 19
PP3V3_S0_NB_VCCA_TVDACC 19

15 LVDS_BKLT_CTL — NC_LVDS_BKLT_CTL (MAKE_BASE=TRUE NO_TEST=TRUE)
15 LVDS_BKLT_EN — NC_LVDS_BKLT_EN (MAKE_BASE=TRUE NO_TEST=TRUE)
15 LVDS_VDD_EN — NC_LVDS_VDD_EN (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_IBG — NC_LVDS_IBG (MAKE_BASE=TRUE NO_TEST=TRUE)
15 TP_LVDS_VBG — NC_LVDS_VBG (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_A_CLK_N — NC_LVDS_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_A_CLK_P — NC_LVDS_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_B_CLK_N — NC_LVDS_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_B_CLK_P — NC_LVDS_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_A_DATA_N<0> — NC_LVDS_A_DATAN<0> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_A_DATA_N<1> — NC_LVDS_A_DATAN<1> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_A_DATA_N<2> — NC_LVDS_A_DATAN<2> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_A_DATA_P<0> — NC_LVDS_A_DATAP<0> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_A_DATA_P<1> — NC_LVDS_A_DATAP<1> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_A_DATA_P<2> — NC_LVDS_A_DATAP<2> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_B_DATA_N<0> — NC_LVDS_B_DATAN<0> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_B_DATA_N<1> — NC_LVDS_B_DATAN<1> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_B_DATA_N<2> — NC_LVDS_B_DATAN<2> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_B_DATA_P<0> — NC_LVDS_B_DATAP<0> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_B_DATA_P<1> — NC_LVDS_B_DATAP<1> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 15 LVDS_B_DATA_P<2> — NC_LVDS_B_DATAP<2> (MAKE_BASE=TRUE NO_TEST=TRUE)
15 TP_LVDS_VREFH — NC_LVDS_VREFH (MAKE_BASE=TRUE NO_TEST=TRUE)
15 TP_LVDS_VREFL — NC_LVDS_VREFL (MAKE_BASE=TRUE NO_TEST=TRUE)
16 GFX_VID<1> — TP_GFX_VID<1> (MAKE_BASE=TRUE)
16 GFX_VID<2> — TP_GFX_VID<2> (MAKE_BASE=TRUE)
16 GFX_VID<3> — TP_GFX_VID<3> (MAKE_BASE=TRUE)
16 GFX_VID<4> — TP_GFX_VID<4> (MAKE_BASE=TRUE)
16 =GFX_VR_EN — TP_GFX_VR_EN (MAKE_BASE=TRUE)

Current numbers from Crestline EDS Addendum, doc #20127.

NB Graphics Decoupling

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

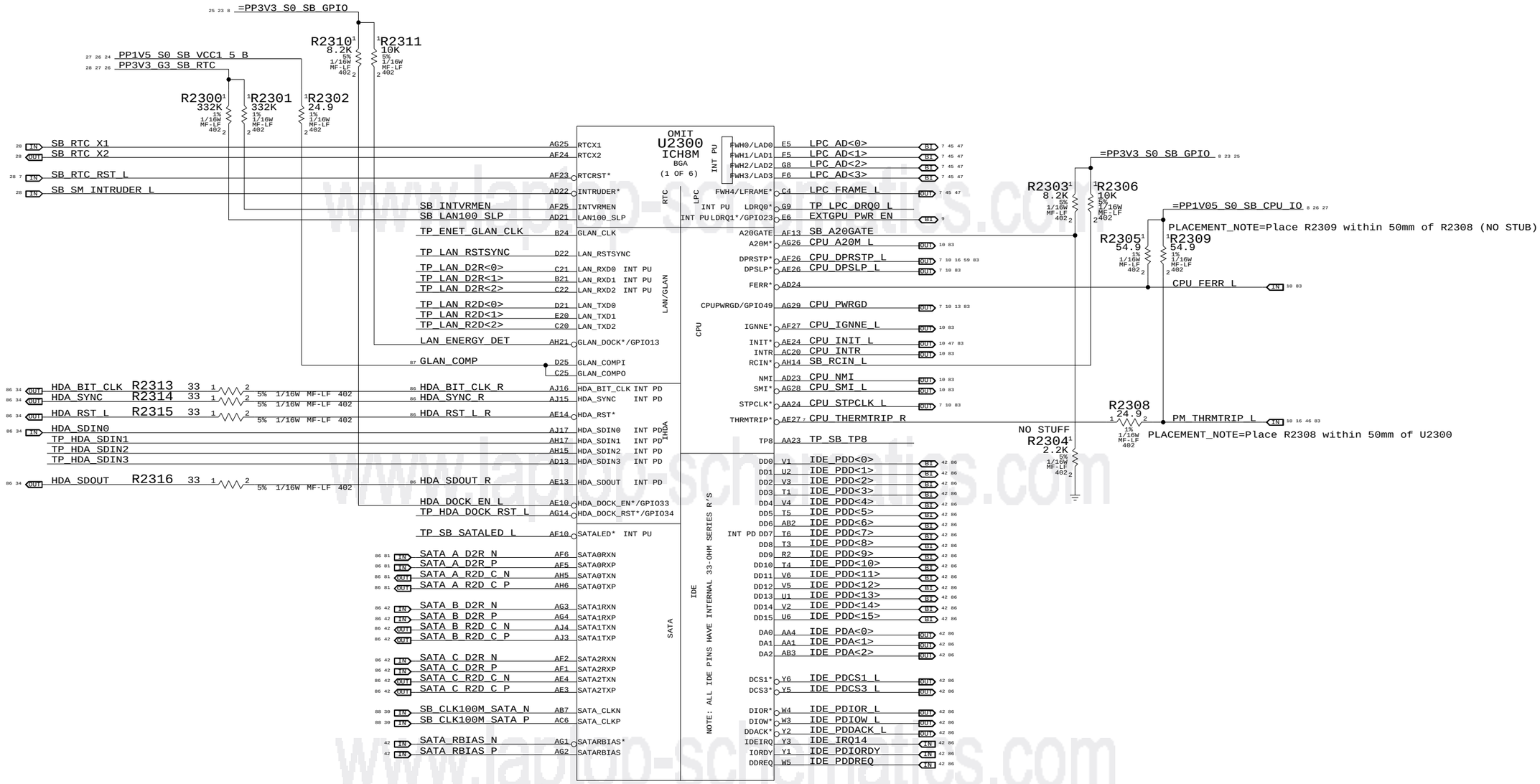
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 22 OF 109	

www.laptop-schematics.com



	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

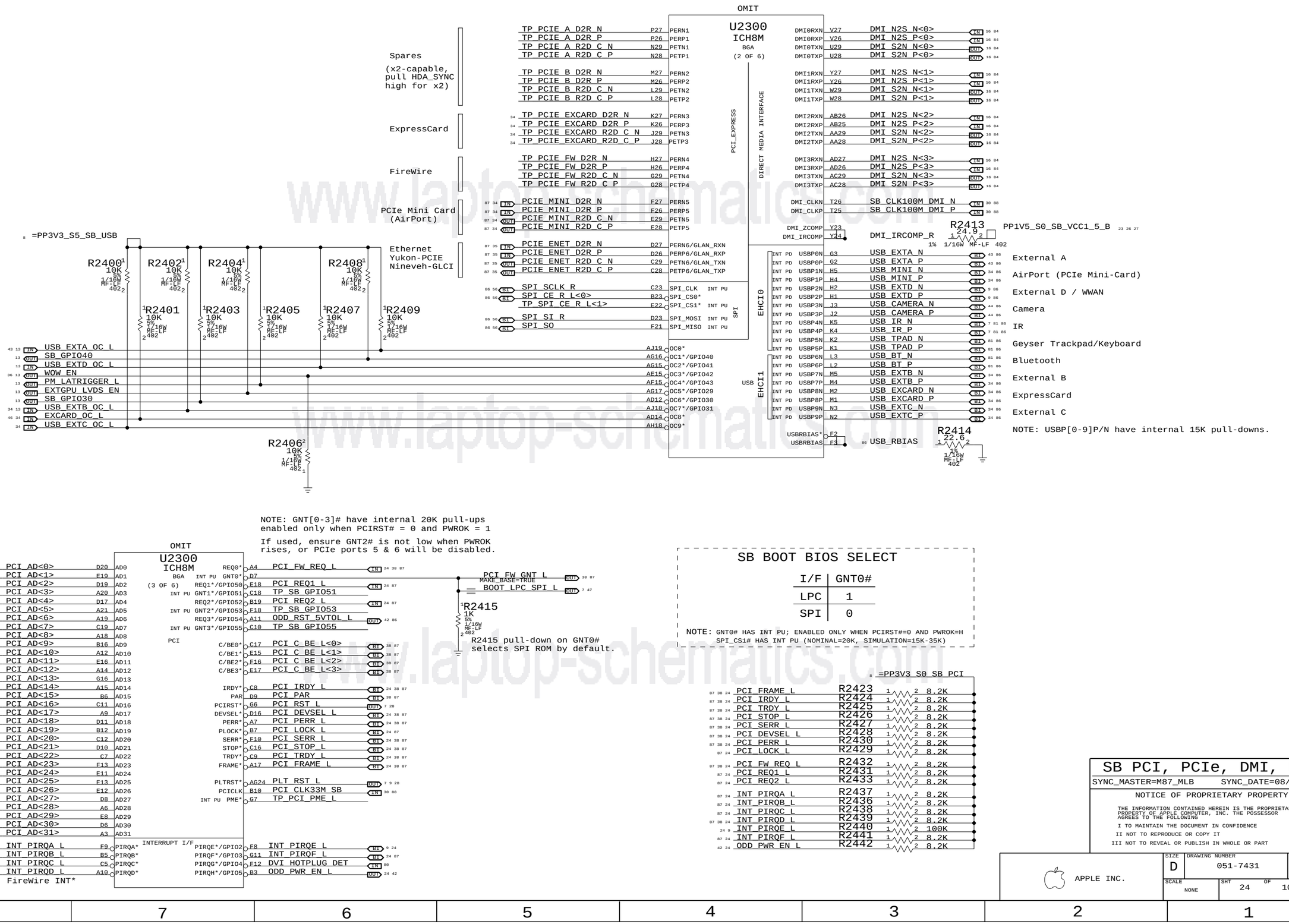
II NOT TO REPRODUCE OR COPY IT

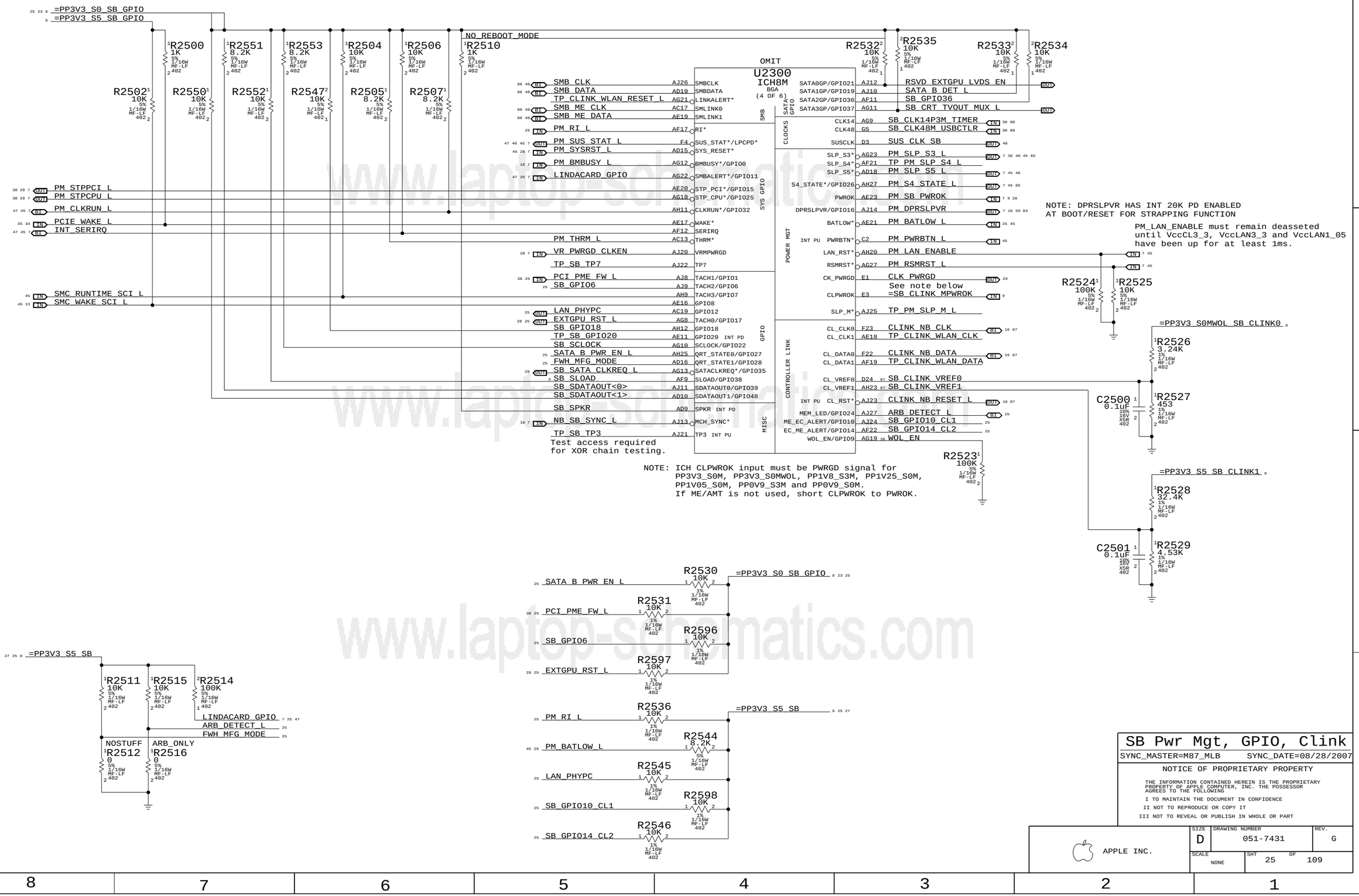
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 23 OF 109	

www.laptop-schematics.com


OMIT
U2300
ICH8M
BGA
(2 OF 6)
PCI_EXPRESS
DIRECT MEDIA INTERFACE
SPI
EHCI0
EHCI1
USB
Spares
(x2-capable, pull HDA_SYNC high for x2)
ExpressCard
FireWire
PCIe Mini Card (AirPort)
Ethernet Yukon-PCIE Nineveh-GLCI
TP_PCIE_A_D2R_N
TP_PCIE_A_D2R_P
TP_PCIE_A_R2D_C_N
TP_PCIE_A_R2D_C_P
TP_PCIE_B_D2R_N
TP_PCIE_B_D2R_P
TP_PCIE_B_R2D_C_N
TP_PCIE_B_R2D_C_P
TP_PCIE_EXCARD_D2R_N
TP_PCIE_EXCARD_D2R_P
TP_PCIE_EXCARD_R2D_C_N
TP_PCIE_EXCARD_R2D_C_P
TP_PCIE_FW_D2R_N
TP_PCIE_FW_D2R_P
TP_PCIE_FW_R2D_C_N
TP_PCIE_FW_R2D_C_P
PCIE_MINI_D2R_N
PCIE_MINI_D2R_P
PCIE_MINI_R2D_C_N
PCIE_MINI_R2D_C_P
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
SPI_SCLK_R
SPI_CE_R_L<0>
TP_SPI_CE_R_L<1>
SPI_SI_R
SPI_SO
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
DMI_N2S_N<0>
DMI_N2S_P<0>
DMI_S2N_N<0>
DMI_S2N_P<0>
DMI_N2S_N<1>
DMI_N2S_P<1>
DMI_S2N_N<1>
DMI_S2N_P<1>
DMI_N2S_N<2>
DMI_N2S_P<2>
DMI_S2N_N<2>
DMI_S2N_P<2>
DMI_N2S_N<3>
DMI_N2S_P<3>
DMI_S2N_N<3>
DMI_S2N_P<3>
SB_CLK100M_DMI_N
SB_CLK100M_DMI_P
DMI_IRCOMP_R
R2413 24.9 1% 1/16W MF-LF 402
PP1V5_S0_SB_VCC1_5_B
USB_EXTA_N
USB_EXTA_P
USB_MINI_N
USB_MINI_P
USB_EXTD_N
USB_EXTD_P
USB_CAMERA_N
USB_CAMERA_P
USB_IR_N
USB_IR_P
USB_TPAD_N
USB_TPAD_P
USB_BT_N
USB_BT_P
USB_EXTB_N
USB_EXTB_P
USB_EXCARD_N
USB_EXCARD_P
USB_EXTC_N
USB_EXTC_P
USBRBIAS*
USBRBIAS
USB_RBIAS
R2414 22.6 1% 1/16W MF-LF 402
External A
AirPort (PCIe Mini-Card)
External D / WWAN
Camera
IR
Geyser Trackpad/Keyboard
Bluetooth
External B
ExpressCard
External C
NOTE: USBP[0-9]P/N have internal 15K pull-downs.
=PP3V3_S5_SB_USB
R2400 10K 5% 1/10W MF-LF 402
R2401 10K 5% 1/16W MF-LF 402
R2402 10K 5% 1/10W MF-LF 402
R2403 10K 5% 1/16W MF-LF 402
R2404 10K 5% 1/10W MF-LF 402
R2405 10K 5% 1/16W MF-LF 402
R2406 10K 5% 1/10W MF-LF 402
R2407 10K 5% 1/16W MF-LF 402
R2408 10K 5% 1/10W MF-LF 402
R2409 10K 5% 1/16W MF-LF 402
USB_EXTA_OC_L
SB_GPIO40
USB_EXTD_OC_L
WOW_EN
PM_LATRIGGER_L
EXTGPU_LVDS_EN
SB_GPIO30
USB_EXTB_OC_L
EXCARD_OC_L
USB_EXTC_OC_L
OC0*
OC1*/GPIO40
OC2*/GPIO41
OC3*/GPIO42
OC4*/GPIO43
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
OC8*
OC9*
NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1
If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.
PCI_AD<0>
PCI_AD<1>
PCI_AD<2>
PCI_AD<3>
PCI_AD<4>
PCI_AD<5>
PCI_AD<6>
PCI_AD<7>
PCI_AD<8>
PCI_AD<9>
PCI_AD<10>
PCI_AD<11>
PCI_AD<12>
PCI_AD<13>
PCI_AD<14>
PCI_AD<15>
PCI_AD<16>
PCI_AD<17>
PCI_AD<18>
PCI_AD<19>
PCI_AD<20>
PCI_AD<21>
PCI_AD<22>
PCI_AD<23>
PCI_AD<24>
PCI_AD<25>
PCI_AD<26>
PCI_AD<27>
PCI_AD<28>
PCI_AD<29>
PCI_AD<30>
PCI_AD<31>
INT_PIRQA_L
INT_PIRQB_L
INT_PIRQC_L
INT_PIRQD_L
FireWire INT*
PCI_FW_REQ_L
PCI_REQ1_L
TP_SB_GPIO51
PCI_REQ2_L
TP_SB_GPIO53
ODD_RST_5VTOL_L
TP_SB_GPIO55
PCI_FW_GNT_L
MAKE_BASE=TRUE
BOOT_LPC_SPI_L
R2415 1K 5% 1/16W MF-LF 402
R2415 pull-down on GNT0# selects SPI ROM by default.
PCI_C_BE_L<0>
PCI_C_BE_L<1>
PCI_C_BE_L<2>
PCI_C_BE_L<3>
PCI_IRDY_L
PCI_PAR
PCI_RST_L
PCI_DEVSEL_L
PCI_PERR_L
PCI_LOCK_L
PCI_SERR_L
PCI_STOP_L
PCI_TRDY_L
PCI_FRAME_L
PLT_RST_L
PCI_CLK33M_SB
TP_PCI_PME_L
INT_PIRQE_L
INT_PIRQF_L
DVI_HOTPLUG_DET
ODD_PWR_EN_L
SB BOOT BIOS SELECT
I/F | GNT0#
LPC | 1
SPI | 0
NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
=PP3V3_S0_SB_PCI
R2423 8.2K
R2424 8.2K
R2425 8.2K
R2426 8.2K
R2427 8.2K
R2428 8.2K
R2430 8.2K
R2429 8.2K
R2432 8.2K
R2431 8.2K
R2433 8.2K
R2437 8.2K
R2436 8.2K
R2438 8.2K
R2439 8.2K
R2440 100K
R2441 8.2K
R2442 8.2K
SB PCI, PCIe, DMI, USB
SYNC_MASTER=M87_MLB
SYNC_DATE=08/28/2007
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE D
DRAWING NUMBER 051-7431
REV. G
SCALE NONE
SHT 24 OF 109



www.laptop-schematics.com

SB Pwr Mgt, GPIO, Clink		
SYNC_MASTER=M87_MLB	SYNC_DATE=08/28/2007	

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	G
	SCALE: NONE	SHT 25 OF 109	

www.laptop-schematics.com

U2300
ICH8M
BGA
(5 OF 6)
OMIT

VSS: A23, A5, AA2, AA7, A25, AB1, AB24, AC11, AC14, AC25, AC26, AC27, AD17, AD20, AD28, AD29, AD3, AD4, AD6, AE1, AE12, AE2, AE22, AD1, AE25, AE5, AE6, AE9, AF14, AF16, AF18, AF3, AF4, AG5, AG6, AH10, AH13, AH16, AH19, AH2, AF28, AH22, AH24, AH26, AH3, AH4, AH8, AJ5, B11, B14, B17, B2, B20, B22, B8, C24, C26, C27, C6, D12, D15, D18, D2, D4, E21, E24, E4, E9, F15, E23, F28, F29, F7, G1, E2, G10, G13, G19, G23, G25, G26, G27, H25, H28, H29, H3, H6, J1, J25, J26, J27, J4, J5, K23, K28, K29, K3, K6

VSS: K7, L1, L13, L15, L26, L27, L4, L5, M12, M13, M14, M15, M16, M17, M23, M28, M29, M3, N1, N11, N12, N13, N14, N15, N16, N17, N18, N26, N27, N4, N5, N6, P12, P13, P14, P15, P16, P17, P23, P28, P29, P11, R11, R12, R13, R14, R15, R16, R17, R18, R28, R4, T12, T13, T14, T15, T16, T17, T2, U12, U13, U14, U15, U16, U17, U23, U26, U27, U3, U5, V13, V15, V28, V29, W2, W26, W27, Y28, Y29, Y4, AB4, AB23, AB5, AB6, AD5, U4, W24

VSS_NCTF: A1, A2, A28, A29, AH1, AH29, AJ1, AJ2, AJ28, AJ29, B1, B29

6 uA S0-G3	28 27 23	PP3V3_G3_SB_RTC	AD25 VCCRTC
1 mA	27	PP5V_S0_SB_V5REF	A16, T7 V5REF
1 mA S0-S5	27	PP5V_S5_SB_V5REF_SUS	G4 V5REF_SUS
657 mA	27 24 23	PP1V5_S0_SB_VCC1_5_B	AA25, AA26, AA27, AB27, AB28, AB29, D28, D29, E25, E26, E27, F24, F25, G24, H23, H24, J23, J24, K24, K25, L23, L24, L25, M24, M25, N23, N24, N25, P24, P25, R24, R25, R26, R27, T23, T24, T27, T28, T29, U24, W25, V24, U25, Y25, V25, V23 VCC1_5_B
47 mA	27	PP1V5_S0_SB_VCCSATAPLL	AJ6 VCCSATAPLL
	27 8	=PP1V5_S0_SB_VCC1_5_A_ARX	AE7, AF7, AG7, AH7, AJ7 VCC1_5_A (ARX)
1080 mA (VCC1_5_A total)	27 8	=PP1V5_S0_SB_VCC1_5_A_ATX	AC1, AC2, AC3, AC4, AC5 VCC1_5_A (ATX)
	8	=PP1V5_S0_SB_VCC1_5_A	AC10, AC9 VCC1_5_A; AA5, AA6 VCC1_5_A; G12, G17 VCC1_5_A
	27 8	=PP1V5_S0_SB_VCC1_5_A_USB_CORE	H7, AC7, AD7 VCC1_5_A
10 mA	27 8	=PP1V5_S0_SB_VCCUSBPLL	D1 VCCUSBPLL
			F1, L6, L7, M6, M7 VCC1_5_A (USB CORE)
			W23 VCC1_5_A24
		TP_VCCLAN1_05_INTERNAL_REG1	F17 VCCLAN1_05
		TP_VCCLAN1_05_INTERNAL_REG2	G18
19 mA S0, 63 mA M1 & WOL	27 8	=PP3V3_S0MWOL_SB_VCCCL3_3	F20, G21 VCCCL3_3
23 mA	27	PP1V5_S0_SB_VCCGLANPLL	A24 VCCGLANPLL
80 mA	27	=PP1V5_S0_SB_VCCGLAN1_5	B27, A27, B28, B26, A26 VCCGLAN1_5 (GLAN POWER)
1 mA	8	=PP3V3_S0_SB_VCCGLAN3_3	B25 VCCGLAN3_3

U2300
ICH8M
BGA
(6 OF 6)
OMIT

VCCA3GP

CORE — VCC1_05: A13, B13, C13, D14, E14, F14, G14, L11, L12, L14, L16, L17, L18, M11, M18, P11, P18, T11, T18, U18, V17, V14, V11, U11, V18, V16, V12

VCCDMIPLL	R29	PP1V5_S0_SB_VCCDMIPLL	27 — 23 mA
VCC_DMI	AE28, AE29	=PP1V25_S0_SB_DMI	8 27 — 50 mA
V_CPU_IO	AC23, AC24	=PP1V05_S0_SB_CPU_IO	8 23 27 — 1 mA
VCC3_3	AF29	=PP3V3_S0_SB_VCC3_3_DMI	8 27
VCC3_3	AD2	=PP3V3_S0_SB_VCC3_3_SATA	8 27

VCCP CORE — AC8, AD8, VCC3_3 AE8, AF8: =PP3V3_S0_SB_VCC3_3_VCCPCORE (8)

IDE — AA3, U7, V7, VCC3_3 W1, W6, W7, Y7: =PP3V3_S0_SB_VCC3_3_IDE (8 27) — 442 mA (VCC3_3 total)

PCI — A8, B15, B18, B4, B9, VCC3_3 C15, D13, D5, E10, E7, F11: =PP3V3_S0_SB_VCC3_3_PCI (8 27)

VCCHDA	AC12	=PP3V3R1V5_S0_SB_VCCHDA	8 27 — 32 mA
VCCSUSHDA	AD11	=PP3V3_S5_SB_3V3_VCCSUSHDA	8 27 — 11 mA S0, 1 mA S3-S5
	J6	TP_VCCSUS1_05_INTERNAL_REG1	
VCCSUS1_05	AF20	TP_VCCSUS1_05_INTERNAL_REG2	
VCCSUS1_5	AC16	TP_VCCSUS1_5_INTERNAL_REG1	
VCCSUS1_5	J7	TP_VCCSUS1_5_INTERNAL_REG2	
VCCSUS3_3	C3	=PP3V3_S5_SB_VCCSUS3_3	8 27

VCCP SUS — AC18, AD21, VCCSUS3_3 AC22, AD20, AH28: =PP3V3_S5_SB_VCCSUS3_3_USB (8 27) — 117 mA S0, 44 mA S3-S5 (VCCSUS3_3 total)

VCCP USB — P6, P7, C1, N7, P1, P2, VCCSUS3_3 P3, P4, P5, R1, R3, R5, R6

VCCCL1_05	G22	TP_VCCCL1_05_INTERNAL_REG	
VCCCL1_5	A22	VCCCL1_5V	
VCCLAN3_3	F19, G20	=PP3V3_S0MWOL_SB_VCCLAN3_3_3	8 27 — 19 mA S0, 51 mA M1 & WOL

C2600 1uF 10% 6.3V CERM 402 — C2601 0.1uF 20% 10V CERM 402 (1, 2)

NOTE:
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.
Current figures provided assume 1.5V.

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

SB Power & Ground

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 26 OF 109	

www.laptop-schematics.com

=PP3V3_S5_SB
=PP5V_S5_SB
1 mA S0-S5

ICH V5REF_SUS Filter & Follower
(ICH Reference for 5V Tolerance on Resume Well Inputs)

R2701 10 5% 1/16W MF-LF 402
D2702 BAT54DW SOT-363

PP5V_S5_SB_V5REF_SUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V

C2704 0.1UF 10% 16V X5R 402
1 mA S0-S5

PLACEMENT NOTE:
PLACE C2704 < 2.54MM OF PIN G4 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

=PP3V3_S0_SB
=PP5V_S0_SB
1 mA

ICH V5REF Filter & Follower
(ICH Reference for 5V Tolerance on Core Well Inputs)

R2702 100 5% 1/16W MF-LF 402
D2702 BAT54DW SOT-363

PP5V_S0_SB_V5REF
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V

C2703 1UF 10% 16V X5R 402
1 mA

PLACEMENT NOTE:
PLACE C2703 < 2.54MM OF PIN A16..T7 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

PLACEMENT NOTE:
PLACE C2700 & C2705-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
DISTRIBUTED BETWEEN AA25..V23

ICH VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)

=PP1V5_S0_SB
837 mA

L2700 FERR-330-OHM-1.5A 0805-1

C2700 220UF 20% 6.3V 60MV CASE-B2-SM CRITICAL
C2705 22UF 20% 6.3V CERM-X5R 805-3
C2706 22UF 20% 6.3V CERM-X5R 805-3
C2707 2.2UF 20% 6.3V CERM1 603

PP1V5_S0_SB_VCC1_5_B
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MARK_BASE=TRUE
657 mA

=PP1V5_S0_SB_VCCGLAN1_5
80 mA

C2736 4.7UF 20% 6.3V CERM 603

PLACEMENT NOTE:
PLACE C2736 NEAR PIN B27..A26

ICH VCCGLANPLL Filter
(ICH GLAN PLL PWR)

PP1V5_S0_SB_VCCGLANPLL
33 mA

C2732 2.2UF 20% 6.3V CERM1 603

PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN A24

ICH VCCSATAPLL Filter
(ICH SATA PLL PWR)

R2735 0 5% 1/16W MF-LF 402
PP1V5_S0_SB_VCCSATAPLL_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
47 mA

L2702 10UH-100MA 0805

C2735 10UF 20% 6.3V X5R 805 603

PP1V5_S0_SB_VCCSATAPLL
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
47 mA

C2717 1UF 10% 6.3V CERM 402

PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AJ6

ICH VCCDMIPLL Filter
(ICH DMI PLL PWR)

R2700 1 5% 1/10W MF-LF 603
PP1V5_S0_SB_VCCDMIPLL_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
23 mA

L2703 1.0UH-0.5A 1210

C2708 10UF 20% 6.3V X5R 805 603

PP1V5_S0_SB_VCCDMIPLL
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
23 mA

C2701 0.01UF 10% 16V X7R 402

PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)

0.6 uA G3

PP3V3_G3_SB_RTC

C2729 0.1UF 10% 16V X5R 402
C2730 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE CAPS NEAR PIN AD25 OF SB

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)

=PP3V3_S5_SB_VCCSUS3_3

C2731 0.1UF 10% 16V X5R 402
C2734 0.1UF 10% 16V X5R 402

(VCCSUS3_3 Total)
117 mA S0 /
44 mA S3-S5

PLACEMENT NOTE:
PLACE CAPS NEAR PINS AC18..AH28

ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)

=PP3V3_S5_SB_VCCSUS3_3_USB

C2733 4.7UF 20% 6.3V CERM 603

PLACEMENT NOTE:
PLACE CAP NEAR PINS
P6..R6

ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)

38 mA S0 /
114 mA M1 & WOL

=PP3V3_S0MWOL_SB_VCCLAN3_3
=PP3V3_S0MWOL_SB_VCCCL3_3

C2719 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS
F19 AND G20

ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)

=PP3V3_S0_SB_VCC3_3_IDE

C2725 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA3...Y7

=PP3V3_S0_SB_VCC3_3_SATA

C2738 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD2

(VCC3_3 Total)
442 mA

=PP3V3_S0_SB_VCC3_3_DMI

C2737 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE CAP < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AF29

ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)

=PP3V3_S0_SB_VCC3_3_PCI

C2726 0.1UF 10% 16V X5R 402
C2727 0.1UF 10% 16V X5R 402
C2728 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A8 ... F11

ICH VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V/1.5V PWR)

32 mA
(@ 1.5V)

=PP3V3R1V5_S0_SB_VCCHDA

C2721 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AC12

ICH VCCSUSHDA BYPASS
(ICH INTEL HDA SUSPEND 3.3V/1.5V PWR)

11 mA S0 /
1 mA S3-S5
(@ 1.5V)

=PP3V3_S5_SB_3V3_VCCSUSHDA

C2741 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD11

ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)

=PP1V5_S0_SB_VCC1_5_A_ARX

C2711 1UF 10% 6.3V CERM 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AE7..AJ7

ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)

(VCC1_5_A Total)
1080 mA

=PP1V5_S0_SB_VCC1_5_A_ATX

C2714 1UF 10% 6.3V CERM 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AC1..AC5

ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)

=PP1V5_S0_SB_VCC1_5_A_USB_CORE

C2712 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS F1..M7

ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)

10 mA

=PP1V5_S0_SB_VCCUSBPLL

C2715 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE C2715 NEAR PIN D1 OF SB

50 mA

=PP1V25_S0_SB_DMI

C2739 22UF 20% 6.3V CERM-X5R 805-3

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AE29

ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)

1130 mA

=PPVCORE_S0_SB

C2718 0.1UF 10% 16V X5R 402
C2702 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB

ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)

1 mA

=PP1V05_S0_SB_CPU_IO

C2724 4.7UF 20% 6.3V CERM 603
C2723 0.1UF 10% 16V X5R 402
C2722 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE NEAR PINS AC23,AC24 OF SB

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

SB Decoupling

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

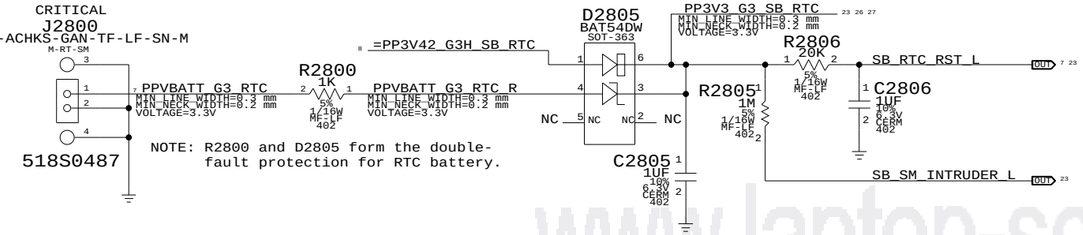
SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 27 OF 109	

RTC Power Sources

Coin-Cell Connector

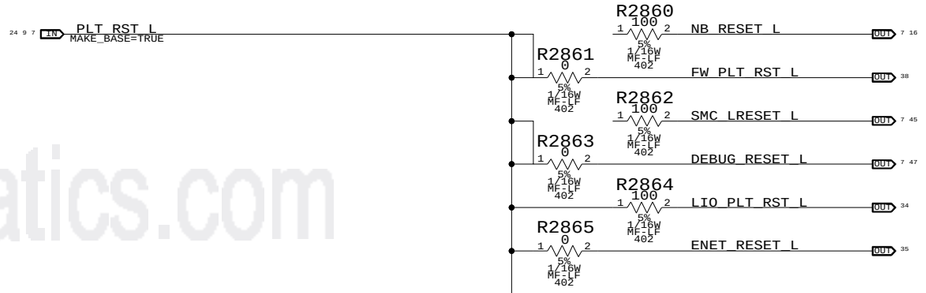
CRITICAL
J2800
BM02B-ACHKS-GAN-TF-LF-SN-M
M-RT-SM
518S0487

NOTE: R2800 and D2805 form the double-fault protection for RTC battery.

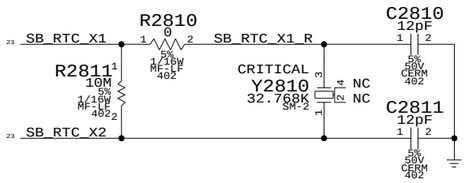


Platform Reset Connections

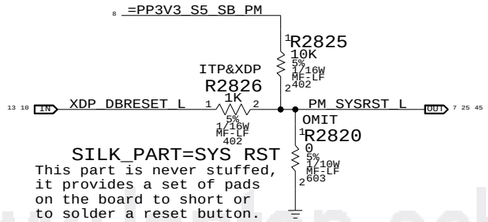
Unbuffered



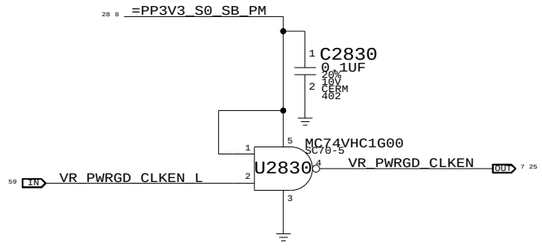
SB RTC Crystal



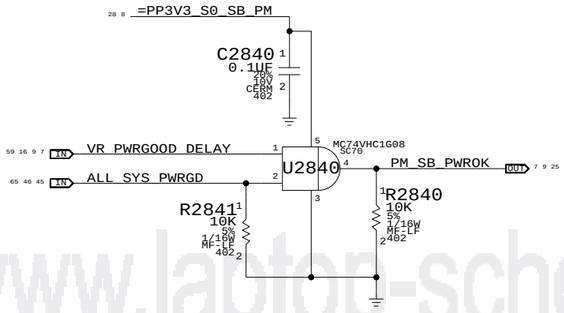
System Reset "Button"



VRMPWRGD Inverter

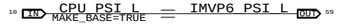


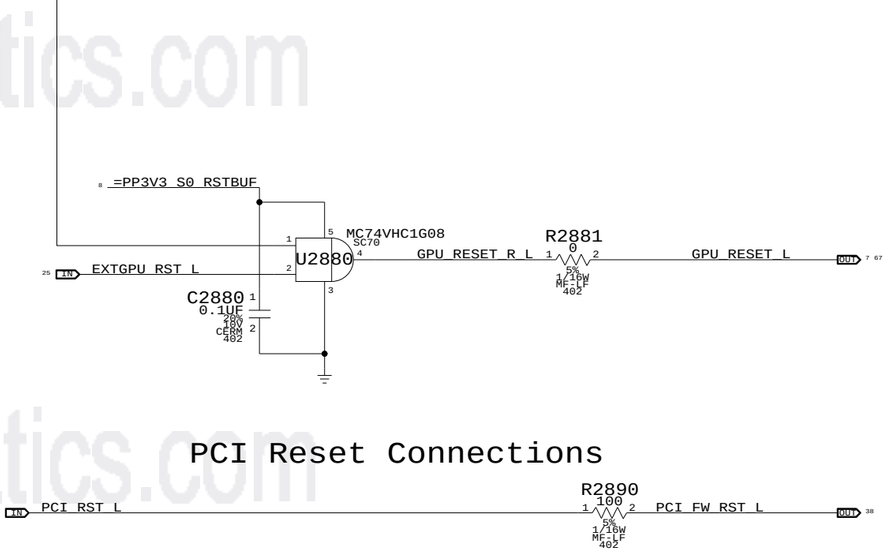
PWROK Circuit



PCI Reset Connections

CPU VCore ForcePSI





SB Misc

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

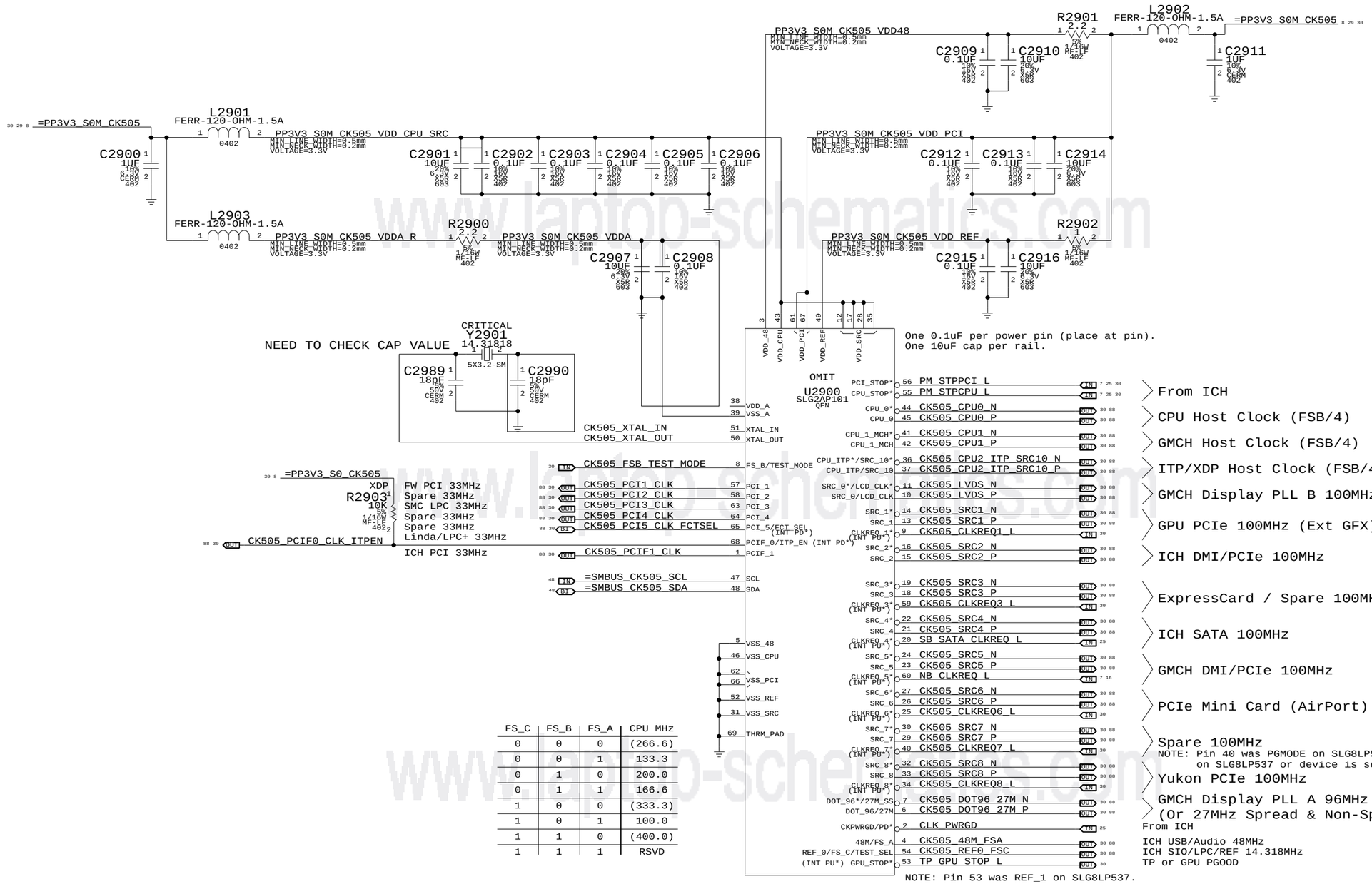
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 28 OF 109	

www.laptop-schematics.com



FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

Clock (CK505)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

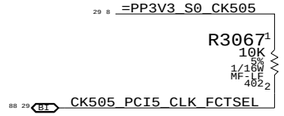
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 29 OF 109	

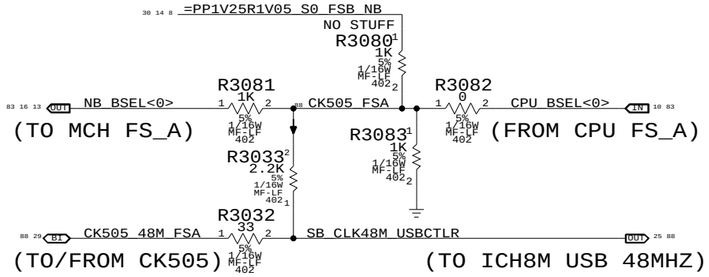
www.laptop-schematics.com

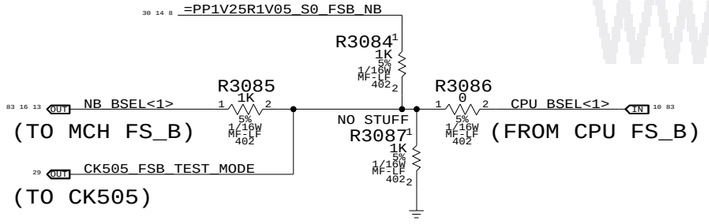
CK505 Configuration Straps

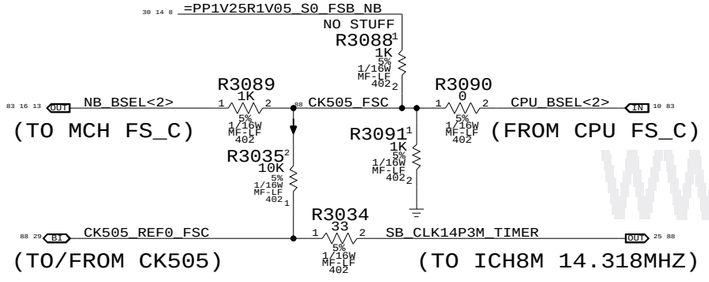
FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)







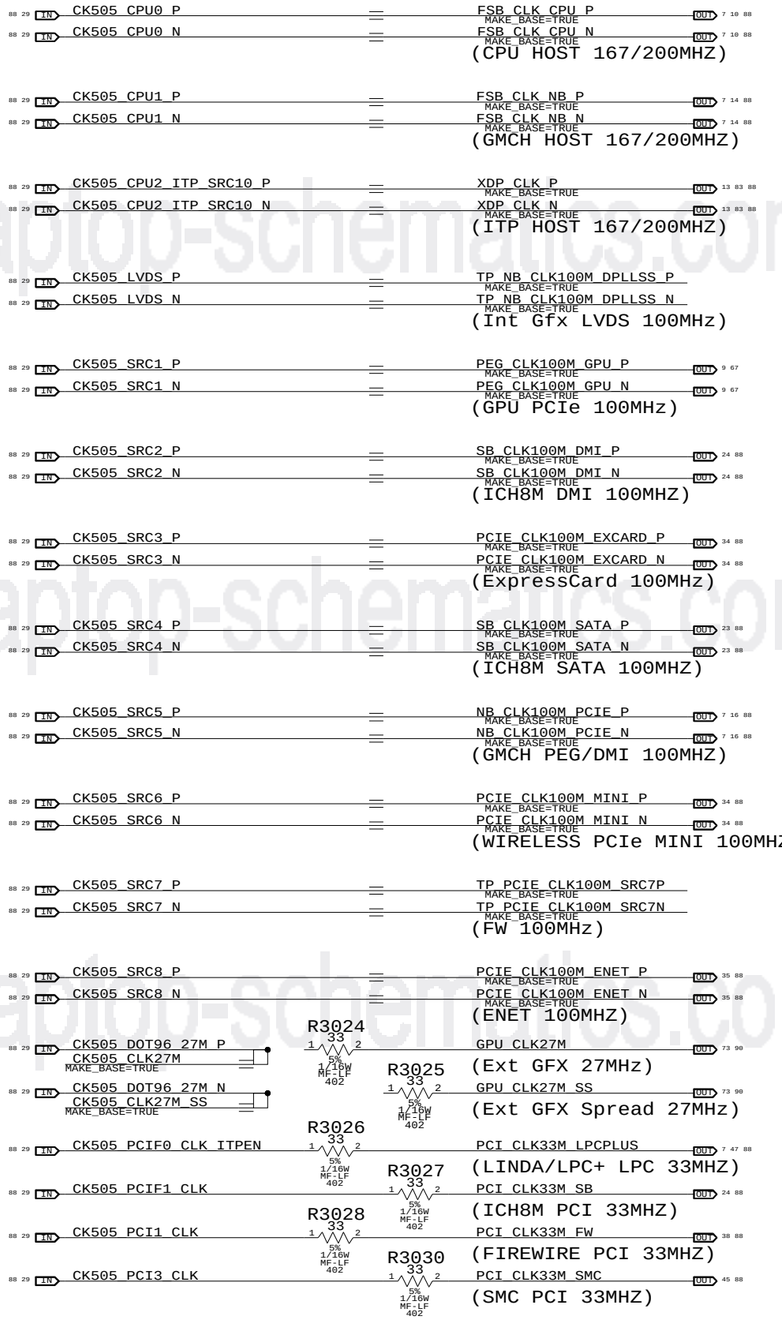
FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

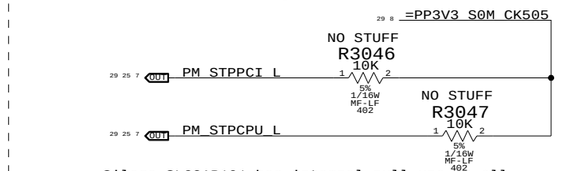
(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

CLK Termination

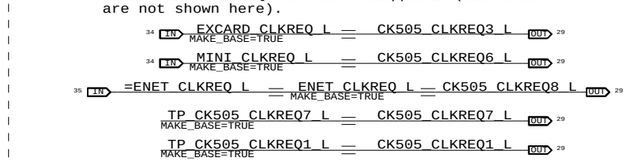
(Note: HOST/SRC/GFX clock termination removed. Silego SL8GLP536 or equiv. support only)



CLKREQ Controls



Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).



GPU Clock Gating

Unused Clocks

www.laptop-schematics.com

Clock Termination

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 30 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

"Factory" (thru-hole) slot

=PP0V9_S3M_MEM_DIMMVREFA

C3101 2.2uF 20% 6.3V CERM 603

C3100 0.1uF 20% 10V CERM 402

=PP1V8_S3M_MEM_A

CRITICAL
J3100
F-RT-TH1
DDR2-SODIMM-DUAL

	1B	VREF		2B	VSS0		
	3B	VSS1		4B	DQ4	MEM_A_DQ<9>	17 85
MEM_A_DQ<14>	5B	DQ0		6B	DQ5	MEM_A_DQ<15>	17 85
MEM_A_DQ<13>	7B	DQ1		8B	VSS2		
	9B	VSS4		10B	DM0	MEM_A_DM<1>	17 85
MEM_A_DQS_N<1>	11B	DQS0*		12B	VSS5		
MEM_A_DQS_P<1>	13B	DQS0		14B	DQ6	MEM_A_DQ<8>	17 85
	15B	VSS6		16B	DQ7	MEM_A_DQ<12>	17 85
MEM_A_DQ<10>	17B	DQ2		18B	VSS7		
MEM_A_DQ<11>	19B	DQ3		20B	DQ12	MEM_A_DQ<2>	17 85
	21B	VSS8		22B	DQ13	MEM_A_DQ<3>	17 85
MEM_A_DQ<7>	23B	DQ8		24B	VSS9		
MEM_A_DQ<0>	25B	DQ9		26B	DM1	MEM_A_DM<0>	17 85
	27B	VSS10		28B	VSS11		
MEM_A_DQS_N<0>	29B	DQS1*		30B	CK0	MEM_CLK_P<0>	16 85
MEM_A_DQS_P<0>	31B	DQS1		32B	CK0*	MEM_CLK_N<0>	16 85
	33B	VSS12		34B	VSS13		
MEM_A_DQ<6>	35B	DQ10		36B	DQ14	MEM_A_DQ<1>	17 85
MEM_A_DQ<4>	37B	DQ11		38B	DQ15	MEM_A_DQ<5>	17 85
	39B	VSS14	KEY	40B	VSS15		
	41B	VSS16		42B	VSS17		
MEM_A_DQ<17>	43B	DQ16		44B	DQ20	MEM_A_DQ<18>	17 85
MEM_A_DQ<21>	45B	DQ17		46B	DQ21	MEM_A_DQ<20>	17 85
	47B	VSS18		48B	VSS19		
MEM_A_DQS_N<2>	49B	DQS2*		50B	NC0	PM_EXTTS_L<0>	16 45
MEM_A_DQS_P<2>	51B	DQS2		52B	DM2	MEM_A_DM<2>	17 85
	53B	VSS21		54B	VSS22		
MEM_A_DQ<23>	55B	DQ18		56B	DQ22	MEM_A_DQ<22>	17 85
MEM_A_DQ<16>	57B	DQ19		58B	DQ23	MEM_A_DQ<19>	17 85
	59B	VSS23		60B	VSS24		
MEM_A_DQ<31>	61B	DQ24		62B	DQ28	MEM_A_DQ<26>	17 85
MEM_A_DQ<27>	63B	DQ25		64B	DQ29	MEM_A_DQ<24>	17 85
	65B	VSS25		66B	VSS26		
MEM_A_DM<3>	67B	DM3		68B	DQS3*	MEM_A_DQS_N<3>	17 85
NC	69B	NC1		70B	DQS3	MEM_A_DQS_P<3>	17 85
	71B	VSS27		72B	VSS28		
MEM_A_DQ<30>	73B	DQ26		74B	DQ30	MEM_A_DQ<25>	17 85
MEM_A_DQ<28>	75B	DQ27		76B	DQ31	MEM_A_DQ<29>	17 85
	77B	VSS29		78B	VSS30		
MEM_CKE<0>	79B	CKE0		80B	NC/CKE1	MEM_CKE<1>	16 33 85
	81B	VDD0		82B	VDD1		
NC	83B	NC2		84B	NC/A15	MEM_A_A<15>	9
MEM_A_BS<2>	85B	BA2		86B	NC/A14	MEM_A_A<14>	16 33 85
	87B	VDD2		88B	VDD3		
MEM_A_A<12>	89B	A12		90B	A11	MEM_A_A<11>	17 33 85
MEM_A_A<9>	91B	A9		92B	A7	MEM_A_A<7>	17 33 85
MEM_A_A<8>	93B	A8		94B	A6	MEM_A_A<6>	17 33 85
	95B	VDD4		96B	VDD5		
MEM_A_A<5>	97B	A5		98B	A4	MEM_A_A<4>	17 33 85
MEM_A_A<3>	99B	A3		100B	A2	MEM_A_A<2>	17 33 85
MEM_A_A<1>	101B	A1		102B	A0	MEM_A_A<0>	17 33 85
	103B	VDD6		104B	VDD7		
MEM_A_A<10>	105B	A10/AP		106B	BA1	MEM_A_BS<1>	17 33 85
MEM_A_BS<0>	107B	BA0		108B	RAS*	MEM_A_RAS_L	17 33 85
MEM_A_WE_L	109B	WE*		110B	S0*	MEM_CS_L<0>	16 33 85
	111B	VDD8		112B	VDD9		
MEM_A_CAS_L	113B	CAS*		114B	ODT0	MEM_ODT<0>	16 33 85
MEM_CS_L<1>	115B	NC/S1*		116B	NC/A13	MEM_A_A<13>	17 33 85
	117B	VDD10		118B	VDD11		
MEM_ODT<1>	119B	NC/ODT1		120B	NC3	NC	
	121B	VSS31		122B	VSS32		
MEM_A_DQ<36>	123B	DQ32		124B	DQ36	MEM_A_DQ<35>	17 85
MEM_A_DQ<38>	125B	DQ33		126B	DQ37	MEM_A_DQ<39>	17 85
	127B	VSS33		128B	VSS34		
MEM_A_DQS_N<4>	129B	DQS4*		130B	DM4	MEM_A_DM<4>	17 85
MEM_A_DQS_P<4>	131B	DQS4		132B	VSS35		
	133B	VSS36		134B	DQ38	MEM_A_DQ<33>	17 85
MEM_A_DQ<37>	135B	DQ34		136B	DQ39	MEM_A_DQ<32>	17 85
MEM_A_DQ<34>	137B	DQ35		138B	VSS37		
	139B	VSS38		140B	DQ44	MEM_A_DQ<63>	17 85
MEM_A_DQ<56>	141B	DQ40		142B	DQ45	MEM_A_DQ<62>	17 85
MEM_A_DQ<59>	143B	DQ41		144B	VSS39		
	145B	VSS40		146B	DQS7*	MEM_A_DQS_N<7>	17 85
MEM_A_DM<7>	147B	DM5		148B	DQS5	MEM_A_DQS_P<7>	17 85
	149B	VSS41		150B	VSS42		
MEM_A_DQ<58>	151B	DQ42		152B	DQ46	MEM_A_DQ<57>	17 85
MEM_A_DQ<60>	153B	DQ43		154B	DQ47	MEM_A_DQ<61>	17 85
	155B	VSS43		156B	VSS44		
MEM_A_DQ<51>	157B	DQ48		158B	DQ52	MEM_A_DQ<55>	17 85
MEM_A_DQ<54>	159B	DQ49		160B	DQ53	MEM_A_DQ<50>	17 85
	161B	VSS45		162B	VSS46		
NC	163B	NC_TEST		164B	CK1	MEM_CLK_P<1>	16 85
	165B	VSS47		166B	CK1*	MEM_CLK_N<1>	16 85
MEM_A_DQS_N<6>	167B	DQS6*		168B	VSS48		
MEM_A_DQS_P<6>	169B	DQS6		170B	DM6	MEM_A_DM<6>	17 85
	171B	VSS49		172B	VSS50		
MEM_A_DQ<48>	173B	DQ50		174B	DQ54	MEM_A_DQ<49>	17 85
MEM_A_DQ<53>	175B	DQ51		176B	DQ55	MEM_A_DQ<52>	17 85
	177B	VSS51		178B	VSS52		
MEM_A_DQ<43>	179B	DQ56		180B	DQ60	MEM_A_DQ<45>	17 85
MEM_A_DQ<42>	181B	DQ57		182B	DQ61	MEM_A_DQ<40>	17 85
	183B	VSS53		184B	VSS54		
MEM_A_DM<5>	185B	DM7		186B	DQS7*	MEM_A_DQS_N<5>	17 85
	187B	VSS55		188B	DQS7	MEM_A_DQS_P<5>	17 85
MEM_A_DQ<46>	189B	DQ58		190B	VSS56		
MEM_A_DQ<41>	191B	DQ59		192B	DQ62	MEM_A_DQ<44>	17 85
=PPSPD_S0M_MEM_A	193B	VSS57		194B	DQ63	MEM_A_DQ<47>	17 85
=I2C_SODIMMA_SDA	195B	SDA		196B	VSS58		
=I2C_SODIMMA_SCL	197B	SCL		198B	SA0		
	199B	VDDSPD		200B	SA1	ADDR=0xA0(WR)/0xA1(RD)	

516-0140

DDR2 Bypass Caps
(For return current)

=PP1V8_S3M_MEM_A

C3108 10UF 20% 6.3V X5R 603

C3109 10UF 20% 6.3V X5R 603

C3110 1UF 10% 6.3V CERM 402

C3111 1UF 10% 6.3V CERM 402

C3112 1UF 10% 6.3V CERM 402

C3113 1UF 10% 6.3V CERM 402

C3114 1UF 10% 6.3V CERM 402

C3115 1UF 10% 6.3V CERM 402

C3116 1UF 10% 6.3V CERM 402

C3117 1UF 10% 6.3V CERM 402

C3118 1UF 10% 6.3V CERM 402

C3119 1UF 10% 6.3V CERM 402

C3120 1UF 10% 6.3V CERM 402

C3121 1UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 31 OF 109	

www.laptopschematics.com

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

=PP0V9_S3M_MEM_DIMMVREFB

C3201 2.2uF 20% 6.3V CERM 603
C3200 0.1uF 20% 10V CERM 402

"Expansion" (surface-mount) slot

=PP1V8_S3M_MEM_B

DDR2-SODIMM-DUAL
CRITICAL
J3200
F-RT-SM-M9

1A	VREF		2A	VSS0			
3A	VSS1		4A	DQ4	MEM_B_DQ<9>	17 85	
5A	DQ0	MEM_B_DQ<15>	6A	DQ5	MEM_B_DQ<11>	17 85	
7A	DQ1	MEM_B_DQ<14>	8A	VSS2			
9A	VSS4		10A	DM0	MEM_B_DM<1>	17 85	
11A	DQS0*	MEM_B_DQS_N<1>	12A	VSS5			
13A	DQS0	MEM_B_DQS_P<1>	14A	DQ6	MEM_B_DQ<12>	17 85	
15A	VSS6		16A	DQ7	MEM_B_DQ<8>	17 85	
17A	DQ2	MEM_B_DQ<10>	18A	VSS7			
19A	DQ3	MEM_B_DQ<13>	20A	DQ12	MEM_B_DQ<3>	17 85	
21A	VSS8		22A	DQ13	MEM_B_DQ<6>	17 85	
23A	DQ8	MEM_B_DQ<7>	24A	VSS9			
25A	DQ9	MEM_B_DQ<2>	26A	DM1	MEM_B_DM<0>	17 85	
27A	VSS10		28A	VSS11			
29A	DQS1*	MEM_B_DQS_N<0>	30A	CK0	MEM_CLK_P<4>	16 85	
31A	DQS1	MEM_B_DQS_P<0>	32A	CK0*	MEM_CLK_N<4>	16 85	
33A	VSS12		34A	VSS13			
35A	DQ10	MEM_B_DQ<1>	36A	DQ14	MEM_B_DQ<0>	17 85	
37A	DQ11	MEM_B_DQ<4>	38A	DQ15	MEM_B_DQ<5>	17 85	
39A	VSS14		40A	VSS15			
KEY							
41A	VSS16		42A	VSS17			
43A	DQ16	MEM_B_DQ<21>	44A	DQ20	MEM_B_DQ<22>	17 85	
45A	DQ17	MEM_B_DQ<19>	46A	DQ21	MEM_B_DQ<18>	17 85	
47A	VSS18		48A	VSS19			
49A	DQS2*	MEM_B_DQS_N<2>	50A	NC0	PM_EXTTS_L<1>	16 45	
51A	DQS2	MEM_B_DQS_P<2>	52A	DM2	MEM_B_DM<2>	17 85	
53A	VSS21		54A	VSS22			
55A	DQ18	MEM_B_DQ<20>	56A	DQ22	MEM_B_DQ<17>	17 85	
57A	DQ19	MEM_B_DQ<23>	58A	DQ23	MEM_B_DQ<16>	17 85	
59A	VSS23		60A	VSS24			
61A	DQ24	MEM_B_DQ<29>	62A	DQ28	MEM_B_DQ<26>	17 85	
63A	DQ25	MEM_B_DQ<24>	64A	DQ29	MEM_B_DQ<28>	17 85	
65A	VSS25		66A	VSS26			
67A	DM3	MEM_B_DM<3>	68A	DQS3*	MEM_B_DQS_N<3>	17 85	
NC 69A	NC1		70A	DQS3	MEM_B_DQS_P<3>	17 85	
71A	VSS27		72A	VSS28			
73A	DQ26	MEM_B_DQ<27>	74A	DQ30	MEM_B_DQ<31>	17 85	
75A	DQ27	MEM_B_DQ<25>	76A	DQ31	MEM_B_DQ<30>	17 85	
77A	VSS29		78A	VSS30			
79A	CKE0	MEM_CKE<3>	80A	NC/CKE1	MEM_CKE<4>	16 33 85	
81A	VDD0		82A	VDD1			
NC 83A	NC2		84A	NC/A15	MEM_B_A<15>	9	
85A	BA2	MEM_B_BS<2>	86A	NC/A14	MEM_B_A<14>	16 33 85	
87A	VDD2		88A	VDD3			
89A	A12	MEM_B_A<12>	90A	A11	MEM_B_A<11>	17 33 85	
91A	A9	MEM_B_A<9>	92A	A7	MEM_B_A<7>	17 33 85	
93A	A8	MEM_B_A<8>	94A	A6	MEM_B_A<6>	17 33 85	
95A	VDD4		96A	VDD5			
97A	A5	MEM_B_A<5>	98A	A4	MEM_B_A<4>	17 33 85	
99A	A3	MEM_B_A<3>	100A	A2	MEM_B_A<2>	17 33 85	
101A	A1	MEM_B_A<1>	102A	A0	MEM_B_A<0>	17 33 85	
103A	VDD6		104A	VDD7			
105A	A10/AP	MEM_B_A<10>	106A	BA1	MEM_B_BS<1>	17 33 85	
107A	BA0	MEM_B_BS<0>	108A	RAS*	MEM_B_RAS_L	17 33 85	
109A	WE*	MEM_B_WE_L	110A	S0*	MEM_CS_L<2>	16 33 85	
111A	VDD8		112A	VDD9			
113A	CAS*	MEM_B_CAS_L	114A	ODT0	MEM_ODT<2>	16 33 85	
115A	NC/S1*	MEM_CS_L<3>	116A	NC/A13	MEM_B_A<13>	17 33 85	
117A	VDD10		118A	VDD11			
119A	NC/ODT1	MEM_ODT<3>	NC 120A	NC3			
121A	VSS31		122A	VSS32			
123A	DQ32	MEM_B_DQ<36>	124A	DQ36	MEM_B_DQ<32>	17 85	
125A	DQ33	MEM_B_DQ<33>	126A	DQ37	MEM_B_DQ<37>	17 85	
127A	VSS33		128A	VSS34			
129A	DQS4*	MEM_B_DQS_N<4>	130A	DM4	MEM_B_DM<4>	17 85	
131A	DQS4	MEM_B_DQS_P<4>	132A	VSS35			
133A	VSS36		134A	DQ38	MEM_B_DQ<38>	17 85	
135A	DQ34	MEM_B_DQ<34>	136A	DQ39	MEM_B_DQ<39>	17 85	
137A	DQ35	MEM_B_DQ<35>	138A	VSS37			
139A	VSS38		140A	DQ44	MEM_B_DQ<56>	17 85	
141A	DQ40	MEM_B_DQ<57>	142A	DQ45	MEM_B_DQ<59>	17 85	
143A	DQ41	MEM_B_DQ<60>	144A	VSS39			
145A	VSS40		146A	DQS5*	MEM_B_DQS_N<7>	17 85	
147A	DM5	MEM_B_DM<7>	148A	DQS5	MEM_B_DQS_P<7>	17 85	
149A	VSS41		150A	VSS42			
151A	DQ42	MEM_B_DQ<61>	152A	DQ46	MEM_B_DQ<63>	17 85	
153A	DQ43	MEM_B_DQ<62>	154A	DQ47	MEM_B_DQ<58>	17 85	
155A	VSS43		156A	VSS44			
157A	DQ48	MEM_B_DQ<48>	158A	DQ52	MEM_B_DQ<54>	17 85	
159A	DQ49	MEM_B_DQ<51>	160A	DQ53	MEM_B_DQ<53>	17 85	
161A	VSS45		162A	VSS46			
NC 163A	NC_TEST		164A	CK1	MEM_CLK_P<3>	16 85	
165A	VSS47		166A	CK1*	MEM_CLK_N<3>	16 85	
167A	DQS6*	MEM_B_DQS_N<6>	168A	VSS48			
169A	DQS6	MEM_B_DQS_P<6>	170A	DM6	MEM_B_DM<6>	17 85	
171A	VSS49		172A	VSS50			
173A	DQ50	MEM_B_DQ<50>	174A	DQ54	MEM_B_DQ<52>	17 85	
175A	DQ51	MEM_B_DQ<55>	176A	DQ55	MEM_B_DQ<49>	17 85	
177A	VSS51		178A	VSS52			
179A	DQ56	MEM_B_DQ<40>	180A	DQ60	MEM_B_DQ<46>	17 85	
181A	DQ57	MEM_B_DQ<47>	182A	DQ61	MEM_B_DQ<43>	17 85	
183A	VSS53		184A	VSS54			
185A	DM7	MEM_B_DM<5>	186A	DQS7*	MEM_B_DQS_N<5>	17 85	
187A	VSS55		188A	DQS7	MEM_B_DQS_P<5>	17 85	
189A	DQ58	MEM_B_DQ<42>	190A	VSS56			
191A	DQ59	MEM_B_DQ<45>	192A	DQ62	MEM_B_DQ<41>	17 85	
193A	VSS57	=PPSPD_S0M_MEM_B	194A	DQ63	MEM_B_DQ<44>	17 85	
195A	SDA	=I2C_SODIMMB_SDA	196A	VSS58			
197A	SCL	=I2C_SODIMMB_SCL	198A	SA0	Resistor prevents pwr-gnd short		
199A	VDDSPD		200A	SA1	SODIMM_B_SA1		

203 201 202 204 516S0471

ADDR=0xA4(WR)/0xA5(RD)

=PPSPD_S0M_MEM_B

R3200 10K 5% 1/16W MF-LF 402

DDR2 Bypass Caps
(For return current)

=PP1V8_S3M_MEM_B

C3208 10UF 20% 6.3V X5R 603
C3209 10UF 20% 6.3V X5R 603
C3210 1UF 10% 6.3V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 1UF 10% 6.3V CERM 402
C3213 1UF 10% 6.3V CERM 402
C3214 1UF 10% 6.3V CERM 402
C3215 1UF 10% 6.3V CERM 402
C3216 1UF 10% 6.3V CERM 402
C3217 0.1UF 20% 10V CERM 402
C3218 0.1UF 20% 10V CERM 402
C3219 0.1UF 20% 10V CERM 402
C3220 0.1UF 20% 10V CERM 402
C3221 0.1UF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

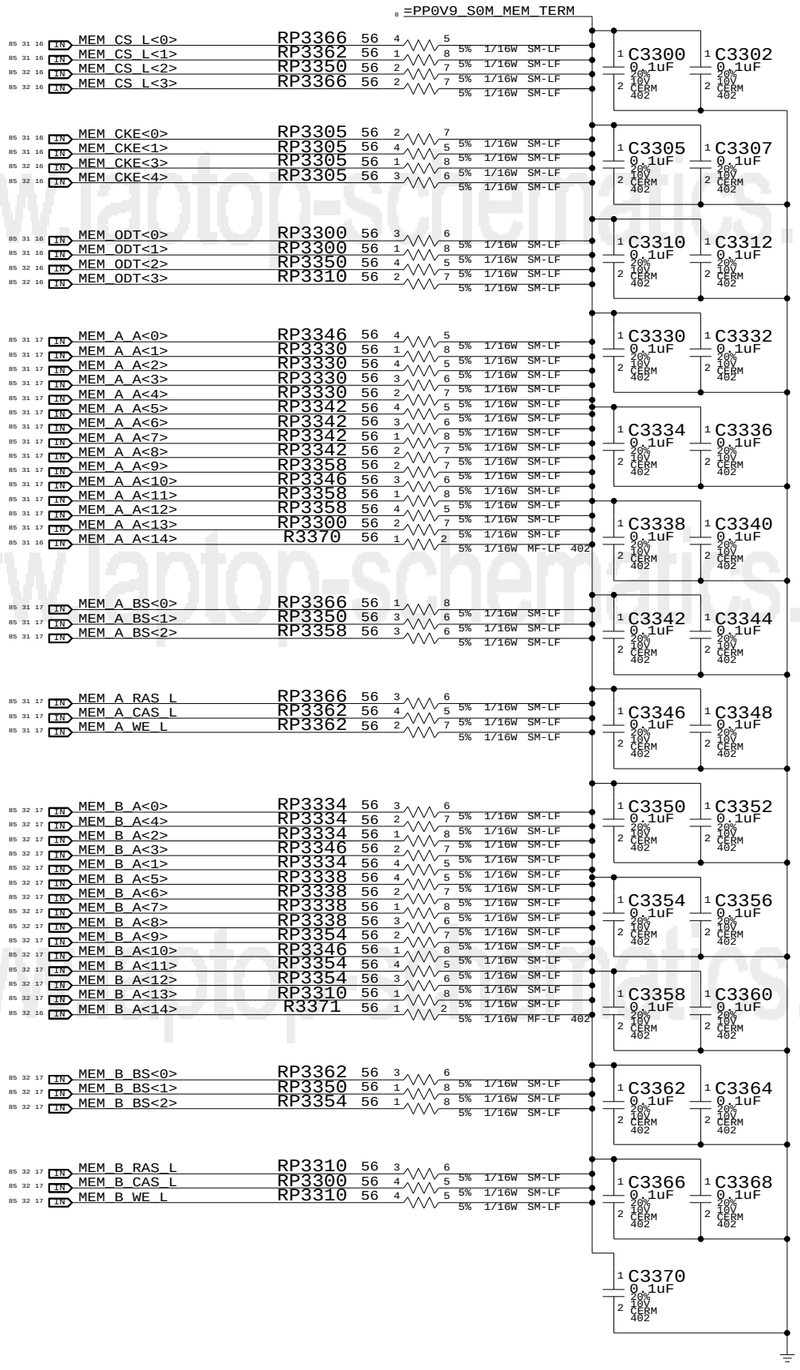
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 32 OF 109	

www.laptopschematics.com

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



www.laptop-schematics.com

Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

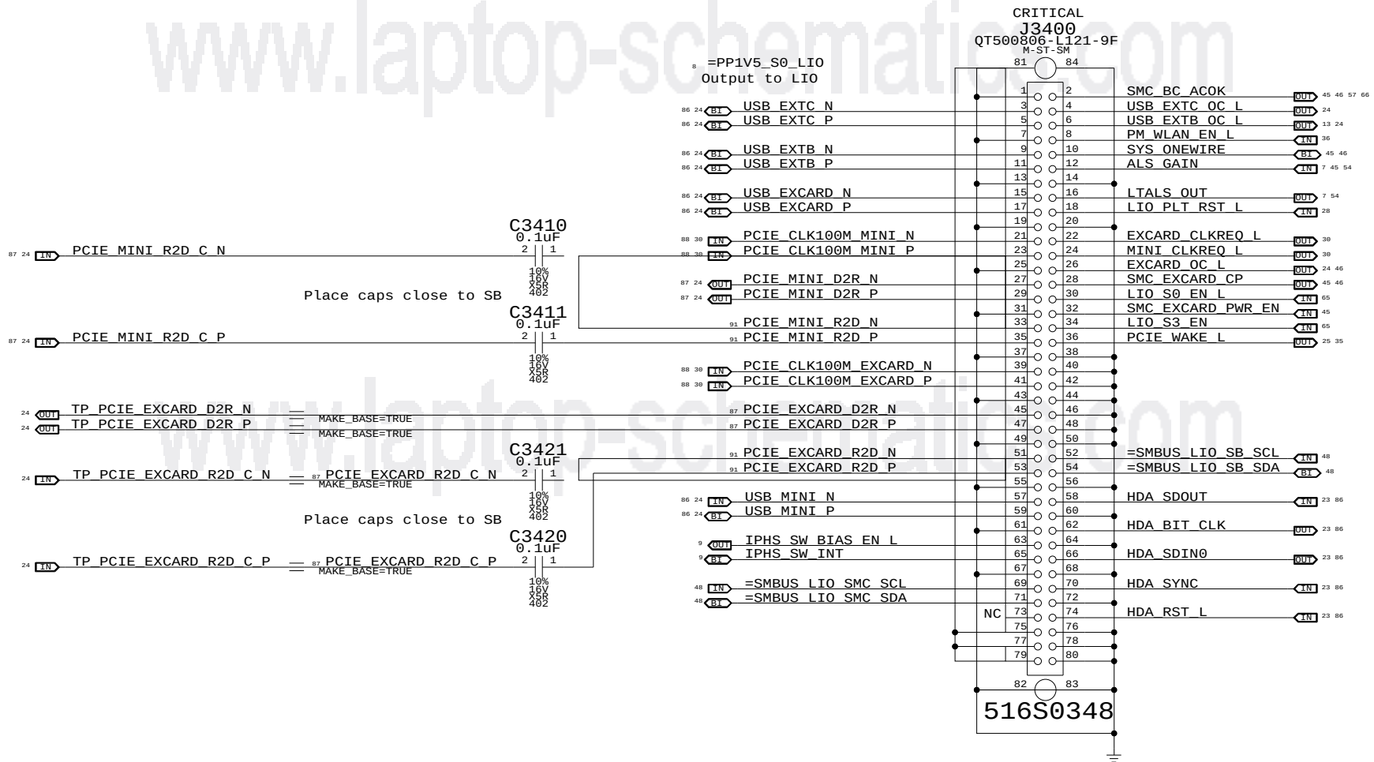
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE	SHT	OF
NONE	33	109

Left I/O Board Connector



www.laptop-schematics.com

Left I/O Board Connector		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	G
	SCALE: NONE	SHT 34 OF 109	

Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

=PP1V2_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	171 mA	No link:	130 mA
10 Mbps:	179 mA	10 Mbps:	130 mA
100 Mbps:	203 mA	100 Mbps:	150 mA
1000 Mbps:	426 mA	1000 Mbps:	290 mA

C3700 4.7UF 20% 6.3V CERM 603; C3701 0.1UF 10% 16V X5R 402; C3702 0.1UF 10% 16V X5R 402; C3703 0.1UF 10% 16V X5R 402; C3704 0.1UF 10% 16V X5R 402; C3705 0.1UF 10% 16V X5R 402; C3706 0.001UF 10% 50V CERM 402; C3707 0.001UF 10% 50V CERM 402; C3708 0.001UF 10% 50V CERM 402

=PP3V3_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	4 mA	No link:	60 mA
10 Mbps:	4 mA	10 Mbps:	70 mA
100 Mbps:	4 mA	100 Mbps:	70 mA
1000 Mbps:	4 mA	1000 Mbps:	80 mA

C3710 4.7UF 20% 6.3V CERM 603; C3711 0.1UF 10% 16V X5R 402; C3712 0.1UF 10% 16V X5R 402; C3713 0.1UF 10% 16V X5R 402; C3714 0.001UF 10% 50V CERM 402; C3715 0.001UF 10% 50V CERM 402

=PP1V8R2V5_ENET_PHY L3720 FERR-120-OHM-1.5A 0402 PP1V8R2V5_ENET_PHY_AVDD
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

Yukon EC (2.5V)		Yukon Ultra (1.8V)	
No link:	82 mA	No link:	0 mA
10 Mbps:	108 mA	10 Mbps:	30 mA
100 Mbps:	126 mA	100 Mbps:	40 mA
1000 Mbps:	218 mA	1000 Mbps:	150 mA

(EC:2.5V)

C3720 4.7UF 20% 6.3V CERM 603; C3721 0.1UF 10% 16V X5R 402; C3722 0.1UF 10% 16V X5R 402; C3723 0.1UF 10% 16V X5R 402; C3724 0.001UF 10% 50V CERM 402

=YUKON_EC_PP2V5_ENET
Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
Yukon Ultra: Alias to GND

PCIE_ENET_D2R_P
PCIE_ENET_D2R_N
PCIE_ENET_R2D_C_P C3730 0.1UF 10% 16V X5R 402
PCIE_ENET_R2D_C_N C3731 0.1UF 10% 16V X5R 402
PLACEMENT_NOTE=Place C3730 close to southbridge.
PLACEMENT_NOTE=Place C3731 close to southbridge.
C3735 0.1UF 10% 16V X5R 402
C3736 0.1UF 10% 16V X5R 402

PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
Yukon EC: Pin 42 should be NC (or TP) net.
=ENET_CLKREQ_L
PCIE_WAKE_L
ENET_RESET_L

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

R3740 R3741 R3742 R3743 R3744 R3745 R3746 R3747 49.9 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY

C3740 C3742 C3744 C3746 0.001UF 10% 50V CERM 402

ENET_CLK25M_XTALI
ENET_CLK25M_XTALO

U3700 88E8058 QFN
CRITICAL
BOMOPTION=OMIT

NC_32	32		
NC_51	51		
NC_52	52		
NC_57	57		
NC_64	64		
AVDD0	19		
AVDD1	22		
AVDD2	23		
AVDD3	28		
		EC:AVDD 2.5V	
VDDO_TTL0	1		
VDDO_TTL1	40		
VDDO_TTL2	45		
VDDO_TTL3	61		
AVDDH	8		
VDD0	2		
VDD1	7		
VDD2	13		
VDD3	33		
VDD4	39		
VDD5	44		
VDD6	48		
VDD7	58		
PCIE_ENET_D2R_C_P	49	TX_P	
PCIE_ENET_D2R_C_N	50	TX_N	
PCIE_ENET_R2D_P	54	RX_P	
PCIE_ENET_R2D_N	53	RX_N	
	55	REFCLKP	
	56	REFCLKN	
	42	CLKREQ*	EC:NO CONNECT
	6	WAKE*	
	5	PERST*	
	17	MDIP0	
	18	MDIN0	
	20	MDIP1	
	21	MDIN1	
	26	MDIP2	
	27	MDIN2	
	30	MDIP3	
	31	MDIN3	
	15	XTALI	
	14	XTALO	
	65	THRML_PAD	

PCI EXPRESS
ANALOG
LED
SPI
MEDIA
TWSI
TEST/RSVD
MAIN CLK

LOM_DISABLE*	10		
VAUX_AVLBL	12		
SWITCH_VAUX	9	NC	
VMAIN_AVLBL	47		
SWITCH_VCC	11	NC	
EC:CTRL25 CTRL18	4		
CTRL12	3		
RSET	16		
LED_ACT*	59	NC	
LED_LINK10/100*	60	NC	
LED_LINK1000*	62	NC	
LED_DUPLEX*	63	NC	
(IPU) SPI_DO	34	NC	
(IPU) SPI_DI	35	NC	
(IPU) SPI_CLK	37	NC	
(IPU) SPI_CS	36	NC	
(IPU) VPD_CLK	38		
(IPU) VPD_DATA	41		
(IPD) TESTMODE	46		
RSVD_24	24	NC	
RSVD_25	25	NC	
RSVD_29	29	NC	
RSVD_43	43	NC	

ENET_LOM_DIS_L
Must be high in S0 state (can use PP3V3_S0 as input)
=ENET_VMAIN_AVLBL
TP_YUKON_CTRL18
TP_YUKON_CTRL12
YUKON_RSET
YUKON_VPD_CLK
YUKON_VPD_DATA

R3760 4.7K 5% 1/10W MF-LF 402
YUKON_ULTRA
R3765 4.99K 1% 1/16W MF-LF 402

VPD ROM
C3780 0.1UF 10% 16V X5R 402
R3780 4.7K 5% 1/10W MF-LF 402
R3781 4.7K 5% 1/16W MF-LF 402
U3780 M24C08 SO8
CRITICAL

VCC	8		
E2	3		
NC1	2	NC	
NC0	1	NC	
SDA	5		
SCL	6		
WC*	7		
VSS	4		

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONs to select stuffed part

www.laptop-schematics.com

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

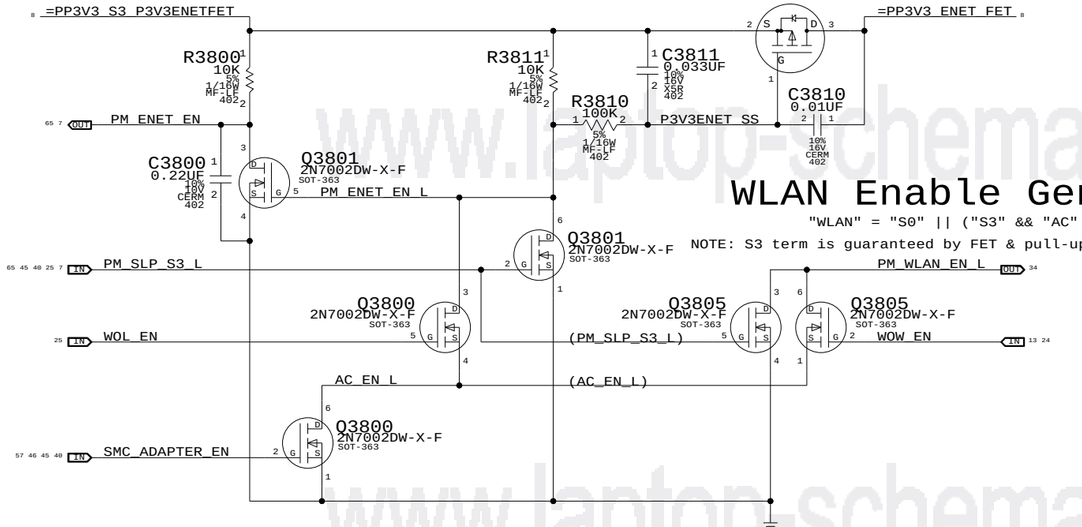
SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 37 OF 109	

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

3.3V ENET FET



WLAN Enable Generation

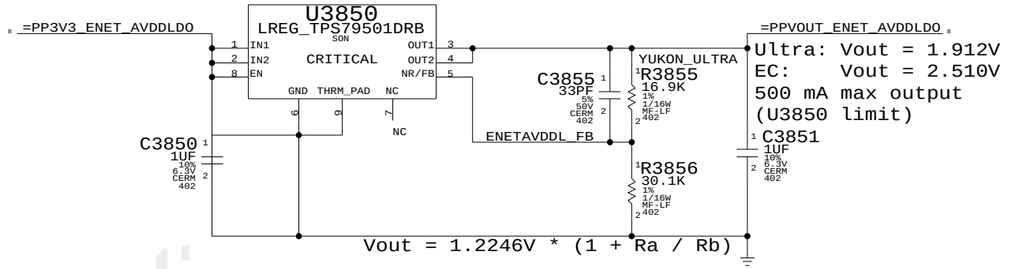
"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")

NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

Yukon AVDDL LDO

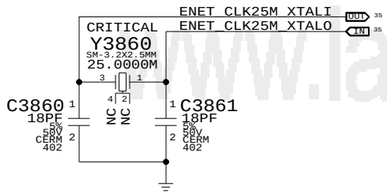
1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 38 OF 109	

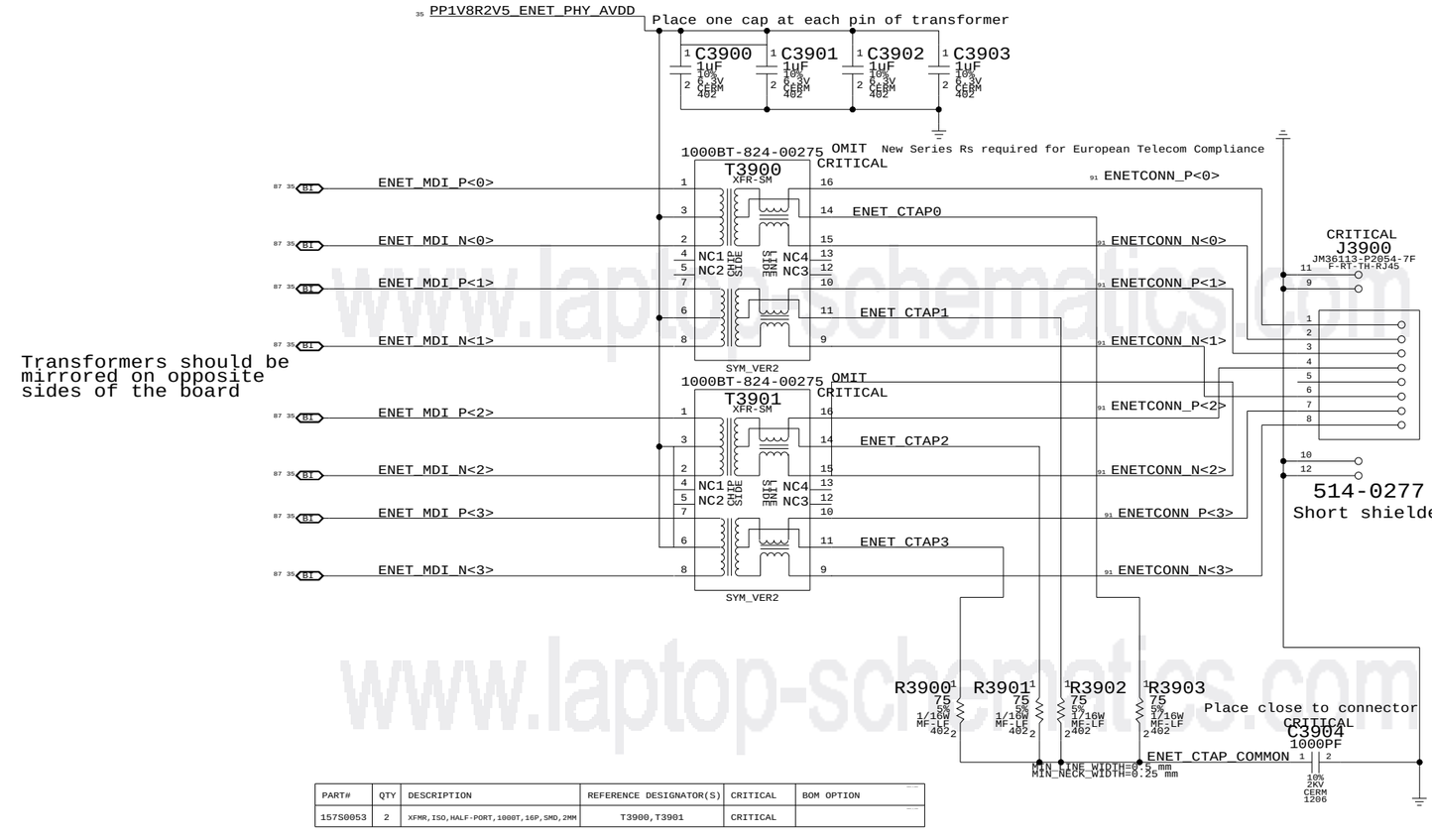
www.laptop-schematics.com

Page Notes

Power aliases required by this page:
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Transformers should be mirrored on opposite sides of the board

New Series Rs required for European Telecom Compliance

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
157S0053	2	XFMR,ISO,HALF-PORT,1000T,16P,SMD,2MM	T3900,T3901	CRITICAL	

www.laptop-schematics.com

Ethernet Connector

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

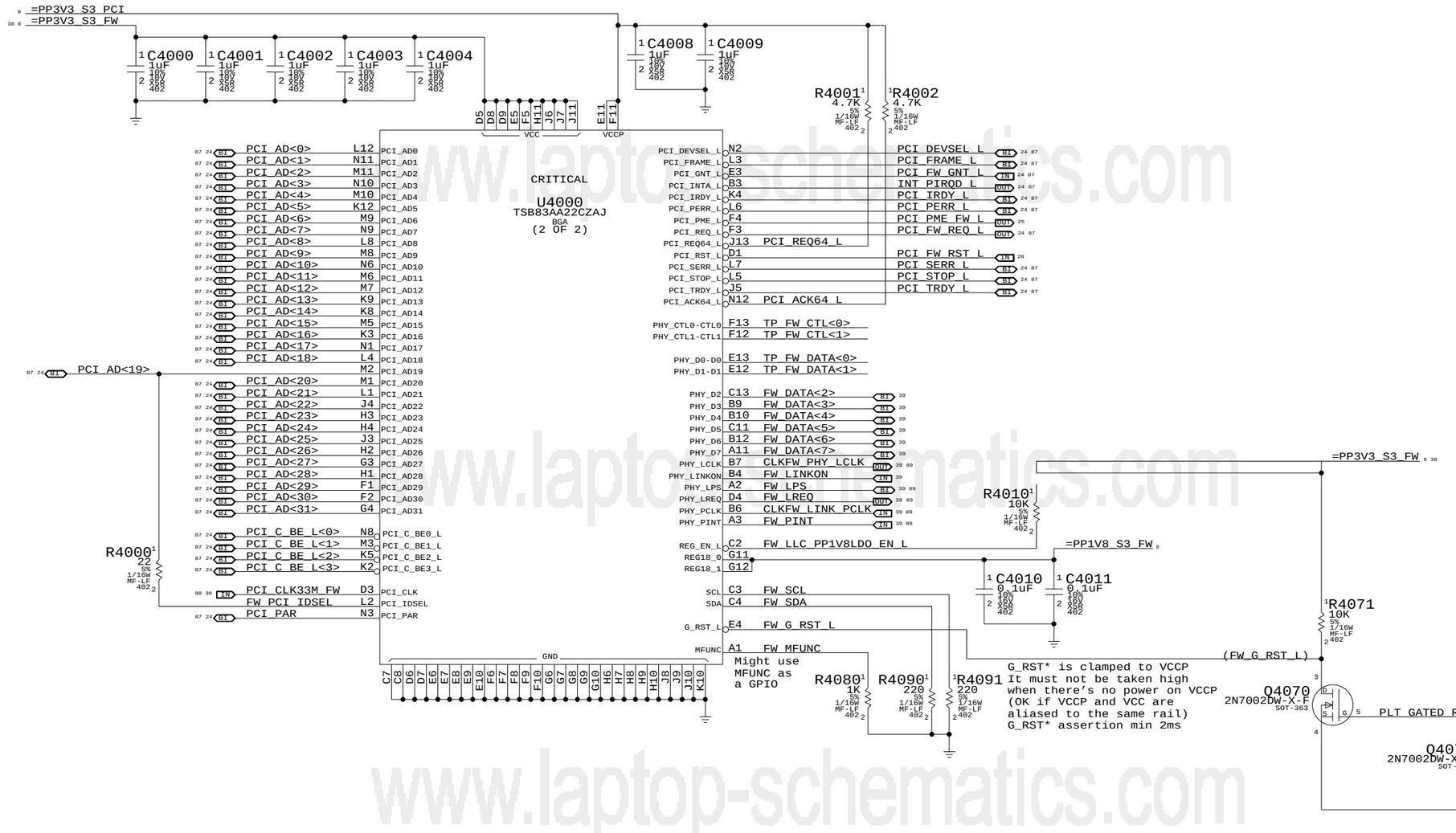
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 39 OF 109	



www.laptop-schematics.com

FireWire Link (TSB83AA22)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

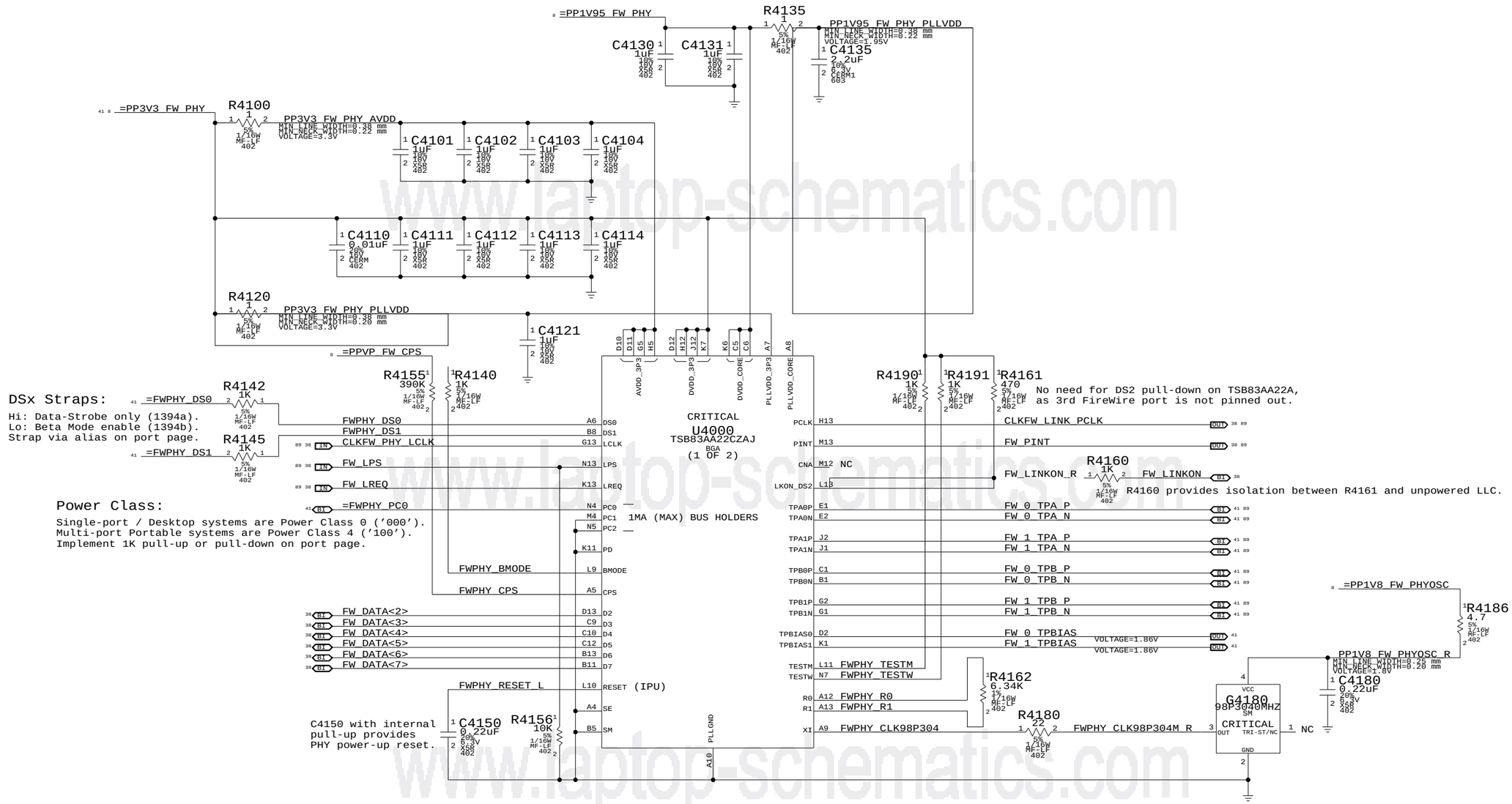
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 40 OF 109	



www.laptop-schematics.com

FireWire PHY (TSB83AA22)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 41 OF 109	

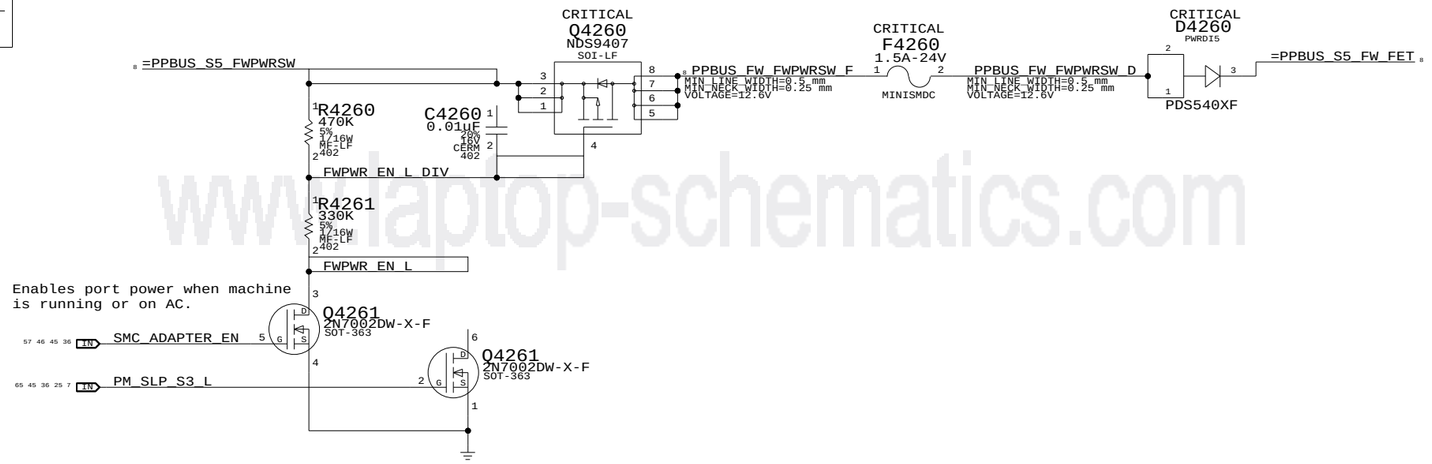
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

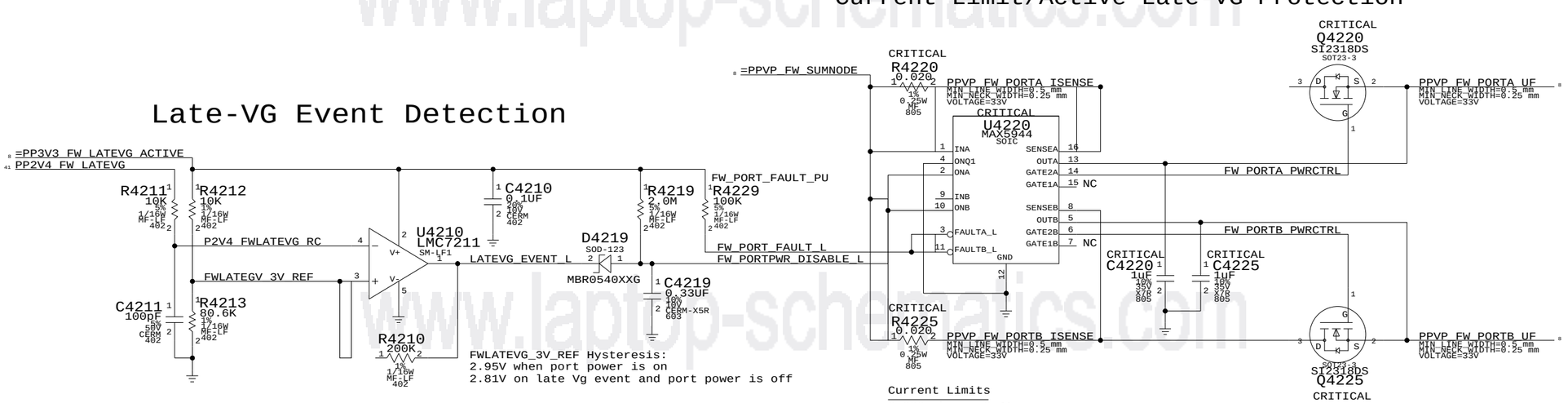
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Current Limit/Active Late-VG Protection



Late-VG Event Detection

Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 42 OF 109	

www.laptop-schematics.com

Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT0
- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG
- =GND_CHASSIS_FW_PORT0L
- =GND_CHASSIS_FW_PORT0U
- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:
- 2-port Portable Power Class (4)
- Port "0" Data-Strobe only (1394A)
- Port "1" Bilingual (1394B)

39 8 =PP3V3_FW_PHY
39 =FWPHY_PC0
39 =FWPHY_DS0
39 =FWPHY_DS1

Termination

Place close to FireWire PHY

TI PHYs require 1uF even though FW spec calls out 0.33uF

39 FW_1_TPBIAS
39 FW_0_TPBIAS
C4350 1uF 10% 6.3V CERM 402
C4360 1uF 10% 6.3V CERM 402
CRITICAL L4360 18NH-250MA 0402
CRITICAL L4361 18NH-250MA 0402
FW_B_TPA_L_P
FW_B_TPA_L_N
R4350 56.2 1% 1/16W MF-LF 402
R4351 56.2 1% 1/16W MF-LF 402
R4360 56.2 1% 1/16W MF-LF 402
R4361 56.2 1% 1/16W MF-LF 402
89 39 FW_0_TPA_P — FW_PORT0_TPA_P 41 MAKE_BASE=TRUE
89 39 FW_0_TPA_N — FW_PORT0_TPA_N 41 MAKE_BASE=TRUE
89 39 FW_0_TPB_P — FW_PORT0_TPB_P 41 MAKE_BASE=TRUE
89 39 FW_0_TPB_N — FW_PORT0_TPB_N 41 MAKE_BASE=TRUE
89 39 FW_1_TPA_P — FW_PORT1_TPA_P 41 MAKE_BASE=TRUE
89 39 FW_1_TPA_N — FW_PORT1_TPA_N 41 MAKE_BASE=TRUE
89 39 FW_1_TPB_P — FW_PORT1_TPB_P 41 MAKE_BASE=TRUE
89 39 FW_1_TPB_N — FW_PORT1_TPB_N 41 MAKE_BASE=TRUE
SIGNAL_MODEL=EMPTY
R4352 56.2 1% 1/16W MF-LF 402
R4353 56.2 1% 1/16W MF-LF 402
R4362 56.2 1% 1/16W MF-LF 402
R4363 56.2 1% 1/16W MF-LF 402
FW_B_TPB_L_N
FW_B_TPB_L_P
CRITICAL L4362 18NH-250MA 0402
CRITICAL L4363 18NH-250MA 0402
SIGNAL_MODEL=EMPTY
SIGNAL_MODEL=EMPTY
FW_PORT0_TPB_C
FW_PORT1_TPB_C
C4354 220pF 5% 25V CERM 402
R4354 4.99K 1% 1/16W MF-LF 402
C4364 220pF 5% 25V CERM 402
R4364 4.99K 1% 1/16W MF-LF 402

Late-VG Protection Power

8 =PP3V3_FW_LATEVG
R4390 332 1% 1/16W MF-LF 402
PP2V4_FW_LATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V 40 41
CRITICAL D4390 MMBZ5227B SOT23

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

ESD and late-VG rail for snap-back diodes (Common to all ports)

Cable Power

"Snapback" & "Late VG" Protection

8 =PPVP_FW_PORT0
CRITICAL L4300 FERR-250-OHM SM
PPVP_FW_PORT0 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V
Note: Trace PPVP_FW_PORT0 must handle up to 5A
C4304 0.01UF 10% 50V X7R 402
41 40 PP2V4_FW_LATEVG
DP4300 BAV99DW-X-F SOT-363
C4300 0.01uF 10% 50V X7R 402
C4301 0.01uF 10% 50V X7R 402
41 FW_PORT0_TPA_P
41 FW_PORT0_TPA_N
41 FW_PORT0_TPB_P
41 FW_PORT0_TPB_N
CRITICAL FL4300 90-OHM-100MA 1210-4SM1
CRITICAL FL4301 90-OHM-100MA 1210-4SM1
91 FW_PORT0_TPA_FL_P
91 FW_PORT0_TPA_FL_N
91 FW_PORT0_TPB_FL_P
91 FW_PORT0_TPB_FL_N
DP4301 BAV99DW-X-F SOT-363
C4302 0.01uF 10% 50V X7R 402
C4303 0.01uF 10% 50V X7R 402
(GND_FW_PORT0_VG)

PORT 0
1394A
CRITICAL J4300 1394A F-RT-TH-LF
TPO (TPA+)
TPO# (TPA-)
TPI (TPB+)
TPI# (TPB-)
VP
VGND
514-0255

Cable Power

"Snapback" & "Late VG" Protection

8 =PPVP_FW_PORT1
CRITICAL L4310 FERR-250-OHM SM
PPVP_FW_PORT1 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V
Note: Trace PPVP_FW_PORT1 must handle up to 5A
C4314 0.01UF 10% 50V X7R 402
41 40 PP2V4_FW_LATEVG
DP4310 BAV99DW-X-F SOT-363
C4311 0.01uF 10% 50V X7R 402
C4310 0.01uF 10% 50V X7R 402
41 FW_PORT1_TPB_N
41 FW_PORT1_TPB_P
41 FW_PORT1_TPA_N
41 FW_PORT1_TPA_P
DP4311 BAV99DW-X-F SOT-363
C4312 0.01uF 10% 50V X7R 402
C4313 0.01uF 10% 50V X7R 402
C4319 0.1uF 10% 50V X7R 603-1
R4319 1M 5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place C4319 close to connector pin 5.

PORT 1
BILINGUAL
CRITICAL J4310 1394B-UG31903 F-RT-SM1
(FW_PORT1_BREF)
(GND_FW_PORT1_VG)
FW_PORT1_AREF
TPB- / TPB<R> / TPB+ / VP / NC / VG / TPA- / TPA<R> / TPA+ — OUTPUT / INPUT
514S0133

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

FireWire Ports

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 43 OF 109	

www.laptop-schematics.com

IDE (ODD) Connector

=PP3V3_S0_IDE

CRITICAL
Q4420
FDC606P
SOT-6

PP5V_ODD
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=5V

=PP5V_S0_ODD

R4420 10K 5% 1/16W MF-LF 402

C4422 0.068UF 10% 10V CERM 402

R4421 47K 5% 1/16W MF-LF 402

C4421 0.01UF 10% 16V CERM 402

R4402 4.7K 5% 1/16W MF-LF 402

=PP5V_S0_ODDPWREN

R4422 100K 5% 1/16W MF-LF 402

P5VODD_SS

P5VODD_EN_L

ODD_PWR_EN

Q4421
2N7002DW-X-F
SOT-363

Q4421
2N7002DW-X-F
SOT-363

24 IN ODD_PWR_EN_L

(SB has internal 5.7k-23.5k pull-down)
(UATA_HSTROBE)
(UATA_DSTROBE)

(UATA_CS0*)

(ODD has internal 10K pull-up to 5V)

CRITICAL
J4400
M-ST-SMI-LF
516S0335

42 IN	ODD_RST_BUF_L				
86 23 BI	IDE_PDD<7>	1	50	IDE_PDD<8>	BI 23 86
86 23 BI	IDE_PDD<6>	2	49	IDE_PDD<9>	BI 23 86
86 23 BI	IDE_PDD<5>	3	48	IDE_PDD<10>	BI 23 86
86 23 BI	IDE_PDD<4>	4	47	IDE_PDD<11>	BI 23 86
		5	46	IDE_PDD<12>	BI 23 86
86 23 BI	IDE_PDD<3>	6	45	IDE_PDD<13>	BI 23 86
86 23 BI	IDE_PDD<2>	7	44	IDE_PDD<14>	BI 23 86
86 23 BI	IDE_PDD<1>	8	43	IDE_PDD<15>	BI 23 86
86 23 BI	IDE_PDD<0>	9	42	IDE_PDIOW_L	IN 23 86 (UATA_STOP)
86 23 OUT	IDE_PDDREQ	10	41	IDE_PDDACK_L	IN 23 86
86 23 IN	IDE_PDIOR_L	11	40	IDE_IRQ14	OUT 23 86
86 23 OUT	IDE_PDIORDY	12	39	IDE_PDA<1>	IN 23 86
		13	38	IDE_PDA<0>	IN 23 86
86 23 IN	IDE_PDA<2>	14	37	IDE_PDCS3_L	IN 23 86 (UATA_CS1*)
86 23 IN	IDE_PDCS1_L	15	36		
		16	35		
		17	34		
		18	33		
		19	32		
		20	31		
		21	30	Indicates disk presence	
		NC 22	29	SMC_ODD_DETECT	OUT 45
		23	28		
		24	27		
		25	26		

R4410 33K 5% 1/16W MF-LF 402

R4403 6.2K 5% 1/16W MF-LF 402

=PP5V_S0_PCIREQFIX

R4430 100K 5% 1/16W MF-LF 402

U4430 MC74VHC1G09 SC70

86 24 IN ODD_RST_5VTOL_L

ODD_RST_BUF_L 42

Unused SATA Ports

86 23 IN	SATA_B_R2D_C_P	TP_SATA_B_R2DP MAKE_BASE=TRUE
86 23 IN	SATA_B_R2D_C_N	TP_SATA_B_R2DN MAKE_BASE=TRUE
86 23 OUT	SATA_B_D2R_P	TP_SATA_B_D2RP MAKE_BASE=TRUE
86 23 OUT	SATA_B_D2R_N	TP_SATA_B_D2RN MAKE_BASE=TRUE
86 23 IN	SATA_C_R2D_C_P	TP_SATA_C_R2DP MAKE_BASE=TRUE
86 23 IN	SATA_C_R2D_C_N	TP_SATA_C_R2DN MAKE_BASE=TRUE
86 23 OUT	SATA_C_D2R_P	TP_SATA_C_D2RP MAKE_BASE=TRUE
86 23 OUT	SATA_C_D2R_N	TP_SATA_C_D2RN MAKE_BASE=TRUE

25 BI SATA_RBIAS_P
25 BI SATA_RBIAS_N
SATA_RBIAS MAKE_BASE=TRUE

R4460 24.9 1% 1/16W MF-LF 402

Placement note
Place within 12.7mm from ball of SB

www.laptop-schematics.com

PATA Connector

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

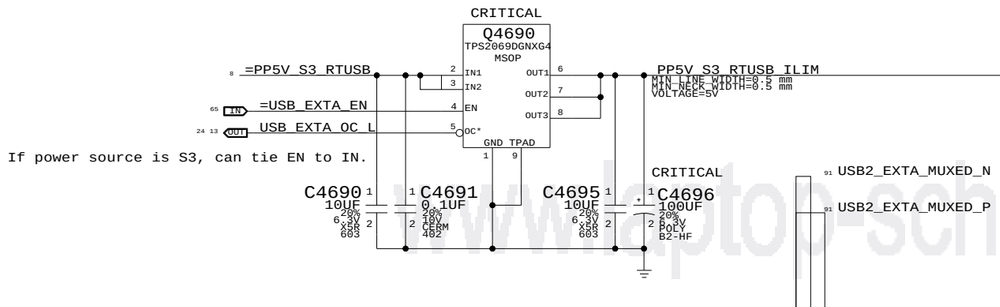
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

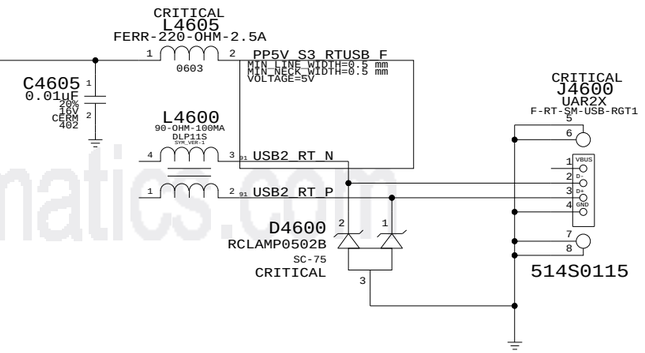
SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 44 OF 109	

www.laptop-schematics.com

Port Power Switch

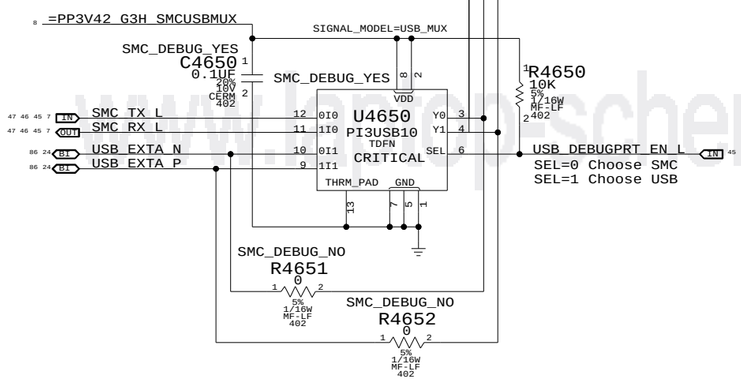


Right USB Port



Place L4600 and L4605 at connector pin

USB/SMC Debug Mux



External USB Connector

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

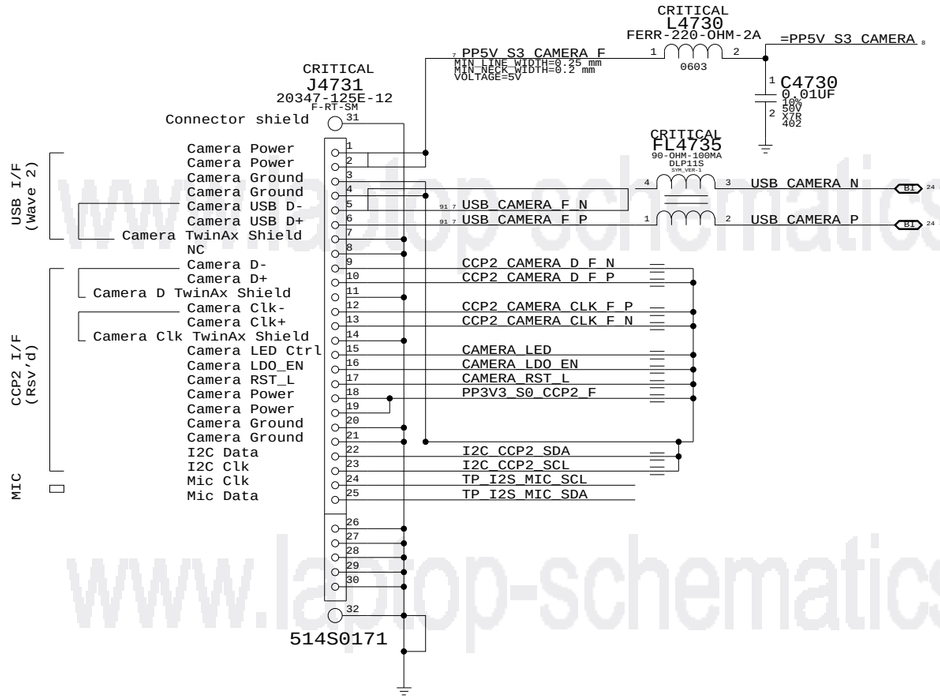
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 46 OF 109	

Left Clutch Barrel Interconnect



www.laptop-schematics.com

www.laptop-schematics.com

www.laptop-schematics.com

Left Clutch Barrel Interconnect

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

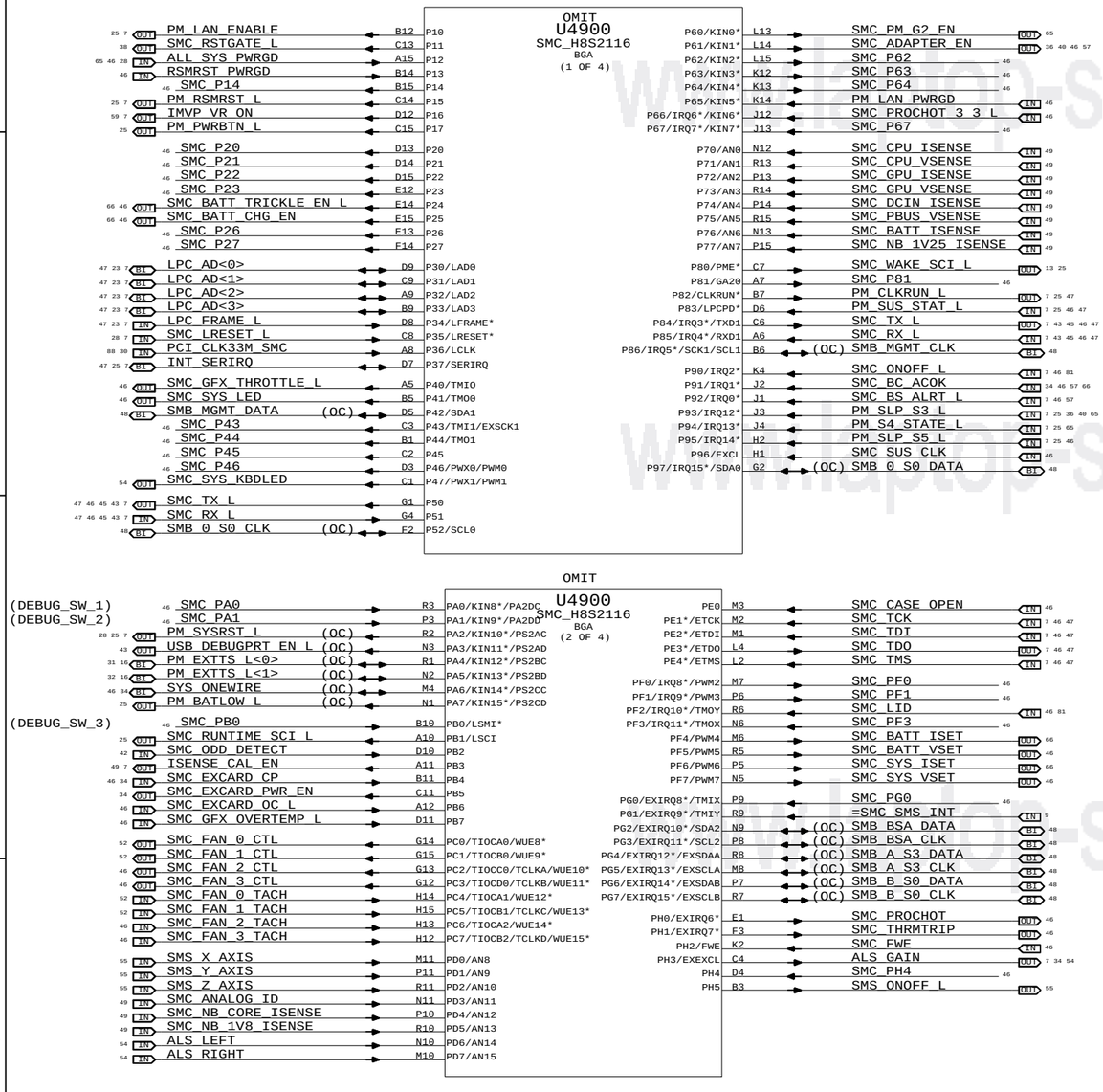
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

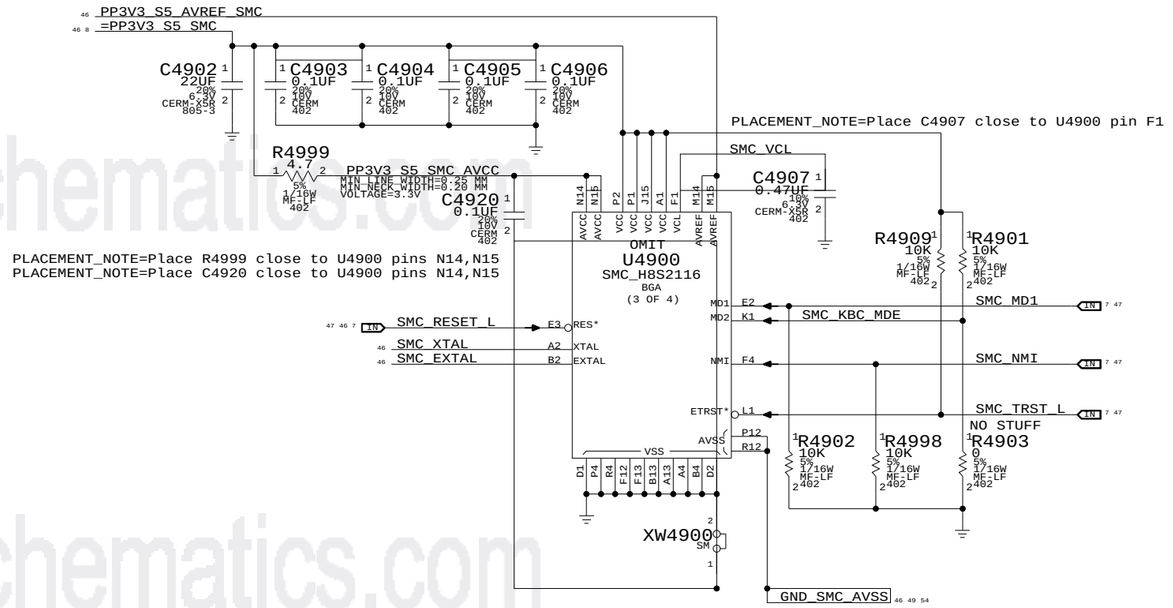
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

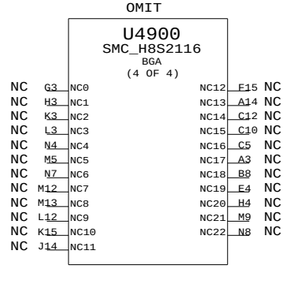
SCALE	SHT	OF
NONE	47	109

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SMC

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

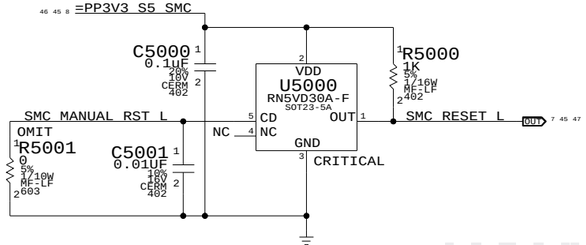
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 49 OF 109	

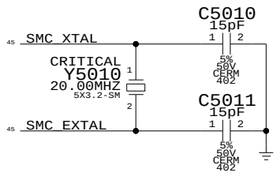
www.laptop-schematics.com

www.laptop-schematics.com

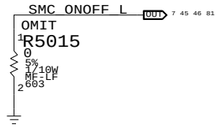
SMC Reset "Button" / Brownout Detect



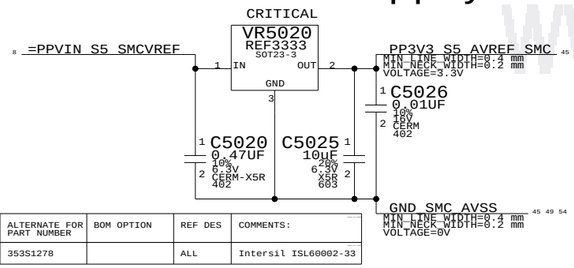
SMC Crystal Circuit



Debug Power "Button"

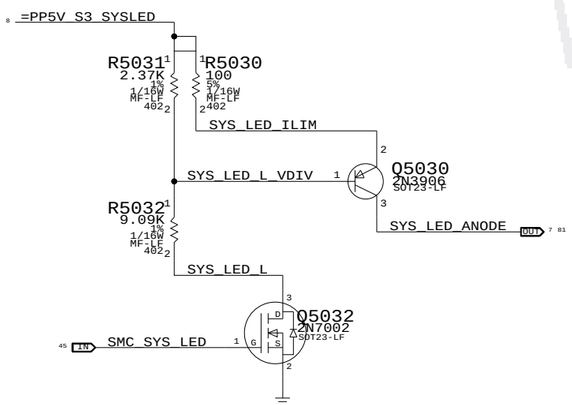


SMC AVREF Supply

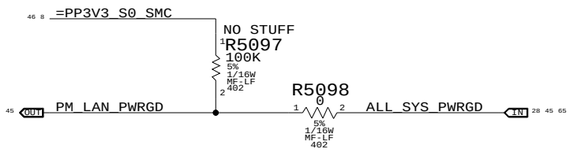


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

System (Sleep) LED Circuit

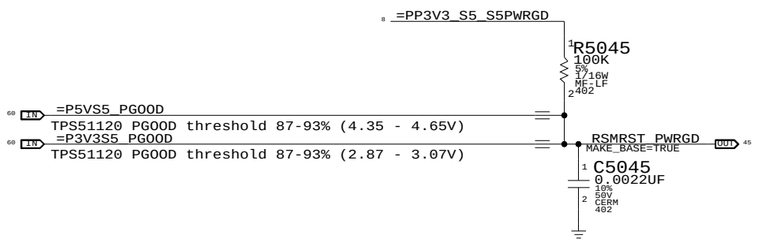


LAN PWRGD Circuit

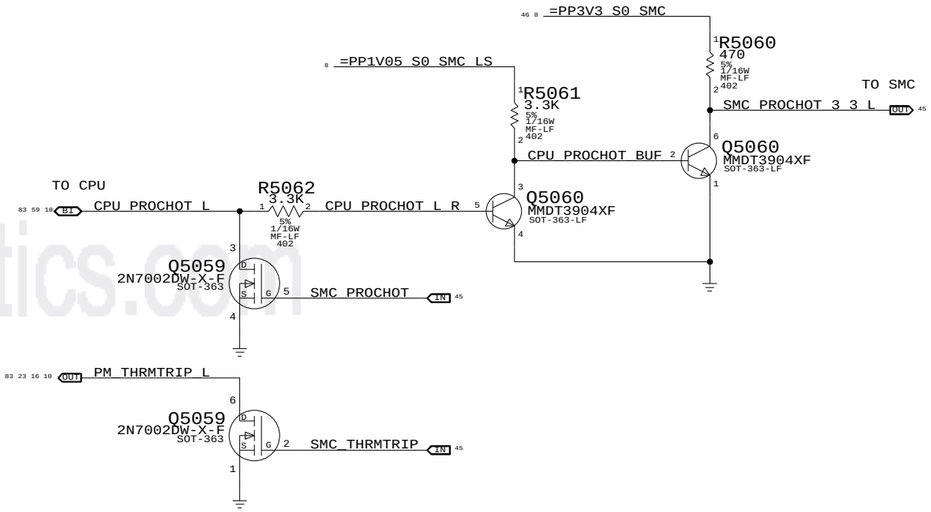


S5 Rail PWRGD Circuit

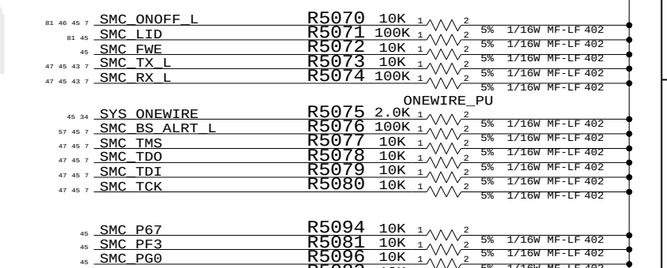
Reports when 5V S5 and 3.3V S5 are in regulation



SMC FSB to 3.3V Level Shifting



SMC Support



SMC FAN / SMC GFX / SMC BATT / SMC SYS / SMC P14–P64 / SMC P81–PF1

SMC_FAN_2_CTL	TP_SMC_FAN_2_CTL	MAKE_BASE=TRUE
SMC_FAN_2_TACH	TP_SMC_FAN_2_TACH	MAKE_BASE=TRUE
SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL	MAKE_BASE=TRUE
SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH	MAKE_BASE=TRUE
SMC_GFX_OVERTEMP_L	TP_SMC_GFX_OVERTEMP_L	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_L	TP_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE
SMC_BATT_VSET	TP_SMC_BATT_VSET	MAKE_BASE=TRUE
SMC_SYS_VSET	TP_SMC_SYS_VSET	MAKE_BASE=TRUE
SMC_P14	TP_SMC_P14	MAKE_BASE=TRUE
SMC_P20	TP_SMC_P20	MAKE_BASE=TRUE
SMC_P21	TP_SMC_P21	MAKE_BASE=TRUE
SMC_P22	TP_SMC_P22	MAKE_BASE=TRUE
SMC_P23	TP_SMC_P23	MAKE_BASE=TRUE
SMC_P26	TP_SMC_P26	MAKE_BASE=TRUE
SMC_P27	TP_SMC_P27	MAKE_BASE=TRUE
SMC_P43	TP_SMC_P43	MAKE_BASE=TRUE
SMC_P44	TP_SMC_P44	MAKE_BASE=TRUE
SMC_P46	TP_SMC_P46	MAKE_BASE=TRUE
SMC_P62	TP_SMC_P62	MAKE_BASE=TRUE
SMC_P63	TP_SMC_P63	MAKE_BASE=TRUE
SMC_P64	TP_SMC_P64	MAKE_BASE=TRUE
SMC_P81	TP_SMC_P81	MAKE_BASE=TRUE
SMC_PF0	TP_SMC_PF0	MAKE_BASE=TRUE
SMC_PF1	TP_SMC_PF1	MAKE_BASE=TRUE

SMC EXCARD / SMC SUS / SMC P45

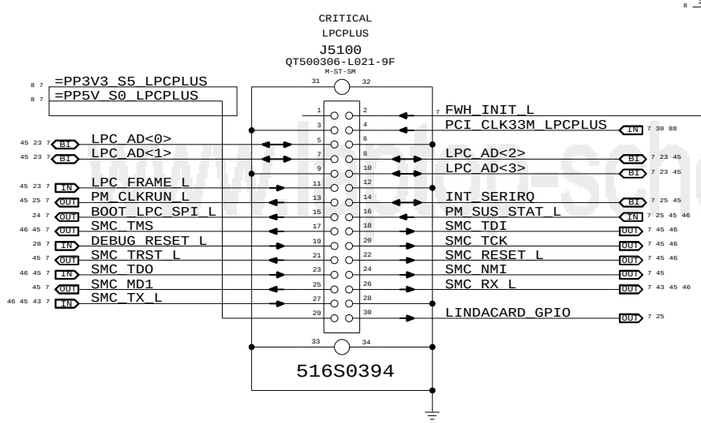
SMC_EXCARD_OC_L	R5095 0 5% 1/16W MF-LF 402	EXCARD_OC_L
SMC_SUS_CLK	SUS_CLK_SB	MAKE_BASE=TRUE
SMC_P45	SMC_ENRGYSTR_LDO_EN	MAKE_BASE=TRUE

SMC_XDP_TDO	TP_SMC_XDP_TDO
SMC_XDP_TDI	TP_SMC_XDP_TDI
SMC_XDP_TMS	TP_SMC_XDP_TMS
SMC_XDP_TCK	TP_SMC_XDP_TCK
SMC_XDP_TRST_L	TP_SMC_XDP_TRST_L

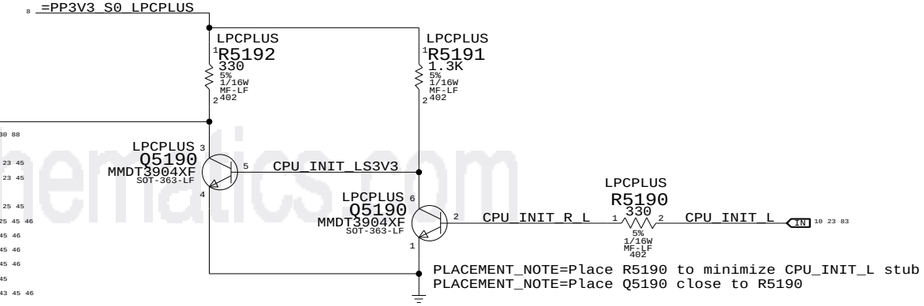
SMC_PECI	TP_SMC_PECI
SMC_RUNTIME_SCI_L	TP_SMC_RUNTIME_SCI_L
SMC_WAKE_SCI_L	TP_SMC_WAKE_SCI_L
SMC_PWRFLR_L	TP_SMC_PWRFLR_L
SMC_RCIN_L	TP_SMC_RCIN_L
SMC_A20GATE	TP_SMC_A20GATE
SMC_RESET_L	TP_SMC_RESET_L
SMC_PME_S4_WAKE_L	TP_SMC_PME_S4_WAKE_L
SMC_LRESET_L	TP_SMC_LRESET_L
SMC_SPI_CS_L	TP_SMC_SPI_CS_L
SMC_SPI_CLK	TP_SMC_SPI_CLK
SMC_SPI_MOSI	TP_SMC_SPI_MOSI
SMC_SPI_MISO	TP_SMC_SPI_MISO
SMC_LPCPD_L	TP_SMC_LPCPD_L
SMC_LPCRESET_L	TP_SMC_LPCRESET_L
SMC_LDRQ1_L	TP_SMC_LDRQ1_L
SMC_SERIRQ	TP_SMC_SERIRQ
SMC_LFRAME_L	TP_SMC_LFRAME_L
SMC_LAD0	TP_SMC_LAD0
SMC_LAD1	TP_SMC_LAD1
SMC_LAD2	TP_SMC_LAD2
SMC_LAD3	TP_SMC_LAD3
SMC_CLKRUN_L	TP_SMC_CLKRUN_L
SMC_PCIRST_L	TP_SMC_PCIRST_L
SMC_PCIRST_BUF_L	TP_SMC_PCIRST_BUF_L
SMC_PCIRST_BUF2_L	TP_SMC_PCIRST_BUF2_L
SMC_PCIRST_BUF3_L	TP_SMC_PCIRST_BUF3_L
SMC_PCIRST_BUF4_L	TP_SMC_PCIRST_BUF4_L
SMC_PCIRST_BUF5_L	TP_SMC_PCIRST_BUF5_L
SMC_PCIRST_BUF6_L	TP_SMC_PCIRST_BUF6_L
SMC_PCIRST_BUF7_L	TP_SMC_PCIRST_BUF7_L
SMC_PCIRST_BUF8_L	TP_SMC_PCIRST_BUF8_L
SMC_PCIRST_BUF9_L	TP_SMC_PCIRST_BUF9_L

www.laptop-schematics.com

LPC+ Connector



FWH_INIT_L Generation



www.laptop-schematics.com

LPC+ Debug Connector

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE	SHT	OF
NONE	51	109

ICH8-M SMBus Connections

=PP3V3_S0_SMBUS_SB

ICH8-M
U2300
(MASTER)

- SMB_CLK
- SMB_DATA
- SMBUS_SB_SCL (MAKE_BASE=TRUE)
- SMBUS_SB_SDA (MAKE_BASE=TRUE)

R5200 4.7K 5% 1/16W MF-LF 402
R5201 4.7K 5% 1/16W MF-LF 402

Clock Chip
CY28545-5: U2900
(Write: 0xD2 Read: 0xD3)

- =SMBUS_CK505_SCL
- =SMBUS_CK505_SDA

SO-DIMM "A"
J3100
(Write: 0xA0 Read: 0xA1)

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

SO-DIMM "B"
J3200
(Write: 0xA4 Read: 0xA5)

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

Left I/O SMBus Connections:
ExpressCard Slot
(Address determined by ARP)

Left I/O
J3400
(See Table)

- =SMBUS_LIO_SB_SCL
- =SMBUS_LIO_SB_SDA

ICH8-M ME SMBus Connections

=PP3V3_S5_SMBUS_SB_ME

ICH8-M
U2300
(MASTER?)

- SMB_ME_CLK
- SMB_ME_DATA
- SMBUS_SB_ME_SCL (MAKE_BASE=TRUE)
- SMBUS_SB_ME_SDA (MAKE_BASE=TRUE)

R5230 10K 5% 1/16W MF-LF 402
R5231 10K 5% 1/16W MF-LF 402

SMC "0" SMBus Connections

=PP3V3_GPU_SMBUS_SMC_0_S0

SMC
U4900
(MASTER)

- SMB_0_S0_CLK
- SMB_0_S0_DATA
- SMBUS_SMC_0_S0_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_0_S0_SDA (MAKE_BASE=TRUE)

R5250 4.7K 5% 1/16W MF-LF 402
R5251 4.7K 5% 1/16W MF-LF 402

GPU Temp (Ext)
TMP401: U5550
(Write: 0x98 Read: 0x99)

- =SMBUS_GPUTHMSNS_SCL
- =SMBUS_GPUTHMSNS_SDA

GPU Temp (Int)
G84M: U8000
(Write: 0x9E Read: 0x9F)

- =GPU_I2CS_SCL
- =GPU_I2CS_SDA

SMC "Battery A" SMBus Connections

=PP3V42_G3H_SMBUS_SMC_BSA

SMC
U4900
(MASTER)

- SMB_BSA_CLK
- SMB_BSA_DATA
- SMBUS_SMC_BSA_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_BSA_SDA (MAKE_BASE=TRUE)

R5280 4.7K 5% 1/16W MF-LF 402
R5281 4.7K 5% 1/16W MF-LF 402

Battery
J6950
(Write: 0x16 Read: 0x17)

- =SMBUS_BATT_SCL
- =SMBUS_BATT_SDA

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

=PP3V3_S3_SMBUS_SMC_MGMT

SMC
U4900
(MASTER)

- SMB_MGMT_CLK
- SMB_MGMT_DATA
- SMBUS_SMC_MGMT_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_MGMT_SDA (MAKE_BASE=TRUE)

R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402

SMS
U5900
(Write: 0x30 Read: 0x31)

- =I2C_SMS_SCL
- =I2C_SMS_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_A_S3

SMC
U4900
(MASTER)

- SMB_A_S3_CLK
- SMB_A_S3_DATA
- SMBUS_SMC_A_S3_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_A_S3_SDA (MAKE_BASE=TRUE)

R5270 3.3K 5% 1/16W MF-LF 402
R5271 3.3K 5% 1/16W MF-LF 402

Top-Case
J9600
TMP275
(Write: 0x9E Read: 0x9F)

- =I2C_TOPCASE_SCL
- =I2C_TOPCASE_SDA

Left I/O SMBus Connections:
Left ALS - TMP102
(Write: 0x92 Read: 0x93)
M35C - TMP106
(Write: 0x90 Read: 0x91)

Left I/O Board
J3400
(See Table)

- =SMBUS_LIO_SMC_SCL
- =SMBUS_LIO_SMC_SDA

Remote Temps
EMC1043-1: U5500
(Write: 0x98 Read: 0x99)

- =SMBUS_REMTHMSNS_SCL
- =SMBUS_REMTHMSNS_SDA

SMC "B" SMBus Connections

=PP3V3_S0_SMBUS_SMC_B_S0

SMC
U4900
(MASTER)

- SMB_B_S0_CLK
- SMB_B_S0_DATA
- SMBUS_SMC_B_S0_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_B_S0_SDA (MAKE_BASE=TRUE)

R5260 3.3K 5% 1/16W MF-LF 402
R5261 3.3K 5% 1/16W MF-LF 402

CPU Temp
EMC1043-1: U5570
(Write: 0x98 Read: 0x99)

- =I2C_CPUTHMSNS_SCL
- =I2C_CPUTHMSNS_SDA

Battery Charger
TMP102:U5750
(Write: 0x92 Read: 0x93)

- =SMBUS_TMPSNSR_SCL
- =SMBUS_TMPSNSR_SDA

www.laptop-schematics.com

SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

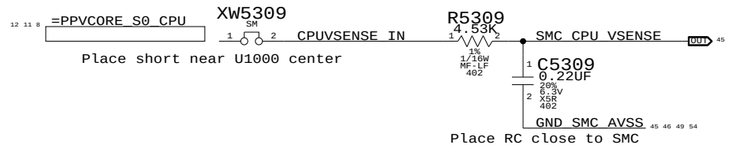
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

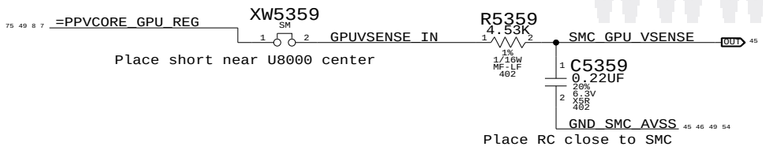
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 52 OF 109	

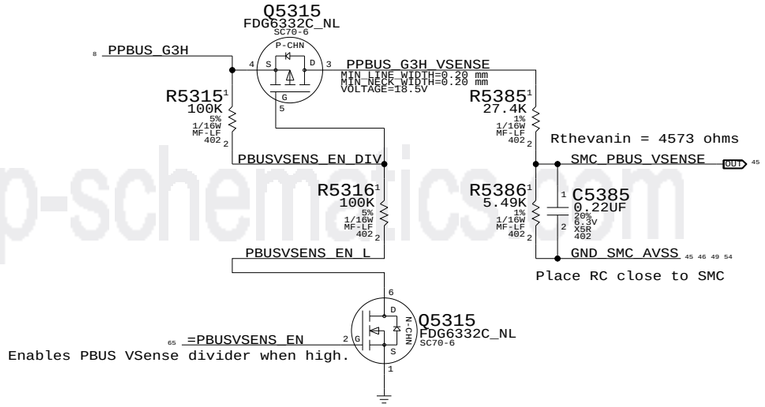
CPU Voltage Sense / Filter



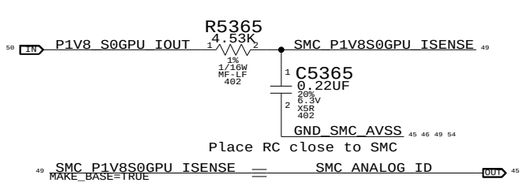
GPU Voltage Sense / Filter



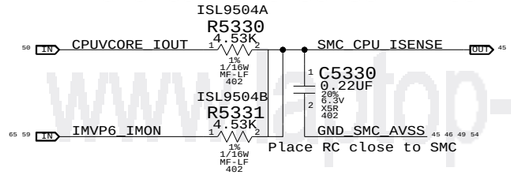
PBUS Voltage Sense & Filter



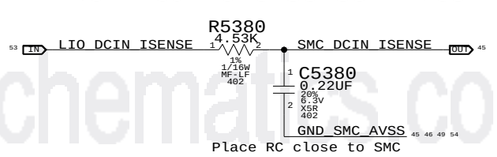
1.8V FB Current Sense Filter



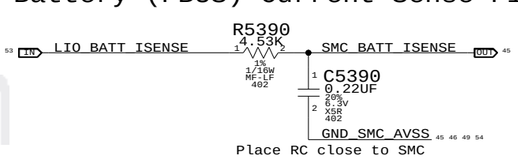
CPU Current Sense Filter



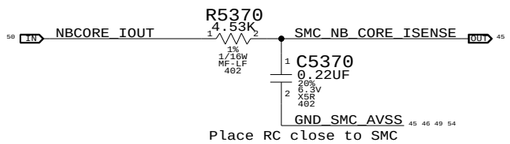
DCIN Current Sense Filter



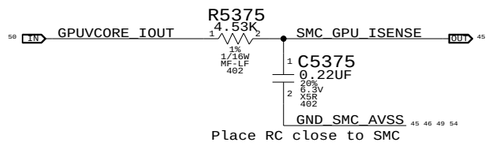
Battery (PBUS) Current Sense Filter



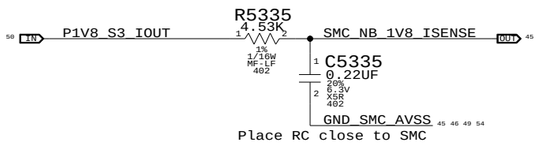
NB Core Current Sense Filter



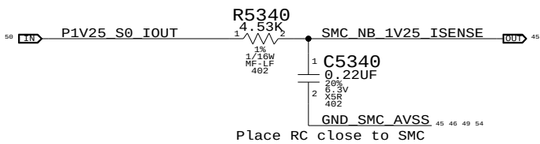
GPU Current Sense Filter



NB 1.8V Current Sense Filter

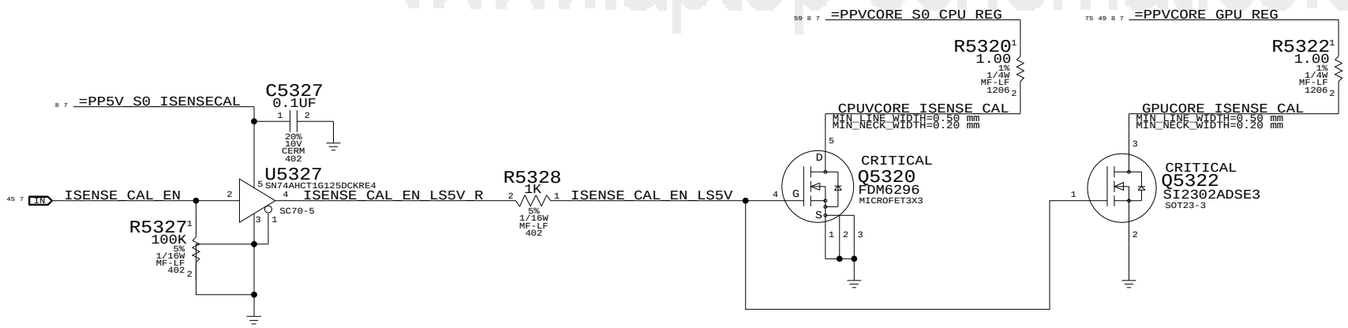


S0/GPU 1.25V Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

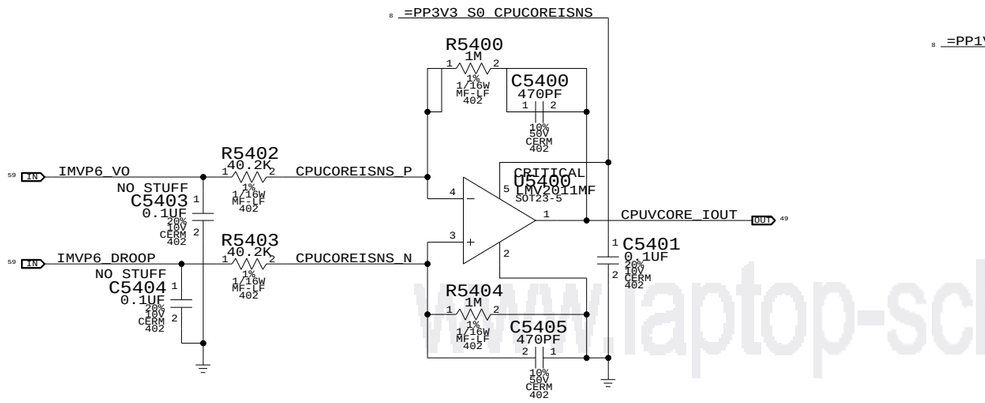
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

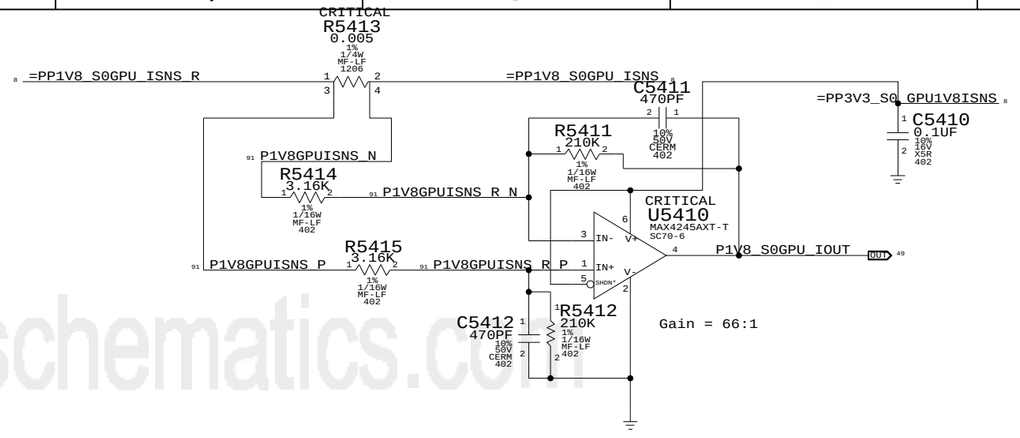
APPLE INC.

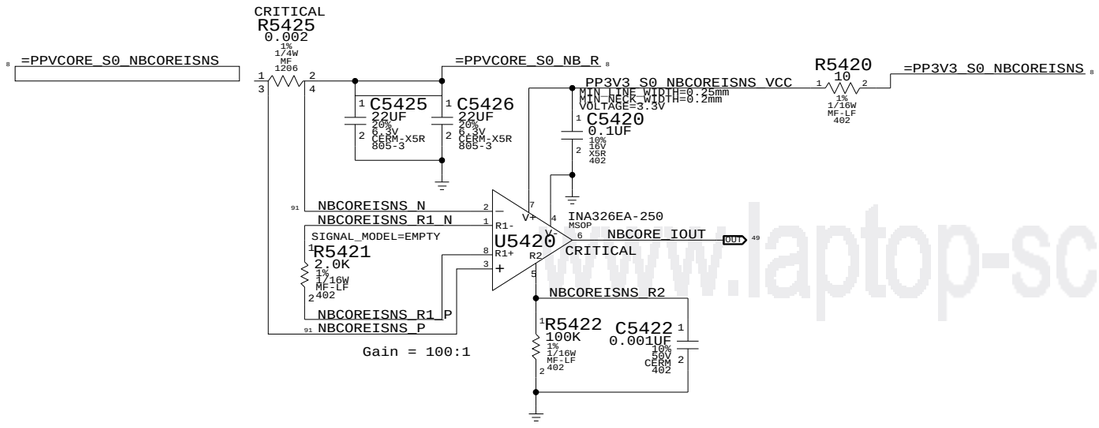
SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 53 OF 109	

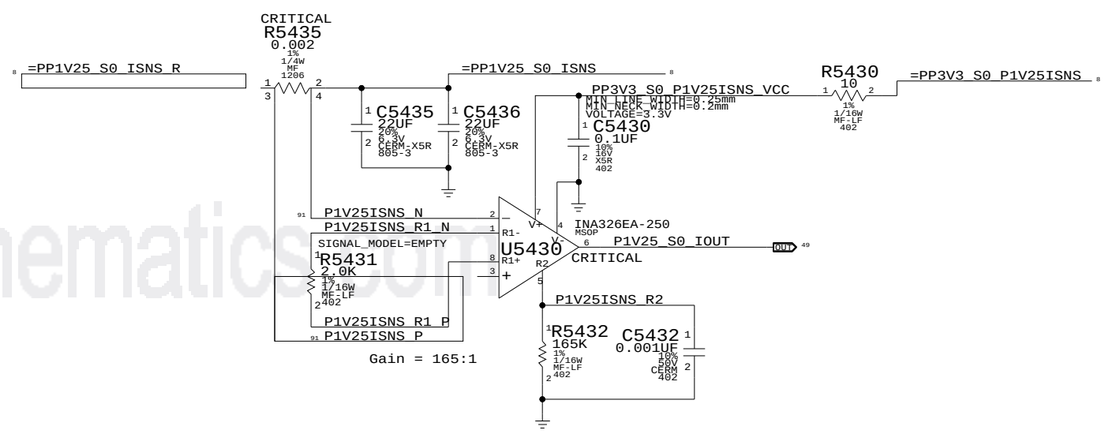
www.laptop-schematics.com

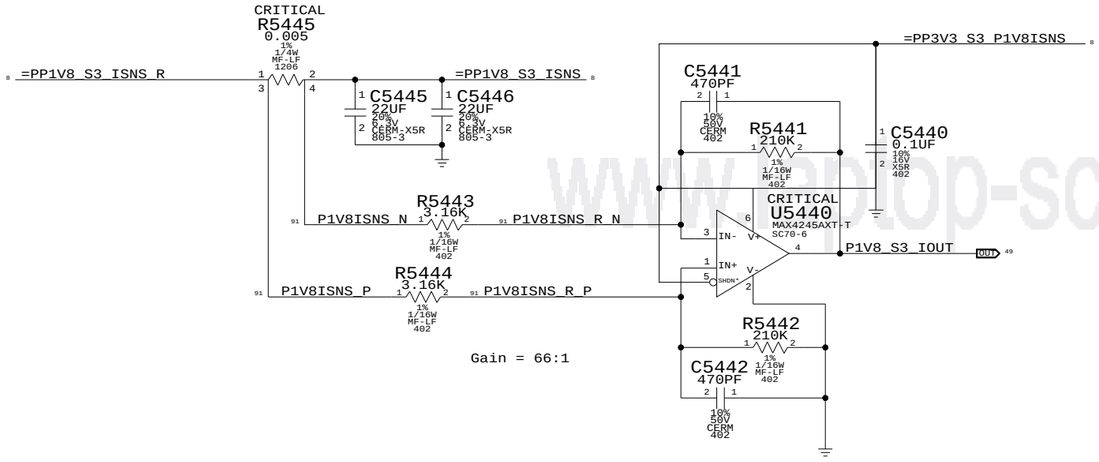
GPU VCore Current Sense

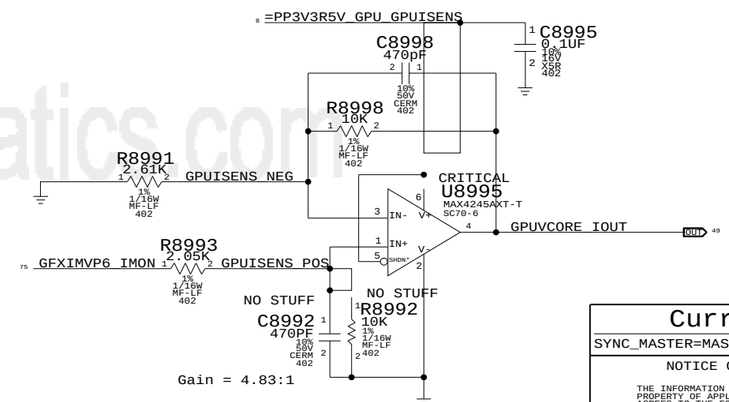












www.laptop-schematics.com

Current Sensing

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

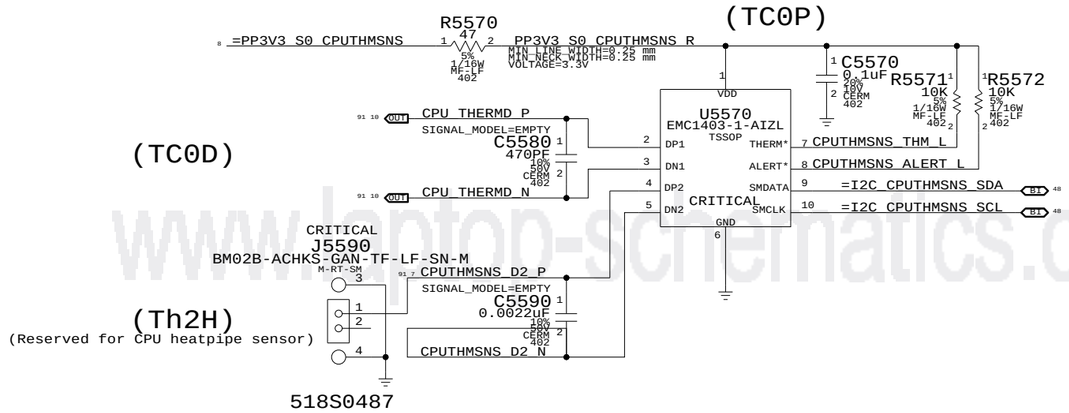
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

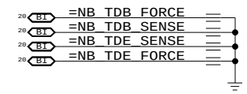
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	G
	SCALE: NONE	SHT 54 OF 109	

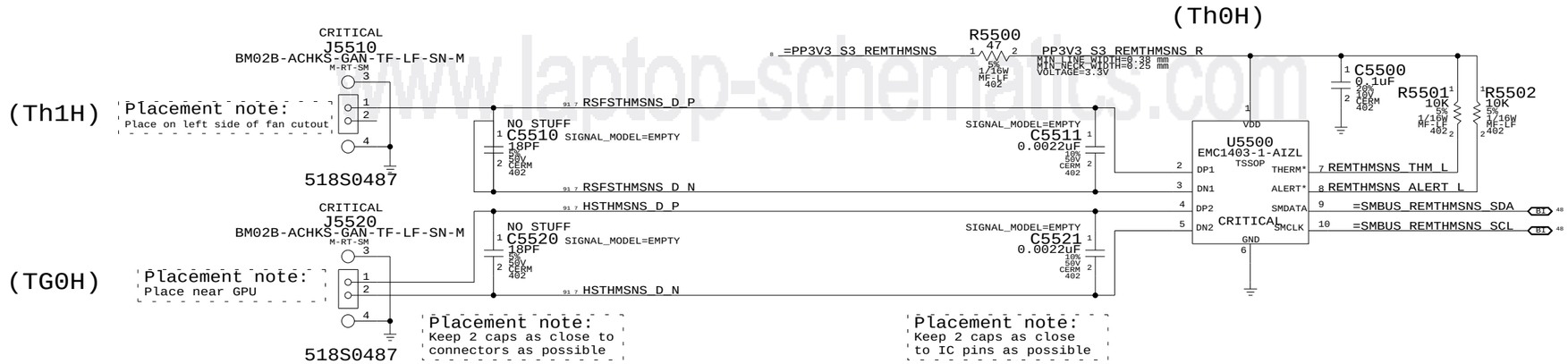
CPU T-Diode Thermal Sensor



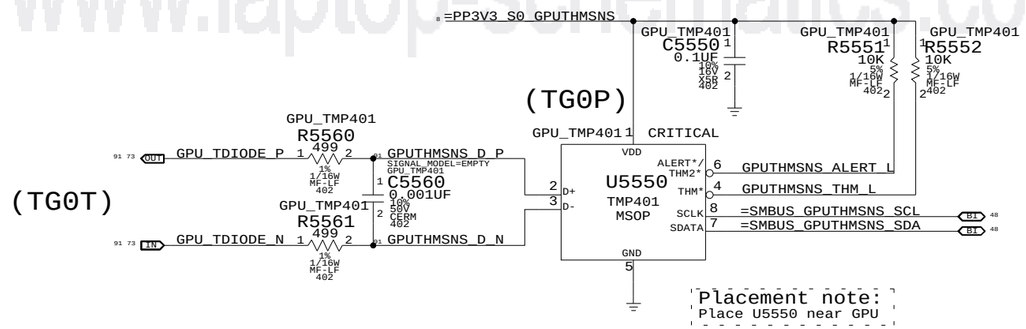
NB Thermal Diodes Not Used



GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



www.laptop-schematics.com

Thermal Sensors

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

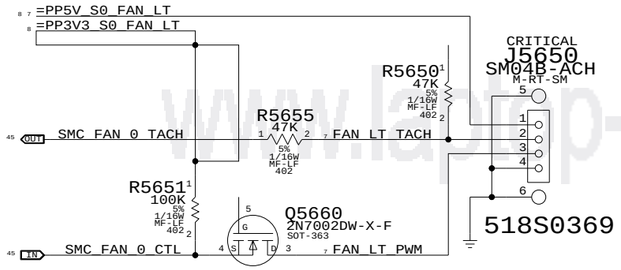
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

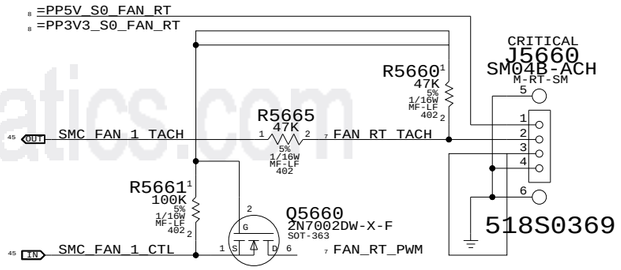
SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 55 OF 109	

www.laptop-schematics.com

Left Fan



Right Fan



www.laptop-schematics.com

www.laptop-schematics.com

Fan Connectors

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

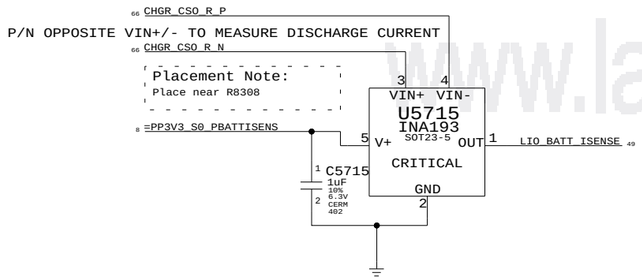
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

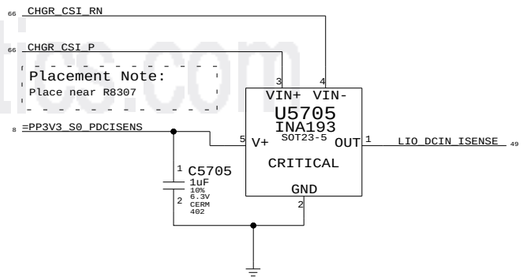
SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE	SHT	OF
NONE	56	109

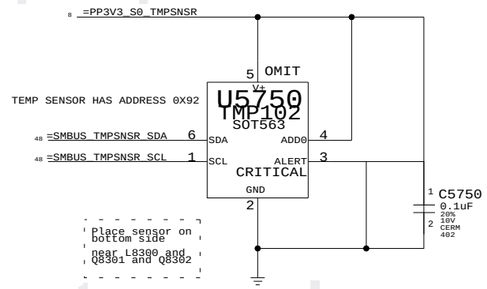
Battery Current Sense



DCIn Current Sense



Battery Charger Thermal Sensor



www.laptop-schematics.com

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2039	1	revE of TMP102	U5750	CRITICAL	

Current & Thermal Sensors

SYNC_MASTER=M87_LIO SYNC_DATE=11/06/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

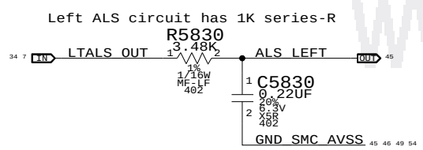
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

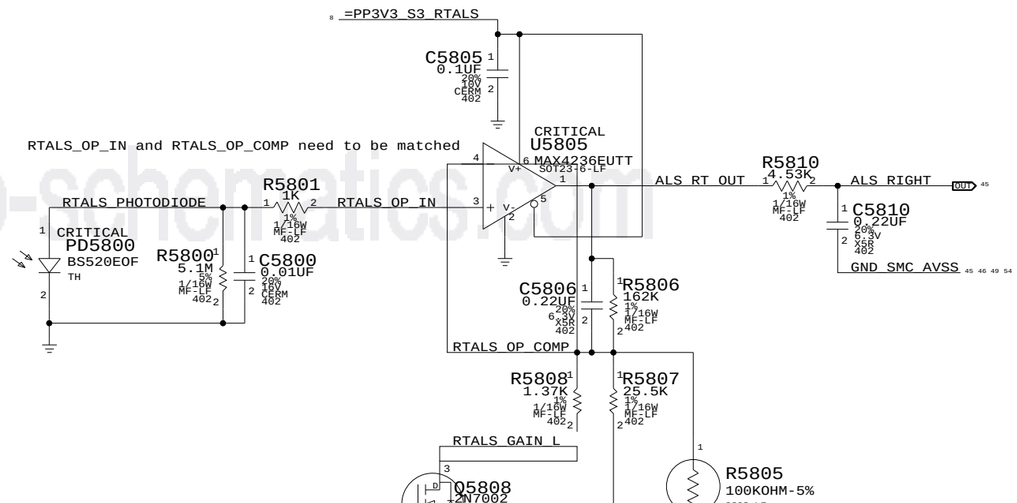
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 57 OF 109	

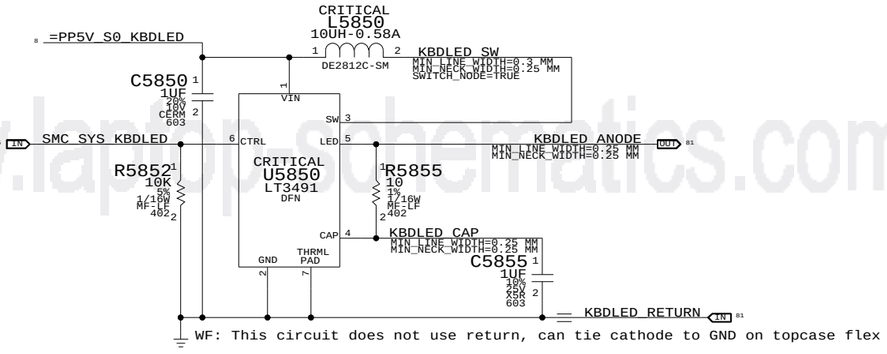
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



www.laptop-schematics.com

ALS Support

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

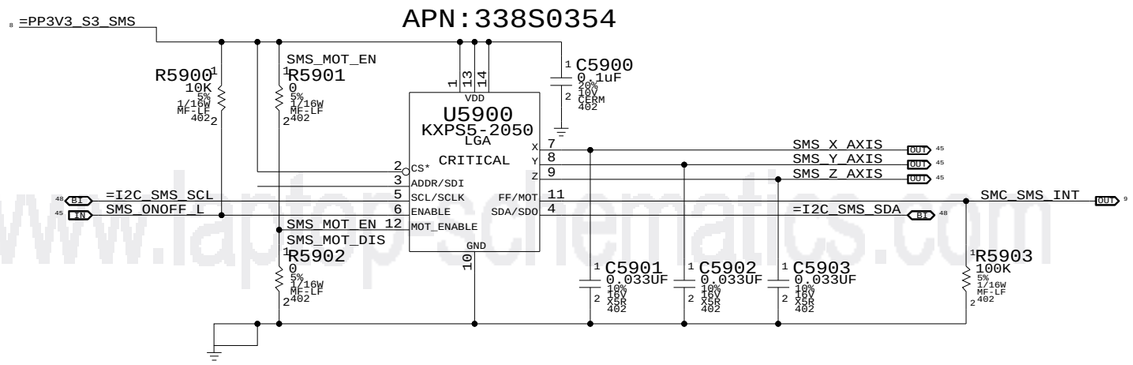
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 58 OF 109	

www.laptop-schematics.com

APN:338S0354

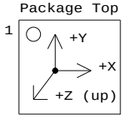


I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

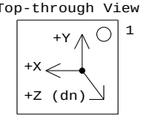
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



www.laptop-schematics.com

Sudden Motion Sensor (SMS)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

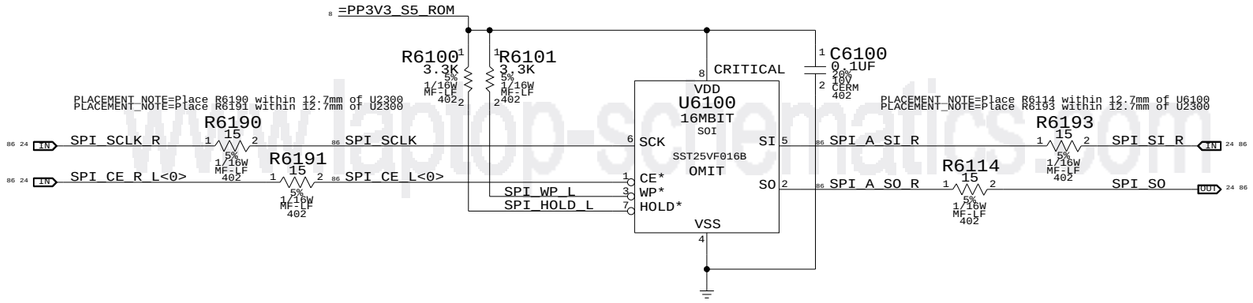
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE: NONE

SHT 59 OF 109

www.laptop-schematics.com



www.laptop-schematics.com

SPI BootROM

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

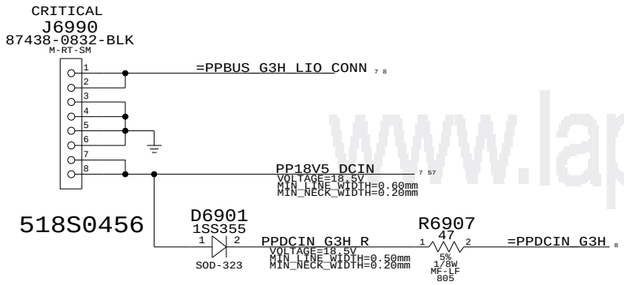
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

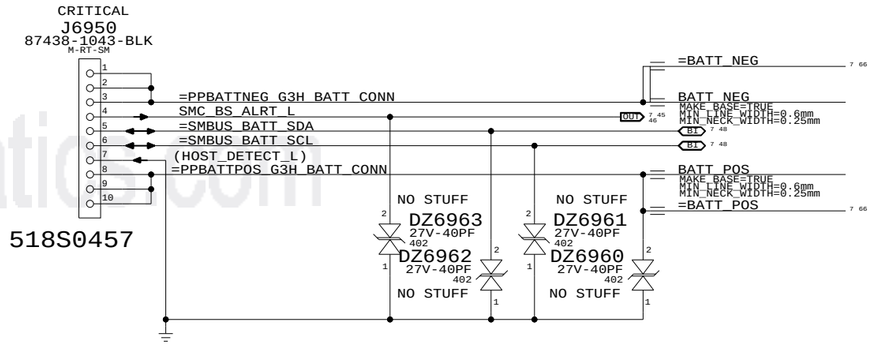
SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE	SHT	OF
NONE	61	109

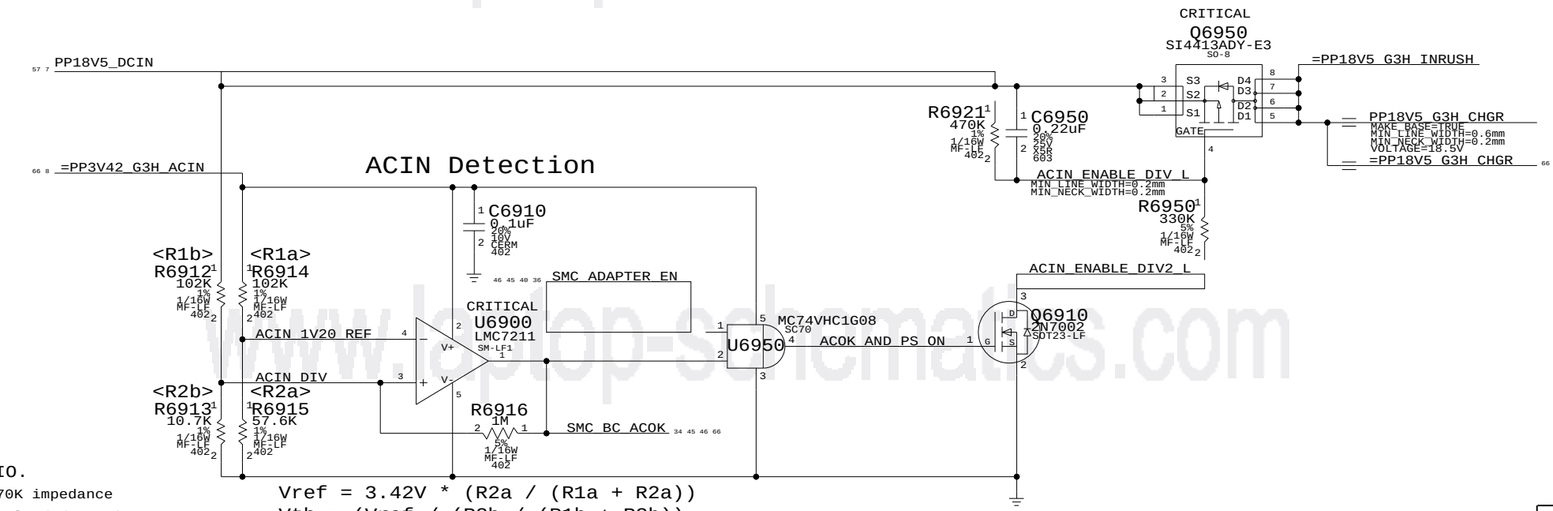
DC-In Connector



Battery Connector



Inrush Limiter



www.laptop-schematics.com

DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

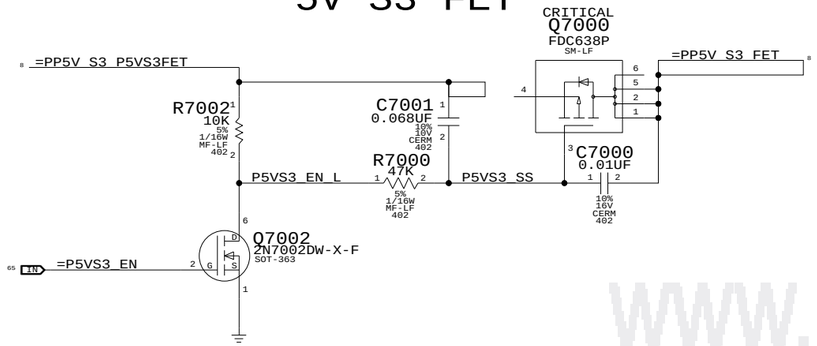
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

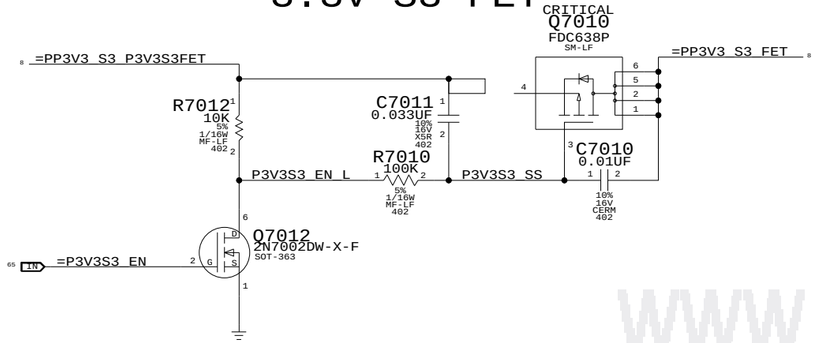
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 69 OF 109	

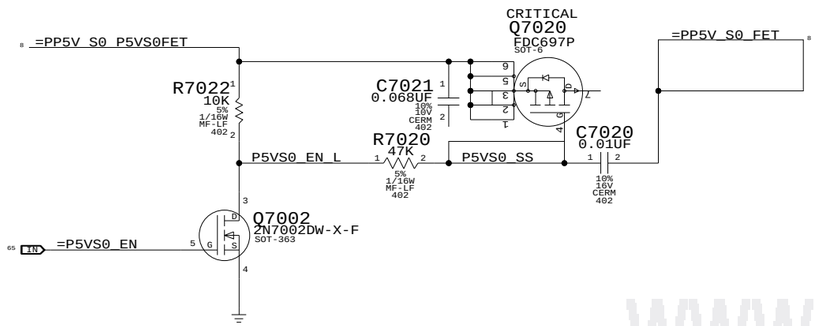
5V S3 FET



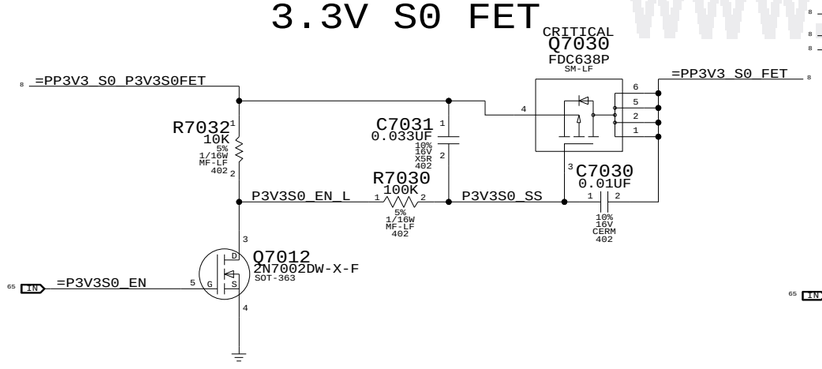
3.3V S3 FET



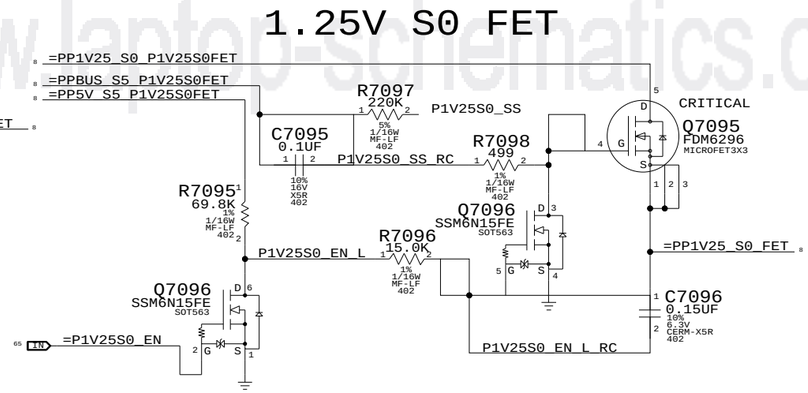
5V S0 FET



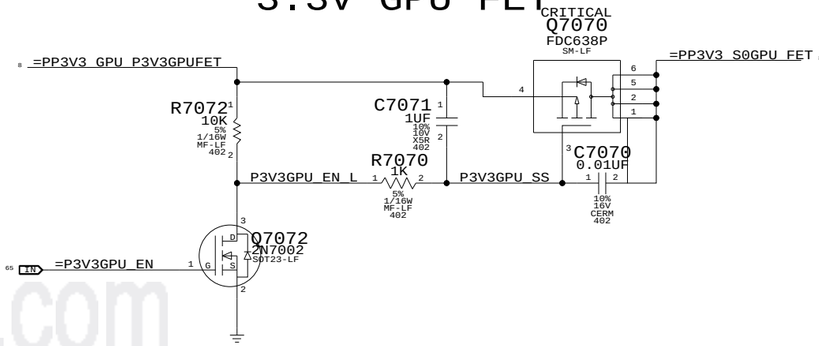
3.3V S0 FET



1.25V S0 FET



3.3V GPU FET



www.laptop-schematics.com

www.laptop-schematics.com

www.laptop-schematics.com

Power FETs

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

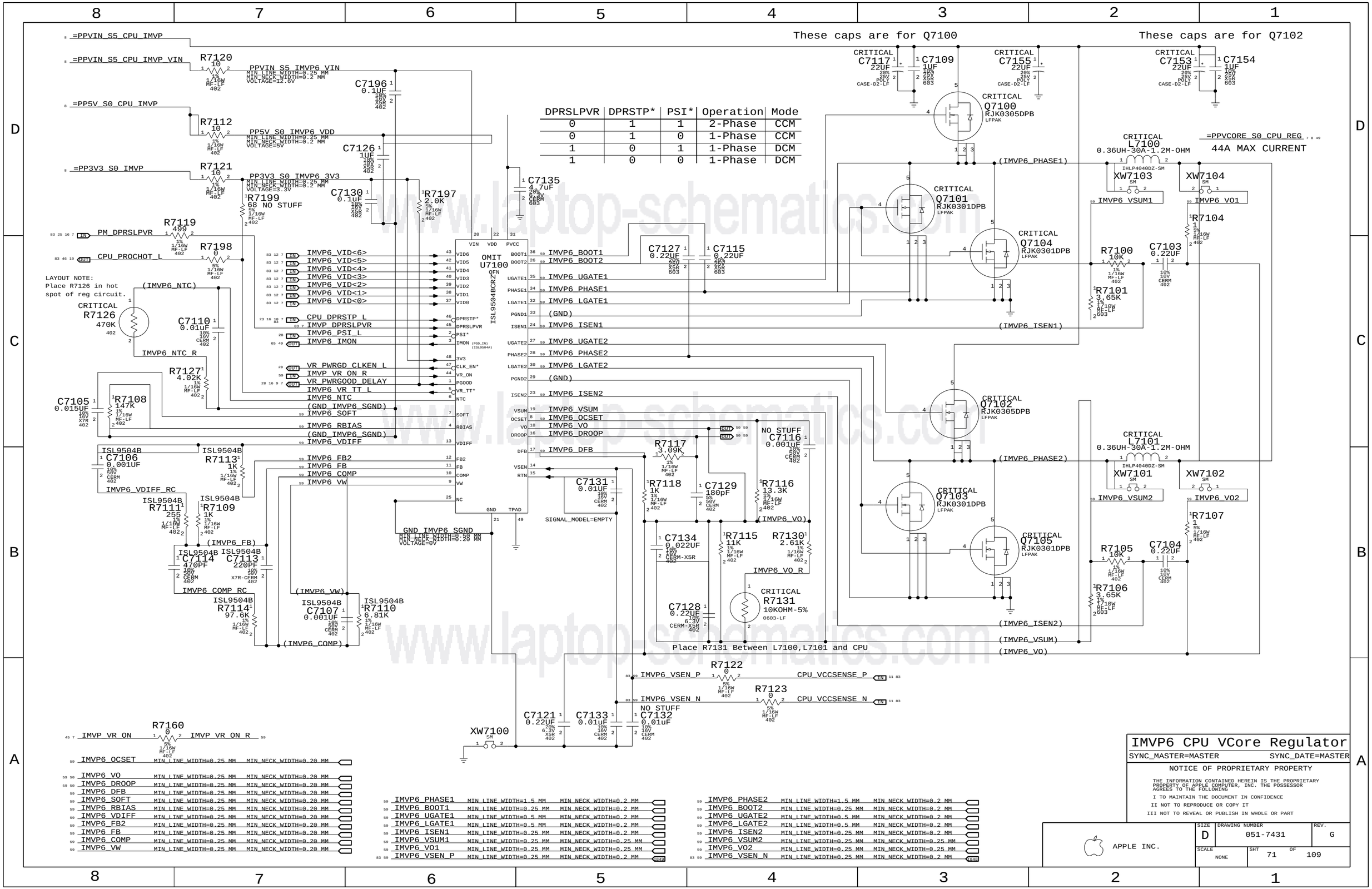
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE	SHT	OF
NONE	70	109



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

www.laptop-schematics.com

IMVP6 CPU VCore Regulator

SYNC_MASTER=MASTER SYNC_DATE=MASTER

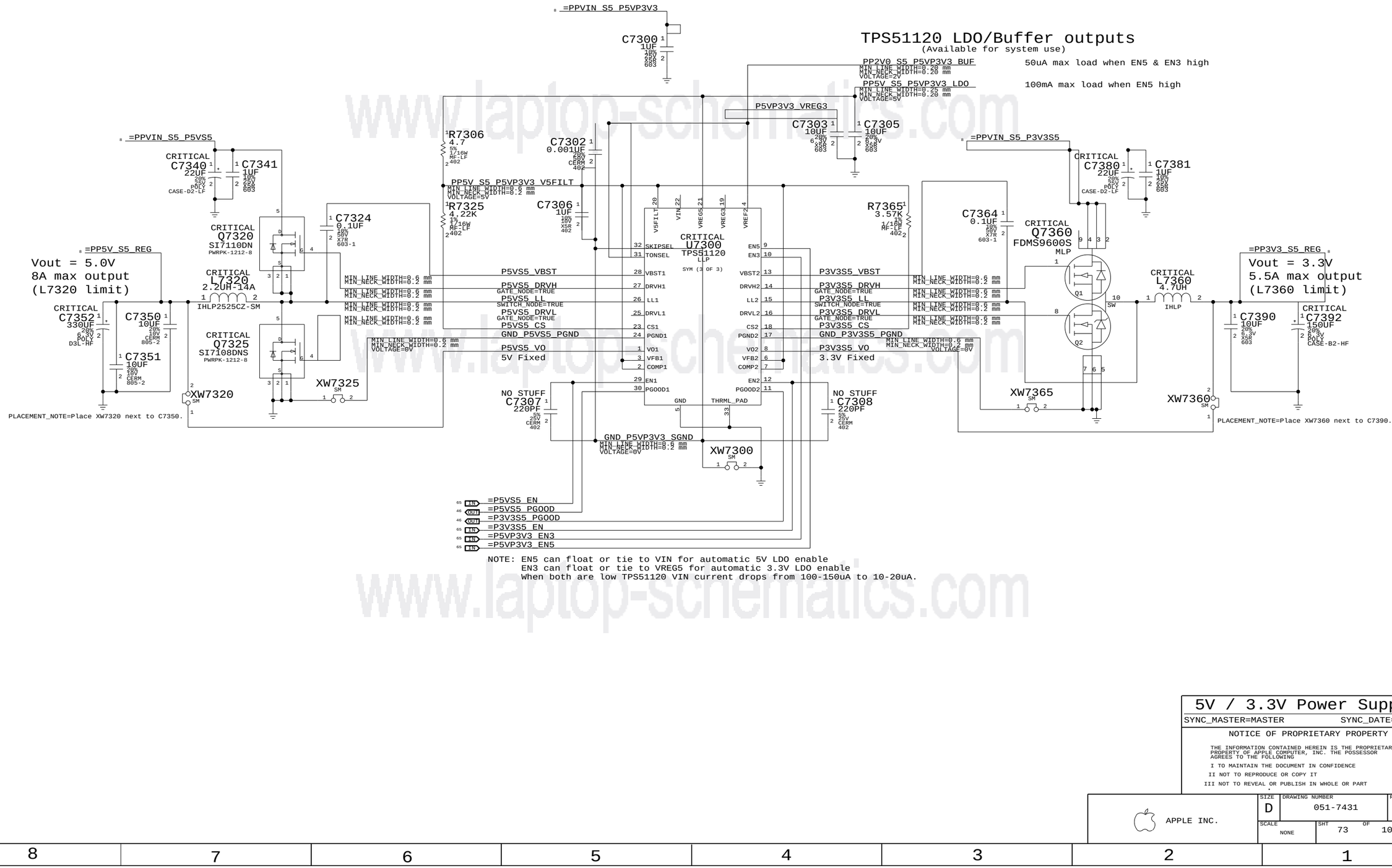
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE NONE	SHT 71 OF 109	



www.laptop-schematics.com

5V / 3.3V Power Supply

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

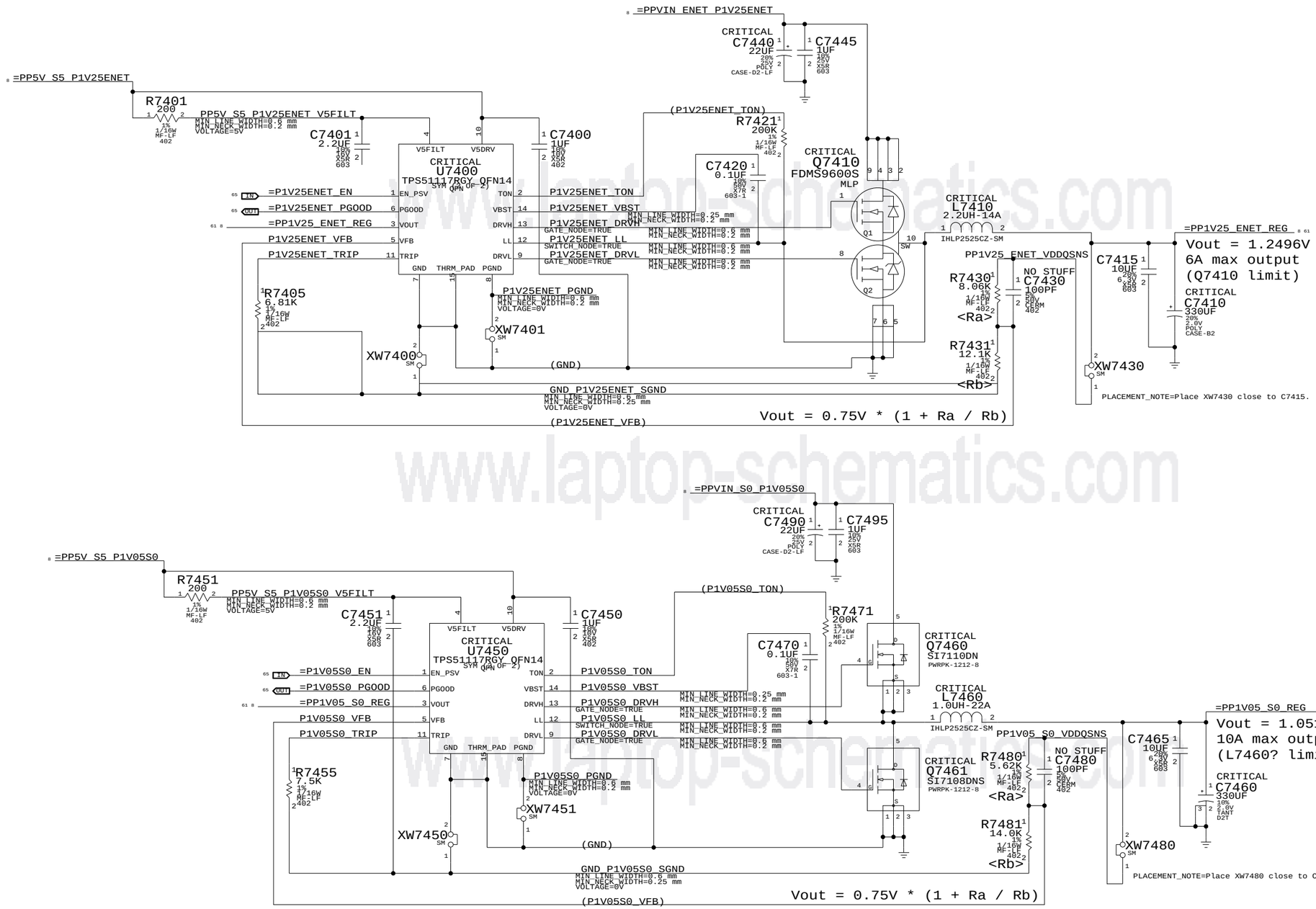
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 73 OF 109	



1.25V / 1.05V Power Supply

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

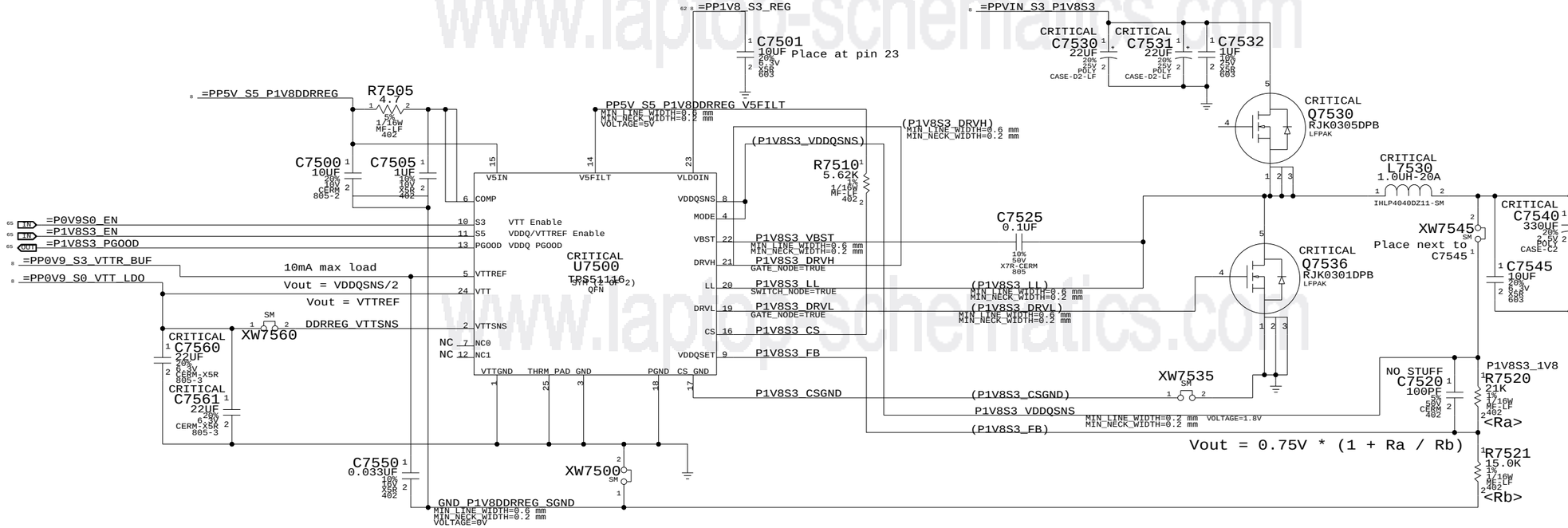
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE	SHT	OF
NONE	74	109

www.laptop-schematics.com



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0346	1	RES,MTL FILM,21.5K,1%,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V825

1.8V DDR2 Supply

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

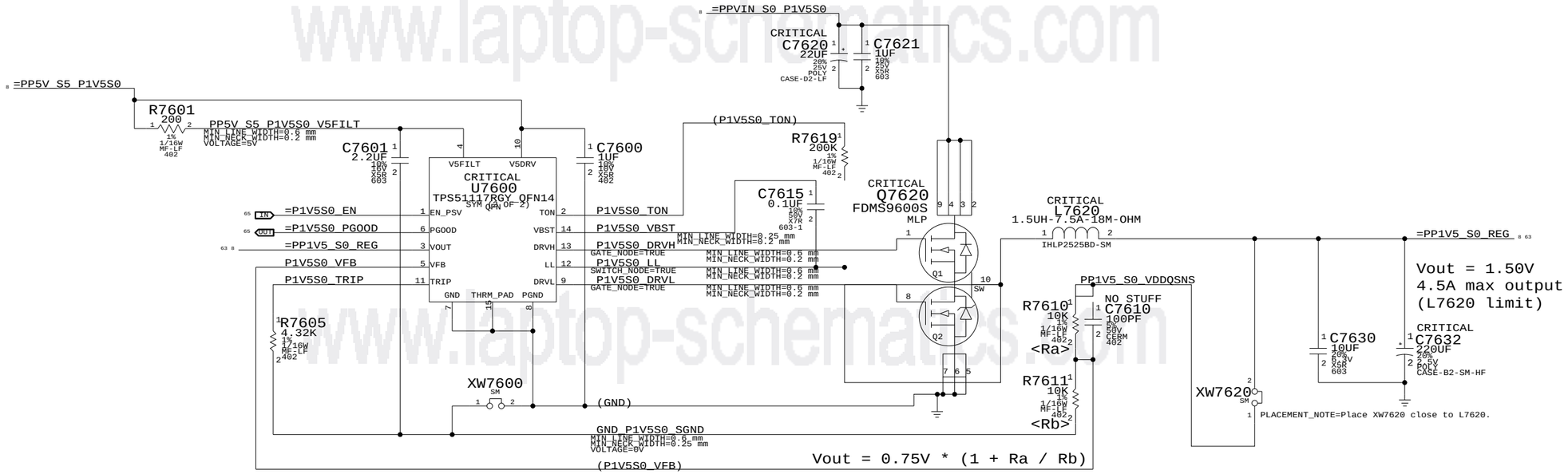
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE	SHT	OF
NONE	75	109

www.laptop-schematics.com

www.laptop-schematics.com



www.laptop-schematics.com

1.5V Power Supply

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

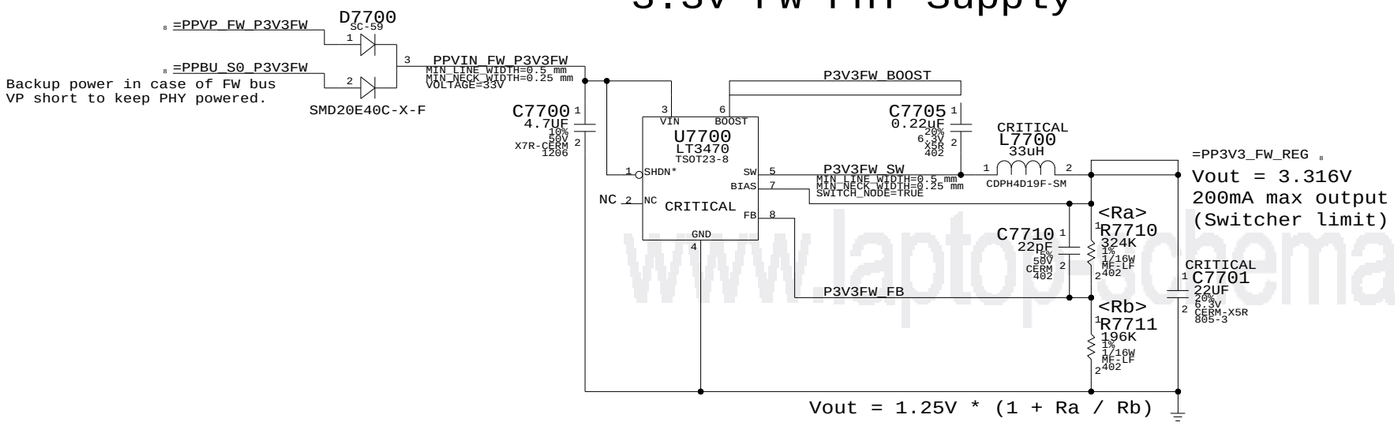
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

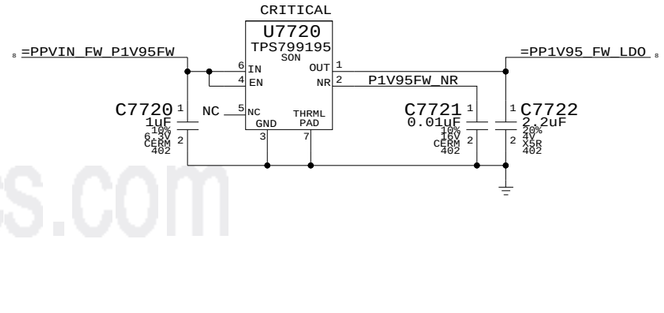
SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 76 OF 109	

www.laptop-schematics.com

3.3V FW PHY Supply



1.95V FW PHY Supply



www.laptop-schematics.com

FW PHY Power Supplies

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 77 OF 109	

Power Control Signals

=PP5V_S5_PWRCTL

=PP3V3_GPU_PWRCTL

G84M GPU requires rails to come up in the following order:
1) 1.2V
2) 3.3V
3) Vcore
4) 1.8V

R7850 10K 5% 1/16W MF-LF 402
R7851 10K 5% 1/16W MF-LF 402
R7852 100K 5% 1/16W MF-LF 402
R7854 10K 5% 1/16W MF-LF 402

=GPUVCORE_PGOOD

Need to ensure that TPS51117 PGOOD does not deassert while GPU VIDs are changing GPU core voltage.

PM_P1V8_S0GPU_EN = MAKE_BASE=TRUE
=P1V8_S0GPU_EN

PM_GPUVCORE_EN = MAKE_BASE=TRUE
=GPUVCORE_EN

Q7850 2N7002DW-X-F SOT-363
Q7851 2N7002DW-X-F SOT-363
Q7851 2N7002DW-X-F SOT-363

C7851 0.1UF 20% 16V CERM 402

PVCOREGPU_EN_L

PM_SLP_S3_LS5V = MAKE_BASE=TRUE
LIO_S0_EN_L

Q7850 2N7002DW-X-F SOT-363

PM_SLP_S3_L

R7856 100K 5% 1/16W MF-LF 402

(PM_SLP_S3_L) MAKE_BASE=TRUE

=PVCOREGPU_EN
=P5VS0_EN
=P3V3S0_EN
=P1V25S0_EN
=P0V9S0_EN
=PBUSVSENS_EN
=ENET_VMAIN_AVLBL
=PM_SLP_S3_DELAY_L

=PP3V3_S0_PWRCTL

=PP3V3_S5_PWRCTL

U7850 MC74VHC1G09 SC70

PM_SLP_S3_DELAY_L = MAKE_BASE=TRUE

R7859 10K 5% 1/16W MF-LF 402

NO STUFF
C7859 0.047UF 10% 16V CERM 402

=P1V5S0_EN
=P1V05S0_EN

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

=PPVIN_G3H_P3V42G3H

P3V42G3H5_BOOST

C7800 10UF 10% 16V CERM 1206-1

U7800 LT3470 TSOT23-8

C7805 0.22UF 20% 6.3V X5R 402

CRITICAL L7810 33UH CDPH4D19F-SM

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

NC CRITICAL

C7810 22pF 5% 50V CERM 402

<Ra> R7810 348K 1% 1/16W MF-LF 402

<Rb> R7811 200K 1% 1/16W MF-LF 402

P3V42G3H_FB

C7815 22UF 20% 6.3V CERM-X5R 805-3

=PP3V42_G3H_REG
Vout = 3.425
200mA max output
(Switcher limit)

Vout = 1.25V * (1 + Ra / Rb)

Unused PGOOD Signals

=P1V25ENET_PGOOD = MAKE_BASE=TRUE TP_P1V25ENET_PGOOD

=P1V8_S0GPU_PGOOD = MAKE_BASE=TRUE TP_P1V8_S0GPU_PGOOD

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

IMVP6_IMON
To CPU IMVP6

=PP3V3_S5_P1V5P1V05PG

ISL9504A

R7865 100K 5% 1/16W MF-LF 402

R7866 0 5% 1/16W MF-LF 402

=PP3V3_S0_ALLSYSPG

C7880 0.1UF 20% 16V CERM 402

=P1V5S0_PGOOD
TPS51117 PGOOD threshold 92.5-97.5% (1.36 - 1.46V)
=P1V05S0_PGOOD
TPS51117 PGOOD threshold 92.5-97.5% (0.98 - 1.02V)
=P1V8S3_PGOOD

P1V8P1V5P1V05S0_PGOOD = MAKE_BASE=TRUE

U7880 MC74VHC1G08 SC70

ALL_SYS_PWRGD

PP1V25_S0_ISNS

=PP3V3_S3_PWRCTL

MAX6838 threshold is 93.5% @ 1.120V

R7860 154K 1% 1/16W MF-LF 402

U7860 MAX6838XSD0 SC70-4

S0PGOOD_1V2_DIV

R7861 100K 1% 1/16W MF-LF 402

C7860 0.0047UF 10% 16V CERM 402

R7862 100K 5% 1/16W MF-LF 402

PM_P3V3GPU_EN = MAKE_BASE=TRUE
=P3V3GPU_EN

=P1V25_PWRGD

PM_ENET_EN
(PM_ENET_EN) MAKE_BASE=TRUE
=P1V25ENET_EN

PM_S4_STATE_L
(PM_S4_STATE_L) MAKE_BASE=TRUE
=P3V3S3_EN
=P5VS3_EN
=USB_EXTA_EN
LIO_S3_EN

R7857 10K 5% 1/16W MF-LF 402

R7855 10K 5% 1/16W MF-LF 402

P1V8S3_EN = MAKE_BASE=TRUE
=P1V8S3_EN

C7855 0.47UF 10% 6.3V CERM-X5R 402

SMC_PM_G2_EN

PM_G2_EN = MAKE_BASE=TRUE
=P5VP3V3_EN5
=P5VP3V3_EN3

=PP3V42_G3H_PWRCTL

C7858 0.1UF 20% 10V CERM 402

R7858 100K 5% 1/16W MF-LF 402

U7858 MC74VHC1G09 SC70

PM_G2_P5VS5_EN = MAKE_BASE=TRUE
=P5VS5_EN

U7859 MC74VHC1G09 SC70

PM_G2_P3V3S5_EN = MAKE_BASE=TRUE
=P3V3S5_EN

NOTE: 0.9V is not checked!

Other S0 Rails PWRGD Circuit

PP3V3GPU_EN IS A PROXY FOR 1.2V

=PP5V_S0
=PP3V3_S0
=PP1V8_S0GPU_ISNS
=P1V25_PWRGD

C7872 0.1UF 20% 10V CERM 402

C7871 0.1UF 20% 10V CERM 402

C7870 0.1UF 20% 10V CERM 402

R7875 10K 5% 1/16W MF-LF 402

U7870 LTC2900 DFN

V1 V2 V3 V4 VREF VPG PBR* RST* CRT GND THRM_PAD

NC

S0PGOOD_PWROK

S0PGOOD_VREF

R7870 9.53K 1% 1/16W MF-LF 402

S0PGOOD_CRT

S0PGOOD_VPG

R7871 93.1K 1% 1/16W MF-LF 402

C7875 0.047UF 10% 16V CERM 402

Trst = 4.6ms/nF
Trst = 216ms

LTC2900 typical threshold is 93.5% (4.675V, 3.086V, 1.685V,1.120V)

www.laptop-schematics.com

3.425V G3Hot Supply & Power Control

SYNC_MASTER=M87_MLB SYNC_DATE=09/26/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 78 OF 109	

PBus Supply & Battery Charger

=PP18V5_G3H_CHGR
=PP3V42_G3H_ACIN
CHGR_VDD
CHGR_SGND
CHGR_EN
CHGR_ACPRN
CHGR_ACSET
CHGR_DCIN
CHGR_CSO_R_N
CHGR_ICOMP
CHGR_VCOMP
CHGR_VCOMP_C
CHGR_ICM_R
CHGR_ACLIM
TP_CHGR_VADJ
CHGR_CSO_P
CHGR_CHLIM
CHGR_VREF
CHGR_ACPRN
CHGR_ACSET
CHGR_SGND
CHGR_VDDP
CHGR_SGATE
CHGR_CSI_P
CHGR_CSI_N
NC_CHGR_BGATE
CHGR_DCIN
CHGR_BOOT
CHGR_UGATE
CHGR_LGATE
CHGR_EN
TP_CHGR_DCPRN
TP_CHGR_DCSET
CHGR_PHASE
CHGR_VDDP
CHGR_CSI_RN
PPVDCIN_G3H_PRE
PPVDCIN_G3H_R
PPVBAT_G3H_CHGR_REG
PPVBAT_G3H_CHGR_OUT
CHGR_CSO_N
CHGR_CSO_P
10A MAX, LIMITED BY L7900, Q7901

Q7940 IRLML5203-2.6A SM
Q7950 SSM3K15FV SOD-VESM
Q7901 RJK0305DPB LFPAK CRITICAL
Q7902 RJK0305DPB LFPAK CRITICAL
D7940 RAV99T-X-F SOT-523-3
D7950 BAT54CW-X-F SOT-323
D7900 B0530WXF SOD-123 CRITICAL
D7903 MMBZ5235B SOT23 CRITICAL
Q7900 SI4413ADY-E3 SO-8 CRITICAL
U7900 ISL6257HRZ QFN CRITICAL
353S1510
L7900 4.7UH-10.2A FDA1254-SM CRITICAL

R7940 110K 1% 1/16W MF-LF 402
R7941 11.3K 1% 1/16W MF-LF 402
R7944 100K 1% 1/16W MF-LF 402
R7950 100K 1% 1/16W MF-LF 402
R7924 100K 1% 1/16W MF-LF 402
R7900 4.7 5% 1/16W MF-LF 402
R7902 3.01K 1% 1/16W MF-LF 402
R7992 56.2K 1% 1/16W MF-LF 402
R7910 NO STUFF 100K 1% 1/16W MF-LF 402
R7907 0.02 1% 1/4W MF 0612
R7905 18 5% 1/16W MF-LF 402
R7903 2.2 5% 1/16W MF-LF 402
R7970 49.9 1% 1/16W MF-LF 603
R7908 0.01 1% 1/4W MF 0612
R7904 0 5% 1/16W MF-LF 402
R7906 2.2 5% 1/16W MF-LF 402

C7911 1UF 10% 6.3V CERM 402
C7901 1000PF 10% 25V X7R 402
C7912 1UF 10% 6.3V CERM 402
C7904 0.1UF 20% 25V CERM 402
C7940 0.1UF 20% 25V CERM 603
C7907 0.1UF 20% 25V CERM 603
C7941 0.1UF 10% 16V X5R 402
C7900 0.033UF 10% 16V X7R 402
C7915 680PF 10% 50V CERM 402
C7902 0.0082UF 10% 16V X7R 402
C7990 470PF 10% 50V CERM 402
C7903 0.1UF 20% 25V CERM 603
C7970 0.0022UF 10% 16V CERM 603
C7916 2.2UF 20% 6.3V X5R-CERM 805
C7917 2.2UF 20% 6.3V X5R-CERM 805
C7905 22UF 20% 6.3V POLY CASE-D2-LF
C7906 22UF 20% 6.3V POLY CASE-D2-LF
C7908 22UF 20% 25V POLY CASE-D2-LF
C7910 1UF 10% 10V X5R 603
C7927 0.001UF 10% 50V CERM 402

XW7900 SM
XW7901 SM
XW7902 SM
XW7903 SM
XW7904 SM

MIN_LINE_WIDTH=0.2mm MIN_NECK_WIDTH=0.2mm NO_TEST=TRUE
MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.2mm
MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm
MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=8.25mm
MIN_LINE_WIDTH=0.2mm MIN_NECK_WIDTH=0.2mm SWITCH_NODE=TRUE
MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.2mm

Energy Star LDO

=PP18V5_G3H_CHGR
PBUS_LDO_EN
LDO_OUT
LDO_FDBK
=PPVBAT_G3H_CHGR_REG

U7950 MAX8719 TDFN
D7950 BAT54CW-X-F SOT-323
R7954 100K 5% 1/16W MF-LF 402
R7952 200K 1% 1/16W MF-LF 402
R7953 19.6K 1% 1/16W MF-LF 402
C7950 1UF 10% 25V X5R 603
C7951 1UF 10% 25V X5R 603

VOLTAGE FOLLOWER GUARANTEES CURRENT LIMIT CIRCUITS ARE PROVIDED WITH SUFFICIENT CURRENT WITHOUT SINKING CURRENT FROM VREF.

=PP3V42_G3H_ACIN
CHGR_VREF
CHGR_VREF_VF
CHGR_SGND

U7901 MAX4245AXT-T SC70-6 CRITICAL
C7980 0.1UF 20% 25V CERM 402

Adapter Input Current Limit

As shown, Isys =~4.6A max

SMC_SYS_ISET
SMC_SYS_ISET_L
CHGR_ACLIM_R

Q7960 SSM6N15FE SOT563
R7968 3.48K 1% 1/16W MF-LF 402
R7969 10K 5% 1/16W MF-LF 402
R7960 3.01K 1% 1/16W MF-LF 402
R7963 20.0K 1% 1/16W MF-LF 402
C7961 0.047UF 10% 16V CERM 402

Battery Charge Current Limit

As shown, Ichg = 4.5A max

SMC_BATT_ISET
SMC_BATT_ISET_L
CHGR_CHLIM_R

Q7961 SSM6N15FE SOT563
R7964 3.57K 1% 1/16W MF-LF 402
R7967 158K 1% 1/16W MF-LF 402
R7962 17.8K 1% 1/16W MF-LF 402
R7966 11.3K 1% 1/16W MF-LF 402
C7962 0.01UF 10% 16V CERM 402

Battery Charge FETs

PPVBAT_G3H_CHGR_OUT
CHG_EN_DIV_L
CHG_EN_DIV2_L
TCHG_EN_DIV_L
TCHG_EN_DIV2_L
SMC_BATT_CHG_EN
CHGR_ACPRN
SMC_BC_ACOK
SMC_BATT_TRICKLE_EN_L
=BATT_POS
=BATT_NEG

Q7920 SI4413ADY-E3 SO-8 CRITICAL
Q7921 SI4413ADY-E3 SO-8 CRITICAL
Q7970 SI4413ADY-E3 SO-8 CRITICAL
Q7924 SSM6N15FE SOT563
Q7922 SSM6N15FE SOT563
F7902 8AMP-24V 1206-1 CRITICAL
D7921 1SS355 SOD-323

R7920 27 5% 1/4W MF 2525-1 CRITICAL
R7921 47 5% 1/8W MF-LF 805
R7930 470K 1% 1/16W MF-LF 402
R7931 330K 5% 1/16W MF-LF 402
R7922 39.2K 1% 1/16W MF-LF 402
R7923 35.7K 1% 1/16W MF-LF 402
R7972 330K 5% 1/16W MF-LF 402
R7971 470K 5% 1/16W MF-LF 402

C7922 0.01UF 10% 16V CERM 402
C7921 0.1UF 10% 16V X5R 402
C7920 0.01UF 10% 16V CERM 402
C7925 0.22UF 10% 16V CERM 402
C7924 0.01UF 10% 16V CERM 402
C7971 0.1UF 10% 25V X5R 402

PPVBAT_G3H_PRE
PPVBAT_G3H_DIO
PPVBAT_G3H_FET
PPVBAT_G3H_FET_F
MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm VOLTAGE=12.6V
MIN_LINE_WIDTH=0.2mm MIN_NECK_WIDTH=0.2mm

PBus Supply & Batt. Charger
SYNC_MASTER=MASTER SYNC_DATE=MASTER
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 79 OF 109	

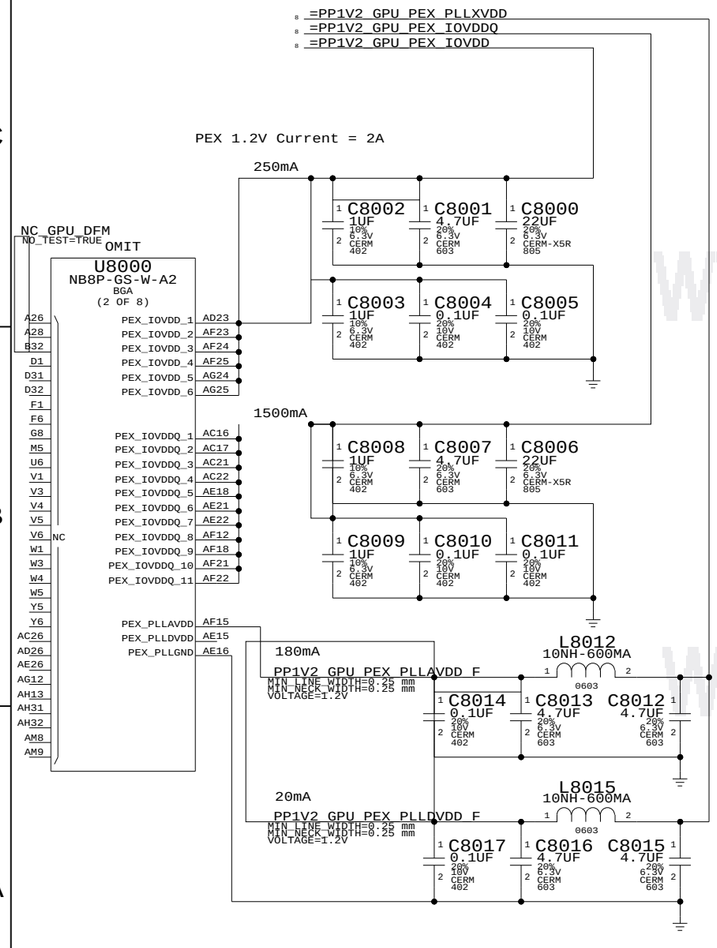
www.laptop-schematics.com

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



OMIT
U8000
NB8P-GS-W-A2
BGA
(1 OF 8)

PCI-EXPRESS BUS INTERFACE

PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AK13 PEX_RX0	PEX_TX0 AJ15	PEG_D2R_C_P<0>	C8055 0.1uF	PEG_D2R_P<0>
PEG_R2D_C_N<0>	C8021 0.1uF	PEG_R2D_N<0>	AK14 PEX_RX0_L	PEX_TX0_L AK15	PEG_D2R_C_N<0>	C8056 0.1uF	PEG_D2R_N<0>
PEG_R2D_C_P<1>	C8022 0.1uF	PEG_R2D_P<1>	AM14 PEX_RX1	PEX_TX1 AH16	PEG_D2R_C_P<1>	C8057 0.1uF	PEG_D2R_P<1>
PEG_R2D_C_N<1>	C8023 0.1uF	PEG_R2D_N<1>	AM15 PEX_RX1_L	PEX_TX1_L AG16	PEG_D2R_C_N<1>	C8058 0.1uF	PEG_D2R_N<1>
PEG_R2D_C_P<2>	C8024 0.1uF	PEG_R2D_P<2>	AL15 PEX_RX2	PEX_TX2 AG17	PEG_D2R_C_P<2>	C8059 0.1uF	PEG_D2R_P<2>
PEG_R2D_C_N<2>	C8025 0.1uF	PEG_R2D_N<2>	AL16 PEX_RX2_L	PEX_TX2_L AH17	PEG_D2R_C_N<2>	C8060 0.1uF	PEG_D2R_N<2>
PEG_R2D_C_P<3>	C8026 0.1uF	PEG_R2D_P<3>	AK16 PEX_RX3	PEX_TX3 AG18	PEG_D2R_C_P<3>	C8061 0.1uF	PEG_D2R_P<3>
PEG_R2D_C_N<3>	C8027 0.1uF	PEG_R2D_N<3>	AK17 PEX_RX3_L	PEX_TX3_L AH18	PEG_D2R_C_N<3>	C8062 0.1uF	PEG_D2R_N<3>
PEG_R2D_C_P<4>	C8028 0.1uF	PEG_R2D_P<4>	AL17 PEX_RX4	PEX_TX4 AK18	PEG_D2R_C_P<4>	C8063 0.1uF	PEG_D2R_P<4>
PEG_R2D_C_N<4>	C8029 0.1uF	PEG_R2D_N<4>	AL18 PEX_RX4_L	PEX_TX4_L AJ18	PEG_D2R_C_N<4>	C8064 0.1uF	PEG_D2R_N<4>
PEG_R2D_C_P<5>	C8030 0.1uF	PEG_R2D_P<5>	AM18 PEX_RX5	PEX_TX5 AJ19	PEG_D2R_C_P<5>	C8065 0.1uF	PEG_D2R_P<5>
PEG_R2D_C_N<5>	C8031 0.1uF	PEG_R2D_N<5>	AM19 PEX_RX5_L	PEX_TX5_L AH19	PEG_D2R_C_N<5>	C8066 0.1uF	PEG_D2R_N<5>
PEG_R2D_C_P<6>	C8032 0.1uF	PEG_R2D_P<6>	AK19 PEX_RX6	PEX_TX6 AG20	PEG_D2R_C_P<6>	C8067 0.1uF	PEG_D2R_P<6>
PEG_R2D_C_N<6>	C8033 0.1uF	PEG_R2D_N<6>	AK20 PEX_RX6_L	PEX_TX6_L AH20	PEG_D2R_C_N<6>	C8068 0.1uF	PEG_D2R_N<6>
PEG_R2D_C_P<7>	C8034 0.1uF	PEG_R2D_P<7>	AL20 PEX_RX7	PEX_TX7 AG21	PEG_D2R_C_P<7>	C8069 0.1uF	PEG_D2R_P<7>
PEG_R2D_C_N<7>	C8035 0.1uF	PEG_R2D_N<7>	AL21 PEX_RX7_L	PEX_TX7_L AH21	PEG_D2R_C_N<7>	C8070 0.1uF	PEG_D2R_N<7>
PEG_R2D_C_P<8>	C8036 0.1uF	PEG_R2D_P<8>	AM21 PEX_RX8	PEX_TX8 AK21	PEG_D2R_C_P<8>	C8071 0.1uF	PEG_D2R_P<8>
PEG_R2D_C_N<8>	C8037 0.1uF	PEG_R2D_N<8>	AM22 PEX_RX8_L	PEX_TX8_L AJ21	PEG_D2R_C_N<8>	C8072 0.1uF	PEG_D2R_N<8>
PEG_R2D_C_P<9>	C8038 0.1uF	PEG_R2D_P<9>	AK22 PEX_RX9	PEX_TX9 AJ22	PEG_D2R_C_P<9>	C8073 0.1uF	PEG_D2R_P<9>
PEG_R2D_C_N<9>	C8039 0.1uF	PEG_R2D_N<9>	AK23 PEX_RX9_L	PEX_TX9_L AH22	PEG_D2R_C_N<9>	C8074 0.1uF	PEG_D2R_N<9>
PEG_R2D_C_P<10>	C8040 0.1uF	PEG_R2D_P<10>	AL23 PEX_RX10	PEX_TX10 AG23	PEG_D2R_C_P<10>	C8075 0.1uF	PEG_D2R_P<10>
PEG_R2D_C_N<10>	C8041 0.1uF	PEG_R2D_N<10>	AL24 PEX_RX10_L	PEX_TX10_L AH23	PEG_D2R_C_N<10>	C8076 0.1uF	PEG_D2R_N<10>
PEG_R2D_C_P<11>	C8042 0.1uF	PEG_R2D_P<11>	AM24 PEX_RX11	PEX_TX11 AK24	PEG_D2R_C_P<11>	C8077 0.1uF	PEG_D2R_P<11>
PEG_R2D_C_N<11>	C8043 0.1uF	PEG_R2D_N<11>	AM25 PEX_RX11_L	PEX_TX11_L AJ24	PEG_D2R_C_N<11>	C8078 0.1uF	PEG_D2R_N<11>
PEG_R2D_C_P<12>	C8044 0.1uF	PEG_R2D_P<12>	AK25 PEX_RX12	PEX_TX12 AJ25	PEG_D2R_C_P<12>	C8079 0.1uF	PEG_D2R_P<12>
PEG_R2D_C_N<12>	C8045 0.1uF	PEG_R2D_N<12>	AK26 PEX_RX12_L	PEX_TX12_L AH25	PEG_D2R_C_N<12>	C8080 0.1uF	PEG_D2R_N<12>
PEG_R2D_C_P<13>	C8046 0.1uF	PEG_R2D_P<13>	AL26 PEX_RX13	PEX_TX13 AH26	PEG_D2R_C_P<13>	C8081 0.1uF	PEG_D2R_P<13>
PEG_R2D_C_N<13>	C8047 0.1uF	PEG_R2D_N<13>	AL27 PEX_RX13_L	PEX_TX13_L AG26	PEG_D2R_C_N<13>	C8082 0.1uF	PEG_D2R_N<13>
PEG_R2D_C_P<14>	C8048 0.1uF	PEG_R2D_P<14>	AM27 PEX_RX14	PEX_TX14 AK27	PEG_D2R_C_P<14>	C8083 0.1uF	PEG_D2R_P<14>
PEG_R2D_C_N<14>	C8049 0.1uF	PEG_R2D_N<14>	AM28 PEX_RX14_L	PEX_TX14_L AJ27	PEG_D2R_C_N<14>	C8084 0.1uF	PEG_D2R_N<14>
PEG_R2D_C_P<15>	C8050 0.1uF	PEG_R2D_P<15>	AL28 PEX_RX15	PEX_TX15 AJ28	PEG_D2R_C_P<15>	C8085 0.1uF	PEG_D2R_P<15>
PEG_R2D_C_N<15>	C8051 0.1uF	PEG_R2D_N<15>	AL29 PEX_RX15_L	PEX_TX15_L AH27	PEG_D2R_C_N<15>	C8086 0.1uF	PEG_D2R_N<15>

All 0.1uF capacitors: 10% 16V X5R 402

PEG_CLK100M_GPU_P	AH14 PEX_REFCLK	PEX_TSTCLK_OUT AM12	TP_GPU_PEXTSTCLK_P
PEG_CLK100M_GPU_N	AJ14 PEX_REFCLK_L	PEX_TSTCLK_OUT_L AM11	TP_GPU_PEXTSTCLK_N
GPU_RESET_L	AH15 PEX_RST_L		

NV G84M PCI-E

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 80 OF 109	

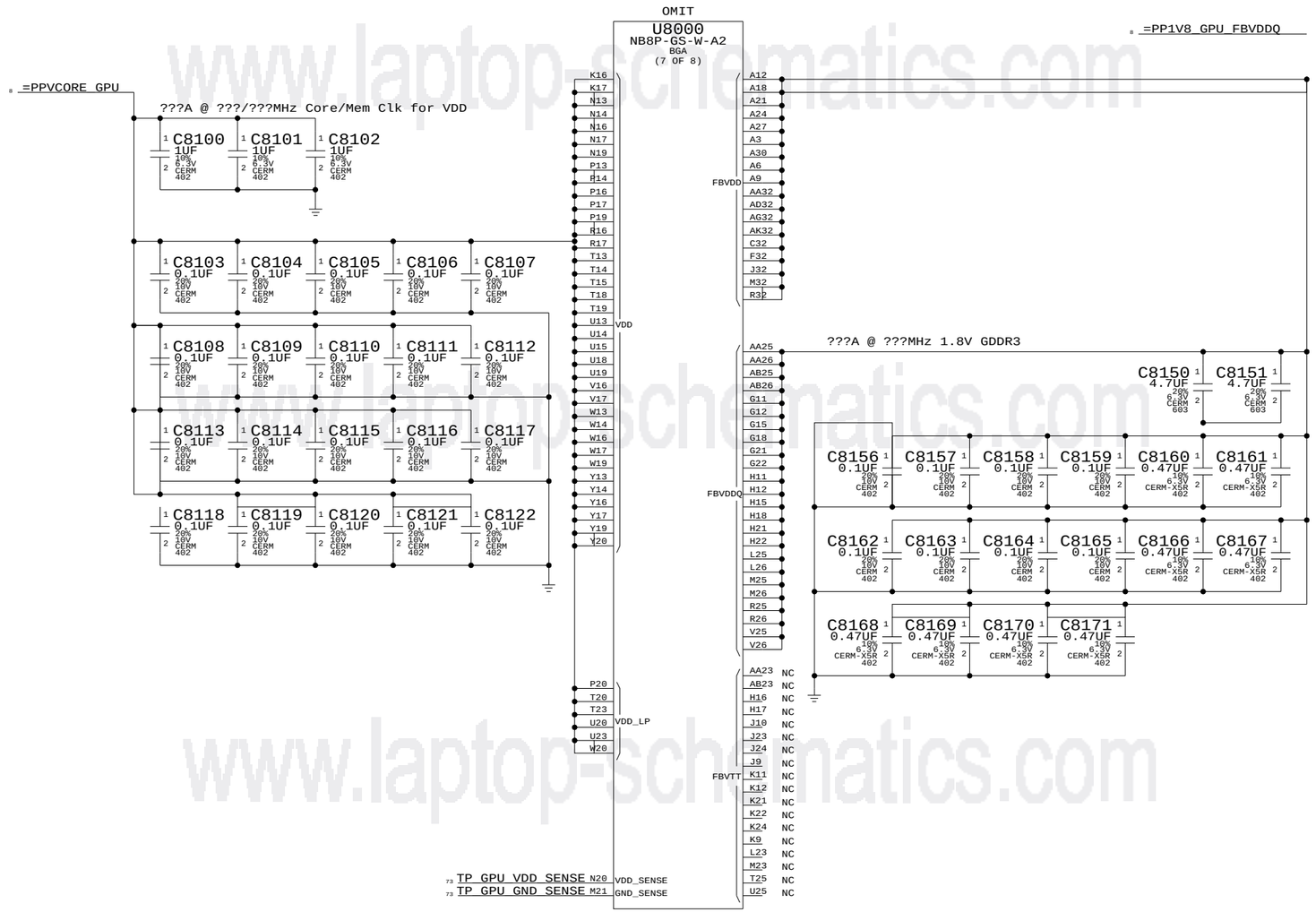
www.laptop-schematics.com

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



www.laptop-schematics.com

NV G84M Core/FB Power

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 81 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8000
NB8P-GS-W-A2
BGA
(3 OF 8)

MEMORY INTERFACE A

FB_A_DQ<0> N27 FBAD0
FB_A_DQ<1> M27 FBAD1
FB_A_DQ<2> N28 FBAD2
FB_A_DQ<3> L29 FBAD3
FB_A_DQ<4> K27 FBAD4
FB_A_DQ<5> K28 FBAD5
FB_A_DQ<6> J29 FBAD6
FB_A_DQ<7> J28 FBAD7
FB_A_DQ<8> P30 FBAD8
FB_A_DQ<9> N31 FBAD9
FB_A_DQ<10> N30 FBAD10
FB_A_DQ<11> N32 FBAD11
FB_A_DQ<12> L31 FBAD12
FB_A_DQ<13> L30 FBAD13
FB_A_DQ<14> J30 FBAD14
FB_A_DQ<15> L32 FBAD15
FB_A_DQ<16> H30 FBAD16
FB_A_DQ<17> K30 FBAD17
FB_A_DQ<18> H31 FBAD18
FB_A_DQ<19> F30 FBAD19
FB_A_DQ<20> H32 FBAD20
FB_A_DQ<21> E31 FBAD21
FB_A_DQ<22> D30 FBAD22
FB_A_DQ<23> E30 FBAD23
FB_A_DQ<24> H28 FBAD24
FB_A_DQ<25> H29 FBAD25
FB_A_DQ<26> E29 FBAD26
FB_A_DQ<27> J27 FBAD27
FB_A_DQ<28> F27 FBAD28
FB_A_DQ<29> E27 FBAD29
FB_A_DQ<30> E28 FBAD30
FB_A_DQ<31> F28 FBAD31
FB_A_DQ<32> AD29 FBAD32
FB_A_DQ<33> AE29 FBAD33
FB_A_DQ<34> AD28 FBAD34
FB_A_DQ<35> AC28 FBAD35
FB_A_DQ<36> AB29 FBAD36
FB_A_DQ<37> AA30 FBAD37
FB_A_DQ<38> Y28 FBAD38
FB_A_DQ<39> AB30 FBAD39
FB_A_DQ<40> AM30 FBAD40
FB_A_DQ<41> AF30 FBAD41
FB_A_DQ<42> AJ31 FBAD42
FB_A_DQ<43> AJ30 FBAD43
FB_A_DQ<44> AJ32 FBAD44
FB_A_DQ<45> AK29 FBAD45
FB_A_DQ<46> AM31 FBAD46
FB_A_DQ<47> AL30 FBAD47
FB_A_DQ<48> AE32 FBAD48
FB_A_DQ<49> AE30 FBAD49
FB_A_DQ<50> AE31 FBAD50
FB_A_DQ<51> AD30 FBAD51
FB_A_DQ<52> AC31 FBAD52
FB_A_DQ<53> AC32 FBAD53
FB_A_DQ<54> AB32 FBAD54
FB_A_DQ<55> AB31 FBAD55
FB_A_DQ<56> AG27 FBAD56
FB_A_DQ<57> AF28 FBAD57
FB_A_DQ<58> AH28 FBAD58
FB_A_DQ<59> AG28 FBAD59
FB_A_DQ<60> AG29 FBAD60
FB_A_DQ<61> AD27 FBAD61
FB_A_DQ<62> AF27 FBAD62
FB_A_DQ<63> AE28 FBAD63

FBA_CMD0 P32 FB_A_LMA<4>
FBA_CMD1 U27 FB_A_RAS_L
FBA_CMD2 P31 FB_A_LMA<5>
FBA_CMD3 U30 FB_A_BA<1>
FBA_CMD4 Y31 FB_A_UMA<2>
FBA_CMD5 W32 FB_A_UMA<4>
FBA_CMD6 W31 FB_A_UMA<3>
FBA_CMD7 T32 FB_A_CS1_L
FBA_CMD8 V27 FB_A_CS0_L
FBA_CMD9 T28 FB_A_MA<11>
FBA_CMD10 T31 FB_A_CAS_L
FBA_CMD11 U32 FB_A_WE_L
FBA_CMD12 W29 FB_A_BA<0>
FBA_CMD13 W30 FB_A_UMA<5>
FBA_CMD14 T27 FB_A_MA<12>
FBA_CMD15 V28 FB_A_DRAM_RST
FBA_CMD16 V30 FB_A_MA<7>
FBA_CMD17 U31 FB_A_MA<10>
FBA_CMD18 R27 FB_A_CKE
FBA_CMD19 V29 FB_A_MA<0>
FBA_CMD20 T30 FB_A_MA<9>
FBA_CMD21 W28 FB_A_MA<6>
FBA_CMD22 R29 FB_A_LMA<2>
FBA_CMD23 R30 FB_A_MA<8>
FBA_CMD24 P29 FB_A_LMA<3>
FBA_CMD25 U28 FB_A_MA<1>
FBA_CMD26 Y32 FB_A_MA<13>
FBA_CMD27 Y30 FB_A_BA<2>
FBA_CMD28 V32 TP_FBA_CMD28

FBA_CLK0 P28 FB_A_CLK_P<0>
FBA_CLK0_L R28 FB_A_CLK_N<0>
FBA_CLK1 Y27 FB_A_CLK_P<1>
FBA_CLK1_L AA27 FB_A_CLK_N<1>

FBADQM0 M29 FB_A_DQM_L<0>
FBADQM1 M30 FB_A_DQM_L<1>
FBADQM2 G30 FB_A_DQM_L<2>
FBADQM3 F29 FB_A_DQM_L<3>
FBADQM4 AA29 FB_A_DQM_L<4>
FBADQM5 AK30 FB_A_DQM_L<5>
FBADQM6 AC30 FB_A_DQM_L<6>
FBADQM7 AG30 FB_A_DQM_L<7>

READ STROBE
FBADQS_RN0 M28 FB_A_RDQS<0>
FBADQS_RN1 K32 FB_A_RDQS<1>
FBADQS_RN2 G31 FB_A_RDQS<2>
FBADQS_RN3 G27 FB_A_RDQS<3>
FBADQS_RN4 AA28 FB_A_RDQS<4>
FBADQS_RN5 AL31 FB_A_RDQS<5>
FBADQS_RN6 AF31 FB_A_RDQS<6>
FBADQS_RN7 AH29 FB_A_RDQS<7>

WRITE STROBE
FBADQS_WP0 L28 FB_A_WDQS<0>
FBADQS_WP1 K31 FB_A_WDQS<1>
FBADQS_WP2 G32 FB_A_WDQS<2>
FBADQS_WP3 G28 FB_A_WDQS<3>
FBADQS_WP4 AB28 FB_A_WDQS<4>
FBADQS_WP5 AL32 FB_A_WDQS<5>
FBADQS_WP6 AF32 FB_A_WDQS<6>
FBADQS_WP7 AH30 FB_A_WDQS<7>

=PP1V8_GPU_FBIO
FBA_DEBUG AC27 TP_FBA_DEBUG

FBCAL_PD_VDDQ K26 FBCAL_PD_VDDQ
FBCAL_PU_GND H26 FBCAL_PU_GND

R8200 10K 5% 1/16W MF-LF 402
R8201 10K 5% 1/16W MF-LF 402
R8290 45.3 1% 1/16W MF-LF 402
R8291 24.9 1% 1/16W MF-LF 402

PP1V2_GPU_FBA_PLL_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V
FBA_PLLAVDD G25
FBA_PLLGND G24

=PP1V2_GPU_FBPLLAVDD
L8200 FERR-220-OHM 0402
C8201 0.1UF 20% 10V CERM 402
C8200 4.7UF 20% 6.3V CERM 603

OMIT
U8000
NB8P-GS-W-A2
BGA
(4 OF 8)

MEMORY INTERFACE B

FB_B_DQ<0> B7 FBCD0
FB_B_DQ<1> A7 FBCD1
FB_B_DQ<2> C7 FBCD2
FB_B_DQ<3> A2 FBCD3
FB_B_DQ<4> B2 FBCD4
FB_B_DQ<5> C4 FBCD5
FB_B_DQ<6> A5 FBCD6
FB_B_DQ<7> B5 FBCD7
FB_B_DQ<8> F9 FBCD8
FB_B_DQ<9> F10 FBCD9
FB_B_DQ<10> D12 FBCD10
FB_B_DQ<11> D9 FBCD11
FB_B_DQ<12> E12 FBCD12
FB_B_DQ<13> D11 FBCD13
FB_B_DQ<14> E8 FBCD14
FB_B_DQ<15> D8 FBCD15
FB_B_DQ<16> E7 FBCD16
FB_B_DQ<17> F7 FBCD17
FB_B_DQ<18> D6 FBCD18
FB_B_DQ<19> D5 FBCD19
FB_B_DQ<20> D3 FBCD20
FB_B_DQ<21> E4 FBCD21
FB_B_DQ<22> C3 FBCD22
FB_B_DQ<23> B4 FBCD23
FB_B_DQ<24> C10 FBCD24
FB_B_DQ<25> B10 FBCD25
FB_B_DQ<26> C8 FBCD26
FB_B_DQ<27> A10 FBCD27
FB_B_DQ<28> C11 FBCD28
FB_B_DQ<29> C12 FBCD29
FB_B_DQ<30> A11 FBCD30
FB_B_DQ<31> B11 FBCD31
FB_B_DQ<32> B28 FBCD32
FB_B_DQ<33> C27 FBCD33
FB_B_DQ<34> C26 FBCD34
FB_B_DQ<35> B26 FBCD35
FB_B_DQ<36> C30 FBCD36
FB_B_DQ<37> B31 FBCD37
FB_B_DQ<38> C29 FBCD38
FB_B_DQ<39> A31 FBCD39
FB_B_DQ<40> D28 FBCD40
FB_B_DQ<41> D27 FBCD41
FB_B_DQ<42> F26 FBCD42
FB_B_DQ<43> D24 FBCD43
FB_B_DQ<44> E23 FBCD44
FB_B_DQ<45> E26 FBCD45
FB_B_DQ<46> E24 FBCD46
FB_B_DQ<47> F23 FBCD47
FB_B_DQ<48> B23 FBCD48
FB_B_DQ<49> A23 FBCD49
FB_B_DQ<50> C25 FBCD50
FB_B_DQ<51> C23 FBCD51
FB_B_DQ<52> A22 FBCD52
FB_B_DQ<53> C22 FBCD53
FB_B_DQ<54> C21 FBCD54
FB_B_DQ<55> B22 FBCD55
FB_B_DQ<56> E22 FBCD56
FB_B_DQ<57> D22 FBCD57
FB_B_DQ<58> D21 FBCD58
FB_B_DQ<59> E21 FBCD59
FB_B_DQ<60> E18 FBCD60
FB_B_DQ<61> D19 FBCD61
FB_B_DQ<62> D18 FBCD62
FB_B_DQ<63> E19 FBCD63

NC G10 FBC_PLLAVDD
NC G9 FBC_PLLGND

FBC_CMD0 C13 FB_B_LMA<4>
FBC_CMD1 A16 FB_B_RAS_L
FBC_CMD2 A13 FB_B_LMA<5>
FBC_CMD3 B17 FB_B_BA<1>
FBC_CMD4 B20 FB_B_UMA<2>
FBC_CMD5 A19 FB_B_UMA<4>
FBC_CMD6 B19 FB_B_UMA<3>
FBC_CMD7 B14 FB_B_CS1_L
FBC_CMD8 E16 FB_B_CS0_L
FBC_CMD9 A14 FB_B_MA<11>
FBC_CMD10 C15 FB_B_CAS_L
FBC_CMD11 B16 FB_B_WE_L
FBC_CMD12 F17 FB_B_BA<0>
FBC_CMD13 C19 FB_B_UMA<5>
FBC_CMD14 D15 FB_B_MA<12>
FBC_CMD15 C17 FB_B_DRAM_RST
FBC_CMD16 A17 FB_B_MA<7>
FBC_CMD17 C16 FB_B_MA<10>
FBC_CMD18 D14 FB_B_CKE
FBC_CMD19 F16 FB_B_MA<0>
FBC_CMD20 C14 FB_B_MA<9>
FBC_CMD21 C18 FB_B_MA<6>
FBC_CMD22 E14 FB_B_LMA<2>
FBC_CMD23 B13 FB_B_MA<8>
FBC_CMD24 E15 FB_B_LMA<3>
FBC_CMD25 F15 FB_B_MA<1>
FBC_CMD26 A20 FB_B_MA<13>
FBC_CMD27 C20 FB_B_BA<2>
FBC_CMD28 A15 TP_FBC_CMD28

FBC_CLK0 E13 FB_B_CLK_P<0>
FBC_CLK0_L F13 FB_B_CLK_N<0>
FBC_CLK1 F18 FB_B_CLK_P<1>
FBC_CLK1_L E17 FB_B_CLK_N<1>

FBCDQM0 A4 FB_B_DQM_L<0>
FBCDQM1 E11 FB_B_DQM_L<1>
FBCDQM2 F5 FB_B_DQM_L<2>
FBCDQM3 C9 FB_B_DQM_L<3>
FBCDQM4 C28 FB_B_DQM_L<4>
FBCDQM5 F24 FB_B_DQM_L<5>
FBCDQM6 C24 FB_B_DQM_L<6>
FBCDQM7 E20 FB_B_DQM_L<7>

READ STROBE
FBCDQS_RN0 C6 FB_B_RDQS<0>
FBCDQS_RN1 E9 FB_B_RDQS<1>
FBCDQS_RN2 E6 FB_B_RDQS<2>
FBCDQS_RN3 A8 FB_B_RDQS<3>
FBCDQS_RN4 B29 FB_B_RDQS<4>
FBCDQS_RN5 E25 FB_B_RDQS<5>
FBCDQS_RN6 A25 FB_B_RDQS<6>
FBCDQS_RN7 F21 FB_B_RDQS<7>

WRITE STROBE
FBCDQS_WP0 C5 FB_B_WDQS<0>
FBCDQS_WP1 E10 FB_B_WDQS<1>
FBCDQS_WP2 E5 FB_B_WDQS<2>
FBCDQS_WP3 B8 FB_B_WDQS<3>
FBCDQS_WP4 A29 FB_B_WDQS<4>
FBCDQS_WP5 D25 FB_B_WDQS<5>
FBCDQS_WP6 B25 FB_B_WDQS<6>
FBCDQS_WP7 F20 FB_B_WDQS<7>

FBC_DEBUG F12 TP_FBC_DEBUG

FBCAL_TERM_GND J26 FBCAL_TERM_GND
FB_VREF E32 GPU_FB_VREF

R8250 10K 5% 1/16W MF-LF 402
R8251 10K 5% 1/16W MF-LF 402
R8292 40.2 1% 1/16W MF-LF 402
R8295 1.07K 1% 1/16W MF-LF 402
R8297 1.02K 1% 1/16W MF-LF 402
R8296 2.49K 1% 1/16W MF-LF 402
C8296 0.1uF 10% 16V X5R 402

=PP1V8_GPU_FBIO

GPU_FB_VREF_UNTERM_L
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

Q8295 SSM6N15FE SOT563
FB_VREF_UNTERM

NV G84M Frame Buffer I/F

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE	SHT	OF
NONE	82	109

www.laptop-schematics.com

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_GPU_FB_VDD

=PP1V8_GPU_FB_VDDQ

CRITICAL
OMIT

U8400
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

U8450
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

Connect to designated pin, then GND

C8400 C8401 C8402 C8403 C8404 C8410 C8415
C8450 C8451 C8452 C8453 C8454 C8460 C8465
10UF 20% 6.3V X5R 603
0.1uF 10% 16V X5R 402

C8420 C8421 C8422 C8423 C8424 C8425 C8426
C8470 C8471 C8472 C8473 C8474 C8475 C8476
10UF 20% 6.3V X5R 603
0.1uF 10% 16V X5R 402

R8430 R8433 2.37K 1% 1/16W MF-LF 402
R8480 R8483 2.37K 1% 1/16W MF-LF 402

R8431 R8434 5.49K 1% 1/16W MF-LF 402
R8481 R8484 5.49K 1% 1/16W MF-LF 402

R8432 R8435 2.21K 1% 1/16W MF-LF 402
R8482 R8485 2.21K 1% 1/16W MF-LF 402

C8431 C8432 0.01UF 10% 16V CERM 402
C8481 C8482 0.01UF 10% 16V CERM 402

FB_A0_VREF
FB_A2_VREF
FB_A2_VREF_UNTERM_L
FB_A0_VREF_UNTERM_L

FB_A1_VREF
FB_A3_VREF
FB_A3_VREF_UNTERM_L
FB_A1_VREF_UNTERM_L

FB_A_CLK0_TERM
VOLTAGE=0.9V
C8446 0.01UF 10% 16V CERM 402
FB_VREF_UNTERM

FB_A_CLK1_TERM
VOLTAGE=0.9V
C8496 0.01UF 10% 16V CERM 402
FB_VREF_UNTERM

R8440 1K 5% 1/16W MF-LF 402
R8442 121 1% 1/16W MF-LF 402
R8444 121 1% 1/16W MF-LF 402
R8446 121 1% 1/16W MF-LF 402
R8447 121 1% 1/16W MF-LF 402
R8443 121 1% 1/16W MF-LF 402
R8445 121 1% 1/16W MF-LF 402

R8490 1K 5% 1/16W MF-LF 402
R8492 121 1% 1/16W MF-LF 402
R8494 121 1% 1/16W MF-LF 402
R8496 121 1% 1/16W MF-LF 402
R8497 121 1% 1/16W MF-LF 402
R8493 121 1% 1/16W MF-LF 402
R8495 121 1% 1/16W MF-LF 402

Q8400 SSM6N15FE SOT563
Q8450 SSM6N15FE SOT563

MFHIGH
MFLOW

FB_A_MA<0>
FB_A_MA<1>
FB_A_LMA<2>
FB_A_LMA<3>
FB_A_LMA<4>
FB_A_LMA<5>
FB_A_MA<6>
FB_A_MA<7>
FB_A_MA<8>
FB_A_MA<9>
FB_A_MA<10>
FB_A_MA<11>
FB_A_CKE
FB_A_CLK_P<0>
FB_A_CLK_N<0>
FB_A_CS0_L
FB_A_WE_L
FB_A_CAS_L
FB_A_RAS_L

FB_A0_ZQ
FB_A0_MF
FB_A0_SEN

FB_A_DRAM_RST

FB_A_RDQS<0>
FB_A_RDQS<1>
FB_A_RDQS<2>
FB_A_RDQS<3>

FB_A_WDQS<0>
FB_A_WDQS<1>
FB_A_WDQS<2>
FB_A_WDQS<3>

FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>

FB_A_MA<12>
FB_A_CS1_L
(For 32Mx32 support)

R8448 243 1% 1/16W MF-LF 402
R8449 100 5% 1/16W MF-LF 402

FB_A_DQM_L<0>
FB_A_DQM_L<1>
FB_A_DQM_L<2>
FB_A_DQM_L<3>

FB_A_DQ<0>
FB_A_DQ<1>
FB_A_DQ<2>
FB_A_DQ<3>
FB_A_DQ<4>
FB_A_DQ<5>
FB_A_DQ<6>
FB_A_DQ<7>
FB_A_DQ<8>
FB_A_DQ<9>
FB_A_DQ<10>
FB_A_DQ<11>
FB_A_DQ<12>
FB_A_DQ<13>
FB_A_DQ<14>
FB_A_DQ<15>
FB_A_DQ<16>
FB_A_DQ<17>
FB_A_DQ<18>
FB_A_DQ<19>
FB_A_DQ<20>
FB_A_DQ<21>
FB_A_DQ<22>
FB_A_DQ<23>
FB_A_DQ<24>
FB_A_DQ<25>
FB_A_DQ<26>
FB_A_DQ<27>
FB_A_DQ<28>
FB_A_DQ<29>
FB_A_DQ<30>
FB_A_DQ<31>

FB_A_DQM_L<7>
FB_A_DQM_L<5>
FB_A_DQM_L<6>
FB_A_DQM_L<4>

FB_A_DQ<62>
FB_A_DQ<56>
FB_A_DQ<58>
FB_A_DQ<59>
FB_A_DQ<57>
FB_A_DQ<63>
FB_A_DQ<60>
FB_A_DQ<61>
FB_A_DQ<40>
FB_A_DQ<47>
FB_A_DQ<46>
FB_A_DQ<45>
FB_A_DQ<42>
FB_A_DQ<44>
FB_A_DQ<41>
FB_A_DQ<43>
FB_A_DQ<50>
FB_A_DQ<48>
FB_A_DQ<52>
FB_A_DQ<51>
FB_A_DQ<55>
FB_A_DQ<49>
FB_A_DQ<54>
FB_A_DQ<53>
FB_A_DQ<34>
FB_A_DQ<33>
FB_A_DQ<35>
FB_A_DQ<32>
FB_A_DQ<36>
FB_A_DQ<37>
FB_A_DQ<39>
FB_A_DQ<38>

www.laptop-schematics.com

GDDR3 Frame Buffer A (Top)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 84 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_GPU_FB_VDD

=PP1V8_GPU_FB_VDDQ

CRITICAL
OMIT

U8500
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

C8500 10UF 20% 6.3V X5R 603
C8501 C8502 C8503 C8504 0.1UF 10% 16V X5R 402
C8510 C8515 0.1UF 10% 16V X5R 402

Connect to designated pin, then GND

U8500.J1
U8500.J12

C8520 10UF 20% 6.3V X5R 603
C8521 C8522 C8523 C8524 C8525 C8526 0.1UF 10% 16V X5R 402

R8530 2.37K 1% 1/16W MF-LF 402
R8533 2.37K 1% 1/16W MF-LF 402

FB_B0_VREF
FB_B2_VREF

R8531 5.49K 1% 1/16W MF-LF 402
R8532 2.21K 1% 1/16W MF-LF 402
C8531 0.01UF 10% 16V CERM 402
R8534 5.49K 1% 1/16W MF-LF 402
R8535 2.21K 1% 1/16W MF-LF 402
C8532 0.01UF 10% 16V CERM 402

FB_B2_VREF_UNTERM_L
FB_B0_VREF_UNTERM_L

FB_B_CLK0_TERM
VOLTAGE=0.9V

C8546 0.01UF 10% 16V CERM 402

FB_VREF_UNTERM

Q8500 SSM6N15FE SOT563

VRAM4
R8540 1K 5% 1/16W MF-LF 402
R8542 121 1% 1/16W MF-LF 402
R8544 121 1% 1/16W MF-LF 402
R8546 121 1% 1/16W MF-LF 402
R8547 121 1% 1/16W MF-LF 402
R8543 121 1% 1/16W MF-LF 402
R8545 121 1% 1/16W MF-LF 402

FB_B_MA<0>
FB_B_MA<1>
FB_B_LMA<2>
FB_B_LMA<3>
FB_B_LMA<4>
FB_B_LMA<5>
FB_B_MA<6>
FB_B_MA<7>
FB_B_MA<8>
FB_B_MA<9>
FB_B_MA<10>
FB_B_MA<11>
FB_B_CKE
FB_B_CLK_P<0>
FB_B_CLK_N<0>
FB_B_CS0_L
FB_B_WE_L
FB_B_CAS_L
FB_B_RAS_L
FB_B_DRAM_RST
FB_B_RDQS<2>
FB_B_RDQS<1>
FB_B_RDQS<3>
FB_B_RDQS<0>
FB_B_WDQS<2>
FB_B_WDQS<1>
FB_B_WDQS<3>
FB_B_WDQS<0>
FB_B_BA<0>
FB_B_BA<1>
FB_B_BA<2>
FB_B_MA<12>
FB_B_CS1_L
(For 32Mx32 support)

FB_B_DQM_L<2>
FB_B_DQM_L<1>
FB_B_DQM_L<3>
FB_B_DQM_L<0>

FB_B_DQ<18>
FB_B_DQ<17>
FB_B_DQ<19>
FB_B_DQ<16>
FB_B_DQ<21>
FB_B_DQ<23>
FB_B_DQ<20>
FB_B_DQ<22>
FB_B_DQ<8>
FB_B_DQ<12>
FB_B_DQ<9>
FB_B_DQ<10>
FB_B_DQ<13>
FB_B_DQ<14>
FB_B_DQ<15>
FB_B_DQ<11>
FB_B_DQ<24>
FB_B_DQ<28>
FB_B_DQ<29>
FB_B_DQ<31>
FB_B_DQ<30>
FB_B_DQ<25>
FB_B_DQ<26>
FB_B_DQ<27>
FB_B_DQ<2>
FB_B_DQ<1>
FB_B_DQ<6>
FB_B_DQ<0>
FB_B_DQ<7>
FB_B_DQ<4>
FB_B_DQ<5>
FB_B_DQ<3>

FB_B0_ZQ
FB_B0_MF
FB_B0_SEN

R8548 243 1% 1/16W MF-LF 402
R8549 100 5% 1/16W MF-LF 402

C8550 10UF 20% 6.3V X5R 603
C8551 C8552 C8553 C8554 0.1UF 10% 16V X5R 402
C8560 C8565 0.1UF 10% 16V X5R 402

C8570 10UF 20% 6.3V X5R 603
C8571 C8572 C8573 C8574 C8575 C8576 0.1UF 10% 16V X5R 402

R8580 2.37K 1% 1/16W MF-LF 402
R8583 2.37K 1% 1/16W MF-LF 402

FB_B1_VREF
FB_B3_VREF

R8581 5.49K 1% 1/16W MF-LF 402
R8582 2.21K 1% 1/16W MF-LF 402
C8581 0.01UF 10% 16V CERM 402
R8584 5.49K 1% 1/16W MF-LF 402
R8585 2.21K 1% 1/16W MF-LF 402
C8582 0.01UF 10% 16V CERM 402

FB_B3_VREF_UNTERM_L
FB_B1_VREF_UNTERM_L

FB_B_CLK1_TERM
VOLTAGE=0.9V

C8596 0.01UF 10% 16V CERM 402

R8590 R8592 R8594 R8596 121 1% 1/16W MF-LF 402
R8593 R8595 R8597 121 1% 1/16W MF-LF 402

FB_B_MA<0>
FB_B_MA<1>
FB_B_UMA<2>
FB_B_UMA<3>
FB_B_UMA<4>
FB_B_UMA<5>
FB_B_MA<6>
FB_B_MA<7>
FB_B_MA<8>
FB_B_MA<9>
FB_B_MA<10>
FB_B_MA<11>
FB_B_CKE
FB_B_CLK_P<1>
FB_B_CLK_N<1>
FB_B_CS0_L
FB_B_WE_L
FB_B_CAS_L
FB_B_RAS_L
FB_B_DRAM_RST
FB_B_RDQS<6>
FB_B_RDQS<5>
FB_B_RDQS<4>
FB_B_RDQS<7>
FB_B_WDQS<6>
FB_B_WDQS<5>
FB_B_WDQS<4>
FB_B_WDQS<7>
FB_B_BA<0>
FB_B_BA<1>
FB_B_BA<2>
FB_B_MA<12>
FB_B_CS1_L
(For 32Mx32 support)

FB_B_DQM_L<6>
FB_B_DQM_L<5>
FB_B_DQM_L<4>
FB_B_DQM_L<7>

FB_B_DQ<49>
FB_B_DQ<50>
FB_B_DQ<48>
FB_B_DQ<51>
FB_B_DQ<52>
FB_B_DQ<55>
FB_B_DQ<54>
FB_B_DQ<53>
FB_B_DQ<40>
FB_B_DQ<42>
FB_B_DQ<41>
FB_B_DQ<45>
FB_B_DQ<43>
FB_B_DQ<46>
FB_B_DQ<47>
FB_B_DQ<44>
FB_B_DQ<36>
FB_B_DQ<39>
FB_B_DQ<37>
FB_B_DQ<38>
FB_B_DQ<34>
FB_B_DQ<32>
FB_B_DQ<35>
FB_B_DQ<33>
FB_B_DQ<63>
FB_B_DQ<58>
FB_B_DQ<61>
FB_B_DQ<59>
FB_B_DQ<62>
FB_B_DQ<56>
FB_B_DQ<60>
FB_B_DQ<57>

FB_B1_ZQ
FB_B1_MF
FB_B1_SEN

R8598 243 1% 1/16W MF-LF 402
R8599 100 5% 1/16W MF-LF 402

www.laptop-schematics.com

GDDR3 Frame Buffer B (Top)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

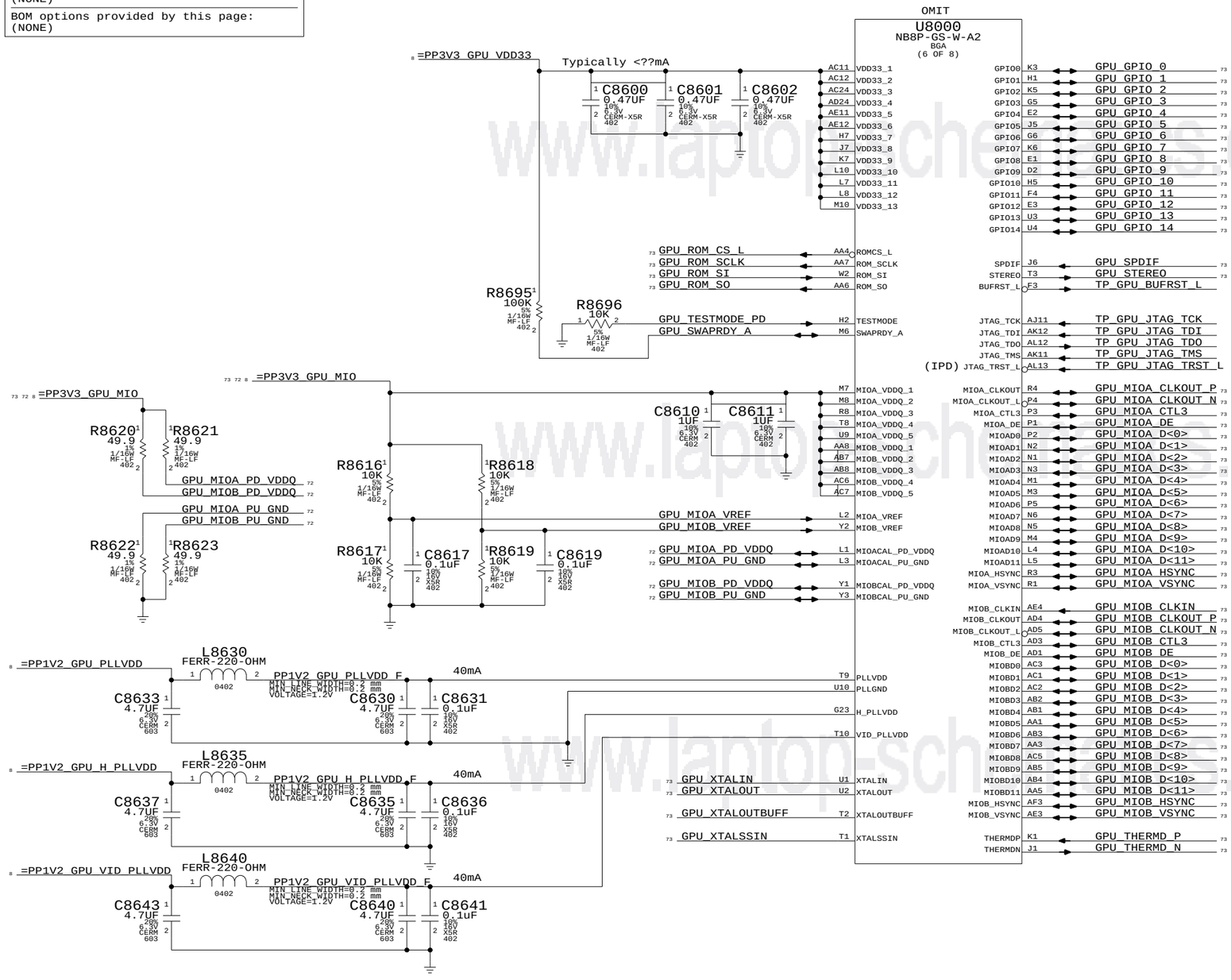
SCALE	SHT	OF
NONE	85	109

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



www.laptop-schematics.com

NV G84M GPIO/MIO/Misc

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 86 OF 109	

GPIOs

	Native Func			
GPU_GPIO_0	HPD0	=	GPU_HPD	IN
GPU_GPIO_1	HPD1	=	NC_GPU_GPIO_1	
GPU_GPIO_2	LCD0_BL_PWM	=	GPU_BL_PWM	OUT
GPU_GPIO_3	LCD0_VDD	=	GPU_PANEL_EN	OUT
GPU_GPIO_4	LCD0_BL_EN	=	GPU_BKLT_EN	OUT
GPU_GPIO_5	VID0	=	TP_GPU_GSTATE<0>	
GPU_GPIO_6	VID1	=	TP_GPU_GSTATE<1>	
GPU_GPIO_7	MEM_VID	=	GPU_VGA_EN_L	
GPU_GPIO_8	THERM	=	NC_GPU_GPIO_8	
GPU_GPIO_9	FAN_PWM	=	NC_GPU_GPIO_9	
GPU_GPIO_10	MEM_VREF	=	FB_VREF_UNTERM	OUT
GPU_GPIO_11	SLI_SYNC	=	GPU_VCORE_VID0	OUT
GPU_GPIO_12	AC_DET	=	GPU_VCORE_VID1	OUT
GPU_GPIO_13	PWR_CTL0	=	GPU_VCORE_VID2	OUT
GPU_GPIO_14	PWR_CTL1	=	GPU_VCORE_VID3	OUT

Renamed signals

GPU_CLK27M	=	GPU_XTALIN
GPU_CLK27M_SS	=	GPU_XTALSSIN
GPU_TDIODE_P	=	GPU_THERMD_P
GPU_TDIODE_N	=	GPU_THERMD_N
GPU_DVI_DDC_CLK	=	GPU_I2CB_SCL
GPU_DVI_DDC_DATA	=	GPU_I2CB_SDA
GPU_PANEL_DDC_CLK	=	GPU_I2CC_SCL
GPU_PANEL_DDC_DATA	=	GPU_I2CC_SDA
GPU_VDD_SENSE	=	TP_GPU_VDD_SENSE
GPU_GND_SENSE	=	TP_GPU_GND_SENSE

Unused I2C Buses

NC_GPU_I2CA_SCL	=	GPU_I2CA_SCL
NC_GPU_I2CA_SDA	=	GPU_I2CA_SDA

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

Unused signals

NC_GPU_XTALOUT	=	GPU_XTALOUT
NC_GPU_SPDIF	=	GPU_SPDIF
NC_GPU_STEREO	=	GPU_STEREO
NC_FBA_MA<13>	=	FB_A_MA<13>
NC_FBB_MA<13>	=	FB_B_MA<13>
NC_FBA_CMD28	=	TP_FBA_CMD28
NC_FBC_CMD28	=	TP_FBC_CMD28
NC_GPU_ROM_CS_L	=	GPU_ROM_CS_L
NC_GPU_ROM_SCLK	=	GPU_ROM_SCLK
NC_GPU_ROM_SI	=	GPU_ROM_SI
NC_GPU_ROM_SO	=	GPU_ROM_SO
NC_GPU_CSYNC	=	GPU_CSYNC
NC_GPU_R2	=	GPU_R2
NC_GPU_G2	=	GPU_G2
NC_GPU_B2	=	GPU_B2
NC_GPU_H2SYNC	=	GPU_H2SYNC
NC_GPU_V2SYNC	=	GPU_V2SYNC
NC_LVDS_U_DATAP<3>	=	LVDS_U_DATA_P<3>
NC_LVDS_U_DATAN<3>	=	LVDS_U_DATA_N<3>
NC_LVDS_L_DATAP<3>	=	LVDS_L_DATA_P<3>
NC_LVDS_L_DATAN<3>	=	LVDS_L_DATA_N<3>
TP_GPU_MIOA_CLKOUT_P	=	GPU_MIOA_CLKOUT_P
TP_GPU_MIOA_CLKOUT_N	=	GPU_MIOA_CLKOUT_N
TP_GPU_MIOA_CTL3	=	GPU_MIOA_CTL3
TP_GPU_MIOA_DE	=	GPU_MIOA_DE
TP_GPU_MIOA_D<5..2>	=	GPU_MIOA_D<5..2>
TP_GPU_MIOA_D<7>	=	GPU_MIOA_D<7>
TP_GPU_MIOA_D<11..10>	=	GPU_MIOA_D<11..10>
TP_GPU_MIOA_HSYNC	=	GPU_MIOA_HSYNC
TP_GPU_MIOA_VSYNC	=	GPU_MIOA_VSYNC
TP_GPU_MIOB_CLKIN	=	GPU_MIOB_CLKIN
TP_GPU_MIOB_CLKOUT_P	=	GPU_MIOB_CLKOUT_P
TP_GPU_MIOB_CLKOUT_N	=	GPU_MIOB_CLKOUT_N
TP_GPU_MIOB_CTL3	=	GPU_MIOB_CTL3
TP_GPU_MIOB_DE	=	GPU_MIOB_DE
TP_GPU_MIOB_D<2>	=	GPU_MIOB_D<2>
TP_GPU_MIOB_D<7..6>	=	GPU_MIOB_D<7..6>
TP_GPU_MIOB_D<10>	=	GPU_MIOB_D<10>
TP_GPU_MIOB_VSYNC	=	GPU_MIOB_VSYNC
NC_GPU_IFPD_CLK_P	=	GPU_IFPD_CLK_P
NC_GPU_IFPD_CLK_N	=	GPU_IFPD_CLK_N

Config Straps

=PP3V3_GPU_MIO

VRAM_SAMSUNG	VRAM_8M	VRAM8	NO STUFF	NO STUFF	NO STUFF	NO STUFF		
R8720	R8722	R8724	R8726	R8728	R8729	R8730	R8731	R8732
10K	10K	10K	10K	2.2K	2.2K	2.2K	2.2K	2.2K

Supported straps:	
RAMCFG0	GPU_MIOB_D<0>
RAMCFG1	GPU_MIOB_D<1>
RAMCFG2	GPU_MIOB_D<8>
RAMCFG3	GPU_MIOB_D<9>
3GIO_PADCFG0	GPU_MIOA_D<6>
3GIO_PADCFG1	GPU_MIOA_D<8>
3GIO_PADCFG2	GPU_MIOA_D<9>
3GIO_PADCFG3	GPU_MIOB_HSYNC
PEX_PLL_EN_TERM	GPU_MIOA_D<0>
SUBVENDOR (BIOS ROM PRESENT)	GPU_MIOA_D<1>
PCI_DEVID<3..0>	

VRAM_HYNIX	NO STUFF	VRAM_16M	VRAM4	
R8721	R8723	R8725	R8727	R8733
10K	10K	10K	10K	2.2K

Straps not supported:	
USER<3..0>	MIOA_D<5..2>
ROMTYPE<1..0>	MIOB_VSYNC, MIOB_D<10>
SLOT_CLOCK_CFG	MIOA_HSYNC
PCI_IOBAR	MIOB_D<7>
BAR2_SIZE	MIOB_DE
PCI_DEVID<4>	MIOB_CTL3

PCI_DEVID3
PCI_DEVID2
PCI_DEVID1
PCI_DEVID0

=PP3V3_GPU_MIO

NO STUFF: R8734 2.2K, R8735 2.2K, R8736 2.2K, R8737 2.2K

GPU_MIOB_D<11>
GPU_MIOB_D<3>
GPU_MIOB_D<5>
GPU_MIOB_D<4>

HDCP Support

=PP3V3_GPU_HDCP

HDCP R8770 10K 5% 1/16W MF-LF 402

GPU_I2CH_SCL
GPU_I2CH_SDA

HDCP R8771 10K 5% 1/16W MF-LF 402

HDCP C8770 0.1UF 20% 10V CERM 402

CRITICAL HDCP U8770 190-00001-0001 SOI

VCC			
SCL	6	NC	7
SDA	5		
NC	3		
NC	2	NC	1
GND	4		

Analog Video Mux

=PP3V3_GPU_VIDEOMUX

C8700 0.1UF 20% 10V CERM 402

CRITICAL U8700 TS3V340 QFN

S1A	2	DA	4
S2A	3	DB	7
S1B	5	DC	9
S2B	6	DD	12
S1C	11	IN	1
S2C	10	EN_L	15
S1D	14		
S2D	13		
THRML PAD	17	GND	8

GPU_VGA_R
GPU_VGA_G
GPU_VGA_B

R8740 150 1% 1/10W MF-LF 402
R8741 150 1% 1/10W MF-LF 402
R8742 150 1% 1/10W MF-LF 402

Place Rs near GPU

GPU_TV_C_VGA_R
GPU_TV_Y_VGA_G
GPU_TV_COMP_VGA_B
NC
GPU_VGA_EN_L

R8700 10K 5% 1/16W MF-LF 402

GPU_TV_C
GPU_TV_Y
GPU_TV_COMP

R8743 150 1% 1/10W MF-LF 402
R8744 150 1% 1/10W MF-LF 402
R8745 150 1% 1/10W MF-LF 402

Place Rs near GPU

TMDS Backdrive Protection

CRITICAL Q8790 SI2305DS SOT-23

=PP3V3_GPU_TMDS
=PP3V3_S0GPU_TMDS_FET

R8790 10K 5% 1/16W MF-LF 402

GPU_TMDS_PWREN_L

Q8791 SSM6N15FE SOT563

=GPUVCORE_EN

R8791 100K 5% 1/10W MF-LF 402

Unused Clocks

GPU_XTALSSIN
GPU_XTALOUTBUFF

R8780 10K 5% 1/10W MF-LF 402
R8781 10K 5% 1/10W MF-LF 402

GPU_SS_INT

GPU Straps

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE D | DRAWING NUMBER 051-7431 | REV. G

SCALE NONE | SHT 87 OF 109

www.laptop-schematics.com

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

=PP1V8_GPU_IFPX

L8800 FERR-220-OHM 0402
20mA peak per diff pair
160mA peak for all pairs
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402
Place at AF9 Place at AF8

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

L8805 FERR-220-OHM 0402
40mA peak
C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPAB_VPROBE
GPU_IFPAB_RSET

=PP3V3_GPU_IFPCD_IOVDD

L8810 FERR-220-OHM 0402
20mA peak per diff pair
200mA peak for all pairs
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402
Place at AD6 Place at AE7

PP3V3_GPU_IFPCD_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

L8815 FERR-220-OHM 0402
40mA peak
C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPCD_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPCD_VPROBE
GPU_IFPCD_RSET

Sum of peak currents: 390mA

=PP3V3_GPU_DAC

L8820 FERR-220-OHM 0402
120mA peak
C8820 4.7UF 20% 6.3V CERM 603
C8821 0.1UF 20% 10V CERM 402

L8830 FERR-220-OHM 0402
150mA peak
C8830 4.7UF 20% 6.3V CERM 603
C8831 0.1UF 20% 10V CERM 402

NO STUFF
L8840 FERR-220-OHM 0402
120mA peak
C8845 4.7UF 20% 6.3V CERM 603
NO STUFF
C8840 4.7UF 20% 6.3V CERM 603
C8841 0.1UF 20% 10V CERM 402

PP3V3_GPU_DACA_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

GPU_DACA_VREF
GPU_DACA_RSET

PP3V3_GPU_DACB_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

GPU_DACB_VREF
GPU_DACB_RSET

PP3V3_GPU_DACC_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

GPU_DACC_VREF
GPU_DACC_RSET

GPU_I2CC_SCL
GPU_I2CC_SDA
GPU_I2CH_SCL
GPU_I2CH_SDA
=GPU_I2CS_SCL
=GPU_I2CS_SDA

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

OMIT
U8000
NB8P-GS-W-A2
BGA
(5 OF 8)

AF9	IFPA_IOVDD	IFPA_TXC	AK9
AF8	IFPB_IOVDD	IFPA_TXC_L	AJ9
		IFPA_TXD0	AH6
AC9	IFPAB_PLLVDD	IFPA_TXD0_L	AJ6
AD9	IFPAB_PLLGND	IFPA_TXD1	AH8
		IFPA_TXD1_L	AH7
		IFPA_TXD2	AJ8
AM4	IFPAB_VPROBE	IFPA_TXD2_L	AK8
AL5	IFPAB_RSET	IFPA_TXD3	AJ5
		IFPA_TXD3_L	AH5
		IFPB_TXC	AK4
		IFPB_TXC_L	AL4
		IFPB_TXD4	AM6
		IFPB_TXD4_L	AM5
		IFPB_TXD5	AM7
		IFPB_TXD5_L	AL7
		IFPB_TXD6	AK6
		IFPB_TXD6_L	AK5
		IFPB_TXD7	AK7
		IFPB_TXD7_L	AL8
AD6	IFPC_IOVDD	IFPC_TXC	AM2
AE7	IFPD_IOVDD	IFPC_TXC_L	AM3
		IFPC_TXD0	AE2
AA10	IFPCD_PLLVDD	IFPC_TXD0_L	AE1
AB10	IFPCD_PLLGND	IFPC_TXD1	AF1
		IFPC_TXD1_L	AF2
		IFPC_TXD2	AG1
AK3	IFPCD_VPROBE	IFPC_TXD2_L	AH1
AH3	IFPCD_RSET		
		IFPD_TXC	AG3
		IFPD_TXC_L	AH2
		IFPD_TXD4	AK1
		IFPD_TXD4_L	AJ1
		IFPD_TXD5	AL2
		IFPD_TXD5_L	AL1
		IFPD_TXD6	AJ2
		IFPD_TXD6_L	AJ3
AD10	DACA_VDD	DACA_RED	AH11
AG9	DACA_IDUMP	DACA_GREEN	AJ12
		DACA_BLUE	AH12
AH10	DACA_VREF		
AH9	DACA_RSET	DACA_HSYNC	AF10
		DACA_VSYNC	AK10
V8	DACB_VDD	DACB_RED	R6
V7	DACB_IDUMP	DACB_GREEN	T5
		DACB_BLUE	T6
R5	DACB_VREF	DACB_CSYNC	U5
R7	DACB_RSET		
AD7	DACC_VDD	DACC_RED	AF6
AG4	DACC_IDUMP	DACC_GREEN	AG6
		DACC_BLUE	AE5
AH4	DACC_VREF		
AF5	DACC_RSET	DACC_HSYNC	AG7
		DACC_VSYNC	AG5
G2	I2CC_SCL	I2CA_SCL	K2
G1	I2CC_SDA	I2CA_SDA	J3
G3	I2CH_SCL		
H3	I2CH_SDA	I2CB_SCL	H4
C1	I2CS_SCL	I2CB_SDA	J4
B1	I2CS_SDA		

Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb

GPU_IFPAB_RSET
GPU_IFPCD_RSET
GPU_DACA_RSET
GPU_DACB_RSET
GPU_DACC_RSET

NO STUFF R8850 1K 1% 1/16W ME-LF 402
NO STUFF R8851 1K 1% 1/16W ME-LF 402
R8852 124 1% 1/16W ME-LF 402
R8853 124 1% 1/16W ME-LF 402
R8854 124 1% 1/16W ME-LF 402

GPU_DACA_VREF
GPU_DACB_VREF
GPU_DACC_VREF

C8852 0.1UF 20% 10V CERM 402
C8853 0.1UF 20% 10V CERM 402
C8854 0.1UF 20% 10V CERM 402

GPU_IFPAB_VPROBE
GPU_IFPCD_VPROBE

NO STUFF C8855 0.01UF 20% 16V CERM 402
NO STUFF C8856 0.01UF 20% 16V CERM 402

NV G84M Video Interfaces

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

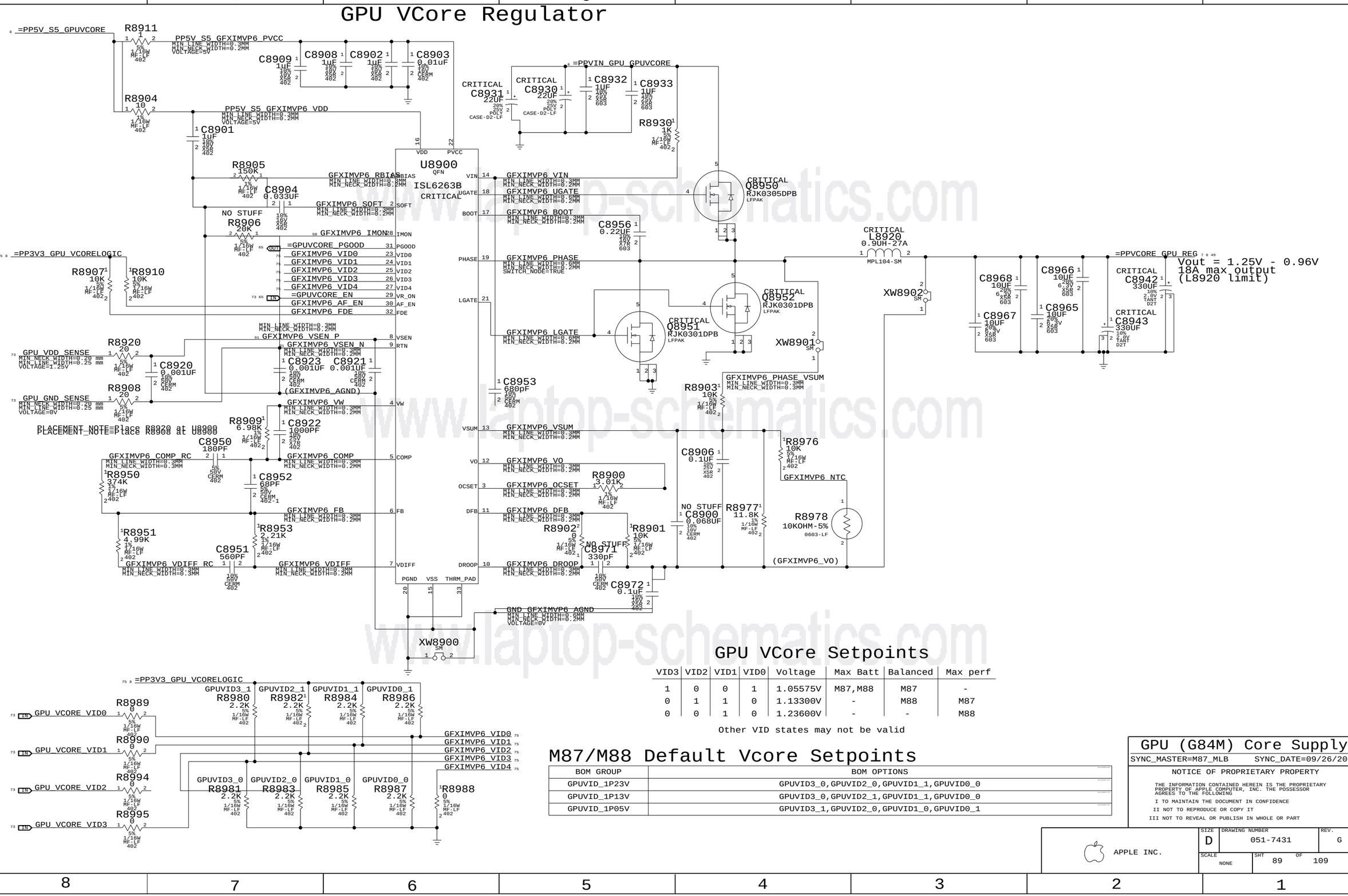
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 88 OF 109	

www.laptop-schematics.com

GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	0	1	1.05575V	M87,M88	M87	-
0	1	1	0	1.13300V	-	M88	M87
0	0	1	0	1.23600V	-	-	M88

Other VID states may not be valid

M87/M88 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P23V	GPUVID3_0,GPUVID2_0,GPUVID1_1,GPUVID0_0
GPUVID_1P13V	GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_0
GPUVID_1P05V	GPUVID3_1,GPUVID2_0,GPUVID1_0,GPUVID0_1

GPU (G84M) Core Supply

SYNC_MASTER=M87_MLB SYNC_DATE=09/26/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

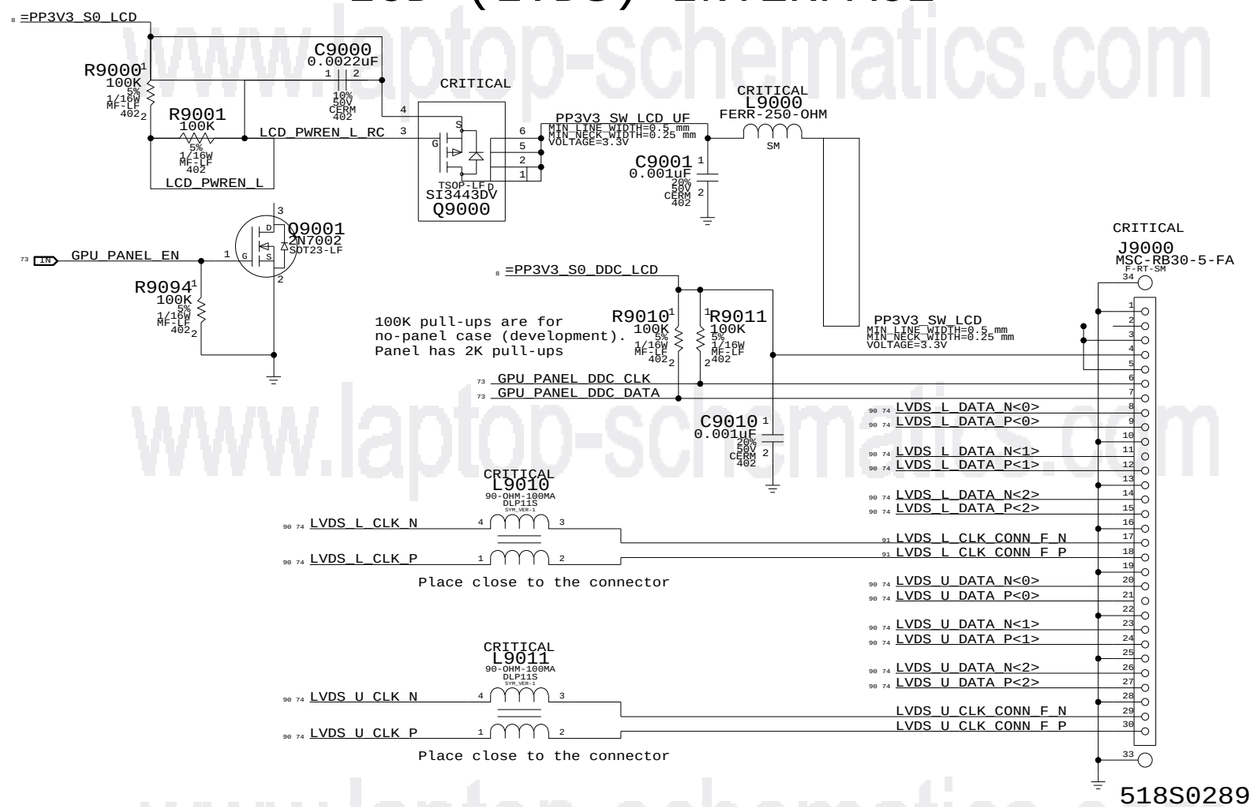
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 89 OF 109	

www.laptop-schematics.com

LCD (LVDS) INTERFACE



www.laptop-schematics.com

LVDS Display Connector

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

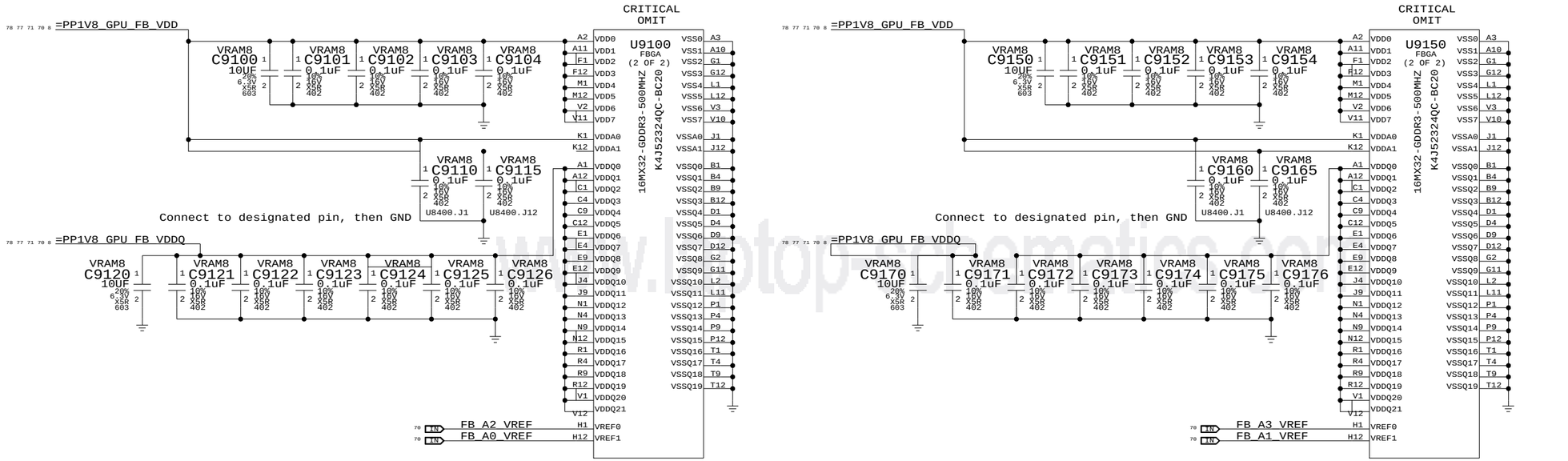
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

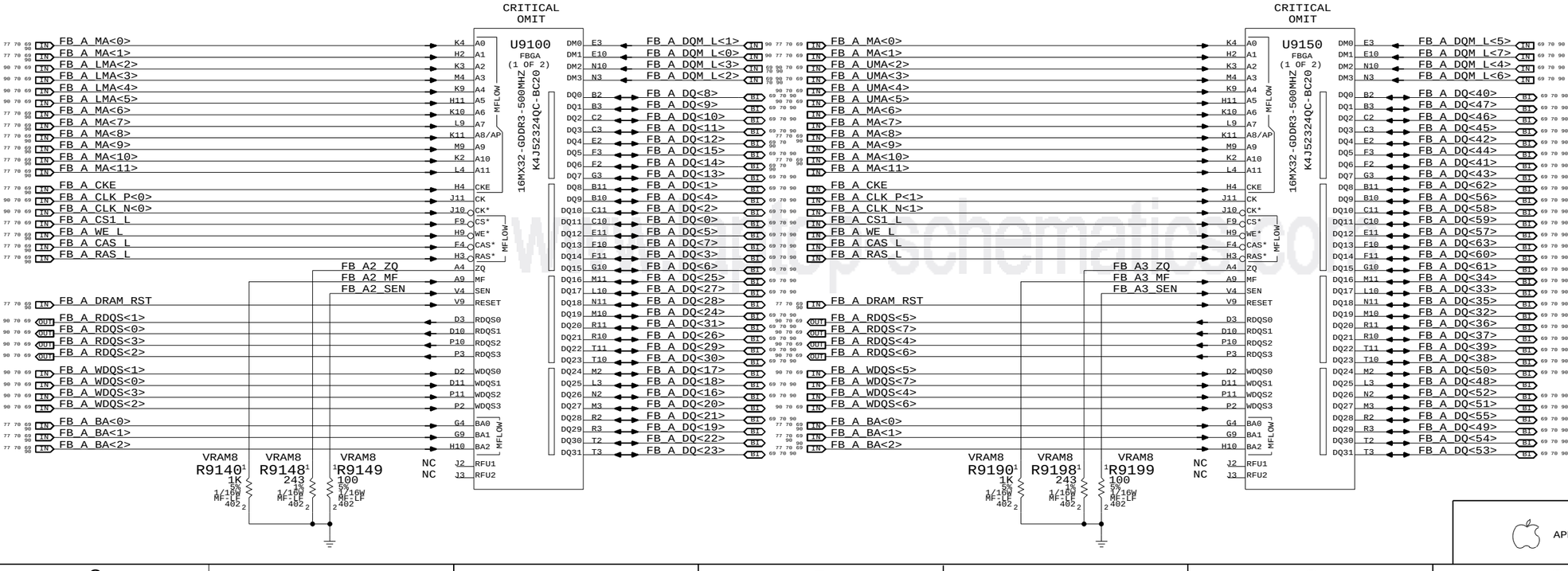
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 90 OF 109	





Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

www.laptop-schematics.com

GDDR3 Frame Buffer A (Bot)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

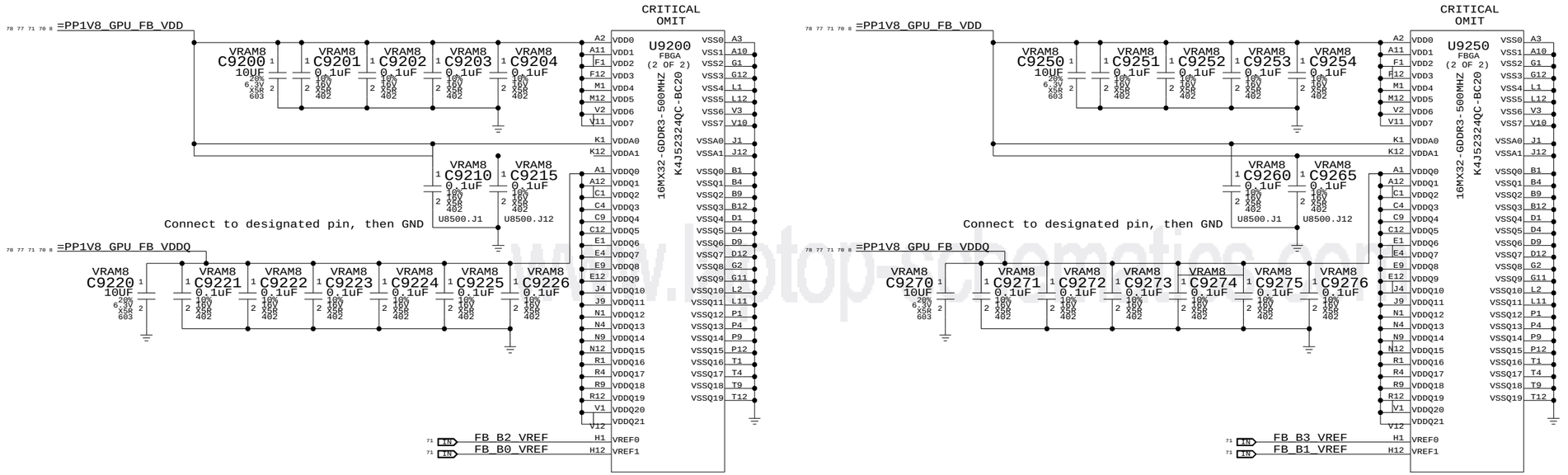
II NOT TO REPRODUCE OR COPY IT

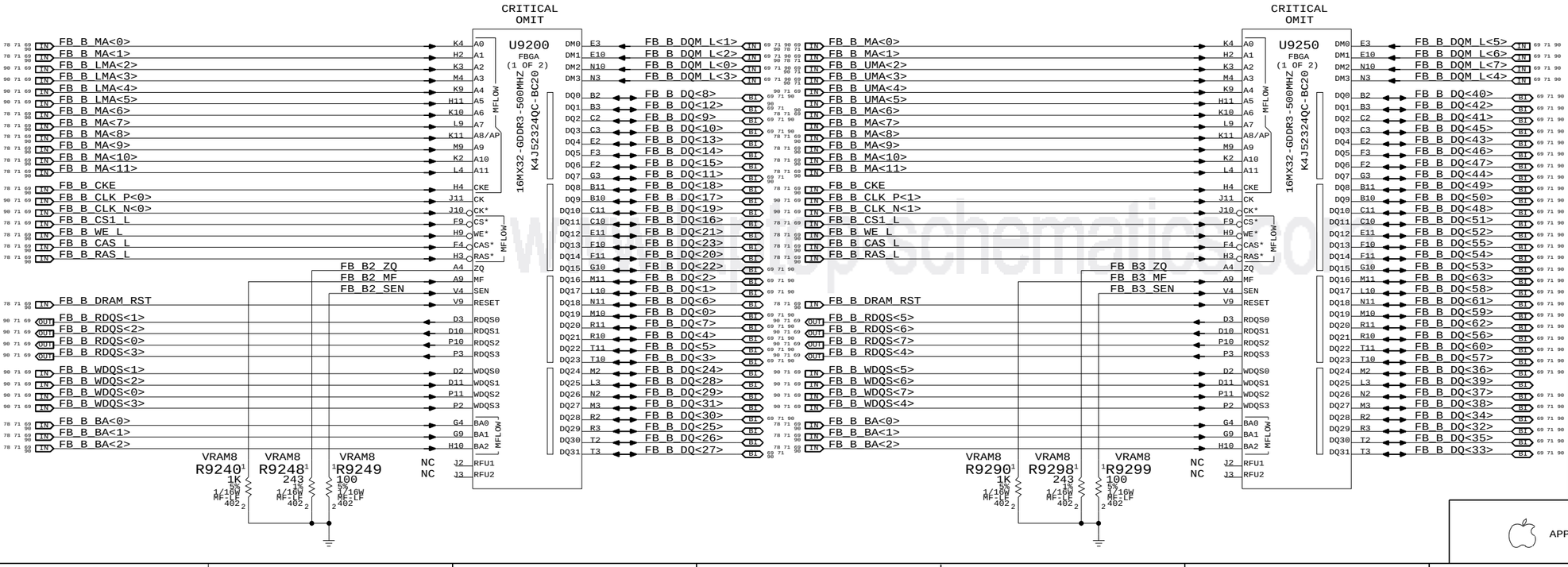
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE	SHT	OF
NONE	91	109





Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

www.laptop-schematics.com

GDDR3 Frame Buffer B (Bot)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

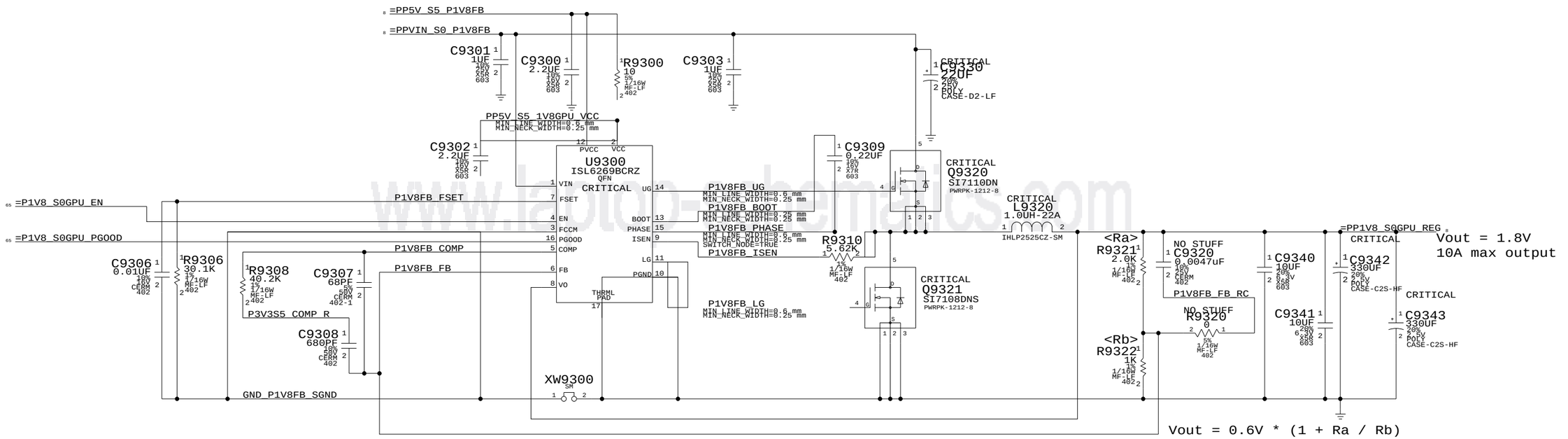
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 92 OF 109	

1.8V Frame Buffer Regulator

www.laptop-schematics.com



1.8V FB Power Supply

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 93 OF 109	

TMDS Filtering

(Place close to GPU) (Place close to connector)

TMDS_DATA_N<0> → NO STUFF R9462 49.9 1% 1/16W MF-LF 402 → CRITICAL L9460 90-OHM-100MA DLP11S → TMDS_DATA_F_N<0>
TMDS_DATA_P<0> → TMDS_DATA_F_P<0>
=PP3V3_GPU_TMDSBIAS → NO STUFF C9462 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY TMDS_DATA_R0
NO STUFF R9463 49.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<1> → NO STUFF R9466 49.9 → CRITICAL L9464 → TMDS_DATA_F_N<1>
TMDS_DATA_P<1> → TMDS_DATA_F_P<1>
=PP3V3_GPU_TMDSBIAS → NO STUFF C9466 0.01UF
SIGNAL_MODEL=EMPTY TMDS_DATA_R1
NO STUFF R9467 49.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<2> → NO STUFF R9470 49.9 → CRITICAL L9468 → TMDS_DATA_F_N<2>
TMDS_DATA_P<2> → TMDS_DATA_F_P<2>
=PP3V3_GPU_TMDSBIAS → NO STUFF C9470 0.01UF
SIGNAL_MODEL=EMPTY TMDS_DATA_R2
NO STUFF R9471 49.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to connector.

TMDS_CLK_N → R9472 0 5% 1/16W MF-LF 402 → TMDS_CLK_R_N → CRITICAL L9472 360-OHM SM → TMDS_CLK_F_N
TMDS_CLK_P → R9473 0 → TMDS_CLK_R_P → TMDS_CLK_F_P
=PP3V3_GPU_TMDSBIAS → NO STUFF C9474 0.01UF
SIGNAL_MODEL=EMPTY TMDS_CLK_CMF
NO STUFF R9474 49.9 1% 1/16W MF-LF 402
NO STUFF R9475 49.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<3> → NO STUFF R9478 49.9 → CRITICAL L9476 → TMDS_DATA_F_N<3>
TMDS_DATA_P<3> → TMDS_DATA_F_P<3>
=PP3V3_GPU_TMDSBIAS → NO STUFF C9478 0.01UF
SIGNAL_MODEL=EMPTY TMDS_DATA_R3
NO STUFF R9479 49.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<4> → NO STUFF R9482 49.9 → CRITICAL L9480 → TMDS_DATA_F_N<4>
TMDS_DATA_P<4> → TMDS_DATA_F_P<4>
=PP3V3_GPU_TMDSBIAS → NO STUFF C9482 0.01UF
SIGNAL_MODEL=EMPTY TMDS_DATA_R4
NO STUFF R9483 49.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to connector.

TMDS_DATA_N<5> → NO STUFF R9486 49.9 → CRITICAL L9484 → TMDS_DATA_F_N<5>
TMDS_DATA_P<5> → TMDS_DATA_F_P<5>
=PP3V3_GPU_TMDSBIAS → NO STUFF C9486 0.01UF
SIGNAL_MODEL=EMPTY TMDS_DATA_R5
NO STUFF R9487 49.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to connector.

VGA SYNC Buffers

=PP3V3_GPU_VGASYNC → C9450 0.1UF → U9450 MC74VHC1G08 SC70
PLACEMENT_NOTE=Place close to connector.
GPU_VGA_VSYNC → U9450 → VGA_VSYNC_R → R9450 33 5% 1/16W MF-LF 402 → VGA_VSYNC

=PP3V3_GPU_VGASYNC → C9451 0.1UF → U9451 MC74VHC1G08 SC70
PLACEMENT_NOTE=Place close to connector.
GPU_VGA_HSYNC → U9451 → VGA_HSYNC_R → R9451 33 5% 1/16W MF-LF 402 → VGA_HSYNC

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

GPU_TV_COMP_VGA_B → VGA_TERM_FILTER R9440 150 1% 1/16W MF-LF 402 → CRITICAL FL9440 → C9440 3.3PF 0.25PF 50V CERM 402 → VGA_B (DACB TV COMP)
GPU_TV_Y_VGA_G → VGA_TERM_FILTER R9441 150 → C9441 3.3PF → VGA_G (DACB TV Y)
GPU_TV_C_VGA_R → VGA_TERM_FILTER R9442 150 → C9442 3.3PF → VGA_R (DACB TV C)
FL9440: 210MHZ MEA2010P-SM

DVI INTERFACE

DVI DDC Current Limit
(55mA requirement per DVI spec)

=PP5V_S0_DVI_DDC → CRITICAL F9410 0.5AMP-13.2V SM-LF → PP5V_S0_DDC_F (MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V)
CRITICAL L9410 400-OHM-EMI SM-1 → PP5V_S0_DDC
C9410 0.01UF 25V CERM 603
CRITICAL J9400 QH11121-RIG02-4F F-RT-TH-DVI

J9400		J9400	
TMDS_DATA_F_N<0>	17	1	TMDS_DATA_F_N<2>
	9		TMDS_DATA_F_N<1>
TMDS_DATA_F_P<0>	18	2	TMDS_DATA_F_P<2>
	10		TMDS_DATA_F_P<1>
	19	3	
	11		
TMDS_DATA_F_N<5>	20	4	TMDS_DATA_F_N<4>
	12		TMDS_DATA_F_N<3>
TMDS_DATA_F_P<5>	21	5	TMDS_DATA_F_P<4>
	13		TMDS_DATA_F_P<3>
	22	6	DVI_DDC_CLK_R
	14		(PP5V_S0_DDC)
	23	7	DVI_DDC_DATA_R
	15		
TMDS_CLK_F_P	24	8	VGA_VSYNC
TMDS_CLK_F_N		16	DVI_HPD_R
VGA_B	C3	C1	VGA_R
	C5B	C5A	
VGA_HSYNC	C4	C2	VGA_G
	34	32	

514-0278

VGA_TERM_CONN R9445 150 1% 1/16W MF-LF 402
VGA_TERM_CONN R9443 150
VGA_TERM_CONN R9444 150

Isolation required for DVI->ADC Adapter

D9410 SOD-123 B0530WXF
PP5V_S0_DDC_PULLUPS (MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V)
R9410 4.7K 5% 1/16W MF-LF 402
R9412 4.7K
R9411 100 → DVI_DDC_CLK
R9413 100 → DVI_DDC_DATA
R9414 100 → DVI_HPD
C9411 100PF 5% 50V CERM 402
C9413 100PF
C9414 100PF

GPU Isolation / Level-Shift

=PP3V3_GPU_DVI
Q9411 2N7002DW-X-F SOT-363
R9420 10K 5% 1/16W MF-LF 402 → GPU_DVI_DDC_CLK OUT
R9421 10K → GPU_DVI_DDC_DATA OUT
Q9411 2N7002DW-X-F SOT-363
R9422 100K 5% 1/16W MF-LF 402 → GPU_HPD OUT
Q9414 2N7002DW-X-F SOT-363
R9415 20K 5% 1/16W MF-LF 402
R9416 10K 5% 1/16W MF-LF 402 ← DVI_HOTPLUG_DET

www.laptop-schematics.com

DVI Display Connector

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

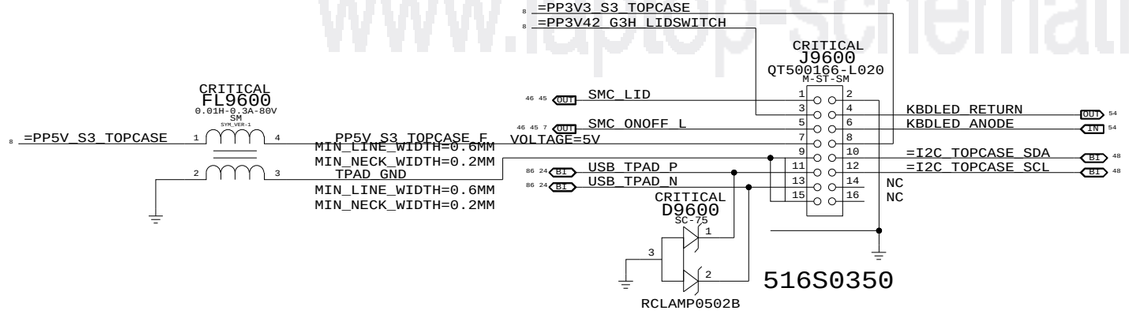
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

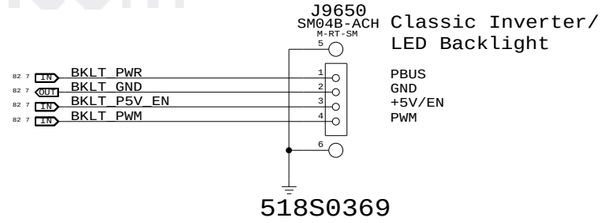
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	G
	SCALE: NONE	SHT 94 OF 109	

www.laptop-schematics.com

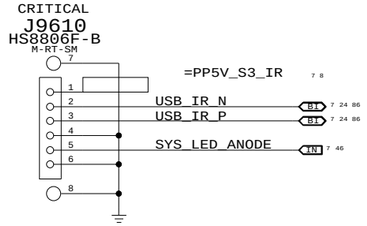
Top-Case Connector



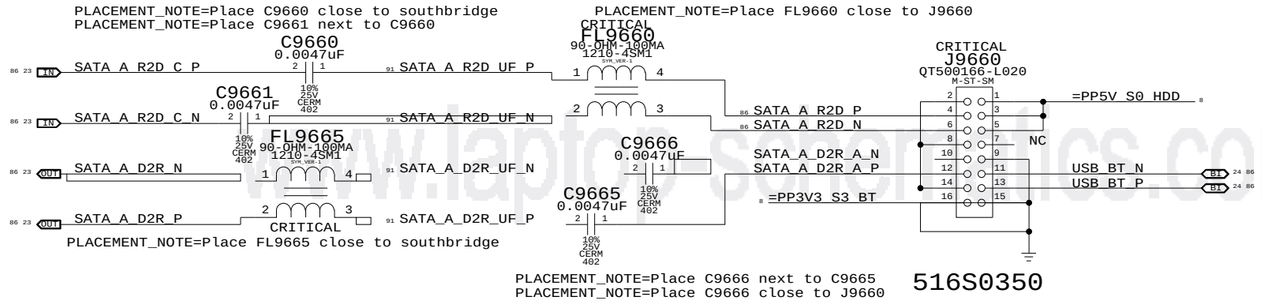
Backlight Connector



IR & Sleep LED Connector



Bluetooth (M13P) & SATA HDD Flex Connector



Project Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

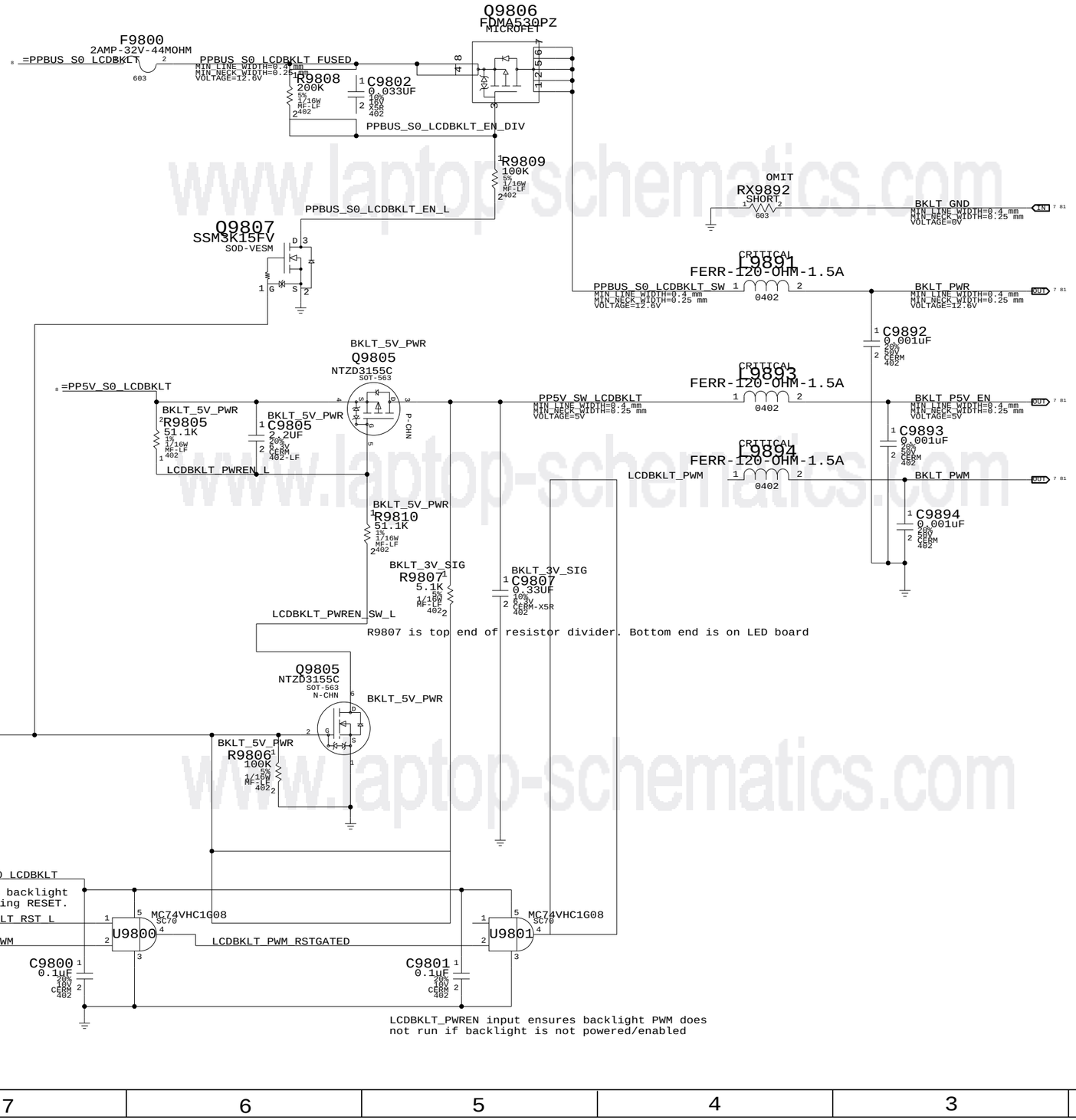
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 96 OF 109	



www.laptop-schematics.com

LCD Backlight Support

SYNC_MASTER=M87_LIO SYNC_DATE=12/06/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 98 OF 109	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	10
CPU_FERR_L	CPU_55S		CPU_FERR_L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	10 46 59
CPU_PWRGD	CPU_55S		CPU_PWRGD	7 10 13 23
CPU_FROM_SB	CPU_55S		CPU_INTR	10 23
CPU_FROM_SB	CPU_55S		CPU_NMI	10 23
CPU_FROM_SB	CPU_55S		CPU_A20M_L	10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	7 10 23
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	10 23 47
CPU_FROM_SB	CPU_55S		CPU_SMI_L	10 23
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	7 10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	7 16 25 59
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	7 59
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	7 10 16 23 59
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 88
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 88
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	13
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	7 12 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 59
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	59
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	59

www.laptop-schematics.com

CPU/FSB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE NONE SHT 100 OF 109

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
LVDS	*	20 MIL	?	
CRT	*	25 MIL	?	DG Says 40 mil spacing minimum
CRT_2CRT	*	20 MIL	?	
CRT_SYNC	*	25 MIL	?	DG Says 30 mil spacing minimum
CRT_SYNC2SYNC	*	20 MIL	?	
TVDAC	*	25 MIL	?	DG Says 40 mil spacing minimum
TVDAC_2TVDAC	*	20 MIL	?	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG_R2D_P<15..0>	67
	PCIE_100D	PCIE	PEG_R2D_N<15..0>	67
	PCIE_100D	PCIE	PEG_R2D_C_P<15..0>	15 67
	PCIE_100D	PCIE	PEG_R2D_C_N<15..0>	15 67
PEG_D2R	PCIE_100D	PCIE	PEG_D2R_P<15..0>	15 67
	PCIE_100D	PCIE	PEG_D2R_N<15..0>	15 67
	PCIE_100D	PCIE	PEG_D2R_C_P<15..0>	67
	PCIE_100D	PCIE	PEG_D2R_C_N<15..0>	67
DMI_N2S	DMI_100D	DMI	DMI_N2S_P<3..0>	16 24
	DMI_100D	DMI	DMI_N2S_N<3..0>	16 24
DMI_S2N	DMI_100D	DMI	DMI_S2N_P<3..0>	16 24
	DMI_100D	DMI	DMI_S2N_N<3..0>	16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	15 22
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	15 22
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_N<3>	
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	15 22
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	15 22
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_P<3>	
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_N<3>	
LVDS_IBG		LVDS	LVDS_IBG	15 22
CRT_TVO_IREF		CRT	CRT_TVO_IREF	
CRT_RED	CRT_50S	CRT	CRT_RED	
CRT_GREEN	CRT_50S	CRT	CRT_GREEN	
CRT_BLUE	CRT_50S	CRT	CRT_BLUE	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R	
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC	
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC	
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC	

www.laptop-schematics.com

www.laptop-schematics.com

NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE	SHT	OF
NONE	101	109

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK_N<2..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK_N<5..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	17 32

www.laptop-schematics.com

Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 102 OF 109	

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L	23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ	23 42
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L	24 42
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	23 81
	SATA_100D	SATA	SATA_A_R2D_C_N	23 81
	SATA_100D	SATA	SATA_A_R2D_P	81
	SATA_100D	SATA	SATA_A_R2D_N	81
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P	23 81
	SATA_100D	SATA	SATA_A_D2R_N	23 81
	SATA_100D	SATA	SATA_A_D2R_C_P	
	SATA_100D	SATA	SATA_A_D2R_C_N	
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D_C_P	23 42
	SATA_100D	SATA	SATA_B_R2D_C_N	23 42
	SATA_100D	SATA	SATA_B_R2D_P	
	SATA_100D	SATA	SATA_B_R2D_N	
SATA_B_D2R	SATA_100D	SATA	SATA_B_D2R_P	23 42
	SATA_100D	SATA	SATA_B_D2R_N	23 42
	SATA_100D	SATA	SATA_B_D2R_C_P	
	SATA_100D	SATA	SATA_B_D2R_C_N	
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D_C_P	23 42
	SATA_100D	SATA	SATA_C_R2D_C_N	23 42
	SATA_100D	SATA	SATA_C_R2D_P	
	SATA_100D	SATA	SATA_C_R2D_N	
SATA_C_D2R	SATA_100D	SATA	SATA_C_D2R_P	23 42
	SATA_100D	SATA	SATA_C_D2R_N	23 42
	SATA_100D	SATA	SATA_C_D2R_C_P	
	SATA_100D	SATA	SATA_C_D2R_C_N	
SATA_RBIAS	SATA_55S		SATA_RBIAS	42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	23 34
	HDA_55S	HDA	HDA_BIT_CLK_R	23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	23 34
	HDA_55S	HDA	HDA_SYNC_R	23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	23 34
	HDA_55S	HDA	HDA_RST_L_R	23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	23 34
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	23 34
	HDA_55S	HDA	HDA_SDOUT_R	23
USB_EXTA	USB_90D	USB	USB_EXTA_P	24 43
	USB_90D	USB	USB_EXTA_N	24 43
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	24 34
	USB_90D	USB	USB_MINI_N	24 34
USB_EXTD	USB_90D	USB	USB_EXTD_P	9 24
	USB_90D	USB	USB_EXTD_N	9 24
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	24 44
	USB_90D	USB	USB_CAMERA_N	24 44
USB_BT	USB_90D	USB	USB_BT_P	24 81
	USB_90D	USB	USB_BT_N	24 81
USB_TPAD	USB_90D	USB	USB_TPAD_P	24 81
	USB_90D	USB	USB_TPAD_N	24 81
USB_IR	USB_90D	USB	USB_IR_P	7 24 81
	USB_90D	USB	USB_IR_N	7 24 81
USB_EXTB	USB_90D	USB	USB_EXTB_P	24 34
	USB_90D	USB	USB_EXTB_N	24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	24 34
	USB_90D	USB	USB_EXCARD_N	24 34
USB_EXTC	USB_90D	USB	USB_EXTC_P	24 34
	USB_90D	USB	USB_EXTC_N	24 34
USB_RBIAS	USB_60S		USB_RBIAS	24
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK	25 48
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA	25 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK	25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA	25 48
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	24 56
	SPI_55S	SPI	SPI_SCLK	56
	SPI_55S	SPI	SPI_A_SCLK_R	
	SPI_55S	SPI	SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	24 56
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	56
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	24 56
	SPI_55S	SPI	SPI_A_SO_R	56
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_I0	SPI_55S	SPI	SPI_CE_R_L<0>	24 56
	SPI_55S	SPI	SPI_CE_L<0>	56
SPI_CE_I1	SPI_55S	SPI	SPI_CE_R_L<1>	
	SPI_55S	SPI	SPI_CE_L<1>	

www.laptop-schematics.com

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE NONE SHT 103 OF 109

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCI_AD	PCI_55S	PCI	PCI_AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI_AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI_AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI_AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI_PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	24 38
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI_LOCK_L	24
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI_FW_REQ_L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI_FW_GNT_L	24 38
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	24
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_REQ2_L	PCI_55S	PCI	PCI_REQ2_L	24
PCI_GNT2_L	PCI_55S	PCI	PCI_GNT2_L	
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	24 38
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE_A_R2D_C_P	
	PCIE_100D	PCIE	PCIE_A_R2D_C_N	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE_A_D2R_P	
	PCIE_100D	PCIE	PCIE_A_D2R_N	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_B_R2D_C_P	
	PCIE_100D	PCIE	PCIE_B_R2D_C_N	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_B_D2R_P	
	PCIE_100D	PCIE	PCIE_B_D2R_N	
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_P	34
	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_N	34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE_EXCARD_D2R_P	34
	PCIE_100D	PCIE	PCIE_EXCARD_D2R_N	34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_100D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE_FW_D2R_P	
	PCIE_100D	PCIE	PCIE_FW_D2R_N	
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE_MINI_R2D_C_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_R2D_C_N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE_MINI_D2R_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_D2R_N	24 34
GLAN_COMP			GLAN_COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE_ENET_R2D_C_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_C_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_P	35
	PCIE_100D	PCIE	PCIE_ENET_R2D_N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE_ENET_D2R_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_P	35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<0>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<1>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<2>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3>	35 37

www.laptop-schematics.com

SB Constraints (2 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE	SHT	OF
NONE	104	109

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	29 30
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	29 30
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	29 30
CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	29 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	7 10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	7 10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 83
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 83
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 47
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	30 38
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	30 45
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_DOT96)	CRT_50S	GND	NB_CLK96M_DOT_P	
(CK505_DOT96)	CRT_50S	GND	NB_CLK96M_DOT_N	
(CK505_LVDS)	CRT_50S	GND	NB_CLK100M_DPLLSS_P	
(CK505_LVDS)	CRT_50S	GND	NB_CLK100M_DPLLSS_N	
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	9
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	9
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	30 34
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	30 34
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 30
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	30 34
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	30 34
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	30 35
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	30 35

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	48
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	48
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	48
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	48
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	48
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	48
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	48
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	48
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48

www.laptop-schematics.com

Clock & SMC Constraints

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 105 OF 109	

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
FW_D_CTL	FW_55S	FW	FW_LINK<7..0>	
FW_D_CTL	FW_55S	FW	FW_CTL<1..0>	
FW_LCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_LCLK	
	CLK_MED_55S	CLK_MED	CLKFW_PHY_LCLK	38 39
FW_PCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_PCLK	38 39
	CLK_MED_55S	CLK_MED	CLKFW_PHY_PCLK	
FW_LKON	FW_55S	FW	FW_LKON	
	FW_55S	FW	FW_LKON_R	
FW_LPS	FW_55S	FW	FW_LPS	38 39
FW_LREQ	FW_55S	FW	FW_LREQ	38 39
FW_PINT	FW_55S	FW	FW_PINT	38 39
FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R	
	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI	
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_P	39 41
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_N	39 41
FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_P	39 41
FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_N	39 41
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_P	39 41
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_N	39 41
FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_P	39 41
FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_N	39 41

Port 2 Not Used

www.laptop-schematics.com

www.laptop-schematics.com

www.laptop-schematics.com

FireWire Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE	SHT	OF
NONE	106	109

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	=55_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<11..6>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CKE
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS0_L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST
FB_A_CMD	GDDR3_50SE	GDDR3_CMD	FB_A_LMA<5..2>
FB_B_CMD	GDDR3_50SE	GDDR3_CMD	FB_A_UMA<5..2>
FB_A_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<0>
FB_A_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<1>
FB_A_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<2>
FB_A_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<3>
FB_A_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<0>
FB_A_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<1>
FB_A_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<2>
FB_A_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<3>
FB_A_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<7..0>
FB_A_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<15..8>
FB_A_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<23..16>
FB_A_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<31..24>
FB_A_DQM0	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<0>
FB_A_DQM1	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<1>
FB_A_DQM2	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<2>
FB_A_DQM3	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<3>
FB_B_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<4>
FB_B_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<5>
FB_B_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<6>
FB_B_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<7>
FB_B_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<4>
FB_B_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<5>
FB_B_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<6>
FB_B_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<7>
FB_B_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<39..32>
FB_B_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<47..40>
FB_B_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<55..48>
FB_B_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<63..56>
FB_B_DQM0	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<4>
FB_B_DQM1	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<5>
FB_B_DQM2	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<6>
FB_B_DQM3	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<7>

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<11..6>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CKE
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS0_L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST
FB_C_CMD	GDDR3_50SE	GDDR3_CMD	FB_B_LMA<5..2>
FB_D_CMD	GDDR3_50SE	GDDR3_CMD	FB_B_UMA<5..2>
FB_C_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<0>
FB_C_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<1>
FB_C_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<2>
FB_C_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<3>
FB_C_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<0>
FB_C_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<1>
FB_C_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<2>
FB_C_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<3>
FB_C_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<7..0>
FB_C_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<15..8>
FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<23..16>
FB_C_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<31..24>
FB_C_DQM0	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<0>
FB_C_DQM1	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<1>
FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<2>
FB_C_DQM3	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<3>
FB_D_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<4>
FB_D_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<5>
FB_D_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<6>
FB_D_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<7>
FB_D_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<4>
FB_D_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<5>
FB_D_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<6>
FB_D_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<7>
FB_D_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<39..32>
FB_D_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<47..40>
FB_D_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<55..48>
FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<63..56>
FB_D_DQM0	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<4>
FB_D_DQM1	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<5>
FB_D_DQM2	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<6>
FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<7>

G84M Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS
LVDS_L_CLK	LVDS_100D	LVDS	LVDS_L_CLK_P
	LVDS_100D	LVDS	LVDS_L_CLK_N
LVDS_L_DATA	LVDS_100D	LVDS	LVDS_L_DATA_P<2..0>
	LVDS_100D	LVDS	LVDS_L_DATA_N<2..0>
I127	LVDS_100D	LVDS	LVDS_L_DATA_P<3>
I126	LVDS_100D	LVDS	LVDS_L_DATA_N<3>
LVDS_U_CLK	LVDS_100D	LVDS	LVDS_U_CLK_P
	LVDS_100D	LVDS	LVDS_U_CLK_N
LVDS_U_DATA	LVDS_100D	LVDS	LVDS_U_DATA_P<2..0>
	LVDS_100D	LVDS	LVDS_U_DATA_N<2..0>
I128	LVDS_100D	LVDS	LVDS_U_DATA_P<3>
I129	LVDS_100D	LVDS	LVDS_U_DATA_N<3>
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_N
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<5..0>
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_N<5..0>
VGA_R_TV_C	VGA_50S	VGA	GPU_TV_C_VGA_R
VGA_G_TV_Y	VGA_50S	VGA	GPU_TV_Y_VGA_G
VGA_B_TV_COMP	VGA_50S	VGA	GPU_TV_COMP_VGA_B
	VGA_50S	VGA	GPU_VGA_R
	VGA_50S	VGA	GPU_VGA_G
	VGA_50S	VGA	GPU_VGA_B
	VGA_50S	VGA	GPU_TV_C
	VGA_50S	VGA	GPU_TV_Y
	VGA_50S	VGA	GPU_TV_COMP
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_HSYNC
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_VSYNC

www.laptop-schematics.com

GPU (G84M) Constraints

SYNC_MASTER=M87_MLB SYNC_DATE=10/02/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 107 OF 109	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
DMI	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	ENET_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	FW_POWER	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*			0.100 MM	2.54 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	ISL10			0.100 MM	2.54 MM		
MEM_85D	ISL4,ISL10			0.100 MM	2.54 MM		

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
TMDS_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

M87 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_P	34
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_N	34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_P	34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_N	34
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3..0>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3..0>	
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
	FW_110D	FW_TP	FW_PORT0_TPA_FL_P	41
	FW_110D	FW_TP	FW_PORT0_TPA_FL_N	41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_P	41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_N	41
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_P	81
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_N	81
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_P	81
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_N	81
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	43
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	43
(USB_EXTA)	USB_90D	USB	USB2_RT_P	43
(USB_EXTA)	USB_90D	USB	USB2_RT_N	43
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_P	
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_N	
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_P	7 44
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_N	7 44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_P	75
	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_N	75
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	NBCOREISNS_P	50
	SENSE_1TO1_55S	SENSE	NBCOREISNS_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8ISNS_P	50
	SENSE_1TO1_55S	SENSE	P1V8ISNS_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V25ISNS_P	50
	SENSE_1TO1_55S	SENSE	P1V25ISNS_N	50
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	7 51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 51
	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 73
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	51 73
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	HSTHMSNS_D_P	7 51
	THERM_1TO1_55S	THERM	HSTHMSNS_D_N	7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	RSFSTHMSNS_D_P	7 51
	THERM_1TO1_55S	THERM	RSFSTHMSNS_D_N	7 51
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_P	76
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_N	76
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8ISNS_R_P	50
	SENSE_1TO1_55S	SENSE	P1V8ISNS_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_P	50
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_N	50
	TMDS_100D	TMDS	TMDS_CLK_R_P	80
	TMDS_100D	TMDS	TMDS_CLK_R_N	80
	TMDS_100D	TMDS	TMDS_CLK_F_P	80
	TMDS_100D	TMDS	TMDS_CLK_F_N	80
	TMDS_100D	TMDS	TMDS_DATA_F_P<5..0>	80
	TMDS_100D	TMDS	TMDS_DATA_F_N<5..0>	80
(VGA_R_TV_Y)	VGA_50S	VGA	VGA_R	80
(VGA_G_TV_C)	VGA_50S	VGA	VGA_G	80
(VGA_B_TV_COMP)	VGA_50S	VGA	VGA_B	80
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC_R	80
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC_R	80
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC	80
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC	80
		PP1V8_MEM	=PP1V8_S3M_MEM_A	8 31
		PP1V8_MEM	=PP1V8_S3M_MEM_B	8 32
		GND	GND	
		ENET_POWER		
		SB_POWER	PP3V3_S5	8
		SB_POWER	PP3V3_S0	8 65
		SB_POWER	PP1V5_S0	8
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_P	50
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_N	50
		FW_POWER		

Project Specific Constraints

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G
SCALE: NONE	SHT 108 OF 109	

www.laptop-schematics.com

M75 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	ISL2,ISL11	Y	0.250 MM	0.076 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.125 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
46_OHM_SE	TOP,BOTTOM	Y	0.126 MM	0.126 MM			
46_OHM_SE	*	Y	0.100 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M87_MLB SYNC_DATE=10/03/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	G

SCALE NONE SHT 109 OF 109

www.laptop-schematics.com