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# Molokai

## Braswell CPU (TDP 6.5W) SoC

### Project Information

Phase: DVT

| POWER PLANE    | VOLTAGE | CONTROL SIGNAL      | Power States ACTIVE IN |
|----------------|---------|---------------------|------------------------|
| +VIN           | +19V    |                     | Always                 |
| VCCRTC         | +1.5V   |                     | Always                 |
| +3V            | +3.3V   | MAIN_ON1            | S0                     |
| +3V_S5         | +3.3V   | S5_LOAD_CODE        | S0-S5                  |
| +3V_ALW        | +3.3V   | AC/DC Insert enable | Always (LDO)           |
| +5V            | +5V     | MAIN_ON             | S0                     |
| +5V_S5         | +5V     | S5_ON               | S0-S5                  |
| +5V_ALW        | +5V     | AC/DC Insert enable | Always (LDO)           |
| +3V_WLAN_P     | +3.3V   | WLAN_ON             | S0-S5                  |
| +3V_LAN        | +3.3V   | LAN_PWR_ON          | S0-S5                  |
| +1.35V_S3      | +1.35V  | S3_ON               | S0-S3                  |
| +1.05V_S5      | +2.5V   | S5_ON               | S0-S5                  |
| +1.8V_S5       | +1.8V   | S5_ON               | S0-S5                  |
| +1.8V          | +1.8V   | MAIN_ON             | S0                     |
| +VNN           | +1.05V  | S5_ON               | S0-S5                  |
| +VGG           | -       | MAIN_ON             | S0                     |
| CPU_CORE       | -       | VGG_PWRGD           | S0                     |
| +1.8V_ALW      | +1.8V   | S5_ON               | S0-S5                  |
| +1.15V_S5      | +1.15V  | S5_ON               | S0-S5                  |
| +1.24V_S5      | +1.24V  | S5_ON               | S0-S5                  |
| +0.65V_DDR_VTT | +0.675V | S3_ON               | S3                     |
| +3V_S5_PRIME   | +1V     | S5_ON               | S0-S5                  |
| +1.5V          | +1.5V   | MAIN_ON             | S0                     |

### BOARD ID SETTING

|               |                            |           |
|---------------|----------------------------|-----------|
|               | Board ID<br>(Default = 00) |           |
| Model         | BOARD_ID1                  | BOARD_ID2 |
| All EVT       | 0                          | 0         |
| All DVT       | 0                          | 1         |
| PVT1          | 1                          | 0         |
| PVT2+         | 1                          | 1         |
| MVB,A         | 0                          | 0         |
| 1st Major ECN | 0                          | 1         |
| 2nd Major ECN | 1                          | 0         |
| 3rd Major ECN | 1                          | 1         |

|          |                           |           |          |                           |           |           |           |  |
|----------|---------------------------|-----------|----------|---------------------------|-----------|-----------|-----------|--|
|          | eMMC ID<br>(Default = 00) |           |          | VRAM ID<br>(Default = 00) |           |           |           |  |
| eMMC     | BOARD_ID3                 | BOARD_ID4 | VRAM     | BOARD_ID3                 | BOARD_ID2 | BOARD_ID1 | BOARD_ID5 |  |
| W/O      | 0                         | 0         | UMA      | 0                         | 0         |           |           |  |
| Hynix    | 0                         | 1         | Hynix    | 0                         | 1         |           |           |  |
| Samsung  | 1                         | 0         | Mircon   | 1                         | 0         |           |           |  |
| Reserved | 1                         | 1         | Reserved | 1                         | 1         |           |           |  |

### Schematic “Value” Definition

| Molokai INTEL Platform |                                | DB/SI/PV Stage   |         |         |          | MP      |         |          |
|------------------------|--------------------------------|------------------|---------|---------|----------|---------|---------|----------|
| By Value format        | Description                    | Auto BOM Control | Molokai | Lanai-U | Lanai-UE | Molokai | Lanai-U | Lanai-UE |
| XX                     | Install                        | V                | V       | V       | V        | V       | V       | V        |
| *XX                    | Non-Install                    | V                |         |         |          |         |         |          |
| EV@XX                  | Install dGPU device            | V                | V       |         |          | V       |         |          |
| SATA@XX                | Install SATA device            | V                | V       | V       |          | V       | V       |          |
| EMMC@XX                | Install EMMC                   | V                |         |         | V        |         |         | V        |
| PROTO@XX               | Install in pre-production only | V                | V       | V       | V        |         |         |          |
| MP@XX                  | Install in MP only             | V                |         |         |          | V       | V       | V        |

\*\*\*Board ID by manual control

Molokai -2G : \*

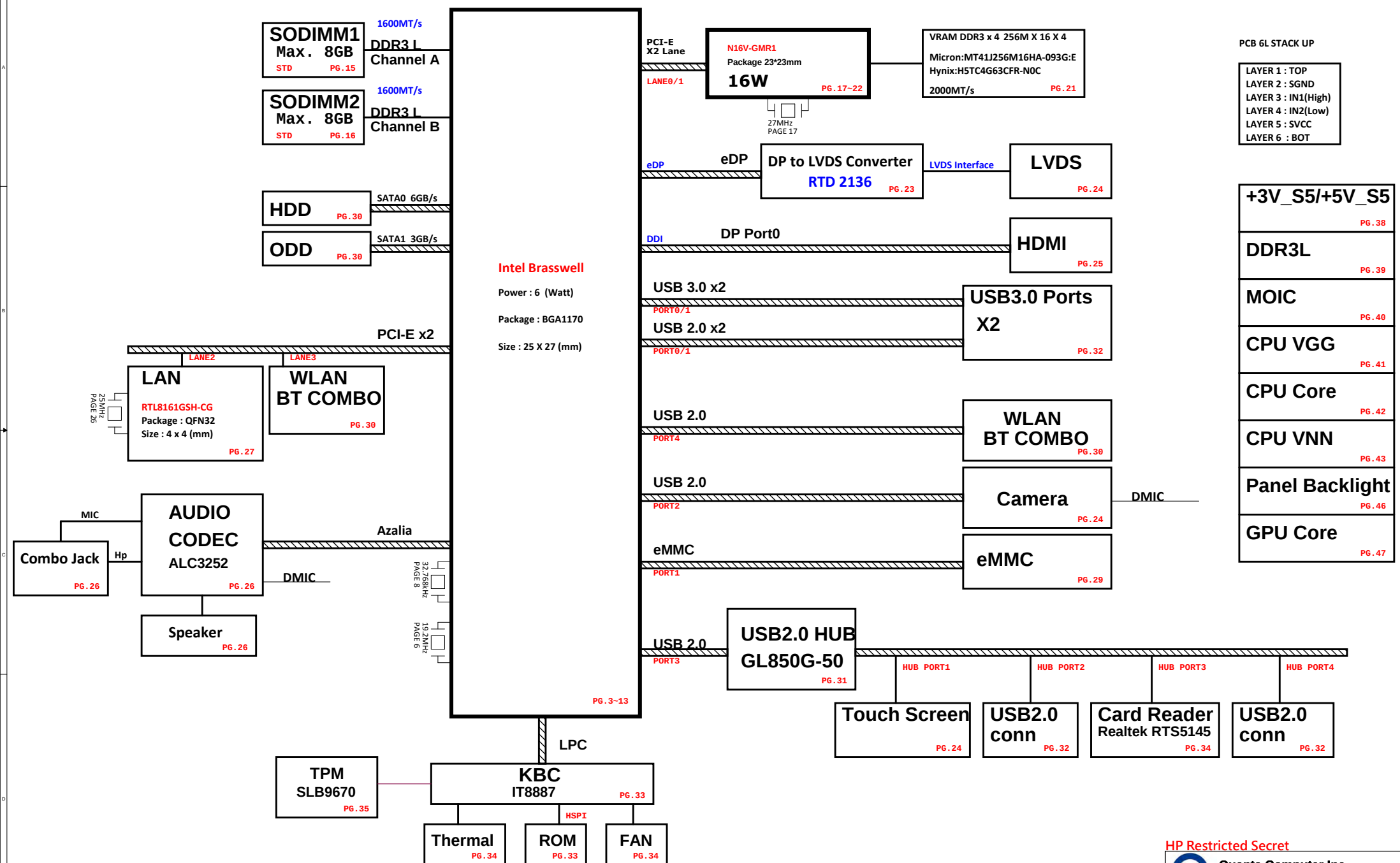
Molokai -UE : \*\*

### PCB AND SILKSCREEN COLOR

| Program Phase        | Color of PCB | Silkscreen |
|----------------------|--------------|------------|
| EVT                  | RED          | YELLOW     |
| DVT                  | LIGHT BLUE   | YELLOW     |
| PVT/MVB / PRODUCTION | GREEN        | WHITE      |

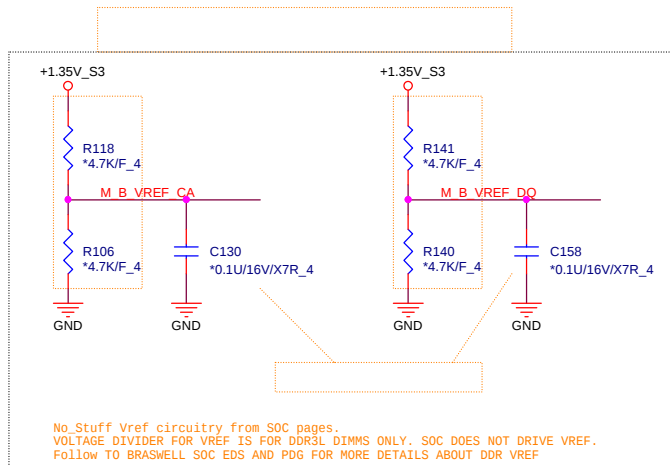
HP Restricted Secret

# Molokai Intel Brasswell-M Platform Block Diagram

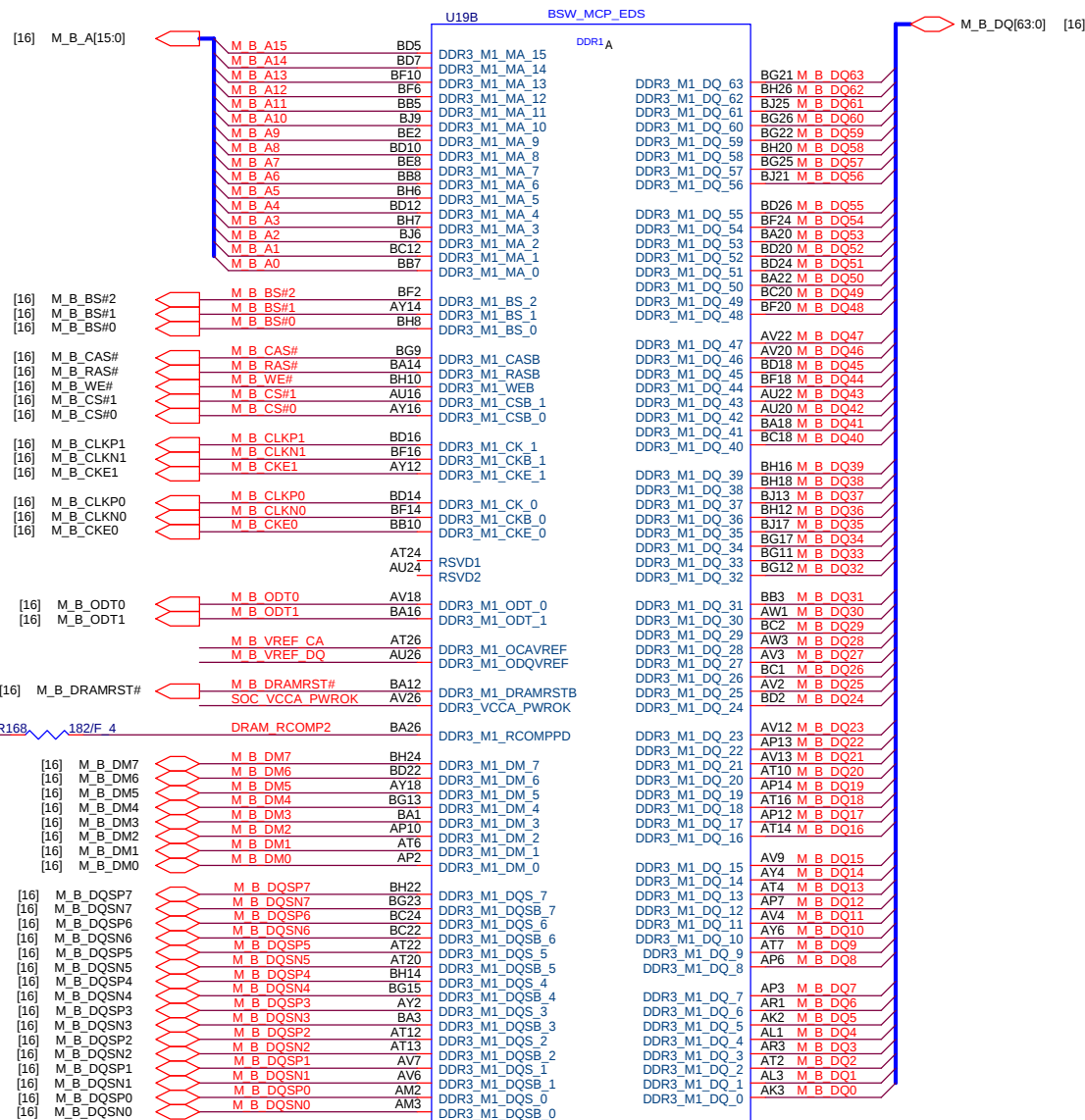
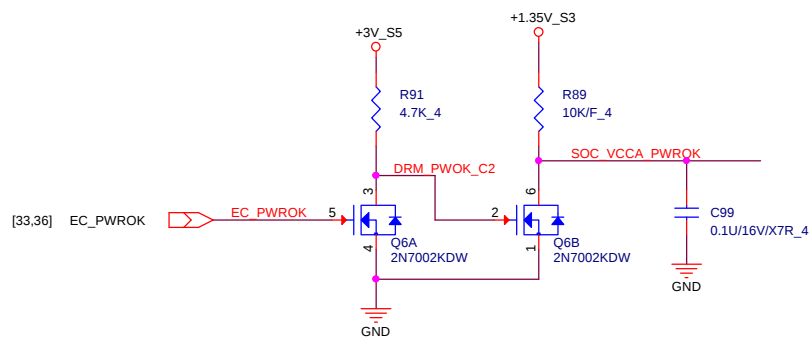


HP Restricted Secret



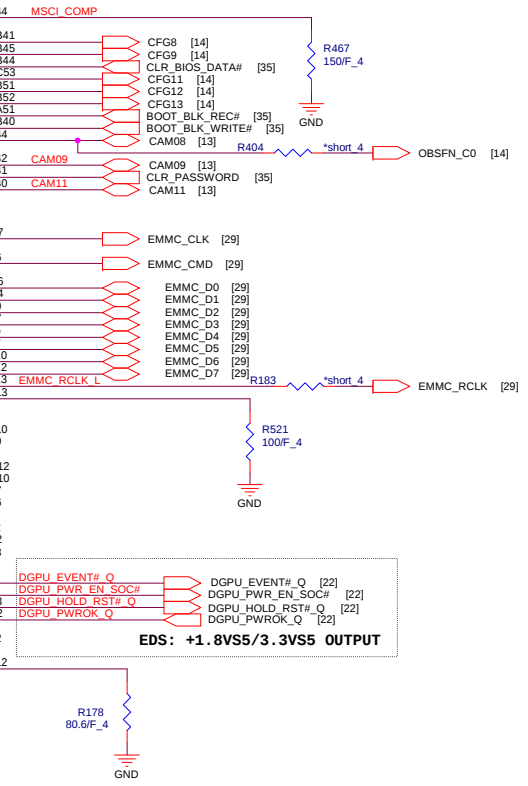
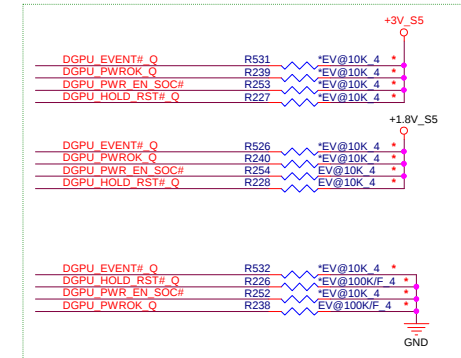
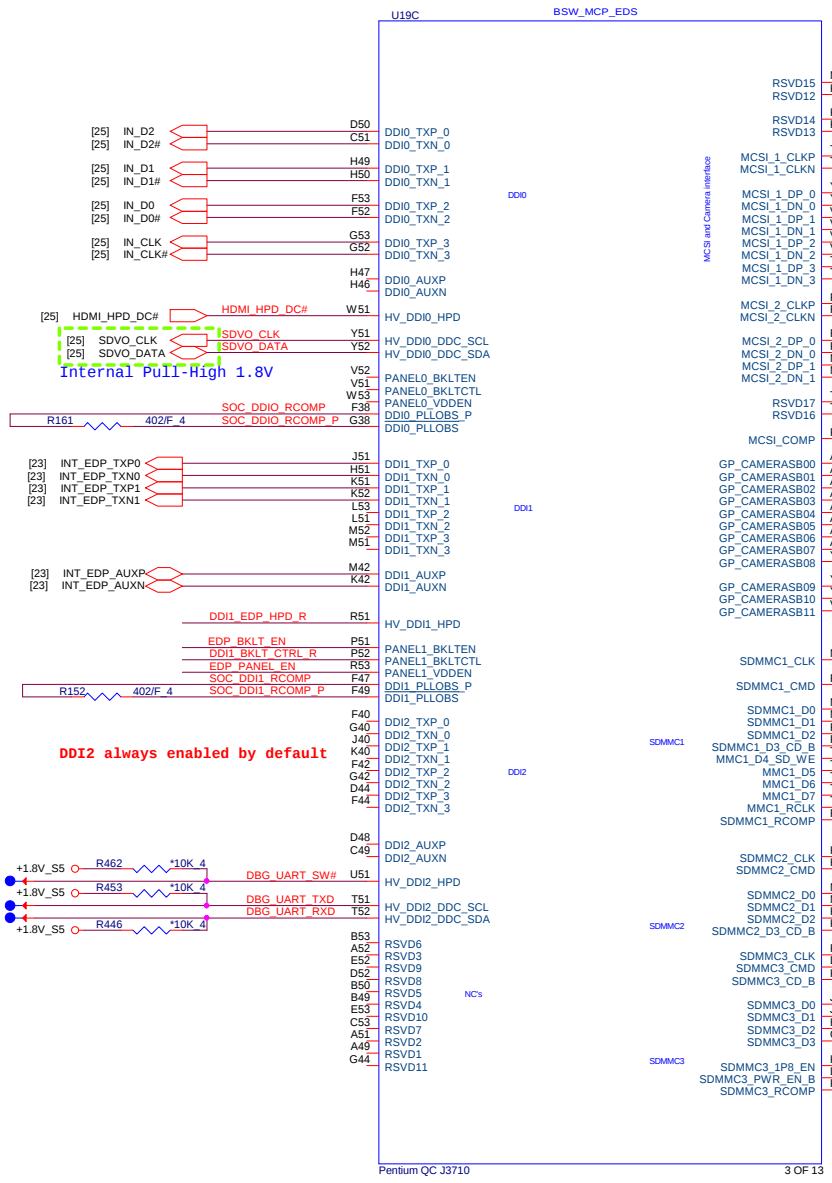
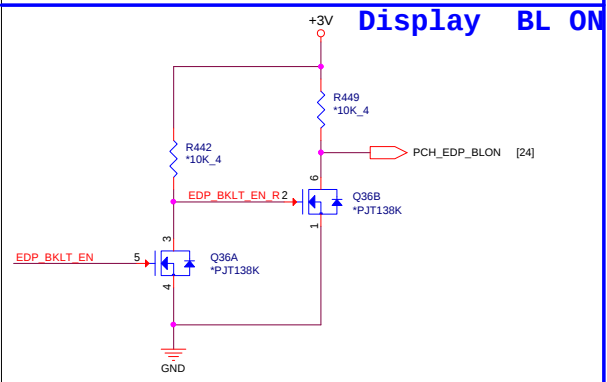
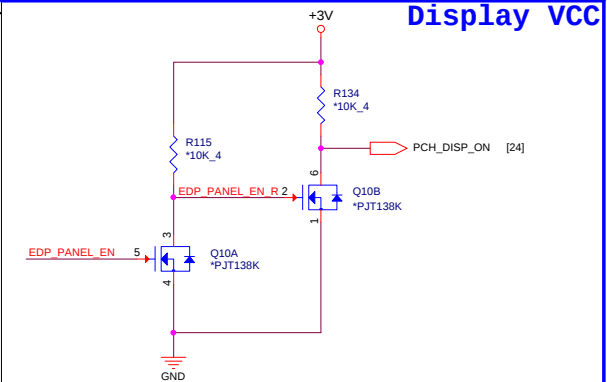
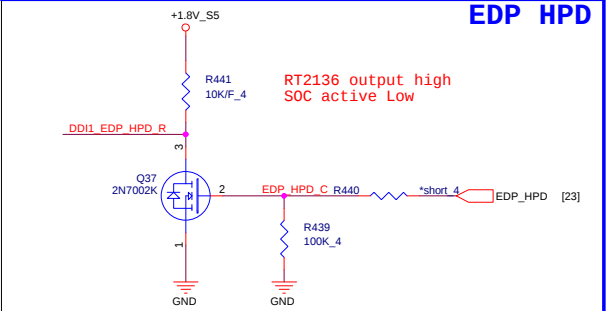
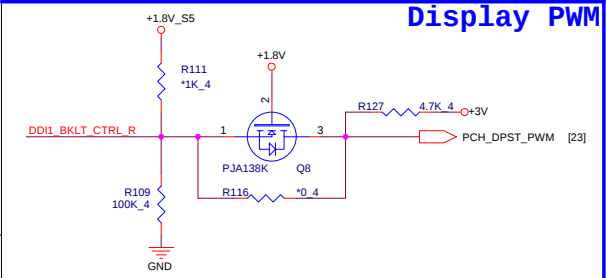


VREF signals are not used for  
DDR3L designs.

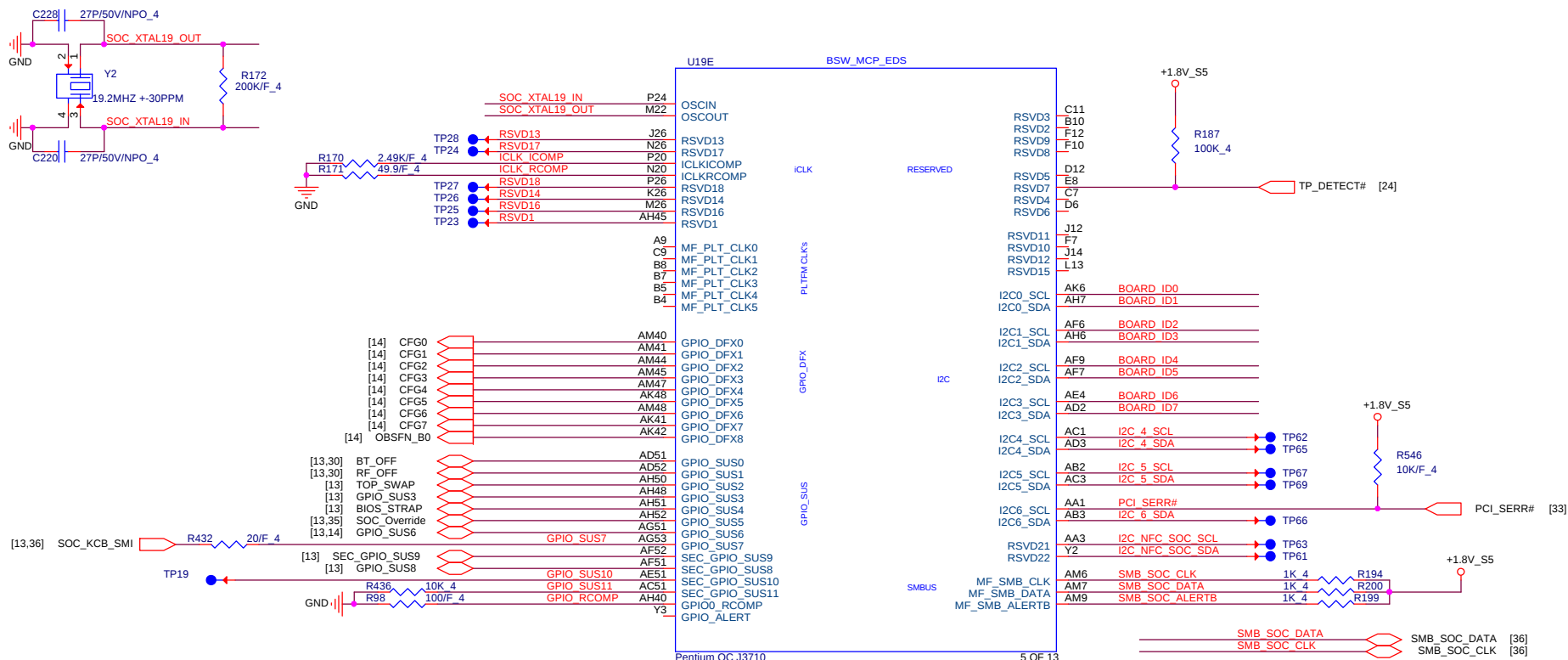


[3,5,6,11,14,22,24,27,30,31,32,33,35,36,37,38,40,41,42,43,44,48] +1.35V\_S3  
+3V\_S5

HP Restricted Secret

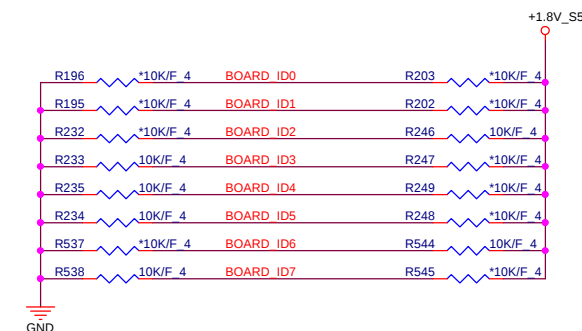


|                                |                                                  |           |
|--------------------------------|--------------------------------------------------|-----------|
| Size<br>Custom                 | Document Number<br><b>Braswell (SP/PC/SA/AU)</b> | Rev<br>1A |
| Date: Monday, January 18, 2016 | Sheet 6 of 54                                    |           |



## BOARD ID SETTING

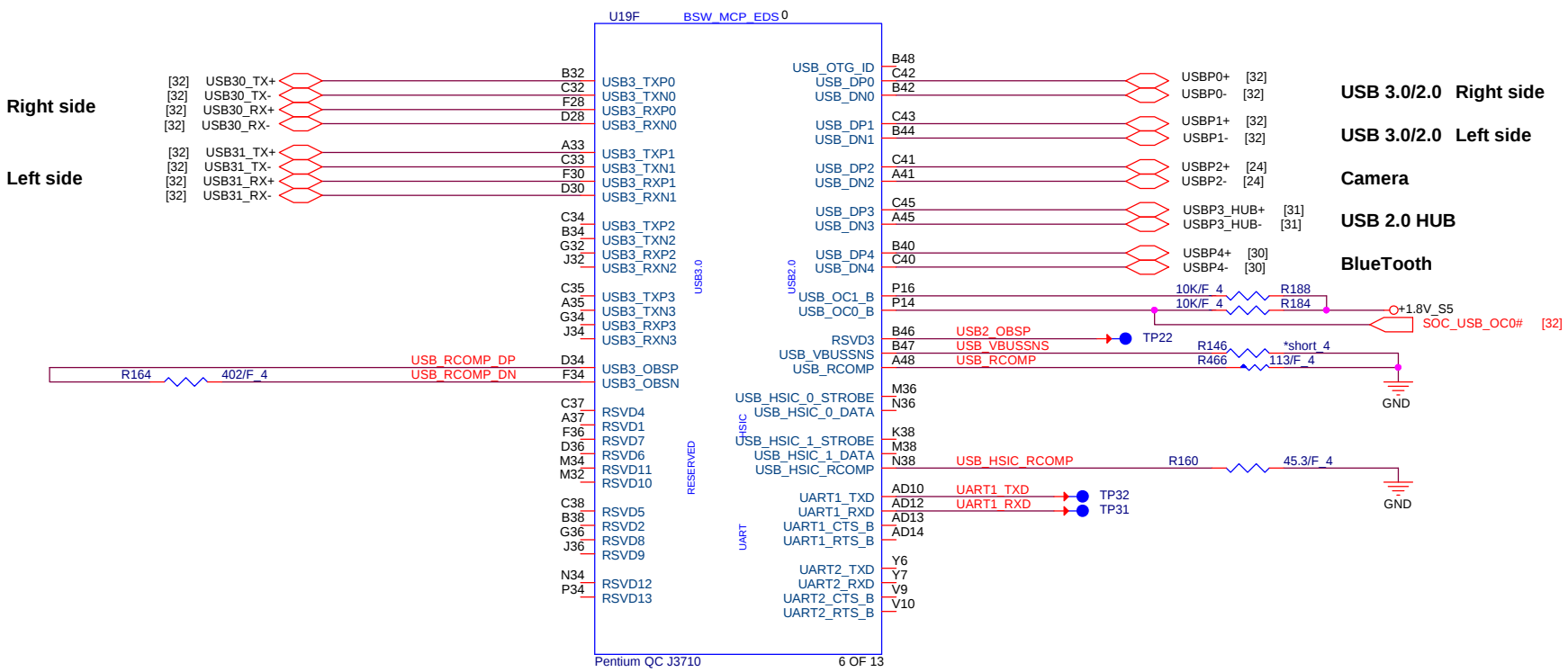
| Board ID<br>(Default = 00) |           |           | Board ID<br>(Default = 00) |           |           | Board ID<br>(Default = 00) |           |           |           |           |
|----------------------------|-----------|-----------|----------------------------|-----------|-----------|----------------------------|-----------|-----------|-----------|-----------|
| Model                      | BOARD_ID7 | BOARD_ID6 | eMMC                       | BOARD_ID5 | BOARD_ID4 | VRAM                       | BOARD_ID3 | BOARD_ID2 | BOARD_ID1 | BOARD_ID0 |
| EC-SI-03                   |           |           |                            |           |           |                            |           |           |           |           |
| All EVT                    | 0         | 0         | W/O                        | 0         | 0         | UMA                        | 0         | 0         |           |           |
| All DVT                    | 0         | 1         | Hynix                      | 0         | 1         | Hynix                      | 0         | 1         |           |           |
| PVT1                       | 1         | 0         | Samsung                    | 1         | 0         | Mircon                     | 1         | 0         |           |           |
| PVT2+                      | 1         | 1         | Reserved                   | 1         | 1         | Reserved                   | 1         | 1         |           |           |
| MVB,A                      | 0         | 0         |                            |           |           |                            |           |           |           |           |
| 1st Major ECN              | 0         | 1         |                            |           |           |                            |           |           |           |           |
| 2nd Major ECN              | 1         | 0         |                            |           |           |                            |           |           |           |           |
| 3rd Major ECN              | 1         | 1         |                            |           |           |                            |           |           |           |           |

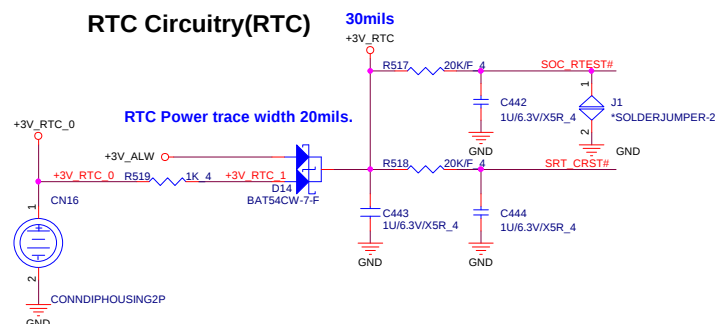
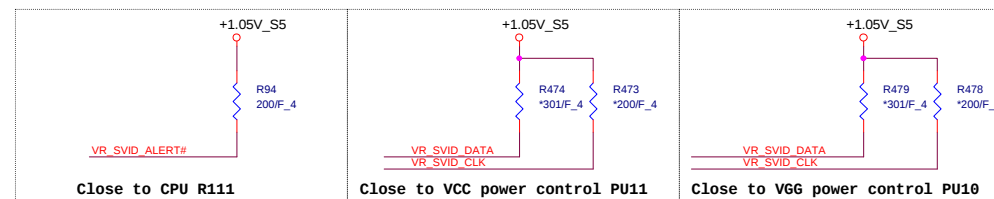
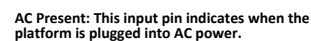
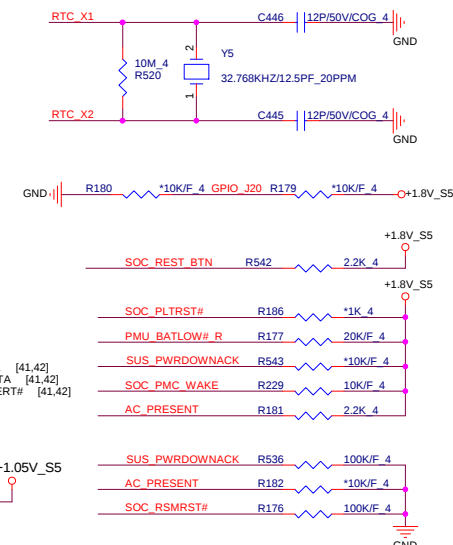


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**Quanta Computer Inc.**  
PROJECT: HP-MoIokai

Size Custom Document Number Braswell (I2C/GPIO/CLK) Rev 2A  
Date: Monday, January 18, 2016 Sheet 7 of 54





HP Restricted Secret

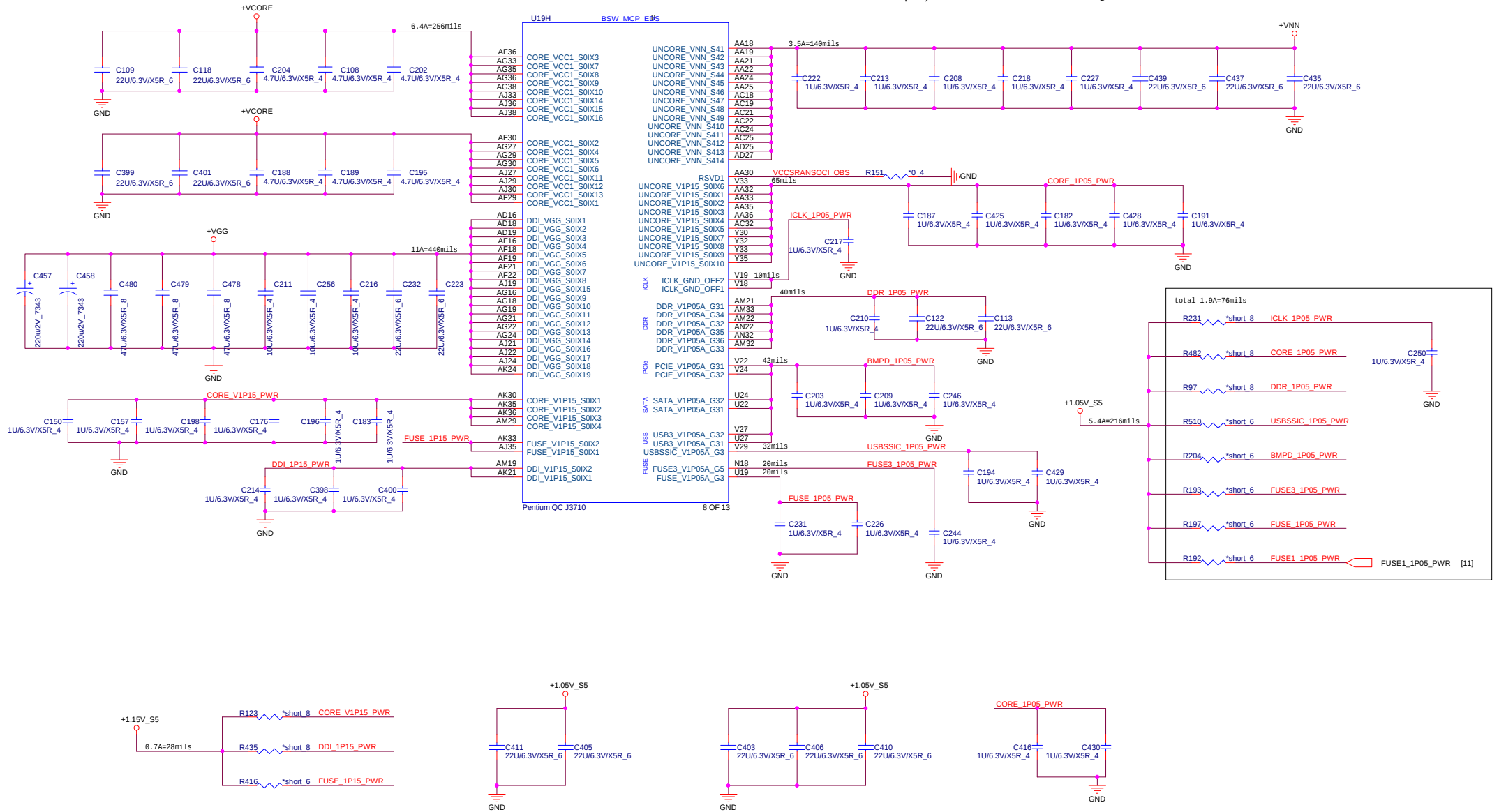


**Quanta Computer Inc.**

**PROJECT: HP-Molokai**

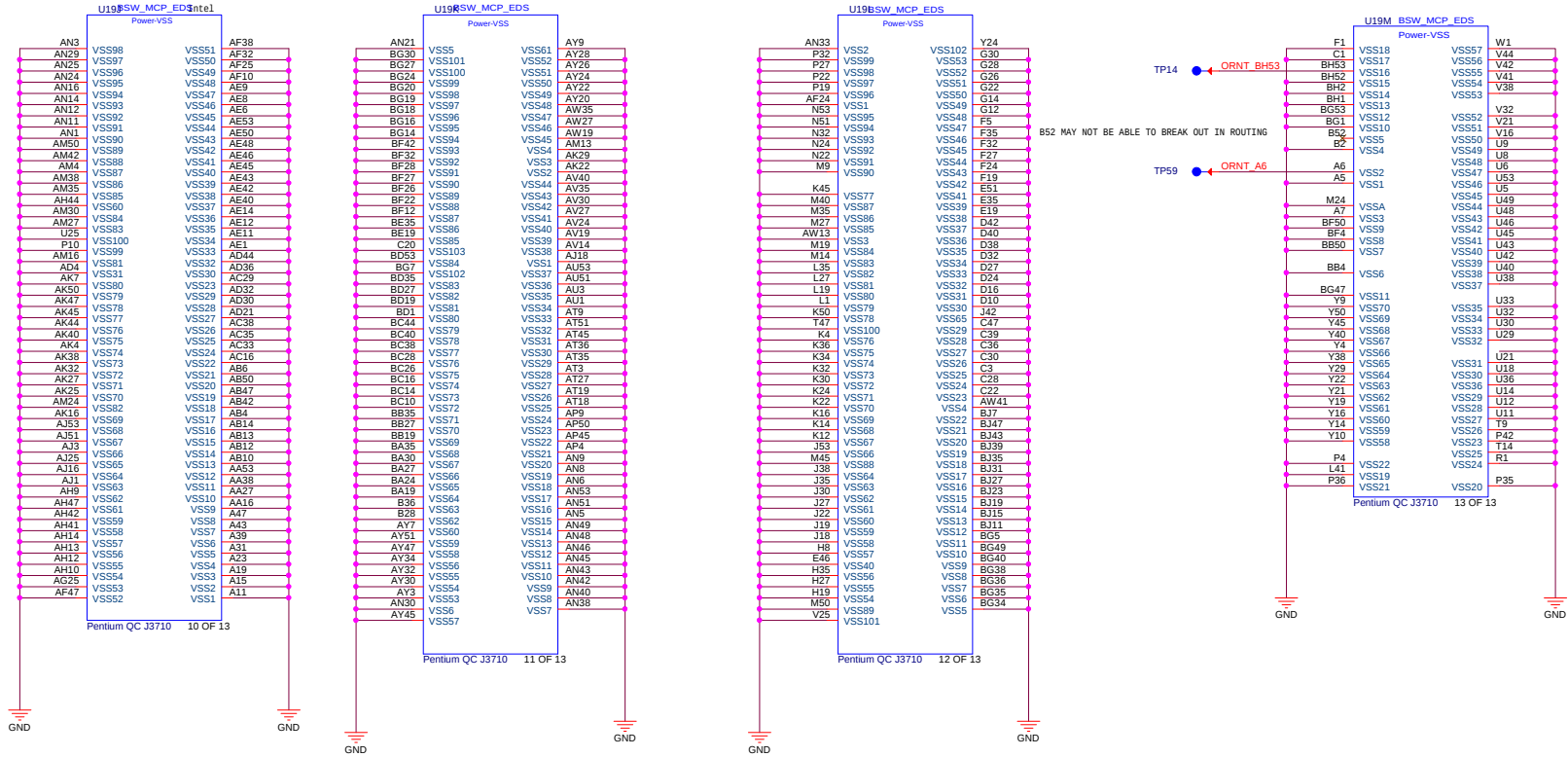
|                |                                                  |               |
|----------------|--------------------------------------------------|---------------|
| Size<br>Custom | Document Number<br><b>Braswell (RTC/LPC/PMU)</b> | Rev<br>1A     |
| Date:          | Monday, January 18, 2016                         | Sheet 9 of 54 |

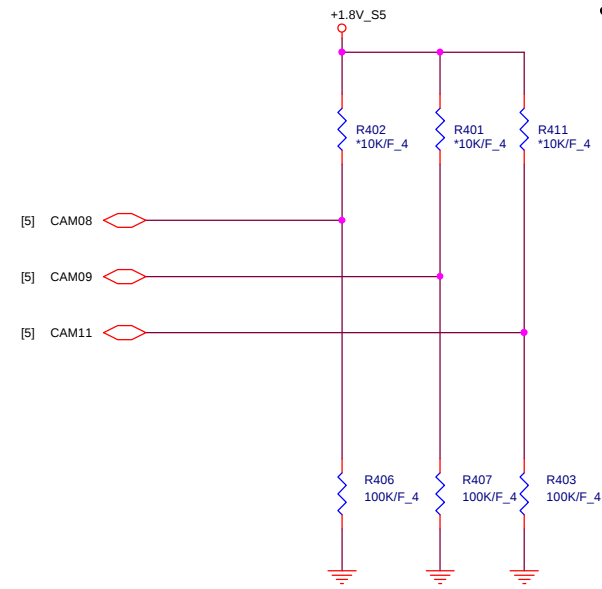
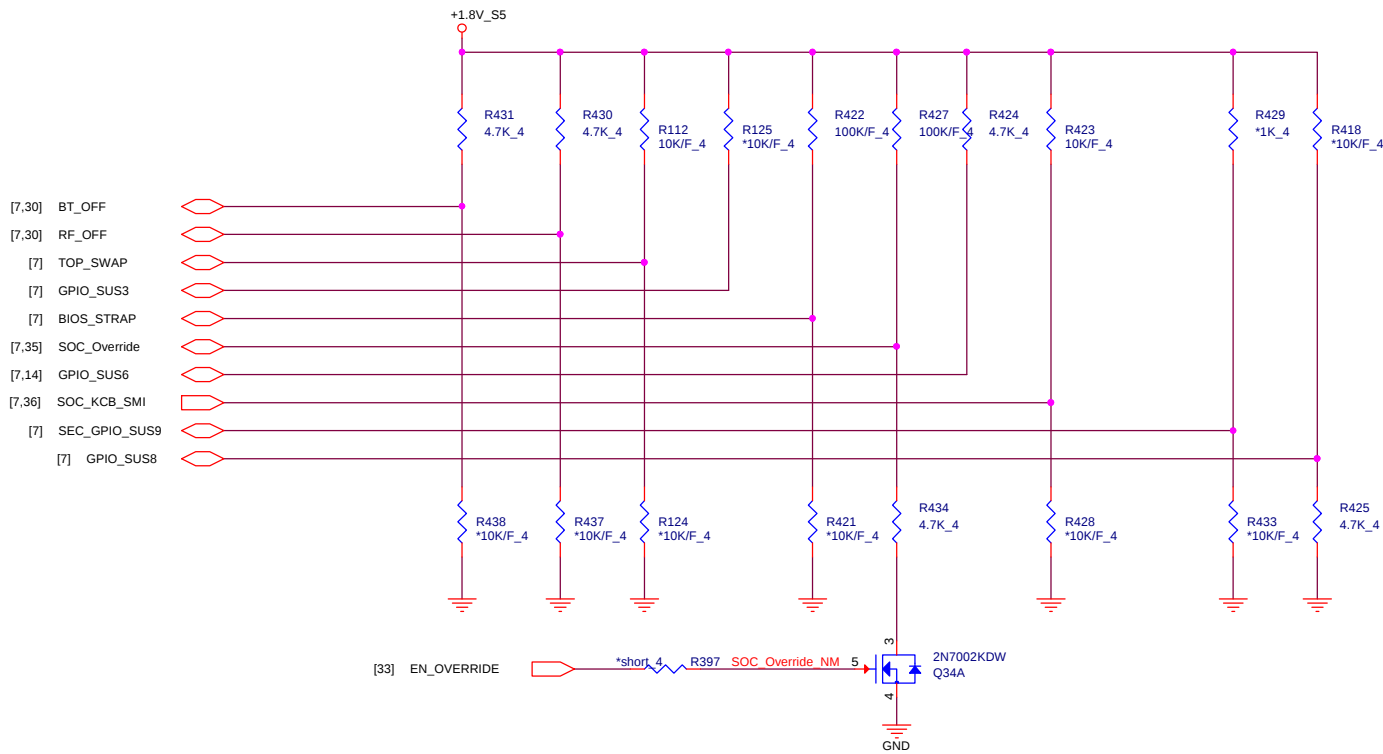
VNN can optionally be merged with V1P05A  
if display resolution is 2560 x1600 @ 60Hz or lower.



HP Restricted Secret







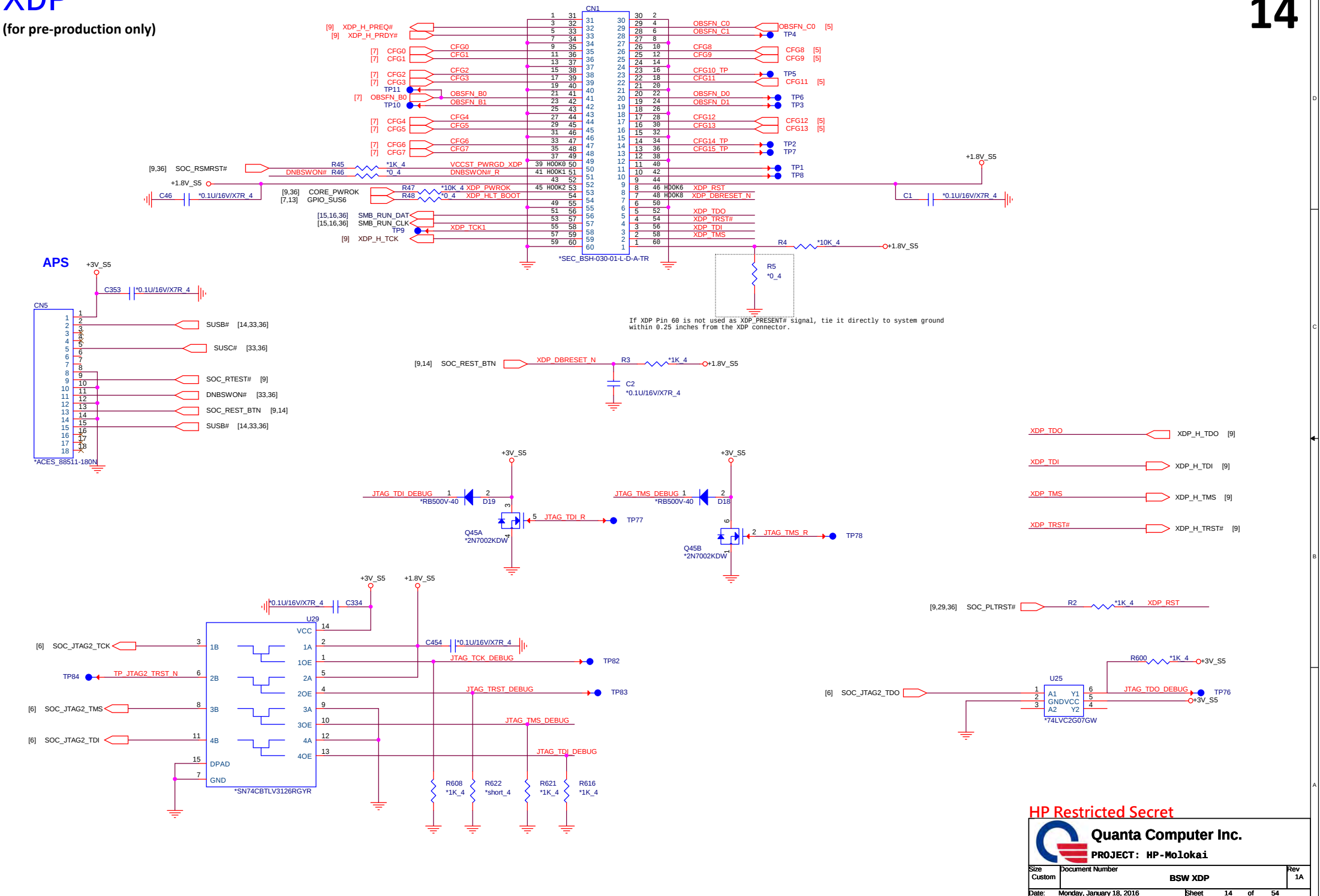
REQUIRED STRAPS

|           | GPIO_SUS0                | GPIO_SUS1                | TOP_SWAP                    | GPIO_SUS3                   | BIOS_STRAP     | SOC_Override                                      | GPIO_SUS6                   | SOC_KCB_SMI                 | GPIO_SUS8                  |
|-----------|--------------------------|--------------------------|-----------------------------|-----------------------------|----------------|---------------------------------------------------|-----------------------------|-----------------------------|----------------------------|
| PULL HIGH | DDI0 detected<br>DEFAULT | DDI1 detected<br>DEFAULT | Normal Operation<br>DEFAULT | Reserve 10 KΩ PU<br>DEFAULT | SPI<br>DEFAULT | Normal Operation<br>DEFAULT<br>20150209 PV change | 10 KΩ PU to 1.8V<br>DEFAULT | Reserve 10 KΩ PU<br>DEFAULT | Supply is 1.35V            |
| PULL LOW  | DDI0 not detected        | DDI1 not detected        | Change Boot Loader address  |                             | LPC            | Override                                          |                             |                             | Supply is 1.25V<br>DEFAULT |

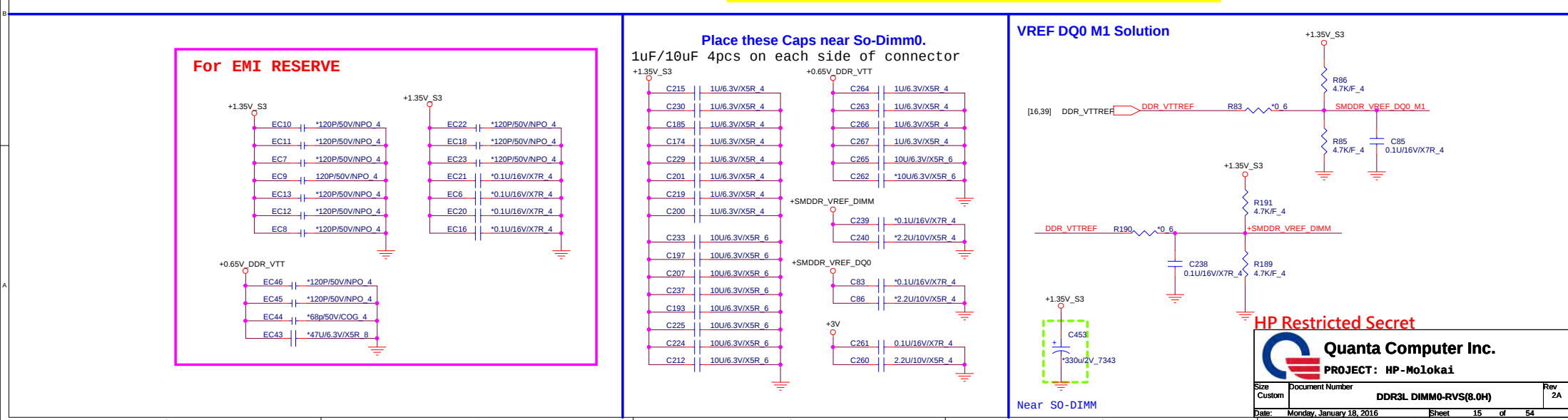
|           | CAM08                              | CAM09                           | CAM11                        |
|-----------|------------------------------------|---------------------------------|------------------------------|
| PULL HIGH | ICLK Xtal OSC Bypass               | CCU SUS RO Bypass               | RTC OSC Bypass               |
| PULL LOW  | ICLK Xtal OSC No Bypass<br>DEFAULT | CCU SUS RO No Bypass<br>DEFAULT | RTC OSC No Bypass<br>DEFAULT |

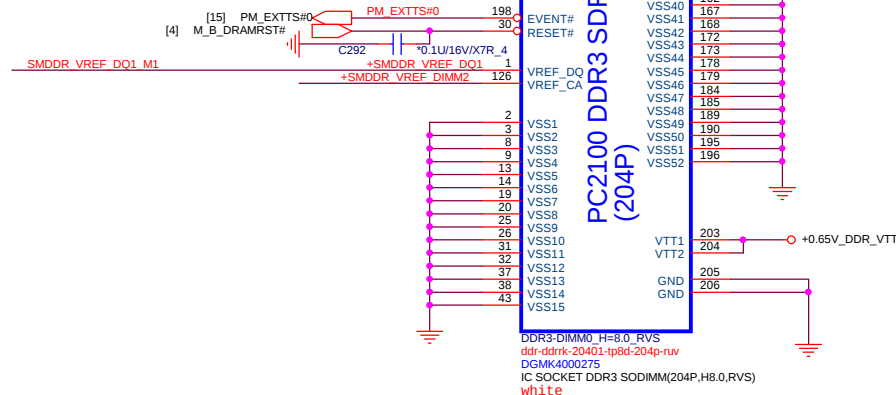
# XDP

**(for pre-production only)**

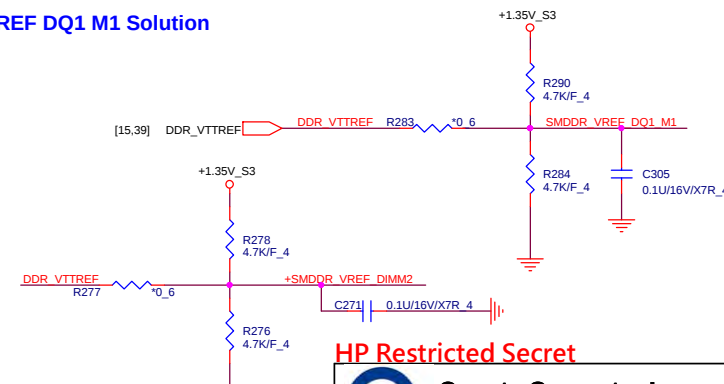


|                                                                                                                   |                                   |          |           |
|-------------------------------------------------------------------------------------------------------------------|-----------------------------------|----------|-----------|
| <b>HP Restricted Secret</b>                                                                                       |                                   |          |           |
|  <b>Quanta Computer Inc.</b> |                                   |          |           |
| <b>PROJECT: HP-Molokai</b>                                                                                        |                                   |          |           |
| Size<br>Custom                                                                                                    | Document Number<br><b>BSW XDP</b> |          | Rev<br>1A |
| Date: Monday, January 18, 2016                                                                                    | Sheet                             | 14 of 54 |           |



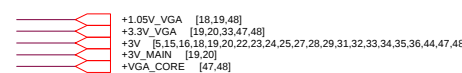
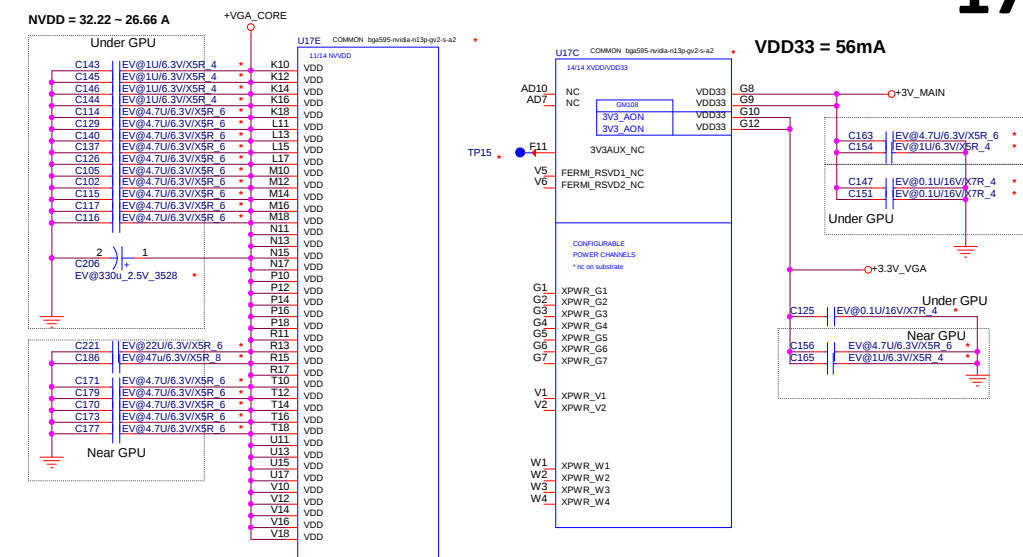


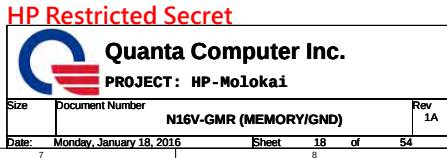
VREF DQ1 M1 Solution



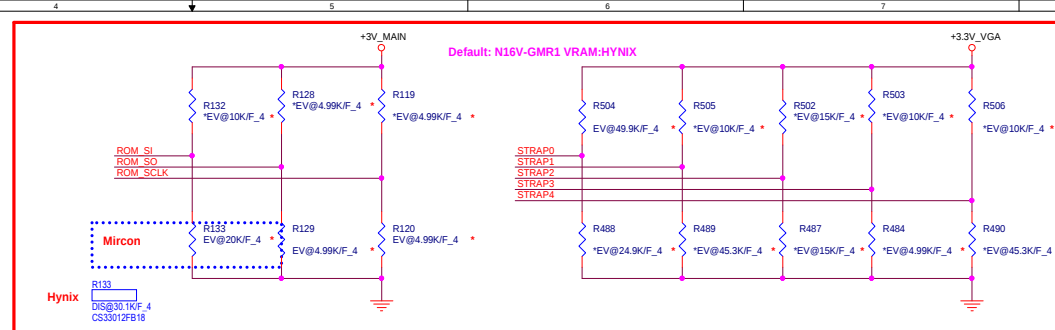
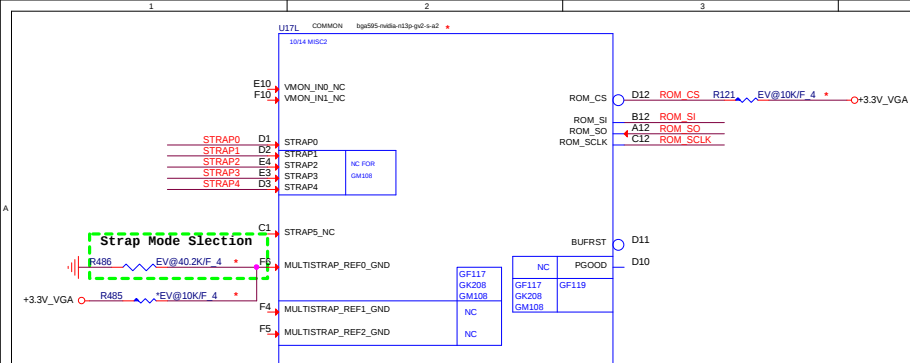
**PROJECT: HP-Molokai**

|                |                                                 |                |
|----------------|-------------------------------------------------|----------------|
| Size<br>Custom | Document Number<br><b>DDR3L DIMM1-RVS(8.0H)</b> | Rev<br>1A      |
| Date:          | Monday, January 18, 2016                        | Sheet 16 of 54 |









## N16S-GT DID=0x1347

GB2B-64

ROM\_SCLK = Stuff 4.99K pull down  
 ROM\_SO = Stuff 4.99K pull down  
 STRAP0 = Stuff 49.9K pull up  
 STRAP1 = NC  
 STRAP2 = NC  
 STRAP3 = NC  
 STRAP4 = NC  
 ROM\_SI = VRAM Configuration follow below table

## N16V-GM DID=0x1299

GB2-64

ROM\_SCLK = Stuff 4.99K pull up  
 ROM\_SO = Stuff 4.99K pull up  
 STRAP0 = Stuff 45.3k pull up. (EDID Panel)  
 STRAP1 = Stuff 4.99k pull down. (Gen3 support)  
 STRAP2 = Stuff 10k pull up. (DID 0x1299)  
 STRAP3 = Stuff 4.99k pull down. (No display out)  
 STRAP4 = Stuff 45.3k pull down. (Gen3/max speed)  
 ROM\_SI = VRAM Configuration follow below table

## N16V-GL DID=0x129A

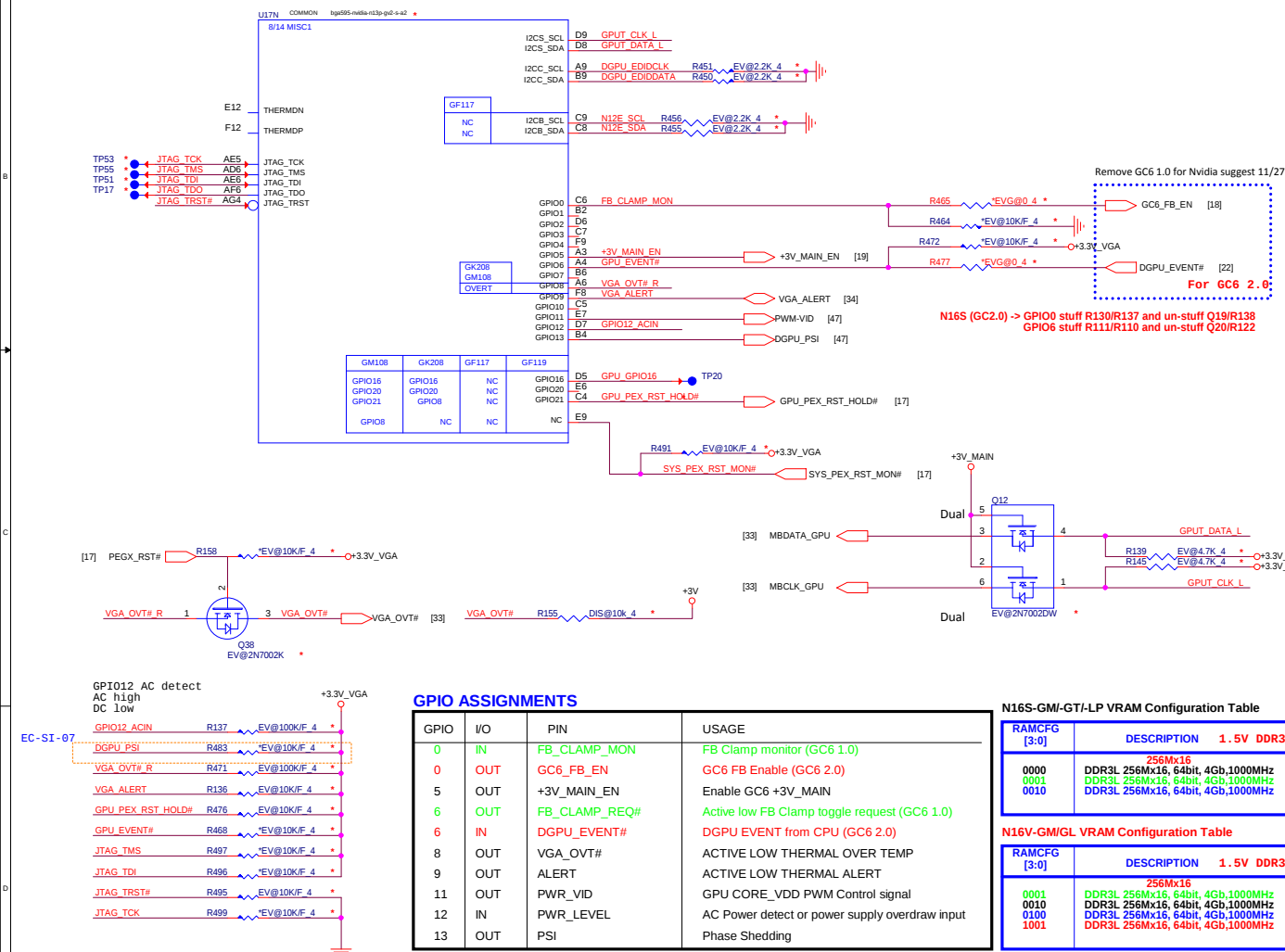
GB2-64

ROM\_SCLK = Stuff 4.99K pull up  
 ROM\_SO = Stuff 4.99K pull up  
 STRAP0 = Stuff 45.3k pull up. (EDID Panel)  
 STRAP1 = Stuff 4.99k pull down. (Gen3 support)  
 STRAP2 = Stuff 15k pull up. (DID 0x129A)  
 STRAP3 = Stuff 4.99k pull down. (No display out)  
 STRAP4 = Stuff 45.3k pull down. (Gen3/max speed)  
 ROM\_SI = VRAM Configuration follow below table

Note: GC6 2.0 is supported by N16x GPU in the GB2B, GB4B-128, and GB3B-256 packages.

### Logical Strap Bit Mapping

|       | PU-VDD | PD   | QCI P/N     |
|-------|--------|------|-------------|
| 4.99K | 1000   | 0000 | CS24992FB26 |
| 10K   | 1001   | 0001 | CS31002FB26 |
| 15K   | 1010   | 0010 | CS31502FB24 |
| 20K   | 1011   | 0011 | CS32002FB29 |
| 24.9K | 1100   | 0100 | CS32492FB16 |
| 30.1K | 1101   | 0101 | CS33012FB18 |
| 34.8K | 1110   | 0110 | CS33482FB06 |
| 45.3K | 1111   | 0111 | CS34532FB18 |



N16S-GM-GT/LP VRAM Configuration Table

ROM\_SI

| RAMCFG [3:0] | DESCRIPTION | 1.5V DDR3                          | Vendor  | Vendor P/N           | ROM_SI      | STN B/S     | Configuration                                     |
|--------------|-------------|------------------------------------|---------|----------------------|-------------|-------------|---------------------------------------------------|
| 0000         | 256Mx16     | DDR3L 256Mx16, 64bit, 4Gb, 1000MHz | HYNIX   | H5TC4663AFR-11C      | PD 4.9K ohm | AKD5P6WTW13 | Single Rank or Single Rank stuffing for Dual Rank |
| 0001         | 256Mx16     | DDR3L 256Mx16, 64bit, 4Gb, 1000MHz | MICRON  | MT41J256M16HA-093G:E | PD 10K ohm  | AKD5P2STL05 | Single Rank or Single Rank stuffing for Dual Rank |
| 0010         | 256Mx16     | DDR3L 256Mx16, 64bit, 4Gb, 1000MHz | SAMSUNG | K4W4G1646D-BC1A      | PD 15K ohm  | AKD5P6WT564 | Dual Rank                                         |

N16V-GM/GL VRAM Configuration Table

ROM\_SI

| RAMCFG [3:0] | DESCRIPTION | 1.5V DDR3                          | Vendor  | Vendor PIN           | ROM_SI       | STN B/S     | Configuration                                     |
|--------------|-------------|------------------------------------|---------|----------------------|--------------|-------------|---------------------------------------------------|
| 0001         | 256Mx16     | DDR3L 256Mx16, 64bit, 4Gb, 1000MHz | Micron  | MT41J256M16HA-093G:E | PD 10K ohm   | AKD5P2STL05 | Single Rank or Single Rank stuffing for Dual Rank |
| 0010         | 256Mx16     | DDR3L 256Mx16, 64bit, 4Gb, 1000MHz | HYNIX   | H5TC4663AFR-11C      | PD 15K ohm   | AKD5P6WTW13 | Single Rank or Single Rank stuffing for Dual Rank |
| 0100         | 256Mx16     | DDR3L 256Mx16, 64bit, 4Gb, 1000MHz | SAMSUNG | K4W4G1646D-BC1A      | PD 24.9K ohm | AKD5P6WT564 | Single Rank or Single Rank stuffing for Dual Rank |
| 1001         | 256Mx16     | DDR3L 256Mx16, 64bit, 4Gb, 1000MHz | HYNIX   | H5TC4663CFR-N0C      | PU 10K ohm   | AKD5P2DTW03 | Single Rank or Single Rank stuffing for Dual Rank |

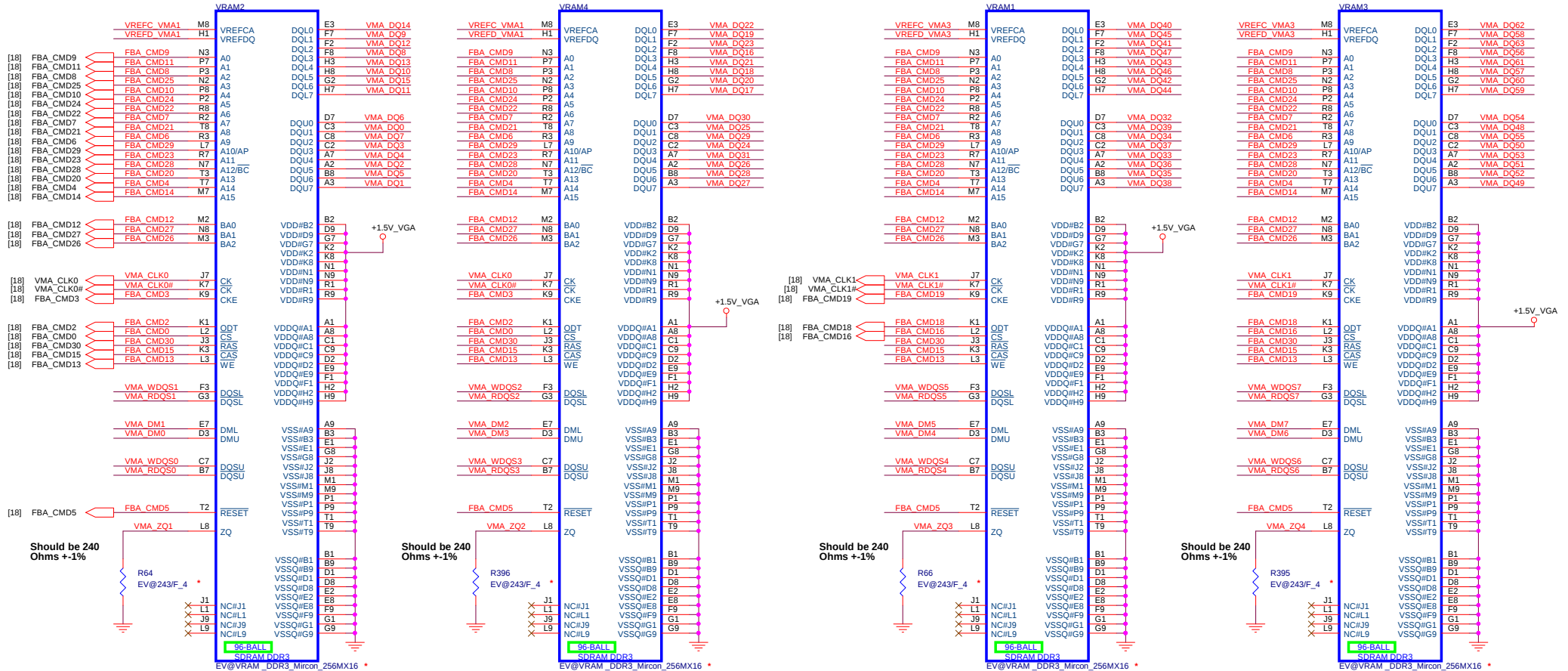
HP Restricted Secret

## CHANNEL A: 2048MB DDR3X16

+1.05V\_VGA [17,18,19,48]  
+1.5V\_VGA [18,48]

[18] VMA\_DQ[63:0]  
[18] VMA\_DM[7:0]  
[18] VMA\_WDQS[7:0]  
[18] VMA\_RDQS[7:0]

HYU 256Mx16, H5TC46G3AFR-11C STN B/S PN : AKD5PGWTW13  
MIC 256Mx16, MT41J256M16HA-093G:E STN B/S PN : AKD5PZTL05  
SAM 256Mx16, K4W4G1646D-BC1A STN B/S PN : AKD5PGWT504



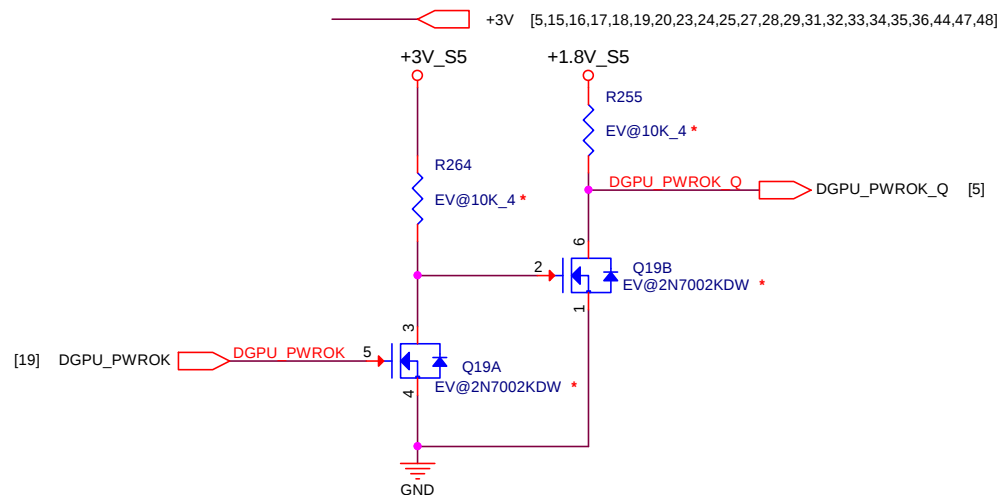
162\_1% ohm  
CS11622FB07 RES CHIP 162 1/16W +-1%(0402)  
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

Fermi : Change to 160 ohm  
1 : CS11602J800 ,RES CHIP 160 1/16W +-5%(0402)  
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

HP Restricted Secret

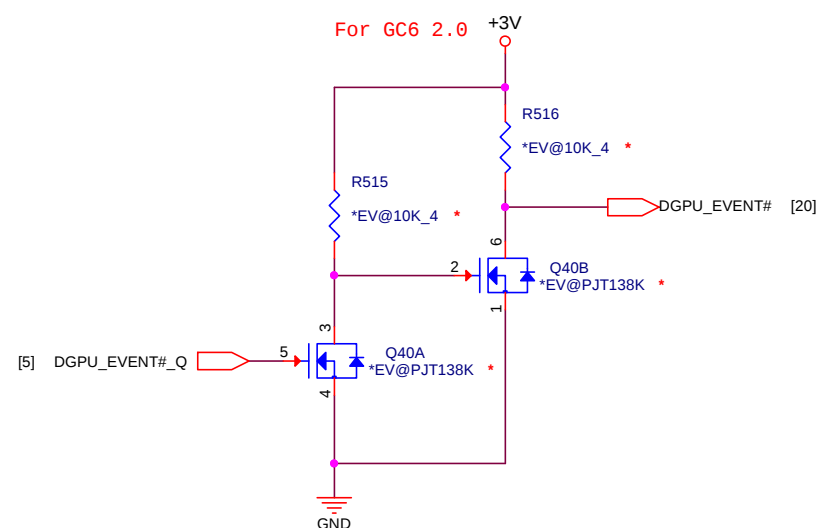
Quanta Computer Inc.  
PROJECT: HP-Molokai

Size Document Number  
N16V-GMR DDR3 VRAM(BGA96)  
Date: Monday, January 18, 2016 Sheet 21 of 54



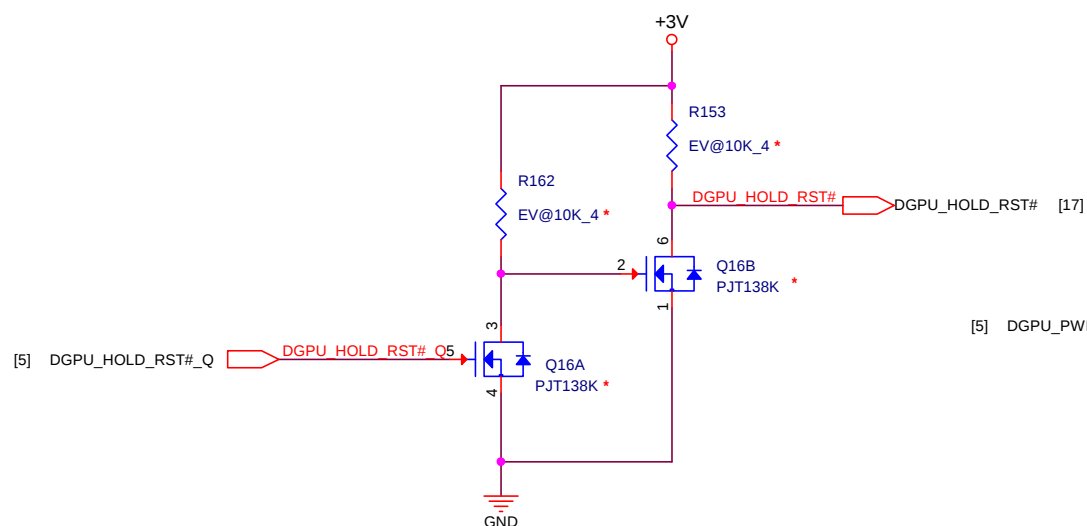
DGPU\_PWROK R257 \*EV@0\_4\* DGPU\_PWROK\_Q

DGPU\_HOLD\_RST#\_Q R154 \*EV@0\_4\* DGPU\_HOLD\_RST#

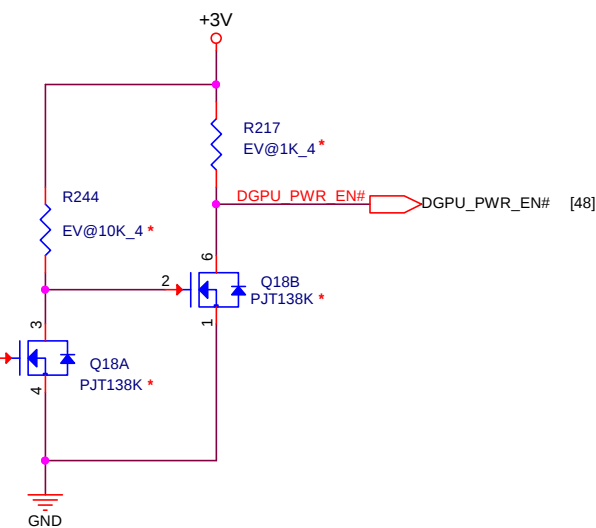


DGPU\_EVENT#\_Q R514 \*EV@0\_4\* DGPU\_EVENT#

DGPU\_PWR\_EN\_SOC# R223 \*EV@0\_4\* DGPU\_PWR\_EN#



[5] DGPU\_PWR\_EN\_SOC# DGPU\_PWR\_EN\_SOC#



HP Restricted Secret

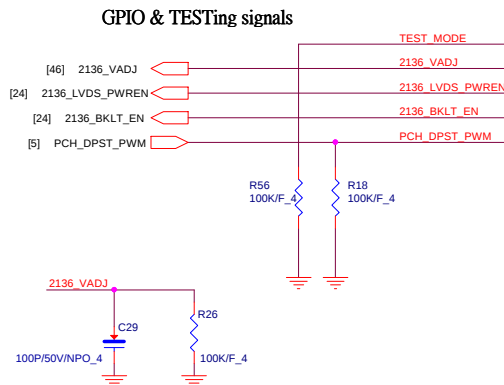
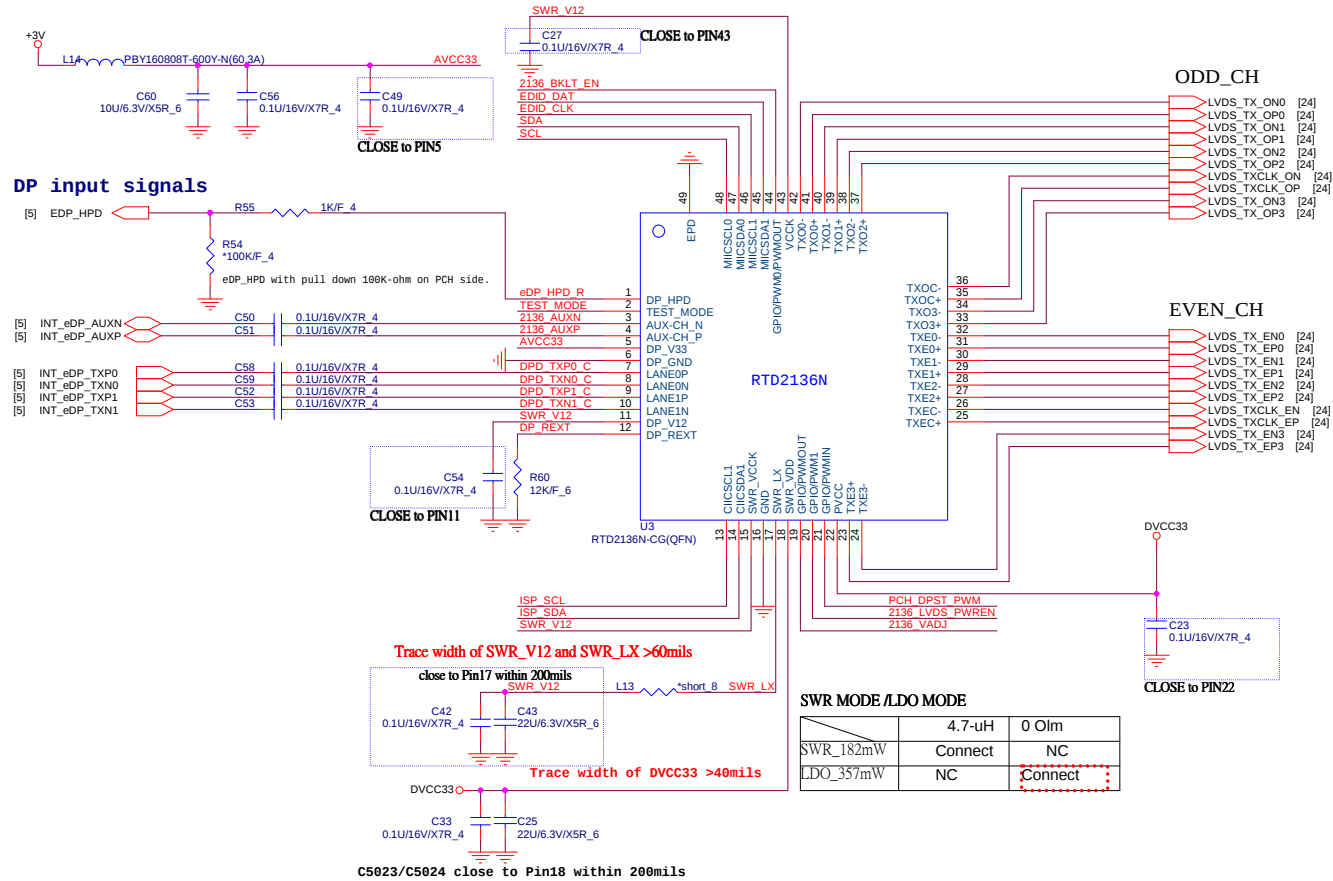
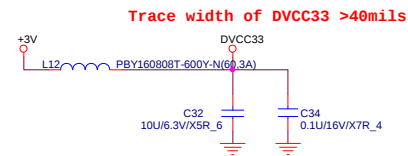


Quanta Computer Inc.

PROJECT: HP-Molokai

|       |                          |                |
|-------|--------------------------|----------------|
| Size  | Document Number          | Rev 1A         |
| Date: | Monday, January 18, 2016 | Sheet 22 of 54 |

dGPU Level Shift

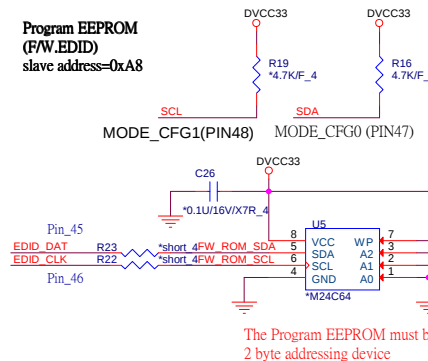


### In System Programming slave address=0xA8

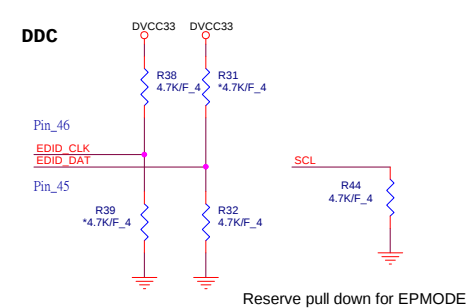


| RTD2136N:<br>Mode Selection | MODE_CFG0 (PIN47) |               |
|-----------------------------|-------------------|---------------|
|                             | 0                 | 1             |
| MODE_CFG1(PIN48)            | 0                 | X             |
|                             | 1                 | ROM ONLY MODE |
|                             |                   | EEPROM MODE   |

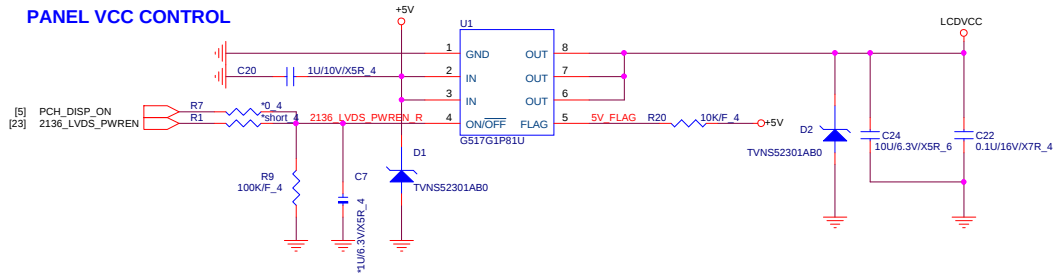
### Program EEPROM (F/W.EDID) slave address=0xA8



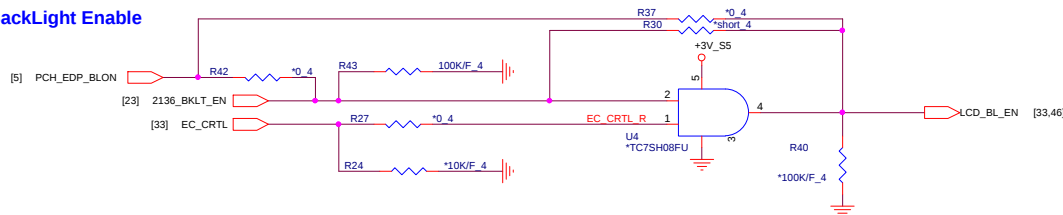
### DDC

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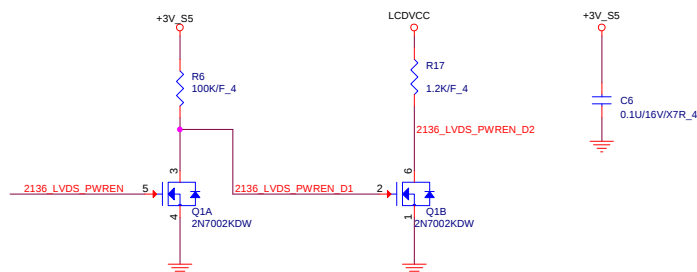
|                                |                                           |           |
|--------------------------------|-------------------------------------------|-----------|
| Size<br>Custom                 | Document Number<br>LVDS converter RTD2136 | Rev<br>1A |
| Date: Monday, January 18, 2016 | Sheet 23 of 54                            |           |



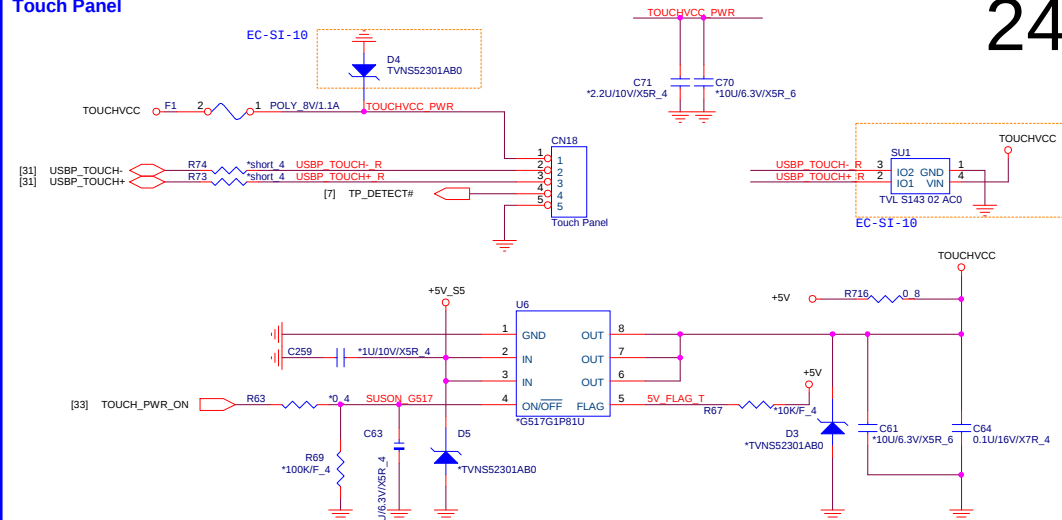
### BackLight Enable



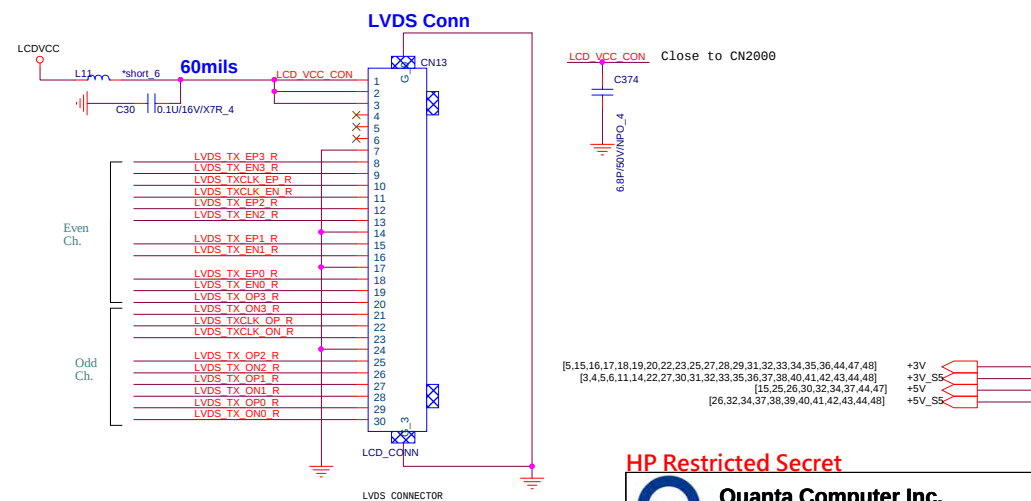
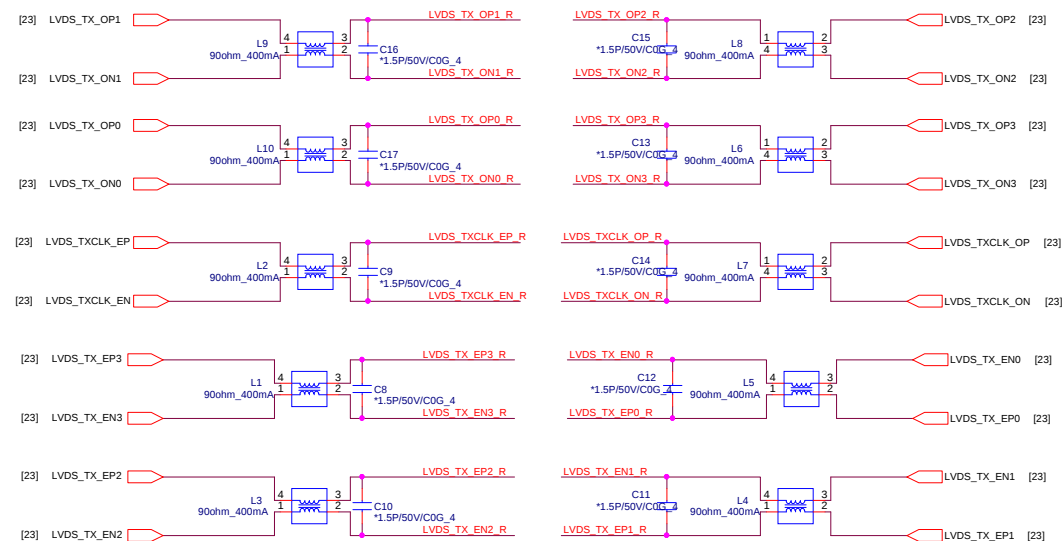
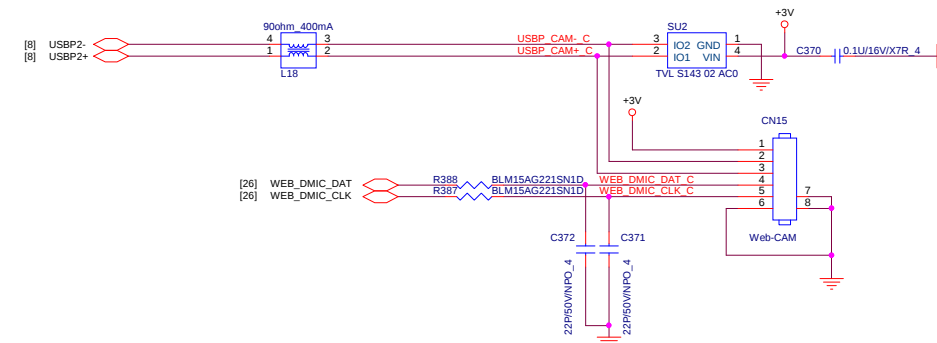
### LCDVCC Discharge Circuit



## Touch Panel



## CCD CONN



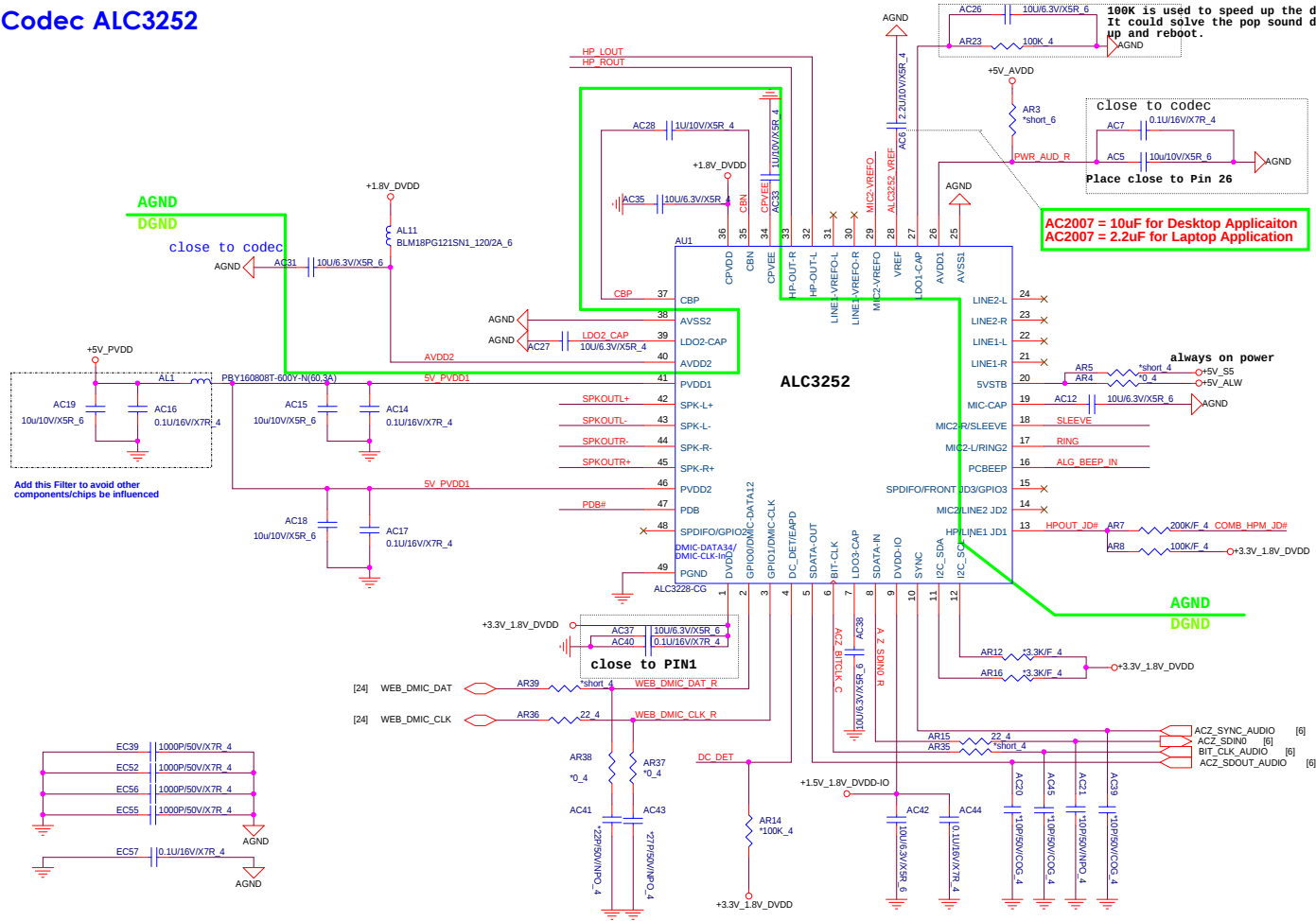
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|                |                                                   |                |
|----------------|---------------------------------------------------|----------------|
| Size<br>Custom | Document Number<br><b>LCD CONN/CCD/TouchPanel</b> | Rev<br>2.      |
| Date:          | Monday, January 25, 2016                          | Sheet 24 of 54 |

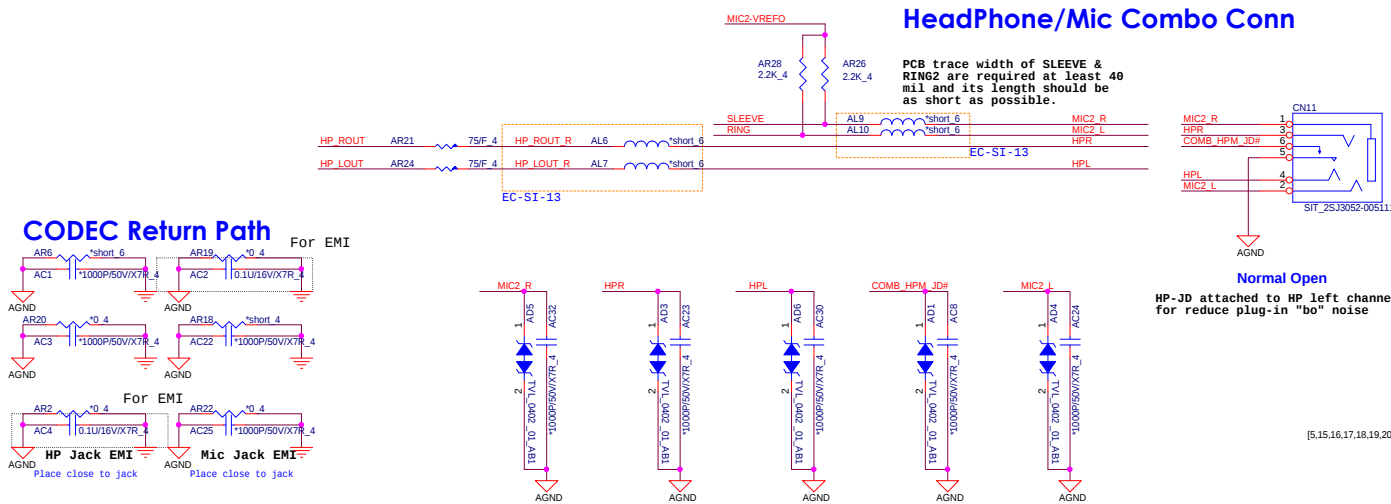


## Codec ALC3252

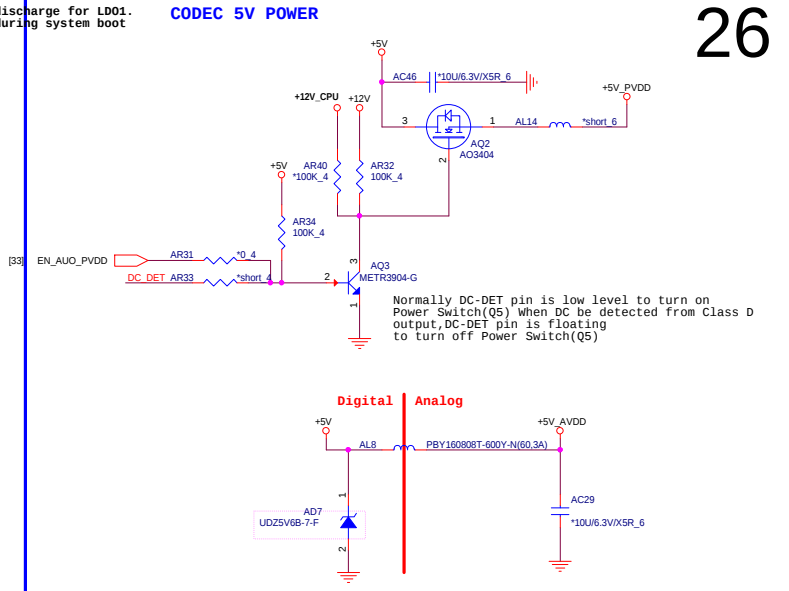


## HeadPhone/Mic Combo Conn

PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possible.

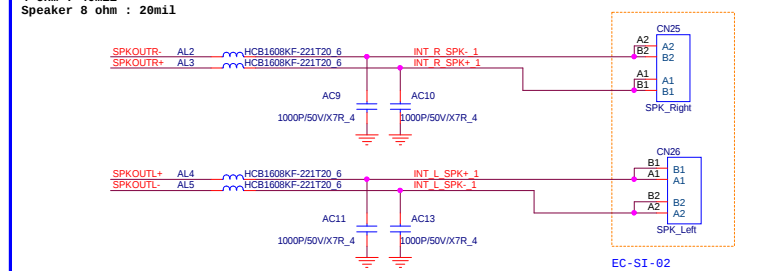


## CODEC 5V POWER

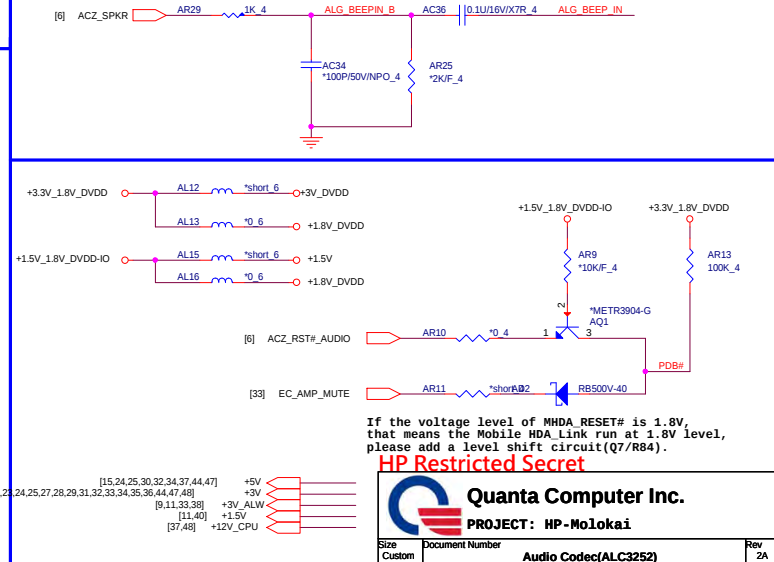


Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-RSpeaker  
4 ohm : 40mil  
Speaker 8 ohm : 20mil

**Internal Speaker (2W, 4 ohm)**

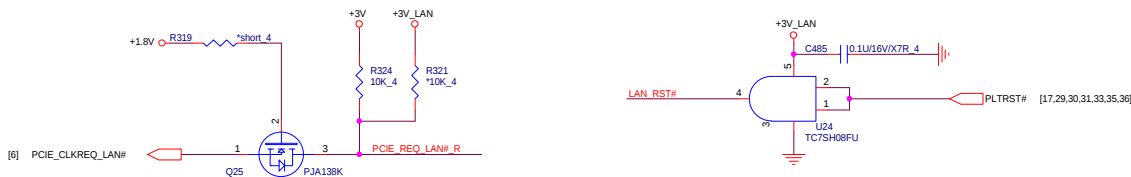
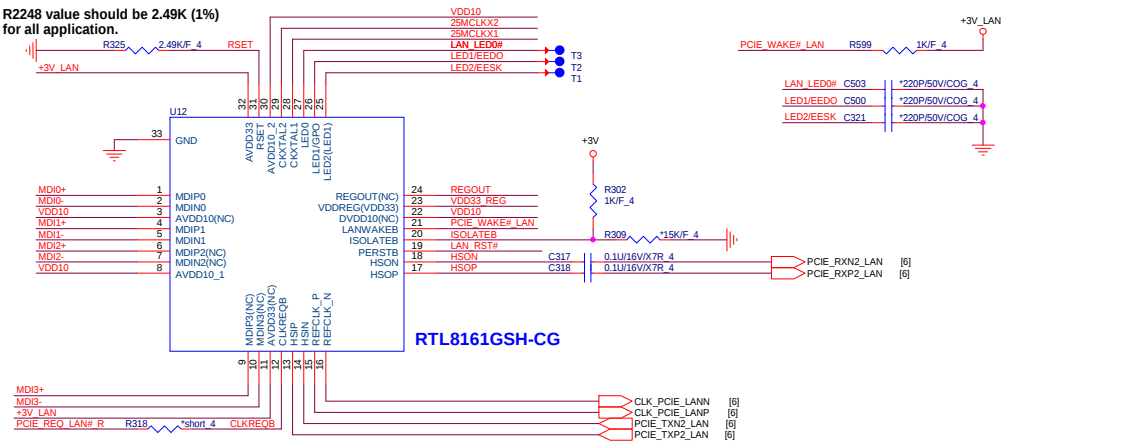


## PC BEEP

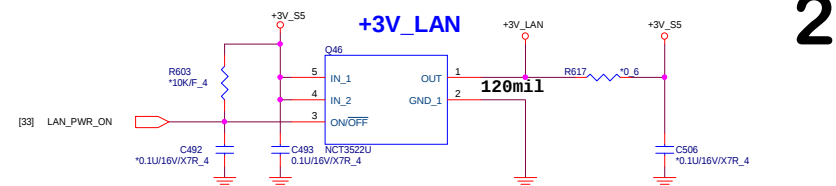
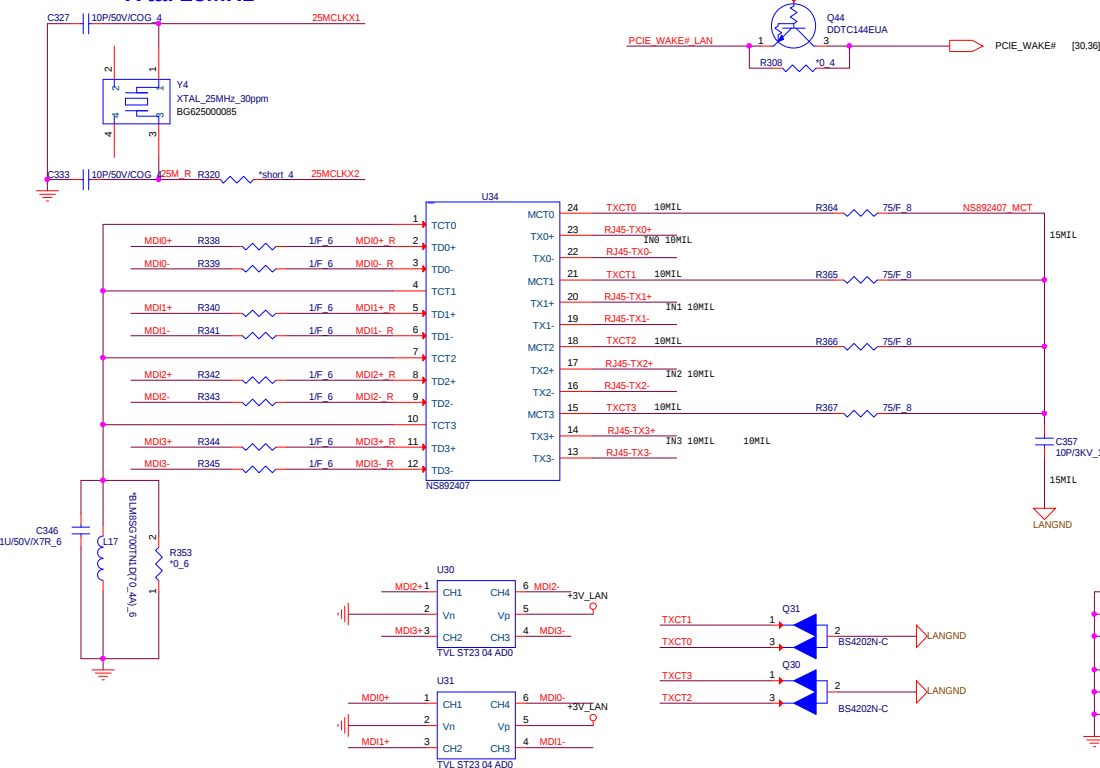


## (RTL8161GSH) 10/100/1000

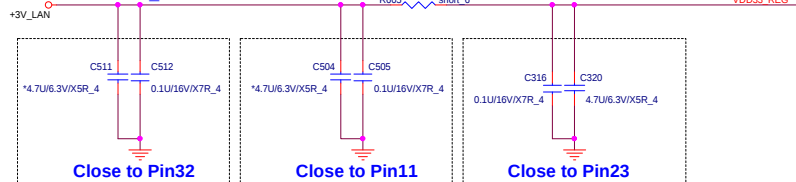
**R2248 value should be 2.49K (1%)  
for all application.**



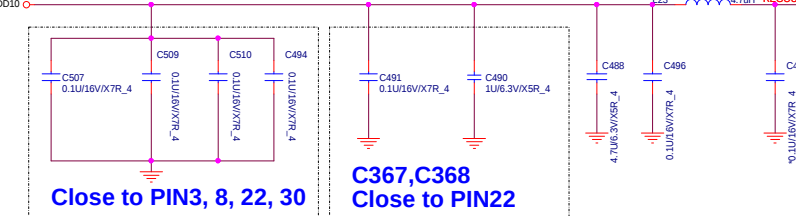
**X'tal 25MHz**



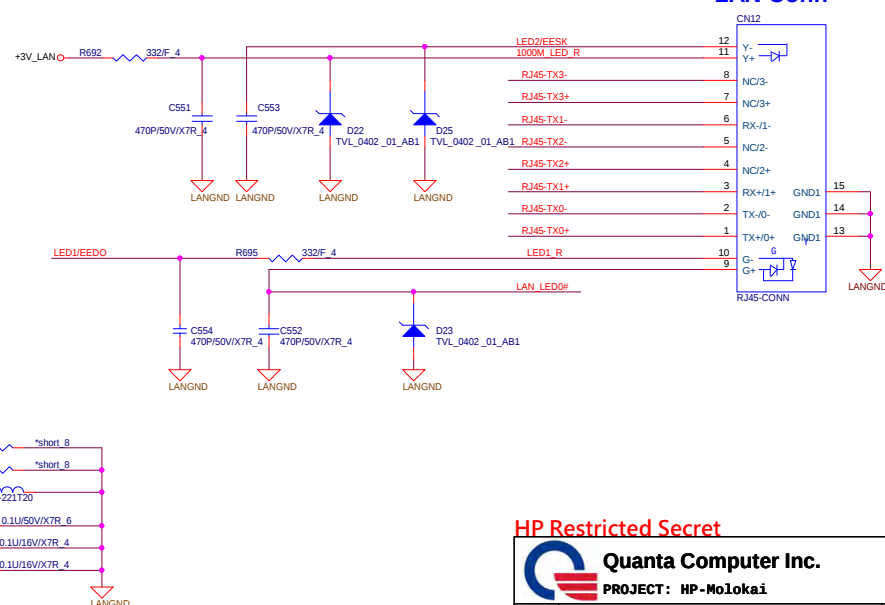
EVDD10/AVDD33\_REG trace width >40mils



EVDD10/N780946/REGOUT trace width >60mils



## LAN Conn



**HP Restricted Secret**

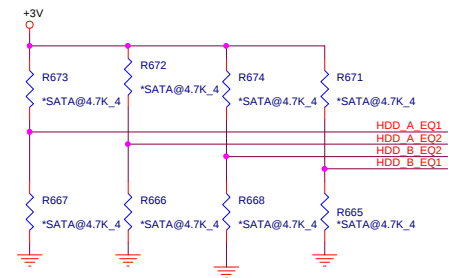
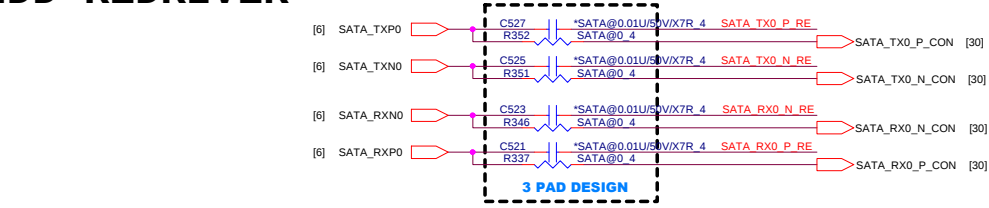
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PROJECT: HP-Molokai

|                                |                                        |           |
|--------------------------------|----------------------------------------|-----------|
| Size<br>Custom                 | Document Number<br><b>RTL8161/RJ45</b> | Rev<br>1A |
| Date: Monday, January 18, 2016 | Sheet 27 of 54                         |           |

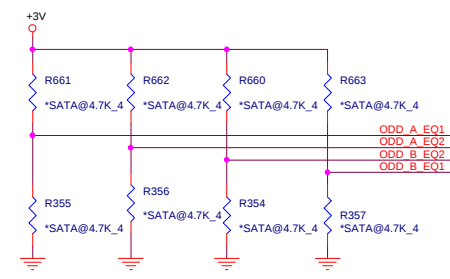
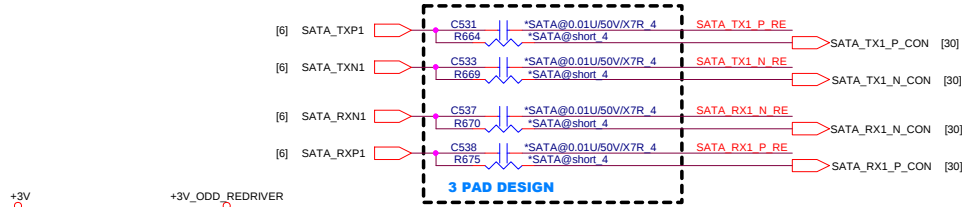
# HDD REDRIVER

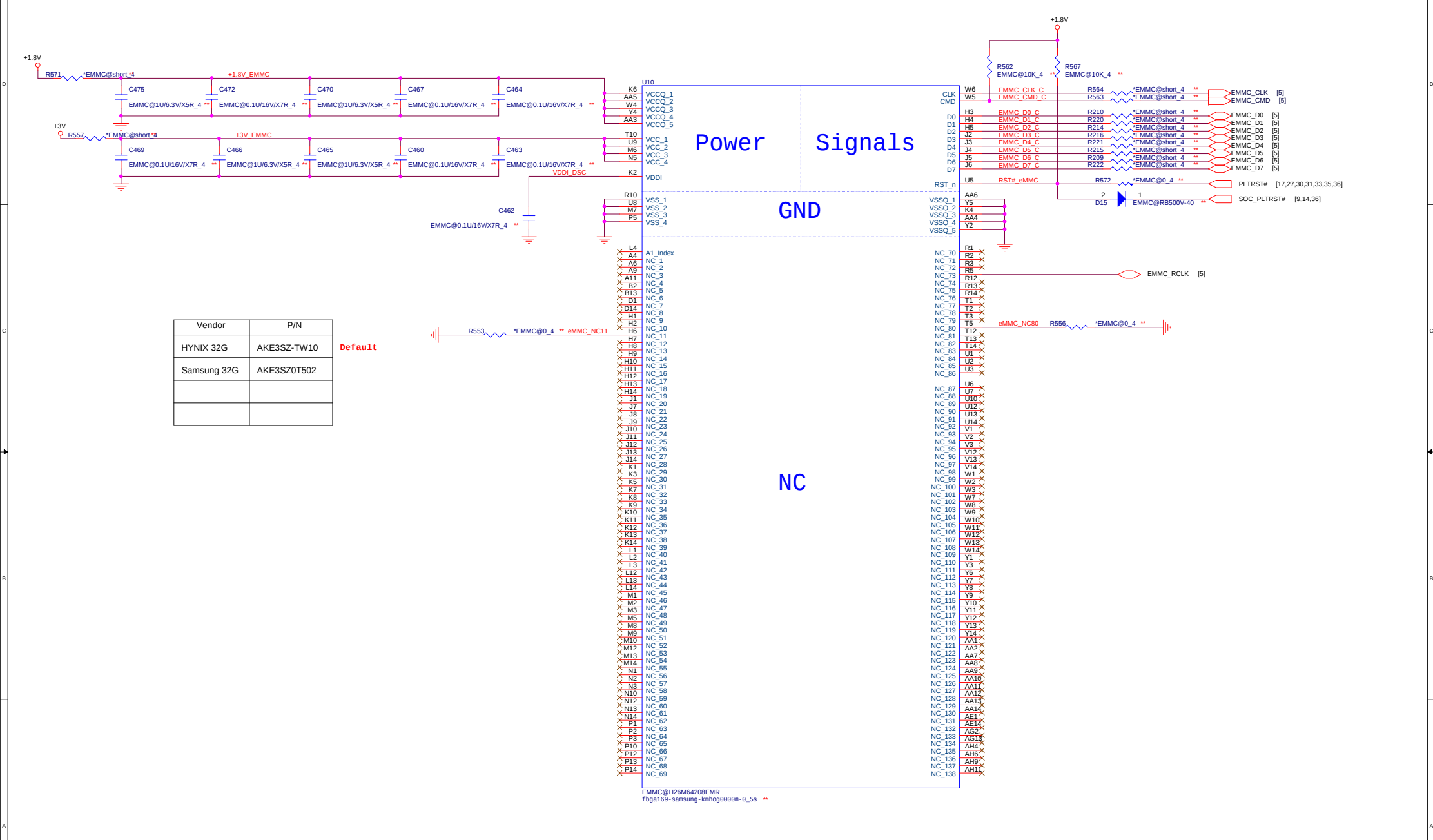
C521,C523,C525,C527 CLOSE TO RE-DRIVER IC



# ODD REDRIVER

C531,C533,C537,C538 CLOSE TO RE-DRIVER IC

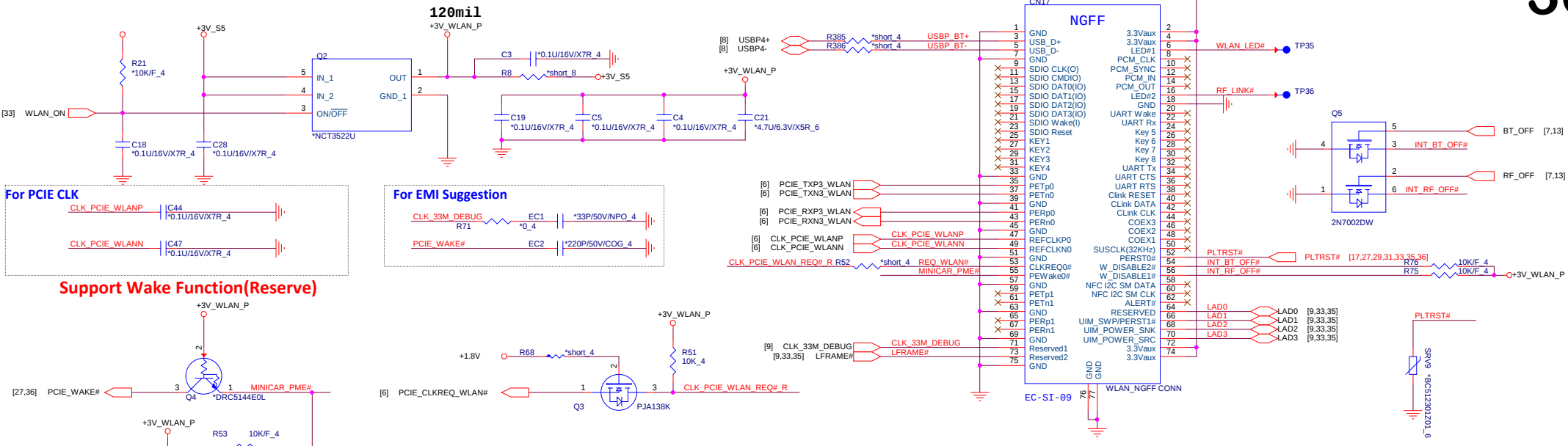




[5,15,16,17,18,19,20,22,23,24,25,27,28,31,32,33,34,35,36,44,47,48]  
[5,6,25,27,30,34,36,40]

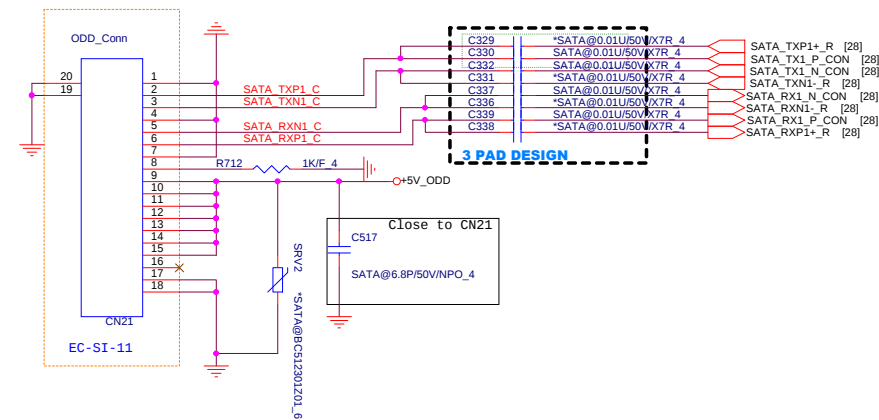
# Mini Card WLAN/BT(Optional) PCIe M.2\_power(S5)

30

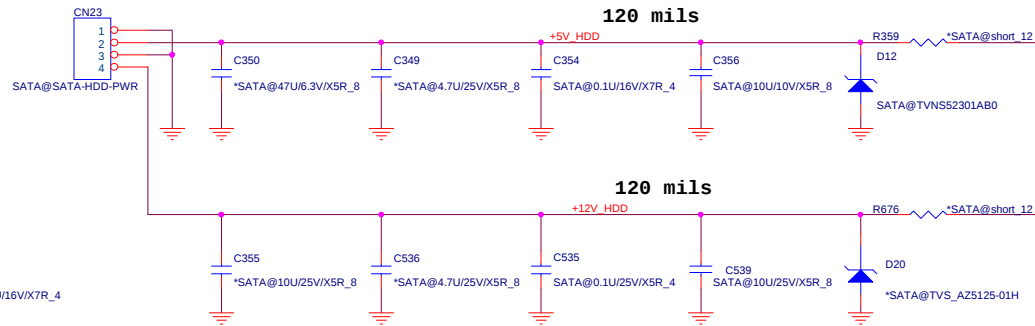


## ODD

### HDD SATA signal for 3.5".



### HDD SATA power for 3.5".



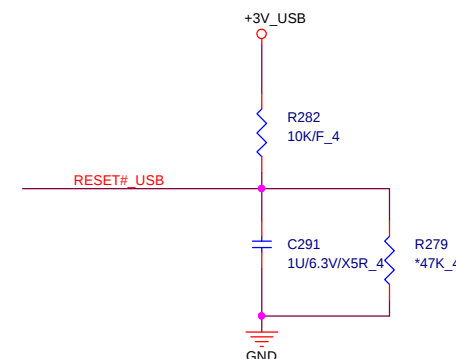
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Size Custom Document Number WLAN(NGFF)/HDD/ODD Rev 2A

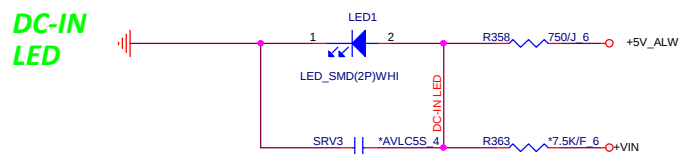
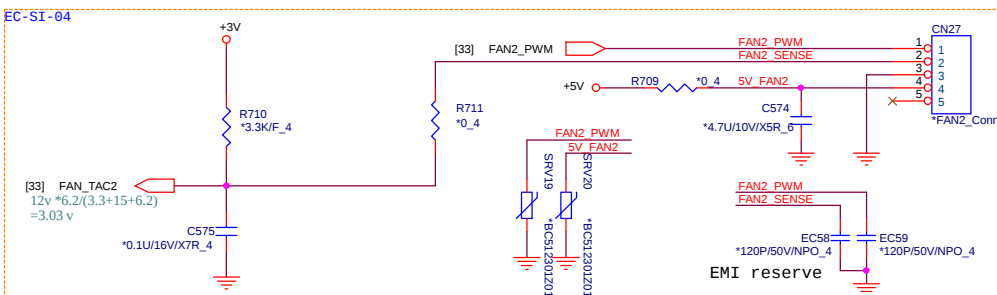
Date: Monday, January 18, 2016 Sheet 30 of 54



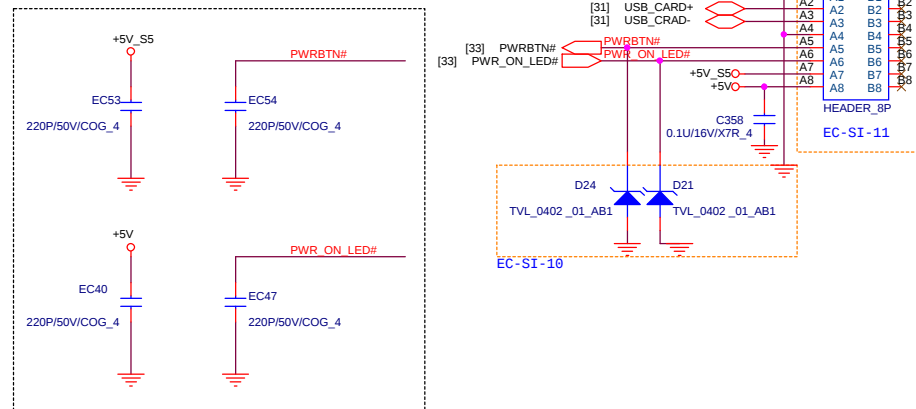
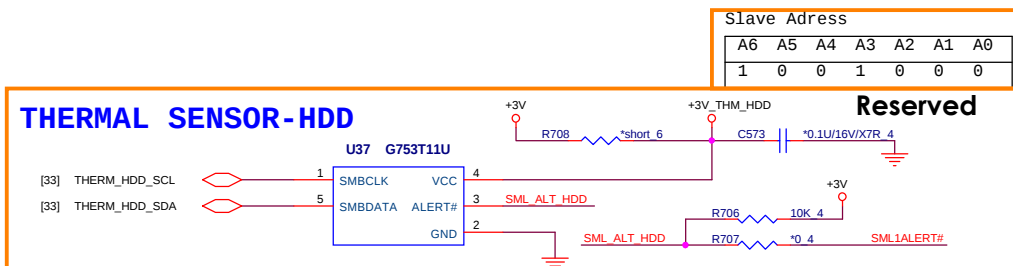




[5,15,16,17,18,19,20,22,23,24,25,27,28,29,31,32,33,35,36,44,47,48] +3V  
[15,24,25,26,30,32,37,44,47] +5V  
[24,26,32,37,38,39,40,41,42,43,44,48] +5V S5



34

[illegible]

**PROJECT: HP-Molokai**

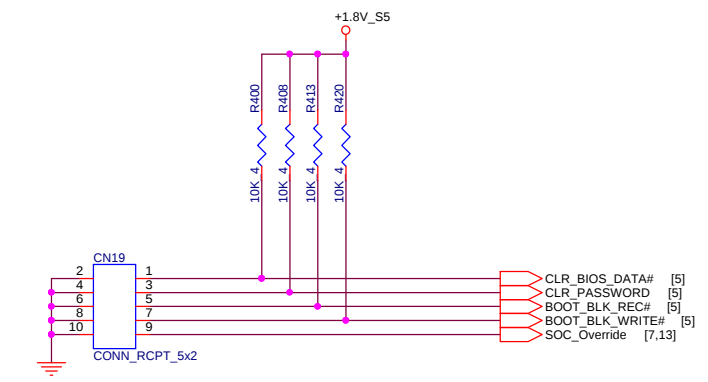
|                                |                                            |           |
|--------------------------------|--------------------------------------------|-----------|
| Size<br>Custom                 | Document Number<br><b>Thermal/FAN/LEDs</b> | Rev<br>2A |
| Date: Monday, January 18, 2016 | Sheet 34 of 54                             |           |

# CLR\_CMOS

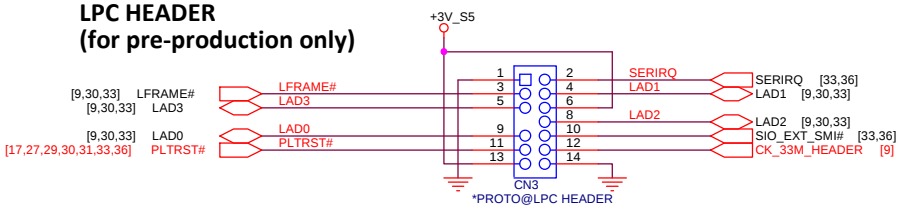
| Jumper            | Pre-production | Production |
|-------------------|----------------|------------|
| BOOT_BLK_Recovery | X              | X          |
| BOOT_BLK_Enable   | 0              | X          |

| Jumper | Type              |
|--------|-------------------|
| Pop    | CLR_BIOS_DAT      |
| Pop    | CLR_PASSWD        |
| Pop    | BOOT_BLK_Recovery |
| Pop    | BOOT_BLK_Enable   |

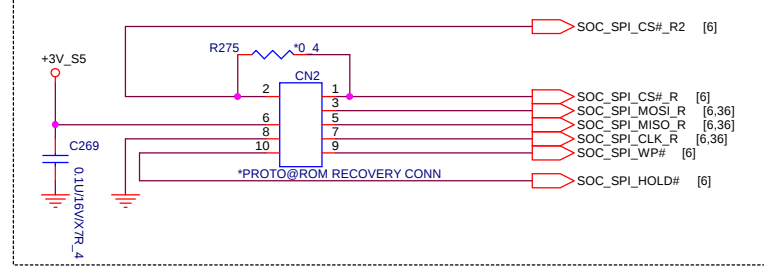
[3,4,5,6,11,14,22,24,27,30,31,32,33,36,37,38,40,41,42,43,44,48]  
[5,6,7,8,9,11,13,14,22,33,36,40,41]  
[5,15,16,17,18,19,20,22,23,24,25,27,28,29,31,32,33,34,36,44,47,48]



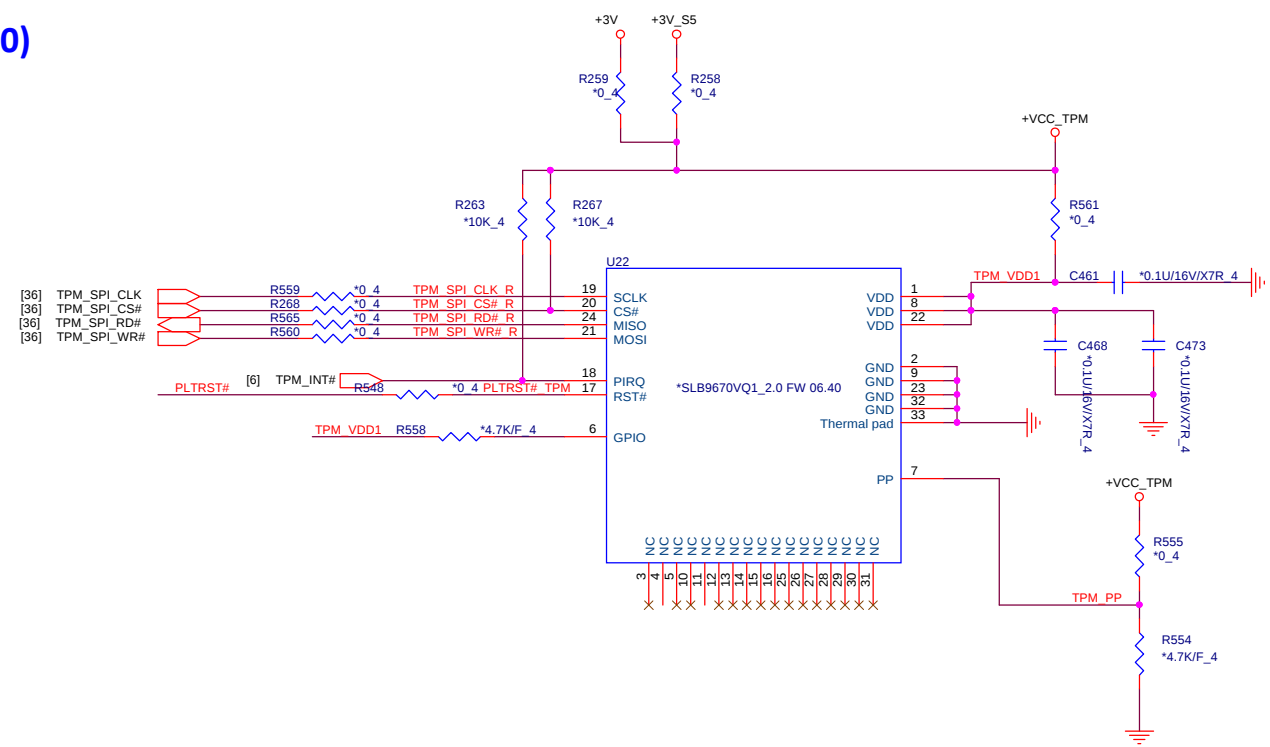
## LPC HEADER (for pre-production only)



## ROM recovery (for pre-production only)



## TPM (1.2 or 2.0)



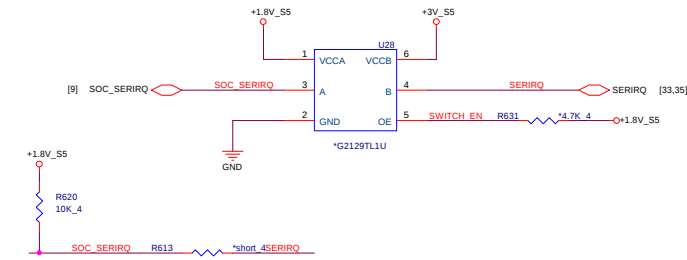
HP Restricted Secret



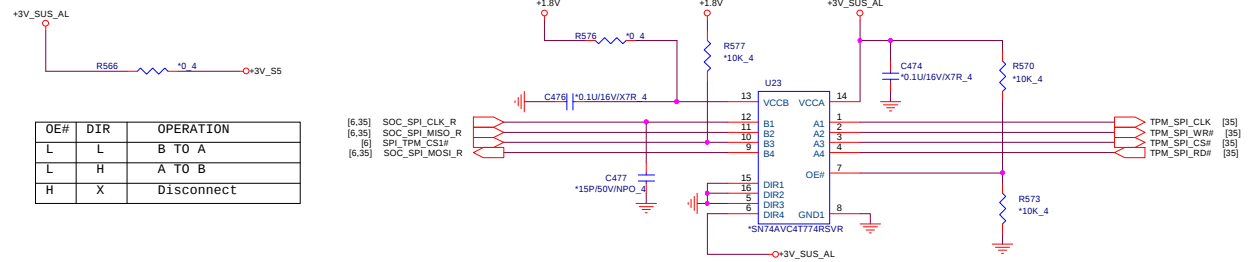
**Quanta Computer Inc.**  
PROJECT: HP-Molokai

|                                |                 |        |
|--------------------------------|-----------------|--------|
| Size Custom                    | Document Number | Rev 1A |
| JUMPER/LPCHeader               |                 |        |
| Date: Monday, January 18, 2016 | Sheet 35 of 54  |        |

## SERIRQ

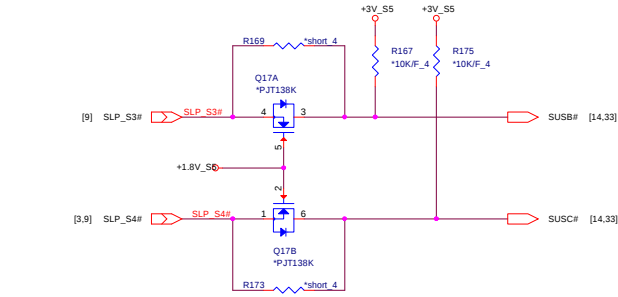


## TPM level shift

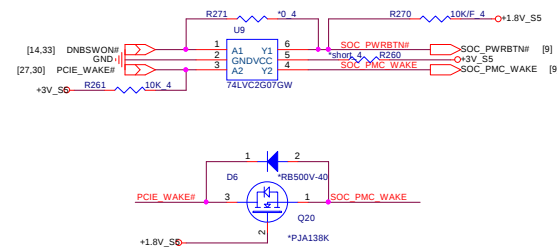


| OE# | DIR | OPERATION  |
|-----|-----|------------|
| L   | L   | B TO A     |
| L   | H   | A TO B     |
| H   | X   | Disconnect |

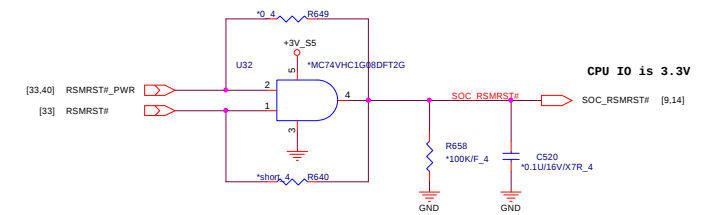
## SUSB/C#



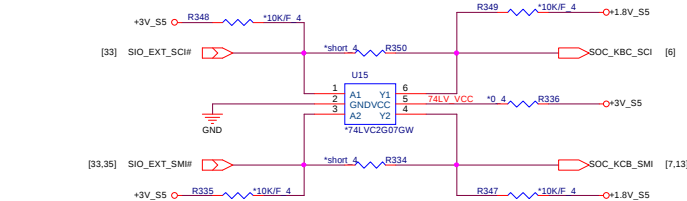
## PWRBTN#/PCIE\_WAKE#



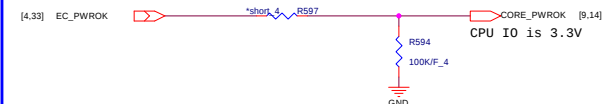
## RSMRST#



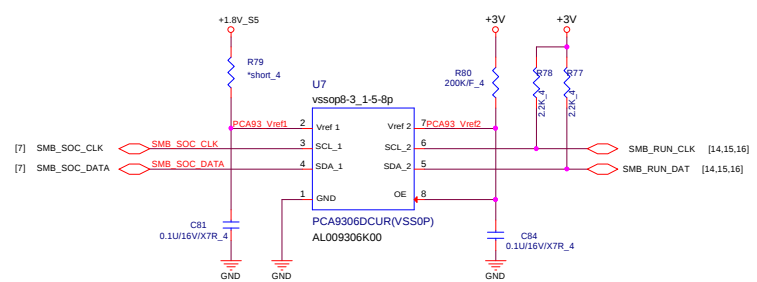
## SCI#/SMI#



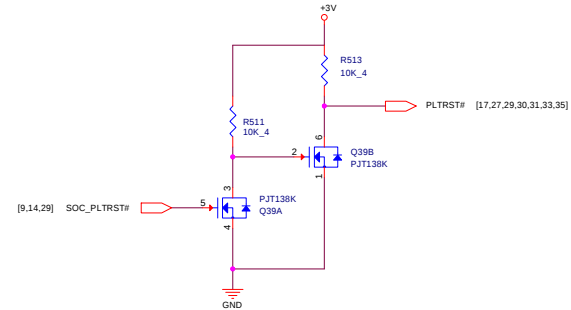
## SYS PWRGD



## SO-DIMM/XDP SMBUS



## PLTRST#



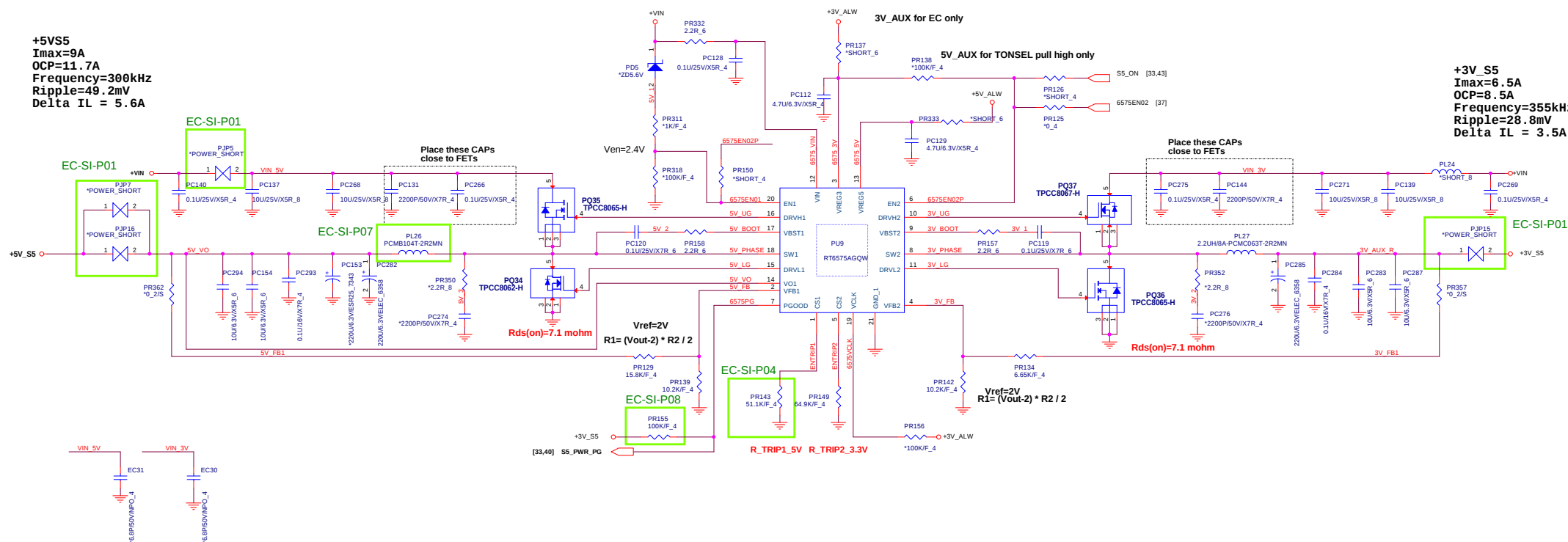
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Quanta Computer Inc.  
PROJECT: HP-Molokai

Size Custom Document Number Level shift Date: Monday, January 18, 2016 Sheet 36 of 54 Rev 1A

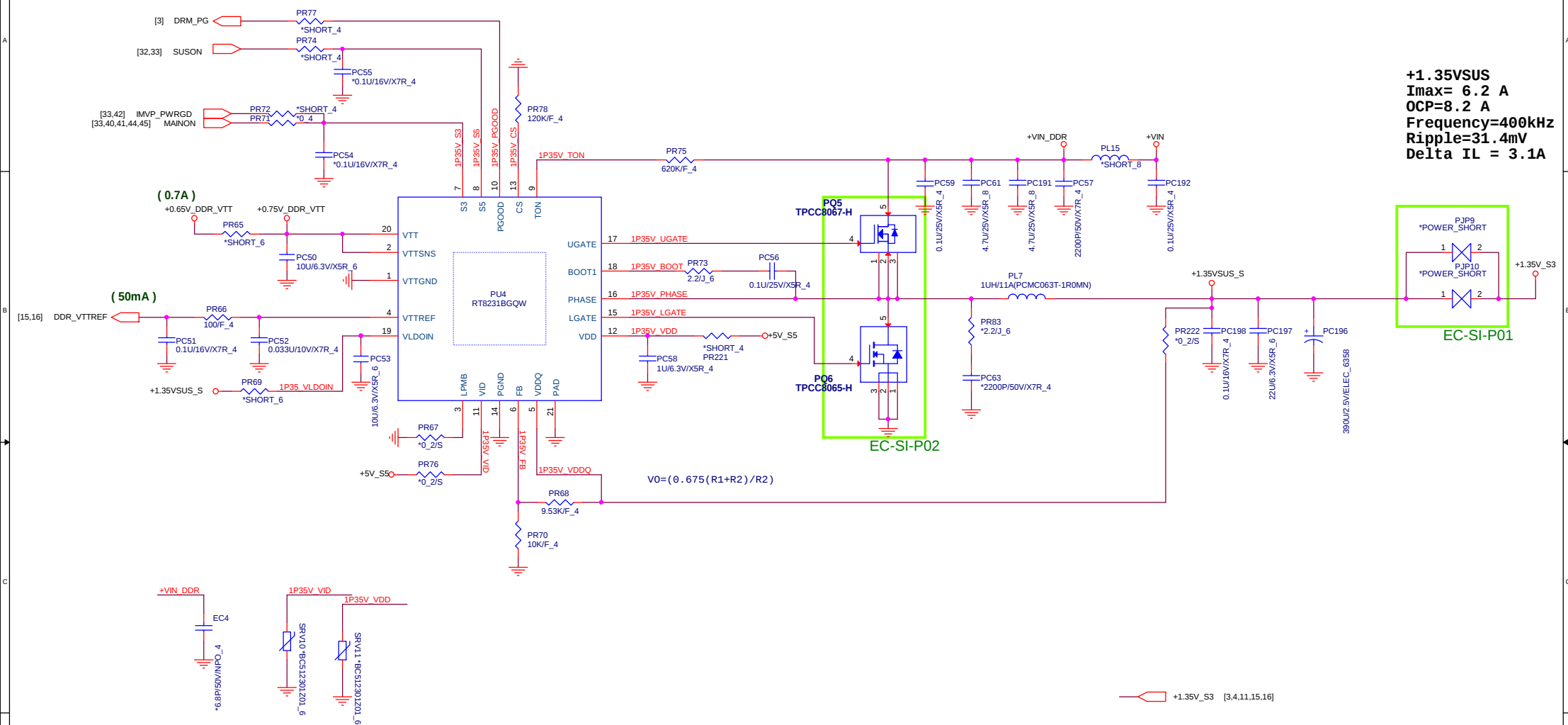


+3V\_S5  
Imax=6.5A  
OCP=8.5A  
Frequency=355kHz  
Ripple=28.8mV  
Delta IL = 3.5A



| MOSFET     | Package | ID (Ta=25C) | Rds_on_max |
|------------|---------|-------------|------------|
| TPCC8067-H | DFN3x3  | 9A          | 26m        |
| TPCC8062-H | DFN3x3  | 27A         | 7.1m       |

| EN0    | ENC    | REF | VREG3 | VREG5 | SMPS1 | SMPS2 |
|--------|--------|-----|-------|-------|-------|-------|
| LOW    | LOW    | OFF | OFF   | OFF   | OFF   | OFF   |
| > 2.4V | LOW    | ON  | ON    | ON    | OFF   | OFF   |
| > 2.4V | > 2.4V | ON  | ON    | ON    | ON    | ON    |

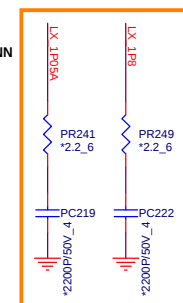


HP Restricted Secret

|                                                                                                                                                 |  |                                   |                                           |           |
|-------------------------------------------------------------------------------------------------------------------------------------------------|--|-----------------------------------|-------------------------------------------|-----------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT: HP-Molokai</b> |  | Size<br>Custom                    | Document Number<br><b>DDR3L (RT8231B)</b> | Rev<br>2A |
|                                                                                                                                                 |  | Date:<br>Monday, January 18, 2016 | Sheet<br>39                               | of<br>54  |

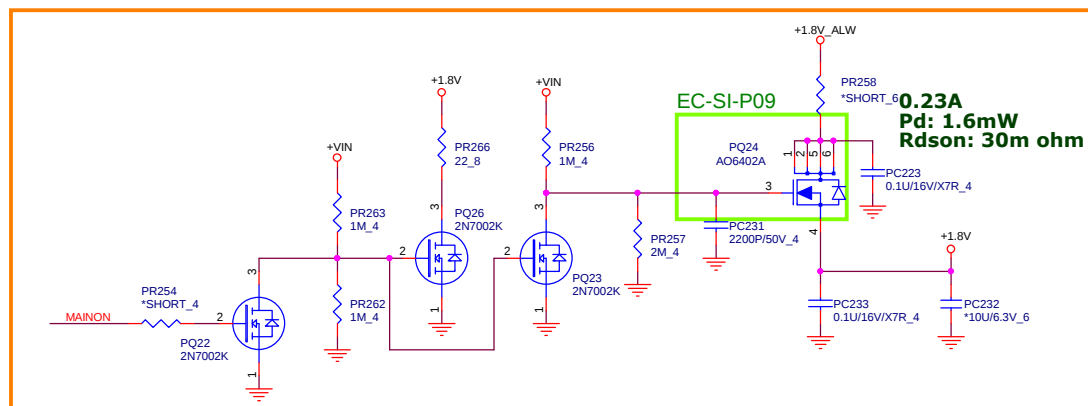
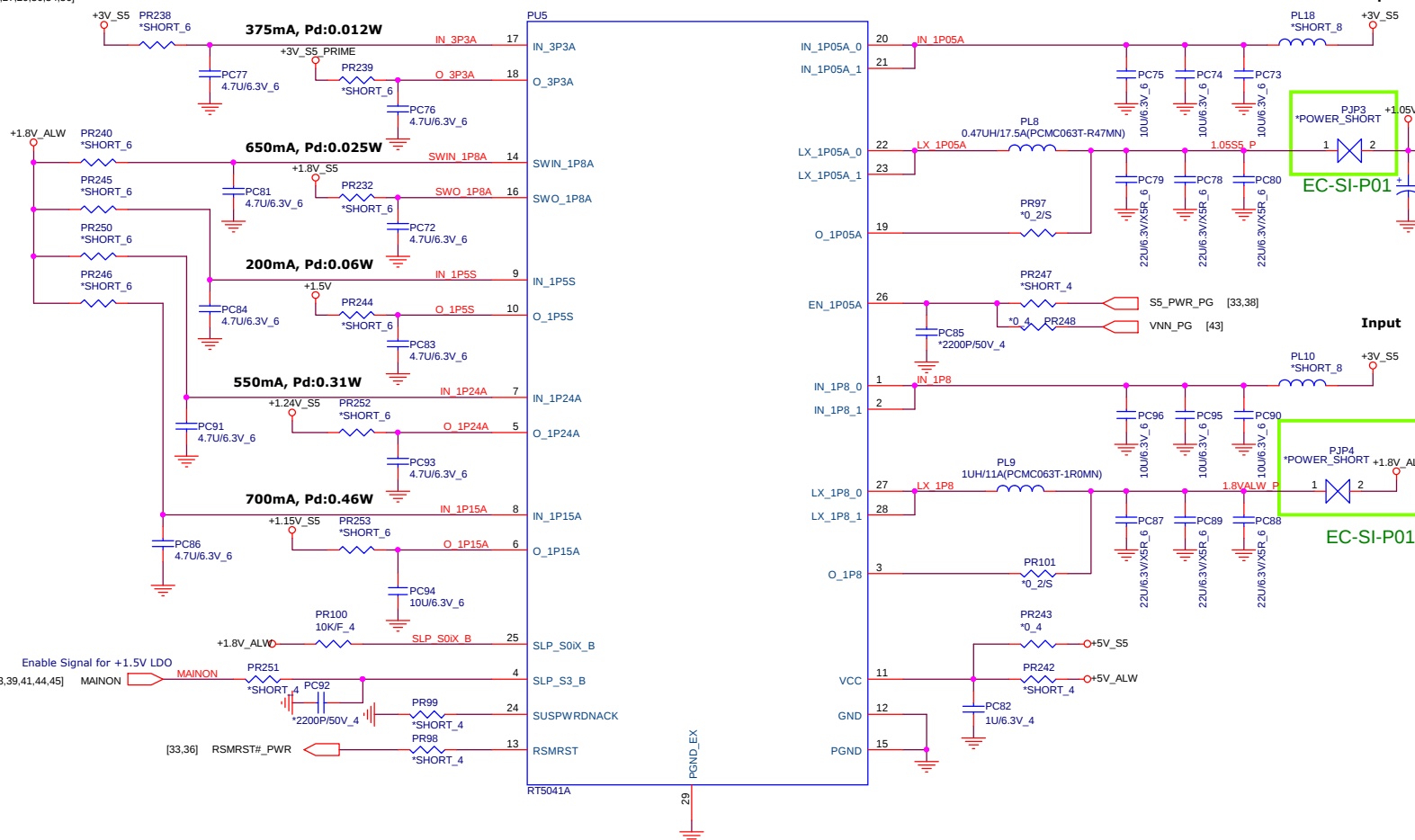
+3V\_S5 [3,4,5,6,11,14,22,24,27,30,31,32,33,35,36,37,38,41,42,43,44,48]  
 +1.8V\_S5 [5,6,7,8,9,11,13,14,22,33,35,36,41]  
 +3V\_S5\_PRIME [11,33]  
 +1.5V [11,26]  
 +1.24V\_S5 [11]  
 +1.15V\_S5 [10]  
 +5V\_ALW [28,34,38]  
 +1.05V\_S5 [9,10,41,42]  
 +1.8V [5,6,25,27,29,30,34,36]

**+1.05VS5**  
**I<sub>max</sub>= 2 A**  
**OCP=6 A**  
**Frequency=1.2MHz**  
**Ripple=5mV**  
**Delta IL = 1.3A**



Snubber

**+1.8VALW**  
**I<sub>max</sub>= 3.1 A**  
**OCP=6 A**  
**Frequency=1.2MHz**  
**Ripple=6.8mV**  
**Delta IL = 0.68 A**

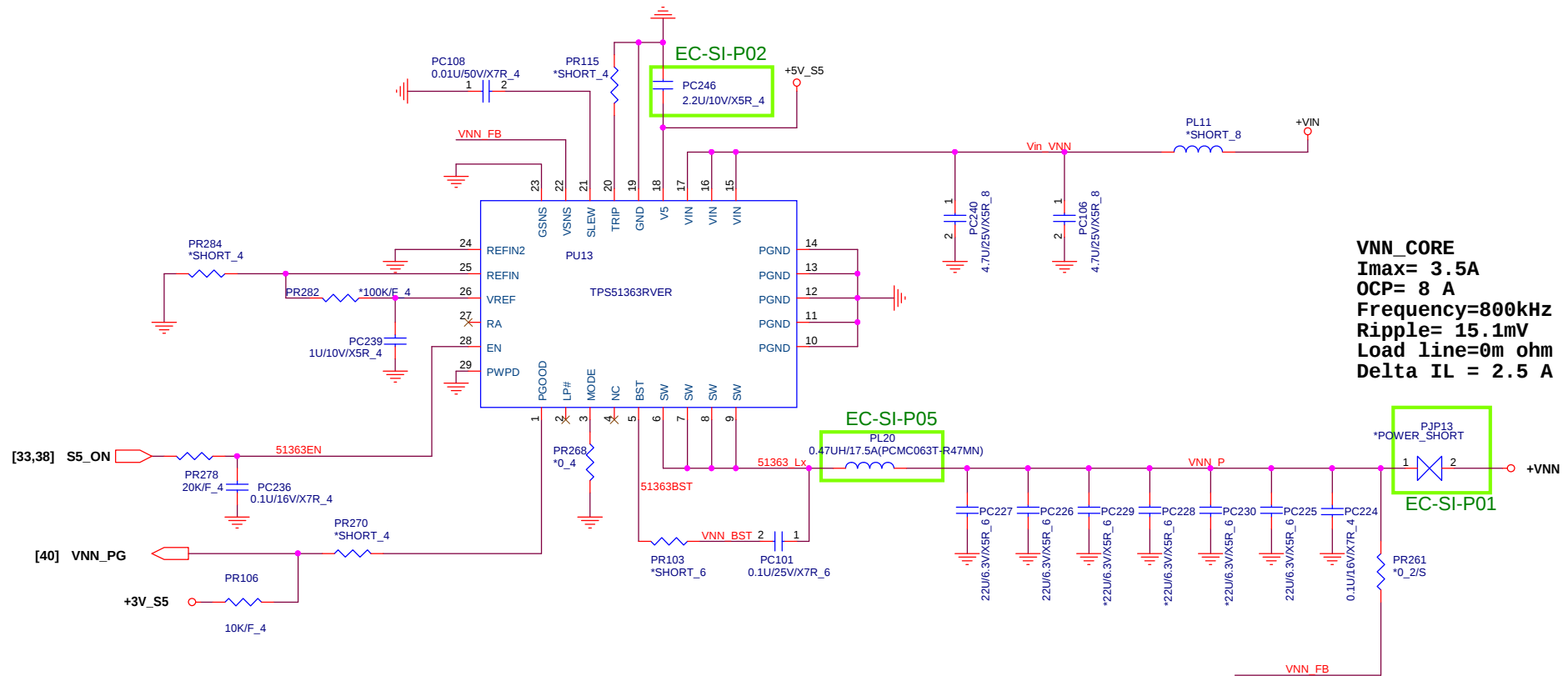


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|                                                                                                                                                 |                          |        |                 |       |
|-------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|--------|-----------------|-------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT: HP-Molokai</b> |                          | Size   | Document Number | Rev   |
|                                                                                                                                                 |                          | Custom | MOIC (RT5041A)  |       |
| Date:                                                                                                                                           | Monday, January 18, 2016 | Sheet  | 40              | of 54 |







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Quanta Computer Inc.

PROJECT: HP-MoIokai

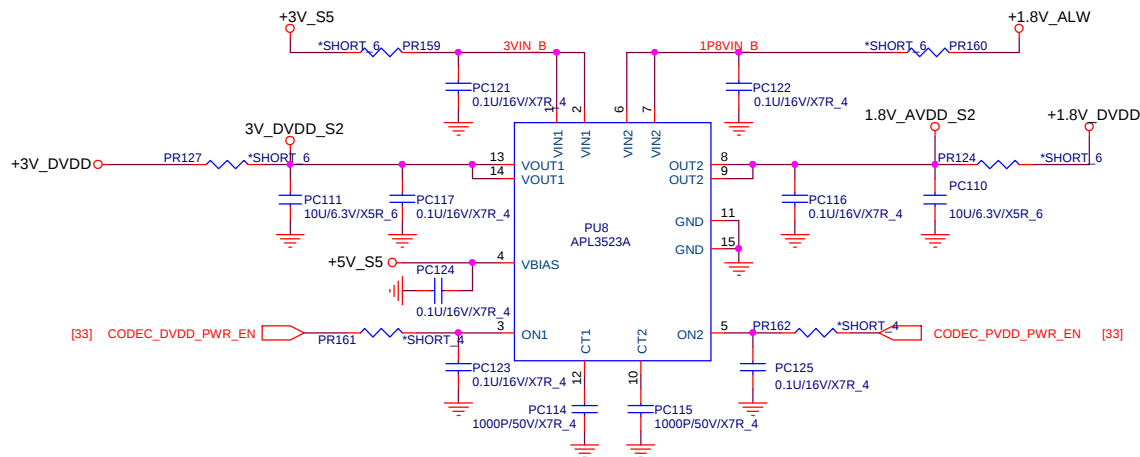
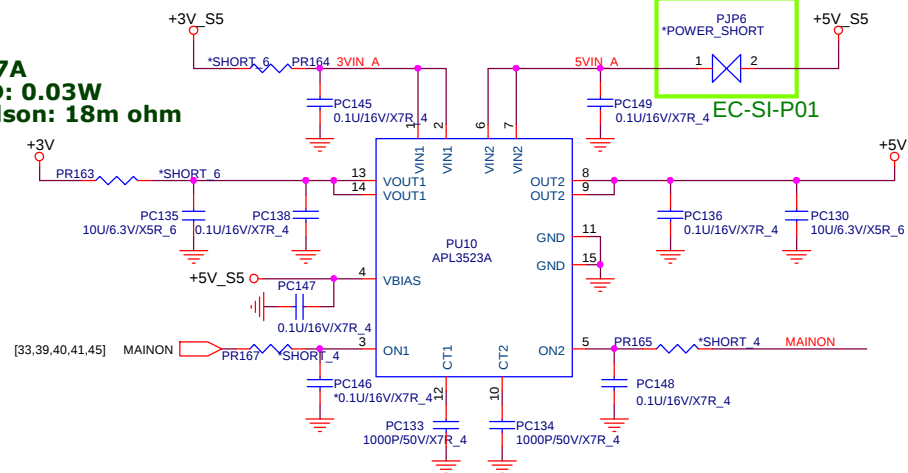
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|------|--------------------------|--------------------|-------|----|
| Size | Document Number          | VNN CORE(TPS51363) | Rev   | 2A |
| Date | Monday, January 18, 2016 | Sheet              | 43 of | 54 |

**1.7A**  
**Pd: 0.03W**  
**Rdson: 18m ohm**

**5.62A**  
**Pd: 0.57W**  
**Rdson: 18m ohm**

**0.5A**  
**Pd: 0.01W**  
**Rdson: 18m ohm**

**0.03A**  
**Pd: 0.01W**  
**Rdson: 18m ohm**



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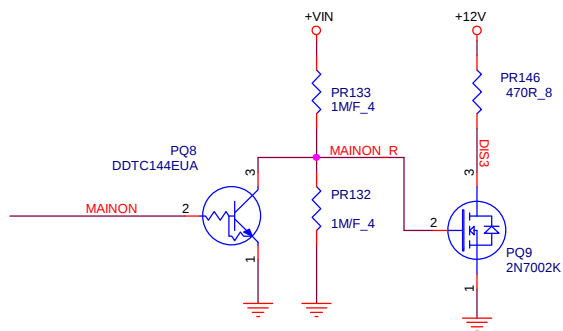
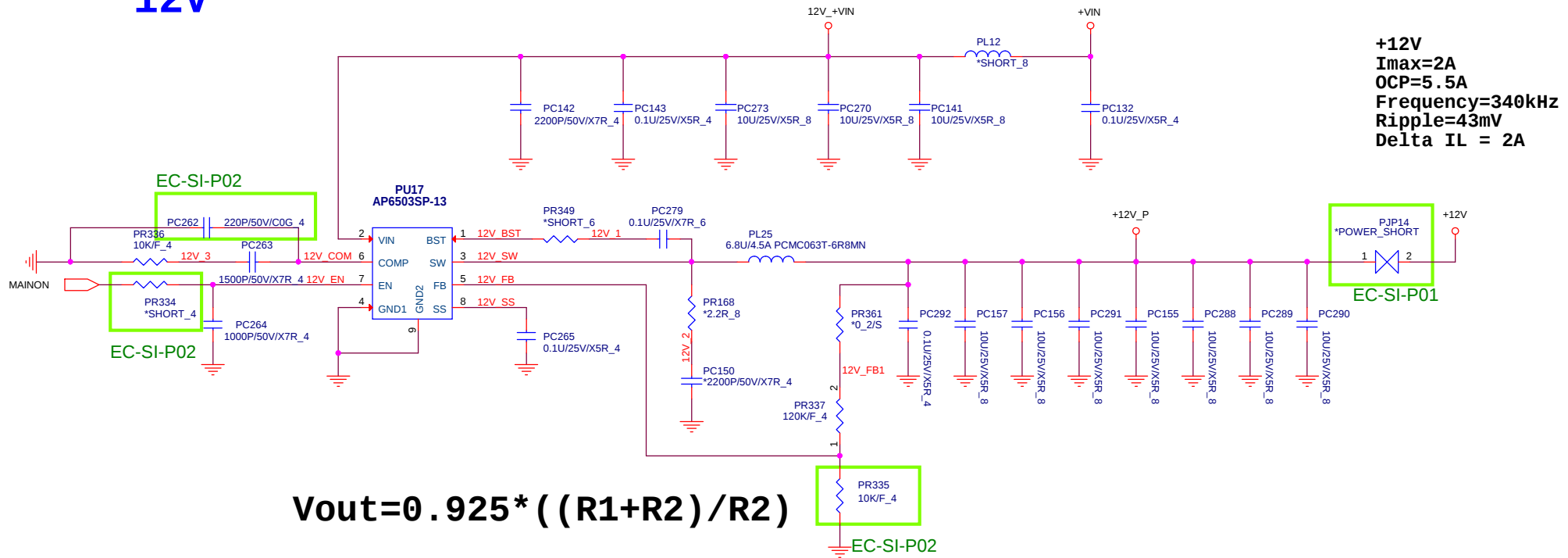


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**PROJECT: HP-Molokai**

|                                |                           |           |
|--------------------------------|---------------------------|-----------|
| Size<br>Custom                 | Document Number           | Rev<br>2A |
| Date: Monday, January 18, 2016 | Load switch IC (APL3523A) |           |
| Sheet 44 of 54                 |                           |           |

12V



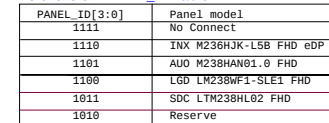
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Quanta Computer Inc.

PROJECT: HP-MoIokai

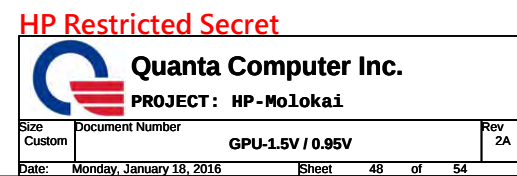
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|-----------|--------------------------|-------|-----------|
| Size<br>B | Document Number          | +12V  | Rev<br>2A |
| Date:     | Monday, January 18, 2016 | Sheet | 45 of 54  |

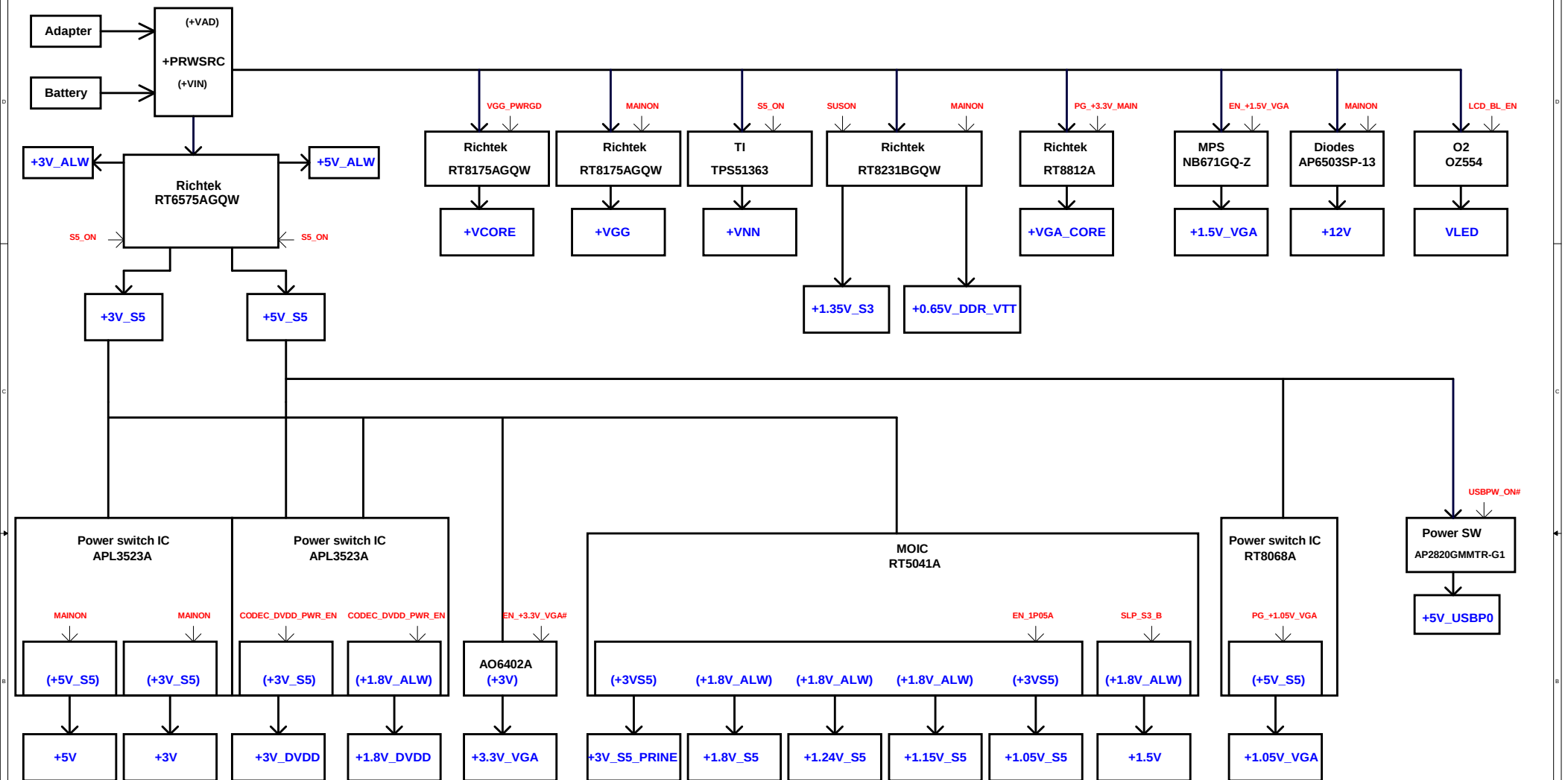


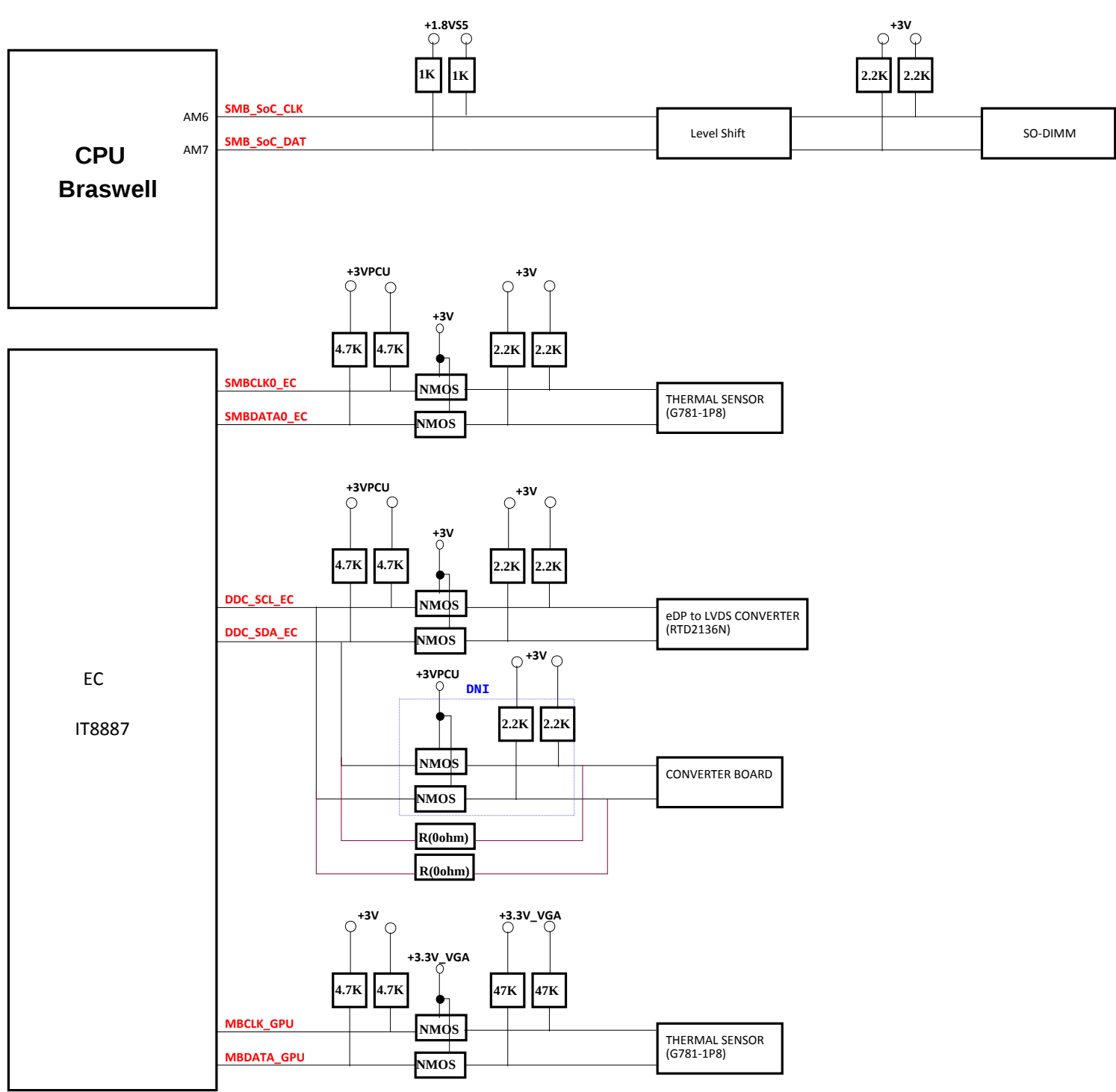
|                                |                                 |           |
|--------------------------------|---------------------------------|-----------|
| Size<br>Custom                 | Document Number<br><b>OZ554</b> | Rev<br>2A |
| Date: Monday, January 18, 2016 | Sheet 46 of 54                  |           |

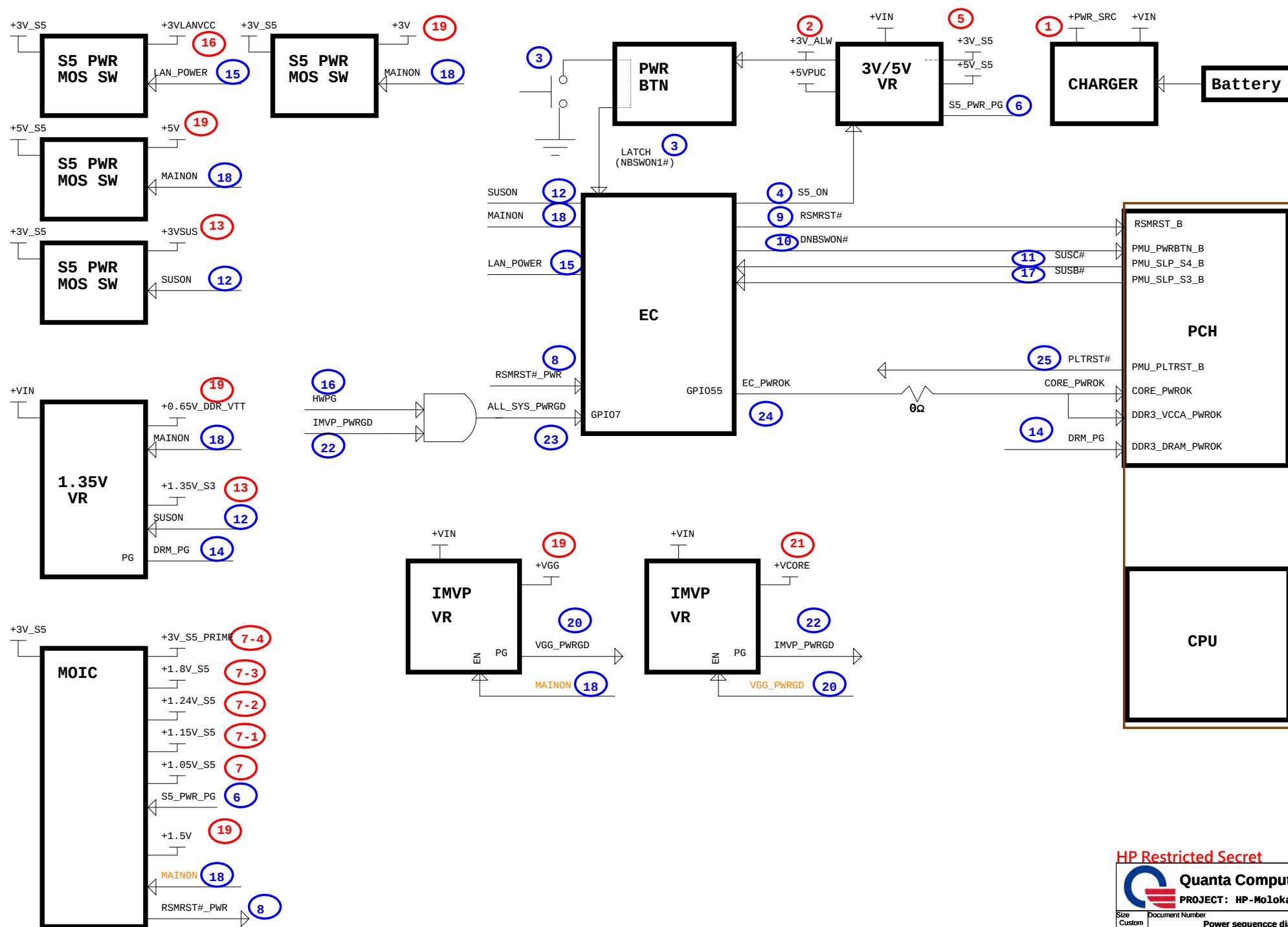


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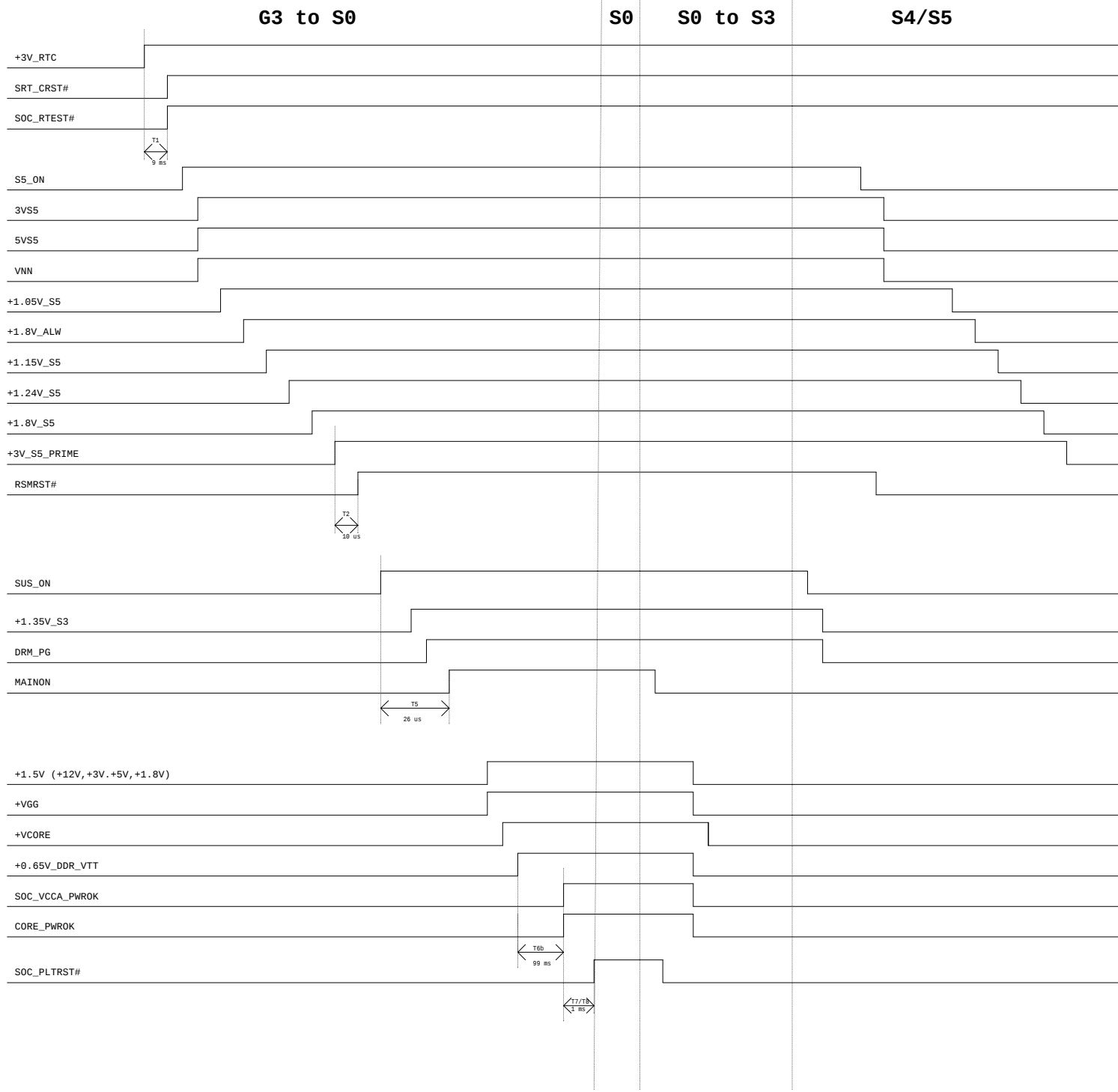


Quanta Computer Inc.

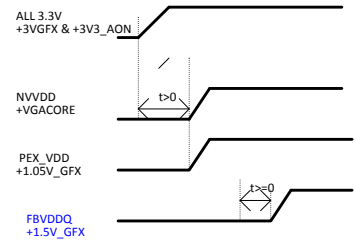
PROJECT: HP-Mo1okai

| Size   | Document Number        | Rev |
|--------|------------------------|-----|
| Custom | Power sequence diagram | 1A  |

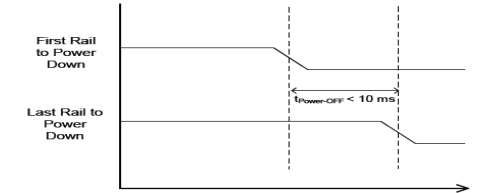
Date: Monday, January 18, 2016 Sheet 51 of 54



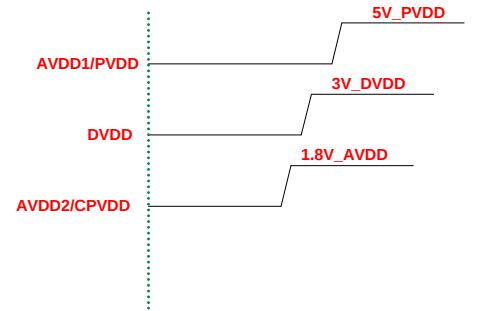
N16V Power up sequence



N16V Power down sequence



AUDIO POWER SEQUENCE



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***N91A EE Schematic EC Tracking Record DB to SI version***

| EC #     | Page  | Description                                                | Part Affected                           |
|----------|-------|------------------------------------------------------------|-----------------------------------------|
| EC-SI-01 | 32    | add GND PAD for EMI                                        | H20,H21                                 |
| EC-SI-02 | 26    | change Audio speaker connector from 1 4pin to 2 2pin       | CN25,CN26                               |
| EC-SI-03 | 07    | change board ID for SI stage, R537 no stuff, R544 stuff    | R537,R544                               |
| EC-SI-04 | 34    | add second fan function                                    | CN27,R709,C574,EC58,EC59,R710,R711,C575 |
| EC-SI-05 | 33    | add ADPID3 for smart adapter                               | U26.pin4,PQ38,PR295                     |
| EC-SI-06 | 15    | add EC60 for EMI                                           | EC60                                    |
| EC-SI-07 | 20    | remove R483 double pull high for PSI                       | R483                                    |
| EC-SI-08 | 33    | add EMMC_DETECTfunction for EC check sku                   | R714,R715                               |
| EC-SI-09 | 30    | change CN17 footprint                                      | CN17                                    |
| EC-SI-10 | 24,34 | change D4,SU1,D21,D24,D26 to stuff for ESD                 | D4,SU1,D21,D24,D26                      |
| EC-SI-11 | 30    | Change ODD connector to 18 pin                             | CN21                                    |
| EC-SI-12 | 34    | Change connector to FFC type of card reader daughter board | CN24                                    |
| EC-SI-12 | 26    | change AL6/AL7/AL9/AL10 to 0 ohm for Realtek suggestion    | AL6,AL7,AL9,AL10                        |

***N91A Power Schematic EC Tracking Record DB to SI version***

| EC #      | Page           | Description                             | Part Affected                                                              |
|-----------|----------------|-----------------------------------------|----------------------------------------------------------------------------|
| EC-SI-P01 | 38~48          | Change default open to default short    | PJP1~PJP11, PJP13~16                                                       |
| EC-SI-P02 | 39,43,45,46,48 | Downsize components                     | PC246, PR334, PR335, PC262, PC14, PC174, PQ5, PQ6<br>PC21, PC181,PC6       |
| EC-SI-P03 | 47, 48         | Correct connection                      |                                                                            |
| EC-SI-P04 | 38,47          | Fine tune OCP function                  | PR143,PR86                                                                 |
| EC-SI-P05 | 43,47          | Change choke for transient              | PL17, PL20                                                                 |
| EC-SI-P06 | 48             | Fine tune offset voltage                | PR21                                                                       |
| EC-SI-P07 | 38, 47         | Change components for ripple voltage    | PL26, PC65                                                                 |
| EC-SI-P08 | 42             | Change components CPU 6.5W              | PQ4, PR16, PR46, PR198, PR199                                              |
| EC-SI-P09 | 40,47,48       | Change components for common part using | PQ24, PR227, PR231, PQ12, PQ14, PQ16                                       |
| EC-SI-P10 | 47             | Fine tune soft start                    | PR90, PC208                                                                |
| EC-SI-P11 | 43             | Reducing VGG Ring Voltage               | PR290, PR267, PC234                                                        |
| EC-SI-P12 | 37             | Add components for SMART ID function    | PR281, PR300, PR295, PR291, PR310, PR271, PR285, PR407<br>PQ29, PQ31, PQ38 |