

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.  
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.  
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# K94 CHOPIN MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
A	0001052699	PRODUCTION RELEASED		2011-01-10

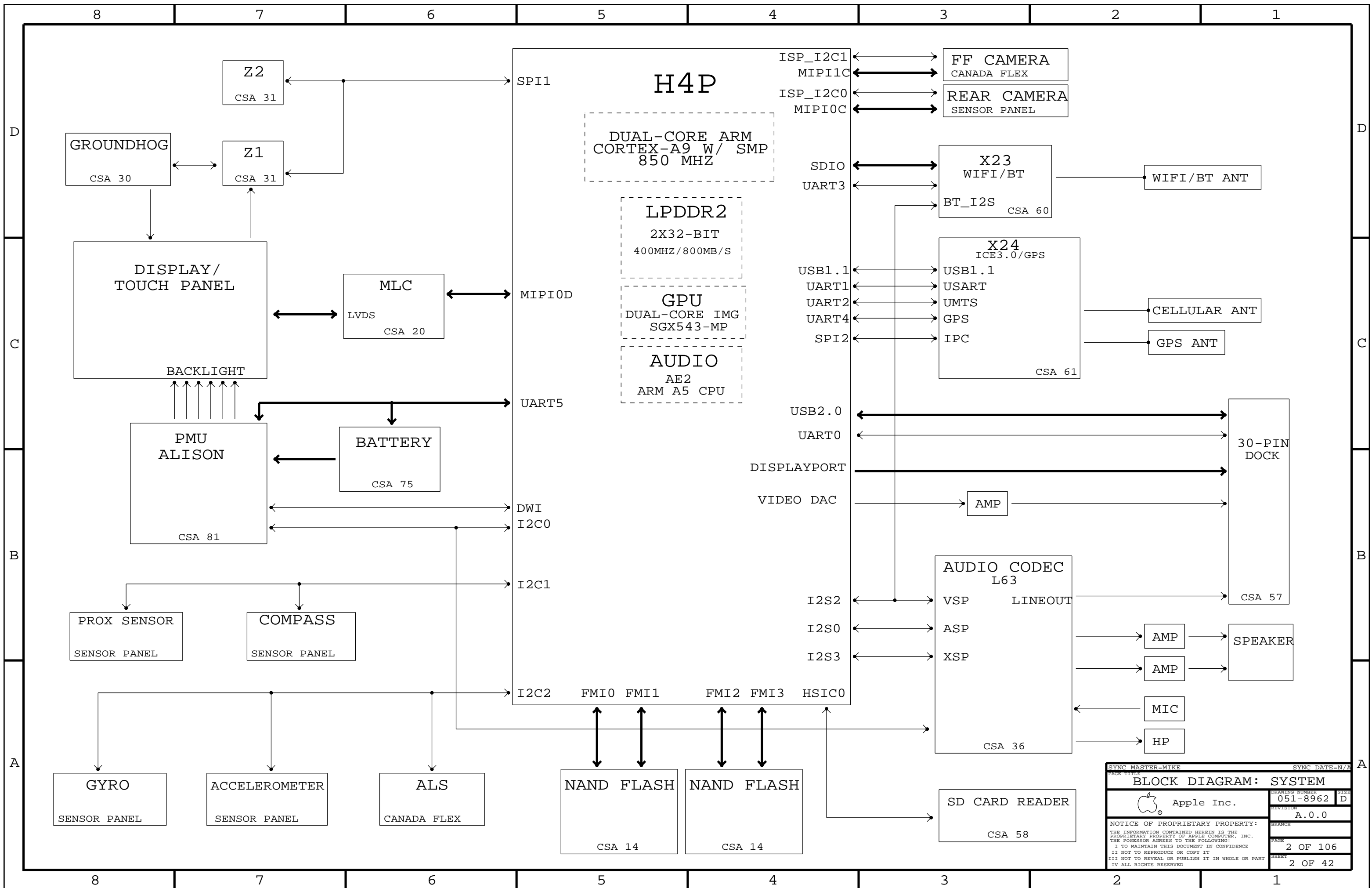
PVT  
REV. A

LAST\_MODIFIED=Mon Jan 10 13:11:06 2011

PDF	CSA	CONTENTS	SYNC	MASTER	DATE	PDF	CSA	CONTENTS	SYNC	MASTER	DATE
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2	2	BLOCK DIAGRAM: SYSTEM		MIKE	N/A	33	75	POWER: BATTERY CONNECTOR		YOSH	N/A
3	5	BOM TABLE		MIKE	N/A	34	81	POWER: PMU		YOSH	N/A
4	6	AP: MAIN		JAMES	N/A	35	82	POWER: PMU		YOSH	N/A
5	7	AP: I/Os		JAMES	N/A	36	83	POWER: 3.3V VR		YOSH	N/A
6	8	AP: NAND		JAMES	N/A	37	90	DEBUG AND MISC		MIKE	N/A
7	9	AP: TV,DP,MIPI		JAMES	N/A	38	93	FCT/ICT TEST/BRACKETS		MIKE	N/A
8	10	AP: PWR		JAMES	N/A	39	100	CONSTRAINTS: ASSIGNMENTS		MIKE	N/A
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13	17	VIDEO: DISPLAY PORT		JAMES	N/A						
14	20	VIDEO: MLC		MIKE	N/A						
15	21	VIDEO: MLC ALIASES		MIKE	N/A						
16	22	VIDEO: LVDS CONNECTOR		ALEX	N/A						
17	30	GRAPE: GROUNDHOG,CONN,BOOST		RAMSIN	N/A						
18	31	GRAPE: Z1, Z2		RAMSIN	N/A						
19	36	AUDIO: L63 CODEC		LENG	N/A						
20	37	AUDIO: SPEAKER AMP		LENG	N/A						
21	38	AUDIO: HEADPHONE OUT		LENG	N/A						
22	39	AUDIO: BLANK		LENG	N/A						
23	42	AUDIO: DETECT/MIC BIAS		LENG	N/A						
24	43	AUDIO: HP/MIC FILTERS		LENG	N/A						
25	54	CONNECTOR: CANADA FLEX CONN,SENSOR PANEL ALIASES		MARK B.	N/A						
26	55	CONNECTOR: CANADA FLEX FILTERS		MARK B.	N/A						
27	56	CONNECTOR: SENSOR PANEL CONNECTOR		MARK B.	N/A						
28	57	IO FLEX: DOCK COMPONENTS		JAMES	N/A						
29	59	IO FELX: B2B Connector		JAMES	N/A						
30	60	CONNECTOR: X23 WIFI/BT		MIKE	N/A						
31	61	CONNECTOR: X24 CELLULAR/GPS		MIKE	N/A						

DRAWING TITLE		CHOPIN MLB	
DRAWING NUMBER		051-8962	SIZE D
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DRAWING  
TITLE=BACH  
ABBREV=DRAWING



SYNC MASTER=MIKE		SYNC DATE=N/A	
BLOCK DIAGRAM: SYSTEM			
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Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:

ALL AVAIL BOM OPTIONS

COMMON  
ALTERNATE  
16GB\_PROD  
32GB\_PROD  
64GB\_PROD  
BKLT\_PLL  
DEVELOPMENT\_JTAG  
DEVELOPMENT\_JTAG\_TAP  
JTAG\_DAP  
JTAG\_TAP\_NOT  
SPEAKER  
INTERNAL\_MIC  
PORTRAIT\_DOCK  
MLC\_DEV  
MLC\_PROD  
K93  
K94

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE

ADD DEVELOPMENT AND OTHER BOMS ONCE YOU GET BOM NUMBERS

# BOM OPTIONS

## PROGRAMMABLE PARTS

### SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-8962	1	SCH, CHOPIN_AUDIO, MLB, K94	SCH1	
820-3069	1	PCBF, CHOPIN_AUDIO, MLB, K94	PCB1	

### PD PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
806-1396	1	FENCE, GRAPE, MLB, K93/K94	FENCE1	
806-1397	1	CAN, GRAPE, MLB, K93/K94	CAN1	NOSTUFF
806-1398	1	FENCE, CPU, MLB, K93/K94	FENCE2	
806-1399	1	CAN, CPU, MLB, K93/K94	CAN2	NOSTUFF
806-1400	1	FENCE, MAND, MLB, K93/K94	FENCE3	
806-1401	1	CAN, MAND, MLB, K93/K94	CAN3	NOSTUFF

### TOP BARCODE LABEL/EEE CODES (ONLY ONE IS USED PER BOM)


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7651	1	EEEE FOR 639-1180 (K93 16G)	DH36	CRITICAL	EEEE_K93_16G
825-7651	1	EEEE FOR 639-1426 (K93 32G)	DH37	CRITICAL	EEEE_K93_32G
825-7651	1	EEEE FOR 639-1428 (K93 64G)	DG99	CRITICAL	EEEE_K93_64G
825-7651	1	EEEE FOR 639-1112 (K94 16G)	DFC4	CRITICAL	EEEE_K94_16G
825-7651	1	EEEE FOR 639-1181 (K94 32G)	DFC5	CRITICAL	EEEE_K94_32G
825-7651	1	EEEE FOR 639-1182 (K94 64G)	DFC6	CRITICAL	EEEE_K94_64G
825-7651	1	EEEE FOR 639-1430 (K95 16G)	DH3C	CRITICAL	EEEE_K95_16G
825-7651	1	EEEE FOR 639-1427 (K95 32G)	DH3D	CRITICAL	EEEE_K95_32G
825-7651	1	EEEE FOR 639-1429 (K95 64G)	DG9C	CRITICAL	EEEE_K95_64G

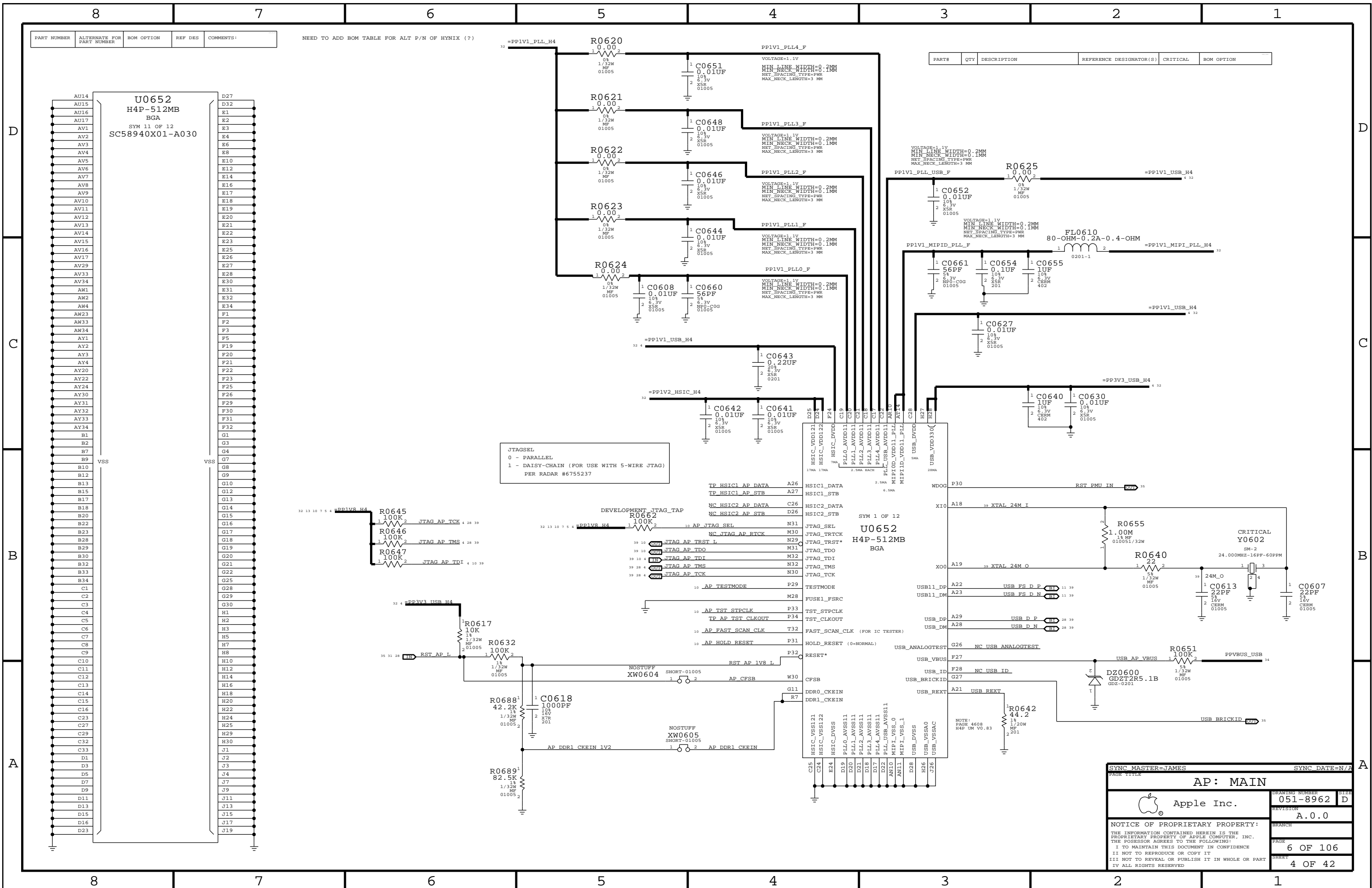
### BOTTOM LABEL TYPE 1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	631- B/C LABEL	LBL1	CRITICAL	
825-7639	1	639- B/C LABEL	LBL2	CRITICAL	

### BOTTOM LABEL TYPE 2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7640	1	MATRIX LABEL	LBL3	CRITICAL	
825-7640	1	631- MATRIX LABEL	LBL4	CRITICAL	

SYNC MASTER=MIKE		SYNC DATE=N/A	
<b>BOM TABLE</b>			
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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NEED TO ADD BOM TABLE FOR ALT P/N OF HYNIX (?)

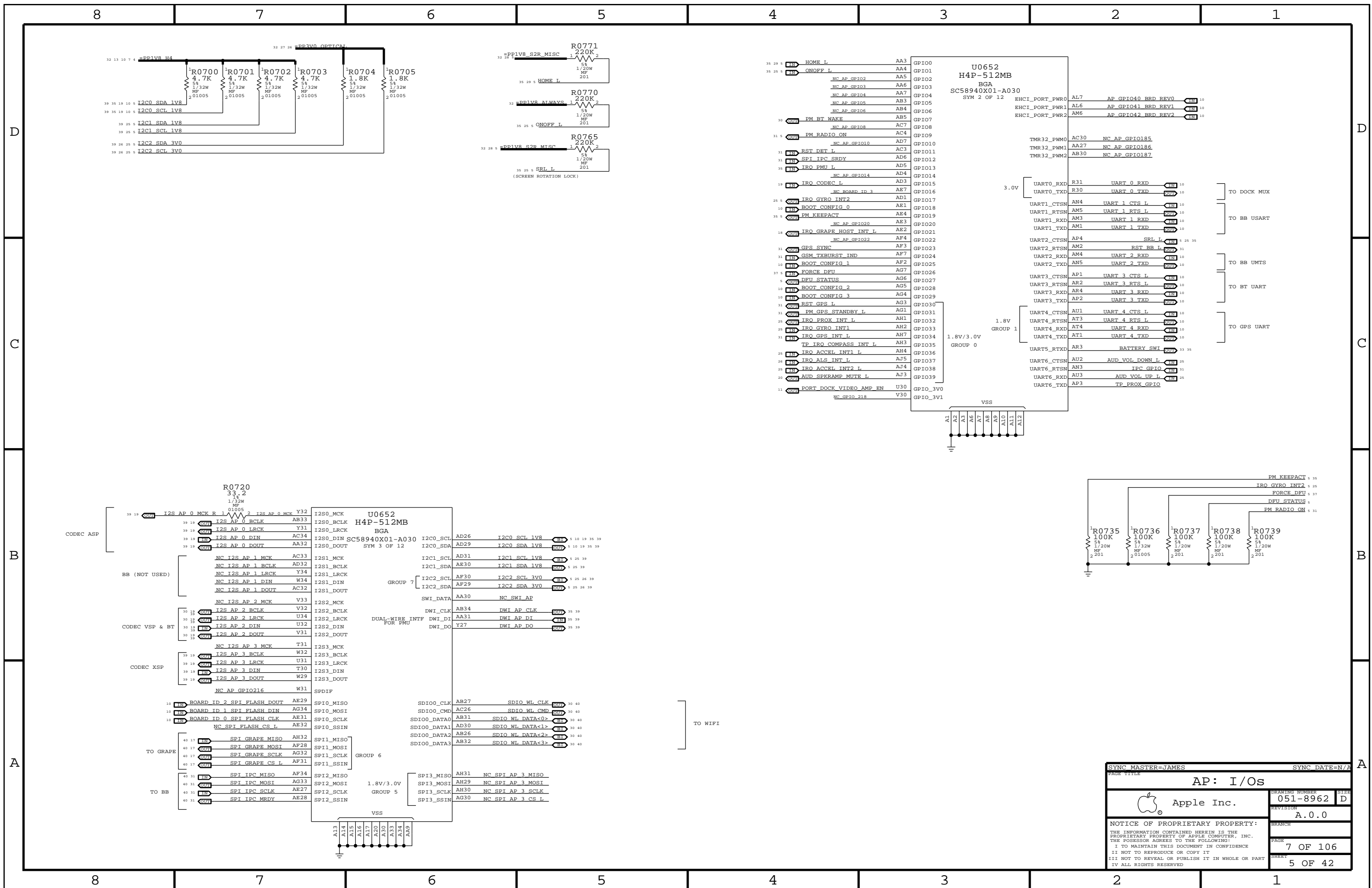
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H4P-512MB  
BGA  
SYM 11 OF 12  
SC58940X01-A030

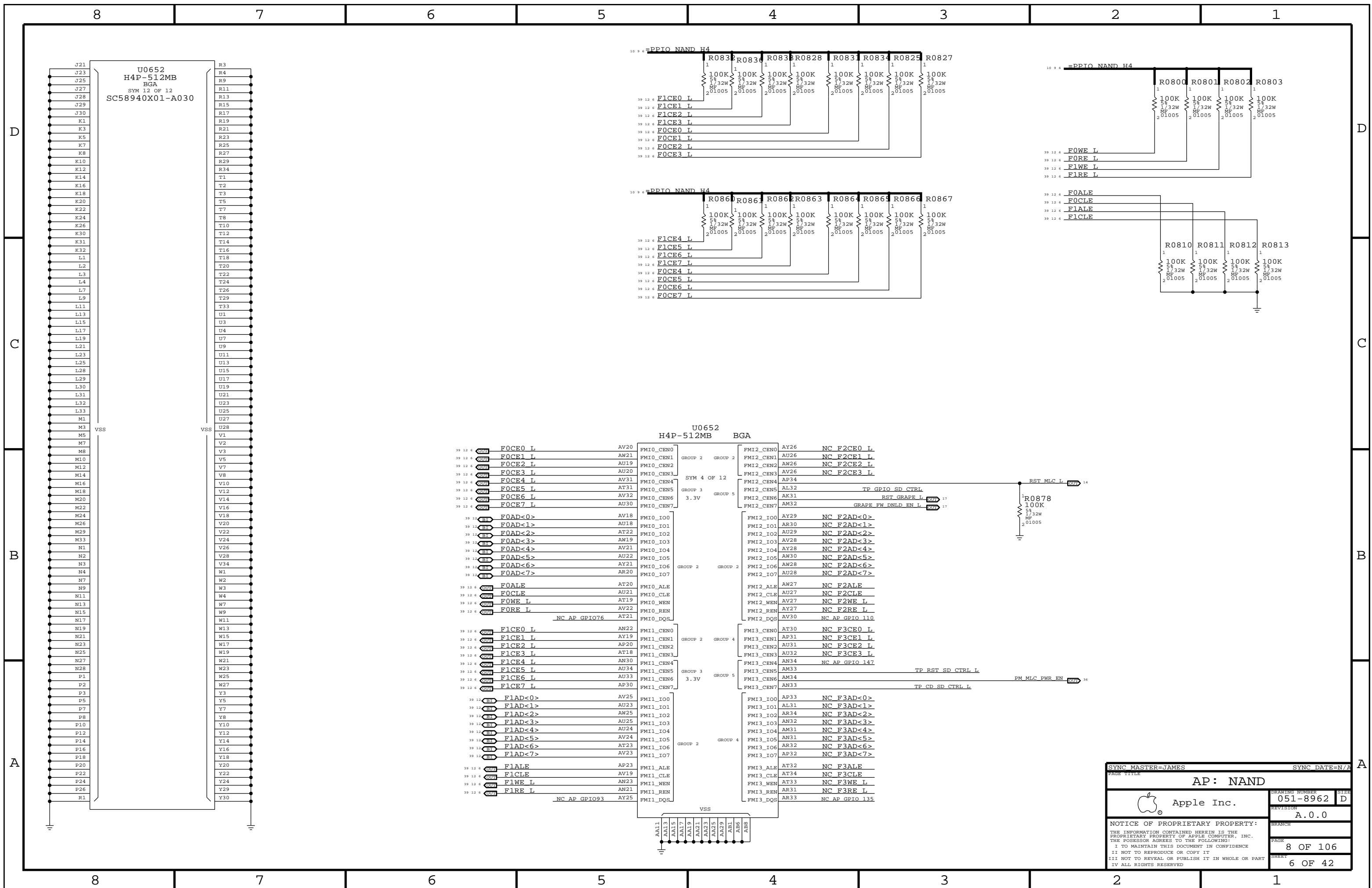
JTAGSEL  
0 - PARALLEL  
1 - DAISY-CHAIN (FOR USE WITH 5-WIRE JTAG)  
PER RADAR #6755237

SYM 11 OF 12  
U0652  
H4P-512MB  
BGA

PAGE TITLE		SYNC DATE=N/A	
<b>AP: MAIN</b>			
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4 OF 42			



SYNC MASTER=JAMES		SYNC DATE=N/A	
PAGE TITLE			
<b>AP: I/Os</b>			
		DRAWING NUMBER	051-8962
		REVISION	A.0.0
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		PAGE	7 OF 106
		SHEET	5 OF 42



8 7 6 5 4 3 2 1

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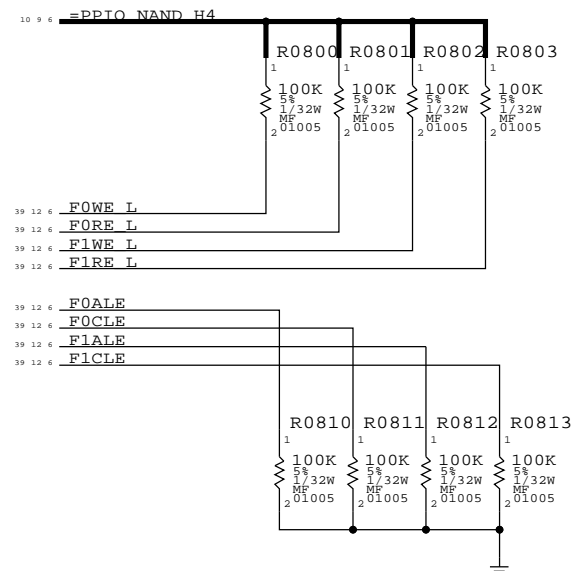
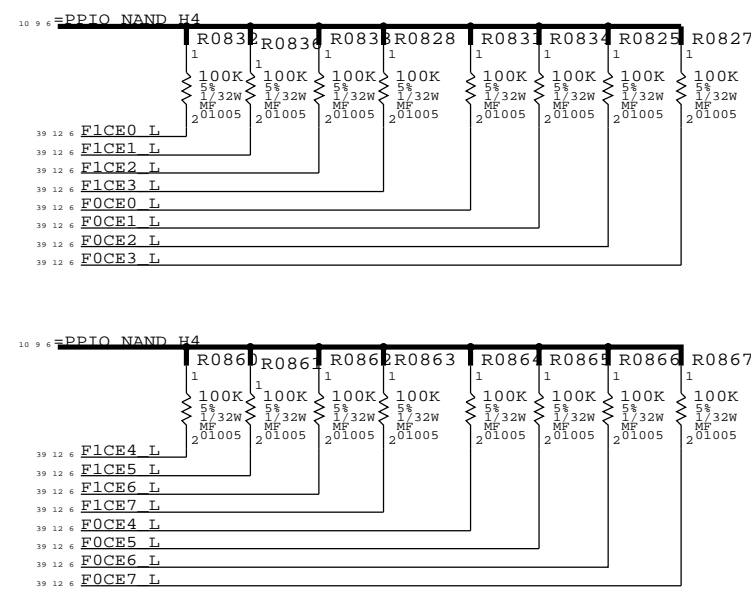
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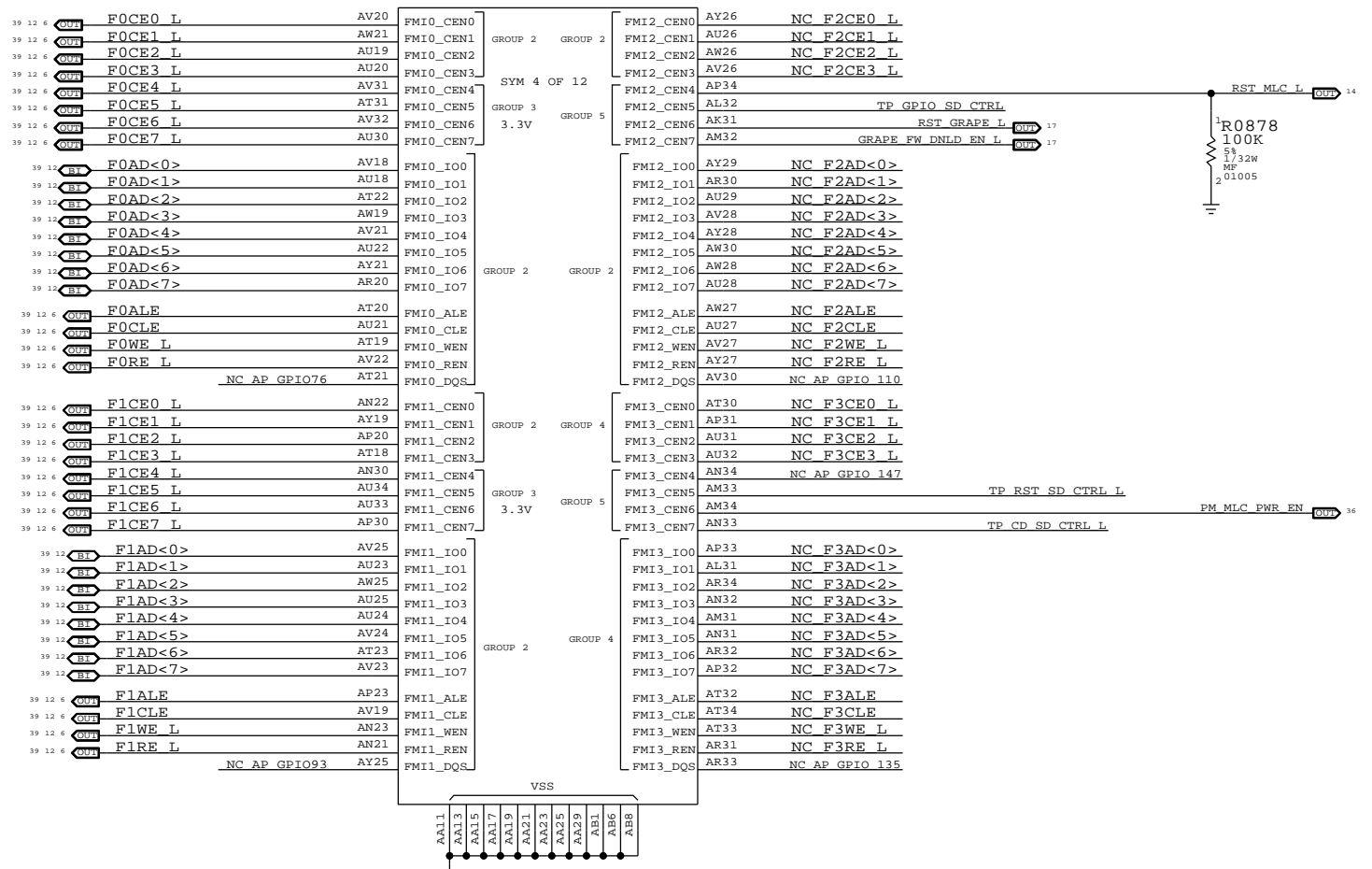
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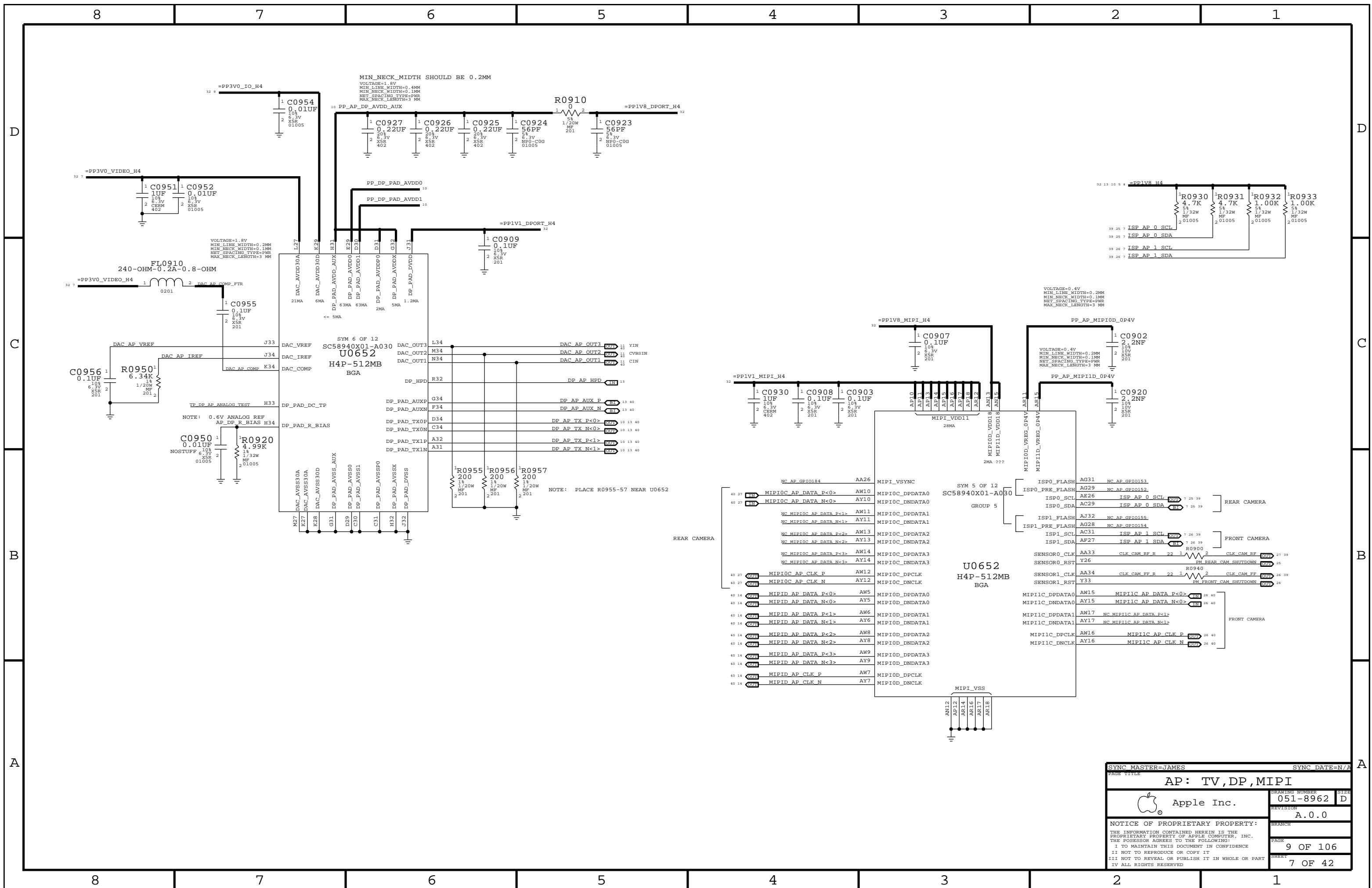
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SYM 12 OF 12  
SC58940X01-A030



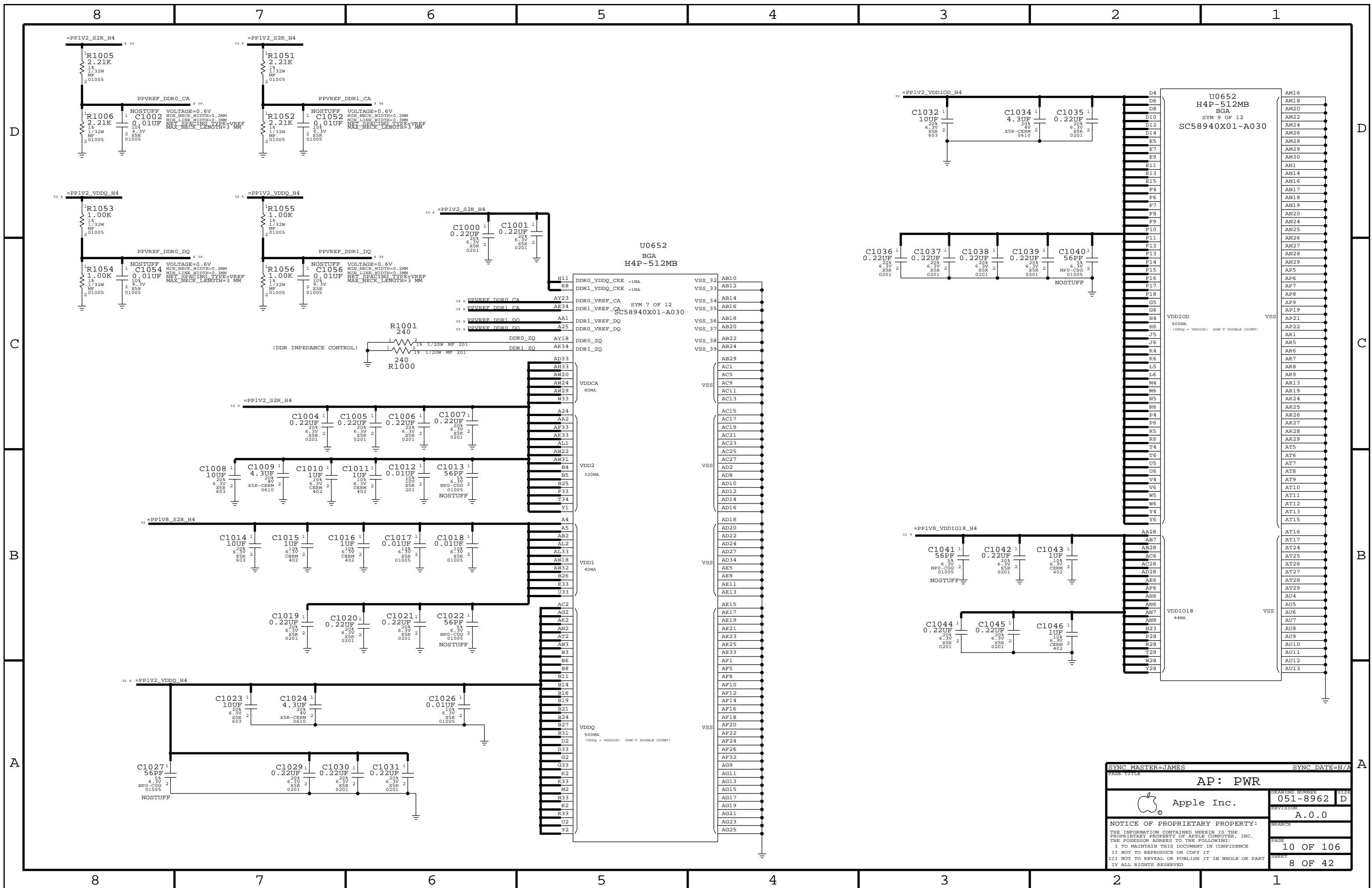
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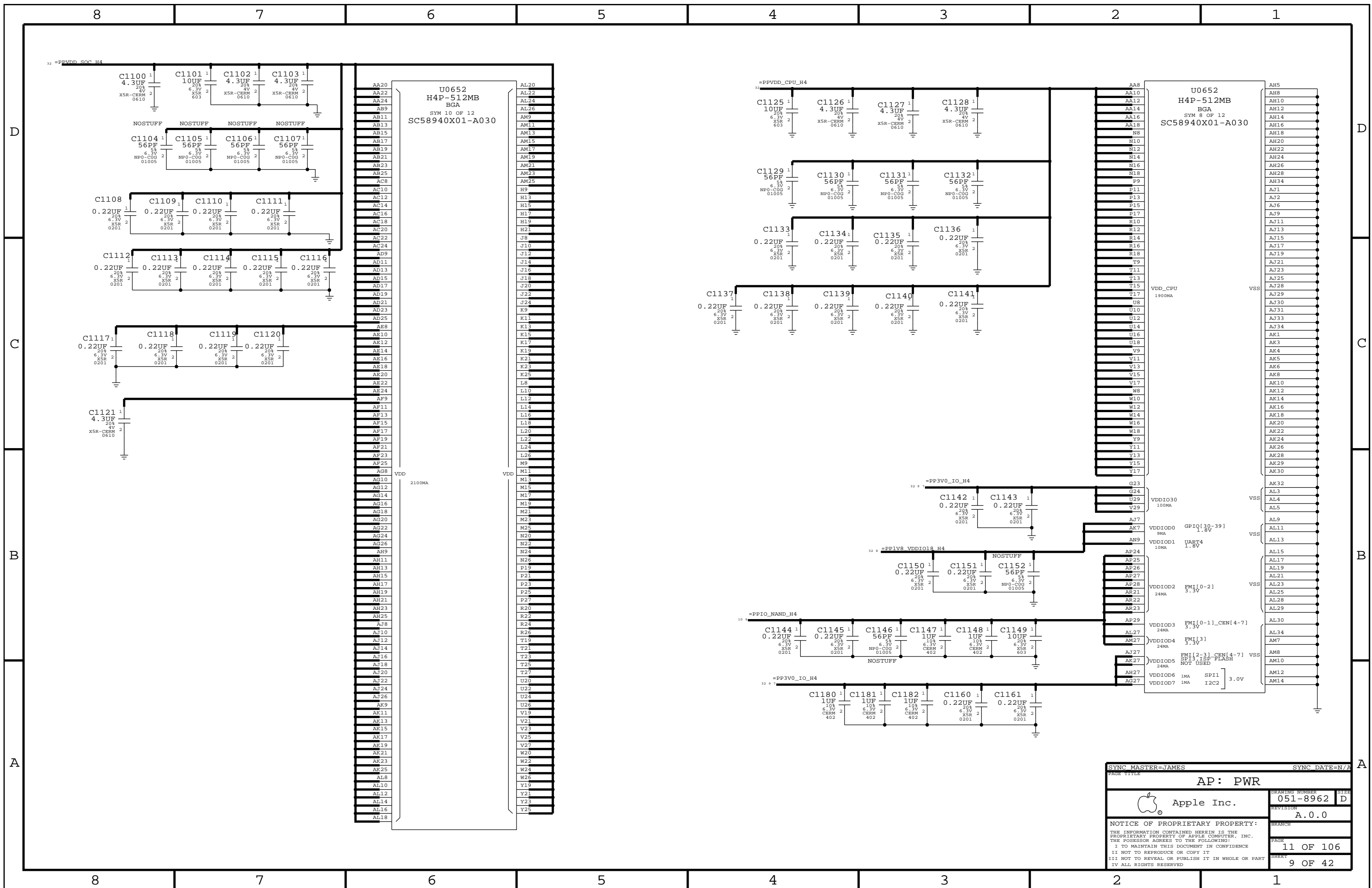
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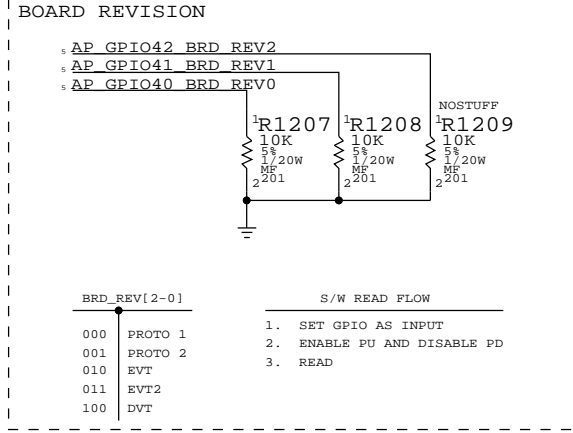
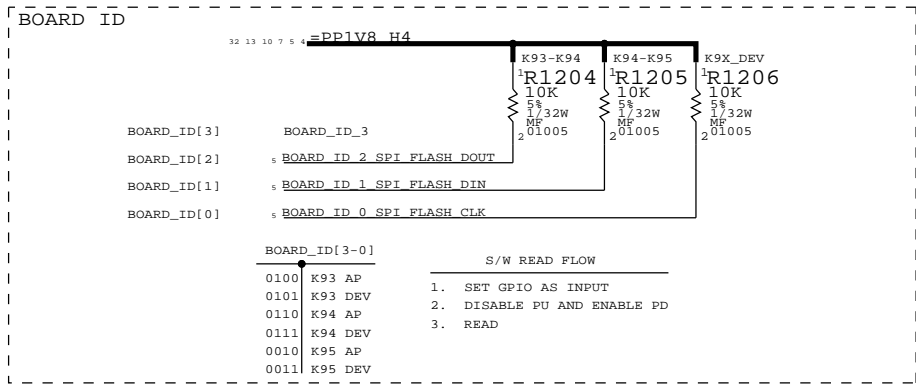
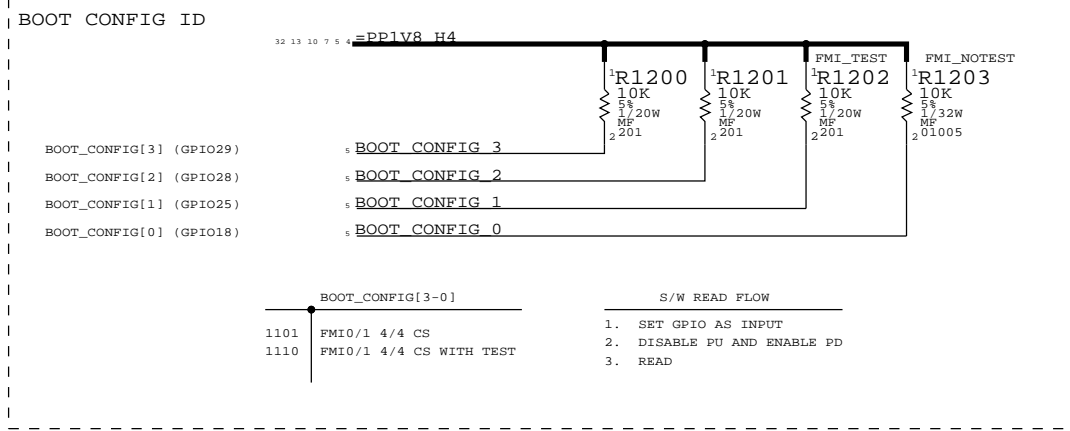
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Apple Inc.	DRAWING NUMBER	051-8962	SIZE
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<b>AP: PWR</b>		DRAWING NUMBER	SIZE
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		PAGE	SHEET
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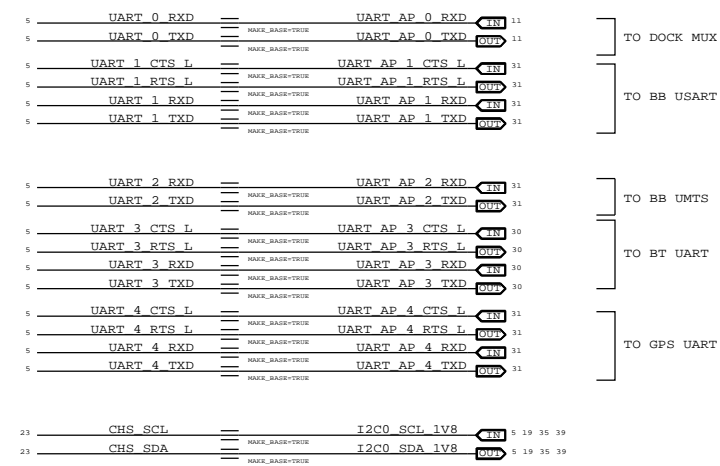
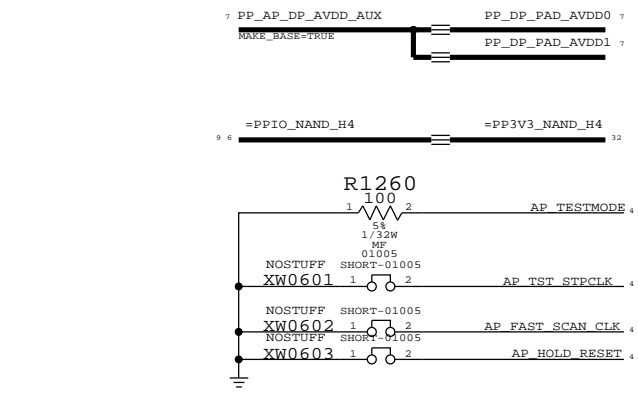
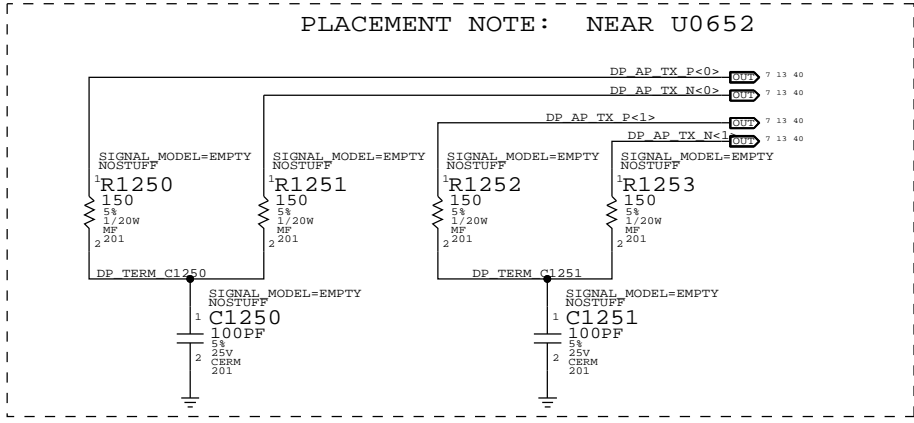
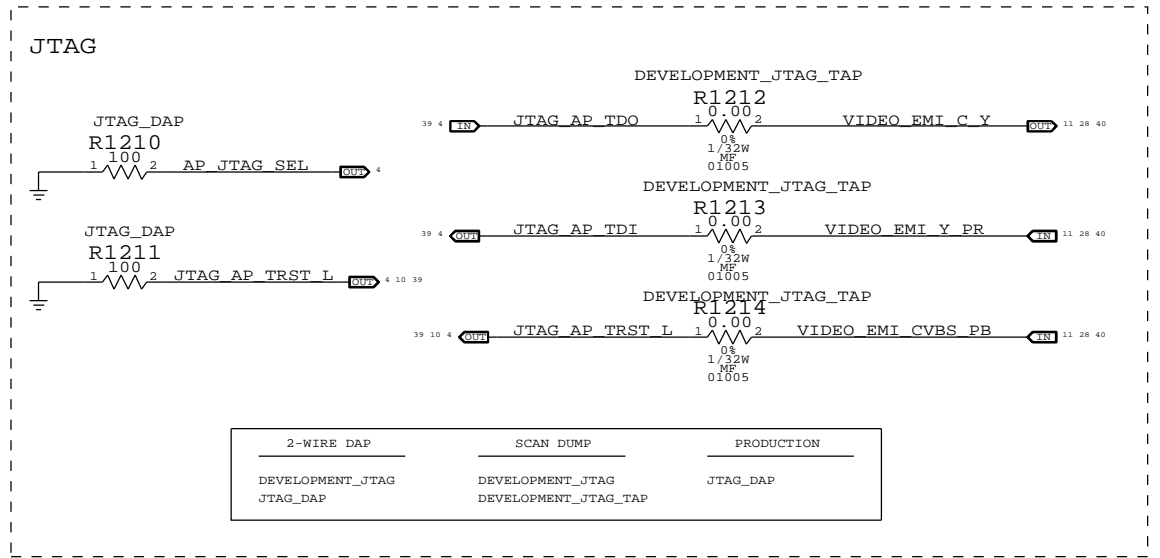
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**FOR REFERENCE**

BOOT_CONFIG[3:0]	
0000	SPI0
0001	SPI3
0010	SPI0 W/TEST
0011	SPI3 W/TEST
0100	FMIO 2CS
0101	FMIO 4CS
0110	FMIO 4CS W/TEST
0111	RESERVED
1000	FMII 2 CS
1001	FMII 4 CS
1010	FMII 4CS W/TEST
1011	RESERVED
1100	FMIO/1 2/2 CS
1101	FMIO/1 4/4 CS
1110	FMIO/1 4/4 CS W/TEST
1111	RESERVED

CURRENT SETTING ->



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**AP: MISC & ALIASES**

Apple Inc.

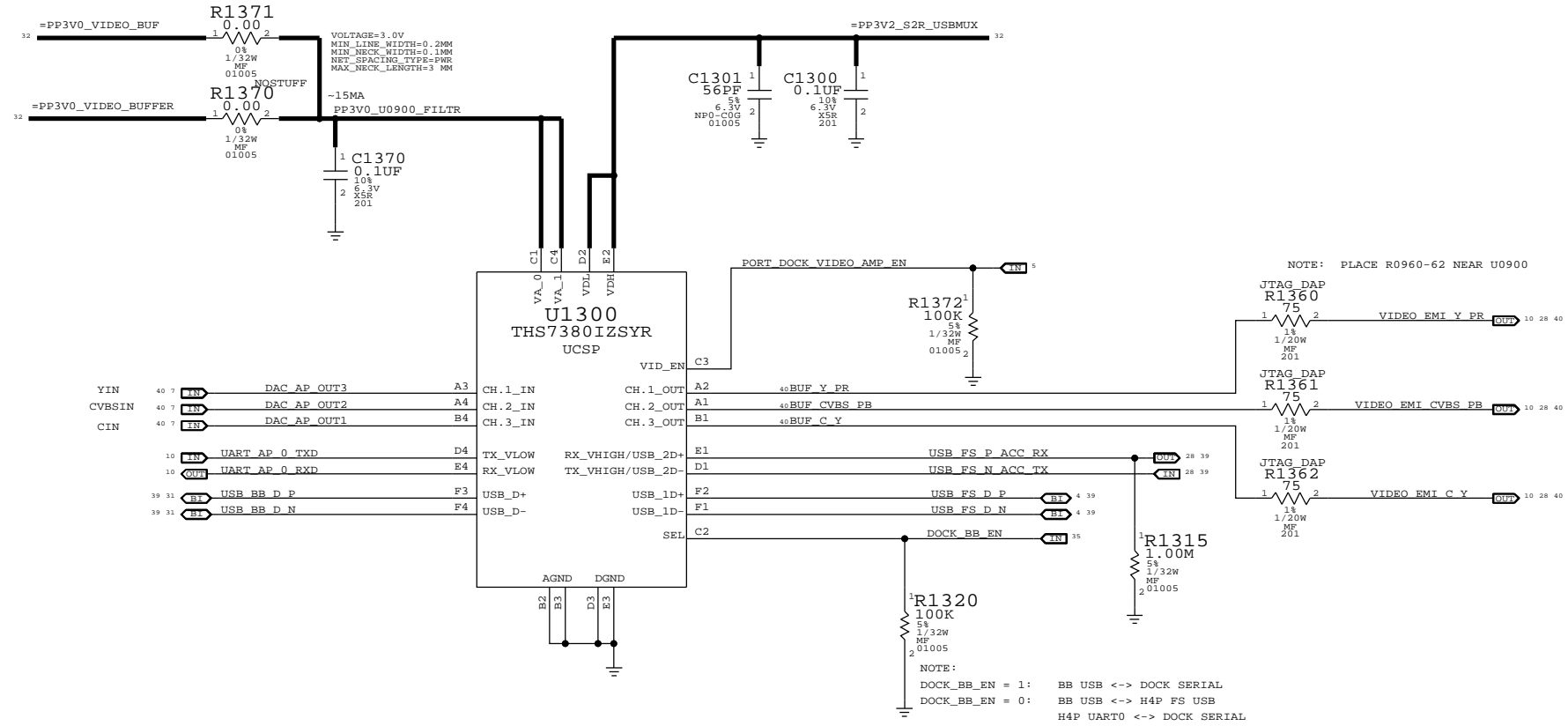
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REVISION: A.0.0

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PAGE: 12 OF 106 SHEET: 10 OF 42

NOTE:  
LDO3 PROVIDES 50MA TO BOTH H4P AND U1300  
IF THAT'S NOT ENOUGH, STUFF R1371 AND NOSTUFF R1370



SYNC MASTER=JAMES		SYNC DATE=N/A	
PAGE TITLE AP: VIDEO BUFFER, BB USB MUXES			
DRAWING NUMBER 051-8962		SIZE D	
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### 16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	1	TOSHIBA 32NM 16GB RAW	U1400	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	16GB_PROD	U1400	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	16GB_PROD	U1400	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	16GB_PROD	U1400	HYNIX 26NM 16GB PPN

### 32GB FLASH CONFIGURATIONS

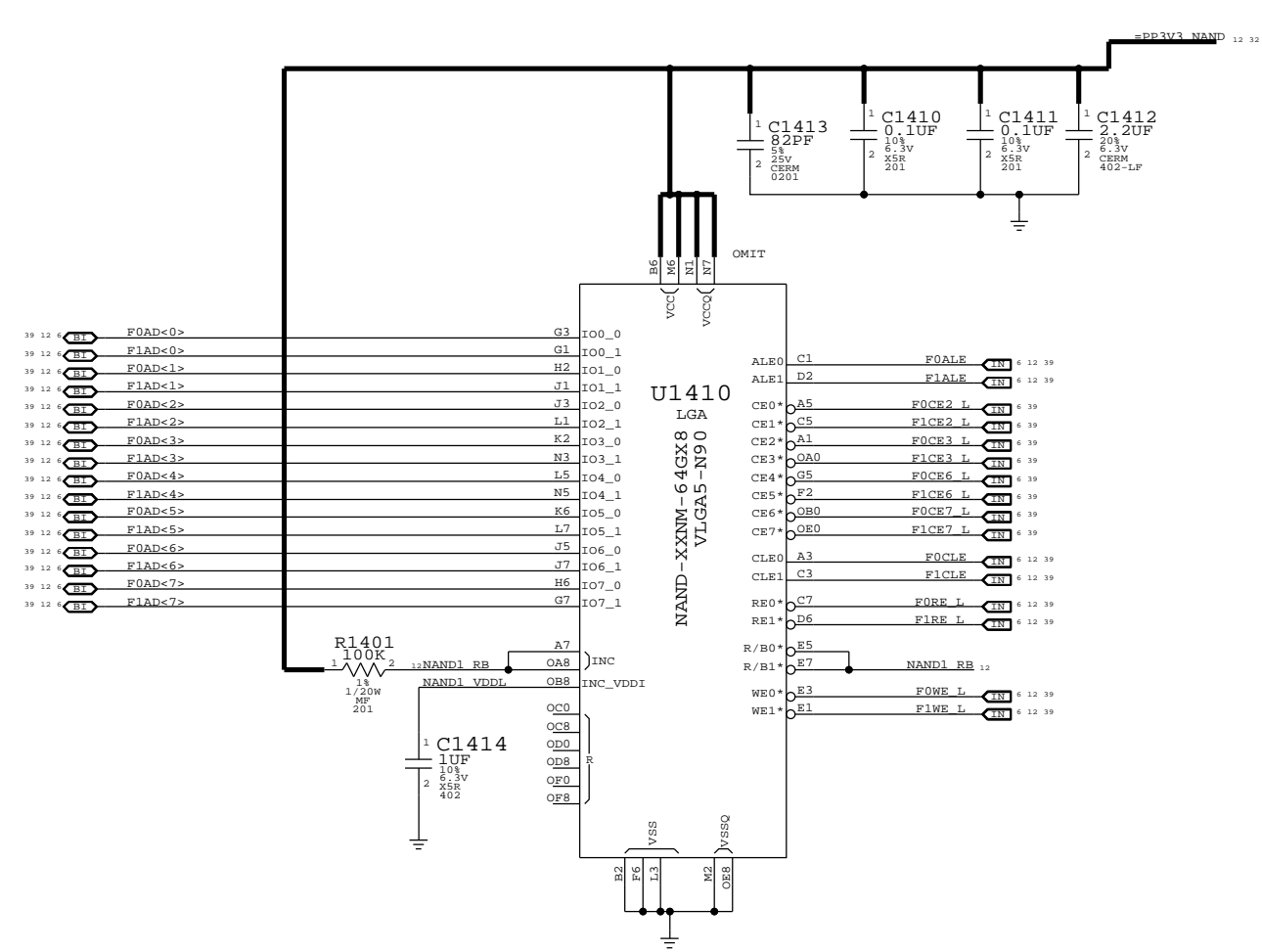
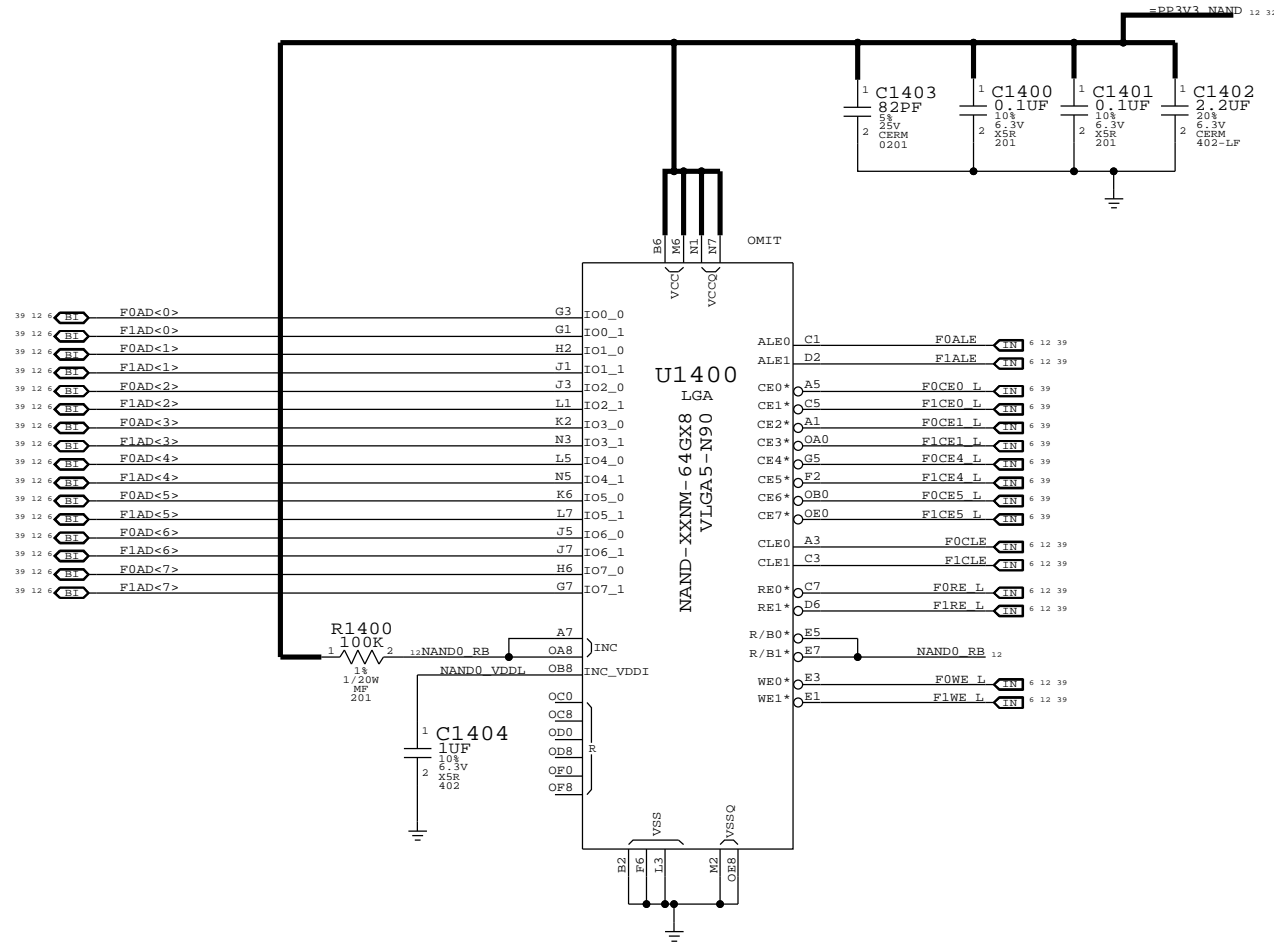
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	2	TOSHIBA 32NM 16GB RAW	U1400,U1410	32GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	32GB_PROD	U1400,U1410	HYNIX 26NM 16GB PPN

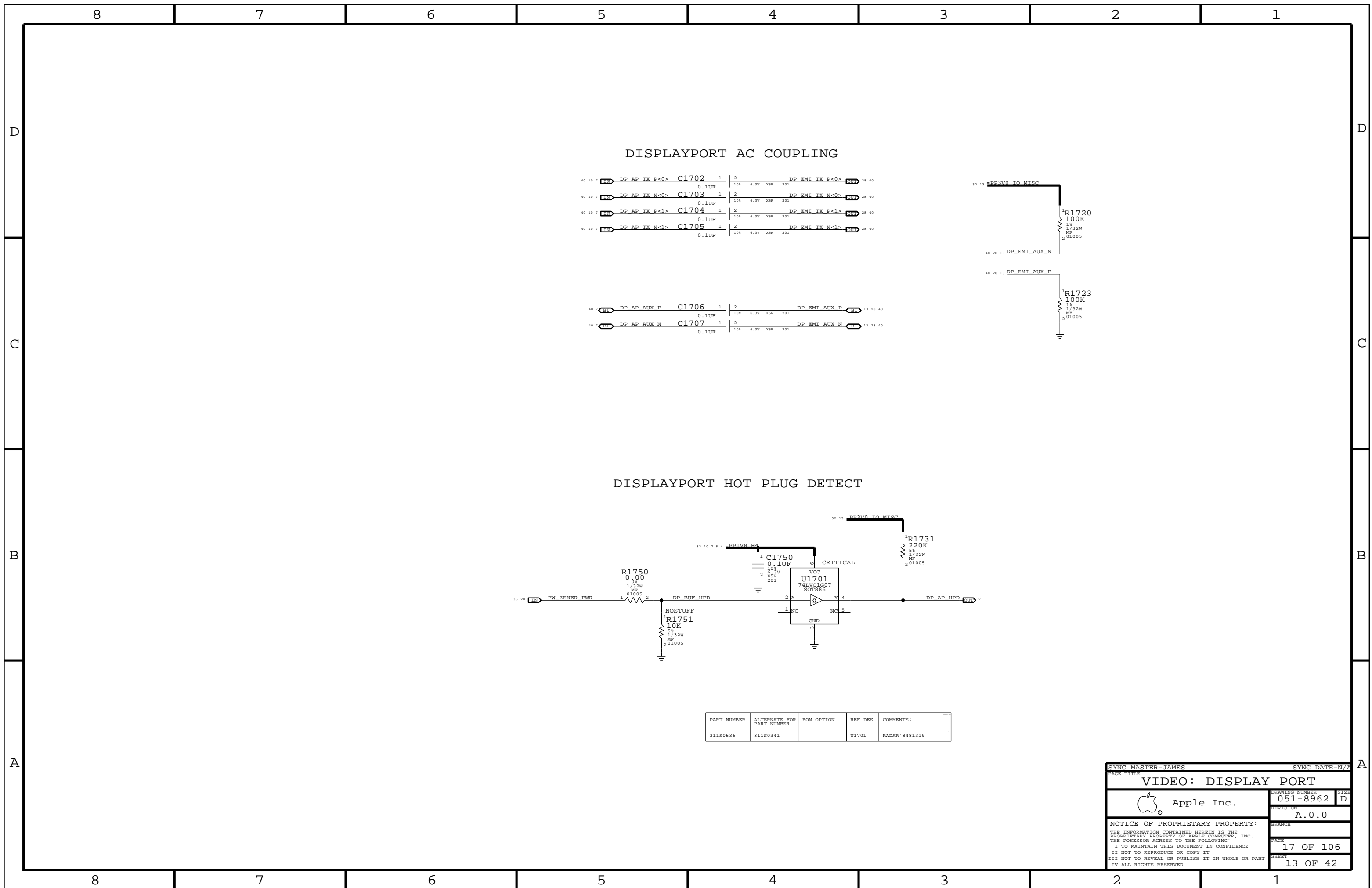
### 64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0702	2	TOSHIBA 32NM 32GB RAW	U1400,U1410	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0665	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 35NM 32GB RAW
335S0791	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 27NM 32GB RAW
335S0722	335S0702	64GB_PROD	U1400,U1410	SANDISK 32NM 32GB RAW
335S0782	335S0702	64GB_PROD	U1400,U1410	HYNIX 26NM 32GB PPN



SYNC MASTER=JONATHAN		SYNC DATE=N/A	
<b>NAND</b>			
Apple Inc.		DRAWING NUMBER	SIZE
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		12 OF 42	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0536	311S0341		U1701	RADAR:8481319

SYNC MASTER=JAMES SYNC DATE=N/A

**VIDEO: DISPLAY PORT**

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

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14	MLC_SDA_3V3	---	MLC_MUX_SDA_3V3	14
14	MLC_SCL_3V3	---	MLC_MUX_SCL_3V3	14

SYNC MASTER=MIKE		SYNC DATE=N/A	
<b>VIDEO: MLC ALIASES</b>			
 Apple Inc.		DRAWING NUMBER	051-8962
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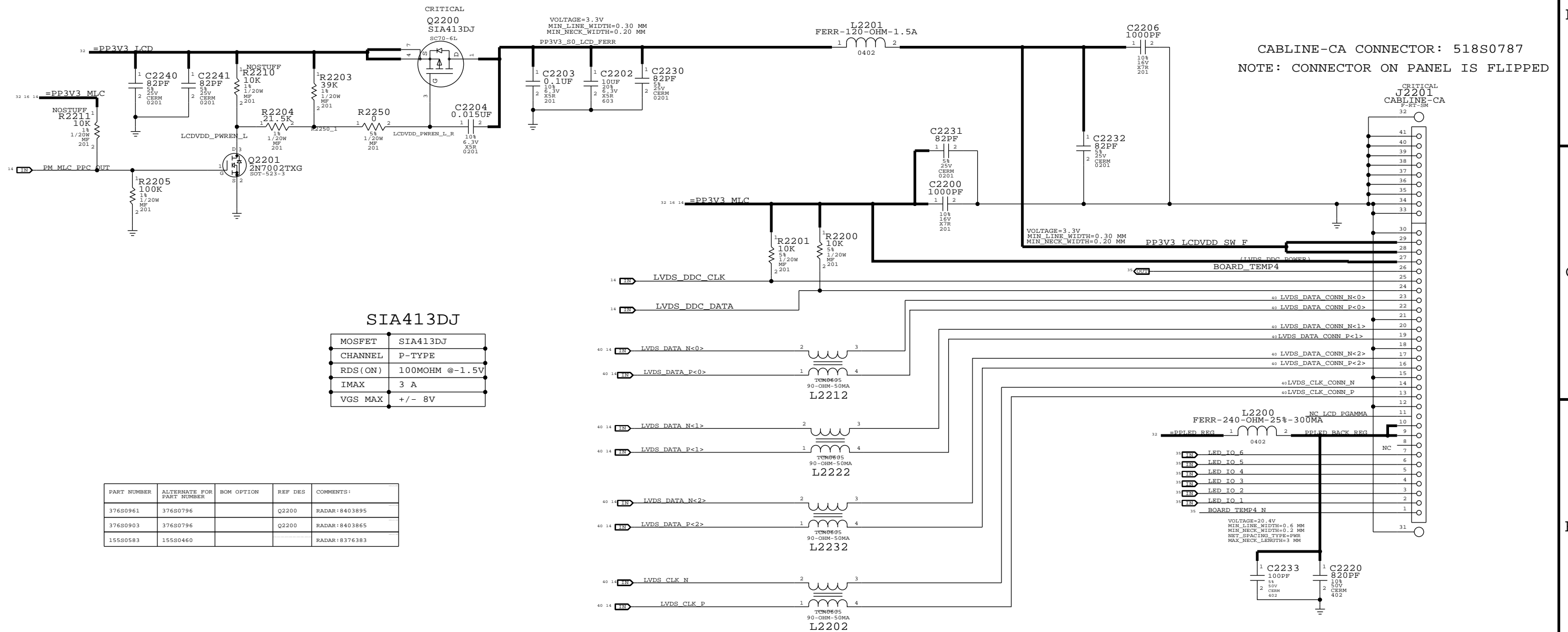
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# LVDS CONNECTOR



**SIA413DJ**

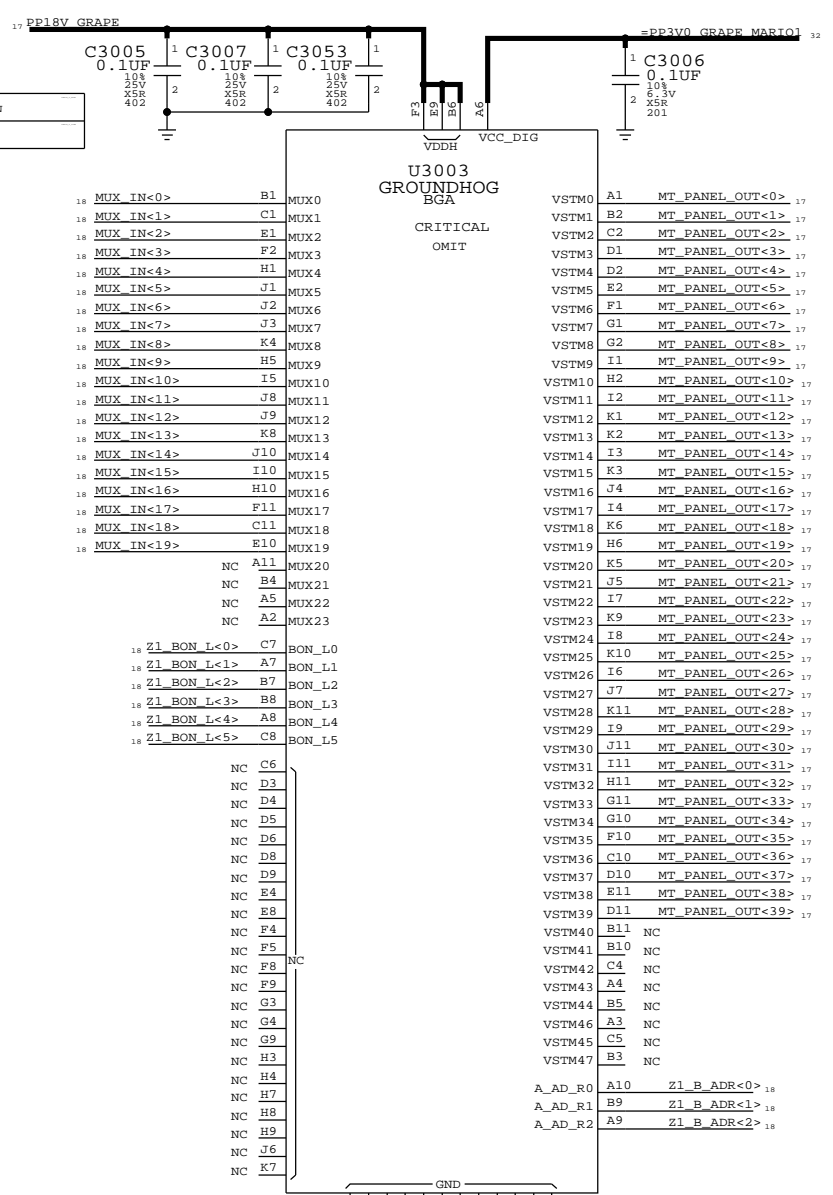
MOSFET	SIA413DJ
CHANNEL	P-TYPE
RDS (ON)	100MOHM @-1.5V
IMAX	3 A
VGS MAX	+/- 8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0961	376S0796		Q2200	RADAR:8403895
376S0903	376S0796		Q2200	RADAR:8403865
155S0583	155S0460			RADAR:8376383

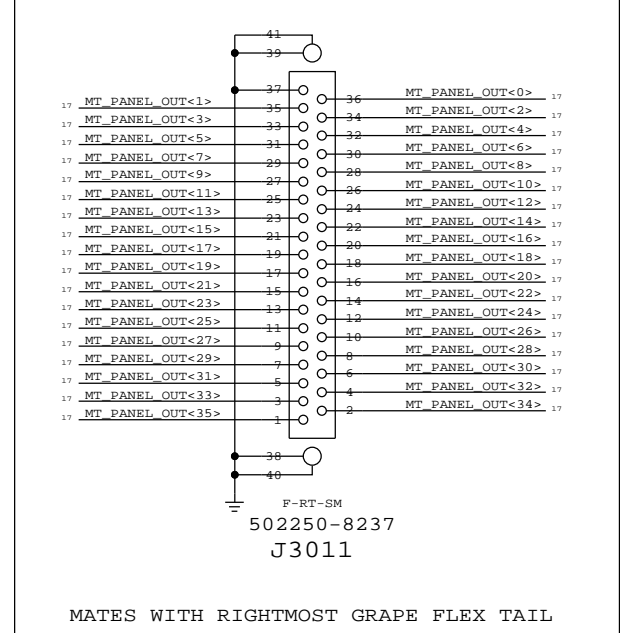
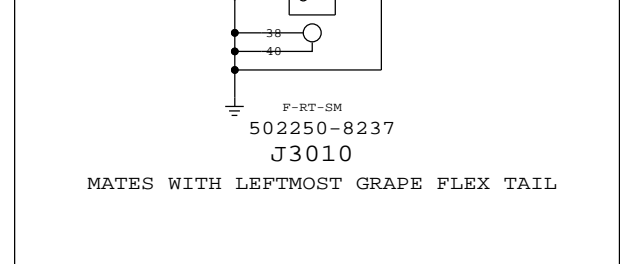
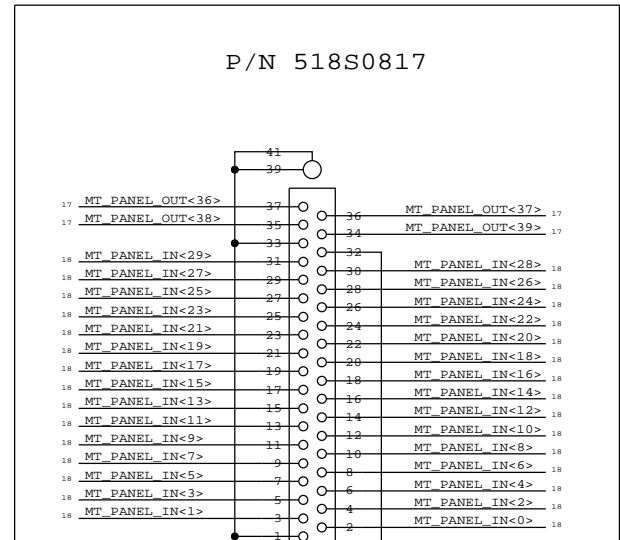
NOSTUFF RESISTORS ARE THERE TO INVESTIGATE POSSIBILITY OF REMOVING THE CHOKE

SYNC MASTER=ALEX		SYNC DATE=N/A	
PAGE TITLE <b>VIDEO: LVDS CONNECTOR</b>			
Apple Inc.		DRAWING NUMBER 051-8962	SIZE D
		REVISION A.0.0	BRANCH
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		PAGE 22 OF 106	SHEET 16 OF 42

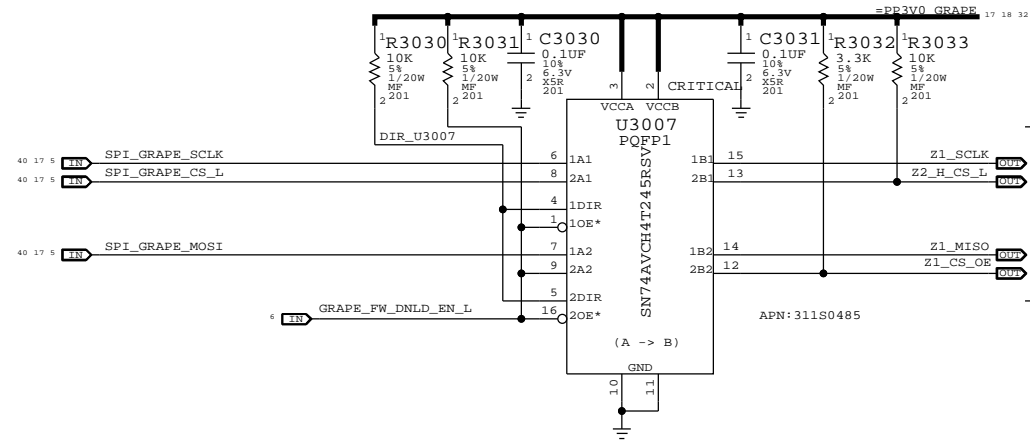
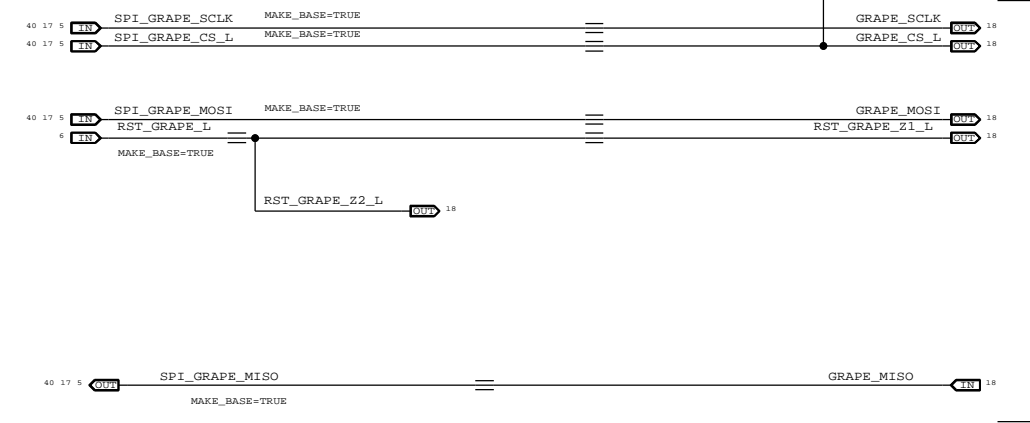
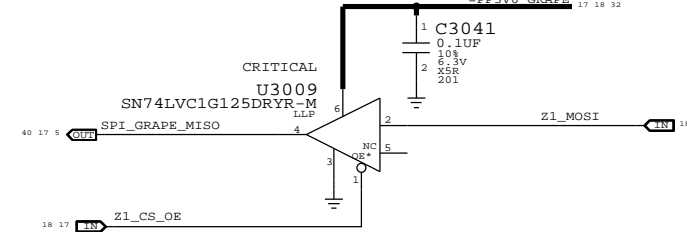
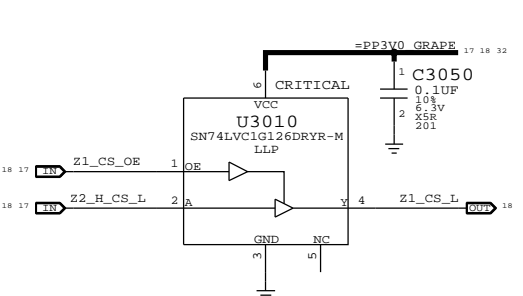
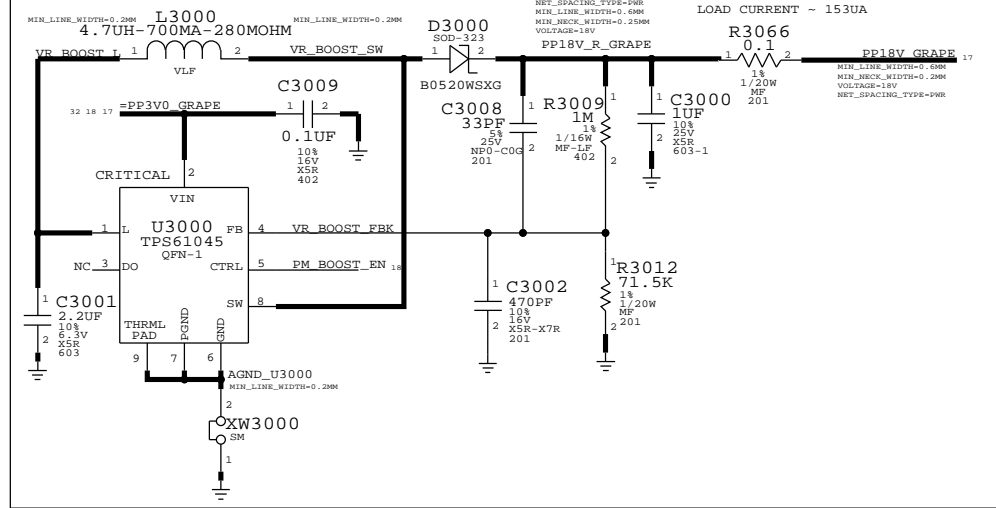
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34380525	1	IC, ASIC, GROUNDHOG B0, 120B BGA	U3003	CRITICAL	



CONNECTORS TO GRAPE FLEX



BOOST CONVERTOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
31150523	31150485		U3007	
31150524	31150533		U3009	
31150525	31150532		U3010	

SYNC MASTER=RAMSIN SYNC DATE=N/A

**GRAPE: GROUNDHOG, CONN, BOOST**

Apple Inc.

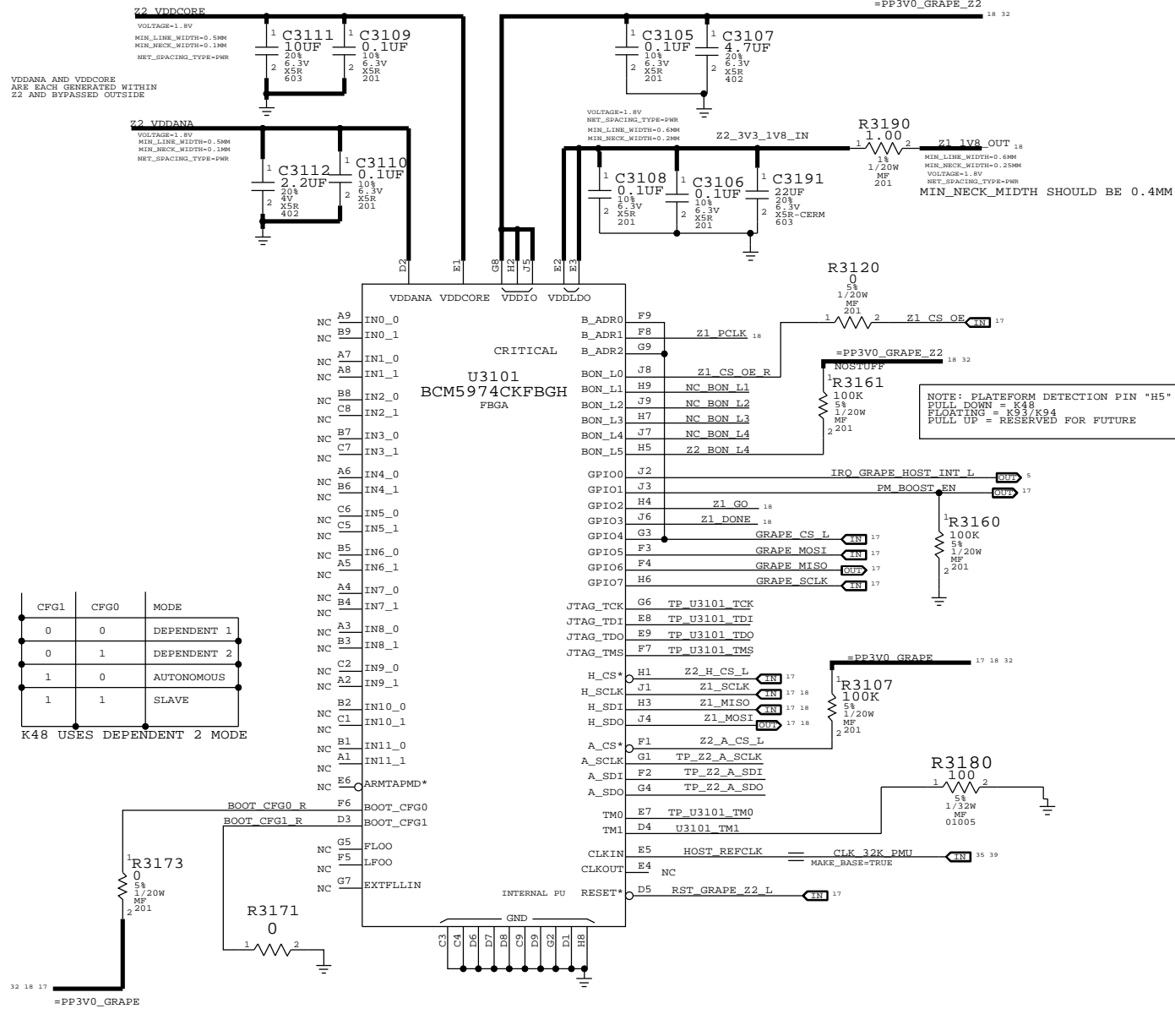
DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

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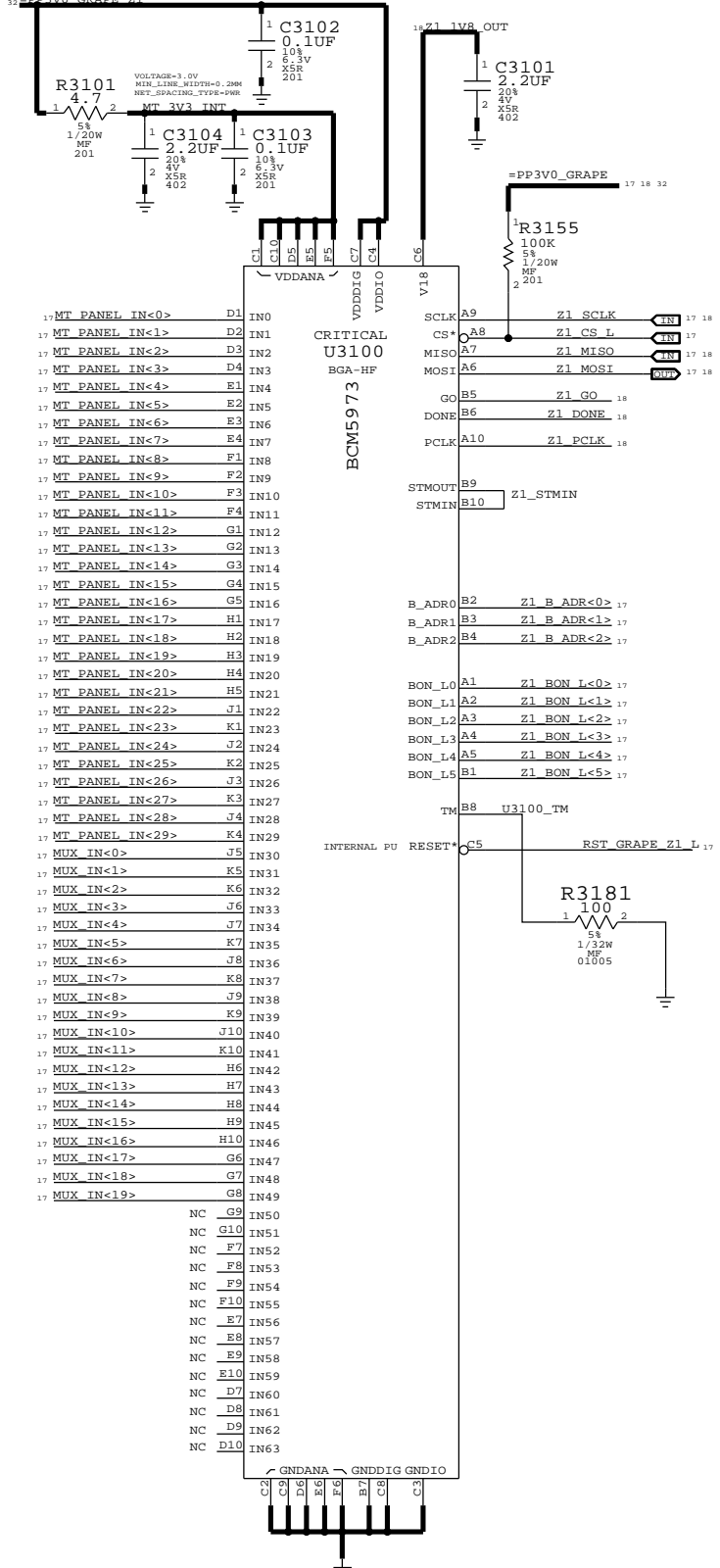
PAGE: 30 OF 106 SHEET: 17 OF 42

ARM9 MCU (Z2 BASED)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0648		C3107	RADAR: 8392120
138S0618	138S0648		C3107	BOM CONSOLIDATION

ZEPHYR 1+ ASIC



SYNC MASTER=RAMSIN SYNC DATE=N/A

GRAPE: Z1, Z2

Apple Inc.

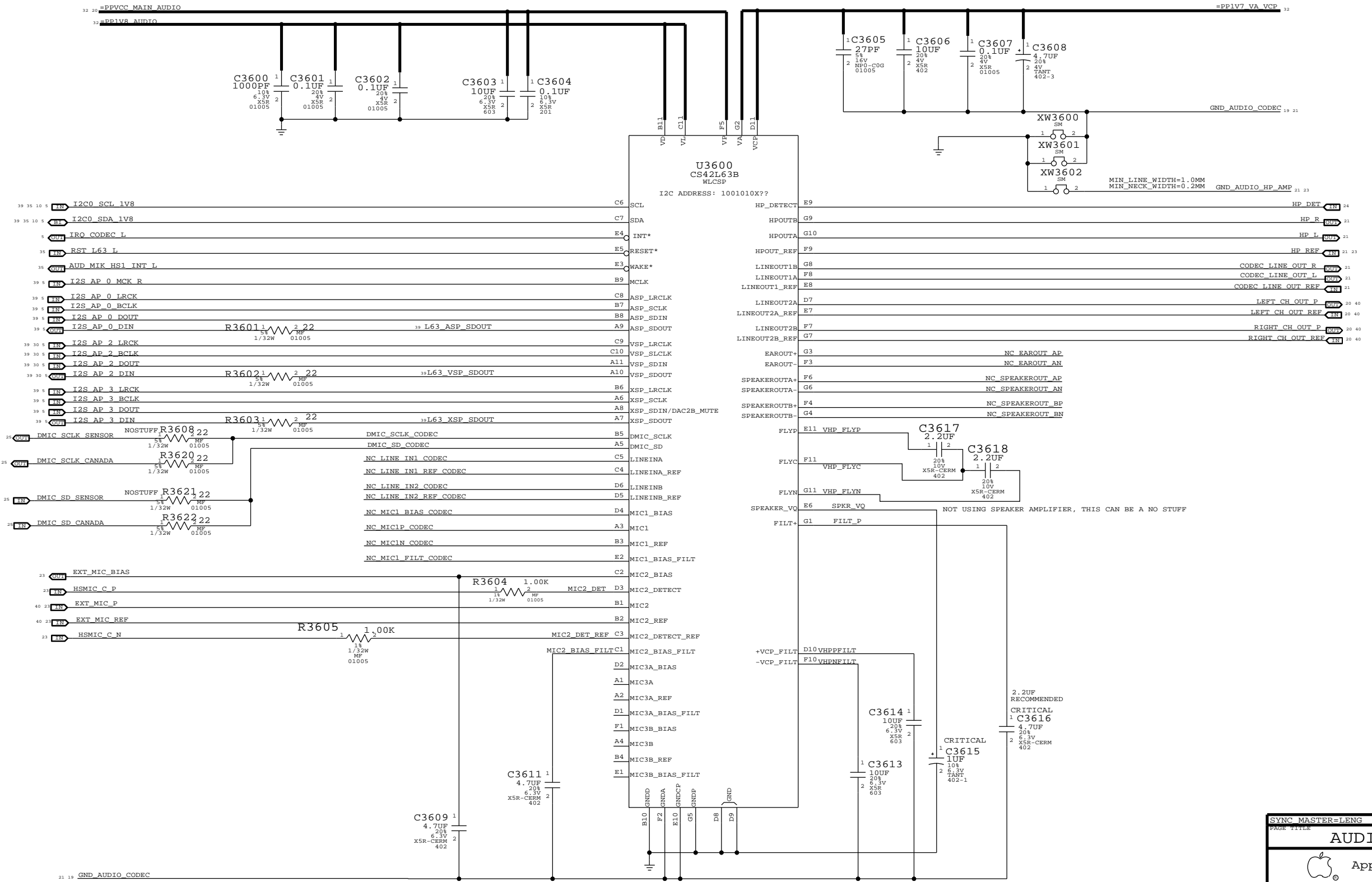
051-8962  
REVISION A.0.0

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# L63 AUDIO CODEC

APN: 338S0940



MIN LINE WIDTH=0.6MM  
MIN NECK WIDTH=0.2MM  
MAX NECK LENGTH=75 MM

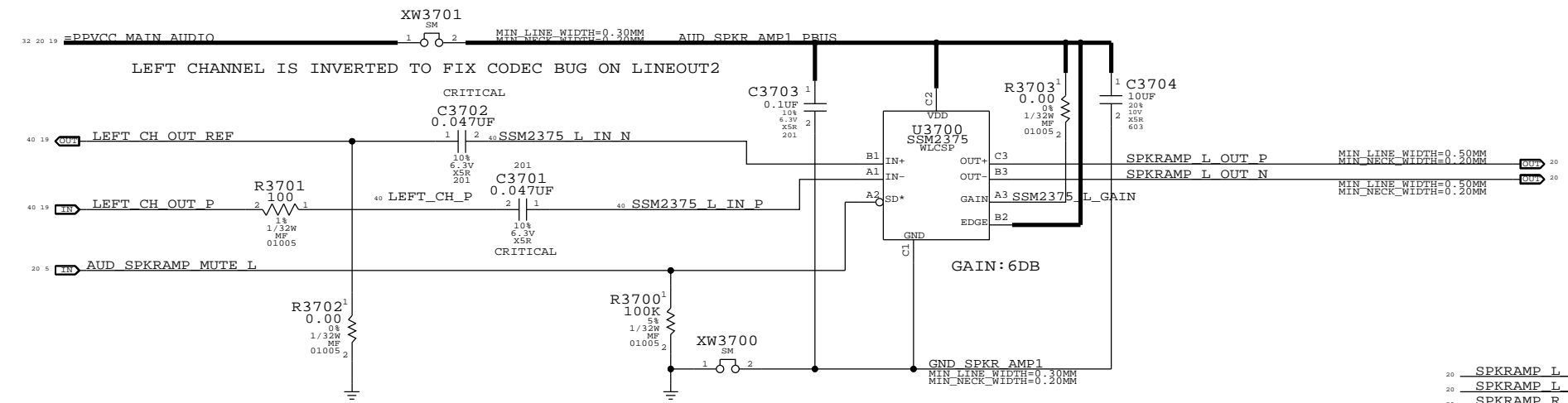
SYNC MASTER=LENG		SYNC DATE=N/A	
<b>AUDIO: L63 CODEC</b>			
Apple Inc.		DRAWING NUMBER 051-8962	SIZE D
REVISION A.0.0		BRANCH	
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# SPEAKER AMPLIFIER

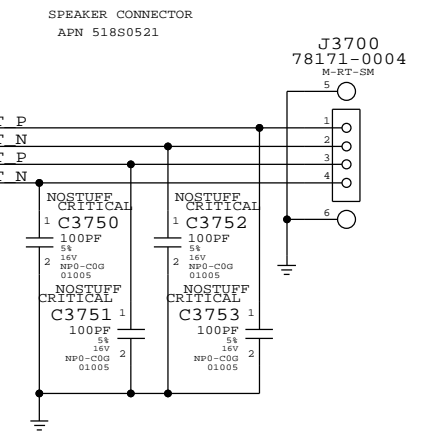
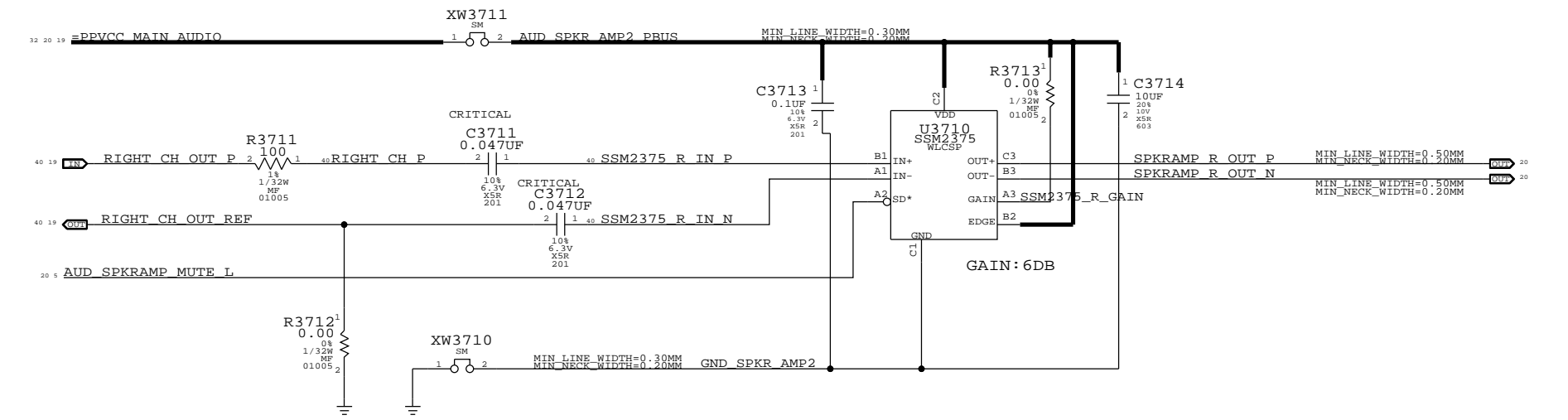
APN:353S2958

80HZ +/- XXX%      TURN ON TIME: 7.5MS  
 TURN ON DELAY: 20MS

GAIN	VDD	GND
12DB	47K	NC
9DB	NC	47K
6DB	SHORT	NC
3DB	NC	NC
0DB	NC	SHORT

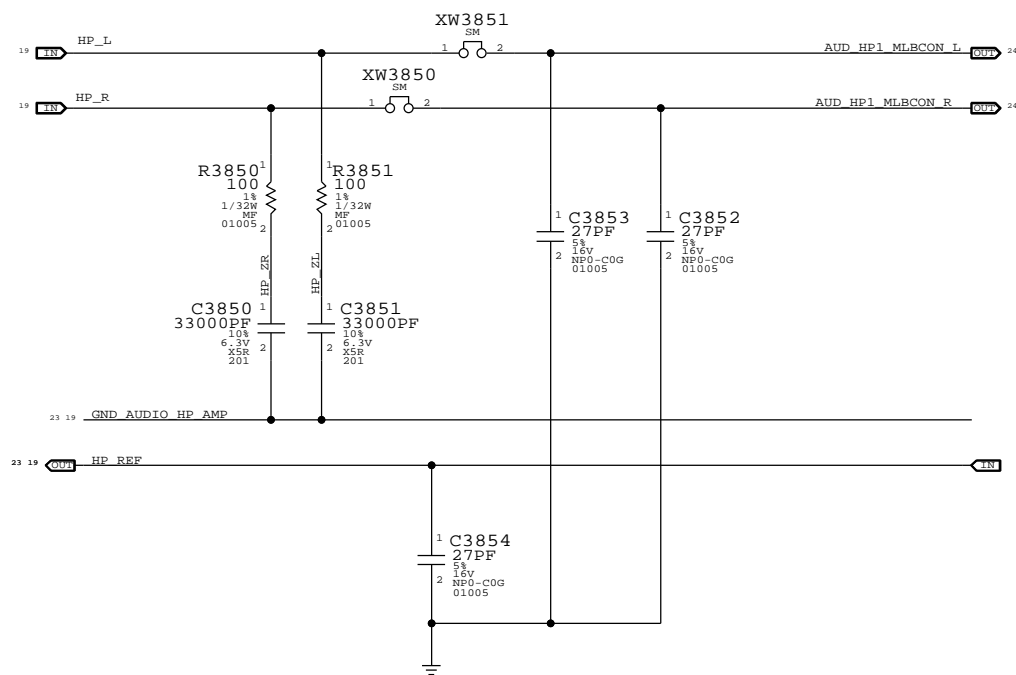


L63 LINEOUT2A IS CONNECTED TO U3700  
 L63 LINEOUT2B IS CONNECTED TO U3710

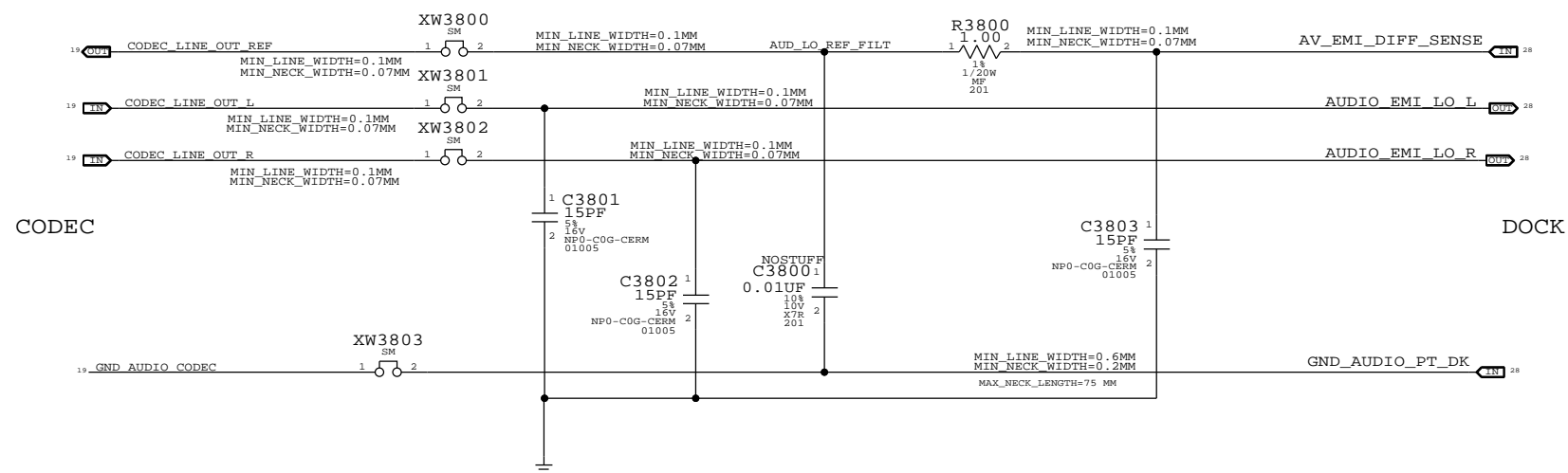


SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE: AUDIO: SPEAKER AMP			
DRAWING NUMBER: 051-8962		SIZE: D	
REVISION: A.0.0		BRANCH:	
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HEADPHONE OUTPUT ZOBEL NETWORK



DOCK LINE OUTPUT



SYNC MASTER=LENG		SYNC DATE=N/A	
<b>AUDIO: HEADPHONE OUT</b>			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8962	D
		REVISION	
		A.0.0	
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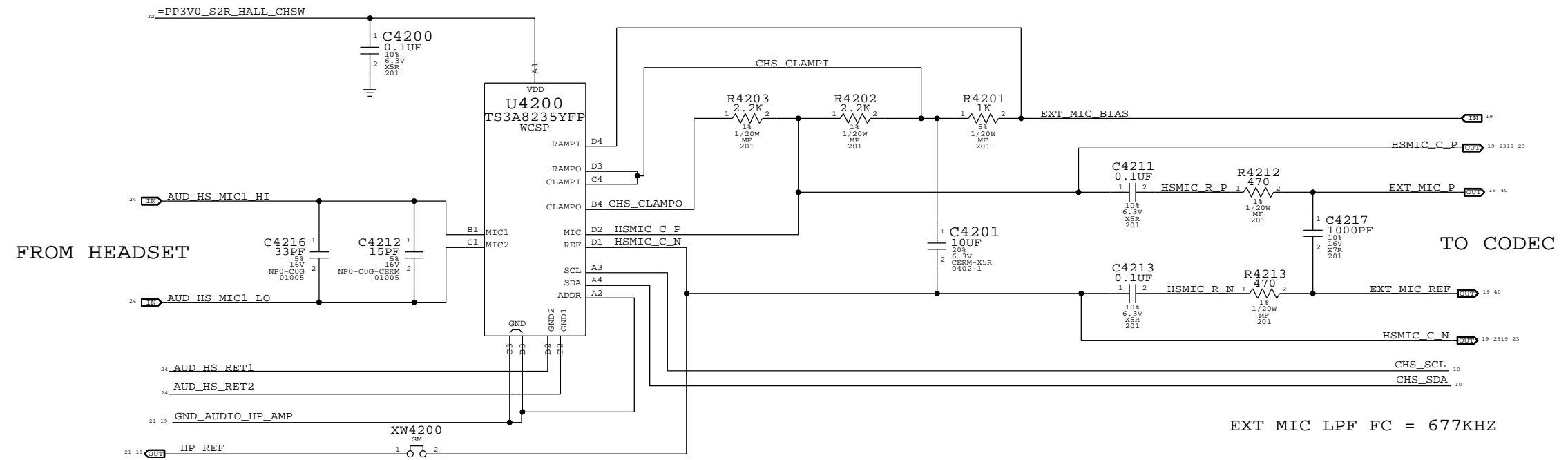
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2

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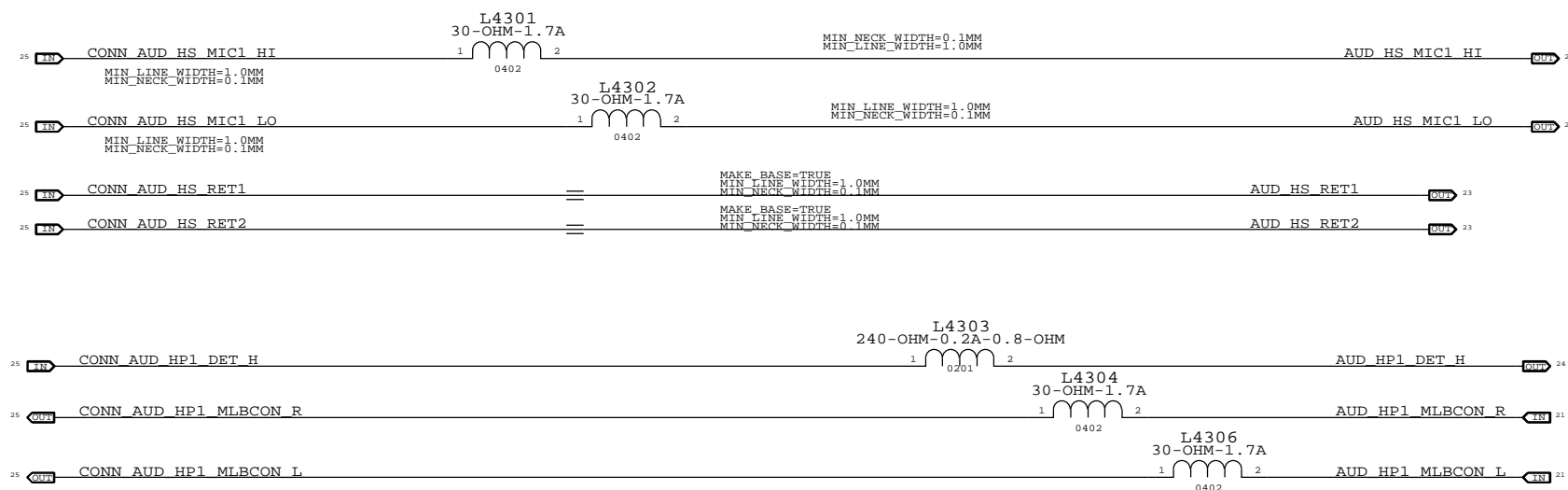
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<b>AUDIO: BLANK</b>			
 Apple Inc.		DRAWING NUMBER	051-8962
		REVISION	A.0.0
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		PAGE	39 OF 106
		SHEET	22 OF 42

EXTERNAL (HEADSET) MIC INPUT CIRCUITRY

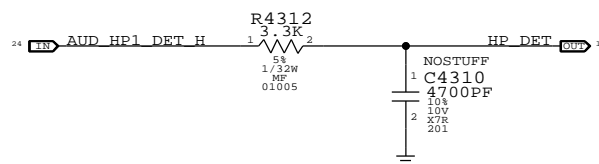


SYNC MASTER=LENG		SYNC DATE=N/A	
AUDIO: DETECT/MIC BIAS			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8962	D
		REVISION	
		A.0.0	
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HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29  
 PLACE ALL COMPONENTS NEAR J5501



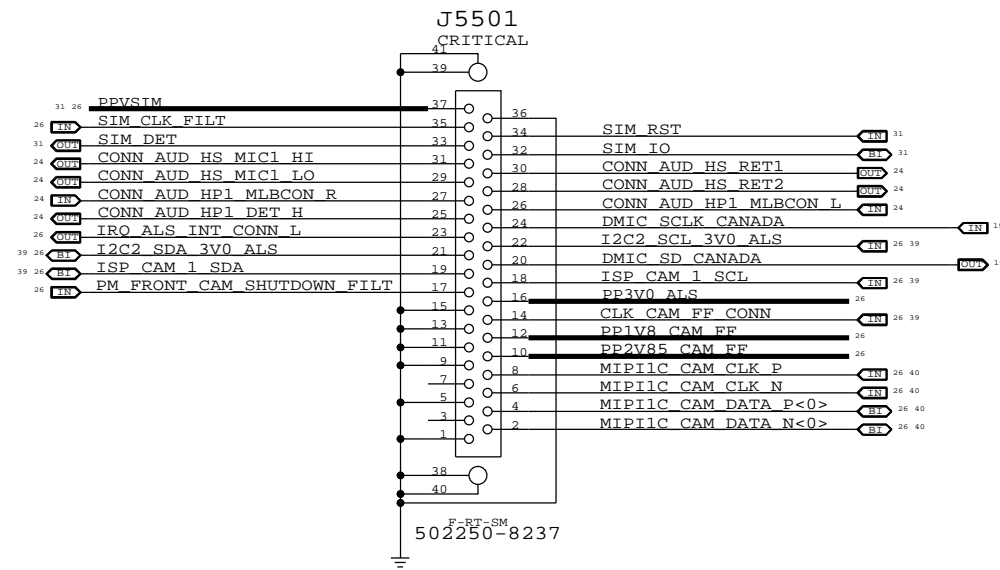
HEADSET JACK INSERTION DETECT



SYNC MASTER=LENG		SYNC DATE=N/A	
AUDIO: HP/MIC FILTERS			
DRAWING NUMBER		SIZE	
051-8962		D	
REVISION		BRANCH	
A.0.0			
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# CANADA FLEXES CONN.

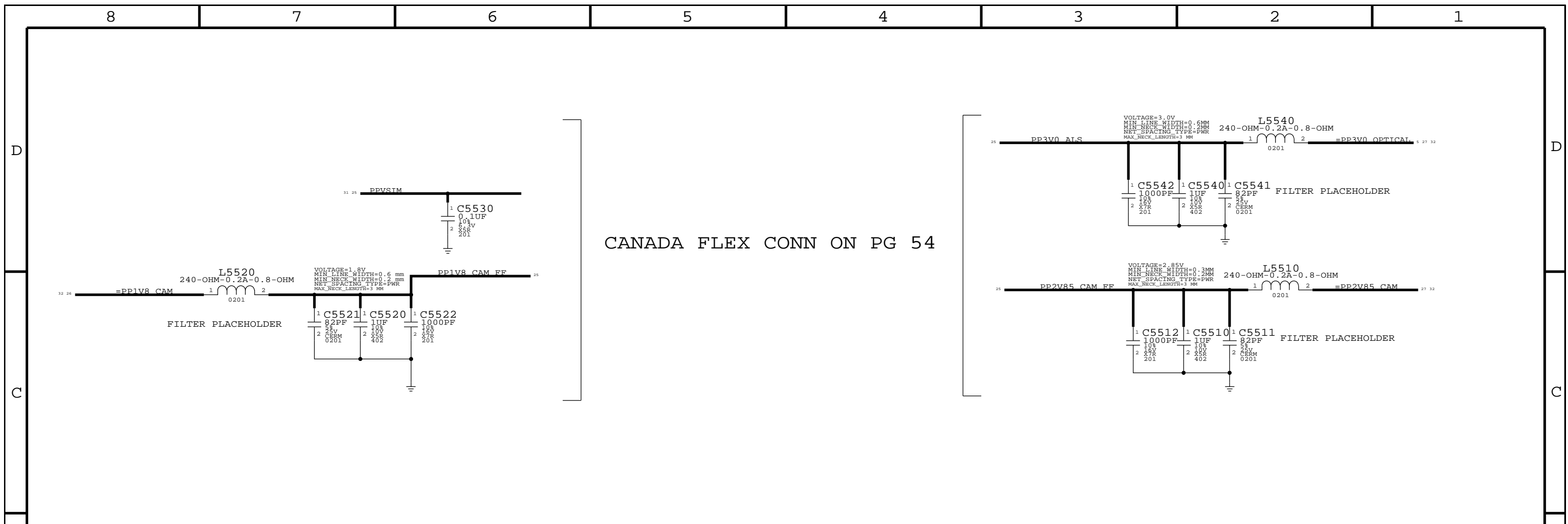
APN: 518S0817



# SENSOR BOARD CONN ALIASES

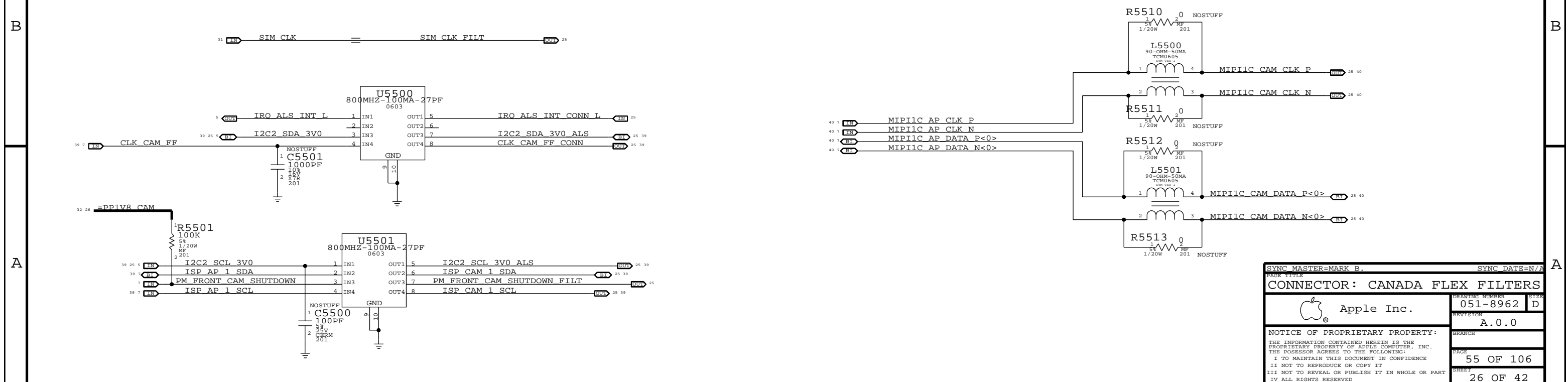
39	CLK CAM RF FILT	==	CONN CLK CAM RF FILT	27
40	MIP10C CAM DATA N<0>	MAKE_BASE-TWIR	CONN MIP10C CAM DATA N<0>	27
40	MIP10C CAM DATA P<0>	MAKE_BASE-TWIR	CONN MIP10C CAM DATA P<0>	27
40	MIP10C CAM CLK N	MAKE_BASE-TWIR	CONN MIP10C CAM CLK N	27
40	MIP10C CAM CLK P	MAKE_BASE-TWIR	CONN MIP10C CAM CLK P	27
7	PM REAR CAM SHUTDOWN	MAKE_BASE-TWIR	CONN PM REAR CAM SHUTDOWN	27
27	PP1V8 SENSOR FILT	MAKE_BASE-TWIR	CONN PP1V8 SENSOR FILT	27
27	PP2V85 CAM REAR	MAKE_BASE-TWIR	CONN PP2V85 CAM REAR	27
19	DMIC SD SENSOR	MAKE_BASE-TWIR	CONN DMIC SD SENSOR	27
19	DMIC SCLK SENSOR	MAKE_BASE-TWIR	CONN DMIC SCLK SENSOR	27
19	ISP AP 0 SCL	MAKE_BASE-TWIR	CONN ISP AP 0 SCL	27
19	ISP AP 0 SDA	MAKE_BASE-TWIR	CONN ISP AP 0 SDA	27
19	I2C2 SCL 3V0	MAKE_BASE-TWIR	CONN I2C2 SCL 3V0	27
19	I2C2 SDA 3V0	MAKE_BASE-TWIR	CONN I2C2 SDA 3V0	27
5	IRO ACCEL INT1 L	MAKE_BASE-TWIR	CONN IRO ACCEL INT1 L	27
5	IRO ACCEL INT2 L	MAKE_BASE-TWIR	CONN IRO ACCEL INT2 L	27
5	IRO GYRO INT1	MAKE_BASE-TWIR	CONN IRO GYRO INT1	27
5	IRO GYRO INT2	MAKE_BASE-TWIR	CONN IRO GYRO INT2	27
19	I2C1 SCL 1V8	MAKE_BASE-TWIR	CONN I2C1 SCL 1V8	27
19	I2C1 SDA 1V8	MAKE_BASE-TWIR	CONN I2C1 SDA 1V8	27
5	IRO HALL	MAKE_BASE-TWIR	CONN IRO HALL	27
5	IRO PROX INT L	MAKE_BASE-TWIR	CONN IRO PROX INT L	27
27	PP3V0 S2R HALL FILT	MAKE_BASE-TWIR	CONN PP3V0 S2R HALL	27
15	ONOFF L	MAKE_BASE-TWIR	CONN ONOFF FTR L	27
15	SRL L	MAKE_BASE-TWIR	CONN SRL FTR L	27
15	AUD VOL UP L	MAKE_BASE-TWIR	CONN AUD VOL UP FTR L	27
15	AUD VOL DOWN L	MAKE_BASE-TWIR	CONN AUD VOL DOWN FTR L	27
27	PP3V0 OPTICAL SENS	MAKE_BASE-TWIR	CONN PP3V0 OPTICAL SENS	27

SYNC MASTER=MARK B.		SYNC DATE=N/A	
CONNECTOR: CANADA FLEX CONN, SENSOR PANEL ALIASES			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE D
	REVISION	A.0.0	
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			PAGE 54 OF 106
			SHEET 25 OF 42

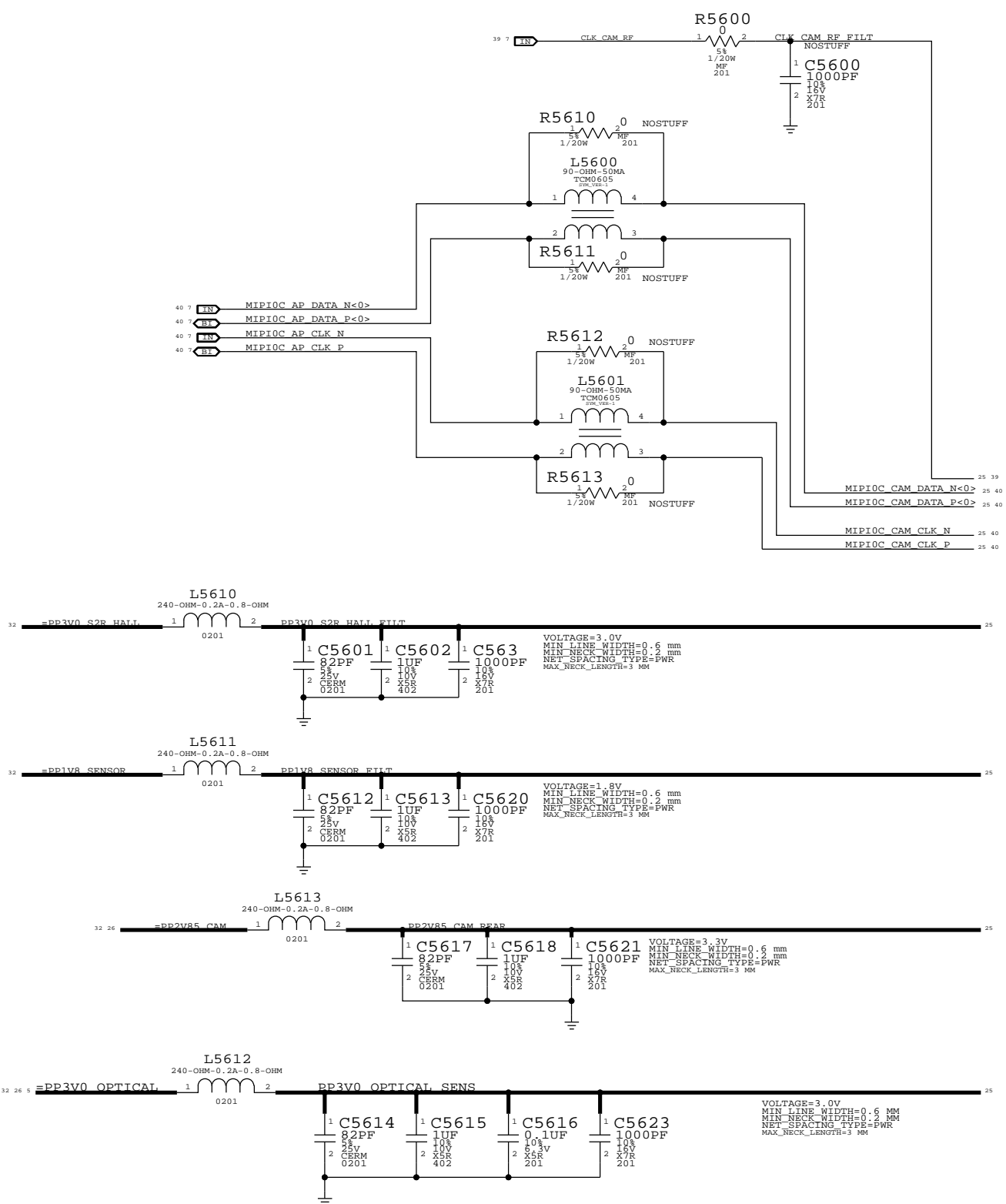


CANADA FLEX CONN ON PG 54

CANADA FLEX SIGNAL FILTERS



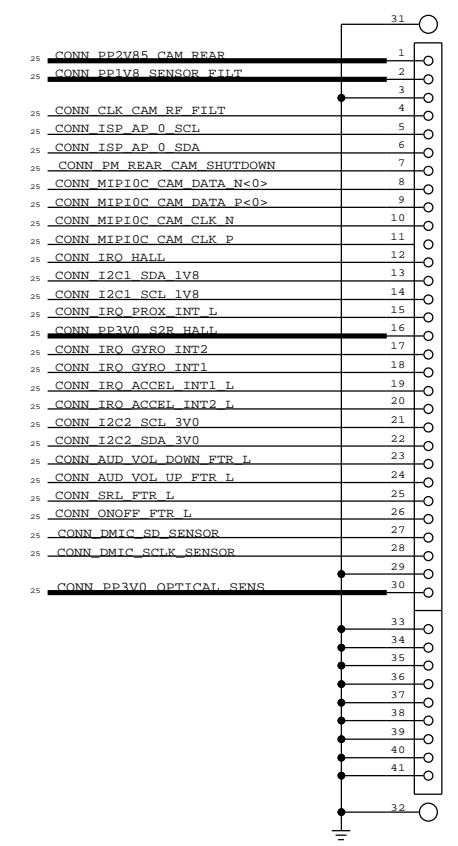
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CONNECTOR: CANADA FLEX FILTERS			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE D
	REVISION	A.0.0	
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SHEET		26 OF 42	



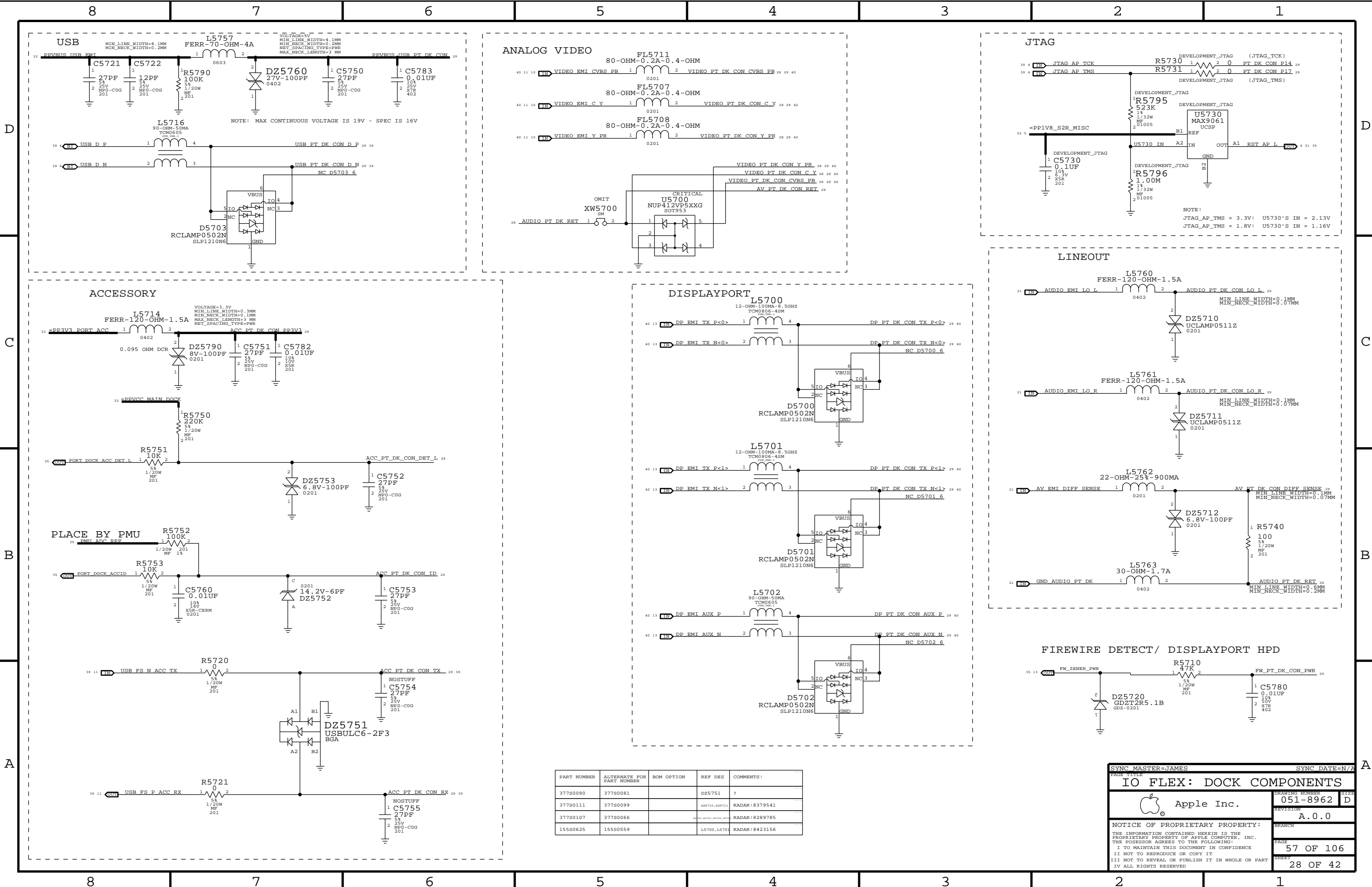
### SENSOR PANEL CONNECTOR CABLINE-CA CONNECTOR: 518S0787

CRITICAL  
J5600  
CABLINE-CA  
F-RT-SM

CONNECTED BY  
PG 54 ALIASES



PAGE TITLE		SYNC DATE=N/A	
CONNECTOR: SENSOR PANEL CONNECTOR			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE
	REVISION	A.0.0	D
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
377S0090	377S0081		DZ5751	?
377S0111	377S0099		085710,028711	RADAR:8379541
377S0107	377S0066		085710,028711	RADAR:8289785
155S0625	155S0559		L5700,L5708	RADAR:8423156

SYNC MASTER=JAMES SYNC DATE=N/A

**IO FLEX: DOCK COMPONENTS**

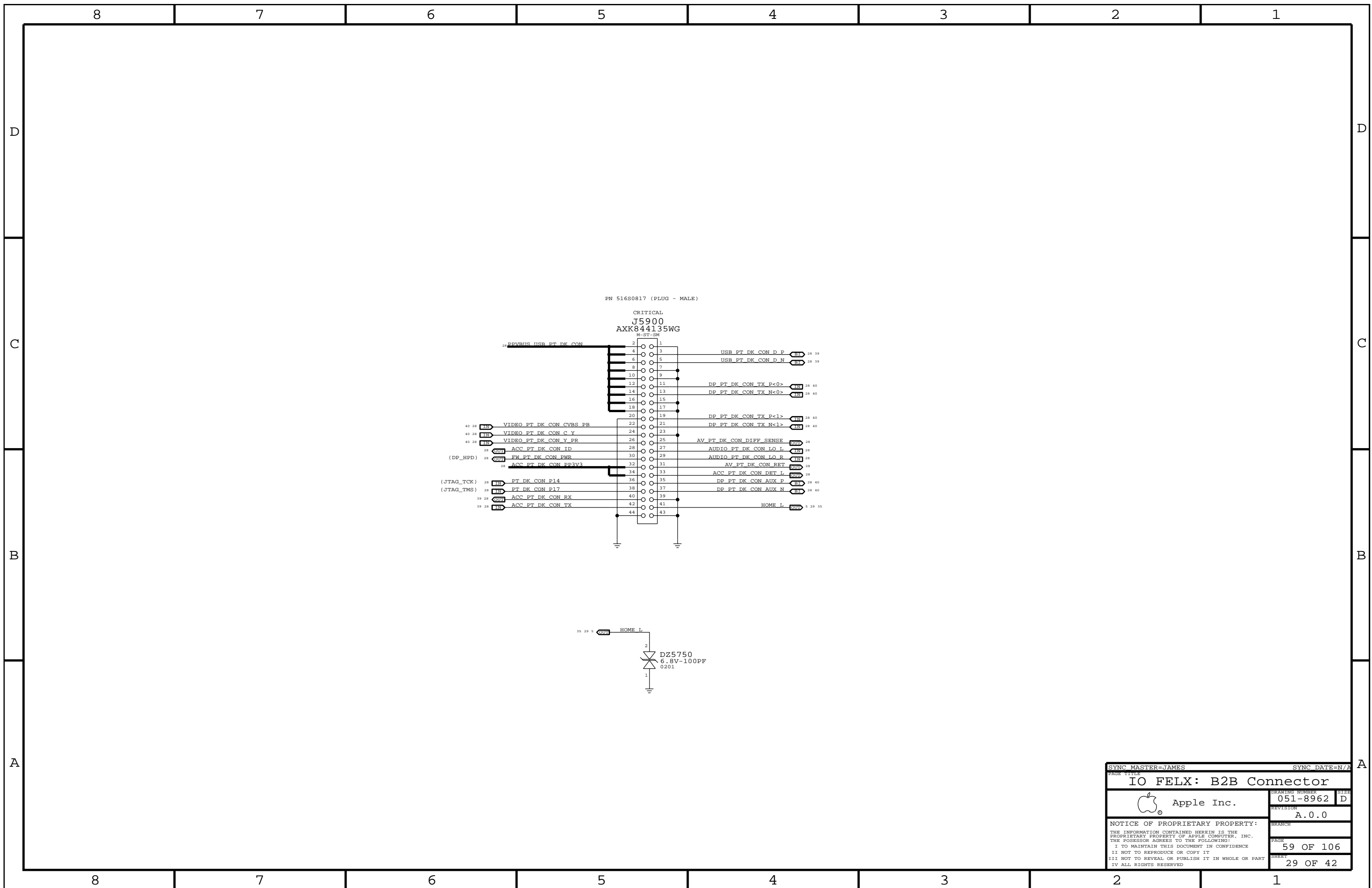
Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

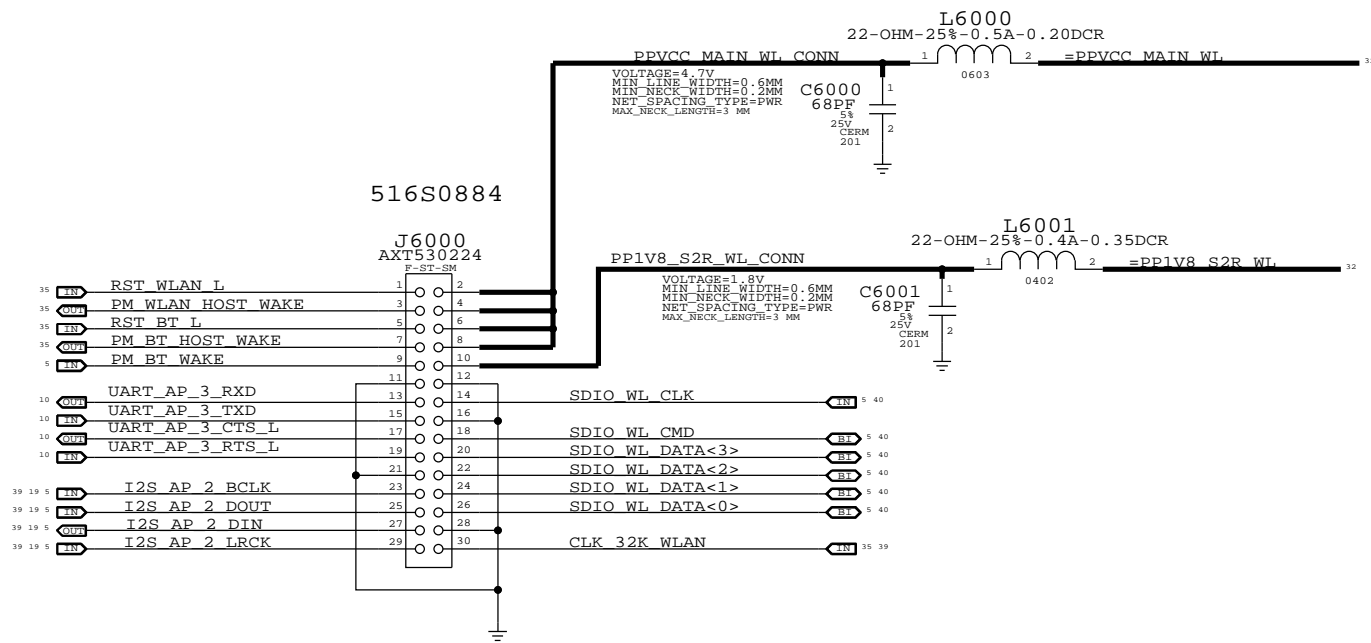
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SYNC MASTER=JAMES		SYNC DATE=N/A	
PAGE TITLE <b>IO FELX: B2B Connector</b>			
DRAWING NUMBER 051-8962		SIZE D	
REVISION A.0.0		BRANCH	
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# X23 WIFI/BT CONNECTOR



SYNC MASTER=MIKE		SYNC DATE=N/A	
CONNECTOR: X23 WIFI/BT			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8962	D
		REVISION	
		A.0.0	
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# X24 CELLULAR/GPS CONNECTOR



SYNC MASTER=MIKE		SYNC DATE=N/A	
CONNECTOR: X24 CELLULAR/GPS			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8962	D
		REVISION	
		A.0.0	
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# POWER CONN / ALIAS

## LDO RAILS

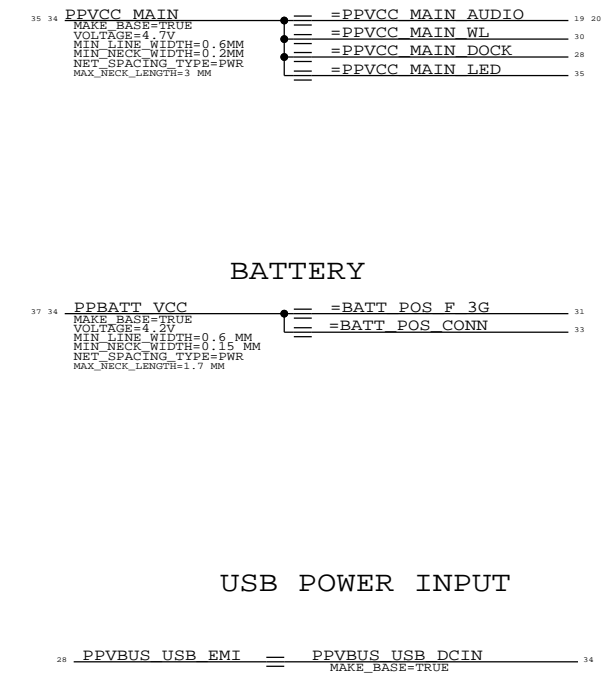
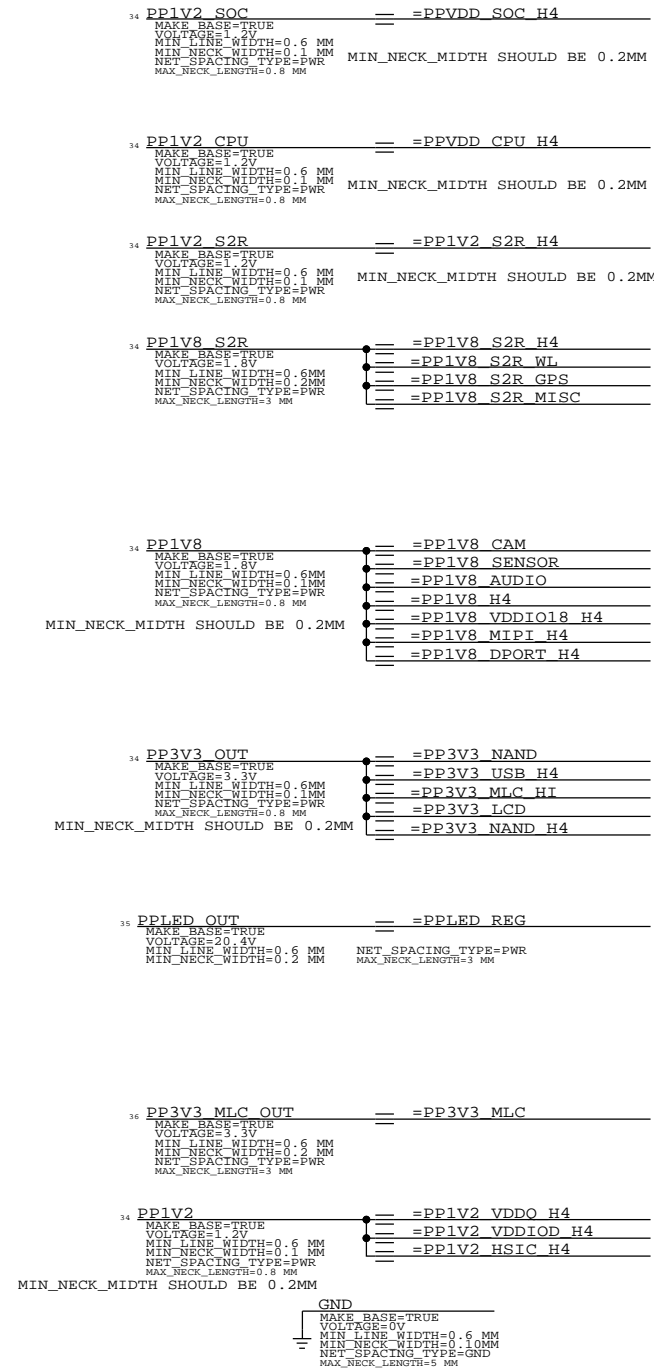
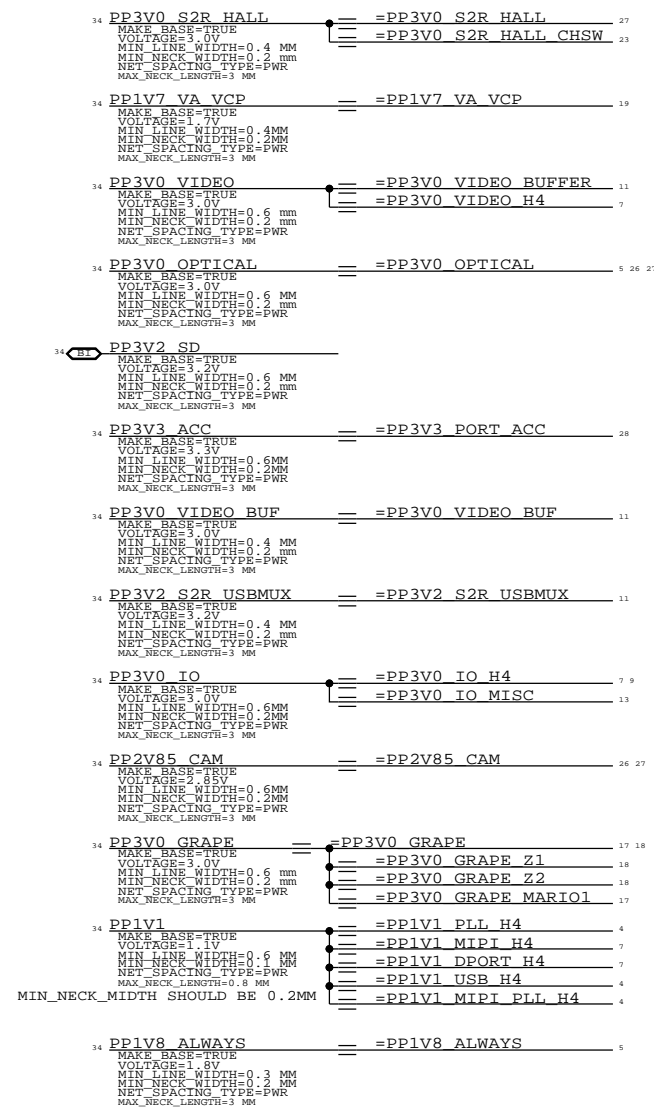
PROGRAMMABLE ON/OFF

## BUCK RAILS

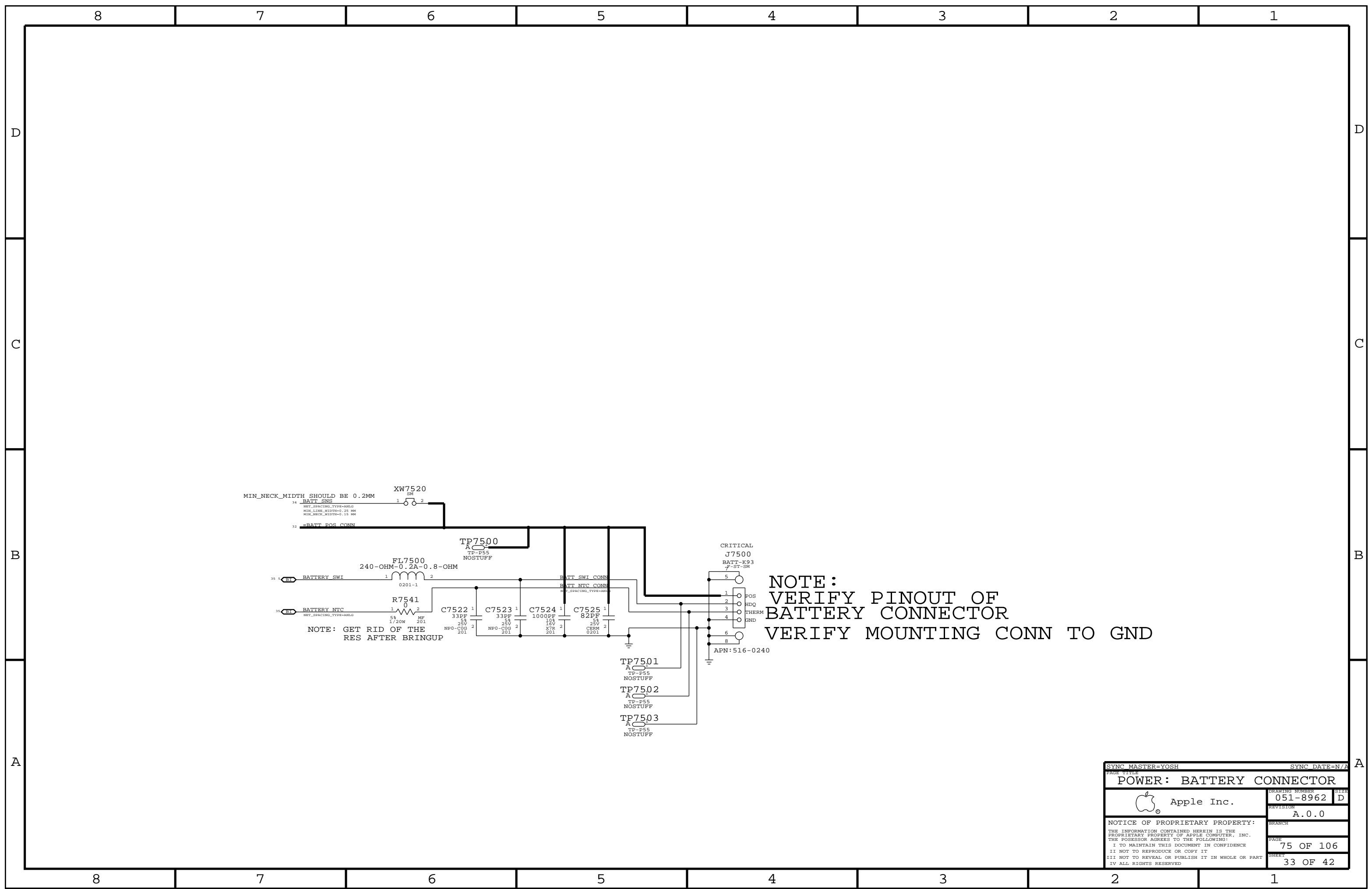
## CHARGER MAIN

## BATTERY

## USB POWER INPUT



SYNC MASTER=YOSH		SYNC DATE=N/A	
PAGE TITLE <b>POWER: ALIASES</b>			
Apple Inc.		DRAWING NUMBER 051-8962	SIZE D
		REVISION A.0.0	
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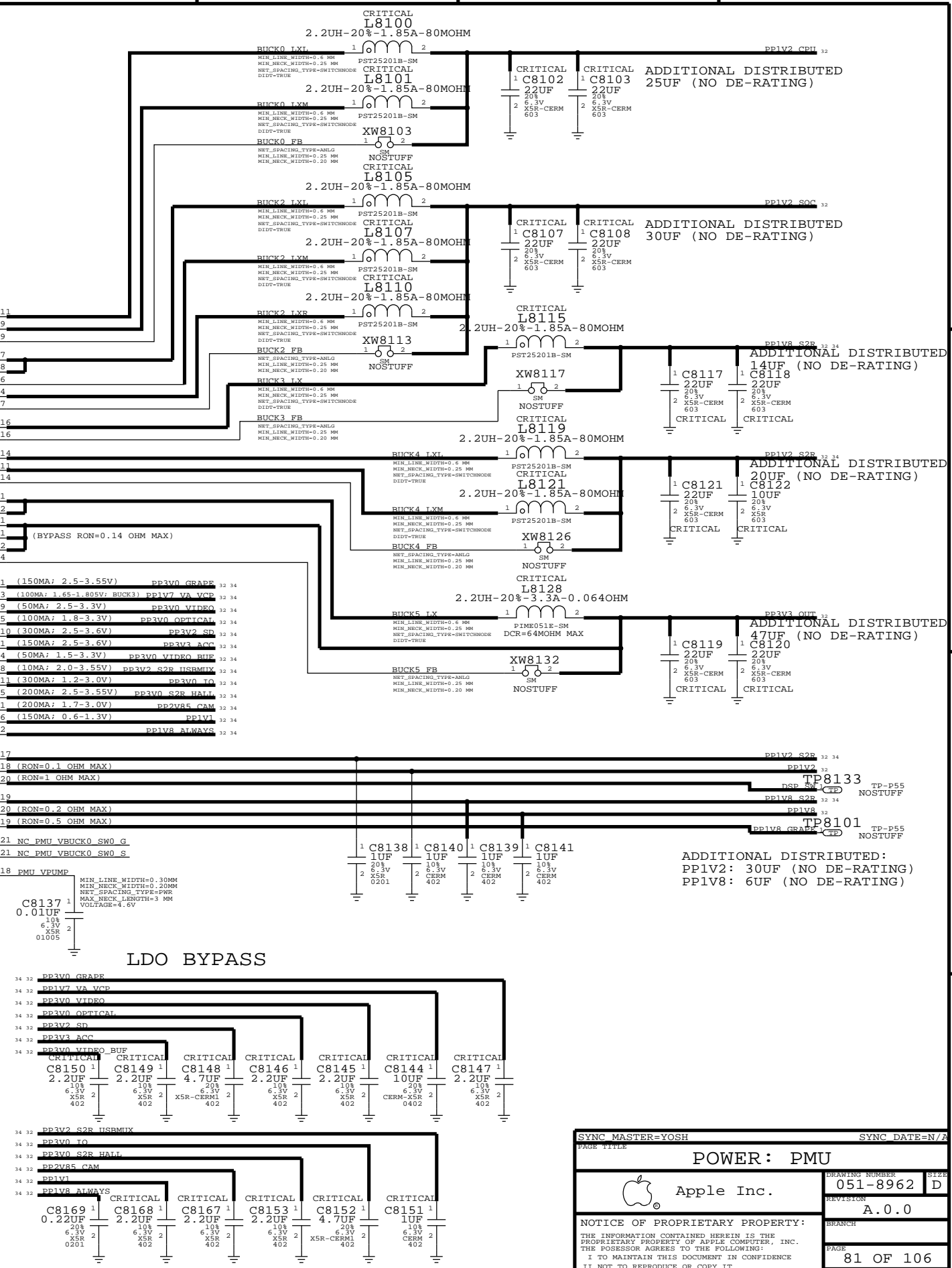
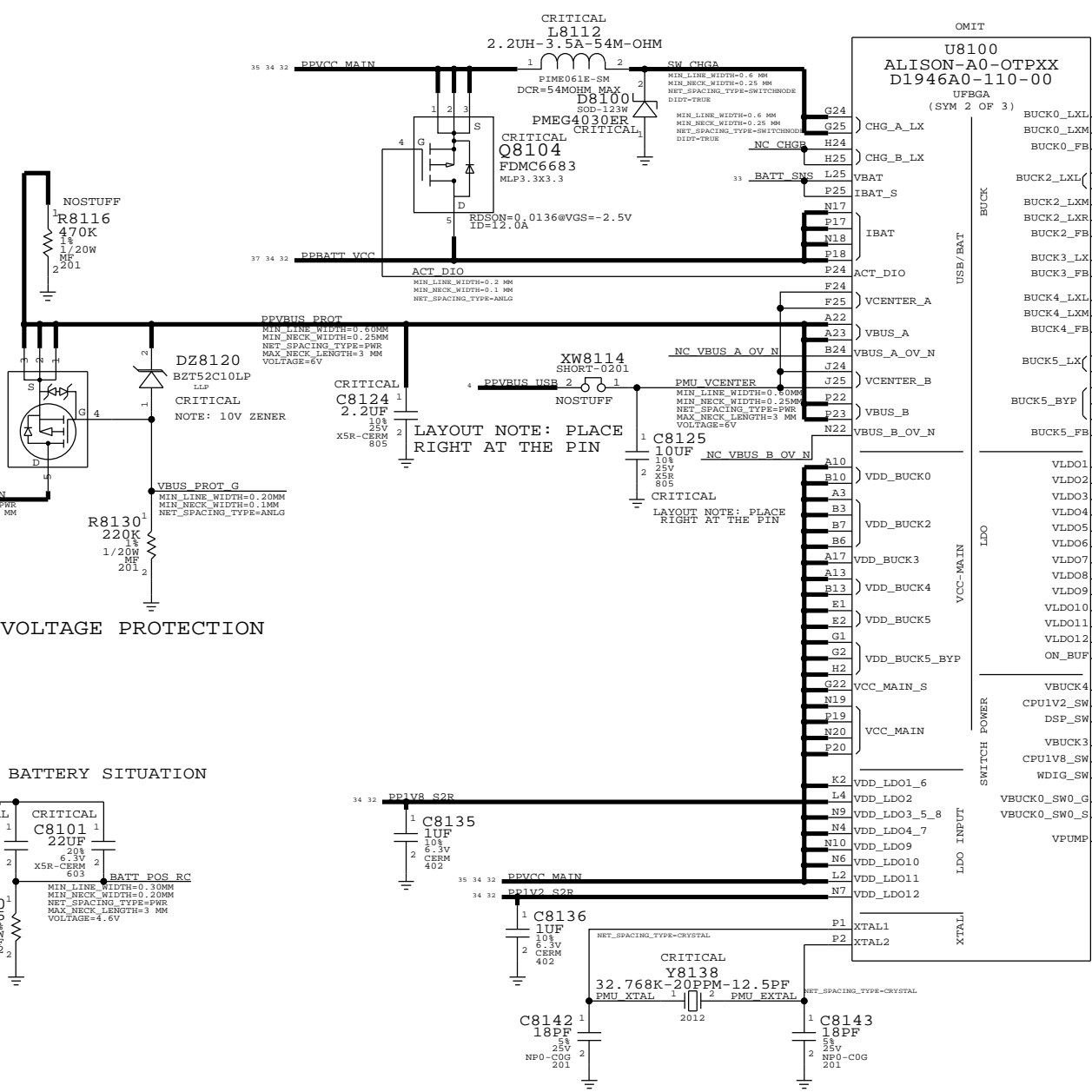
NOTE:  
 VERIFY PINOUT OF  
 BATTERY CONNECTOR  
 VERIFY MOUNTING CONN TO GND

SYNC MASTER=YOSH		SYNC DATE=N/A	
PAGE TITLE <b>POWER: BATTERY CONNECTOR</b>			
DRAWING NUMBER 051-8962		SIZE D	
REVISION A.0.0		BRANCH	
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PAGE 75 OF 106		SHEET 33 OF 42	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34380542	1	IC, PMU, ALISON, D1946A2, OTPXX, UFBGA292	U8100	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
19780392	19780299		Y8138	ALT FOUNDRY

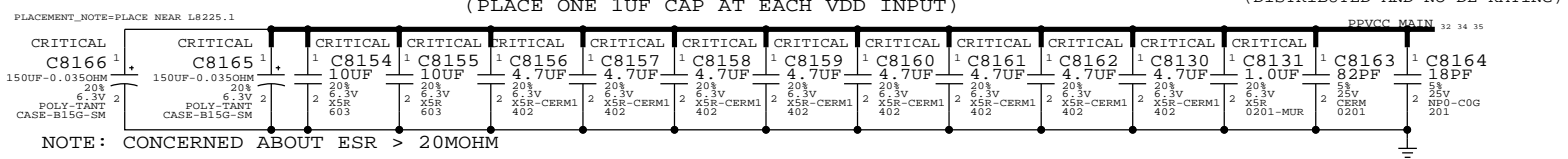
MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V



USB REVERSE VOLTAGE PROTECTION

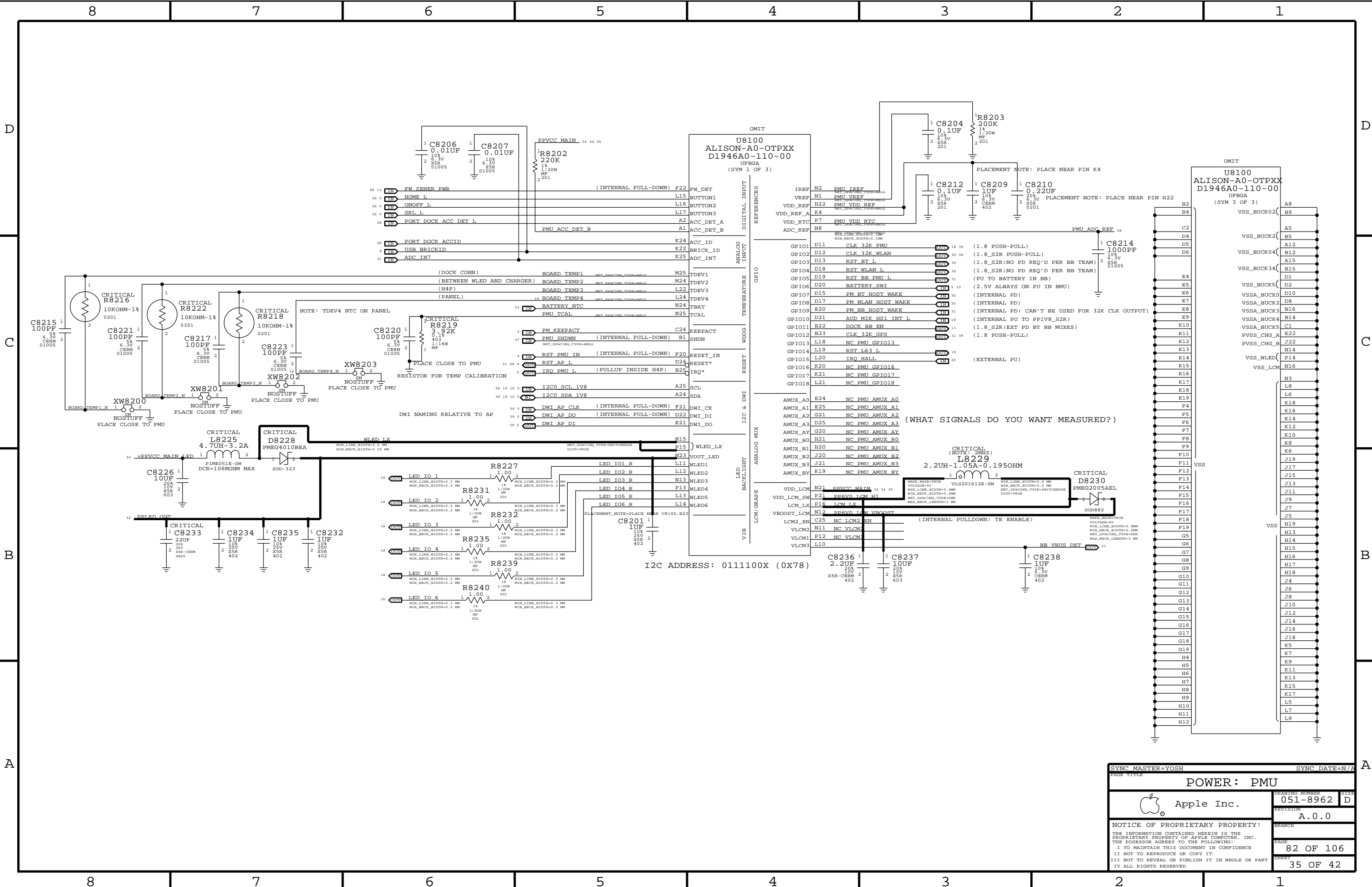
NOTE: FOR NO BATTERY SITUATION

VCC\_MAIN BYPASS  
TOTAL CAPS = ~400UF  
(DISTRIBUTED AND NO DE-RATING)

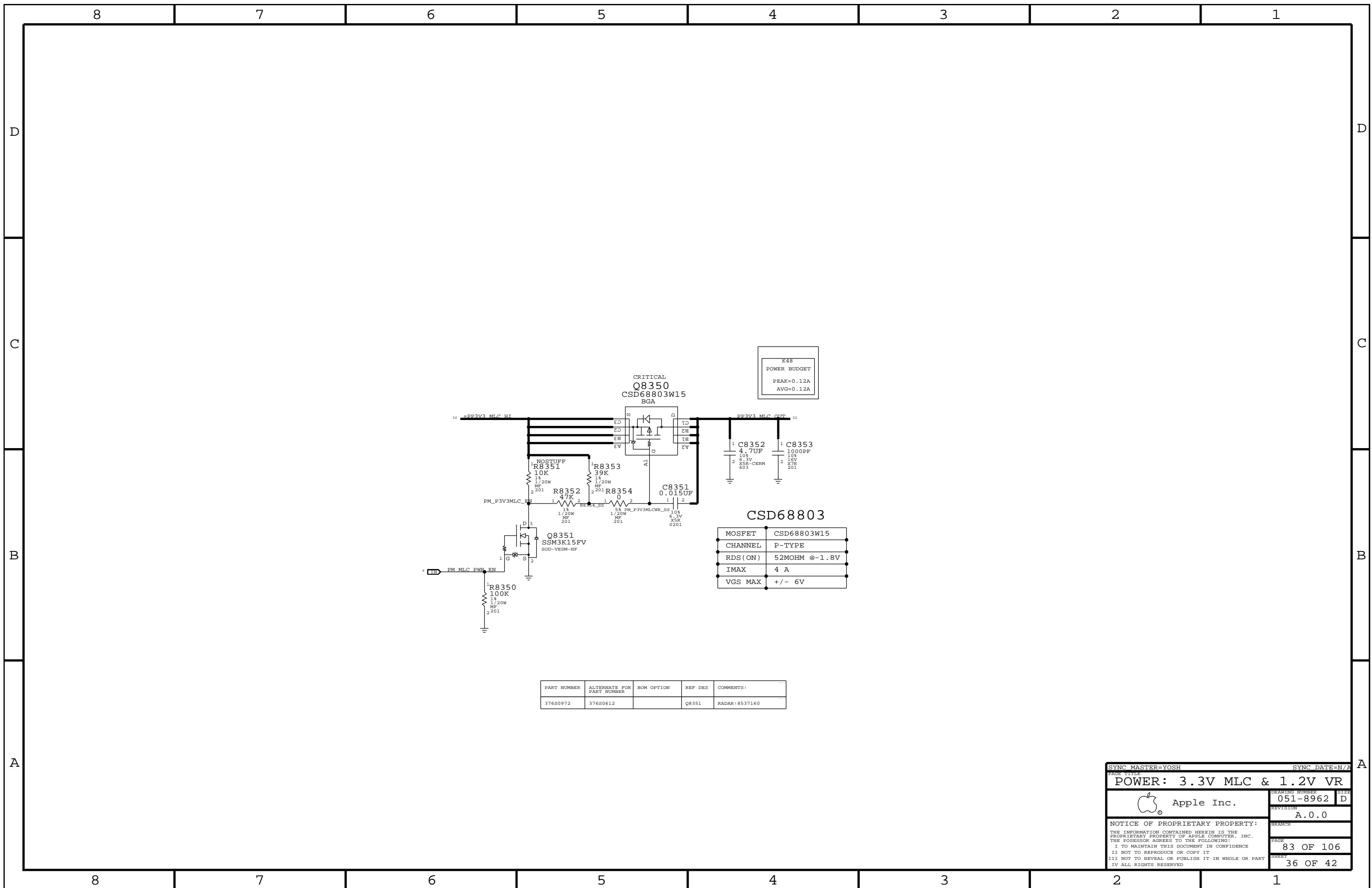


ADDITIONAL DISTRIBUTED:  
PPIV2: 30UF (NO DE-RATING)  
PPIV8: 6UF (NO DE-RATING)

SYNC MASTER=YOSH		SYNC DATE=N/A	
PAGE TITLE			
<b>POWER: PMU</b>		DRAWING NUMBER	SIZE
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SYNC MASTER=YOSH		SYNC DATE=N/A	
<b>POWER: PMU</b>			
DRAWING NUMBER		SIZE	
051-8962		D	
REVISION		BRANCH	
A.0.0			
PAGE		SHEET	
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K48  
POWER BUDGET  
PEAK=0.12A  
AVG=0.12A

CRITICAL  
Q8350  
CSD68803W15  
BGA

CSD68803

MOSFET	CSD68803W15
CHANNEL	P-TYPE
RDS (ON)	52MOHM @-1.8V
IMAX	4 A
VGS MAX	+/- 6V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
376S0972	376S0612		Q8351	RADAR: 8537160

SYNC MASTER=YOSH SYNC DATE=N/A

POWER: 3.3V MLC & 1.2V VR

Apple Inc.

051-8962 D

REVISION A.0.0

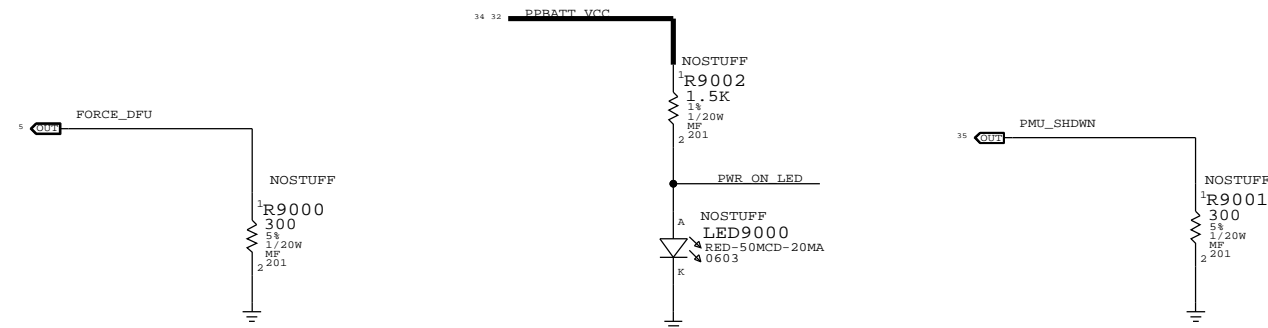
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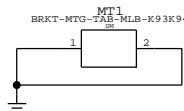
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# DEBUG RESET ACCESS

PLACE OUTSIDE OF CAN?



LEFT AND RIGHT MOUNTING TABS



SYNC MASTER=MIKE		SYNC DATE=N/A	
PAGE TITLE <b>DEBUG AND MISC</b>			
DRAWING NUMBER 051-8962		SIZE D	
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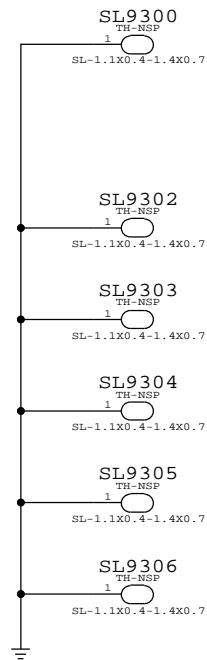
3


2

1

PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM  
PLATING SIZE: 1.4MM X 0.7MM



SYNC MASTER=MIKE		SYNC DATE=N/A	
PAGE TITLE <b>FCT/ICT TEST/BRACKETS</b>			
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		REVISION A.0.0	
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		PAGE	93 OF 106
		SHEET	38 OF 42

Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0	CLK_50S	CLK	CLK 32K PMU 18 35
HE1	CLK_50S	CLK	CLK 32K WLAN 30 35
HE2	CLK_50S	CLK	CLK 32K GPS 31 35
HE3	CLK_50S	CLK	CLK CAM FF 7 26
HE4	CLK_50S	CLK	CLK CAM FF FILT 7 26
HE5	CLK_50S	CLK	CLK CAM FF CONN 25 26
HE6	CLK_50S	CLK	CLK CAM RF 7 27
HE7	CLK_50S	CLK	CLK CAM RF FILT 25 27
HE8	CLK_50S	CLK	I2S AP 0 MCK 5
HE9	CLK_50S	CLK	I2S AP 0 MCK R 5 19
HE10	CLK_50S	CLK	CLK CAM FF R 7
HE11	CLK_50S	CLK	CLK CAM RF R 7

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0	NAND_50S	NAND	F0AD<7...0> 6 12
HE1	NAND_50S	NAND	F0CE0 L 6 12
HE2	NAND_50S	NAND	F0CE1 L 6 12
HE3	NAND_50S	NAND	F0CE2 L 6 12
HE4	NAND_50S	NAND	F0CE3 L 6 12
HE5	NAND_50S	NAND	F0CE4 L 6 12
HE6	NAND_50S	NAND	F0CE5 L 6 12
HE7	NAND_50S	NAND	F0CE6 L 6 12
HE8	NAND_50S	NAND	F0CE7 L 6 12
HE9	NAND_50S	NAND	F0CLE 6 12
HE10	NAND_50S	NAND	F0ALE 6 12
HE11	NAND_50S	NAND	FORE L 6 12
HE12	NAND_50S	NAND	F0WE L 6 12
HE13	NAND_50S	NAND	F0WP L 6 12
HE14	NAND_50S	NAND	F1AD<7...0> 6 12
HE15	NAND_50S	NAND	F1CE0 L 6 12
HE16	NAND_50S	NAND	F1CE1 L 6 12
HE17	NAND_50S	NAND	F1CE2 L 6 12
HE18	NAND_50S	NAND	F1CE3 L 6 12
HE19	NAND_50S	NAND	F1CE4 L 6 12
HE20	NAND_50S	NAND	F1CE5 L 6 12
HE21	NAND_50S	NAND	F1CE6 L 6 12
HE22	NAND_50S	NAND	F1CE7 L 6 12
HE23	NAND_50S	NAND	F1CLE 6 12
HE24	NAND_50S	NAND	F1ALE 6 12
HE25	NAND_50S	NAND	F1RE L 6 12
HE26	NAND_50S	NAND	F1WE L 6 12
HE27	NAND_50S	NAND	F1WP L 6 12
HE28	NAND_50S	NAND	F2AD<7...0>
HE29	NAND_50S	NAND	F2CE0 L
HE30	NAND_50S	NAND	F2CE1 L
HE31	NAND_50S	NAND	F2CE2 L
HE32	NAND_50S	NAND	F2CE3 L
HE33	NAND_50S	NAND	F2CLE
HE34	NAND_50S	NAND	F2ALE
HE35	NAND_50S	NAND	F2RE L
HE36	NAND_50S	NAND	F2WE L
HE37	NAND_50S	NAND	F2WP L
HE38	NAND_50S	NAND	F3AD<7...0>
HE39	NAND_50S	NAND	F3CE0 L
HE40	NAND_50S	NAND	F3CE1 L
HE41	NAND_50S	NAND	F3CE2 L
HE42	NAND_50S	NAND	F3CE3 L
HE43	NAND_50S	NAND	F3CLE
HE44	NAND_50S	NAND	F3ALE
HE45	NAND_50S	NAND	F3RE L
HE46	NAND_50S	NAND	F3WE L
HE47	NAND_50S	NAND	F3WP L

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0		JTAG	JTAG AP TCK 4 28
HE1		JTAG	JTAG AP TMS 4 28
HE2		JTAG	JTAG AP TDI 4 10
HE3		JTAG	JTAG AP TDO 4 10
HE4		JTAG	JTAG AP TRST L 4 10

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0	I2C_50S	I2C	I2C1 SDA 1V8 5 25
HE1	I2C_50S	I2C	I2C1 SCL 1V8 5 25
HE2	I2C_50S	I2C	I2C0 SDA 1V8 5 10 19 35
HE3	I2C_50S	I2C	I2C0 SCL 1V8 5 10 19 35
HE4	I2C_50S	I2C	I2C2 SDA 3V0 5 25 26
HE5	I2C_50S	I2C	I2C2 SCL 3V0 5 25 26
HE6	I2C_50S	I2C	ISP AP 0 SCL 7 25
HE7	I2C_50S	I2C	ISP AP 0 SDA 7 25
HE8	I2C_50S	I2C	ISP AP 1 SCL 7 26
HE9	I2C_50S	I2C	ISP AP 1 SDA 7 26
HE10	I2C_50S	I2C	I2C2 SCL 3V0 ALS 25 26
HE11	I2C_50S	I2C	I2C2 SDA 3V0 ALS 25 26
HE12	I2C_50S	I2C	ISP CAM 1 SCL 25 26
HE13	I2C_50S	I2C	ISP CAM 1 SDA 25 26

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0		CRYSTAL	XTAL 24M I 4
HE1		CRYSTAL	XTAL 24M O 4
HE2		CRYSTAL	24M_O 4

VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0		VREF	PPVREF DDR0 CA 8
HE1		VREF	PPVREF DDR0 DO 8
HE2		VREF	PPVREF DDR1 CA 8
HE3		VREF	PPVREF DDR1 DO 8

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFP

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0	USB_90D	USB	USB D P 4 28
HE1	USB_90D	USB	USB D N 4 28
HE2	USB_90D	USB	USB PT DK CON D P 28 29
HE3	USB_90D	USB	USB PT DK CON D N 28 29
HE4	USB_90D	USB	USB BB D P 11 31
HE5	USB_90D	USB	USB BB D N 11 31
HE6	USB_90D	USB	USB FS D P 4 11
HE7	USB_90D	USB	USB FS D N 4 11
HE8	USB_90D	USB	USB FS N ACC TX 11 28
HE9	USB_90D	USB	USB FS P ACC RX 11 28
HE10	USB_90D	USB	ACC PT DK CON TX 28 29
HE11	USB_90D	USB	ACC PT DK CON RX 28 29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_90S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0	I2S_50S	I2S	I2S AP 0 BCLK 5 19
HE1	I2S_50S	I2S	I2S AP 0 LRCK 5 19
HE2	I2S_50S	I2S	I2S AP 0 DIN 5 19
HE3	I2S_50S	I2S	I2S AP 0 DOUT 5 19
HE4	I2S_50S	I2S	I2S AP 0 SDOUT 19
HE5	I2S_50S	I2S	I2S AP 2 BCLK 5 19 30
HE6	I2S_50S	I2S	I2S AP 2 LRCK 5 19 30
HE7	I2S_50S	I2S	I2S AP 2 DIN 5 19 30
HE8	I2S_50S	I2S	I2S AP 2 DOUT 5 19 30
HE9	I2S_50S	I2S	I2S AP 2 SDOUT 19
HE10	I2S_50S	I2S	I2S AP 3 BCLK 5 19
HE11	I2S_50S	I2S	I2S AP 3 LRCK 5 19
HE12	I2S_50S	I2S	I2S AP 3 DIN 5 19
HE13	I2S_50S	I2S	I2S AP 3 DOUT 5 19
HE14	I2S_50S	I2S	I2S AP 3 SDOUT 19

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0		DWI	DWI AP CLK 5 35
HE1		DWI	DWI AP DI 5 35
HE2		DWI	DWI AP DO 5 35

SYNC MASTER=MIKE		SYNC DATE=N/A	
<b>CONSTRAINTS: ASSIGNMENTS</b>			
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		REVISION	A.0.0
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		SHEET	39 OF 42

ANALOG VIDEO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VID_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ANALOG_VIDEO	*	*	5:1_SPACING
ANALOG_VIDEO	ANALOG_VIDEO	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
E230	VID_50S	ANALOG_VIDEO	DAC AP OUT1	7 11
E230	VID_50S	ANALOG_VIDEO	DAC AP OUT2	7 11
E230	VID_50S	ANALOG_VIDEO	DAC AP OUT3	7 11
E230	VID_50S	ANALOG_VIDEO	BUF C Y	11
E230	VID_50S	ANALOG_VIDEO	BUF CVBS PB	11
E230	VID_50S	ANALOG_VIDEO	BUF Y PR	11
E230	VID_50S	ANALOG_VIDEO	VIDEO EMI CVBS_PB	10 11 28
E230	VID_50S	ANALOG_VIDEO	VIDEO EMI C Y	10 11 28
E230	VID_50S	ANALOG_VIDEO	VIDEO EMI Y PR	10 11 28
E230	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON CVBS_PB	28 29
E230	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON C Y	28 29
E230	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON Y PR	28 29

LVDS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
E240	LVDS_100D	LVDS	LVDS DATA P<2..0>	14 16
E240	LVDS_100D	LVDS	LVDS DATA N<2..0>	14 16
E240	LVDS_100D	LVDS	LVDS DATA CONN_P<2..0>	16
E240	LVDS_100D	LVDS	LVDS DATA CONN_N<2..0>	16
E240	LVDS_100D	LVDS	LVDS CLK P	14 16
E240	LVDS_100D	LVDS	LVDS CLK N	14 16
E240	LVDS_100D	LVDS	LVDS CLK CONN_P	16
E240	LVDS_100D	LVDS	LVDS CLK CONN_N	16

DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
E244	DP_100D	DP	DP AP TX P<0>	7 10 13
E244	DP_100D	DP	DP AP TX N<0>	7 10 13
E244	DP_100D	DP	DP AP TX P<1>	7 10 13
E244	DP_100D	DP	DP AP TX N<1>	7 10 13
E244	DP_100D	DP	DP AP AUX P	7 13
E244	DP_100D	DP	DP AP AUX N	7 13
E244	DP_100D	DP	DP EMI TX P<0>	13 28
E244	DP_100D	DP	DP EMI TX N<0>	13 28
E244	DP_100D	DP	DP EMI TX P<1>	13 28
E244	DP_100D	DP	DP EMI TX N<1>	13 28
E244	DP_100D	DP	DP EMI AUX P	13 28
E244	DP_100D	DP	DP EMI AUX N	13 28
E244	DP_100D	DP	DP PT DK CON_TX_P<0>	28 29
E244	DP_100D	DP	DP PT DK CON_TX_N<0>	28 29
E244	DP_100D	DP	DP PT DK CON_TX_P<1>	28 29
E244	DP_100D	DP	DP PT DK CON_TX_N<1>	28 29
E244	DP_100D	DP	DP PT DK CON_AUX_P	28 29
E244	DP_100D	DP	DP PT DK CON_AUX_N	28 29

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
E248	MIPI_100D	MIPI	MIPI AP DATA P<0>	7 14
E248	MIPI_100D	MIPI	MIPI AP DATA N<0>	7 14
E248	MIPI_100D	MIPI	MIPI AP DATA P<1>	7 14
E248	MIPI_100D	MIPI	MIPI AP DATA N<1>	7 14
E248	MIPI_100D	MIPI	MIPI AP DATA P<2>	7 14
E248	MIPI_100D	MIPI	MIPI AP DATA N<2>	7 14
E248	MIPI_100D	MIPI	MIPI AP DATA P<3>	7 14
E248	MIPI_100D	MIPI	MIPI AP DATA N<3>	7 14
E248	MIPI_100D	MIPI	MIPI AP CLK P	7 14
E248	MIPI_100D	MIPI	MIPI AP CLK N	7 14
E248	MIPI_100D	MIPI	MIPI OC AP DATA P<0>	7 27
E248	MIPI_100D	MIPI	MIPI OC AP DATA N<0>	7 27
E248	MIPI_100D	MIPI	MIPI OC AP CLK P	7 27
E248	MIPI_100D	MIPI	MIPI OC AP CLK N	7 27
E248	MIPI_100D	MIPI	MIPI OC CAM DATA P<0>	25 27
E248	MIPI_100D	MIPI	MIPI OC CAM DATA N<0>	25 27
E248	MIPI_100D	MIPI	MIPI OC CAM CLK P	25 27
E248	MIPI_100D	MIPI	MIPI OC CAM CLK N	25 27
E248	MIPI_100D	MIPI	MIPI IC AP DATA P<0>	7 26
E248	MIPI_100D	MIPI	MIPI IC AP DATA N<0>	7 26
E248	MIPI_100D	MIPI	MIPI IC AP CLK P	7 26
E248	MIPI_100D	MIPI	MIPI IC AP CLK N	7 26
E248	MIPI_100D	MIPI	MIPI IC CAM DATA P<0>	25 26
E248	MIPI_100D	MIPI	MIPI IC CAM DATA N<0>	25 26
E248	MIPI_100D	MIPI	MIPI IC CAM CLK P	25 26
E248	MIPI_100D	MIPI	MIPI IC CAM CLK N	25 26

AUDIO/SPEAKER

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIO	*	1:1_DIFFPAIR
SPEAKER	*	SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
E250	AUDIO	AUDIO	LEFT CH OUT P	19 20
E250	AUDIO	AUDIO	LEFT CH OUT REF	19 20
E250	AUDIO	AUDIO	LEFT CH P	20
E250	AUDIO	AUDIO	SSM2375 L IN P	20
E250	AUDIO	AUDIO	SSM2375 L IN N	20
E250	AUDIO	AUDIO	RIGHT CH OUT P	19 20
E250	AUDIO	AUDIO	RIGHT CH OUT REF	19 20
E250	AUDIO	AUDIO	RIGHT CH P	20
E250	AUDIO	AUDIO	SSM2375 R IN P	20
E250	AUDIO	AUDIO	SSM2375 R IN N	20
E250	AUDIO	AUDIO	EXT MIC P	19 23
E250	AUDIO	AUDIO	EXT MIC REF	19 23

SDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SDIO_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SDIO	*	*	2:1_SPACING
SDIO_CLK	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
E252	SDIO_50S	SDIO_CLK	SDIO WL CLK	5 30
E252	SDIO_50S	SDIO_CLK	SDIO WL CLK R	5 30
E252	SDIO_50S	SDIO	SDIO WL CMD	5 30
E252	SDIO_50S	SDIO	SDIO WL DATA<3..0>	5 30

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
E254	SPI_50S	SPT	SPI GRAPE MISO	5 17
E254	SPI_50S	SPT	SPI GRAPE MOSI	5 17
E254	SPI_50S	SPT	SPI GRAPE SCLK	5 17
E254	SPI_50S	SPT	SPI GRAPE CS L	5 17
E254	SPI_50S	SPT	SPI IPC MISO	5 31
E254	SPI_50S	SPT	SPI IPC MOSI	5 31
E254	SPI_50S	SPT	SPI IPC SCLK	5 31
E254	SPI_50S	SPT	SPI IPC MRDY	5 31

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# MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, BOTTOM	NO_TYPE, BGA, BGA06-06	MM	15.2

## PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

### SINGLE-ENDED PHYSICAL RULES 45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL2, ISL3, ISL8, ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4, ISL5, ISL6, ISL7	Y	0.060 MM	0.060 MM	3.0 MM		
45_OHM_SE	*	N	0.060 MM	0.060 MM	3.0 MM		

### 50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.085 MM	0.085 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

### 50 OHMS - CLEAR ON LAYER 2 AND 5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP	Y	0.240 MM	0.240 MM	3.0 MM		
50_OHM_SE	ISL4	Y	0.060 MM	0.060 MM	3.0 MM		

### 50 OHMS - CLEAR ON TOP AND BOTTOM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL2, ISL9	Y	0.090 MM	0.090 MM	3.0 MM		

### DIFFERENTIAL PAIR PHYSICAL RULES

#### 100 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP, BOTTOM	Y	0.076 MM	0.076 MM		0.210 MM	0.210 MM
100_OHM_DIFF	N	Y	0.057 MM	0.057 MM	=STANDARD	0.300 MM	0.300 MM

#### 90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL3, ISL8, ISL9	Y	0.054 MM	0.054 MM	=STANDARD	0.200 MM	0.100 MM
90_OHM_DIFF	ISL4, ISL5, ISL6, ISL7	Y	0.060 MM	0.060 MM	=STANDARD	0.200 MM	0.100 MM

### AUDIO PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	0.08 MM

### BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

## SPACING CONSTRAINTS

### DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

### REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.060 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.090 MM	?
2:1_SPACING	*	0.120 MM	?
2.5:1_SPACING	*	0.150 MM	?
3:1_SPACING	*	0.180 MM	?
4:1_SPACING	*	0.240 MM	?
5:1_SPACING	*	0.300 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

\*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS

### POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP, BOTTOM	0.2 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING

### NOTES:

- 0.075 MM ~ 3 MIL
- 0.089 MM ~ 3.5 MIL
- 0.102 MM ~ 4 MIL
- 0.114 MM ~ 4.5 MIL
- 0.125 MM ~ 5 MIL
- 0.140 MM ~ 5.5 MIL
- 0.15 MM ~ 6 MIL
- 0.18 MM ~ 7 MIL
- 0.2 MM ~ 8 MIL
- 0.25 MM ~ 10 MIL
- 0.3 MM ~ 12 MIL
- 0.33 MM ~ 13 MIL
- 0.4 MM ~ 16 MIL
- 1.0 MM = 39.37 MIL

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