1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
8	0003549590	ENGINEERING RELEASED	2014-12-19

X304 MLB SCHEMATIC - DVT

Fri Dec 19 12:14:48 2014

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-1573	1	SCHEM,MLB,X304	SCH	CRITICAL	
820-4924	1	PCBF,MLB,X304	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,X304

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D
REVISION: 8.0.0
BRANCH: dvt1
PAGE: 1 OF 120
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BOM Groups

BOM GROUP	BOM OPTIONS
X304_COMMON	ALTERNATE,COMMON,X304_COMMON1,X304_COMMON2,X304_COMMON3,X304_COMMON4,X304_PROGPARTS
X304_COMMON1	TBTHV:P15V,SKIP_5V3V3:AUDIBLE,PANEL:NEW,SSD_CLKREQ:BI
X304_COMMON2	EDP,EDP_LS_CAP,CAMERA_3V3:S0,CAM_WAKE:NO,CAM_XTAL:NO,VCORE_FETS
X304_COMMON3	XDP,SAMCONN,BKLT:PROD,CPUTHRM:ALRT,LOADRC:NO,OTHERRC:NO,DDRRC:NO,TBTRC:NO,BMONRC:NO,TPADRC:NO
X304_PROGPARTS	SMC_PROG:PROTO0,BOOTROM_PROG,TBTROM_PROG
X304_DEVEL:ENG	ALTERNATE,ENGISNS,XDP_CONN,DBGLED
X304_DEVEL:DVT	ALTERNATE,ENGISNS,XDP_CONN,S0PGOOD_ISL
X304_DEVEL:PVT	ALTERNATE
ENGISNS	LOADISNS,OTHERISNS,DDRISNS,TBTISNS,BMONISNS,TPADISNS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00107	1	CPU,BW,SR26K,PRQ,F0-B2,2.7,28W,1.05,1168	U0500	CRITICAL	CPU_BDW23:2.7G
337S00108	1	CPU,BW,SR26H,PRQ,F0-B2,2.9,28W,1.1,1168	U0500	CRITICAL	CPU_BDW23:2.9G
337S00109	1	CPU,BW,SR26E,PRQ,F0-B2,3.1,28W,1.1,1168	U0500	CRITICAL	CPU_BDW23:3.1G

DVT

998-7866	1	INTERPOSER,BGA1168P, SINGLE SIDE	U0500	CRITICAL	CPU_SOCKET
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
338S1264	1	IC,BCM15700A2KFEB4G,S2 CMRA,8X8,208FCBGA	U3900	CRITICAL	
376S1194	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
376S00036	2	MOSFET,N-CH,30V,52A,5.9MO,3.3X3.3 DFN8	Q7310,Q7320	CRITICAL	VCORE_FET:ONSMI
376S00037	2	MOSFET,N-CH,30V,64A,3.5MO,3.3X3.3 DFN8	Q7311,Q7321	CRITICAL	VCORE_FET:ONSMI

Programmables (All Builds)

TBT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00192	1	T29,EPROM,FALCON RIDGE (V27.1) EVT2,X304	U2890	CRITICAL	TBTROM_PROG

SMC

341S3982	1	IC,SMC-B1,EXT(V2.21A5) PROTO 0,X304	U5000	CRITICAL	SMC_PROG:PROTO0

EFI ROM

341S00235	1	EFI ROM,MLB (V0145) DVT,X304	U6100	CRITICAL	BOOTROM_PROG

Variable BOM Groups

BOM GROUP	BOM OPTIONS
X304_COMMON4	SMCBOARDID:16

Development/Base BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-1314	1	X304 MLB COMMON BOM	BASE	CRITICAL	BASE_BOM
985-1319	1	X304 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-1318	1	VCORE FET,VSHY,X304	VCOREFETS	CRITICAL	VCORE_FETS

Main DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_16G_HYNIX_1600	16G_HYNIX_1600,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_16G_HYNIX_1866	16G_HYNIX_1866,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM_8G_HYNIX_1600	8G_HYNIX_1600,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_8G_HYNIX_1866	8G_HYNIX_1866,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_4G_HYNIX_1600	4G_HYNIX_1600,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_4G_HYNIX_1866	4G_HYNIX_1866,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_16G_ELPIDA_1600	16G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_16G_ELPIDA_1866	16G_ELPIDA_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM_8G_ELPIDA_1600	8G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_8G_ELPIDA_1866	8G_ELPIDA_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_4G_ELPIDA_1600	4G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_4G_ELPIDA_1866	4G_ELPIDA_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_8G_SAMSUNG_1600	8G_SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_8G_SAMSUNG_1866	8G_SAMSUNG_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM_4G_SAMSUNG_1600	4G_SAMSUNG_1600,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_SAMSUNG_1866	4G_SAMSUNG_1866,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00068	08	CPU
337S00069	08	CPU
337S00070	08	CPU
337S00071	08	CPU
353S00200	07	TPAD ELEC FUSE
333S0786	07	SYS MEMORY HYNIX
333S0784	07	SYS MEMORY HYNIX
333S0792	07	SYS MEMORY MICRON
333S0790	07	SYS MEMORY MICRON
333S00004	07	SYS MEMORY SAMSUNG
311S0597	02	KEYBOARD I2C EXPANDER
359S0197	01	GREEN CLOCK
338S1247	01	FALCON RIDGE
353S3931	01	TBT PWR MUX
353S3812	01	TBT MUX
353S3814	01	TBT MUX
353S00095	01	DDC CROSSBAR
353S3328	01	DDC CROSSBAR
343S0511	01	PCIE DELAY IC
338S1264	01	S2
333S0700	01	S2 MEMORY
333S0704	01	S2 MEMORY
353S3054	01	USB POWER/SAFETY
343S0649	01	SMC RESET CHIP
353S4080	01	AUDIO
353S2888	01	AUDIO AMPS
353S2958	01	AUDIO AMPS
353S2929	01	BAT CHARGER
353S00036	01	VR12.6 CONTROLLER
353S4160	01	BEN
343S0666	01	SAK, HDMI SELECT
341S3982	01	SMC
341S00192	01	T29 ROM
341S00235	01	EFI ROM

Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0783	4	IC,SDRAM,25nm 32Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	16G_HYNIX_1600
333S0784	4	IC,SDRAM,25nm 32Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	16G_HYNIX_1866
333S0785	4	IC,SDRAM,29nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	8G_HYNIX_1600
333S0786	4	IC,SDRAM,29nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	8G_HYNIX_1866
333S0787	4	IC,SDRAM,29nm 8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	4G_HYNIX_1600
333S0788	4	IC,SDRAM,29nm 8Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	4G_HYNIX_1866
333S0789	4	IC,SDRAM,25nm 32Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	16G_ELPIDA_1600
333S0790	4	IC,SDRAM,25nm 32Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	16G_ELPIDA_1866
333S0791	4	IC,SDRAM,25nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	8G_ELPIDA_1600
333S0792	4	IC,SDRAM,25nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	8G_ELPIDA_1866
333S0793	4	IC,SDRAM,25nm 8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	4G_ELPIDA_1600
333S0794	4	IC,SDRAM,25nm 8Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	4G_ELPIDA_1866
333S00003	4	IC,SDRAM,23nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	8G_SAMSUNG_1600
333S00004	4	IC,SDRAM,23nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	8G_SAMSUNG_1866
333S00001	4	IC,SDRAM,23nm 8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	4G_SAMSUNG_1600
333S00002	4	IC,SDRAM,23nm 8Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	4G_SAMSUNG_1866

S2 DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0700	1	IC,SDRAM,4GBIT.DDR3L-1600,HUMA,96B BGA	U4000		

SYNC_MASTER=SHART_J44 SYNC_DATE=11/27/2013

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-1314	COMMON,MLB,X304	X304_COMMON
985-1319	DEV,MLB,X304	X304_DEVEL:ENG
639-00772	MLB,BDW2+3,2.7GHz,8GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_8G_HYNIX_1866
639-00773	MLB,BDW2+3,2.7GHz,16GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_16G_HYNIX_1866
639-00774	MLB,BDW2+3,2.7GHz,8GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_8G_ELPIDA_1866
639-00775	MLB,BDW2+3,2.7GHz,16GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_16G_ELPIDA_1866
639-00776	MLB,BDW2+3,2.7GHz,8GB-SM-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_8G_SAMSUNG_1866
639-00777	MLB,BDW2+3,2.9GHz,8GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_8G_HYNIX_1866
639-00778	MLB,BDW2+3,2.9GHz,16GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_16G_HYNIX_1866
639-00779	MLB,BDW2+3,2.9GHz,8GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_8G_ELPIDA_1866
639-00780	MLB,BDW2+3,2.9GHz,16GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_16G_ELPIDA_1866
639-00781	MLB,BDW2+3,2.9GHz,8GB-SM-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_8G_SAMSUNG_1866
639-00782	MLB,BDW2+3,3.1GHz,8GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_8G_HYNIX_1866
639-00783	MLB,BDW2+3,3.1GHz,16GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_16G_HYNIX_1866
639-00784	MLB,BDW2+3,3.1GHz,8GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_8G_ELPIDA_1866
639-00785	MLB,BDW2+3,3.1GHz,16GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_16G_ELPIDA_1866
639-00786	MLB,BDW2+3,3.1GHz,8GB-SM-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_8G_SAMSUNG_1866

BOM NUMBER	BOM NAME	BOM OPTIONS
639-00035	PCBA,MLB,NO CPU,X304	BASE_BOM,DEVEL_BOM,RAM_8G_HYNIX_1866
639-00036	PCBA,MLB,CPU SOCKET,X304	BASE_BOM,DEVEL_BOM,CPU_SOCKET,RAM_8G_HYNIX_1866
685-1318	VCORE FET,VSHY,X304	VCORE_FET:VSHY
685-00022	VCORE FET,ONSMI,X304	VCORE_FET:ONSMI

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
685-00022	685-1318		ALL		Onsemi alt to Vishay for CPU Core Mosfets
333S0704	333S0700		ALL		Elpida alt to Hynix for S2 Camera DDR3 Memory

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
376S1053	376S0604		ALL		Diodes alt to Fairchild
128S0311	128S0329		ALL		NEC alt to Sanyo
138S0739	138S0706		ALL		Samsung alt to Murata
197S0481	197S0480		ALL		Epson alt to NDK
152S0461	152S1645		ALL		Cyntec alt to Vishay
376S1080	376S0820		ALL		Diodes alt to On Semi
138S0725	138S0724		ALL		Samsung alt to Murata
376S00074	376S0855		ALL		Toshiba alt for Diodes Dual
376S1129	376S0855		ALL		NXP Alt for Diodes Dual
376S1089	376S1128		ALL		NXP Alt for Diodes Single
353S3452	353S1286		ALL		Maxim alt to Microchip
128S0364	128S0264		ALL		Sanyo 2nd Factory alt
107S0254	107S0241		ALL		Cyntec alt to TFT
138S0843	138S0674		ALL		Samsung alt to Murata (BKLT)
138S0846	138S0811		ALL		Samsung alt to Murata (BKLT)
197S0542	197S0544		ALL		NDK alt to TXC
197S0545	197S0544		ALL		Epson alt to TXC
107S0248	107S0250		ALL		TFT alt to Cyntec
127S0164	127S0162		ALL		Rohm alt to Vishay
353S4070	353S4069		ALL		Pericom alt to TI DP Mux U9750
353S4068	353S4069		ALL		NXP alt to TI DP Mux U9750
353S3814	353S3812		ALL		TI alt to NXP
311S0649	311S0541		ALL		ONsemi alt to Toshiba
138S0614	138S0578		ALL		Murata, TDK, Samsung, Taiyo Yuden alt to Murata, TDK
155S0694	155S0387		ALL		Murata alt to TDK
155S0660	155S0513		ALL		Murata alt to TDK
740S00003	740S0135		ALL		AEM alt to Tyco
138S0738	138S1101		ALL		Samsung alt to Murata for LCD BKL caps
353S00095	353S3328		ALL		Pericom alt to TI
311S00007	311S0426		ALL		Diodes alt to NXP
128S0398	128S0220		ALL		Kemet alt to Sanyo
128S0386	128S0284		ALL		Kemet alt to Sanyo
128S0397	128S0325		ALL		Kemet alt to Sanyo
377S00011	377S0184		ALL		Infineon alt to Infineon
377S0155	377S0184		ALL		On Semi alt to Infineon
155S0914	155S0897		ALL		Panasonic alt to TDK
371S0558	371S0713		ALL		ST Micro alt to Diodes
128S0436	128S0392		ALL		Kemet alt to Sanyo
128S0445	128S0392		ALL		Panasonic alt to Sanyo
353S00034	353S2220		ALL		Pericom alt to Fairchild
311S00014	311S0515		ALL		Diodes alt to NXP
311S00008	311S0271		ALL		Diodes alt to NXP
197S0479	197S0478		ALL		Epson alt to NDK
311S00013	311S0508		ALL		Diodes alt to NXP
376S00014	376S0761		ALL		Toshiba alt to Vishay
371S00019	371S0463		ALL		Rohm alt to Rohm
371S00018	371S0619		ALL		Rohm alt to Rohm
311S00015	311S0450		ALL		Diodes alt to NXP
371S00017	371S0749		ALL		Diodes alt to Onsemi
353S00107	353S3239	ANY	ALL		Onsemi alt to Intersil
107S00024	107S0226		ALL		Yageo alt to Cyntec
372S0186	372S0185		ALL		NXP alt to Diodes
353S00231	353S3987		ALL		NXP alt to TI
353S00135	353S2220		ALL		Onsemi alt to Fairchild
353S00133	353S2741		ALL		Onsemi alt to TI
131S00040	131S00041		ALL		Murata alt to Taiyo Yuden
107S00015	107S00011		ALL		TFT alt to Cyntec
107S00031	107S00032		ALL		TFT alt to Cyntec
107S00029	107S00030		ALL		TFT alt to Cyntec

SYNC_MASTER=J14 SYNC_DATE=09/04/2013

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Apple Inc.

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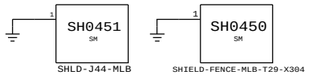
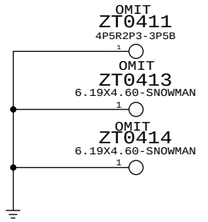
Shield Cans



USB Cage

TBT Cage

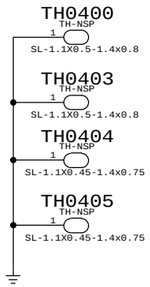
Mounting Holes & Slots



ABOVE GUMSTICK CARD IN MIDDLE OF BOARD
(998-1195)

SNOWMAN-SHAPED SLOT AT LEFT OF MEMORY BANK
(998-5879)

SNOWMAN-SHAPED SLOT AT RIGHT OF MEMORY BANK
(998-5879)



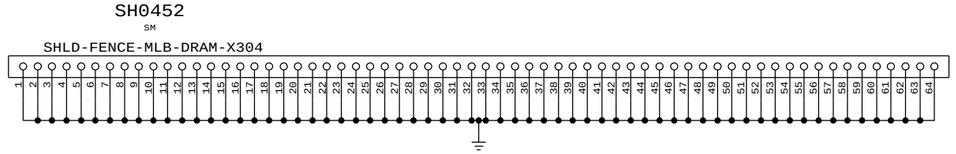
Upper TBT can Ground slot
(862-0118)

Lower TBT can Ground slot
(862-0118)

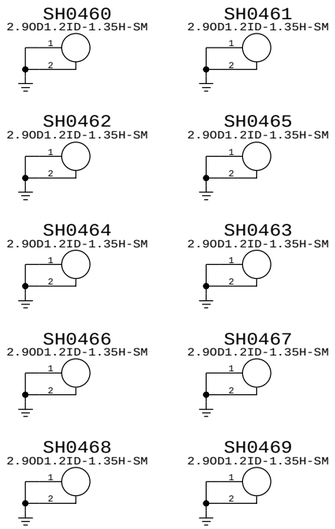
USB can Ground slot
(998-3975)

USB can Ground slot
(998-3975)

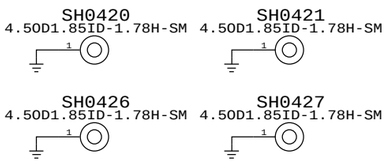
Memory Shield CAN (806-00037)



Rubber Mount Standoffs (860-1448)

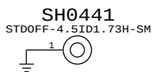


THERMAL MODULE STANDOFF (860-00165)



SSD STANDOFF (860-00164)

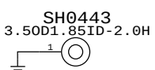
FAN STANDOFF (860-00183)



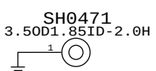
POGO PINS (870-00607)

SH0435 & SH0436 removed.

RIO FLEX BRACKET BOSSES (860-00166)



IPD FLEX BRACKET BOSSES (860-00166)



BOM_COST_GROUP=PD PARTS

SYNC_MASTER=LDUNN_J44 SYNC_DATE=01/13/2012

PAGE TITLE: PD Parts

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

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DDI Port Assignments:

TBT Sink 0

TBT Sink 1
(MUXed with HDMI
if necessary)

OMIT_TABLE
CRITICAL
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 1 OF 19

DP_TBTSNK0_ML_C_N<0>	C54	DDI1_TXN0		EDP_TXN0	C45	DP_INT_ML_C_N<0>	
DP_TBTSNK0_ML_C_P<0>	C55	DDI1_TXP0		EDP_TXP0	B46	DP_INT_ML_C_P<0>	
DP_TBTSNK0_ML_C_N<1>	B58	DDI1_TXN1		EDP_TXN1	A47	DP_INT_ML_C_N<1>	
DP_TBTSNK0_ML_C_P<1>	C58	DDI1_TXP1		EDP_TXP1	B47	DP_INT_ML_C_P<1>	
DP_TBTSNK0_ML_C_N<2>	B55	DDI1_TXN2		EDP_TXN2	C47	DP_INT_ML_C_N<2>	
DP_TBTSNK0_ML_C_P<2>	A55	DDI1_TXP2		EDP_TXP2	C46	DP_INT_ML_C_P<2>	
DP_TBTSNK0_ML_C_N<3>	A57	DDI1_TXN3		EDP_TXN3	A49	DP_INT_ML_C_N<3>	
DP_TBTSNK0_ML_C_P<3>	B57	DDI1_TXP3		EDP_TXP3	B49	DP_INT_ML_C_P<3>	
=DP_TBTSNK1_ML_C_N<0>	C51	DDI2_TXN0					
=DP_TBTSNK1_ML_C_P<0>	C50	DDI2_TXP0					
=DP_TBTSNK1_ML_C_N<1>	C53	DDI2_TXN1					
=DP_TBTSNK1_ML_C_P<1>	B54	DDI2_TXP1		EDP_AUXN	A45	DP_INT_AUXCH_C_N	
=DP_TBTSNK1_ML_C_N<2>	C49	DDI2_TXN2		EDP_AUXP	B45	DP_INT_AUXCH_C_P	
=DP_TBTSNK1_ML_C_P<2>	B50	DDI2_TXP2					
=DP_TBTSNK1_ML_C_N<3>	A53	DDI2_TXN3		EDP_RCOMP	D20	MCP_EDP_RCOMP	
=DP_TBTSNK1_ML_C_P<3>	B53	DDI2_TXP3		EDP_DISP_UTIL	A43	TP_EDP_DISP_UTIL	

eDP Port Assignment:

Internal panel

PPVCOMP_S0_CPU

R0530
24.9
1%
1/20W
MF
201

MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.

OMIT_TABLE
CRITICAL
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 17 OF 19

	NO_TEST				NO_TEST	
MCP_DC_AW2_AY2	TRUE	AY2	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A3 TRUE	MCP_DC_A3_B3
MCP_DC_AW3_AY3	TRUE	AY3	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A4	MCP_DC_A4 → TP0500
MCP_DC_AY60		AY60	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A60	MCP_DC_A60 → TP0510
TP0531 → MCP_DC_AW61_AY61	TRUE	AY61	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A61 TRUE	MCP_DC_A61_B61
MCP_DC_AW62_AY62	TRUE	AY62	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	A62	MCP_DC_A62 → TP0511
TP0501 → MCP_DC_B2		B2	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AV1	MCP_DC_AV1 → TP0520
MCP_DC_A3_B3	TRUE	B3	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW1	MCP_DC_AW1 → TP0521
MCP_DC_A61_B61	TRUE	B61	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW2 TRUE	MCP_DC_AW2_AY2
MCP_DC_B62_B63	TRUE	B62	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW3 TRUE	MCP_DC_AW3_AY3
		B63	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW61 TRUE	MCP_DC_AW61_AY61
MCP_DC_C1_C2	TRUE	C1	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW62 TRUE	MCP_DC_AW62_AY62
		C2	DAISY_CHAIN_NCTF	DAISY_CHAIN_NCTF	AW63	MCP_DC_AW63 → TP0530

OMIT_TABLE
CRITICAL
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 18 OF 19
SPARE

NC	AT2	RSVD	RSVD	N23 NC
NC	AU44	RSVD	RSVD	R23 NC
NC	AV44	RSVD	RSVD	T23 NC
NC	D15	RSVD	RSVD	U10 NC
NC	F22	RSVD	RSVD	AL1 NC
NC	H22	RSVD	RSVD	AM11 NC
NC	J21	RSVD	RSVD	AP7 NC
			RSVD	AU10 NC
			RSVD	AU15 NC
			RSVD	AW14 NC
			RSVD	AY14 NC

BOM_COST_GROUP=CPU

SYNC_MASTER=J41 SYNC_DATE=10/23/2012

PAGE TITLE
CPU GFX,NCTF,RSVD

Apple Inc.

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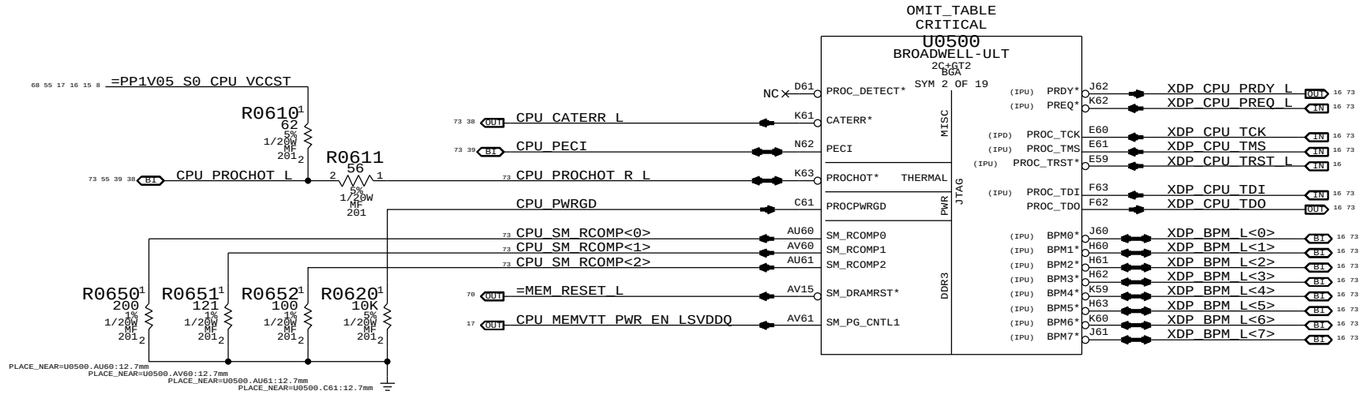
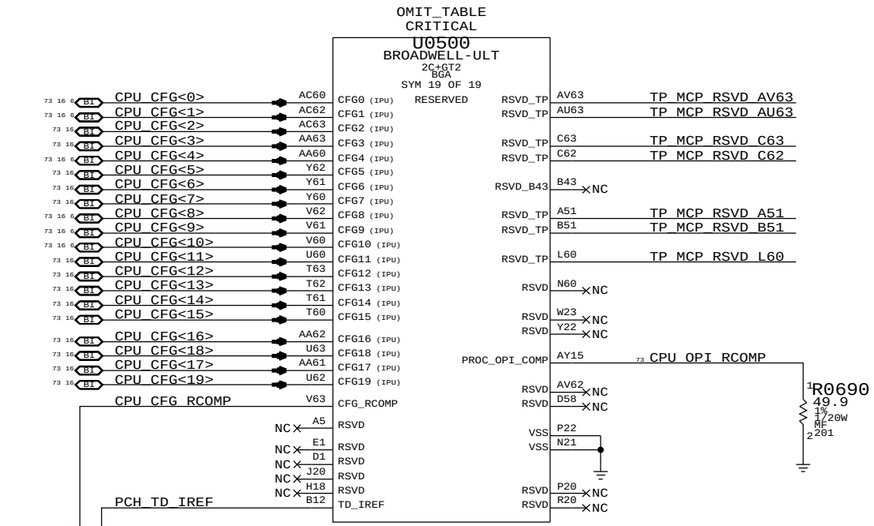
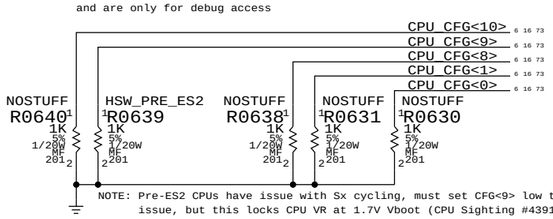
SHEET 5 OF 82



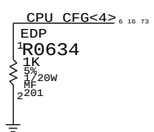


CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



BOM_COST_GROUP=CPU

SYNC_MASTER=J41	SYNC_DATE=10/23/2012
PAGE TITLE	CPU Misc,JTAG,CFG,RSVD
Apple Inc.	DRAWING NUMBER 051-1573 SIZE D
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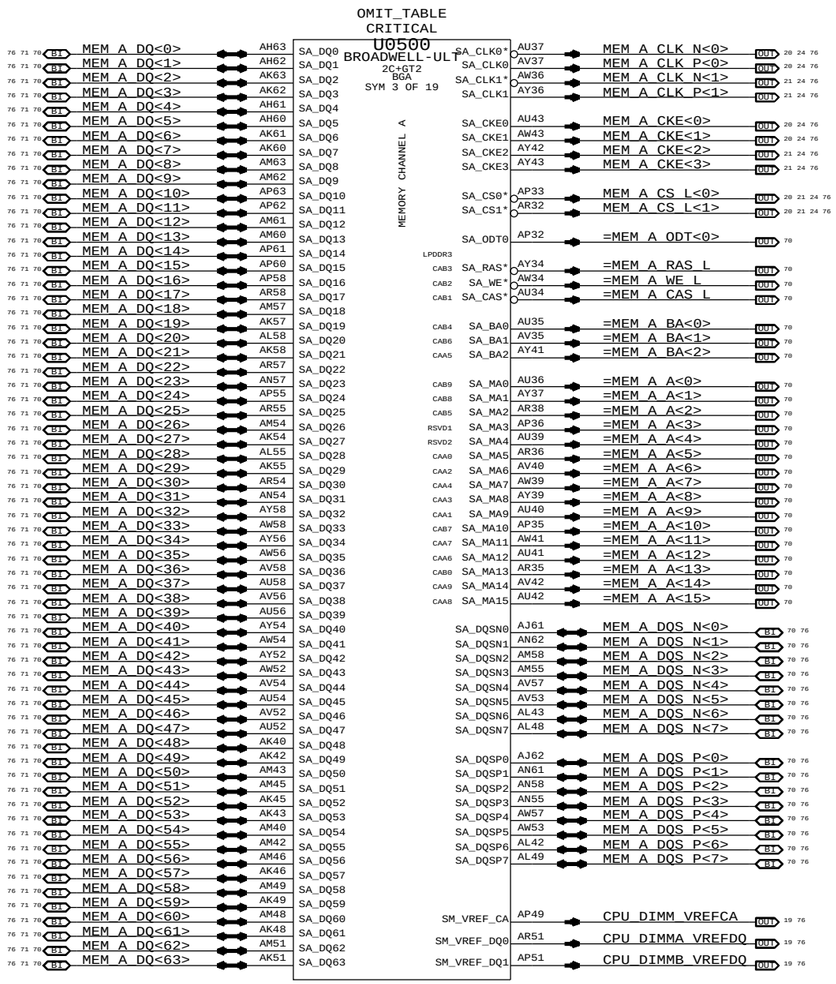

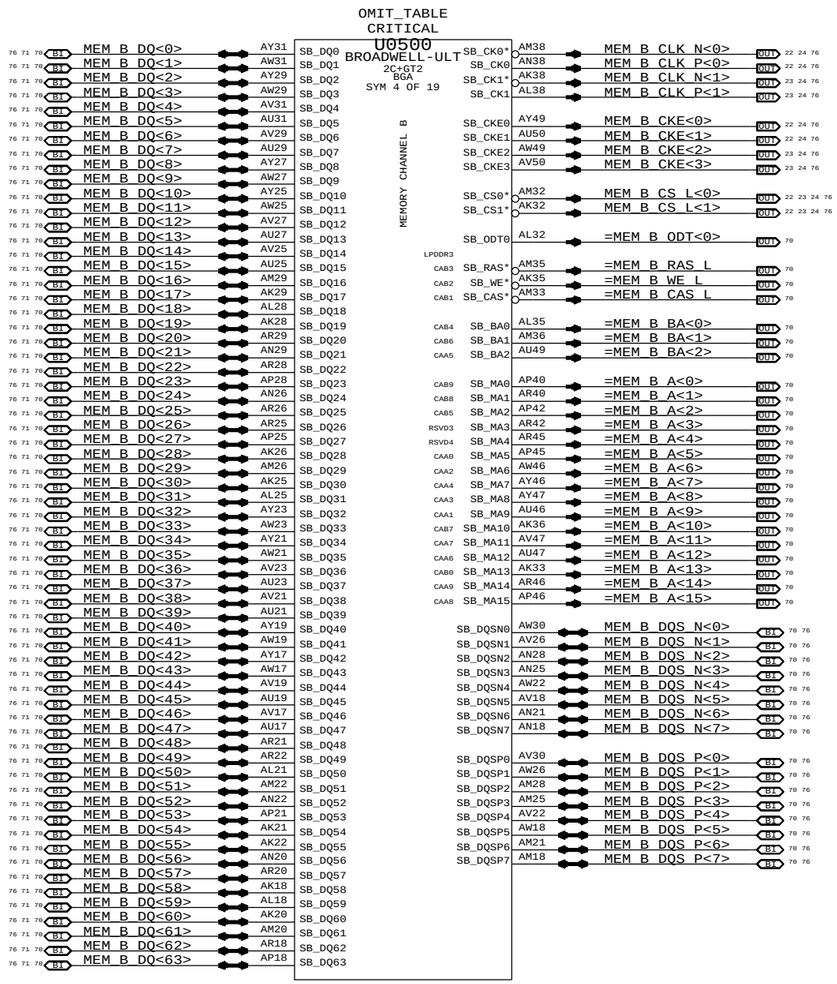

SYNC_MASTER=J41 SYNC_DATE=10/23/2012

PAGE TITLE

CPU LPDDR3 Interfaces

Apple Inc.

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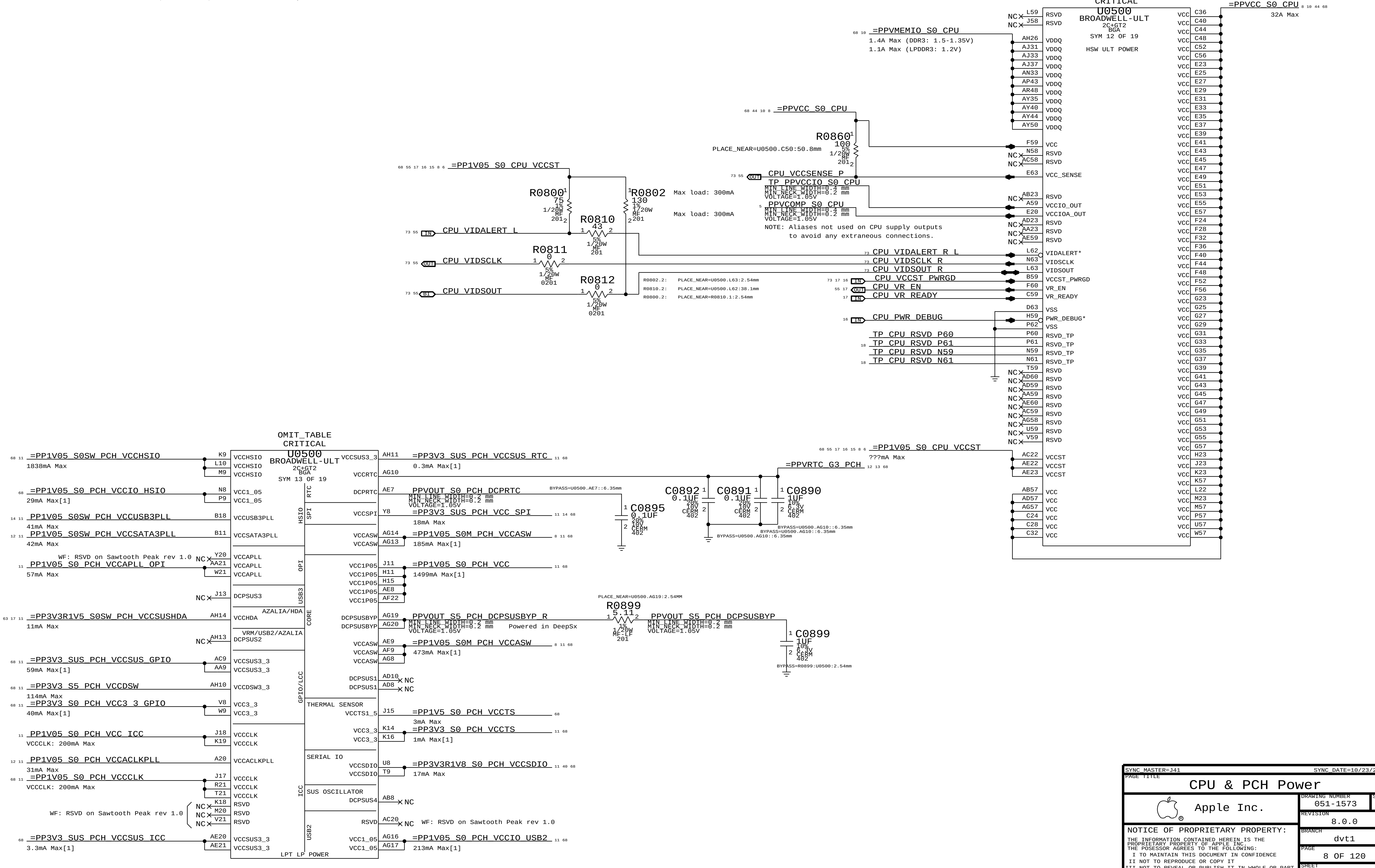
BOM_COST_GROUP=CPU

BDW-ULT current estimates from Broadwell Mobile ULT Processor EDS vol.1 Doc# 514405, Rev.: 0.9v1
Wildcat Point-LP current estimates from Wildcat Point-LP PCH EDS, Doc# 515621, Rev. 0.9
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



BOM_COST_GROUP=CPU

SYNC_MASTER=J41 SYNC_DATE=10/23/2012

PAGE TITLE

CPU & PCH Power

Apple Inc.

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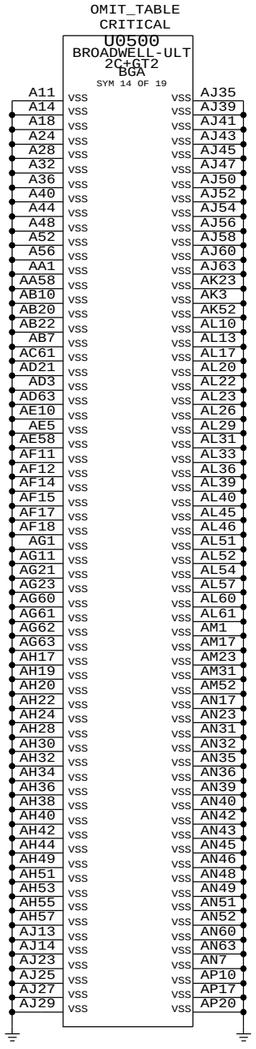

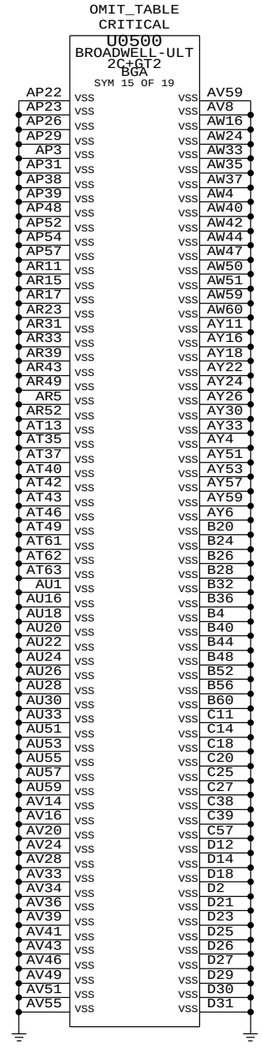

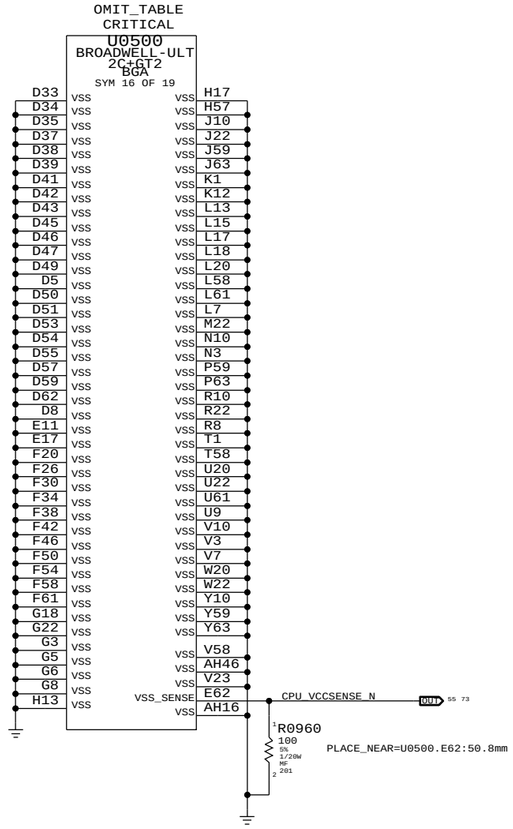

SYNC_MASTER=J41 SYNC_DATE=10/23/2012

PAGE TITLE

CPU & PCH Grounds

Apple Inc.

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BOM_COST_GROUP=CPU

All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 0.9 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 22uF 0603 stuff, 80x 22uF 0603 nostuff

=PPVCC_S0_CPU

C1000 CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1001 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1002 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1003 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1004 CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1008 CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1009 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1010 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1011 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1012 CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1014 CRITICAL 12PF 5% 50V C0G-CERM 0402
C105A CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C105B CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C105C CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C105D CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C105E CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C105F CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1018 CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1019 CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1020 CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1021 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1030 CRITICAL 12PF 5% 50V C0G-CERM 0402
C104E CRITICAL 12PF 5% 50V C0G-CERM 0402
C104F CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C106D CRITICAL 12PF 5% 50V C0G-CERM 0402
C106E CRITICAL 12PF 5% 50V C0G-CERM 0402
C1070 CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1072 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1073 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1074 CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1075 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1077 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1081 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1082 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1083 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1084 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1085 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1086 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1087 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1088 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1089 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1090 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1091 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1092 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1093 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1094 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1095 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1096 CRITICAL 10UF 20% 4V X6S 0402 NO STUFF
C1097 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1022 CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1023 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1024 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1025 NO STUFF 10UF 20% 4V X6S 0402
C1026 CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1027 NO STUFF 10UF 20% 4V X6S 0402
C1028 NO STUFF 10UF 20% 4V X6S 0402
C1029 NO STUFF 10UF 20% 4V X6S 0402
C1032 NO STUFF 10UF 20% 4V X6S 0402
C1033 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1034 CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1035 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1036 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1037 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1038 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1039 NO STUFF 10UF 20% 4V X6S 0402
C1044 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1045 NO STUFF 10UF 20% 4V X6S 0402
C1046 NO STUFF 10UF 20% 4V X6S 0402
C1047 NO STUFF 10UF 20% 4V X6S 0402
C1048 NO STUFF 10UF 20% 4V X6S 0402
C1049 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1056 NO STUFF 10UF 20% 4V X6S 0402
C1057 NO STUFF 10UF 20% 4V X6S 0402
C1058 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1059 NO STUFF 10UF 20% 4V X6S 0402
C1062 NO STUFF 10UF 20% 4V X6S 0402
C1063 NO STUFF 10UF 20% 4V X6S 0402
C1064 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1065 CRITICAL 10UF 20% 4V X6S 0402 OMIT_TABLE
C1066 NO STUFF 10UF 20% 4V X6S 0402
C1067 NO STUFF 10UF 20% 4V X6S 0402
C1068 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1069 CRITICAL 12PF 5% 50V C0G-CERM 0402
C1098 NO STUFF 10UF 20% 4V X6S 0402
C1099 CRITICAL 12PF 5% 50V C0G-CERM 0402
C109A NO STUFF 10UF 20% 4V X6S 0402
C109B NO STUFF 10UF 20% 4V X6S 0402
C109C CRITICAL 12PF 5% 50V C0G-CERM 0402
C109D NO STUFF 10UF 20% 4V X6S 0402
C109E CRITICAL 12PF 5% 50V C0G-CERM 0402
C109F NO STUFF 10UF 20% 4V X6S 0402
C108A CRITICAL 12PF 5% 50V C0G-CERM 0402
C108B CRITICAL 12PF 5% 50V C0G-CERM 0402
C108C NO STUFF 10UF 20% 4V X6S 0402
C108D NO STUFF 10UF 20% 4V X6S 0402
C108E CRITICAL 12PF 5% 50V C0G-CERM 0402
C108F CRITICAL 12PF 5% 50V C0G-CERM 0402
C107A NO STUFF 10UF 20% 4V X6S 0402
C107B CRITICAL 12PF 5% 50V C0G-CERM 0402
C1031 CRITICAL 470UF-0.0045OHM 20% 2.5V POLY-TANT SM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0942	18	CAP,CER,10UF,20%,4V,X6S,HRZTL,0402		CRITICAL	

C1000,C1004,C1008,C1012,C1018,C1019,C1020,C1022,C1026,C1034,C1065,C1070,C1074,C105A,C105C,C105D,C104F,C105F

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 2x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 2x 2.2uF 0402, 6x 10uF 0402

=PPVMEMIO_S0_CPU

C1040 2.2UF 20% 6.3V CERM 402-LF
C1041 2.2UF 20% 6.3V CERM 402-LF
C1042 2.2UF 20% 6.3V CERM 402-LF
C1043 2.2UF 20% 6.3V CERM 402-LF

Added 2 extra 2.2uF per Harris Beach v0.9 schematic

C1050 10UF 20% 6.3V CERM-X5R 0402-1 OMIT_TABLE
C1051 10UF 20% 6.3V CERM-X5R 0402-1 OMIT_TABLE
C1052 10UF 20% 6.3V CERM-X5R 0402-1 OMIT_TABLE
C1053 10UF 20% 6.3V CERM-X5R 0402-1 OMIT_TABLE
C1054 10UF 20% 6.3V CERM-X5R 0402-1 OMIT_TABLE
C1055 10UF 20% 6.3V CERM-X5R 0402-1 OMIT_TABLE
C1079 12PF 5% 25V NP0-C0G 0201
C1080 12PF 5% 25V NP0-C0G 0201
C1060 270UF 20% 2V TANT CASE-B2-SM
C1061 NO STUFF 270UF 20% 2V TANT CASE-B2-SM

1x Bulk nostuff, Harris Beach has 2x nostuff

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	6	CAP,CER,10UF,20%,6.3V,HRZTL,0402		CRITICAL	

C1050,C1051,C1052,C1053,C1054,C1055

CPU VCC Decoupling

NOTE: 38X capacitors are STUFFED and have been changed to 12pF for Noise Floor Reasons (Radar # 17754026).

BOM_COST_GROUP=CPU

SYNC_MASTER=J41 SYNC_DATE=10/23/2012
PAGE TITLE: CPU Decoupling
Apple Inc.
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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
68 8 =PP3V3_S5_PCH_VCCDSW
NO STUFF
C1200 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH10::6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
68 14 8 =PP3V3_SUS_PCH_VCC_SPI
NO STUFF
C1202 0.1UF 20% 10V CERM 402
BYPASS=U0500.Y8::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
68 8 =PP3V3_SUS_PCH_VCCSUS_GPIO
C1204 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.AC9::12.7mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
68 8 =PP3V3_SUS_PCH_VCCSUS_RTC
C1206 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH11::6.35mm

PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
68 40 8 =PP3V3R1V8_S0_PCH_VCCSDIO
C1208 1UF 10% 6.3V CERM 402
BYPASS=U0500.U8::6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
63 17 8 =PP3V3R1V5_S0SW_PCH_VCCSUSHDA
C1210 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH14::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
68 8 =PP3V3_S0_PCH_VCC3_3_GPIO
C1212 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.V8::12.7mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
68 8 =PP3V3_S0_PCH_VCCTS
C1214 0.1UF 20% 10V CERM 402
BYPASS=U0500.K14::6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
68 8 =PP1V05_S0M_PCH_VCCASW
NO STUFF
C1250 22UF 20% 6.3V X5R-CERM-1 603
C1251 1UF 10% 6.3V CERM 402
BYPASS=U0500.AE9::12.7mm
BYPASS=U0500.AE9::6.35mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
68 8 =PP1V05_S0_PCH_VCC
C1255 10UF 20% 6.3V X5R 603
C1256 1UF 10% 6.3V CERM 402
C1257 1UF 10% 6.3V CERM 402
BYPASS=U0500.J11::12.7mm
BYPASS=U0500.J11::6.35mm
BYPASS=U0500.AE8::6.35mm

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
68 8 =PP1V05_S0SW_PCH_VCCHSIO
C1260 1UF 10% 6.3V CERM 402
C1261 1UF 10% 6.3V CERM 402
C1262 10UF 20% 6.3V CERM-X5R 0402-1
OMIT_TABLE
BYPASS=U0500.K9::6.35mm
BYPASS=U0500.L10::6.35mm
BYPASS=U0500.M9::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
68 8 =PP1V05_S0_PCH_VCCIO_USB2
C1264 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG16::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
68 8 =PP1V05_S0_PCH_VCCCLK
C1266 1UF 10% 6.3V CERM 402
C1267 1UF 10% 6.3V CERM 402
BYPASS=U0500.J17::6.35mm
BYPASS=U0500.R21::6.35mm

68 =PP1V05_S0_PCH_PLLFILTERS
??mA Max
R1270 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603
PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL 8 12
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max
C1270 47UF 20% 4V X6S 0805
C1271 47UF 20% 4V X6S 0805
C1272 1UF 10% 10V X5R 402
BYPASS=U0500.A20::12.7mm
BYPASS=U0500.A20::12.7mm
BYPASS=U0500.A20::6.35mm

R1275 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603
PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC 8
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max
C1275 47UF 20% 4V X6S 0805
C1276 47UF 20% 4V X6S 0805
C1277 1UF 10% 10V X5R 402
BYPASS=U0500.J18::12.7mm
BYPASS=U0500.J18::12.7mm
BYPASS=U0500.J18::6.35mm

R1280 0 5% 1/16W MF-LF 402
CRITICAL
NO STUFF
L1280 2.2UH-240MA-0.221OHM 0603
PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI 8
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max
NO STUFF C1280 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1281 47UF 20% 4V CERM-X5R 0805-1
C1282 1UF 10% 10V X5R 402
BYPASS=U0500.AA21::12.7mm
BYPASS=U0500.AA21::12.7mm
BYPASS=U0500.AA21::6.35mm

68 =PP1V05_S0SW_PCH_VCCPLL_HSIO
83mA Max
CRITICAL
L1290 2.2UH-240MA-0.221OHM 0603
PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL 8 12
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max
NO STUFF C1290 47UF 20% 4V X6S 0805
C1291 47UF 20% 4V CERM-X5R 0805-1
C1292 1UF 10% 10V X5R 402
BYPASS=U0500.B11::12.7mm
BYPASS=U0500.B11::12.7mm
BYPASS=U0500.B11::6.35mm

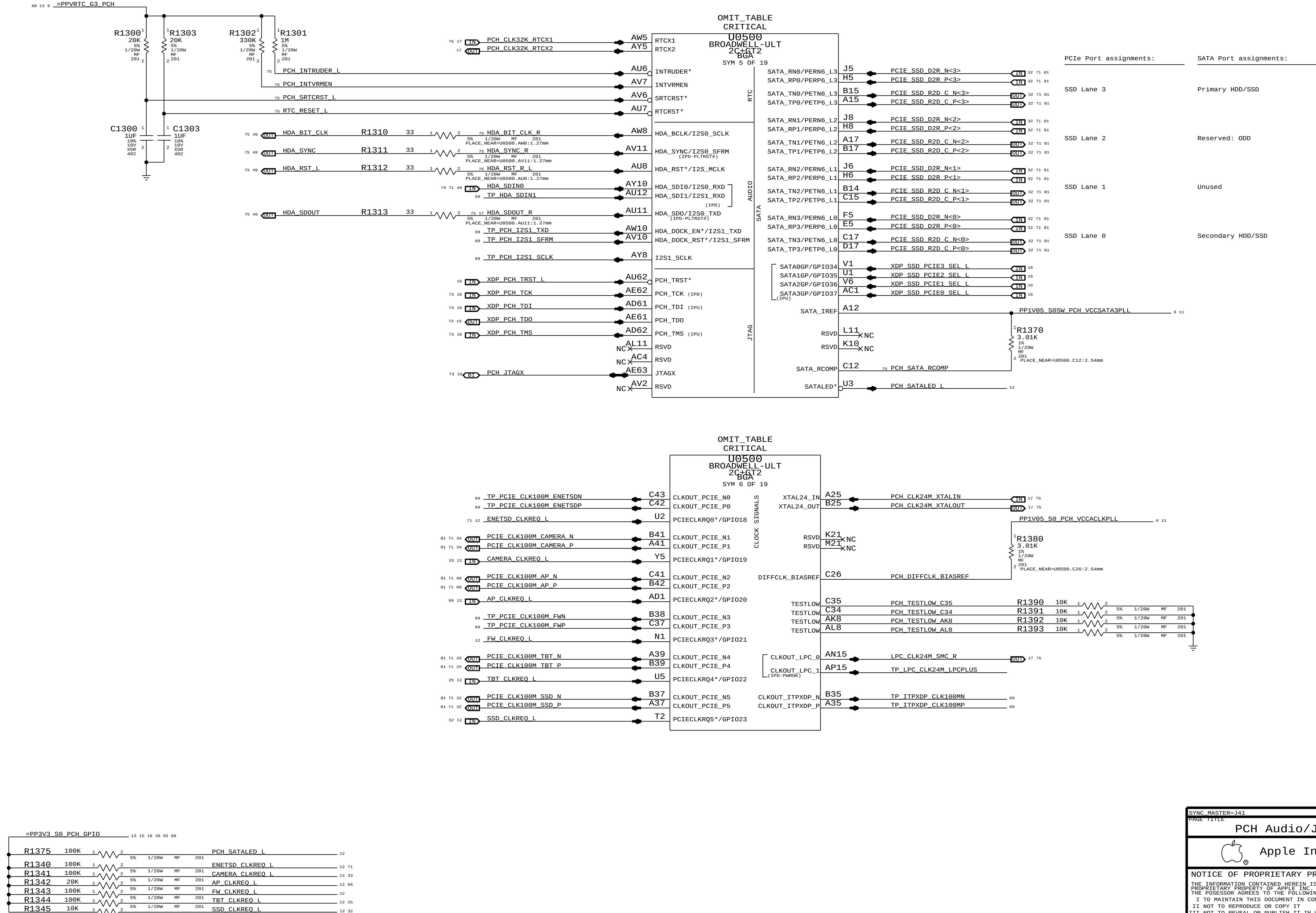
CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603
PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL 8 14
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max
C1295 47UF 20% 4V X6S 0805
C1297 1UF 10% 10V X5R 402
BYPASS=U0500.B18::12.7mm
BYPASS=U0500.B18::6.35mm

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	1	CAP,CER,10UF,20%,6.3V,HRZTL,0402	C1262	CRITICAL	

Wildcat Point-LP current estimates from Wildcat Point-LP PCH EDS, Doc# 515621, Rev. 0.9
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

BOM_COST_GROUP=CPU

SYNC_MASTER=J41 SYNC_DATE=10/23/2012
PAGE TITLE: PCH Decoupling
Apple Inc.
DRAWING NUMBER: 051-1573 SIZE: D
REVISION: 8.0.0
BRANCH: dvt1
PAGE: 12 OF 120
SHEET: 11 OF 82


=PPVRTC_G3_PCH
R1300 20K 5% 1/20W MF 201
R1303 20K 5% 1/20W MF 201
R1302 330K 5% 1/20W MF 201
R1301 1M 5% 1/20W MF 201
C1300 1UF 10% 10V X5R 402
C1303 1UF 10% 10V X5R 402
OMIT_TABLE
CRITICAL
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 5 OF 19
PCH_CLK32K_RTCX1 AW5 RTCX1
PCH_CLK32K_RTCX2 AY5 RTCX2
PCH_INTRUDER_L AU6 INTRUDER*
PCH_INTVRMEN AV7 INTVRMEN
PCH_SRTCRST_L AV6 SRTCRST*
RTC_RESET_L AU7 RTCRST*
RTC
HDA_BIT_CLK R1310 33 HDA_BIT_CLK_R AW8 HDA_BCLK/I2S0_SCLK
PLACE_NEAR=U0500.AW8:1.27mm
HDA_SYNC R1311 33 HDA_SYNC_R AV11 HDA_SYNC/I2S0_SFRM (IPD-PLTRST#)
PLACE_NEAR=U0500.AV11:1.27mm
HDA_RST_L R1312 33 HDA_RST_R_L AU8 HDA_RST*/I2S_MCLK
PLACE_NEAR=U0500.AU8:1.27mm
HDA_SDIN0 AY10 HDA_SDI0/I2S0_RXD
TP_HDA_SDIN1 AU12 HDA_SDI1/I2S1_RXD (IPD)
HDA_SDOUT R1313 33 HDA_SDOUT_R AU11 HDA_SDO/I2S0_TXD (IPD-PLTRST#)
PLACE_NEAR=U0500.AU11:1.27mm
TP_PCH_I2S1_TXD AW10 HDA_DOCK_EN*/I2S1_TXD
TP_PCH_I2S1_SFRM AV10 HDA_DOCK_RST*/I2S1_SFRM
TP_PCH_I2S1_SCLK AY8 I2S1_SCLK
AUDIO
XDP_PCH_TRST_L AU62 PCH_TRST*
XDP_PCH_TCK AE62 PCH_TCK (IPD)
XDP_PCH_TDI AD61 PCH_TDI (IPU)
XDP_PCH_TDO AE61 PCH_TDO
XDP_PCH_TMS AD62 PCH_TMS (IPU)
NC AL11 RSVD
NC AC4 RSVD
PCH_JTAGX AE63 JTAGX
NC AV2 RSVD
JTAG
SATA
SATA_RN0/PERN6_L3 J5 PCIE_SSD_D2R_N<3>
SATA_RP0/PERP6_L3 H5 PCIE_SSD_D2R_P<3>
SATA_TN0/PETN6_L3 B15 PCIE_SSD_R2D_C_N<3>
SATA_TP0/PETP6_L3 A15 PCIE_SSD_R2D_C_P<3>
SATA_RN1/PERN6_L2 J8 PCIE_SSD_D2R_N<2>
SATA_RP1/PERP6_L2 H8 PCIE_SSD_D2R_P<2>
SATA_TN1/PETN6_L2 A17 PCIE_SSD_R2D_C_N<2>
SATA_TP1/PETP6_L2 B17 PCIE_SSD_R2D_C_P<2>
SATA_RN2/PERN6_L1 J6 PCIE_SSD_D2R_N<1>
SATA_RP2/PERP6_L1 H6 PCIE_SSD_D2R_P<1>
SATA_TN2/PETN6_L1 B14 PCIE_SSD_R2D_C_N<1>
SATA_TP2/PETP6_L1 C15 PCIE_SSD_R2D_C_P<1>
SATA_RN3/PERN6_L0 F5 PCIE_SSD_D2R_N<0>
SATA_RP3/PERP6_L0 E5 PCIE_SSD_D2R_P<0>
SATA_TN3/PETN6_L0 C17 PCIE_SSD_R2D_C_N<0>
SATA_TP3/PETP6_L0 D17 PCIE_SSD_R2D_C_P<0>
SATA0GP/GPIO34 V1 XDP_SSD_PCIE3_SEL_L
SATA1GP/GPIO35 U1 XDP_SSD_PCIE2_SEL_L
SATA2GP/GPIO36 V6 XDP_SSD_PCIE1_SEL_L
SATA3GP/GPIO37 AC1 XDP_SSD_PCIE0_SEL_L (IPU)
SATA_IREF A12 PP1V05_S0SW_PCH_VCCSATA3PLL
RSVD L11 NC
RSVD K10 NC
R1370 3.01K 1% 1/20W MF 201 PLACE_NEAR=U0500.C12:2.54mm
SATA_RCOMP C12 PCH_SATA_RCOMP
SATALED* U3 PCH_SATALED_L
PCIe Port assignments:
SATA Port assignments:
SSD Lane 3 Primary HDD/SSD
SSD Lane 2 Reserved: ODD
SSD Lane 1 Unused
SSD Lane 0 Secondary HDD/SSD
OMIT_TABLE
CRITICAL
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 6 OF 19
TP_PCIE_CLK100M_ENETSDN C43 CLKOUT_PCIE_N0
TP_PCIE_CLK100M_ENETSDP C42 CLKOUT_PCIE_P0
ENETSD_CLKREQ_L U2 PCIECLKRQ0*/GPIO18
PCIE_CLK100M_CAMERA_N B41 CLKOUT_PCIE_N1
PCIE_CLK100M_CAMERA_P A41 CLKOUT_PCIE_P1
CAMERA_CLKREQ_L Y5 PCIECLKRQ1*/GPIO19
PCIE_CLK100M_AP_N C41 CLKOUT_PCIE_N2
PCIE_CLK100M_AP_P B42 CLKOUT_PCIE_P2
AP_CLKREQ_L AD1 PCIECLKRQ2*/GPIO20
TP_PCIE_CLK100M_FWN B38 CLKOUT_PCIE_N3
TP_PCIE_CLK100M_FWP C37 CLKOUT_PCIE_P3
FW_CLKREQ_L N1 PCIECLKRQ3*/GPIO21
PCIE_CLK100M_TBT_N A39 CLKOUT_PCIE_N4
PCIE_CLK100M_TBT_P B39 CLKOUT_PCIE_P4
TBT_CLKREQ_L U5 PCIECLKRQ4*/GPIO22
PCIE_CLK100M_SSD_N B37 CLKOUT_PCIE_N5
PCIE_CLK100M_SSD_P A37 CLKOUT_PCIE_P5
SSD_CLKREQ_L T2 PCIECLKRQ5*/GPIO23
CLOCK SIGNALS
XTAL24_IN A25 PCH_CLK24M_XTALIN
XTAL24_OUT B25 PCH_CLK24M_XTALOUT
PP1V05_S0_PCH_VCCACLKPLL
RSVD K21 NC
RSVD M21 NC
R1380 3.01K 1% 1/20W MF 201 PLACE_NEAR=U0500.C26:2.54mm
DIFFCLK_BIASREF C26 PCH_DIFFCLK_BIASREF
TESTLOW C35 PCH_TESTLOW_C35 R1390 10K
TESTLOW C34 PCH_TESTLOW_C34 R1391 10K
TESTLOW AK8 PCH_TESTLOW_AK8 R1392 10K
TESTLOW AL8 PCH_TESTLOW_AL8 R1393 10K
5% 1/20W MF 201
CLKOUT_LPC_0 AN15 LPC_CLK24M_SMC_R
CLKOUT_LPC_1 AP15 TP_LPC_CLK24M_LPCPLUS (IPD-PWROK)
CLKOUT_ITPXDP_N B35 TP_ITPXDP_CLK100MN
CLKOUT_ITPXDP_P A35 TP_ITPXDP_CLK100MP
=PP3V3_S0_PCH_GPIO
R1375 100K 5% 1/20W MF 201 PCH_SATALED_L
R1340 100K 5% 1/20W MF 201 ENETSD_CLKREQ_L
R1341 100K 5% 1/20W MF 201 CAMERA_CLKREQ_L
R1342 20K 5% 1/20W MF 201 AP_CLKREQ_L
R1343 100K 5% 1/20W MF 201 FW_CLKREQ_L
R1344 100K 5% 1/20W MF 201 TBT_CLKREQ_L
R1345 10K 5% 1/20W MF 201 SSD_CLKREQ_L
BOM_COST_GROUP=CPU

SYNC_MASTER=J41 SYNC_DATE=12/17/2012

PAGE TITLE

PCH Audio/JTAG/SATA/CLK

Apple Inc.

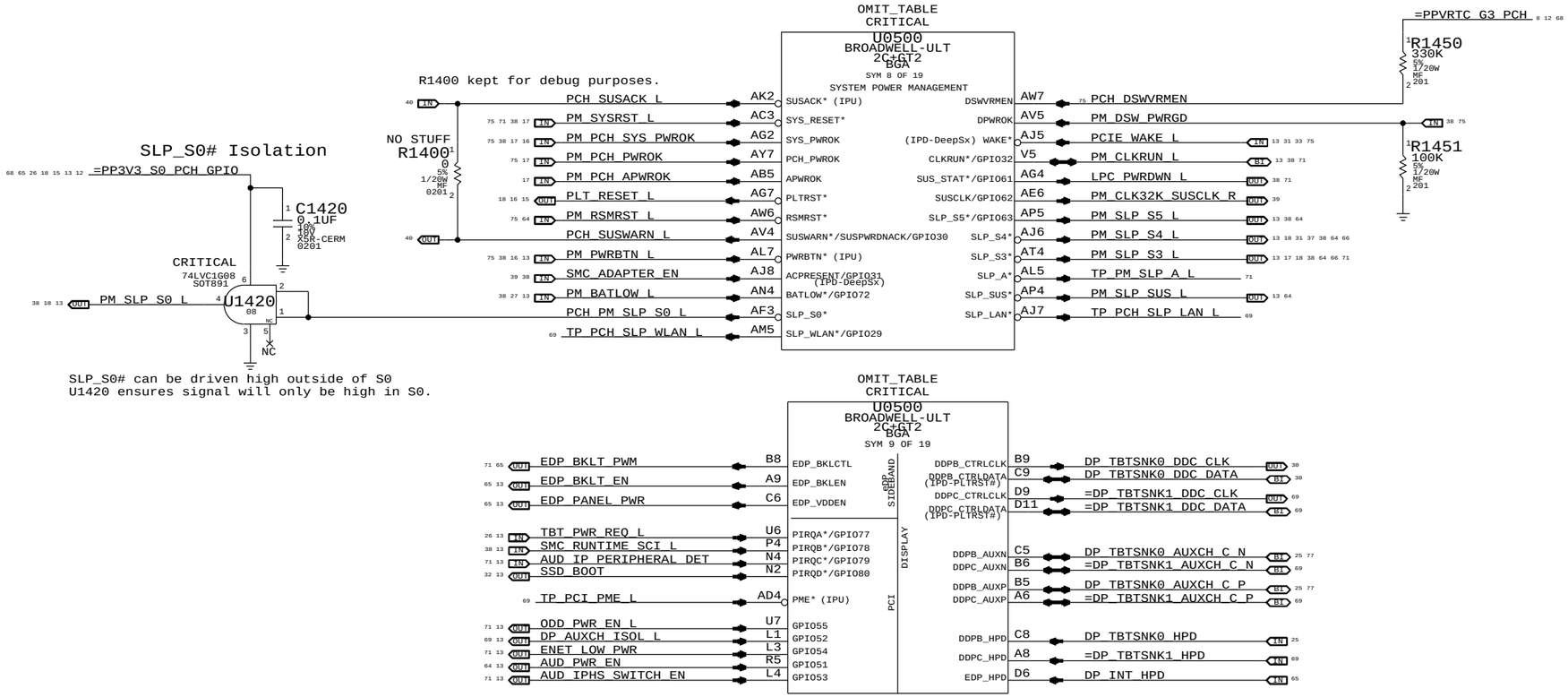
DRAWING NUMBER 051-1573 SIZE D

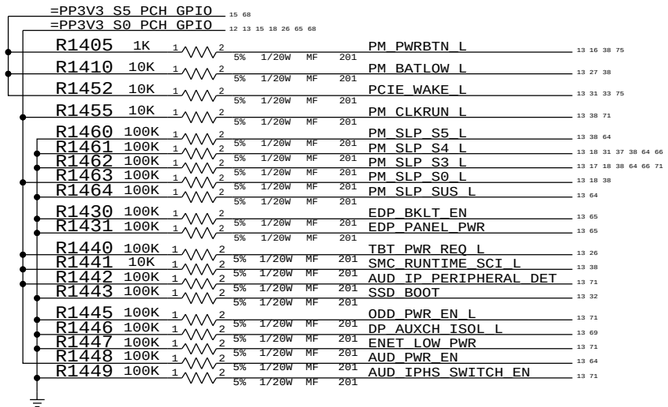
REVISION 8.0.0

BRANCH dvt1

PAGE 13 OF 120

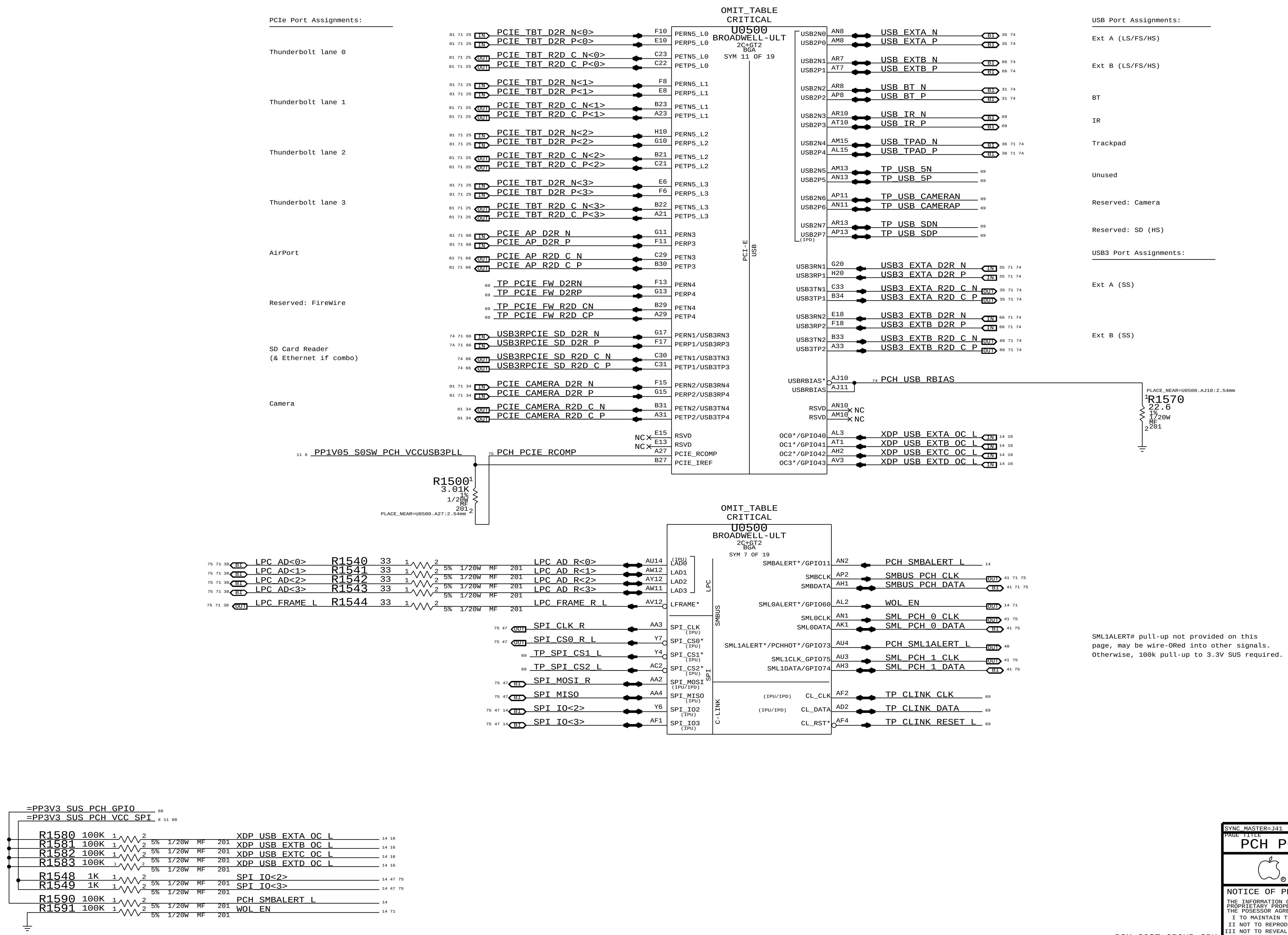
SHEET 12 OF 82





BOM_COST_GROUP=CPU

SYNC_MASTER=J41	SYNC_DATE=02/21/2013
PAGE TITLE	PCH PM/PCI/GFX
	Apple Inc.
DRAWING NUMBER	051-1573
SIZE	D
REVISION	8.0.0
BRANCH	dvt1
PAGE	14 OF 120
SHEET	13 OF 82



SYNC_MASTER=J41 SYNC_DATE=10/23/2012

PAGE TITLE: PCH PCIe,USB,LPC,SPI,SMBus

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

=PP3V3_S0_PCH_GPIO 12 13 15 18 26 65 68

RAMCFG3:H R1631 1 100K 5% 1/20W MF 201 2
RAMCFG2:H R1636 1 100K 5% 1/20W MF 201 2
RAMCFG1:H R1635 1 100K 5% 1/20W MF 201 2
RAMCFG0:H R1611 1 100K 5% 1/20W MF 201 2

XDP_MLB_RAMCFG0 15 16 18
XDP_MLB_RAMCFG1 15 16 18
XDP_MLB_RAMCFG2 15 16 18
XDP_MLB_RAMCFG3 15 16 18

GPIO12:
CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC

D1600 BAT54XV2T1 SOD-523
69 BI =TBT_GO2SX_BIDIR

R1600 1 1M 5% 1/20W MF 201 2

18 16 15 13 IN PLT_RESET_L
R1621 1 100K 5% 1/20W MF 201 2
18 OUT

TPAD_SPI_INT_GPIO28_L 15
R1681 1 0 5% 1/20W MF 0201 2
71 36 18 IN TPAD_SPI_INT_L
R1682 1 0 5% 1/20W MF 0201 2
TPAD_SPI_INT_GPIO46_L 15

R1639 1 100K 5% 1/20W MF 201 2
R1680 1 100K 5% 1/20W MF 201 2

68 65 26 18 15 13 12 =PP3V3_S0_PCH_GPIO
R1641 1K 1 2 5% 1/20W MF 201

OMIT_TABLE
CRITICAL
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 10 OF 19

16 15 BI XDP_PCH_GPIO76	P1	BMBUSY*/GPIO76
18 16 15 BI XDP_MLB_RAMCFG0	AU2	GPIO8
HDMI_TBT_MUX_SEL_GPIO12	AM7	LAN_PHY_PWR_CTRL/GPIO12
TP_MEM_VDD_SEL_1V5_L	AD6	GPIO15 (IPD-RSMRST#)
16 15 BI XDP_LPCPLUS_GPIO	Y1	GPIO16
16 15 IN XDP_PCH_GPIO17	T3	GPIO17
66 15 OUT SD_RESET_L	AD5	GPIO24
38 15 IN SMC_WAKE_SCI_L	AN5	GPIO27 (IPD-DeepSx)
15 TPAD_SPI_INT_GPIO28_L	AD7	GPIO28
37 15 TPAD_USB_IF_EN	AN3	GPIO26
64 32 15 OUT SSD_PWR_EN	AG6	GPIO56
PCH_TBT_PCIE_RESET_L	AP1	GPIO57
71 15 OUT HDD_PWR_EN	AL4	GPIO58
16 15 BI XDP_SDCONN_STATE_CHANGE_L	AT5	GPIO59
66 15 OUT SD_PWR_EN	AK4	GPIO44
25 15 OUT TBT_PWR_EN	AB6	GPIO47
16 15 OUT XDP_JTAG_ISP_TCK	U4	GPIO48
16 15 OUT XDP_JTAG_ISP_TDI	Y3	GPIO49
18 15 OUT JTAG_TBT_TMS_PCH	P3	GPIO50
63 15 OUT PCH_HSIO_PWR_EN	Y2	HSIOPC/GPIO71
37 15 OUT TPAD_SPI_IF_EN	AT3	GPIO13
18 16 15 BI XDP_MLB_RAMCFG3	AH4	GPIO14
71 47 15 BI SPIROM_USE_MLB	AM4	GPIO25
18 15 OUT CAMERA_PWR_EN_PCH	AG5	GPIO45
15 TPAD_SPI_INT_GPIO46_L	AG3	GPIO46
18 16 15 BI XDP_MLB_RAMCFG1	AM3	GPIO9
18 16 15 BI XDP_MLB_RAMCFG2	AM2	GPIO10
32 15 OUT SSD_SR_EN_L	P2	DEVSLP0/GPIO33
31 15 OUT AP_S0IX_WAKE_SEL	C4	SDIO_POWER_EN/GPIO70
32 OUT SSD_RESET_L	L2	DEVSLP1/GPIO38
33 18 OUT CAM_PCIE_RESET_L	N5	DEVSLP2/GPIO39
PCH_TCO_TIMER_DISABLE	V2	SPKR/GPIO81 (IPD-PLTRST#)

CPU/MISC

THERMTRIP*	D60	PM_THRMTRIP_L OUT 39 75
RCIN*/GPIO82	V4	=TBT_CIO_PLUG_EVENT IN 18
SERIRQ	T4	LPC_SERIRQ BI 15 38 71
PCH_OPI_COMP	AW15	75 PCH_OPI_COMP
RSVD	AF20	NC
RSVD	AB21	NC

GPIO LPIO

GSPI0_CS*/GPIO83	R6	PCH_GSPI0_CS_L 15
GSPI0_CLK/GPIO84	L6	PCH_GSPI0_CLK 15
GSPI0_MISO/GPIO85 (IPD)	N6	PCH_GSPI0_MISO 15
GSPI0_MOSI/GPIO86 (IPD-PLTRST#)	L8	PCH_GSPI0_MOSI 15
GSPI1_CS*/GPIO87	R7	TPAD_SPI_CS_L OUT 15 37 75
GSPI1_CLK/GPIO88	L5	TPAD_SPI_CLK OUT 15 37 75
GSPI1_MISO/GPIO89 (IPD)	N7	TPAD_SPI_MISO IN 15 37 75
GSPI_MOSI/GPIO90	K2	TPAD_SPI_MOSI OUT 15 37 75
UART0_RXD/GPIO91	J1	AP_S0IX_WAKE_L IN 15 31
UART0_TXD/GPIO92	K3	HDMITBTMUX_FLAG_L IN 15 67
UART0_RTS*/GPIO93	J2	JTAG_ISP_TDO IN 15 18
UART0_CTS*/GPIO94	G1	AP_RESET_L OUT 66
UART1_RXD/GPIO0	K4	PCH_UART1_RXD 15
UART1_TXD/GPIO1	G2	PCH_UART1_TXD 15
UART1_RST*/GPIO2	J3	PCH_UART1_RTS_L 15
UART1_CTS*/GPIO3	J4	PCH_UART1_CTS_L 15
I2C0_SDA/GPIO4	F2	PCH_I2C0_SDA 15
I2C0_SCL/GPIO5	F3	PCH_I2C0_SCL 15
I2C1_SDA/GPIO6	G4	PCH_I2C1_SDA 15
I2C1_SCL/GPIO7	F1	PCH_I2C1_SCL 15
SDIO_CLK/GPIO64	E3	TBT_POC_RESET_L OUT 26
SDIO_CMD/GPIO65	F4	BT_PWRRST_L OUT 15 71
SDIO_D0/GPIO66 (IPD-PLTRST#)	D3	PCH_STRP_TOPBLK_SWP_L IN 40
SDIO_D1/GPIO67	E4	ENET_MEDIA_SENSE IN 15 71
SDIO_D2/GPIO68	C3	LCD_IRQ_L IN 65 71
SDIO_D3/GPIO69	E2	LCD_PSR_EN OUT 15 65

68 55 17 16 8 6 =PP1V05_S0_CPU_VCCST
R1650 1 1K 5% 1/20W MF 201 2

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

PLACE_NEAR=U0500.AW15:2.54mm
R1655 1 49.9 1% 1/20W MF 201 2

PLT_RESET_L IN 13 15 16 18
R1671 1 100K 5% 1/20W MF 201 2 OUT 66

Pull-up on TBT page

Requires connection to SMC via 1K series R

R1694 10K 5% 1/20W MF 201
65 41 PP3V3_S0_EDP_SW 1 2

=PP3V3_S5_PCH_GPIO 13 68
=PP3V3_S3RS4_PCH_GPIO 68
=PP3V3_S3SW_SD_RESET 68
=PP3V3_S3_PCH_GPIO 68
=PP3V3_S3RS0_CAMPWREN 18 44
=PP3V3_S0_PCH_GPIO 12 13 15 18 26 65 68
=PP3V3_S0RTBTLC_PCH_GPIO 68

TBTLC for CR, S0 for RR

R1610 100K	XDP_PCH_GPIO76	15 16
R1614 100K	XDP_LPCPLUS_GPIO	15 16
R1615 100K	XDP_PCH_GPIO17	15 16
SD_ON_MLB		
R1616 100K	SD_RESET_L	15 66
R1617 100K	SMC_WAKE_SCI_L	15 38
R1618 100K	TPAD_SPI_INT_L	15 36 71
R1619 100K	TPAD_USB_IF_EN	15 37
R1620 100K	SSD_PWR_EN	15 32 64
R1622 100K	HDD_PWR_EN	15 71
R1623 100K	XDP_SDCONN_STATE_CHANGE_L	15 16
R1624 100K	SD_PWR_EN	15 66
R1625 100K	TBT_PWR_EN	15 25
R1626 100K	XDP_JTAG_ISP_TCK	15 16
R1627 100K	XDP_JTAG_ISP_TDI	15 16
R1628 100K	JTAG_TBT_TMS_PCH	15 18
R1629 100K	PCH_HSIO_PWR_EN	15 63
R1630 100K	TPAD_SPI_IF_EN	15 37
R1632 100K	SPIROM_USE_MLB	15 47 71
R1633 100K	CAMERA_PWR_EN_PCH	15 18
R1637 100K	SSD_SR_EN_L	15 32
R1638 100K	AP_S0IX_WAKE_SEL	15 31
R1652 10K	LPC_SERIRQ	15 38 71
R1670 100K	JTAG_ISP_TDO	15 18
R1691 100K	BT_PWRRST_L	15 71
R1693 100K	ENET_MEDIA_SENSE	15 71
R1695 100K	LCD_PSR_EN	15 65

All: 1 2 5% 1/20W MF 201

R1616 should also be stuffed if platform does not use SD card

STUFFED R1632

68 65 26 18 15 13 12 =PP3V3_S0_PCH_GPIO

PCH_GSPI0_CS_L	R1660 100K	15
PCH_GSPI0_CLK	R1661 100K	15
PCH_GSPI0_MISO	R1662 100K	15
PCH_GSPI0_MOSI	R1663 100K	15
TPAD_SPI_CS_L	R1664 47K	75 37 15
TPAD_SPI_CLK	R1665 47K	75 37 15
TPAD_SPI_MISO	R1666 47K	75 37 15
TPAD_SPI_MOSI	R1667 47K	75 37 15
AP_S0IX_WAKE_L	R1668 100K	31 15
HDMITBTMUX_FLAG_L	R1669 100K	67 15
PCH_UART1_RXD	R1672 100K	15
PCH_UART1_TXD	R1673 100K	15
PCH_UART1_RTS_L	R1674 100K	15
PCH_UART1_CTS_L	R1675 100K	15
PCH_I2C0_SDA	R1676 100K	15
PCH_I2C0_SCL	R1677 100K	15
PCH_I2C1_SDA	R1678 100K	15
PCH_I2C1_SCL	R1679 100K	15

All: 1 2 5% 1/20W MF 201

SYNC_MASTER=J41 SYNC_DATE=01/19/2013

PAGE TITLE
PCH GPIO/MISC/LPIO

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
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BOM_COST_GROUP=CPU

Merged (CPU/PCH) Micro2-XDP

Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807
(TP-P6)

=PP1V05_S0_XDP

R1830 150 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1
518S0847

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_CPU_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_CPU_TDI
	TCK0	TMS	XDP_CPU_TMS
		XDP_PRESENT#	XDP_CPU_PRESENT_L

XDP_CPU_VCCST_PWRGD → R1800 1K XDP 5% 1/20W MF 201, PLACE_NEAR=U0500.C61:2.54mm
PM_PWRBTN_L → R1802 0 XDP 5% 1/20W MF 0201, PLACE_NEAR=U5000.J3:2.54mm
PM_PCH_SYS_PWROK → R1804 0 XDP 5% 1/16W MF-LF 402
XDP_CPU_TCK
PCH_JTAGX → R1835 0 XDP 5% 1/20W MF 0201, PLACE_NEAR=J1800.58:28mm

C1804 0.1UF 10% 6.3V X5R-CERM 0201 XDP
R1831 1K 5% 1/16W MF-LF 402 XDP
C1800 0.1UF 10% 6.3V X5R-CERM 0201 XDP
C1801 0.1UF 10% 6.3V X5R-CERM 0201 XDP
C1806 0.1UF 10% 6.3V X5R-CERM 0201 XDP

=PP1V05_S0_CPU_VCCST
XDP_CPU_TDO → R1810 51 XDP, PLACE_NEAR=U0500.F62:28mm
XDP_CPU_TCK → R1813 51 XDP, PLACE_NEAR=U0500.E60:28mm
TDI and TMS are terminated in CPU.

R1805 1K XDP 5% 1/20W MF 201, PLACE_NEAR=U0500.AG7:2.54mm
PLT_RESET_L
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS

CRITICAL XDP Q1840 DMN5L06VK-7 SOT563 VER 3
SIGNAL_MODEL=DMN5L06VK_7
PLACE_NEAR=J1800.51:28mm
XDP_CPU_TDO

CRITICAL XDP Q1840 DMN5L06VK-7 SOT563 VER 3
SIGNAL_MODEL=DMN5L06VK_7
PLACE_NEAR=J1800.53:28mm
XDP_CPUPCH_TRST_L (MAKE_BASE=TRUE)
XDP_CPU_TRST_L
XDP_PCH_TRST_L

CRITICAL XDP Q1842 DMN5L06VK-7 SOT563 VER 3
SIGNAL_MODEL=DMN5L06VK_7
PLACE_NEAR=J1800.55:28mm
XDP_CPU_TDI

CRITICAL XDP Q1842 DMN5L06VK-7 SOT563 VER 3
SIGNAL_MODEL=DMN5L06VK_7
PLACE_NEAR=J1800.57:28mm
XDP_CPU_TMS

CPU JTAG Isolation

=PP5V_S0_XDPJTAGISOL
=PP3V3_S5_XDPJTAGISOL
C1845 0.1UF 10% 10V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, GND, A, Y, NC)
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

=PP1V05_SUS_PCH_JTAG
PCH_JTAGX → R1899 1K NO STUFF, PLACE_NEAR=U0500.AE63:28mm
XDP_PCH_TDO → R1890 51 XDP, PLACE_NEAR=U0500.AE61:28mm
XDP_PCH_TDI → R1891 51 XDP, PLACE_NEAR=U0500.AD61:28mm
XDP_PCH_TMS → R1892 51 XDP, PLACE_NEAR=U0500.AD62:28mm
XDP_PCH_TCK → R1896 51 NO STUFF, PLACE_NEAR=U0500.AE62:28mm
XDP_PCH_TRST_L → R1897 51 NO STUFF, PLACE_NEAR=U0500.AU62:28mm

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals		Non-XDP Signals
XDP_MLB_RAMCFG0	TP1870	
XDP_USB_EXTA_OC_L	(MAKE_BASE=TRUE)	USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	(MAKE_BASE=TRUE)	USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	TP1873	
XDP_USB_EXTD_OC_L	TP1874	
XDP_SDCONN_STATE_CHANGE_L	(MAKE_BASE=TRUE)	SDCONN_STATE_CHANGE_L
XDP_MLB_RAMCFG1	TP1876	
XDP_MLB_RAMCFG2	TP1877	
XDP_MLB_RAMCFG3	TP1878	
XDP_JTAG_ISP_TCK	(MAKE_BASE=TRUE)	JTAG_ISP_TCK
XDP_SSD_PCIE3_SEL_L	R1881 1K	
XDP_SSD_PCIE2_SEL_L	R1882 1K	NOTE: Must not short XDP pins together!
XDP_SSD_PCIE1_SEL_L	R1883 1K	
XDP_SSD_PCIE0_SEL_L	R1884 1K	SSD_PCIE_SEL_L
XDP_LPCPLUS_GPIO	(MAKE_BASE=TRUE)	LPCPLUS_GPIO
XDP_PCH_GPIO17	TP1886	
XDP_PCH_GPIO76	TP1887	
XDP_JTAG_ISP_TDI	(MAKE_BASE=TRUE)	JTAG_ISP_TDI

(R1881–R1884: 5% 1/20W MF 201)

Unused & MLB_RAMCFGx GPIOs have TPs.
USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.
JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.
NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.
SSD_PCIEx_SEL_L straps are connected via 1K to common net.
LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

BOM_COST_GROUP=CPU SUPPORT

SYNC_MASTER=WFERRY_J43 SYNC_DATE=12/21/2012
PAGE TITLE: CPU/PCH Merged XDP
Apple Inc.
DRAWING NUMBER: 051-1573
SIZE: D
REVISION: 8.0.0
BRANCH: dvt1
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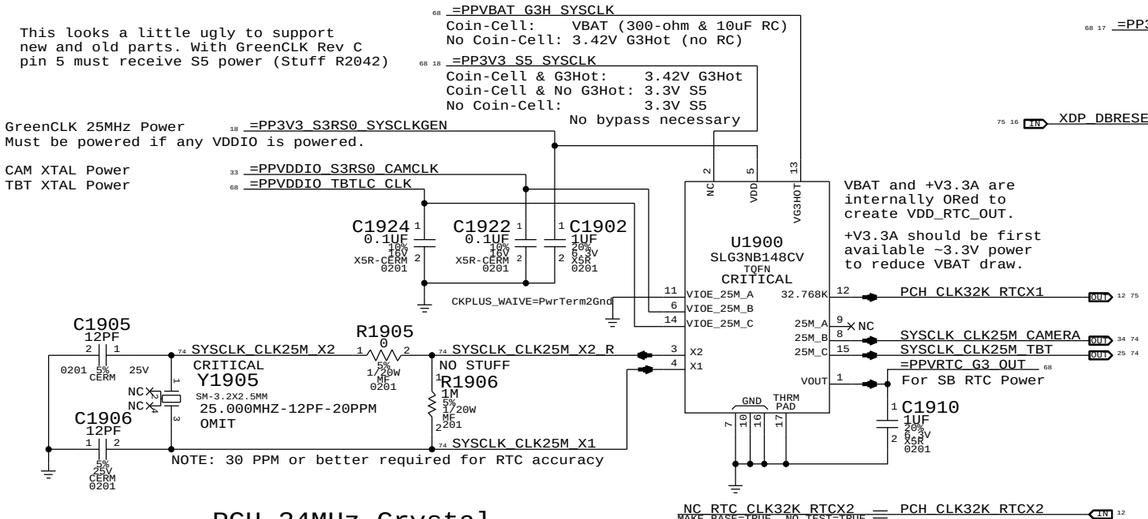
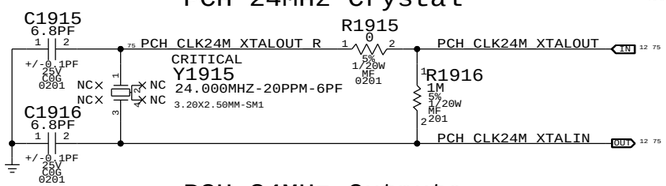
System RTC Power Source & 32kHz / 25MHz Clock Generator

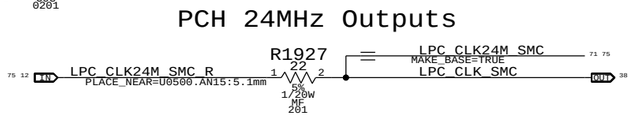
Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal



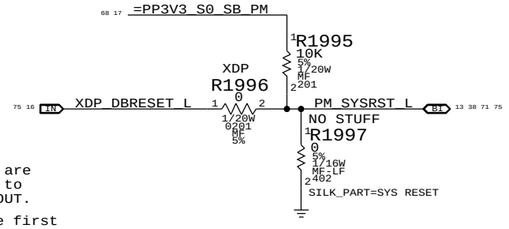
PCH 24MHz Crystal



PCH 24MHz Outputs

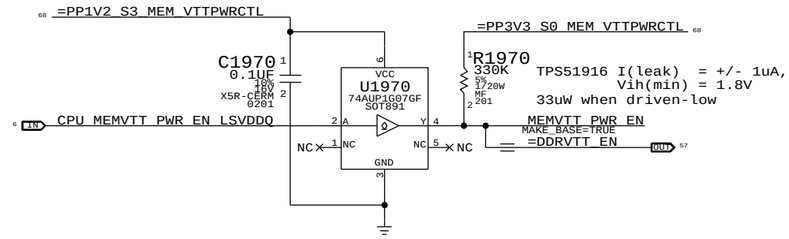


PCH Reset Button

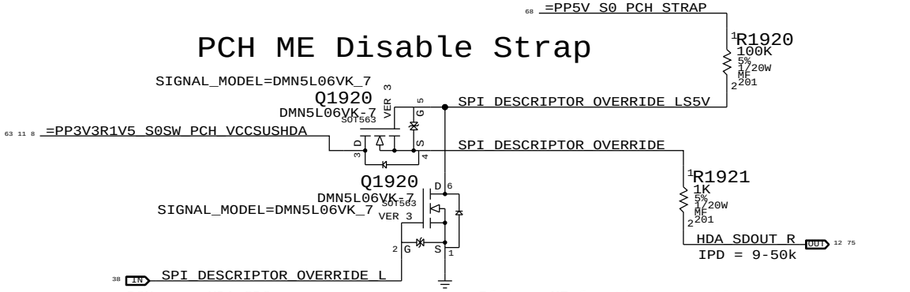


Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

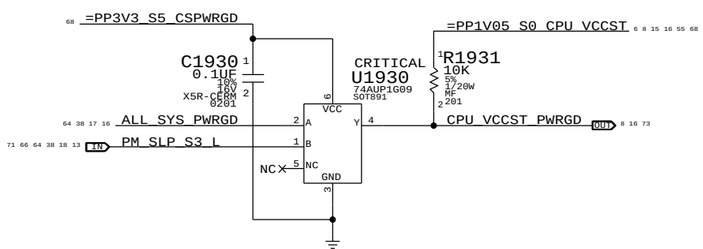


PCH ME Disable Strap

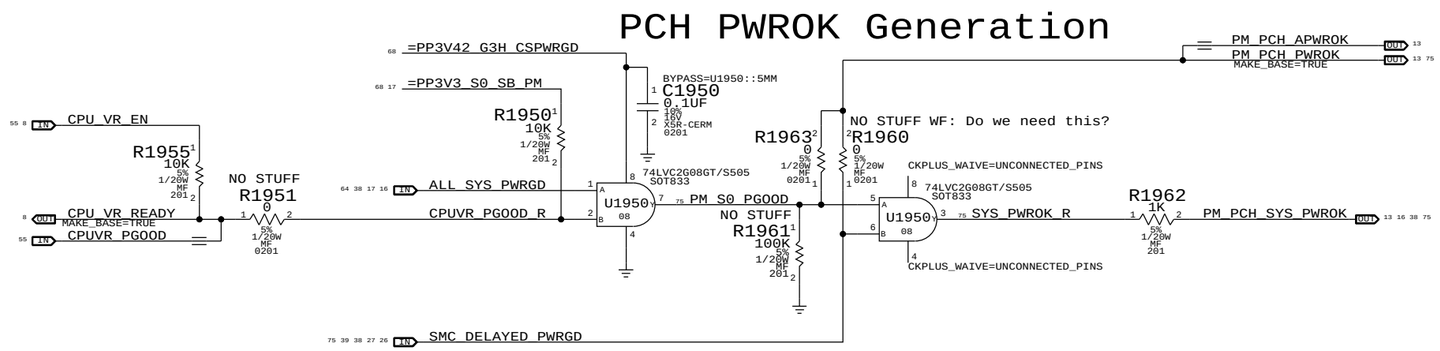


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

VCCST (1.05V S0) PWRGD



PCH PWROK Generation



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0480	1	XTAL,25MHZ,20PPM,12PF,3.2X2.5X.6MM,85C	Y1905		

BOM_COST_GROUP=CPU SUPPORT

SYNC_MASTER=J41 SYNC_DATE=01/30/2013

PAGE TITLE: Chipset Support

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

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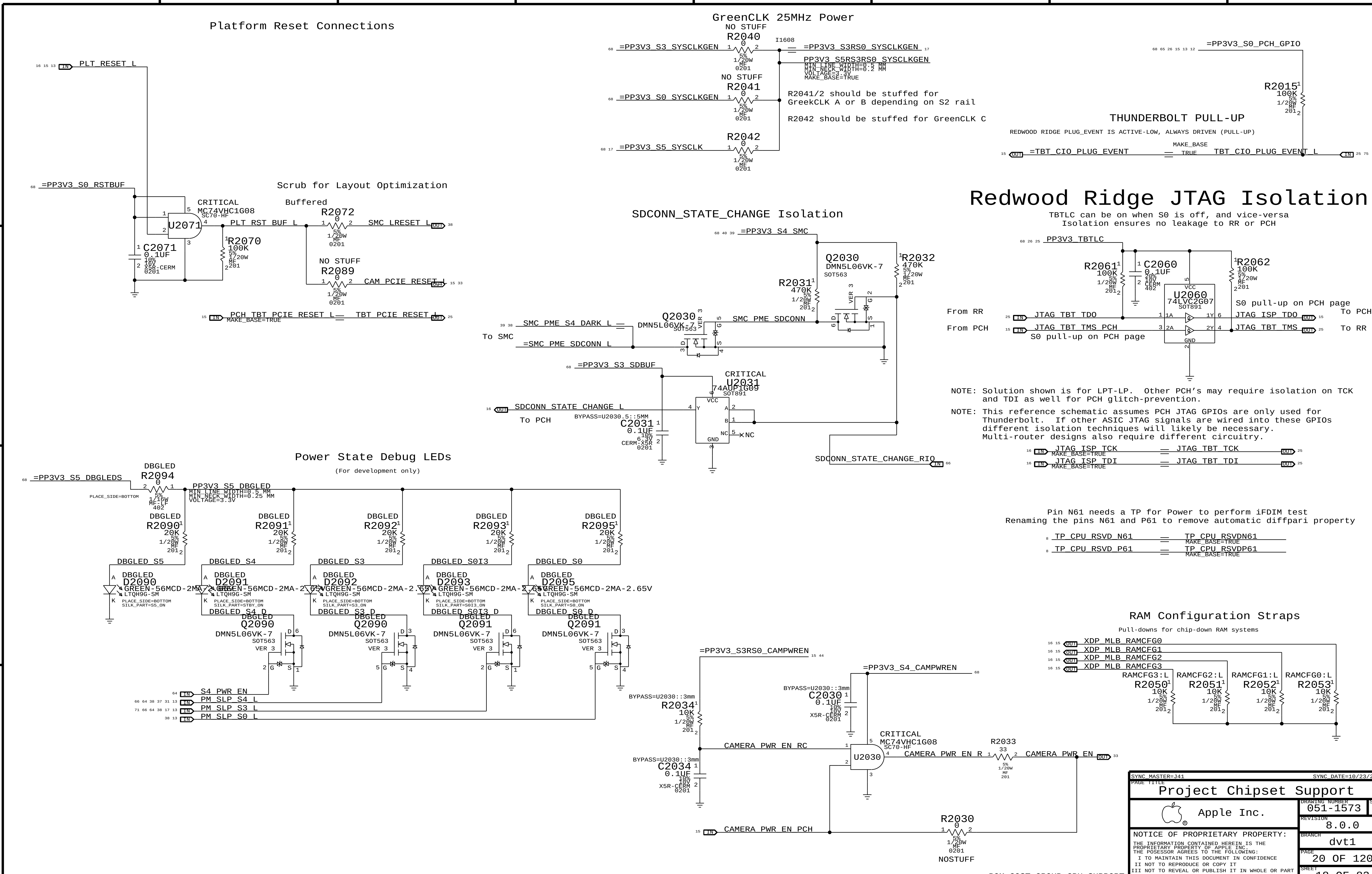

Platform Reset Connections
PLT_RESET_L
=PP3V3_S0_RSTBUF
CRITICAL
MC74VHC1G08
SC70-HF
U2071
C2071
0.1UF
R2070
100K
Scrub for Layout Optimization
Buffered
R2072
PLT_RST_BUF_L
SMC_LRESET_L
NO STUFF
R2089
CAM_PCIE_RESET_L
PCH_TBT_PCIE_RESET_L
TBT_PCIE_RESET_L
MAKE_BASE=TRUE
GreenCLK 25MHz Power
NO STUFF
R2040
=PP3V3_S3_SYSCLKGEN
=PP3V3_S3RS0_SYSCLKGEN
PP3V3_S5RS3RS0_SYSCLKGEN
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
NO STUFF
R2041
=PP3V3_S0_SYSCLKGEN
R2041/2 should be stuffed for
GreekCLK A or B depending on S2 rail
R2042 should be stuffed for GreenCLK C
R2042
=PP3V3_S5_SYSCLK
SDCONN_STATE_CHANGE Isolation
=PP3V3_S4_SMC
Q2030
DMN5L06VK-7
SOT563
R2032
470K
R2031
470K
SMC_PME_S4_DARK_L
SMC_PME_SDCONN
To SMC
=SMC_PME_SDCONN_L
=PP3V3_S3_SDBUF
CRITICAL
U2031
74AUP1G09
SOT891
SDCONN_STATE_CHANGE_L
To PCH
BYPASS=U2030.5::5MM
C2031
0.1UF
NC
SDCONN_STATE_CHANGE_RIO
=PP3V3_S0_PCH_GPIO
R2015
100K
THUNDERBOLT PULL-UP
REDWOOD RIDGE PLUG_EVENT IS ACTIVE-LOW, ALWAYS DRIVEN (PULL-UP)
=TBT_CIO_PLUG_EVENT
MAKE_BASE
TRUE
TBT_CIO_PLUG_EVENT_L
Redwood Ridge JTAG Isolation
TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
PP3V3_TBTLC
R2061
100K
C2060
0.1UF
R2062
100K
U2060
74LVC2G07
SOT891
S0 pull-up on PCH page
From RR
JTAG_TBT_TDO
JTAG_ISP_TDO
To PCH
From PCH
JTAG_TBT_TMS_PCH
JTAG_TBT_TMS
To RR
S0 pull-up on PCH page
NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.
NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary. Multi-router designs also require different circuitry.
JTAG_ISP_TCK
JTAG_TBT_TCK
JTAG_ISP_TDI
JTAG_TBT_TDI
Power State Debug LEDs
(For development only)
=PP3V3_S5_DBGLEDS
DBGLED
R2094
PLACE_SIDE=BOTTOM
PP3V3_S5_DBGLED
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=3.3V
R2090
R2091
R2092
R2093
R2095
20K
DBGLED_S5
DBGLED_S4
DBGLED_S3
DBGLED_S0I3
DBGLED_S0
D2090
D2091
D2092
D2093
D2095
GREEN-56MCD-2MA-2.65V
LTQH9G-SM
DBGLED_S4_D
DBGLED_S3_D
DBGLED_S0I3_D
DBGLED_S0_D
Q2090
Q2091
DMN5L06VK-7
SOT563
S4_PWR_EN
PM_SLP_S4_L
PM_SLP_S3_L
PM_SLP_S0_L
Pin N61 needs a TP for Power to perform iFDIM test
Renaming the pins N61 and P61 to remove automatic diffpari property
TP_CPU_RSVD_N61
TP_CPU_RSVDN61
TP_CPU_RSVD_P61
TP_CPU_RSVDP61
MAKE_BASE=TRUE
RAM Configuration Straps
Pull-downs for chip-down RAM systems
XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3
RAMCFG3:L
RAMCFG2:L
RAMCFG1:L
RAMCFG0:L
R2050
R2051
R2052
R2053
10K
=PP3V3_S3RS0_CAMPWREN
=PP3V3_S4_CAMPWREN
BYPASS=U2030::3mm
C2030
0.1UF
R2034
10K
CAMERA_PWR_EN_RC
CRITICAL
MC74VHC1G08
SC70-HF
U2030
CAMERA_PWR_EN_R
R2033
33
CAMERA_PWR_EN
C2034
0.1UF
CAMERA_PWR_EN_PCH
R2030
NOSTUFF
BOM_COST_GROUP=CPU SUPPORT

SYNC_MASTER=J41 SYNC_DATE=10/23/2012

PAGE TITLE: Project Chipset Support

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

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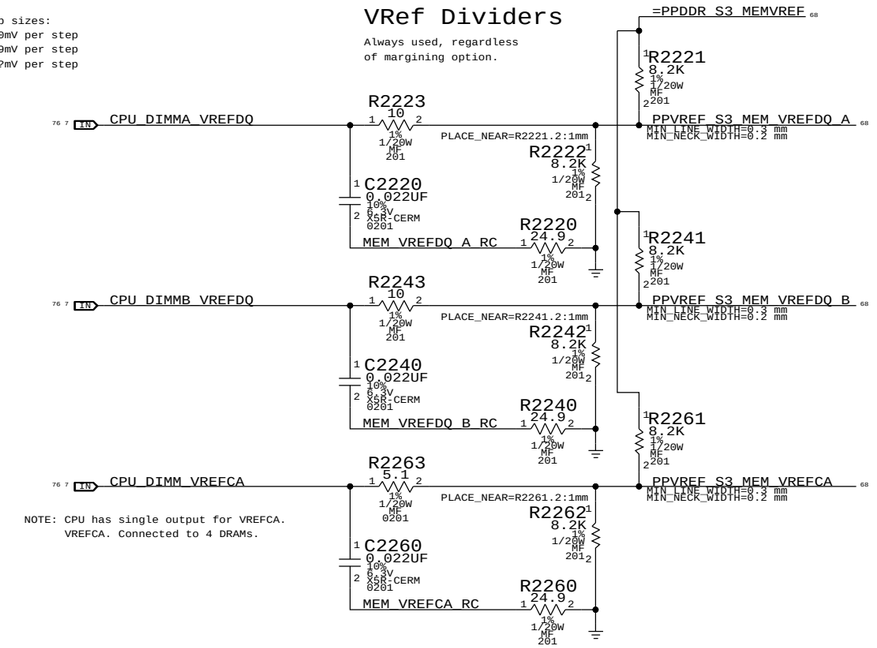
CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

VRef Dividers

Always used, regardless of margining option.



NOTE: CPU has single output for VREFCA. VREFCA. Connected to 4 DRAMs.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output	3.53mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

BOM_COST_GROUP=CPU SUPPORT

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/02/2013

PAGE TITLE: LPDDR3 VREF Margining

Apple Inc.

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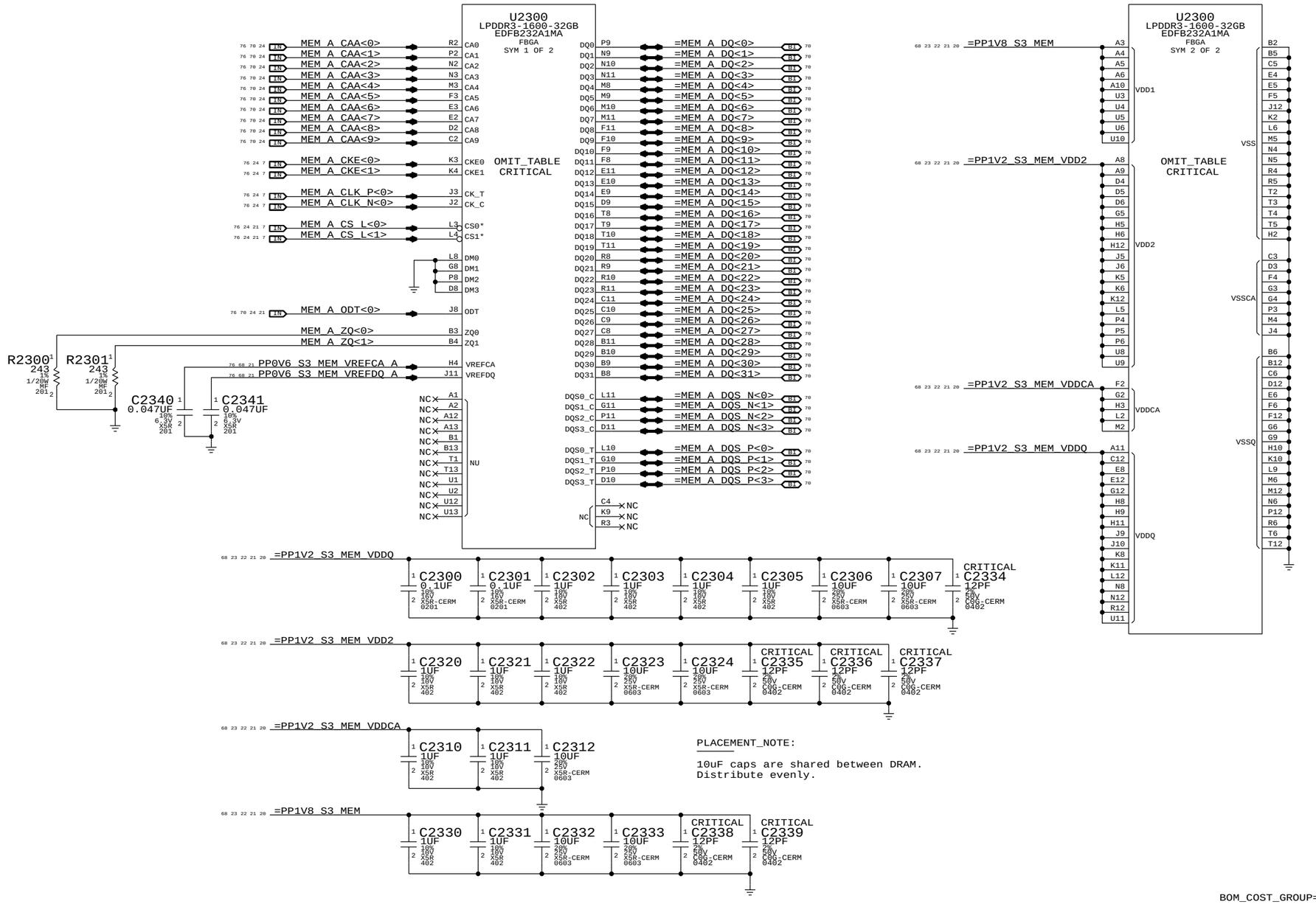
LPDDR3 CHANNEL A (0-31)



SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
LPDDR3 DRAM Channel A (00-31)

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
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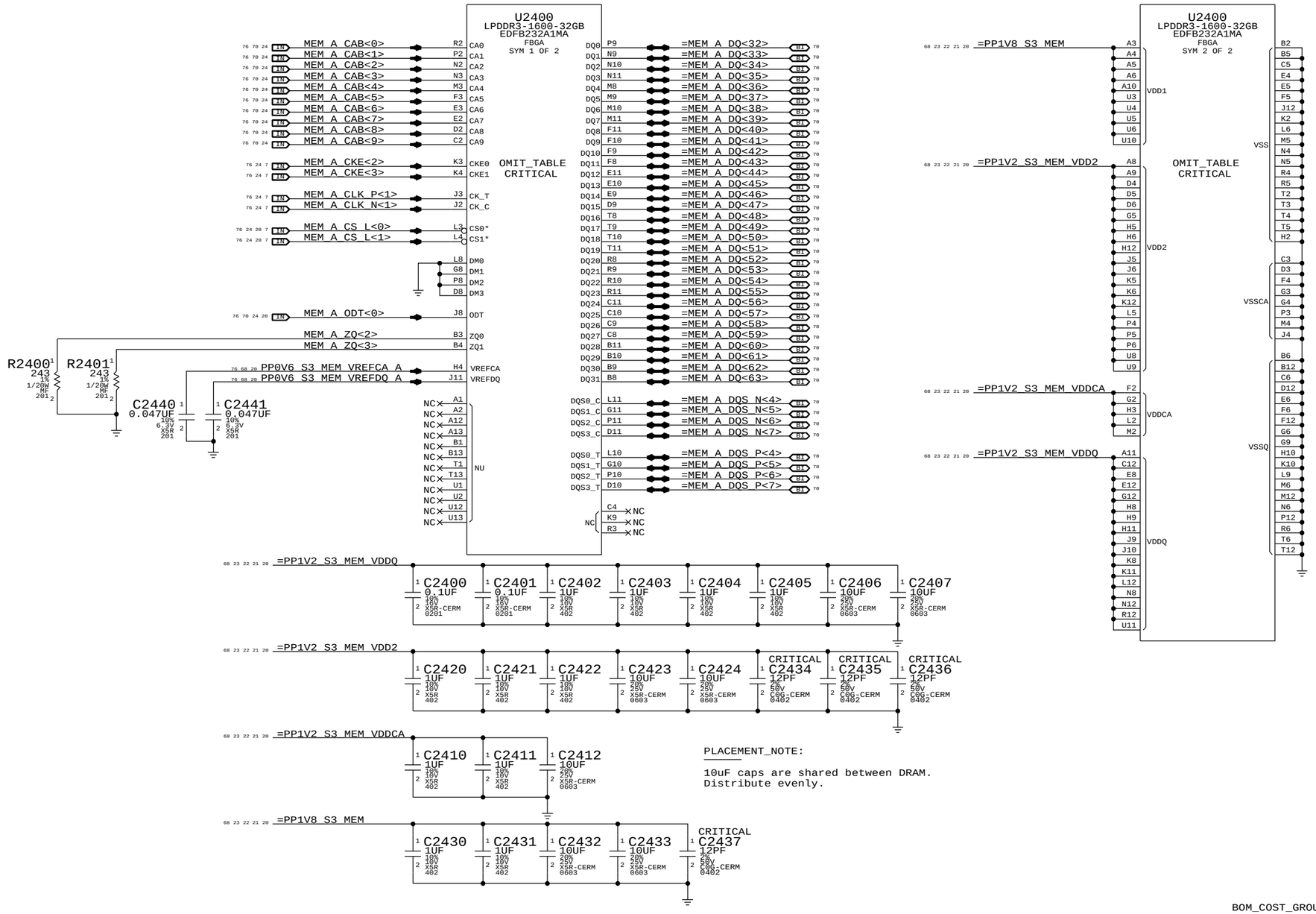
SHEET 20 OF 82

LPDDR3 CHANNEL A (32-63)



BOM_COST_GROUP=DRAM

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: LPDDR3 DRAM Channel A (32-63)

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

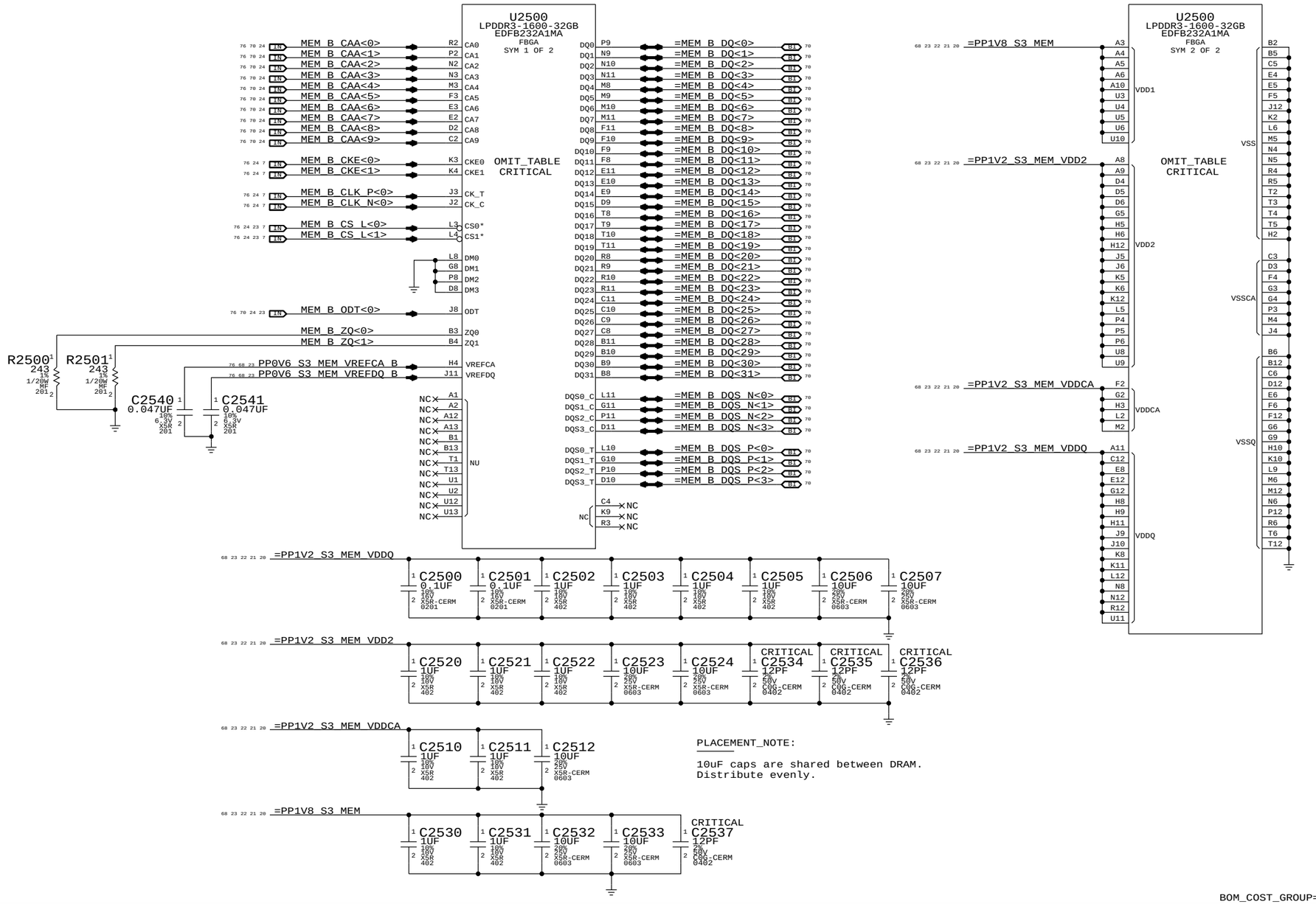
REVISION: 8.0.0

BRANCH: dvt1

PAGE: 24 OF 120

SHEET: 21 OF 82

LPDDR3 CHANNEL B (0-31)



BOM_COST_GROUP=DRAM

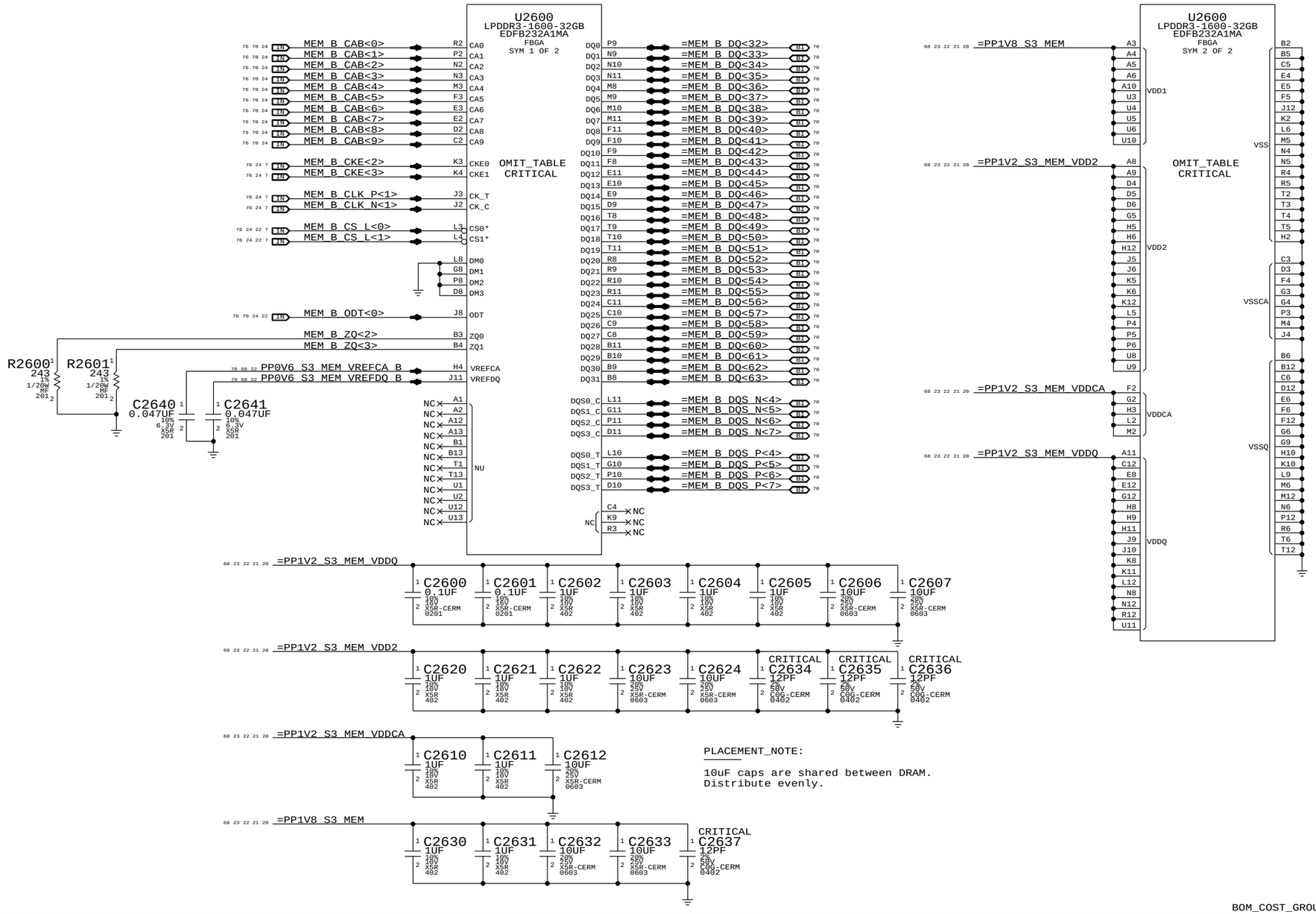
SYNC_MASTER=J41 MLB SYNC_DATE=02/06/2013

PAGE TITLE
LPDDR3 DRAM Channel B (00-31)

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
PAGE 25 OF 120
SHEET 22 OF 82

LPDDR3 CHANNEL B (32-63)



BOM_COST_GROUP=DRAM

SYNC_MASTER=J41 MLB	SYNC_DATE=02/06/2013
PAGE TITLE: LPDDR3 DRAM Channel B (32-63)	
Apple Inc.	DRAWING NUMBER: 051-1573 SIZE: D
	REVISION: 8.0.0
	BRANCH: dvt1
	PAGE: 26 OF 120
	SHEET: 23 OF 82

Intel recommends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

68 =PP0V6_S0_MEM_VTT_A

76 70 20	MEM_A_CAA<9>	R2700	56	1% 1/20W 201 MF	
76 70 20	MEM_A_CAA<8>	R2701	56	1% 1/20W 201 MF	
76 70 20	MEM_A_CAA<6>	R2702	56	1% 1/20W 201 MF	
76 70 20	MEM_A_CAA<7>	R2703	56	1% 1/20W 201 MF	
76 70 20	MEM_A_CAA<5>	R2704	56	1% 1/20W 201 MF	
76 20 7	MEM_A_CLK_P<0>	R2705	39	1% 1/20W 201 MF	
76 20 7	MEM_A_CLK_N<0>	R2706	39	1% 1/20W 201 MF	
76 20 7	MEM_A_CKE<1>	R2707	82	1% 1/20W 201 MF	
76 20 7	MEM_A_CKE<0>	R2708	82	1% 1/20W 201 MF	
76 70 20	MEM_A_CAA<4>	R2709	56	1% 1/20W 201 MF	
76 70 20	MEM_A_CAA<3>	R2710	56	1% 1/20W 201 MF	
76 70 20	MEM_A_CAA<2>	R2711	56	1% 1/20W 201 MF	
76 70 20	MEM_A_CAA<1>	R2712	56	1% 1/20W 201 MF	
76 70 20	MEM_A_CAA<0>	R2713	56	1% 1/20W 201 MF	
76 70 21	MEM_A_CAB<9>	R2714	56	1% 1/20W 201 MF	
76 70 21	MEM_A_CAB<8>	R2715	56	1% 1/20W 201 MF	
76 70 21	MEM_A_CAB<6>	R2716	56	1% 1/20W 201 MF	
76 70 21	MEM_A_CAB<7>	R2717	56	1% 1/20W 201 MF	
76 70 21	MEM_A_CAB<5>	R2718	56	1% 1/20W 201 MF	
76 21 7	MEM_A_CLK_P<1>	R2719	39	1% 1/20W 201 MF	
76 21 7	MEM_A_CLK_N<1>	R2720	39	1% 1/20W 201 MF	
76 21 7	MEM_A_CKE<2>	R2721	82	1% 1/20W 201 MF	
76 21 7	MEM_A_CKE<3>	R2722	82	1% 1/20W 201 MF	
76 70 21	MEM_A_CAB<4>	R2723	56	1% 1/20W 201 MF	
76 70 21	MEM_A_CAB<2>	R2724	56	1% 1/20W 201 MF	
76 70 21	MEM_A_CAB<3>	R2725	56	1% 1/20W 201 MF	
76 70 21	MEM_A_CAB<1>	R2726	56	1% 1/20W 201 MF	
76 70 21	MEM_A_CAB<0>	R2727	56	1% 1/20W 201 MF	
76 21 20 7	MEM_A_CS_L<0>	R2728	82	1% 1/20W 201 MF	
76 21 20 7	MEM_A_CS_L<1>	R2729	82	1% 1/20W 201 MF	
76 70 21 20	MEM_A_ODT<0>	R2730	82	1% 1/20W 201 MF	

C2700 0.47UF 20% 4V CERM-X5R-1 201
C2730 12PF 5% 25V NP0-C0G 0201
C2701 0.47UF 20% 4V CERM-X5R-1 201
C2702 0.47UF 20% 4V CERM-X5R-1 201
C2703 0.47UF 20% 4V CERM-X5R-1 201
C2704 0.47UF 20% 4V CERM-X5R-1 201
C2705 0.47UF 20% 4V CERM-X5R-1 201
C2706 0.47UF 20% 4V CERM-X5R-1 201
C2707 0.47UF 20% 4V CERM-X5R-1 201
C2708 0.47UF 20% 4V CERM-X5R-1 201
C2709 0.47UF 20% 4V CERM-X5R-1 201
CRITICAL
C2720 22UF 20% 6.3V X6S-CERM-1 603

68 =PP0V6_S0_MEM_VTT_B

76 70 22	MEM_B_CAA<9>	R2740	56	1% 1/20W 201 MF	
76 70 22	MEM_B_CAA<8>	R2741	56	1% 1/20W 201 MF	
76 70 22	MEM_B_CAA<7>	R2742	56	1% 1/20W 201 MF	
76 70 22	MEM_B_CAA<6>	R2743	56	1% 1/20W 201 MF	
76 70 22	MEM_B_CAA<5>	R2744	56	1% 1/20W 201 MF	
76 22 7	MEM_B_CLK_P<0>	R2745	39	1% 1/20W 201 MF	
76 22 7	MEM_B_CLK_N<0>	R2746	39	1% 1/20W 201 MF	
76 22 7	MEM_B_CKE<1>	R2747	82	1% 1/20W 201 MF	
76 22 7	MEM_B_CKE<0>	R2748	82	1% 1/20W 201 MF	
76 70 22	MEM_B_CAA<4>	R2749	56	1% 1/20W 201 MF	
76 70 22	MEM_B_CAA<2>	R2750	56	1% 1/20W 201 MF	
76 70 22	MEM_B_CAA<3>	R2751	56	1% 1/20W 201 MF	
76 70 22	MEM_B_CAA<1>	R2752	56	1% 1/20W 201 MF	
76 70 22	MEM_B_CAA<0>	R2753	56	1% 1/20W 201 MF	
76 70 23	MEM_B_CAB<9>	R2754	56	1% 1/20W 201 MF	
76 70 23	MEM_B_CAB<8>	R2755	56	1% 1/20W 201 MF	
76 70 23	MEM_B_CAB<7>	R2756	56	1% 1/20W 201 MF	
76 70 23	MEM_B_CAB<6>	R2757	56	1% 1/20W 201 MF	
76 70 23	MEM_B_CAB<5>	R2758	56	1% 1/20W 201 MF	
76 23 7	MEM_B_CLK_N<1>	R2759	39	1% 1/20W 201 MF	
76 23 7	MEM_B_CLK_P<1>	R2760	39	1% 1/20W 201 MF	
76 23 7	MEM_B_CKE<2>	R2761	82	1% 1/20W 201 MF	
76 23 7	MEM_B_CKE<3>	R2762	82	1% 1/20W 201 MF	
76 70 23	MEM_B_CAB<4>	R2763	56	1% 1/20W 201 MF	
76 70 23	MEM_B_CAB<2>	R2764	56	1% 1/20W 201 MF	
76 70 23	MEM_B_CAB<3>	R2765	56	1% 1/20W 201 MF	
76 70 23	MEM_B_CAB<1>	R2766	56	1% 1/20W 201 MF	
76 70 23	MEM_B_CAB<0>	R2767	56	1% 1/20W 201 MF	
76 23 22 7	MEM_B_CS_L<0>	R2768	82	1% 1/20W 201 MF	
76 23 22 7	MEM_B_CS_L<1>	R2769	82	1% 1/20W 201 MF	
76 70 23 22	MEM_B_ODT<0>	R2770	82	1% 1/20W 201 MF	

C2710 0.47UF 20% 4V CERM-X5R-1 201
C2731 12PF 5% 25V NP0-C0G 0201
C2711 0.47UF 20% 4V CERM-X5R-1 201
C2712 0.47UF 20% 4V CERM-X5R-1 201
C2713 0.47UF 20% 4V CERM-X5R-1 201
C2714 0.47UF 20% 4V CERM-X5R-1 201
C2715 0.47UF 20% 4V CERM-X5R-1 201
C2716 0.47UF 20% 4V CERM-X5R-1 201
C2717 0.47UF 20% 4V CERM-X5R-1 201
C2718 0.47UF 20% 4V CERM-X5R-1 201
C2719 0.47UF 20% 4V CERM-X5R-1 201
CRITICAL
C2740 22UF 20% 6.3V X6S-CERM-1 603

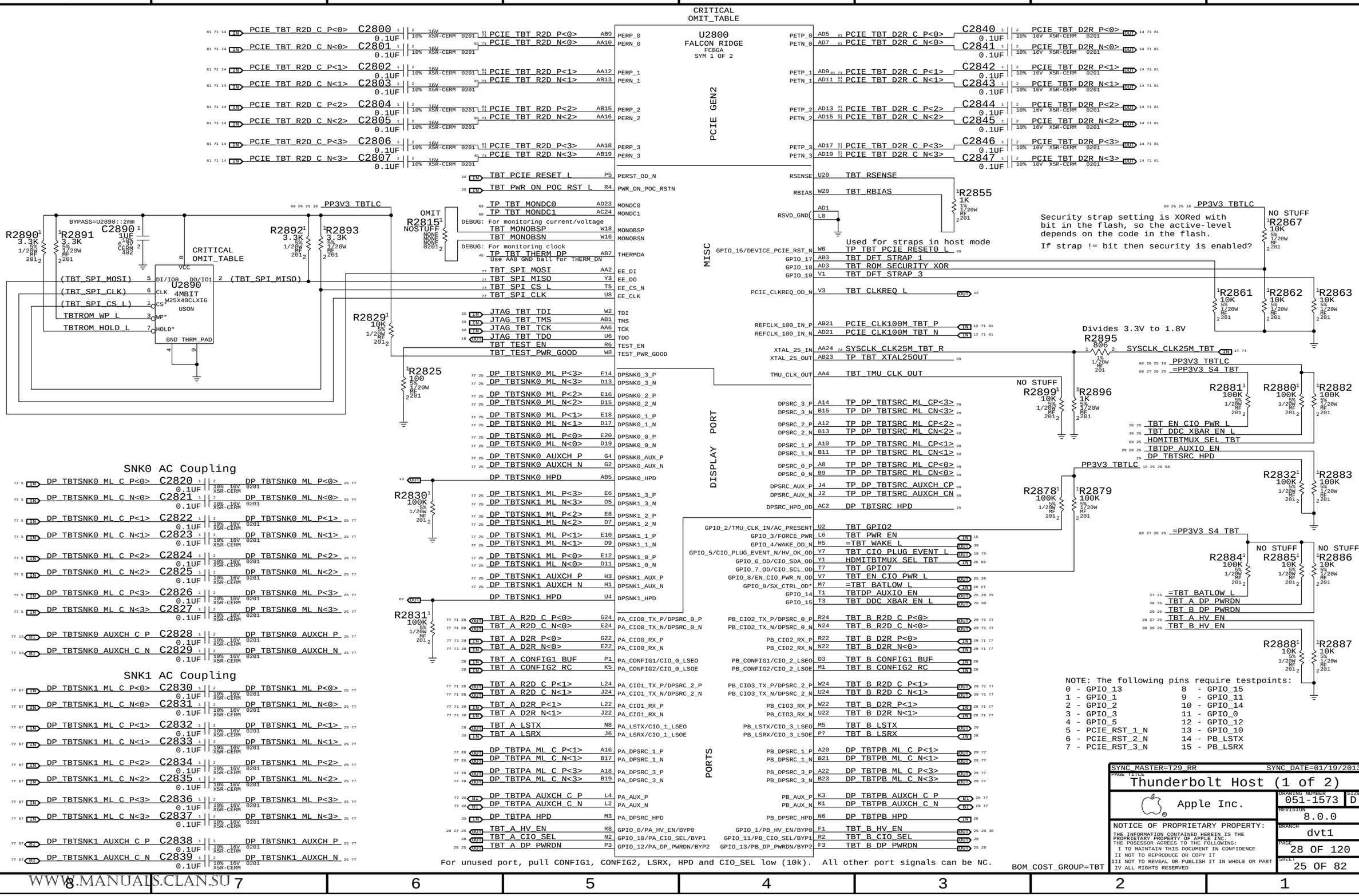
BOM_COST_GROUP=DRAM

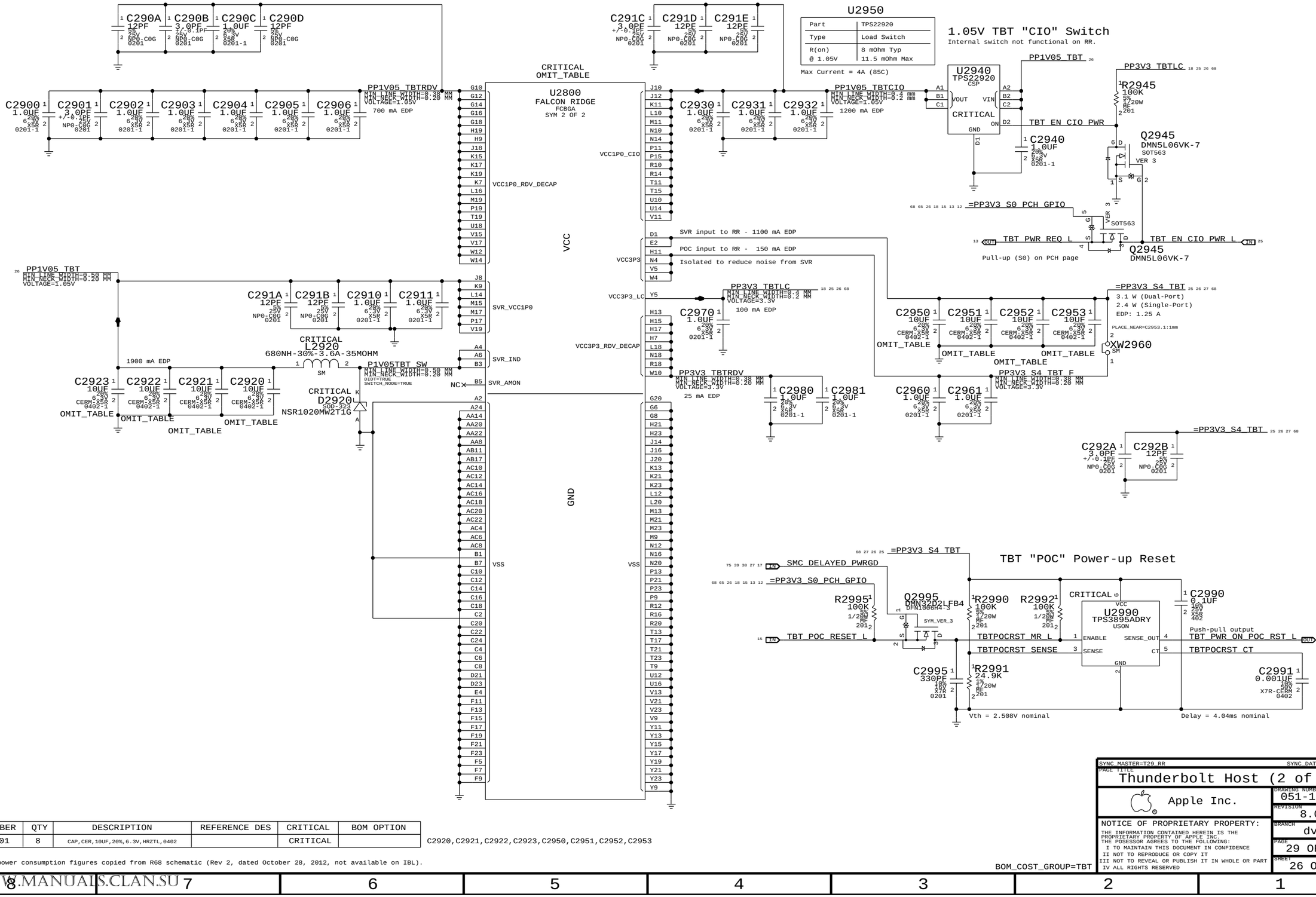
SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE
LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
PAGE 27 OF 120
SHEET 24 OF 82





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	8	CAP,CER,10UF,20%,6.3V,HRZTL,0402		CRITICAL	

C2920,C2921,C2922,C2923,C2950,C2951,C2952,C2953

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

BOM_COST_GROUP=TBT

SYNC MASTER=T29_RR SYNC DATE=12/17/2012

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 29 OF 120

SHEET: 26 OF 82

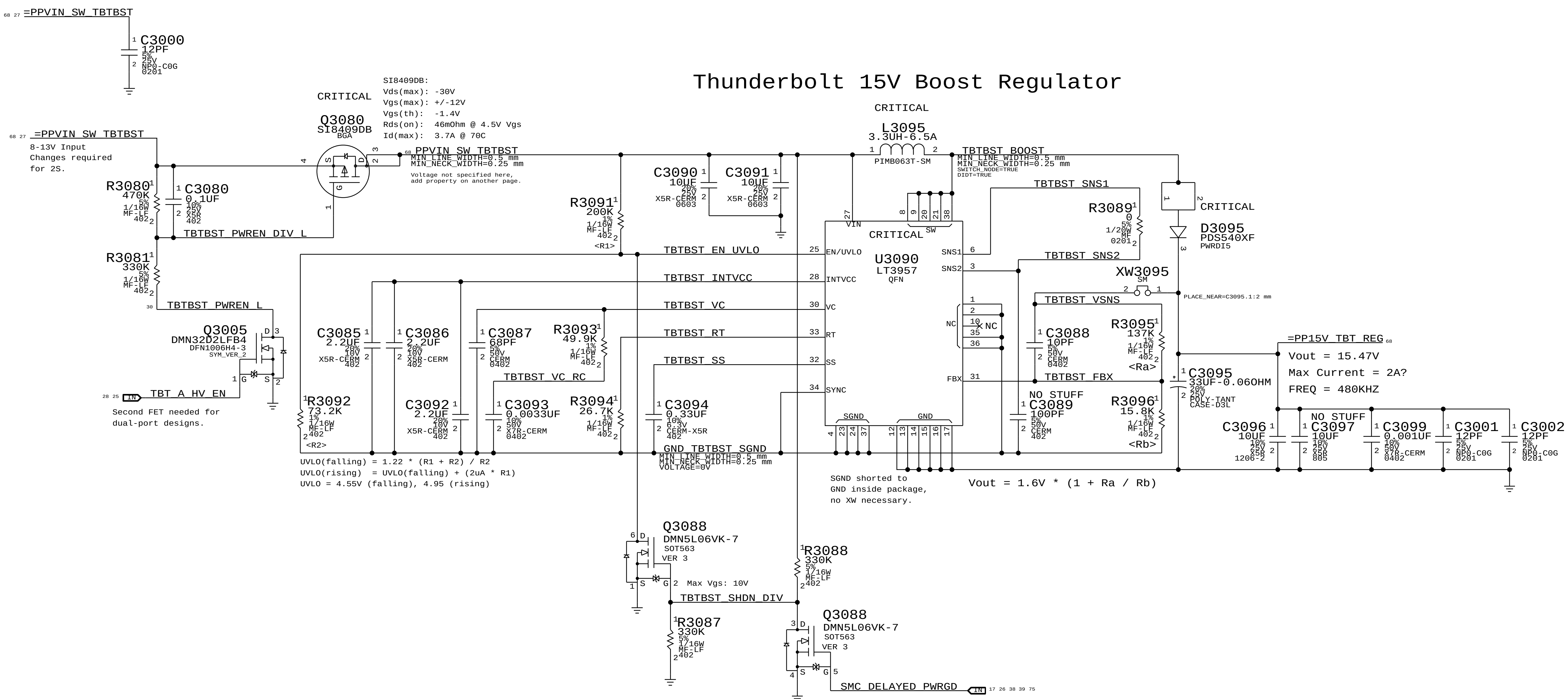
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

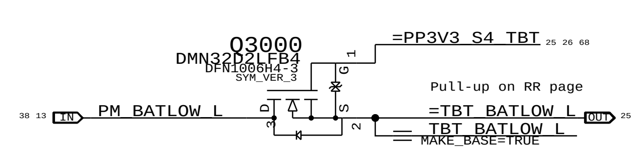
BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator



=PPVIN_SW_TBTBST
C3000 12PF
8-13V Input Changes required for 2S.
CRITICAL
Q3080 SI8409DB BGA
SI8409DB: Vds(max): -30V Vgs(max): +/-12V Vgs(th): -1.4V Rds(on): 46mOhm @ 4.5V Vgs Id(max): 3.7A @ 70C
PPVIN_SW_TBTBST MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.
R3080 470K
C3080 0.1UF
TBTBST_PWREN_DIV_L
R3081 330K
TBTBST_PWREN_L
Q3005 DMN32D2LFB4 DFN1006H4-3
TBT_A_HV_EN
Second FET needed for dual-port designs.
CRITICAL
L3095 3.3UH-6.5A PIMB063T-SM
TBTBST_BOOST
C3090 10UF
C3091 10UF
R3091 200K
TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
CRITICAL
U3090 LT3957 QFN
TBTBST_SNS1
TBTBST_SNS2
TBTBST_VSNS
TBTBST_FBX
R3089 0
CRITICAL
D3095 PDS540XF PWRDI5
XW3095 SM
PLACE_NEAR=C3095.1:2 mm
C3085 2.2UF
C3086 2.2UF
C3087 68PF
R3093 49.9K
TBTBST_VC_RC
C3088 10PF
R3095 137K <Ra>
C3095 33UF-0.060OHM POLY-TANT CASE-D3L
=PP15V_TBT_REG
Vout = 15.47V
Max Current = 2A?
FREQ = 480KHZ
R3092 73.2K <R2>
C3092 2.2UF
C3093 0.0033UF
R3094 26.7K
C3094 0.33UF
GND_TBTBST_SGND MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=0V
NO STUFF
C3089 100PF
R3096 15.8K <Rb>
C3096 10UF
NO STUFF
C3097 10UF
C3099 0.001UF
C3001 12PF
C3002 12PF
UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)
SGND shorted to GND inside package, no XW necessary.
Vout = 1.6V * (1 + Ra / Rb)
Q3088 DMN5L06VK-7 SOT563 VER 3
Max Vgs: 10V
R3088 330K
TBTBST_SHDN_DIV
R3087 330K
Q3088 DMN5L06VK-7 SOT563 VER 3
SMC_DELAYED_PWRGD

BATLOW# Isolation



BOM_COST_GROUP=TBT

SYNC_MASTER=T29_RR SYNC_DATE=11/19/2012

PAGE TITLE: Thunderbolt Mobile Support

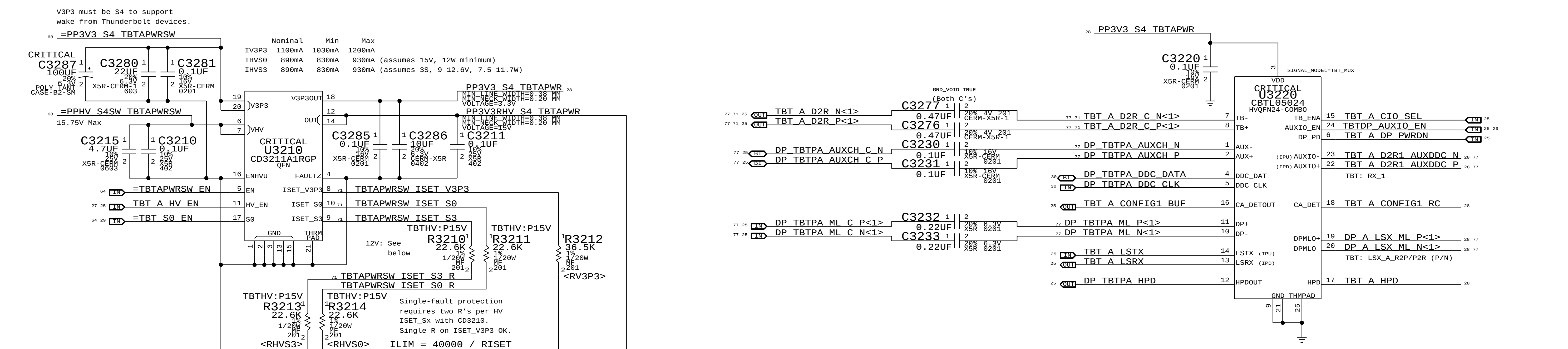
Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

3.3V/HV Power MUX



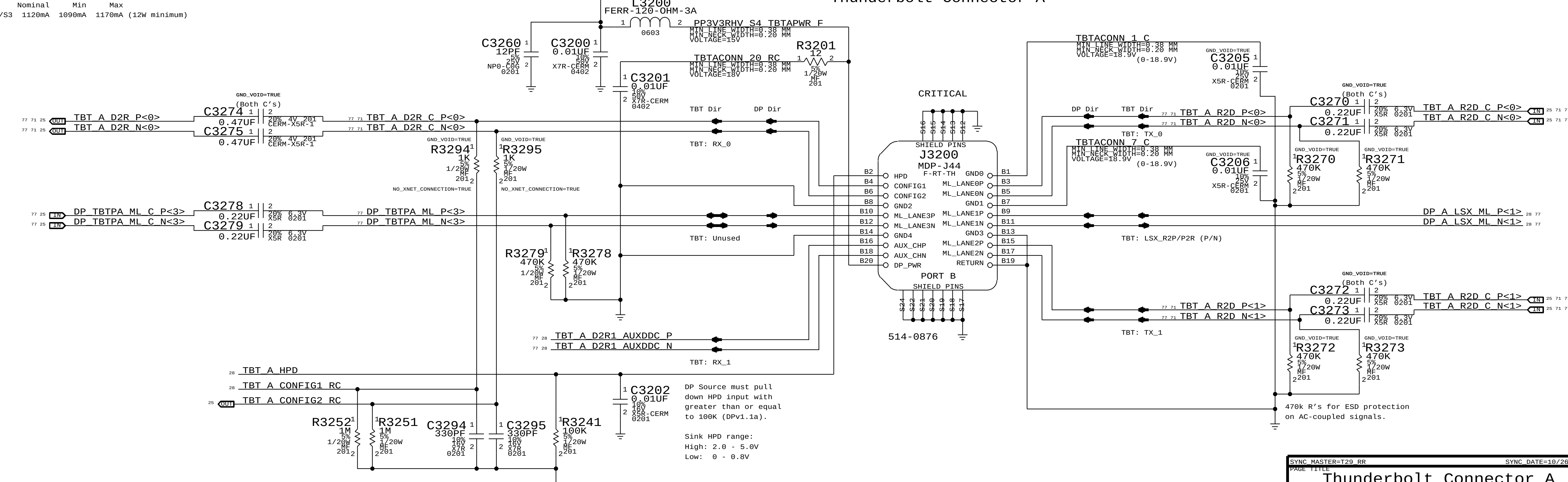
V3P3 must be S4 to support
wake from Thunderbolt devices.
=PP3V3_S4_TBTAPWRSW
Nominal Min Max
IV3P3 1100mA 1030mA 1200mA
IHVS0 890mA 830mA 930mA (assumes 15V, 12W minimum)
IHVS3 890mA 830mA 930mA (assumes 3S, 9-12.6V, 7.5-11.7W)
CRITICAL
C3287
C3280
C3281
=PPHV_S4SW_TBTAPWRSW
15.75V Max
C3215
C3210
CRITICAL
U3210
CD3211A1RGP
PP3V3_S4_TBTAPWR
PP3V3RHV_S4_TBTAPWR
C3285
C3286
C3211
=TBTAPWRSW_EN
=TBT_A_HV_EN
=TBT_S0_EN
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTHV:P15V
R3210
R3211
R3212
12V: See below
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R3213
R3214
<RHVS3>
<RHVS0>
<RV3P3>
Single-fault protection
requires two R's per HV
ISET_Sx with CD3210.
Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET
PP3V3_S4_TBTAPWR
C3220
CRITICAL
U3220
CBTL05024
HVQFN24-COMBO
SIGNAL_MODEL=TBT_MUX
TBT_A_D2R_N<1>
TBT_A_D2R_P<1>
C3277
C3276
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
C3230
C3231
TBT_A_D2R_C_N<1>
TBT_A_D2R_C_P<1>
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
C3232
C3233
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_HPD
TBT_A_CIO_SEL
TBTDP_AUXIO_EN
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R1_AUXDDC_P
TBT: RX_1
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)

Thunderbolt Connector A



CRITICAL
L3200
FERR-120-OHM-3A
PP3V3RHV_S4_TBTAPWR_F
C3260
C3200
C3201
TBTACONN_20_RC
R3201
TBTACONN_1_C
C3205
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
C3274
C3275
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
TBT Dir
DP Dir
TBT: RX_0
R3294
R3295
CRITICAL
J3200
MDP-J44
F-RT-TH
PORT B
514-0876
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT: TX_0
C3270
C3271
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBTACONN_7_C
C3206
R3270
R3271
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
C3278
C3279
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>
TBT: Unused
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)
R3279
R3278
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
C3272
C3273
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
TBT: TX_1
R3272
R3273
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
TBT: RX_1
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
C3202
DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
R3252
R3251
C3294
C3295
R3241
470k R's for ESD protection
on AC-coupled signals.

SYNC_MASTER=T29_RR SYNC_DATE=10/26/2012

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

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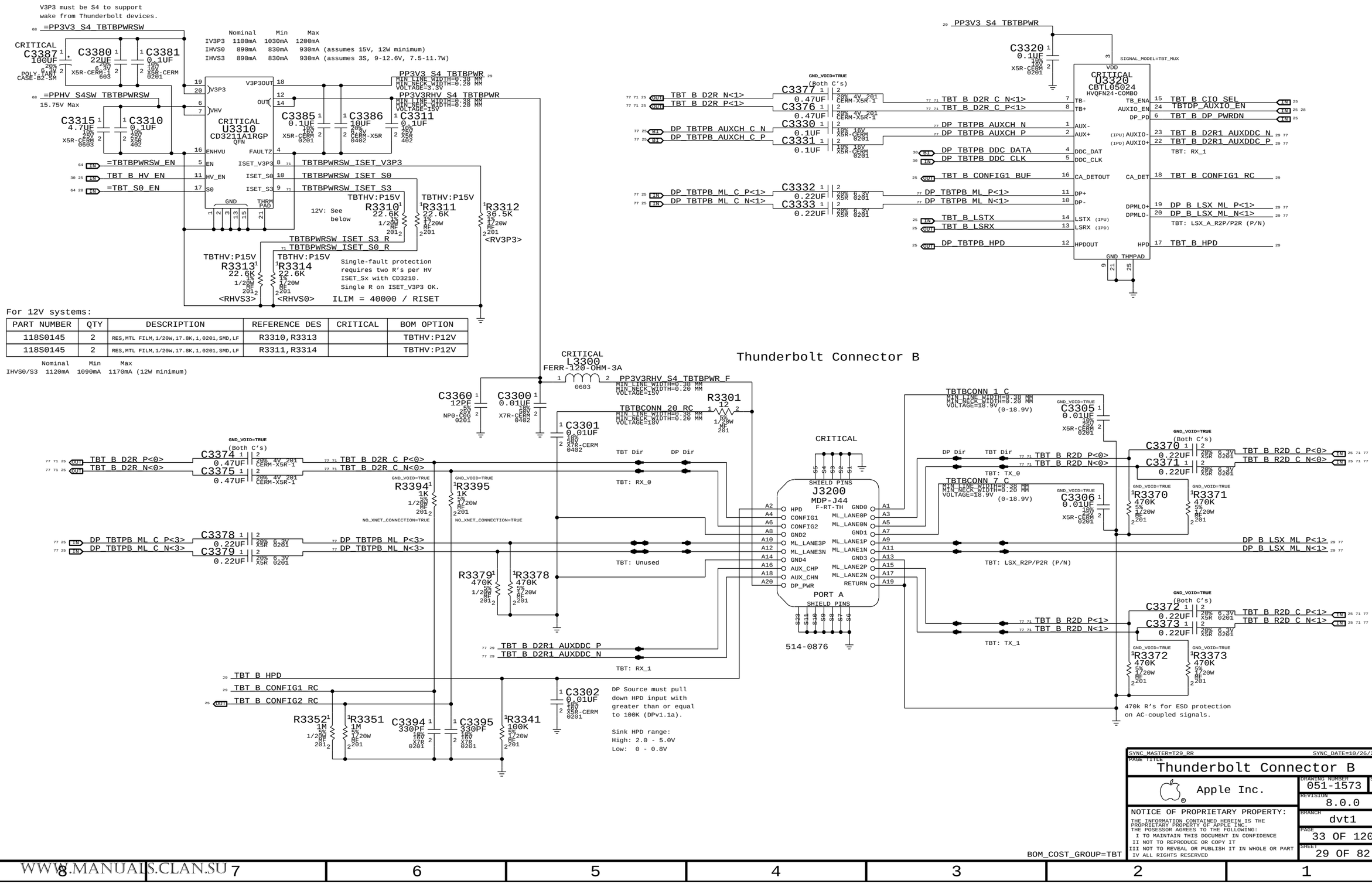
SHEET: 28 OF 82

BOM_COST_GROUP=TBT



DDC Pull-Ups

2.2k pull-ups are required by PCH
to indicate active display interface.

DP++ spec violation, should remove!

NOTE: Only DDC_DATA is sensed, so DDC_CLK
pull-ups are unstuffed.

DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!

68 =PP3V3_S0_DDCMUX

R3451 2.2K 1% 1/20W MF 201
R3452 2.2K 1% 1/20W MF 201
R3453 2.2K 1% 1/20W MF 201
R3454 2.2K 1% 1/20W MF 201

R3485 100K 5% 1/20W MF 201

C3480 0.1UF 20% 10V CERM 402

U3400
TS3DS10224
QFN
CRITICAL

		13	VCC
	ENA	16	
28 OUT DP_TBTPA_DDC_CLK	INA+	1	
28 BI DP_TBTPA_DDC_DATA	INA-	2	
	SAI	14	
	ENB	10	
29 OUT DP_TBTPB_DDC_CLK	INB+	3	
29 BI DP_TBTPB_DDC_DATA	INB-	4	
TBT_DDC_XBAR_EN	SBI	12	
	GND	5	
	THRM PAD	21	
	OUTA1+	20	
	OUTA1-	19	
	OUTA0+	18	DP_TBTSNK1_DDC_CLK IN 67
	OUTA0-	17	DP_TBTSNK1_DDC_DATA BI 67
	SAO	15	
	OUTB1+	6	
	OUTB1-	7	
	OUTB0+	8	DP_TBTSNK0_DDC_CLK IN 13
	OUTB0-	9	DP_TBTSNK0_DDC_DATA BI 13
	SBO	11	

SAI/SBI = 1: INA == OUTA0, INB == OUTB0
SAI/SBI = 0: INA == OUTB0, INB == OUTA0

Q3485
DMN5L06VK-7
SOT563
VER 3

TBT_DDC_XBAR_EN
25 IN TBT_DDC_XBAR_EN_L

Second FET needed for
dual-port designs.
CONNECTS TO TBTBTS_PWREN_L ON PAGE 30.

Q3485
DMN5L06VK-7
SOT563
VER 3

TBTBST_PWREN_L OUT 27
29 25 IN TBT_B_HV_EN

BOM_COST_GROUP=TBT

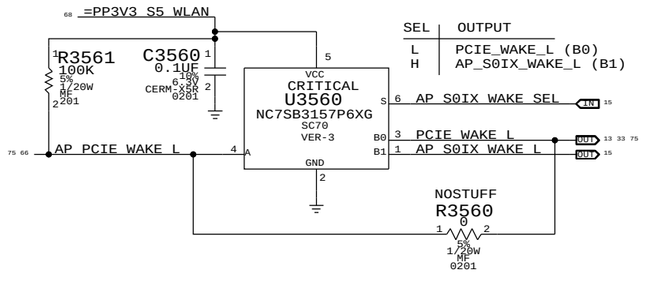
SYNC_MASTER=J14 SYNC_DATE=10/23/2012

PAGE TITLE: DDC Crossbar

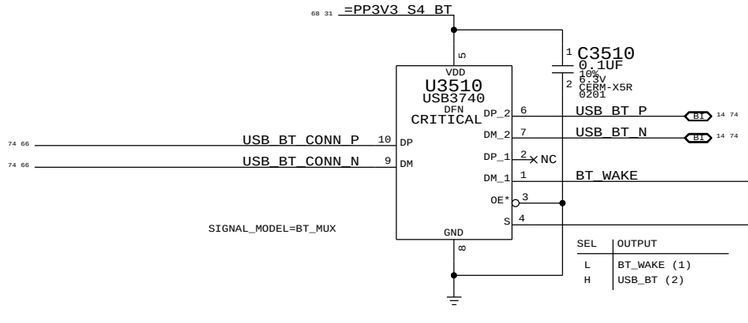
Apple Inc.

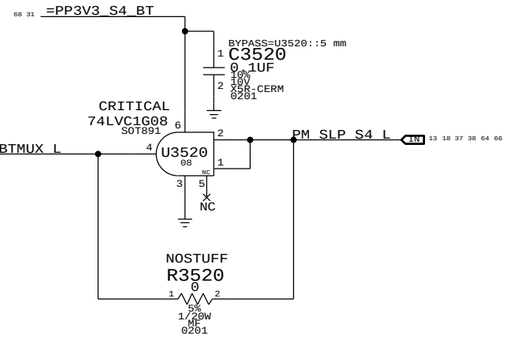
DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
PAGE 34 OF 120
SHEET 30 OF 82

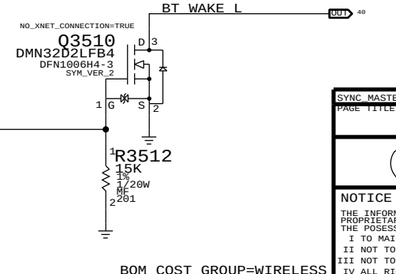
PCIe Wake Muxing



BLUETOOTH







BOM_COST_GROUP=WIRELESS

SYNC_MASTER=J41 SYNC_DATE=11/01/2012

PAGE TITLE: Wireless Support

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

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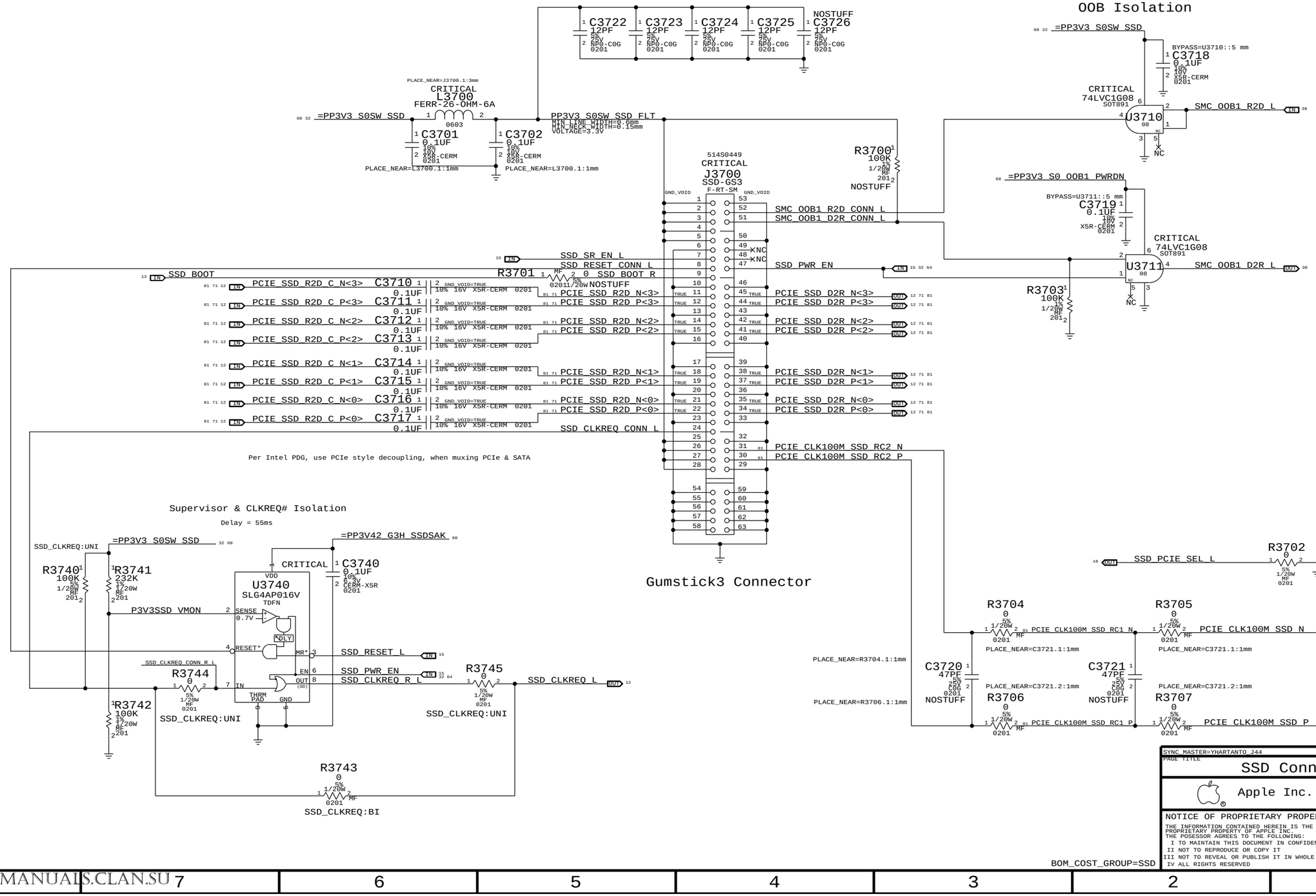
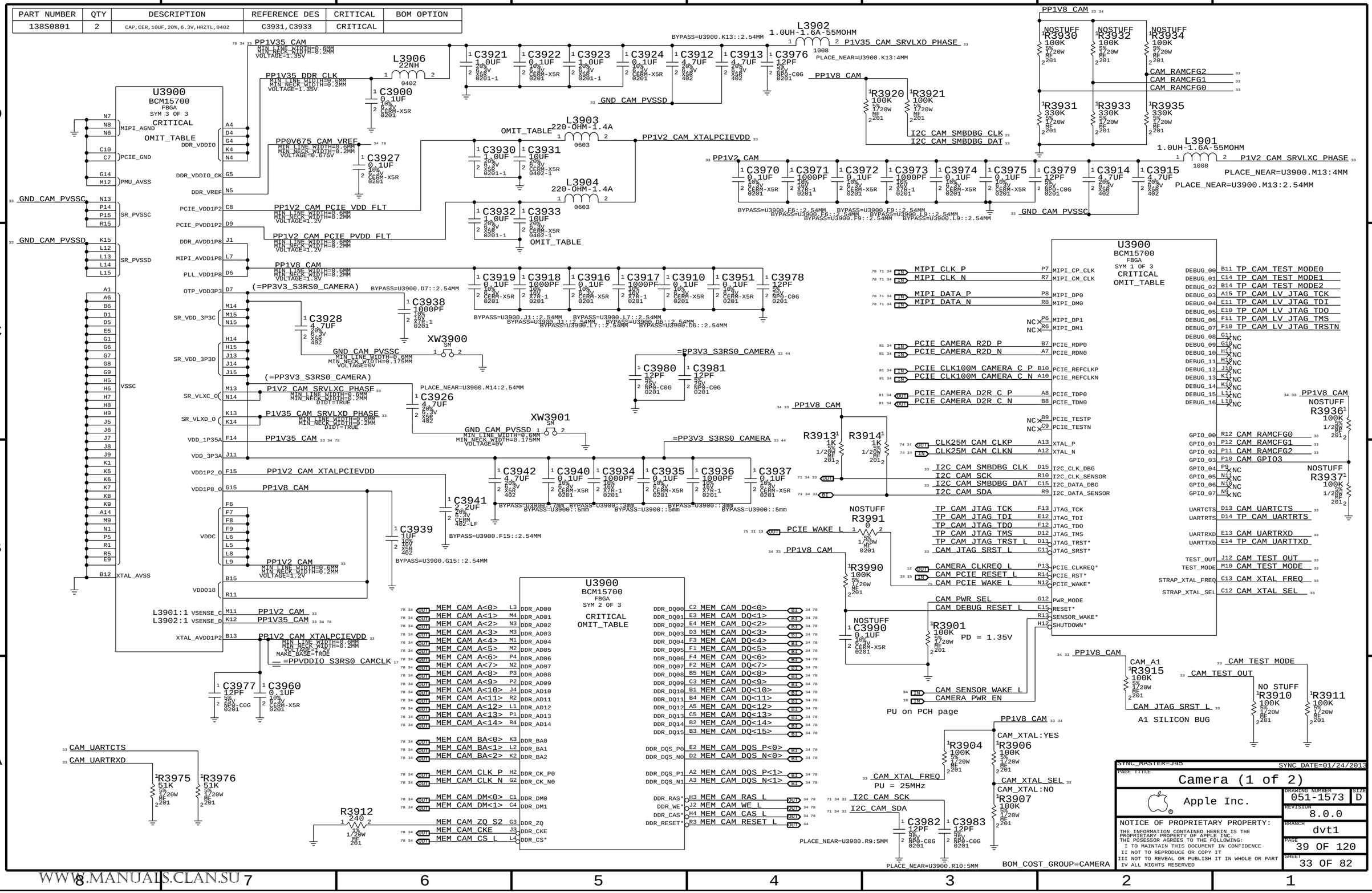
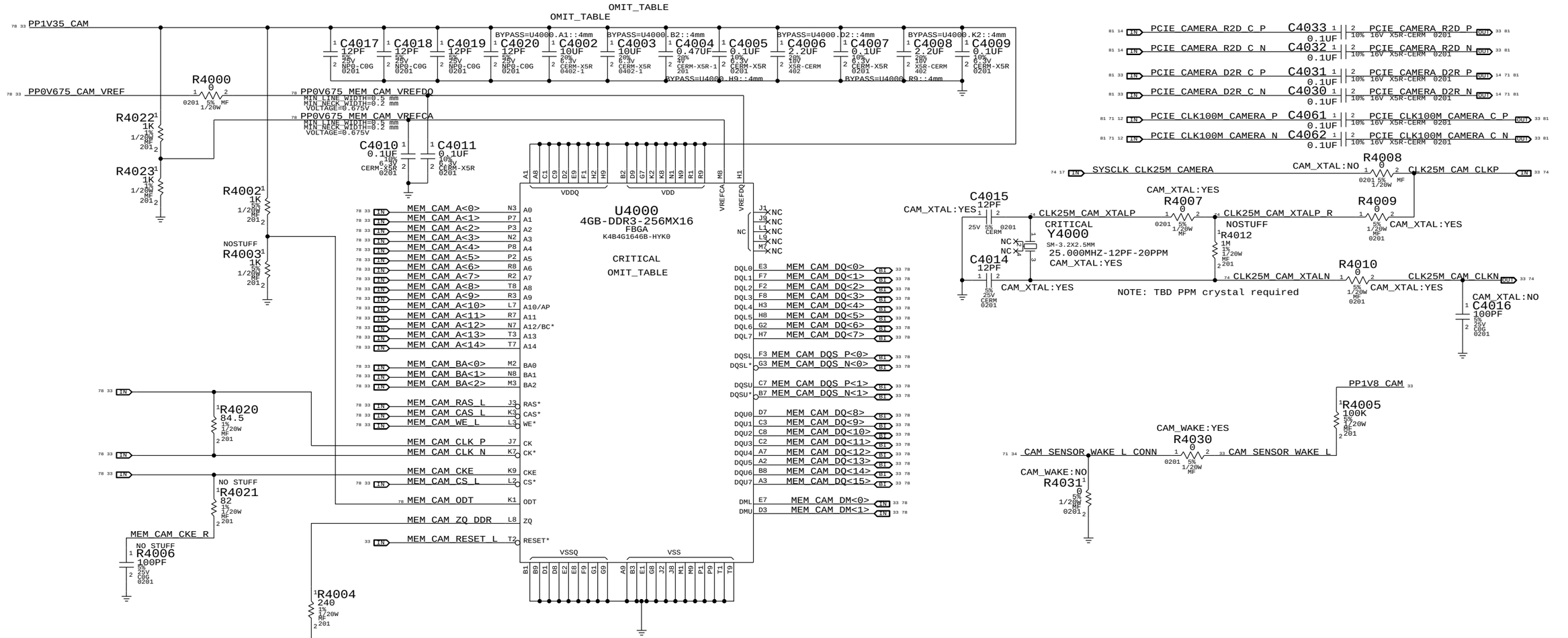
SHEET: 31 OF 82



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	2	CAP,CER,10UF,20%,6.3V,HRZTL,0402	C3931,C3933	CRITICAL	





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	2	CAP,CER,10UF,20%,6.3V,HRZTL,0402	C4002,C4003	CRITICAL	

BOM_COST_GROUP=CAMERA

SYNC_MASTER=J41 SYNC_DATE=12/21/2012

PAGE TITLE: Camera (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

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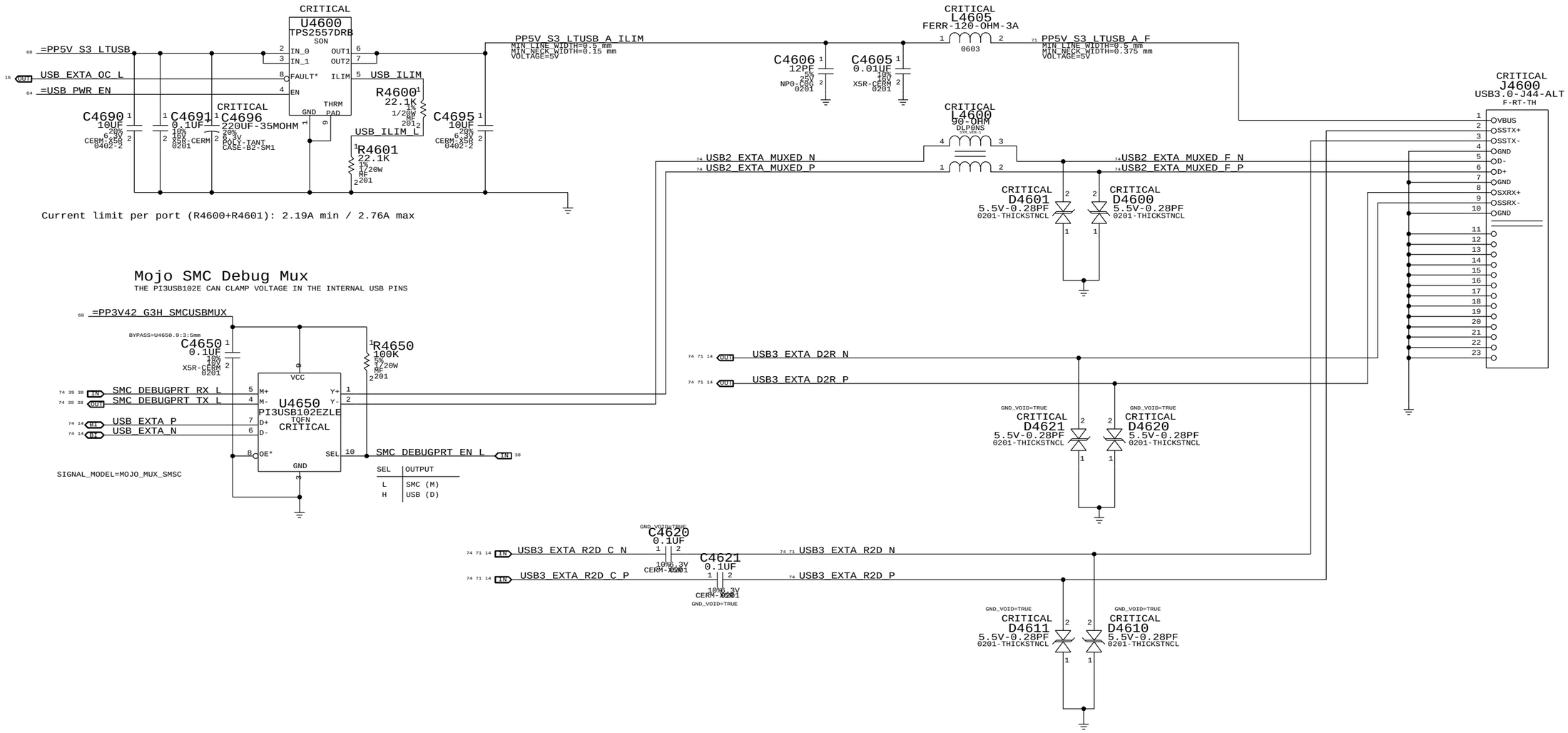
RIGHT USB PORT A

USB Port Power Switch



Current limit per port (R4600+R4601): 2.19A min / 2.76A max

Mojo SMC Debug Mux

THE PI3USB102E CAN CLAMP VOLTAGE IN THE INTERNAL USB PINS

BOM_COST_GROUP=IO PORTS

SYNC_MASTER=J41	SYNC_DATE=10/23/2012
PAGE TITLE	External A USB3 Connector
Apple Inc.	DRAWING NUMBER 051-1573 · SIZE D
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	BRANCH dvt1
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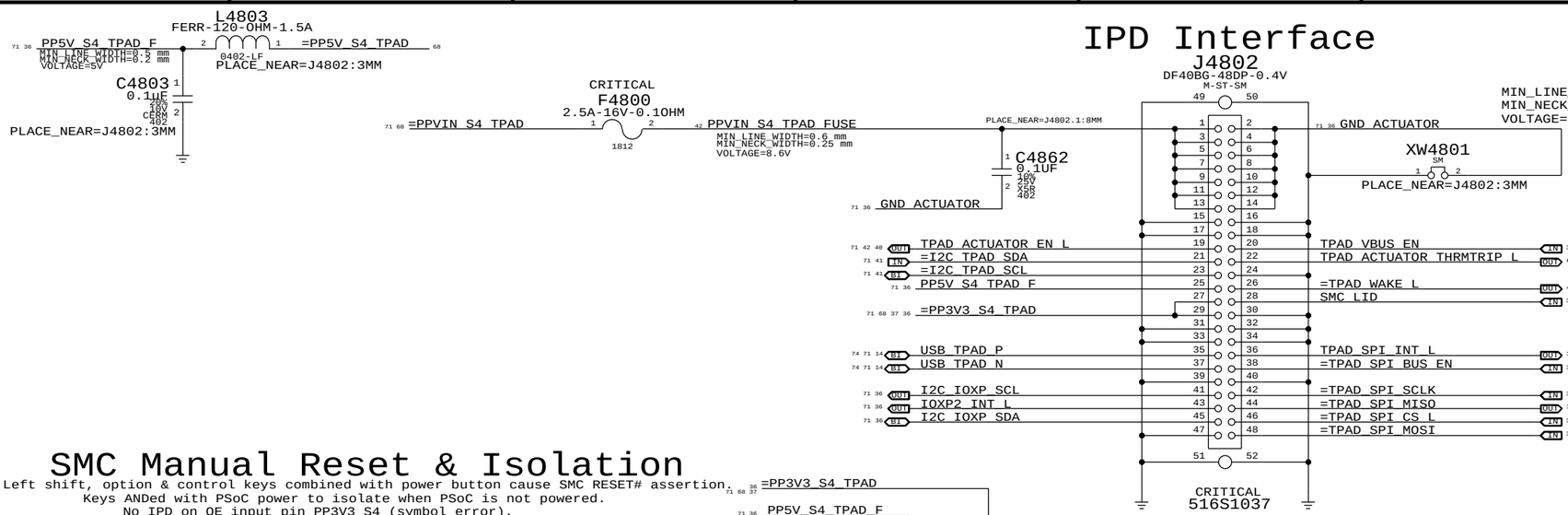
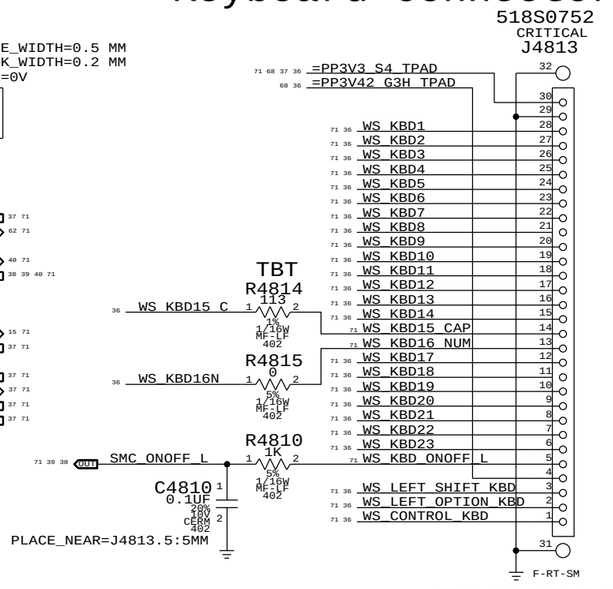
IPD Interface

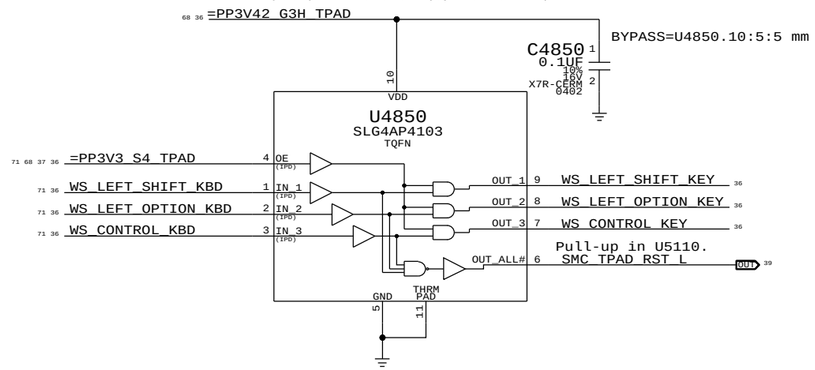


Keyboard Connector

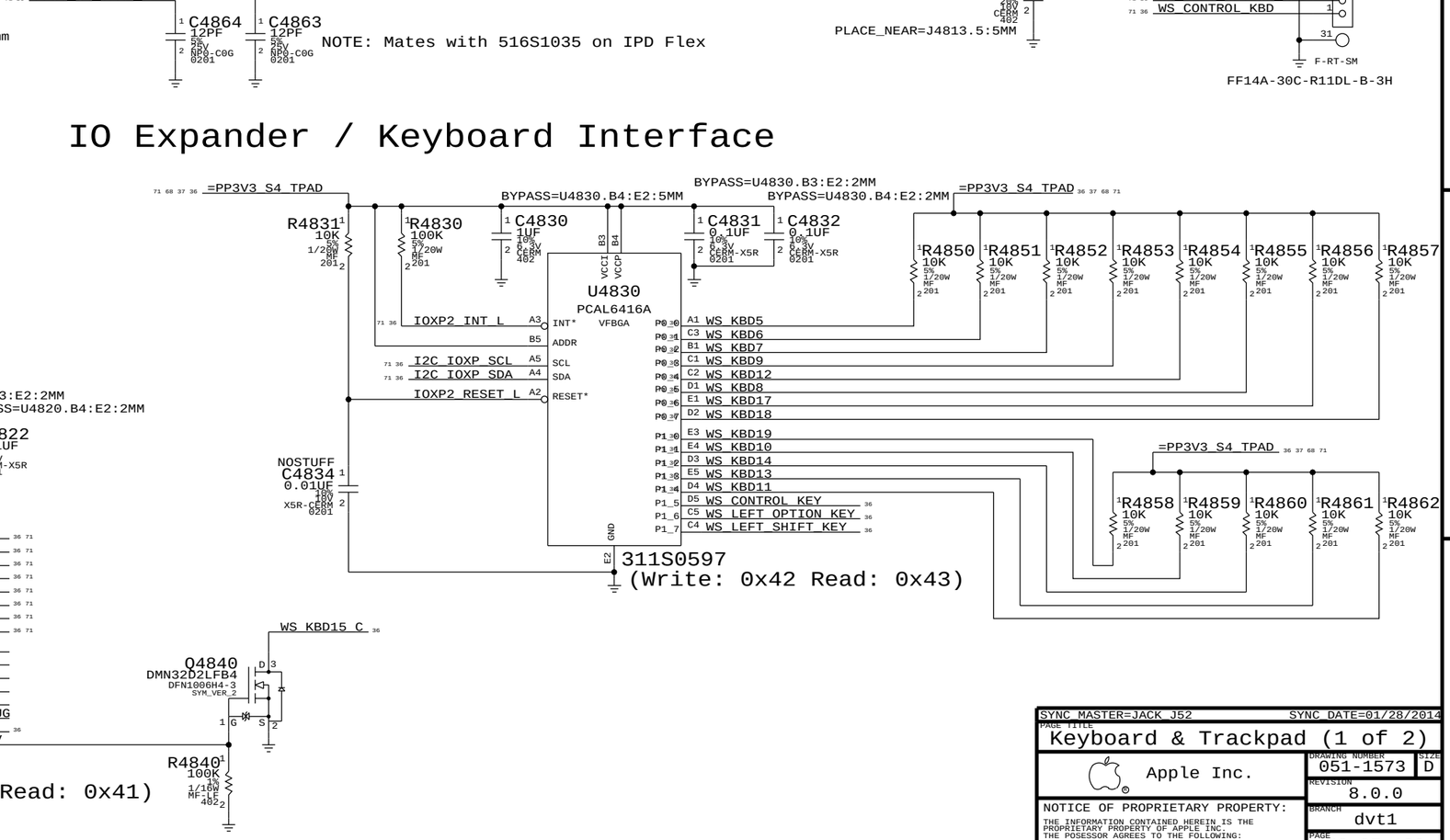


SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).



IO Expander / Keyboard Interface



SYNC_MASTER=JACK_J52	SYNC_DATE=01/28/2014
PAGE TITLE	Keyboard & Trackpad (1 of 2)
Apple Inc.	DRAWING NUMBER 051-1573 · SIZE D
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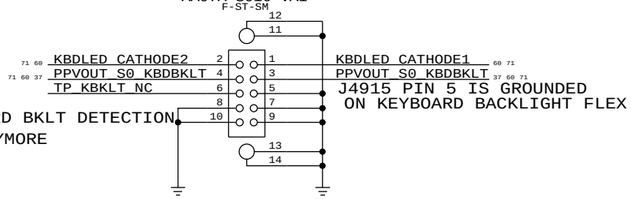
BOM_COST_GROUP=TRACKPAD

Keyboard Backlight Connector

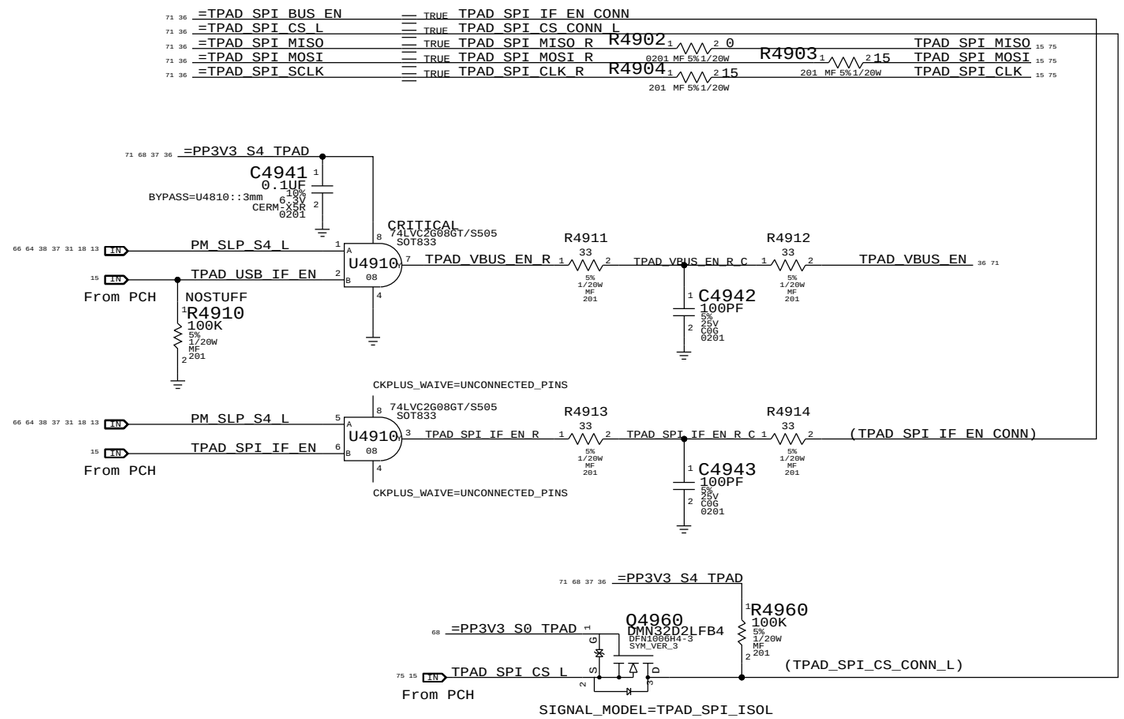
516S0899
CRITICAL
J4915
AA07A-S010-VA1
F-ST-SM



PIN 6 WAS USED KEYBOARD BKLT DETECTION
NOT USED ANYMORE

J4915 PIN 5 IS GROUNDED
ON KEYBOARD BACKLIGHT FLEX

TPAD SPI WITH SRC TERMINATION



BOM_COST_GROUP=TRACKPAD

SYNC MASTER=JACK J58 SYNC DATE=01/31/2014

PAGE TITLE
Keyboard & Trackpad (2 of 2)

Apple Inc.

DRAWING NUMBER 051-1573 | SIZE D
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BRANCH dvt1
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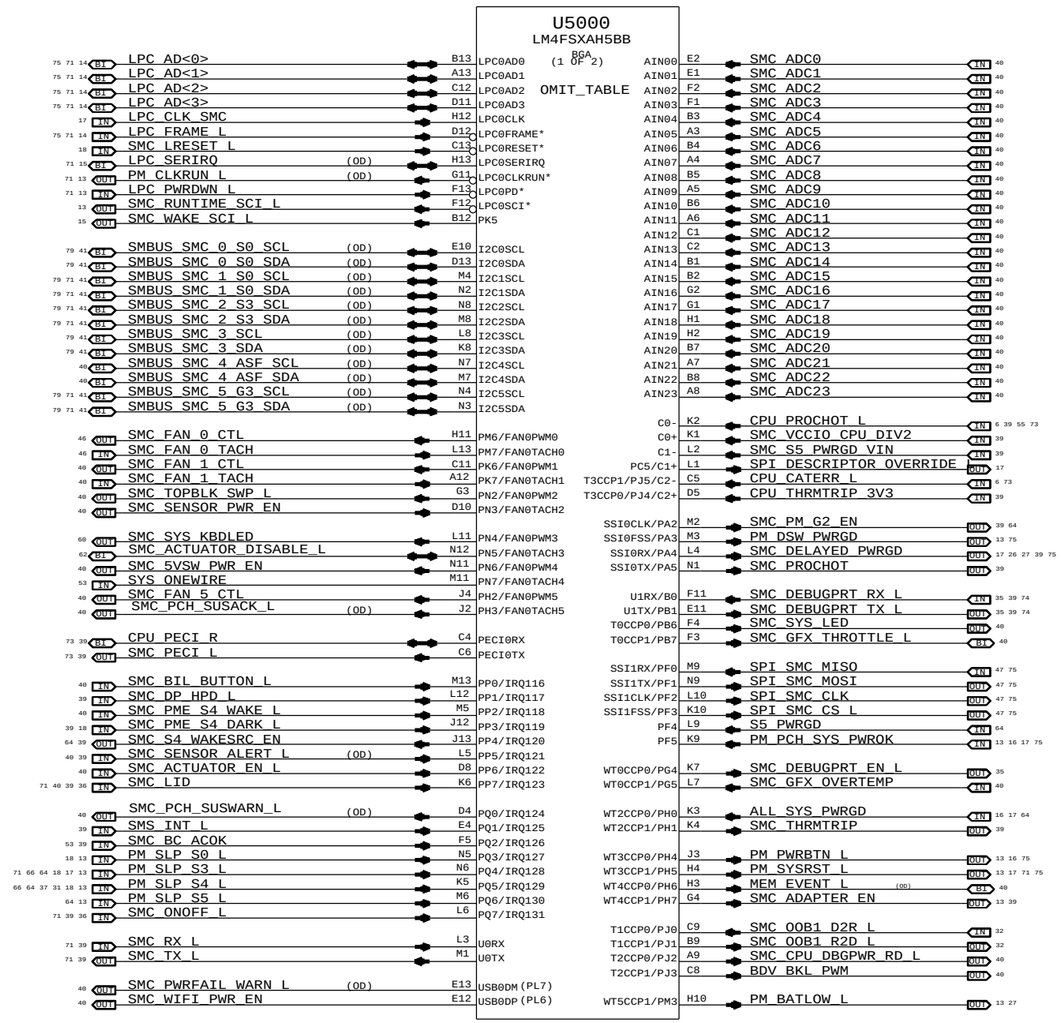

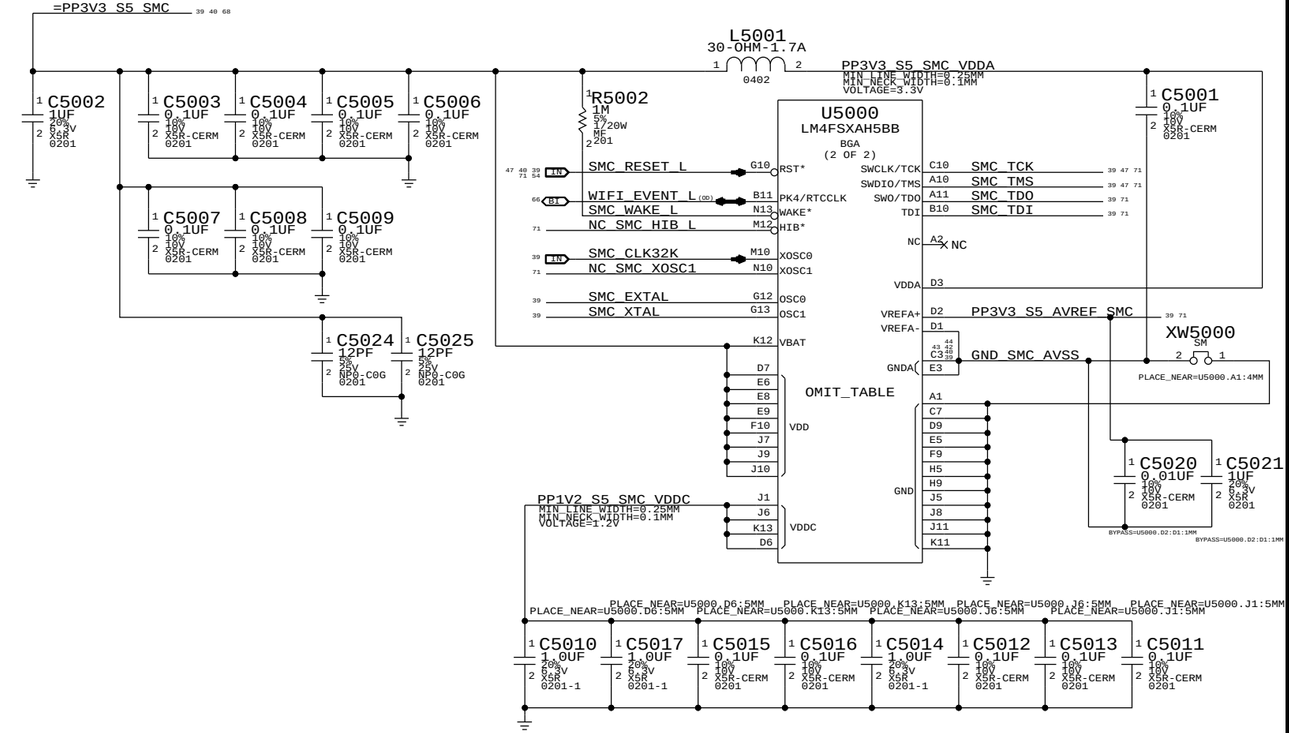

NOTE:
SMS INTERRUPT IS NOT USED, PULL UP TO SMC RAIL.

NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

BOM_COST_GROUP=SMC

SYNC_MASTER=JACK_J52 SYNC_DATE=11/07/2013

PAGE TITLE: SMC

Apple Inc.

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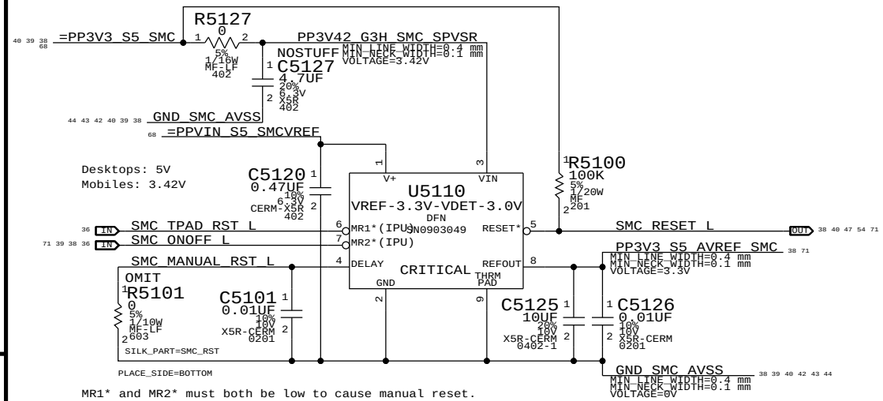
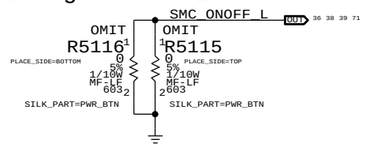
SMC Reset "Button", Supervisor & AVREF Supply



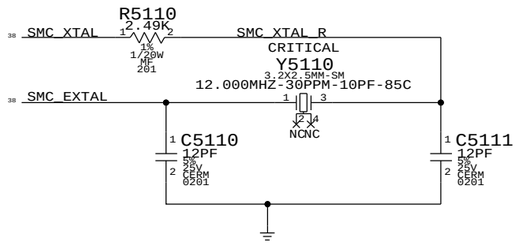
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

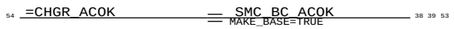
Debug Power "Buttons"

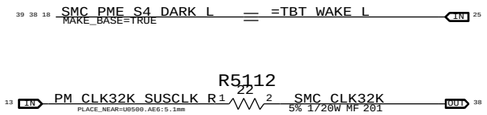


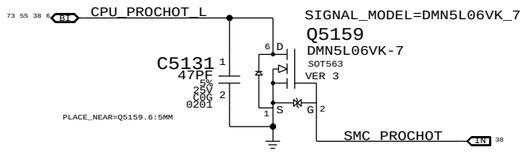
SMC Crystal Circuit

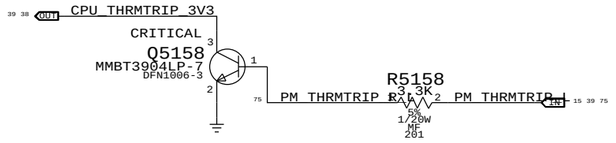
SMC USB Clock require these crystal
values:5,6,8,10,12,16,18,20,24,25 MHz

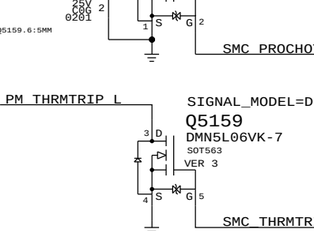




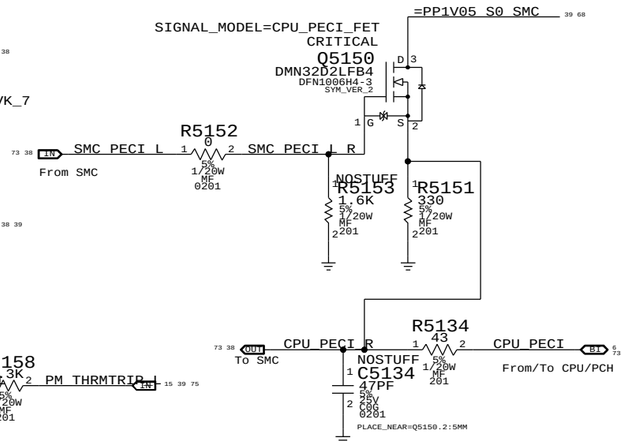


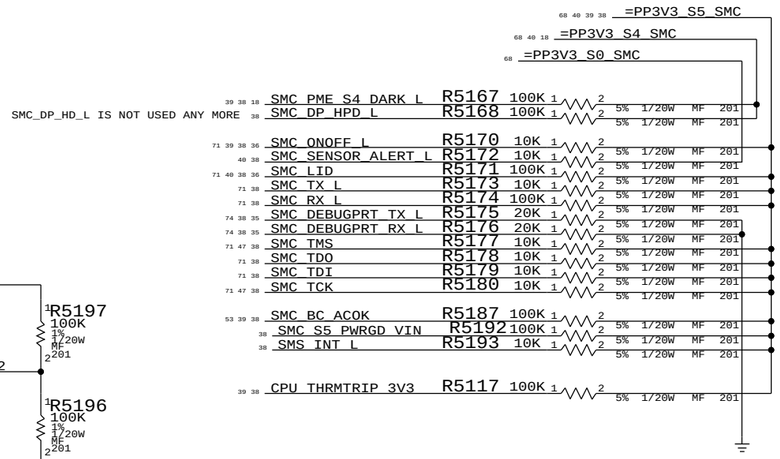






SMC12 PECI Support





BOM_COST_GROUP=SMC

SYNC MASTER=JACK_J52 SYNC DATE=10/24/2013

PAGE TITLE: SMC Shared Support

Apple Inc.

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SMC12 ADC Assignments

SMC_ADC0	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE
SMC_ADC1	SMC_PBUS_VSENSE	MAKE_BASE=TRUE
SMC_ADC2	SMC_BMON_ISENSE	MAKE_BASE=TRUE
SMC_ADC3	SMC_DCIN_ISENSE	MAKE_BASE=TRUE
SMC_ADC4	SMC_DCIN_VSENSE	MAKE_BASE=TRUE
SMC_ADC5	SMC_BMON_DISCRETE_ISENSE	MAKE_BASE=TRUE
SMC_ADC6	SMC_CPU_ISENSE	MAKE_BASE=TRUE
SMC_ADC7	SMC_OTHER5V_HI_ISENSE	MAKE_BASE=TRUE
SMC_ADC8	SMC_OTHER3V3_HI_ISENSE	MAKE_BASE=TRUE
SMC_ADC9	SMC_DDR_ISENSE	MAKE_BASE=TRUE
SMC_ADC10	SMC_LCDBKLT_ISENSE	MAKE_BASE=TRUE
SMC_ADC11	SMC_TPAD_ISENSE	MAKE_BASE=TRUE
SMC_ADC12	SMC_DDR1V8_ISENSE	MAKE_BASE=TRUE
SMC_ADC13	SMC_SSD_ISENSE	MAKE_BASE=TRUE
SMC_ADC14	SMC_PP3V3S0_ISENSE	MAKE_BASE=TRUE
SMC_ADC15	SMC_CAMERA_ISENSE	MAKE_BASE=TRUE
SMC_ADC16	SMC_TPAD_VSENSE	MAKE_BASE=TRUE
SMC_ADC17	SMC_PP5VS0_ISENSE	MAKE_BASE=TRUE
SMC_ADC18	SMC_CPUDDR_ISENSE	MAKE_BASE=TRUE
SMC_ADC19	SMC_PCH_ISENSE	MAKE_BASE=TRUE
SMC_ADC20	SMC_CPU_VSENSE	MAKE_BASE=TRUE
SMC_ADC21	SMC_LCDPANEL_ISENSE	MAKE_BASE=TRUE
SMC_ADC22	SMC_CPU_IMON_ISENSE	MAKE_BASE=TRUE
SMC_ADC23	SMC_TBT_ISENSE	MAKE_BASE=TRUE

SMC12 Pin Assignments

SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE, NO_TEST=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE, NO_TEST=TRUE
BDV_BKL_PWM	NC_SMC_TPAD_BOOST_DISABLE_L	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_SYS_LED	NC_SMC_SYS_LED	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_5VSW_PWR_EN	NC_SMC_5VSW_PWR_EN	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_FAN_5_CTL	NC_SMC_FAN_5_CTL	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_BIL_BUTTON_L	NC_SMC_BIL_BUTTON_L	MAKE_BASE=TRUE, NO_TEST=TRUE
MEM_EVENT_L	NC_MEM_EVENT_L	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_PWRFAIL_WARN_L	NC_SMC_PWRFAIL_WARN_L	MAKE_BASE=TRUE, NO_TEST=TRUE

Thermal Alerts

PCH_SML1ALERT_L — R5215 NOSTUFF 100 5% 1/20W MF 201

SMC_CPUHI_COMP_ALERT_L — R5217 CPUHYS 100 5% 1/20W MF 201

SMC_BMON_COMP_ALERT_L — R5213 BMONHYS 100 5% 1/20W MF 201

CPUTHMSNS_THM_L — R5216 100 5% 1/20W MF 201 — CPUTHRM_THRM:SMC

CPUTHMSNS_ALERT_L — R5214 100 5% 1/20W MF 201 — CPUTHRM_ALRT:SMC

TBTTHMSNS_THM_L — R5220 100 5% 1/20W MF 201 — TBTTHRM_THRM:SMC

TBTTHMSNS_ALERT_L — R5210 100 5% 1/20W MF 201 — TBTTHRM_ALRT:SMC

SMC_SENSOR_ALERT_L

=PP3V3_S5_SMC — R5232 10K 5% 1/20W MF 201 — SMC_CPU_DBGPWR_RD_L — SMC_BOARDID (MAKE_BASE=TRUE) — SMCBOARDID:16

SMC_BOARDID — R5233 10K 5% 1/20W MF 201 — SMCBOARDID:8

Hall Effect Pads

APN: 998-00296

OMIT_TABLE
J5250
HALL-EFFECT-MLB-J44
SM

=PP3V42_G3H_HALL — R5250 0 5% 1/10W MF-LF 402 — SMC_LID_R — SMC_LID — C5250 0.001UF 10% 50V X7R-CERM 0402

NC, NC, NC, NC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-01216	1	SUBASSY,PCBA,HALL EFFECT,X304	J5250	CRITICAL	

639-00525 (PCBA,HALL EFFECT,X304) REPORTS TO 677-01216

Specify one of these BOM GROUPs.

BOM GROUP	BOM OPTIONS
CPUTHRM:BOTH	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:SMC
CPUTHRM:THRM	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:PU
CPUTHRM:ALRT	CPUTHRM_THRM:PU,CPUTHRM_ALRT:SMC
CPUTHRM:NONE	CPUTHRM_THRM:PU,CPUTHRM_ALRT:PU

Specify one of these BOM GROUPs.

BOM GROUP	BOM OPTIONS
TBTTHRM:BOTH	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:SMC
TBTTHRM:THRM	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:PU
TBTTHRM:ALRT	TBTTHRM_THRM:PU,TBTTHRM_ALRT:SMC
TBTTHRM:NONE	TBTTHRM_THRM:PU,TBTTHRM_ALRT:PU

Requires EMC1412-1 or EMC1412-2 instead of EMC1412-A, new APN needs to be created.

S4 SMC Wake Sources

=PP3V3_S4_SMC — R5282 100K 5% 1/20W MF 201

=TPAD_WAKE_L
BT_WAKE_L
— SMC_PME_S4_WAKE_L (MAKE_BASE=TRUE)

R5230 0 5% 1/20W MF 0201 — SMC_PCH_SUSWARN_L (MAKE_BASE=TRUE) — PCH_SUSWARN_L

R5231 0 5% 1/20W MF 0201 — SMC_PCH_SUSACK_L (MAKE_BASE=TRUE) — PCH_SUSACK_L

SMC_SENSOR_PWR_EN (MAKE_BASE=TRUE) — P3V3S4SW_SNS_EN
SMC_SENSOR_PWR_EN — PBUSVSENSE_EN

SMC_WIFI_PWR_EN (MAKE_BASE=TRUE) — PM_WLAN_EN

=PP3V3_S4_SMC
SMC_WIFI_PWR_EN — R5295 10K 5% 1/20W MF 201 NOSTUFF
SMC_SENSOR_PWR_EN — R5294 10K 5% 1/20W MF 201 NOSTUFF

Top Block Swap

=PP3V3R1V8_S0_PCH_VCCSDIO — R5296 1K 5% 1/20W MF 201 — SMC_TOPBLK_SWP_L — R5283 1K 5% 1/20W MF 201 — PCH_STRP_TOPBLK_SWP_L

TPAD_ACTUATOR_EN_L — R5297 100 1% 1/20W MF 201 — TPAD_ACTUATOR_EN_RC_L (MAKE_BASE=TRUE) — SMC_ACTUATOR_EN_L

RC Placeholder to filter noise on this signal towards SMC IO.

C5271 220PF 10% 25V X7R-CERM 201

NOSTUFF C5270 1000PF 10% 16V X7R-1 0201

SMC_RESET_L
GND_SMC_AVSS

BOM_COST_GROUP=SMC

PAGE TITLE: SMC Project Support

Apple Inc.

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DRAWING NUMBER	051-1573
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REVISION	8.0.0
BRANCH	dvt1
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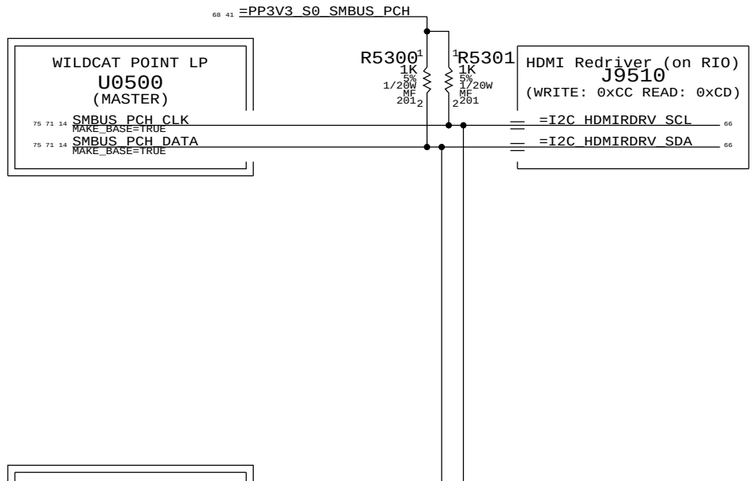
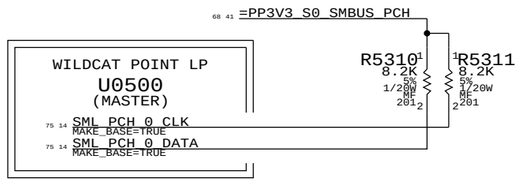
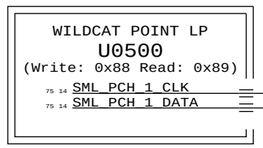
WILDCAT POINT LP S0 "SMBus 0" Connections



WILDCAT POINT LP S0 "SMLink 0" Connections

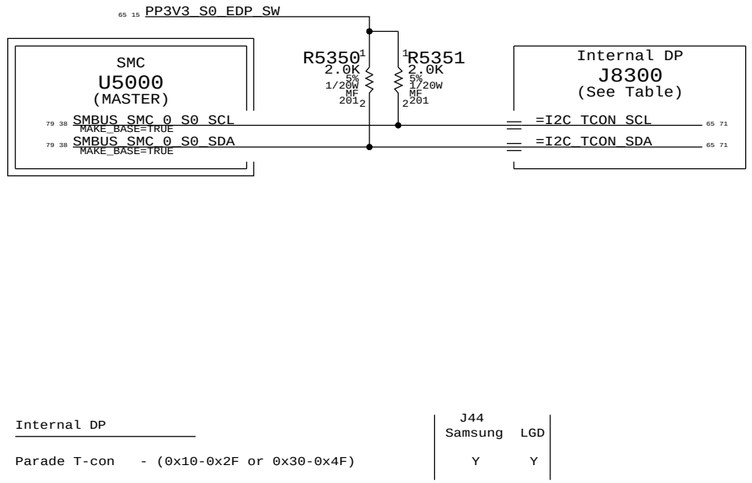


WILDCAT POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to access PCH.

SMC SMBus "0" S0 Connections

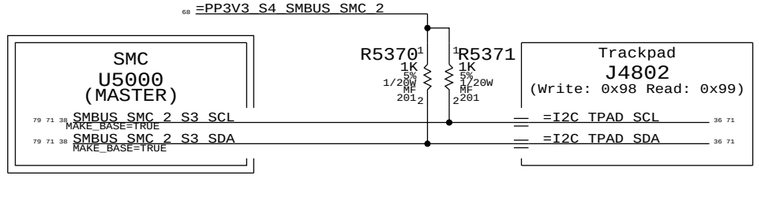


Internal DP

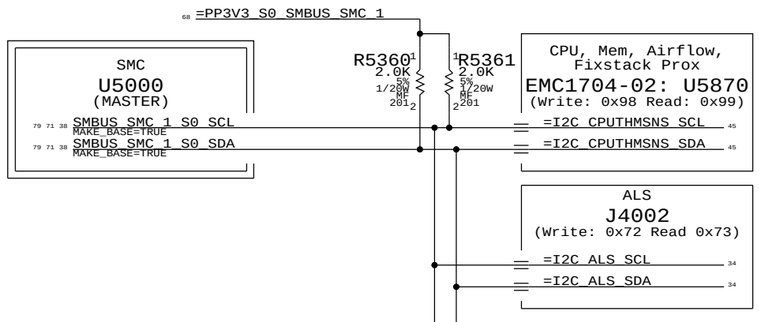
Parade T-con - (0x10-0x2F or 0x30-0x4F)

	J44 Samsung	J44 LGD
	Y	Y

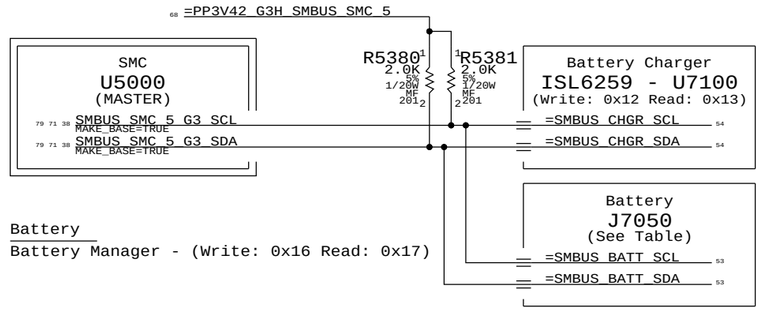
SMC SMBus "2" S3 Connections



SMC SMBus "1" S0 Connections



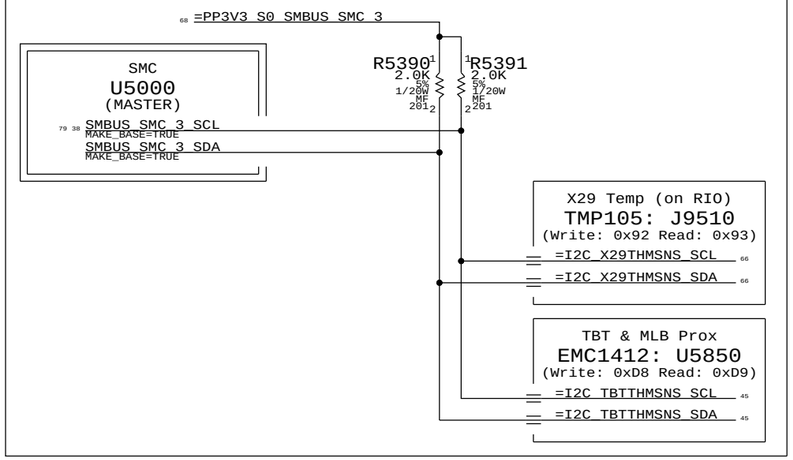
SMC SMBus "5" G3H Connections



Battery

Battery Manager - (Write: 0x16 Read: 0x17)

SMC SMBus "3" S0 Connections



BOM_COST_GROUP=SMC

SYNC_MASTER=GKOO_J52 SYNC_DATE=12/06/2013

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

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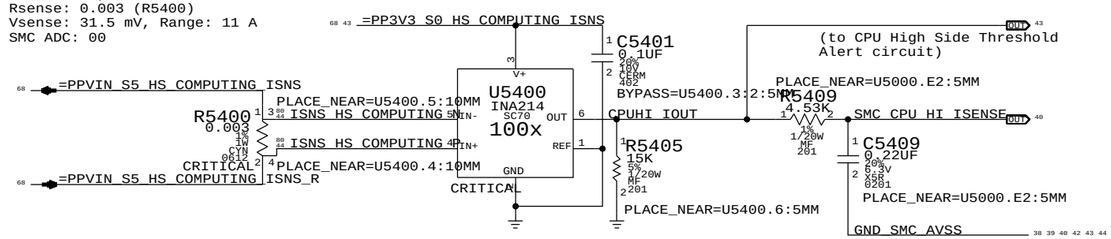
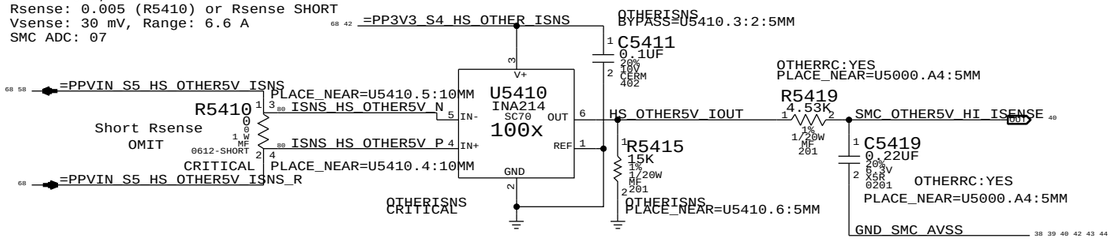
CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 10.5 A
Rsense: 0.003 (R5400)
Vsense: 31.5 mV, Range: 11 A
SMC ADC: 00



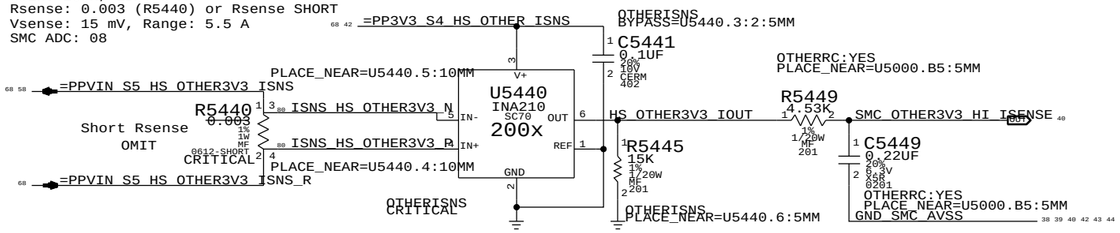
OTHER 5V High Side Current Sense (IO5R)

Gain: 100x, EDP: 6 A
Rsense: 0.005 (R5410) or Rsense SHORT
Vsense: 30 mV, Range: 6.6 A
SMC ADC: 07



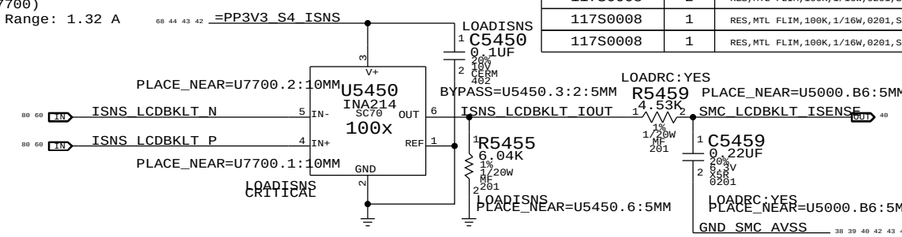
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 5 A
Rsense: 0.003 (R5440) or Rsense SHORT
Vsense: 15 mV, Range: 5.5 A
SMC ADC: 08



LCD Backlight Current Sense (IBLC)

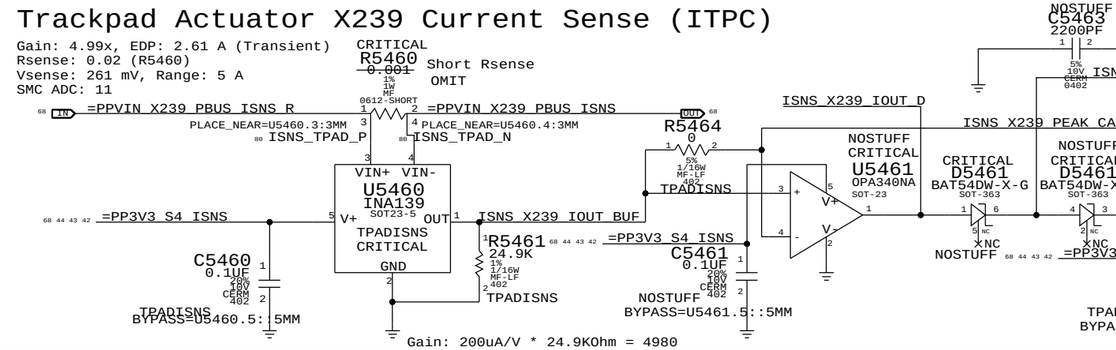
Gain: 100x. EDP: 0.9 A
Rsense: 0.025 (R7700)
Vsense: 22.5 mV, Range: 1.32 A
SMC AD: 10



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		OTHERRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		TPADRC:NO

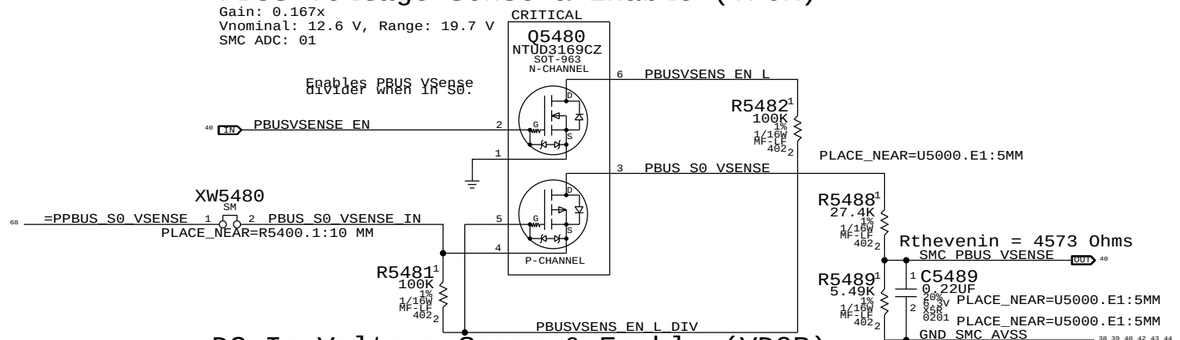
Trackpad Actuator X239 Current Sense (ITPC)

Gain: 4.99x, EDP: 2.61 A (Transient)
Rsense: 0.02 (R5460)
Vsense: 261 mV, Range: 5 A
SMC ADC: 11



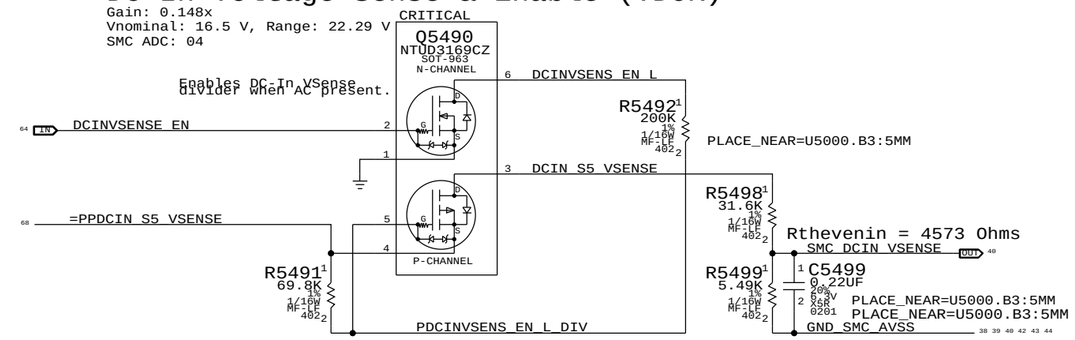
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 19.7 V
SMC ADC: 01



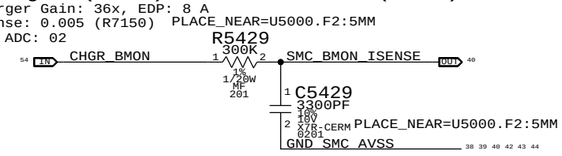
DC In Voltage Sense & Enable (VD0R)

Gain: 0.148x
Vnominal: 16.5 V, Range: 22.29 V
SMC ADC: 04



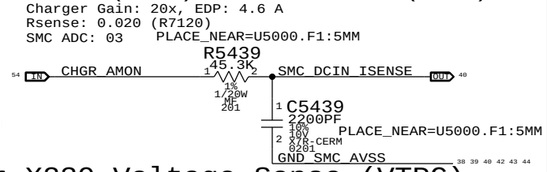
Charger (BMON) Current Sense (IPBR)

Charger Gain: 36x, EDP: 8 A
Rsense: 0.005 (R7150)
SMC ADC: 02



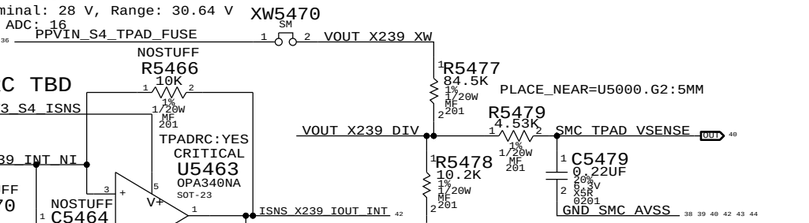
DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7120)
SMC ADC: 03

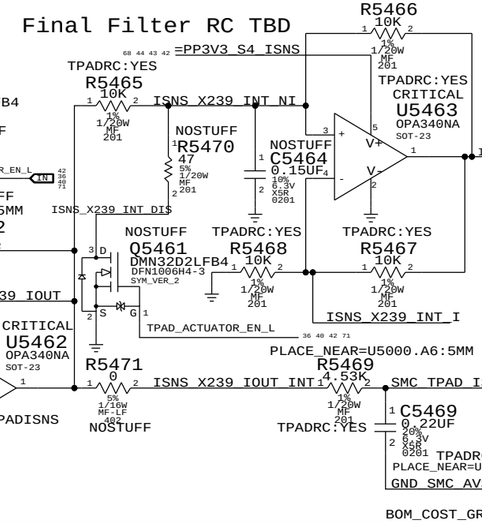


Trackpad Actuator X239 Voltage Sense (VTPC)

Gain: 0.10771
Vnominal: 28 V, Range: 30.64 V
SMC ADC: 16



Final Filter RC TBD



SYNC MASTER=JACK J52 SYNC DATE=12/15/2013
PAGE TITLE: Power Sensors: High Side
Apple Inc.
DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
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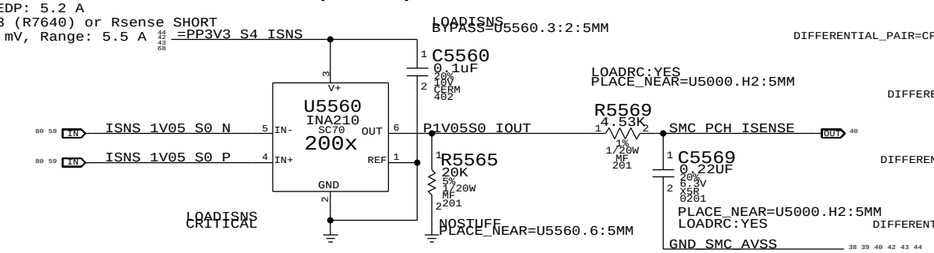
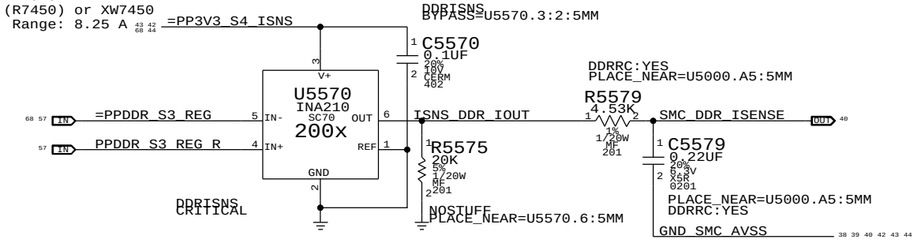
PCH 1.05V Current Sense (IC1C)

Gain: 200x, EDP: 5.2 A
Rsense: 0.003 (R7640) or Rsense SHORT
Vsense: 15.6 mV, Range: 5.5 A
SMC ADC: 19



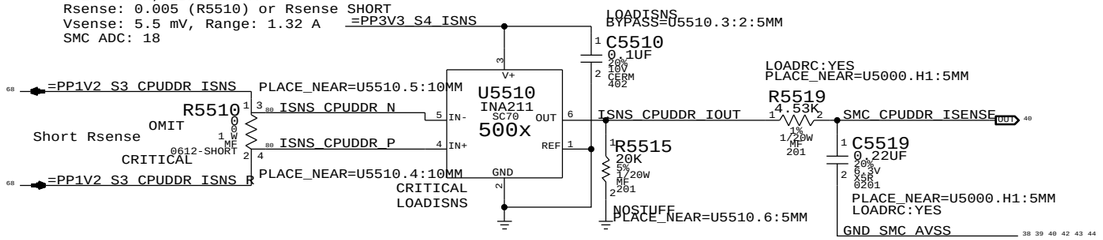
DDR 1.2V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 200x, EDP: 9.5 A
Rsense: 0.002 (R7450) or XW7450
Vsense: 19 mV, Range: 8.25 A
SMC ADC: 09



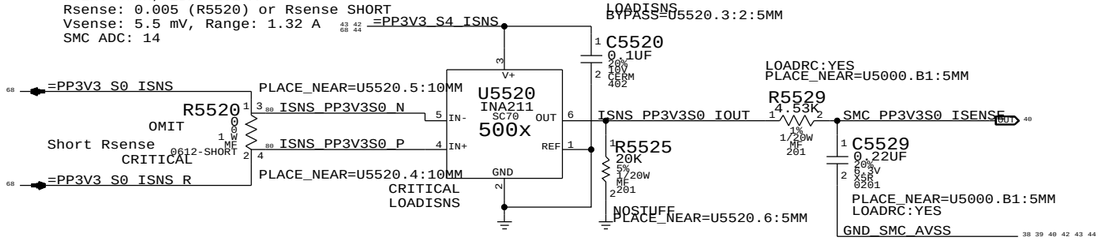
CPU DDR 1.2V S3 (CPU Only) Current Sense (IM1C)

Gain: 500x, EDP: 1.1 A
Rsense: 0.005 (R5510) or Rsense SHORT
Vsense: 5.5 mV, Range: 1.32 A
SMC ADC: 18



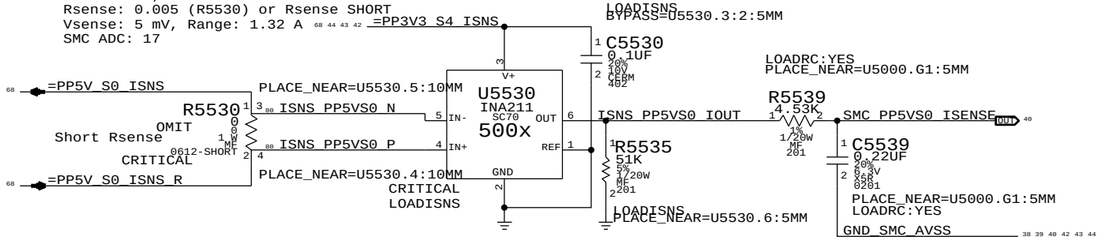
3.3V S0 Rail Current Sense (IR3C)

Gain: 500x, EDP: 1.1 A
Rsense: 0.005 (R5520) or Rsense SHORT
Vsense: 5.5 mV, Range: 1.32 A
SMC ADC: 14



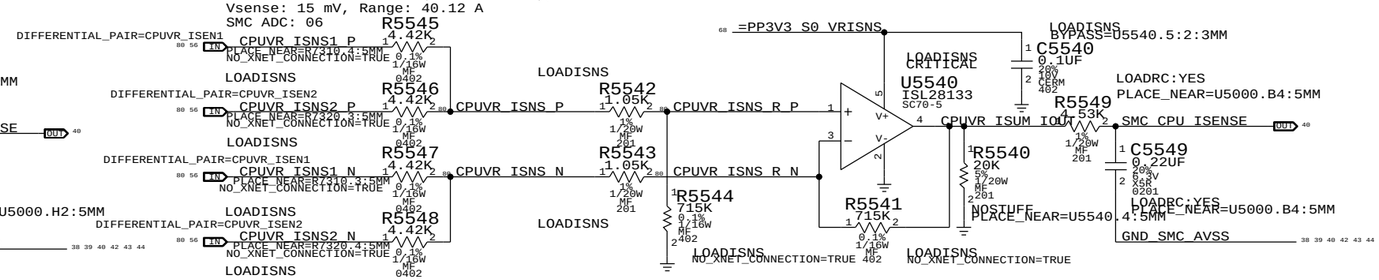
5V S0 Rail Current Sense (IR5C)

Gain: 500x, EDP: 1.0 A
Rsense: 0.005 (R5530) or Rsense SHORT
Vsense: 5 mV, Range: 1.32 A
SMC ADC: 17



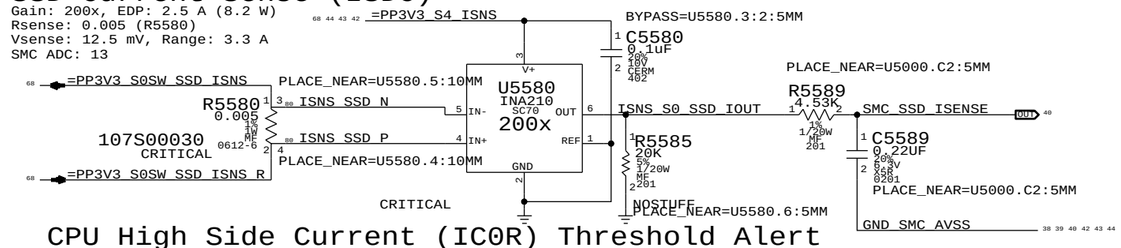
CPU Fixed Current Sense (IC0C)

Gain: 219.33x, EDP: 40 A
Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
Vsense: 15 mV, Range: 40.12 A
SMC ADC: 06



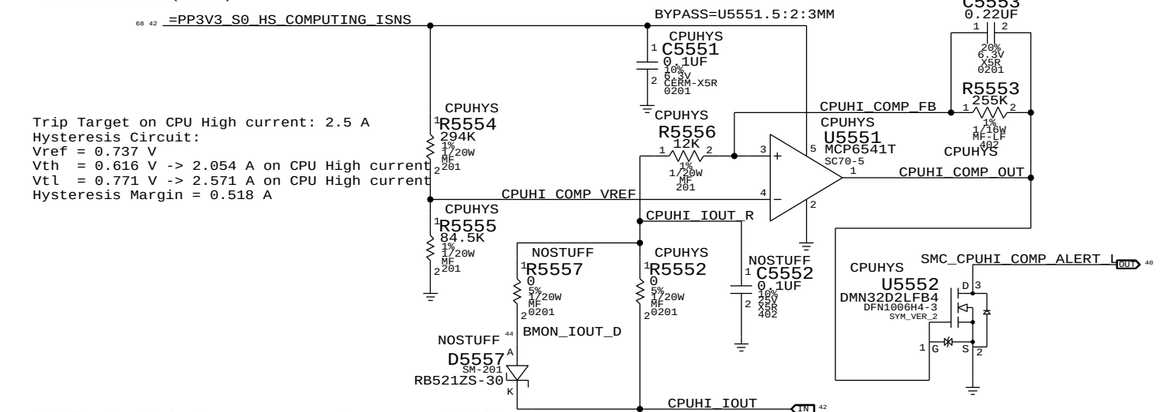
SSD Current Sense (ISDC)

Gain: 200x, EDP: 2.5 A (8.2 W)
Rsense: 0.005 (R5580)
Vsense: 12.5 mV, Range: 3.3 A
SMC ADC: 13



CPU High Side Current (IC0R) Threshold Alert

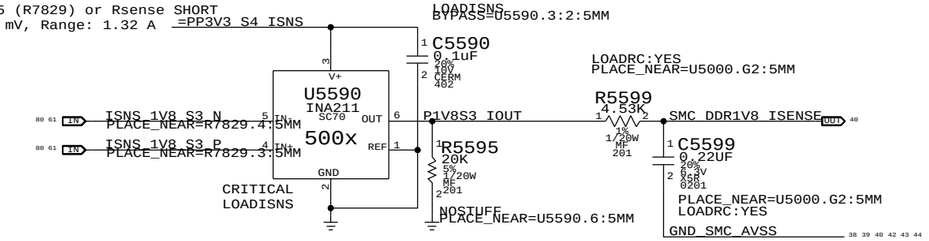
Gain: 100x
Rsense: 0.003 (R5400)



Trip Target on CPU High current: 2.5 A
Hysteresis Circuit:
Vref = 0.737 V
Vth = 0.616 V -> 2.054 A on CPU High current
Vtl = 0.771 V -> 2.571 A on CPU High current
Hysteresis Margin = 0.518 A

DDR 1.8V Current Sense (IM2C)

Gain: 500x, EDP: 0.45 A
Rsense: 0.005 (R7829) or Rsense SHORT
Vsense: 2.25 mV, Range: 1.32 A
SMC ADC: 12



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5569,C5519,C5599		LOADRC:NO
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5529,C5539,C5549		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRC:NO

BOM_COST_GROUP=SENSORS

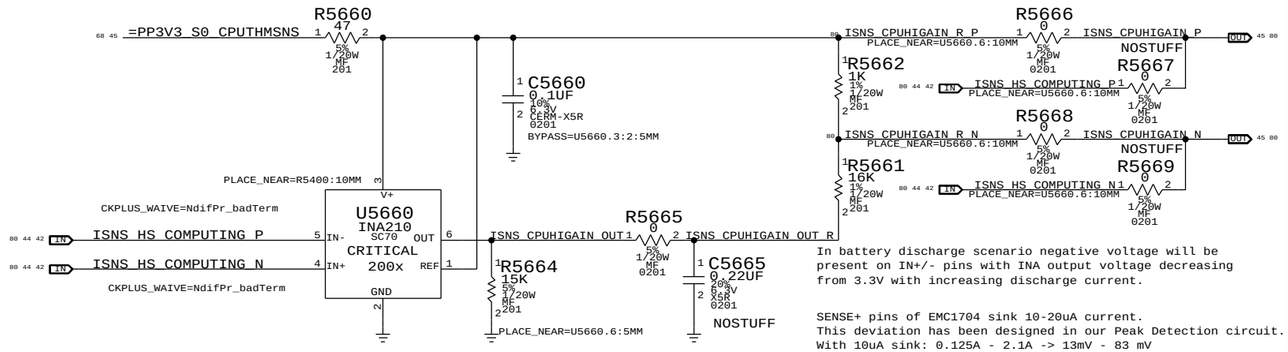
SYNC_MASTER=JACK_J52 SYNC_DATE=12/06/2013

PAGE TITLE: Power Sensors: Load Side

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D
REVISION: 8.0.0
BRANCH: dvt1
PAGE: 55 OF 120
SHEET: 43 OF 82

CPU High Side (IC0R) Peak Detection Support

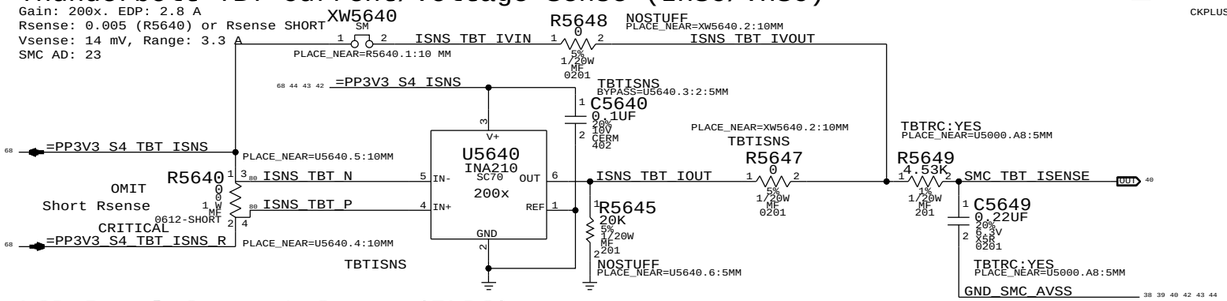


In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

SENSE+ pins of EMC1704 sink 10-20uA current.
This deviation has been designed in our Peak Detection circuit.
With 10uA sink: 0.125A - 2.1A -> 13mV - 83 mV
With 20uA sink: 0.125A - 2.1A -> 23mV - 92 mV

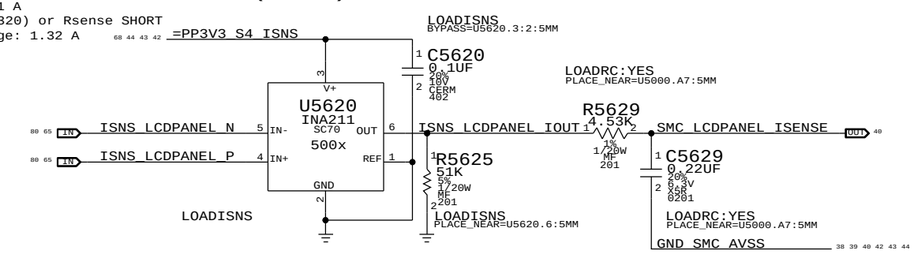
Thunderbolt TBT Current/Voltage Sense (IHSC/VHSC)

Gain: 200x. EDP: 2.8 A
Rsense: 0.005 (R5640) or Rsense SHORT
Vsense: 14 mV, Range: 3.3 A
SMC AD: 23



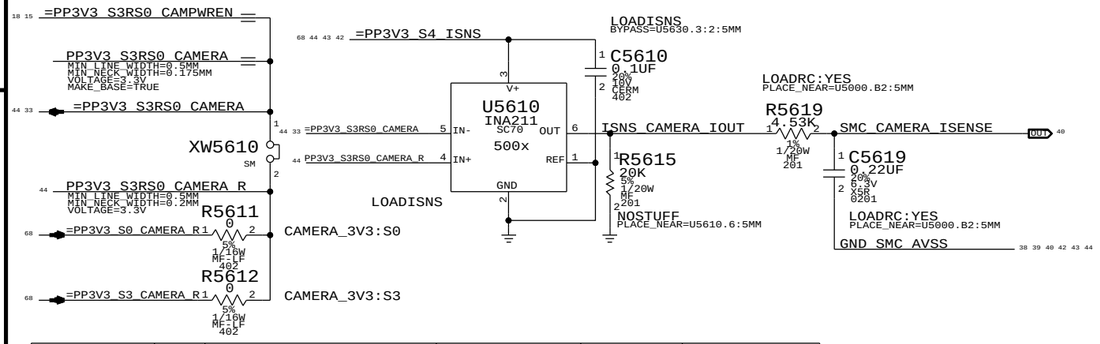
LCD Panel Current Sense (ILDC)

Gain: 500x. EDP: 1 A
RSENSE: 0.005 (R8320) or Rsense SHORT
Vsense: 5 mV, Range: 1.32 A
SMC AD: 21



Camera (S2 Controller) Current Sense (ICMC)

Gain: 500x. EDP: 0.82 A
Rsense: 0.005 (R5610) or XW5610
Vsense: 4.1 mV, Range: 1.32 A
SMC AD: 15



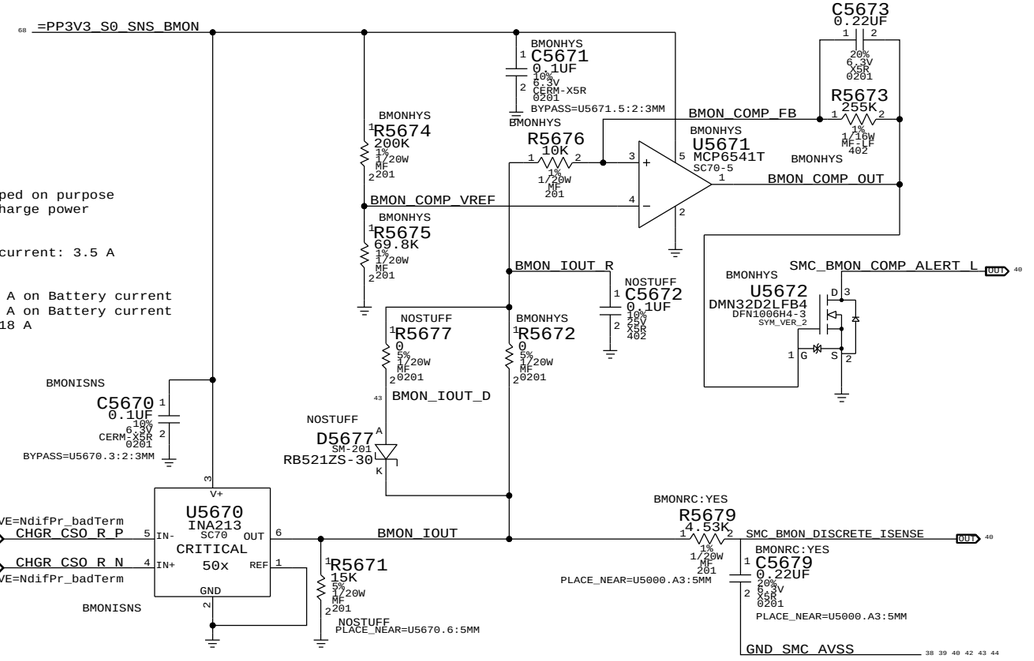
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629		LOADRC:NO
117S0008	1	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5679		BMONRC:NO
117S0008	1	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5649		TBTRC:NO

CHGR_CSO_R_P/N are swapped on purpose to measure Battery discharge power into system.

Trip Target on Battery current: 3.5 A
Hysteresis Circuit:
Vref = 0.854 V
Vth = 0.758 V -> 3.031 A on Battery current
Vtl = 0.887 V -> 3.549 A on Battery current
Hysteresis Margin = 0.518 A

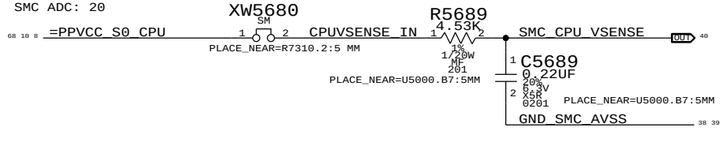
Battery BMON Discrete Current Sense (IP0R) & Threshold Alert

Gain: 50x. EDP: 8 A
Rsense: 0.005 (R7150)
Vsense: 50 mV, Range: 13.2 A
SMC AD: 05



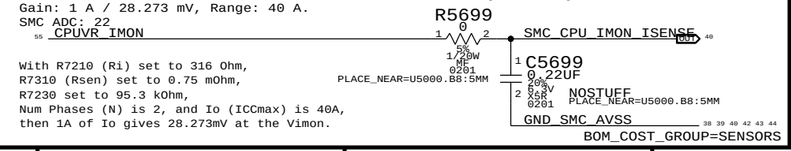
CPU Core Voltage Sense (VC0C)

SMC ADC: 20



CPU Core IMON Current Sense (IC2C)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 22



With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.

BOM_COST_GROUP=SENSORS

SYNC_MASTER=JACK J52 SYNC_DATE=10/26/2013

PAGE TITLE
Power Sensors: Extended

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
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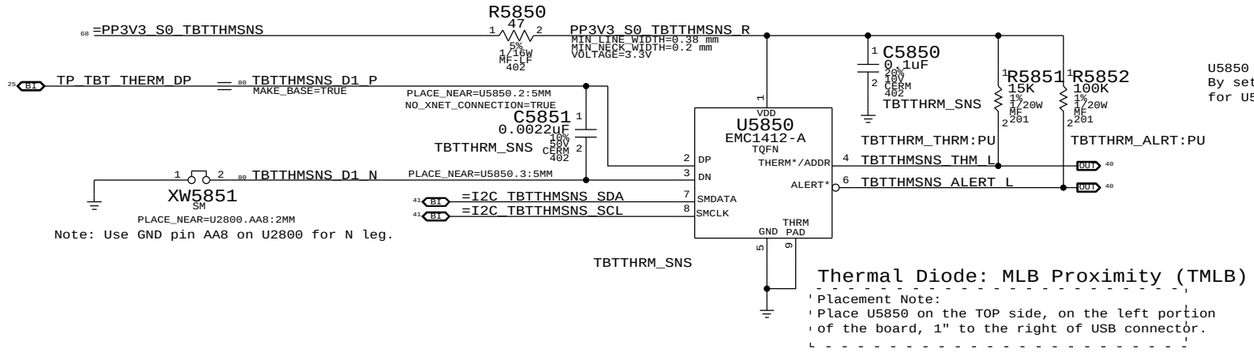
Thermal Sensor A:
Thunderbolt Die, MLB Proximity

I2C Write: 0xD8, I2C Read: 0xD9



Note: Use GND pin AA8 on U2800 for N leg.

U5850 I2C Address:
By setting R5851 to 15k, I2C address for U5850 is 0xD8/0xD9.

Thermal Diode: TBT Die (THSP)

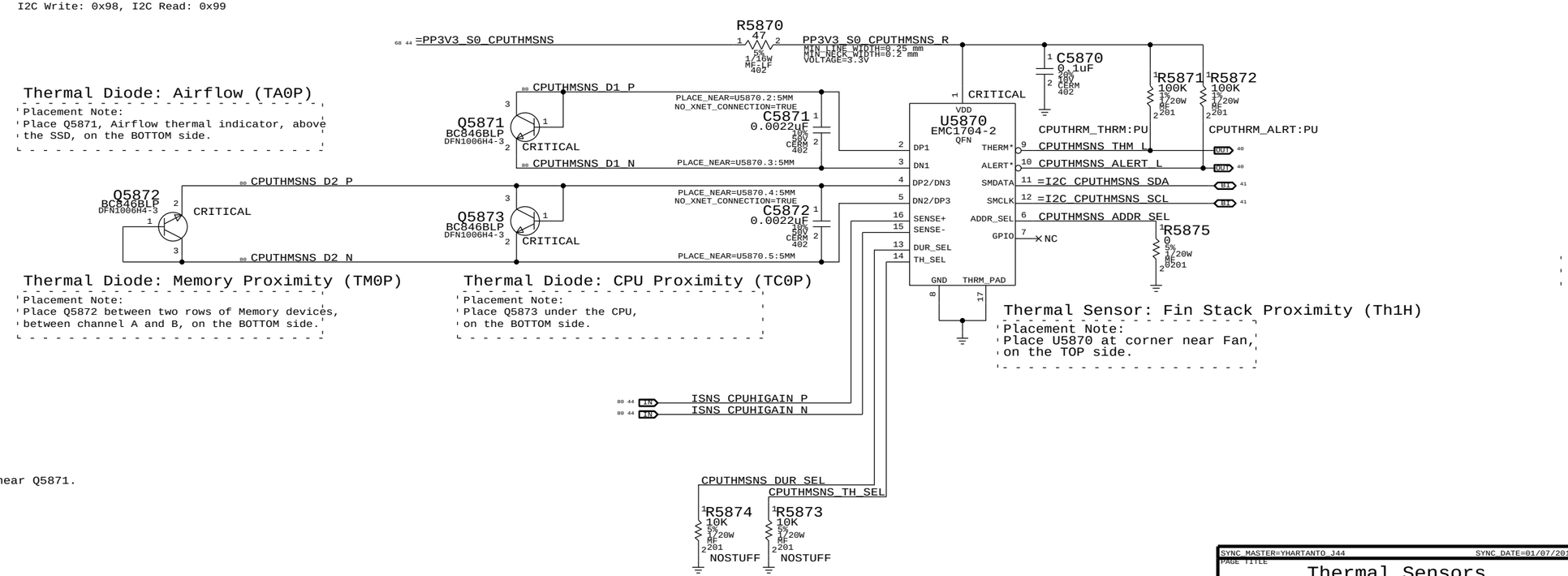
Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AA8.

Thermal Diode: MLB Proximity (TMLB)

Placement Note:
Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

Thermal Sensor B & CPU High Peak Detection:
CPU Proximity, Memory Proximity, Airflow, Fin Stack Proximity

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: Airflow (TA0P)

Placement Note:
Place Q5871, Airflow thermal indicator, above the SSD, on the BOTTOM side.

Thermal Diode: Memory Proximity (TM0P)

Placement Note:
Place Q5872 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

Thermal Diode: CPU Proximity (TC0P)

Placement Note:
Place Q5873 under the CPU, on the BOTTOM side.

Thermal Sensor: Fin Stack Proximity (Th1H)

Placement Note:
Place U5870 at corner near Fan, on the TOP side.

Placement Note: Place C5800 and C5801 near Q5871.

NC C5800 0.0022UF 10% 50V CERM-X7R 0603 NC

NC C5801 0.0022UF 10% 50V CERM-X7R 0603 NC

BOM_COST_GROUP=SENSORS

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/07/2013

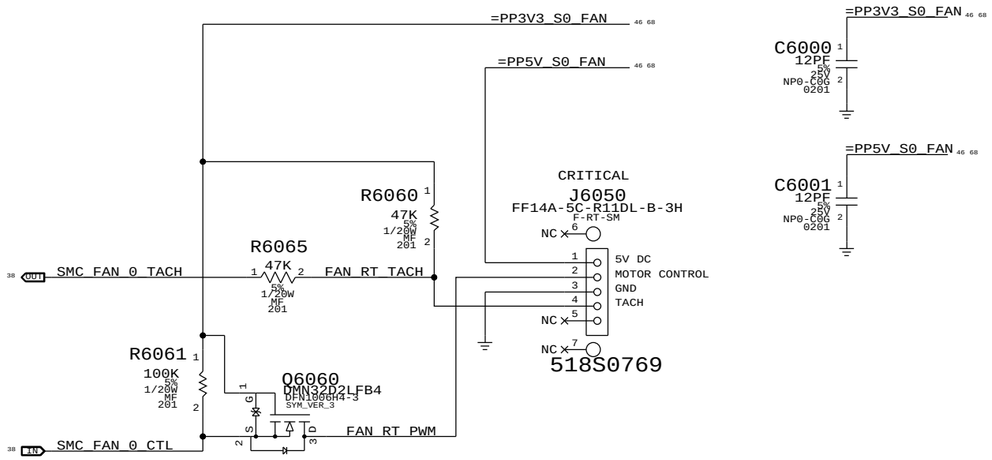
PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D
REVISION: 8.0.0
BRANCH: dvt1
PAGE: 58 OF 120
SHEET: 45 OF 82

FAN CONNECTOR

KEEP THE 5 PIN CONNECTOR FROM D1



Placement Note: Place C6002 and C6003 near Q6060

BOM_COST_GROUP=FAN

SYNC_MASTER=J41 SYNC_DATE=10/23/2012

PAGE TITLE: Fan

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

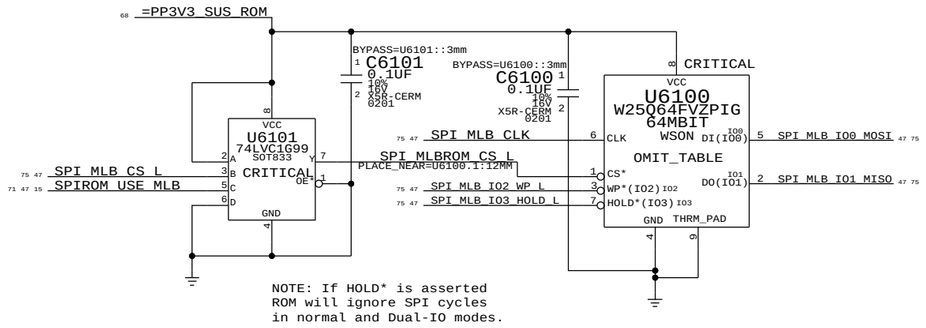
BRANCH: dvt1

PAGE: 60 OF 120

SHEET: 46 OF 82

SPI ROM

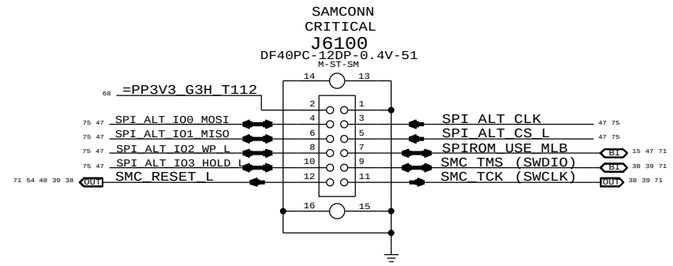
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

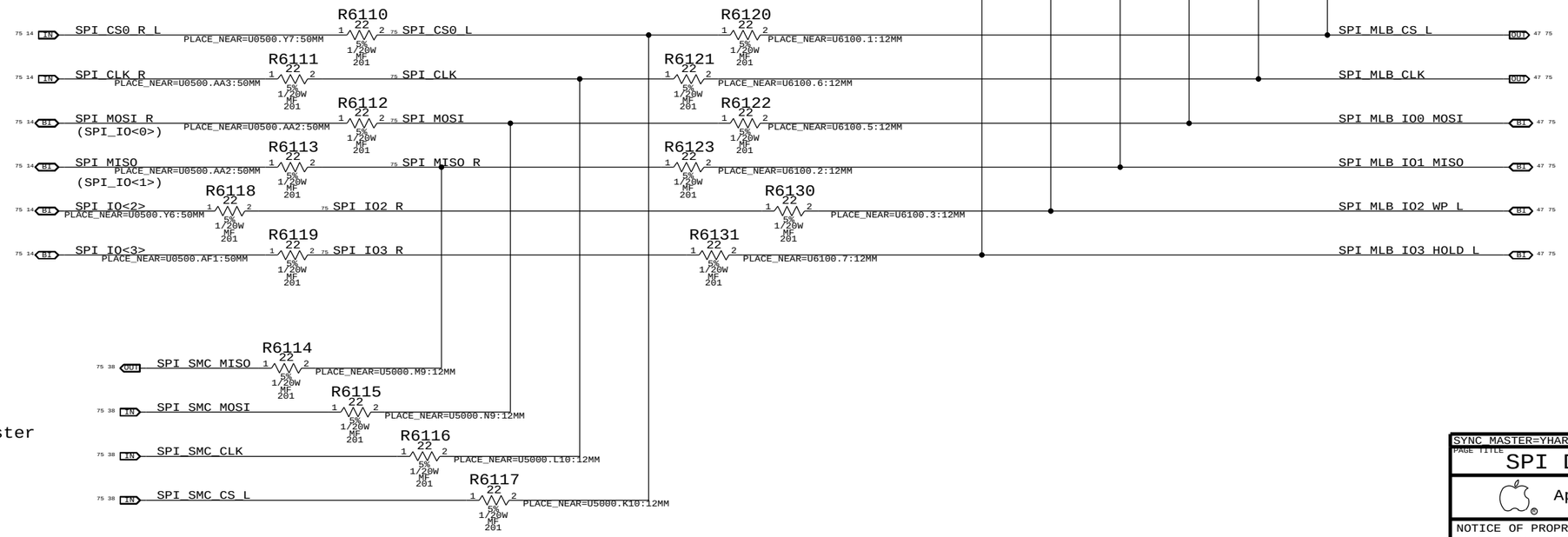
SPI+SWD SAM Connector



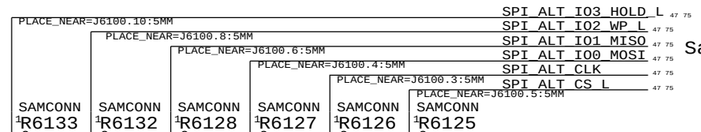
SPI Bus Series Termination

CPU Master

SMC12 Master



Sam Card ROM Slave



SPI ROM Slave

BOM_COST_GROUP=CPU SUPPORT

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/09/2013

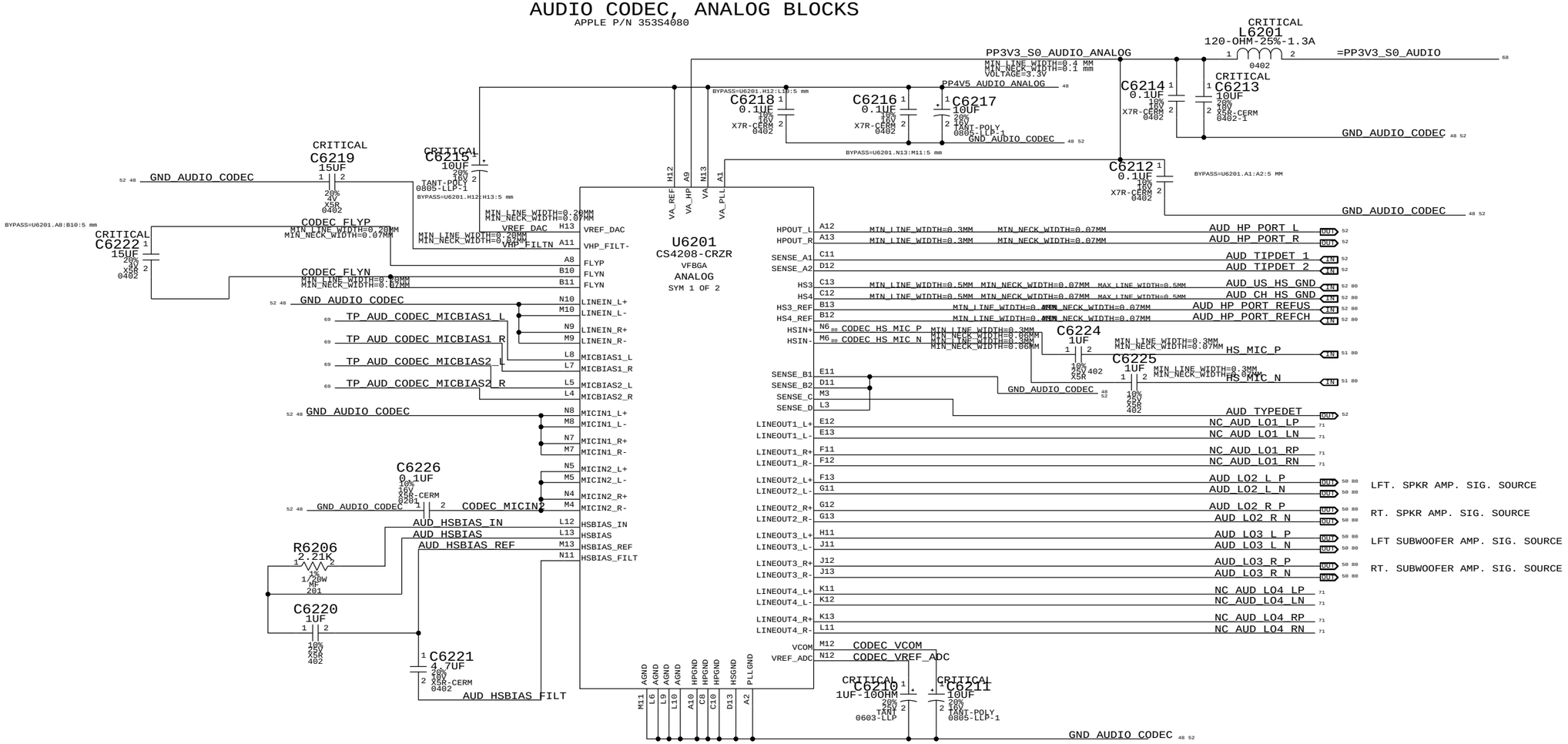
PAGE TITLE: SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D
REVISION: 8.0.0
BRANCH: dvt1
PAGE: 61 OF 120
SHEET: 47 OF 82

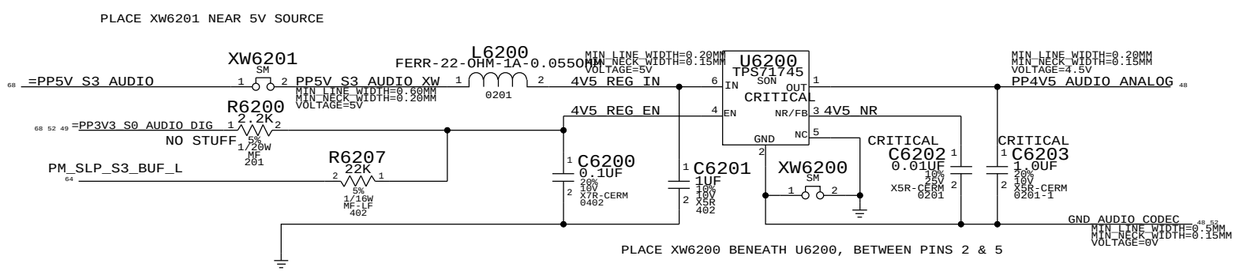
AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



SYNC_MASTER=JCURCIO_J44	SYNC_DATE=05/13/2013
PAGE TITLE	Audio: Codec,Analog
	Apple Inc.
DRAWING NUMBER	051-1573
SIZE	D
REVISION	8.0.0
BRANCH	dvt1
PAGE	62 OF 120
SHEET	48 OF 82

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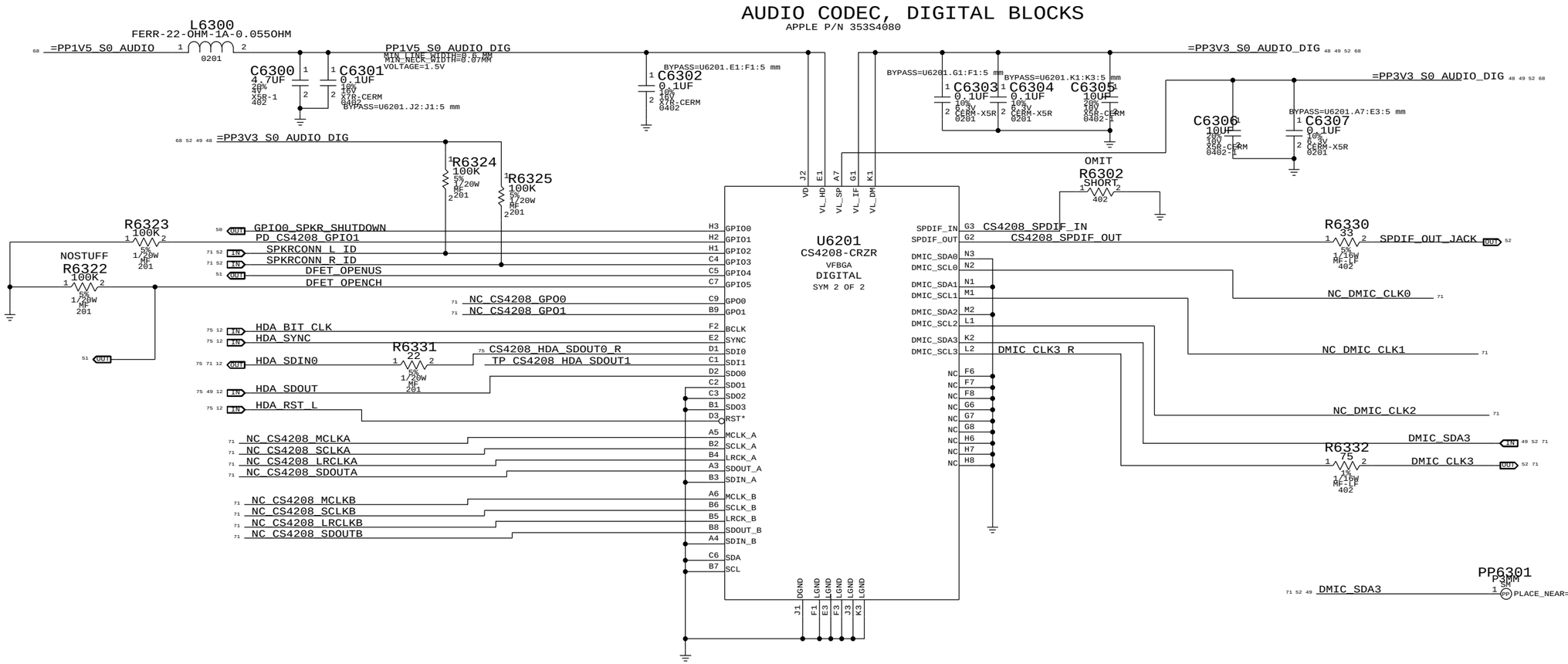
BOM_COST_GROUP=AUDIO

AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080

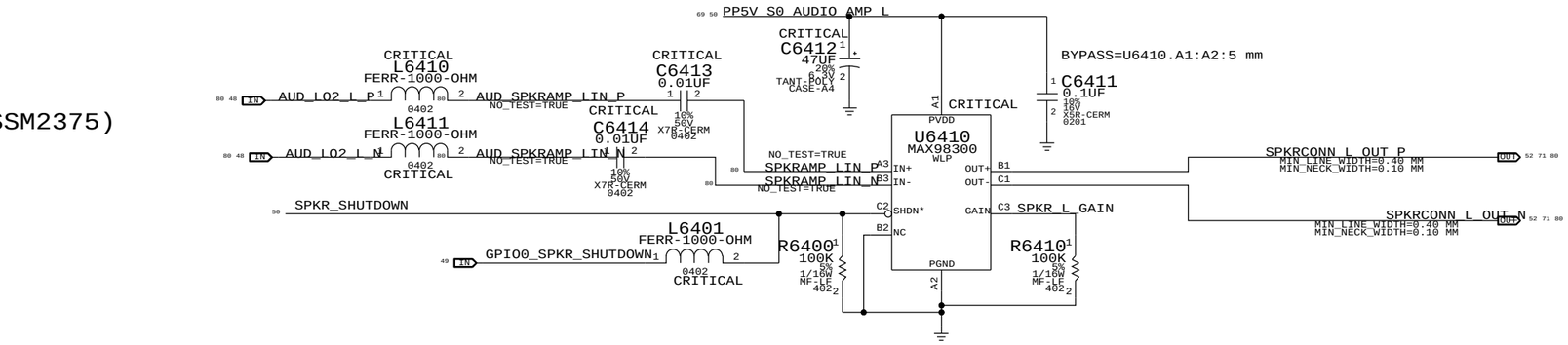


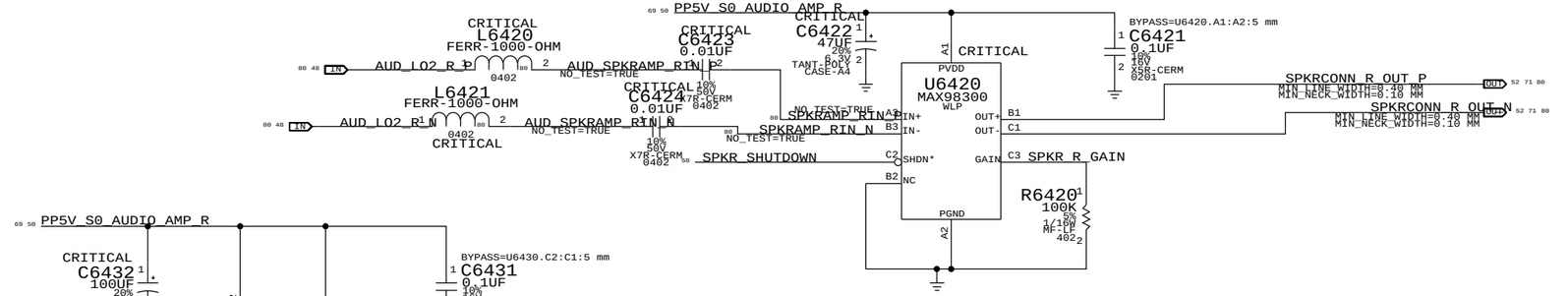
SYNC_MASTER=JCURCIO_J44	SYNC_DATE=07/25/2013
PAGE TITLE	Audio: Codec,Digital
Apple Inc.	DRAWING NUMBER 051-1573 · SIZE D
	REVISION 8.0.0
	BRANCH dvt1
	PAGE 63 OF 120
	SHEET 49 OF 82

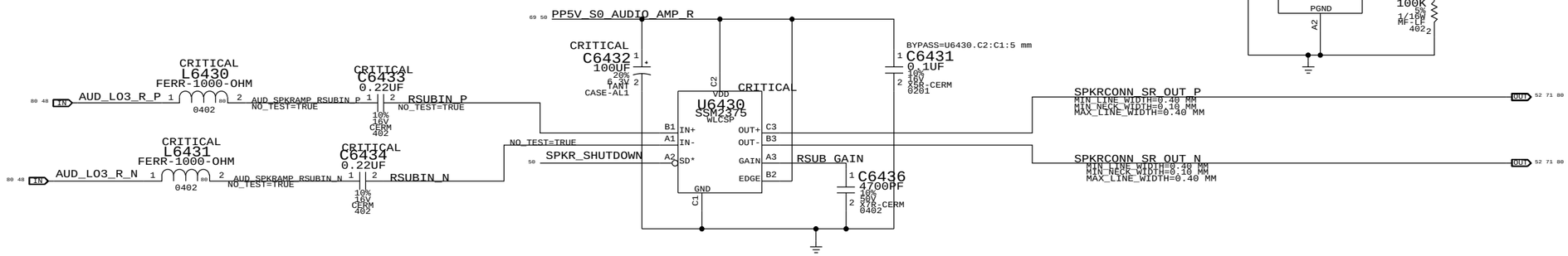
BOM_COST_GROUP=AUDIO

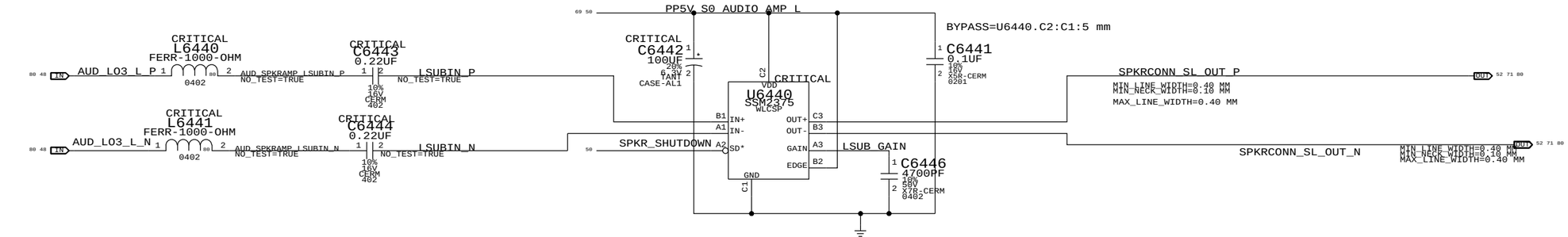
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)

APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









Placement Note: Place C6447 and C6452 near U6420

NC C6447 0.0022UF 10% 50V CERM-X7R 0603 NC
NC C6452 0.0022UF 10% 50V CERM-X7R 0603 NC

Placement Note: Place C6448 and C6449 near U6430

NC C6448 0.0022UF 10% 50V CERM-X7R 0603 NC
NC C6449 0.0022UF 10% 50V CERM-X7R 0603 NC

Placement Note: Place C6450 near U6410

NC C6450 0.0022UF 10% 50V CERM-X7R 0603 NC

Placement Note: Place C6451 near U6440

NC C6451 0.0022UF 10% 50V CERM-X7R 0603 NC

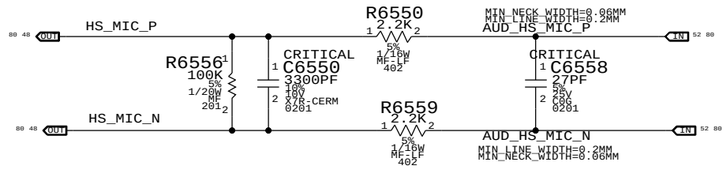
BOM_COST_GROUP=AUDIO

SYNC_MASTER=DIRK_J44 SYNC_DATE=01/09/2013

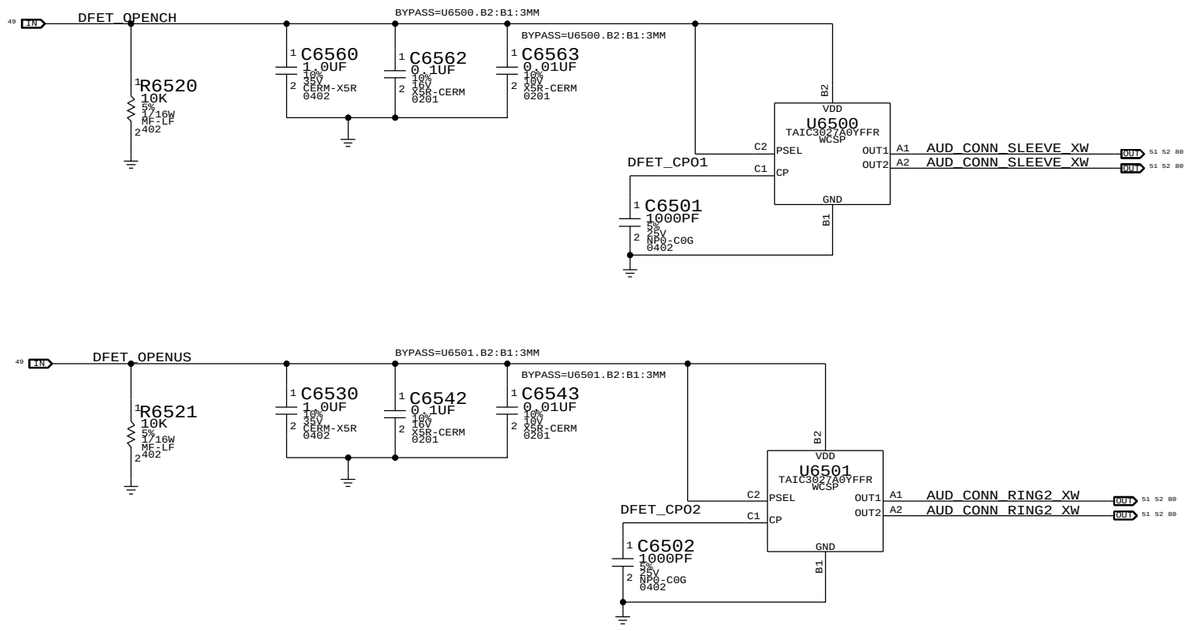
PAGE TITLE: Audio: Speaker Amps

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D
REVISION: 8.0.0
BRANCH: dvt1
PAGE: 64 OF 120
SHEET: 50 OF 82



R/C6550 FILTER TO ADDRESS OUT-OF-BAND
NOISE ISSUE SEEN ON EARLY HEADSETS
(SEE RADAR # 6210118)



BOM_COST_GROUP=AUDIO

SYNC_MASTER=JCURCIO_J44 SYNC_DATE=07/25/2013

PAGE TITLE
Audio: Jack Support

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
PAGE 65 OF 120
SHEET 51 OF 82

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2 INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3 INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4 OUTPUT	HIGH = DFETS OPEN

2-MIC CONNECTOR

APN: 518S0818

68 52 49 48 =PP3V3_S0_AUDIO_DIG

71 49 OUT DMIC_SDA3

OMIT
R6680
SHORT
402
71 DMIC_SDA2

71 49 OUT DMIC_CLK3

CRITICAL
J6601
FF14A-6C-R11DL-B-3H
F-RT-SM
7 1 2 3 4 5 6 8

SPEAKER CONNECTOR

HP=80HZ

APN: 518S0672

CRITICAL
J6602
78171-6006
M-RT-SM
7 1 2 3 4 5 6 8

80 71 58 IN SPKRCONN_L_OUT_P
80 71 58 IN SPKRCONN_L_OUT_N
71 49 IN SPKRCONN_L_ID
80 71 58 IN SPKRCONN_SL_OUT_P
80 71 58 IN SPKRCONN_SL_OUT_N

CRITICAL
J6603
78171-6006
M-RT-SM
7 1 2 3 4 5 6 8

80 71 58 IN SPKRCONN_R_OUT_P
80 71 58 IN SPKRCONN_R_OUT_N
71 49 IN SPKRCONN_R_ID
80 71 58 IN SPKRCONN_SR_OUT_P
80 71 58 IN SPKRCONN_SR_OUT_N

80 48 OUT AUD_HP_PORT_REFCH — CRITICAL L6611 120-OHM-25%-1.3A 0402 — 80 AUD_CONN_SLEEVE
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.06MM
PLACE_NEAR=J6600.5:5mm XW6600 SM

80 48 OUT AUD_CH_HS_GND — CRITICAL L6612 120-OHM-25%-1.3A 0402 — 80 51 AUD_CONN_SLEEVE_XW
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.1MM
XW6601 SM
80 51 OUT AUD_HS_MIC_P

80 48 OUT AUD_HP_PORT_REFUS — CRITICAL L6613 120-OHM-25%-1.3A 0402 — 80 AUD_CONN_RING2
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.06MM
PLACE_NEAR=J6600.6:5mm XW6602 SM

80 48 OUT AUD_US_HS_GND — CRITICAL L6614 120-OHM-25%-1.3A 0402 — 80 51 AUD_CONN_RING2_XW
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.1MM
XW6603 SM
80 51 OUT AUD_HS_MIC_N

48 IN AUD_HP_PORT_L — R6602 2.2K 5% 1/16W MF-LF 402 — CRITICAL L6604 120-OHM-25%-1.3A 0402 — AUD_CONN_HP_LEFT
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.06MM

GND_AUDIO_CODEC

R6603 2.2K 5% 1/16W MF-LF 402

48 OUT AUD_TIPDET_2 — CRITICAL L6608 FERR-470-OHM 0201 — AUD_CONN_TIPDET_2

48 OUT AUD_TIPDET_1 — CRITICAL L6607 FERR-470-OHM 0201 — AUD_CONN_TIPDET_1

48 IN AUD_HP_PORT_R — CRITICAL L6605 120-OHM-25%-1.3A 0402 — AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.06MM

48 OUT AUD_TYPEDET — CRITICAL L6606 FERR-470-OHM 0201 — AUD_CONN_TYPEDET

49 IN SPDIF_OUT_JACK

68 52 49 48 =PP3V3_S0_AUDIO_DIG

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH

5 MIC
6 AUDIO GND
2 2RTN
1 DET2
8 DET1
NC
7 1RTN
3 R.AUDIO
4 AUDIO GND
AUDIO

9 VIN
10 VDD
11 GND
OPERATING VOLTAGE 3.3
POF

C6600 1UF 10% 10V X5R 402
C6601 0.1UF 10% 6.3V CERM-X5R 0201
12 13 14 15 SHELL PINS

R6601 10K 5% 1/16W MF-LF 402

C6602 100PF 5% 25V C0G 0201
CRITICAL DZ6607 ESDALC5-1BM2 SOD882
C6603 100PF 5% 25V C0G 0201
CRITICAL DZ6601 ESDALC5-1BM2 SOD882
C6604 100PF 5% 25V C0G 0201
CRITICAL DZ6602 ESDALC5-1BM2 SOD882
C6605 100PF 5% 25V C0G 0201
CRITICAL DZ6603 ESDALC5-1BM2 SOD882
C6606 100PF 5% 25V C0G 0201
CRITICAL DZ6606 ESDALC5-1BM2 SOD882
CRITICAL DZ6605 ESDALC5-1BM2 SOD882
C6607 100PF 5% 25V C0G 0201
C6608 100PF 5% 25V C0G 0201
CRITICAL DZ6604 ESDALC5-1BM2 SOD882

BOM_COST_GROUP=AUDIO

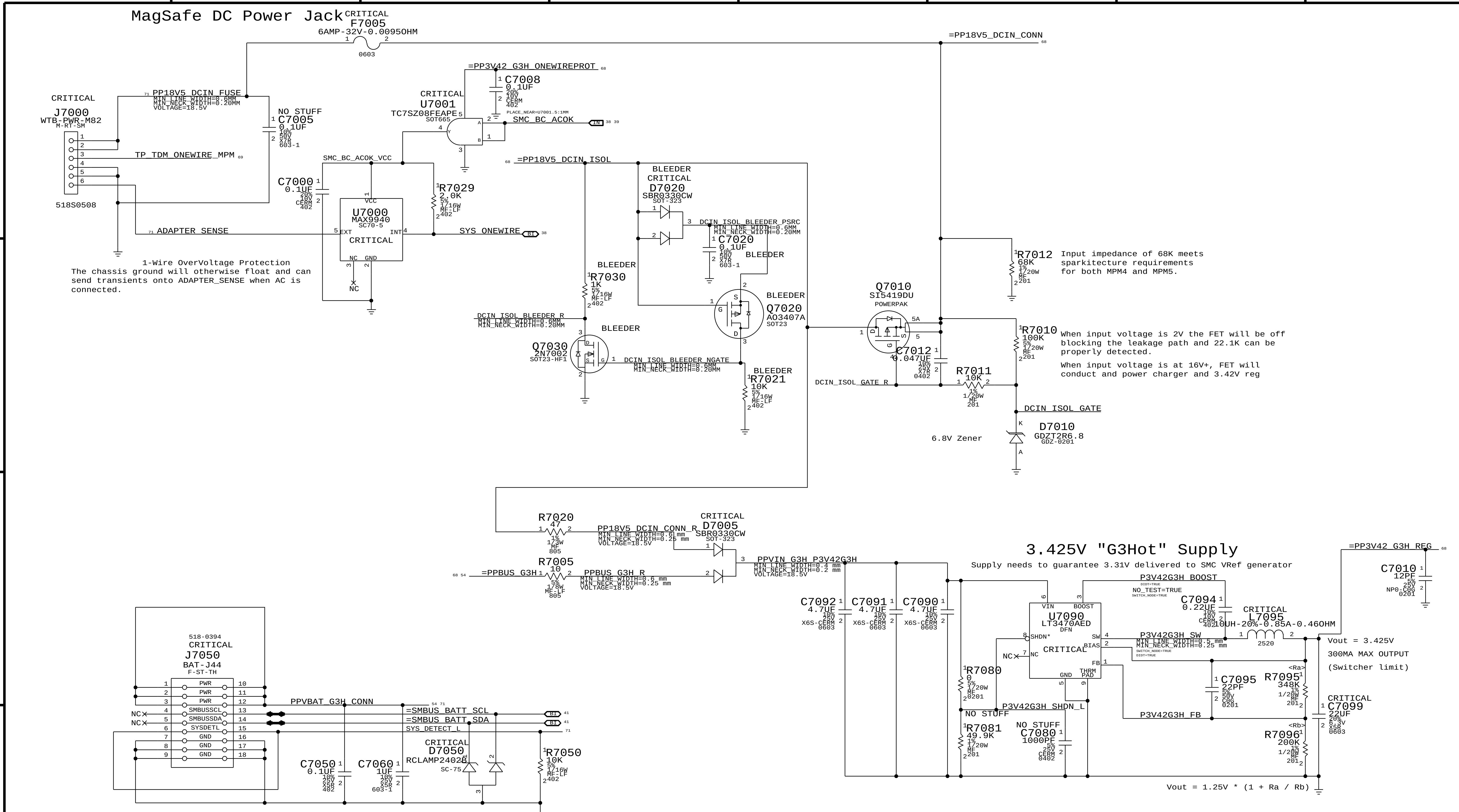
SYNC_MASTER=JCURCIO_J44 SYNC_DATE=05/13/2013

PAGE TITLE
Audio: Jack Translators

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D
REVISION 8.0.0
BRANCH dvt1
PAGE 66 OF 120
SHEET 52 OF 82

MagSafe DC Power Jack



SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/09/2013

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER	SIZE
051-1573	D

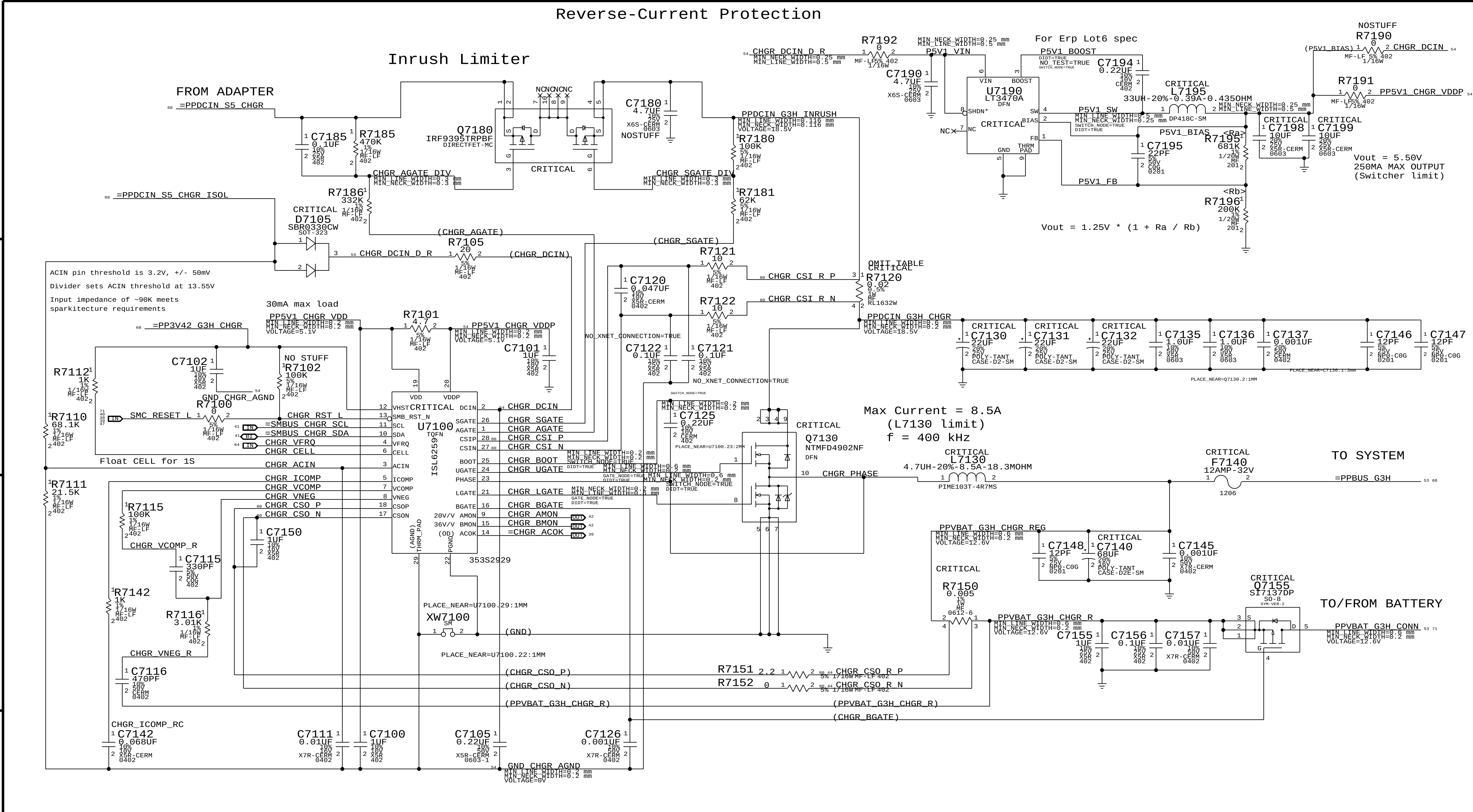
REVISION: 8.0.0

BRANCH: dvt1

PAGE: 70 OF 120

SHEET: 53 OF 82

BOM_COST_GROUP=POWER



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0387	1	RES,MTL FILM,1W,20MOHM,0.5%,0612,LF,BLK	R7120	CRITICAL	

BOM_COST_GROUP=POWER

SYNC_MASTER=AHARTMAN_J52 SYNC_DATE=11/06/2013

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

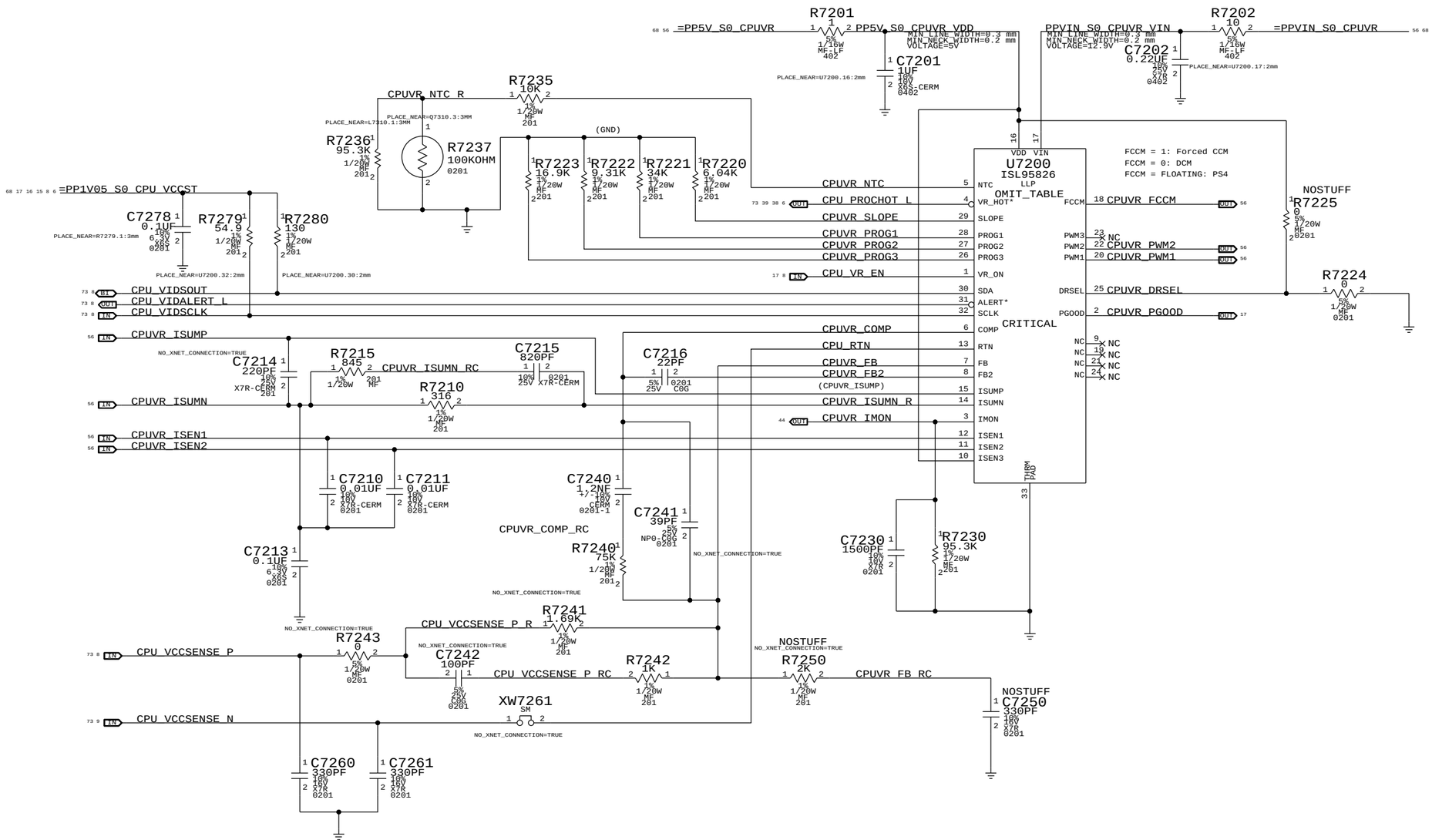
REVISION 8.0.0

BRANCH dvt1

PAGE 71 OF 120

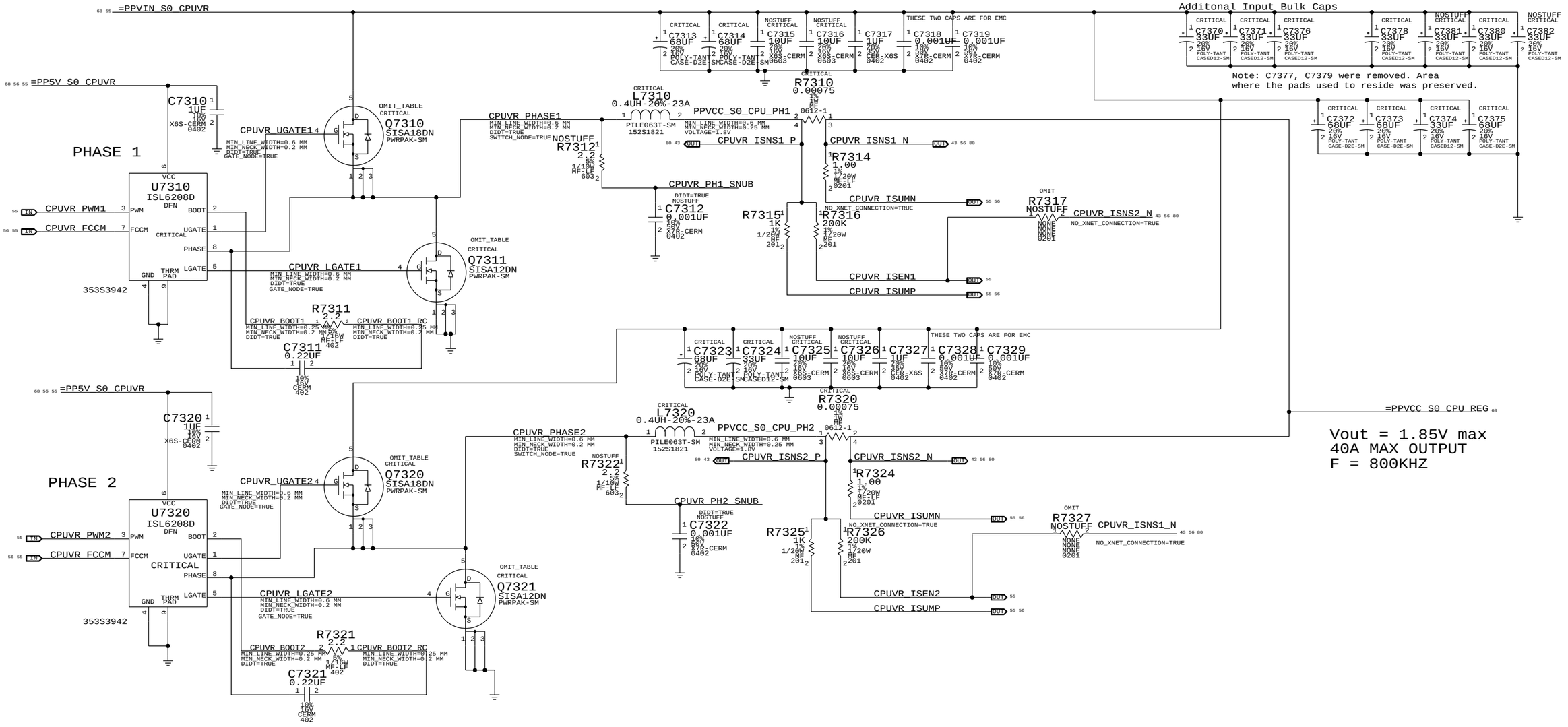
SHEET 54 OF 82

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00036	1	IC,ISL95826AS2378,PWM,PG,VR12.5/6,QFN-32	U7200	CRITICAL	



BOM_COST_GROUP=POWER

SYNC_MASTER=J41	SYNC_DATE=10/23/2012
PAGE TITLE	CPU VR12.6 VCC Regulator IC
Apple Inc.	DRAWING NUMBER 051-1573 · SIZE D
	REVISION 8.0.0
	BRANCH dvt1
	PAGE 72 OF 120
	SHEET 55 OF 82



SYNC_MASTER=J41 SYNC_DATE=10/23/2012

PAGE TITLE: CPU VR12.6 VCC Power Stage

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

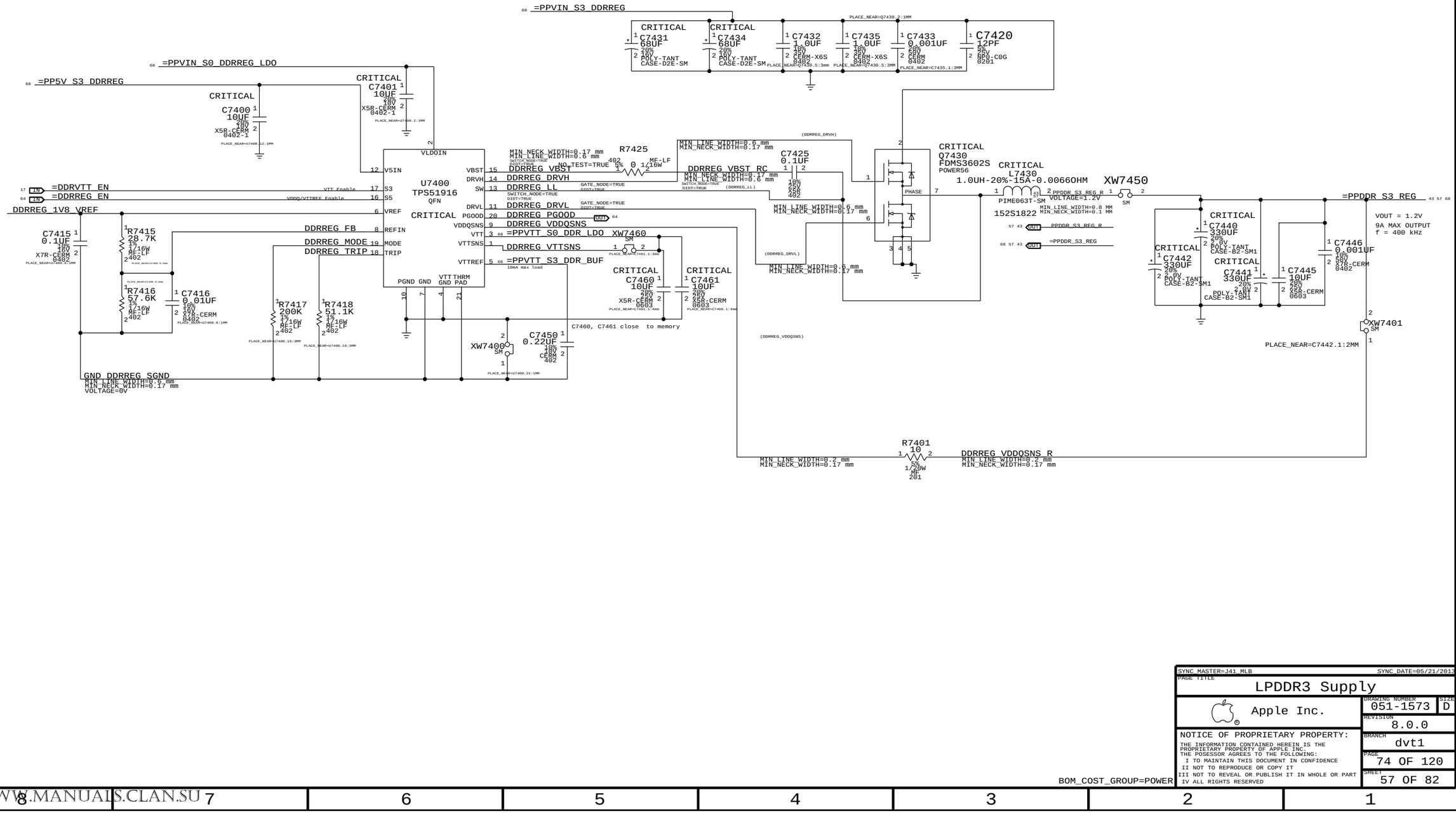
BRANCH: dvt1

PAGE: 73 OF 120

SHEET: 56 OF 82

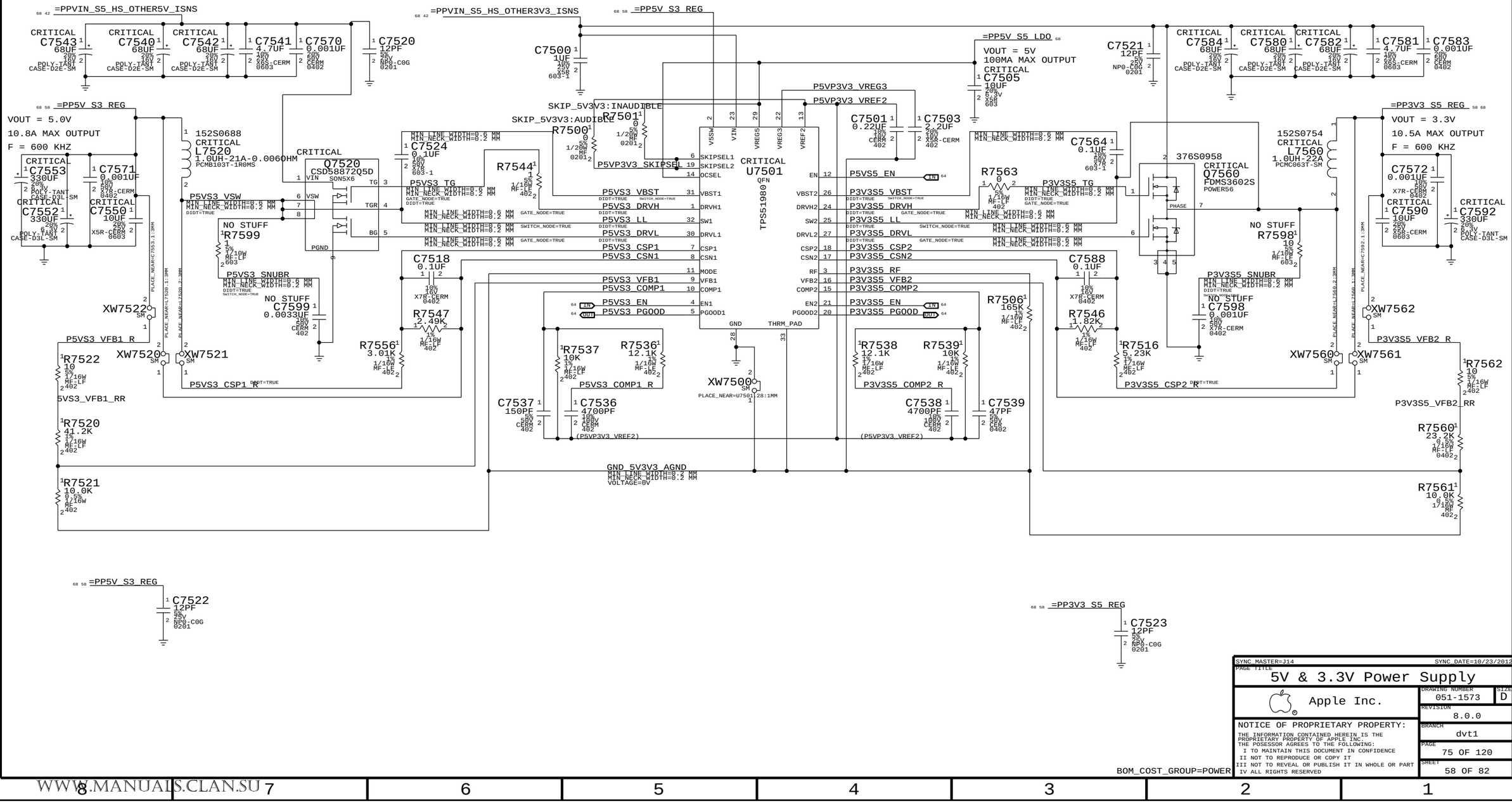
BOM_COST_GROUP=POWER

1.2V S3 Regulator

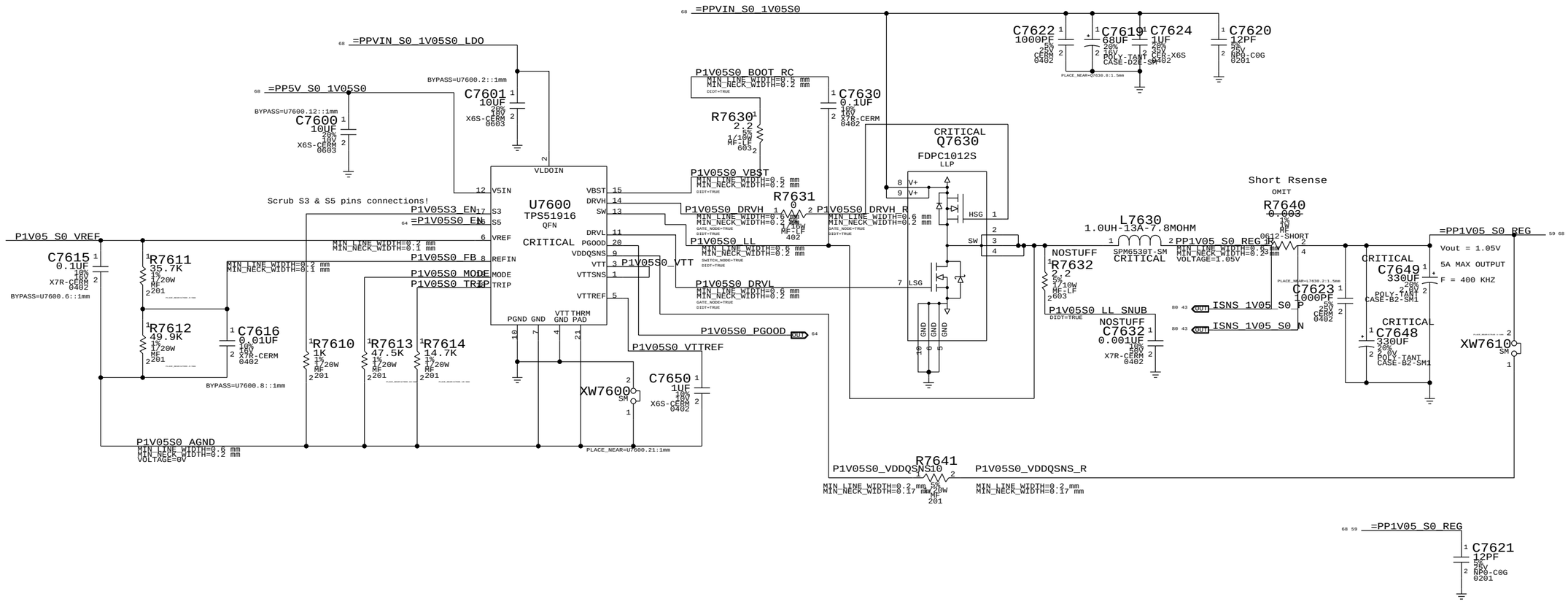


SYNC_MASTER=J41_MLB	SYNC_DATE=05/21/2013
PAGE TITLE	LPDDR3 Supply
Apple Inc.	DRAWING NUMBER 051-1573 · SIZE D
	REVISION 8.0.0
	BRANCH dvt1
	PAGE 74 OF 120
	SHEET 57 OF 82

BOM_COST_GROUP=POWER



1.05V S0 Regulator



SYNC_MASTER=AHARTMAN_J52	SYNC_DATE=10/29/2013
PAGE TITLE	1.05V Power Supply
Apple Inc.	DRAWING NUMBER 051-1573 · SIZE D
	REVISION 8.0.0
	BRANCH dvt1
	PAGE 76 OF 120
	SHEET 59 OF 82

BOM_COST_GROUP=POWER

Page Notes

Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)
- =PP5V_S0SW_KBDLED (5V KEYBOARD BACKLIGHT INPUT)

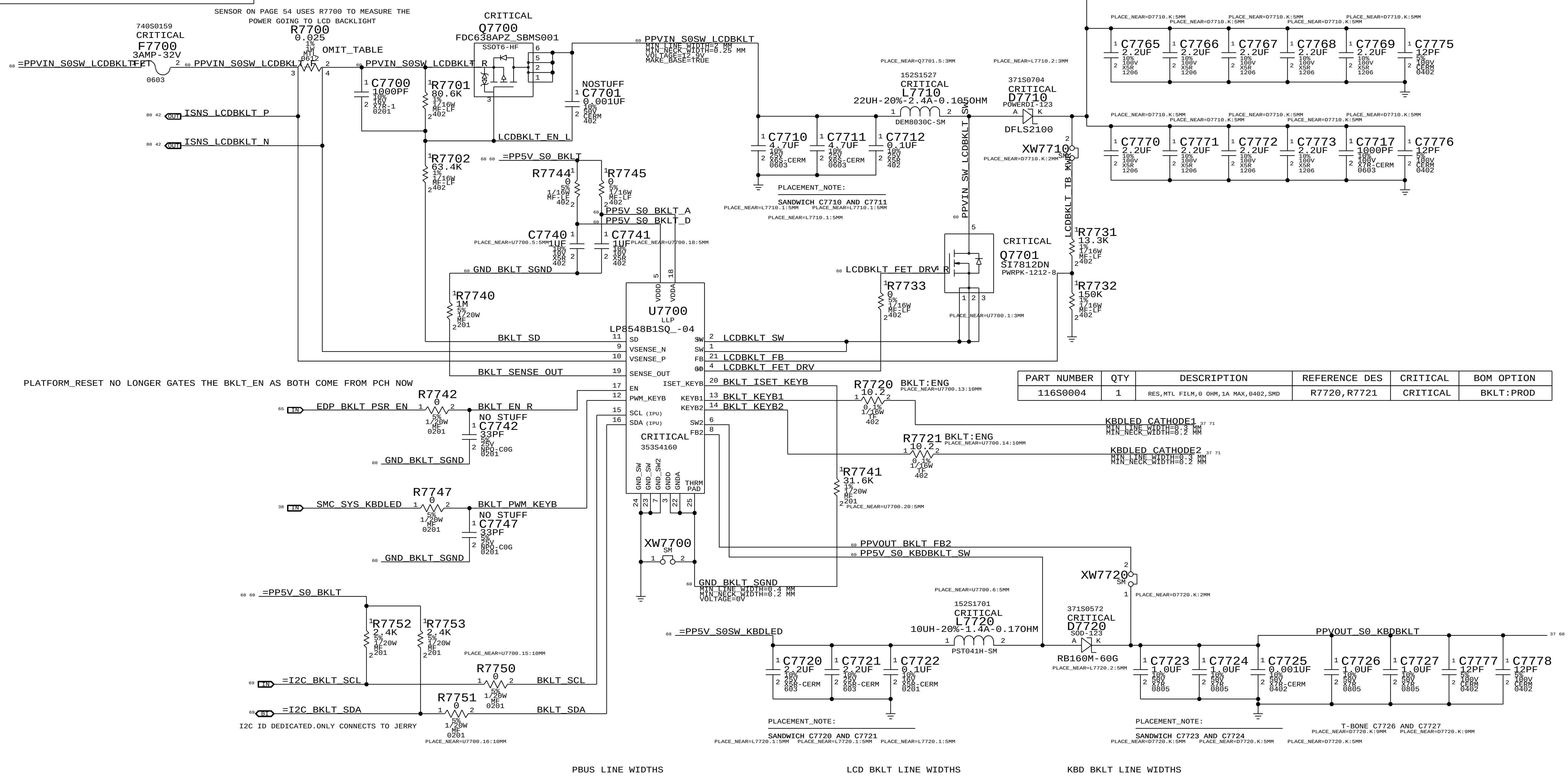
BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0386	1	RES,MTL FILM,1W,25MOHM,1%,4TERM,0612,BLK	R7700	CRITICAL	

SENSOR ON PAGE 54 USES R7700 TO MEASURE THE POWER GOING TO LCD BACKLIGHT

PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD



PBUS LINE WIDTHS

PP5V_S0_BKLT_A MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=5V

PP5V_S0_BKLT_D MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=5V

PPVIN_S0SW_LCDBKLT_F MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=12.9V

PPVIN_S0SW_LCDBKLT_R MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=12.9V

PPVIN_S0SW_LCDBKLT_FET MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=12.9V

PPVIN_S0SW_LCDBKLT MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=12.9V

LCD BKLT LINE WIDTHS

LCDBKLT_FET_DRV_R MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=5V GATE_NODE=TRUE DIDT=TRUE

LCDBKLT_FET_DRV MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=5V GATE_NODE=TRUE DIDT=TRUE

LCDBKLT_SW MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=53V SWITCH_NODE=TRUE DIDT=TRUE

PPVIN_SW_LCDBKLT_SW MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=53V SWITCH_NODE=TRUE DIDT=TRUE

PPVOUT_S0_LCDBKLT MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=53V

PPVOUT_BKLT_FB MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=53V

KBD BKLT LINE WIDTHS

PP5V_S0_KBDBKLT_SW MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=40V SWITCH_NODE=TRUE DIDT=TRUE

PPVOUT_S0_KBDBKLT MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=40V

PPVOUT_BKLT_FB2 MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=40V

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=SHART_J44 SYNC_DATE=11/20/2012

PAGE TITLE
LCD & KBD Backlight Driver

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

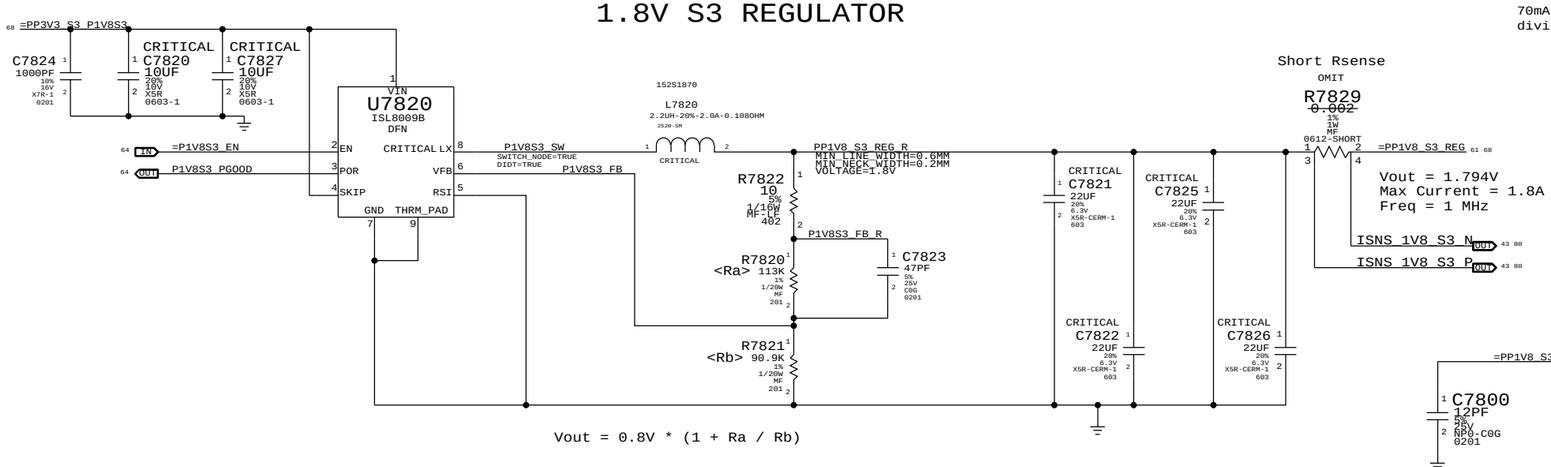
REVISION 8.0.0

BRANCH dvt1

PAGE 77 OF 120

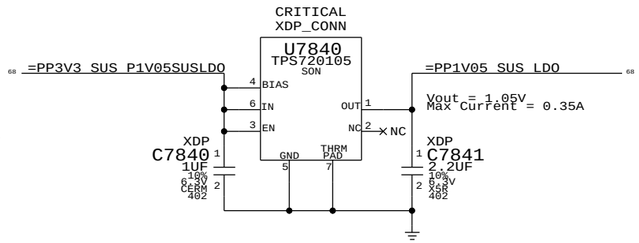
SHEET 60 OF 82

1.8V S3 REGULATOR

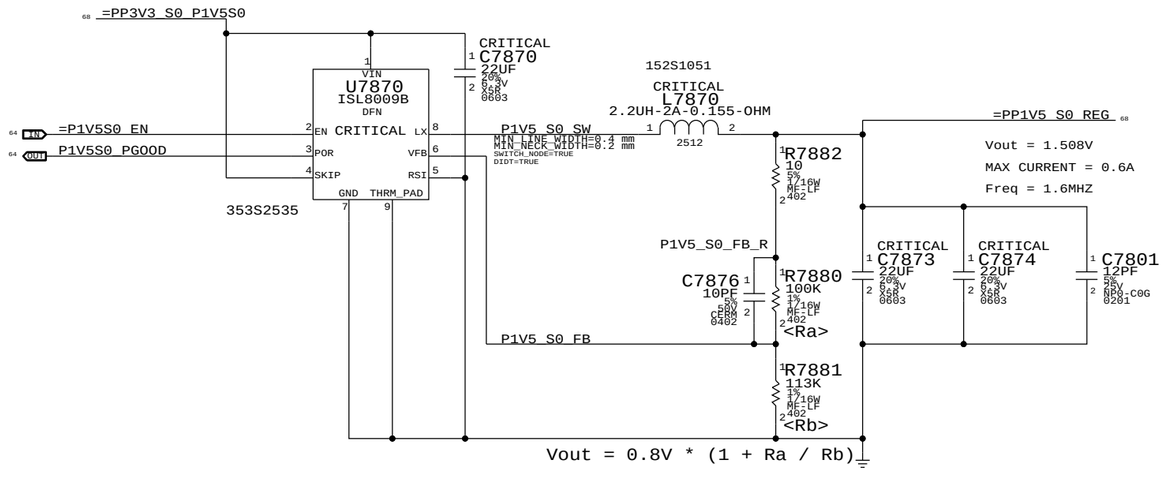


1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 Switcher



SYNC_MASTER=AHARTMAN_J52 SYNC_DATE=11/06/2013

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

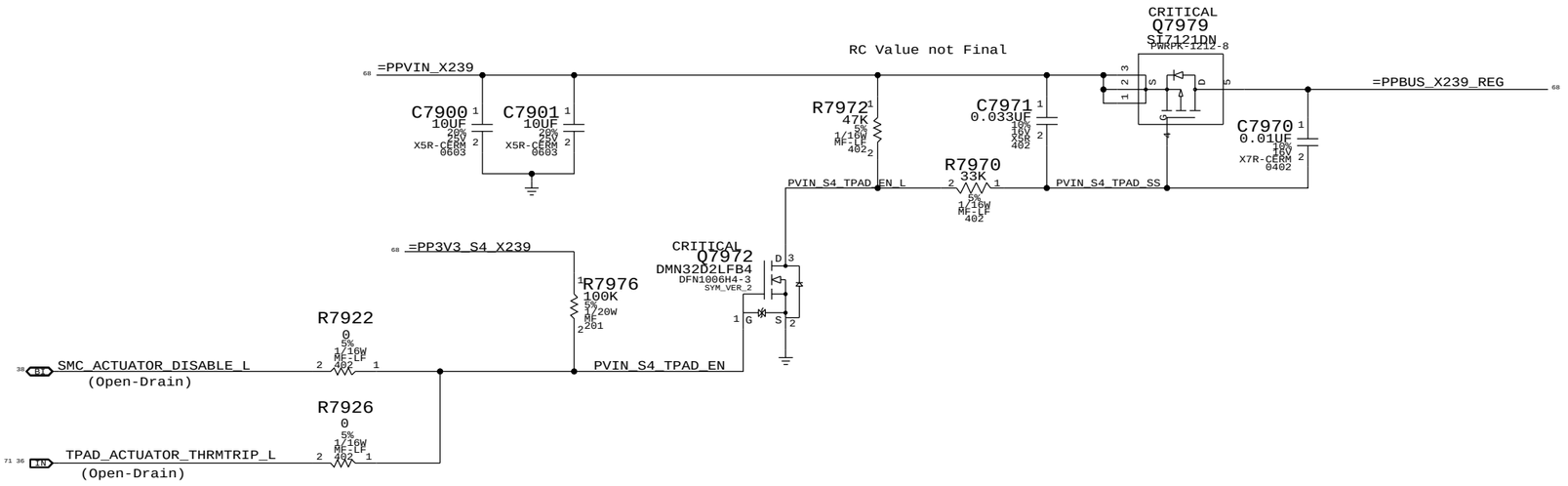
REVISION: 8.0.0

BRANCH: dvt1

PAGE: 78 OF 120

SHEET: 61 OF 82

BOM_COST_GROUP=POWER



BOM_COST_GROUP=TRACKPAD

SYNC_MASTER=AHARTMAN_J52 SYNC_DATE=11/06/2013

PAGE TITLE: X239 Power Supply

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

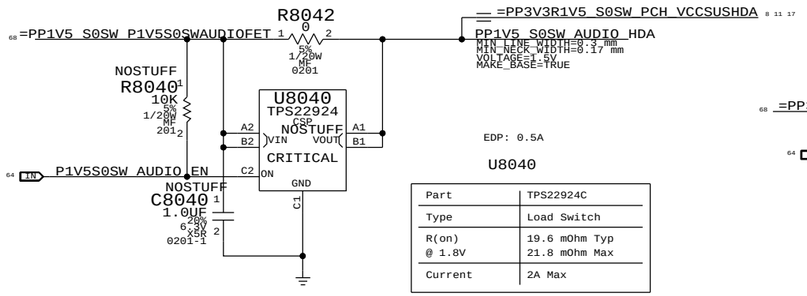
BRANCH: dvt1

PAGE: 79 OF 120

SHEET: 62 OF 82

1.5V S0 Audio Switch (BYPASSED)

Loading specs per J41/43_PowerBudget_Riviera_rev0.99e

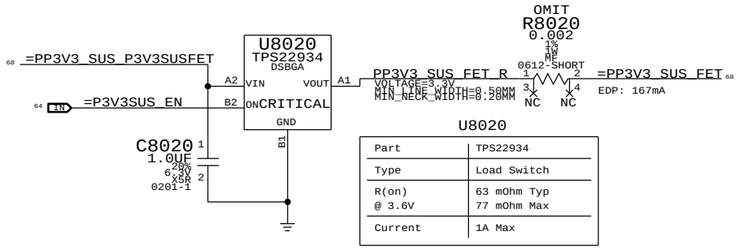


EDP: 0.5A

U8040

Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

3.3V SUS Switch

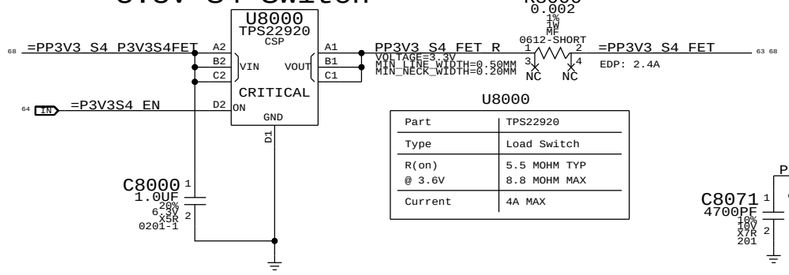


EDP: 167mA

U8020

Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max

3.3V S4 Switch

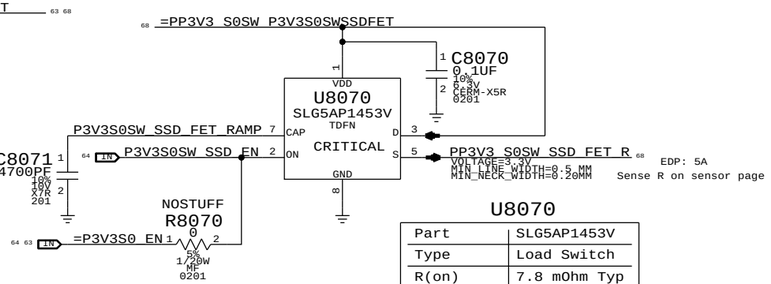


EDP: 2.4A

U8000

Part	TPS22920
Type	Load Switch
R(on) @ 3.6V	5.5 MOHM TYP 8.8 MOHM MAX
Current	4A MAX

3.3V SSD Switch



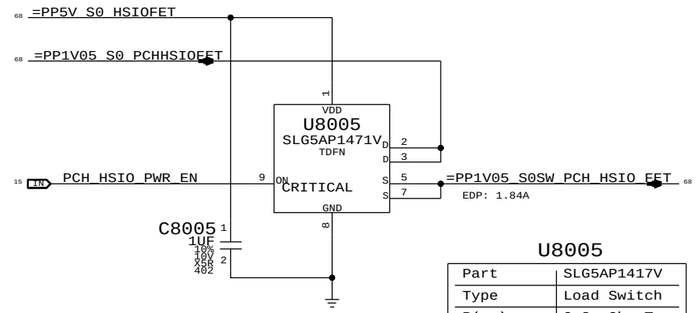
EDP: 5A

Sense R on sensor page

U8070

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

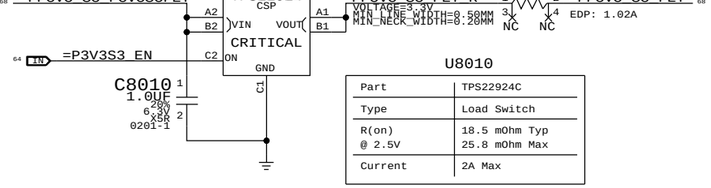
1.05V PCH HSIO Switch



U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

3.3V S3 Switch

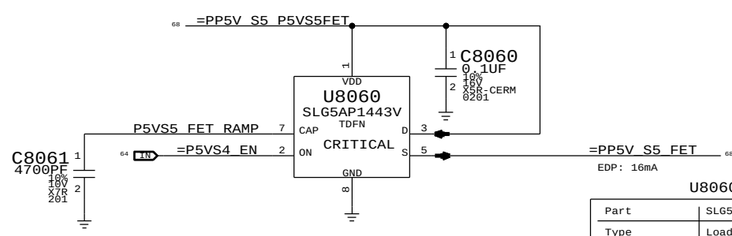


EDP: 1.02A

U8010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

5V S4 Switch



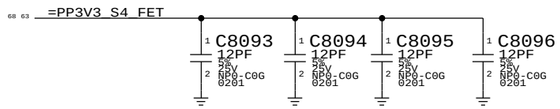
EDP: 16mA

U8060

Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ 19 mOhm Max
Current	2.5A

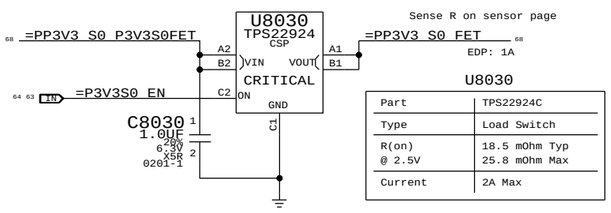
REMOVED THE ANALOG POWER GATE AS SLG5AP1471 SHOULD BE AVAILABLE BY THEN

CAPACITORS ADDED FOR NOISE FLOOR REASONS:



Placement Note: Place C8090, C8091 and C8092 near U8000

3.3V S0 Switch



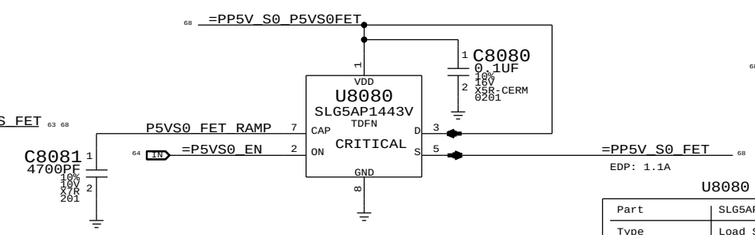
Sense R on sensor page

EDP: 1A

U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

5V S0 Switch

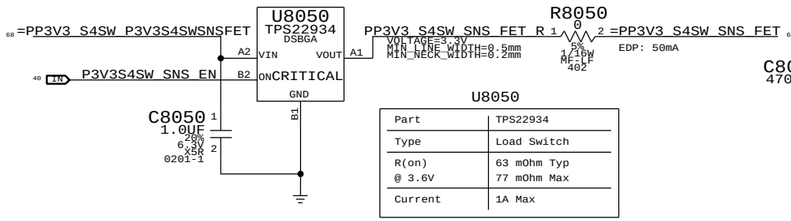


EDP: 1.1A

U8080

Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ 19 mOhm Max
Current	2.5A

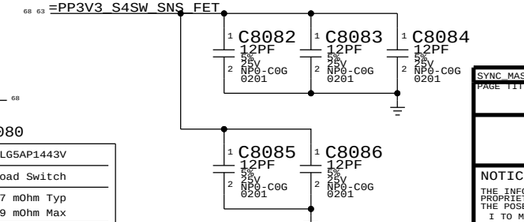
3.3V Sensor Switch



EDP: 50mA

U8050

Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max



BOM_COST_GROUP=POWER

SYNC_MASTER=J41 SYNC_DATE=10/23/2012

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

REVISION 8.0.0

BRANCH dvt1

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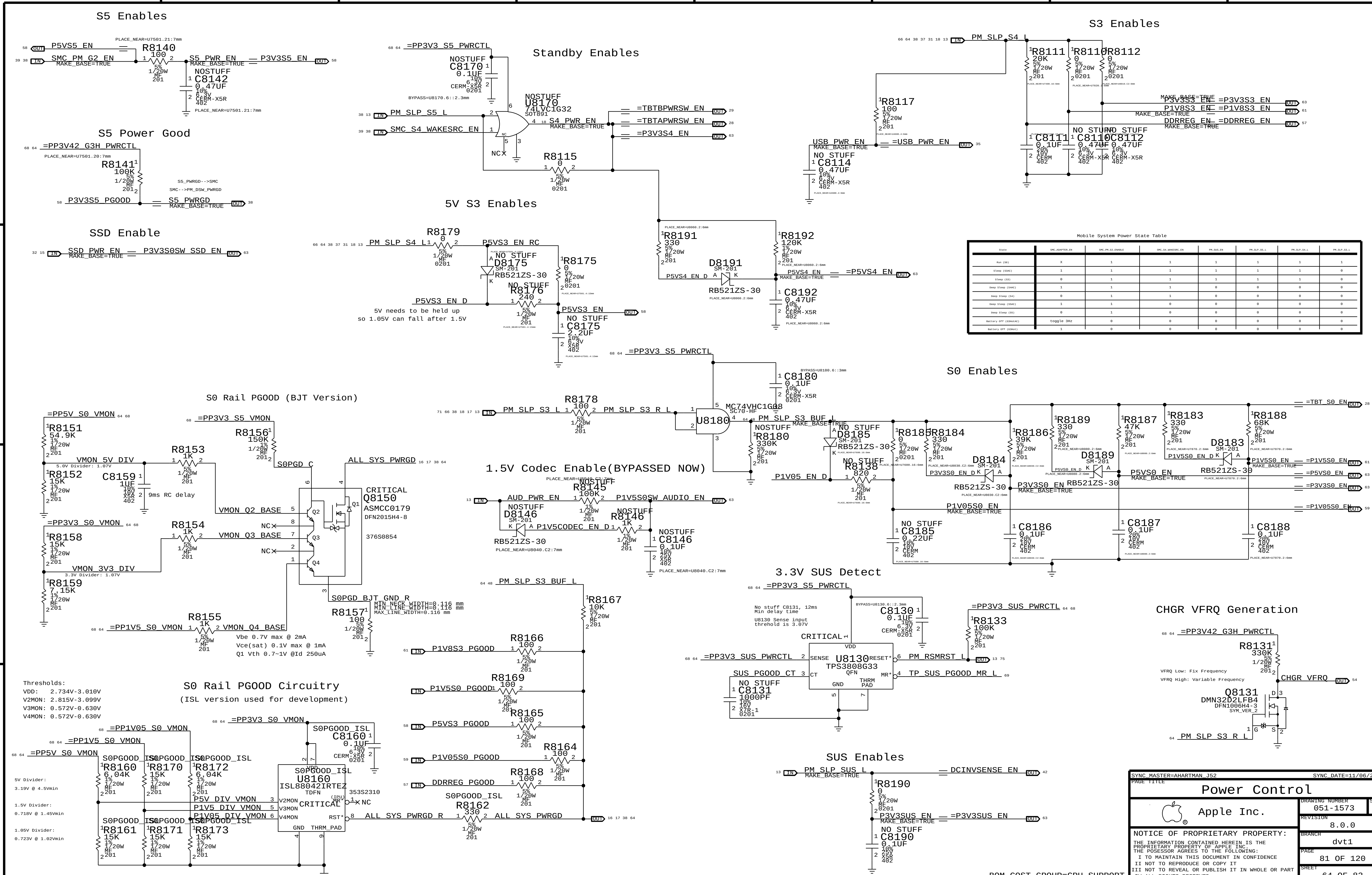
SHEET 63 OF 82



Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

SYNC_MASTER=AHARTMAN_J52 SYNC_DATE=11/06/2013

PAGE TITLE

Power Control

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

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BRANCH dvt1

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LCD PANEL INTERFACE (eDP)

LCD_HPD_CONN IS A 2.5V SIGNAL
NEEDS TO BE LEVEL SHIFTED TO 3.3V

=PP3V3_S0_PCH_GPIO

C8330 0.1UF 10% 16V CERM-X5R 0201 BYPASS=U8330.8!::3MM NOSTUFF

U8330 SOT833 74LVC2G32GT

EDP_BKLT_EN
LCD_PSR_EN
EDP_PANEL_PWR
EDP_BKLT_PSR_EN
EDP_PANEL_PWR_OR_PSR_EN

R8310 100K 5% 1/10W MF-LF 0402
R8309 100K 5% 1/10W MF-LF 0402

R8330 0 5% 1/20W MF 0201 NO STUFF
R8331 0 5% 1/20W MF 0201 NO STUFF

PANEL USES EDP_PANEL_PWR_PSR_EN TO DISCHARGE THE LCD BEFORE POWER GOES AWAY

Y = B

U8340 SOT891 74AUP1T97 PANEL:OLD
C8340 0.1UF 10% 16V X5R-CERM 0201 BYPASS=U8340.5::3MM

R8340 100K 5% 1/10W MF-LF 0402
R8341 0 5% 1/20W MF 0201 PANEL:NEW
R8342 10K 5% 1/20W MF 0201 VOLTAGE=3.3V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.2 mm OMIT_TABLE

PP3V3_S0_EDP_SW
C8304 0.1UF 10% 16V CERM-X5R 0201 BYPASS=J8300.5::5MM

DP_INT_HPD

EDP_LS_CAP C8350 12PF 5% NP0-C0G 0201 25V
EDP_LS_CAP C8351 12PF 5% NP0-C0G 0201 25V
EDP_LS_CAP C8352 12PF 5% NP0-C0G 0201 25V
EDP_LS_CAP C8353 12PF 5% NP0-C0G 0201 25V
EDP_LS_CAP C8354 12PF 5% NP0-C0G 0201 25V
EDP_LS_CAP C8355 12PF 5% NP0-C0G 0201 25V
EDP_LS_CAP C8356 12PF 5% NP0-C0G 0201 25V
EDP_LS_CAP C8357 12PF 5% NP0-C0G 0201 25V
EDP_LS_CAP C8358 12PF 5% NP0-C0G 0201 25V
EDP_LS_CAP C8359 12PF 5% NP0-C0G 0201 25V

CRITICAL
J8300 20525-130E-01 F-RT-SM

PPVOUT_S0_LCDBKLT
I2C_BKLT_SCL
I2C_BKLT_SDA
PP3V3_S0_EDP_R
=I2C_TCON_SCL
=I2C_TCON_SDA
EDP_BKLT_PWM
LCD_HPD_CONN
NC

3.3V TCON Switch

=PP3V3_S0_EDP

R8321 24.9K 1% 1/20W MF 201
R8322 4.32K 1% 1/20W MF 201
D8322 SM-201 RB521ZS-30
C8308 1.0UF 10% 6.3V X5R 0201-1
C8318 1UF 10% 6.3V CERM 402

U8310 TPS22904 CSP CRITICAL
PP3V3_S0_EDP_SW VOLTAGE=3.3V MIN_LINE_WIDTH=0.50MM MIN_NECK_WIDTH=0.20MM

EDP: 1.02A

U8310

Part	TPS22904
Type	Load Switch
R(on) @ 2.5V	75 mOhm Typ 95 mOhm Max
Current	0.5A Max

LCD_IRQ_L

DP_INT_AUXCH_C_P
DP_INT_AUXCH_C_N
C8328 0.1UF 10% 16V X5R-CERM 0201
C8329 0.1UF 10% 16V X5R-CERM 0201

DP_INT_AUX_P
DP_INT_AUX_N

DP_INT_ML_C_P<0>
DP_INT_ML_C_N<0>
DP_INT_ML_C_P<1>
DP_INT_ML_C_N<1>
DP_INT_ML_C_P<2>
DP_INT_ML_C_N<2>
DP_INT_ML_C_P<3>
DP_INT_ML_C_N<3>
C8320 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
C8321 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
C8322 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
C8323 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
C8324 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
C8325 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
C8326 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
C8327 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE

DP_INT_ML_F_P<0>
DP_INT_ML_F_N<0>
DP_INT_ML_F_P<1>
DP_INT_ML_F_N<1>
DP_INT_ML_F_P<2>
DP_INT_ML_F_N<2>
DP_INT_ML_F_P<3>
DP_INT_ML_F_N<3>
3.25-OHM-0.1A-2.4GHZ TAM0605-4SM
FL8300 FL8301 FL8302 FL8303

DP_INT_ML_P<0>
DP_INT_ML_N<0>
DP_INT_ML_P<1>
DP_INT_ML_N<1>
DP_INT_ML_P<2>
DP_INT_ML_N<2>
DP_INT_ML_P<3>
DP_INT_ML_N<3>

=PP5V_S0_LCD

U8300 SLG5AP1443V TDFN CRITICAL
C8309 0.1UF 10% 16V X7R-CERM 0402

R8319 11K 1% 1/20W MF 201
R8323 3.01K 1% 1/20W MF 201
D8323 SM-201 RB521ZS-30
C8319 1UF 10% 6.3V CERM 402
C8310 4700PF 10% 16V X7R 201
C8311 0.1UF 10% 16V X7R-CERM 0402
C8312 10UF 20% 6.3V X5R 603

PP5V_S0_LCD_FETCAP
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=5V

PP5VR3V3_SW_LCD_ISNS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

OMIT
R8320 0 1W MF 0612-SHORT Short Rsense

ISNS_LCDPANEL_N
ISNS_LCDPANEL_P

PP5VR3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

CRITICAL
L8300 FERR-220-OHM 0805

PP5VR3V3_SW_LCD
C8301 0.1UF 10% 16V X5R-CERM 0201
C8302 0.1UF 10% 16V X5R-CERM 0201
C8305 12PF 5% 100V CERM 0402
C8303 1000PF 10% 16V X7R-CERM 0603
C8300 1000PF 10% 16V X7R-CERM 0603

518S0829

U8300

Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ 19 mOhm Max
Current	2.5A

LCD Panel AUX strapping
S0 Enables

=PP3V3_S0_LCD

R8303 1M 5% 1/20W MF 201 NOSTUFF NO_XNET_CONNECTION=TRUE
R8302 1M 5% 1/20W MF 201 NOSTUFF NO_XNET_CONNECTION=TRUE

R8311 1M 5% 1/20W MF 201 NOSTUFF NO_XNET_CONNECTION=TRUE GND_VOID=TRUE
R8312 1M 5% 1/20W MF 201 NOSTUFF NO_XNET_CONNECTION=TRUE GND_VOID=TRUE
R8313 1M 5% 1/20W MF 201 NOSTUFF NO_XNET_CONNECTION=TRUE GND_VOID=TRUE
R8314 1M 5% 1/20W MF 201 NOSTUFF NO_XNET_CONNECTION=TRUE GND_VOID=TRUE
R8315 1M 5% 1/20W MF 201 NOSTUFF NO_XNET_CONNECTION=TRUE GND_VOID=TRUE
R8316 1M 5% 1/20W MF 201 NOSTUFF NO_XNET_CONNECTION=TRUE GND_VOID=TRUE
R8317 1M 5% 1/20W MF 201 NOSTUFF NO_XNET_CONNECTION=TRUE GND_VOID=TRUE
R8318 1M 5% 1/20W MF 201 NOSTUFF NO_XNET_CONNECTION=TRUE GND_VOID=TRUE

BOM_COST_GROUP=DISPLAY

PP5VR3V3_SW_LCD
C8306 12PF 5% NP0-C0G 0201 25V
C8307 12PF 5% NP0-C0G 0201 25V
C8313 12PF 5% NP0-C0G 0201 25V

PANEL COMPATIBILITY

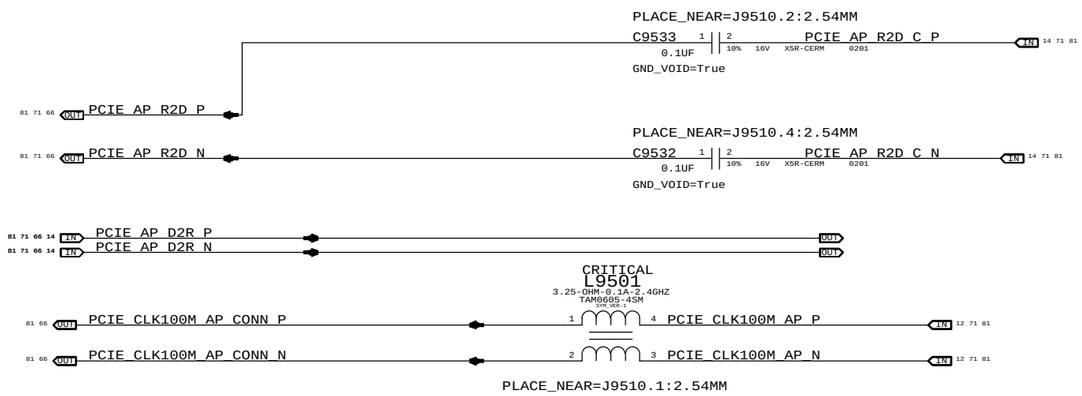
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0007	1	RES,MF,1/20W,10K OHM,5,0201,SMD	R8342	CRITICAL	PANEL:OLD
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	R8342	CRITICAL	PANEL:NEW

SYNC_MASTER=GKOO_J52 SYNC_DATE=05/04/2014

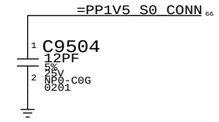
PAGE TITLE: eDP Display Connector

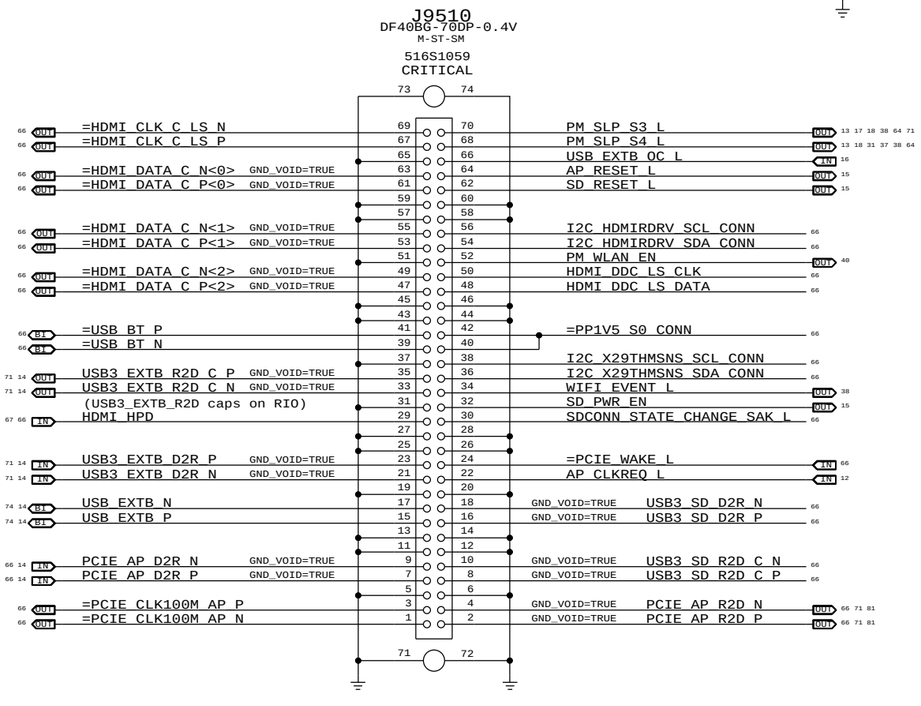
Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D
REVISION: 8.0.0
BRANCH: dvt1
PAGE: 83 OF 120
SHEET: 65 OF 82



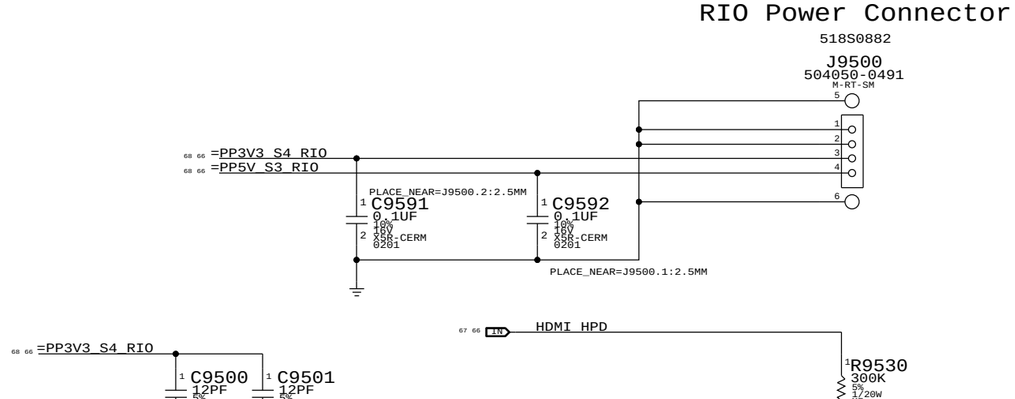
RIO FLEX CONNECTOR

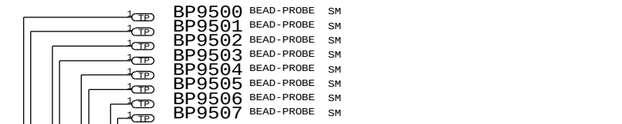




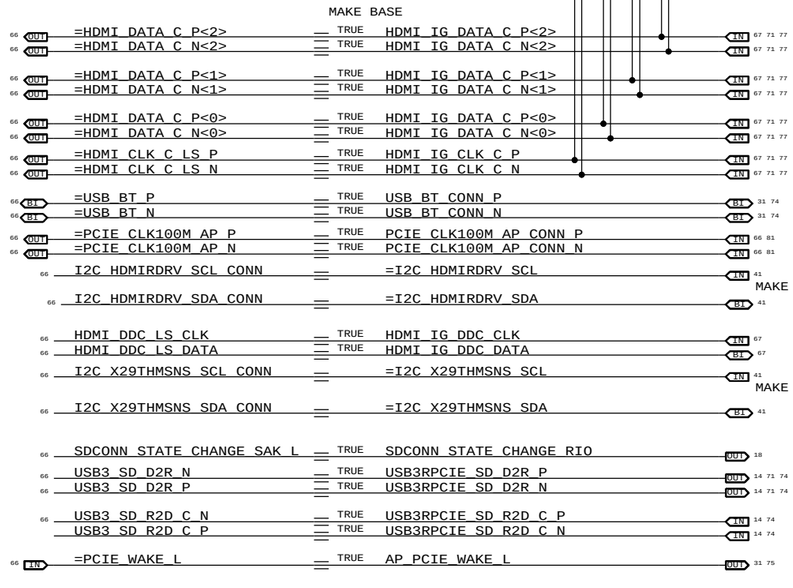
NOTE: This connector is shielded 70P Hirose Plug APN 516S1059, mates with APN 516S1058.

RIO Power Connector





MAKE BASE



BOM_COST_GROUP=IO PORTS

SYNC_MASTER=GKOO_J52 SYNC_DATE=05/01/2014

PAGE TITLE: RIO Connector

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 95 OF 120

SHEET: 66 OF 82

DISPLAY MUX: DP OR HDMI

=PP3V3_S0_DPMUX

DP 1:2 ANALOG DEMUX

C9750 0.1UF 20% 10V X7S-CERM 0402

C9751 0.1UF 20% 10V X7S-CERM 0402

U9750 HD3SS213ZQE BGA CRITICAL

DP_TBTSNK1_ML_C_P<0>	B4	DA0(P)	
DP_TBTSNK1_ML_C_N<0>	A4	DA0(N)	
DP_TBTSNK1_ML_C_P<1>	B5	DA1(P)	
DP_TBTSNK1_ML_C_N<1>	A5	DA1(N)	
DP_TBTSNK1_ML_C_P<2>	B6	DA2(P)	
DP_TBTSNK1_ML_C_N<2>	A6	DA2(N)	
DP_TBTSNK1_ML_C_P<3>	A8	DA3(P)	
DP_TBTSNK1_ML_C_N<3>	A9	DA3(N)	
DP_TBTSNK1_AUXCH_C_P	H9	AUXA(P)	
DP_TBTSNK1_AUXCH_C_N	J9	AUXA(N)	
DP_TBTSNK1_DDC_CLK	H8	DDCCLK_A	
DP_TBTSNK1_DDC_DATA	J8	DDCDAT_A	
DP_TBTSNK1_HPD	J2	HPDA	
HDMI_IG_DATA_C_P<2>	B8	DB0(P)	
HDMI_IG_DATA_C_N<2>	B9	DB0(N)	
HDMI_IG_DATA_C_P<1>	D8	DB1(P)	
HDMI_IG_DATA_C_N<1>	D9	DB1(N)	
HDMI_IG_DATA_C_P<0>	E8	DB2(P)	
HDMI_IG_DATA_C_N<0>	E9	DB2(N)	
HDMI_IG_CLK_C_P	F8	DB3(P)	
HDMI_IG_CLK_C_N	F9	DB3(N)	
NC	H6	AUXB(P)	
NC	J6	AUXB(N)	
HDMI_IG_DDC_CLK	H5	DDCCLK_B	
HDMI_IG_DDC_DATA	J5	DDCDAT_B	
HDMI_HPD	H3	HPDB	
DISP_MUX_SEL_L	A1	DX_SEL	
DISP_MUX_EN	B7	OE	
		GND	B3 C8 G8 H4 H7 G2
	B2	DC0(P)	DP_HDMI_TBT_ML_P<0>
	B1	DC0(N)	DP_HDMI_TBT_ML_N<0>
	D2	DC1(P)	DP_HDMI_TBT_ML_P<1>
	D1	DC1(N)	DP_HDMI_TBT_ML_N<1>
	E2	DC2(P)	DP_HDMI_TBT_ML_P<2>
	E1	DC2(N)	DP_HDMI_TBT_ML_N<2>
	F2	DC3(P)	DP_HDMI_TBT_ML_P<3>
	F1	DC3(N)	DP_HDMI_TBT_ML_N<3>
	H2	AUXC(P)	DP_HDMI_TBT_AUX_P
	H1	AUXC(N)	DP_HDMI_TBT_AUX_N
	J1	HPDC	DPMUX_HPD_OUT
	J3	DDCCLK_C	DP_HDMI_TBT_DDC_CLK
	J7	DDCDAT_C	DP_HDMI_TBT_DDC_DATA
	C2	AUX_SEL	DPMUX_AUX_DDC_SEL

TOWARDS PORTS

TOWARDS CPU

R9752 100K 5% 1/20W MF 201

R9753 100K 5% 1/20W MF 201

Q9700 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2

DISP_MUX_SEL

DISP MUX SEL_L
SEL_L 0 = DP
SEL_L 1 = HDMI

NOTE: HDMI ML SWIZZLED INTENTIONALLY AS PER TABLE 9-1 HASWELL-ULT PDG

=PP3V3_S0_DPMUX

C9725 0.1UF 20% 10V X6S-CERM 0201

NO STUFF R9725 10K 5% 1/20W MF 201

R9726 10K 5% 1/20W MF 201

R9727 10K 5% 1/20W MF 201

TOWARDS PORTS

NO STUFF R9755 100K 5% 1/20W MF 201

NO STUFF Q9701 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2

DISP_MUX_EN

U9725 PI3USB102ZLE TQFN CRITICAL

VCC, GND, SIGNAL_MODEL=MOJO_MUX

HDMI_IG_DDC_CLK	5	M+	
HDMI_IG_DDC_DATA	4	M-	
DP_TBTSNK1_DDC_CLK	7	D+	
DP_TBTSNK1_DDC_DATA	6	D-	
DISP_MUX_EN_L	8	OE*	
	1	Y+	DP_HDMI_TBT_DDC_CLK
	2	Y-	DP_HDMI_TBT_DDC_DATA
	10	SEL	DISP_MUX_SEL

TOWARDS CPU

DISP MUX SEL
SEL 0 = HDMI
SEL 1 = DP

=PP3V3_S0_DPMUX

C9700 0.1UF 10% 6.3V CERM-X5R 0201

OMIT_TABLE

U9700 SLG4APXXX TDFN

DP_TBTSNK1_HPD	2	IO_2	
HDMI_HPD	3	IO_3	
HDMITBTMUX_LATCH	4	IO_4	
	8	IO_8	DISP_MUX_EN
	7	IO_7	DISP_MUX_SEL
	6	IO_6	HDMITBTMUX_FLAG_L
	1	VDD	
	5	GND	
	9	THRM PAD	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0666	1	IC, SAK,AP4179,DP MUX CTRLR,TDFN-8	U9700	CRITICAL	

=PP3V3_S0_DPMUX

NOSTUFF R9701 100K 5% 1/20W MF 201

R9702 100K 5% 1/20W MF 201

DISP_MUX_PRIORITY

R9703 510K 5% 1/20W MF 201

R9704 510K 5% 1/20W MF 201

DPMUX_AUX_DDC_SEL

PRIORITY 0 = HDMI WINS OVER DP
PRIORITY 1 = DP WINS OVER HDMI

AUX_SEL 0 = AUX ONLY
AUX_SEL 1 = DDC ONLY
AUX_SEL Vdd/2 = AUX & DDC

=PP3V3_S4_DPMUX

C9775 0.1UF 10% 6.3V CERM-X5R 0201

=PP3V3_S0_DPMUX

R9754 100K 5% 1/20W MF 201

NOSTUFF CRITICAL U9775 SLG46400V TDFN

HDMI_HPD	2	GPI(2)	
DP_TBTSNK1_HPD	3	GPIO(3)	
	4	GPIO(4)	
NC	5	GPIO(5)	
DISP_MUX_PRIORITY	6	GPIO(6)	
HDMITBTMUX_LATCH	13	THRM_PAD	
	1	VDD	
	12	GPIO(12)	NC
	11	GPIO(11)	NC
	10	GPIO(10)	HDMITBTMUX_FLAG_L
	9	GPIO(9)	DISP_MUX_EN
	8	GPIO(8)	DISP_MUX_SEL
	7	GND	

DISP MUX SEL
SEL 0 = HDMI
SEL 1 = DP

BOM_COST_GROUP=TBT

SYNC_MASTER=SRAMAN_J44 SYNC_DATE=01/29/2013

PAGE TITLE: Display Mux: HDMI vs DP

Apple Inc.

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BRANCH dvt1

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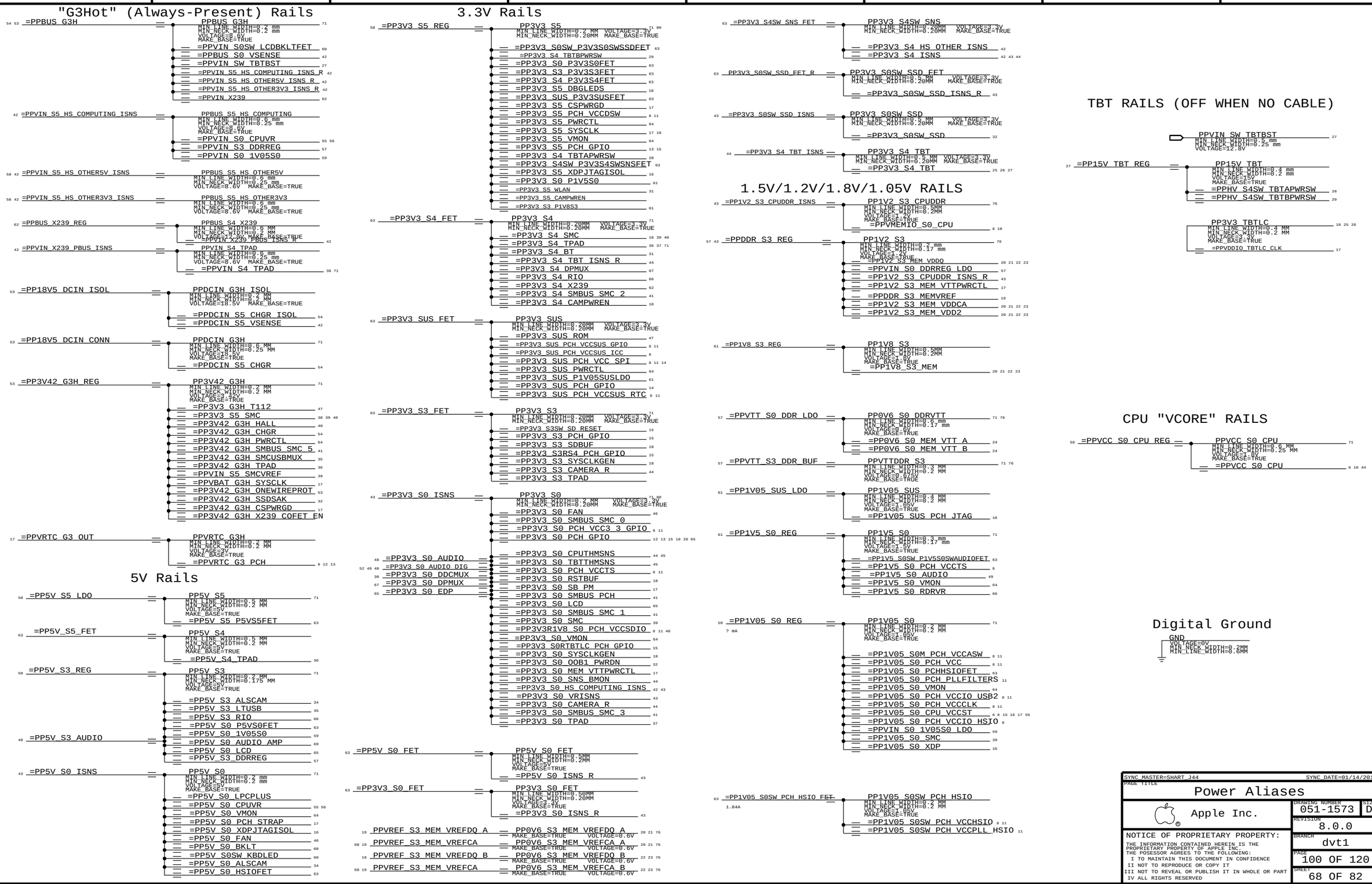

HDMI VS TBT

MAKE_BASE

5	=DP_TBTSNK1_ML_C_P<0>	TRUE	DP_HDMI_TBT_ML_P<0>	67	77
5	=DP_TBTSNK1_ML_C_N<0>	TRUE	DP_HDMI_TBT_ML_N<0>	67	77
5	=DP_TBTSNK1_ML_C_P<1>	TRUE	DP_HDMI_TBT_ML_P<1>	67	77
5	=DP_TBTSNK1_ML_C_N<1>	TRUE	DP_HDMI_TBT_ML_N<1>	67	77
5	=DP_TBTSNK1_ML_C_P<2>	TRUE	DP_HDMI_TBT_ML_P<2>	67	77
5	=DP_TBTSNK1_ML_C_N<2>	TRUE	DP_HDMI_TBT_ML_N<2>	67	77
5	=DP_TBTSNK1_ML_C_P<3>	TRUE	DP_HDMI_TBT_ML_P<3>	67	77
5	=DP_TBTSNK1_ML_C_N<3>	TRUE	DP_HDMI_TBT_ML_N<3>	67	77
13	=DP_TBTSNK1_AUXCH_C_P	TRUE	DP_HDMI_TBT_AUX_P	67	77
13	=DP_TBTSNK1_AUXCH_C_N	TRUE	DP_HDMI_TBT_AUX_N	67	77
13	=DP_TBTSNK1_DDC_CLK	TRUE	DP_HDMI_TBT_DDC_CLK	67	
13	=DP_TBTSNK1_DDC_DATA	TRUE	DP_HDMI_TBT_DDC_DATA	67	
13	=DP_TBTSNK1_HPD	TRUE	DPMUX_HPD_OUT	67	

25	HDMITBTMUX_SEL_TBT MAKE_BASE=TRUE	=TBT_GO2SX_BIDIR		15
		DISP_MUX_SEL		67
13	DP_AUXCH_ISOL_L	HDMITBTMUX_LATCH MAKE_BASE=TRUE		67

EPD PANEL

MAKE_BASE

60	=I2C_BKLT_SCL	TRUE	I2C_BKLT_SCL	65	71
60	=I2C_BKLT_SDA	TRUE	I2C_BKLT_SDA	65	71

UNUSED SIGNALS

MAKE_BASE

12	TP_PCIE_CLK100M_FWP	TRUE	NO_TEST=TRUE	NC_PCIE_CLK100M_FWP	
12	TP_PCIE_CLK100M_FWN	TRUE	NO_TEST=TRUE	NC_PCIE_CLK100M_FWN	
14	TP_PCIE_FW_D2RP	TRUE	NO_TEST=TRUE	NC_PCIE_FW_D2RP	
14	TP_PCIE_FW_D2RN	TRUE	NO_TEST=TRUE	NC_PCIE_FW_D2RN	
14	TP_PCIE_FW_R2D_CP	TRUE	NO_TEST=TRUE	NC_PCIE_FW_R2D_CP	
14	TP_PCIE_FW_R2D_CN	TRUE	NO_TEST=TRUE	NC_PCIE_FW_R2D_CN	
12	TP_PCIE_CLK100M_ENETSDP	TRUE	NO_TEST=TRUE	NC_PCIE_CLK100M_ENETSDP	
12	TP_PCIE_CLK100M_ENETSDN	TRUE	NO_TEST=TRUE	NC_PCIE_CLK100M_ENETSDN	
14	TP_USB_IR_P	TRUE	NO_TEST=TRUE	NC_USB_IRP	74
14	TP_USB_IR_N	TRUE	NO_TEST=TRUE	NC_USB_IRN	74
14	TP_USB_CAMERAP	TRUE	NO_TEST=TRUE	NC_USB_CAMERAP	74
14	TP_USB_CAMERAN	TRUE	NO_TEST=TRUE	NC_USB_CAMERAN	74
14	TP_USB_SDP	TRUE	NO_TEST=TRUE	NC_USB_SDP	74
14	TP_USB_SDN	TRUE	NO_TEST=TRUE	NC_USB_SDN	74
12	TP_HDA_SDIN1	TRUE	NO_TEST=TRUE	NC_HDA_SDIN1	
13	TP_PCI_PME_L	TRUE	NO_TEST=TRUE	NC_PCI_PME_L	
14	TP_CLINK_CLK	TRUE	NO_TEST=TRUE	NC_CLINK_CLK	
14	TP_CLINK_DATA	TRUE	NO_TEST=TRUE	NC_CLINK_DATA	
14	TP_CLINK_RESET_L	TRUE	NO_TEST=TRUE	NC_CLINK_RESET_L	
12	TP_ITPXDP_CLK100MN	TRUE	NO_TEST=TRUE	NC_ITPXDP_CLK100MN	
12	TP_ITPXDP_CLK100MP	TRUE	NO_TEST=TRUE	NC_ITPXDP_CLK100MP	
12	TP_PCH_I2S1_TXD	TRUE	NO_TEST=TRUE	NC_PCH_I2S1_TXD	
12	TP_PCH_I2S1_SFRM	TRUE	NO_TEST=TRUE	NC_PCH_I2S1_SFRM	
12	TP_PCH_I2S1_SCLK	TRUE	NO_TEST=TRUE	NC_PCH_I2S1_SCLK	
13	TP_PCH_SLP_WLAN_L	TRUE	NO_TEST=TRUE	NC_PCH_SLP_WLAN_L	
13	TP_PCH_SLP_LAN_L	TRUE	NO_TEST=TRUE	NC_PCH_SLP_LAN_L	
14	TP_SPI_CS1_L	TRUE	NO_TEST=TRUE	NC_SPI_CS1_L	
14	TP_SPI_CS2_L	TRUE	NO_TEST=TRUE	NC_SPI_CS2_L	
14	TP_USB_5N	TRUE	NO_TEST=TRUE	NC_USB_5N	74
14	TP_USB_5P	TRUE	NO_TEST=TRUE	NC_USB_5P	74
48	TP_AUD_CODEC_MICBIAS1_L	TRUE	NO_TEST=TRUE	NC_AUD_CODEC_MICBIAS1_L	
48	TP_AUD_CODEC_MICBIAS1_R	TRUE	NO_TEST=TRUE	NC_AUD_CODEC_MICBIAS1_R	
48	TP_AUD_CODEC_MICBIAS2_L	TRUE	NO_TEST=TRUE	NC_AUD_CODEC_MICBIAS2_L	
48	TP_AUD_CODEC_MICBIAS2_R	TRUE	NO_TEST=TRUE	NC_AUD_CODEC_MICBIAS2_R	
64	TP_SUS_PGOOD_MR_L	TRUE	NO_TEST=TRUE	NC_SUS_PGOOD_MR_L	
	TP_SMC_TRST_L	TRUE	NO_TEST=TRUE	NC_SMC_TRST_L	
	TP_SMC_MD1	TRUE	NO_TEST=TRUE	NC_SMC_MD1	
53	TP_TDM_ONEWIRE_MPM	TRUE	NO_TEST=TRUE	NC_TDM_ONEWIRE_MPM	

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

Digital Ground

68 =PP5V_S0_AUDIO_AMP

XWA202
SM
1 2
PP5V_S0_AUDIO_AMP_L 50
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

XWA203
SM
1 2
PP5V_S0_AUDIO_AMP_R 50
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

TBT UNUSED NETS

25	TP_TBT_MONDC0	TRUE MAKE_BASE=TRUE	NC_TBT_MONDC0	
25	TP_TBT_MONDC1	TRUE MAKE_BASE=TRUE	NC_TBT_MONDC1	
25	TP_TBT_PCIE_RESET0_L	TRUE MAKE_BASE=TRUE	NC_TBT_PCIE_RESET0_L	
25	TP_TBT_XTAL25OUT	TRUE MAKE_BASE=TRUE	NC_TBT_XTAL25OUT	
25	TP_DP_TBTSRC_ML_CP<3>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CP<3>	
25	TP_DP_TBTSRC_ML_CN<3>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CN<3>	
25	TP_DP_TBTSRC_ML_CP<2>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CP<2>	
25	TP_DP_TBTSRC_ML_CN<2>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CN<2>	
25	TP_DP_TBTSRC_ML_CP<1>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CP<1>	
25	TP_DP_TBTSRC_ML_CN<1>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CN<1>	
25	TP_DP_TBTSRC_ML_CP<0>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CP<0>	
25	TP_DP_TBTSRC_ML_CN<0>	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CN<0>	
25	TP_DP_TBTSRC_AUXCH_CP	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_AUXCH_CP	
25	TP_DP_TBTSRC_AUXCH_CN	TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_AUXCH_CN	

SYNC_MASTER=SHART_J44 SYNC_DATE=11/19/2012

PAGE TITLE
Signal Aliases

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LPDDR3 COMMAND/ADDRESS

		MAKE_BASE		
=MEM_A_A<5>	⟷	TRUE	MEM_A_CAA<0>	20 24 76
=MEM_A_A<9>	⟷	TRUE	MEM_A_CAA<1>	20 24 76
=MEM_A_A<6>	⟷	TRUE	MEM_A_CAA<2>	20 24 76
=MEM_A_A<8>	⟷	TRUE	MEM_A_CAA<3>	20 24 76
=MEM_A_A<7>	⟷	TRUE	MEM_A_CAA<4>	20 24 76
=MEM_A_BA<2>	⟷	TRUE	MEM_A_CAA<5>	20 24 76
=MEM_A_A<12>	⟷	TRUE	MEM_A_CAA<6>	20 24 76
=MEM_A_A<11>	⟷	TRUE	MEM_A_CAA<7>	20 24 76
=MEM_A_A<15>	⟷	TRUE	MEM_A_CAA<8>	20 24 76
=MEM_A_A<14>	⟷	TRUE	MEM_A_CAA<9>	20 24 76
=MEM_A_A<13>	⟷	TRUE	MEM_A_CAB<0>	21 24 76
=MEM_A_CAS_L	⟷	TRUE	MEM_A_CAB<1>	21 24 76
=MEM_A_WE_L	⟷	TRUE	MEM_A_CAB<2>	21 24 76
=MEM_A_RAS_L	⟷	TRUE	MEM_A_CAB<3>	21 24 76
=MEM_A_BA<0>	⟷	TRUE	MEM_A_CAB<4>	21 24 76
=MEM_A_A<2>	⟷	TRUE	MEM_A_CAB<5>	21 24 76
=MEM_A_BA<1>	⟷	TRUE	MEM_A_CAB<6>	21 24 76
=MEM_A_A<10>	⟷	TRUE	MEM_A_CAB<7>	21 24 76
=MEM_A_A<1>	⟷	TRUE	MEM_A_CAB<8>	21 24 76
=MEM_A_A<0>	⟷	TRUE	MEM_A_CAB<9>	21 24 76
=MEM_A_ODT<0>	⟷	TRUE	MEM_A_ODT<0>	20 21 24 76
=MEM_A_A<3>	⟷	TRUE	TP_LPDDR3_RSVD1	
=MEM_A_A<4>	⟷	TRUE	TP_LPDDR3_RSVD2	
=MEM_B_A<5>	⟷	TRUE	MEM_B_CAA<0>	22 24 76
=MEM_B_A<9>	⟷	TRUE	MEM_B_CAA<1>	22 24 76
=MEM_B_A<6>	⟷	TRUE	MEM_B_CAA<2>	22 24 76
=MEM_B_A<8>	⟷	TRUE	MEM_B_CAA<3>	22 24 76
=MEM_B_A<7>	⟷	TRUE	MEM_B_CAA<4>	22 24 76
=MEM_B_BA<2>	⟷	TRUE	MEM_B_CAA<5>	22 24 76
=MEM_B_A<12>	⟷	TRUE	MEM_B_CAA<6>	22 24 76
=MEM_B_A<11>	⟷	TRUE	MEM_B_CAA<7>	22 24 76
=MEM_B_A<15>	⟷	TRUE	MEM_B_CAA<8>	22 24 76
=MEM_B_A<14>	⟷	TRUE	MEM_B_CAA<9>	22 24 76
=MEM_B_A<13>	⟷	TRUE	MEM_B_CAB<0>	23 24 76
=MEM_B_CAS_L	⟷	TRUE	MEM_B_CAB<1>	23 24 76
=MEM_B_WE_L	⟷	TRUE	MEM_B_CAB<2>	23 24 76
=MEM_B_RAS_L	⟷	TRUE	MEM_B_CAB<3>	23 24 76
=MEM_B_BA<0>	⟷	TRUE	MEM_B_CAB<4>	23 24 76
=MEM_B_A<2>	⟷	TRUE	MEM_B_CAB<5>	23 24 76
=MEM_B_BA<1>	⟷	TRUE	MEM_B_CAB<6>	23 24 76
=MEM_B_A<10>	⟷	TRUE	MEM_B_CAB<7>	23 24 76
=MEM_B_A<1>	⟷	TRUE	MEM_B_CAB<8>	23 24 76
=MEM_B_A<0>	⟷	TRUE	MEM_B_CAB<9>	23 24 76
=MEM_B_ODT<0>	⟷	TRUE	MEM_B_ODT<0>	22 23 24 76
=MEM_B_A<3>	⟷	TRUE	TP_LPDDR3_RSVD3	
=MEM_B_A<4>	⟷	TRUE	TP_LPDDR3_RSVD4	

UNUSED MEMORY SIGNALS

		MAKE_BASE		
=MEM_RESET_L	⟷	TRUE	TP_CPU_MEM_RESET_L	

Memory Bit/Byte Swizzle

		TRUE		
MEM_A_DQ<0>	⟷		=MEM_A_DQ<7>	20
MEM_A_DQ<1>	⟷		=MEM_A_DQ<6>	20
MEM_A_DQ<2>	⟷		=MEM_A_DQ<5>	20
MEM_A_DQ<3>	⟷		=MEM_A_DQ<1>	20
MEM_A_DQ<4>	⟷		=MEM_A_DQ<3>	20
MEM_A_DQ<5>	⟷		=MEM_A_DQ<2>	20
MEM_A_DQ<6>	⟷		=MEM_A_DQ<0>	20
MEM_A_DQ<7>	⟷		=MEM_A_DQ<4>	20
MEM_A_DQ<8>	⟷		=MEM_A_DQ<10>	20
MEM_A_DQ<9>	⟷		=MEM_A_DQ<14>	20
MEM_A_DQ<10>	⟷		=MEM_A_DQ<8>	20
MEM_A_DQ<11>	⟷		=MEM_A_DQ<9>	20
MEM_A_DQ<12>	⟷		=MEM_A_DQ<15>	20
MEM_A_DQ<13>	⟷		=MEM_A_DQ<11>	20
MEM_A_DQ<14>	⟷		=MEM_A_DQ<12>	20
MEM_A_DQ<15>	⟷		=MEM_A_DQ<13>	20
MEM_A_DQ<16>	⟷		=MEM_A_DQ<21>	20
MEM_A_DQ<17>	⟷		=MEM_A_DQ<16>	20
MEM_A_DQ<18>	⟷		=MEM_A_DQ<23>	20
MEM_A_DQ<19>	⟷		=MEM_A_DQ<18>	20
MEM_A_DQ<20>	⟷		=MEM_A_DQ<19>	20
MEM_A_DQ<21>	⟷		=MEM_A_DQ<22>	20
MEM_A_DQ<22>	⟷		=MEM_A_DQ<17>	20
MEM_A_DQ<23>	⟷		=MEM_A_DQ<20>	20
MEM_A_DQ<24>	⟷		=MEM_A_DQ<27>	20
MEM_A_DQ<25>	⟷		=MEM_A_DQ<26>	20
MEM_A_DQ<26>	⟷		=MEM_A_DQ<25>	20
MEM_A_DQ<27>	⟷		=MEM_A_DQ<29>	20
MEM_A_DQ<28>	⟷		=MEM_A_DQ<30>	20
MEM_A_DQ<29>	⟷		=MEM_A_DQ<31>	20
MEM_A_DQ<30>	⟷		=MEM_A_DQ<24>	20
MEM_A_DQ<31>	⟷		=MEM_A_DQ<28>	20
MEM_A_DQ<32>	⟷		=MEM_A_DQ<38>	21
MEM_A_DQ<33>	⟷		=MEM_A_DQ<39>	21
MEM_A_DQ<34>	⟷		=MEM_A_DQ<37>	21
MEM_A_DQ<35>	⟷		=MEM_A_DQ<33>	21
MEM_A_DQ<36>	⟷		=MEM_A_DQ<35>	21
MEM_A_DQ<37>	⟷		=MEM_A_DQ<34>	21
MEM_A_DQ<38>	⟷		=MEM_A_DQ<32>	21
MEM_A_DQ<39>	⟷		=MEM_A_DQ<36>	21
MEM_A_DQ<40>	⟷		=MEM_A_DQ<42>	21
MEM_A_DQ<41>	⟷		=MEM_A_DQ<46>	21
MEM_A_DQ<42>	⟷		=MEM_A_DQ<40>	21
MEM_A_DQ<43>	⟷		=MEM_A_DQ<41>	21
MEM_A_DQ<44>	⟷		=MEM_A_DQ<47>	21
MEM_A_DQ<45>	⟷		=MEM_A_DQ<43>	21
MEM_A_DQ<46>	⟷		=MEM_A_DQ<44>	21
MEM_A_DQ<47>	⟷		=MEM_A_DQ<45>	21
MEM_A_DQ<48>	⟷		=MEM_A_DQ<61>	21
MEM_A_DQ<49>	⟷		=MEM_A_DQ<60>	21
MEM_A_DQ<50>	⟷		=MEM_A_DQ<58>	21
MEM_A_DQ<51>	⟷		=MEM_A_DQ<62>	21
MEM_A_DQ<52>	⟷		=MEM_A_DQ<63>	21
MEM_A_DQ<53>	⟷		=MEM_A_DQ<59>	21
MEM_A_DQ<54>	⟷		=MEM_A_DQ<57>	21
MEM_A_DQ<55>	⟷		=MEM_A_DQ<56>	21
MEM_A_DQ<56>	⟷		=MEM_A_DQ<48>	21
MEM_A_DQ<57>	⟷		=MEM_A_DQ<49>	21
MEM_A_DQ<58>	⟷		=MEM_A_DQ<55>	21
MEM_A_DQ<59>	⟷		=MEM_A_DQ<51>	21
MEM_A_DQ<60>	⟷		=MEM_A_DQ<53>	21
MEM_A_DQ<61>	⟷		=MEM_A_DQ<52>	21
MEM_A_DQ<62>	⟷		=MEM_A_DQ<54>	21
MEM_A_DQ<63>	⟷		=MEM_A_DQ<50>	21

		TRUE		
MEM_B_DQ<0>	⟷		=MEM_B_DQ<7>	22
MEM_B_DQ<1>	⟷		=MEM_B_DQ<6>	22
MEM_B_DQ<2>	⟷		=MEM_B_DQ<5>	22
MEM_B_DQ<3>	⟷		=MEM_B_DQ<1>	22
MEM_B_DQ<4>	⟷		=MEM_B_DQ<3>	22
MEM_B_DQ<5>	⟷		=MEM_B_DQ<2>	22
MEM_B_DQ<6>	⟷		=MEM_B_DQ<0>	22
MEM_B_DQ<7>	⟷		=MEM_B_DQ<4>	22
MEM_B_DQ<8>	⟷		=MEM_B_DQ<10>	22
MEM_B_DQ<9>	⟷		=MEM_B_DQ<14>	22
MEM_B_DQ<10>	⟷		=MEM_B_DQ<8>	22
MEM_B_DQ<11>	⟷		=MEM_B_DQ<9>	22
MEM_B_DQ<12>	⟷		=MEM_B_DQ<15>	22
MEM_B_DQ<13>	⟷		=MEM_B_DQ<11>	22
MEM_B_DQ<14>	⟷		=MEM_B_DQ<12>	22
MEM_B_DQ<15>	⟷		=MEM_B_DQ<13>	22
MEM_B_DQ<16>	⟷		=MEM_B_DQ<22>	22
MEM_B_DQ<17>	⟷		=MEM_B_DQ<18>	22
MEM_B_DQ<18>	⟷		=MEM_B_DQ<17>	22
MEM_B_DQ<19>	⟷		=MEM_B_DQ<16>	22
MEM_B_DQ<20>	⟷		=MEM_B_DQ<23>	22
MEM_B_DQ<21>	⟷		=MEM_B_DQ<19>	22
MEM_B_DQ<22>	⟷		=MEM_B_DQ<20>	22
MEM_B_DQ<23>	⟷		=MEM_B_DQ<21>	22
MEM_B_DQ<24>	⟷		=MEM_B_DQ<27>	22
MEM_B_DQ<25>	⟷		=MEM_B_DQ<26>	22
MEM_B_DQ<26>	⟷		=MEM_B_DQ<24>	22
MEM_B_DQ<27>	⟷		=MEM_B_DQ<28>	22
MEM_B_DQ<28>	⟷		=MEM_B_DQ<31>	22
MEM_B_DQ<29>	⟷		=MEM_B_DQ<30>	22
MEM_B_DQ<30>	⟷		=MEM_B_DQ<29>	22
MEM_B_DQ<31>	⟷		=MEM_B_DQ<25>	22
MEM_B_DQ<32>	⟷		=MEM_B_DQ<39>	23
MEM_B_DQ<33>	⟷		=MEM_B_DQ<38>	23
MEM_B_DQ<34>	⟷		=MEM_B_DQ<37>	23
MEM_B_DQ<35>	⟷		=MEM_B_DQ<33>	23
MEM_B_DQ<36>	⟷		=MEM_B_DQ<35>	23
MEM_B_DQ<37>	⟷		=MEM_B_DQ<34>	23
MEM_B_DQ<38>	⟷		=MEM_B_DQ<32>	23
MEM_B_DQ<39>	⟷		=MEM_B_DQ<36>	23
MEM_B_DQ<40>	⟷		=MEM_B_DQ<42>	23
MEM_B_DQ<41>	⟷		=MEM_B_DQ<46>	23
MEM_B_DQ<42>	⟷		=MEM_B_DQ<40>	23
MEM_B_DQ<43>	⟷		=MEM_B_DQ<41>	23
MEM_B_DQ<44>	⟷		=MEM_B_DQ<47>	23
MEM_B_DQ<45>	⟷		=MEM_B_DQ<43>	23
MEM_B_DQ<46>	⟷		=MEM_B_DQ<44>	23
MEM_B_DQ<47>	⟷		=MEM_B_DQ<45>	23
MEM_B_DQ<48>	⟷		=MEM_B_DQ<53>	23
MEM_B_DQ<49>	⟷		=MEM_B_DQ<55>	23
MEM_B_DQ<50>	⟷		=MEM_B_DQ<49>	23
MEM_B_DQ<51>	⟷		=MEM_B_DQ<54>	23
MEM_B_DQ<52>	⟷		=MEM_B_DQ<51>	23
MEM_B_DQ<53>	⟷		=MEM_B_DQ<52>	23
MEM_B_DQ<54>	⟷		=MEM_B_DQ<48>	23
MEM_B_DQ<55>	⟷		=MEM_B_DQ<50>	23
MEM_B_DQ<56>	⟷		=MEM_B_DQ<62>	23
MEM_B_DQ<57>	⟷		=MEM_B_DQ<63>	23
MEM_B_DQ<58>	⟷		=MEM_B_DQ<57>	23
MEM_B_DQ<59>	⟷		=MEM_B_DQ<60>	23
MEM_B_DQ<60>	⟷		=MEM_B_DQ<61>	23
MEM_B_DQ<61>	⟷		=MEM_B_DQ<56>	23
MEM_B_DQ<62>	⟷		=MEM_B_DQ<58>	23
MEM_B_DQ<63>	⟷		=MEM_B_DQ<59>	23

=MEM_A_DQS_P<0>	⟷	TRUE	MEM_A_DQS_P<0>	7 76
=MEM_A_DQS_N<0>	⟷	TRUE	MEM_A_DQS_N<0>	7 76
=MEM_A_DQS_P<1>	⟷	TRUE	MEM_A_DQS_P<1>	7 76
=MEM_A_DQS_N<1>	⟷	TRUE	MEM_A_DQS_N<1>	7 76
=MEM_A_DQS_P<2>	⟷	TRUE	MEM_A_DQS_P<2>	7 76
=MEM_A_DQS_N<2>	⟷	TRUE	MEM_A_DQS_N<2>	7 76
=MEM_A_DQS_P<3>	⟷	TRUE	MEM_A_DQS_P<3>	7 76
=MEM_A_DQS_N<3>	⟷	TRUE	MEM_A_DQS_N<3>	7 76
=MEM_A_DQS_P<4>	⟷	TRUE	MEM_A_DQS_P<4>	7 76
=MEM_A_DQS_N<4>	⟷	TRUE	MEM_A_DQS_N<4>	7 76
=MEM_A_DQS_P<5>	⟷	TRUE	MEM_A_DQS_P<5>	7 76
=MEM_A_DQS_N<5>	⟷	TRUE	MEM_A_DQS_N<5>	7 76
=MEM_A_DQS_P<6>	⟷	TRUE	MEM_A_DQS_P<7>	7 76
=MEM_A_DQS_N<6>	⟷	TRUE	MEM_A_DQS_N<7>	7 76
=MEM_A_DQS_P<7>	⟷	TRUE	MEM_A_DQS_P<6>	7 76
=MEM_A_DQS_N<7>	⟷	TRUE	MEM_A_DQS_N<6>	7 76

=MEM_B_DQS_P<0>	⟷	TRUE	MEM_B_DQS_P<0>	7 76
=MEM_B_DQS_N<0>	⟷	TRUE	MEM_B_DQS_N<0>	7 76
=MEM_B_DQS_P<1>	⟷	TRUE	MEM_B_DQS_P<1>	7 76
=MEM_B_DQS_N<1>	⟷	TRUE	MEM_B_DQS_N<1>	7 76
=MEM_B_DQS_P<2>	⟷	TRUE	MEM_B_DQS_P<2>	7 76
=MEM_B_DQS_N<2>	⟷	TRUE	MEM_B_DQS_N<2>	7 76
=MEM_B_DQS_P<3>	⟷	TRUE	MEM_B_DQS_P<3>	7 76
=MEM_B_DQS_N<3>	⟷	TRUE	MEM_B_DQS_N<3>	7 76
=MEM_B_DQS_P<4>	⟷	TRUE	MEM_B_DQS_P<4>	7 76
=MEM_B_DQS_N<4>	⟷	TRUE	MEM_B_DQS_N<4>	7 76
=MEM_B_DQS_P<5>	⟷	TRUE	MEM_B_DQS_P<5>	7 76
=MEM_B_DQS_N<5>	⟷	TRUE	MEM_B_DQS_N<5>	7 76
=MEM_B_DQS_P<6>	⟷	TRUE	MEM_B_DQS_P<6>	7 76
=MEM_B_DQS_N<6>	⟷	TRUE	MEM_B_DQS_N<6>	7 76
=MEM_B_DQS_P<7>	⟷	TRUE	MEM_B_DQS_P<7>	7 76
=MEM_B_DQS_N<7>	⟷	TRUE	MEM_B_DQS_N<7>	7 76

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Functional Test Points

J6050 (LEFT FAN CONN)

FUNC_TEST
- PP5V_S0 (68 71) — 3 TPs per Fan
- FAN_LT_PWM
- FAN_LT_TACH

J4002 (ALS/CAMERA CONN)
- SMBUS_SMC_1_S0_SCL (38 41 79)
- SMBUS_SMC_1_S0_SDA (38 41 79)
- PP5V_S3RS0_ALSCAM_F (34)
- MIPI_CLK_CONN_N (34 78)
- MIPI_CLK_CONN_P (34 78)
- CAM_SENSOR_WAKE_L_CONN (34)
- MIPI_DATA_CONN_N (34 78)
- MIPI_DATA_CONN_P (34 78)
- I2C_CAM_SCK (33 34)
- I2C_CAM_SDA (33 34)

J9500 (RIO POWER PINS)
- PP3V3_S4 (68 71)
- PP5V_S3 (68 71)
- PP1V5_S0 (68)
- GND

U0500 CHARZ TPS

P2MM
- PCIE_TBT_D2R_P<0> (81 25 14) — PP400
- PCIE_TBT_D2R_N<0> (81 25 14) — PP401
- PCIE_CLK100M_TBT_P (81 71 25 32) — PP423
- PCIE_CLK100M_TBT_N — PP424
- PCIE_CAMERA_D2R_P (81 34 14) — PP402
- PCIE_CAMERA_D2R_N (81 34 14) — PP403
- PCIE_SSD_D2R_P<0> (81 71 32 12) — PP404
- PCIE_SSD_D2R_N<0> (81 71 32 12) — PP405
- PCIE_AP_D2R_P (81 71 66 14) — PP410
- PCIE_AP_D2R_N (81 71 66 14) — PP411
- USB3RPCIE_SD_D2R_P (74 66 14) — PP420
- USB3RPCIE_SD_D2R_N (74 66 14) — PP421
- HDA_SDIN0 (75 49 12) — PP408 PLACE_NEAR=U0500.AY10:6MM
- MIPI_CLK_N (78 34 33) — PP441
- MIPI_CLK_P — PP442
- MIPI_DATA_N (78 34 33) — PP443
- MIPI_DATA_P — PP444

U5000 CHARZ TPS

P2MM
- LPC_CLK24M_SMC (79 37) — PP419

J6601 (AUDIO 2-MIKE CONN)
- DMIC_SDA3
- DMIC_SDA2
- DMIC_CLK3

J6602 (AUDIO LEFT SPEAKER CONN)
- SPKRCONN_L_OUT_P (50 52 80)
- SPKRCONN_L_OUT_N (50 52 80)
- SPKRCONN_L_ID (49 52)
- SPKRCONN_SL_OUT_P (50 52 80)
- SPKRCONN_SL_OUT_N (50 52 80)

J6603 (AUDIO RIGHT SPEAKER CONN)
- SPKRCONN_R_OUT_P (50 52 80)
- SPKRCONN_R_OUT_N (50 52 80)
- SPKRCONN_R_ID (49 52)
- SPKRCONN_SR_OUT_P (50 52 80)
- SPKRCONN_SR_OUT_N (50 52 80)
- GND

J8300 (EDP CONN)
- PP5VR3V3_SW_LCD (65)
- PPVOUT_S0_LCDBKLT (60 65) — 2 TP needed
- I2C_BKLT_SCL (65 69)
- I2C_BKLT_SDA (65 69)
- LCD_HPD_CONN (65)
- LCD_IRQ_L (15 65)
- EDP_BKLT_PWM (13 65)
- =I2C_TCON_SCL (41 65)
- =I2C_TCON_SDA (41 65)
- EDP_PANEL_PWR_OR_PSR_EN (65)
- DP_INT_AUX_P (65 77)
- DP_INT_AUX_N (65 77)
- DP_INT_ML_P<0> (65 77)
- DP_INT_ML_N<0> (65 77)
- DP_INT_ML_P<1> (65 77)
- DP_INT_ML_N<1> (65 77)
- DP_INT_ML_P<2> (65 77)
- DP_INT_ML_N<2> (65 77)
- DP_INT_ML_P<3> (65 77)
- DP_INT_ML_N<3> (65 77)

J4813 (KEY BOARD CONN)
- PP3V3_S4 (68 71)
- PP3V42_G3H (68 71)
- WS_KBD1 (36)
- WS_KBD2 (36)
- WS_KBD3 (36)
- WS_KBD4 (36)
- WS_KBD5 (36)
- WS_KBD6 (36)
- WS_KBD7 (36)
- WS_KBD8 (36)
- WS_KBD9 (36)
- WS_KBD10 (36)
- WS_KBD11 (36)
- WS_KBD12 (36)
- WS_KBD13 (36)
- WS_KBD14 (36)
- WS_KBD15_CAP (36)
- WS_KBD16_NUM (36)
- WS_KBD17 (36)
- WS_KBD18 (36)
- WS_KBD19 (36)
- WS_KBD20 (36)
- WS_KBD21 (36)
- WS_KBD22 (36)
- WS_KBD23 (36)
- WS_KBD_ONOFF_L (36)
- WS_LEFT_SHIFT_KBD (36)
- WS_LEFT_OPTION_KBD (36)
- WS_CONTROL_KBD (36)

J4802 (TPAD CONN)
- SMBUS_SMC_2_S3_SDA (38 41 79)
- SMBUS_SMC_2_S3_SCL (38 41 79)
- =PPVIN_S4_TPAD (36 68)
- TPAD_ACTUATOR_EN_L (36 40 42)
- TPAD_ACTUATOR_THRMTRIP_L (36 62)
- =TPAD_WAKE_L (36 40)
- SMC_LID (36 38 39 40)
- =PP3V3_S4_TPAD (36 37 68)
- I2C_IOXP_SDA (36)
- I2C_IOXP_SCL (36)
- TPAD_SPI_INT_L (15 36)
- =TPAD_SPI_SCLK (36 37)
- =TPAD_SPI_MISO (36 37)
- =TPAD_SPI_MOSI (36 37)
- TPAD_VBUS_EN (36 37)
- PP5V_S4_TPAD_F (36)
- IOXP2_INT_L (36)
- =TPAD_SPI_BUS_EN (36 37)
- =TPAD_SPI_CS_L (36 37)
- GND_ACTUATOR (36)
- USB_TPAD_P (14 36 74)
- USB_TPAD_N (14 36 74)
- =I2C_TPAD_SCL (36 41)
- =I2C_TPAD_SDA (36 41)

J7000 (DC POWER CONN)
- TDM_ONEWIRE_MPM
- ADAPTER_SENSE (53)
- PP18V5_DCIN_FUSE (53)
- GND
- PM_CLKRUN_L (13 38 71)
- PM_SYSRST_L (13 17 38 75)
- SMC_ONOFF_L (36 38 39)

J6100 (LPC + SPI CONN)
- PP3V42_G3H (68 71)
- PP5V_S0 (68 71)
- LPC_AD<0> (14 38 75)
- LPC_AD<2> (14 38 75)
- LPC_AD<1> (14 38 75)
- LPC_AD<3> (14 38 75)
- LPCPLUS_GPIO (16)
- LPCPLUS_RESET_L
- SMC_TDO (38 39)
- SMC_TX_L (38 39)
- LPC_FRAME_L (14 38 75)
- SPIROM_USE_MLB (15 47)
- PM_CLKRUN_L (13 38 71)
- LPC_SERIRQ (15 38)
- LPC_PWRDWN_L (13 38)
- SMC_TDI (38 39)
- SMC_TCK (38 39 47)
- SMC_RESET_L (38 39 40 47 54)
- SMC_ROMBOOT
- SMC_RX_L (38 39)
- SMC_TMS (38 39 47)

POWER RAILS

FUNC_TEST
- PM_SLP_S3_L (13 17 18 38 64 66)
- PP0V6_S0_DDRVTT (68 76)
- PP1V05_S0 (68)
- GND — 4 TPs
- PP3V3_S0 (68 80)
- PP3V3_S3 (68)
- PP3V3_S5 (68 80)
- PP3V3_S5_AVREF_SMC (38 39)
- PP3V42_G3H (68 71)
- PP5V_S0 (68 71)
- PP5V_S3 (68 71)
- PP5V_S5 (68)
- PPBUS_G3H (68)
- PPDCIN_G3H (68)
- PPVCC_S0_CPU (68)
- PPVTTDDR_S3 (68 71 76 13) — TP_PM_SLP_A_L — TRUE — MAKE_BASE=TRUE — NC_PM_SLP_A_L

NO_TESTs
- TBTBPWRSW_ISET_V3P3 (29)
- TBTBPWRSW_ISET_S0_R (29)
- TBTBPWRSW_ISET_S3 (29)
- TBTAPWRSW_ISET_V3P3 (28)
- TBTAPWRSW_ISET_S0 (28)
- TBTAPWRSW_ISET_S3 (28)
- TBTAPWRSW_ISET_S3_R (28)
- TBT_A_R2D_C_P<1..0> (25 28 77)
- TBT_A_R2D_C_N<1..0> (25 28 77)
- TBT_A_R2D_P<1..0> (28 77)
- TBT_A_R2D_N<1..0> (28 77)
- TBT_A_D2R_C_P<1> (28 77)
- TBT_A_D2R_C_N<1> (28 77)
- TBT_A_D2R_C_P<0> (28 77)
- TBT_A_D2R_C_N<0> (28 77)
- TBT_A_D2R_P<1> (25 28 77)
- TBT_A_D2R_N<1> (25 28 77)
- TBT_A_D2R_P<0> (25 28 77)
- TBT_A_D2R_N<0> (25 28 77)
- TBT_B_R2D_C_P<1..0> (25 29 77)
- TBT_B_R2D_C_N<1..0> (25 29 77)
- TBT_B_R2D_P<1..0> (29 77)
- TBT_B_R2D_N<1..0> (29 77)
- TBT_B_D2R_C_P<0> (29 77)
- TBT_B_D2R_C_N<0> (29 77)
- TBT_B_D2R_C_P<1> (29 77)
- TBT_B_D2R_C_N<1> (29 77)
- TBT_B_D2R_P<0> (25 29 77)
- TBT_B_D2R_N<0> (25 29 77)
- TBT_B_D2R_P<1> (25 29 77)
- TBT_B_D2R_N<1> (25 29 77)
- PCIE_AP_D2R_P (14 66 71 81)
- PCIE_AP_D2R_N (14 66 71 81)
- PCIE_AP_R2D_P (66 81)
- PCIE_AP_R2D_N (66 81)

MEM_A_DQ<63..0> (7 70 76)

PPVTTDDR_S3 (68 71 76)

MEM_B_DQ<63..0> (7 70 76)

HDMI_IG_CLK_C_P (66 67 77)
HDMI_IG_CLK_C_N (66 67 77)
HDMI_IG_DATA_C_P<2..0> (66 67 77)
HDMI_IG_DATA_C_N<2..0> (66 67 77)

TP_XDP_PCH_HOOK4 — NC_XDP_PCH_HOOK4
TP_XDP_PCH_HOOK5 — NC_XDP_PCH_HOOK5
TP_XDP_PCH_OBSFN_B<0> — NC_XDP_PCH_OBSFN_B<0>
TP_XDP_PCH_OBSFN_B<1> — NC_XDP_PCH_OBSFN_B<1>
TP_XDP_PCH_OBSFN_A<0> — NC_XDP_PCH_OBSFN_A<0>
TP_XDP_PCH_OBSFN_A<1> — NC_XDP_PCH_OBSFN_A<1>
TP_XDP_PCH_OBSFN_D<0> — NC_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_D<1> — NC_XDP_PCH_OBSFN_D<1>
TP_XDP_PCH_TRST_L — NC_XDP_PCH_TRST_L
TP_1V05_S0_PCH_VCCAPLLEXP — NC_1V05_S0_PCH_VCCAPLLEXP
TP_AUD_CODEC_MICBIAS — NC_AUD_CODEC_MICBIAS
TP_AUD_MIC_INRP — NC_AUD_MIC_INRP
TP_AUD_MIC_INRN — NC_AUD_MIC_INRN

(all: TRUE — MAKE_BASE=TRUE)

ICT Test Points

- NC_AUD_LO1_LN (48)
- NC_AUD_LO1_LP (48)
- NC_AUD_LO1_RN (48)
- NC_AUD_LO1_RP (48)
- NC_AUD_LO4_LN (48)
- NC_AUD_LO4_LP (48)
- NC_AUD_LO4_RN (48)
- NC_AUD_LO4_RP (48)
- NC_CS4208_GPO0 (49)
- NC_CS4208_GPO1 (49)
- NC_CS4208_LRCLKA (49)
- NC_CS4208_LRCLKB (49)
- NC_CS4208_MCLKA (49)
- NC_CS4208_MCLKB (49)
- NC_CS4208_SCLKA (49)
- NC_CS4208_SCLKB (49)
- NC_CS4208_SDOUTA (49)
- NC_CS4208_SDOUTB (49)
- NC_DMIC_CLK0 (49)
- NC_DMIC_CLK1 (49)
- NC_DMIC_CLK2 (49)

(all: TRUE)

- NC_SMC_HIB_L (38)
- NC_SMC_XOSC1 (38)

(all: TRUE)

NC NO_TEST

High Speed NO_TEST
- PCIE_AP_R2D_C_P (14 66 81)
- PCIE_AP_R2D_C_N (14 66 81)
- PCIE_AP_D2R_P (14 66 71 81)
- PCIE_AP_D2R_N (14 66 71 81)
- PCIE_SSD_R2D_C_P<3..0> (12 32 81)
- PCIE_SSD_R2D_C_N<3..0> (12 32 81)
- PCIE_SSD_R2D_P<3..0> (32 81)
- PCIE_SSD_R2D_N<3..0> (32 81)
- PCIE_SSD_D2R_P<3..0> (12 32 71 81)
- PCIE_SSD_D2R_N<3..0> (12 32 71 81)
- PCIE_TBT_R2D_C_P<3..0> (14 25 81)
- PCIE_TBT_R2D_C_N<3..0> (14 25 81)
- PCIE_TBT_R2D_P<3..0> (25 81)
- PCIE_TBT_R2D_N<3..0> (25 81)
- PCIE_TBT_D2R_P<3..1> (14 25 81)
- PCIE_TBT_D2R_N<3..1> (14 25 81)
- PCIE_TBT_D2R_C_P<3..1> (25 81)
- PCIE_TBT_D2R_C_N<3..1> (25 81)
- USB3_EXTA_D2R_P (14 35 74)
- USB3_EXTA_D2R_N (14 35 74)
- USB3_EXTA_R2D_C_P (14 35 74)
- USB3_EXTA_R2D_C_N (14 35 74)
- USB3_EXTA_R2D_N (35 71 74)
- USB3_EXTA_R2D_N (35 71 74)
- USB3_EXTB_D2R_P (14 66 74)
- USB3_EXTB_D2R_N (14 66 74)
- USB3_EXTB_R2D_C_P (14 66 74)
- USB3_EXTB_R2D_C_N (14 66 74)
- PCIE_CLK100M_SSD_P (12 32 81)
- PCIE_CLK100M_SSD_N (12 32 81)
- PCIE_CLK100M_TBT_P (12 25 71 81)
- PCIE_CLK100M_TBT_N (12 25 71 81)
- PCIE_CLK100M_AP_P (12 66 81)
- PCIE_CLK100M_AP_N (12 66 81)
- PCIE_CLK100M_CAMERA_P (12 34 81)
- PCIE_CLK100M_CAMERA_N (12 34 81)

(all: TRUE)

Unused nets with offpage

(Nets with offpages not used on this project)
- HDD_PWR_EN (15)
- WOL_EN (14)
- BT_PWRRST_L (15)
- ENET_MEDIA_SENSE (15)
- ODD_PWR_EN_L (13)
- ENET_LOW_PWR (13)
- AUD_IP_PERIPHERAL_DET (13)
- AUD_IPHS_SWITCH_EN (13)
- ENETSD_CLKREQ_L (12)

J7715 (KBD BACKLIGHT CONN)
- PPVOUT_S0_KBDBKLT (37 60)
- KBDLED_CATHODE1 (37 60)
- KBDLED_CATHODE2 (37 60)

J7050 (MAIN BATT CONN)
- PPVBAT_G3H_CONN (53 54)
- SMBUS_SMC_5_G3_SCL (38 41 79)
- SMBUS_SMC_5_G3_SDA (38 41 79)
- SYS_DETECT_L (53)

J6601 (2 MIC CONN)
- CON_DMIC_PWR
- CON_DMIC_SDA1
- CON_DMIC_CLK

J4600 (LEFT USB CONN)
- PP5V_S3_LTUSB_A_F (35)
- USB_LT1_N (74)
- USB_LT1_P (74)

FUNC_TEST
- GND
- GND
- GND — 6 TPs

SMBUS_PCH_CLK (14 41 75)
SMBUS_PCH_DATA (14 41 75)

PCH_VSS_NCTF<19> (71)
PCH_VSS_NCTF<19> (71)

(all: TRUE)

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X304 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA,BGA_MEM	MM	16.5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.120 MM	0.120 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.120 MM	0.120 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.155 MM	0.155 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
73_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.110 MM	0.110 MM		0.120 MM	0.120 MM
73_OHM_DIFF	ISL2,ISL11	Y	0.110 MM	0.110 MM		0.120 MM	0.120 MM
73_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.141 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	.	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_08MIL	*	0.203 MM	?
CPU_12MIL	*	0.305 MM	?
CPU_18MIL	*	0.457 MM	?
CPU_25MIL	*	0.635 MM	?

CPU Signal Properties

ELECTRICAL CONST SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
XDP_TCK0	CPU_45S	CPU_18MIL	XDP_CPU_TCK	6 16
XDP_TCK0	CPU_45S	CPU_18MIL	PCH_JTAGX	12 16
XDP_TCK1	CPU_45S	CPU_18MIL	XDP_PCH_TCK	12 16
XDP_TDO	CPU_45S		XDP_CPU_TDO	6 16
XDP_TDO	CPU_45S		XDP_PCH_TDO	12 16
XDP_TDI	CPU_45S		XDP_CPU_TDI	6 16
XDP_TDI	CPU_45S		XDP_PCH_TDI	12 16
XDP_TMS	CPU_45S		XDP_CPU_TMS	6 16
XDP_TMS	CPU_45S		XDP_PCH_TMS	12 16
XDP_TRST_L	CPU_45S		XDP_TRST_L	16
XDP_TRST_L	CPU_45S		XDP_CPUPCH_TRST_L	16
XDP_PRDY_L	CPU_45S		XDP_CPU_PRDY_L	6 16
XDP_PREQ_L	CPU_45S		XDP_CPU_PREQ_L	6 16
CPU_VCCST_PWRGD	CPU_45S	CPU_08MIL	CPU_VCCST_PWRGD	8 16 17
CPU_VCCST_PWRGD	CPU_45S	CPU_08MIL	XDP_CPU_VCCST_PWRGD	16
CPU_BPM	CPU_45S	CPU_08MIL	XDP_BPM_L<1..0>	6 16
CPU_BPM_TP	CPU_45S		XDP_BPM_L<7..2>	6 16
CPU_RCOMP_SM	CPU_27P4S	CPU_25MIL	CPU_SM_RCOMP<2..0>	6
CPU_RCOMP_EDP	CPU_27P4S	CPU_25MIL	MCP_EDP_RCOMP	5
CPU_RCOMP_OPI	CPU_27P4S	CPU_12MIL	CPU_OPI_RCOMP	6
CPU_PROCHOT	CPU_45S	CPU_08MIL	CPU_PROCHOT_L	6 38 39 55
CPU_PROCHOT	CPU_45S	CPU_08MIL	CPU_PROCHOT_R_L	6
CPU_CATERR	CPU_45S	CPU_08MIL	CPU_CATERR_L	6 38
CPU_VIDALERT	CPU_45S	CPU_18MIL	CPU_VIDALERT_L	8 55
CPU_VIDALERT	CPU_45S	CPU_18MIL	CPU_VIDALERT_R_L	8
CPU_VIDSCLK	CPU_45S	CPU_18MIL	CPU_VIDSCLK	8 55
CPU_VIDSCLK	CPU_45S	CPU_18MIL	CPU_VIDSCLK_R	8
CPU_VIDSOUT	CPU_45S	CPU_18MIL	CPU_VIDSOUT	8 55
CPU_VIDSOUT	CPU_45S	CPU_18MIL	CPU_VIDSOUT_R	8
CPU_PECI	CPU_45S	CPU_18MIL	CPU_PECI	6 39
CPU_PECI	CPU_45S	CPU_18MIL	CPU_PECI_R	38 39
CPU_PECI	CPU_45S	CPU_18MIL	SMC_PECI_L	38 39
CPU_PECI	CPU_45S	CPU_18MIL	SMC_PECI_L_R	39
CPU_CFG	CPU_45S		CPU_CFG<19..11>	6 16
CPU_CFG_PD	CPU_45S		CPU_CFG<10..8>	6 16
CPU_CFG	CPU_45S		CPU_CFG<7..5>	6 16
CPU_CFG_PD	CPU_45S		CPU_CFG<4>	6 16
CPU_CFG_3	CPU_45S		CPU_CFG<3>	6 16
CPU_CFG	CPU_45S		CPU_CFG<2>	6 16
CPU_CFG_PD	CPU_45S		CPU_CFG<1..0>	6 16
CPU_MEM_RESET	CPU_45S	CPU_08MIL	MEM_RESET_L	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 55
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 55

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USB 2 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?

USB 3 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	*	*	USB3_2OTHER
USB3_*	=SAME	*	USB3_2SAME
USB3_TX	*_RX	*	USB3_TXRX
USB3_RX	*_TX	*	USB3_TXRX

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5x_DIELECTRIC	?

SATA Interface Constraints (Not Used)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	*	*	SATA_2OTHER
SATA_*	=SAME	*	SATA_2SAME
SATA_TX	*_RX	*	SATA_TXRX
SATA_RX	*_TX	*	SATA_TXRX

USB Constraints

ELECTRICAL CONST SET	NET TYPE: PHYSICAL	NET TYPE: SPACING	
USB_BT	USB_85D	USB	USB_BT_P 14 31
USB_BT	USB_85D	USB	USB_BT_N 14 31
USB_BT	USB_85D	USB	USB_BT_CONN_P 31 66
USB_BT	USB_85D	USB	USB_BT_CONN_N 31 66
USB_EXTA	USB_85D	USB	USB_EXTA_P 14 35
USB_EXTA	USB_85D	USB	USB_EXTA_N 14 35
	DEFAULT	DEFAULT	SMC_DEBUGPRT_RX_L 35 38 39
	DEFAULT	DEFAULT	SMC_DEBUGPRT_TX_L 35 38 39
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_P 35
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_N 35
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_F_P 35
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_F_N 35
USB_EXTA	USB_85D	USB	USB_LT1_P 71
USB_EXTA	USB_85D	USB	USB_LT1_N 71
USB_EXTB	USB_85D	USB	USB_EXTB_P 14 66
USB_EXTB	USB_85D	USB	USB_EXTB_N 14 66
USB_TPAD	USB_85D	USB	USB_TPAD_P 14 36 71
USB_TPAD	USB_85D	USB	USB_TPAD_N 14 36 71
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3_EXTA_D2R_P 14 35 71
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3_EXTA_D2R_N 14 35 71
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_P 35
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_N 35 71
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_C_P 14 35 71
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_C_N 14 35 71
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3_EXTB_D2R_P 14 66 71
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3_EXTB_D2R_N 14 66 71
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3_EXTB_R2D_C_P 14 66 71
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3_EXTB_R2D_C_N 14 66 71
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_P 14 66 71
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_N 14 66 71
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_P 14 66
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_N 14 66
USB_NC	USB_85D	USB	NC_USB_IRP 69
USB_NC	USB_85D	USB	NC_USB_IRN 69
USB_NC	USB_85D	USB	NC_USB_5P 69
USB_NC	USB_85D	USB	NC_USB_5N 69
USB_NC	USB_85D	USB	NC_USB_SDP 69
USB_NC	USB_85D	USB	NC_USB_SDN 69
USB_NC	USB_85D	USB	NC_USB_CAMERAP 69
USB_NC	USB_85D	USB	NC_USB_CAMERAN 69
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS 14
	SATA_85D	SATA_RX	DUMMY_SATA_D2R_P
	SATA_85D	SATA_RX	DUMMY_SATA_D2R_N
	SATA_85D	SATA_TX	DUMMY_SATA_R2D_P
	SATA_85D	SATA_TX	DUMMY_SATA_R2D_N
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1 17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2 17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R 17
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA 17 34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP 33 34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R 34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP 34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN 34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN 33 34
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT 17 25
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R 25

Notes:
This is here to keep the SATA rules.

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
PCH_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_12MIL	*	0.305 MM	?
PCH_15MIL	*	0.381 MM	?
PCH_18MIL	*	0.457 MM	?
PCH_20MIL	*	0.508 MM	?

PCH Net Properties

ELECTRICAL CONST SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 38 71
LPC_AD	LPC_45S	LPC	LPC_FRAME_L	14 38 71
LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 71
SMBUS_PCH	SMB_45S	SMB	SMBUS_PCH_CLK	14 41 71
SMBUS_PCH	SMB_45S	SMB	SMBUS_PCH_DATA	14 41 71
SML_PCH_0	SMB_45S	SMB	SML_PCH_0_CLK	14 41
SML_PCH_0	SMB_45S	SMB	SML_PCH_0_DATA	14 41
	SMB_45S	SMB	SML_PCH_1_CLK	14 41
	SMB_45S	SMB	SML_PCH_1_DATA	14 41
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 49
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 49
HDA_SYNC	HDA_45S	HDA	HDA_SYNC_R	12
HDA_RST	HDA_45S	HDA	HDA_RST_R_L	12
HDA_RST	HDA_45S	HDA	HDA_RST_L	12 49
HDA_SDIN	HDA_45S	HDA	HDA_SDIN0	12 49 71
HDA_SDIN	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	49
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 49
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT_R	12 17
SPI_MLB	SPI_45S	SPI	SPI_ALT_CLK	47
SPI_MLB	SPI_45S	SPI	SPI_CLK	47
SPI_MLB	SPI_45S	SPI	SPI_CLK_R	14 47
SPI_MLB	SPI_45S	SPI	SPI_MLB_CLK	47
SPI_MLB	SPI_45S	SPI	SPI_SMC_CLK	38 47
SPI_MLB	SPI_45S	SPI	SPI_ALT_CS_L	47
SPI_MLB	SPI_45S	SPI	SPI_CS0_L	47
SPI_MLB	SPI_45S	SPI	SPI_CS0_R_L	14 47
SPI_MLB	SPI_45S	SPI	SPI_MLB_CS_L	47
SPI_MLB	SPI_45S	SPI	SPI_SMC_CS_L	38 47
SPI_MLB	SPI_45S	SPI	SPI_ALT_IO1_MISO	47
SPI_MLB	SPI_45S	SPI	SPI_MISO	14 47
SPI_MLB	SPI_45S	SPI	SPI_MISO_R	47
SPI_MLB	SPI_45S	SPI	SPI_MLB_IO1_MISO	47
SPI_MLB	SPI_45S	SPI	SPI_SMC_MISO	38 47
SPI_MLB	SPI_45S	SPI	SPI_ALT_IO0_MOSI	47
SPI_MLB	SPI_45S	SPI	SPI_MOSI	47
SPI_MLB	SPI_45S	SPI	SPI_MOSI_R	14 47
SPI_MLB	SPI_45S	SPI	SPI_MLB_IO0_MOSI	47
SPI_MLB	SPI_45S	SPI	SPI_SMC_MOSI	38 47
SPI_MLB_IO2	SPI_45S	SPI	SPI_IO<2>	14 47
SPI_MLB_IO2	SPI_45S	SPI	SPI_IO2_R	47
SPI_MLB_IO2	SPI_45S	SPI	SPI_MLB_IO2_WP_L	47
SPI_MLB_IO2	SPI_45S	SPI	SPI_ALT_IO2_WP_L	47
SPI_MLB_IO3	SPI_45S	SPI	SPI_IO<3>	14 47
SPI_MLB_IO3	SPI_45S	SPI	SPI_IO3_R	47
SPI_MLB_IO3	SPI_45S	SPI	SPI_MLB_IO3_HOLD_L	47
SPI_MLB_IO3	SPI_45S	SPI	SPI_ALT_IO3_HOLD_L	47
SPI_TPAD	SPI_45S	SPI	TPAD_SPI_CLK	15 37
SPI_TPAD_CS	SPI_45S	SPI	TPAD_SPI_CS_L	15 37
SPI_TPAD	SPI_45S	SPI	TPAD_SPI_MISO	15 37
SPI_TPAD	SPI_45S	SPI	TPAD_SPI_MOSI	15 37
PCH_RTCX	PCH_45S	PCH_15MIL	PCH_CLK32K_RTCX1	12 17
PCH_SRTCRST	PCH_45S	PCH_15MIL	PCH_SRTCRST_L	12
PCH_RTCRST	PCH_45S	PCH_15MIL	RTC_RESET_L	12
PCH_THRMTRIP	PCH_45S	PCH_18MIL	PM_THRMTRIP_L	15 39
PCH_THRMTRIP	PCH_45S	PCH_18MIL	PM_THRMTRIP_R_L	39
	PCH_45S	PCH_15MIL	PCH_INTRUDER_L	12
	PCH_45S	PCH_15MIL	PCH_INTVRMEN	12
	PCH_45S	PCH_15MIL	PCH_DSWVRMEN	13
	PCH_45S	PCH_15MIL	PM_RSMRST_L	13 64
	PCH_45S	PCH_15MIL	PM_SYSRST_L	13 17 38 71
	PCH_45S	PCH_15MIL	XDP_DBRESET_L	16 17
	PCH_45S	PCH_15MIL	PM_PCH_SYS_PWROK	13 16 17 38
	PCH_45S	PCH_15MIL	XDP_SYS_PWROK	16
	PCH_45S	PCH_15MIL	SYS_PWROK_R	17
	PCH_45S	PCH_15MIL	PM_PCH_PWROK	13 17
	PCH_45S	PCH_15MIL	PM_S0_PGOOD	17
	PCH_45S	PCH_15MIL	SMC_DELAYED_PWRGD	17 26 27 38 39
	PCH_45S	PCH_15MIL	PM_DSW_PWRGD	13 38
	PCH_45S	PCH_15MIL	PM_PWRBTN_L	13 16 38
	PCH_45S	PCH_15MIL	XDP_CPU_PWRBTN_L	16
	PCH_45S	PCH_15MIL	PCIE_WAKE_L	13 31 33
	PCH_45S	PCH_15MIL	AP_PCIE_WAKE_L	31 66
	PCH_45S	PCH_15MIL	CAM_PCIE_WAKE_L	33
	PCH_45S	PCH_15MIL	TBT_CIO_PLUG_EVENT_L	18 25
PCH_CLK24M_XTAL	PCH_45S	PCH_20MIL	PCH_CLK24M_XTALIN	12 17
PCH_CLK24M_XTAL	PCH_45S	PCH_20MIL	PCH_CLK24M_XTALOUT	12 17
PCH_CLK24M_XTAL	PCH_45S	PCH_20MIL	PCH_CLK24M_XTALOUT_R	17
PCH_RCOMP_PCIE	PCH_27P4S	PCH_12MIL	PCH_PCIE_RCOMP	14
PCH_RCOMP_OPI	PCH_27P4S	PCH_12MIL	PCH_OPI_COMP	15
PCH_RCOMP_SATA	PCH_27P4S	PCH_12MIL	PCH_SATA_RCOMP	12

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PAGE TITLE: PCH Constraints

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	0.066 MM	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTL	*	=3x_DIELECTRIC	?
MEM_CTL2CTL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?
MEM_CMD2CMD_BM	*	=3x_DIELECTRIC	?
MEM_CMD2CTL_BM	*	=3x_DIELECTRIC	?
MEM_CTL2CTL_BM	*	=3x_DIELECTRIC	?
MEM_12MIL	*	0.305 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTL2CTL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_CMD2CMD_BM	TOP,BOTTOM	=3x_DIELECTRIC	?
MEM_CMD2CTL_BM	TOP,BOTTOM	=3x_DIELECTRIC	?
MEM_CTL2CTL_BM	TOP,BOTTOM	=3x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTL	*	MEM_CMD2CTL
MEM_CTL	MEM_CTL	*	MEM_CTL2CTL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_CMD	MEM_CMD	BGA_MEM	MEM_CMD2CMD_BM
MEM_CMD	MEM_CTL	BGA_MEM	MEM_CMD2CTL_BM
MEM_CTL	MEM_CTL	BGA_MEM	MEM_CTL2CTL_BM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DQBYTE_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DQBYTE_7	*	MEM_DQS2OWNDATA

Broadwell ULT Memory Down LPDDR3 1x4 Length Matching

LPDDR3 Signal Group	Unit	Min Length	Max Length
CTL/CKEmax - CTL/CKEmin	mils	0	50
CTL/CKE to CLK	mils	CLK - 100	0
(CMDmax - CMDmin)	mils	0	50
CMD to CLK	mils	CLK - 250	CLK + 250
DQmax - DQmin per byte	mils	0	125
DQmax to DQs per byte	mils	DQS - 200	DQS + 50
DQS to DQS#	mils	-2.5	2.5
DQS to CLK (Rule 1)	mils	CLK - 750	CLK + 1250
CLK to CLK#	mils	-2.5	2.5

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	BGA_MEM	MEM_73D
MEM_40S	BGA_MEM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL CONST SET	NET TYPE: PHYSICAL	NET TYPE: SPACING	
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0> 7 20 24
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0> 7 20 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1> 7 21 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1> 7 21 24
MEM_A_CTL	MEM_40S	MEM_CTL	MEM_A_CS_L<1..0> 7 20 21 24
MEM_A_CTL	MEM_40S	MEM_CTL	MEM_A_ODT<0> 20 21 24 70
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0> 7 20 24
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2> 7 21 24
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0> 20 24 70
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0> 21 24 70
MEM_A_DQBYTE0	MEM_40S	MEM_A_DQBYTE_0	MEM_A_DQ<7..0> 7 70 71
MEM_A_DQBYTE1	MEM_40S	MEM_A_DQBYTE_1	MEM_A_DQ<15..8> 7 70 71
MEM_A_DQBYTE2	MEM_40S	MEM_A_DQBYTE_2	MEM_A_DQ<23..16> 7 70 71
MEM_A_DQBYTE3	MEM_40S	MEM_A_DQBYTE_3	MEM_A_DQ<31..24> 7 70 71
MEM_A_DQBYTE4	MEM_40S	MEM_A_DQBYTE_4	MEM_A_DQ<39..32> 7 70 71
MEM_A_DQBYTE5	MEM_40S	MEM_A_DQBYTE_5	MEM_A_DQ<47..40> 7 70 71
MEM_A_DQBYTE6	MEM_40S	MEM_A_DQBYTE_6	MEM_A_DQ<55..48> 7 70 71
MEM_A_DQBYTE7	MEM_40S	MEM_A_DQBYTE_7	MEM_A_DQ<63..56> 7 70 71
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0> 7 70
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0> 7 70
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1> 7 70
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1> 7 70
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2> 7 70
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2> 7 70
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3> 7 70
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3> 7 70
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4> 7 70
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4> 7 70
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5> 7 70
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5> 7 70
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6> 7 70
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6> 7 70
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7> 7 70
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7> 7 70
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0> 7 22 24
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0> 7 22 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1> 7 23 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1> 7 23 24
MEM_B_CTL	MEM_40S	MEM_CTL	MEM_B_CS_L<1..0> 7 22 23 24
MEM_B_CTL	MEM_40S	MEM_CTL	MEM_B_ODT<0> 22 23 24 70
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0> 7 22 24
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2> 7 23 24
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0> 22 24 70
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0> 23 24 70
MEM_B_DQBYTE0	MEM_40S	MEM_B_DQBYTE_0	MEM_B_DQ<7..0> 7 70 71
MEM_B_DQBYTE1	MEM_40S	MEM_B_DQBYTE_1	MEM_B_DQ<15..8> 7 70 71
MEM_B_DQBYTE2	MEM_40S	MEM_B_DQBYTE_2	MEM_B_DQ<23..16> 7 70 71
MEM_B_DQBYTE3	MEM_40S	MEM_B_DQBYTE_3	MEM_B_DQ<31..24> 7 70 71
MEM_B_DQBYTE4	MEM_40S	MEM_B_DQBYTE_4	MEM_B_DQ<39..32> 7 70 71
MEM_B_DQBYTE5	MEM_40S	MEM_B_DQBYTE_5	MEM_B_DQ<47..40> 7 70 71
MEM_B_DQBYTE6	MEM_40S	MEM_B_DQBYTE_6	MEM_B_DQ<55..48> 7 70 71
MEM_B_DQBYTE7	MEM_40S	MEM_B_DQBYTE_7	MEM_B_DQ<63..56> 7 70 71
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0> 7 70
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0> 7 70
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1> 7 70
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1> 7 70
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2> 7 70
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2> 7 70
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3> 7 70
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3> 7 70
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4> 7 70
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4> 7 70
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5> 7 70
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5> 7 70
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6> 7 70
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6> 7 70
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7> 7 70
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_N<7> 7 70
		MEM_PWR	PP1V2_S3 68
		MEM_PWR	PP1V2_S3_CPUDDR 68
		MEM_PWR	PP0V6_S0_DDRVTT 68 71
		MEM_PWR	PPVTTDDR_S3 68 71
		MEM_12MIL	CPU_DIMMA_VREFDQ 7 19
		MEM_12MIL	CPU_DIMMB_VREFDQ 7 19
		MEM_12MIL	CPU_DIMM_VREFCA 7 19
		MEM_12MIL	PP0V6_S3_MEM_VREFDQ_A 20 21 68
		MEM_12MIL	PP0V6_S3_MEM_VREFDQ_B 22 23 68
		MEM_12MIL	PP0V6_S3_MEM_VREFCA_A 20 21 68
		MEM_12MIL	PP0V6_S3_MEM_VREFCA_B 22 23 68

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Thunderbolt, DP, HDMI Constraints

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt & DisplayPort Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	*	*	TBTDP_2OTHER
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_TX	*_RX	*	TBTDP_TXRX
TBTDP_RX	*_TX	*	TBTDP_TXRX

DisplayPort & HDMI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?
HDMICLK_2DPHDMI	*	=4x_DIELECTRIC	?
HDMIDATA_2SAME	*	=3x_DIELECTRIC	?
HDMIDATA_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DPHDMI	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMIDATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMIDATA_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDMI_DATA	*	*	HDMIDATA_2OTHER
HDMI_DATA	=SAME	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_TX	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_RX	*	TBTDP_TXRX
HDMI_CLK	*	*	HDMICLK_2OTHER
HDMI_CLK	HDMI_DATA	*	HDMICLK_2DPHDMI
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DPHDMI
HDMI_CLK	TBTDP_TX	*	HDMICLK_2DPHDMI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_2OTHER
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	HDMI_DATA	*	DP_2SAME
DISPLAYPORT	TBTDP_TX	*	DP_2SAME
DISPLAYPORT	TBTDP_RX	*	TBTDP_TXRX

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
SPI_TBT_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	25
SPI_TBT_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	25
SPI_TBT_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	25
SPI_TBT_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	25
DP_HDMI_TBT_ML	DP_85D	DISPLAYPORT	DP_HDMI_TBT_ML_P<3..0>	67 69
DP_HDMI_TBT_ML	DP_85D	DISPLAYPORT	DP_HDMI_TBT_ML_N<3..0>	67 69
DP_HDMI_TBT_AUX	DP_85D		DP_HDMI_TBT_AUX_P	67 69
DP_HDMI_TBT_AUX	DP_85D		DP_HDMI_TBT_AUX_N	67 69
HDMI_CLOCK	HDMI_85D	HDMI_CLK	HDMI_IG_CLK_C_P	66 67 71
HDMI_CLOCK	HDMI_85D	HDMI_CLK	HDMI_IG_CLK_C_N	66 67 71
HDMI_DATA	HDMI_85D	HDMI_DATA	HDMI_IG_DATA_C_P<2..0>	66 67 71
HDMI_DATA	HDMI_85D	HDMI_DATA	HDMI_IG_DATA_C_N<2..0>	66 67 71

Only used on hosts supporting Thunderbolt video-in

Thunderbolt, DP, HDMI Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A_R2D_C_P<1..0>	25 28 71
TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A_R2D_C_N<1..0>	25 28 71
TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A_R2D_P<1..0>	28 71
TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A_R2D_N<1..0>	28 71
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	25 28
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	25 28
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	28
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	28
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	28
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	28
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	25 28
1355 DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	25 28
1354 DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	28
1353 DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	28
1352 DP_TBTPA_ML	DP_85D	DISPLAYPORT		
TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A_D2R_C_P<0>	28 71
TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A_D2R_C_N<0>	28 71
TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A_D2R_P<0>	25 28 71
TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A_D2R_N<0>	25 28 71
1343 TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R_C_P<1>	28 71
1342 TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R_C_N<1>	28 71
1341 TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R_P<1>	25 28 71
1340 TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R_N<1>	25 28 71
TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P	28
TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N	28
DP_TBTPA_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P	25 28
DP_TBTPA_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N	25 28
DP_TBTPA_AUXCH	DP_85D		DP_TBTPA_AUXCH_P	28
DP_TBTPA_AUXCH	DP_85D		DP_TBTPA_AUXCH_N	28
TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B_R2D_C_P<1..0>	25 29 71
TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B_R2D_C_N<1..0>	25 29 71
TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B_R2D_P<1..0>	29 71
TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B_R2D_N<1..0>	29 71
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	25 29
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	25 29
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	29
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	29
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	29
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	29
1351 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	25 29
1350 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	25 29
1348 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	29
1349 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	29
TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B_D2R_C_P<0>	29 71
TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B_D2R_C_N<0>	29 71
TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B_D2R_P<0>	25 29 71
TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B_D2R_N<0>	25 29 71
1347 TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R_C_P<1>	29 71
1346 TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R_C_N<1>	29 71
1344 TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R_P<1>	25 29 71
1345 TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R_N<1>	25 29 71
TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P	29
TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N	29
DP_TBTPB_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P	25 29
DP_TBTPB_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N	25 29
DP_TBTPB_AUXCH	DP_85D		DP_TBTPB_AUXCH_P	29
DP_TBTPB_AUXCH	DP_85D		DP_TBTPB_AUXCH_N	29
1338 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	5 25
1339 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	5 25
1336 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	25
1337 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	25
1335 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_C_P	13 25
1334 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_C_N	13 25
1324 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	25
1333 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	25
1332 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	25 67
1330 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	25 67
1331 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	25
1328 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	25
1329 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_C_P	25 67
1327 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_C_N	25 67
1325 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P	25
1326 DP_TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N	25
1358 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	65
1360 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	65
1316 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	5 65
1315 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	5 65
1357 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	65 71
1359 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	65 71
1320 DP_INT_AUXCH	DP_85D		DP_INT_AUXCH_C_P	5 65
1321 DP_INT_AUXCH	DP_85D		DP_INT_AUXCH_C_N	5 65
1322 DP_INT_AUXCH	DP_85D		DP_INT_AUX_P	65 71
1323 DP_INT_AUXCH	DP_85D		DP_INT_AUX_N	65 71

Notes:
AUX and DDC was removed from DISPLAYPORT or TBTDP_RX/TX because it's not high speed, and to save routing space.

Only used on dual-port hosts.

SYNC_MASTER=GKOO_J52 SYNC_DATE=12/06/2013

PAGE TITLE: TBT,DP,HDMI Constraints

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D
REVISION: 8.0.0
BRANCH: dvt1
PAGE: 115 OF 120
SHEET: 77 OF 82

MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL CONST SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	33 34
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	33 34
S2_MEM_CKE	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	33 34
S2_MEM_CS	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	33 34
	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	34
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	33 34
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	33 34
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	33 34
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	33 34
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	33 34
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	33 34
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	33 34
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	33 34
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	33 34
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	33 34
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	33 34
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	33 34
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	33 34
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	33 34
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	33 34
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	33 34 71
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	33 34 71
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	34 71
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	34 71
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	33 34 71
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	33 34 71
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	34 71
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	34 71
		S2_MEM_PWR	PP1V35_CAM	33 34
		S2_MEM_PWR	PP0V675_CAM_VREF	33 34
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	34
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ	34

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SMC SMBus & Charger Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	38 41 71
SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	38 41 71
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	38 41 71
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	38 41 71
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	38 41
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	38 41
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SCL	38 41 71
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	38 41 71
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SCL	38 41
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SDA	38 41

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
THERM_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
DIG_AUDIO	*	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	0.1 MM	0.1 MM
ANL_AUDIO	*	=1TO1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
ANL_AUDIO_WIDE	*	=1TO1_DIFFPAIR	0.3 MM	0.3 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.070 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.100 MM	500 MIL		
CPU_27P4S	BOTTOM			0.230 MM	100 MIL		
USB3_85D	TOP			0.100 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DP, SATA, HDMI, PCIE CONSTRAINT RELAXATIONS

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	P65_BGA
PCIE_85D	BGA	P65_BGA
CLK_PCIE_85D	BGA	P65_BGA
HDMI_85D	BGA	P65_BGA

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SENSE_45S	*	SENSE_45S
THERM_45S	*	THERM_45S
DIG_AUDIO	*	DIG_AUDIO
ANL_AUDIO	*	ANL_AUDIO

X304 Specific Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
THERM_DP_TBT_D1	THERM_45S	THERM	TBTTHMSNS_D1_P	45
THERM_DP_TBT_D1	THERM_45S	THERM	TBTTHMSNS_D1_N	45
THERM_DP_CPU_D1	THERM_45S	THERM	CPUTHMSNS_D1_P	45
THERM_DP_CPU_D1	THERM_45S	THERM	CPUTHMSNS_D1_N	45
THERM_DP_CPU_D2	THERM_45S	THERM	CPUTHMSNS_D2_P	45
THERM_DP_CPU_D2	THERM_45S	THERM	CPUTHMSNS_D2_N	45
SENSE_DP	SENSE_45S	SENSE	ISNS_CPUDDR_P	43
SENSE_DP	SENSE_45S	SENSE	ISNS_CPUDDR_N	43
SENSE_DP_LCDBKLT	SENSE_45S	SENSE	ISNS_LCDBKLT_P	42 60
SENSE_DP_LCDBKLT	SENSE_45S	SENSE	ISNS_LCDBKLT_N	42 60
SENSE_DP_TBT	SENSE_45S	SENSE	ISNS_TBT_P	44
SENSE_DP_TBT	SENSE_45S	SENSE	ISNS_TBT_N	44
SENSE_DP	SENSE_45S	SENSE	ISNS_LCDPANEL_P	44 65
SENSE_DP	SENSE_45S	SENSE	ISNS_LCDPANEL_N	44 65
	SENSE_45S	SENSE	ISNS_HS_COMPUTING_P	42 44
	SENSE_45S	SENSE	ISNS_HS_COMPUTING_N	42 44
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_OTHER5V_P	42
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_OTHER5V_N	42
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_OTHER3V3_P	42
SENSE_DP	SENSE_45S	SENSE	ISNS_HS_OTHER3V3_N	42
SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR_ISNS_P	43
SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR_ISNS_N	43
SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR_ISNS_R_P	43
SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR_ISNS_R_N	43
SENSE_DP	SENSE_45S	SENSE	ISNS_1V05_S0_P	43 59
SENSE_DP	SENSE_45S	SENSE	ISNS_1V05_S0_N	43 59
SENSE_DP	SENSE_45S	SENSE	ISNS_SSD_P	43
SENSE_DP	SENSE_45S	SENSE	ISNS_SSD_N	43
SENSE_DP	SENSE_45S	SENSE	ISNS_TPAD_P	42
SENSE_DP	SENSE_45S	SENSE	ISNS_TPAD_N	42
SENSE_DP	SENSE_45S	SENSE	ISNS_1V8_S3_P	43 61
SENSE_DP	SENSE_45S	SENSE	ISNS_1V8_S3_N	43 61
SENSE_DP	SENSE_45S	SENSE	ISNS_PP3V3S0_P	43
SENSE_DP	SENSE_45S	SENSE	ISNS_PP3V3S0_N	43
SENSE_DP	SENSE_45S	SENSE	ISNS_PP5VS0_P	43
SENSE_DP	SENSE_45S	SENSE	ISNS_PP5VS0_N	43
SENSE_DP_CPUHIGN	SENSE_45S	SENSE	ISNS_CPUHIGAIN_P	44 45
SENSE_DP_CPUHIGN	SENSE_45S	SENSE	ISNS_CPUHIGAIN_N	44 45
SENSE_DP_CPUHIGN	SENSE_45S	SENSE	ISNS_CPUHIGAIN_R_P	44
SENSE_DP_CPUHIGN	SENSE_45S	SENSE	ISNS_CPUHIGAIN_R_N	44
SENSE_DP_CHGR_CSI	SENSE_45S	SENSE	CHGR_CSI_P	54
SENSE_DP_CHGR_CSI	SENSE_45S	SENSE	CHGR_CSI_N	54
SENSE_DP_CHGR_CSI	SENSE_45S	SENSE	CHGR_CSI_R_P	54
SENSE_DP_CHGR_CSI	SENSE_45S	SENSE	CHGR_CSI_R_N	54
SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR_CSO_P	54
SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR_CSO_N	54
SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR_CSO_R_P	44 54
SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR_CSO_R_N	44 54

The signals below have no topologies assigned.

DP_NO_TOPOLOGY	SENSE_45S	SENSE	CPUVR_ISNS1_P	43 56
DP_NO_TOPOLOGY	SENSE_45S	SENSE	CPUVR_ISNS1_N	43 56
DP_NO_TOPOLOGY	SENSE_45S	SENSE	CPUVR_ISNS2_P	43 56
DP_NO_TOPOLOGY	SENSE_45S	SENSE	CPUVR_ISNS2_N	43 56

X304 Specific Net Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING		
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LO2_L_P	48 50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LO2_L_N	48 50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LIN_P	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LIN_N	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_LIN_P	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_LIN_N	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LO2_R_P	48 50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LO2_R_N	48 50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RIN_P	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RIN_N	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_RIN_P	50
AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_RIN_N	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_LO3_L_P	48 50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_LO3_L_N	48 50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LSUBIN_P	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LSUBIN_N	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	LSUBIN_P	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	LSUBIN_N	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_LO3_R_P	48 50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_LO3_R_N	48 50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RSUBIN_P	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RSUBIN_N	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	RSUBIN_P	50
AUDIO_DP_AMPSUB	ANL_AUDIO	AUDIO	RSUBIN_N	50
AUDIO_DP_SPKSUB	DIG_AUDIO	AUDIO	SPKRCONN_SL_OUT_P	50 52 71
AUDIO_DP_SPKSUB	DIG_AUDIO	AUDIO	SPKRCONN_SL_OUT_N	50 52 71
AUDIO_DP_SPKSUB	DIG_AUDIO	AUDIO	SPKRCONN_SR_OUT_P	50 52 71
AUDIO_DP_SPKSUB	DIG_AUDIO	AUDIO	SPKRCONN_SR_OUT_N	50 52 71
AUDIO_DP_SPKTWT	DIG_AUDIO	AUDIO	SPKRCONN_L_OUT_P	50 52 71
AUDIO_DP_SPKTWT	DIG_AUDIO	AUDIO	SPKRCONN_L_OUT_N	50 52 71
AUDIO_DP_SPKTWT	DIG_AUDIO	AUDIO	SPKRCONN_R_OUT_P	50 52 71
AUDIO_DP_SPKTWT	DIG_AUDIO	AUDIO	SPKRCONN_R_OUT_N	50 52 71
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CH_HS_GND	48 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_HS_MIC_P	
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_SLEEVE	52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_SLEEVE_XW	51 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HP_PORT_REFCH	48 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HS_MIC_P	51 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	CODEC_HS_MIC_P	48
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	HS_MIC_P	48 51
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_HS_MIC_N	
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_RING2	52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_RING2_XW	51 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HP_PORT_REFUS	48 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HS_MIC_N	51 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_US_HS_GND	48 52
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	HS_MIC_N	48 51
AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	CODEC_HS_MIC_N	48
		SB_POWER	PP3V3_S5	68 71
		SB_POWER	PP3V3_S0	68 71
		GND	GND	

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PCI Express Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=3X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER
PCIE_TX	*_RX	*	PCIE_TXRX
PCIE_RX	*_TX	*	PCIE_TXRX

PCI Express Properties

ELECTRICAL CONST SET	NET TYPE PHYSICAL	NET TYPE SPACING	
PCIE_SSD_D2R	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_P<3..1> 12 32 71
PCIE_SSD_D2R	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_N<3..1> 12 32 71
PCIE_SSD_D2R_PP	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_P<0> 12 32 71
PCIE_SSD_D2R_PP	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_N<0> 12 32 71
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_C_P<3..0> 12 32 71
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_C_N<3..0> 12 32 71
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_P<3..0> 32 71
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_N<3..0> 32 71
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_P<0> 14 25 71
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_N<0> 14 25 71
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_P<0> 25
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_N<0> 25
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_P<3..1> 14 25 71
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_N<3..1> 14 25 71
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_P<3..1> 25 71
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_N<3..1> 25 71
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_P<3..0> 25 71
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_N<3..0> 25 71
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_C_P<3..0> 14 25 71
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_C_N<3..0> 14 25 71
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_P 66 71
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_N 66 71
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_C_P 14 66 71
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_C_N 14 66 71
PCIE_AP_D2R	PCIE_85D	PCIE_RX	PCIE_AP_D2R_P 14 66 71
PCIE_AP_D2R	PCIE_85D	PCIE_RX	PCIE_AP_D2R_N 14 66 71
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P 66
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N 66
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P 12 66 71
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N 12 66 71
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P 12 34 71
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N 12 34 71
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P 33 34
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N 33 34
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P 12 32 71
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N 12 32 71
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_RC1_P 32
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_RC1_N 32
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_RC2_P 32
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_RC2_N 32
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P 12 25 71
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N 12 25 71
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE_CAMERA_D2R_P 14 34 71
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE_CAMERA_D2R_N 14 34 71
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE_CAMERA_D2R_C_P 33 34
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE_CAMERA_D2R_C_N 33 34
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE_CAMERA_R2D_P 33 34
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE_CAMERA_R2D_N 33 34
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE_CAMERA_R2D_C_P 14 34
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE_CAMERA_R2D_C_N 14 34

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Kismet:
AFP://KISMET.APPLE.COM/KISMET-PROJECTS/X304

Useful Wiki Links:
Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions
Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

MobileMac HW Radar:
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