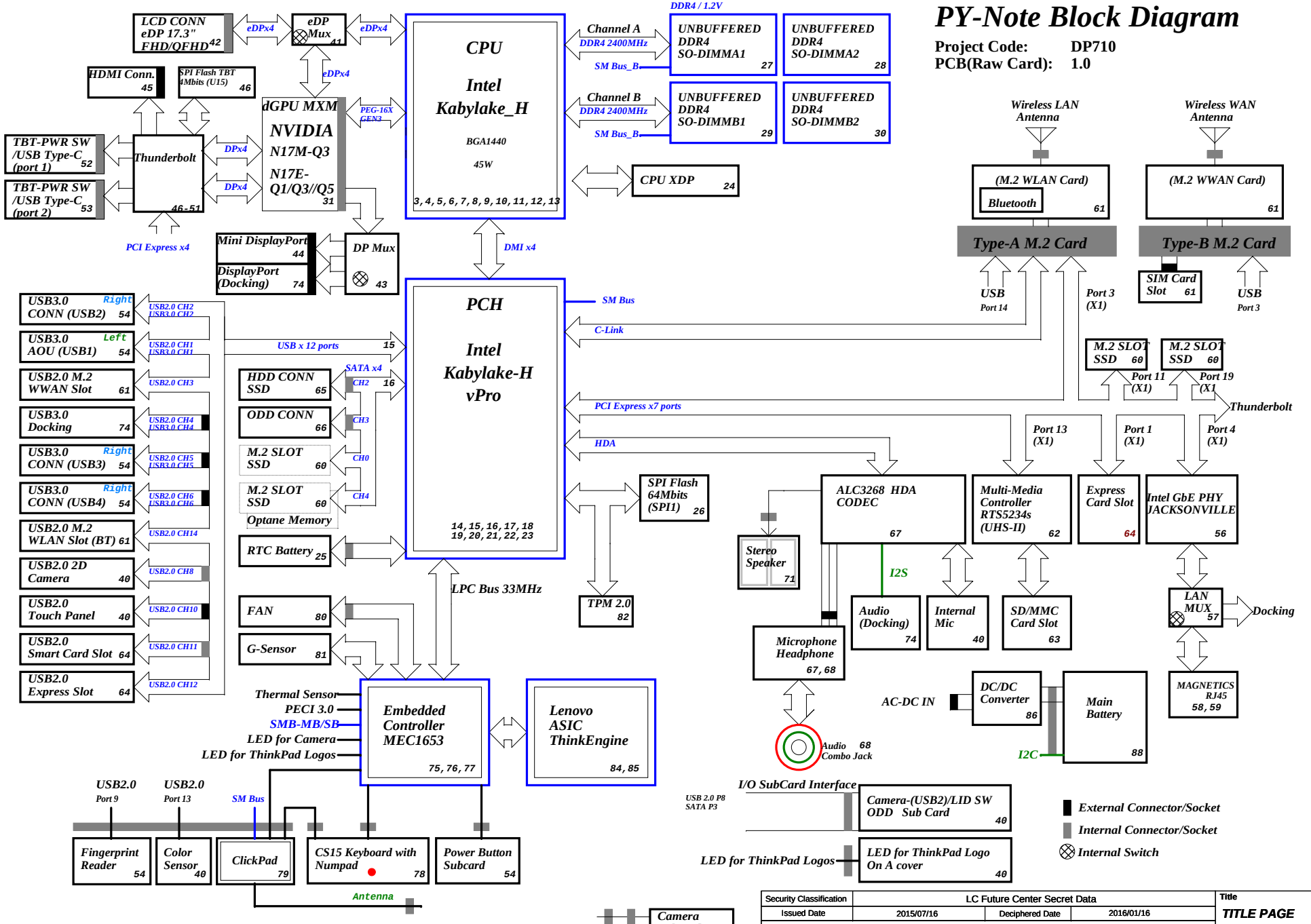
PY-Note Block Diagram

Project Code: DP710
PCB(Raw Card): 1.0



PCB Layer Stackup

L1:TOP
L2:GND
L3:Signal
L4:PWR
L5:Signal
L6:Signal
L7:GND
L8:Signal
L9:GND
L10:BOTTOM

Battery Charger

BQ24780SRUYR 88

INPUTS	OUTPUTS
DOCK_PWR20	M-BAT-PWR

System DC/DC

TPS51285BRUKR 90

VINT20	VCC5M VCC3M

CPU DC/DC

M: NCP81205MNTXG 91
S: NCP81382MNTXG 92, 93, 94

VINT20	VCCCPUCORE VCCGFXCORE_1 VCCSA

VCCCPUIO

NB681GD-C623-Z 95

VCC5M	VCCCPUIO

VCC1R0_SUS

TPS51362RVER 96

VCC5M	VCC1R0_SUS

VCC1R2A/VCC0R6B +SMDDR_VREF_DIMM

TPS51716RUKR 99

VINT20	+SMDDR_VREF_DIMM VCC0R6B VCC1R2A

VCC1R8B

BD9B300MUV-E2 98

VCC5M	VCC1R8B

VCC2R5A

BD91364AMUU-ZE2 100

VCC5M	VCC2R5A

VCCOPC/VCCEOPIO(44e)

NB681GD-C623-Z 101
NB681GD-C623-Z 103

VCC5M VCC5M	VCCOPC VCCEOPIO

VCCGTX (44e)

NCP81210MNTXG 102

VINT20	VCCGTX

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Issued Date	2015/07/16	Deciphered Date	2016/01/16

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Title: TITLE PAGE
Size: Custom
Document Number: PAYTON
Rev: 0.1
Date: Wednesday, December 07, 2016
Sheet 1 of 111

TABLE: SYSTEM POWER STATE

Power state to be determined

EC SMBus0 address

Device	Address
Smart Battery	0001 011X b

EC SMBus1 address

Device	Address
G-Senor (LIS3DH)	0011 000Xb
G-Senor (KX023)	0011 110Xb

EC SMBus2 address

Device	Address
Charge Controller	0001 0010

EC SMBus10 address

Device	Address
Master VGA	0x9E

PCH SM Bus address

Device		Address
CH-A P	DDR DIMM0	1001 0000b
CH-A S	DDR DIMM1	1001 0001b
CH-B P	DDR DIMM2	1001 0010b
CH-B S	DDR DIMM3	1001 0011b

PCH SM Bus0 address

Device	Address
Intel Lan_I219	0XC8

Schematics Mark Definition

BOM Structure	4+2 CPU	4+4e CPU	Note
@	NO ASM	NO ASM	
EMC@	ASM	ASM	EMC
RF@	ASM	ASM	RF
ME@	ASM	ASM	ME
PRxxx,PCxxx, PLxxx	ASM	ASM	Power
42@	ASM	NO ASM	4+2 CPU
44e@	NO ASM	ASM	4+4e CPU

Any other mark like below is prohibited on Payton/Walter.
ESD@,EMI@,EMC_NS@,EMC_PX@,EMC_OPT@,CONN@,
CONN_NS@... RH,CH,LH(PCH related RLC)..

Capacitor Naming Note

Ceramic Capacitors:

0.1U_0402_6.3VXX

- Tolerance
- Temperature Characteristics
- Rated Voltage
- Package Size

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7	8	9	A
Code	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R	NPO	C0G	X6S

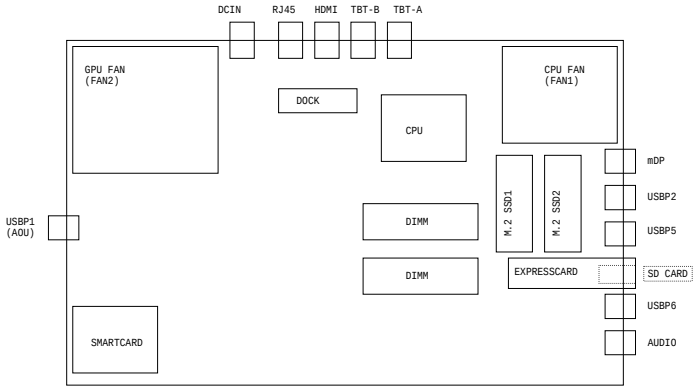
B	C	D	E	F	G	H	I	J	K	L
BJ	CH	CJ	CK	SH	SJ	UJ	UK	SL	X5S	NOJ

Tolerance:

Symbol	A	B	C	D	F	G	H	J	K	M	N
Tolerance	+-0.05PF	+-0.1PF	+-0.25PF	+-0.5PF	+-1%	+-2%	+-3%	+-5%	+-10%	+-20%	+-30%

Symbol	P	Q	V	X	Z	S	Y
Tolerance	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	+50,-20%	-30% ~ 10%

TABLE: SYSTEM COMPONENT PLACEMENT (AS OF 2014 Dec 8)



PCB_MB
XXX
PCB NM-B121
DAA00007D00

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Title: **Blank**

LCFC

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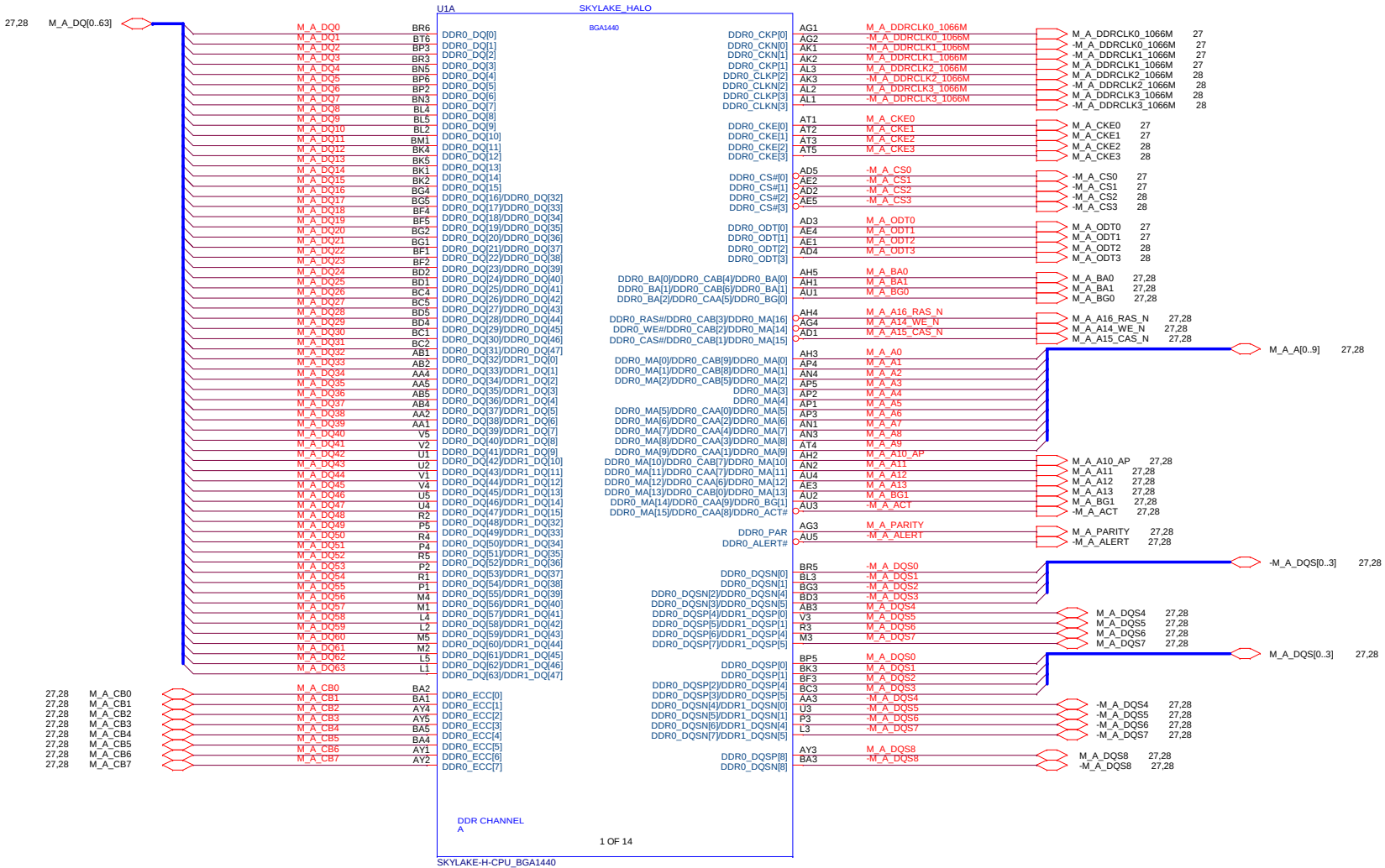

DDR4 INTERLEAVE IMPLEMENTATION

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Title: *CPU SKL-H : DDR4 CH-A*

LCFC

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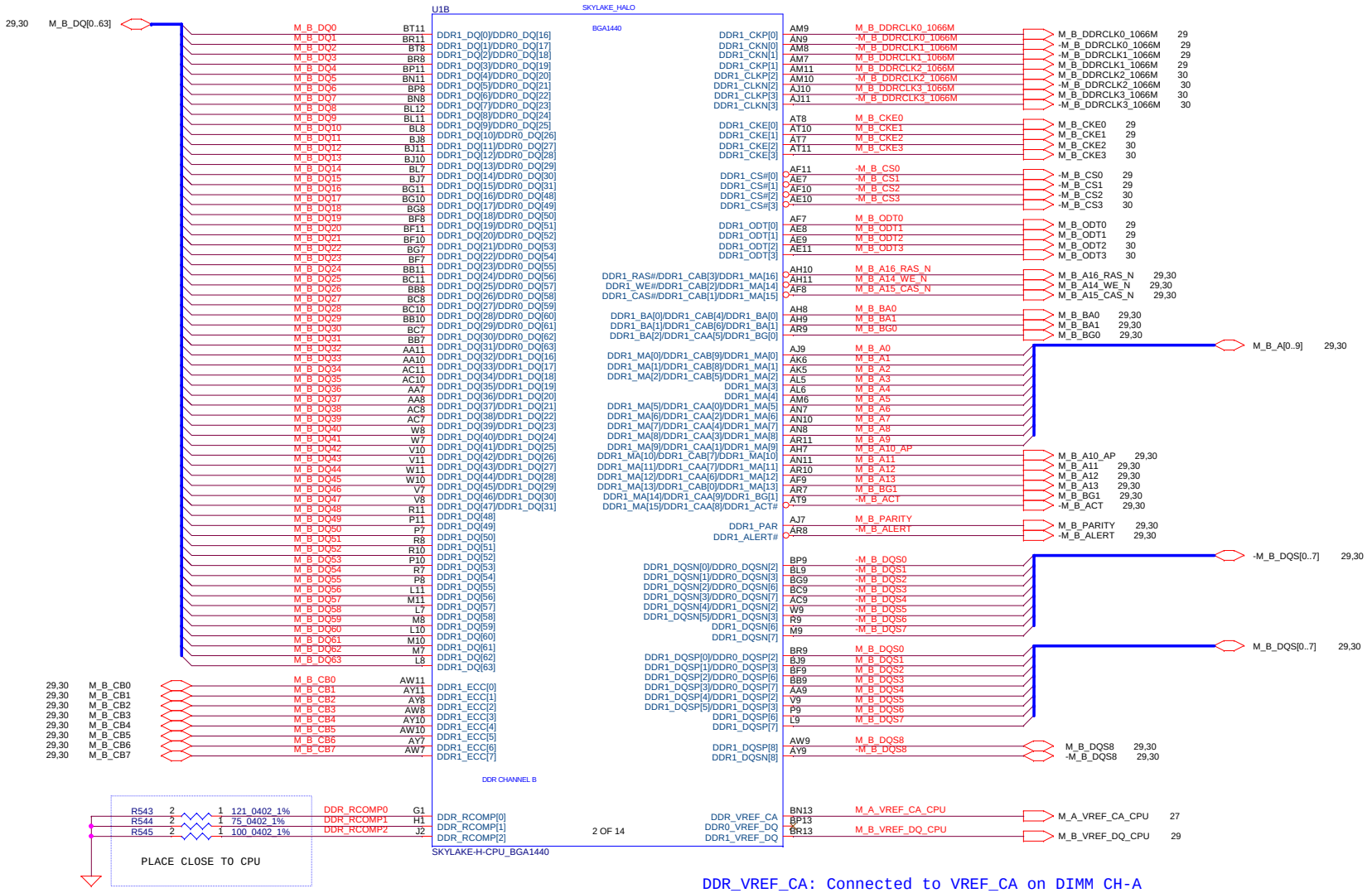
Date: Wednesday, December 07, 2016 | Sheet 3 of 111



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Title: CPU SKL-H : DDR4 CH-B

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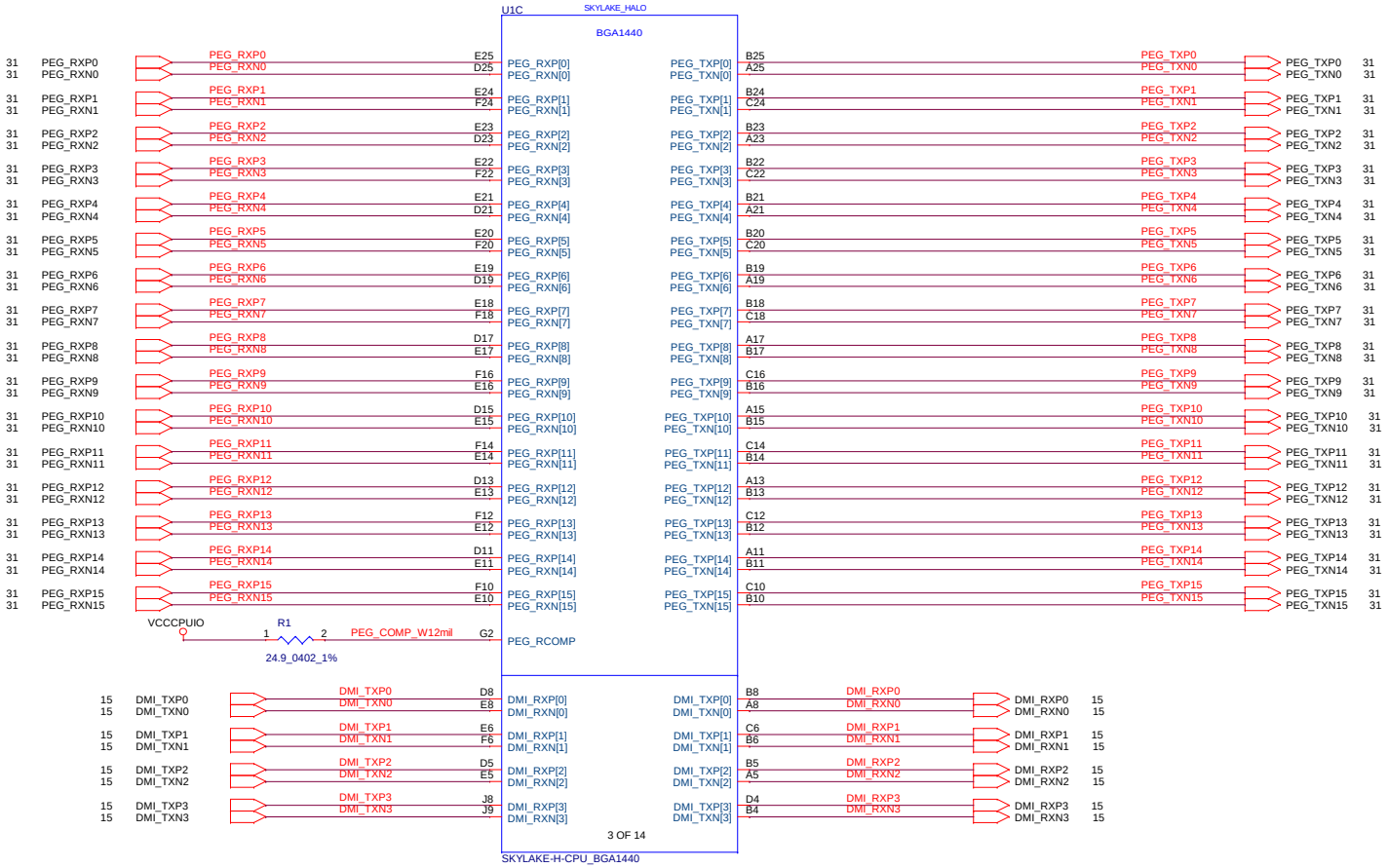

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Title: CPU SKL-H : PEG/DMI

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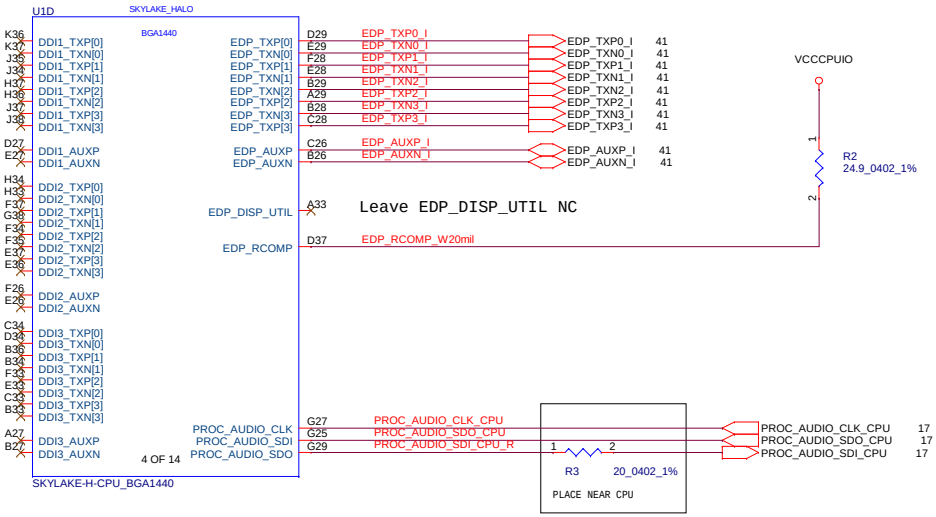
Date: Wednesday, December 07, 2016 | Sheet 5 of 111



Security Classification	LC Future Center Secret Data		
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Title: CPU SKL-H : DDI/EDP

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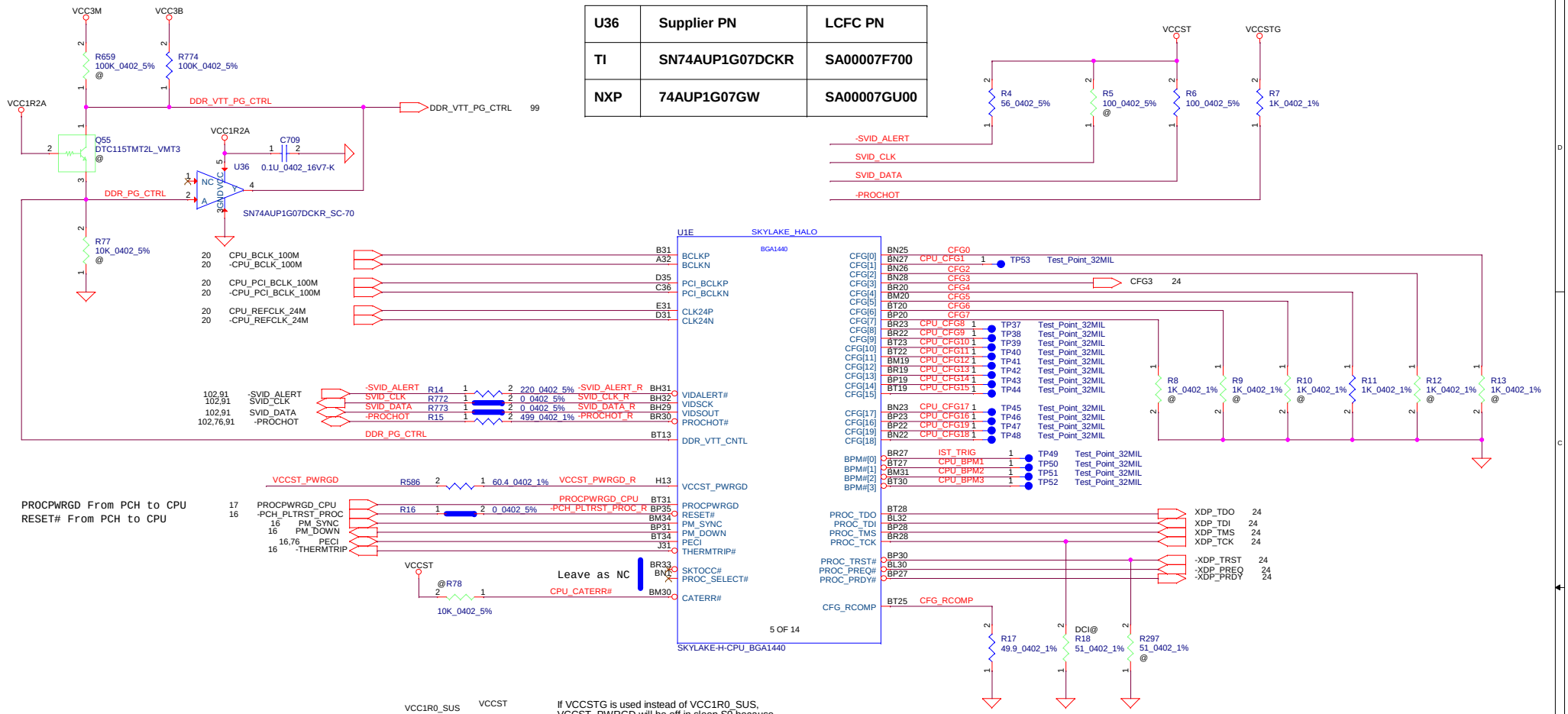
Date: Wednesday, December 07, 2016 | Sheet 6 of 111

U36	Supplier PN	LCFC PN
TI	SN74AUP1G07DCKR	SA00007F700
NXP	74AUP1G07GW	SA00007GU00



If VCCSTG is used instead of VCC1R0_SUS,
VCCST_PWRGD will be off in sleep S0 because
VCCSTG may be turned off when in sleep S0.
Currently, VCCSTG is still on in sleep S0,
but we may change logic to turn off VCCSTG in sleep S0.
(CT_20141216)

VCCST_PWRGD requirements (546884_SKL_H_PDG_Rev0_71)

1) Indication that the VCCST/VDDQ power supplies are stable and within specification. (Table 41-1)
2) VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST. (Figure 41-1 Note 1)
3) VCCST_PWRGD should be equal or ealier than PCH_PWROK. (Table 41-5, tCPU16. See also 543016_SKL_PDG_UY_1_0)
4) VCCST_PWRGD is typically made from ALL_SYS_PWRGD (CPUCORE_ON/VR_ON for CPU DCDC), not PCH_PWROK (CPUCORE_PWRGD). (Figure 41-1)

TABLE CFG[19:0] pin has internal Pull up to VCCCPUIO with 5-8 k ohm.

CFG[0] : Stall reset sequence after CPU PLL lock until de-asserted:
1 : No Stall ← LOGIC
0 : Stall

CFG[2] : PEG Static Lane Reversal
1 : Normal Operation ← LOGIC
0 : Lane Reversal

CFG[4] : eDP enable
1 : Disabled
0 : Enabled ← LOGIC

CFG[6:5] : PEG Bifurcation, bus#:dev#:func#=0:1:0
11 : 1x16 ← LOGIC

CFG[7] : PEG Training
1 : PEG Train immediately following RESET# deassertion ← LOGIC
0 : PEG Wait for BIOS for training

CFG[19:8] : Reserved

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Title: CPU SKL-H : MISC/CLK/JTAG/CFG

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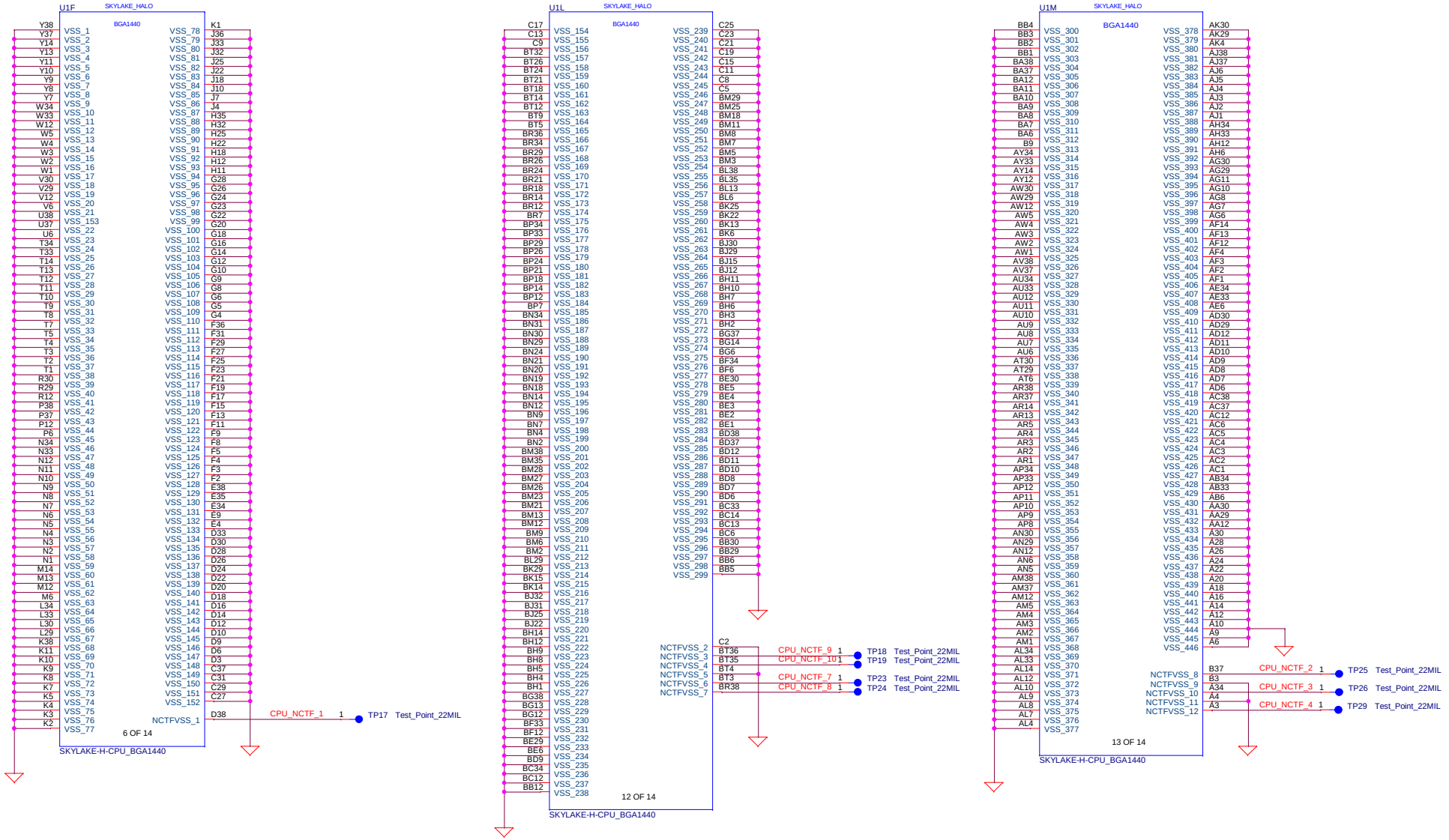
Date: Wednesday, December 07, 2016 | Sheet 7 of 111



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Title: **CPU SKL-H : GND**

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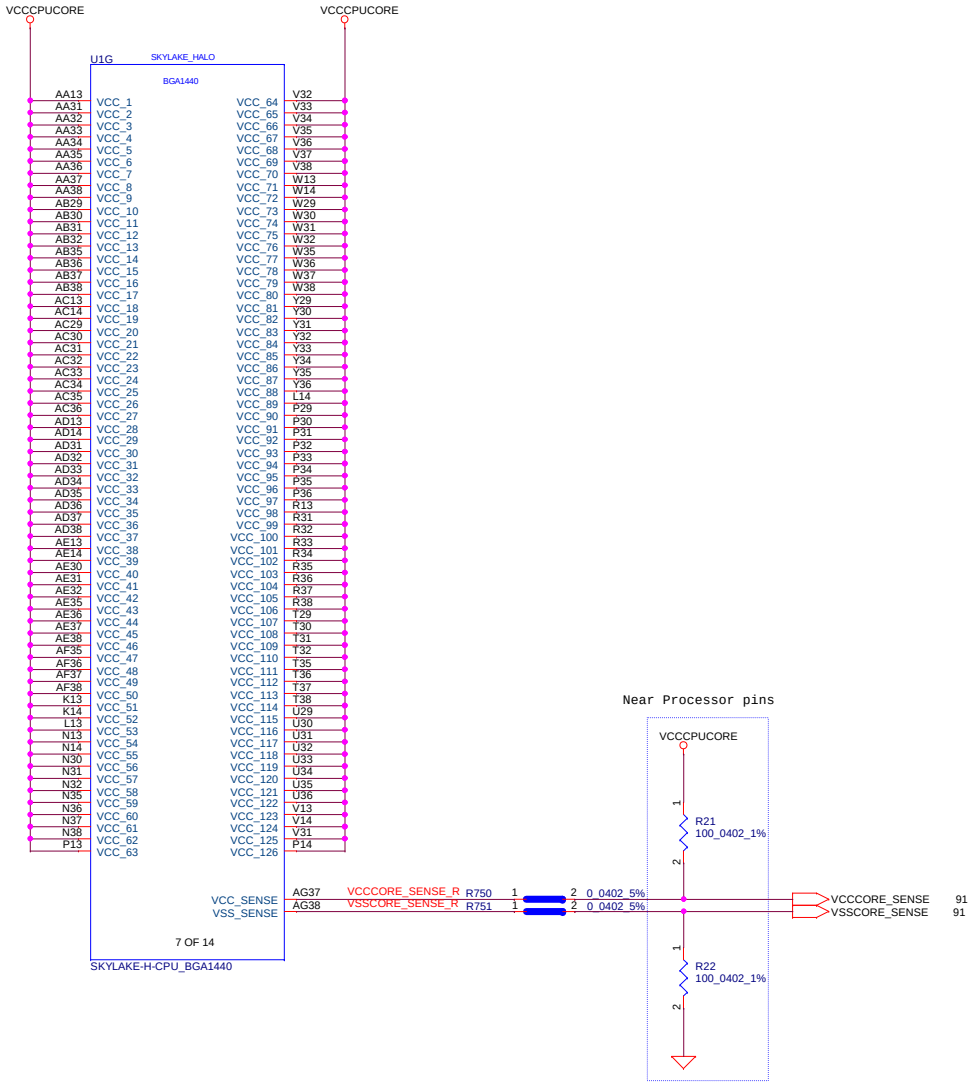

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Title: *CPU SKL-H : VCC*

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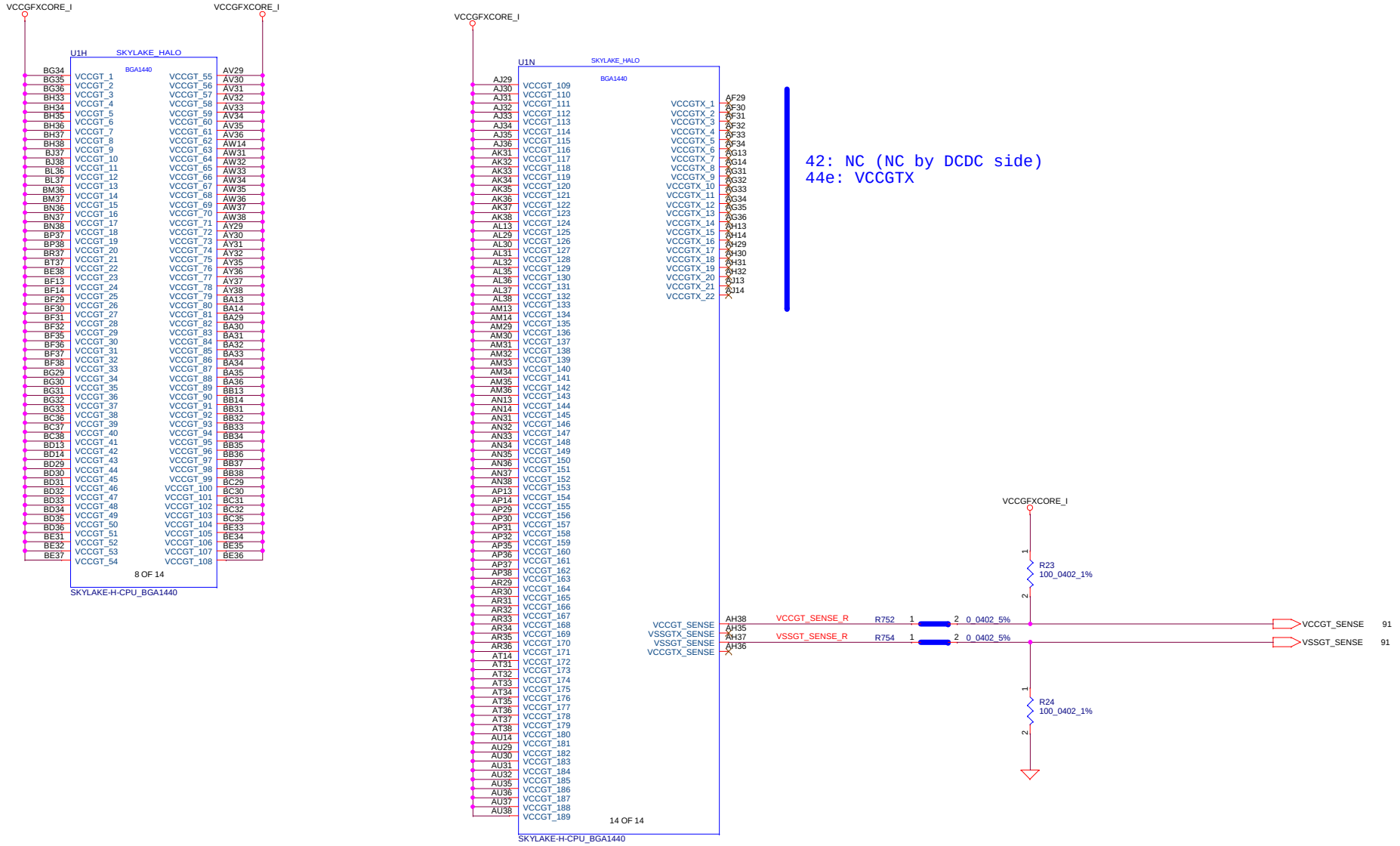
Date: Wednesday, December 07, 2016	Sheet 9 of 111	



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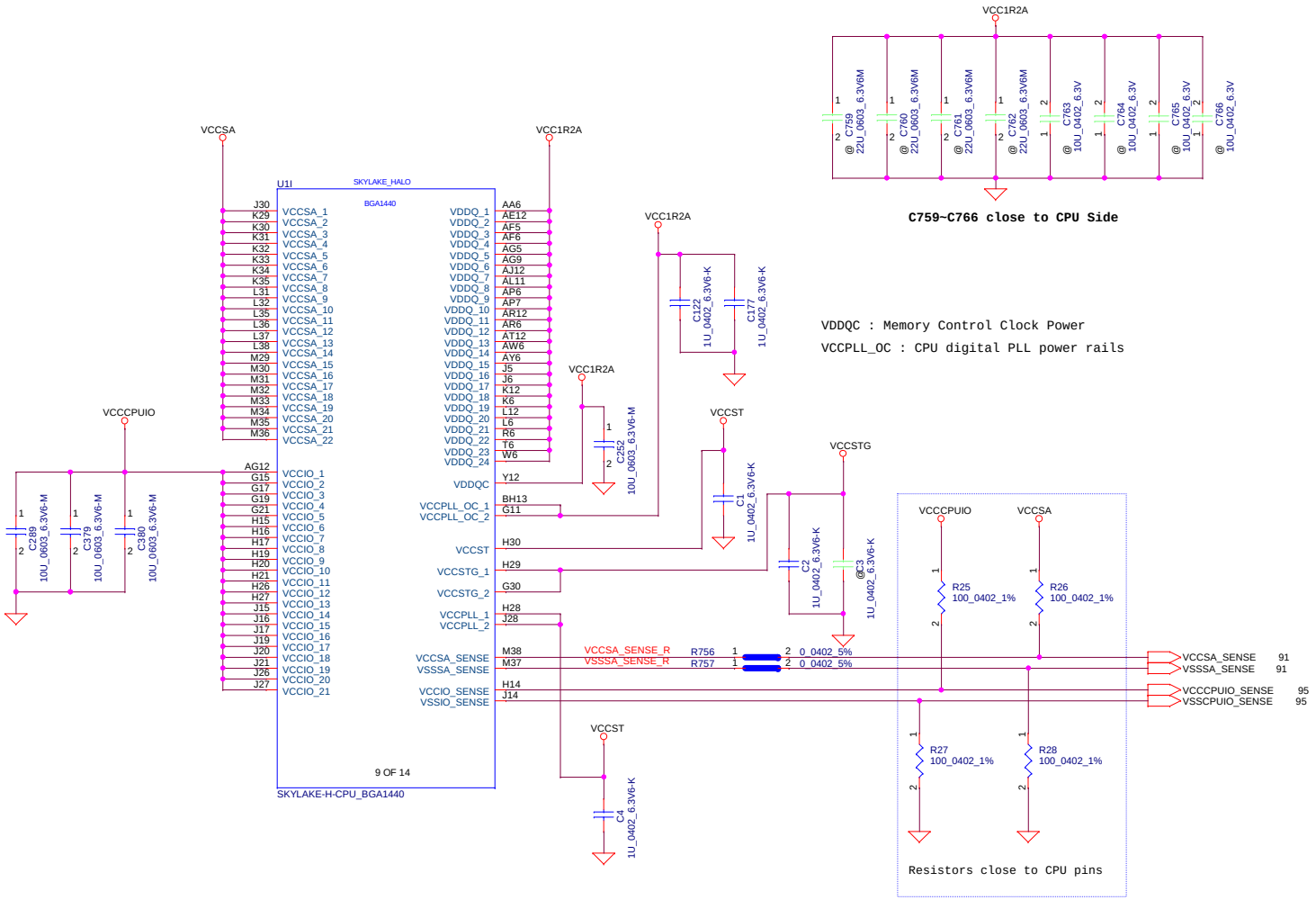
Title: CPU SKL-H : VCCGT/VCCGTX

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 10 of 111



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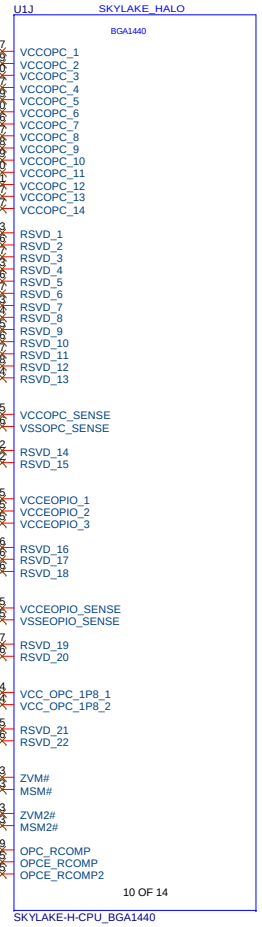
Title: *CPU SKL-H : VCCSA/VCCIO/VDDQ*

LCFC

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 11 of 111



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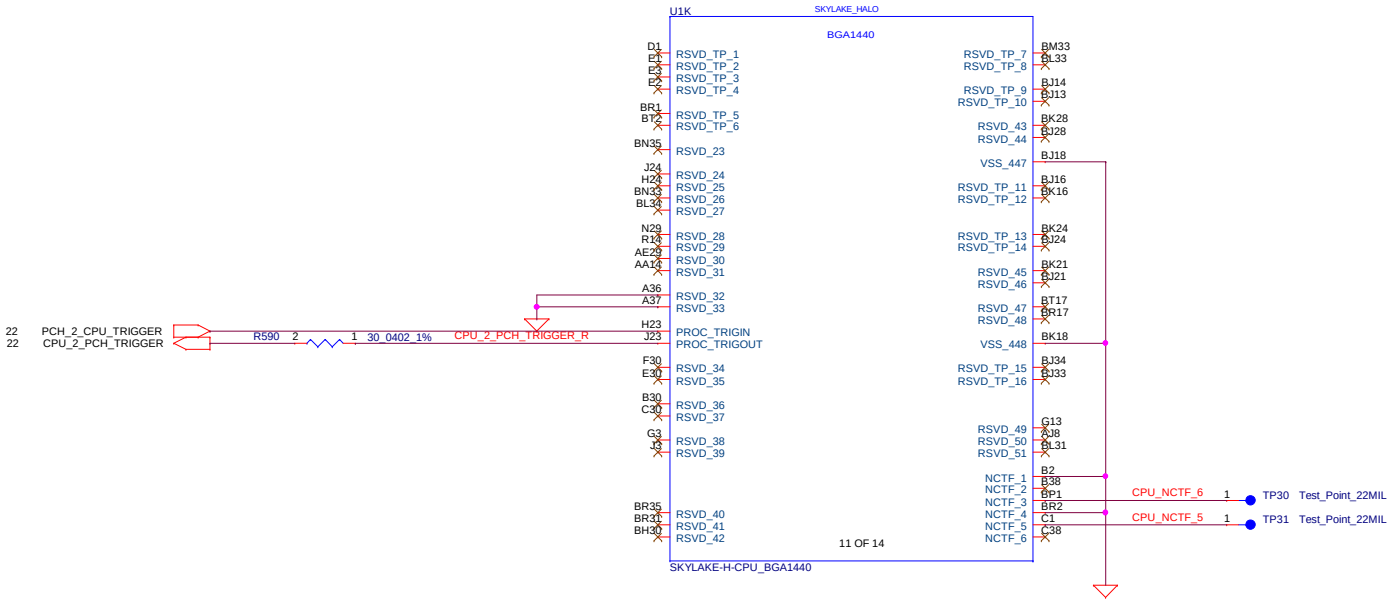
Title: *CPU SKL-H : VCCOPC/RSVD*

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 12 of 111



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Title: *CPU SKL-H : RSVD*

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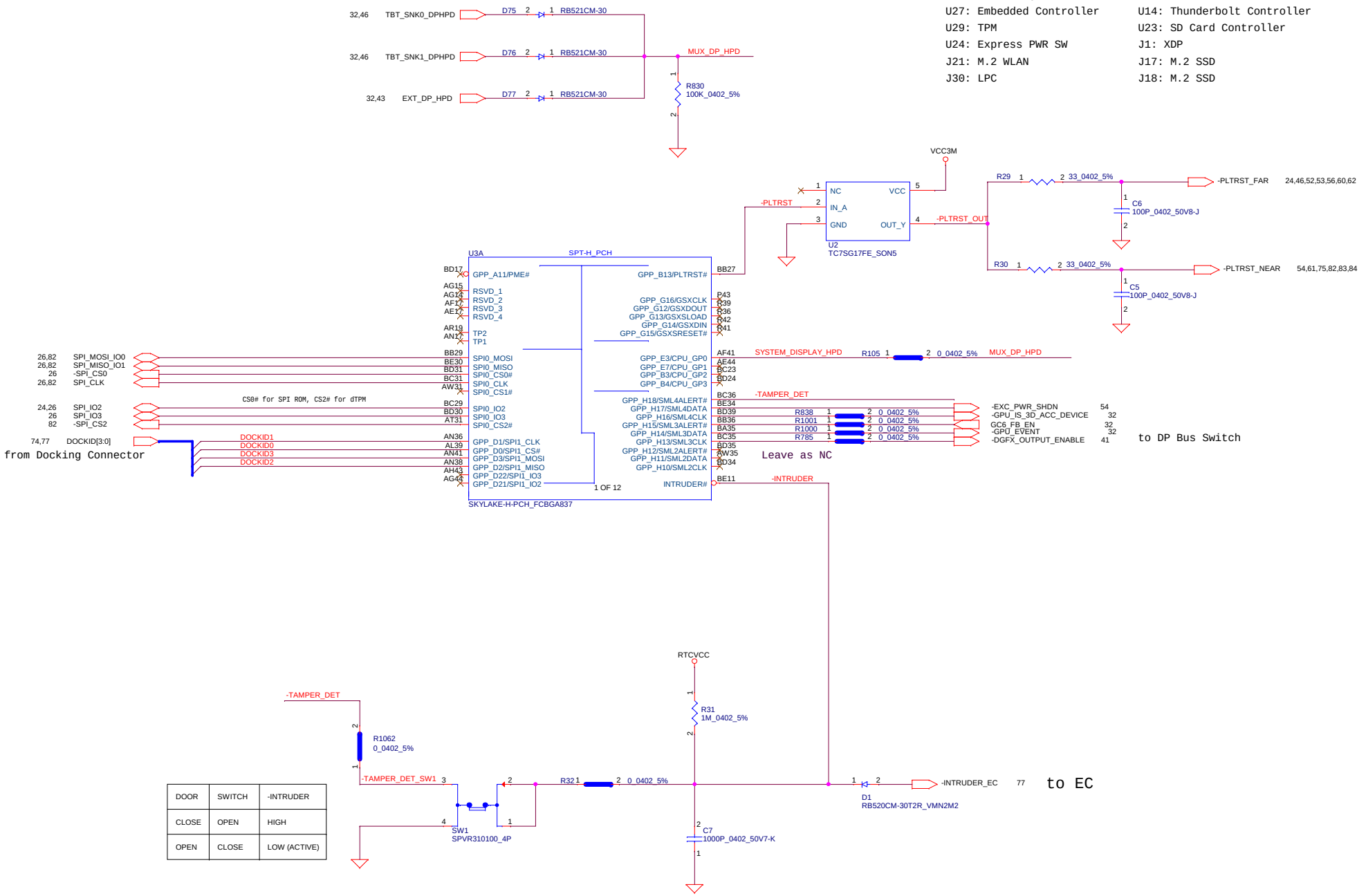
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 13 of 111

NEAR----------
U32: Think Engine 2
U27: Embedded Controller
U29: TPM
U24: Express PWR SW
J21: M.2 WLAN
J30: LPC

FAR----------
U21: GbE
U14: Thunderbolt Controller
U23: SD Card Controller
J1: XDP
J17: M.2 SSD
J18: M.2 SSD



DOOR	SWITCH	-INTRUDER
CLOSE	OPEN	HIGH
OPEN	CLOSE	LOW (ACTIVE)

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Title: PCH SKL-H : SPI

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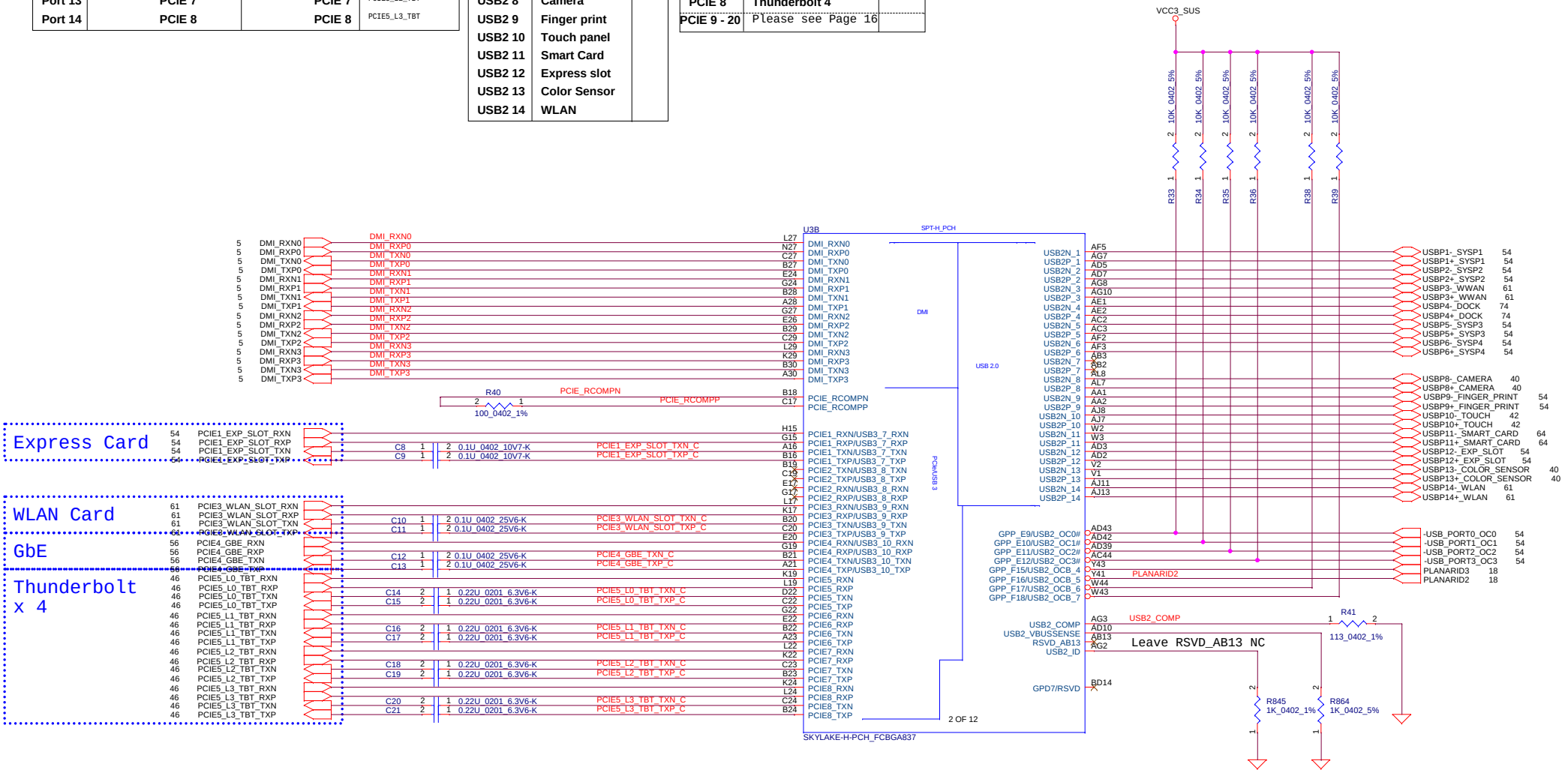
Date: Wednesday, December 07, 2016 | Sheet 14 of 111

Flexible I/O Configuration (v0.51)			
I/O	High Speed Signals	Configuration	Net Name
Port 1 - 6		Please see Page 19	
Port 7	USB3 7 / PCIE 1	USB3 7 or PCIE 1	PCIE1_EXP_SLOT
Port 8	USB3 8 / PCIE 2	USB3 8	
Port 9	USB3 9 / PCIE 3	PCIE 3	PCIE3_WLAN_SLOT
Port 10	USB3 10 / PCIE 4 (GBE)	GBE	PCIE4_GBE
Port 11	PCIE 5 (GBE)	PCIE 5	PCIE5_L0_TBT
Port 12	PCIE 6	PCIE 6	PCIE5_L1_TBT
Port 13	PCIE 7	PCIE 7	PCIE5_L2_TBT
Port 14	PCIE 8	PCIE 8	PCIE5_L3_TBT

USB2.0 Configuration (v0.51)		
USB2 #	Assignment	OCx #
USB2 1	System Port 1	0
USB2 2	System Port 2	1
USB2 3	WWAN	
USB2 4	DOCK	
USB2 5	System Port 3	2
USB2 6	System Port 4	3
USB2 7	Reserved	
USB2 8	Camera	
USB2 9	Finger print	
USB2 10	Touch panel	
USB2 11	Smart Card	
USB2 12	Express slot	
USB2 13	Color Sensor	
USB2 14	WLAN	

PCIE Configuration (v0.51)		
PCIE #	High Speed Signals	GEN
PCIE 1	Express slot	2
PCIE 2		
PCIE 3	WLAN Card	2
PCIE 4	GBE	
PCIE 5	Thunderbolt 1	3
PCIE 6	Thunderbolt 2	
PCIE 7	Thunderbolt 3	
PCIE 8	Thunderbolt 4	
PCIE 9 - 20	Please see Page 16	

USB3.0 Configuration (v0.51)	
USB 3#	High Speed Signals
USB3 1 - 6	Please see Page 19
USB3 7	
USB3 8	
USB3 9	
USB3 10	



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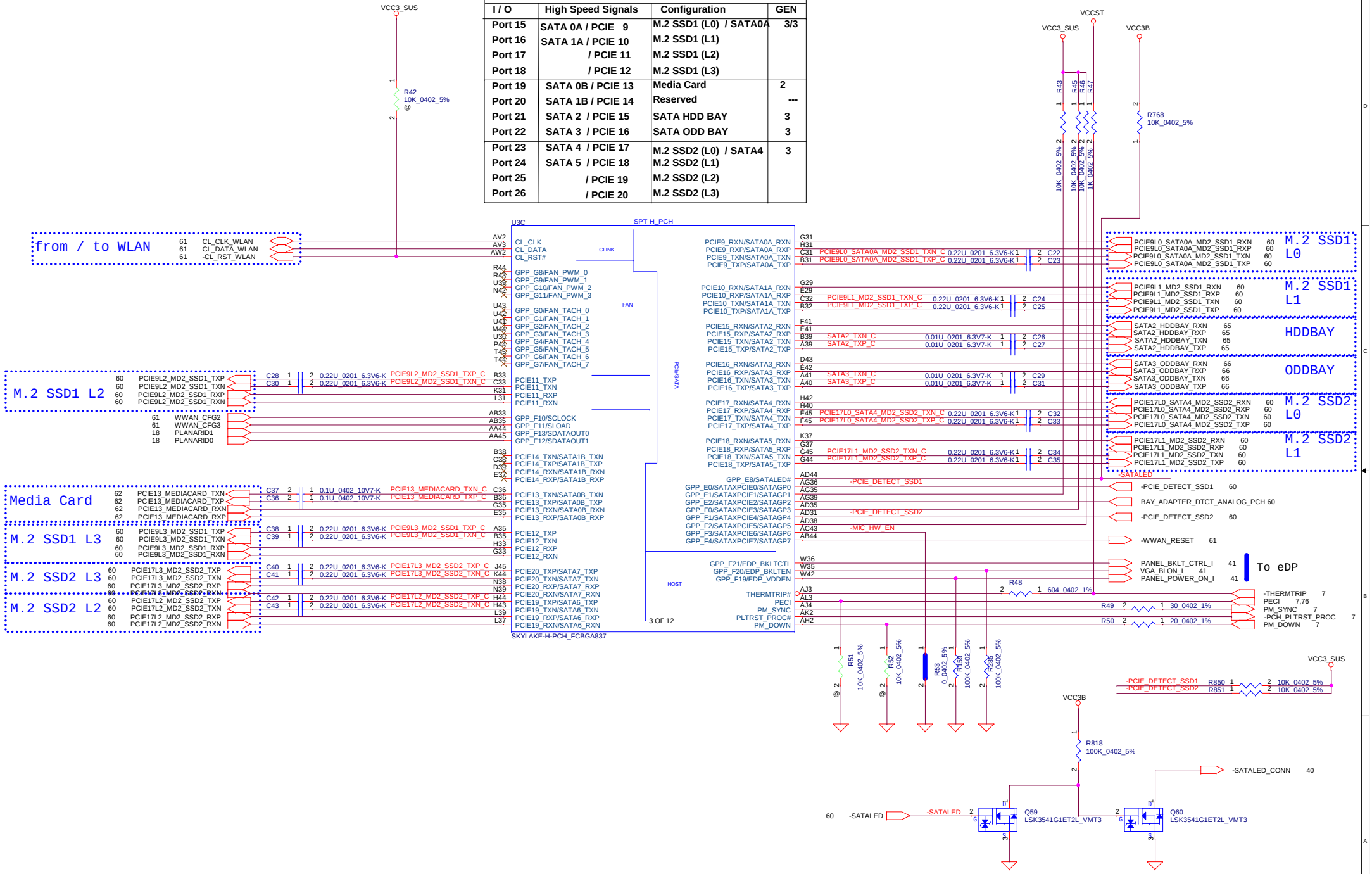
Title: PCH SKL-H : DMI/PCIE/USB

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 15 of 111

PCIE / SATA Configuration (v0.51)			
I / O	High Speed Signals	Configuration	GEN
Port 15	SATA 0A / PCIE 9	M.2 SSD1 (L0) / SATA0A	3/3
Port 16	SATA 1A / PCIE 10	M.2 SSD1 (L1)	
Port 17	/ PCIE 11	M.2 SSD1 (L2)	
Port 18	/ PCIE 12	M.2 SSD1 (L3)	
Port 19	SATA 0B / PCIE 13	Media Card	2
Port 20	SATA 1B / PCIE 14	Reserved	---
Port 21	SATA 2 / PCIE 15	SATA HDD BAY	3
Port 22	SATA 3 / PCIE 16	SATA ODD BAY	3
Port 23	SATA 4 / PCIE 17	M.2 SSD2 (L0) / SATA4	3
Port 24	SATA 5 / PCIE 18	M.2 SSD2 (L1)	
Port 25	/ PCIE 19	M.2 SSD2 (L2)	
Port 26	/ PCIE 20	M.2 SSD2 (L3)	



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Issued Date	2015/07/16	Deciphered Date	2016/01/16

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Title: PCH SKL-H : SATA/PCIE

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 16 of 111

TABLE : Functional Strap

HDA_SDO Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

HDA_SDO is used to update the Descriptor and/or the ME regions of the SPI after MFG Done bit is set.

TABLE : Functional Strap

GPP_C5/SML0ALERT# (LPC or eSPI)		
HIGH	eSPI is selected	
LOW	LPC is selected(Default)	<------LOGIC

TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)		
HIGH	Enable ME Crypto TLS with Confidentiality	
LOW	Disable ME Crypto TLS (Default)	<------LOGIC

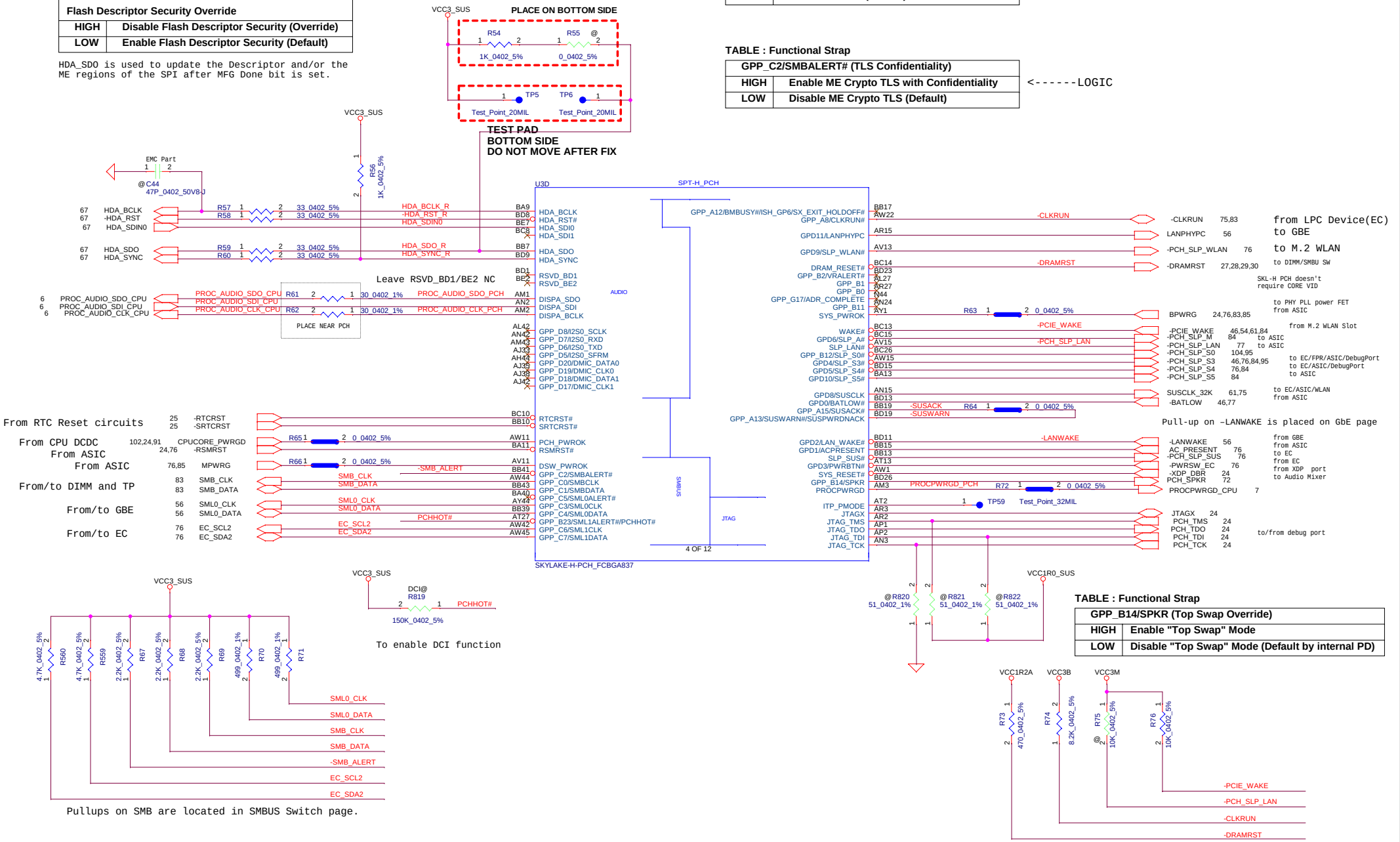

TABLE : Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default by internal PD)

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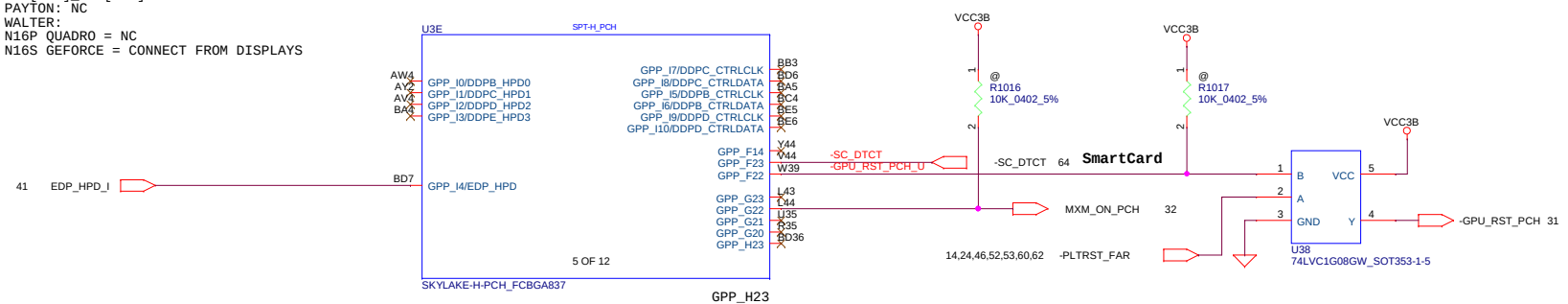
Title: PCH SKL-H : AUDIO/SMBUS/JTAG

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 17 of 111

DDP[B:D]_HPD[0:2]
PAYTON: NC
WALTER:
N16P QUADRO = NC
N16S GEFORCE = CONNECT FROM DISPLAYS

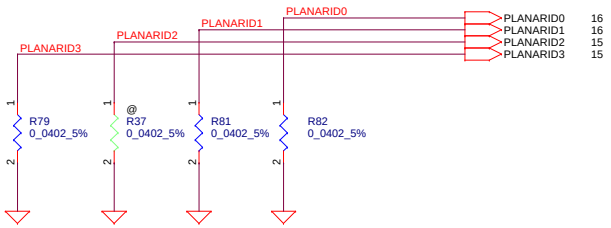
DDP[B:C]_CTRLCLK/DATA
PAYTON: NC
WALTER:
N16P QUADRO = NC
N16S GEFORCE = CONNECT FROM DISPLAYS



GPP_H23
PAYTON: NC
WALTER: -DGFX_WITH_DISPLAYOUT(INPUT)
N16P QUADRO = LOW
N16S GEFORCE = HIGH

TABLE

	PLANAR ID			
	3	2	1	0
	R79	R37	R81	R82
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM



TABLE

LEVEL	PLANARID[3..0]	CPU	PCH
4+2 SDV	0001b	ES ()	ES ()
4+2 FVT	0010b	ES ()	ES ()
4+2 SIT	0011b	QS ()	QS ()
4+2 SVT	0100b	QS ()	QS ()
4+2 SOVP	0101b	Prod	Prod
Reserved	1000b		
Reserved	1001b		
Reserved	1010b		
Reserved	1011b		

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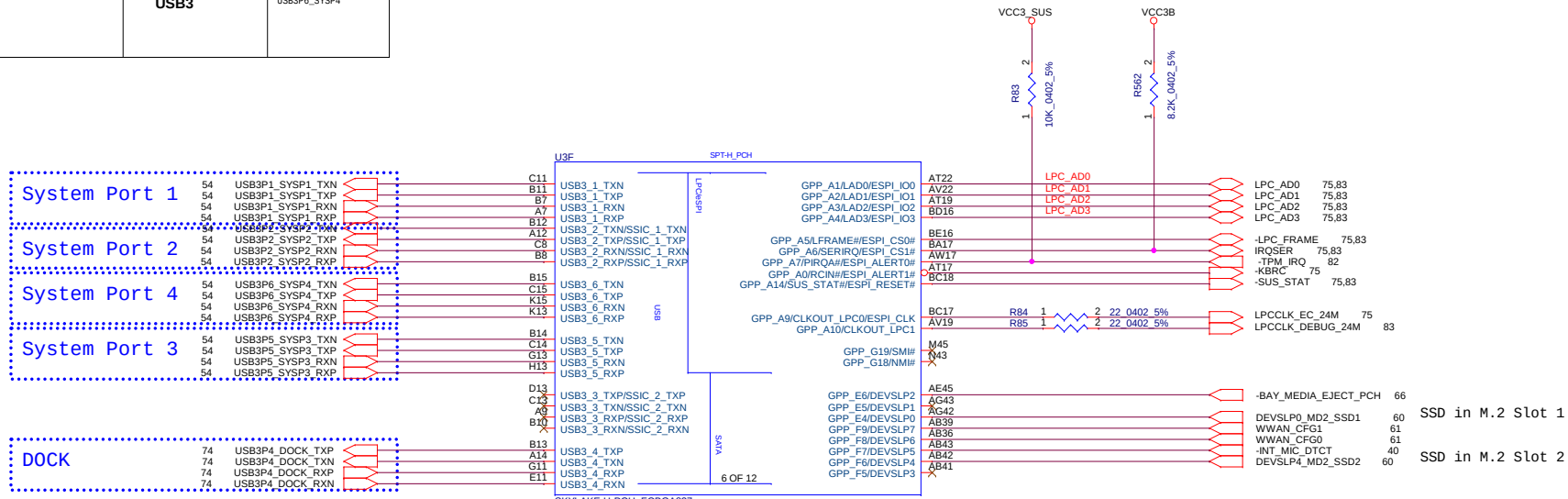
Title: *PCH SKL-H : DDI CONTROL*

LCFC

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 18 of 111

Flexible I/O Configuration (v0.51)			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1 Capable of OTG	USB3	USB3P1_SYSP1
Port 2	USB2 3 / SSIC 1	USB3	USB3P2_SYSP2
Port 3	USB3 3 / SSIC 2	USB3 or SSIC	USB3P3_WWAN
Port 4	USB3 4	USB3	USB3P4_DOCK
Port 5	USB3 5	USB3	USB3P5_SYSP3
Port 6	USB3 6	USB3	USB3P6_SYSP4



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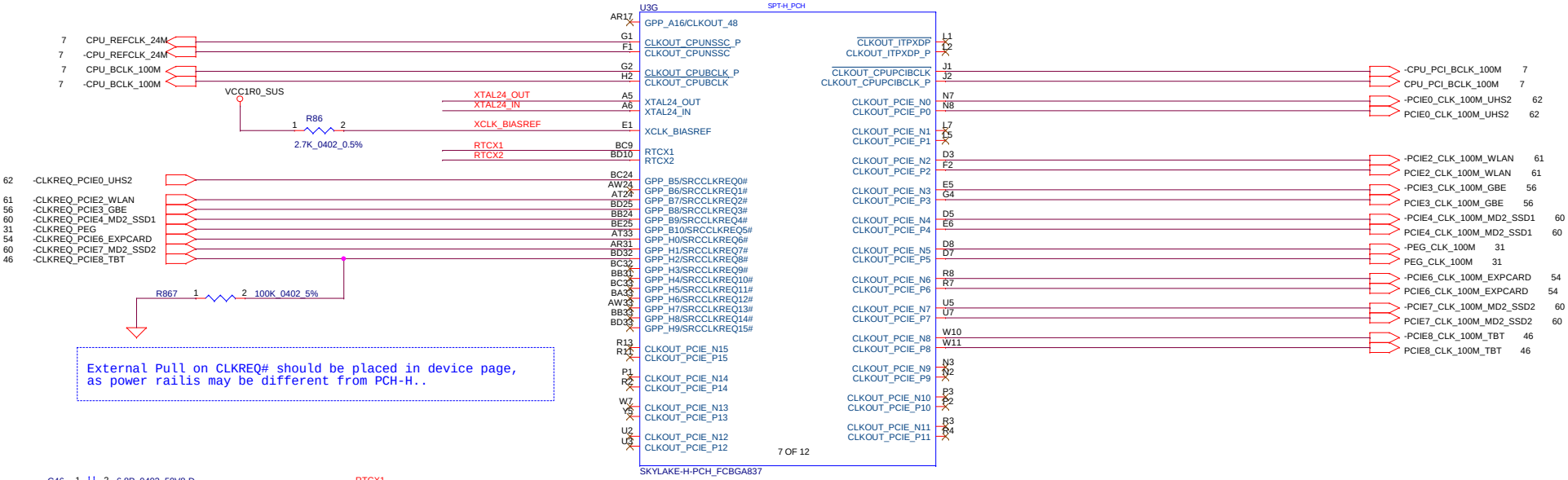
Title: **PCH SKL-H : USB3/LPC**

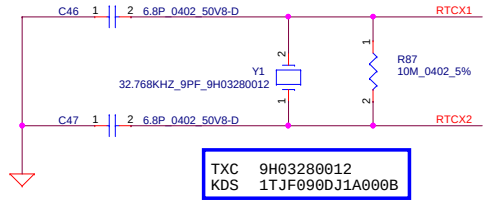
Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 19 of 111

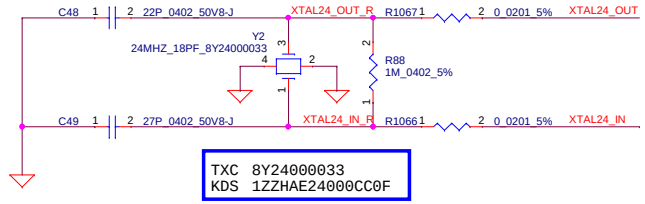
R86 Need change to 2.71K_0.5%



External Pull on CLKREQ# should be placed in device page, as power railis may be different from PCH-H..



TXC 9H03280012
KDS 1TJF090DJ1A000B



TXC 8Y24000033
KDS 1ZZHAE24000CC0F

PCIE Clock Assignment
Clock 0 : UHS II
Clock 1 : NA
Clock 2 : Wireless LAN M.2 Slot
Clock 3 : Giga Bit Ethernet
Clock 4 : PCIe SSD on M.2 Slot
Clock 5 : Discrete GFX(MXM or Onboard)
Clock 6 : Express Slot
Clock 7 : PCIe SSD on M.2 Slot
Clock 8 : Thunderbolt
Clock 9 - 15 : NA

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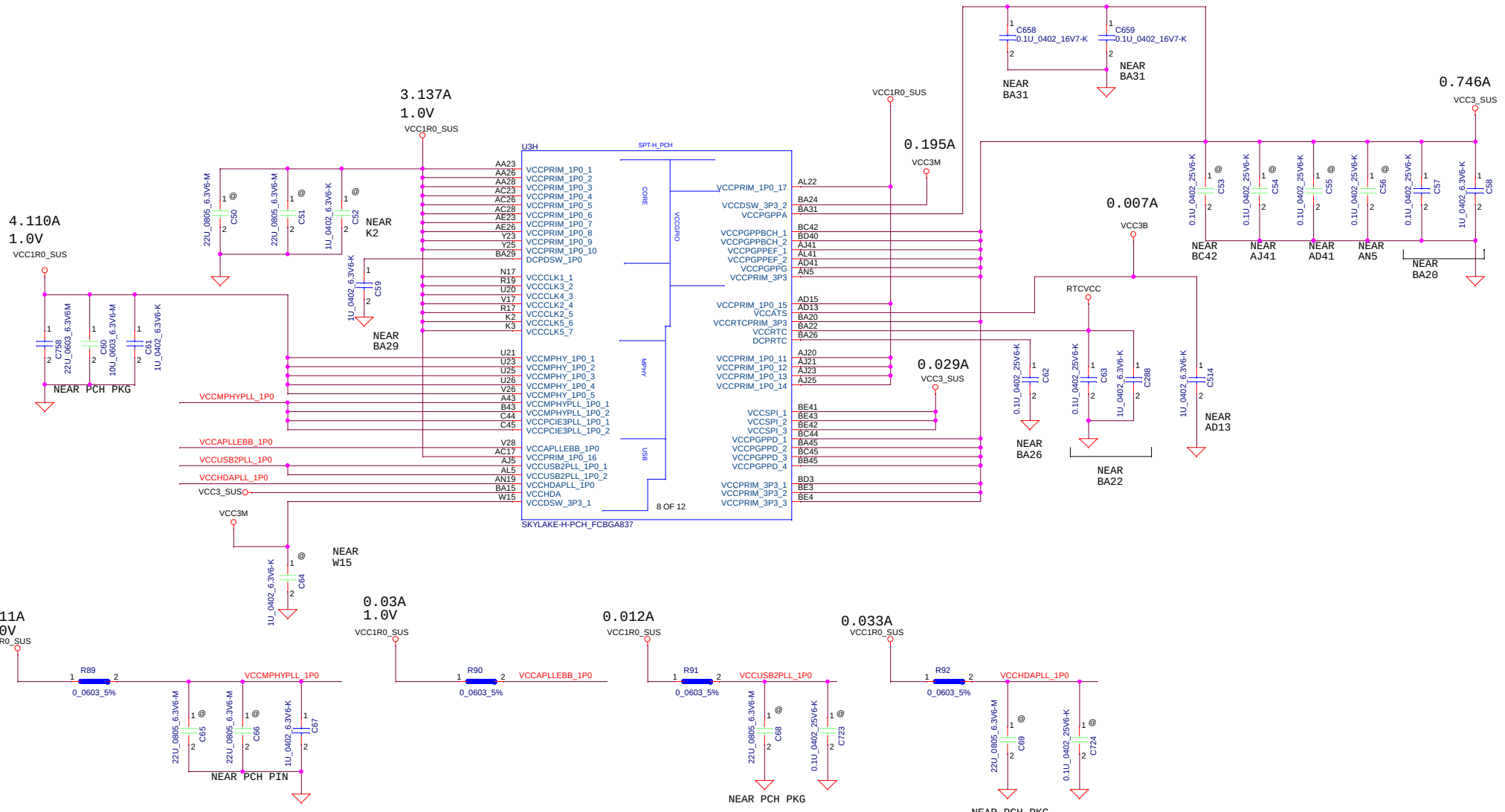
Title: PCH SKL-H : CLK

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 20 of 111



Note 1: Ampere in this page means Iccmax current described in SKL PCH H EDS r0.91 page 57.

Note 2: Decoupling capacitors refers SKL H PDG r0.71 page 526.
SKL H RVP11 schematics r0.7 also referred.

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Issued Date	2015/07/16	Deciphered Date	2016/01/16

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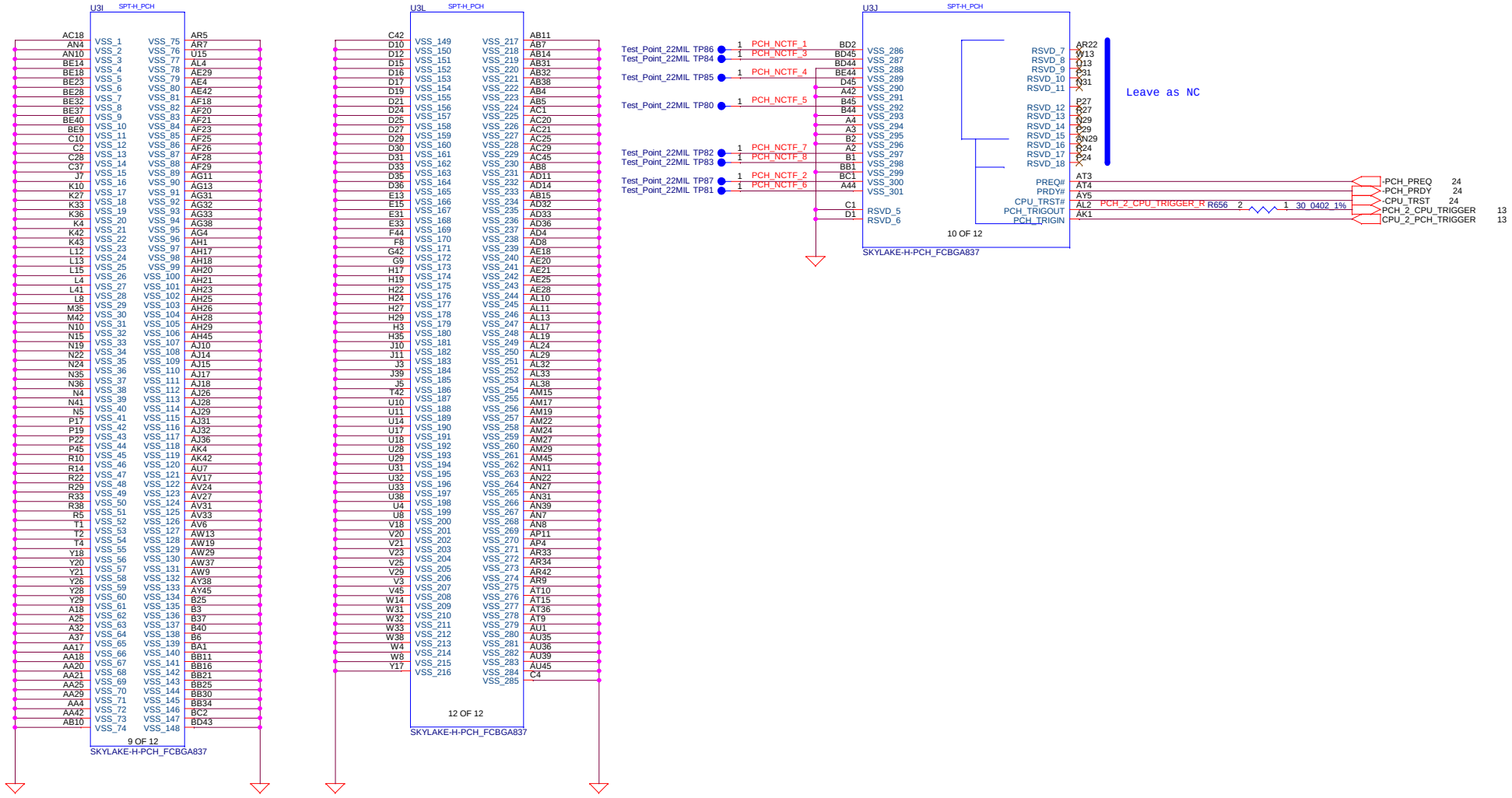
Title: **PCH SKL-H : POWER**

Size: Custom	Document Number: PAYTON	Rev: 0.1
Date: Wednesday, December 07, 2016	Sheet 21 of 111	



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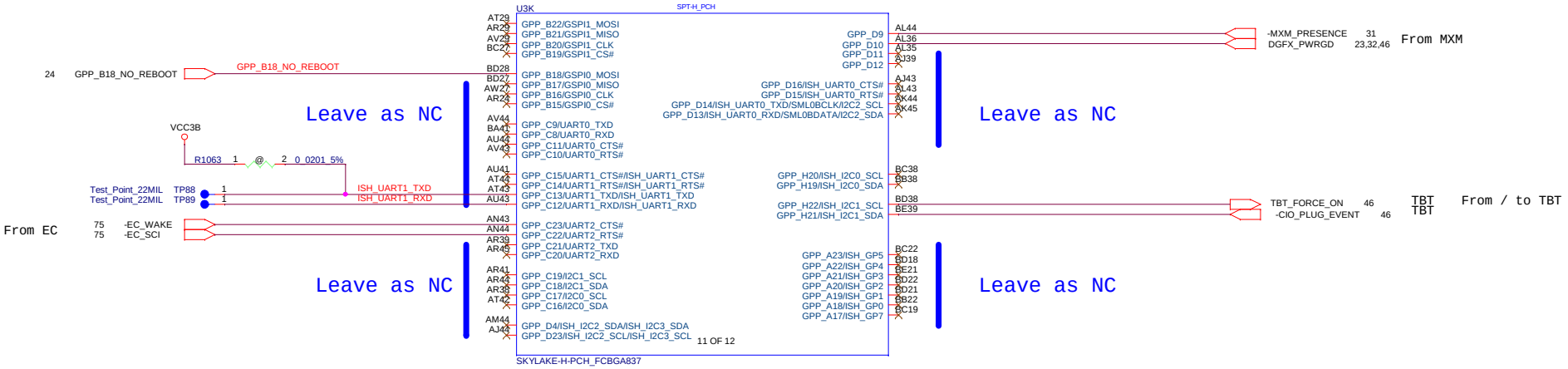
Title: *PCH SKL-H : GND/RSVD*

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 22 of 111

	PAYTON	WALTER
GPP_D9	-MXM_PRESENCE	-DISCRETE_PRESENCE



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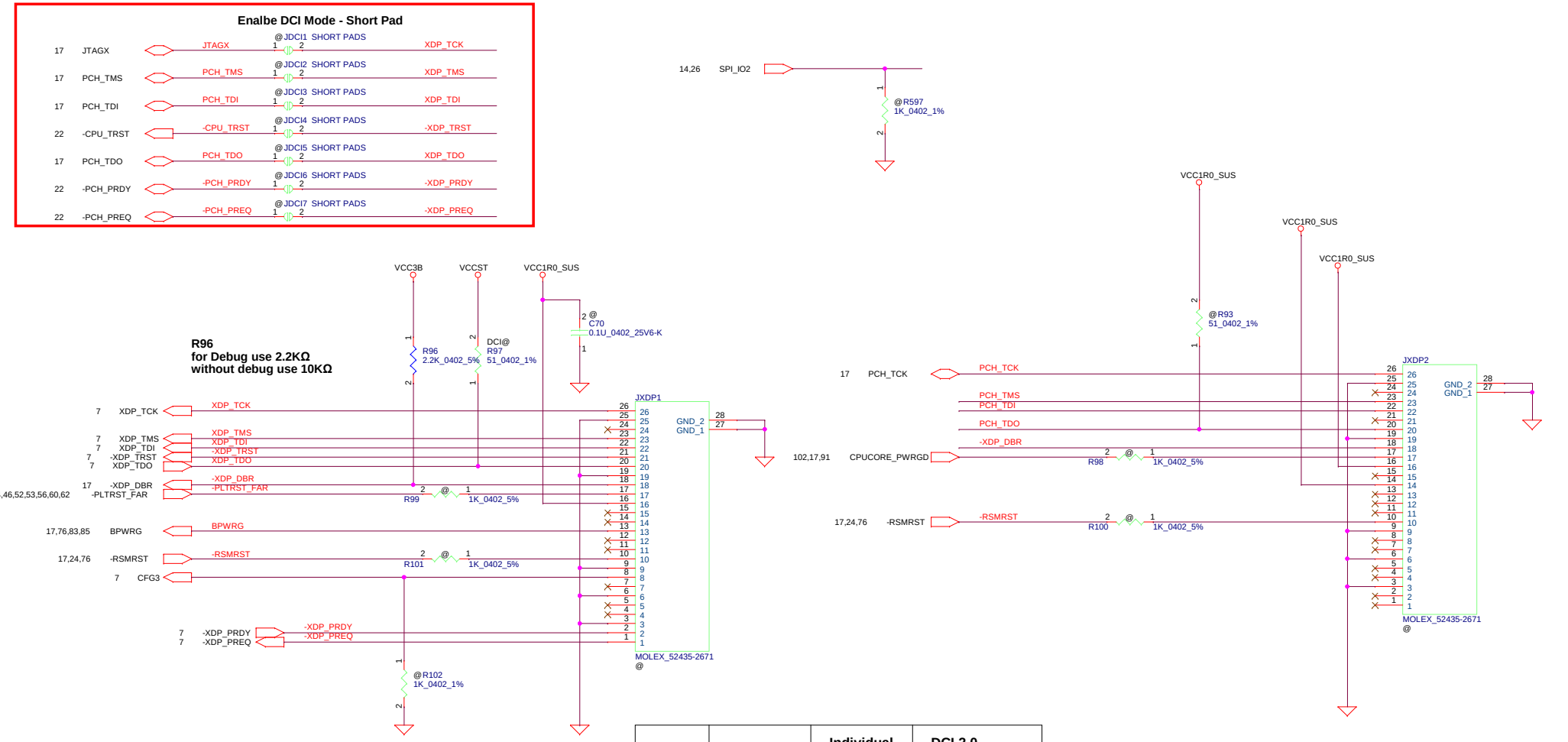
Title: **PCH SKL-H : GSPI/UART/I2C**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 23 of 111



	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R18	NO ASM	ASM	ASM
R297	NO ASM	ASM	NO ASM

SHEET 7

LOGIC

R820	NO ASM	ASM	NO ASM
R821	NO ASM	ASM	NO ASM
R822	NO ASM	ASM	NO ASM

SHEET 17

	No use	Individual Port	DCI 2.0 w/o connector
R97	NO ASM	ASM	ASM
J1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	ASM	ASM	ASM
R101	NO ASM	ASM	NO ASM
R93	NO ASM	ASM	NO ASM
J2	NO ASM	ASM	NO ASM
R98	NO ASM	ASM	NO ASM
R100	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC

VCC3_SUS
@R563 1K_0402_5%
Place near PCH
GPP_B18_NO_REBOOT
GPP_B18_NO_REBOOT 23

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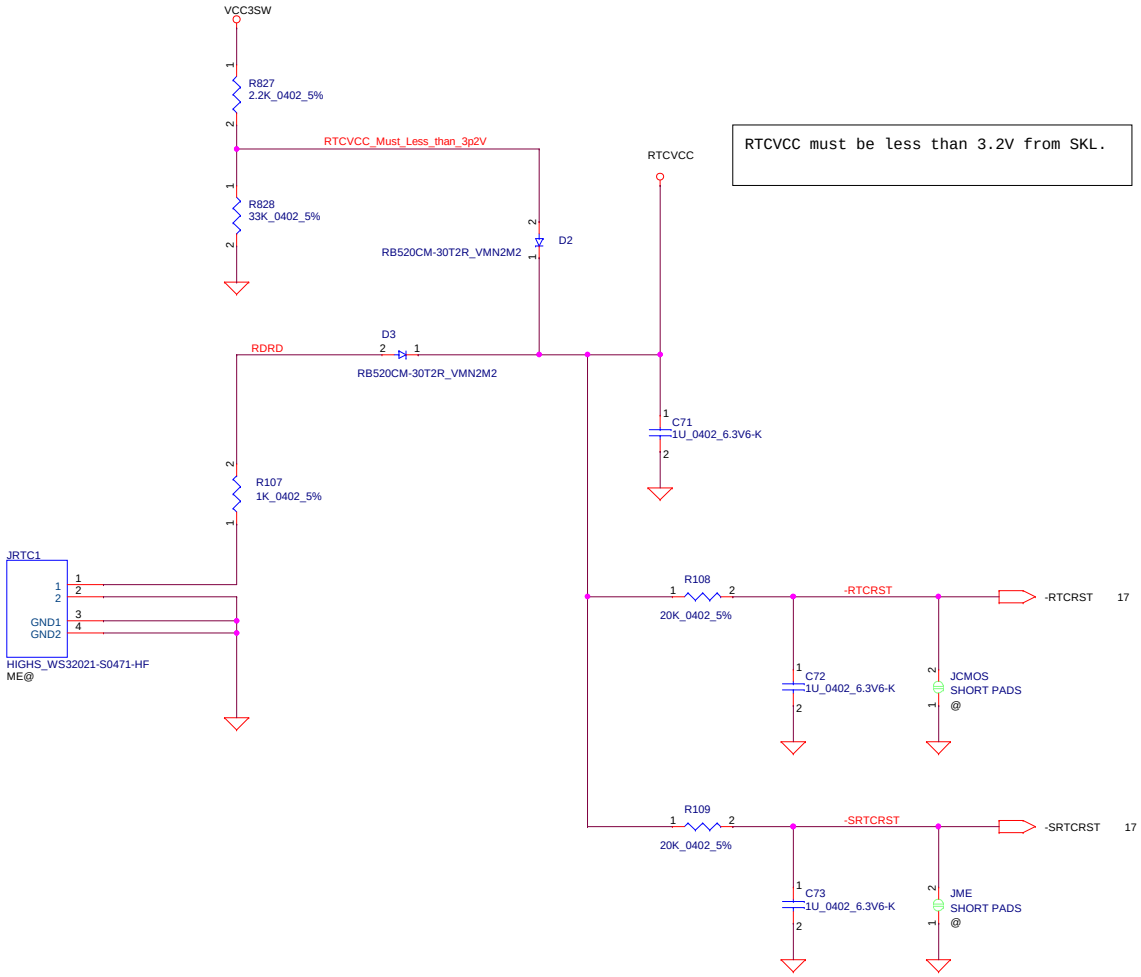
Title: **XDP CONNECTOR**

Size	Document Number	Rev
Custom	PAYTON	0.1

Date: Wednesday, December 07, 2016 Sheet 24 of 111



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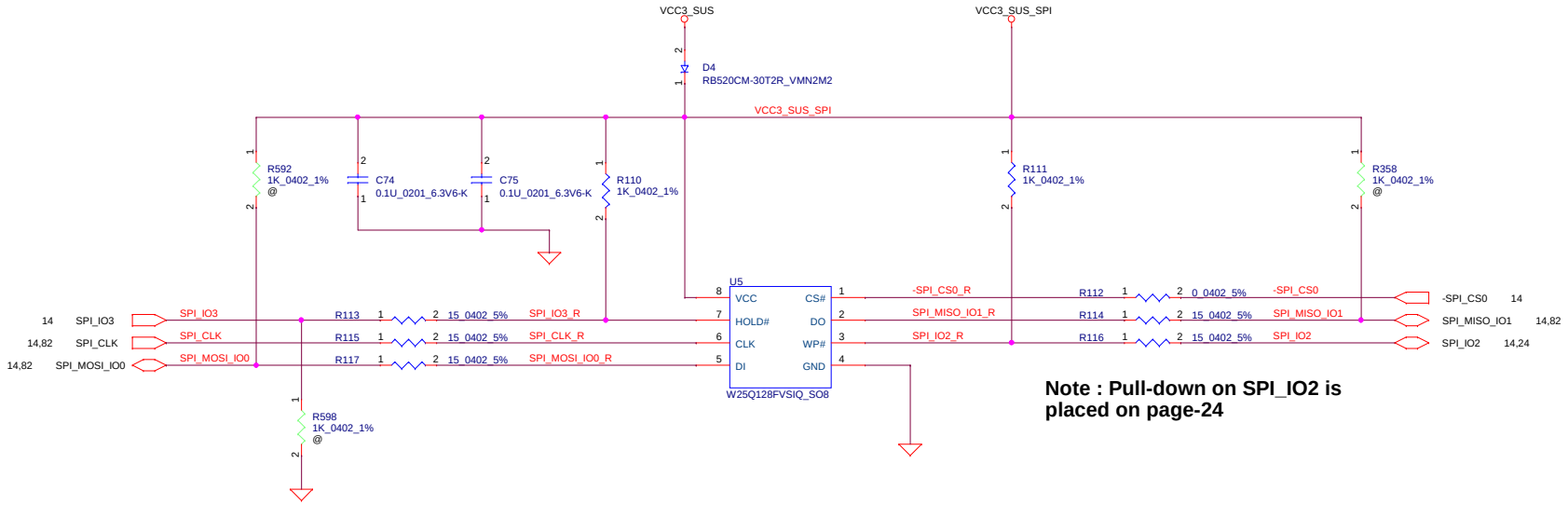
Title: **RTC BATTERY**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 25 of 111

	R110	R598	U5	R592	R358
PRE ES1 ES1/ ES2	NO ASM	ASM	QE="1"	ASM	ASM
AFTER QS	ASM	NO ASM	QE=Don't Care	NO ASM	NO ASM

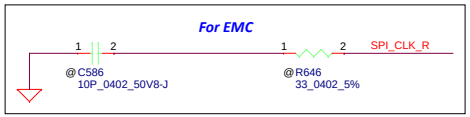
← LOGIC



Note : Pull-down on SPI_IO2 is placed on page-24

TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)					
1	VCC	D12.1	GND	GND	2
3	CS#	R322.2	R681.2	CLK	4
5	MISO	R694.2	R674.2	MOSI	6
7	(KEY)	N/A	N/A	(RESET)	8



U5 SPI ROM

vPRO model(16MB)	
WINBOND	W25Q128FVSIQ
MACRONIX	MX25L12873FM2I-10G
MICRON	N25Q128A13ESEDFF

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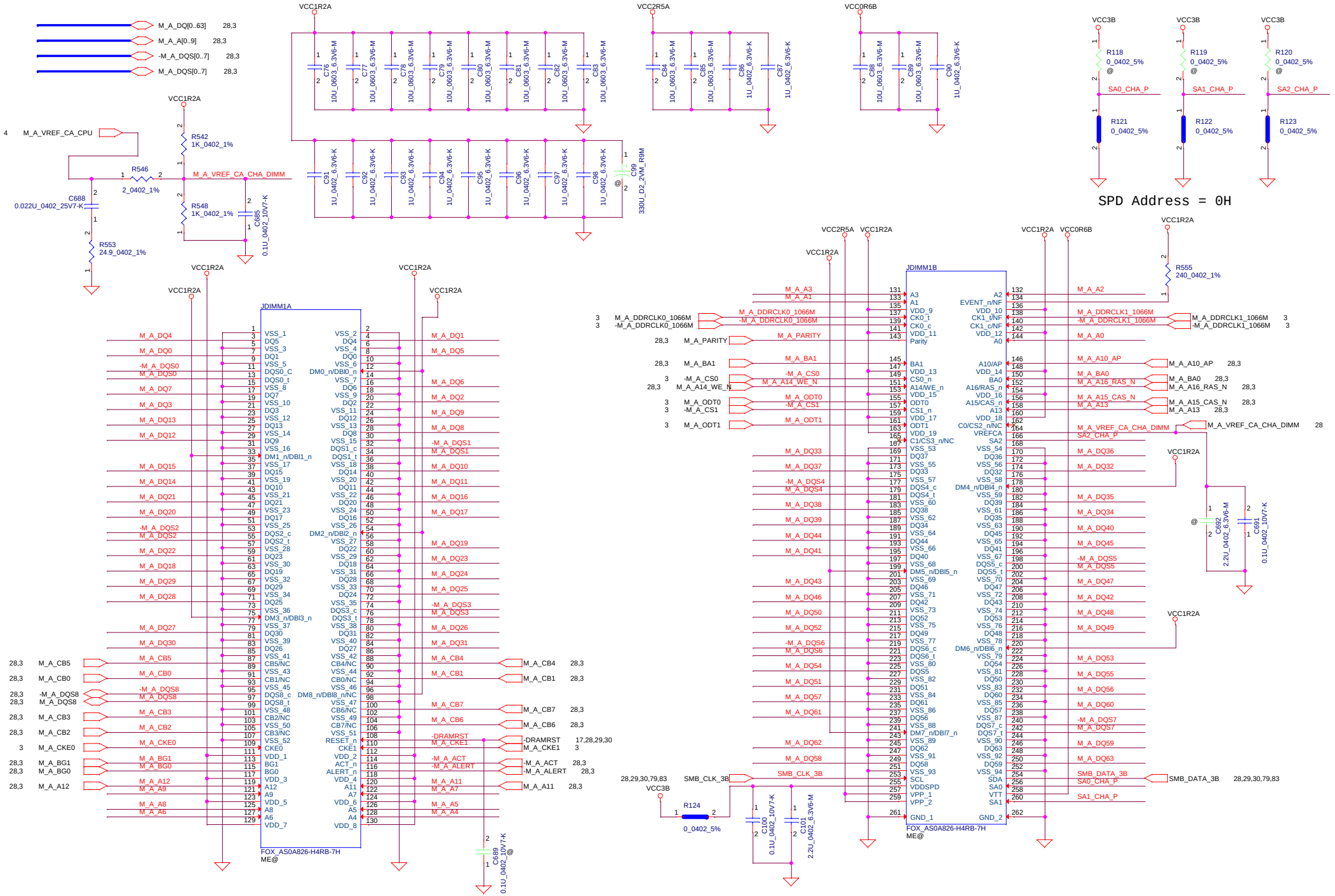
Title: **SPI FLASH**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 26 of 111



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Title: **DDR4 CH-A PRIMARY**

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Size	Document Number	Rev
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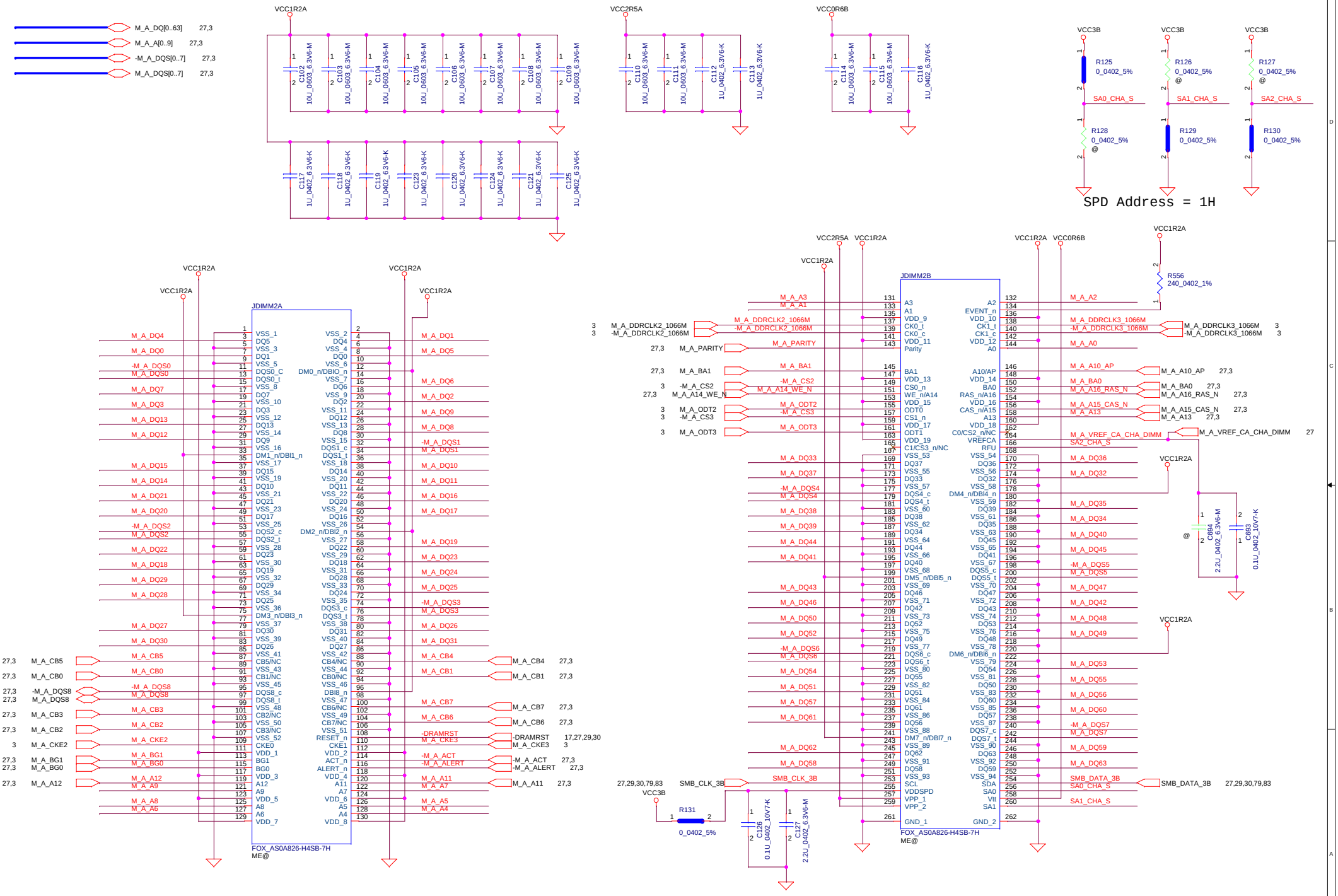
Date: Wednesday, December 07, 2016 Sheet 27 of 111



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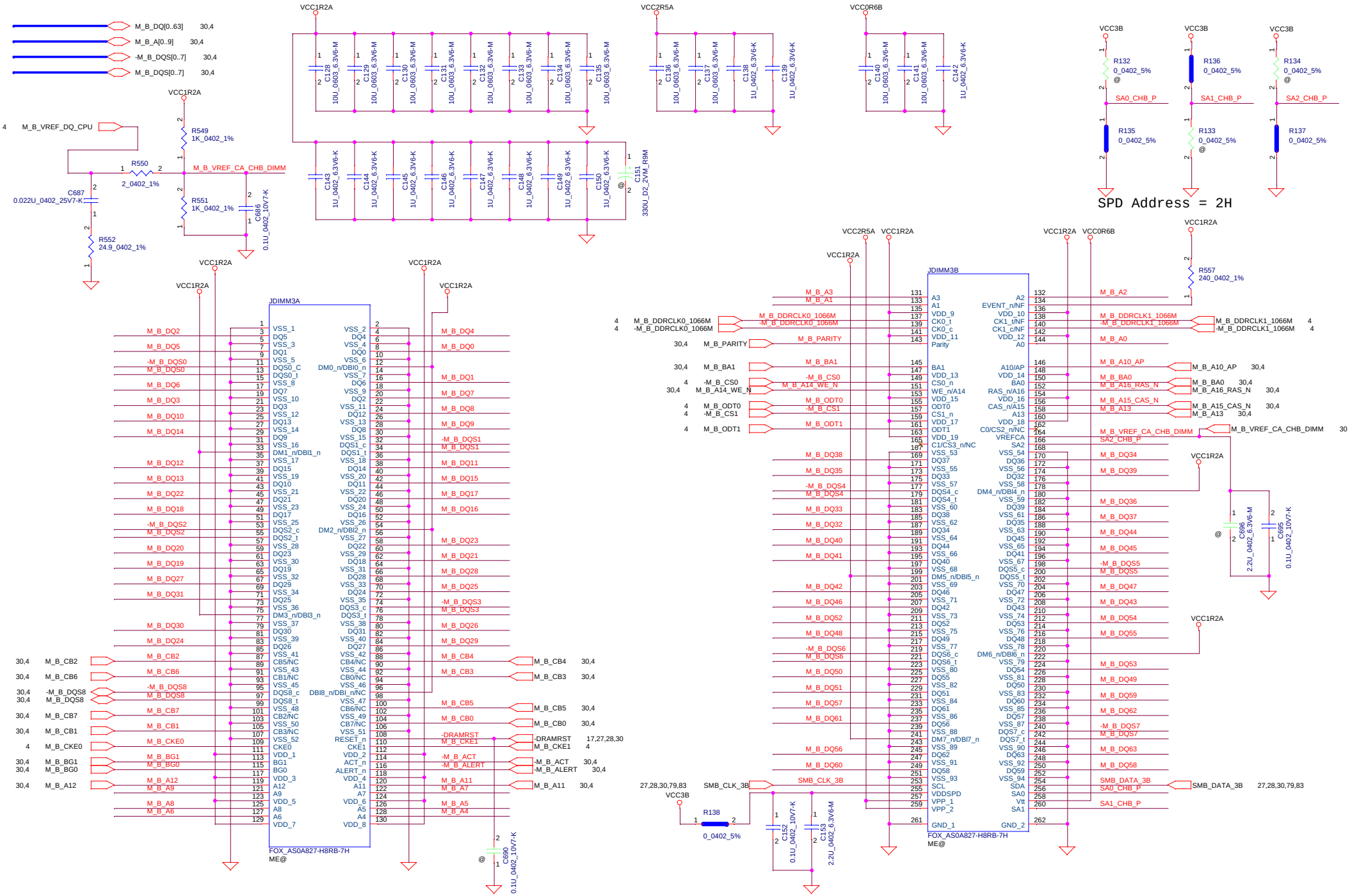
Title: **DDR4 CH-A SECONDARY**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 28 of 111



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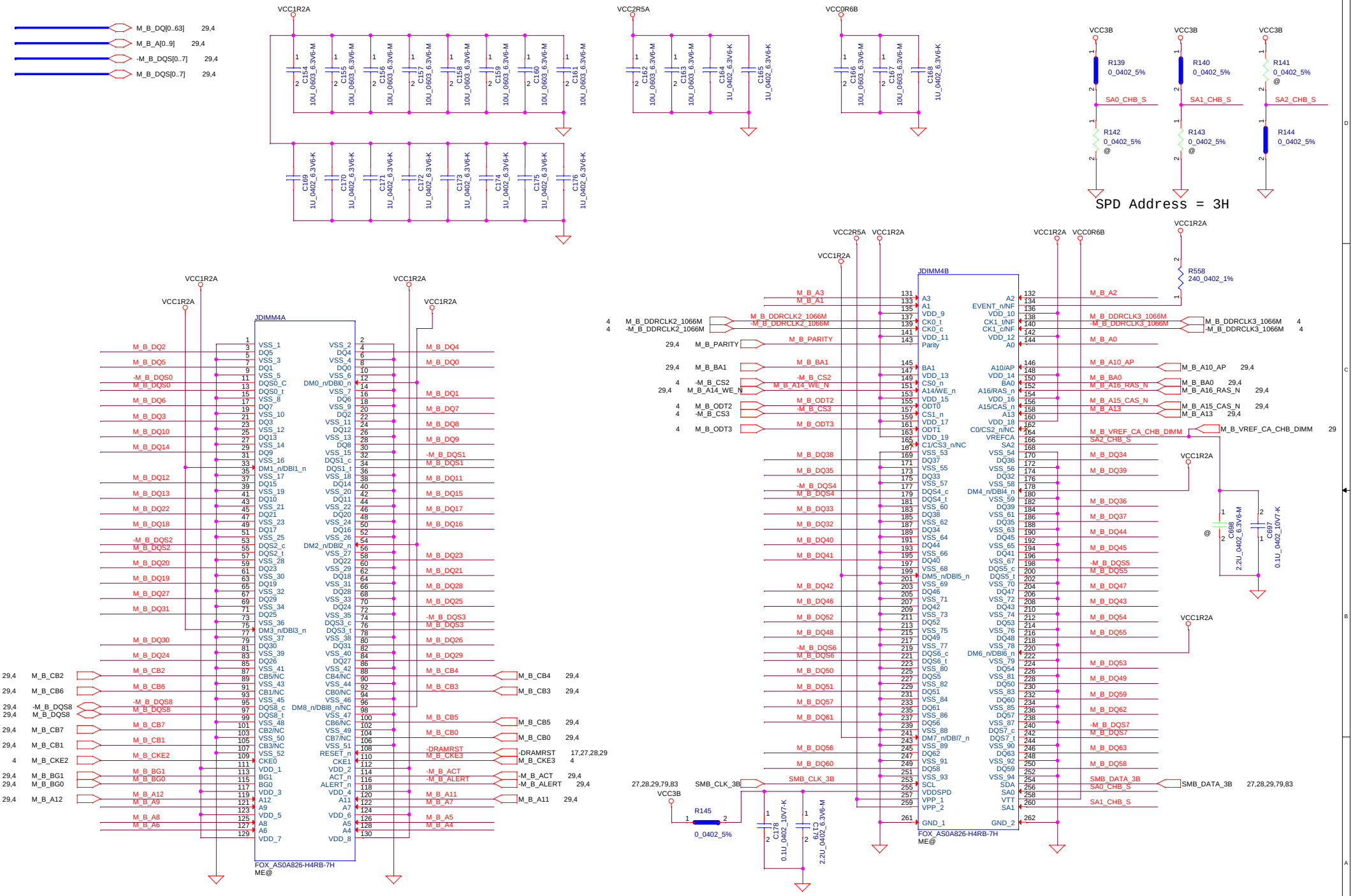
Title: **DDR4 CH-B PRIMARY**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 29 of 111


M_B_DQ[0..63] 29,4
M_B_A[0..9] 29,4
-M_B_DQS[0..7] 29,4
M_B_DQS[0..7] 29,4
VCC1R2A
VCC2R5A
VCC0R6B
VCC3B
SPD Address = 3H
JDIMM4A
JDIMM4B
FOX_AS0A826-H4RB-7H
ME@
SMB_CLK_3B
SMB_DATA_3B
SA0_CHB_S
SA1_CHB_S
SA2_CHB_S
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LCFC
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Custom
Document Number
Rev
0.1
Date:
Wednesday, December 07, 2016
Sheet
30
of
111

PEX_STD_SW# PD	NO_ASM	147K	7.15K	0
8GT/s TXEQ Preset	P1,P3,P5	P1,P3,P5	P1,P7,P8	P7,P8
Channel Class	Short	Mid Short	Mid Long	Long

See MXM spec v3.1 for detail.

For UART RX DEBUG
IOR-B change FL8, FL9 to 0Ω
@R315 and R317 Mount JTX and JRX

3.3V +/-6%
MAX 1.0A

5.0V +/-6%
MAX 2.5A

7-20V
MAX 10A

PLACE CAPS NEAR MXM CONN

PLACE CAPS NEAR MXM CONN

Leave as NC

MXM CONN
TOP VIEW

MXM INSERT DIRECTION

MXM Planar

PLACE CAPS NEAR MXM CONN (within 0.5")
MXM Spec requires both TX and RX caps near MXM on planar

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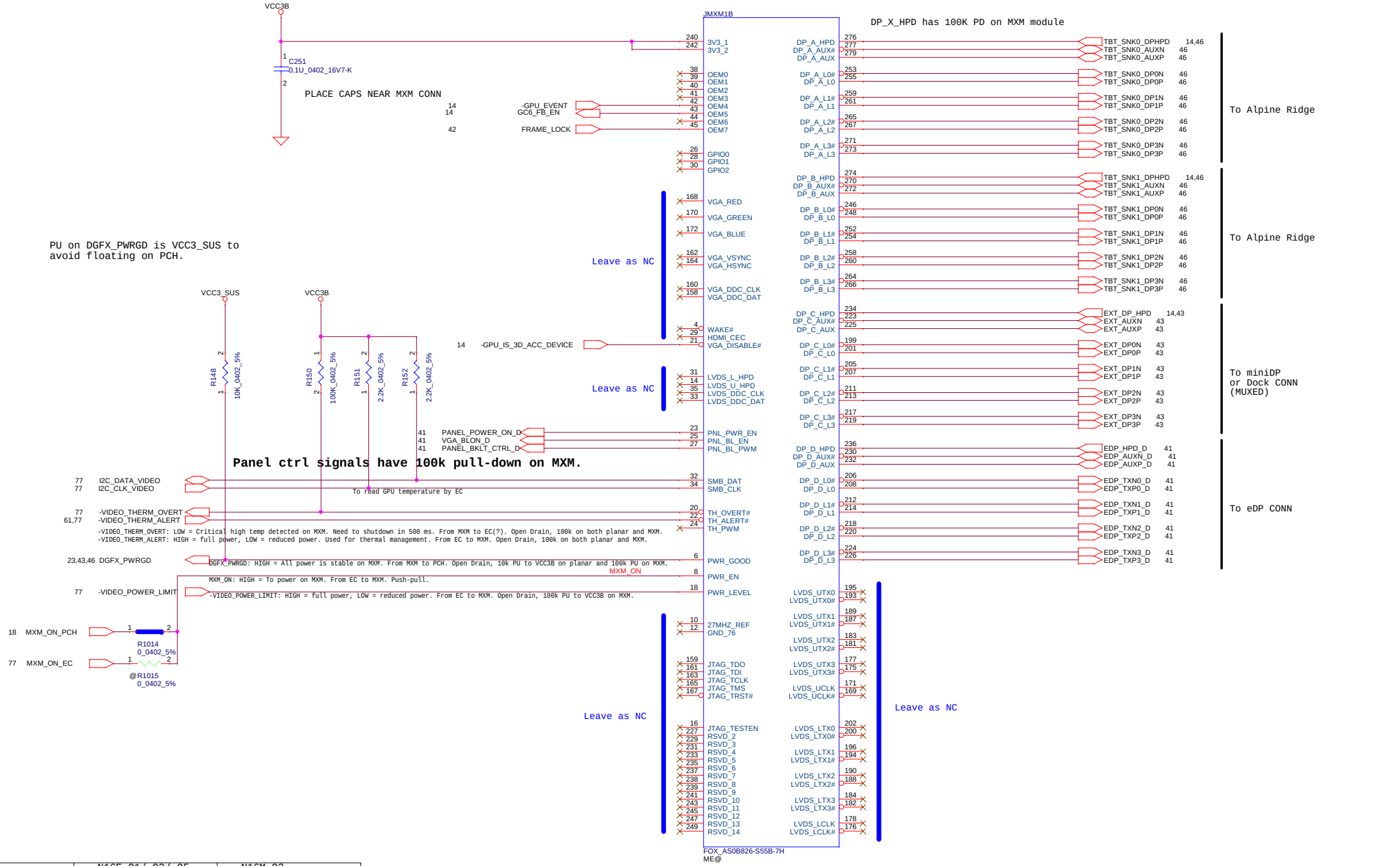
Title: MXM (1/2)

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 31 of 111



MXM OEM /GPIO PIN3	N16E-Q1/-Q3/-Q5		N16M-Q2	
	Signal Name	I/O Tpye	Signal Name	I/O Tpye
OEM4	GPU_EVENT#	Bi-Dir	GPU_EVENT#	Bi-Dir
OEM5	GC6_FB_EN	IN	GC6_FB_EN	IN
OEM6	GPIO19_STEREO	OUT	GPIO7_STEREO	OUT
OEM7	FRAMELOCK	IN	FRAMELOCK#	IN
GPIO0	GPIO26	Tri-state	NC(Default)	NC
GPIO1	NC	NC	GPIO1	Tri-state
GPIO2	GPIO25	Tri-state	NC(Default)	NC

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Title: *MXM (2/2)*

Size	Document Number	Rev
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Date: Wednesday, December 07, 2016 Sheet 32 of 111

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Date: Wednesday, December 07, 2016	Sheet 33 of 111	

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Title
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Date: Wednesday, December 07, 2016	Sheet 36 of 111	

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Title: *BLANK*

LCFC

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LCFC

Size	Document Number	Rev
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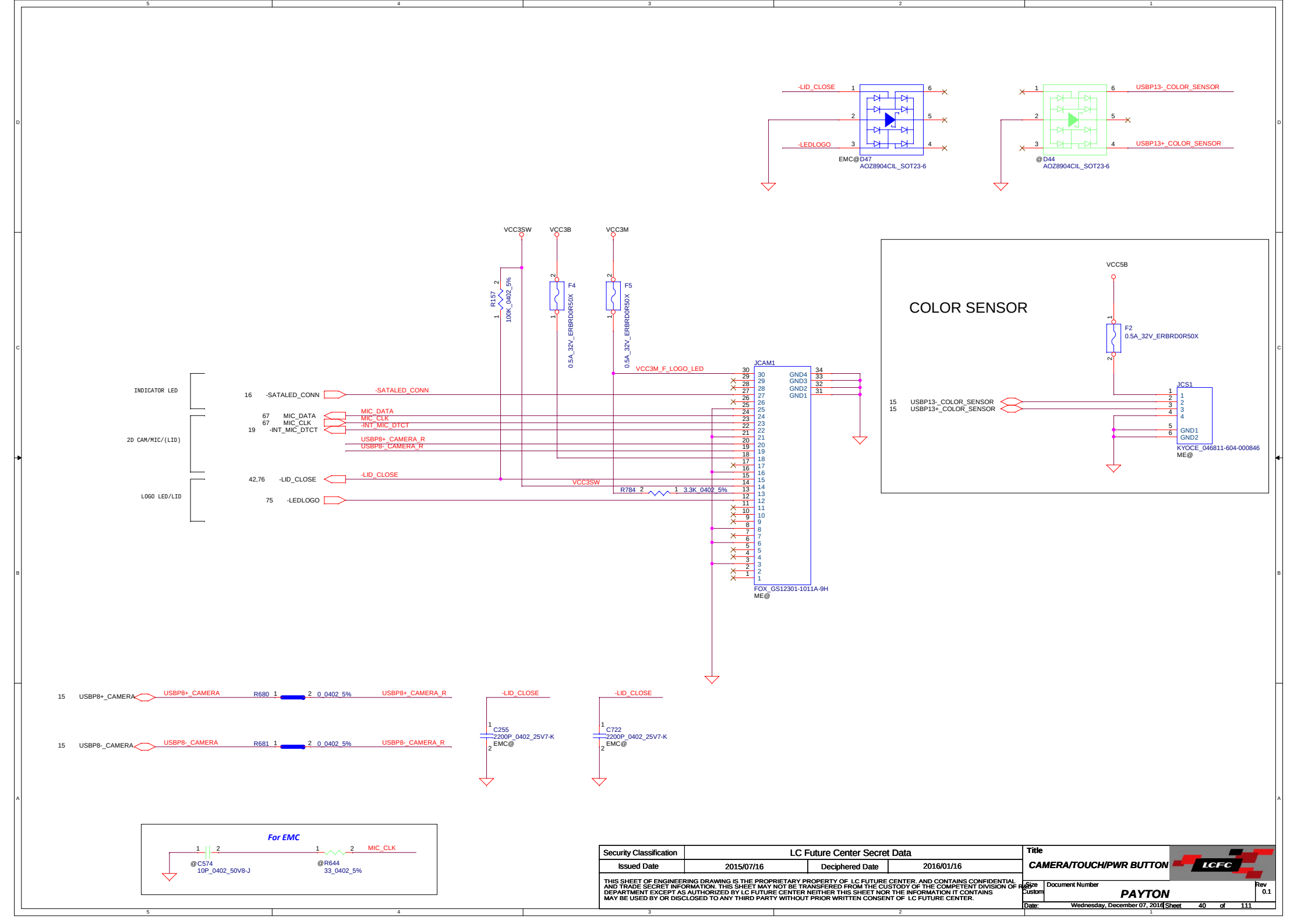
Date: Wednesday, December 07, 2016 Sheet 39 of 111



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Title: CAMERA/TOUCH/PWR BUTTON

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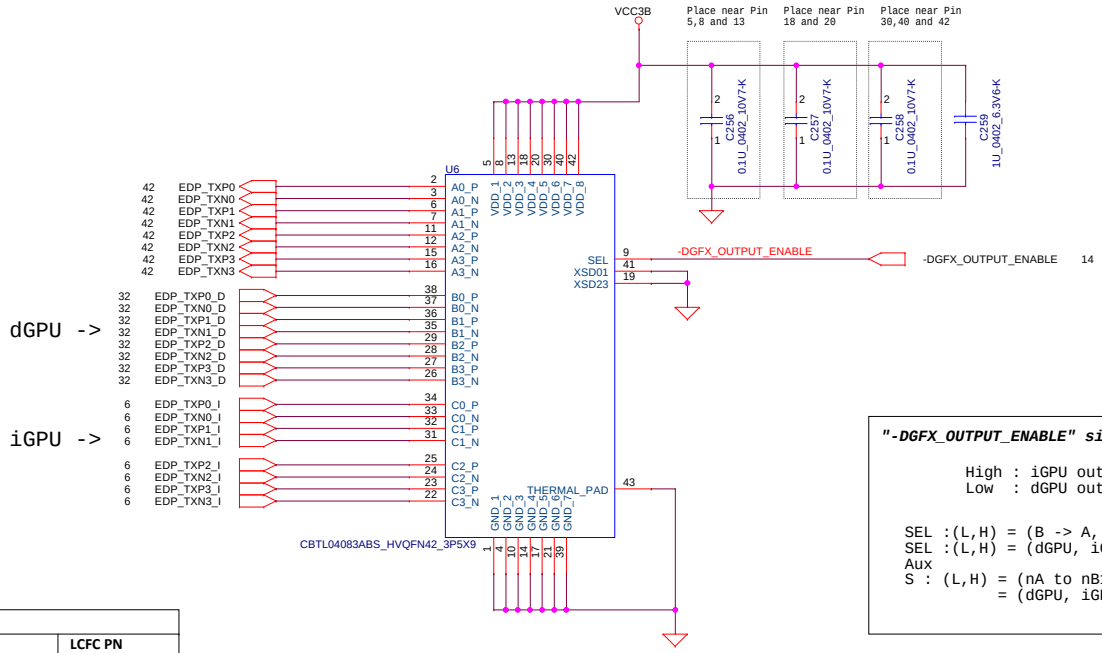
Date: Wednesday, December 07, 2016 | Sheet 40 of 111



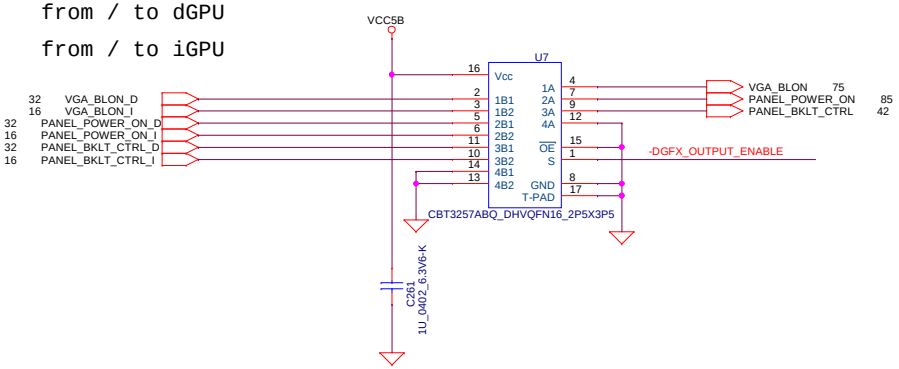
"-DGFX_OUTPUT_ENABLE" signal controls DOCK DP Bus switch

High : iGPU output is selected.
Low : dGPU output is selected.

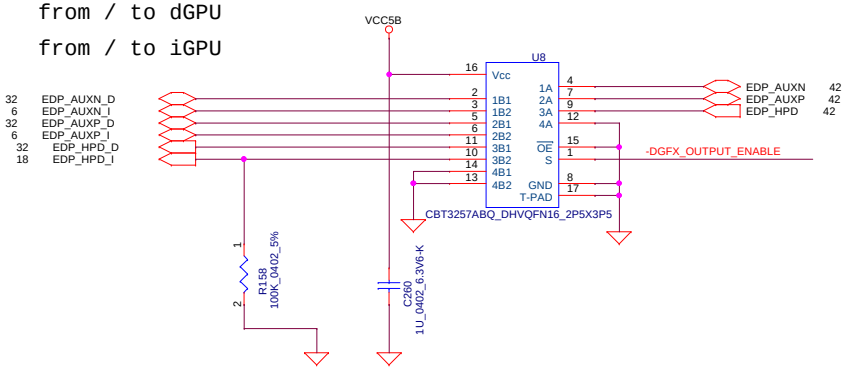
SEL :(L,H) = (B -> A, C ->A)
SEL :(L,H) = (dGPU, iGPU)
Aux
S : (L,H) = (nA to nB1, nA to nB2)
= (dGPU, iGPU)

DOCK DP Switch		
Vendor	Vendor PN	LCFC PN
NXP	CBTL04083ABS	
Pericom	PI3PCIE3412ZHE+DAX	

from / to dGPU
from / to iGPU



from / to dGPU
from / to iGPU



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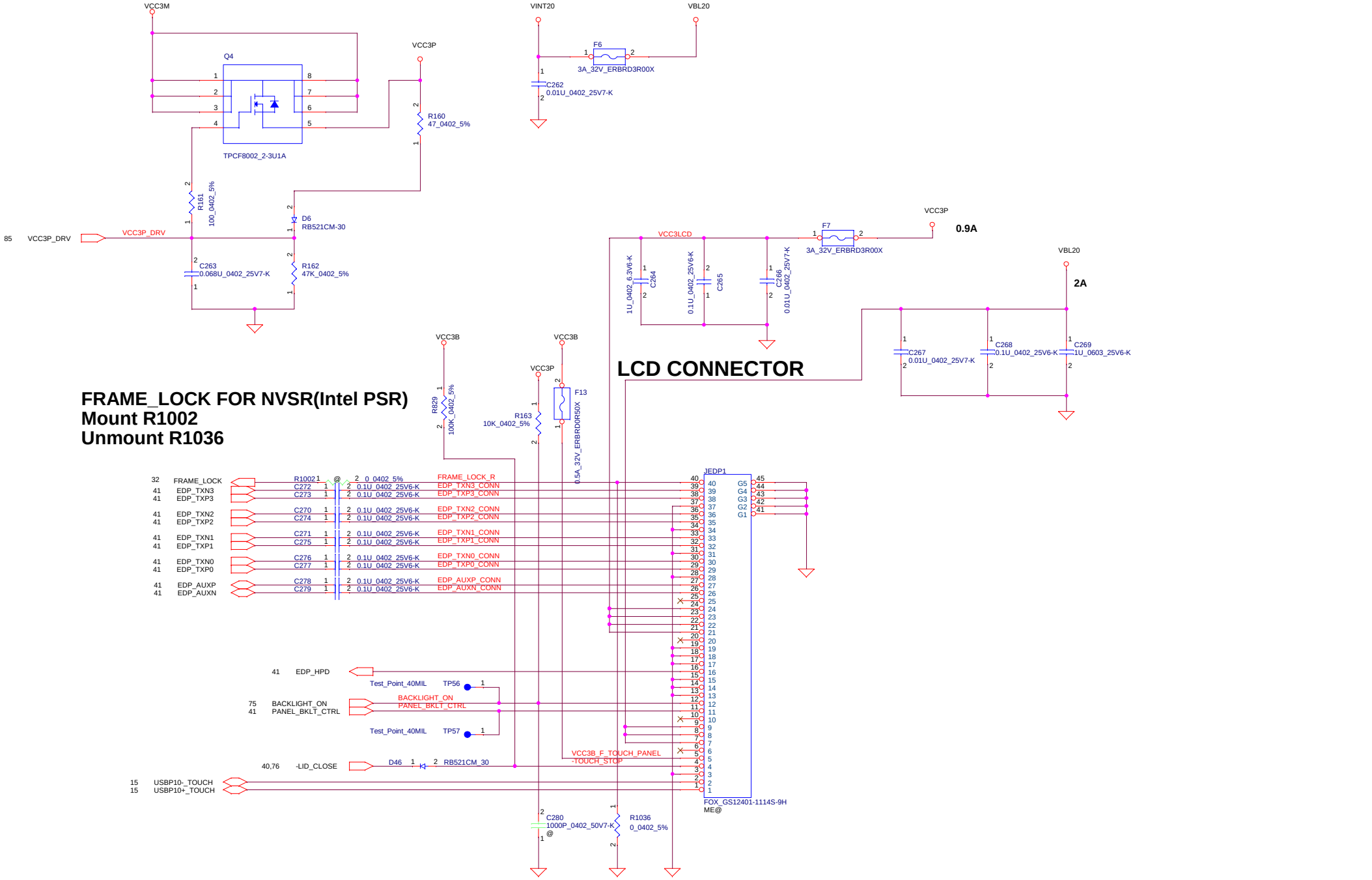
Title: eDP DEMUX

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 41 of 111



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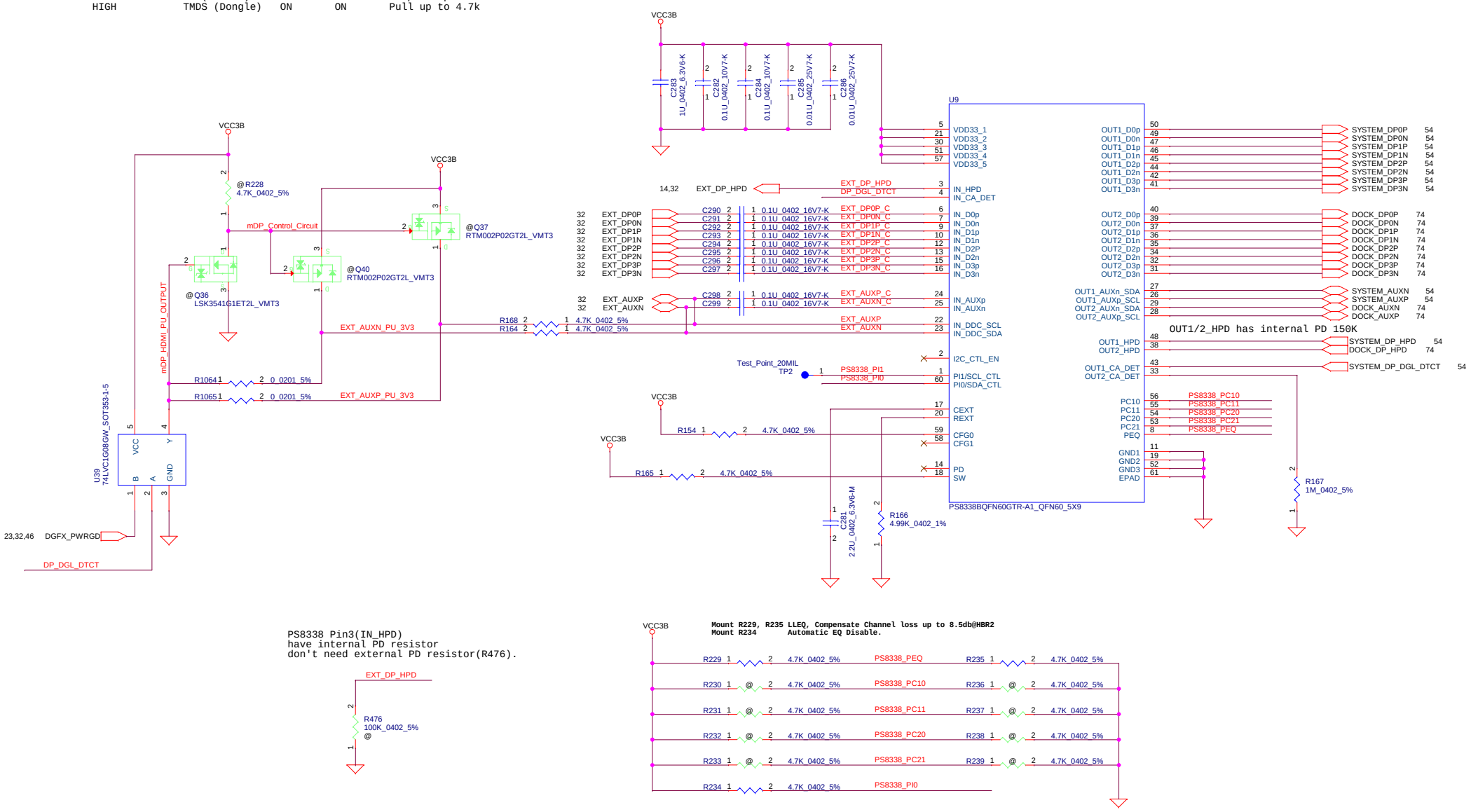
Title: LCD CONNECTOR

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 42 of 111

Circuit to turn on/off pull up resistors on AUXP/AUXN to support DP dongles.

DP_DGL_DTCT	DP MODE	2SK3541	RTM002	AUXP/N
LOW	DP (Native)	OFF	OFF	No pull-up
HIGH	TMDS (Dongle)	ON	ON	Pull up to 4.7k



PS8338 Pin3(IN_HPD)
have internal PD resistor
don't need external PD resistor(R476).

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Title: DP DEMUX

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 43 of 111

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

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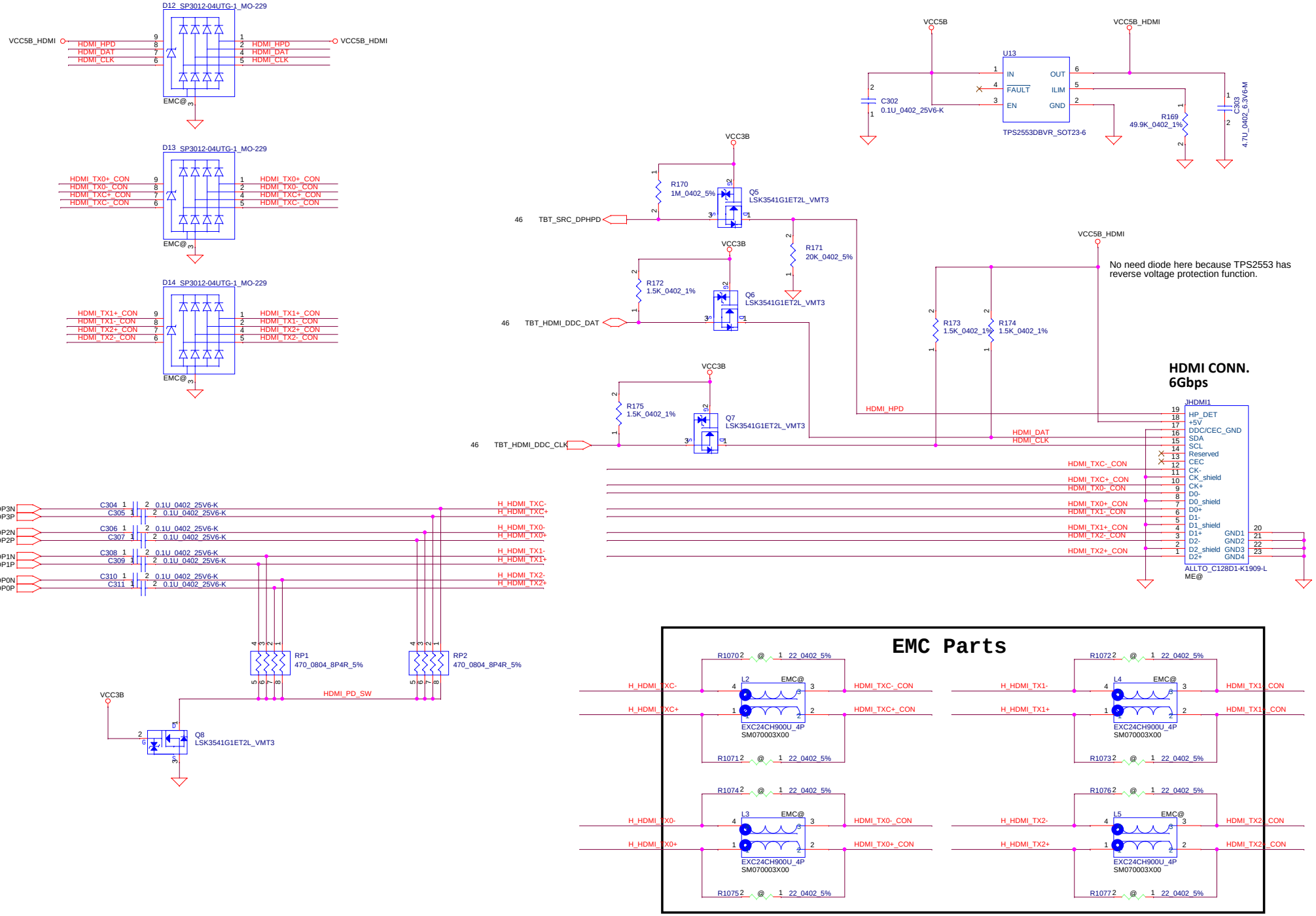
Title

DISPLAY PORT CONNECTOR

Size: Custom	Document Number: PAYTON	Rev: 0.1
Date: Wednesday, December 07, 2016	Sheet 44 of 111	



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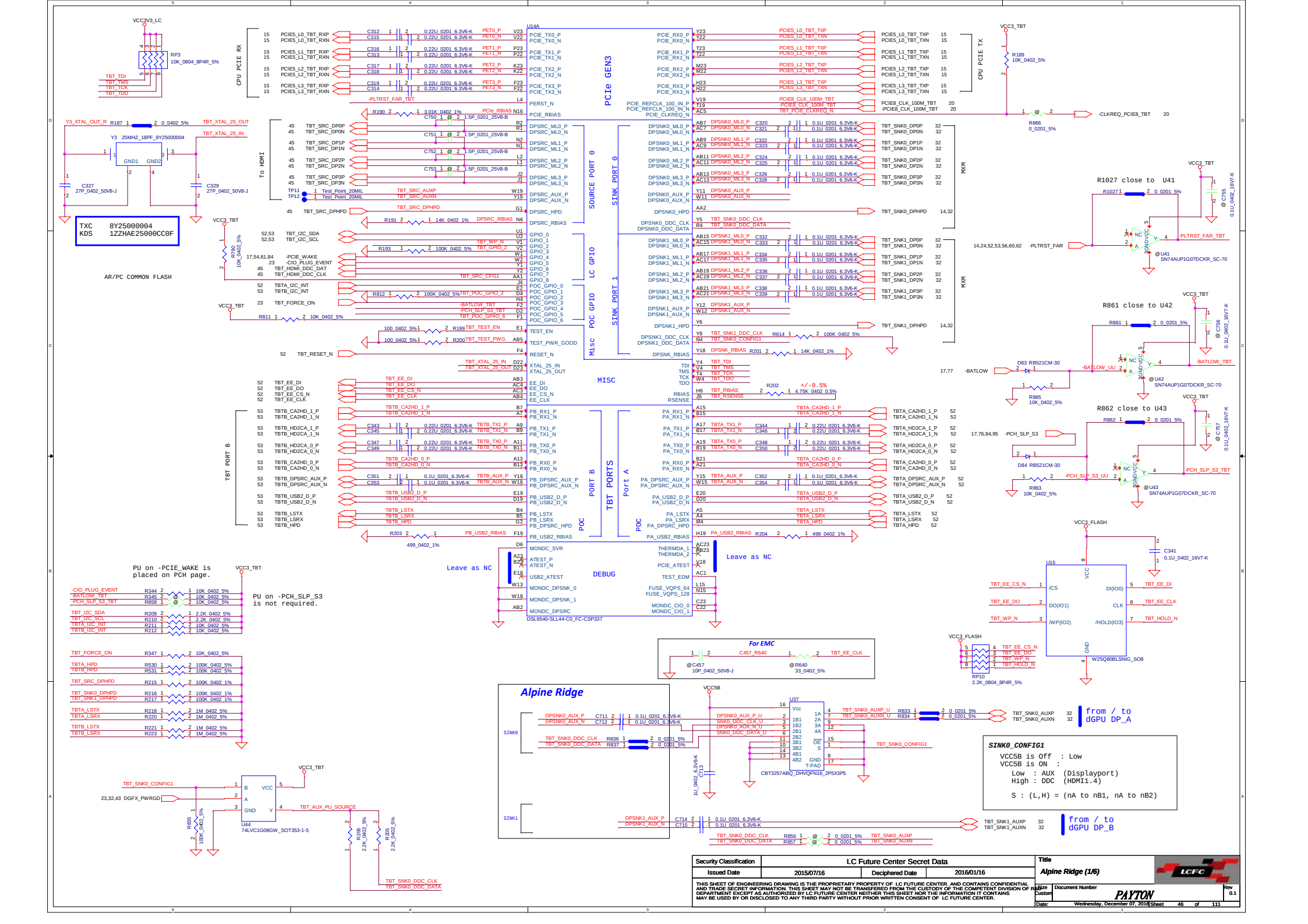
Title: **HDMI CONNECTOR**

LCFC

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 45 of 111



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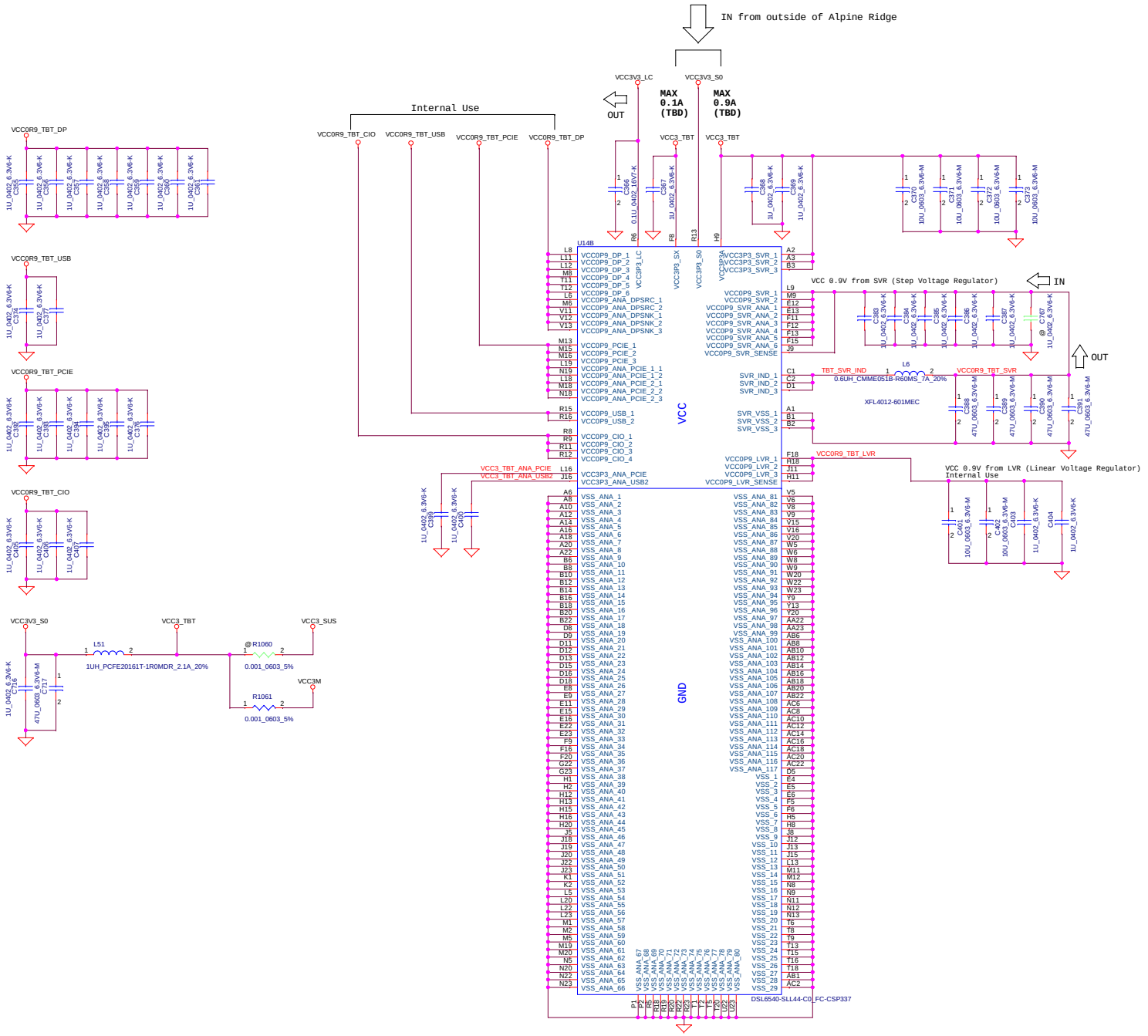
Title: *Alpine Ridge (1/6)*

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 46 of 111



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Title: *Alpine Ridge (2/6)*

Size	Document Number	Rev
Custom	PAYTON	0.1
Date: Wednesday, December 07, 2016	Sheet 47 of 111	

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Title

Alpine Ridge (3/6)

Size	Document Number	Rev
Custom	***PAYTON***	0.1

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Title

Alpine Ridge (4/6)

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Date: Wednesday, December 07, 2016	Sheet 49 of 111	

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Title
Alpine Ridge (5/6)

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Date: Wednesday, December 07, 2016	Sheet 50 of 111	

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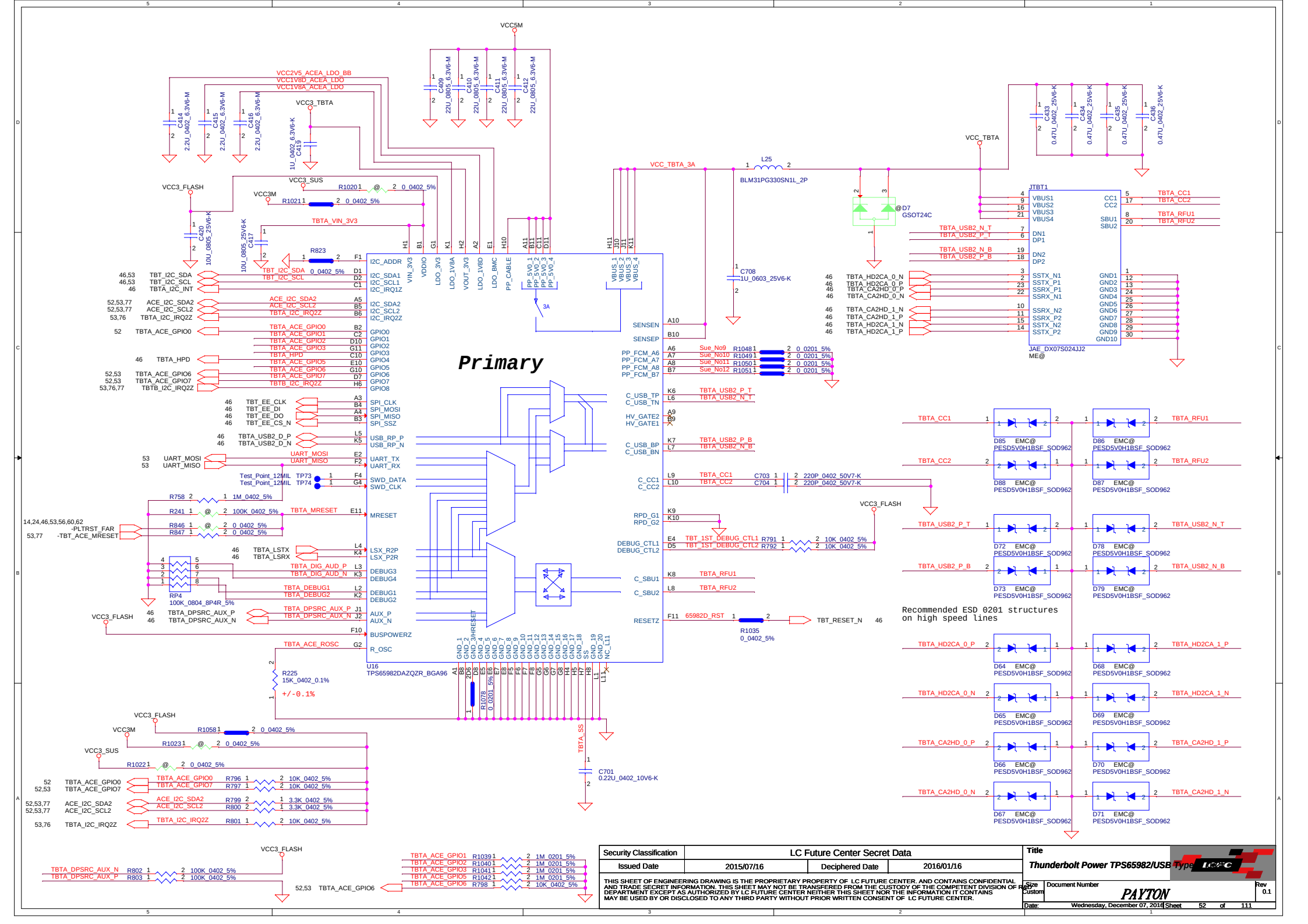
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U16
TPS65982DAZQZR_BGA96
JTBT1
JAE_DX07S024JJ2
ME@
VCC5M
VCC_TBTA
VCC_TBTA_3A
VCC3_TBTA
VCC3_FLASH
VCC3_SUS
VCC3M
L25
BLM31PG330SN1L_2P
@D7
GSOT24C
C708
1U_0603_25V6-K
R823
TBTA_VIN_3V3
TBT_I2C_SDA
TBT_I2C_SCL
TBTA_I2C_INT
ACE_I2C_SDA2
ACE_I2C_SCL2
TBTA_I2C_IRQ2Z
TBTB_I2C_IRQ2Z
TBTA_ACE_GPIO0
TBTA_ACE_GPIO1
TBTA_ACE_GPIO2
TBTA_ACE_GPIO3
TBTA_HPD
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TBTA_ACE_GPIO6
TBTA_ACE_GPIO7
TBT_EE_CLK
TBT_EE_DI
TBT_EE_DO
TBT_EE_CS_N
TBTA_USB2_D_P
TBTA_USB2_D_N
UART_MOSI
UART_MISO
Test_Point_12MIL
SWD_DATA
SWD_CLK
TBTA_MRESET
-PLTRST_FAR
-TBT_ACE_MRESET
TBTA_LSTX
TBTA_LSRX
TBTA_DIG_AUD_P
TBTA_DIG_AUD_N
TBTA_DEBUG1
TBTA_DEBUG2
RP4
100K_0804_8P4R_5%
TBTA_DPSRC_AUX_P
TBTA_DPSRC_AUX_N
TBTA_ACE_ROSC
R225
15K_0402_0.1%
+/-0.1%
TBTA_SS
C701
0.22U_0402_10V6-K
SENSEN
SENSEP
PP_FCM_A6
PP_FCM_A7
PP_FCM_A8
PP_FCM_B7
C_USB_TP
C_USB_TN
HV_GATE2
HV_GATE1
C_USB_BP
C_USB_BN
C_CC1
C_CC2
RPD_G1
RPD_G2
DEBUG_CTL1
DEBUG_CTL2
C_SBU1
C_SBU2
RESETZ
TBT_RESET_N
TBTA_USB2_P_T
TBTA_USB2_N_T
TBTA_USB2_P_B
TBTA_USB2_N_B
TBTA_RFU1
TBTA_RFU2
TBTA_CC1
TBTA_CC2
TBTA_HD2CA_0_P
TBTA_HD2CA_0_N
TBTA_HD2CA_1_P
TBTA_HD2CA_1_N
TBTA_CA2HD_0_P
TBTA_CA2HD_0_N
TBTA_CA2HD_1_P
TBTA_CA2HD_1_N
TBTA_ACE_GPIO1
TBTA_ACE_GPIO2
TBTA_ACE_GPIO3
TBTA_ACE_GPIO5
TBTA_ACE_GPIO6
Recommended ESD 0201 structures
on high speed lines
Security Classification
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Issued Date
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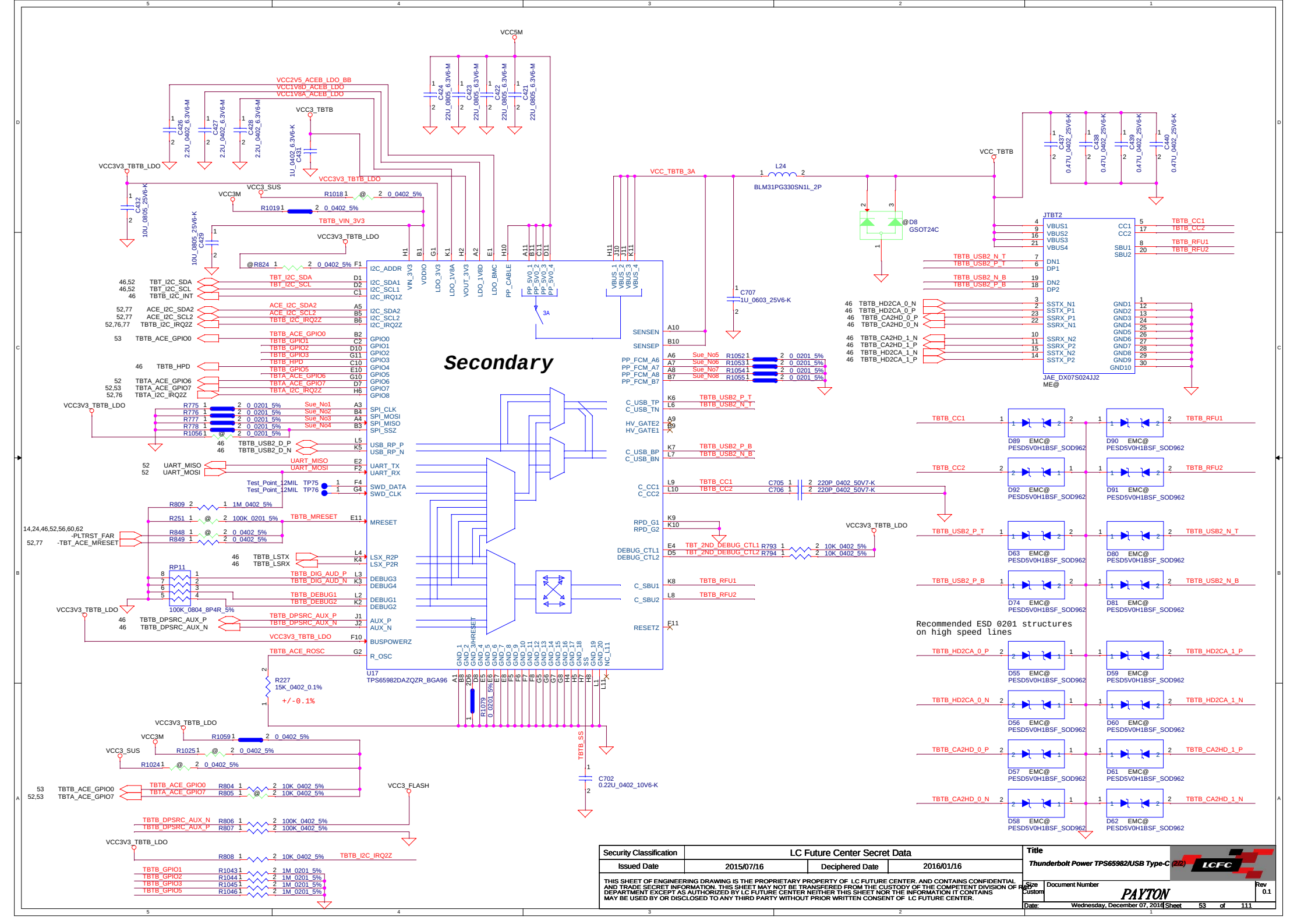
Title
Thunderbolt Power TPS65982/USB Type-C
Size
Custom
Document Number
PAYTON
Rev
0.1
Date:
Wednesday, December 07, 2016
Sheet
52
of
111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VCC3V3_TBTB_LDO
VCC3M
VCC3_SUS
VCC_TBTB
VCC_TBTB_3A
TBTB_VIN_3V3
VCC2V5_ACEB_LDO_BB
VCC1V8D_ACEB_LDO
VCC1V8A_ACEB_LDO
L24
BLM31PG330SN1L_2P
@D8
GSOT24C
C707
1U_0603_25V6-K
JTBT2
JAE_DX07S024JJ2
ME@
U17
TPS65982DAZQZR_BGA96
I2C_ADDR
I2C_SDA1
I2C_SCL1
I2C_IRQ1Z
I2C_SDA2
I2C_SCL2
I2C_IRQ2Z
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SSZ
USB_RP_P
USB_RP_N
UART_TX
UART_RX
SWD_DATA
SWD_CLK
MRESET
LSX_R2P
LSX_P2R
DEBUG3
DEBUG4
DEBUG1
DEBUG2
AUX_P
AUX_N
BUSPOWERZ
R_OSC
SENSEN
SENSEP
C_USB_TP
C_USB_TN
HV_GATE2
HV_GATE1
C_USB_BP
C_USB_BN
C_CC1
C_CC2
RPD_G1
RPD_G2
DEBUG_CTL1
DEBUG_CTL2
C_SBU1
C_SBU2
RESETZ
TBTB_SS
C702
0.22U_0402_10V6-K
R227
15K_0402_0.1%
+/-0.1%
VCC3_FLASH
Recommended ESD 0201 structures
on high speed lines
Security Classification
LC Future Center Secret Data
Issued Date
2015/07/16
Deciphered Date
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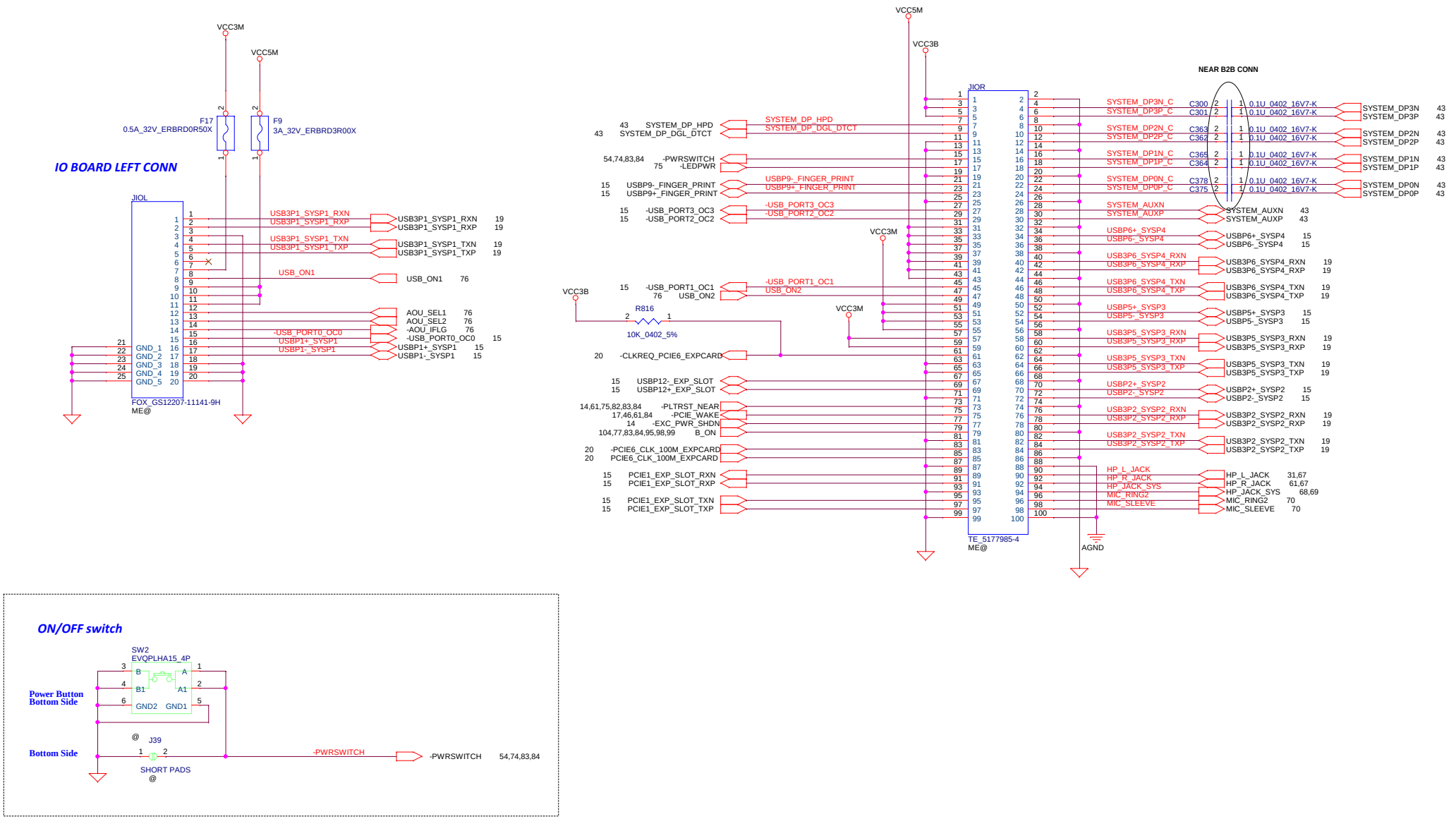
Title
Thunderbolt Power TPS65982/USB Type-C (2/2)
LCFC
Size
Custom
Document Number
PAYTON
Rev
0.1
Date:
Wednesday, December 07, 2016
Sheet
53
of
111



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Title: B2B CONN (IO BOARD RIGHT)

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Date: Wednesday, December 07, 2016 Sheet 54 of 111

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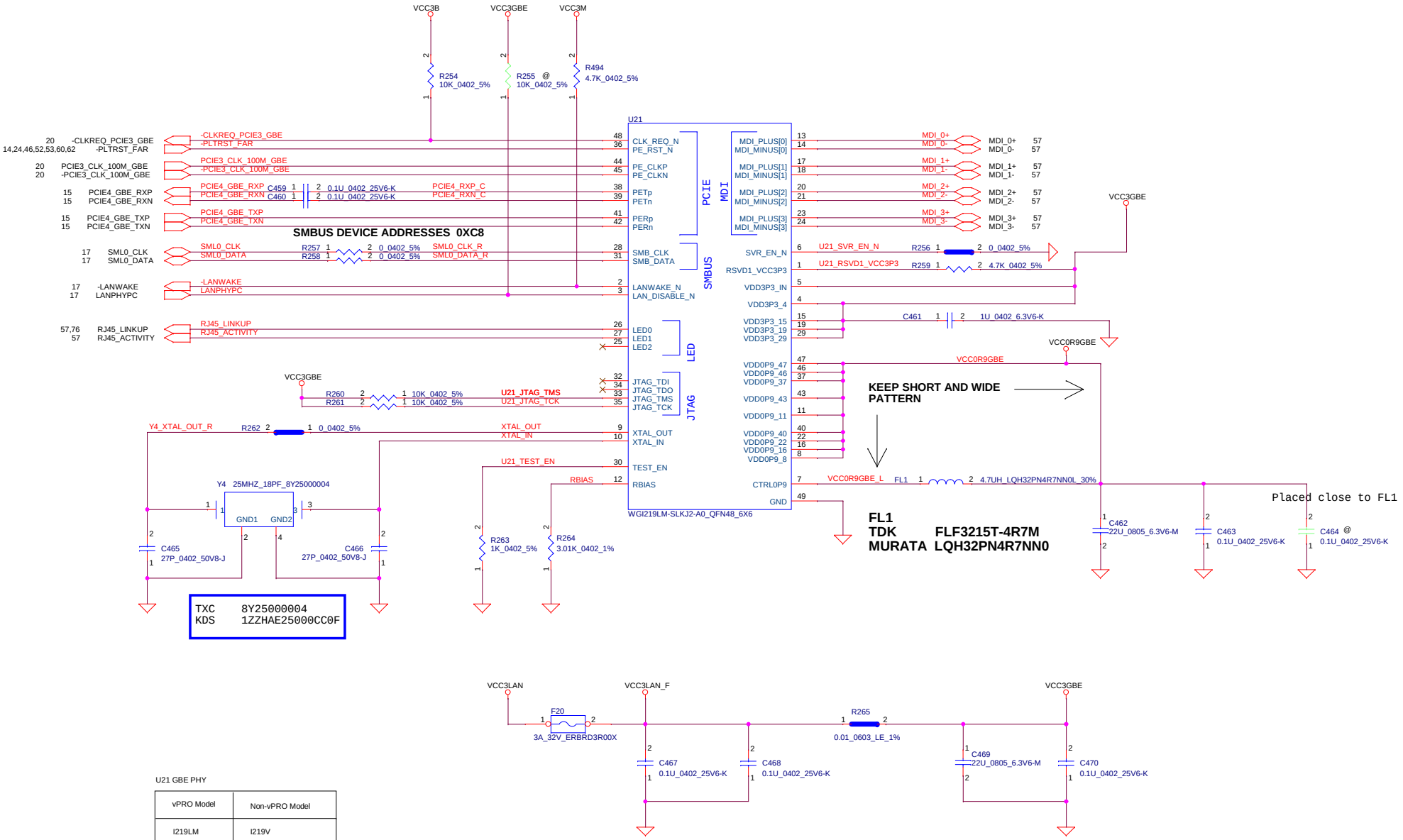
Title

USB POWER/CONN (2/2)

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 55 of 111



U21 GBE PHY

vPRO Model	Non-vPRO Model
I219LM	I219V

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Issued Date	2015/07/16	Deciphered Date	2016/01/16

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Title: GBE JACKSONVILLE

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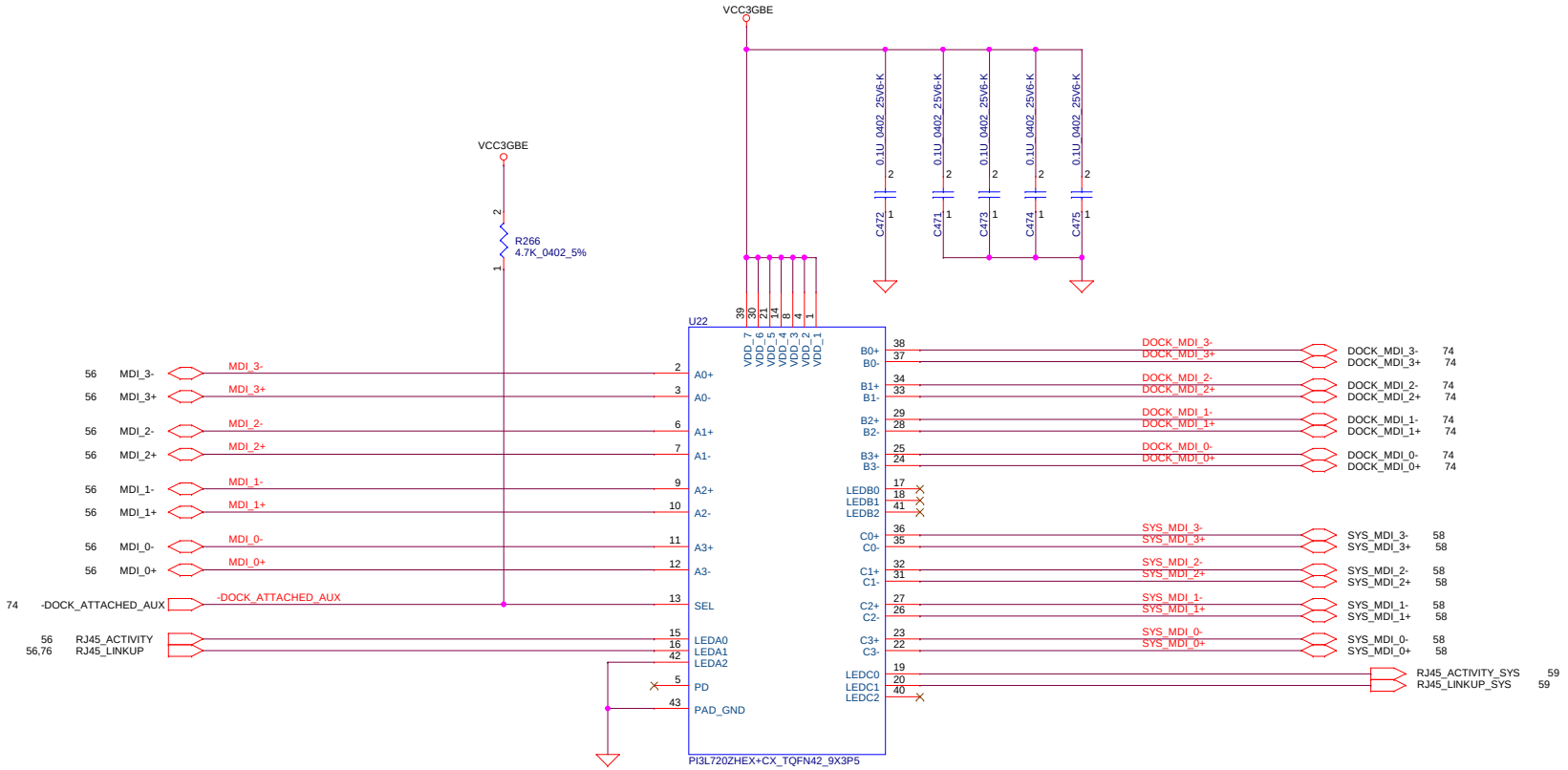
Date: Wednesday, December 07, 2016 | Sheet 56 of 111



U22

Vendor	P/N
Pericom TI	PI3L720ZHEX+CX TS3L501E

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Issued Date	2015/07/16	Deciphered Date	2016/01/16

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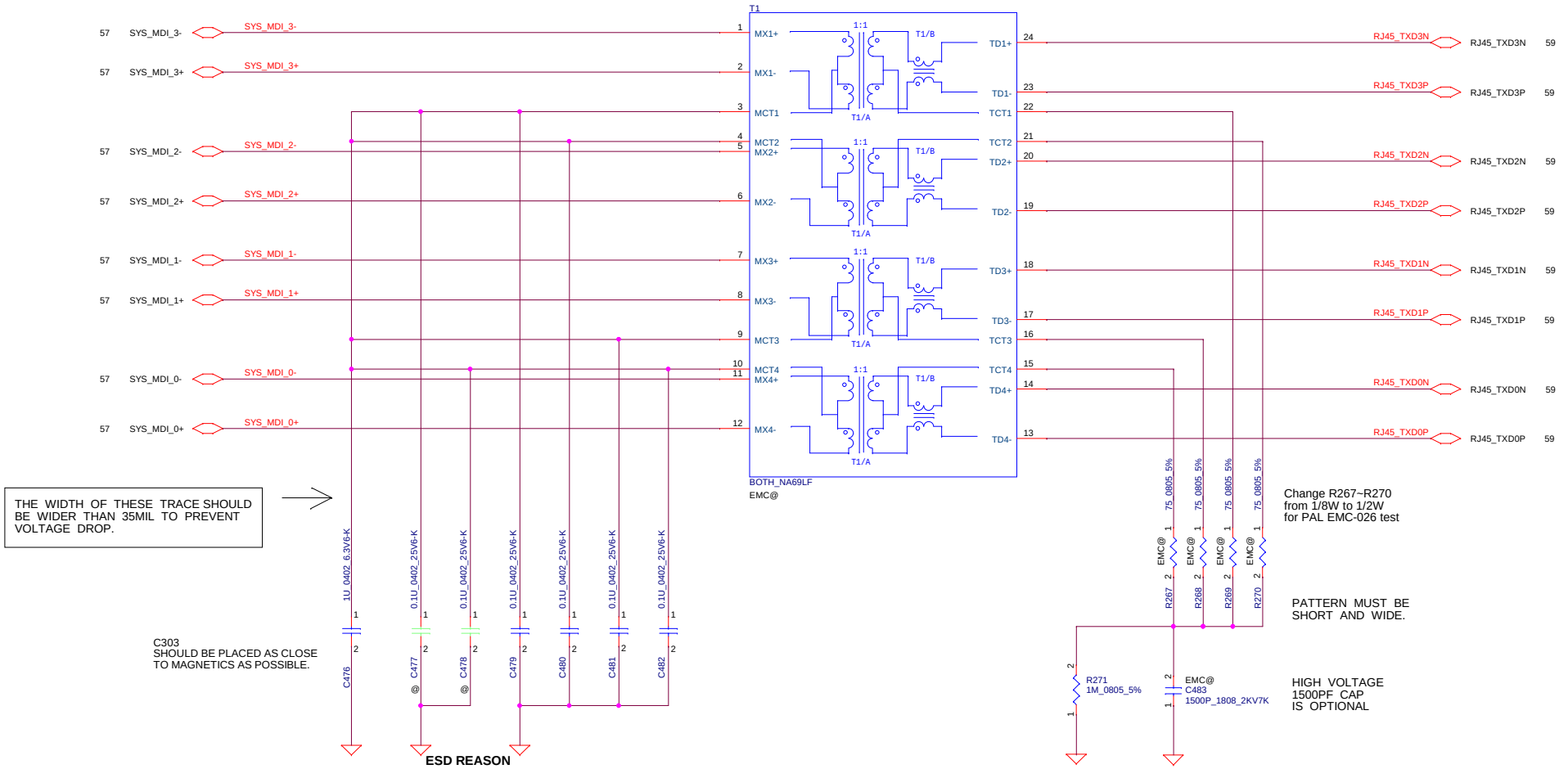
Title: GBE LAN SWITCH

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 57 of 111



Vendor	P/N
Timag	IH-115-F
Bothhand	NA69LF

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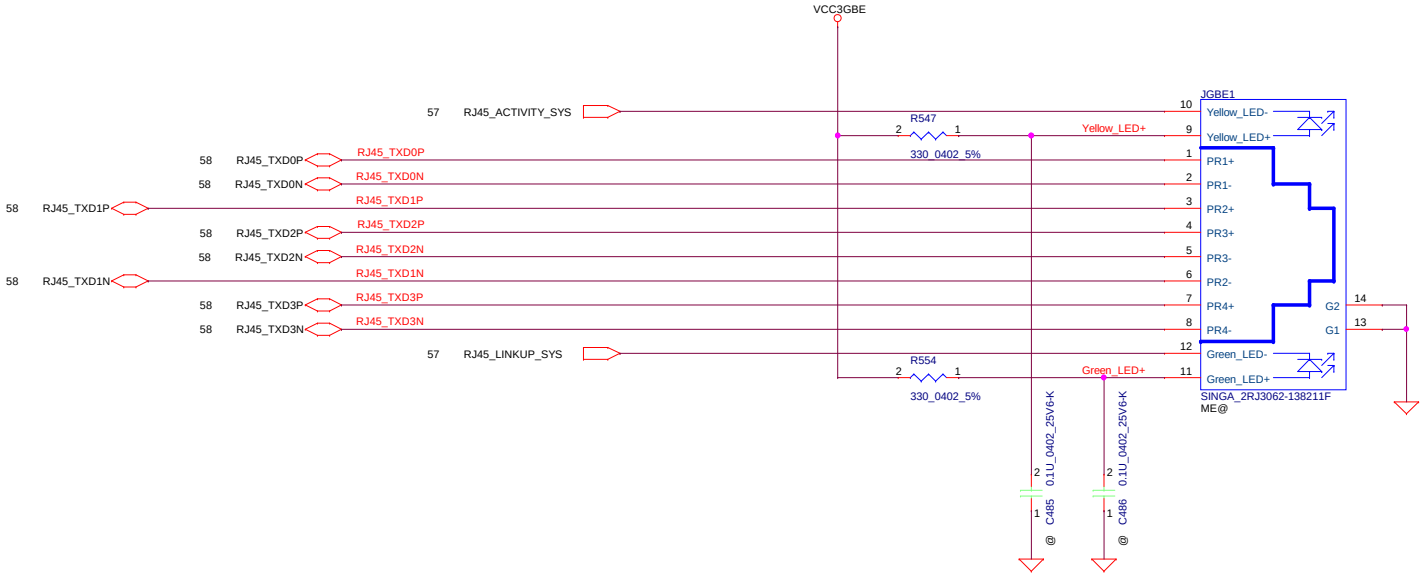
Title: GBE MAGNETICS

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 58 of 111

D23, D24 EMC Parts



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Title: **RJ45 CONNECTOR**

LCFC

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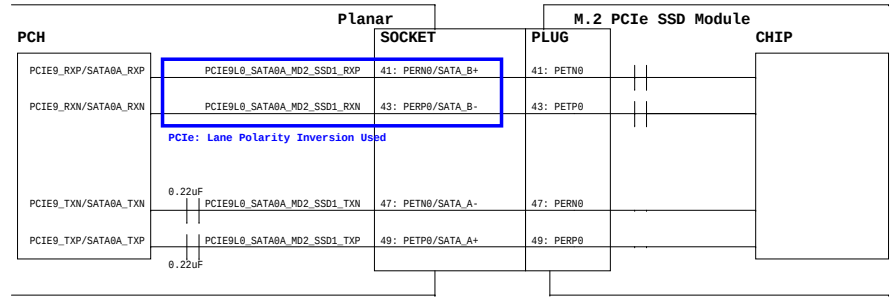
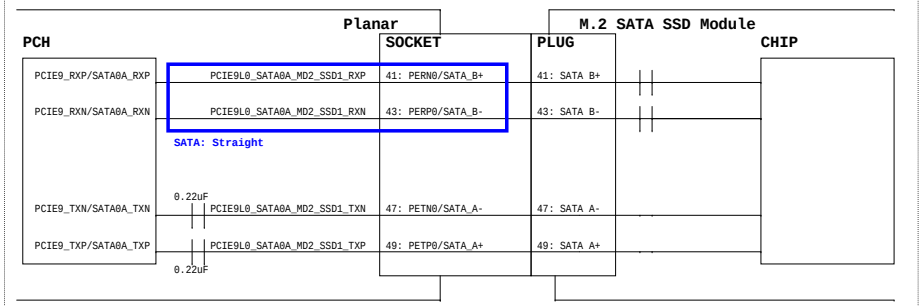
Date: Wednesday, December 07, 2016 | Sheet 59 of 111

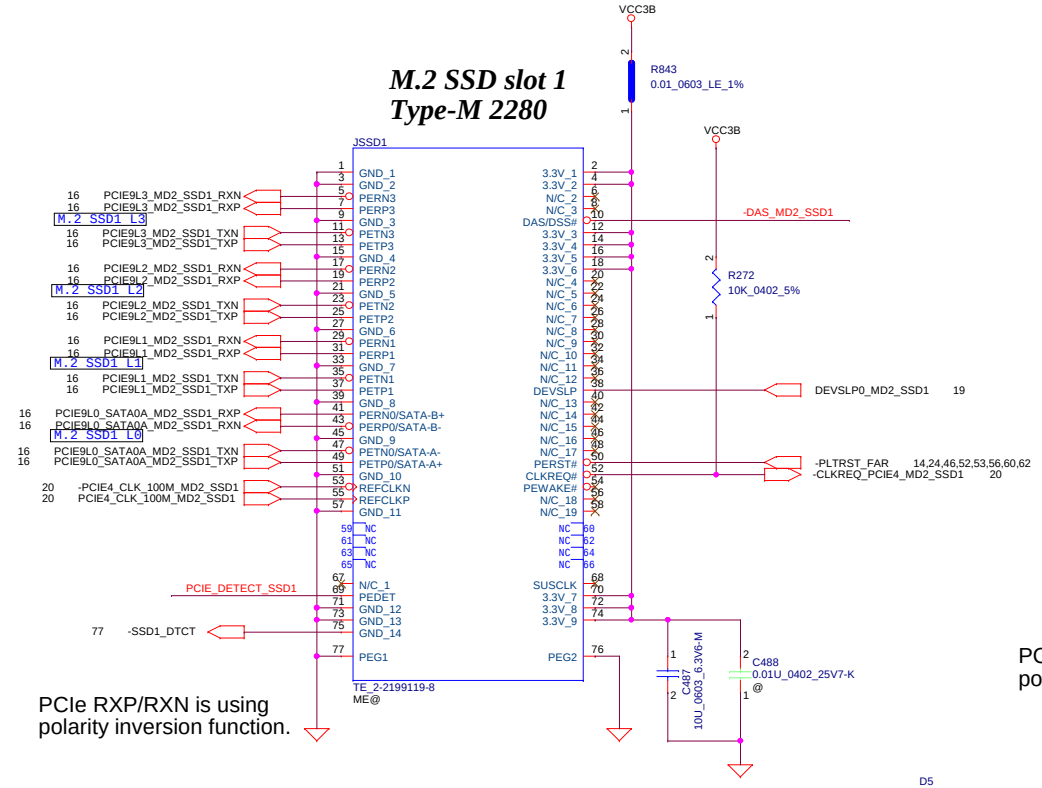
M.2 PCIe SSD



M.2 SATA SSD

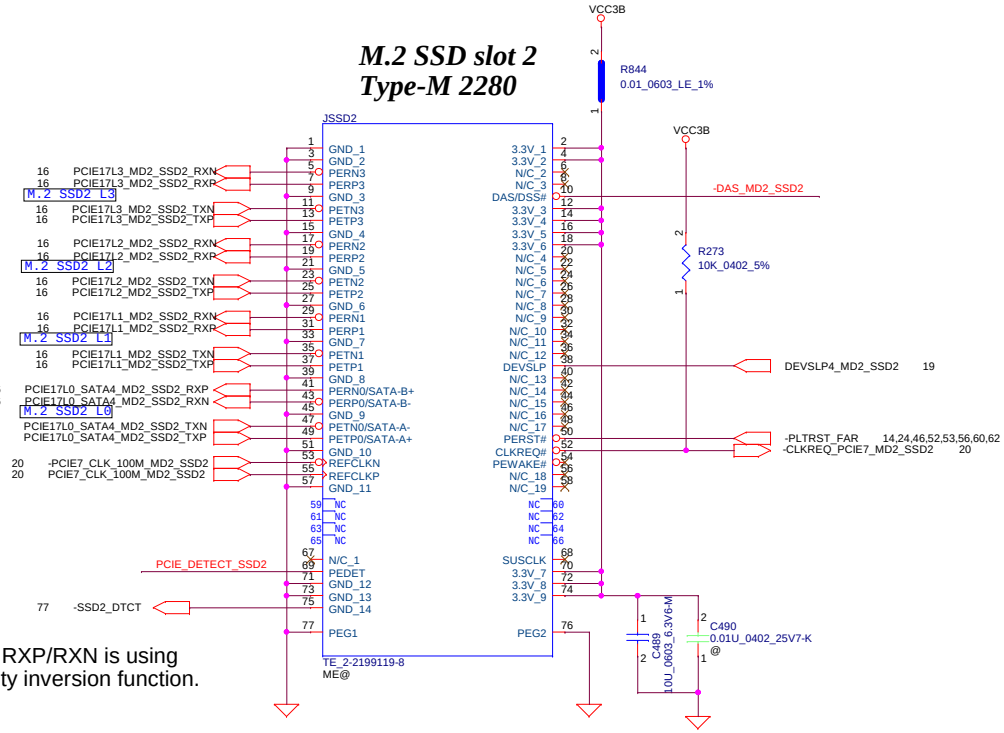


M.2 SSD slot 1 Type-M 2280

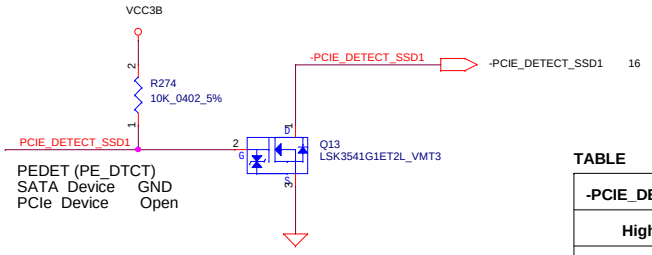


PCIe RXP/RXN is using polarity inversion function.

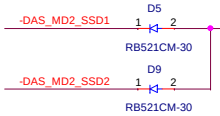
M.2 SSD slot 2 Type-M 2280

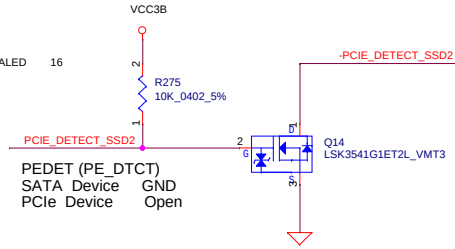


PCIe RXP/RXN is using polarity inversion function.



PEDET (PE_DTCT)
SATA Device GND
PCIe Device Open





PEDET (PE_DTCT)
SATA Device GND
PCIe Device Open

TABLE

-PCIE_DETECT_SSD1	Device
High	SATA SSD
Low	PCIe SSD

TABLE

-PCIE_DETECT_SSD2	Device
High	SATA SSD
Low	PCIe SSD

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Title: *M.2 SATA/PCIE SSD CARD SLOT*

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 60 of 111

PRTC3

BATT CR2032 3V 225MAH

RTC@

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Issued Date	2013/11/08	Deciphered Date	2013/11/08

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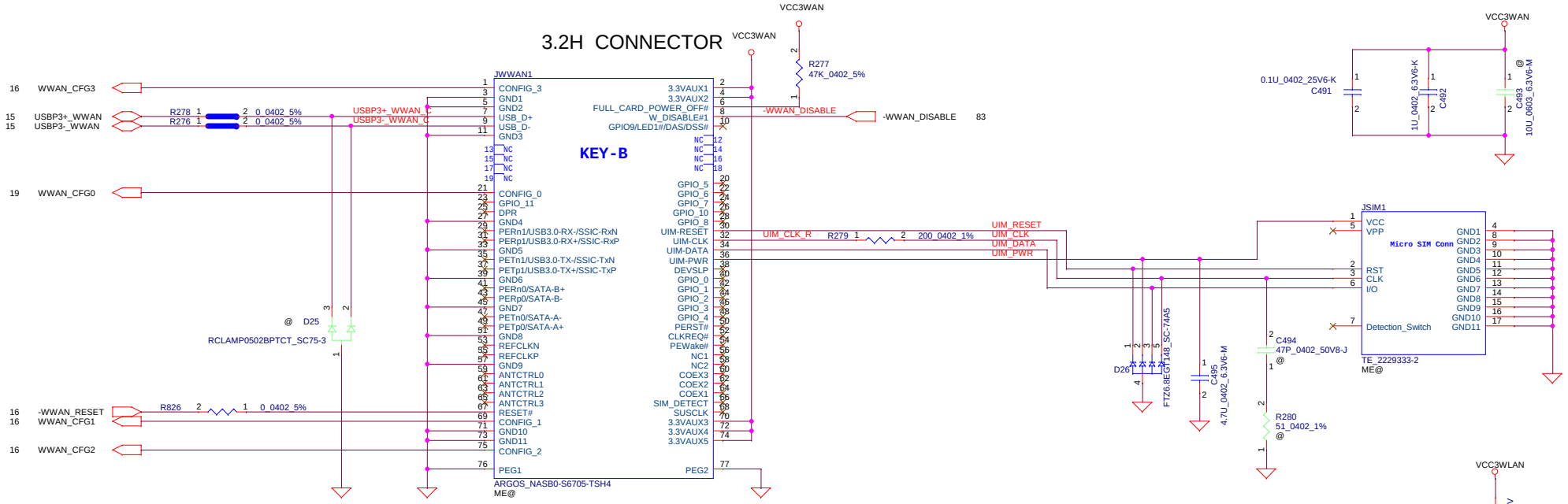
Title

Load BOM Only(RTC BATTE

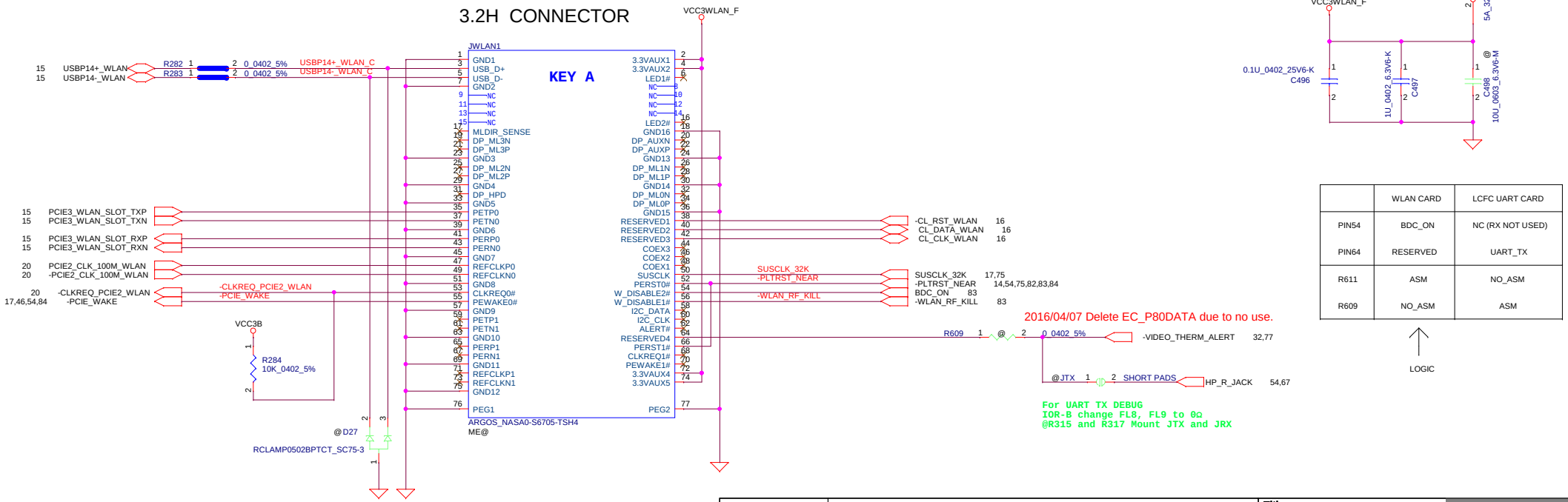
Size	Document Number	Rev
B		0.2

Date: Wednesday, December 07, 2016 Sheet 60 of 60

TYPE-B NGFF CCARD FOR WWAN



TYPE-A NGFF CCARD FOR WLAN



	WLAN CARD	LCFC UART CARD
PIN54	BDC_ON	NC (RX NOT USED)
PIN64	RESERVED	UART_TX
R611	ASM	NO_ASM
R609	NO_ASM	ASM

LOGIC

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Issued Date	2015/07/16	Deciphered Date	2016/01/16

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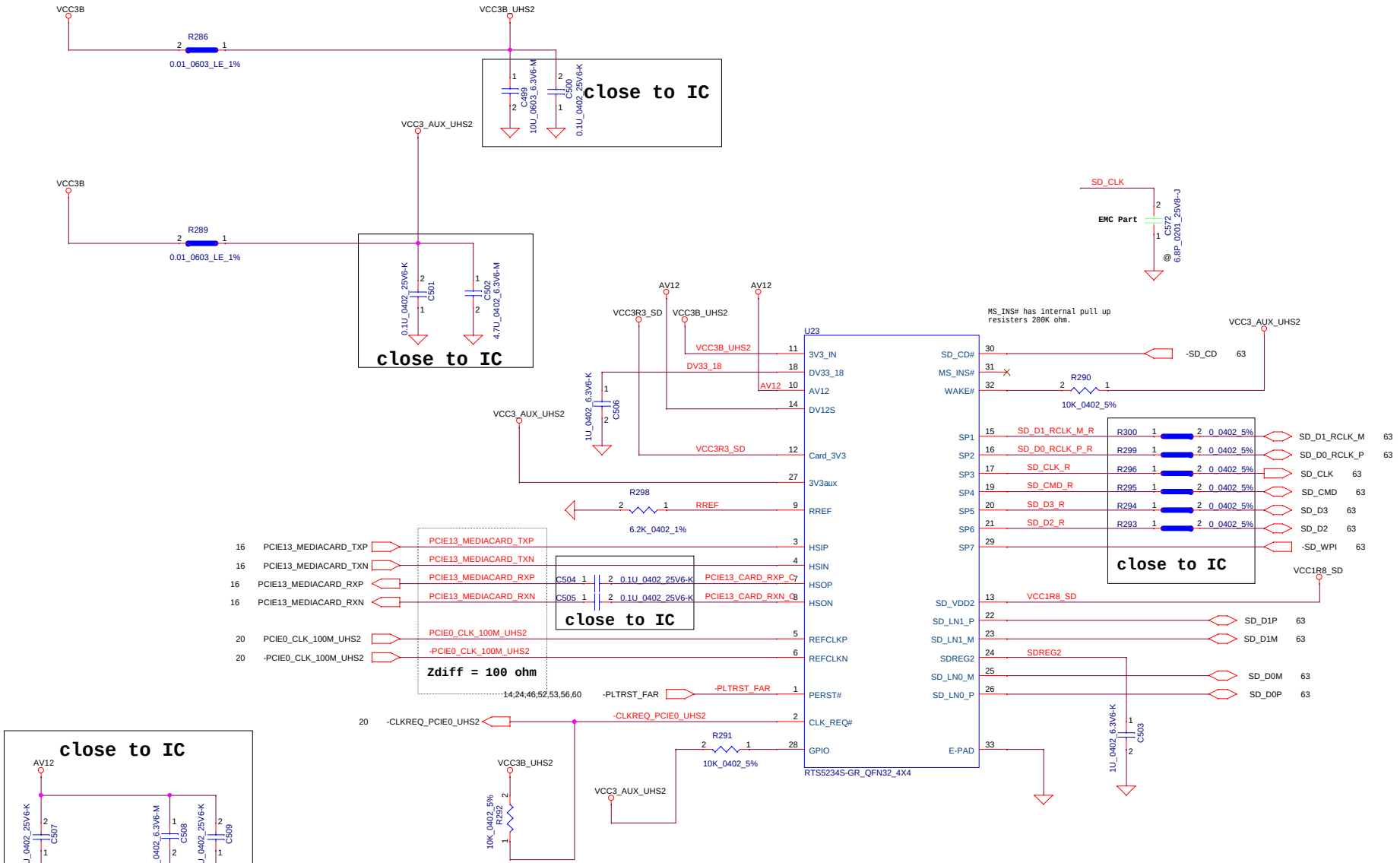
Title: **M.2 WIRELESS CARD SLOT**

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 61 of 111



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Title: MEDIA CARD CONTROLLER UHS-II

LCFC

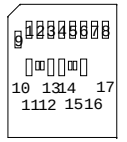
Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 62 of 111

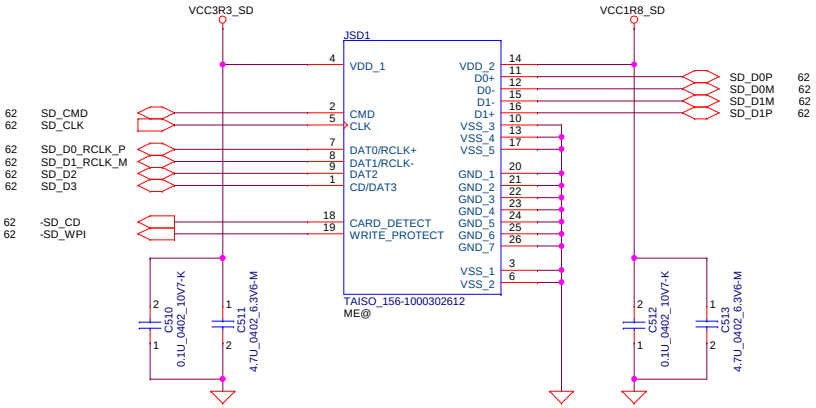
Normal type UHS-II SD Slot

Pin No	SD Mode	UHS II Mode
1	CD/DAT3	
2	CMD	
3	VSS1	
4	VDD	VDD1
5	CLK	
6	VSS2	
7	DAT0	RCLKP
8	DAT1	RCLKM
9	DAT2	
10		VSS3
11		D0P
12		D0M
13		VSS4
14		VDD2
15		D1M
16		D1P
17		VSS5
CD		
WP		
	CARD DETECT	
	WRITE PROTECT	

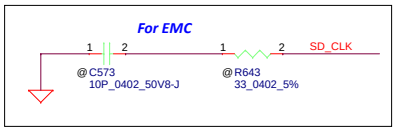
Bottom View



UHS II Interface	UHS I Inteface
4 VDD1 3.3V	1 CD/DAT3
7 RCLKP	2 CMD
8 RCLKM	3 VSS1
10 VSS3	4 VDD 3.3V
11 D0P	5 CLK
12 D0M	6 VSS2
13 VSS4	7 DAT0
14 VDD2 1.8V	8 DAT1
15 D1M	9 DAT2
16 D1P	
17 VSS5	



CD : Low => Insertion Card
High => No Card
WP : Low => Write Protection On
High => Wite Protection Off or No Card



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Title: MEDIA CARD INTERFACE UHS-II

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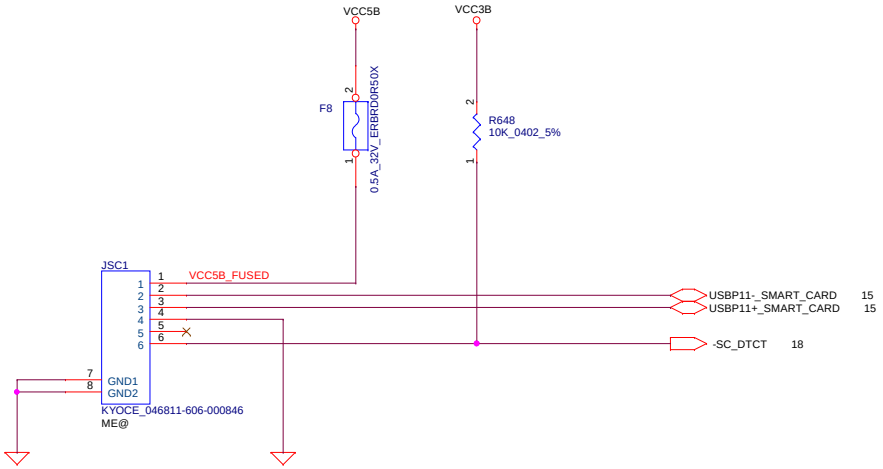
Date: Wednesday, December 07, 2016 | Sheet 63 of 111



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Title: ***SMART CARD READER***

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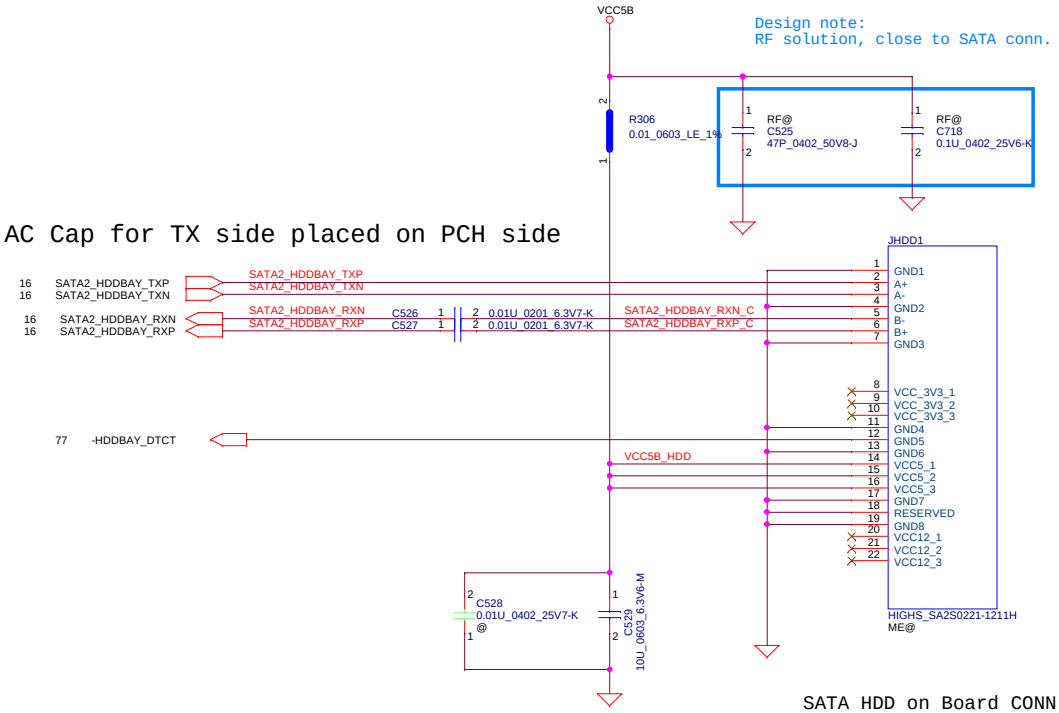
Date: Wednesday, December 07, 2016	Sheet 64 of 111	



SATA HDD on Board CONN

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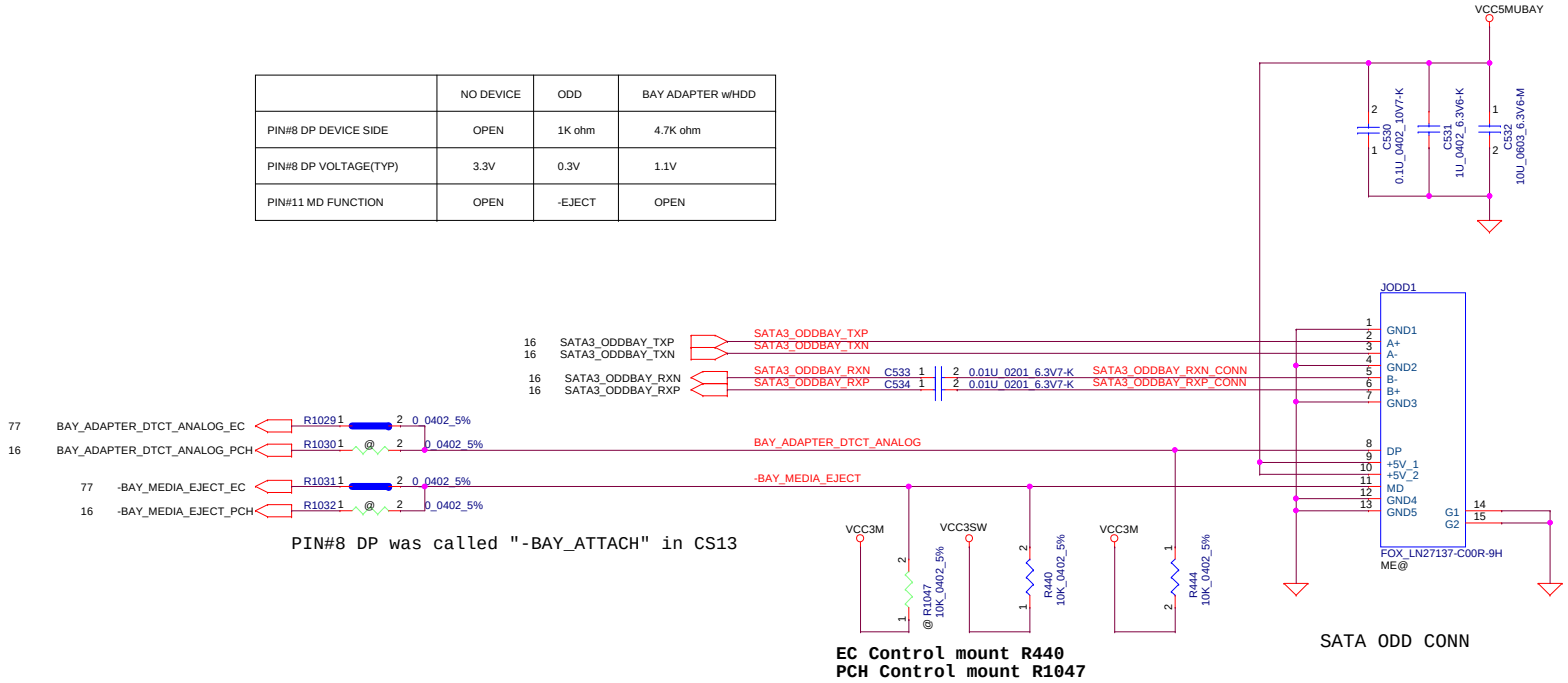
Title: SATA HDD CONN

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 65 of 111

	NO DEVICE	ODD	BAY ADAPTER w/HDD
PIN#8 DP DEVICE SIDE	OPEN	1K ohm	4.7K ohm
PIN#8 DP VOLTAGE(TYP)	3.3V	0.3V	1.1V
PIN#11 MD FUNCTION	OPEN	-EJECT	OPEN



PIN#8 DP was called "-BAY_ATTACH" in CS13

EC Control mount R440
PCH Control mount R1047

SATA ODD CONN

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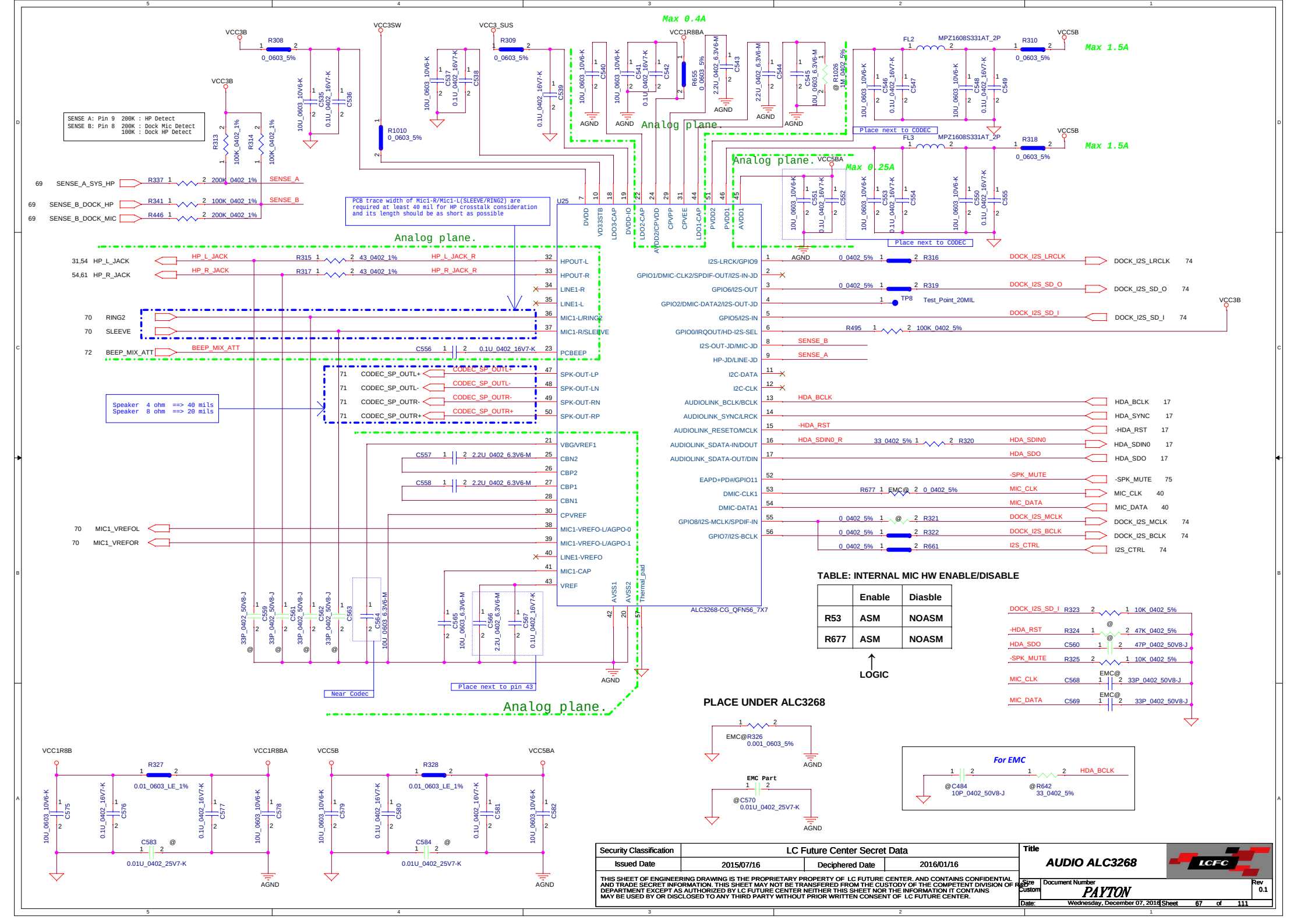
Title: **SATA ODD CONN**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 66 of 111


Max 0.4A
Max 1.5A
Max 1.5A
Max 0.25A
Analog plane.
Analog plane.
Analog plane.
Analog plane.
Place next to CODEC
Place next to CODEC
SENSE A: Pin 9 200K : HP Detect
SENSE B: Pin 8 200K : Dock Mic Detect
100K : Dock HP Detect
PCB trace width of Mic1-R/Mic1-L(SLEEVE/RING2) are required at least 40 mil for HP crosstalk consideration and its length should be as short as possible
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils
Near Codec
Place next to pin 43
ALC3268-CG_QFN56_7X7
TABLE: INTERNAL MIC HW ENABLE/DISABLE
Enable
Diasble
R53 ASM NOASM
R677 ASM NOASM
LOGIC
PLACE UNDER ALC3268
EMC@R326 0.001_0603_5%
EMC Part
@C570 0.01U_0402_25V7-K
For EMC
@C484 10P_0402_50V8-J
@R642 33_0402_5%
0.01U_0402_25V7-K
0.01U_0402_25V7-K
Security Classification
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Title
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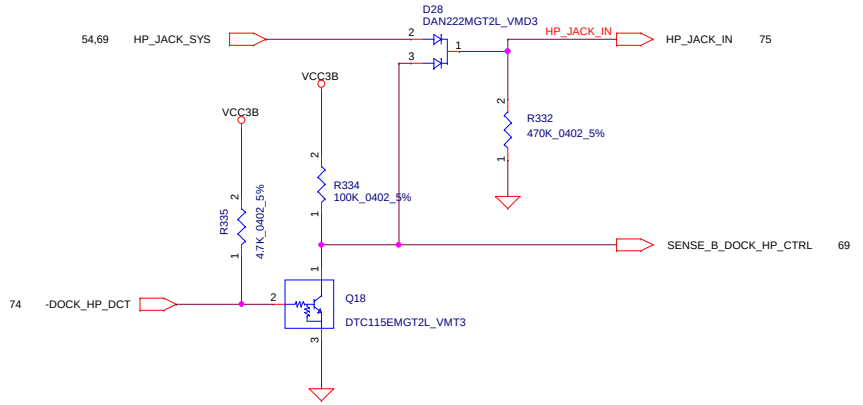
Size
Custom
Document Number
PAYTON
Rev
0.1
Date:
Wednesday, December 07, 2016
Sheet
67
of
111



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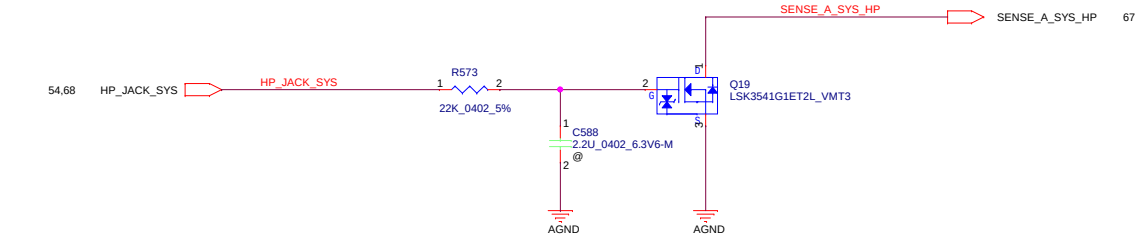
Title: **AUDIO CONNECTOR**

Size: Custom	Document Number: PAYTON	Rev: 0.1
Date: Wednesday, December 07, 2016	Sheet 68 of 111	



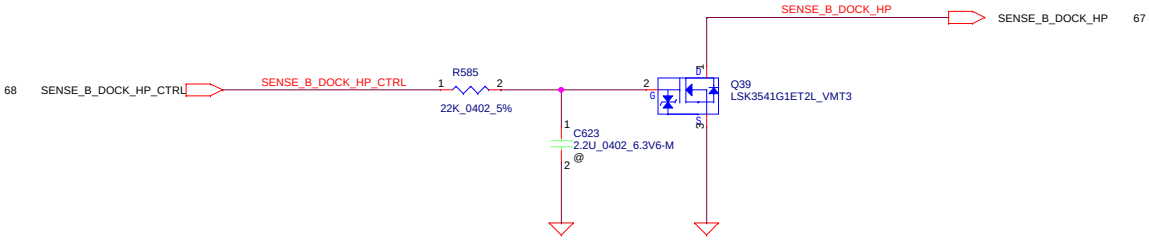
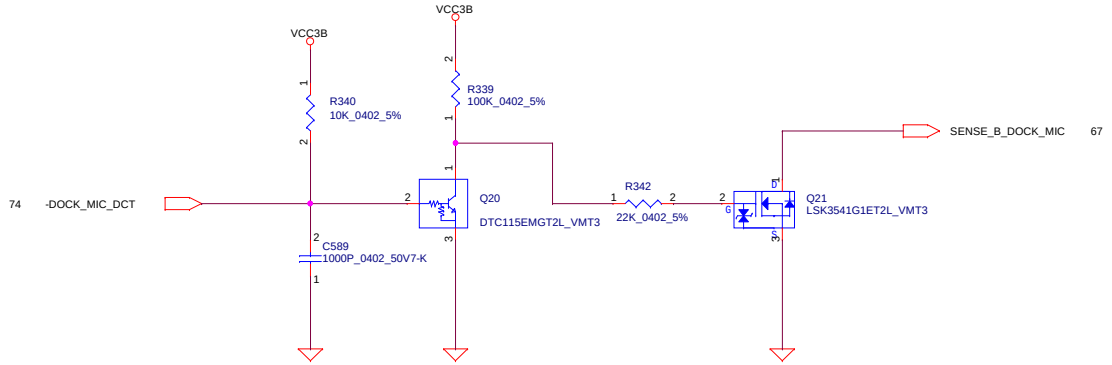
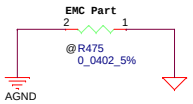


TABLE: DOCK MIC HW ENABLE/DISABLE

	Enable	Diasble
R340	ASM	NOASM
R446	ASM	NOASM
R339	ASM	NOASM
Q20	ASM	NOASM
R342	ASM	NOASM
Q21	ASM	NOASM

LOGIC





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Issued Date	2015/07/16	Deciphered Date	2016/01/16

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Title: **AUDIO JACK SENSE**

LCFC

Size	Document Number	Rev
Custom	PAYTON	0.1

Date: Wednesday, December 07, 2016 Sheet 69 of 111

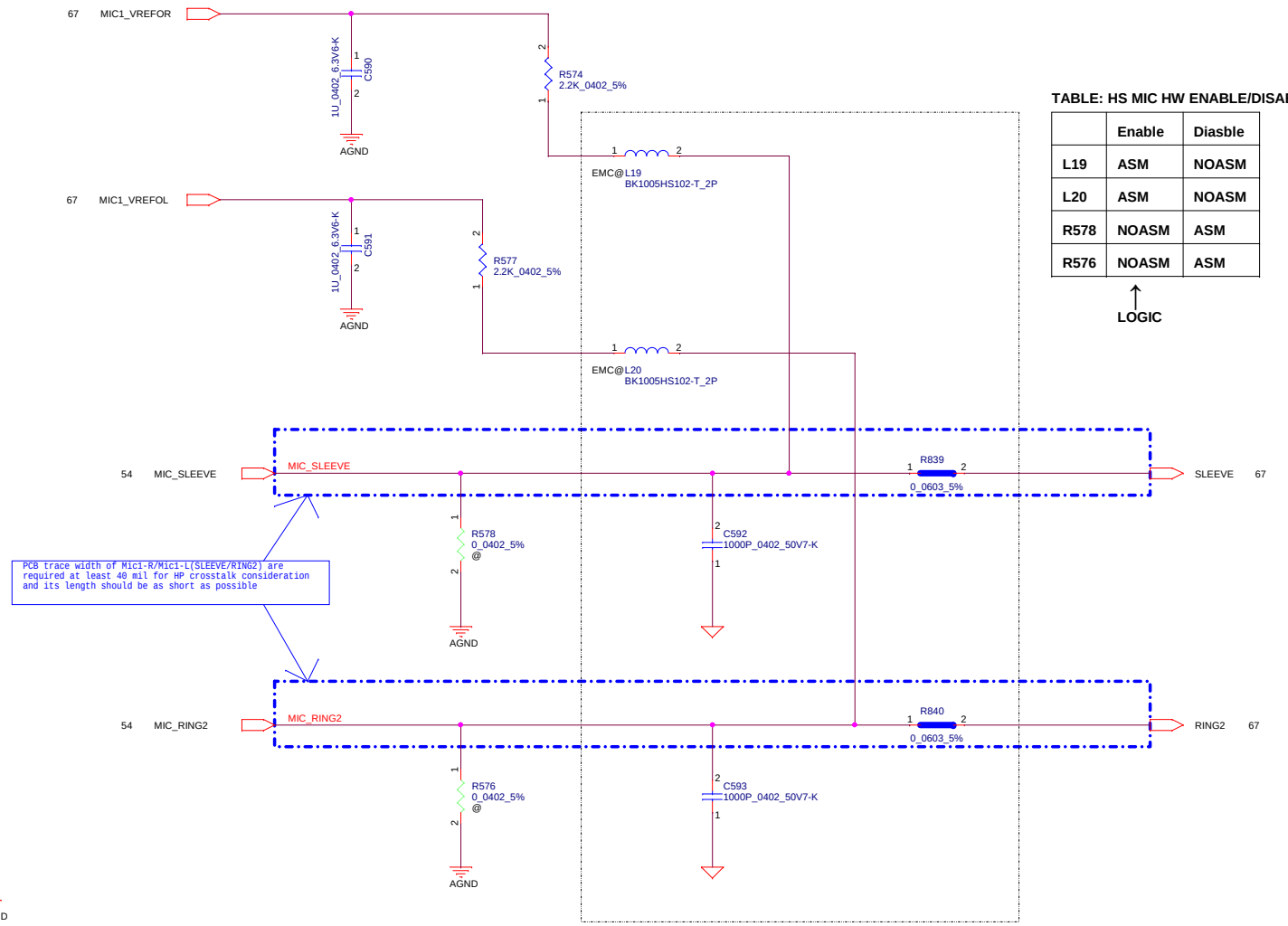

TABLE: HS MIC HW ENABLE/DISABLE

	Enable	Diasble
L19	ASM	NOASM
L20	ASM	NOASM
R578	NOASM	ASM
R576	NOASM	ASM

LOGIC

NEAR EXT MIC CONN

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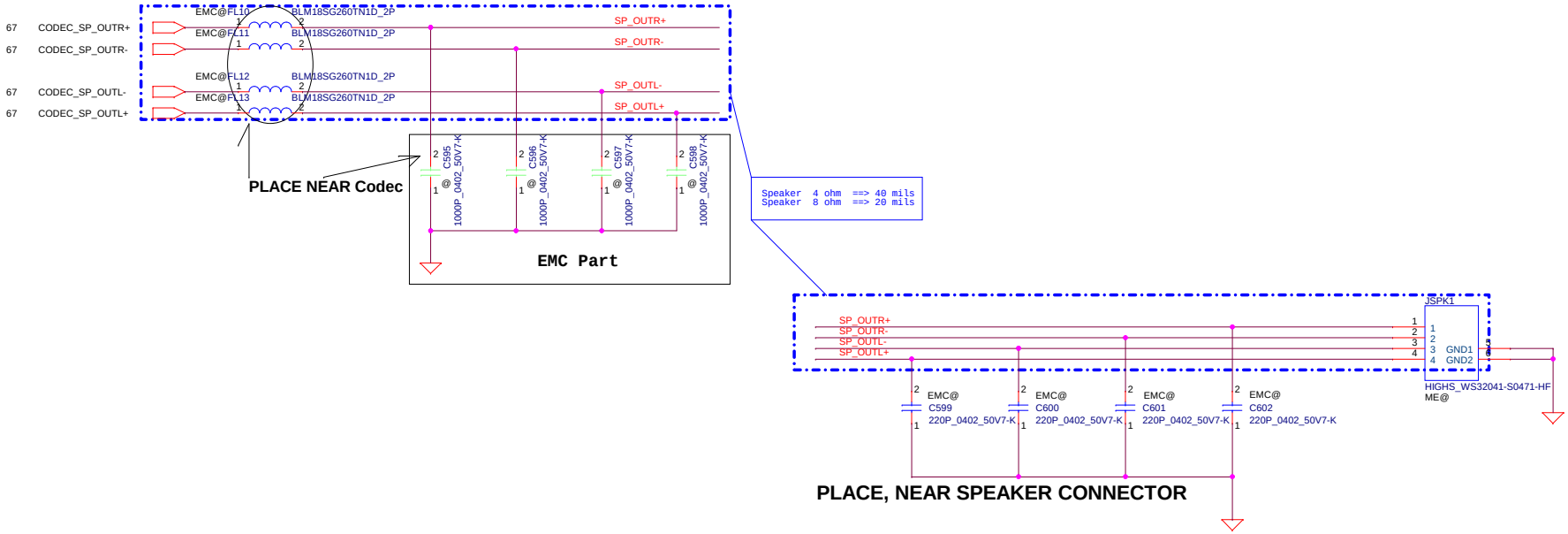
Title: **AUDIO EXT MIC I/F**

Size: Custom	Document Number	Rev: 0.1
Date: Wednesday, December 07, 2016	Sheet 70 of 111	

ALC3268 speaker output part



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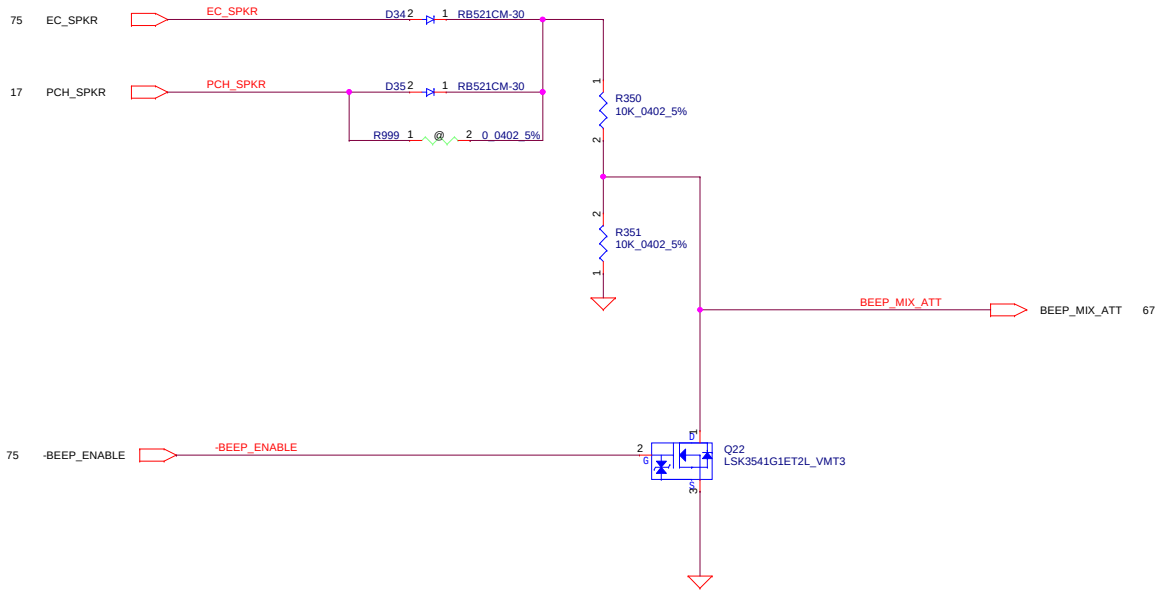
Title: **AUDIO SPEAKER**

LCFC

Size	Document Number	Rev
Custom	PAYTON	0.1

Date: Wednesday, December 07, 2016 Sheet 71 of 111

D34 for Enhanced PC Beep function.
No use mount R999, unmount D34, D35



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Title: AUDIO BEEP

Size: Custom | Document Number: PAYTON | Rev: 0.1

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Title

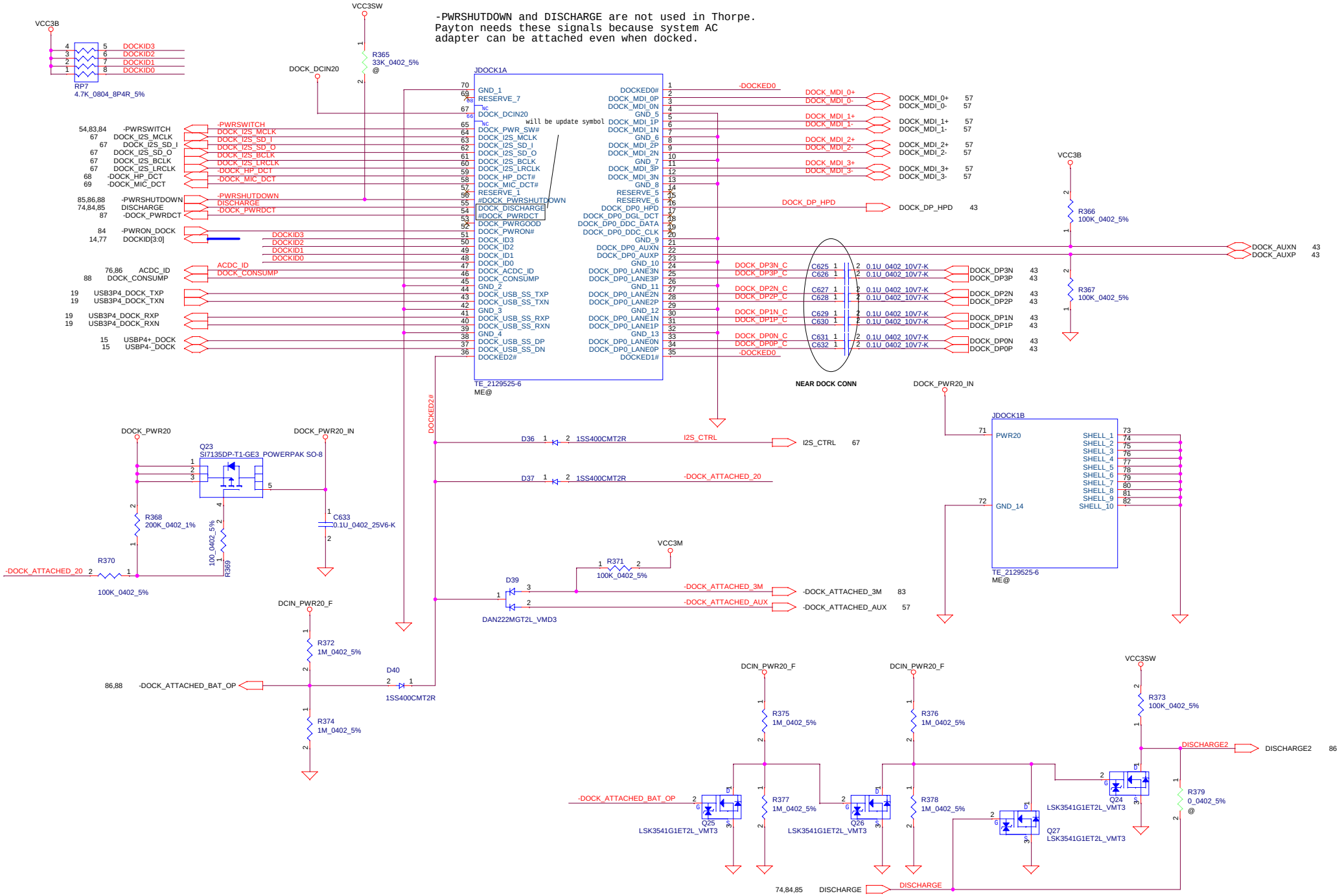
SMART AMP

LCFC

Size	Document Number	Rev
Custom	PAYTON	0.1

Date: Wednesday, December 07, 2016 Sheet 73 of 111

-PWRSHUTDOWN and DISCHARGE are not used in Thorpe.
Payton needs these signals because system AC
adapter can be attached even when docked.



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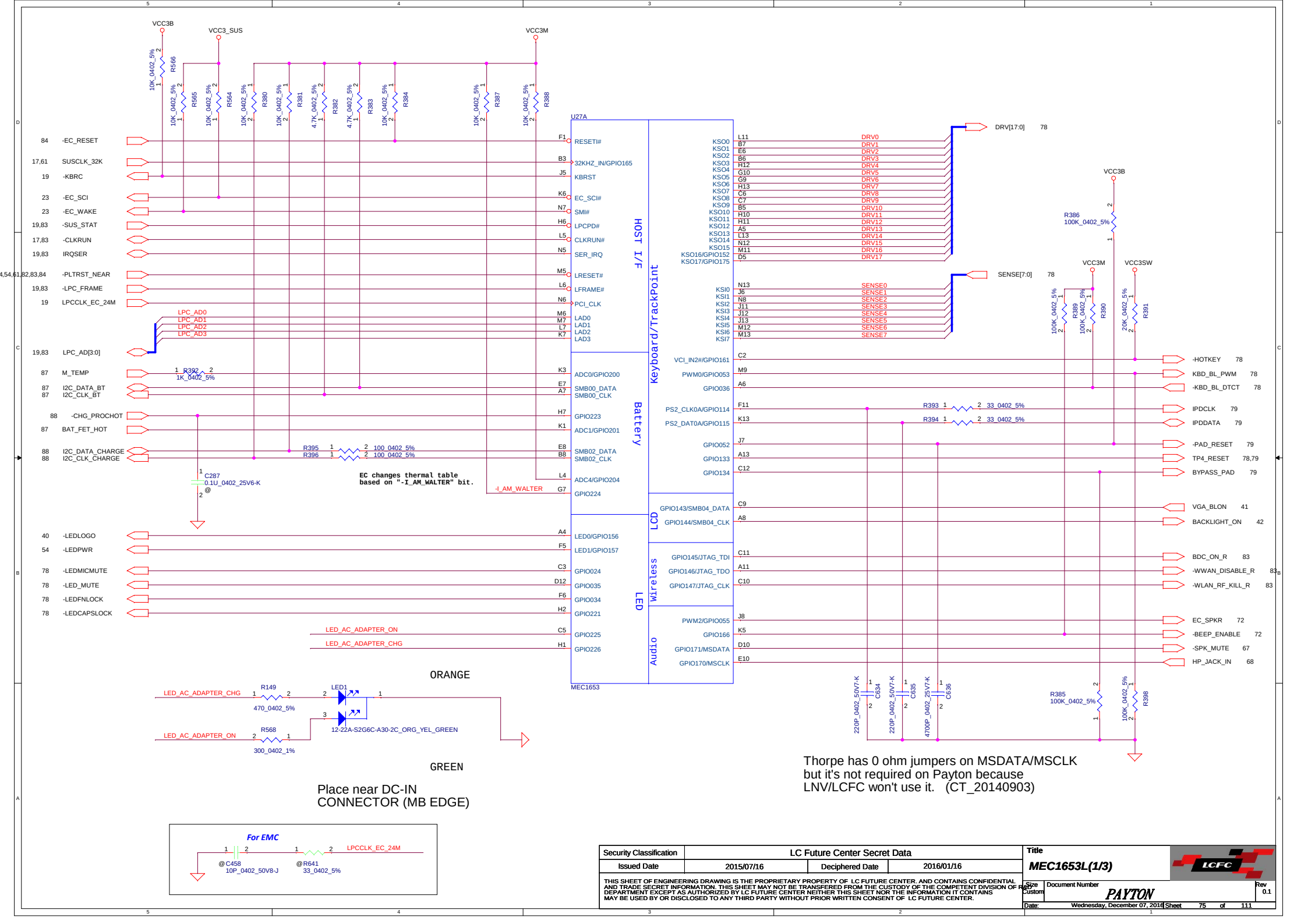
Title: **DOCKING CONNECTOR**

LCFC

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 74 of 111



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Issued Date	2015/07/16	Deciphered Date	2016/01/16

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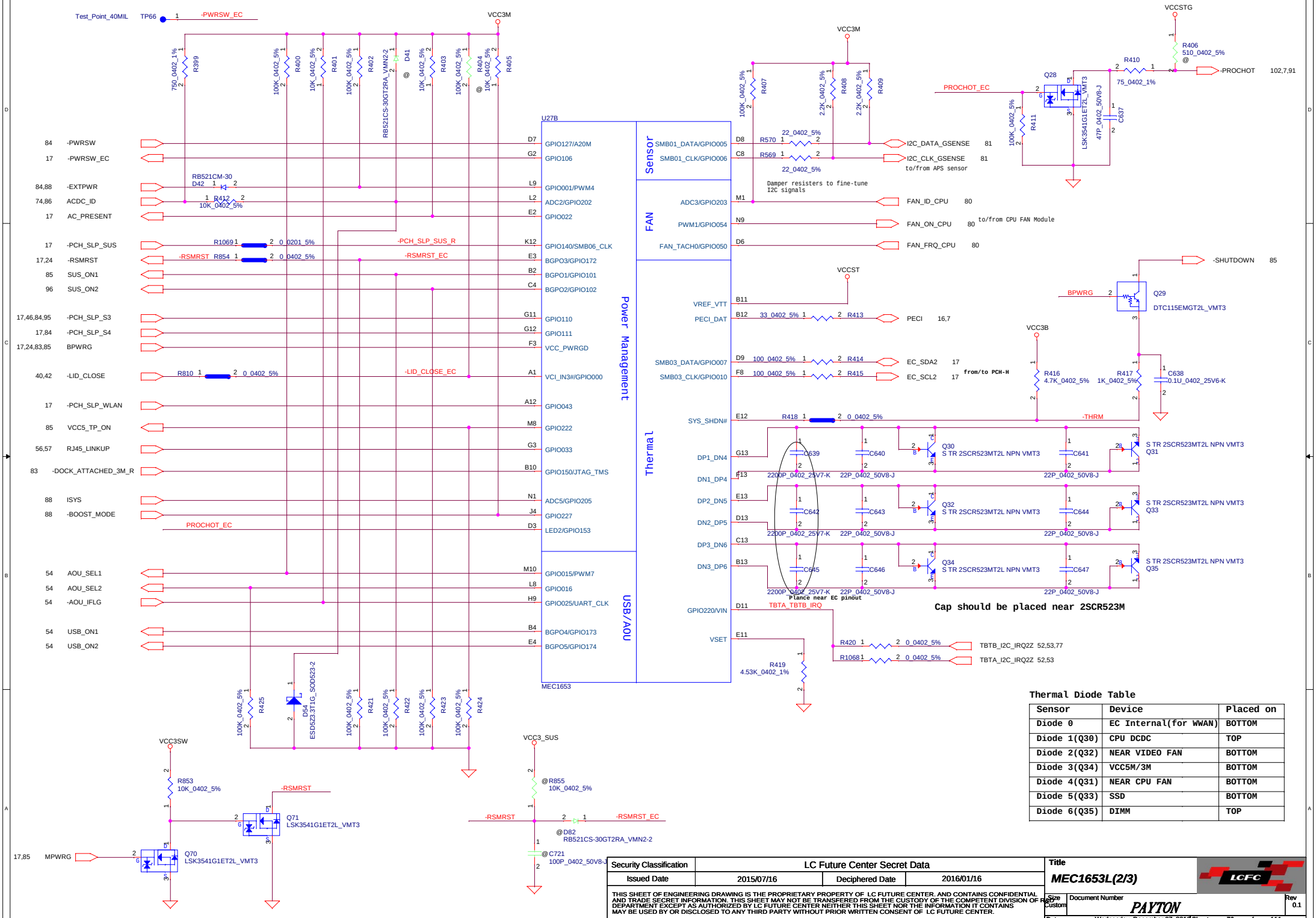
Title: **MEC1653L(1/3)**

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 75 of 111



Thermal Diode Table

Sensor	Device	Placed on
Diode 0	EC Internal(for WWAN)	BOTTOM
Diode 1(Q30)	CPU DCDC	TOP
Diode 2(Q32)	NEAR VIDEO FAN	BOTTOM
Diode 3(Q34)	VCC5M/3M	BOTTOM
Diode 4(Q31)	NEAR CPU FAN	BOTTOM
Diode 5(Q33)	SSD	BOTTOM
Diode 6(Q35)	DIMM	TOP

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

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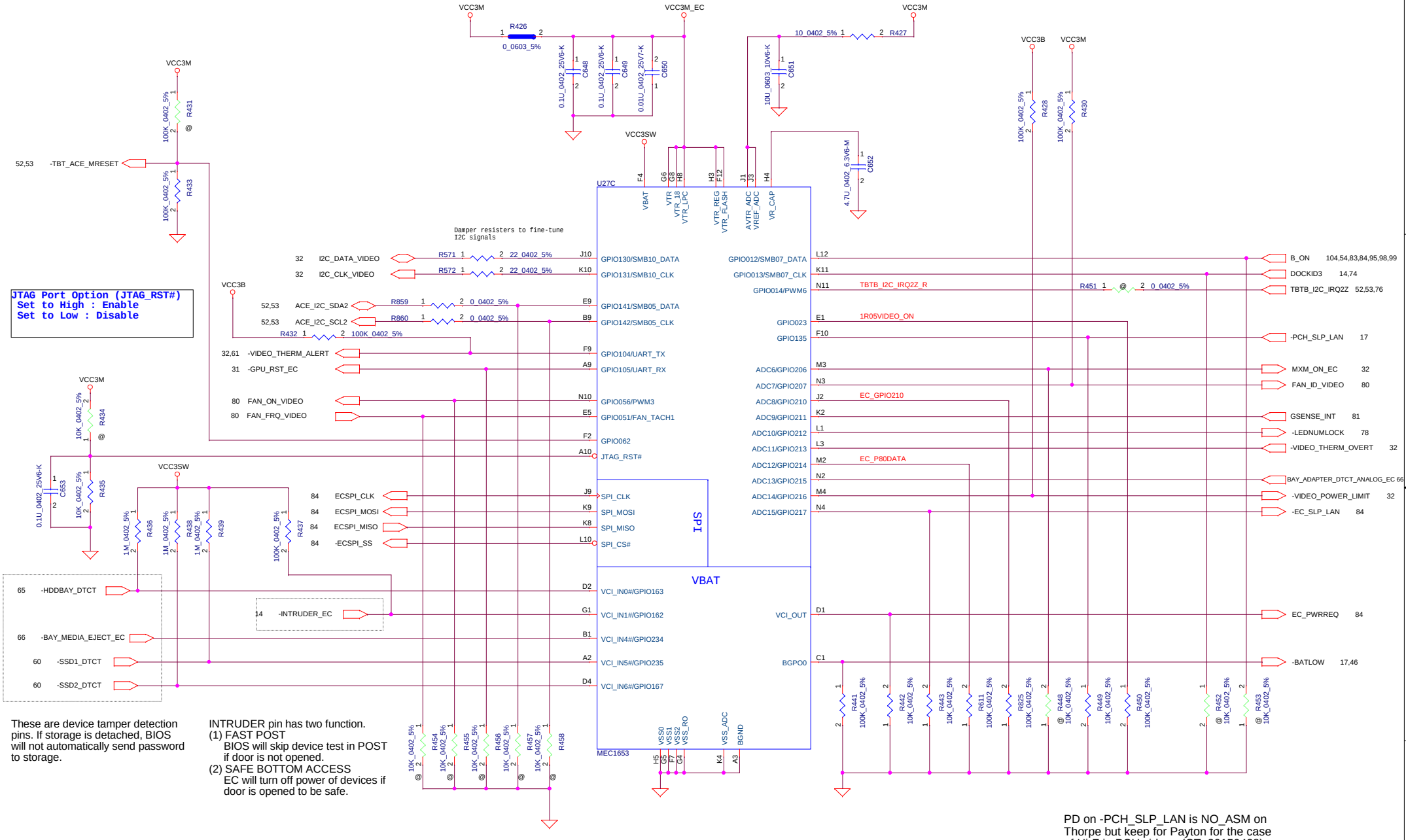
Title: **MEC1653L(2/3)**

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 76 of 111



These are device tamper detection pins. If storage is detached, BIOS will not automatically send password to storage.

INTRUDER pin has two function.
(1) FAST POST
BIOS will skip device test in POST if door is not opened.
(2) SAFE BOTTOM ACCESS
EC will turn off power of devices if door is opened to be safe.

PD on -PCH_SLP_LAN is NO_ASM on Thorpe but keep for Payton for the case of Hi-Z in PCH side. (CT_20150428)

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Issued Date	2015/07/16	Deciphered Date	2016/01/16

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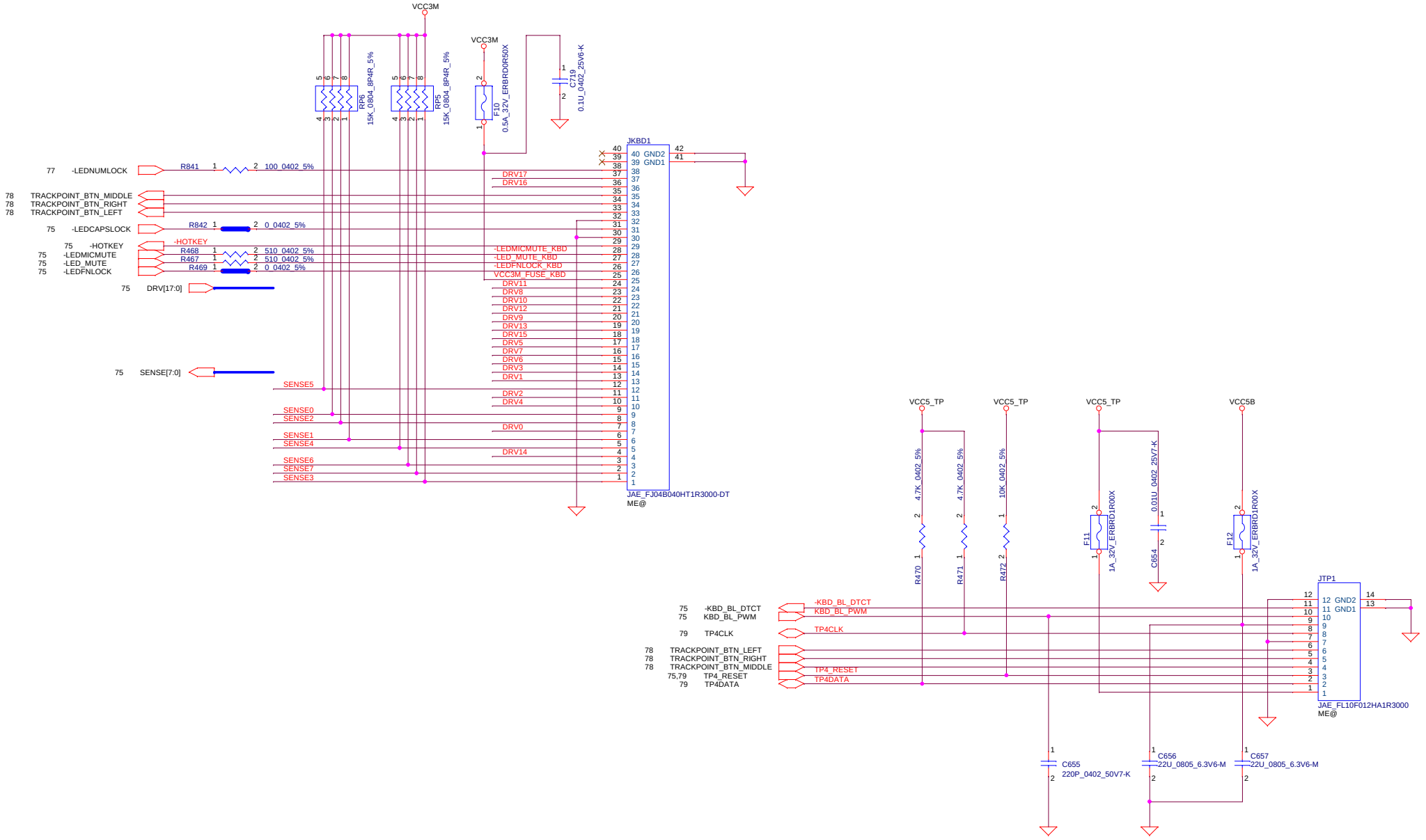
Title: MEC1653L(3/3)

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 77 of 111



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Issued Date	2015/07/16	Deciphered Date	2016/01/16

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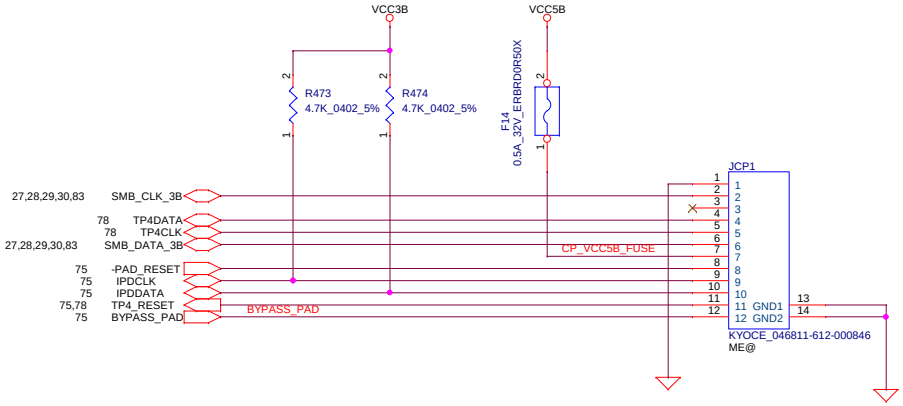
Title: **KEYBOARD CONNECTOR**

Size: Custom	Document Number: PAYTON	Rev: 0.1
Date: Wednesday, December 07, 2016	Sheet 78 of 111	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

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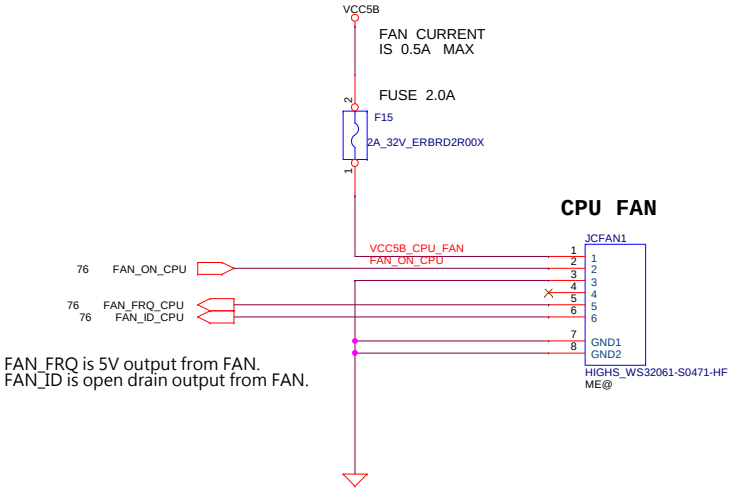
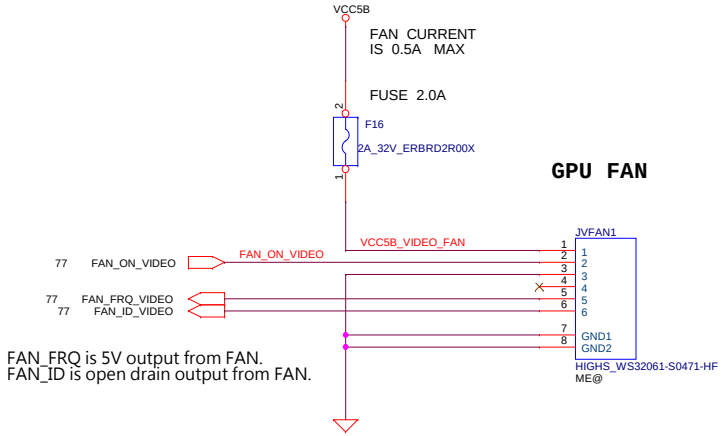
Title: **TOUCH PAD**

Size	Document Number	Rev
Custom	PAYTON	0.1

Date: Wednesday, December 07, 2016 Sheet 79 of 111





Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

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Title: FAN CONNECTOR

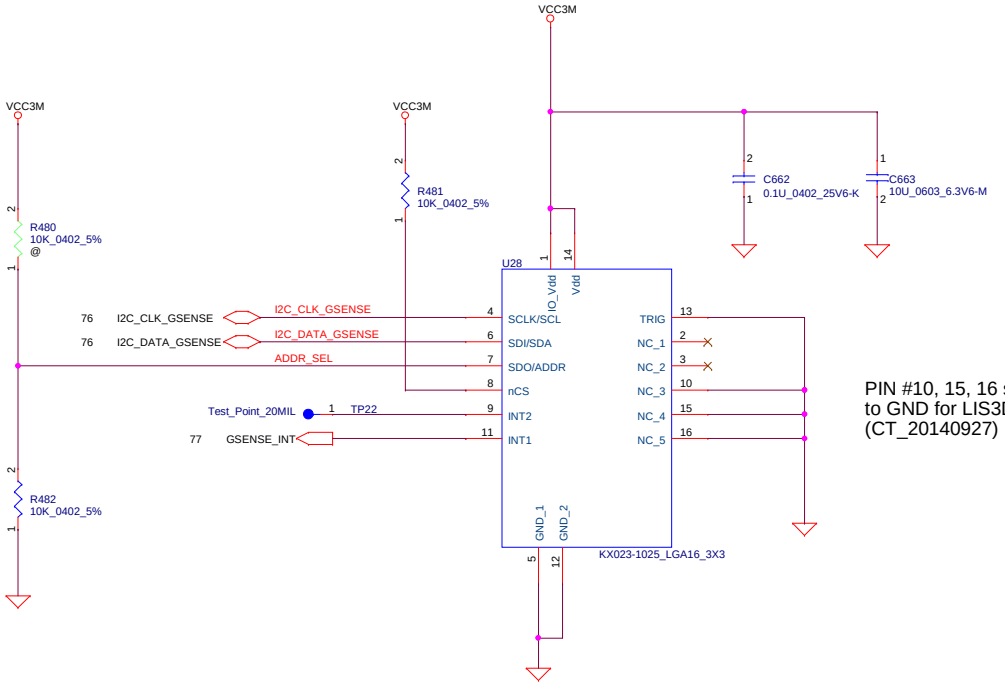
Size: Custom	Document Number: PAYTON	Rev: 0.1
Date: Wednesday, December 07, 2016	Sheet 80 of 111	

TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

TABLE

P/N	ADDR_SEL	Address
LIS3DH	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)



PIN #10, 15, 16 should be connected to GND for LIS3DH.
(CT_20140927)

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Issued Date	2015/07/16	Deciphered Date	2016/01/16

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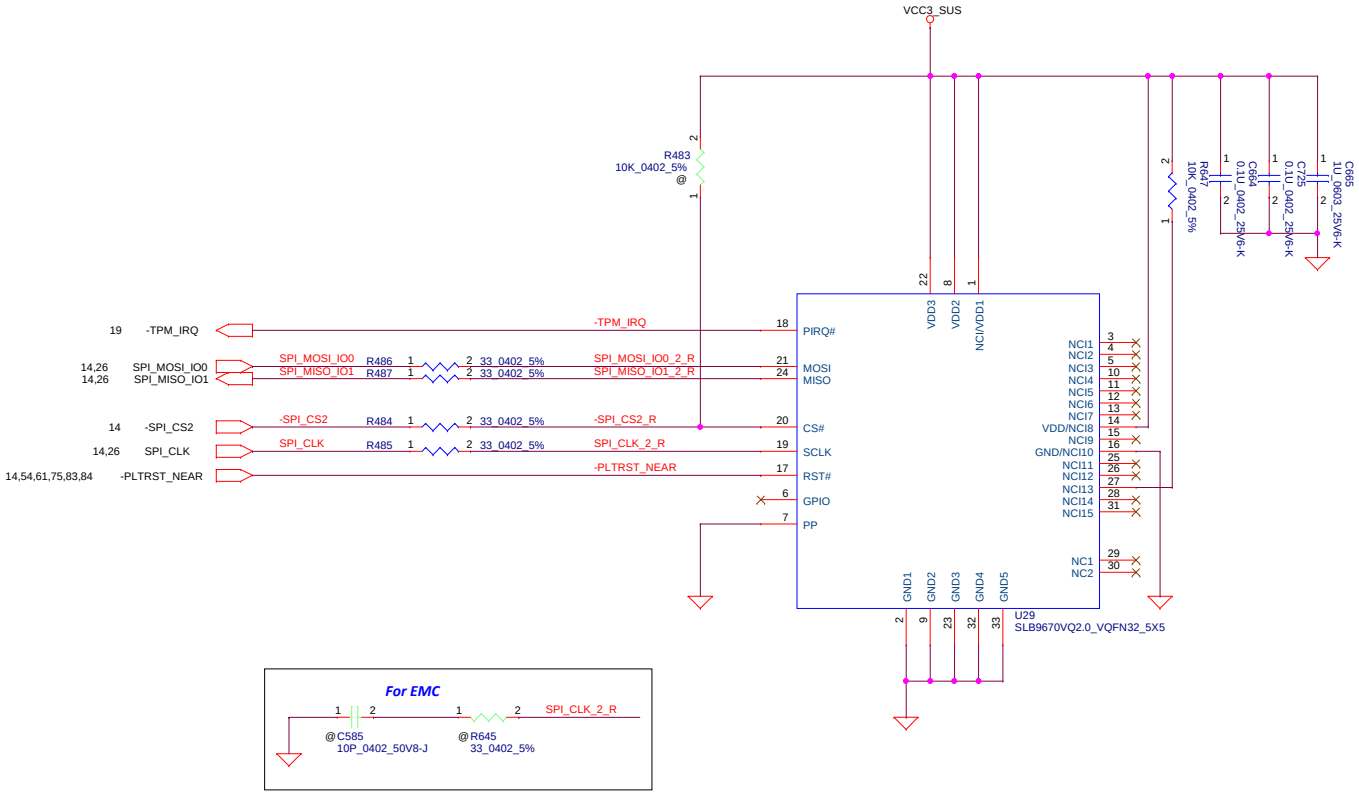
Title: **G-SENSOR**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 81 of 111



TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0	ST ST33HTPH2E32AAE6
1	VDD	VDD	NIC
2	GND	GND	GND
3	GPIO	NCI	NIC
4	GPIO	NCI	NIC
5	NC	NCI	NIC
6	VNC/GPIO	GPIO	NC
7	GPIO/VDD	PP	PP
8	VDD	VDD	NIC
9	GND	GND	NIC
10	VNC	NCI	NIC
11	NC	NCI	NIC
12	NC	NCI	NIC
13	VNC/GPIO	NCI	NIC
14	VDD	NCI/VDD	NIC
15	NC	NCI	NIC
16	GND	NCI/GND	NIC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#
21	MOSI	MOSI	MOSI
22	VDD	VDD	VPS
23	GND	GND	NIC
24	MISO	MISO	MISO
25	NC	NCI	NIC
26	NC	NCI	NIC
27	NC	NCI	NIC
28	NC	NCI	NIC
29	VNC/GPIO	NC	NIC
30	VNC/GPIO	NC	NIC
31	VNC	NCI	NIC
32	GND	GND	NIC

Infineon NCI : Not Connected Internally
ST NIC : Not Internally connected

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Title: TPM

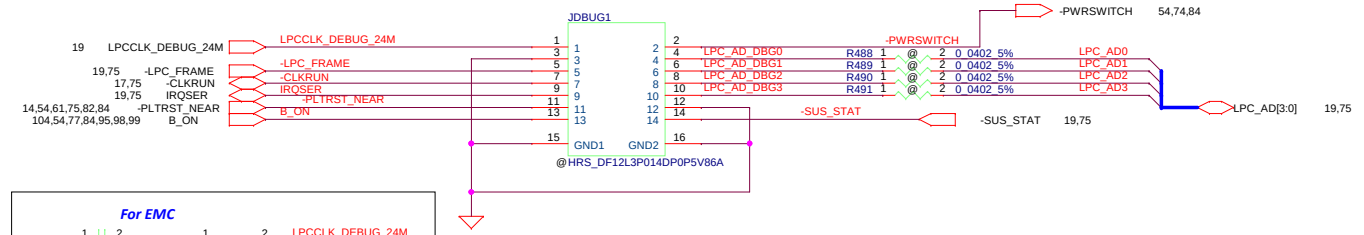
Size: Custom | Document Number: PAYTON | Rev: 0.1

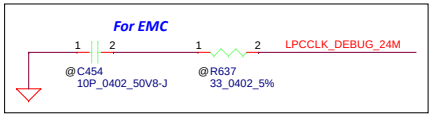
Date: Wednesday, December 07, 2016 | Sheet 82 of 111

LPC Debug Port

	ENABLE	DISABLE
J30	ASM	NO_ASM
R488	ASM	NO_ASM
R489	ASM	NO_ASM
R490	ASM	NO_ASM
R491	ASM	NO_ASM

LOGIC



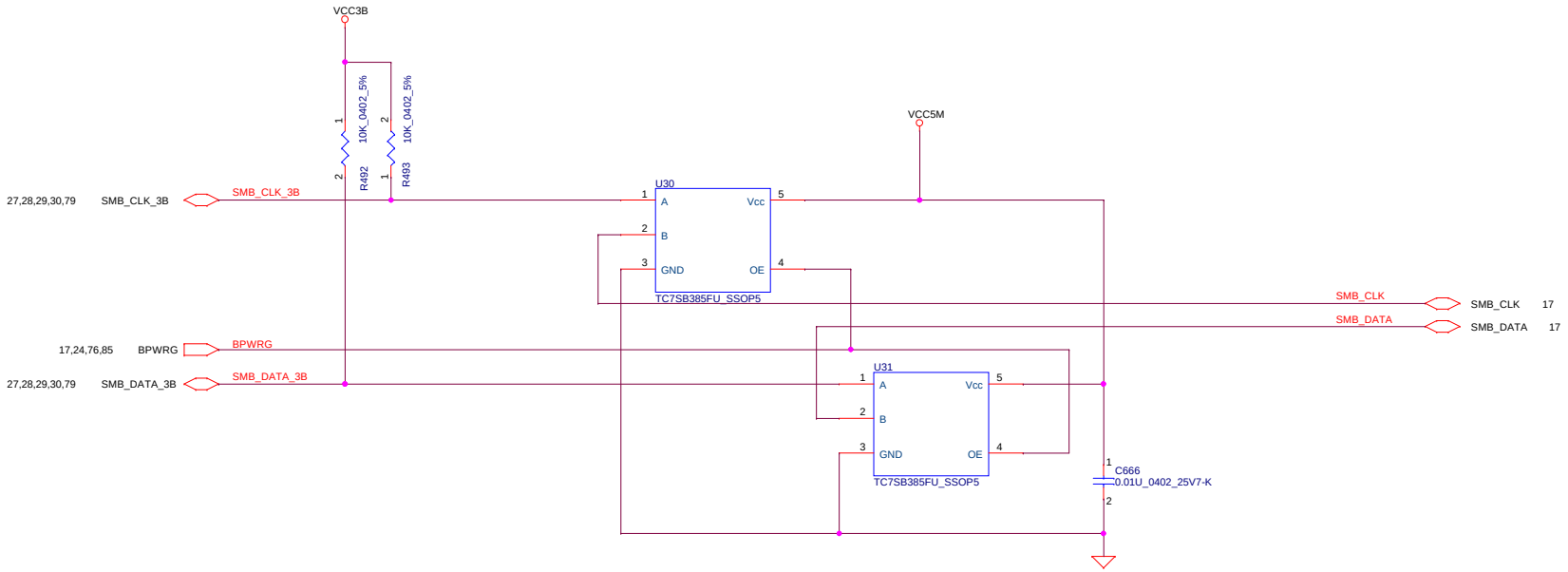


JTAG DEBUG CONN FOR EC
PAYTON PRE DV ONLY

Page : 77
JTAG Port Option (JTAG_RST#)
Set to High : Enable
Set to Low : Disable

JTAG can work in MHz order

DO NOT PLACE UNDER WLAN



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Issued Date	2015/07/16	Deciphered Date	2016/01/16

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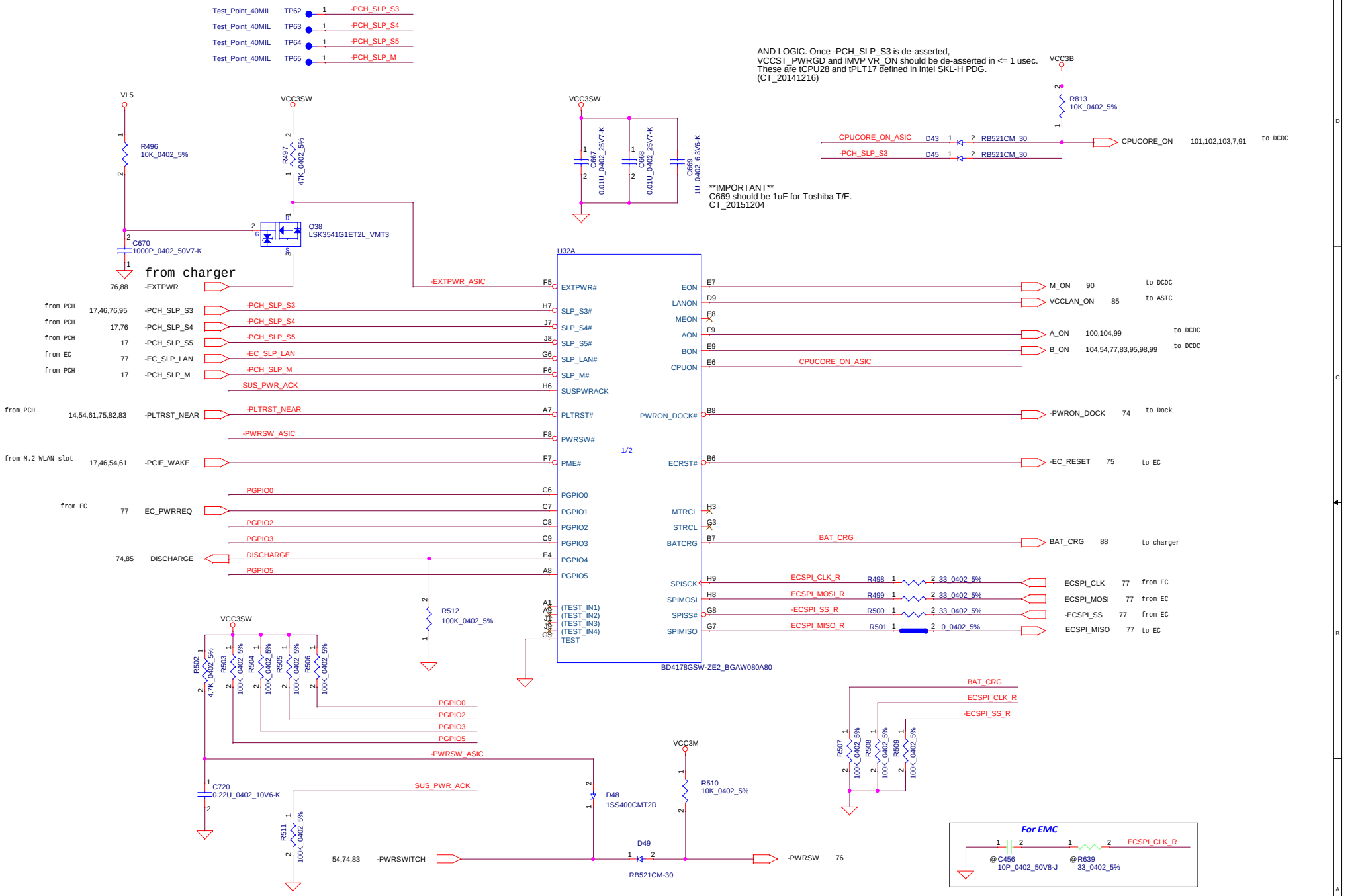
Title: **EEPROM/SMBUS SW**

Size: Custom | Document Number: PAYTON | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 83 of 111



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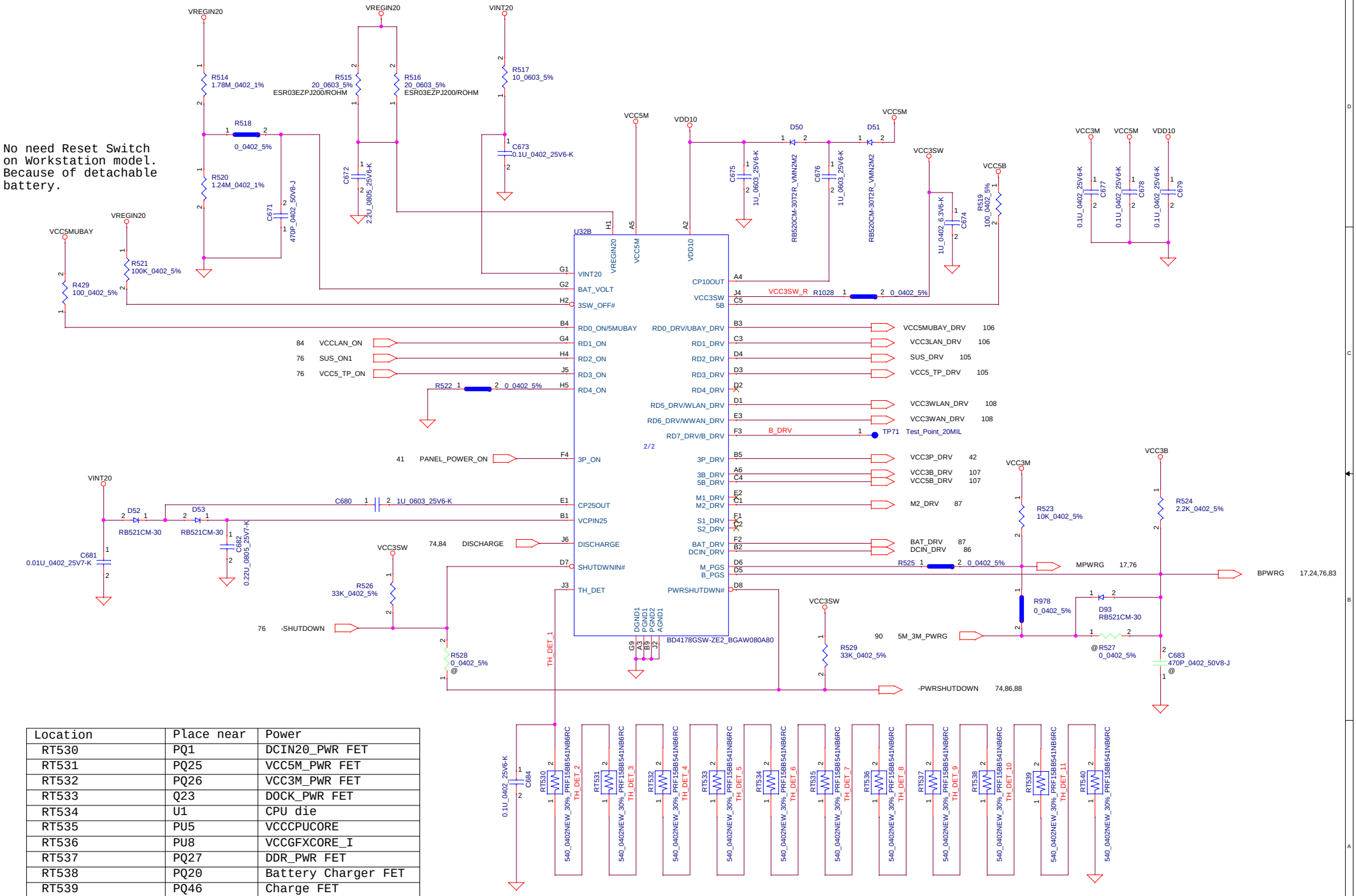
Title: THINK ENGINE 2(1/2)

Size: Custom	Document Number	Rev: 0.1
Date: Wednesday, December 07, 2016	Sheet 84 of 111	



Location	Place near	Power
RT530	PQ1	DCIN20_PWR FET
RT531	PQ25	VCC5M_PWR FET
RT532	PQ26	VCC3M_PWR FET
RT533	Q23	DOCK_PWR FET
RT534	U1	CPU die
RT535	PU5	VCCCPUCORE
RT536	PU8	VCCGFXCORE_I
RT537	PQ27	DDR_PWR FET
RT538	PQ20	Battery Charger FET
RT539	PQ46	Charge FET
RT540	PQ10	M_BAT_PWR FET
PRT1(BAT_FET_HOT)	PQ11	BAT_IN

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Issued Date	2015/07/16	Deciphered Date	2016/01/16

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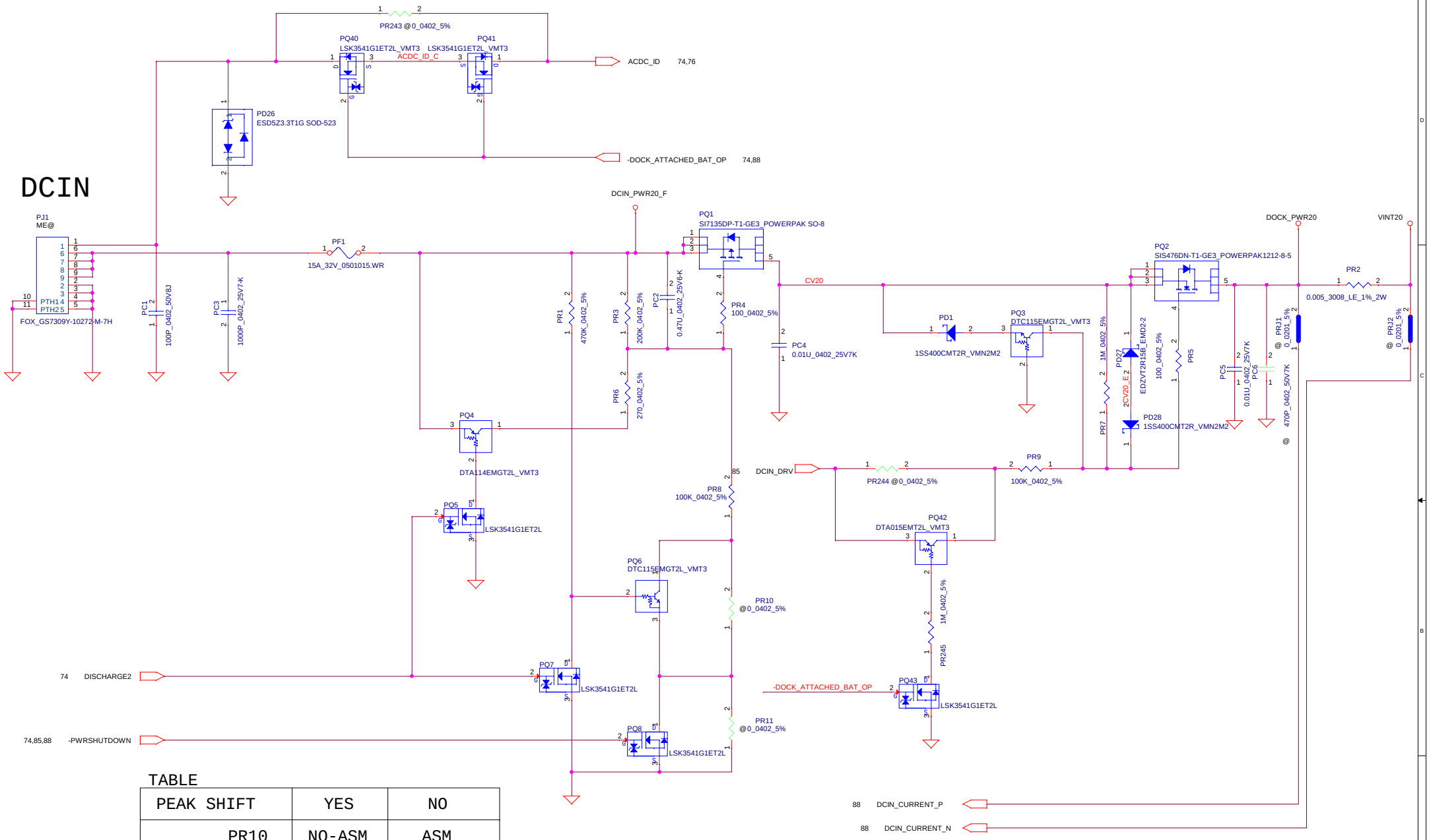
Title: *THINK ENGINE 2(2/2)*

LCFC

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 07, 2016 Sheet 85 of 111



TABLE

PEAK SHIFT	YES	NO
PR10	NO-ASM	ASM
PR1	ASM	NO-ASM
PQ6	ASM	NO-ASM
PQ7	ASM	NO-ASM

LOGIC

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

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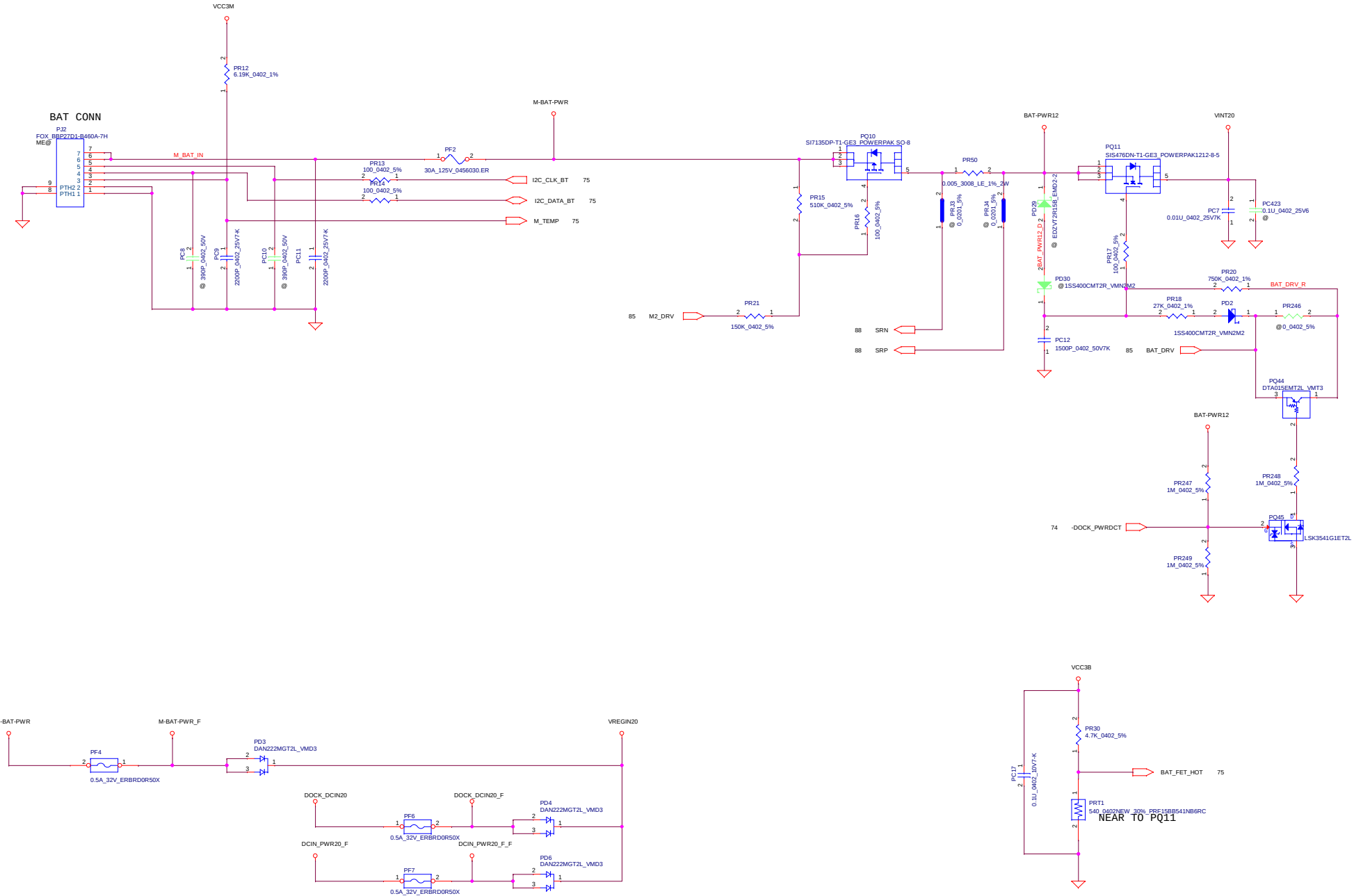
Title: **DC-IN**

Size: Custom | Document Number: **Payton17** | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 86 of 111



Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

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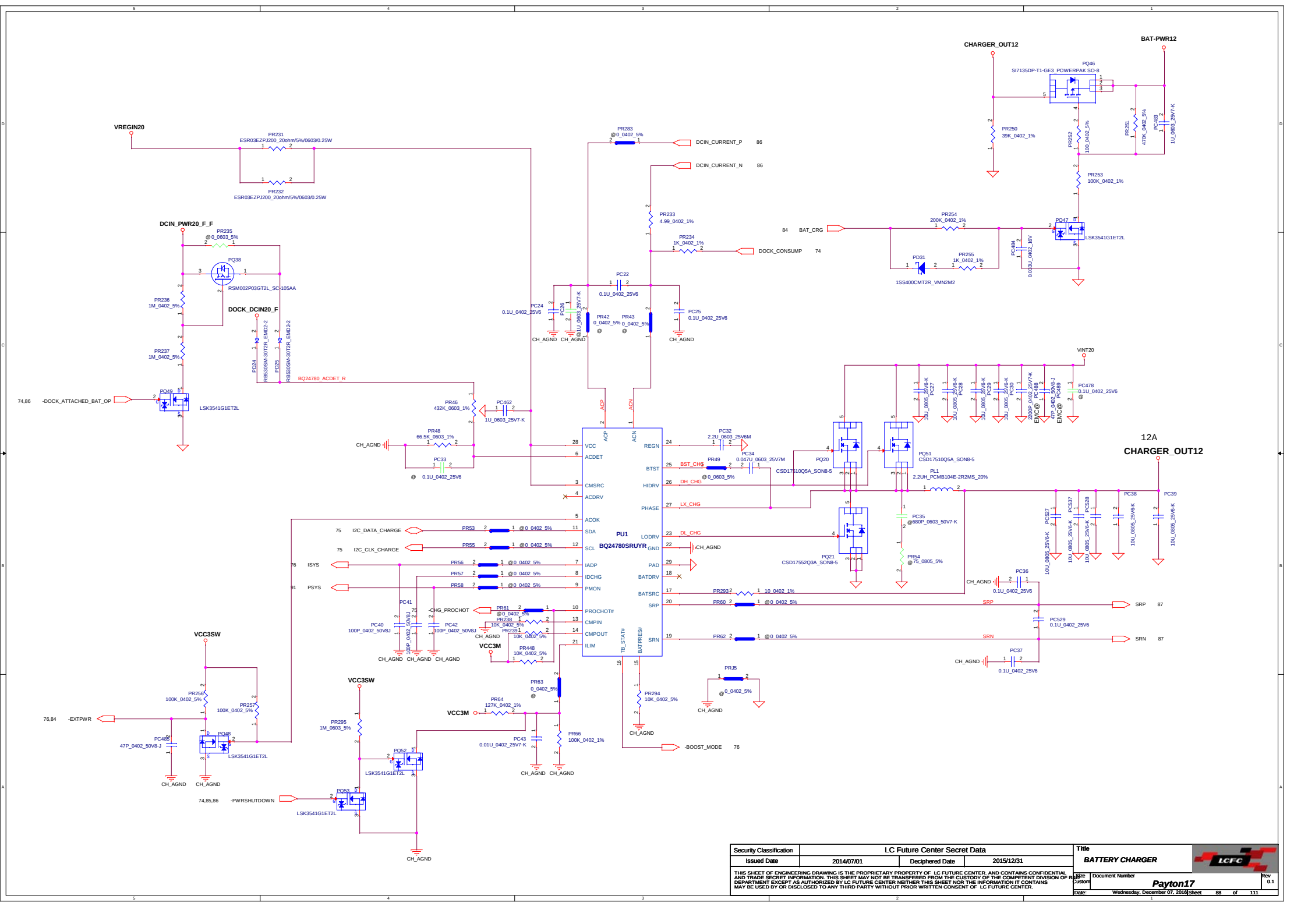
Title: **BATTERY INPUT**

Size: Custom	Document Number: Payton17	Rev: 0.1
Date: Wednesday, December 07, 2016	Sheet 87 of 111	



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Title: **BATTERY CHARGER**

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Date: Wednesday, December 07, 2016 Sheet 88 of 111

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Title: ***BLANK***

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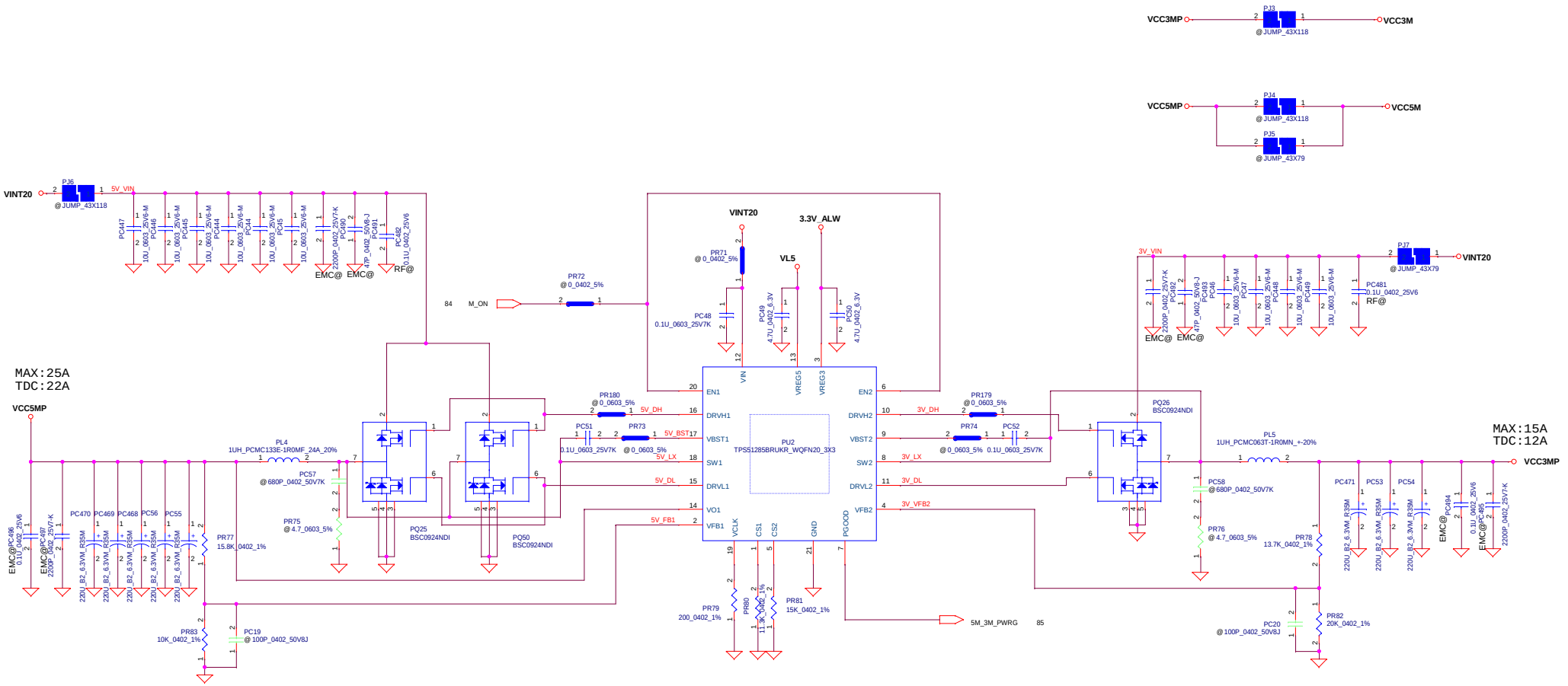
Custom	***Payton17***	0.1

Date: Wednesday, December 07, 2016 Sheet 89 of 111



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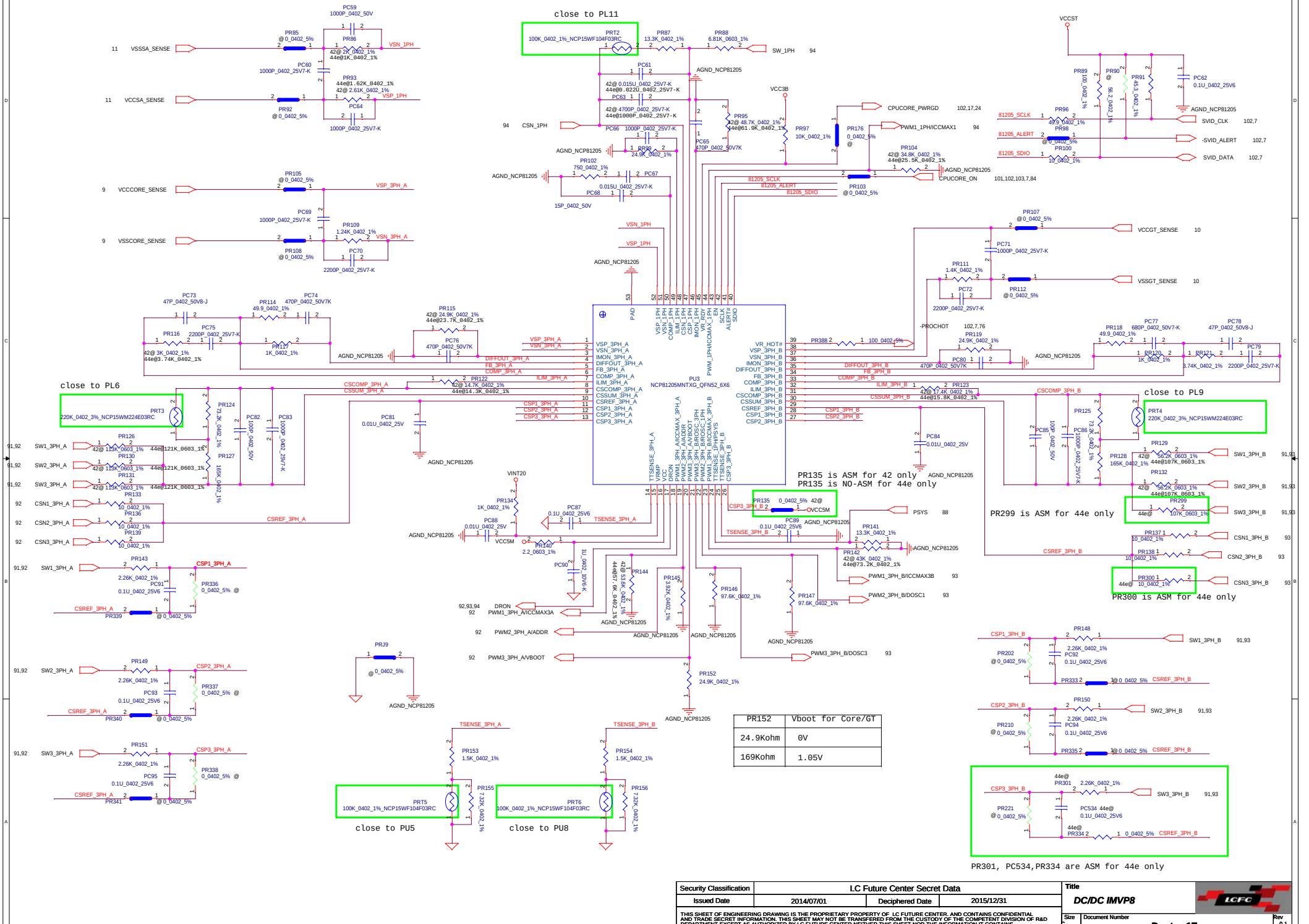
Title: DC/DC VCC5M/VCC3M

Size	Document Number	Rev
C	Payton17	0.1

Date: Wednesday, December 07, 2016 Sheet 90 of 111


close to PL11
close to PL6
close to PL9
close to PU5
close to PU8
PR135 is ASM for 42 only
PR135 is NO-ASM for 44e only
PR299 is ASM for 44e only
PR300 is ASM for 44e only
PR301, PC534,PR334 are ASM for 44e only
PR152 | Vboot for Core/GT
24.9Kohm | 0V
169Kohm | 1.05V
Security Classification | LC Future Center Secret Data
Issued Date | 2014/07/01 | Deciphered Date | 2015/12/31
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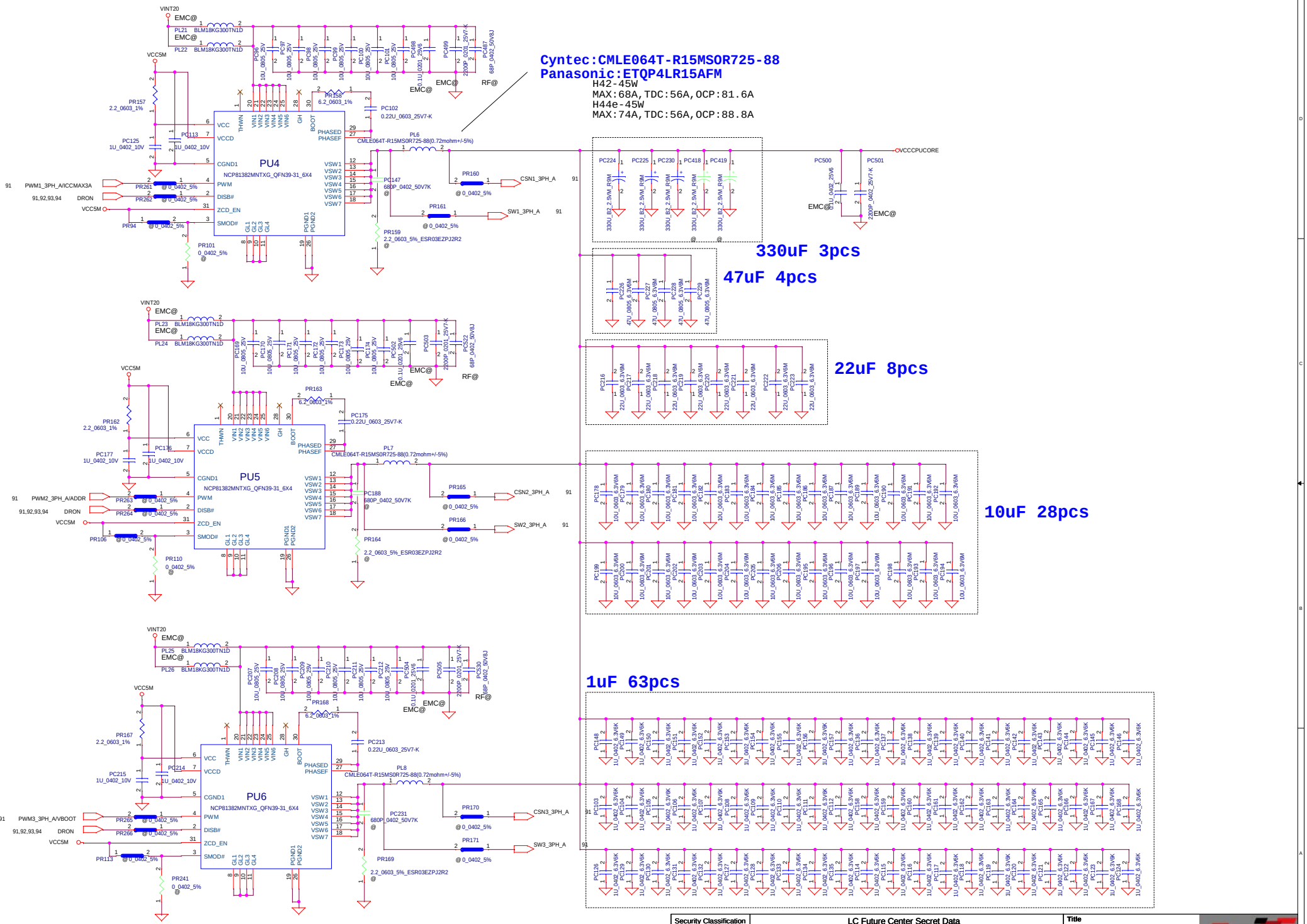
Title
DC/DC IMVP8
Size C
Document Number
Payton17
Rev 0.1
Date: Wednesday, December 07, 2016
Sheet 91 of 111



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Title: DC/DC VCCPUCORE

Size: C | Document Number: Payton17 | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 92 of 111

H42-45W
MAX:55A,TDC:39A,OCP:66A
H44e-45W
MAX:94A,TDC:80A,OCP:112.8A

PC337 and PC338 are ASM for 44e only

330uF 4pcs

47uF 6pcs

22uF 8pcs

10uF 35pcs

1uF 68pcs

VCCGFXCORE_I Phase3 are POP for 44e only

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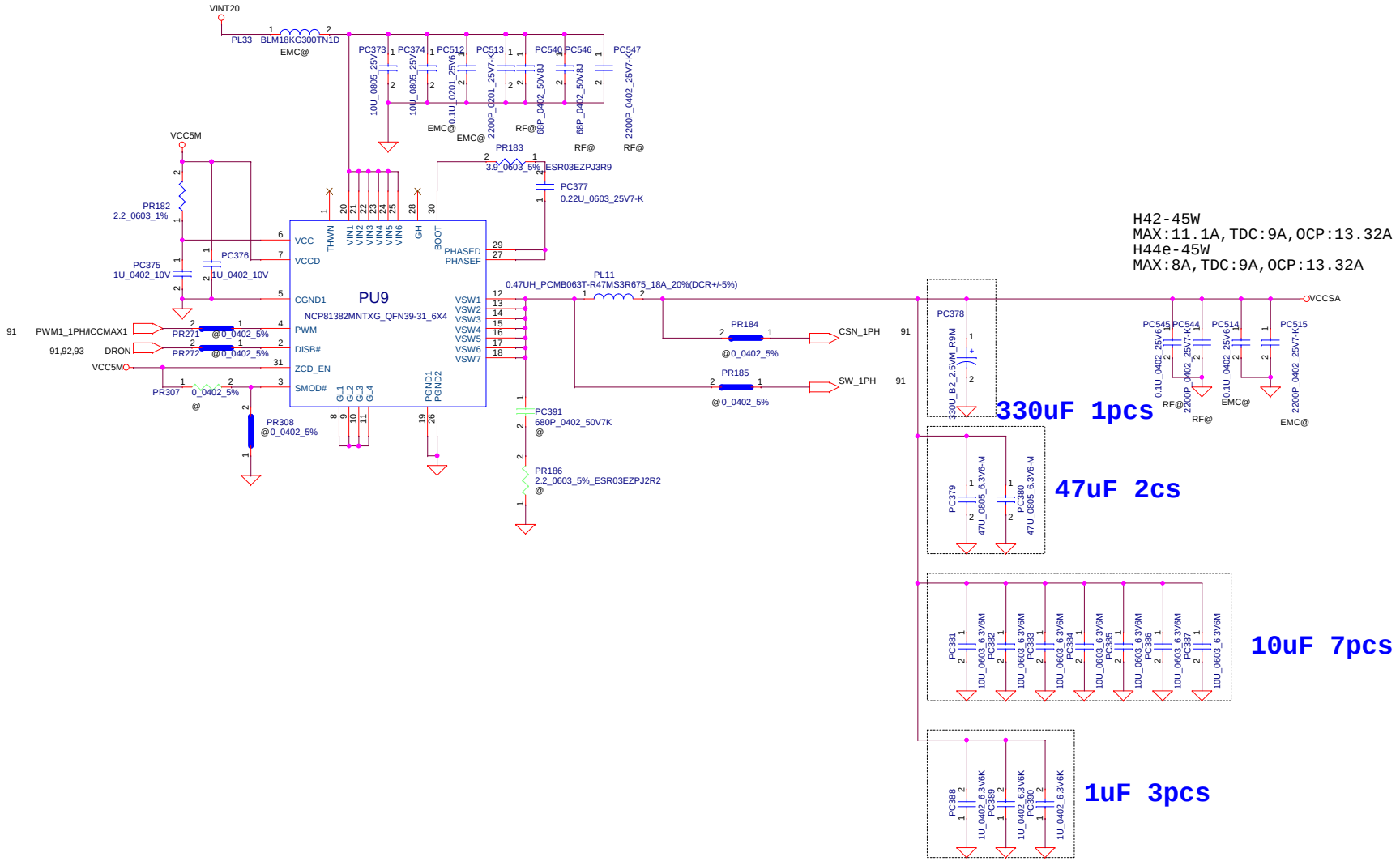
Title: DC/DC VCCGFXCORE_I

Size: Custom | Document Number: Payton17 | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 93 of 111



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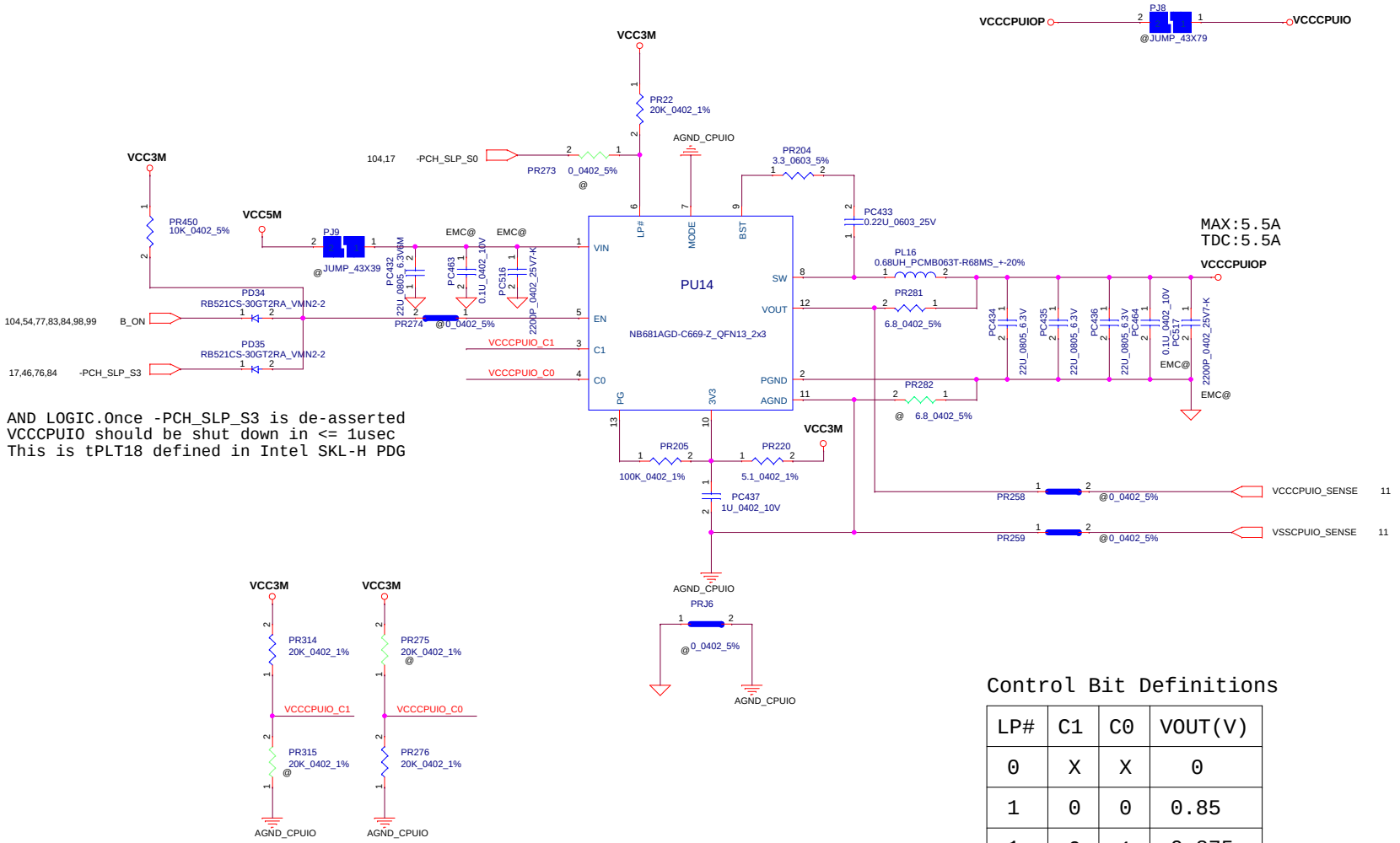
Title: DC/DC VCCSA

Size: Custom | Document Number: Payton17 | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 94 of 111



AND LOGIC.Once -PCH_SLP_S3 is de-asserted
VCCCPUIO should be shut down in <= 1usec
This is tPLT18 defined in Intel SKL-H PDG

Control Bit Definitions

LP#	C1	C0	VOUT(V)
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

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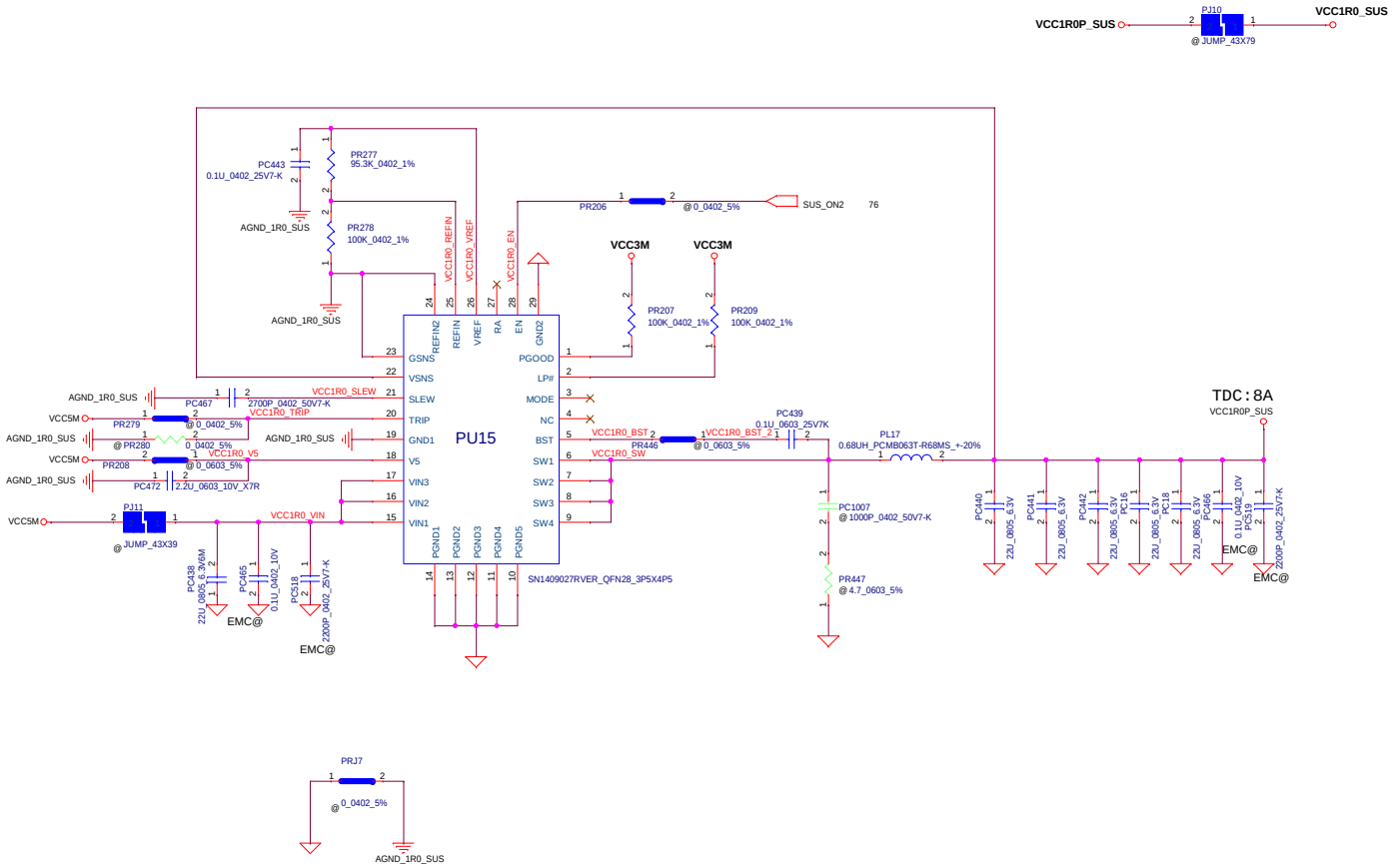
Title: DC/DC VCCCPUIO

Size: Custom | Document Number: Payton17 | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 95 of 111



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Title: **DC/DC VCC1R0_SUS**

Size	Document Number	Rev
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Date: Wednesday, December 07, 2016 Sheet 96 of 111

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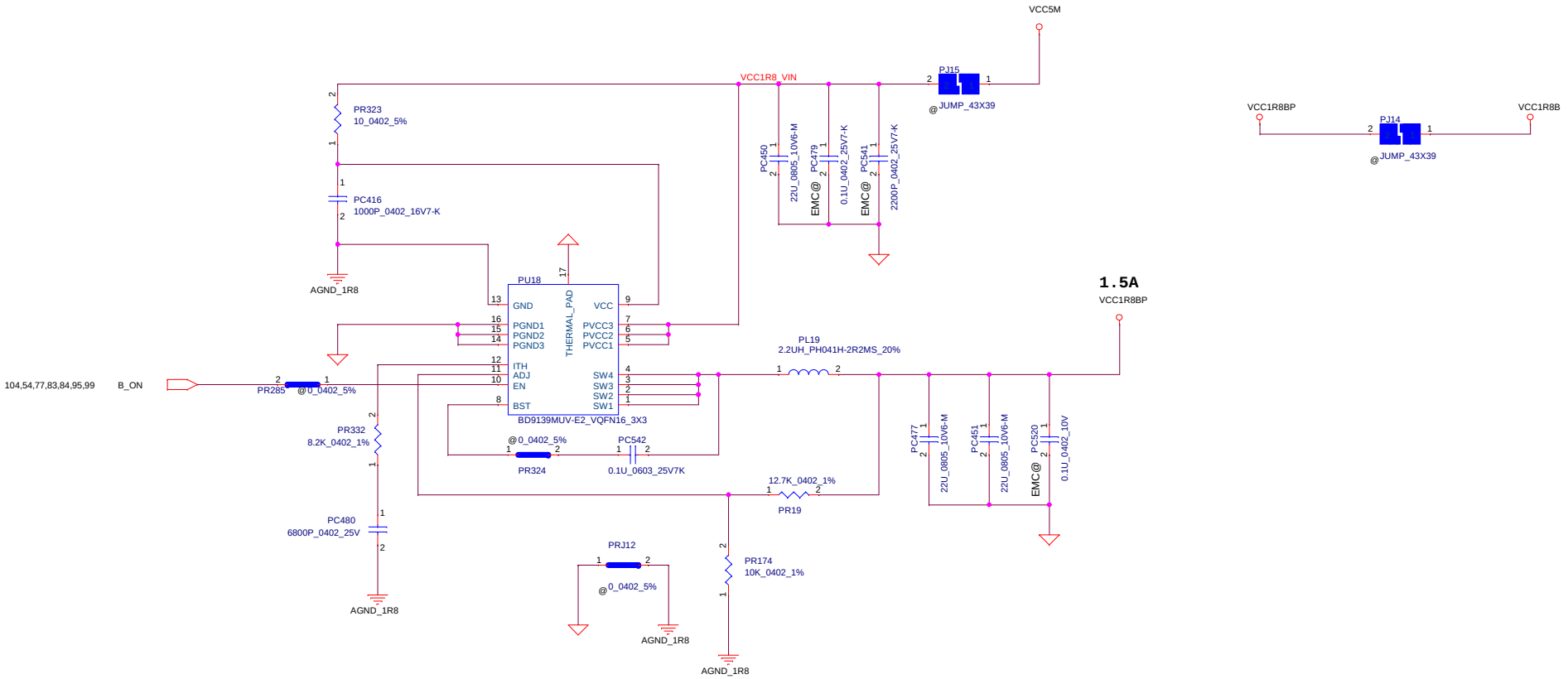
Title: **BLANK**

Size: Custom	Document Number: **Payton17**	Rev: 0.1
Date: Wednesday, December 07, 2016	Sheet 97 of 111	



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Title: DC/DC VCC1R8B

Size: Custom	Document Number: Payton17	Rev: 0.1
Date: Wednesday, December 07, 2016	Sheet 98 of 111	

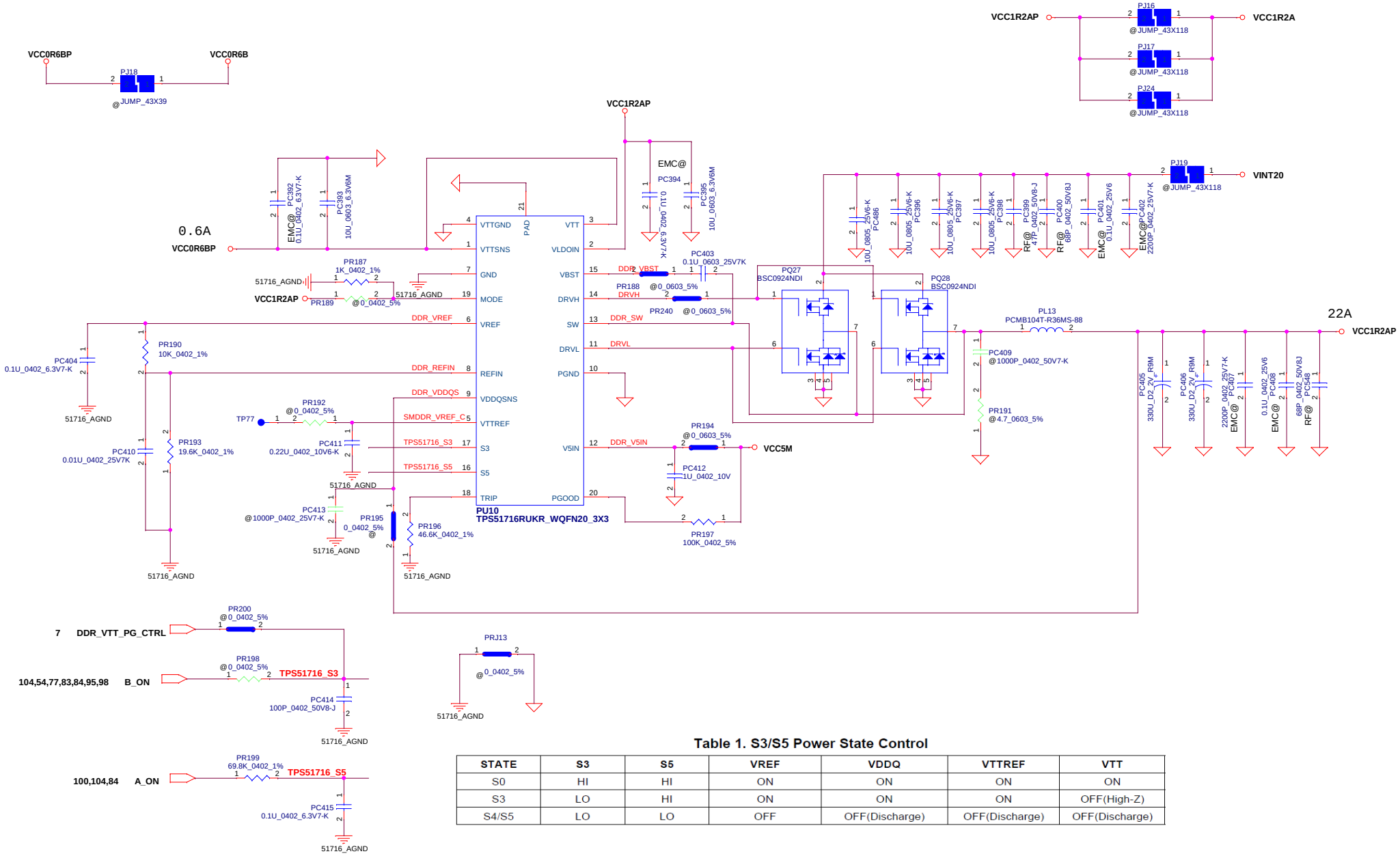

Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

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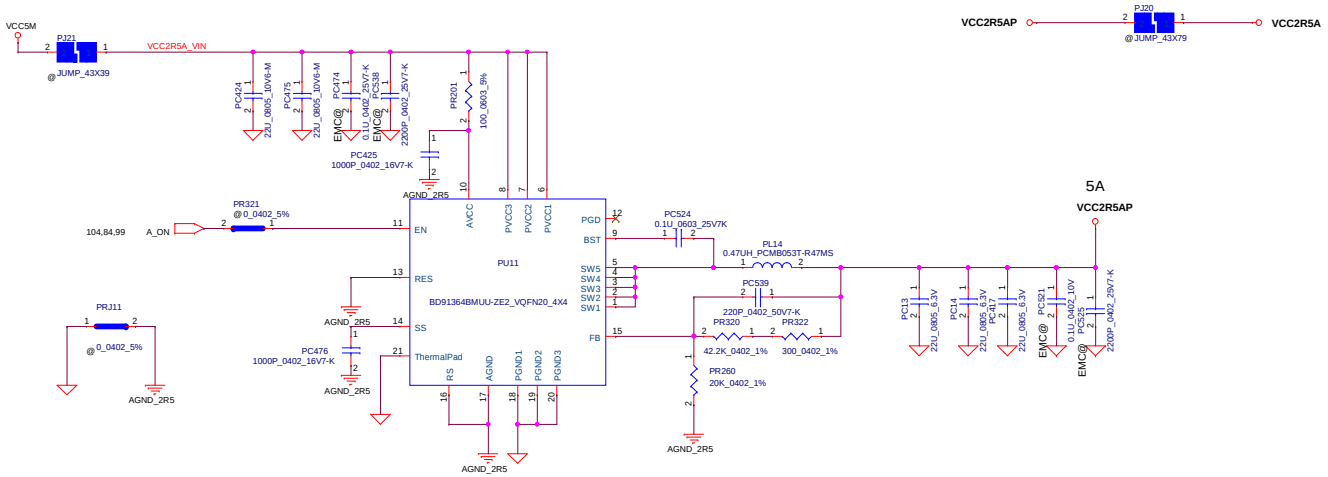
Title: DC/DC VCC1R2A/VCC0R6B

Size: Custom | Document Number: Payton17 | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 99 of 111



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Title: **DC/DC VCC2R5A**

Size	Document Number	Rev
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Date: Wednesday, December 07, 2016 Sheet 100 of 111

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Issued Date	2014/07/01	Deciphered Date	2015/12/31

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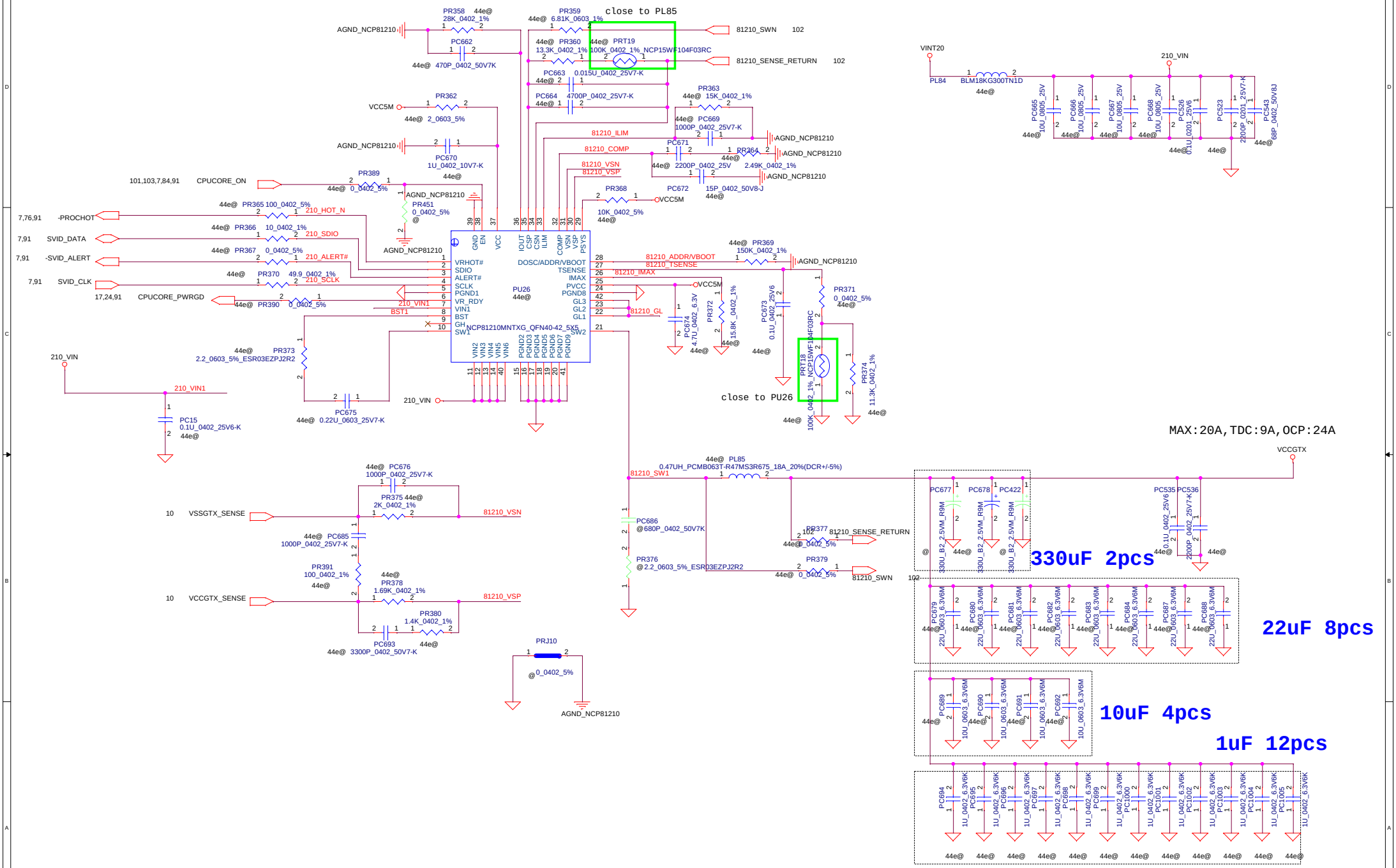
Date: Wednesday, December 07, 2016	Sheet 101 of 111	



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Date: Wednesday, December 07, 2016 | Sheet 102 of 111

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Title: ***BLANK***

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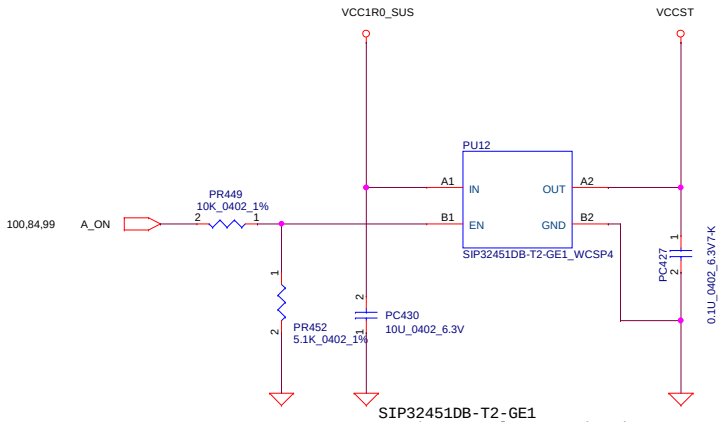
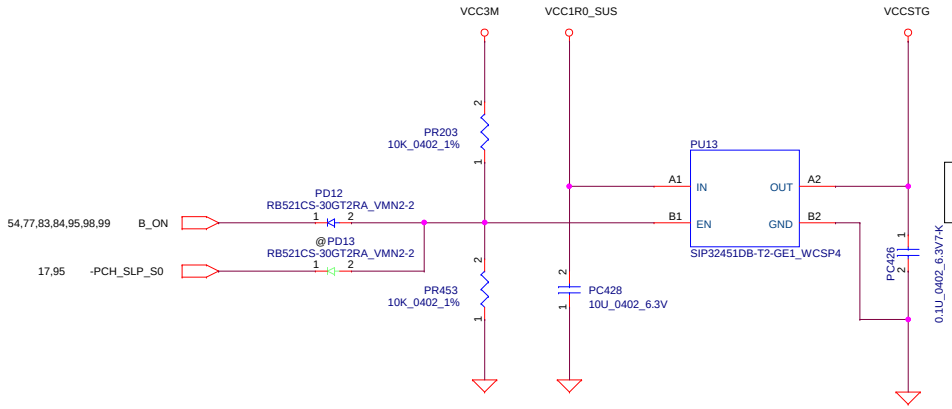
Custom	***Payton17***	0.1

Date: Wednesday, December 07, 2016 Sheet 103 of 111



SIP32451DB-T2-GE1
EN pin Max Voltage Rating is 2.75V



SIP32451DB-T2-GE1
EN pin Max Voltage Rating is 2.75V

Slew Rate=10uS<TR<65us

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Title: LOAD SW VCCST/VCCSTG

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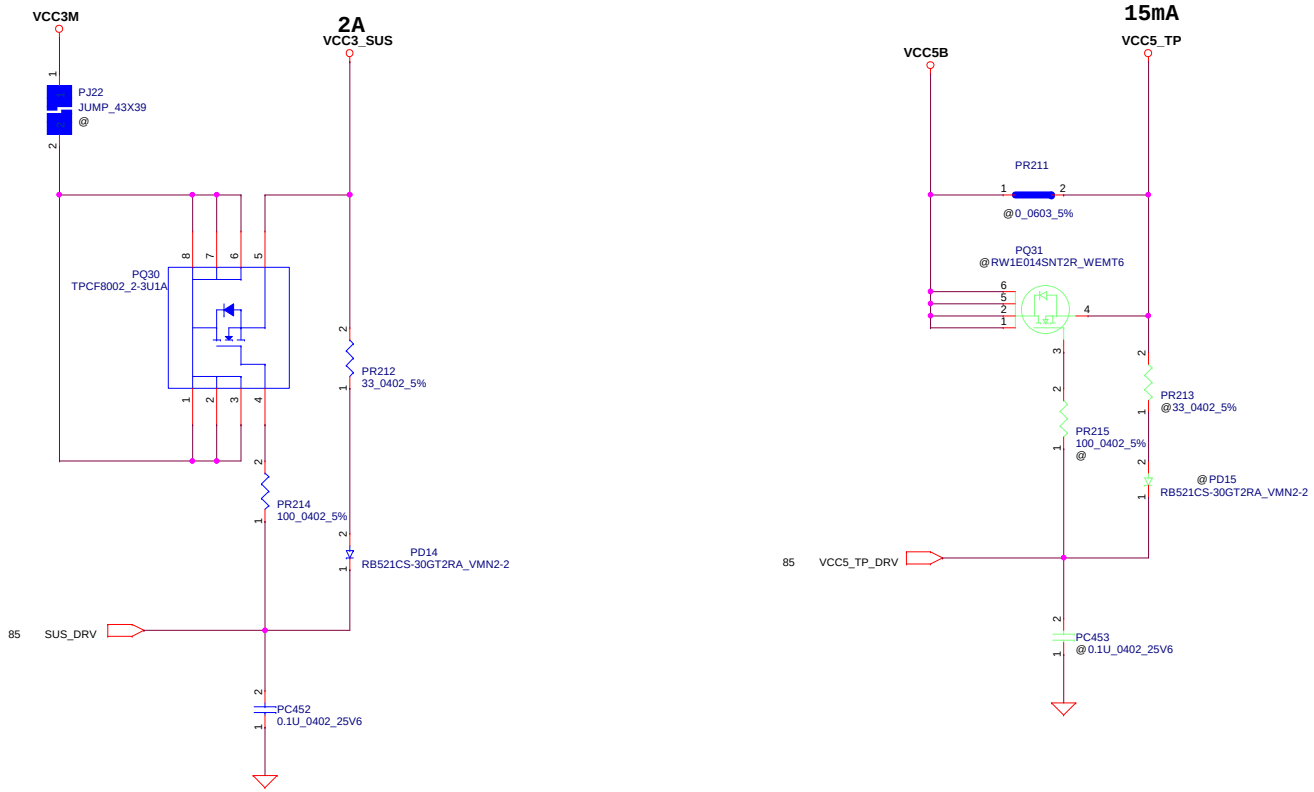
Date: Wednesday, December 07, 2016 | Sheet 104 of 111



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Title: LOAD SW PCH SUS/TRACK POINT

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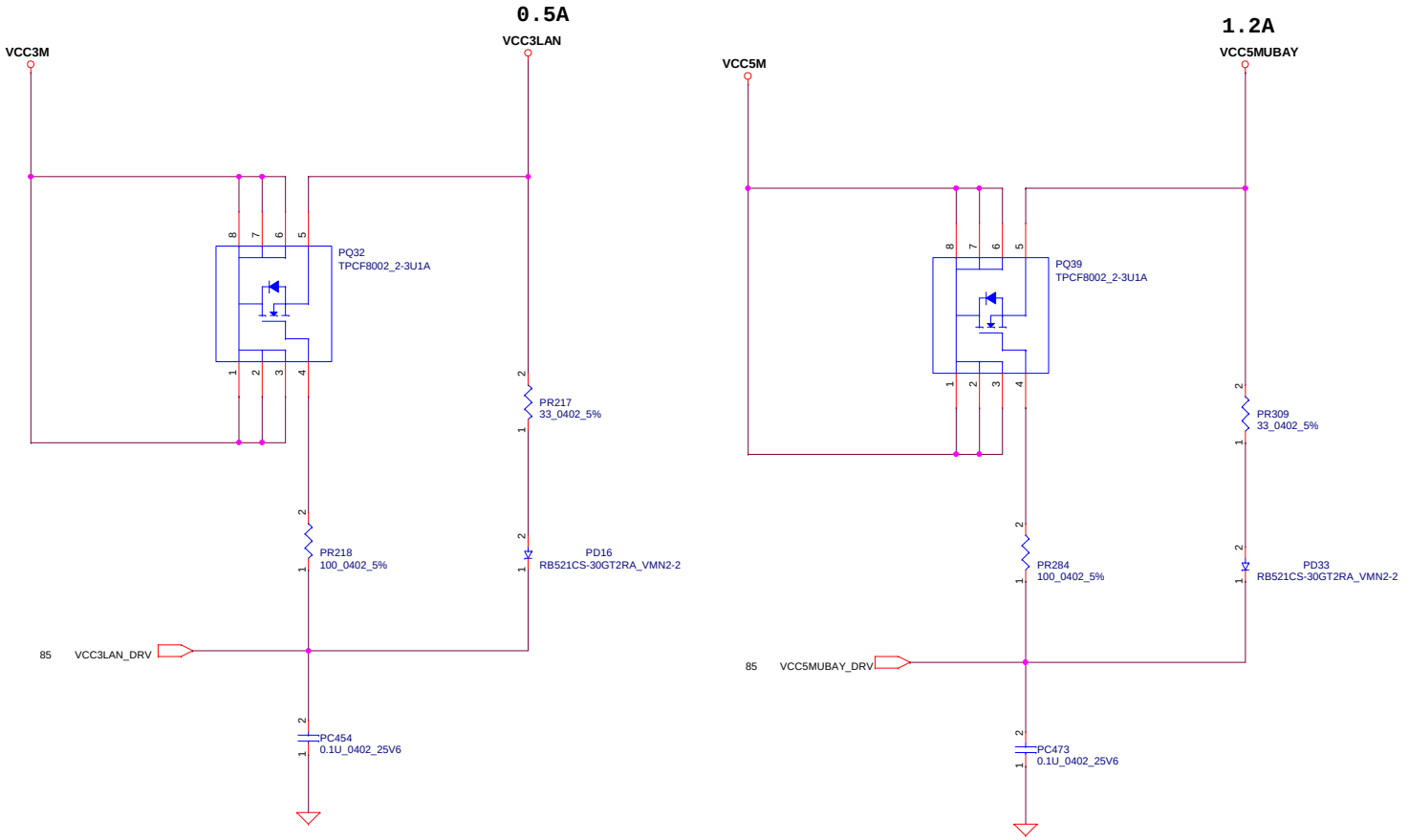
Date: Wednesday, December 07, 2016 | Sheet 105 of 111



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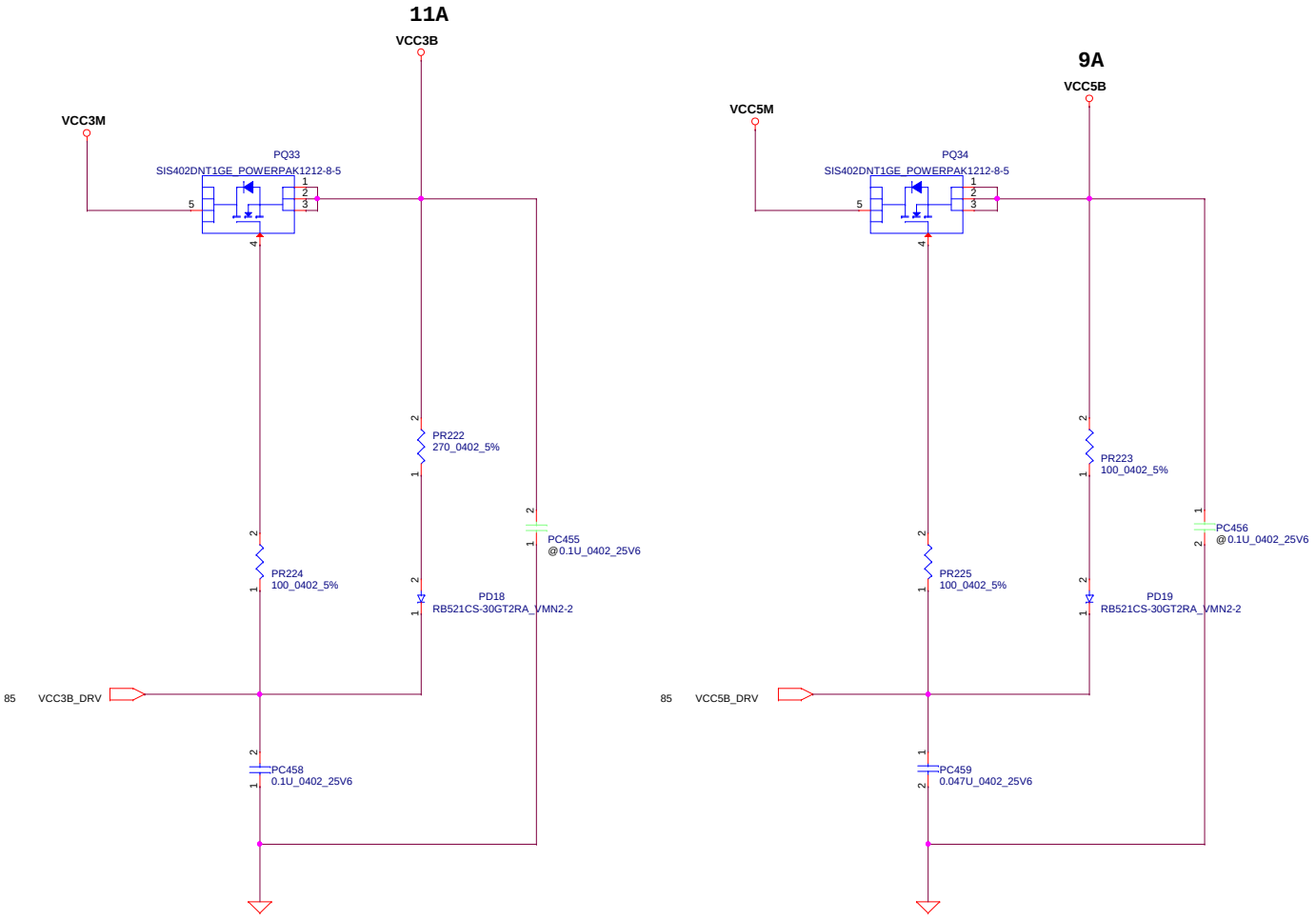
Title: LOAD SW LAN

Size: Custom | Document Number: Payton17 | Rev: 0.1

Date: Wednesday, December 07, 2016 | Sheet 106 of 111



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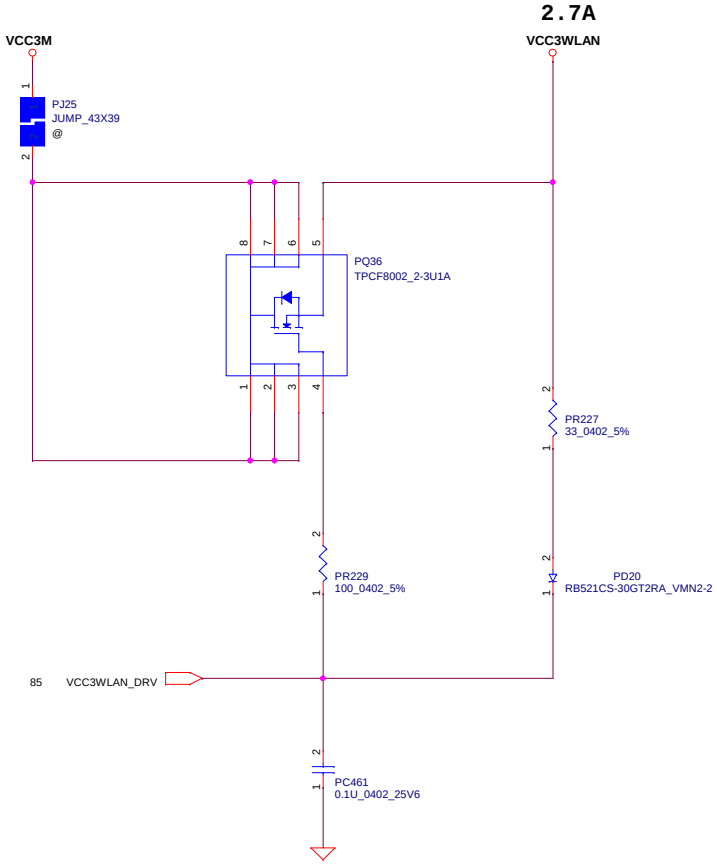
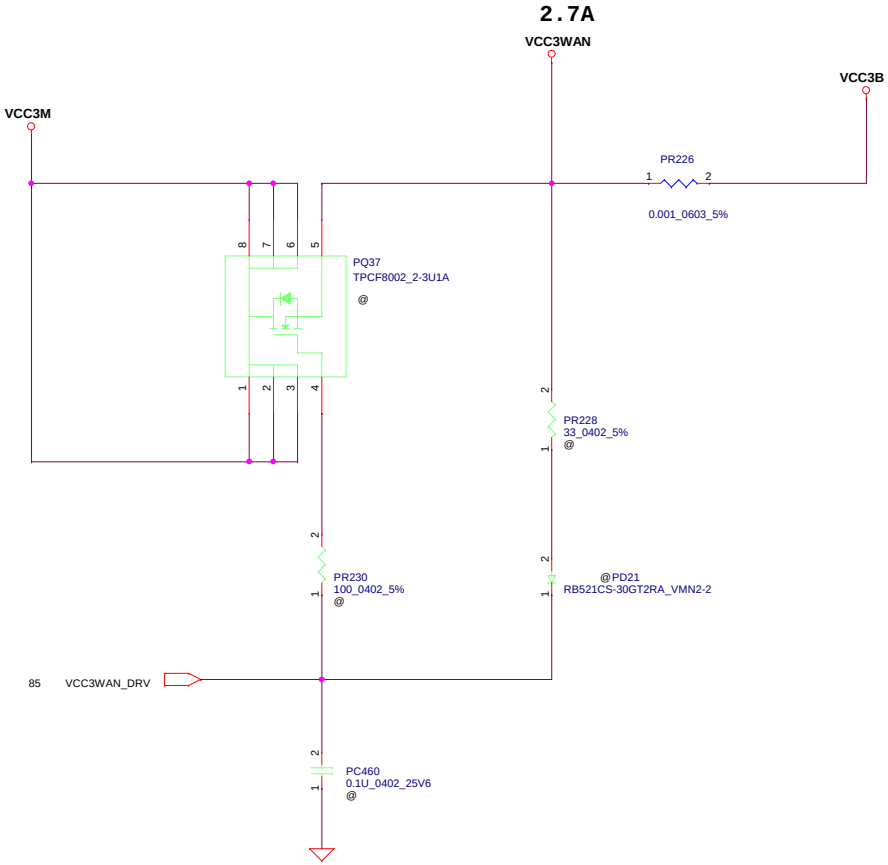
Title: **LOAD SW B**

Size: Custom	Document Number: **Payton17**	Rev: 0.1
Date: Wednesday, December 07, 2016	Sheet 107 of 111	





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Title: **LOAD SW WWAN&WLAN**

Size	Document Number	Rev
Custom	Payton17	0.1

Date: Wednesday, December 07, 2016 Sheet 108 of 111

H15
PAD_C8P0D2P5

H16
PAD_C8P0D2P5

H20
PAD_CT6P0B8P0D2P5

H21
PAD_C8P0D2P5

H1
PAD_C6P0D3P3

H2
PAD_C6P0D3P3

H3
PAD_C6P0D3P3

H4
PAD_C6P0D3P3

H5
PAD_CT4P5B6P0D3P3

H6
PAD_CT4P5B6P0D3P3

H7
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H8
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H9
PAD_C6P0D3P3

H10
PAD_C6P0D3P3

H14
PAD_C8P0D3P3

H11
PAD_C6P0D2P0

H12
PAD_CT6P0D2P0

H23
PAD_C6P0D2P5

H24
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H25
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H26
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H28
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H29
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H31
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H32
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H33
PAD_C2P1D2P1N

H34
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H36
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PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

Security Classification	LC Future Center Secret Data		
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