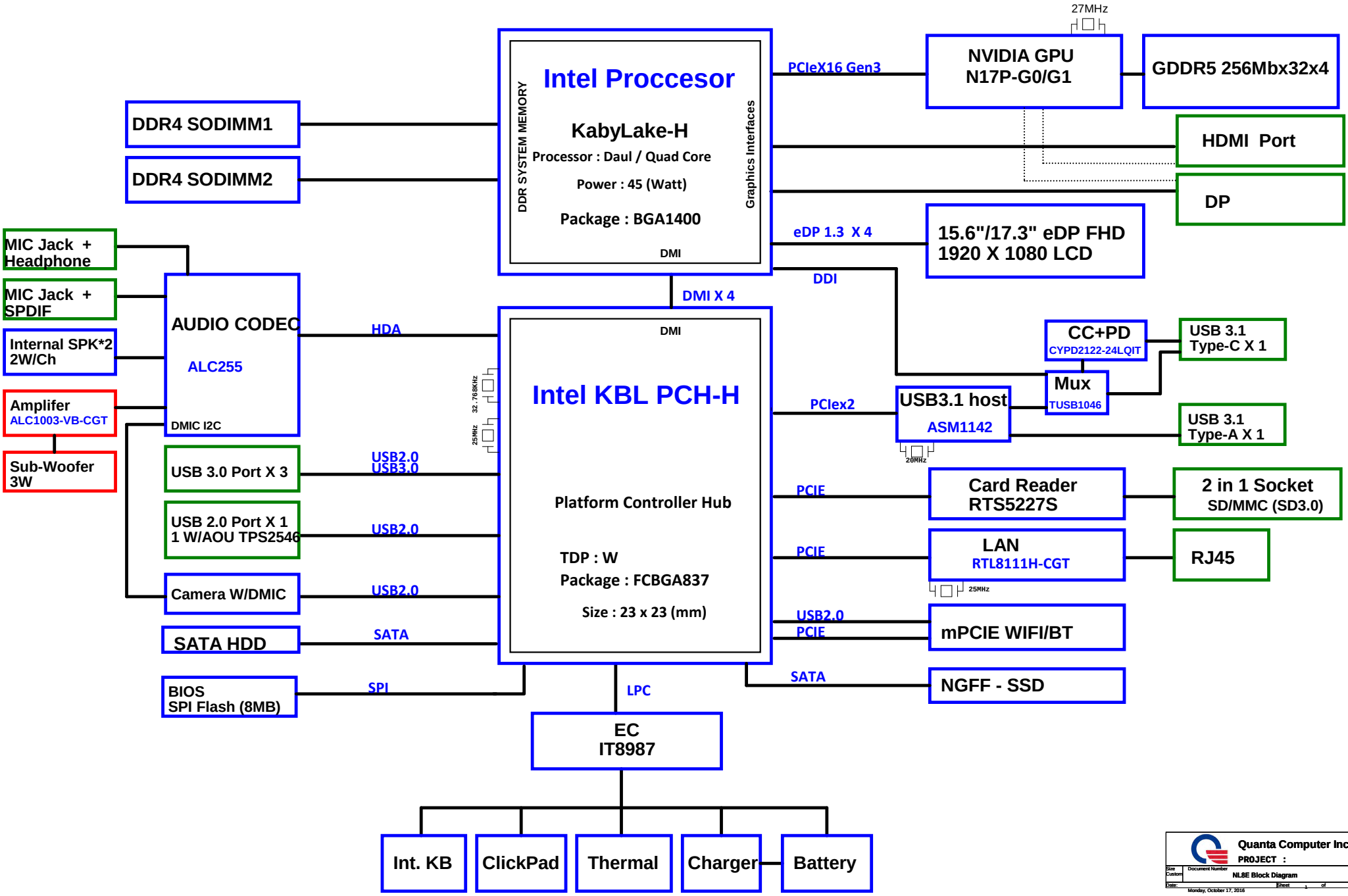
NL8K Block Diagram

01

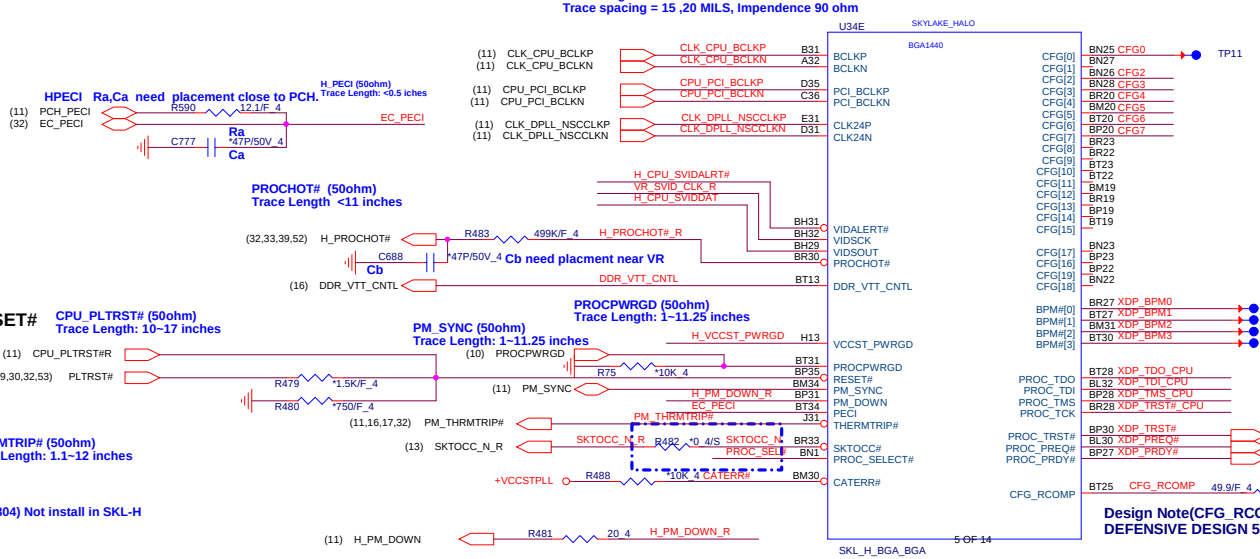


Quanta Computer Inc.
PROJECT :
Size: Custom | Document Number: NL8E Block Diagram | Rev: 1A
Date: Monday, October 17, 2016 | Sheet 1 of 66

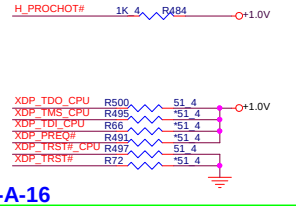
SKYLAKE Processor (CLK,MISC,JTAG)

02

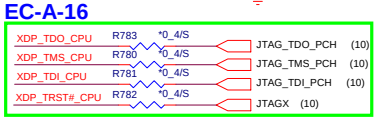
Host CLK:
Trace length < 11000 MILS
Trace spacing = 15 ,20 MILS, Impendence 90 ohm



Processor pull-up (CPU)

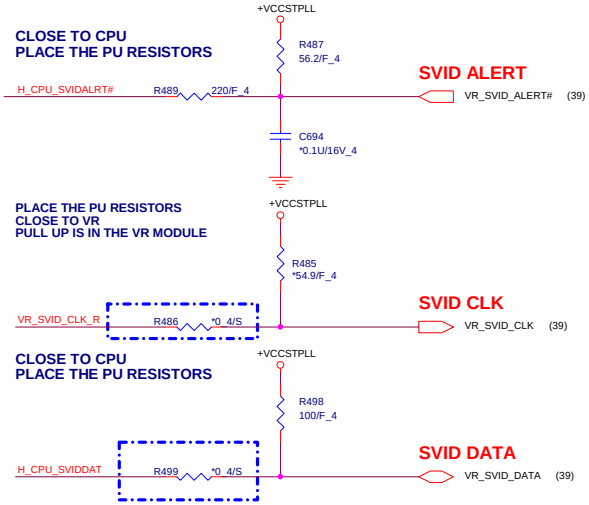


EC-A-16



CPU CORE SVID

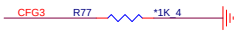
Layout note: need routing together and ALERT need between CLK and DATA.



CFG

0 Enable; SET DFX ENABLED BIT IN DEBUG

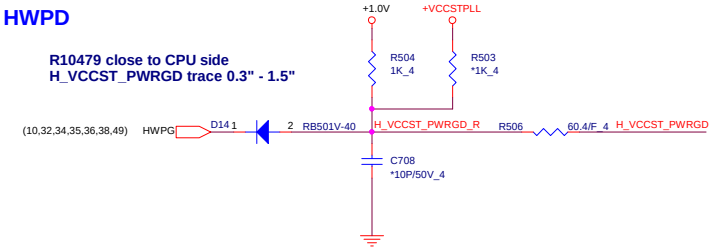
1 , Disable;



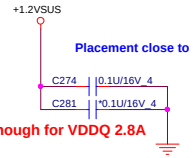
Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OxM board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R83 1K_4
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R507 1K_4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG6 R509 *1K_4 CFG5 R508 *1K_4
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	CFG7 R505 *1K_4

HWPD

R10479 close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



CPU VDDQ



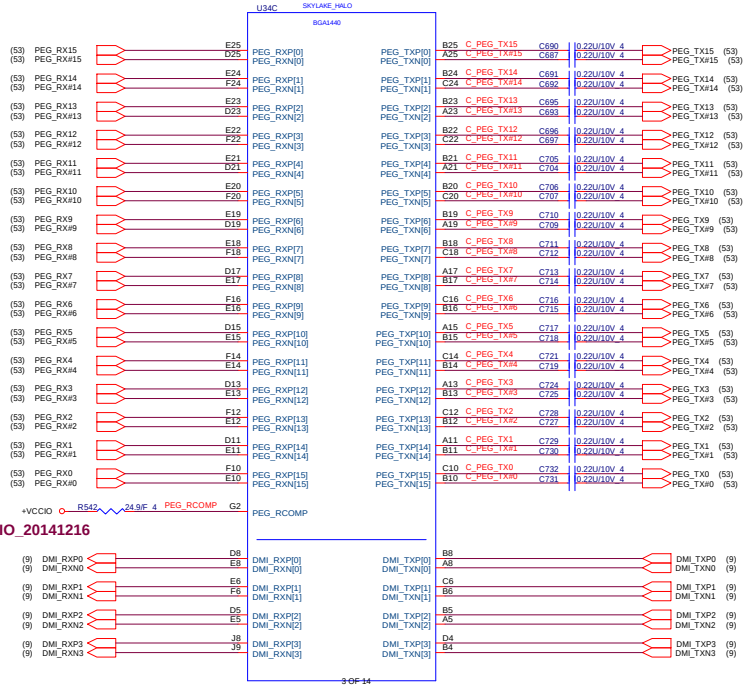
Note: please keep plane is enough for VDDQ 2.8A

Quanta Computer Inc.
PROJECT :

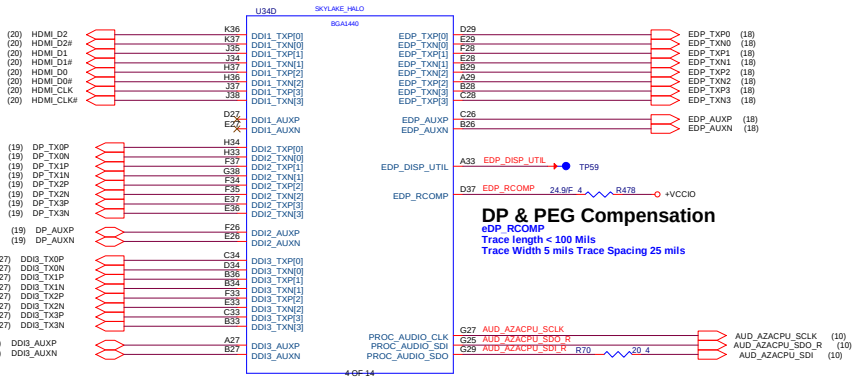
Size	Document Number	Rev
Custom	02 -- SKYPAKE 1/20(eDP/DDI)	1A
Date: Wednesday, October 26, 2016	Sheet 2 of 2	66

SKYLAKE Processor (DMI,PEG,FDI)

03



Change PWR rail from +1.0V to +VCCIO_20141216



HDMI

DP

USB3.1 type-C

DP & PEG Compensation

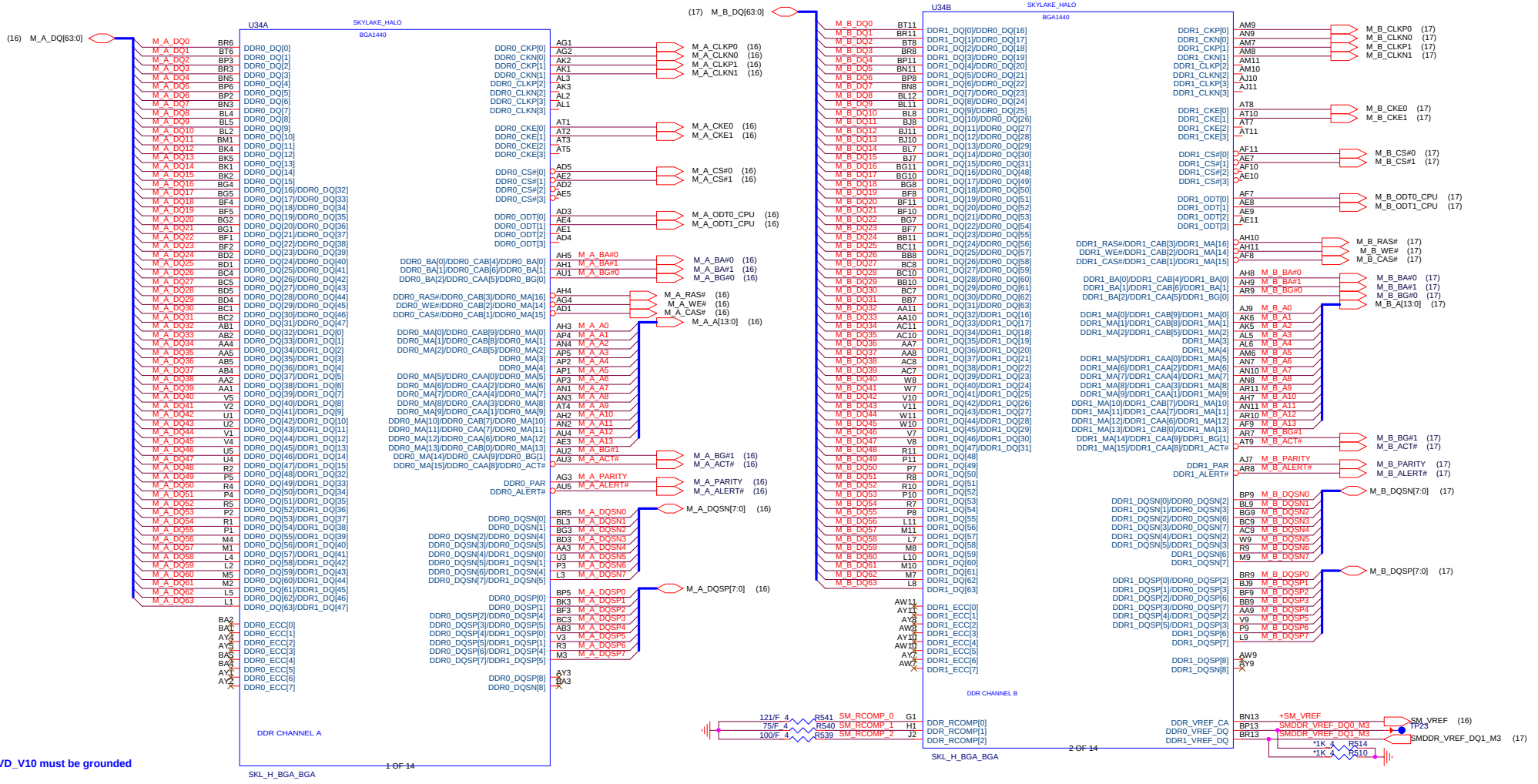
eDP_RCOMP
Trace length < 100 Mils
Trace Width 5 mils Trace Spacing 25 mils

+VCCIO (37,6)
+1.2VSUS (10,16,17,2,35,43,44,50,6)
+3V_S5 (10,12,14,21,23,25,26,27,28,31,32,34,37,38,39,43,49,52)
+3V (10,11,12,13,14,16,17,18,19,20,21,22,23,24,26,27,28,29,30,31,32,36,43,45,50,52,9)

Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	Custom SNB 1/5 (PCIE&DMI&FDI)	2A
Date: Wednesday, October 15, 2014	Sheet 8 of 66	

SKYLAKE Processor (DDR4)

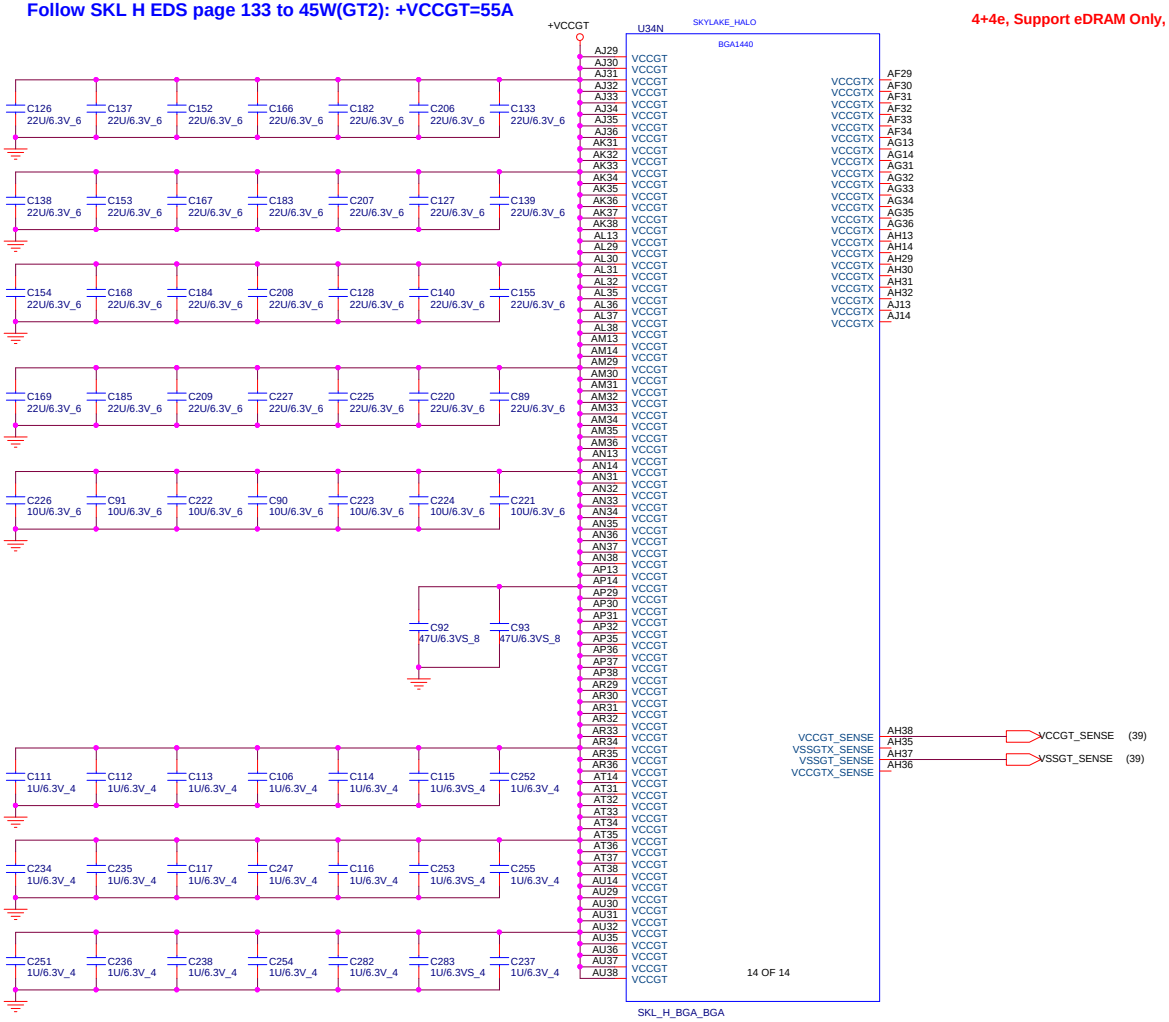


SKYLAKE Processor (POWER)

Follow SKL H EDS page 133 to 45W(GT4+OPC): +VCCGT=104A/12A (GTx)
Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

4+4e, Support eDRAM Only, GTX 12A

+VCC_CORE (40,44,7)
+1.2VSUS (10,16,17,2,35,43,44,50,6)

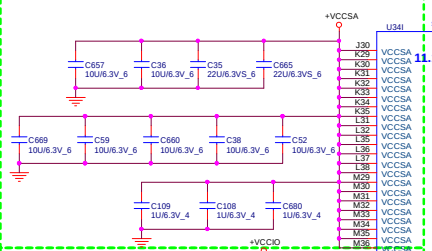


VCC Output Decoupling Recommendations		

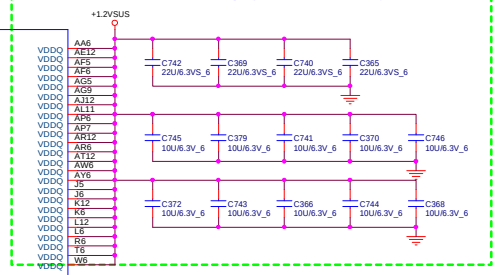
Quanta Computer Inc.
PROJECT :

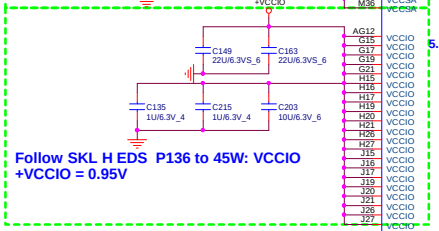
Size	Document Number	Rev
	Custom SNB 3/5 (POWER)	2A
Date: Wednesday, October 19, 2016	Sheet 5 of 66	

Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A (GTx)

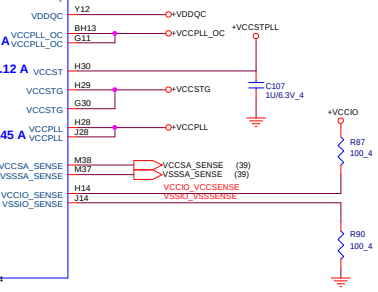


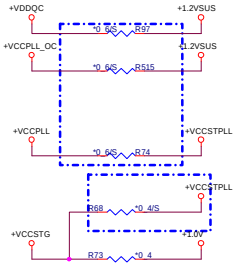
Follow SKL H EDS page 135 45W: VDDQ=2.8A

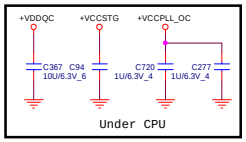


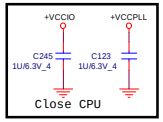


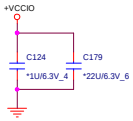
Follow SKL H EDS P136 to 45W: VCCIO
+VCCIO = 0.95V



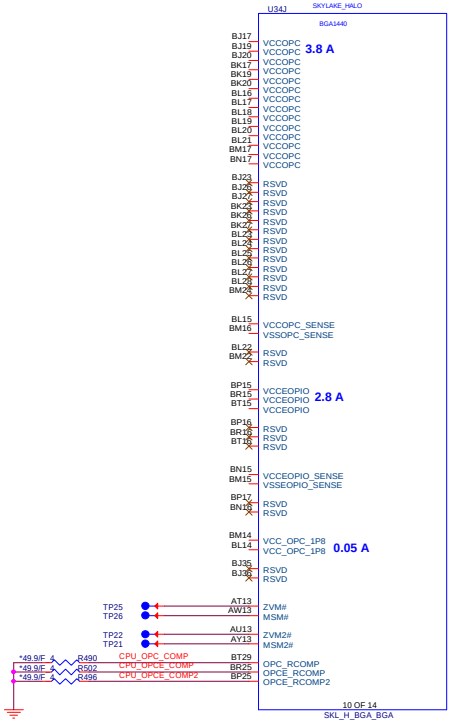








EDRAM Only, PLACE CAPS IN ACK SIDE

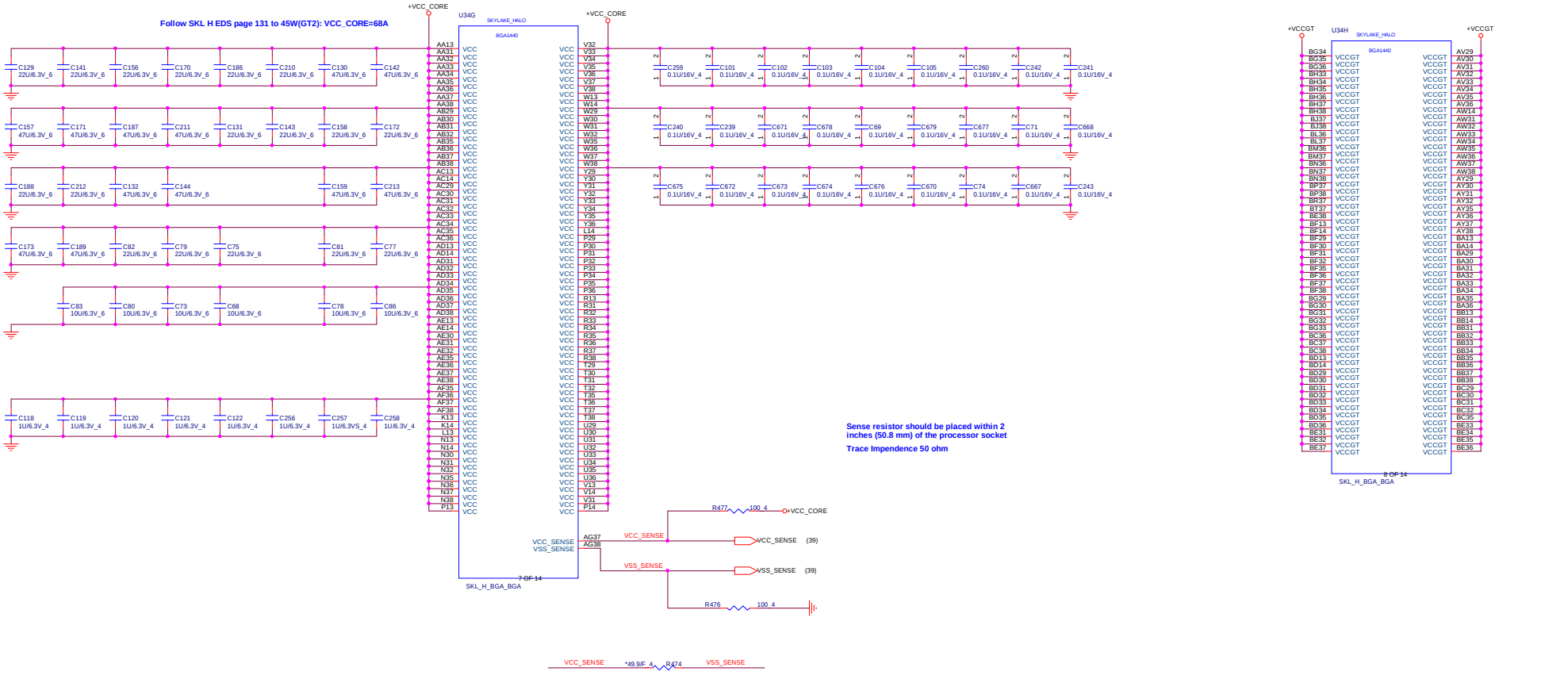


Unconnected for Processors without OPC.

Quanta Computer Inc.

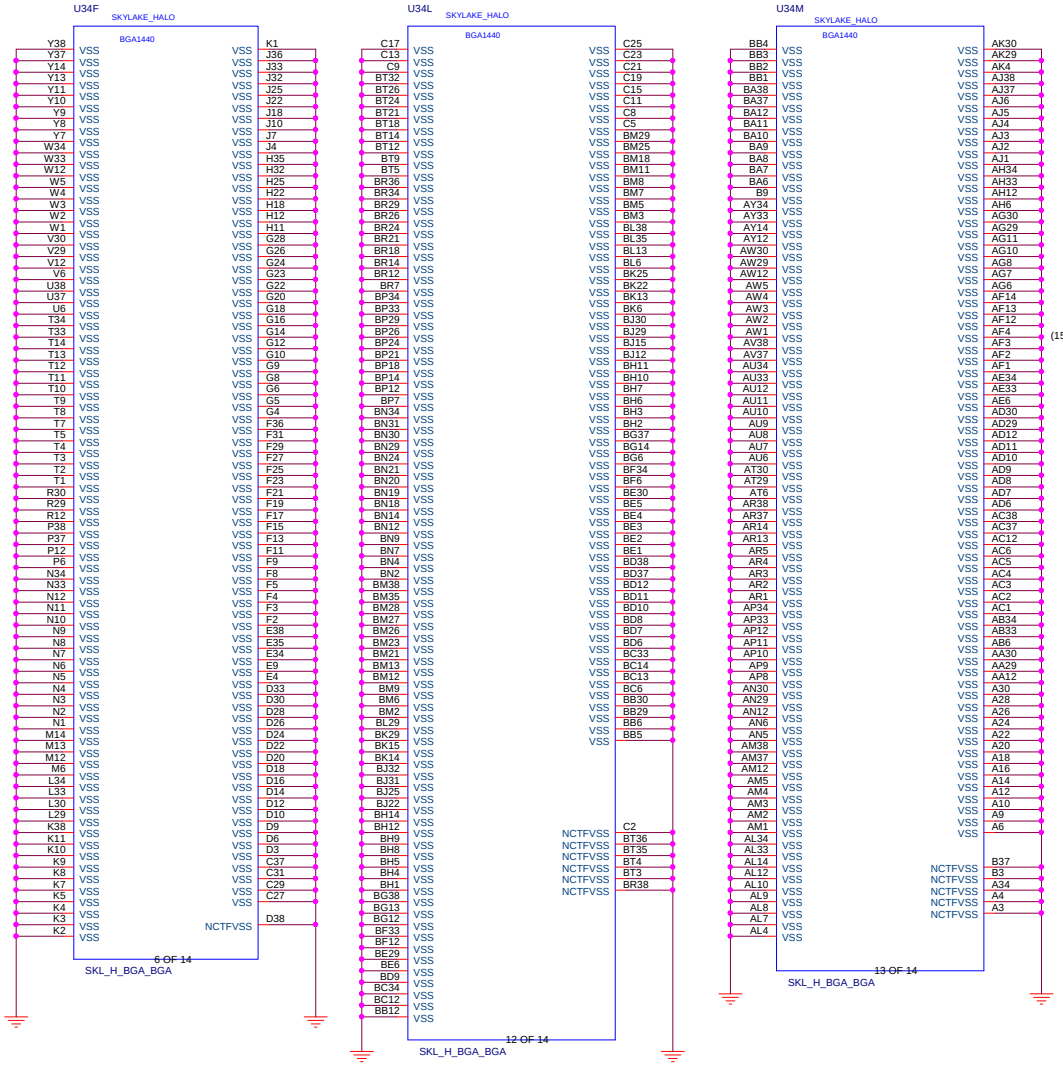
PROJECT :

Size	Document Number	Rev
	Custom SNB 4/5 (POWER & GND)	2A
Date: Wednesday, October 12, 2016	Sheet 6 of 66	

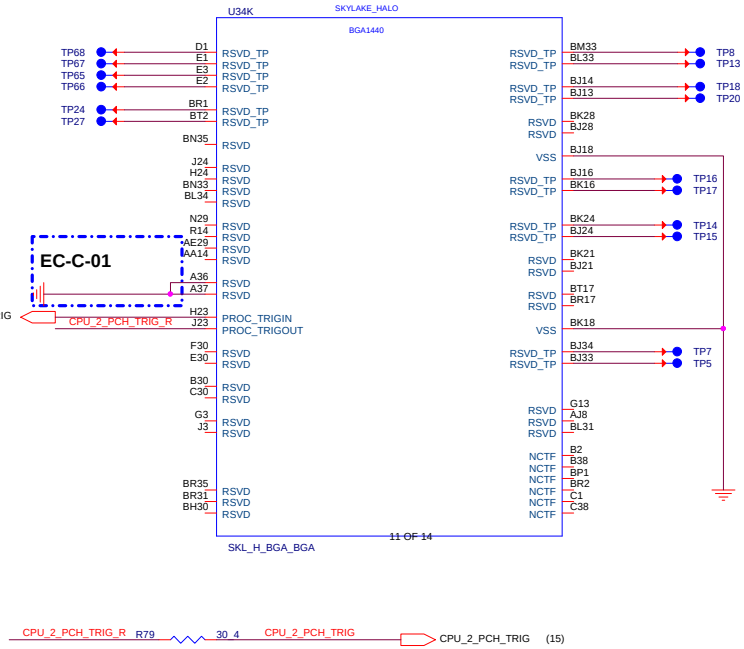


Quanta Computer Inc.			
PROJECT :			
Size	Document Number		Rev
	Custom	SNB 4/5 (POWER & GND)	2A
Date:	Wednesday, October 19, 2016	Sheet	66

Haswell Processor (GND)



Haswell Processor (RESERVED, CFG)



Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	Custom SNB 5/5 (GND)	2A

Date: Wednesday, October 19, 2016 Sheet 8 of 66

Change DMI TX/RX connect_20150109

U49B — SPT-H_PCH

DMI_TXN0 L27 — DMI_RXN0 N27 — DMI_RXP0 C27 — DMI_TXN0 B27 — DMI_TXP0 E24 — DMI_RXN1 G24 — DMI_RXP1 B28 — DMI_TXN1 A28 — DMI_TXP1 G27 — DMI_RXN2 E26 — DMI_RXP2 B29 — DMI_TXN2 C29 — DMI_TXP2 L29 — DMI_RXN3 K29 — DMI_RXP3 B30 — DMI_TXN3 A30 — DMI_TXP3

R637 100/F_4 PCIECOMP_N B18 — PCIECOMP_P C17 — PCIE_RCOMPN — PCIE_RCOMPP

PCIE1_RXN/USB3_7_RXN H15 — PCIE1_RXP/USB3_7_RXP G15 — PCIE1_TXN/USB3_7_TXN A16 — PCIE1_TXP/USB3_7_TXP B16 — PCIE2_TXN/USB3_8_TXN B19 — PCIE2_TXP/USB3_8_TXP C19 — PCIE2_RXN/USB3_8_RXN E17 — PCIE2_RXP/USB3_8_RXP G17 — PCIE3_RXN/USB3_9_RXN L17 — PCIE3_RXP/USB3_9_RXP K17 — PCIE3_TXN/USB3_9_TXN B20 — PCIE3_TXP/USB3_9_TXP C20 — PCIE4_RXN/USB3_10_RXN E20 — PCIE4_RXP/USB3_10_RXP G19 — PCIE4_TXN/USB3_10_TXN B21 — PCIE4_TXP/USB3_10_TXP A21 — PCIE5_RXN K19 — PCIE5_RXP L19 — PCIE5_TXN D22 — PCIE5_TXP C22 — PCIE6_RXN G22 — PCIE6_RXP E22 — PCIE6_TXN B23 — PCIE6_TXP A23 — PCIE7_RXN L22 — PCIE7_RXP K22 — PCIE7_TXN C23 — PCIE7_TXP B23 — PCIE8_RXN L24 — PCIE8_RXP K24 — PCIE8_TXN C24 — PCIE8_TXP B24

PCIe/USB3

USB 2.0

USB2N_1 AF5 — USB2P_1 AG7 — USB2N_2 AD5 — USB2P_2 AD7 — USB2N_3 AG8 — USB2P_3 AG10 — USB2N_4 AE1 — USB2P_4 AE2 — USB2N_5 AC2 — USB2P_5 AC3 — USB2N_6 AF2 — USB2P_6 AF3 — USB2N_7 AB3 — USB2P_7 AB2 — USB2N_8 AL8 — USB2P_8 AL7 — USB2N_9 AA1 — USB2P_9 AA2 — USB2N_10 AJ8 — USB2P_10 AJ7 — USB2N_11 W2 — USB2P_11 W3 — USB2N_12 AD3 — USB2P_12 AD2 — USB2N_13 Y2 — USB2P_13 Y1 — USB2N_14 AJ11 — USB2P_14 AJ13

USBP3- (18) — USBP3+ (18) — **Camera**

USBP6- (29) — USBP6+ (29) — **USB2.0 Combo USB3.0 DB**

USBP7- (25) — USBP7+ (25) — **WLAN/BT**

USBP8- (29) — USBP8+ (29) — **USB DB**

GPP_E9/USB2_OC0# AD43 — GPP_E10/USB2_OC1# AD42 — GPP_E11/USB2_OC2# AD39 — GPP_E12/USB2_OC3# AC44 — GPP_F15/USB2_OC8_4 Y43 — GPP_F16/USB2_OC8_5 Y41 — GPP_F17/USB2_OC8_6 W44 — GPP_F18/USB2_OC8_7 W43

USB_OC3# — USB_OC4# — USB_OC5# — PCH_AOCS#

USB_OC3# (26) — USB_OC4# (26) — USB_OC5# (29) — USB_OC6# (29)

USB2_COMP AG3 — USB2_VBUSSENSE AD10 — RSVD_AB13 AB13 — USB2_ID AG2

USB2_COMP R211 113/F_4

GPD7/RSVD BD14

2 OF 12

SPT_PCH_H

USB3.1 Host x2

Cardreader(DB)

WLAN

cap @ host ic

(26) PCIE_U3P1_RXN5 — (26) PCIE_U3P1_RXP5 — (26) PCIE_U3P1_TXN5 — (26) PCIE_U3P1_TXP5 — (26) PCIE_U3P1_RXP6 — (26) PCIE_U3P1_RXN6 — (26) PCIE_U3P1_TXP6 — (26) PCIE_U3P1_TXN6

(29) PCIE_RXN7_CARD — (29) PCIE_RXP7_CARD — (29) PCIE_TXN7_CARD — (29) PCIE_TXP7_CARD — (25) PCIE_RXN8_WLAN — (25) PCIE_RXP8_WLAN — (25) PCIE_TXN8_WLAN — (25) PCIE_TXP8_WLAN

C832 0.1U/16V_4 PCIE_TXN7_CARD_C — C827 0.1U/16V_4 PCIE_TXP7_CARD_C

C839 0.1U/16V_4 PCIE_TXN8_WLAN_C — C836 0.1U/16V_4 PCIE_TXP8_WLAN_C

GPU Strap

DFX TEST MODE
XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL
DGPU_PWROK_Q *10K_4 R736

RING OSCILLATOR BYPASS
DGPU_HOLD_RST# 100K_4 R739

XTAL INPUT FREQUENCY[0]
GPU_EVENT# *100K_4 R738

XTAL INPUT FREQUENCY[1]
GFXON *10K_4 R347

DGPU_EVENT#-- For BIOS check
+3V
GPU_OVERT#_PCH *10K_4 R714
GPU_EVENT# 10K_4 R727
DGPU_HOLD_RST# *10K_4 R729
GFXON 10K_4 R356
DGPU_PWROK_Q 10K_4 R732
SIO_EXT_SMI# 10K_4 R715
EC_RCIN# 10K_4 R248

PU at USB3.1 host
+3V_DEEP_SUS
USB_OC5# 10K_4 R716
USB_OC3# *10K_4 R737
USB_OC4# 10K_4 R726
USB_OC6# 10K_4 R718
PCH_AOCS# 10K_4 R717

1V8_AON
DGPU_PWROK_Q 3 — 2 — 1 — DGPU_PWROK (32,53,56)
DMG1012T-7 Q66

EC-A-10

+3V — 10K_4 R744 — GC6FBEN_Q
R766 10K_4
(51,55,56) GC6FBEN — Q72 DMG1012T-7 — C934 *0.1U/16V_4 — Q71 DMG1012T-7

USB3.0 (DB)

(29) USB30_TX2- — (29) USB30_TX2+ — (29) USB30_RX2- — (29) USB30_RX2+

USB3.0 (DB)

(29) USB30_TX3+ — (29) USB30_TX3- — (29) USB30_RX3+ — (29) USB30_RX3-

U49F — SPT-H_PCH

USB3_1_TXN C11 — USB3_1_TXP B11 — USB3_1_RXN B7 — USB3_1_RXP A7

USB3_2_TXN/SSIC_1_TXN B12 — USB3_2_TXP/SSIC_1_TXP A12 — USB3_2_RXN/SSIC_1_RXN C8 — USB3_2_RXP/SSIC_1_RXP B8

USB3_6_TXN B15 — USB3_6_TXP C15 — USB3_6_RXN K15 — USB3_6_RXP K13

USB3_5_TXN B14 — USB3_5_TXP C14 — USB3_5_RXN G13 — USB3_5_RXP H13

USB3_3_TXP/SSIC_2_TXP D13 — USB3_3_TXN/SSIC_2_TXN C13 — USB3_3_RXP/SSIC_2_RXP A9 — USB3_3_RXN/SSIC_2_RXN B10

USB3_4_TXP B13 — USB3_4_TXN A14 — USB3_4_RXP G11 — USB3_4_RXN E11

LPC&SPI — USB — SATA

GPP_A1/LAD0/ESPI_IO0 AT22 — GPP_A2/LAD1/ESPI_IO1 AV22 — GPP_A3/LAD2/ESPI_IO2 AT19 — GPP_A4/LAD3/ESPI_IO3 BD16

LPC_LAD0 (25,32) — LPC_LAD1 (25,32) — LPC_LAD2 (25,32) — LPC_LAD3 (25,32)

GPP_A5/LFRAME#/ESPI_CS0# BE16 — GPP_A6/SERIRQ/ESPI_CS1# BA17 — GPP_A7/PIRQA#/ESPI_ALERT0# AW17 — GPP_A0/RCIN#/ESPI_ALERT1# AT17 — GPP_A14/SUS_STAT#/ESPI_RESET# BC18

SERIRQ — BOARD_ID8 — BOARD_ID7

LPC_LFRAME# (25,32) — R255 8.2K_4 — +3V — SERIRQ (32)

BOARD_ID8 (13) — EC_RCIN# (32) — BOARD_ID7 (13)

EC70 18P/50V_4

GPP_A9/CLKOUT_LPC0/ESPI_CLK BC17 — GPP_A10/CLKOUT_LPC1 AV19

CLK_PCI_EC_R — CLK_PCI_LPC_R

R640 22/F_4 — R258 22/F_4 — CLK_24M_KBC (32) — PCLK_DEBUG (25)

GPP_G19/SMI# M45 — GPP_G18/NMI# N43

SIO_EXT_SMI# (26,32)

EC35 18P/50V_4

EMI(near PCH)

GPP_E6/DEVSLP2 AE45 — GPP_E5/DEVSLP1 AG43 — GPP_E4/DEVSLP0 AG42 — GPP_F9/DEVSLP7 AB39 — GPP_F8/DEVSLP6 AB36 — GPP_F7/DEVSLP5 AB43 — GPP_F6/DEVSLP4 AB42 — GPP_F5/DEVSLP3 AB41

GC6FBEN_Q — SSD_DEVSLP — DGPU_HOLD_RST# — GPU_EVENT# — GFXON — DGPU_PWROK_Q — GPU_OVERT#_PCH

SSD_DEVSLP (24) — DGPU_HOLD_RST# (53) — GPU_EVENT# (55) — GFXON (45,50,51,56) — GPU_OVERT#_PCH (56)

6 OF 12

SPT_PCH_H

(10,12,13,14,16,43) +3V_DEEP_SUS

Quanta Computer Inc.			
PROJECT :			
Size	Document Number Custom	PCH 1/6 (DMI/FDI/VIDEO)	Rev 2A
Date: Wednesday, October 28, 2015		Sheet 6 of 66	

HDA Bus(CLG)

(21) ACZ_BIT_CLK_AUDIO — R606 33_4 — ACZ_BCLK
(21) ACZ_RST#_AUDIO — R619 33_4 — ACZ_RST#
(12) ACZ_SDOUT
(21) ACZ_SDOUT_AUDIO — R597 33_4 — ACZ_SDOUT
(21) ACZ_SYNC_AUDIO — R622 33_4 — ACZ_SYNC
R623 *1M_4

Reserve for EMI
EC66 *10P/50V_4
(21) ACZ_SDIN0

Change R2032 from 33 to 30_20141218

+3V_DEEP_SUS
Add PU _20141212
R354 2.2K_4 SMB_ME0_CLK
R355 2.2K_4 SMB_ME0_DAT
R723 2.2K_4 SMB_ME1_CLK
R724 2.2K_4 SMB_ME1_DAT
R353 2.2K_4 SMB_PCH_CLK
R352 2.2K_4 SMB_PCH_DAT
R626 10K_4 RF_OFF_PCH
R646 10K_4 SUSWARN#
R649 *10K_4 SUSACK#
(32) GPIO33_EC — R596 1K_4 — ACZ_SDOUT

DDR3_DRAMRST# RV9 *EGA-0402
PCIE_WAKE# RV25 *EGA-0402
SYS_RESET# RV8 *EGA-0402

RSMRST# C461 *220P/50V_4
EC_PWROK C440 *220P/50V_4

(3) AUD_AZACPU_SDO_R — R601 30_4 AUD_AZACPU_SDO
(3) AUD_AZACPU_SDI — AUD_AZACPU_SDI
(3) AUD_AZACPU_SCLK — R608 30_4 AUD_AZACPU_SCLK_R
AUD_AZACPU_SCLK
EC65 *33P/50V_4
EMI
+3V_DEEP_SUS — R598 *4.7K_4 — ACZ_SDOUT

(32) RSMRST# — RSMRST#
(12) SML0ALERT# — DSWROK_EC_R — SML0ALERT# — SMB_PCH_CLK — SMB_PCH_DAT
(12) DRAMRST_CNTRL_PCH — DRAMRST_CNTRL_PCH — SMB_ME0_CLK — SMB_ME0_DAT
(12) SML1ALERT#_R — SML1ALERT#_R — SMB_ME1_CLK — SMB_ME1_DAT
TP49

U49D — SPT-H_PCH — AUDIO — SMBUS — JTAG

ACZ_BCLK — BA9 — HDA_BCLK
ACZ_RST# — BD8 — HDA_RST#
BE7 — HDA_SDI0
BC8 — HDA_SDI1
ACZ_SDOUT — BB7 — HDA_SDO
ACZ_SYNC — BD9 — HDA_SYNC
BD1 — RSVD_BD1
BE2 — RSVD_BE2
DISPA_SDO — AM1
DISPA_SDI — AN2
DISPA_BCLK — AM2
AL42 — GPP_D8/I2S0_SCLK
AN42 — GPP_D7/I2S0_RXD
AM43 — GPP_D6/I2S0_TXD
AJ33 — GPP_D5/I2S0_SFRM
AH44 — GPP_D20/DMIC_DATA0
AJ35 — GPP_D19/DMIC_CLK0
AJ38 — GPP_D18/DMIC_DATA1
AJ42 — GPP_D17/DMIC_CLK1
RTC_RST# — BC10 — RTCRST#
SRTC_RST# — BB10 — SRTCRST#
PCH_PWROK — AW11 — PCH_PWROK
RSMRST# — BA11 — RSMRST#
DSW_PWROK
GPP_C2/SMBALERT#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C5/SML0ALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
SPT_PCH_H
4 OF 12

GPP_A12/BMBUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
GPD11/LANPHYPC
GPD9/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1
GPP_B0
GPP_G17/ADR_COMPLETE
GPP_B11
SYS_PWROK
WAKE#
GPD6/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD8/SUSCLK
GPD0/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
PROCPWRGD
ITP_PMODE
JTAGX
JTAG_TMS
JTAG_TDO
JTAG_TDI
JTAG_TCK

BB17
AW22 — CLKRUN# — TP47 — CLKRUN# (32)
AR15 — LAN_DISABLE — TP46
AV13 — TP43
BC14 — DDR3_DRAMRST# — DDR3_DRAMRST# (16,17)
BD23 — GPP_B2
AL27
AR27
N44
AN24
AY1 — EC_PWROK
BC13 — PCIE_WAKE# — PCIE_WAKE# (23,25,26,32)
BC15 — TP44
AV15
BC26 — PCH_SLP_S0_N — PCH_SLP_S0_N (32,37)
AW15 — SUSB# (32)
BD15 — SUSC# (32)
BA13 — TP90
AN15 — PCH_SUSCLK
BD13 — RF_OFF_PCH — RF_OFF_PCH (25)
BB19 — SUSACK# — *0_4/S — R645 — SUSACK#_EC (32)
BD19 — SUSWARN# — *0_4/S — R643 — SUSWARN#_EC (32)
EC-A-15
EC-B-05
BD11
BB15 — AC_PRESENT_R — *0_4 — R246 — AC_PRESENT (32,55)
BB13 — SLP_SUS#_EC — SLP_SUS#_EC (32)
AT13 — DNBSWON# — DNBSWON# (32)
AW1 — SYS_RESET# — TP81
BD26 — ACZ_SPKR — ACZ_SPKR (12,21)
AM3 — PROCPWRGD — PROCPWRGD (2)
AT2 — ITP_PMODE — R593 1K_4 — +1.0V_DEEP_SUS
AR3 — JTAGX — TP74
AE2 — JTAG_TMS_PCH — TP78
AP1 — JTAG_TDO_PCH — TP75
AP2 — JTAG_TDI_PCH — TP77
AN3 — JTAG_TCK_PCH — TP76

+1.2VSUS
R630 470/F_4

*0_4 — R644 — SUSWARN#

SYS_RESET# — R600 10K_4 — +3V
GPP_B2 — R678 10K_4

+1.0V
R604 *51_4
R603 *51_4
R602 *51_4
JTAGX — JTAGX (2)
JTAG_TMS_PCH — JTAG_TMS_PCH (2)
JTAG_TDI_PCH — JTAG_TDI_PCH (2)
JTAG_TDO_PCH — JTAG_TDO_PCH (2)
JTAG_TCK_PCH
R612 *51_4
R611 *51_4
R610 *51_4
R616 51_4

EC-A-16

CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Q65 — +3V
(32) MBCLK2 — SMB_ME1_CLK
(32) MBDATA2 — SMB_ME1_DAT
*2N7002DW

Q30 — +3V
+3V — R361 4.7K_4 — (16,17) SMB_RUN_DAT — SMB_PCH_DAT
+3V — R366 4.7K_4 — (16,17) SMB_RUN_CLK — SMB_PCH_CLK
2N7002KDW

DPt o CRT
DDR4

System PWR_OK(CLG)

+3V_S5 — C424 *0.1U/10V_4
PCH_PWROK — U13 TC7SH08FU — IMVP_PWRGD — IMVP_PWRGD (39)
EC_PWROK — EC_PWROK (21,32)
R200 100K_4
R195 *0_4

For DS3 Sequence

For DS3 -->Ra<----
Non-DS3 -->Rb

Rb
RSMRST# — R226 — *0_4
(32) DSWROK_EC — R205 — *0_4/S — DSWROK_EC_R
Ra

RTC Circuitry(RTC)

+5VPCU
R397 1.2K_4
R398 1K_4
Q35 MMBT3904
R396 4.7K/F_4
R395 15K/F_4
RTC Power trace width 20mils.
D21 BAT54CW
+3VPCU
+3V_RTC_0 — R752 1K_4 — +3V_RTC_1
CN22
RTC_B
C850 1U/6.3V_4

30mils
+3V_RTC
R659 20K/F_4
J1 *SOLDERJUMPER-2
RTC_RST#
C830 1U/6.3V_4
R669 20K/F_4
SRTC_RST#
C849 1U/6.3V_4
Q64 2N7002K
EC_RTC_RST (32)
R680 10K_4

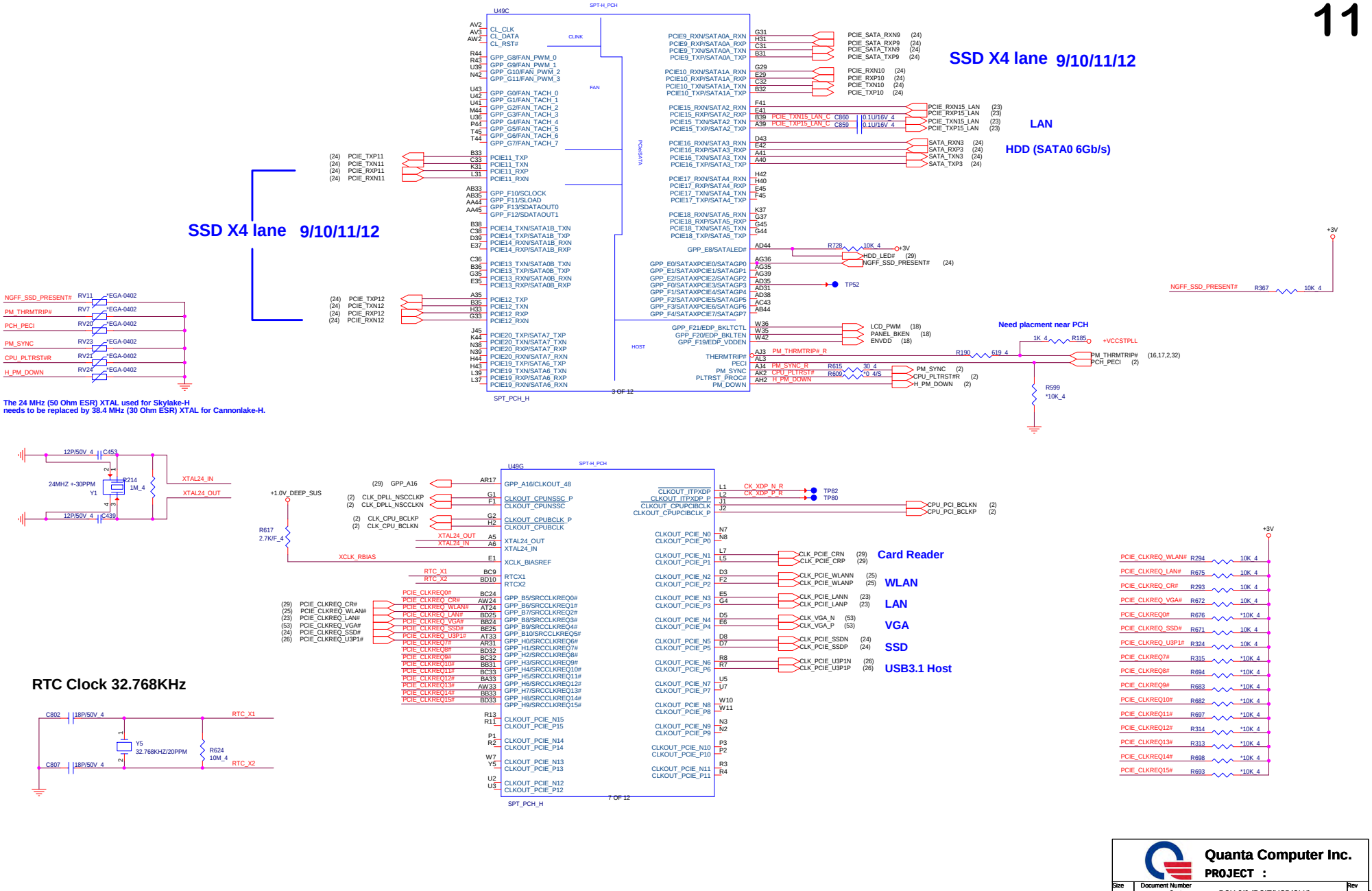
For HWPG Sequence

+3V_S5
+5V_S5
+1.0V
R364 100K_4
R340 10K_4
HWPG — HWPG (2,32,34,35,36,38,49)
R344 15K/F_4
+1.0V_PWRGD_G2
Q29 2N7002K
R341 100K_4
+1.0V_PWRGD_G1
Q31 METR3904-G
C525 0.1U/16V_4
R343 100K_4

+3V_S5
R625 1K_4 — PCIE_WAKE#
R629 10K_4 — AC_PRESENT_R
+3V
R284 8.2K/F_4 — CLKRUN#
RSMRST# — R240 10K_4
DSWROK_EC — R193 100K_4
IMVP_PWRGD — R176 *100K_4

Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	Custom	PCH 2/6 (SATA/HDA/SPI)	2A
Date:	Wednesday, October 29, 2014	Sheet	66

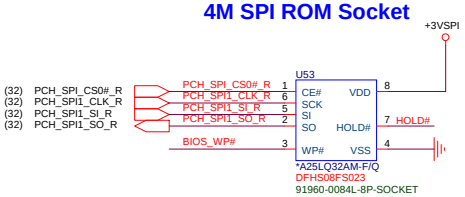

SSD X4 lane 9/10/11/12
SSD X4 lane 9/10/11/12
LAN
HDD (SATA0 6Gb/s)
Need placment near PCH
The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H
needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.
RTC Clock 32.768KHz
Card Reader
WLAN
LAN
VGA
SSD
USB3.1 Host
U49C
SPT-H_PCH
SPT_PCH_H
3 OF 12
U49G
7 OF 12
HOST
CLINK
FAN
PCIE/SATA
NGFF_SSD_PRESENT#
PM_THRMTRIP#
PCH_PECI
PM_SYNC
CPU_PLTRST#R
H_PM_DOWN
24MHZ +-30PPM
Y1
32.768KHZ/20PPM
+1.0V_DEEP_SUS
XCLK_RBIAS
TP52
TP82
TP80
Quanta Computer Inc.
PROJECT :
PCH 3/6 (PCIE/USB/CLK)
Wednesday, October 19, 2016

PCH Strap Pin

PCH SPI ROM(CLG)

Vender	Size	P/N
EON		
Winbond	16MB	AKE3DZN0N01
GigaDevice		
Socket		DFHS08FS023

4M SPI ROM Socket



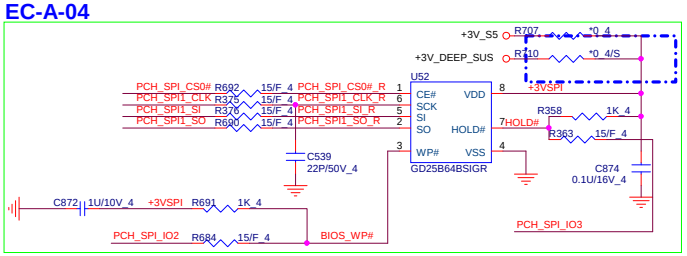
TP66-71 need place to TOP

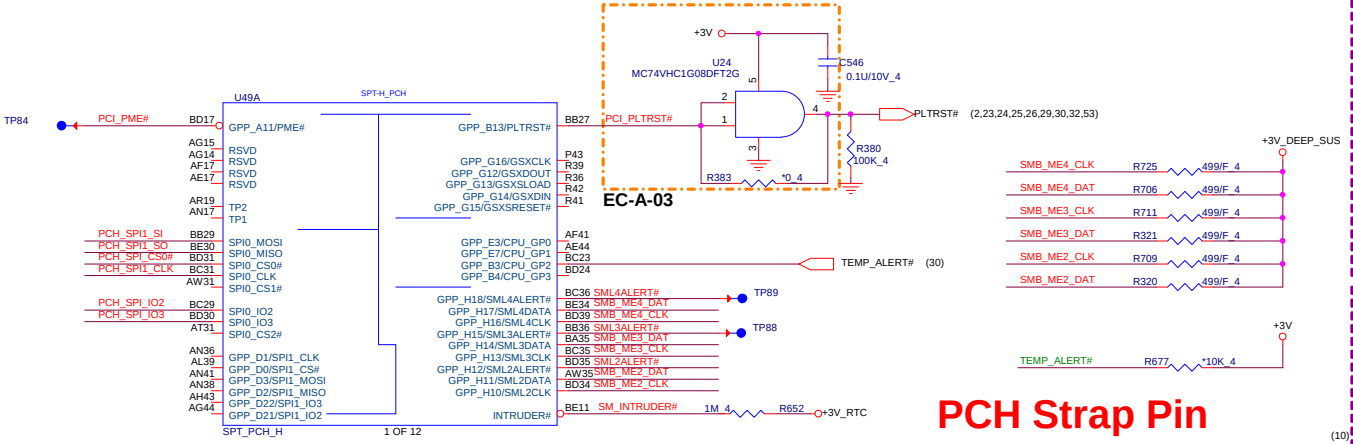
TP86 PCH_SPI_CS0#_R
TP56 PCH_SPI1_CLK_R
TP56 PCH_SPI1_SI_R
TP87 PCH_SPI1_SO_R
TP85 BIOS_WP#
TP54 HOLD#

U2003&U2004 footprint must overlap

PCH SPI ROM(CLG)

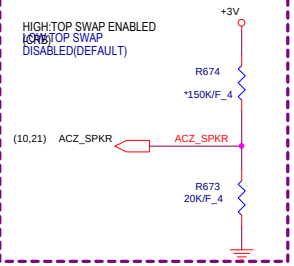
EC-A-04





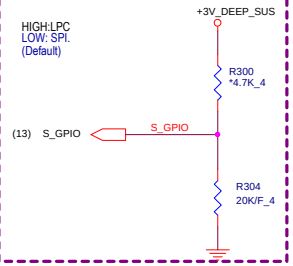
TOP SWAP OVERRIDE STRAP

HIGH:TOP SWAP ENABLED
LOW:TOP SWAP DISABLED(DEFAULT)



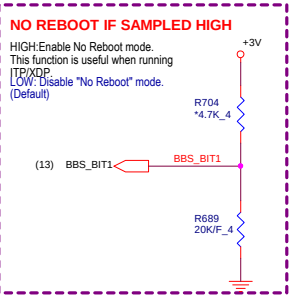
BOOT SELECT STRAP

HIGH:LPC
LOW: SPI.
(Default)



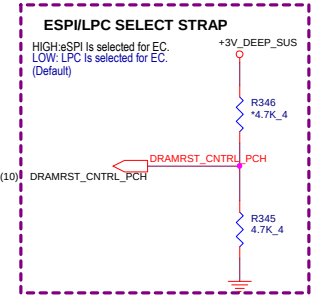
NO REBOOT IF SAMPLED HIGH

HIGH:Enable No Reboot mode.
This function is useful when running ITP/XDP.
LOW: Disable "No Reboot" mode.
(Default)



ESPI/LPC SELECT STRAP

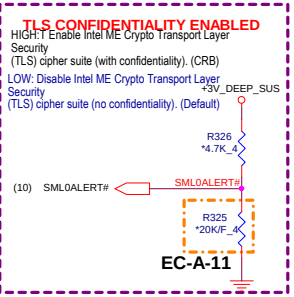
HIGH:eSPI Is selected for EC.
LOW: LPC Is selected for EC.
(Default)



TLS CONFIDENTIALITY ENABLED

HIGH:T Enable Intel ME Crypto Transport Layer Security
(TLS) cipher suite (with confidentiality). (CRB)

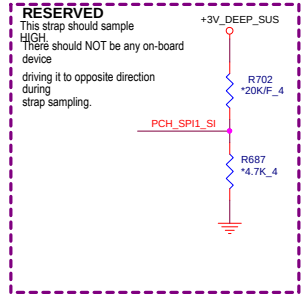
LOW: Disable Intel ME Crypto Transport Layer Security
(TLS) cipher suite (no confidentiality). (Default)



EC-A-11

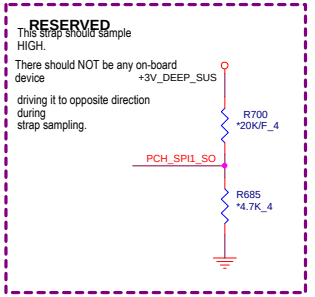
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device
driving it to opposite direction during strap sampling.



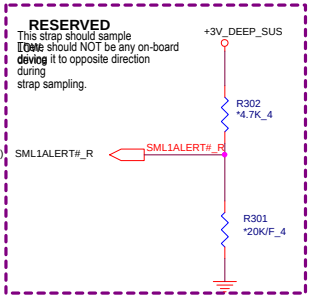
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device
driving it to opposite direction during strap sampling.



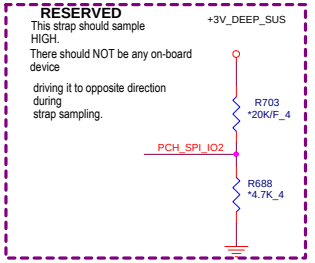
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device
driving it to opposite direction during strap sampling.



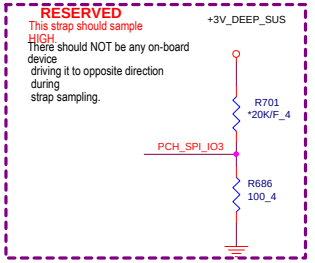
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device
driving it to opposite direction during strap sampling.



RESERVED

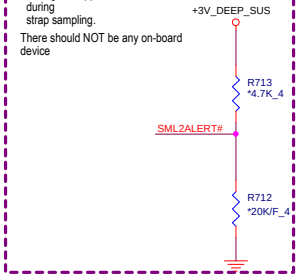
This strap should sample HIGH.
There should NOT be any on-board device
driving it to opposite direction during strap sampling.



ESPI FLASH SHARING MODE

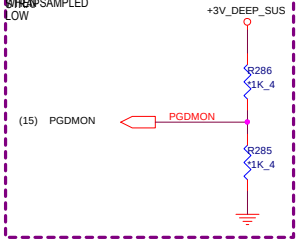
HIGH:SLAVE ATTACEHD FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING

This strap should sample LOW.
driving it to opposite direction during strap sampling.
There should NOT be any on-board device



DFX TEST MODE QUALIFIER FOR OTHER DFX

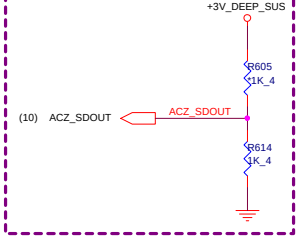
This strap should be sampled LOW



TLS CONFIDENTIALITY ENABLED

HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.(CRB)

LOW: security measures defined in the Flash Descriptor. (Default)



Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	Custom PCH 4/6 (GPIO/MISC)	2A
Date:	Wednesday, October 19, 2016	Sheet 66 of 66

(10,12,14,16,43,9) +3V_DEEP_SUS

Need check PCI_GNT3#_20141119

(12) S_GPIO — TP50 — S_GPIO — PCI_GNT3#

(12) BBS_BIT1
(16) PM_EXTTS#0
(16) EXTTS#1
BBS_BIT1

U49K — SPT-H_PCH

GPP_B22/GSPI1_MOSI — AT29
GPP_B21/GSPI1_MISO — AR29
GPP_B20/GSPI1_CLK — AV29
GPP_B19/GSPI1_CS# — BC27
GPP_B18/GSPI0_MOSI — BD28
GPP_B17/GSPI0_MISO — BD27
GPP_B16/GSPI0_CLK — AW27
GPP_B15/GSPI0_CS# — AR24
GPP_C9/UART0_TXD — AV44
GPP_C8/UART0_RXD — BA41
GPP_C11/UART0_CTS# — AU44
GPP_C10/UART0_RTS# — AV43
GPP_C15/UART1_CTS#/ISH_UART1_CTS# — AU41
GPP_C14/UART1_RTS#/ISH_UART1_RTS# — AT44
GPP_C13/UART1_TXD/ISH_UART1_TXD — AT43
GPP_C12/UART1_RXD/ISH_UART1_RXD — AU43
GPP_C23/UART2_CTS# — AN43
GPP_C22/UART2_RTS# — AN44
GPP_C21/UART2_TXD — AR39
GPP_C20/UART2_RXD — AR45
GPP_C19/I2C1_SCL — AR41
GPP_C18/I2C1_SDA — AR44
GPP_C17/I2C0_SCL — AR38
GPP_C16/I2C0_SDA — AT42
GPP_D4/ISH_I2C2_SDA/ISH_I2C3_SDA — AM44
GPP_D23/ISH_I2C2_SCL/ISH_I2C3_SCL — AJ44

GPP_D9 — AL44
GPP_D10 — AL36 — CAM_EN_R — R318 *0 4/S — CAM_EN (18)
GPP_D11 — AL35 — RF_OFF — TP51
GPP_D12 — AJ39 — BT_OFF — BT_OFF (25)
GPP_D16/ISH_UART0_CTS# — AJ43 — NVDDS_EN — NVDDS_EN (46)
GPP_D15/ISH_UART0_RTS# — AL43 — NVDD_EN — NVDD_EN (45)
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C2_SCL — AK44 — 1V8AON_EN — 1V8AON_EN (50)
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C2_SDA — AK45
GPP_H20/ISH_I2C0_SCL — BC38
GPP_H19/ISH_I2C0_SDA — BB38
GPP_H22/ISH_I2C1_SCL — BD38
GPP_H21/ISH_I2C1_SCL — BE39
GPP_A23/ISH_GP5 — BC22 — BOARD_ID6
GPP_A22/ISH_GP4 — BD18 — BOARD_ID5
GPP_A21/ISH_GP3 — BE21 — BOARD_ID4
GPP_A20/ISH_GP2 — BD22 — BOARD_ID3
GPP_A19/ISH_GP1 — BD21 — BOARD_ID2
GPP_A18/ISH_GP0 — BB22 — BOARD_ID1
GPP_A17/ISH_GP7 — BC19 — BOARD_ID0

11 OF 12

SPT_PCH_H

+3V_DEEP_SUS
R721 49.9K/F_4
R722 49.9K/F_4
+3V_DEEP_SUS — R720 10K_4 — SIO_EXT_SCI# — (32) SIO_EXT_SCI#
(29) UART2_TXD — UART2_TXD
(29) UART2_RXD — UART2_RXD

BOARD_ID0 (18)
R641 *10K_4 BOARD_ID0 — R642 10K_4 — +3V_DEEP_SUS
R662 *10K_4 BOARD_ID1 — R663 10K_4
R647 10K_4 BOARD_ID2 — R648 *10K_4
R660 10K_4 BOARD_ID3 — R661 *10K_4
R655 *10K_4 BOARD_ID4 — R656 10K_4
R634 10K_4 BOARD_ID5 — R635 *10K_4
R653 10K_4 BOARD_ID6 — R654 *10K_4
R636 10K_4 BOARD_ID7 — R639 *10K_4
R271 10K_4 BOARD_ID8 — R277 *10K_4
BOARD_ID7 (9)
BOARD_ID8 (9)

BT_OFF — R365 10K_4
NVDDS_EN — R740 10K_4
NVDD_EN — R741 10K_4
1V8AON_EN — R719 10K_4

Model	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4]	BOARD_ID[3:2]	BOARD_ID[1:0]
Definition	Reserve (Default = 00)	Reserve (Default = 00)	1:DDR4 (default)	00 N17P-G1 01 N17P-G0 10	10 NL8E 11 NL9E Cable detect

EC-B-01

U49E — SPT-H_PCH

GPP_I0/DDPB_HPD0 — AW4
GPP_I1/DDPC_HPD1 — AY2
GPP_I2/DDPD_HPD2 — AV4
GPP_I3/DDPE_HPD3 — BA4
GPP_I4/EDP_HPD — BD7
GPP_I7/DDPC_CTRLCLK — BB3
GPP_I8/DDPC_CTRLDATA — BD6
GPP_I5/DDPB_CTRLCLK — BA5
GPP_I6/DDPB_CTRLDATA — BC4
GPP_I9/DDPD_CTRLCLK — BE5
GPP_I10/DDPD_CTRLDATA — BE6
GPP_F14 — Y44
GPP_F23 — V44
GPP_F22 — W39
GPP_G23 — L43
GPP_G22 — L44
GPP_G21 — U35
GPP_G20 — R35
GPP_H23 — BD36

DP_HDMI_SCL — DP_HDMI_SCL (19)
DP_HDMI_SDA — DP_HDMI_SDA (19)
HDMI_SCL (20)
HDMI_SDA (20)
DDPD_CTRLCLK — TP94
DDPD_CTRLDATA — TP39
SKTOCC_N_R — SKTOCC_N_R (2)

5 OF 12

SPT_PCH_H

This signal has a weak internal pull-down.
0 = Port C D is not detected.
1 = Port C D is detected.

+3V
DDPD_CTRLDATA — R225 2.2K_4
DP_HDMI_SCL — R156 2.2K_4
DP_HDMI_SDA — R784 2.2K_4

EC-B-01

Reserve EDP_HPD opposites circuit!

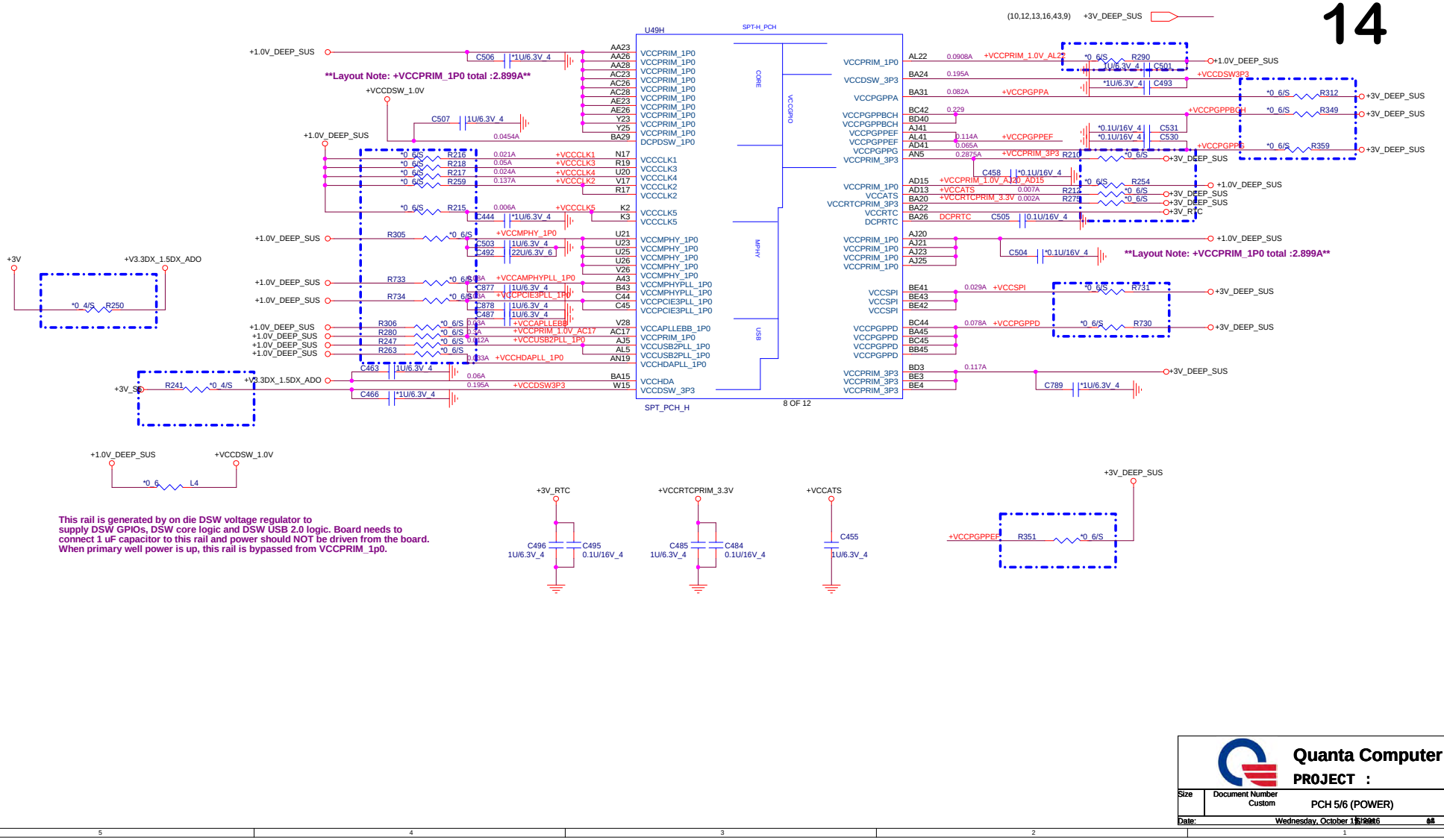
+3V
R202 10K/F_4
EDP_HPD
R227 100K_4

(20,55) HDMI_HPD_CON — HDMI_HPD_CON — R233 *0_4_S — HHC_R
(19) DP_HPD_Q — DP_HPD_Q — R166 *0_4_S — TDH
(13,27,28) TypeC1_DDI1_HPD

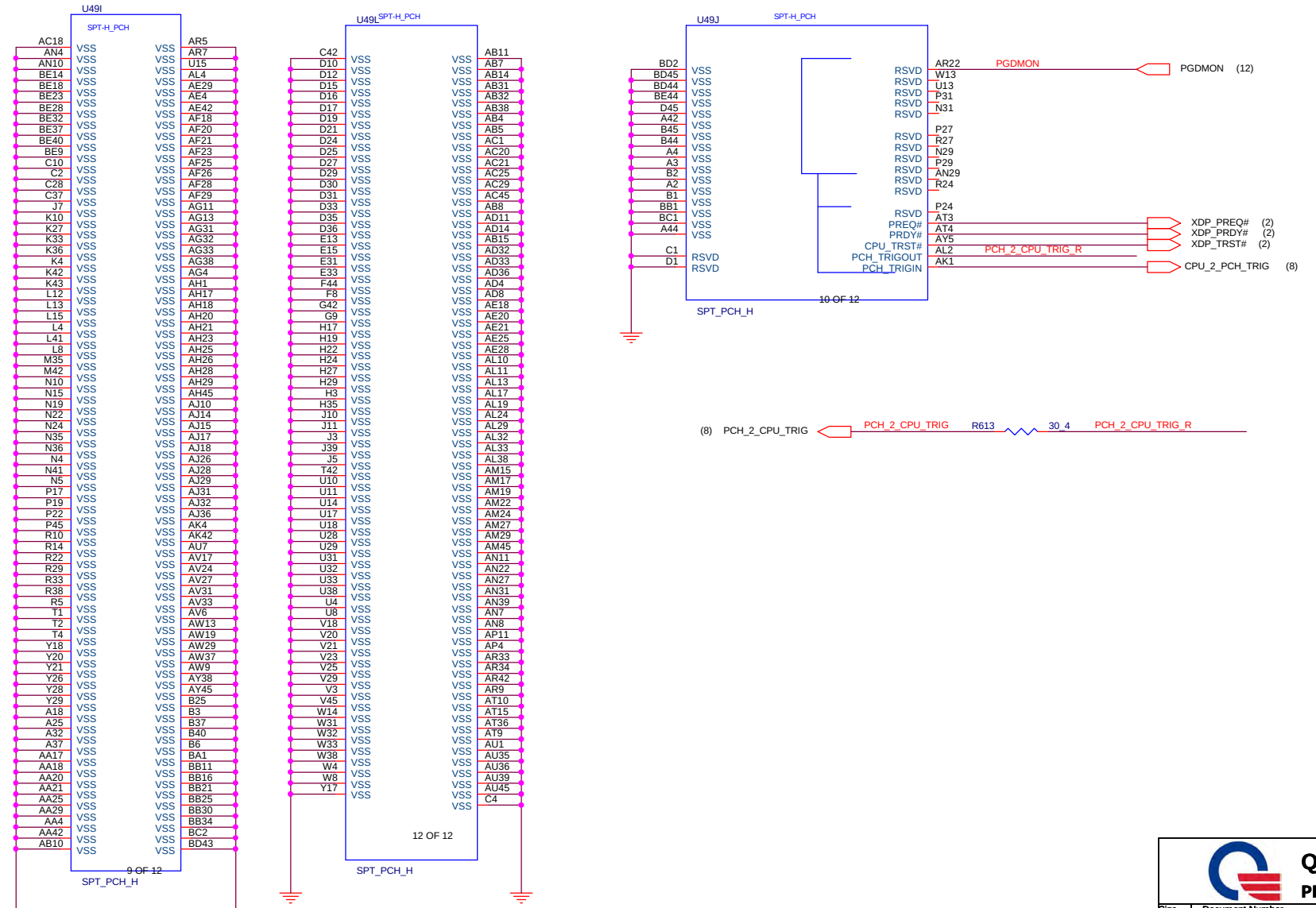
DP_HPD_Q — R201 100K_4
(18) EDP_HPD — EDP_HPD

+3V
TDH — 1 — Q69 *2N7002K — 3 — TypeC1_DDI1_HPD (13,27,28)
2
R30 *1M/F_4
R759 100K_4

Quanta Computer Inc.			
PROJECT :			
Size	Document Number Custom	PCH 4/6 (GPIO/MISC)	Rev 2A
Date: Wednesday, October 19, 2016		Sheet 48 of 66	

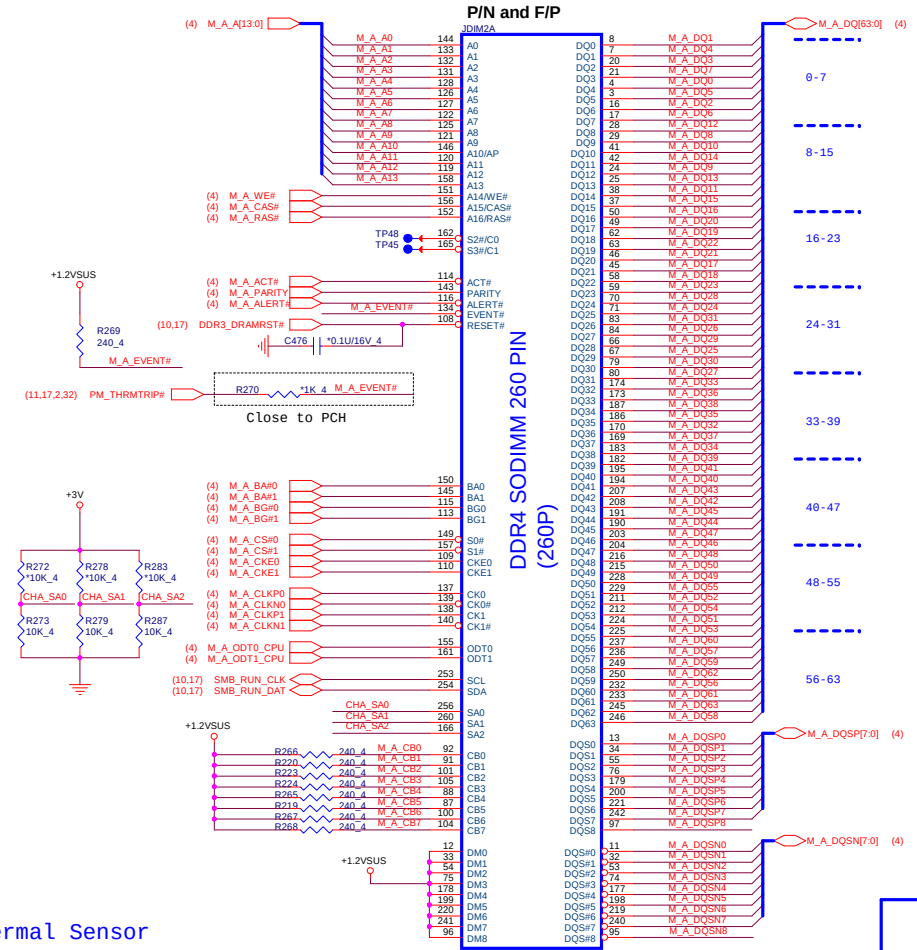


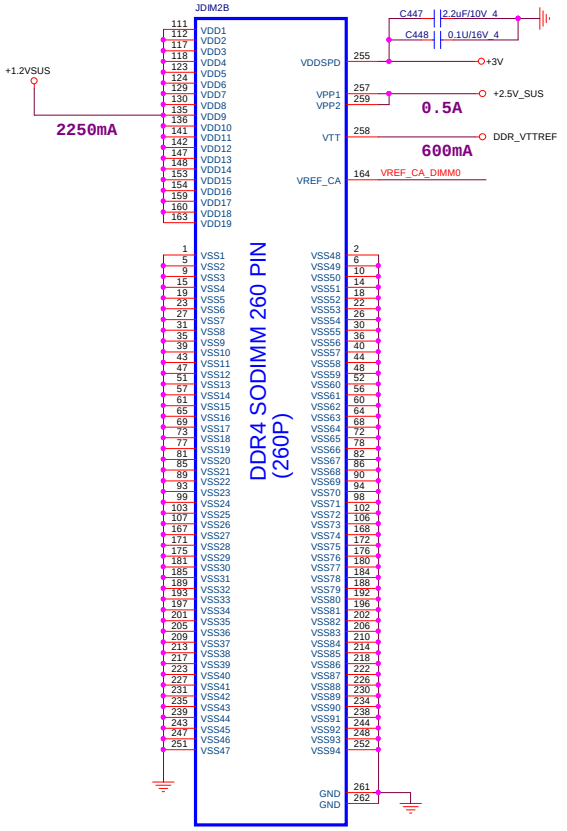
Quanta Computer Inc.			
PROJECT :			
Size	Document Number Custom	PCH 5/6 (POWER)	Rev 2A
Date:	Wednesday, October 19, 2016	Sheet 66	



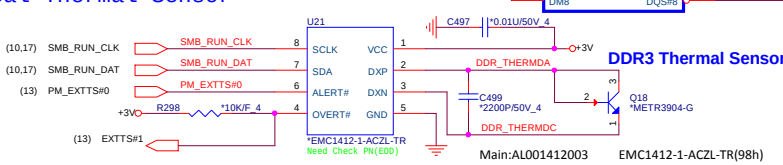
Quanta Computer Inc.		
PROJECT :		
Size	Document Number	Rev
	B PCH 6/6 (GND)	2A
Date: Wednesday, October 19, 2011	Sheet 15 of 66	

P/N and F/P





Local Thermal Sensor

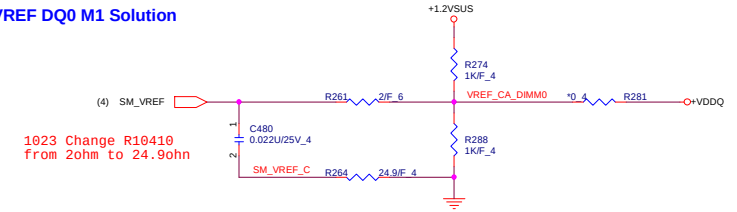


DDR3 Thermal Sensor

Main:AL001412003 EMC1412-1-ACZL-TR(98h)

2nd:AL000431014 TMP431ADGKR(98h)

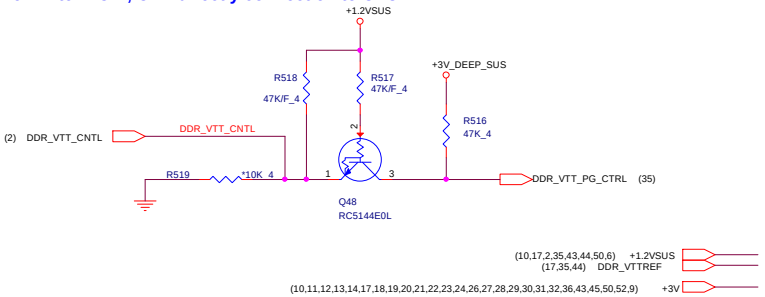
VREF DQ0 M1 Solution



1023 Change R10410 from 2ohm to 24.9ohn

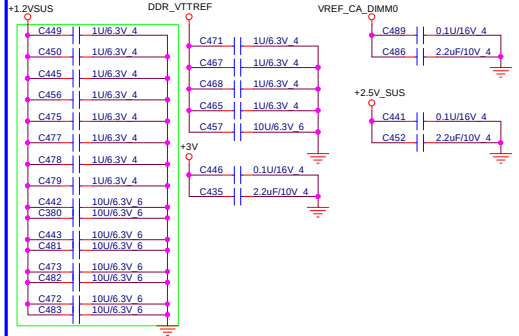
Co-lay for ODT

From Intel MOW, ODT directly connection to CPU



Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector



PROJECT :ZRY
Quanta Computer Inc.

Size	Document Number	Rev
Custom	18 -- DDR3 DIMM1-RVS(8.0H)	1A
Date: Monday, October 17, 2016	Sheet 16 of 66	

P/N and F/P

JDIM1A

DDR4 SODIMM 260 PIN (260P)

JDIM1B

DDR4 SODIMM 260 PIN (260P)

Close to PCH

2250mA

0.5A

600mA

For EMI RESERVE

Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector

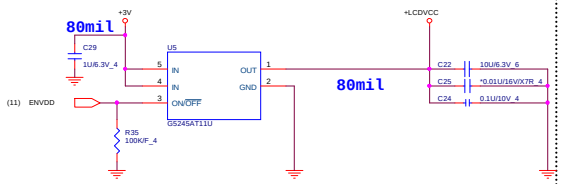
VREF DQ1 M1 Solution

1022 Del R10432

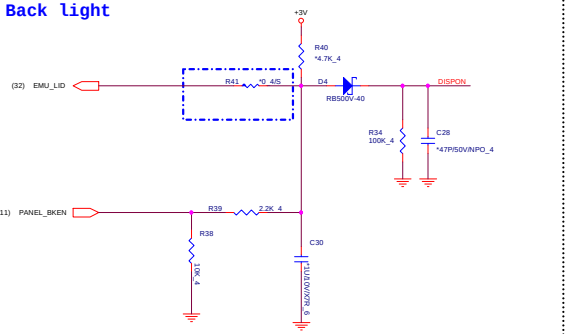
PROJECT :	ZRY
Quanta Computer Inc.	
Size: Custom	Document Number: 17 – DDR3 DIMM0-STD(4.0H)
Rev: 1A	
Date: Monday, October 17, 2016	Sheet 17 of 66

(10,11,12,13,14,16,17,19,20,21,22,23,24,26,27,28,29,30,31,32,36,43,45,50,52,9) +3V
(10,21,29,31,32,33,34,55) +3VPCU
(33,34,35,36,39,40,41,42,47,50,52,63) +VIN

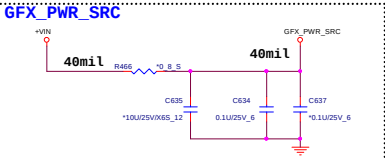
LCDVCC

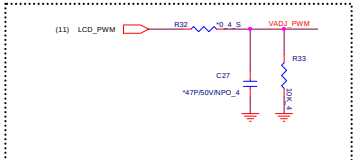


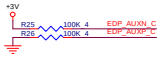
Back light



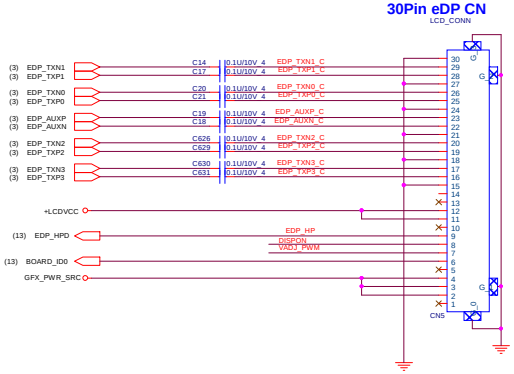
GFX_PWR_SRC



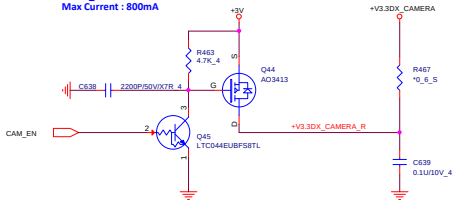




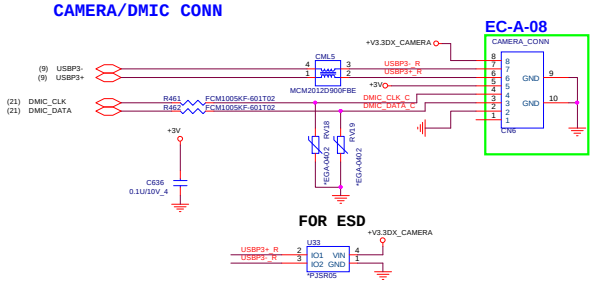
30Pin eDP CN



CAMERA VCC Control



CAMERA/DMIC CONN



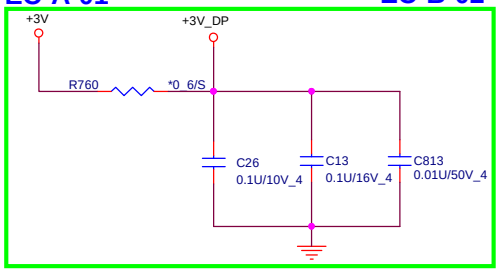
FOR ESD

Quanta Computer Inc.
PROJECT :

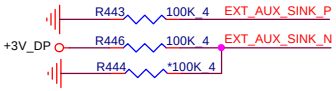
Size	Document Number	Rev
Custom	eDP LCD/CAMERA	3B

Date: Monday, October 17, 2016 Sheet 18 of 66

EC-A-01

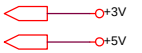


EC-B-02

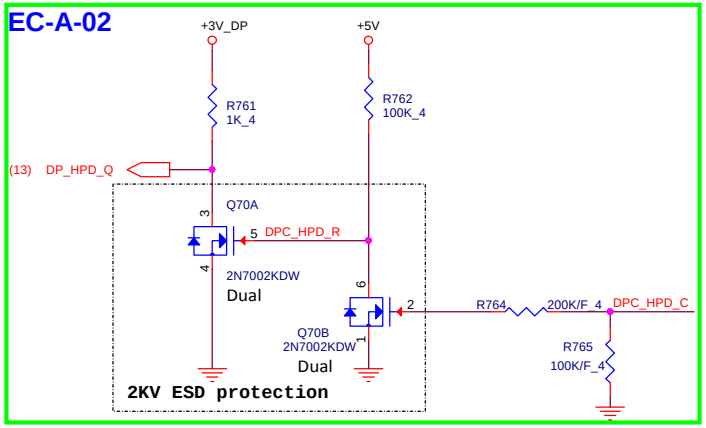


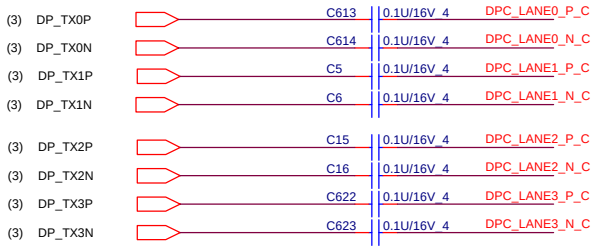
(10,11,12,13,14,16,17,18,20,21,22,23,24,26,27,28,29,30,31,32,36,43,45,50,52,9) +3V

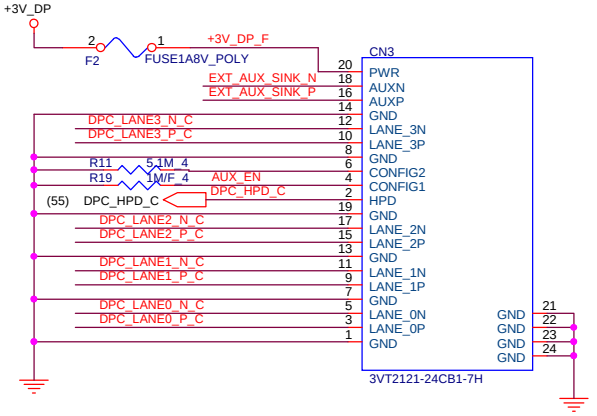
(20,21,22,24,30,31,43,45,52,63) +5V



EC-A-02



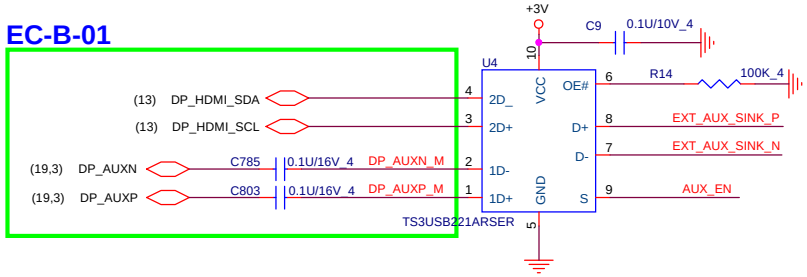




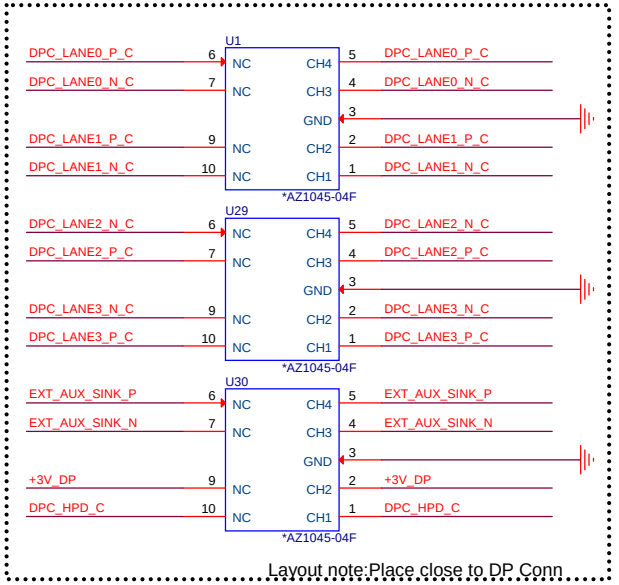
(19,3) DP_AUXP — R457 *0_4 — DP_AUXP_R — C628 *0.1U/16V_4 — EXT_AUX_SINK_P

(19,3) DP_AUXN — R456 *0_4 — DP_AUXN_R — C627 *0.1U/16V_4 — EXT_AUX_SINK_N

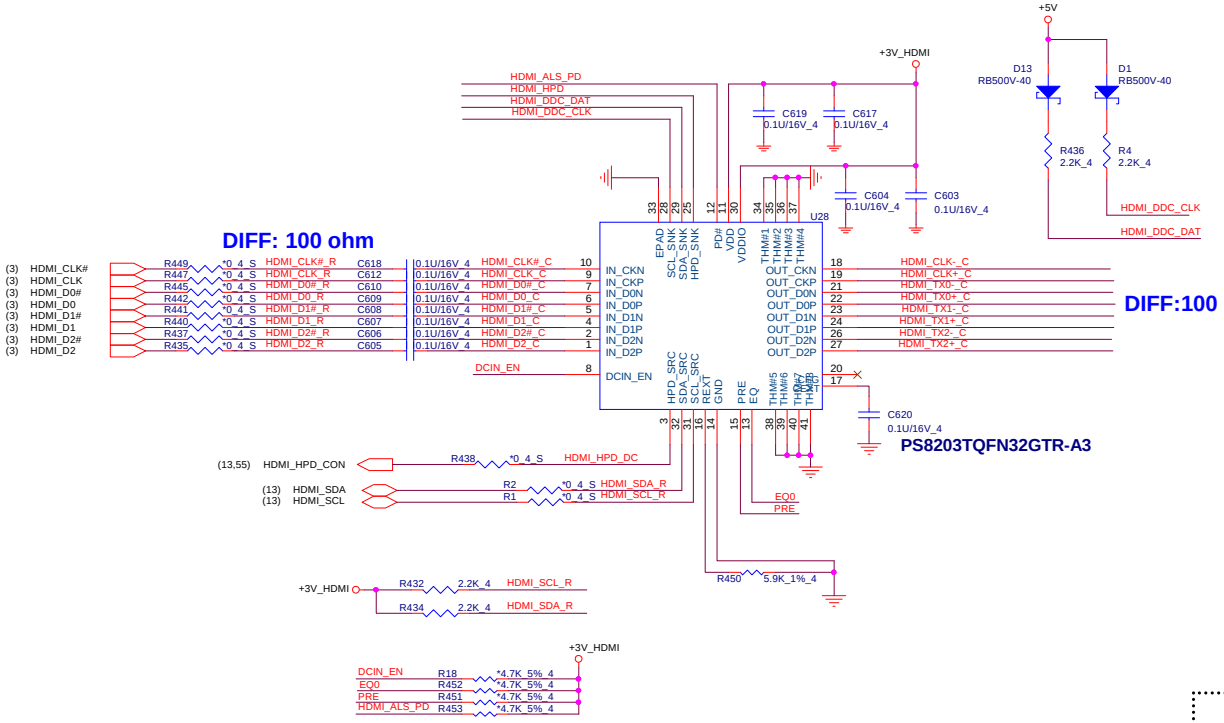
EC-B-01

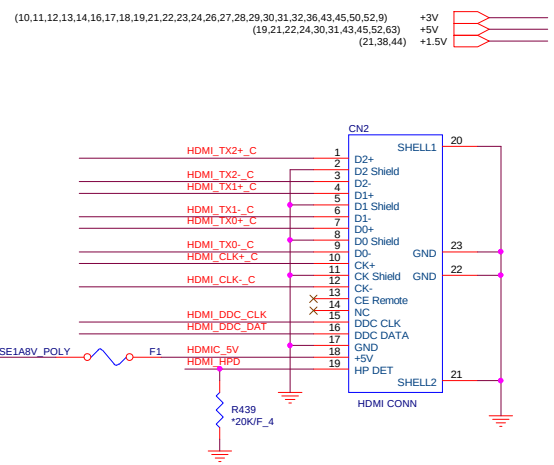


For ESD

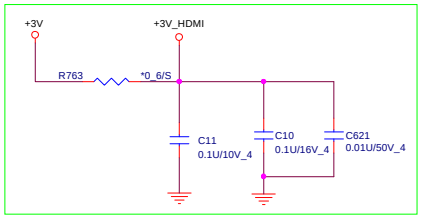


Quanta Computer Inc.		
PROJECT :		
Size: Custom	Document Number: DP Conn	Rev: 1A
Date: Friday, October 28, 2016	Sheet 19 of 66	

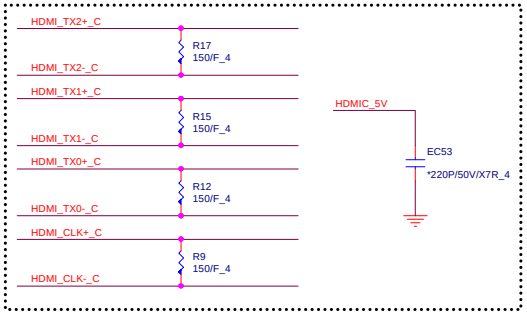




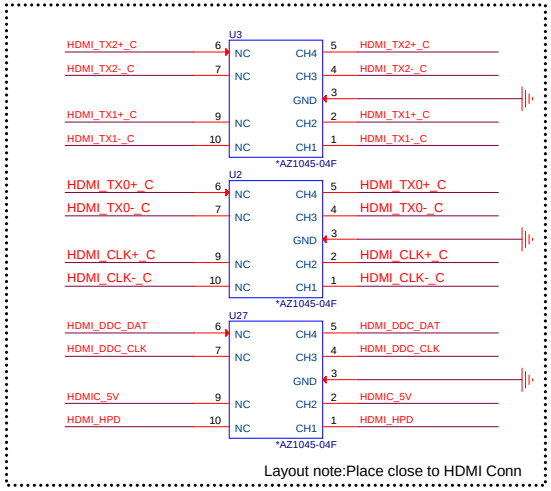
EC-A-03



EMI reserve for HDMI

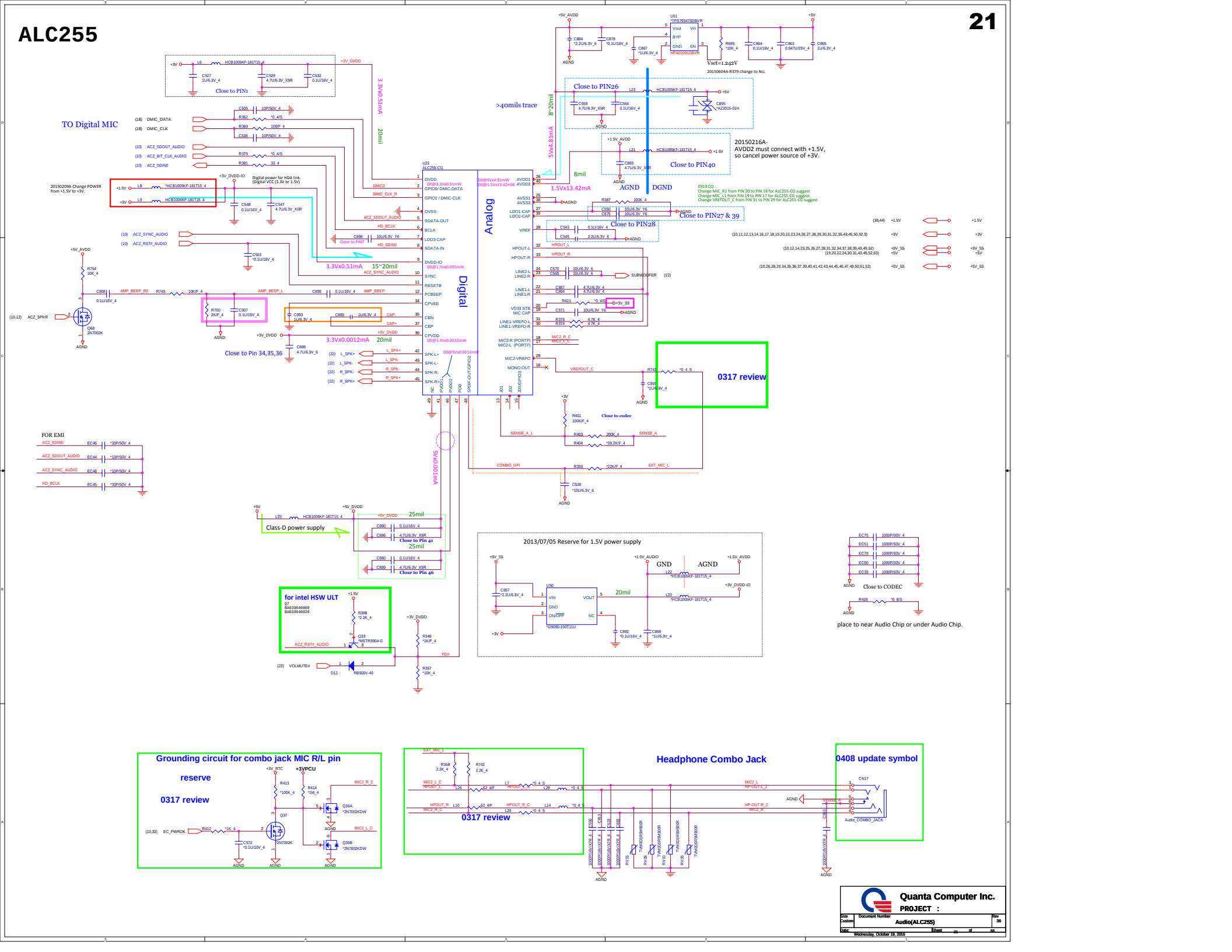


For ESD



Quanta Computer Inc.		
PROJECT :		
Size: Custom	Document Number: HDMI CONN	Rev: 3B
Date: Wednesday, November 02, 2016	Sheet 20 of 66	

ALC255


TO Digital MIC
Close to PIN1
Close to PIN26
Close to PIN40
Close to PIN27 & 39
Close to PIN28
Close to Pin 34,35,36
Close to Pin 7
Close to Pin 41
Close to Pin 46
Close to codec
Close to CODEC
place to near Audio Chip or under Audio Chip.
Analog
Digital
AGND
DGND
Vset=1.242V
20150604A-R379 change to NU.
20150216A-
AVDD2 must connect with +1.5V,
so cancel power source of +3V.
>40mils trace
1.5Vx13.42mA
3.3Vx0.51mA
3.3Vx0.0012mA
5Vx0.001mA
0317 review
FOR EMI
Class-D power supply
2013/07/05 Reserve for 1.5V power supply
for intel HSW ULT
Grounding circuit for combo jack MIC R/L pin
reserve
0317 review
Headphone Combo Jack
0408 update symbol
Quanta Computer Inc.
PROJECT :
Audio(ALC255)
Wednesday, October 19, 2016

Reserve for Input attenuation
To have optimization output power

Placement C4609
and then C4611

Close to IC

need to Close to connector
Reserve for EMI Depression

need to very
Close to IC

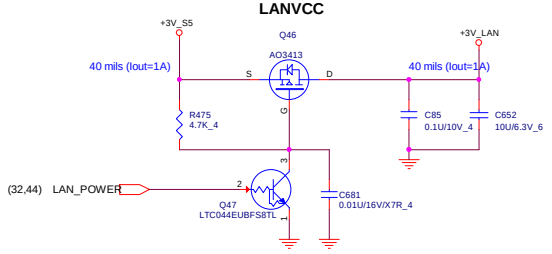
GND PAD 6 VIA (2x3)
inner 12mil, outer 20mil

Output Gain Table

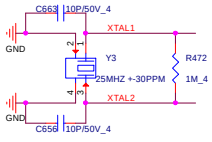
R364	R363	R373	R372	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

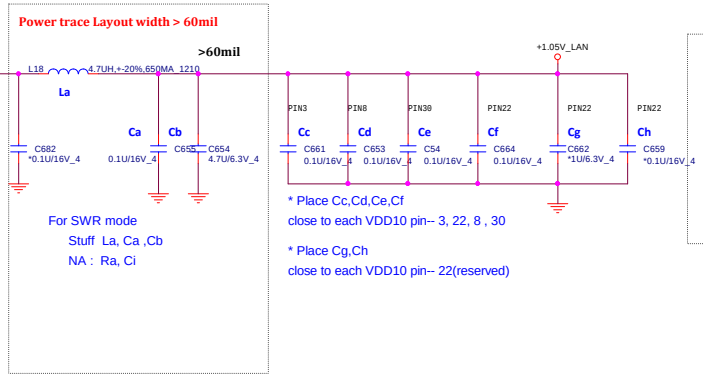
Quanta Computer Inc.	PROJECT :	
Size: Custom	Document Number: Amplifer(ALC1003)	Rev: 3B
Date: Wednesday, October 19, 2016	Sheet 22 of 66	

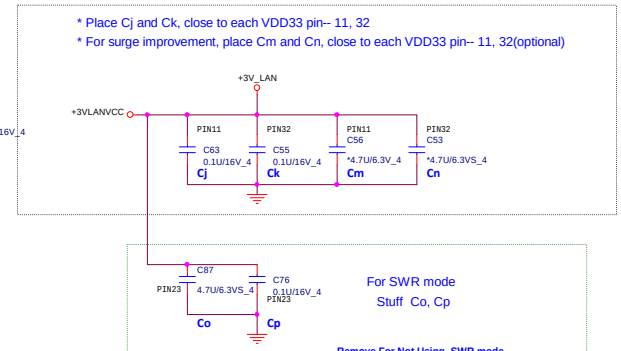
LANVCC

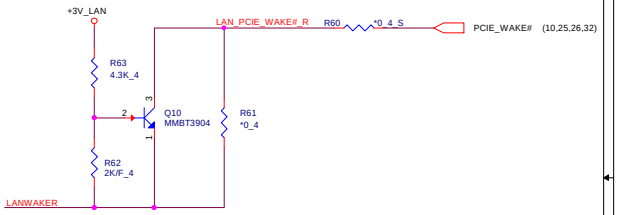


LANVCC
Trace width>60mil,
Trace length<200mil

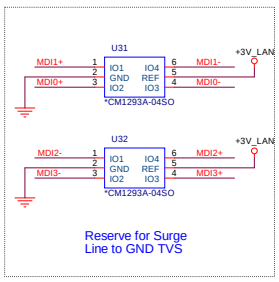






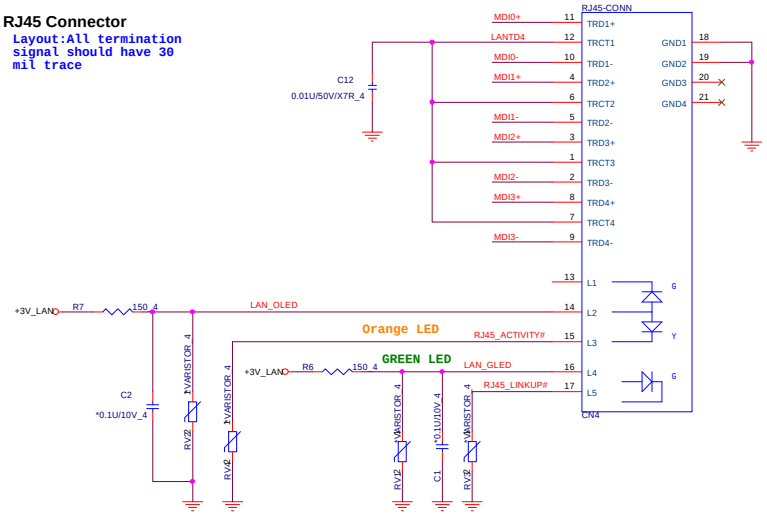


Tramsformer

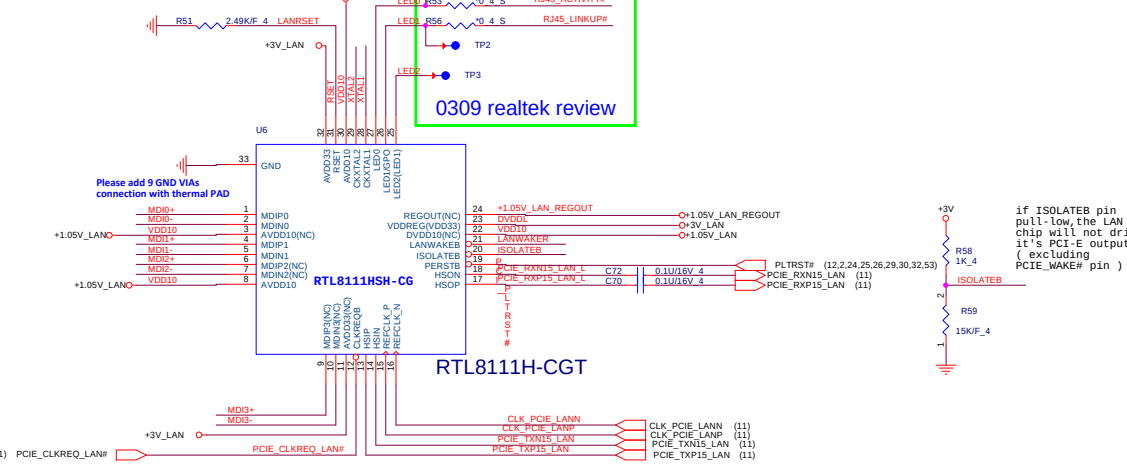


RJ45 Connector

Layout:All termination signal should have 30 mil trace



RJ45 Connector



Quanta Computer Inc.			
PROJECT :			
Size: Custom	Document Number: LAN(RTL8111GUS-CG)		Rev: 3B
Date: Wednesday, October 19, 2016	Sheet 23	of	66

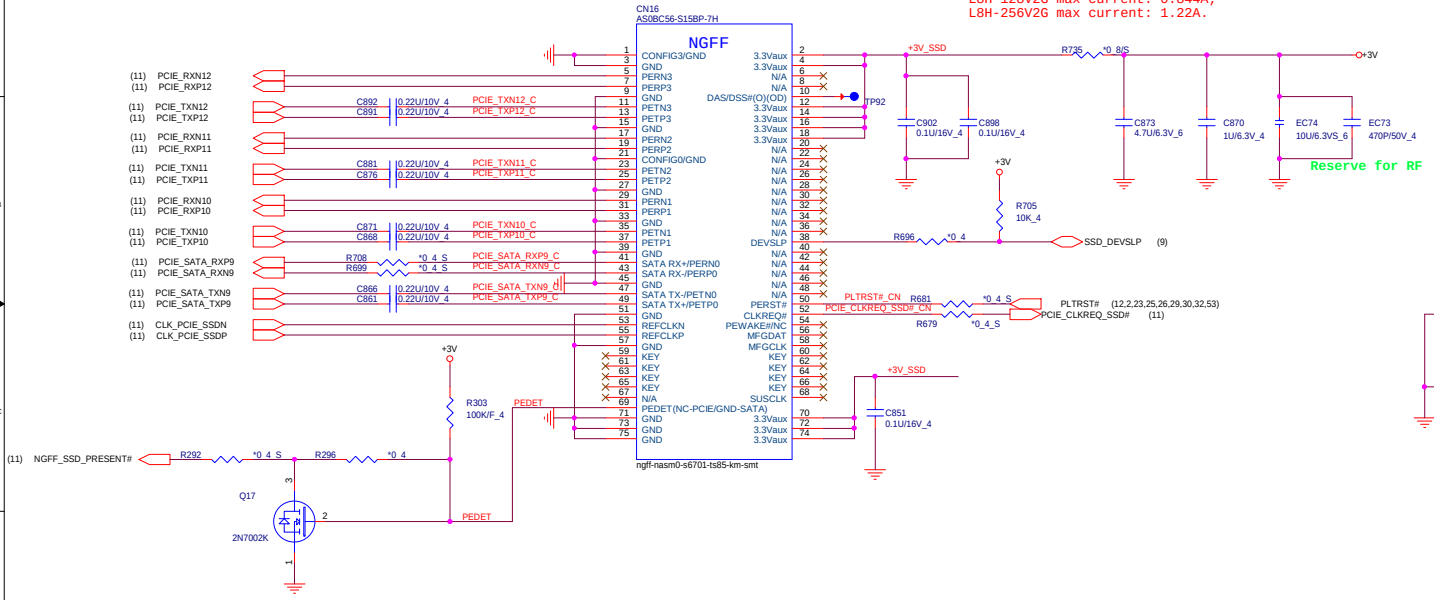
SSD

(10,11,12,13,14,16,17,18,19,20,21,22,23,26,27,28,29,30,31,32,36,43,45,50,52,9) +3V

(19,20,21,22,30,31,43,45,52,63) +5V

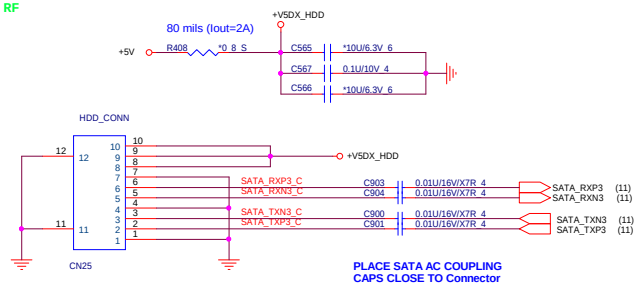
24

L8H-128V2G max current: 0.844A;
L8H-256V2G max current: 1.22A.



HDD

DC Current rating: 2 A (MAX)



PLACE SATA AC COUPLING CAPS CLOSE TO Connector

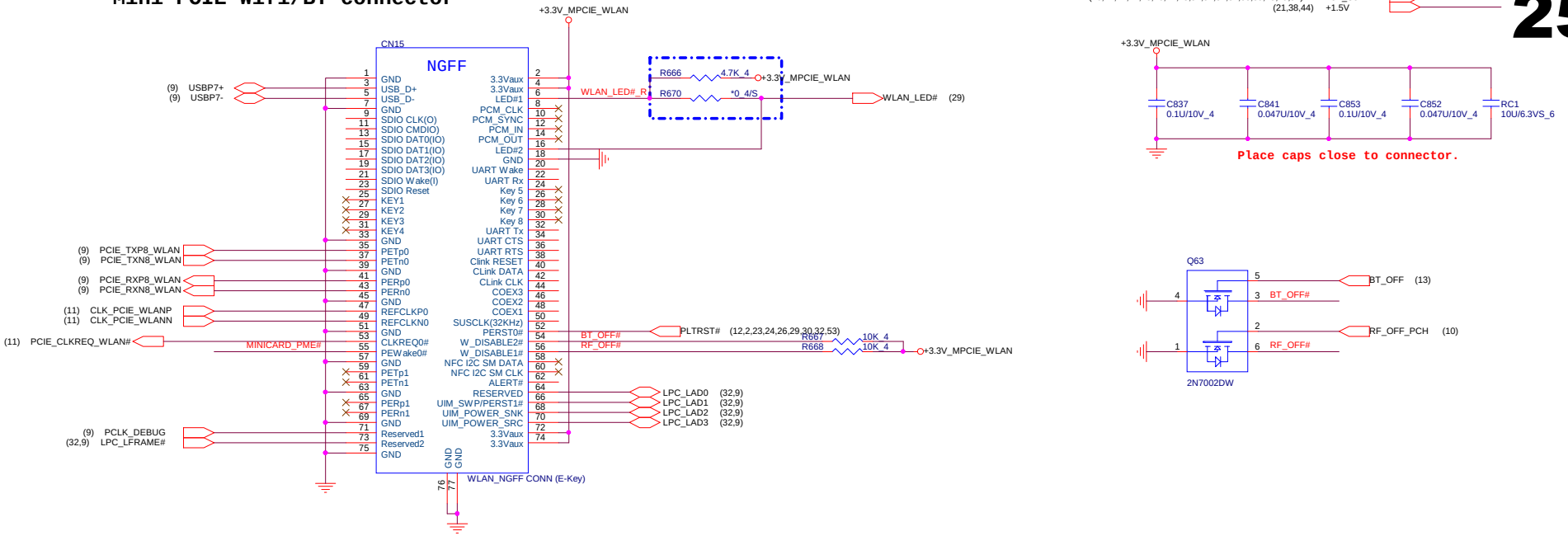
Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
Custom	SSD mSATA X2	3B

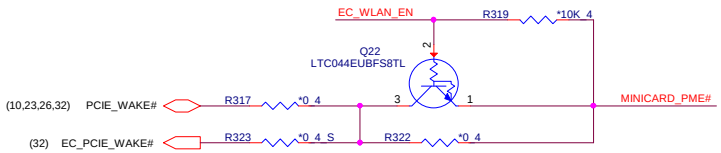
Date: Wednesday, October 19, 2016 Sheet 24 of 66

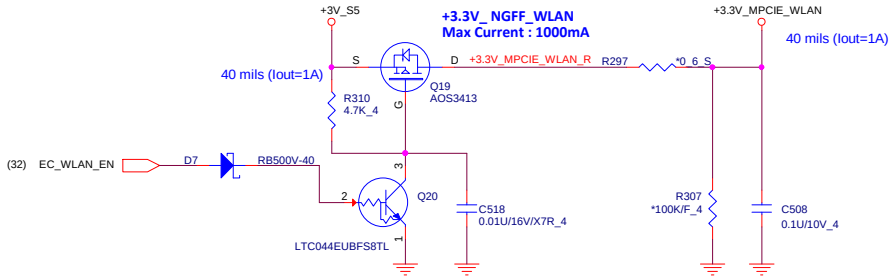
Mini PCIE Wifi/BT connector



(10,12,14,21,23,26,27,28,31,32,34,37,38,39,43,49,52) +3V_S5
(21,38,44) +1.5V

Place caps close to connector.





Quanta Computer Inc.		
PROJECT :		
Size: Custom	Document Number: Wifi/BT MiniPCIE	Rev: 3B
Date: Monday, October 17, 2016	Sheet 25 of 66	

Confirm package???

SPI FLASH

U44 W25X10CLSNIG (SOP8)1M

EC-A-06

EC-A-05

PCIE Gen3 < 2.5"

From Source side

+1.2V Max:705mA

+3V Max:275mA

USB3.1 < 2"

For USB3.1 Type C

For USB3.1 Type A

12/04 EE Control Table

0322 review
Pin13,Pin14,Pin16,Pin17 NC

ASM1142

Max:5mA

+1.2_S5 for ASM1142

0.033A

Power On Sequence

OCI#

+1.2V_S5/+3V_S5

+1.2V/+3V

U3P1_PORST#

<10mS

>50mS

>2mS <80mS

H/W Strapping

UR_TX	UR_RX	Function
1	1	Asynchronous Mode with External 20MHz Crystal

U3P1_SPI_CLK	Function
1	1:D3cold (default)
0	0:D3Hot

0322 review

For ESD

High Actice

Place CAP,close to USB3.1 CONN

USB3.1 typeA

USB3.0 CONN

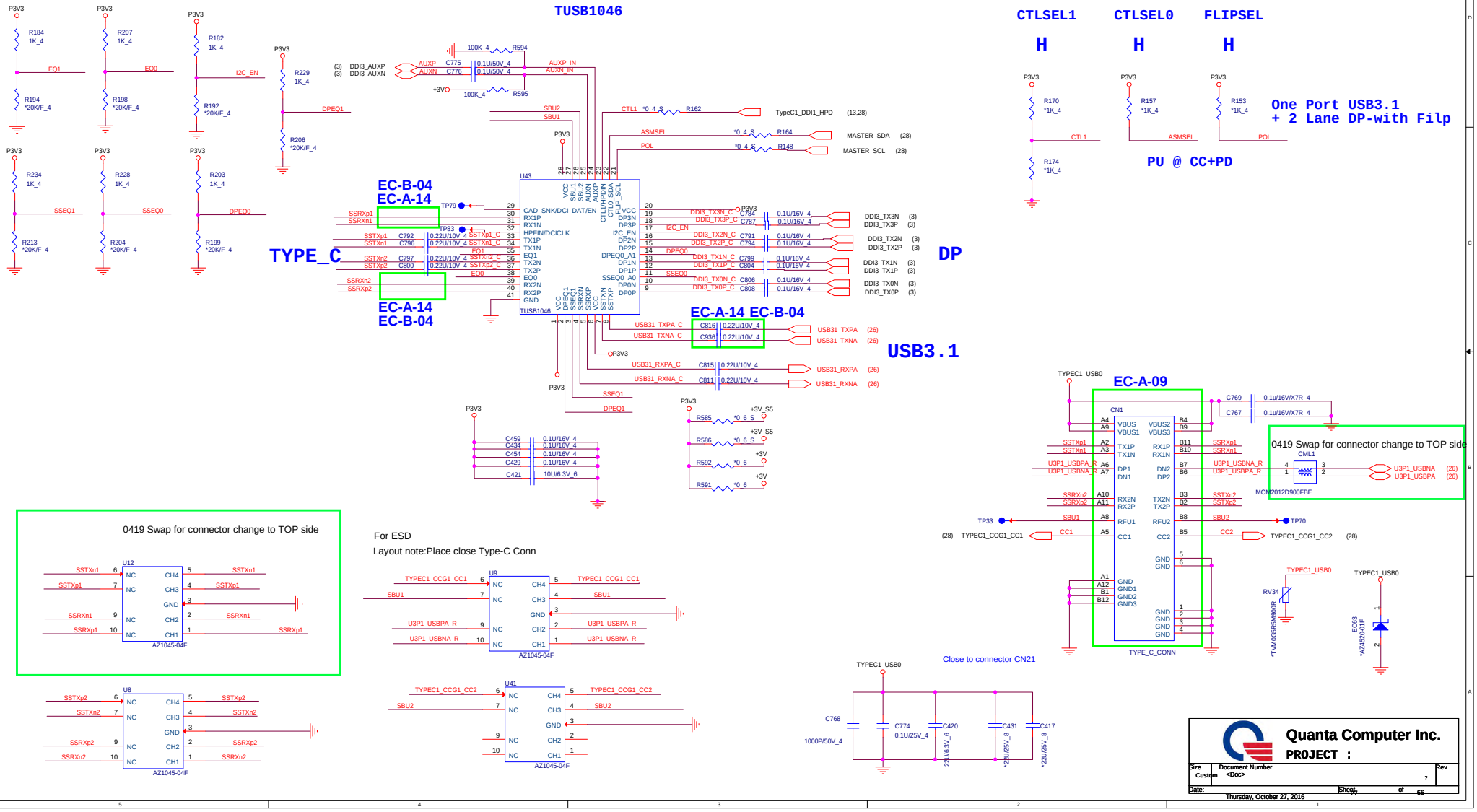
Quanta Computer Inc.

PROJECT : NL8E

Size: | Document Number: USB3.1 HOST IC | Rev: 1A

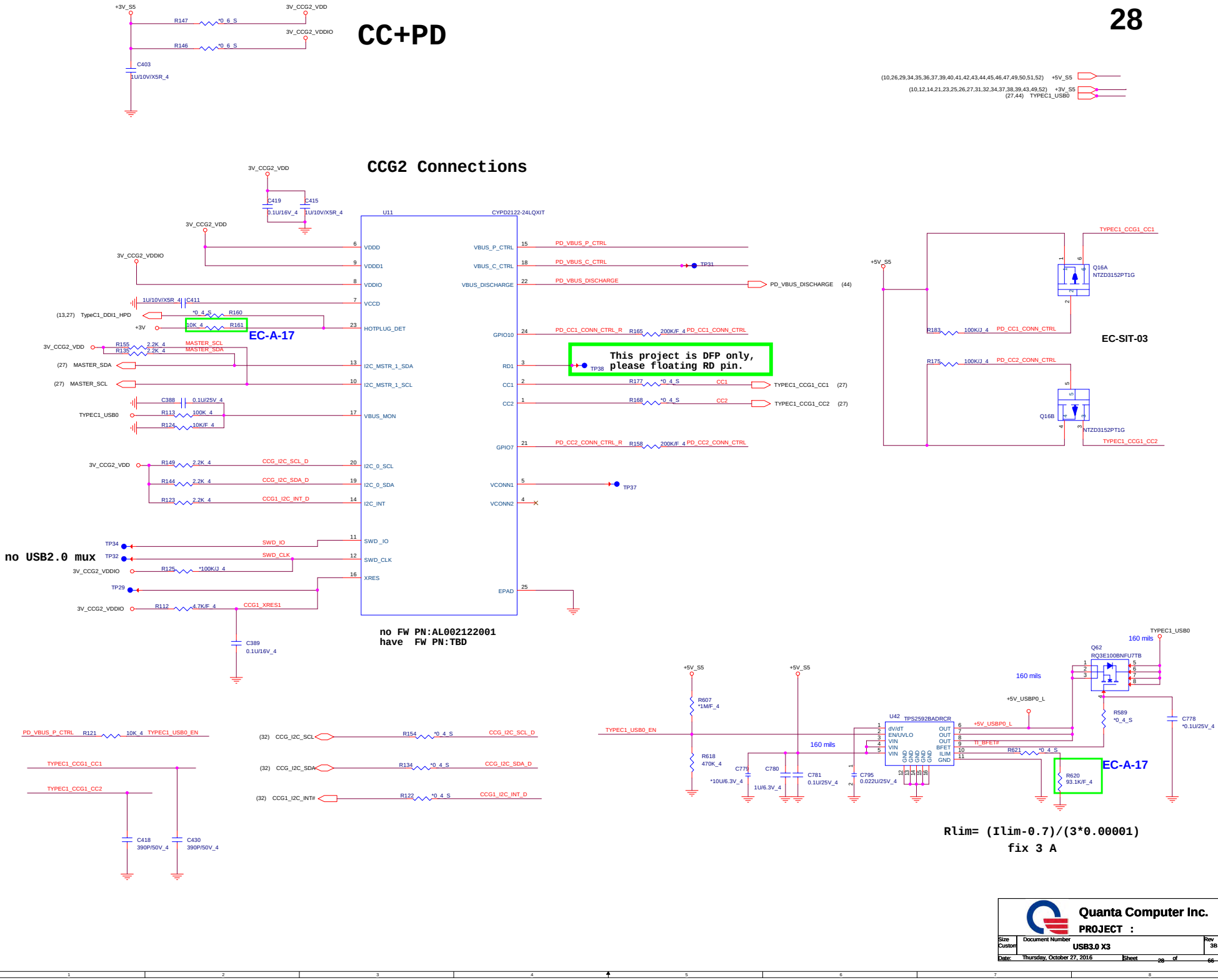
Date: Thursday, October 27, 2016 | Sheet 26 of 66

Mux


TUSB1046
CTLSEL1
CTLSEL0
FLIPSEL
H
H
H
One Port USB3.1
+ 2 Lane DP-with Filp
PU @ CC+PD
TYPE_C
DP
USB3.1
EC-B-04
EC-A-14
EC-A-14
EC-B-04
EC-A-14 EC-B-04
EC-A-09
0419 Swap for connector change to TOP side
For ESD
Layout note:Place close Type-C Conn
Close to connector CN21
Quanta Computer Inc.
PROJECT :
Thursday, October 27, 2016

CC+PD

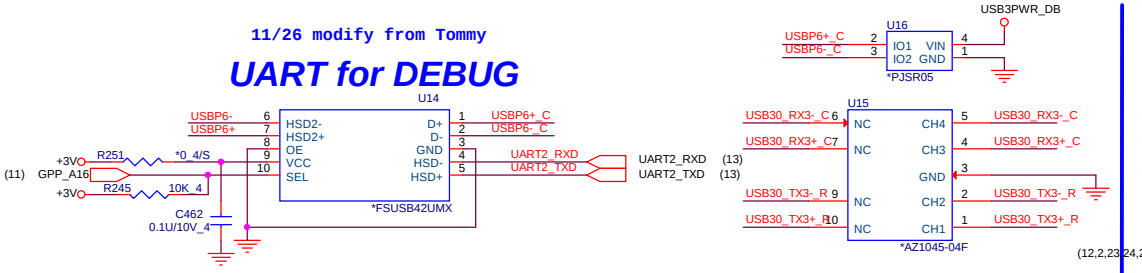
CCG2 Connections



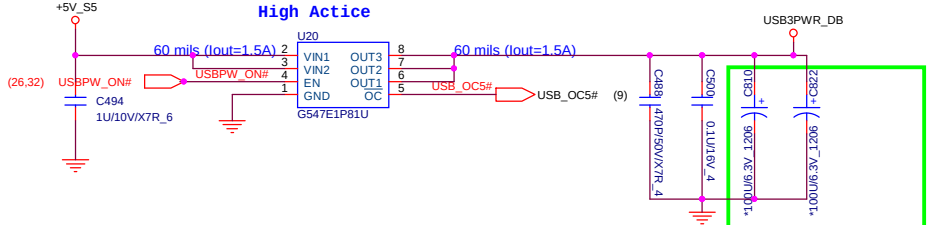
Quanta Computer Inc.	
PROJECT :	
Size: Custom	Document Number: USB3.0 X3
Rev: 3B	
Date: Thursday, October 27, 2016	Sheet 28 of 66

11/26 modify from Tommy

UART for DEBUG

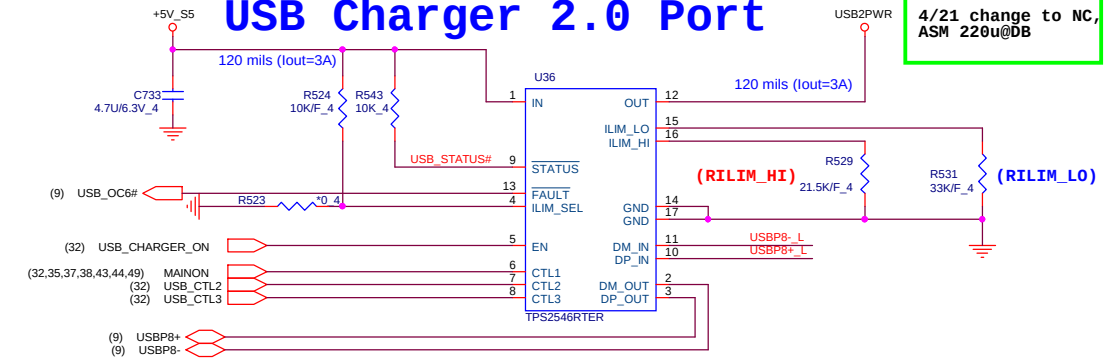


High Actice



USB Charger 2.0 Port

4/21 change to NC, ASM 220u@DB

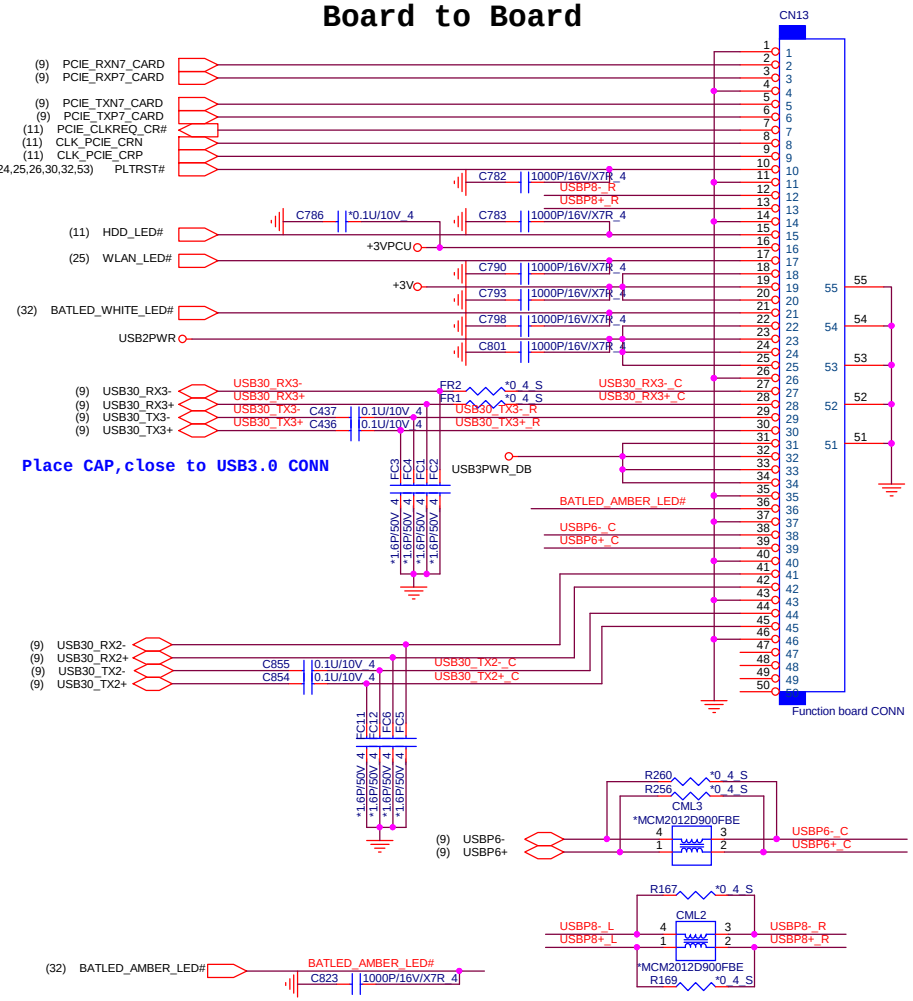


RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$I_{OS\_typ}(mA) = \frac{50{,}500}{(R_{ILIM\_XX}(k\Omega) + 0.1)}$$

(10,26,28,34,35,36,37,39,40,41,42,43,44,45,46,47,49,50,51,52) +5V_S5
(10,11,12,13,14,16,17,18,19,20,21,22,23,24,26,27,28,30,31,32,36,43,45,50,52,9) +3V

Board to Board



Quanta Computer Inc.

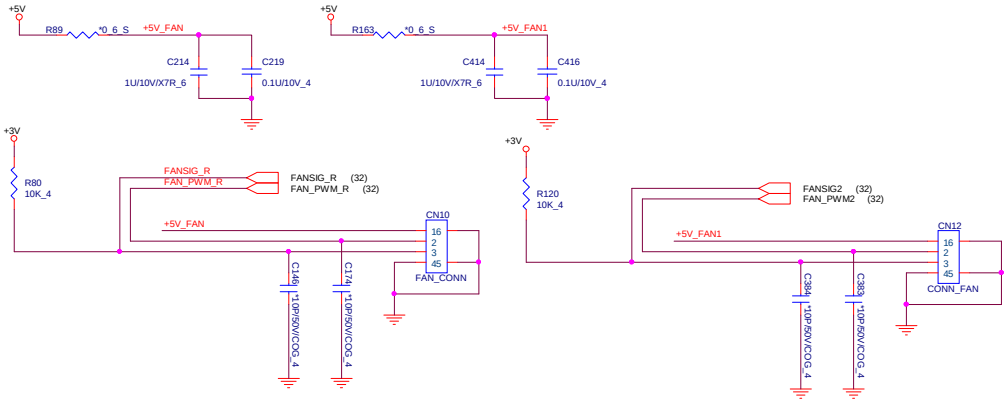
PROJECT :

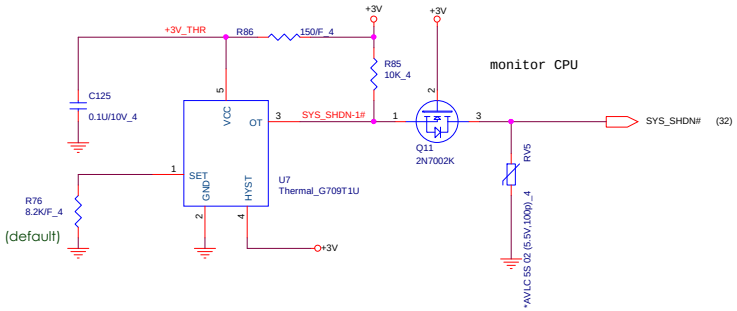
Size	Document Number	Rev
Custom	USB2.0 X1/FUNCTION B	3B
Date: Monday, October 17, 2016	Sheet 29 of 66	

FAN CONTROL

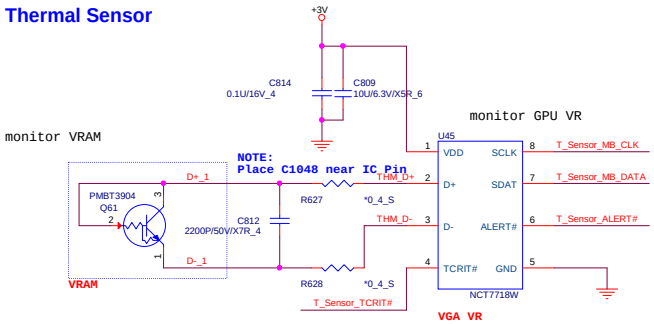
(10,11,12,13,14,16,17,18,19,20,21,22,23,24,26,27,28,29,31,32,36,43,45,50,52,9) +3V
(19,20,21,22,24,31,43,45,52,63) +5V

Thermal Sensor

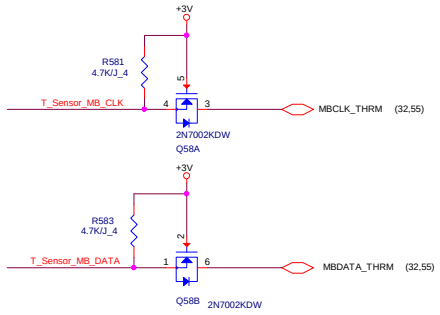


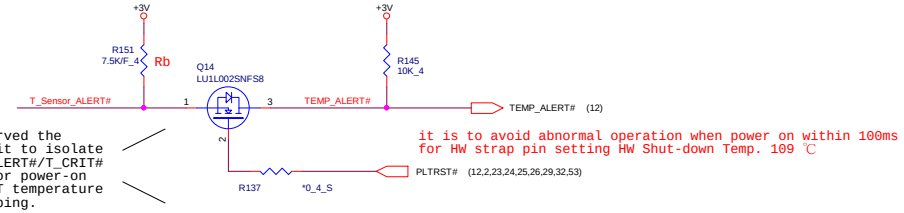


Thermal Sensor



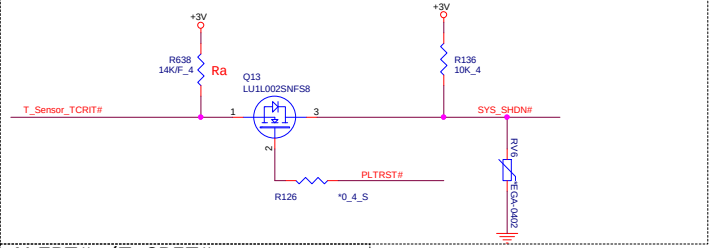
ADDRESS: 98





*Reserved the circuit to isolate the ALERT#/T_CRIT# pin for power-on T_CRIT temperature strapping.

it is to avoid abnormal operation when power on within 100ms for HW strap pin setting HW Shut-down Temp. 109 ℃



ALERT# /T_CRIT#
Pull-up Resistor

Rb \ Ra	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

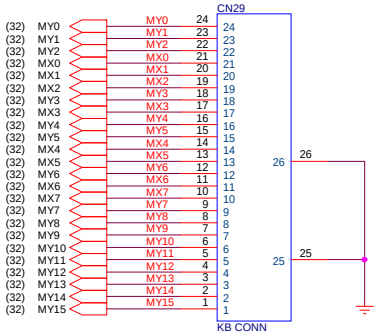
T_CRIT temperature strapping point

Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
Custom	FAN/Thermal	3B

Date: Monday, October 17, 2016 Sheet 30 of 66

KEYBOARD

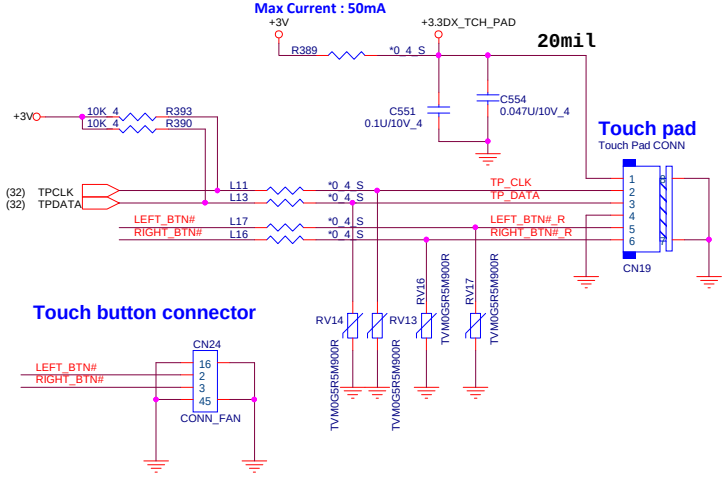


For EMI

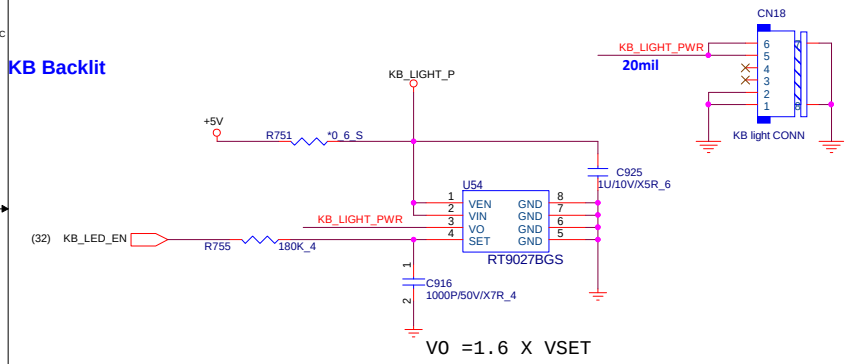
MY15	C593	220P/50V/X7R_4	C591	220P/50V/X7R_4	MY13
MY10	C588	220P/50V/X7R_4	C590	220P/50V/X7R_4	MY12
MY11	C589	220P/50V/X7R_4	C600	220P/50V/X7R_4	MY3
MY14	C592	220P/50V/X7R_4	C582	220P/50V/X7R_4	MY6
MX0	C597	220P/50V/X7R_4	C598	220P/50V/X7R_4	MX1
MY1	C595	220P/50V/X7R_4	C584	220P/50V/X7R_4	MX7
MY5	C579	220P/50V/X7R_4	C583	220P/50V/X7R_4	MX6
MX3	C601	220P/50V/X7R_4	C587	220P/50V/X7R_4	MY9
MX2	C599	220P/50V/X7R_4	C586	220P/50V/X7R_4	MY8
MY0	C594	220P/50V/X7R_4	C585	220P/50V/X7R_4	MY7
MX5	C581	220P/50V/X7R_4	C578	220P/50V/X7R_4	MY4
MX4	C580	220P/50V/X7R_4	C596	220P/50V/X7R_4	MY2

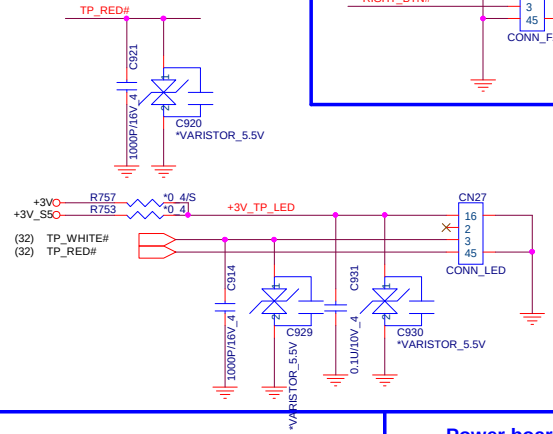
(19,20,21,22,24,30,43,45,52,63) +5V
(10,11,12,13,14,16,17,18,19,20,21,22,23,24,26,27,28,29,30,32,36,43,45,50,52,9) +3V
(10,21,29,32,33,34,55) +3VPCU
(10,12,14,21,23,25,26,27,28,32,34,37,38,39,43,49,52) +3V_S5

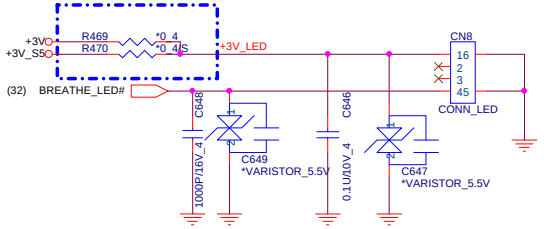
+3V_TP
Max Current : 50mA



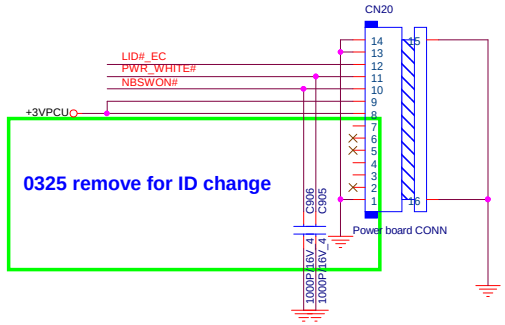
KB Backlit



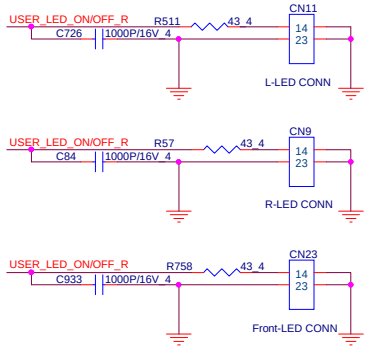




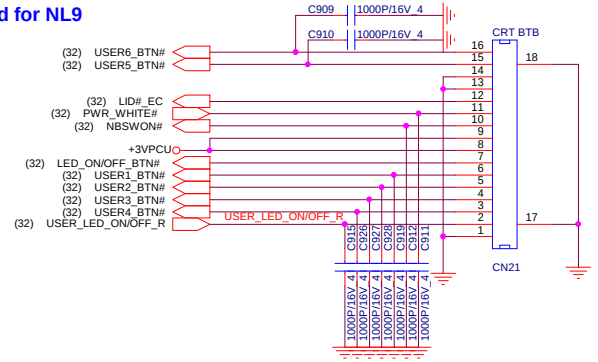
Power board for NL8



LED CONN

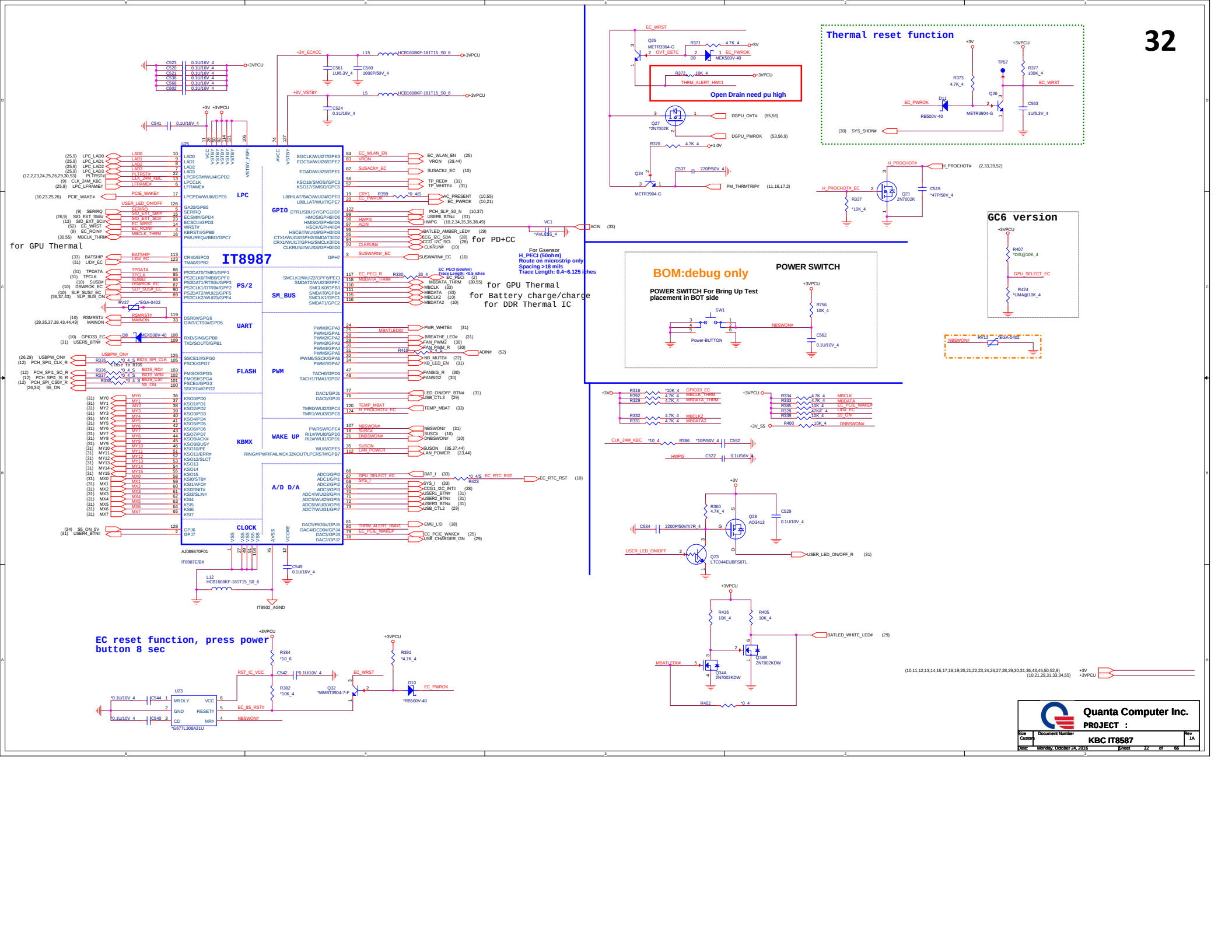


Power board for NL9



Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
Custom	KB/TP/LID	3B
Date: Monday, October 24, 2016	Sheet 31 of 66	


IT8987
for GPU Thermal
for PD+CC
for GPU Thermal
for Battery charge/charge
for DDR Thermal IC
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
Thermal reset function
Open Drain need pu high
POWER SWITCH
BOM:debug only
POWER SWITCH For Bring Up Test placement in BOT side
GC6 version
EC reset function, press power button 8 sec
Quanta Computer Inc.
PROJECT :
KBC IT8587

(52) +VA
(18,34,35,36,39,40,41,42,47,50,52,63) +VIN
(10,21,29,31,32,34,55) +3VPCU

230W for N17E-G1 ; N17P-G1
180W for N16E-GT (970M)
150W for N16P-GX (960M) ; N16E-GS (965M)
120W for N16P-GT (950M)

System Adaptor
DC-IN

CN7
51202-00901-V01

Do Not add test pad on BATDIS_G signal

EMI request for ISN

5m ohm for 180W adapter

Place this ZVS close to Diode away +VIN

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

For ISN

BQ24780SRUYR

ACDET=17.2V

VIDCHG = 8 or 16 × (VSRN – VSRP)

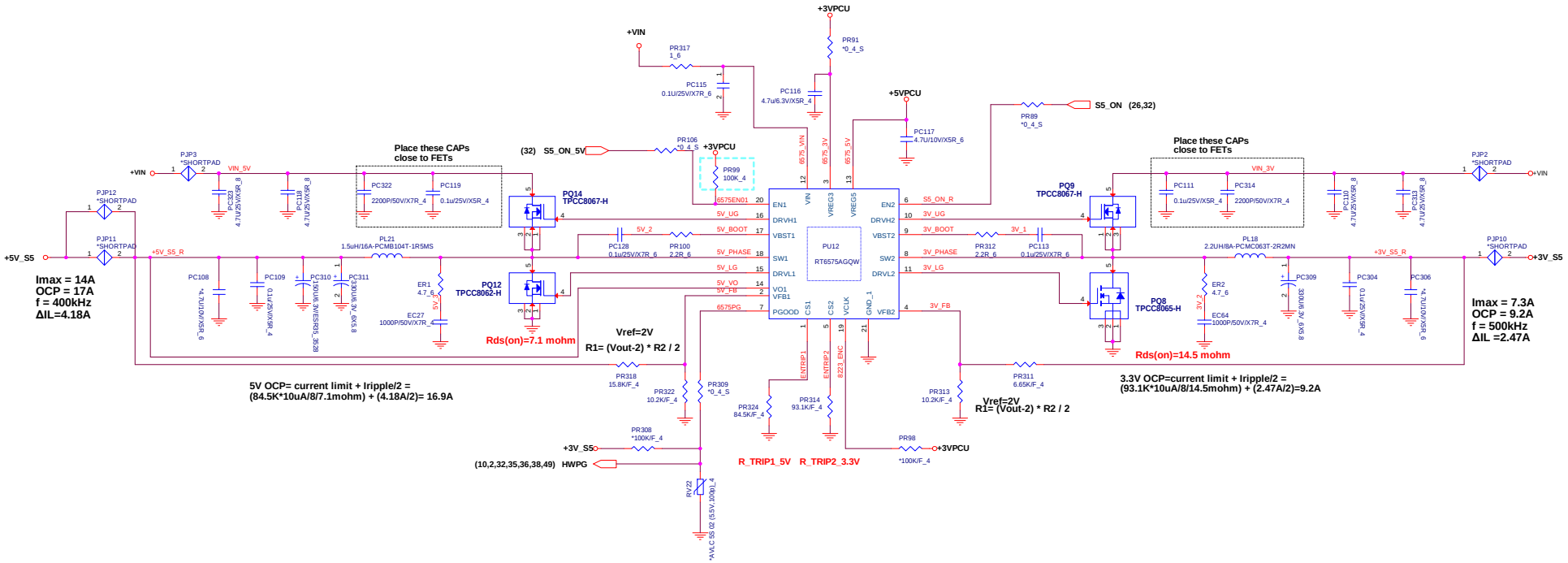
Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

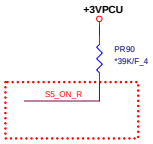
Quanta Computer Inc.			
PROJECT :			
Size: Custom	Document Number: Charger (BQ24780S)		Rev: 3B
Date: Friday, October 28, 2016	Sheet: 33	of: 66	

(18,33,35,36,39,40,41,42,47,50,52,63) +VIN
(10,26,28,29,35,36,37,39,40,41,42,43,44,45,46,47,49,50,51,52) +5V_S5
(10,21,29,31,32,33,55) +3VPCU
(10,12,14,21,23,25,26,27,28,31,32,37,38,39,43,49,52) +3V_S5



L/S Mosfet parameter

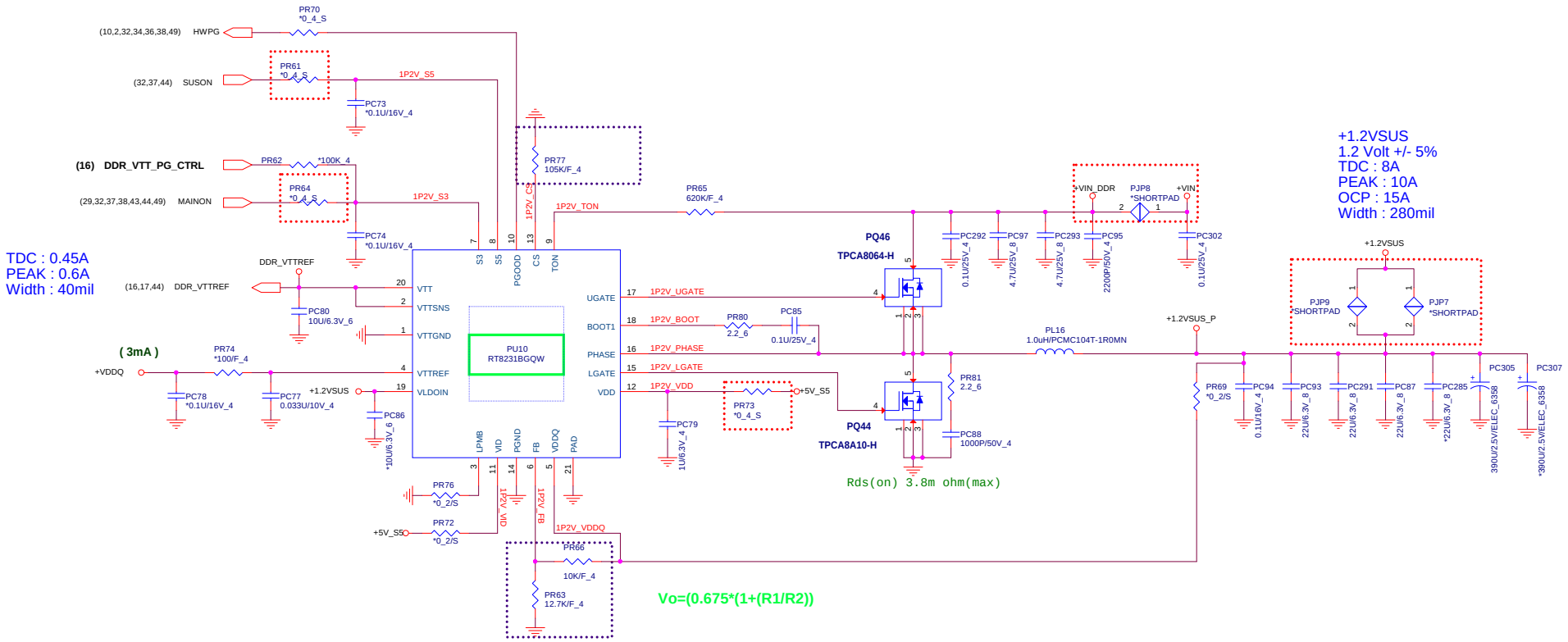
MOSFET	Package	ID (Ta=25C)	Rds_on_max
TPCC8067-H	DFN3x3	9A	26m
TPCC8062-H	DFN3x3	27A	7.1m



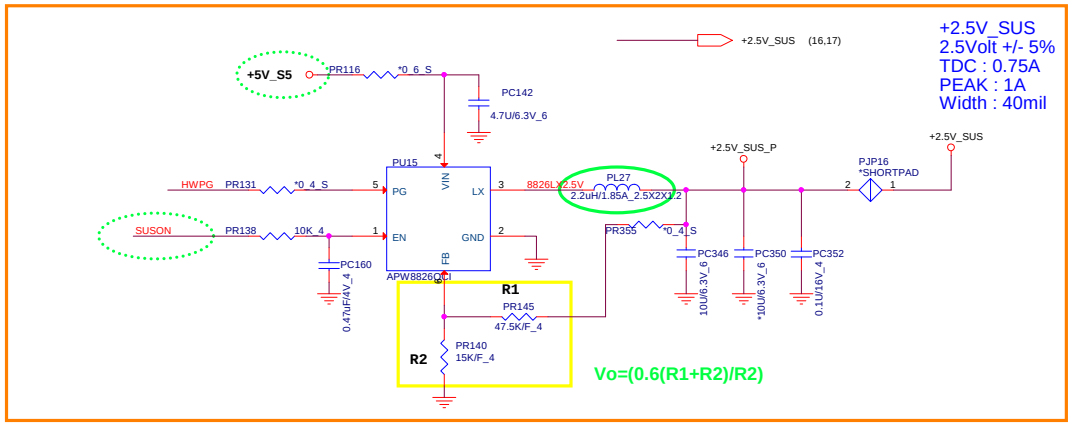
Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
Custom	3V/5V (TPS51285BRUKR)	3B
Date: Thursday, October 27, 2016	Sheet 34 of 66	

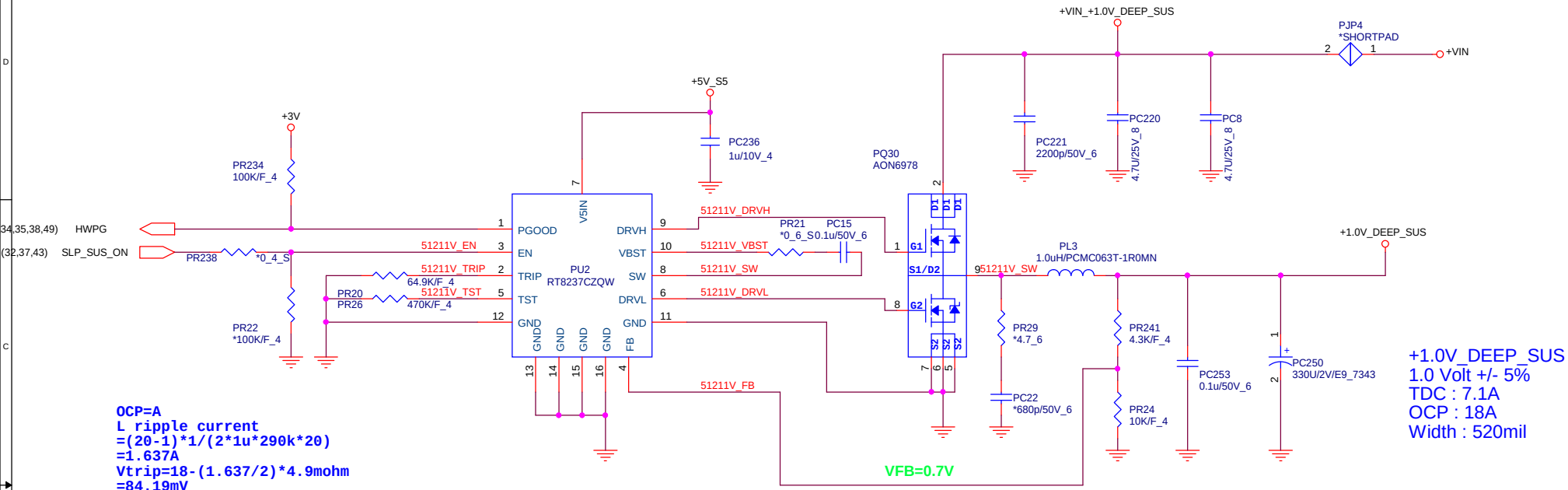
(10,16,17,2,43,44,50,6) +1.2VSUS
(10,26,28,29,34,36,37,39,40,41,42,43,44,45,46,47,49,50,51,52) +5V_S5
(18,33,34,36,39,40,41,42,47,50,52,63) +VIN



7/09 Chaneg DDR3L to DDR4
Adding +2.5V Power Rail



Quanta Computer Inc.		
PROJECT :		
Size: Custom	Document Number: DDR3 (RT8231B)	Rev: 3B
Date: Thursday, October 27, 2016	Sheet 35 of 66	

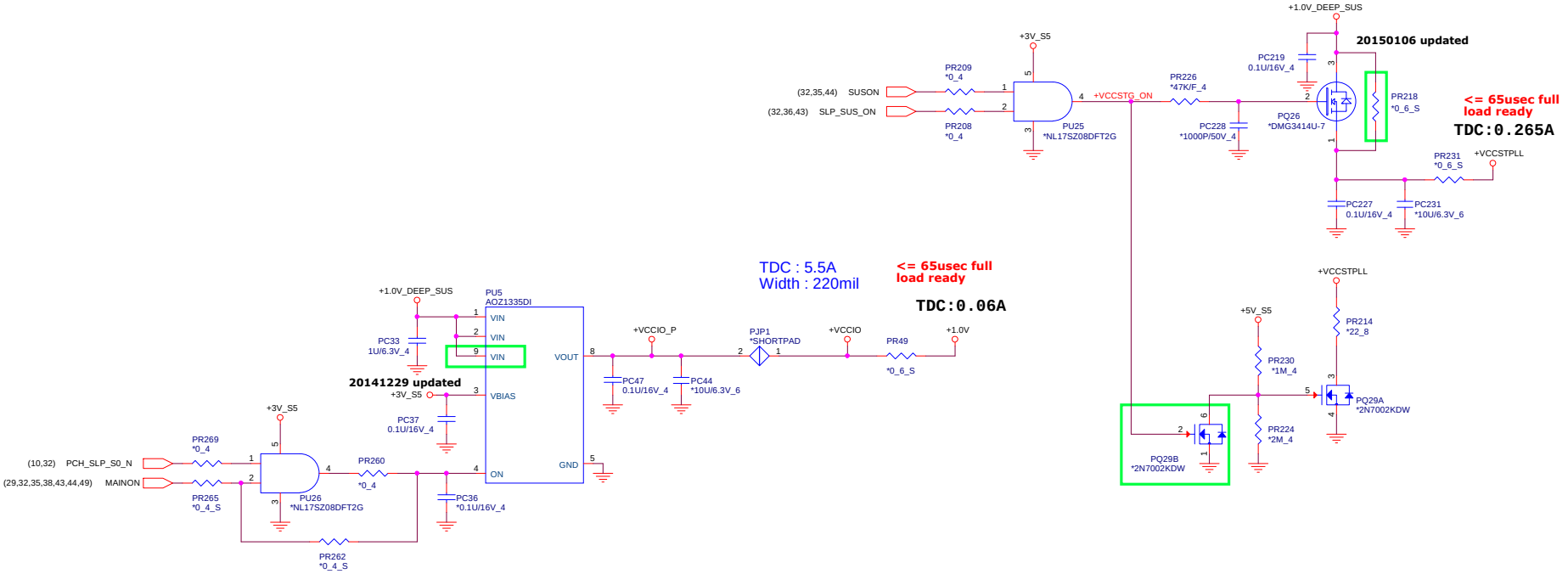


OCP=A
L ripple current
=(20-1)*1/(2*1u*290k*20)
=1.637A
Vtrip=18-(1.637/2)*4.9mohm
=84.19mV
Rlimit=84.19mV/10uA*8= 67.3Kohm

+1.0V_DEEP_SUS
1.0 Volt +/- 5%
TDC : 7.1A
OCP : 18A
Width : 520mil

Quanta Computer Inc.		
PROJECT : NL8E		
Size	Document Number: +1V_S5 (RT8237CZQW)	Rev: 1A
Date: Thursday, October 27, 2016	Sheet 36 of 66	

+1.0V (10,2,32,6)
+3V_S5 (10,12,14,21,23,25,26,27,28,31,32,34,38,39,43,49,52)
+5V_S5 (10,26,28,29,34,35,36,39,40,41,42,43,44,45,46,47,49,50,51,52)
+VCCIO (3,6)
+VCCSTPLL (11,2,6)
+1.0V_DEEP_SUS (10,11,14,36,39,44)



NB5

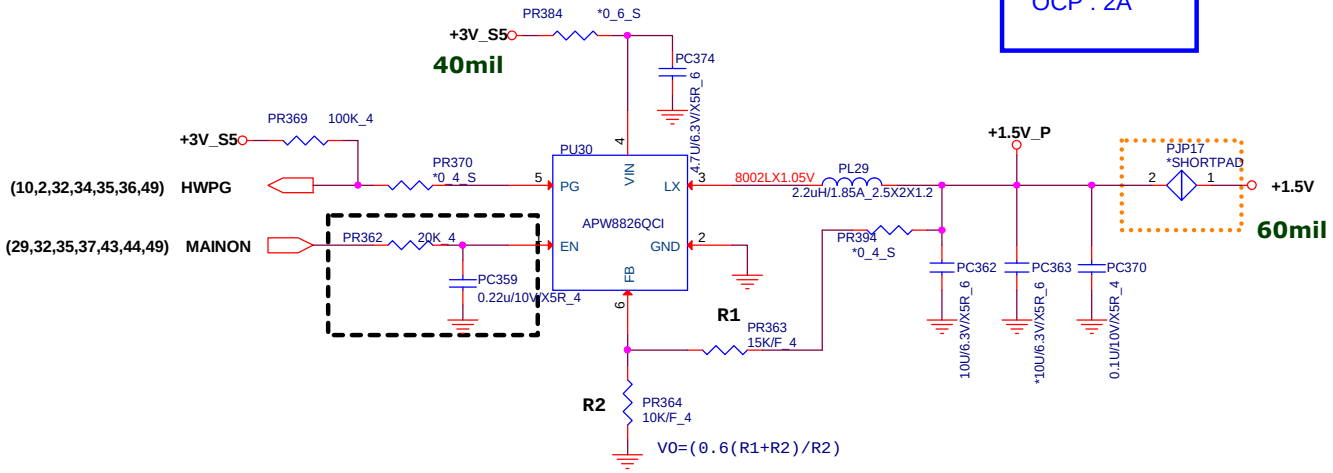
PROJECT : X1B-10L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A

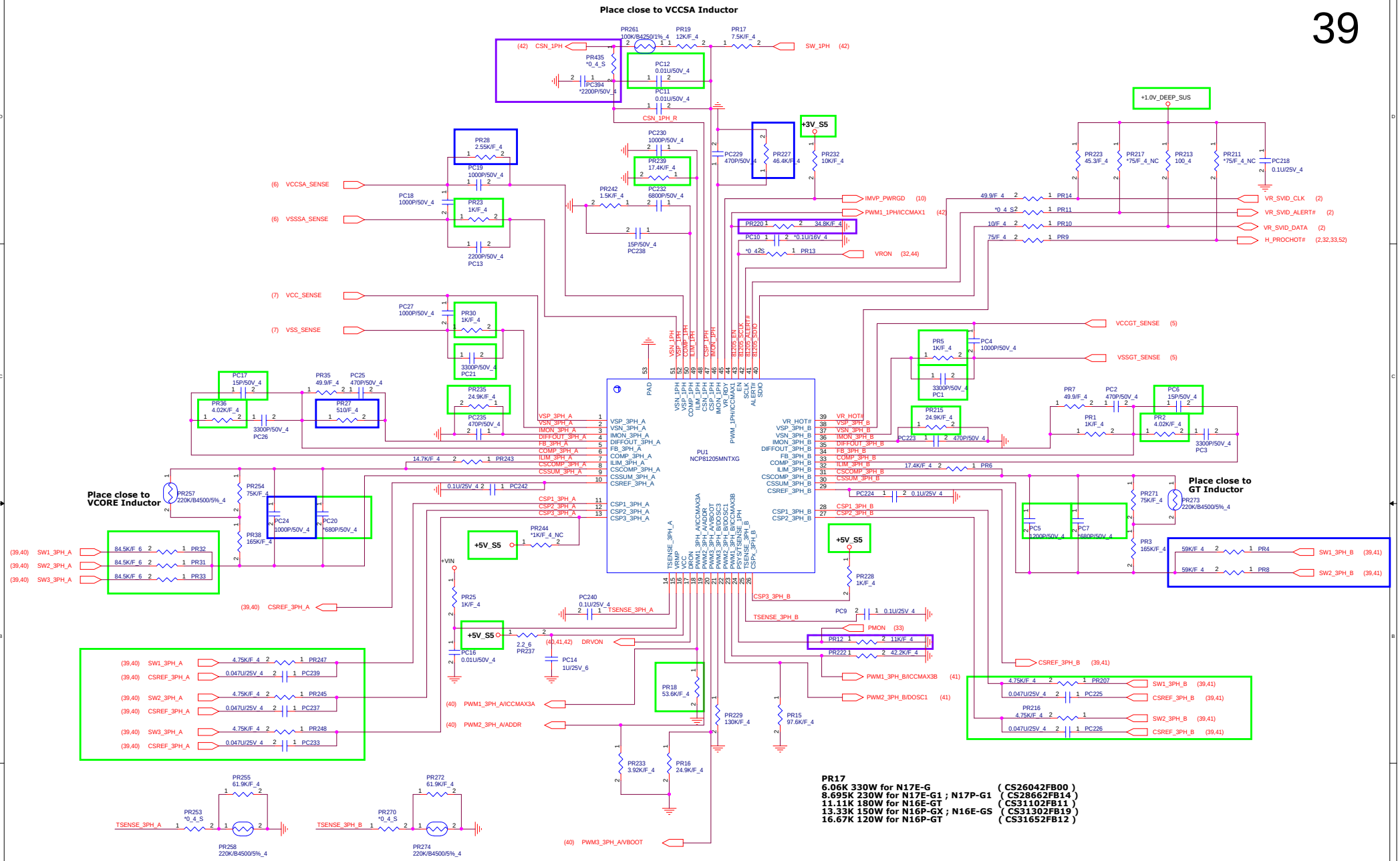
Date: Thursday, October 27, 2016 | Sheet 37 of 66

(10,26,28,29,34,35,36,37,39,40,41,42,43,44,45,46,47,49,50,51,52) +5V_S5
(18,33,34,35,36,39,40,41,42,47,50,52,63) +VIN

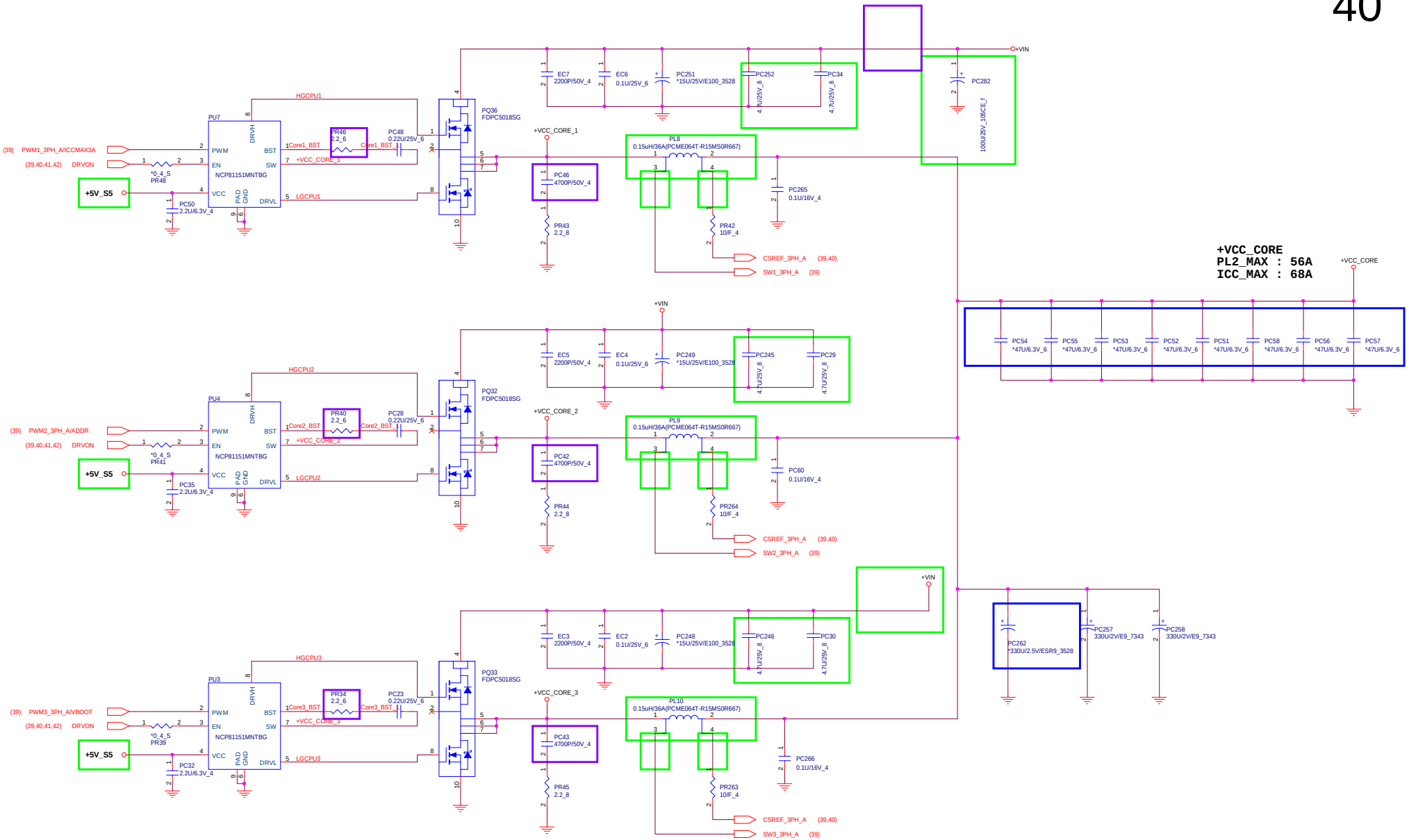
+1.5V
Fsw : 1.5MHz
Peak : 1A
OCP : 2A



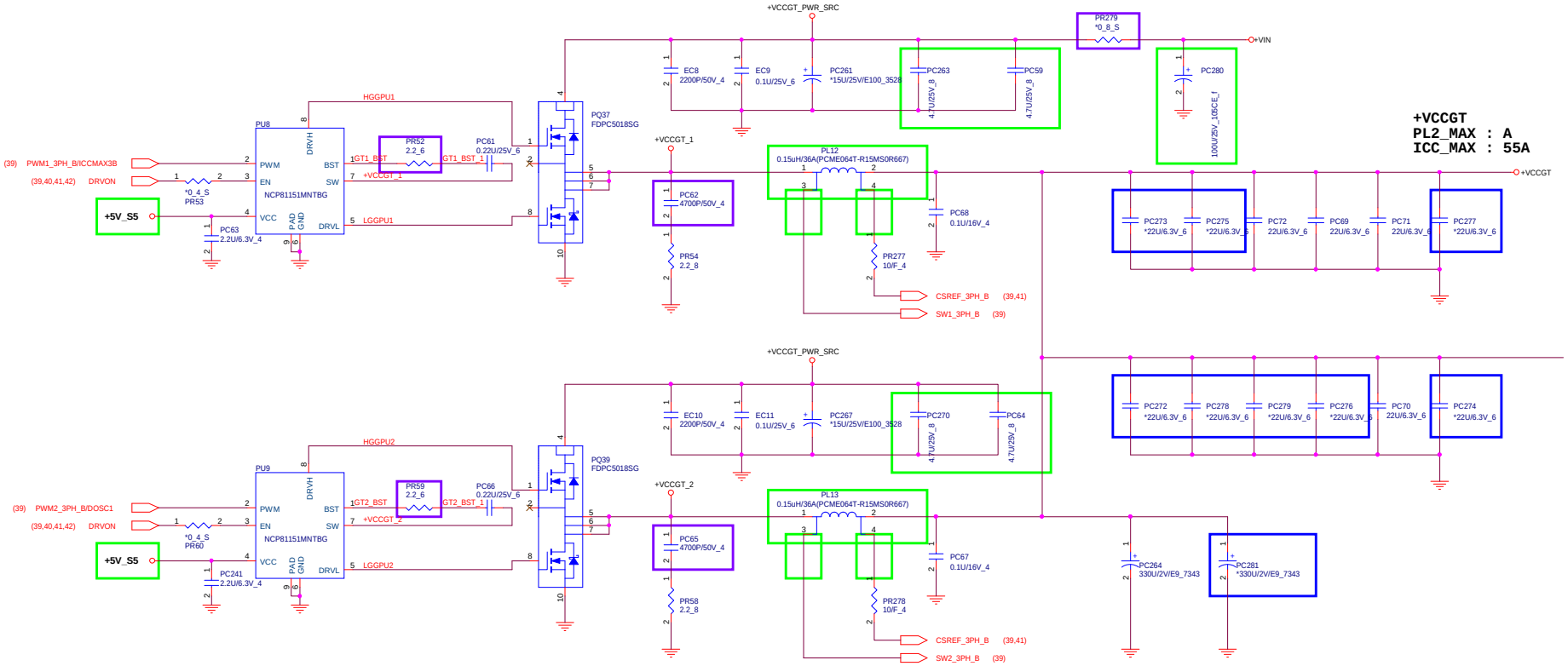
Quanta Computer Inc.		
PROJECT :		
Size: Custom	Document Number: +1.8V (APW8713)	Rev: 3B
Date: Thursday, October 27, 2016	Sheet 38 of 66	



Quanta Computer Inc.		
PROJECT : NL8E		
Size	Document Number	Rev
	IMVP8 VR (NCP81205)	A
Date: Friday, October 28, 2016	Sheet 39 of 66	



Quanta Computer Inc.			
PROJECT : NL8E			
Size	Document Number		Rev
	VCCIA 3-Phase Power Stage		A
Date: Thursday, October 27, 2016		Sheet 40 of 66	

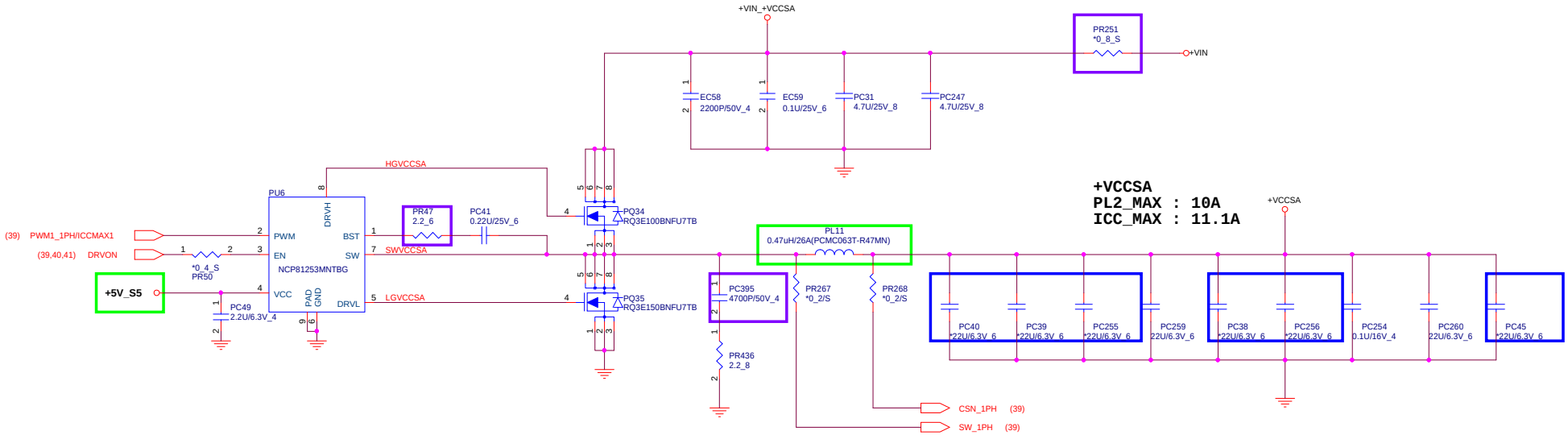


Quanta Computer Inc.

PROJECT : NL8E

Size	Document Number	Rev
	VCCGT 2-Phase Power Stage	A

Date: Thursday, October 27, 2016 Sheet 41 of 66

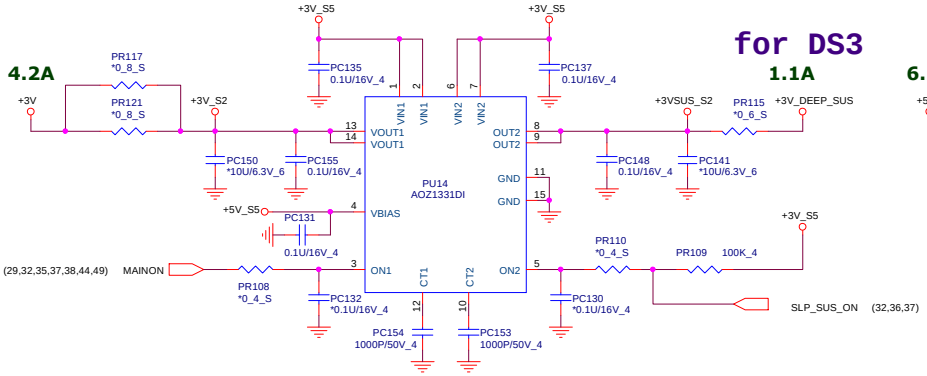


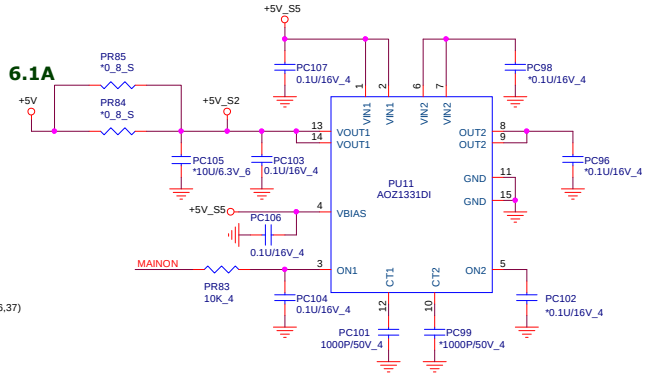
Quanta Computer Inc.		
PROJECT : NL8E		
Size	Document Number: VCCSA 1-Phase Power Stage	Rev A
Date: Thursday, October 27, 2016	Sheet 42 of 66	

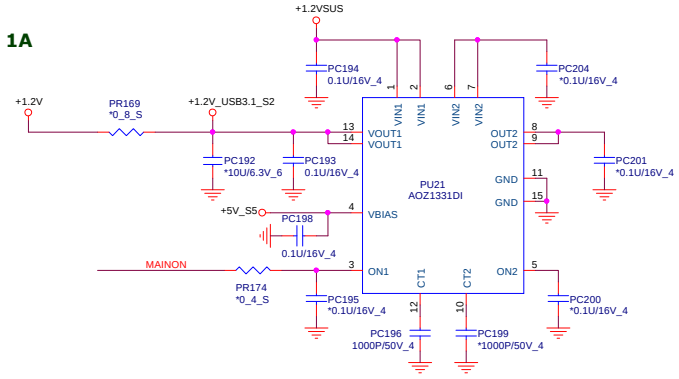
+3V (10,11,12,13,14,16,17,18,19,20,21,22,23,24,26,27,28,29,30,31,32,36,45,50,52,9)
+5V (19,20,21,22,24,30,31,45,52,63)
+3V_S5 (10,12,14,21,23,25,26,27,28,31,32,34,37,38,39,49,52)
+5V_S5 (10,26,28,29,34,35,36,37,39,40,41,42,44,45,46,47,49,50,51,52)

+VIN (18,33,34,35,36,39,40,41,42,47,50,52,63)

for DS3







NB5

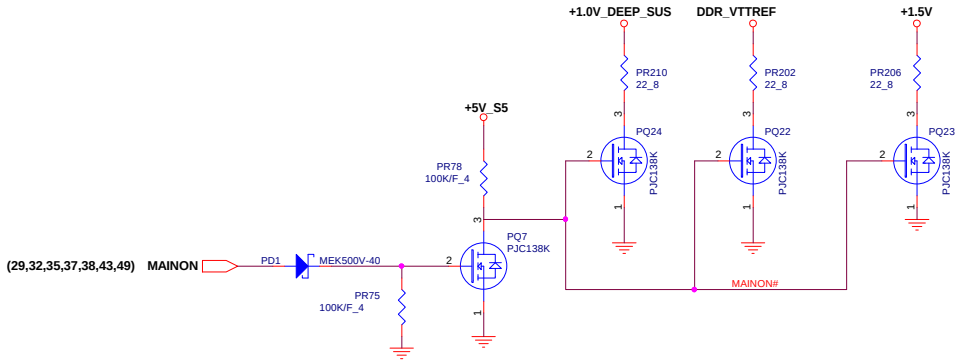
PROJECT : X1B-10L
Quanta Computer Inc.

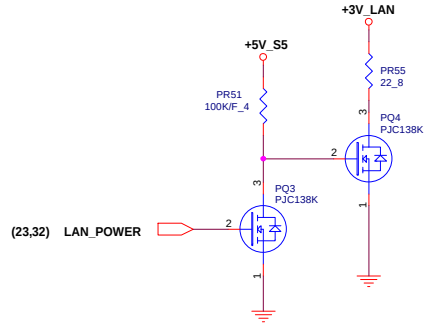
Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448)	1A

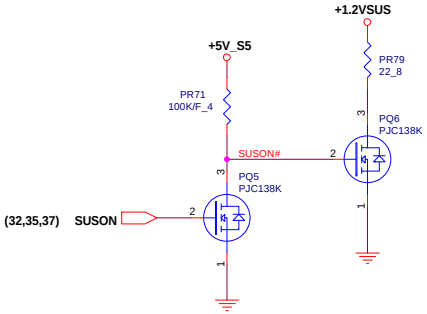
Date: Thursday, October 27, 2016 | Sheet 43 of 66

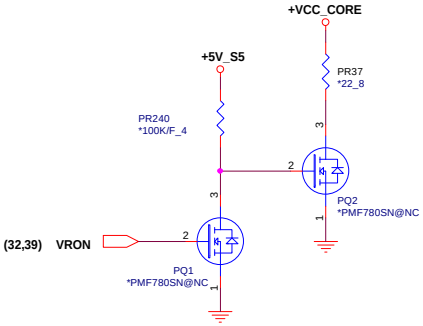
DISCHARGE

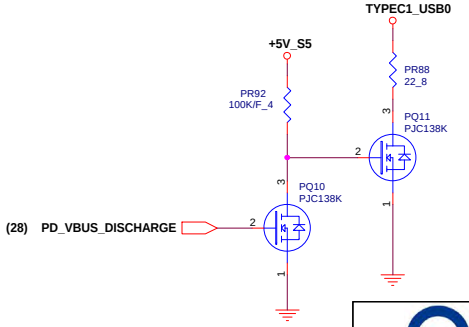
(19,20,21,22,24,30,31,43,45,52,63) +5V
(10,11,12,13,14,16,17,18,19,20,21,22,23,24,26,27,28,29,30,31,32,36,43,45,50,52,9) +3V
(10,11,14,36,37,39) +1.0V_DEEP_SUS
(16,17,35) DDR_VTTREF
(21,38) +1.5V
(10,16,17,2,35,43,50,6) +1.2VSUS
(10,26,28,29,34,35,36,37,39,40,41,42,43,45,46,47,49,50,51,52) +5V_S5
(40,7) +VCC_CORE
(23) +3V_LAN







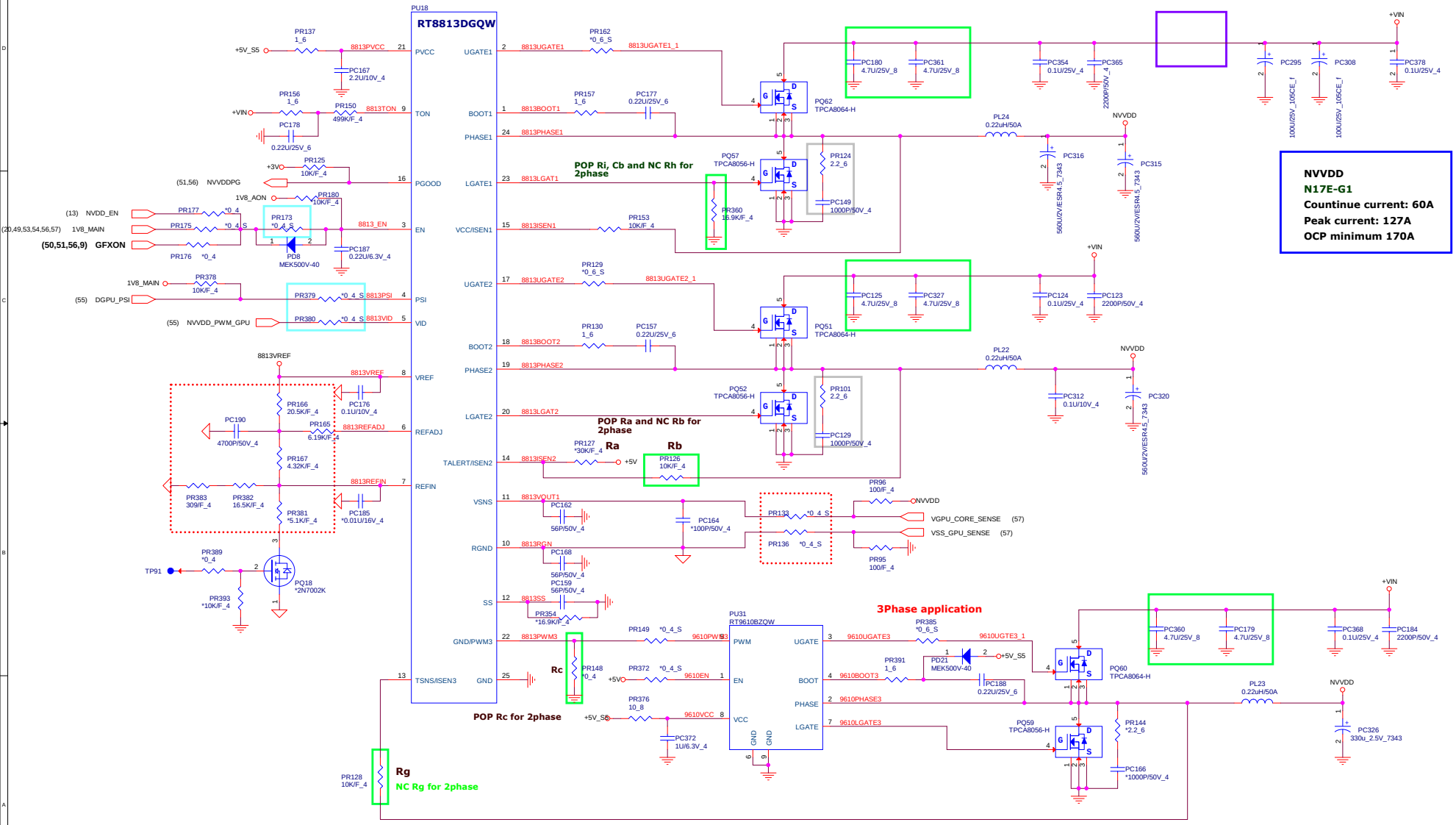




Quanta Computer Inc.
PROJECT :

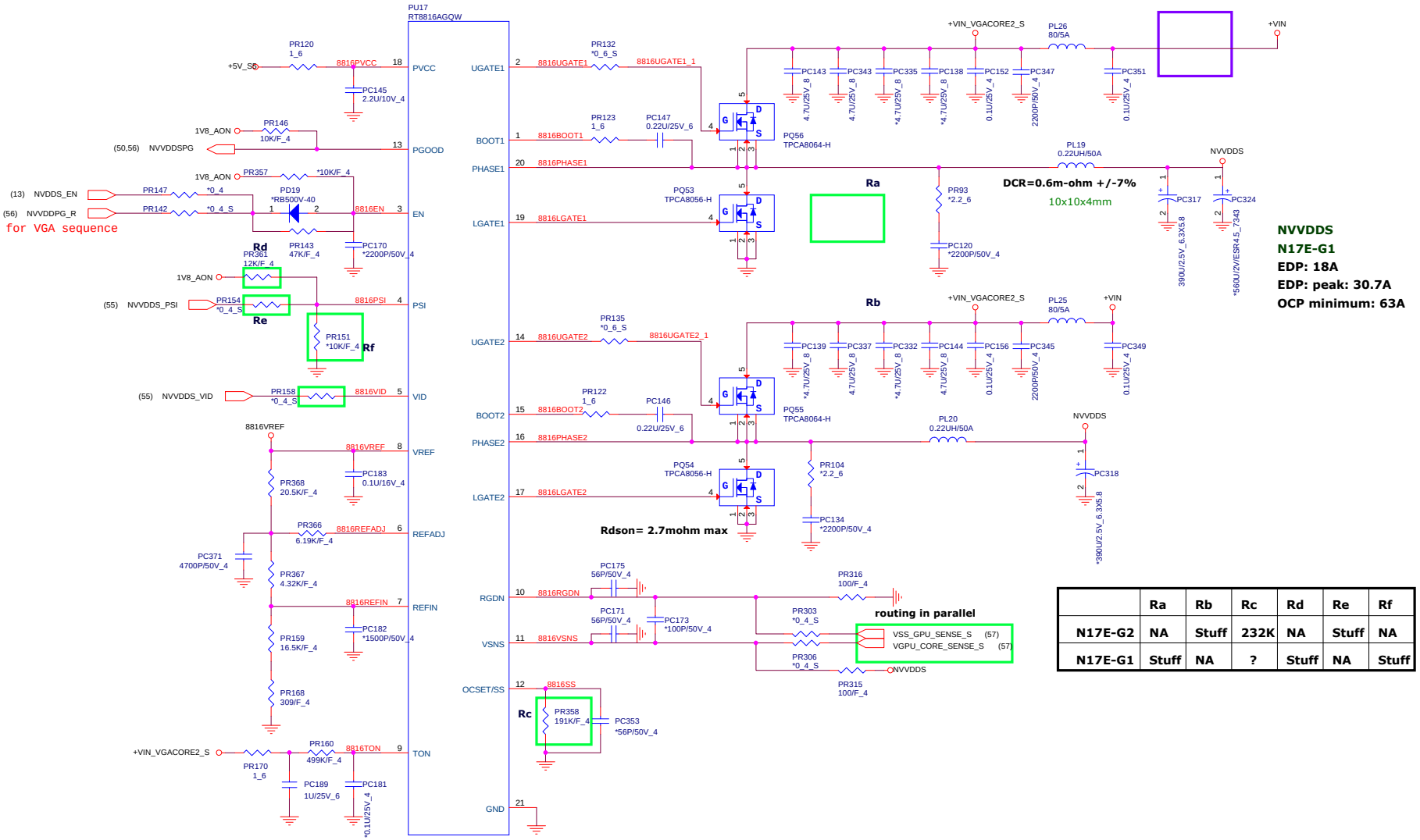
Size	Document Number	Rev
Custom	Discharge	3B
Date: Thursday, October 27, 2016	Sheet 44 of 66	

(10,26,29,29,34,35,36,37,39,40,41,42,43,44,46,47,49,50,51,52) +5V_S5
(10,11,12,13,14,16,17,18,19,20,21,22,23,24,26,27,28,29,30,31,32,36,43,50,52,9) +3V
(51,56,57) NVVDD



NVVDD
N17E-G1
Countinue current: 60A
Peak current: 127A
OCP minimum 170A

Quanta Computer Inc.	PROJECT :	
Size: Custom	Document Number: +VGACORE_N15PGX(RT8813A)	Rev: 3B
Date: Thursday, October 27, 2016	Sheet 45 of 66	



	Ra	Rb	Rc	Rd	Re	Rf
N17E-G2	NA	Stuff	232K	NA	Stuff	NA
N17E-G1	Stuff	NA	?	Stuff	NA	Stuff

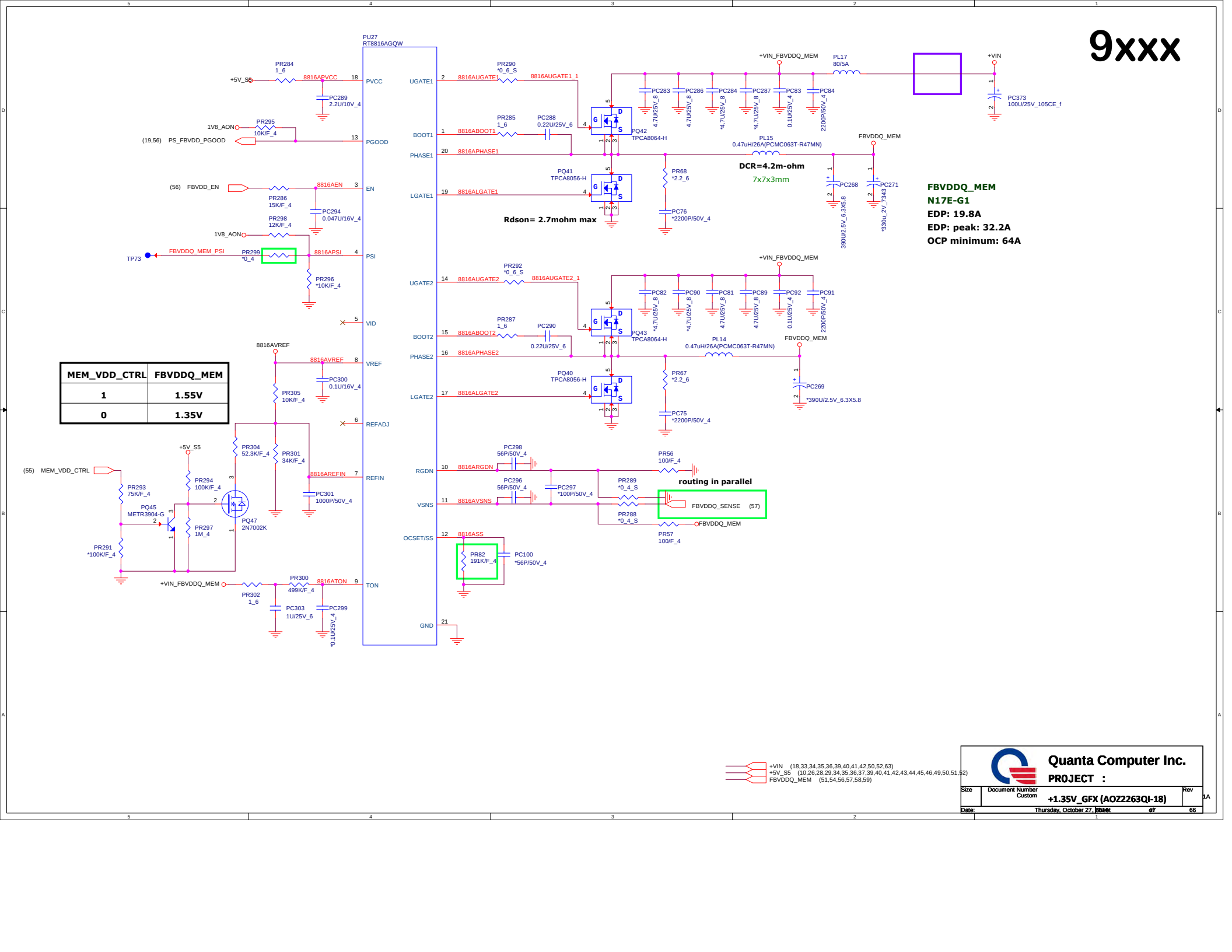
+3V (10,11,12,13,14,16,17,18,19,20,21,22,23,24,26,27,28,29,30,31,32,36,43,45,50,52,9)
+VIN (18,33,34,35,36,39,40,41,42,47,50,52,63)
+5V_S5 (10,26,28,29,34,35,36,37,39,40,41,42,43,44,45,47,49,50,51,52)
NVVDDS (51,57)
1V8_AON (45,47,49,50,53,55,56,57,9)

NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8813C)	1A

Date: Thursday, October 27, 2016 Sheet 46 of 66


9xxx
PU27
RT8816AGQW
PVCC
PGOOD
EN
PSI
VID
VREF
REFADJ
REFIN
TON
UGATE1
BOOT1
PHASE1
LGATE1
UGATE2
BOOT2
PHASE2
LGATE2
RGDN
VSNS
OCSET/SS
GND
8816APVCC
8816AUGATE1
8816ABOOT1
8816APHASE1
8816ALGATE1
8816AUGATE2
8816ABOOT2
8816APHASE2
8816ALGATE2
8816ARGDN
8816AVSNS
8816ASS
8816AEN
8816APSI
8816AVREF
8816AREFIN
8816ATON
PQ41 TPCA8056-H
PQ42 TPCA8064-H
PQ43 TPCA8064-H
PQ40 TPCA8056-H
PQ45 METR3904-G
PQ47 2N7002K
PL17 80/5A
PL15 0.47uH/26A(PCMC063T-R47MN)
PL14 0.47uH/26A(PCMC063T-R47MN)
+VIN_FBVDDQ_MEM
FBVDDQ_MEM
+VIN
+5V_S5
1V8_AON
(19,56) PS_FBVDD_PGOOD
(56) FBVDD_EN
FBVDDQ_MEM_PSI
TP73
(55) MEM_VDD_CTRL
DCR=4.2m-ohm
7x7x3mm
Rdson= 2.7mohm max
routing in parallel
FBVDDQ_SENSE (57)
FBVDDQ_MEM
FBVDDQ_MEM
N17E-G1
EDP: 19.8A
EDP: peak: 32.2A
OCP minimum: 64A
MEM_VDD_CTRL | FBVDDQ_MEM
1 | 1.55V
0 | 1.35V
+VIN (18,33,34,35,36,39,40,41,42,50,52,63)
+5V_S5 (10,26,28,29,34,35,36,37,39,40,41,42,43,44,45,46,49,50,51,52)
FBVDDQ_MEM (51,54,56,57,58,59)
Quanta Computer Inc.
PROJECT :
+1.35V_GFX (AOZ2263QI-18)
Size
Document Number
Custom
Rev
1A
Date: Thursday, October 27, 2022
Sheet 47 of 66

Quanta Computer Inc.

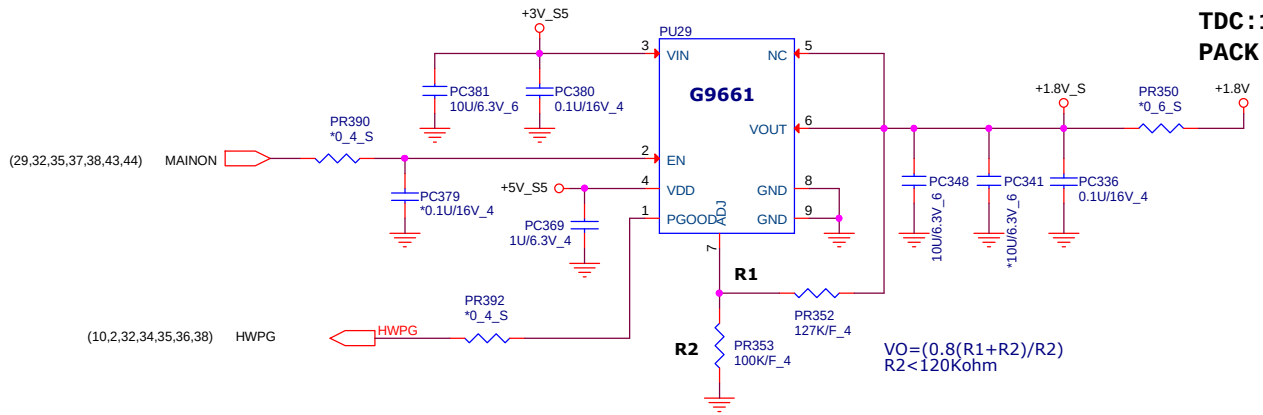
PROJECT :

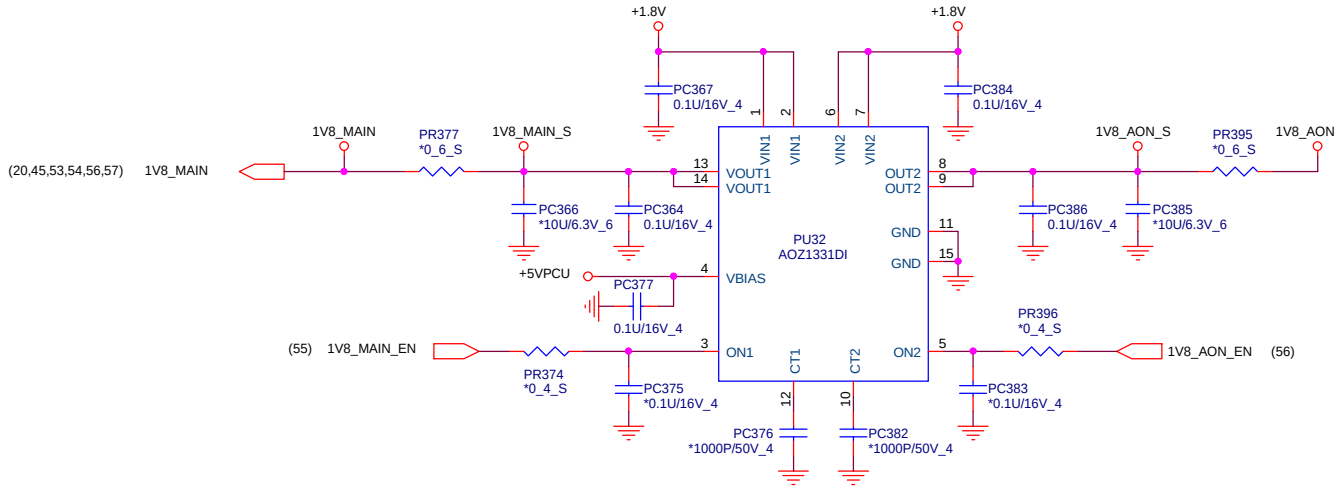
Size	Document Number	Rev
Custom	+1.35V_GPU(TPS51211DSCR)	3B

Date: Thursday, October 27, 2016 Sheet 48 of 66

(10,26,28,29,34,35,36,37,39,40,41,42,43,44,45,46,47,50,51,52) +5V_S5
(18,33,34,35,36,39,40,41,42,47,50,52,63) +VIN

+1.8V +/- 5%
TDC:1A
PACK:2A





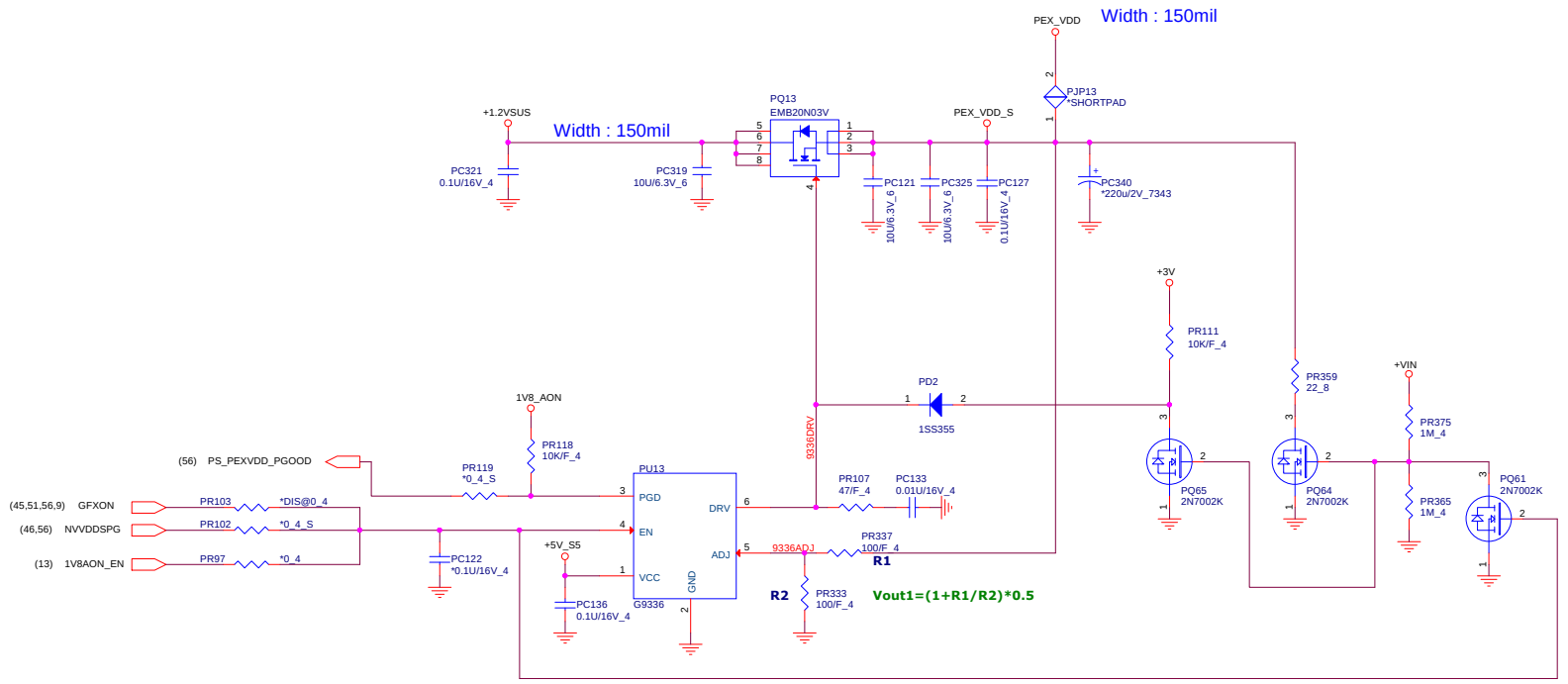
Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
Custom	+1.8V (APW8713)	3B
Date: Thursday, October 27, 2016	Sheet 49 of 66	

+VIN (18,33,34,35,36,39,40,41,42,47,52,63)
+3V_S5 (10,12,14,21,23,25,26,27,28,31,32,34,37,38,39,43,49,52)
+5V_S5 (10,26,28,29,34,35,36,37,39,40,41,42,43,44,45,46,47,49,51,52)

+1.2VSUS (10,16,17,2,35,43,44,6)
PEX_VDD (51,53,55)

+1.0V +/- 5%
EDP=3A

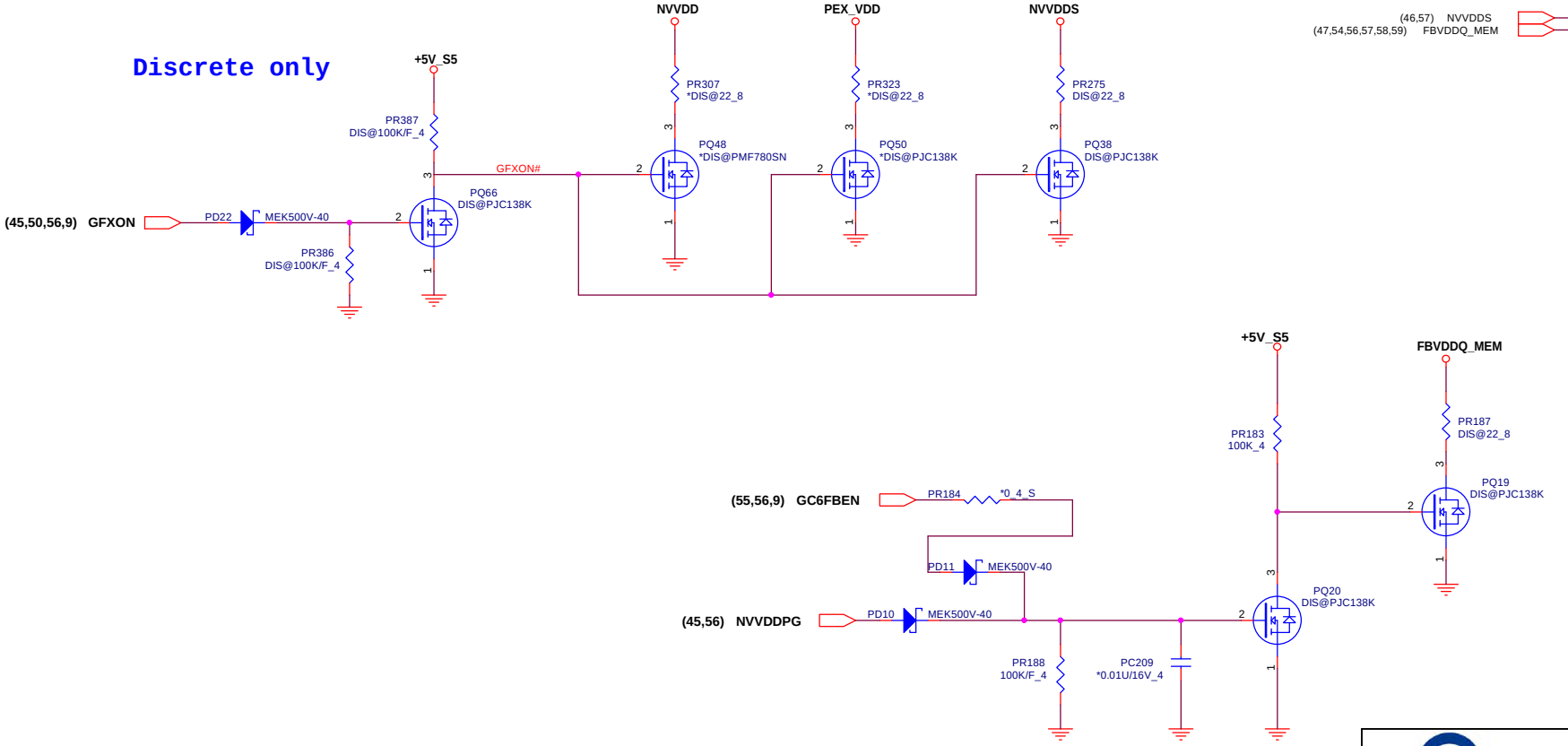


NB5	**PROJECT : X1B-10L** Quanta Computer Inc.	
Size: Custom	Document Number: 1.05V_VGA/3V_VGA	Rev: 1A
Date: Thursday, October 27, 2016	Sheet 50 of 66	

(45,56,57) NVVDD
(50,53,55) PEX_VDD

(46,57) NVVDDS
(47,54,56,57,58,59) FBVDDQ_MEM

Discrete only

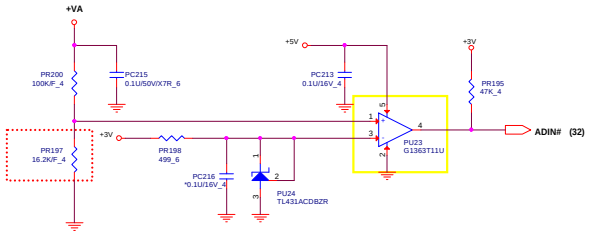


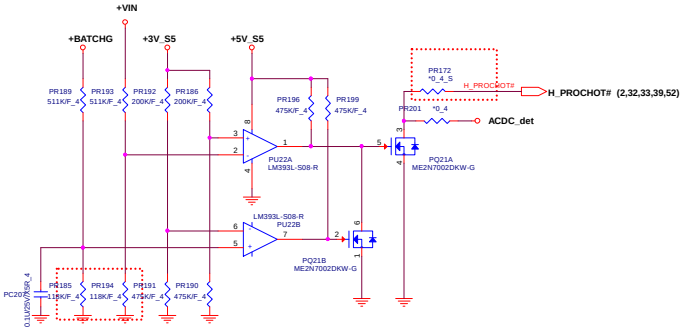
Quanta Computer Inc.

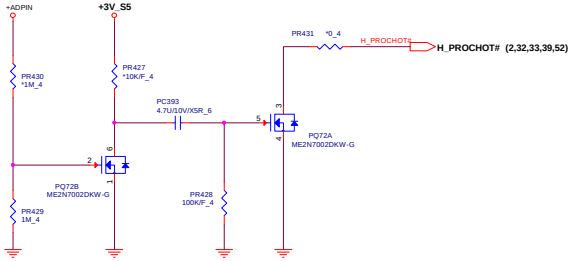
PROJECT :

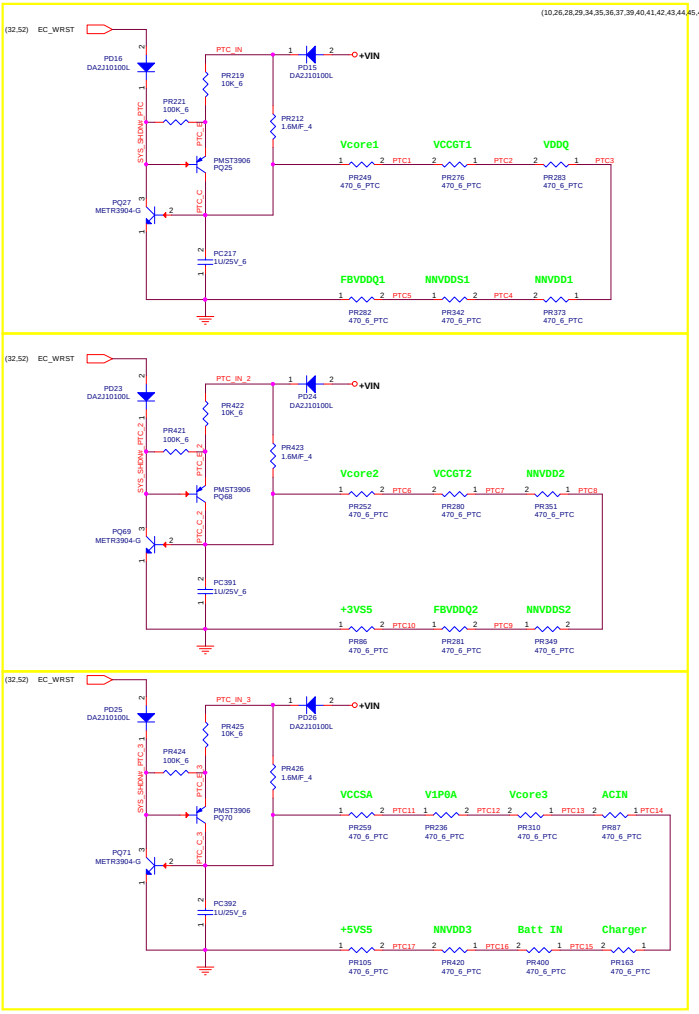
Size	Document Number	Rev
Custom	Discrete Discharge	3B

Date: Thursday, October 27, 2016 Sheet 51 of 66

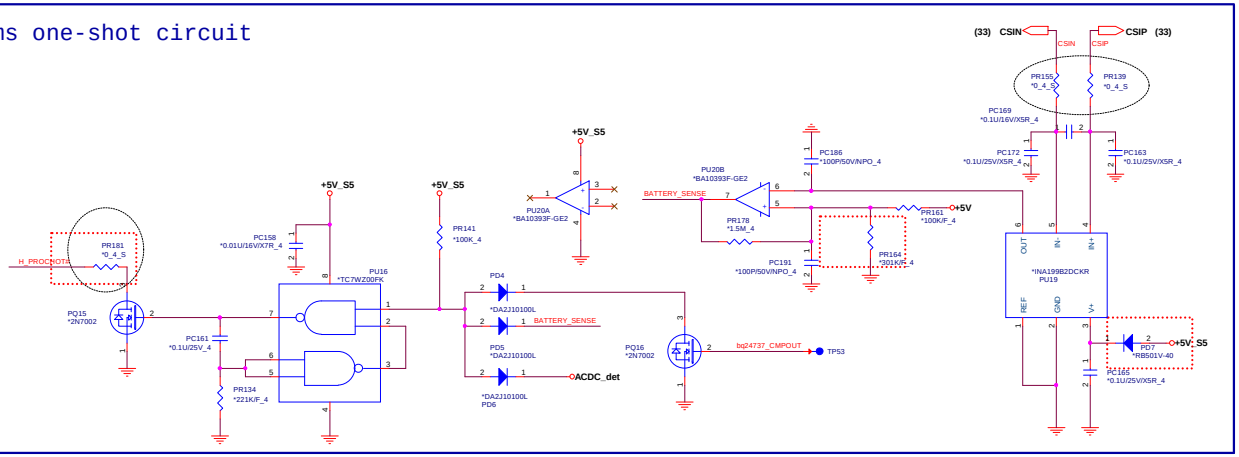




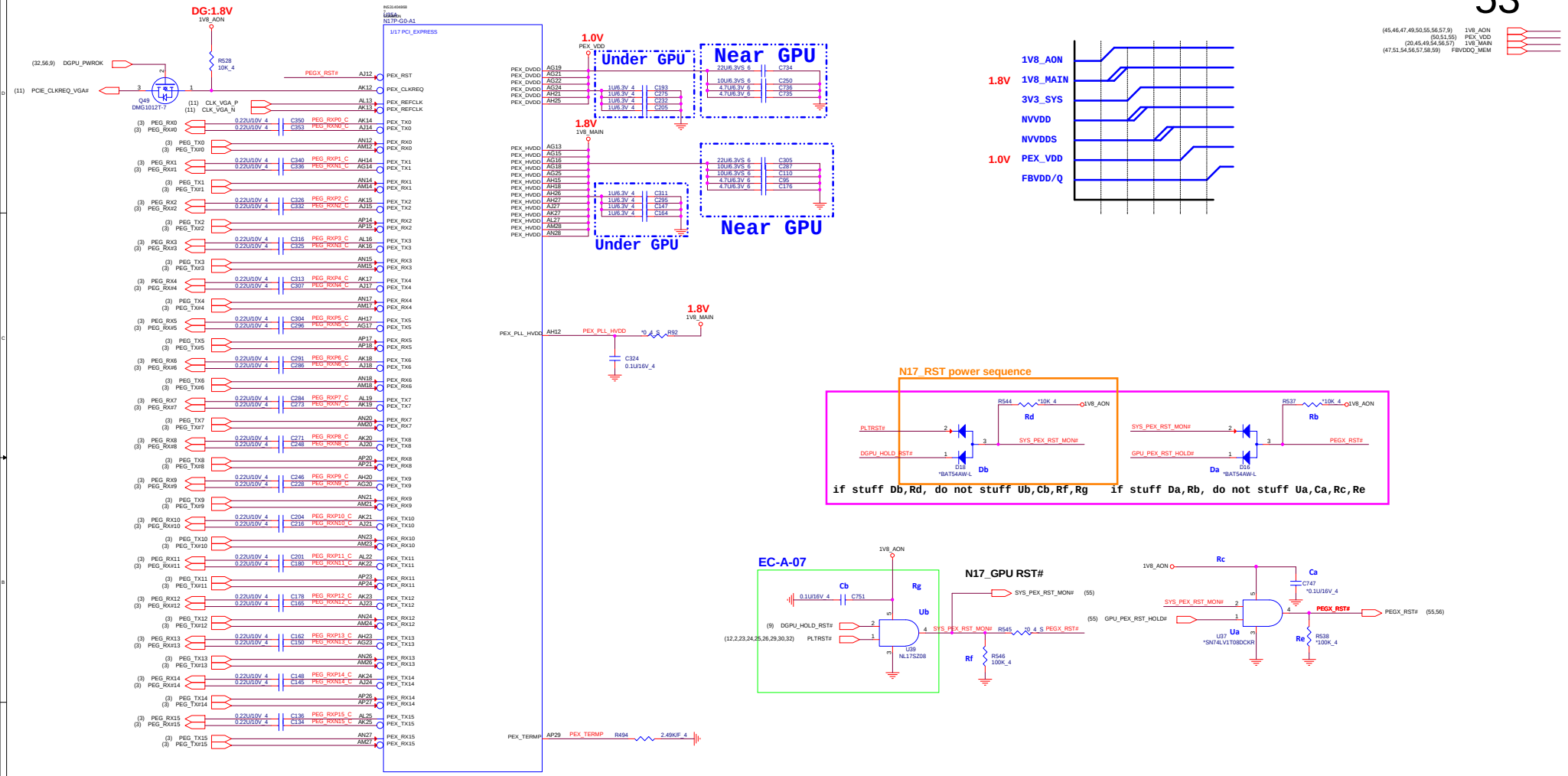




10ms one-shot circuit



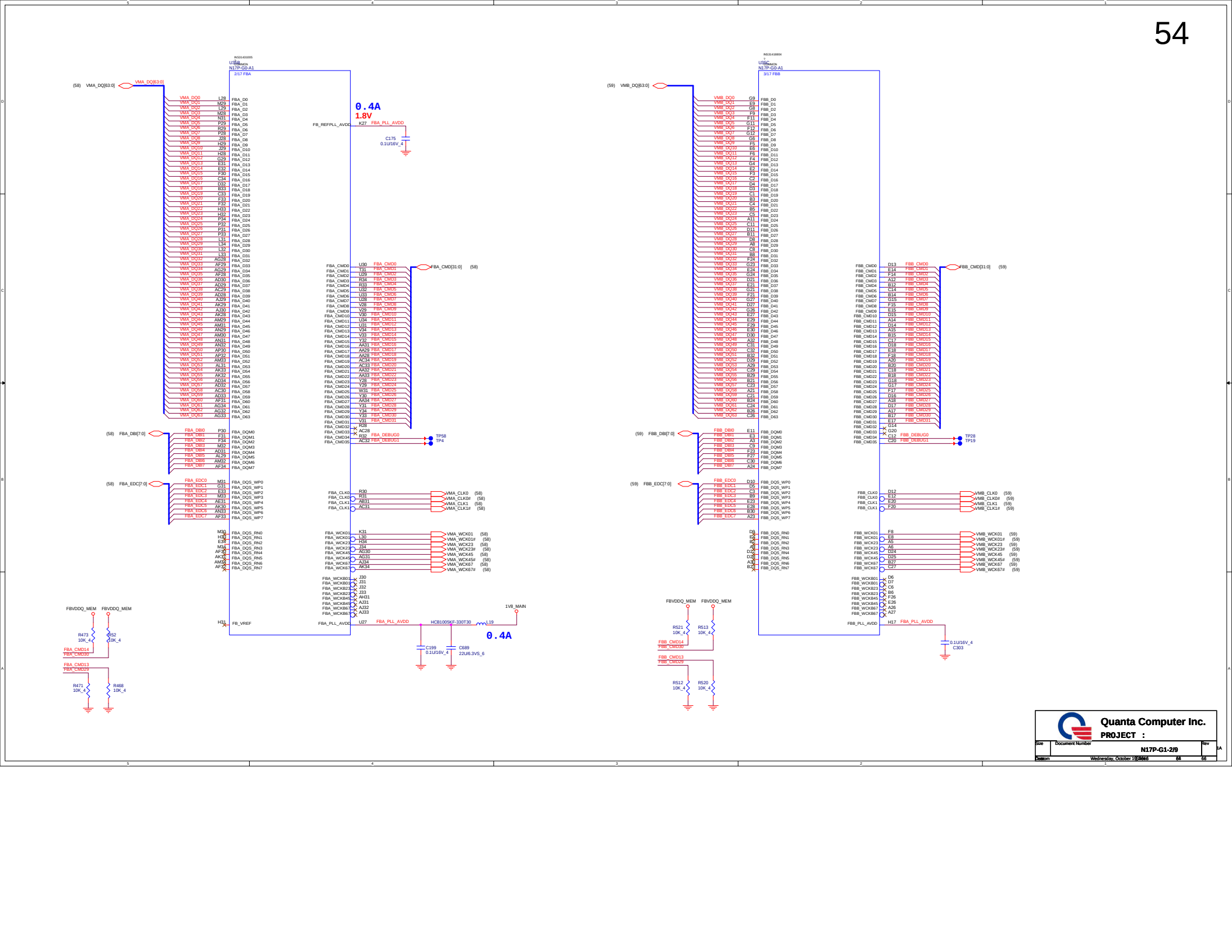
Quanta Computer Inc.
PROJECT :
Size: Custom
Document Number: 10ms
Rev: 3B
Date: Thursday, October 27, 2016
Sheet 52 of 66



Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	N17P-GX-1/9	1A
Date:	Wednesday, October 19, 2016	Sheet 53 of 53


U35B
N17P-G0-A1
2/17 FBA
(58) VMA_DQ[63:0]
VMA_DQ[63:0]
FBA_D0
FBA_D1
FBA_D2
FBA_D3
FBA_D4
FBA_D5
FBA_D6
FBA_D7
FBA_D8
FBA_D9
FBA_D10
FBA_D11
FBA_D12
FBA_D13
FBA_D14
FBA_D15
FBA_D16
FBA_D17
FBA_D18
FBA_D19
FBA_D20
FBA_D21
FBA_D22
FBA_D23
FBA_D24
FBA_D25
FBA_D26
FBA_D27
FBA_D28
FBA_D29
FBA_D30
FBA_D31
FBA_D32
FBA_D33
FBA_D34
FBA_D35
FBA_D36
FBA_D37
FBA_D38
FBA_D39
FBA_D40
FBA_D41
FBA_D42
FBA_D43
FBA_D44
FBA_D45
FBA_D46
FBA_D47
FBA_D48
FBA_D49
FBA_D50
FBA_D51
FBA_D52
FBA_D53
FBA_D54
FBA_D55
FBA_D56
FBA_D57
FBA_D58
FBA_D59
FBA_D60
FBA_D61
FBA_D62
FBA_D63
0.4A
1.8V
FB_REFPLL_AVDD
K27 FBA_PLL_AVDD
C175
0.1U/16V_4
(58) FBA_DBI[7:0]
FBA_DBI[7:0]
FBA_DQM0
FBA_DQM1
FBA_DQM2
FBA_DQM3
FBA_DQM4
FBA_DQM5
FBA_DQM6
FBA_DQM7
(58) FBA_EDC[7:0]
FBA_EDC[7:0]
FBA_DQS_WP0
FBA_DQS_WP1
FBA_DQS_WP2
FBA_DQS_WP3
FBA_DQS_WP4
FBA_DQS_WP5
FBA_DQS_WP6
FBA_DQS_WP7
FBA_DQS_RN0
FBA_DQS_RN1
FBA_DQS_RN2
FBA_DQS_RN3
FBA_DQS_RN4
FBA_DQS_RN5
FBA_DQS_RN6
FBA_DQS_RN7
H31 FB_VREF
FBA_CMD[31:0] (58)
FBA_CMD0
FBA_CMD1
FBA_CMD2
FBA_CMD3
FBA_CMD4
FBA_CMD5
FBA_CMD6
FBA_CMD7
FBA_CMD8
FBA_CMD9
FBA_CMD10
FBA_CMD11
FBA_CMD12
FBA_CMD13
FBA_CMD14
FBA_CMD15
FBA_CMD16
FBA_CMD17
FBA_CMD18
FBA_CMD19
FBA_CMD20
FBA_CMD21
FBA_CMD22
FBA_CMD23
FBA_CMD24
FBA_CMD25
FBA_CMD26
FBA_CMD27
FBA_CMD28
FBA_CMD29
FBA_CMD30
FBA_CMD31
FBA_DEBUG0
FBA_DEBUG1
TP58
TP4
FBA_CLK0
FBA_CLK0#
FBA_CLK1
FBA_CLK1#
VMA_CLK0 (58)
VMA_CLK0# (58)
VMA_CLK1 (58)
VMA_CLK1# (58)
FBA_WCK01
FBA_WCK01#
FBA_WCK23
FBA_WCK23#
FBA_WCK45
FBA_WCK45#
FBA_WCK67
FBA_WCK67#
VMA_WCK01 (58)
VMA_WCK01# (58)
VMA_WCK23 (58)
VMA_WCK23# (58)
VMA_WCK45 (58)
VMA_WCK45# (58)
VMA_WCK67 (58)
VMA_WCK67# (58)
FBA_WCKB01
FBA_WCKB01
FBA_WCKB23
FBA_WCKB23
FBA_WCKB45
FBA_WCKB45
FBA_WCKB67
FBA_WCKB67
FBA_PLL_AVDD
U27
HCB1005KF-330T30
L19
1V8_MAIN
0.4A
C199
0.1U/16V_4
C689
22U/6.3VS_6
FBVDDQ_MEM
FBVDDQ_MEM
R473
10K_4
R52
10K_4
FBA_CMD14
FBA_CMD30
FBA_CMD13
FBA_CMD29
R471
10K_4
R468
10K_4
U35C
N17P-G0-A1
3/17 FBB
(59) VMB_DQ[63:0]
VMB_DQ[63:0]
FBB_D0
FBB_D1
FBB_D2
FBB_D3
FBB_D4
FBB_D5
FBB_D6
FBB_D7
FBB_D8
FBB_D9
FBB_D10
FBB_D11
FBB_D12
FBB_D13
FBB_D14
FBB_D15
FBB_D16
FBB_D17
FBB_D18
FBB_D19
FBB_D20
FBB_D21
FBB_D22
FBB_D23
FBB_D24
FBB_D25
FBB_D26
FBB_D27
FBB_D28
FBB_D29
FBB_D30
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FBB_D32
FBB_D33
FBB_D34
FBB_D35
FBB_D36
FBB_D37
FBB_D38
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FBB_D46
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FBB_D49
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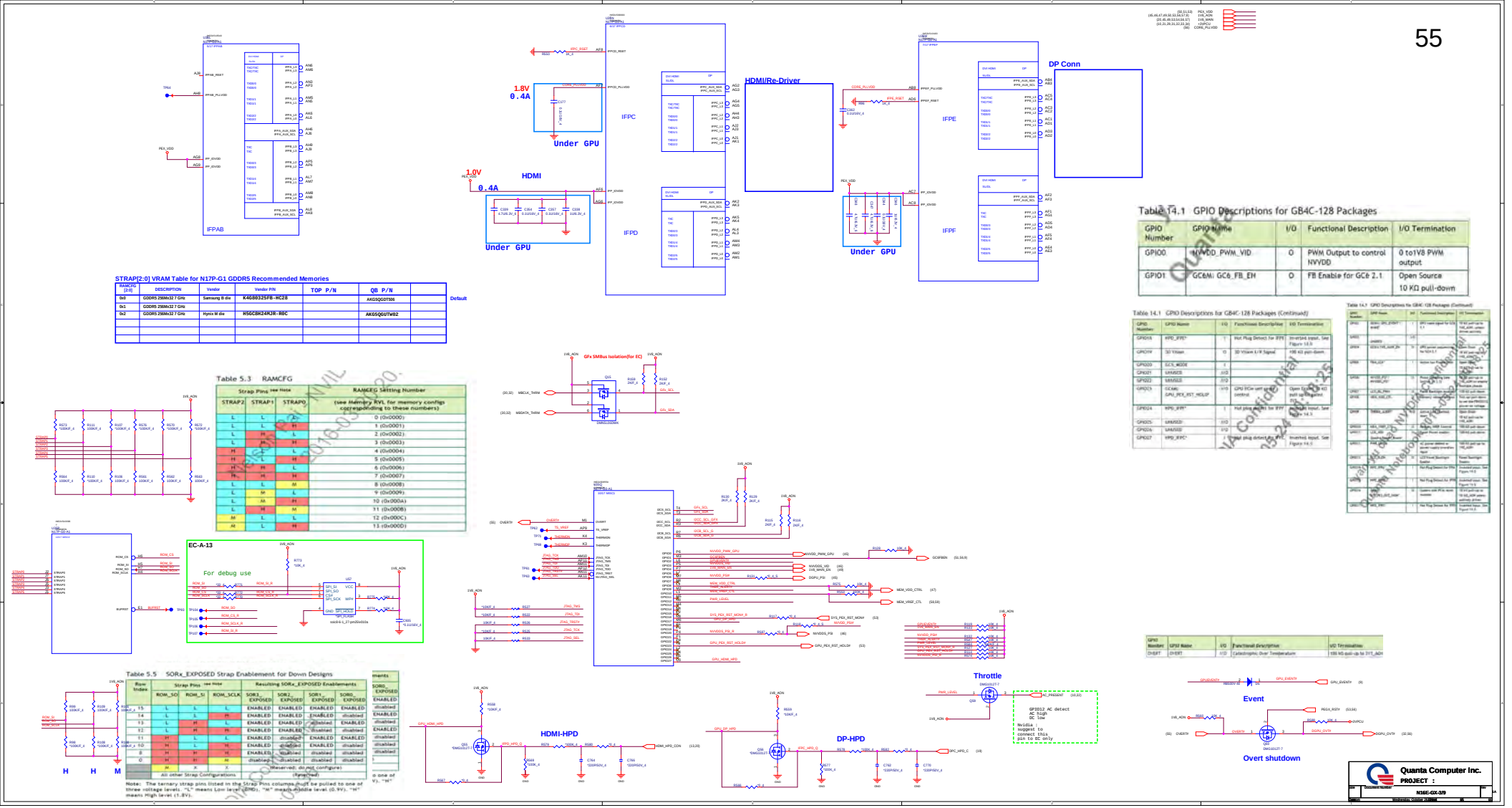
FBB_D52
FBB_D53
FBB_D54
FBB_D55
FBB_D56
FBB_D57
FBB_D58
FBB_D59
FBB_D60
FBB_D61
FBB_D62
FBB_D63
(59) FBB_DBI[7:0]
FBB_DBI[7:0]
FBB_DQM0
FBB_DQM1
FBB_DQM2
FBB_DQM3
FBB_DQM4
FBB_DQM5
FBB_DQM6
FBB_DQM7
(59) FBB_EDC[7:0]
FBB_EDC[7:0]
FBB_DQS_WP0
FBB_DQS_WP1
FBB_DQS_WP2
FBB_DQS_WP3
FBB_DQS_WP4
FBB_DQS_WP5
FBB_DQS_WP6
FBB_DQS_WP7
FBB_DQS_RN0
FBB_DQS_RN1
FBB_DQS_RN2
FBB_DQS_RN3
FBB_DQS_RN4
FBB_DQS_RN5
FBB_DQS_RN6
FBB_DQS_RN7
FBB_CMD[31:0] (59)
FBB_CMD0
FBB_CMD1
FBB_CMD2
FBB_CMD3
FBB_CMD4
FBB_CMD5
FBB_CMD6
FBB_CMD7
FBB_CMD8
FBB_CMD9
FBB_CMD10
FBB_CMD11
FBB_CMD12
FBB_CMD13
FBB_CMD14
FBB_CMD15
FBB_CMD16
FBB_CMD17
FBB_CMD18
FBB_CMD19
FBB_CMD20
FBB_CMD21
FBB_CMD22
FBB_CMD23
FBB_CMD24
FBB_CMD25
FBB_CMD26
FBB_CMD27
FBB_CMD28
FBB_CMD29
FBB_CMD30
FBB_CMD31
FBB_DEBUG0
FBB_DEBUG1
TP28
TP19
FBB_CLK0
FBB_CLK0#
FBB_CLK1
FBB_CLK1#
VMB_CLK0 (59)
VMB_CLK0# (59)
VMB_CLK1 (59)
VMB_CLK1# (59)
FBB_WCK01
FBB_WCK01#
FBB_WCK23
FBB_WCK23#
FBB_WCK45
FBB_WCK45#
FBB_WCK67
FBB_WCK67#
VMB_WCK01 (59)
VMB_WCK01# (59)
VMB_WCK23 (59)
VMB_WCK23# (59)
VMB_WCK45 (59)
VMB_WCK45# (59)
VMB_WCK67 (59)
VMB_WCK67# (59)
FBB_WCKB01
FBB_WCKB01
FBB_WCKB23
FBB_WCKB23
FBB_WCKB45
FBB_WCKB45
FBB_WCKB67
FBB_WCKB67
FBB_PLL_AVDD
H17 FBA_PLL_AVDD
0.1U/16V_4
C303
FBVDDQ_MEM
FBVDDQ_MEM
R521
10K_4
R513
10K_4
FBB_CMD14
FBB_CMD30
FBB_CMD13
FBB_CMD29
R512
10K_4
R520
10K_4
Quanta Computer Inc.
PROJECT :
Size
Document Number
N17P-G1-2/9
Rev
1A
Date:
Wednesday, October 19, 2016
Sheet
58
of
68



STRAP[2:0] VRAM Table for N17P-G1 GDDR5 Recommended Memories

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP_P/N	QB_P/N	
0x0	GDDR5 256Mx32 7 GHz	Samsung B die	K4G80325FB-HC28		AKG5QGDT306	Default
0x1	GDDR5 256Mx32 7 GHz					
0x2	GDDR5 256Mx32 7 GHz	Hynix M die	H5GC8H24MJR-R0C		AKG5Q6UTW02	

Table 5.3 RAMCFG

Strap Pins (see Note)			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins (see Note)			Resulting SORx_EXPOSED Enablements				SORx_EXPOSED Assignments
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED	disabled
10	H	L	H	ENABLED	disabled	ENABLED	disabled	disabled
9	H	H	L	ENABLED	disabled	disabled	ENABLED	disabled
8	H	H	H	disabled	disabled	disabled	disabled	disabled
7	M	X	X	Reserved; do not configure (Keep Float)				one of V1, "H"
All other Strap Configurations								

Note: The ternary strap pins listed in the Strap Pins columns must be pulled to one of three voltage levels. "L" means Low level (GND), "M" means middle level (0.5V), "H" means High level (1.8V).

Table 14.1 GPIO Descriptions for GB4C-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to1V8 PWM output
GPIO1	GC6#/ GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down

Table 14.1 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO16	HPD_EPC*	I	Hot Plug Detect for EPC	Inverted input. See Figure 13.5
GPIO19	3D Vision	O	3D Vision L/R Signal	100 kΩ pull-down.
GPIO20	ECS_MODE	I		
GPIO21	UMASCS	I/O		
GPIO22	UMASCLK	I/O		
GPIO23	GC6#/ GPU_PEX_RST_HOLD*	I/O	GPU PCIe card reset control	Open Source 10 KΩ pull-up to internal 3V3_ALW.
GPIO24	HPD_EPF*	I	Hot plug detect for EPF	Inverted input. See Figure 14.5
GPIO25	UMASDI	I/O		
GPIO26	UMASDO	I/O		
GPIO27	HPD_EPC*	I	Hot plug detect for EPC	Inverted input. See Figure 14.5

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
DVERT	DVERT	I/O	Catastrophic Over Temperature	100 MΩ pull-up to 3V3_ALW

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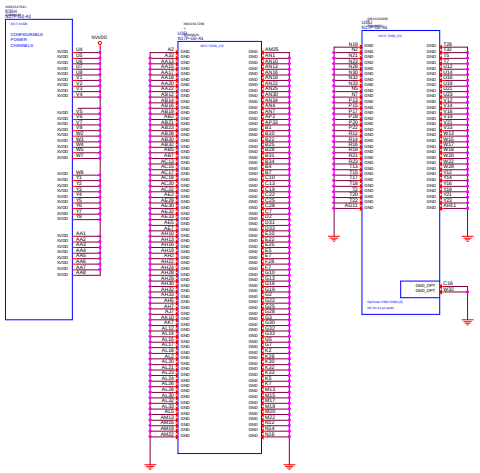
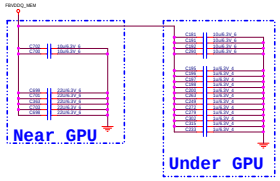
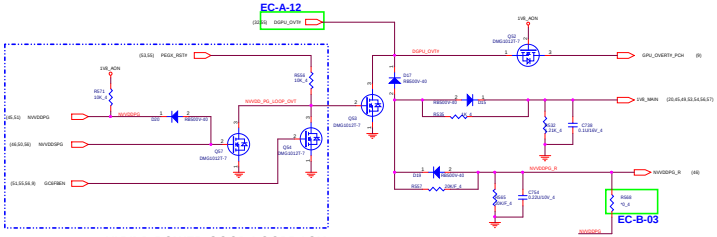
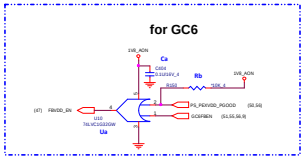




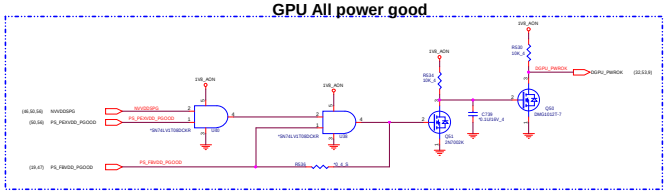


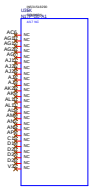
NVVDD POWER GOOD LOOPBACK

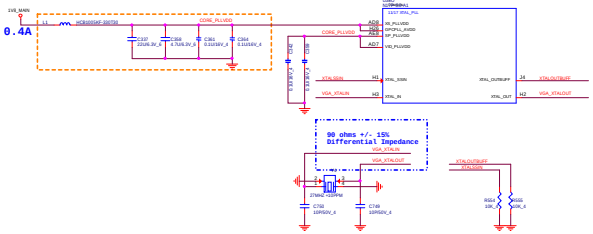
Overt temp ckt for NVVDD and NVVDDS



GPU All power good







For N17 Power off sequence

EC-A-11

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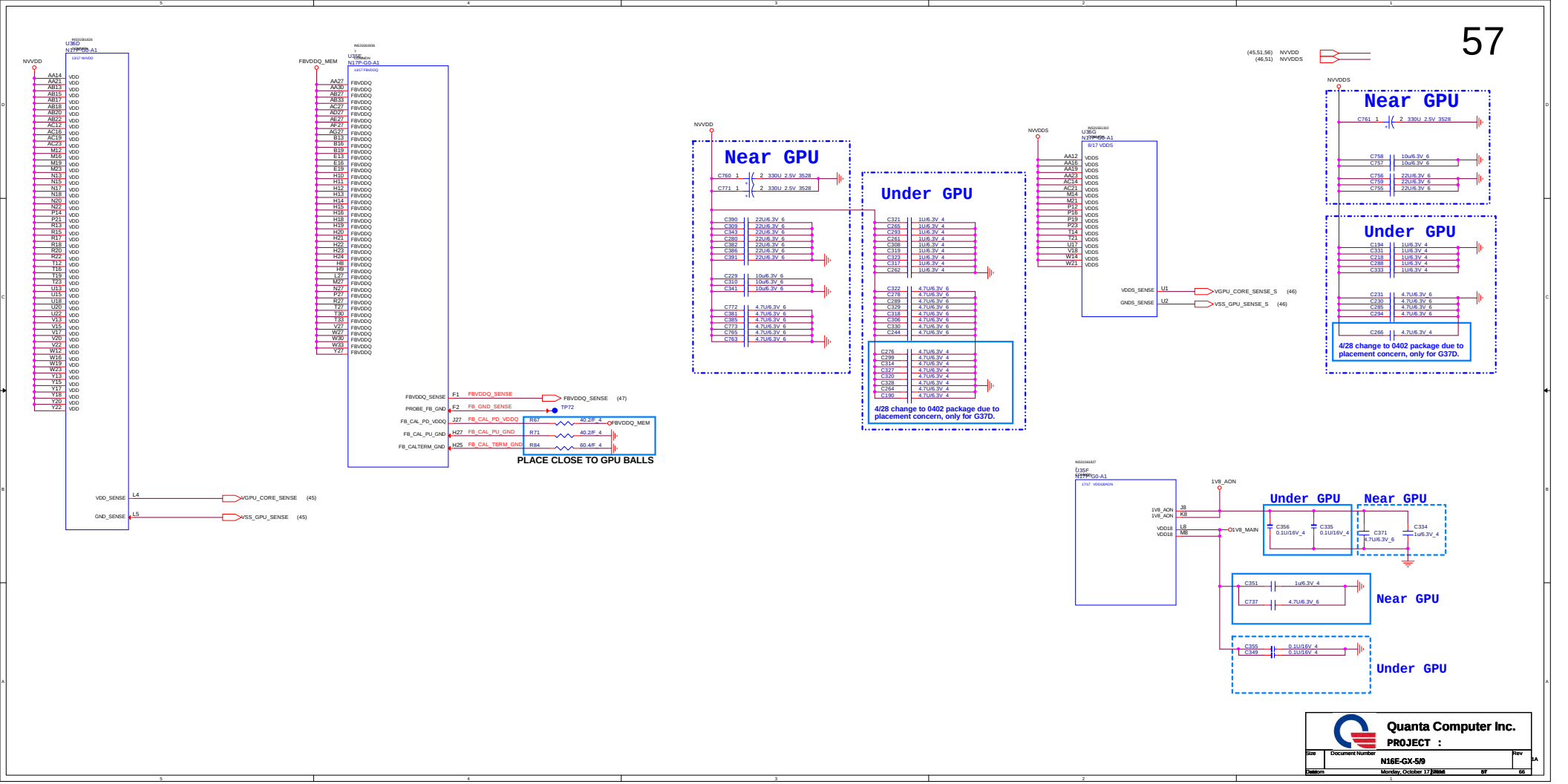
N16E-GX-4/8



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PROJECT : N16E-GX-5/9			
Size	Document Number		Rev 1A
Date: Monday, October 17, 2016	Sheet 57	of 65	

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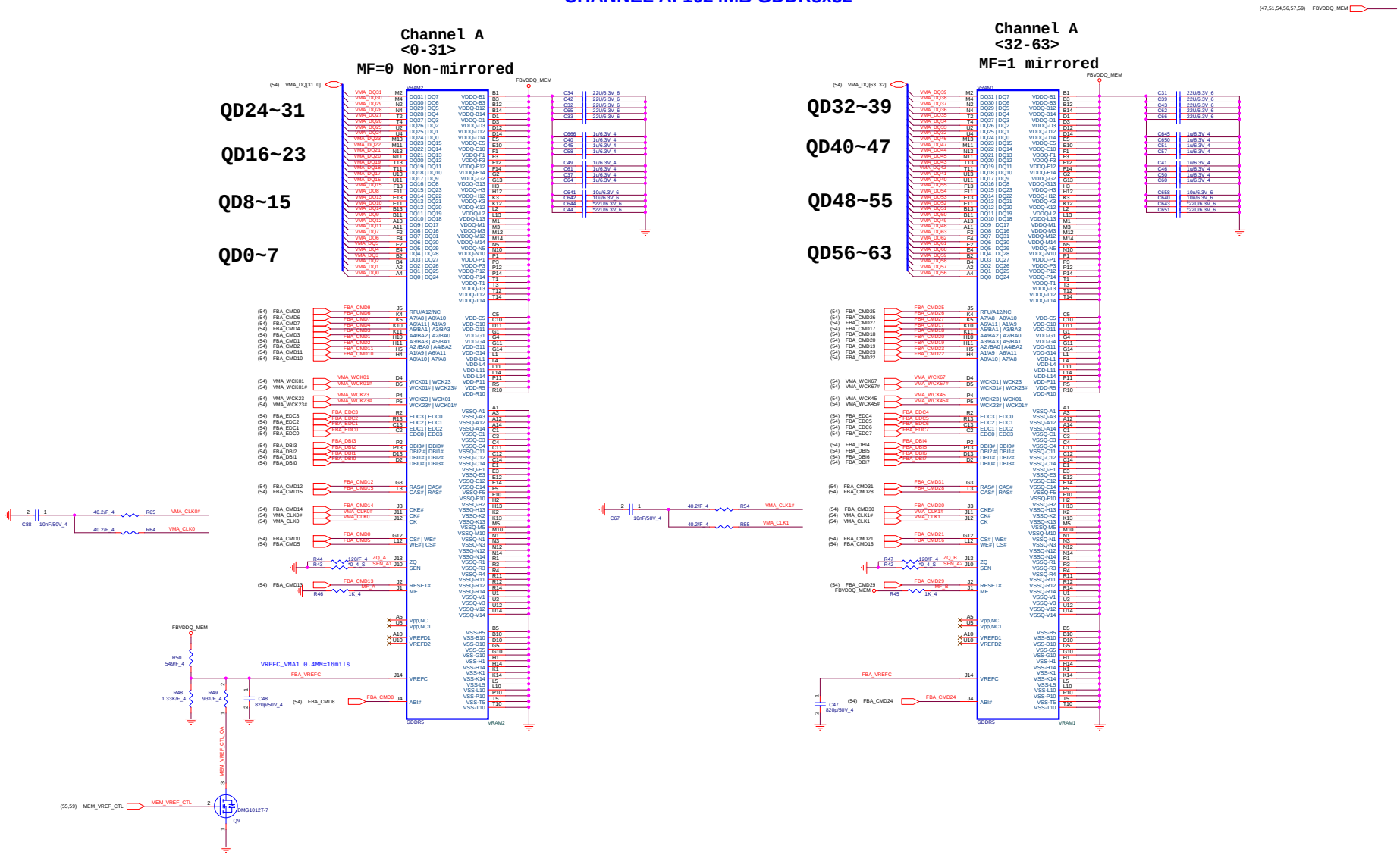
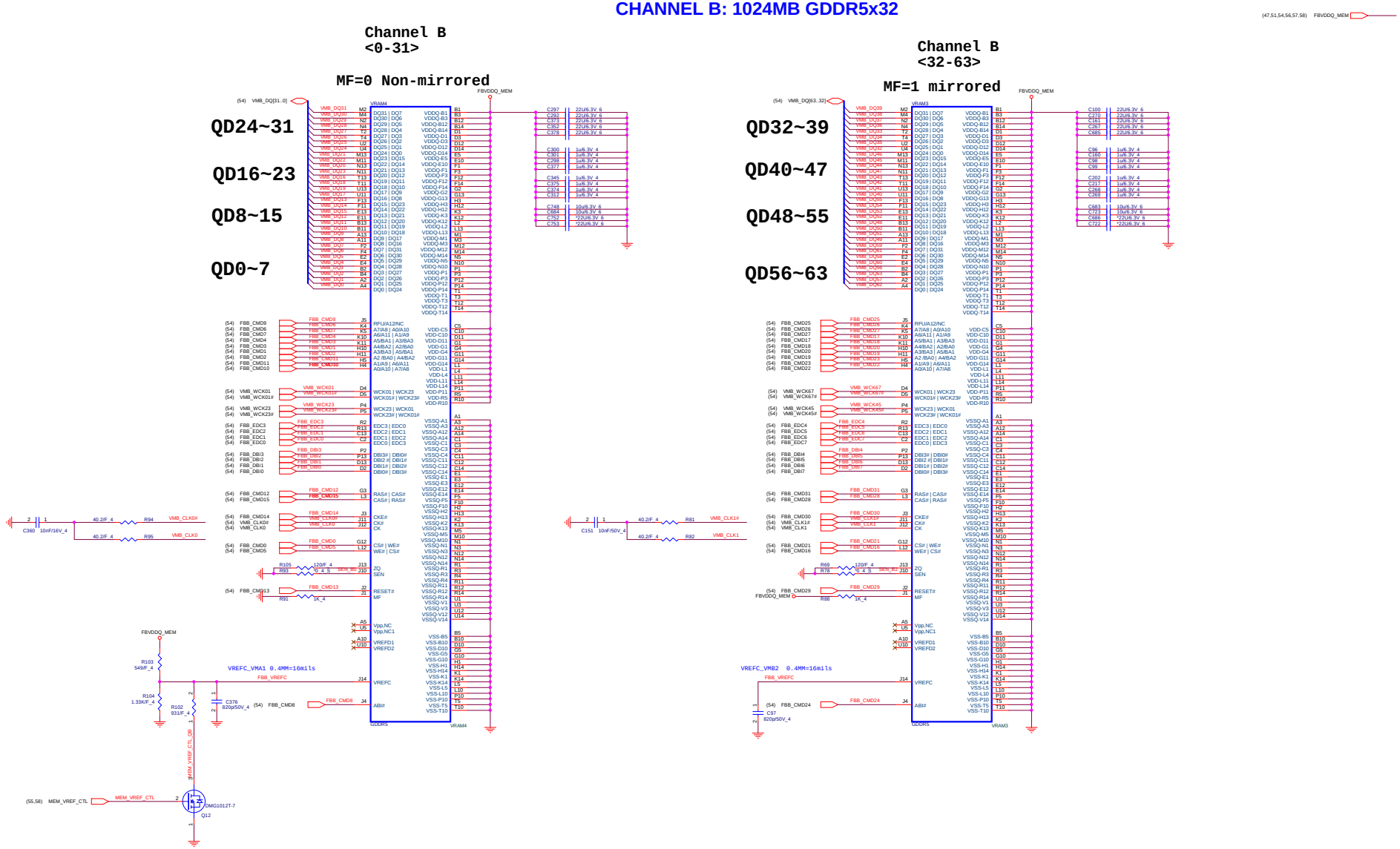


CHANNEL B: 1024MB GDDR5x32



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PROJECT :

Size	Document Number	Rev
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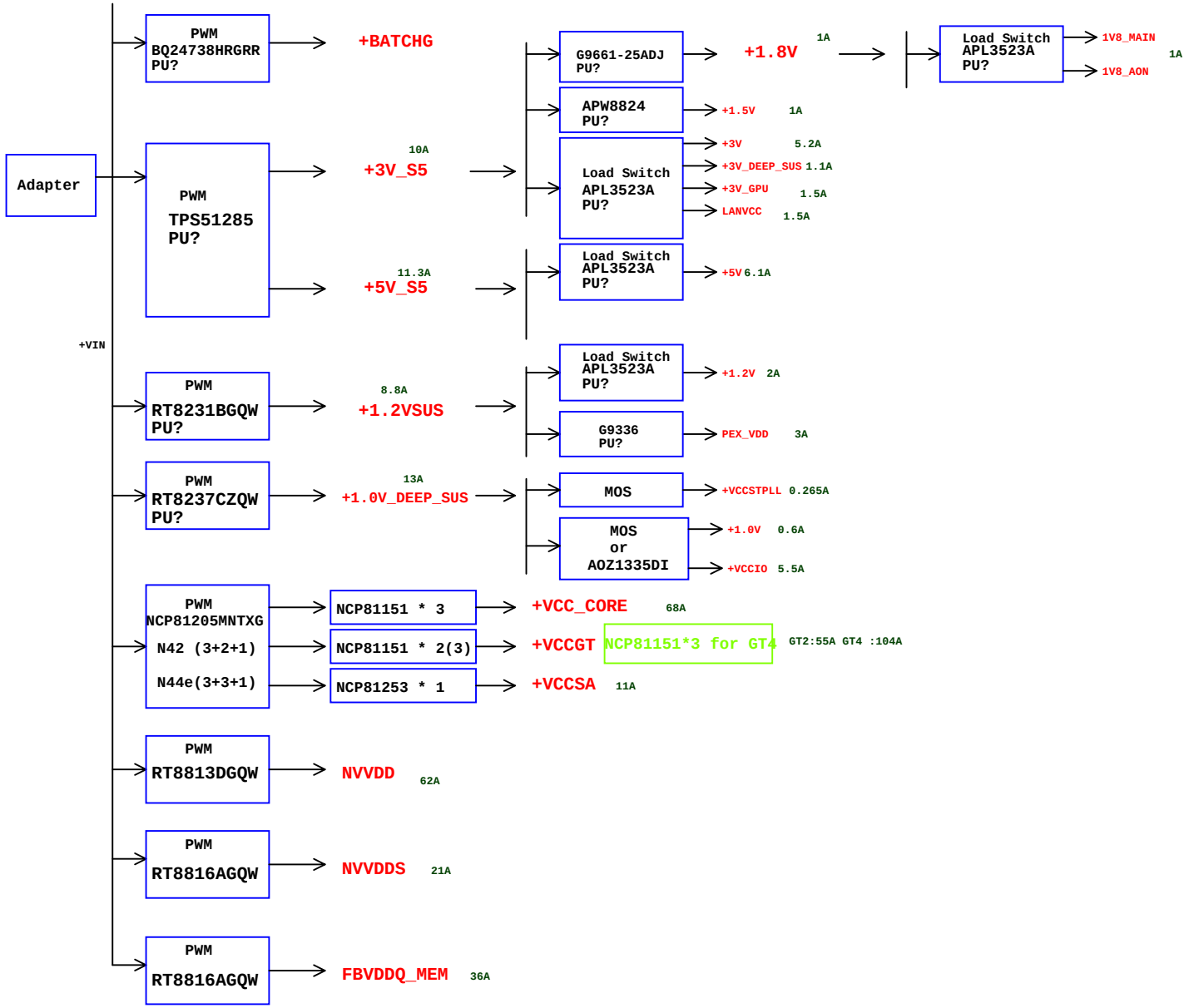
Date: Monday, October 17, 2016 Sheet 61 of 66

Power Delivery Map



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Power Deliver Map
Monday, October 17, 2016

(19,20,21,22,24,30,31,43,45,52) +5V
(18,33,34,35,36,39,40,41,42,47,50,52) +VIN

CPU BRACKET

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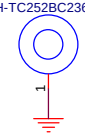

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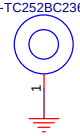

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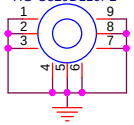

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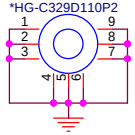

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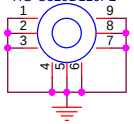

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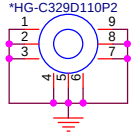

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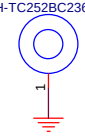

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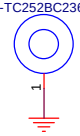

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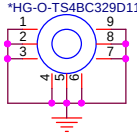

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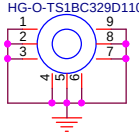

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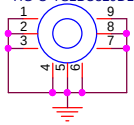

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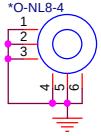

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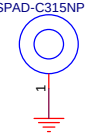

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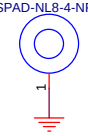

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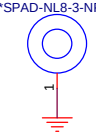

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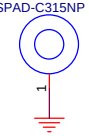

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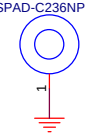

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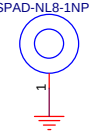
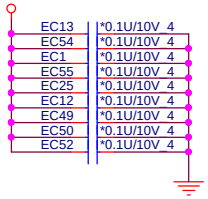


EMI

+5V



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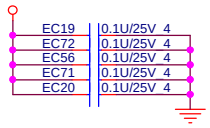
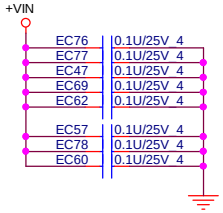


+VIN



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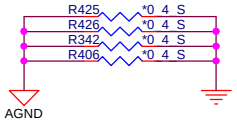

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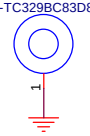

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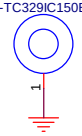

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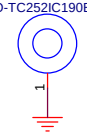

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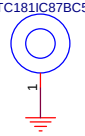

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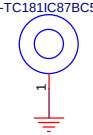

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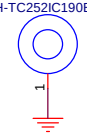

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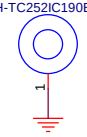

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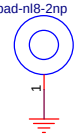

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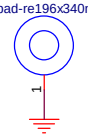

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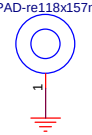

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Size	Document Number	Rev
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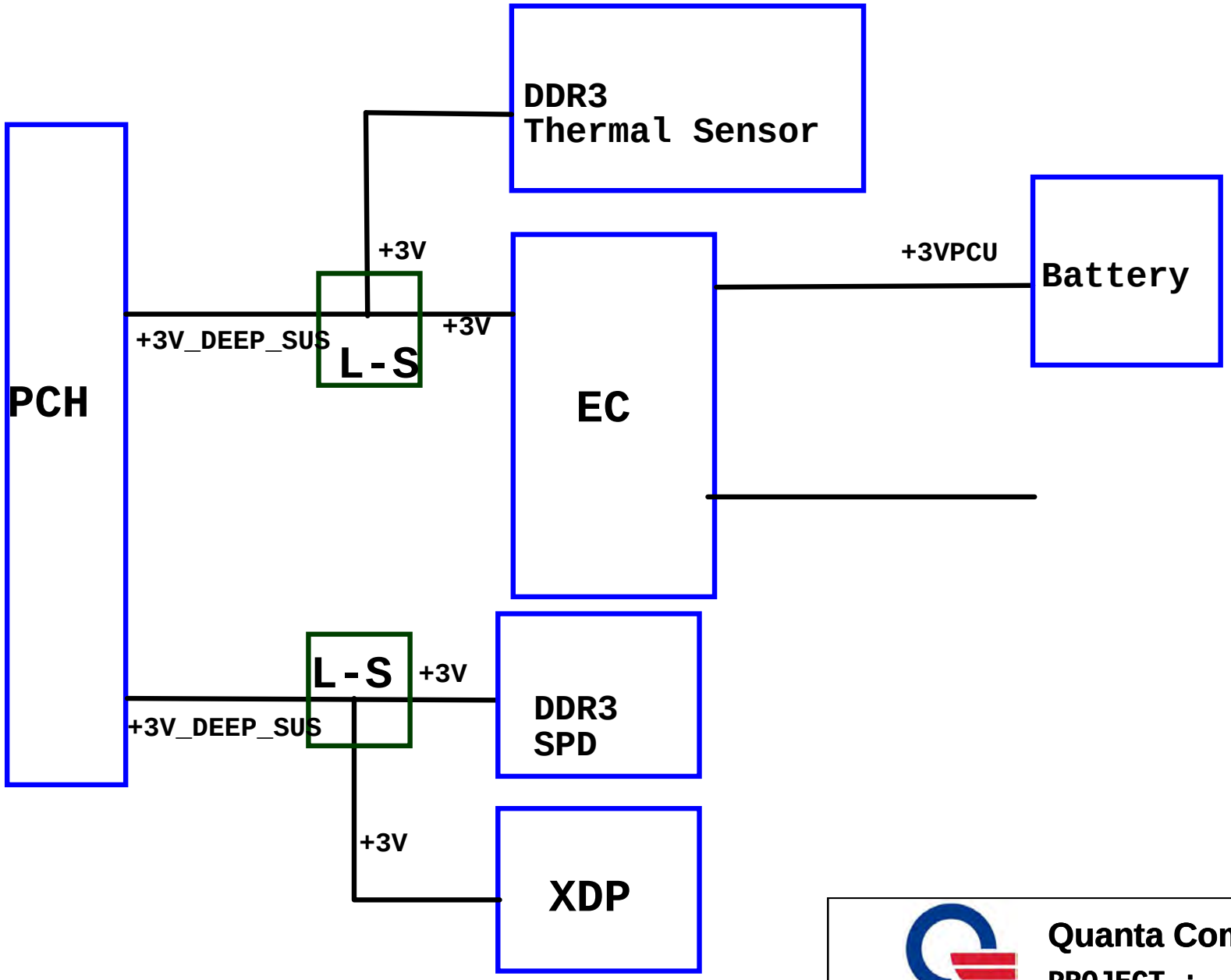
Date: Monday, October 17, 2016	Sheet 63 of 66	



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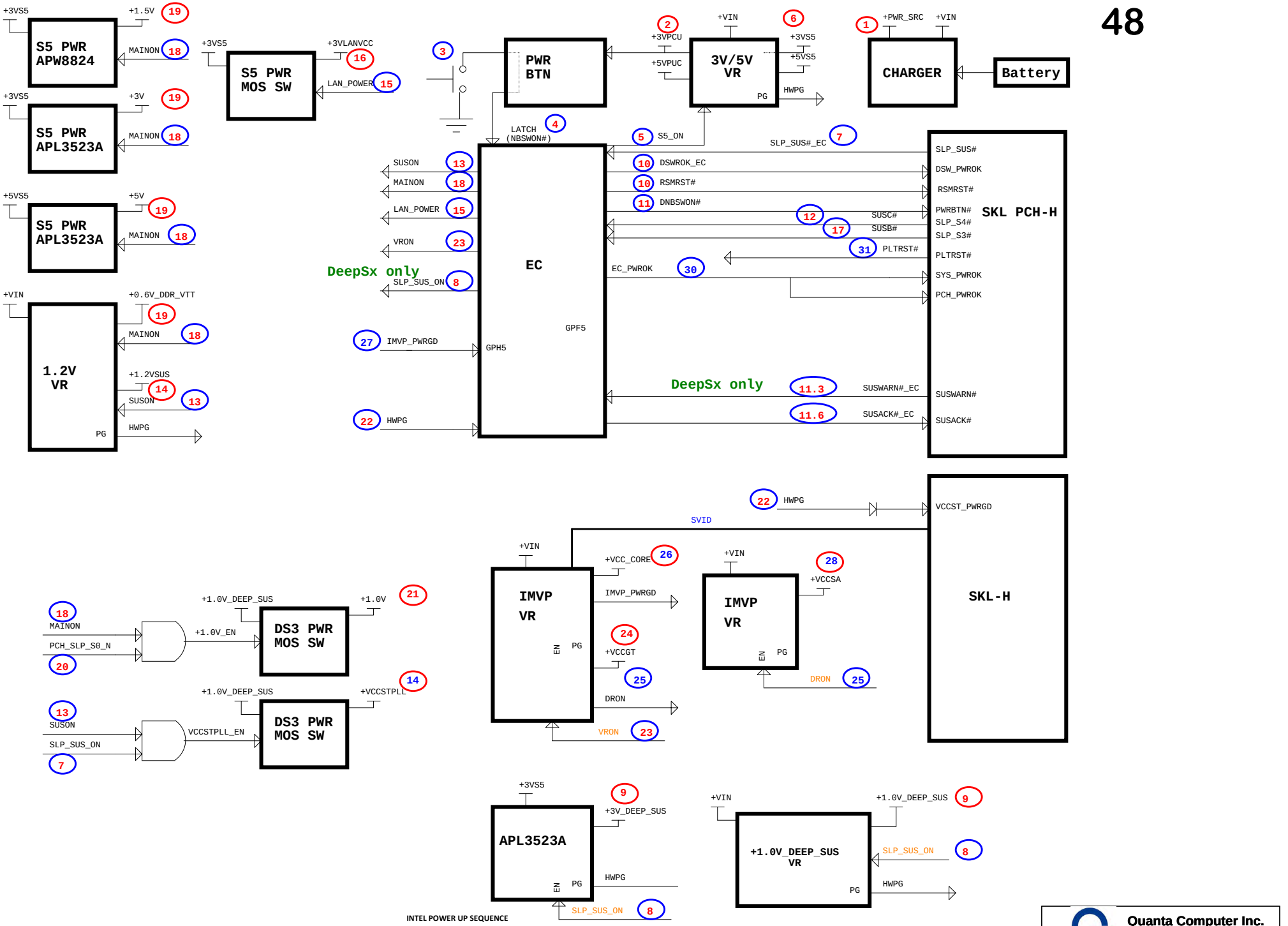
PROJECT :

Size	Document Number	Rev
A	SMBus Map	3B

Date: Monday, October 17, 2016 Sheet 64 of 66



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PROJECT :
Power sequencce diagram
Monday, October 17, 2016
65
66

2016	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
SDV	EC-A-01	19	8/10	R760	DP_Power add 0 ohm
	EC-A-02	19	8/10	Q70,R761,R762	DP_HPD change to dual mos type
	EC-A-03	20	8/10	R763	HDMI_Power add 0 ohm
	EC-A-04	12	8/10	Add U52,del U53	BIOS change socket to rom for B test
	EC-A-05	26	8/10	C835	change 0402 correct PN
	EC-A-06	26	8/10	C509,Y2	change cap,crystal for vendor recommend
	EC-A-07	53	8/10	U39	change PN for 2nd source team recommend
	EC-A-08	18	8/10	CN6	change to Vertical type &FP and upsidedown pin order
	EC-A-09	27	8/10	CN1	change to type-C FP
	EC-A-10	9	8/10	Q71,Q72,R766,C934	change GC6EN circuit
	EC-A-11	56	8/10	U55,U56,R767,R768,R769	GPU power down sequence
	EC-A-12	56	8/11		change from OVERT# to DGPU_OVT#
	EC-A-13	55	8/17		Reserve GPU external bios for debug use
	EC-A-14	30	8/19	R778,R779,R458,R448,R776,R777	cypress review CCG2 to Mux can't have cap
	EC-A-15	10	8/19	R246	EC S5 leakage form AC_PRESENT
	EC-A-16	2,10	8/19	R780,R781,R782,R783	xHCI Debug Capability Compliance issue
	EC-A-17	28	9/6	R161,R620	change Ilim to 93.1k ohm for 3A,asm R161 for type c hpd open drain
SIV	EC-B-01	13,19	10/17	R784,C785,C803	for DP to hdmi dongle cable issue
	EC-B-02	20	10/17	C10,C621	change 0805 size to 0402 size
	EC-B-03	56	10/17	R568	for remove R568 NV PWRGD path
	EC-B-04	27	10/19	C816,C936	for FAE suggest
	EC-B-05	10	10/26	R246	For ME check fail issue

Quanta Computer Inc.

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Size	Document Number	Rev
Custom	EC list-1	1A
Date: Wednesday, October 26, 2016	Sheet 66 of 66	