

ZZZ PCB@



PCB 1Q3 LA-D821P REV1 M/B 1
DA80017D010

UC1 KBL_15W_2+2@



S IC A31 FJ8067702739720 QKKS G0 2.4G
SA00009PJ0L

UC1 SKL_15W@



S IC FJ8066201931104 SR2EU D1 2.3G A31!
SA000092N4L

UC1 KBL_15W_I3@



SA0000A382L
KBL U SR2VN
S IC FJ8067702739738 SR2VN H0 2.4G A31!

UC1 KBL_15W_I5@



SA0000A372L
KBL U SR2VL
S IC FJ8067702739739 SR2VL H0 2.5G A31!

UC1 KBL_15W_I7@



SA0000A342L
KBL U SR2VM
S IC FJ8067702739740 SR2VM H0 2.7G A31!

UC1 KBL_15W_2+1@



S IC A31 FJ8067702739920 QKKQ G0 1.7G
SA00009QM0L

UC1 KBL_15W_SUP_ES@



S IC A31 FJ8067702739718 QKJW G0 2.6G
SA00009UR0L

Compal Confidential

BJA50 / BJA40 / BKD50 / BKD40 MB Schematic Document

LA-D821P

Rev: 1.0
2016.05.30

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
1	USB3.0 Port0
2	USB3.0 Port1
3	USB3.0 Port2 (IO Board)
4	USB2.0 Port0
5	HD CAM
6	Card Reader
7	Touch Screen
8	BT
9	Finger Printer
10	N/A

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				USB3.0 Port0
USB3.0-2	SSIC-1			USB3.0 Port1
USB3.0-3	SSIC-2			USB3.0 Port2 (IO Board)
USB3.0-4				N/A
USB3.0-5		PCIE-1		GPU
USB3.0-6		PCIE-2		GPU
		PCIE-3		GPU
		PCIE-4		GPU
		PCIE-5		WLAN
		PCIE-6		GLAN
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	N/A
		PCIE-9		N/A
		PCIE-10		N/A
		PCIE-11	SATA-1*	N/A
		PCIE-12	SATA-2	SATA SSD

PM TABLE

power plane State	+RTC_CELL +RTC_VCC +3VLP +19VB	+1.0V_PRIM +1.0V_MPHYPLL +5VALW +3VALW +3.3V_ALW_DSW +1.8V_PRIM	+1.0V_VCCST +1.2V_DDR +2.5V_MEM +3VALW_PCH	+1.0VS_VCCIO +1.0V_VCCSTG +VCC_GT +VCC_SA +VCC_CORE +GPU_CORE +5VS +3VS +1.8VS +0.6V_DDR_VTT
S0	ON	ON	ON	ON
S3	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	OFF	OFF
S4&S5 / DC	ON	OFF	OFF	OFF

Board ID & Model ID table

Item	Pull-down(K ohm)	Pull-up (K ohm)	Voltage	Board ID/Model ID
1	100	10.0	3.000	EVT(X00)
2	100	13.7	2.902	DVT1(X01)
3	100	17.8	2.801	DVT2(X02)
4	100	22.1	2.703	Pilot(A00)
5	100	27.0	2.598	
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	

CPU PWR
GPU PWR
Peripheral Device PWR

ADAPTER

CHARGER
ISL95521HRZ
(PU703)

BATTERY

+PWR_SRC
(+19VB)

ISL95859HRTZ
(PU602)

ISL95808HRZ
(PU606)

IMVP_VR_ON

+VCC_SA

AOZ5019QI
(PU603)

IMVP_VR_ON

+VCC_CORE

AOZ5019QI
(PU605)

DRMOS_EN

+VCC_GT

RT8812AGQW
(PU1100)

DGPU_MAIN_EN

+GPU_CORE

RT8207PGQW
(PU200)

SIO_SLP_S4#

+1.2VP

+1.2V_DDR

0.6V_DDR_VTT_ON

+0.6VSP

+0.6V_DDR_VTT

SY8286RAC
(PU300)

(NGN-DS3)
POK

+1VALWP

+1.0V_PRIM

0ohm 0805
(R5214)

+DCBATOUT_LCD

0ohm 0402
(R6528)

+IR_LED+

SY8286RAC
(PU1400)

1.35V_PWR_EN

+1.35VGPUP

+1.35VS_VRAM

SY8286CRAC
(PU102)

EN_3V
ENLDO_3V5V

+5VALWP

+5VALW

AP22802BW5
(U3504)

+USB30_VCCB

TPS22961
(UZ19)

SIO_SLP_S3#
SIO_SLP_S0#

+1.0V_VCCSTG_C

JUMP
(JP17)

+1.0V_MPHYPLL

TPS22967
(UZ21)

SIO_SLP_S4#

+1.0V_VCCST

EM5209VF
(UV10)

DGPU_PWBOK

+1.0VS_DGPU

TPS2544RTER
(UUS5)

USB_POWERSHARE_VBUS_EN

+USB30_VCCA

AP22802BW5
(U3504)

USB_EN#

+USB30_VCCB

AP22802BW5
(U3505)

USB_EN#

+USB30_VCCC

EM5209VF
(UZ2)

JP21
SIO_SLP_S3#

+5VS

0ohm 0603
(R5232)

+TPAN_VDD

0ohm 0805
(R5601)

5V_HDD

RB551V-30
(D5204)

FUSE 1.1A_6V
(F6202)

5V_HDMI

FUSE 0.5A_13.2V
(F6201)

+5V_KB_BL

RT9724GB
(U5201)

LCDVDD_EN

LCDVDD

SY6288C20AAC
(UL3)

+3.3V_LAN

0ohm 0805
(R5809)

+3.3V_WLAN

DMG2301U-7
(QV6)

DGPU_PWR_EN

+3VS_DGPU_AON

0ohm 0603
(R5229)

+3.3V_CAM

JUMP
(JP1)

+3VS_SSD

RT8061AZQW
(PU500)

(NGN-DS3)
POK

+1.8VALWP

+1.8V_PRIM

LN2306LT1G
(Q6205)

+3VS

+1.8V_AVDD

CPVDD

RT9059GSP
(PU800)

SIO_SLP_S4#

+2.5VP

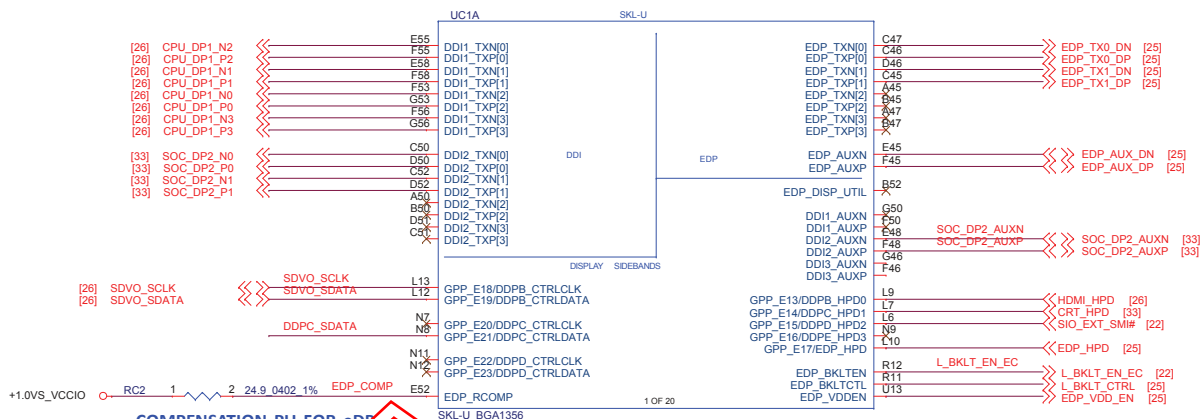
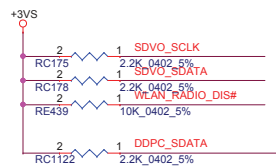
+2.5V_MEM

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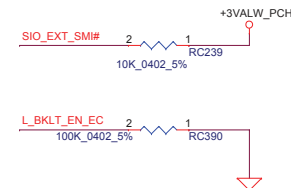
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COMPENSATION PU FOR EDP
 CAD Note: Trace width=20 mils, Spacing=25mil, Max length=100 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



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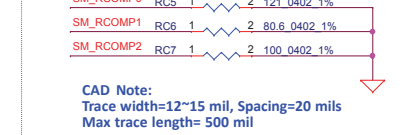
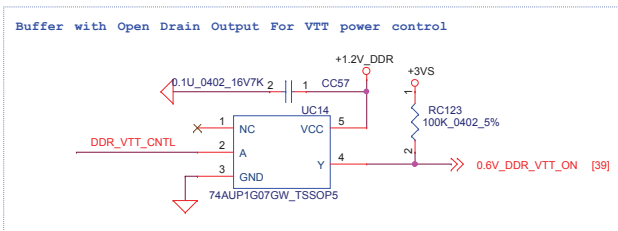
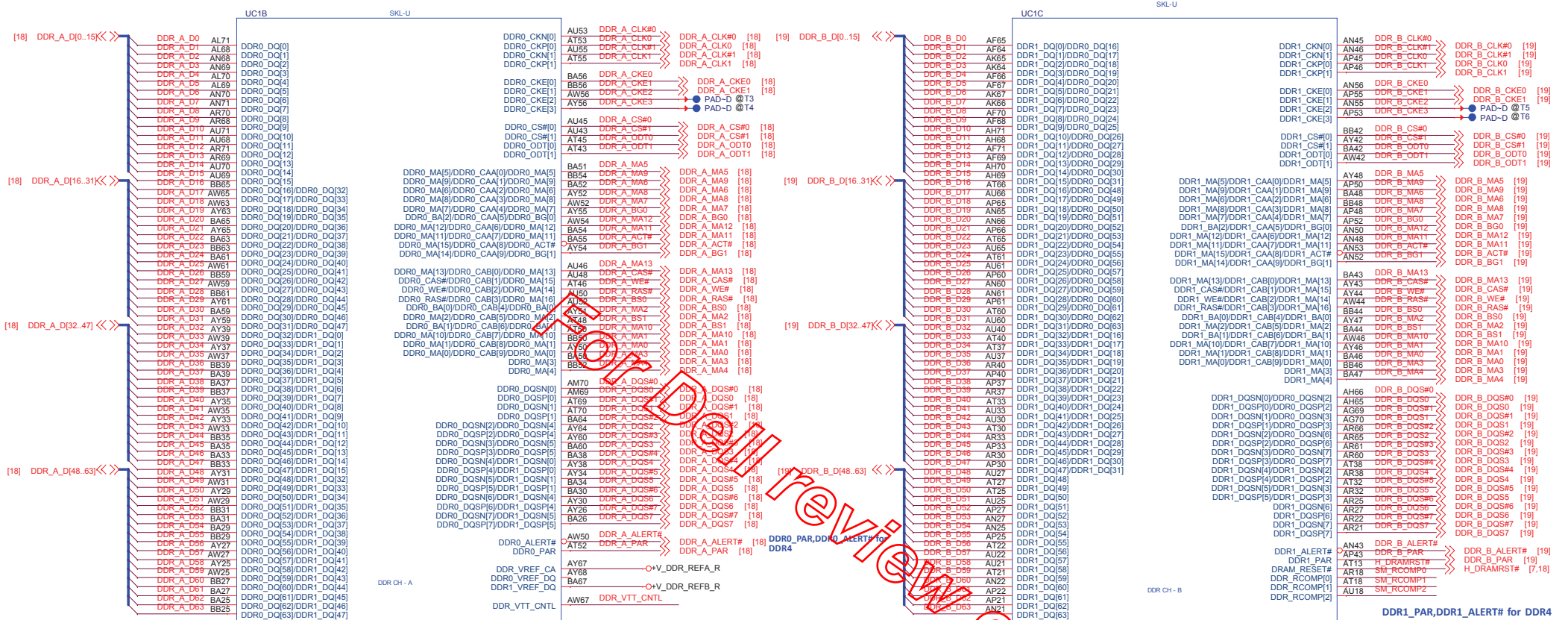
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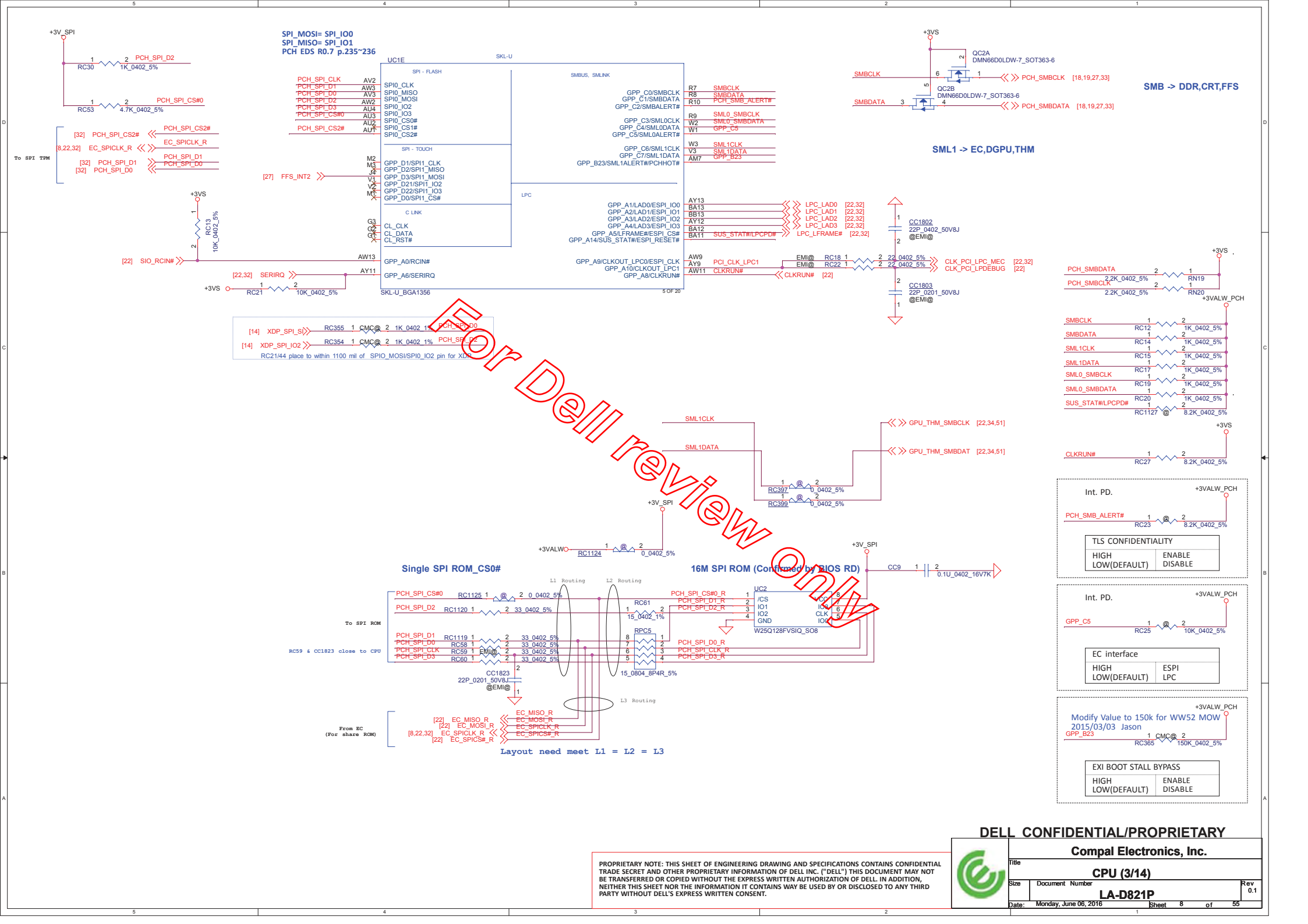
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DDR4, Ballout for B2B(Interleave)



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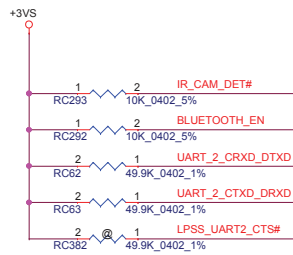


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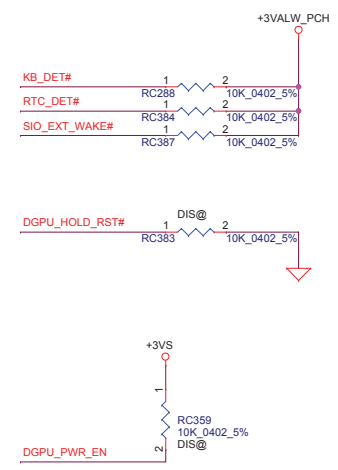
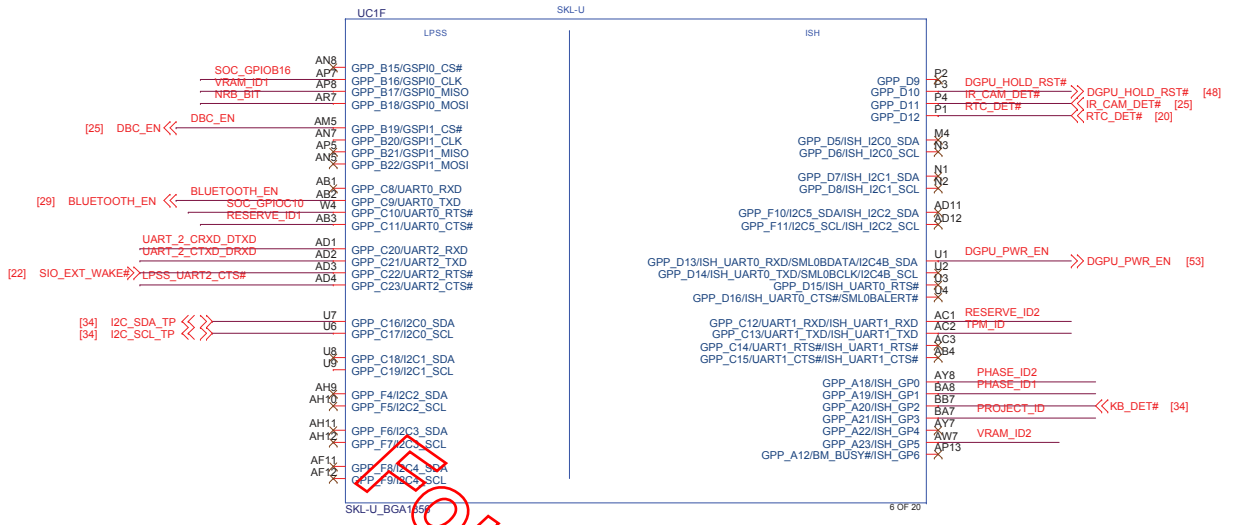
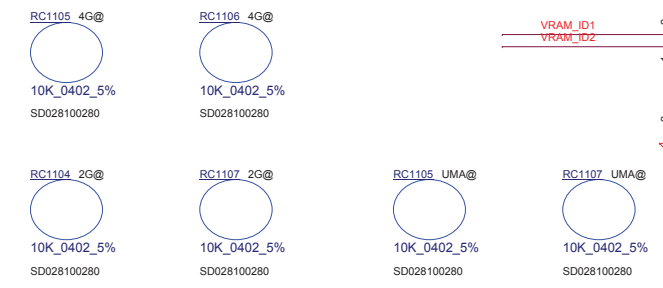
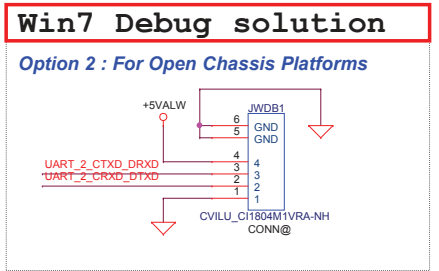
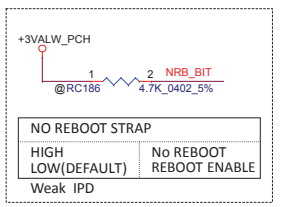
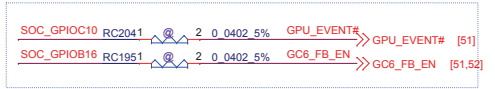
CPU (3/14)

LA-D821P

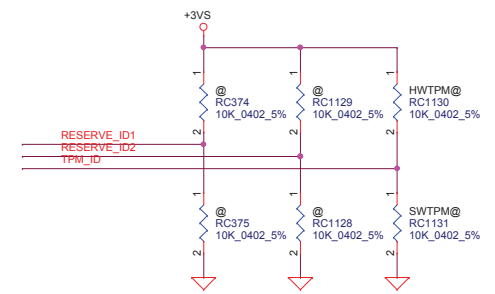
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TO DGPU



PHASE ID	PHASE_ID1 (GPP_A19)	PHASE_ID2 (GPP_A18)
EVT	0	0
DVT1	0	1
DVT2	1	0
Pilot		1

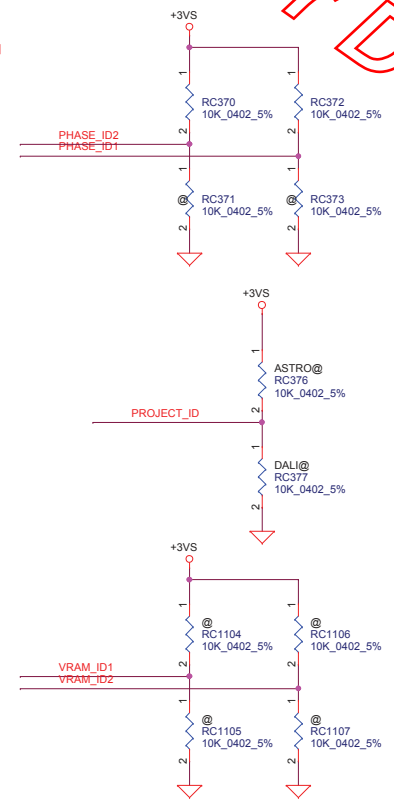


PROJECT ID	PROJECT_ID (GPP_A21)
Dali	0
Astro	1

PROJECT ID	TPM_ID (GPP_C13)
SW_TPM	0
HW_TPM	1

VRAM ID (PCBA VRAM Size Config.)	VRAM_ID2 (GPP_A23)	VRAM_ID1 (GPP_B17)
UMA	0	0
2G	0	1
4G	1	0
Reserved	1	1

RESERVE ID	RESERVE_ID1 (GPP_C11)	RESERVE_ID2 (GPP_C12)



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GPU

WLAN

LAN

HDD

SSD

UC1H

SKL-U

PCIe/USB3/SATA

SSIC / USB3

USB2

SKL-U_BGA1356

8 OF 20

USB3 Port 0

USB3 Port 1

USB3 Port 2

USB3 Port 0

USB3 Port 1

USB3 Port 2

USB2 Port 0

HD CAM

Card Reader

Touch Screen

BT

Finger Printer

3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U



There are 16 HSIO lanes on SKL PCH-LP U Series, supporting the following port configurations:

- Up to 12 PCIe* lanes (multiplexed with USB 3.0 ports, SATA Ports)
 - Only a maximum of 6 PCIe* ports (or devices) can be enabled at any time.
 - Ports 1-4, Ports 5-8, and Ports 9-12, can each be individually configured as 4x1, 2x2, 1x2 + 1x1, or 1x4.
- Up to 3 SATA ports (multiplexed with PCIe*)
 - SATA Port 1 has the flexibility to be mapped to either PCIe* Port 8 or Port 11.
- Up to 6 USB 3.0 ports (multiplexed with PCIe*)
 - USB Dual Role (COTG) capability is available on USB 3.0 Port 1.
 - One SSIC x1 port is multiplexed with USB 3.0 Port 2.
- One GBE lane
 - GBE can be mapped into one of the PCIe* Ports 3-5 and Ports 9-10.
 - When GBE is enabled, there can be at most up to 5 PCIe* ports enabled.
- Up to 2 Intel RST for PCIe* storage devices supported
 - Devices can be x2 or x4.
 - Devices can be implemented on PCIe Ports 5-8 and Ports 9-12.

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/OTG	USB 3.0/SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe	SATA	SATA	PCIe/LAN	PCIe/LAN	N/A	N/A
Premium-U	USB 3.0/OTG	USB 3.0/SSIC	USB 3.0	USB 3.0	PCIe/USB 3.0	PCIe/USB 3.0	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe	PCIe/SATA	PCIe/SATA	PCIe/LAN	PCIe/LAN	PCIe/SATA	PCIe/SATA
Premium-Y	USB 3.0/OTG	USB 3.0/SSIC	USB 3.0	USB 3.0	PCIe/USB 3.0	PCIe/USB 3.0	PCIe/LAN	PCIe/LAN	PCIe/LAN	PCIe	PCIe/SATA	PCIe/SATA	PCIe/LAN	PCIe/LAN	N/A	N/A

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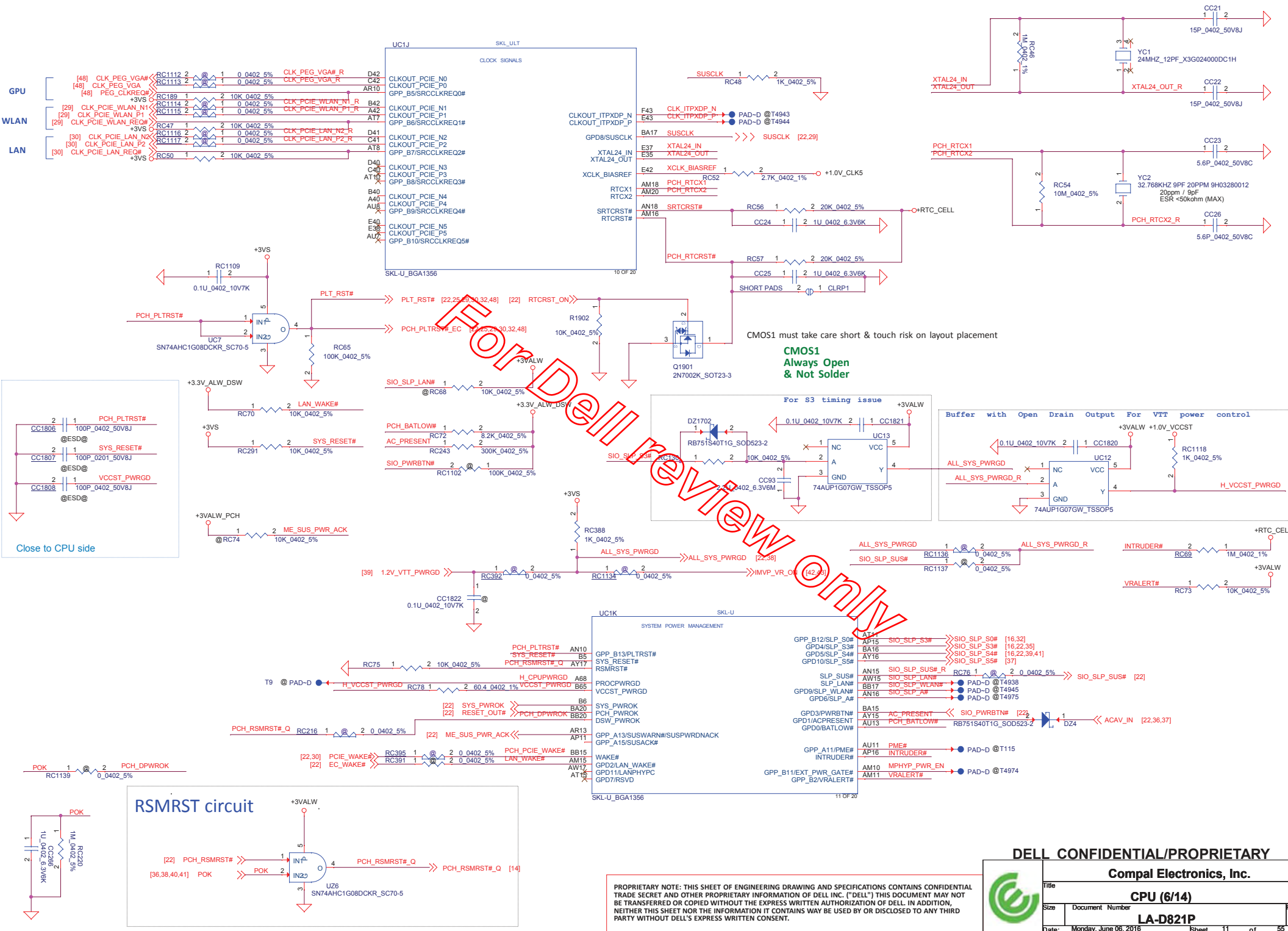


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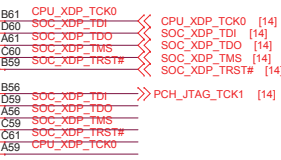
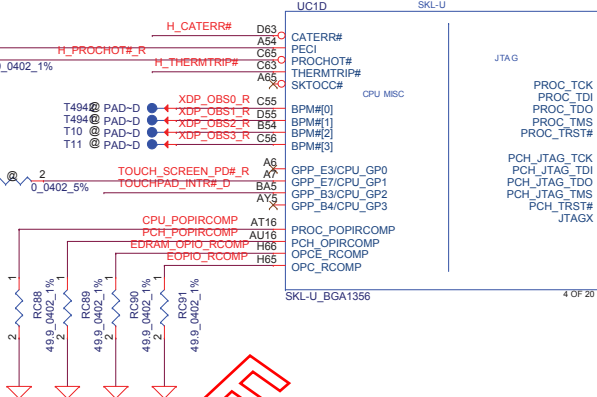
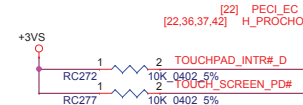
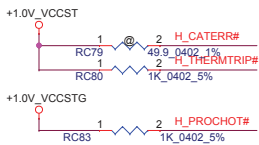
GPU
WLAN
LAN



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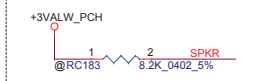
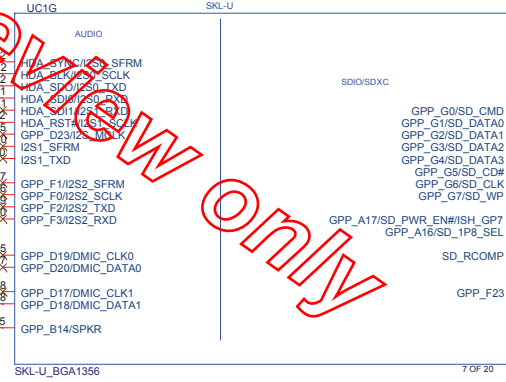
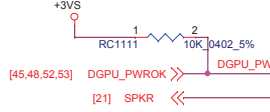
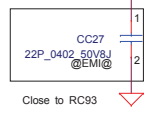
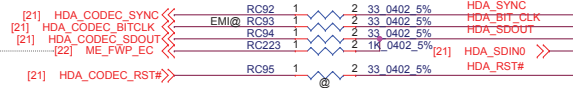
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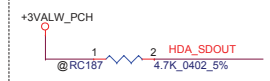
ME_FWP_EC

LOW = ENABLE --> ME lock can't update ME

HIGH = DISABLE --> ME unlock can update ME



TOP SWAP STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE



Flash Descriptor Security override	
HIGH	DISABLE
LOW(DEFAULT)	ENABLE

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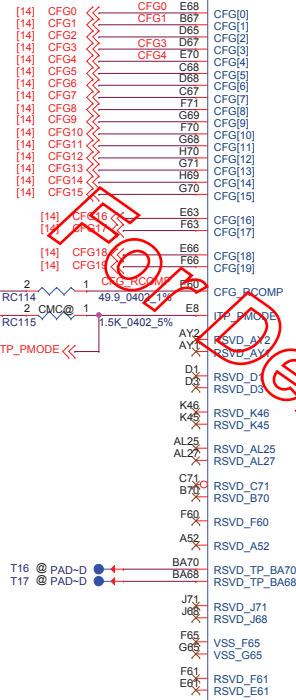
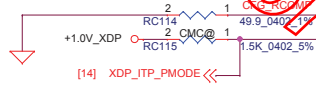
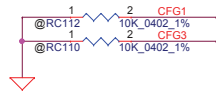
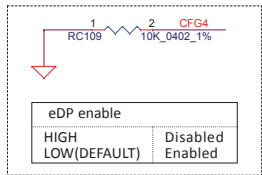
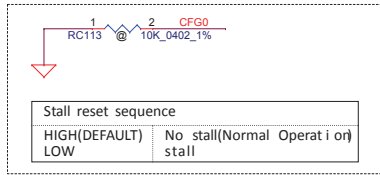
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CFG[2][5][6][7] for SKYLAKE-H CPU CFG strap pin



For 2+3e Solut i on

PM_ZVM#
Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.

PM_MSM#
Minimum Speed Mode: Control signal to VccEOP10 VR (connected only in 2 VR solut i on f or OPQ.

Follow 546765_20160609_Skylake_MOW_Rev_1_0
Stuff 100k (RC184) for Cannonlake.
Un-stuff 100k (RC184) for Skylake

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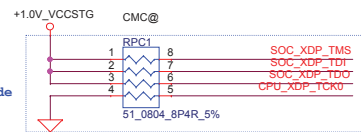
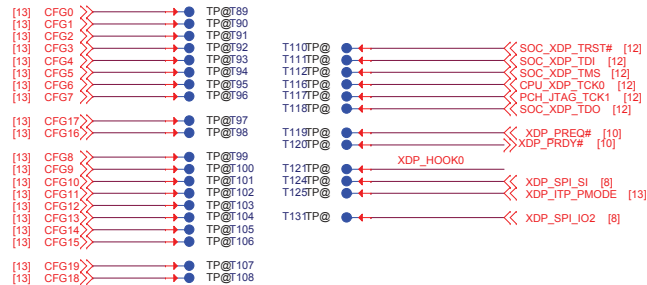
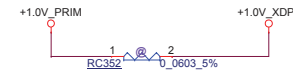


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PRIMARY CMC CONN

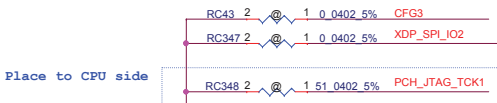


Place to CPU side

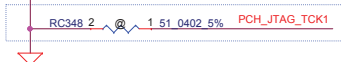


XDP_SPI_IO2 = XDP_PRESENT_PCH

```
CFG3 = XDP_PRESENT_CPU
```

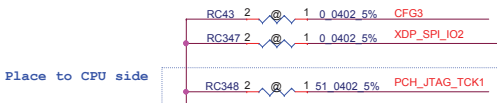


Place to CPU side

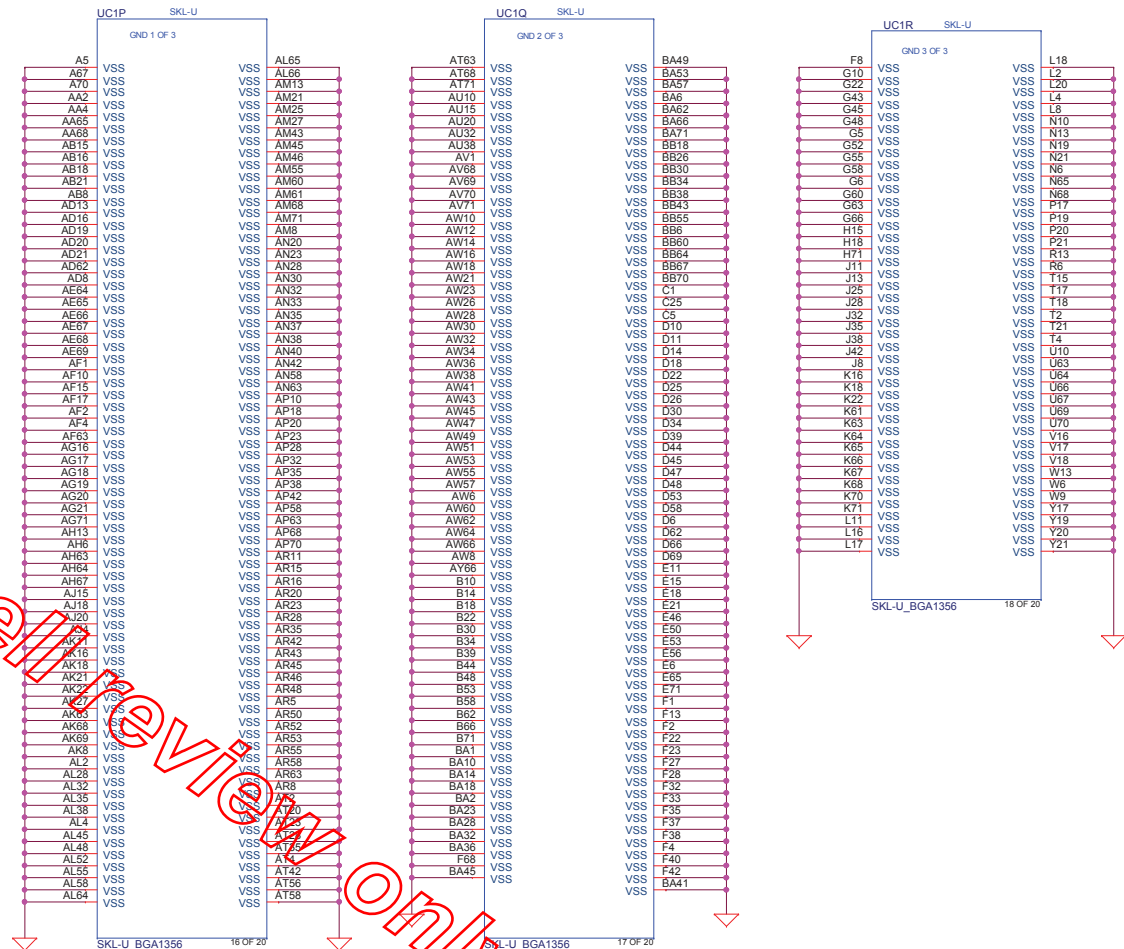
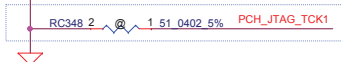


XDP_SPI_IO2 = XDP_PRESENT_PCH

```
CFG3 = XDP_PRESENT_CPU
```



Place to CPU side



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V VID option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage up to 1.00V will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, that specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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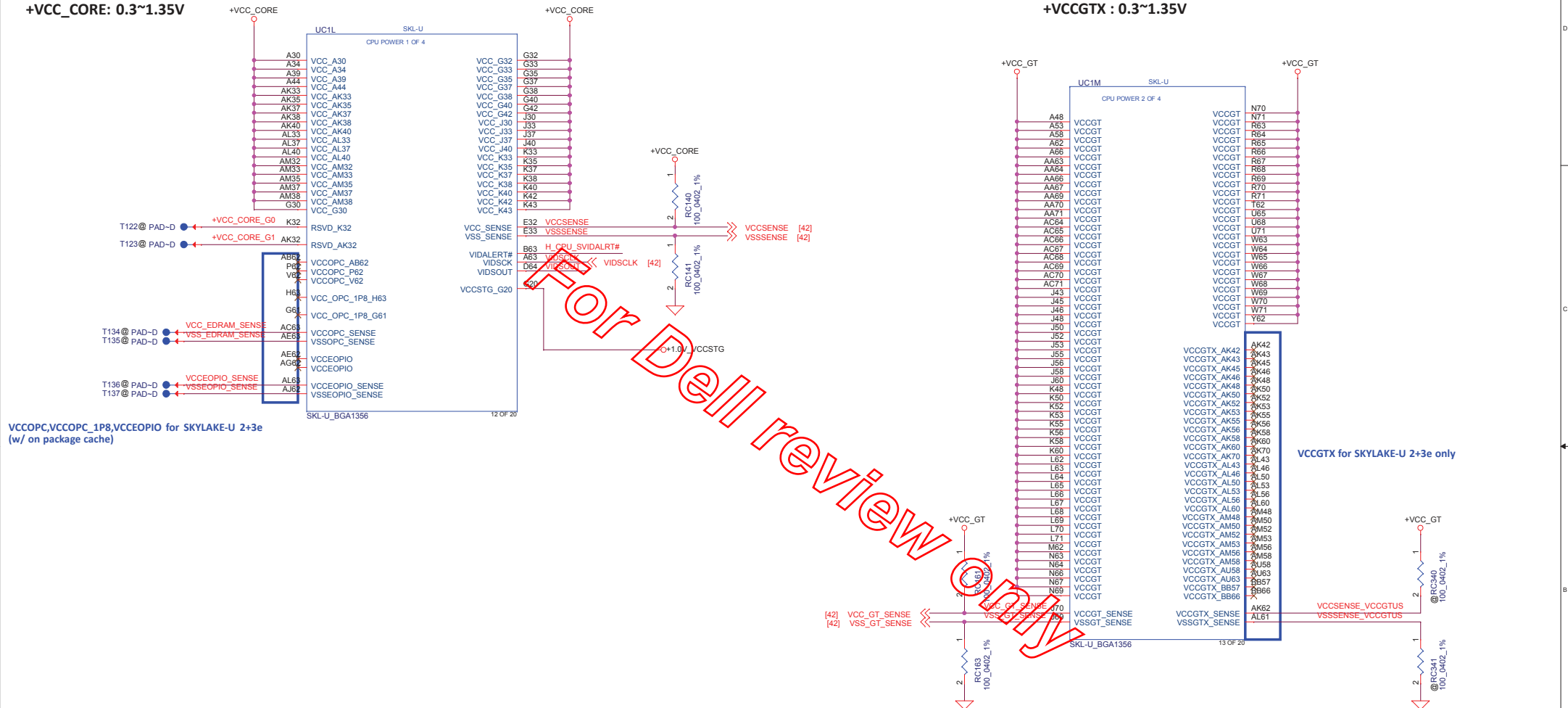


PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

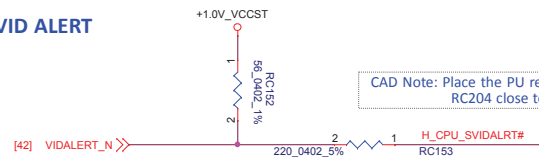
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

+VCC_CORE: 0.3~1.35V

+VCCGT: 0.3~1.35V
+VCCGTx: 0.3~1.35V

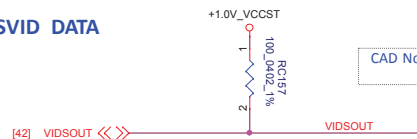


SVID ALERT



CAD Note: Place the PU resistors close to CPU
RC204 close to CPU 300 - 1500mils

SVID DATA



CAD Note: Place the PU resistors close to CPU
RC208 close to CPU 300 - 1500mils

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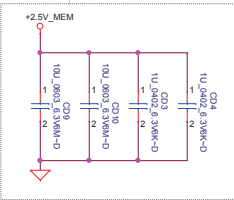
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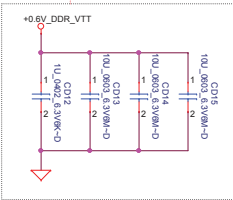
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CPU (10/14)			
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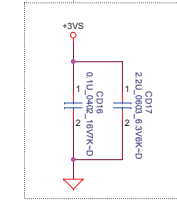
Layout Note:
Place near JDIMM1.257,259



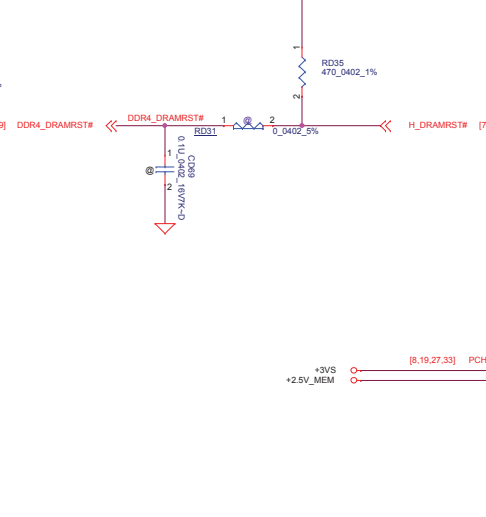
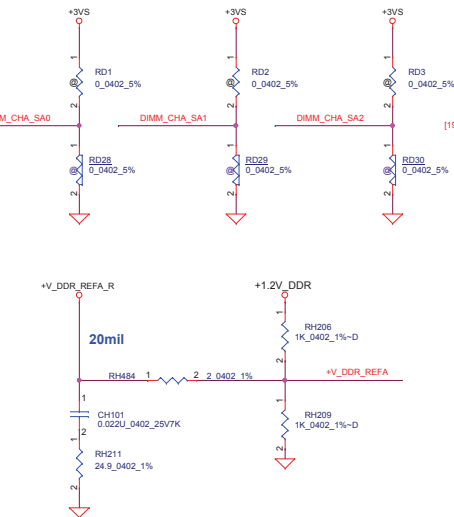
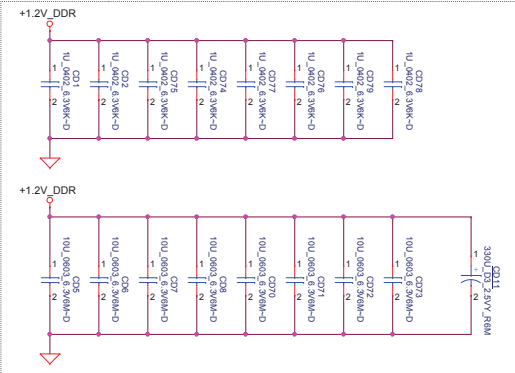
Layout Note:
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Layout Note:
Place near JDIMM1.255



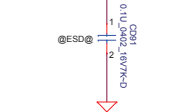
Layout Note:
Place near JDIMM1



[7] DDR_A_D0_63
[7] DDR_A_MA0_13
[7] DDR_A_DQ5#D_7
[7] DDR_A_DQ5#_7



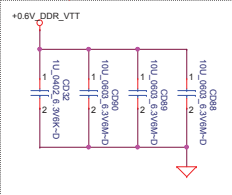
place cap near DIM RESET PIN



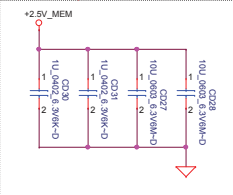
All VREF traces should
have 10 mil trace width

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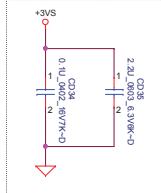
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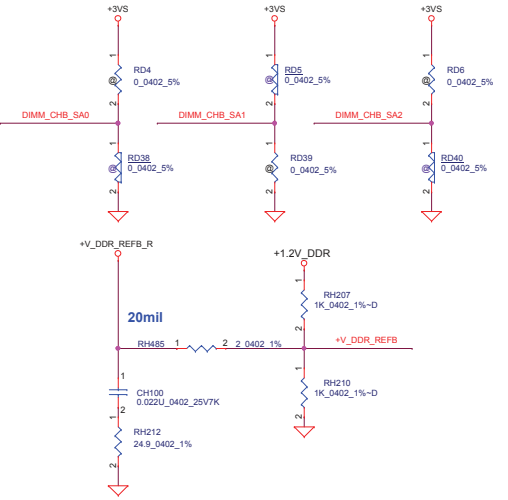
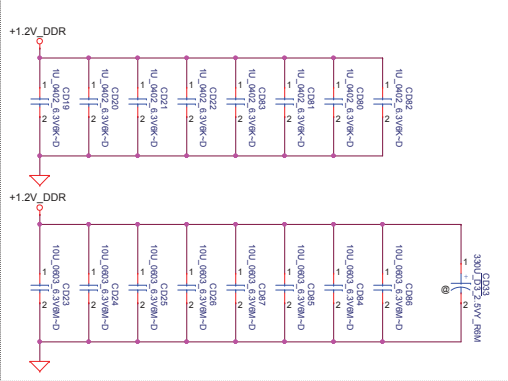
Layout Note:
Place near JDIMM2.257,259



Layout Note:
Place near JDIMM2.255

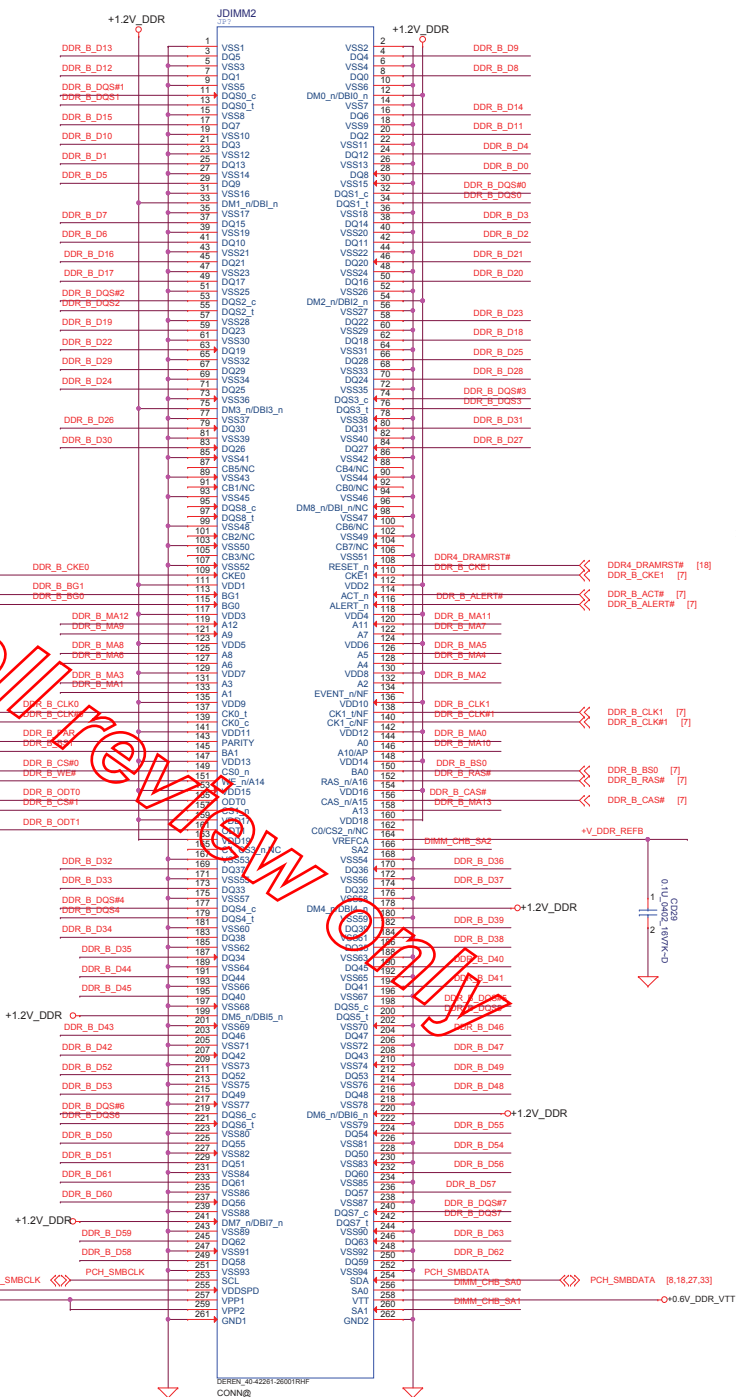


Layout Note:
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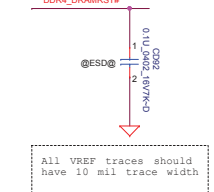


DDR_B_D0[63]
DDR_B_MA0[13]
DDR_B_DQS#0[7]
DDR_B_DQS#0[7]

For Deliberate Review Only



place cap near DIMM RESET PIN

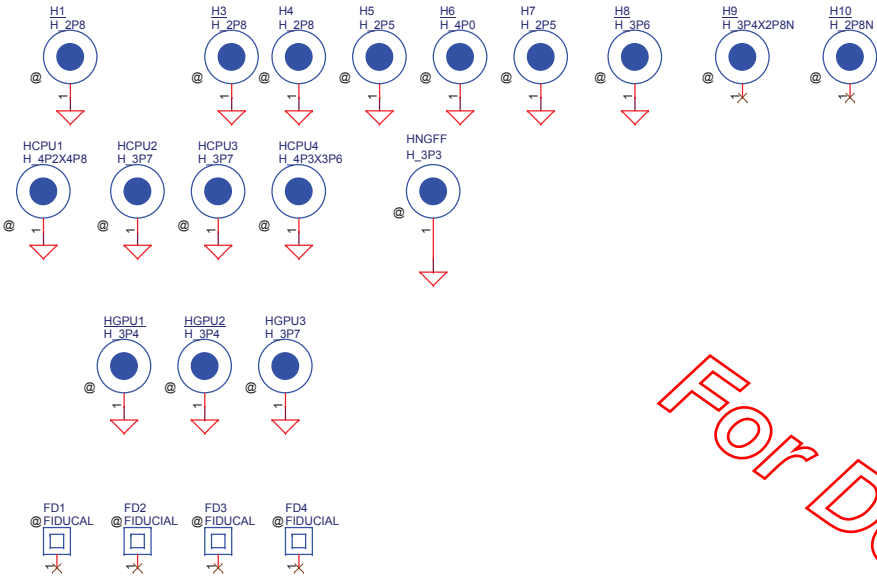


All VREF traces should
have 10 mil trace width

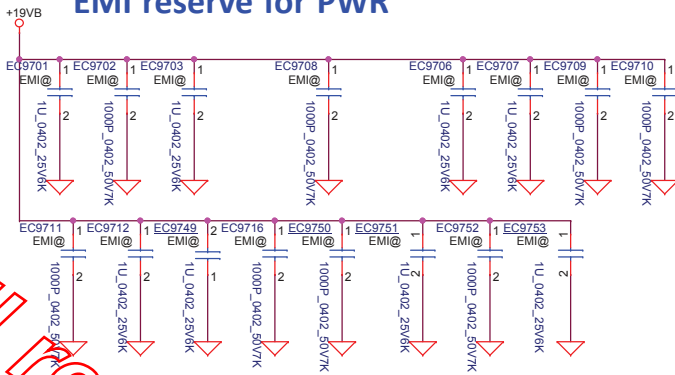
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Main Func = Other

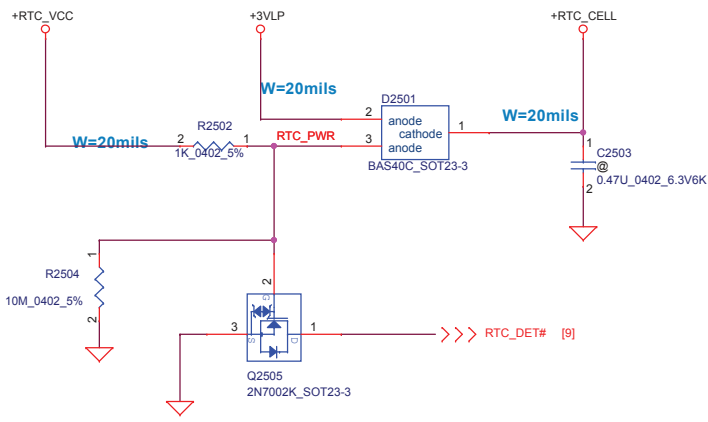
Screw hole/FD/EMI stop



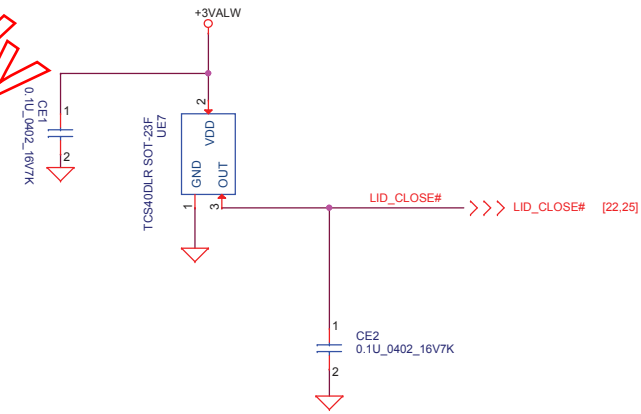
EMI reserve for PWR



Main Func = RTC

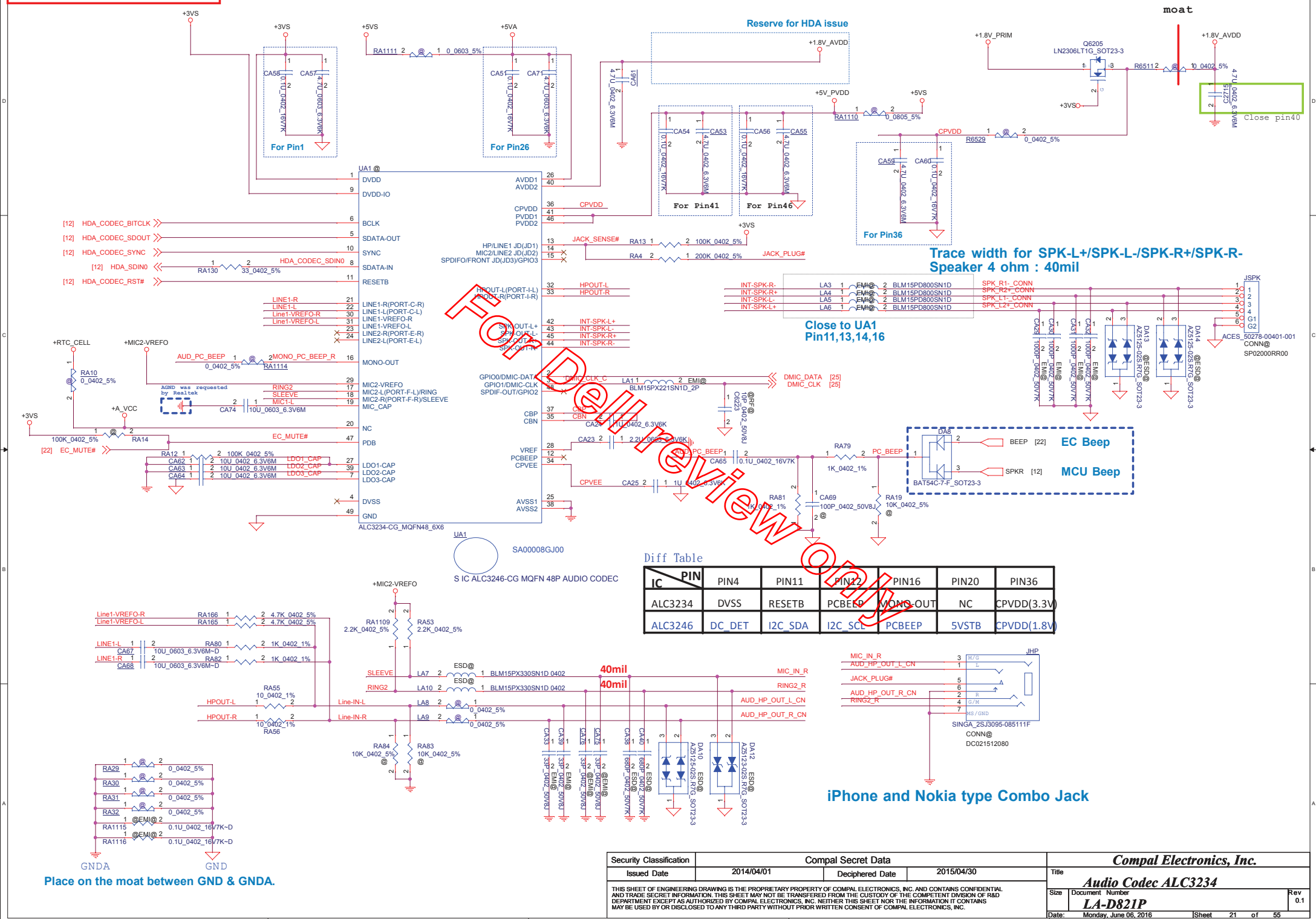


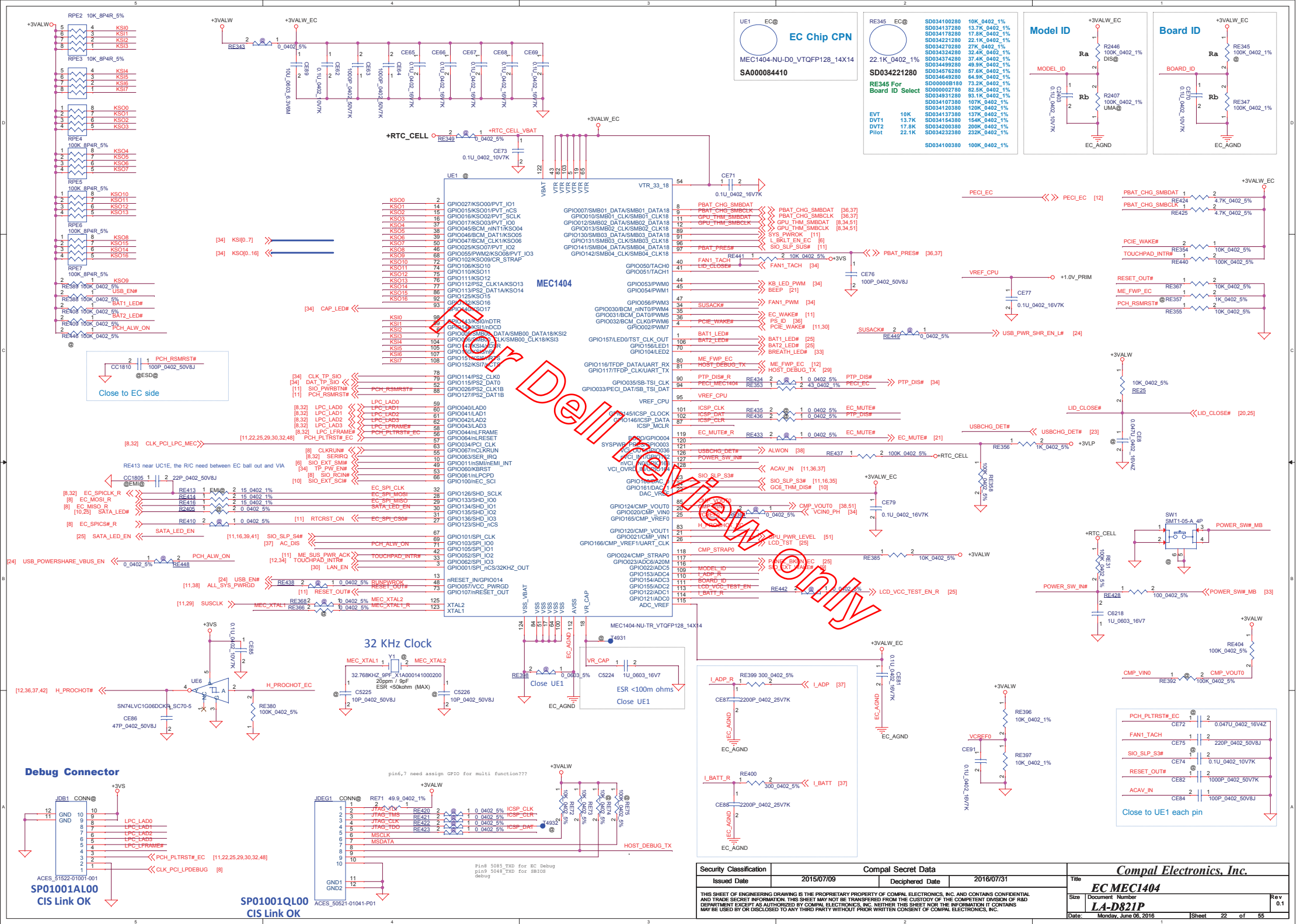
Main Func = LID Switch



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Main Func = Audio

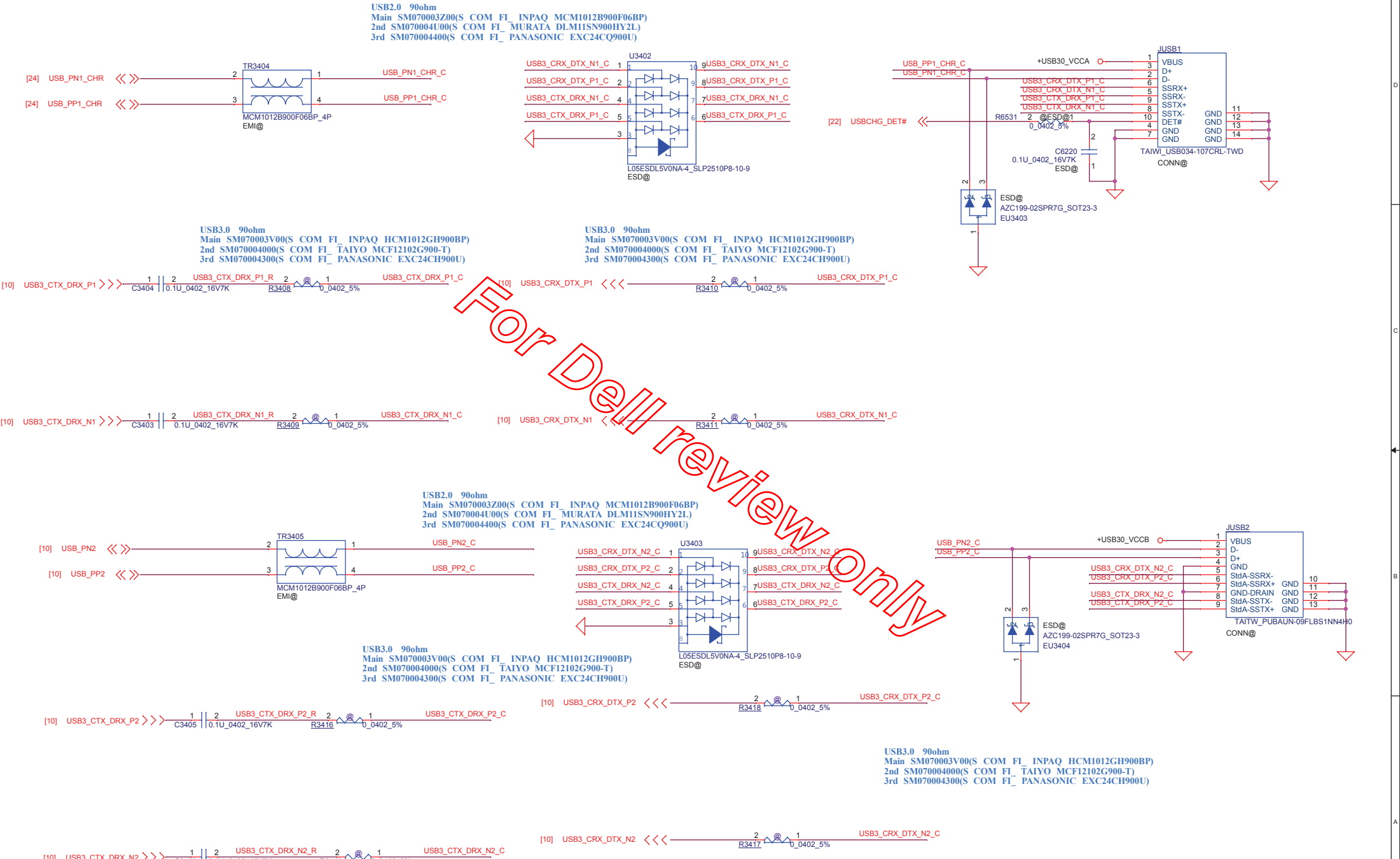




Main Func = USB3.0 Port1/Port2

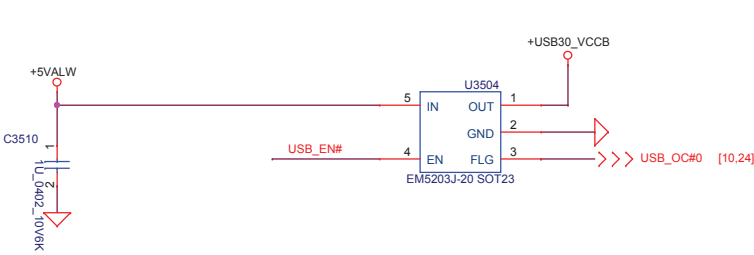
USB3.0 Port1

USB2.0 Port2 and USB2.0 Port3 are on IOBD

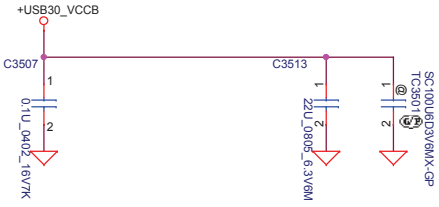


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				Size	Document Number
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Main Func = USB3.0 Port2

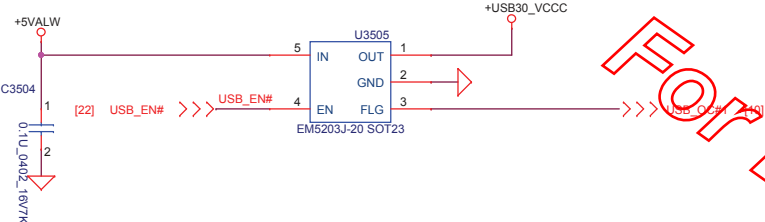


USB3.0 Port2



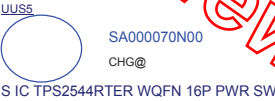
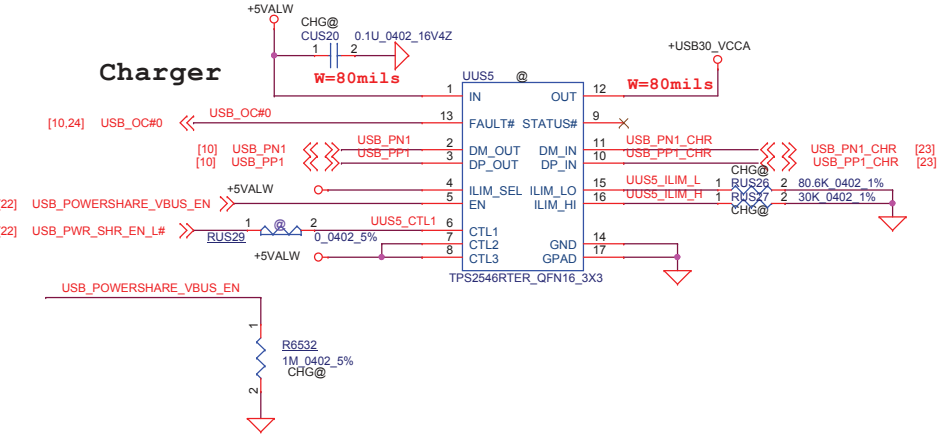
Main Func = USB3.0 Port3

USB3 Port3/USB2 Port1 (IO Board)



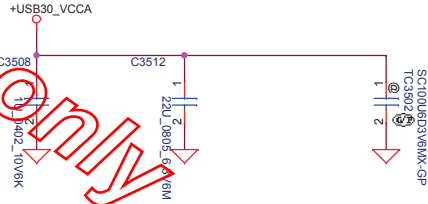
Main Func = USB Chager

Charger

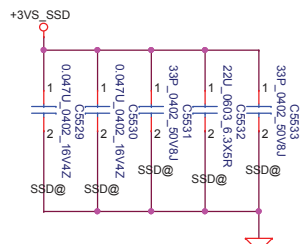


Diff Table

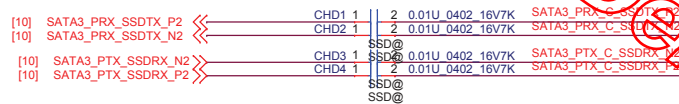
IC	PIN	PIN9
TPS2546	STATUS#	
TPS2544	NC	



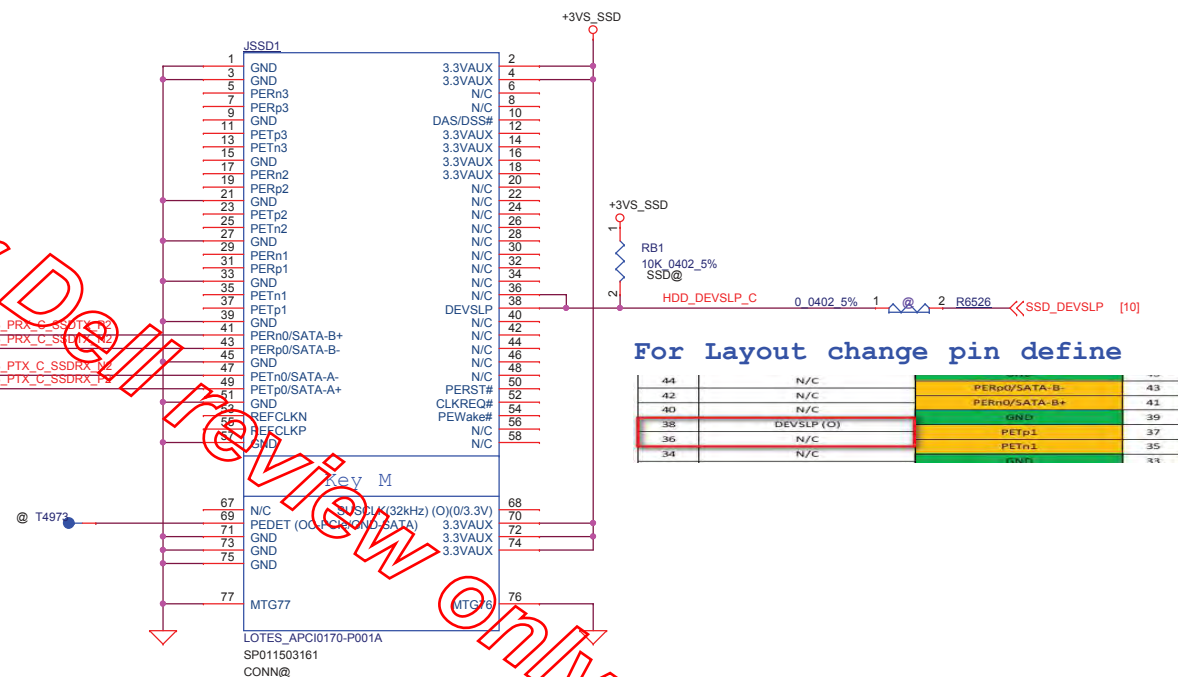
Charger CT	CTL1	CTL2	CTL3	ILIM_SEL
EC GPIO	GPXIOA07 (pin104)	GPIO22 (pin41)	GPXIOA11 (pin108)	GPIO21 (pin40)
S0/S3 (CDP)	1	1	1	1
S4/S5 (DCP)	0	1	1	1



2/6 TX Cap change P/N,
Now It's 0402 0ohm resistor



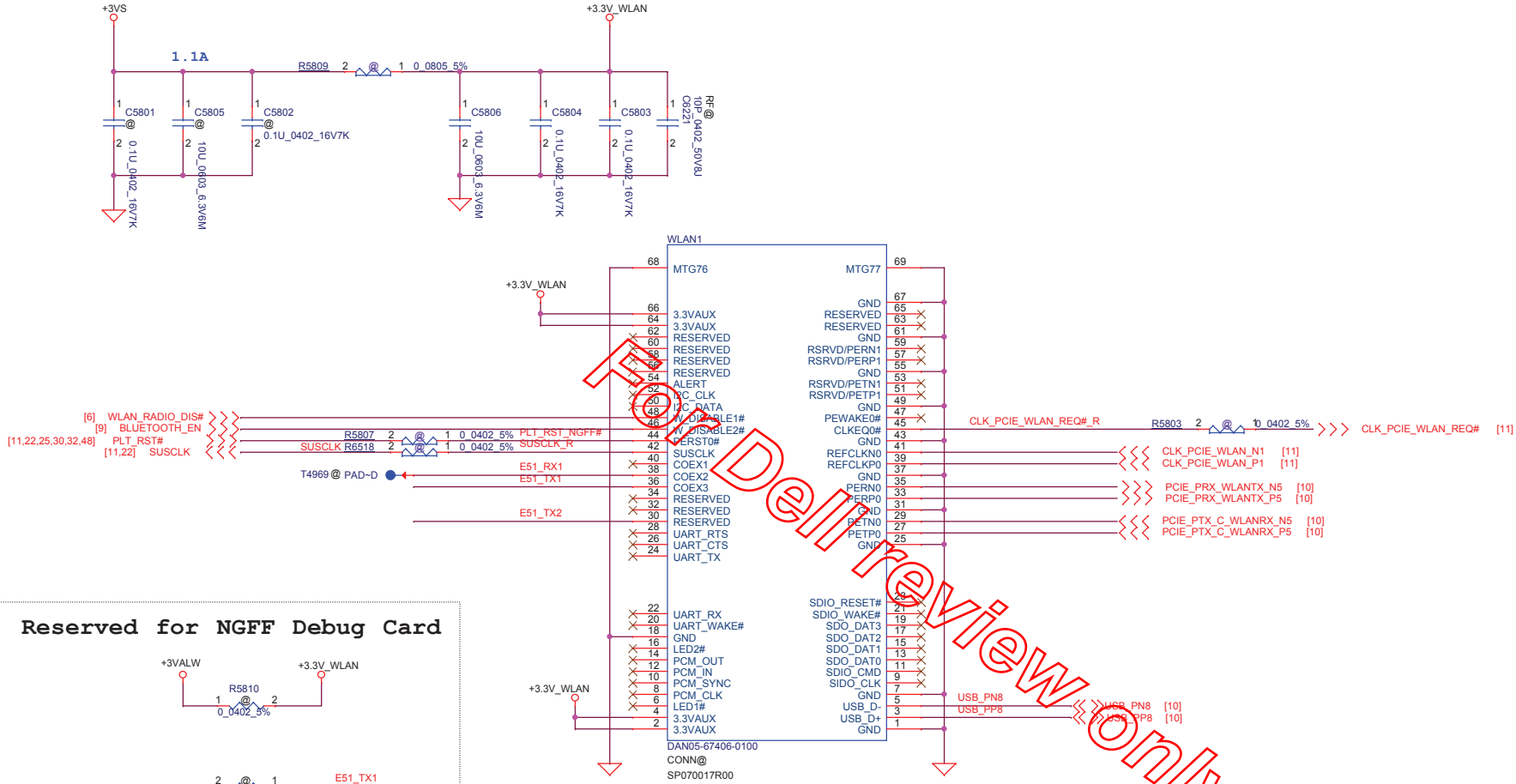
SSD
NGFF Slot_2 Key M



44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GNO	39
38	DEVSLP (O)	PETp1	37
36	N/C	PETn1	35
34	N/C		

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				Size	Document Number	Rev
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Main Func = WLAN

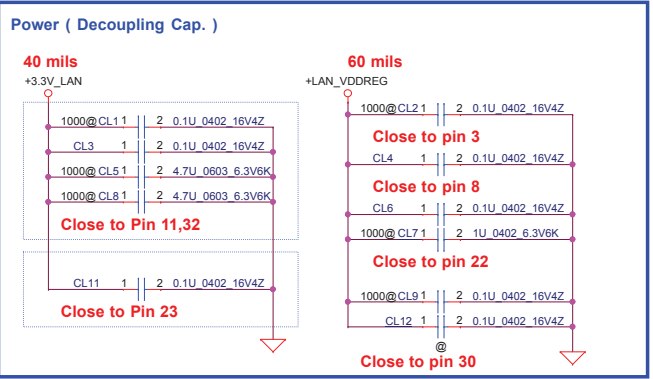
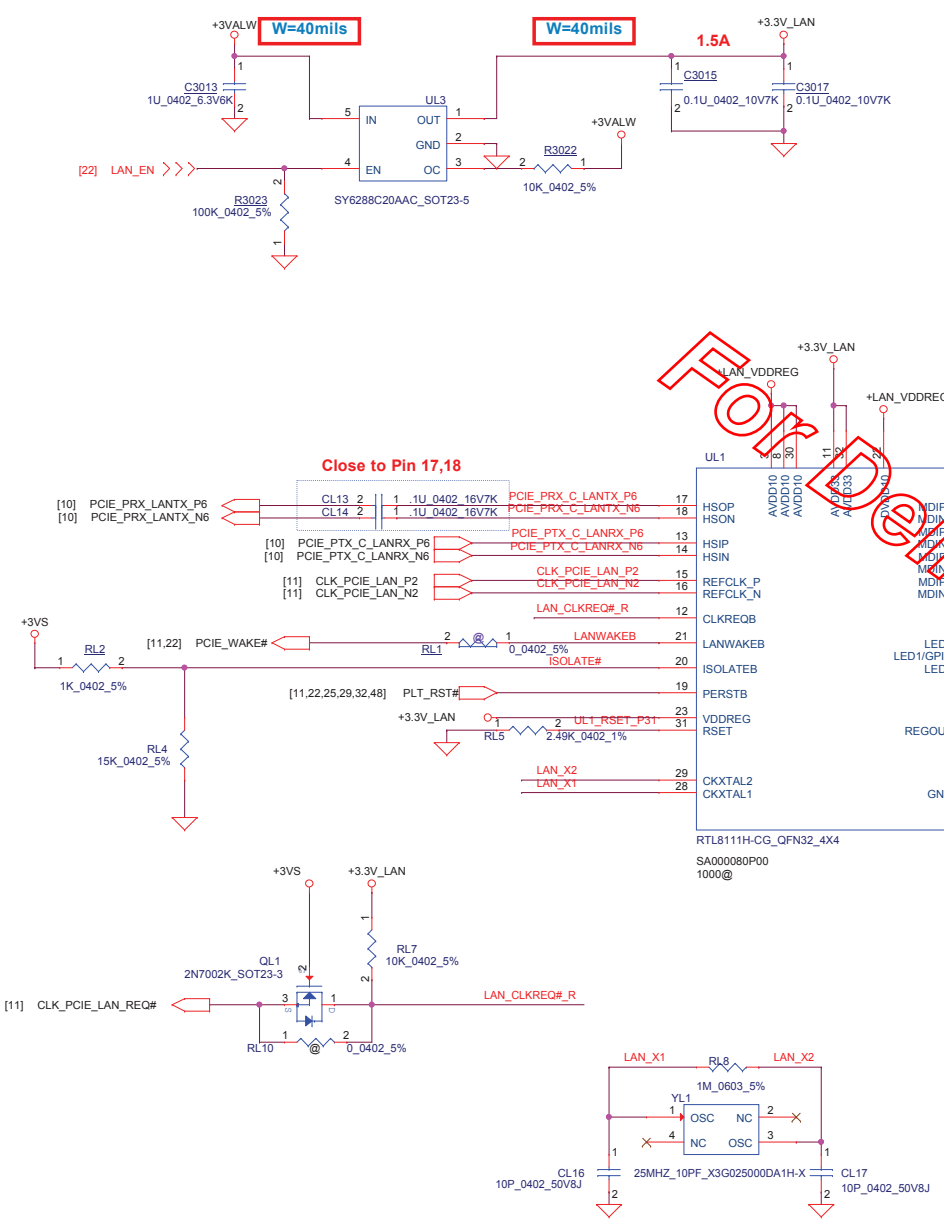


Support: Intel Dual Band Wireless-AC 3160

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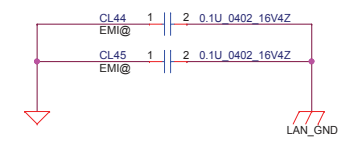
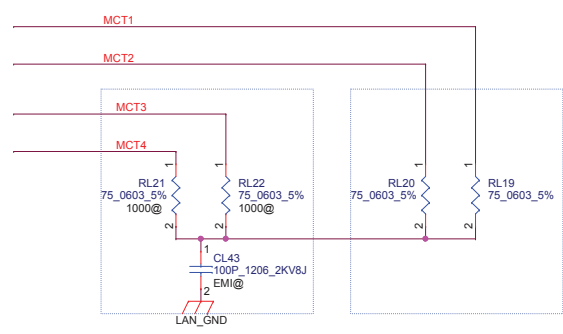
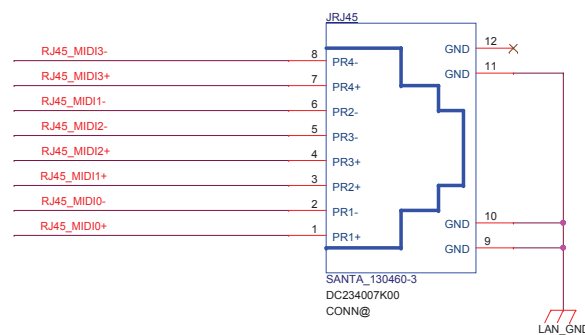
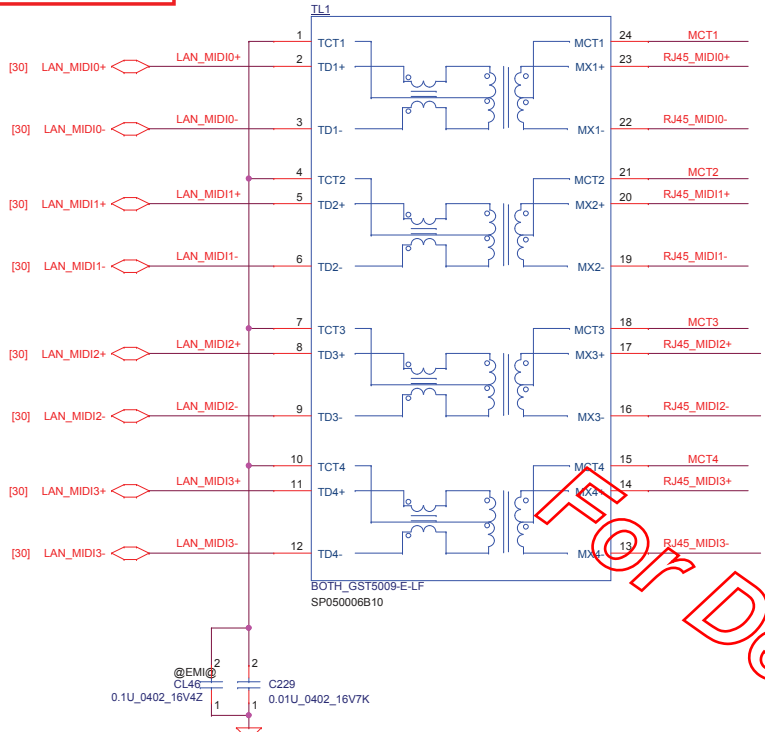
Main Func = LAN

+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.



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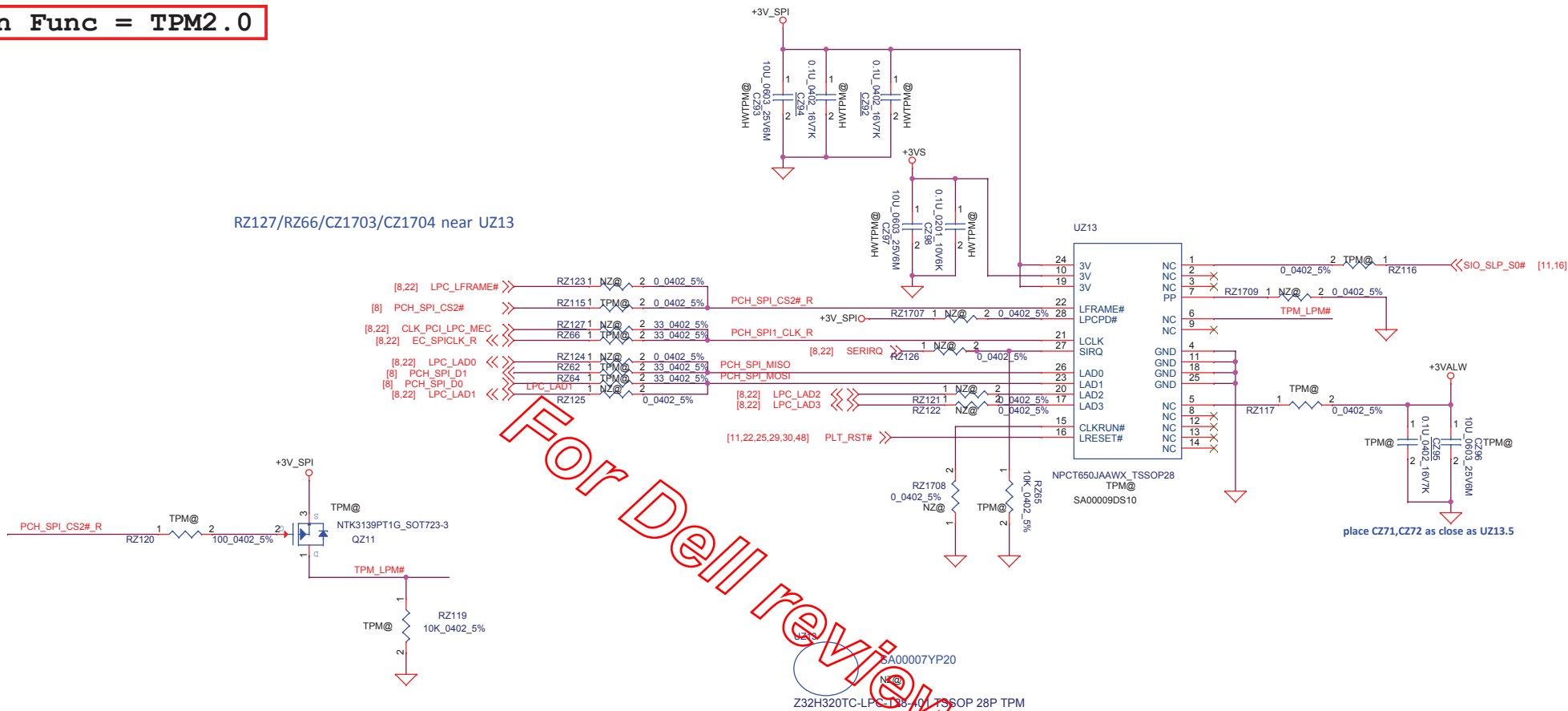
Main Func = LAN



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								JMB385 Media Card Controller			
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						Custom		LA-D821P		0.1	
				Date: Monday, June 06, 2016		Sheet 31		of 55			

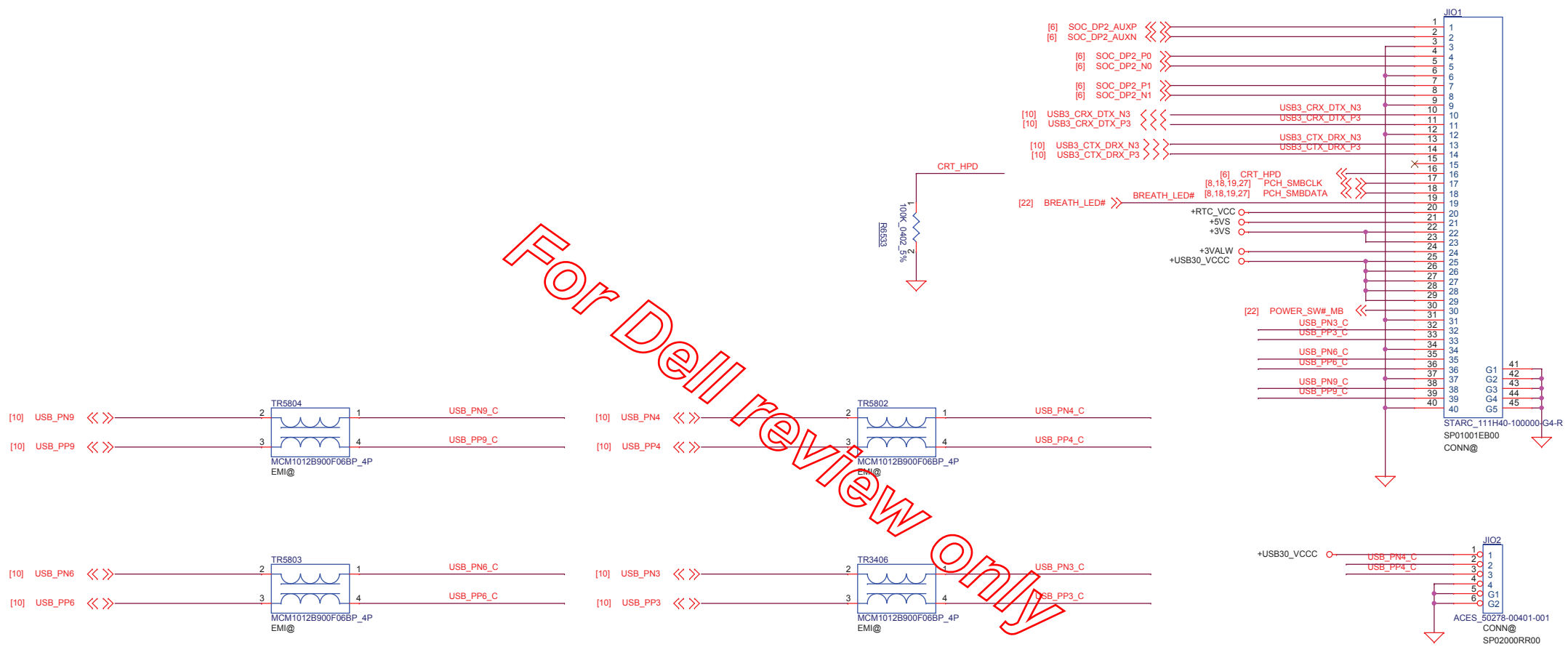
Main Func = TPM2.0



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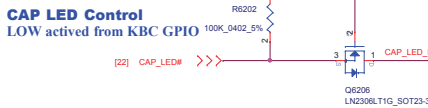
Main Func = IO Connector

I/O Board Connector



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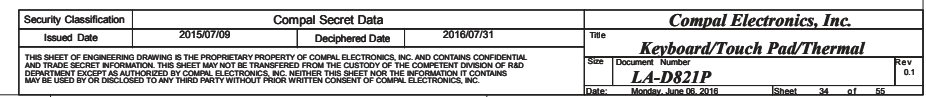
Main Func = KB



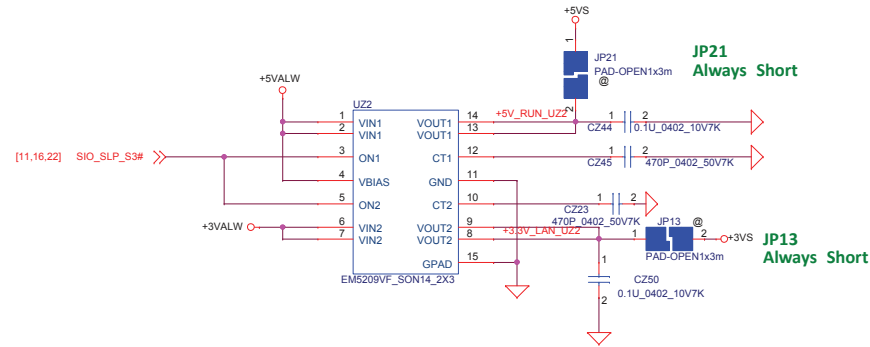
Main Func = Thermal



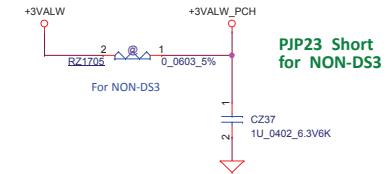
TEMPERATURE (°C)		T_CRTW				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	16.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	91	91	101	111	121
	14KΩ	83	93	103	113	123
	16.7KΩ	85	95	105	115	125



+5V_RUN/+3.3V_RUN for System



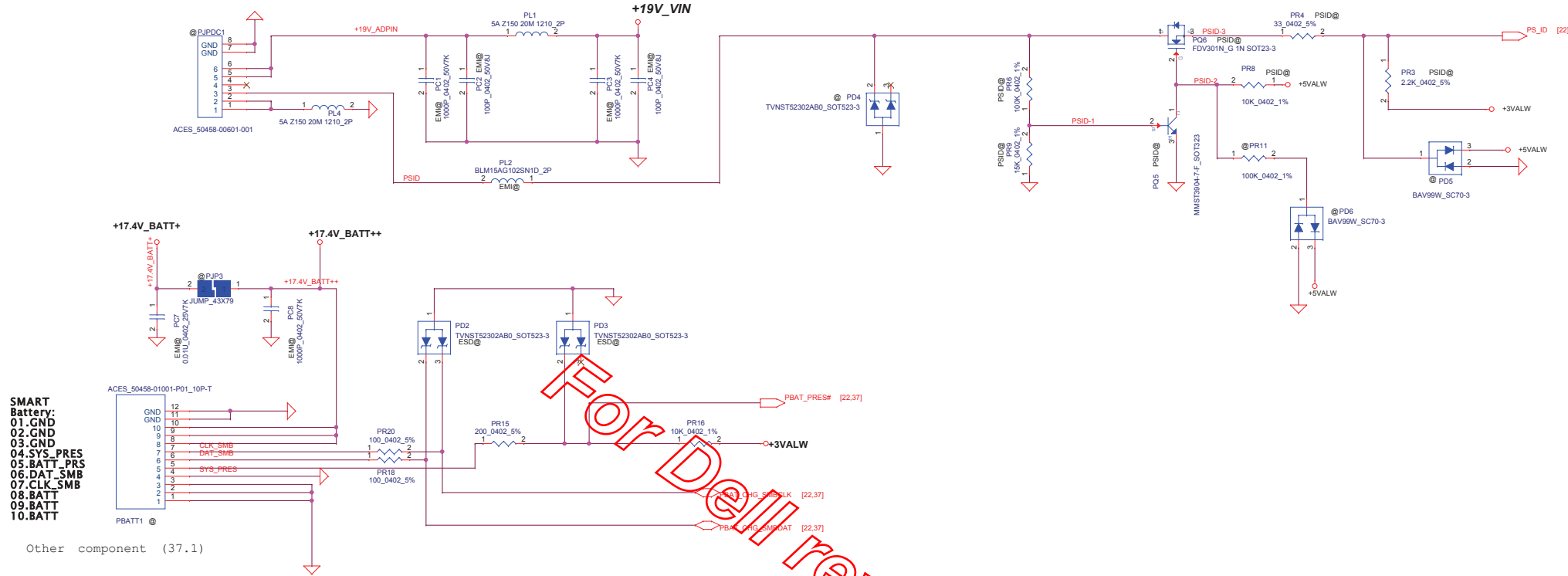
+3VALW_PCH for System



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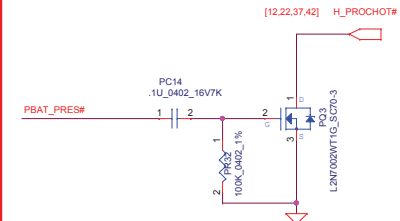
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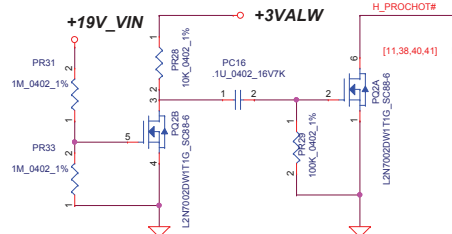
Adapter protection

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep @ in BOM since battery can not
be removed by end user

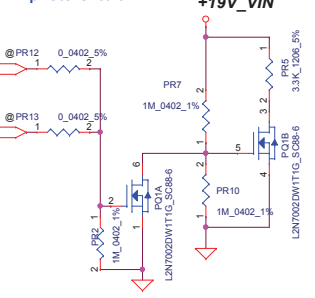


Battery protection

asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW_PROCHOT# is issued by EC



Erp lot6 Circuit



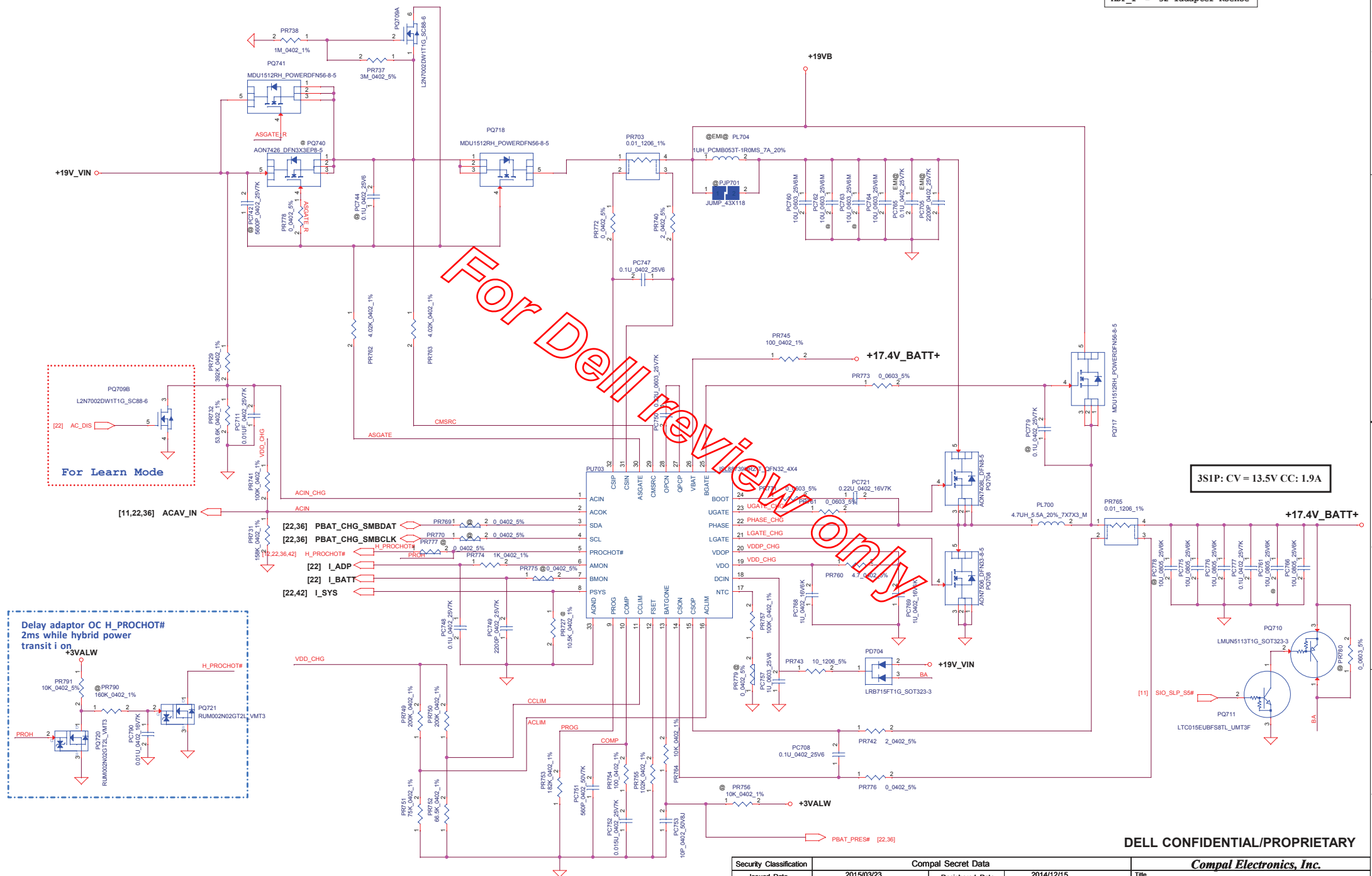
15W_U22+VGA(SKL)
X63:PSID@/U22_SKL@/VGA@
X4P:EMI@/ESD@/VGA@EMI@/RF@VGA@

15W_U22+VGA(KBL)
X63:PSID@/U22_KBL@/VGA@
X4P:EMI@/ESD@/VGA@EMI@/RF@VGA@

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Date:	Monday, June 06, 2016	Sheet	36 of 55	PWR DCIN/BATT CONN/OTP	

I_{ada}=0~2.30A (45W)

$$ADP_I = 32 \cdot I_{\text{adapter}} \cdot R_{\text{sense}}$$


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PWR CHARGER

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		Y010

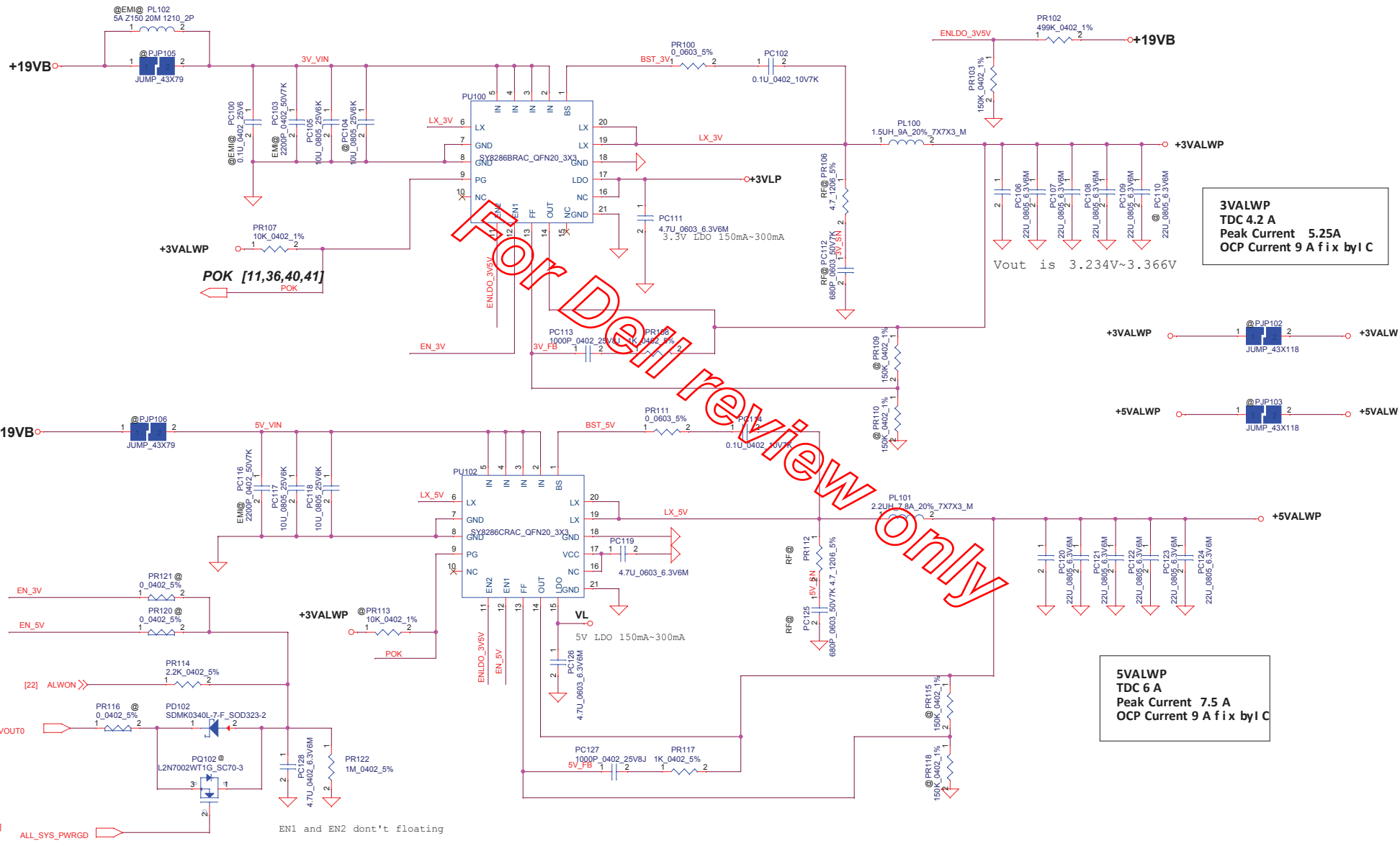
Date:	Monday, June 06, 2016	Sheet	37	of	55
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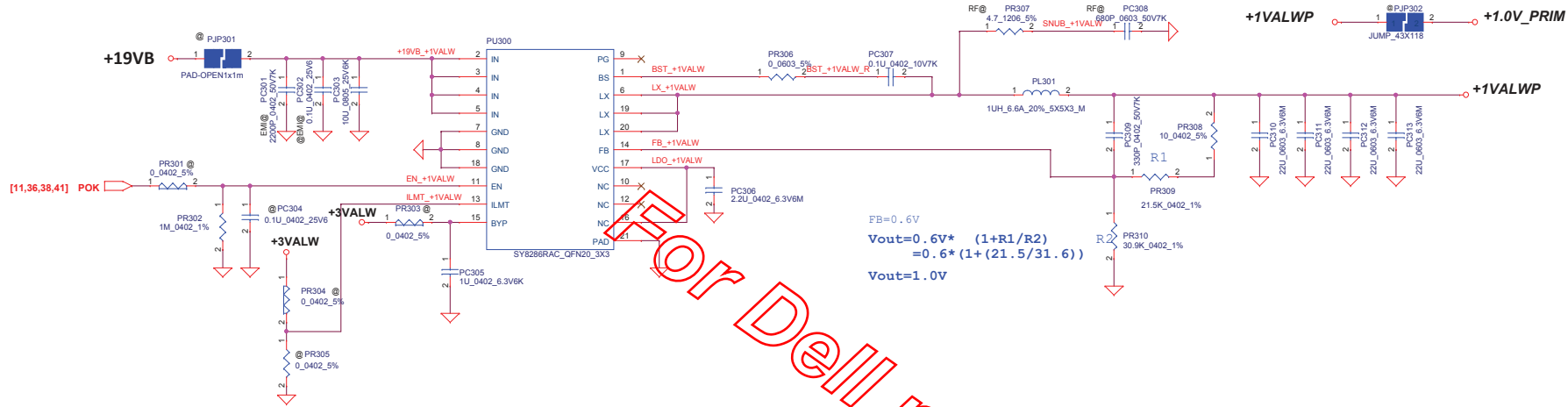


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Title			
PWR_3.3VALWP/5VALWP			
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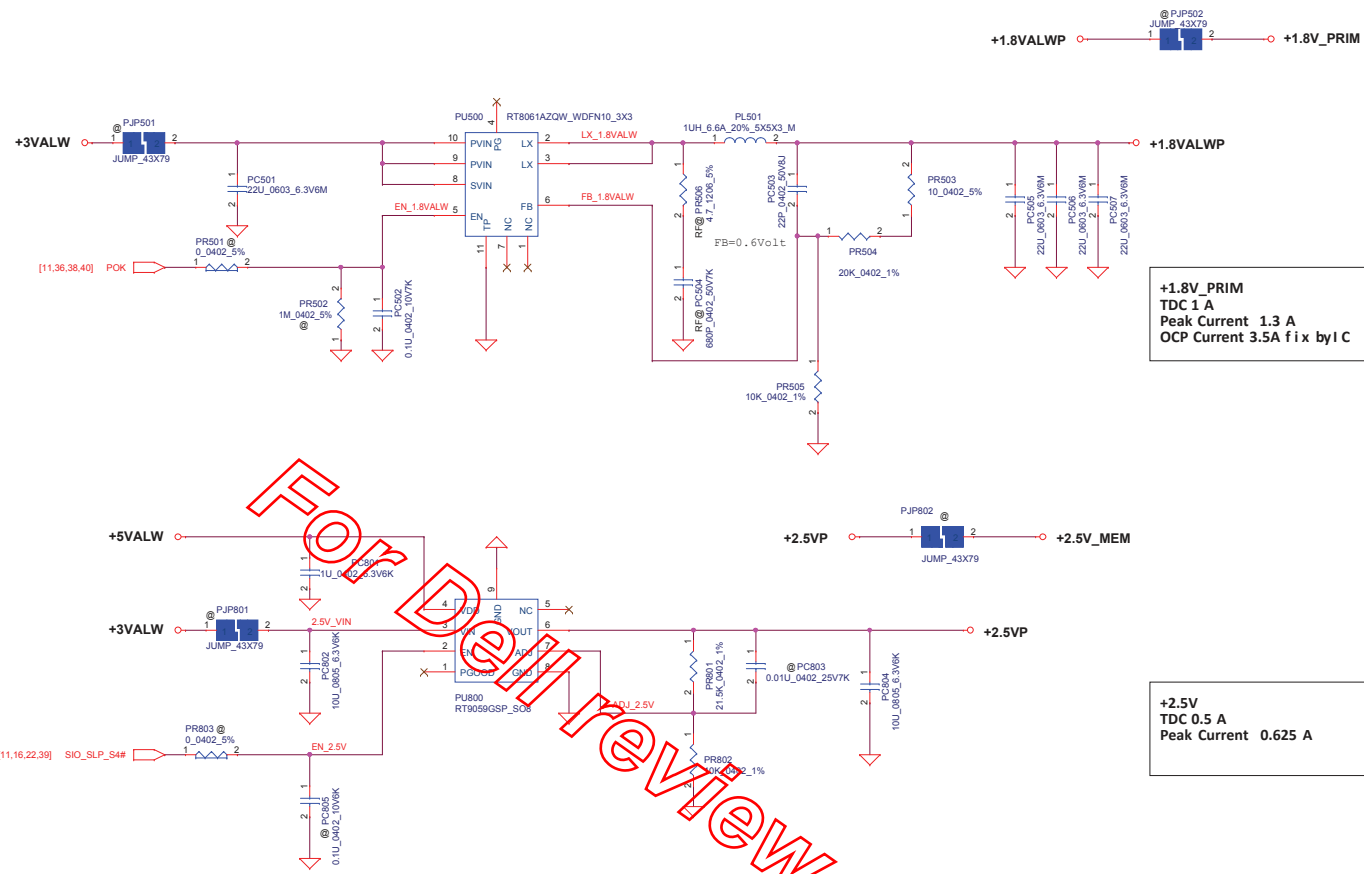
The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

OCP setting	ILMT(pin3)
6A	Pull low
9A	Floating
12A	Pull high

$FB = 0.6V$
 $V_{out} = 0.6V * (1 + R1/R2)$
 $= 0.6 * (1 + (21.5/31.6))$
 $V_{out} = 1.0V$

+1.0V_PRIM
 TDC 6 A
 Peak Current 8.6 A
 OCP Current 12 A Fix by IC
 TYP MAX
 Choke DCR 11.0mohm , 12.0mohm

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Local sense put on HW site

+1.0V_VCCST

VCC_SA
Loadline : 10.3m-ohm

TDC 5A
Peak Current 5A
OCP current 7A
Choke DCR 12 +-5% ohm

VCCSA_B+
PAD-OPEN1x1m
+19VB

VCCSA_B+

VCCSA_B+

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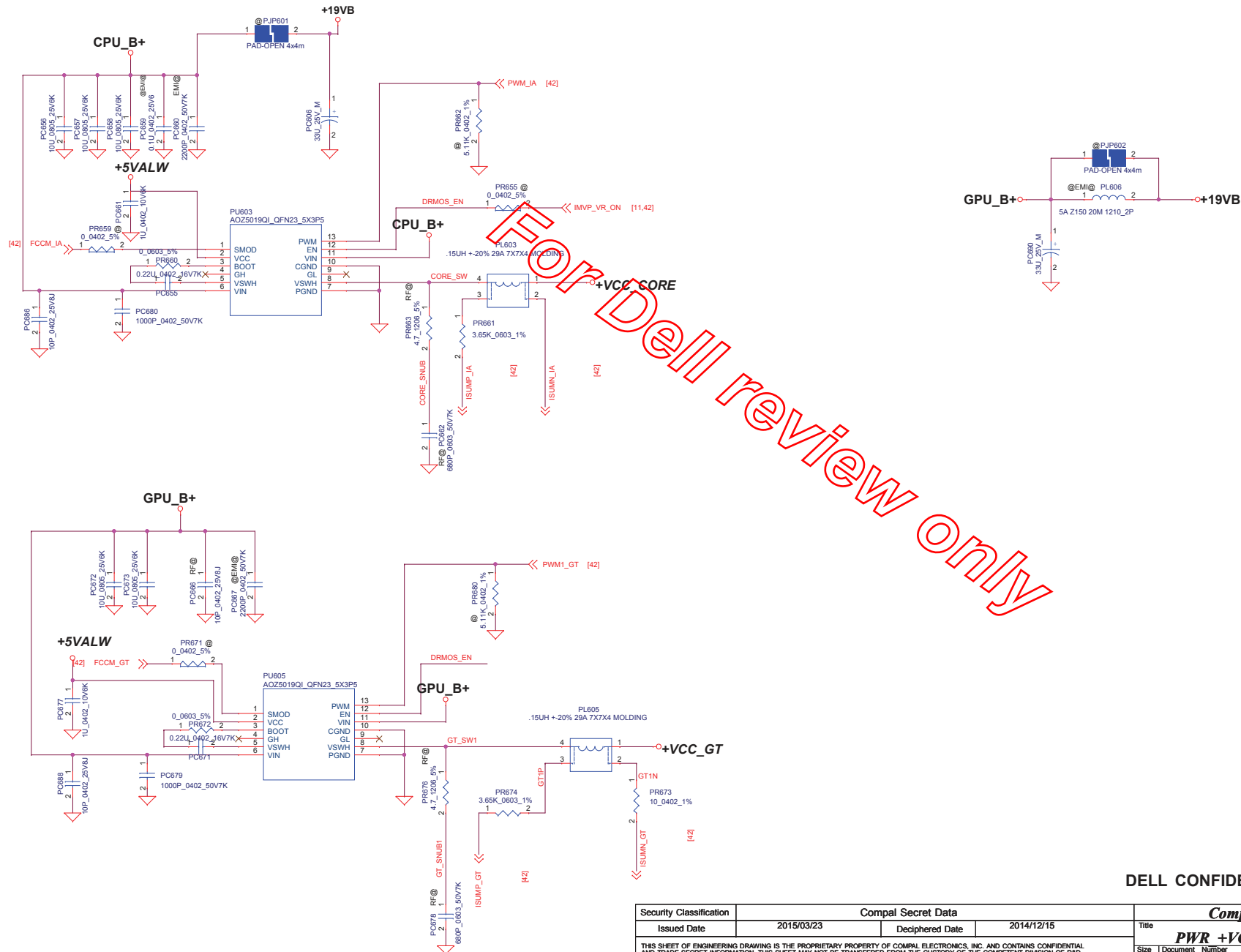
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VCC_core
U22 - 15W
Loadline : 2.4m-ohm

TDC 21A
Peak Current 29A
OCP current 34A
Choke DCR 0.66 +-7% ohm

VCC_GT
U22 - 15W
Loadline : 3.1m-ohm

U22-15W
TDC 18A
Peak Current 31A
OCP current 37A
Choke DCR 0.66 +-7% ohm



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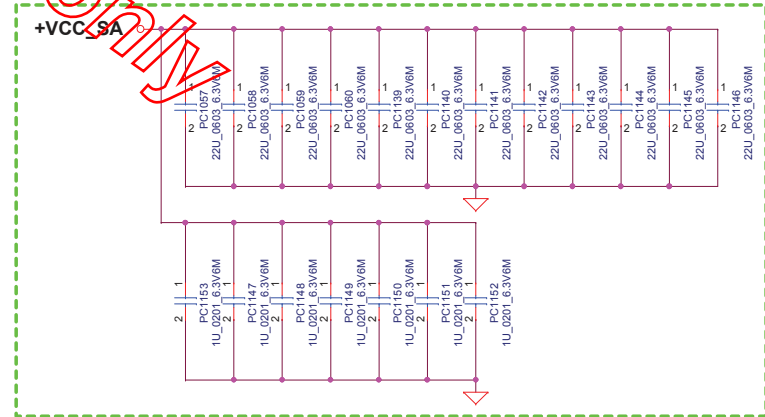
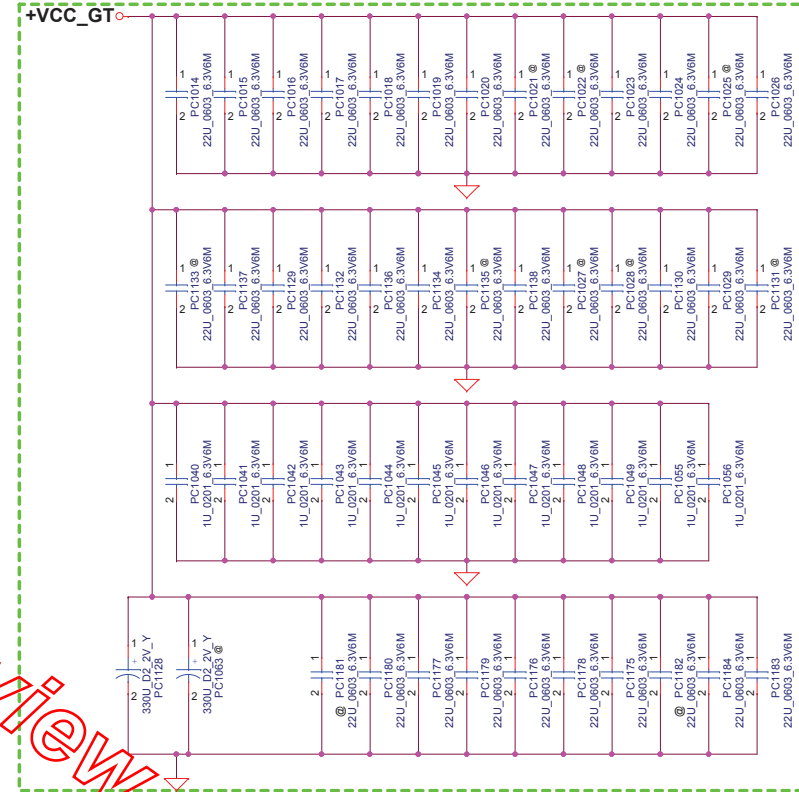
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VCC_CORE Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*35 pcs
Primary Side.
22U_0603 * 20 pcs+220u_D2*2 pcs



VCC_SA Place on CPU
Back Side.
22U_0603 * 4 pcs + 1U_0201*7 pcs
Primary Side.
22U_0603 * 8 pcs

VCC_GT Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 13 pcs +330u_D2*1 pcs



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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P37	PWR	20160303	COMPAL	to change charger IC	change charger IC(PU703) to ISL88739	0.2 (X00)
2	P39 P43 P45 P46	PWR	20160303	COMPAL	to prevent RF issue	add PC208 add PC666,PR676,PC678 add PC1116,PR1122,PC1109, add PC1402,PR1408,PC1408	
3	P42	PWR	20160303	COMPAL	to adjust +VCC_CORE and +VCC_GT load line	change PR622 to 1.91K,PR638 to 287 ohm,PC626 to 0.1uF,PC642 to 0.1uF	
4	P36,P42	PWR	20160303	COMPAL	to save layout space	delete PL3,PL602(reserve location)	
5	P36	PWR	20160303	COMPAL	to fix battery connector ME issue	to change battery connector	
6	P37	PWR	20160304	COMPAL	to fix Temp/Voltage 19.5V DC-IN issue	change PR732 to 53.6K	
7	P44	PWR	20160304	COMPAL	to fix DFB solder open problem	change PC1127,PC1062,PC1128 footprint	
8	P38	PWR	20160308	COMPAL	to prevent OTF functions abnormal issue	to reserve PQ102 and connect to ALL_SYS_PWRGD	
9	P37	PWR	20160316	COMPAL	to save layout space by EMI request	change PC760,PC762,PC763,PC764 to 0603 size and delete PR766,PC767	
10	P43	PWR	20160328	COMPAL	according to test result to adjust VCC_CORE and GT_CORE's load line	to unmount PC624 and PC646	
11	P44	PWR	20160328	COMPAL	according to test result to adjust VCC_CORE and GT_CORE's output MLCC's location(only change BOM) and bulk cap	unmount:PC1021,PC1135,PC1133,PC1131,PC1022,PC1025,PC1027,PC1028,PC1063, PC1008,PC1003,PC1011,PC1072,PC1076,PC1071,PC1081,PC1082,PC1004,PC1007,PC1012 to mount:PC1176,PC1175,PC1177,PC1179,PC1178,PC1180,PC1183,PC1184,PC1170,PC1173,PC1174 to change PC1127,PC1062 to 220uF/9m ohm	0.3 (X02)
12	P36	PWR	20160429	COMPAL	To improve EMI and reduce inrush current to mount n filter's bead and change cap	unmount:PL1,PL4 change PC2,PC4 to 100pF	
13	P37	PWR	20160429	COMPAL	ISL88739 doesn't support PSYS function	unmount:PR727 change PR774 to 1K ohm change PC748 0.1uF	
14	P39	PWR	20160429	COMPAL	to adjust 1.2V OCP to 10.2A	change PR205 to 11K	
15	P37	PWR	20160429	COMPAL	to avoid inrush to damage MOS	to reserve PQ741	

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Main Func : dGPU

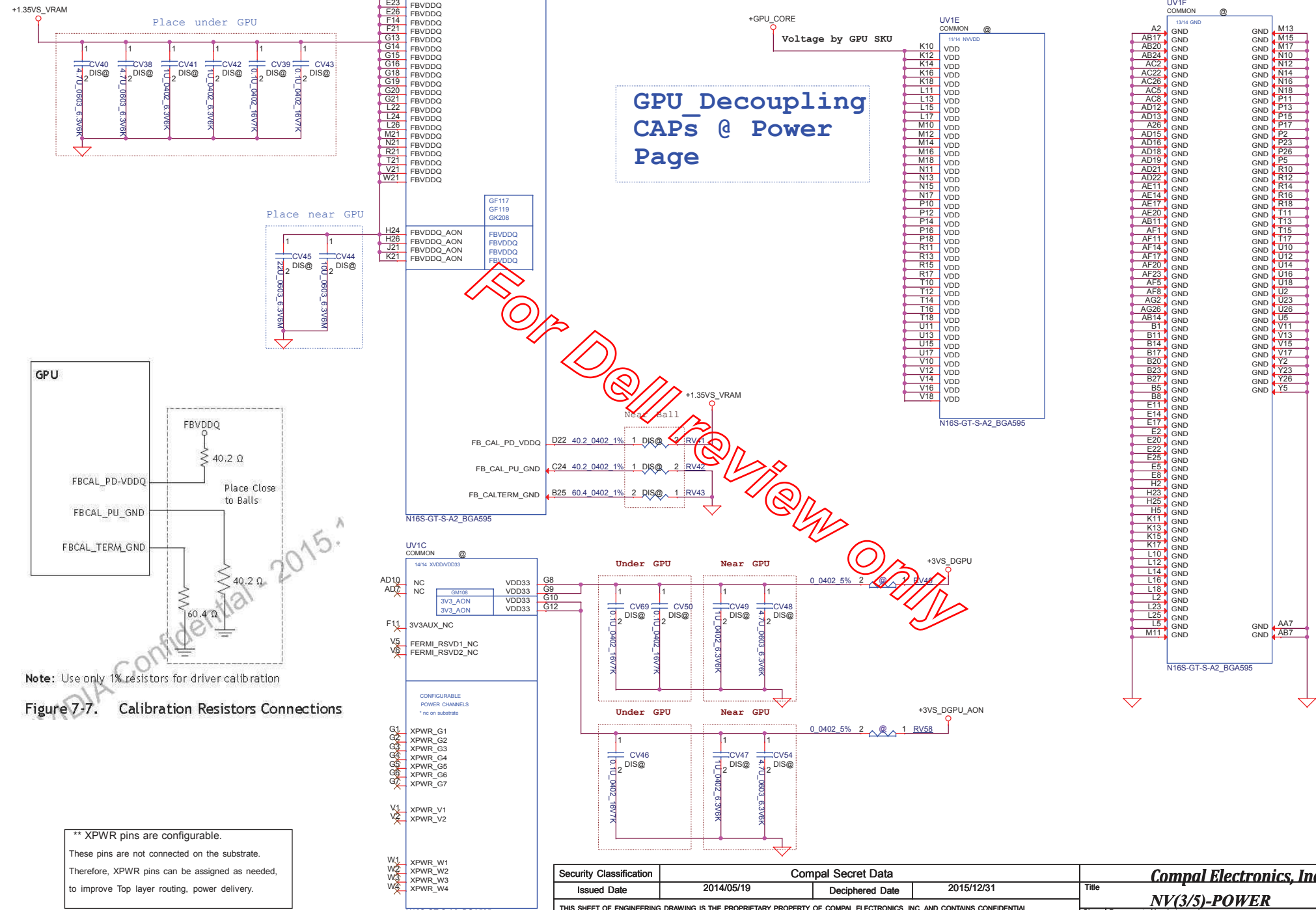
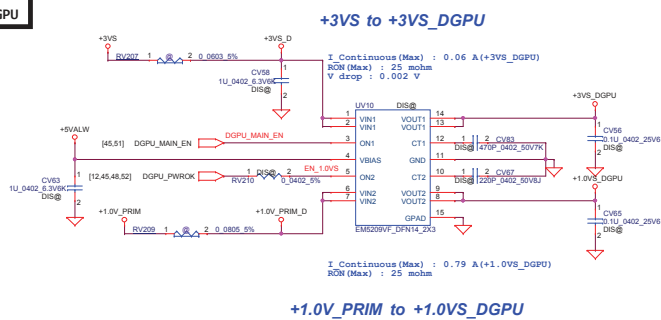
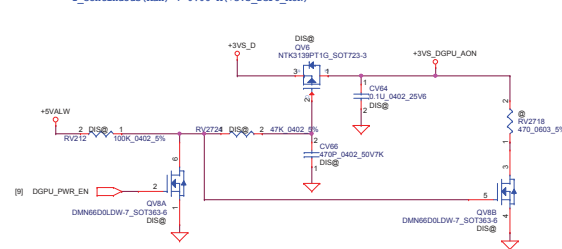


Figure 7-7. Calibration Resistors Connections

** XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.

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Size	Document	Number	Rev	LA-C071P	
Custom			0.2		
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**+3VS to +3VS_DGPU_AON**Table 5. EDP-Continuous³

Products	VRAM Type	GPU Core	GPU FBIO	FB Total ^{1,5}		1.05V Total ²		3.3V Total
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N165-GWR	GDDR5	19.0	—	2.0	—	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N165-GTR	GDDR5	26.5	—	2.0	—	4.7	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

Table 3-8. Power Rail Specification for GDDR5 Frame Buffer Interface

Constraint Parameter	Requirement
FBVDD/FBVDDQ	1.35, 1.50V, or 1.50 V memory with DVS ¹ support at 1.35V
FBVDDQ/FBVDDQ switching time	< 68 μs
DC Tolerance	± 3%
AC Tolerance	Transient noise tolerance: 80 mV pk-pk within 20 MHz BW High frequency noise tolerance: 200 mV pk-pk within 1 GHz BW
GPU FBVREF ²	Internal VREF
Memory FBVREF	0.7 × FBVDDQ when termination is enabled 0.5 × FBVDDQ when termination is disabled

Note:
¹ DVS = Dynamic Voltage Switching.
² Since the GPU Internal VREF is used, the FBVREF pin on the GPU can be left unconnected.

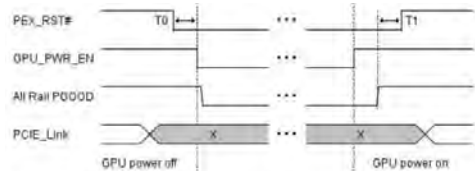


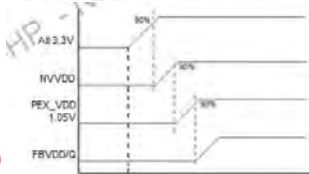
Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# deassertion	0.1	5	ms

Chapter 3

- Added 1.0V support to PEX_VDD and all 1.05V Power Rails



Notes: All 3.3V includes all rails powered at 3.3V
 PEX_VDD 1.05V includes all rails that are shared

Figure 3-7. Example of Power-Up Sequencing Order

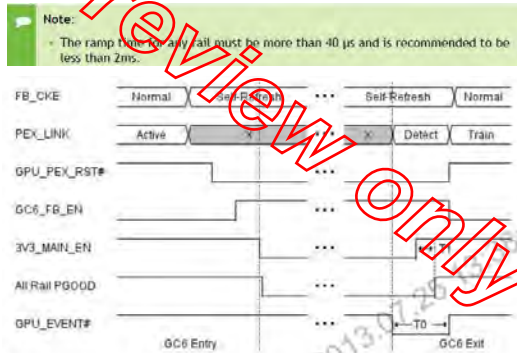
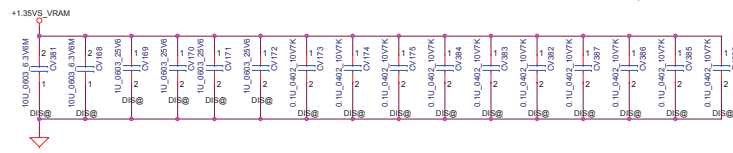


Figure 18-15. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-3. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	H/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

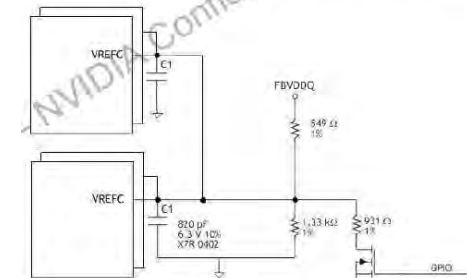
$$MF=0$$


Component	Value
R1	80 Ω , 1%, 0402

Configuration	Requirement	Notes
*32	Share one Vref-C circuit for two memory parts.	GD54R DRAMs have internal VREF for DQ, ODI, EDC (VREF-D).
*16	Share one VREF-C circuit for four memory parts.	Command, Address VREF (VREF-C) needs to be externally supplied since DRAMs do NOT internally generate VREF for those needs.

VREF-D pins can be left floating.

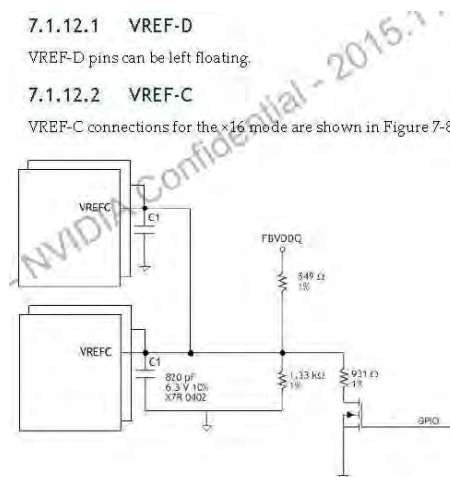
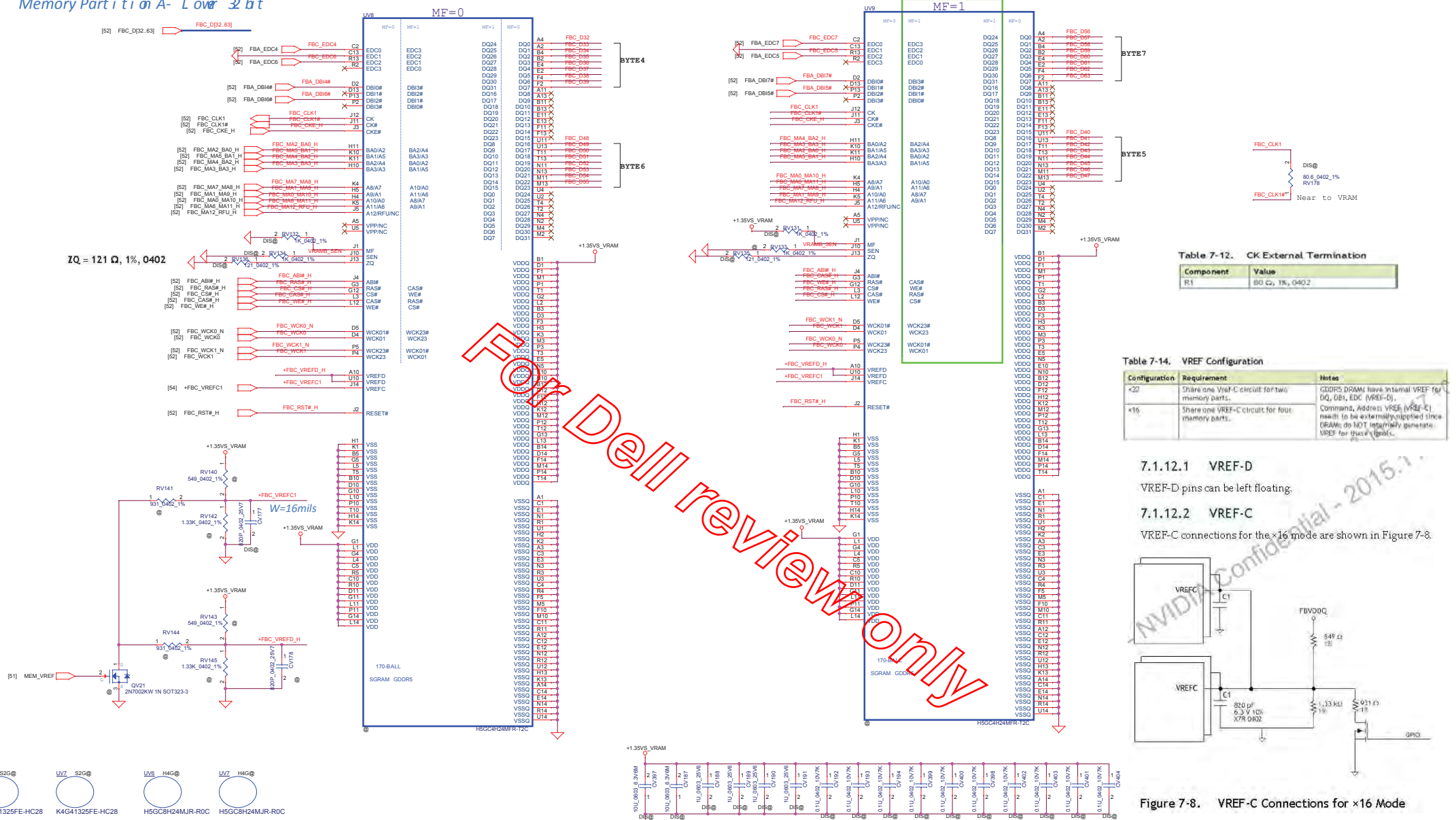
VREF-C connections for the $\times 16$ mode are shown in Figure 7-8.

Figure 7-8. VREF-C Connections for $\times 16$ Mode

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Memory Partition A- Low 3 bit



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