

DM4/RB4 Intel Huron River Platform with UMA

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT

POWER

AC/BATT CONNECTOR
PG 41

SYSTEM RESET CIRCUIT
PG 7

BATT CHARGER
PG 41

RUN POWER SW
3VSUS, 5VSUS, 3V_S5, 5V_S5
+3V, +5V
PG 42

POWER

REGULATOR
+1.05V
PG 39

REGULATOR
1.5VSUS, 0.75VSMDRR_VTERM, SMDRR_VREF
PG 36

REGULATOR
+1.8V, +0.85V
PG 39,38

CPU Core
VCC_CORE
PG 35

DC/DC
3.3PCU, 5VPCU, 15VPCU
PG 40

VGA Core
UMA
PG 35

FAN / THERMAL
G990P11U
PG 30

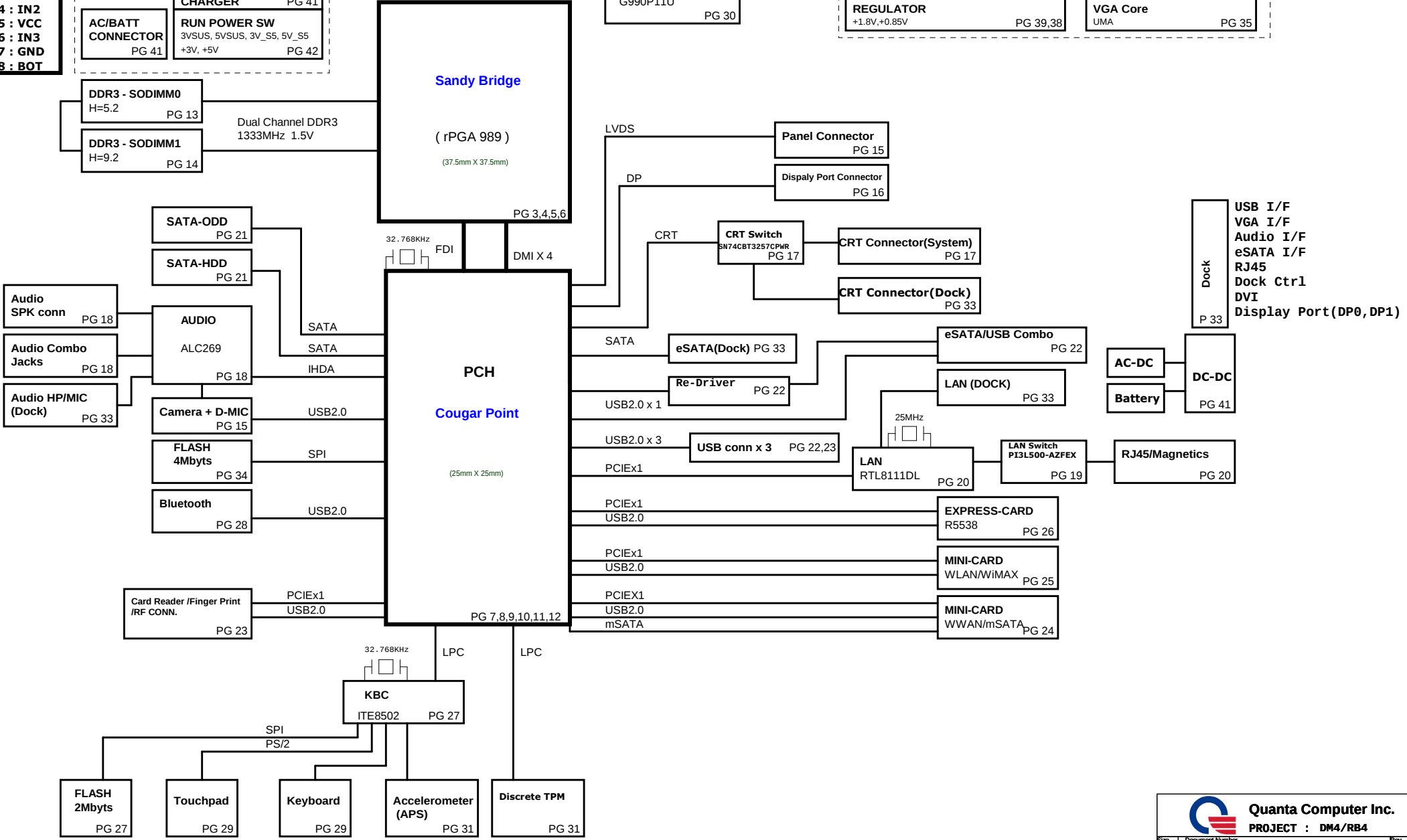


Table of Contents

PAGE	DESCRIPTION
01	LOCK DIAGRAM(UMA)
02	FRONT PAGE
03-06	Sandy Bridge
07-12	Cougar Point-PCH
13-14	DDRIII SO-DIMM
15	LCD CONN
16	Display Port
17	CRT CONN
18	AUDIO CODEC(ALC269Q)
19	LAN SW
20	LAN(8111DL-VB
21	SATA HDD/CD-ROM
22	USB X1/USB+ESATA
23	USB X2/SIM_CARD/LEDs/RF
24	MINI-Card (WWAN/SSD)
25	MINI-Card (WLAN/Wimax)
26	Express Card
27	KBC IT8518/19
28	B/T
29	K/B, T/P
30	FAN & THERMAL
31	G-SENSOR/TPM
32	Daughter Boards
33	Docking CON
34	iTPM & RFID EEPROM
35	+VCC_CORE(ISL95831)
36	+1.5V_SUS/VTT (UPI6163)
37	Blank
38	+VCCSA
39	+1.05V (OZ8115)
40	SYSTEM 5V/3V
41	CHARGER (ISL88731)
42	Discharg
43	Power Block Diagram
44	XDP
45	Schematic Value Descript
46	GC9E HOLE & SCREW
47	BOM Matrix Table

Power States

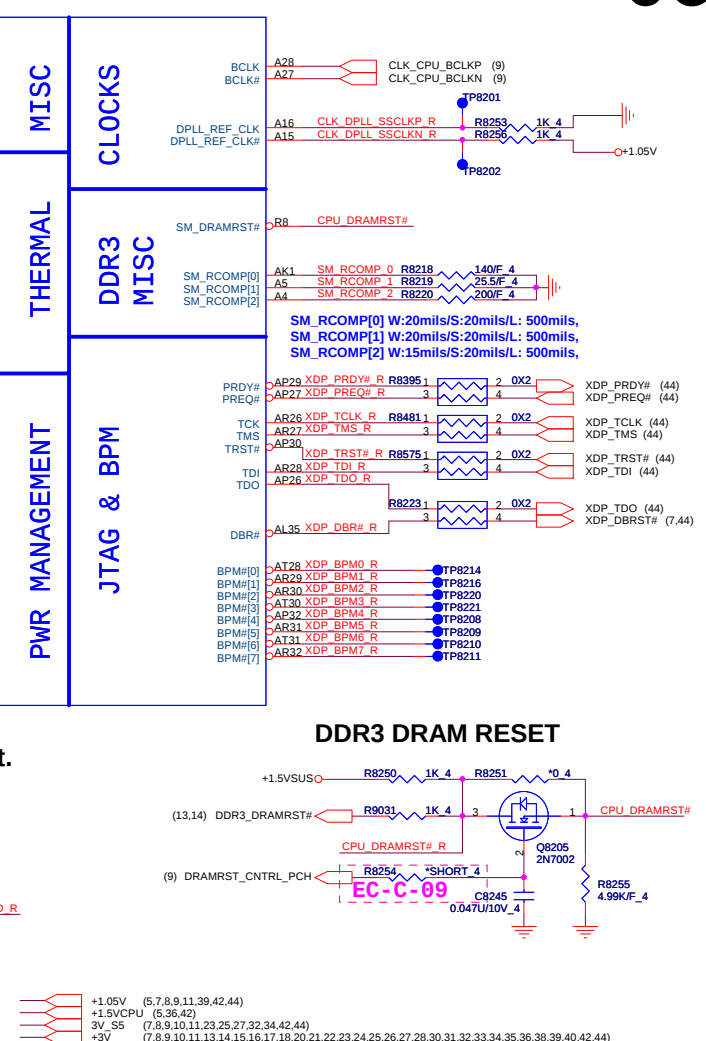
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	15,35,36,38,39,40,41,42	MAIN POWER		S0~S5
+3V_RTC	+3.0V~+3.3V	7,8,11,27	RTC		S0~S5
3VPCU	+3.3V	8,13,14,15,20,27,32,33,39,40,41,42,44	IT8518/19 POWER	3V5V_EN	S0~S5
5VPCU	+5V	13,21,27,36,38,39,40,41,42	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	15,31,36,40,42	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	19,20,33,42	LAN POWER	LAN_ON	
5V_S5	+5V	11,22,23,42	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	3,7,8,9,10,11,22,23,25,27,34,42	Sys Management,PCH Resume Well, USB,WLAN,WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	15,35,42	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	23,26,27,42	SLP_S4# CTRLD POWER	SUSON	S0~S3
+1.5VSUS	+1.5V	3,11,13,14,36,42	DDR3 SODIMM POWER	SUSON	S0~S3
0.75VSMDDR_VTERM	+0.75V	13,14,36,42	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	7,8,11,16,17,18,21,27,29,30,42	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	7,8,9,10,11,13,14,15,16,17,18,20,21,22,23,24 25,26,27,28,30,31,32,33,34,35,36,38,39,40 42,44	SLP_S3# CTRLD POWER	MAINON	S0
+VCC_GFX		5,35,42	VGA CORE POWER	MAINON	S0
+VCCSA	+0.8V~+0.9V	5,38,42	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5,8,11,39,42	LVDS,NVM POWER	MAINON	S0
+1.05V	+1.05V	3,5,7,8,9,11,39,42	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
+VCC_CORE		5,35,42	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	15	LCD Power	ENVDD	S0
+5V_ODD	+5V	21	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	21	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	41	MAIN BATTERY	CHG_PBATT	S0~S5
+1.5VCPU	+1.5V	3,5,36,42	DDR3 1.5V Rails	PS_S3CNTRL	S0



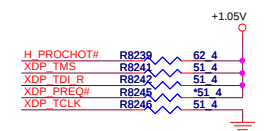
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PROJECT : DM4/RB4

Size	Document Number	Rev 1A
System Block Diagram		
Date: Friday, December 24, 2010	Sheet 2 of 53	



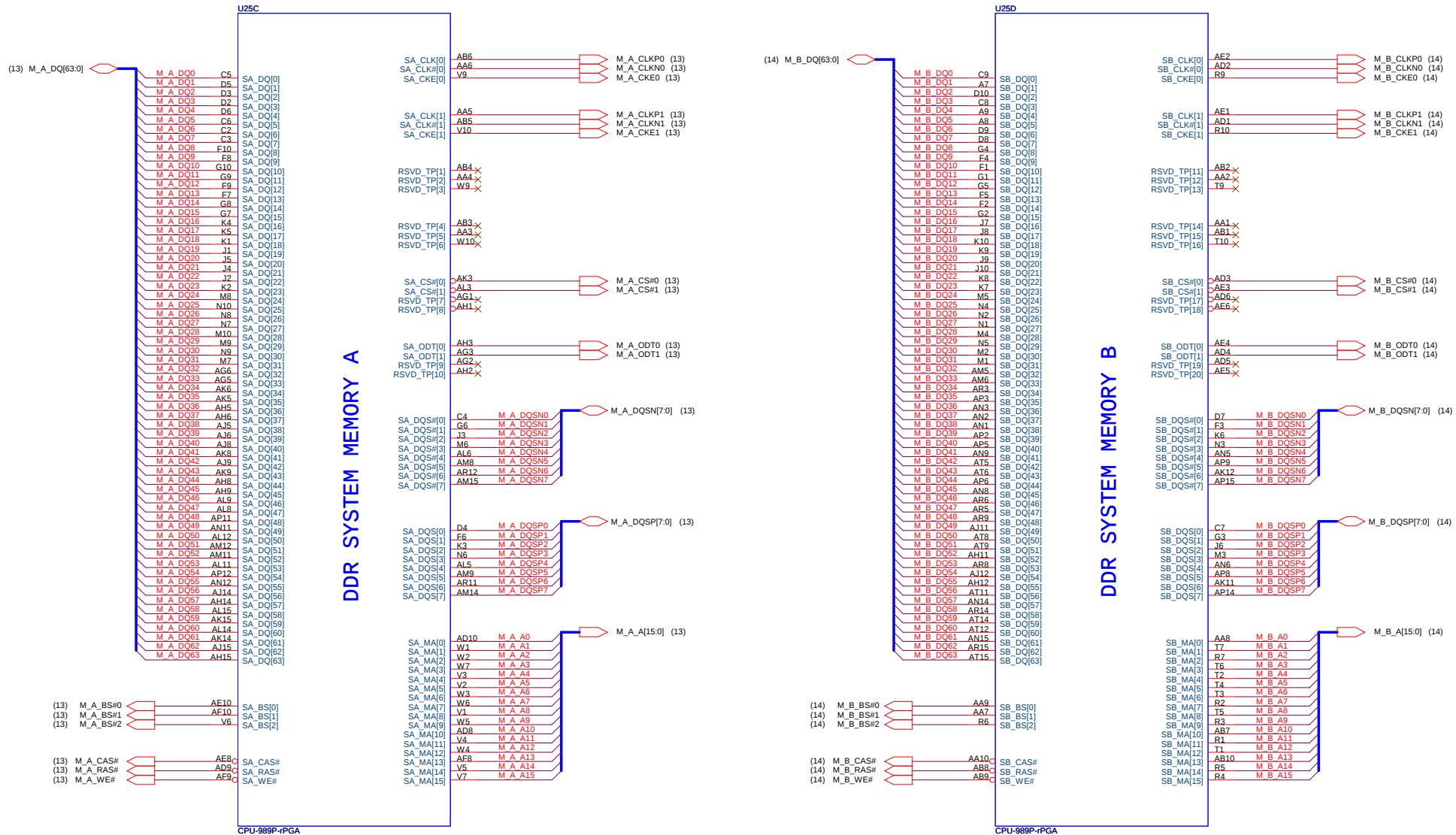
Processor pull-up (CPU)



 **Quanta Computer Inc.**
PROJECT : DM4/RB4

Size	Document Number	Rev
	SNB 1/4 (PCIE&DMI&FDI)	1A
Date:	Friday, December 24, 2010	Sheet 3 of 53

Sandy Bridge Processor (DDR3)



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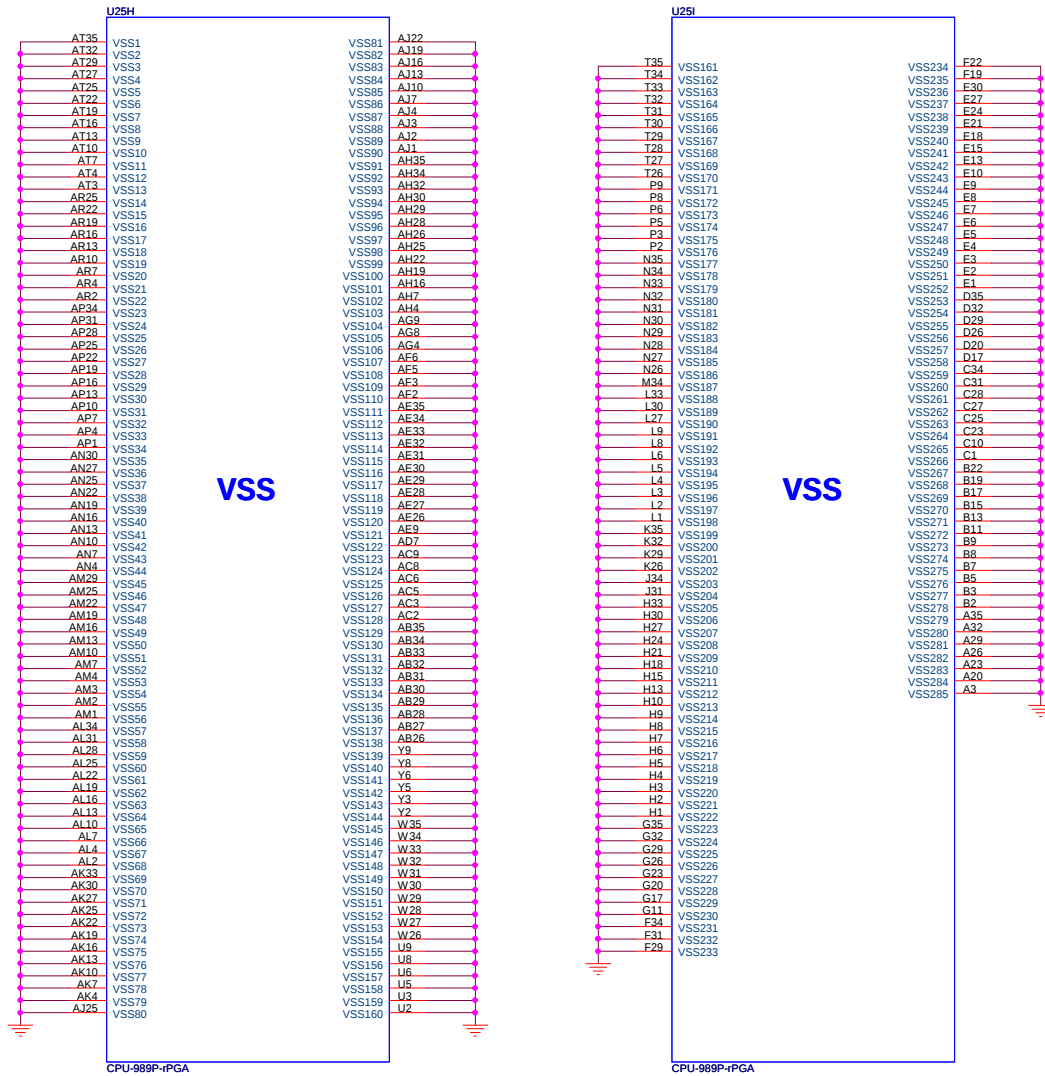
PROJECT : DM4/RB4

Size	Document Number	Rev
	SNB 214 (DDR3 I/F)	1A

Date: Friday, December 24, 2010 1 Sheet 4 of 53

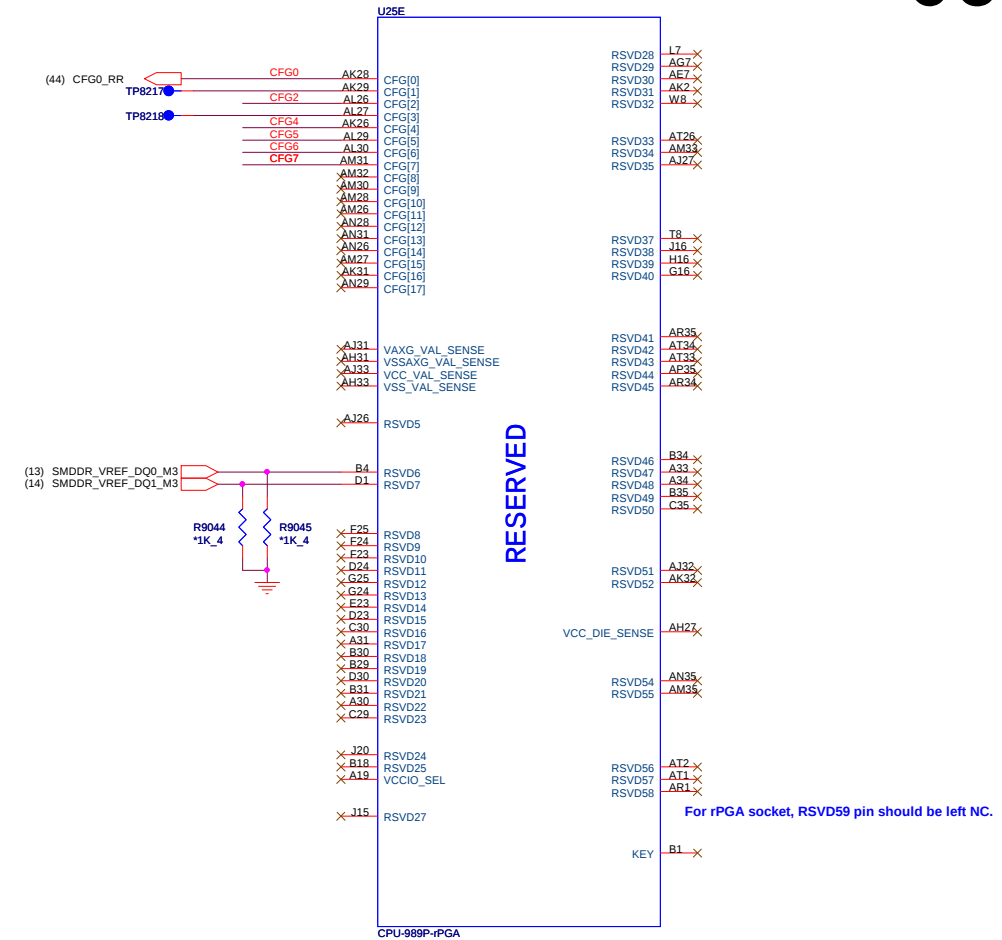


Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

06



Processor Strapping

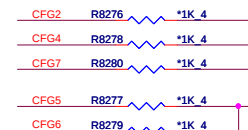
The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed (Default)
CFG4 (DP Presence Strap)	(Default) Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	(Default) PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

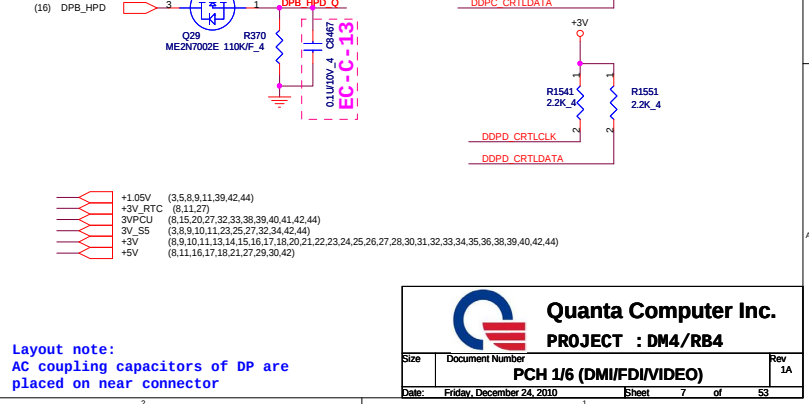
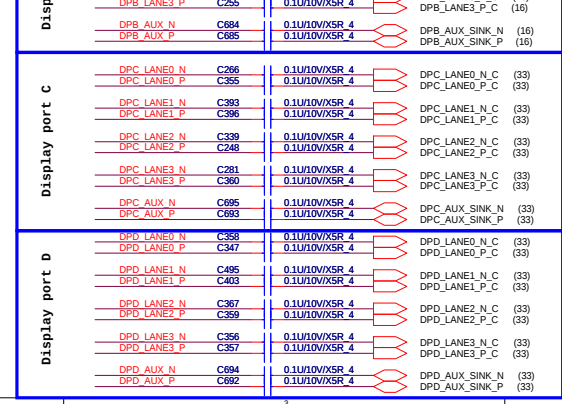
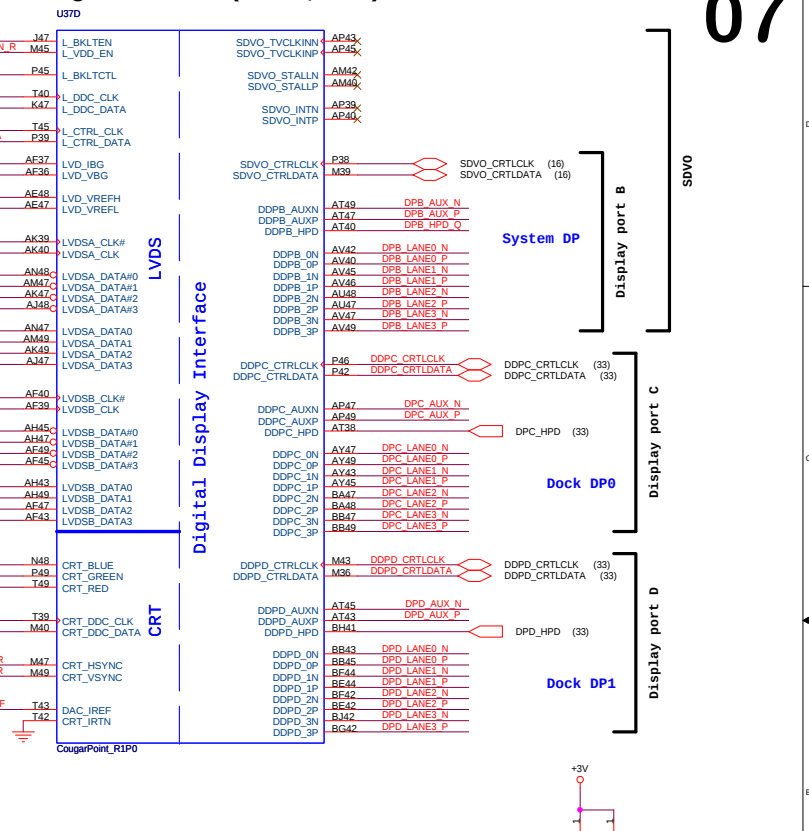
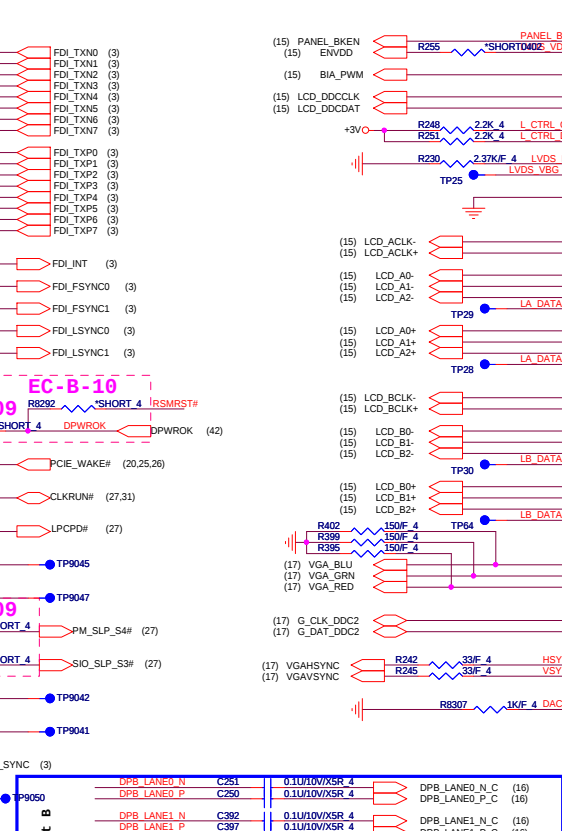
11(Default)

CFG[6:5] (PCIe Port Bifurcation Straps)

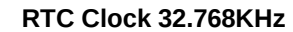
11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



07



08



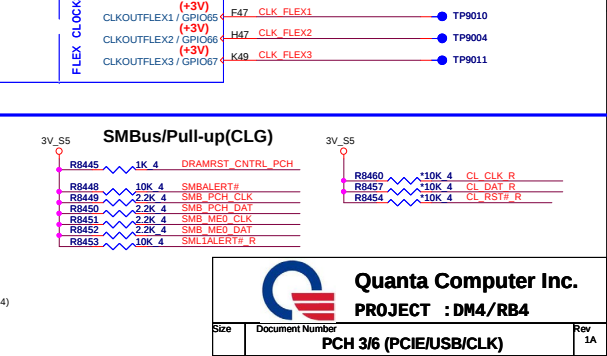
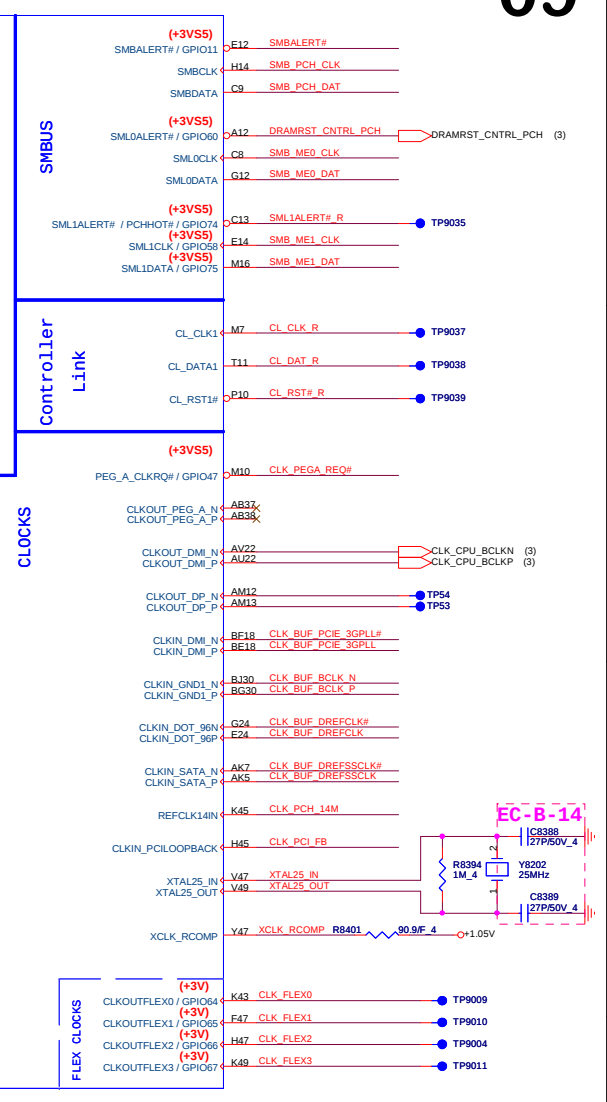
RTC BATTERY

HDA Bus(CLG)

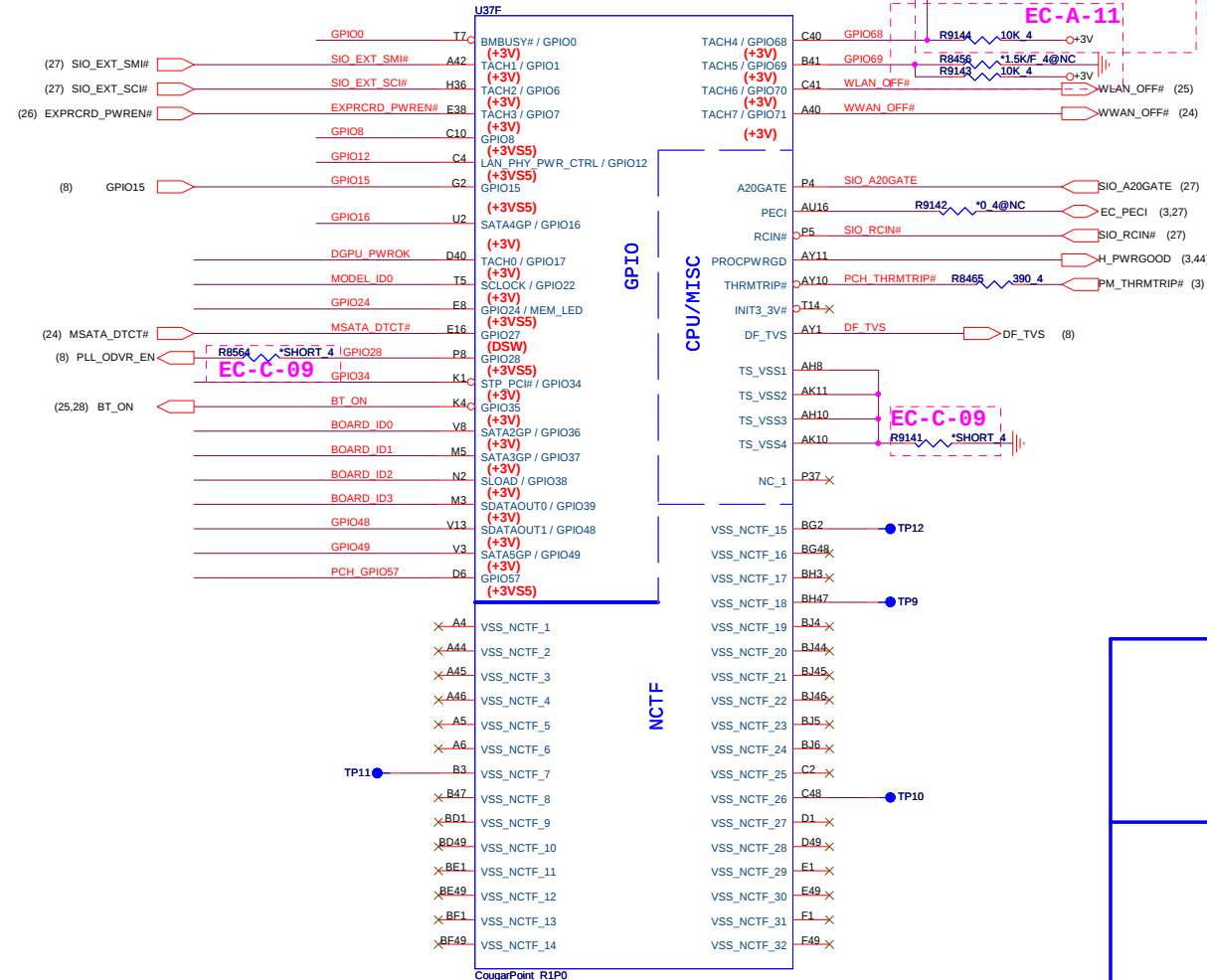


 Quanta Computer Inc. PROJECT : DM4/RB4			
Size	Document Number		Rev
	PCH 2/6 (SATA/HDA/SPI)		1A
Date:	Friday, December 24, 2010	Sheet	8 of 53

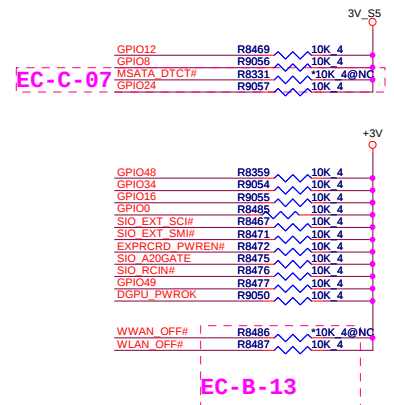
09



Cougar Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down(CLG)

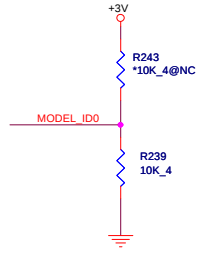
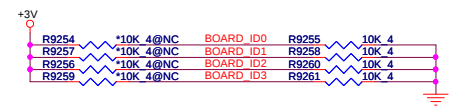


BOARD ID SETTING

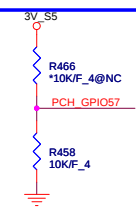
Board ID For Function	ID2 GPIO38	ID1 GPIO37	ID0 GPIO36
SDV	0	0	0
SIV	0	0	1
STT	0	1	0
SVT	0	1	1
SOVP	1	0	0

	BOARD_ID3 GPIO39
w/ Dock	0
w/o Dock	1

Model ID	MODEL_ID0
14"	0
15"	1



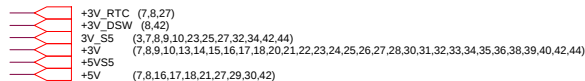
TPM physical presence	
PCH_GPIO57	Low: Default



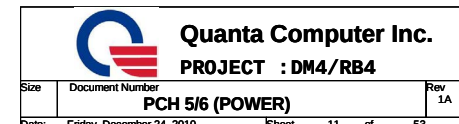
**Quanta Computer Inc.**
PROJECT : DM4/RB4

Size	Document Number	Rev
	PCH 4/6 (GPIO/MISC)	1A
Date:	Friday, December 24, 2010	Sheet 10 of 53

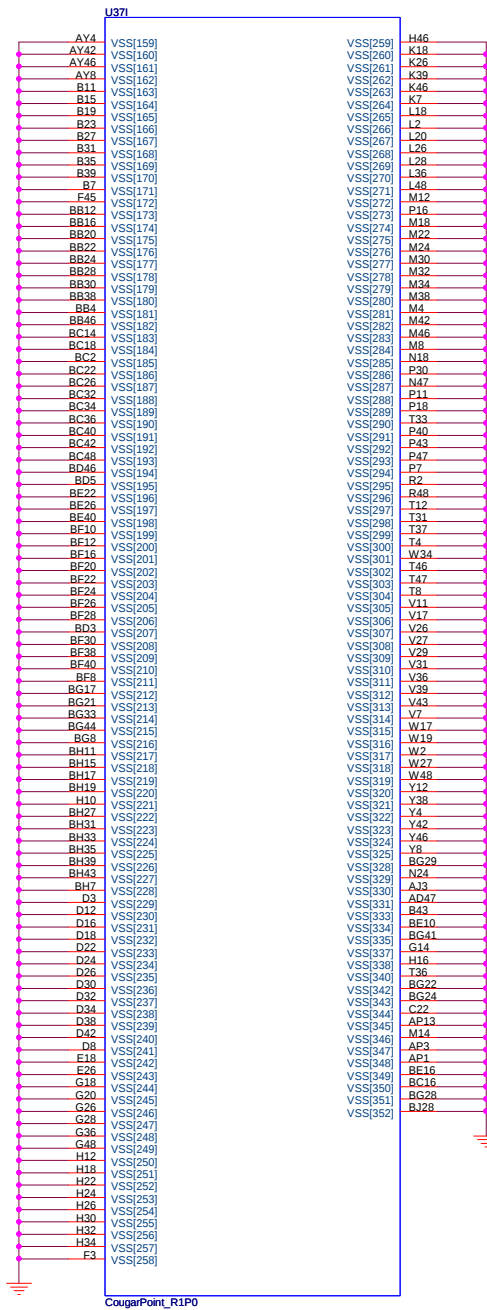
POWER



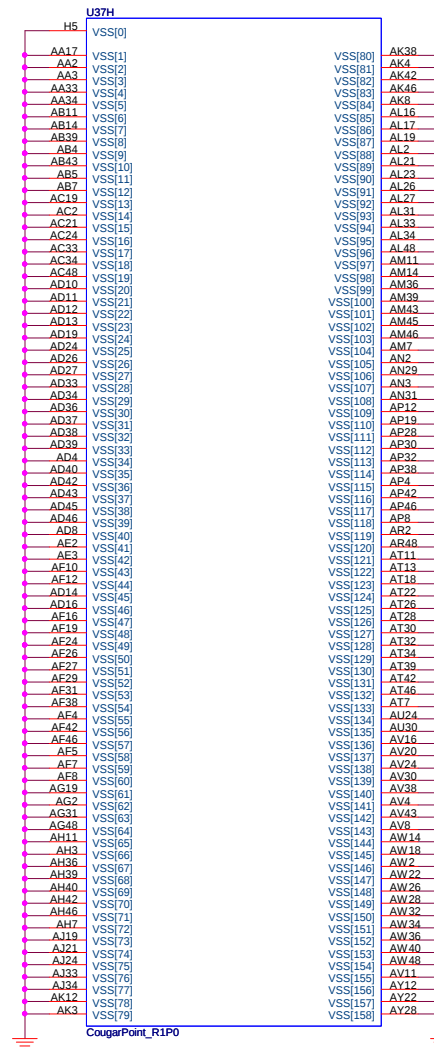
POWER



IBEX PEAK-M (GND)



IBEX PEAK-M (GND)

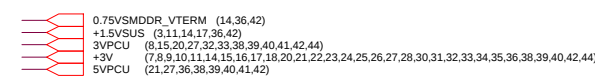


Quanta Computer Inc.

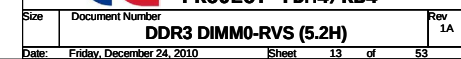
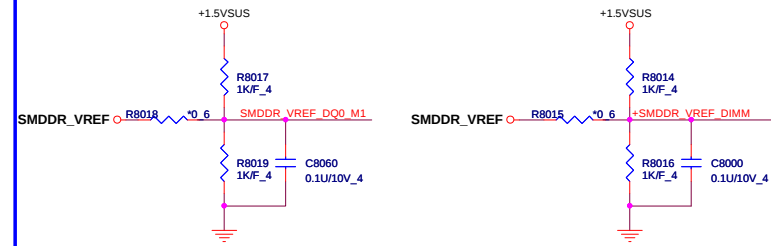
PROJECT : DM4/RB4

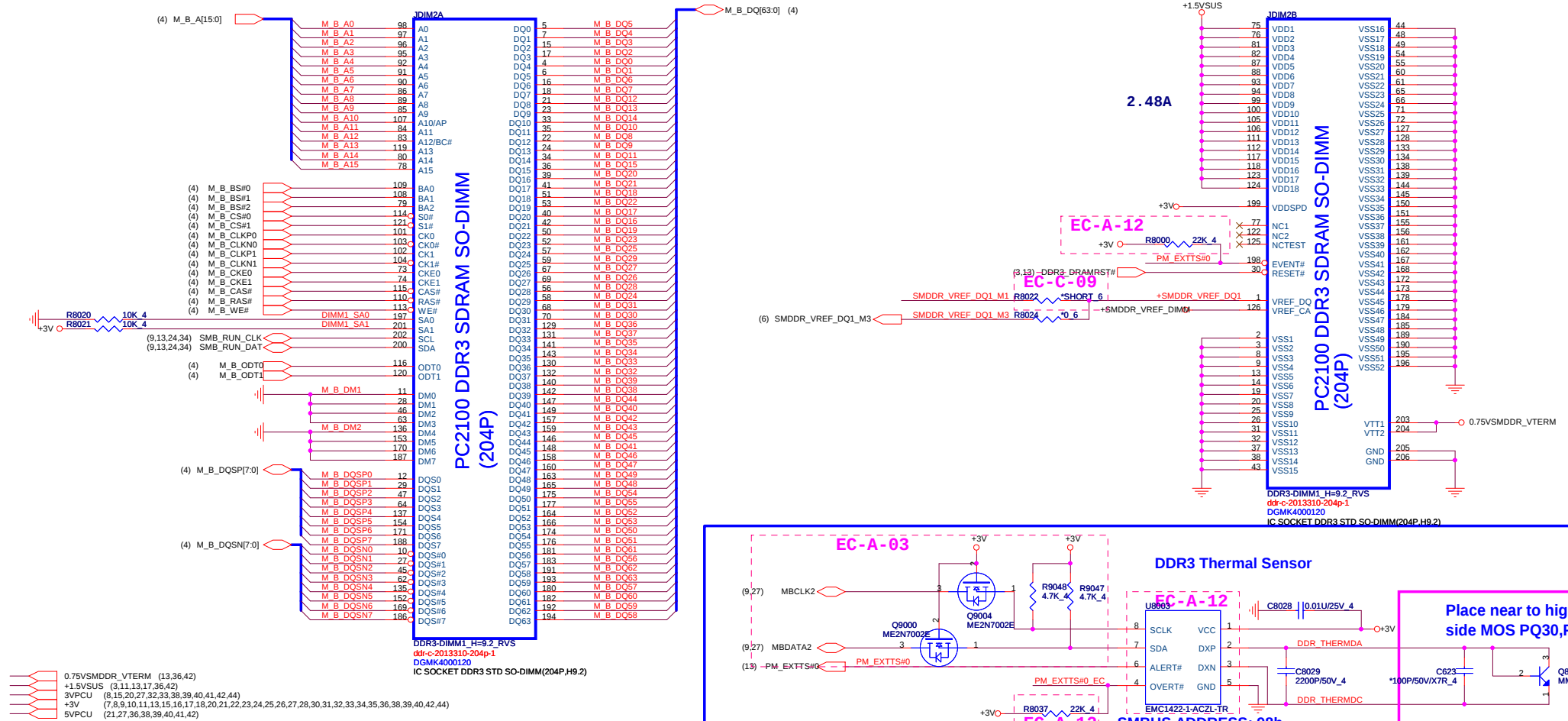
Size	Document Number	Rev
	PCH 6/6 (GND)	1A

Date: Friday, December 24, 2010 Sheet 12 of 53

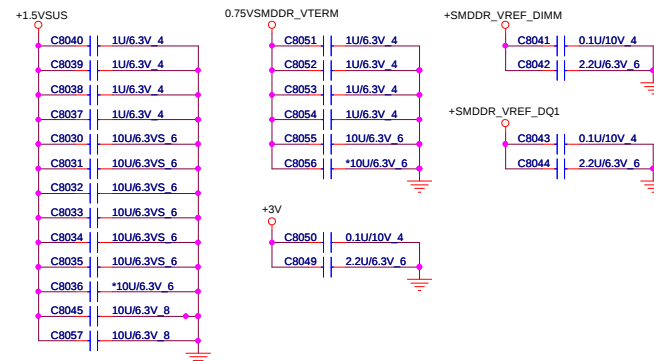


VREF DQ0 M1 Solution

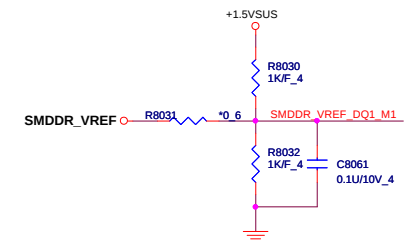




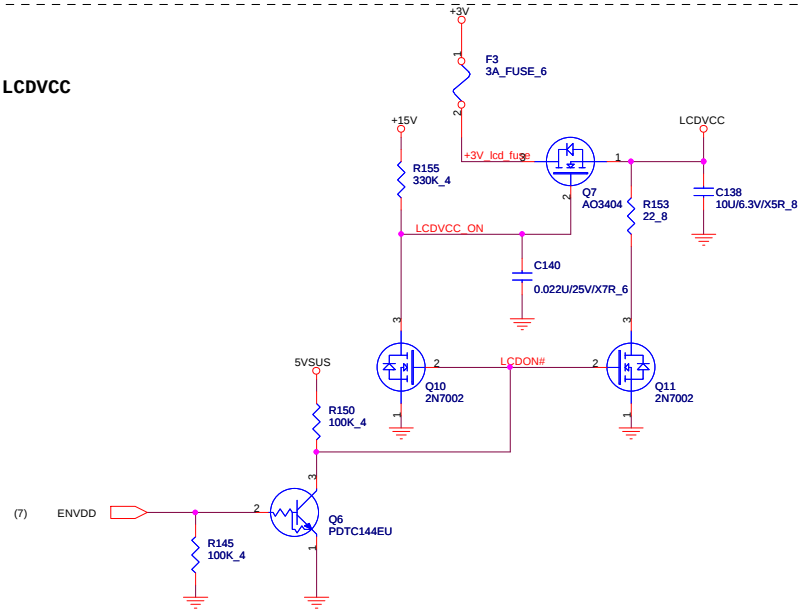
VREF DQ1 M2 Solution



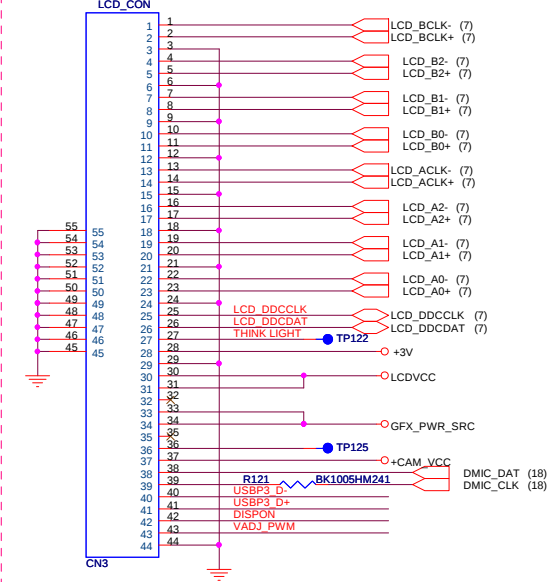
VREF DQ1 M1 Solution



LCDVCC

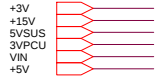


EC-B-04



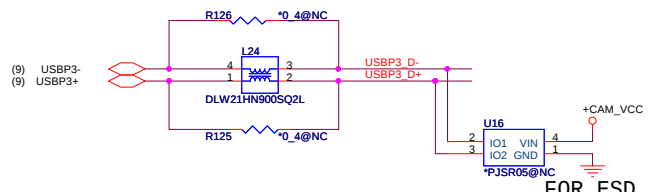
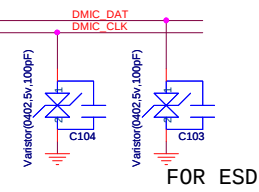
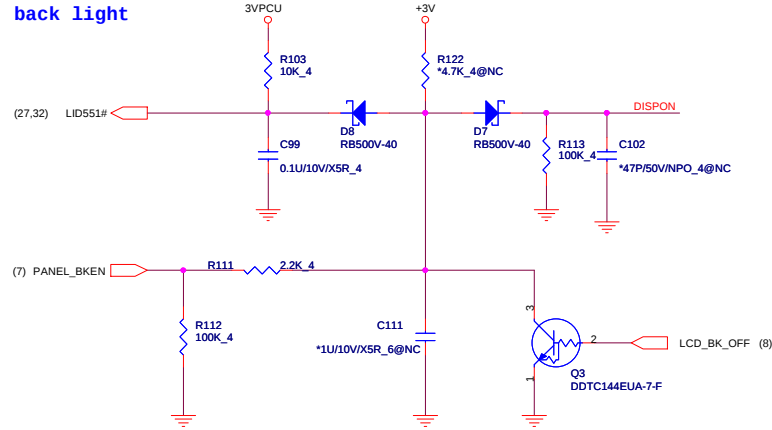
Address : A9H --Contrast
AAH --Backlight

(7,8,9,10,11,13,14,16,17,18,20,21,22,23,24,25,26,27,28,30,31,32,33,34,35,36,38,39,40,42,44)
(31,36,40,42)
(35,42)
(8,20,27,32,33,38,39,40,41,42,44)
(35,36,38,39,40,41,42)
(7,8,11,16,17,18,21,27,29,30,42)

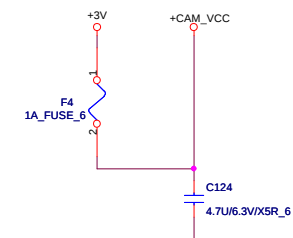


15

back light

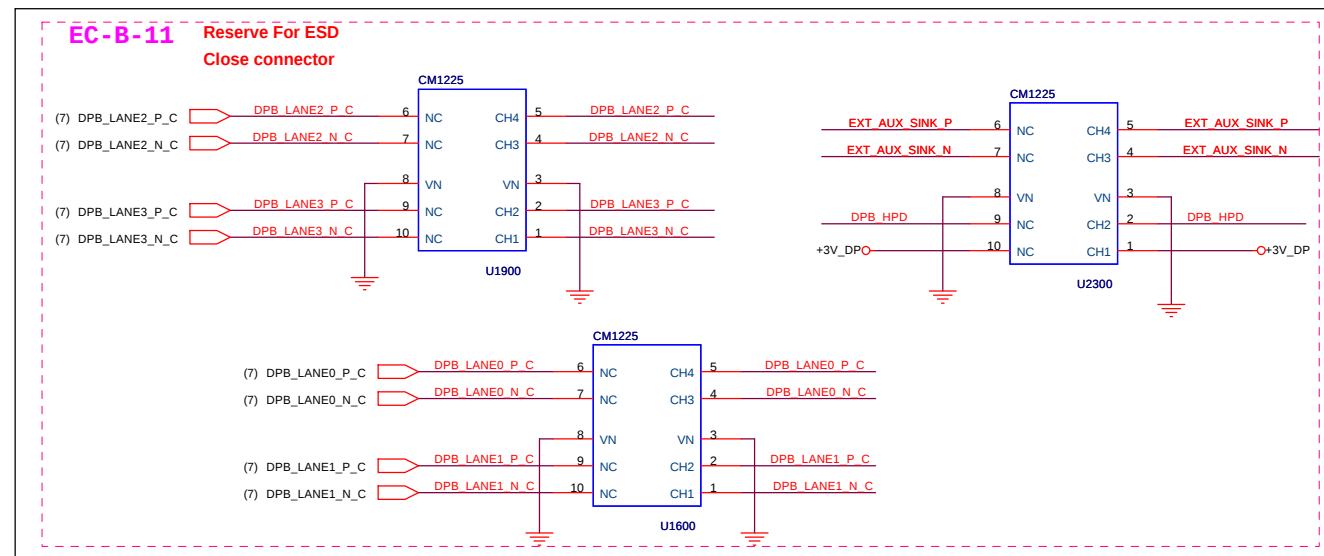
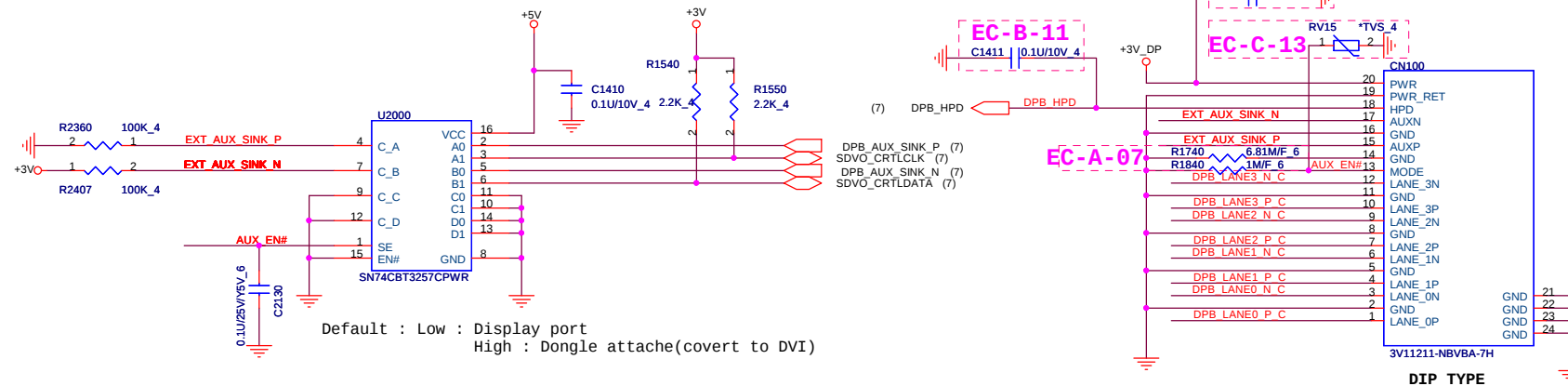


CAMERA VCC Control

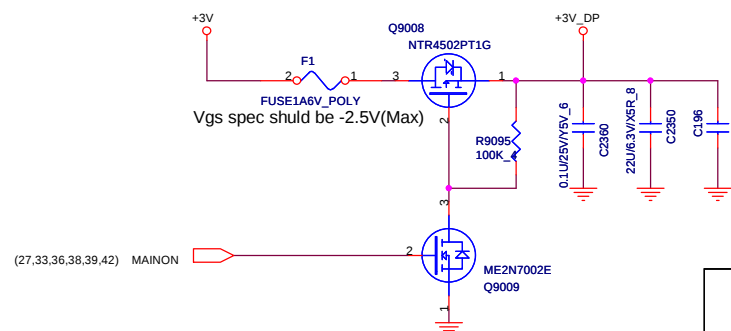
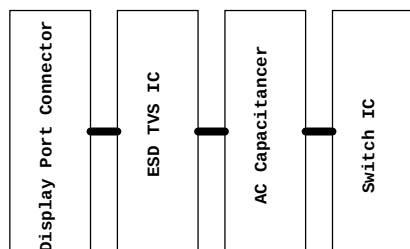


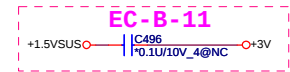
Display Port

16

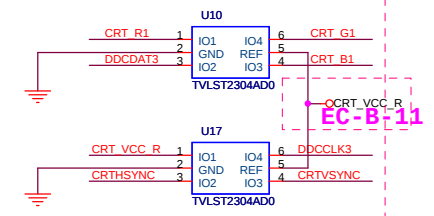


Layout Topology



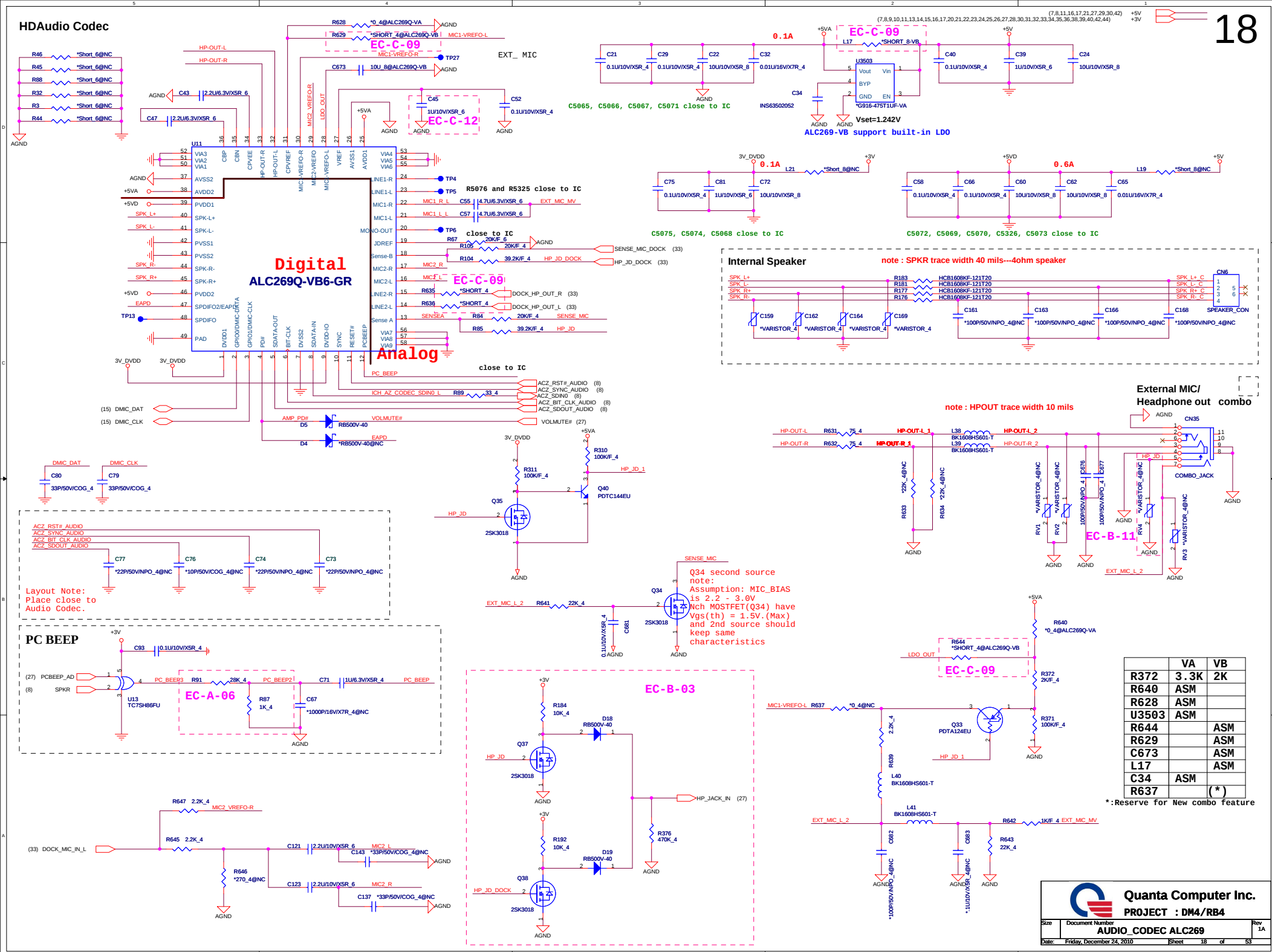


ESD PROTECTION



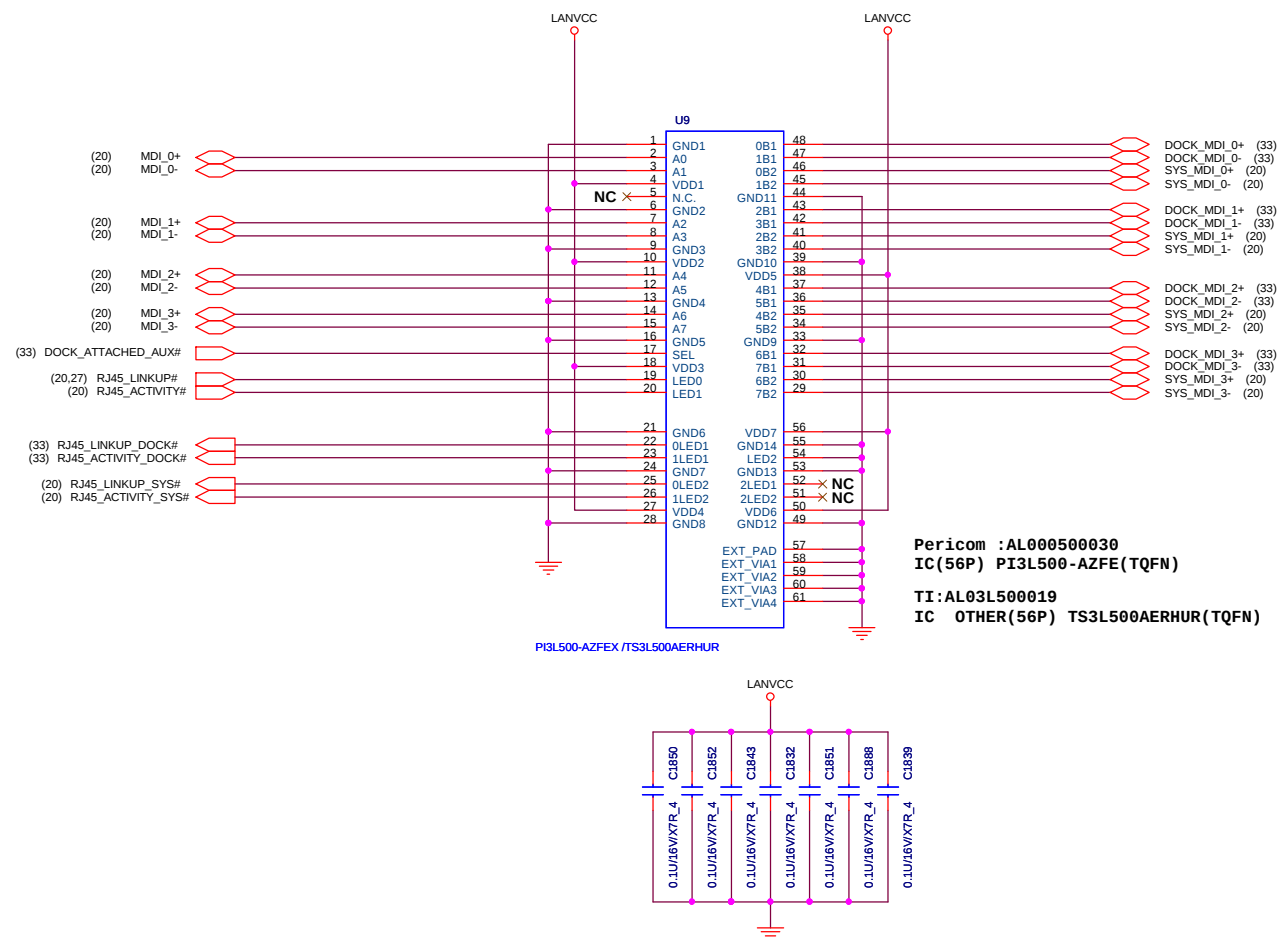
SEL	FUNCTION(COM)
LOW	IN_x0
HIGH	IN_x1

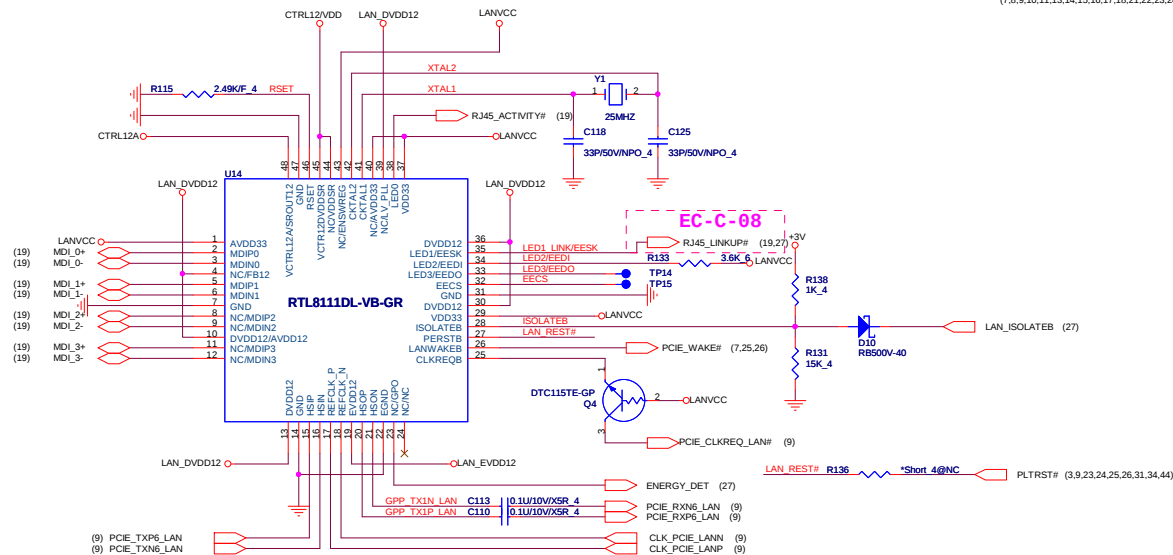
HDAudio Codec



	VA	VB
R372	3.3K	2K
R640	ASM	
R628	ASM	
U3503	ASM	
R644		ASM
R629		ASM
C673		ASM
L17		ASM
C34	ASM	
R637		(*)

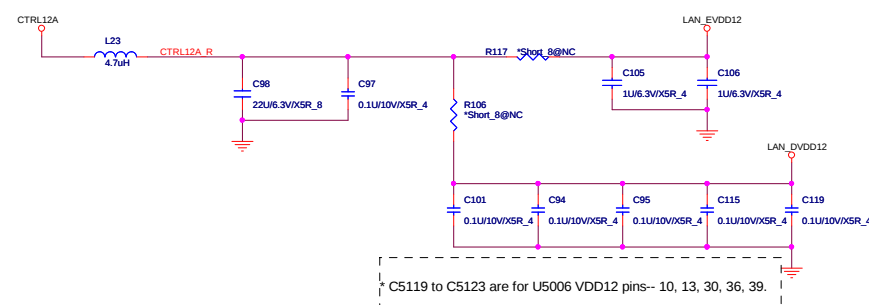
*:Reserve for New combo feature



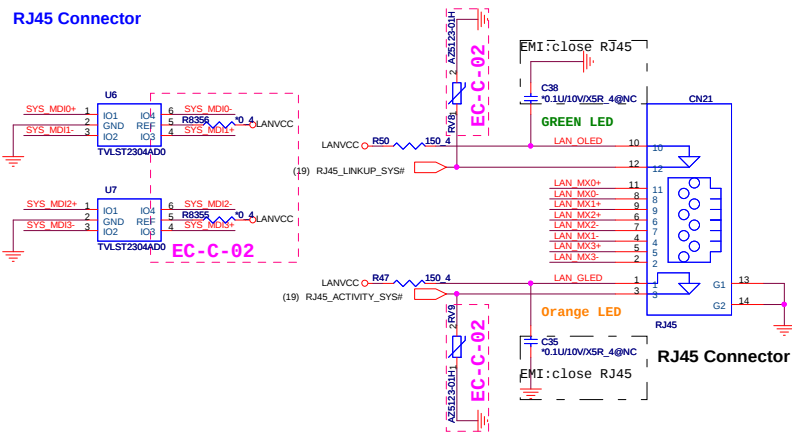


* C5110
and 40.

Place C5113 ,C5094 closed to U5006 pins44,45.



Layout: All termination signal should have 20 mil trace

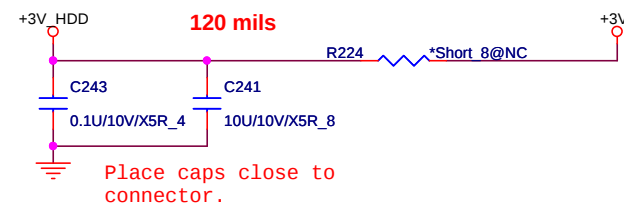
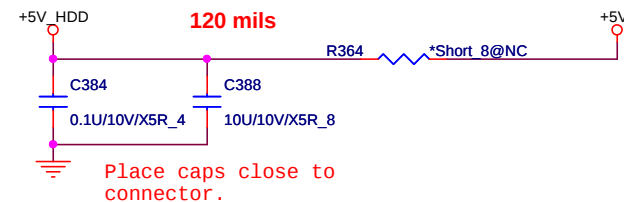
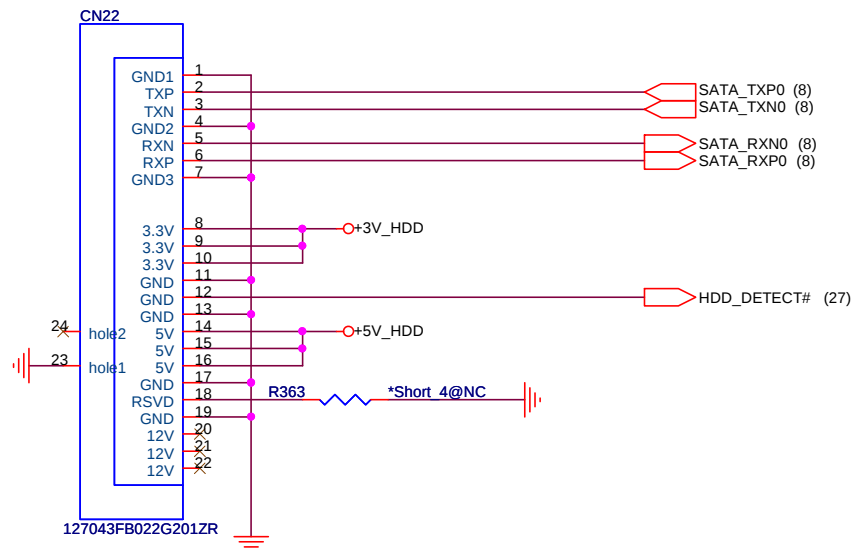


SATA Connector.

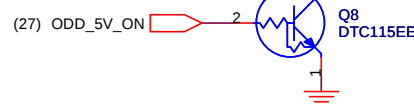
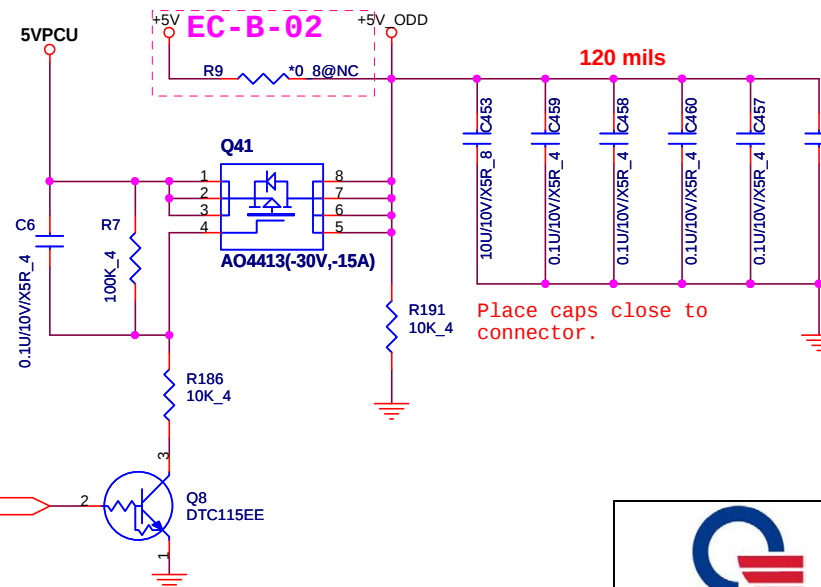
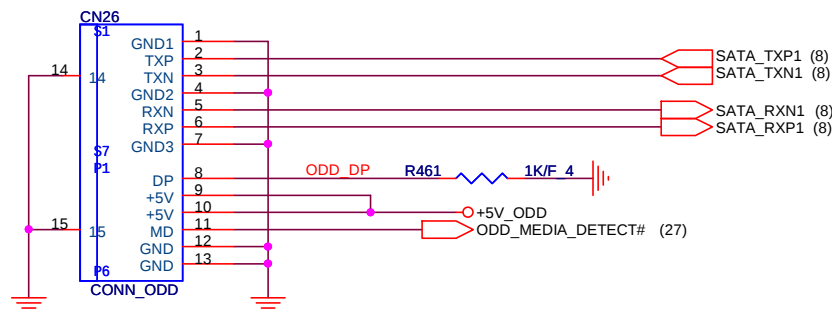
(7,8,11,16,17,18,27,29,30,42) +5V
(7,8,9,10,11,13,14,15,16,17,18,20,22,23,24,25,26,27,28,30,31,32,33,34,35,36,38,39,40,42,44) +3V



21



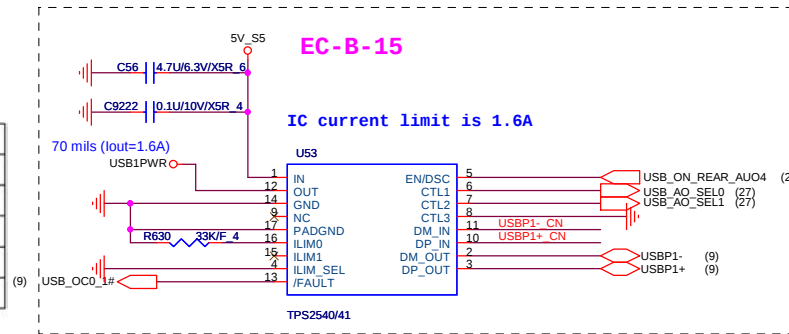
ODD Connector



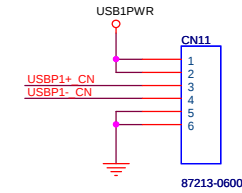
TPS2541 table

CTL1	CTL2	CTL3	Mode
0	0	X	Dedicated Charging Port, Auto-detect
0	1	X	Dedicated Charging Port, BC Specification 1.1 Only
1	0	X	Dedicated Charging Port, Apple Only
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

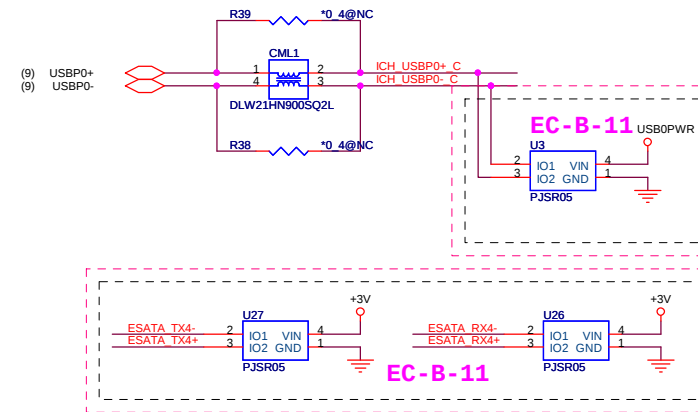
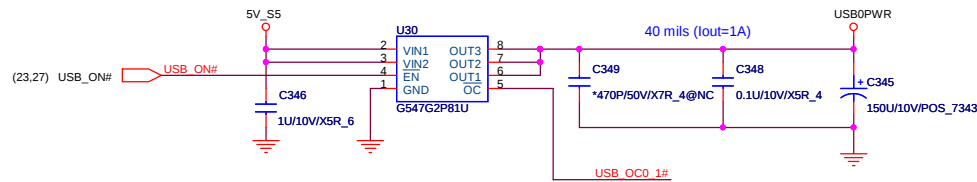
Table 3 – TPS2541 Control Truth Table



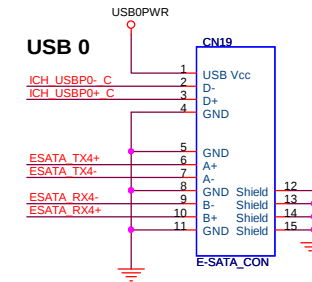
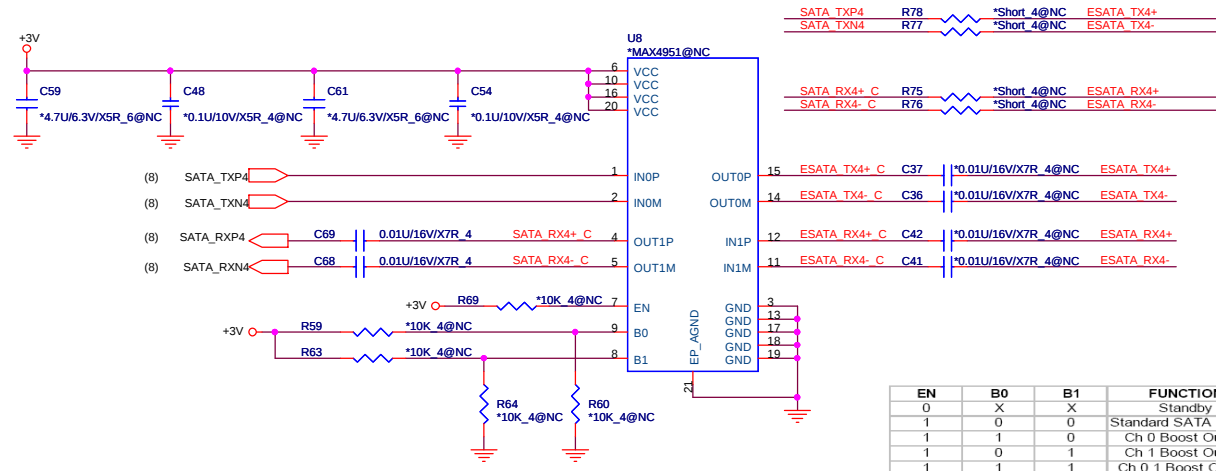
USB X1----> Wire to board conn



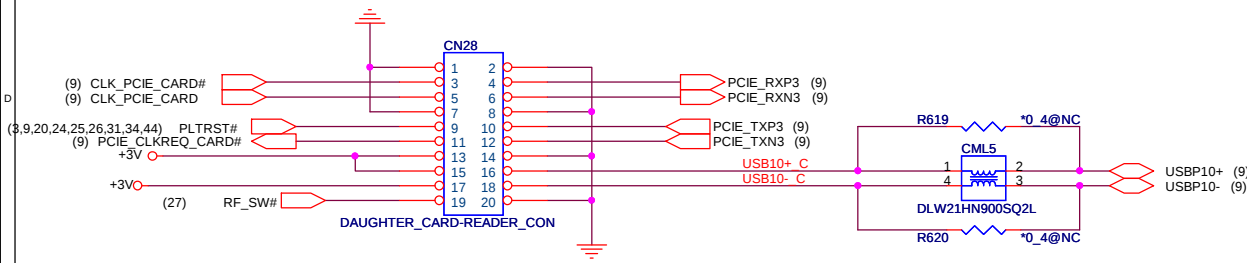
USB + E-SATA



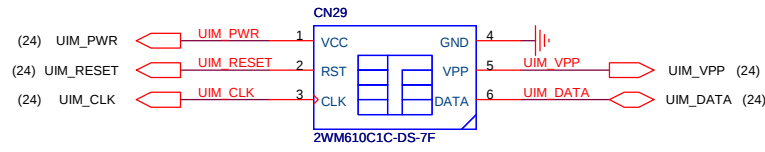
E-SATA RE-DRIVER



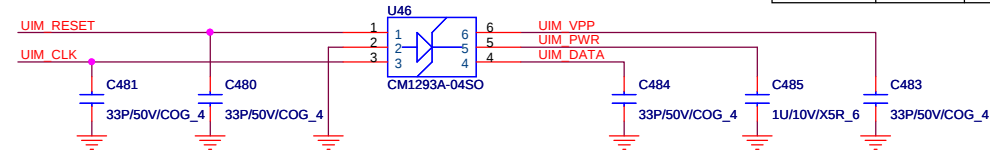
Quanta Computer Inc.
PROJECT : DM4/RB4



SIM Card CONN

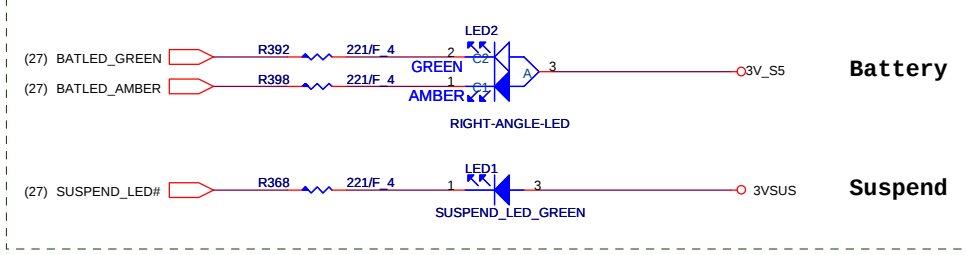


Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible

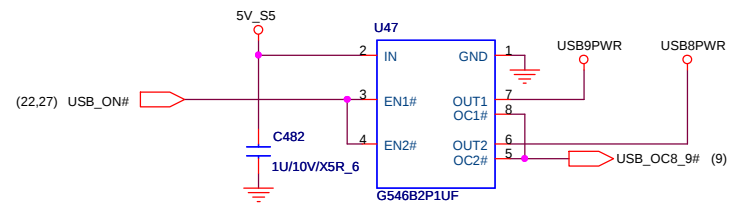
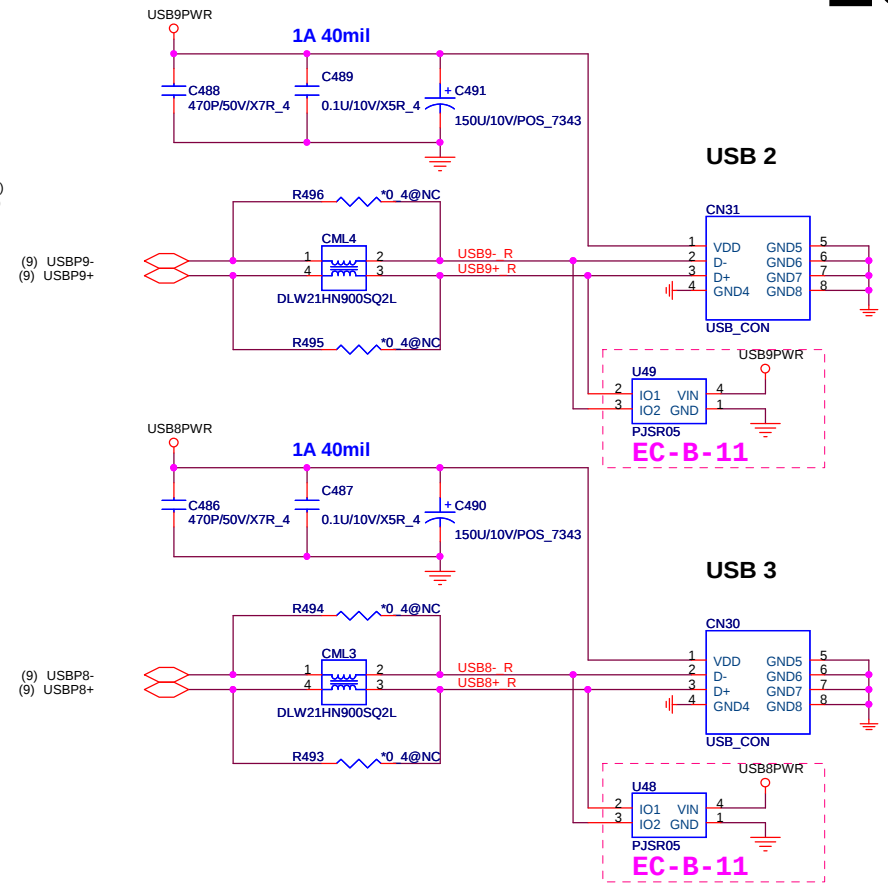


	w/ WWAN	w/o WWAN
CN29	ASM	NO ASM
U46	ASM	NO ASM
C480-C481	ASM	NO ASM
C483-C485	ASM	NO ASM

FRONT LEDs

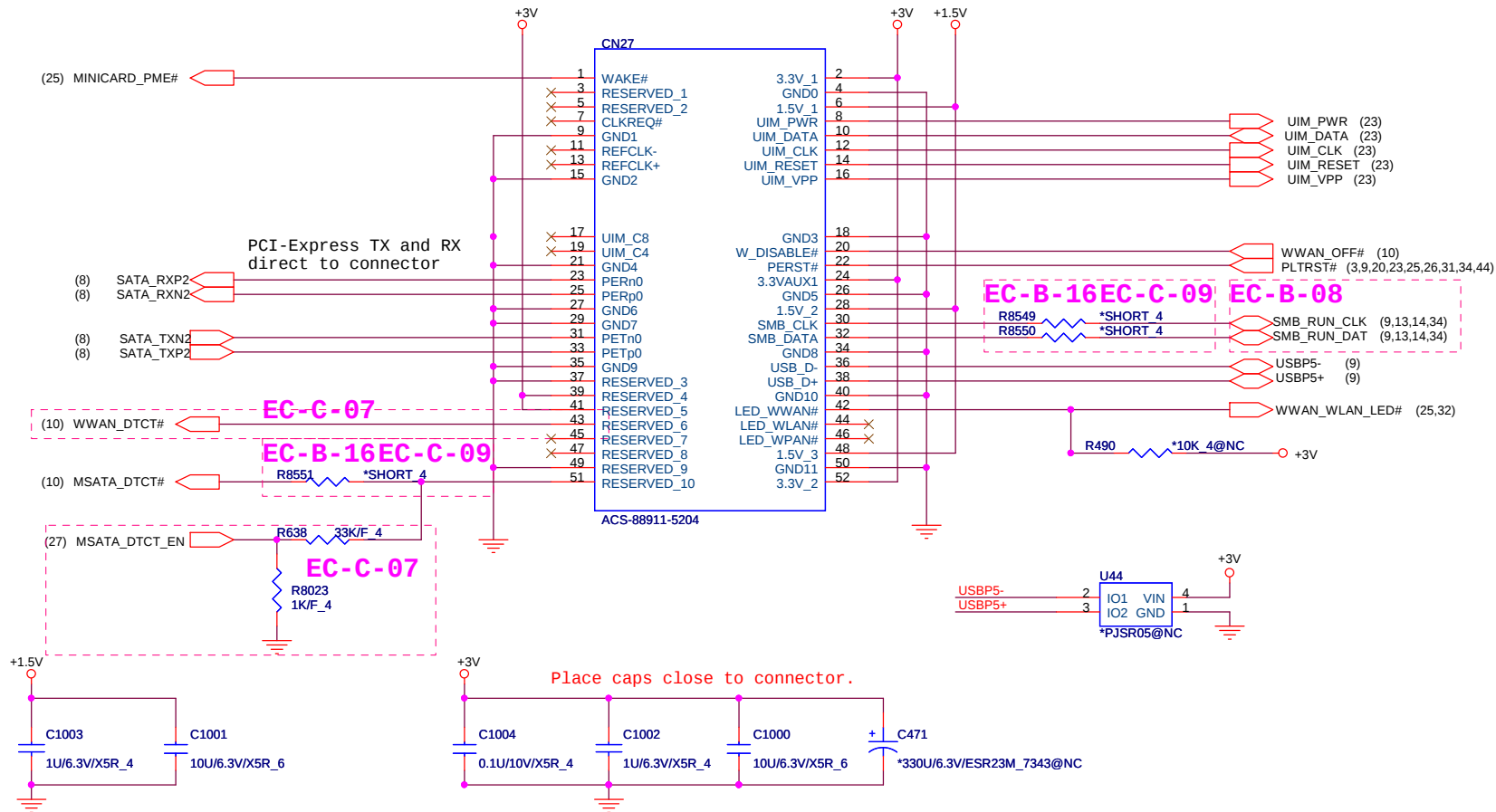


(7,8,9,10,11,13,14,15,16,17,18,20,21,22,24,25,26,27,28,30,31,32,33,34,35,36,38,39,40,42,44)
(8,15,20,27,32,33,38,39,40,41,42,44)
(11,22,42)
5V_S5
+3V
3VPCU
3VSUS



MiniCard WWAN connector

24



	w/ WWAN	w/o WWAN
CN27	ASM	NO ASM
R489	ASM	NO ASM
R484	ASM	NO ASM
R483	ASM	NO ASM
C1000~C1004	ASM	NO ASM



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PROJECT : DM4/RB4

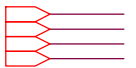
Size	Document Number	Rev
	MINI-Card (SSD, WWAN)	1A

Date: Friday, December 24, 2010 Sheet 24 of 53

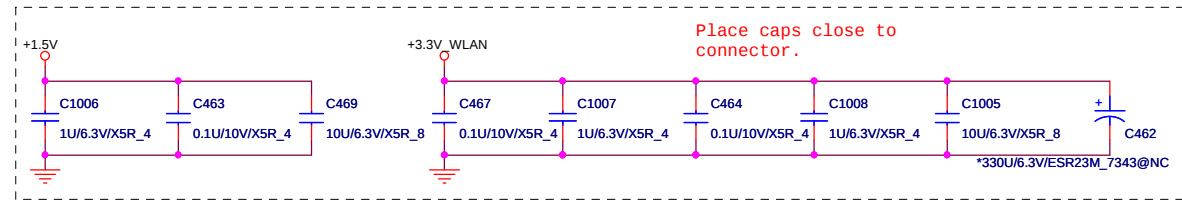
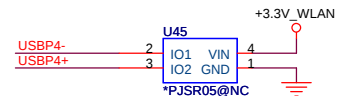
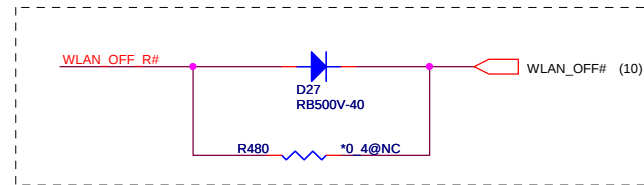
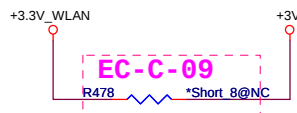
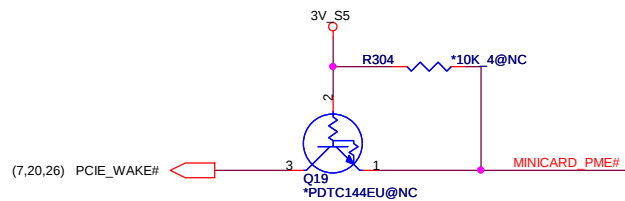
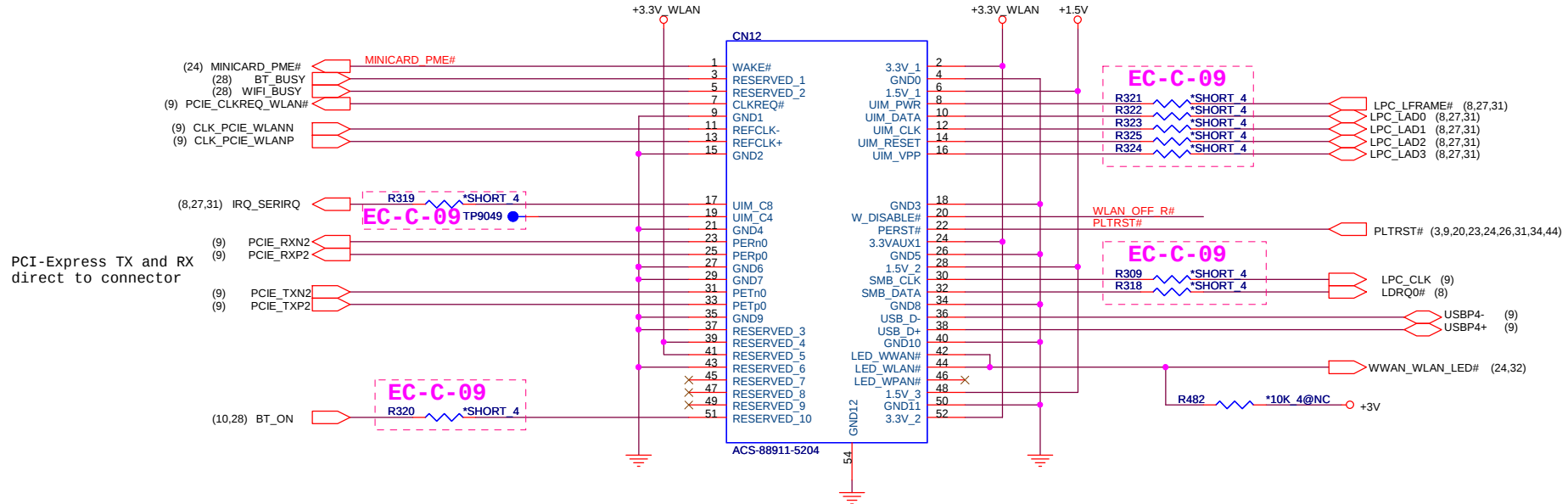
MiniCard WLAN/WiMAX connector

(7,8,9,10,11,13,14,15,16,17,18,20,21,22,23,24,26,27,28,30,31,32,33,34,35,36,38,39,40,42,44)
(11,24,26,36)
(8,15,20,27,32,33,38,39,40,41,42,44)
(15,35,36,38,39,40,41,42)

+3V
+1.5V
3VPCU
VIN



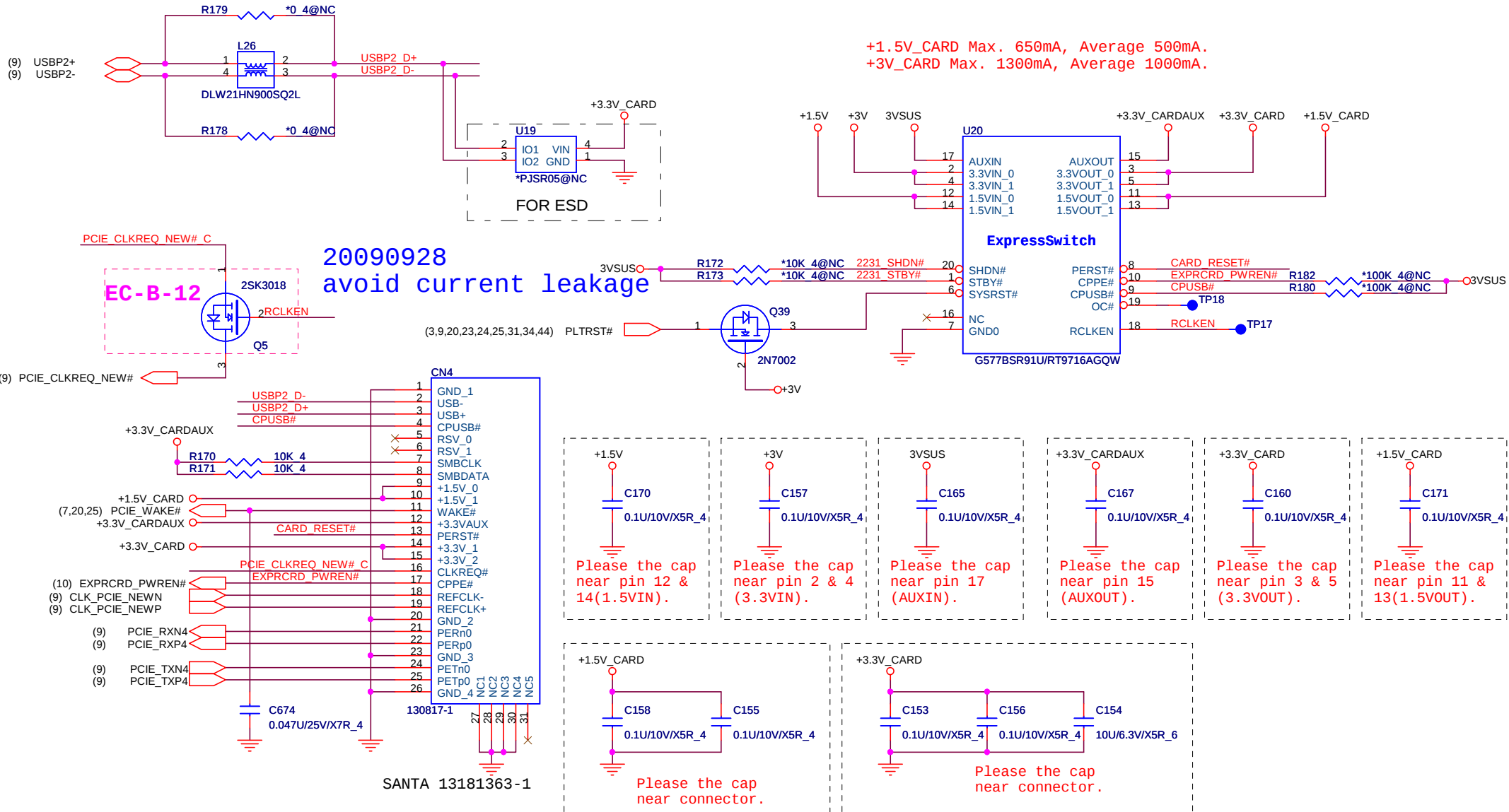
25

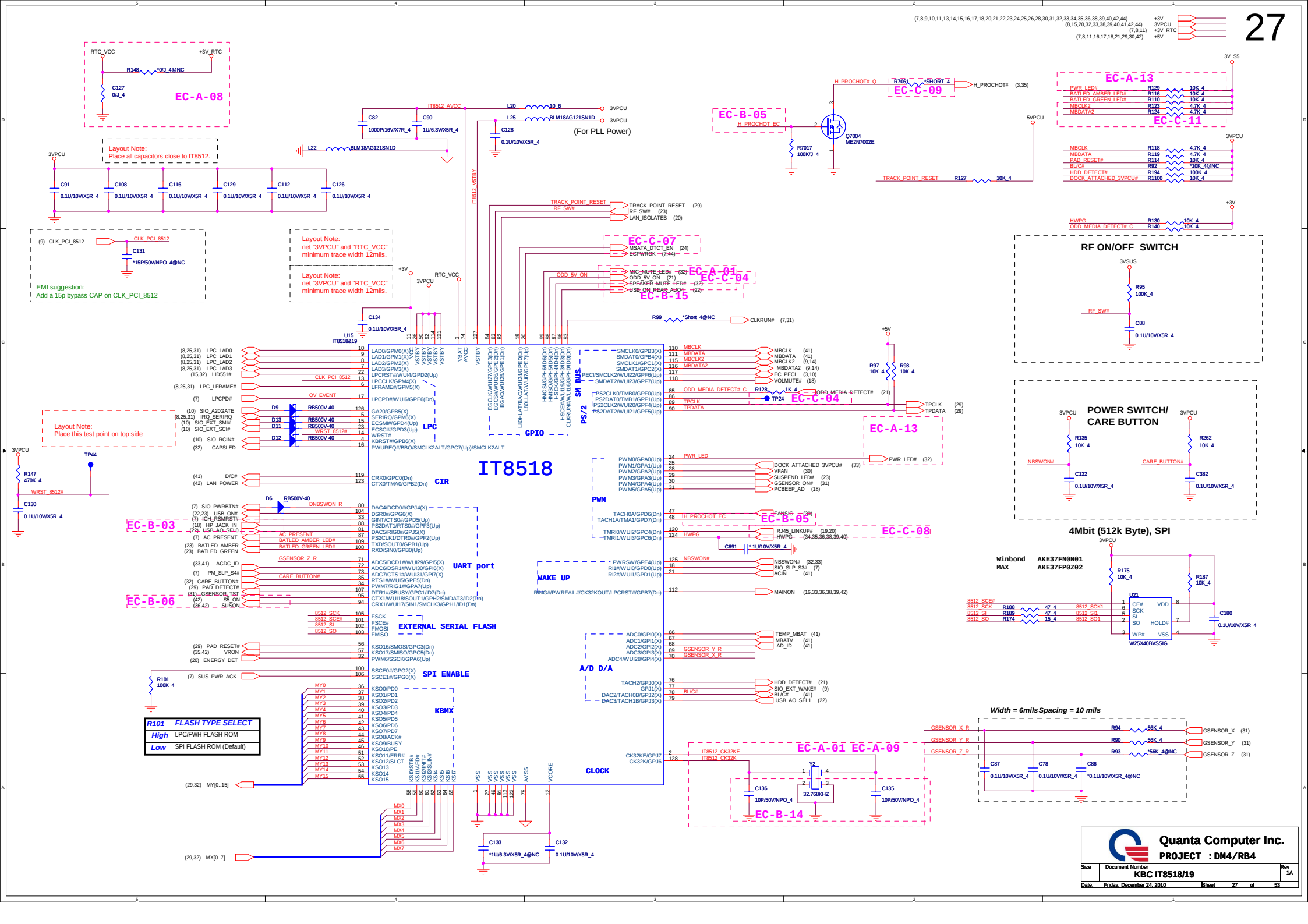


Express Card

(7,8,9,10,11,13,14,15,16,17,18,20,21,22,23,24,25,27,28,30,31,32,33,34,35,36,38,39,40,42,44) +3V
(11,24,25,36) +1.5V
(23,27,42) 3VSUS

26



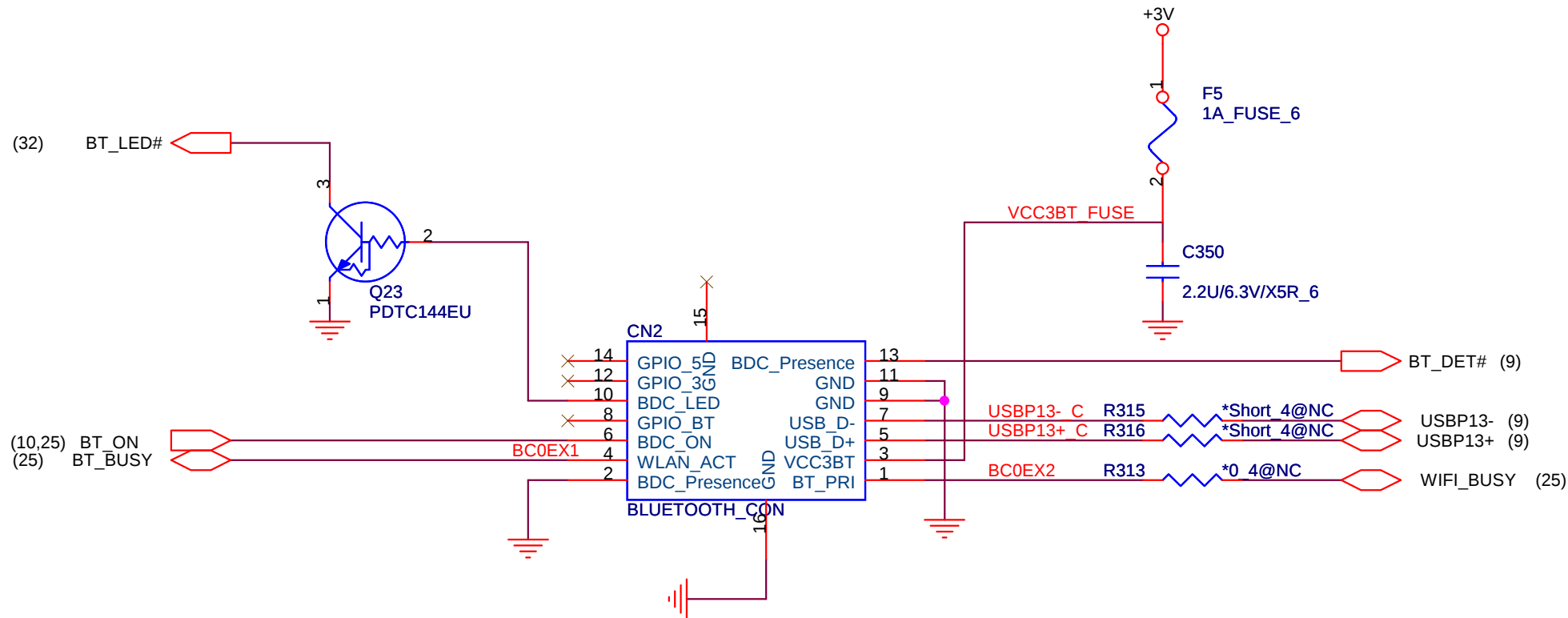


BLUETOOTH

(7,8,9,10,11,13,14,15,16,17,18,20,21,22,23,24,25,26,27,30,31,32,33,34,35,36,38,39,40,42,44)

+3V

28



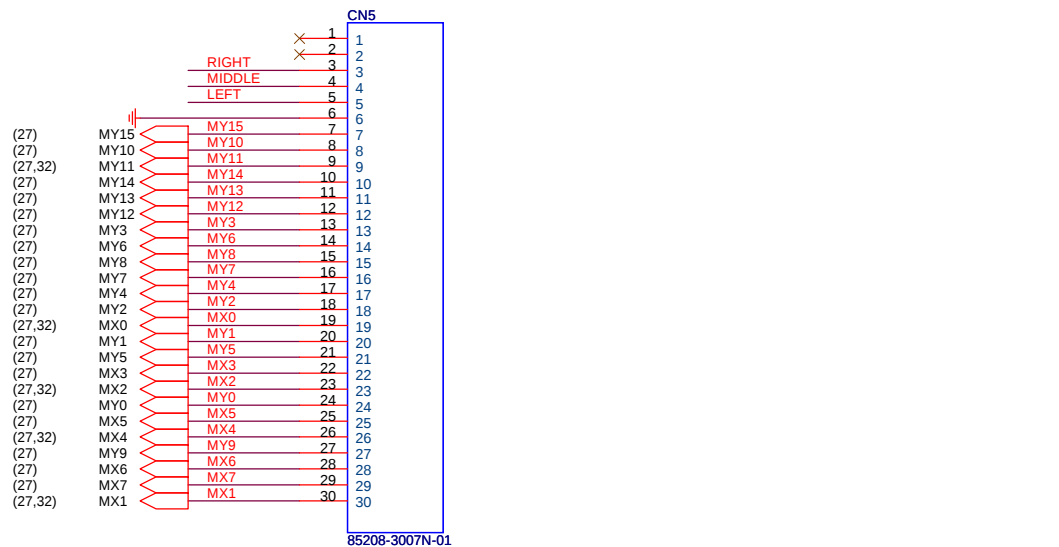
Quanta Computer Inc.

PROJECT : DM4/RB4

Size	Document Number B/T	Rev 1A
Date:	Friday, December 24, 2010	Sheet 28 of 53

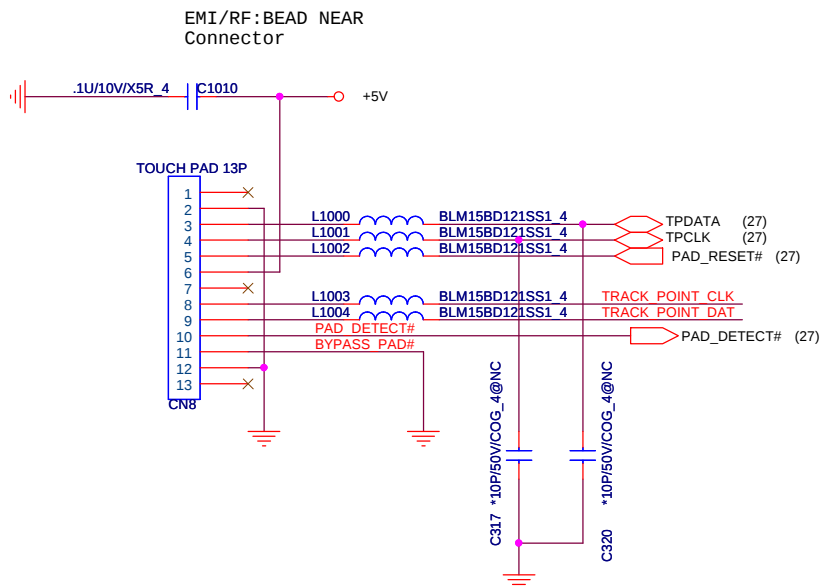
KEYBOARD

KEYBOARD connector

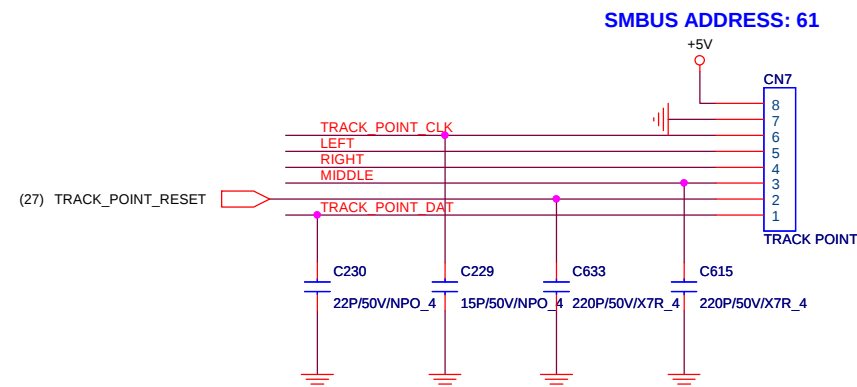


29

Touch pad



TRACK POINT



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PROJECT : DM4/RB4

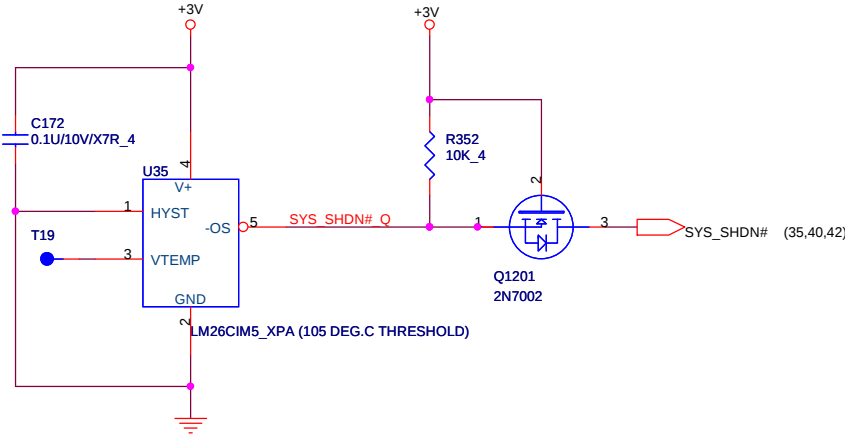
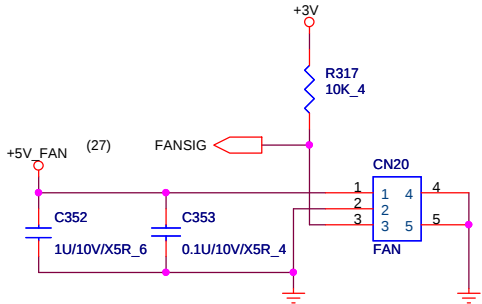
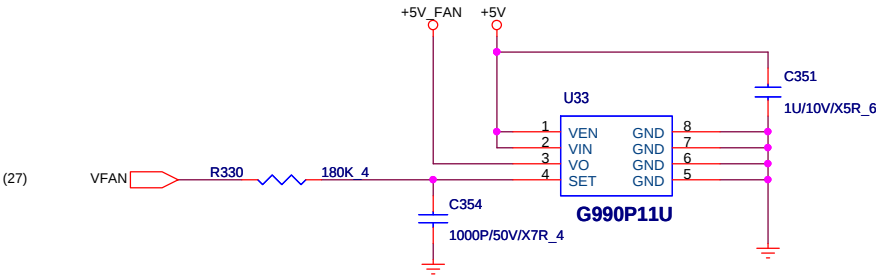
Size	Document Number	Rev
	K/B, T/P	1A

Date: Friday, December 24, 2010 Sheet 29 of 53

FAN CONTROL

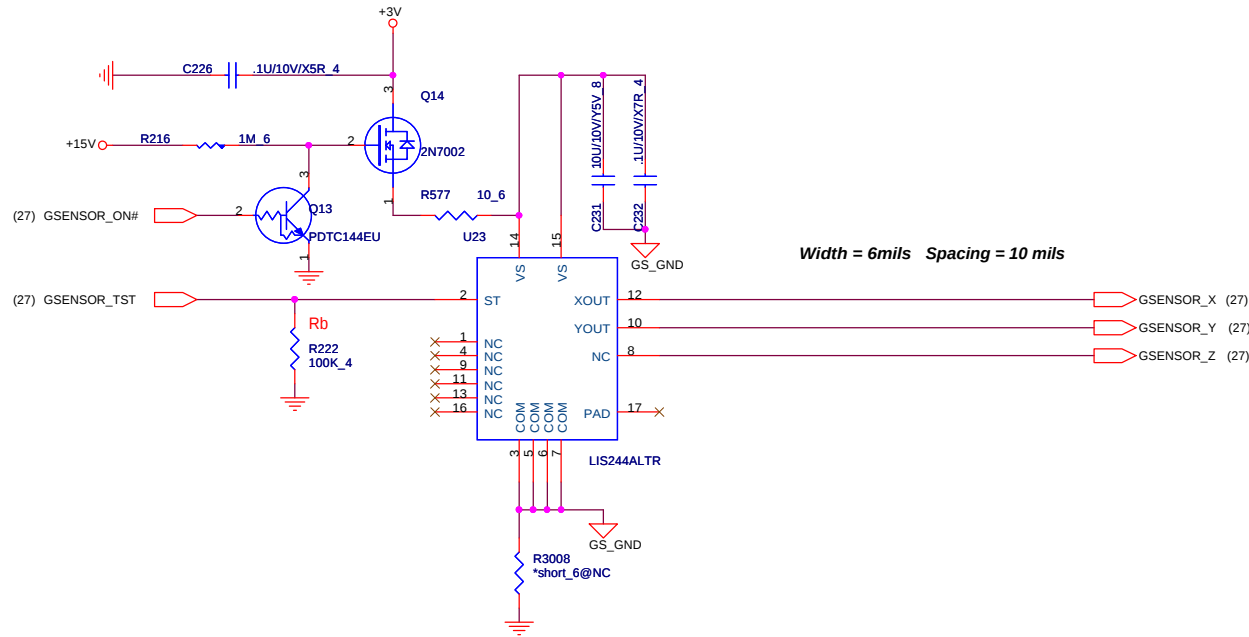
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(7,8,11,16,17,18,21,27,29,42)

+3V
+5V

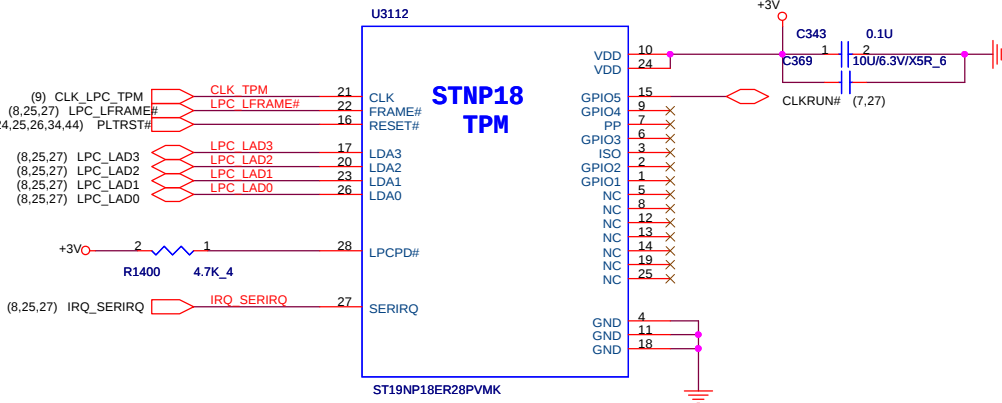


G-SENSOR (2-Axial)

31



Discrete TPM



supplier P/N:ST19NP18ER28PVMK
Quanta P/N:AL19NP18K27
F/P:tssop28-6_4-65-1_2h

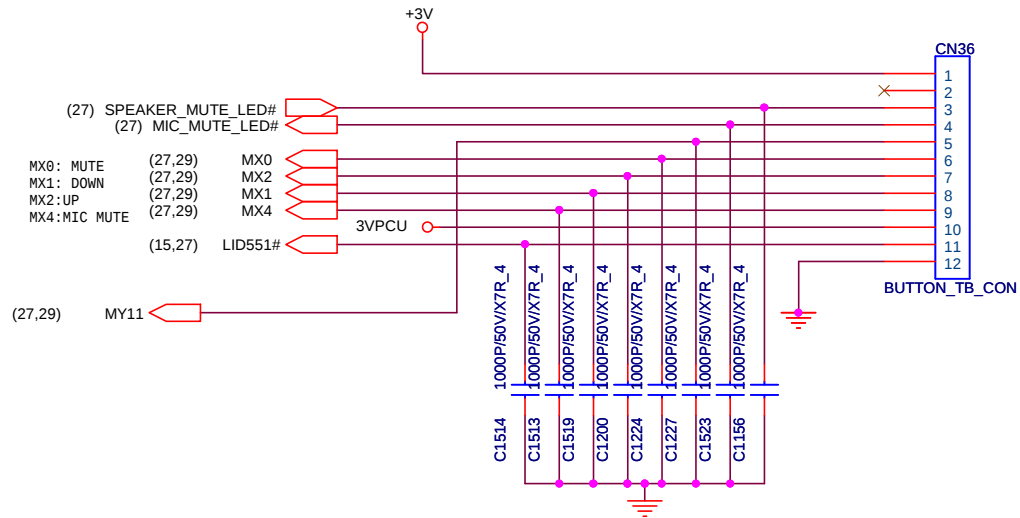


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PROJECT : DM4/RB4

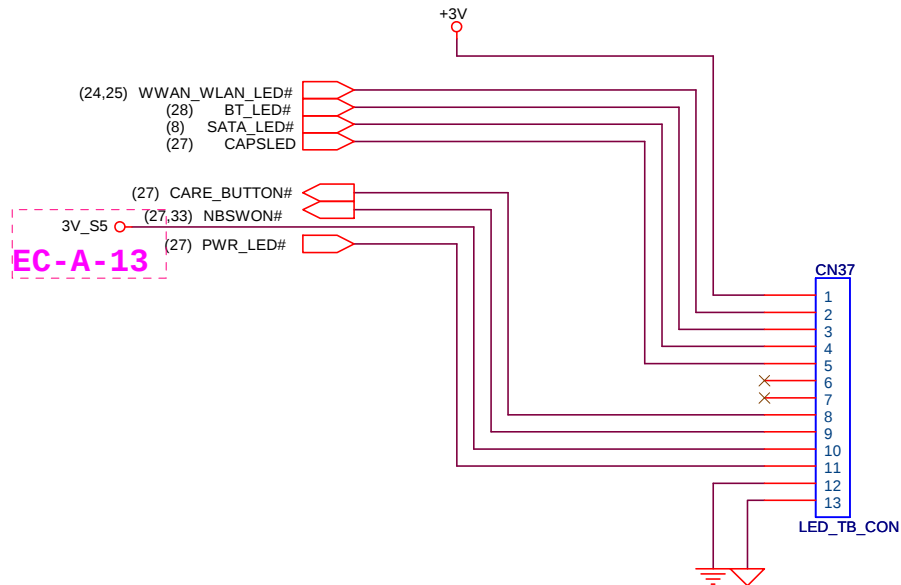
Size	Document Number	Rev
	G-SENSOR/Discrete TPM	1A
Date:	Friday, December 24, 2010	Sheet 31 of 53

Daughter Boards for LEDs & Ports

FFC TO KBD LEFT SIDE CONNECTOR



FFC TO LED RIGHT SIDE CONNECTOR



EC-A-13

iTPM ENABLE/DISABLE

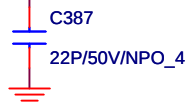


iTPM Function	R366
Enable	1K
Disable	NC

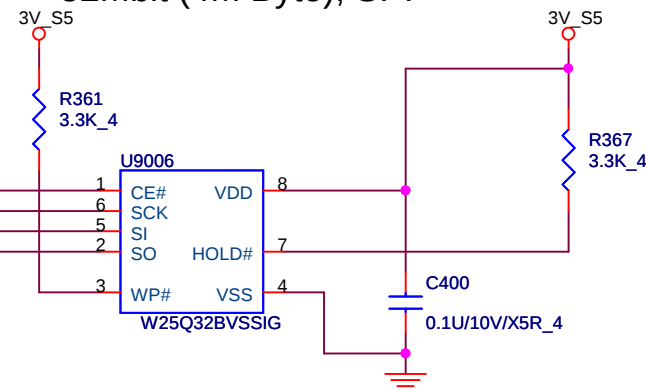
(8) SPI_CS0#_R
(8) SPI_CLK_R
(8) SPI_SI_R
(8) SPI_SO

SPI_CS0#_R
SPI_CLK_R
SPI_SI_R
SPI_SO

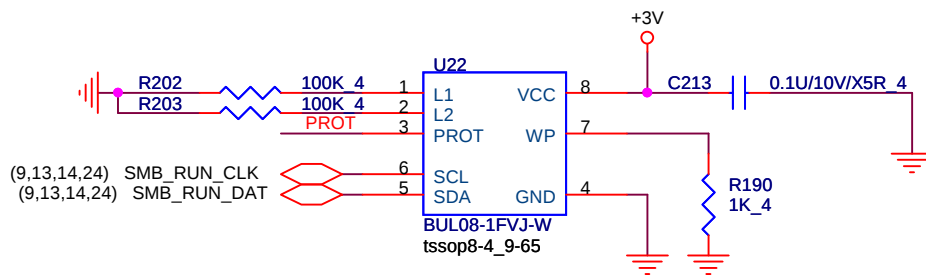
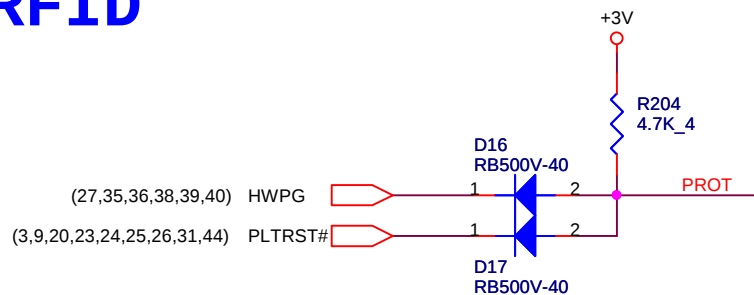
R377 *SHORT 4 SPI_CS0#
R365 *SHORT 4 SPI_CLK
R362 *SHORT 4 SPI_SI
R378 *SHORT 4 SPI_SO_R
EC-C-09



For PCH
32Mbit (4M Byte), SPI

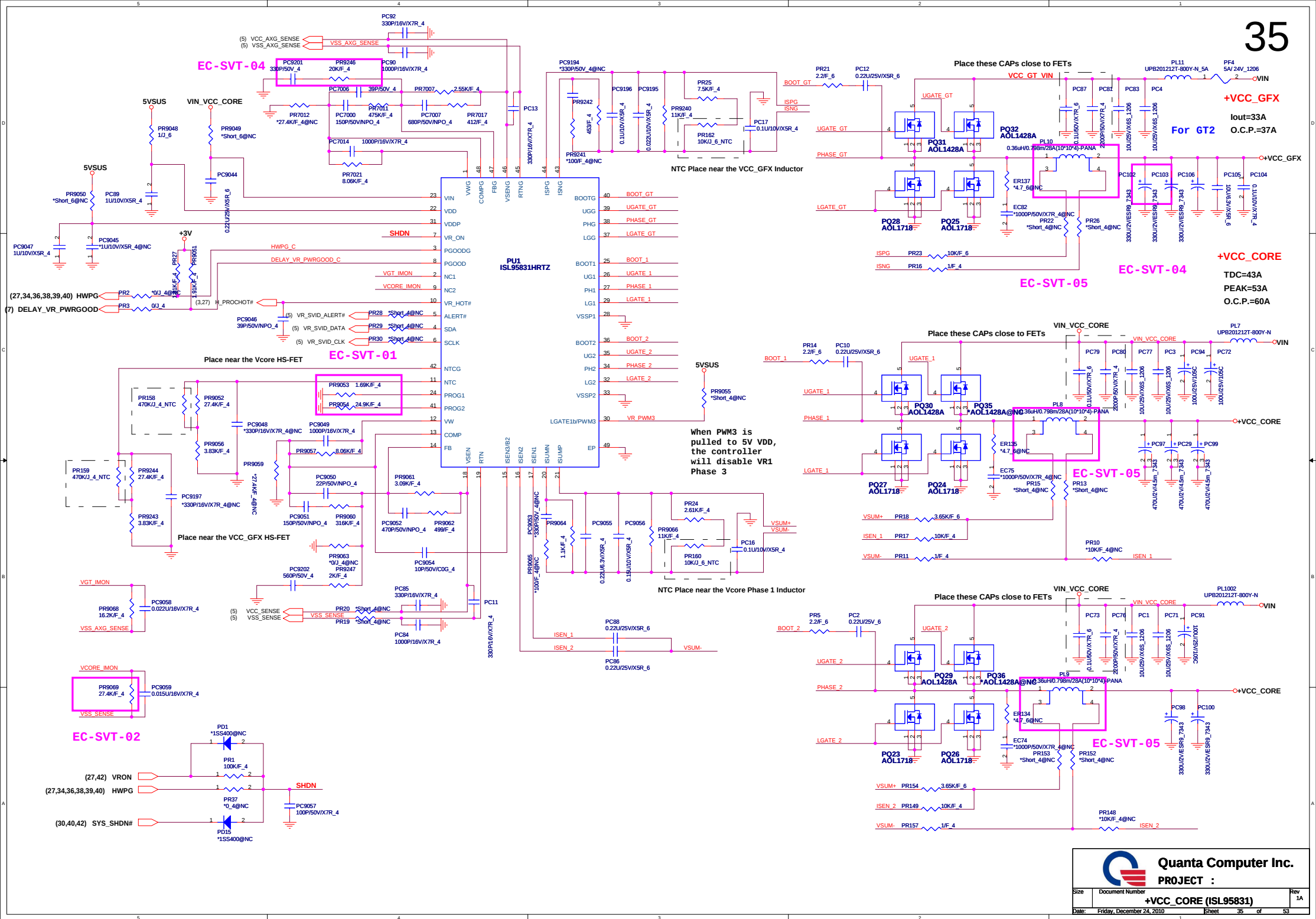


RFID



Quanta Computer Inc.
PROJECT : DM4/RB4

Size	Document Number	Rev
	iTPM & RFID EEPROM	1A
Date:	Friday, December 24, 2010	Sheet 34 of 53





D
C
B
A

D
C
B
A

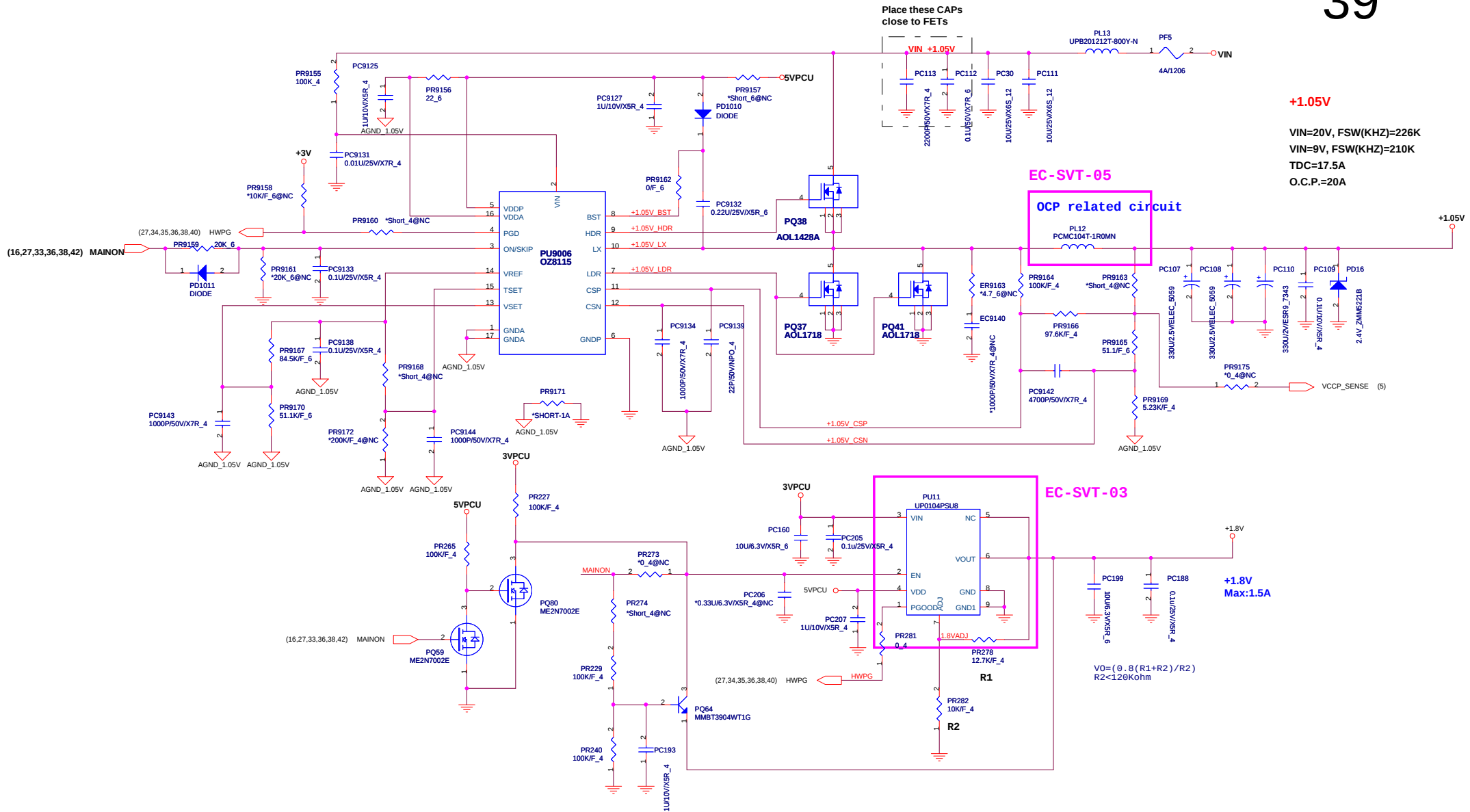


Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev 1A
Date: Friday, December 24, 2010	Sheet 37 of 53	





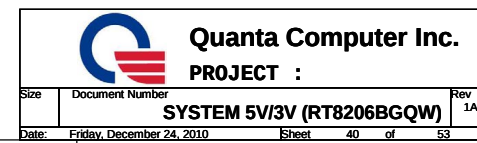
Quanta Computer Inc.

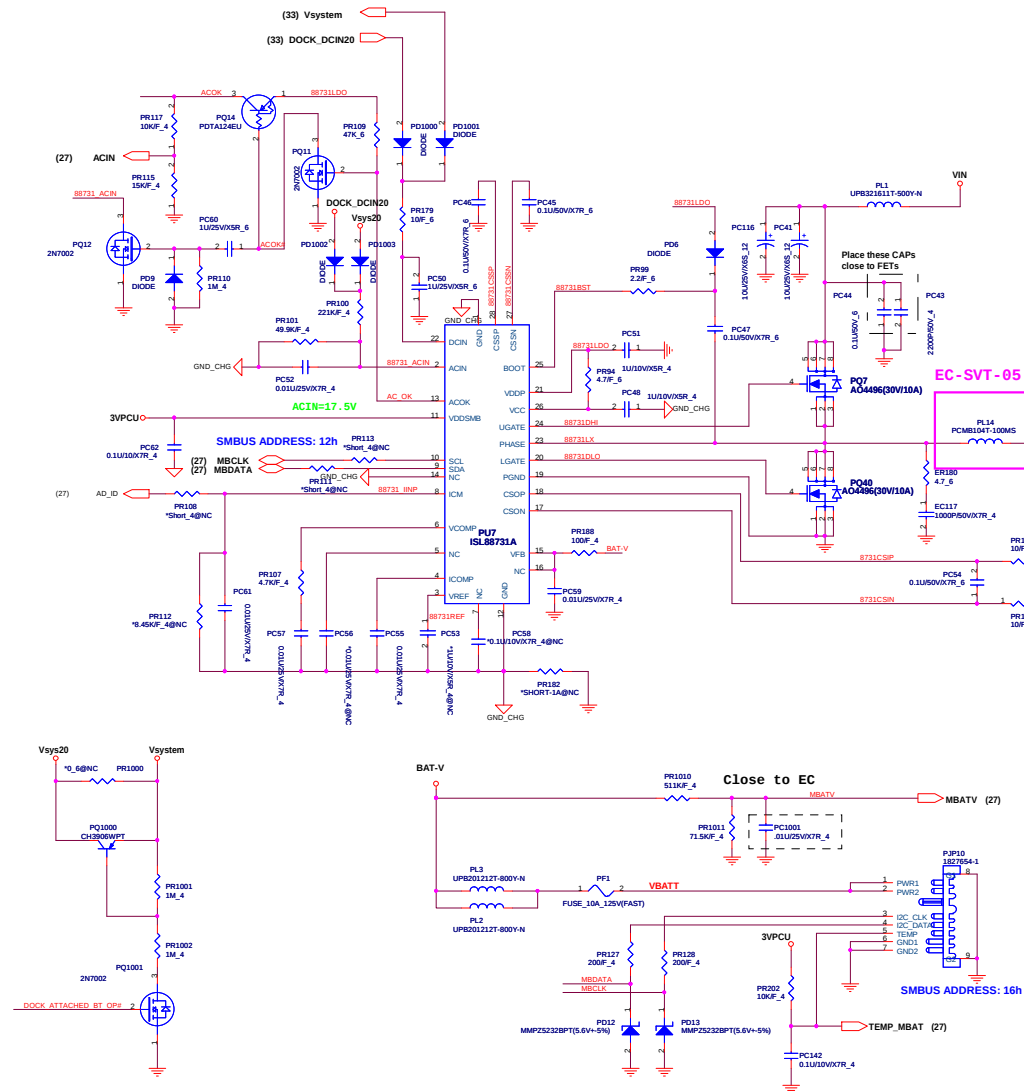
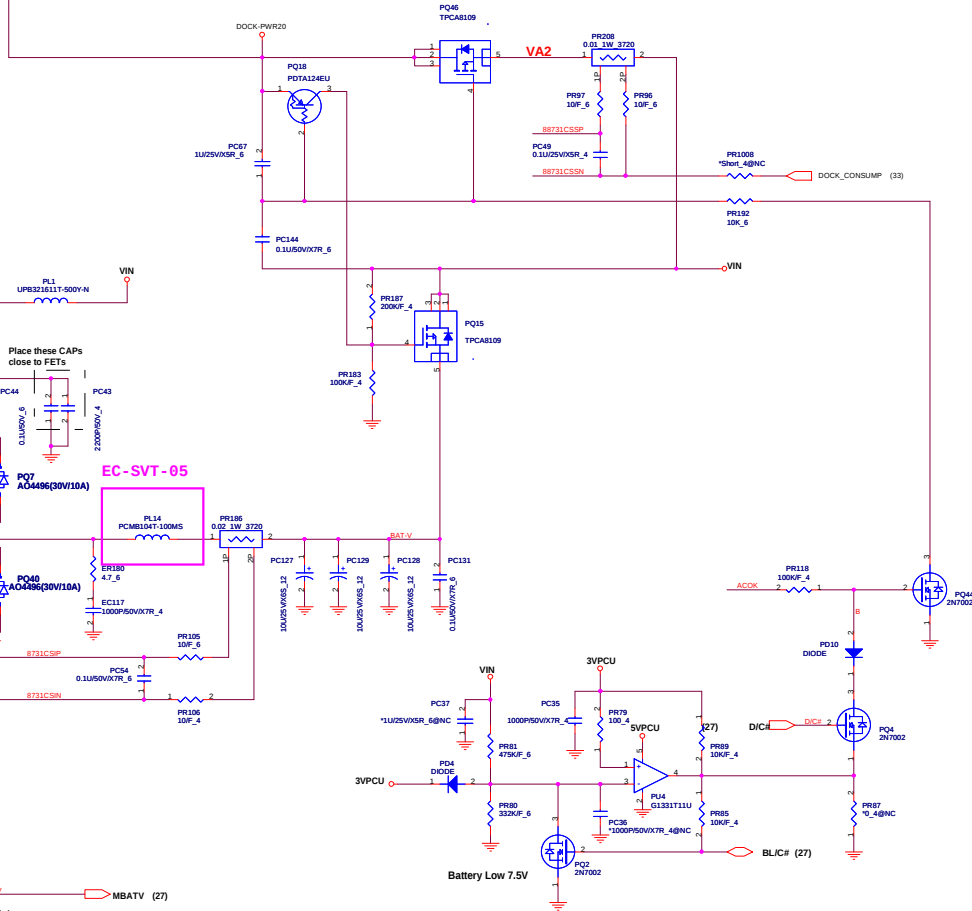
PROJECT :

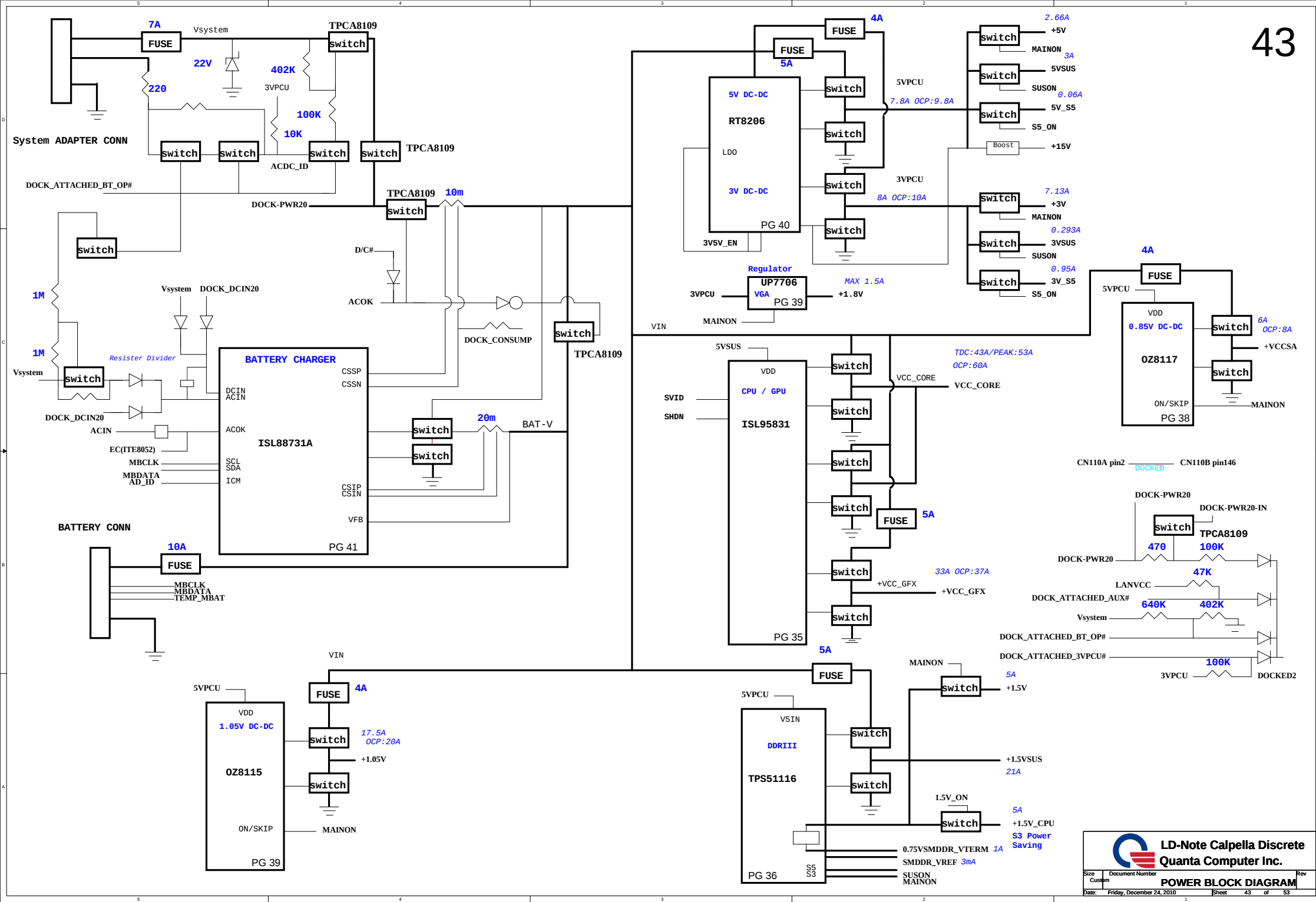
Size	Document Number	Rev
		1A

+1.05_PCH (OZ8115)

Date: Friday, December 24, 2010 Sheet 39 of 53







44

[illegible]

PCH JTAG Debug(CLG)

[illegible]

 Quanta Computer Inc. PROJECT : PD3	
Size	Document Number XDP
Date: Friday, December 24, 2010	Sheet 44 of 53

Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
1A		DV	Initial release		

Schematic Value Explanation Description :

RESISTOR

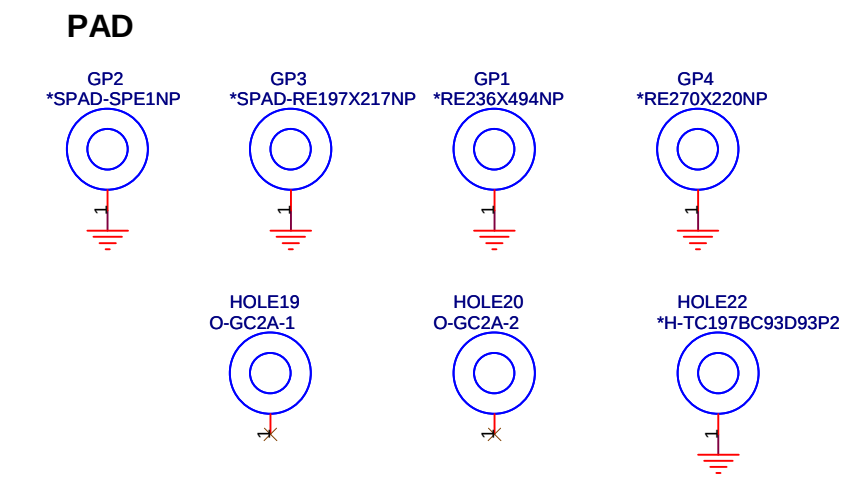
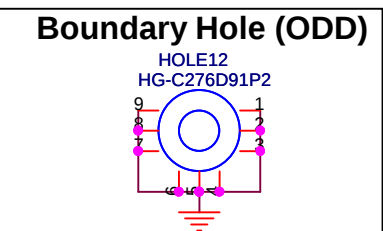
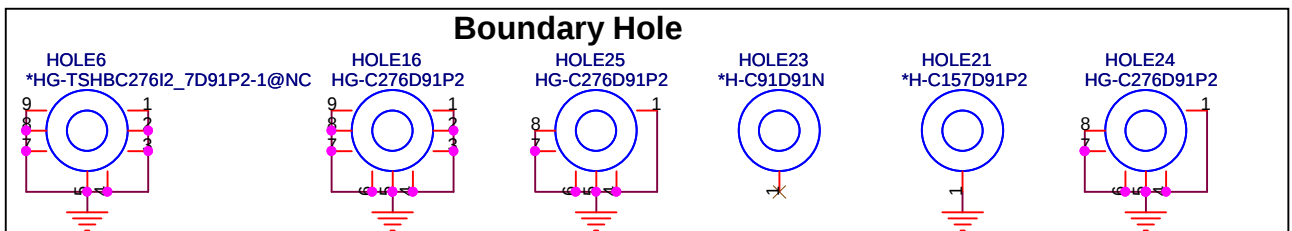
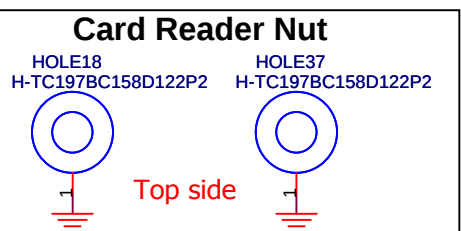
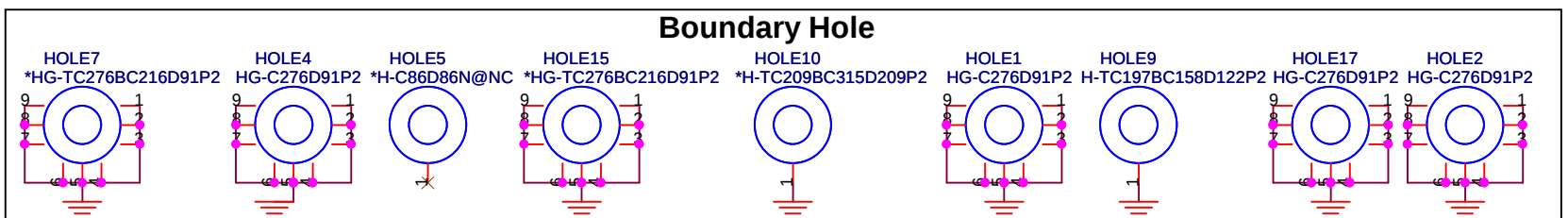
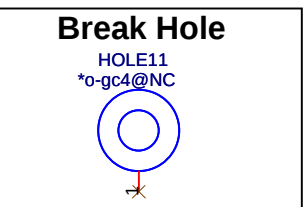
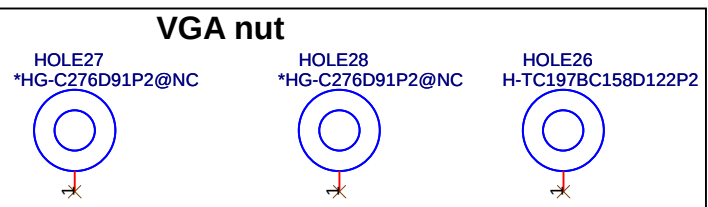
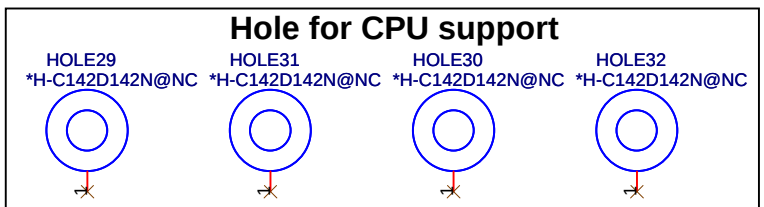
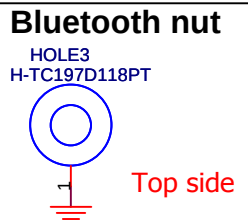
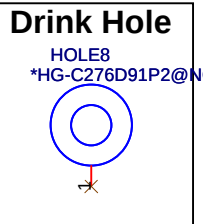
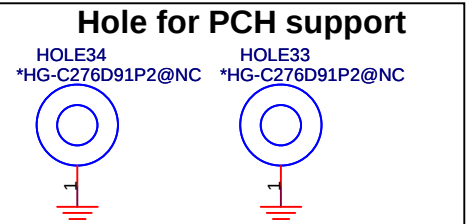
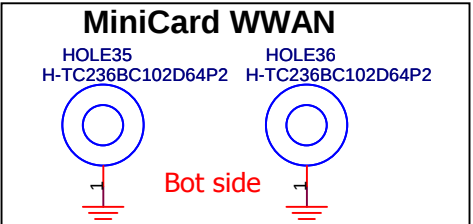
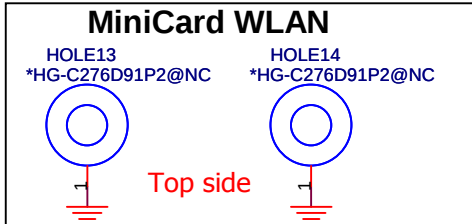
Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP

CAPACITOR

Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP



PROJECT: GC9A
Quanta Computer Inc.



[illegible]

2010	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
SDV~SIV	EC-A-01	27	07/05	U15,C135,C136,Y2	Change connection of MIC_MUTE_LED# and SPEAKER_MUTE_LED#, and reserved crystal for IT8518 per EC engineer request.
	EC-A-02	17	07/05	D20,D21,D22,D23, D24,D25,D26,D28, U10,U17	Change ESD protection component per ESD engineer request.
	EC-A-03	14	07/06	R9047,R9048, Q9000,Q9004	Add switch on SMBUS which connect to memory thermal sensor.
	EC-A-04	3,8	07/07	R390	Add connection to PROC_SELECT#
	EC-A-05	13	07/13	R8001	Alert pin have two pullup.R8001set no ASM.
	EC-A-06	18	07/21	R91,R87	NORAM loud beep fix
	EC-A-07	16	07/26	R1740	According to VESA DP interoperability guideline, R1740 value should be 5M or Larger for Dual-mode Device which support both Display port 1.1a and HDMI.
	EC-A-08	27	07/28	C127,R148	Change C127 to 0ohm, change R148 to 0ohm and not stuff for version B KBC(IT8518) per ITE fae suggestion.
	EC-A-09	27	07/28	C135,C136,Y2	Add crystal for EC
	EC-A-10	08	07/30	R9146,R8357	Remove redundant resistor R9146 and replace it by R8357 in PCH Strap Table
	EC-A-11	10	08/02	R9143,R9144, R8357	Remove R8456 and add pull high 10K resistor R9143,R9144 base on INTEL Design Guideline.
	EC-A-12	14	08/02	R8000,R8037	Change CPU FET/DDR3 thermal sensor to EMC1422-1-ACZL-TR which Local/Remote Thermal Shutdown Limit define by Hardware, for DMRB4, default Thermal Shutdown Limit value will be set on 105 degree celcius.
	EC-A-13	27	08/13	R129,Q24,CN37	Change PWR_LED# power rail to 3V_S5 and remove Q24 to prevent LED flash at the first time when insert adapter.
SIV~SIT	EC-B-01	07	09/06	R413	Power good:pull up 200ohm
	EC-B-02	21	09/06		ODD: reserve +5v path
	EC-B-03	18,27	09/06	R184,R192,D18, D19,R376,R375	Audio :change HP jack in circuit for realtek/lenovo recommend Add: R184,R192,D18,D19,R376 Delete: R375
	EC-B-04	15	09/06	CN3,CN13	Merge LCD+Camera connector same as DMRB3.
	EC-B-05	27	09/06		Correct the netname from H_PROCHOT#_EC to H_PROCHOT_EC which cause wrong define on EC setting and result of slow system issue.
	EC-B-06	27	09/06		Correct the netname assign of SUSON and S5_ON
	EC-B-07	03	09/09	U8250	Change U8250 to 74AHC1G09(OD AND gate)
	EC-B-08	24	09/09	CN27	Add AT3.0 hook connection to WWAN connector
	EC-B-09	44	09/27		Change PCH XDP signal pull up power rail from 3VPCU to 3V_S5 according to Intel CRB (Huron River Platform Emerald Lake Revision 1.0 June 2010)
	EC-B-10	07	09/28	R8292	Change connection to RSMRST# due to GC89E do not support the Deep Sx state.
	EC-B-11	16,17, 20,22, 23	09/28	C10,C1411,R45,R46, RV4,U1600, U1900, U2300,U3,U26,U27, U48,U49,C173,	Add for ESD
	EC-B-12	26	09/30	Q5	Change Q5 to 2SK3018 from DTC115
	EC-B-13	7	09/30	R8486,R8342	Add WWAN detection circuit
	EC-B-14	8,9, 20	09/30	C135,C136,C8360, C8362,C8388, C8389	Fine tune crystal shunt capacitance Y2(C135=C136=10pF),Y8200(C8360=C8362=15pF),Y8202(C8388,C8389=27pF),Y1 no need modify
	EC-B-15	22	1005	C56,C9222,R630,U53	Change from AUO3 to AUO4(TPS2254)



Quanta Computer Inc.
PROJECT : DM4/RB4

Size	Document Number	Rev
	KBC IT8518/19	1A
Date:	Friday, December 24, 2010	Sheet 48 of 53

2010	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
	EC-B-16	24	10/06	R8549,R8550, R8551	Add 0ohm optional resistor on AT 3.0 hook signals connection.
	EC-B-17	7,8, 11	10/06	R8345,R8393,R8503, R8509,R8341	GC89E didn't support DSW function,change some power rail to non-DSW power.
SIT~SVT	EC-C-01	10	12/06		Add GPIO 39 Dock w/,w/o for Assembly request
	EC-C-02	20	12/06	R8355,R8356,RV8,RV9	ESD team recommend
	EC-C-03	20	12/06	C173	Final solution from ESD,EMI and safety team.
	EC-C-04	27	12/06		Solve issue ODD Drive LED turn on once at Battery pack plugged, change ODD_5V_ON connection from GPIO#86 to GCPIO#98.
	EC-C-05	3	12/06	C8237	Add 0.1u cap for +1.5VCPU per ESD request.
	EC-C-06				Cancel this EC
	EC-C-07	10,24 ,27	12/09	R8331,R638,R8023	Modify for mSATA and WWAN exclusive support design
	EC-C-08	20,27	12/16		Connect U15 pin120 to RJ45_LINKUP# for LAN cable detection under S5 state
	EC-C-09	3,5,7, 8,9, 10,11, 13,14, 18,24, 25,27, 33 34	12/17	R8222,R8225,R8254, R648,R8566,R8291, R8292,R8294,R8295, R8296,R8297,R8298, R8301,R8303,R8344, R8393,R9023,R8564, R7061,R8238,R9141, R8500,R8503,R8504, R8506,R8507,R8510, R8511,R8513,R8514, R8519,R8522,R8523, R8524,R8525,R8526, R8528,R8529,R8530, R8531,R8532,R8533, R8534,R8538,R8542, R8546,R8002,R8022, L17,R629,R635,R636, R644,R8549,R8550,R8551, R309,R318,R319,R320, R321,R322,R323,R324, R325,R478,R9262,R362, R365,R377,R378	Change 0 ohm to shortpad.
	EC-C-10	5,11	12/21	C8541,C8542,C8543,RV10, RV11,RV12,RV13,RV14	Reserve 0.1u and 0402 TVS space for ESD



Quanta Computer Inc.
PROJECT : DM4/RB4

Size	Document Number	Rev
	KBC IT8518/19	1A
Date:	Friday, December 24, 2010	Sheet 49 of 53

2010	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
	EC-C-11	27	12/24	R123,R124	Change power rail from 3VPCU to 3V_S5
	EC-C-12	18	12/24	C45	Change from 2.2u to 1u to solve pop noise when resume from S3
	EC-C-13	11,16	12/24	RV15,C8460,C8465,C8466, C8467,C8468,C8469, C8470,C1412	Add for ESD display port CDE solution.
SIT~SVT					



Quanta Computer Inc.
PROJECT : DM4/RB4

Size	Document Number	Rev
	KBC IT8518/19	1A
Date:	Friday, December 24, 2010	Sheet 50 of 53

EC NO	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-P-01	35	7/6	PR7007	change from 2.37K to 2.32K
EC-P-02	35	7/6	PR9059	change from 27.4K to NC(*)
EC-P-03	35	7/6	PC9058	change from 0.068u to 0.022u
EC-P-04	35	7/6	PC9059	change from 0.068u to 0.015u
EC-P-05	41	7/6	PR107	change from 10K to 4.7K
EC-P-06	36	8/17	PQ82	change to NC(*) for S3 issue
EC-P-07	38	8/17		change 5VPCU to 3VPCU for 0Z8117 new version
EC-P-08	40	9/7	PC192	change to NC(*)
EC-P-09	39	9/7	PR278,PR282	change PR278 to 12.7K,change PR282 to 10K for +1.8V ripple
EC-P-10	39	9/7	PR9170	change PR9170 to 51.1K for +1.05V regulation
EC-P-11	39	9/7	PL12	change PL12 to 1uH for +1.05V ripple
EC-P-12	39	9/7	PR9166	change PR9166 to 97.6K for +1.05V OCP
EC-P-13	39	9/7	PC9142	change PC9142 to 4700pF for +1.05V transient
EC-P-14	38	9/7	PR9130	change PR9130 to 2.2ohm for +VCCSA Ringing voltage
EC-P-15	38	9/7	ER9133,EC9114	Add ER9133 to 4.7ohm and add EC9114 to 1000pF for +VCCSA Ringing voltage
EC-P-16	36	9/7	PR124	Change PR124 to 10K for 1.5V regulation
EC-P-17	38	9/7	PR9137	Change PR9137 to 78.7K for +VCCSA OCP
EC-P-18	36	9/7	PR122	Change PR122 to 4.53K for 1.5V OCP
EC-P-19	40	9/7	PR255	Change PR255 to 267K for 3VPCU OCP
EC-P-20	40	9/7	PR262	Change PR262 to 249K for 5VPCU OCP
EC-P-21	36	9/8	PR9245	S3 Function Modify
EC-P-22	35	9/8		Change for CPU transient quality
EC-P-23	35	9/8		Change for GFX transient quality



Quanta Computer Inc.
PROJECT : DM4/RB4

Size	Document Number	Rev
	EC	1A
Date:	Friday, December 24, 2010	Sheet 51 of 53

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-SIT-01	35	9/28	PR9049,PR9050 PR28,PR29 PR30,PR19 PR20,PR152 PR153,PR15 PR13,PR22 PR26,PR9055	change to short-pad
	36	9/28	PR195,PR207 PR196,PR199 PR200,PR125	change to short-pad
	38	9/28	PR9129,PR9136 PR9145,PR9239	change to short-pad
	39	9/28	PR9160,PR9168 PR274,PR9163 PR9157	change to short-pad
	40	9/28	PR270,PR250 PR263,PR261 PR256,PR285 PR249,PR260	change to short-pad
	41	9/28	PR1008,PR113 PR111,PR108	change to short-pad
EC-SIT-02	42	9/28	PR9228,PC9190 PQ9050,PR9227 PQ9051,PD32	change to NC for HW request
EC-SIT-03	38	9/28	PR9139,PR9140	Reduce leakage current
EC-SIT-04	35	10/1	PR9053,PR2,PR3	Intel VBoot setting to 0V request



Quanta Computer Inc.
PROJECT : DM4/RB4

Size	Document Number	Rev
	EC	1A
Date:	Friday, December 24, 2010	Sheet 52 of 53

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-SVT-01	35	11/24	PR9053 PR9054	change PR9053 to 1.69K for CPU Iccmax change PR9054 to 24.9K for CPU Iccmax
EC-SVT-02	35	11/30	PR9069	change PR9069 to 27.4K for when Iccmax=53A Vimon can within 2.7V
EC-SVT-03	39	11/30	PU11 PR281	change PU11 to UP0104PSU8 change PR281 to 0hm for HW requrest
EC-SVT-04	35	12/10	PC103 PC9201 PR9246	change PC103 to 330uF,change PC9201 to 330pF,change PR9246 to 20k for GFX OVP issue
EC-SVT-05	35 36 38 39 40 41	12/21	PL8,PL9,PL10, PL15,PL12,PL1006 PL19,PL20 PL14	DC to CV inductor p/n change



Quanta Computer Inc.
PROJECT : DM4/RB4

Size	Document Number	Rev
	EC	1A
Date:	Friday, December 24, 2010	Sheet 53 of 53