POWER PAVILION PUFF INTEL SKL / KABY -H SYSTEM DIAGRAM

01

Charge PG.40
DDR4 PG.42
CPU Core PG.43~45
+1.0V/+1.2VSUS PG.47~48
+3V/+5V S5 PG.41
+VGACORE PG.49
+1.35V_GFX PG.50

Config#3 SODIMM 1DPC

SODIMM1 Max. 8GB STD PG.17 — DDR4 2133MHz — Channel A
SODIMM2 Max. 8GB RSV PG.18 — DDR4 2133MHz — Channel B

INTEL
SkyLake - H4+2
Kaby Lake - H4+2
Processor : Quad Core
Power : 45 (Watt)
Package : BGA1440
Size : 42 x 28 (mm)
Die Size : 13.6 x 9.1 (mm)
PG.2~8

PEG X8 Lane — NVIDIA N16P-GX / N16E-GR
Package 29 x 29mm
40W PG.19~23
27MHz PAGE 21
VRAM gDDR5 x 4pcs 128M x32 / 256M x32 2.5GHz PG.14~25
HDMI v2.0 PG.27
eDP (5.4Gb/s) eDP — 17" eDP Panel HD/FHD/UHD PG.26

DMI

INTEL PCH
Lynx Point
Power : Watt
Package : FCBGA837
Size : 23 x 23 (mm)
PG.9~16

M.2 2280-S3 SSD PG.33 — SATA0 6GB/s SATA0A; PCIEx4 32GB/s LANE9,10,11,12
HDD PG.32 — SATA0 6GB/s SATA1B

USB 3.0
PORT1 — USB 3.0 Ports PG.30
PORT2 — USB 3.0 Ports (DB) PG.30
PORT4 — USB3.0 Re-Driving IC PTN36241G PG.31 — 3D Camera Intel F200 3D PG.31

USB 2.0
PORT3 — USB 2.0 Ports (DB) PG.30
PORT4 — HD CAM PG.26
PORT5 — HD + IR CAM (OPTION) PG.26,34
PORT8 — Touch Screen Synaptics S7817 PG.26

PCI-E x 1 Gen1
LANE7 — LAN RTL8107ESH/ 10/100 RTL8111HSH/ Gbe PG.35
LANE5 — Card Reader RTS5237S-GR PG.36
LANE6 — WLAN BT COMBO PG.33
USB 2.0 PORT7

SPI — ROM PG.12
G-Sensor HP2DC PG.34
SMBUS
LPC — KBC ITE IT8987E/BX PG.37
LPC
TPM 2.0 SLB9665TT2.0 (OPTION) PG.34
KB PG.38
TP PG.38
FAN PG.38

Azalia — AUDIO CODEC ALC3258-CG PG.28
Headphone amplifier HPA0022642RTJR PG.29 — Hp / MIC — Combo Jack (DB) PG.30
Speaker PG.28
Dual Digital MIC PG.28
3D CAM MIC INT CAM MIC PG.26

STACKUP
TOP
GND
IN1
IN2
VCC
IN3
GND
BOT

PROJECT : G35
Quanta Computer Inc.

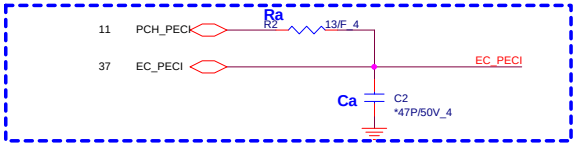
Size	Document Number	Rev
Custom	01 -- Block Diagram	1A

Date: Tuesday, December 01, 2015 | Sheet 1 of 51

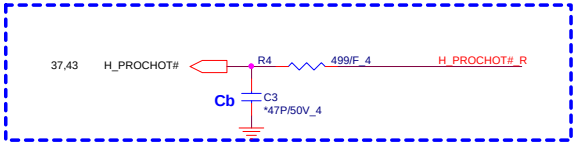
SKYLAKE Processor (CLK,MISC,JTAG)

02

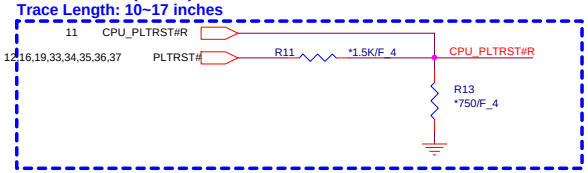
H_PECI (50ohm)
Trace Length: <0.5 iches
Ra,Ca need placement close to PCH.



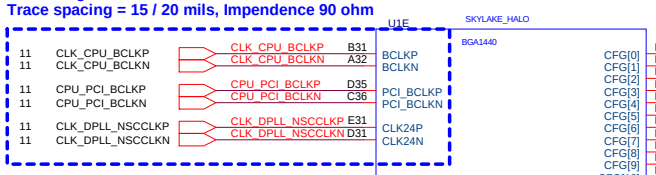
PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placment near VR

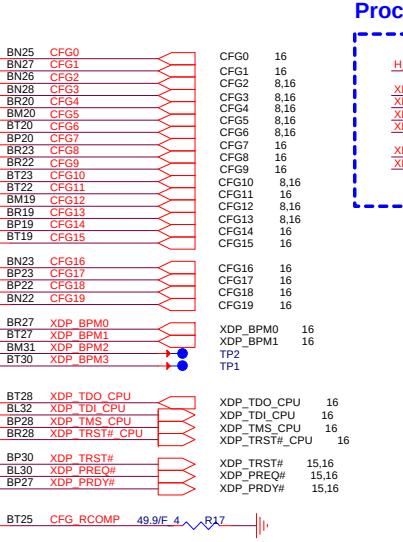


CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



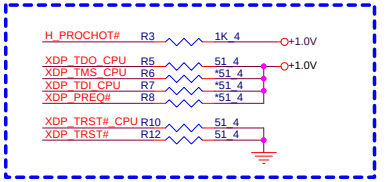
Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 90 ohm





Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

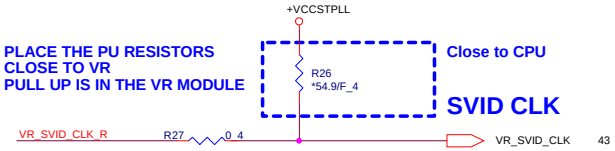
Processor pull-up (CPU)



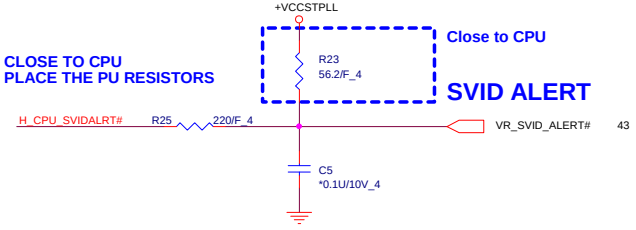
PM_SYNC (50ohm)
Trace Length: 1~11.25 inches

CPU CORE SVID
Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

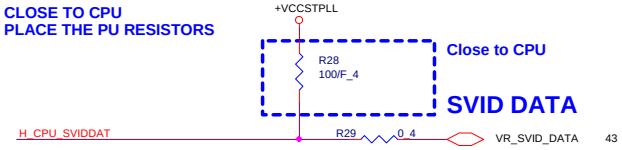
PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE



CLOSE TO CPU
PLACE THE PU RESISTORS

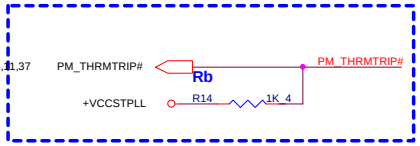


CLOSE TO CPU
PLACE THE PU RESISTORS

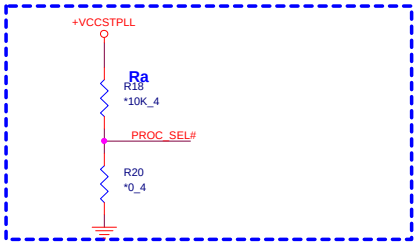


PROCPWRGD (50ohm)
Trace Length: 1~11.25 inches

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
Rb need placment near PCH

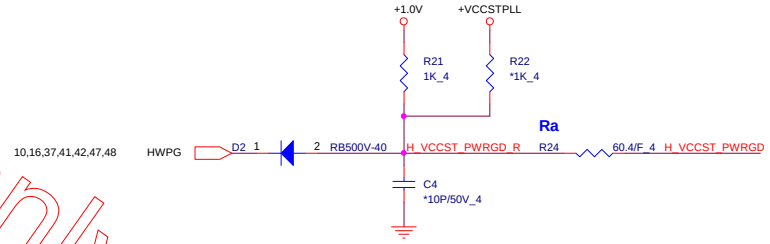


Ra(R10804) Not install in SKL-H



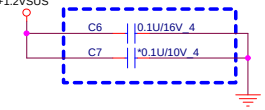
HWPD

Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A

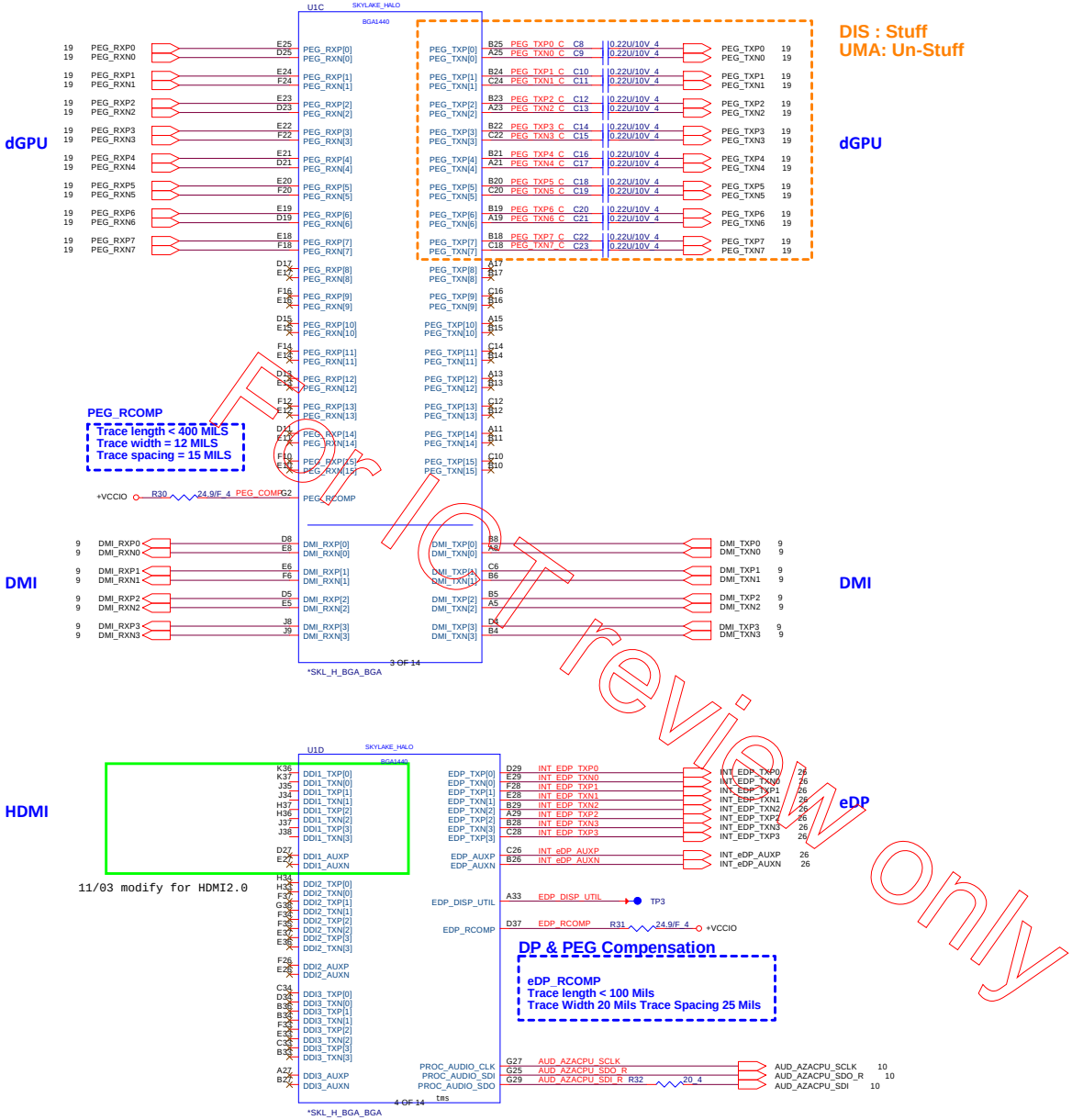


PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 -- SKL 1/7 (JTAG/MISC)	1A
Date: Monday, November 30, 2015	Sheet 2 of 51	

SKYLAKE Processor (DMI,PEG,FDI)

03



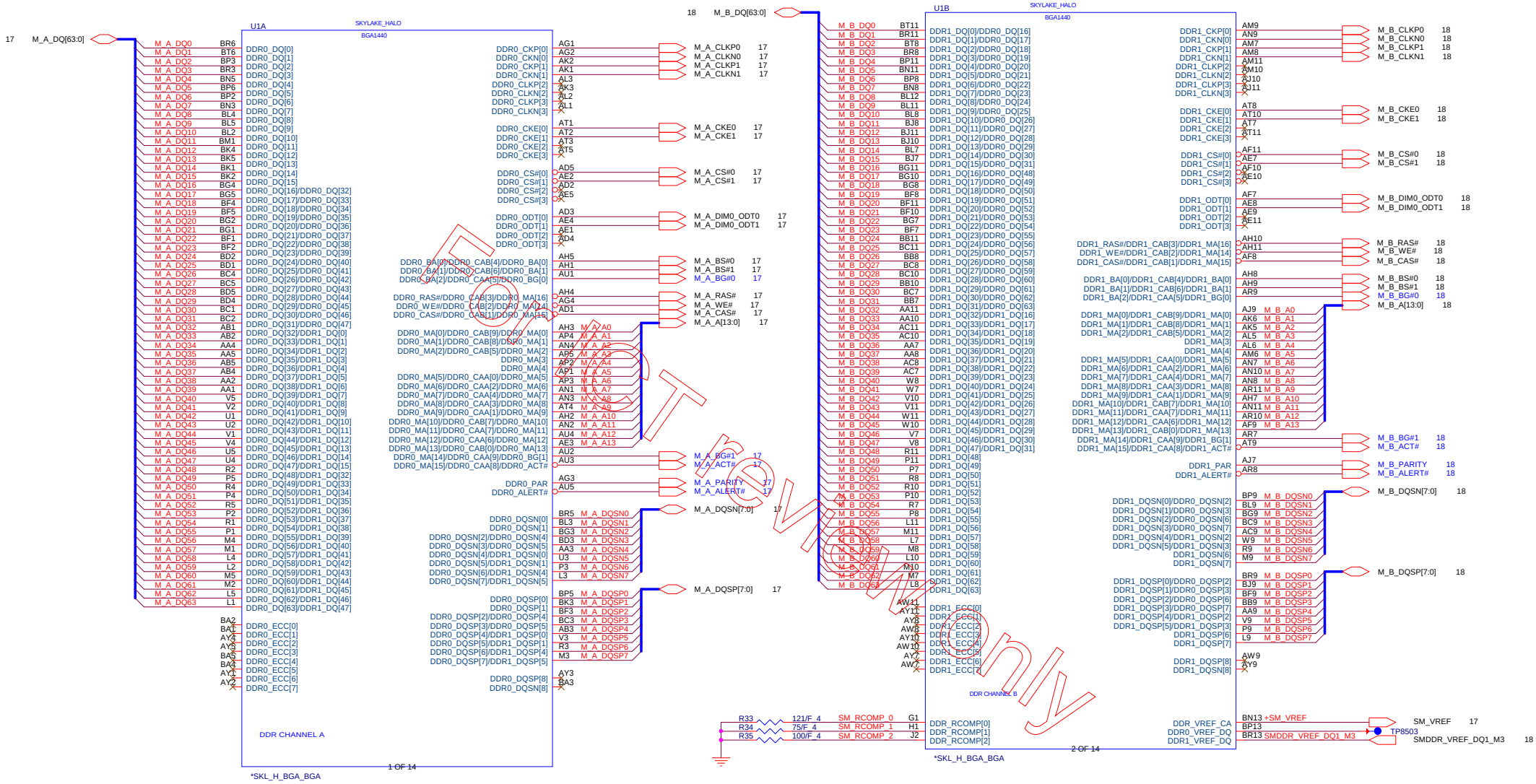
+1.2VSUS 2,6,10,17,18,42,48,51
+3VS5 10,12,14,16,26,33,37,41,42,46,
+3V 5,9,10,11,12,13,14,16,17,18,19,22,

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	03 – SKL 2/7 (DMI/EDP/PEG)	1A

Date: Tuesday, December 01, 2015 | Sheet 3 of 51

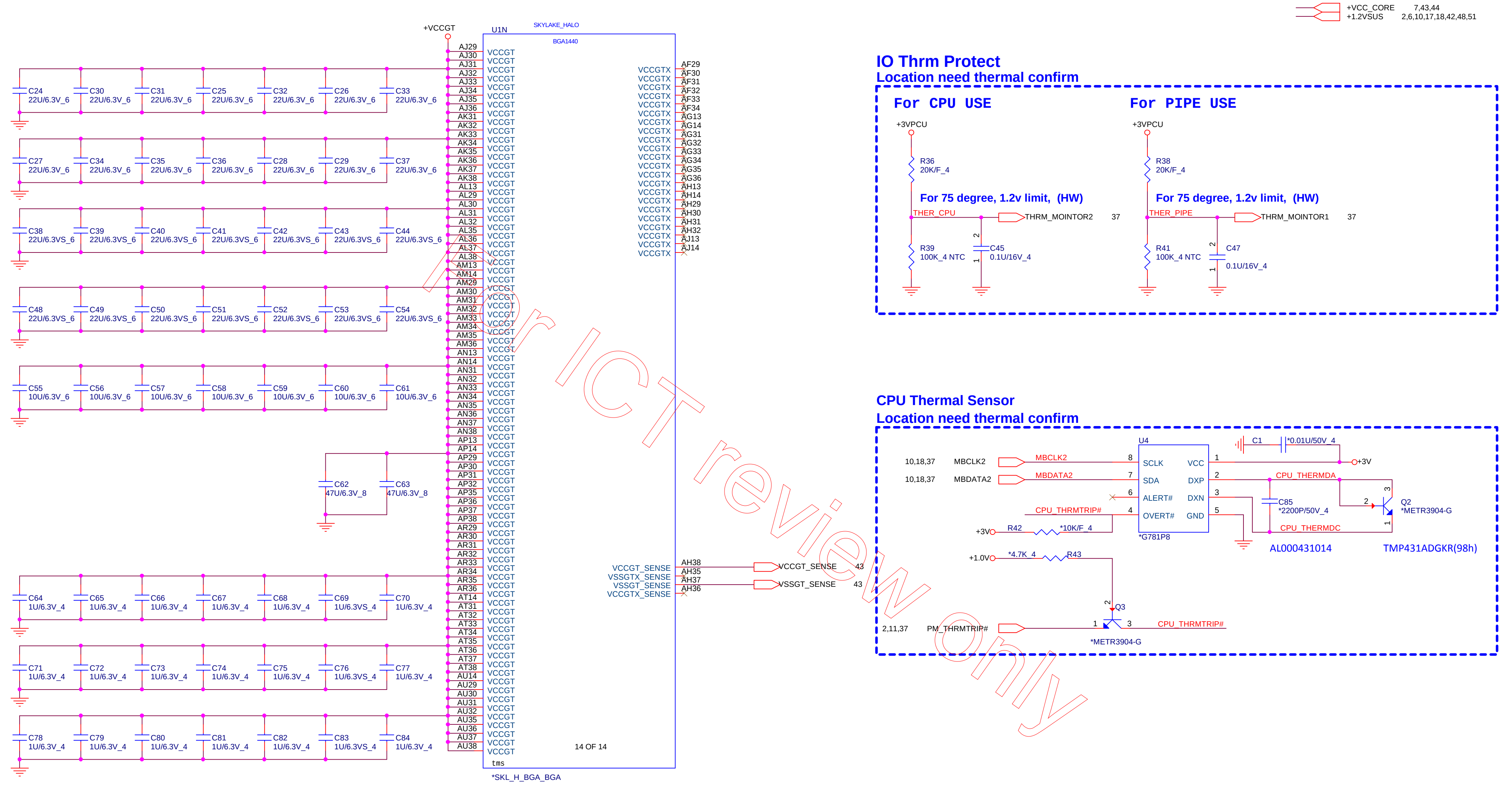
SKYLAKE Processor (DDR4)



PROJECT : G35		
Quanta Computer Inc.		
Size: Custom	Document Number: 04 -- SKL 3/7 (DDR4 I/F)	Rev: 1A
Date: Monday, November 30, 2015	Sheet 4 of 51	

SKYLAKE Processor (POWER)

Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A



PROJECT : G35

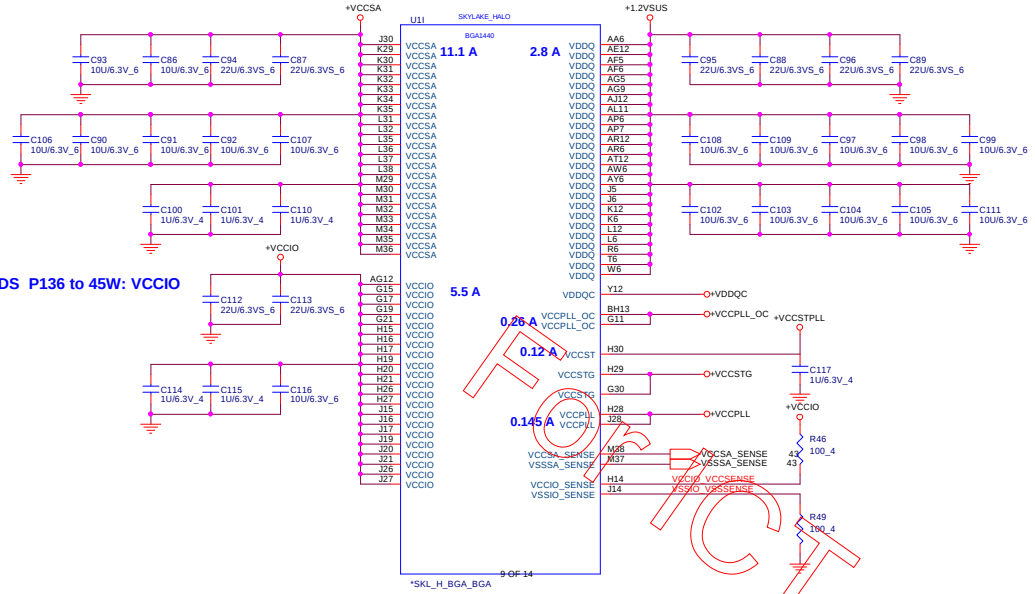
Quanta Computer Inc.

Size	Document Number	Rev
Custom	05 -- SKL 4/7 (POWER)	1A

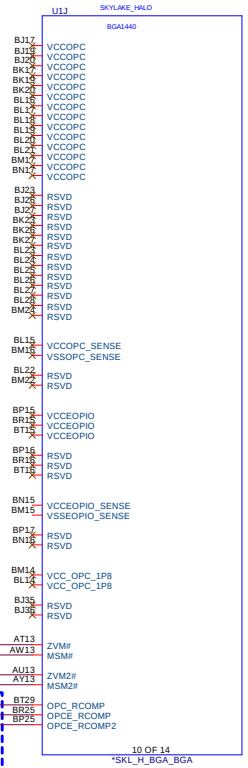
Date: Tuesday, December 01, 2015 Sheet 5 of 51

Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A

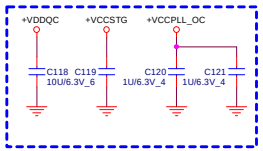
Follow SKL H EDS page 135 45W: VDDQ=2.8A



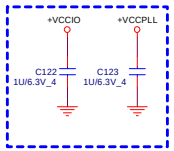
Follow SKL H EDS P136 to 45W: VCCIO
+VCCIO = 0.95V

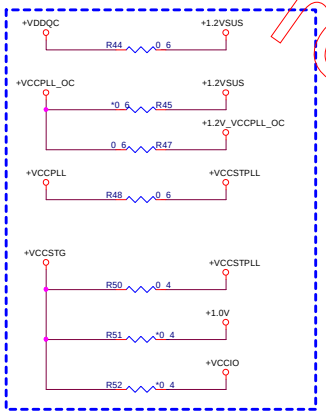


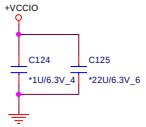
Under CPU

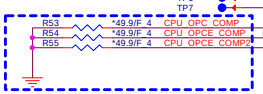


Close CPU



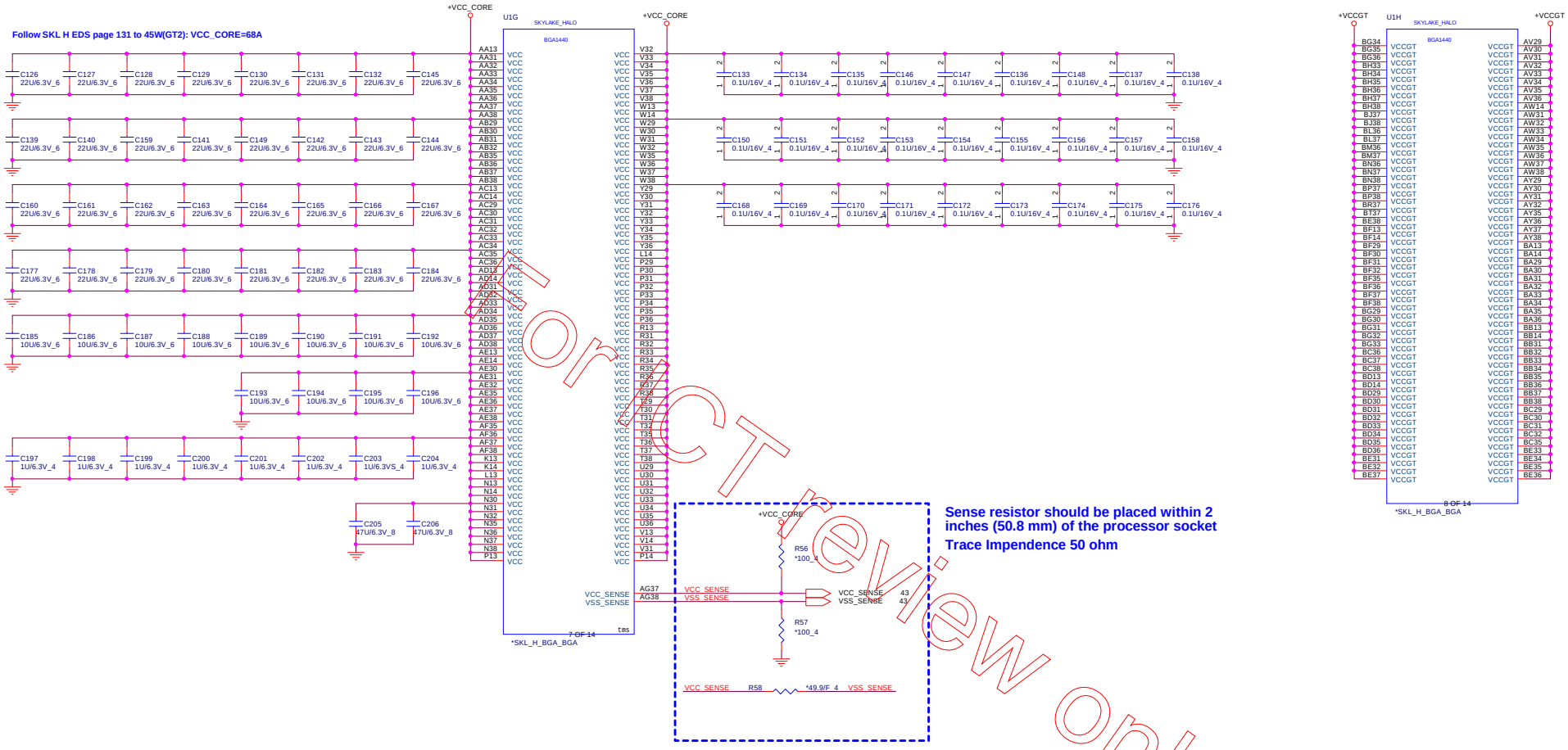






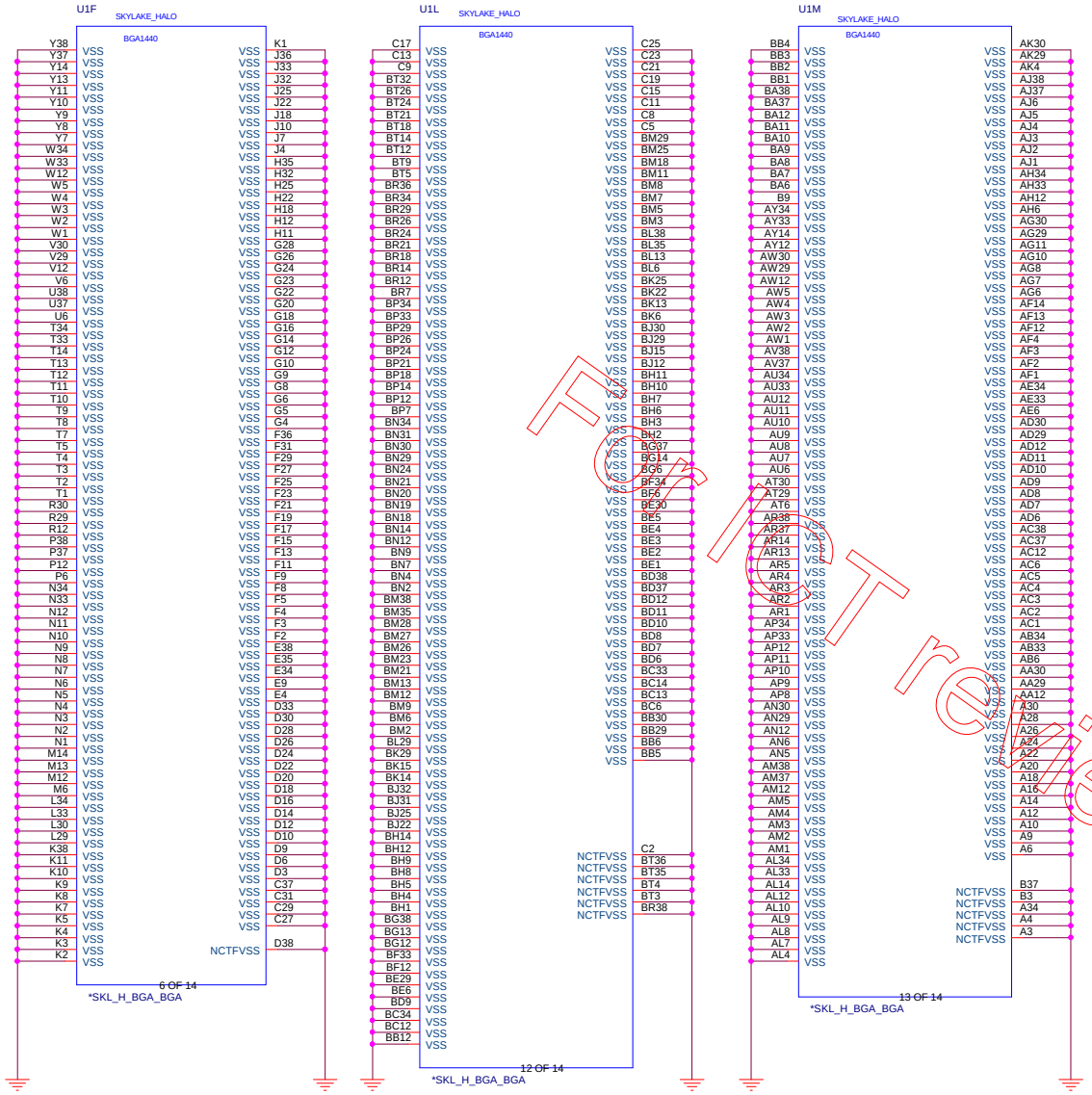
Unconnected for Processors without OPC.

Quanta Computer Inc.	PROJECT : G35		
Size: Custom	Document Number: 06 – SKL 5/7 (POWER&GND)		Rev: 1A
Date: Monday, November 30, 2015	Sheet 6 of 51		

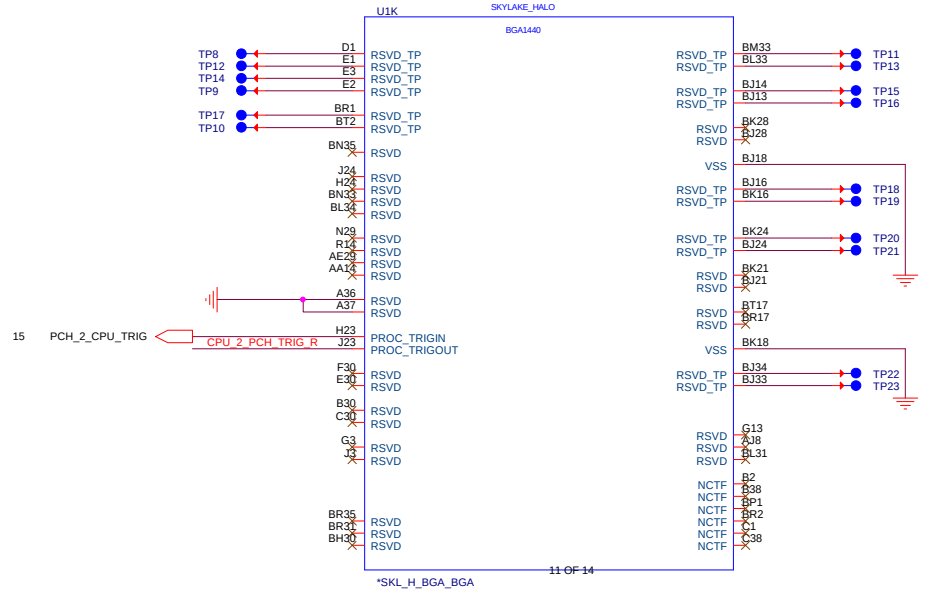


PROJECT : G35 Quanta Computer Inc.		
Size: Custom	Document Number: 07 -- SKL 6/7 (POWER&GND)	Rev: 1A
Date: Tuesday, December 01, 2015	Sheet 7 of 51	

SKL-HProcessor (GND)



SKL-H Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

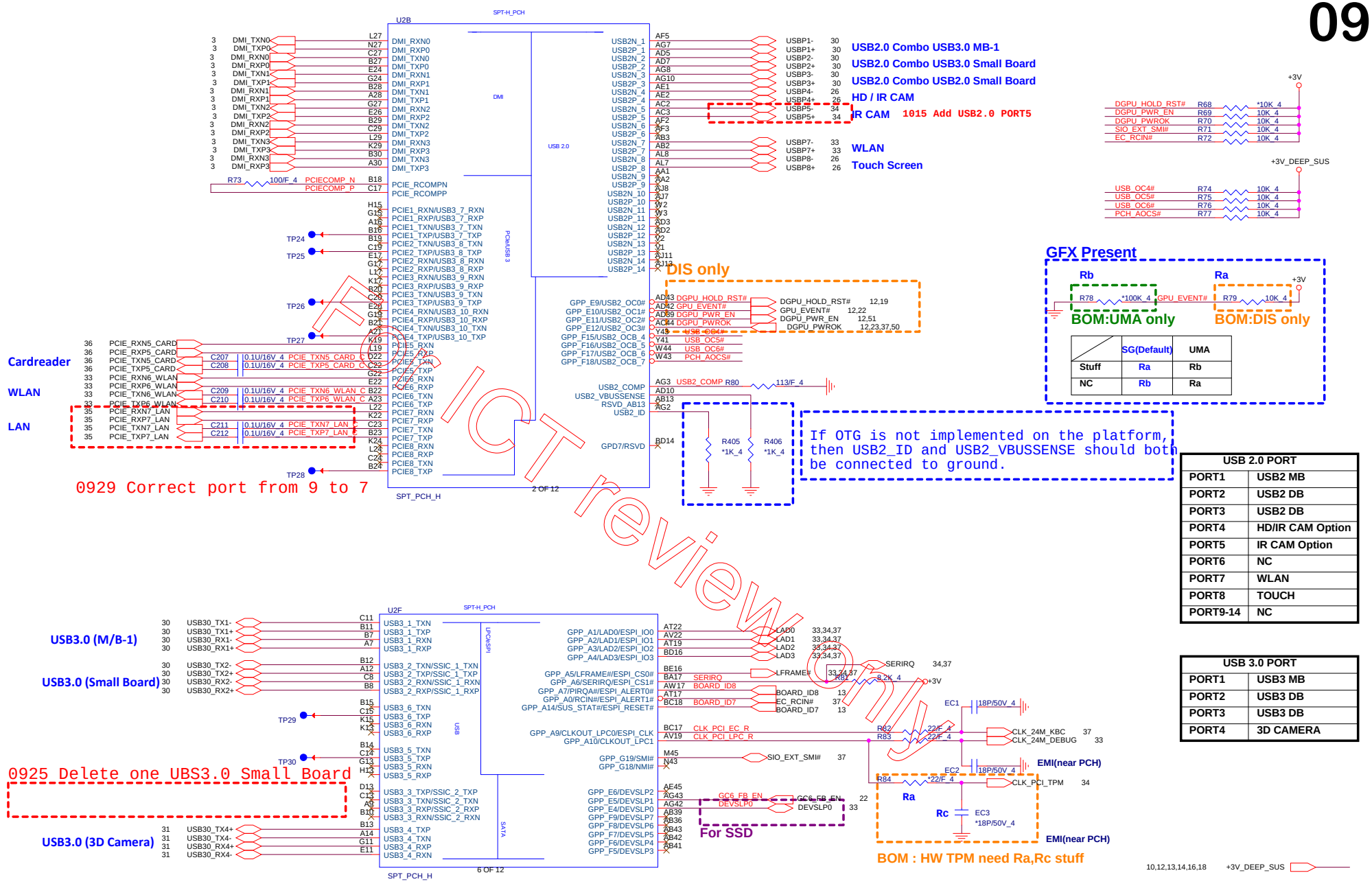
2,16	CFG3	CFG3	R60	*1K_4
2,16	CFG2	CFG2	R61	*1K_4
2,16	CFG4	CFG4	R62	1K_4
2,16	CFG5	CFG5	R63	*1K_4
2,16	CFG6	CFG6	R64	*1K_4
2,16	CFG10	CFG10	R65	*1K_4
2,16	CFG12	CFG12	R66	*1K_4
2,16	CFG13	CFG13	R67	*1K_4

PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
Custom	08 -- SKL 7/7 (GND)	1A

Date: Monday, November 30, 2015 | Sheet 8 of 51



USB 2.0 PORT	
PORT1	USB2 MB
PORT2	USB2 DB
PORT3	USB2 DB
PORT4	HD/IR CAM Option
PORT5	IR CAM Option
PORT6	NC
PORT7	WLAN
PORT8	TOUCH
PORT9-14	NC

USB 3.0 PORT	
PORT1	USB3 MB
PORT2	USB3 DB
PORT3	USB3 DB
PORT4	3D CAMERA

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	09 -- PCH 1/7 (DMI/USB/PCIE)	1A

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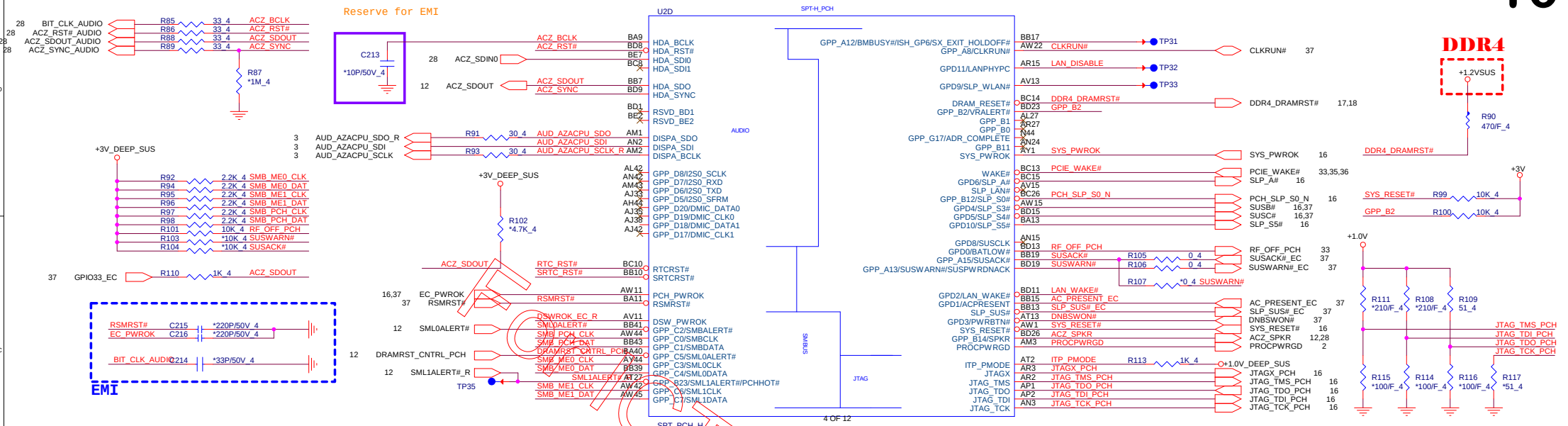
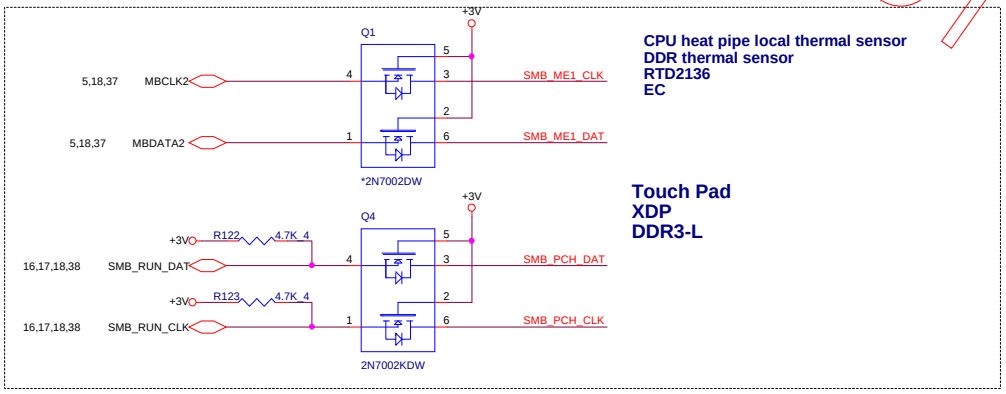
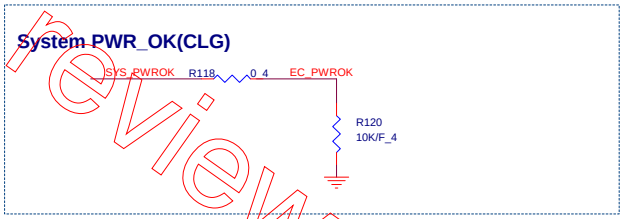
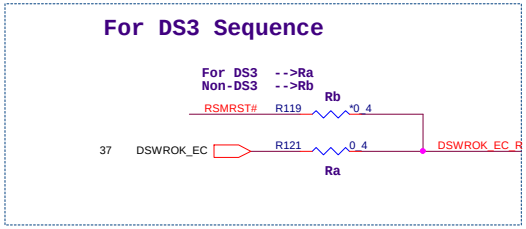
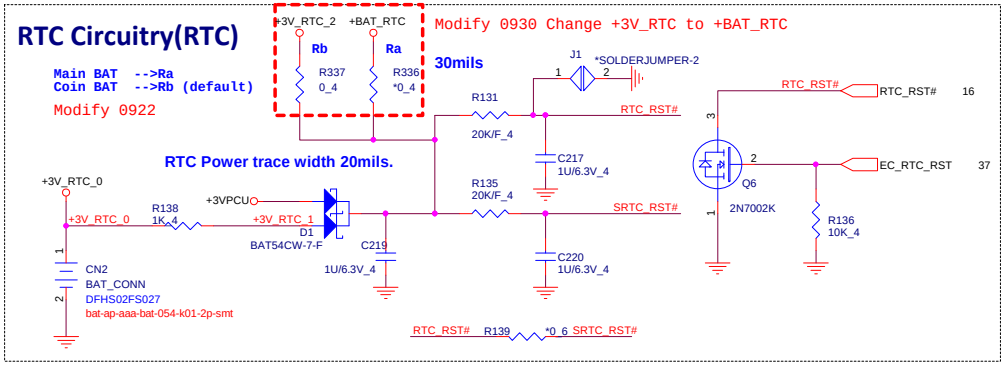
HDA Bus(CLG)

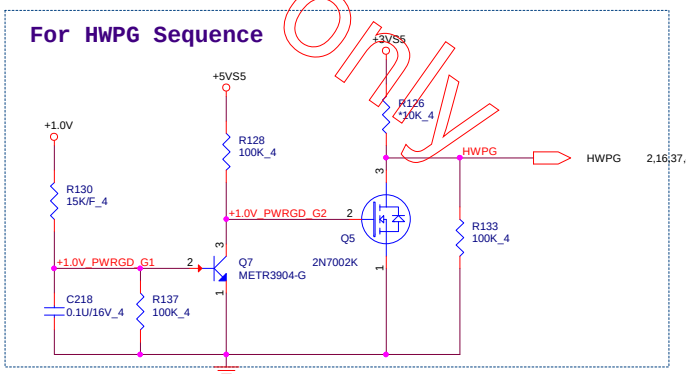


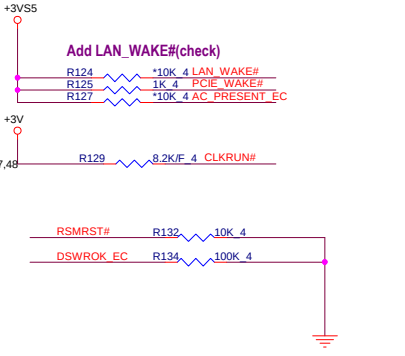












9,12,13,14,16,18 +3V_DEEP_SUS

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- PCH 2/7 (HDA/SMBUS)	1A
Date: Monday, November 30, 2015	Sheet 10 of 51	

HSIO MUX PORT	
PCIE1-4	NC
PCIE5	Cardreader
PCIE6	Wlan
PCIE7	Lan
PCIE8	NC
PCIE9/SATA0A	SSD PCIE * 4
PCIE10	
PCIE11	
PCIE12	
PCIE13	NC
PCIE14	NC
PCIE15	HDD
PCIE16	NC
PCIE17	NC
PCIE18-20	NC

SSD PCIE x4 LANE

Modify 1005 Change HDD SATA Port2 to port1B

HDD1 (SATA1B 6Gb/s)

SSD PCIE x4 LANE

SSD PCIE x4 LANE

SSD PCIE x4 LANE

ODD (SATA2 3.0Gb/s)

HDD2 (SATA3 6Gb/s)

GPIO35:
SSD SATA IF => High
SSD PCIE IF => Low

For SSD Det (SATA0A)

1002 add

BOM:SSD only

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H
needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.

1123 Change Y1 P/N from 16pF to 20pF

Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out:4-10 mil Wide GND Shield Trace

RTC Clock 32.768KHz

32.768KHz
BG332768453 CRYSTAL SMD 32.768KHZ(+-20PPM,12.5PF)
footprint: xtl-3_2X1_5-2_5-0_8h

Card Reader

WLAN

LAN

VGA

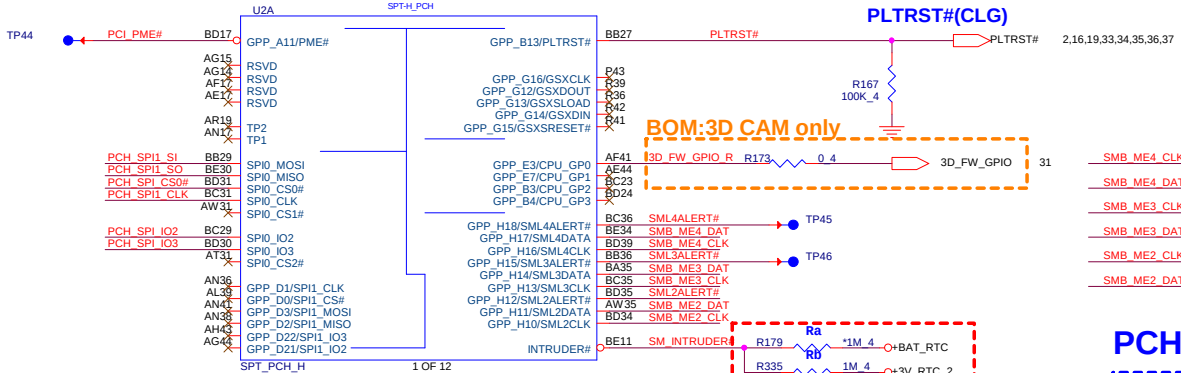
SSD

BOM:DIS only

BOM:SSD only

PROJECT : G35
Quanta Computer Inc.

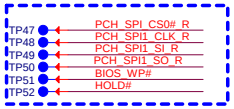
Size	Document Number	Rev
Custom	11 – PCH 3/7 (SATA/LPC/CLK)	1A
Date: Monday, November 30, 2015	Sheet 11 of 51	



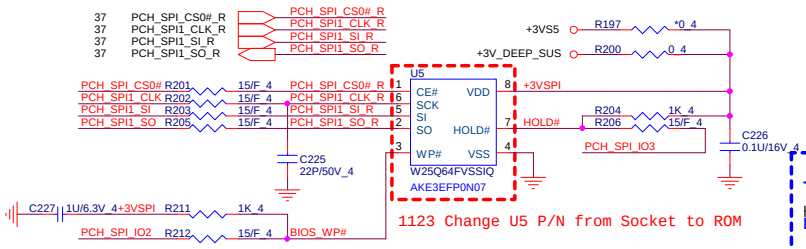
support HW TPM -->Ra
support SW TPM -->Rb (default)

Modify 0930 Change +3V_RTC to +BAT_RTC

PCH SPI ROM(CLG)



Place to TOP

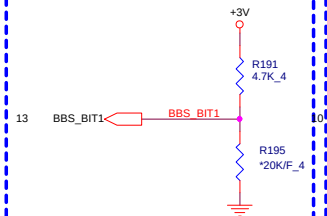


1123 Change U5 P/N from Socket to ROM

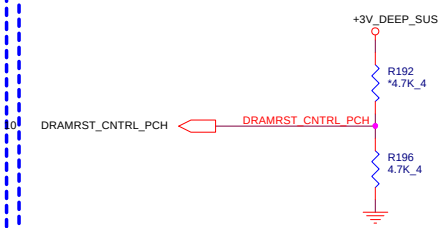
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

PCH Strap Pin

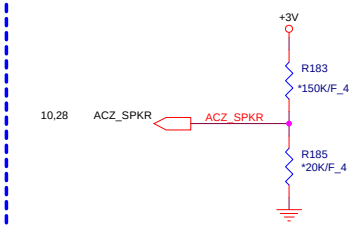
NO REBOOT IF SAMPLED HIGH
HIGH:TOP SWAP ENABLED (CRB)
LOW: Disable "No Reboot" mode. (Default)



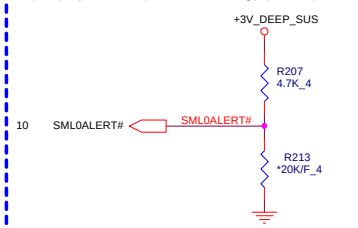
ESPI/LPC SELECT STRAP
HIGH:eSPI Is selected for EC.
LOW: LPC Is selected for EC. (Default)



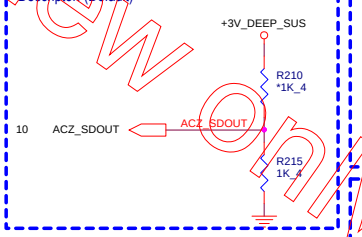
TOP SWAP OVERRIDE STRAP
HIGH:TOP SWAP ENABLED (CRB)
LOW:TOP SWAP DISABLED(DEFAULT)



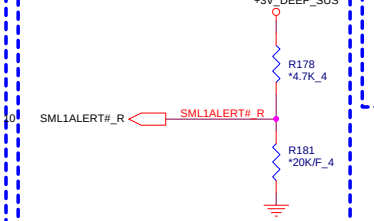
TLS CONFIDENTIALITY ENABLED
HIGH:T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)



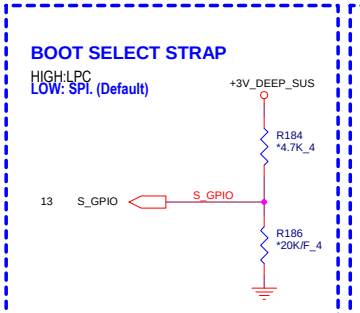
TLS CONFIDENTIALITY ENABLED
HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.(CRB)
LOW: security measures defined in the Flash Descriptor. (Default)



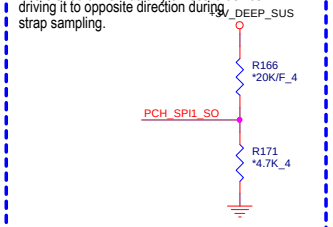
RESERVED
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



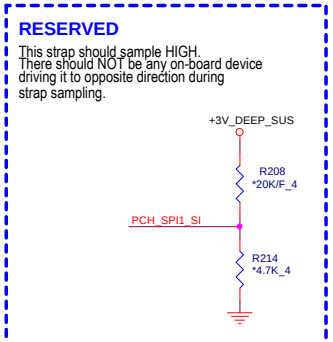
BOOT SELECT STRAP
HIGH:LPC
LOW: SPI. (Default)



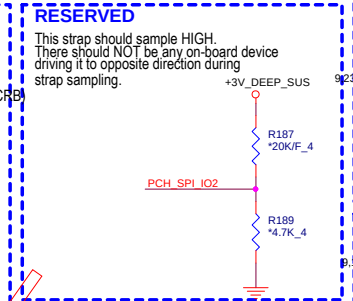
RESERVED
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



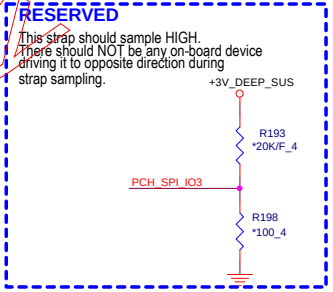
RESERVED
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



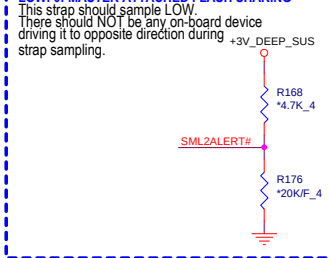
RESERVED
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



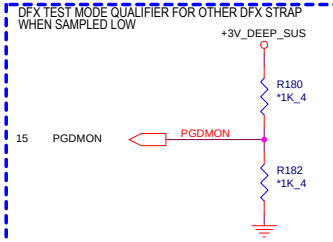
RESERVED
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



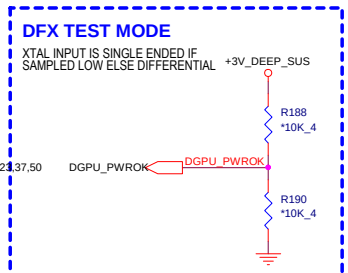
ESPI FLASH SHARING MODE
HIGH:SLAVE ATTACEHD FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



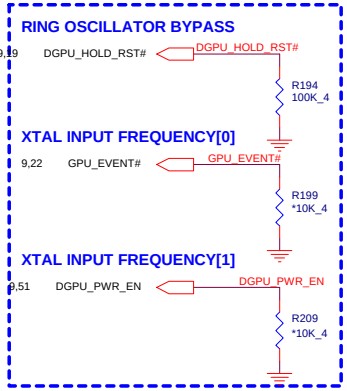
DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP WHEN SAMPLED LOW



DFX TEST MODE
XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL



RING OSCILLATOR BYPASS



PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	12 -- PCH 4/7 (GPIO/MISC)	1A
Date: Monday, November 30, 2015	Sheet 12 of 51	

9,10,12,14,16,18 +3V_DEEP_SUS

3D CAMERA
BOM: 3D CAM Un-Stuff

1124 Add SPK_ID for Smart amp feature

1002 modify

Reserve EDP_HPD opposites circuit!

Model	BOARD_ID[8:7] ID8;ID7	BOARD_ID[6:5] ID6;ID5	Board ID [4:3] ID4;ID3	BOARD_ID[2:1] ID2;ID1	BOARD_ID0 ID0
Definition	00 Non 3D SKU 01 3D SKU	00 Reserve	00 Reserve	00 15" 01 17" 10 17" SP	0 : UMA 1 : DIS

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.

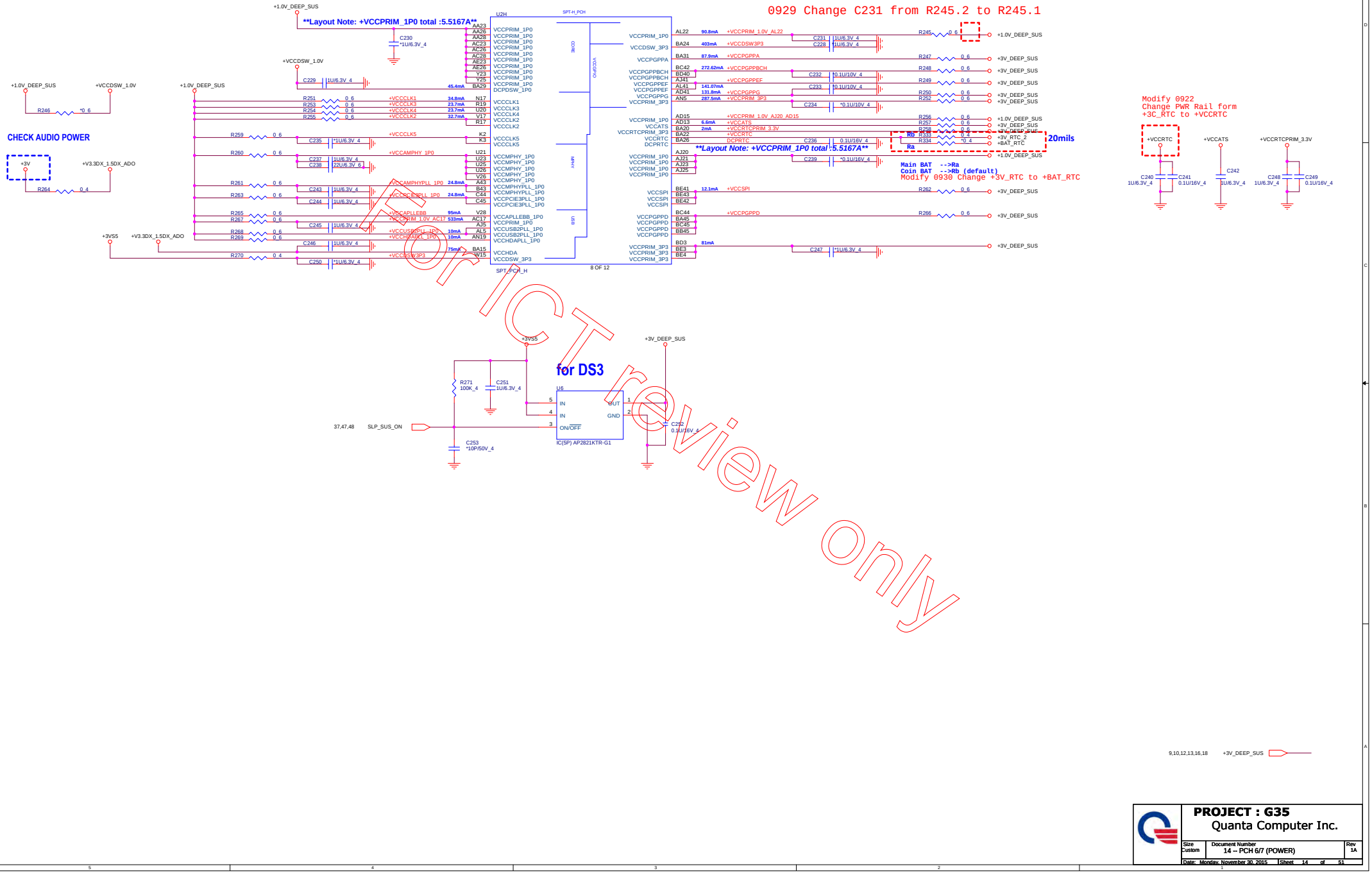
11/03 modify for HDMI2.0

11/03 modify for HDMI2.0

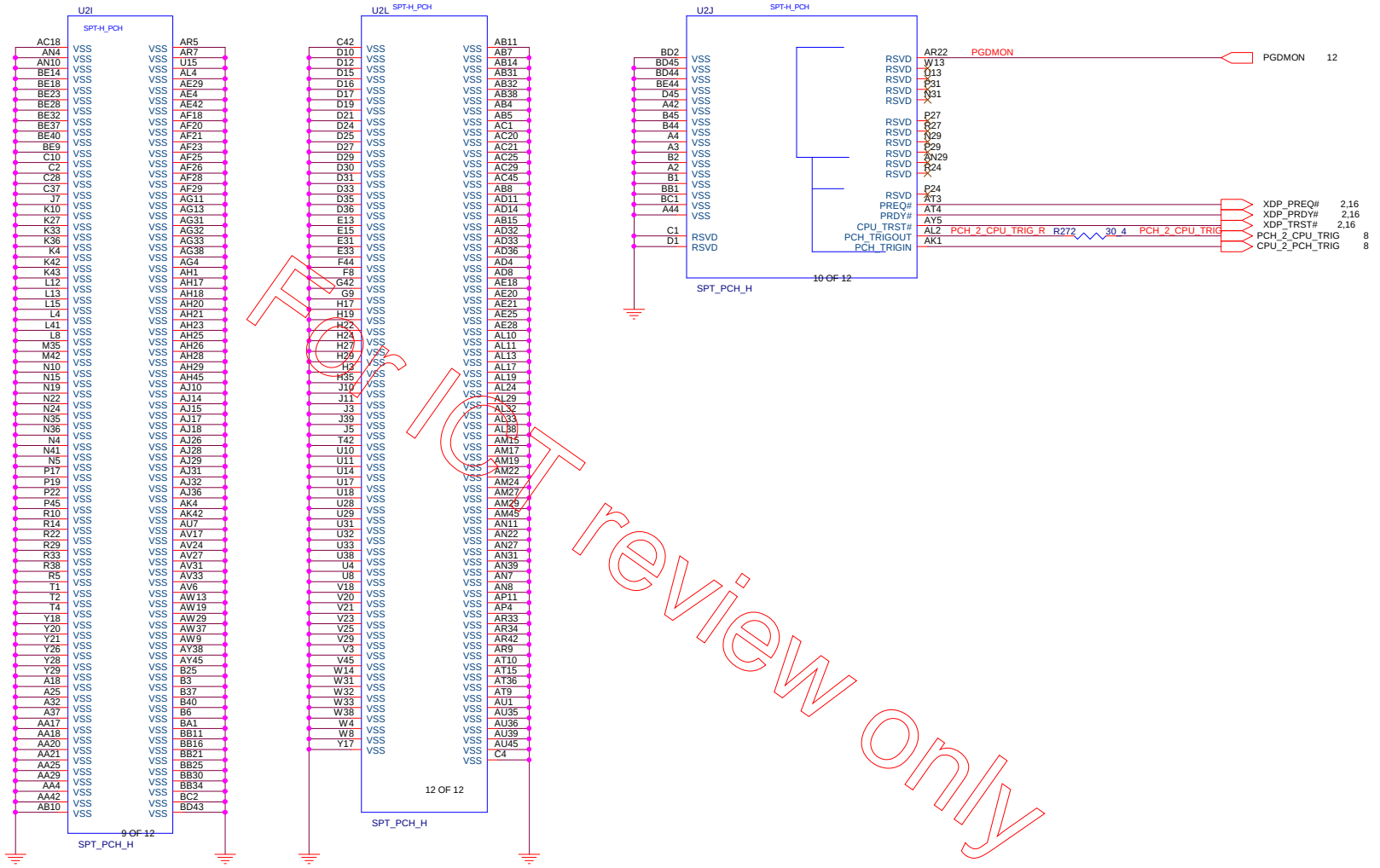
PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- PCH 5/7 (GPIO)	1A

Date: Monday, November 30, 2015 Sheet 13 of 51



PROJECT : G35	Quanta Computer Inc.
Size: Custom	Document Number: 14 -- PCH 6/7 (POWER)
Rev: 1A	
Date: Monday, November 30, 2015	Sheet 14 of 51



PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	15 -- PCH 7/7 (GND)	1A
Date: Monday, November 30, 2015	Sheet 15 of 51	

+3VS5 10,12,14,26,33,37,41,42,46,47,48,51
+3V_DEEP_SUS 9,10,12,13,14,18
+3V 5,9,10,11,12,13,14,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49
+1.0V_DEEP_SUS 10,11,14,47,48
+VCCIO 3,6,48
+1.0V 2,5,6,10,37,48

CPU XDP

CN3 *Samtec BSH-030-01

2,15	XDP_PREQ#	3	OBSFN_A0	VCC_OBS_CD	44
2,15	XDP_PRDY#	5	OBSFN_A1	VCC_OBS_AB	43
2	CFG0	9	OBSDATA_A0	OBSFN_B0	21
2	CFG1	11	OBSDATA_A1	OBSFN_B1	23
2,8	CFG2	15	OBSDATA_A2	OBSFN_C0	4
2,8	CFG3	17	OBSDATA_A3	OBSFN_C1	6
2,8	CFG4	27	OBSDATA_B0	OBSDATA_C0	10
2,8	CFG5	29	OBSDATA_B1	OBSDATA_C1	12
2,8	CFG6	33	OBSDATA_B2	OBSDATA_C2	16
2	CFG7	35	OBSDATA_B3	OBSDATA_C3	18
16	ON/OFFBTN_KBC#	41	HOOK1	OBSFN_D0	22
		45	HOOK2	OBSFN_D1	24
11	CK_XDP_P	40	ITPCLK/HOOK4	OBSDATA_D0	28
11	CK_XDP_N	42	ITPCLK#/HOOK5	OBSDATA_D1	30
		48	DBR#/HOOK7	OBSDATA_D2	34
10,17,18,38	SMB_RUN_DAT	51	SDA	OBSDATA_D3	36
10,17,18,38	SMB_RUN_CLK	53	SCL	HOOK3	47
		52	TDO	TCK1	55
		54	TRSTN	PWRGOOD/HOOK0	39
		56	TDI	RESET#/HOOK6	46
		58	TMS	GND0	1
		57	TCK0	GND1	2
		60	GND17	GND2	7
		59	GND16	GND3	8
		50	GND15	GND4	13
		49	GND14	GND5	14
		38	GND13	GND6	19
		37	GND12	GND7	20
		32	GND11	GND8	25
		31	GND10	GND9	26

R273 *1K_4 XDP_DBRESET_N
R274 *1K_4 CFG0 R275 *1K_4 PWR_DEBUG
R276 *0_4 SMB_RUN_DAT_XDP
R277 *0_4 SMB_RUN_CLK_XDP
XDP_TDO XDP_TRST# XDP_TDI XDP_TMS XDP_TCK0
TP58

+1.0V_DEEP_SUS
TP56
XDP_BPM0 2
XDP_BPM1 2
CFG17 2
CFG16 2
CFG8 2
CFG9 2
CFG10 2,8
CFG11 2
CFG19 2
CFG18 2
CFG12 2,8
CFG13 2,8
CFG14 2
CFG15 2
EC_PWROK 10,37
XDP_TCK1 TP57
SYS_PWROK 10,16
XDP_RST R278 *1K_4
PLTRST# 2,12,16,19,33,34,35,36,37

XDP_DBRESET_N R279 *1K_4 +3V
C254 *0.1U/16V_4
SYS_PWROK R280 *1K_4 +3V_DEEP_SUS
C257 *0.1U/16V_4
+1.0V_DEEP_SUS
C255 *0.1U/16V_4
C256 *0.1U/16V_4
+VCCIO
R281 150/F_4
PWR_DEBUG
R282 *10K_4

APS

+3V_DEEP_SUS
+3VS5
CN1 *ACES_88511-180N

	SUSB#	10,16,37
	SLP_S5#	10
2,10,37,41,42,47,48	SUSC# / HWPG	10,37
	SLP_A#	10
	RTC_RST#	10
	ON/OFFBTN_KBC#	16
	SYS_RESET#	10
	R283 *0_4 PCH_SLP_S0_N	10
	SUSB#	10,16,37

+3V
C258 *0.1U/16V_4
+1.0V
R284 *51_4 XDP_TDO
TP59 XDP_TDI
TP60 XDP_TMS
2,15 XDP_TRST# XDP_TRST#

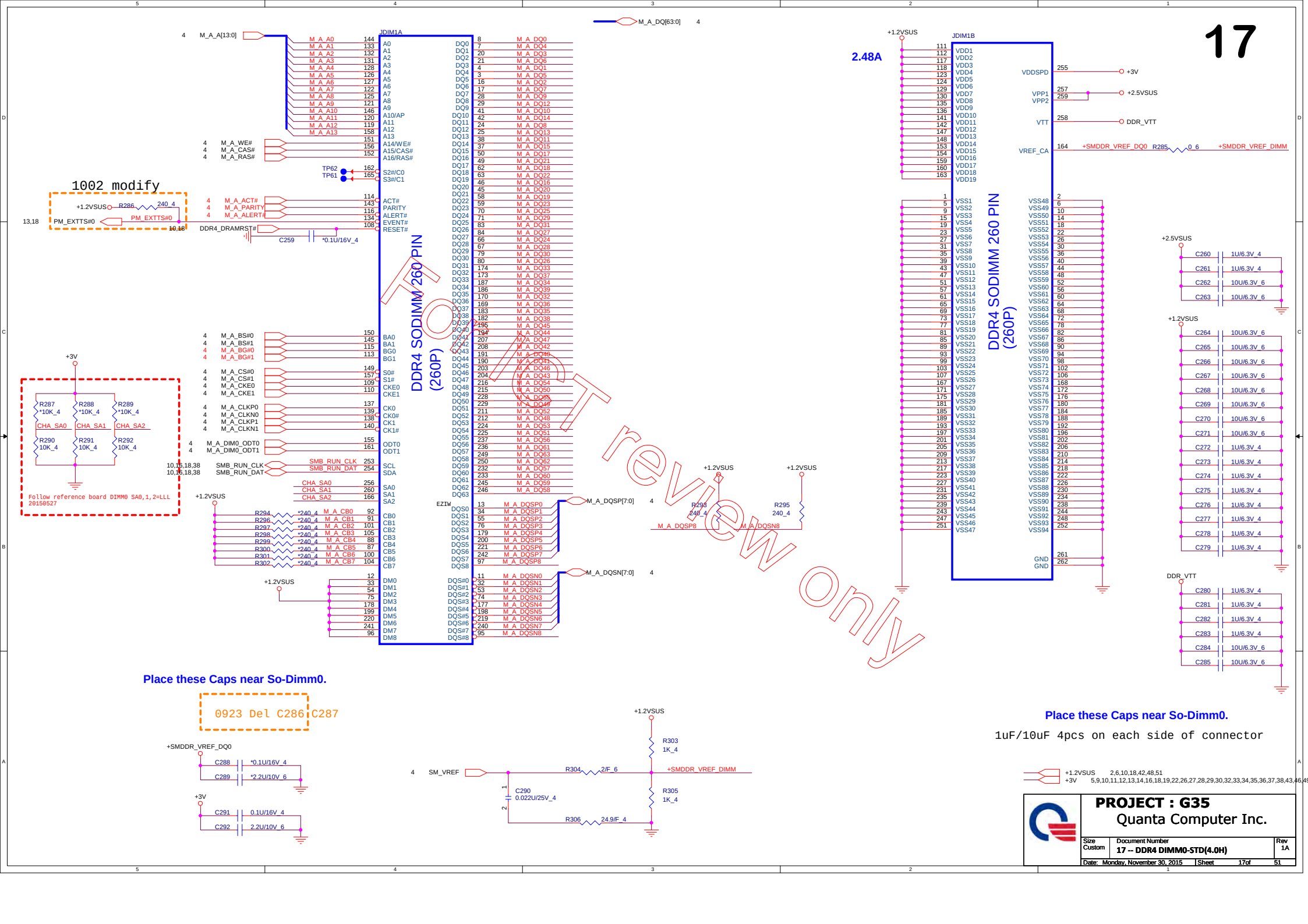
U7 *SN74CBTLV3126RGYR

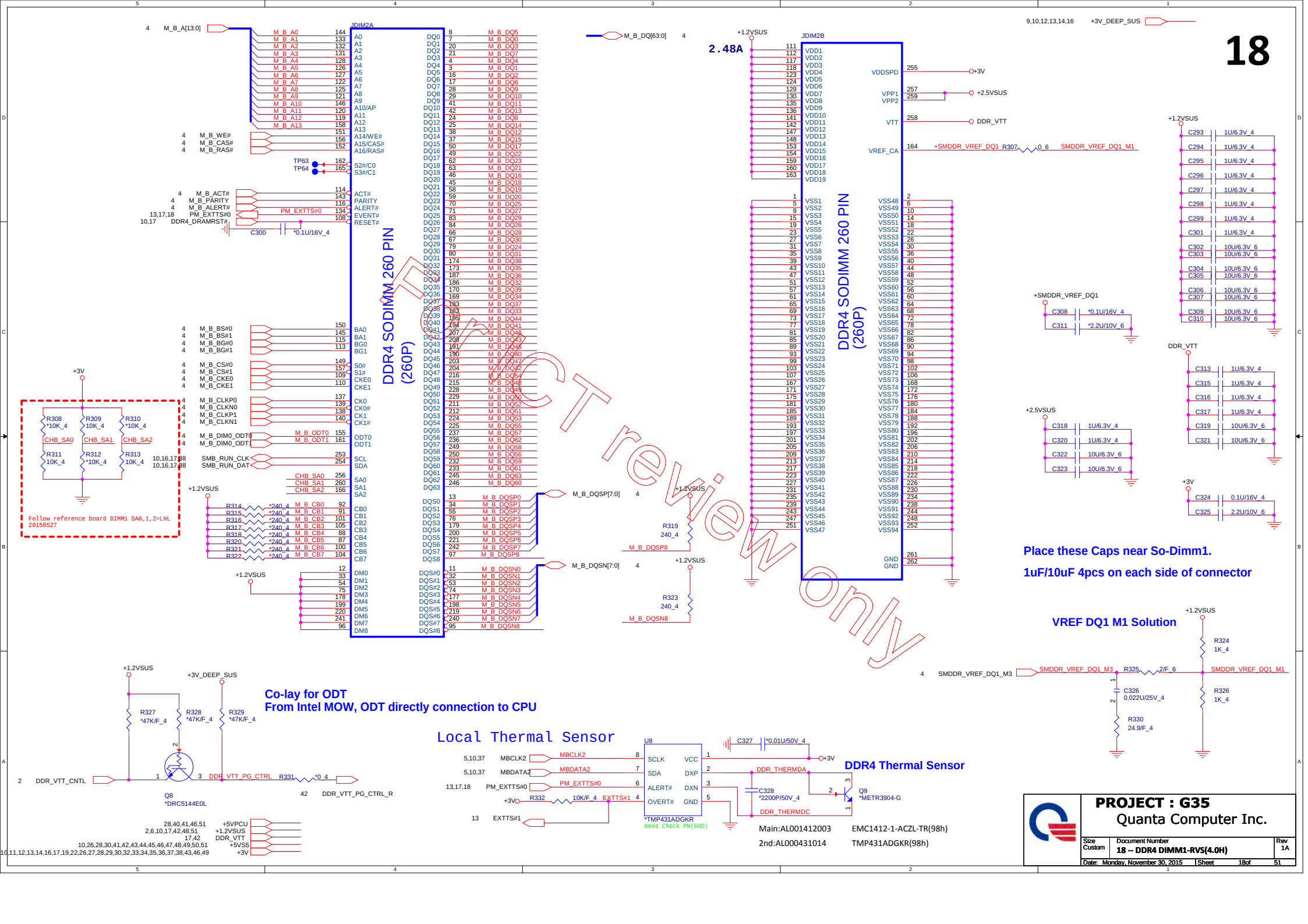
14	VCC		
2	1A	1B	3 XDP_TDO_CPU 2
1	1OE		
5	2A	2B	6 XDP_TDI_CPU 2
4	2OE		
9	3A	3B	8 XDP_TMS_CPU 2
10	3OE		
12	4A	4B	11 XDP_TRST#_CPU 2
13	4OE		
	DPAD		15
	GND		7

10,16 SYS_PWROK
2,12,16,19,33,34,35,36,37 PLTRST#
R340 *1K_4 XDP_RST
+1.0V
R347 *51_4
R345 *0_4 XDP_TDO
10 JTAGX_PCH XDP_TCK0
10 JTAG_TMS_PCH XDP_TMS
10 JTAG_TDI_PCH XDP_TDI
10 JTAG_TDO_PCH XDP_TDO
R342 *0_4 XDP_TDI
R344 *0_4 XDP_TCK0
10 JTAG_TCK_PCH XDP_TCK1

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
	16 -- XDP & APS	1A
Date: Monday, November 30, 2015	Sheet 16 of 51	


JDIM1A
DDR4 SODIMM 260 PIN
(260P)
JDIM1B
DDR4 SODIMM 260 PIN
(260P)
2.48A
1002 modify
0923 Del C286 C287
Follow reference board DIMM0 SA0,1,2=LLL
20150527
Place these Caps near So-Dimm0.
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
For Internal review only
PROJECT : G35
Quanta Computer Inc.
Size Custom
Document Number
17 -- DDR4 DIMM0-STD(4.0H)
Rev 1A
Date: Monday, November 30, 2015
Sheet 17of 51


JDIM2A
DDR4 SODIMM 260 PIN (260P)
JDIM2B
DDR4 SODIM 260 PIN (260P)
2.48A
Intel Confidential
Review Only
Follow reference board DIMM1 SA0,1,2=LHL 20150527
Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector
VREF DQ1 M1 Solution
Co-lay for ODT
From Intel MOW, ODT directly connection to CPU
Local Thermal Sensor
DDR4 Thermal Sensor
*TMP431ADGKR
Need Check PN(EOD)
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)
PROJECT : G35
Quanta Computer Inc.
Size Custom
Document Number 18 -- DDR4 DIMM1-RVS(4.0H)
Rev 1A
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+3V 5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49
+3V_AON 22,23,27,51
+3V_GFX 20,21,22,23,49,51
+1.05V_GFX 20,21,23,51

U1001A
N16E-GR-A1

PEX_IOVDD/Q : 3300mA
+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU

C1004 22U/6.3VS_6
C1005 22U/6.3VS_6
C1006 22U/6.3VS_6
C1001 22U/6.3VS_6
C1007 10U/6.3VS_6
C1008 10U/6.3VS_6
C1009 10U/6.3VS_6
C1002 10U/6.3VS_6

PLACE NEAR BALLS

C1010 1U/6.3V_4
C1011 1U/6.3V_4
C1003 1U/6.3V_4
C1013 1U/6.3V_4

PLACE UNDER BGA

C1014 4.7U/6.3V_4
C1015 4.7U/6.3V_4

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6

AG13 PEX_IOVDDQ_1
AG15 PEX_IOVDDQ_2
AG16 PEX_IOVDDQ_3
AG18 PEX_IOVDDQ_4
AG25 PEX_IOVDDQ_5
AH15 PEX_IOVDDQ_6
AH18 PEX_IOVDDQ_7
AH26 PEX_IOVDDQ_8
AH27 PEX_IOVDDQ_9
AJ27 PEX_IOVDDQ_10
AK27 PEX_IOVDDQ_11
AL27 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

[PEG Interface]

PEX_RX0 AN12
PEX_RX0_N AM12
PEX_RX1 AN14
PEX_RX1_N AM14
PEX_RX2 AP14
PEX_RX2_N AP15
PEX_RX3 AN15
PEX_RX3_N AM15
PEX_RX4 AN17
PEX_RX4_N AM17
PEX_RX5 AP17
PEX_RX5_N AP18
PEX_RX6 AN18
PEX_RX6_N AM18
PEX_RX7 AN20
PEX_RX7_N AM20
PEX_RX8 AP20
PEX_RX8_N AP21
PEX_RX9 AN21
PEX_RX9_N AM21
PEX_RX10 AN23
PEX_RX10_N AM23
PEX_RX11 AP23
PEX_RX11_N AP24
PEX_RX12 AN24
PEX_RX12_N AM24
PEX_RX13 AN26
PEX_RX13_N AM26
PEX_RX14 AP26
PEX_RX14_N AP27
PEX_RX15 AN27
PEX_RX15_N AM27

PEG_TXP0 3
PEG_TXN0 3
PEG_TXP1 3
PEG_TXN1 3
PEG_TXP2 3
PEG_TXN2 3
PEG_TXP3 3
PEG_TXN3 3
PEG_TXP4 3
PEG_TXN4 3
PEG_TXP5 3
PEG_TXN5 3
PEG_TXP6 3
PEG_TXN6 3
PEG_TXP7 3
PEG_TXN7 3

PEX_TX0 AK14 PEG_RXP0_C C1016 0.22U/10V_4 PEG_RXP0 3
PEX_TX0_N AJ14 PEG_RXN0_C C1017 0.22U/10V_4 PEG_RXN0 3
PEX_TX1 AH14 PEG_RXP1_C C1018 0.22U/10V_4 PEG_RXP1 3
PEX_TX1_N AG14 PEG_RXN1_C C1019 0.22U/10V_4 PEG_RXN1 3
PEX_TX2 AK15 PEG_RXP2_C C1020 0.22U/10V_4 PEG_RXP2 3
PEX_TX2_N AJ15 PEG_RXN2_C C1021 0.22U/10V_4 PEG_RXN2 3
PEX_TX3 AJ16 PEG_RXP3_C C1022 0.22U/10V_4 PEG_RXP3 3
PEX_TX3_N AK16 PEG_RXN3_C C1023 0.22U/10V_4 PEG_RXN3 3
PEX_TX4 AK17 PEG_RXP4_C C1194 0.22U/10V_4 PEG_RXP4 3
PEX_TX4_N AJ17 PEG_RXN4_C C1196 0.22U/10V_4 PEG_RXN4 3
PEX_TX5 AH17 PEG_RXP5_C C1190 0.22U/10V_4 PEG_RXP5 3
PEX_TX5_N AG17 PEG_RXN5_C C1193 0.22U/10V_4 PEG_RXN5 3
PEX_TX6 AK18 PEG_RXP6_C C1195 0.22U/10V_4 PEG_RXP6 3
PEX_TX6_N AJ18 PEG_RXN6_C C1192 0.22U/10V_4 PEG_RXN6 3
PEX_TX7 AL19 PEG_RXP7_C C1191 0.22U/10V_4 PEG_RXP7 3
PEX_TX7_N AK19 PEG_RXN7_C C1197 0.22U/10V_4 PEG_RXN7 3
PEX_TX8 AK20
PEX_TX8_N AJ20
PEX_TX9 AH20
PEX_TX9_N AG20
PEX_TX10 AK21
PEX_TX10_N AJ21
PEX_TX11 AL22
PEX_TX11_N AK22
PEX_TX12 AK23
PEX_TX12_N AJ23
PEX_TX13 AH23
PEX_TX13_N AG23
PEX_TX14 AK24
PEX_TX14_N AJ24
PEX_TX15 AL25
PEX_TX15_N AK25

AC6 NC_1
AJ28 NC_2
AJ4 NC_3
AJ5 NC_4
AL11 NC_5
C15 NC_6
D19 NC_7
D20 NC_8
D23 NC_9
D26 NC_10
H31 NC_11
T8 NC_12
V32 NC_13

PLACE CLOSE TO BGA

C1024 4.7U/6.3V_4
C1025 1U/6.3V_4
C1026 0.1U/16V_4

PLACE CLOSE TO GPU BALLS

+3V_AON
+3V_GFX
VDD33 : 85mA

J8 VDD33_1
K8 VDD33_2
L8 VDD33_3
M8 VDD33_4

PLACE CLOSE TO BGA

C1027 4.7U/6.3V_4
C1028 1U/6.3V_4
C1029 0.1U/16V_4
C1030 0.1U/16V_4

PLACE CLOSE TO GPU BALLS

PEX_REFCLK AL13 CLK_VGA_P 11
PEX_REFCLK_N AK13 CLK_VGA_N 11

PEX_TSTCLK_OUT AJ26 PEX_TSTCLK R1006 *200/F_4
PEX_TSTCLK_OUT_N AK26 PEX_TSTCLK#

PEX_WAKE AJ11
PEX_RST_N AJ12 VGA_RST# R1007 0_4 PEGX_RST#

PEX_CLKREQ_N AK12 PEX_CLKREQ# R1008 10K_4 +3V_AON

PEX_TERMP AP29 PEX_TERMP R1009 2.49K/F_4

TESTMODE AK11 TESTMODE R1010 10K_4 R1011 0_6 +1.05V_GFX

PEX_PLLVDD AG26 PEX_PLLVDD PEX_PLLVDD : 150mA
C1031 4.7U/6.3V_4
C1032 1U/6.3V_4
C1035 0.1U/16V_4
PLACE NEAR GPU
PLACE NEAR GPU
PLACE UNDER GPU

PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
PEX_SVDD_3V3 : 210mA
+3V_AON
0.1U/16V_4 C1033
4.7U/6.3V_4 C1034
4.7U/6.3V_4 C1036
PLACE NEAR GPU

3.3V_AUX_NC P8

VDD_SENSE L4 VGPU_CORE_SENSE 49

GND_SENSE L5 VSS_GPU_SENSE 49

All 3.3V
NVVDD
PEX_VDD 1.05V
FBVDD/Q
90%
90%
90%

+3V_GFX R1001 4.7K_4 PCIE_CLKREQ_VGA# 11
PEX_CLKREQ# Q1001 DRC5144E0L Q1002 DRC5144E0L

If stuff Da,Db,Ra,Rb, do not stuff Ua,Ub,Ca,Cb,Rc,Rd

Ra R1124 *10K_4 +3V_AON
PLTRST# SYS_PEX_RST_MON#
DGPU_HOLD_RST# GPU_PEX_RST_HOLD#
Da D1004 *BAT54AW-L
Db D1000 BAT54AW-L
Rb R1005 10K_4 +3V_AON
PEGX_RST#

Ua U1002 MC74VHC1G08DFT2G
Ca C1012 0.1U/16V_4
Ub U1000 *MC74VHC1G08DFT2G
Cb C1000 *0.1U/16V_4
2,12,16,33,34,35,36,37
9,12 DGPU_HOLD_RST#
PLTRST#
R1002 Rc 0_4
R1000 *0_4
Rd R1003 *100K/F_4
SYS_PEX_RST_MON# 22
PEGX_RST# 22,27
22 GPU_PEX_RST_HOLD#

1130 Change D1004,R1124 from I to NI
Change U1002,R1002,C1012 from NI to I

GPU type	Part Number	Part Description	Where USed
N16P-GT	AJ0N16P0T05	IC CTRL(908P)N16P-GT-A2(BGA)TOPBSQ	G35A
	AJ0N16P0T06	IC CTRL(908P)N16P-GT-A2(BGA)QBCON	
N16P-GX	AJ0N16P0T14	IC CTRL(908P)N16P-GX-A2(BGA)TOPBSQ	G35A / G37A
	AJ0N16P0T15	IC CTRL(908P)N16P-GX-A2(BGA)QBCON	
N16E-GR	AJ0N16E0T02	IC CTRL(908P)N16E-GR-A1(BGA)TOPBSQ	G35A / G37A
	AJ0N16E0T03	IC CTRL(908P)N16E-GR-A1(BGA)QBCON	

PROJECT : G35
Quanta Computer Inc.
Size Custom
Document Number N16P-GX/GT - 1/5 (PCIE)
Rev 1A
Date: Monday, November 30, 2015 Sheet 19 of 51

+3V_GFX 19,21,22,23,49,51
+1.35V_GFX 23,24,25,50
+1.05V_GFX 19,21,23,51
NV_PLLVDD 21

U1001B
N16E-GR-A1

[MEMORY I/F A]

U1001C
N16E-GR-A1

MEMORY I/F C

GDDR5 NO USE

GDDR5 NO USE

PLACE CLOSE TO GPU BALLS

PLACE CLOSE TO BGA

MUST BE on GPU ball

BOM
N16E-GR: Ra (Default)
N16P-GX/GT/N16S-GTR-B: Rb

BOM
N16E-GR: La (Default)
N16P-GX/GT/N16S-GTR-B: Lb

PLACE CLOSE TO GPU

PLACE CLOSE TO BALL

1029 Change

+FB_PLLAVDD : 62mA

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N16P-GX/GT - 2/5 (Memory)	1A

Date: Monday, November 30, 2015 Sheet 20 of 51

+1.05V_GFX 19,20,23,51
NV_PLLVDD 20

U1001D
N16E-GR-A1

[IFPA/B_LVDS]
AH8 IFPAB_PLLVDD
AG8 IFPA_IOVDD
AG9 IFPB_IOVDD
AJ8 IFPAB_RSET
IFPA_TXC AM6
IFPA_TXC_N AN6
IFPA_TXD0 AP3
IFPA_TXD0_N AN3
IFPA_TXD1 AN5
IFPA_TXD1_N AM5
IFPA_TXD2 AL6
IFPA_TXD2_N AK6
IFPA_TXD3 AJ6
IFPA_TXD3_N AH6
IFPB_TXC AJ9
IFPB_TXC_N AH9
IFPB_TXD4 AP6
IFPB_TXD4_N AP5
IFPB_TXD5 AM7
IFPB_TXD5_N AL7
IFPB_TXD6 AN8
IFPB_TXD6_N AM8
IFPB_TXD7 AK8
IFPB_TXD7_N AL8

[IFPC/D_TMDS]
AF7 IFPC_PLLVDD
AG7 IFPD_PLLVDD
AF6 IFPC_IOVDD
AG6 IFPD_IOVDD
AF8 IFPC_RSET
AN2 IFPD_RSET
IFPC_AUX_I2CW_SCL AG3
IFPC_AUX_I2CW_SDA_N AG2
IFPC_L0 AK1
IFPC_L0_N AJ1
IFPC_L1 AJ3
IFPC_L1_N AJ2
IFPC_L2 AH3
IFPC_L2_N AH4
IFPC_L3 AG5
IFPC_L3_N AG4
IFPD_AUX_I2CX_SCL AK3
IFPD_AUX_I2CX_SDA_N AK2
IFPD_L0 AM1
IFPD_L0_N AM2
IFPD_L1 AM3
IFPD_L1_N AM4
IFPD_L2 AL3
IFPD_L2_N AL4
IFPD_L3 AK4
IFPD_L3_N AK5

IFPC_PLLVDD
C8626 0.1U/16V_4
C8627 0.1U/16V_4
PLACE AT BALLS
IFPC_IOVDD
C8629 0.1U/16V_4
C8628 0.1U/16V_4
PLACE AT BALLS
11/04 modify for HDMI2.0

0.25A
+3V_GFX L7517 FCM1005KF-301T03 IFPC_PLLVDD
PLACE OUTSIDE OF BALL
C8597 4.7U/6.3V_6
C8596 1U/6.3V_4
C8598 0.1U/16V_4
PLACE AT BALLS
0.3A
+1.05V_GFX L7518 HCB1005KF-181T15(180,1.5A)_4 IFPC_IOVDD
PLACE OUTSIDE OF BALL
C8593 4.7U/6.3V_6
C8594 1U/6.3V_4
C8624 0.1U/16V_4
C8595 0.1U/16V_4
PLACE AT BALLS
R8559 1K_4

AB8 IFPEF_PLLVDD
AC7 IFPE_IOVDD
AC8 IFPF_IOVDD
AD6 IFPEF_RSET

[IFPE/F_DP]
IFPE_AUX_I2CY_SCL AB3
IFPE_AUX_I2CY_SDA_N AB4
IFPE_L0 AD2
IFPE_L0_N AD3
IFPE_L1 AD1
IFPE_L1_N AC1
IFPE_L2 AC2
IFPE_L2_N AC3
IFPE_L3 AC4
IFPE_L3_N AC5
IFPF_AUX_I2CZ_SCL AF3
IFPF_AUX_I2CZ_SDA_N AF2
IFPF_L0 AE3
IFPF_L0_N AE4
IFPF_L1 AF4
IFPF_L1_N AF5
IFPF_L2 AD4
IFPF_L2_N AD5
IFPF_L3 AG1
IFPF_L3_N AF1

GPU_DDCCLK 27
GPU_DDCDATA 27
GPU_D2 27
GPU_D2# 27
GPU_D1 27
GPU_D1# 27
GPU_D0 27
GPU_D0# 27
GPU_CLK 27
GPU_CLK# 27
11/03 modify for HDMI2.0

AG10 DACA_VDD
AP9 DACA_VREF
AP8 DACA_RSET

[DACA/B_CRT]
DACA_RED AK9
DACA_GREEN AL10
DACA_BLUE AL9
DACA_HSYNC AM9
DACA_VSYNC AN9
I2CA_SCL R4 I2CA_SCL R1022 1.8K/F_4
I2CA_SDA R5 I2CA_SDA R1023 1.8K/F_4

1029 Change
NV_PLLVDD
PLLVDD : 200mA
+1.05V_GFX L1002 HCB1005KF-330T30 NV_PLLVDD AD8
C1059 22U/6.3VS_6
C1060 0.1U/16V_4
SP_PLLVDD AE8
+1.05V_GFX L1003 HCB1005KF-181T15 VID_PLLVDD AD7
C1061 47U/6.3VS_6
C1062 10U/6.3V_6
C1063 0.1U/16V_4
C1064 0.1U/16V_4
PLACE CLOSE TO GPU PLACE CLOSE TO BALLS

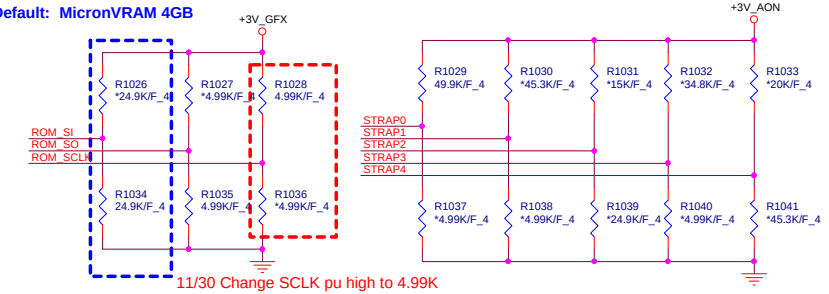
AD8 PLLVDD
AE8 SP_PLLVDD
AD7 VID_PLLVDD

[XTAL IN]
XTAL_IN H3 XTAL27_IN
XTAL_OUT H2 XTAL27_OUT
XTAL_OUTBUFF J4 R1024 10K_4
XTAL_SSIN H1 R1025 10K_4
Y1000
27MHZ +-10PPM
C1065 10P/50V_4
C1066 10P/50V_4

PROJECT : G35
Quanta Computer Inc.
Size A3 | Document Number N16P-GX/GT - 3/5 (Display) | Rev 1A
Date: Monday, November 30, 2015 | Sheet 21 of 51

+3V 5,9,10,11,12,13,14,16,17,18,19,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49
+3V_AON 19,23,27,51
+3V_GFX 19,20,21,23,49,51

Default: MicronVRAM 4GB



11/30 Change SCLK pu high to 4.99K

GPU Netname	N16P-GT	N16P-GX	N16E-GR
ROM_SO	4.99K PD	4.99K PD	4.99K PD
ROM_SCLK	4.99K PD	4.99K PD	4.99K PD
STRAP0	49.9K PU	49.9K PU	49.9K PU
STRAP1	NC	NC	NC
STRAP2	NC	NC	NC
STRAP3	NC	NC	NC
STRAP4	NC	NC	NC

4.99K/F_4: CS24992FB26 RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
15K/F_4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
24.9K/F_4: CS32492FB16 RES CHIP 24.9K 1/16W +-1%(0402)
30.1K/F_4: CS33012FB18 RES CHIP 30.1K 1/16W +-1%(0402)
34.8K/F_4: CS33482FB22 RES CHIP 34.8K 1/16W +-1% (0402)
45.3K/F_4: CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

Resistor Values	PU to 3V3_MAIN	PD to GND
4.99K OHM	1000	0000
10K OHM	1001	0001
15K OHM	1010	0010
20K OHM	1011	0011
24.9K OHM	1100	0100
30.1K OHM	1101	0101
34.8K OHM	1110	0110
45.3K OHM	1111	0111

VRAM Table of N16P-GX N16P-GX device ID = 0x139B

Vendor	TOP B/S / QBCON	Mfr. P/N	SIZE	ROM_SI
Hynix	AKG5PWUTW19 / AKG5PWUTW20	H5GC4H24AJR-T2C	256Mx16	0x6 0110 PD 34.8K
Micron	AKG5PW0TL05 / AKG5PW0TL06	EDW4032BABG-60-F-R	256Mx16	0x4 0100 PD 24.9K
Micron	AKG5LGUTL02 / AKG5LGUTL03	MT51J256M32HF-60:A	256Mx32	0x9 1001 PU 10K
Samsung	AKG5QGDT503 / AKG5QGDT504	K4G80325FB-HC03	256Mx32	0x8 1000 PU 4.99K

VRAM Table of N16E-GR N16E-GR device ID = 0x1427

Vendor	TOP B/S / QBCON	Mfr. P/N	SIZE	ROM_SI
Hynix	AKG5PWUTW19 / AKG5PWUTW20	H5GC4H24AJR-T2C	256Mx16	0x0 0110 PD 4.99K
Micron	AKG5PW0TL05 / AKG5PW0TL06	EDW4032BABG-60-F-R	256Mx16	0x1 0001 PD 10K
Micron	AKG5LGUTL02 / **AKG5LGUTL03**	**MT51J256M32HF-60:A**	**256Mx32**	**0x4 0100 PD 24.9K**
Samsung	AKG5QGDT503 / AKG5QGDT504	K4G80325FB-HC03	256Mx32	0x3 0011 PD 20K

VRAM Table of N16P-GT N16P-GT device ID = 0x139A

Vendor	TOP B/S / QBCON	Mfr. P/N	SIZE	ROM_SI
Hynix	AKG5PWUTW19 / AKG5PWUTW20	H5GC4H24AJR-T2C	256Mx16	0x6 0110 PD 34.8K
Micron	AKG5PW0TL05 / AKG5PW0TL06	EDW4032BABG-60-F-R	256Mx16	0x4 0100 PD 24.9K

U1001E
N16E-GR-A1

[MIOA]

[MIOB]

[MISC_GPIO/I2C/JTAG/THER]

[MISC2_ROM]

+3V_AON

GPU_EVENT# GPU R1042 10K_4
VGA_OVT# R1043 10K_4
ALERT R1044 10K_4
PWR_LEVEL R1045 10K_4
+3V_MAIN_EN R1046 10K_4
SYS_PEX_RST_MON# R1047 *10K_4
GPU_PEX_RST_HOLD# R1048 10K_4

GPIO10_VREF R1049 100K/F_4
JTAG_TRST# R1050 10K_4
GC6_FB_EN R1051 10K_4

TP1002 TP1003 TP1004 TP1005
AM10 AP11 AM11 AP12 AN11
JTAG_TCK JTAG_TMS JTAG_TDI JTAG_TDO JTAG_TRST_N

1.8K/F_4 R1053 I2CB_SCL R7
1.8K/F_4 R1054 I2CB_SDA R6
I2CB_SCL I2CB_SDA

1.8K/F_4 R1055 I2CC_SCL R2
1.8K/F_4 R1056 I2CC_SDA R3
I2CC_SCL I2CC_SDA

GFx_SCL T4
GFx_SDA T3
I2CS_SCL I2CS_SDA

K4 THERMDP
K3 THERMDN

STRAP0 J2
STRAP1 J7
STRAP2 J6
STRAP3 J5
STRAP4 J3

R1059 *40.2K/F_4
J1 MULTISTRAP_REF_GND
R1063 40.2K/F_4

GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13 GPIO14 GPIO15 GPIO16 GPIO17 GPIO18 GPIO19 GPIO20 GPIO21

P6 GPIO0 R1052 0_4 GC6_FB_EN

GPU_EVENT# should be connected to PCH GPIO pin for GC6 2.0 function.

M7 GPU_EVENT# GPU 2 D1001 1 RB500V-40 +3V_MAIN_EN 49,51 GPU_EVENT# 9,12
M1 VGA_OVT#
M2 ALERT
L1 GPIO10_VREF GPIO10_VREF 24,25
M5 GPU_VID 49
N3 PWR_LEVEL 2 D1002 1 RB500V-40 DGPU_PROCHOT_EC# 37,49
M4 PSI 49
N4 R1057 10K_4 +3V_AON
P2
R8
M6
R1 R8567 0_4 HDMI_HPD_GPU 27
P3
P4
P1 GPU_PEX_RST_HOLD# 19 R8568 100K/F_4

PEGX_RST# 2 Q1000 *2N7002K 1 3 PEGX_RST# 19,27
VGA_OVT# DGPU_OVT# 37

H4 ROM_SCLK
H6 ROM_CS_N
H5 ROM_SI
H7 ROM_SO
ROM_SCLK ROM_SI ROM_SO

11/04 modify for HDMI2.0

L2 BUFRST_N
L3 CEC
R1064 0_4 SYS_PEX_RST_MON# 19 +3V_AON R1067 4.7K_4 R1068 *0_4
R1066 10K_4

1129 Change R1066 from NI to I

GFx SMBus Isolation

+3V_AON R1061 4.7K_4 R1062 *0_4 R1060 0_4
GFx_SCL 4 Q1003 2N7002KDW 5 3 GPUT_CLK
GFx_SDA 1 2 6 GPUT_DATA

1130 Change D1003, R1123 from I to NI
Change U1003, C1067 from NI to I

If stuff Da,Ra, do not stuff Ua,Ca

GC6_FB_EN DGPU_VC_EN D1003 *BAT54CW-7-F Da R1123 Ra *100K/F_4 DGPU_FB_EN

+3V Ca C1067 0.1U/16V_4 R1058 *10K_4 +3V
50 DGPU_FB_EN 4 U1003 NL17SZ32DFT2G Ua 5 2 1 3 GC6_FB_EN 9 DGPU_VC_EN 49,51
37 37

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N16P-GX/GT - 4/5 (MISC)	1A

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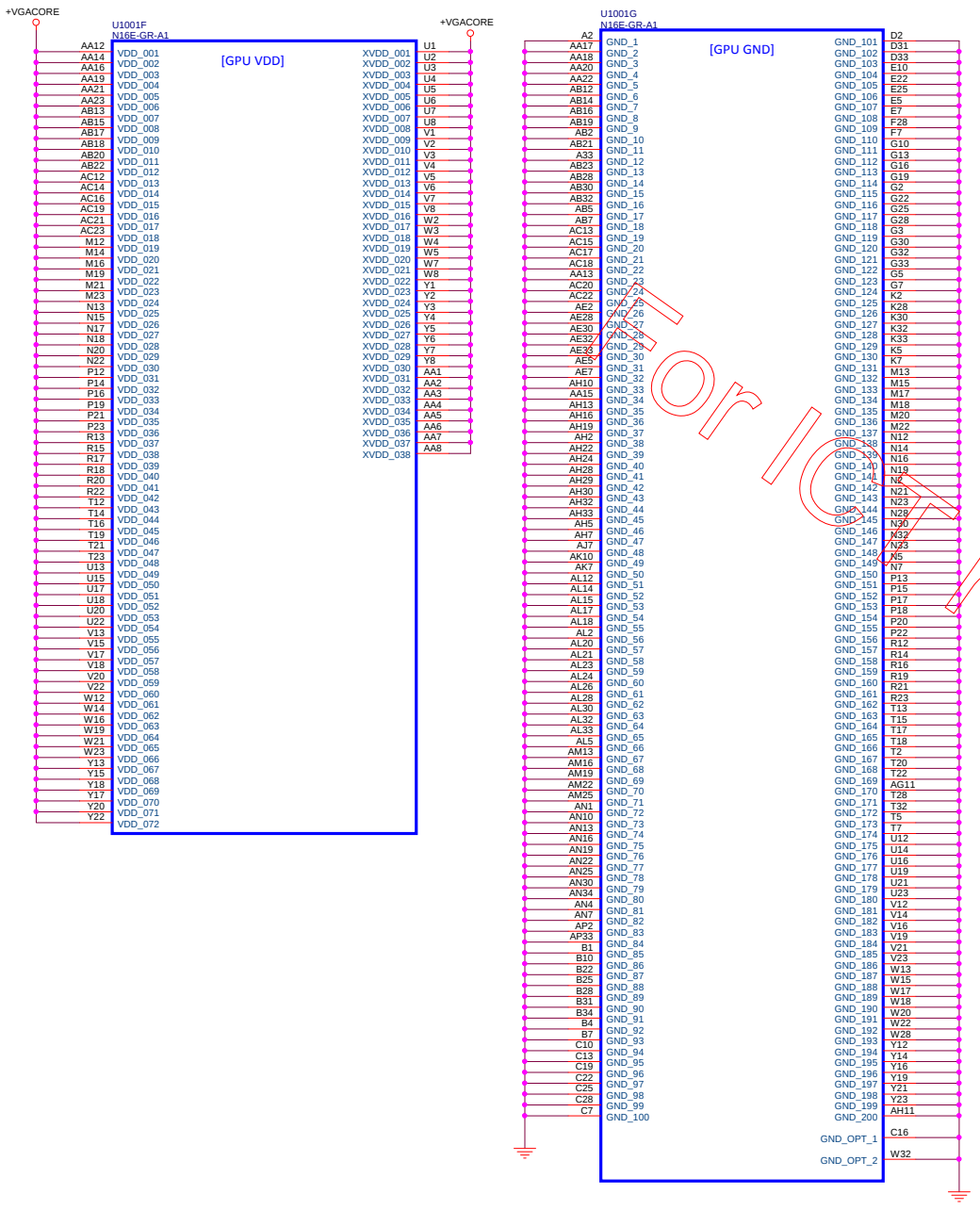
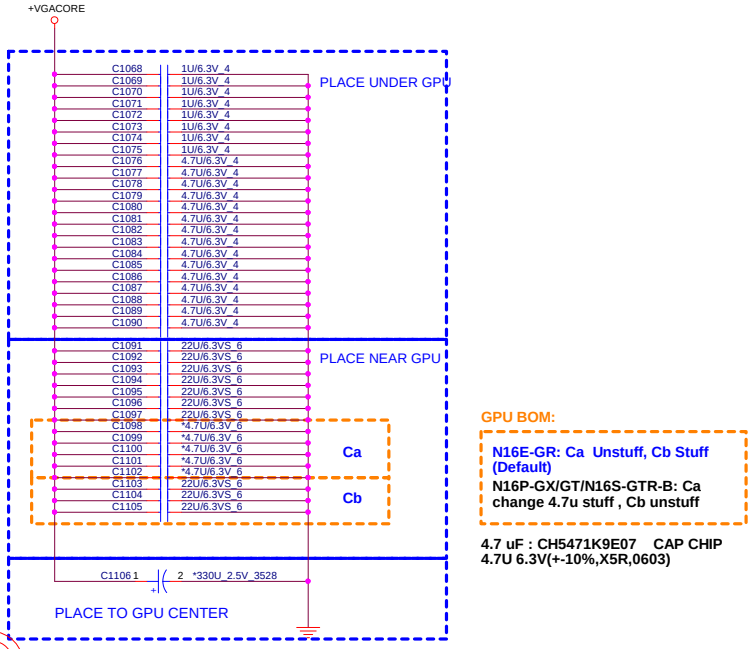
+3V_AON 19,22,27,51
+3V_GFX 19,20,21,22,49,51
+1.35V_GFX 20,24,25,50
+1.05V_GFX 19,20,21,51
+VGACORE 49

VDD/XVDD : 62A



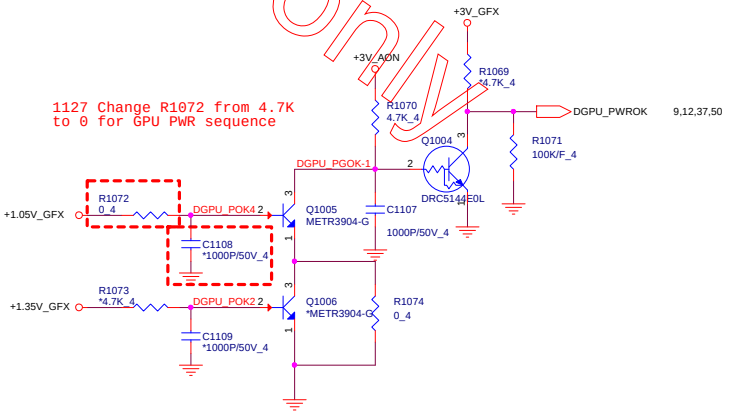


GPU BOM:

N16E-GR: Ca Unstuff, Cb Stuff (Default)
N16P-GX/GT/N16S-GTR-B: Ca change 4.7u stuff , Cb unstuff

4.7 uF : CH5471K9E07 CAP CHIP 4.7U 6.3V(+-10%,X5R,0603)

For meet Power down sequence for +3V_GFX



PROJECT : G35
Quanta Computer Inc.

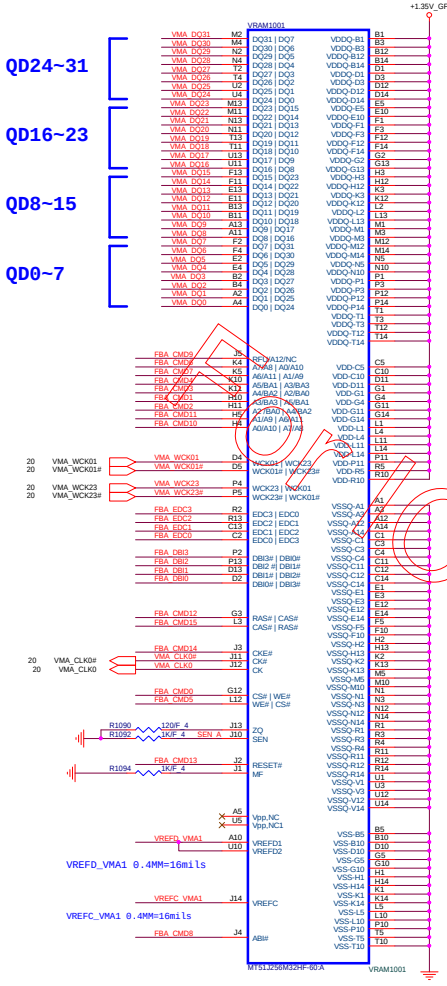
Size	Document Number	Rev
Custom	N16P-GX/GT - 5/5 (Power)	1A

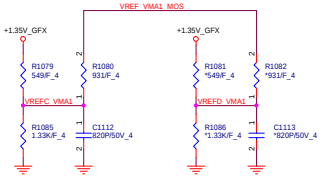
Date: Monday, November 30, 2015 Sheet 23 of 51

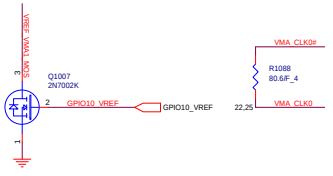
CHANNEL A: 2G/4G GDDR5

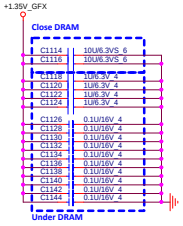
MF=0 Non-mirrored

QD24~31
QD16~23
QD8~15
QD0~7



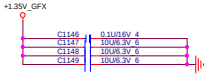


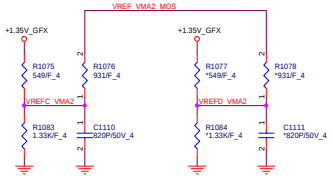


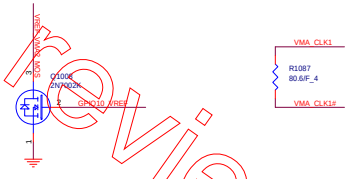


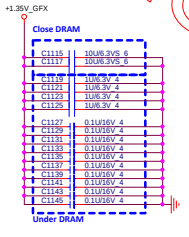
VREFD_VMA1 0.4MM=16mils

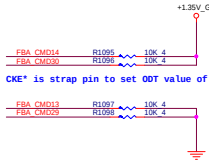
VREFC_VMA1 0.4MM=16mils









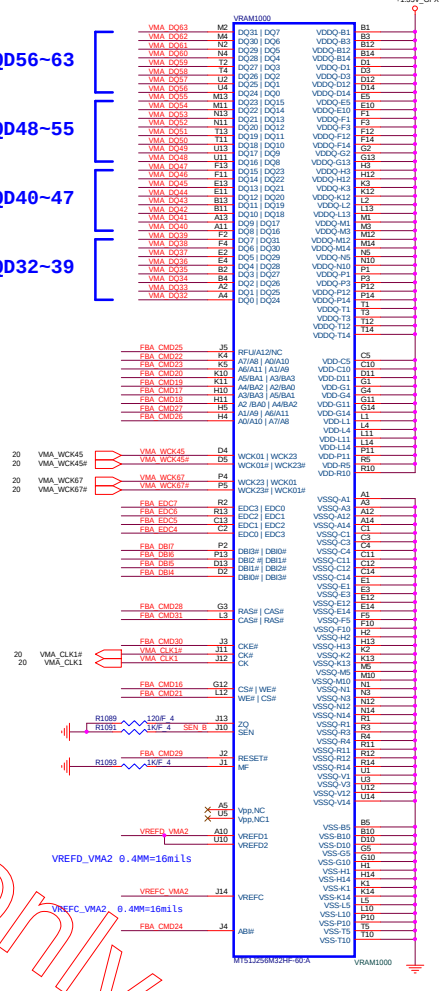


CKE* is strap pin to set ODT value of memory chip

RST PD place to the end of daisy-chain.

MF=0 Non-mirrored

QD56~63
QD48~55
QD40~47
QD32~39



VREFD_VMA2 0.4MM=16mils

VREFC_VMA2 0.4MM=16mils

GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

+1.35V_GFX 20,23,24,50

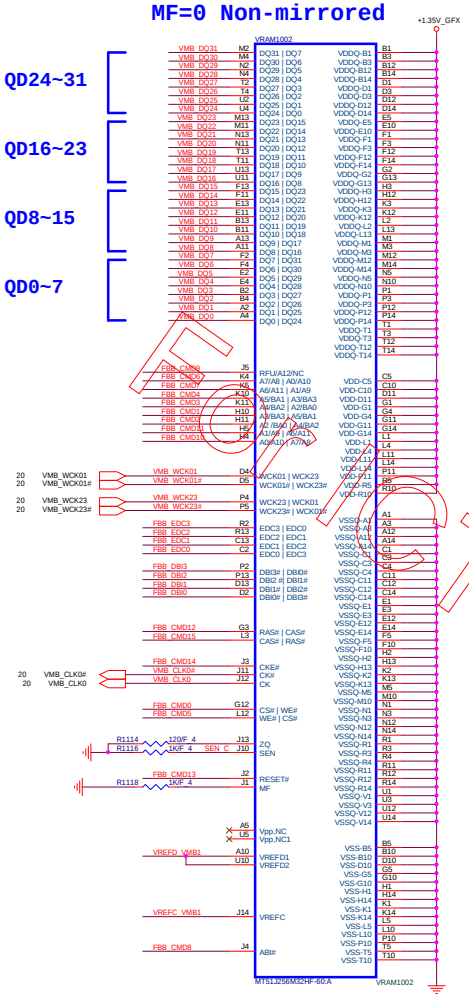
20 VMB_DQ[63:0] VMB_DQ[63:0]
20 FBB_CMD[31:0] FBB_CMD[31:0]
20 FBB_DBI[7:0] FBB_DBI[7:0]
20 FBB_EDC[7:0] FBB_EDC[7:0]

N16S-GTR-B: unstuff VRAM
N16P-GX/GT/N16E-GR: stuff VRAM (Default)

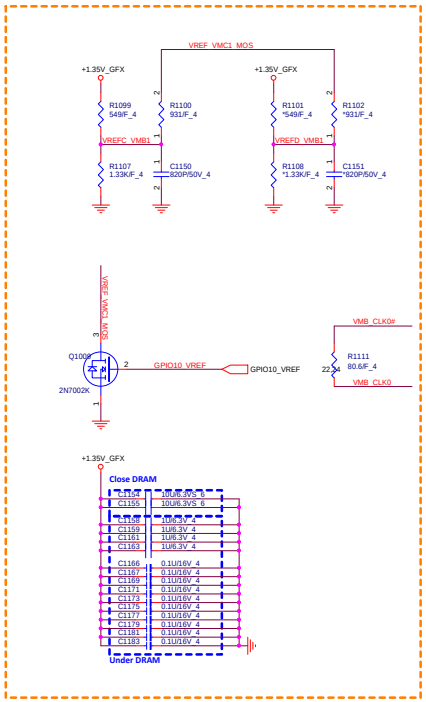
MF=0 Non-mirrored

QD24~31
QD16~23
QD8~15
QD0~7

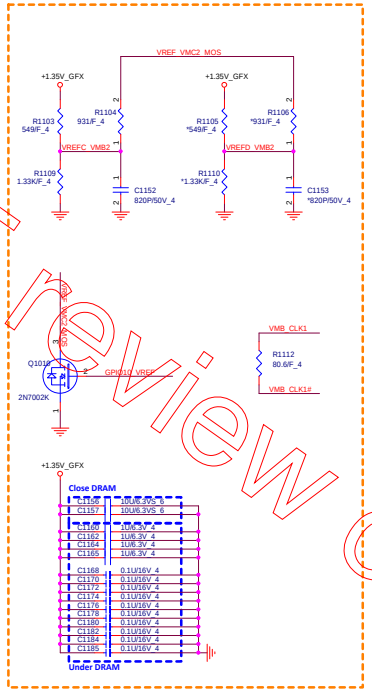
VRAM1002



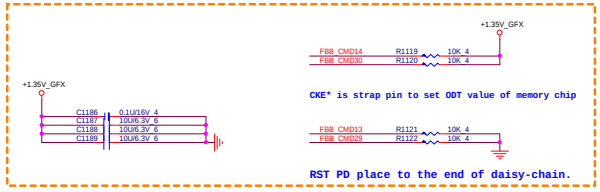
N16S-GTR-B: unstuff VRAM
N16P-GX/GT/N16E-GR: stuff VRAM (Default)



N16S-GTR-B: unstuff VRAM
N16P-GX/GT/N16E-GR: stuff VRAM (Default)



N16S-GTR-B: unstuff VRAM
N16P-GX/GT/N16E-GR: stuff VRAM (Default)

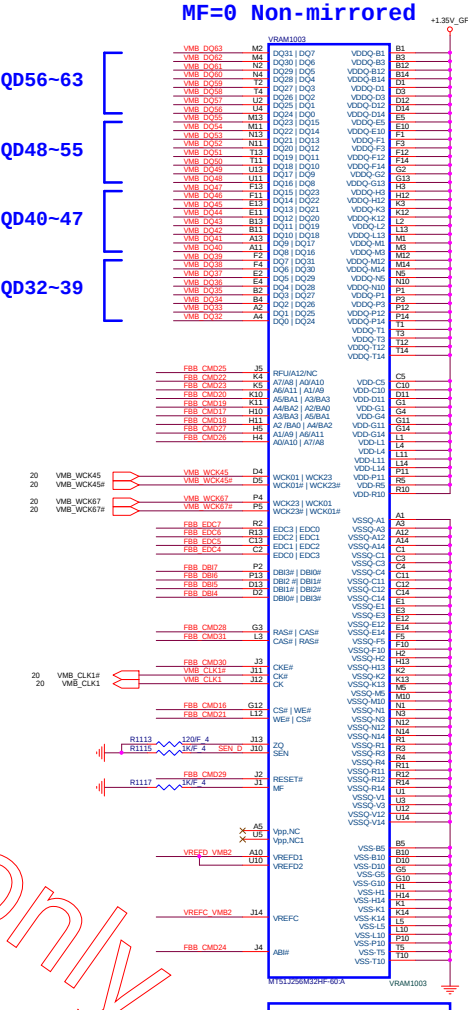


N16S-GTR-B: unstuff VRAM
N16P-GX/GT/N16E-GR: stuff VRAM (Default)

MF=0 Non-mirrored

QD56~63
QD48~55
QD40~47
QD32~39

VRAM1003



GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

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Quanta Computer Inc.
Size | Document Number | Rev
N16P-GX/GT GDDR5 VRAM 2/2 | 1A
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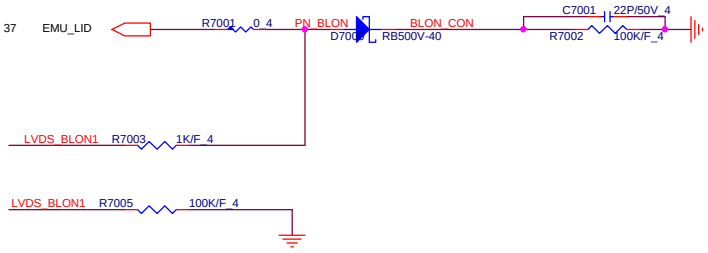
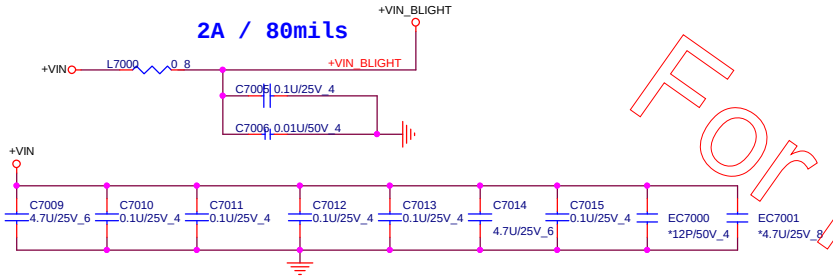
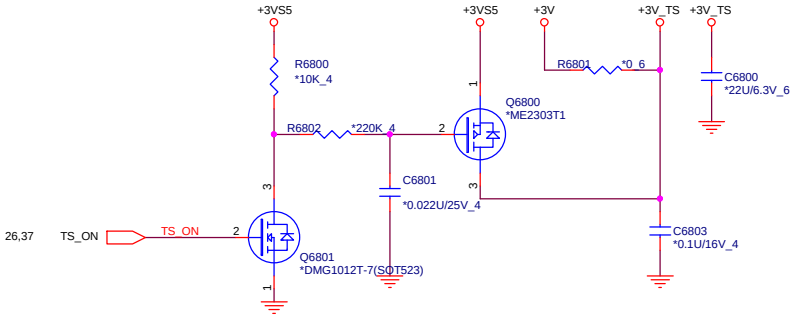
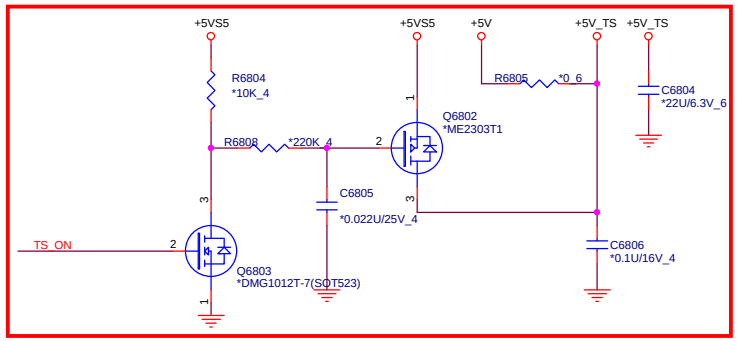
LID Switch





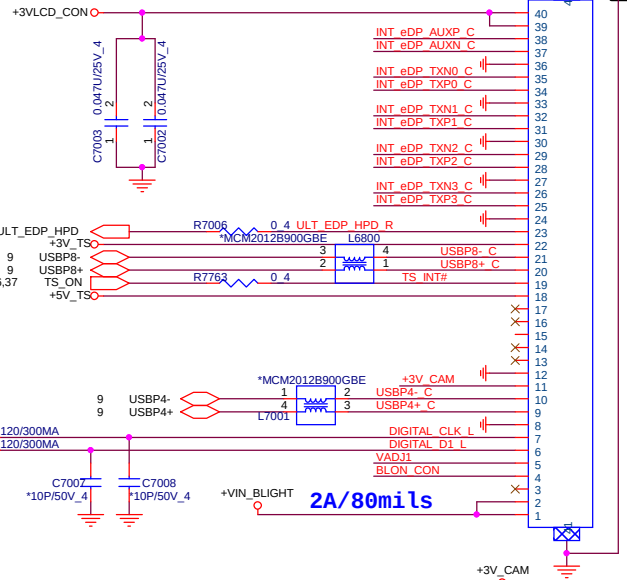
Touch screen





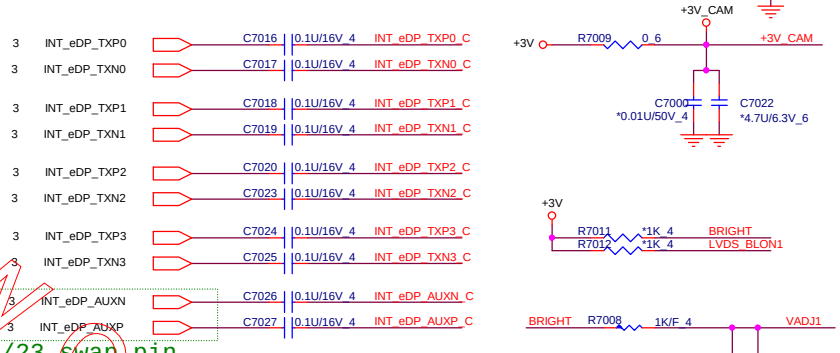
eDP Conn.

GS12401-1011-9H
51519-0400t-v02-40p-l
DFFC40FR081
CN7000

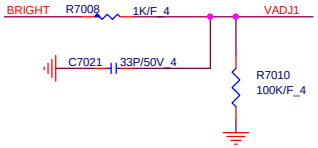


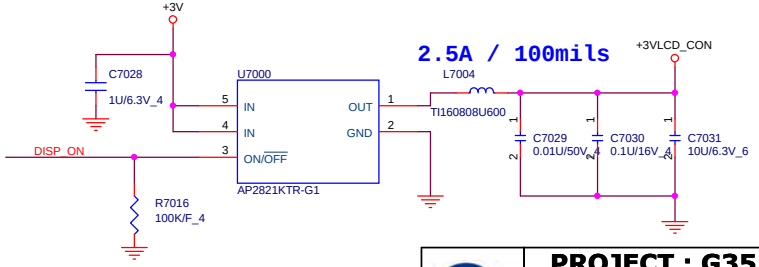
10/01 modify

TS USB Interface



9/23 swap pin





5,9,10,11,12,13,14,16,17,18,19,22,27,28,29,30,32,33,34,35,36,37,38,43,46,49 +3V
5,10,30,33,37,38,40,41 +3VPCU
27,28,29,31,32,38,46,49 +5V
38,39,40,41,42,43,44,45,46,47,48,49,50 +VIN

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Quanta Computer Inc.

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Custom	LCD CONN/LID/CAM	1A
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5,9,10,11,12,13,14,16,17,18,19,22,26,28,29,30,32,33,34,35,36,37,38,43,46,49 +3V

26,28,29,31,32,38,46,49 +5V

11/26 change to 6.8 ohm for NV suggest

TX2_HDMI+	6.8/F_4	R8574		TX2_HDMI+CN
TX2_HDMI-	6.8/F_4	R8571		TX2_HDMI-CN
TX1_HDMI+	6.8/F_4	R8573		TX1_HDMI+CN
TX1_HDMI-	6.8/F_4	R8576		TX1_HDMI-CN
TX0_HDMI+	6.8/F_4	R8572		TX0_HDMI+CN
TX0_HDMI-	6.8/F_4	R8569		TX0_HDMI-CN
TXC_HDMI+	6.8/F_4	R8575		TXC_HDMI+CN
TXC_HDMI-	6.8/F_4	R8570		TXC_HDMI-CN

11/04 modify for HDMI2.0

EMI Solution

TX2_HDMI+	R7716	120/F_4	TX2_HDMI-
TX1_HDMI+	R7717	120/F_4	TX1_HDMI-
TX0_HDMI+	R7719	120/F_4	TX0_HDMI-
TXC_HDMI+	R7722	120/F_4	TXC_HDMI-

11/04 modify for HDMI2.0

+3V_AON, Q7704 2N7002K, DGPU_CL_HDMIP

R7727	499/F_4	TX2_HDMI+	
R7728	499/F_4	TX2_HDMI-	
R7729	499/F_4	TX1_HDMI+	
R7730	499/F_4	TX1_HDMI-	
R7733	499/F_4	TX0_HDMI+	
R7734	499/F_4	TX0_HDMI-	
R7737	499/F_4	TXC_HDMI+	
R7738	499/F_4	TXC_HDMI-	

R7741 1M_4, C7728 0.1U/16V_4

11/03 modify for HDMI2.0

21 GPU_D0	C7723	0.1U/16V_4		TX0_HDMI+
21 GPU_D0#	C7724	0.1U/16V_4		TX0_HDMI-
21 GPU_D1	C7721	0.1U/16V_4		TX1_HDMI+
21 GPU_D1#	C7722	0.1U/16V_4		TX1_HDMI-
21 GPU_D2	C7725	0.1U/16V_4		TX2_HDMI+
21 GPU_D2#	C7726	0.1U/16V_4		TX2_HDMI-
21 GPU_CLK	C7727	0.1U/16V_4		TXC_HDMI+
21 GPU_CLK#	C7729	0.1U/16V_4		TXC_HDMI-
21 GPU_DDCCLK				
21 GPU_DDCDATA				

+3V, C8625 0.1U/16V_4, U8503 TC7SH08FU(F)

19,22 PEGX_RST# → HDMI_HPD_CON → HDMI_HPD_GPU → HDMI_HPD_GPU 22

11/04 modify for HDMI2.0

HDMI SMBus Isolation

Close to HDMI connector

+3V, R7745 1M_4, Q7700 2N7002

13 HDMI_HPD_CON → HDMI_HPD_CON → HDMI_HPD

R7747 20K/F_4

11/03 modify for HDMI2.0

+3V_AON, R7748 10K_4, Q7705, R7750 10K_4, 2N7002KDW

GPU_DDCCLK → HDMI_SCLK

GPU_DDCDATA → HDMI_SDATA

ESD

U7701 *CPDA10R5V0P-HF

TX0_HDMI-CN	1	IN1	NC 10	TX0_HDMI-CN
TX0_HDMI+CN	2	IN2	NC 9	TX0_HDMI+CN
	3	GND	GND 8	
TXC_HDMI-CN	4	IN3	NC 7	TXC_HDMI-CN
TXC_HDMI+CN	5	IN4	NC 6	TXC_HDMI+CN

U7702 *CPDA10R5V0P-HF

TX1_HDMI-CN	1	IN1	NC 10	TX1_HDMI-CN
TX1_HDMI+CN	2	IN2	NC 9	TX1_HDMI+CN
	3	GND	GND 8	
TX2_HDMI-CN	4	IN3	NC 7	TX2_HDMI-CN
TX2_HDMI+CN	5	IN4	NC 6	TX2_HDMI+CN

1125 Reserve ESD protection component

1125 SWAP

D7701 BAT54AW-L, +5V_HDMIC, 5V_HSMBCK R7751 2.2K_4, 5V_HSMBDT R7752 2.2K_4, C7730 *10P/50V_4, C7731 *10P/50V_4, F7701 FUSE1A6V_POLY, +5V, 40 mils

VC7702 *TVM0G5R5M220R, C7740 0.1U/16V_4, VC7703 *TVM0G5R5M220R, C7741 220P/50V_4

CN7701 HDMI CONN

TX2_HDMI+CN	1	SHELL1	20
	2	D2+	
TX2_HDMI-CN	3	D2 Shield	
TX1_HDMI+CN	4	D2-	
	5	D1+	
TX1_HDMI-CN	6	D1 Shield	
TX0_HDMI+CN	7	D1-	
	8	D0+SHELL2	23
TX0_HDMI-CN	9	D0 Shield	
TXC_HDMI+CN	10	D0-	
	11	CK+	
TXC_HDMI-CN	12	CK Shield	
	13	CK- SHELL2	22
	14	CE Remote	
	15	NC	
HDMI_SCLK	16	DDC CLK	
HDMI_SDATA	17	DDC DATA	
	18	GND	
+5V_HDMIC	19	+5V	
		HP DET	
HDMI_HPD		SHELL2	21

0925 Del Net HDMI_DET_C

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	27 -- HDMI/HDMI REDRIVER	1A
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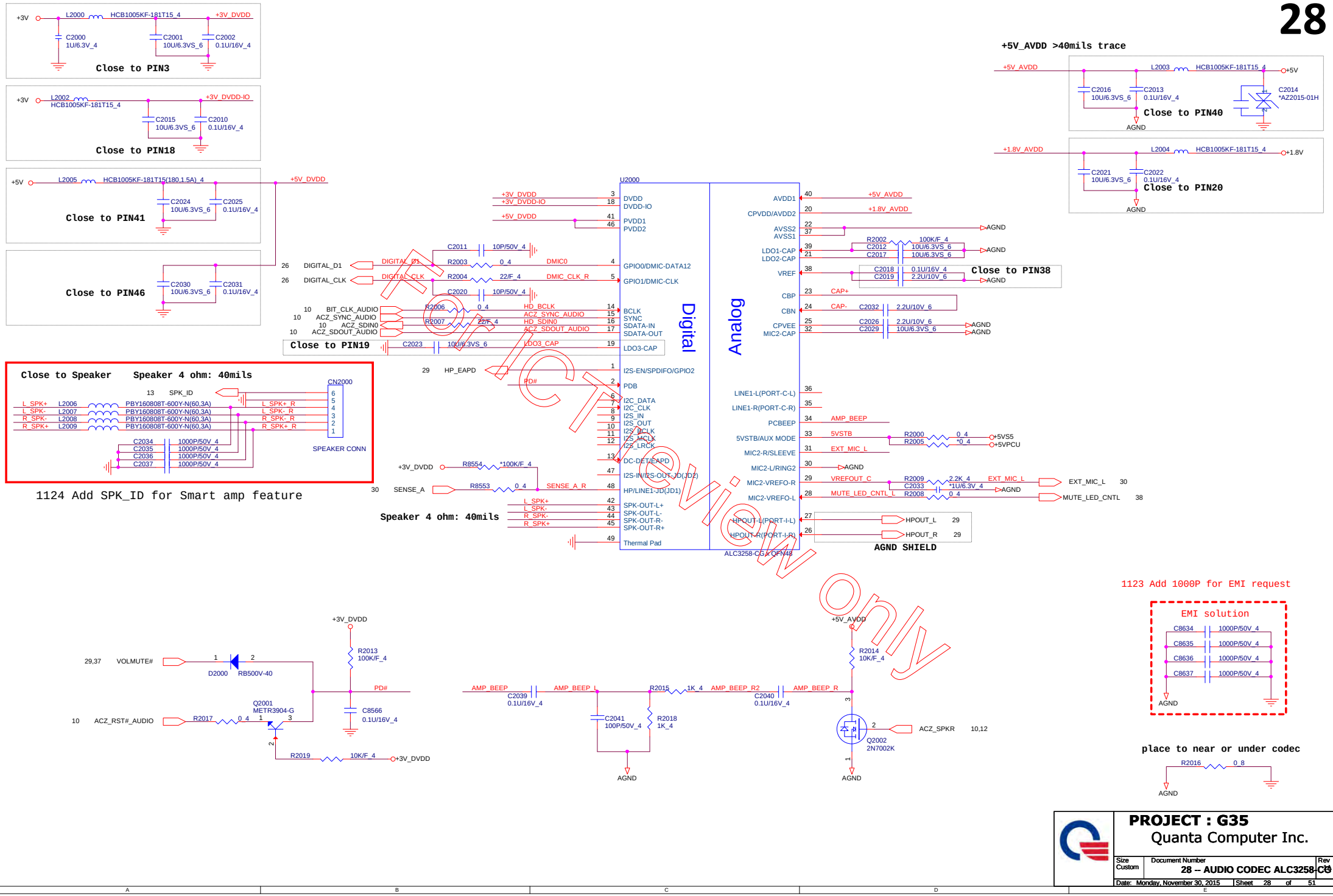

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	28 – AUDIO CODEC ALC3258-CG	1A

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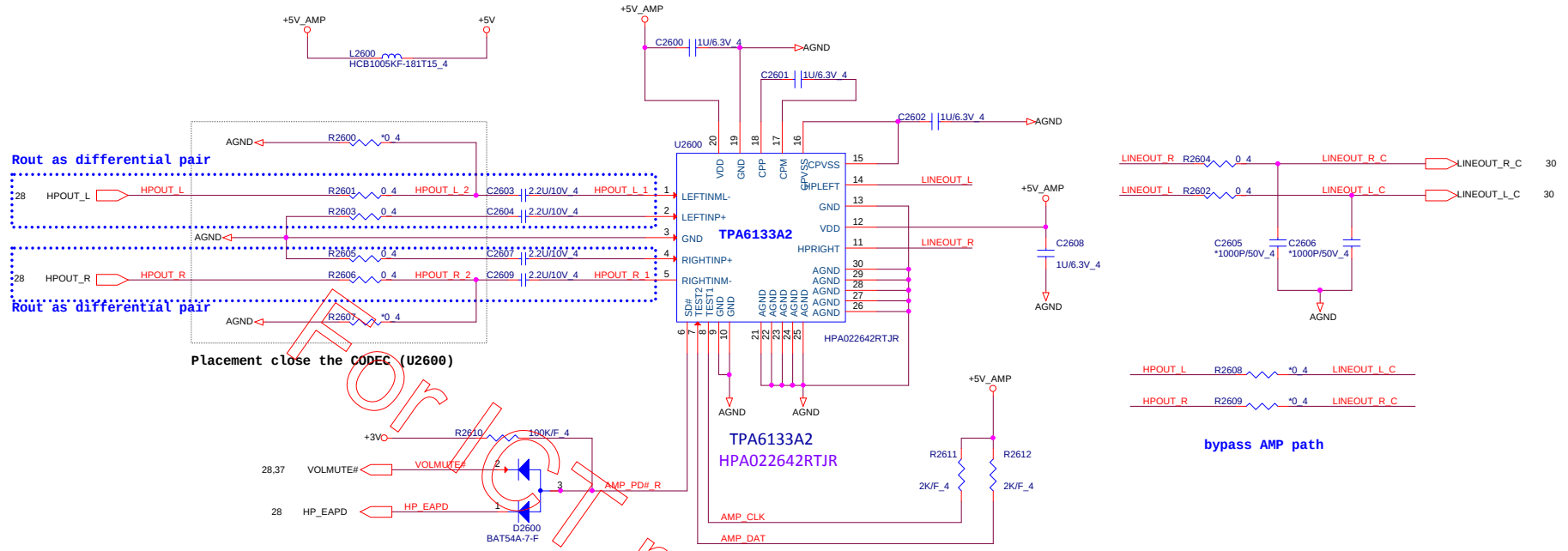
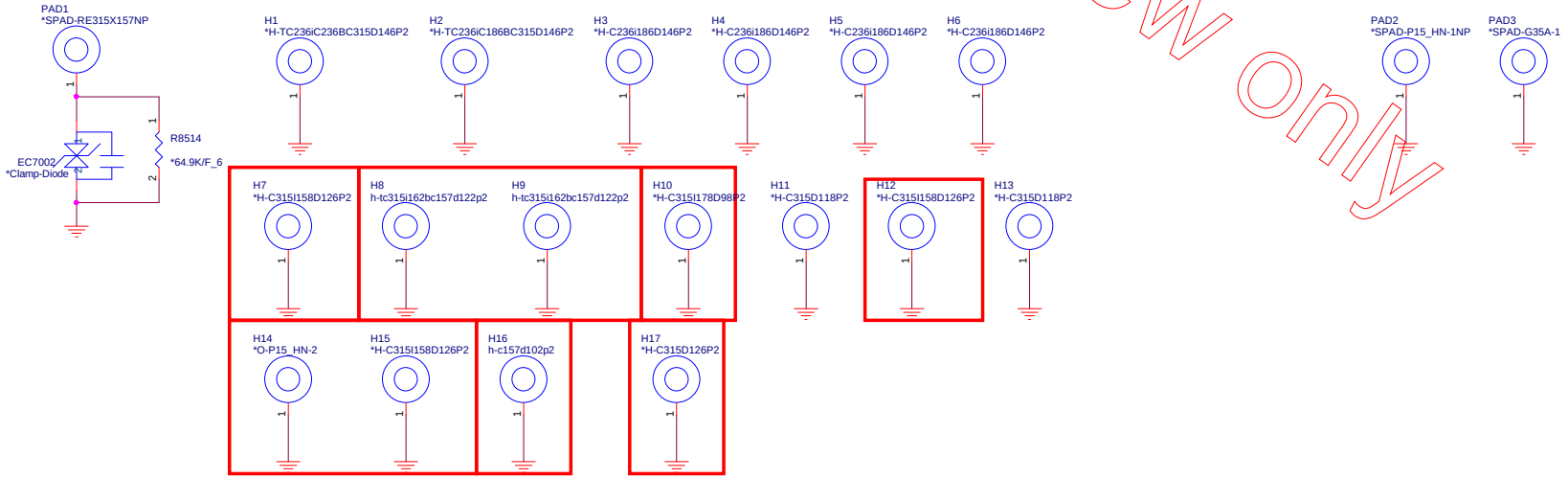
Head Phone out



HOLE



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Size Custom	Document Number 29-- HP AMP HPA022642RTJR	Rev 1A
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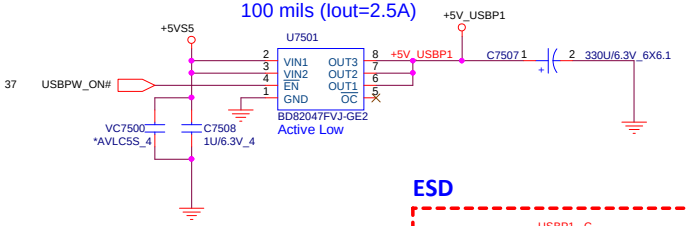
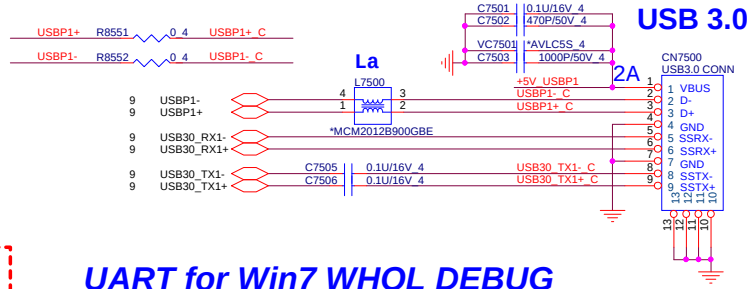
USB 2.0/3.0 Combo

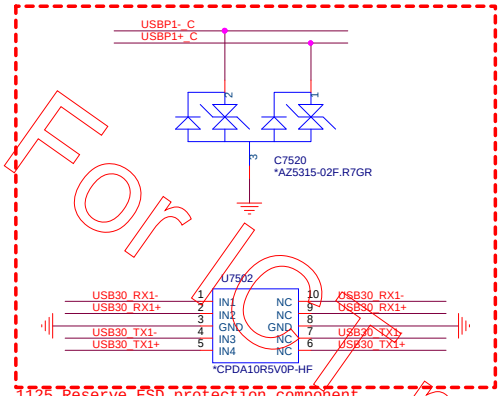
100 mils (Iout=2.5A)



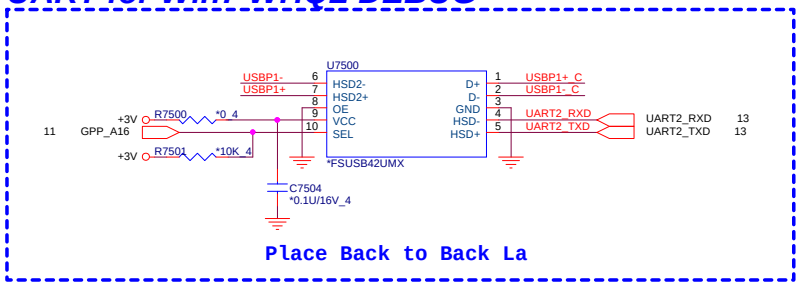
USB 3.0



ESD

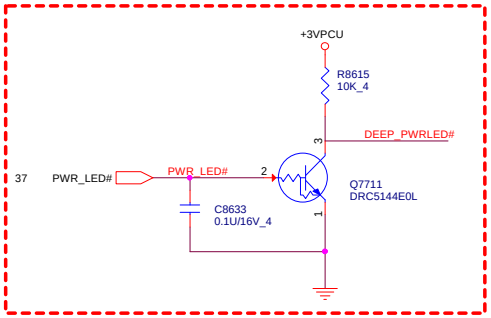


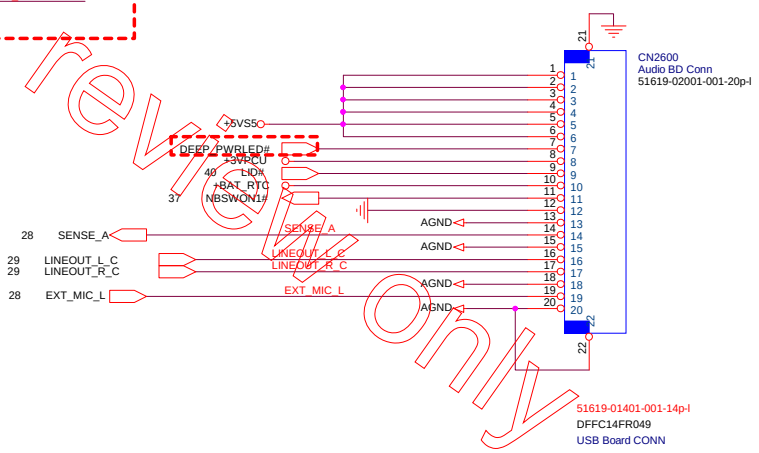
UART for Win7 WHQL DEBUG

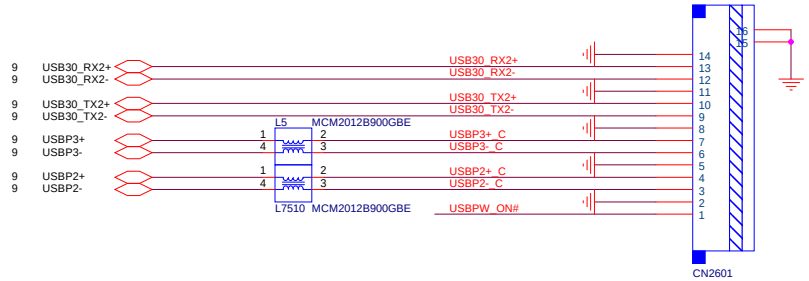


Daughter Board

1123 Add PWR LED MOS Circuit







PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	30 – USB3.0/DB	1A

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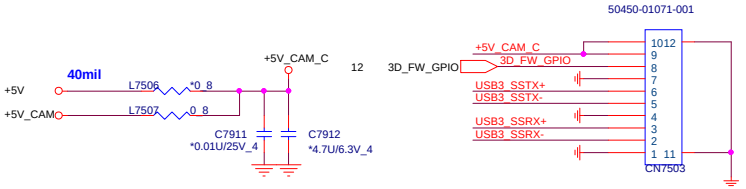
10/08 3D Camera MIC combine in LCD CONN

3D Camera Conn.



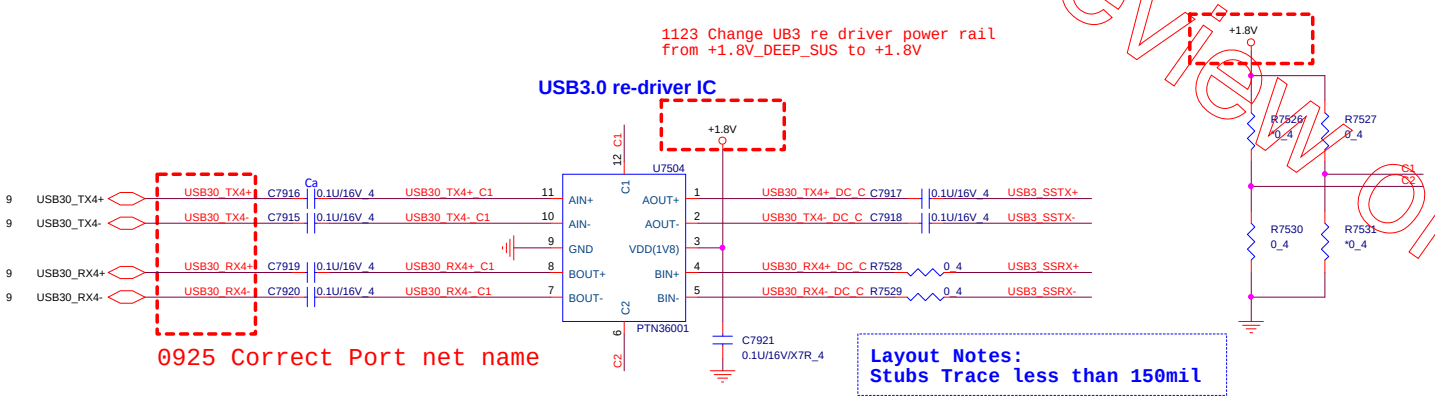
USB3.0

USB3.0 Re-driver IC

1123 Change UB3 re driver power rail
from +1.8V_DEEP_SUS to +1.8V

1123 Change UB3 re driver power rail
from +1.8V_DEEP_SUS to +1.8V

USB3.0 re-driver IC



0925 Correct Port net name

Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ[1]	DE[2]	OS[2]
H	Long	H	9 dB	–5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	–3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

Table 5. C2 pin controls long/medium/short traces

State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ[1]	DE[2]	OS[2]
H	Long	H	9 dB	–5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	–3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

Layout Notes:
Stubs Trace less than 150mil

28,40,41,46,51 +5VPCU
5,10,30,33,37,38,40,41 +3VPCU
28,47 +1.8V

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Custom	31 – 3D CAM/REDRIVER	1A

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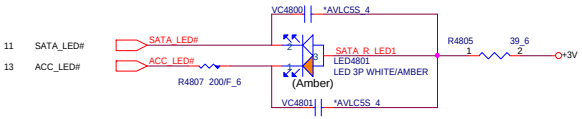
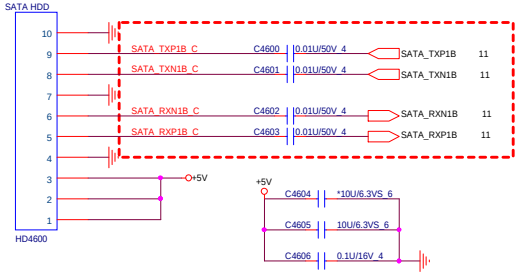
+3V
+5V
+3VPCU

SATA LED



HDD



PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
C	32 -- HDD/ODD	1A

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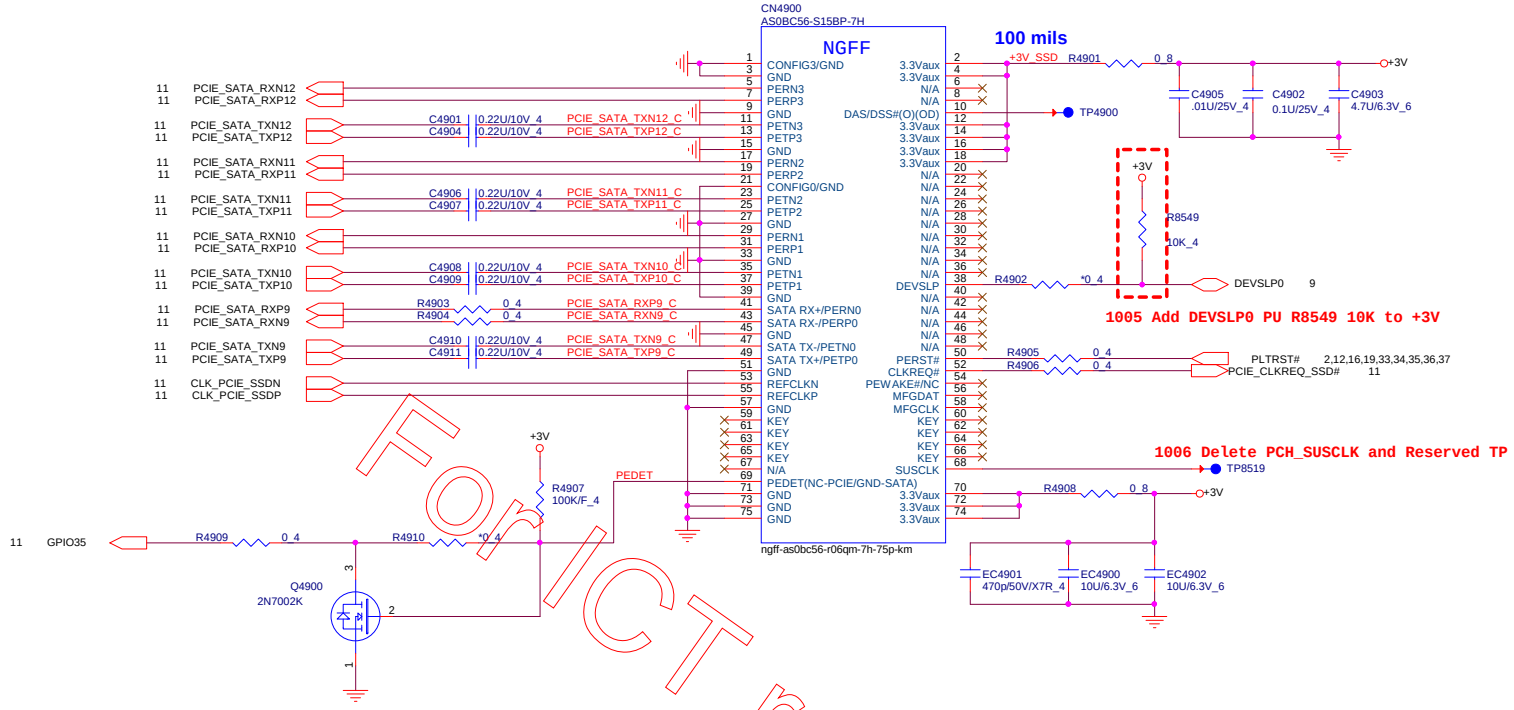
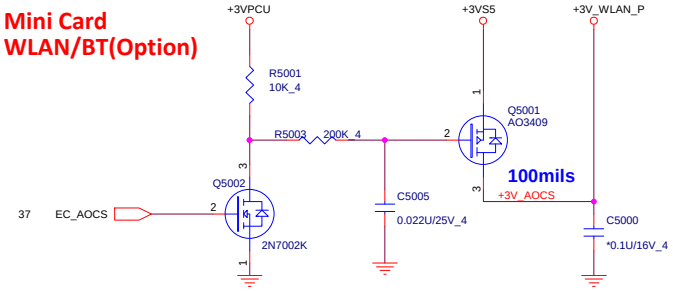
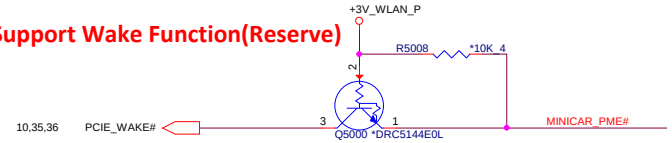
SSD

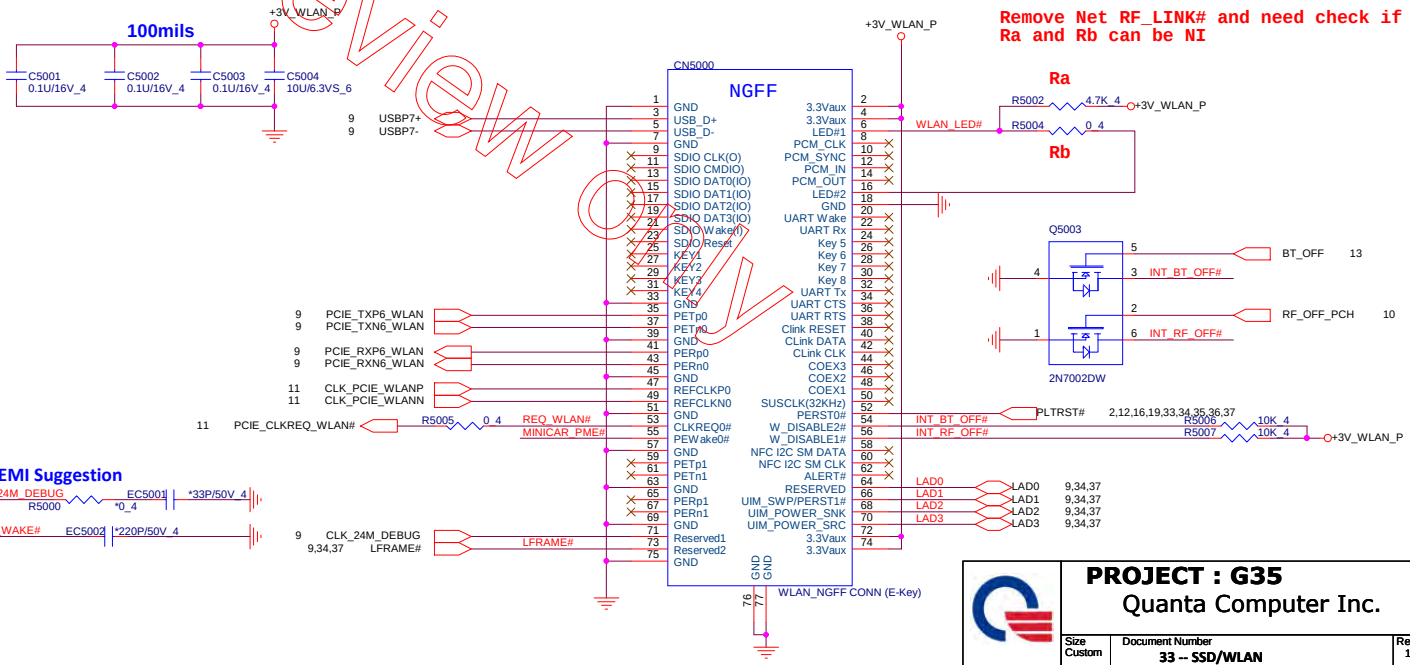


Mini Card WLAN/BT(Option)



Support Wake Function(Reserve)





For EMI Suggestion

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Size: Custom	Document Number: 33 -- SSD/WLAN	Rev: 1A
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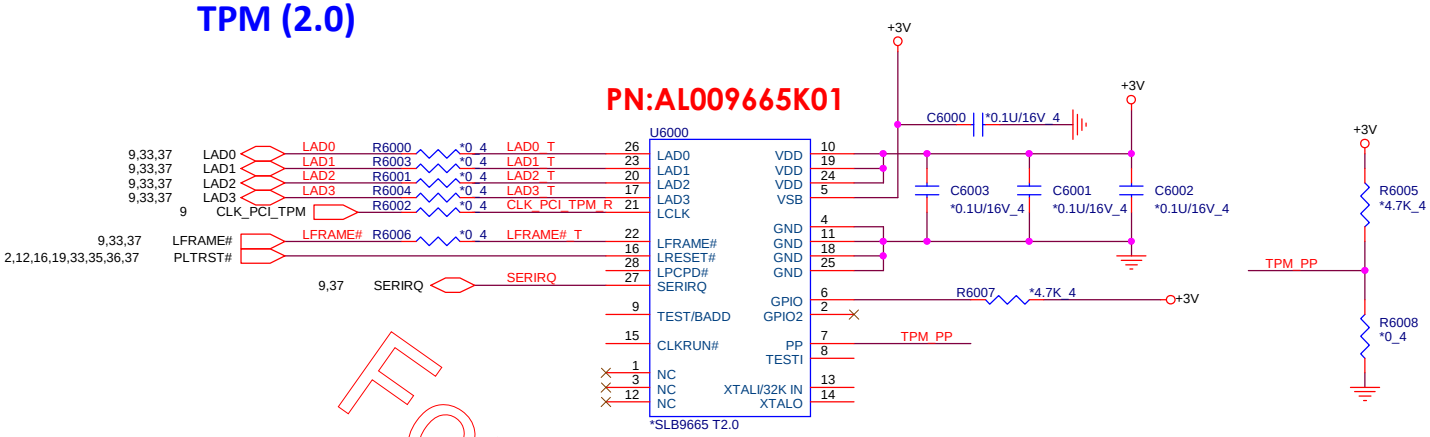
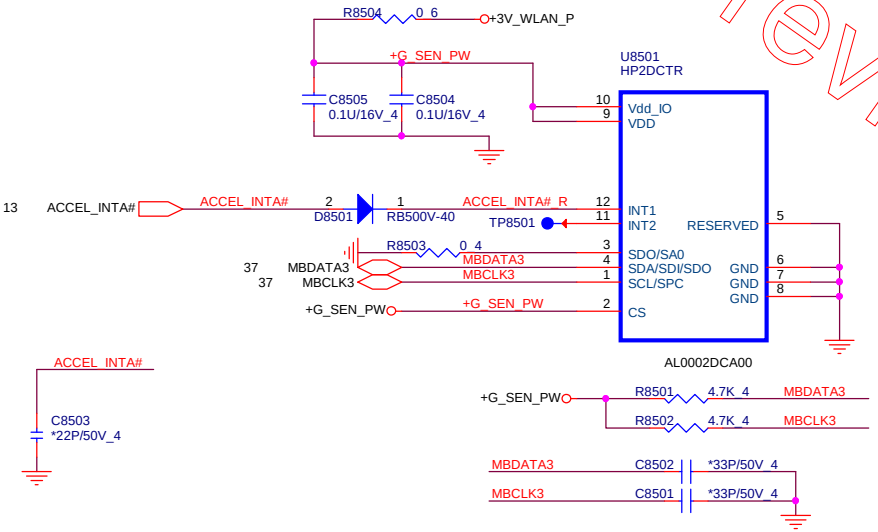
TPM (2.0)

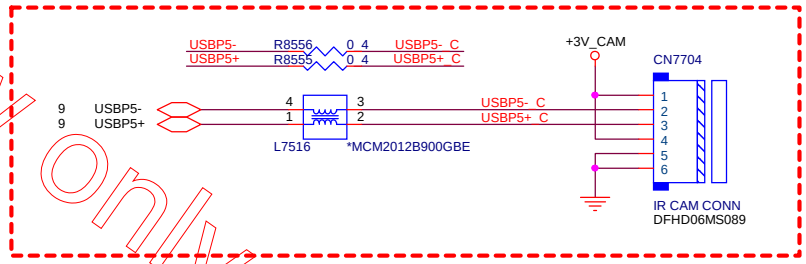
PN:AL009665K01



Accelerometer Sensor



IR CAM



1015 Add IR CAM circuit

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Quanta Computer Inc.			
B	34 -- TPM/Sensor	Document Number	1A Rev
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Date:		Sheet	of

LAN & RJ45

For SWR mode support RTL8111HSH/RTL8107ESH

Stuff La, Ca ,Cb

* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 3, 22, 8 , 30

* Place Cg,Ch for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 22(reserved)

Power trace Layout 寬度> 60mil

>60mil >60mil

+1.05V_LAN_REGOUT L3000 4.7UH,+-20%,650MA_1210 La

Ca C3004 0.1U/16V_4

Cb C3005 4.7U/6.3VS_4

PIN3 Cc C3006 0.1U/16V_4

PIN8 Cd C3007 0.1U/16V_4

PIN30 Ce C3008 0.1U/16V_4

PIN22 Cf C3009 0.1U/16V_4

PIN22 Cg C3010 1U/6.3V_4

PIN22 Ch C3011 0.1U/16V_4

+1.05V_LAN

LAN_XTAL1 R3000 10_4 XTAL1

Y3000 25MHZ +-10PPM

XTAL2

C3000 10P/50V_4

C3001 10P/50V_4

1028 Change Y3000 footprint to xtl-2x1_6-1_35x1_05

R3001 2.49K/F_4

+3V_LAN

LAN_AMBLED# TP3000

LAN_LED1 TP3001

LED2 TP3002

+1.05V_LAN

LAN_AMBLED# Ra R3003 0_4 LAN_WLED#

R3004 *0_4 LAN_WLED# Rb

For GbE

* Place Ra

For 10/100

* Place Rb

+3V R3002 1K_4 ISOLATEB R3005 15K/F_4

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

U3000

Please add 9 GND VIAs connection with thermal PAD

GND

MDIP0 MDIN0 AVDD10(NC) MDIP1 MDIN1 MDIP2(NC) MDIN2(NC) AVDD10

RTL8107ESH-CG

REGOUT(NC) VDDREG(VDD33) DVDD10(NC) LANWAKEB ISOLATEB PERSTB HSON HSOP

AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 LED0 LED1/GPO LED2(LED1)

MDIP3(NC) MDIN3(NC) AVDD33(NC) CLKREQB HSIP HSIN REFCLK_P REFCLK_N

RTL8111HSH-CG

+1.05V_LAN_REGOUT +3V_LAN +1.05V_LAN

PCIE_WAKE# R R3006 0_4 PCIE_WAKE# 10,33,36

PLTRST# 2,12,16,19,33,34,36

PCIE_RXN7_LAN_L C3002 0.1U/16V_4 PCIE_RXN7_LAN 9

PCIE_RXP7_LAN_L C3003 0.1U/16V_4 PCIE_RXP7_LAN 9

0929 correct port from 9 to 7

For GbE

* Place RTL8111HSH-CG

For 10/100

* Place RTL8107ESH-CG

MDI3+ MDI3-

PCIE_CLKREQ_LAN# 11

CLK_PCIE_LANN CLK_PCIE_LANP PCIE_TXN7_LAN PCIE_TXP7_LAN

CLK_PCIE_LANN 11

CLK_PCIE_LANP 11

PCIE_TXN7_LAN 9

PCIE_TXP7_LAN 9

0929 Correct port from 9 to 7

+3VLANVCC 360_4 R3017 LED3000 3P AMBER LED LAN_AMBLED#

VC3000 *AVLC5S_4

+3VLANVCC 360_4 R3018 LED3001 3P WHITE LED LAN_WLED#

VC3001 *AVLC5S_4

For 10/100 stuff only Close RJ45

MDI3-_1 R3007 *0_4

MDI3+_1 R3008 *0_4

MDI2-_1 R3009 *0_4

MDI2+_1 R3010 *0_4

C3012 *68P/50V_4

* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S) & RTL8107E(S)

* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

+3VLANVCC +3V_LAN

PIN11 C3013 0.1U/16V_4 Cj

PIN32 C3014 0.1U/16V_4 Ck

PIN11 C3015 *4.7U/6.3VS_4 Cm

PIN32 C3016 *4.7U/6.3VS_4 Cn

PIN23 C3017 4.7U/6.3VS_4 Co

PIN23 C3018 0.1U/16V_4 Cp

For SWR mode support RTL8111HSH/RTL8107ESH

Stuff Co, Cp

For 10/100：Ua

For Giga：Ub

Ua U3001

MDI1+_1 MDI1-_1 LAN_MCTG1 MDI0+_1 MDI0-_1 LAN_MCTG0

TD+ TD- CT RD+ RD- CT GND

TX+ CMT TX- RX- CT RX+

MDI1+ TRA_V_DAC MDI1- MDI0- TRA_V_DAC MDI0+

C3022 0.01U/50V_4

*NS681684

DB0LE6LAN20

1st source：NS681684 DB0LE6LAN20

2nd source：N-3110M DB0Y11LAN00

Ub U3002

MDI2+ MDI2- MDI3- MDI3+ MDI0- MDI0+ MDI1- MDI1+

TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4-

MX1+ MX1- MX2+ MX2- MX3+ MX3- MX4+ MX4-

MDI2+_1 MDI2-_1 MDI3-_1 MDI3+_1 MDI0-_1 MDI0+_1 MDI1-_1 MDI1+_1

TRA_V_DAC TRA_V_DAC TRA_V_DAC TRA_V_DAC TRA_V_DAC

TCT1 TCT2 TCT3 TCT4 GND

MCT1 MCT2 MCT3 MCT4 MCT1

LAN_MCTG0 Ra R3011 75/F_4

LAN_MCTG1 Rb R3012 75/F_4

LAN_MCTG2 Rc R3014 75/F_4

LAN_MCTG3 Rd R3016 75/F_4

NS892407

For GiGA

BOT:GST5009B LF,DB0Z06LAN00

FCE :NS892407 ,DB0LL1LAN00

For 10/100：Ra,Rb

For Giga：Ra,Rb,Rc,Rd

C3020 10P/3KV_1808

RJ45

CN3000

MDI3-_1 MDI3+_1 MDI1-_1 MDI2-_1 MDI2+_1 MDI1+_1 MDI0-_1 MDI0+_1

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+

GND2 GND1

R3013 0_6

R3015 0_6

RJ45_CONN

DFTJ08FR335

rj45-c10220-10833-I-8p

5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,36,37,38,43,46,49

46 +3V +3VLANVCC

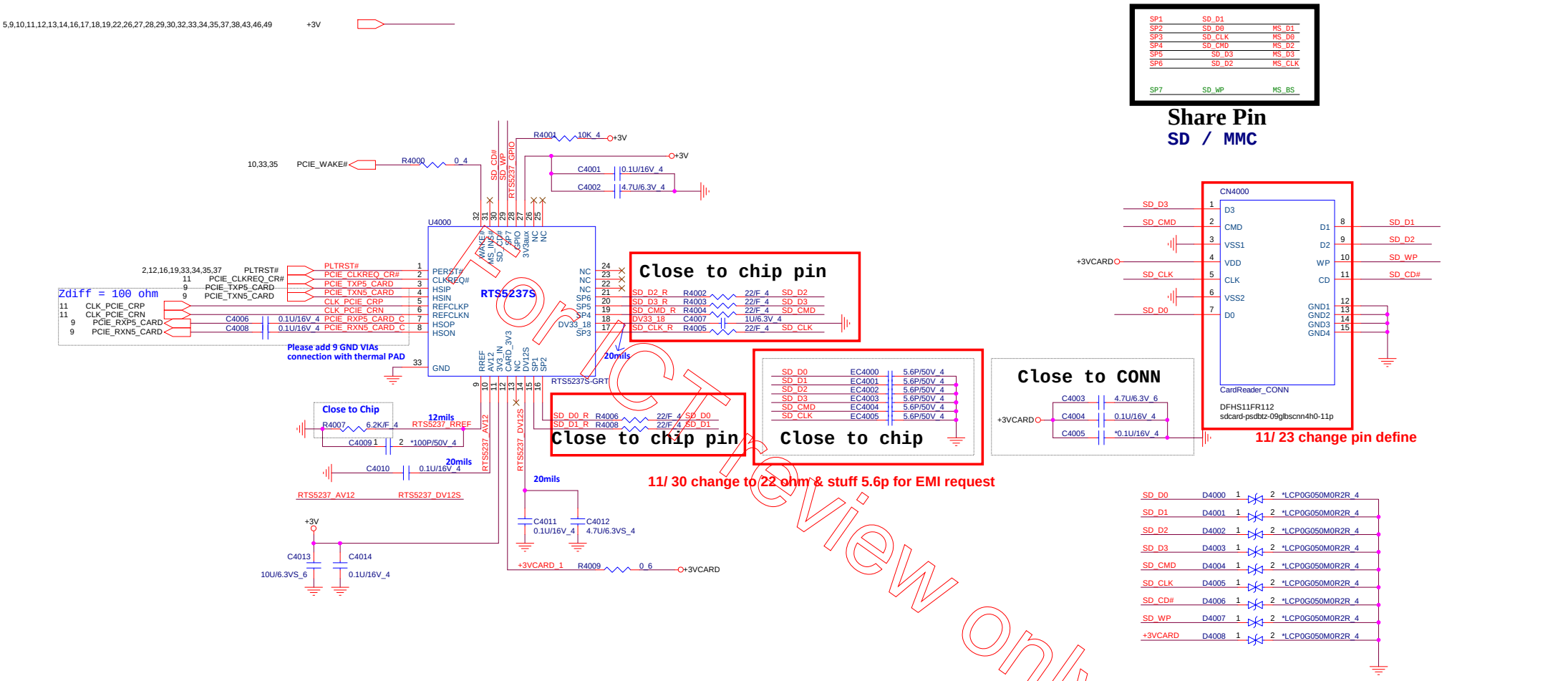
PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
Custom	35 – LAN RTL8107ESH-CG/RJ45	1A

Date: Monday, November 30, 2015 Sheet 35 of 51

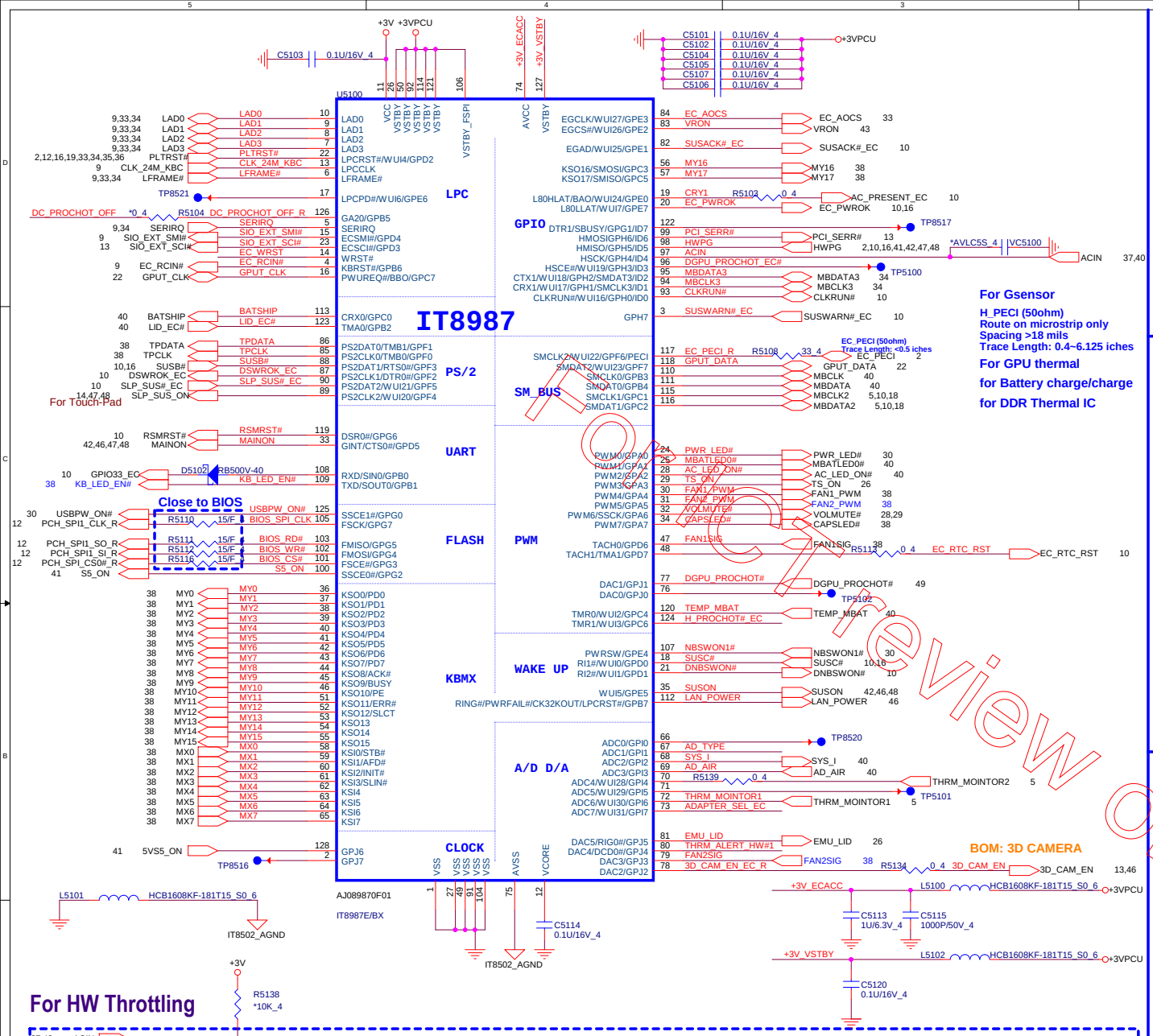
RTS5237S PCIE CARD READER Controller

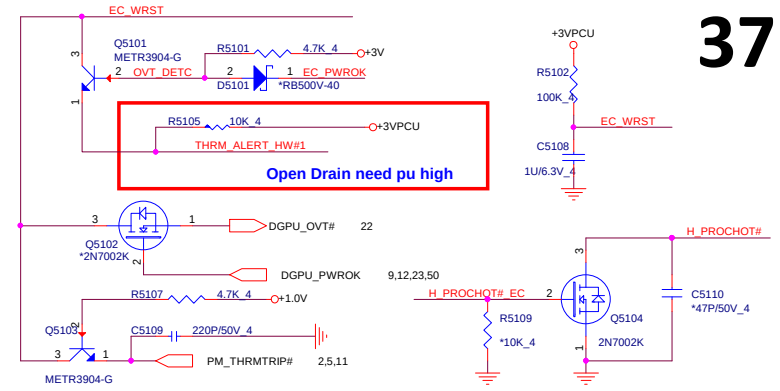


PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	36 – CR RTS5237S/CR SOCKET	1A

Date: Monday, November 30, 2015 Sheet 36 of 51

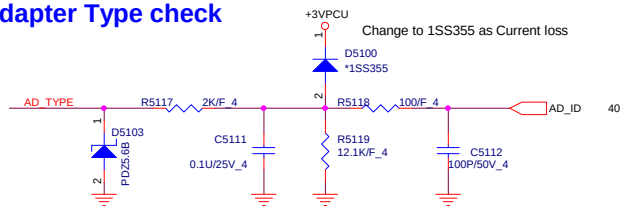


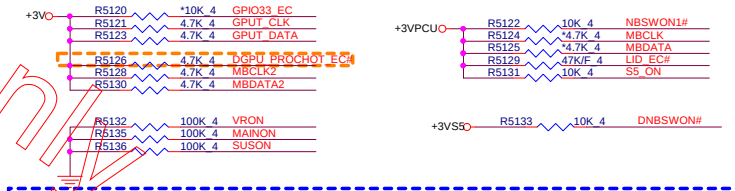


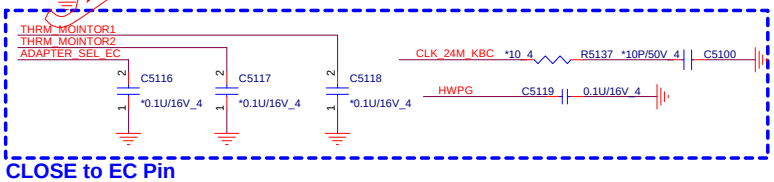
Adapter select for EC

	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	2.42V	
120W	10K(CS31002FB26)	12.1K(CS31212FB28)	1.8V	DIS
90W	10K(CS31002FB26)	6.2K(CS26202FB17)	1.26V	UMA
65W	10K(CS31002FB26)	2.2K(CS22202FB08)	0.59V	
45W	NC	10K(CS31002FB26)	0V	

Adapter Type check





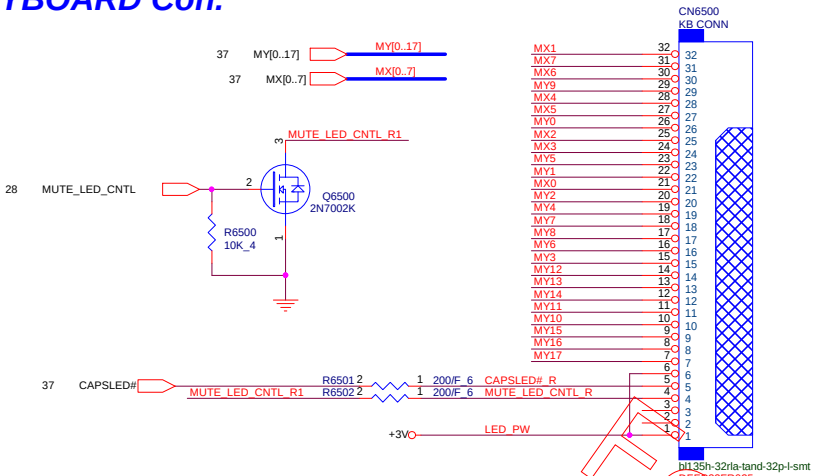


5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,38,43,46,49 +3V
10,12,14,16,26,33,41,42,46,47,48,51 +3VS5
5,10,30,33,38,40,41 +3VPCU

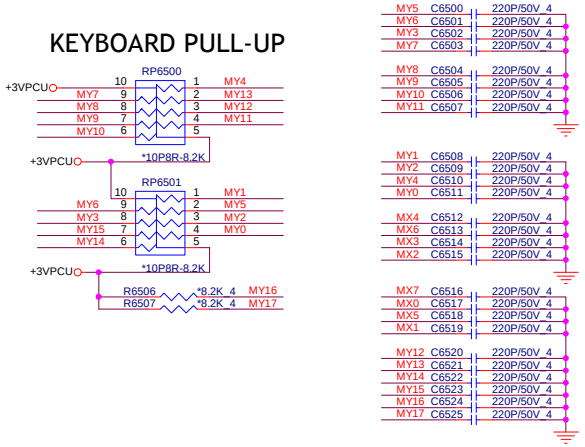
PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	37 -- EC (IT8987)	1A
Date: Monday, November 30, 2015	Sheet 37of 51	

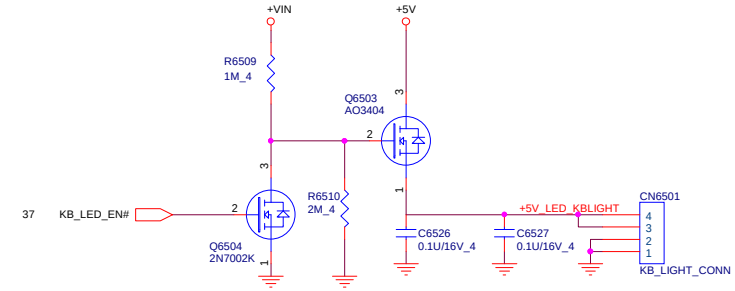
KEYBOARD Con.



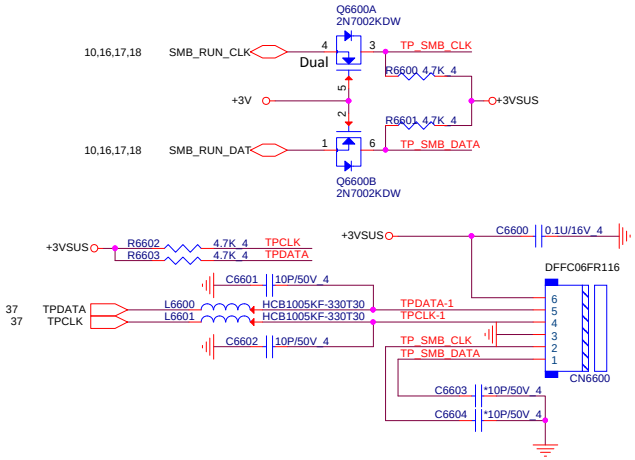
KEYBOARD PULL-UP



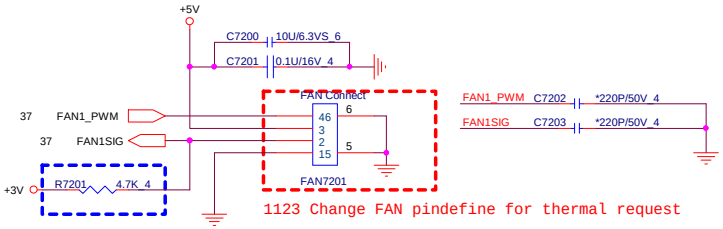
KB LIGHT CONN

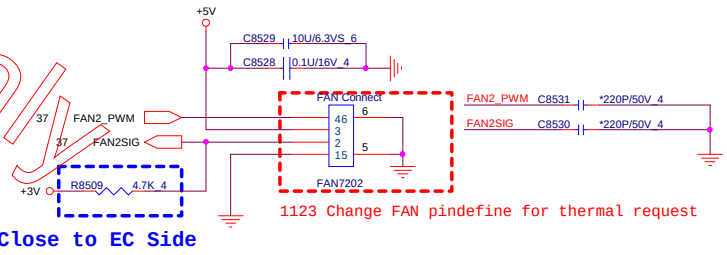


Touch Pad Connector

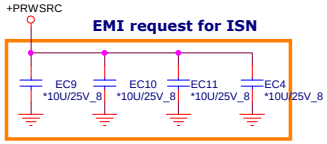


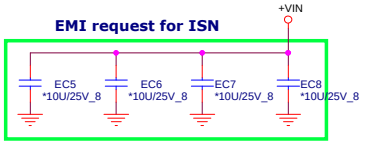
FAN





PROJECT : G35		
Quanta Computer Inc.		
Size: Custom	Document Number: 38 -- KB/TP/FAN/HOLE	Rev: 1A
Date: Monday, November 30, 2015	Sheet 38 of 51	



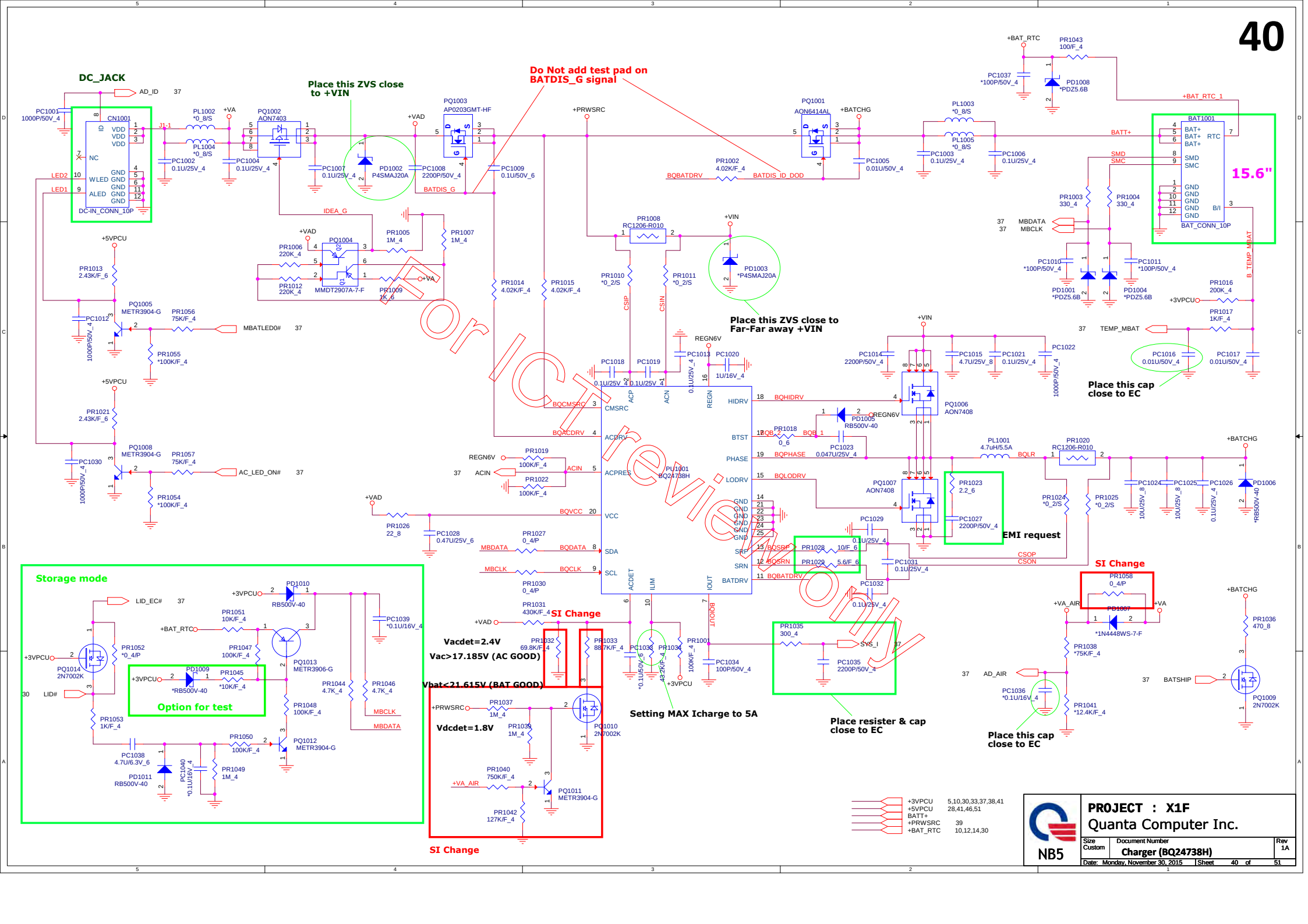


NB5

PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**RF Solution**	1A

Date: Monday, November 30, 2015 | Sheet 39of 51


DC_JACK
Place this ZVS close to +VIN
Do Not add test pad on BATDIS_G signal
Place this ZVS close to Far-Far away +VIN
Place this cap close to EC
EMI request
SI Change
Storage mode
Option for test
Vacdet=2.4V
Vac>17.185V (AC GOOD)
Vbat<21.615V (BAT GOOD)
Vdcdet=1.8V
Setting MAX Icharge to 5A
Place resister & cap close to EC
Place this cap close to EC
15.6"
For ICT review only
+3VPCU 5,10,30,33,37,38,41
+5VPCU 28,41,46,51
BATT+
+PRWSRC 39
+BAT_RTC 10,12,14,30
PROJECT : X1F
Quanta Computer Inc.
NB5
Charger (BQ24738H)
Rev 1A
Date: Monday, November 30, 2015
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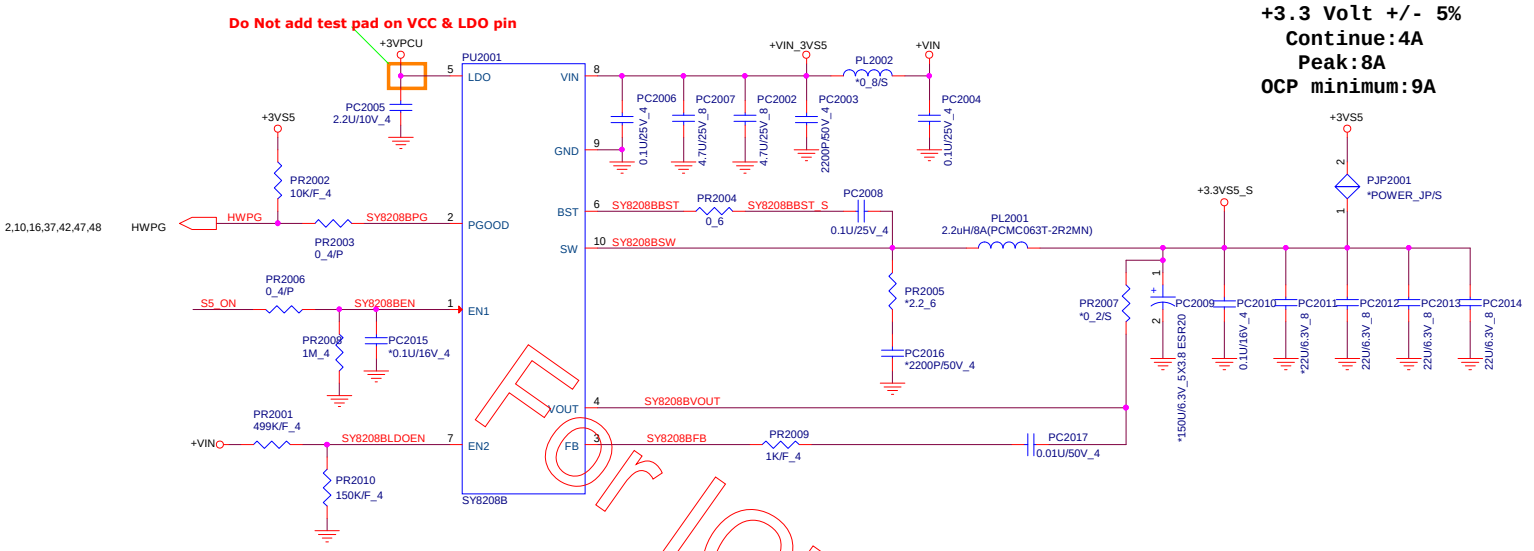


USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

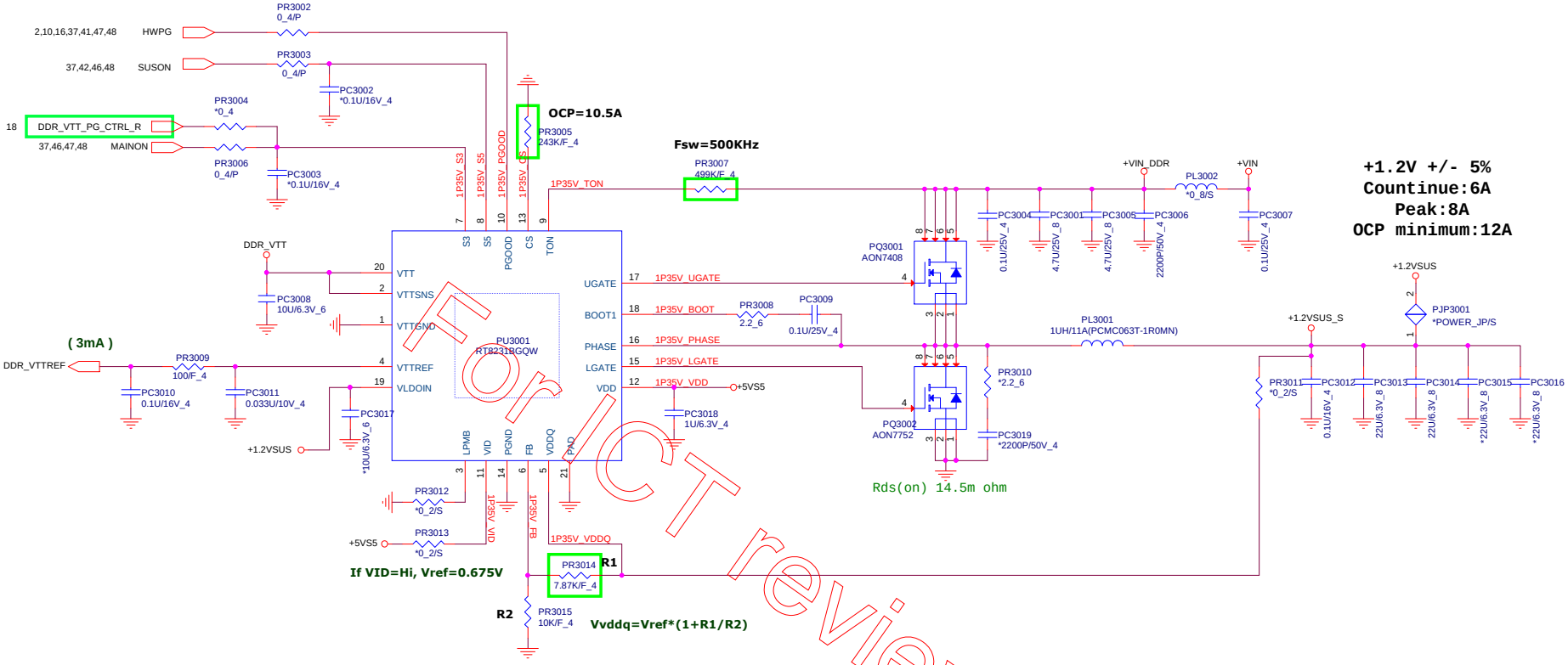
+VIN	26,38,39,40,42,43,44,45,46,47,48,49,50
+3VS5	10,12,14,16,26,33,37,42,46,47,48,51
+5VS5	10,26,28,30,42,43,44,45,46,47,48,49,50,51
+3VPCU	5,10,30,33,37,38,40
+5VPCU	28,40,46,51

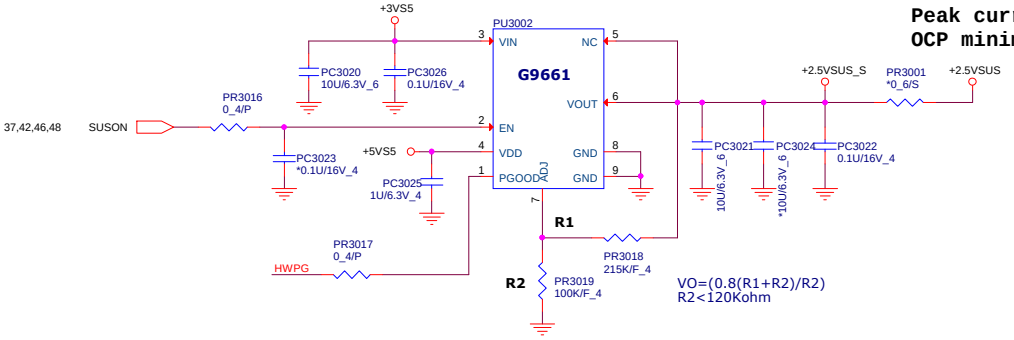
NB5

PROJECT : X1F

Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
Date: Monday, November 30, 2015	Sheet 41 of 51	





+VIN	26,38,39,40,41,43,44,45,46,47,48,49,50
+5VS5	10,26,28,30,41,43,44,45,46,47,48,49,50,51
+1.2VSUS	2,6,10,17,18,48,51
DDR_VTT	17,18
+2.5VSUS	17,18

NB5

PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 (RT8231B)	1A

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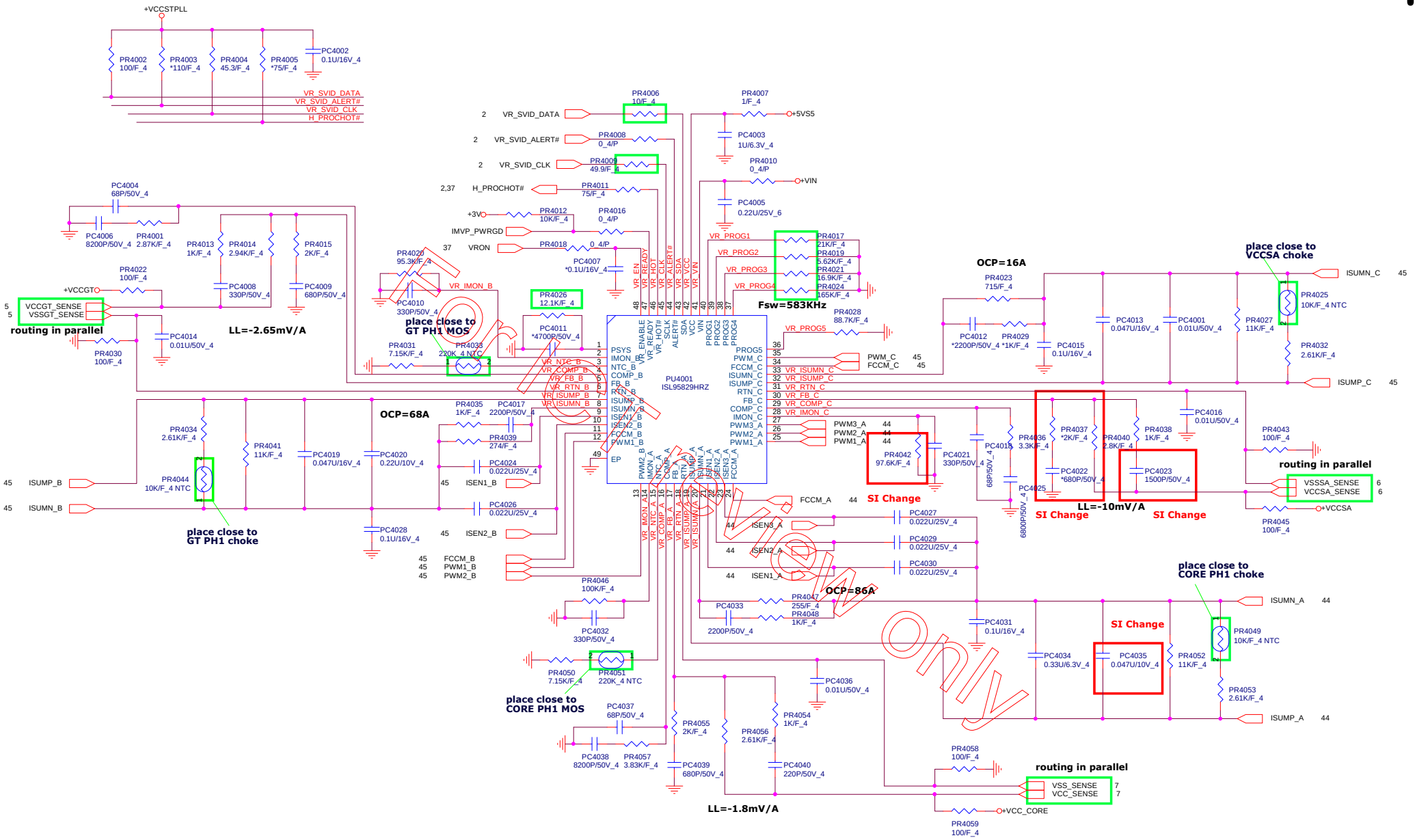
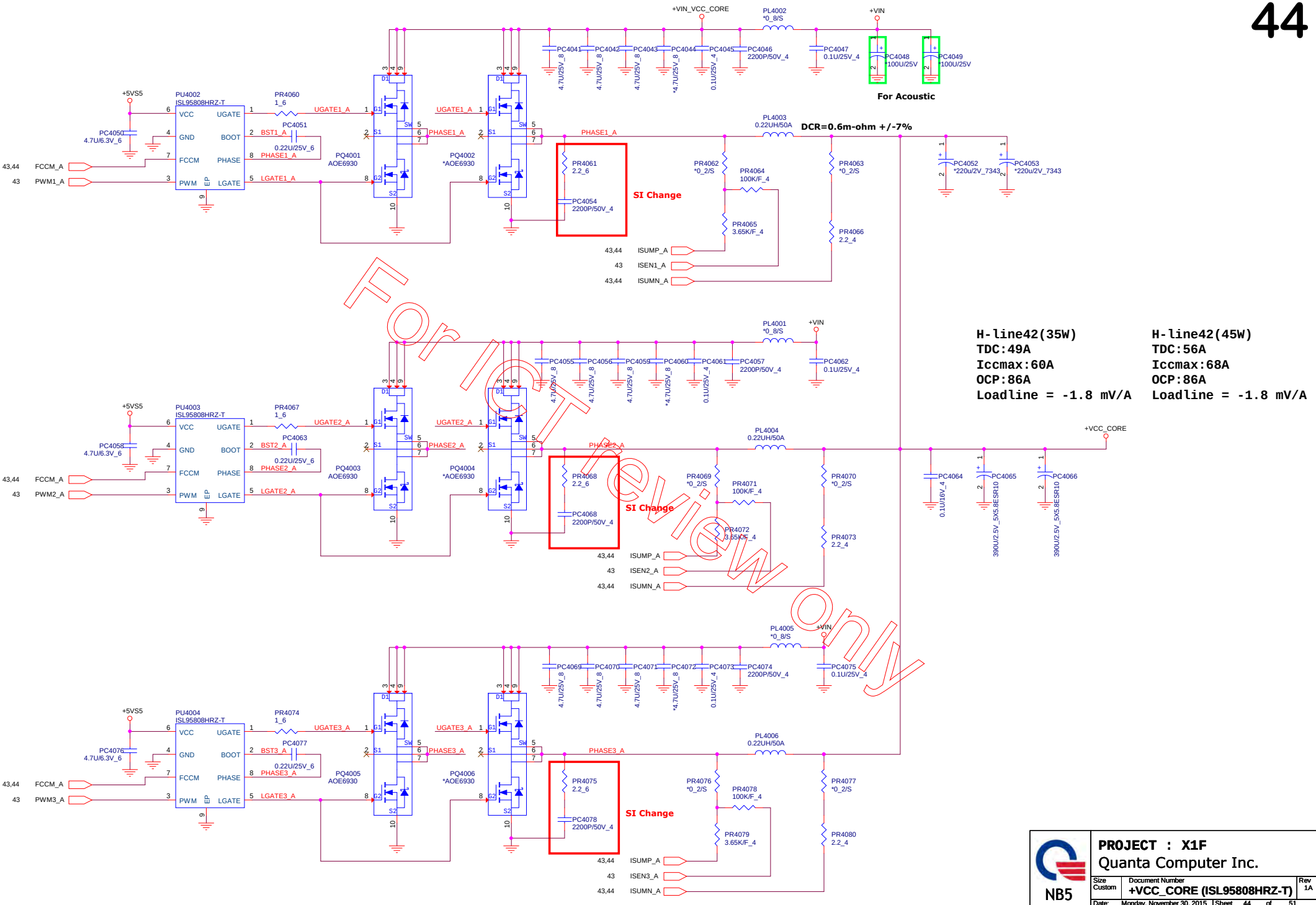


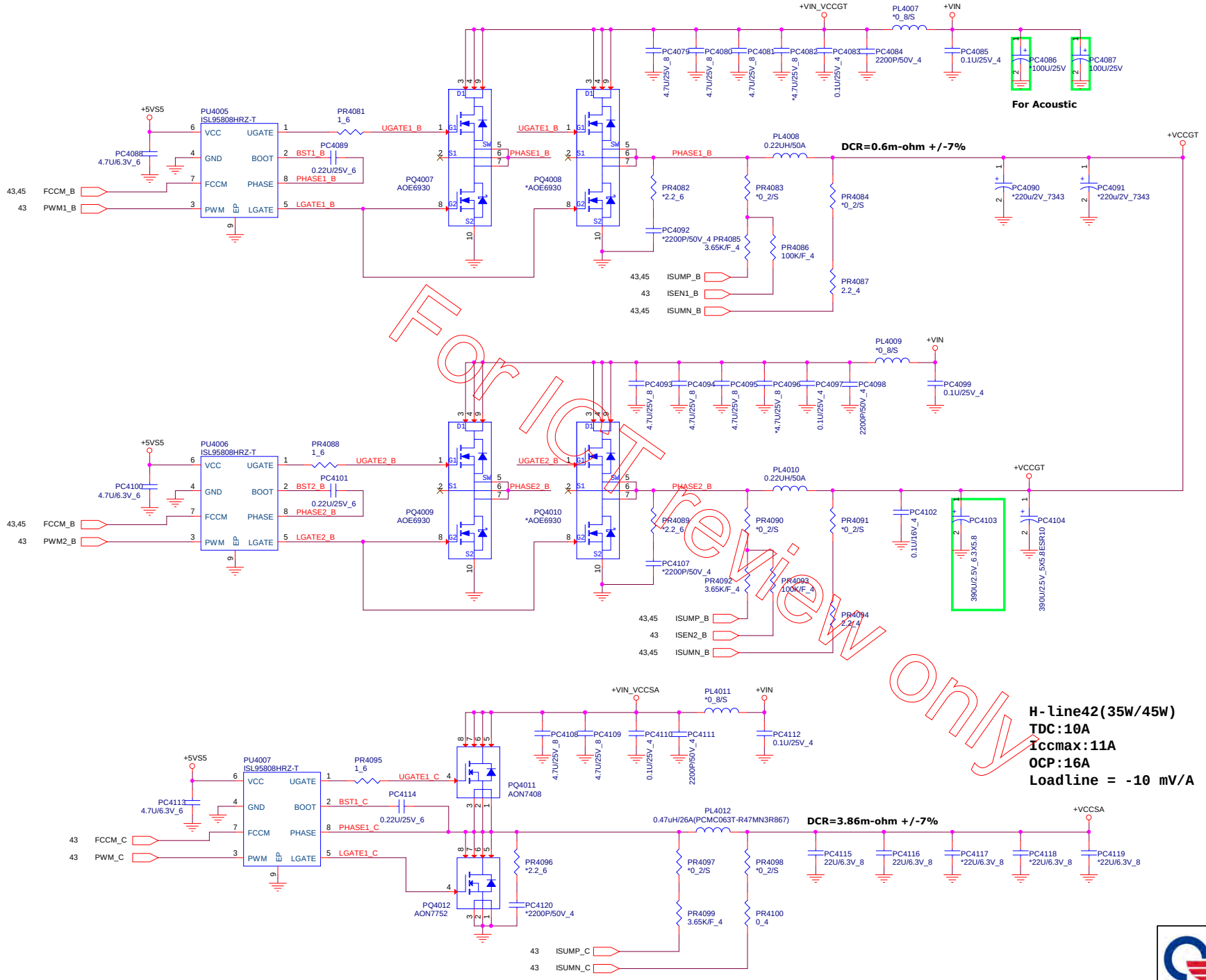
NB5	PROJECT : X1F Quanta Computer Inc.	
	Size: Custom Document Number: CPU VR IC (ISL95829HRZ)	Rev: 1A
	Date: Monday, November 30, 2015	Sheet 43 of 51



H-line42(35W)
TDC:49A
Iccmax:60A
OCP:86A
Loadline = -1.8 mV/A

H-line42(45W)
TDC:56A
Iccmax:68A
OCP:86A
Loadline = -1.8 mV/A

NB5	**PROJECT : X1F** Quanta Computer Inc.	
	Size: Custom Document Number: **+VCC_CORE (ISL95808HRZ-T)**	Rev: 1A
	Date: Monday, November 30, 2015	Sheet 44 of 51



H-line42(35W)
TDC:41A
Iccmax:55A
OCP:68A
Loadline = -2.65 mV/A

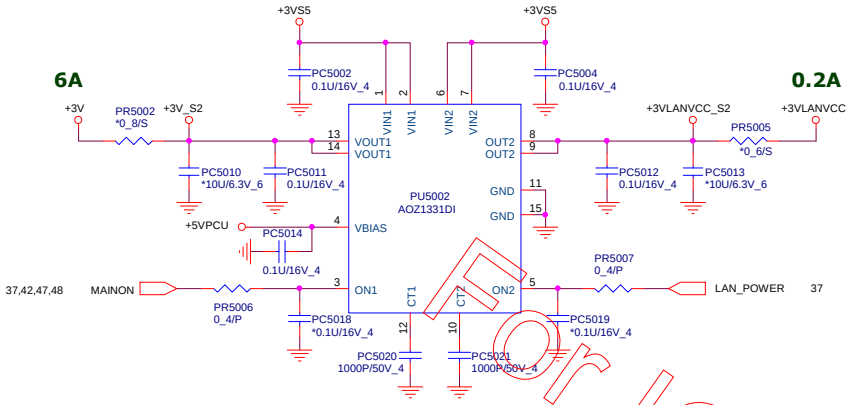
H-line42(45W)
TDC:39A
Iccmax:55A
OCP:68A
Loadline = -2.65 mV/A

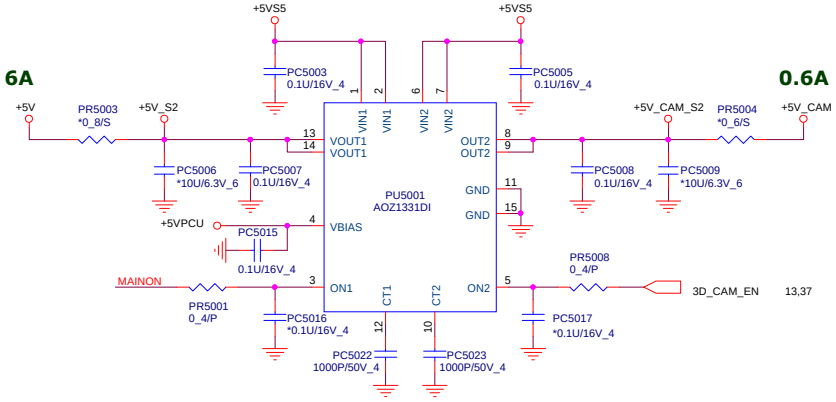
H-line42(35W/45W)
TDC:10A
Iccmax:11A
OCP:16A
Loadline = -10 mV/A

NB5

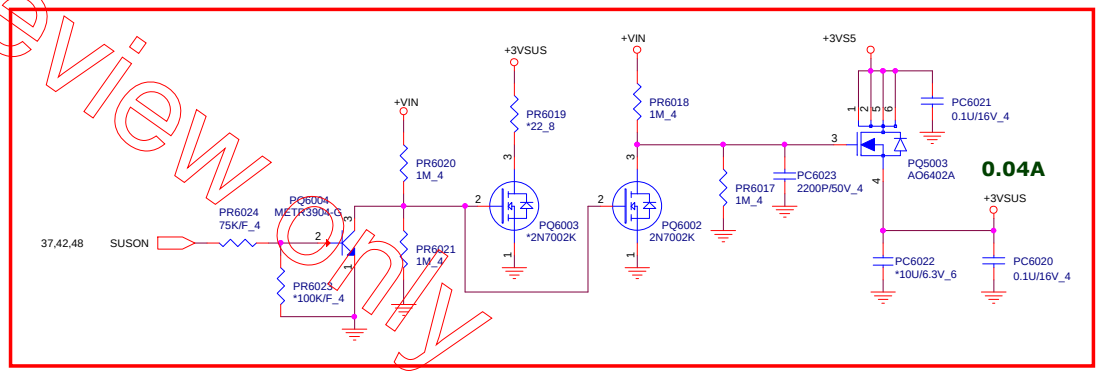
PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCGT/SA (ISL95808HRZ-T)	1A
Date: Monday, November 30, 2015	Sheet 45 of 51	





SI Change



+3V	5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,49
+5V	26,27,28,29,31,32,38,49
+3VS5	10,12,14,16,26,33,37,41,42,47,48,51
+5VS5	10,26,28,30,41,42,43,44,45,47,48,49,50,51
+3VSUS	38
+3VLANVCC	35
+5V_CAM	31
+3V_DEEP_SUS	9,10,12,13,14,16,18

NB5

PROJECT : X1F

Quanta Computer Inc.

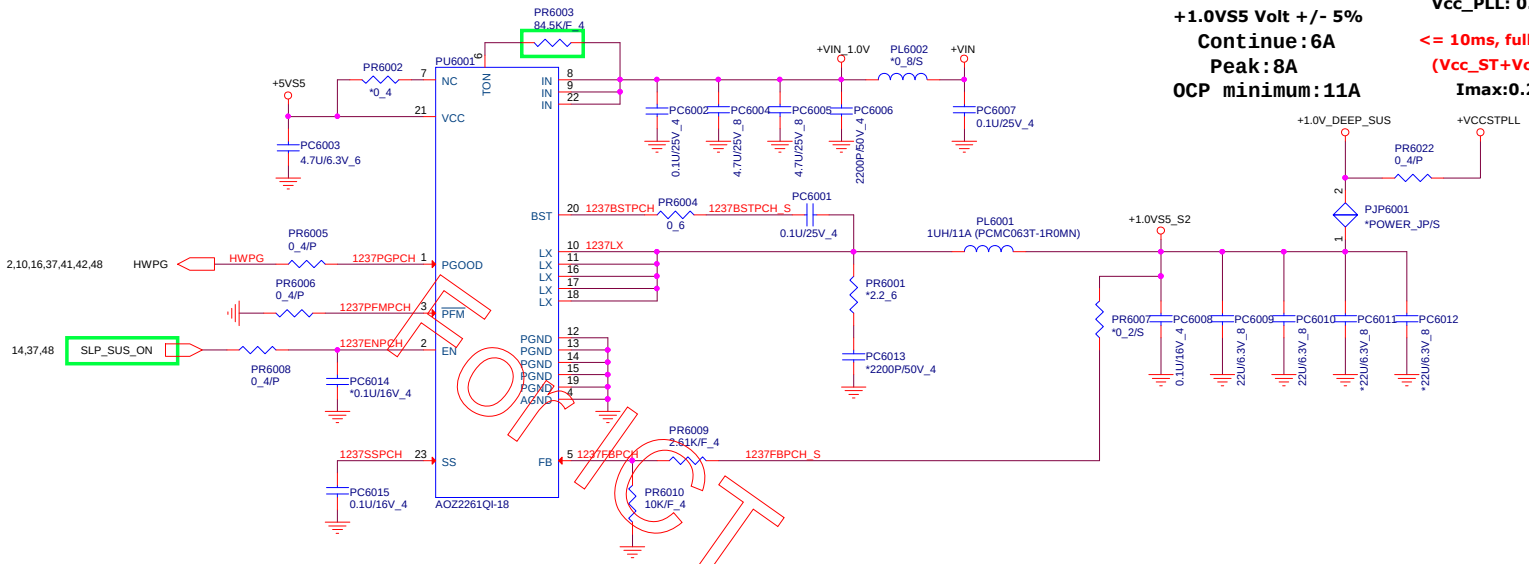
Size	Document Number	Rev
Custom	**Load switch IC (AOZ1331D)**	1A

Date: Monday, November 30, 2015 | Sheet 46 of 51

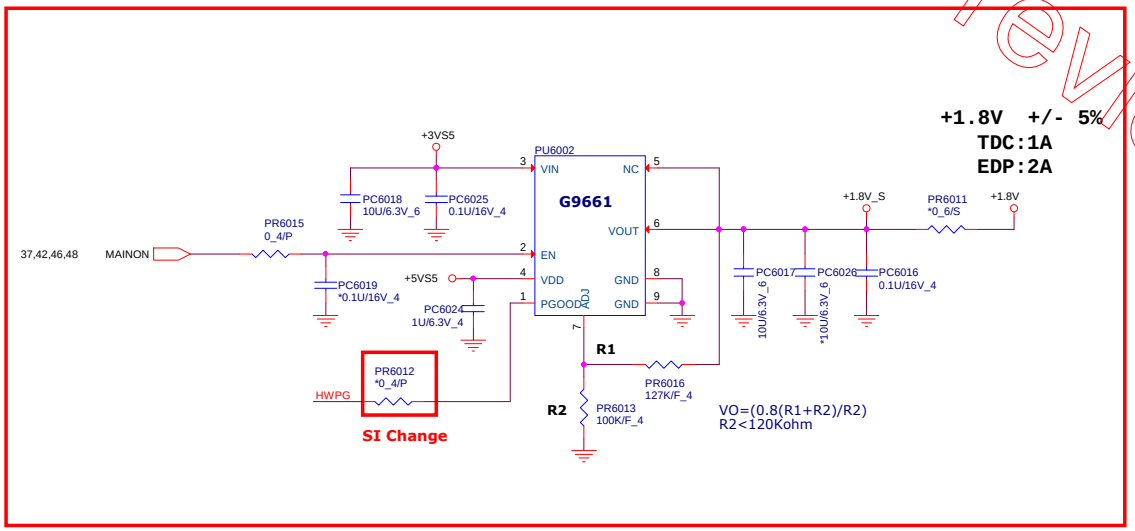
Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

(V1.00A+V1.00_MODPHY+VccPRIM_CORE)
+1.0VS5 Volt +/- 5%
Continue:6A
Peak:8A
OCP minimum:11A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)
Imax:0.24A



SI Change



SI Change

+VIN	26,38,39,40,41,42,43,44,45,46,48,49,50
+3VS5	10,12,14,16,26,33,37,41,42,46,48,51
+5VS5	10,26,28,30,41,42,43,44,45,46,48,49,50,51
+1.0V_DEEP_SUS	10,11,14,16,48
+1.8V_DEEP_SUS	
+1.8V	28,31
+VCCSTPLL	2,6,43

NB5

PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0_DEEP_SUS	1A
Date: Monday, November 30, 2015	Sheet 47 of 51	

Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 5.5A

<= 10ms full load ready
Imax:5.5A

Imax:0.04A

<= 240us, full load ready
TDC:0.26A

Reserve for separating +1.0V and VCCIO

+0.95 +/- 5%
Continue:4A
Peak:5.5A
OCP minimum:8A

+1.0V 2,5,6,10,16,37
+3VS5 10,12,14,16,26,33,37,41,42,46,47,51
+5VS5 10,26,28,30,41,42,43,44,45,46,47,49,50,51
+VCCIO 3,6,16
+1.0V_DEEP_SUS 10,11,14,16,47
+1.2V_VCCPLL_OC 6
+1.2VSUS 2,6,10,17,18,42,51

NB5	**PROJECT : X1F** Quanta Computer Inc.	
Size: Custom	Document Number: **+1.0V/+VCCSTPLL/+VCCIO**	Rev: 1A
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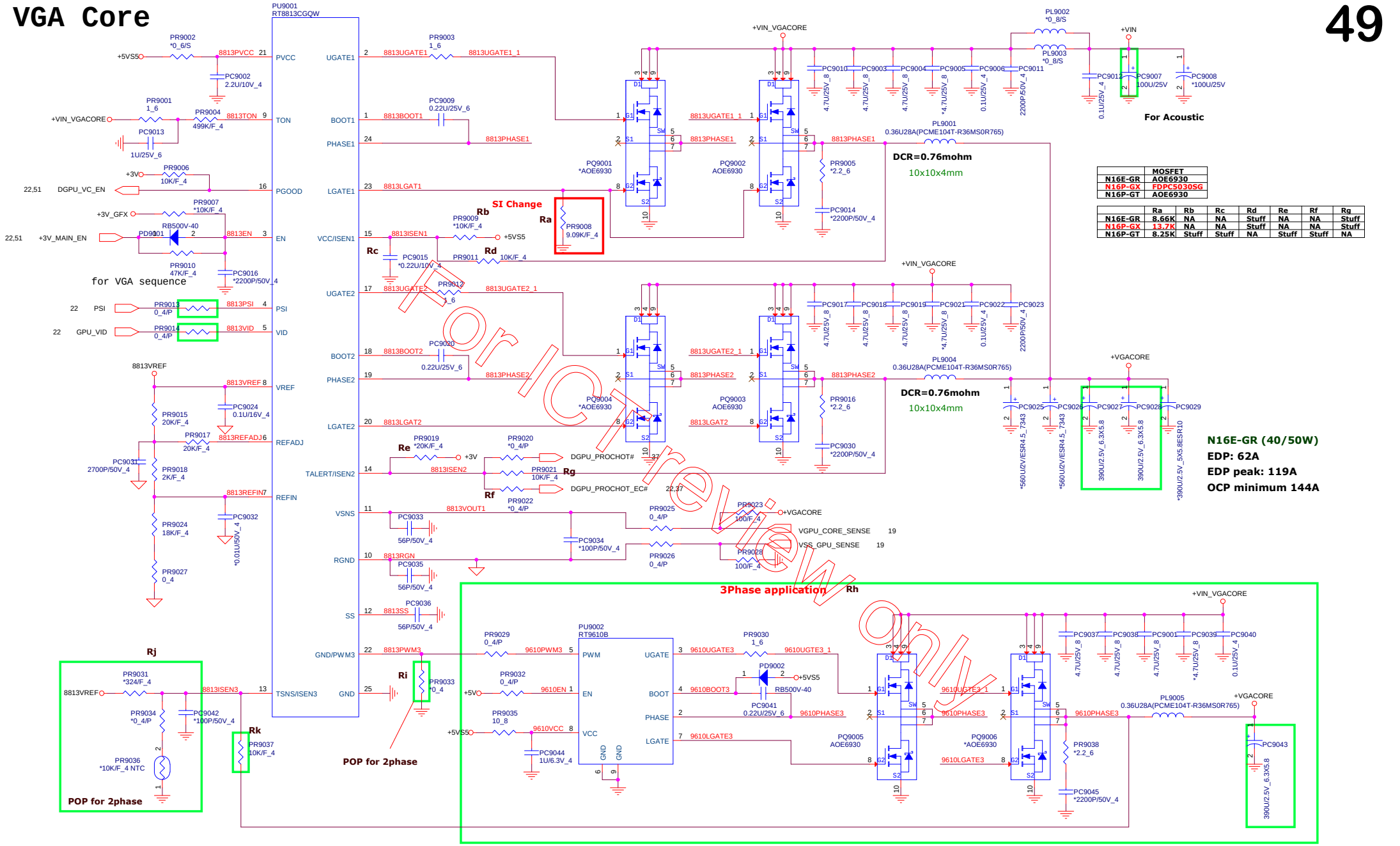
VGA Core



	MOSFET
N16E-GR	AOE6930
N16P-GX	FDPC5030SG
N16P-GT	AOE6930

	Ra	Rb	Rc	Rd	Re	Rf	Rg
N16E-GR	8.66K	NA	NA	Stuff	NA	NA	Stuff
N16P-GX	13.7K	NA	NA	Stuff	NA	NA	Stuff
N16P-GT	8.25K	Stuff	Stuff	NA	Stuff	Stuff	NA

	Rh	Ri	Rj	Rk
N16E-GR	Stuff	NA	NA	Stuff
N16P-GX	Stuff	NA	NA	Stuff
N16P-GT	NA	Stuff	Stuff	NA

+3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46
+VIN 26,38,39,40,41,42,43,44,45,46,47,48,50
+5VS5 10,26,28,30,41,42,43,44,45,46,47,48,50,51
+3V_GFX 19,20,21,22,23,51
+VGACORE 23

NB5

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Size	Document Number	Rev
Custom	+VGACORE (RT8813C)	1A

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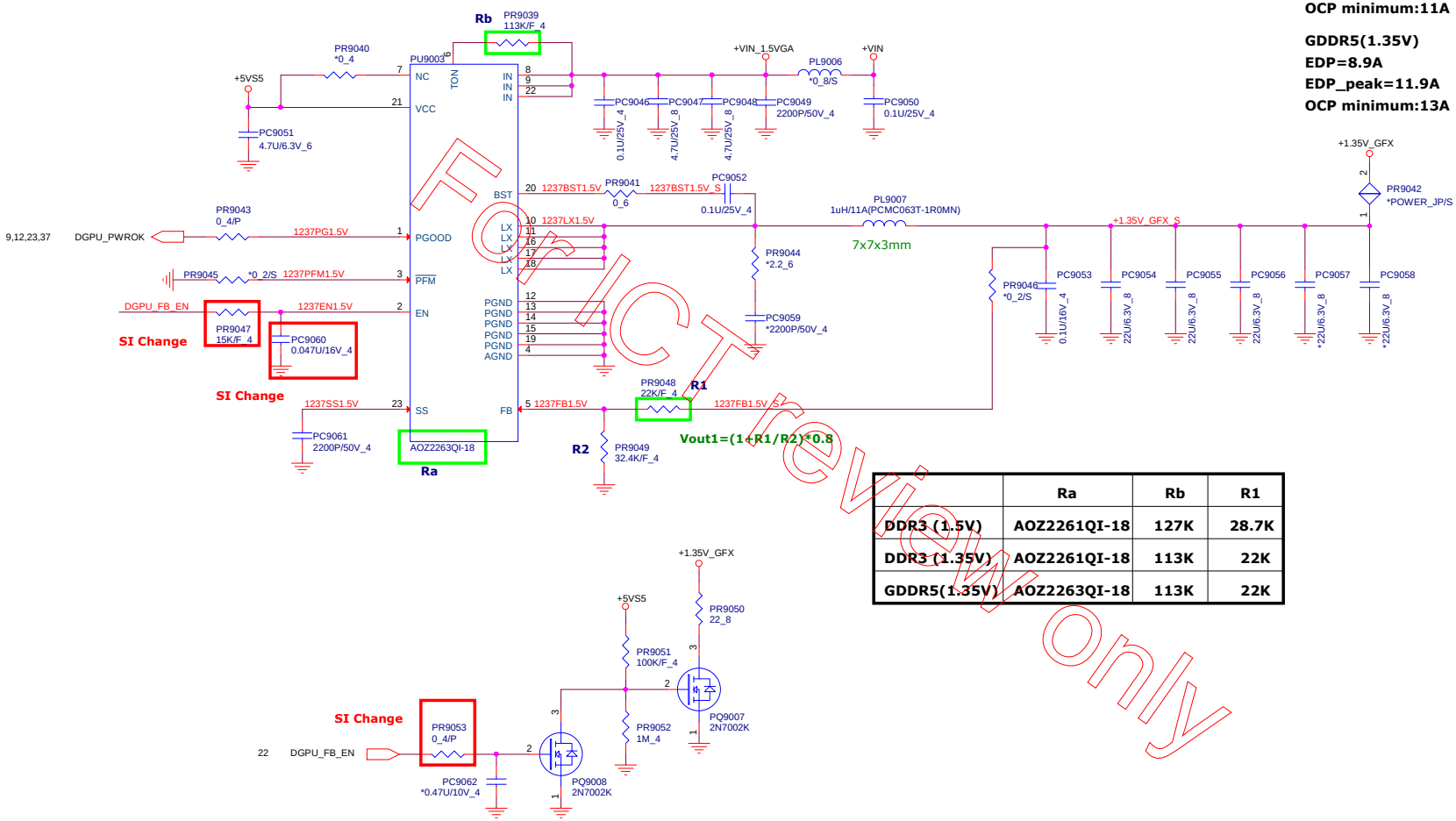
DDR3(1.5V / 1.35V)
EDP=4.18A
EDP_peak=6.54A
OCP minimum:11A

GDDR5(1.35V)
EDP=8.9A
EDP_peak=11.9A
OCP minimum:13A



	Ra	Rb	R1
DDR3 (1.5V)	AOZ2261QI-18	127K	28.7K
DDR3 (1.35V)	AOZ2261QI-18	113K	22K
GDDR5(1.35V)	AOZ2263QI-18	113K	22K

+VIN 26,38,39,40,41,42,43,44,45,46,47,48,49
+5VS5 10,26,28,30,41,42,43,44,45,46,47,48,49,51
+1.35V_GFX 20,23,24,25

NB5

PROJECT : X1Q
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Size	Document Number	Rev
Custom	+1.35V_GFX (AOZ2263QI-18)	1A

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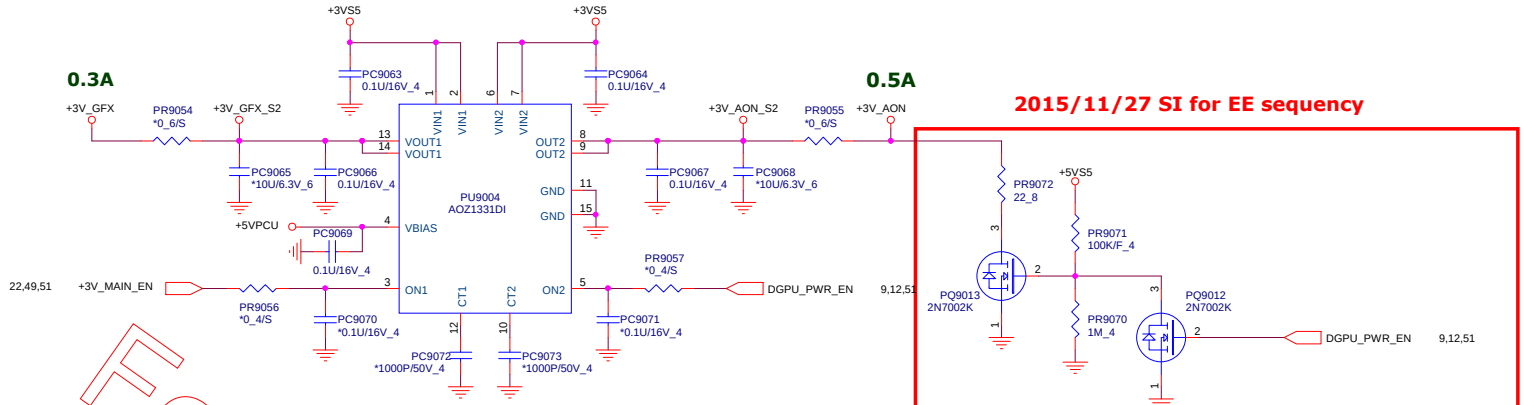
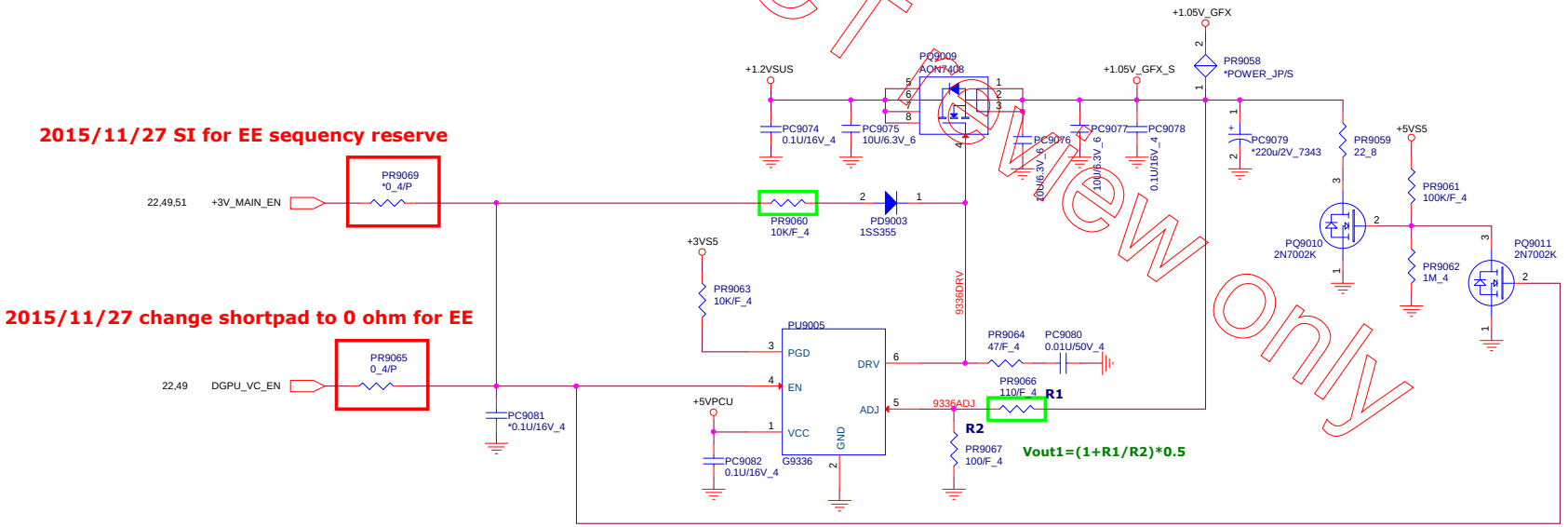


+1.05V_GFX Volt +/- 5%
EDP=2.38A
EDP_peak = 2.45A



+VIN	26,38,39,40,41,42,43,44,45,46,47,48,49,50
+3VS5	10,12,14,16,26,33,37,41,42,46,47,48
+5VS5	10,26,28,30,41,42,43,44,45,46,47,48,49,50
+3V_GFX	19,20,21,22,23,49
+3V_AON	19,22,23,27
+1.2VSUS	2,6,10,17,18,42,48
+1.05V_GFX	19,20,21,23

NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3V/+1.05V_GFX(AOZ1331DI)	1A
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