1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K60 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2011-02-08

LAST_MODIFIED=Tue Feb 8 14:39:56 2011

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DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Tue Feb 8 14:39:56 2011

DRAWING TITLE: SCH,K60,MLB

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
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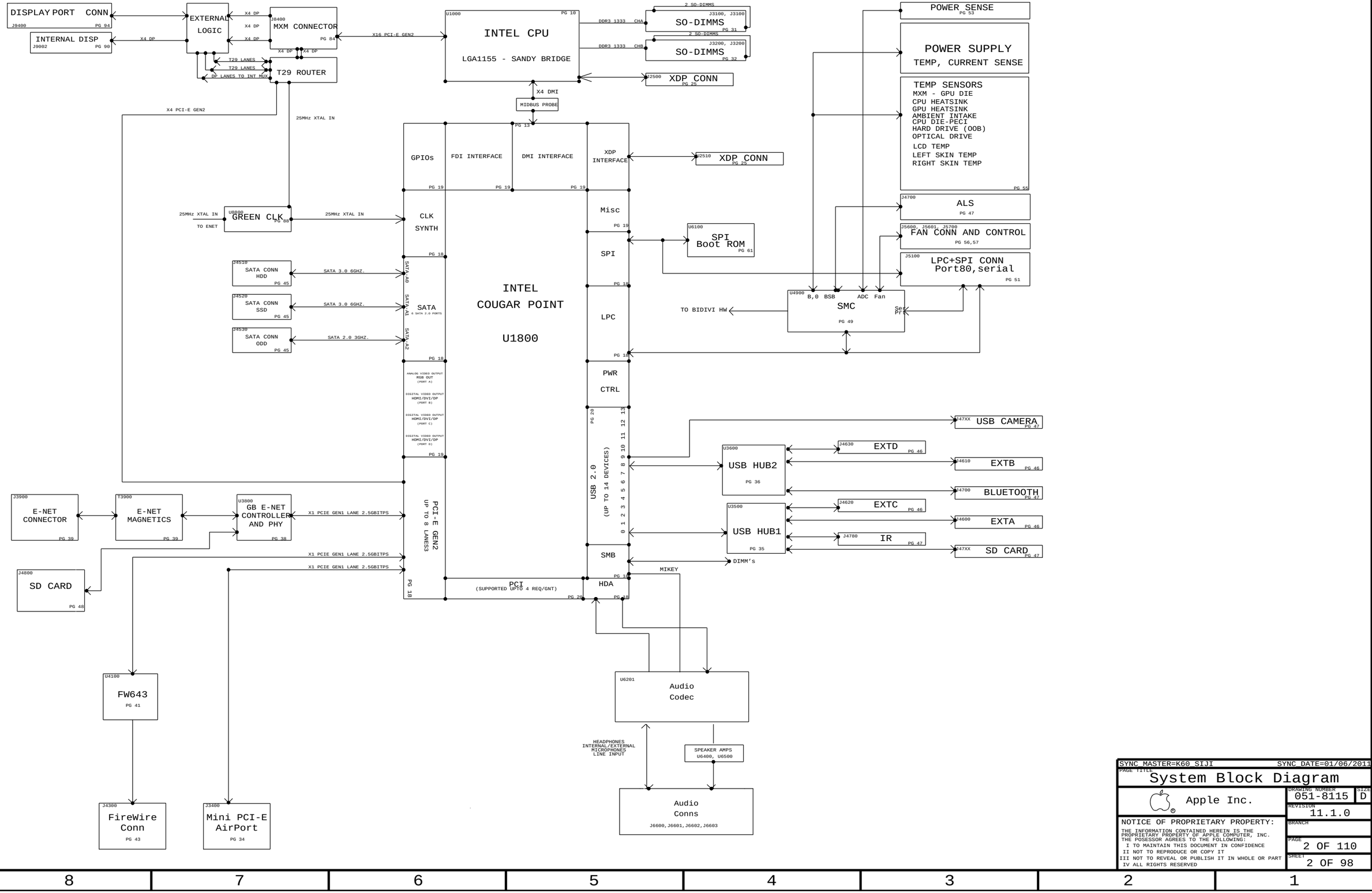

SYNC_MASTER=K60_SIJI SYNC_DATE=01/06/2011

PAGE TITLE

System Block Diagram

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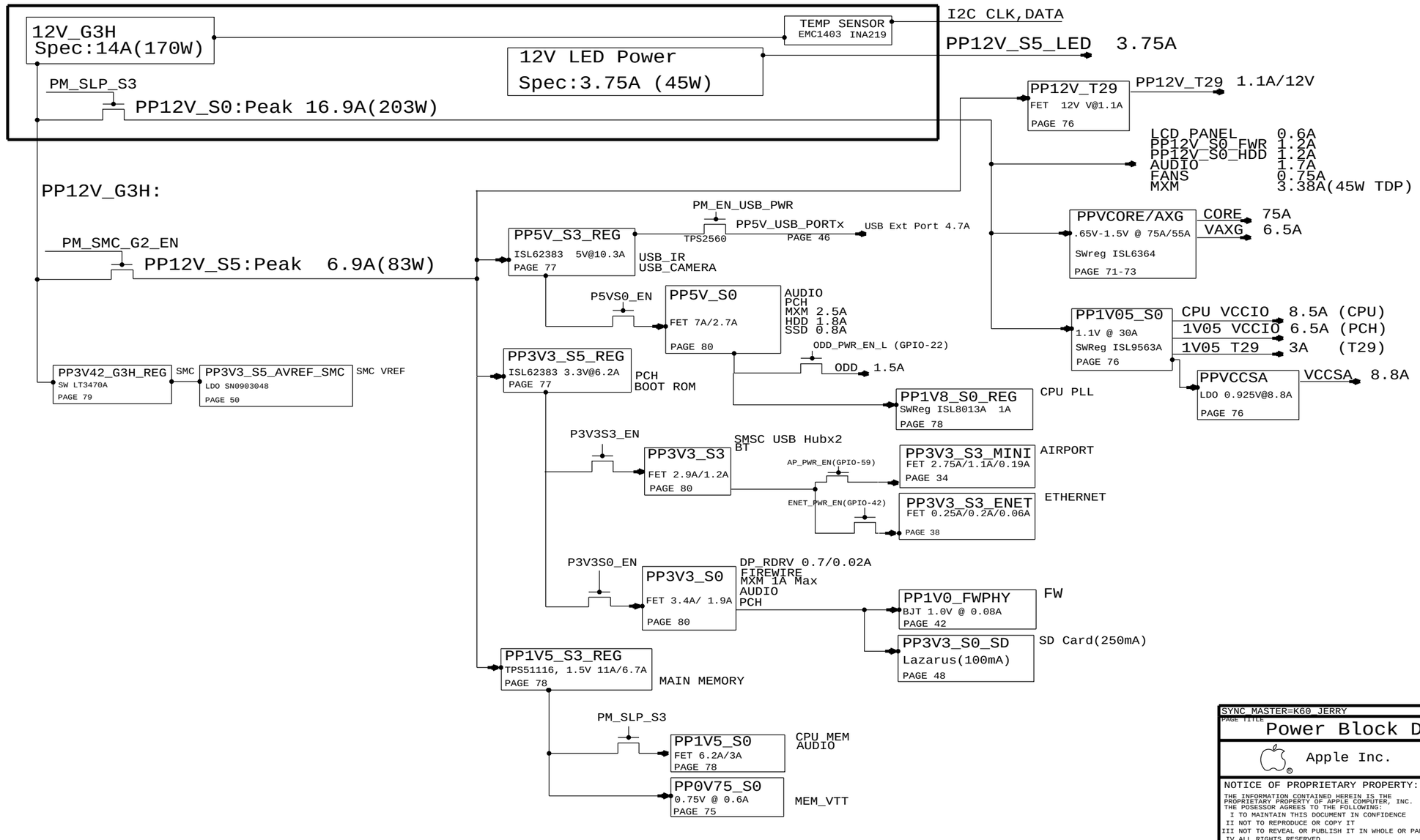
AC/DC POWER SUPPLY (Spec:215W)



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Power Block Diagram

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-0801	PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD	DEVELOPMENT,DEV_GROUP
639-1767	PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-1820	PCBA,MLB,K60,2.7G,4C,PRQ,P2_ODD	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-1821	PCBA,MLB,K60,2.8G,4C,PRQ,P2_ODD	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-2160	PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD,NO_DBG	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2159	PCBA,MLB,K60,2.7G,4C,PRQ,P2_ODD,NO_DBG	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2161	PCBA,MLB,K60,2.8G,4C,PRQ,P2_ODD,NO_DBG	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2118	PCBA,MLB,K60,2.5G,4C,PRQ,P1_ODD	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2122	PCBA,MLB,K60,2.7G,4C,PRQ,P1_ODD	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2119	PCBA,MLB,K60,2.8G,4C,PRQ,P1_ODD	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2132	PCBA,MLB,K60,2.5G,4C,PRQ,P1_ODD,NO_DBG	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG
639-2133	PCBA,MLB,K60,2.7G,4C,PRQ,P1_ODD,NO_DBG	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG
639-2134	PCBA,MLB,K60,2.8G,4C,PRQ,P1_ODD,NO_DBG	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC1	COMMON,ALTERNATE,MXM,FCIM,CPU_1V5_SENSE,CPU_VCCSA_SENSE,1V05_PCH_SENSE,HUB_USX2061,PRODUCTION,VAXG,SSD
BASIC2	AP,BT,IR,T29
DEV_GROUP	VREFMRGN_A,VREFMRGN_B,DIMM_1V5_SENSE
YES_DBG	XDP,XDP_CONN,XDP_CPU_BPM,MOJOMUX:YES,LPCPLUS:YES
NO_DBG	MOJOMUX:NO,LPCPLUS:NO

CPU SOCKET & ILM SUB-BOMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0071	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	TYCO_SOCKET
604-1474	1	ASSY,PURCHASED,ILM,TYCO	ILM	CRITICAL	TYCO_SOCKET
511S0073	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	MOLEX_SOCKET
604-1161	1	ASSY,PURCHASED,ILM,MOLEX	ILM	CRITICAL	MOLEX_SOCKET

BOM NUMBER	BOM NAME	BOM OPTIONS
085-2452	SUB ASSY,CPU SOCKET,K60,TYCO	TYCO_SOCKET
085-2453	SUB ASSY,CPU SOCKET,K60,MOLEX	MOLEX_SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
085-2452	1	TYCO CPU SOCKET AND ILM	SKT_ILM	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
085-2453	085-2452		SKT_ILM	MOLEX ALTERNATE

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	337S4088	1	IC,COUGAR POINT,SLJ4F,BD82Z68,PRQ,B3	U1800	CRITICAL	
	353S3055	1	IC,PI3VEDP212,X2 DP MUX,QFN	U9390	CRITICAL	
	338S0753	1	IC,FW643,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
	825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
	343S0534	1	IC,BCM57765,ENET&SD,8X8	U3900	CRITICAL	
RAW:	335S0807	1	341T0184	FLASH,EFI BOOTROM,K60/K62	U6100	CRITICAL
RAW:	335S0539	1	341T0328	SFLASH ENET 2MBIT,CIV	U3990	CRITICAL
		1	338S0945	T29 ROUTER, IC ASSP	U9700	CRITICAL T29
RAW:	335S0550	1	341T0257	IC,T29,SERIAL EEPROM	U9790	CRITICAL T29
RAW:	337S3997	1	341T0326	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL T29
RAW:	335S0709	1	341T0330	IC,MXM SYS ROM,24C02	U8570	CRITICAL
RAW:	338S0878	1	341T0185	IC,SMC,K60	U4900	CRITICAL K60

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4043	1	SNB,SR00S,PRQ,D2,2.5,65W,4+1,6M,LGA	CPU	CRITICAL	2P5GHZ_SNB_CPU_PRQ
337S4062	1	SNB,SR009,PRQ,D2,2.7,65W,4+1,6M,LGA	CPU	CRITICAL	2P7GHZ_SNB_CPU_PRQ
337S4061	1	SNB,SR00E,PRQ,D2,2.8,65W,4+1,8M,LGA	CPU	CRITICAL	2P8GHZ_SNB_CPU_PRQ

K60 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8115	1	SCH,MLB,K60	SCH1		K60
820-2641	1	PCBF,MLB,K60	MLB1		K60

K60 ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0298	128S0293			330UF
371S0679	371S0652			PIN DIODE
377S0107	377S0066			USB DIODE
376S0972	376S0612			ROHM TRA-BJT

SYNC_MASTER=K60_AARON SYNC_DATE=N/A

PAGE TITLE

BOM Configuration

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DRAWING NUMBER 051-8115 SIZE D

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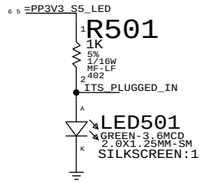
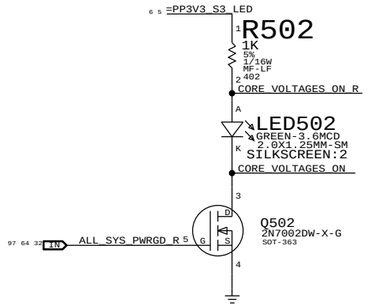
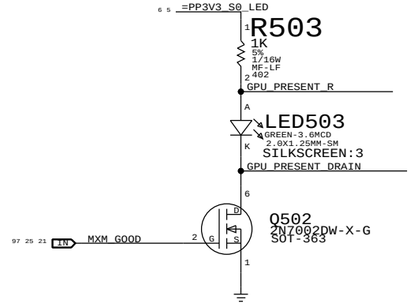
S5 Led



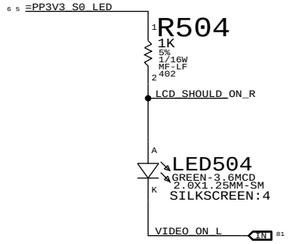
ALL_SYS_PWRGD Led



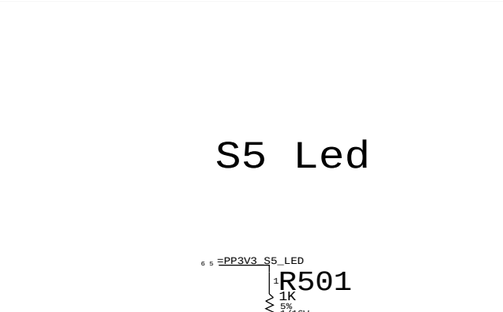
MXM PWR GOOD Led

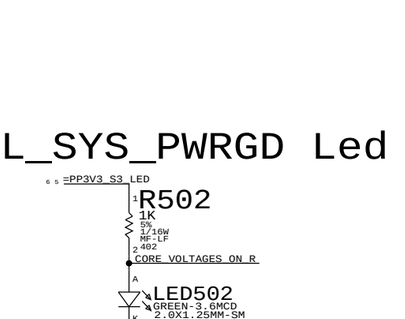


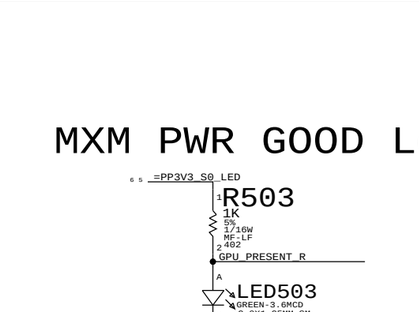
VIDEO ON Led

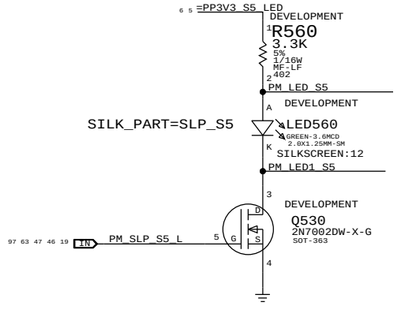


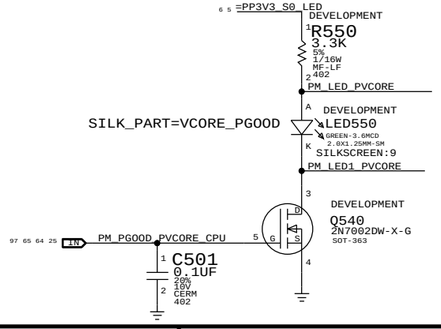
PROTO DEBUG LEDS ARE SHOWN BELOW

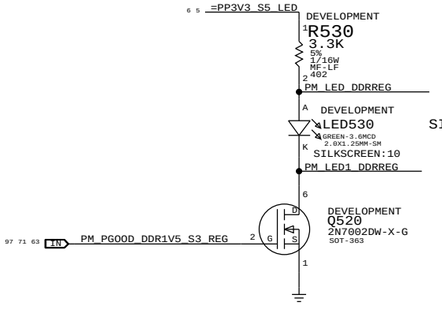


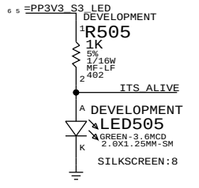












SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: DEBUG LEDS

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DRAWING NUMBER: 051-8115 SIZE: D

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POWER SUPPLY TO MLB

J600
76833-0106
M-RT-TH

518-0373

PP12V_G3H_ACDC 6
PP12V_S0_PS 6

C611 1UF 10% 25V X5R 603-1
PLACE C611 CLOSE TO CONNECTOR

C610 1UF 10% 25V X5R 603-1
PLACE C610 CLOSE TO CONNECTOR

MLB TO BLC

94 81 49 BI SMB_BLC_TCON_SDA
94 81 49 IN SMB_BLC_TCON_SCL

R630 0 1/16W 402 5%
R631 0 1/16W 402 5%

SMB_BLC_TCON_SDA_R
SMB_BLC_TCON_SCL_R

NOSTUFF C627 47PF 5% 50V CERM 402
NOSTUFF C628 47PF 5% 50V CERM 402

49 6 =PP3V3_S0_SMBUS

FET DIODE IS S TO D (FACES BLC WHICH 3V3 RISES BEFORE MLB 3V3).

NOSTUFF C621 47PF 5% 50V CERM 402

Q600 2N7002DW-X-G SOT-363

49 BI =SMB_BLC_PCH_SDA
49 IN =SMB_BLC_PCH_SCL

NOSTUFF R618 0 1/16W 402 5%
NOSTUFF R617 0 1/16W 402 5%

SMB_BLC_PCH_SDA_R
SMB_BLC_PCH_SCL_R

BLC SDA/SCL ISOLATION CIRCUIT

NOSTUFF C622 47PF 5% 50V CERM 402

Q600 2N7002DW-X-G SOT-363

R622 0 1/16W 402 5%

91 21 15 IN BLC_GPIO
BLC_GPIO_R

L602 FERR-1000-OHM 0402

97 81 IN VSYNC_DP_CONN
VSYNC_DP_CONN_R

CRITICAL
J602
53780-8608
F-RT-SM

518S0543

ISOLATED_GND
R620 0 5% 1/16W MF-LF 402

MLB TO PS

PLACE C606 CLOSE TO CONNECTOR

97 63 IN PM_EN_P12V_S0_FET

Q610 2N7002 SOT23-HF1

C606 0.001UF 10% 50V X7R 402

R602 0 1/16W 402 5%
R601 0 1/16W 402 5%

49 IN =SMB_ACDC_SCL
49 BI =SMB_ACDC_SDA

SMB_ACDC_SCL_RC
SMB_ACDC_SDA_RC

PS_ON
R605 0 1/16W 402 5%
ISOLATED_GND2

97 81 BL_EN
97 83 BL_PWM

C604 47PF 5% 50V CERM 402
C602 47PF 5% 50V CERM 402
C603 0.001UF 10% 50V X7R 402

PLACE C603 CLOSE TO CONNECTOR

CRITICAL
J601
50293-00771-H01
M-ST-SM

518S0813

95 PP0V75_S0
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PPVTT_S0_DDR_LDO 71
=PP0V75_S0_MEM_VTT_S0FET 32

95 PPVTT_S0_DDR
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PPVTT_S0_DDR_FET 32
=PP0V75_S0_MEM_VTT_B 31
=PP0V75_S0_MEM_VTT_A 30

95 PPVCORE_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_CPU_REG 66
=PPVCORE_S0_CPU 13 16 50 65

95 PPVAXG_S0
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PPVAXG_S0_REG 67
=PPVAXG_S0_CPU 13 17 50 65

95 PP1V05_S0
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V05_S0_REG 68
=PP1V05_S0_PWR 50
=PPVCCIO_S0_XDP 25
=PPVCCIO_S0_CPU 10 11 13 16 65
=PPVCCIO_S0_SMC 46 47
=PP1V05_S0_PCH_PWR 50
=PPVCCSA_S0_INPUT_PWR 50 69
=PP1V05_S0_CK505 26

95 PP1V05_S0_PCH
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V05_S0_PCH_SNS 50
=PP1V05_S0_PCH_VCC_DMI 22 24
=PP1V05_S0_PCH_VCCADPLL 17
=PP1V05_S0_PCH_VCCIO_DMI 22 24
=PP1V05_S0_PCH_VCCIO_SATA 18 22 24
=PP1V05_S0_PCH_VCCIO_PCIE 18 19 22 24
=PP1V05_S0_PCH_VCC_CORE 22 24
=PP1V05_S0_PCH_VCCIO_USB 22 24
=PP1V05_S0_PCH 18 24 79
=PP1V05_S0_PCH_VCCDIFFCLK 22 24
=PP1V05_S0_PCH_VCCSSC 22 24
=PP1V05_S0_PCH_VCCASW 22 24
=PP1V05_S0_PCH_V_PROC_IO 22 24
=PP1V05_S0_P1V05T29FET 80

95 PP1V05_S0_INPUT_VCCSA
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PPVCCSA_S0_INPUT_SNS 50
=PPVCCIO_S0_CPU_VCCSA 69

95 PPVCCSA_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=0.925V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PPVCCSA_S0_FET 69
=PPVCCSA_S0_CPU 13 50
=PPVCCSA_S0_PWRCTL 64

95 PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V5_S0_FET 73
=PP1V5_S0_AUD_DIG 56
=PP1V5_S0_CK505 26
=PP1V5_S0_MINI 33
=PP1V5_S0_PWR 50
=PP1V5_S0_DP 83

95 PP1V5_S0_CPU_MEM
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V5_S0_CPU_MEM_SNS 50
=PP1V5_S0_CPU_MEM 11 13 16 28 29

95 PP3V3_S0
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP3V3_S0_FET 73
=PP3V3_S0_PCH 18 21 24
=PP3V3_S0_FAN 53 54
=PP3V3_S0_PCH_VCCADAC 17
=PPSPD_S0_MEM_A 30 47
=PPSPD_S0_MEM_B 31
=PP3V3_S0_AUDIO 56 58 59 60 61 62
=PP3V3R1V5_S0_PCH_VCCSUSHDA 24
=PP3V3_S0_SMBUS 6 49
=PP3V3_S0_SMC_LS 47 51
=PP3V3_S0_SMBUS_SMC_0 49
=PP3V3_S0_SMBUS_SMC_B 49
=PP3V3_S0_SMBUS_SMC_MGMT 49
=PP3V3_S0_MXM 21 64 75 76
=PP3V3_S0_ODD 42
=PP3V3_S0_SATALED 18 42
=PP3V3_S0_SENSE 50 52
=PP3V3_S0_PWRCTL 63 64 73 80
=PP3V3_S0_PCH_VCC3_3_GPIO 22 24
=PP3V3_S0_FWPHY 39 40 41
=PP3V3_S0_DP 81
=PP3V3_S0_PCH_VCC3_3_PCI 22 24
=PP3V3_S0_CK505 26
=PP3V3_S0_PCH_GPIO 20 45
=PP3V3_S0_PCH_STRAPS 15
=PP3V3_S0_PCH_VCC3_3_SATA 22 24
=PP3V3_S0_RSTBUF 11 27
=PP3V3_S0_PCH_PM 27
=PP3V3_S0_SMBUS_SMC_BSA 49
=PP3V3_S0_SDCARD 45
=PP3V3_S0_P1V05_VREG 68
=PP3V3_S0_PCH_VCC3V3 22 24
=PP3V3_S0_VRD 65 68
=PP3V3_S0_LED 5
=PP3V3_S0_P3V3T29FET 80
=PP3V3_S0_DPSDRVA 84
=PP3V3_S0_INTDPMUX 83
=PP3V3_S0_T29PWRCTL 80
=PP3V3_S0_T29I2C 49
=PP3V3_S0_ENET_PHY 36 37

"S0" RAILS

ONLY ON IN RUN

95 PP1V8_S0
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V8_S0_REG 71
=PP3V3R1V8_S0_PCH_VCCDFTERM 22 24
=PP1V8R1V5_S0_PCH_VCCVRM 24 79
=PP1V8_S0_CPU_PLL 13 16
=PP1V8_S0_PCH 19
=PP1V8_S0_PWRCTL 64

98 95 PP5V_S0
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP5V_S0_FET 73
=PP5V_S0_AUDIO 56
=PP5V_S0_SATA 42
=PP5V_S0_MXM 75
=PP5V_S0_VRD 65 67
=PP5V_S0_ISENSE 50
=PP5V_S0_PCH 24
=PP5V_S0_P1V05_VREG 68
=PP5V_S0_LPCPLUS 48
=PP5V_S0_P1V8_REG 71

95 PP12V_S0
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.5mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP12V_S0_PS 6
=PP12V_S0_AUDIO_SPKRAMP 58 59
=PP12V_S0_VRD 65
=PP12V_S0_MXM_PWR 50
=PP12V_S0_LCD 81
=PP12V_S0_P1V05_VREG 68
=PP12V_S0_PWRCTL 63 64 80
=PP12V_S0_SENSE 51
=PP12V_S0_FW 41
=PP12V_S0_CPU_VCCSA 69
=PP12V_S0_SATA 42
=PP12V_S0_FAN 53 54

95 PP12V_S0_MXM
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP12V_S0_MXM_SNS 50
=PP12V_S0_MXM 75

"S3" RAILS

ON IN RUN AND SLEEP

95 PP1V5_S3
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V5_S3_REG 71
=PP1V5_S3_MEM_PWR 50
=PP1V5_S3_S0FET 73

95 PP1V5_S3_MEM
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V5_S3_MEM_SNS 50
=PP1V5_S3_MEMRESET 32
=PP1V5_S3_MEM_A 28 29 30
=PP1V5_S3_MEM_B 28 29 31

98 95 PP3V3_S3
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP3V3_S3_FET 73
=PP3V3_S3_BT 44
=PP3V3_S3_SMBUS_SMC_A 49
=PP3V3_S3_MINI 33
=PP3V3_S3_PWRCTL 64 73 82
=PP3V3_S3_MEMRESET 32
=PP3V3_S3_USB_HUB 34 35
=PP3V3_S3_ENET_PHY 36
=PP3V3_S3_SDCARD 44 45
=PP3V3_S3_VREFMRGN 28
=PP3V3_S3_VRD 71
=PP3V3_S3_LED 5
=PP3V3_SW_DPAPWR 78
=PP3V3_S3_SYSCLK 79
=PP3V3_S3_P3V3R2V9_REG_A 82
=PP3V3_S3_PCH 21

98 95 PP5V_S3
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP5V_S3_REG 70
=PP5V_S3_USB 43
=PP5V_S3_S0FET 73
=PP5V_S3_CAMERA 44
=PP5V_S3_IR 44
=PP5V_S3_MEMRESET 32
=PP5V_S3_DDR_VREG 71
=PP5V_S3_VREFMRGN 28
=PP5V_S3_P3V3R2V9_REG_A 82

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN S5

95 PP3V3_S5
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP3V3_S5_REG 70
=PP3V3_S5_PCH 18 19 21 24
=PP3V3_S5_PCH_GPIO 20
=PP3V3_S5_ROM 48 55
=PP3V3_S5_PCH_VCCSUS3_3_USB 22 24
=PP3V3_S5_PWRCTL 11 63 64
=PP3V3_S5_S3FET 73
=PP3V3_S5_S0FET 73
=PP3V3_S5_PCH_STRAPS 15
=PP3V3_S5_XDP 25
=PP3V3_S5_LPCPLUS 48
=PP3V3_S5_PCH_VCCDSW 22 24
=PP3V3_S5_USB_HUB 34
=PP3V3_S5_CPU_VCCSA 69
=PP3V3_S5_PCH_VCCSPI 22 24
=PP3V3_S5_VRD 70
=PP3V3_S5_LED 5
=PP3V3_S5_MEMRESET 32
=PP3V3_S5_RSTBUF 27
=PP3V3_S5_P3V3R2V9_A 82
=PP3V3_S5_SMCUSBMUX 43
=PP3V3R1V5_S5_PCH_VCCSUSHDA 24

95 PP5V_S5
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP5V_S5_LDO 70
=PP5V_S5_PCH 24

95 PP12V_S5
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP12V_S5_FET 74 95
=PP12V_S5_DDR_VREG 71
=PP12V_S5_P5VS3_VREG 70
=PP12V_S5_PWRCTL 33 64 73
=PP12V_S5_T29_A 82

"G3H" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN G3HOT PER SMC

G3H: ALIASES

95 PP3V42_G3H
MAKE_BASE=TRUE
VOLTAGE=3.42V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP3V42_G3H_REG 72
=PP3V3_G3H_RTC_D 27
=PP3V3_G3H_SMC 46 47
=PP3V3_G3H_SMCUSBMUX 43
=PP3V3_G3H_LPCPLUS 48

95 PP12V_G3H
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP12V_G3H_ACDC 6
=PP12V_G3H_S5_FET 74
=PP12V_G3H_3V42 72

T29 RAILS

95 PP3V3_S0_T29
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP3V3_T29_FET 80
=PP3V3_T29_RTR 79 80 86 87

95 PP1V05_S0_T29
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
=PP1V05_T29_FET 80
=PP1V05_T29_RTR 87
=PP1V05_T29 80

GND RAILS

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
NET_SPACING_TYPE=GND
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

SYNC_MASTER=K60_MARK SYNC_DATE=12/30/2010

PAGE TITLE
Power Conn / Alias

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 6 OF 110
SHEET 6 OF 98

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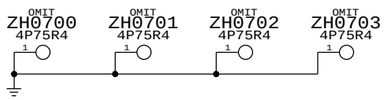
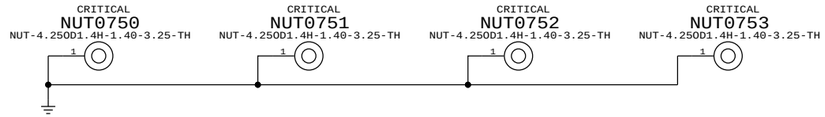
CPU Heatsink

4mm Plated Holes (998-0850)



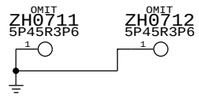
DIMM CONNECTOR NUTS

Nuts (805-9582)



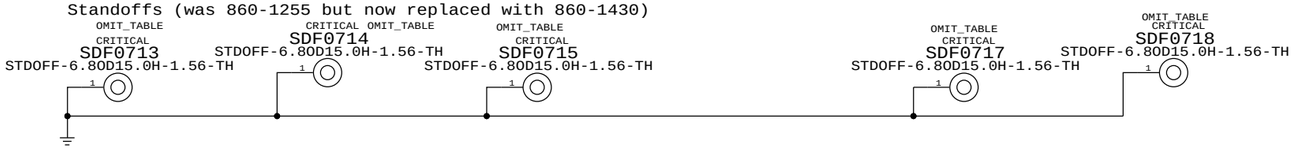
PCH HEATSINK

MOUNTING HOLES (998-0873, 998-0976)



Rear Cover

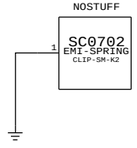
Standoffs (was 860-1255 but now replaced with 860-1430)



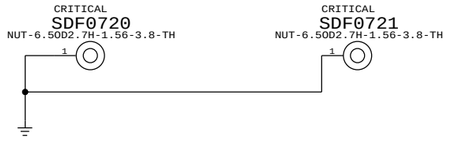
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-1430	5	STANDOFF,MLB,K60/K62	SDF0713,SDF0714,SDF0715,SDF0717,SDF0718	

For EMC

EMC Spring (870-1577); Near DIMMs



MXM STANDOFFS (835-0272)



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: Holes

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

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UNUSED CPU SIGNALS

10	TP_CPU_RSVD<16..1>	NC_CPU_RSVD<16..1>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_RSVD<46..19>	NC_CPU_RSVD<46..19>	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCI ALIASES

20	TP_PCI_AD<31..0>	NC_PCI_AD<31..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_RESET_L	NC_PCI_RESET_L	MAKE_BASE=TRUE NO_TEST=TRUE

18	TP_LPC_DREQ0_L	NC_LPC_DREQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MEM ALIASES

12	TP_MEM_A_DQ_CB<7..0>	NC_MEM_A_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_N<8>	NC_MEM_A_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_P<8>	NC_MEM_A_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQ_CB<7..0>	NC_MEM_B_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_N<8>	NC_MEM_B_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_P<8>	NC_MEM_B_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MISC ALIASES

18	TP_HDA_SDIN1	NC_HDA_SDIN1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN2	NC_HDA_SDIN2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN3	NC_HDA_SDIN3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM0	NC_PCH_PWM0	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM1	NC_PCH_PWM1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM2	NC_PCH_PWM2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM3	NC_PCH_PWM3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_SST	NC_PCH_SST	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_CLK1	NC_PCH_CL_CLK1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_DATA1	NC_PCH_CL_DATA1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_RST1	NC_PCH_CL_RST1	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCIE ALIASES

18	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7P	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7N	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_N<3..0>	NC_PE_RXN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_P<3..0>	NC_PE_RXP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_N<3..0>	NC_PE_TXN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_P<3..0>	NC_PE_TXP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_D2R_PERN4	NC_PCIE_D2R_PERN4	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_D2R_PERP4	NC_PCIE_D2R_PERP4	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_R2D_PETN4	NC_PCIE_R2D_PETN4	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_R2D_PETP4	NC_PCIE_R2D_PETP4	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED USB ALIASES

20	TP_USB_1N	NC_USB_1N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_1P	NC_USB_1P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_2N	NC_USB_2N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_2P	NC_USB_2P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_3N	NC_USB_3N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_3P	NC_USB_3P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_4N	NC_USB_4N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_4P	NC_USB_4P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_5N	NC_USB_5N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_5P	NC_USB_5P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_6N	NC_USB_6N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_6P	NC_USB_6P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_7N	NC_USB_7N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_7P	NC_USB_7P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10N	NC_USB_10N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10P	NC_USB_10P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_11N	NC_USB_11N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_11P	NC_USB_11P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_12N	NC_USB_12N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_12P	NC_USB_12P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_13N	NC_USB_13N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_13P	NC_USB_13P	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED DISPLAY ALIASES

19	TP_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_RED	NC_CRT_IG_RED	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_GREEN	NC_CRT_IG_GREEN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_BLUE	NC_CRT_IG_BLUE	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_MLN<3..0>	NC_DP_IG_B_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_MLP<3..0>	NC_DP_IG_B_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_AUX_N	NC_DP_IG_B_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_AUX_P	NC_DP_IG_B_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_HPD	NC_DP_IG_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_DDC_CLK	NC_DP_IG_B_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_DDC_DATA	NC_DP_IG_B_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_MLN<3..0>	NC_DP_IG_C_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_MLP<3..0>	NC_DP_IG_C_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_AUX_N	NC_DP_IG_C_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_AUX_P	NC_DP_IG_C_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_HPD	NC_DP_IG_C_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_CTRL_CLK	NC_DP_IG_C_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_CTRL_DATA	NC_DP_IG_C_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_MLN<3..0>	NC_DP_IG_D_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_MLP<3..0>	NC_DP_IG_D_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_AUXN	NC_DP_IG_D_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_AUXP	NC_DP_IG_D_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_HPD	NC_DP_IG_D_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_CTRL_CLK	NC_DP_IG_D_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_CTRL_DATA	NC_DP_IG_D_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINN	NC_SDVO_TVCLKINN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINP	NC_SDVO_TVCLKINP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLN	NC_SDVO_STALLN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLP	NC_SDVO_STALLP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTN	NC_SDVO_INTN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTP	NC_SDVO_INTP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTCTL	NC_PCH_L_BKLTCTL	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTEN	NC_PCH_L_BKLTEN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_VDD_EN	NC_PCH_L_VDD_EN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPN	NC_PCH_CLKOUT_DPN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPP	NC_PCH_CLKOUT_DPP	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED FDI ALIASES

10	TP_CPU_FDI_TX_N<7..0>	NC_CPU_FDI_TXN<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_TX_P<7..0>	NC_CPU_FDI_TXP<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_FDI_RX_N<7..0>	NC_PCH_FDI_RXN<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_FDI_RX_P<7..0>	NC_PCH_FDI_RXP<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED SATA ALIASES

10	TP_SATA_D_D2RN	NC_SATA_D_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_D_D2RP	NC_SATA_D_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_D_R2D_CN	NC_SATA_D_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_D_R2D_CP	NC_SATA_D_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_E_D2RN	NC_SATA_E_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_E_D2RP	NC_SATA_E_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_E_R2D_CN	NC_SATA_E_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_E_R2D_CP	NC_SATA_E_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_F_D2RN	NC_SATA_F_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_F_D2RP	NC_SATA_F_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_F_R2D_CN	NC_SATA_F_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_SATA_F_R2D_CP	NC_SATA_F_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE

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UNUSED SIGNAL ALIAS

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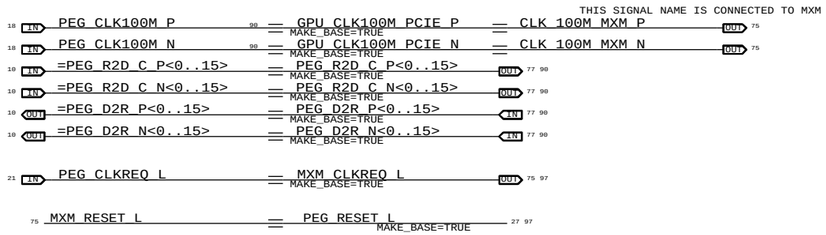
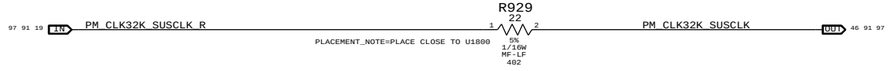
PEG Slot Support





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Signal Aliases

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SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4 MIL TRACE TO R1010.1
ROUTE B5 TO R1010.1 AS A SEPERATE 10 MIL TRACE.

OMIT
U1000
SANDY_BRIDGE
LGA1155-SKT
(1 OF 10)

DMI
DMI_RX_0* W4
DMI_RX_1* V4
DMI_RX_2* Y4
DMI_RX_3* AA5
DMI_RX_0 W5
DMI_RX_1 V3
DMI_RX_2 Y3
DMI_RX_3 AA4
DMI_TX_0* V6
DMI_TX_1* W8
DMI_TX_2* Y7
DMI_TX_3* AA8
DMI_TX_0 V7
DMI_TX_1 W7
DMI_TX_2 Y6
DMI_TX_3 AA7

FLEXIBLE DISPLAY INTERFACE
(Unused)
FDI_TX_0* AC7
FDI_TX_1* AC3
FDI_TX_2* AD1
FDI_TX_3* AD3
FDI_TX_4* AD6
FDI_TX_5* AE8
FDI_TX_6* AF2
FDI_TX_7* AG1
FDI_TX_0 AC8
FDI_TX_1 AC2
FDI_TX_2 AD2
FDI_TX_3 AD4
FDI_TX_4 AD7
FDI_TX_5 AE7
FDI_TX_6 AF3
FDI_TX_7 AG2
FDI_FSYNC_0 AC5
FDI_FSYNC_1 AE5
FDI_INT AG3
FDI_LSYNC_0 AC4
FDI_LSYNC_1 AE4
FDI_COMPIO AE2
FDI_ICOMPO AE1

PCI EXPRESS -- GRAPHICS
(Available for Workstation only)
PCI EXPRESS
PE_RX_0* P4
PE_RX_1* R1
PE_RX_2* T3
PE_RX_3* U1
PE_RX_0 P3
PE_RX_1 R2
PE_RX_2 T4
PE_RX_3 U2
PE_TX_0* P7
PE_TX_1* T8
PE_TX_2* R5
PE_TX_3* U6
PE_TX_0 P8
PE_TX_1 T7
PE_TX_2 R6
PE_TX_3 U5

PEG_COMPI B4
PEG_ICOMPO B5
PEG_RCOMPO C4
PEG_RX_0* B12
PEG_RX_1* D11
PEG_RX_2* C9
PEG_RX_3* E9
PEG_RX_4* B7
PEG_RX_5* C5
PEG_RX_6* A6
PEG_RX_7* E1
PEG_RX_8* F3
PEG_RX_9* G1
PEG_RX_10* H4
PEG_RX_11* J2
PEG_RX_12* K4
PEG_RX_13* L2
PEG_RX_14* M4
PEG_RX_15* N2
PEG_RX_0 B11
PEG_RX_1 D12
PEG_RX_2 C10
PEG_RX_3 E10
PEG_RX_4 B8
PEG_RX_5 C6
PEG_RX_6 A5
PEG_RX_7 E2
PEG_RX_8 F4
PEG_RX_9 G2
PEG_RX_10 H3
PEG_RX_11 J1
PEG_RX_12 K3
PEG_RX_13 L1
PEG_RX_14 M3
PEG_RX_15 N1
PEG_TX_0* C14
PEG_TX_1* E13
PEG_TX_2* G13
PEG_TX_3* F11
PEG_TX_4* J13
PEG_TX_5* D7
PEG_TX_6* C3
PEG_TX_7* E5
PEG_TX_8* F7
PEG_TX_9* G9
PEG_TX_10* G6
PEG_TX_11* K8
PEG_TX_12* J6
PEG_TX_13* M7
PEG_TX_14* L5
PEG_TX_15* N6
PEG_TX_0 C13
PEG_TX_1 E14
PEG_TX_2 G14
PEG_TX_3 F12
PEG_TX_4 J14
PEG_TX_5 D8
PEG_TX_6 D3
PEG_TX_7 E6
PEG_TX_8 F8
PEG_TX_9 G10
PEG_TX_10 G5
PEG_TX_11 K7
PEG_TX_12 J5
PEG_TX_13 M8
PEG_TX_14 L6
PEG_TX_15 N5

PLACEMENT_NOTE=Place within 12.7MM of CPU
R1010 24.9 1% 1/10W MF-LF 402
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=CPU_RCOMP
CPU_PEG_COMP
=PPVCCIO_S0_CPU

PLACEMENT_NOTE=Place within 12.7MM of CPU
R1011 0 5% 1/10W MF-LF 402
CPU_FDI_COMPIO

OMIT
U1000
SANDY_BRIDGE
LGA1155-SKT
(5 OF 10)

RESERVED
RSVD_C38 TP_CPU_RSVD<1>
RSVD_C39 TP_CPU_RSVD<2>
RSVD_D38 TP_CPU_RSVD<3>
RSVD_H7 TP_CPU_RSVD<4>
RSVD_H8 TP_CPU_RSVD<5>
RSVD_J9 TP_CPU_RSVD<6>
RSVD_J31 TP_CPU_RSVD<7>
RSVD_J33 TP_CPU_RSVD<8>
RSVD_J34 TP_CPU_RSVD<9>
RSVD_K9 TP_CPU_RSVD<10>
RSVD_K31 TP_CPU_RSVD<11>
RSVD_K34 TP_CPU_RSVD<12>
RSVD_L9 TP_CPU_RSVD<13>
RSVD_L31 TP_CPU_RSVD<14>
RSVD_L33 TP_CPU_RSVD<15>
RSVD_L34 TP_CPU_RSVD<16>
RSVD_M34 ThermDC SNS_CPU_THERMD_N
RSVD_N33 ThermDA SNS_CPU_THERMD_P
RSVD_N34 TP_CPU_RSVD<19>
CFG_0 CPU_CFG<0>
CFG_1 CPU_CFG<1>
CFG_2 CPU_CFG<2>
CFG_3 CPU_CFG<3>
CFG_4 CPU_CFG<4>
CFG_5 CPU_CFG<5>
CFG_6 CPU_CFG<6>
CFG_7 CPU_CFG<7>
CFG_8 CPU_CFG<8>
CFG_9 CPU_CFG<9>
CFG_10 CPU_CFG<10>
CFG_11 CPU_CFG<11>
CFG_12 CPU_CFG<12>
CFG_13 CPU_CFG<13>
CFG_14 CPU_CFG<14>
CFG_15 CPU_CFG<15>
CFG_16 CPU_CFG<16>
CFG_17 CPU_CFG<17>
RSVD_P35 P35 TP_CPU_RSVD<20>
RSVD_P37 P37 TP_CPU_RSVD<21>
RSVD_P39 P39 TP_CPU_RSVD<22>
RSVD_R34 R34 TP_CPU_RSVD<23>
RSVD_R36 R36 TP_CPU_RSVD<24>
RSVD_R38 R38 TP_CPU_RSVD<25>
RSVD_R40 R40 TP_CPU_RSVD<26>
RSVD_AB6 AB6 TP_CPU_RSVD<27>
RSVD_AB7 AB7 TP_CPU_RSVD<28>
RSVD_AD34 AD34 TP_CPU_RSVD<29>
RSVD_AD35 AD35 TP_CPU_RSVD<30>
RSVD_AD37 AD37 TP_CPU_RSVD<31>
RSVD_AE6 AE6 TP_CPU_RSVD<32>
RSVD_AF4 AF4 TP_CPU_RSVD<33>
RSVD_AG4 AG4 TP_CPU_RSVD<34>
RSVD_AJ11 AJ11 TP_CPU_RSVD<35>
RSVD_AJ29 AJ29 TP_CPU_RSVD<36>
RSVD_AJ30 AJ30 TP_CPU_RSVD<37>
RSVD_AJ31 AJ31 TP_CPU_RSVD<38>
RSVD_AN20 AN20 TP_CPU_RSVD<39>
RSVD_AP20 AP20 TP_CPU_RSVD<40>
RSVD_AT11 AT11 TP_CPU_RSVD<41>
RSVD_AT14 AT14 TP_CPU_RSVD<42>
RSVD_AU10 AU10 TP_CPU_RSVD<43>
RSVD_AV34 AV34 TP_CPU_RSVD<44>
RSVD_AW34 AW34 TP_CPU_RSVD<45>
RSVD_AY10 AY10 TP_CPU_RSVD<46>
RSVD_NCTF_AV1 AV1 TP_CPU_RSVD_NCTF<1>
RSVD_NCTF_AW2 AW2 TP_CPU_RSVD_NCTF<2>
RSVD_NCTF_AY3 AY3 TP_CPU_RSVD_NCTF<3>
RSVD_NCTF_B39 B39 TP_CPU_RSVD_NCTF<4>
NCTF_A38 A38 TP_CPU_NCTF<1>
NCTF_C2 C2 TP_CPU_NCTF<2>
NCTF_D1 D1 TP_CPU_NCTF<3>
NCTF_AU40 AU40 TP_CPU_NCTF<4>
NCTF_AW38 AW38 TP_CPU_NCTF<5>

INTEL SUGGESTS TO KEEP THESE TPS

FOR SANDYBRIDGE PROCESSOR

CFG [6:5] :PCIE CONFIGURATION SELECT 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [2] :PCIE LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

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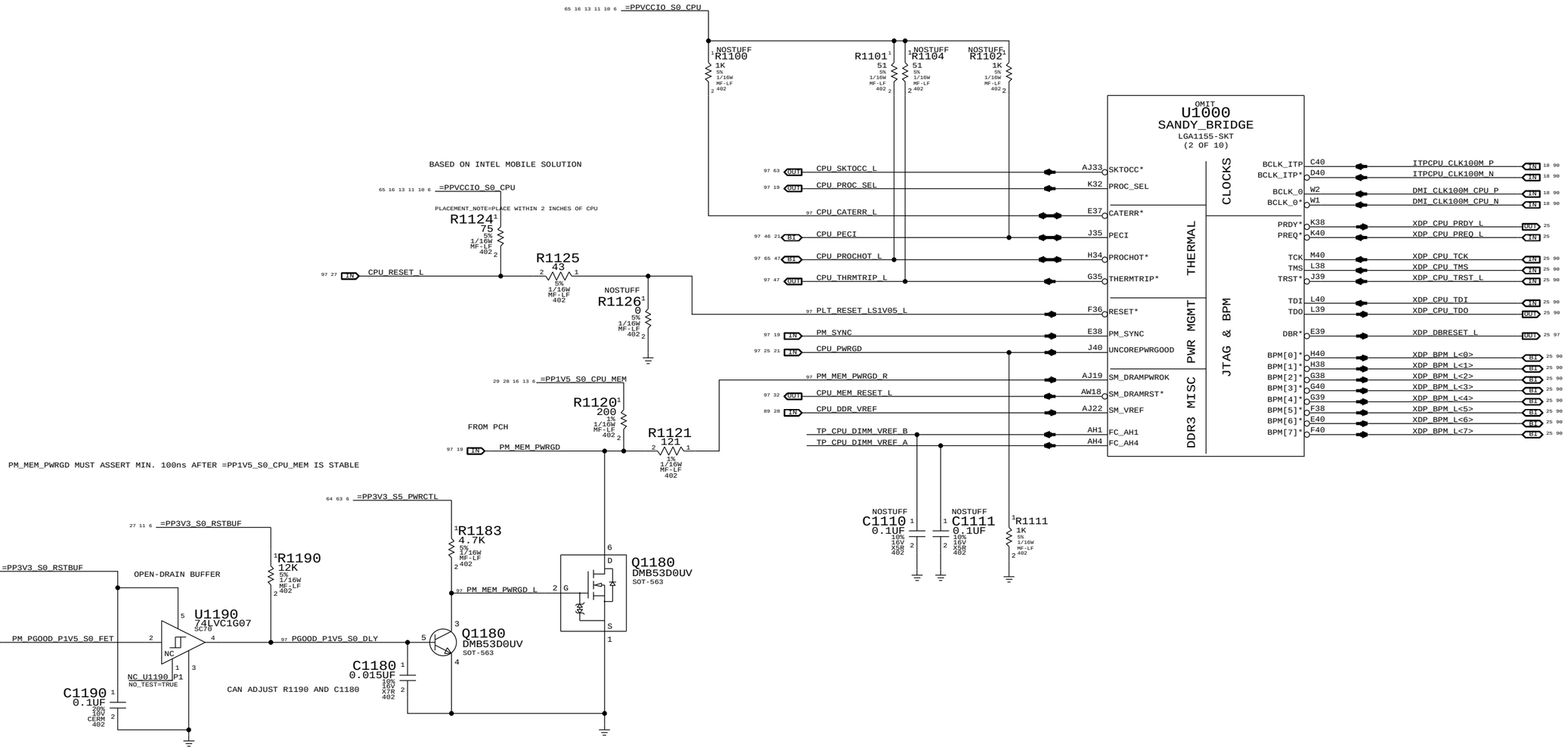

PAGE TITLE	CPU CLOCK/MISC/JTAG
	Apple Inc.
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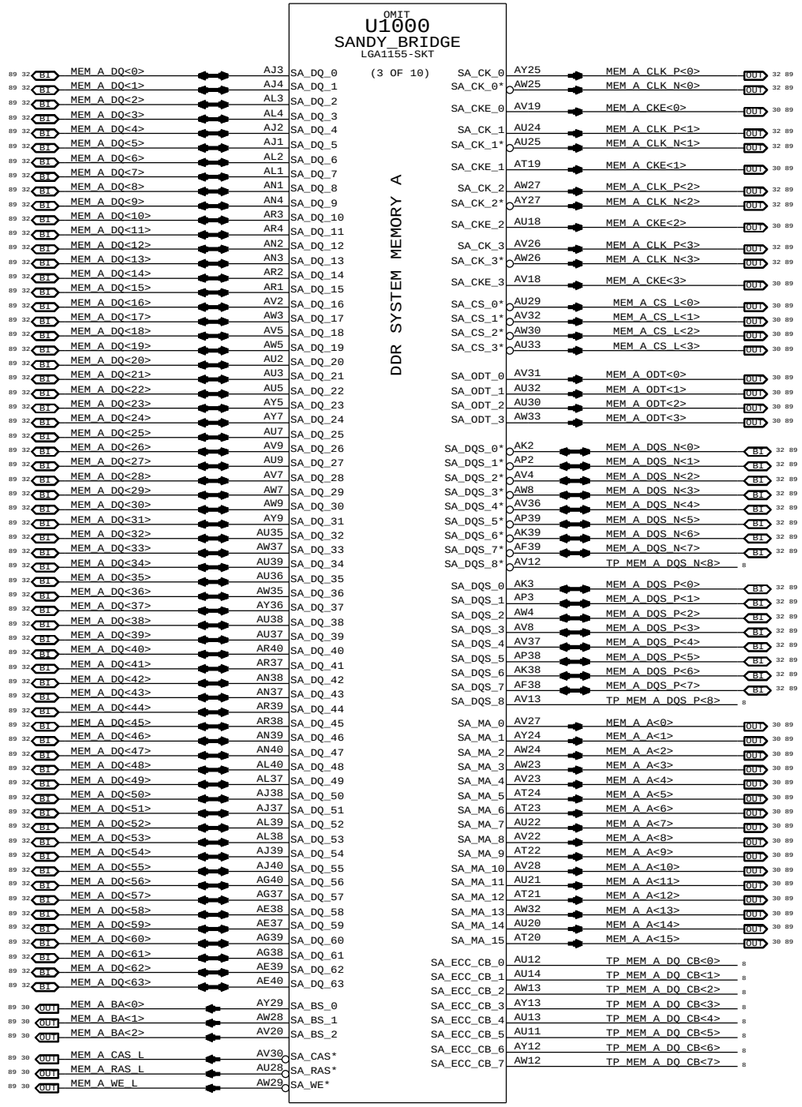

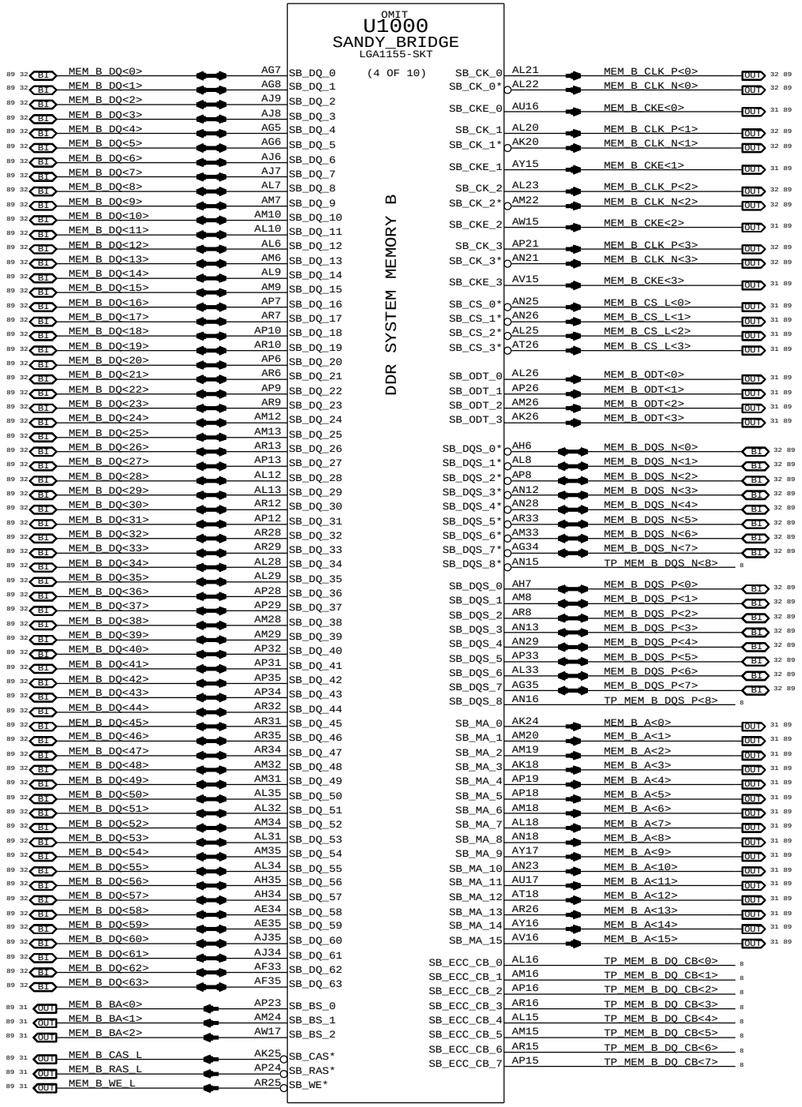

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PAGE TITLE
CPU DDR3 INTERFACES

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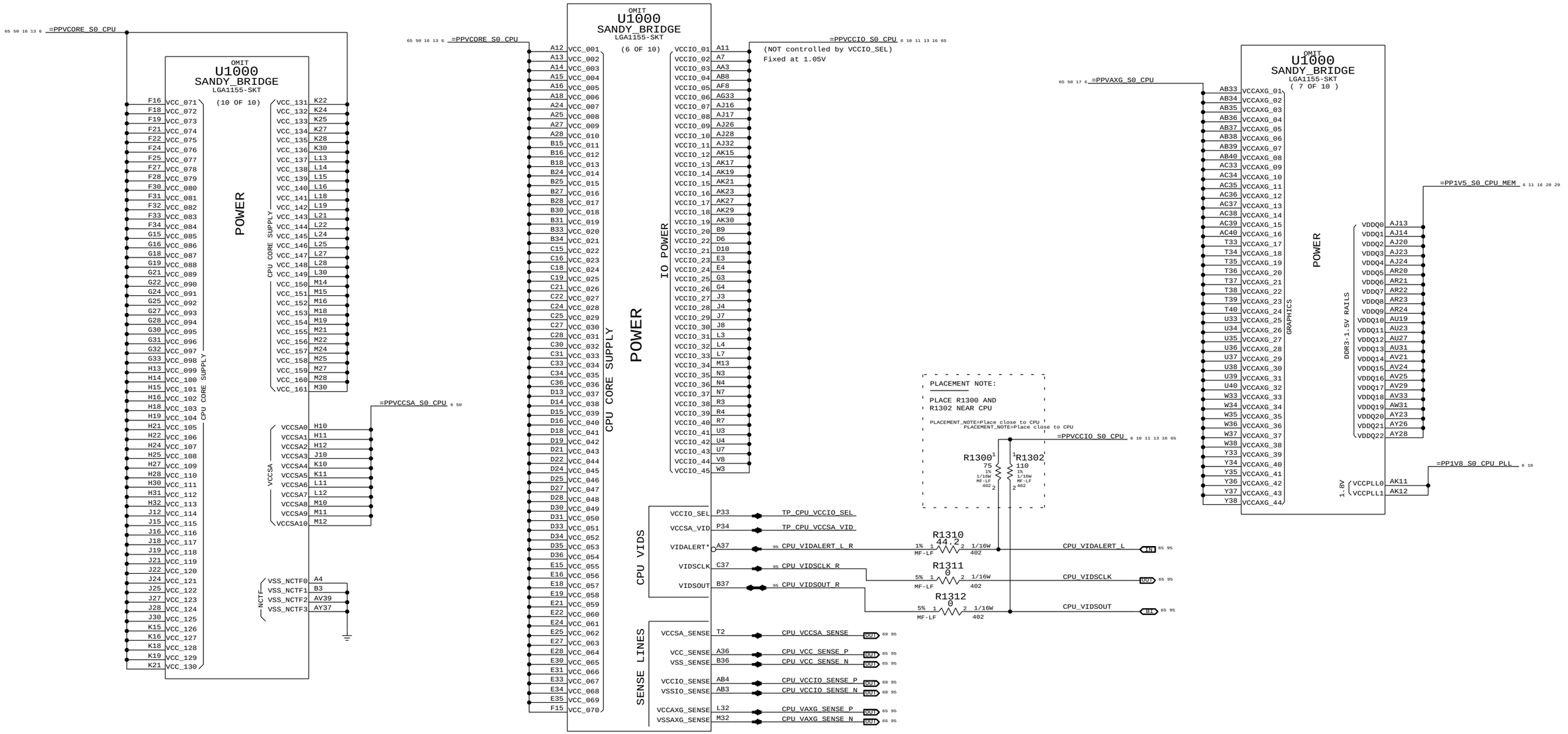

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PAGE TITLE
CPU POWER

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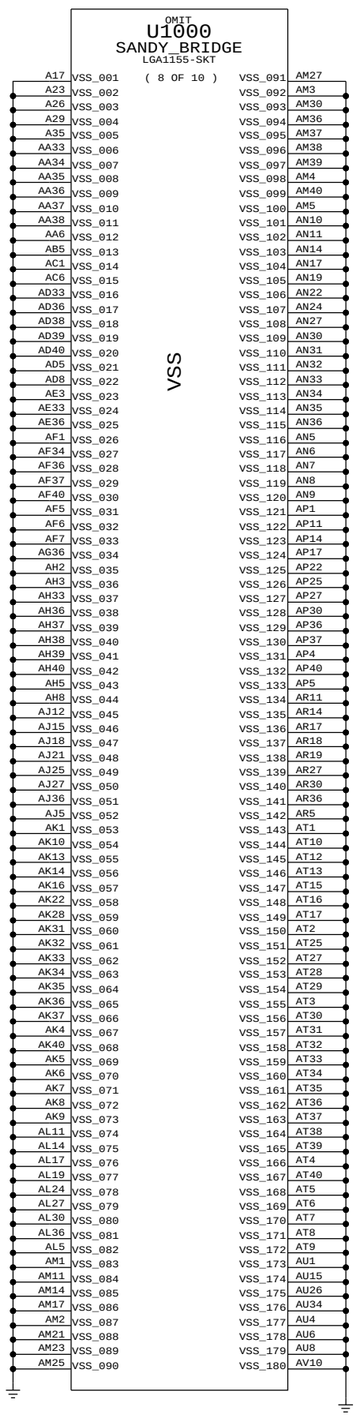

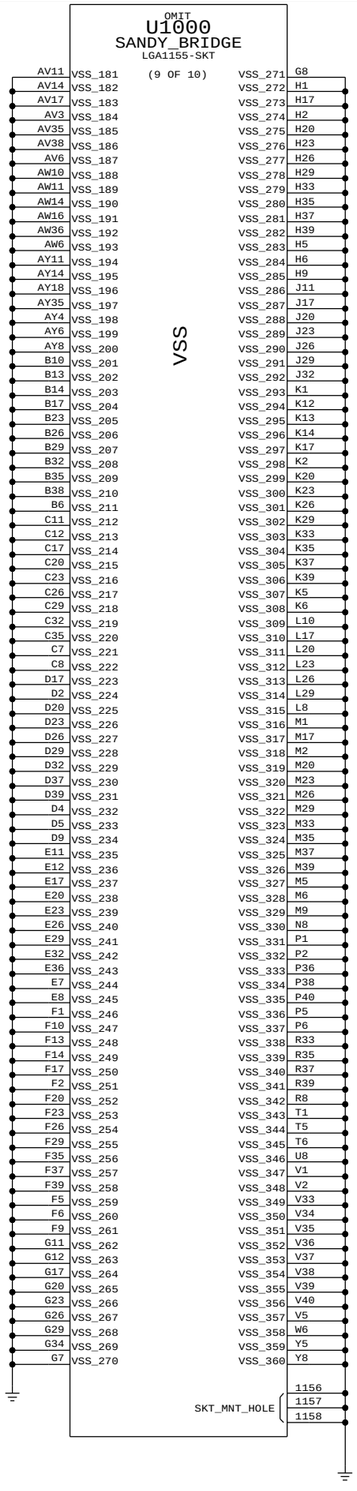

PAGE TITLE

CPU GROUNDS

Apple Inc.

DRAWING NUMBER 051-8115

SIZE D

REVISION 11.1.0

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PAGE 14 OF 110

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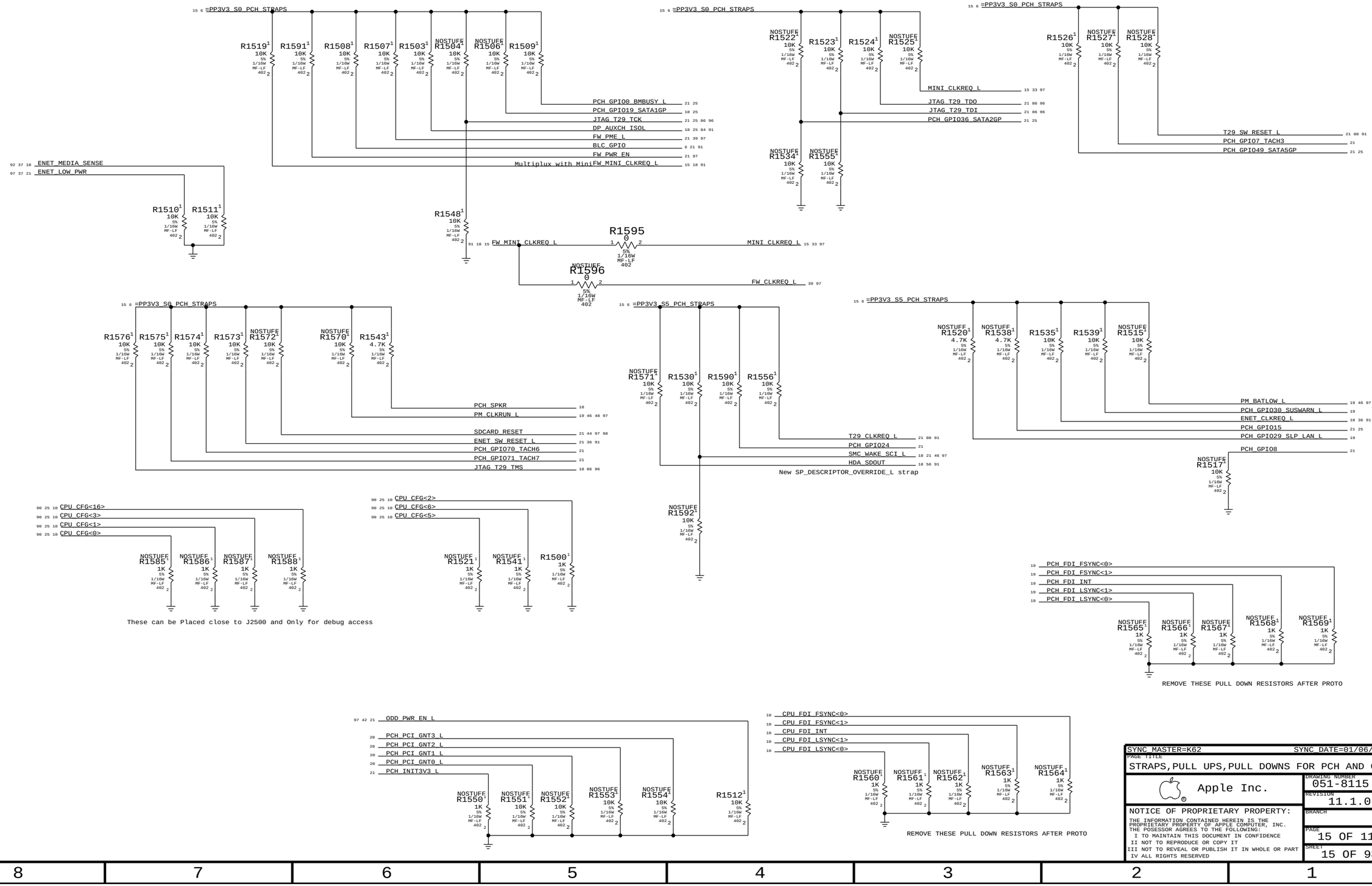
15 6 =PP3V3_S0_PCH_STRAPS
R1519 1 10K 5% 1/16W MF-LF 402
R1591 1 10K 5% 1/16W MF-LF 402
R1508 1 10K 5% 1/16W MF-LF 402
R1507 1 10K 5% 1/16W MF-LF 402
R1503 1 10K 5% 1/16W MF-LF 402
NOSTUFF R1504 1 10K 5% 1/16W MF-LF 402
NOSTUFF R1506 1 10K 5% 1/16W MF-LF 402
R1509 1 10K 5% 1/16W MF-LF 402
PCH_GPIO0_BMBUSY_L 21 25
PCH_GPIO19_SATA1GP 18 25
JTAG_T29_TCK 21 25 86 96
DP_AUXCH_ISOL 18 25 84 91
FW_PME_L 21 39 97
BLC_GPIO 6 21 91
FW_PWR_EN 21 97
Multiplux with Mini FW_MINI_CLKREQ_L 15 18 91
92 37 18 ENET_MEDIA_SENSE
97 37 21 ENET_LOW_PWR
R1510 1 10K 5% 1/16W MF-LF 402
R1511 1 10K 5% 1/16W MF-LF 402
R1548 1 10K 5% 1/16W MF-LF 402
91 18 15 FW_MINI_CLKREQ_L
R1595 0 5% 1/16W MF-LF 402
MINI_CLKREQ_L 15 33 97
NOSTUFF R1596 0 5% 1/16W MF-LF 402
FW_CLKREQ_L 39 97
15 6 =PP3V3_S0_PCH_STRAPS
NOSTUFF R1522 10K 5% 1/16W MF-LF 402
R1523 1 10K 5% 1/16W MF-LF 402
R1524 1 10K 5% 1/16W MF-LF 402
NOSTUFF R1525 10K 5% 1/16W MF-LF 402
MINI_CLKREQ_L 15 33 97
JTAG_T29_TDO 21 86 96
JTAG_T29_TDI 21 86 96
PCH_GPIO36_SATA2GP 21 25
NOSTUFF R1534 10K 5% 1/16W MF-LF 402
NOSTUFF R1555 10K 5% 1/16W MF-LF 402
15 6 =PP3V3_S0_PCH_STRAPS
R1526 1 10K 5% 1/16W MF-LF 402
NOSTUFF R1527 10K 5% 1/16W MF-LF 402
NOSTUFF R1528 10K 5% 1/16W MF-LF 402
T29_SW_RESET_L 21 80 91
PCH_GPIO7_TACH3 21
PCH_GPIO49_SATA5GP 21 25
15 6 =PP3V3_S0_PCH_STRAPS
R1576 1 10K 5% 1/16W MF-LF 402
R1575 1 10K 5% 1/16W MF-LF 402
R1574 1 10K 5% 1/16W MF-LF 402
R1573 1 10K 5% 1/16W MF-LF 402
NOSTUFF R1572 10K 5% 1/16W MF-LF 402
NOSTUFF R1570 10K 5% 1/16W MF-LF 402
R1543 1 4.7K 5% 1/16W MF-LF 402
PCH_SPKR 18
PM_CLKRUN_L 19 46 48 97
SDCARD_RESET 21 44 97 98
ENET_SW_RESET_L 21 36 91
PCH_GPIO70_TACH6 21
PCH_GPIO71_TACH7 21
JTAG_T29_TMS 18 86 96
15 6 =PP3V3_S5_PCH_STRAPS
NOSTUFF R1571 10K 5% 1/16W MF-LF 402
R1530 1 10K 5% 1/16W MF-LF 402
R1590 1 10K 5% 1/16W MF-LF 402
R1556 1 10K 5% 1/16W MF-LF 402
T29_CLKREQ_L 21 80 91
PCH_GPIO24 21
SMC_WAKE_SCI_L 18 21 46 97
HDA_SDOUT 18 56 91
New SP_DESCRIPTOR_OVERRIDE_L strap
NOSTUFF R1592 10K 5% 1/16W MF-LF 402
15 6 =PP3V3_S5_PCH_STRAPS
NOSTUFF R1520 4.7K 5% 1/16W MF-LF 402
NOSTUFF R1538 4.7K 5% 1/16W MF-LF 402
R1535 1 10K 5% 1/16W MF-LF 402
R1539 1 10K 5% 1/16W MF-LF 402
NOSTUFF R1515 10K 5% 1/16W MF-LF 402
PM_BATLOW_L 19 46 97
PCH_GPIO30_SUSWARN_L 19
ENET_CLKREQ_L 18 36 91
PCH_GPIO15 21 25
PCH_GPIO29_SLP_LAN_L 19
PCH_GPIO8 21
NOSTUFF R1517 10K 5% 1/16W MF-LF 402
90 25 10 CPU_CFG<16>
90 25 10 CPU_CFG<3>
90 25 10 CPU_CFG<1>
90 25 10 CPU_CFG<0>
NOSTUFF R1585 1K 5% 1/16W MF-LF 402
NOSTUFF R1586 1K 5% 1/16W MF-LF 402
NOSTUFF R1587 1K 5% 1/16W MF-LF 402
NOSTUFF R1588 1K 5% 1/16W MF-LF 402
These can be Placed close to J2500 and Only for debug access
90 25 10 CPU_CFG<2>
90 25 10 CPU_CFG<6>
90 25 10 CPU_CFG<5>
NOSTUFF R1521 1K 5% 1/16W MF-LF 402
NOSTUFF R1541 1K 5% 1/16W MF-LF 402
R1500 1K 5% 1/16W MF-LF 402
19 PCH_FDI_FSYNC<0>
19 PCH_FDI_FSYNC<1>
19 PCH_FDI_INT
19 PCH_FDI_LSYNC<1>
19 PCH_FDI_LSYNC<0>
NOSTUFF R1565 1K 5% 1/16W MF-LF 402
NOSTUFF R1566 1K 5% 1/16W MF-LF 402
NOSTUFF R1567 1K 5% 1/16W MF-LF 402
NOSTUFF R1568 1K 5% 1/16W MF-LF 402
NOSTUFF R1569 1K 5% 1/16W MF-LF 402
REMOVE THESE PULL DOWN RESISTORS AFTER PROTO
97 42 21 ODD_PWR_EN_L
20 PCH_PCI_GNT3_L
20 PCH_PCI_GNT2_L
20 PCH_PCI_GNT1_L
20 PCH_PCI_GNT0_L
21 PCH_INIT3V3_L
NOSTUFF R1550 1K 5% 1/16W MF-LF 402
NOSTUFF R1551 10K 5% 1/16W MF-LF 402
NOSTUFF R1552 10K 5% 1/16W MF-LF 402
R1553 10K 5% 1/16W MF-LF 402
R1554 10K 5% 1/16W MF-LF 402
R1512 10K 5% 1/16W MF-LF 402
10 CPU_FDI_FSYNC<0>
10 CPU_FDI_FSYNC<1>
10 CPU_FDI_INT
10 CPU_FDI_LSYNC<1>
10 CPU_FDI_LSYNC<0>
NOSTUFF R1560 1K 5% 1/16W MF-LF 402
NOSTUFF R1561 1K 5% 1/16W MF-LF 402
NOSTUFF R1562 1K 5% 1/16W MF-LF 402
NOSTUFF R1563 1K 5% 1/16W MF-LF 402
NOSTUFF R1564 1K 5% 1/16W MF-LF 402
REMOVE THESE PULL DOWN RESISTORS AFTER PROTO
SYNC_MASTER=K62
SYNC_DATE=01/06/2011
PAGE TITLE
STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU
Apple Inc.
DRAWING NUMBER 051-8115
SIZE D
REVISION 11.1.0
BRANCH
PAGE 15 OF 110
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CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

16 13 6 =PPVCORE_S0_CPU
65 50

PLACEMENT_NOTE (C1600-C1613):

Place inside socket cavity

C1600	C1601	C1602	C1603	C1604	C1605	C1606	C1607	C1608	C1609
22UF	22UF	22UF	22UF	22UF	22UF	22UF	22UF	22UF	22UF
20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
6.3V	6.3V	6.3V	6.3V	6.3V	6.3V	6.3V	6.3V	6.3V	6.3V
CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R
805-3	805-3	805-3	805-3	805-3	805-3	805-3	805-3	805-3	805-3

C1610	C1611	C1612	C1613
22UF	22UF	22UF	22UF
20%	20%	20%	20%
6.3V	6.3V	6.3V	6.3V
CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R
805-3	805-3	805-3	805-3

BULK CAPS ON CPU VREG PAGE 72

10x 10UF and 10x 1UF CAPACITORS

65 50 16 13 6 =PPVCORE_S0_CPU

Place inside socket cavity

C1620	C1621	C1622	C1623	C1624	C1625	C1626	C1627	C1628	C1629
10UF	10UF	10UF	10UF	10UF	10UF	10UF	10UF	10UF	10UF
20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
10V	10V	10V	10V	10V	10V	10V	10V	10V	10V
X5R	X5R	X5R	X5R	X5R	X5R	X5R	X5R	X5R	X5R
603	603	603	603	603	603	603	603	603	603

C1630	C1631	C1632	C1633	C1634	C1635	C1636	C1637	C1638	C1639
1UF	1UF	1UF	1UF	1UF	1UF	1UF	1UF	1UF	1UF
10%	10%	10%	10%	10%	10%	10%	10%	10%	10%
16V	16V	16V	16V	16V	16V	16V	16V	16V	16V
X5R	X5R	X5R	X5R	X5R	X5R	X5R	X5R	X5R	X5R
402	402	402	402	402	402	402	402	402	402

CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

13 11 10 6 6s =PPVCCIO_S0_CPU

PLACEMENT_NOTE (C1650-C1657):

Place under socket cavity on secondary side.

C1650	C1651	C1652	C1653	C1654	C1655	C1656	C1657
22UF	22UF	22UF	22UF	22UF	22UF	22UF	22UF
20%	20%	20%	20%	20%	20%	20%	20%
6.3V	6.3V	6.3V	6.3V	6.3V	6.3V	6.3V	6.3V
CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R
805	805	805	805	805	805	805	805

PLACEMENT_NOTE (C1660-C1665):

Place at edge of socket.

BULK CAPS ON CPU VREG PAGE 72

C1660	C1661	C1662	C1663	C1664	C1665
10uF	10uF	10uF	10uF	10uF	10uF
20%	20%	20%	20%	20%	20%
6.3V	6.3V	6.3V	6.3V	6.3V	6.3V
X5R	X5R	X5R	X5R	X5R	X5R
603	603	603	603	603	603

C1670
330UF-0.0045OHM
20%
2V
POLY
CASE-D2-SM

Memory (CPU VCCDDR) DECOUPLING

6x 22uF 0805, 5x 1uF 0402. INTEL RECOMMENDATION 9X 22uF 0805

28 13 11 6 29 =PP1V5_S0_CPU_MEM

C1676	C1677	C1678	C1679	C1680	C1681	C1682	C1683	C1684	C1685	C1686
22uF	22uF	22uF	22uF	22uF	22uF	1UF	1UF	1UF	1UF	1UF
20%	20%	20%	20%	20%	20%	10%	10%	10%	10%	10%
6.3V	6.3V	6.3V	6.3V	6.3V	6.3V	10V	10V	16V	16V	16V
CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R	CERM-X5R	X5R	X5R	X5R	X5R	X5R
805	805	805	805	805	805	402	402	402	402	402

PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 10x 10uF 0805

13 6 =PP1V8_S0_CPU_PLL

C1693	C1694	C1692	C1691	C1695	C1690	C1696	C1697
1UF	1UF	2.2UF	4.7UF	10UF	22uF	47UF	47UF
10%	10%	10%	10%	20%	20%	20%	20%
10V	10V	6.3V	6.3V	6.3V	6.3V	6.3V	6.3V
X5R	X5R	X5R	X5R-CERM	X5R	CERM-X5R	X5R	X5R
402	402	402	603	603	805	0805	0805

BULK CAPS ON VTT REG PAGE 78

Note: VCCSA decoupling is on regulator page

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
CPU NON-GFX DECOUPLING

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
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VAXG DECOUPLING

INTEL RECOMMENDATION 6X22UF 0805,3X 4.7UF

PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity

65 50 13 6 =PPVAXG_S0_CPU

VAXG C1704 22UF 20% 6.3V CERM-X5R 805-3	VAXG C1705 22UF 20% 6.3V CERM-X5R 805-3	VAXG C1706 22UF 20% 6.3V CERM-X5R 805-3	VAXG C1707 22UF 20% 6.3V CERM-X5R 805-3	VAXG C1708 22UF 20% 6.3V CERM-X5R 805-3	VAXG C1709 22UF 20% 6.3V CERM-X5R 805-3

OMIT C1710 4.7UF 10% 6.3V X5R-CERM 603	VAXG C1711 4.7UF 10% 6.3V X5R-CERM 603	VAXG C1712 4.7UF 10% 6.3V X5R-CERM 603

BULK CAPS ON CPU VREG PAGE 73

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
138S0586	1	CAP,4.7UF,10%,6.3V,0603	C1710	VAXG
113S0022	1	RES,0 OHM,5%,0603	C1710	NO_VAXG

6 =PP3V3_S0_PCH_VCCADAC — R1750 0 5% 1/16W MF-LF 402 — PP3V3_S0_PCH_VCCA_DAC_F (22 95)
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

6 =PP1V05_S0_PCH_VCCADPLL — R1760 0 5% 1/16W MF-LF 402 — PP1V05_S0_PCH_VCCADPLLA_F (22 95)
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V

R1765 0 5% 1/16W MF-LF 402 — PP1V05_S0_PCH_VCCADPLLB_F (22 95)
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
GFX DECOUPLING & PCH PWR ALIAS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
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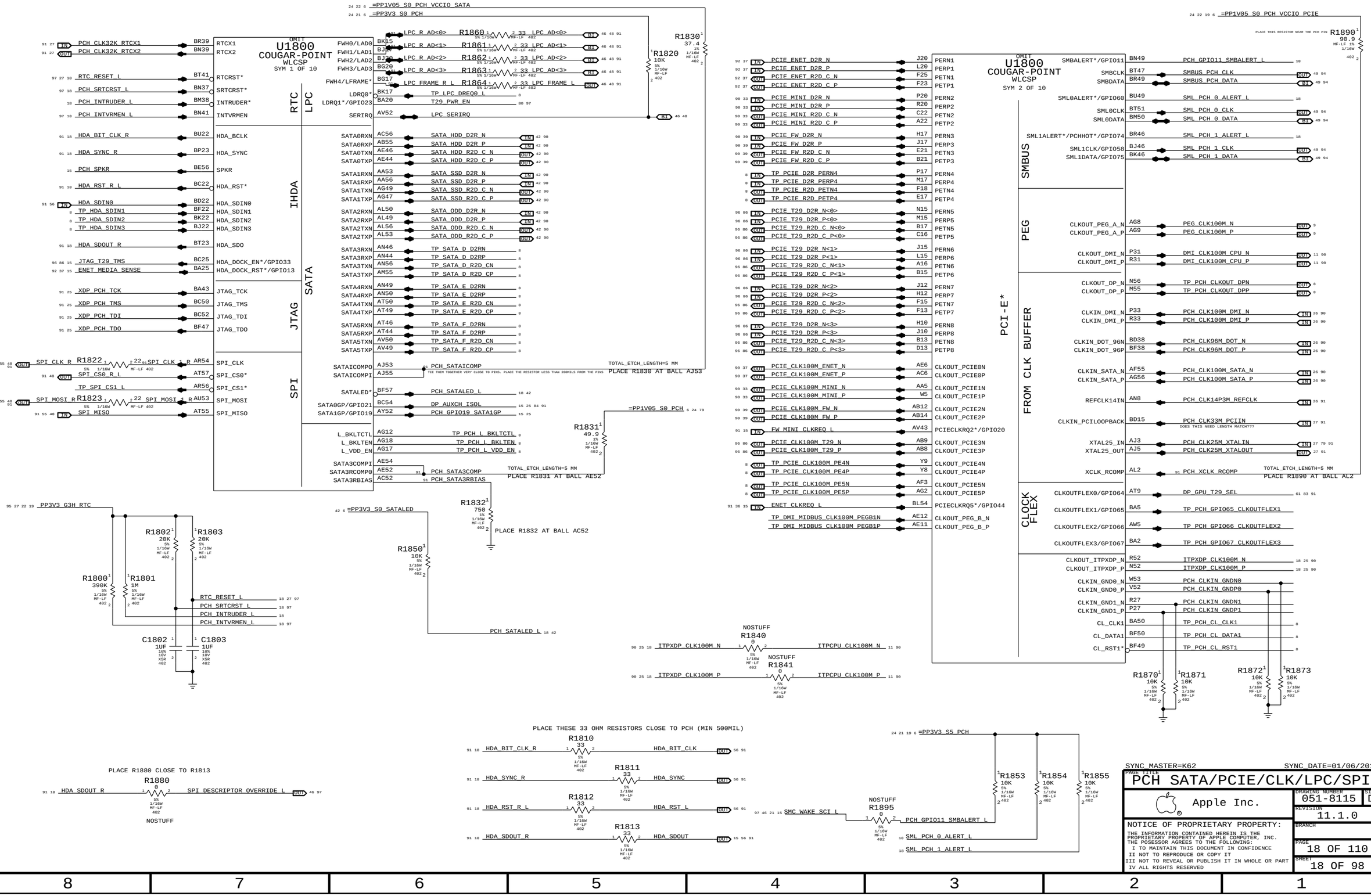
U1800
COUGAR-POINT
WLCSP
SYM 1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
PCI-E*
FROM CLK BUFFER
SMBUS
PEG
CLOCK FLEX
PCH_CLK32K_RTCX1
PCH_CLK32K_RTCX2
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
HDA_BIT_CLK_R
HDA_SYNC_R
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
JTAG_T29_TMS
ENET_MEDIA_SENSE
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
SPI_MOSI_R
SPI_MISO
LPC_R_AD<0>
LPC_R_AD<1>
LPC_R_AD<2>
LPC_R_AD<3>
LPC_FRAME_R_L
TP_LPC_DREQ0_L
T29_PWR_EN
LPC_SERIRQ
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA_SSD_D2R_N
SATA_SSD_D2R_P
SATA_SSD_R2D_C_N
SATA_SSD_R2D_C_P
SATA_ODD_D2R_N
SATA_ODD_D2R_P
SATA_ODD_R2D_C_N
SATA_ODD_R2D_C_P
TP_SATA_D_D2RN
TP_SATA_D_D2RP
TP_SATA_D_R2D_CN
TP_SATA_D_R2D_CP
TP_SATA_E_D2RN
TP_SATA_E_D2RP
TP_SATA_E_R2D_CN
TP_SATA_E_R2D_CP
TP_SATA_F_D2RN
TP_SATA_F_D2RP
TP_SATA_F_R2D_CN
TP_SATA_F_R2D_CP
PCH_SATAICOMP
PCH_SATALED_L
DP_AUXCH_ISOL
PCH_GPIO19_SATA1GP
TP_PCH_L_BKLTCTL
TP_PCH_L_BKLTEN
TP_PCH_L_VDD_EN
PCH_SATA3COMP
PCH_SATA3RBIAS
=PP1V05_S0_PCH_VCCIO_SATA
=PP3V3_S0_PCH
=PP1V05_S0_PCH
=PP3V3_S0_SATALED
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_MINI_D2R_N
PCIE_MINI_D2R_P
PCIE_MINI_R2D_C_N
PCIE_MINI_R2D_C_P
PCIE_FW_D2R_N
PCIE_FW_D2R_P
PCIE_FW_R2D_C_N
PCIE_FW_R2D_C_P
TP_PCIE_D2R_PERN4
TP_PCIE_D2R_PERP4
TP_PCIE_R2D_PETN4
TP_PCIE_R2D_PETP4
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PCIE_T29_D2R_P<0>
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PCIE_T29_D2R_P<1>
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PCIE_T29_D2R_P<3>
PCIE_T29_R2D_C_N<3>
PCIE_T29_R2D_C_P<3>
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PCIE_CLK100M_ENET_P
PCIE_CLK100M_MINI_N
PCIE_CLK100M_MINI_P
PCIE_CLK100M_FW_N
PCIE_CLK100M_FW_P
FW_MINI_CLKREQ_L
PCIE_CLK100M_T29_N
PCIE_CLK100M_T29_P
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
TP_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P
ENET_CLKREQ_L
TP_DMI_MIDBUS_CLK100M_PEGB1N
TP_DMI_MIDBUS_CLK100M_PEGB1P
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2*/GPIO20
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5*/GPIO44
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
SMBUS_PCH_CLK
SMBUS_PCH_DATA
SML_PCH_0_ALERT_L
SML_PCH_0_CLK
SML_PCH_0_DATA
SML_PCH_1_ALERT_L
SML_PCH_1_CLK
SML_PCH_1_DATA
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
PEG_CLK100M_N
PEG_CLK100M_P
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
TP_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP
PCH_CLK100M_DMI_N
PCH_CLK100M_DMI_P
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
PCH_CLK25M_XTALIN
PCH_CLK25M_XTALOUT
PCH_XCLK_RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
DP_GPU_T29_SEL
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
CLKIN_GND0_N
CLKIN_GND0_P
CLKIN_GND1_N
CLKIN_GND1_P
PCH_CLKIN_GNDN0
PCH_CLKIN_GNDP0
PCH_CLKIN_GNDN1
PCH_CLKIN_GNDP1
CL_CLK1
CL_DATA1
CL_RST1*
TP_PCH_CL_CLK1
TP_PCH_CL_DATA1
TP_PCH_CL_RST1
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
ITPCPU_CLK100M_N
ITPCPU_CLK100M_P
PP3V3_G3H_RTC
=PP3V3_S5_PCH
SMC_WAKE_SCI_L
PCH_GPIO11_SMBALERT_L
SML_PCH_0_ALERT_L
SML_PCH_1_ALERT_L
PLACE THESE 33 OHM RESISTORS CLOSE TO PCH (MIN 500MIL)
PLACE R1880 CLOSE TO R1813
NOSTUFF
TOTAL_ETCH_LENGTH=5 MM
PLACE R1830 AT BALL AJ53
PLACE R1831 AT BALL AE52
PLACE R1832 AT BALL AC52
PLACE R1890 AT BALL AL2
PLACE THIS RESISTOR NEAR THE PCH PIN
SYNC_MASTER=K62
SYNC_DATE=01/06/2011
PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER
051-8115
SIZE
D
REVISION
11.1.0
BRANCH
PAGE
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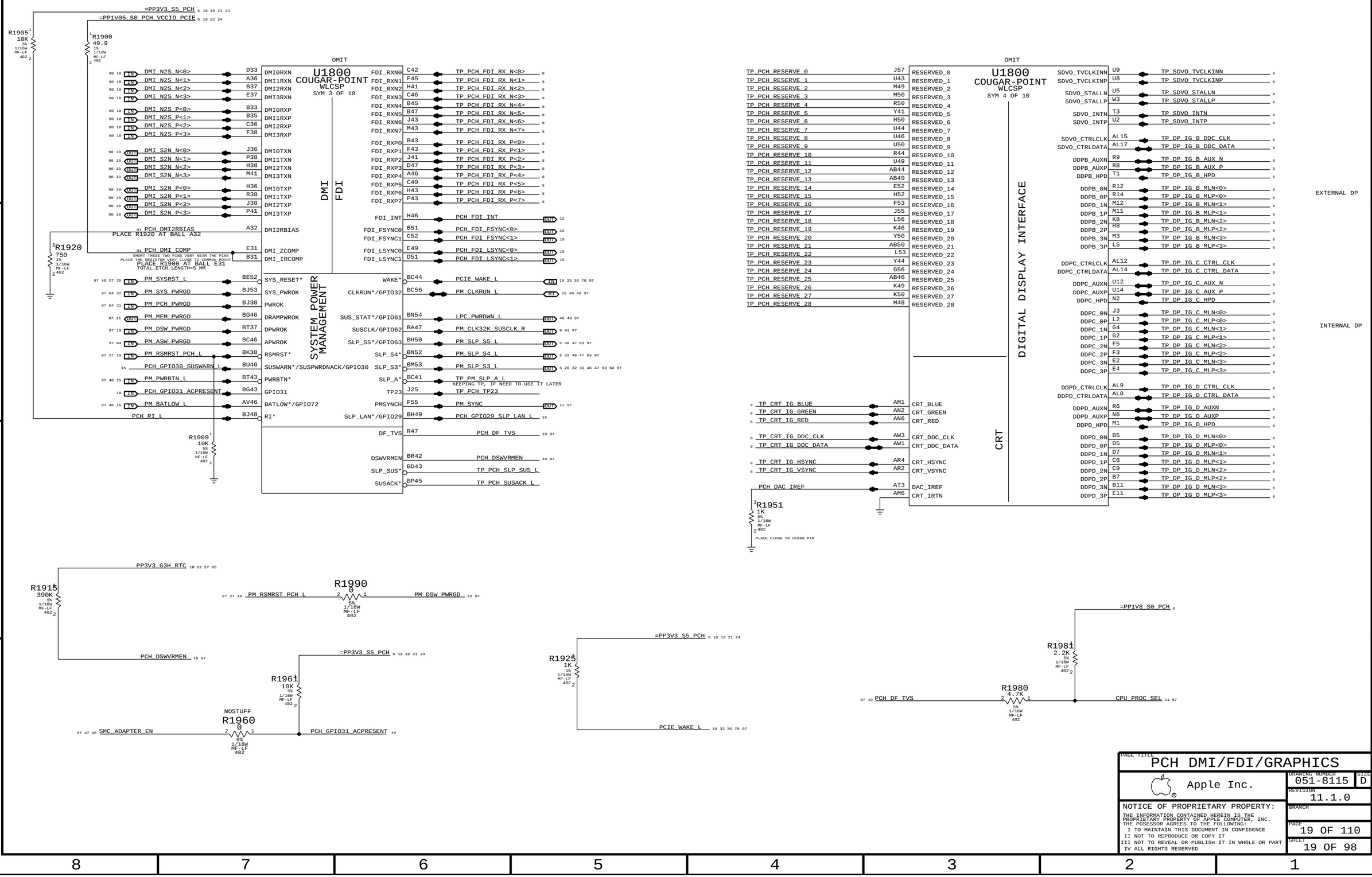

PAGE TITLE
PCH DMI/FDI/GRAPHICS

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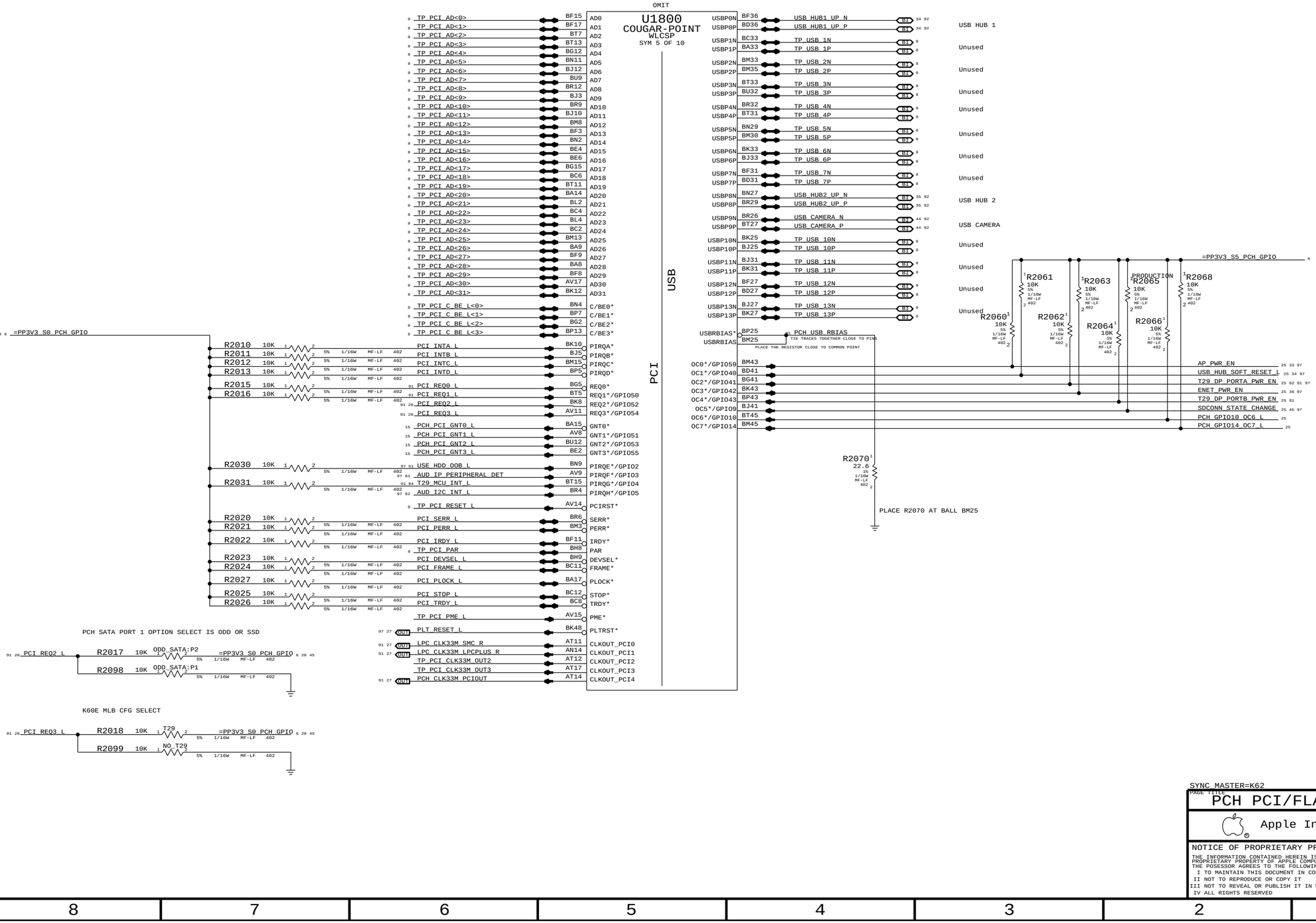

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PAGE TITLE
PCH PCI/FLASHCACHE/USB

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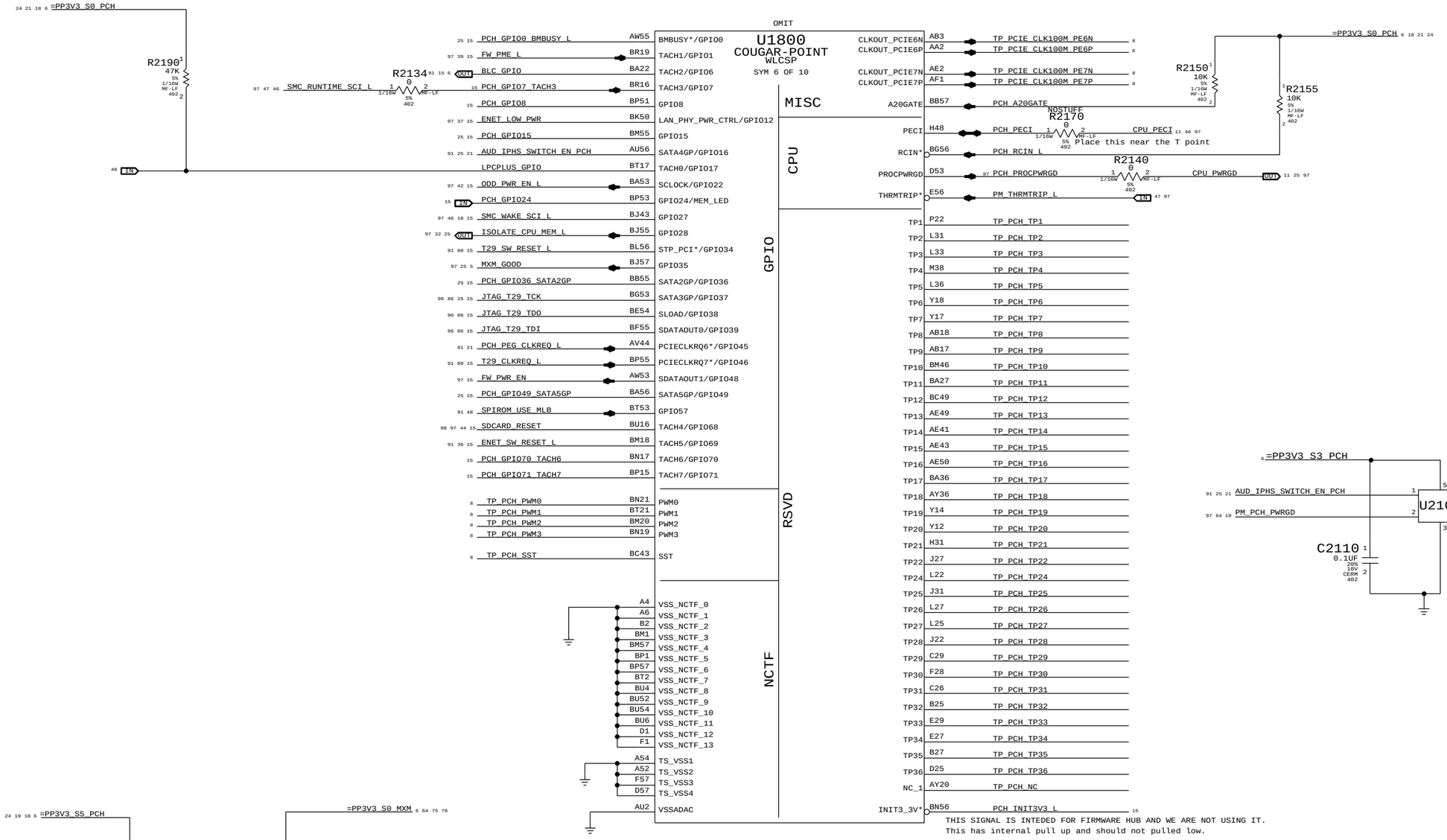

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PAGE TITLE: PCH MISC

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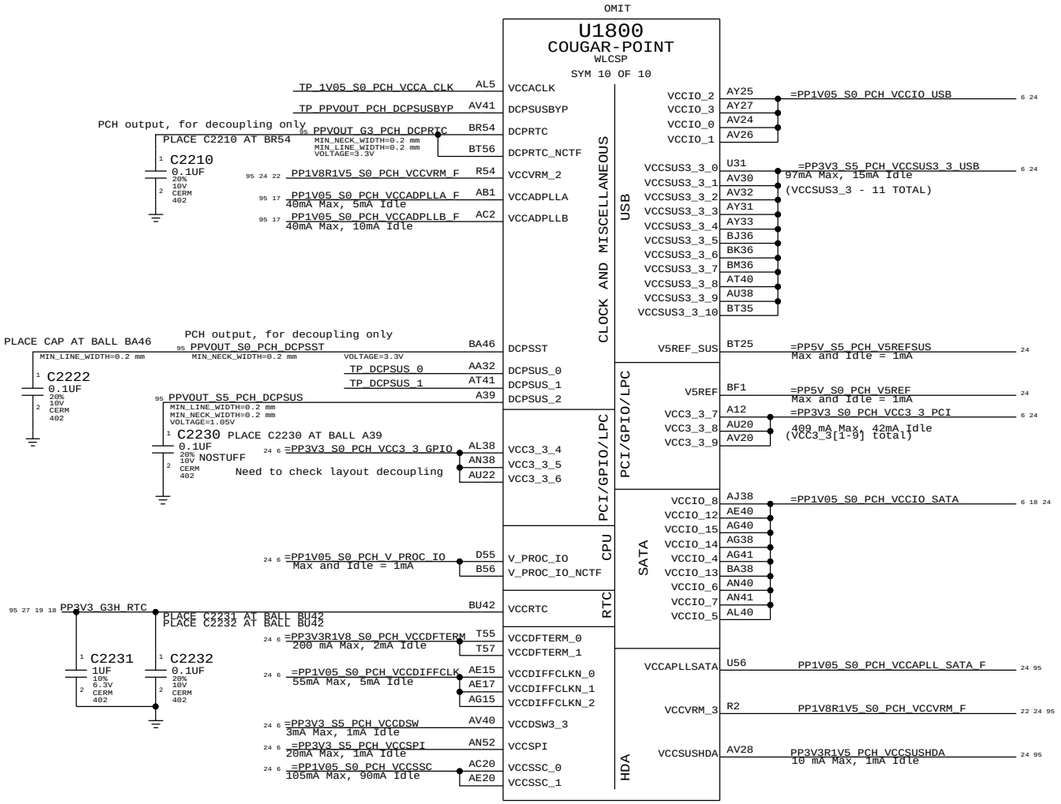

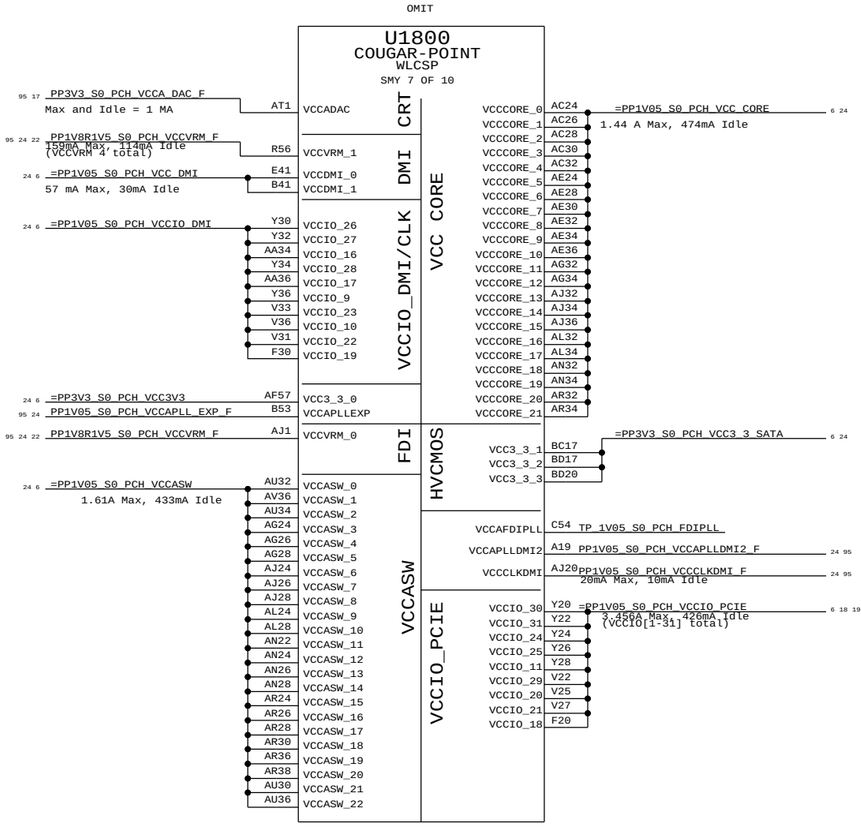

PAGE TITLE

PCH POWER

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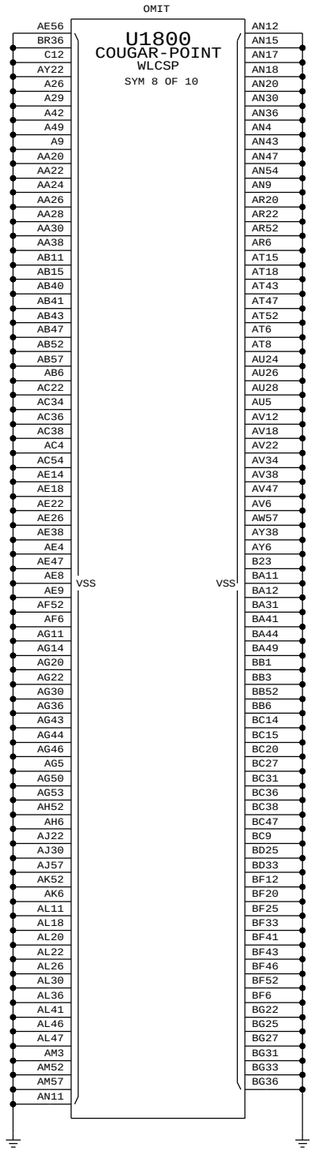

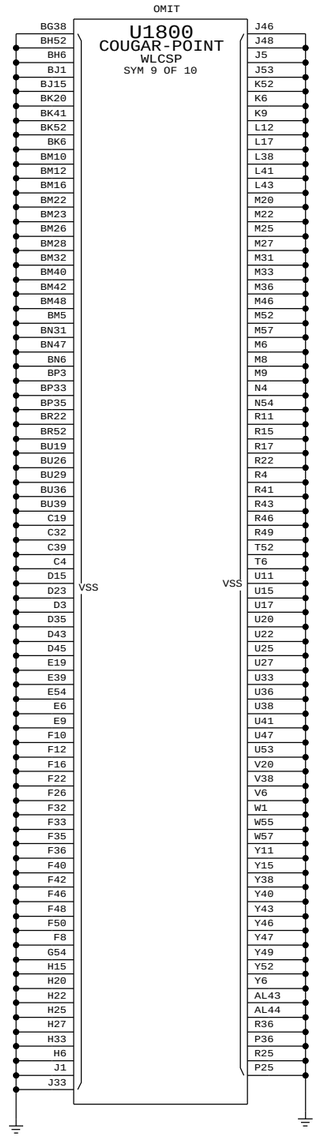

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PCH GROUNDS

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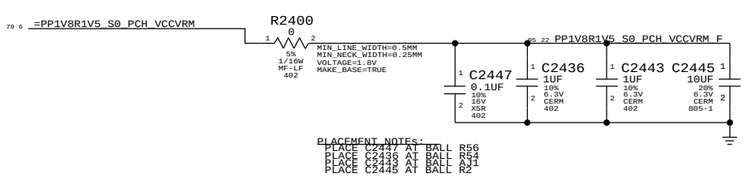

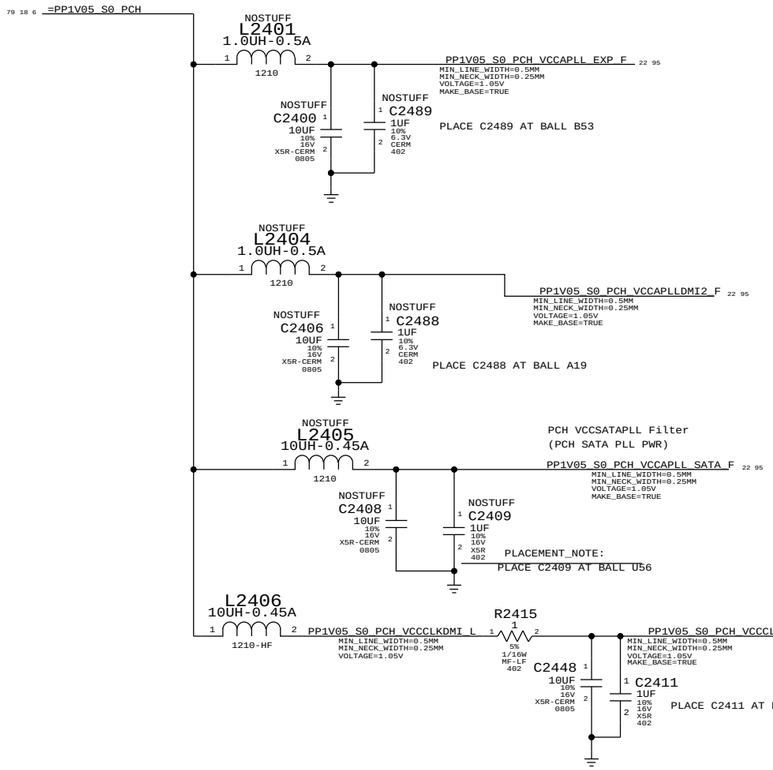

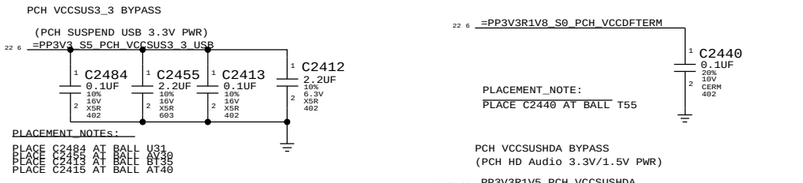

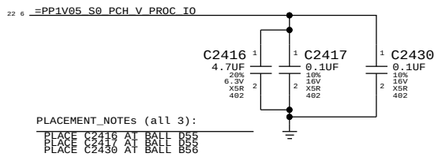

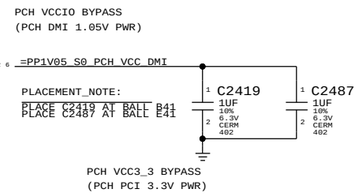

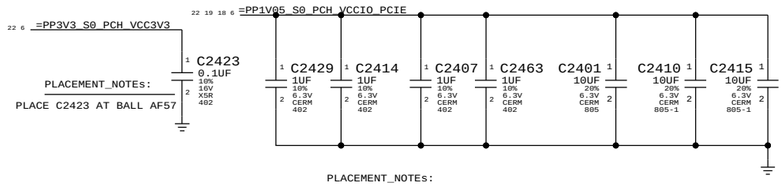

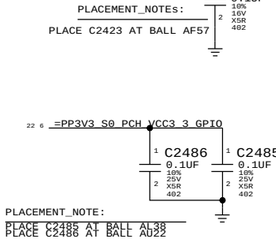

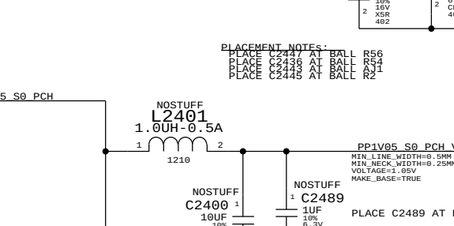

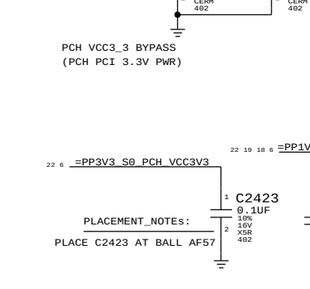

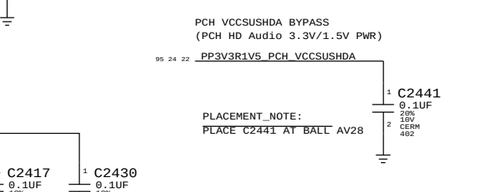

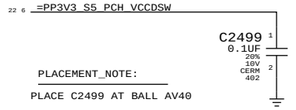

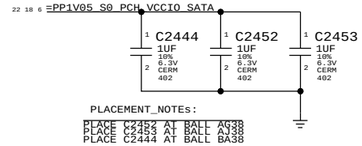

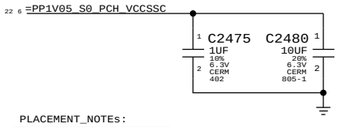

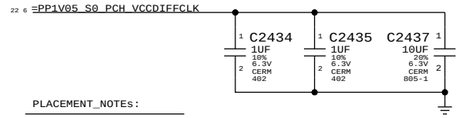

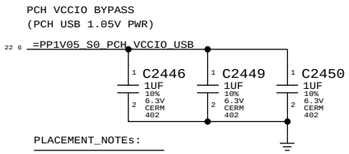

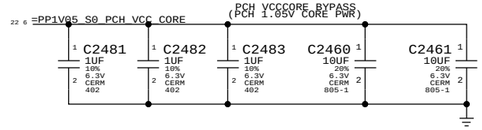

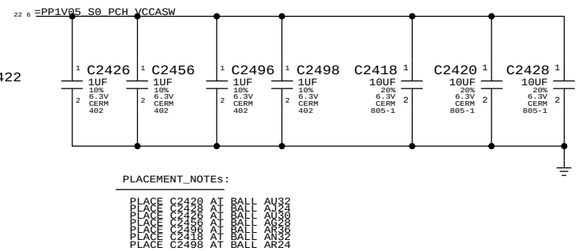

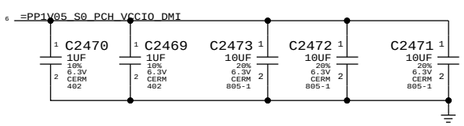

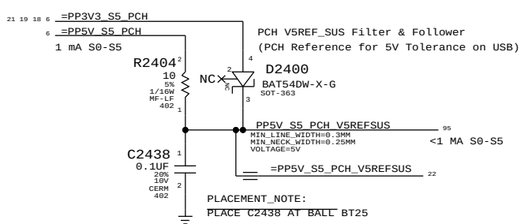

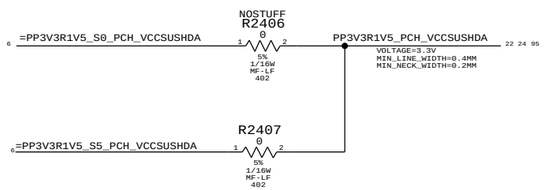

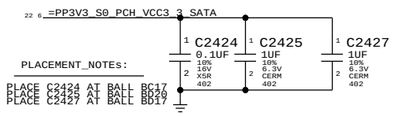

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PROCESSOR MINI XDP

PLACEMENT_NOTE=Place R2501 close to R2500 to minimize stubs

XDP_CPU_BPM
RP2500
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_BPM_L<6>
XDP_BPM_L<7>

XDP_CPU_CFG
RP2501
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>

PLACEMENT_NOTE=Place close to CPU
XDP R2500 1K MF-LF 402 1/16W
CPU_PWRGD

PLACEMENT_NOTE=Place close to SMC
XDP R2502 0 MF-LF 402 1/16W
PM_PWRBTN_L

PLACEMENT_NOTE=Place close to CPU
XDP R2501 1K MF-LF 402 1/16W
CPU_CFG<0>

XDP R2504 0 MF-LF 402 1/16W
PM_PGOOD_PVCORE_CPU

=PPVCCIO_S0_XDP

CRITICAL
XDP_CONN
J2500
DF40C-60DS-0.4V
F-ST-SM-HF
518S0774

XDP_CPU_PREQ_L
XDP_CPU_PRDY_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
CPU_CFG<10>
CPU_CFG<11>
XDP_OBSDATA_B<0>
XDP_OBSDATA_B<1>
XDP_OBSDATA_B<2>
XDP_OBSDATA_B<3>
XDP_CPU_PWRGD
XDP_CPU_PWRBTN_L
XDP_CPU_CFG<0>
XDP_VR_READY
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_CPU_TCK

OBSEN_A0 OBSEN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3 OBSEN_B0 OBSEN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3 PWRGD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 SDA SCL TCK1 TCK0

OBSEN_C0 OBSEN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3 OBSEN_D0 OBSEN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 TDO TRSTn TDI TMS XDP_PRESENT#

CPU_CFG<16> CPU_CFG<17> CPU_CFG<0> CPU_CFG<1> CPU_CFG<2> CPU_CFG<3> CPU_CFG<8> CPU_CFG<9> CPU_CFG<4> CPU_CFG<5> CPU_CFG<6> CPU_CFG<7> XDP_CPU_CLK100M_P XDP_CPU_CLK100M_N XDPCPU_PLTRST_L XDP_DBRESET_L XDP_CPU_TDO XDP_CPU_TRST_L XDP_CPU_TDI XDP_CPU_TMS

XDP C2500 0.1uF 10% 16V X5R 402
XDP C2501 0.1uF 10% 16V X5R 402

XDP R2515 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to R1841 ITPXDP_CLK100M_P
XDP R2516 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to R1840 ITPXDP_CLK100M_N

<- 1K SERIES R ON PCH SUPPORT P. 28

DESIGN NOTE:
ODT AVAILABLE ON JTAG

=PPVCCIO_S0_XDP
PLACEMENT NOTE:
PLACE TDO TERM NEAR SNB XDP CONN
XDP R2510 51 1/16W MF-LF 402 5%
XDP R2511 51 1/16W MF-LF 402 5%
XDP R2512 51 1/16W MF-LF 402 5%
PLACEMENT_NOTE=Place close to CPU
PLACEMENT_NOTE=Place close to J2500
XDP_CPU_TDO
XDP_CPU_TDI
XDP_CPU_TMS
XDP_CPU_TCK
XDP_CPU_TRST_L
XDP R2513 51 1/16W MF-LF 402 5%
XDP R2514 51 1/16W MF-LF 402 5%
PLACEMENT NOTE:
PLACE TCK/TDI/TMS/TRST* TERM NEAR CPU

PLACEMENT_NOTE=Place close to SW2800
XDP R2506 0 1/16W MF-LF 402 5%
XDP_DBRESET_L
To Reset Button
PM_SYSRST_L

PCH MINI XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J2550
DF40C-60DS-0.4V
F-ST-SM-HF
518S0774

XDP_PCH_OBSFN_A<0>
XDP_PCH_OBSFN_A<1>
XDP_PCH_AP_PWR_EN
XDP_PCH_USB_HUB_SOFT_RST_L
XDP_PCH_T29_DP_PORTA_PWR_EN
XDP_PCH_ENET_PWR_EN
XDP_PCH_OBSFN_B<0>
XDP_PCH_OBSFN_B<1>
XDP_PCH_T29_DP_PORTB_PWR_EN
XDP_PCH_SDCONN_CHANGE
PCH_GPIO10_OC6_L
PCH_GPIO14_OC7_L
XDP_PCH_S5_PWRGD
XDP_PCH_PWRBTN_L
XDP_XDPPCH_HOOK2
XDP_XDPPCH_HOOK3
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_PCH_TCK

OBSEN_A0 OBSEN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3 OBSEN_B0 OBSEN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3 PWRGD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 SDA SCL TCK1 TCK0

OBSEN_C0 OBSEN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3 OBSEN_D0 OBSEN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 TDO TRSTn TDI TMS XDP_PRESENT#

XDP_PCH_GPIO15 XDP_PCH_ISOLATE_CPU_MEM_L XDP_PCH_MXM_GOOD XDP_PCH_DP_AUXCH_ISOL PCH_GPIO19_SATA1GP TP_XDP_PCH_OBSFN_D<0> TP_XDP_PCH_OBSFN_D<1> PCH_GPIO36_SATA2GP XDP_PCH_JTAG_T29_TCK XDP_PCH_AUD_IPHS_SWITCH_EN PCH_GPIO49_SATA5GP TP_XDP_PCH_HOOK4 TP_XDP_PCH_HOOK5 XDPPCH_PLTRST_L XDP_DBRESET_L XDP_PCH_TDO TP_XDP_PCH_TRST_L XDP_PCH_TDI XDP_PCH_TMS

XDP C2580 0.1uF 10% 16V X5R 402
XDP C2581 0.1uF 10% 16V X5R 402

XDP R2578 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to PCH GPIO15 PCH_GPIO15
XDP R2576 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to PCH MGPIO7/GPIO28 ISOLATE_CPU_MEM_L
XDP R2577 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to PCH GPIO35 MXM_GOOD
XDP R2575 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to PCH SATA0GP/GPIO21 DP_AUXCH_ISOL
XDP R2573 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to PCH SATA3GP/GPIO37 JTAG_T29_TCK
XDP R2579 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to PCH SATA4GP/GPIO16 AUD_IPHS_SWITCH_EN_PCH

<- 1K SERIES R ON PCH SUPPORT P. 28

XDP R2582 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to PCH OC0#/GPIO59 AP_PWR_EN
XDP R2580 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to PCH OC1#/GPIO40 USB_HUB_SOFT_RESET_L
XDP R2583 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to PCH OC2#/GPIO41 T29_DP_PORTA_PWR_EN
XDP R2587 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to PCH OC3#/GPIO42 ENET_PWR_EN
XDP R2586 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to PCH OC4#/GPIO43 T29_DP_PORTB_PWR_EN
XDP R2581 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to PCH OC5#/GPIO9 SDCONN_STATE_CHANGE
XDP R2584 1K MF-LF 402 1/16W PLACEMENT_NOTE=Place close to J2550 =PP3V3_S5_XDP
XDP R2585 0 MF-LF 402 1/16W PLACEMENT_NOTE=Place close to SMC PM_PWRBTN_L

PLACEMENT NOTE:
PLACE TDO TERM NEAR PCH XDP CONN
XDP R2550 200 1/16W MF-LF 402 5%
XDP R2551 200 1/16W MF-LF 402 5%
XDP R2552 200 1/16W MF-LF 402 5%
PLACEMENT_NOTE=Place close to PCH
PLACEMENT_NOTE=Place close to J2550
XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS
XDP_PCH_TCK
XDP R2553 100 1/16W MF-LF 402 5%
XDP R2554 100 1/16W MF-LF 402 5%
XDP R2555 100 1/16W MF-LF 402 5%
XDP R2556 51 1/16W MF-LF 402 5%
This is to derive 1.05V SUS RAIL
PLACEMENT NOTE:
PLACE TCK/TDI/TMS/TRST* TERM NEAR PCH

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: CPU & PCH XDP

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DRAWING NUMBER: 051-8115 SIZE: D
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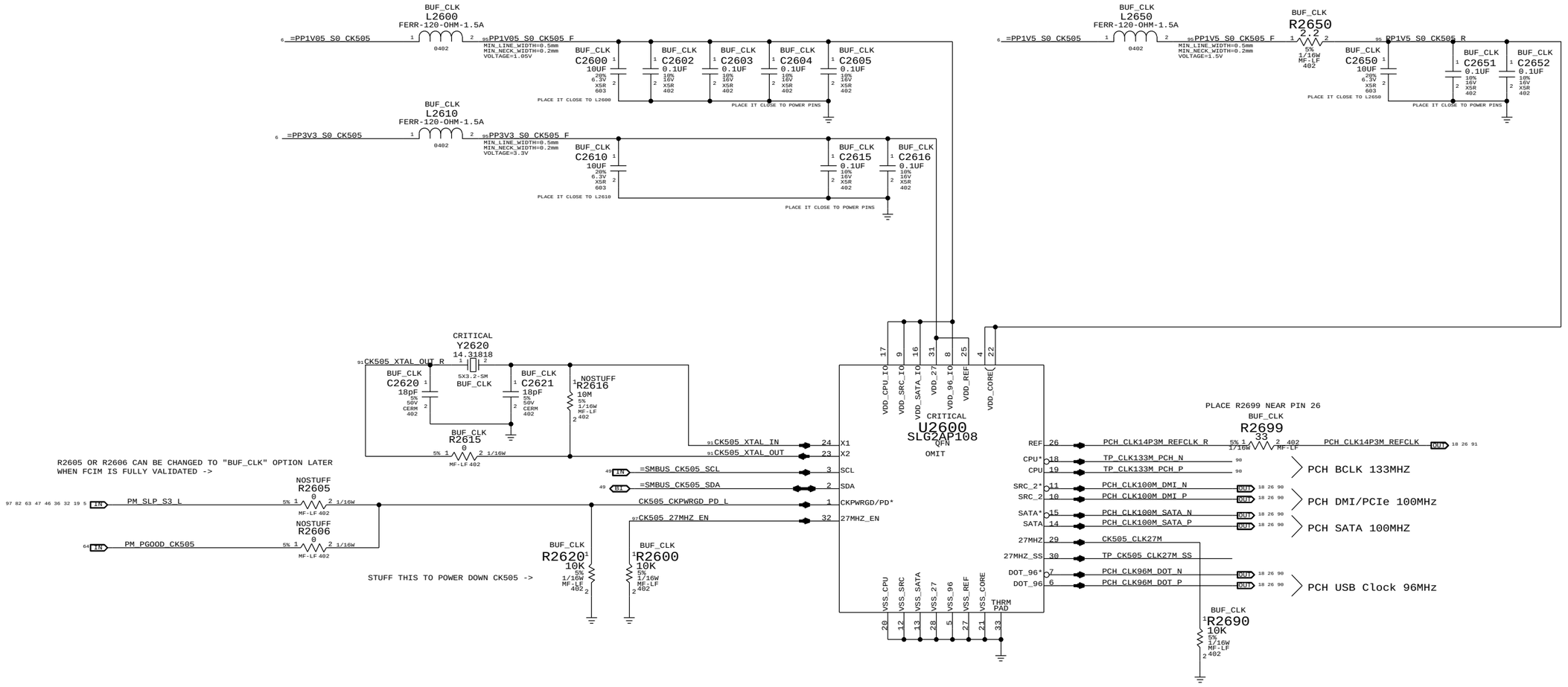
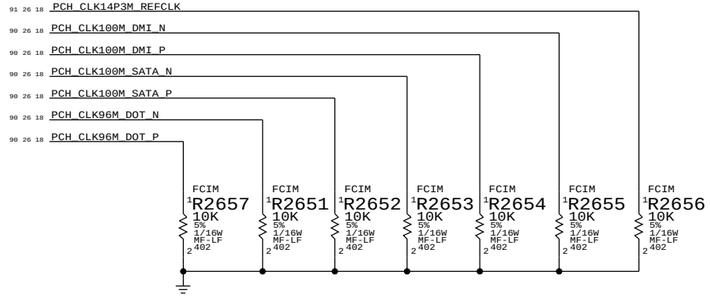


UNUSED clock terminations for FCIM MODE



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: CLOCK (CK505)

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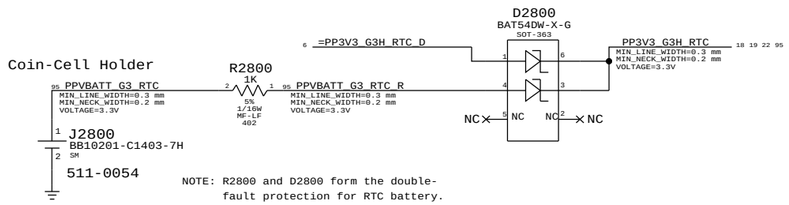
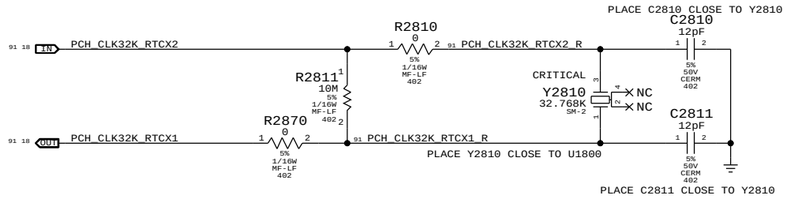
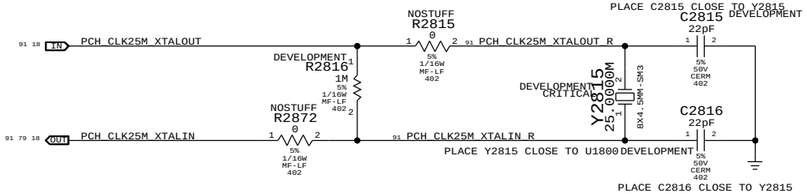
RTC Power Sources

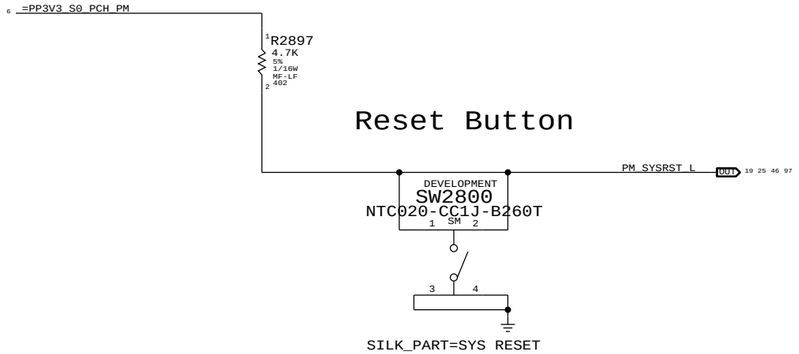


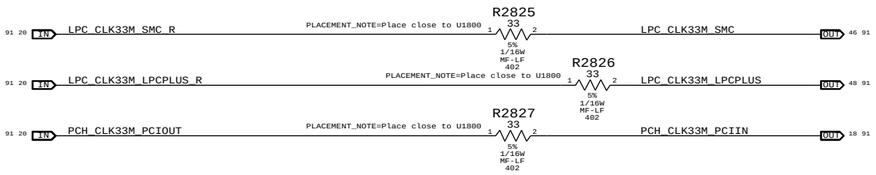
PCH RTC Crystal



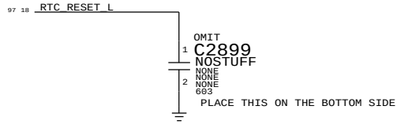
PCH 25MHZ CRYSTAL



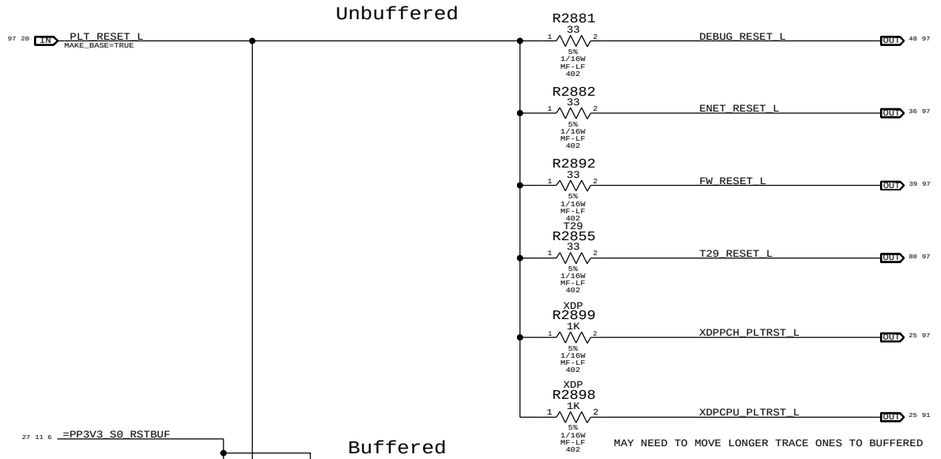




Platform Reset Connections



Unbuffered



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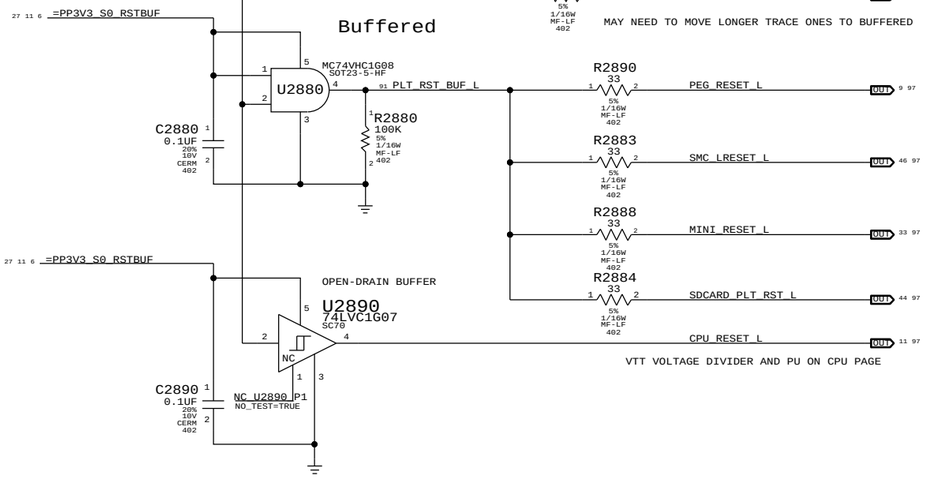

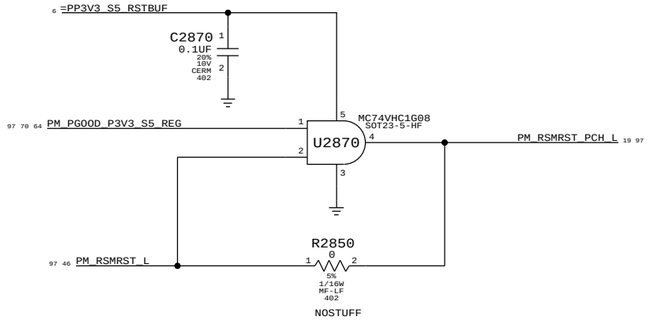

SMC PROVIDES RSMRST_L DE-ASSERTION DELAY UPON ENTRY TO S5
SMC PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON EXPECTED EXIT FROM S5
SMC MAY FORCE A RSMRST_L ASSERTION WITHOUT AN S5 POWER TRANSITION IN SOME ERROR CASES
PGOOD PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON AN UN-EXPECTED EXIT FROM S5 (POWER LOSS)

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: CHIPSET SUPPORT

Apple Inc.

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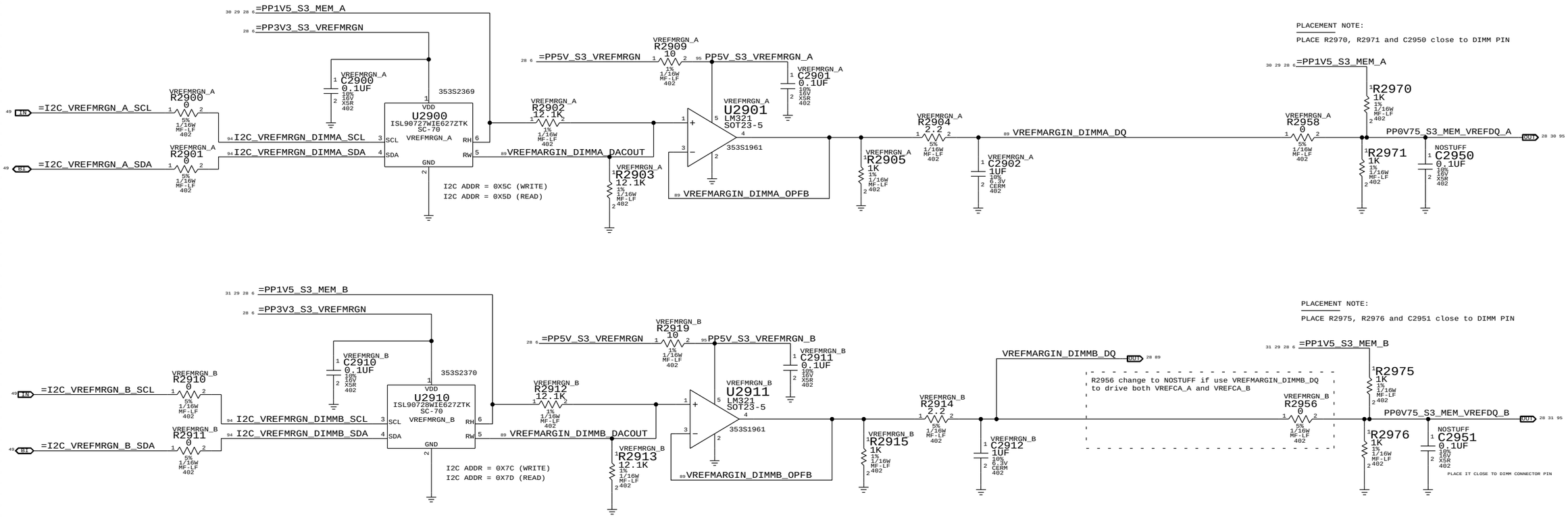
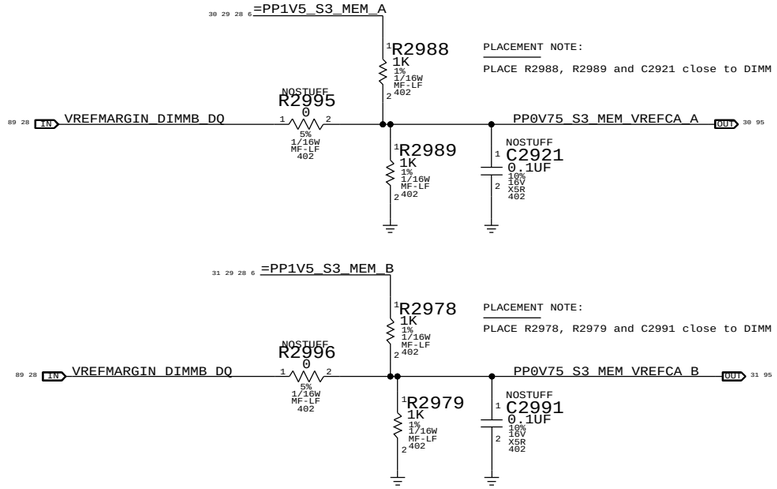
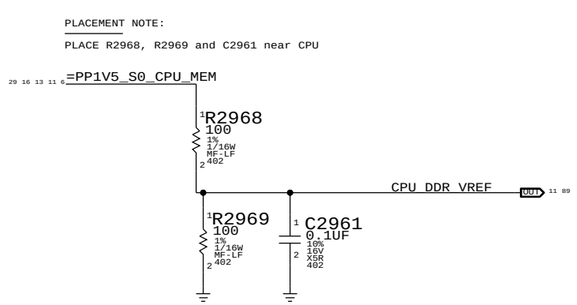
DIMM VREFDQ



DIMM VREFCA



CPU VREF



SYNC_MASTER=K62 SYNC_DATE=01/06/2013

PAGE TITLE: DDR3 VREF MARGINING

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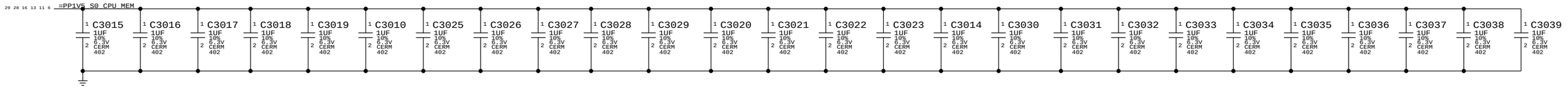
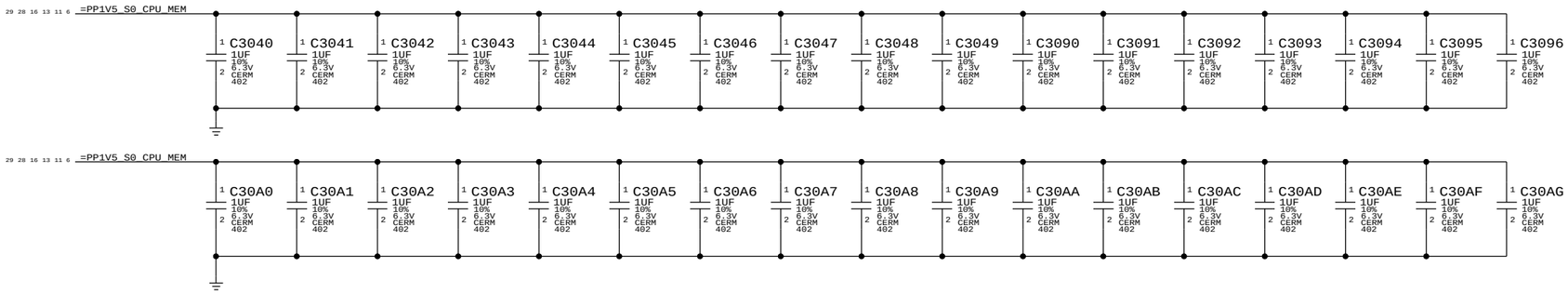
DIMM A (CLOSER TO CPU)

CAPS TO STITCH 1V5_CPU_MEM TO GND NEAR DIMM

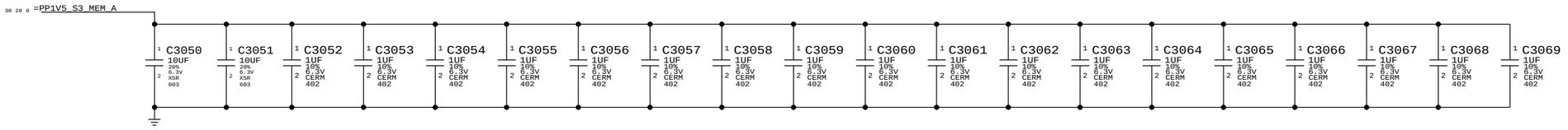
DIMM B (FURTHER FROM CPU)



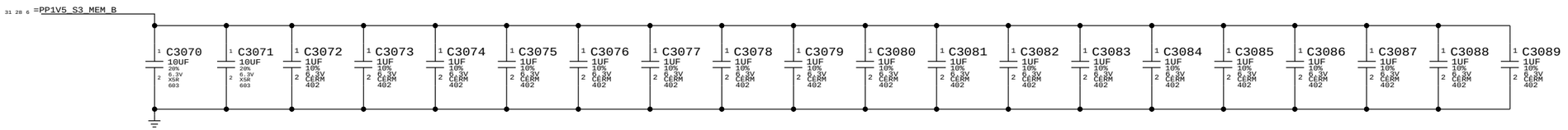
EXTRA DECOUPLING CAPS FOR 1V5_CPU_MEM RAIL



DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL A DIMM CONNECTOR



DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL B DIMM CONNECTOR



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PAGE TITLE

MEMORY CAPS

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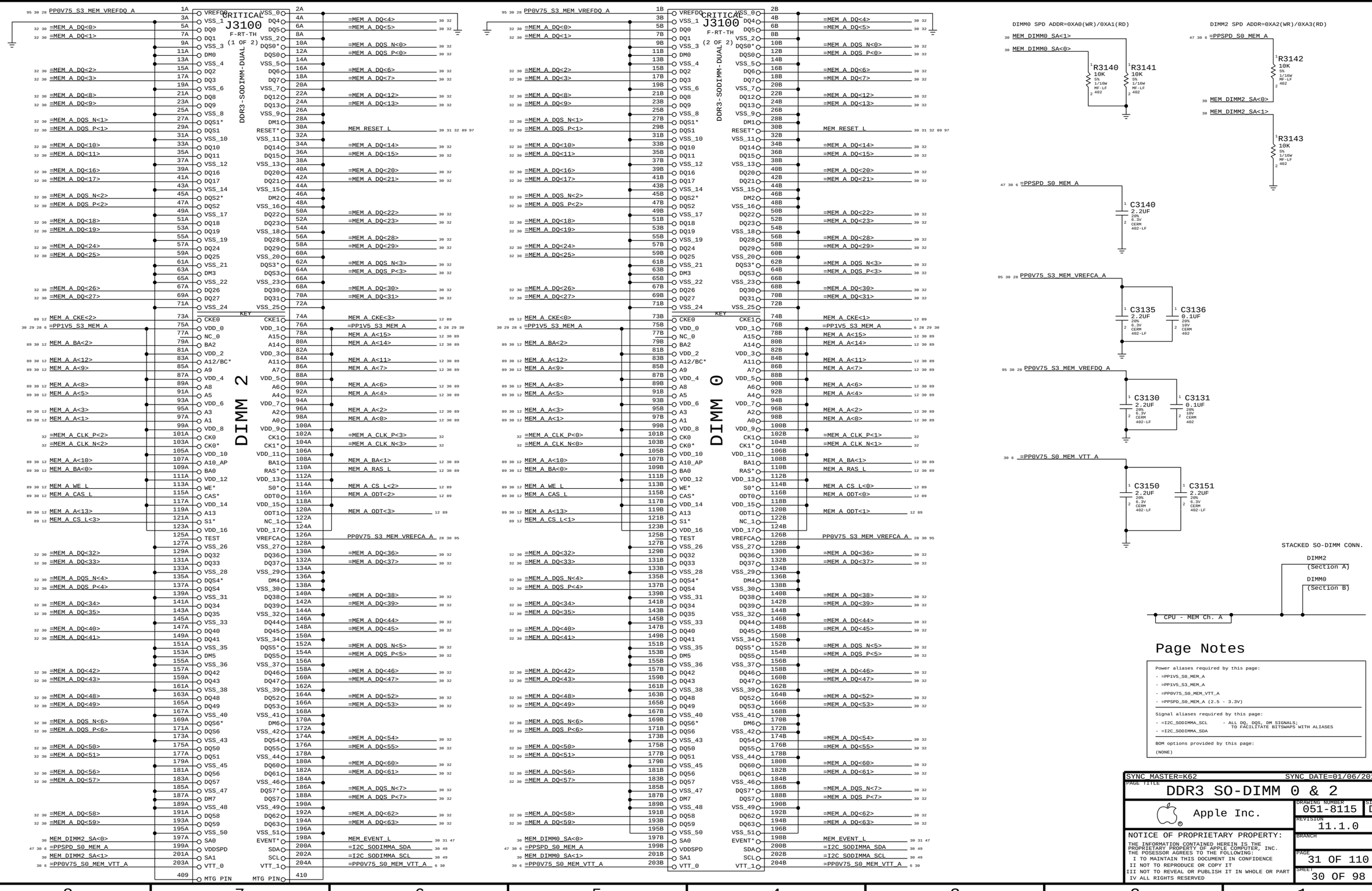

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

- ALL DQ, DQS, DM SIGNALS: TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: DDR3 SO-DIMM 0 & 2

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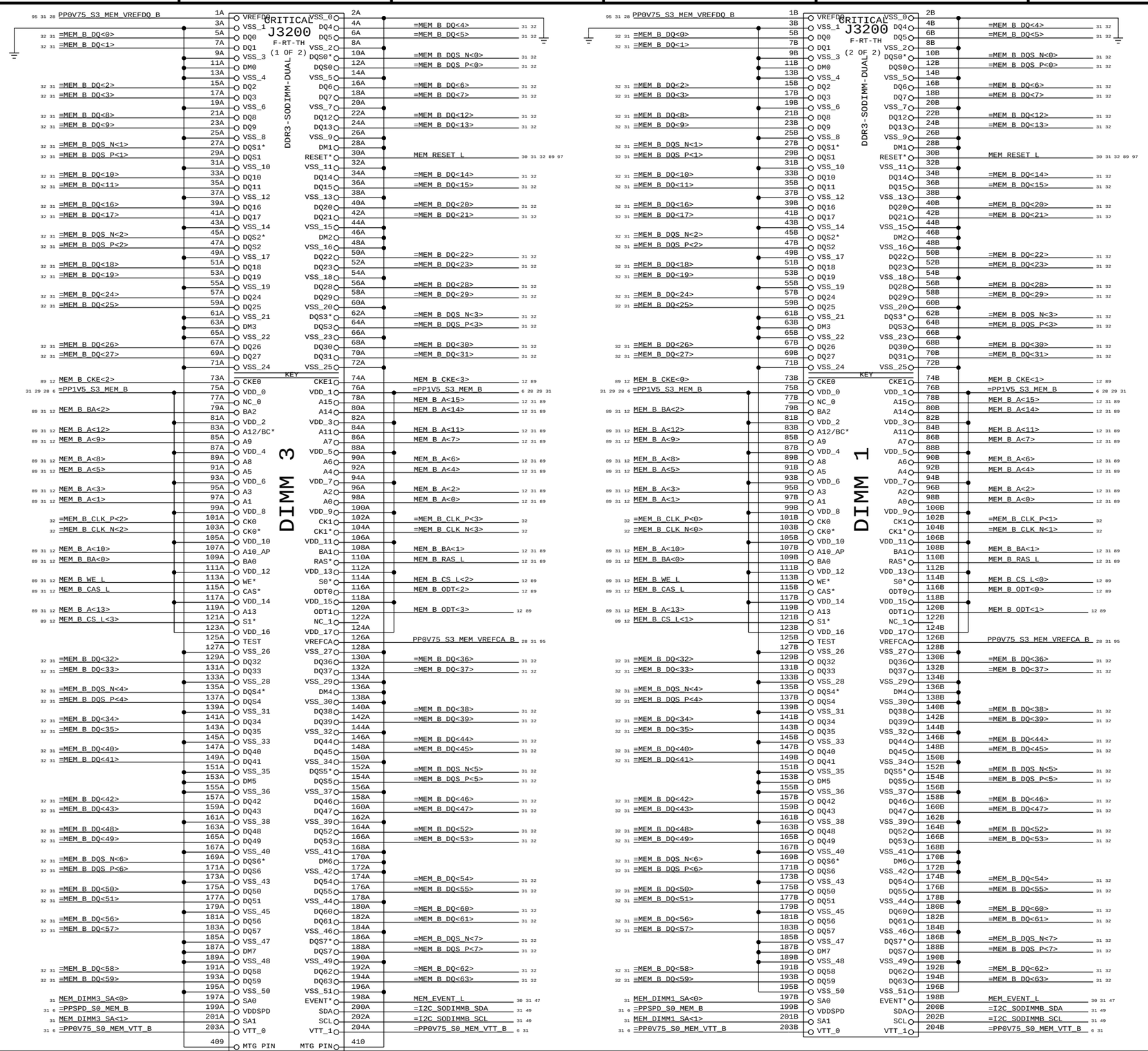

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: DDR3 SO-DIMM 1 & 3

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CPU CHANNEL A DQS 0 -> DIMM A DQS 7

MEM_A_DQS_N<0>			=MEM_A_DQS_N<7>	
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<7>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_A_DQ<7>			=MEM_A_DQ<57>	
MEM_A_DQ<6>	MAKE_BASE=TRUE		=MEM_A_DQ<56>	
MEM_A_DQ<5>	MAKE_BASE=TRUE		=MEM_A_DQ<58>	
MEM_A_DQ<4>	MAKE_BASE=TRUE		=MEM_A_DQ<59>	
MEM_A_DQ<3>	MAKE_BASE=TRUE		=MEM_A_DQ<60>	
MEM_A_DQ<2>	MAKE_BASE=TRUE		=MEM_A_DQ<61>	
MEM_A_DQ<1>	MAKE_BASE=TRUE		=MEM_A_DQ<62>	
MEM_A_DQ<0>	MAKE_BASE=TRUE		=MEM_A_DQ<63>	

CPU CHANNEL A DQS 1 -> DIMM A DQS 6

MEM_A_DQS_N<1>			=MEM_A_DQS_N<6>	
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<6>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_A_DQ<15>			=MEM_A_DQ<49>	
MEM_A_DQ<14>	MAKE_BASE=TRUE		=MEM_A_DQ<52>	
MEM_A_DQ<13>	MAKE_BASE=TRUE		=MEM_A_DQ<51>	
MEM_A_DQ<12>	MAKE_BASE=TRUE		=MEM_A_DQ<50>	
MEM_A_DQ<11>	MAKE_BASE=TRUE		=MEM_A_DQ<48>	
MEM_A_DQ<10>	MAKE_BASE=TRUE		=MEM_A_DQ<53>	
MEM_A_DQ<9>	MAKE_BASE=TRUE		=MEM_A_DQ<55>	
MEM_A_DQ<8>	MAKE_BASE=TRUE		=MEM_A_DQ<54>	

CPU CHANNEL A DQS 2 -> DIMM A DQS 5

MEM_A_DQS_N<2>			=MEM_A_DQS_N<5>	
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<5>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_A_DQ<23>			=MEM_A_DQ<40>	
MEM_A_DQ<22>	MAKE_BASE=TRUE		=MEM_A_DQ<45>	
MEM_A_DQ<21>	MAKE_BASE=TRUE		=MEM_A_DQ<46>	
MEM_A_DQ<20>	MAKE_BASE=TRUE		=MEM_A_DQ<47>	
MEM_A_DQ<19>	MAKE_BASE=TRUE		=MEM_A_DQ<41>	
MEM_A_DQ<18>	MAKE_BASE=TRUE		=MEM_A_DQ<44>	
MEM_A_DQ<17>	MAKE_BASE=TRUE		=MEM_A_DQ<43>	
MEM_A_DQ<16>	MAKE_BASE=TRUE		=MEM_A_DQ<42>	

CPU CHANNEL A DQS 3 -> DIMM A DQS 4

MEM_A_DQS_N<3>			=MEM_A_DQS_N<4>	
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<4>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_A_DQ<31>			=MEM_A_DQ<37>	
MEM_A_DQ<30>	MAKE_BASE=TRUE		=MEM_A_DQ<33>	
MEM_A_DQ<29>	MAKE_BASE=TRUE		=MEM_A_DQ<35>	
MEM_A_DQ<28>	MAKE_BASE=TRUE		=MEM_A_DQ<34>	
MEM_A_DQ<27>	MAKE_BASE=TRUE		=MEM_A_DQ<36>	
MEM_A_DQ<26>	MAKE_BASE=TRUE		=MEM_A_DQ<32>	
MEM_A_DQ<25>	MAKE_BASE=TRUE		=MEM_A_DQ<38>	
MEM_A_DQ<24>	MAKE_BASE=TRUE		=MEM_A_DQ<39>	

CPU CHANNEL A DQS 4 -> DIMM A DQS 3

MEM_A_DQS_N<4>			=MEM_A_DQS_N<3>	
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<3>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_A_DQ<39>			=MEM_A_DQ<28>	
MEM_A_DQ<38>	MAKE_BASE=TRUE		=MEM_A_DQ<29>	
MEM_A_DQ<37>	MAKE_BASE=TRUE		=MEM_A_DQ<27>	
MEM_A_DQ<36>	MAKE_BASE=TRUE		=MEM_A_DQ<31>	
MEM_A_DQ<35>	MAKE_BASE=TRUE		=MEM_A_DQ<25>	
MEM_A_DQ<34>	MAKE_BASE=TRUE		=MEM_A_DQ<24>	
MEM_A_DQ<33>	MAKE_BASE=TRUE		=MEM_A_DQ<26>	
MEM_A_DQ<32>	MAKE_BASE=TRUE		=MEM_A_DQ<30>	

CPU CHANNEL A DQS 5 -> DIMM A DQS 2

MEM_A_DQS_N<5>			=MEM_A_DQS_N<2>	
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<2>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_A_DQ<47>			=MEM_A_DQ<17>	
MEM_A_DQ<46>	MAKE_BASE=TRUE		=MEM_A_DQ<16>	
MEM_A_DQ<45>	MAKE_BASE=TRUE		=MEM_A_DQ<22>	
MEM_A_DQ<44>	MAKE_BASE=TRUE		=MEM_A_DQ<23>	
MEM_A_DQ<43>	MAKE_BASE=TRUE		=MEM_A_DQ<21>	
MEM_A_DQ<42>	MAKE_BASE=TRUE		=MEM_A_DQ<20>	
MEM_A_DQ<41>	MAKE_BASE=TRUE		=MEM_A_DQ<18>	
MEM_A_DQ<40>	MAKE_BASE=TRUE		=MEM_A_DQ<19>	

CPU CHANNEL A DQS 6 -> DIMM A DQS 1

MEM_A_DQS_N<6>			=MEM_A_DQS_N<1>	
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<1>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_A_DQ<55>			=MEM_A_DQ<12>	
MEM_A_DQ<54>	MAKE_BASE=TRUE		=MEM_A_DQ<13>	
MEM_A_DQ<53>	MAKE_BASE=TRUE		=MEM_A_DQ<10>	
MEM_A_DQ<52>	MAKE_BASE=TRUE		=MEM_A_DQ<15>	
MEM_A_DQ<51>	MAKE_BASE=TRUE		=MEM_A_DQ<8>	
MEM_A_DQ<50>	MAKE_BASE=TRUE		=MEM_A_DQ<9>	
MEM_A_DQ<49>	MAKE_BASE=TRUE		=MEM_A_DQ<11>	
MEM_A_DQ<48>	MAKE_BASE=TRUE		=MEM_A_DQ<14>	

CPU CHANNEL A DQS 7 -> DIMM A DQS 0

MEM_A_DQS_N<7>			=MEM_A_DQS_N<0>	
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<0>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_A_DQ<63>			=MEM_A_DQ<5>	
MEM_A_DQ<62>	MAKE_BASE=TRUE		=MEM_A_DQ<4>	
MEM_A_DQ<61>	MAKE_BASE=TRUE		=MEM_A_DQ<3>	
MEM_A_DQ<60>	MAKE_BASE=TRUE		=MEM_A_DQ<2>	
MEM_A_DQ<59>	MAKE_BASE=TRUE		=MEM_A_DQ<1>	
MEM_A_DQ<58>	MAKE_BASE=TRUE		=MEM_A_DQ<0>	
MEM_A_DQ<57>	MAKE_BASE=TRUE		=MEM_A_DQ<7>	
MEM_A_DQ<56>	MAKE_BASE=TRUE		=MEM_A_DQ<6>	

CPU CHANNEL B DQS 0 -> DIMM B DQS 7

MEM_B_DQS_N<0>			=MEM_B_DQS_N<7>	
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<7>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_B_DQ<7>			=MEM_B_DQ<61>	
MEM_B_DQ<6>	MAKE_BASE=TRUE		=MEM_B_DQ<60>	
MEM_B_DQ<5>	MAKE_BASE=TRUE		=MEM_B_DQ<62>	
MEM_B_DQ<4>	MAKE_BASE=TRUE		=MEM_B_DQ<63>	
MEM_B_DQ<3>	MAKE_BASE=TRUE		=MEM_B_DQ<56>	
MEM_B_DQ<2>	MAKE_BASE=TRUE		=MEM_B_DQ<57>	
MEM_B_DQ<1>	MAKE_BASE=TRUE		=MEM_B_DQ<58>	
MEM_B_DQ<0>	MAKE_BASE=TRUE		=MEM_B_DQ<59>	

CPU CHANNEL B DQS 1 -> DIMM B DQS 6

MEM_B_DQS_N<1>			=MEM_B_DQS_N<6>	
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<6>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_B_DQ<15>			=MEM_B_DQ<51>	
MEM_B_DQ<14>	MAKE_BASE=TRUE		=MEM_B_DQ<54>	
MEM_B_DQ<13>	MAKE_BASE=TRUE		=MEM_B_DQ<53>	
MEM_B_DQ<12>	MAKE_BASE=TRUE		=MEM_B_DQ<52>	
MEM_B_DQ<11>	MAKE_BASE=TRUE		=MEM_B_DQ<48>	
MEM_B_DQ<10>	MAKE_BASE=TRUE		=MEM_B_DQ<49>	
MEM_B_DQ<9>	MAKE_BASE=TRUE		=MEM_B_DQ<50>	
MEM_B_DQ<8>	MAKE_BASE=TRUE		=MEM_B_DQ<55>	

CPU CHANNEL B DQS 2 -> DIMM B DQS 5

MEM_B_DQS_N<2>			=MEM_B_DQS_N<5>	
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<5>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_B_DQ<23>			=MEM_B_DQ<45>	
MEM_B_DQ<22>	MAKE_BASE=TRUE		=MEM_B_DQ<40>	
MEM_B_DQ<21>	MAKE_BASE=TRUE		=MEM_B_DQ<42>	
MEM_B_DQ<20>	MAKE_BASE=TRUE		=MEM_B_DQ<47>	
MEM_B_DQ<19>	MAKE_BASE=TRUE		=MEM_B_DQ<44>	
MEM_B_DQ<18>	MAKE_BASE=TRUE		=MEM_B_DQ<41>	
MEM_B_DQ<17>	MAKE_BASE=TRUE		=MEM_B_DQ<46>	
MEM_B_DQ<16>	MAKE_BASE=TRUE		=MEM_B_DQ<43>	

CPU CHANNEL B DQS 3 -> DIMM B DQS 4

MEM_B_DQS_N<3>			=MEM_B_DQS_N<4>	
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<4>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_B_DQ<31>			=MEM_B_DQ<32>	
MEM_B_DQ<30>	MAKE_BASE=TRUE		=MEM_B_DQ<39>	
MEM_B_DQ<29>	MAKE_BASE=TRUE		=MEM_B_DQ<37>	
MEM_B_DQ<28>	MAKE_BASE=TRUE		=MEM_B_DQ<38>	
MEM_B_DQ<27>	MAKE_BASE=TRUE		=MEM_B_DQ<35>	
MEM_B_DQ<26>	MAKE_BASE=TRUE		=MEM_B_DQ<34>	
MEM_B_DQ<25>	MAKE_BASE=TRUE		=MEM_B_DQ<36>	
MEM_B_DQ<24>	MAKE_BASE=TRUE		=MEM_B_DQ<33>	

CPU CHANNEL B DQS 4 -> DIMM B DQS 3

MEM_B_DQS_N<4>			=MEM_B_DQS_N<3>	
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<3>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_B_DQ<39>			=MEM_B_DQ<28>	
MEM_B_DQ<38>	MAKE_BASE=TRUE		=MEM_B_DQ<24>	
MEM_B_DQ<37>	MAKE_BASE=TRUE		=MEM_B_DQ<31>	
MEM_B_DQ<36>	MAKE_BASE=TRUE		=MEM_B_DQ<30>	
MEM_B_DQ<35>	MAKE_BASE=TRUE		=MEM_B_DQ<29>	
MEM_B_DQ<34>	MAKE_BASE=TRUE		=MEM_B_DQ<25>	
MEM_B_DQ<33>	MAKE_BASE=TRUE		=MEM_B_DQ<27>	
MEM_B_DQ<32>	MAKE_BASE=TRUE		=MEM_B_DQ<26>	

CPU CHANNEL B DQS 5 -> DIMM B DQS 2

MEM_B_DQS_N<5>			=MEM_B_DQS_N<2>	
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<2>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_B_DQ<47>			=MEM_B_DQ<18>	
MEM_B_DQ<46>	MAKE_BASE=TRUE		=MEM_B_DQ<20>	
MEM_B_DQ<45>	MAKE_BASE=TRUE		=MEM_B_DQ<23>	
MEM_B_DQ<44>	MAKE_BASE=TRUE		=MEM_B_DQ<22>	
MEM_B_DQ<43>	MAKE_BASE=TRUE		=MEM_B_DQ<19>	
MEM_B_DQ<42>	MAKE_BASE=TRUE		=MEM_B_DQ<21>	
MEM_B_DQ<41>	MAKE_BASE=TRUE		=MEM_B_DQ<17>	
MEM_B_DQ<40>	MAKE_BASE=TRUE		=MEM_B_DQ<16>	

CPU CHANNEL B DQS 6 -> DIMM B DQS 1

MEM_B_DQS_N<6>			=MEM_B_DQS_N<1>	
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<1>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_B_DQ<55>			=MEM_B_DQ<8>	
MEM_B_DQ<54>	MAKE_BASE=TRUE		=MEM_B_DQ<14>	
MEM_B_DQ<53>	MAKE_BASE=TRUE		=MEM_B_DQ<10>	
MEM_B_DQ<52>	MAKE_BASE=TRUE		=MEM_B_DQ<11>	
MEM_B_DQ<51>	MAKE_BASE=TRUE		=MEM_B_DQ<9>	
MEM_B_DQ<50>	MAKE_BASE=TRUE		=MEM_B_DQ<15>	
MEM_B_DQ<49>	MAKE_BASE=TRUE		=MEM_B_DQ<12>	
MEM_B_DQ<48>	MAKE_BASE=TRUE		=MEM_B_DQ<13>	

CPU CHANNEL B DQS 7 -> DIMM B DQS 0

MEM_B_DQS_N<7>			=MEM_B_DQS_N<0>	
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<0>	
	MAKE_BASE=TRUE	NO_TEST=TRUE		
MEM_B_DQ<63>			=MEM_B_DQ<2>	
MEM_B_DQ<62>	MAKE_BASE=TRUE		=MEM_B_DQ<1>	
MEM_B_DQ<61>	MAKE_BASE=TRUE		=MEM_B_DQ<3>	
MEM_B_DQ<60>	MAKE_BASE=TRUE		=MEM_B_DQ<7>	
MEM_B_DQ<59>	MAKE_BASE=TRUE		=MEM_B_DQ<4>	
MEM_B_DQ<58>	MAKE_BASE=TRUE		=MEM_B_DQ<5>	
MEM_B_DQ<57>	MAKE_BASE=TRUE		=MEM_B_DQ<6>	
MEM_B_DQ<56>	MAKE_BASE=TRUE		=MEM_B_DQ<0>	

DDR3 RESET SUPPORT

SNB? CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0

S	R	CLK	D	Q	QB
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	POSEDGE	L	L	H
H	H	POSEDGE	H	H	L

MEMORY CLOCK ALIASING

MEM_A_CLK_P<0>			=MEM_A_CLK_P<0>
MEM_A_CLK_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_N<0>
MEM_A_CLK_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_P<1>
MEM_A_CLK_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_N<1>
MEM_A_CLK_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_P<2>
MEM_A_CLK_N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_N<2>
MEM_A_CLK_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_P<3>
MEM_A_CLK_N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_N<3>
MEM_B_CLK_P<0>			=MEM_B_CLK_P<0>
MEM_B_CLK_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_N<0>
MEM_B_CLK_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_P<1>
MEM_B_CLK_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_N<1>
MEM_B_CLK_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_P<2>
MEM_B_CLK_N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_N<2>
MEM_B_CLK_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_P<3>
MEM_B_CLK_N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_N<3>

SYNC_MASTER=K62			SYNC_DATE=01/06/2011
PAGE TITLE	DDR3 SUPPORT AND BITSWAPS		
Apple Inc.		DRAWING NUMBER	051-8115
		SIZE	D
		REVISION	11.1.0
		BRANCH	
		PAGE	33 OF 110
		SHEET	32 OF 98

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3.3V S3 CURRENT	D0 D2 D2HOT	D3COLD
MAX CONT.	1760MA	750MA
MAX PEAK	2750MA	2750MA
1.5V CURRENT		
MAX CONT.	N/U	N/U
MAX PEAK	N/U	N/U

NOTE: CURRENT DATA PER APR 5,2010 PCIE MINI CEM ECN

AP WAKE# ISOLATION

=PP3V3_S3_MINI_CONN 33

Q3470 SSM3K15FV SOD-VESM-HF

R3470 10K 5% 1/16W MF-LF 402

97 78 36 19 OUT PCIE WAKE L

NOSTUFF R3400 0 5% 1/16W MF-LF 402

NOSTUFF R3401 0 5% 1/16W MF-LF 402

CRITICAL J3400 AS0B226-S40N-7F F-RT-SM

AP_WAKE_L

RSVD MINI WLAN ACTIVE

RSVD MINI BT ACTIVE

33 OUT AP MINI CLKREQ L

90 18 IN PCIE CLK100M MINI N

90 18 IN PCIE CLK100M MINI P

RESERVED

RESERVED

90 18 OUT PCIE MINI D2R N

90 18 OUT PCIE MINI D2R P

PLACEMENT_NOTE=PLACE CLOSE TO U1800.

C3431 0.1uF 10% 16V X5R 402

90 18 IN PCIE MINI R2D C N

PLACEMENT_NOTE=PLACE CLOSE TO U1800.

C3430 0.1uF 10% 16V X5R 402

90 18 IN PCIE MINI R2D C P

90 PCIE MINI R2D N

90 PCIE MINI R2D P

AP MINI RESET L 33 IN 97

SMB MINI SCL

SMB MINI SDA

TP USB MININ

TP USB MINIP

NO AVAILALBLE USB ON THIS PLATFORM
TARGET CARDS DO NOT USE IT

NOSTUFF R3490 0 5% 1/16W MF-LF 402 =SMB MINI SCL 49

NOSTUFF R3491 0 5% 1/16W MF-LF 402 =SMB MINI SDA 49

=PP3V3_S3_MINI_CONN 33

C3410 0.1uF 20% 10V CERM 402

C3420 0.1uF 20% 10V CERM 402

C3421 10uF 20% 6.3V X5R 603

=PP1V5_S0_MINI 6

NOSTUFF C3400 0.1uF 20% 10V CERM 402

NOSTUFF C3401 10uF 20% 6.3V X5R 603

AP PWR EN ISOLATION

=PP3V3_S3_MINI 6 33

Q3471 SSM3K15FV SOD-VESM-HF AP

R3471 10K 5% 1/16W MF-LF 402

97 25 20 AP PWR EN

33 AP_PWR_EN_FET

=PP3V3_S3_MINI_CONN 33

C3408 0.1UF 10% 16V X5R 402

=PP3V3_S3_MINI 6 33

R3412 100K 1% 1/16W MF-LF 402

97 33 PM_PGOOD_MINI

Q3406 SLG4AP016V TDFN

VDD

SENSE 0.7V

RDLY

RESET*

MR*

EN

IN

OUT (OD)

THRM PAD

GND

RESET HAS 100MS DELAY ONCE ENABLE IS HIGH

MINI RESET L 27 97

AP_PWR_EN_FET 33

MINI CLKREQ L 15 97

33 IN AP MINI CLKREQ L

73 64 6 =PP12V_S5_PWRCTL

CRITICAL Q3403 IRFH3702TRPBF PQFN

C3461 0.1UF 10% 16V X5R 402

PP3V3_S3_MINI_CONN 95

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

=PP3V3_S3_MINI_CONN 33

33 6 =PP3V3_S3_MINI

P3V3_S0_MINI_EN

=PP3V3_S3_MINI

R3410 10K 5% 1/16W MF-LF 402

97 33 PM_PGOOD_MINI

U3404 SLG5AP001 TDFN

VCC

D

G

PG

ON

S

NC

THRM PAD

GND

CRITICAL

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE: PCI-E Wireless Connector	
Apple Inc.	DRAWING NUMBER: 051-8115 SIZE: D
	REVISION: 11.1.0
	BRANCH:
	PAGE: 34 OF 110
	SHEET: 33 OF 98

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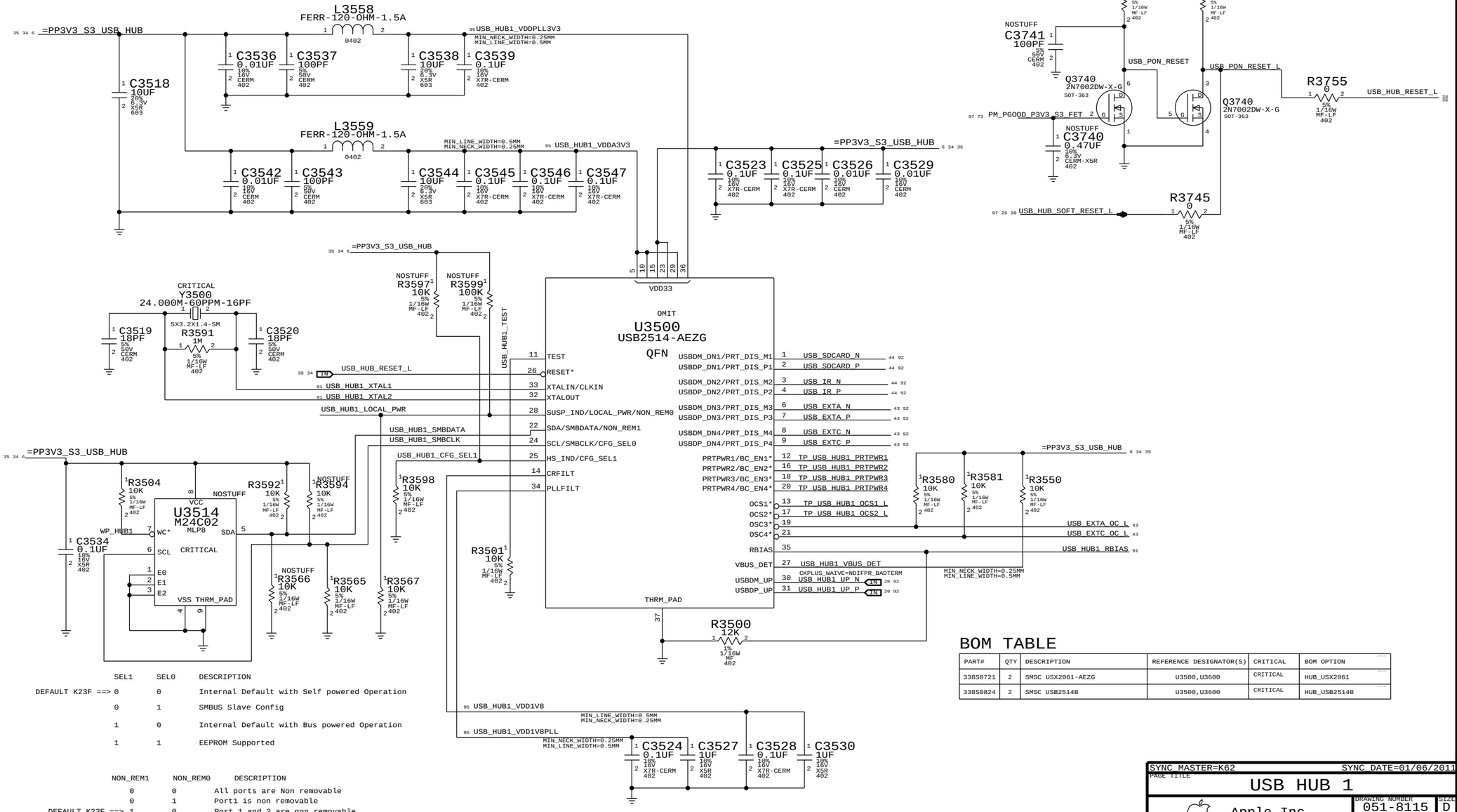
USB HUB-1



SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==> 0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are Non removable
0	1	Port1 is non removable
DEFAULT K23F ==> 1	0	Port 1 and 2 are non removable
1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0721	2	SMSC USX2061-AEZG	U3500,U3600	CRITICAL	HUB_USX2061
338S0824	2	SMSC USB2514B	U3500,U3600	CRITICAL	HUB_USB2514B

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: USB HUB 1

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

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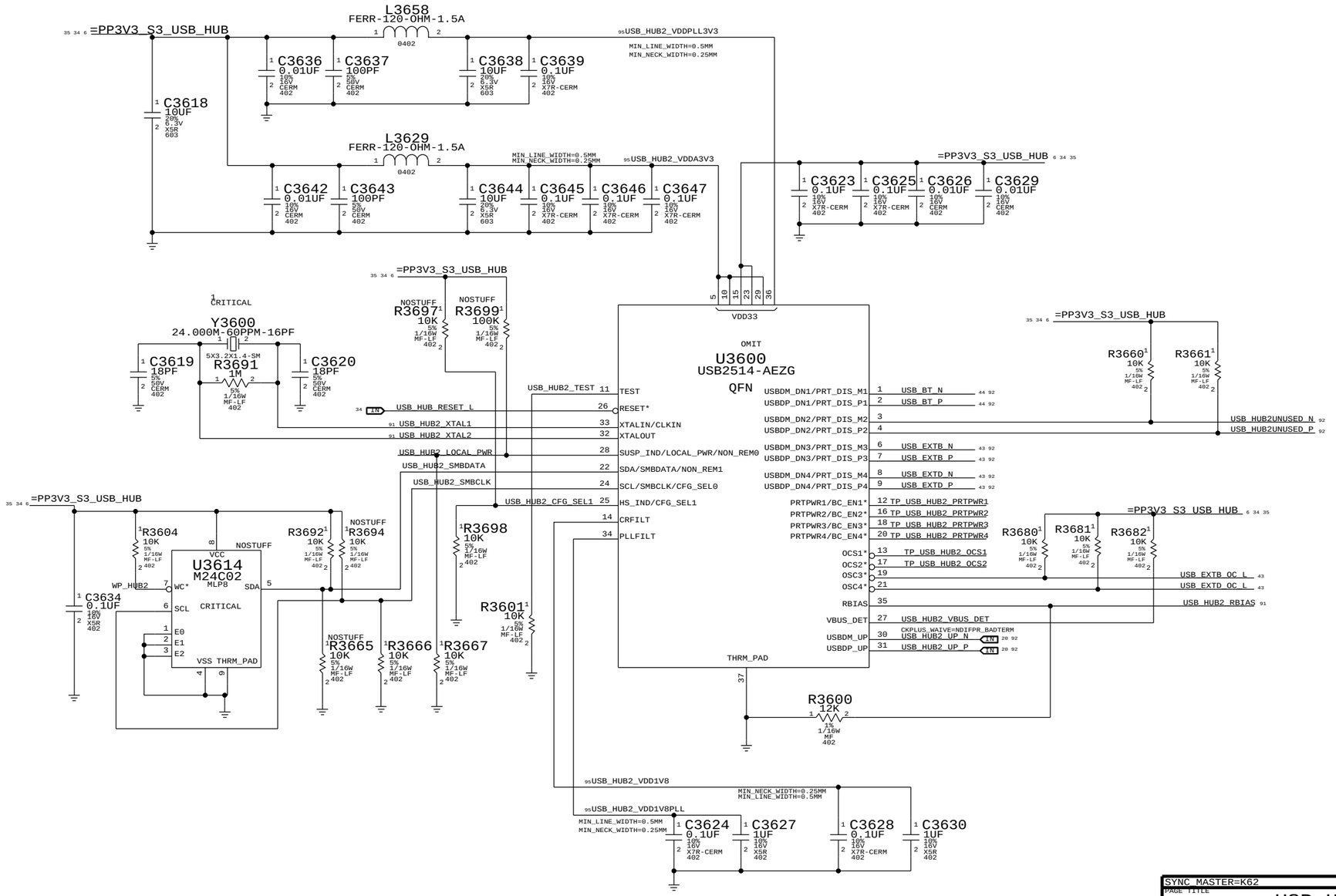
USB HUB-2



SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE	USB HUB 2
Apple Inc.	DRAWING NUMBER 051-8115 SIZE D
	REVISION 11.1.0
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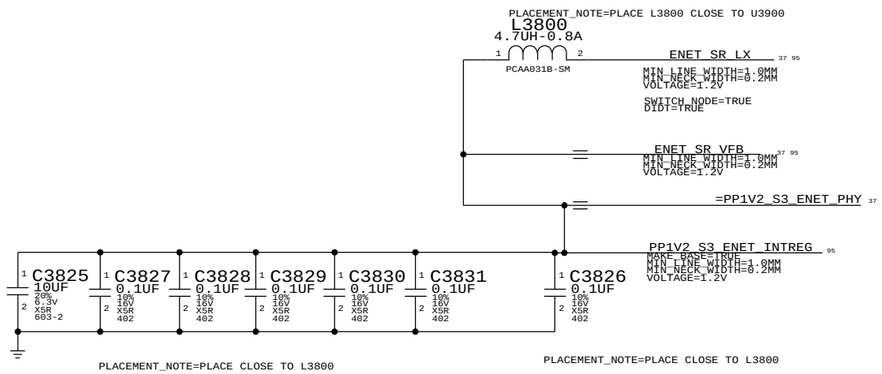
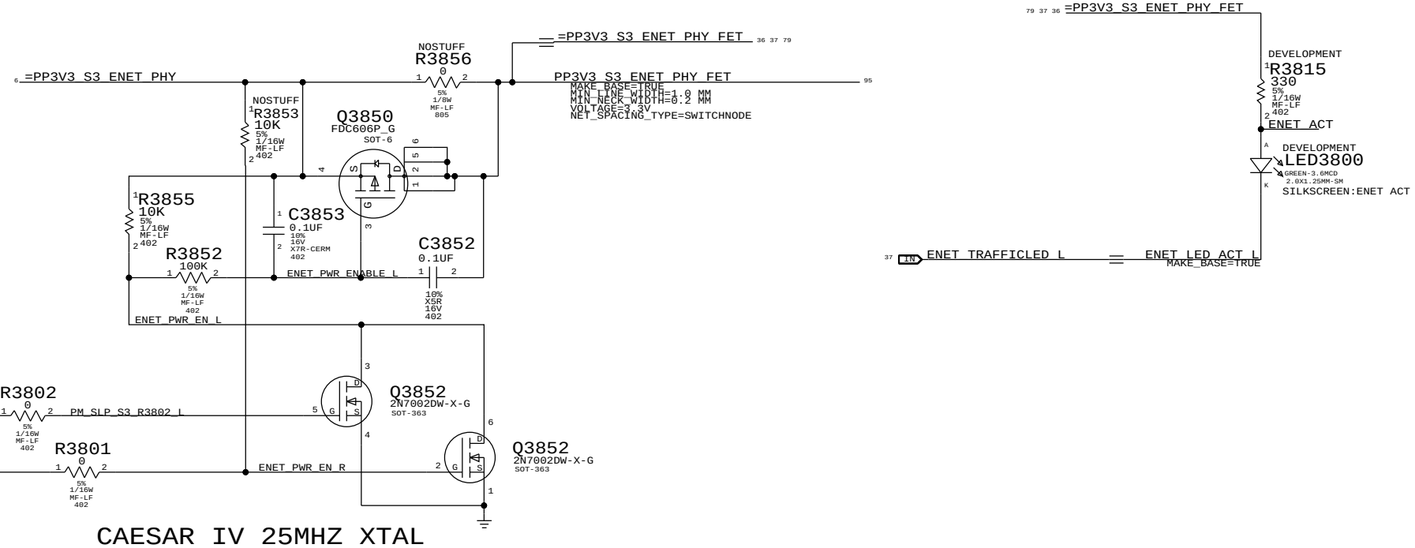
CAESAR IV 1.2V INT.VR CMPTS



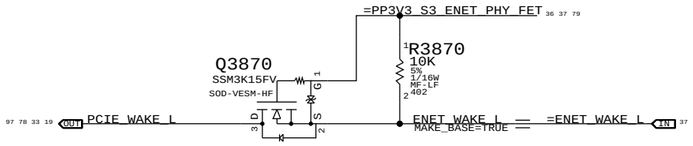
CAESAR IV POWER ENABLE CIRCUIT

3V3_ENET_PHY_FET = S0 || (S3 POWER && ENET_PWR_EN)

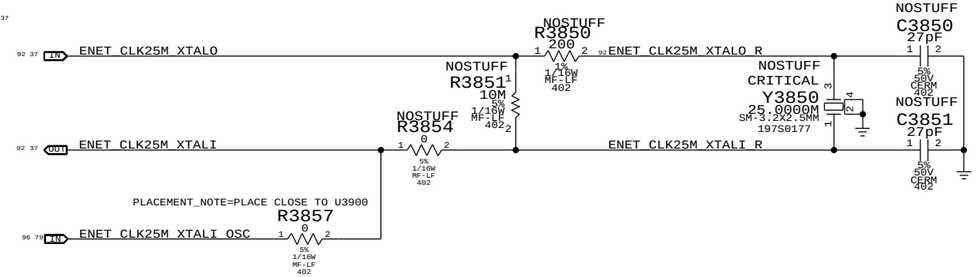


CAESAR IV ACTIVITY LED

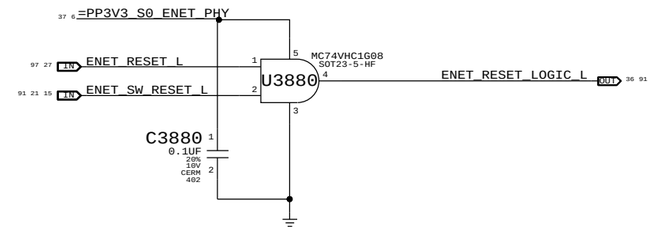
CAESAR IV WAKE# ISOLATION



CAESAR IV 25MHZ XTAL

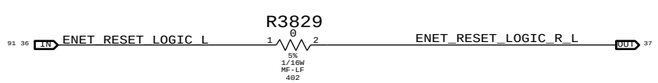


CAESAR IV SW RESET GATING

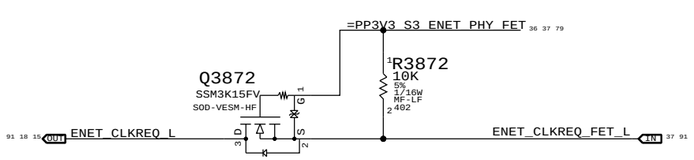


CAESAR IV STRAPS (NONE)

CAESAR IV RESET CONNECTION



CAESAR IV CLKREQ ISOLATION



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: CAESAR IV SUPPORT

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

281mA (1000base-T max power, Caesar IV)

79 37 36 =PP3V3_S3_ENET_PHY_FET

R3901 0 5% 1/16W MF-LF 402 — 95 ENET_3V3_S3_SR_IN
SWITCH_NODE=TRUE
DIDT=TRUE
NET_SPACING_TYPE=SWITCHNODE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

C3980 0.1UF 10% 16V X5R 402
C3981 0.1UF 10% 16V X5R 402
C3979 4.7UF 20% 6.3V CERM 603

CRITICAL
L3900 FERR-600-OHM-0.5A SM — 95 PP3V3_S3_ENET_PHY_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3900 0.1UF 10% 16V X7R-CERM 402

R3900 0 5% 1/16W MF-LF 402 — 95 ENET_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

VDD for Card Reader I/O
37 =PP3V3R1V8_ENET_LR_OUT

CRITICAL
L3905 FERR-600-OHM-0.5A SM — 95 PP3V3_S3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL
L3910 FERR-600-OHM-0.5A SM — 95 PP3V3_S3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 402
C3911 0.1UF 10% 16V X7R-CERM 402

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402

C3917 0.1UF 10% 16V X7R-CERM 402
C3918 0.1UF 10% 16V X7R-CERM 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

42 AVDDH
48 BIASVDDH
37 XTALVDDH
17
7
20 VDDO
56
62
14 SR_VDD
15 SR_VDDP
16 SR_LX
13 SR_VFB
39
45 AVDDL
51
29
32 PCIE_PLLVDDL
36 GPHY_PLLVDDL
35 VDDC
61

ENET_SR_LX 36 95
ENET_SR_VFB 36 95

Internal 1.2V Switching Regulator pins.

=PP1V2_S3_ENET_PHY 36
396mA (1000base-T, Caesar II)

CRITICAL
L3920 FERR-600-OHM-0.5A SM — 95 PP1V2_S3_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3921 0.1UF 10% 16V X7R-CERM 402
C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL
L3925 FERR-600-OHM-0.5A SM — 95 PP1V2_S3_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3926 0.1UF 10% 16V X7R-CERM 402
C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL
L3930 FERR-600-OHM-0.5A SM — 95 PP1V2_S3_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3931 0.1UF 10% 16V X7R-CERM 402
C3930 4.7UF 10% 6.3V X5R-CERM 603

C3936 0.1UF 10% 16V X7R-CERM 402
C3935 10UF 10% 6.3V X5R 805

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

=PP3V3R1V8_ENET_LR_OUT 37
PP3V3R1V8_ENET_LR_OUT_REG 95
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

DEVELOPMENT
C3970 4.7UF 10% 6.3V X5R-CERM 603
C3971 0.1UF 10% 16V X7R-CERM 402
C3972 0.1UF 10% 16V X7R-CERM 402
NOSTUFF
R3959 150 5% 1/16W MF-LF 402
NOSTUFF
C3959 10PF 5% 50V CERM 402

MUST DO: REMOVE C/R3959 AFTER PROTO 2

36 6 =PP3V3_S0_ENET_PHY

R3942 1K 5% 1/16W MF-LF 402 — Current Limiting Resistor

C3950 0.1uF 10% 16V X5R 402
C3951 0.1uF 10% 16V X5R 402
C3955 0.1uF 10% 16V X5R 402
C3956 0.1uF 10% 16V X5R 402

92 18 OUT PCIE_ENET_D2R_N
92 18 OUT PCIE_ENET_D2R_P
92 18 IN PCIE_ENET_R2D_C_P
92 18 IN PCIE_ENET_R2D_C_N

R3943 0 5% 1/16W MF-LF 402
36 IN =ENET_WAKE_L
(See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT — 58 VMAIN_PRSNT (IPD-ENET)
92 PCIE_ENET_D2R_C_N — 27 PCIE_TXD_N
92 PCIE_ENET_D2R_C_P — 28 PCIE_TXD_P
92 PCIE_ENET_R2D_P — 33 PCIE_RXD_P
92 PCIE_ENET_R2D_N — 34 PCIE_RXD_N
90 18 IN PCIE_CLK100M_ENET_P — 31 PCIE_REFCLK_P
90 18 IN PCIE_CLK100M_ENET_N — 30 PCIE_REFCLK_N
36 IN ENET_RESET_LOGIC_R_L — 11 PERST* (IPD)
91 36 OUT ENET_CLKREQ_FET_L — 12 CLKREQ* (OD)
ENET_WAKE_R_L — 3 WAKE* (OD)
97 21 15 IN ENET_LOW_PWR — 4 LOW_PWR (IPD)
ENET_SMB_CLK — 6 SMB_CLK
ENET_SMB_DATA — 10 SMD_DATA (IPD-ENETM)
37 BI ENET_SCLK — 66 SCLK
37 IN ENET_MISO — 64 SI/LINKLED*
37 BI ENET_MOSI — 65 SO
37 BI ENET_CS_L — 63 CS*
(IPU)
TP_ENET_SPD100LED_L — 2 SPD100LED*/SERIAL_DO (OD)
36 OUT ENET_TRAFFICLED_L — 67 TRAFFICLED*/SERIAL_DI (OD)
92 36 IN ENET_CLK25M_XTALI — 18 XTALI
92 36 OUT ENET_CLK25M_XTALO — 19 XTALO
92 ENET_RDAC — 38 RDAC

R3965 1.24K 1% 1/16W MF-LF 402

OMIT
U3900
BCM57765
QFN-8X8

TRD0_P 40 — ENETCONN_MDI_P<0> — 84 38 92
TRD0_N 41 — ENETCONN_MDI_N<0> — 84 38 92
TRD1_P 44 — ENETCONN_MDI_P<1> — 84 38 92
TRD1_N 43 — ENETCONN_MDI_N<1> — 84 38 92
TRD2_P 46 — ENETCONN_MDI_P<2> — 84 38 92
TRD2_N 47 — ENETCONN_MDI_N<2> — 84 38 92
TRD3_P 50 — ENETCONN_MDI_P<3> — 84 38 92
TRD3_N 49 — ENETCONN_MDI_N<3> — 84 38 92

(IPD) GPIO_0 5 — NC
GPIO_1/CR_BUS_PWR 8
RE*/GPIO_2 9 — ENET_MEDIA_SENSE — OUT 15 18 92

NOTE: "IPx" == Programmable pull-up/down
(IPx-ENET) SD_DETECT/WE* 1 — ENET_SD_DETECT_L — R3960 0 — SDCONN_DETECT_L — IN 45
SD_DETECT can only be used active low due to errata.
(IPU-ENET) CR_CMD/CLE 26 — ENET_SD_CMD — R3961 33 — SDCONN_CMD — IN 45 92
CR_CLK/RY_BY* 21 — ENET_SD_CLK — R3979 33 — SDCONN_CLK — OUT 45 92
(IPU-ENET) CR_DATA0 25 — ENET_CR_DATA<0> — R3971 33 — SDCONN_DATA<0> — BI 45 92
CR_DATA1 24 — ENET_CR_DATA<1> — R3972 33 — SDCONN_DATA<1> — BI 45 92
CR_DATA2 23 — ENET_CR_DATA<2> — R3973 33 — SDCONN_DATA<2> — BI 45 92
CR_DATA3 22 — ENET_CR_DATA<3> — R3974 33 — SDCONN_DATA<3> — BI 45 92
CR_DATA4 52 — ENET_CR_DATA<4> — R3975 33 — SDCONN_DATA<4> — BI 45 92
CR_DATA5 53 — ENET_CR_DATA<5> — R3976 33 — SDCONN_DATA<5> — BI 45 92
CR_DATA6 54 — ENET_CR_DATA<6> — R3977 33 — SDCONN_DATA<6> — BI 45 92
CR_DATA7 55 — ENET_CR_DATA<7> — R3978 33 — SDCONN_DATA<7> — BI 45 92
(IPU-ENET) CE*/MS_INS* 59 — NC_ENET_CE_L_MS_INS_L — NO_TEST=TRUE
(IPU-ENET) CR_LED/ALE 60 — ENET_CR_PWREN — OUT 45
(IPU-ENET) CR_WP*/XD_WP* 57 — SDCONN_WP — IN 45
XD_DETECT 68 — ENET_SR_DISABLE — R3980 1K — NOSTUFF — =PP3V3_S3_ENET_PHY_FET 36 37 79
(See note) — R3981 1K

(NO IPU OR IPD-ENET) THRM_PAD 69

ENET 1.2V SR IS ENABLED IF FLOATING.

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

ENET supports both active-levels for WP.

PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900
PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin can float (alias to TP_). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

79 37 36 =PP3V3_S3_ENET_PHY_FET

R3993 4.7K 5% 1/16W MF-LF 402
R3992 4.7K 5% 1/16W MF-LF 402
R3904 0 5% 1/16W MF-LF 402

U3990
AT45DB021D
SOIC-8S1
OMIT_TABLE

C3990 0.1UF 10% 16V X7R-CERM 402

37 IN ENET_SCLK — ENET_SCLK_R — SCK
37 IN ENET_CS_L — CS*
ENET_SWP_L — WP*
ENET_SRESET_L — RESET*
GND
SI — ENET_MOSI — IN 37
SO — ENET_MISO — OUT 37

NOSTUFF
R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=K62 SYNC_DATE=01/06/2013

PAGE TITLE
ETHERNET PHY (CAESAR IV)

Apple Inc.

DRAWING NUMBER 051-8115
SIZE D
REVISION 11.1.0
BRANCH
PAGE 39 OF 110
SHEET 37 OF 98

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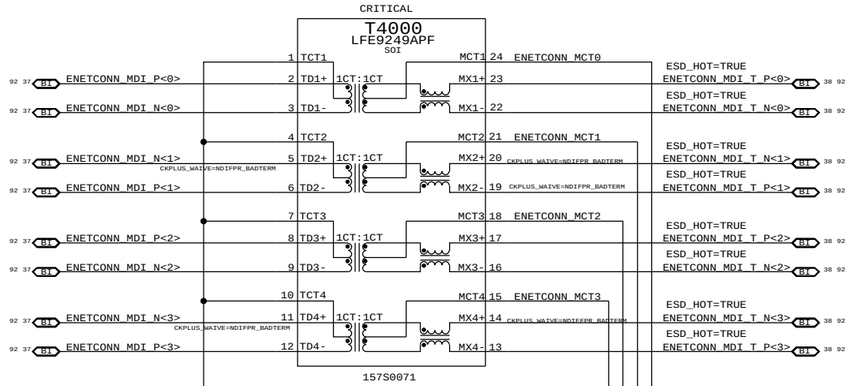
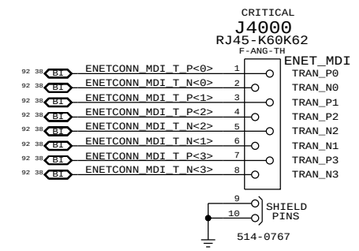
THIS PAGE DIFFERENT BETWEEN K60 and K62.



NO PAIR AND PIN POLARITY SWAPS



SYNC_MASTER=K60_MARK SYNC_DATE=01/06/2011

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 40 OF 110

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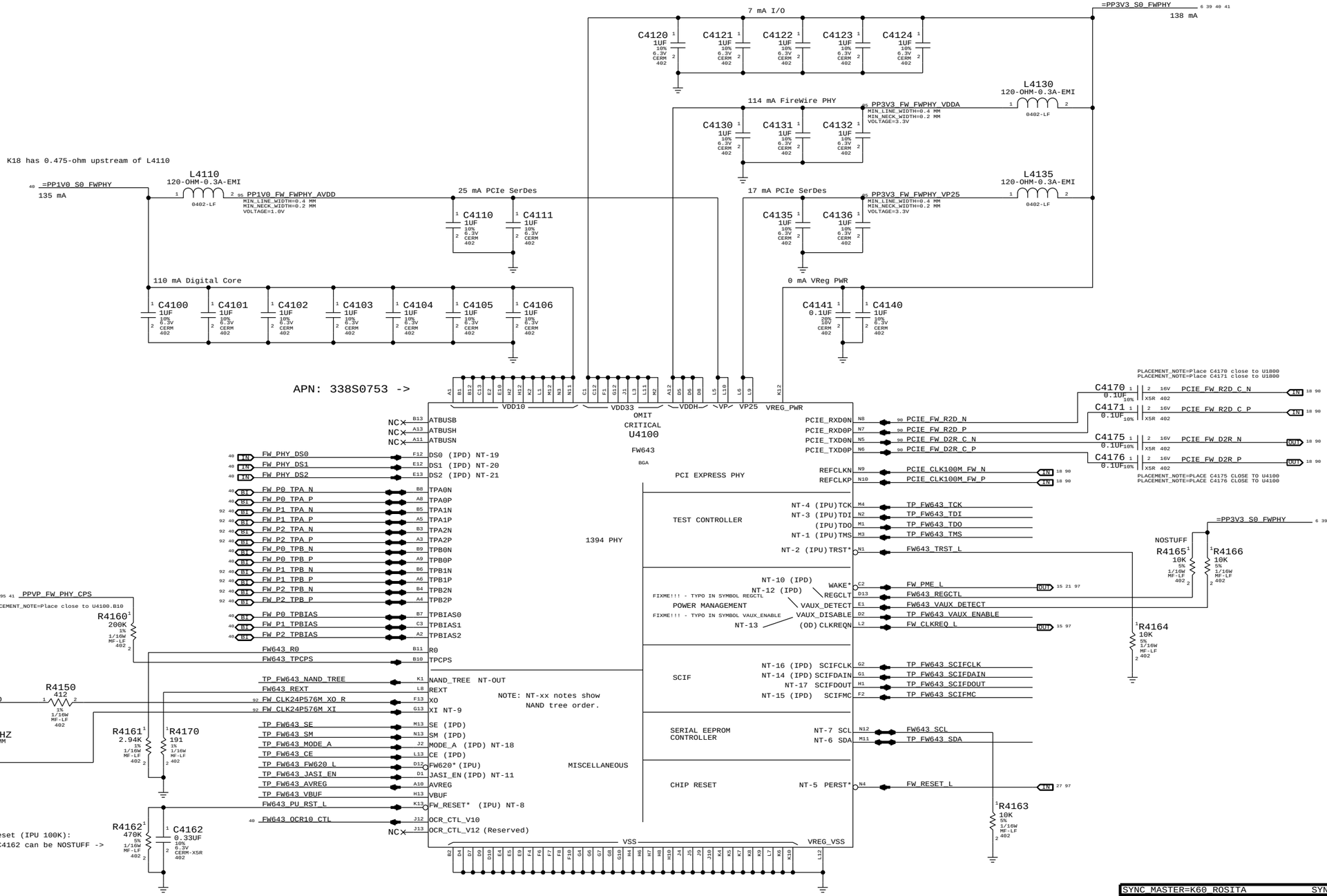

SYNC_MASTER=K60_ROSITA SYNC_DATE=01/06/2011

PAGE TITLE

FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

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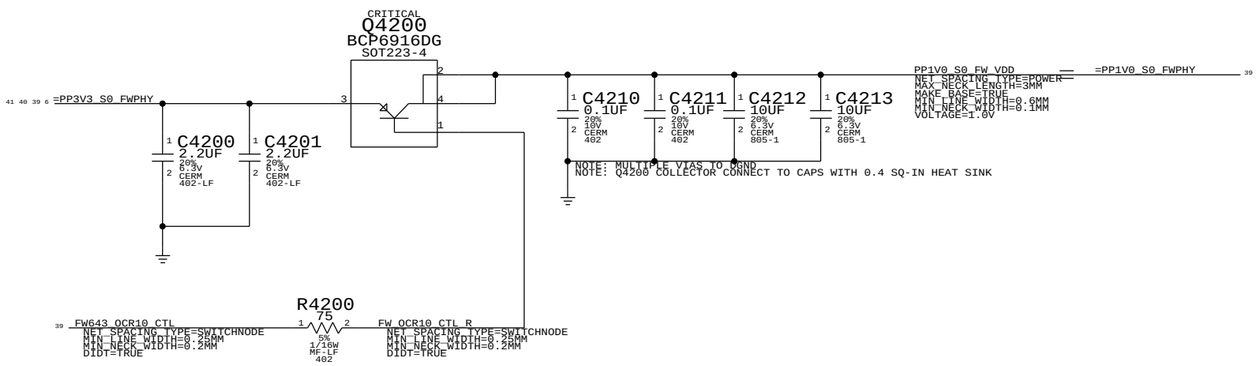
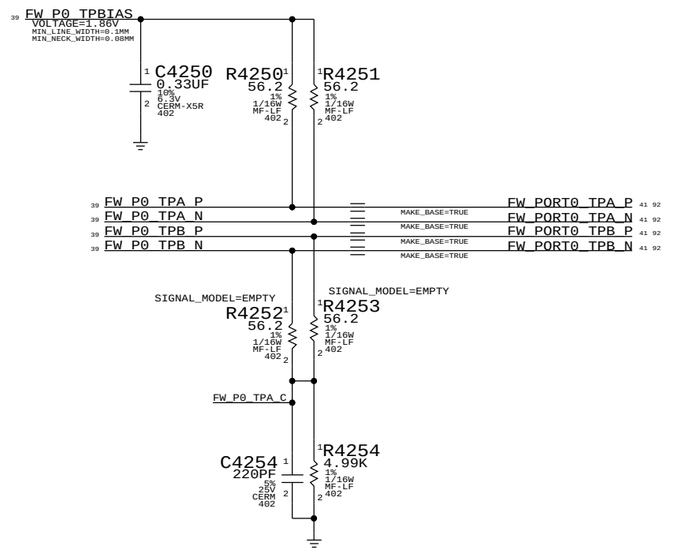
FW643 1.0V GENERATION

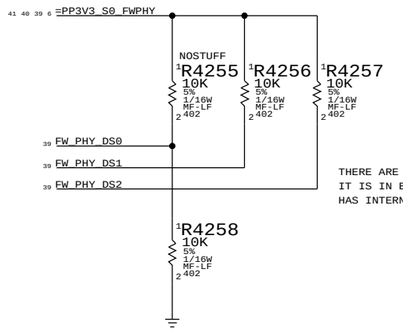


Termination

Place close to FireWire PHY



1394 PHY DATA/STROBE OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

2ND & 3RD TPA/TPB PAIR UNUSED

39	FW_P1_TPBIAS	NC_FW_PORT1_TPBIAS	MAKE_BASE=TRUE, NO_TEST=TRUE
92 39	FW_P1_TPA_P	NC_FW_PORT1_TPA_P	MAKE_BASE=TRUE, NO_TEST=TRUE
92 39	FW_P1_TPA_N	NC_FW_PORT1_TPA_N	MAKE_BASE=TRUE, NO_TEST=TRUE
92 39	FW_P1_TPB_P	NC_FW_PORT1_TPB_P	MAKE_BASE=TRUE, NO_TEST=TRUE
92 39	FW_P1_TPB_N	NC_FW_PORT1_TPB_N	MAKE_BASE=TRUE, NO_TEST=TRUE
39	FW_P2_TPBIAS	NC_FW_PORT2_TPBIAS	MAKE_BASE=TRUE, NO_TEST=TRUE
92 39	FW_P2_TPA_P	NC_FW_PORT2_TPA_P	MAKE_BASE=TRUE, NO_TEST=TRUE
92 39	FW_P2_TPA_N	NC_FW_PORT2_TPA_N	MAKE_BASE=TRUE, NO_TEST=TRUE
92 39	FW_P2_TPB_P	NC_FW_PORT2_TPB_P	MAKE_BASE=TRUE, NO_TEST=TRUE
92 39	FW_P2_TPB_N	NC_FW_PORT2_TPB_N	MAKE_BASE=TRUE, NO_TEST=TRUE

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: FireWire: 1394B MISC

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

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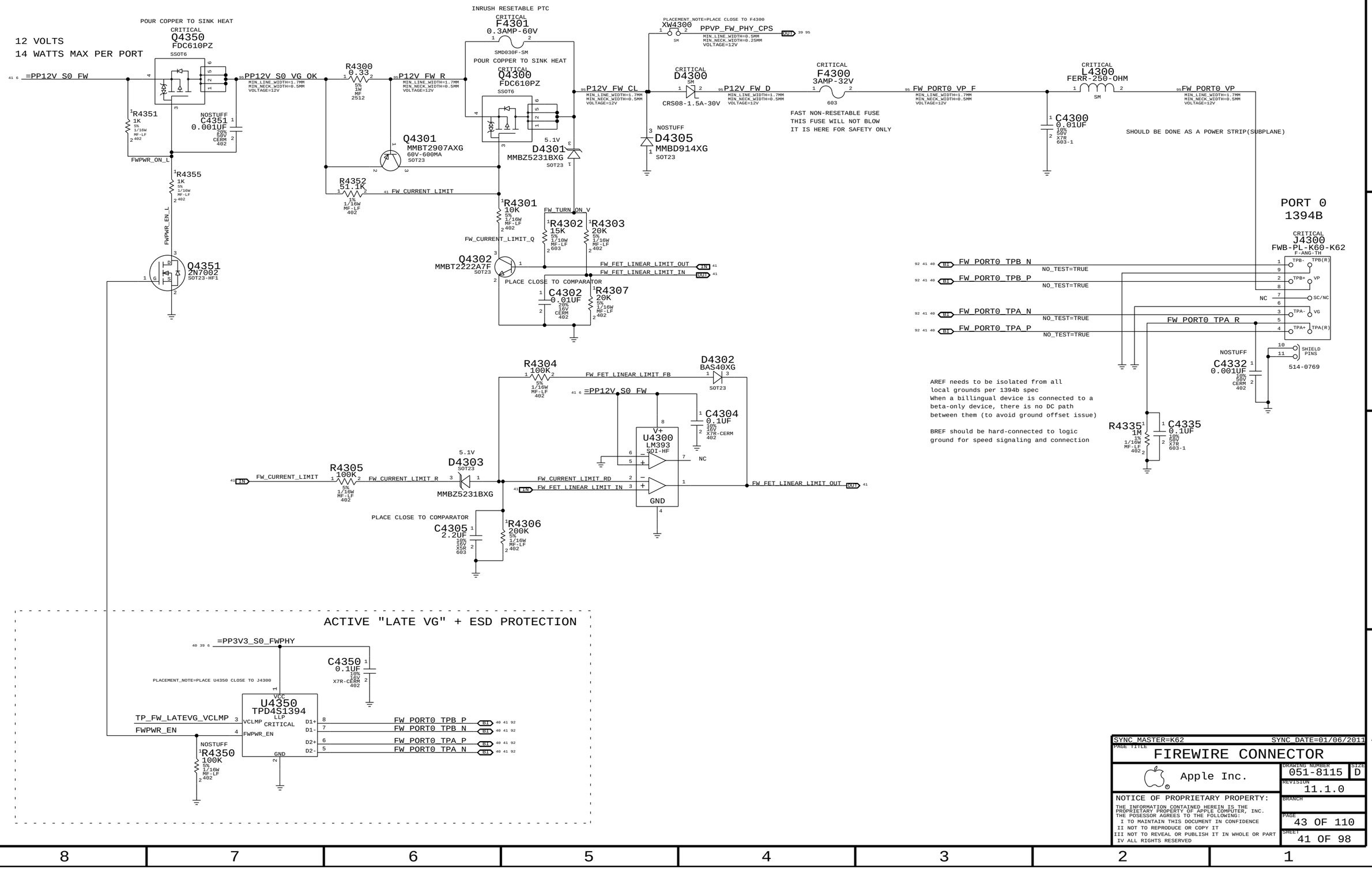

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PAGE TITLE

FIREWIRE CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

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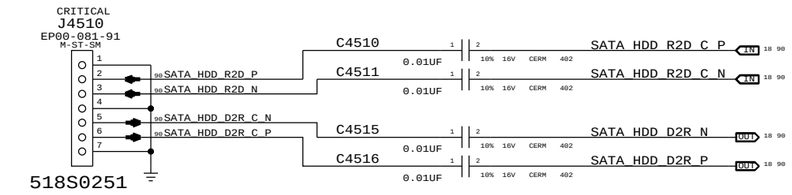
BOMOPTION OPTIONS FOR SATA PORT A1 AND A2

A1	A2	ODD_SATA:P1	ODD_SATA:P2
SSD	ODD		X
ODD		X	

USE OF PORT A2 FOR SSD IS NOT INTENDED VIA BOMOPTION THOUGH MLB SUPPORTS IT.
K60E should stuff S_P1_ODD:YES because it has no SSD option.

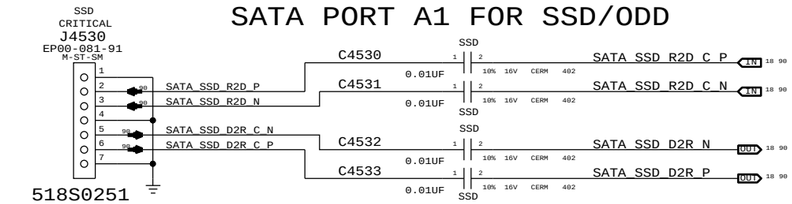
SILKSCREEN:SATA0

SATA PORT A0 FOR HDD



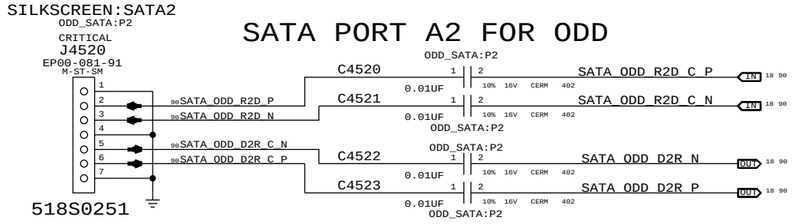
SILKSCREEN:SATA1

SATA PORT A1 FOR SSD/ODD

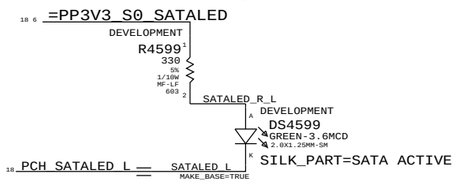


SILKSCREEN:SATA2
ODD_SATA:P2

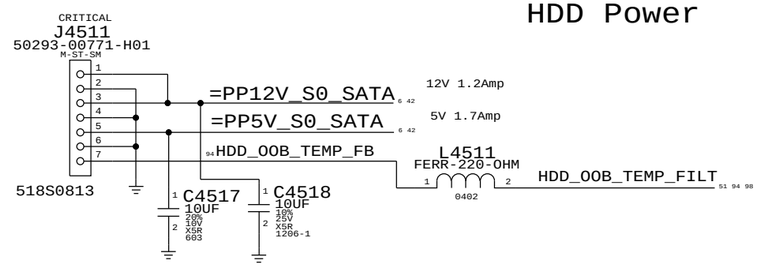
SATA PORT A2 FOR ODD



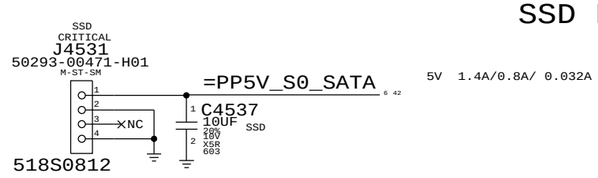
SATA Activity LED



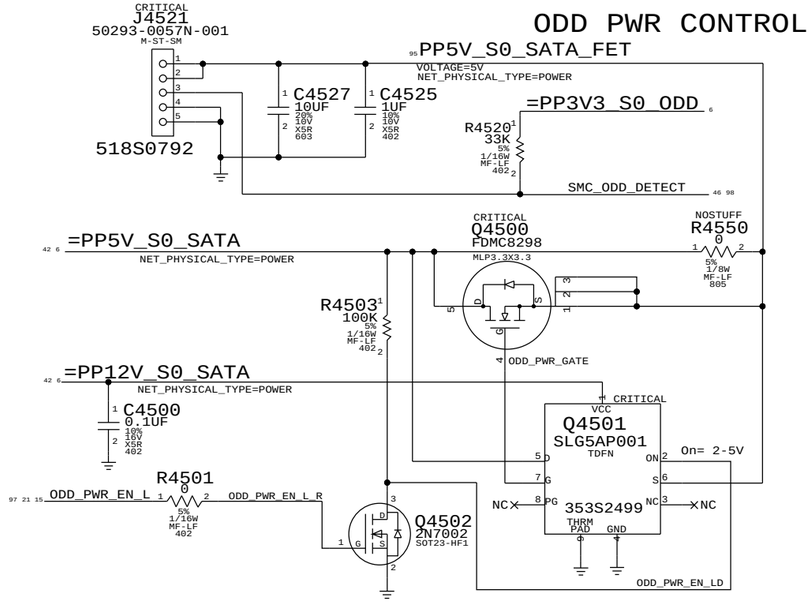
HDD Power



SSD Power



ODD PWR CONTROL



SYNC_MASTER=K60_JERRY SYNC_DATE=01/06/2011

PAGE TITLE

SATA Connectors

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DRAWING NUMBER 051-8115 SIZE D

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USB/SMC DEBUG MUX

ADDED AT EVT & SWITCH TO S5 RAIL

Current Limit at 2.1Amp (@ S3 & S0)

=PP5V_S3_USB

U4600 TPS2561DR SON

C4601 0.1UF 20% 16V CERM 402

C4602 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

R4600 23.2K 1% 1/16W MF-LF 402

Place R4600 very close to ILIM pin

PM_EN_USB_PWR

USB_EXTC_OC_L

USB_EXTD_OC_L

=PP3V3_G3H_SMCUSBMUX

=PP3V3_S5_SMCUSBMUX

R4653 0 NOSTUFF

R4654 0 MOJOMUX:YES

PP5V_USB_PORT3

155S0329 L4630 FERR-220-OHM-2.5A

VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB_PORT2

C4603 0.1UF C4630 0.01uF C4661 0.1UF C4660 0.01uF

(PUT CAP ON CONNECTOR SIDE)

PP3V3_SMCUSBMUX

C4650 0.1UF MOJOMUX:YES

PP5V_USB_PORT3_F

PP5V_USB_PORT2_F

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V

SMC_RX_L

SMC_TX_L

USB_EXTD_P

USB_EXTD_N

U4650 PI3USB102ZLE TQFN

R4651 0 MOJOMUX:NO

R4652 0 MOJOMUX:NO

USB_DEBUGPRT_EN_L

SEL=1: CHOOSE USB
SEL=0: CHOOSE SMC

L4631 120-OHM-90MA DLP0NS

USB_D_MUXED_N

USB_D_MUXED_P

USB_PORT3_N

USB_PORT3_P

J4630 USB-K60K62 F-ANG-TH

514-0768

D4630 RCLAMP0502N SLP1210N6

PORT 3

=PP5V_S3_USB

U4620 TPS2561DR SON

C4621 0.1UF C4622 330UF

R4620 23.2K

Place R4620 very close to ILIM pin

PP5V_USB_PORT0

155S0329 L4600 FERR-220-OHM-2.5A

PP5V_USB_PORT0_F

VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB_PORT1

155S0329 L4620 FERR-220-OHM-2.5A

C4623 0.1UF C4624 0.01uF

C4633 0.1UF C4600 0.01uF

PP5V_USB_PORT1_F

VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

(PUT CAP ON CONNECTOR SIDE)

USB_EXTA_OC_L

USB_EXTB_OC_L

L4621 120-OHM-90MA DLP0NS

USB_EXTC_N

USB_EXTC_P

USB_PORT2_N

USB_PORT2_P

J4620 USB-K60K62 F-ANG-TH

514-0768

D4620 RCLAMP0502N SLP1210N6

PORT 2

L4611 120-OHM-90MA DLP0NS

USB_EXTB_N

USB_EXTB_P

USB_PORT1_N

USB_PORT1_P

J4610 USB-MG6-K60-K62 F-ANG-TH

514-0770

D4610 RCLAMP0502N SLP1210N6

PORT 1

L4601 120-OHM-90MA DLP0NS

USB_EXTA_N

USB_EXTA_P

USB_PORT0_N

USB_PORT0_P

J4600 USB-MG6-K60-K62 F-ANG-TH

514-0770

D4600 RCLAMP0502N SLP1210N6

PORT 0

USB PORT POWER:

EACH PORT IS HARDWARE Capable of :

STATE	MAX	MIN (WITHIN THE TOLERANCE)
S0, S3	2.7A	2.1A -- PER PORT

WHEN CURRENT HITS LIMIT, TPS2561 BECOME CONSTANT CURRENT MODE AND STAY AT THE LIMIT LEVEL UNTIL THERMAL SHUTDOWN WHEN JUNCTION REACH 130C

SOFTWARE WILL ALOW 500MA/PORT, PLUS 2700MA EXTRA POWER TO BE distributed to approved devices on a 1st-come, 1st-served basis.

EXAMPLE: Port 1 - iPad fast charging = 2100mA
Port 2 - Wired Keyboard = 1100mA
Port 3 - iPhone fast charging = 1000mA
PORT 4 - USB 2.0 500MA = 500MA
TOTAL: 4700MA

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: EXTERNAL USB CONNECTORS

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 46 OF 110

SHEET: 43 OF 98

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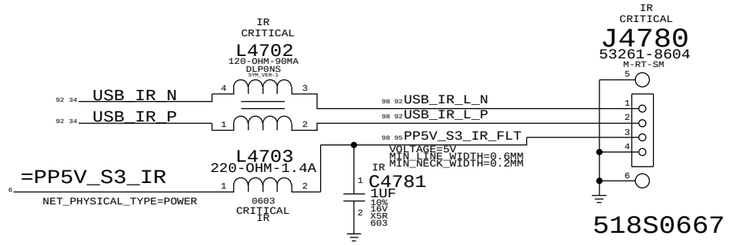
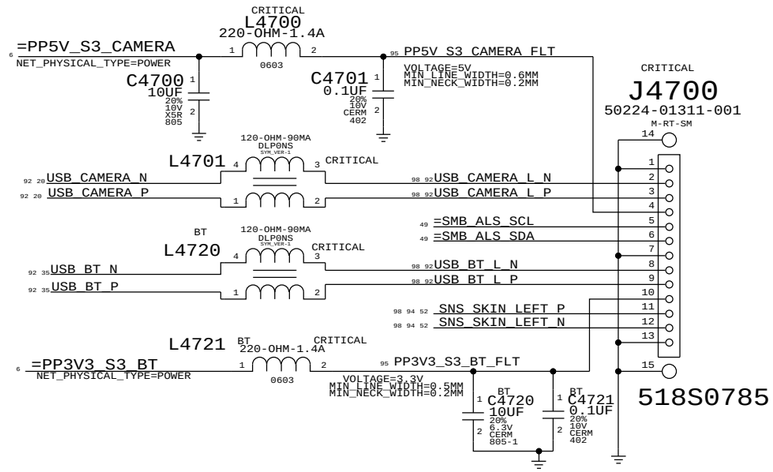
IR RECEIVER CONNECTOR

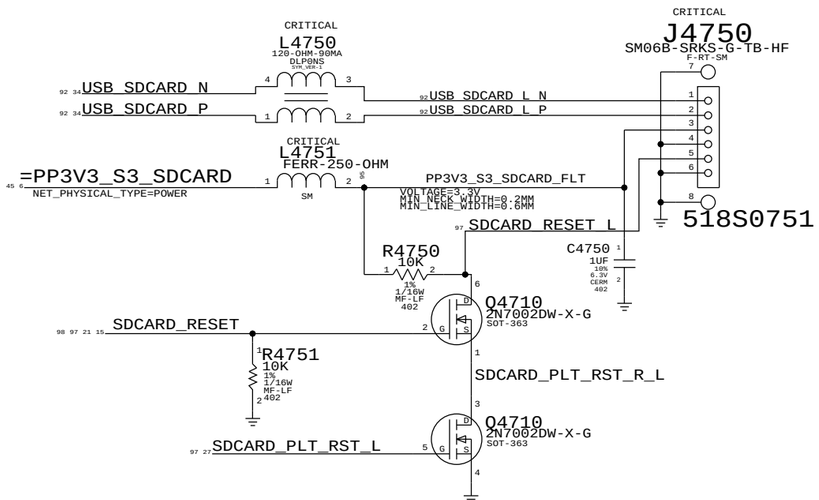


CAMERA/ALS & BLUETOOTH (K37A) CONNECTOR



Skin Temp sense at upper Left Screen corner

SD Card Reader Board (Lazarus)



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

Internal USB Connections

Apple Inc.

DRAWING NUMBER	051-8115
SIZE	D
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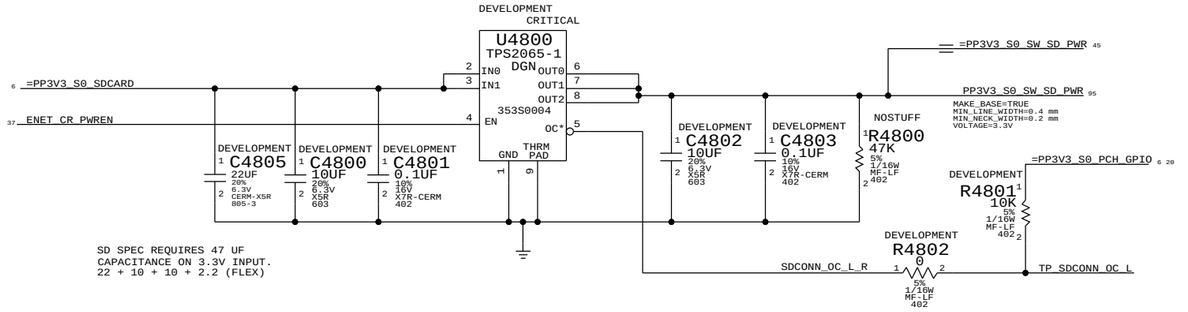
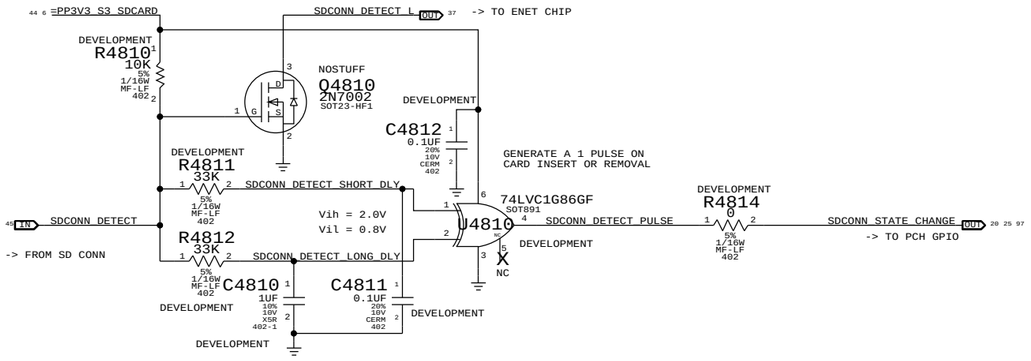
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

TPS2065-1 (1.0A LIMIT) HAS ACTIVE LOAD DISCHARGE SO R4800 IS NOSTUFF.

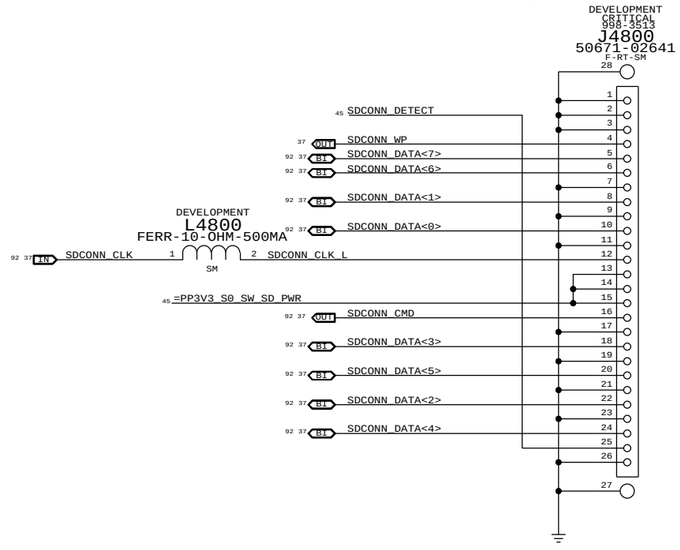


SD SPEC REQUIRES 47 UF
CAPACITANCE ON 3.3V INPUT.
22 + 10 + 10 + 2.2 (FLEX)

SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO CIRCUIT



SD CARD CONNECTOR



(CARD INSERTED = OPEN)
CAESAR-IV CARD DETECT IS PROGRAMMABLE, BUT A SILICON BUG MAKES THE ACTIVE-HIGH CASE UNUSABLE.

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
SD READER CONNECTOR

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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

338S0878

U4900
H8S2117
LFBGA
(1 OF 4)
OMIT

47 OUT	SMC_EXCARD_PWR_EN	B12	P10	
47 OUT	SMC_RSTGATE_L	C13	P11	
97 64 IN	ALL_SYS_PWRGD_SMC	A15	P12	
97 64 IN	RSMRST_PWRGD	B14	P13	
	NC	B15	P14	
97 27 OUT	PM_RSMRST_L	C14	P15	
47 OUT	CPUIMVP_VR_ON	D12	P16	
97 25 19 OUT	PM_PWRBTN_L	C15	P17	
K62 NEW:NOT USE	NC	D13	P20	
	NC	D14	P21	
	NC	D15	P22	
	NC	E12	P23	
K62 NEW:NOT USE	NC	E14	P24	
	NC	E15	P25	
K62 NEW:NOT USE	NC	E13	P26	
	NC	F14	P27	
91 48 18 BI	LPC_AD<0>	D9	P30	
91 48 18 BI	LPC_AD<1>	C9	P31	
91 48 18 BI	LPC_AD<2>	A9	P32	
91 48 18 BI	LPC_AD<3>	B9	P33	
91 48 18 IN	LPC_FRAME_L	D8	P34	
97 27 IN	SMC_LRESET_L	C8	P35	
91 27 IN	LPC_CLK33M_SMC	A8	P36	
48 18 BI	LPC_SERIRQ	D7	P37	
	NC	A5	P40	
K62 P1 NOT USED, WAS OOB_TEMP	NC	B5	P41	
49 BI	SMB_MGMT_DATA	D5	P42 (OC)	
47 OUT	SMS_ONOFF_L	C3	P43	
	NC	B1	P44	
	NC	C2	P45	
47 OUT	SMC_GFX_THROTTLE_L	D3	P46	
	NC	C1	P47	
48 47 46 43 OUT	SMC_TX_L	G1	P50	
48 47 46 43 IN	SMC_RX_L	G4	P51	
49 BI	SMB_0_S0_CLK	F2	P52 (OC)	

P60	L13	SMC_PM_G2_EN	OUT	74 97
P61	L14	NC		
P62	L15	NC		
P63	K12	NC		
P64	K13	SMC_ADAPTER_EN	OUT	19 47 97
P65	K14	NC		
P66	J12	SMC_PROCHOT_3_3_L	IN	47 97
P67	J13	SMC_BIL_BUTTON_L	IN	47
P70	N12	SMC_VCORE_ISENSE	IN	50 94 (IMON)
P71	R13	SMC_VCORE_VSENSE	IN	50 94 (IMON)
P72	P13	SMC_CPU_1V5_ISENSE	IN	50 94
P73	R14	SMC_CPU_1V5_VSENSE	IN	50 94
P74	P14	SMC_VCCSA_ISENSE	IN	50 94
P75	R15	SMC_VCCSA_VSENSE	IN	50 94
P76	N13	SMC_VAXG_ISENSE	IN	50 94 (IMON)
P77	P15	SMC_VAXG_VSENSE	IN	50 94 (IMON)
P80	C7	SMC_WAKE_SCI_L	OUT	15 18 21 97 PROTO-3, Change back to WAKE_SCI_L
P81	A7	NC		
P82	B7	PM_CLKRUN_L	OUT	15 19 48 97
P83	D6	LPC_PWRDWN_L	IN	19 48 97
P84	C6	SMC_TX_L	OUT	43 46 47 48
P85	A6	SMC_RX_L	IN	43 46 47 48
P86	B6	(OC) SMB_MGMT_CLK	BI	49
P90	K4	SMC_ONOFF_L	IN	47 97
P91	J2	SMC_BC_ACOK	IN	47
P92	J1	NC		
P93	J3	PM_SLP_S3_L	IN	5 19 26 32 36 47 63 82 97
P94	J4	PM_SLP_S4_L	IN	5 19 32 47 53 97 K60 New Change
P95	H2	PM_SLP_S5_L	IN	5 19 47 63 97 K60 New Change
P96	H1	PM_CLK32K_SUSCLK	IN	9 91 97
P97	G2	(OC) SMB_0_S0_DATA	BI	49

U4900
H8S2117
LFBGA
(2 OF 4)
OMIT

K62 NEW:NOT USE,PULLED UP	47 IN	SMC_PA0	R3	PA0
	97 18 OUT	SPI_DESCRIPTOR_OVERRIDE_L (OC)	P3	PA1
	97 27 25 19 OUT	PM_SYSRST_L (OC)	R2	PA2
	47 43 OUT	USB_DEBUGPRT_EN_L (OC)	N3	PA3
	47 IN	MEM_EVENT_A_L (OC)	R1	PA4
	47 IN	MEM_EVENT_B_L (OC)	N2	PA5
	47 BI	SYS_ONEWIRE (OC)	M4	PA6
	97 19 15 OUT	PM_BATLOW_L (OC)	N1	PA7
	NC		B10	PB0
PROTO-3:back to K75F	97 47 23 OUT	SMC_RUNTIME_SCI_L	A10	PB1
	98 42 IN	SMC_ODD_DETECT	D10	PB2
K62 NEW:NOT USE,PULLED UP	47 IN	(See below) SMC_PB3	A11	PB3
	94 51 IN	SMC_HDD_OOB_TEMP	B11	PB4
	NC		C11	PB5
K62 NEW:NOT USE,PULLED UP	IN	SMC_PB6	A12	PB6
	47 IN	SMC_GFX_OVERTEMP_L	D11	PB7
	53 OUT	SMC_FAN_0_CTL	G14	PC0
	53 OUT	SMC_FAN_1_CTL	G15	PC1
	NC		G13	PC2
	54 OUT	SMC_FAN_3_CTL	G12	PC3
	53 IN	SMC_FAN_0_TACH	H14	PC4
	53 IN	SMC_FAN_1_TACH	H15	PC5
	NC		H13	PC6
	54 IN	SMC_FAN_3_TACH	H12	PC7
(IMON)	94 50 IN	SMC_1V05_ISENSE	M11	PD0
(IMON)	94 50 IN	SMC_1V05_VSENSE	P11	PD1
	94 50 IN	SMC_PCH_1V05_ISENSE	R11	PD2
	94 50 IN	SMC_PCH_1V05_VSENSE	N11	PD3
	94 50 IN	SMC_GPU_ISENSE	P10	PD4
	94 50 IN	SMC_GPU_VSENSE	R10	PD5
	94 50 IN	SMC_DIMM_ISENSE	N10	PD6
	94 50 IN	SMC_DIMM_VSENSE	M10	PD7

PE0	M3	SMC_PE0	IN	47 K62 NEW:NOT USE,PULLED UP
PE1*	M2	SMC_TCK	IN	47 48
PE2*	M1	SMC_TDI	IN	47 48
PE3*	L4	SMC_TDO	OUT	47 48
PE4*	L2	SMC_TMS	IN	47 48
PF0	M7	G3_POWERON_L	IN	47
PF1	P6	SMC_SYS_LED	OUT	47
PF2	R6	SMC_LID		47
PF3	N6	NC		
PF4	M6	NC		
PF5	R5	BDV_BKL_PWM	OUT	83 97 K62 PROTO-2:NEW
PF6	P5	NC		
PF7	N5	NC		
PG0	P9	NC		
PG1	R9	SMC_SMS_INT	IN	47
PG2	N9	(OC) SMB_BSA_DATA	BI	49
PG3	P8	(OC) SMB_BSA_CLK	BI	49
PG4	R8	(OC) SMB_A_S3_DATA	BI	49
PG5	M8	(OC) SMB_A_S3_CLK	BI	49
PG6	P7	(OC) SMB_B_S0_DATA	BI	49
PG7	R7	(OC) SMB_B_S0_CLK	BI	49
PH0	E1	SMC_PROCHOT	OUT	47 97
PH1	F3	SMC_THRMTRIP	OUT	
PH2	K2	NC		
PECI	PH3 C4	CPU_PECI_R		97
PEVref	PH4 D4	PVCCIO_S0_SMC_R		97
PEVSTP	PH5 B3	PM_PECI_PWRGD_R		97

R4910 0 MF-LF 5% 1/16W 402 — CPU_PECI 11 21 97
R4911 0 MF-LF 5% 1/16W 402 — =PPVCCIO_S0_SMC 6 47
R4912 0 MF-LF 5% 1/16W 402 — PM_PECI_PWRGD 64 97
C4910 0.1UF 20% 10V CERM 402

SMC PB3: SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SMC PG1: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

95 47 46 PP3V3_G3H_AVREF_SMC Peak/Ave/Standby = 2mA/1mA/5uA
47 46 6 =PP3V3_G3H_SMC Peak/Ave/Sleep/Standby = 40mA/25mA/20mA/50uA

C4902 22UF 20% 6.3V CERM 805
C4903 0.1UF 20% 10V CERM 402
C4904 0.1UF 20% 10V CERM 402
C4905 0.1UF 20% 10V CERM 402
C4906 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place C4907 close to U4900 pin 13

R4999 4.7 5% 1/16W MF-LF 402

95 46 PP3V3_G3H_SMC_AVCC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.4V

SMC_VCL
C4907 0.47UF 10% 6.3V CERM-X5R 402

C4920 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place R4999 close to U4900 pin 76
PLACEMENT_NOTE=Place C4920 close to U4900 pin 76

U4900
H8S2117
LFBGA
(3 OF 4)
OMIT

97 48 47 IN	SMC_RESET_L	E3	RES*
94 47	SMC_XTAL	A2	XTAL
94 47	SMC_EXTAL	B2	EXTAL
		MD1	E2
		MD2	K1
		NMI	F4
		ETRST*	L1
		AVSS	R12

R4909 10K 5% 1/16W MF-LF 402
R4901 10K 5% 1/16W MF-LF 402
SMC_MD1 IN 48
SMC_KBC_MDE
SMC_NMI IN 48
SMC_TRST_L IN 48
NOSTUFF
R4902 10K 5% 1/16W MF-LF 402
R4998 10K 5% 1/16W MF-LF 402
R4903 0 5% 1/16W MF-LF 402
XW4900 SM
VSS

GND_SMC_AVSS 46 47 50 94

95 47 46 PP3V3_G3H_AVREF_SMC
47 46 6 =PP3V3_G3H_SMC
95 46 PP3V3_G3H_SMC_AVCC

U4900
H8S2117
LFBGA
(4 OF 4)
OMIT

E4		PJ0	C5 NC
N4		PJ1	B8 NC
M9		PJ2	C10 NC
M12	NC	PJ3	C12 NC
M13		PJ4	A14 NC
L12		PJ5	F15 NC
A3		PJ6	J14 NC
		PJ7	K15 NC
		PI0	N8 NC
		PI1	N7 NC
		PI2	M5 NC
		PI3	L3 NC
		PI4	K3 NC
		PI5	H3 NC
		PI6	H4 NC
		PI7	G3 NC

GND_SMC_AVSS 94 50 47 46

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
SMC

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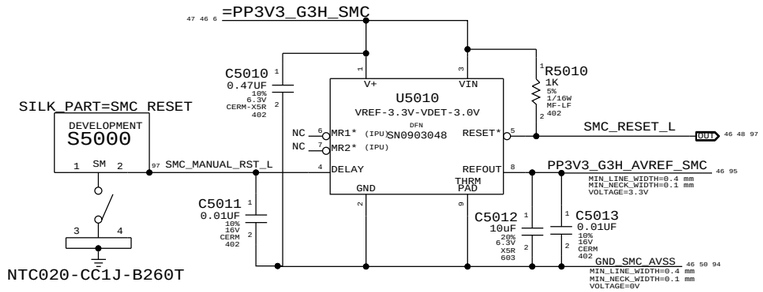
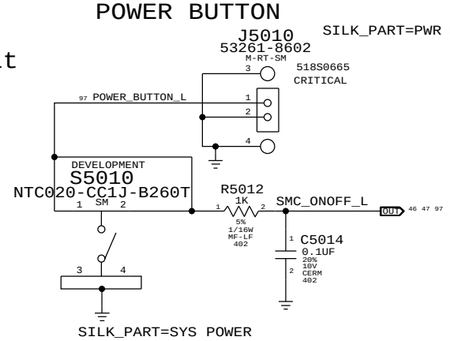
SMC Reset "Button", Supervisor & AVREF Supply



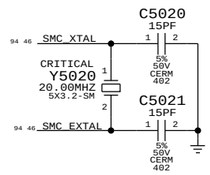
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

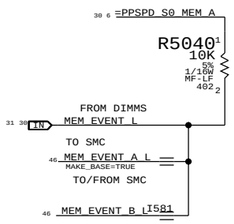
POWER BUTTON



SMC Crystal Circuit



MEM_EVENT



MISC. SIGNAL ALIASES

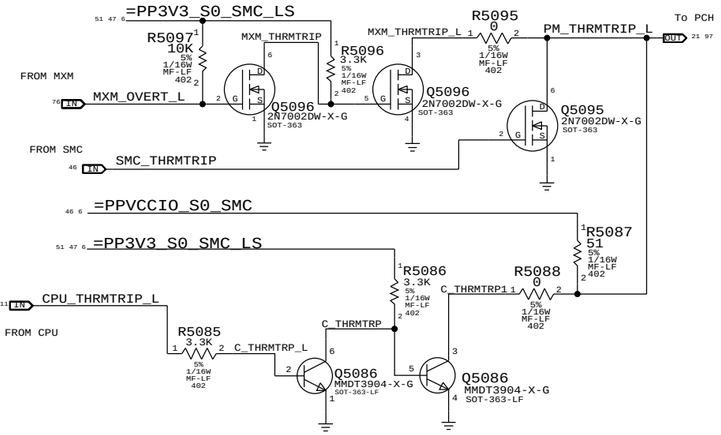
SMC_GFX_OVERTEMP_L ═ MXM_ALERT_L (MAKE_BASE=TRUE)
SMC_GFX_THROTTLE_L ═ MXM_PWR_LEVEL (MAKE_BASE=TRUE)
CPUIMVP_VR_ON ═ SMC_DELAYED_PWRGD (MAKE_BASE=TRUE)

UNUSED PORT 7 ANALOG SENSORS

UNUSED TP/NC ALIASES

SMC_EXCARD_PWR_EN ═ TP_SMC_EXCARD_PWR_EN (MAKE_BASE=TRUE)
SMS_ONOFF_L ═ TP_SMS_ONOFF_L (MAKE_BASE=TRUE)
SMC_RSTGATE_L ═ TP_SMC_RSTGATE_L (MAKE_BASE=TRUE)
SMC_SYS_LED ═ TP_SMC_SYS_LED (MAKE_BASE=TRUE)
SMC_PB3 ═ TP_SMC_PB3 (MAKE_BASE=TRUE)

SMC & MXM THERMTRIP LEVEL SHIFTING



=PP3V3_G3H_SMC

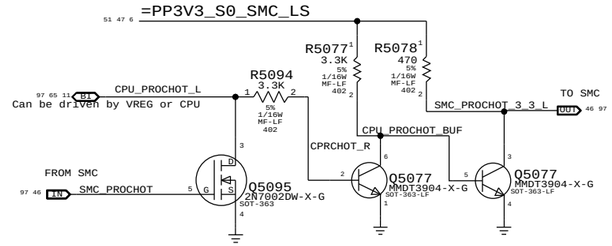
SMC_ONOFF_L	R5020	10K	5%	1/16W	MF-LF	402		
SMC_TX_L	R5021	10K	5%	1/16W	MF-LF	402		
SMC_RX_L	R5022	100K	5%	1/16W	MF-LF	402		
SYS_ONEWIRE	R5023	2.0K	5%	1/16W	MF-LF	402		
SMC_TMS	R5024	10K	5%	1/16W	MF-LF	402		
SMC_TDO	R5025	10K	5%	1/16W	MF-LF	402		
SMC_TDI	R5026	10K	5%	1/16W	MF-LF	402		
SMC_TCK	R5027	10K	5%	1/16W	MF-LF	402		
SMC_BIL_BUTTON_L	R5028	10K	5%	1/16W	MF-LF	402		
SMC_BC_ACOK	R5029	10K	5%	1/16W	MF-LF	402		
SMC_ADAPTER_EN	R5030	10K	5%	1/16W	MF-LF	402		
USB_DEBUGPRT_EN_L	R5031	10K	5%	1/16W	MF-LF	402		
G3_POWERON_L	R5034	10K	5%	1/16W	MF-LF	402		
SMC_SMS_INT	R5032	10K	5%	1/16W	MF-LF	402		
SMC_LID	R5033	10K	5%	1/16W	MF-LF	402		
SMC_PA0	R5037	100K	5%	1/16W	MF-LF	402		
SMC_PB6	R5038	100K	5%	1/16W	MF-LF	402		
SMC_PE0	R5036	100K	5%	1/16W	MF-LF	402		

=PP3V3_S0_SMC_LS

SMC_GFX_OVERTEMP_L	R5035	10K	5%	1/16W	MF-LF	402		
SMC_RUNTIME_SCI_L	R5044	10K	5%	1/16W	MF-LF	402		

PM_SLP_S3_L	R5041	100K	5%	1/16W	MF-LF	402		
PM_SLP_S5_L	R5042	100K	5%	1/16W	MF-LF	402		
PM_SLP_S4_L	R5043	100K	5%	1/16W	MF-LF	402		

SMC PROCHOT 3.3V LEVEL SHIFTING



SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER 051-8115
	SIZE D
	REVISION 11.1.0
	BRANCH
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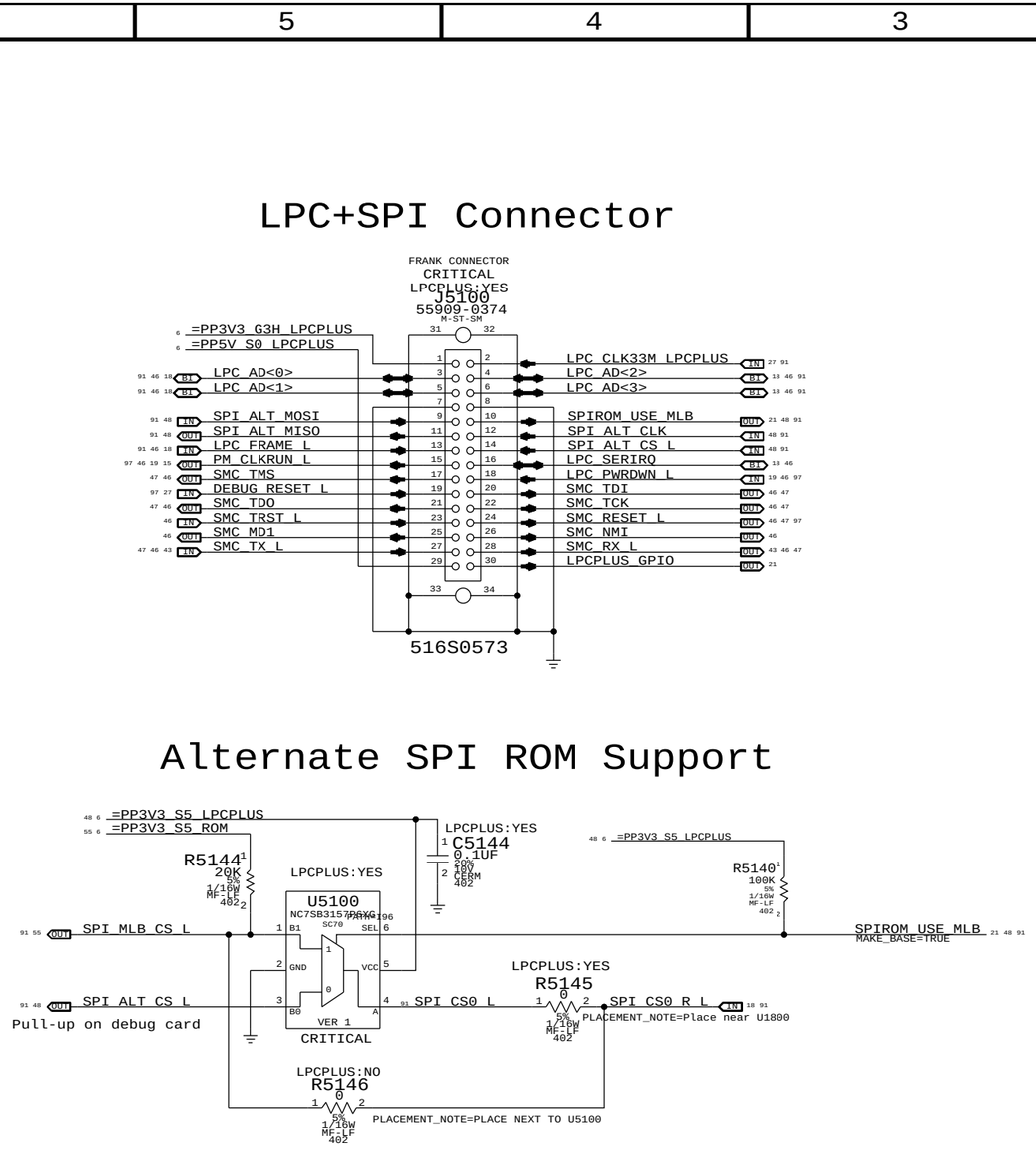
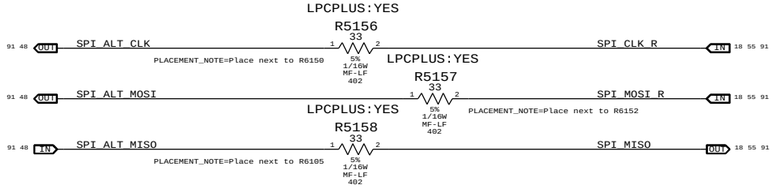
LPC+SPI Connector

Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC_MASTER=K62_AARON SYNC_DATE=11/30/2009

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

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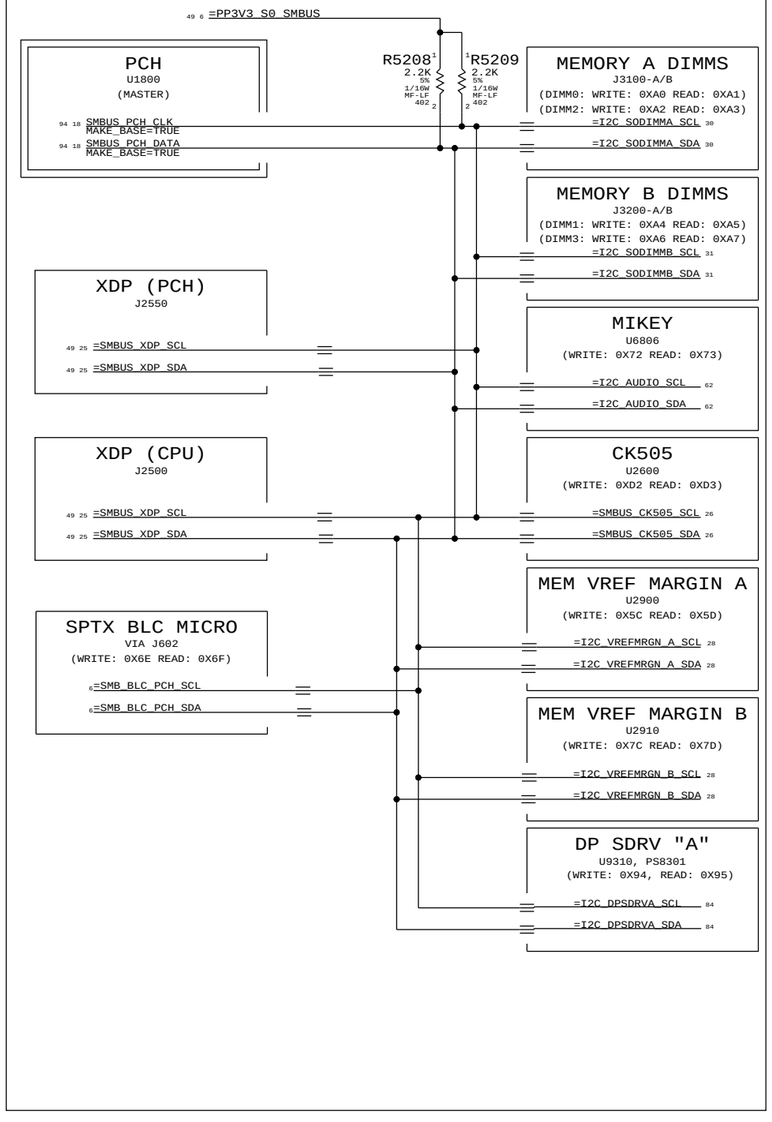
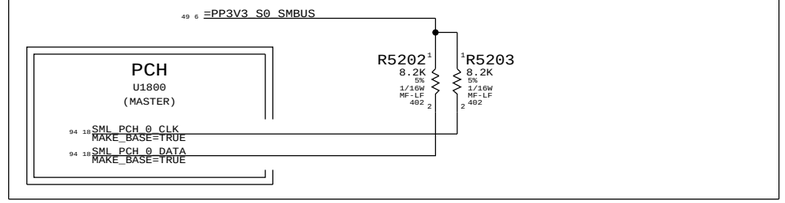
PCH "SMBUS" CONNECTIONS



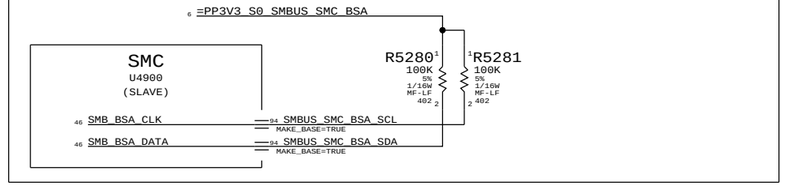
PCH "SML 0" CONNECTIONS



THIS PAGE DIFFERENT BETWEEN K60 AND K62.

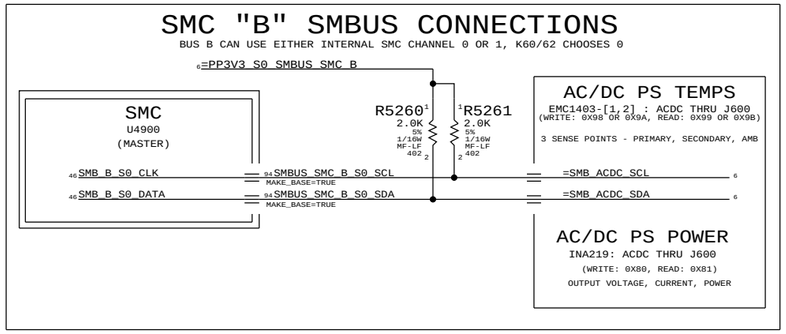
SMC SLAVE SMBUS "2" CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 2 ONLY (NO CONNECTIONS, JUST PULLUP)



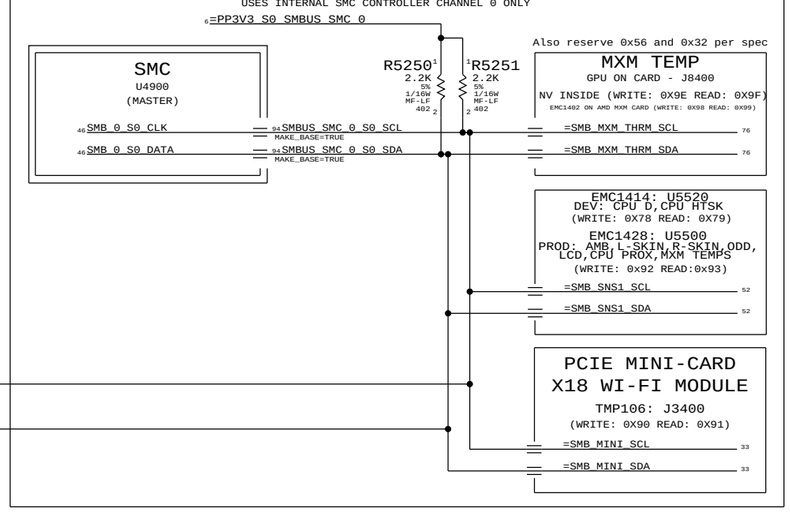
SMC "B" SMBUS CONNECTIONS

BUS B CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K60/62 CHOOSES 0

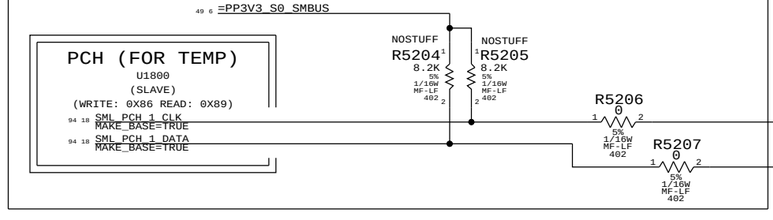


SMC "0" SMBUS CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 0 ONLY



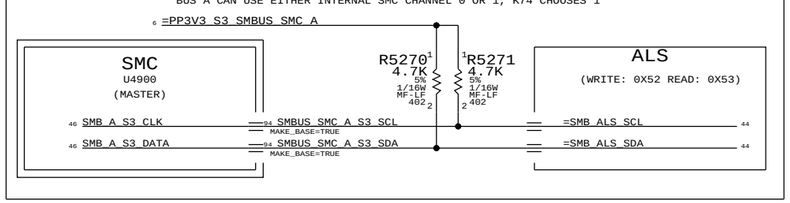
PCH "SML 1" CONNECTIONS



THE PCH address is user programmable by SPI ROM

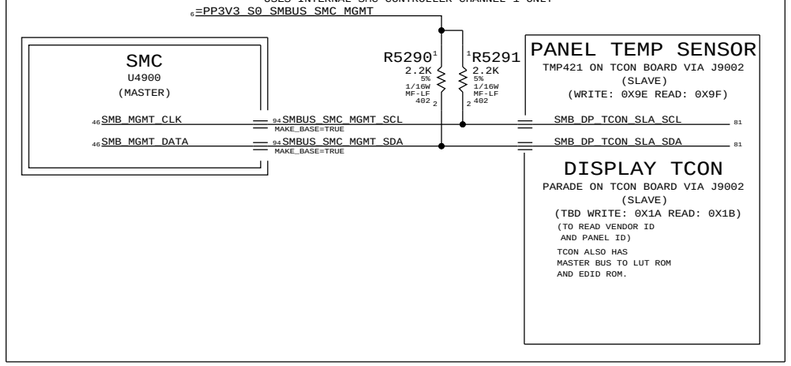
SMC "A" SMBUS CONNECTIONS

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE
BUS A CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K74 CHOOSES 1

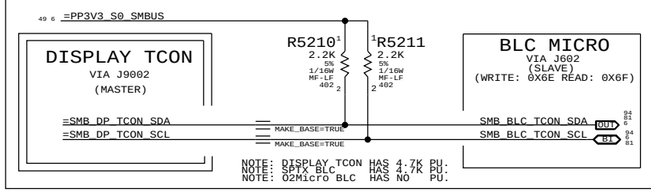


SMC "MANAGEMENT" SMBUS (BUS 1)

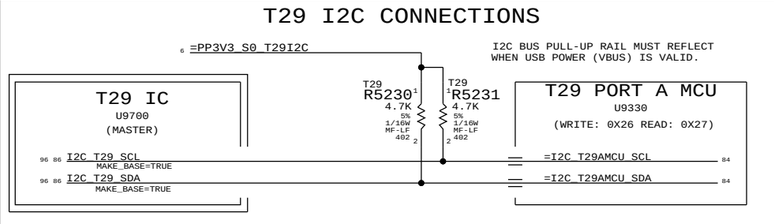
USES INTERNAL SMC CONTROLLER CHANNEL 1 ONLY



DISPLAY TCON TO SPTX OR O2M BLC



T29 I2C CONNECTIONS



SYNC_MASTER=K60_MARK SYNC_DATE=01/06/2011

PAGE TITLE

SMBUS CONNECTIONS

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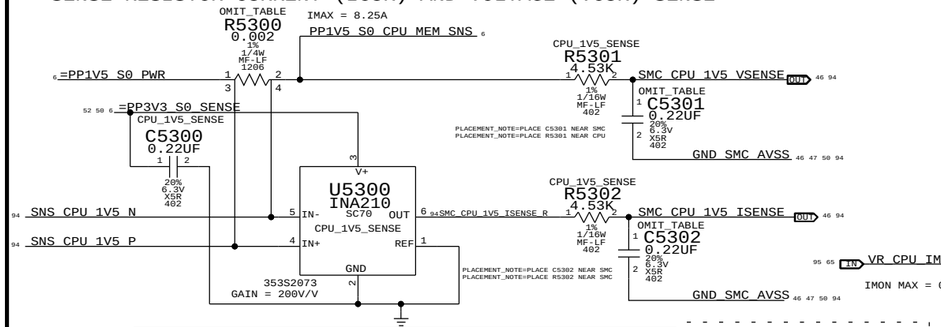
CPU VDD 1.5V

SENSE RESISTOR CURRENT (IC5R) AND VOLTAGE (VC5R) SENSE

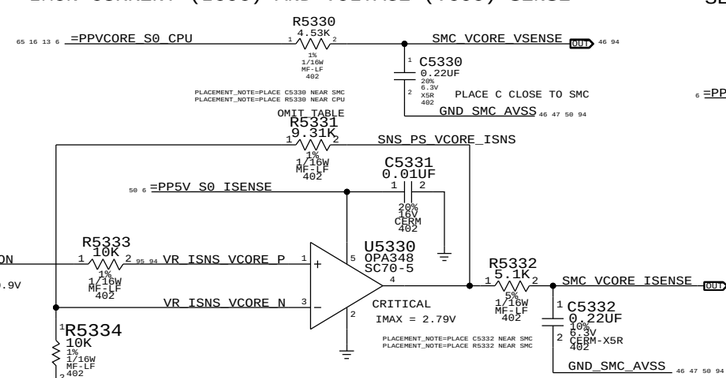


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5300	CPU_1V5_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5300	NO_CPU_1V5_SENSE
132S0080	2	CAP,0.22UF,402	C5301,C5302	CPU_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5301,C5302	NO_CPU_1V5_SENSE

THE NO_1V05_PCH_SENSE, NO_CPU_VCCSA_SENSE, AND NO_CPU_1V5_SENSE CONFIGURATIONS SHOULD IDEALLY NEVER BE USED AS TOTAL CPU POWER SENSING REQUIRES ALL 3 SENSORS.

CPU VCC (VCORE)

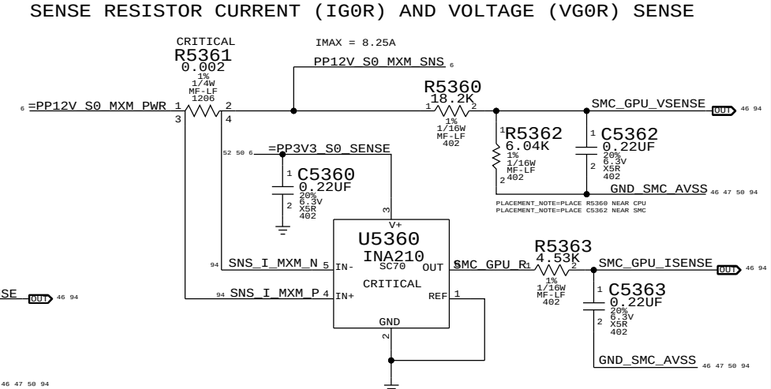
IMON CURRENT (IC0C) AND VOLTAGE (VC0C) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0312	1	RES,MTL FILM,1/16W,9.31K,0402	R5331	CPUVCORE-3PH
114S0345	1	RES,MTL FILM,1/16W,21K,0402	R5331	CPUVCORE-4PH

GPU MXM

SENSE RESISTOR CURRENT (IG0R) AND VOLTAGE (VG0R) SENSE



CPU VCCSA

SENSE RESISTOR CURRENT (ICSR) AND VOLTAGE (VCSR) SENSE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5310	CPU_VCCSA_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5310	NO_CPU_VCCSA_SENSE
132S0080	2	CAP,0.22UF,402	C5311,C5312	CPU_VCCSA_SENSE
116S0004	2	RES,0 OHM,402	C5311,C5312	NO_CPU_VCCSA_SENSE

CPU VAXG

IMON CURRENT (IC0G) AND VOLTAGE (VC0G) SENSE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5340,C5342	VAXG
116S0004	2	RES,0 OHM,402	C5340,C5342	NO_VAXG

DIMM VDD 1.5V (LIKELY DEVELOPMENT ONLY)

SENSE RESISTOR CURRENT (IM0R) AND VOLTAGE (VM0R) SENSE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5371,C5372	DIMM_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5371,C5372	PRODUCTION

PCH 1.05V

SENSE RESISTOR CURRENT (IN1R) AND VOLTAGE (VN1R) SENSE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5320	1V05_PCH_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5320	NO_1V05_PCH_SENSE
132S0080	2	CAP,0.22UF,402	C5321,C5322	1V05_PCH_SENSE
116S0004	2	RES,0 OHM,402	C5321,C5322	NO_1V05_PCH_SENSE

1.05V FOR CPU VCCIO, CPU VCCSA & PCH 1.05V

IMON CURRENT (IV1R) AND VOLTAGE (VV1R) SENSE

NOTE: TOTAL CPU POWER = VC0C+IC0C
+ VC5R*IC5R
+ VCSR*ICSR
+ VC0G*IC0G
+ VV1R*IC1R

where
IC1R = IV1R - IN1R - ICSR

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
CPU/PCH/GPU POWER SENSE

Apple Inc.

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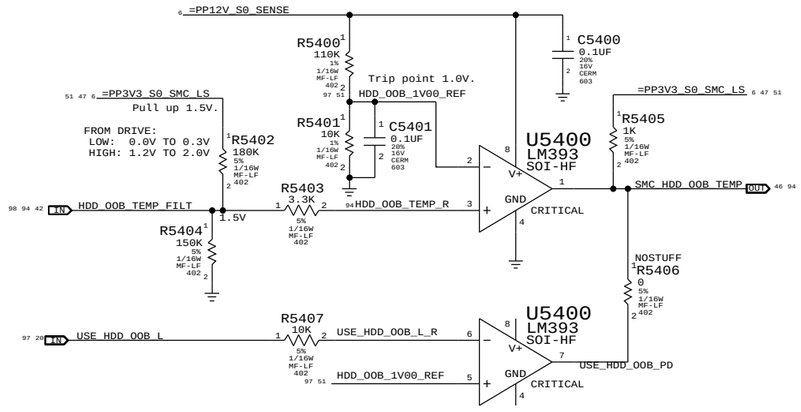
HDD OOB TEMPERATURE SENSING



DRIVE ACTIVE = VALID SIGNAL PROTOCOL BETWEEN 0-2.0V.
DRIVE ASLEEP = HDD DRIVES HDD_OOB_TEMP LOW
DRIVE ABSENT = OOB IS PULLED HIGH UNLESS PCH DETERMINES SSD PRESENT AND DRIVES USE_HDD_OOB_L LOW WHICH THEN PULLS HDD_OOB_TEMP LOW.

NOTE: WILL BE CONNECTED TO SATA PWR CONNECTOR PIN 11
THIS PIN IS ORIGINALLY INTENDED FOR HDD LED OUTPUT,
AND ALSO FOR HDD STAGGERED PIN UP (FLOATING) OR IMMEDIATE SPIN-UP (GROUND).
BOTH FUNCTIONS NOT USED.

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
HDD OOB SENSE

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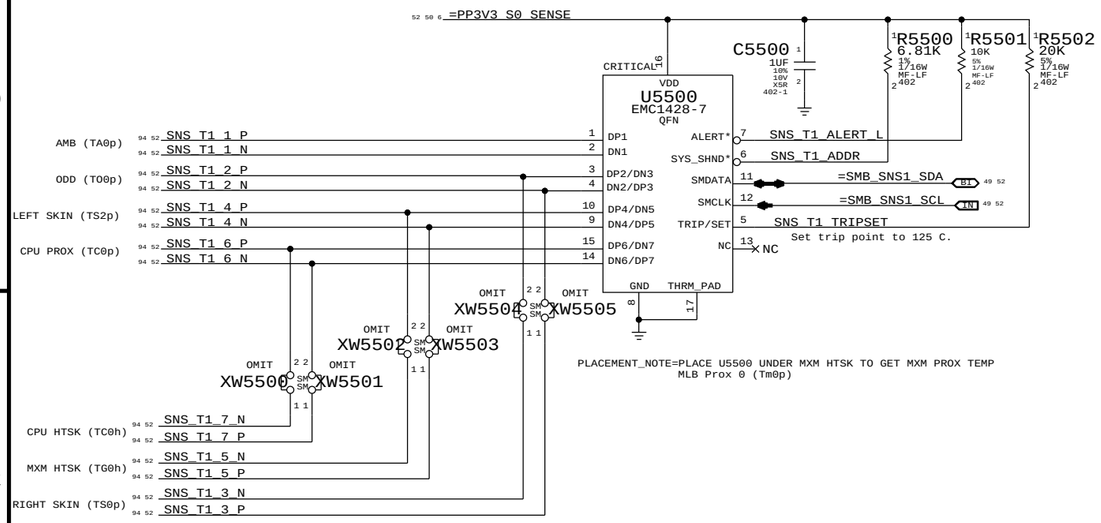
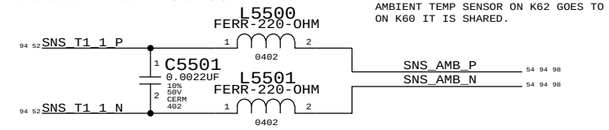
SNS T1: PRODUCTION TEMP SENSOR IC



PLACEMENT_NOTE=PLACE U5500 UNDER MXM HTSK TO GET MXM PROX TEMP
MLB Prox 0 (Tm0p)

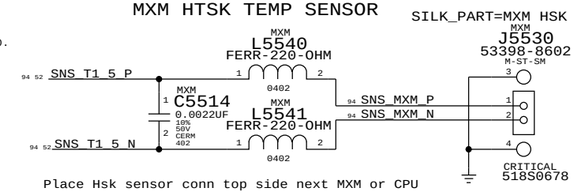
EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

AMBIENT TEMP SENSOR



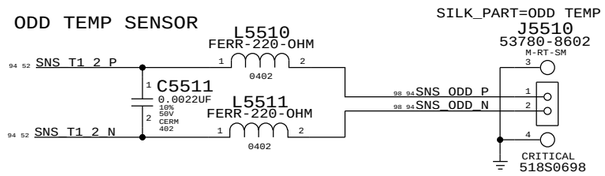
AMBIENT TEMP SENSOR ON K62 GOES TO J5500.
ON K60 IT IS SHARED.

MXM HTSK TEMP SENSOR

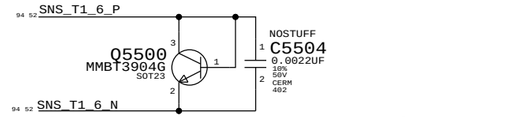


Place Hsk sensor conn top side next MXM or CPU

ODD TEMP SENSOR

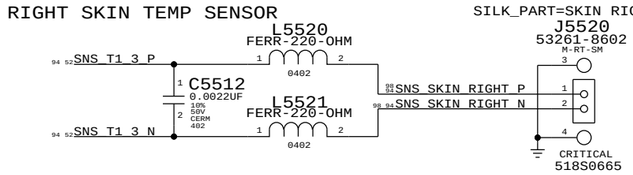


CPU PROXIMITY TEMP SENSOR

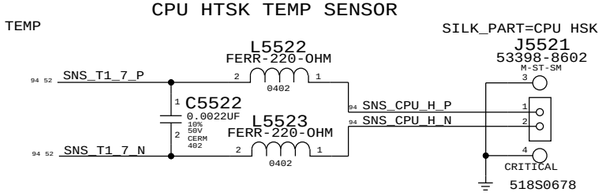


Place Q5500 (CPU Proximity Sensor) at the solder side
at edge near backer plate of CPU to replace HeatSink Temp Sensor

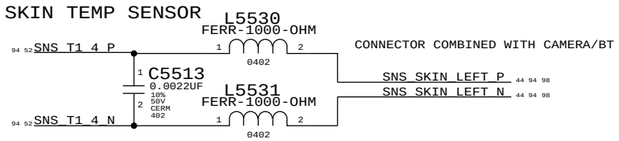
RIGHT SKIN TEMP SENSOR



CPU HTSK TEMP SENSOR

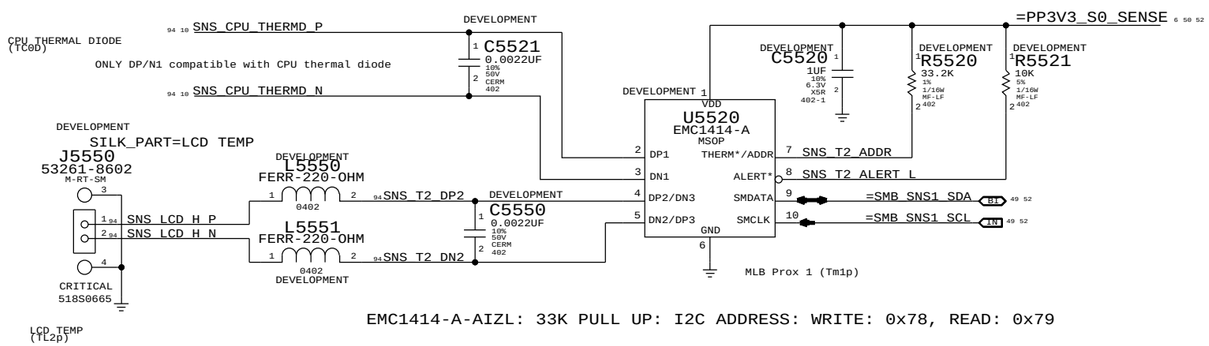


LEFT SKIN TEMP SENSOR



THIS PAGE DIFFERENT BETWEEN K60 AND K62.

SNS T2: DEVELOPMENT TEMP SENSOR IC



EMC1414-A-AIZL: 33K PULL UP: I2C ADDRESS: WRITE: 0x78, READ: 0x79

SYNC_MASTER=K60_MARK SYNC_DATE=01/06/2011

PAGE TITLE: TEMP SENSORS

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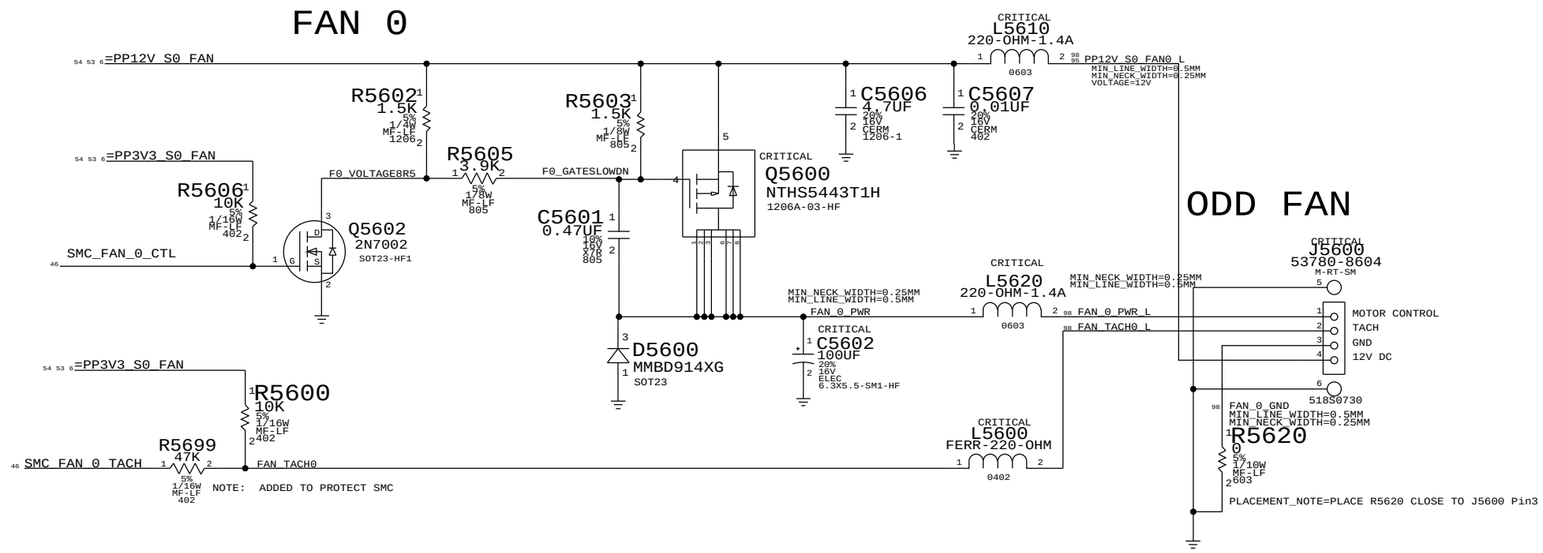
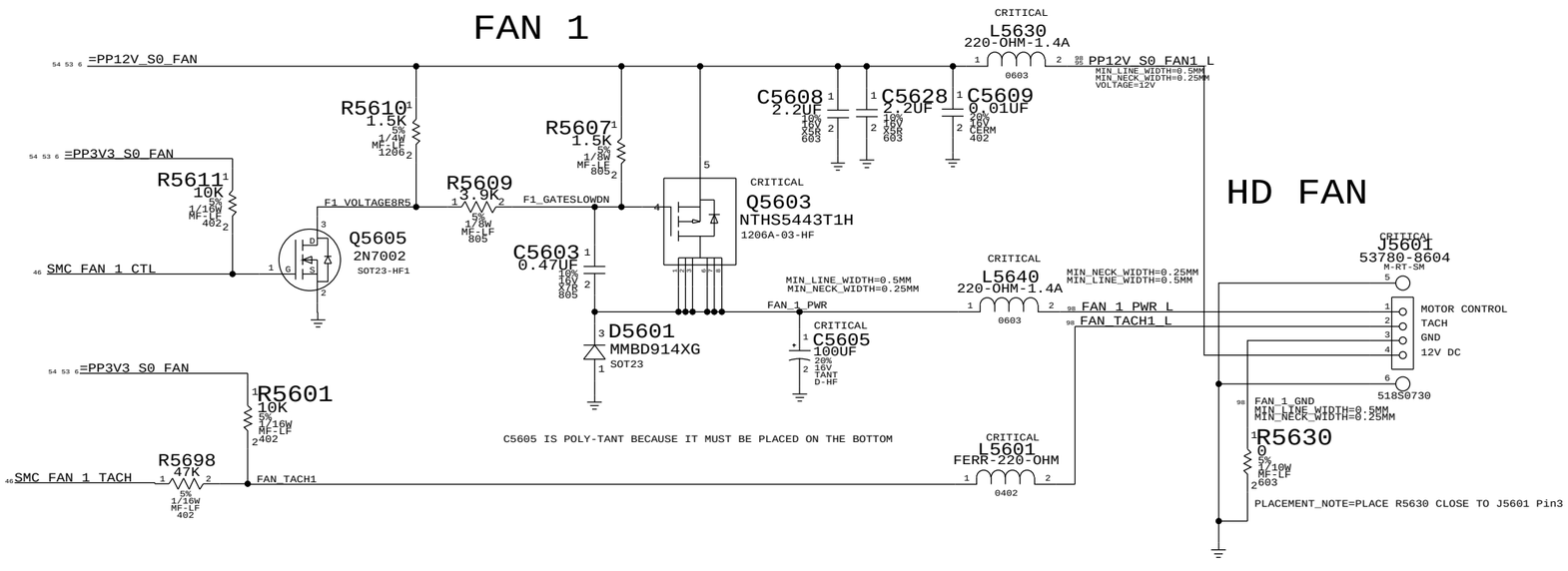
FAN 0



FAN 1



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: HD AND OD FAN

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DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

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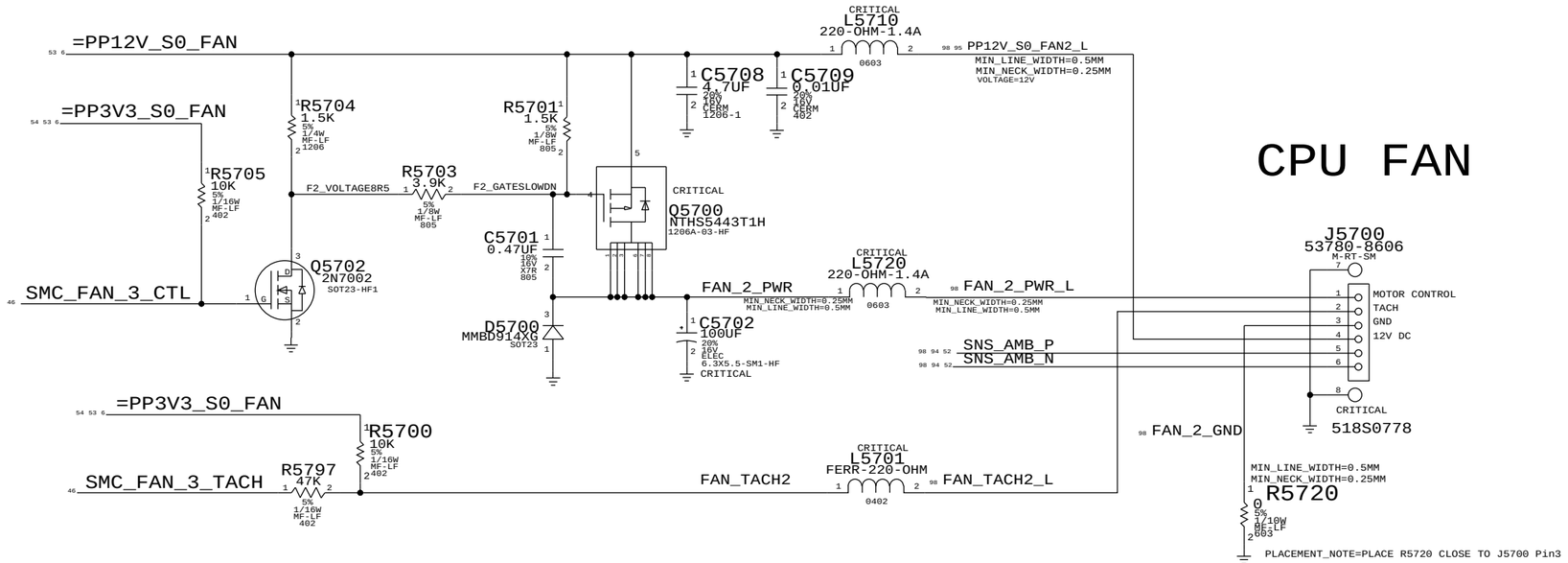
SMC’S FAN3 OUTPUT CONTROL FAN 2



CPU FAN

FAN 3 SMC CONTROL (UNUSED)

SYNC_MASTER=K60_JERRY SYNC_DATE=01/06/2011

PAGE TITLE: CPU FAN

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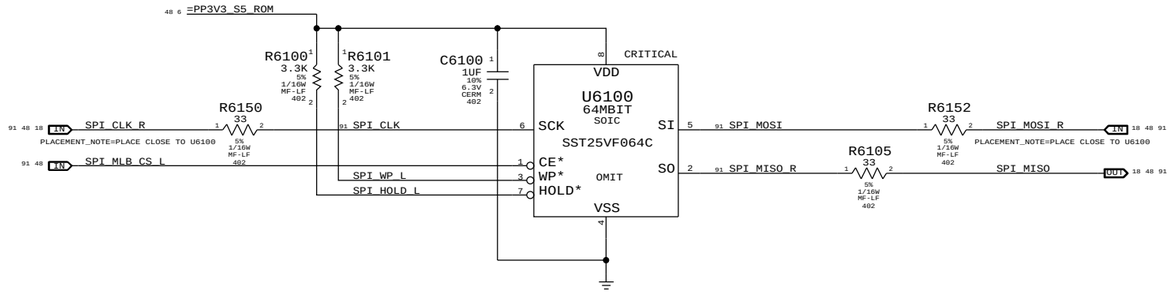

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

SPI ROM

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AUDIO CODEC

APPLE P/N 353S2592

PLACE C6200 AS CLOSE TO PIN 9 AS POSSIBLE

VD MUST BE LESS THAN OR EQUAL TO VL_HD

=PP1V5_S0_AUD_DIG

C6201 4.7UF 20% 4V X5R-1 402

C6200 0.47UF 10% 10V X5R 402

C6208 10UF 20% 10V POLY-TANT CASE-B2-SM

C6202 0.47UF 10% 10V X5R 402

C6203 10UF 20% 10V POLY-TANT CASE-B2-SM

C6205 1UF 10% 10V X5M 402-1

C6204 0.47UF 10% 10V X5M 402

C6206 0.47UF 10% 10V X5R 402

CRITICAL C6207 10UF 20% 6.3V CERM-X5R 0402-1

PP5V_AUDIO_HPAMP

=PP3V3_S0_AUDIO

PP4V5_AUDIO_ANALOG

GND_AUDIO_HPAMP

GND_AUDIO_CODEC

GND_AUDIO_HPAMP

PP4V5_AUDIO_ANALOG

R6200 2.67K 1% 1/16W MF-LF 402

C6209 2.2UF 20% 6.3V CERM 402-LF

C6210 2.2UF 20% 6.3V CERM 402-LF

VBIAS_DAC

CS4206_FP

CS4206_FN

CRITICAL U6201 CS4206B QFN

29	VBIAS_DAC					
44	VHP_FILT+	HPOUT_L	38	MIN_LINE_WIDTH=0.1MM	MIN_NECK_WIDTH=0.1MM	AUD_HP_L_P
41	VHP_FILT-	HPOUT_R	40	MIN_LINE_WIDTH=0.1MM	MIN_NECK_WIDTH=0.1MM	AUD_HP_R_P
		HPREF	39	MIN_LINE_WIDTH=0.2MM	MIN_NECK_WIDTH=0.1MM	AUD_HP_PORT_REF

TWEETERS

R6205 0 5% 1/16W MF-LF 402

XW6200 AUD_HP_L_N

XW6201 AUD_HP_R_N

HP AMP/LINE OUT

PLACE XWS 6200 & 6201 NEAR PINS 38 & 40

2	GPIO0/DMIC_SDA1	LINEOUT_L1+	35	AUD_LO1_L_P	
12	GPIO1/DMIC_SDA2	LINEOUT_L1-	34	AUD_LO1_L_N	
14	GPIO2/SPDIF_OUT2	LINEOUT_R1+	36	AUD_LO1_R_P	
15	GPIO3	LINEOUT_R1-	37	AUD_LO1_R_N	
13	SENSE_A	LINEOUT_L2+	31	AUD_LO2_L_P	
		LINEOUT_L2-	30	TP_AUD_LO2_N_L	NC
		LINEOUT_R2+	32	AUD_LO2_R_P	
		LINEOUT_R2-	33	TP_AUD_LO2_N_R	NC

WOOFERS

XW6202 AUD_LO2_L_N

XW6203 AUD_LO2_R_N

GND_AUDIO_CODEC

PLACE XWS 6202 & 6203 NEAR PINS 35 & 36

NC TP_AUD_DMIC_SDA1

NC TP_AUD_GPIO_1

HP AMP SPEAKERS AUD_GPIO_2

AUD_GPIO_3

AUD_SENSE_A

CS4206_FLYP

CS4206_FLYC

C6211 2.2UF 20% 6.3V CERM 402-LF

C6212 2.2UF 20% 6.3V CERM 402-LF

CS4206_FLYN

MICBIAS	16			AUD_CODEC_MICBIAS	
VCOM	28	CS4206_VCOM	MIN_LINE_WIDTH=0.20MM	MIN_NECK_WIDTH=0.15MM	

PLACE TP FOR ALL HDA SIGNALS NEAR CODEC

6	BITCLK	LINEIN_L+	21	AUD_LI_P_L	
10	SYNC	LINEIN_C-	22	AUD_LI_COM	
8	SDI	LINEIN_R+	23	AUD_LI_P_R	
5	SDO	MICIN_L+	18	AUD_MIC_INP_L	
11	RESET*	MICIN_L-	17	AUD_MIC_INN_L	
47	SPDIF_IN	MICIN_R+	19	AUD_MIC_INR_P	
48	SPDIF_OUT	MICIN_R-	20	AUD_MIC_INR_N	
		VREF+_ADC	27	CS4206_VREF_ADC	NC
		DMIC_SCL	4	TP_CS4206_DMIC_SCL	NC

HDA_BIT_CLK

HDA_SYNC

HDA_SDIN0

HDA_SDOUT

HDA_RST_L

AUD_SPDIF_IN_CODEC

AUD_SPDIF_OUT

R6201 22 5% 1/16W MF-LF 402

AUD_SDI_R

R6202 22 5% 1/16W MF-LF 402

AUD_SPDIF_CHIP

R6203 100K 1% 1/16W MF-LF 402

DGND THRM_PAD AGND

MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

CRITICAL C6213 1UF 10% 25V TANT CASE-P3-MF

CRITICAL C6214 10UF 20% 10V POLY-TANT CASE-B2-SM

GND_AUDIO_HPAMP

GND_AUDIO_CODEC

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S2592	353S3199		U6201	CS4206A

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

=PP5V_S0_AUDIO

L6210 FERR-220-OHM 0402

VR6201 TPS71745 SON CRITICAL

4V5_REG_IN

4V5_REG_EN

4V5_OUT

4V5_NR

R6213 0 5% 1/16W MF-LF 603

PP4V5_AUDIO_ANALOG

MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.28MM VOLTAGE=4.5V

MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM

R6220 0 5% 1/16W MF-LF 402

NOSTUFF C6221 1UF 10% 10V X5R 402-1

C6222 1UF 10% 10V X5R 402-1

C6223 0.1UF 10% 16V X7R-CERM 402

C6224 1UF 10% 10V X5R 402-1

NOSTUFF R6212 0 5% 1/16W MF-LF 402

R6210 0 5% 1/16W MF-LF 603

XW6211

GND_AUDIO_HPAMP MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM VOLTAGE=0V

GND_AUDIO_CODEC MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

XW6212

PP5V_AUDIO_HPAMP

NOSTUFF L6212 FERR-220-OHM 0402

PP5V_LAMP_VREG

MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.28MM VOLTAGE=4.5V

VOLTAGE=4.5V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.4MM

ISOLATED 5 V POWER SUPPLY FOR HP AMP

APN 152S1314

=PP5V_S0_AUDIO

C6250 10UF 20% 10V X5R 603

CRITICAL Q6250 DMMT3906W-7-F SOT-363

NOSTUFF R6258 1K 1% 1/16W MF-LF 402

CRITICAL C6256 1UF 10% 25V X5R 402

R6255 1.0K 1% 1/10W MF-LF 603

SC4503_SW

SC4503_SW_SNBR MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM

CRITICAL T6250 1.8UH-1.6A-243MOHM LPD3015-SM

AUD_XFRMR_SEC MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM

D6252 DO222-SM STPS1L30MF

PP5V_AUDIO_ISO MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V

CRITICAL C6258 150UF-.025-OHM 6.3V TANT CASE-B2-SM

APN 128S0271

C6259 10UF 20% 10V X5R 603

R6257 4.99K 1% 1/10W MF-LF 603

GND_AUDIO_ISO MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

SC4503_FB_DDROP

C6257 0.1UF 10% 16V X7R-CERM 402

R6256 49.9K 1% 1/16W MF-LF 402

D6250 SOD-523 BAT54XV2T1

R6254 20 1% 1/16W MF-LF 603

R6260 10 1% 1/16W MF-LF 603

GND_AUDIO_ISO

APN 353S3080

SOT-363 DMMT3906W-7-F Q6250 CRITICAL

SC4503_FB_RDIV

SC4503_FB_PNP

SC4503_FB_FILT

D6251 SOD-523 BAT54XV2T1

SC4503_SW_D

R6253 43.2K 1% 1/16W MF-LF 402

C6254 0.01UF 10% 16V CERM 402

NOSTUFF C6261 0.001UF 10% 50V X7R 402

NOSTUFF R6259 100K 1% 1/16W MF-LF 402

C6255 0.001UF 10% 50V X7R 402

R6250 40.2K 1% 1/16W MF-LF 402

R6251 3.40K 1% 1/16W MF-LF 402

R6252 12.4K 1% 1/16W MF-LF 402

U6250 SC4503 TSOT-23 SYM VER 2 CRITICAL

SC4503_SHDN

SC4503_FB

C6252 0.1UF 10% 16V X7R-CERM 402

C6251 0.1UF 10% 16V X7R-CERM 402

NOSTUFF C6253 1UF 10% 10V X5R 402-1

SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE: AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

BRANCH

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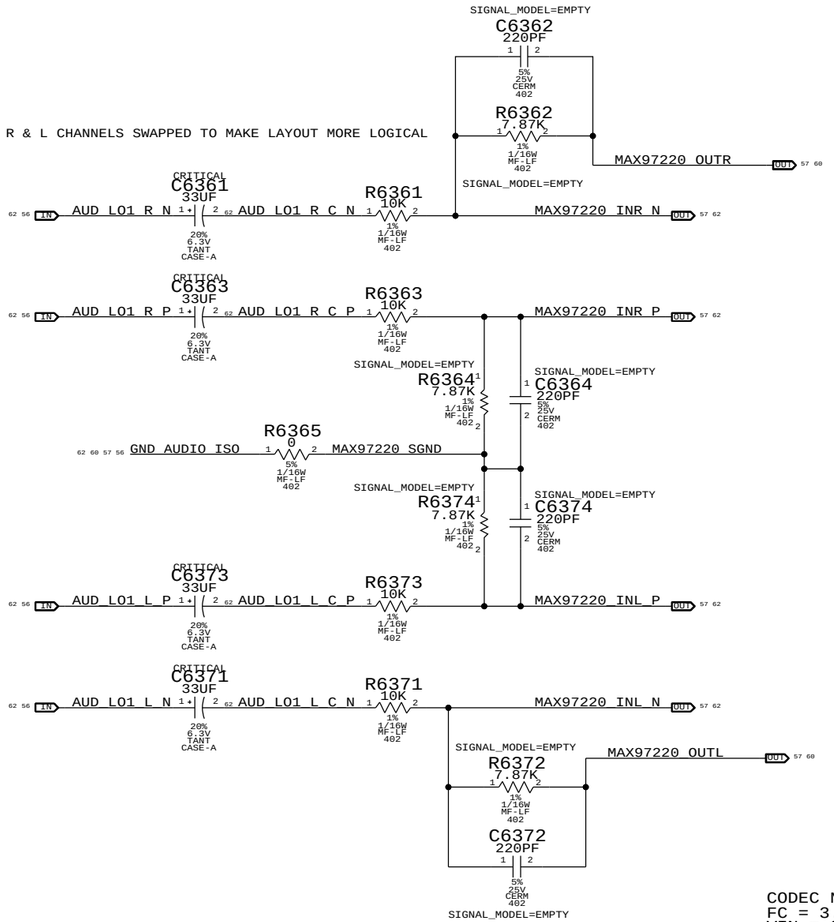
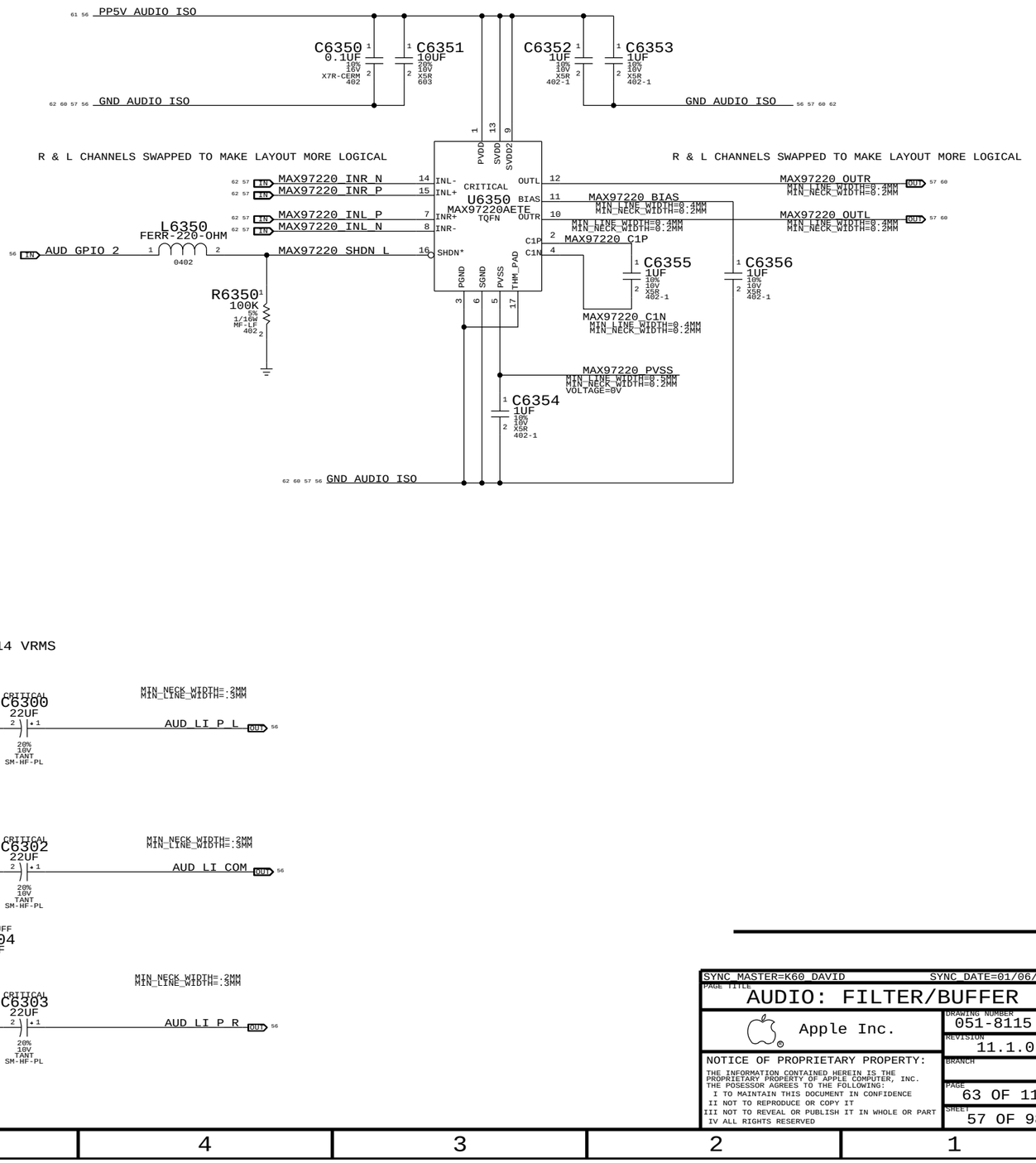
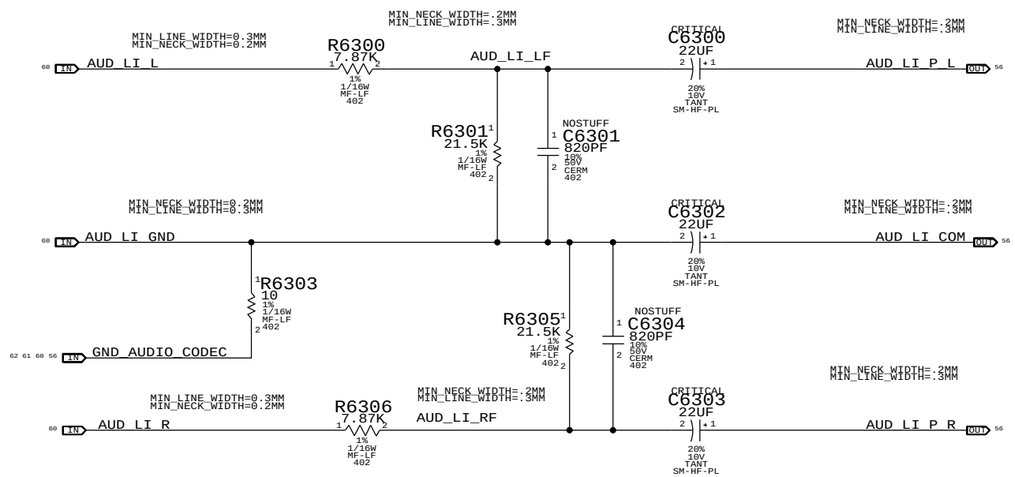




CODEC Nom SE RIN = 20K OHMS
FC = 3.62 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



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SYNC_DATE=01/06/2011

PAGE TITLE
AUDIO: FILTER/BUFFER

Apple Inc.

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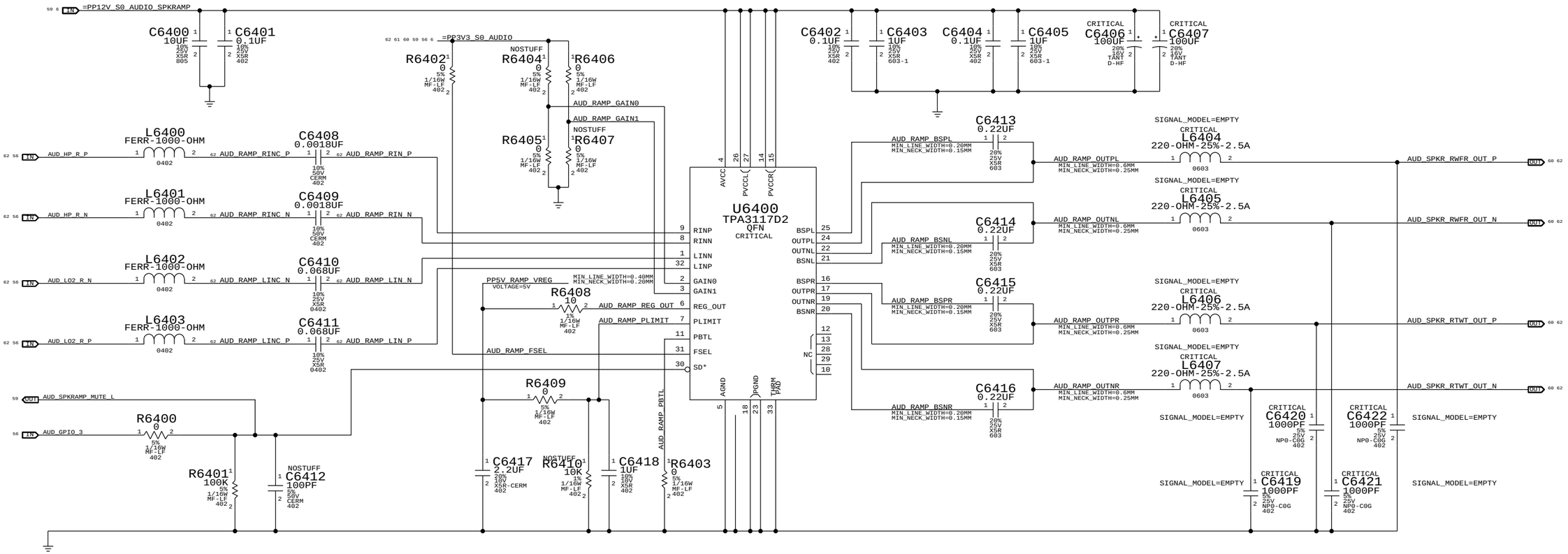
RIGHT CH SPEAKER AMP
APPLE P/N 353S3069

R6402 = HIGH = 400 KHZ
SPEAKER AMP GAIN = +15.2 DB
SPEAKER AMP RIN = 104K NOMINAL W/ +15.2 DB GAIN
FC_HPF, TWEETERS = ~850 HZ (0.0018 UF)
FC_HPF, WOOFERS = ~22.5 HZ (0.068 UF)



SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE
AUDIO: SPEAKER AMP_1

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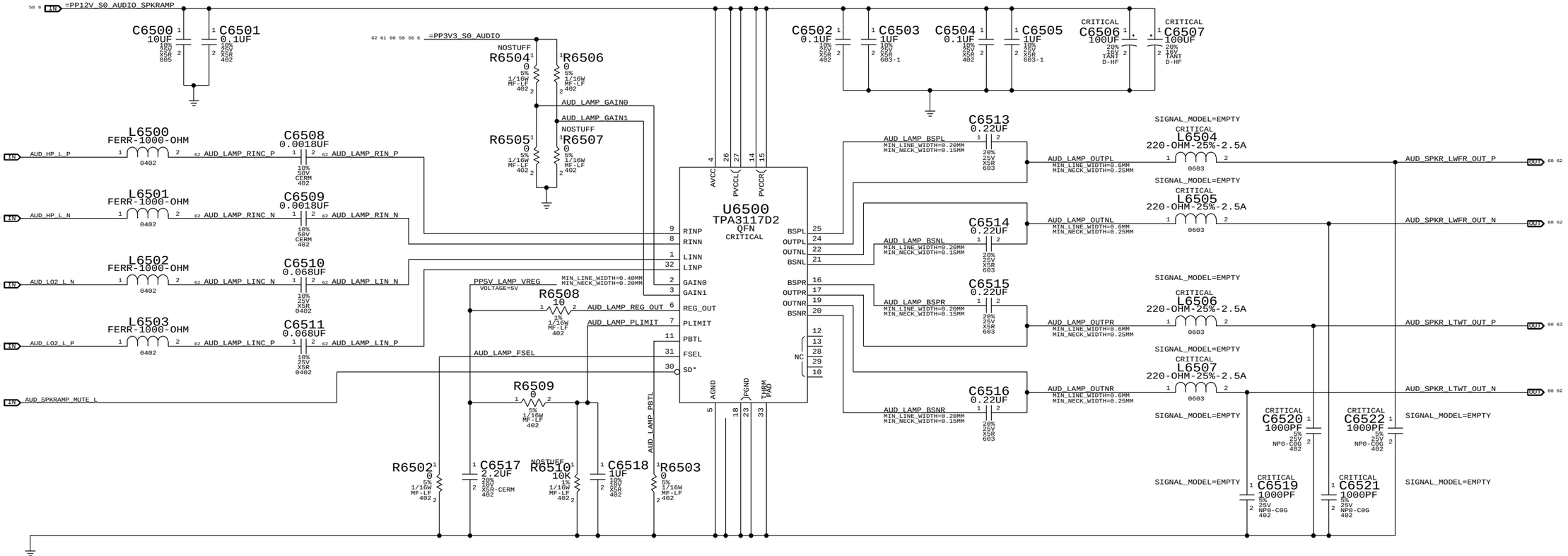
LEFT CH SPEAKER AMP
APPLE P/N 353S3069

R6502 = LOW = 300 KHZ
SPEAKER AMP GAIN = +15.2 DB
SPEAKER AMP RIN = 104K NOMINAL W/ +15.2 DB GAIN
FC_HPF, TWEETERS = ~850 HZ (0.0018 UF)
FC_HPF, WOOFERS = ~22.5 HZ (0.068 UF)



SYNC_MASTER=K60_DAVID	SYNC_DATE=01/06/2011
PAGE TITLE	AUDIO: SPEAKER AMP
Apple Inc.	DRAWING NUMBER 051-8115 · SIZE D
	REVISION 11.1.0
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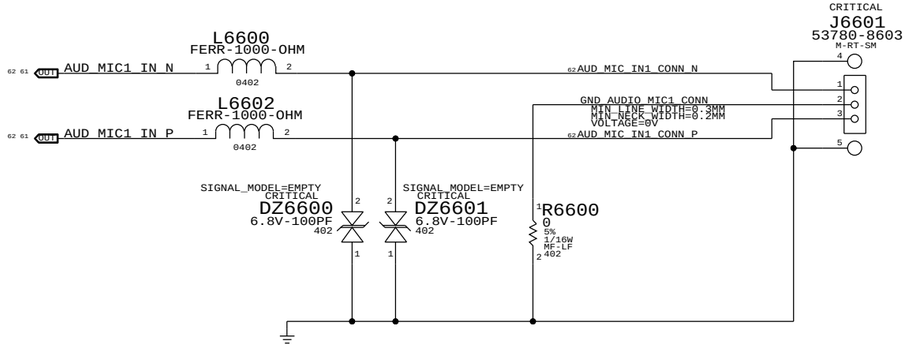
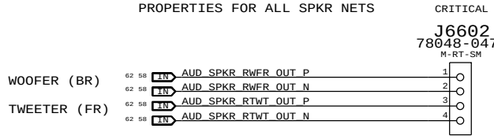
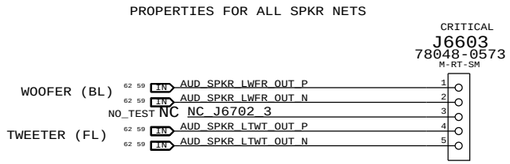
INTERNAL MIC CON
APPLE P/N 518S0677

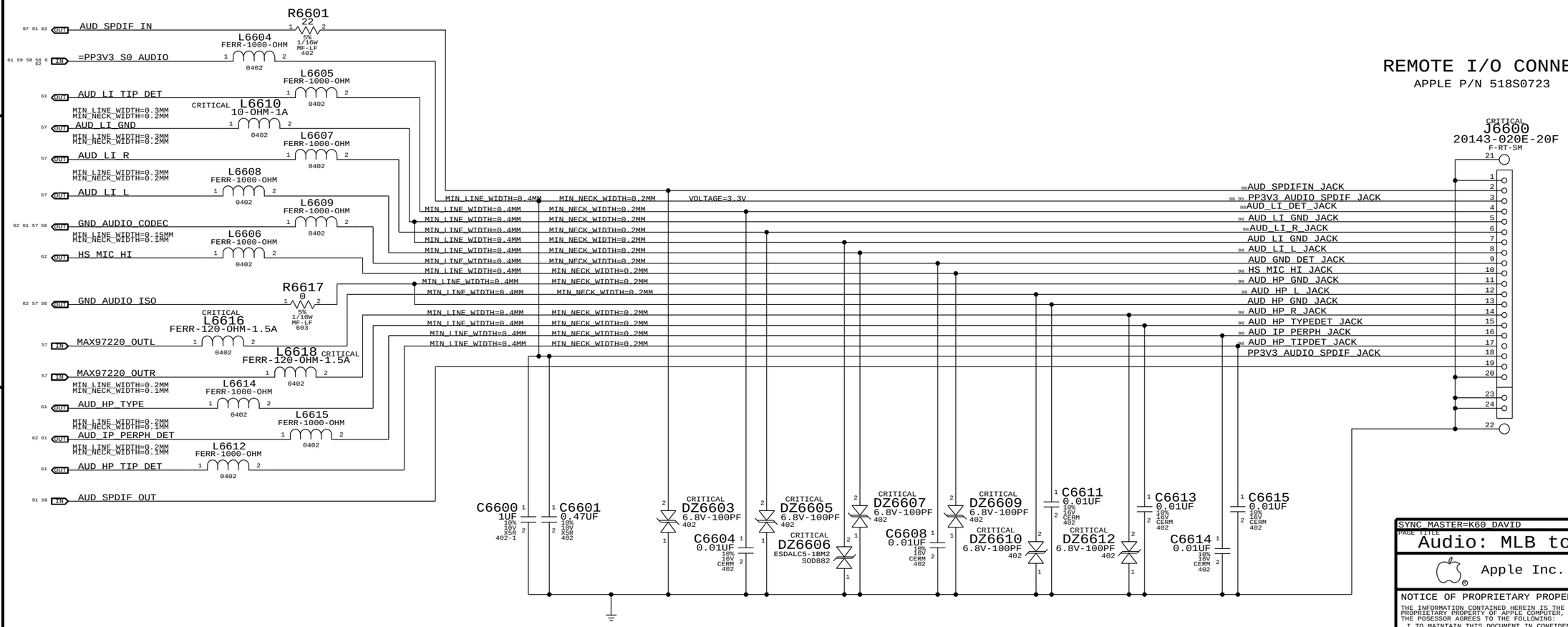


SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656





REMOTE I/O CONNECTOR
APPLE P/N 518S0723



SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE
Audio: MLB to I/O Conn.

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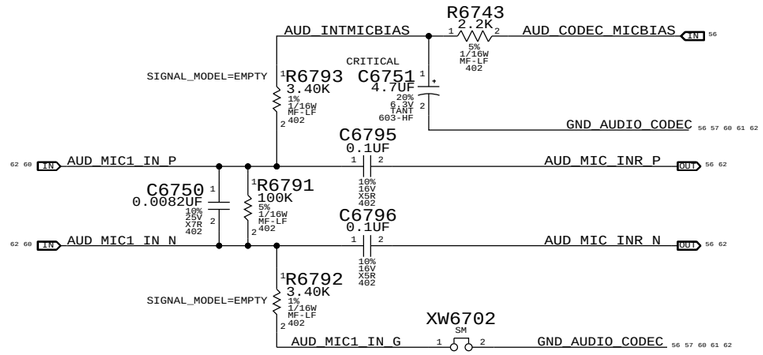
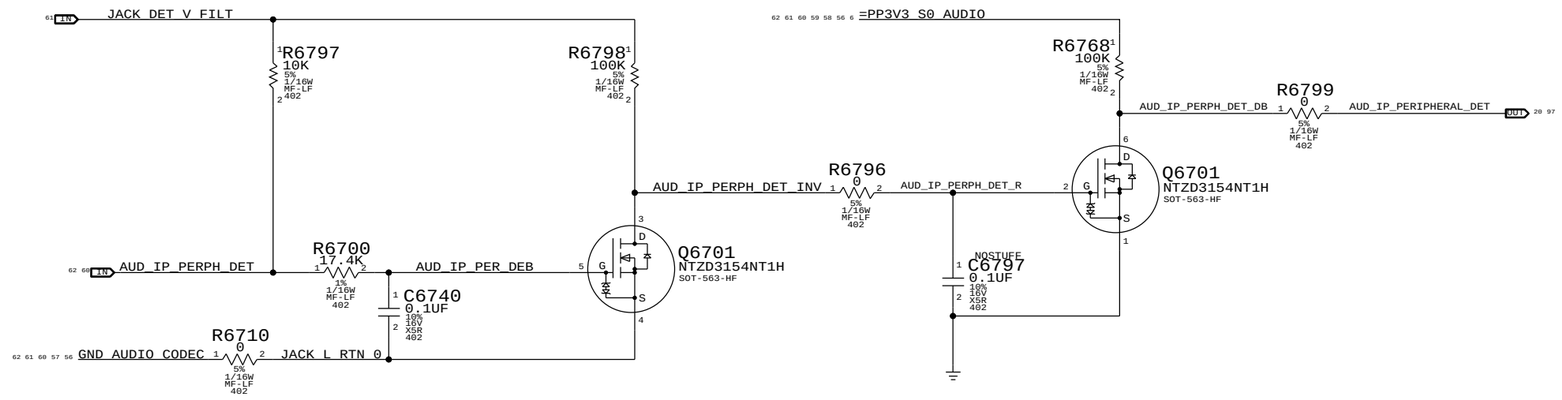
Internal Microphone Impedance Matching



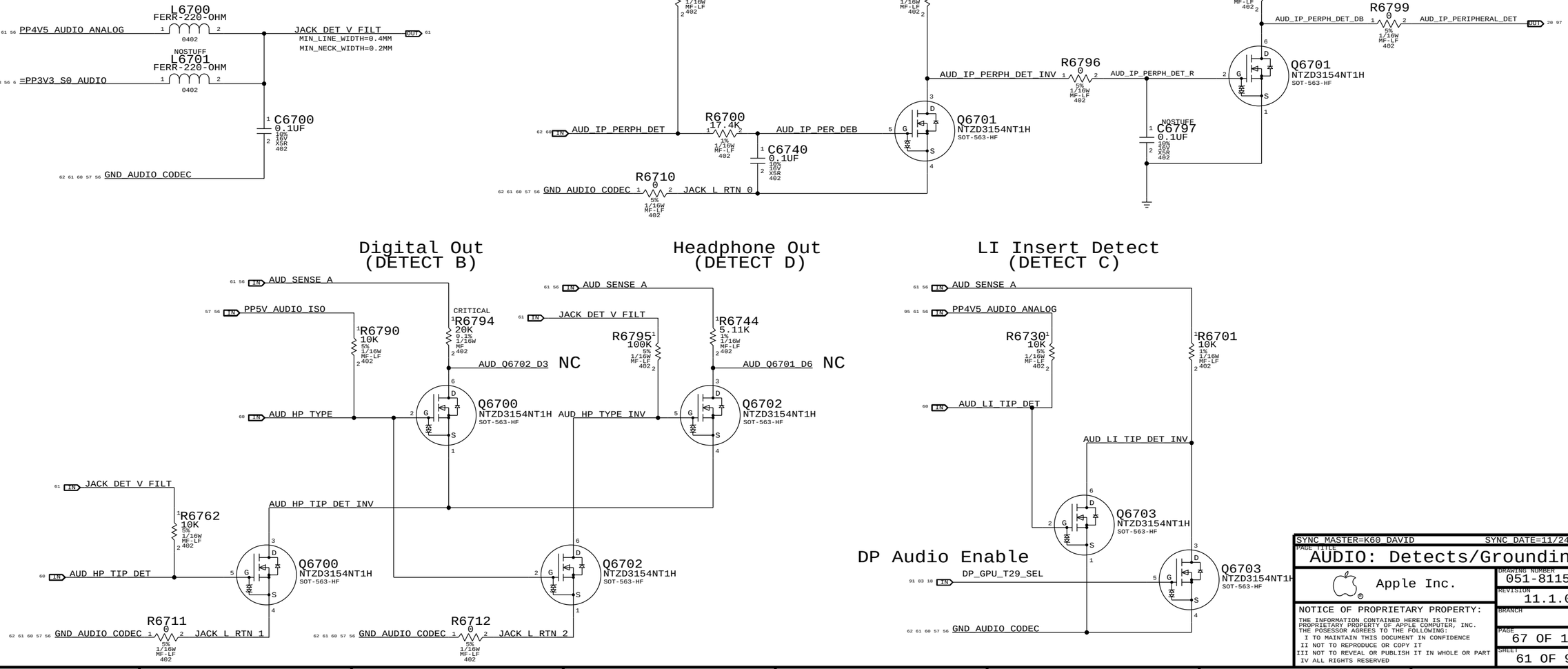
IPHS HS Detect Debounce CKT



Digital Out (DETECT B)

Headphone Out (DETECT D)

LI Insert Detect (DETECT C)



SYNC_MASTER=K60_DAVID SYNC_DATE=11/24/2010

PAGE TITLE
AUDIO: Detects/Grounding

Apple Inc.

DRAWING NUMBER	051-8115
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	0X0A (D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X02 (2)	0X02 (2)	0X09 (09)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0x0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0E (14,LEFT & RIGHT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	COUGAR POINT GPIO 16	COUGAR POINT GPIO 5 (PCVR_INT) COUGAR POINT GPIO 3 (PERIPH_DET)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

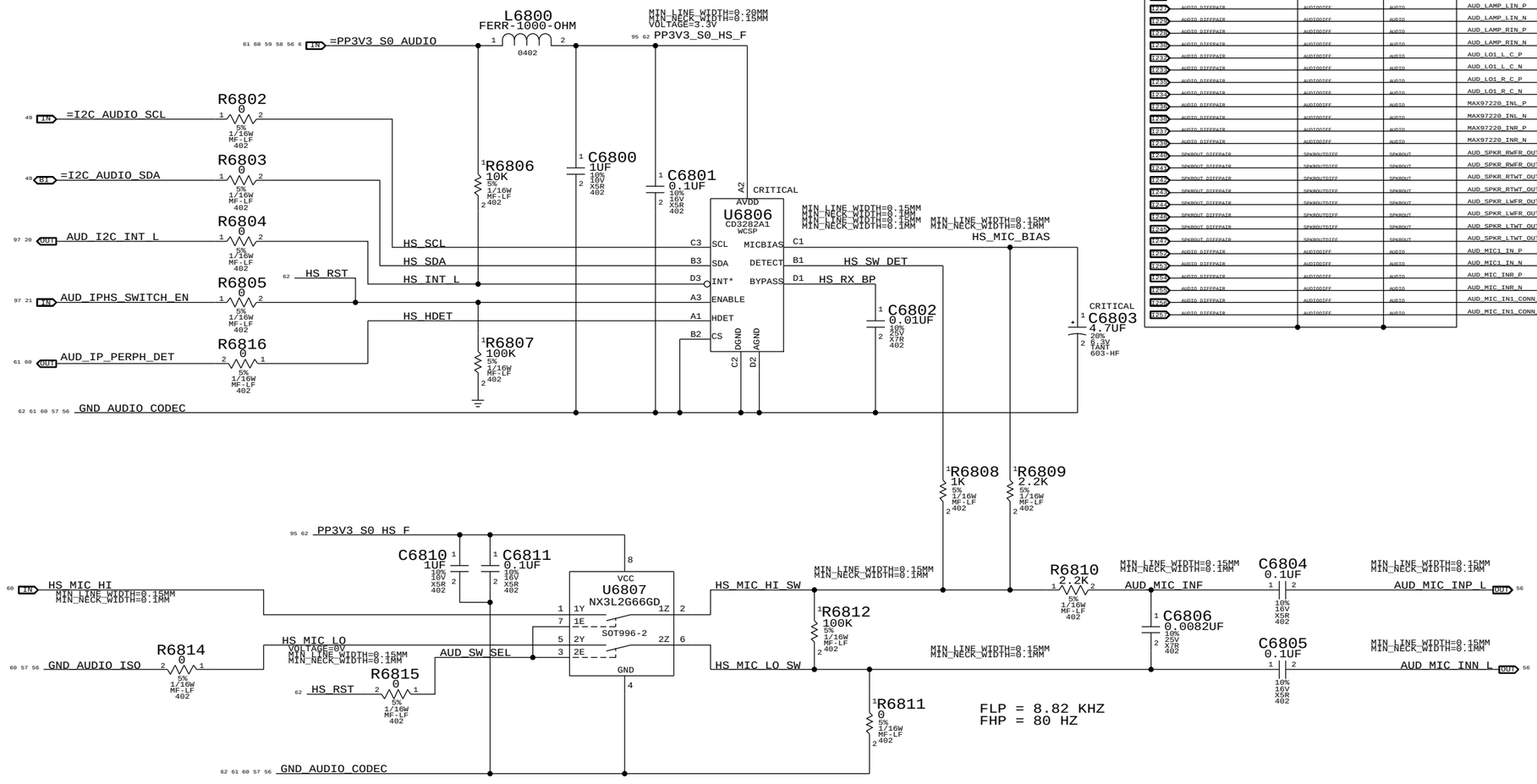
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_L_P	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_L_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_R_P	56 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_R_N	56 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	56 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	56 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	56 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	56 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	58 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	58 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	58 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	58 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	59 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	59 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	59 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	59 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC1_IN_P	60 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC1_IN_N	60 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_P	56 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_N	56 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_IN1_CONN_P	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_IN1_CONN_N	60

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2640



SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE

AUDIO: Mikey

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DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

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SLP_S4 ENABLES

MEMVTT_EN SEQUENCE

=PP3V3_S0_PWRCTL
R6951 10K 5% 1/16W MF-LF 402
R6952 10K 5% 1/16W MF-LF 402
NOSTUFF C6951 100PF 5% 50V CERM 402
PM_EN_DDRVTT_S0_REG 32 63 71 97
NOSTUFF C6953 0.1UF 10% 10V X5R 402
VTT_REG_PGOOD_L
Q6911 MMDT3904-X-G SOT-363-LF
R6950 10K 5% 1/16W MF-LF 402
64 63 PM_PGOOD_P1V05_S0_REG
97 68
CPUVTT_REG_PGOOD_R 97
Q6911 SOT-363-LF
MMDT3904-X-G
NOSTUFF C6952 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S5_PWRCTL
97 47 46 19 5 PM_SLP_S5_L
R6971 0 5% 1/16W MF-LF 402
NOSTUFF
R6972 0 5% 1/16W MF-LF 402
97 63 47 46 32 19 5 PM_SLP_S4_L
97 PM_SLP_S4_1_L_R
74LVC08 TSSOP-HF U6900 08
C6910 0.1UF 20% 10V CERM 402
S4_ENABLES 97
R6911 33 5% 1/16W MF-LF 402
R6912 33 5% 1/16W MF-LF 402
PM_EN_P3V3_S3_FET 73 97
Enable FET
PM_EN_P5V_S3_REG 70 97
ENABLE REGULATOR

=PP3V3_S5_PWRCTL
R6916 100K 5% 1/16W MF-LF 402
R6915 10K 5% 1/16W MF-LF 402
CPU_SKTOCC 91
97 11 CPU_SKTOCC_L
Q6910 2N7002 SOT23-HF1
NOSTUFF R6917 10K 5% 1/16W MF-LF 402
PLACE TOP SIDE
REWORK TO POWER UP WITH NO CPU

NOSTUFF C6920 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6921 0.47UF 10% 6.3V CERM-X5R 402

97 82 70 63 PM_PGOOD_P5V_S3_REG
R6970 0 5% 1/16W MF-LF 402
PM_EN_USB_PWR 43 91
NOSTUFF C6924 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S5_PWRCTL
97 63 47 46 32 19 5 PM_SLP_S4_L
74LVC08 TSSOP-HF U6900 08
PM_EN_DDR1V5_S3_REG 71 97
97 82 70 63 PM_PGOOD_P5V_S3_REG

NOSTUFF R6931 33 5% 1/16W MF-LF 402
97 73 64 63 PM_PGOOD_P3V3_S0_FET
PM_EN_P1V5_S0_FET 63 73 97

SLP_S3 ENABLES

=PP3V3_S5_PWRCTL
R6955 10K 5% 1/16W MF-LF 402
P3V3_S5_PWRCTL_U6900_R
97 64 PGOOD_P12V_S0
74LVC08 TSSOP-HF U6900 08

=PP3V3_S5_PWRCTL
97 82 47 46 36 32 26 19 5 PM_SLP_S3_L
97 71 5 PM_PGOOD_DDR1V5_S3_REG
74LVC08 TSSOP-HF U6900 08
PM_EN_P12V_S0_FET 6 97

NOSTUFF R6946 33 5% 1/16W MF-LF 402
PM_EN_P3V3_S0_FET
Enable FET
OUT 63 73 97
NOSTUFF R6947 33 5% 1/16W MF-LF 402
PM_EN_P5V_S0_FET
Enable FET
OUT 73 97

OTHER RAILS ENABLED BY P3V3_S0 AND P5V_S0:
PP1V8_S0 VREG (CPU PLL)

NOSTUFF R6944 33 5% 1/16W MF-LF 402
NOSTUFF R6941 10K 5% 1/16W MF-LF 402
PM_SLP_S3_BUF_L 97
Enable FET
PM_EN_P1V5_S0_FET 63 73 97
PM_EN_DDRVTT_S0_REG 32 63 71 97
Enable regulator

=PP12V_S0_PWRCTL 6 64 80
R6934 82K 5% 1/16W MF-LF 402
PM_PGOOD_P5V_S0_FET 63 64 73 97
R6935 33K 5% 1/16W MF-LF 402

OPTION TO DELAY 1V8
97 73 64 63 PM_PGOOD_P3V3_S0_FET
R6932 33 5% 1/16W MF-LF 402
NOSTUFF R6990 33 5% 1/16W MF-LF 402
97 73 64 63 PM_PGOOD_P5V_S0_FET
PM_EN_P1V8_S0_REG 71 97
NOSTUFF C6994 0.47UF 10% 6.3V CERM-X5R 402

NOSTUFF C6947 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6944 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6941 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6945 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6946 0.47UF 10% 6.3V CERM-X5R 402

OPTIONAL SEQUENCE TO DELAY 3V,1V5
97 73 64 63 PM_PGOOD_P5V_S0_FET
R6930 33 5% 1/16W MF-LF 402
PM_EN_P3V3_S0_FET 63 73 97
97 73 64 63 PM_PGOOD_P5V_S0_FET
R6933 33 5% 1/16W MF-LF 402
PM_EN_P1V5_S0_FET 63 73 97

NOSTUFF R6942 33 5% 1/16W MF-LF 402
Enable regulator
PM_EN_P1V1S_S0_REG
NOSTUFF C6942 1UF 10% 6.3V CERM 402
CPUVTT VREG/ PCH CORE
68 97
97 68 64 63

97 73 64 63 PM_PGOOD_P3V3_S0_FET
R6936 33 5% 1/16W MF-LF 402
OPTION TO DELAY 1V05

NOTE: PM_PGOOD_P1V05_S0_REG ENABLES VCCSA REGULATOR CIRCUIT ON PAGE 70
PM_PGOOD_P1V05_S0_REG = =PM_EN_VCCSA_S0_CPU
MAKE_BASE=TRUE

VCCSA REGULATOR
97 64
PM_PGOOD_PVCCSA_S0_REG = Enable regulator PM_EN_PVCORE_CPU 65 97
MAKE_BASE=TRUE
TO ENABLE OF CPU VCORE

SYNC_MASTER=K62 SYNC_DATE=01/06/2011
PAGE TITLE
POWER SEQUENCING ENABLES

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DRAWING NUMBER 051-8115
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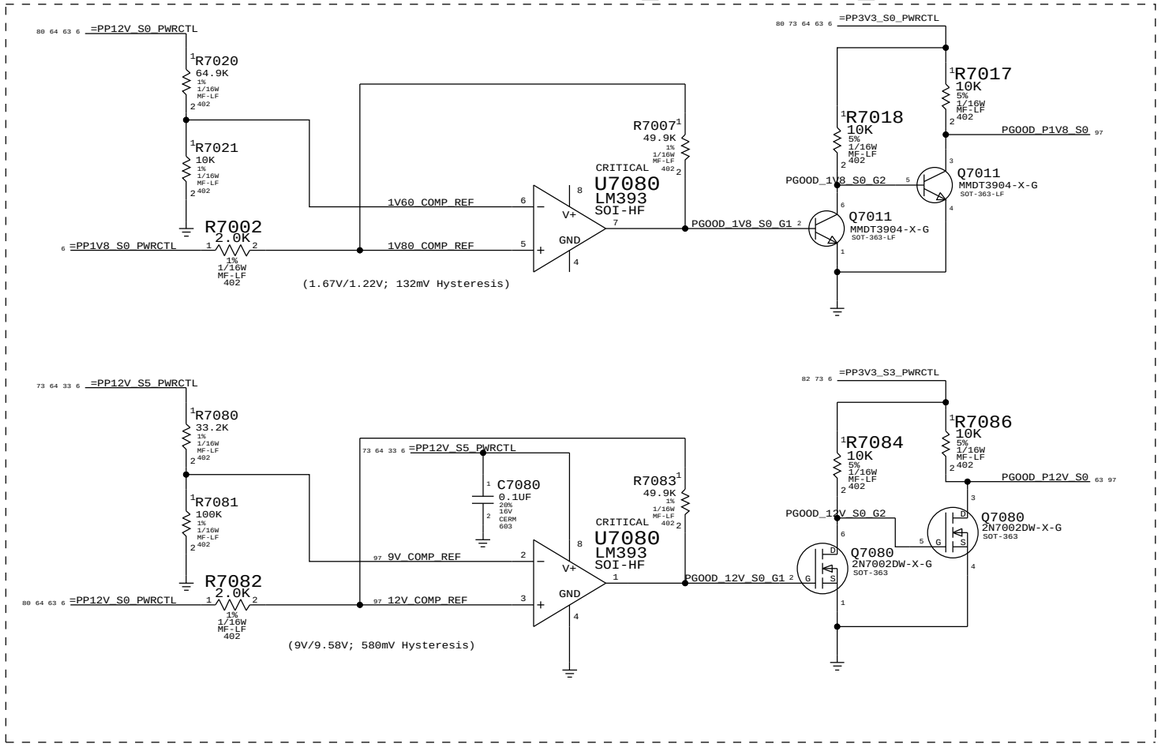
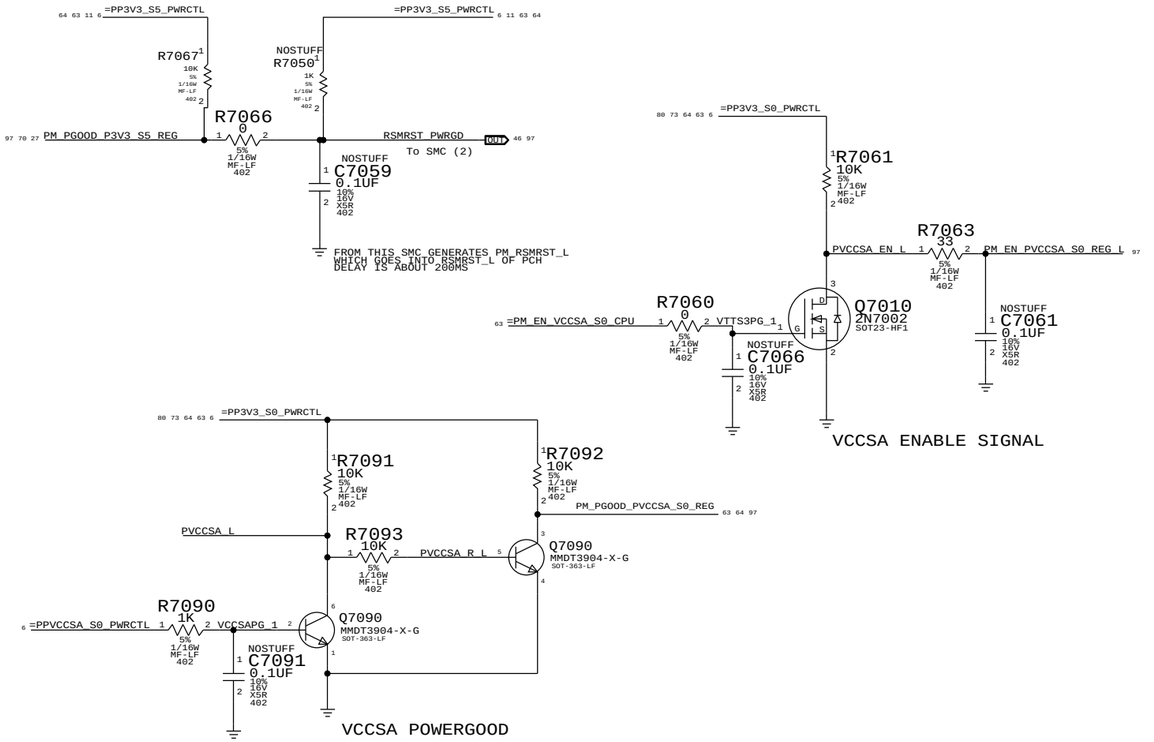
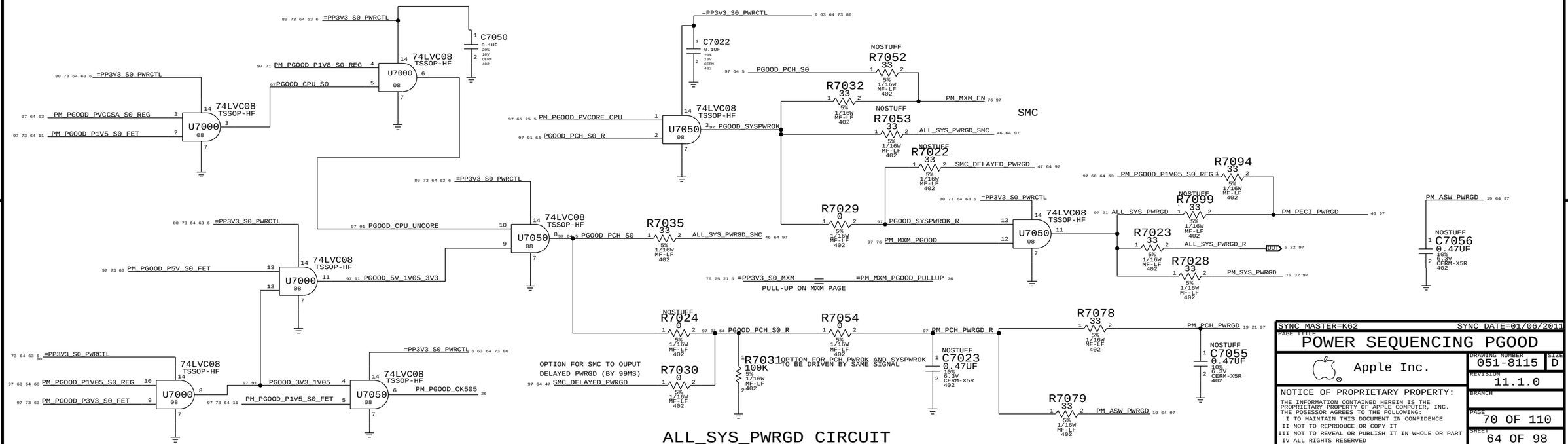
PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0



S0 RAILS PGOOD





ALL_SYS_PWRGD CIRCUIT

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: POWER SEQUENCING PGOOD

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CPU CORE/AXG REG 1.1V/75A O/P= PPVCORE_S0_CPU_REG

=PPVAXG_S0_CPU

CPU_VAXG_SENSE_P

CPU_VAXG_SENSE_N

1.25 mOhm loadline

=PP5V_S0_VRD

=PP3V3_S0_VRD

PP5V_S0_CPU_VCORE_VCC

MAX_NECK_LENGTH=3MM
MIN_NECK_WIDTH=0.3MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=5V

CPU VCORE
VOUT = VCORE
PEAK = 75A
AVG = 55A

U7100
ISL6364
QFN

LOCAL 5V

=PPVCCIO_S0_CPU

=PPVCORE_S0_CPU

=PP12V_S0_VRD

L7100
1UH-20A-4.5MOHM
TH-VERT-HF

CPU CORE INPUT FILTER

PP12V_S0_CPU_FLTRD

SYNC_MASTER=K60_AARON SYNC_DATE=N/A

PAGE TITLE
VREG: PPVCORE_S0_CPU

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PHASE 1

PP12V_S0_CPU_FLTRD
NET_SPACING_TYPE=POWER
CRITICAL C7272 220UF 20% 16V ALUM-POLY 8X7-TH
CRITICAL C7270 220UF 20% 16V ALUM-POLY 8X7-TH
CRITICAL C7271 220UF 20% 16V ALUM-POLY 8X7-TH
R7202 10 5% 1/10W MF-LF 603
R7205 0 5% 1/10W MF-LF 603
NOSTUFF R7201 10 5% 1/10W MF-LF 603
VR_CPU_DRV1_VCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
VR_CPU_DRV1_UVCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
VR_CPU_DRV1_PVCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
C7201 1UF 10% 16V X5R 603
VR_CPU_BOOT1_RC
NET_PHYSICAL_TYPE=VR_CTL_PHY NET_SPACING_TYPE=VR_CONTROL DIDT=TRUE NO_TEST=TRUE
R7204 0 5% 1/10W MF-LF 603
C7203 0.22UF 10% 16V X7R 603
U7201 ISL6622 DFN
VCC UVCC LVCC BOOT GDSEL UGATE PHASE PWM LGATE GND THRML PAD
VR_CPU_DRV1_GDSEL
VR_CPU_DRV1_BOOT NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL NO_TEST=TRUE
VR_CPU_DRV1_UGATE NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_PHASE1 NET_PHYSICAL_TYPE=POWER DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
VR_CPU_DRV1_LGATE NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
C7202 1UF 10% 16V X5R 603
C7200 1UF 10% 16V X5R 603
NOSTUFF R7207 0 5% 1/10W MF-LF 603
VR_CPU_PWM1
376S0772
CRITICAL Q7201 IRF6710 S1
CRITICAL C7205 220UF 20% 16V ALUM-POLY 8X7-TH
CRITICAL C7206 10UF 10% 16V X5R-CERM 0805
CRITICAL C7215 10UF 10% 16V X5R-CERM 0805
C7207 1UF 10% 16V X5R 603
C7281 1UF 10% 16V X5R 603
THESE TWO CAPS ARE FOR EMC
C7210 0.001UF 10% 50V X7R 402
C7211 1UF 10% 16V X5R 402
CRITICAL L7201 0.24UH+/-20%-0.000420HM-40A SDP1108M-TH
SWITCH_NODE=TRUE
CRITICAL R7208 0.0005 1% 1W MF 0612
PPVCORE_S0_CPU_REG
NOSTUFF R7206 2.2 5% 1/8W MF-LF 805
VR_CPU_PH1_SNUB
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
C7208 0.001UF 10% 50V CERM 402 NOSTUFF
376S0771
CRITICAL Q7202 IRF6795 DIRECTFET-MX
VR_CPU_ISNS1_P
VR_CPU_ISNS1_N

PHASE 2

R7222 10 5% 1/10W MF-LF 603
NOSTUFF R7225 0 5% 1/10W MF-LF 603
R7221 10 5% 1/10W MF-LF 603
VR_CPU_DRV2_VCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
VR_CPU_DRV2_UVCC
NET_PHYSICAL_TYPE=POWER
VR_CPU_DRV2_PVCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
C7221 1UF 10% 16V X5R 603
VR_CPU_BOOT2_RC
NET_PHYSICAL_TYPE=VR_CTL_PHY NET_SPACING_TYPE=VR_CONTROL DIDT=TRUE NO_TEST=TRUE
R7224 0 5% 1/10W MF-LF 603
C7223 0.22UF 10% 16V X7R 603
C7222 1UF 10% 16V X5R 603
NOSTUFF C7220 1UF 10% 16V X5R 603
U7221 ISL6612 QFN1
VCC PVCC BOOT PWM UGATE PHASE NC NC LGATE GND THRML PAD
VR_CPU_PWM2
VR_CPU_DRV2_BOOT NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL NO_TEST=TRUE
VR_CPU_DRV2_UGATE NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_PHASE2 NET_PHYSICAL_TYPE=POWER DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
VR_CPU_DRV2_LGATE NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_DRV2_GDSEL
NOSTUFF R7227 0 5% 1/10W MF-LF 603
376S0772
CRITICAL Q7221 IRF6710 S1
CRITICAL C7225 220UF 20% 16V ALUM-POLY 8X7-TH
CRITICAL C7226 10UF 10% 16V X5R-CERM 0805
CRITICAL C7229 10UF 10% 16V X5R-CERM 0805
C7282 1UF 10% 16V X5R 603
C7227 1UF 10% 16V X5R 603
THESE TWO CAPS ARE FOR EMC
C7230 0.001UF 10% 50V X7R 402
C7231 1UF 10% 16V X5R 402
CRITICAL L7221 0.24UH+/-20%-0.000420HM-40A SDP1108M-TH 152-0118
SWITCH_NODE=TRUE
CRITICAL R7228 0.0005 1% 1W MF 0612
PPVCORE_S0_CPU_REG
NOSTUFF R7226 2.2 5% 1/8W MF-LF 805
VR_CPU_PH2_SNUB
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
C7228 0.001UF 10% 50V CERM 402 NOSTUFF
376S0771
CRITICAL Q7222 IRF6795 DIRECTFET-MX
VR_CPU_ISNS2_P
VR_CPU_ISNS2_N

PHASE 3

376S0772
R7242 10 5% 1/10W MF-LF 603
NOSTUFF R7245 0 5% 1/10W MF-LF 603
R7241 10 5% 1/10W MF-LF 603
VR_CPU_DRV3_VCC
NO_TEST=TRUE NET_PHYSICAL_TYPE=POWER
VR_CPU_DRV3_UVCC
NET_PHYSICAL_TYPE=POWER
VR_CPU_DRV3_PVCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
C7241 1UF 10% 16V X5R 603
VR_CPU_BOOT3_RC
NET_PHYSICAL_TYPE=VR_CTL_PHY NET_SPACING_TYPE=VR_CONTROL DIDT=TRUE NO_TEST=TRUE
R7244 0 5% 1/10W MF-LF 603
C7243 0.22UF 10% 16V X7R 603
C7242 1UF 10% 16V X5R 603
NOSTUFF C7240 1UF 10% 16V X5R 603
U7241 ISL6612 QFN1
VCC PVCC BOOT PWM UGATE PHASE NC NC LGATE GND THRML PAD
VR_CPU_PWM3
VR_CPU_DRV3_BOOT NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_DRV3_UGATE NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_PHASE3 NET_PHYSICAL_TYPE=POWER DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
VR_CPU_DRV3_LGATE NET_PHYSICAL_TYPE=VR_CTL_PHY NO_TEST=TRUE DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_DRV3_GDSEL
NOSTUFF R7247 0 5% 1/10W MF-LF 603
376S0771
CRITICAL Q7241 IRF6710 S1
CRITICAL C7245 220UF 20% 16V ALUM-POLY 8X7-TH
CRITICAL C7246 10UF 10% 16V X5R-CERM 0805
CRITICAL C7249 10UF 10% 16V X5R-CERM 0805
C7283 1UF 10% 16V X5R 603
C7247 1UF 10% 16V X5R 603
THESE TWO CAPS ARE FOR EMC
C7250 0.001UF 10% 50V X7R 402
C7251 1UF 10% 16V X5R 402
CRITICAL L7241 0.24UH+/-20%-0.000420HM-40A SDP1108M-TH 152-0118
SWITCH_NODE=TRUE
CRITICAL R7248 0.0005 1% 1W MF 0612
PPVCORE_S0_CPU_REG
NOSTUFF R7246 2.2 5% 1/8W MF-LF 805
VR_CPU_PH3_SNUB
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
C7248 0.001UF 10% 50V CERM 402 NOSTUFF
CRITICAL Q7242 IRF6795 DIRECTFET-MX
VR_CPU_ISNS3_P
VR_CPU_ISNS3_N

OUTPUT BULK DECOUPLING:

128S0209
PPVCORE_S0_CPU_REG
75A MAX
C7260 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7261 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7262 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7263 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7264 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7265 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

SYNC_MASTER=K62 SYNC_DATE=01/06/2011
PAGE TITLE
VREG: CPU CORE - PHASES 1-3
Apple Inc.
DRAWING NUMBER 051-8115 SIZE D
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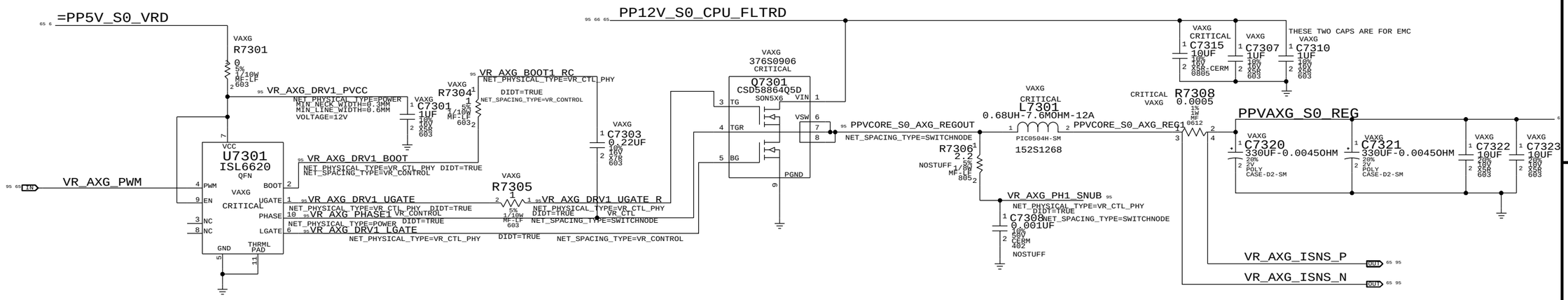
AXG PHASE (MAX 15A)



SYNC_MASTER=K60_AARON SYNC_DATE=N/A

PAGE TITLE
VREG:AXG PHASE/CORE - CAPS

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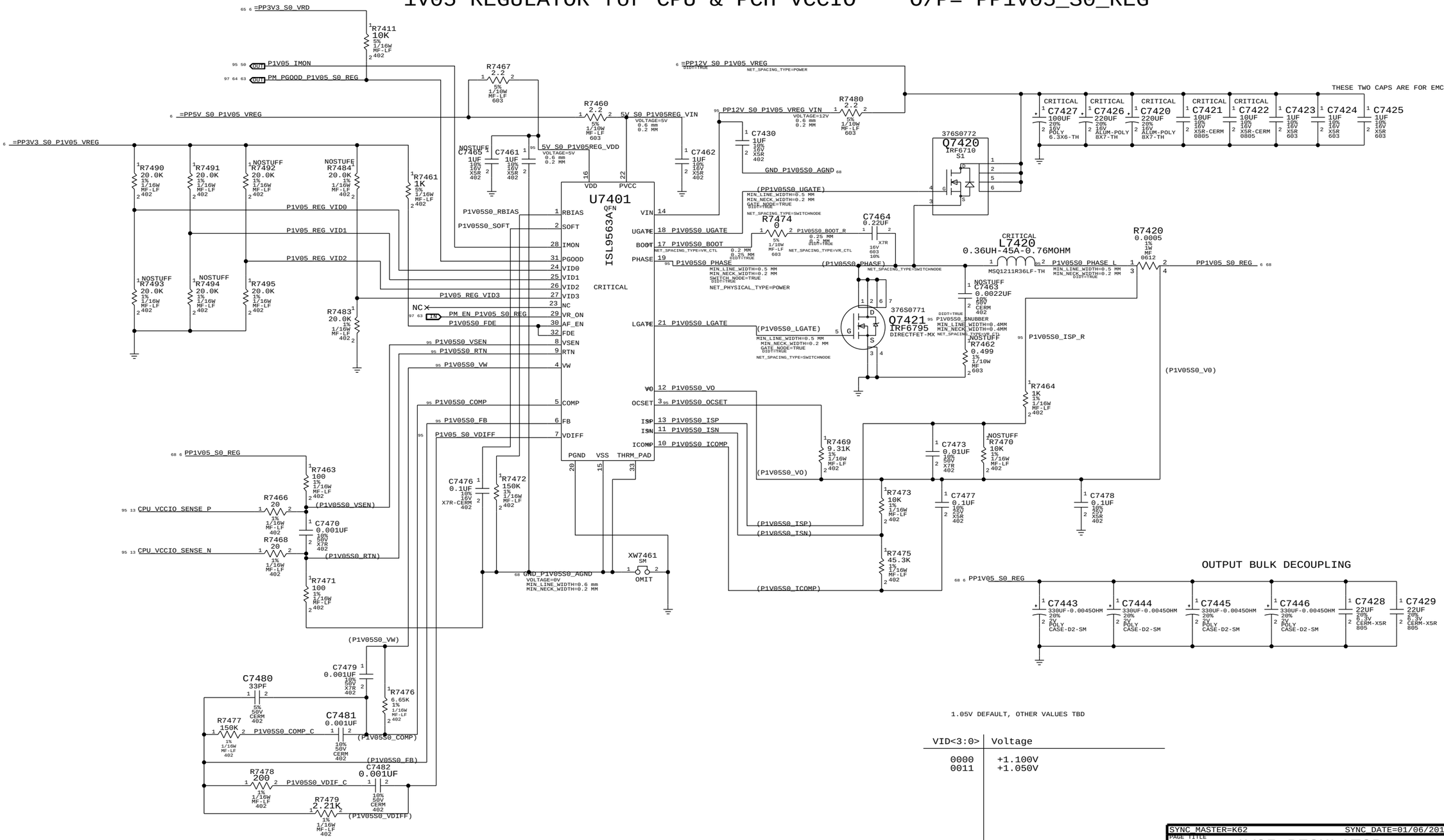
1V05 REGULATOR for CPU & PCH VCCIO O/P= PP1V05_S0_REG



1.05V DEFAULT, OTHER VALUES TBD

VID<3:0>	Voltage
0000	+1.100V
0011	+1.050V

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: 1V05 REGULATOR

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CPU VCCSA 0.925V (8.8A MAX)

=PPVCCIO_S0_CPU_VCCSA

NOTE: THIS RAIL IS COMING FROM PPVCCSA_S0_INPUT_SNS AFTER SENSE RES

=PP3V3_S5_CPU_VCCSA — R7531 100 5% 1/10W MF-LF 402 — VCCSA_REF

CRITICAL
U7505 ISL21070 SOT23-3
VIN, VOUT, GND

C7515 1UF 10% 10V X5R 402
C7516 1UF 10% 10V X5R 402

C7551 10PF 5% 50V CERM 402

R7550 49.9K 1% 1/16W MF-LF 402 — VCCSA_FIL — C7550 560PF 10% 50V CERM 402

R7505 0 5% 1/10W MF-LF 402 — VCCSA_GATE
NET_PHYSICAL_TYPE=VR_CTL_PHY
DIDT=TRUE
NET_SPACING_TYPE=VR_CTL

Q7500 IRFH3702TRPBF PQFN
376S0910

VCCSA_CNTRL_INPUT1

U7501 LM358-SOI-HF

VCCSA_OUT
NET_PHYSICAL_TYPE=VR_CTL_PHY
DIDT=TRUE
NET_SPACING_TYPE=VR_CTL

NOSTUFF R7506 1K 5% 1/10W MF-LF 402
NET_PHYSICAL_TYPE=POWER
DIDT=TRUE
NET_SPACING_TYPE=POWER

PPVCCSA_S0_FET

OMIT_TABLE C7509 220UF-25MOHM 20% 6V POLY-TANT CASE-D2E-SM
OMIT_TABLE C7510 220UF-25MOHM 20% 6V POLY-TANT CASE-D2E-SM
C7507 10UF 10% 6.3V X5R 805
C7508 10UF 10% 6.3V X5R 805

Place C7507 inside cavity
Place C7508 inside cavity

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0330	2	POLYTANT,6V,220UF,25MOHM	C7509,C7510	

=PP12V_S0_CPU_VCCSA

R7504 2.2 5% 1/10W MF-LF 603

VCCSA_PWR_RC

C7502 1UF 10% 25V X5R 603-1

VCCSA_CNTRL_INPUT2

R7507 5.49K 1% 1/16W MF-LF 402

VCCSA_CNTRL_INPUT2_R

R7535 22 5% 1/10W MF-LF 402

R7533 10K 1% 1/16W MF-LF 402

NOSTUFF C7512 10PF 5% 50V CERM 402

R7552 1K 5% 1/16W MF-LF 402 — VCCSA_CRL — C7552 1000PF 5% 25V NP0-C0G 402

CPU_VCCSA_SENSE

R7503 0 5% 1/10W MF-LF 402

C7501 100PF 5% 50V CERM 402

=PPVCCSA_S0_INPUT_PWR

CRITICAL C7506 330UF-0.009OHM 20% 2V POLY CASE-D2-HF
C7504 4.7UF 20% 6.3V X5R-CERM1 402
C7505 0.1UF 20% 10V CERM 402

U7501 LM358-SOI-HF

NOTE: THIS POWER RAIL IS BEFORE THE SENSE RES R5310

SYNC_MASTER=K62 SYNC_DATE=11/15/2010

PAGE TITLE: CPU VCCSA REGULATOR

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 75 OF 110
SHEET: 69 OF 98

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3V3 S5 REGULATOR

3V3 OUTPUT

=PP12V_S5_P5VS3_VREG
NET_SPACING_TYPE=POWER

EMC CAPS
PLACE CLOSE TO FET

C7718 100UF 20% 16V POLY 6.3X6-TH
C7712 10UF 10% 16V X5R-CERM 0805
C7710 10UF 10% 16V X5R-CERM 0805
C7711 1UF 10% 16V X5R 603
C7722 1UF 10% 16V X5R 603

NET_PHYSICAL_TYPE=POWER
DIDT=TRUE

PP3V3_S5_REG
R7776 0.002 1% 1/4W MF-LF 1206
CRITICAL
L7710 2.2UH-14A MMD06CZ-SM
PP3V3_S5_REG_R
NET_PHYSICAL_TYPE=POWER
C7790 0.01UF 10% 16V CERM 402
R7790 15.8K 1% 1/16W MF-LF 402
R7791 15.8K 1% 1/16W MF-LF 402
C7730 1000PF 5% 25V NP0-C0G 402 NOSTUFF
NET_SPACING_TYPE=VR_CTL
R7730 0.499 1% 1/10W MF 603
P3V3S5_REG_SNUB
DIDT=TRUE

Q7710
RJK0384DPA
WPAK
376S0801
D1
G1 1 (P3V3S5_UGATE)
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
GATE_NODE=TRUE
NET_SPACING_TYPE=VR_CONTROL
S1/D2 7
G2 6 (P3V3S5_LGATE)
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
GATE_NODE=TRUE
NET_SPACING_TYPE=VR_CONTROL
S2

C7714 0.1UF 10% 50V X7R 603-1
P3V3S5_REG_BOOT_R
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
DIDT=TRUE
NET_SPACING_TYPE=VR_CONTROL
(P3V3S5_PHASE)
R7710 0 5% 1/10W MF-LF 603
NET_SPACING_TYPE=VR_CONTROL
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
DIDT=TRUE
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
NET_SPACING_TYPE=SWITCHNODE
NET_PHYSICAL_TYPE=POWER

OUTPUT BULK DECOUPLING:
PLACEMENT_NOTE=PLACE NEXT TO C7716
C7715 10UF 10% 16V X5R-CERM 0805
C7717 10UF 10% 16V X5R-CERM 0805
128S0237
CRITICAL
C7721 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
XW7716 SM OMIT
C7723 0.1UF 20% 16V CERM 603
C7716 0.1UF 20% 16V CERM 603
EMC CAPS
PLACE CLOSE TO L

R7720 45.3K 1% 1/16W MF-LF 402 <Ra>
R7721 10.0K 0.5% 1/16W MF 402 <Rb>
R7724 976 1% 1/16W MF-LF 402
C7720 1000PF 5% 25V NP0-C0G 402
P3V3S5_REG_FB_R

Vout = 0.6V * (1 + Ra / Rb)

PM_EN_P5V_S3_REG

=PP12V_S5_P5VS3_VREG
NOSTUFF
R7725 20K 5% 1/16W MF-LF 402

U7700
ISL62383
QFN
CRITICAL

PM_PGOOD_P3V3_S5_REG	7 PGOOD1	PGOOD2 1	
P3V3S5_REG_UGATE	14 UGATE1	UGATE2 22	P5VS3_REG_UGATE
P3V3S5_REG_BOOT	15 BOOT1	BOOT2 21	P5VS3_REG_BOOT
P3V3S5_REG_PHASE	13 PHASE1	PHASE2 23	P5VS3_REG_PHASE
P3V3S5_REG_LGATE	16 LGATE1	LGATE2 20	P5VS3_REG_LGATE
P3V3S5_REG_ISEN	10 ISEN1	ISEN2 26	P5VS3_REG_ISEN
P3V3S5_REG_OCSET	11 OCSET1	OCSET2 25	P5VS3_REG_OCSET
P3V3S5_REG_VOUT1	9 VOUT1	VOUT2 27	P5VS3_REG_VOUT2
P3V3S5_REG_FB	8 FB1	FB2 28	P5VS3_REG_FB
P3V3S5_REG_FSET1	6 FSET1	FSET2 2	P5VS3_REG_FSET2
	12 EN1	EN2 24	
		FCCM 3	TP_P5VS3_REG_FCCM
	18 LDO5	VIN 17	VIN_5V_S5_REG_RC
	THRM PAD 29	PGND 29	

R7722 68K 5% 1/16W MF-LF 402
PM_EN_P3V3_S5_REG
R7723 33K 5% 1/16W MF-LF 402
P3V3S5_REG_FSET1
C7701 0.01UF 10% 16V CERM 402
R7701 16.5K 1% 1/16W MF-LF 402

C7719 100UF 20% 16V POLY 6.3X6-TH
C7766 100UF 20% 16V POLY 6.3X6-TH
C7767 100UF 20% 16V POLY 6.3X6-TH
C7768 100UF 20% 16V POLY 6.3X6-TH
C7758 10UF 10% 16V X5R-CERM 0805
C7765 10UF 10% 16V X5R-CERM 0805

=PP3V3_S5_VRD
R7726 20K 5% 1/16W MF-LF 402

PP5V_S5_LDO
EMC: C7753-C7755
PLACE AT Q7330
C7754 1UF 10% 16V X5R 603
C7755 1UF 10% 16V X5R 603

NET_PHYSICAL_TYPE=POWER
C7742 4.7UF 20% 6.3V CERM 603
R7740 2.2 5% 1/8W MF-LF 805
R7741 1 5% 1/8W MF-LF 805
P5V_S5_LDO_R
P5V_S5_VCC1
C7740 1UF 10% 16V X5R 603
C7741 1UF 10% 16V X5R 603
C7743 1UF 10% 16V X5R 603

PM_PGOOD_P5V_S3_REG
CRITICAL
Q7750 FDMS0346 POWER56 376S0875
MIN_LINE_WIDTH=0.6MM
NET_SPACING_TYPE=VR_CONTROL
P5VS3_REG_BOOT_R
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.6MM
NET_SPACING_TYPE=VR_CONTROL
R7750 0 5% 1/10W MF-LF 603
DIDT=TRUE
C7756 0.1UF 10% 25V X5R 402
NET_SPACING_TYPE=SWITCHNODE
DIDT=TRUE
NET_PHYSICAL_TYPE=POWER
NOSTUFF
C7757 0.001UF 10% 50V CERM 402
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.6MM
NET_SPACING_TYPE=VR_CONTROL
5V_SNUBBER
DIDT=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=SWITCHNODE
R7752 0.499 1% 1/10W MF 603 NOSTUFF
CRITICAL
Q7751 FDMS0355S POWER56 376S0917

C7747 0.01UF 10% 16V CERM 402
R7747 16.5K 1% 1/16W MF-LF 402
NOSTUFF
C7777 0.001UF 10% 50V CERM 402

5V S3 REGULATOR

Power Rating ?

5V OUTPUT

EMC: C7763-C7764
PLACE AT L7750.2
C7763 0.001UF 10% 50V X7R 402
C7764 0.001UF 10% 50V X7R 402

PP5V_S3_REG
R7775 0.002 1% 1/4W MF-LF 1206
CRITICAL
L7750 2.2UH+/-20%-0.0069OHM-16A PIC1005H-SM
PP5V_S3_REG_R
NET_PHYSICAL_TYPE=POWER
R7770 9.76K 1% 1/16W MF-LF 402
C7770 27.0NF 10% 10V X5R 402
R7771 9.76K 1% 1/16W MF-LF 402

OUTPUT BULK DECOUPLING:
C7760 10UF 20% 6.3V CERM 805-1
C7769 10UF 20% 6.3V CERM 805-1
CRITICAL
C7761 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
CRITICAL
C7762 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

XW7751 SM OMIT

R7759 976 1% 1/16W MF-LF 402
P5VS5_REG_FB_R
C7759 1000PF 5% 25V NP0-C0G 402
R7755 75K 1% 1/16W MF-LF 402 RA
R7756 10K 1% 1/16W MF-LF 402 RB

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE	5V_S3 / 3V3_S5 VREGS
Apple Inc.	DRAWING NUMBER 051-8115
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1.5 V DDR SUPPLY

PPDDR_S3_REG
VOUT = 1.5V
PEAK = 11A
AVG = 6.7A

=PP12V_S5_DDR_VREG
=PP5V_S3_DDR_VREG
=PP3V3_S3_VRD
PP5V_S3_DDR_REG_V5FILT
PM_EN_DDRVTT_S0_REG
PM_EN_DDR1V5_S3_REG
PM_PGOOD_DDR1V5_S3_REG
TP_PPVTT_S3_DDR_BUF (NOT USED)
PPVTT_S0_DDR_LDO
U7800 TPS51116 QFN SYM (2 OF 2)
Q7830 CSD58864Q5D SON5X6
L7830 1.5UH-15%-22A-3.3MOHM SDP1182M-TH
L7850 1.5UH-4A MMD04BZ-SM
U7850 ISL8013A QFN
PP1V5_S3_REG
PP1V8_S0_REG
OUTPUT BULK DECOUPLING:

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

Vout = 0.75V * (1 + Ra / Rb)

1.8 V SUPPLY

1A Average current

Vo=0.8*(1+ Ra/Rb)
Vo=0.8*(1+ 59/47)=1.804V

=PP5V_S0_P1V8_REG
PM_EN_P1V8_S0_REG
PM_PGOOD_P1V8_S0_REG
P1V8_REG_SYNC
P1V8_REG_PHASE
P1V8_REG_VFB

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE	1.5V / 1.8V VREGS
Apple Inc.	DRAWING NUMBER 051-8115 SIZE D
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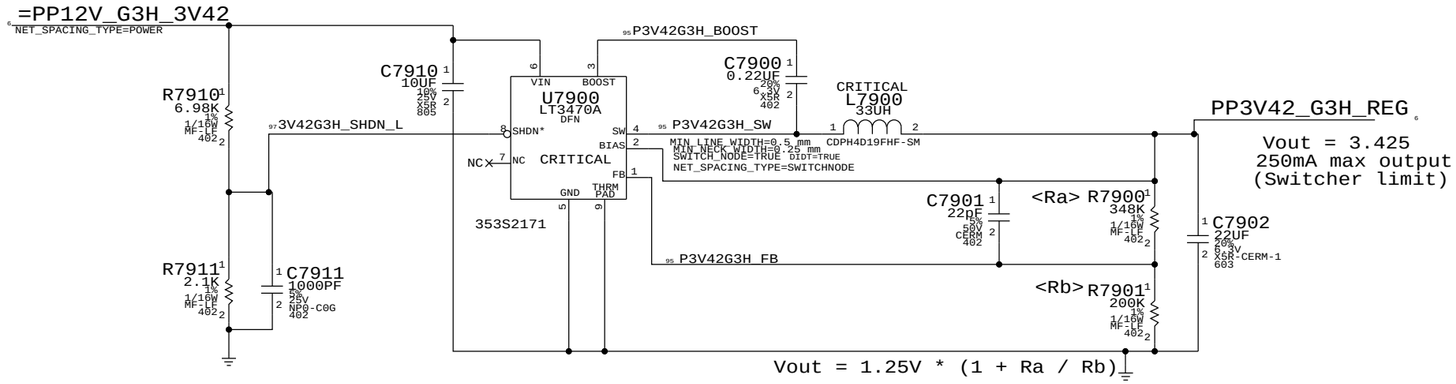
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

3.42 G3HOT SUPPLY

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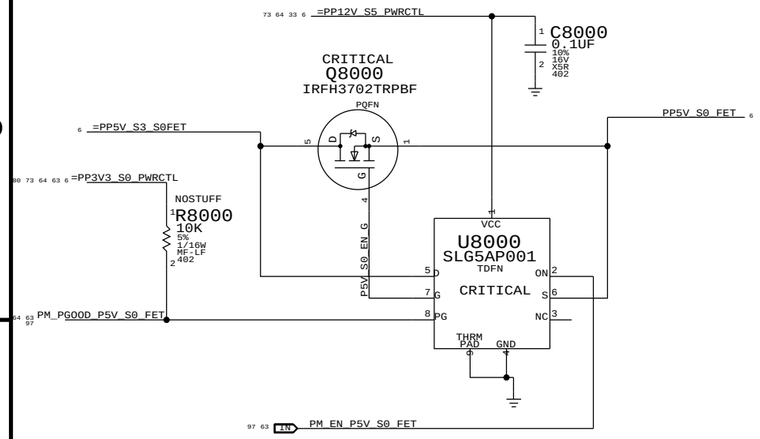
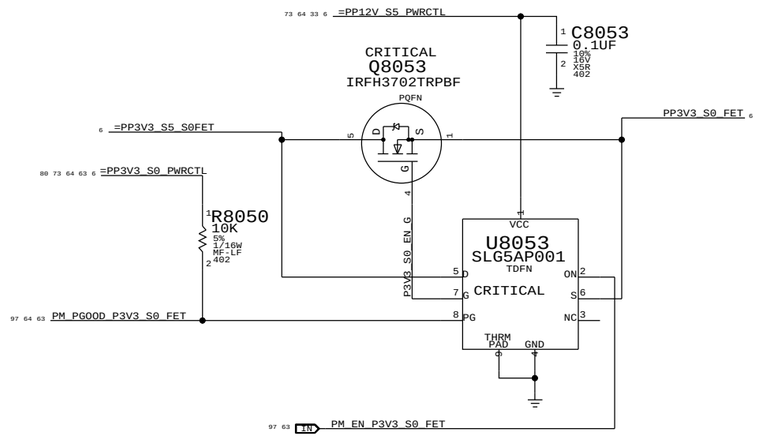
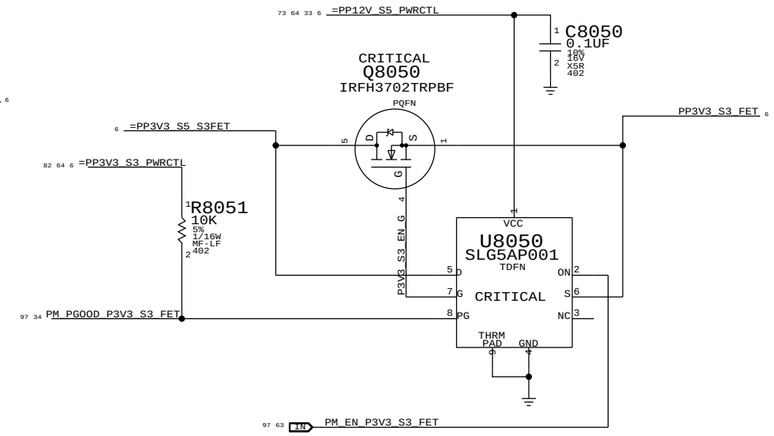
5V S0 FET (6.6A PK/3.1A AVG)



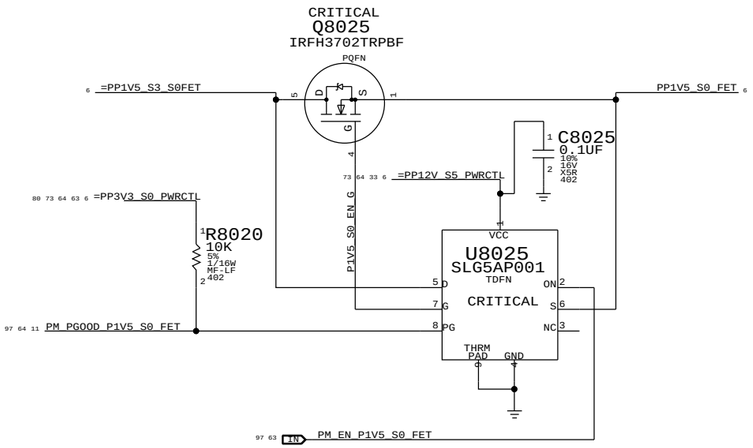
3.3V S0 FET (2.9APK / 2.0A AVG)



3.3V S3 FET (3.4A PK / 1.6A AVG)



1.5V S0 FET (4.8A PK / 4.8A AVG)



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

S3+S0 FETS

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376S0933
Q8110
IRFH9310PBF
P-CH MOSFET 376S0933 4.6-MOHM 20A (WHEN USED W/Q8112)
PWR CRITICAL

=PP12V_G3H_S5_FET

R8110 10K 5% 1/10W MF-LF 402

C8111 2.2UF 10% 16V X7R-CERM 805

C8110 0.47UF 10% 16V X7R 805-1

PP12V_S5_RSN

NET_PHYSICAL_TYPE=POWER
VOLTAGE=12V
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.5mm

R8132 0.005 1% 1W MF 2512

PP12V_S5_FET

10Amp-7Amp

NC NC

Short R8132 BEFORE DVT

R8111 10K 5% 1/10W MF-LF 402

S5_DG_1

S5_MSFT_G1

R8112 10K 5% 1/10W MF-LF 402

SMC_PM_G2_EN_L

Proto-3:Add C8111

SMC_PM_G2_EN

R8113 0 5% 1/10W MF-LF 402

SMC_PM_G2_EN_R

Q8112 2N7002 SOT23-HF1

High=3.3V
(2.4-5.5V)

R8115 100K 5% 1/10W MF-LF 402

SYNC_MASTER=K60 JERRY SYNC_DATE=01/06/2011

PAGE TITLE
12V_S0 & 12V_S5 switch

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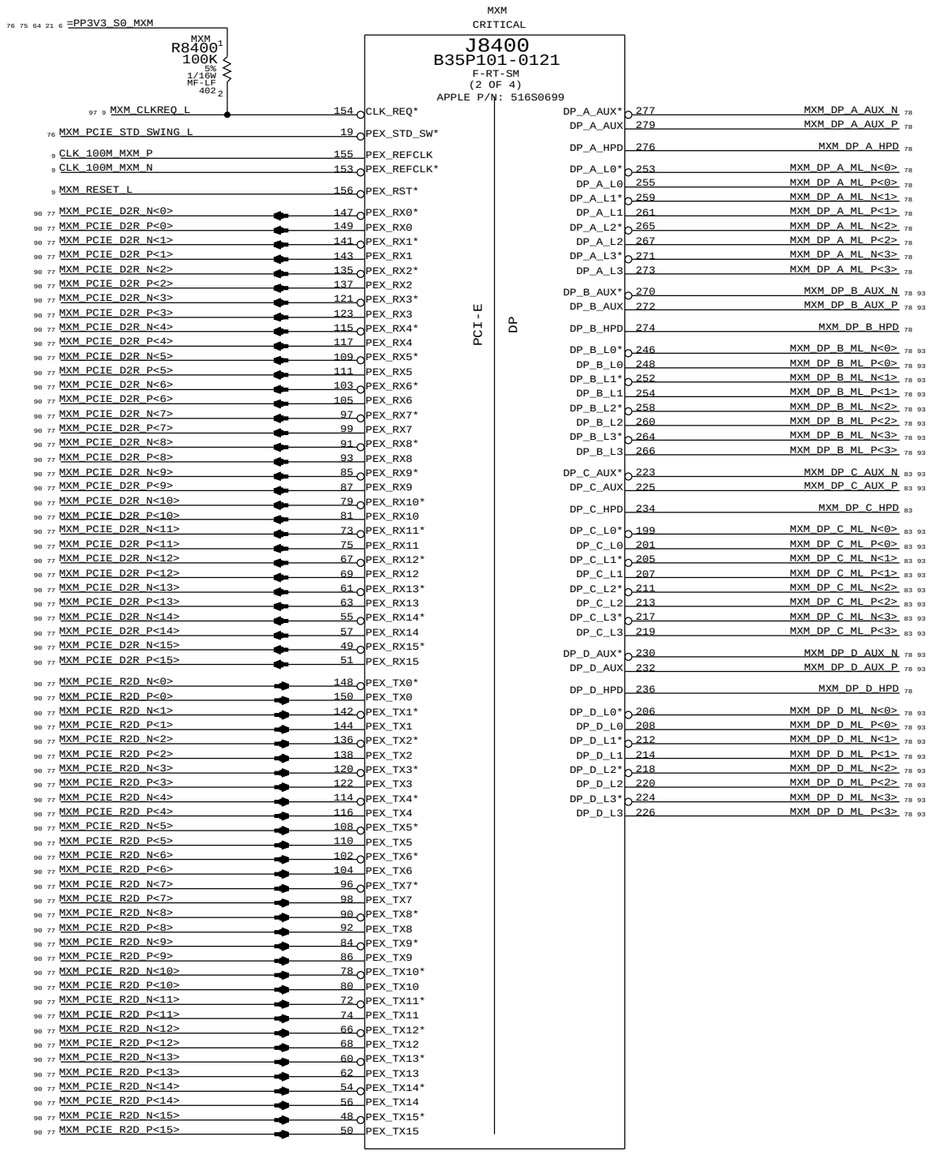
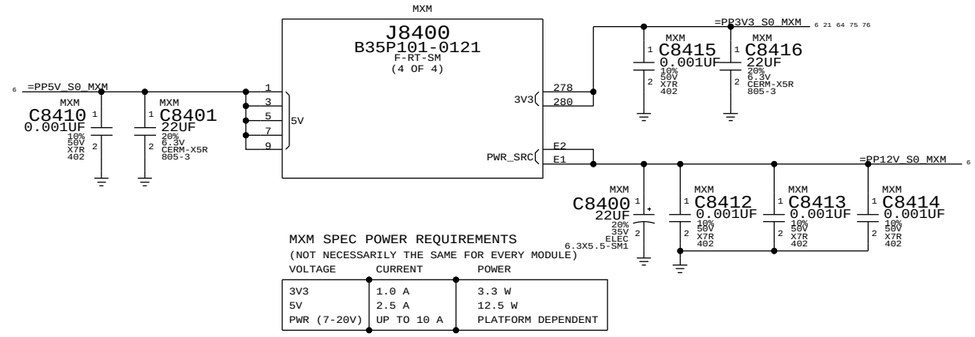
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM





MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

MXM DP PORT ROUTING

	K62	K60
DP A	EXT DP1	EXT DP1
DP B	T29 DP2	T29 DP2
DP C	INT DP	INT DP
DP D	T29 DP1	T29 DP1
DP E	EXT DP2	

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
MXM PCIe, DP & Power

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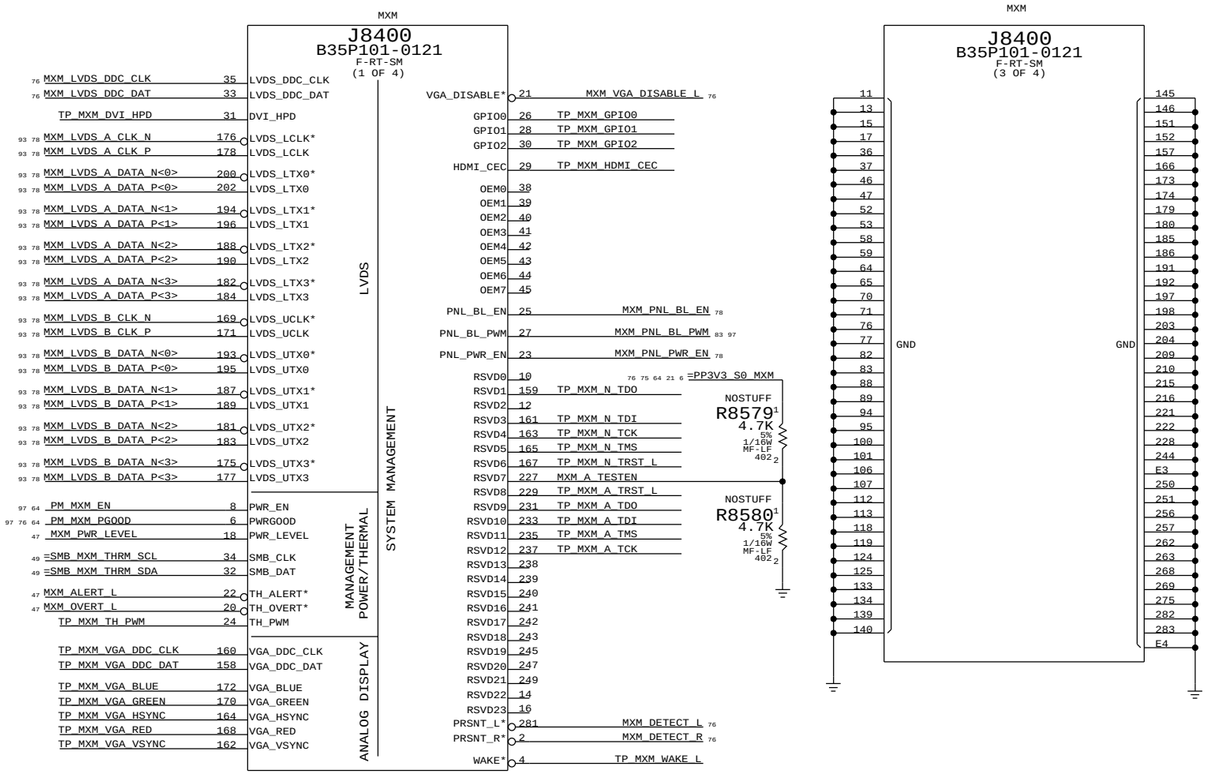
Page Notes

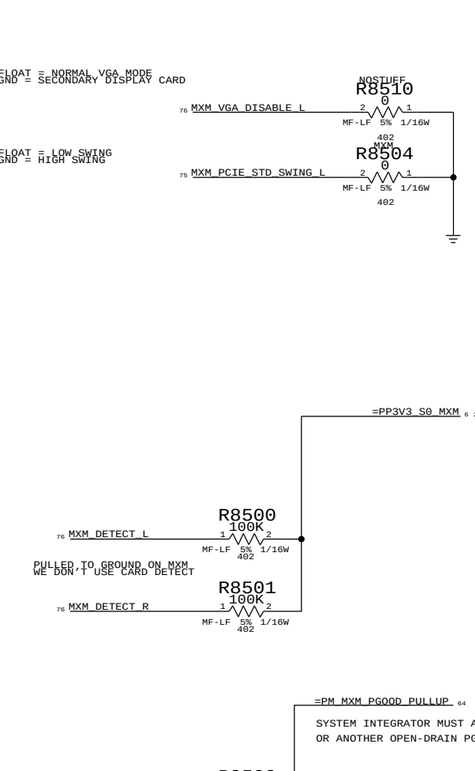
Power aliases required by this page:
- =PP3V3_S0_MXM

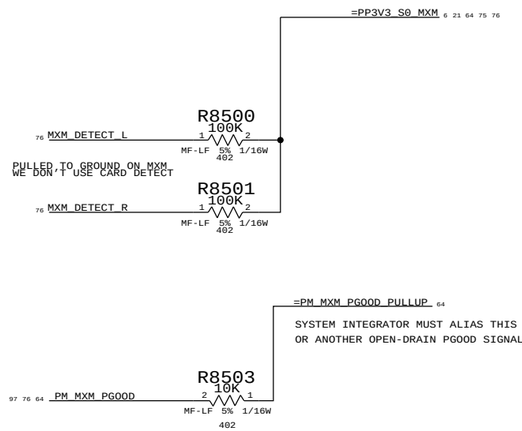
Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR

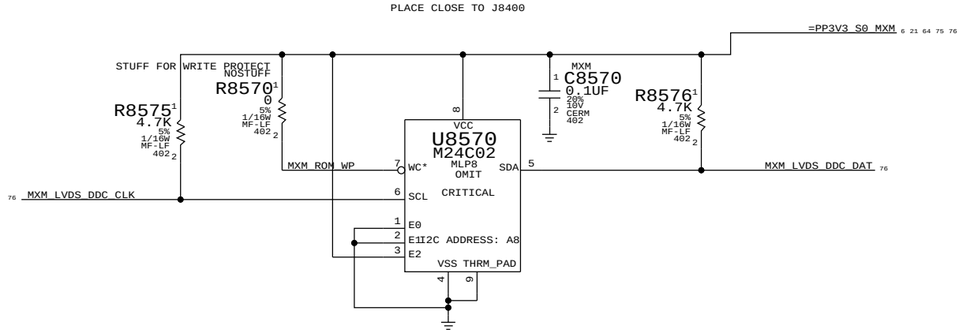






MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



SYNC_MASTER=K60_MASTER SYNC_DATE=N/A

PAGE TITLE: MXM I/O

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DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
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MXM TX CAPS

PEG_R2D_C_P<0>	MXM	C8600	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>
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MXM RX CAPS

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SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

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Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MXM ALIAS

75	MXM_DP_A_ML_P<0..3>	=	DP_EXTA_ML_C_P<0..3>		84 93
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	
75	MXM_DP_A_ML_N<0..3>	=	DP_EXTA_ML_C_N<0..3>		84 93
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	
75	MXM_DP_A_AUX_P	=	DP_EXTA_AUXCH_C_P		78 84 93
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	
75	MXM_DP_A_AUX_N	=	DP_EXTA_AUXCH_C_N		78 84 93
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	
75	MXM_DP_A_HPD	=	DP_EXTA_HPD		84
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	

Unused MXM Interfaces

93 76	MXM_LVDS_A_CLK_N	=	NC_MXM_LVDS_A_CLK_N	
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93 76	MXM_LVDS_A_CLK_P	=	NC_MXM_LVDS_A_CLK_P	
		=	MAKE_BASE=TRUE	NO_TEST=TRUE
93 76	MXM_LVDS_A_DATA_N<3..0>	=	NC_MXM_LVDS_A_DATA_N<3..0>	
		=	MAKE_BASE=TRUE	NO_TEST=TRUE
93 76	MXM_LVDS_A_DATA_P<3..0>	=	NC_MXM_LVDS_A_DATA_P<3..0>	
		=	MAKE_BASE=TRUE	NO_TEST=TRUE
93 76	MXM_LVDS_B_CLK_N	=	NC_MXM_LVDS_B_CLK_N	
		=	MAKE_BASE=TRUE	NO_TEST=TRUE
93 76	MXM_LVDS_B_CLK_P	=	NC_MXM_LVDS_B_CLK_P	
		=	MAKE_BASE=TRUE	NO_TEST=TRUE
93 76	MXM_LVDS_B_DATA_N<3..0>	=	NC_MXM_LVDS_B_DATA_N<3..0>	
		=	MAKE_BASE=TRUE	NO_TEST=TRUE
93 76	MXM_LVDS_B_DATA_P<3..0>	=	NC_MXM_LVDS_B_DATA_P<3..0>	
		=	MAKE_BASE=TRUE	NO_TEST=TRUE

Unused T29 Interfaces

96 86	T29_D2R_N<2..3>	=	NC_T29_D2R_N<2..3>			
		=	MAKE_BASE=TRUE	NO_TEST=TRUE		
96 86	T29_D2R_P<2..3>	=	NC_T29_D2R_P<2..3>			
		=	MAKE_BASE=TRUE	NO_TEST=TRUE		
96 86	T29_R2D_C_N<2..3>	=	NC_T29_R2D_C_N<2..3>			
		=	MAKE_BASE=TRUE	NO_TEST=TRUE		
96 86	T29_R2D_C_P<2..3>	=	NC_T29_R2D_C_P<2..3>			
		=	MAKE_BASE=TRUE	NO_TEST=TRUE		
86	T29_LSEO<3>	=	T29_LSEO_LSOE3	=	T29_LSOE<3>	86
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	=	
86	T29_LSEO<2>	=	T29_LSEO_LSEO2	=	T29_LSOE<2>	86
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	=	

DDC/AUX ALIAS

93 84 78	DP_EXTA_AUXCH_C_P	=	DP_EXTA_DDC_CLK		84
	MAKE_BASE=TRUE	=			
93 84 78	DP_EXTA_AUXCH_C_N	=	DP_EXTA_DDC_DATA		84
	MAKE_BASE=TRUE	=			

T29 CONN POWER CONTROL ALIAS

95 84	PP3V3_SW_DPAPWR	=	=PP3V3_SW_DPAPWR		6
		=			
97 36 33 19	PCIE_WAKE_L	=	=T29_WAKE_L		84
		=			

T29 MXM DP ALIAS

93 75	MXM_DP_D_ML_P<0..3>	=	DP_T29SNK0_ML_C_P<0..3>		86 96
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	
93 75	MXM_DP_D_ML_N<0..3>	=	DP_T29SNK0_ML_C_N<0..3>		86 96
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	
93 75	MXM_DP_D_AUX_P	=	DP_T29SNK0_AUXCH_C_P		86 96
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	
93 75	MXM_DP_D_AUX_N	=	DP_T29SNK0_AUXCH_C_N		86 96
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	
75	MXM_DP_D_HPD	=	DP_T29SNK0_HPD		86
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	
93 75	MXM_DP_B_ML_P<0..3>	=	DP_T29SNK1_ML_C_P<0..3>		86 96
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	
93 75	MXM_DP_B_ML_N<0..3>	=	DP_T29SNK1_ML_C_N<0..3>		86 96
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	
93 75	MXM_DP_B_AUX_P	=	DP_T29SNK1_AUXCH_C_P		86 96
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	
93 75	MXM_DP_B_AUX_N	=	DP_T29SNK1_AUXCH_C_N		86 96
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	
75	MXM_DP_B_HPD	=	DP_T29SNK1_HPD		86
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	

UNUSED MXM CONTROL SIGNALS

76	MXM_PNL_BL_EN	=	NC_MXM_PNL_BL_EN		
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76	MXM_PNL_PWR_EN	=	NC_MXM_PNL_PWR_EN		
		=	MAKE_BASE=TRUE	NO_TEST=TRUE	

SYNC_MASTER=K60_AARON SYNC_DATE=07/18/2010

PAGE TITLE
DP ALIAS AND CONTROL

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
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System RTC Power Source & 32kHz / 25MHz Clock Generator

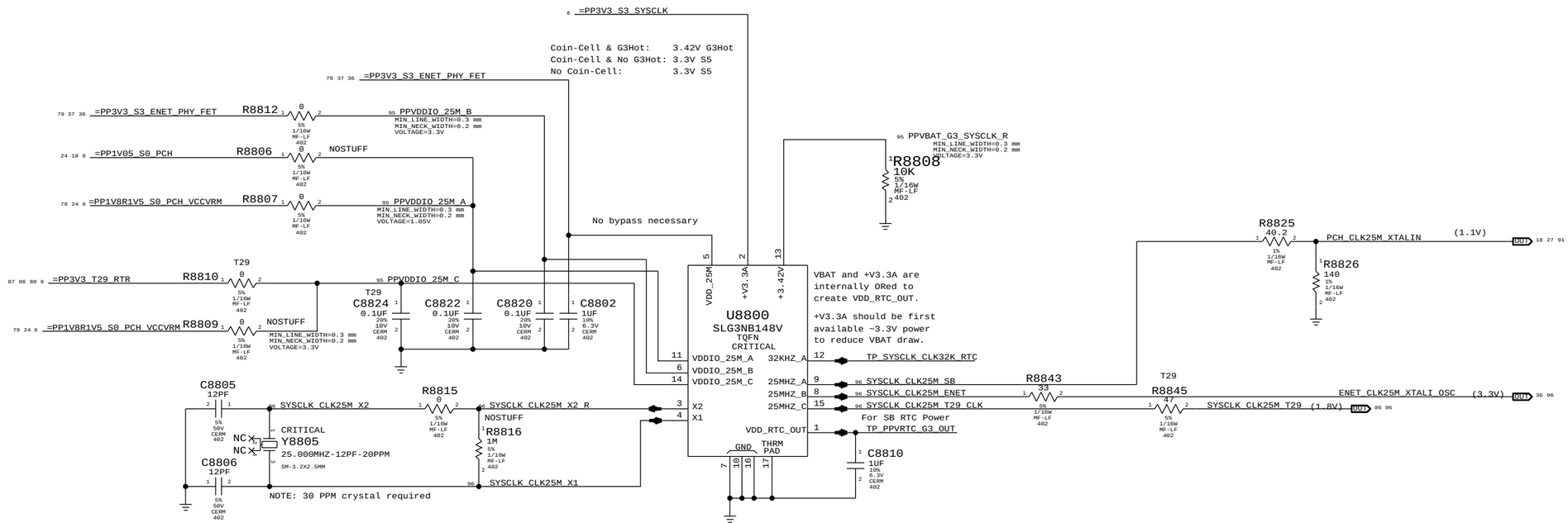
GreenCLK Implementation Notes:

VBAT: Alias as appropriate (see note below & Desktop Example)
+V3.3A: Alias as appropriate (see note below)
VDD_25M: 3.3V matching 'highest' VDDIO power state (ENET)

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

For Cougar Point Desktop: VDDIO = VCCVRM (1.8V), Vclk = 1.1V Max, Divider: 604 / 1000
For Cougar Point Mobile: VDDIO = VCCVRM (1.5V), Vclk = 1.1V Max, Divider: 332 / 1000
For Caesar-IV (BCM57765): VDDIO = XTALVDDH (3.3V), Vclk = 3.3V Max. No Divider Necessary



SYNC MASTER=K62	SYNC DATE=01/06/2012
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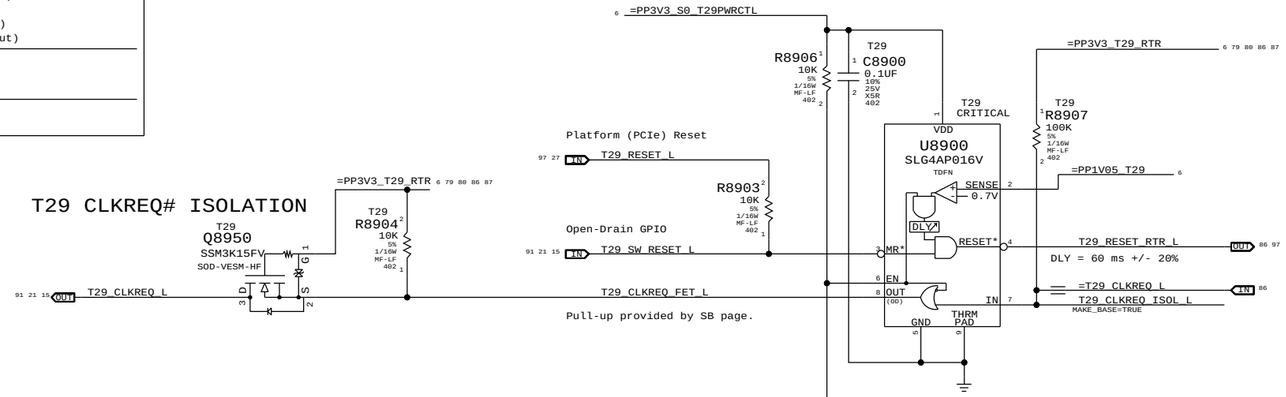
Page Notes

Power aliases required by this page:
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

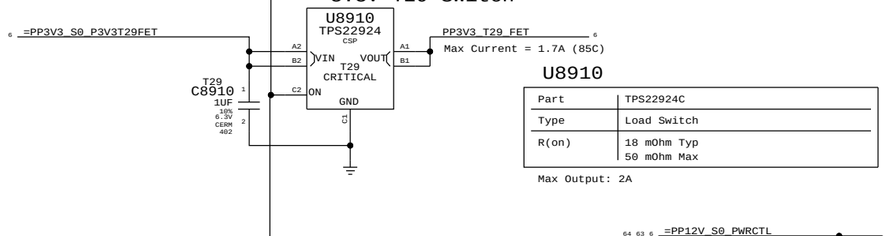
Signal aliases required by this page:
- =T29_CLKREQ_L
- T29_RESET_L

BOM options provided by this page:
(NONE)

Supervisor & CLKREQ# Isolation



3.3V T29 Switch

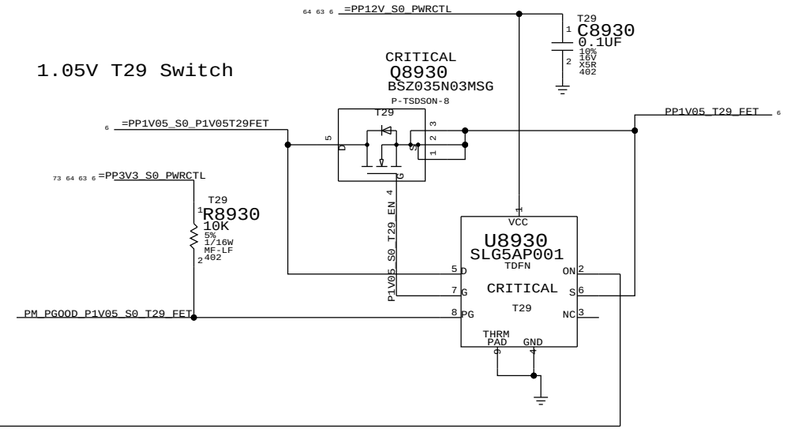


U8910

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.05V T29 Switch



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: T29 POWER

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Page Notes

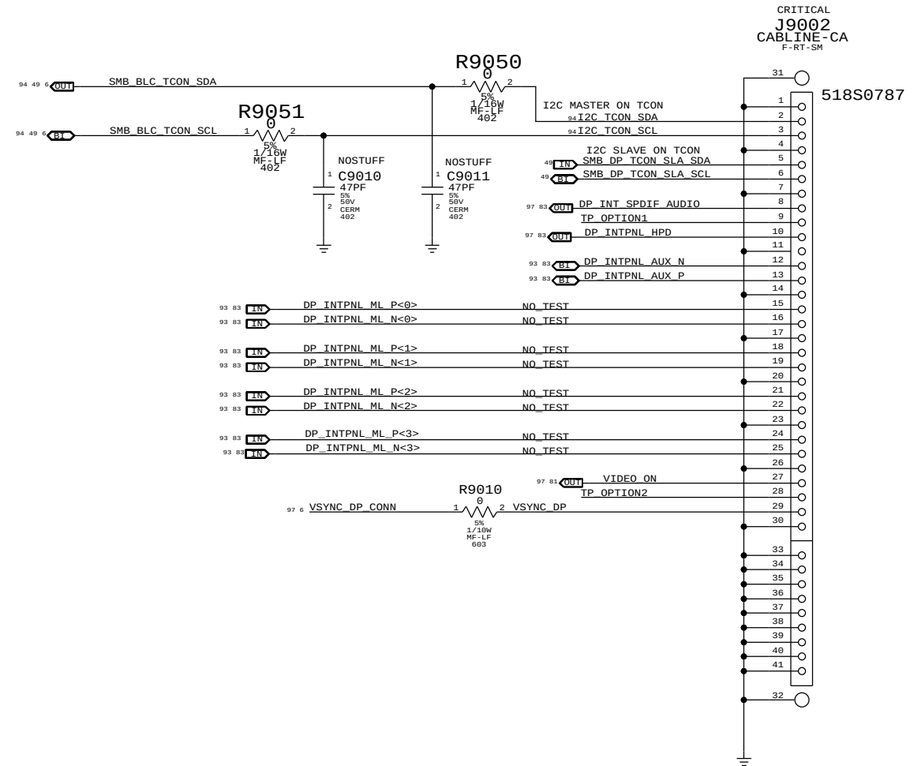
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

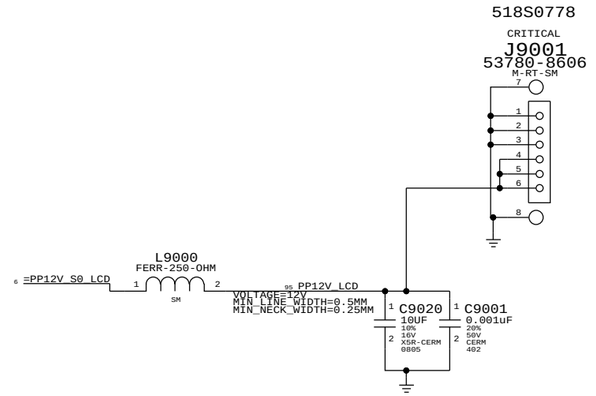
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

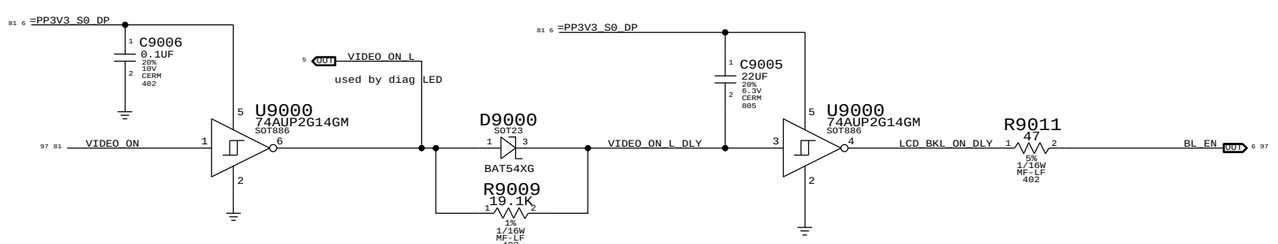


INTERNAL DP POWER



BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
Display: Int DP Connector

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3V3(DP)/2V9(T29) PORTA SUPPLY

=PP5V_S3_P3V3R2V9_REG_A

C9120 10UF 10% 16V X5R-CERM 0805

CRITICAL
U9101 ISL80101A DFN
VIN, ENABLE, SS, ISET, GND, THRM PAD, VOUT, ADJ, PG

T29_DP_PORTA_PWR_EN_REG
3V3R2V9_SS_A
3V3R2V9_DPAPWR_ADJ
PM_PGOOD_P3V3_2V9_A

C9121 0.022UF 10% 16V CERM-X5R 402
R9130 25.5K 1/16W 1% MF-LF 402
80101A1_ISET

PP3V3R2V9_DPAPWR_D

C9122 10UF 10% 16V X5R-CERM 0805
R9121 20K 1/16W 5% MF-LF 402
C9123 330PF 10% 50V 402 CERM

D9101 POWERDI-123 DFLS260

PP3V3R12V_SW_DPAPWR

NET_PHYSICAL_TYPE=POWER
MIN_LINE_WIDTH=0.38MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V

C9124 10UF 10% 16V X5R-CERM 0805
NOSTUFF C9125 10UF 10% 16V X5R-CERM 0805
R9150 2.2K 1/10W 5% MF-LF 603

NET_PHYSICAL_TYPE=POWER
MIN_LINE_WIDTH=0.38MM
VOLTAGE=12V
MIN_NECK_WIDTH=0.20 MM

R9124 11.5K 1/16W 1% MF-LF 402 <RA>
R9123 2.05K 1/16W 1% MF-LF 402 <RB2>
NOSTUFF R9125 15.0K 1/16W 1% MF-LF 402 <RB1>

=PP3V3_S3_P3V3R2V9_REG_A
R9122 100K 1/16W 5% MF-LF 402

VO=0.5*(1+ RA/RB)
VO=3.304V

=PP3V3_S5_P3V3R2V9_A
C9150 0.1UF 10% 16V X5R 402

=PP3V3_S3_PWRCTL
NOSTUFF R9126 10K 5% 1/16W MF-LF 402

DP_A_PWRDWN_FET_R
DP_A_PWRDWN_INV

NOSTUFF Q9120 2N7002DW-X-G SOT-363
NOSTUFF Q9120 2N7002DW-X-G SOT-363

T29_DP_PORTA_PWR_EN
PM_PGOOD_P5V_S3_REG
U9120 MC74VHC1G08 SOT23-5-HF
T29_DP_PORTA_PWR_EN_REG

T29_A_BIAS
LO: 3V3 FOR DP
HI: 2V8 FOR T29
2V9 measured at CDR

NO_T29 R9128 0 5% 1/16W MF-LF 402
PM_SLP_S3_L

12V T29 PORTA SUPPLY

12 VOLTS
12 WATTS MAX PER PORT

=PP12V_S5_T29_A

NEED TO UPDATE TABLE BELOW LATER

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance unknown

T29 R9116 15K 5% 1/16W MF-LF 402

T29 C9110 0.1UF 10% 50V X7R 603-1

CRITICAL
T29 U9110 SN1010017 QFN
EN* (IPU-Weak!), RTRY*, CT, FLT*, ILIM, IFLT, GND, THRM PAD, VOUT, VIN

T29 C9111 0.1UF 10% 50V X7R 603-1

T29 D9105 DSN2 NSR20F20NXT5G

PP3V3R12V_SW_DPAPWR_D
PP3V3R12V_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=12V

DPAPWRSW_HVEN_L_R
DPAPWRSW_CT
DPAPWRSW_ILIM
DPAPWRSW_IFLT
TP_DPAPWRSW_FLT_L

T29 CRITICAL D9103 MMBZ5227BLT1H SOT23

NOSTUFF R9117 13K 5% 1/16W MF-LF 402

T29 R9112 0 5% 1/16W MF-LF 402 <CT>

T29 R9110 100K 1% 1/16W MF-LF 402 <RFLT>

T29 R9111 174K 1% 1/16W MF-LF 402 <RLIM>

T29 Q9115 SSM3K15FV SOD-VESM-HF

T29_A_HV_EN

IFLT = 200K / RFLT = 2A
ILIM = 201K / RLIM = 1.155A.
TFLT = CCT * 38900
TSD = CCT * 100000

SYNC_MASTER=K62 SYNC_DATE=11/14/2010

PAGE TITLE: 2V9/3V3/12V POWER SWITCH

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 91 OF 110
SHEET: 82 OF 98

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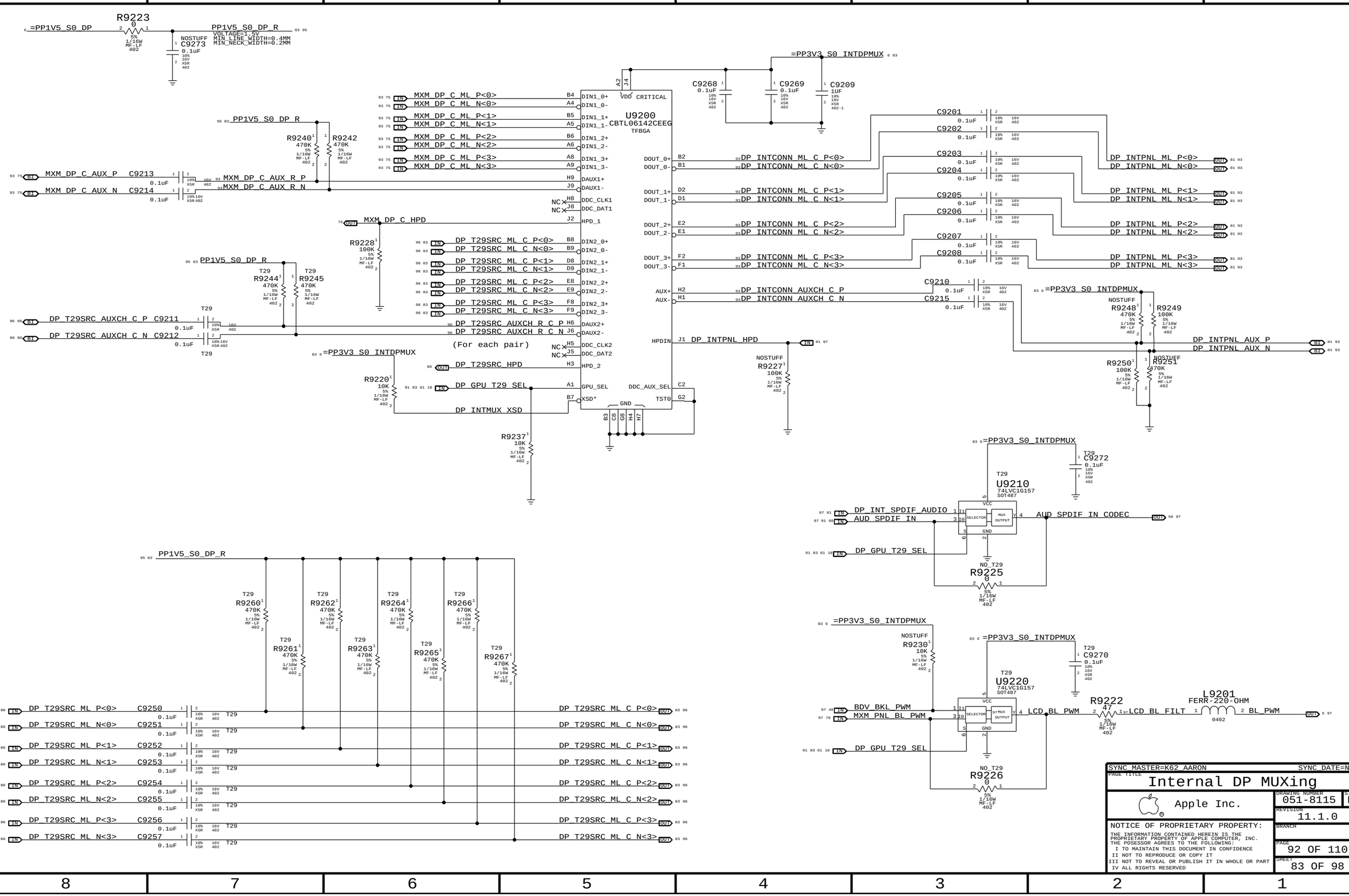
R9223 0 5% 1/16W MF-LF 402
=PP1V5_S0_DP
PP1V5_S0_DP_R
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NOSTUFF C9273 0.1uF 10% 16V X5R 402
=PP3V3_S0_INTDPMUX
C9268 0.1uF
C9269 0.1uF
C9209 1UF
U9200 CBTL06142CEEG TFBGA
VDD CRITICAL
MXM_DP_C_ML_P<0>
MXM_DP_C_ML_N<0>
MXM_DP_C_ML_P<1>
MXM_DP_C_ML_N<1>
MXM_DP_C_ML_P<2>
MXM_DP_C_ML_N<2>
MXM_DP_C_ML_P<3>
MXM_DP_C_ML_N<3>
PP1V5_S0_DP_R
R9240 470K
R9242 470K
MXM_DP_C_AUX_P C9213 0.1uF
MXM_DP_C_AUX_N C9214 0.1uF
MXM_DP_C_AUX_R_P
MXM_DP_C_AUX_R_N
MXM_DP_C_HPD
R9228 100K
DP_T29SRC_ML_C_P<0>
DP_T29SRC_ML_C_N<0>
DP_T29SRC_ML_C_P<1>
DP_T29SRC_ML_C_N<1>
DP_T29SRC_ML_C_P<2>
DP_T29SRC_ML_C_N<2>
DP_T29SRC_ML_C_P<3>
DP_T29SRC_ML_C_N<3>
R9244 470K
R9245 470K
DP_T29SRC_AUXCH_C_P C9211 0.1uF
DP_T29SRC_AUXCH_C_N C9212 0.1uF
DP_T29SRC_AUXCH_R_C_P
DP_T29SRC_AUXCH_R_C_N
(For each pair)
=PP3V3_S0_INTDPMUX
R9220 10K
DP_T29SRC_HPD
DP_GPU_T29_SEL
DP_INTMUX_XSD
R9237 10K
DDC_AUX_SEL
TST0
GND
DOUT_0+
DOUT_0-
DOUT_1+
DOUT_1-
DOUT_2+
DOUT_2-
DOUT_3+
DOUT_3-
AUX+
AUX-
HPDIN
DP_INTCONN_ML_C_P<0>
DP_INTCONN_ML_C_N<0>
DP_INTCONN_ML_C_P<1>
DP_INTCONN_ML_C_N<1>
DP_INTCONN_ML_C_P<2>
DP_INTCONN_ML_C_N<2>
DP_INTCONN_ML_C_P<3>
DP_INTCONN_ML_C_N<3>
DP_INTCONN_AUXCH_C_P
DP_INTCONN_AUXCH_C_N
DP_INTPNL_HPD
NOSTUFF R9227 100K
C9201 0.1uF
C9202 0.1uF
C9203 0.1uF
C9204 0.1uF
C9205 0.1uF
C9206 0.1uF
C9207 0.1uF
C9208 0.1uF
DP_INTPNL_ML_P<0>
DP_INTPNL_ML_N<0>
DP_INTPNL_ML_P<1>
DP_INTPNL_ML_N<1>
DP_INTPNL_ML_P<2>
DP_INTPNL_ML_N<2>
DP_INTPNL_ML_P<3>
DP_INTPNL_ML_N<3>
C9210 0.1uF
C9215 0.1uF
=PP3V3_S0_INTDPMUX
NOSTUFF R9248 470K
R9249 100K
R9250 100K
NOSTUFF R9251 470K
DP_INTPNL_AUX_P
DP_INTPNL_AUX_N
=PP3V3_S0_INTDPMUX
T29 C9272 0.1uF
T29 U9210 74LVC1G157 SOT487
DP_INT_SPDIF_AUDIO
AUD_SPDIF_IN
AUD_SPDIF_IN_CODEC
DP_GPU_T29_SEL
NO_T29 R9225 0
=PP3V3_S0_INTDPMUX
NOSTUFF R9230 10K
=PP3V3_S0_INTDPMUX
T29 C9270 0.1uF
T29 U9220 74LVC1G157 SOT487
BDV_BKL_PWM
MXM_PNL_BL_PWM
R9222 47
LCD_BL_PWM
LCD_BL_FILT
L9201 FERR-220-OHM 0402
BL_PWM
DP_GPU_T29_SEL
NO_T29 R9226 0
PP1V5_S0_DP_R
R9260 470K
R9261 470K
R9262 470K
R9263 470K
R9264 470K
R9265 470K
R9266 470K
R9267 470K
DP_T29SRC_ML_P<0> C9250 0.1uF
DP_T29SRC_ML_N<0> C9251 0.1uF
DP_T29SRC_ML_P<1> C9252 0.1uF
DP_T29SRC_ML_N<1> C9253 0.1uF
DP_T29SRC_ML_P<2> C9254 0.1uF
DP_T29SRC_ML_N<2> C9255 0.1uF
DP_T29SRC_ML_P<3> C9256 0.1uF
DP_T29SRC_ML_N<3> C9257 0.1uF
DP_T29SRC_ML_C_P<0>
DP_T29SRC_ML_C_N<0>
DP_T29SRC_ML_C_P<1>
DP_T29SRC_ML_C_N<1>
DP_T29SRC_ML_C_P<2>
DP_T29SRC_ML_C_N<2>
DP_T29SRC_ML_C_P<3>
DP_T29SRC_ML_C_N<3>
SYNC_MASTER=K62_AARON
SYNC_DATE=N/A
PAGE TITLE
Internal DP MUXing
Apple Inc.
DRAWING NUMBER 051-8115
SIZE D
REVISION 11.1.0
BRANCH
PAGE 92 OF 110
SHEET 83 OF 98
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DP A Super-Driver

DP_EXTA_ML_C_P<0> C9300 0.1uF DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1uF DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1uF DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1uF DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1uF DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1uF DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1uF DP_EXTA_ML_P<3>
DP_EXTA_AUXCH_C_P C9308 0.1uF DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1uF DP_EXTA_AUXCH_N

DP_EXTA_ML_C_N<3> C9307 0.1uF DP_EXTA_ML_N<3>

=PP3V3_S0_DPSDRVA
R9309 1M 5% MF-LF 1/16W 402 DP_EXTA_AUXCH_P
R9308 1M 5% MF-LF 1/16W 402 DP_EXTA_AUXCH_N

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

=PP3V3_S0_DPSDRVA
C9310 2.2UF 20% 6.3V CERM 402-LF
C9311 0.1UF 20% 10V CERM 402
C9312 0.1UF 20% 10V CERM 402

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NO STUFF R9311 1K 5% 1/16W MF-LF 402
R9310 1K 5% 1/16W MF-LF 402
R9312 1K 5% 1/16W MF-LF 402

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL

DP_EXTA_ML_P<0>	1	IN_D0P	OUT_D0P
DP_EXTA_ML_N<0>	2	IN_D0N	OUT_D0N
DP_EXTA_ML_P<1>	4	IN_D1P	OUT_D1P
DP_EXTA_ML_N<1>	5	IN_D1N	OUT_D1N
DP_EXTA_ML_P<2>	7	IN_D2P	OUT_D2P
DP_EXTA_ML_N<2>	8	IN_D2N	OUT_D2N
DP_EXTA_ML_P<3>	9	IN_D3P	OUT_D3P
DP_EXTA_ML_N<3>	10	IN_D3N	OUT_D3N
DP_EXTA_DDC_CLK	14	IN_SCL	AC_AUXP
DP_EXTA_DDC_DATA	13	IN_SDA	AC_AUXN
DP_EXTA_AUXCH_P	16	IN_AUXP	OUT_AUXP_SCL
DP_EXTA_AUXCH_N	15	IN_AUXN	OUT_AUXN_SDA
DP_EXTA_HPD	3	IN_HPD	(IPD) OUT_HPD
DPSDRVA_I2C_CTL_EN	26	I2C_CTL_EN (IPU)	CA_DET
DPSDRVA_I2C_ADDR0	36	I2C_ADDR0 (IPD)	CEXT
DPSDRVA_I2C_ADDR1	35	I2C_ADDR1 (IPD)	
=I2C_DPSDRVA_SCL	38	SCL_CTL	
=I2C_DPSDRVA_SDA	37	SDA_CTL	
DPSDRVA_REXT	12	REXT	
DP_AUXCH_ISOL	39	AUXDDC_OFF (IPD)	
DP_A_PWRDWN_R	34	PD (IPD)	
	21, 40	VDD	
	6, 33, 41	GND, THMPAD	

DP_A_CA_DET 32
CEXT 11 — PLACE_NEAR=U9310.11:2 mm — C9319 2.2UF 20% 6.3V CERM 402-LF

SDRV_PD R9318 0 5% 1/16W MF-LF 402
R9319 4.02K 1% 1/16W MF-LF 402

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

R9370 390 5% 1/20W MF 201
R9371 390 5% 1/20W MF 201
R9352 390 5% 1/20W MF 201
R9353 390 5% 1/20W MF 201

R9354 22 5% 1/20W MF 201 DP_SDRVA_ML_R_P<0>
R9355 22 5% 1/20W MF 201 DP_SDRVA_ML_R_N<0>
R9350 22 5% 1/20W MF 201 DP_SDRVA_ML_R_P<2>
R9351 22 5% 1/20W MF 201 DP_SDRVA_ML_R_N<2>

DP_SDRVA_ML_C_P<0>
DP_SDRVA_ML_C_N<0>
DP_SDRVA_ML_C_P<1>
DP_SDRVA_ML_C_N<1>
DP_SDRVA_ML_C_P<2>
DP_SDRVA_ML_C_N<2>
DP_SDRVA_ML_C_P<3>
DP_SDRVA_ML_C_N<3>
DP_SDRVA_AUXCH_C_P
DP_SDRVA_AUXCH_C_N
(DP_SDRVA_AUXCH_P)
(DP_SDRVA_AUXCH_N)
(DP_SDRVA_HPD)

C9363 0.1UF 10% 16V X5R-CERM 0201
C9362 0.1UF 10% 16V X5R-CERM 0201
C9367 0.1UF 10% 16V X5R-CERM 0201
C9366 0.1UF 10% 16V X5R-CERM 0201
C9369 0.1UF 10% 16V X5R 402
C9368 0.1UF 10% 16V X5R 402

AUXCH Snoop Port, used by PS8301 during training.

R9335 1K 5% 1/16W MF-LF 402
R9336 10K 5% 1/16W MF-LF 402

=T29_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#

=T29_WAKE_L
OMIT R9330 0 5% 1/16W MF-LF 402 SWCLK
SWDIO
T29_A_UC_ADDR

R9330 provides pads for programming/debug of MCU, please make accessible.
If project has space for 10-pin programming header it should be used.

T29 A High-Speed Signals

T29_A_BIAS_R2D_P0 VOLTAGE=3.3V
GND_VOID=TRUE (C9370/C9371)
C9370 0.47UF 20% 4V CERM-X5R-1 201
C9371 0.47UF 20% 4V CERM-X5R-1 201

T29_D2R_N<0> OUT
T29_D2R_P<0> OUT
OVERSIZE_PAD=0.875 mm^2 (Both L's)
L9372 1.0NH+/-0.1NH 0201-1
L9373 1.0NH+/-0.1NH 0201-1
T29_R2D_C_P<0> IN
T29_R2D_C_N<0> IN
T29_R2D_C_F_N<0>
T29_R2D_C_F_P<0>
C9372 0.47UF 20% 4V CERM-X5R-1 201 (C9372.2) GND_VOID=TRUE
C9373 0.47UF 20% 4V CERM-X5R-1 201 (C9373.2) GND_VOID=TRUE
R9372 1.5K 5% MF 1/20W 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
R9373 1.5K 5% MF 1/20W 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
T29_R2D_P<0>
T29_R2D_N<0>

T29_A_BIAS_R2D_N0 VOLTAGE=3.3V

T29 signals are P/N-swapped after AC caps to improve layout.

(All 4 L's)

T29_A_BIAS_R2D_P1 VOLTAGE=3.3V
GND_VOID=TRUE (C9380/C9381)
C9380 0.47UF 20% 4V CERM-X5R-1 201
C9381 0.47UF 20% 4V CERM-X5R-1 201

T29_D2R_P<1> OUT
T29_D2R_N<1> OUT
OVERSIZE_PAD=0.875 mm^2 (Both L's)
L9382 1.0NH+/-0.1NH 0201-1
L9383 1.0NH+/-0.1NH 0201-1
T29_R2D_C_N<1> IN
T29_R2D_C_P<1> IN
T29_R2D_C_F_N<1>
T29_R2D_C_F_P<1>
C9382 0.47UF 20% 4V CERM-X5R-1 201 (C9383.2) GND_VOID=TRUE
C9383 0.47UF 20% 4V CERM-X5R-1 201 (C9383.2) GND_VOID=TRUE
R9382 1.5K 5% MF 1/20W 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
R9383 1.5K 5% MF 1/20W 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
T29_R2D_N<1>
T29_R2D_P<1>

T29_A_BIAS_R2D_N1 VOLTAGE=3.3V
C9364 0.22UF 20% 6.3V X5R 0201
C9365 0.22UF 20% 6.3V X5R 0201
C9360 0.22UF 20% 6.3V X5R 0201
C9361 0.22UF 20% 6.3V X5R 0201
DP_SDRVA_ML_P<0>
DP_SDRVA_ML_N<0>
DP_SDRVA_ML_P<2>
DP_SDRVA_ML_N<2>

T29 Path Biasing

T29_D2R_C_P<0> IN
T29_D2R_C_N<0> IN
T29_D2R_C_P<1> IN
T29_D2R_C_N<1> IN

D9364 BAR90-02LRH TSLP-2-7 GND_VOID=TRUE (D9364.2)
D9372 BAR90-02LRH TSLP-2-7
D9373 BAR90-02LRH TSLP-2-7
D9365 BAR90-02LRH TSLP-2-7
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY

T29: TX_0
T29DPA_ML_C_P<0> OUT
T29DPA_ML_C_N<0> OUT
GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)
R9374 1.5K 5% MF 1/20W 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
R9375 1.5K 5% MF 1/20W 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY

D9360 BAR90-02LRH TSLP-2-7 GND_VOID=TRUE (D9360.2)
D9382 BAR90-02LRH TSLP-2-7
D9383 BAR90-02LRH TSLP-2-7
D9361 BAR90-02LRH TSLP-2-7
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)

T29: TX_1
T29DPA_ML_C_P<2> OUT
T29DPA_ML_C_N<2> OUT
GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)
R9384 1.5K 5% MF 1/20W 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
R9385 1.5K 5% MF 1/20W 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY

DP Path Biasing

R9361 1.5K 5% MF 1/20W 201 DP_A_BIAS_N_2 VOLTAGE=3.3V R9362 51 5% 1/20W MF 201
R9360 1.5K 5% MF 1/20W 201 DP_A_BIAS_P_2 VOLTAGE=3.3V R9363 51 5% 1/20W MF 201
R9365 1.5K 5% MF 1/20W 201 DP_A_BIAS_N_0 VOLTAGE=3.3V R9366 51 5% 1/20W MF 201
R9364 1.5K 5% MF 1/20W 201 DP_A_BIAS_P_0 VOLTAGE=3.3V R9367 51 5% 1/20W MF 201

Both R's:
C9358 0.1UF 10% 16V X5R-CERM 0201

=PP3V3_S0_DPSDRVA
C9359 0.1UF 10% 16V X5R 402
DP_A_PWRDWN
CRITICAL U9359 74LVC1G04DBVCK SC70
DP_A_BIAS

IC supports input high while Vcc = 0V.

DP/T29 A Low-Speed MUX

PP3V3_SW_DPAPWR
Must be 3.3V DP A port power

C9390 0.1UF 10% 16V X5R 402
C9391 0.1UF 10% 16V X5R 402

U9390 CBTL04DP081 HVQFN OMIT CRITICAL

DP_SDRVA_ML_N<3>	31	DIN1_0+	DOUT_0+
DP_SDRVA_ML_P<3>	30	DIN1_0-	DOUT_0-
DP_SDRVA_ML_N<1>	27	DIN1_1+	DOUT_1+
DP_SDRVA_ML_P<1>	26	DIN1_1-	DOUT_1-
DP_SDRVA_AUXCH_P	19	AUX1+	AUX+
DP_SDRVA_AUXCH_N	18	AUX1-	AUX-
DP_SDRVA_HPD	17	HPD_1	HPD_IN
T29_A_RSVD_N	25	DIN2_0+	
T29_A_RSVD_P	24	DIN2_0-	
(T29_A_LSX_P2R)	23	DIN2_1+	
(T29_A_LSX_R2P)	22	DIN2_1-	
T29_D2R1_BIASP	15	AUX2+	
T29_D2R1_BIASN	14	AUX2-	
NC	13	HPD_2	
DP_A_PWRDWN	10	GPU_SEL	
T29_A_BIAS	32	AUX_SEL	LO=Port A HI=Port B
	11	NC	
	29, 20, 16, 12, 9, 3	VDD	
	33, 28, 21	THMPAD, GND	

CKPLUS_WAIVE=NdifPr_badTerm

R9399 100K 5% 1/16W MF-LF 402
T29DPA_ML_N<3> OUT
T29DPA_ML_P<3> OUT
T29: Unused
T29DPA_ML_N<1> OUT
T29DPA_ML_P<1> OUT
T29: LSX_A_R2P/P2R (P/N)
DP_A_EXT_AUXCH_P OUT
DP_A_EXT_AUXCH_N OUT
T29: RX_1 Bias Sink
DP_A_EXT_HPD IN
R9398 100K 5% 1/16W MF-LF 402

T29 R9392 51 5% 1/16W MF-LF 402
T29 R9393 51 5% 1/16W MF-LF 402

T29 R9396 1K 5% 1/16W MF-LF 402
T29 R9397 1K 5% 1/16W MF-LF 402

CBTL04DP081 (353S3151) and PI3VEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

SIGNAL_MODEL=T29DP_MUX

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

Port A MCU

PP3V3_SW_DPAPWR
Must be 3.3V DP A port power

C9330 0.1UF 20% 16V CERM 402
C9331 0.1UF 20% 16V CERM 402

CRITICAL U9330 LPC1112A HVQFN25 VDD OMIT

DP_A_CA_DET	1	RESET#/PIO0_0	R/PIO1_0/AD1
T29_LSEO<0>	7	PIO0_1/CLKOUT	R/PIO1_1/AD2
		PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3
=I2C_T29AMCU_SCL	8	PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4
=I2C_T29AMCU_SDA	9	PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP
T29DPA_HPD	10	PIO0_6/SCK	PIO1_6/RXD
T29_A_BIAS	11	PIO0_7/CTS#	PIO1_7/TXD
T29_LSOE<0>	12	PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0
T29_LSOE<1>	13	PIO0_9/MOSI/CT16B0_MAT1	
	14	SWCLK/PIO0_10/SCK/CT16B0_MAT2	(OD)
T29_MCU_INT_L	15	R/PIO0_11/AD0	(OD) XTALIN
	4		
	3, 21, 25	VSS	THRM PAD

T29DPA_CONFIG1_RC
T29DPA_CONFIG2_RC
T29_A_HV_EN_R
T29_A_UC_ADDR
DP_A_EXT_HPD
T29_A_LSX_P2R (P2R = PLUG TO RECEPTACLE)
T29_A_LSX_R2P (R2P = RECEPTACLE TO PLUG)
T29_LSEO<1>

I2C Addr: 0x26/0x27 (Wr/Rd)

T29 R9338 10K 5% 1/16W MF-LF 402
T29 R9334 10K 5% 1/16W MF-LF 402 T29_A_HV_EN

T29 R9339 1M 5% 1/16W MF-LF 402

NO_T29 R9378 T29_A_BIAS 0 5% MF 1/20W 201
NO_T29 R9380 T29DPA_CONFIG1_RC 0 5% MF 1/20W 201 DP_A_CA_DET
NO_T29 R9379 T29DPA_HPD 0 5% MF 1/20W 201 DP_A_EXT_HPD
NO_T29 R9381 DP_A_PWRDWN 0 5% MF 1/20W 201

SYNC_MASTER=K62 SYNC_DATE=11/14/2016
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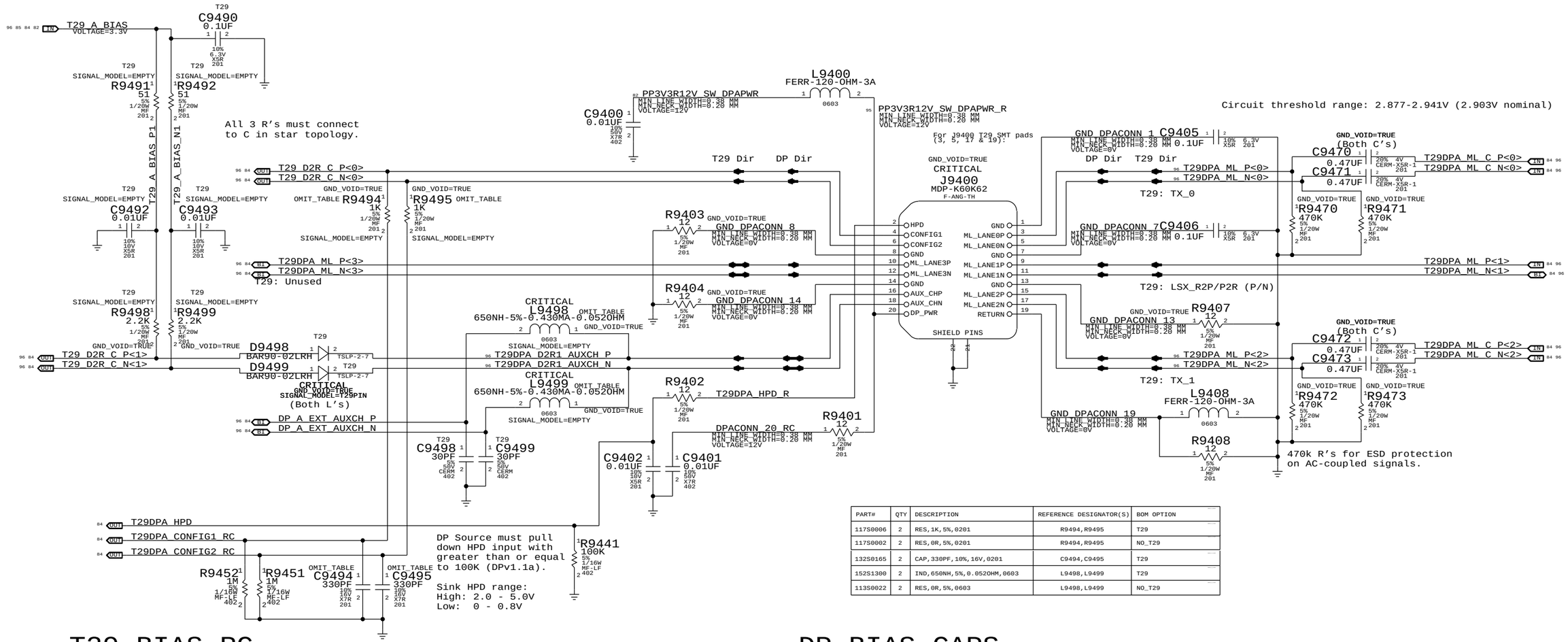
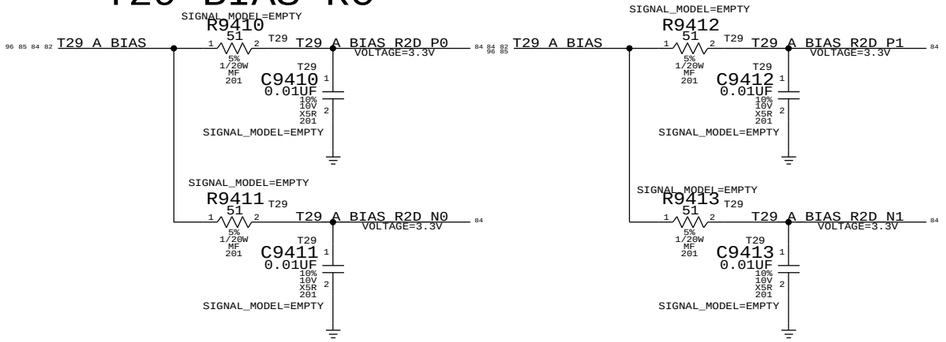
DisplayPort/T29 A Connector

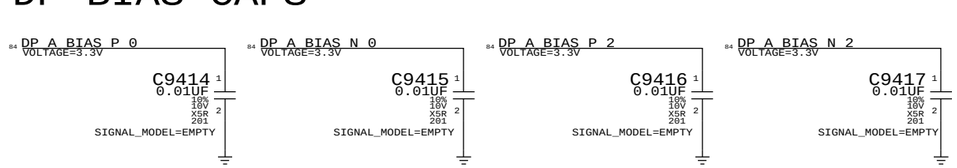


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0006	2	RES,1K,5%,0201	R9494,R9495	T29
117S0002	2	RES,0R,5%,0201	R9494,R9495	NO_T29
132S0165	2	CAP,330PF,10%,16V,0201	C9494,C9495	T29
152S1300	2	IND,650NH,5%,0.052OHM,0603	L9498,L9499	T29
113S0022	2	RES,0R,5%,0603	L9498,L9499	NO_T29

T29 BIAS RC



DP BIAS CAPS



SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE: DisplayPort/T29 A Connector

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DRAWING NUMBER: 051-8115 SIZE: D

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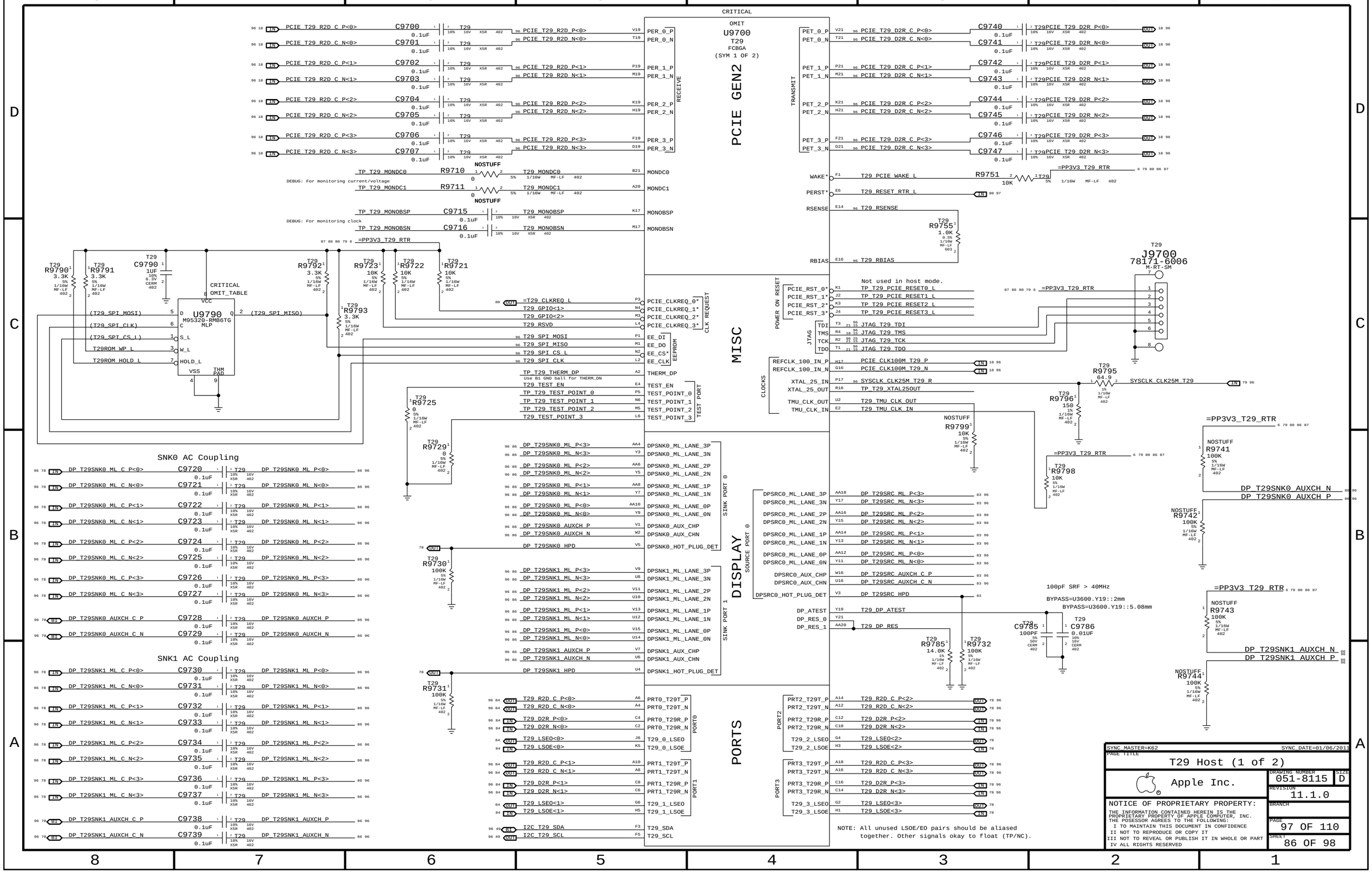
CRITICAL
OMIT
U9700
T29
FCBGA
(SYM 1 OF 2)
PCIE GEN2
RECEIVE
TRANSMIT
PCIE_T29_R2D_C_P<0>
PCIE_T29_R2D_C_N<0>
PCIE_T29_R2D_C_P<1>
PCIE_T29_R2D_C_N<1>
PCIE_T29_R2D_C_P<2>
PCIE_T29_R2D_C_N<2>
PCIE_T29_R2D_C_P<3>
PCIE_T29_R2D_C_N<3>
PCIE_T29_R2D_P<0>
PCIE_T29_R2D_N<0>
PCIE_T29_R2D_P<1>
PCIE_T29_R2D_N<1>
PCIE_T29_R2D_P<2>
PCIE_T29_R2D_N<2>
PCIE_T29_R2D_P<3>
PCIE_T29_R2D_N<3>
PER_0_P
PER_0_N
PER_1_P
PER_1_N
PER_2_P
PER_2_N
PER_3_P
PER_3_N
PET_0_P
PET_0_N
PET_1_P
PET_1_N
PET_2_P
PET_2_N
PET_3_P
PET_3_N
PCIE_T29_D2R_C_P<0>
PCIE_T29_D2R_C_N<0>
PCIE_T29_D2R_C_P<1>
PCIE_T29_D2R_C_N<1>
PCIE_T29_D2R_C_P<2>
PCIE_T29_D2R_C_N<2>
PCIE_T29_D2R_C_P<3>
PCIE_T29_D2R_C_N<3>
PCIE_T29_D2R_P<0>
PCIE_T29_D2R_N<0>
PCIE_T29_D2R_P<1>
PCIE_T29_D2R_N<1>
PCIE_T29_D2R_P<2>
PCIE_T29_D2R_N<2>
PCIE_T29_D2R_P<3>
PCIE_T29_D2R_N<3>
NOSTUFF
TP_T29_MONDC0
TP_T29_MONDC1
TP_T29_MONOBSP
TP_T29_MONOBSN
MONDC0
MONDC1
MONOBSP
MONOBSN
DEBUG: For monitoring current/voltage
DEBUG: For monitoring clock
=PP3V3_T29_RTR
WAKE*
PERST*
RSENSE
RBIAS
T29_PCIE_WAKE_L
T29_RESET_RTR_L
T29_RSENSE
T29_RBIAS
MISC
CLK REQUEST
PCIE_CLKREQ_0*
PCIE_CLKREQ_1*
PCIE_CLKREQ_2*
PCIE_CLKREQ_3*
T29_GPIO<1>
T29_GPIO<2>
T29_RSVD
EEPROM
EE_DI
EE_DO
EE_CS*
EE_CLK
T29_SPI_MOSI
T29_SPI_MISO
T29_SPI_CS_L
T29_SPI_CLK
THERM_DP
TP_T29_THERM_DP
Use B1 GND ball for THERM_DN
TEST PORT
TEST_EN
TEST_POINT_0
TEST_POINT_1
TEST_POINT_2
TEST_POINT_3
T29_TEST_EN
T29_TEST_POINT_0
T29_TEST_POINT_1
T29_TEST_POINT_2
T29_TEST_POINT_3
POWER ON RESET
PCIE_RST_0*
PCIE_RST_1*
PCIE_RST_2*
PCIE_RST_3*
Not used in host mode.
TP_T29_PCIE_RESET0_L
TP_T29_PCIE_RESET1_L
TP_T29_PCIE_RESET2_L
TP_T29_PCIE_RESET3_L
JTAG
TDI
TMS
TCK
TDO
JTAG_T29_TDI
JTAG_T29_TMS
JTAG_T29_TCK
JTAG_T29_TDO
CLOCKS
REFCLK_100_IN_P
REFCLK_100_IN_N
XTAL_25_IN
XTAL_25_OUT
TMU_CLK_IN
TMU_CLK_OUT
PCIE_CLK100M_T29_P
PCIE_CLK100M_T29_N
SYSCLK_CLK25M_T29_R
TP_T29_XTAL25OUT
T29_TMU_CLK_OUT
T29_TMU_CLK_IN
SYSCLK_CLK25M_T29
DISPLAY
SOURCE PORT 0
SINK PORT 0
SINK PORT 1
DPSRC0_ML_LANE_3P
DPSRC0_ML_LANE_3N
DPSRC0_ML_LANE_2P
DPSRC0_ML_LANE_2N
DPSRC0_ML_LANE_1P
DPSRC0_ML_LANE_1N
DPSRC0_ML_LANE_0P
DPSRC0_ML_LANE_0N
DPSRC0_AUX_CHP
DPSRC0_AUX_CHN
DPSRC0_HOT_PLUG_DET
T29_DP_SRC_ML_P<3>
T29_DP_SRC_ML_N<3>
T29_DP_SRC_ML_P<2>
T29_DP_SRC_ML_N<2>
T29_DP_SRC_ML_P<1>
T29_DP_SRC_ML_N<1>
T29_DP_SRC_ML_P<0>
T29_DP_SRC_ML_N<0>
T29_DP_SRC_AUXCH_C_P
T29_DP_SRC_AUXCH_C_N
T29_DP_SRC_HPD
DP_ATEST
DP_RES_0
DP_RES_1
T29_DP_ATEST
T29_DP_RES
100pF SRF > 40MHz
BYPASS=U3600.Y19::2mm
BYPASS=U3600.Y19::5.08mm
PORTS
PORT0
PORT1
PORT2
PORT3
T29_R2D_C_P<0>
T29_R2D_C_N<0>
T29_R2D_P<0>
T29_R2D_N<0>
T29_LSEO<0>
T29_LSOE<0>
T29_R2D_C_P<1>
T29_R2D_C_N<1>
T29_R2D_P<1>
T29_R2D_N<1>
T29_LSEO<1>
T29_LSOE<1>
T29_R2D_C_P<2>
T29_R2D_C_N<2>
T29_R2D_P<2>
T29_R2D_N<2>
T29_LSEO<2>
T29_LSOE<2>
T29_R2D_C_P<3>
T29_R2D_C_N<3>
T29_R2D_P<3>
T29_R2D_N<3>
T29_LSEO<3>
T29_LSOE<3>
I2C_T29_SDA
I2C_T29_SCL
NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).
SNK0 AC Coupling
SNK1 AC Coupling
DP_T29SNK0_ML_C_P<0>
DP_T29SNK0_ML_C_N<0>
DP_T29SNK0_ML_C_P<1>
DP_T29SNK0_ML_C_N<1>
DP_T29SNK0_ML_C_P<2>
DP_T29SNK0_ML_C_N<2>
DP_T29SNK0_ML_C_P<3>
DP_T29SNK0_ML_C_N<3>
DP_T29SNK0_AUXCH_C_P
DP_T29SNK0_AUXCH_C_N
DP_T29SNK1_ML_C_P<0>
DP_T29SNK1_ML_C_N<0>
DP_T29SNK1_ML_C_P<1>
DP_T29SNK1_ML_C_N<1>
DP_T29SNK1_ML_C_P<2>
DP_T29SNK1_ML_C_N<2>
DP_T29SNK1_ML_C_P<3>
DP_T29SNK1_ML_C_N<3>
DP_T29SNK1_AUXCH_C_P
DP_T29SNK1_AUXCH_C_N
DP_T29SNK0_ML_P<3>
DP_T29SNK0_ML_N<3>
DP_T29SNK0_ML_P<2>
DP_T29SNK0_ML_N<2>
DP_T29SNK0_ML_P<1>
DP_T29SNK0_ML_N<1>
DP_T29SNK0_ML_P<0>
DP_T29SNK0_ML_N<0>
DP_T29SNK0_AUXCH_P
DP_T29SNK0_AUXCH_N
DP_T29SNK0_HPD
DP_T29SNK1_ML_P<3>
DP_T29SNK1_ML_N<3>
DP_T29SNK1_ML_P<2>
DP_T29SNK1_ML_N<2>
DP_T29SNK1_ML_P<1>
DP_T29SNK1_ML_N<1>
DP_T29SNK1_ML_P<0>
DP_T29SNK1_ML_N<0>
DP_T29SNK1_AUXCH_P
DP_T29SNK1_AUXCH_N
DP_T29SNK1_HPD
DPSNK0_ML_LANE_3P
DPSNK0_ML_LANE_3N
DPSNK0_ML_LANE_2P
DPSNK0_ML_LANE_2N
DPSNK0_ML_LANE_1P
DPSNK0_ML_LANE_1N
DPSNK0_ML_LANE_0P
DPSNK0_ML_LANE_0N
DPSNK0_AUX_CHP
DPSNK0_AUX_CHN
DPSNK0_HOT_PLUG_DET
DPSNK1_ML_LANE_3P
DPSNK1_ML_LANE_3N
DPSNK1_ML_LANE_2P
DPSNK1_ML_LANE_2N
DPSNK1_ML_LANE_1P
DPSNK1_ML_LANE_1N
DPSNK1_ML_LANE_0P
DPSNK1_ML_LANE_0N
DPSNK1_AUX_CHP
DPSNK1_AUX_CHN
DPSNK1_HOT_PLUG_DET
T29_SDA
T29_SCL
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Apple Inc.
SYNC_MASTER=K62
SYNC_DATE=01/06/2013
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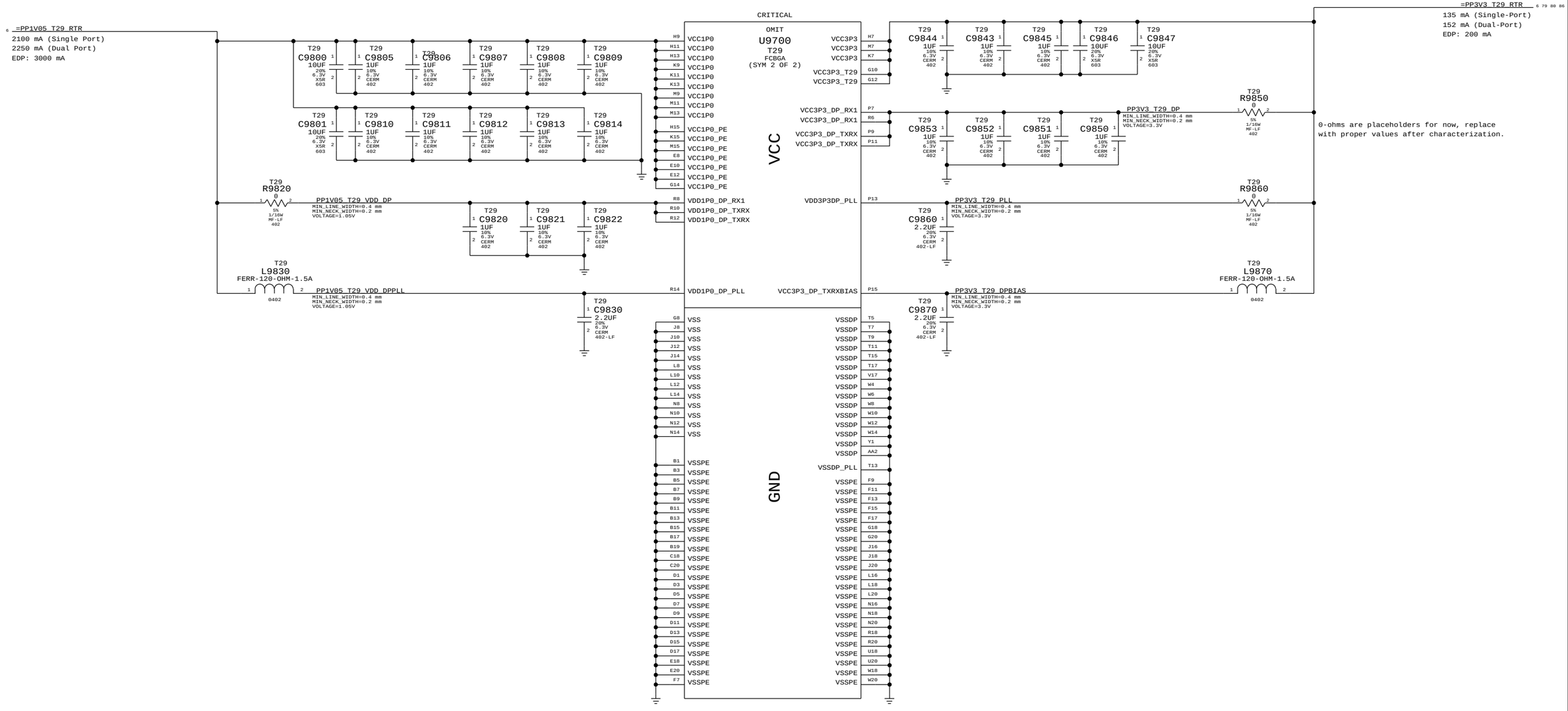

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

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K60/62 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	TOP,BOTTOM	Y	0.21 MM	0.090 MM	=STANDARD		
34_OHM_SE	*	Y	0.19 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.090 MM	=STANDARD		
39_OHM_SE	*	Y	0.159 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	TOP,BOTTOM	Y	0.151 MM	0.090 MM	=STANDARD		
42_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
68_OHM_DIFF	ISL3,ISL6	Y	0.16 MM	0.090 MM	=STANDARD	0.13 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.090 MM	=STANDARD	0.13 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.115 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.2 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.081 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL6	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_CTL	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
3.5:1_SPACING	*	0.35 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?
6:1_SPACING	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.8 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.155 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.145 MM	?
3X_DIELECTRIC	*	0.230 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.215 MM	?
4X_DIELECTRIC	*	0.305 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.285 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.355 MM	?
7X_DIELECTRIC	*	0.532 MM	?
7X_DIELECTRIC	TOP,BOTTOM	0.497 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P1P5MM	*	0.15 MM	?
BGA_P2MM	*	0.2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P1P5MM
CLK_PCIE	*	BGA	BGA_P1MM
CLK_LPC	*	BGA	BGA_P1MM
CLK_PCI	*	BGA	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CONTROL	*	*	SWITCHNODE
VR_CONTROL	VR_CONTROL	*	STANDARD
VR_CONTROL	SWITCHNODE	*	STANDARD
VR_CONTROL	GND	*	STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

BOARD STACK-UP

TOP	HALF OZ	SIGNAL
	0.071	PREPREG
2	TWO OZ	GND
	0.076	PREPREG
3	ONE OZ	SIGNAL
	0.370	PREPREG
4	TWO OZ	POWER
	0.101	CORE
5	TWO OZ	POWER
	0.370	PREPREG
6	ONE OZ	SIGNAL
	0.076	PREPREG
7	TWO OZ	GND
	0.071	PREPREG
BOTTOM	HALF OZ	SIGNAL

BOARD THICKNESS = 62 MIL (1.5748 mm)

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: K60/K62 RULE DEFINITIONS

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
MEM_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
MEM_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
MEM_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF
MEM_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2.5:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=2:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DQ_SAMEBYTE	*	=3:1_SPACING	?
MEM_DQ_DIFFBYTE	*	=5:1_SPACING	?
MEM_DATA2MEM	*	=4:1_SPACING	?
MEM_DQS2MEM	*	=4:1_SPACING	?
MEM_2OTHER	*	=5:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE0	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE1	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE2	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE3	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE4	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE5	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE6	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE7	*	MEM_DQS2MEM
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE5	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE5	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE5	MEM_DQ_BYTE5	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE5	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE5	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE5	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE6	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE6	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE6	MEM_DQ_BYTE6	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE6	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE6	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE7	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE7	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE7	MEM_DQ_BYTE7	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE7	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE0	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE0	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE0	MEM_DQ_BYTE0	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE1	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE2	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE3	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE1	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE1	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE1	MEM_DQ_BYTE1	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE2	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE3	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE2	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE2	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE2	MEM_DQ_BYTE2	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE3	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE3	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE3	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE3	MEM_DQ_BYTE3	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE4	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE4	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE4	MEM_DQ_BYTE4	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE4	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE4	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE4	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE4	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_68D	MEM_CLK	MEM_A_CLK_P<3..0>	12 32
	MEM_68D	MEM_CLK	MEM_A_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_A_CKE<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_CS_L<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_ODT<3..0>	12 30
	MEM_34S	MEM_CMD	MEM_A_A<15..0>	12 30
	MEM_34S	MEM_CMD	MEM_A_BA<2..0>	12 30
	MEM_34S	MEM_CMD	MEM_A_RAS_L	12 30
	MEM_34S	MEM_CMD	MEM_A_CAS_L	12 30
	MEM_34S	MEM_CMD	MEM_A_WE_L	12 30
	MEM_42S	MEM_DQ_BYTE0	MEM_A_DQ<7..0>	12 32
	MEM_42S	MEM_DQ_BYTE1	MEM_A_DQ<15..8>	12 32
	MEM_42S	MEM_DQ_BYTE2	MEM_A_DQ<23..16>	12 32
	MEM_42S	MEM_DQ_BYTE3	MEM_A_DQ<31..24>	12 32
	MEM_42S	MEM_DQ_BYTE4	MEM_A_DQ<39..32>	12 32
	MEM_42S	MEM_DQ_BYTE5	MEM_A_DQ<47..40>	12 32
	MEM_42S	MEM_DQ_BYTE6	MEM_A_DQ<55..48>	12 32
	MEM_42S	MEM_DQ_BYTE7	MEM_A_DQ<63..56>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<7>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<7>	12 32
H17	MEM_50S	PM	MEM_RESET_L	30 31 32 97

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_68D	MEM_CLK	MEM_B_CLK_P<3..0>	12 32
	MEM_68D	MEM_CLK	MEM_B_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_B_CKE<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_CS_L<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_ODT<3..0>	12 31
	MEM_34S	MEM_CMD	MEM_B_A<15..0>	12 31
	MEM_34S	MEM_CMD	MEM_B_BA<2..0>	12 31
	MEM_34S	MEM_CMD	MEM_B_RAS_L	12 31
	MEM_34S	MEM_CMD	MEM_B_CAS_L	12 31
	MEM_34S	MEM_CMD	MEM_B_WE_L	12 31
	MEM_42S	MEM_DQ_BYTE0	MEM_B_DQ<7..0>	12 32
	MEM_42S	MEM_DQ_BYTE1	MEM_B_DQ<15..8>	12 32
	MEM_42S	MEM_DQ_BYTE2	MEM_B_DQ<23..16>	12 32
	MEM_42S	MEM_DQ_BYTE3	MEM_B_DQ<31..24>	12 32
	MEM_42S	MEM_DQ_BYTE4	MEM_B_DQ<39..32>	12 32
	MEM_42S	MEM_DQ_BYTE5	MEM_B_DQ<47..40>	12 32
	MEM_42S	MEM_DQ_BYTE6	MEM_B_DQ<55..48>	12 32
	MEM_42S	MEM_DQ_BYTE7	MEM_B_DQ<63..56>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<7>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<7>	12 32

MEMORY MISC PROPERTIES

VOLTAGE	NET_TYPE PHYSICAL	NET_TYPE SPACING	VOLTAGE		
	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_A	
	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_B	
H167	MEM_POWER_PHY	MEM_POWER		CPU_DDR_VREF	11 28
H168	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMA_DACOUT	28
H169	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMA_OPFB	28
H170	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMA_DQ	28
H171	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_A_SW	
H172	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMB_DACOUT	28
H173	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMB_OPFB	28
H174	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMB_DQ	28
H175	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_B_SW	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	=3:1_SPACING	?

SYNC_MASTER=K60_ROSITA SYNC_DATE=01/06/2011

PAGE TITLE: Memory Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4:1_SPACING	?

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_RCOMP_PHY	*	Y	0.254 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP	*	0.2 MM	?
CPU_RCOMP	*	0.2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=6:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=6:1_SPACING	?

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
SATA				
H50	SATA_90D	SATA	SATA_SSD_R2D_C_P	18 42
F50	SATA_90D	SATA	SATA_SSD_R2D_C_N	18 42
H51	SATA_90D	SATA	SATA_SSD_R2D_P	42
H52	SATA_90D	SATA	SATA_SSD_R2D_N	42
H53	SATA_90D	SATA	SATA_SSD_D2R_P	18 42
H54	SATA_90D	SATA	SATA_SSD_D2R_N	18 42
H55	SATA_90D	SATA	SATA_SSD_D2R_C_P	42
H56	SATA_90D	SATA	SATA_SSD_D2R_C_N	42
PCIE				
H31	PCIE_85D	PCIE	PCIE_USB3_1_R2D_P	
H32	PCIE_85D	PCIE	PCIE_USB3_1_R2D_N	
F27	PCIE_85D	PCIE	PCIE_USB3_1_R2D_C_P	
H33	PCIE_85D	PCIE	PCIE_USB3_1_R2D_C_N	
H34	PCIE_85D	PCIE	PCIE_USB3_1_D2R_P	
F28	PCIE_85D	PCIE	PCIE_USB3_1_D2R_N	
H35	PCIE_85D	PCIE	PCIE_USB3_1_D2R_C_P	
H36	PCIE_85D	PCIE	PCIE_USB3_1_D2R_C_N	
H37	PCIE_85D	PCIE	PCIE_USB3_2_R2D_P	
H38	PCIE_85D	PCIE	PCIE_USB3_2_R2D_N	
H39	PCIE_85D	PCIE	PCIE_USB3_2_R2D_C_P	
H40	PCIE_85D	PCIE	PCIE_USB3_2_R2D_C_N	
F29	PCIE_85D	PCIE	PCIE_USB3_2_D2R_P	
H41	PCIE_85D	PCIE	PCIE_USB3_2_D2R_N	
H42	PCIE_85D	PCIE	PCIE_USB3_2_D2R_C_P	
H43	PCIE_85D	PCIE	PCIE_USB3_2_D2R_C_N	
CPU ITP				
F45	CPU_50S	CPU_ITP	XDP_BPM_L<7..0>	11 25
H45	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 15 25
H44	CPU_50S	CPU_ITP	XDP_OBSDATA_B<3..0>	25
H44	CPU_50S	CPU_ITP	XDP_CPU_CFG<0>	25
H48	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 25
F47	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 25
H46	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 25
H47	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 25
H50	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 25
CPU_MISC				
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_PEG_COMP	10

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
PCIE GRAPHICS				
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	9 77
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	9 77
	PCIE_85D	PCIE	PEG_D2R_P<15..0>	9 77
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	9 77
	PCIE_85D	PCIE	MXM_PCIE_R2D_P<7..0>	75 77
	PCIE_85D	PCIE	MXM_PCIE_R2D_N<7..0>	75 77
	PCIE_85D	PCIE	MXM_PCIE_D2R_P<7..0>	75 77
	PCIE_85D	PCIE	MXM_PCIE_D2R_N<7..0>	75 77
PCIE I/O				
	PCIE_85D	PCIE	PCIE_MINI_R2D_P	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_N	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_N	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_N	18 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	18 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_P	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
DMI				
H15	CLK_PCIE_90D	CLK_PCIE	DMI_MIDBUS_CLK100M_N	
H15	CLK_PCIE_90D	CLK_PCIE	DMI_MIDBUS_CLK100M_P	
H16	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	11 18
H17	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	11 18
	PCIE_85D	PCIE	DMI_S2N_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_S2N_N<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_N<3..0>	10 19
PCIE REF CLOCKS				
	CLK_PCIE_90D	CLK_PCIE	GPU_CLK100M_PCIE_P	9
	CLK_PCIE_90D	CLK_PCIE	GPU_CLK100M_PCIE_N	9
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_MINI_P	18 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_MINI_N	18 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	18 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	18 39
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_P	18 37
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_N	18 37
SATA				
	SATA_90D	SATA	SATA_HDD_R2D_C_P	18 42
	SATA_90D	SATA	SATA_HDD_R2D_C_N	18 42
	SATA_90D	SATA	SATA_HDD_R2D_P	42
	SATA_90D	SATA	SATA_HDD_R2D_N	42
	SATA_90D	SATA	SATA_HDD_D2R_P	18 42
	SATA_90D	SATA	SATA_HDD_D2R_N	18 42
	SATA_90D	SATA	SATA_HDD_D2R_C_P	42
	SATA_90D	SATA	SATA_HDD_D2R_C_N	42
	SATA_90D	SATA	SATA_ODD_R2D_C_P	18 42
	SATA_90D	SATA	SATA_ODD_R2D_C_N	18 42
	SATA_90D	SATA	SATA_ODD_R2D_P	42
	SATA_90D	SATA	SATA_ODD_R2D_N	42
	SATA_90D	SATA	SATA_ODD_D2R_P	18 42
	SATA_90D	SATA	SATA_ODD_D2R_N	18 42
	SATA_90D	SATA	SATA_ODD_D2R_C_P	42
	SATA_90D	SATA	SATA_ODD_D2R_C_N	42
CLOCKS				
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_DMI_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_DMI_N	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	18 26
	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	18 25
	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	18 25
	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 18
	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 18
H37	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	25
H38	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	25
UNUSED CLOCKS				
H35	CLK_PCIE_90D	CLK_PCIE	TP_CLK133M_PCH_N	26
H36	CLK_PCIE_90D	CLK_PCIE	TP_CLK133M_PCH_P	26
UNUSED PCIE				
H39	PCIE_85D	PCIE	MXM_PCIE_R2D_P<8..15>	75 77
H40	PCIE_85D	PCIE	MXM_PCIE_R2D_N<8..15>	75 77
H42	PCIE_85D	PCIE	MXM_PCIE_D2R_P<8..15>	75 77
H43	PCIE_85D	PCIE	MXM_PCIE_D2R_N<8..15>	75 77

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PCIE/DMI/FDI/SATA CONSTRAINTS

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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	0.2 MM	?
ITP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

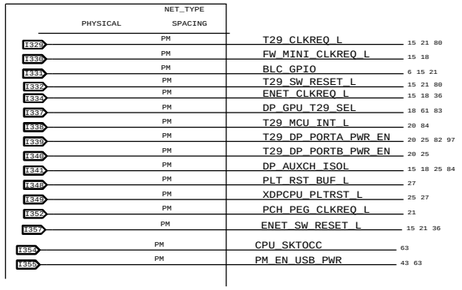
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

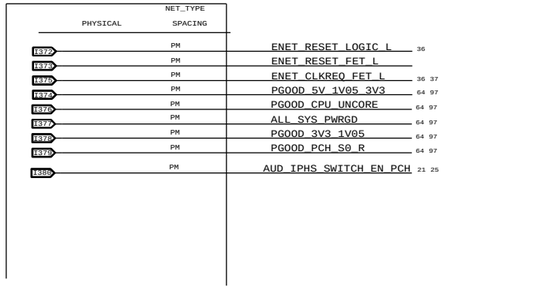
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

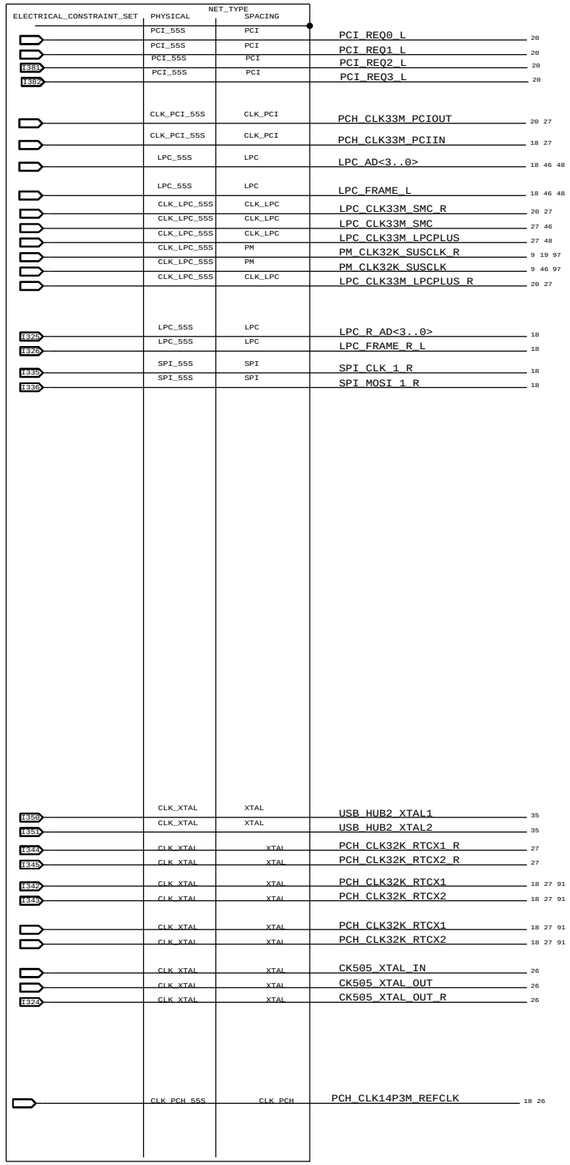
XTAL Constraints

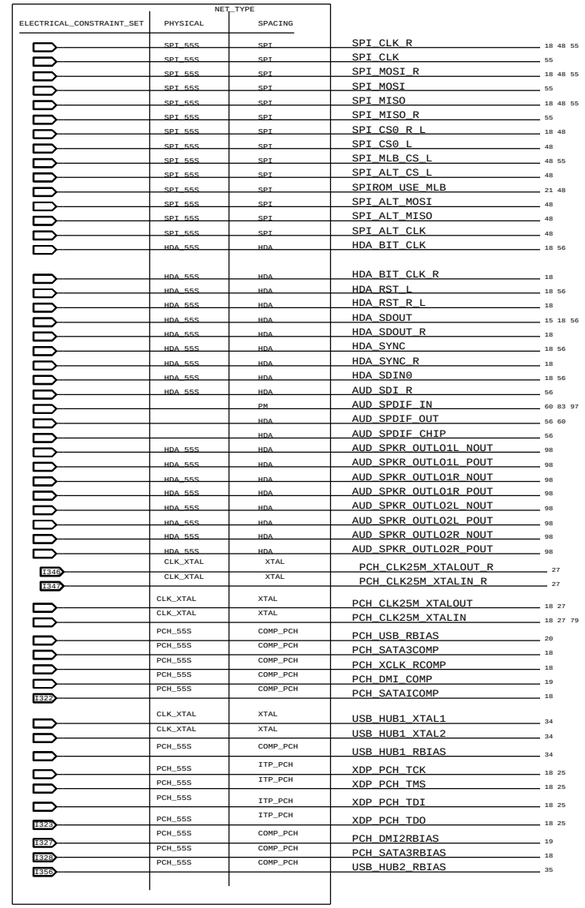
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?









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IBEX PEAK CONSTRAINTS

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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

SOURCE:BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_2OTHER	*	=50MIL_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
50MIL_SPACING	*	1.27 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_DIFF_T	*	*	ENET_2OTHER

CAESAR IV (SD) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD	*	=3:1_SPACING	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

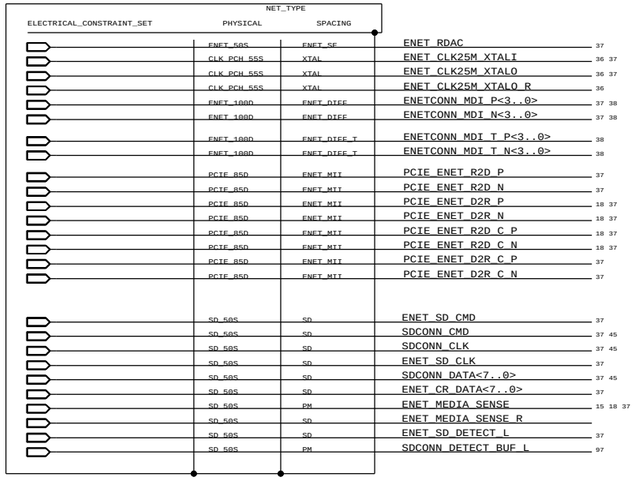
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

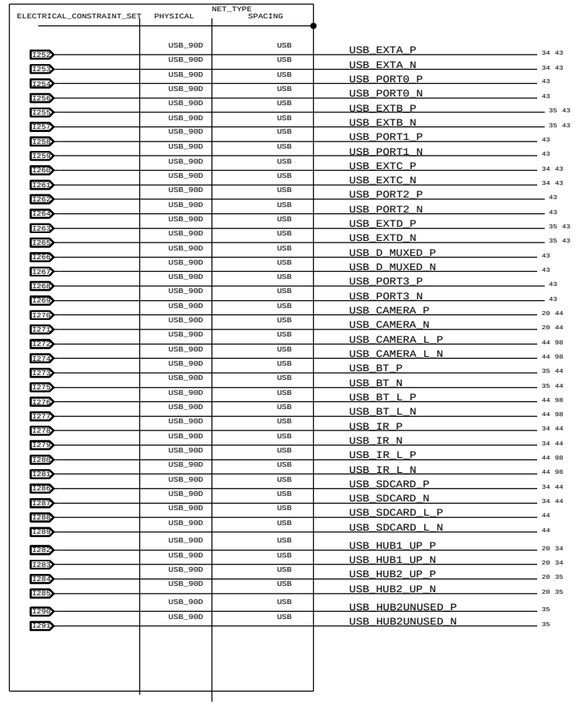
USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

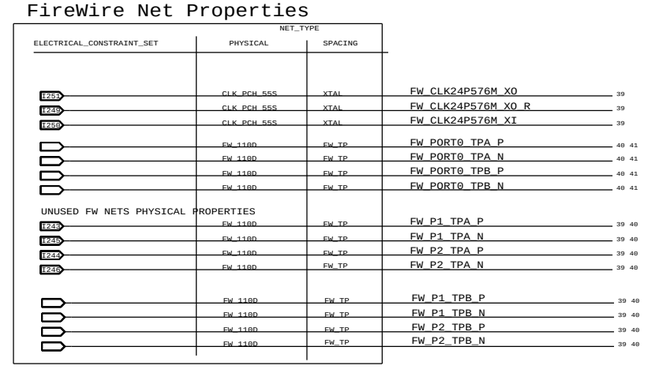
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?





FireWire Net Properties



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USB/ENET/SD/FW/AUD CONSTRAINTS

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GRAPHICS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

USE 5X_DIELECTRIC IN K62

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL_CONSTRAINT_SET
ASSINGED IN CONT. MGR.

NET_TYPE	PHYSICAL	SPACING	
I16O	DP_85D	DISPLAYPORT	DP_INTCONN_ML_C_P<3..0> 83
I17O	DP_85D	DISPLAYPORT	DP_INTCONN_ML_C_N<3..0> 83
	DP_85D	DISPLAYPORT	DP_INTCONN_AUXCH_C_P 83
	DP_85D	DISPLAYPORT	DP_INTCONN_AUXCH_C_N 83
I15O	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0> 81 83
I14O	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0> 81 83
	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P 81 83
	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N 81 83
I18O	DP_85D	DISPLAYPORT	DP_EXTA_ML_P<3..0> 84
I18O	DP_85D	DISPLAYPORT	DP_EXTA_ML_N<3..0> 84
I18O	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_P 84
I18O	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_N 84
I17O	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0> 78 84
I17O	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0> 78 84
I17O	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P 78 84
I17O	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N 78 84
I19O	DP_85D	DISPLAYPORT	DP_EXTB_ML_P<3..0>
I19O	DP_85D	DISPLAYPORT	DP_EXTB_ML_N<3..0>
I19O	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_P
I19O	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_N
I19O	DP_85D	DISPLAYPORT	DP_EXTB_ML_C_P<3..0>
I19O	DP_85D	DISPLAYPORT	DP_EXTB_ML_C_N<3..0>
I19O	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_C_P
I19O	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_C_N
P19O	DP_85D	DISPLAYPORT	MXM_DP_B_ML_P<3..0> 75 78
P20O	DP_85D	DISPLAYPORT	MXM_DP_B_ML_N<3..0> 75 78
P20O	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_P 75 78
P20O	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_N 75 78
P20O	DP_85D	DISPLAYPORT	MXM_DP_C_ML_P<3..0> 75 83
P20O	DP_85D	DISPLAYPORT	MXM_DP_C_ML_N<3..0> 75 83
P20O	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_P 75 83
P20O	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_N 75 83
P21O	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_R_P 83
P21O	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_R_N 83
P20O	DP_85D	DISPLAYPORT	MXM_DP_D_ML_P<3..0> 75 78
P20O	DP_85D	DISPLAYPORT	MXM_DP_D_ML_N<3..0> 75 78
P20O	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_P 75 78
P21O	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_N 75 78

UNUSED VIDEO NET PHYSICAL CONSTRAINTS

	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_P 76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_N 76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_P 76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_N 76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_P<3..0> 76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_N<3..0> 76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_P<3..0> 76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_N<3..0> 76 78

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GRAPHICS CONSTRAINTS

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	49
	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	49
	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	49
	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	49
	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	49
	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	49
	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	49
	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	49
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	49 94
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	49 94
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	49 94
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	49 94
	SMB_55S	SMB	SMBUS_PCH_CLK	18 49
	SMB_55S	SMB	SMBUS_PCH_DATA	18 49
	SMB_55S	SMB	SML_PCH_0_CLK	18 49
	SMB_55S	SMB	SML_PCH_0_DATA	18 49
	SMB_55S	SMB	SML_PCH_1_CLK	18 49
	SMB_55S	SMB	SML_PCH_1_DATA	18 49
	CLK_XTAL	XTAL	SMC_EXTAL	46 47
	CLK_XTAL	XTAL	SMC_XTAL	46 47
I254	SMB_55S	SMB	I2C_VREFMRGN_DIMMA_SCL	28
I253	SMB_55S	SMB	I2C_VREFMRGN_DIMMA_SDA	28
I255	SMB_55S	SMB	I2C_VREFMRGN_DIMMB_SCL	28
I254	SMB_55S	SMB	I2C_VREFMRGN_DIMMB_SDA	28
I265	SMB_55S	SMB	SMB_BLC_TCON_SCL	6 49 81
I264	SMB_55S	SMB	SMB_BLC_TCON_SDA	6 49 81
I268	SMB_55S	SMB	I2C_TCON_SCL	81
I269	SMB_55S	SMB	I2C_TCON_SDA	81
I266	SMB_55S	SMB	SMB_BLC_PCH_SCL_R	6
I267	SMB_55S	SMB	SMB_BLC_PCH_SDA_R	6

SMC THERMAL NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	THERM_DIFF	THERMAL	SNS_T1_1_P	52
	THERM_DIFF	THERMAL	SNS_T1_1_N	52
	THERM_DIFF	THERMAL	SNS_T2_DP2	52
	THERM_DIFF	THERMAL	SNS_T2_DN2	52
I209	THERM_DIFF	THERMAL	SNS_T1_2_P	52
I208	THERM_DIFF	THERMAL	SNS_T1_2_N	52
I207	THERM_DIFF	THERMAL	SNS_T1_3_P	52
I206	THERM_DIFF	THERMAL	SNS_T1_3_N	52
I213	THERM_DIFF	THERMAL	SNS_T1_4_P	52
I212	THERM_DIFF	THERMAL	SNS_T1_4_N	52
I211	THERM_DIFF	THERMAL	SNS_T1_5_P	52
I210	THERM_DIFF	THERMAL	SNS_T1_5_N	52
I215	THERM_DIFF	THERMAL	SNS_T1_6_P	52
I214	THERM_DIFF	THERMAL	SNS_T1_6_N	52
I217	THERM_DIFF	THERMAL	SNS_T1_7_P	52
I216	THERM_DIFF	THERMAL	SNS_T1_7_N	52
I224	THERM_DIFF	THERMAL	SNS_CPU_THERMD_P	10 52
I225	THERM_DIFF	THERMAL	SNS_CPU_THERMD_N	10 52
I219	THERM_DIFF	THERMAL	SNS_LCD_H_P	52
I218	THERM_DIFF	THERMAL	SNS_LCD_H_N	52
	THERM_DIFF	THERMAL	SNS_ODD_P	52 98
	THERM_DIFF	THERMAL	SNS_ODD_N	52 98
	THERM_DIFF	THERMAL	SNS_CPU_H_P	52
	THERM_DIFF	THERMAL	SNS_CPU_H_N	52
I222	THERM_DIFF	THERMAL	SNS_SKIN_RIGHT_P	52 98
I223	THERM_DIFF	THERMAL	SNS_SKIN_RIGHT_N	52 98
	THERM_DIFF	THERMAL	SNS_SKIN_LEFT_P	44 52 98
	THERM_DIFF	THERMAL	SNS_SKIN_LEFT_N	44 52 98
	THERM_DIFF	THERMAL	SNS_AMB_P	52 54 98
	THERM_DIFF	THERMAL	SNS_AMB_N	52 54 98
	THERM_DIFF	THERMAL	SNS_MXM_P	52
	THERM_DIFF	THERMAL	SNS_MXM_N	52
		THERMAL	HDD_OOB_TEMP_FILT	42 51 98
		THERMAL	HDD_OOB_TEMP_FB	42
		THERMAL	HDD_OOB_TEMP_R	51
		THERMAL	SMC_HDD_OOB_TEMP	46 51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	THERM_DIFF	THERMAL	SNS_I_MXM_P	50
	THERM_DIFF	THERMAL	SNS_I_MXM_N	50
	THERM_DIFF	THERMAL	SNS_DIMM_1V5_P	50
	THERM_DIFF	THERMAL	SNS_DIMM_1V5_N	50
	SNS_DIFF	THERMAL	VR_ISNS_VCORE_P	50 95
	SNS_DIFF	THERMAL	VR_ISNS_VCORE_N	50 95
	SNS_DIFF	THERMAL	VR_ISNS_VAXG_P	50 95
	SNS_DIFF	THERMAL	VR_ISNS_VAXG_N	50 95
I243	SNS_DIFF	THERMAL	VR_ISNS_1V05_P	95
I244	SNS_DIFF	THERMAL	VR_ISNS_1V05_N	95
I245	THERM_DIFF	THERMAL	SNS_CPU_1V5_P	50
I246	THERM_DIFF	THERMAL	SNS_CPU_1V5_N	50
I247	THERM_DIFF	THERMAL	SNS_VCCSA_P	50
I248	THERM_DIFF	THERMAL	SNS_VCCSA_N	50
I251	THERM_DIFF	THERMAL	SNS_1V05_PCH_P	50
I252	THERM_DIFF	THERMAL	SNS_1V05_PCH_N	50
I230		THERMAL	GND_SMC_AVSS	46 47 50 94
I241		THERMAL	SMC_CPU_1V5_ISENSE	46 50
I240		THERMAL	SMC_CPU_1V5_ISENSE_R	50
I242		THERMAL	SMC_CPU_1V5_VSENSE	46 50
I229		THERMAL	GND_SMC_AVSS	46 47 50 94
I238		THERMAL	SMC_DIMM_ISENSE	46 50
I228		THERMAL	SMC_DIMM_1V5_R	50
I231		THERMAL	SMC_DIMM_VSENSE	46 50
I229		THERMAL	GND_SMC_AVSS	46 47 50 94
I276		THERMAL	SMC_VCCSA_ISENSE	46 50
I275		THERMAL	SMC_VCCSA_ISENSE_R	50
I277		THERMAL	SMC_VCCSA_VSENSE	46 50
		THERMAL	GND_SMC_AVSS	46 47 50 94
		THERMAL	SMC_PCH_1V05_ISENSE	46 50
		THERMAL	SMC_VAXG_VSENSE	46 50
		THERMAL	SMC_PCH_1V05_VSENSE	46 50
I229		THERMAL	GND_SMC_AVSS	46 47 50 94
I233		THERMAL	SMC_1V05_ISENSE	46 50
I232		THERMAL	SMC_VAXG_ISENSE	46 50
I234		THERMAL	SMC_1V05_VSENSE	46 50
I235		THERMAL	SMC_GPU_ISENSE	46 50
		THERMAL	SMC_GPU_VSENSE	46 50
		THERMAL	SMC_VCORE_ISENSE	46 50
I237		THERMAL	SMC_VCORE_VSENSE	46 50
I239		THERMAL	SMC_CPU_VSENSE	

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NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

NET_TYPE PHYSICAL	SPACING	VOLTAGE		
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE1	66
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE2	66
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE3	66
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE4	
POWER	SWITCHNODE	1.5V	VR_AXG_PHASE1	67
POWER	SWITCHNODE	3.3V	P3V3S5_REG_PHASE	70
POWER	SWITCHNODE	5V	P5VS3_REG_PHASE	70
POWER	SWITCHNODE	1.05V	P1V05S0_PHASE	70
POWER	SWITCHNODE	1.05V	P1V05_REG_PHASE	68
POWER	SWITCHNODE	3.4V	P3V42G3H_SW	72
POWER	SWITCHNODE	3.3V	ENET_3V3_S3_SR_IN	37
POWER	SWITCHNODE	1.2V	ENET_SR_LX	36 37
POWER	SWITCHNODE	1.5V	DDR_REG_PHASE	71
POWER	SWITCHNODE	1.8V	P1V8_REG_PHASE	71
POWER	POWER	0.75V	PP0V75_S3_MEM_VREFCA_A	28 30
POWER	POWER	0.75V	PP0V75_S3_MEM_VREFCA_B	28 31
POWER	POWER	0.75V	PP0V75_S3_MEM_VREFDQ_A	28 30
POWER	POWER	0.75V	PP0V75_S3_MEM_VREFDQ_B	28 31
POWER	POWER	12V	PP12V_S0	6
POWER	POWER	12V	PP12V_S0_CPU_FLTRD	65 66 67
POWER	POWER	12V	PP12V_S0_FAN0_L	53 98
POWER	POWER	12V	PP12V_S0_FAN1_L	53 98
POWER	POWER	12V	PP12V_S0_FAN2_L	54 98
POWER	POWER	12V	VR_CPU_DRV1_PVCC	66
POWER	POWER	12V	VR_CPU_DRV1_UVCC	66
POWER	POWER	12V	VR_CPU_DRV2_PVCC	66
POWER	POWER	12V	VR_CPU_DRV2_UVCC	66
POWER	POWER	12V	VR_CPU_DRV3_PVCC	66
POWER	POWER	12V	VR_CPU_DRV3_UVCC	66
POWER	POWER	12V	VR_CPU_DRV4_PVCC	
POWER	POWER	12V	VR_CPU_DRV4_UVCC	
POWER	POWER	12V	VR_AXG_DRV1_PVCC	67
POWER	POWER	12V	VR_AXG_DRV1_UVCC	
POWER	POWER	12V	VR_CPU_DRV1_VCC	66
POWER	POWER	12V	VR_CPU_DRV2_VCC	66
POWER	POWER	12V	VR_CPU_DRV3_VCC	66
POWER	POWER	12V	VR_CPU_DRV4_VCC	
POWER	POWER	12V	PP12V_S0_VG_OK	41
POWER	POWER	12V	P12V_FW_R	41
POWER	POWER	12V	P12V_FW_CL	41
POWER	POWER	12V	P12V_FW_D	41
POWER	POWER	12V	FW_PORT0_VP	41
POWER	POWER	12V	FW_PORT0_VP_F	41
POWER	POWER	12V	PPVP_FW_PHY_CPS	39 41
POWER	POWER	12V	PP12V_S0_P1V05_VREG_VIN	68
POWER	POWER	12V	VCCSA_PWR_RC	69
POWER	POWER	12V	PP12V_S0_BL_R	
POWER	POWER	12V	PP12V_S5_FET	6 74
POWER	POWER	12V	PP12V_LCD	81
POWER	POWER	12V	PP12V_G3H	6
POWER	POWER	12V	PP12V_S5	6
POWER	POWER	12V	PP12V_S5_RSN	74
POWER	POWER	0.75V	PPVTT_S0_DDR	6
POWER	POWER	0.75V	PP0V75_S0	6
POWER	POWER	0.925V	PPVCCSA_S0_CPU	6
POWER	POWER	1.0V	PP1V0_FW_FWPHY_AVDD	39
POWER	POWER	1.0V	PP1V0_S0_FW_VDD	40
POWER	POWER	1.05V	PP1V05_S0_T29	6
POWER	POWER	1.05V	PP1V05_S0_INPUT_VCCSA	6
POWER	POWER	1.05V	PPVAXG_S0	6
POWER	POWER	1.05V	PP1V05_S0	6
POWER	POWER	1.05V	PP1V05_S0_PCH	6
POWER	POWER	1.05V	PP1V05_S0_CK505_F	26
POWER	POWER	1.05V	PPVOUT_S5_PCH_DCPSUS	22
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA_F	17 22
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F	17 22
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_EXP_F	22 24
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLLDMI2_F	22 24
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_SATA_F	22 24
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCCLKDMI_F	22 24
POWER	POWER	1.1V	PPVCORE_S0_AXG_REG1	67
POWER	POWER	1.1V	PPVCORE_S0_AXG_REGOUT	67
POWER	POWER	1.1V	PPVCORE_S0_CPU	6
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG1	66
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG2	66
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG3	66
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG4	
VR_CTL_PHY	VR_CTL	1.2V	PP1V2_S3_ENET_INTREG	36
POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_AVDDL	37
POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_PCIEPLL	37
POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_GPHYPLL	37
POWER	POWER	1.5V	PP1V5_S0	6
POWER	POWER	1.5V	PP1V5_S0_CK505_F	26
POWER	POWER	1.5V	PP1V5_S0_CK505_R	26
POWER	POWER	1.5V	PP1V5_S0_CPU_MEM	6
POWER	POWER	1.5V	PP1V5_S0_CPU_SNS	
POWER	POWER	1.5V	PP1V5_S3	6
POWER	POWER	1.5V	PP1V5_S3_MEM	6

POWER NET PROPERTIES

NET_TYPE PHYSICAL	SPACING	VOLTAGE		
POWER	POWER	12V	PP12V_S0_MXM	6
POWER	POWER	12V	PP12V_SLG1	
POWER	POWER	12V	PP3V3R12V_SW_DPAPWR_1	
POWER	POWER	12V	PP3V3R12V_SW_DPBPWR_1	
POWER	POWER	1.8V	USB_HUB2_VDD1V8	35
POWER	POWER	1.8V	USB_HUB2_VDD1V8PLL	35
POWER	POWER	1.8V	PP1V8_S0	6
POWER	POWER	1.8V	PP1V8R1V5_S0_PCH_VCCVRM_F	22 24
POWER	POWER	1.8V	USB_HUB1_VDD1V8	34
POWER	POWER	1.8V	USB_HUB1_VDD1V8PLL	34
POWER	POWER	1.8V	PP3V3R1V8_ENET_LR_OUT_REG	37
POWER	POWER	3.3V	PPVBAT_G3_SYSCLK_R	79
POWER	POWER	3.3V	USB_HUB1_VDDPLL3V3	34
POWER	POWER	3.3V	USB_HUB1_VDDA3V3	34
POWER	POWER	3.3V	USB_HUB2_VDDPLL3V3	35
POWER	POWER	3.3V	USB_HUB2_VDDA3V3	35
POWER	POWER	3.3V	PP3V3R1V5_PCH_VCCSUSHDA	22 24
POWER	POWER	3.3V	PP3V3_S0_CK505_F	26
POWER	POWER	3.3V	PP3V3_S0_HS_F	62
POWER	POWER	3.3V	PP3V3_S0_SW_SD_PWR	45
POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC_F	17 22
POWER	POWER	3.3V	PP3V3_S0	6
POWER	POWER	3.3V	PP3V3_SMCUSBMUX	43
POWER	POWER	3.3V	PP3V3_S3	6 98
POWER	POWER	3.3V	PP3V3_S3_BT_FLT	44
POWER	POWER	3.3V	PP3V3_S3_MINI_CONN	33
POWER	POWER	3.3V	PP3V3_S3_SDCARD_FLT	44
POWER	SWITCHNODE	3.3V	PP3V3_S3_ENET_PHY_FET	36
POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_XTALVDDH	37
POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_BIASVDDH	37
POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_AVDDH	37
POWER	POWER	3.3V	ENET_XTALVDDH	37
POWER	POWER	3.3V	PP3V3_S5	6
POWER	POWER	3.3V	PP3V3_S5_REG_R	70
POWER	POWER	3.3V	PPVOUT_S0_PCH_DCPSST	22
POWER	POWER	3.3V	PPVOUT_PCH_DCPSUSBYP	
POWER	POWER	3.3V	PPVOUT_G3_PCH_DCPRTC	22
POWER	POWER	3.3V	PPVBATT_G3_RTC	27
POWER	POWER	3.3V	PPVBATT_G3_RTC_R	27
POWER	POWER	3.3V	PP3V3_AUDIO_SPDIF_JACK	60 98
POWER	POWER	3.3V	PP3V3_FW_FWPHY_VDDA	39
POWER	POWER	3.3V	PP3V3_FW_FWPHY_VP25	39
POWER	POWER	3.3V	PP3V3_S0_T29	6
POWER	POWER	3.3V	PP3V3_SW_DPAPWR	78 84
POWER	POWER	3.3V	PP3V3_SW_DPBPWR	
POWER	POWER	3.3V	PP3V3_G3H_RTC	18 19 22 27
POWER	POWER	3.3V	PP3V3_G3H_AVREF_SMC	46 47
POWER	POWER	3.4V	PP3V3_G3H_SMC_AVCC	46
POWER	POWER	3.42V	PP3V42_G3H	6
POWER	POWER	4.5V	4V5_REG_IN	56
POWER	POWER	4.5V	PP4V5_AUDIO_ANALOG	56 61
POWER	POWER	4.5V	PP5V_AUDIO_HPAMP	56
POWER	POWER	5V	PP5V_LAMP_VREG	56 59
POWER	POWER	5V	PP5V_RAMP_VREG	58
POWER	POWER	5V	PP5V_S0	6 98
POWER	POWER	5V	PP5V_S0_CPU_VCORE_VCC	65
POWER	POWER	5V	PP5V_S0_PCH_VSREF	74
POWER	POWER	5V	PP5V_S0_SATA_FET	42
POWER	POWER	5V	5V_S0_P1V05REG_VIN	68
POWER	POWER	5V	5V_S0_P1V05REG_VDD	68
POWER	POWER	5V	PP5V_S3	6 98
POWER	POWER	5V	PP5V_S3_VREFMRGN_A	28
POWER	POWER	5V	PP5V_S3_VREFMRGN_B	28
POWER	POWER	5V	PP5V_S3_DDR_REG_V5FILT	71
POWER	POWER	5V	PP5V_S3_CAMERA_FLT	44
POWER	POWER	5V	PP5V_S3_REG_R	70
POWER	POWER	5V	PP5V_S3_IR_FLT	44 98
POWER	POWER	5V	PP5V_S5	6
POWER	POWER	5V	PP5V_S5_PCH_V5REFSUS	24
POWER	POWER	5V	PP5V_USB_PORT0	43
POWER	POWER	5V	PP5V_USB_PORT0_F	43
POWER	POWER	5V	PP5V_USB_PORT1	43
POWER	POWER	5V	PP5V_USB_PORT1_F	43
POWER	POWER	5V	PP5V_USB_PORT2	43
POWER	POWER	5V	PP5V_USB_PORT2_F	43
POWER	POWER	5V	PP5V_USB_PORT3	43
POWER	POWER	5V	PP5V_USB_PORT3_F	43
POWER	POWER		DDR_REG_PGND	71
POWER	POWER		DDR_REG_CSGND	71
	POWER	3.3V	PPVDDIO_25M_B	79
	POWER	1.05V	PPVDDIO_25M_A	79
	POWER	3.3V	PPVDDIO_25M_C	79
	POWER	12V	PP3V3R12V_SW_DPAPWR_R	85
	POWER	12V	PP3V3R12V_SW_DPAPWR_D	82
	POWER	1.5V	PP1V5_S0_DP_R	83

SENSING NET PROPERTIES

NET_TYPE PHYSICAL	SPACING		
SNS_DIFF	THERMAL	VR_CPU_ISNS1_P	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS1_N	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N	65
SNS_DIFF	THERMAL	VR_CPU_ISNS2_P	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS2_N	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N	65
SNS_DIFF	THERMAL	VR_CPU_ISNS3_P	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS3_N	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N	65
SNS_DIFF	THERMAL	VR_CPU_ISNS4_P	
SNS_DIFF	THERMAL	VR_CPU_ISNS4_N	
SNS_DIFF	THERMAL	VR_CPU_ISNS4_R_N	
SNS_DIFF	THERMAL	P1V05S0_ISN	68
SNS_DIFF	THERMAL	P1V05S0_ISP	68
SNS_DIFF	THERMAL	VR_AXG_ISNS_R_P	65
SNS_DIFF	THERMAL	VR_AXG_ISNS_R_N	65
SNS_DIFF	THERMAL	VR_AXG_ISNS_N	65 67
SNS_DIFF	THERMAL	VR_AXG_ISNS_P	65 67
SNS_DIFF	THERMAL	VR_ISNS_1V05_N	94
SNS_DIFF	THERMAL	VR_ISNS_1V05_P	94
SNS_DIFF	THERMAL	VR_ISNS_VAXG_N	50 94
SNS_DIFF	THERMAL	VR_ISNS_VAXG_P	50 94
SNS_DIFF	THERMAL	VR_ISNS_VCORE_N	50 94
SNS_DIFF	THERMAL	VR_ISNS_VCORE_P	50 94
SNS_DIFF		CPU_VAXG_SENSE_P	13 65
SNS_DIFF		CPU_VAXG_SENSE_N	13 65
SNS_DIFF		VR_AXG_VSNS_R_N	65
SNS_DIFF		VR_AXG_VSNS_R_P	65
SNS_DIFF		VR_AXG_VSEN	65
SNS_DIFF		VR_AXG_RGND	65
SNS_DIFF		VR_AXG_VSNS_XW_N	65
SNS_DIFF		VR_AXG_VSNS_XW_P	65
SNS_DIFF		CPU_VCC_SENSE_N	13 65
SNS_DIFF		CPU_VCC_SENSE_P	13 65
SNS_DIFF		VR_CPU_VSEN	65
SNS_DIFF		VR_CPU_RGND	65
SNS_DIFF		VR_CPU_VSNS_R_N	65
SNS_DIFF		VR_CPU_VSNS_R_P	65
SNS_DIFF		VR_CPU_VSNS_XW_P	65
SNS_DIFF		VR_CPU_VSNS_XW_N	65
SNS_DIFF		CPU_VCCIO_SENSE_P	13 68
SNS_DIFF		CPU_VCCIO_SENSE_N	13 68
SNS_DIFF		P1V05S0_VSEN	68
SNS_DIFF		P1V05S0_RTN	68

VR CTRL NET PROPERTIES

NET_TYPE PHYSICAL	SPACING		
VR_CTL_PHY	SWITCHNODE	VR_CPU_PH1_SNUB	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_PH2_SNUB	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_PH3_SNUB	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_PH4_SNUB	
VR_CTL_PHY	VR_CTL	VR_CPU_COMP	65
VR_CTL_PHY	VR_CTL	VR_AXG_TM	65
VR_CTL_PHY	VR_CTL	VR_AXG_PWM_R	65
VR_CTL_PHY	VR_CTL	VR_AXG_PWM	65 67
VR_CTL_PHY	VR_CTL	VR_CPU_PWM2	65 66
VR_CTL_PHY	VR_CTL	VR_CPU_PWM1	65 66
VR_CTL_PHY	VR_CTL	VR_CPU_PWM1_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_PWM2_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_PWM3	65 66
VR_CTL_PHY	VR_CTL	VR_CPU_PWM3_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_PWM4	
VR_CTL_PHY	VR_CTL	VR_CPU_PWM4_R	65
VR_CTL_PHY	VR_CTL	VR_AXG_SW_FREQ	65
VR_CTL_PHY	VR_CTL	VR_EN_PWR_OVP	65
VR_CTL_PHY	VR_CTL	VR_RSET	65
VR_CTL_PHY	VR_CTL	VR_EN_PWR_OVP_R	65
VR_CTL_PHY	VR_CONTROL	VR_CPU_BOOT1_RC	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_BOOT2_RC	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_BOOT3_RC	66
VR_CTL_PHY	VR_CONTROL	VR_AXG_BOOT1_RC	67
VR_CTL_PHY	VR_CTL	VR_CPU_BOOT4_RC	
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV1_BOOT	66
VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_GDSEL	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV1_LGATE	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV1_UGATE	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV2_BOOT	66
VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_GDSEL	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV2_LGATE	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV2_UGATE	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV3_BOOT	66
VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_GDSEL	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV3_LGATE	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV3_UGATE	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV4_BOOT	
VR_CTL_PHY	VR_CTL	VR_CPU_DRV4_GDSEL	
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV4_LGATE	
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV4_UGATE	
VR_CTL_PHY	VR_CONTROL	VR_AXG_DRV1_BOOT	67
VR_CTL_PHY	VR_CTL	VR_AXG_DRV1_UGATE_R	67
VR_CTL_PHY	VR_CONTROL	VR_AXG_DRV1_LGATE	67
VR_CTL_PHY	VR_CONTROL	VR_AXG_DRV1_UGATE	67
VR_CTL_PHY	VR_CTL	VR_CPU_SW_FREQ	65
VR_CTL_PHY	VR_CTL	VR_CPU_FB	65
VR_CTL_PHY	VR_CTL	VR_CPU_FB_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_RAMP_ADJ	65
VR_CTL_PHY	VR_CTL	VR_CPU_IMON	50 65
VR_CTL_PHY	VR_CTL	VR_CPU_SUTH	65
VR_CTL_PHY	VR_CTL	VR_CPU_N_PSI	65
VR_CTL_PHY	VR_CTL	VR_CPU_FDVID	65
VR_CTL_PHY	VR_CTL	VR_CPU_PSICOMP	65
VR_CTL_PHY	VR_CTL	VR_CPU_IAUTO	65
VR_CTL_PHY	VR_CTL	VR_CPU_PSICOMP1	65
VR_CTL_PHY	VR_CTL	VR_CPU_PSICOMP2	65
VR_CTL_PHY	VR_CTL	VR_CPU_FB_RC	65
VR_CTL_PHY	VR_CTL	VR_CPU_FB2	65
VR_CTL_PHY	VR_CTL	VR_CPU_IMON_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_HFREQ_COMP	65
VR_CTL_PHY	SWITCHNODE	VR_AXG_PH1_SNUB	67
VR_CTL_PHY	VR_CTL	VR_AXG_IMON	50 65
VR_CTL_PHY	VR_CTL	VR_AXG_IMON_R	65
VR_CTL_PHY	VR_CTL	VR_AXG_HFREQ_COMP	65
VR_CTL_PHY	VR_CTL	VR_AXG_FB	65
VR_CTL_PHY	VR_CTL	VR_SEN_R1	65
VR_CTL_PHY	VR_CTL	VR_SEN_R2	65
VR_CTL_PHY	VR_CTL	VR_SEN_R3	65
VR_CTL_PHY	VR_CTL	VR_AXG_COMP_RC	65
VR_CTL_PHY	VR_CTL	VR_AXG_COMP	65
VR_CTL_PHY	VR_CTL	VR_AXG_TCOMP	65
VR_CTL_PHY	SWITCHNODE	P1V05S0_UGATE	68
VR_CTL_PHY	SWITCHNODE	P1V05S0_LGATE	68
VR_CTL_PHY	VR_CTL	P1V05S0_BOOT	68
VR_CTL_PHY	VR_CTL	P1V05S0_BOOT_R	68
VR_CTL_PHY	VR_CTL	P1V05_IMON	50 68
VR_CTL_PHY	VR_CTL	P1V05S0_FB	68
VR_CTL_PHY	VR_CTL	P1V05S0_PHASE_L	68
VR_CTL_PHY	VR_CTL	P1V05S0_VW	68
VR_CTL_PHY	VR_CTL	P1V05S0_COMP	68
VR_CTL_PHY	VR_CTL	P1V05S0_ICOMP	68
VR_CTL_PHY	VR_CTL	P1V05_S0_VDIFF	68
VR_CTL_PHY	VR_CTL	P1V05S0_COMP_C	68
VR_CTL_PHY	VR_CTL	P1V05S0_VDIF_C	68
VR_CTL_PHY	VR_CTL	P1V05S0_VO	68
VR_CTL_PHY	VR_CTL	P1V05S0_OCSET	68
VR_CTL_PHY	VR_CTL	P1V05S0_SNUBBER	68
VR_CTL_PHY	VR_CTL	P1V05_REG_VFB	
VR_CTL_PHY	VR_CTL	ENET_SR_VFB	36 37
VR_CTL_PHY	VR_CTL	P1V05S0_ISP_R	68
VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2_R	69 95
VR_CTL_PHY	VR_CTL	T29BST_FBX	
VR_CTL_PHY	VR_CTL	P3V42G3H_BOOST	72
VR_CTL_PHY	VR_CTL	P3V42G3H_FB	72

VR CTRL NET PROPERTIES

NET_TYPE PHYSICAL	SPACING		
VR_CTL_PHY	VR_CTL	DDR_REG_CS	71
VR_CTL_PHY	VR_CTL	DDR_REG_FB	71
VR_CTL_PHY	VR_CONTROL	DDR_REG_LGATE	71
VR_CTL_PHY	VR_CONTROL	DDR_REG_UGATE	71
VR_CTL_PHY	VR_CONTROL	DDR_REG_BOOT	71
VR_CTL_PHY	VR_CONTROL	DDR_REG_BOOT_R	71
VR_CTL_PHY	VR_CTL	DDR_REG_VDDQSNS	71
VR_CTL_PHY	VR_CTL	DDR_REG_VTTSNS	71
VR_CTL_PHY	VR_CTL	DDR_REG_PHASE_R	71
VR_CTL_PHY	VR_CTL	DDR_REG_UGATE_R	71
VR_CTL_PHY	SWITCHNODE	1V5_SNUBBER	71
VR_CTL_PHY	VR_CTL	P1V8_REG_VFB	71
VR_CTL_PHY	VR_CTL	P1V8_REG_SYNC	71
VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_BOOT	70
VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_BOOT_R	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_FB	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_ISEN	70
VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_LGATE	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_OCSET	70
VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_VOUT1	70
VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_FSET1	70
VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_UGATE	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_SNUB	70
VR_CTL_PHY	VR_CONTROL	P5VS3_REG_BOOT	70
VR_CTL_PHY	VR_CTL	P5VS3_REG_FB	70
VR_CTL_PHY	VR_CTL	P5VS3_REG_ISEN	70
VR_CTL_PHY	VR_CONTROL	P5VS3_REG_LGATE	70
VR_CTL_PHY	VR_CTL	P5VS3_REG_OCSET	70
VR_CTL_PHY	VR_CTL	P5VS3_REG_FSET2	70
VR_CTL_PHY	VR_CONTROL	P5VS3_REG_UGATE	70
VR_CTL_PHY	VR_CONTROL	P5VS3_REG_VOUT2	70
VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT1	69
VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2	69
VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2_R	69 95
VR_CTL_PHY	VR_CTL	VCCSA_OUT	69
VR_CTL_PHY	VR_CTL	VCCSA_GATE	69
VR_CTL_PHY	VR_CTL	VCCSA_REF	69
VR_CTL_PHY	VR_CTL	VCCSA_CRL	69
VR_CTL_PHY	VR_CTL	CPU_VCCSA_SENSE	13 69
VR_CTL_PHY	PM	VR_CPU_TM	65
VR_CTL_PHY	PM	3V3R2V9_DPAPWR_ADJ	82 97

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VID_PHY	*	50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL	*	0.35MM	?

VR VID NET PROPERTIES

NET_TYPE PHYSICAL	SPACING		
VID_PHY	VR_CTL_VIDS	CPU_VIDSCLK_R	13
VID_PHY	VR_CTL_VIDS	CPU_VIDALERT_L_R	13
VID_PHY	VR_CTL_VIDS	CPU_VIDSOUT_R	13
VID_PHY	VR_CTL_VIDS	CPU_VIDSCLK	13 65
VID_PHY	VR_CTL_VIDS	CPU_VIDALERT_L	13 65
VID_PHY	VR_CTL_VIDS	CPU_VIDSOUT	13 65

PULL-UP STUB < 1-INCH
VID LENGTH SKEW < 1-INCH
VID LENGTH RANGE< 1 TO 15-INCH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_VIDS	*	=4X_DIELECTRIC	?

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: POWER CONSTRAINTS

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T29 ELECTRICAL ROUTES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	*	=5X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	TOP,BOTTOM	=7X_DIELECTRIC	?

T29 PCI-EXPRESS (SAME RULE AS PCIE)

T29 SPI INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	0.2 MM	?

T29 XTAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_XTAL_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_XTAL	*	=4X_DIELECTRIC	?

T29 SMBUS INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SMB_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SMB	*	=2x_DIELECTRIC	?

GREEN CLOCK CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5X_DIELECTRIC	?

T29 BIAS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_COMP	*	0.2 MM	?

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
		NET_TYPE	
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_P<3..0> 78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_N<3..0> 78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_D2R_C_P<3..0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29_D2R_C_N<3..0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29_R2D_P<3..0> 84
NO_TEST=TRUE	T29_90D	T29	T29_R2D_N<3..0> 84
NO_TEST=TRUE	T29_90D	T29	T29_D2R_P<3..0> 78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_D2R_N<3..0> 78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_F_P<3..0> 84
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_F_N<3..0> 84
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_P<3..0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_N<3..0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_P<3..0>
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_N<3..0>
NO_TEST=TRUE	T29_90D	T29	DP_A_EXT_AUXCH_P 84 85
NO_TEST=TRUE	T29_90D	T29	DP_A_EXT_AUXCH_N 84 85
NO_TEST=TRUE	T29_90D	T29	DP_SDRVA_AUXCH_C_P 84
NO_TEST=TRUE	T29_90D	T29	DP_SDRVA_AUXCH_C_N 84
NO_TEST=TRUE	T29_90D	T29	DP_SDRVB_AUXCH_C_P
NO_TEST=TRUE	T29_90D	T29	DP_SDRVB_AUXCH_C_N
NO_TEST=TRUE	T29_90D	T29	DP_B_EXT_AUXCH_P
NO_TEST=TRUE	T29_90D	T29	DP_B_EXT_AUXCH_N
NO_TEST=TRUE	T29_90D	T29	T29DPA_D2R1_AUXCH_P 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_D2R1_AUXCH_N 85
NO_TEST=TRUE	T29_90D	T29	T29DPB_D2R3_AUXCH_P
NO_TEST=TRUE	T29_90D	T29	T29DPB_D2R3_AUXCH_N
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_N<0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_P<0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_N<2> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_P<2> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_N<0>
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_P<0>
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_N<2>
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_P<2>
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0> 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0> 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0> 18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0> 18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0> 18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0> 18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0> 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0> 86
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P 18 86
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N 18 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0> 83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0> 83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_P<3..0> 83 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_N<3..0> 83 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0> 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0> 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0> 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0> 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0> 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0> 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0> 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0> 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_R_C_P 83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_R_C_N 83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P 83 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N 83 86
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_AUXCH_P 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_AUXCH_N 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_AUXCH_P
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_AUXCH_N
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_C_P<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_C_N<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_P<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_N<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_R_P<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_R_N<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_C_P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_C_N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_R_P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_R_N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_A_RSVD_N 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_A_RSVD_P 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_B_RSVD_N
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_B_RSVD_P

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
		NET_TYPE	
	T29_SPI_55S	T29_SPI	JTAG_T29_TDI 15 21 86
	T29_SPI_55S	T29_SPI	JTAG_T29_TMS 15 18 86
	T29_SPI_55S	T29_SPI	JTAG_T29_TCK 15 21 25 86
	T29_SPI_55S	T29_SPI	JTAG_T29_TDO 15 21 86
L43J	T29_SPI_55S	T29_SPI	T29_SPI_MOSI 86
L43H	T29_SPI_55S	T29_SPI	T29_SPI_MISO 86
L43G	T29_SPI_55S	T29_SPI	T29_SPI_CS_L 86
L44H	T29_SPI_55S	T29_SPI	T29_SPI_CLK 86
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29 79 86 96
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R 86 96
	T29_SMB_55S	T29_SMB	I2C_T29_SDA 49 86
	T29_SMB_55S	T29_SMB	I2C_T29_SCL 49 86
L42J	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB 79
L42G	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET 79
L42E	CLK_25M_55S	CLK_25M	ENET_CLK25M_XTALI_OSC 36 79
L42K	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_CLK 79
L43K	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29 79 86 96
L42H	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R 86 96
L42C	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X2 79
L42D	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X2_R 79
L42F	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X1 79
L43L	T29_55S	T29_COMP	T29_RSENSE 86
L43C	T29_55S	T29_COMP	T29_RBIAS 86
L43E		T29_COMP	T29_A_BIAS 82 84 85
L43D		T29_COMP	T29_B_BIAS
L42B		T29_COMP	DP_A_BIAS 84

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T29 CONSTRAINTS

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PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

NET_TYPE PHYSICAL	NET_TYPE SPACING		
T357	PM	4V5_REG_EN	56
T358	PM	3V42G3H_SHDN_L	72
T359	PM	ALL_SYS_PWRGD_R	5 32 64
T360	PM	ALL_SYS_PWRGD_SMC	46 64
T361	PM	AP_PWR_EN	20 25 33
T362	PM	AP_MINI_RESET_L	33
T363	PM	AUD_I2C_INT_L	20 62
T364	PM	AUD_IP_PERIPHERAL_DET	20 61
T365	PM	AUD_IPHS_SWITCH_EN	21 62
T366	PM	AUD_SPDIF_IN	60 83 91
T367	PM	AUD_SPDIF_IN_CODEC	56 83
T368	PM	BDV_BKL_PWM	46 83 97
T369	PM	BL_PWM	6 83
T410	PM	BL_EN	6 81
T411	PM	BDV_BKL_PWM	46 83 97
T369	PM	CK505_27MHZ_EN	26
T367	PM	CPUVTT_REG_EN	
T365	PM_VTT	CPUVTT_REG_PGOOD_R	63
T365	PM	CPU_MEM_RESET_L	11 32
T372	PM	CPU_PECI_R	46
T373	PM_VTT	CPU_PWRGD	11 21 25
T374	PM	CPU_RESET_L	11 27
T374	PM	CPU_SKTOCC_L	11 63
T375	PM	CPU_CATERR_L	11
T376	PM	CPU_PECI	11 21 46
T376	PM	CPU_PROCHOT_L	11 47 65
T377	PM	CPU_THRMTRIP_L	11 47
T378	PM	CPU_PROC_SEL	11 19
T379	PM	DEBUG_RESET_L	27 48
T380	PM	DDRVTT_EN	
T381	PM	DP_INT_SPDIF_AUDIO	81 83
T382	PM	DP_INTPNL_HPD	81 83
T383	PM	3V3R2V9_DPAPWR_ADJ	82 95
T384	PM	DP_A_PWRDWN	84
T385	PM	DP_A_PWRDWN_FET_R	82
T386	PM	DP_A_PWRDWN_INV	82
T387	PM	DPAPWRSW_HVEN_L_R	82
T388	PM	DPAPWRSW_CT	82
T389	PM	DPAPWRSW_ILIM	82
T390	PM	DPAPWRSW_IFLT	82
T391	PM	T29_A_HV_EN	82 84
T392	PM	3V3R2V9_DPBPWR_ADJ	
T393	PM	DP_B_PWRDWN	
T394	PM	DP_B_PWRDWN_FET_R	
T395	PM	DP_B_PWRDWN_INV	
T396	PM	DPBPWRSW_HVEN_L_R	
T397	PM	DPBPWRSW_CT	
T398	PM	DPBPWRSW_ILIM	
T399	PM	DPBPWRSW_IFLT	
T400	PM	T29_B_HV_EN	
T429	PM	T29_PWR_EN	18 80 97
T427	PM	T29_RESET_RTR_L	80 86
T412	PM	LCD_BL_FILT	83
T413	PM	LCD_BLK_ON_DLY	
T405	PM	LCD_BL_PWM	83
T406	PM	MXM_PNL_BL_PWM	76 83

NET_TYPE PHYSICAL	NET_TYPE SPACING		
T230	PM	ENET_PWR_EN	20 25 36
T224	PM	ENET_LOW_PWR	15 21 37
T229	PM	FW_RESET_L	27 39
T231	PM	ENET_RESET_L	27 36
T236	PM	FW_PME_L	15 21 39
T237	PM	FW_PWR_EN	15 21
T235	PM	FW_CLKREQ_L	15 39
T248	PM	ISOLATE_CPU_MEM_L	21 25 32
T260	PM	LPC_PWRDWN_L	19 46 48
T265	PM	MEM_RESET_L	30 31 32 89
T262	PM	MINI_CLKREQ_L	15 33
T263	PM	MINI_RESET_L	27 33
T267	PM	MXM_CLKREQ_L	9 75
T272	PM	MXM_GOOD	5 21 25
T274	PM	ODD_PWR_EN_L	15 21 42
T68	PM	RTC_RESET_L	18 27 97
T48	PM	RSMRST_PWRGD	46 64
T47	PM	RTC_RESET_L	18 27 97
T331	PM	S4_ENABLES	63
T488	PM	SDCONN_STATE_RST_L	
T489	PM	SDCONN_DETECT_BUF_L	92
T487	PM	SDCONN_STATE_CHANGE	20 25 45
T485	PM	SDCARD_RESET	15 21 44 98
T434	PM	SDCARD_RESET_L	44
T435	PM	SDCARD_PLT_RST_L	27 44
T436	PM	SDCARD_PLT_RST_L_R	
T435	PM	SMC_PM_G2_EN	46 74
T436	PM	SMC_PM_G2_EN_R	74
T436	PM	SMC_PM_G2_EN_L	74
T436	PM	S5_DG_1	74
T436	PM	S5_MSFT_G1	74
T415	PM	USE_HDD_OOB_L	20 51
T416	PM	HDD_OOB_1V00_REF	51
T408	PM	SMC_ADAPTER_EN	19 46 47
T408	PM	SMC_RUNTIME_SCI_L	21 46 47
T408	PM	SMC_WAKE_SCI_L	15 18 21 46
T418	PM	SMC_DELAYED_PWRGD	47 64
T418	PM	SMC_LRESET_L	27 46
T420	PM	SMC_RESET_L	46 47 48
T419	PM	SMC_PROCHOT	46 47
T417	PM	SMC_PROCHOT_3_3_L	46 47
T414	PM	SMC_ONOFF_L	46 47
T410	PM	SMC_MANUAL_RST_L	47
T239	PM	SPI_DESCRIPTOR_OVERRIDE_L	18 46
T415	PM	T29_PWR_EN	18 80 97
T408	PM	T29_RESET_L	27 80
T408	PM	T29_DP_PORTA_PWR_EN	20 25 82 91
T409	PM	T29_DP_PORTA_PWR_EN_REG	82
T265	PM_VTT	XDP_CPUPWRGD	
T263	PM_VTT	XDP_DBRESET_L	11 25
T273	PM_VTT	XDP_PWRGD	
T266	PM	XDPPCH_PLTRST_L	25 27
T266	PM	USB_HUB_SOFT_RESET_L	20 25 34
T424	PM	VSYNC_DP_CONN	6 81
T424	PM	VSYNC_DP	81
T424	PM	VIDEO_ON	81
T844	PM	VTT_REG_PGOOD_L	63

NET_TYPE PHYSICAL	NET_TYPE SPACING		
T272	PM	PLT_RESET_L	20 27
T442	PM_VTT	PLT_RESET_LS1V05_L	11
T274	PM	PM_BATLOW_L	15 19 46
T275	PM	PM_CLK32K_SUSCLK	9 46 91
T275	PM	PM_CLK32K_SUSCLK_R	9 19 91
T277	PM	PM_CLKRUN_L	15 19 46 48
T278	PM	PM_PWRBTN_L	19 25 46
T279	PM	PM_RSMRST_L	27 46
T276	PM	PM_RSMRST_PCH_L	19 27
T438	PM	PCH_SRTCRST_L	18
T437	PM	PCH_INTVRMEN_L	18
T441	PM	PCH_DSWVRMEN	19
T439	PM	PCH_DF_TVS	19
T452	PM	PCH_PROCPWRGD	21
T444	PM	PCIE_WAKE_L	19 33 36 78
T443	PM	PM_DSW_PWRGD	19
T445	PM	PM_ASW_PWRGD	19 64
T446	PM	PM_MEM_PWRGD_R	11
T450	PM	PM_EN_DDR1V5_S3_REG	63 71
T447	PM	PM_EN_DDRVTT_S0_REG	32 63 71
T448	PM	PM_EN_P12V_S0_FET	6 63
T449	PM	PM_EN_P1V05_S0_REG	63 68
T470	PM	PM_EN_P1V05_S3_REG	
T471	PM	PM_EN_P1V5_S0_FET	63 73
T472	PM	PM_EN_P1V8_S0_REG	63 71
T473	PM	PM_EN_P3V3_S0_FET	63 73
T474	PM	PM_EN_P3V3_S3_FET	63 73
T475	PM	PM_EN_P3V3_S5_REG	70
T476	PM	PM_EN_P5V_S0_FET	63 73
T477	PM	PM_EN_P5V_S3_REG	63 70
T478	PM	PM_EN_PVCCSA_S0_REG_L	64
T479	PM	PM_EN_VCCSA_S0_CPU	
T480	PM	PM_EN_PVCORE_CPU	63 65
T438	PM_VTT	PM_MEM_PWRGD	11 19 97
T454	PM	PM_MXM_EN	64 76
T452	PM	PM_PCH_PWRGD_R	64
T453	PM	PM_PECI_PWRGD	46 64
T455	PM	PM_PECI_PWRGD_R	46
T456	PM	PM_PGOOD_DDR1V5_S3_REG	5 63 71
T457	PM	PM_PGOOD_P1V05_S0_REG	63 64 68
T458	PM	PM_PGOOD_P1V5_S0_FET	11 64 73
T459	PM	PM_PGOOD_P1V8_S0_REG	64 71
T460	PM	PM_PGOOD_P3V3_S0_FET	63 64 73
T461	PM	PM_PGOOD_P3V3_S3_FET	34 73
T462	PM	PM_PGOOD_P3V3_S5_REG	27 64 70
T463	PM	PM_PGOOD_P5V_S0_FET	63 64 73
T464	PM	PM_PGOOD_MINI	33
T465	PM	PM_PGOOD_PVCORE_CPU	5 25 64 65
T466	PM	PM_PGOOD_PVCCSA_S0_REG	63 64
T467	PM	PM_PGOOD_P5V_S3_REG	63 70 82
T468	PM	PM_PGOOD_PVAXG	5 65
T439	PM_VTT	PM_MEM_PWRGD	11 19 97
T441	PM	PM_MEM_PWRGD_L	11
T454	PM	PM_MXM_PGOOD	64 76
T452	PM	PM_PCH_PWRGD	19 21 64
T429	PM	PM_SLP_S3_5V	32
T430	PM	PM_SLP_S3_5V_L	32
T431	PM	PM_SLP_S3_5V_R2	32
T428	PM	PM_SLP_S3_L	5 19 26 32 36 46 47 63 82
T426	PM	PM_SLP_S4_L	5 19 32 46 47 63 97
T427	PM	PM_SLP_S5_L	5 19 46 47 63
T437	PM_VTT	PM_SYNC	11 19
T425	PM	PM_SYSRST_L	19 25 27 46
T440	PM	PM_SYS_PWRGD	19 32 64
T481	PM_VTT	PM_THRMTRIP_L	21 47
T482	PM	PM_SLP_S3_BUF_L	63
T483	PM	PM_SLP_S4_1_1_R	63
T484	PM	PM_SLP_S4_D_L	32
T434	PM	PM_SLP_S4_L	5 19 32 46 47 63 97
T435	PM	PGOOD_P1V5_S0_DLY	11
T439	PM	PGOOD_1V8_S0_G1	64
T440	PM	PGOOD_1V8_S0_G2	64
T480	PM	PGOOD_P12V_S0	63 64
T430	PM	PGOOD_P1V8_S0	64
T431	PM	PGOOD_PCH_S0	5 64
T429	PM	PGOOD_PCH_S0_R	64 91
T432	PM	PGOOD_SYSPWROK	64
T433	PM	PGOOD_SYSPWROK_R	64
T434	PM	POWER_BUTTON_L	47
T431	PM	PEG_RESET_L	9 27
T431	PM	PGOOD_CPU_S0	64
T422	PM	PGOOD_CPU_UNCORE	64 91
T423	PM	PGOOD_5V_1V05_3V3	64 91
T420	PM	PGOOD_3V3_1V05	64 91
T421	PM	PGOOD_12V_S0_G1	64
T489	PM	PGOOD_12V_S0_G2	64
T422	PM	9V_COMP_REF	64
T496	PM	12V_COMP_REF	64
T430	PM	ALL_SYS_PWRGD	64 91

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PM RESETS ENABLES PGOOD CONST

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

95 6	IN	PP5V_S3	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
92 44	IN	USB_CAMERA_L_P	FUNC_TEST=TRUE
92 44	IN	USB_CAMERA_L_N	FUNC_TEST=TRUE
92 44	IN	USB_BT_L_P	FUNC_TEST=TRUE
92 44	IN	USB_BT_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
1 PP3V3_S3 TESTPOINT NEAR J4700
6 GROUND TESTPOINTS NEAR J4700

J4750 USB CARD READER

97 44 21 15	IN	SDCARD_RESET	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4780 IR BOARD

92 44	IN	USB_IR_L_P	FUNC_TEST=TRUE
92 44	IN	USB_IR_L_N	FUNC_TEST=TRUE
95 44	IN	PP5V_S3_IR_FLT	FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J4780

J4520 SATA ODD (HIGH SPEED)

46 42	IN	SMC_ODD_DETECT	FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
1 GROUND TESTPOINTS NEAR J4520

J5551 ODD TEMP SENSOR

94 52	IN	SNS_ODD_P	FUNC_TEST=TRUE
94 52	IN	SNS_ODD_N	FUNC_TEST=TRUE

J5600 ODD FAN

53	IN	FAN_0_PWR_L	FUNC_TEST=TRUE
53	IN	FAN_TACH0_L	FUNC_TEST=TRUE
95 53	IN	PP12V_S0_FAN0_L	FUNC_TEST=TRUE
53	IN	FAN_0_GND	FUNC_TEST=TRUE

J5700 CPU FAN

54	IN	FAN_2_PWR_L	FUNC_TEST=TRUE
54	IN	FAN_TACH2_L	FUNC_TEST=TRUE
95 54	IN	PP12V_S0_FAN2_L	FUNC_TEST=TRUE
54	IN	FAN_2_GND	FUNC_TEST=TRUE
94 54 52	IN	SNS_AMB_P	FUNC_TEST=TRUE
94 54 52	IN	SNS_AMB_N	FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J5700

J5601 HD FAN

53	IN	FAN_1_PWR_L	FUNC_TEST=TRUE
53	IN	FAN_TACH1_L	FUNC_TEST=TRUE
95 53	IN	PP12V_S0_FAN1_L	FUNC_TEST=TRUE
53	IN	FAN_1_GND	FUNC_TEST=TRUE

J5400 HDD TEMP SENSOR

94 51 42	IN	HDD_OOB_TEMP_FILT	FUNC_TEST=TRUE

1 GROUND TESTPOINTS NEAR J5400

J5560 SKIN TEMP SENSOR

94 52 44	IN	SNS_SKIN_LEFT_P	FUNC_TEST=TRUE
94 52 44	IN	SNS_SKIN_LEFT_N	FUNC_TEST=TRUE
94 52	IN	SNS_SKIN_RIGHT_P	FUNC_TEST=TRUE
94 52	IN	SNS_SKIN_RIGHT_N	FUNC_TEST=TRUE

J6602 AUDIO RIGHT SPEAKER

91	IN	AUD_SPKR_OUTLO2R_POUT	FUNC_TEST=TRUE
91	IN	AUD_SPKR_OUTLO2R_NOUT	FUNC_TEST=TRUE
91	IN	AUD_SPKR_OUTLO1R_POUT	FUNC_TEST=TRUE
91	IN	AUD_SPKR_OUTLO1R_NOUT	FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

91	IN	AUD_SPKR_OUTLO2L_POUT	FUNC_TEST=TRUE
91	IN	AUD_SPKR_OUTLO2L_NOUT	FUNC_TEST=TRUE
91	IN	AUD_SPKR_OUTLO1L_POUT	FUNC_TEST=TRUE
91	IN	AUD_SPKR_OUTLO1L_NOUT	FUNC_TEST=TRUE

J6600 AUDIO AUXILIARY CONNECTOR

2 TP'S

95 60	IN	PP3V3_AUDIO_SPDIF_JACK	FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
60	IN	AUD_LI_DET_JACK	FUNC_TEST=TRUE
60	IN	AUD_LI_R_JACK	FUNC_TEST=TRUE
60	IN	AUD_LI_GND_JACK	FUNC_TEST=TRUE
60	IN	AUD_LI_L_JACK	FUNC_TEST=TRUE
60	IN	HS_MIC_HI_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_L_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_GND_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_R_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_TYPEDET_JACK	FUNC_TEST=TRUE
60	IN	AUD_IP_PERPH_JACK	FUNC_TEST=TRUE
60	IN	AUD_HP_TIPDET_JACK	FUNC_TEST=TRUE
60	IN	AUD_SPDIFIN_JACK	FUNC_TEST=TRUE

4 GROUND TESTPOINTS NEAR J6600

		GND	17 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=17
95 6	IN	PP3V3_S3	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
95 6	IN	PP5V_S0	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

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