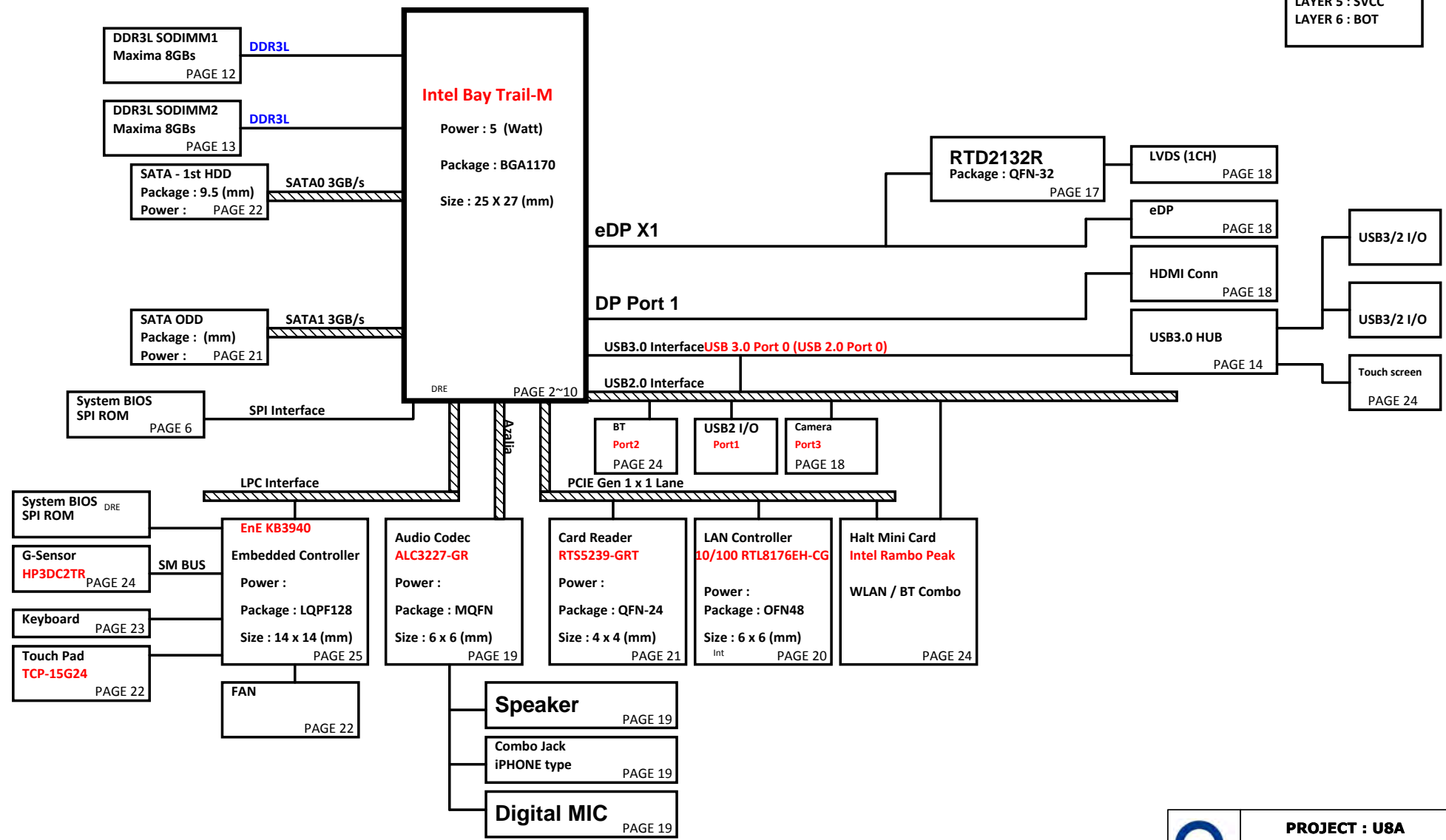
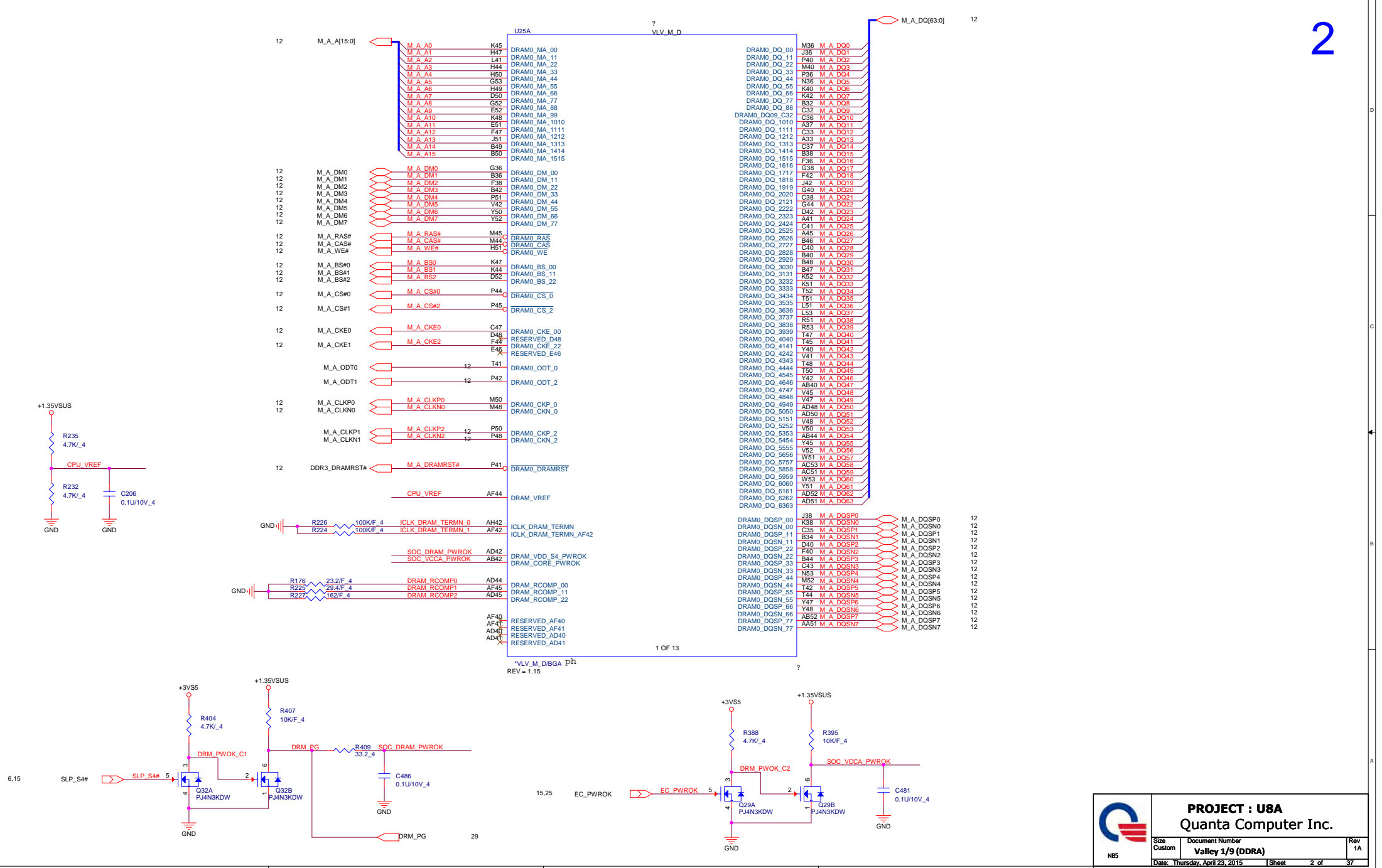



U87/U88 UMA (14"/15.6") Ultra/Slim Intel Bay trail-M Platform Block Diagram

PCB 6L STACK UP
 LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(Low)
 LAYER 5 : SVCC
 LAYER 6 : BOT

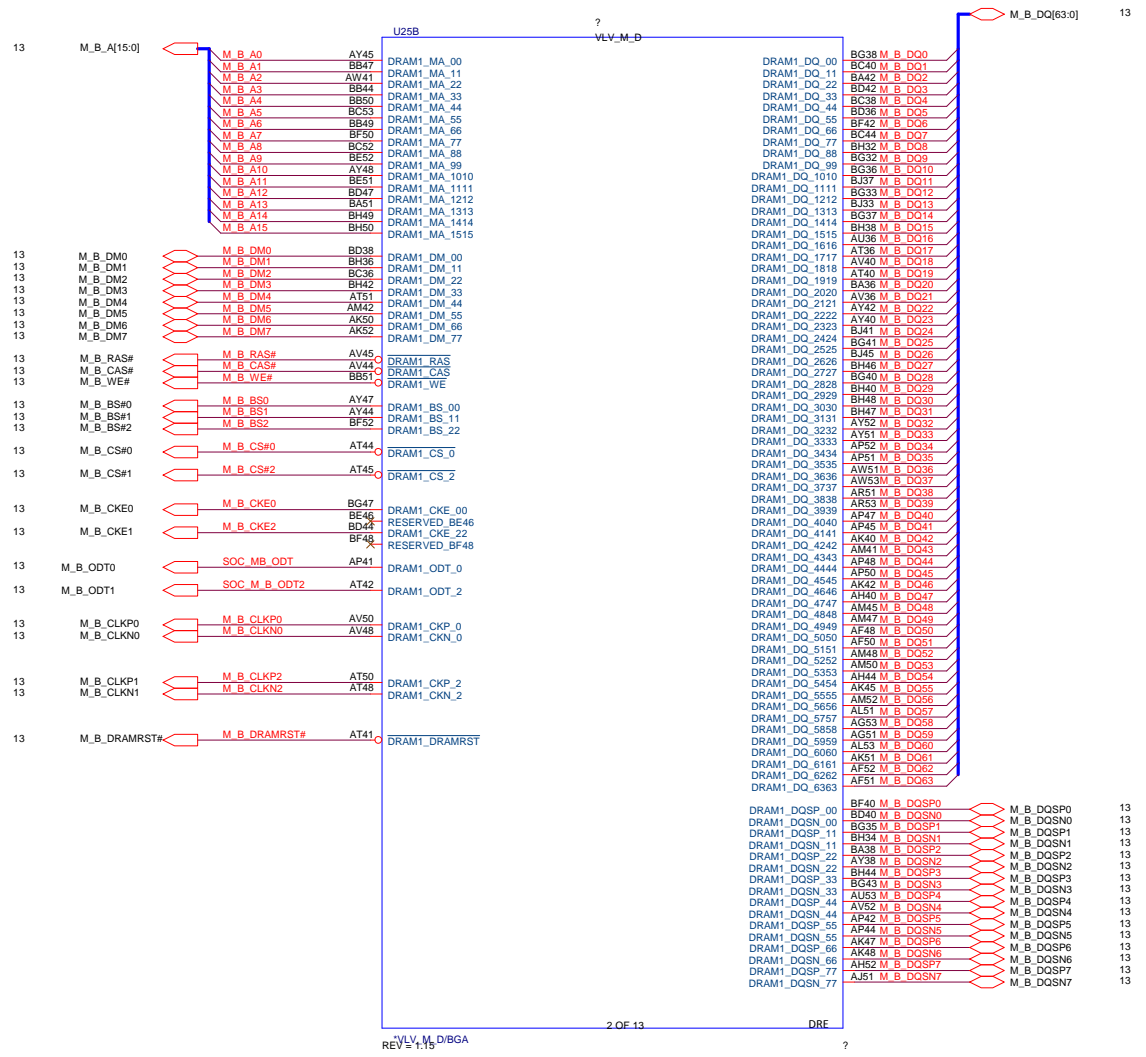





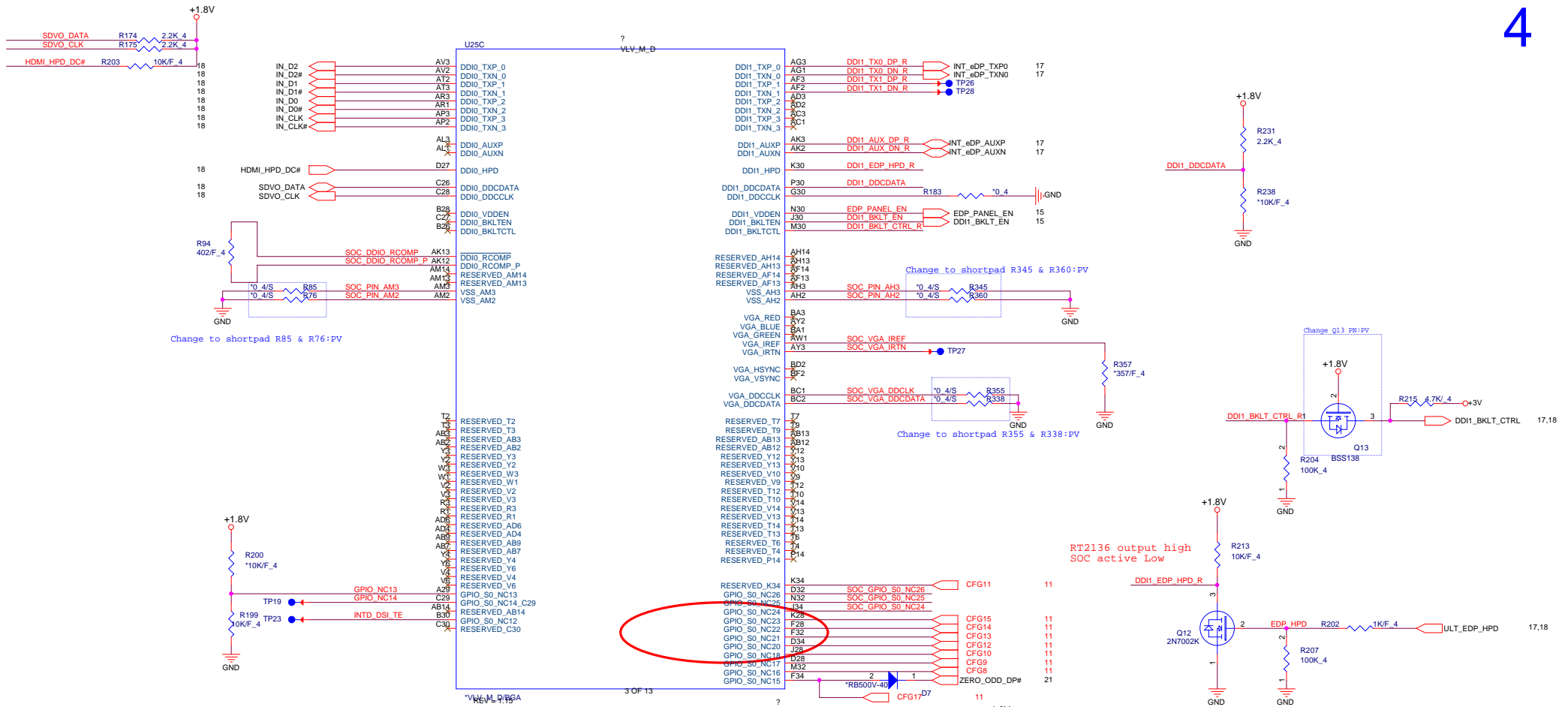


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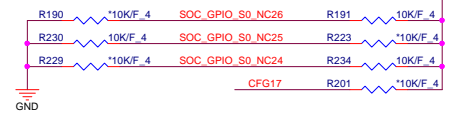
Size Custom	Document Number	Rev 1A
Valley 1/9 (DDRA)		
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Size Custom	Document Number	Rev 1A	
	Valley 2/9 (DDR8)		
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Need to discuss with BIOS



GPIO26	0	1	0=W/FAN , 1=FANLESS
GPIO25	0	0	
GPIO24	0	1	0=14 " , 1=15 "

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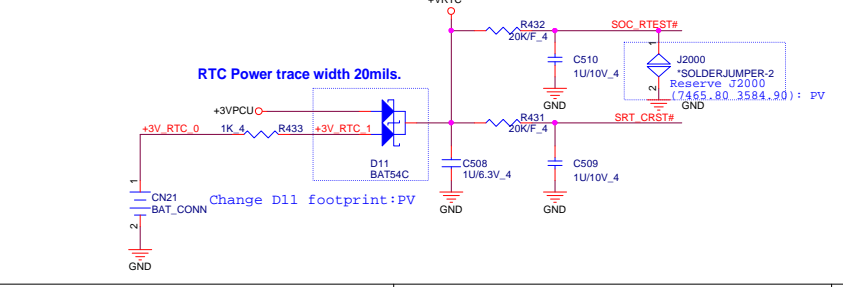
Size Custom	Document Number Valley 3/9 (Display)	Rev 1A
Date: Thursday, April 23, 2015	Sheet 4 of 37	

D
C
B
A

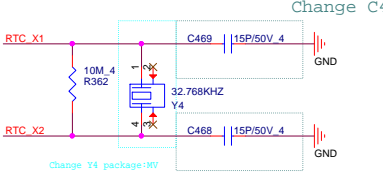
D
C
B
A



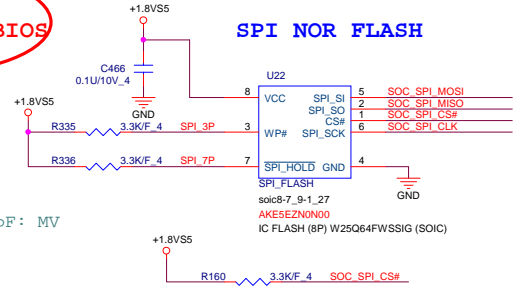
RTC Circuitry(RTC)



RTC Clock 32.768KHZ



SPI NOR FLASH



Check with BIOS

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Size Custom	Document Number	Rev 1A
	Valley 5/9 (SPI/GPIO/CLK)	
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+1.8VS5

- R337 *10K/F 4 SOC_VOL_UP
- R346 *10K/F 4 SOC_VOL_DOWN
- R340 *10K/F 4 SOC_HOME_BUT
- R341 *10K/F 4 SOC_ROTATE
- R342 *10K/F 4 SOC_PWR_BUT

Add HUB power detect circuit: PV

14 HUB_PWR_DET

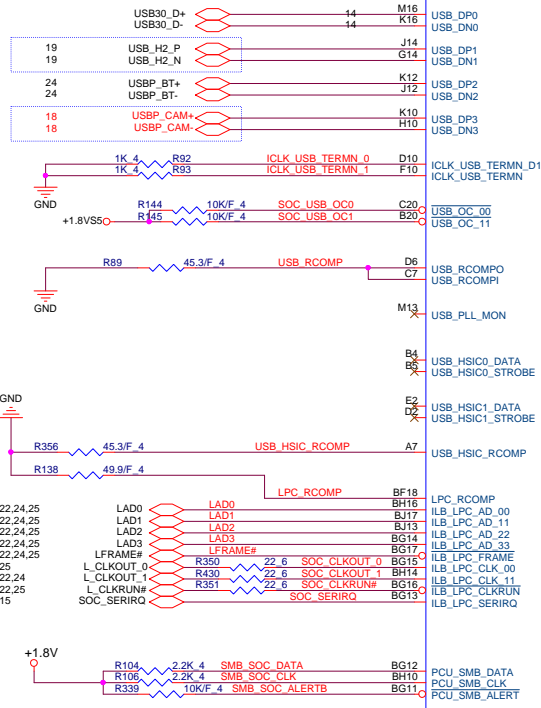
Change USB port define: PV

USB 3.0/2.0 HUB

USB2.0 CONN

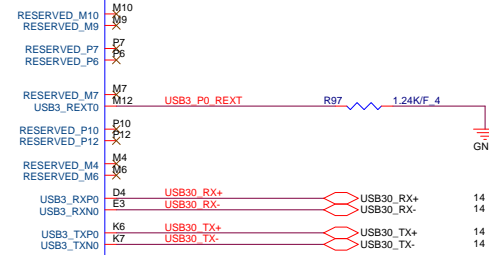
BT

Camera



- 15 SMB_SOC_DATA
- 15 SMB_SOC_CLK

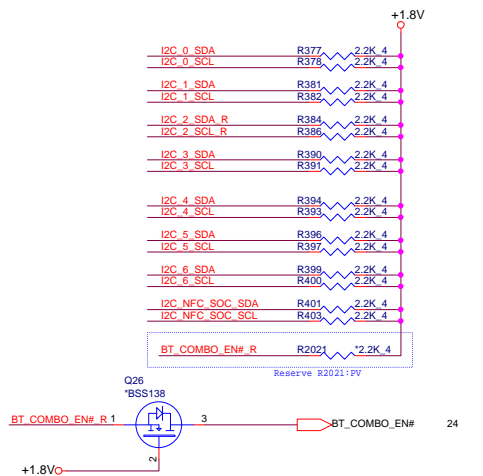
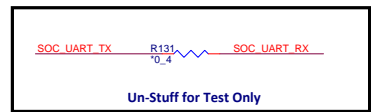
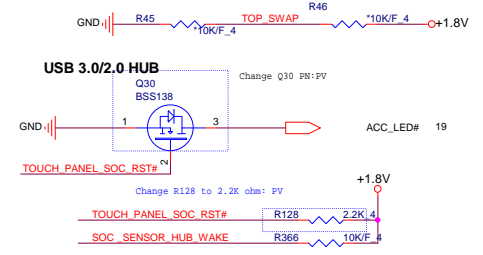
- GPIO_S5_31
- GPIO_S5_32
- GPIO_S5_33
- GPIO_S5_34
- GPIO_S5_35
- GPIO_S5_36
- GPIO_S5_37
- GPIO_S5_38
- GPIO_S5_39
- GPIO_S5_40
- GPIO_S5_41
- GPIO_S5_42
- GPIO_S5_43
- USB_DP0
- USB_DN0
- USB_DP1
- USB_DN1
- USB_DP2
- USB_DN2
- USB_DP3
- USB_DN3
- ICLK_USB_TERMIN_D10
- ICLK_USB_TERMIN
- USB_OC_00
- USB_OC_11
- USB_RCOMP
- USB_RCOMP
- USB_PLL_MON
- USB_HSIC0_DATA
- USB_HSIC0_STROBE
- USB_HSIC1_DATA
- USB_HSIC1_STROBE
- USB_HSIC_RCOMP
- LPC_RCOMP
- ILB_LPC_AD_00
- ILB_LPC_AD_11
- ILB_LPC_AD_22
- ILB_LPC_AD_33
- ILB_LPC_FRAME
- ILB_LPC_CLK_00
- ILB_LPC_CLK_11
- ILB_LPC_CLKRUN
- ILB_LPC_SERIRQ
- PCU_SMB_DATA
- PCU_SMB_CLK
- PCU_SMB_ALERTB




- BD12 BT_COMBO_EN# R
- BC12 TOP_SWAP
- BD14 SOC_UART_TX
- BC14
- BF14 SOC_SENSOR_HUB_WAKE
- BD16 TOUCH_PANEL_SOC_RST#
- BC16 SOC_UART_RX
- BH12 ACZ_SPKR
- BH22 I2C_0_SDA
- BG23 I2C_0_SCL
- BG24 I2C_1_SDA
- BH24 I2C_1_SCL
- BG25 I2C_2_SDA_R
- BJ25 I2C_2_SCL_R
- BG26 I2C_3_SDA
- BH26 I2C_3_SCL
- BF27 I2C_4_SDA
- BG27 I2C_4_SCL
- BH28 I2C_5_SDA
- BG28 I2C_5_SCL
- BJ29 I2C_6_SDA
- BG29 I2C_6_SCL
- BH30 I2C_NFC_SOC_SDA
- BG30 I2C_NFC_SOC_SCL

GPS, BT & WIFI

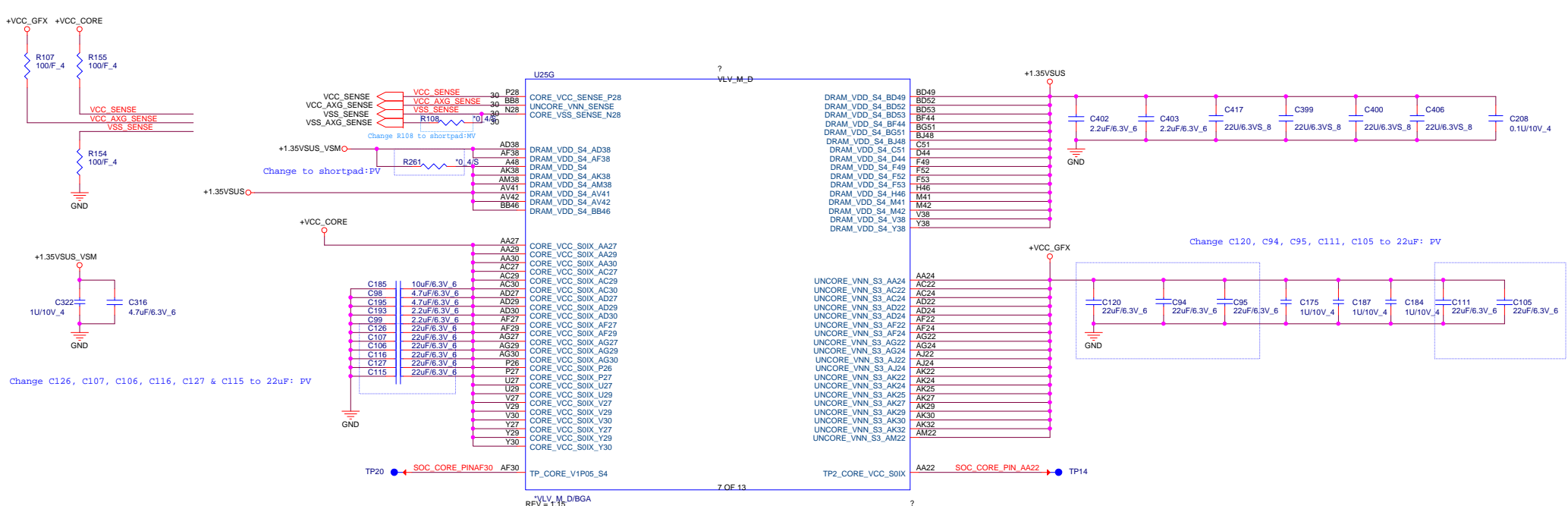
CODEC





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Change C126, C107, C106, C116, C127 & C115 to 22uF: PV


Change R108 to shortpad:RV

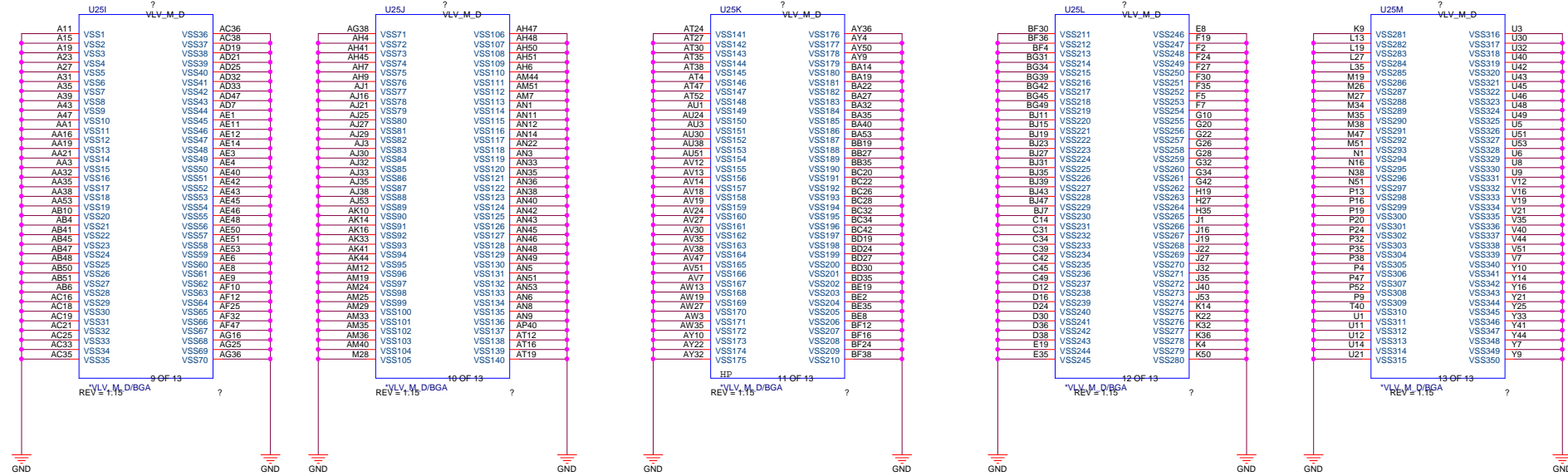
Change to shortpad:PV


Change C120, C94, C95, C111, C105 to 22uF: PV

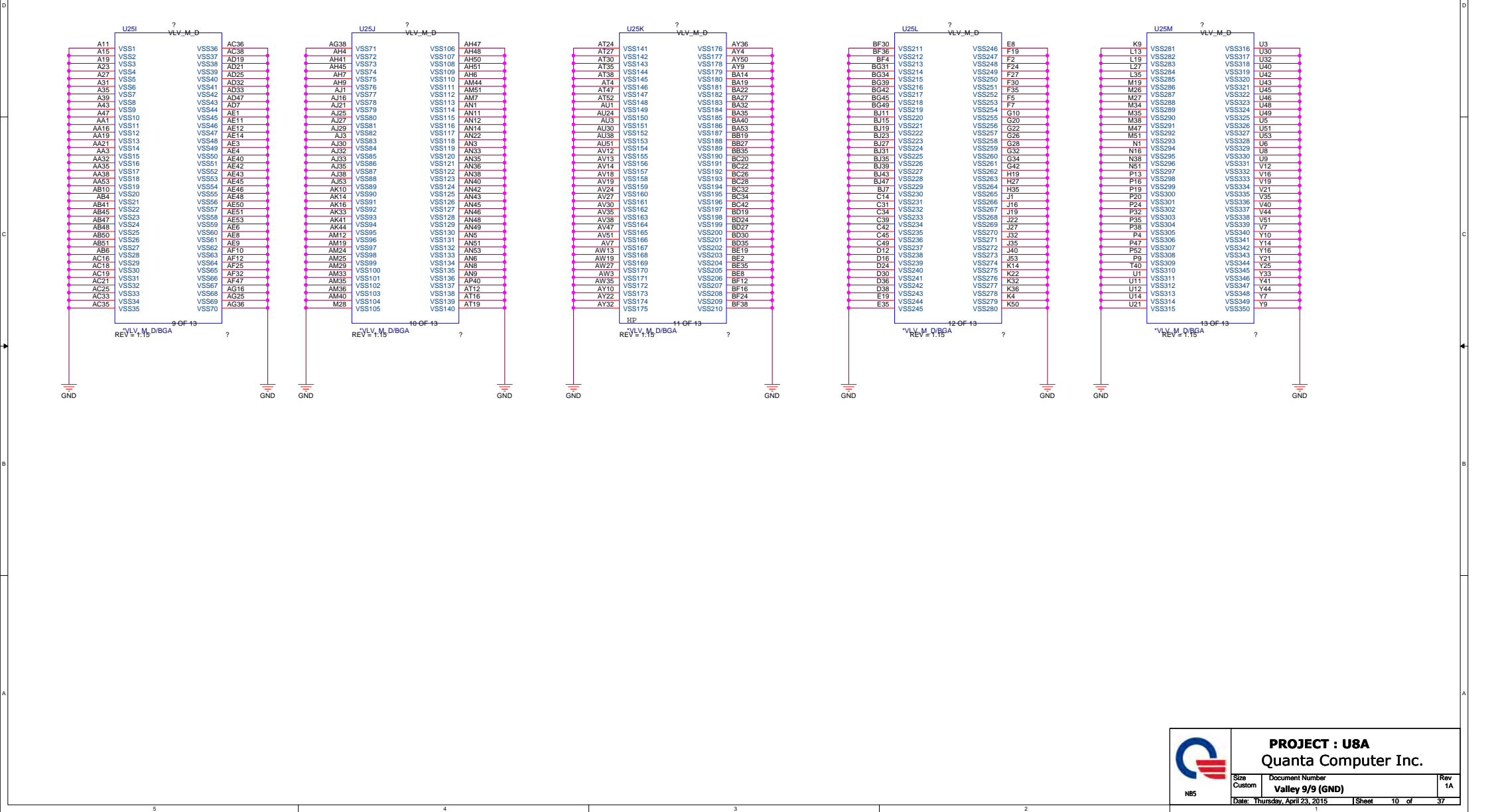
RVLV_M_D/BGA
REV = 1.15

7 OF 13

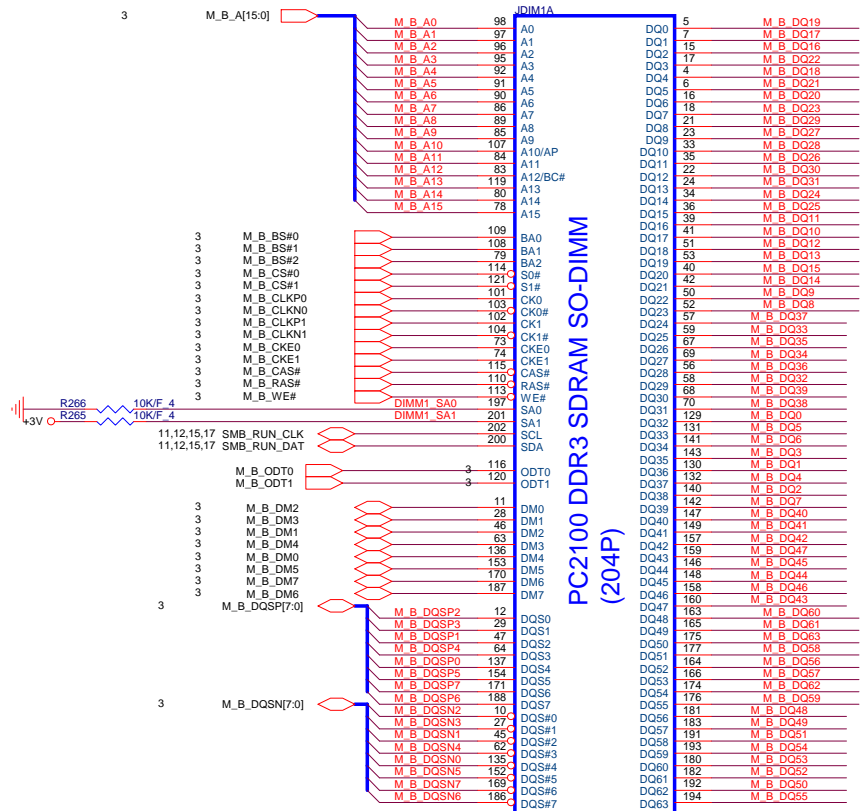
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	Size Custom	Document Number Valley 7/9 (Power 1)	
1 Sheet		8 of 37	



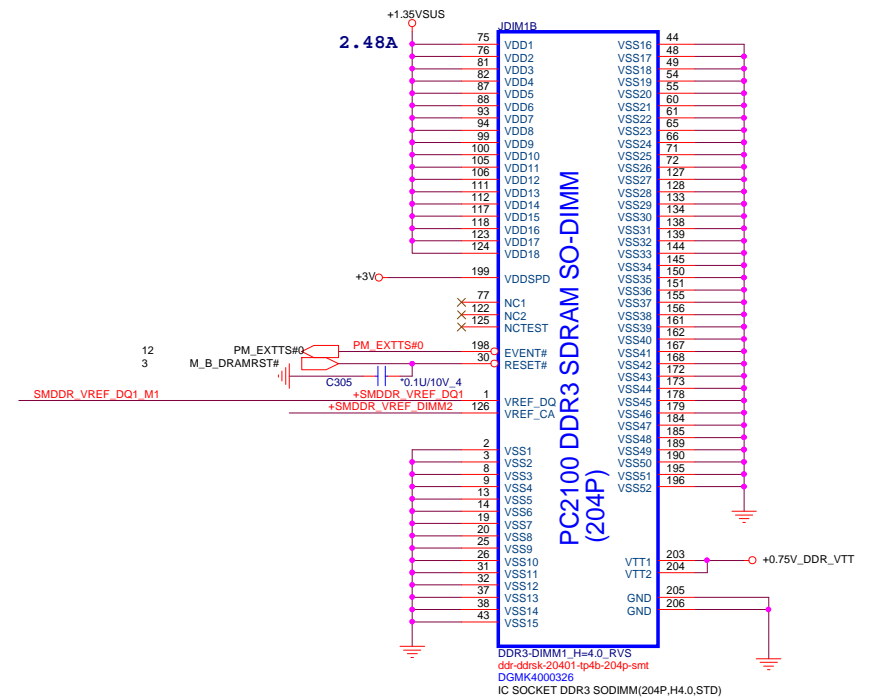
	PROJECT : USA		
	Quanta Computer Inc.		
Size Custom	Document Number Valley 9/9 (GND)	Rev 1A	
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M_B_DQ[63:0]

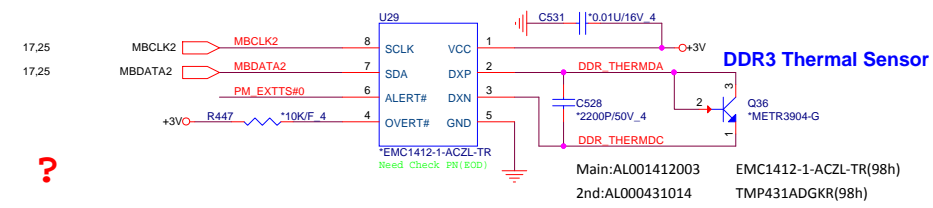


DDR3-DIMM1_H=4.0_RVS
 ddr-ddrsk-20401-tp4b-204p-smt
 DGMK4000326
 IC SOCKET DDR3 SODIMM(204P,H4.0,STD)



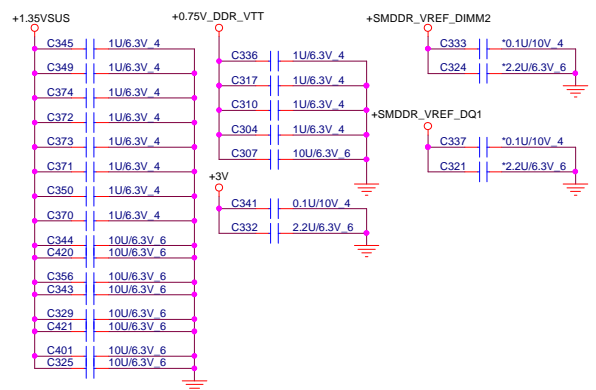
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 ddr-ddrsk-20401-tp4b-204p-smt
 DGMK4000326
 IC SOCKET DDR3 SODIMM(204P,H4.0,STD)

Local Thermal Sensor



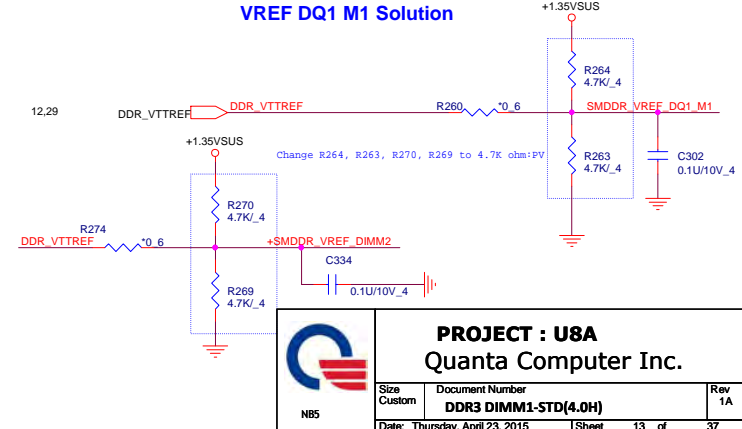
Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector



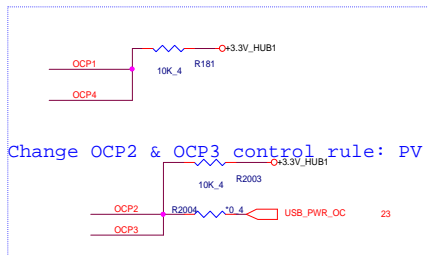
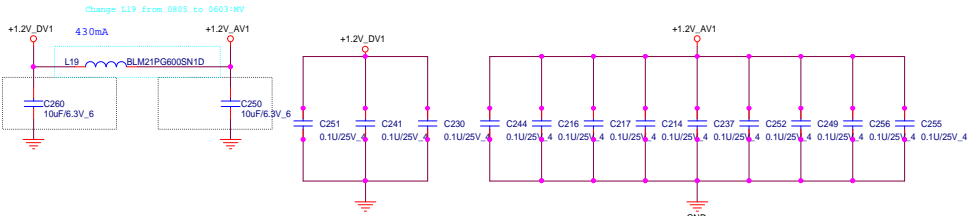
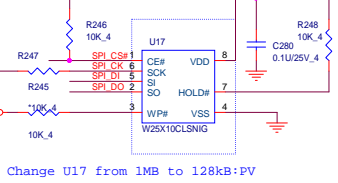
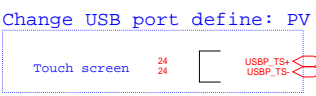
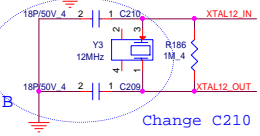
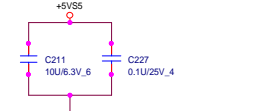
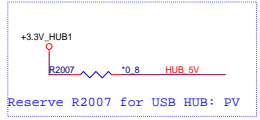
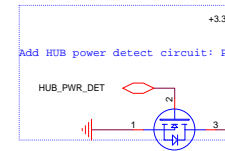
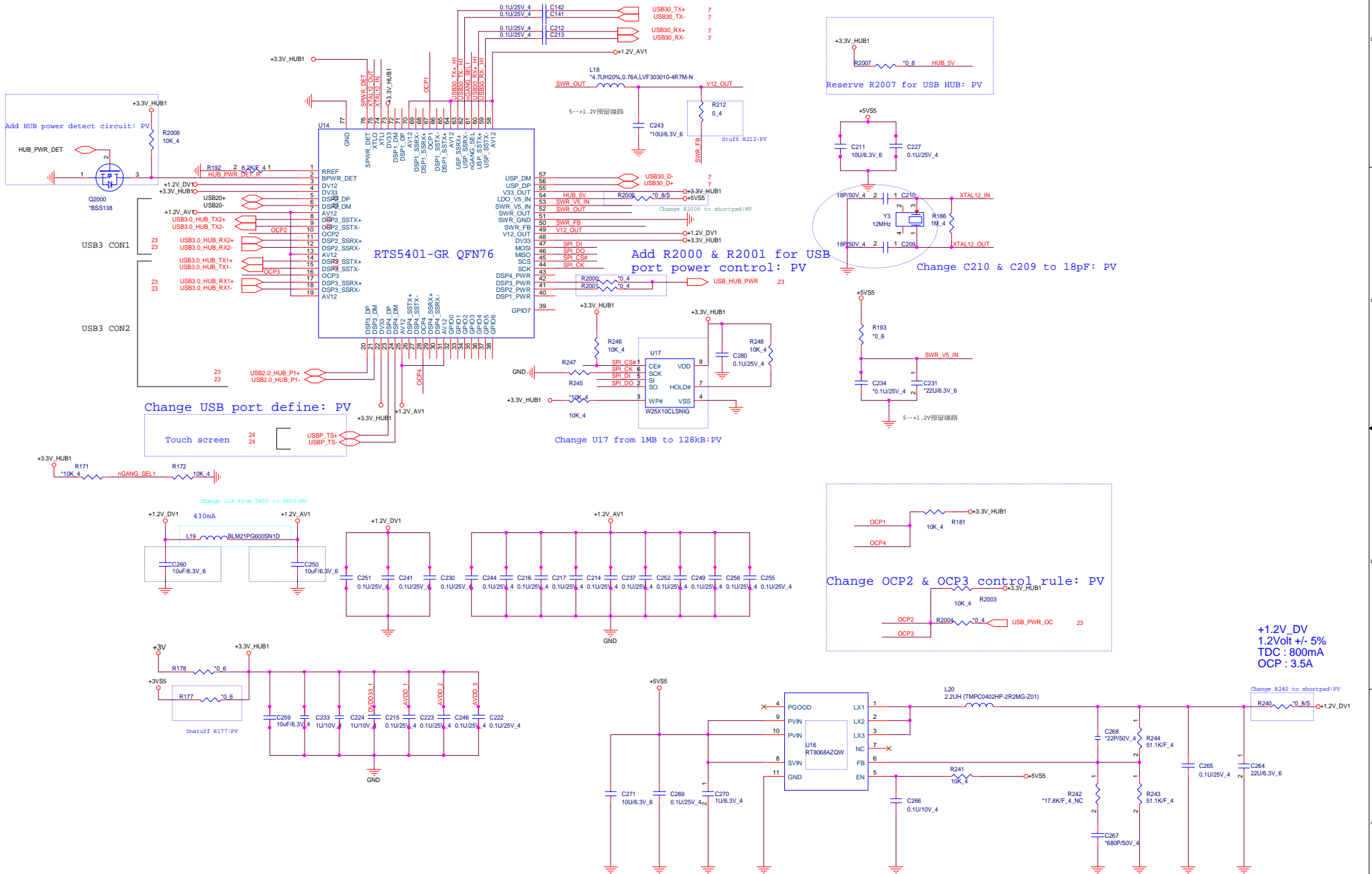
2,8,12,22,29,32 +1.35VSUS
 12,29 +0.75V_DDR_VTT
 4,9,11,12,14,15,17,18,19,20,21,22,23,24,25,32

VREF DQ1 M1 Solution

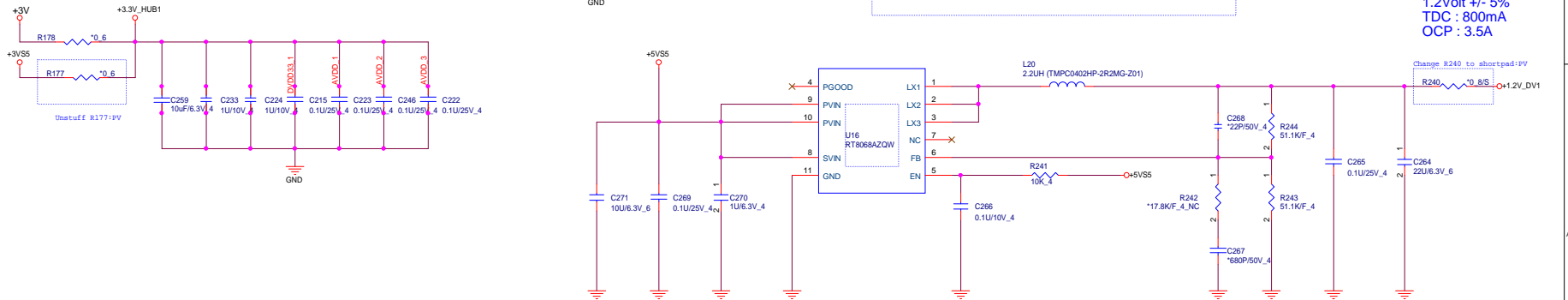


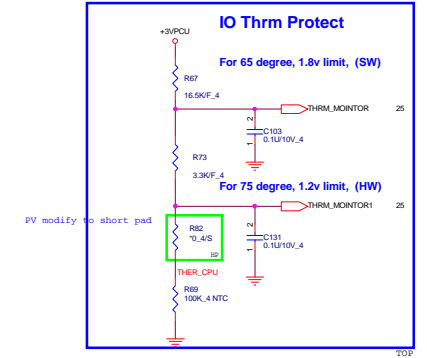
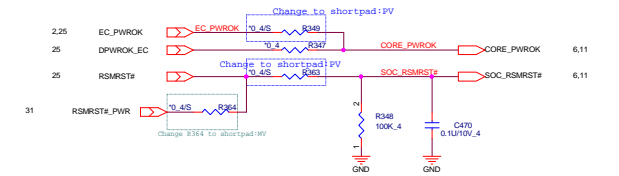
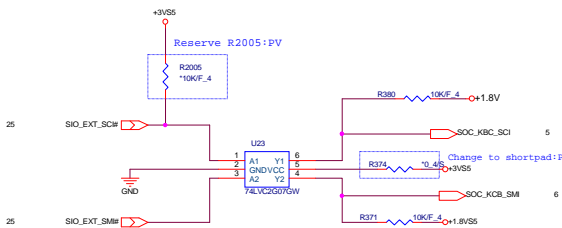
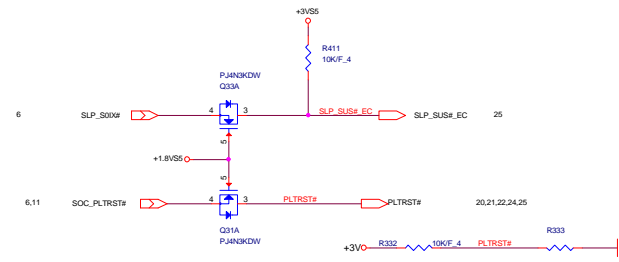
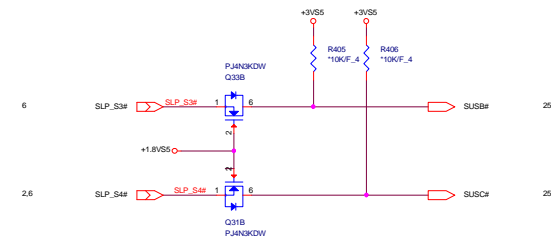
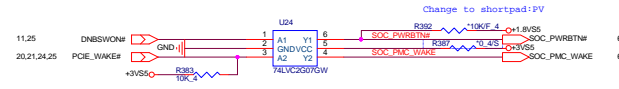
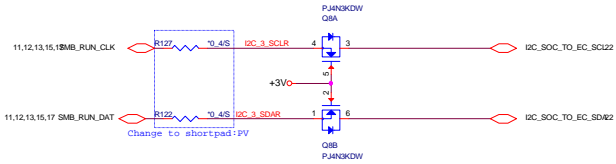
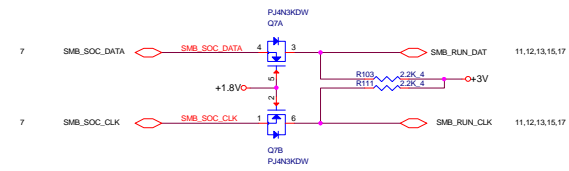
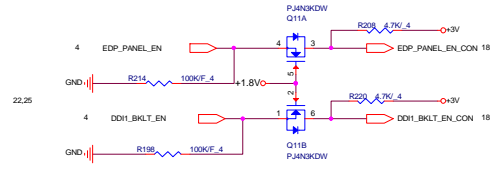
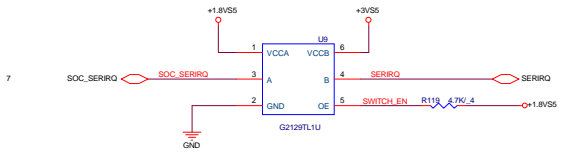
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DDR3 DIMM1-STD(4.0H)		
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**+1.2V_DV
 1.2Volt +/- 5%
 TDC : 800mA
 OCP : 3.5A**





S5 to S0 Cold Boot Sequence without S0ix

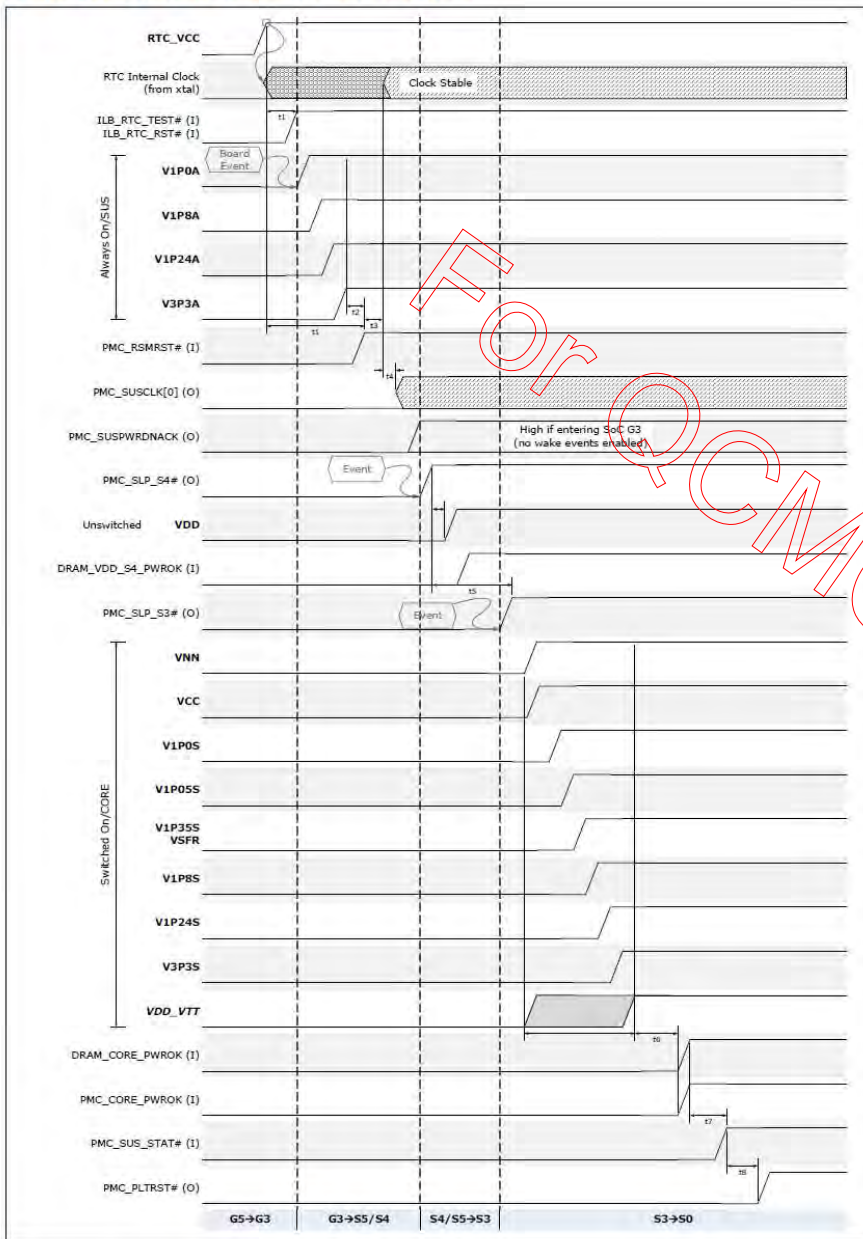


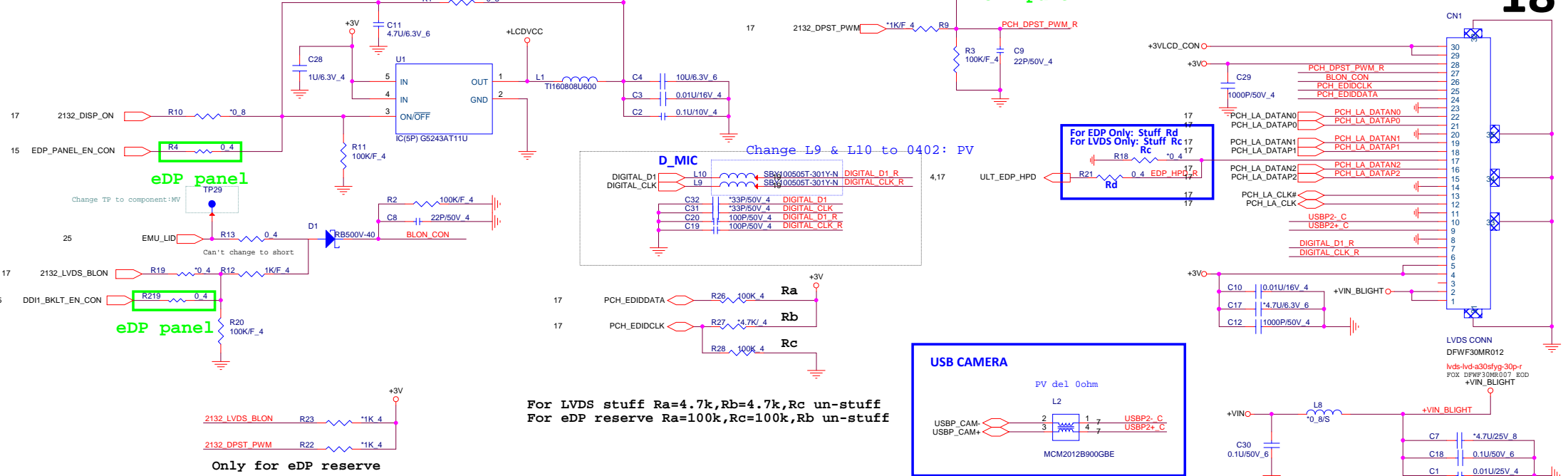
Table 4-12. Cold Boot Timing Spec

Parameter	Description	Min	Typ	Max	Units
T0	RTC_VCC stable to ILB_RTC_TEST# high	9			ms
T1	VR ramp up time from 10% to 90% voltage level			2	ms
T2	Rail to subsequent rail turn on delay	10		2000	us
T3	VSUS stable to PMC_RSMRST# high	10			ms
T4	S and SX rails stable to PMC_CORE_PWROK	100			ms

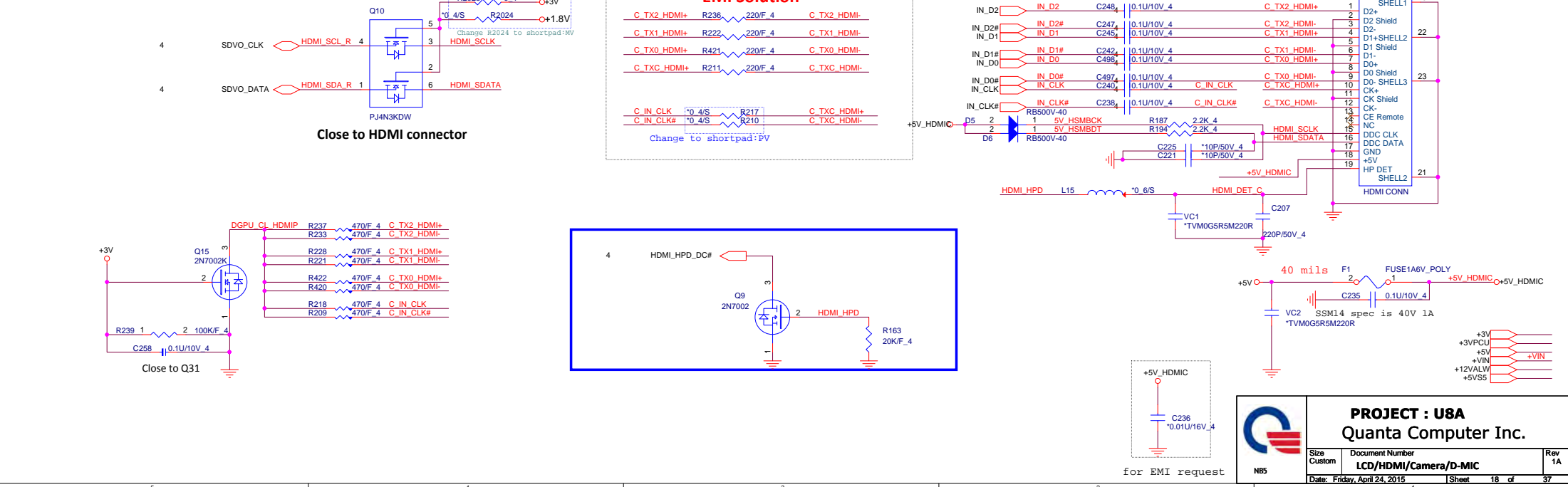
NOTES:

- T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.
- Violation of rail-to-rail sequencing may cause the SoC part long term reliability issue.
- Platform devices other than SoC sequencing are not explicitly shown as they are not limited by the SoC sequencing requirement.

LVDS Conn.

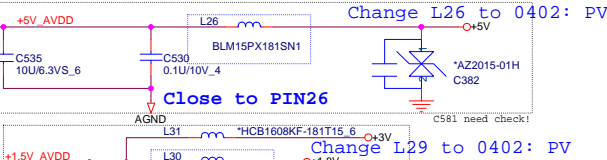
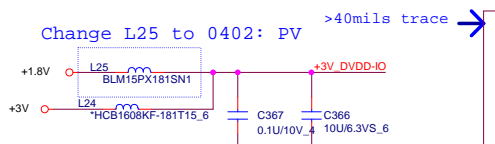
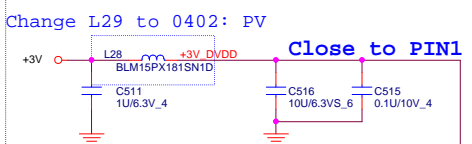


HDMI Conn.

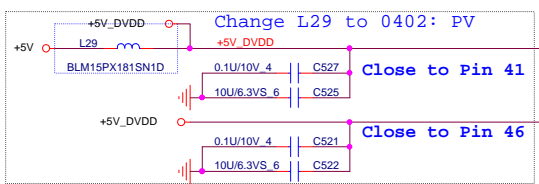
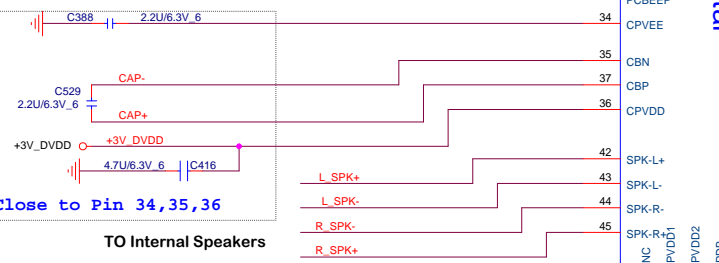
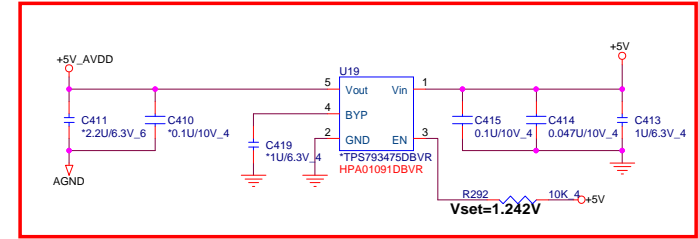
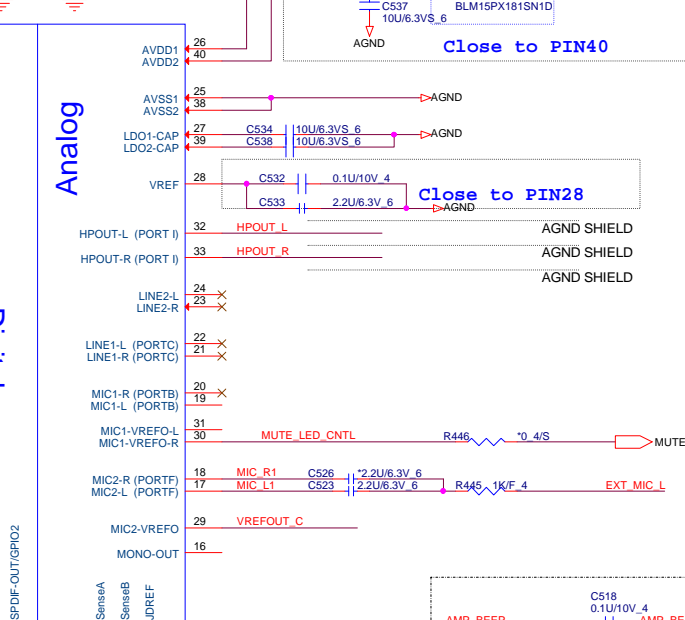
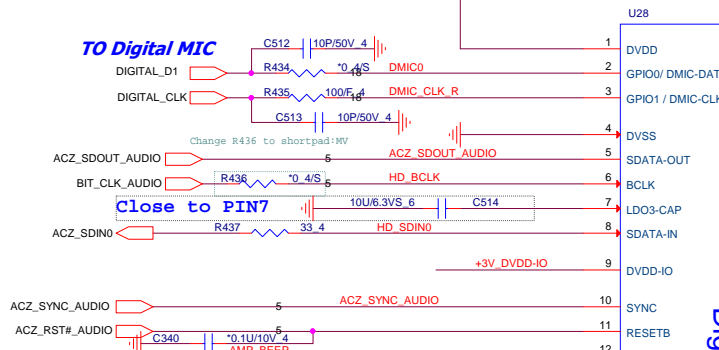


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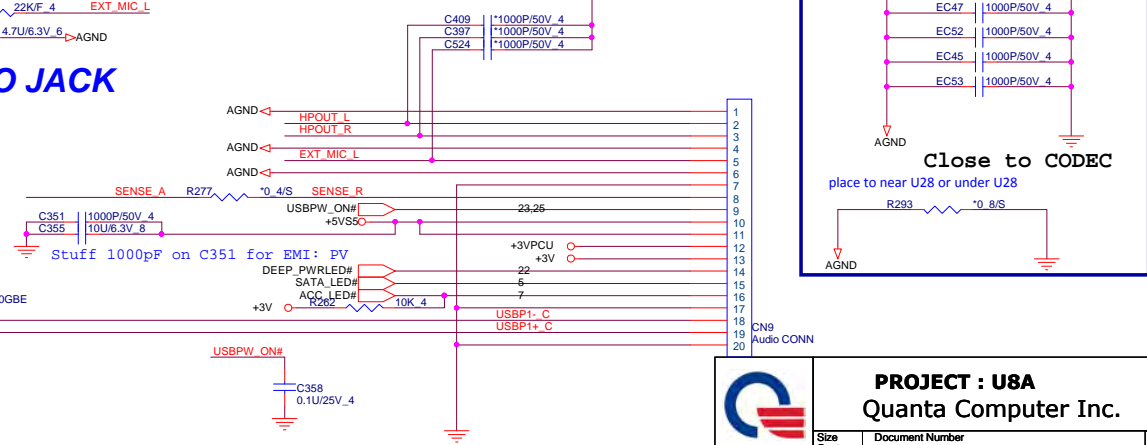
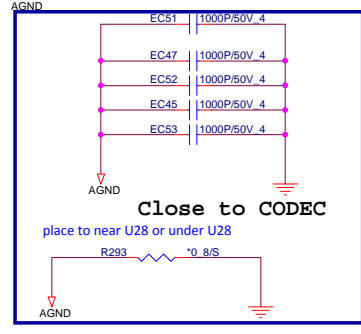
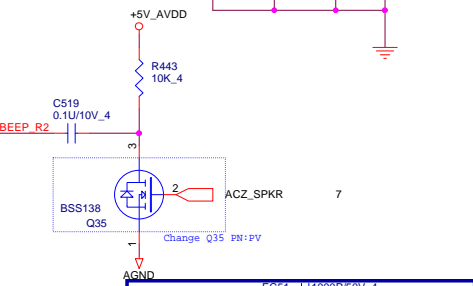
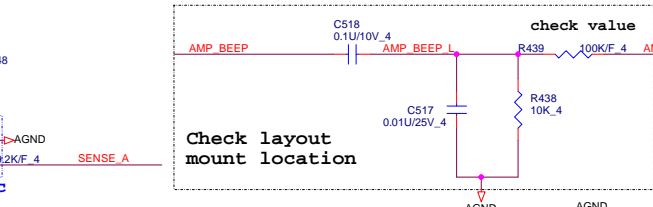
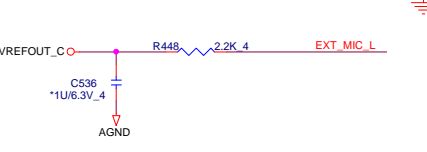
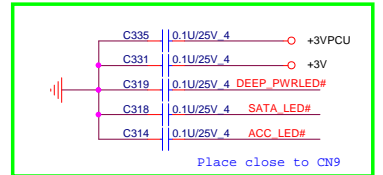
Size Custom	Document Number LCD/HDMI/Camera/D-MIC	Rev 1A
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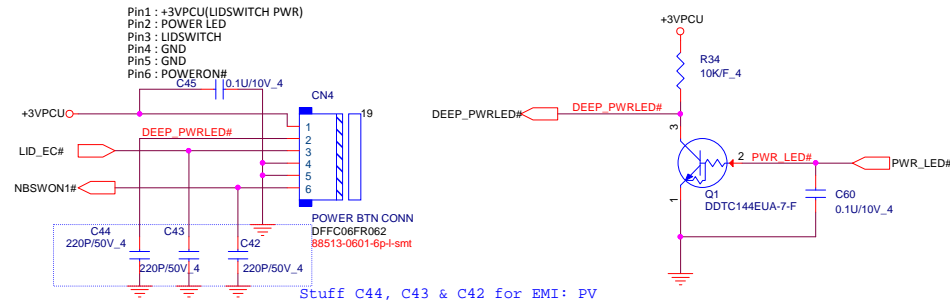
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9,24,28,32



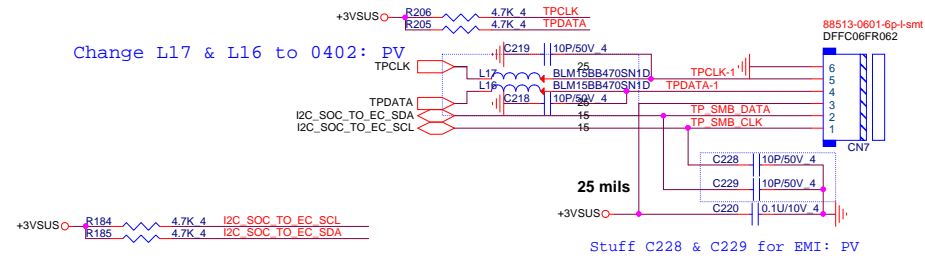
USB 2.0 AND AUDIO COMBO JACK



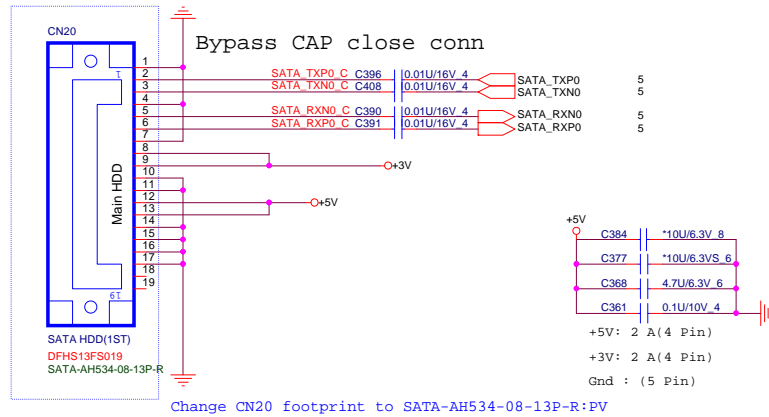
Power Botton Connector



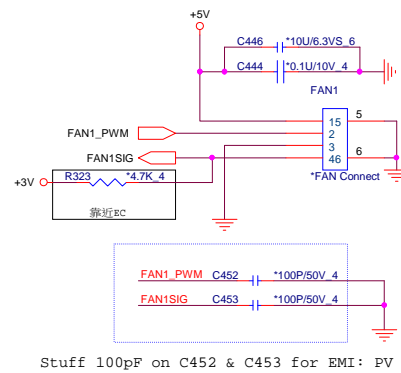
Touch Pad Connector



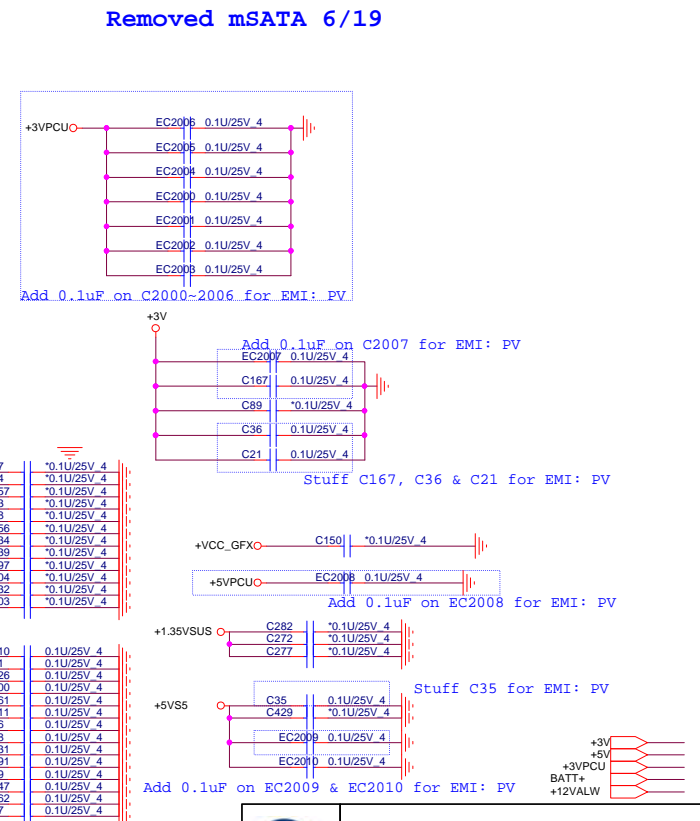
SATA HDD Connector(Cable type)



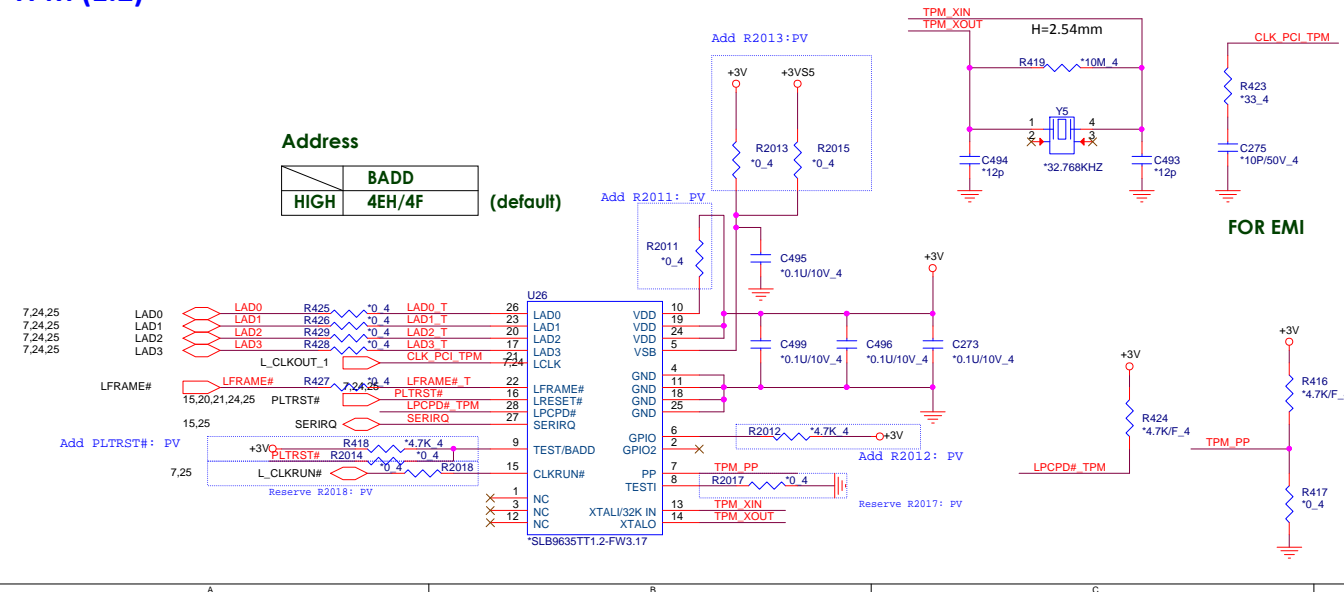
FAN

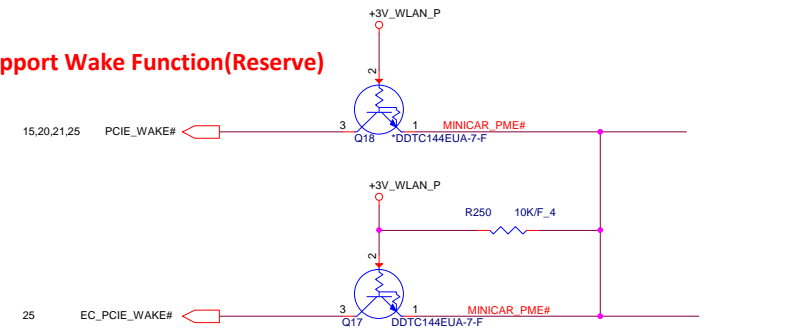
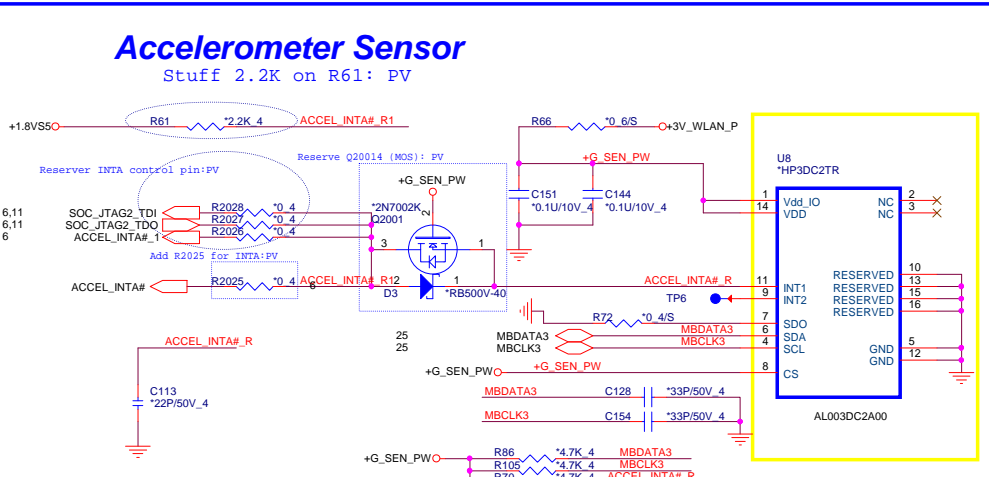
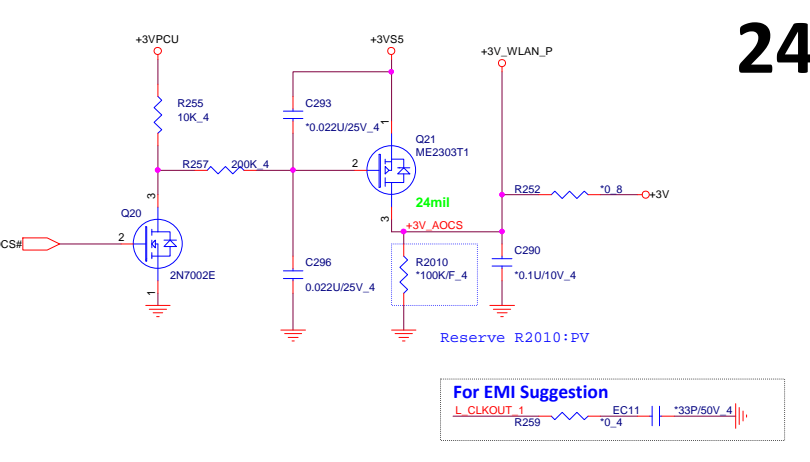
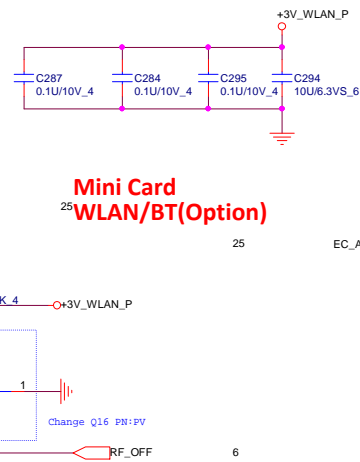
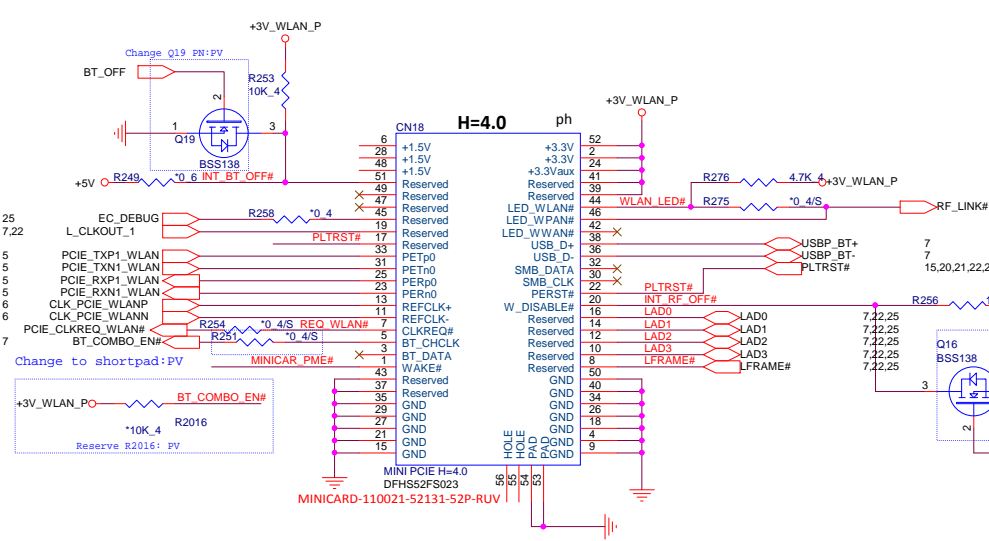


Mini PCI-E Card 2- Full size mSATA

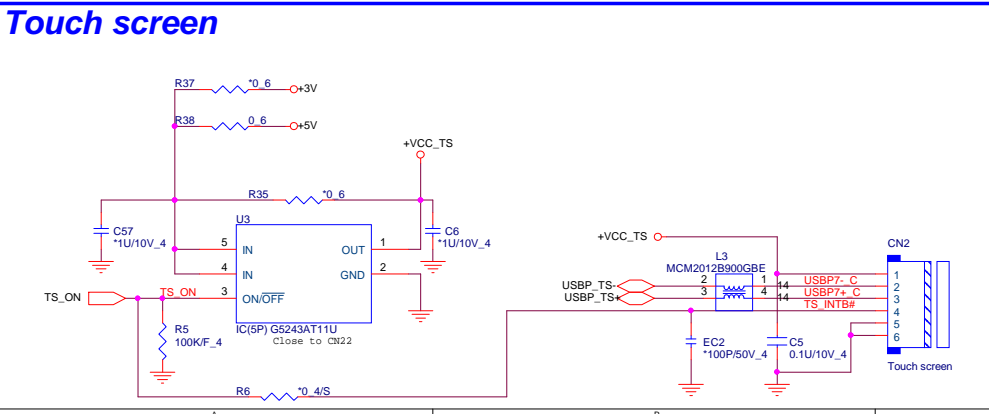


TPM (1.2)





Green CLK Circuitry

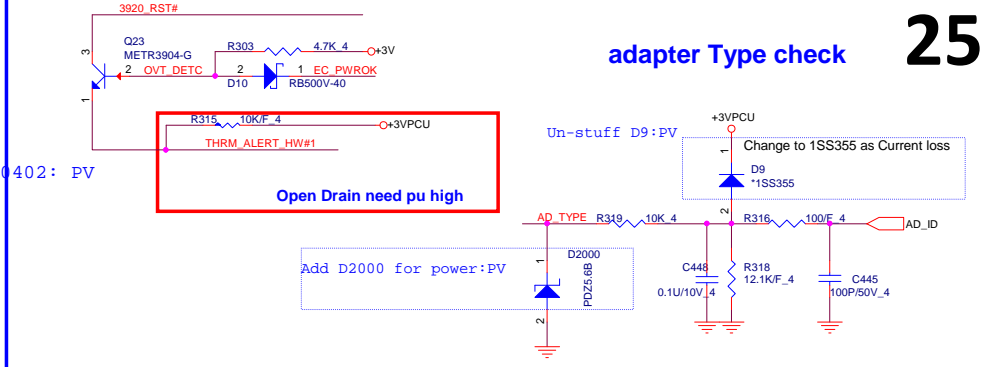


+3V
+5V
+3VPCU

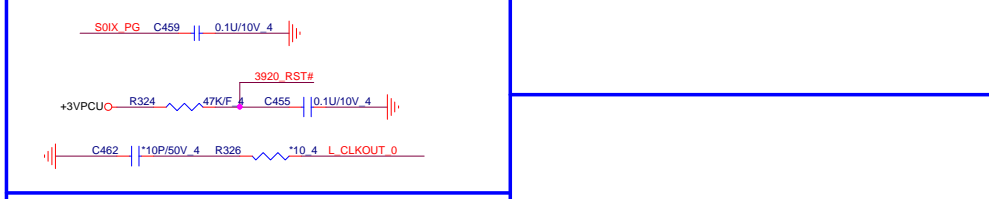
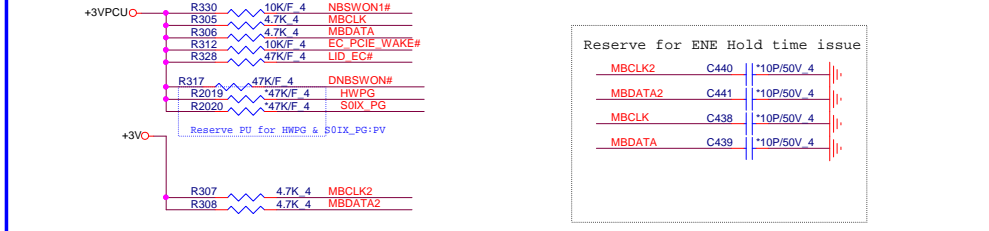
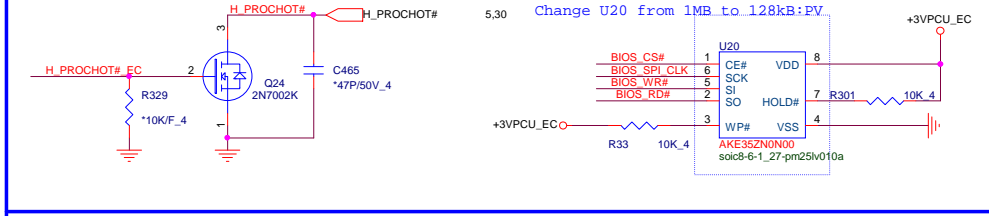
4,9,11,12,13,14,15,17,18,19,20,21,22,23,25,32
12,18,19,21,22,23,32
6,15,19,22,23,25,26,27

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		Quanta Computer Inc.	
Size	Document Number	Rev	
Custom	WLAN/G-Sensor/G-CLK/TS	1A	
Date: Thursday, April 23, 2015	Sheet	24	of 37

adapter Type check



Vender	Size	P/N
WINBOND	128KB	W25X10CLSNIG(AKE35ZN000)
MXIC	128KB	MX25L1006EMI-10G(AKE35FN020)
Socket		DFHS08FS023



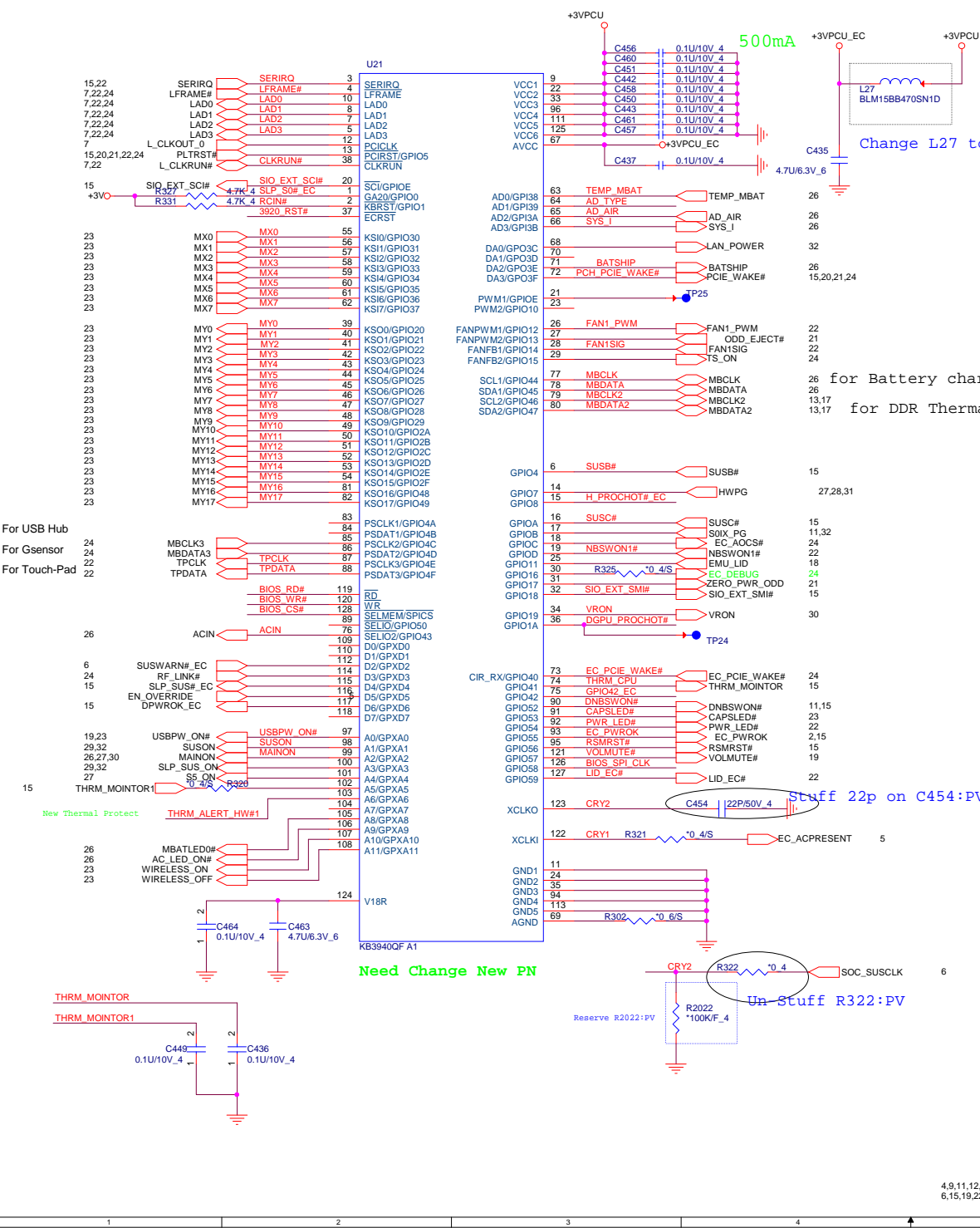
PROJECT : U8A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC (KB3940)	1A
Date: Thursday, April 23, 2015		Sheet 25 of 37

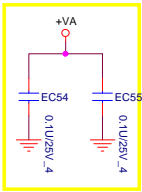
4,9,11,12,13,14,15,17,18,19,20,21,22,23,24,32

6,15,19,22,23,24,26,27 +3VPCU

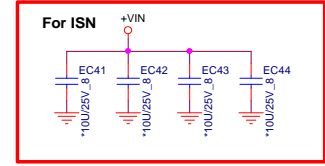
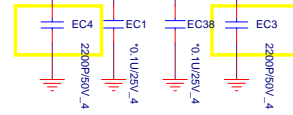


PV modify 0905

+VAD



PV modify 0905



For ISN

DC JACK 90W

Place this ZVS close to INPUT

Place this ZVS close to Far-Far away +VIN

Place this Rsense close to Battery connect

To PWR LED

PV modify 0902

PV modify 0902

PV modify 0902

OZ8691ALN

PV modify 0902

PV modify 0902

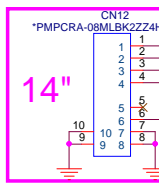
PV modify 0902

VAC= AC Adapter detection
ACAV = To indicate the adapter status.
 Pin ACAV goes high when Vvac > 8.7V/13.2V & Vvac > Vichm + 0.8V the Vvac = 8,7 or 13.2V threshold can be chosen via Smbus comment

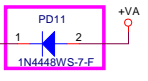
Place this cap close to EC

15"

Place this cap close to EC



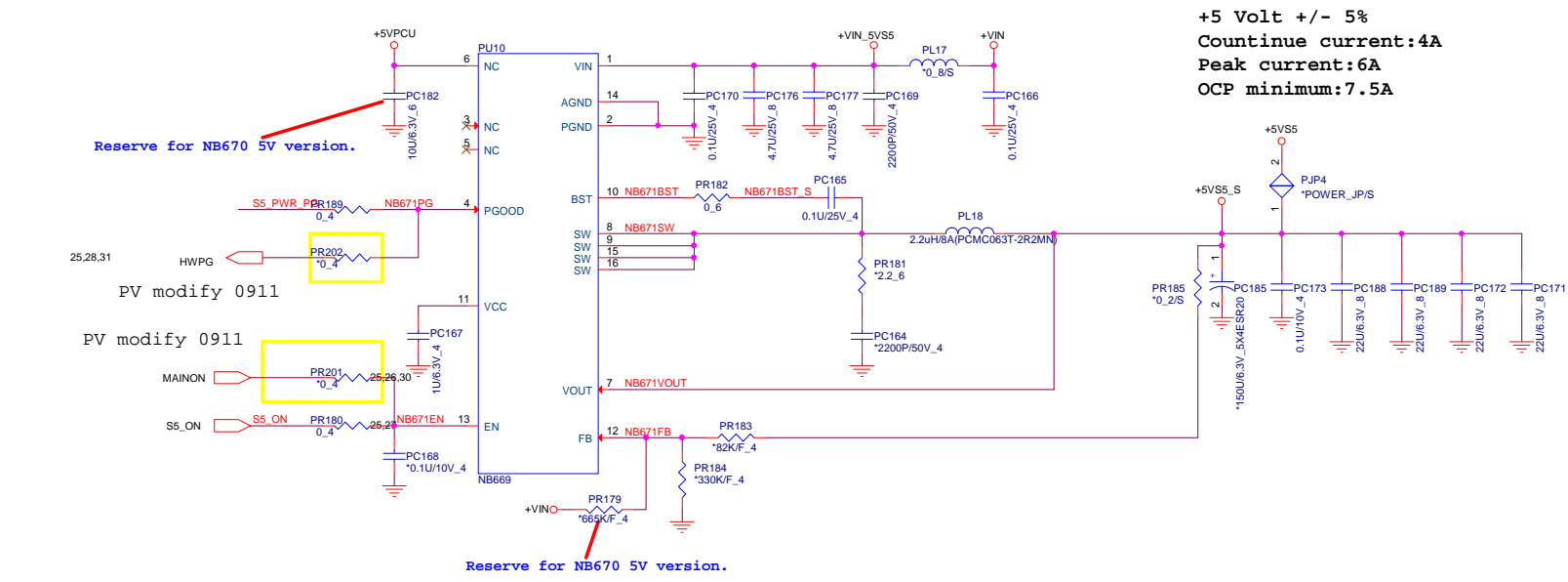
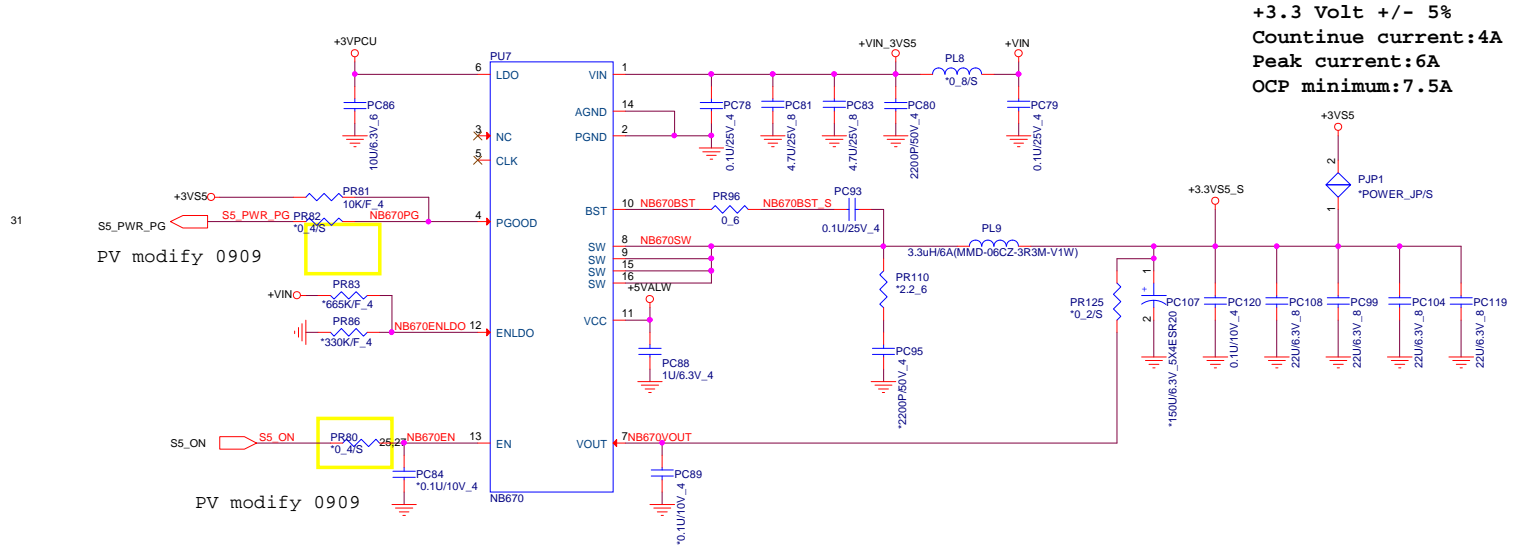
14"



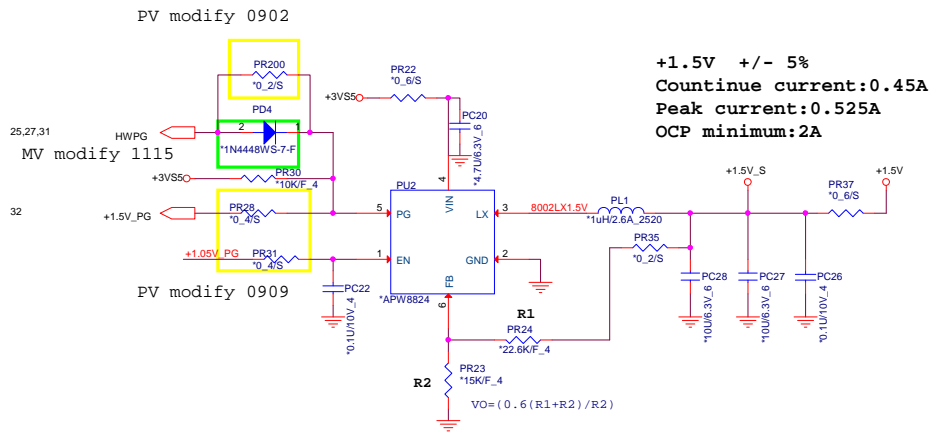
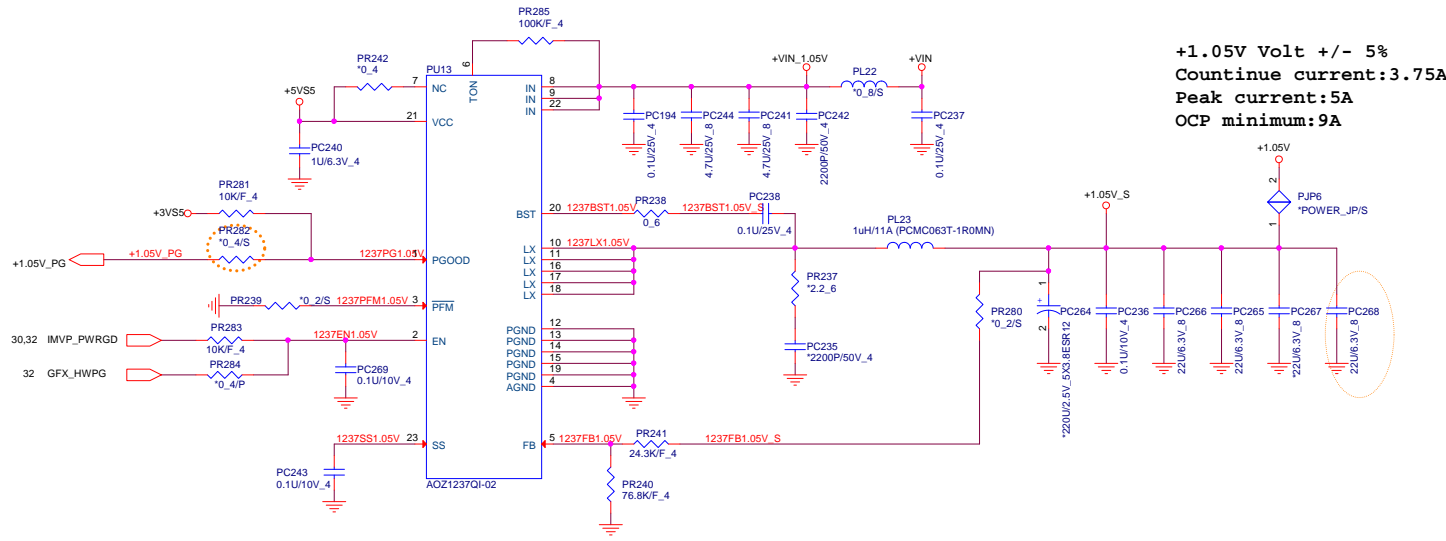
Place this cap close to EC

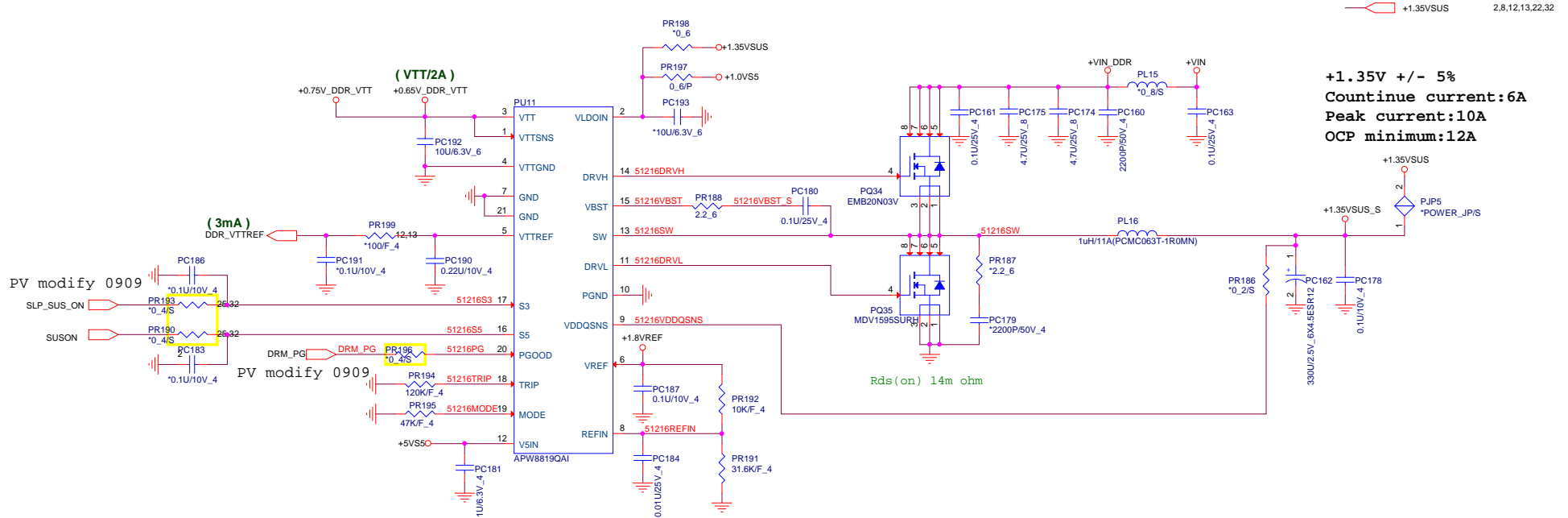
		PROJECT : U8A	
		Quanta Computer Inc.	
Size Custom	Document Number	Charger (OZ8691)	
Date: Thursday, April 23, 2015			
NB5	Rev 1A	Sheet 26 of	37

DC/DC +3VS5/+5VS5



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	Quanta Computer Inc.		
	Size Custom	Document Number 3/5VPCU(NB670/NB669)	
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+1.35VSUS 2.8,12,13,22,32

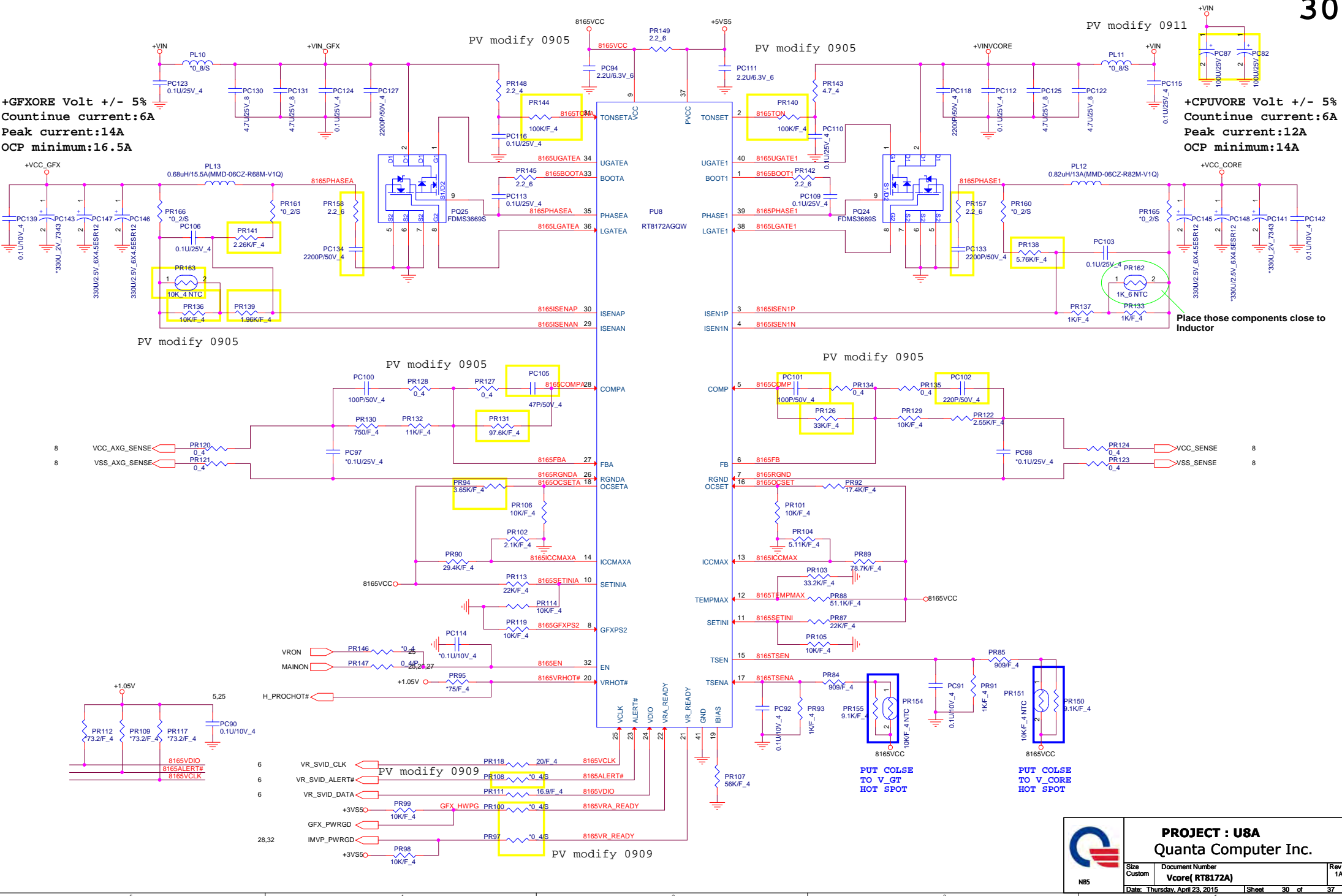
+1.35V +/- 5%
Continue current: 6A
Peak current: 10A
OCP minimum: 1.2A

Rds(on) 14m ohm

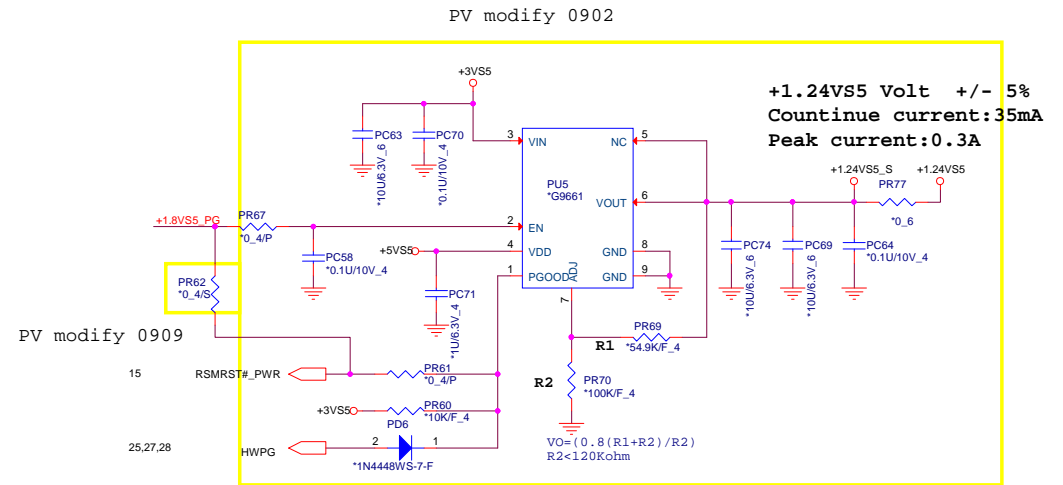
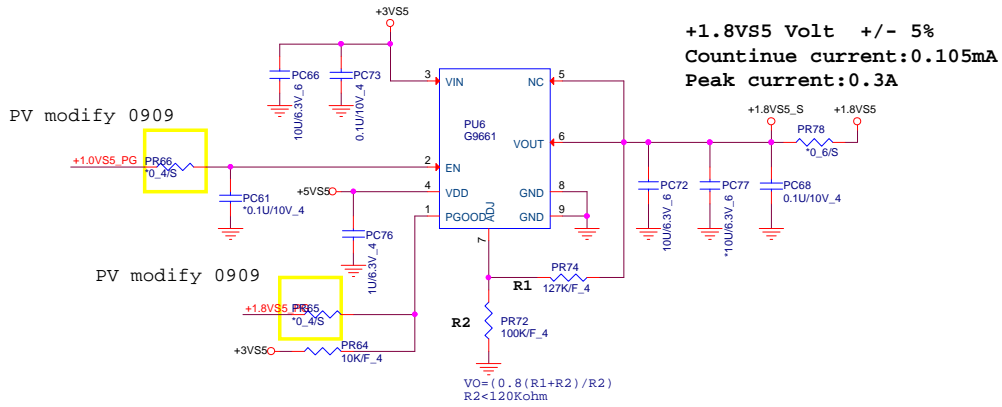
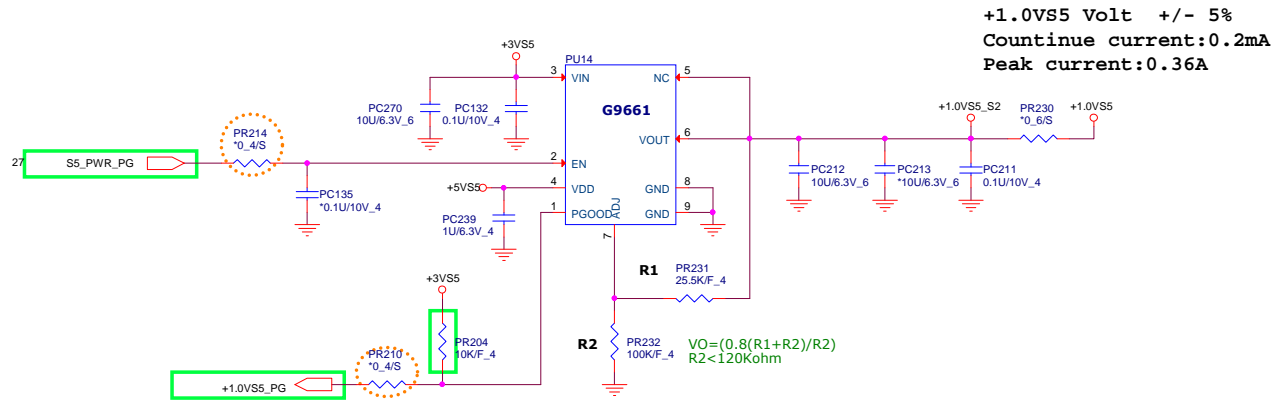
 NB5	PROJECT : U8A		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number DDR3 (APW8819)	
		Sheet 29 of 37	37

+GFXORE Volt +/- 5%
Countinue current:6A
Peak current:14A
OCP minimum:16.5A

+CPUVORE Volt +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum:14A



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USB3.0	Port Assignment	Power control pin
PORT0	USB HUB	

USB2.0	Port Assignment	Power control pin
PORT0	USB HUB	N/A
PORT1	Right side USB Daughter BD	USBPW_ON#(from EC)
PORT2	BT	N/A
PORT3	Camera	N/A

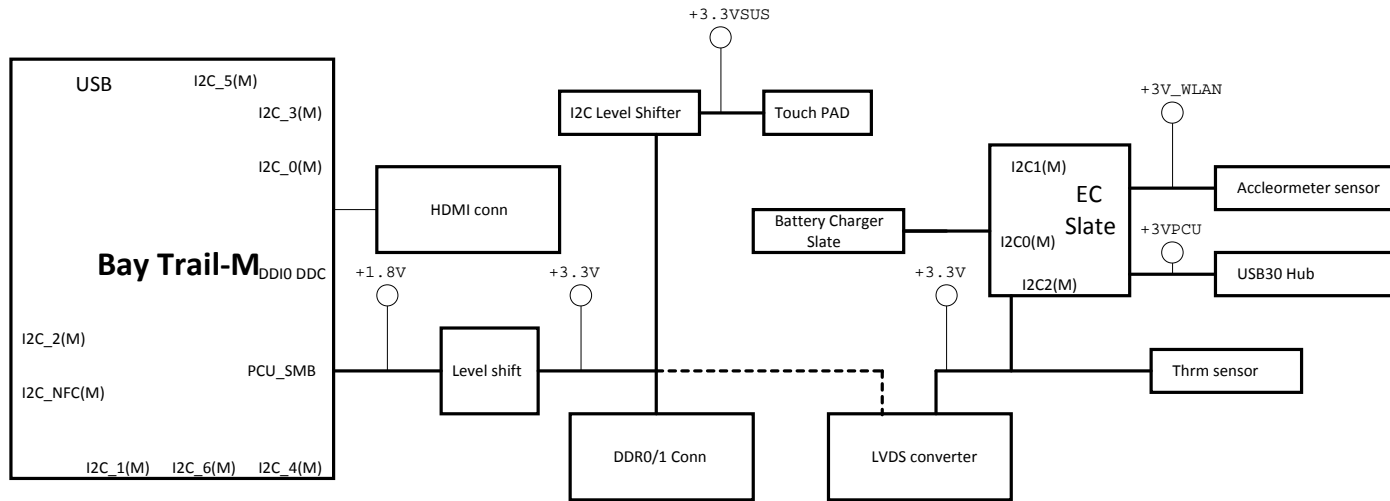
USB HUB	Port Assignment	Power control pin
USB30 PORT1	USB2.0/USB3.0 COMBO 1ST	USBPW_ON#(from EC)
USB30 PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
USB30 PORT3	N/A	
USB30 PORT4	N/A	
USB20 PORT1	USB2.0/USB3.0 COMBO 1ST	USBPW_ON#(from EC)
USB20 PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
USB20 PORT3	TS	TS_ON
USB20 PORT4		

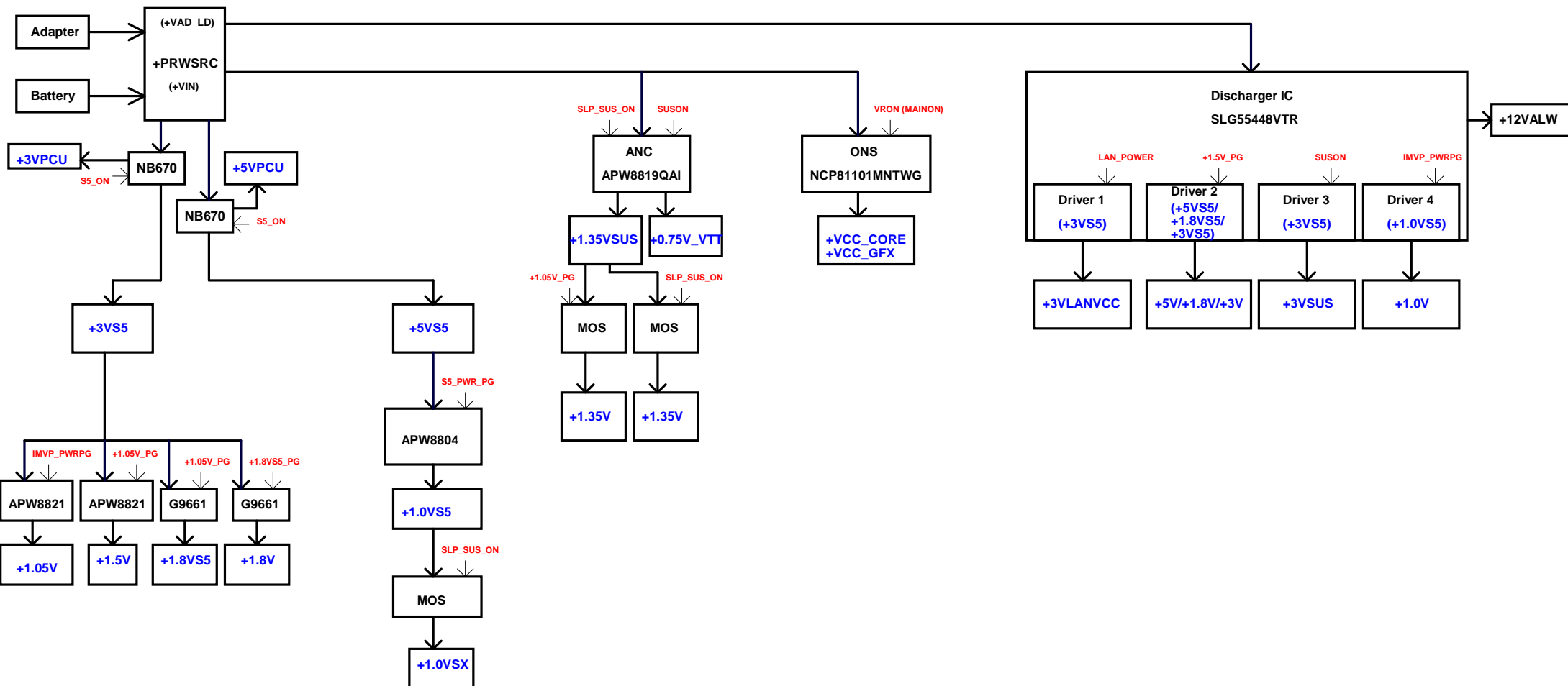
SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	ODD	ZERO_PWR_ODD

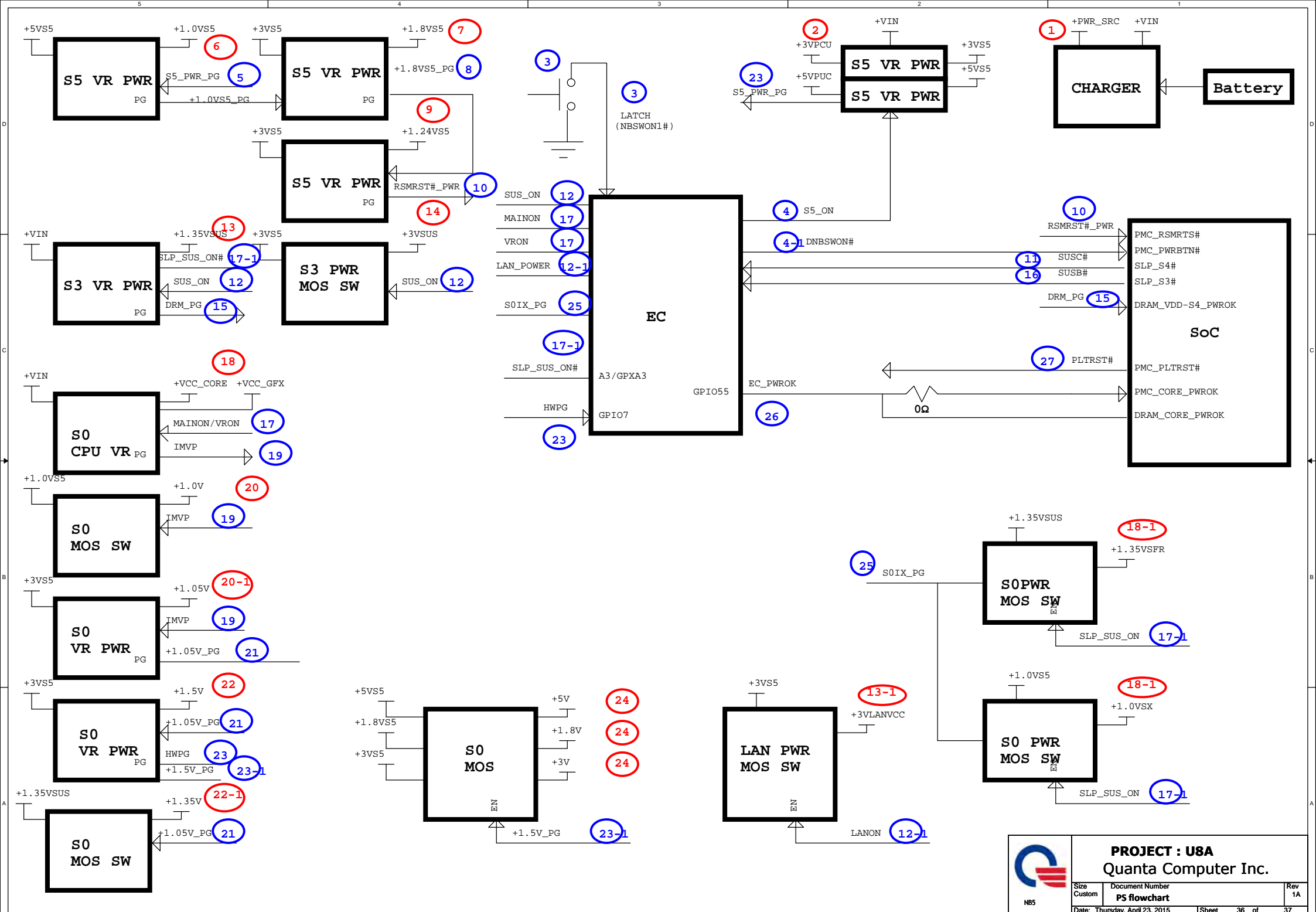
PCIE	Port Assignment	Control pin
PCIE 0	Card reader	
PCIE 1	WLAN	
PCIE 2	LAN	
PCIE 3	NC	

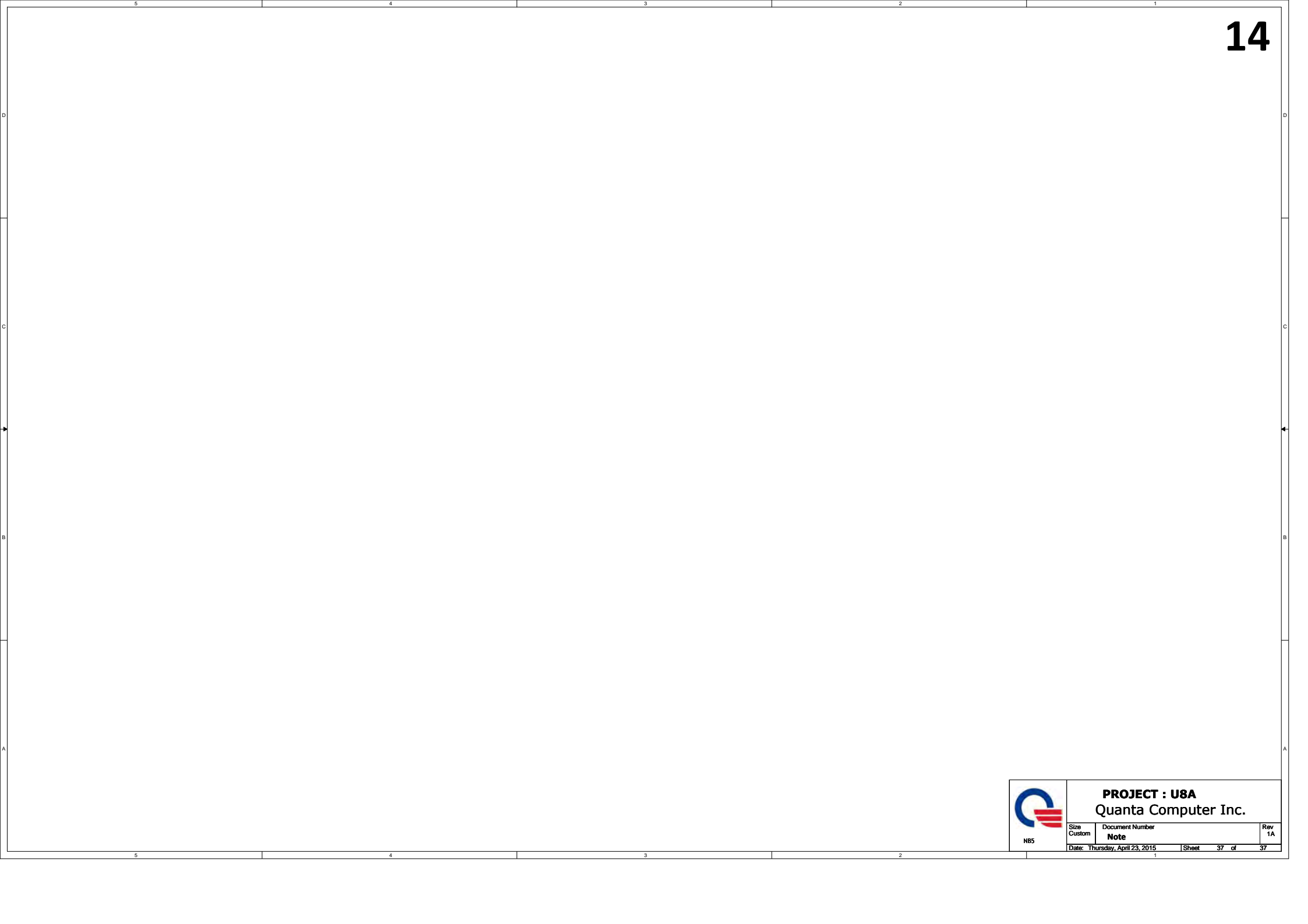



PROJECT : USA
Quantia Computer Inc.









 NB5	PROJECT : USA		
	Quanta Computer Inc.		
Size Custom	Document Number Note	Rev 1A	
Date: Thursday, April 23, 2015		Sheet	37 of 37