LCFC Confidential

G Project M/B Schematics Document

AMD FP4 Bristol Ridge and Stoney Ridge SOC with DDRVI

AMD R16M-M1-30

2015-06-06

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: Cover Page		
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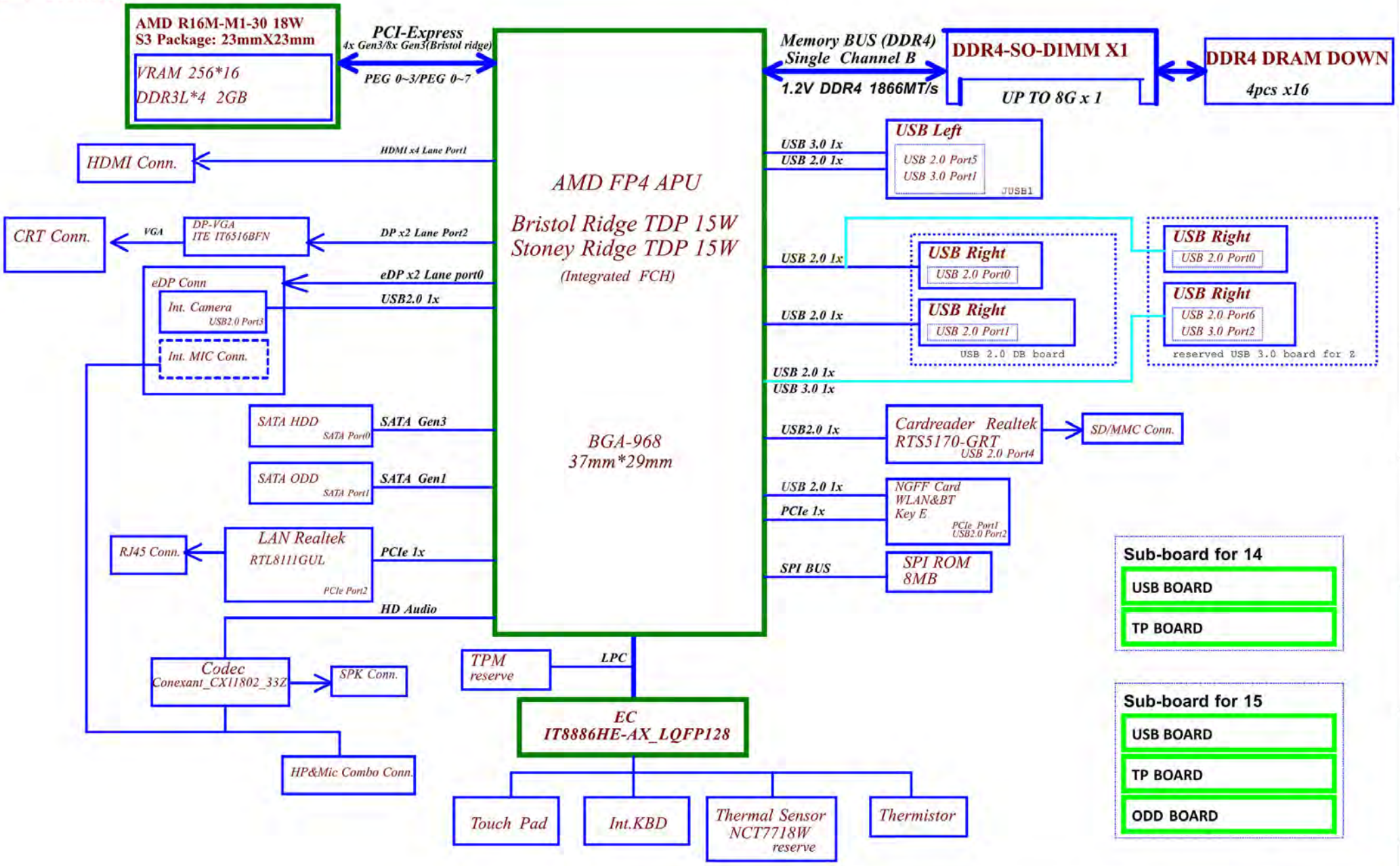
File Name : Toronto



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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

power plane / State	B+ (+20VSB) +3VL +5VLP	+5VALW +3VALW (+3VALW_APU) +1.8VALW +0.95VALW +0.775VALW	+1.2V (+VSYSMEM_APU)	+5VS +3VS +1.8VS +1.5VS +0.95VS +0.6VS +2.5VS +APU_CORE +APU_CORE_NB +APU_GFX +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

DRAM Config.	BOARD_ID0 APIO8	BOARD_ID1 AGPIO10	BOARD_ID2 AGPIO16 internal pull up 40K
	0: 14''	0: Dis	0: No KBL
	1: 15''	1: UMA	0: KBL

USB Port Table

USB 2.0	USB 3.0	Port	ST Port device	BR Port device
EHCI0		0	RIGHT USB (2.0)	RIGHT USB (2.0)
		1	RIGHT USB (2.0)	N/A
		2	Blue Tooth	Blue Tooth
		3	Camera	Camera
xHCI	0	4	Card Reader USB 2.0 bus	Card Reader USB 2.0bus
	1	5	LEFT USB (3.0)	LEFT USB (3.0)
	2	6	N/A	RIGHT USB (3.0)
	3	7	N/A	N/A

SMBUS Control Table

X

	SOURCE	GPU	BATT	IT8586E	SODIMM	WLAN	Thermal Sensor	APU	Charger	PMIC	Vcore VR	GFXcore VR
EC_SMB_CK0 EC_SMB_DA0	IT886H +3VL	X	X		X	X	X	X	X	V	X	V +3VALW
EC_SMB_CK1 EC_SMB_DA1	IT886H +3VL	X	V		X	X	X	X	V	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT886H +3VS	V +3VS_VGA	X		X	X	V	V 1.8VS	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT886H +3VALW	X	X		X	X	X	X	X	X	V	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V	V	X		X	X	X	X

PCIE PORT LIST

	Port	Device	
GPP	0	N/A	
	1	WLAN	
	2	LAN	
	3	N/A	
GFX	0	ST GPU	BR GPU
	1		
	2		
	3		
	4	N/A	
	5		
	6		
	7		

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
ME@	Connector
14@	For 14" part
15@	For 15" part
EMC@	EMC Part
EMC_NS@	EMC reserve Part
EMC_14@	EMC 14 part
EMC_15@	EMC 15 part
RF@	RF Part
RF_PXNS@	RF GPU reserve part
UMA@	UMA SKU ID part
PX@	Discrete GPU SKU part
EXO@	EXO GPU Part
TOPAZ@	TOPAZ GPU Part
TPM@	TPM part
KBL@	keyboard backlight part
HDT@	HDT Debug part
BR@	Bristol Ridge Part
ST@	Stoney Ridge part
BRPX@	Bristol Ridge Discrete Part
S4GX4@	X76 SAMSUNG 2G
M4GX4@	X76 MICRON 2G
H4GX4@	X76 HYNIX 2G
S2G@	SAMSUNG 2G
M2G@	MICRON 2G
H2G@	HYNIX 2G
HDMI@	HDMI Logo

VRAM

EC SM Bus0 address

Device	Address
PMIC	?
GFXcore VR	?

EC SM Bus1 address

Device	Address
Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor	1001_100xb(reserve)
GPU	0x41(default)
APU SB-TSI	releate to F3x1E4[SbiAddr] or Address Select Pins setting

EC SM Bus3 address

Device	Address
Vcore VR	?

APU SM Bus address

Device	Address
DDR4 SO-DIMM	?
WLAN	RSVD

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Title: Notes List

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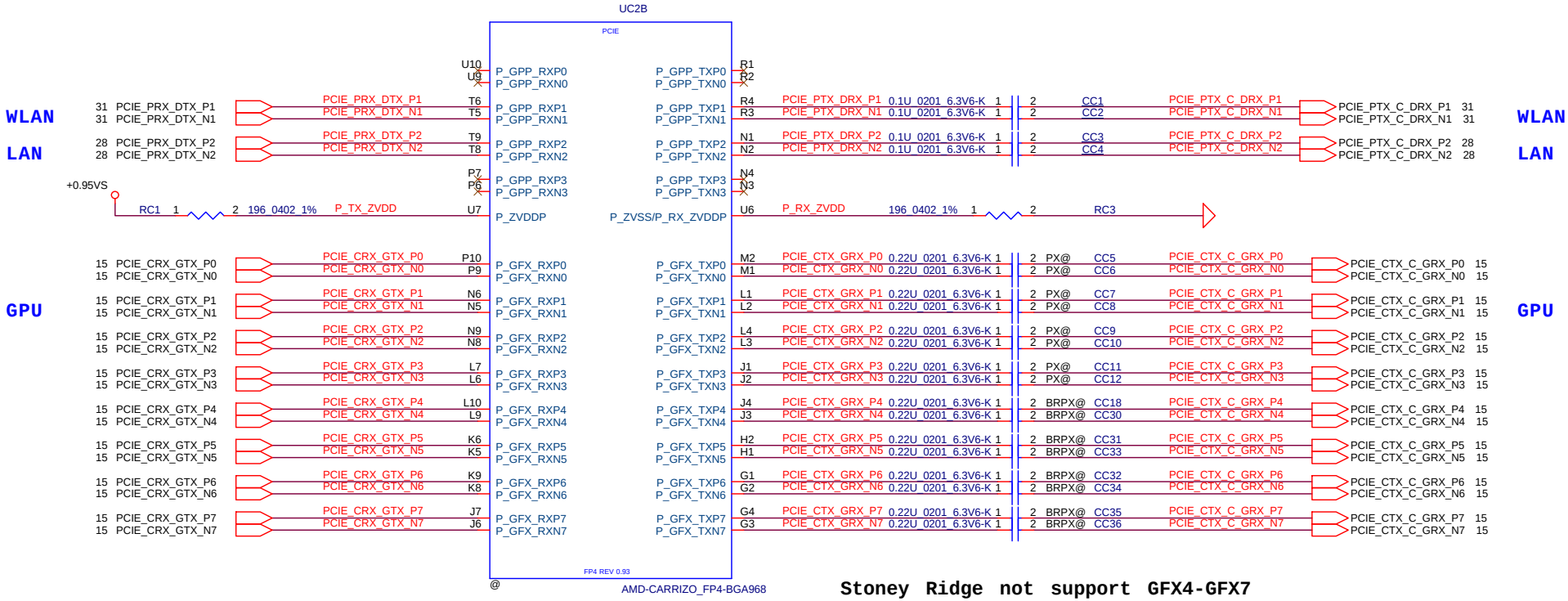

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Title: **FP4 (PCIE I/F)**

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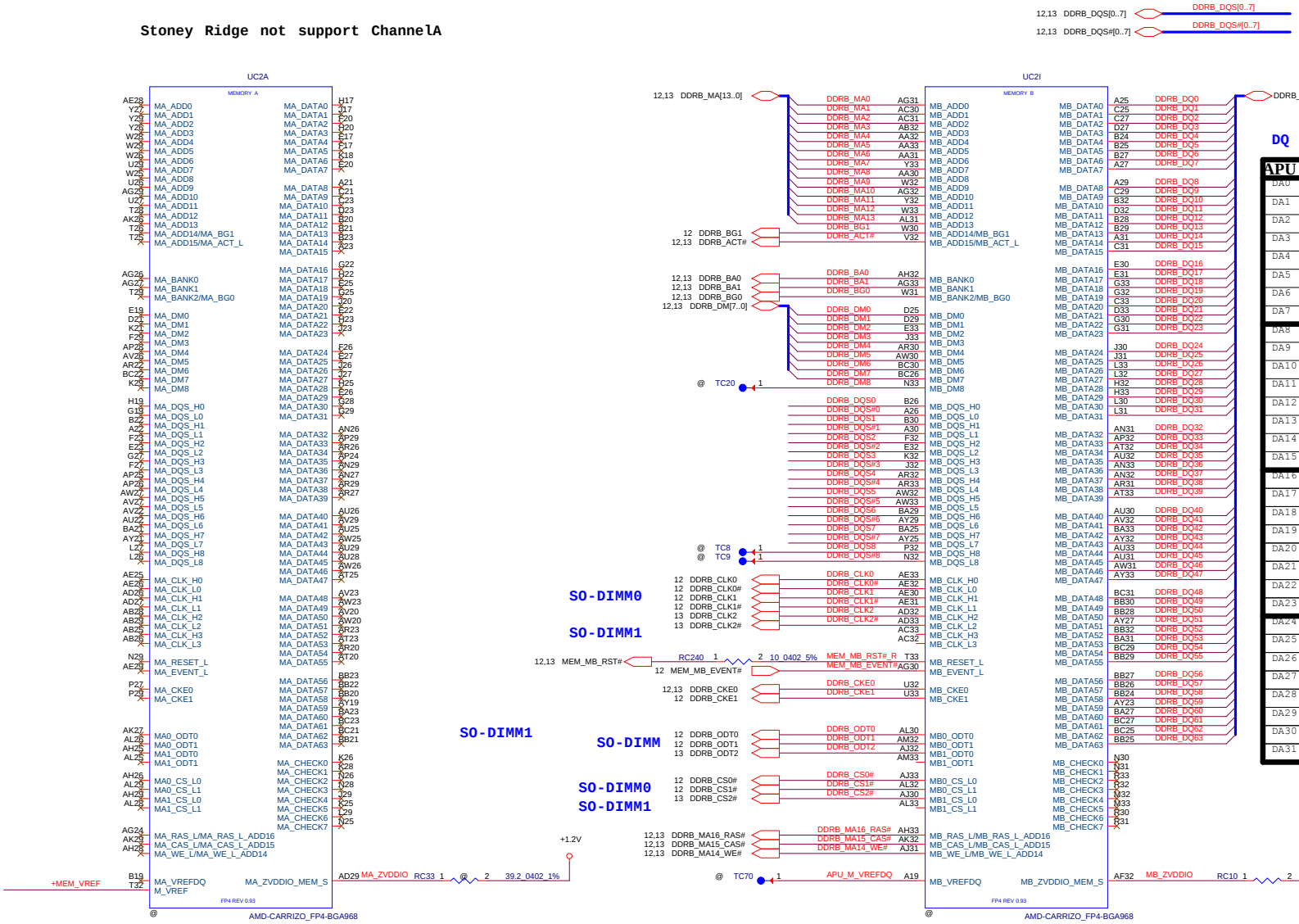
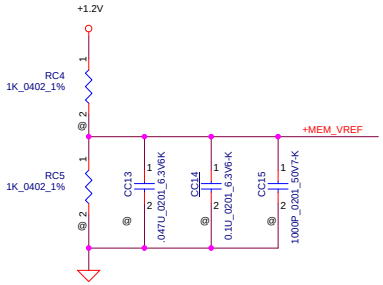
Stoney Ridge not support ChannelA



DQ bit swapping is allowed in a byte lane.

APU	SO-DIMM	DRAM
DA0	DQ2	UD1.0
DA1	DQ7	UD1.3
DA2	DQ6	UD1.4
DA3	DQ0	UD1.5
DA4	DQ1	UD1.2
DA5	DQ5	UD1.7
DA6	DQ4	UD1.1
DA7	DQ3	UD1.6
DA8	DQ12	UD1.11
DA9	DQ13	UD1.9
DA10	DQ11	UD1.12
DA11	DQ10	UD1.14
DA12	DQ9	UD1.13
DA13	DQ8	UD1.15
DA14	DQ15	UD1.8
DA15	DQ14	UD1.10
DA16	DQ20	UD2.7
DA17	DQ16	UD2.3
DA18	DQ19	UD2.4
DA19	DQ18	UD2.1
DA20	DQ17	UD2.0
DA21	DQ21	UD2.2
DA22	DQ22	UD2.6
DA23	DQ23	UD2.5
DA24	DQ24	UD2.9
DA25	DQ28	UD2.11
DA26	DQ30	UD2.12
DA27	DQ26	UD2.8
DA28	DQ25	UD2.13
DA29	DQ29	UD2.15
DA30	DQ27	UD2.14
DA31	DQ31	UD2.10

APU	SO-DIMM	DRAM
DA32	DQ39	UD3.1
DA33	DQ36	UD3.6
DA34	DQ35	UD3.2
DA35	DQ34	UD3.7
DA36	DQ37	UD3.5
DA37	DQ32	UD3.3
DA38	DQ38	UD3.4
DA39	DQ33	UD3.0
DA40	DQ45	UD3.15
DA41	DQ44	UD3.9
DA42	DQ47	UD3.14
DA43	DQ46	UD3.8
DA44	DQ40	UD3.13
DA45	DQ41	UD3.11
DA46	DQ43	UD3.12
DA47	DQ42	UD3.10
DA48	DQ55	UD4.0
DA49	DQ49	UD4.3
DA50	DQ54	UD4.2
DA51	DQ48	UD4.7
DA52	DQ53	UD4.5
DA53	DQ52	UD4.1
DA54	DQ50	UD4.6
DA55	DQ51	UD4.4
DA56	DQ61	UD4.14
DA57	DQ56	UD4.10
DA58	DQ63	UD4.11
DA59	DQ58	UD4.12
DA60	DQ60	UD4.13
DA61	DQ57	UD4.9
DA62	DQ59	UD4.15
DA63	DQ62	UD4.8



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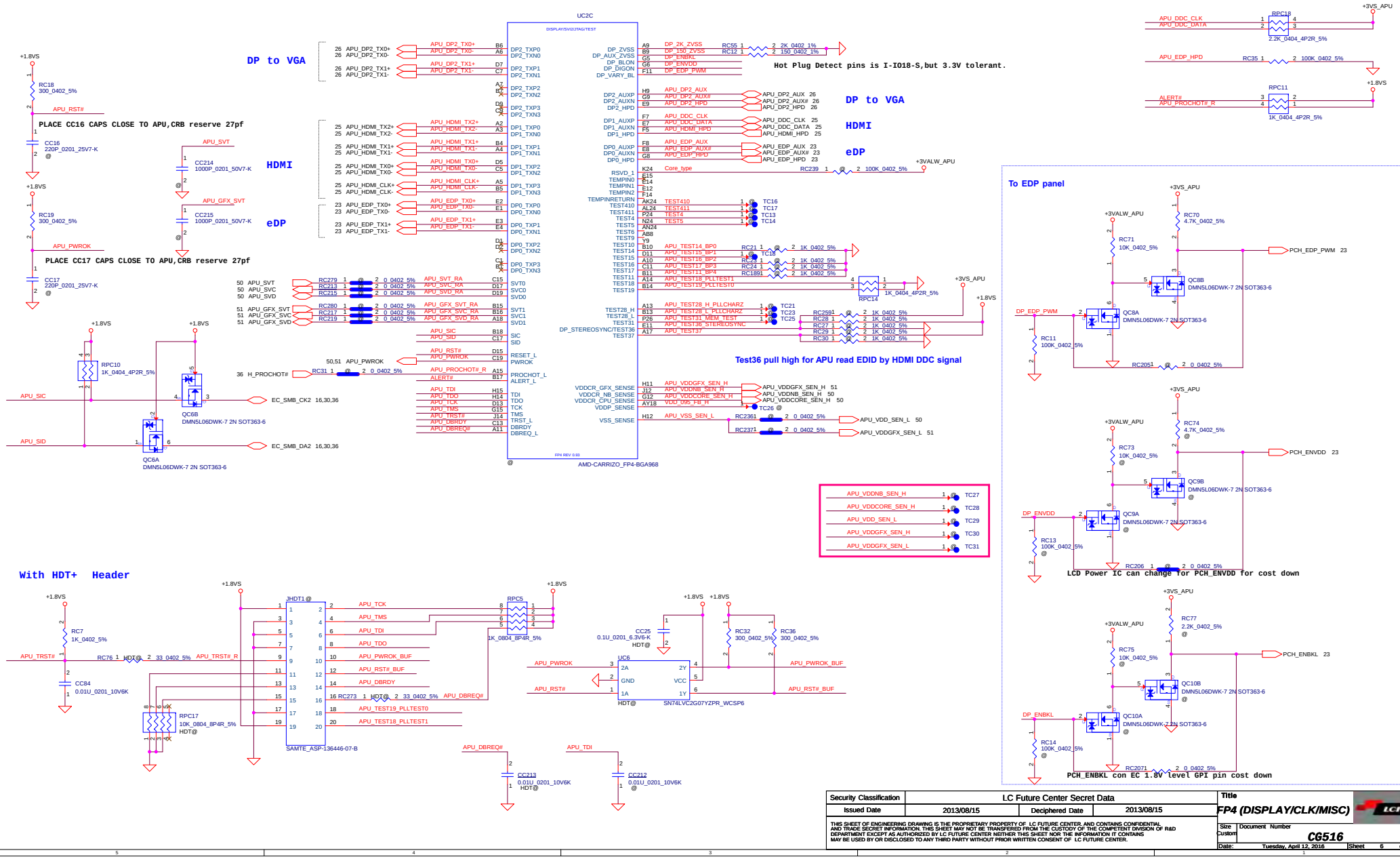

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Title	FP4 (DISPLAY/CLK/MISC)		
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30,36 APU_LPC_RST# — RC46 33_0402_5% — LPC_RST#_R; CC20 150P_0402_50V8-J

15,28,31 PLT_RST# — RC38 33_0402_5% — PCIE_RST#_R; RC43 100K_0402_5%; CC19 100P_0201_25V8J

+1.8VALW — RC243 0_0402_5%; RC53 1K_0402_5%; DC1 RB751V-40_SOD323-2; 36 EC_RSMRST# — RSMRST#_R; CC21 0.1U_0402_25V6

EC set RSMRST OD output

Connected to 10-ms RC-delay circuit on VDD_18_S5 power rail. (CRB PWR Dealy: 22K/0.1uF)

+3VALW_APU — RC39 10K_0402_5% 15@; RC40 10K_0402_5% UMA@; RC41 10K_0402_5% NOKBL@; RC257 10K_0402_5% @; RC265 10K_0402_5% @; RC263 10K_0402_5% @; RC268 2K_0402_5% @

BOARD_ID0 … BOARD_ID6

RC47 10K_0402_5% 14@; RC269 10K_0402_5% PX@; RC49 2K_0402_5% KBL@; RC258 2K_0402_5% @; RC264 2K_0402_5% @; RC266 2K_0402_5% @; RC267 10K_0402_5% @

ID2--5 internal pull up 40K
ID6 internal pull low 40K

+3VS_APU — RC72 10K_0402_5% @; 36 EC_SYS_PWRGD — RC95 0_0402_5% — SYS_PWRGD_R; CC22 0.1U_0201_6.3V6-K @

PCIE_WAKE#_RA — RC88 0_0402_5%; AGPIO5 — RC92 0_0402_5% — PCIE_WAKE# 28,31,36; DC3 SDM10U45LP-7_DFN1006-2-2 @

+3VALW_APU — RC84 2.2K_0402_5% @; RC85 1K_0402_5% @; RC20 2.2K_0402_5% @; TEST0; TEST1; TEST2; RC195 15K_0402_5%; RC196 15K_0402_5%; RC197 15K_0402_5%

SYS_RESET# — DC4 RB751V-40_SOD323-2 @ — SYS_PWRGD_R; CC38 0.1U_0201_6.3V6-K

Max ESR < 65K ohm !!

2/22: change to 50K ohm for Crystal vendor suggest

+3VS_APU — RC98 PX@ 10K_0402_5%; RC101 100K_0402_5% — PXS_PWREN_R

+3VS_APU — RC100 @ 10K_0402_5%; RC104 UMA@ 2K_0402_5% — VR_VGA_PWRGD

UC2D — ACPI/SDI/AZ/GPIO/RTC/I2C/UART/MISC

LPC_RST# AN7; RSMRST# AE4; PWR_BTN_L/AGPIO0 AE1; PWR_GOOD BC9; SYS_RESET_L/AGPIO1 AF2; WAKE_L/AGPIO2 AG2; SLP_S3_L AK7; SLP_S5_L AH5; S0A3_GPIO/AGPIO10 AE8; S5_MUX_CTRL/EGPIO42 AH8; TEST0 AH6; TEST1/TMS AK8; TEST2 AE3; ESPI_RESET_L/KBRST_L/AGPIO129 AY15; GA20IN/AGPIO126 BC19; LPC_PME_L/AGPIO22 AD7; LPC_SMI_L/AGPIO86 BB13

AC_PRES/USB_OC4_L/IR_RX0/AGPIO23 AG3; IR_TX0/USB_OC5_L/AGPIO13 AD5; IR_TX1/USB_OC6_L/AGPIO14 AL8; IR_RX1/AGPIO15 AN8; IR_LED_L/LLB_L/AGPIO12 AE2; CLK_REQ0_L/SATA_ISO_L/SATA_ZP0_L/AGPIO92 BC15; CLK_REQ1_L/AGPIO115 BB17; CLK_REQ2_L/AGPIO116 BC17; CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO131 BB18; CLK_REQG_L/OSCIN/EGPIO132 BB16; USB_OC0_L/TRST_L/AGPIO16 AH9; USB_OC1_L/TDI/AGPIO17 AG1; USB_OC2_L/TCK/AGPIO18 AH2; USB_OC3_L/TDO/AGPIO24 AL9

AZ_BITCLK/I2S_BCLK_MIC AU6; AZ_SDIN0/I2S_DATA_MIC0 AR8; AZ_SDIN1/I2S_LR_PLAYBACK AP6; AZ_SDIN2/I2S_DATA_MIC1 AR5; AZ_RST_L/I2S_LR_MIC AU9; AZ_SYNC/I2S_BCLK_PLAYBACK AT9; AZ_SDOUT/I2S_DATA_PLAYBACK AR7

I2C0_SCL/EGPIO145 BB10; I2C0_SDA/EGPIO146 BB9; I2C1_SCL/EGPIO147 BB7; I2C1_SDA/EGPIO148 BC7

RTCCLK AG7

X32K_X1 AT1; X32K_X2 AT2

SD0_WP/EGPIO101 BB2; SD0_PWR_CTRL/AGPIO102 BB5; SD0_CD/AGPIO25 BC2; SD0_CLK/EGPIO95 BB4; SD0_CMD/EGPIO96 AY5

SD0_DATA0/EGPIO97 BC3; SD0_DATA1/EGPIO98 BA3; SD0_DATA2/EGPIO99 BC5; SD0_DATA3/EGPIO100 BA5; SD0_LED/EGPIO93 BB6

SCL0/I2C2_SCL/EGPIO113 BA15; SDA0/I2C2_SDA/EGPIO114 AY17 — APU_SMB_CLK 12,31; APU_SMB_DATA 12,31

SCL1/I2C3_SCL/AGPIO19 AG5; SDA1/I2C3_SDA/AGPIO20 AG4

AGPIO3 AL5; AGPIO4 AL6; AGPIO5 AJ1; AGPIO6/LDT_RST_L AJ3; AGPIO7/LDT_PWROK AH1; AGPIO8 AJ4; AGPIO9 AK5; VDDGFX_PD/AGPIO39 AD8; AGPIO40 AG8; AGPIO64 AW15; AGPIO65 AU15

APU_SHUTDOWN# AT15; HVB_EN AU12; AGPIO69 AT14; AR14; BC13

SPKR/AGPIO91 BA17; BLINK AN5

GENINT1_L/AGPIO89 BB14; GENINT2_L/AGPIO90 BA19; VR_VGA_PWRGD

FANIN0/AGPIO84 BC18; FANOUT0/AGPIO85 BB19 — PXS_PWREN_R

UART0_CTS_L/EGPIO135 AY9; UART0_RXD/EGPIO136 AW8; UART0_RTS_L/EGPIO137 AV5; UART0_TXD/EGPIO138 AV8; UART0_INTR/AGPIO139 AW9

UART1_CTS_L/BT_I2S_BCLK/EGPIO140 AV11; UART1_RXD/BT_I2S_SDI/EGPIO141 AU7; UART1_RTS_L/EGPIO142 AT11; UART1_TXD/BT_I2S_SDO/EGPIO143 AR11; UART1_INTR/BT_I2S_LRCLK/AGPIO144 AP9

FP4 REV 0.93

@ AMD-CARRIZO_FP4-BGA968

DIMM1, DIMM2, Mini CARD

BB2 BB5 BC2 BB4 AY5 — TC61 TC44 TC71 TC45 TC59

BC3 BA3 BC5 BA5 BB6 — TC62 TC63 TC64 TC65 TC72

RPC2 10K_0404_4P2R_5%

AGPIO3 11

AGPIO5 — LDT_RST_L TC67; LDT_PWROK C68

BOARD_ID0

VDDGFX_PD 36

AGPIO64 — RC278 0_0402_5% — VR_GFX_PWRGD 36,51

ECBTN 36

APU_SHUTDOWN# 16

PCH_BEEP 35

HVB_EN 11; VR_VGA_PWRGD 15,49

PXS_PWREN 19,48,49

RPC9 2.2K_0404_4P2R_5%

APU_SMB_CLK; APU_SMB_DATA

RPC6 10K_0804_8P4R_5%

KBRST#; WLAN_CLKREQ#; PCH_BT_OFF#; PCH_WLAN_OFF#

LAN_CLKREQ# RC67; GATEA20 RC78; GPU_CLKREQ# RC64; APU_SHUTDOWN# RC96 — 10K_0402_5% / 2K_0402_5%

RPC15 10K_0804_8P4R_5%

PBTN_OUT#; AC_PRESENT; PCIE_WAKE#_RA; AGPIO5

RPC16 10K_0404_4P2R_5%

USB_OC1#; USB_OC2#

AGPIO12 RC141; PM_SLP_S3# RC203; PM_SLP_S5# RC208 — 2.2K_0402_5%

BLINK RC158; VDDGFX_PD RC247 — 10K_0402_5%

BLINK isn't strap pin, don't need pull high

AGPIO40 RC93; AGPIO69 RC248 — 10K_0402_5%

VDDGFX_PD RC250 — 10K_0402_5%

GPU_CLKREQ# RC65 — PX@ 2K_0402_5%

HDA_BITCLK RC90; HDA_SDIN0_R RC91; APU_SHUTDOWN# RC256 — BR@ 1K_0402_5% / 10K_0402_5% / 2K_0402_5%

RSMRST#_R RC87; SYS_PWRGD_R RC89 — 100K_0402_5%

HDA_SDIN2 RC241; HDA_SDIN1 RC242 — 10K_0402_5%

36 PBTN_OUT# — PBTN_OUT# RC191 0_0402_5% — PWRBTN#_R; SYS_PWRGD_R; SYS_RESET#_R; PCIE_WAKE#_RA

11 SYS_RESET#

36 PM_SLP_S3# — PM_SLP_S3# RC193 0_0402_5%

36 PM_SLP_S5# — PM_SLP_S5# RC194 0_0402_5%

9 APU_S5_MUX_CTRL

36 KBRST#; 36 GATEA20; 36 EC_SCI#

36 AC_PRESENT

31 PCH_WLAN_OFF#; 31 WLAN_CLKREQ#; 28 LAN_CLKREQ#; 31 PCH_BT_OFF#; 16 GPU_CLKREQ#

32 USB_OC1#; 37 USB_OC2#

35 HDA_SDIN0 — RC201 0_0402_5%

RPC3 10K_0804_8P4R_5% — I2C1SDA; I2C1SCL; I2C0SCL; I2C0SDA

I2C0SCL; I2C0SDA; I2C1SCL; I2C1SDA

11,31 SUSCLK

RC102 20M_0402_5% — YC1 32.768KHZ_12.5PF_2027 40-PG14

CC23 20P_0402_50V8; CC210 20P_0402_50V8

change YC1 PN to ESPON S CRYSTAL 32.768KHZ X1A000141000300, footprint no change

RPC4 33_0804_8P4R_5%

35 HDA_RST_AUDIO#; 35 HDA_SYNC_AUDIO; 35 HDA_BITCLK_AUDIO; 35 HDA_SDOUT_AUDIO — HDA_RST#; HDA_SYNC; HDA_BITCLK; HDA_SDOUT

RC260 BR@ 1K_0402_5%; RC261 BR@ 1K_0402_5%; RC262 BR@ 1K_0402_5%

PXS_PWREN_R/PXS_RST#_R/VR_VGA_PWRGD internal pull up 40k

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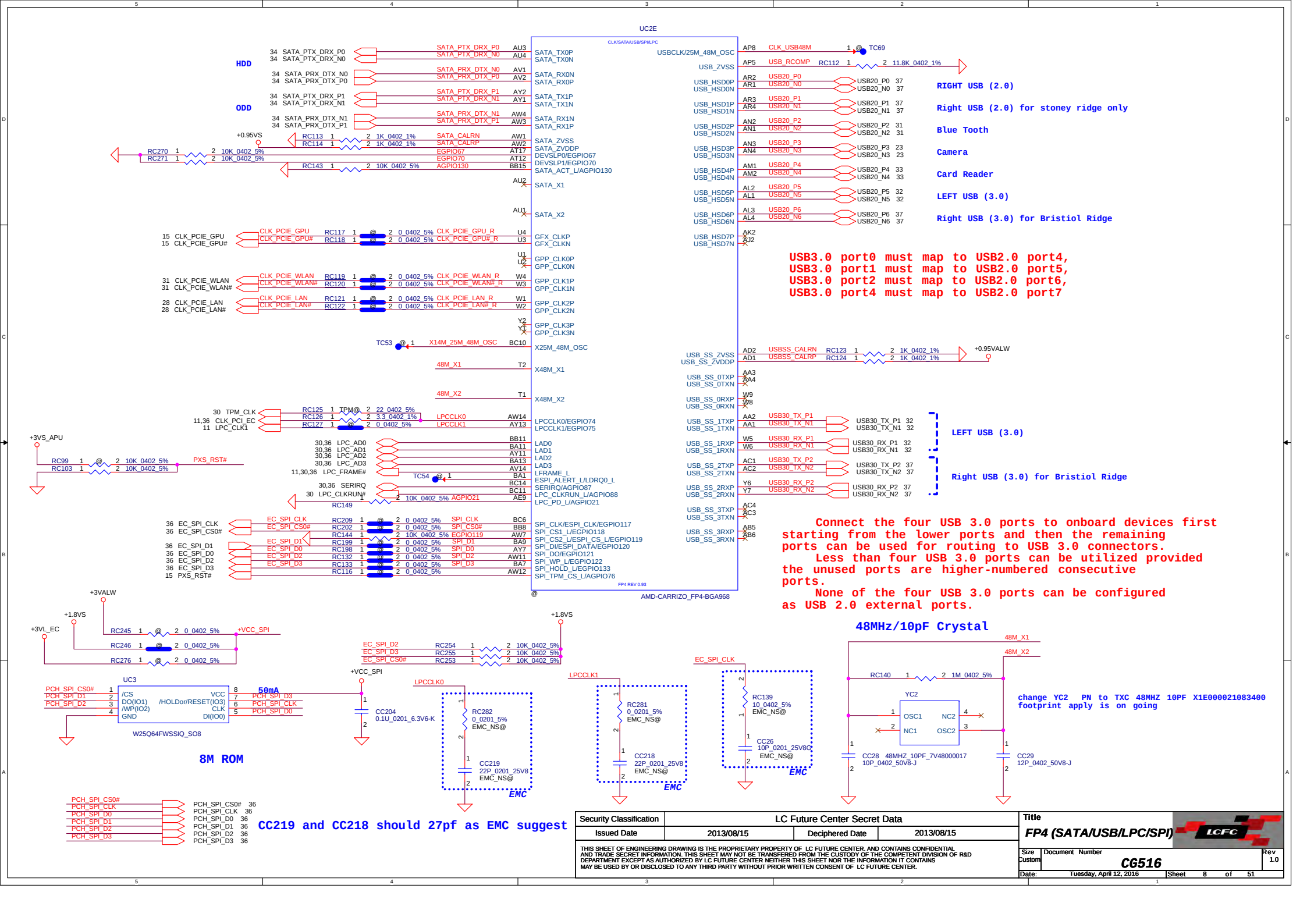
UC2E
AMD-CARRIZO_FP4-BGA968
HDD
ODD
RIGHT USB (2.0)
Right USB (2.0) for stoney ridge only
Blue Tooth
Camera
Card Reader
LEFT USB (3.0)
Right USB (3.0) for Bristiol Ridge
USB3.0 port0 must map to USB2.0 port4,
USB3.0 port1 must map to USB2.0 port5,
USB3.0 port2 must map to USB2.0 port6,
USB3.0 port4 must map to USB2.0 port7
Connect the four USB 3.0 ports to onboard devices first starting from the lower ports and then the remaining ports can be used for routing to USB 3.0 connectors.
Less than four USB 3.0 ports can be utilized provided the unused ports are higher-numbered consecutive ports.
None of the four USB 3.0 ports can be configured as USB 2.0 external ports.
48MHz/10pF Crystal
change YC2 PN to TXC 48MHZ 10PF X1E000021083400 footprint apply is on going
8M ROM
50mA
W25Q64FWSSIQ_SO8
CC219 and CC218 should 27pf as EMC suggest
EMC
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Wake-on-Ring not supported:
+VDDIO_AZ_APU Connect to +1.5V S0 rail

RC210,CC180,CC181 must add BRUMA@ in Virtual symbol

DECOUPLING BETWEEN PROCESSOR AND DIMMs ACROSS VDDIO AND VSS SPLIT

	Design Guide	G FP4	CRB
VDDCR_CPU	9*22uF 0603 8*0.22uF 0402 1*180pF 0402	9*22uF 0805 8*0.22uF 0402 1*180pF 0402	13*22uF 0603 8*0.22uF 0402 1*180pF 0402
VDDCR_NB	4*22uF 0603 8*0.22uF 0402 1*180pF 0402	4*22uF 0805 8*0.22uF 0402 1*180pF 0402	6*22uF 0603 8*0.22uF 0402 split *5 1*180pF 0402
VDDCR_GFX	8*22uF 0603 9*0.22uF 0402 1*180pF 0402	10*22uF 0805 9*0.22uF 0402 1*180pF 0402	13*22uF 0603 9*0.22uF 0402 1*180pF 0402
VDDIO_MEM_S3	8*22uF 0603 6*0.22uF 0402 split*4 1*180pF 0402 split*2	8*22uF 0603 6*0.22uF 0402 split*4 1*180pF 0402 split*2	8*22uF 0603 8*0.22uF 0402 split*4 1*180pF 0402 split*2
VDDCR_FCH_S5	2*10uF 0402 1*0.22uF 0402	2*10uF 0603 1*0.22uF 0402	2*10uF 0603 1*0.22uF 0402
VDDP	4*10uF 0402 1*0.22uF 0402 1*180pF 0402	4*10uF 0603 1*0.22uF 0402 1*180pF 0402	4*10uF 0603 1*0.22uF 0402 1*180pF 0402
VDDP_GFX	1*10uF 0402 1*0.22uF 0402	1*10uF 0603 1*0.22uF 0402	1*10uF 0603 1*0.22uF 0402
VDDP_S5	1*10uF 0402 1*0.22uF 0402	1*10uF 0603 1*0.22uF 0402	1*10uF 0603 1*0.22uF 0402
VDD_18	1*22uF 0603 1*10uF 0402	1*22uF 0603 1*10uF 0402	1*22uF 0603 1*10uF 0603
VDD_18_S5	1*10uF 0402 1*0.22uF 0402	1*10uF 0603 1*0.22uF 0402	1*10uF 0603 1*0.22uF 0402
VDD_33	1*10uF 0402	1*10uF 0603	1*10uF 0603
VDD_33_S5	1*10uF 0402 1*0.22uF 0402	1*10uF 0403 1*0.22uF 0402	1*10uF 0603 1*0.22uF 0402
VDDIO_AUDIO	3*1uF 0402	3*1uF 0402	3*1uF 0402
VDDBT_RTC_G	1*0.22uF 0402	1*0.22uF 0402	1*0.22uF 0402

QC1/QC2/QC3/QC4 Rds on should less possible, CRB is 11.8mohm, there is no load swtich for 0.775V power, so it need mos

Decoupling cap near APU ball

S5_MUX_CTRL: Enable MUX(S0 to S3)-->LOW
Disable MUX(S3 to S0)-->HIGH

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: FP4 (POWER&DECOUPLING)

Size	Document Number	Rev
Custom	CG516	1.0

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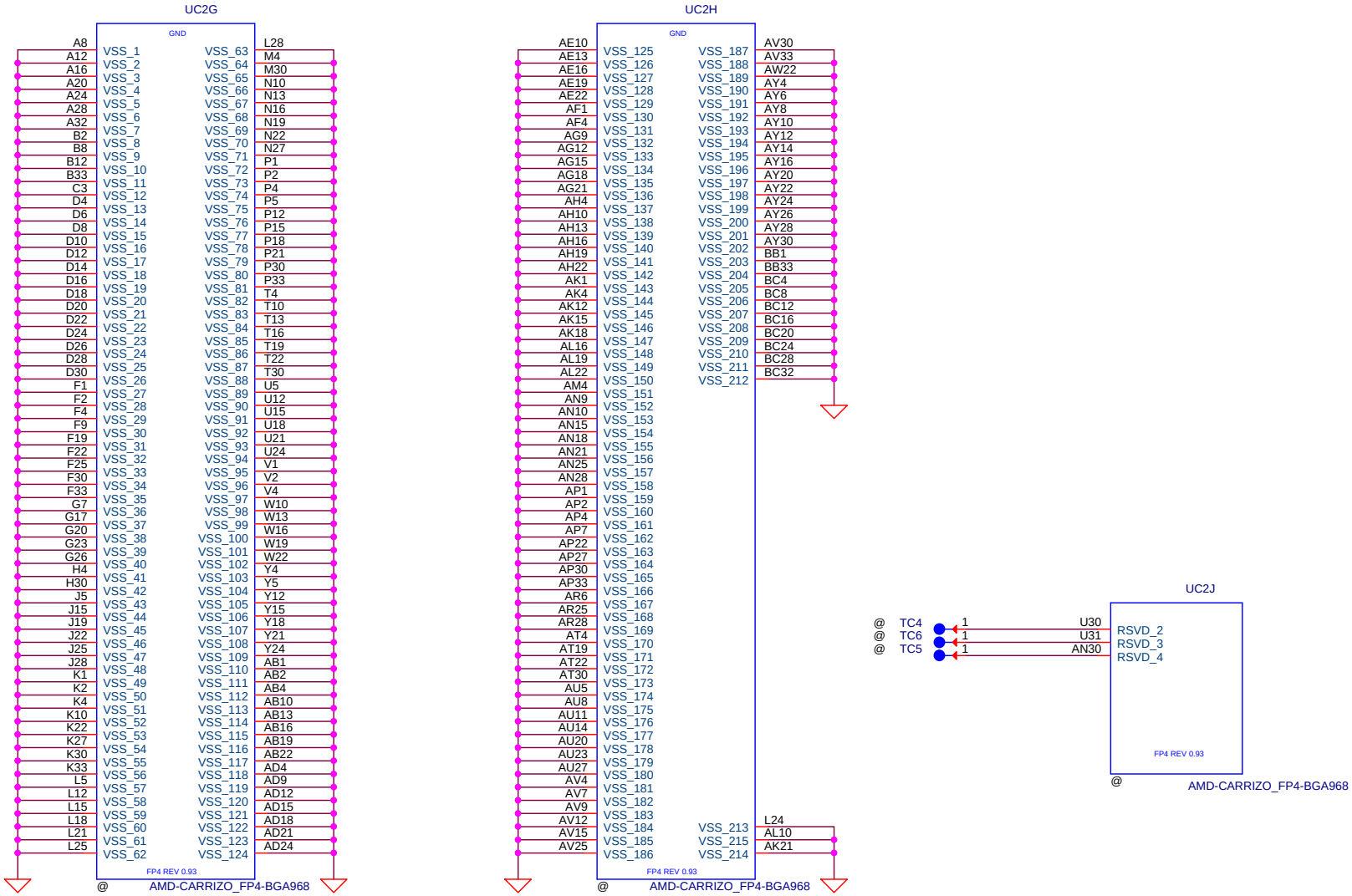

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title

FP4 (VSS)

Size: Custom	Document Number: CG516	Rev: 1.0
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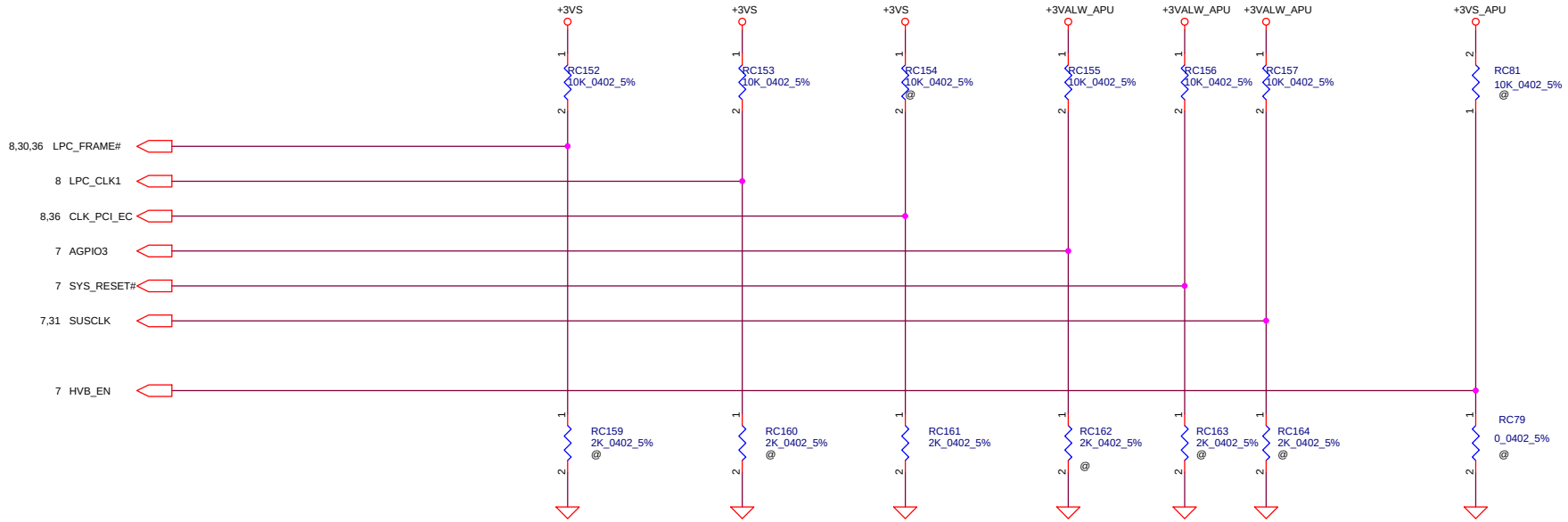

STRAP PINS

Signal	LFRAME_L	LPCCLK1	LPCCLK0	RTCCLK Int pull-up	SYS_RESET_L Int pull-up	AGPIO3 Int pull-up	HVB_EN
Type	II	II	II	I	I	I	
PULL HIGH	SPI ROM Default	Internal CLK Gen Default	Boot Fail Timer Enabled	RTC Coin Battery is implemented Default	Normal Power Up &Reset Timing Default	Enhanced reset logic (for quicker S5 resume) Default	floating Disable HVB on FP4 platforms Default
PULL LOW	LPC ROM	Reserved	Boot Fail Timer Disabled Default	RTC Coin Battery is not implemented	Reserved	traditional reset logic	connected to VSS Enable HVB on FP4 platforms

Type I straps become valid immediately after capture with the rising edge of RSMRST_L,they are captured only once when power is first applied to the processor

Type II straps become valid after PWR_GOOD is asserted,straps are captured every time the systems powers up from the S5 state. A transition from S3 to S0 does not trigger capture.
Type II straps should be pulled up to S0 power rail to prevent leakage when the signal is connected to a device in S0 power domain.

If the LPC bus is connected to devices that are on S0 power rail, then a pull-up resistor to VDD_33 is implemented.

All Strap pins must be configured with either external pull-up or pull-down resistors.

Platforms that are designed for AOAC complaint are recommended to use the Alternate Reset by strapping this pin to ‘ 1’ for ⧉ AGPIO3

Title		
FP4 (STRAPS)		
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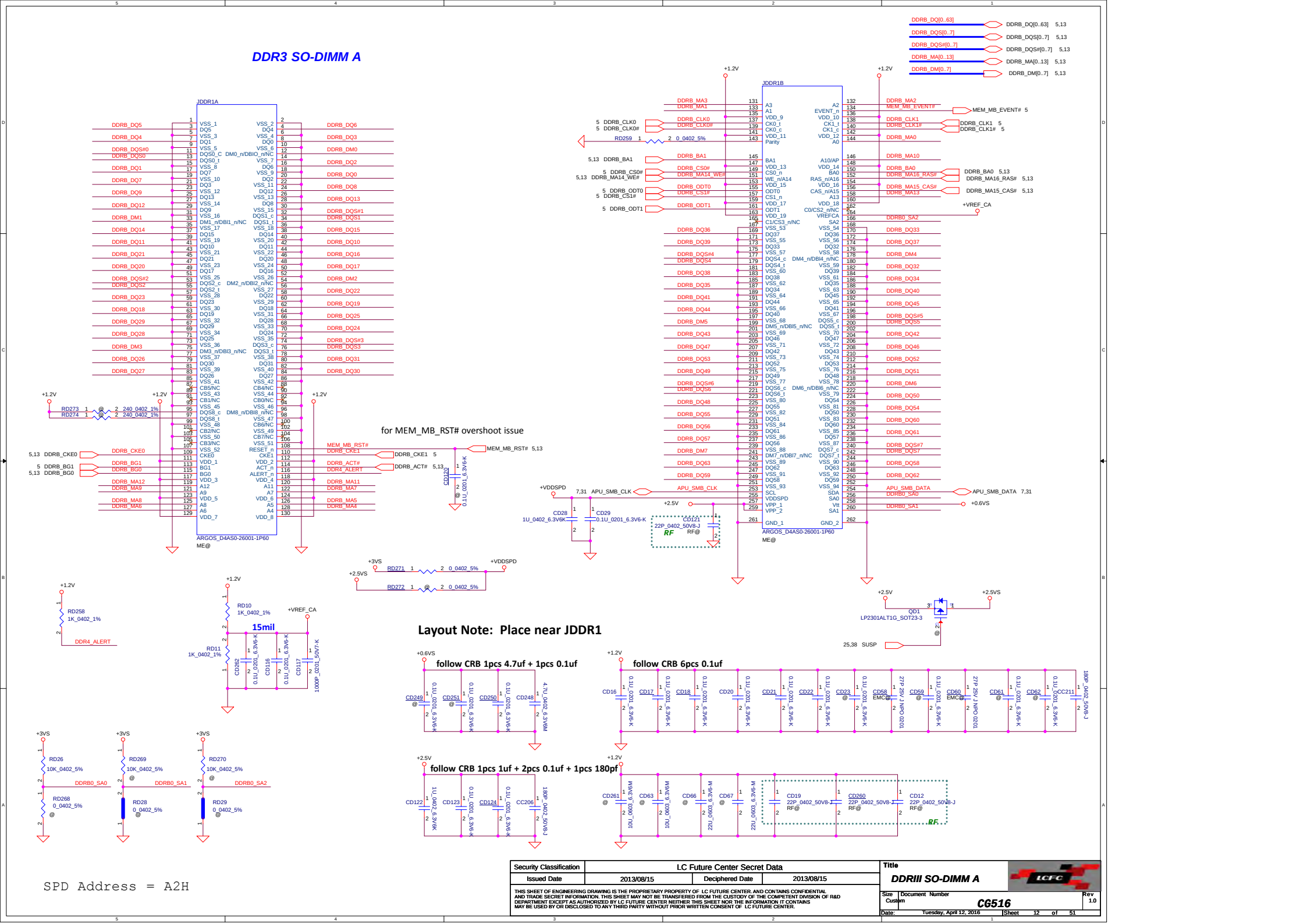
DDR3 SO-DIMM A



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: DDRIII SO-DIMM A

Size: Custom | Document Number: CG516 | Rev: 1.0

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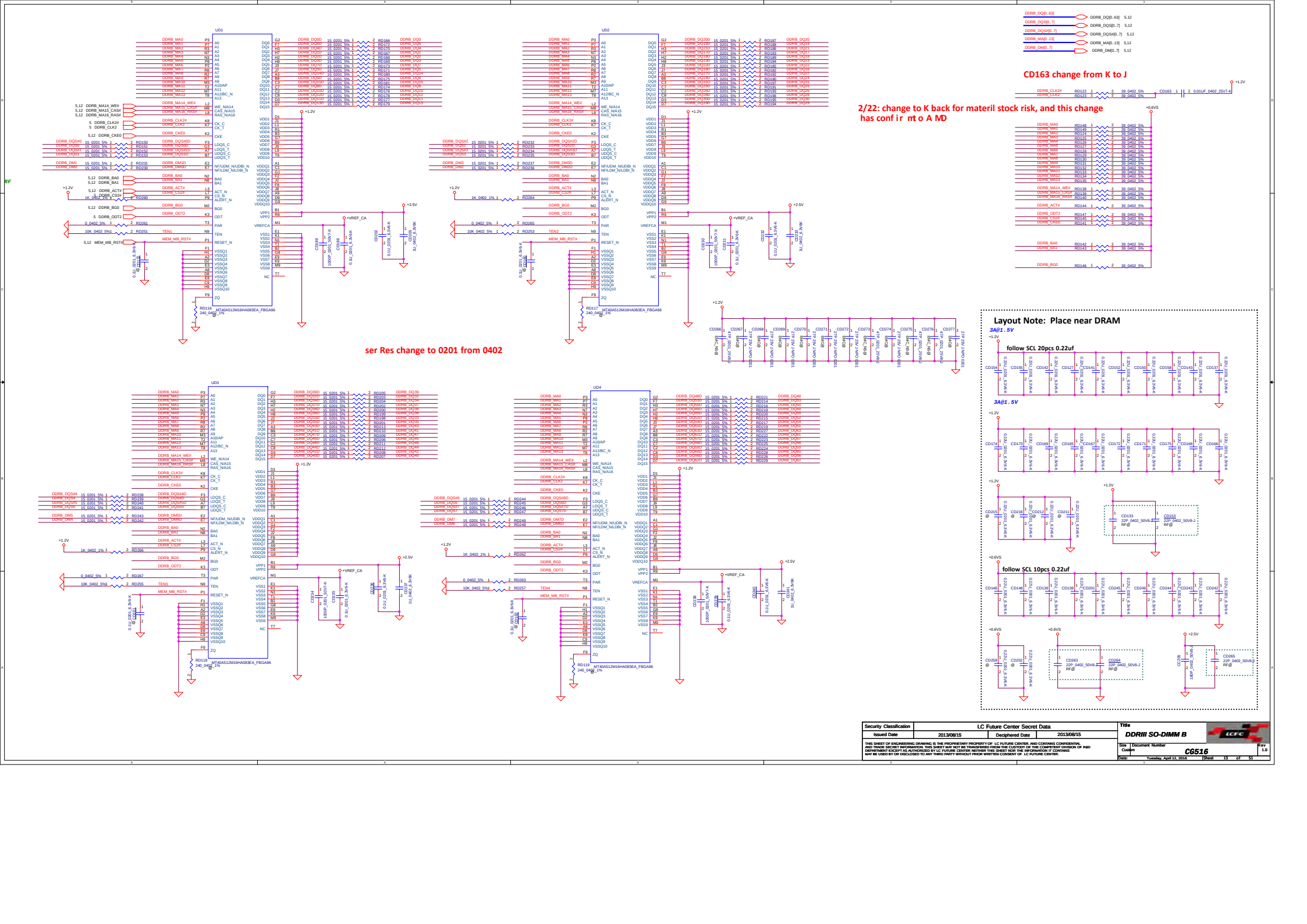
CD163 change from K to J
2/22: change to K back for materil stock risk, and this change has conf i r mt o A MD
ser Res change to 0201 from 0402
Layout Note: Place near DRAM
3A@1.5V
follow SCL 20pcs 0.22uf
3A@1.5V
follow SCL 10pcs 0.22uf
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/15
Deciphered Date
2013/08/15
Title
DDRII SO-DIMM B
Size
Custom
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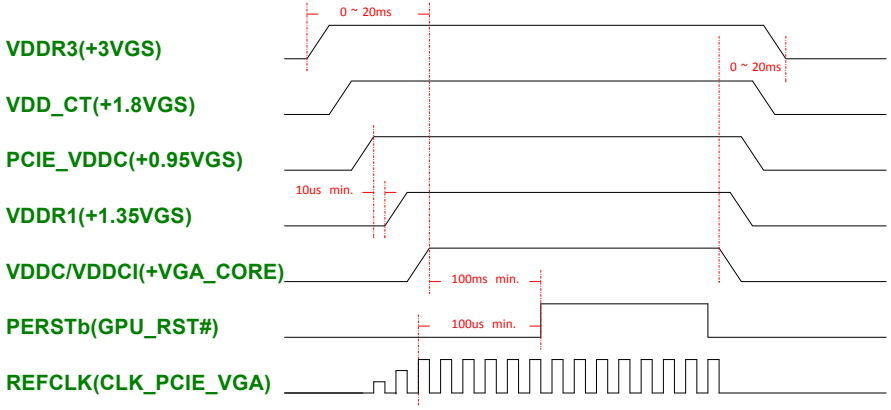
Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µ s.
It is recommended that the 3.3-V rail ramp up first.
The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 µ s before VDDC, VDDCI, and VMEMIO start to ramp up.
The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/µ s).
For power down, reversing the ramp-up sequence is recommended.



VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

Title: VGA Notes List

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4 PCIE_CTX_C_GRX_P[7..0] → PCIE_CTX_C_GRX_P[7..0]
4 PCIE_CTX_C_GRX_N[7..0] → PCIE_CTX_C_GRX_N[7..0]

PCIE_CRX_GTX_P[7..0] → PCIE_CRX_GTX_P[7..0] 4
PCIE_CRX_GTX_N[7..0] → PCIE_CRX_GTX_N[7..0] 4

UV1A

PCIE_CTX_C_GRX_P0	AF30	PCIE_RX0P	PCIE_TX0P	AH30	PCIE_CRX_C_GTX_P0	0.22U_0201_6.3V6-K	1	2 PX@	CV1	PCIE_CRX_GTX_P0
PCIE_CTX_C_GRX_N0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	PCIE_CRX_C_GTX_N0	0.22U_0201_6.3V6-K	1	2 PX@	CV2	PCIE_CRX_GTX_N0
PCIE_CTX_C_GRX_P1	AE29	PCIE_RX1P	PCIE_TX1P	AG29	PCIE_CRX_C_GTX_P1	0.22U_0201_6.3V6-K	1	2 PX@	CV3	PCIE_CRX_GTX_P1
PCIE_CTX_C_GRX_N1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	PCIE_CRX_C_GTX_N1	0.22U_0201_6.3V6-K	1	2 PX@	CV4	PCIE_CRX_GTX_N1
PCIE_CTX_C_GRX_P2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	PCIE_CRX_C_GTX_P2	0.22U_0201_6.3V6-K	1	2 PX@	CV5	PCIE_CRX_GTX_P2
PCIE_CTX_C_GRX_N2	AC31	PCIE_RX2N	PCIE_TX2N	AF26	PCIE_CRX_C_GTX_N2	0.22U_0201_6.3V6-K	1	2 PX@	CV6	PCIE_CRX_GTX_N2
PCIE_CTX_C_GRX_P3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	PCIE_CRX_C_GTX_P3	0.22U_0201_6.3V6-K	1	2 PX@	CV7	PCIE_CRX_GTX_P3
PCIE_CTX_C_GRX_N3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	PCIE_CRX_C_GTX_N3	0.22U_0201_6.3V6-K	1	2 PX@	CV8	PCIE_CRX_GTX_N3
PCIE_CTX_C_GRX_P4	AB30	PCIE_RX4P	PCIE_TX4P	AC25	PCIE_CRX_C_GTX_P4	0.22U_0201_6.3V6-K	1	2 BRPX@	CV17	PCIE_CRX_GTX_P4
PCIE_CTX_C_GRX_N4	AA31	PCIE_RX4N	PCIE_TX4N	AB25	PCIE_CRX_C_GTX_N4	0.22U_0201_6.3V6-K	1	2 BRPX@	CV9	PCIE_CRX_GTX_N4
PCIE_CTX_C_GRX_P5	AA29	PCIE_RX5P	PCIE_TX5P	Y23	PCIE_CRX_C_GTX_P5	0.22U_0201_6.3V6-K	1	2 BRPX@	CV13	PCIE_CRX_GTX_P5
PCIE_CTX_C_GRX_N5	Y28	PCIE_RX5N	PCIE_TX5N	Y24	PCIE_CRX_C_GTX_N5	0.22U_0201_6.3V6-K	1	2 BRPX@	CV11	PCIE_CRX_GTX_N5
PCIE_CTX_C_GRX_P6	Y30	PCIE_RX6P	PCIE_TX6P	AB27	PCIE_CRX_C_GTX_P6	0.22U_0201_6.3V6-K	1	2 BRPX@	CV14	PCIE_CRX_GTX_P6
PCIE_CTX_C_GRX_N6	W31	PCIE_RX6N	PCIE_TX6N	AB26	PCIE_CRX_C_GTX_N6	0.22U_0201_6.3V6-K	1	2 BRPX@	CV12	PCIE_CRX_GTX_N6
PCIE_CTX_C_GRX_P7	W29	PCIE_RX7P	PCIE_TX7P	Y27	PCIE_CRX_C_GTX_P7	0.22U_0201_6.3V6-K	1	2 BRPX@	CV10	PCIE_CRX_GTX_P7
PCIE_CTX_C_GRX_N7	V28	PCIE_RX7N	PCIE_TX7N	Y26	PCIE_CRX_C_GTX_N7	0.22U_0201_6.3V6-K	1	2 BRPX@	CV20	PCIE_CRX_GTX_N7

V30	NC#V30	NC#W24	W24
U31	NC#U31	NC#W23	W23
U29	NC#U29	NC#V27	V27
T28	NC#T28	NC#U26	U26
T30	NC#T30	NC#U24	U24
R31	NC#R31	NC#U23	U23
R29	NC#R29	NC#T26	T26
P28	NC#P28	NC#T27	T27
P30	NC#P30	NC#T24	T24
N31	NC#N31	NC#T23	T23
N29	NC#N29	NC#P27	P27
M28	NC#M28	NC#P26	P26
M30	NC#M30	NC#P24	P24
L31	NC#L31	NC#P23	P23
L29	NC#L29	NC#M27	M27
K30	NC#K30	NC#N26	N26

PCI EXPRESS INTERFACE

CLOCK

8 CLK_PCIE_GPU → CLK_PCIE_GPU AK30 PCIE_REFCLKP
8 CLK_PCIE_GPU# → CLK_PCIE_GPU# AK32 PCIE_REFCLKN

1K_0402_1% 1 PX@ 2 RV4 → N10 TEST_PG

16 GPU_RST# → GPU_RST# AL27 PERSTB

CALIBRATION

+0.95VGS
Y22 PCIE_CALR_TX — RV3 1 PX@ 2 1.69K_0402_1%
AA22 PCIE_CALR_RX — RV5 1 PX@ 2 1K_0402_1%

S IC 216-0867-071 A0 FCBGA 631P GPU 12
EXO@

RV7 1 @ 2 0_0402_5%
+3VGS
RV6 100K_0402_5% PX@

UV2
8 PXS_RST# → 1 IN1
7,28,31 PLT_RST# → 2 IN2
5 VCC
3 GND
4 OUT → GPU_RST#
MC74VHC1G08DFT2G_SC70-5
PX@

DV3 PX@
GPU_RST# → 2
7,49 VR_VGA_PWRGD → 3
1 → VGA_PWROK → VGA_PWROK 49
LBAT54AWT1G SOT323

with BOM strcture control, CV1--CV8 change to 0.22uf for CZ

change the GPU PN to AMD(EXO-S3 PRO), symbol check ok

11/4 change to PC sample SA000074V10

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Title: ATI_JET-LE_PCIE

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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 001 = 256MB	x
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 1= Not support	x
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	x
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	x
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system' s VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 100 = Hynix 1G 000 = Hynix 2G 111 = Micron 1G 010 = Micron 2G 110 = Samsung 1G 001 = Samsung 2G	x
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 111= No usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	11

MLPS	Bit					BOM		
	5	4	3	2	1	R_pu ( )	R_pd ( )	C(nF)
PS_0[5:1]	1	1	0	0	1	RV71=8.45K	RV77=2K	CV15=NC
PS_1[5:1]	1	1	0	0	1	RV74=NC	RV77=4.75K	CV16=NC
PS_2[5:1]	1	1	0	0	0	RV60=NC	RV69=4.75K	CV18=NC
PS_3[5:1]	1	1	X	X	X	RV63=X76	RV70=X76	CV19=X76

with BOM strcture control,
RV63,RV70 change to different value to adjust VRAM config

with BOM strcture control,
when config PE63
RV74 change to 8.45K,
RV80 change to 2K

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Reserve for Topaz

Pull down for none OBFF design

no symbol for 8pf cap, PLM has PN,change the PN

(1.8V@20mA TSVDD)

Connect GPIO_28 to 10K pull down to enable MLPS.

For Topaz, RV16/RV19 stuff 100ohm
for EXO, RV16/RV19 stuff 0hm.

Internal VGA Thermal Sensor

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Title: ATI_JET-LE_Main_MSIC

Size	Document Number	Rev
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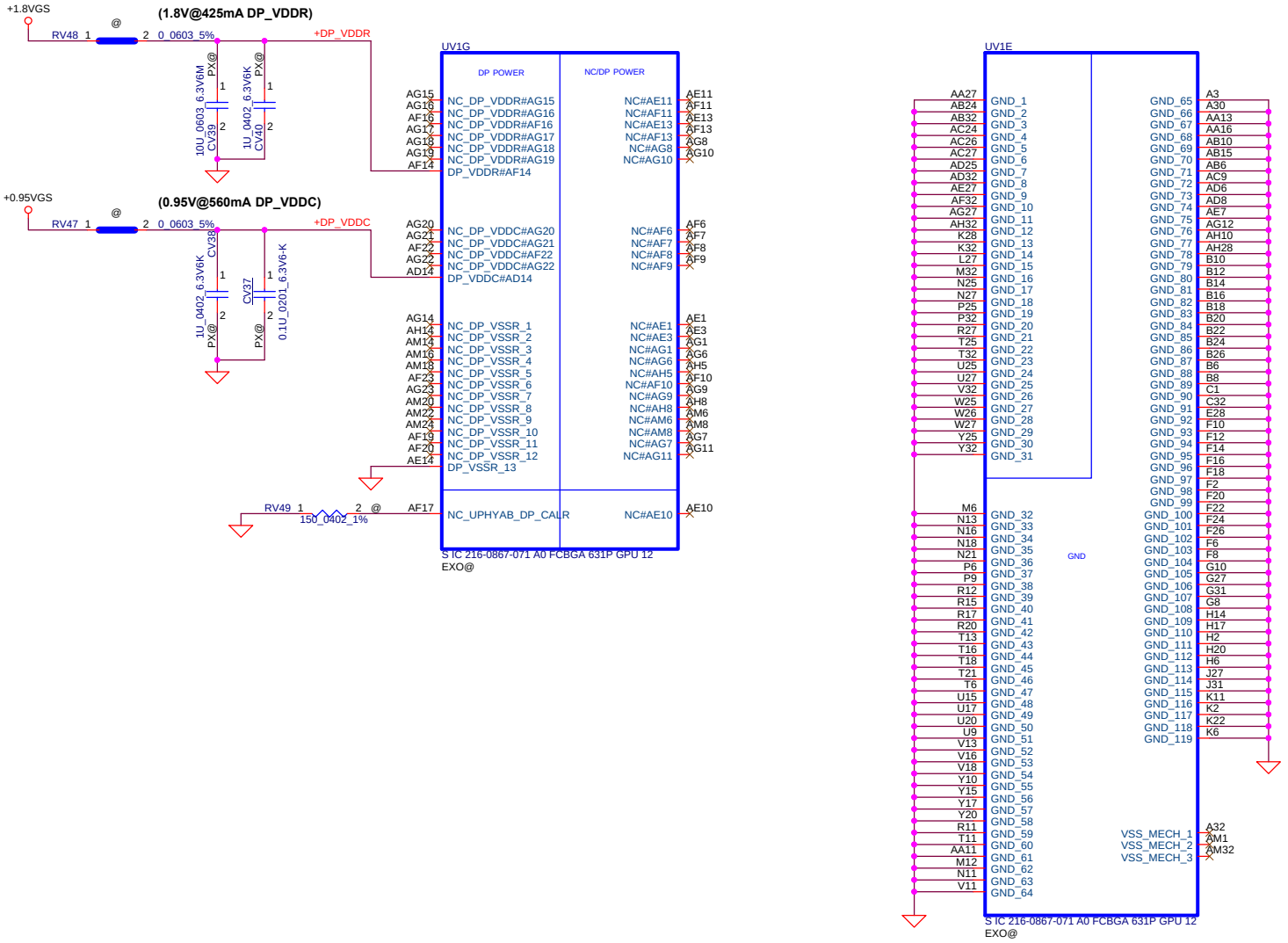
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_TMDP

Size: Custom	Document Number: CG516	Rev: 1.0
Date: Tuesday, April 12, 2016	Sheet 17 of 51	



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: *ATI_JET-LE_DP Power*

Size	Document Number	Rev
Custom	CG516	1.0

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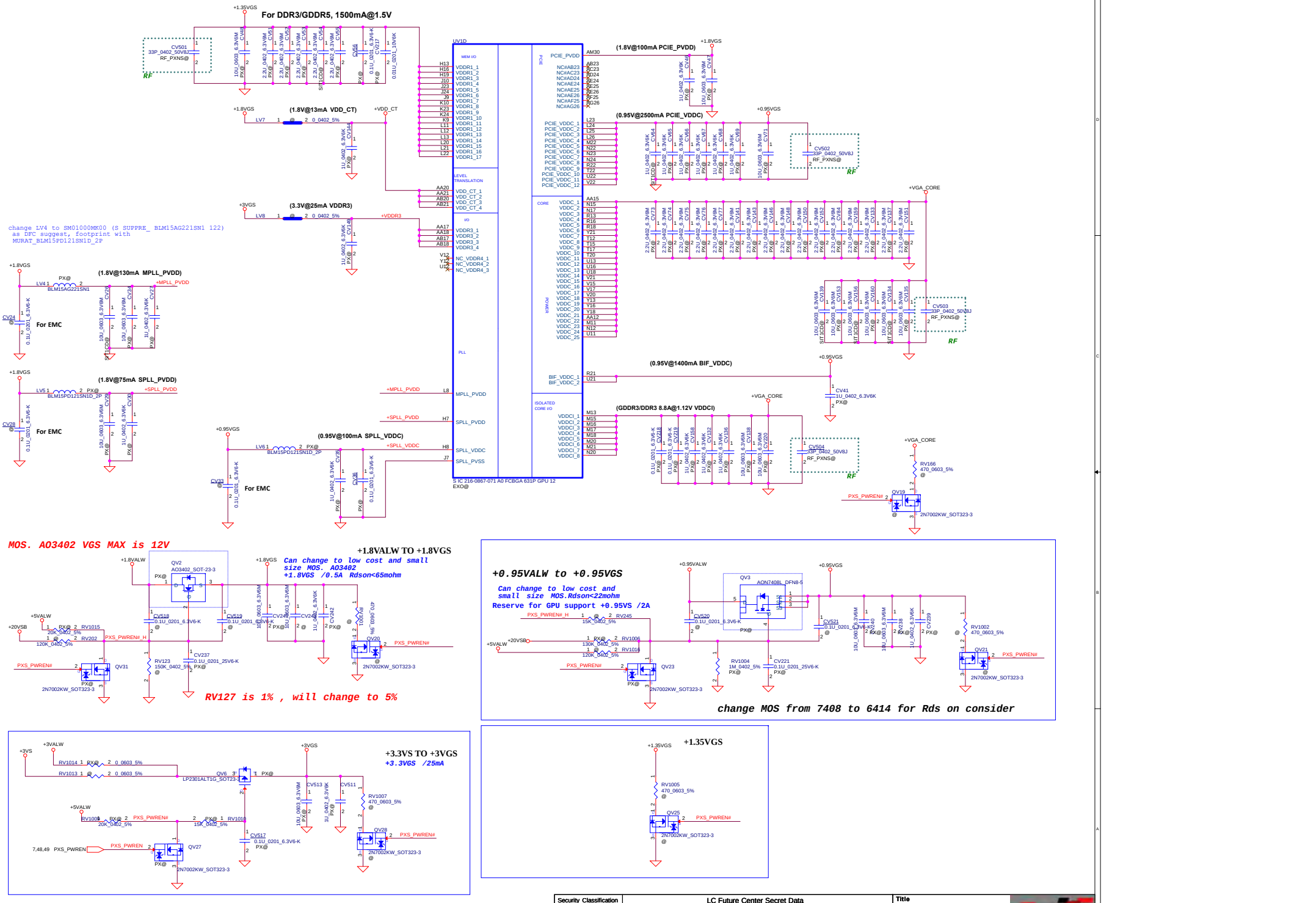

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Size: Custom | Document Number: CG516 | Rev: 1.0

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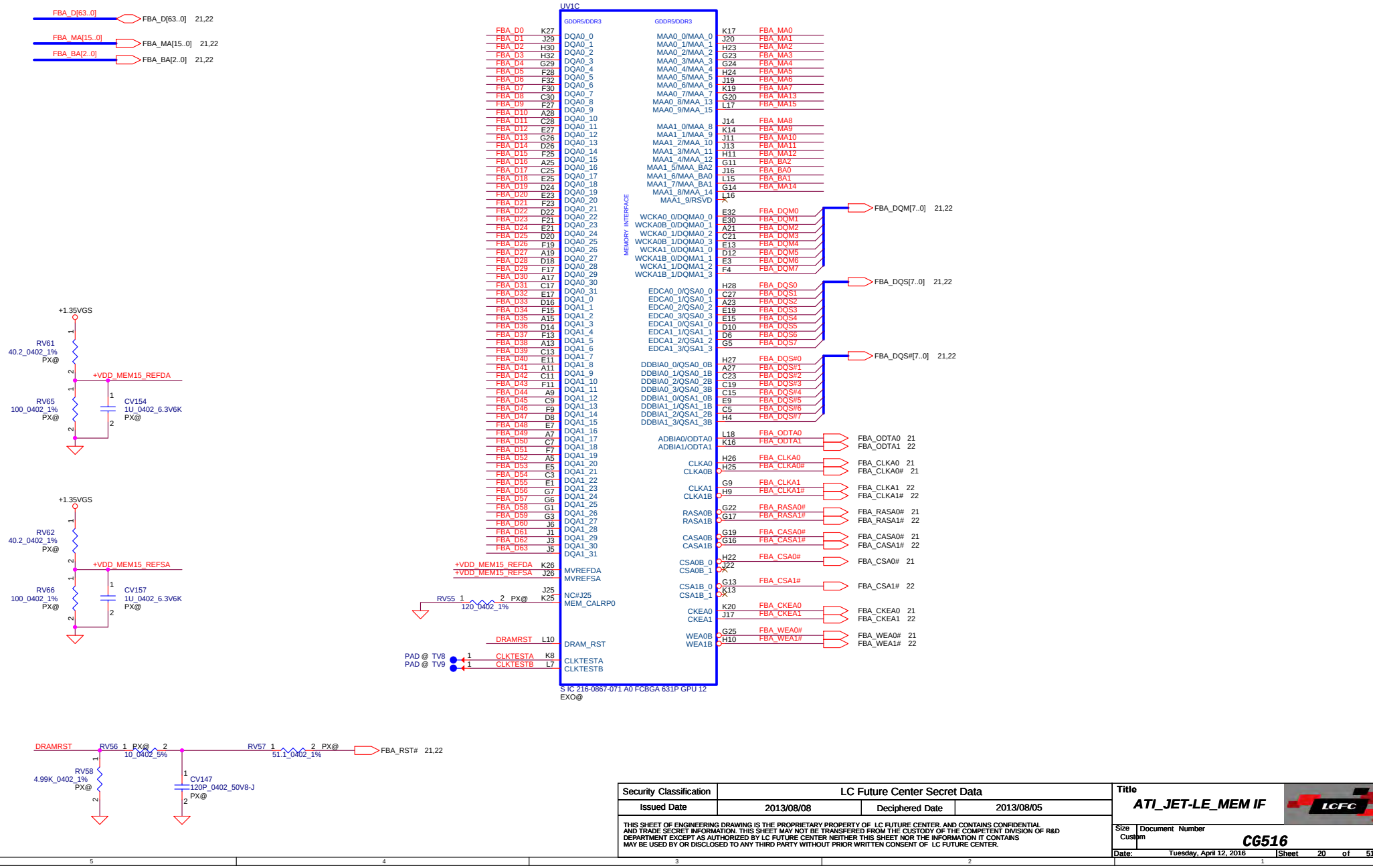

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_MEM IF

Size: Custom | Document Number: CG516 | Rev: 1.0

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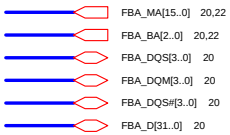
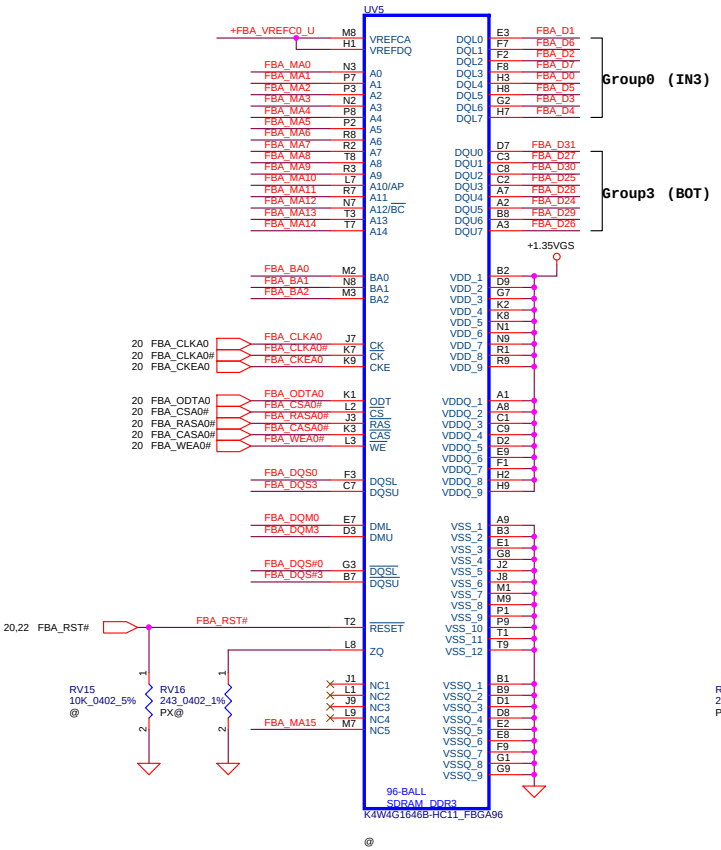
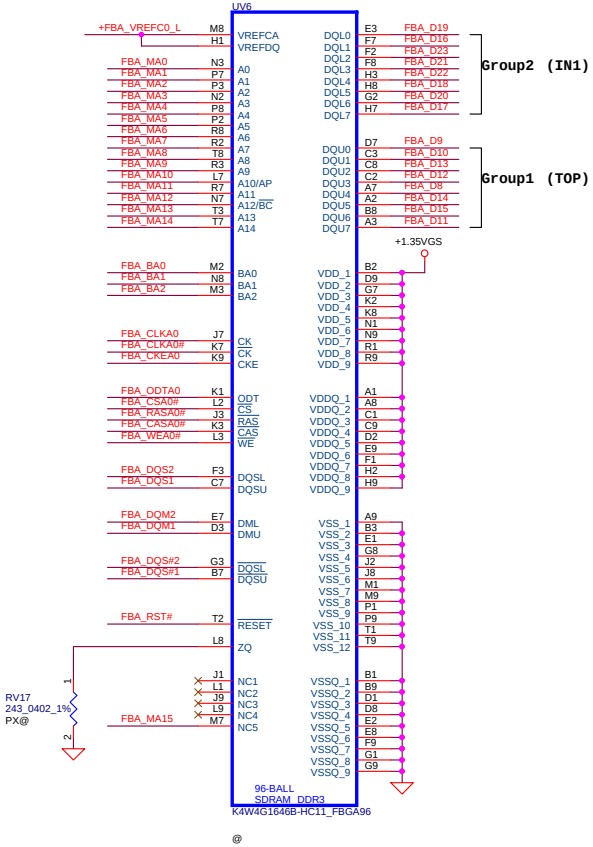
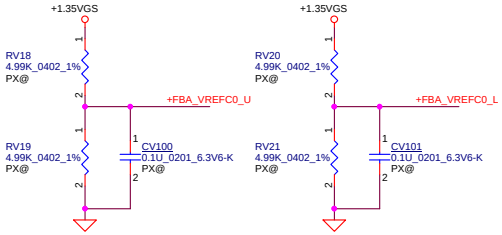
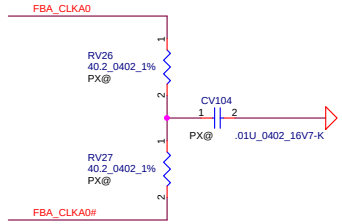
Memory Partition A - Lower 32 bits

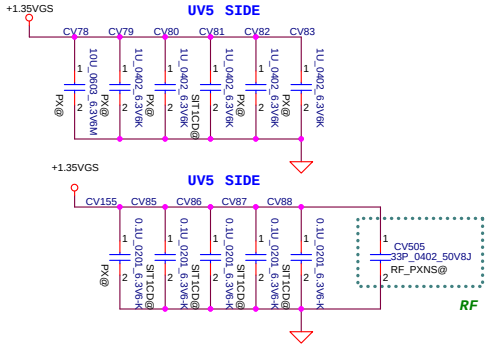


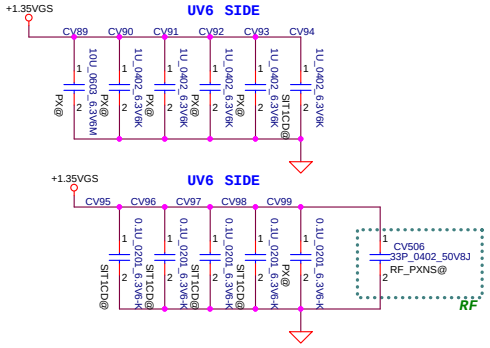












Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_VRAM_A

Size: Custom | Document Number: CG516 | Rev: 1.0

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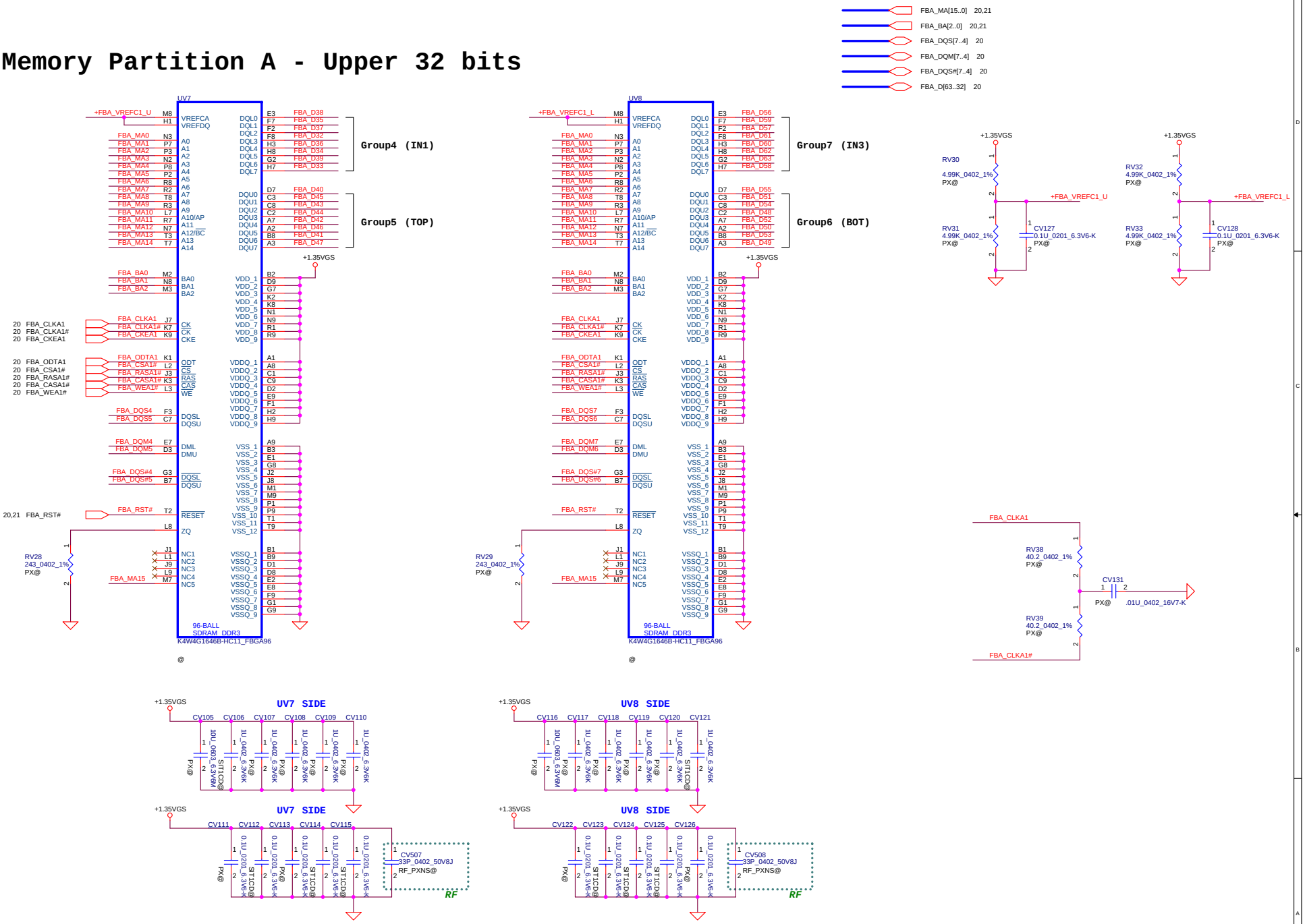
Memory Partition A - Upper 32 bits



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_VRAM_B

Size: Custom | Document Number: CG516 | Rev: 1.0

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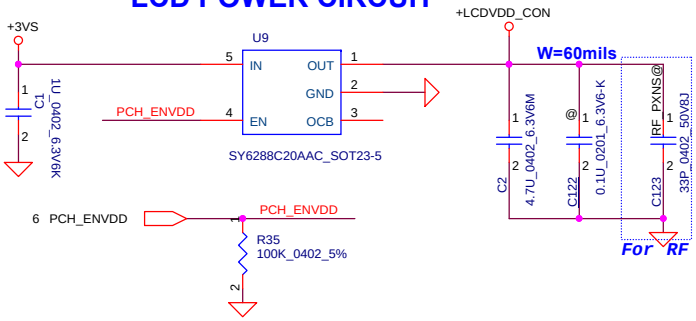
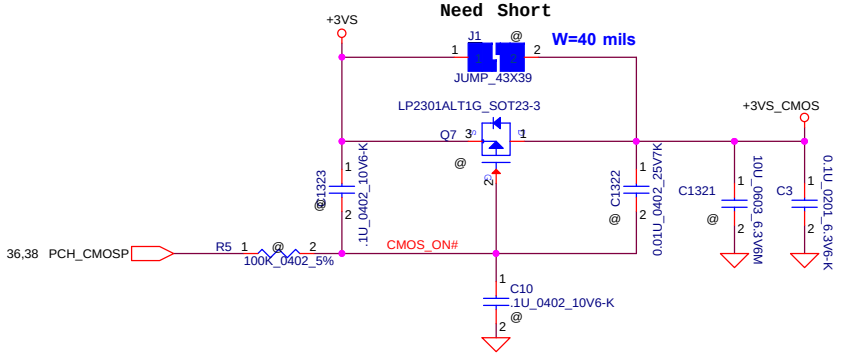
LCD POWER CIRCUIT

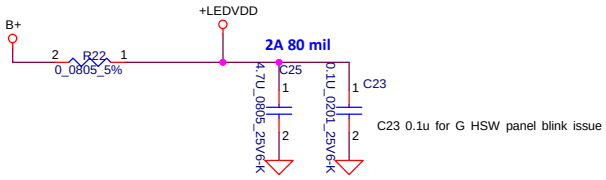


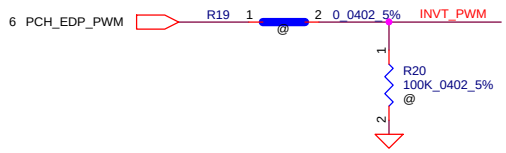
APU output enable Voh min is 1.8V-0.45V=1.35V

Need Short

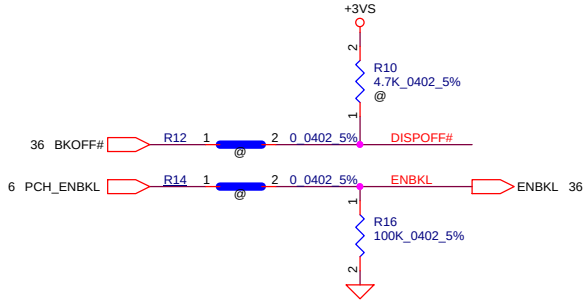


B+ to +LEDVDD POWER

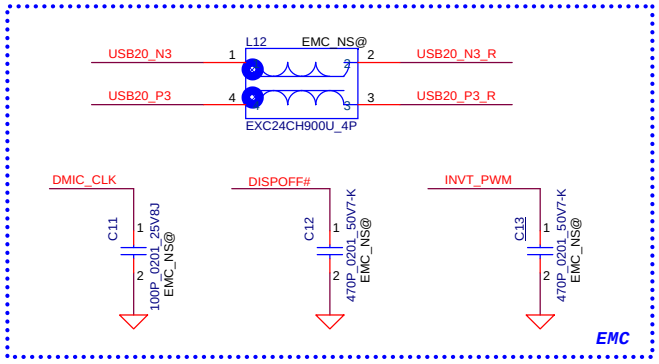


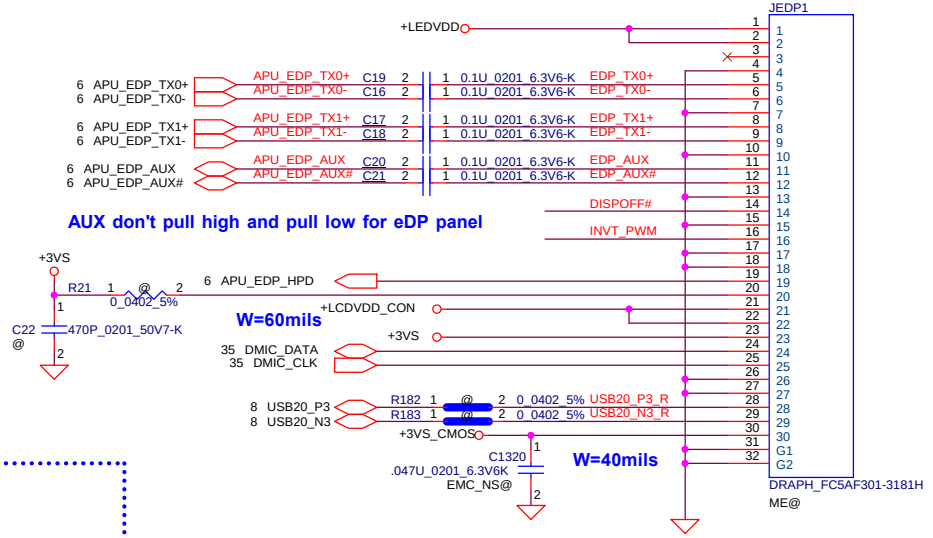


Need Short



CMOS Camera





Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: *eDP/CMOS*

Size	Document Number	Rev
Custom	CG516	1.0

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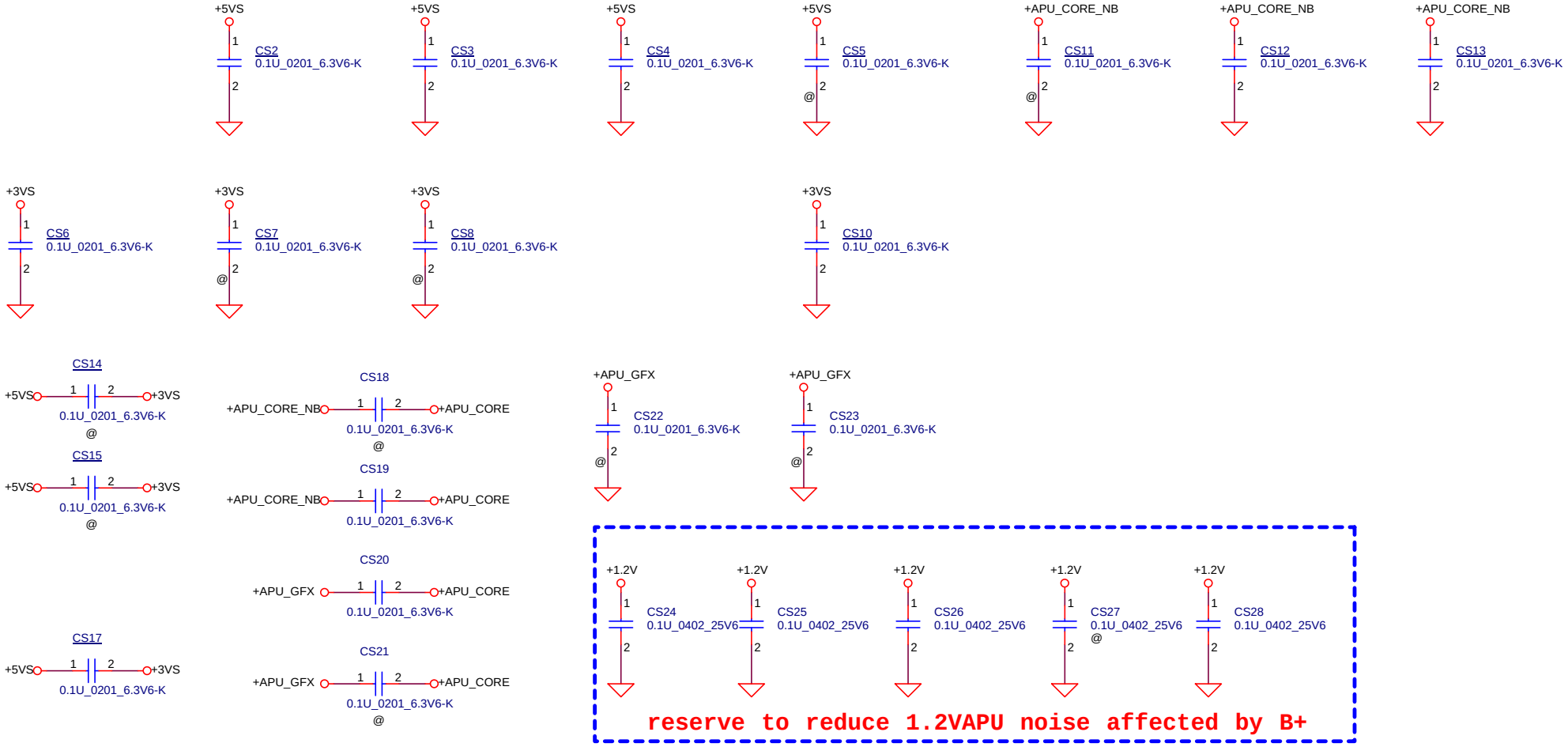

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: StitchingCap

Size	Document Number	Rev
Custom	CG516	1.0

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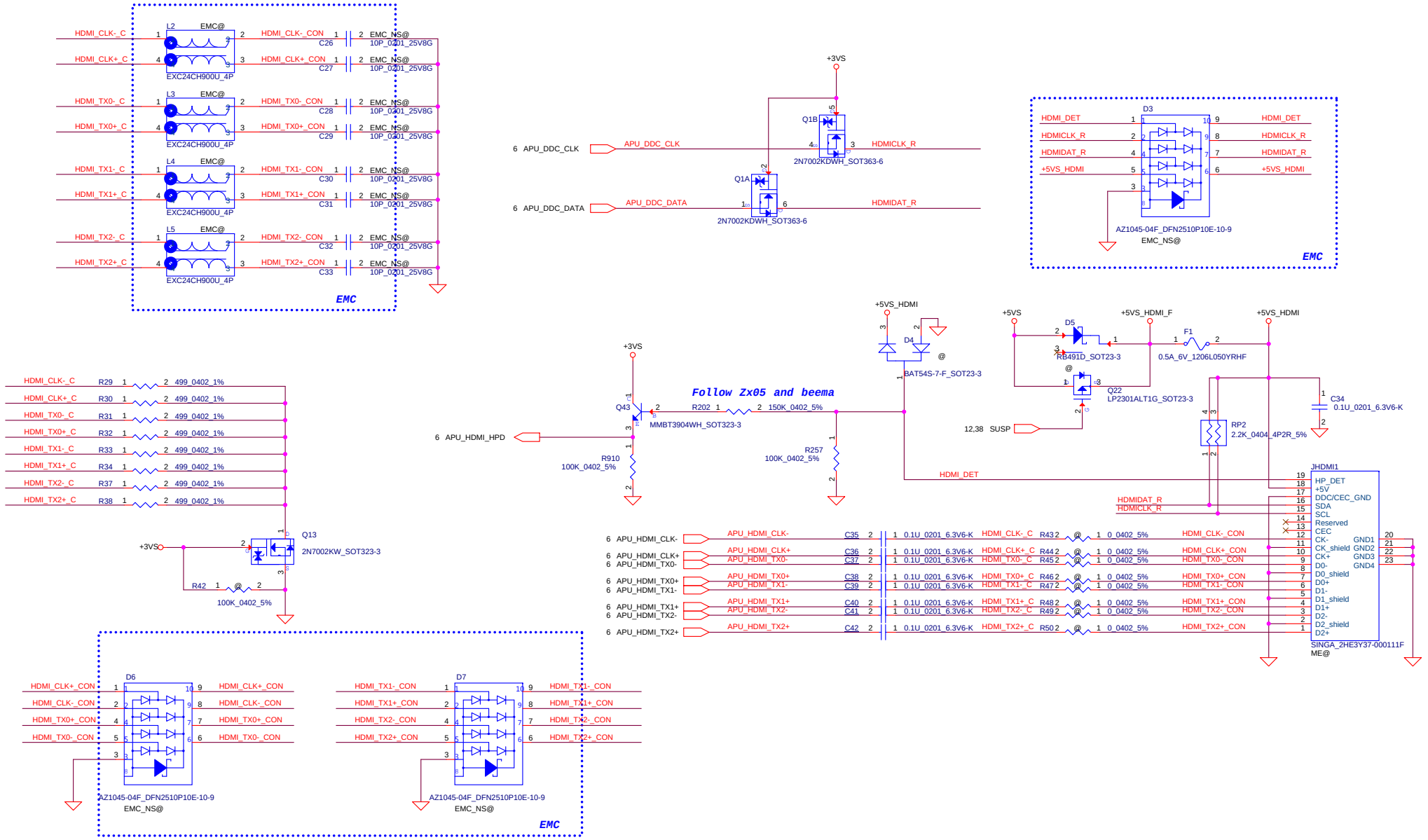
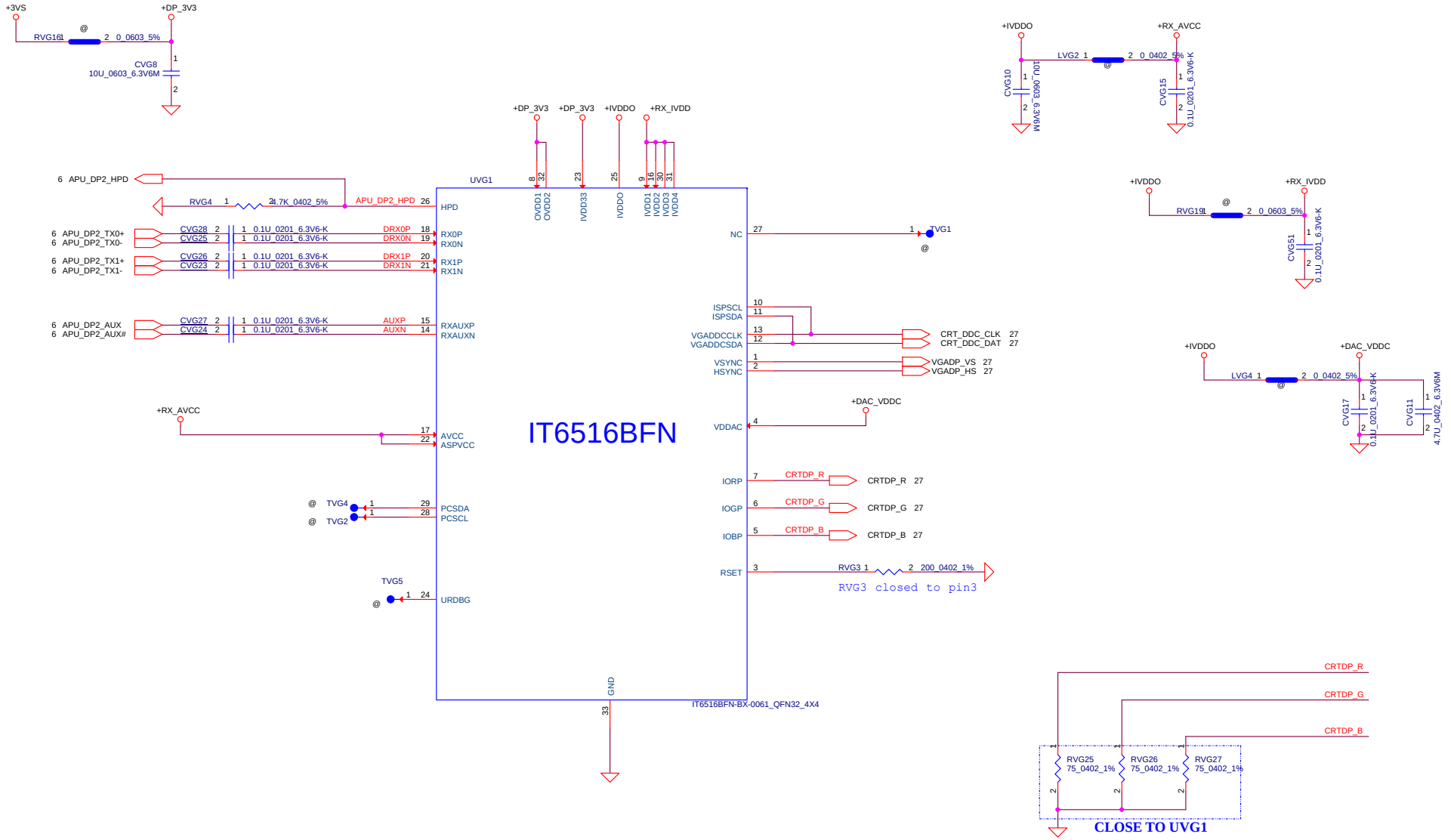


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	HDMI_CONN		
Size	Document Number		Rev
Custom	CG516		1.0
Date:	Tuesday, April 12, 2016	Sheet	25 of 51



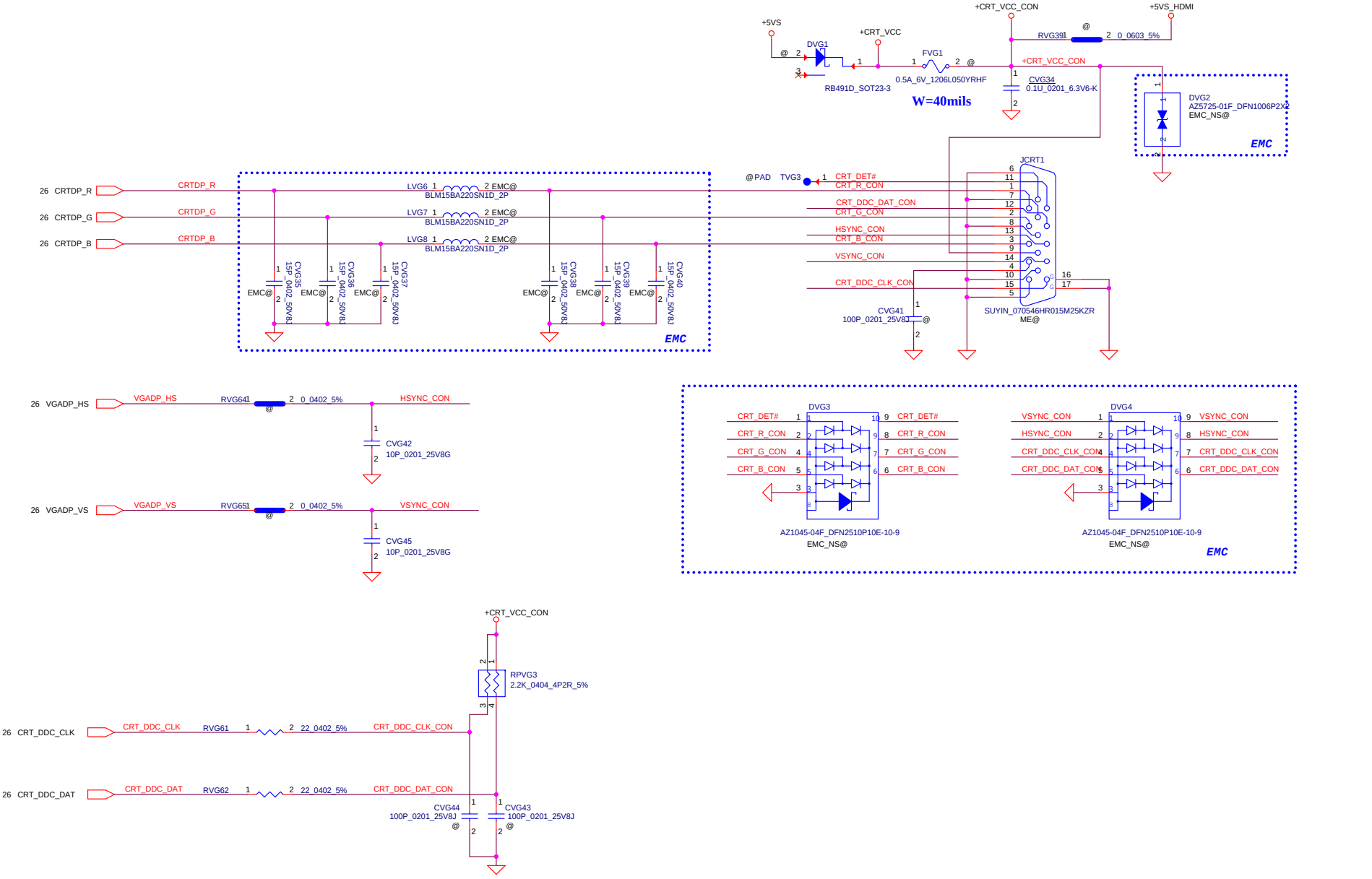
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: DP to CRT Convert(IT6515FN)

Size	Document Number	Rev
Custom	CG516	1.0

Date: Tuesday, April 12, 2016 Sheet 26 of 51

CRT Connector



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	CRT		
Size	Document Number		Rev
Custom	CG516		1.0
Date:	Tuesday, April 12, 2016	Sheet	27 of 51

+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%) 0.5ms < spec < 10 0ms

Need short

width : 40 mils

JL1 JUMP_43X79

Q14 LP2301ALT1G_SOT23-3

RL2 100K_0402_5% @

RL3 47K_0402_5%

36 LAN_PWR_ON#

CL8 0.1U_0201_6.3V6-K @

CL9 0.01U_0201_10V6K @

CL4 4.7U_0402_6.3V6M SIT1CD@

CL5 4.7U_0402_6.3V6M SIT1CD@

CL6 0.1U_0201_6.3V6-K

CL7 0.1U_0201_6.3V6-K

Close to Pin11 Close to Pin32 Close to Pin11 Close to Pin32

RL1 0_0603_5% @

CL1 4.7U_0402_6.3V6M SIT1CD@

CL2 0.1U_0201_6.3V6-K SIT1CD@

RL5 10K_0402_5% @

RL7 0_0402_5% @

RL6 0_0402_5% @

7,31,36 PCIE_WAKE#

31,36 LAN_WAKE#

PCIE_WAKE#_R

RL4 10K_0402_5% @

QL1 2N7002KW_SOT323-3

LAN_CLKREQ#_R

LAN_CLKREQ# 7

RL18 0_0402_5%

APU CLKREQ all both 3VS power plane

RL9 1K_0402_1%

RL11 15K_0402_5% @

ISOLATE# RL10 0_0402_5% LAN_PWR_ON#

RL8 2.49K_0402_1%

LAN_PWR_ON# RL12 0_0402_5%

TL3 TL4

7,15,31 PLT_RST#

4 PCIE_PRX_DTX_N2

4 PCIE_PRX_DTX_P2

CL10 0.1U_0201_6.3V6-K

CL11 0.1U_0201_6.3V6-K

CL10 close to Pin18

CL11 close to Pin17

UL1

33	GND		
32	AVDD33_2		
31	RSET		
30	AVDD10		
29	CKXTAL2		
28	CKXTAL1		
27	LED0		
26	LED1/GPIO		
25	LED2		
24	REGOUT		
23	VDDREG		
22	DVDD10		
21	LANWAKEB		
20	ISOLATEB		
19	PERSTB		
18	HSON	REFCLK_N	16 CLK_PCIE_LAN# → CLK_PCIE_LAN# 8
17	HSOP	REFCLK_P	15 CLK_PCIE_LAN → CLK_PCIE_LAN 8
		HSIN	14 PCIE_PTX_C_DRX_N2 → PCIE_PTX_C_DRX_N2 4
		HSIP	13 PCIE_PTX_C_DRX_P2 → PCIE_PTX_C_DRX_P2 4
		CLKREQB	12 LAN_CLKREQ#_R
		AVDD33_1	11 +3VALW_LAN
		MDIN3	10 LAN_MDI3- → LAN_MDI3- 29
		MDIP3	9 LAN_MDI3+ → LAN_MDI3+ 29
		AVDD10_2	8 +LAN_VDD10
		MDIN2	7 LAN_MDI2- → LAN_MDI2- 29
		MDIP2	6 LAN_MDI2+ → LAN_MDI2+ 29
		MDIN1	5 LAN_MDI1- → LAN_MDI1- 29
		MDIP1	4 LAN_MDI1+ → LAN_MDI1+ 29
		AVDD10_1	3 +LAN_VDD10
		MDIN0	2 LAN_MDI0- → LAN_MDI0- 29
		MDIP0	1 LAN_MDI0+ → LAN_MDI0+ 29

RTL8111GUL-CG_QFN32_4X4

8111GUL@

YL1 25MHZ_10PF_7V25000014

LAN_XTALI LAN_XTALO

CL12 10P_0402_50V8J

CL13 12P_0402_50V8-J

follow G CarrizoL 10pf

For RTL8111GUL/ RTL8106EUL (SWR mode)
For RTL8111H (LDO mode) RL19 stuf f

8111H@ RL19 0_0805_5%

+LAN_REGOUT LL1 2.2UH_NLC252018T-2R2J-N_5% 8111GUL@

Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

CL15 4.7U_0603_6.3V6K

CL16 0.1U_0201_6.3V6-K

+LAN_VDD10

CL17 0.1U_0201_6.3V6-K

CL18 0.1U_0201_6.3V6-K

CL19 0.1U_0201_6.3V6-K

CL20 0.1U_0201_6.3V6-K

CL21 1U_0402_6.3V6K @

CL22 0.1U_0201_6.3V6-K @

Close to Pin3, 8, 22, 30

Close to Pin22(Reserved)

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: LAN_RTL8111GUL

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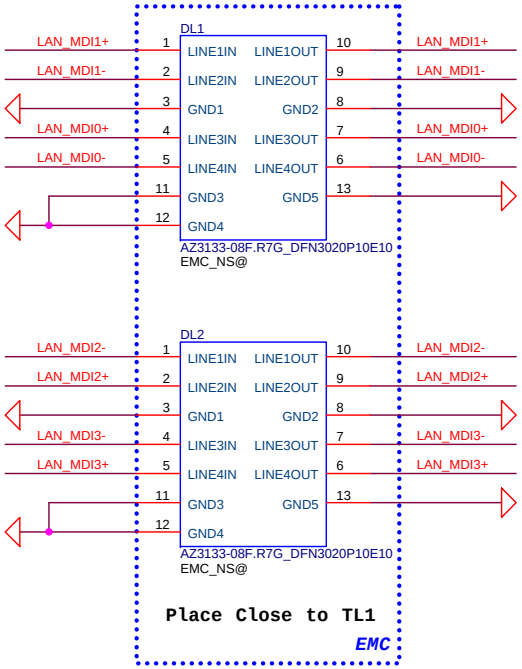
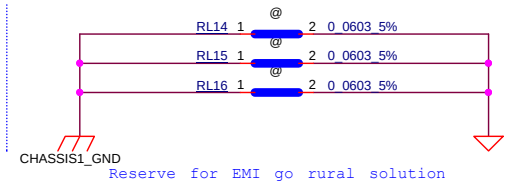
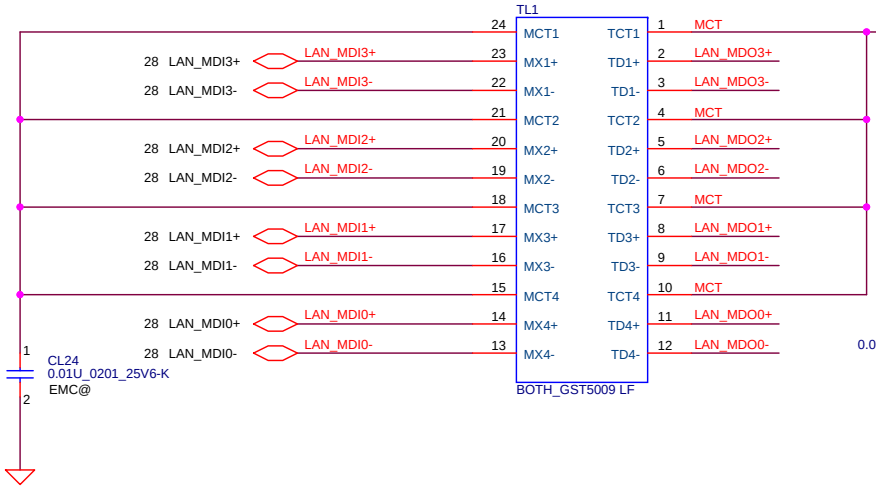
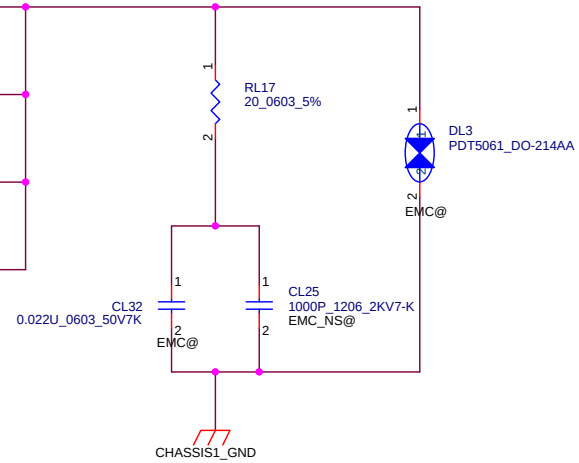
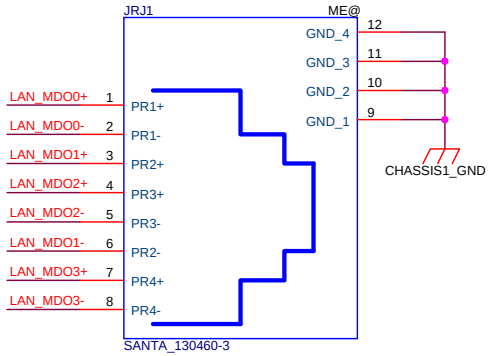
DL1/DL2
1'S PN:SC300003M00











Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: LAN_Transformer

Size	Document Number	Rev
B	CG516	1.0

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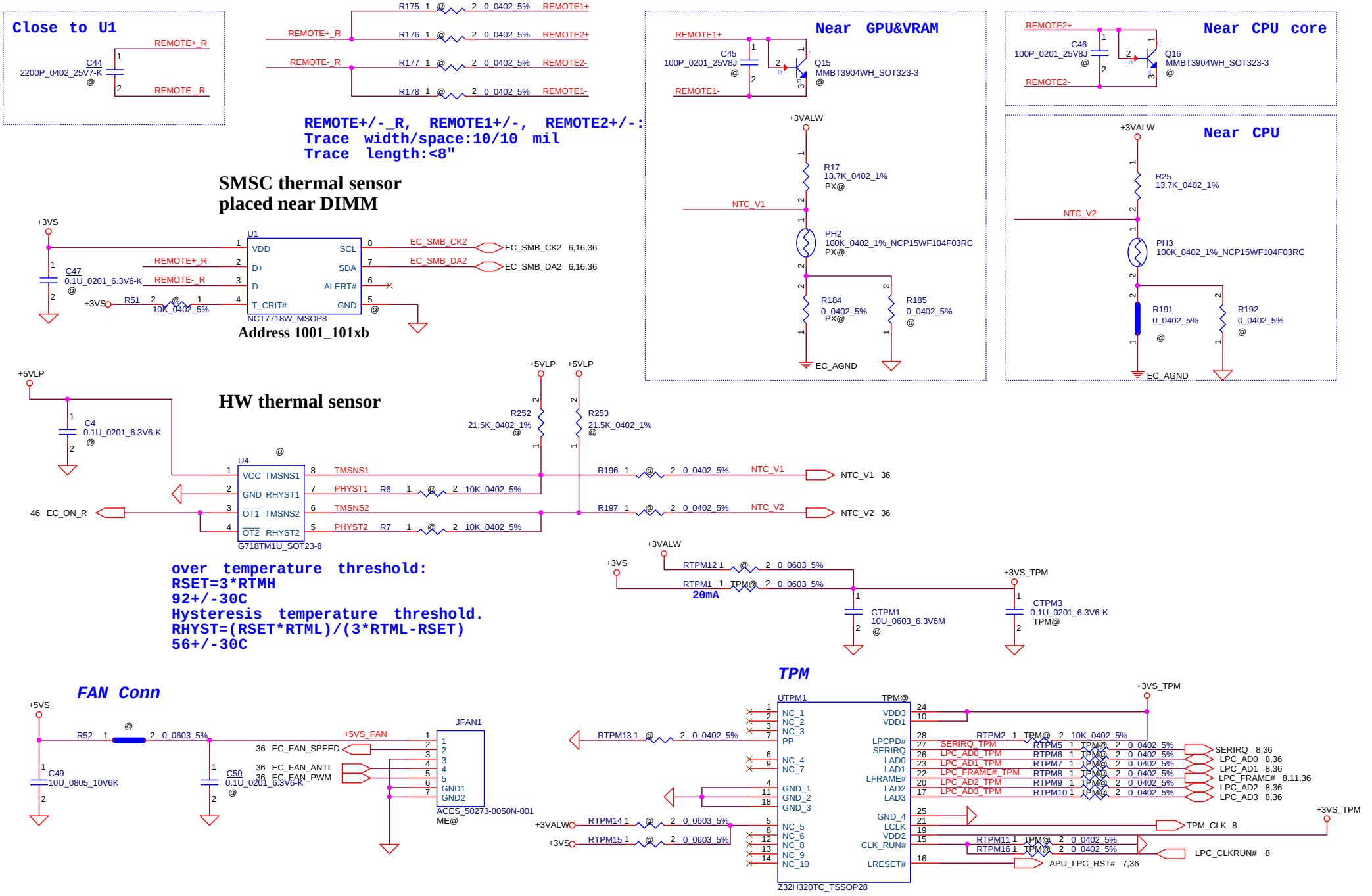

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: *Thermal sensor/FAN CONN/TPM*

Size	Document Number	Rev
Custom	CG516	1.0

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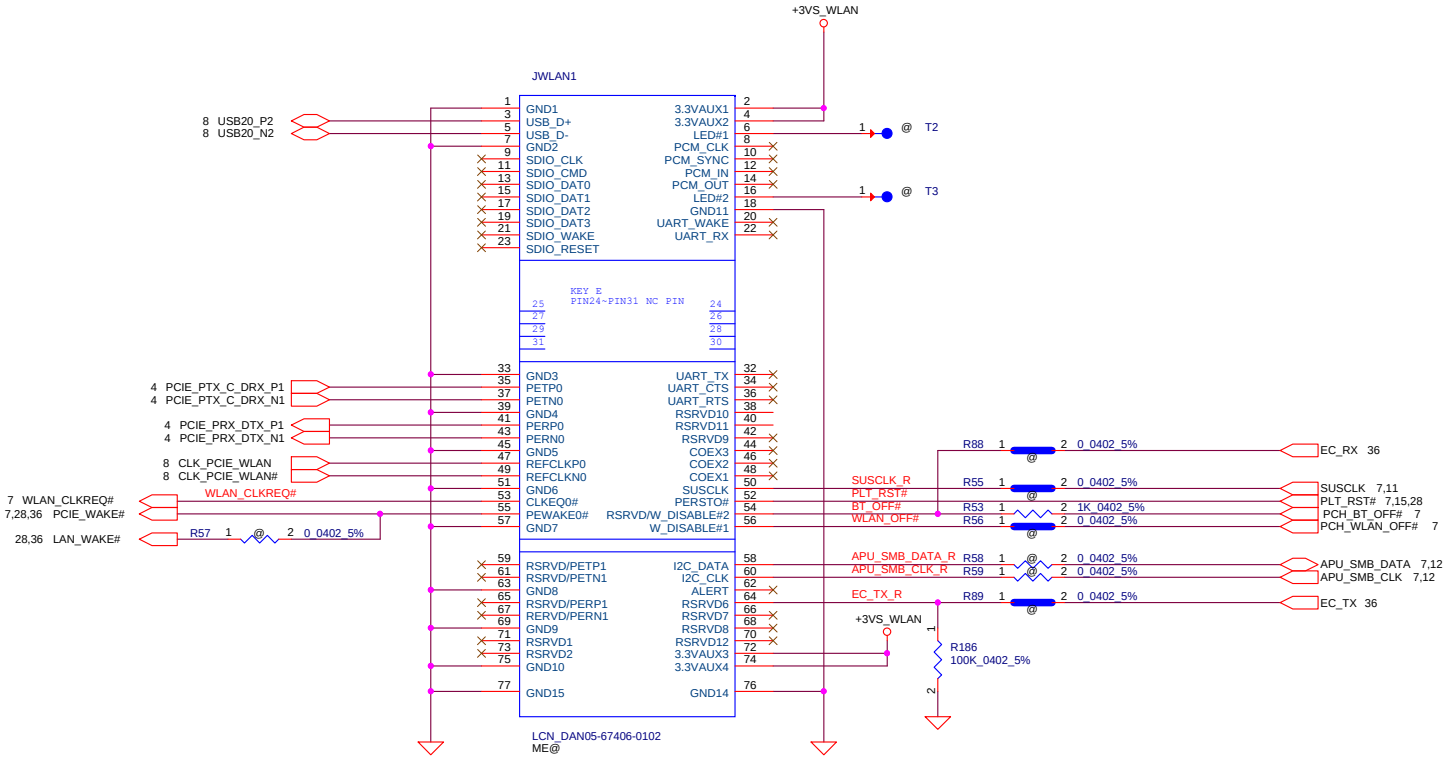
Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: NGFF WLAN

Size	Document Number	Rev
Custom	CG516	1.0

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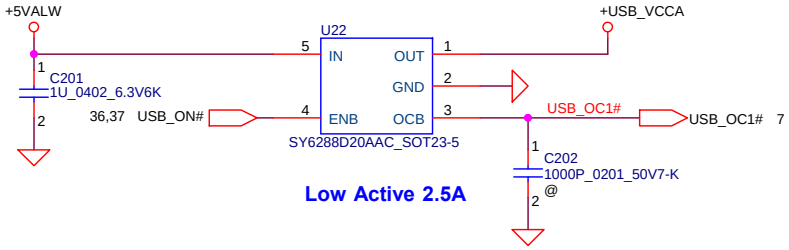
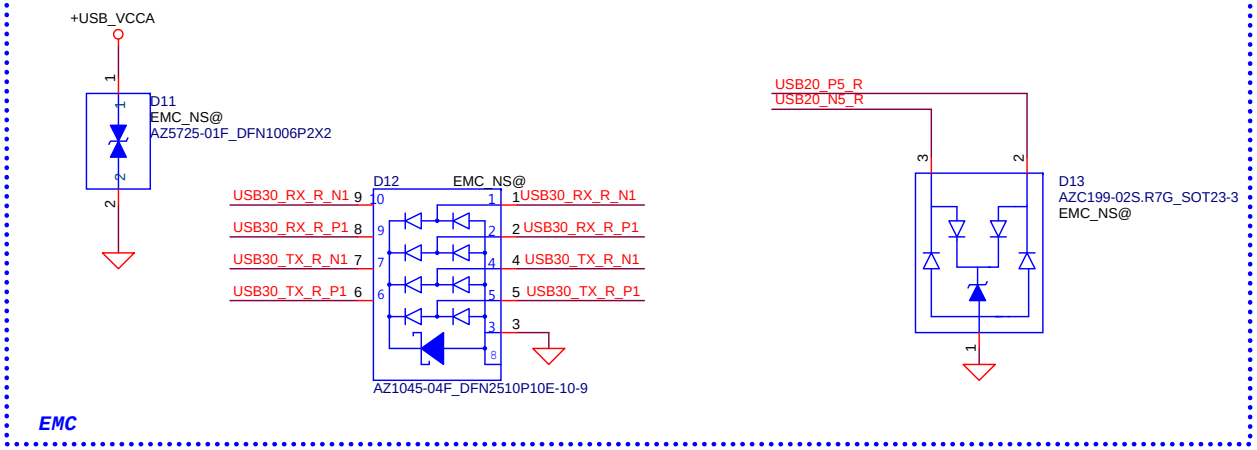
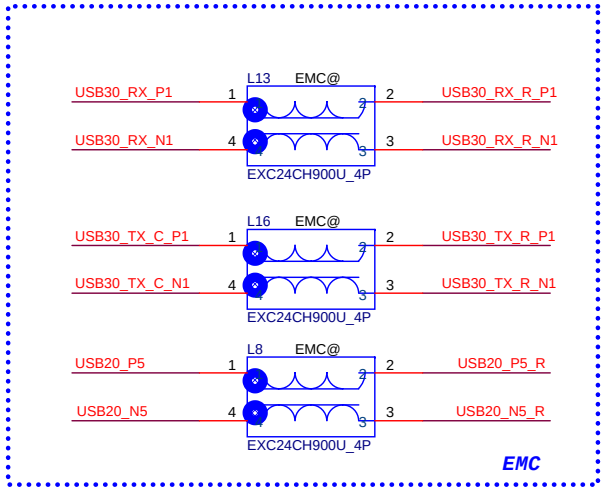
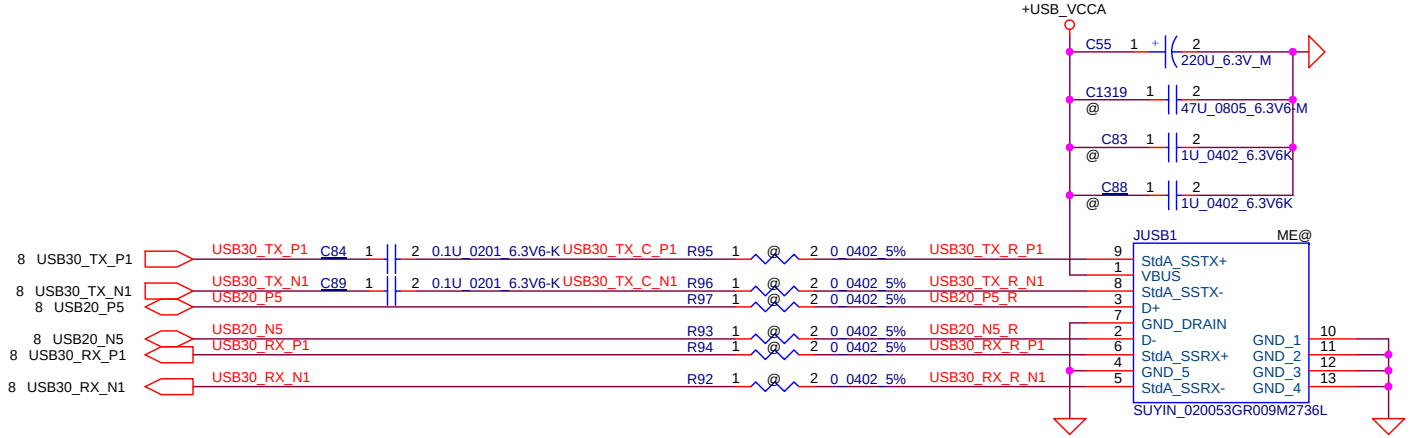
Left Side USB3.0 Port X 1









Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **USB PORT (LEFT)**

Size	Document Number	Rev
Custom	CG516	1.0

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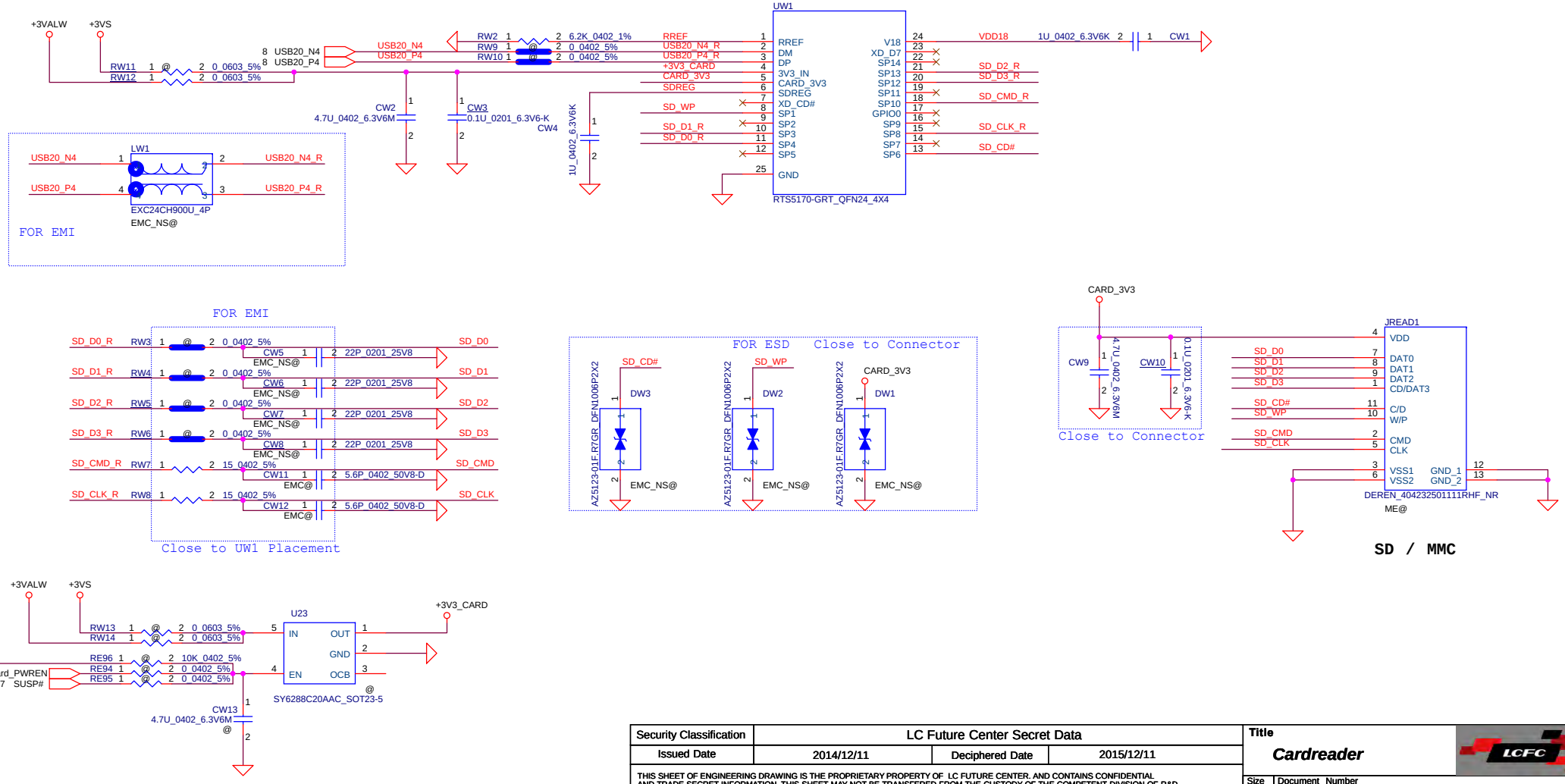

Security Classification	LC Future Center Secret Data		
Issued Date	2014/12/11	Deciphered Date	2015/12/11

Title: **Cardreader**

Size	Document Number	Rev
Custom	**CG516**	1.0

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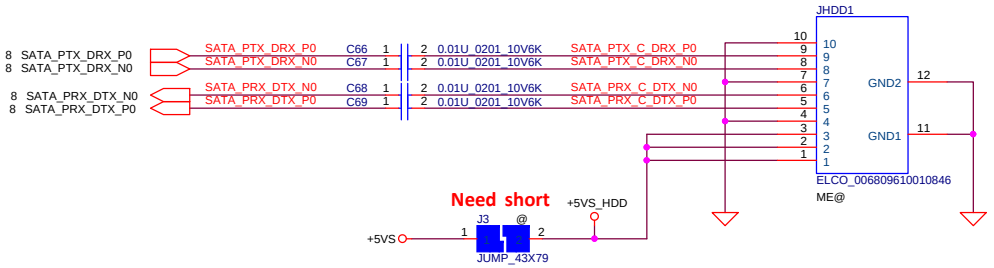
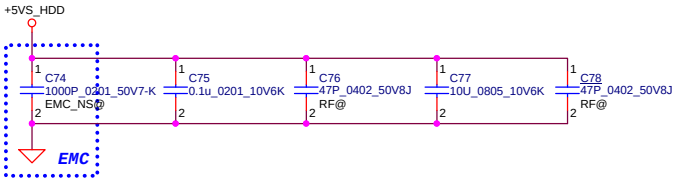
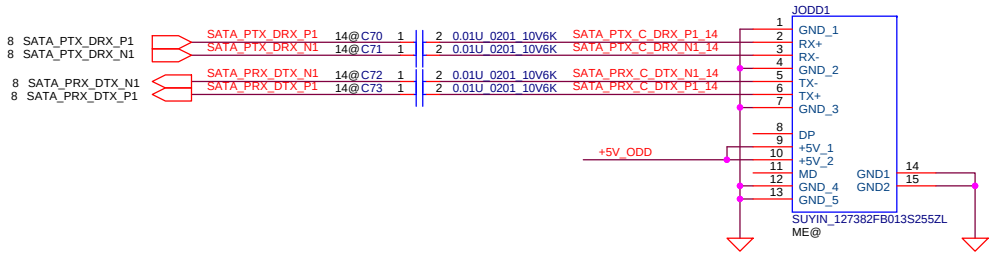
SATA HDD Conn.



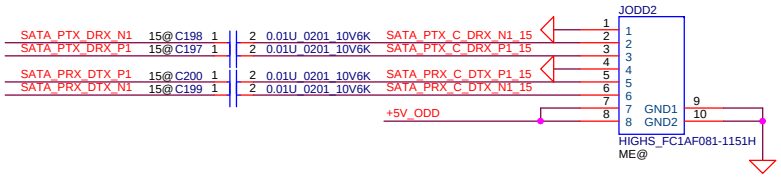


FOR 14" SATA ODD Conn.

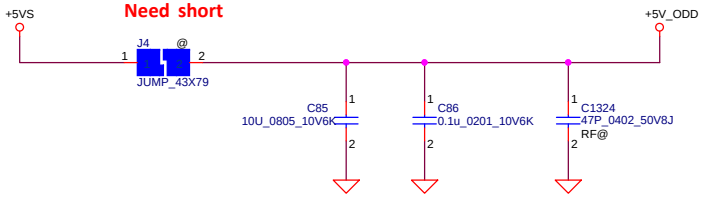


FOR 15" SATA ODD FFC Conn

SATA 15 ODD P/N pin assgin is different from G SKL



+5VS to +5V_ODD



ODD DA???

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	HDD/ODD CONN		
Size	Document Number		Rev
Custom	CG516		1.0
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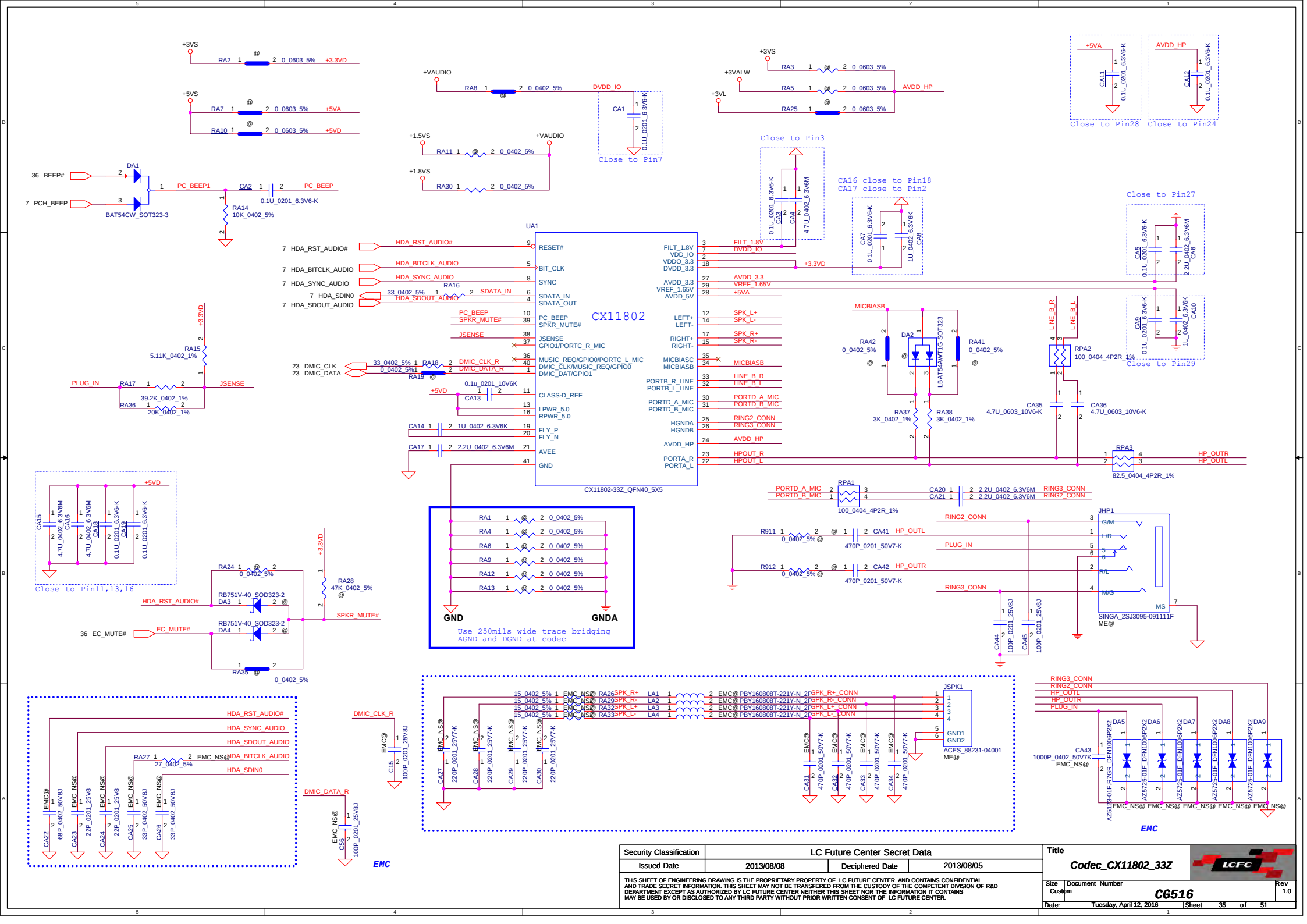

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title: Codec_CX11802_33Z

Size	Document Number	Rev
Custom	CG516	1.0

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Config LPC 3.3V S0 power
set register GCR23 0 Bit to 1b Config SERIRQ 3.3V S0 power

IT8886H need VHSPI ready before VCC,
at least 2ms mismatch.

Close EC

minimum trace width 12 mil

All capacitors close to EC

HSPI (supplied by VHSPI if IT8886HE): CPU to EC 1.8VS
FSPI (supplied by VSTBY if IT8886HE): EC to SPI Rom 3.3VALW/VL?

EC_SCI# in APU internal pull high to 3VALW

ENBKL is 1.8V level signal, GPD4 EC setting 1.8V GPI

IT8886HE/AX
LQFP-128L

AMD request SIC/SID (EC_SMB2) pull high 1K

SMBus0:PMIC
SMBus1:Charger/Battery
SMBus2:APU/GPU/thermal sensor

FSPI,GPG6 can't pull up

GPG0 (VGA_AC_DET)can't pull up

EC set GPH0 OD output for EC_RSMRST# is 1.8V level
1224 change GPH0 to push pull output

XLP_OUT can't be set normal GPIO Pin

change reserved EC_RTCRST#_ON for GPU HOT

GPG0 def mode GPO H
GPG1 def mode GPO L internal Pull down

H_PROCHOT#

VDDGFX_PD=0 -> VDDCR_GFX VRM turned ON.
VDDGFX_PD=1 -> VDDCR_GFX VRM turned OFF

will cost down in future if EC internal logic verify ok

change reserved APUTYPE for GPU HOT

Mirror Core strap

when mirror, GPG2 pull high
when no mirror, GPG2 pull low

for VR_APU_PWRGD undershoot issue

Reserve Factory EC flash, need confirm with ITE

EMC

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title: EC ITE8586LQFP

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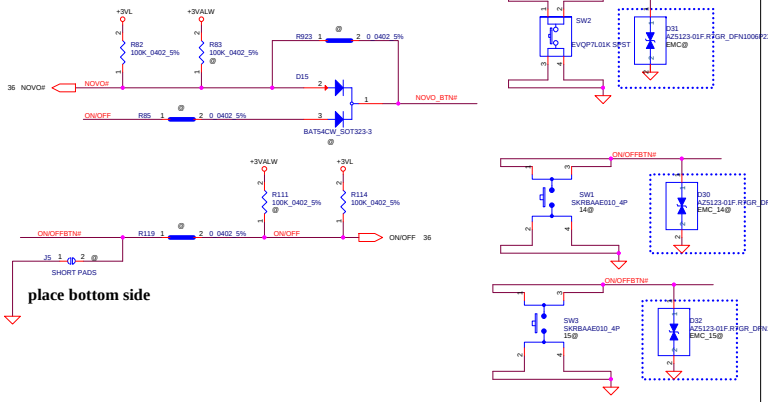
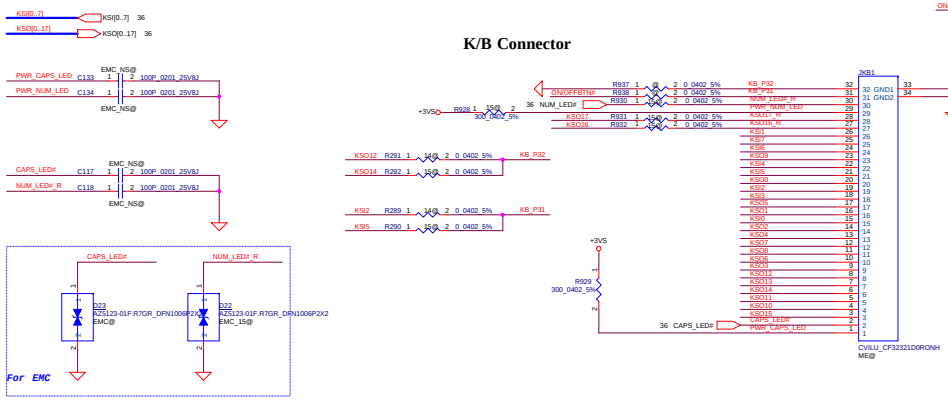
ON/OFF switch



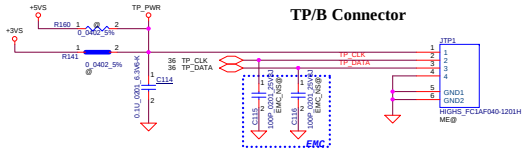
place bottom side

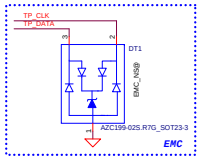
K/B Connector



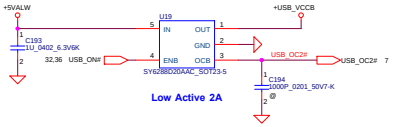
place near KB Conn

TP/B Connector

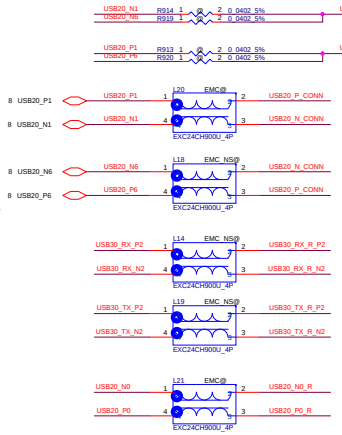


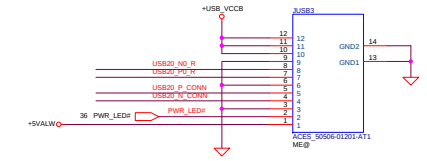


Right Side USB2.0 Port X 2 (USB/B)



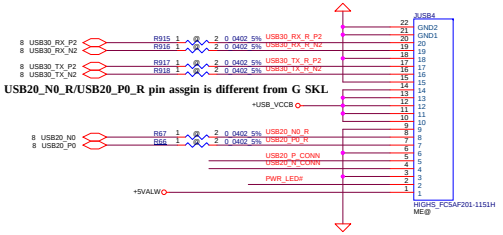
Low Active 2A





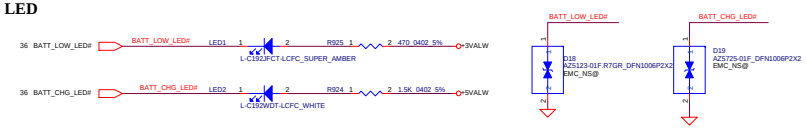
USB I/O Connector for G, USB2.0*2

USB20_N0_R/USB20_P0_R pin assgin is different from G SKL

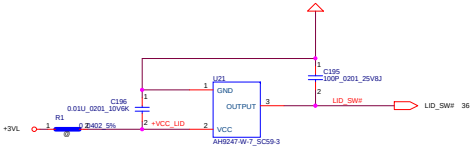


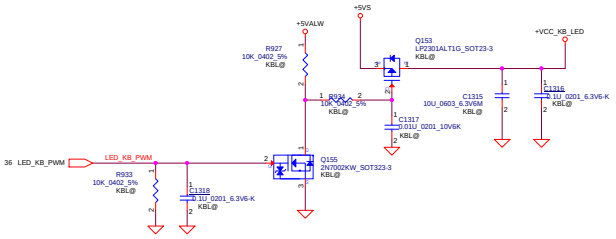
USB I/O Connector for Z, USB2.0*1+USB3.0*1

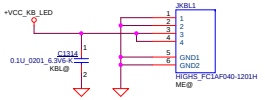
LED



check LED location and BOM structure when placement and Load BOM, PWR LED and BATT LED have the same location on 14"/15" 02/26







Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **KBD/PWR/IO/LED/TP Conn.**

Size: Custom | Document Number: **CG5516** | Rev: 1.0

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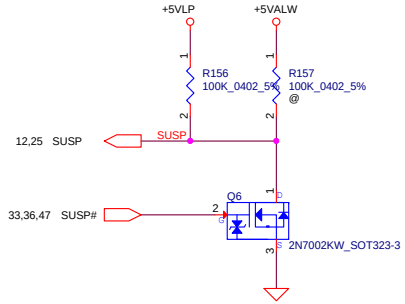
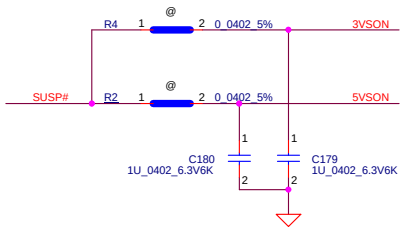
EC need 1.8VS power ready before 3.3VS, chagne C173 from 2200pf to 4700pf

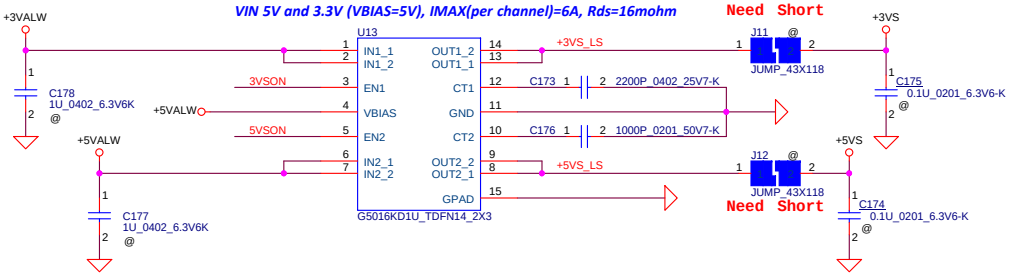
Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 5.78ms
+5VS, C176 --> 1.71ms

modify load swt ich fro m APL3523 to G5016KD1UTDFN14P





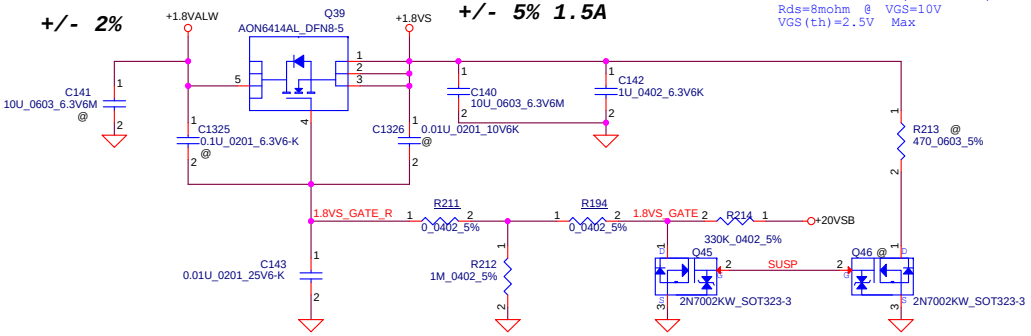


+1.8VALW to +1.8VS

+/- 2%

+/- 5% 1.5A

AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max

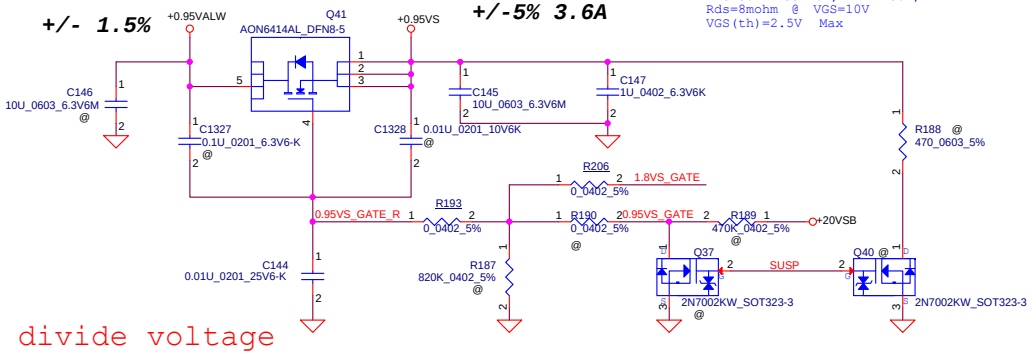


+0.95VALW to +0.95VS

+/- 1.5%

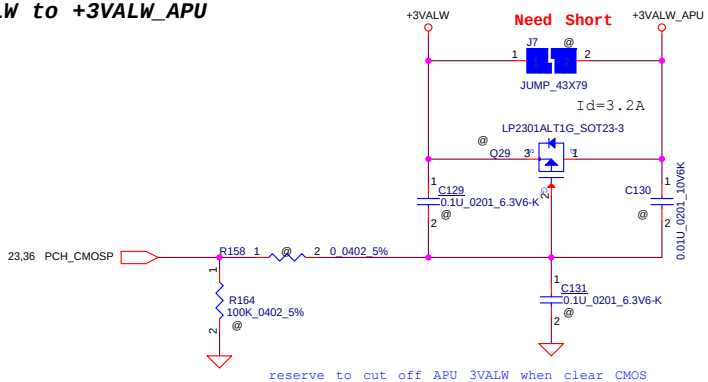
+/-5% 3.6A

AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max



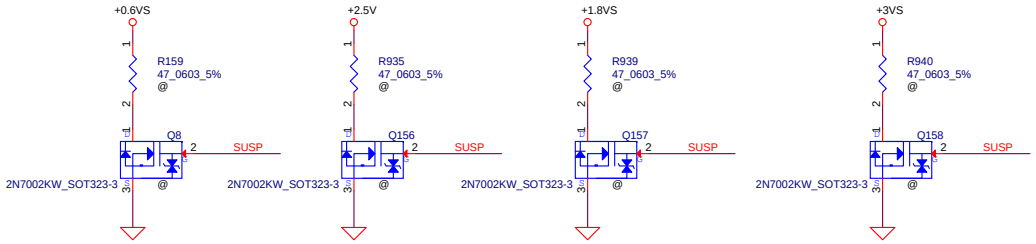
20VSB will change to 6V in DC mode, careful the Res divide voltage

+3VALW to +3VALW_APU



reserve to cut off APU 3VALW when clear CMOS

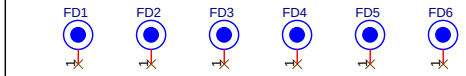
For DisCharge



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	DC V TO VS INTERFACE		
Size: Custom	Document Number: CG516		Rev: 1.0
Date: Tuesday, April 12, 2016	Sheet 38 of 51		

PCB Fedical Mark PAD



NH1 HOLEA — PAD_O2P6X2P5D2P6X2P5N
NH2 HOLEA — PAD_O3P0X2P5d3P0X2P5N
NH3 HOLEA — PAD_O2P5X2P9D2P5X2P9N

H1 HOLEA — PAD_D3P4
H3 HOLEA — CHASSIS1_GND, PAD_CT7P0B9P0D3P0
NH4 HOLEA — PAD_C3P0D3P0N
H5 HOLEA — PAD_C8P0
H6 HOLEA — PAD_C5P0
H4 HOLEA — pad_ct4p5b7p0d3p3
H10 HOLEA — PAD_C7P0D3P3

H11 HOLEA — PAD_CT7P0B9P0D3P0
H12 HOLEA — pad_ct6p0b7p0d4p0
H13 HOLEA — pad_ct6p0b7p0d4p0
H14 HOLEA — pad_ct6p0b7p0d4p0
H15 HOLEA — pad_ct6p0b7p0d4p0
H16 HOLEA — PAD_ShapeT9P0X8P0CB9P0D3P0
H17 HOLEA — PAD_ShapeT7P5X8P0D3P4
H18 HOLEA — PAD_CT7P0B6P0D3P3
H19 HOLEA — PAD_C7P0D3P0
H20 HOLEA — PAD_C7P0

H21 HOLEA — PAD_C6P0D2P5

JSPON1 — SHIELDING_PS-25G_5P5X3_1P

JSPON2 — SHIELDING_PS-25G_5P5X3_1P

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: Hole

Size	Document Number	Rev
B	CG516	1.0

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ZZZ1
PCB CG516 NM-A741 NS-A741/A743/A744
DAZ12300100 **PCB_MB**

UL1
LAN Chip
SA000074W00
8111H@ **LAN Chip**

ZZZ3
HDMI Loga
HDMI@
RO00000040J **HDMI Logo**

UC2
BRISTOL FM980PADY44AB 2.7G PR 1.0
FX9800P@
SA00007RC10

UC2
BRISTOL AM970PADY44AB 2.5G PR 1.0
A129700P@
SA00007RE10

UC2
BRISTOL AM960PADY44AB 2.4G PR 1.0
A109600P@
SA00007TF00 **APU type**

ZZZ8
Samsung DRAM
MDS8GX4@
X7611912002

ZZZ9
Micron DRAM
MDM8GX4@
X7611912001 **DRAM X76 BOM**

UD1 MD_S8G@ K4A8G165WB-BCPB SA00007DA10
UD2 MD_S8G@ K4A8G165WB-BCPB SA00007DA10
UD3 MD_S8G@ K4A8G165WB-BCPB SA00007DA10
UD4 MD_S8G@ K4A8G165WB-BCPB SA00007DA10
RC257 MD_S8G@ 10K_0402_5% SD028100 28J
RC264 MD_S8G@ 2K_0402_5% SD028200 18J
DRAM_Samsung 4G

UD1 MD_M8G@ MT40A512M16HA-083E:A SA000079F10
UD2 MD_M8G@ MT40A512M16HA-083E:A SA000079F10
UD3 MD_M8G@ MT40A512M16HA-083E:A SA000079F10
UD4 MD_M8G@ MT40A512M16HA-083E:A SA000079F10
RC258 MD_M8G@ 2K_0402_5% SD028200 18J
RC265 MD_M8G@ 10K_0402_5% SD028100 28J
DRAM_Micron 4G

DRAM_Hynix 4G

ZZZ5
Hynix
H4GX4@
X7610512101

ZZZ6
Samsung
S4GX4@
X7610612101

ZZZ7
MICRON
M4GX4@
X7610612001

UV5 H4G@ H5TC4G63CFR-N0C 4Gb SA00007DU10
UV6 H4G@ H5TC4G63CFR-N0C 4Gb SA00007DU10
UV7 H4G@ H5TC4G63CFR-N0C 4Gb SA00007DU10
UV8 H4G@ H5TC4G63CFR-N0C 4Gb SA00007DU10
RV70 H4G@ 4.75K_0402_1% SD034475 18J
VRAM_Hynix_256M*16 **000**

UV5 M4G@ MT41J256M16LY-091G:N SA00007QJ00
UV6 M4G@ MT41J256M16LY-091G:N SA00007QJ00
UV7 M4G@ MT41J256M16LY-091G:N SA00007QJ00
UV8 M4G@ MT41J256M16LY-091G:N SA00007QJ00
RV63 M4G@ 4.53K_0402_1% SD034453 18J
RV70 M4G@ 2K_0402_1% SD034200 18J
VRAM_Micron_256M*16 **010**

UV5 S4G@ K4W4G1646E-BC1A 4Gb SA000063F20
UV6 S4G@ K4W4G1646E-BC1A 4Gb SA000063F20
UV7 S4G@ K4W4G1646E-BC1A 4Gb SA000063F20
UV8 S4G@ K4W4G1646E-BC1A 4Gb SA000063F20
RV63 S4G@ 8.45K_0402_1% SD000011R00
RV70 S4G@ 2K_0402_1% SD034200 18J
VRAM_Samsung_256M*16 **001**

DRAM ID config

Memory Type		BOARD_ID3 AGPIO15 internal pull up 40K	BOARD_ID4 AGPIO13 internal pull up 40K	BOARD_ID5 AGPIO14 internal pull up 40K	BOARD_ID6 AGPIO9 internal pull Low 40K
512Mx16	Samsung K4A8G165WB-BCPB	1 RC257:stuff RC258:NC	0 RC265:NC RC264:stuff		
	Micron MT40A512M16HA-083E:A	0 RC257:NC RC258:stuff	1 RC265:stuff RC264:NC		

VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: *Virtual symbol*

Size	Document Number	Rev
Custom	CG412	0.1
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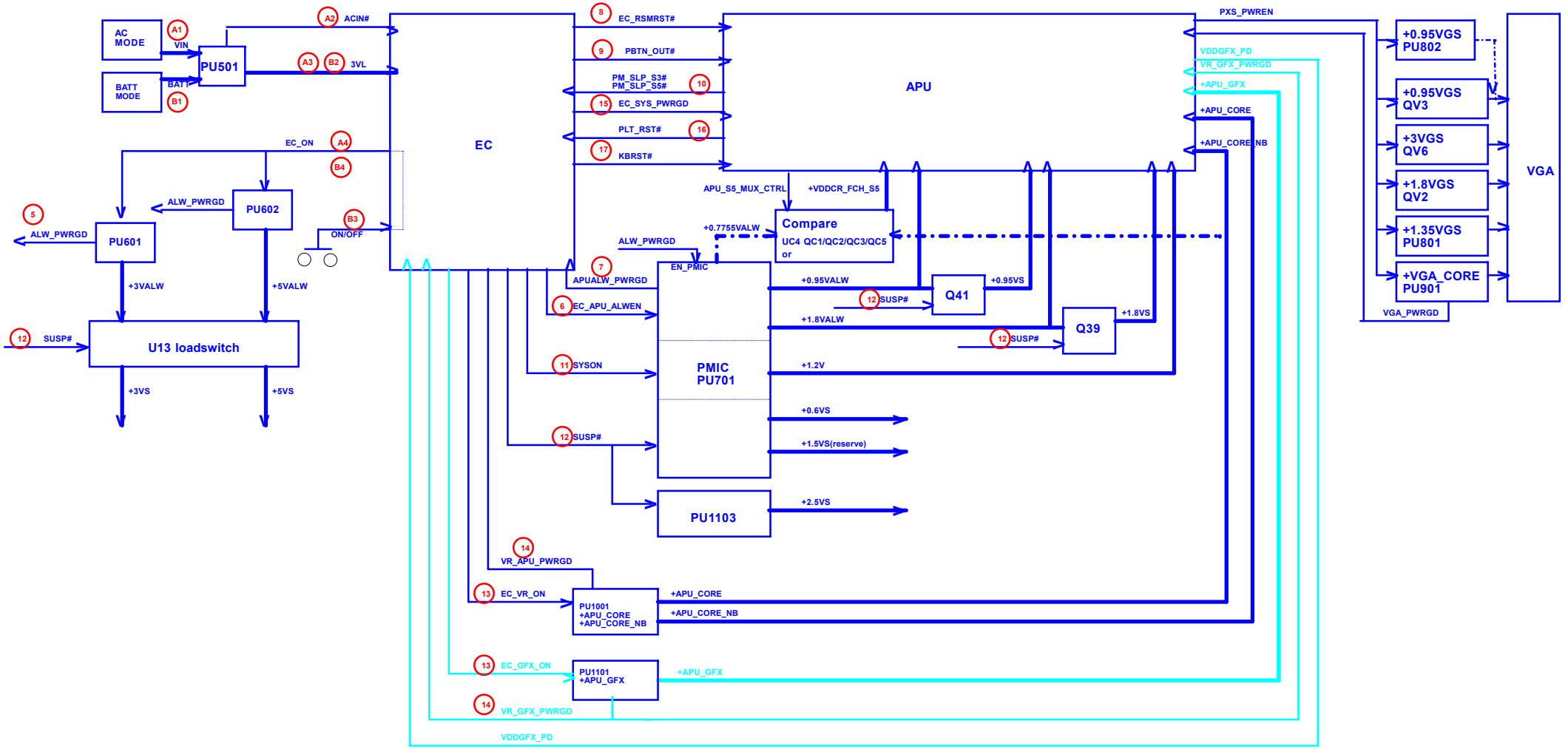

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: *Power sequence Block*

Size	Document Number	Rev
Custom	CG516	1.0

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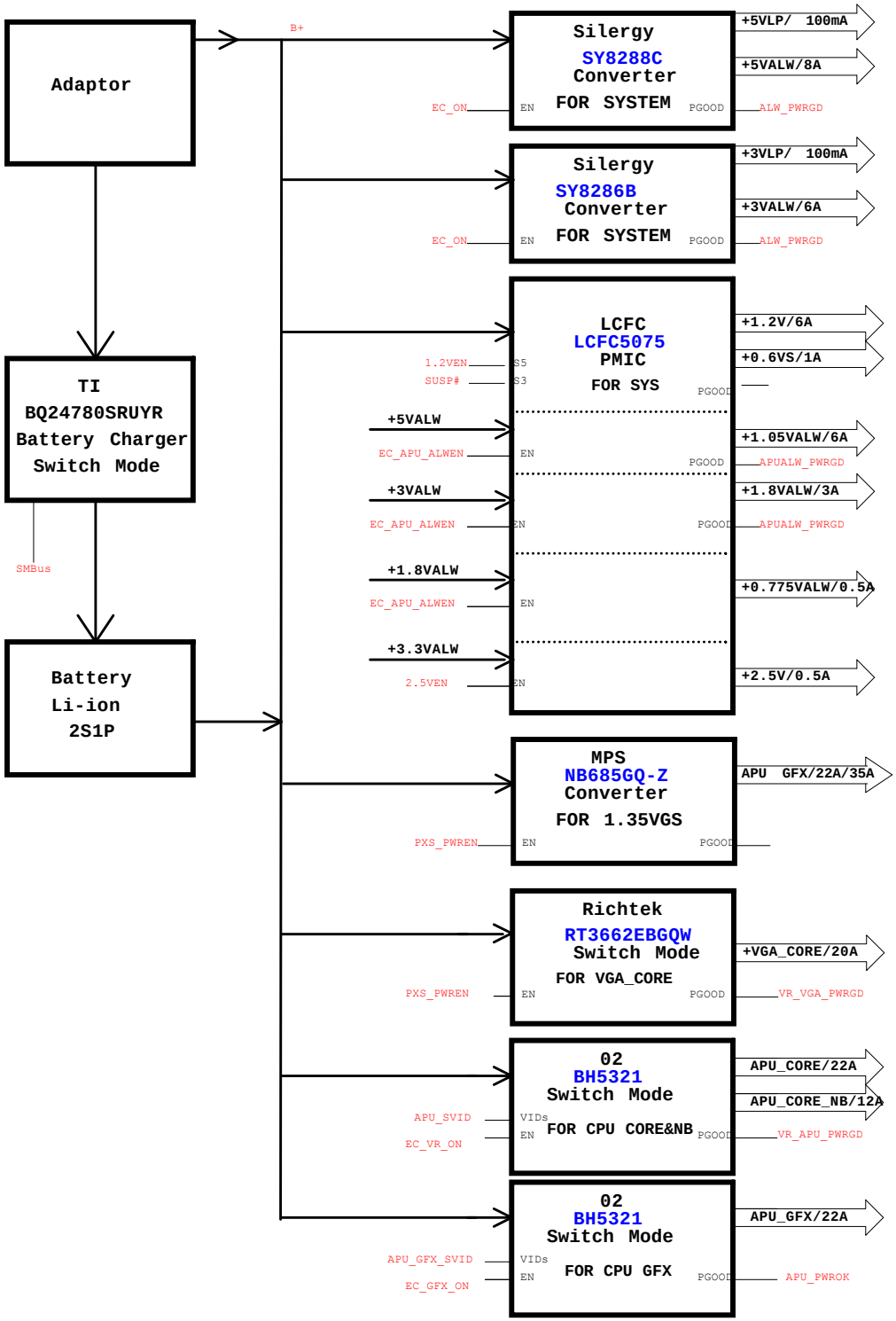
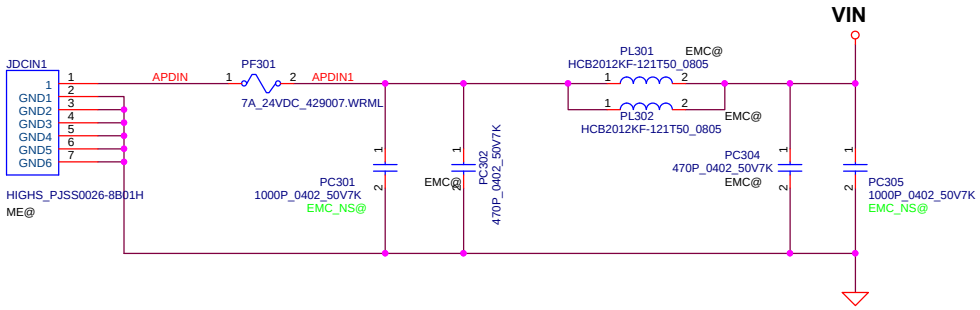


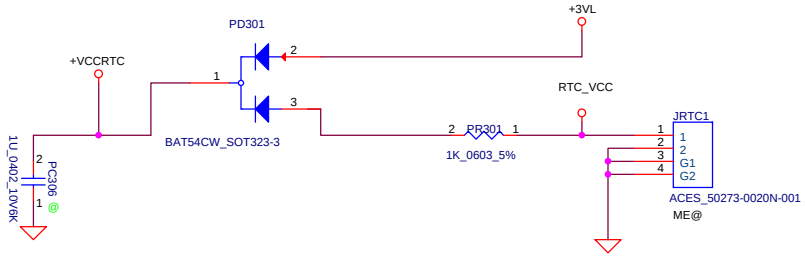
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: **Power Diagram**

Size	Document Number	Rev
Custom	CG516	1.0

Date: Tuesday, April 12, 2016 Sheet 42 of 51

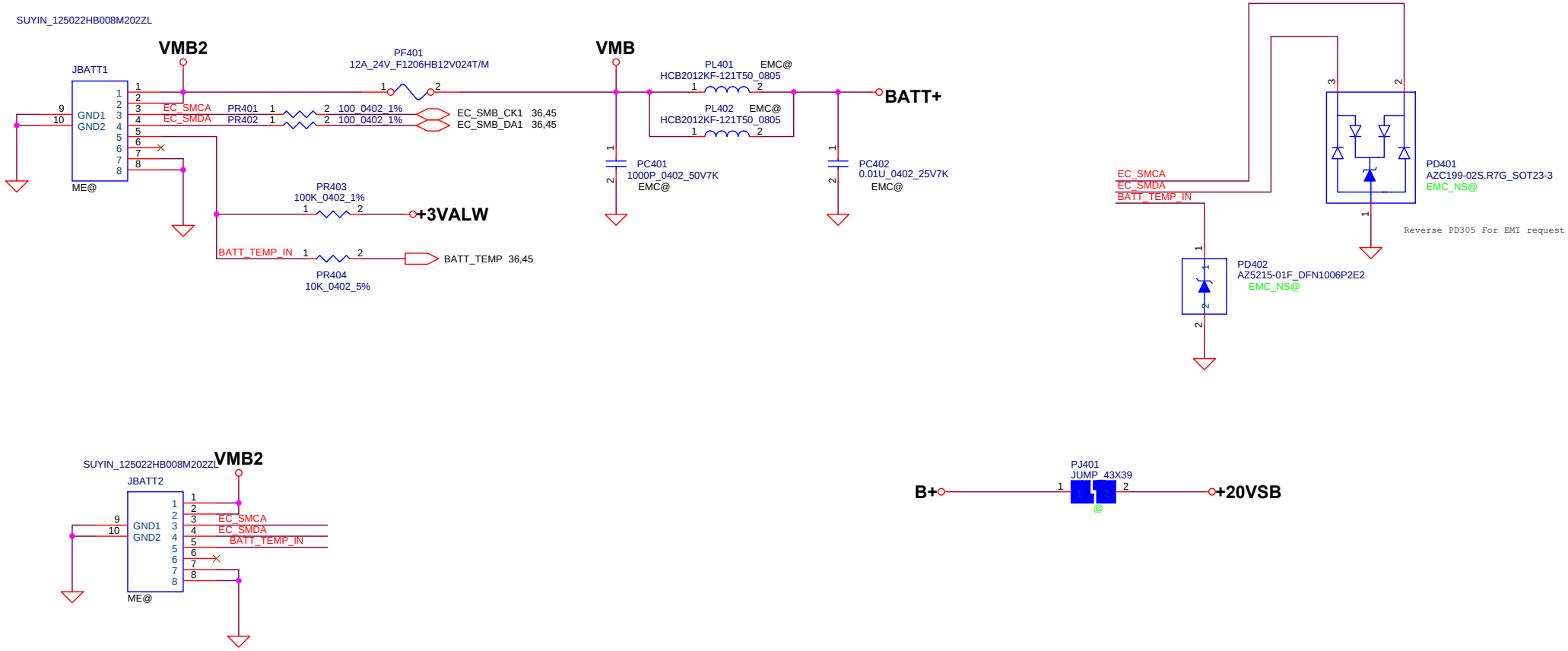




Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: **DCIN / RTC**

Size: Custom	Document Number: CG516	Rev: 1.0
Date: Tuesday, April 12, 2016	Sheet 43 of 51	



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: **BATTERY CONN/OTP**

Size	Document Number	Rev
B	CG516	1.0

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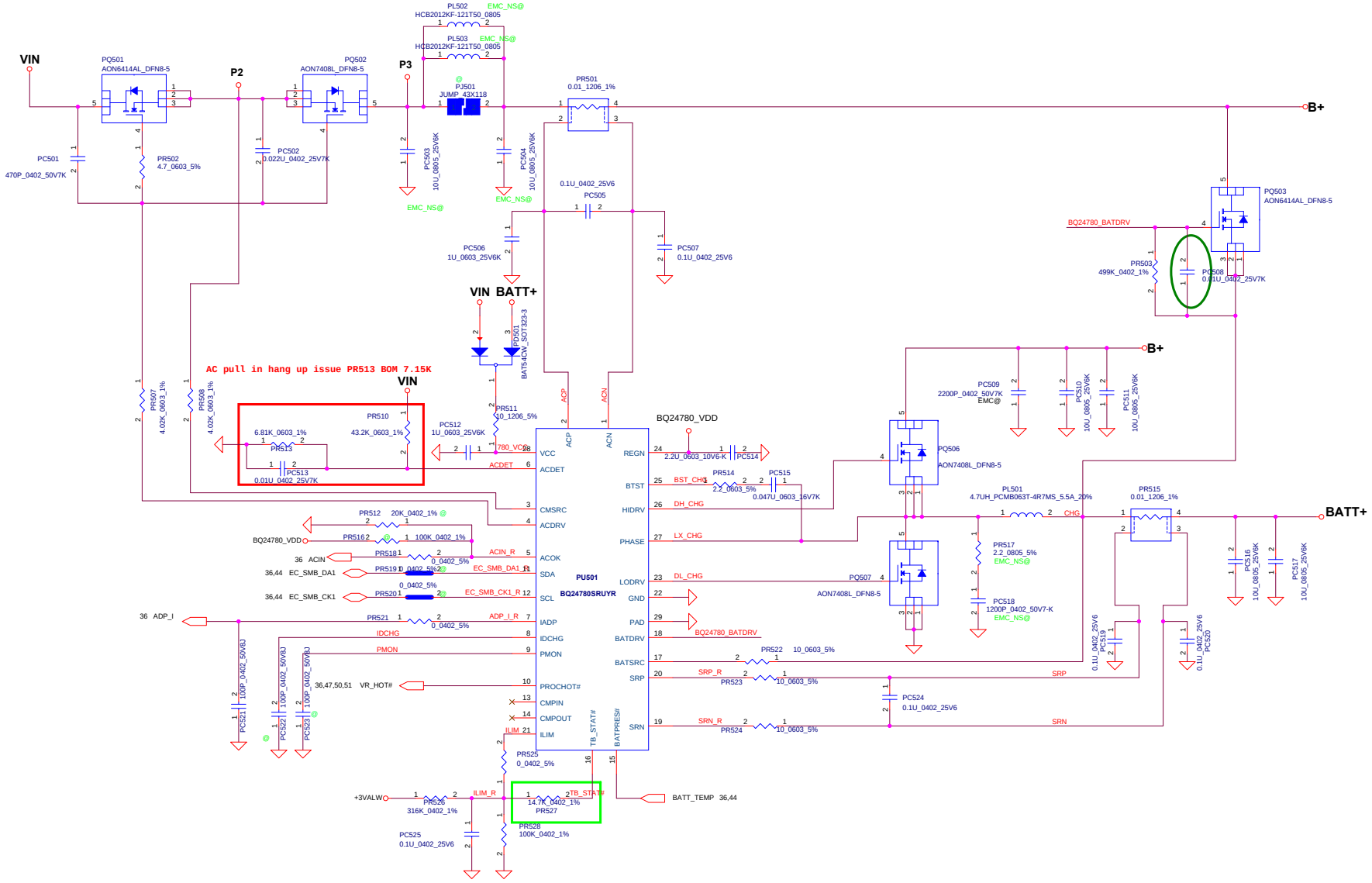

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **CHARGER**

Size	Document Number	Rev
C	CG516	1.0

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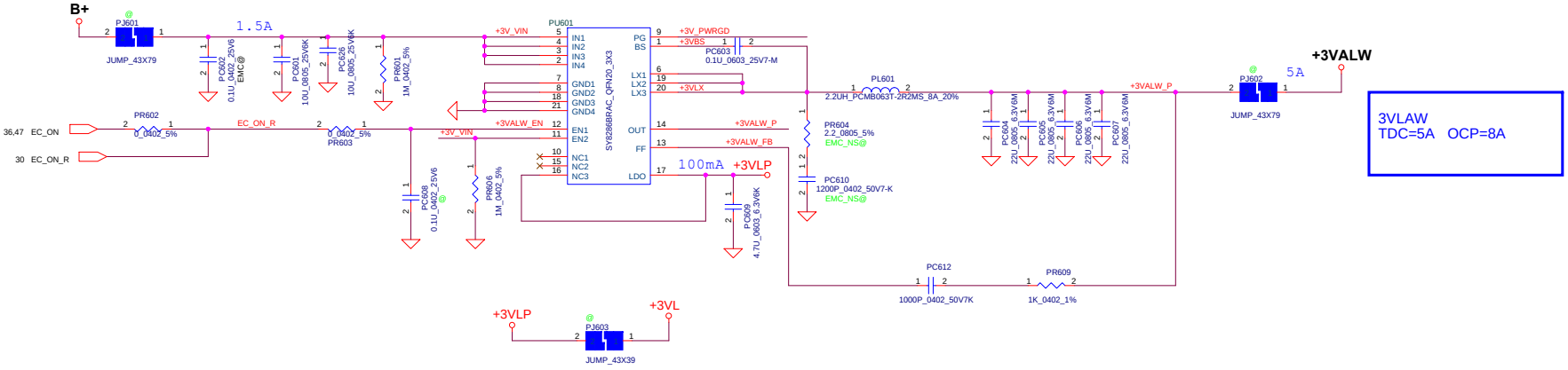

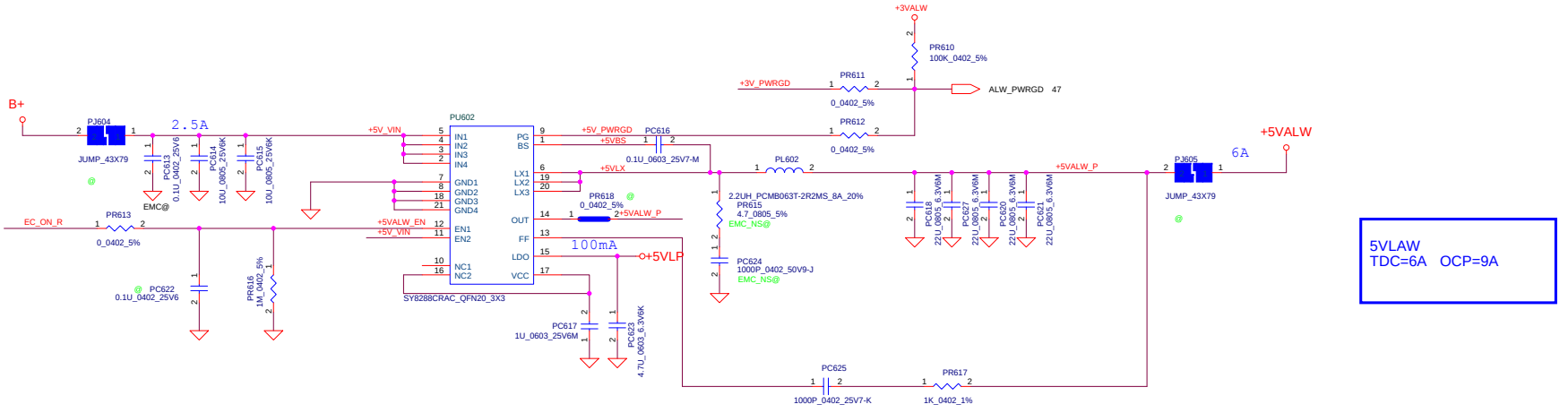

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: PWR_3VALW/5VALW

Size	Document Number	Rev
C	CG516	1.0

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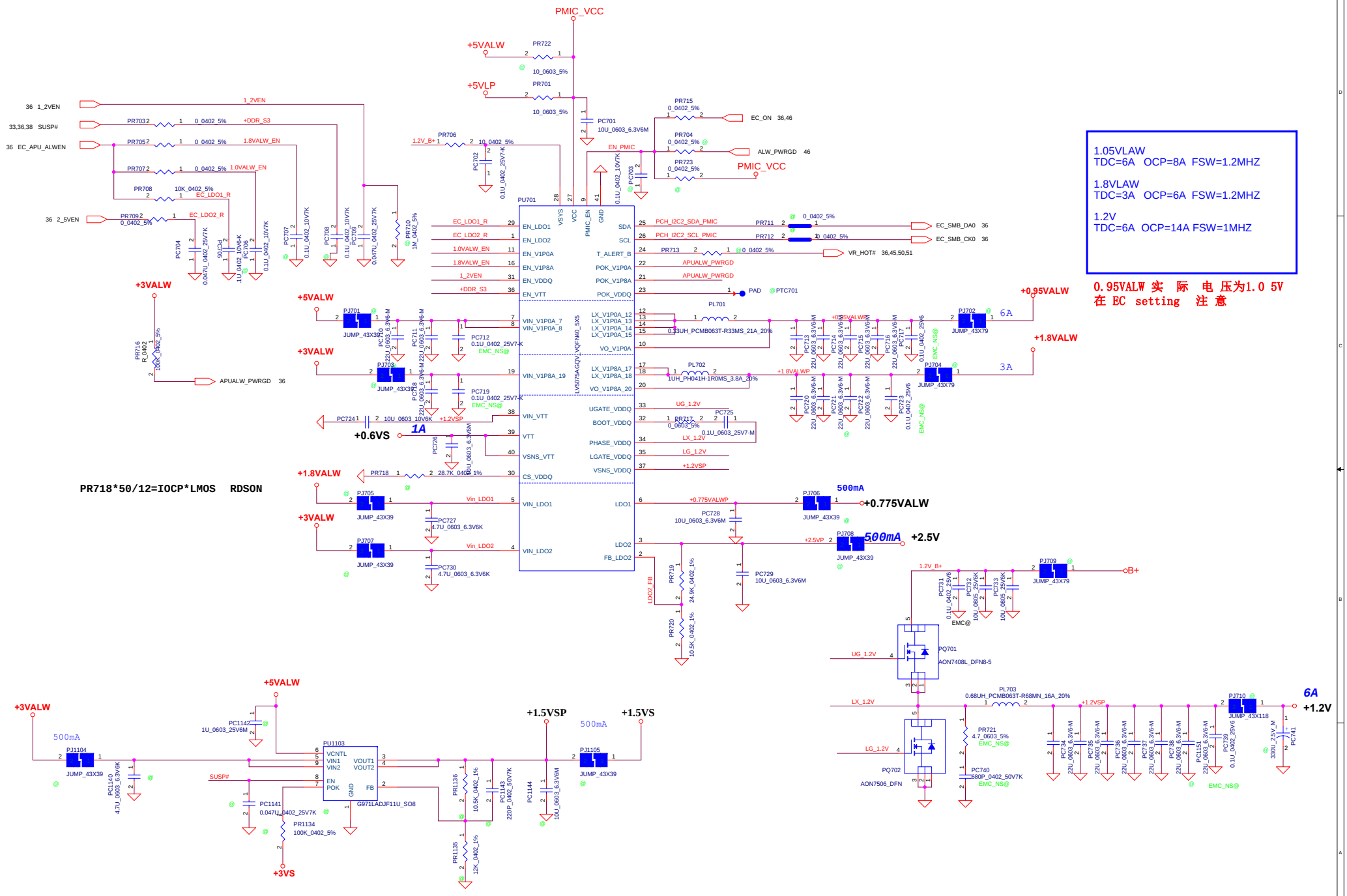

1.05VLAW
TDC=6A OCP=8A FSW=1.2MHZ

1.8VLAW
TDC=3A OCP=6A FSW=1.2MHZ

1.2V
TDC=6A OCP=14A FSW=1MHZ

0.95VALW 实 际 电 压为1.0 5V
在 EC setting 注 意

Security Classification	LC Future Center Secret Data		
Issued Date	2014/02/20	Deciphered Date	2014/02/20

Title: System PMIC

Size	Document Number	Rev
C	CG516	1.0

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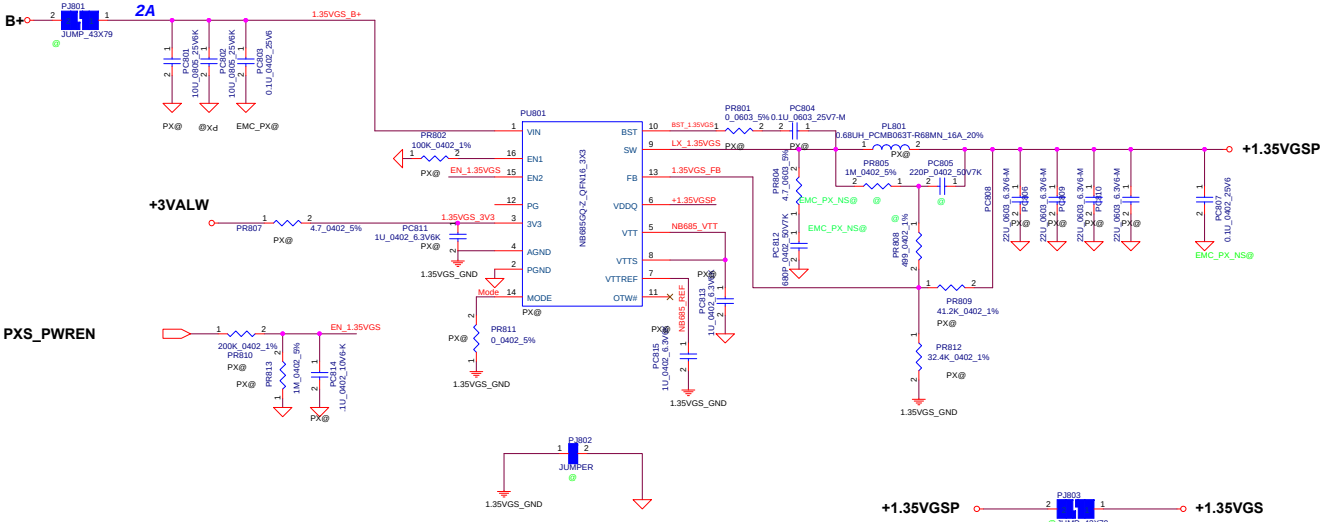

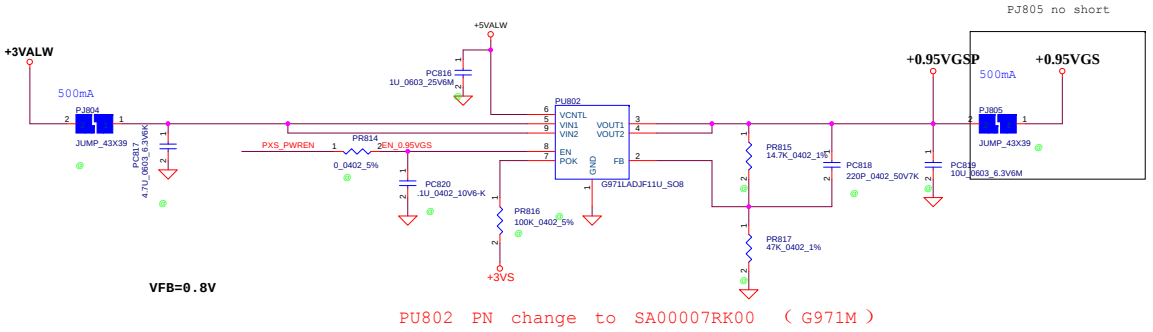

PU802 PN change to SA00007RK00 (G971M)

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

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Title: 1.35VGS

Size	Document Number	Rev
Custom	C6516	1.0

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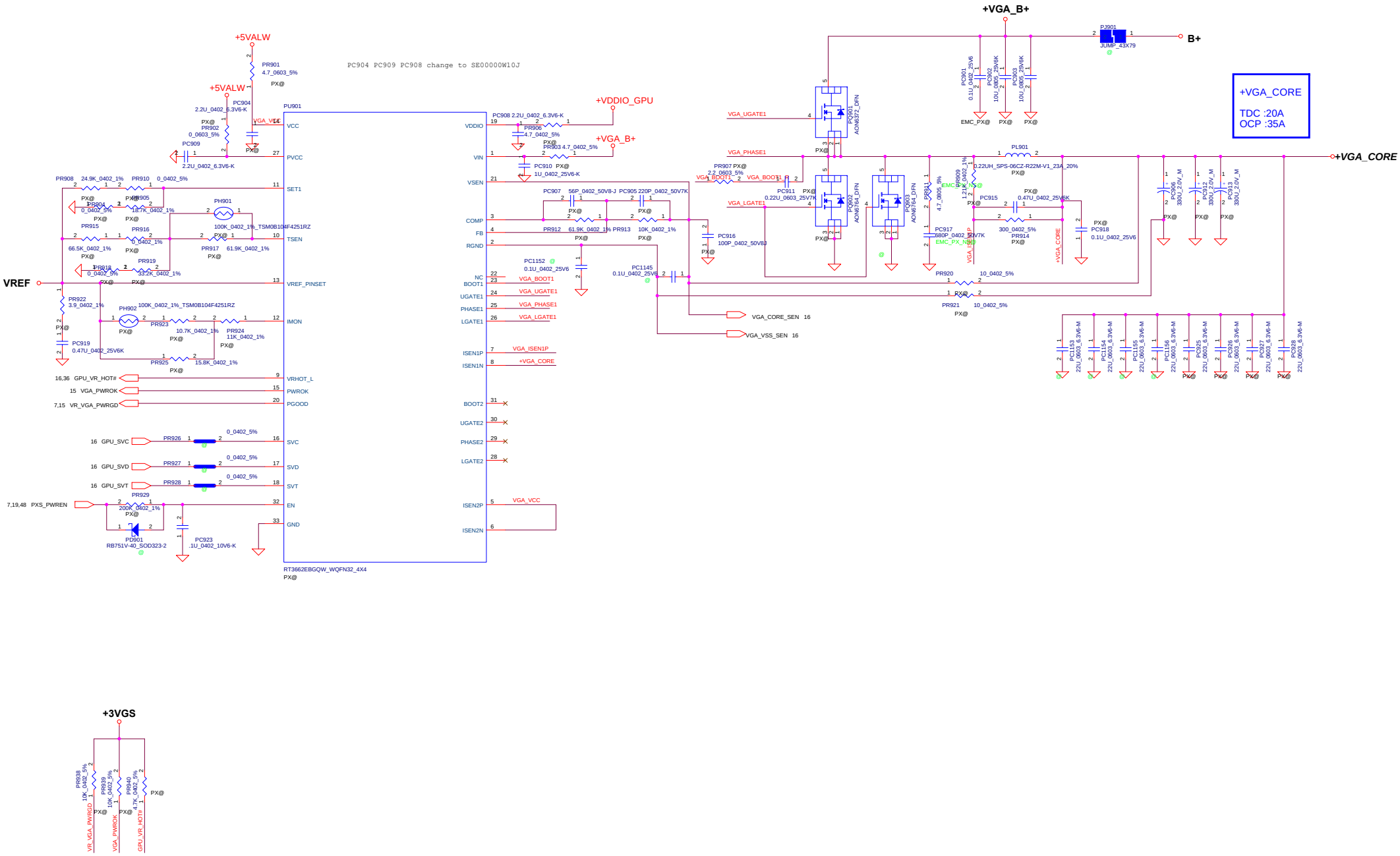
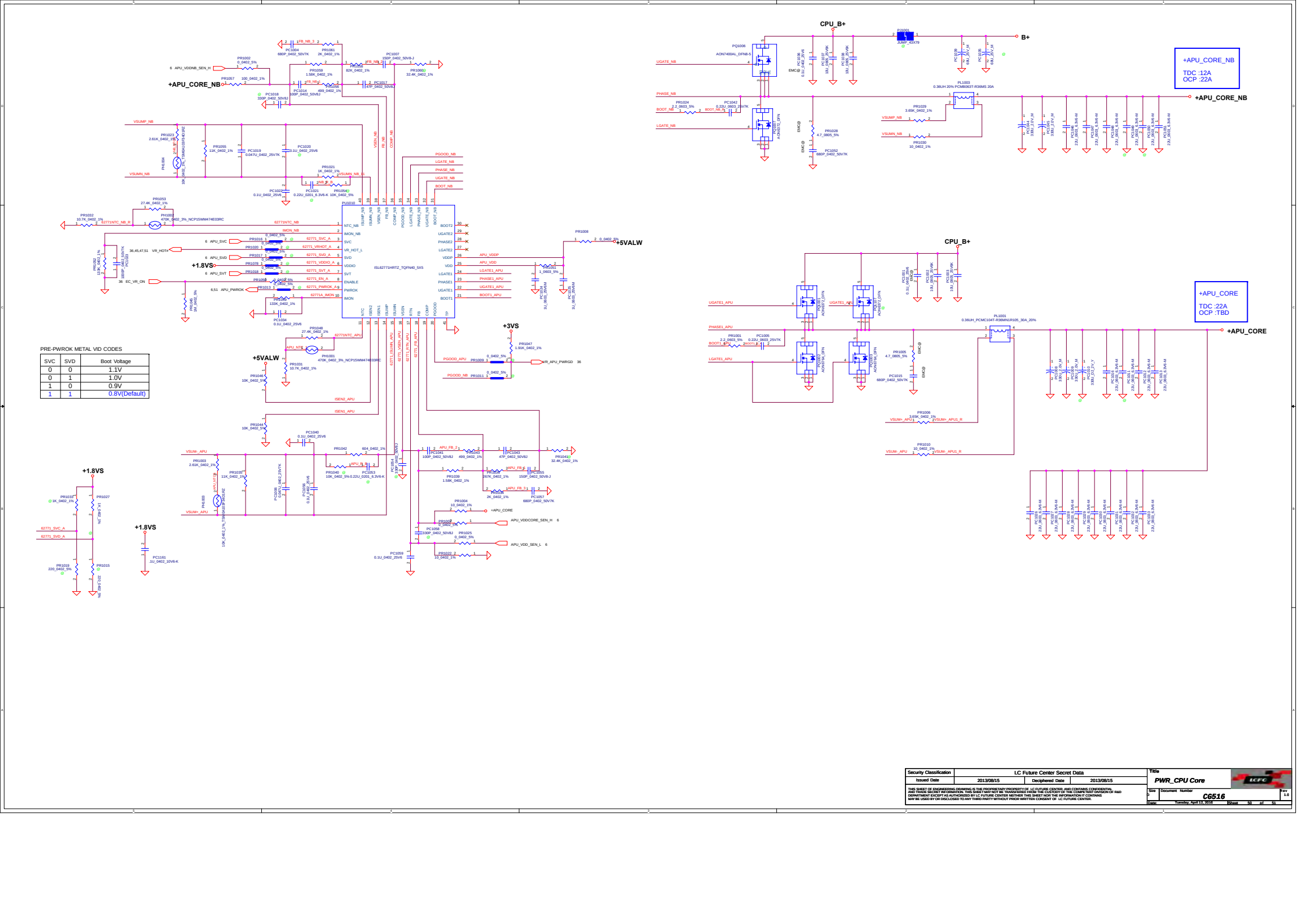


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	+VGA_CORE		
Size	Document Number		Rev
Custom	CG516		1.0
Date:	Tuesday, April 12, 2016	Sheet	49 of 51


+APU_CORE_NB
TDC :12A
OCP :22A
+APU_CORE
TDC :22A
OCP :TBD
CPU_B+
B+
+5VALW
+3VS
+1.8VS
PRE-PWROK METAL VID CODES
SVC SVD Boot Voltage
0 0 1.1V
0 1 1.0V
1 0 0.9V
1 1 0.8V(Default)
ISL62771HRTZ_TQFN40_5X5
Security Classification
LC Future Center Secret Data
Issued Date 2013/08/15
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PWR_CPU Core
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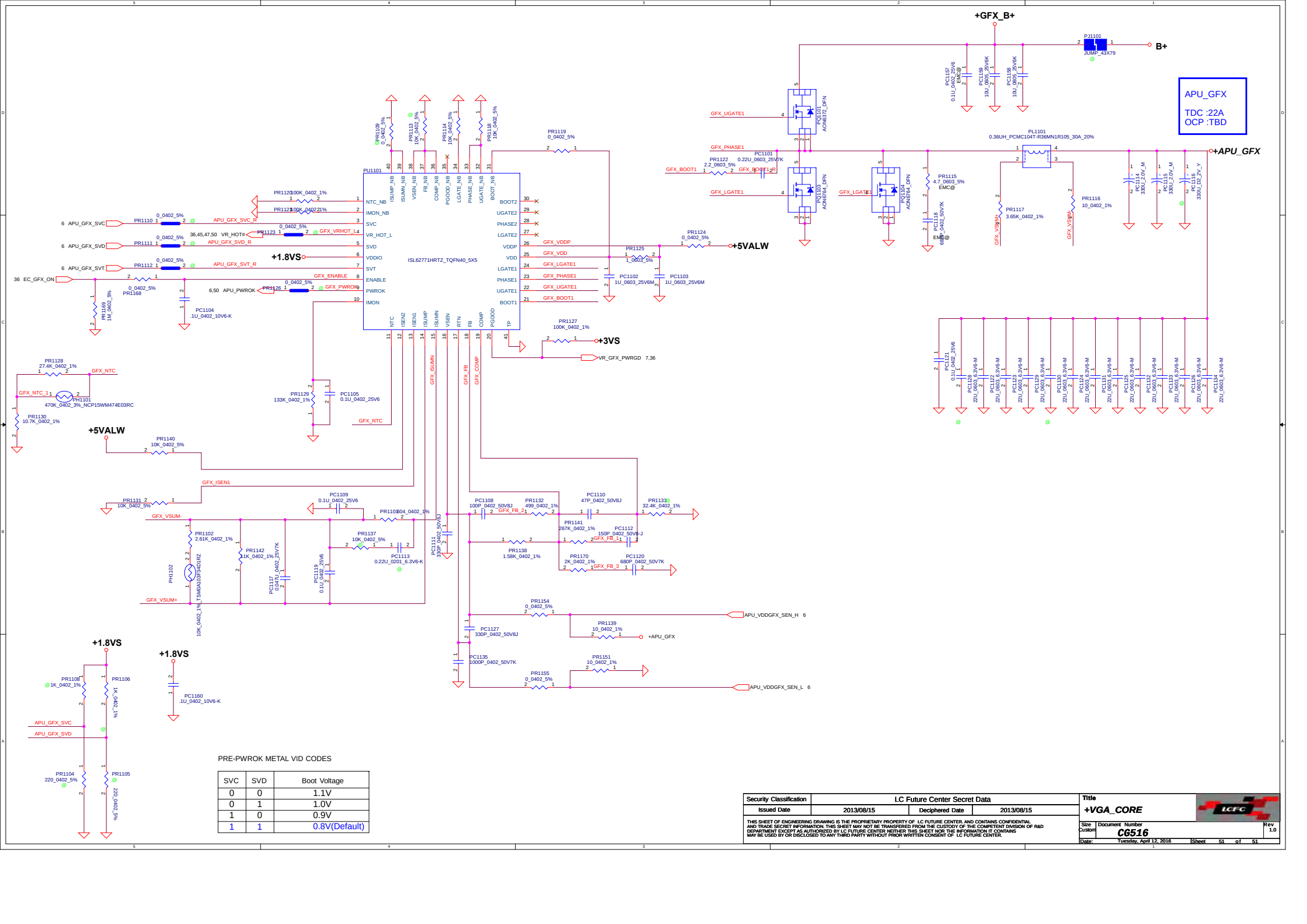
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GFX_BOOT1
GFX_LGATE1
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Document Number
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