LCFC Confidential

CG413/CG513 MB Schematics Document

Intel Skylake-U22/Kabylake-U22 with DDR4 + Nvidia N16S-GTR/N16V-GMR1 GPU

2016-06-12

REV:1.0

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Title: Cover Page

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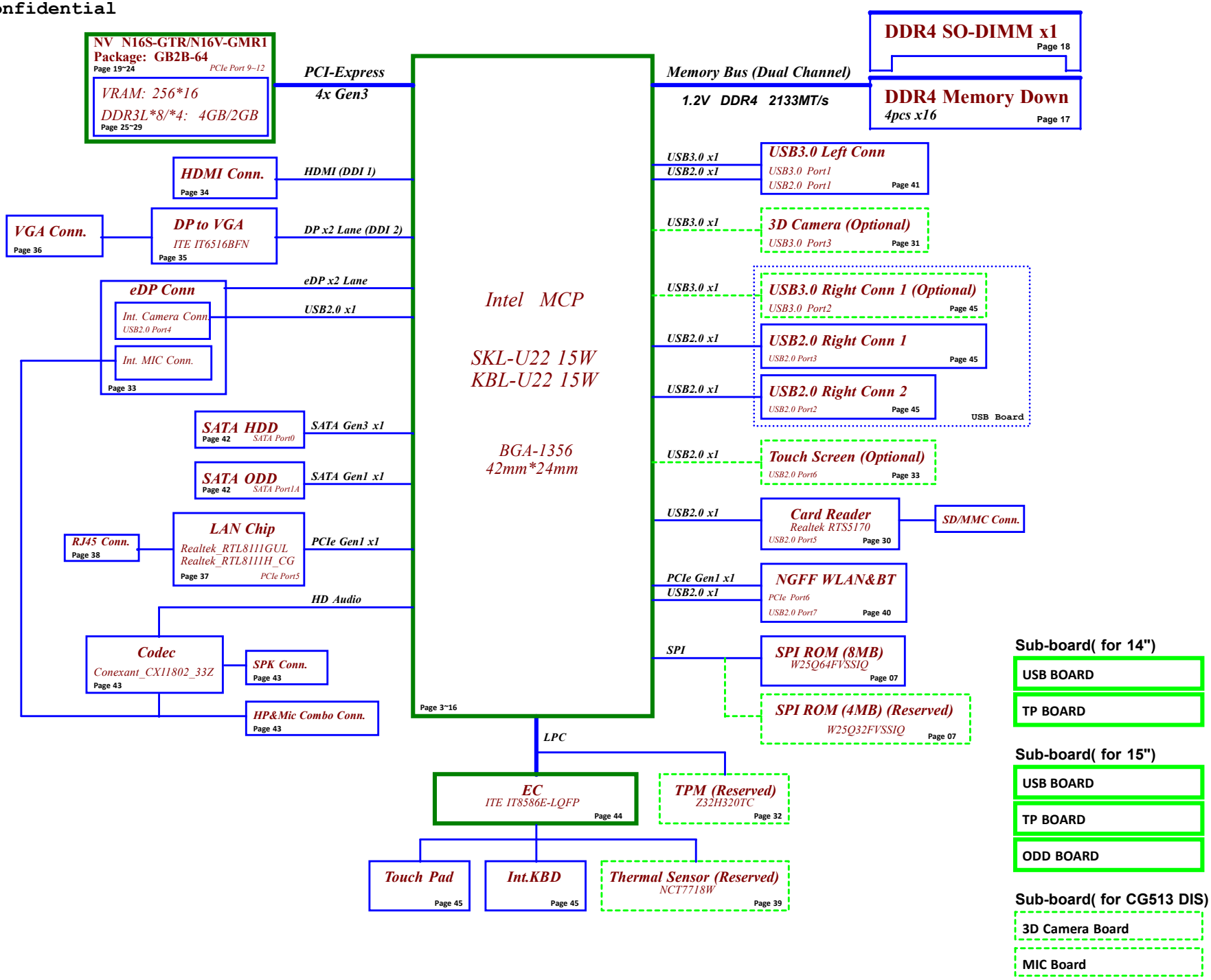

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Title: **Block Diagram**

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn Left
	2	USB3.0 Conn Right(optional)
	3	3D Camera(optional)
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn Left
	2	USB2.0 Conn1 Right
	3	USB2.0 Conn2 Right
	4	Camera
	5	Cardreader
	6	Touch Panel
	7	Bluetooth
	8	NC
	9	NC
	10	NC
PCIE	1	NC
	2	NC
	3	NC
	4	NC
	5	LAN
	6	WLAN
	7	used as SATA
	8	used as SATA
	9~12 X4 PCIE	DGPU
SATA	0	HDD
	1A	ODD
	1B	used as PCIE
	2	used as PCIE

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
14or15@	For 14" or 15" part
14or17@	For 14" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
NTS@	For nu-touch part
PX@	For PX part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek_SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAN rank part
DUALRANK@	For dual VRAN rank part
TS@	For touch screen part
TPM@	For TPM part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

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Title: **Notes List**

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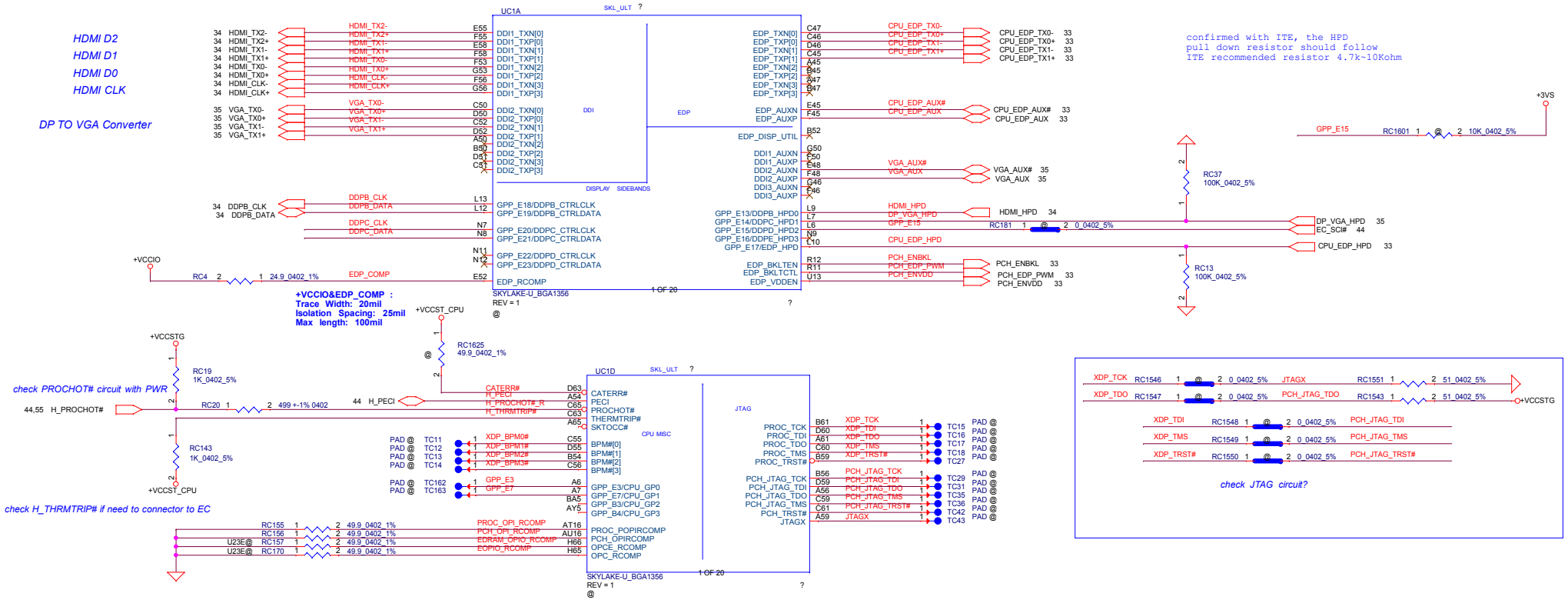

DDP*_CTRLDATA strapping sampled on the rising edge of PWROK

Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC

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Title: **MCP (DDI,EDP)**

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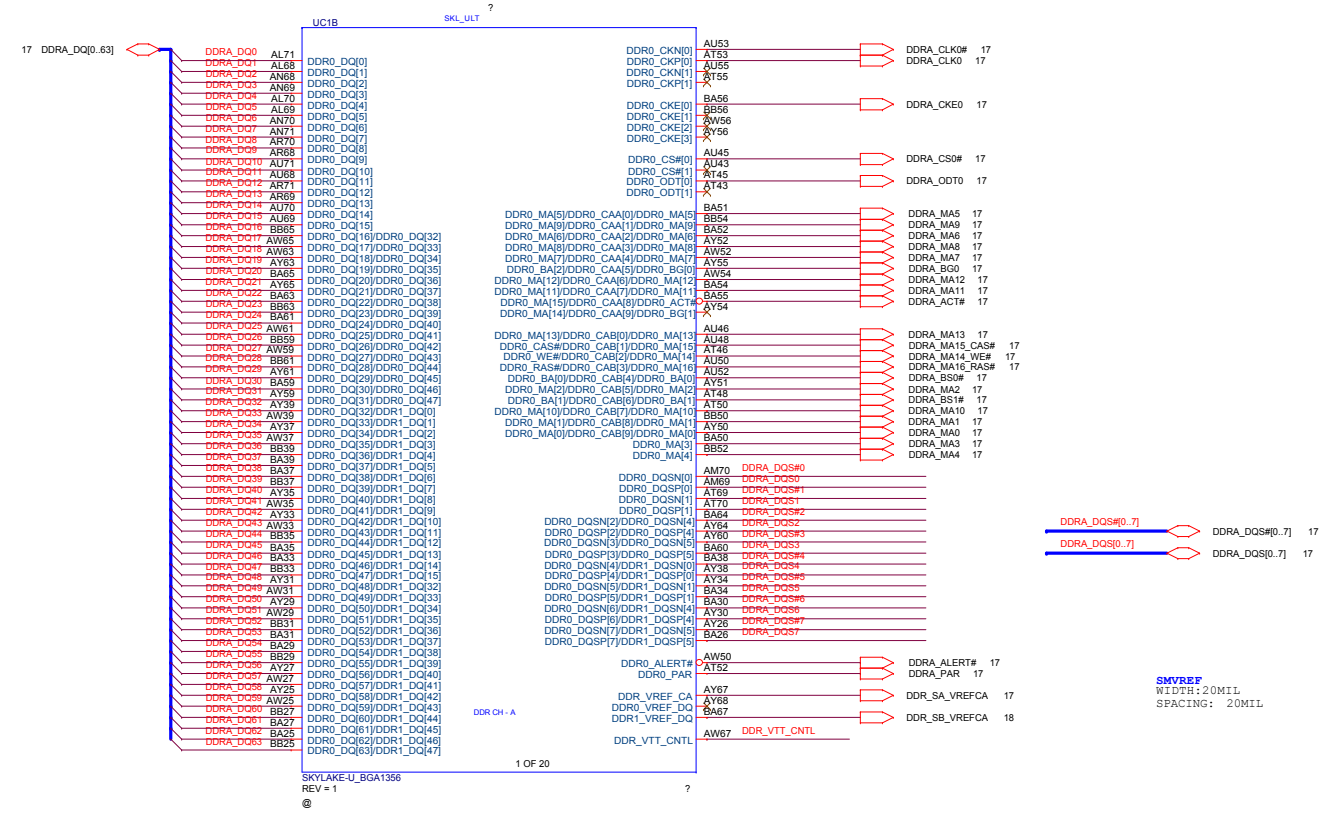

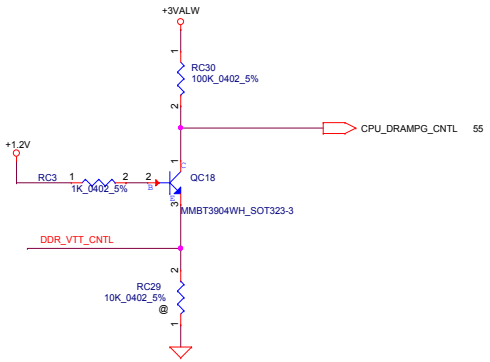

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Title: **MCP (DDR4)**

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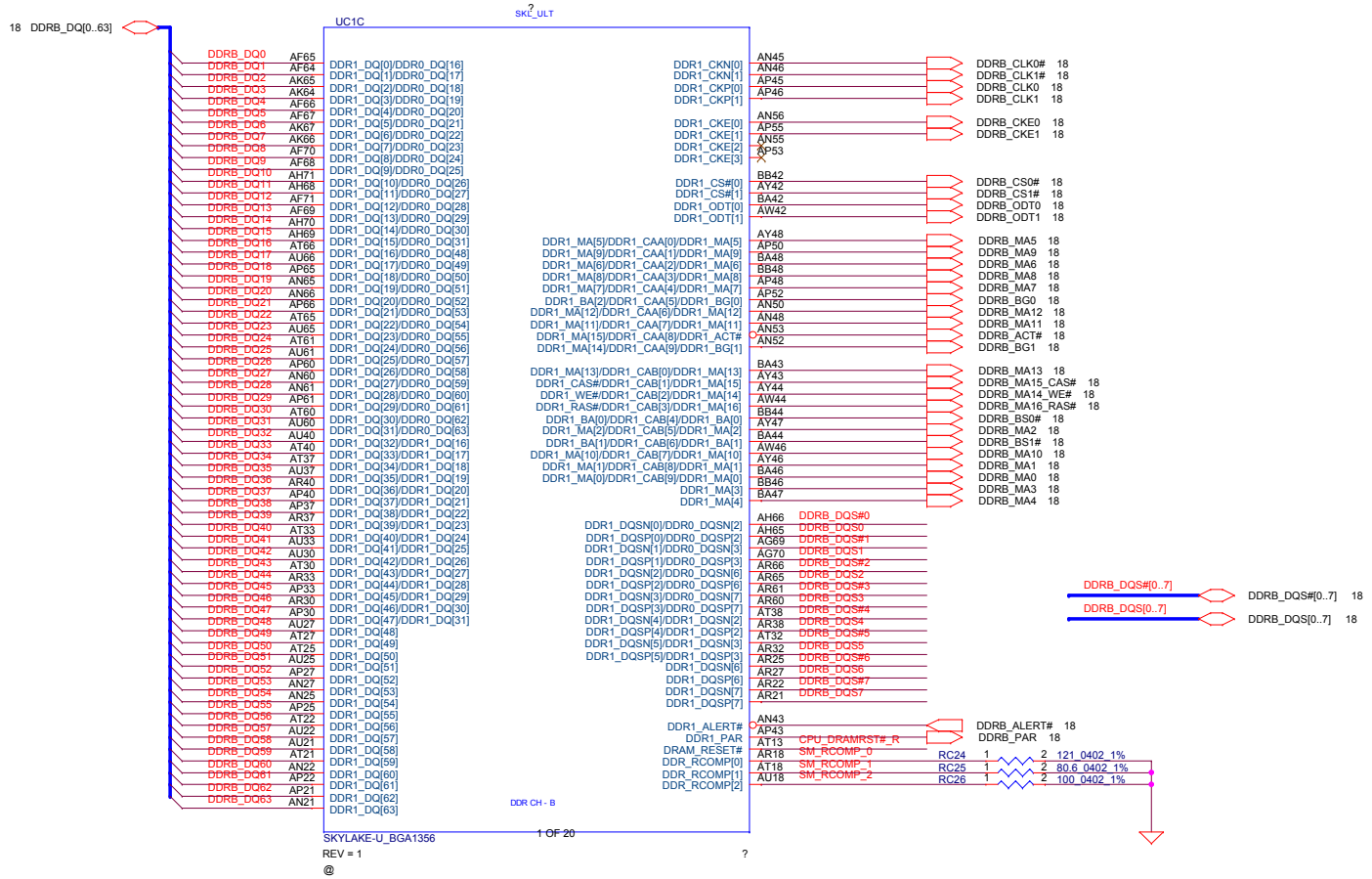

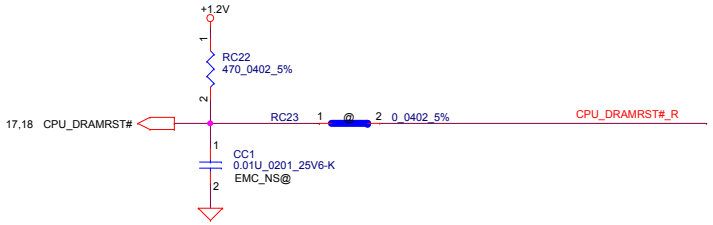

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Title: **MCP (DDR4)**

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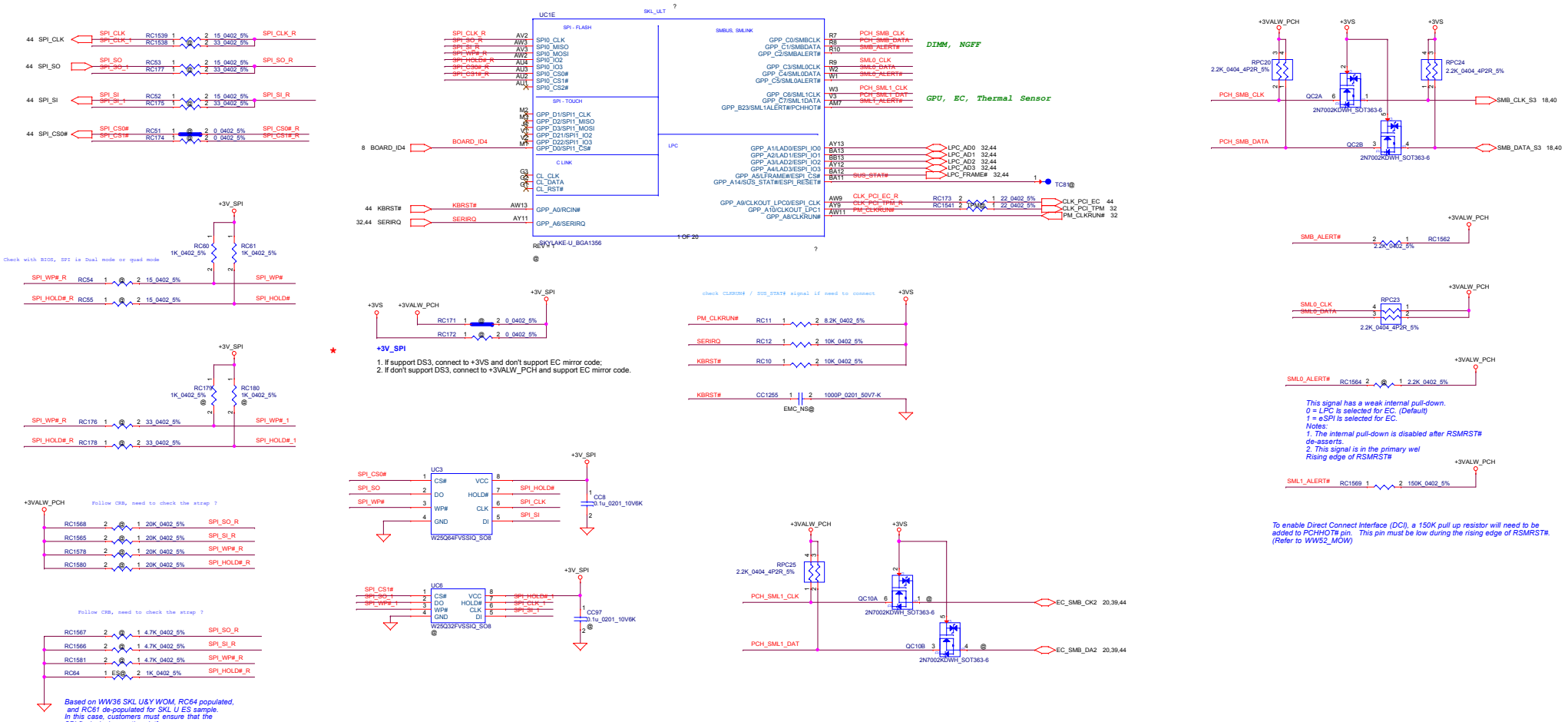

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Title: MCP (MISC,JTAG,SPI,LPC,

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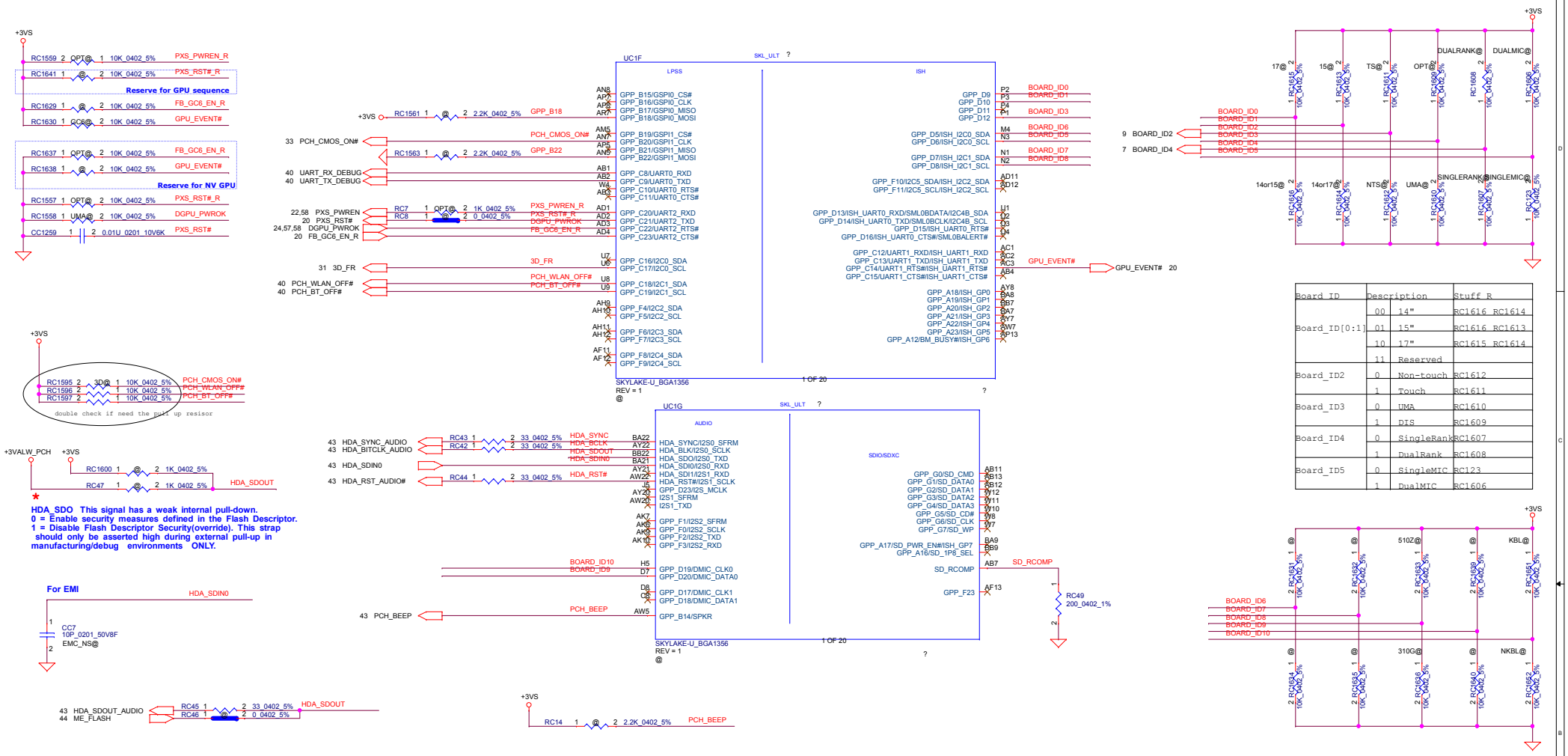

Board ID	Description		Stuff R
Board_ID[0:1]	00	14"	RC1616 RC1614
	01	15"	RC1616 RC1613
	10	17"	RC1615 RC1614
	11	Reserved	
Board_ID2	0	Non-touch	RC1612
	1	Touch	RC1611
Board_ID3	0	UMA	RC1610
	1	DIS	RC1609
Board_ID4	0	SingleRank	RC1607
	1	DualRank	RC1608
Board_ID5	0	SingleMIC	RC123
	1	DualMIC	RC1606

Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable " Top Swap" mode. (Default) ★ 1 = Enable " Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable " No Reboot" mode. (Default) ★ 1 = Enable " No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) 1 = LPC ★	0	Rising edge of PCH_PWROK

Board ID	Description		Stuff R
Board_ID [6,7,9]	000	Samsung 8Gb 2133 MT/s	RC1634 RC1635 RC1640
	010	Hynix 8Gb 2133 MT/s	RC1634 RC1632 RC1640
	100	Micron 8Gb 2133 MT/s	RC1631 RC1635 RC1640
	110	Reserved	RC1631 RC1632 RC1640
	001	Samsung 8Gb 2400 MT/s	RC1634 RC1635 RC1639
	011	Hynix 8Gb 2400 MT/s	RC1634 RC1632 RC1639
	101	Micron 8Gb 2400 MT/s	RC1631 RC1635 RC1639
	111	Reserved	RC1631 RC1632 RC1639
Board_ID8	0	310G	RC1636
	1	510Z	RC1633
Board_ID10	0	Non-KBL	RC1652
	1	KBL	RC1651

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Title: MCP (LPSS,ISH,AUDIO,SDI

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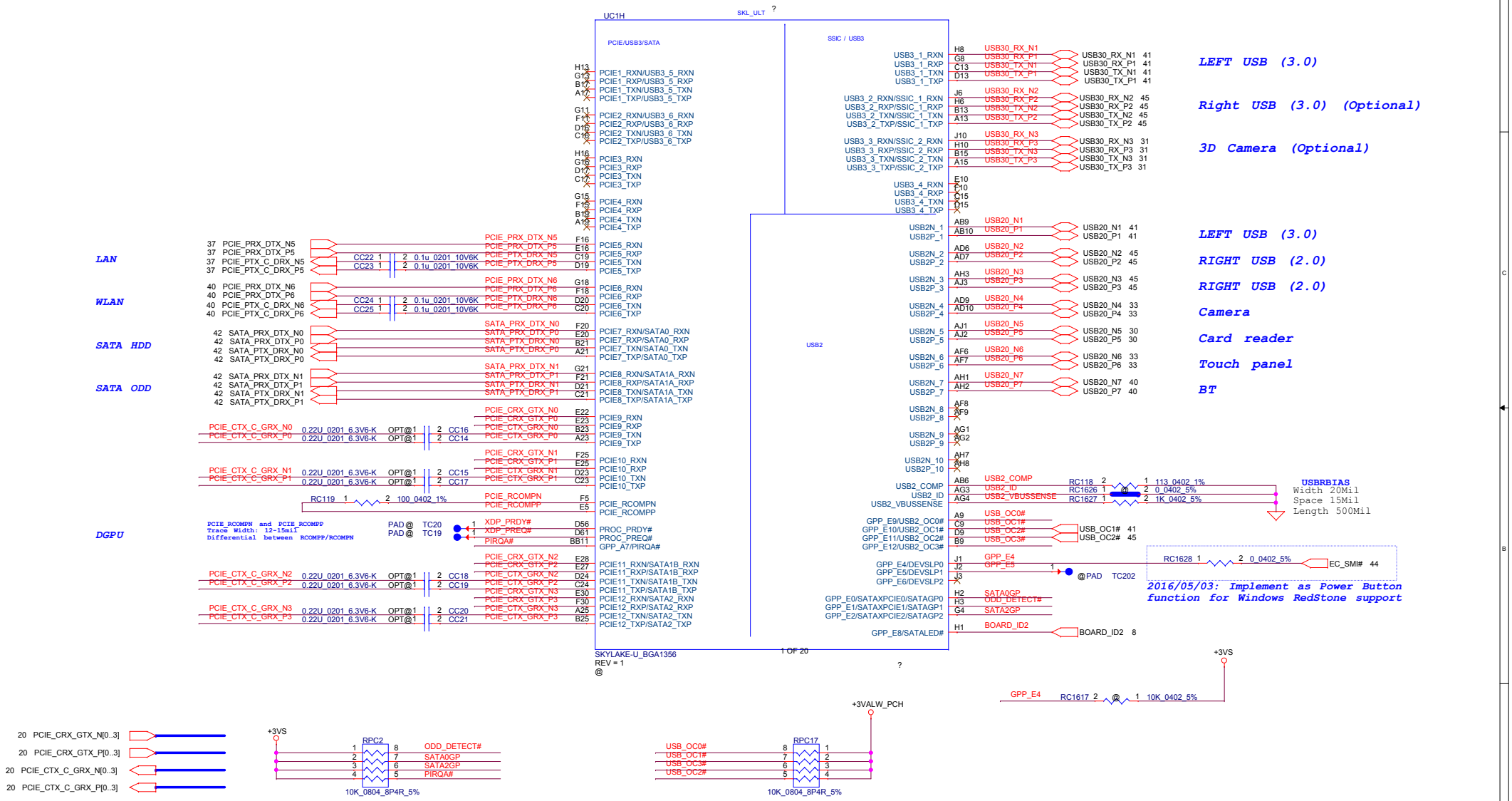

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Title: MCP (PCIE,SATA,USB3,US

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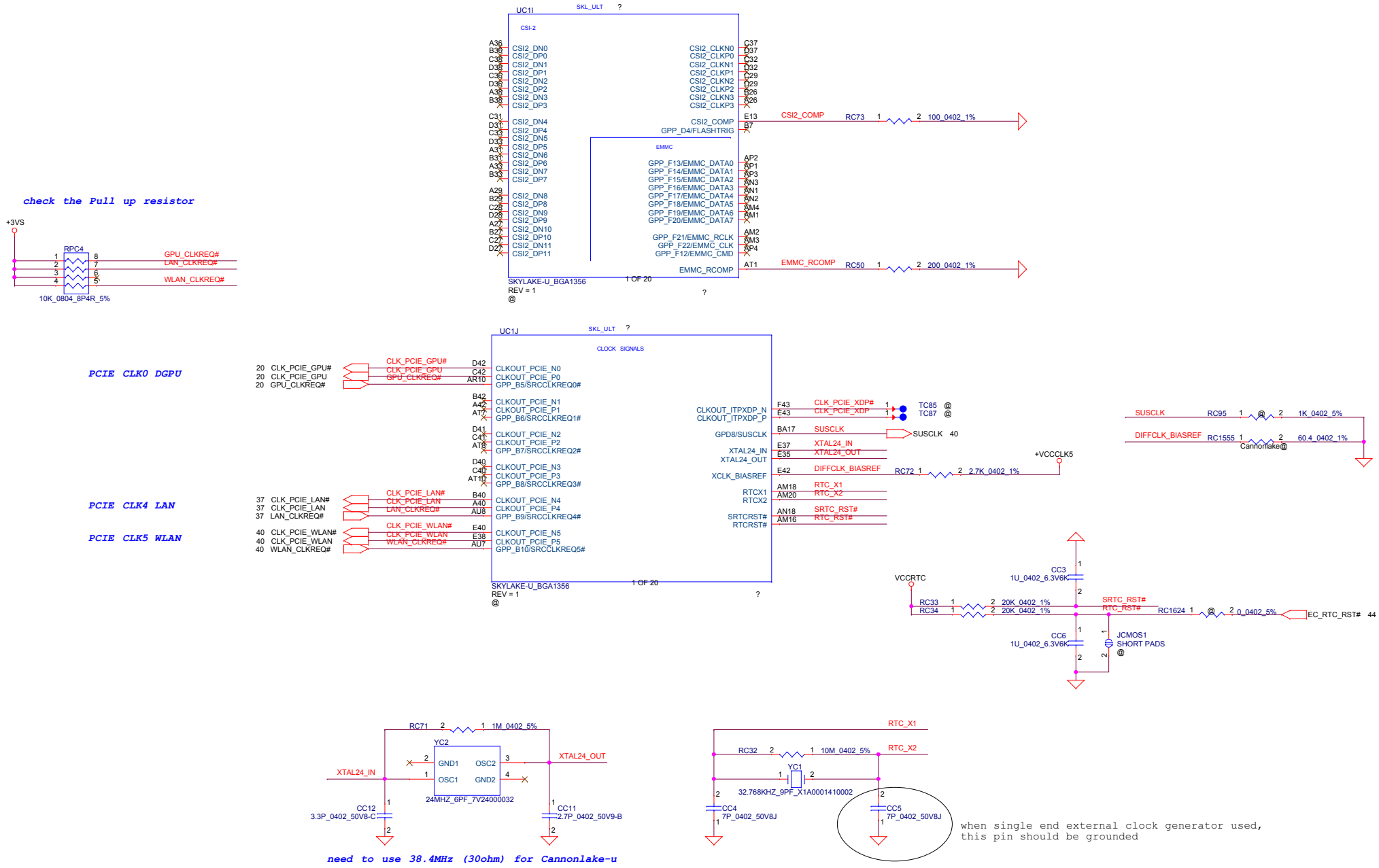

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Title: MCP (CSI2,EMMC,CLOCK)

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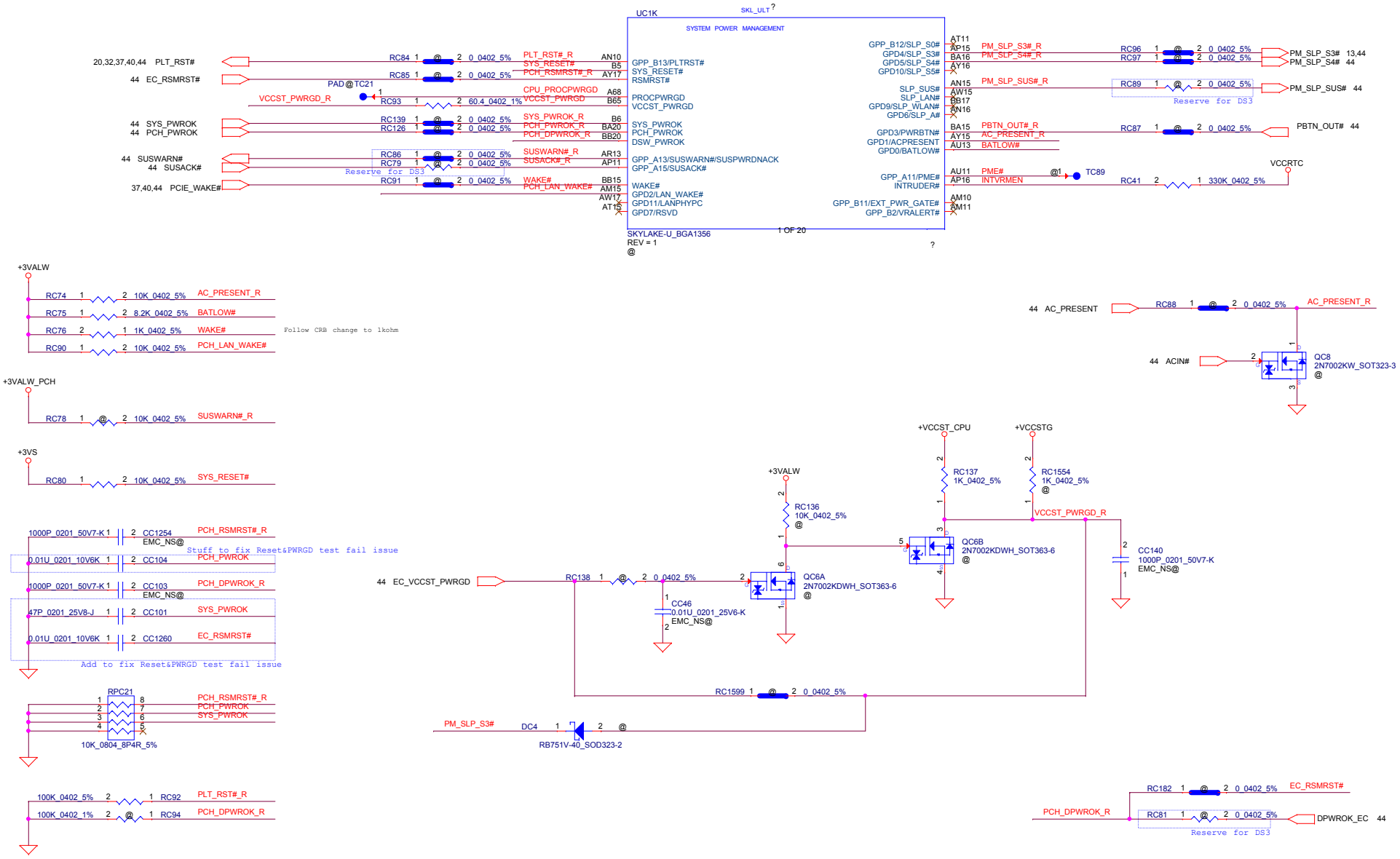

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Title: MCP (SYSTEM PWR MANAGEMENT)

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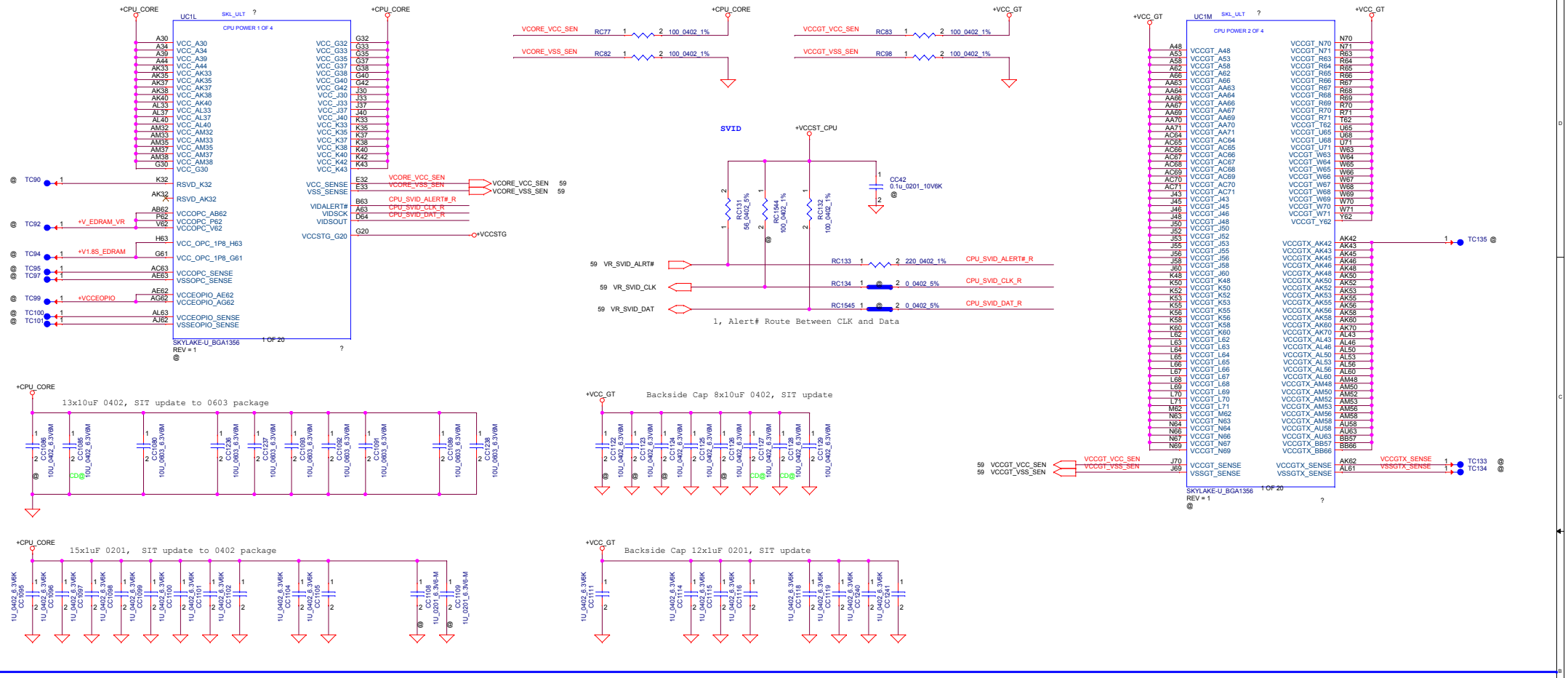

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Title: **MCP (CPU PWR1)**

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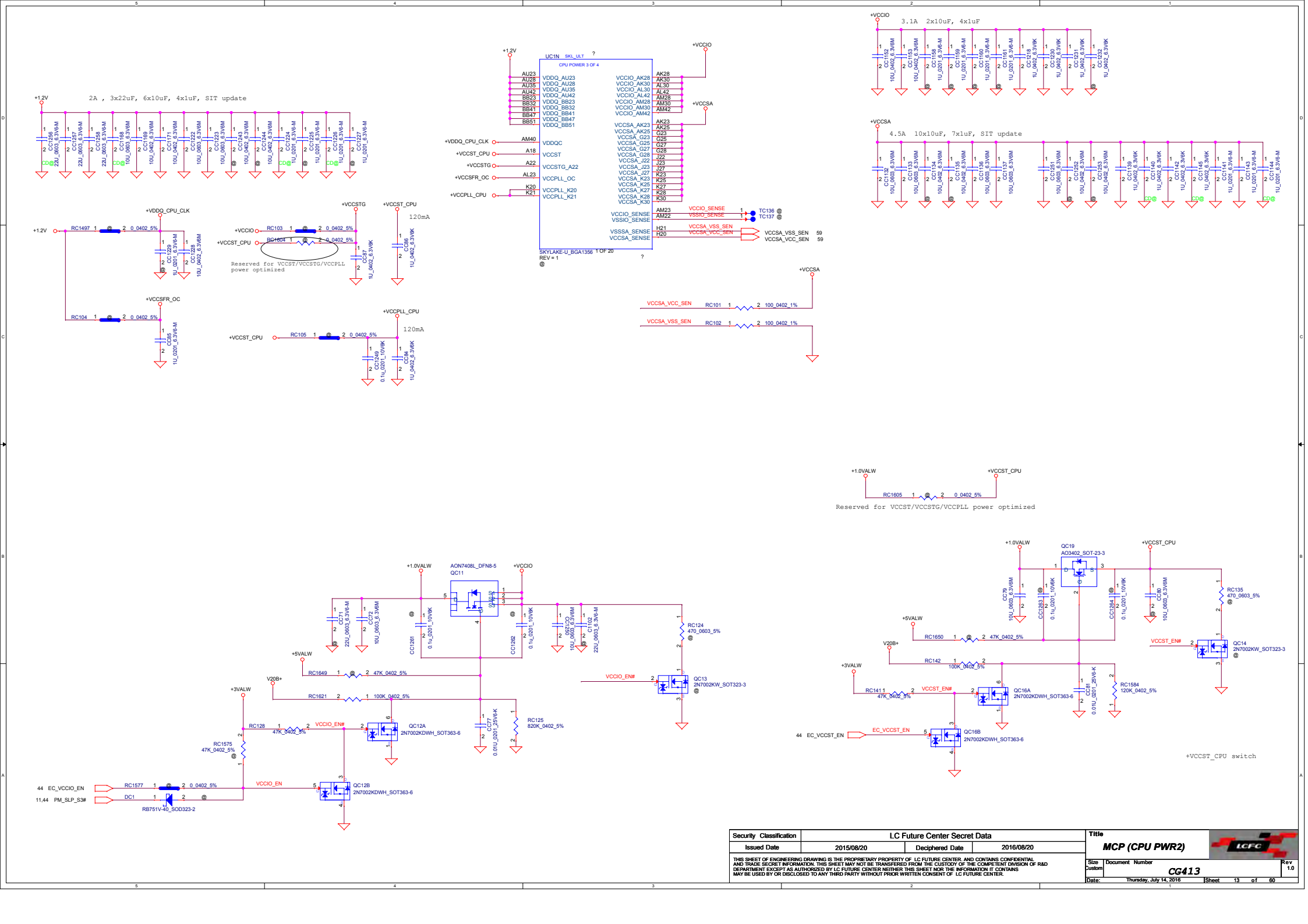

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Title: **MCP (CPU PWR2)**

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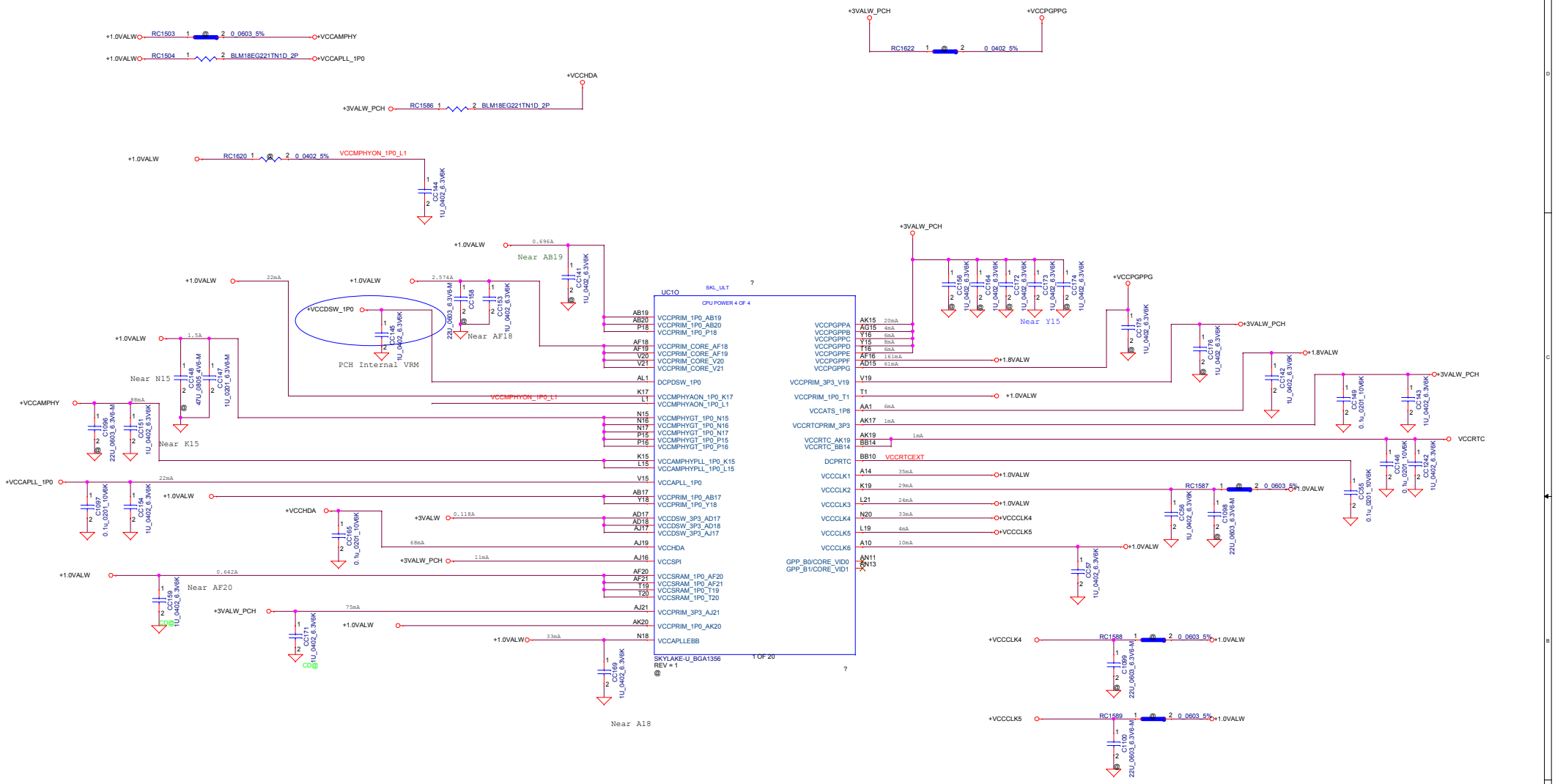

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Title: **MCP (PCH PWR)**

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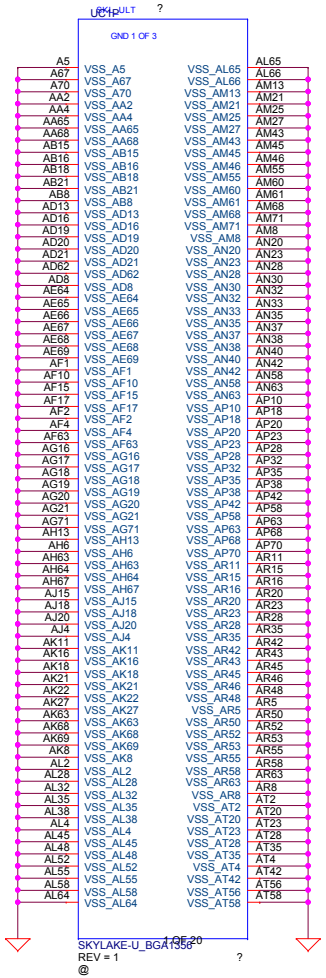

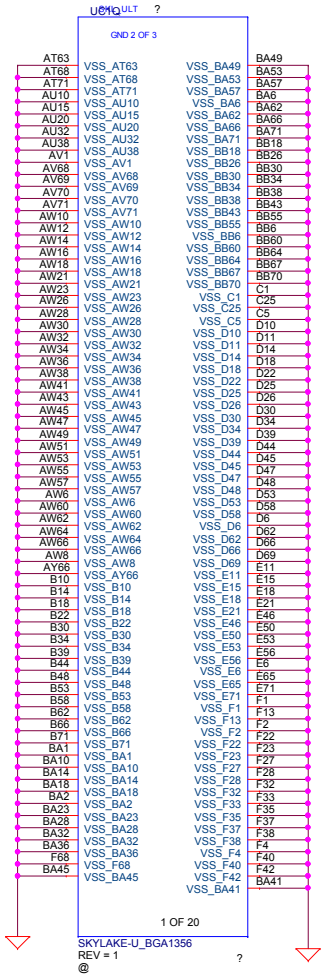

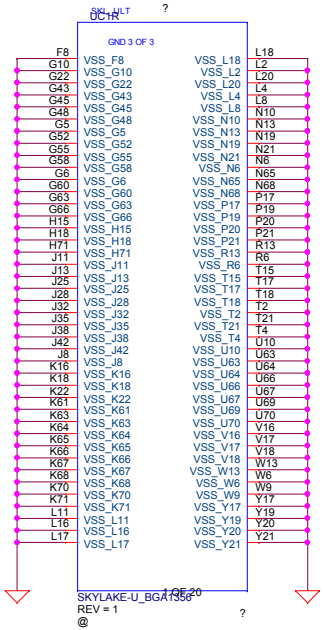

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Title

MCP (VSS)

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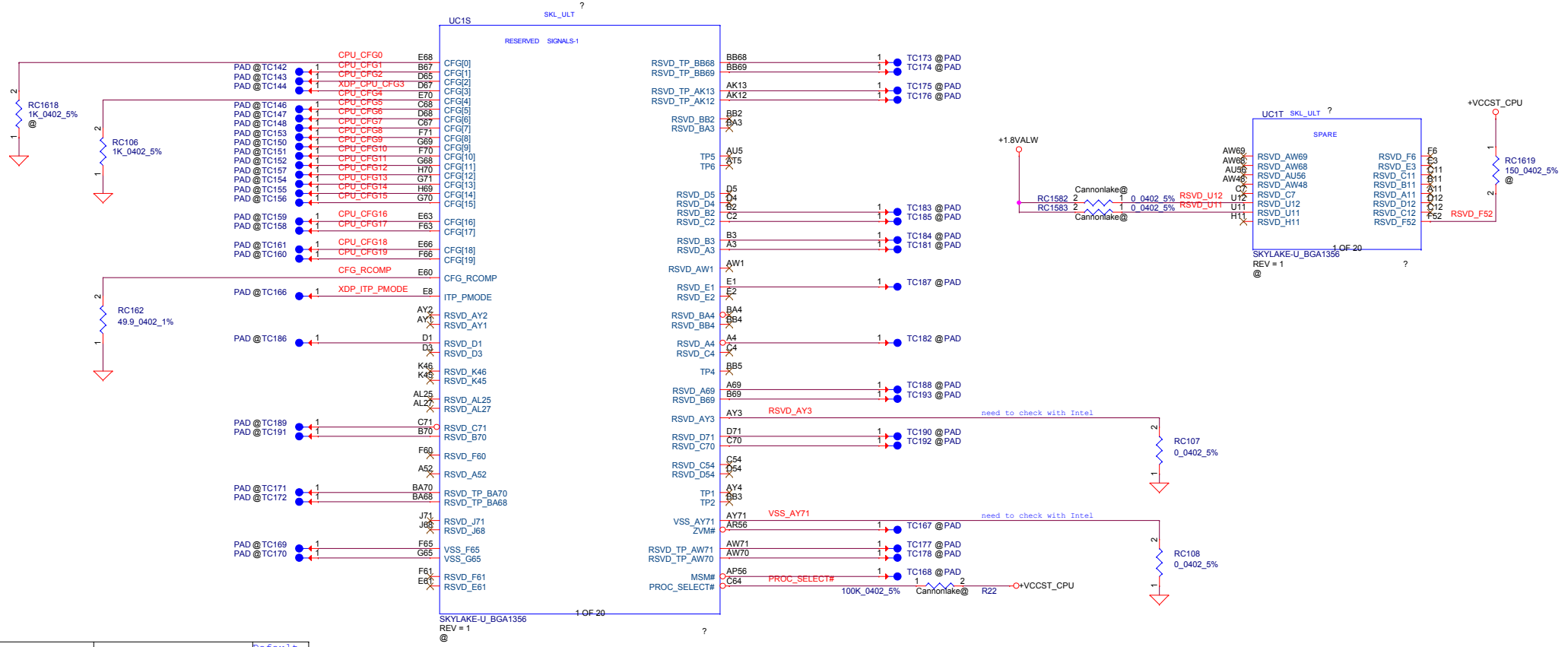

Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	– 1 = eDP Disabled – 0 = eDP Enabled ★	1

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Title: **MCP (CFG,RESERVED)**

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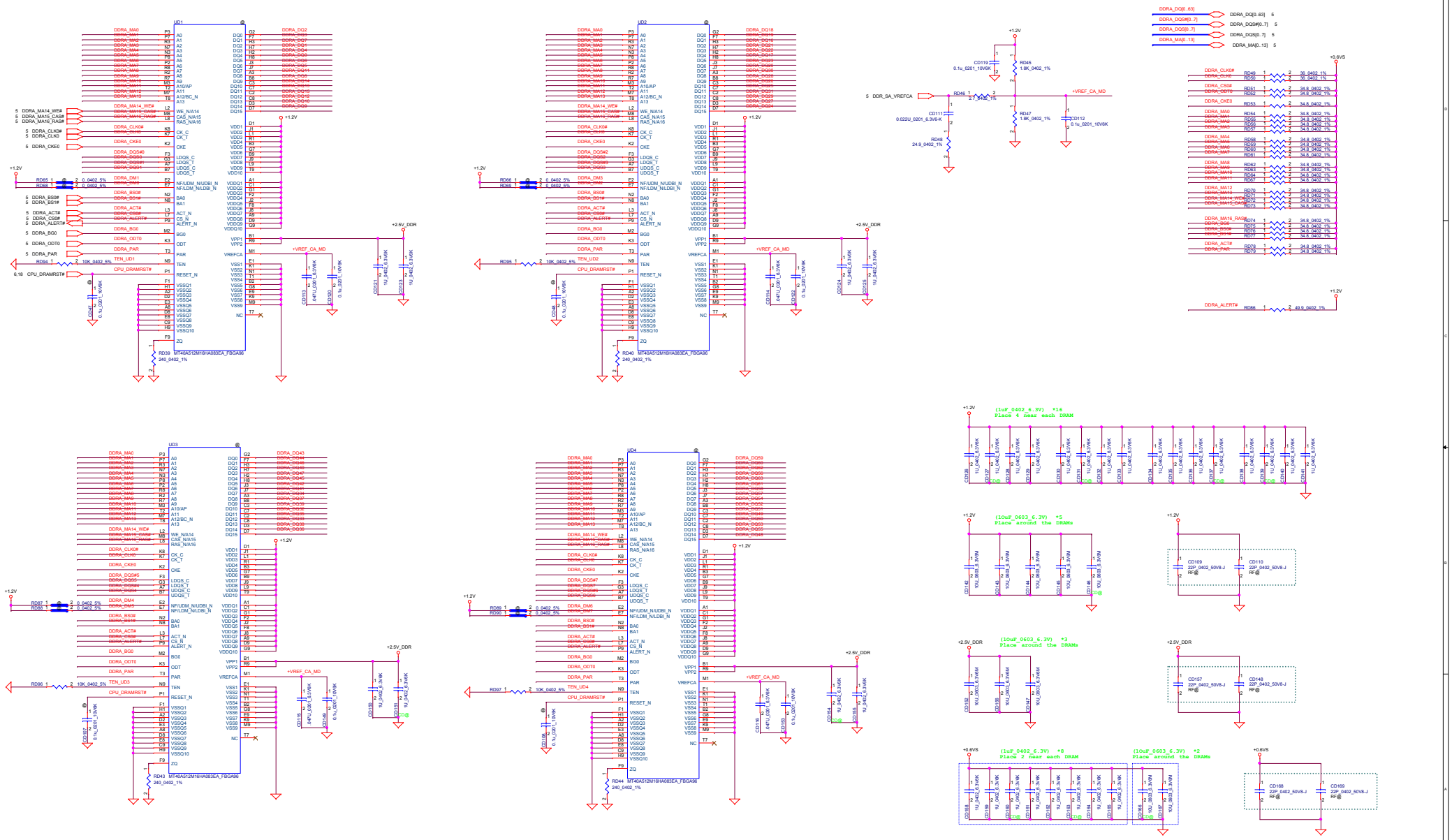

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Title: **DDR4 Memory Down**

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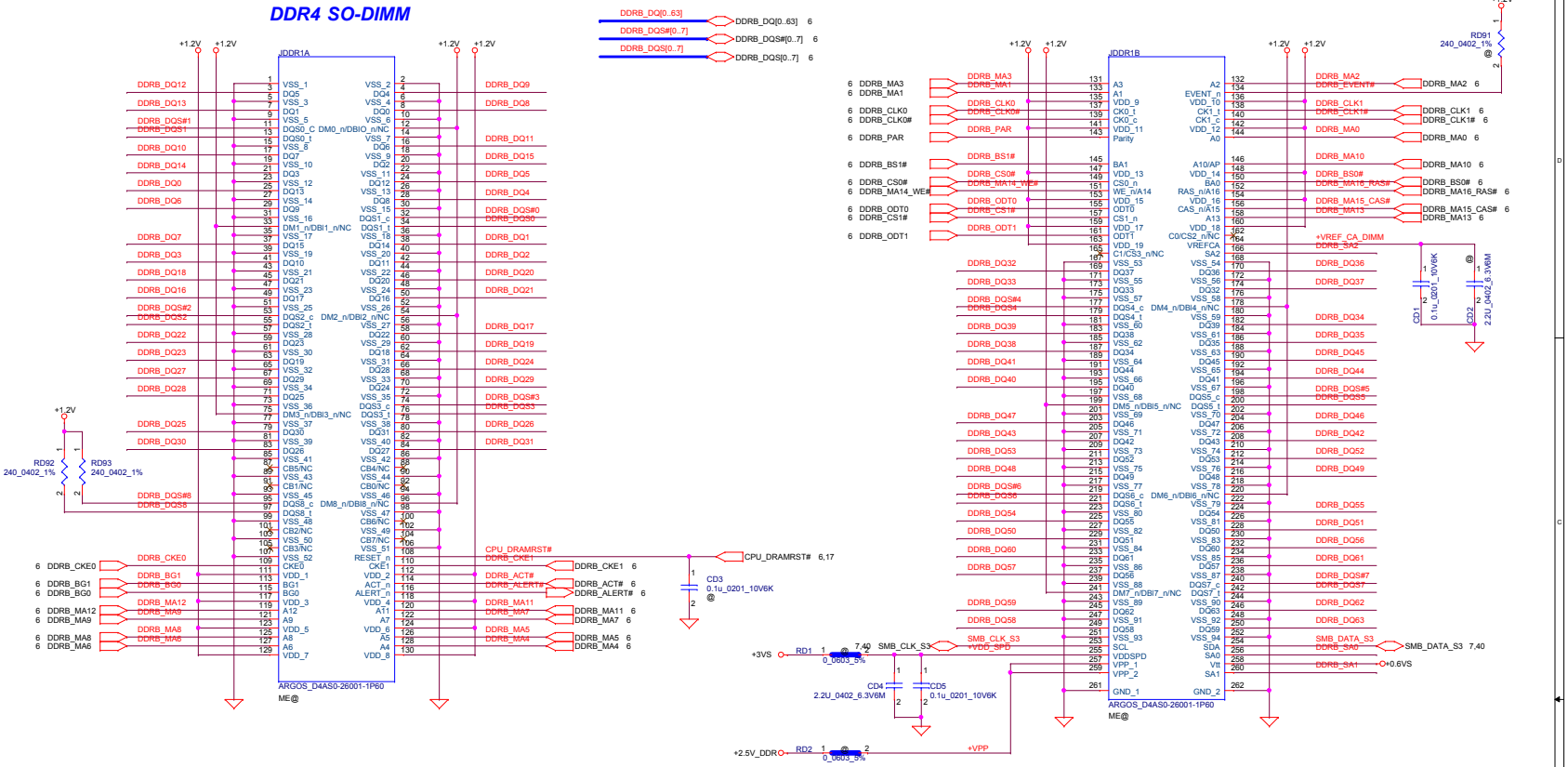
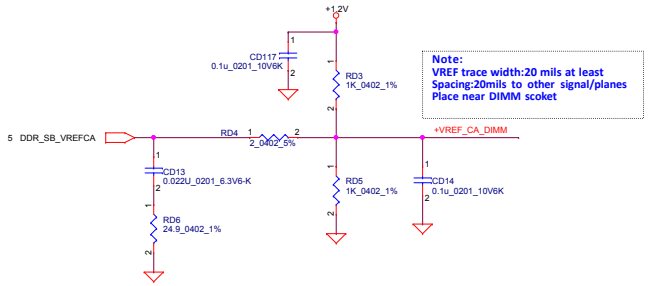
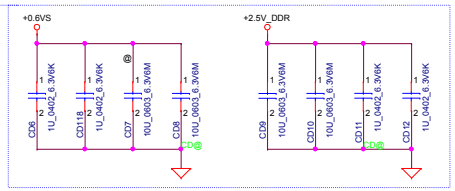
DDR4 SO-DIMM

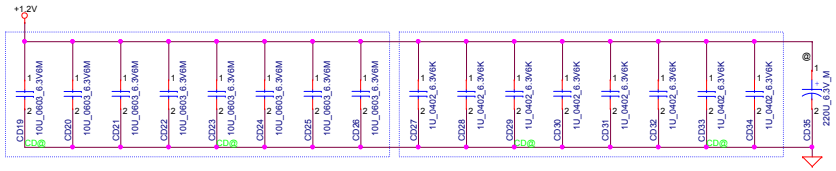


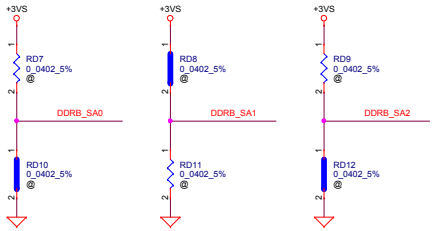


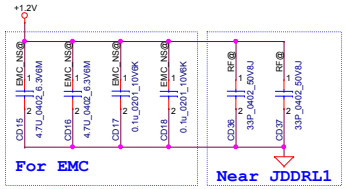
Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM scoket

Layout Note:
Place near DIMM









SPD Address = 2H

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Title: **DDR4 SO-DIMM**

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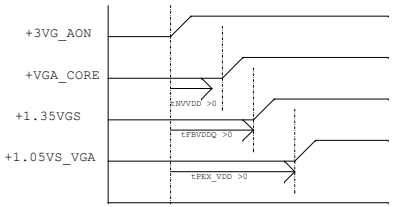
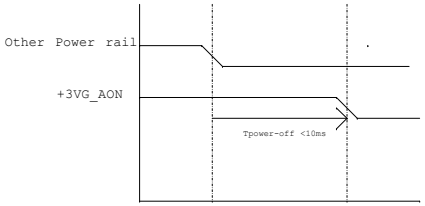
N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

N15V-GM Power Sequence

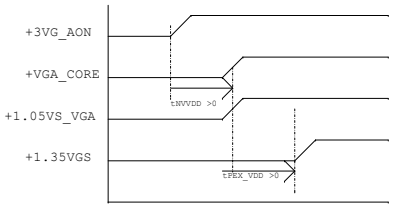


1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

N15S-GT Power Sequence



1. all power rail ramp up time should be larger than 40us

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)			I/O and PLLVDD (1.05V)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)		(mA)	(W)	(mA)	(W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD		TBD	TBD	TBD	TBD

N15x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

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Title: VGA Notes List

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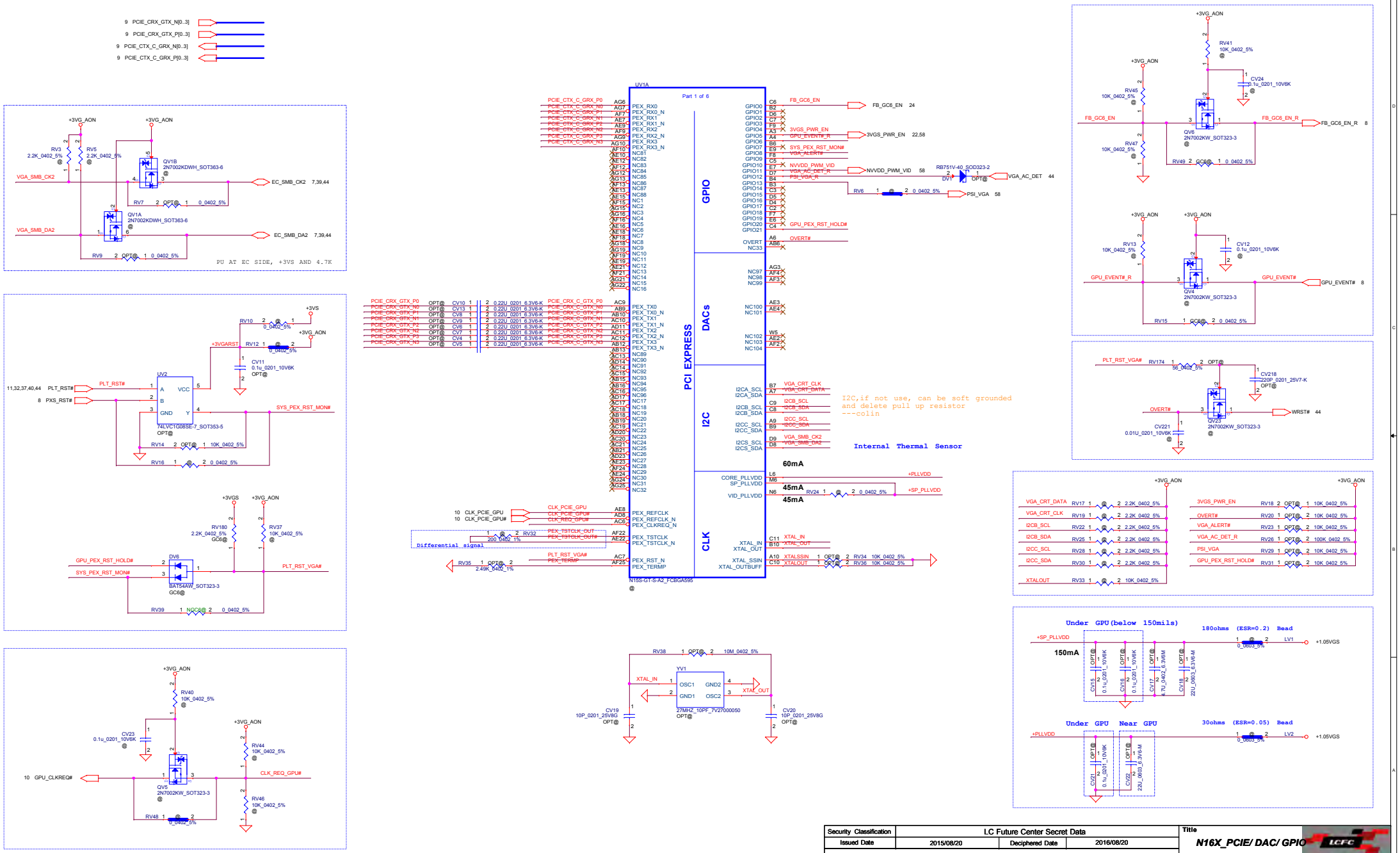

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Title: N16X_PCIE/ DAC/ GPIO

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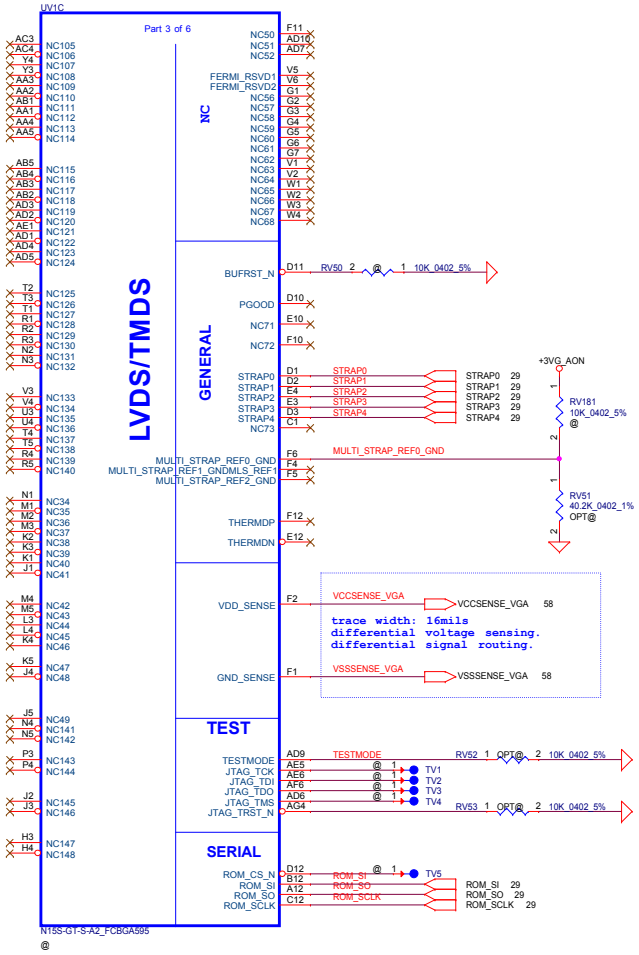

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Title: N16X_LVDS/ HDMI/ THERM

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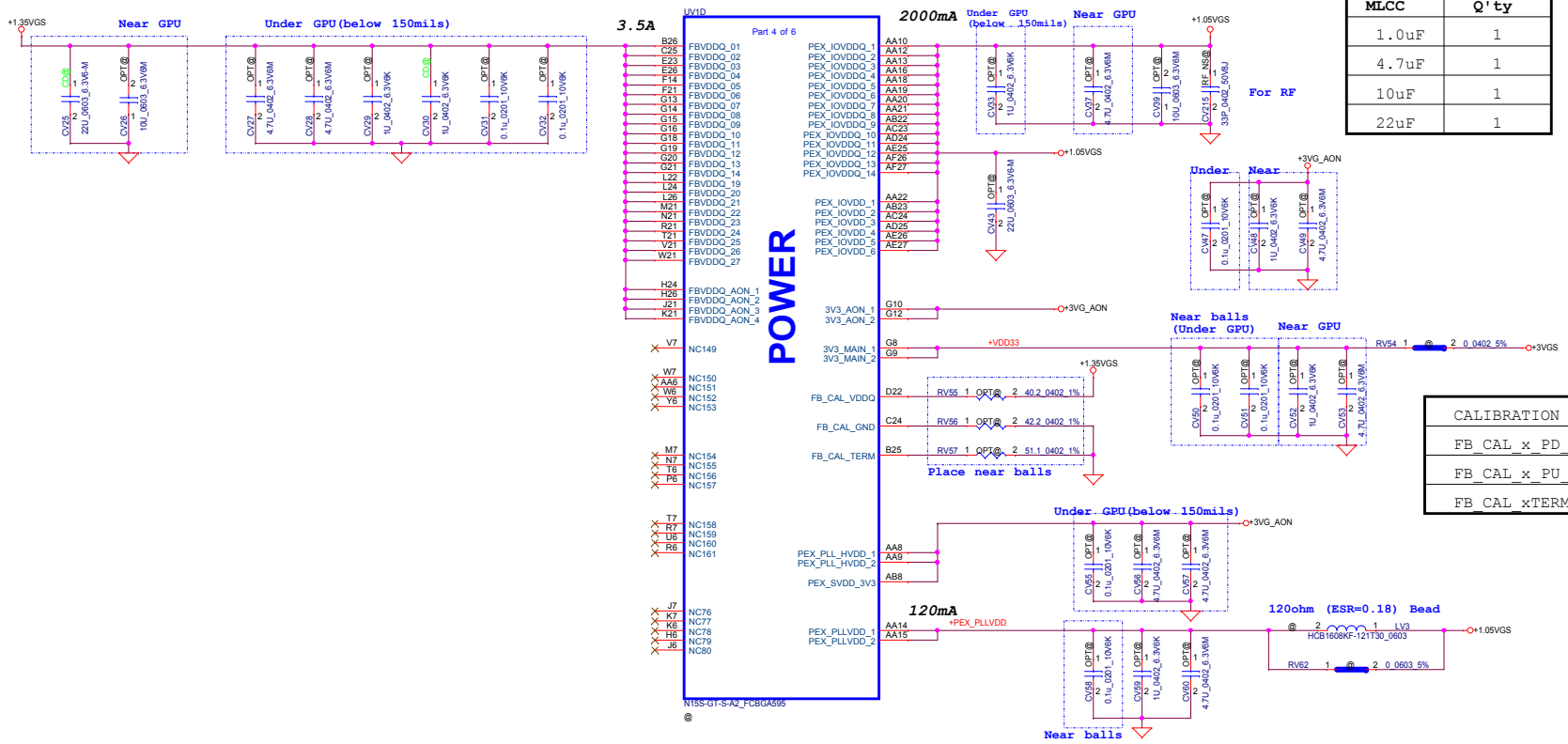
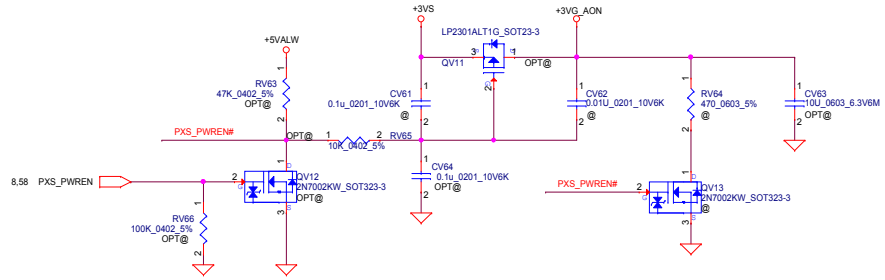


PEX_IOVVDD/Q Decouling

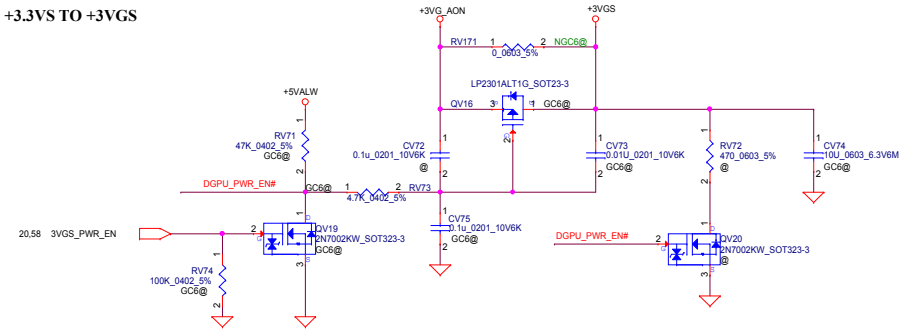
MLCC	Q'ty
1.0uF	1
4.7uF	1
10uF	1
22uF	1

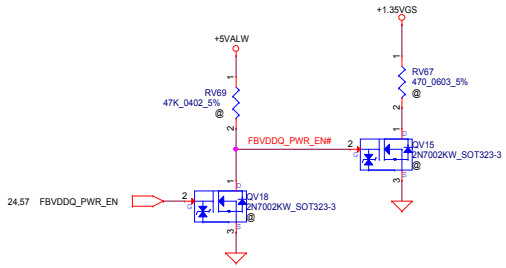
CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

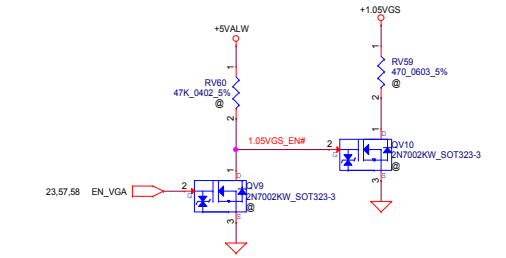
+3.3VS TO +3VG_AON



+3.3VS TO +3VGS







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Title: **N16X_Power**

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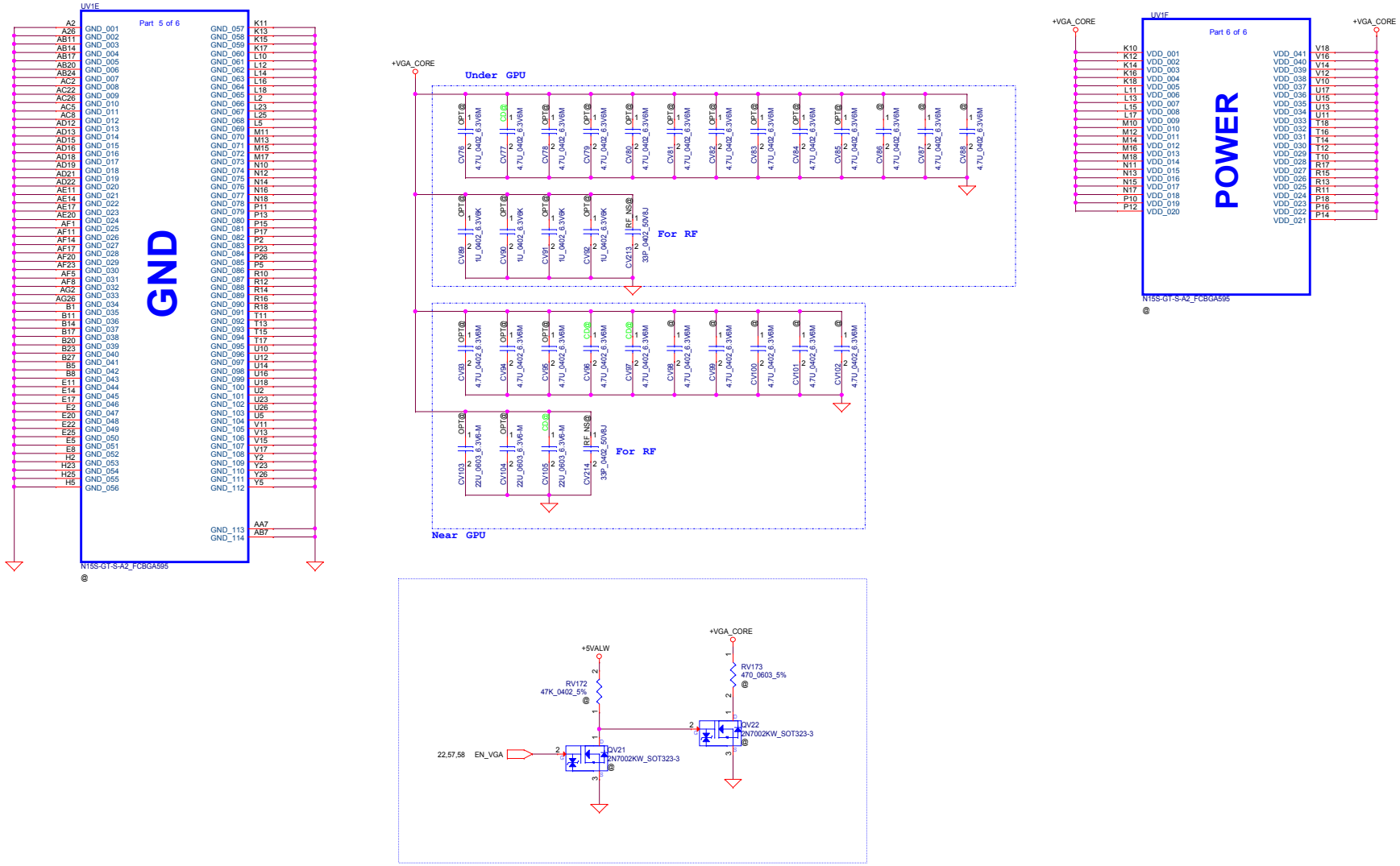

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Title: N16X_+VGA CORE, GND

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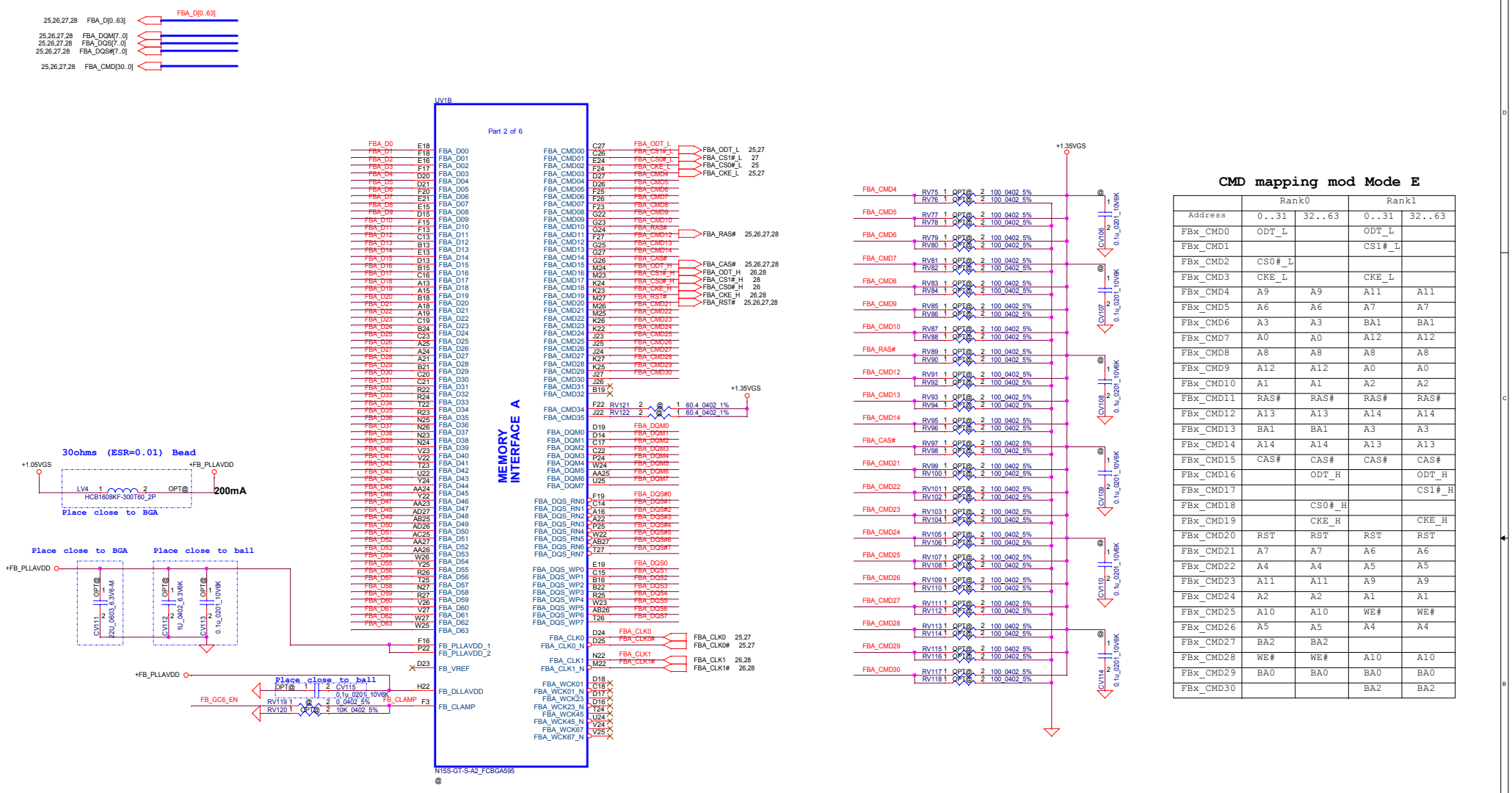
Date: Thursday, July 14, 2016 | Sheet 23 of 60



CMD mapping mod Mode E

	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2

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Title: **N16X_MEM Interface**

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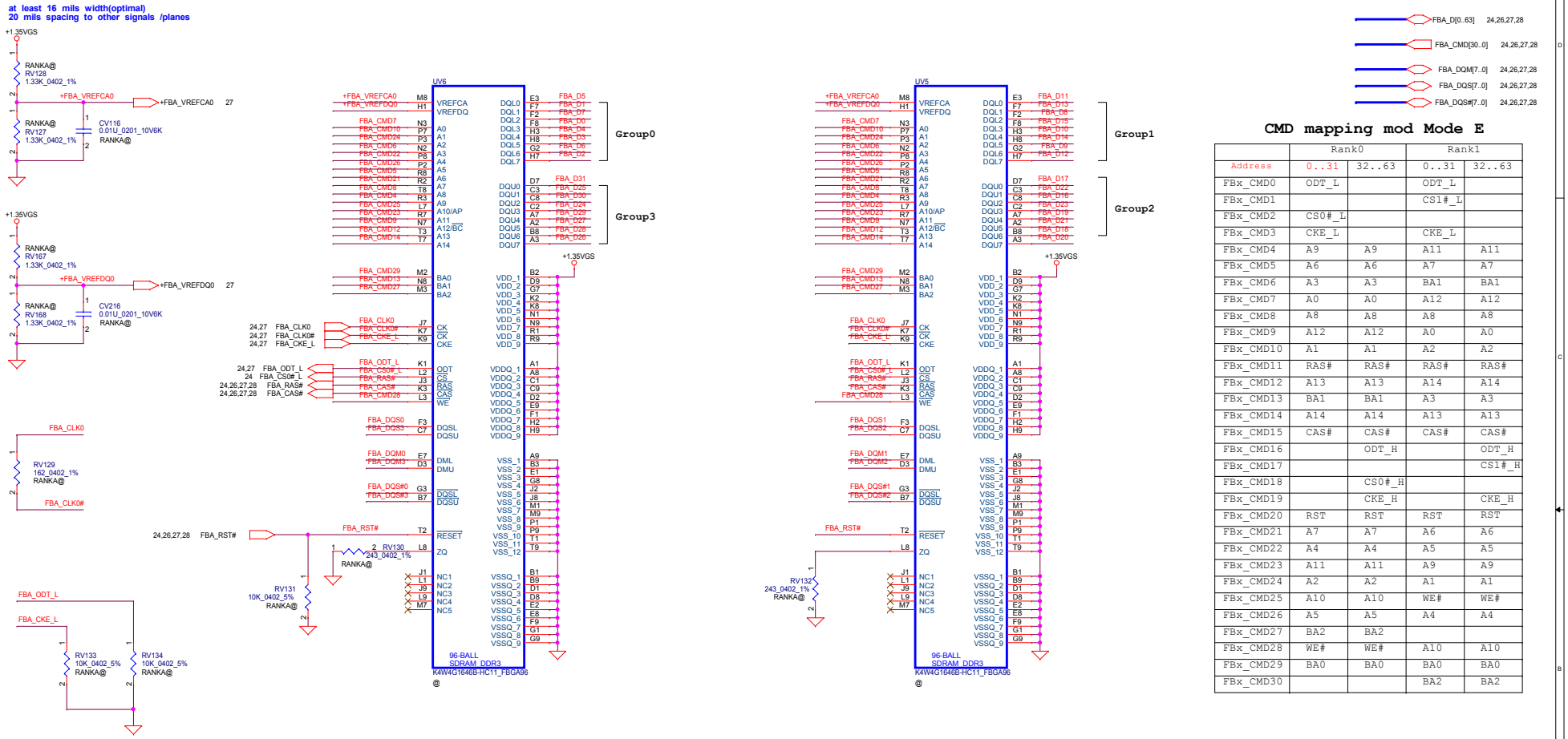
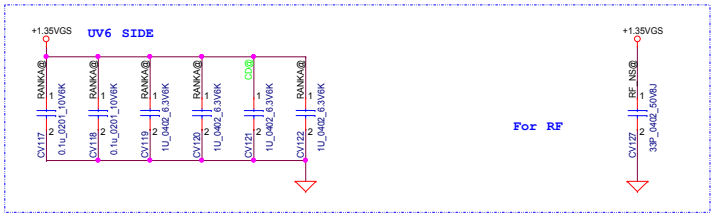
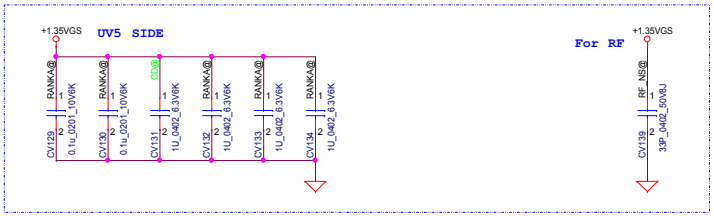


CMD mapping mod Mode E

	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2





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Title: N16X_DDR3_Rank0_[31:0]

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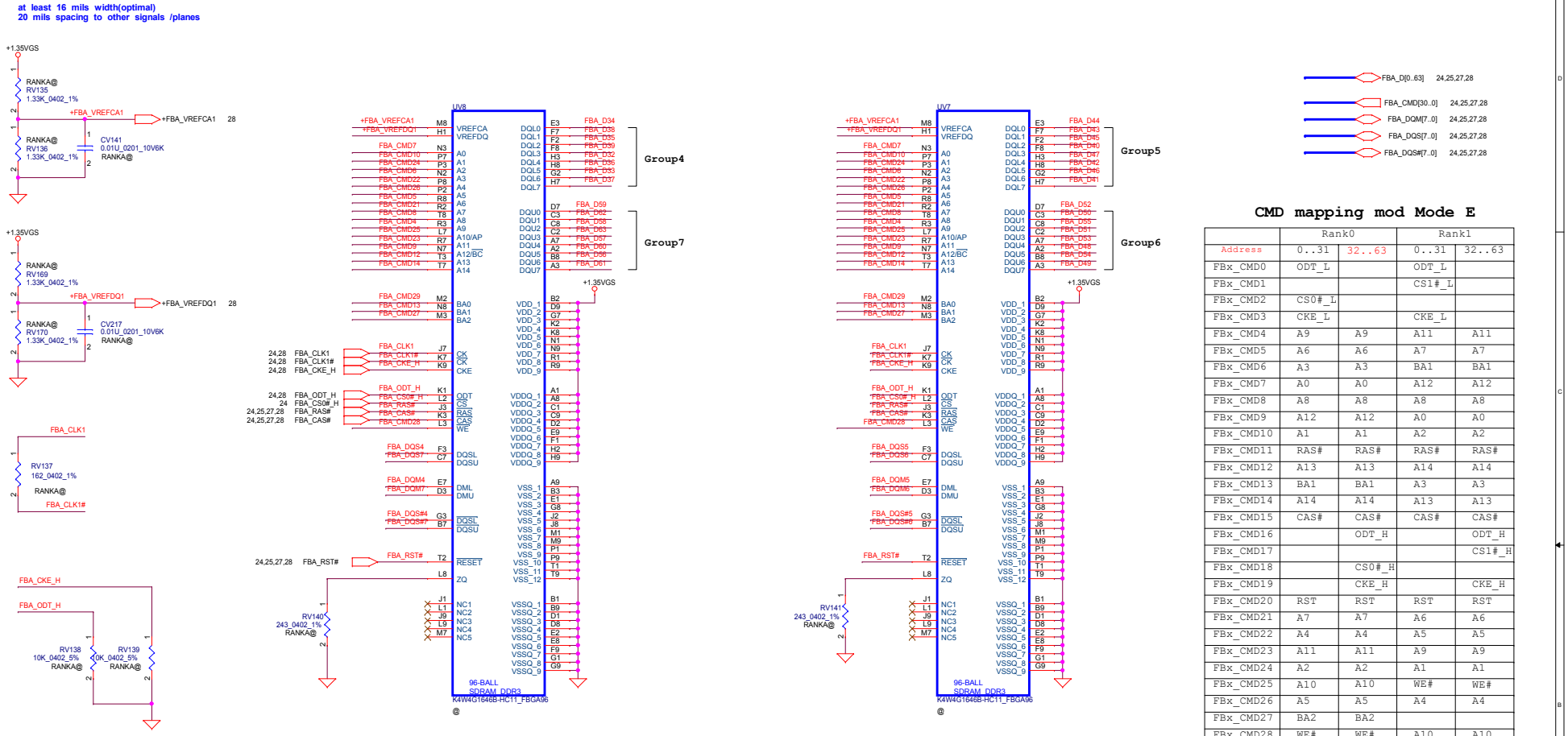
Date: Thursday, July 14, 2016 | Sheet 25 of 60



CMD mapping mod Mode E

	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: N16X_DDR3_Rank0_[64:32]

Size: C | Document Number: CG413 | Rev: 1.0

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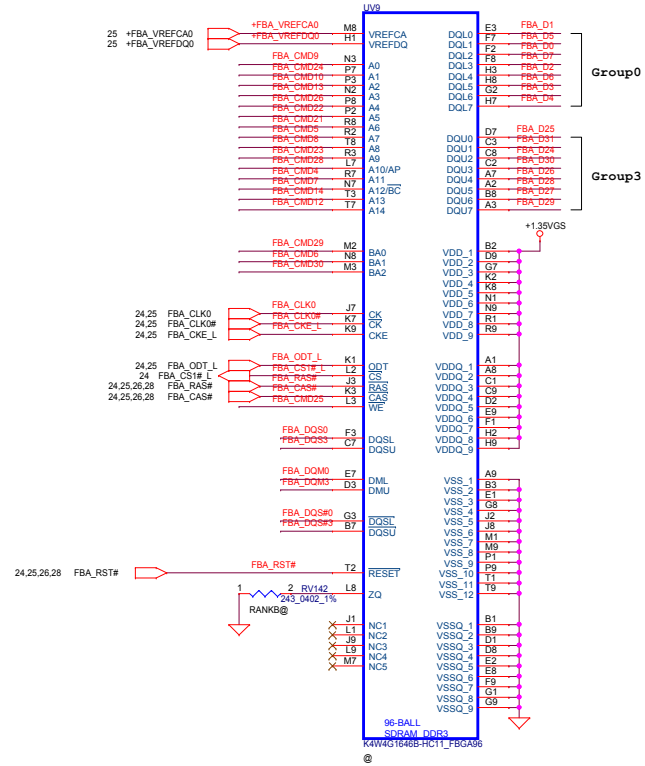
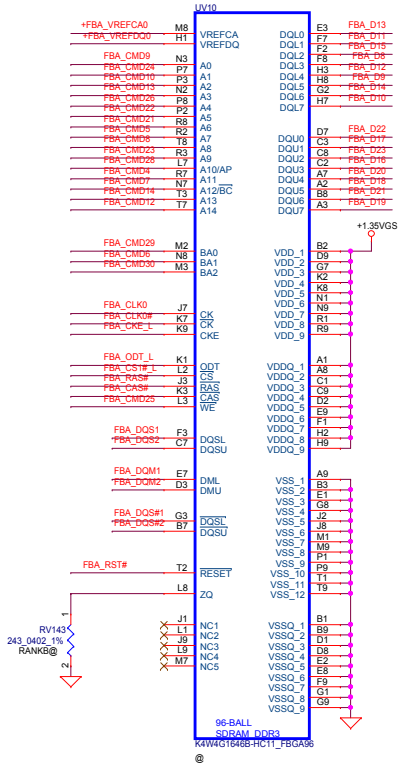
FBA_D[0..63] 24,25,26,28
FBA_CMD[30..0] 24,25,26,28
FBA_DQM[7..0] 24,25,26,28
FBA_DQS[7..0] 24,25,26,28
FBA_DQS#[7..0] 24,25,26,28

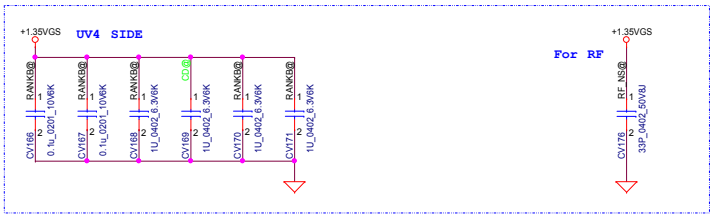
at least 16 mils width(optimal)
20 mils spacing to other signals /planes

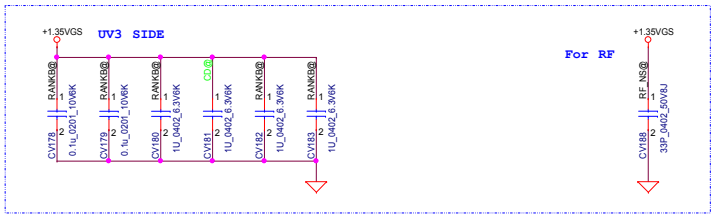




CMD mapping mod Mode E

	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2





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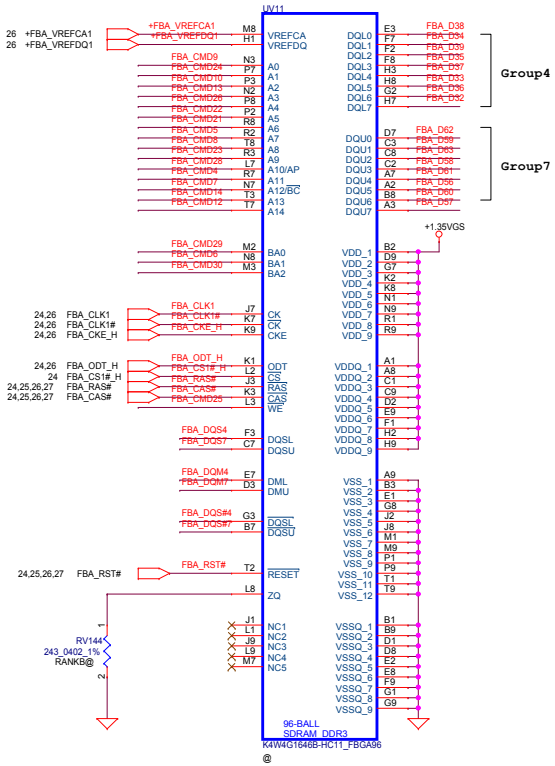
Title: **N16X_DDR3_Rank1_[31:0]**

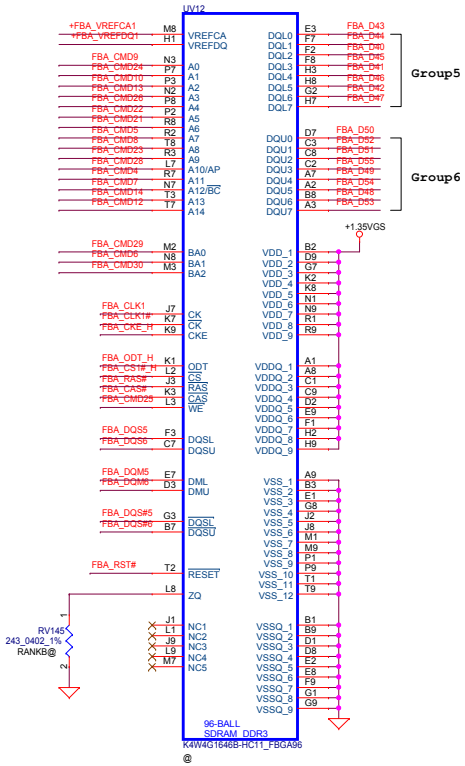
Size: C | Document Number: **CG413** | Rev: 1.0

Date: Thursday, July 14, 2016 | Sheet 27 of 60

FBA_D[0..63] 24,25,26,27
FBA_CMD[30..0] 24,25,26,27
FBA_DQM[7..0] 24,25,26,27
FBA_DQS[7..0] 24,25,26,27
FBA_DQS#[7..0] 24,25,26,27

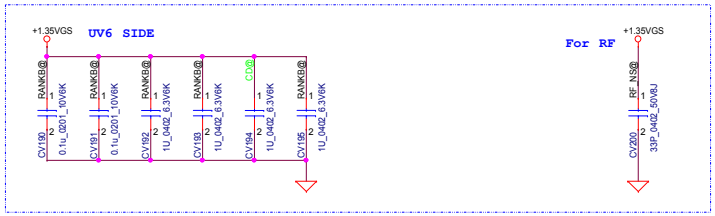
at least 16 mils width(optimal)
20 mils spacing to other signals /planes

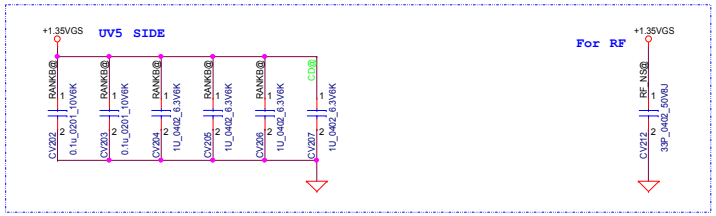




CMD mapping mod Mode E

	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2





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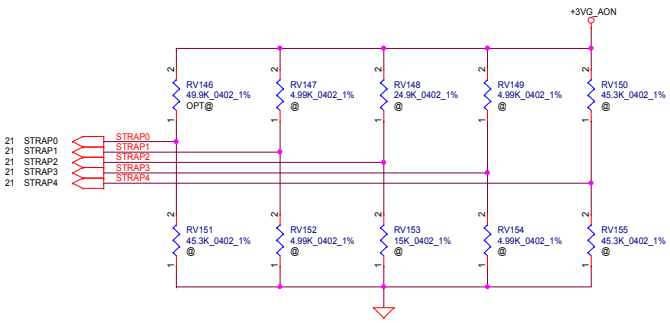
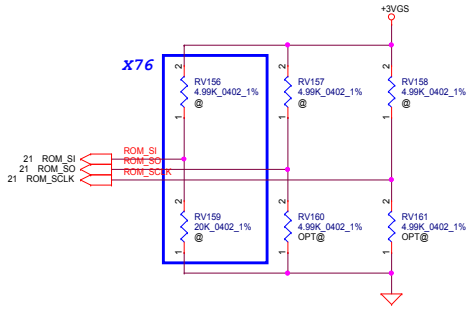
Title: N16X_DDR3_Rank1_[64:32]

Size: C | Document Number: CG413 | Rev: 1.0

Date: Thursday, July 14, 2016 | Sheet 28 of 60





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

GPU	Configuration	FB Memory (DDR3L)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR N16V-GMR1	Single-Rank	Samsung 900MHz	K4W4G1646E-BC1A	0x1	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
			256M x 16	PD 10K							
		Hynix 900MHz	H5TC4G63CFR-N0C	0x2							
			256M x 16	PD 15K							
		Micron 900MHz	MT41J256M16LY-091G:N	0x6							
			256M x 16	PD 34.8K							
	Dual-Rank	Samsung 900MHz	K4W4G1646E-BC1A	0xF							
			256M x 16	PU 45.3K							
		Hynix 900MHz	H5TC4G63CFR-N0C	0xE							
			256M x 16	PU 34.8K							
		Micron 900MHz	MT41J256M16LY-091G:N	0xA							
			256M x 16	PU 15K							

VRAM	X76 P/N	VRAM Q'ty	VRAM P/N
Samsung	X7610212201	4	SA000063F20
	X7610212001	8	
Hynix	X7610212202	4	SA00007DU10
	X7610212101	8	
Micron	X7610212203	4	SA00007QJ00
	N/A	8	

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Issued Date: 2015/08/20 Deciphered Date: 2016/08/20

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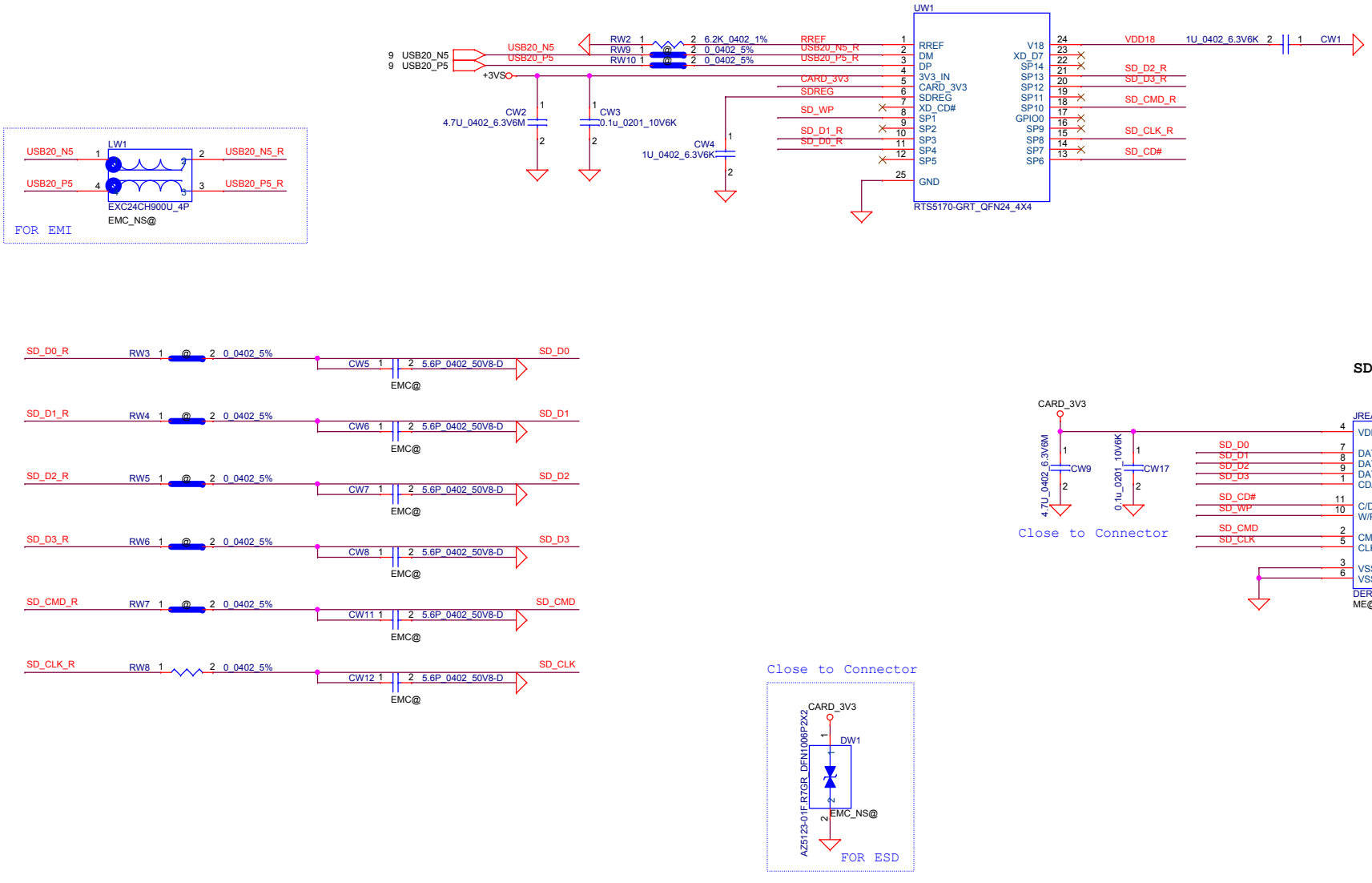
Title: N16X_MISC

Size: C | Document Number: CG413 | Rev: 1.0

Date: Thursday, July 14, 2016 | Sheet 29 of 60



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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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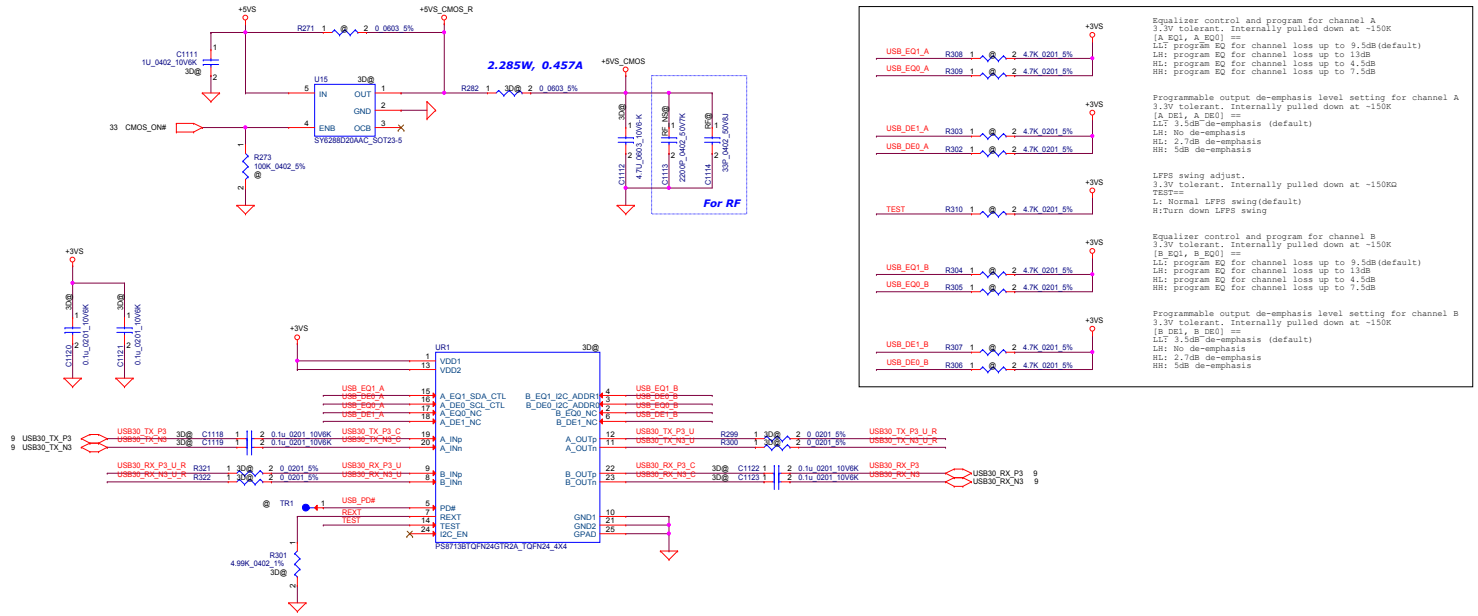
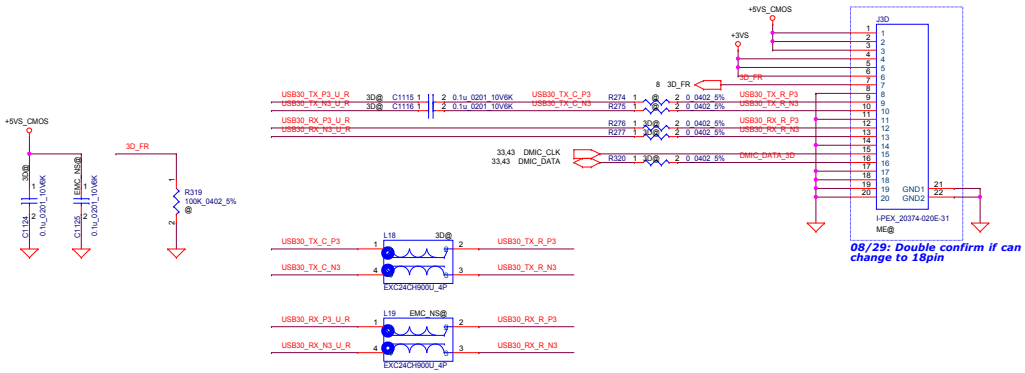
Title: **Cardreader**

Size: Custom | Document Number: CG413 | Rev: 1.0

Date: Thursday, July 14, 2016 | Sheet 30 of 60



3D Camera Connector



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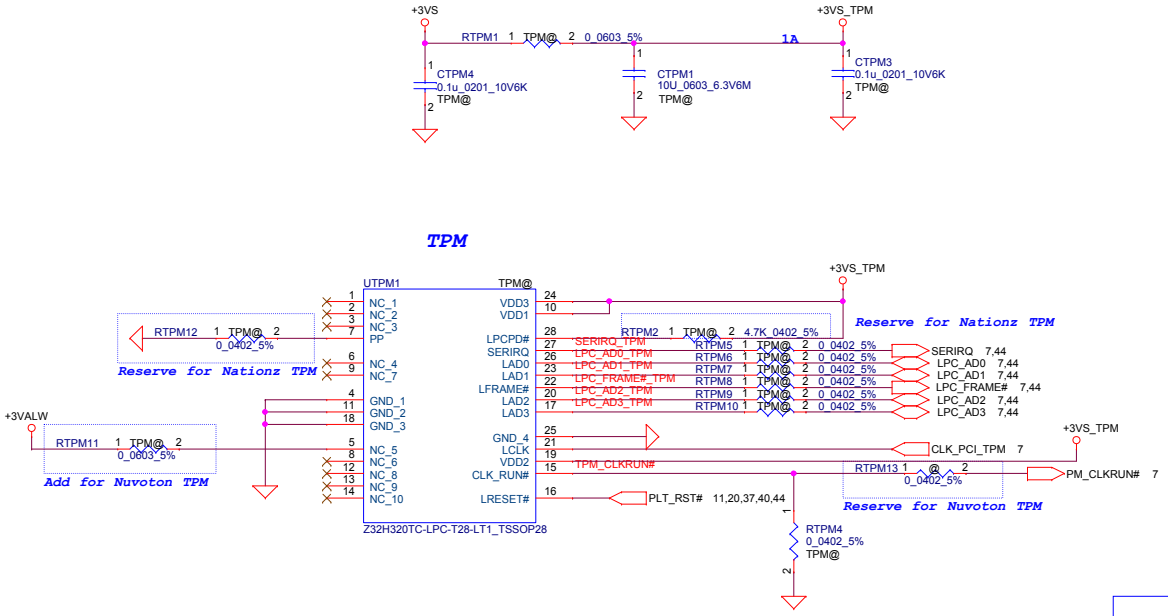
Title: 3D Camera

Size: Custom | Document Number: CG413 | Rev: 1.0

Date: Thursday, July 14, 2016 | Sheet 31 of 60



	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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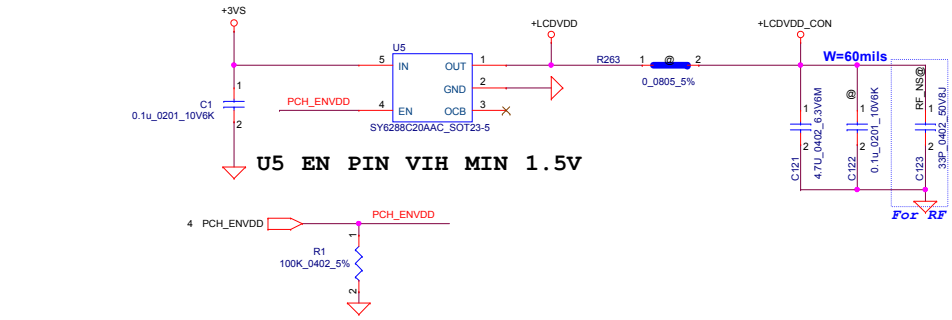
Title: TPM

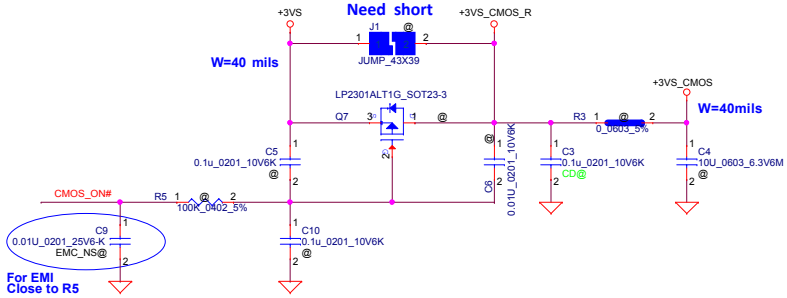
Size: Custom | Document Number: CG413 | Rev: 1.0

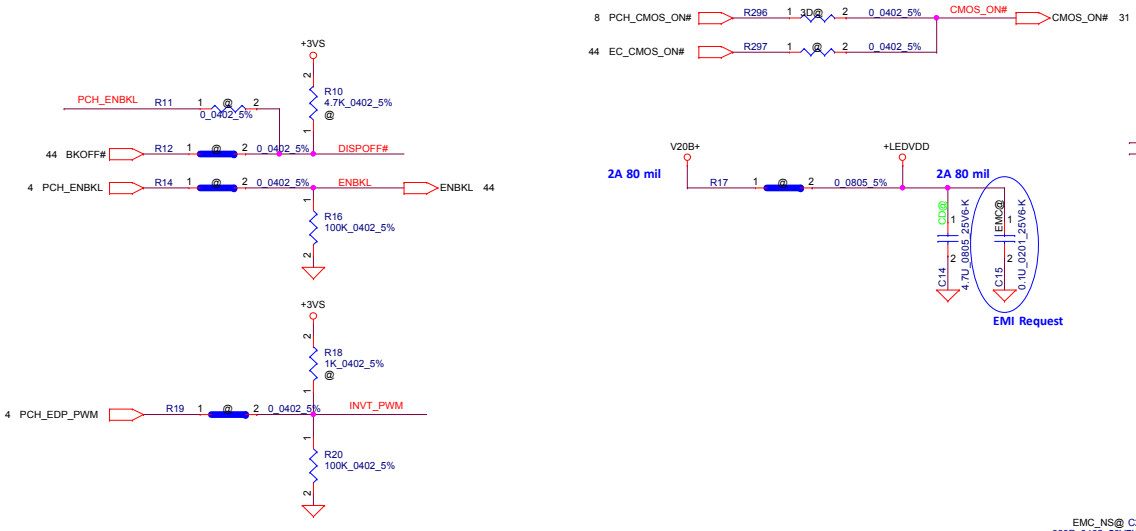
Date: Thursday, July 14, 2016 | Sheet 32 of 60

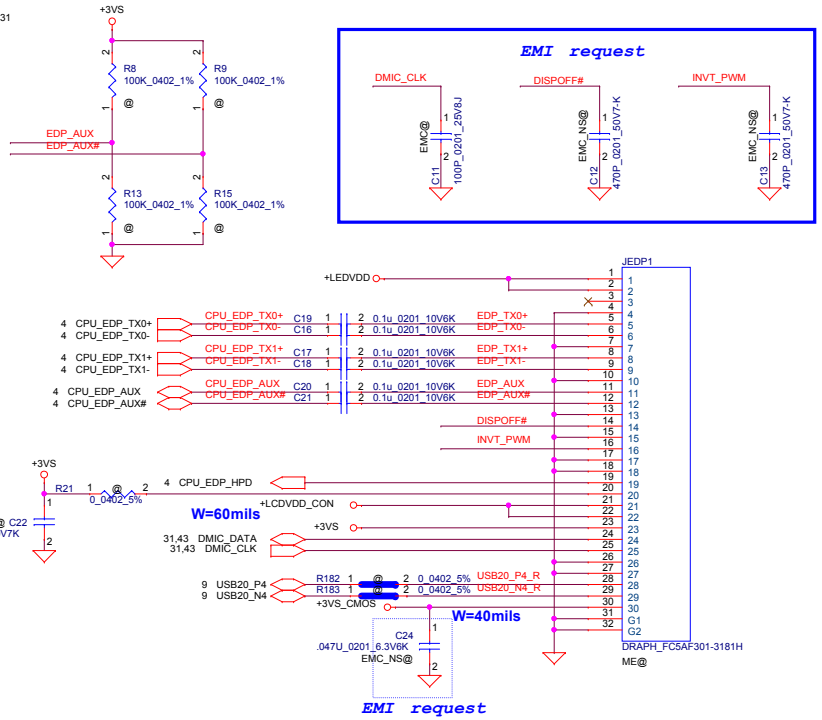
LCD POWER CIRCUIT



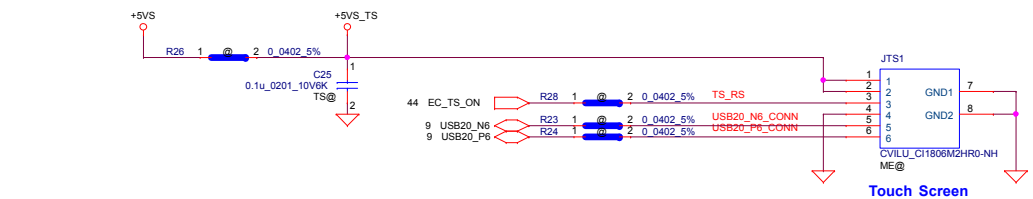
CMOS Camera

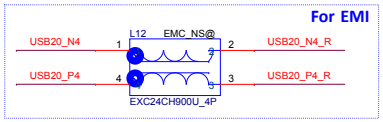


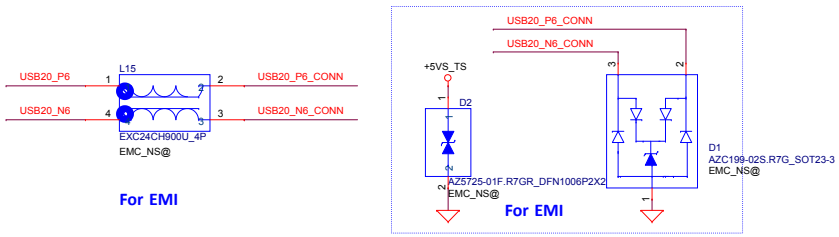




Touch Screen







Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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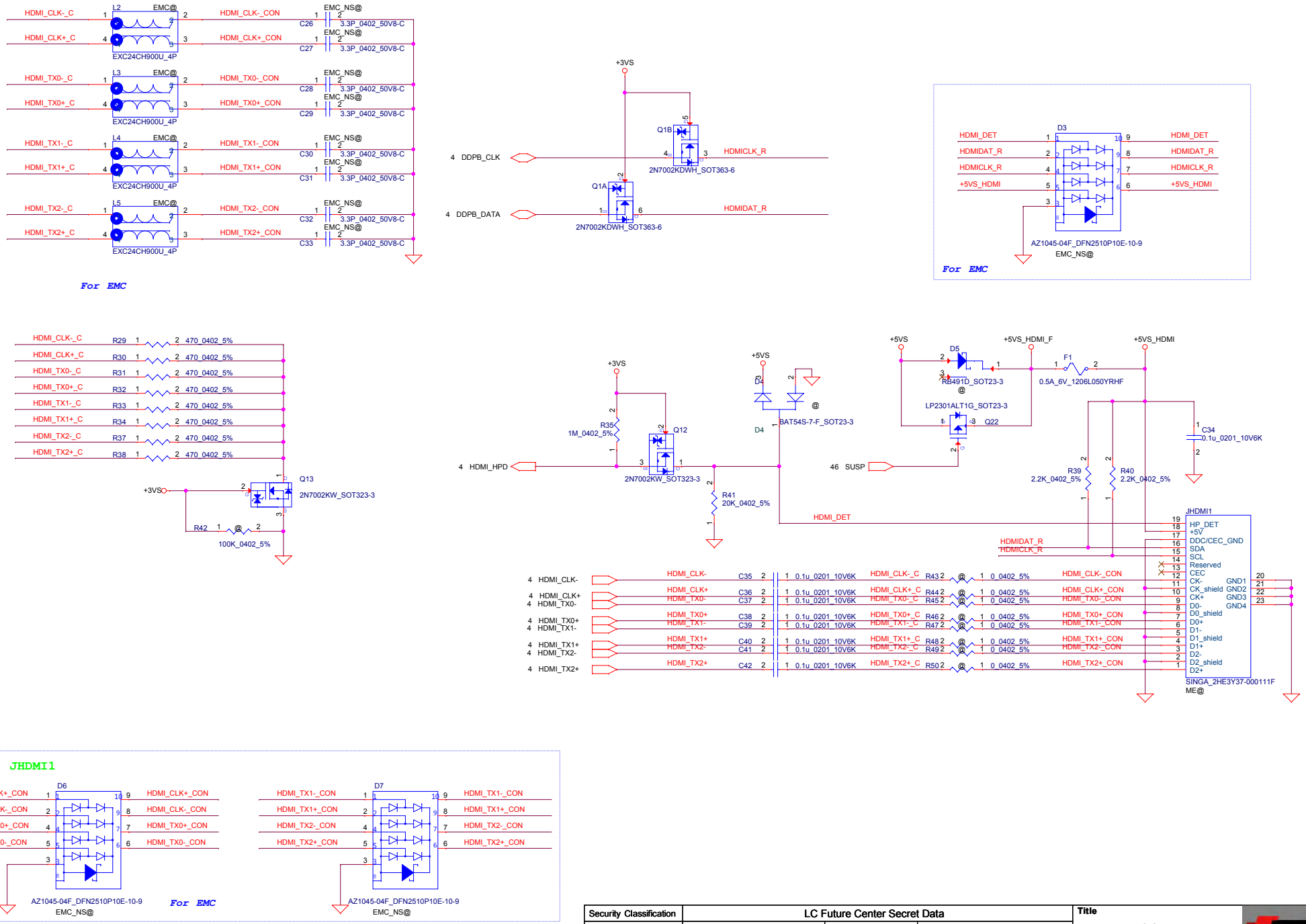
Title: eDP/CMOS/Touch screen

Size: Custom | Document Number: CG413 | Rev: 1.0

Date: Thursday, July 14, 2016 | Sheet 33 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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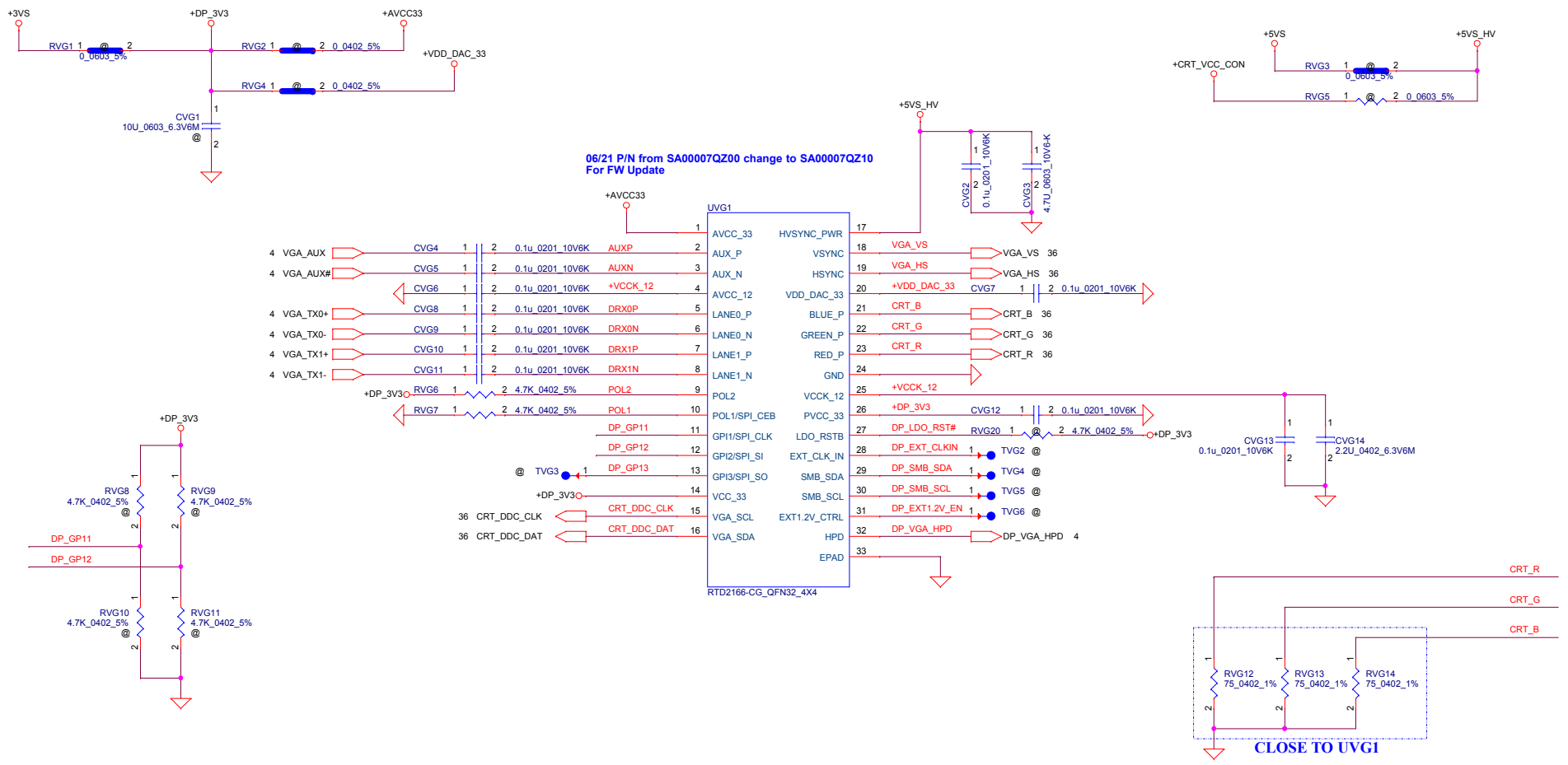
Title: **HDMI_CONN**

LCFC

Size	Document Number	Rev
Custom	CG413	1.0

Date: Thursday, July 14, 2016 | Sheet 34 of 60



Security Classification	LC Future Center Secret Data		
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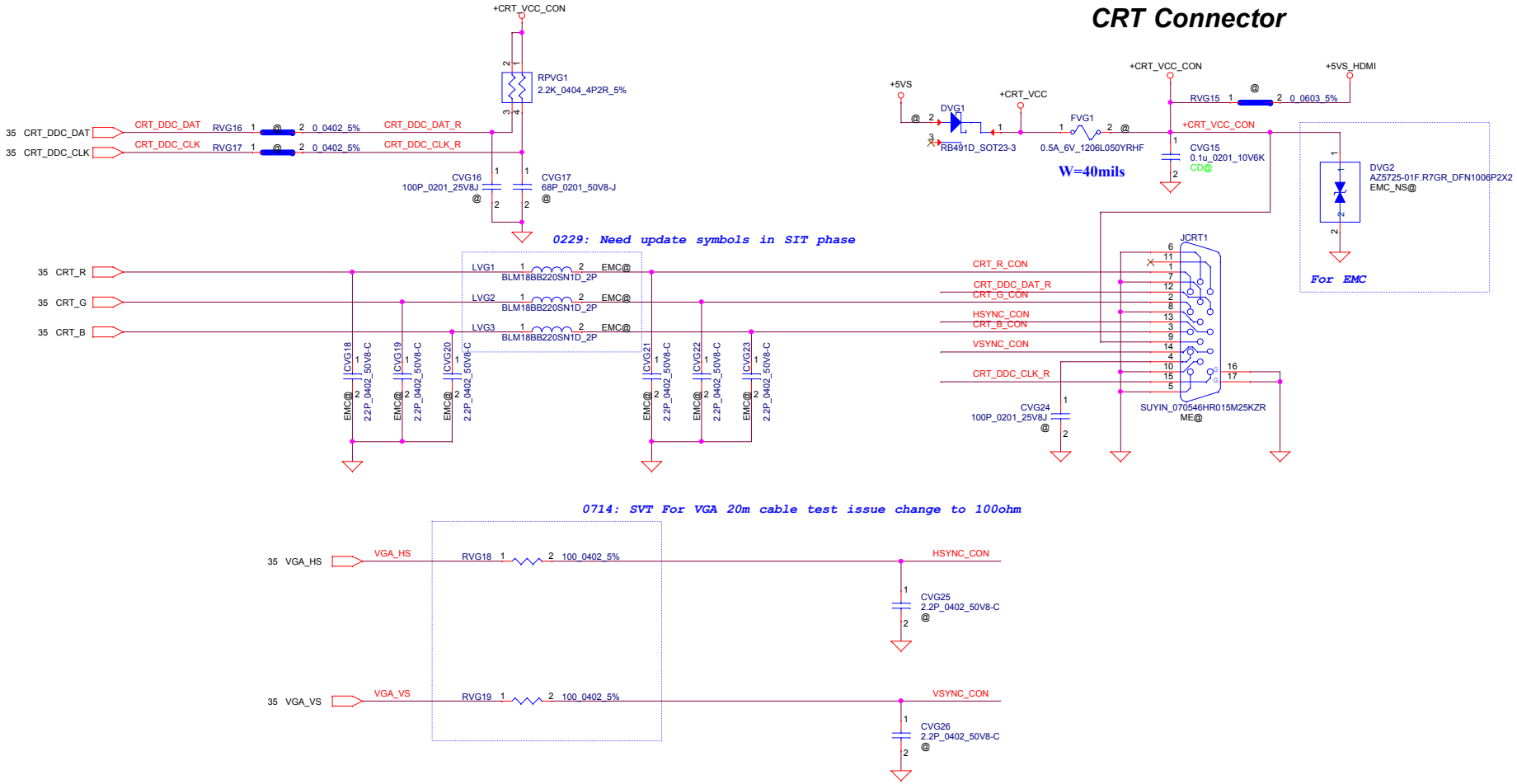
Title: **P35-DP to VGA (RTD2166)**

Size: Custom | Document Number: **CG413** | Rev: 1.0

Date: Thursday, July 14, 2016 | Sheet 35 of 60

CRT Connector



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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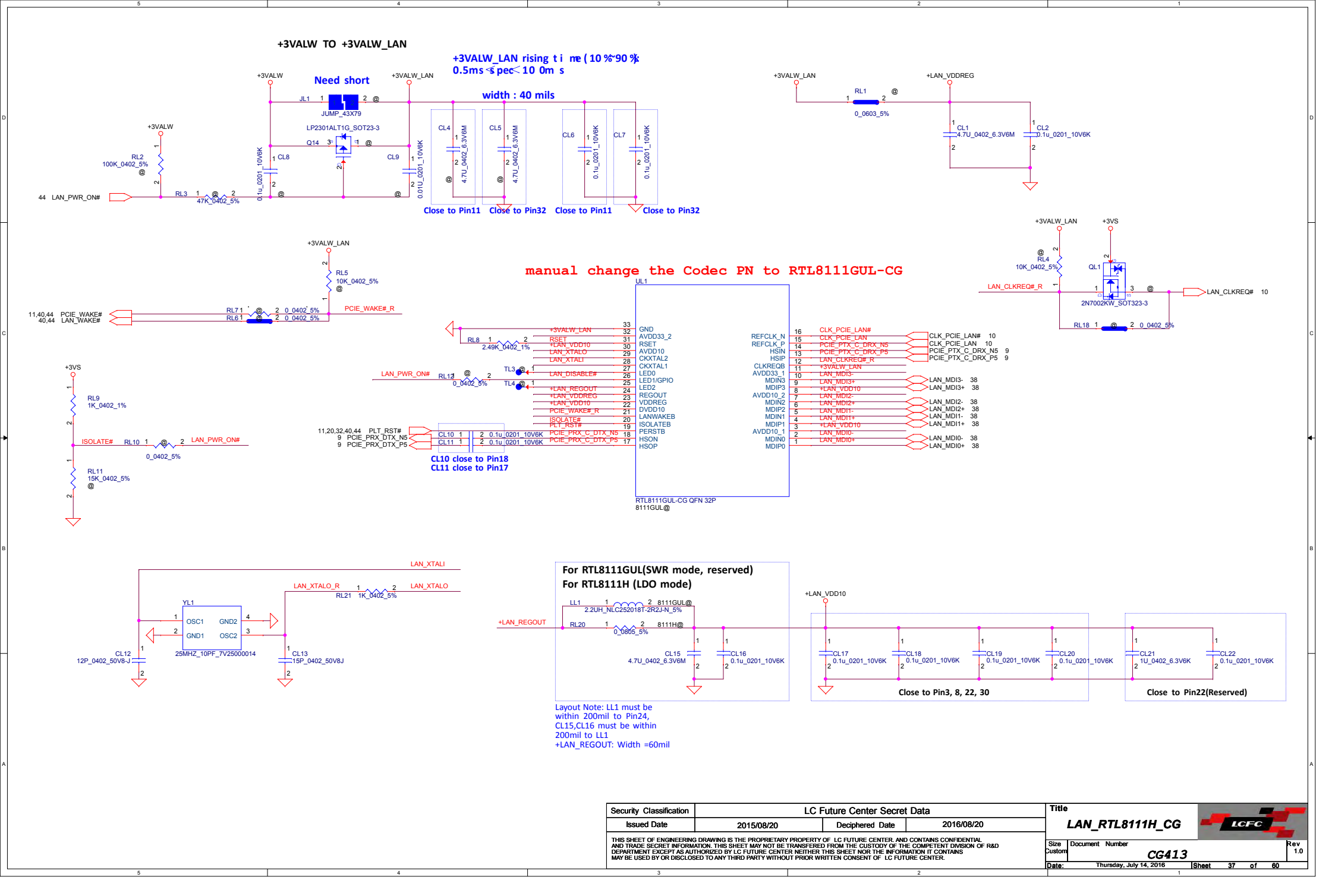
Title: CRT_CONN

Size: Custom | Document Number: CG413 | Rev: 1.0

Date: Thursday, July 14, 2016 | Sheet 36 of 60



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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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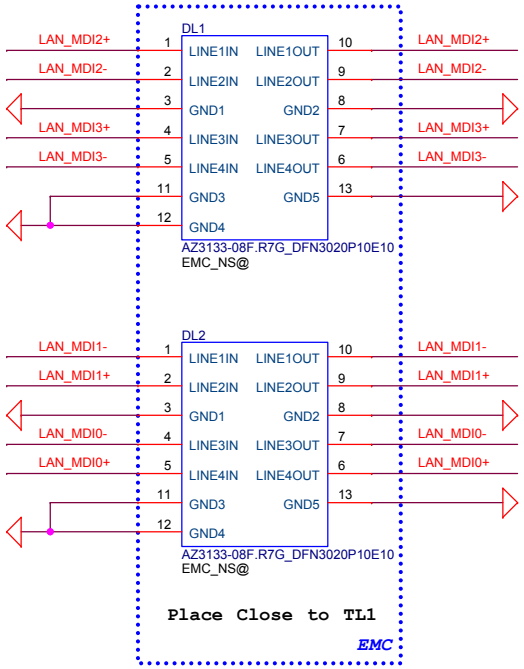
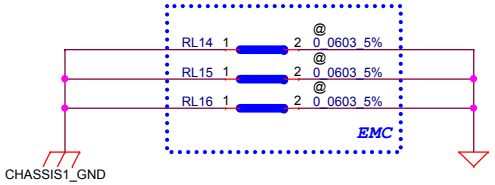
Title: LAN_RTL8111H_CG

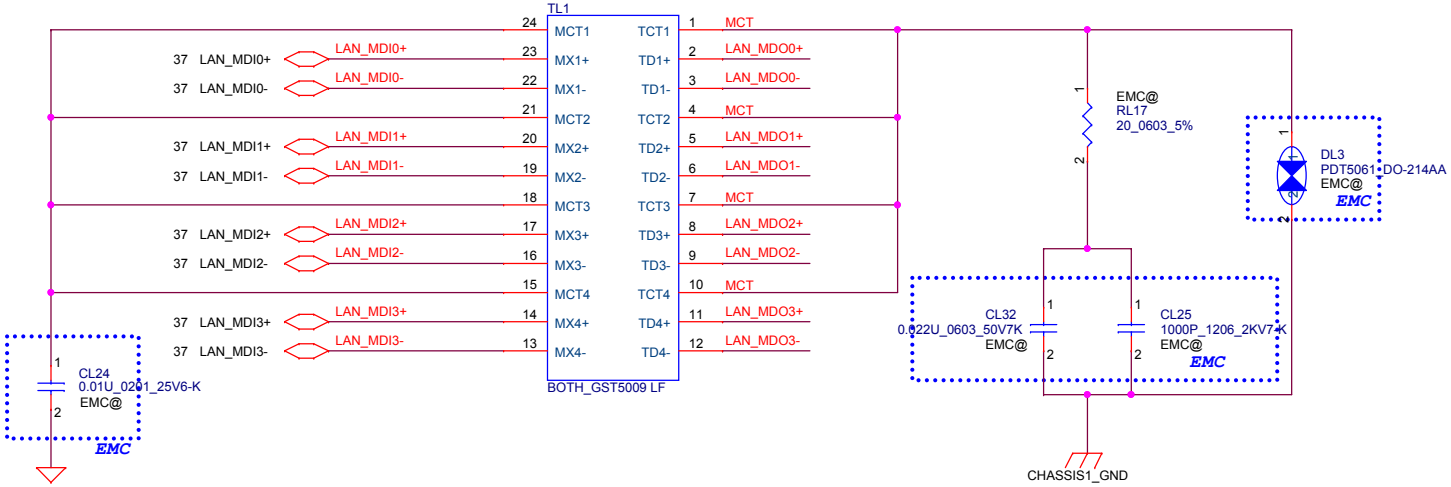
Size: Custom | Document Number: CG413 | Rev: 1.0

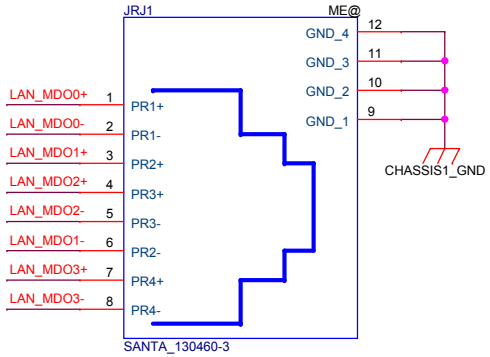
Date: Thursday, July 14, 2016 | Sheet 37 of 60

DL1/DL2
1'S PN:SC300003M00









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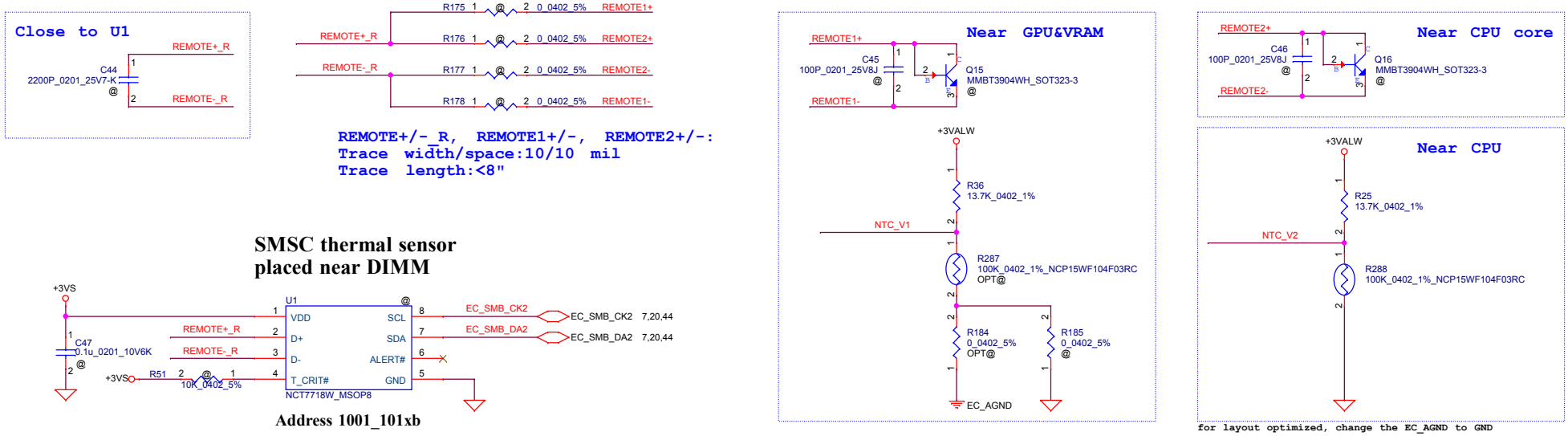
Title: LAN_Transformer

Size: B | Document Number: CG413 | Rev: 1.0

Date: Thursday, July 14, 2016 | Sheet 38 of 60



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Title: Thermal sensor/FAN CONN

Size: Custom | Document Number: CG413 | Rev: 1.0

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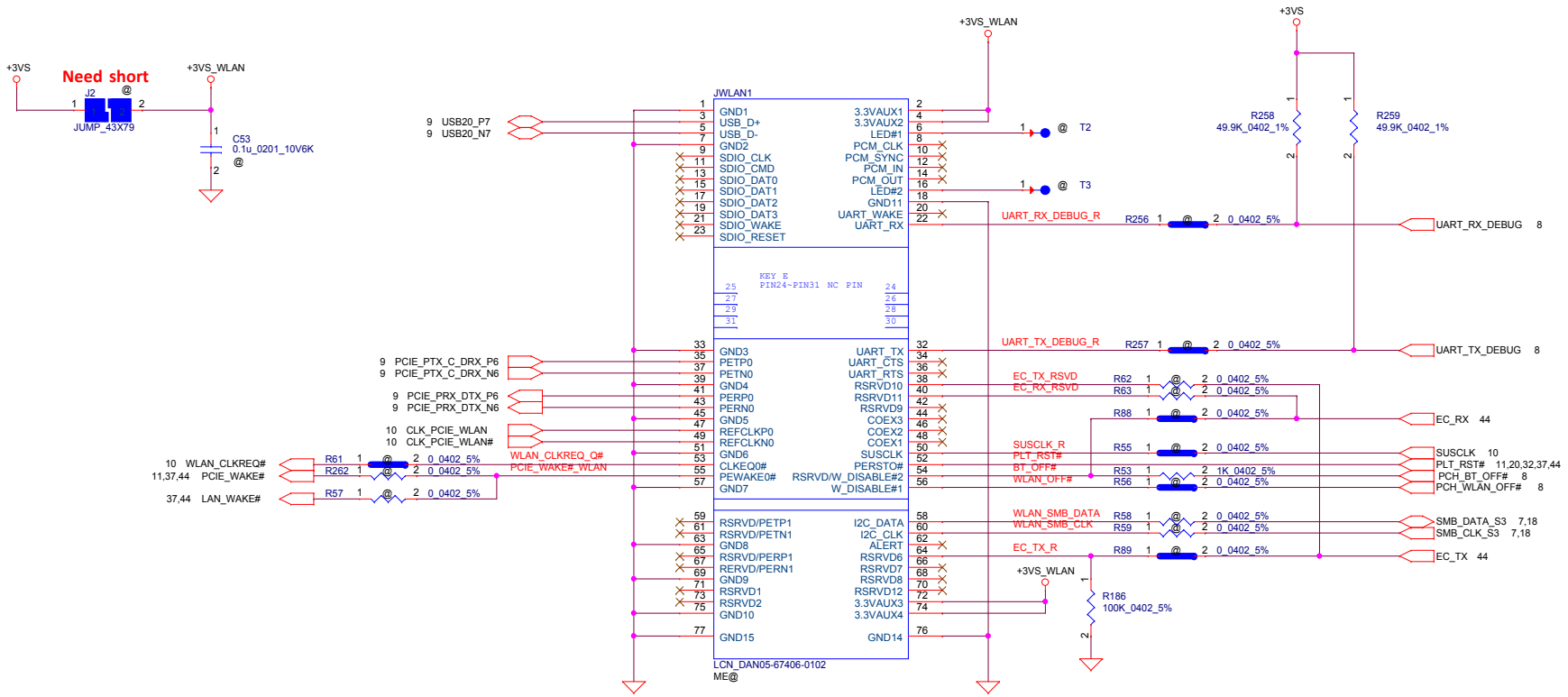
Mini-Express Card(WLAN/WiMAX)



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Title: NGFF WLAN

Size: Custom | Document Number: CG413 | Rev: 1.0

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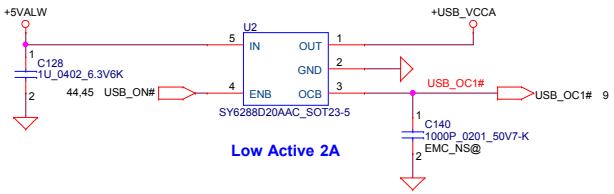
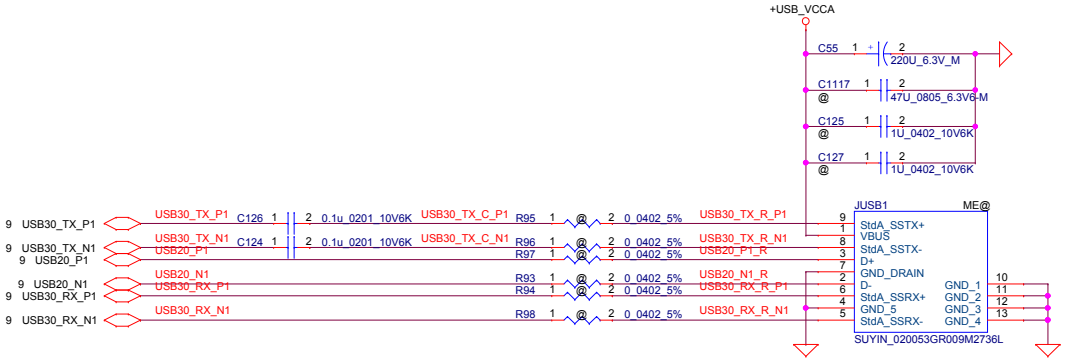
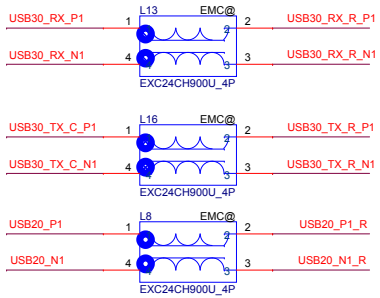
LEFT SIDE USB3.0 PORT x1

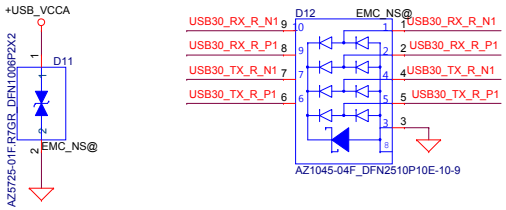


Low Active 2A





EMC



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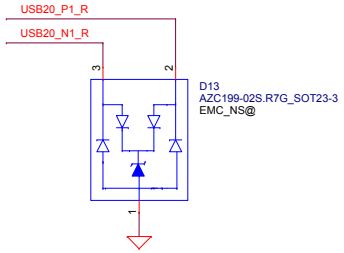

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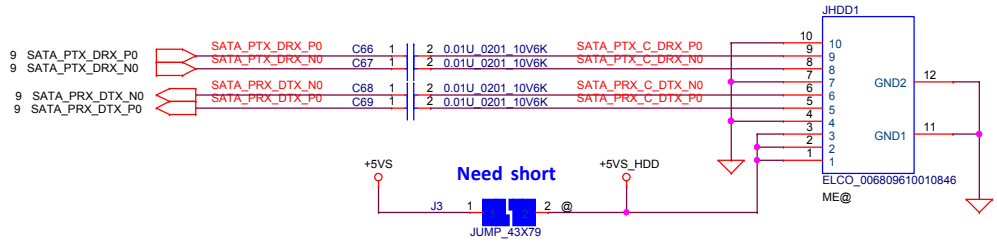
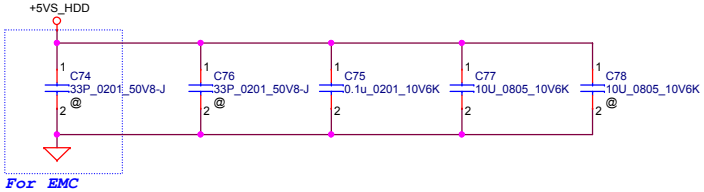
Title: **USB3.0 PORT (LEFT)**

Size: Custom | Document Number: **CG413** | Rev: 1.0

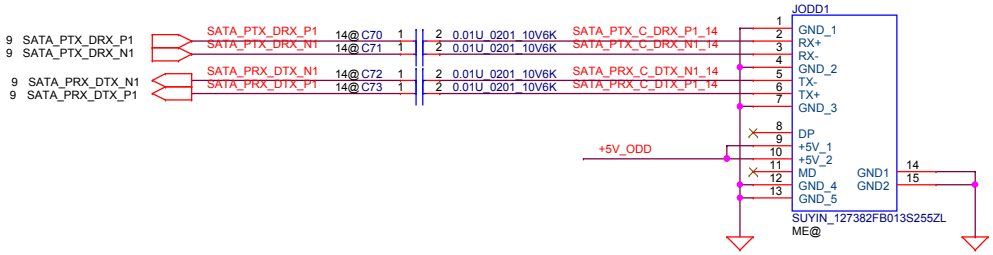
Date: Thursday, July 14, 2016 | Sheet 41 of 60

SATA HDD Conn.

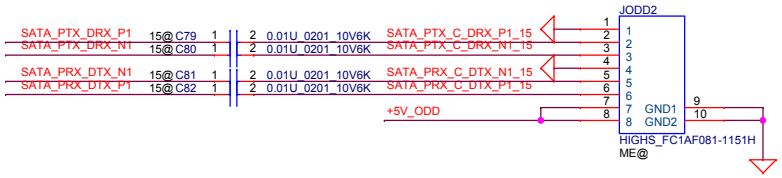


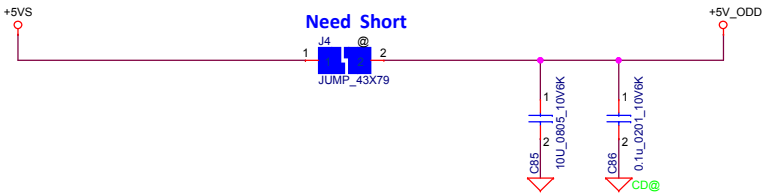


FOR 14"
SATA ODD Conn.



FOR 15"
SATA ODD FFC Conn





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Title: **HDD/ODD CONN**

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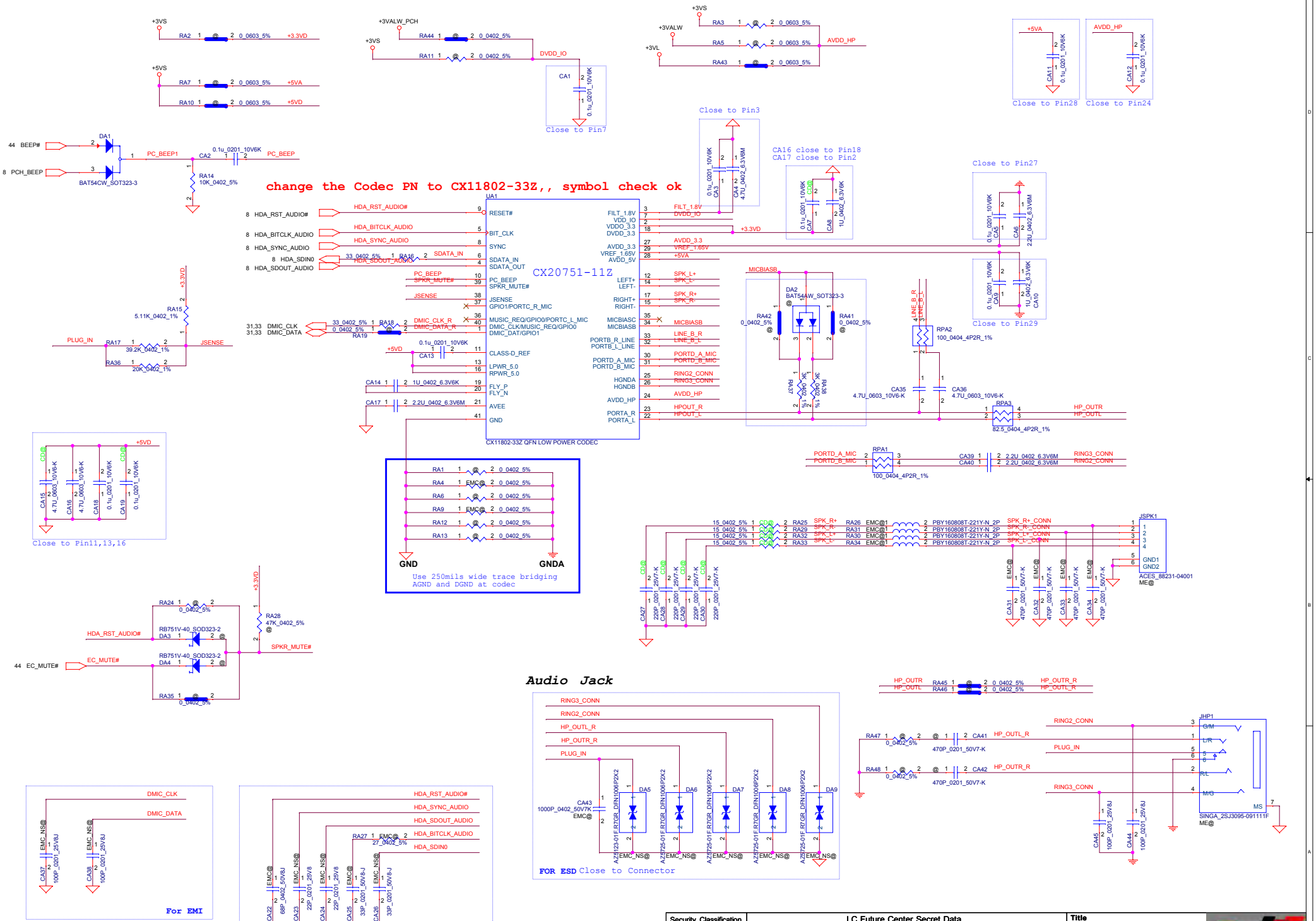

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Title: Codec_CX11802 & Audio jack

Size: Custom | Document Number: CG413 | Rev: 1.0

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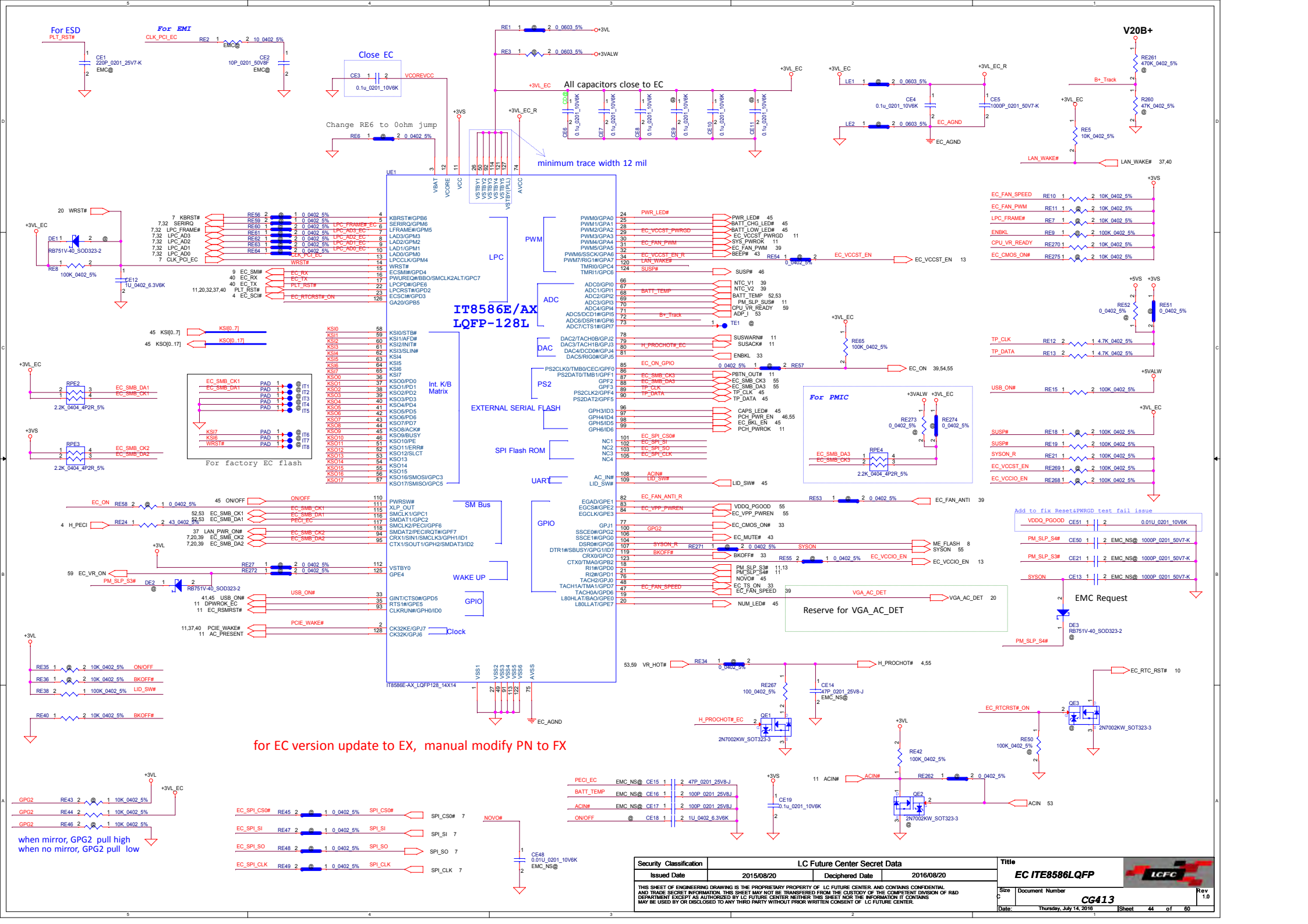
V20B+
IT8586E/AX
LQFP-128L
UE1
For ESD
For EMI
Close EC
Change RE6 to 0ohm jump
All capacitors close to EC
minimum trace width 12 mil
For PMIC
For factory EC flash
Reserve for VGA_AC_DET
EMC Request
Add to fix Reset&PWRGD test fail issue
for EC version update to EX, manual modify PN to FX
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
LPC
PWM
ADC
DAC
PS2
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
Int. K/B Matrix
SM Bus
WAKE UP
GPIO
Clock
IT8586E-AX_LQFP128_14X14
Security Classification
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Title
EC ITE8586LQFP
Size
C
Document Number
CG413
Rev
1.0
Date:
Thursday, July 14, 2016
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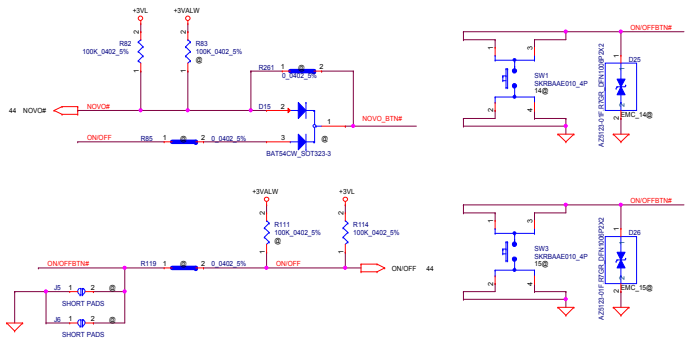
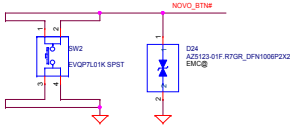
44
of
60

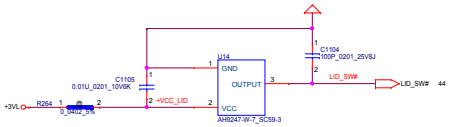
ON/OFF switch



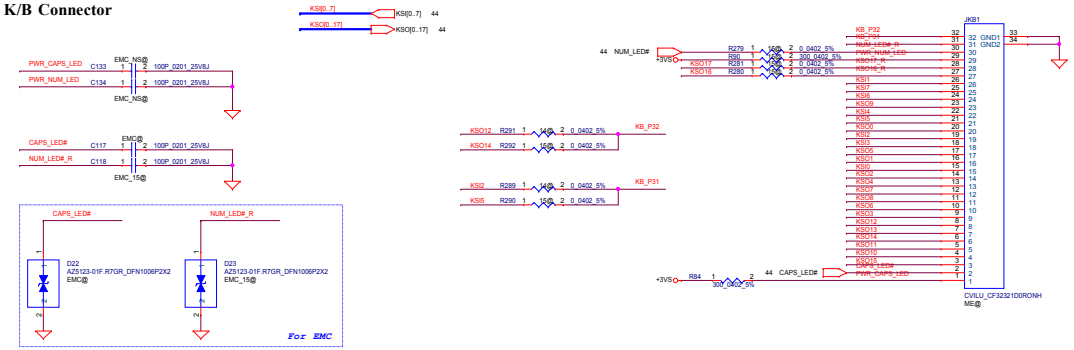
Novo button



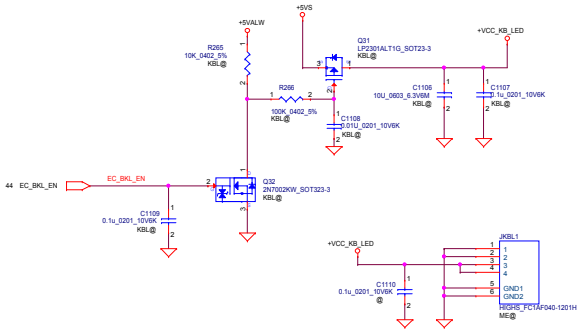
LID switch



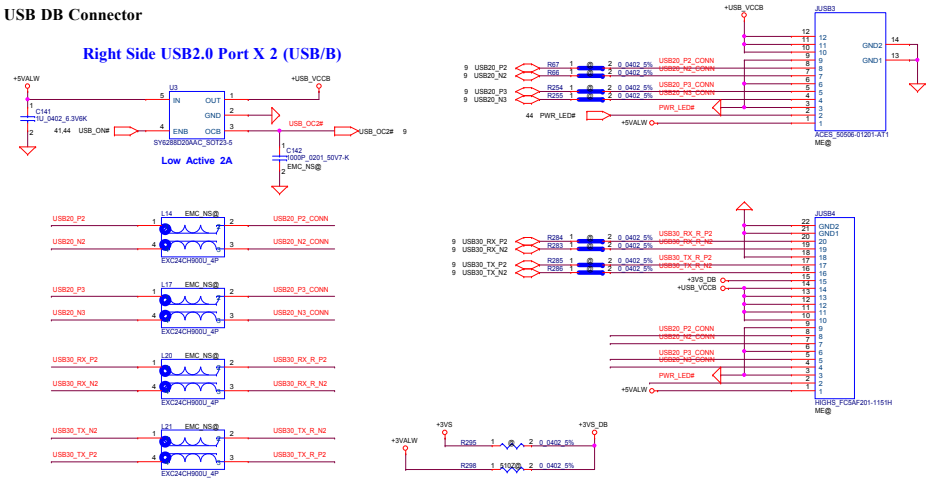
K/B Connector



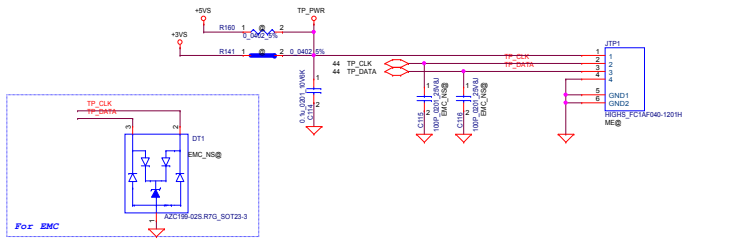
KB Backlight Connector

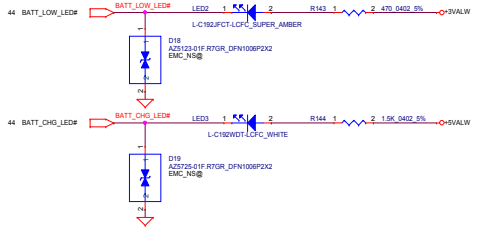


USB DB Connector



TP/B Connector





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Title: KBD/PWR/IO/LED/TP Conn.

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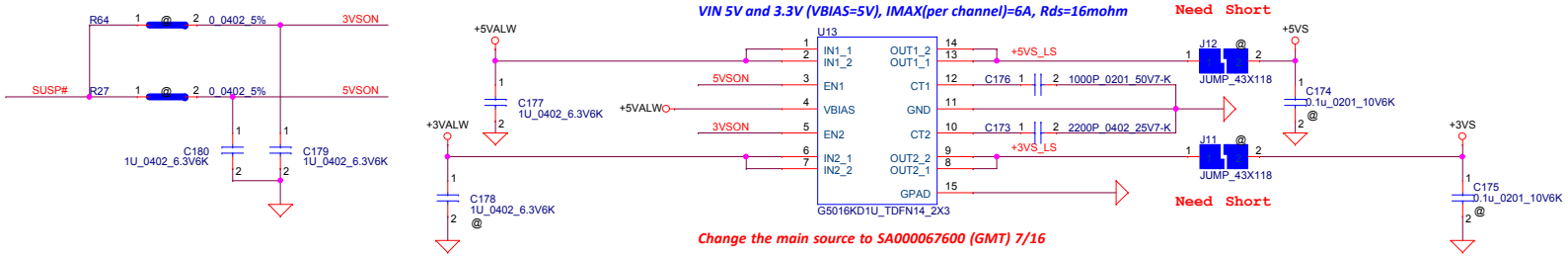
Load Switch

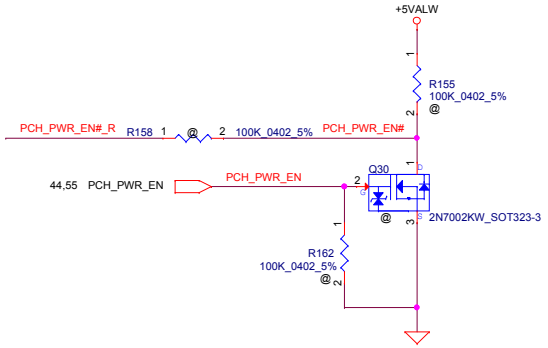
+5VALW To +5VS — **+3VS, C173 --> 2.74ms**

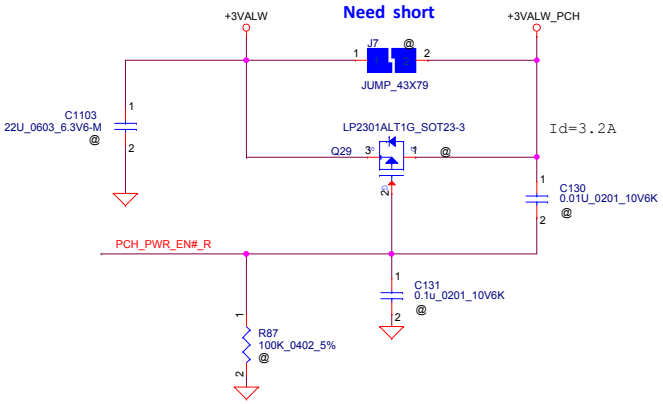
+3VALW To +3VS — **+5VS, C176 --> 2.03ms**

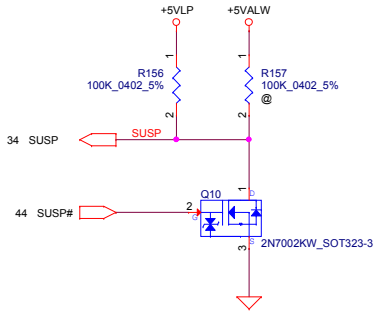
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm



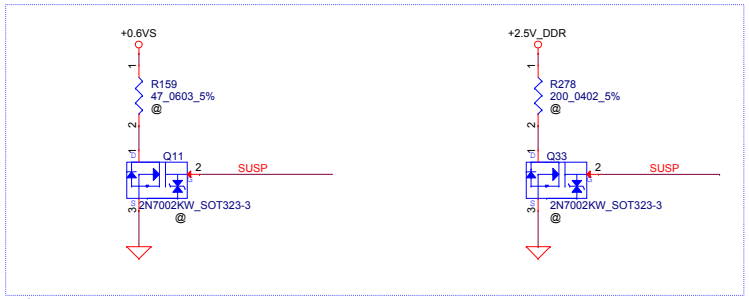
Change the main source to SA000067600 (GMT) 7/16







For DisCharge



08/29: Need double check enable signal and the resistance

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Title: **DC V TO VS INTERFACE**

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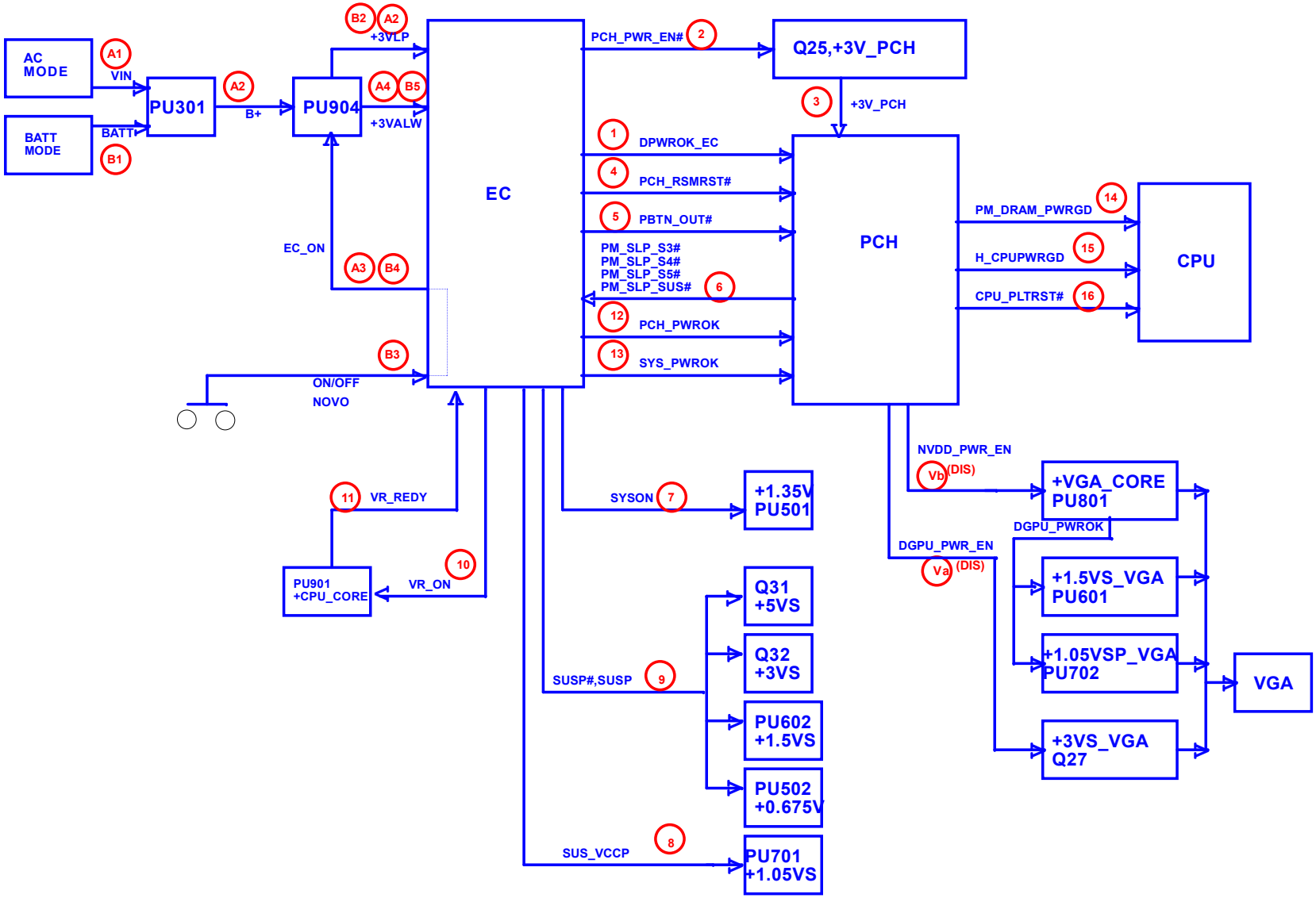

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Title: **Power sequence block**

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ZZZ1 @ — PCB PN, DAZ11500100
ZZZ1 @ — PCB PN, DAZ11600100
ZZZ1 @ — PCB PN, DAZ11500200
ZZZ1 @ — PCB PN, DAZ11600200
ZZZ1 @ — PCB PN, DAZ11300100
ZZZ1 @ — PCB PN, DAZ11300200

PCB_MB

UL1 8111H@ — RTL8111H-CG, SA000074W00

LAN Chip

UV1 N16SGTR@ — N16S-GTR GPU, SA00007DA10
UV1 N16VGMR1@ — N16V-GMR1 GPU, SA00007QX00

GPU

ZZZ2 @ — Samsung, X76XXXXXXXXX
ZZZ2 @ — Micron, X76XXXXXXXXX

2133MT/s DRAM X76 BOM

UD1 @ — K4A8G165WB-BCPB, SA00007DA10
UD2 @ — K4A8G165WB-BCPB, SA00007DA10
UD3 @ — K4A8G165WB-BCPB, SA00007DA10
UD4 @ — K4A8G165WB-BCPB, SA00007DA10
RC1634 @ — 10K_0402_5%, SD02B10028J
RC1635 @ — 10K_0402_5%, SD02B10028J
RC1640 @ — 10K_0402_5%, SD02B10028J

2133MT/s DRAM_Samsung 4G

2133MT/s DRAM_Hynix 4G

UD1 @ — MT40A512M16HA-083E:A, SA000079F10
UD2 @ — MT40A512M16HA-083E:A, SA000079F10
UD3 @ — MT40A512M16HA-083E:A, SA000079F10
UD4 @ — MT40A512M16HA-083E:A, SA000079F10
RC1631 @ — 10K_0402_5%, SD02B10028J
RC1635 @ — 10K_0402_5%, SD02B10028J
RC1640 @ — 10K_0402_5%, SD02B10028J

2133MT/s DRAM_Micron 4G

ZZZ2 DRAM_S4G@ — Samsung, X7612912002
ZZZ2 DRAM_M4G@ — Micron, X7612912003

2400MT/s DRAM X76 BOM

UD1 MD_S8Gb@ — K4A8G165WB-BCRC, SA00007TQ00
UD2 MD_S8Gb@ — K4A8G165WB-BCRC, SA00007TQ00
UD3 MD_S8Gb@ — K4A8G165WB-BCRC, SA00007TQ00
UD4 MD_S8Gb@ — K4A8G165WB-BCRC, SA00007TQ00
RC1634 MD_S8Gb@ — 10K_0402_5%, SD02B10028J
RC1635 MD_S8Gb@ — 10K_0402_5%, SD02B10028J
RC1639 MD_S8Gb@ — 10K_0402_5%, SD02B10028J

2400MT/s DRAM_Samsung 4G

2400MT/s DRAM_Hynix 4G

UD1 MD_M8Gb@ — MT40A512M16JY-083E:B, SA00007TS00
UD2 MD_M8Gb@ — MT40A512M16JY-083E:B, SA00007TS00
UD3 MD_M8Gb@ — MT40A512M16JY-083E:B, SA00007TS00
UD4 MD_M8Gb@ — MT40A512M16JY-083E:B, SA00007TS00
RC1631 MD_M8Gb@ — 10K_0402_5%, SD02B10028J
RC1635 MD_M8Gb@ — 10K_0402_5%, SD02B10028J
RC1639 MD_M8Gb@ — 10K_0402_5%, SD02B10028J

2400MT/s DRAM_Micron 4G

ZZZ4 HDMI@ — HDMI PN, R00000040J

HDMI Royalty

UC1 80710@ — KBL-U CPU, SA00080710
UC1 80310@ — KBL-U CPU, SA00080310
UC1 80410@ — KBL-U CPU, SA00080410

CPU

ZZZ3 S4GX4@ — Samsung, X7612912001
ZZZ3 H4GX4@ — Hynix, X7612712003
ZZZ3 M4GX4@ — Micron, X7612712002
ZZZ3 S4GX8@ — Samsung, X7612712001
ZZZ3 H4GX8@ — Hynix, X7612712008
ZZZ3 M4GX8@ — Micron, X7612712007

VRAM X76 BOM

UV5 S4G_SR@ — K4W4G1646E-BC1A, SA000063F20
UV6 S4G_SR@ — K4W4G1646E-BC1A, SA000063F20
UV7 S4G_SR@ — K4W4G1646E-BC1A, SA000063F20
UV8 S4G_SR@ — K4W4G1646E-BC1A, SA000063F20
RV159 S4G_SR@ — 10K_0402_1%, SD03410028J

VRAM_Samsung 4GX4

UV5 H4G_SR@ — H5TC4G63CFR-N0C, SA00007DU10
UV6 H4G_SR@ — H5TC4G63CFR-N0C, SA00007DU10
UV7 H4G_SR@ — H5TC4G63CFR-N0C, SA00007DU10
UV8 H4G_SR@ — H5TC4G63CFR-N0C, SA00007DU10
RV159 H4G_SR@ — 15K_0402_1%, SD03415028J

VRAM_Hynix 4GX4

UV5 M4G_SR@ — MT41J256M16LY-091G:N, SA00007QJ00
UV6 M4G_SR@ — MT41J256M16LY-091G:N, SA00007QJ00
UV7 M4G_SR@ — MT41J256M16LY-091G:N, SA00007QJ00
UV8 M4G_SR@ — MT41J256M16LY-091G:N, SA00007QJ00
RV159 M4G_SR@ — 34.8K_0402_1%, SD03434828J

VRAM_Micron 4GX4

UV5 S4G_DR@ — K4W4G1646E-BC1A, SA000063F20
UV6 S4G_DR@ — K4W4G1646E-BC1A, SA000063F20
UV7 S4G_DR@ — K4W4G1646E-BC1A, SA000063F20
UV8 S4G_DR@ — K4W4G1646E-BC1A, SA000063F20
RV156 S4G_DR@ — 45.3K_0402_1%, SD03445328J
UV9 S4G_DR@ — K4W4G1646E-BC1A, SA000063F20
UV10 S4G_DR@ — K4W4G1646E-BC1A, SA000063F20
UV11 S4G_DR@ — K4W4G1646E-BC1A, SA000063F20
UV12 S4G_DR@ — K4W4G1646E-BC1A, SA000063F20

VRAM_Samsung 4GX8

UV5 H4G_DR@ — H5TC4G63CFR-N0C, SA00007DU10
UV6 H4G_DR@ — H5TC4G63CFR-N0C, SA00007DU10
UV7 H4G_DR@ — H5TC4G63CFR-N0C, SA00007DU10
UV8 H4G_DR@ — H5TC4G63CFR-N0C, SA00007DU10
RV156 H4G_DR@ — 34.8K_0402_1%, SD03434828J
UV9 H4G_DR@ — H5TC4G63CFR-N0C, SA00007DU10
UV10 H4G_DR@ — H5TC4G63CFR-N0C, SA00007DU10
UV11 H4G_DR@ — H5TC4G63CFR-N0C, SA00007DU10
UV12 H4G_DR@ — H5TC4G63CFR-N0C, SA00007DU10

VRAM_Hynix 4GX8

UV5 M4G_DR@ — MT41J256M16LY-091G:N, SA00007QJ00
UV6 M4G_DR@ — MT41J256M16LY-091G:N, SA00007QJ00
UV7 M4G_DR@ — MT41J256M16LY-091G:N, SA00007QJ00
UV8 M4G_DR@ — MT41J256M16LY-091G:N, SA00007QJ00
RV156 M4G_DR@ — 15K_0402_1%, SD03415028J
UV9 M4G_DR@ — MT41J256M16LY-091G:N, SA00007QJ00
UV10 M4G_DR@ — MT41J256M16LY-091G:N, SA00007QJ00
UV11 M4G_DR@ — MT41J256M16LY-091G:N, SA00007QJ00
UV12 M4G_DR@ — MT41J256M16LY-091G:N, SA00007QJ00

VRAM_Micron 4GX8

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Title: *Virtual symbol*

Size: Custom | Document Number: CG413 | Rev: 1.0

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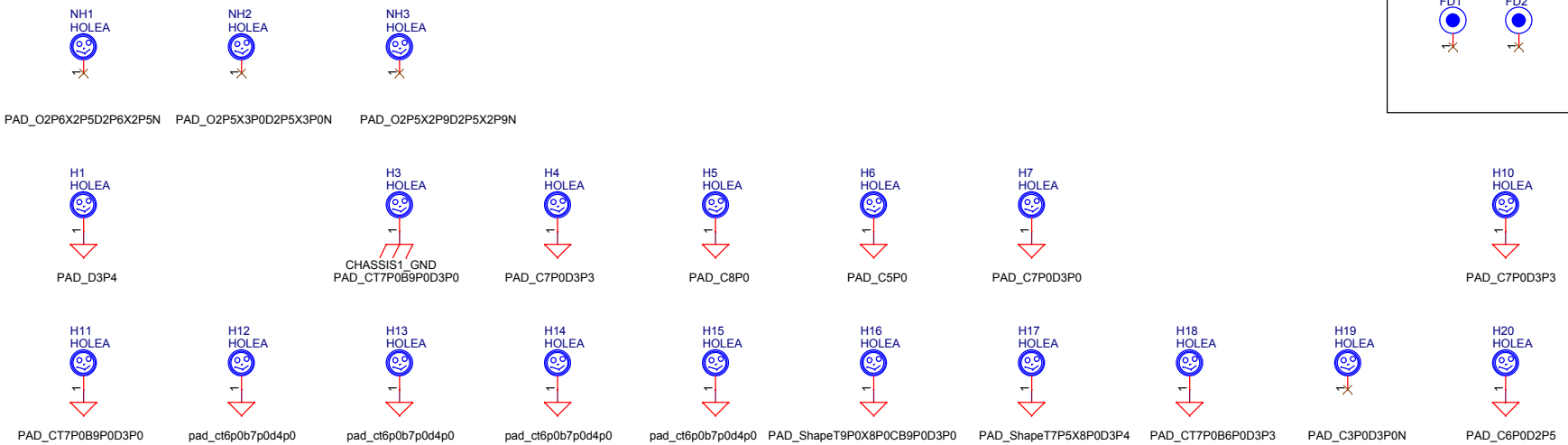

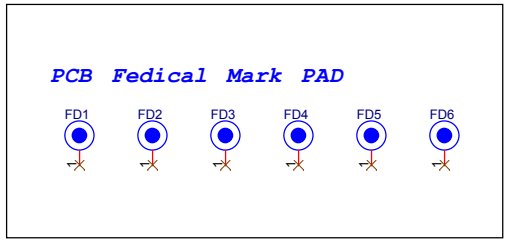

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Title: **Hole**

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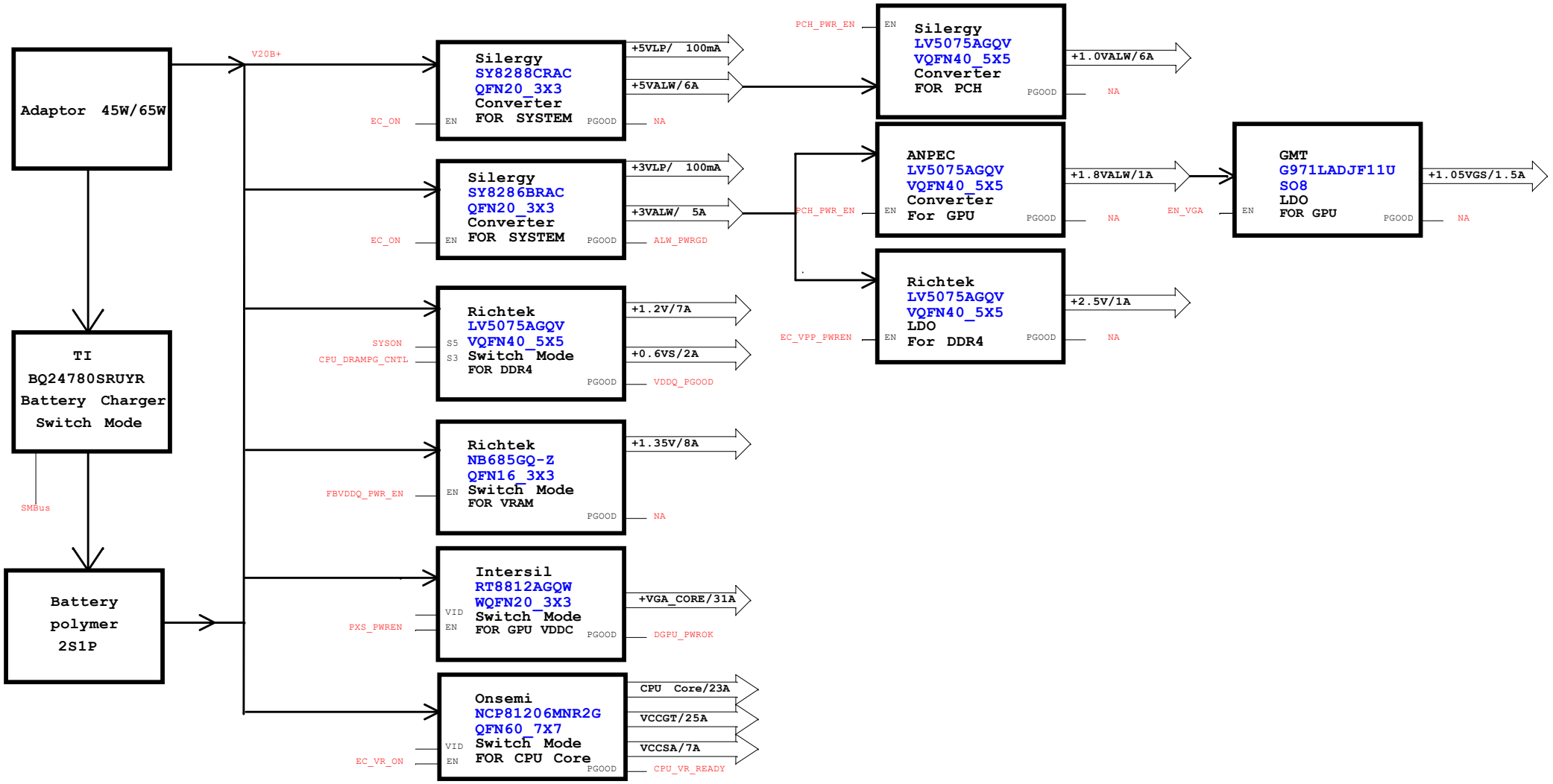

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Title: **PWR-Power Diagram**

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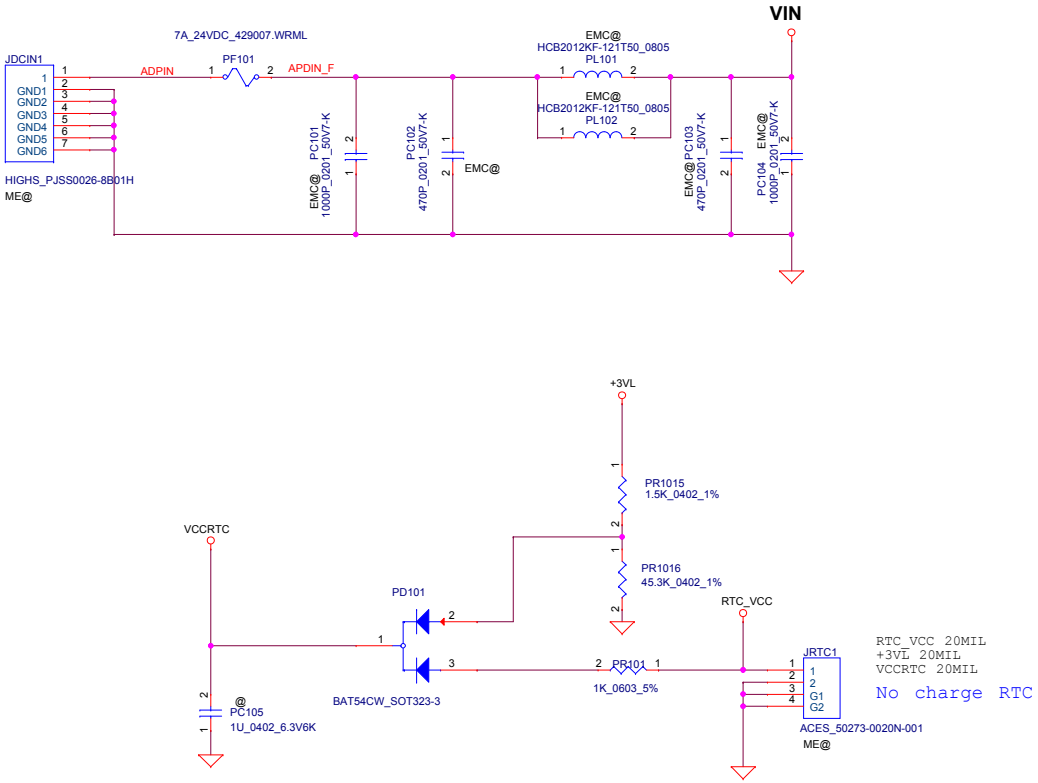

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Title: **PWR-DCIN / RTC charger**

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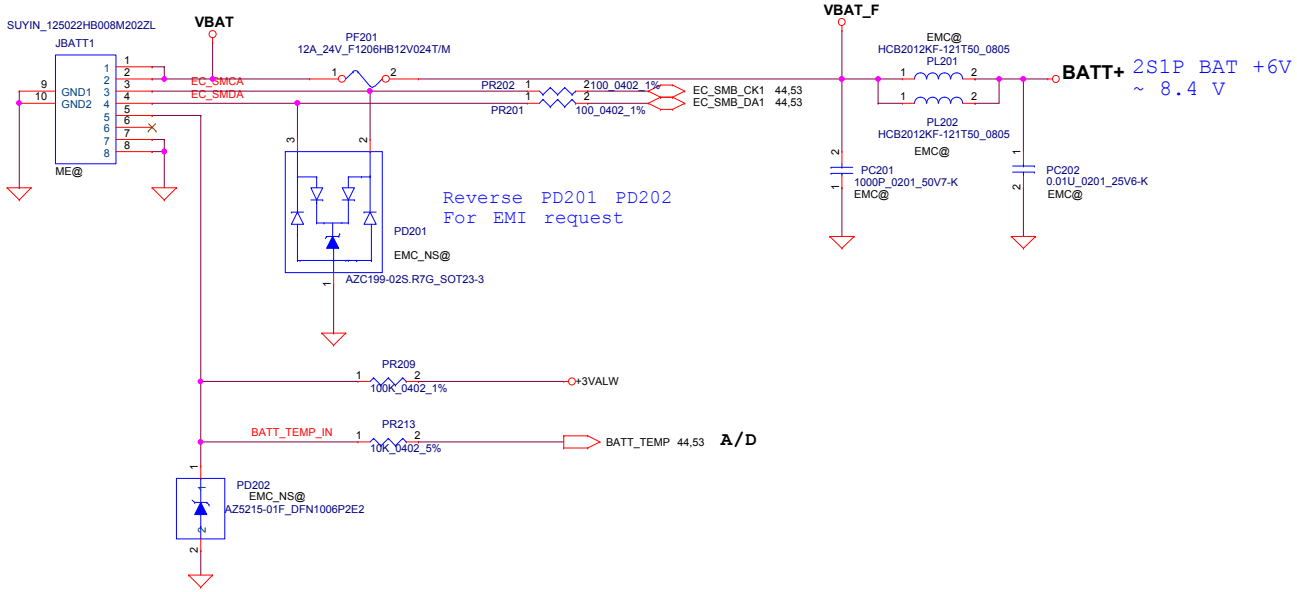

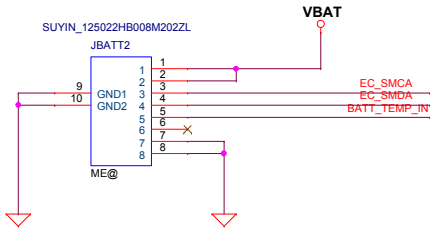

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Title: PWR-BATTERY CONN/OTP

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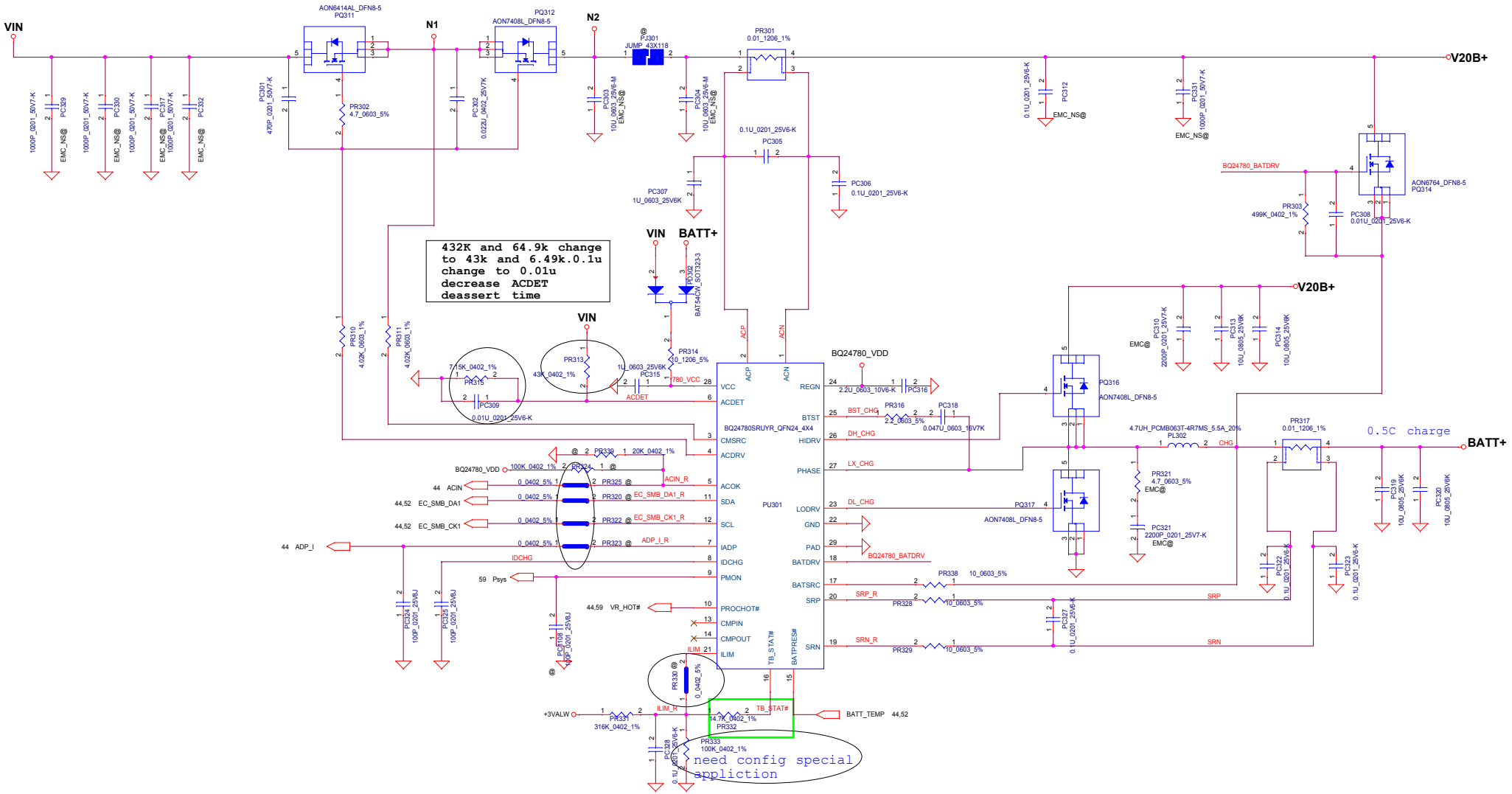

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Title: **PWR-CHARGER**

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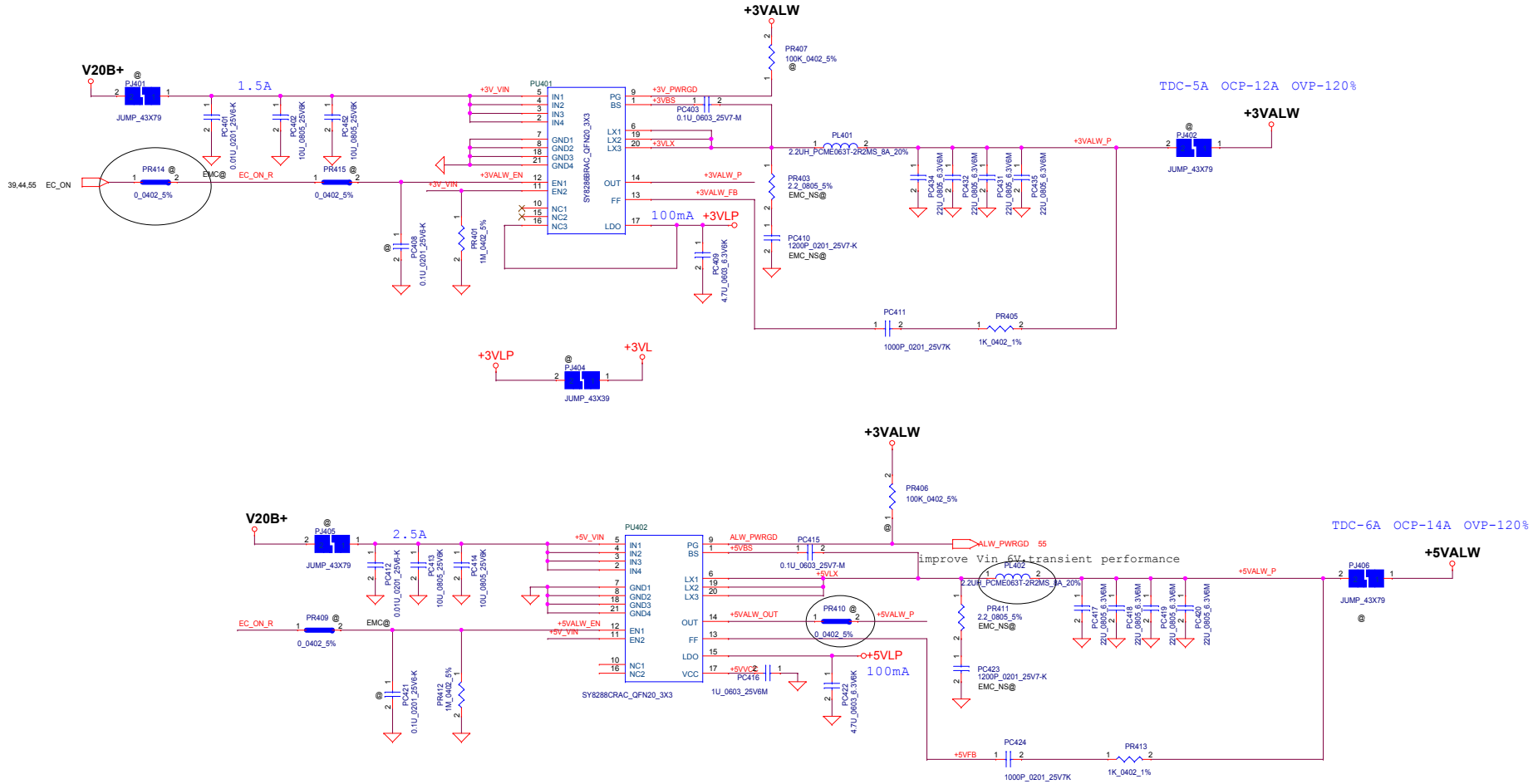

6800pf soft start 2ms
47nf soft start 7ms

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Title: PWR_3VALW/5VALW

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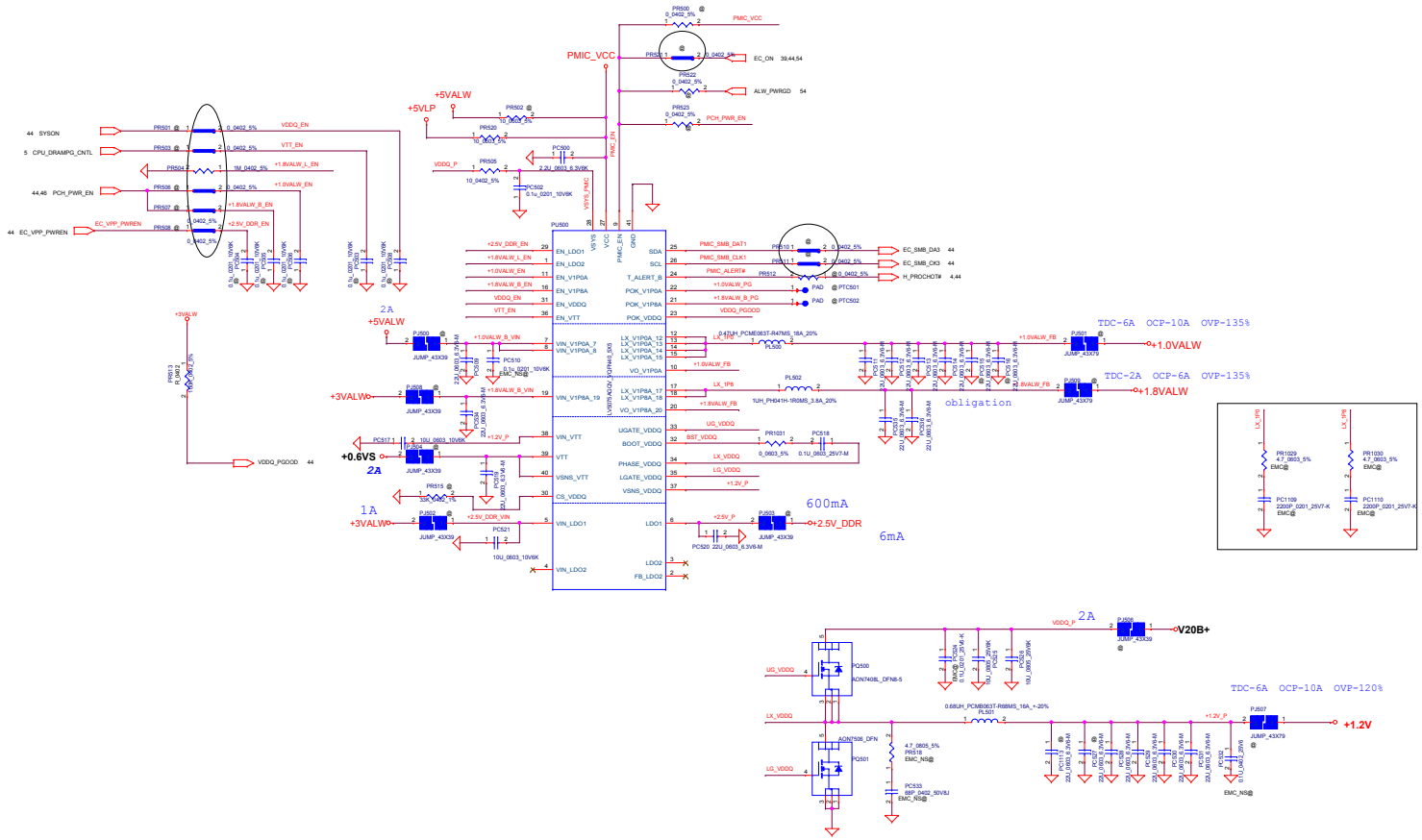

Security Classification	LC Future Center Secret Data		Title
Issued Date	2015/08/20	Deciphered Date 2016/08/20	PWR PMIC-DDR4/1.0ALW/1.8ALW

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Title

PWR

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Custom	CG413	1.0

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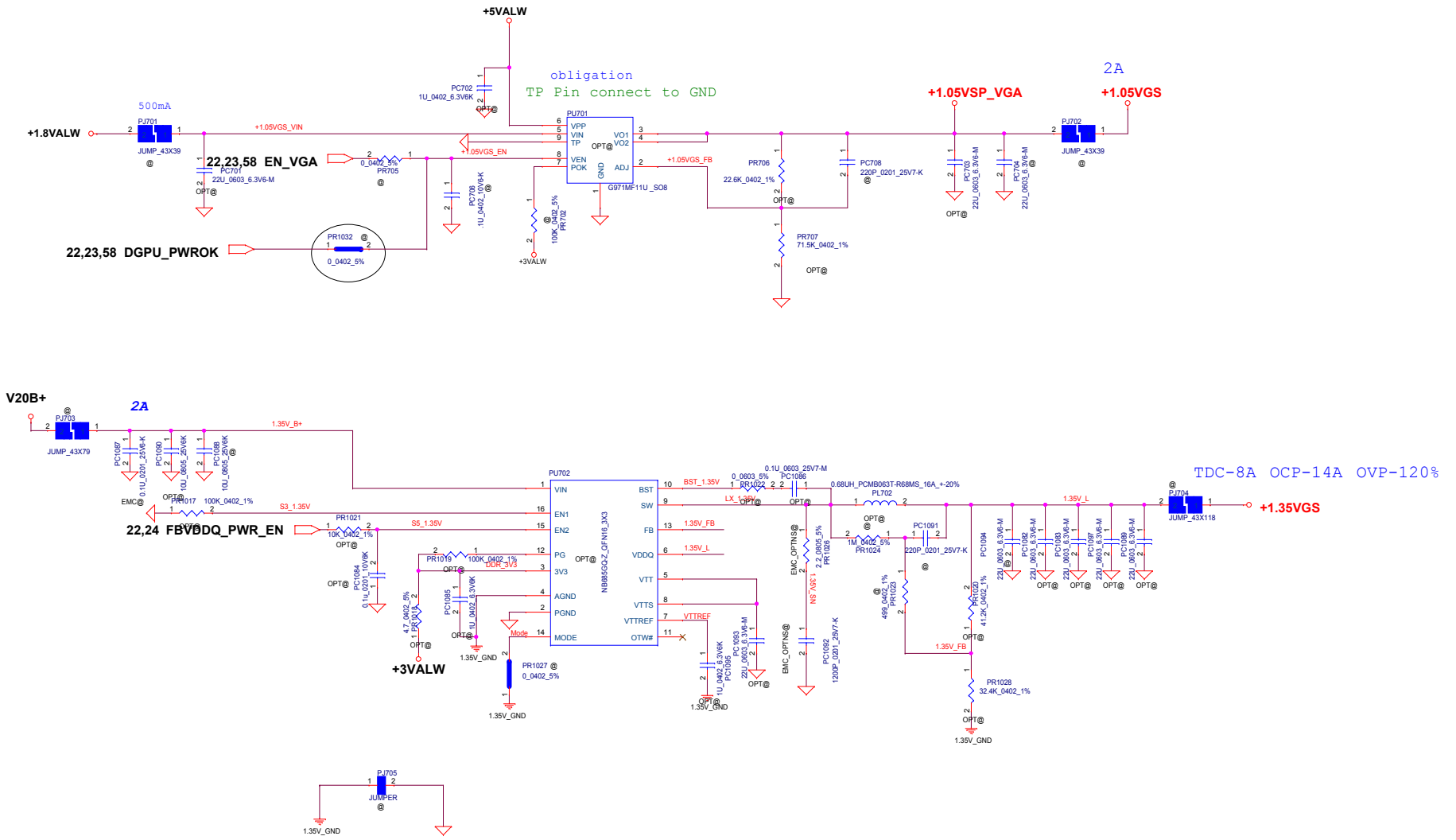

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: PWR-+1.05VGS/+1.35V_VRA

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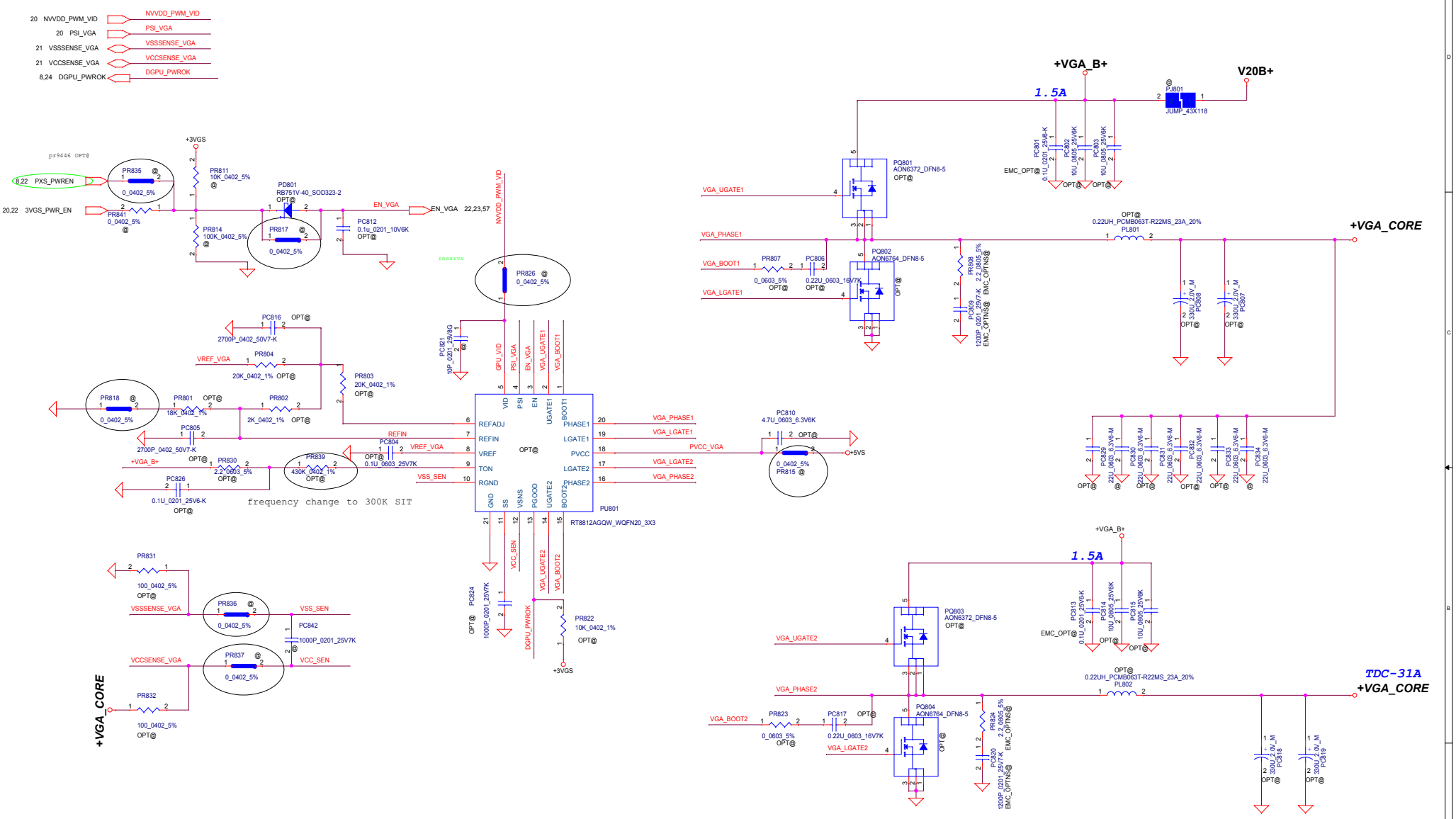

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Title: **PWR-VGA_CORE**

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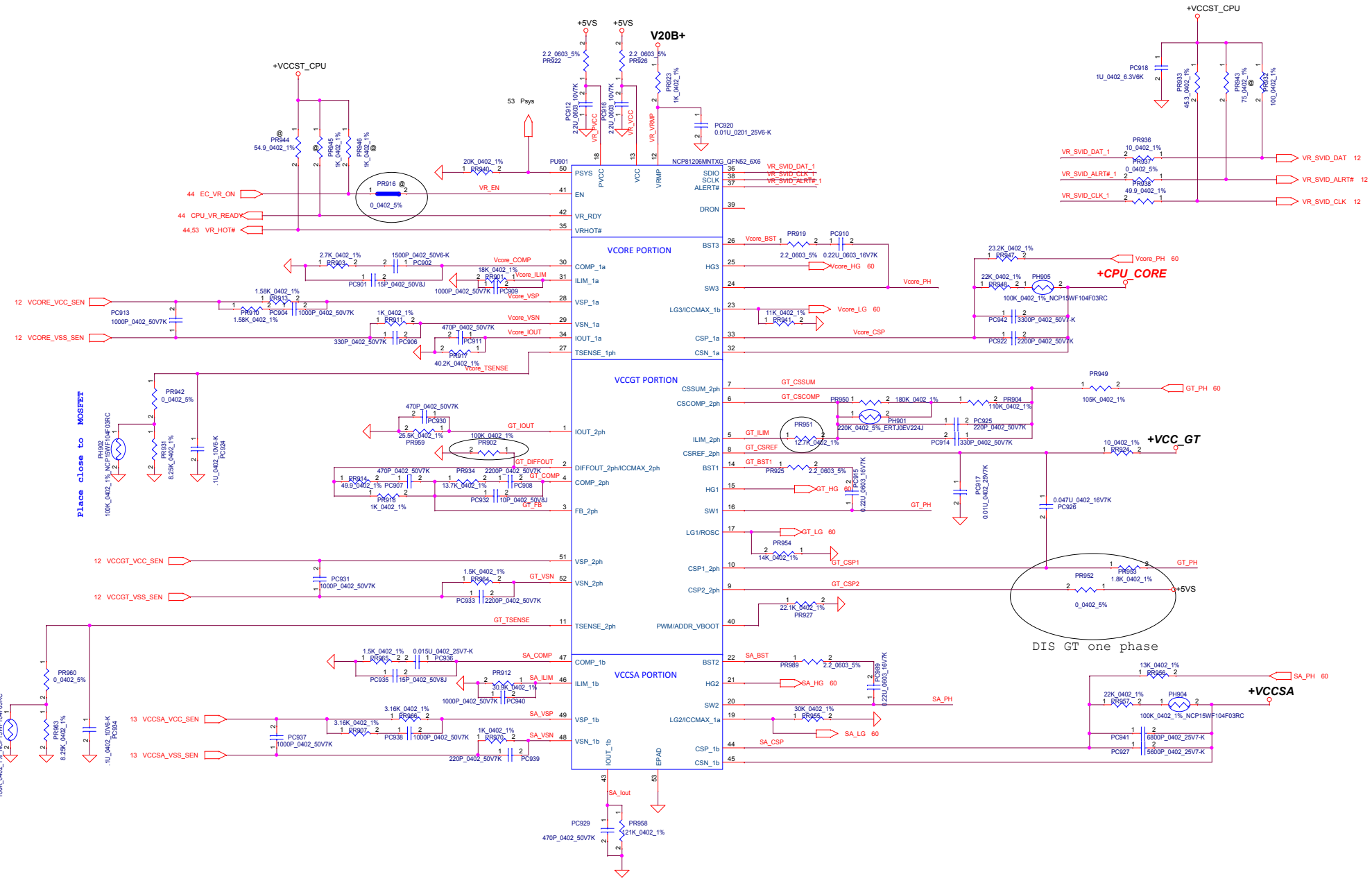

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Title: **PWR_CPU_CORE1**

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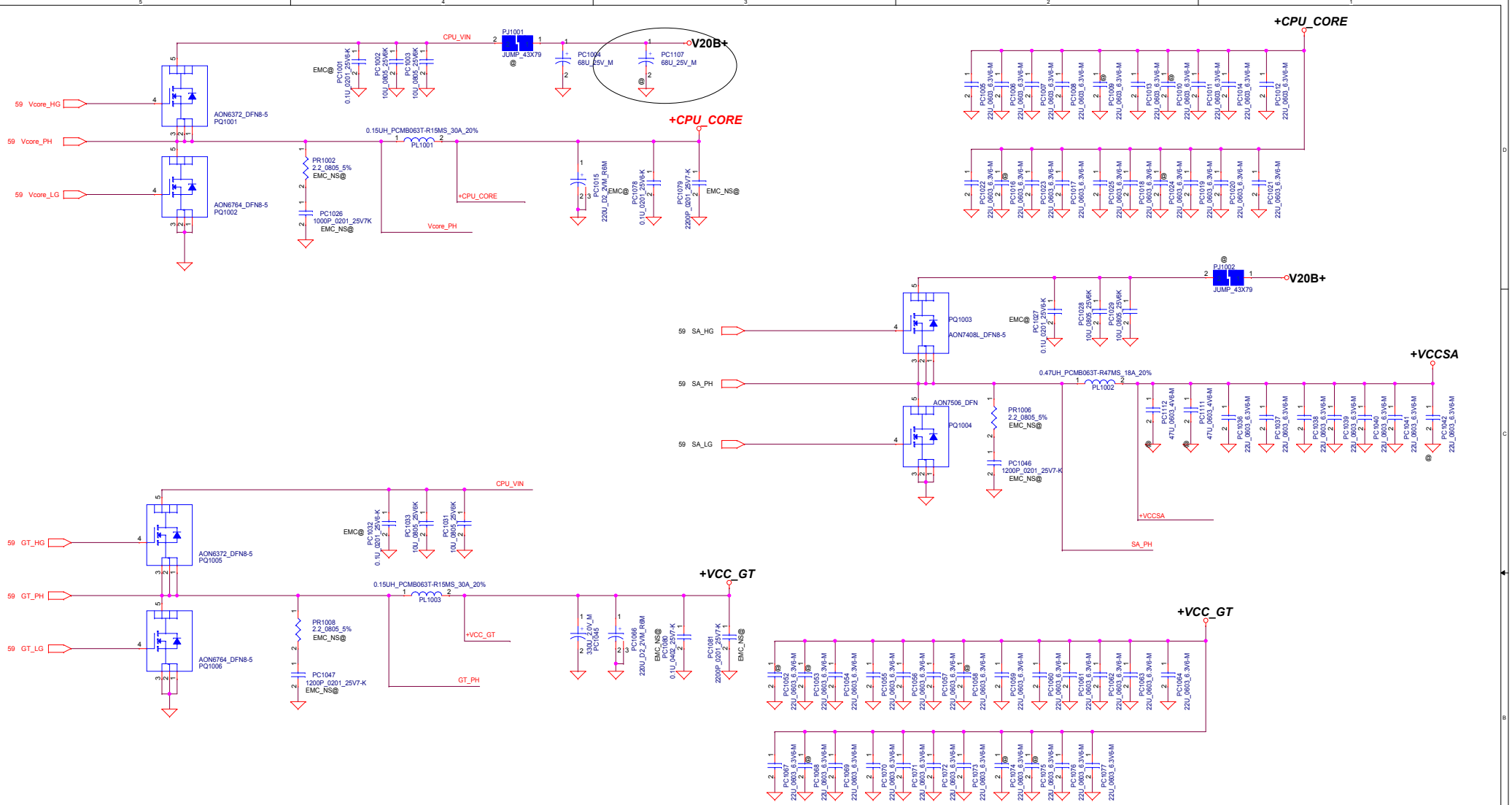

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Title: PWR_CPU_CORE2

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