

1. Schematic Page Description :

ZHS/BTM-origins Schematic Ver :

- | | |
|---------------------------------|---------------------------------|
| 01 -- Sch Page description | 21 -- WIFI/BT(NGFF)/Video Codec |
| 02 -- Block Diagram | 22 -- eMMC |
| 03 -- Valley 1/9 (DDRA) | 23 -- TPM /LED |
| 04 -- Valley 2/9 (DDRB) | 24 -- DB /Thermal sensor |
| 05 -- Valley 3/9 (Display) | 25 -- Audio Codec |
| 06 -- Valley 4/9 (SD/PCIE/SATA) | 26 -- USB3/Charger/Hole |
| 07 -- Valley 5/9 (SPI/GPIO/CLK) | 27 -- KB/TP/HW RST |
| 08 -- Valley 6/9 (USB/LPC/I2C) | 28 -- KBC |
| 09 -- Valley 7/9 (Power 1) | 29 -- Charger (BQ24715RGRR) |
| 10 -- Valley 8/9 (Power 2) | 30 -- SYSTEM 5V/3V (MPS670/671) |
| 11 -- Valley 9/9 (GND) | 31 -- Load Switch |
| 12 -- BTM XDP & APS | 32 -- DDR 1.35V(TPS51216) |
| 13 -- DDR3L MEMORY DOWNx16 CHA | 33 -- +1.05V/+1V(TPS54318) |
| 14 -- DDR3L MEMORY DOWNx16 CHB | 34 -- +VCC_CORE(ISL95833) |
| 15 -- Level Shifter (SOC_EC) | 35 -- LDO-1 (G9661) |
| 16 -- Level Shifter (SOC_DEV) | 36 -- LDO-2 (G9661) |
| 17 -- SDIO CardReader | 37 -- Thermal protect |
| 18 -- LCD/CCD/DMIC | 38 -- Power Sequence |
| 19 -- Google Debug | 39 -- SMBUS/I2C |
| 20 -- HDMI | 40 -- BTM PWR TREE |
| | 41 -- Change List |

I2C table

Function	Channel	Read	Write
Touch pad	I2C0	0x67	
Audio codec	I2C1	0x21	0x20
Light sensor	I2C4		

SMBus table

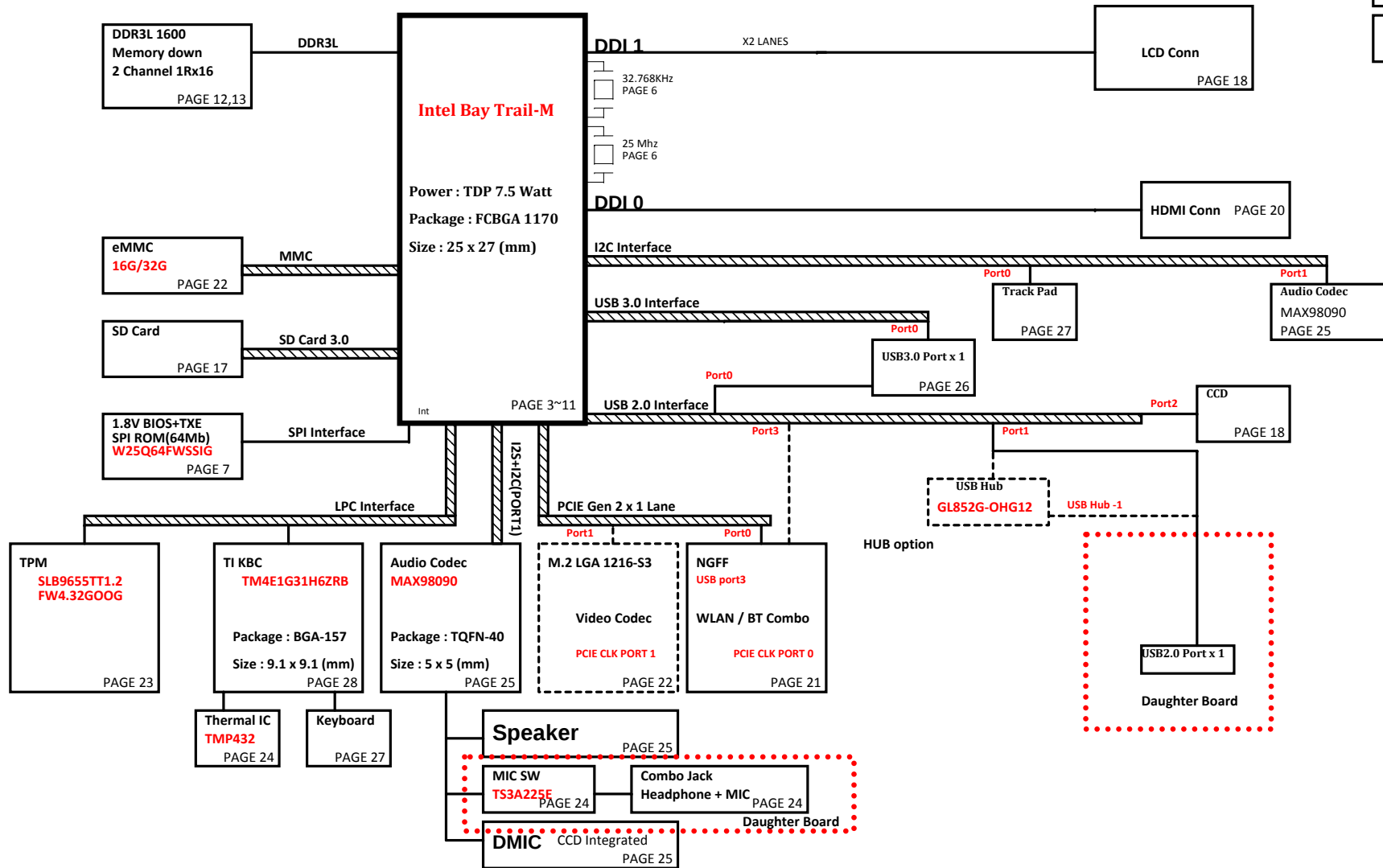
Function	Channel	Address
Battery	SMB0	
Thermal	SMB2	0x4C

Function	Channel
PP3300_DSW	0x42
PP5000	0x41
PP1350	0x49
PP1050_PCH	0x43
PP1000_PCH	0x47

ZHR/BTM-Origins

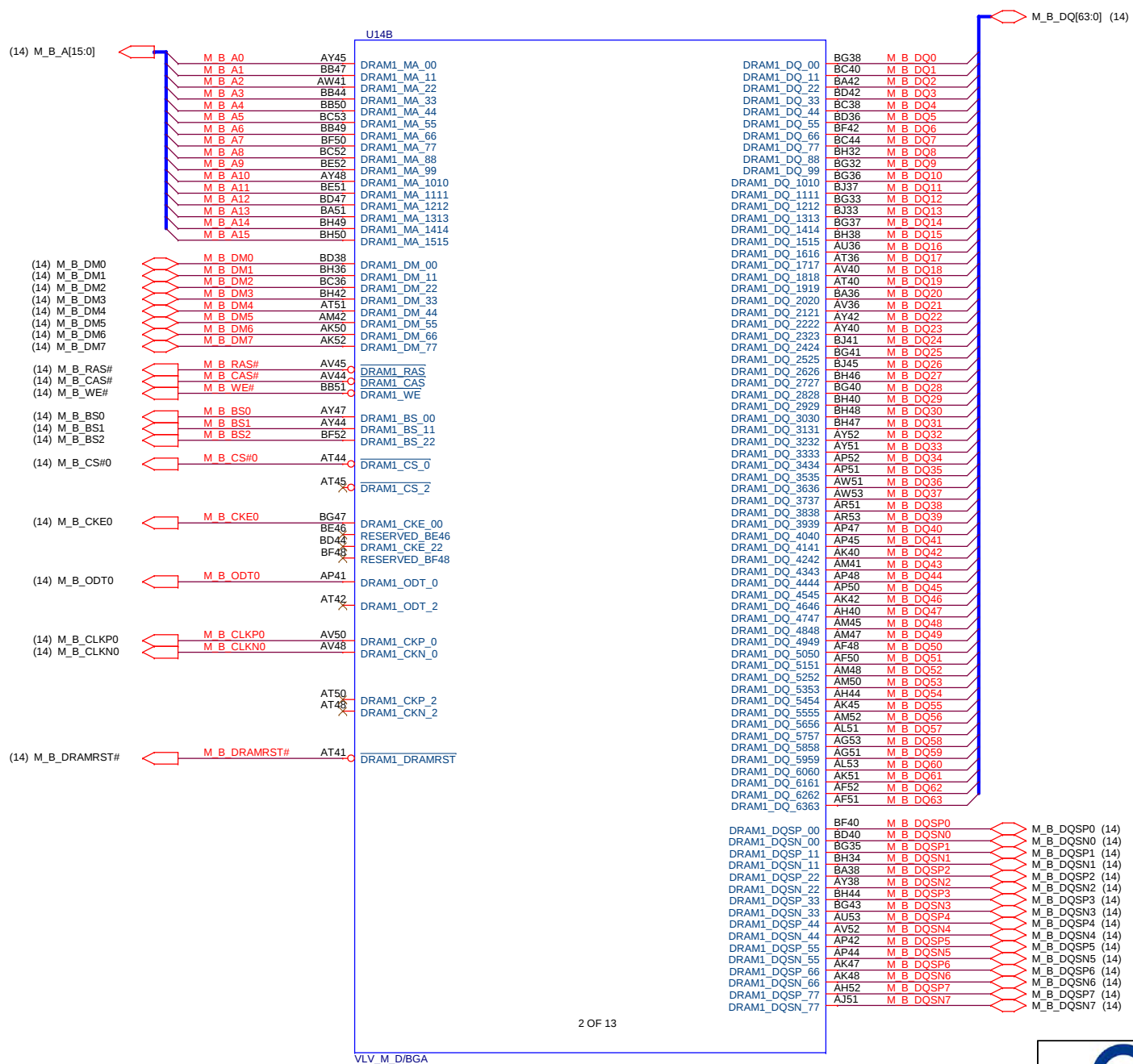
Intel Bay Trail-M Platform Block Diagram

SKU# DC N2820
AJSR1SGUT03 --CPU(1170P)N2820 2.13G SR1SG(FCBGA)STNBSQ

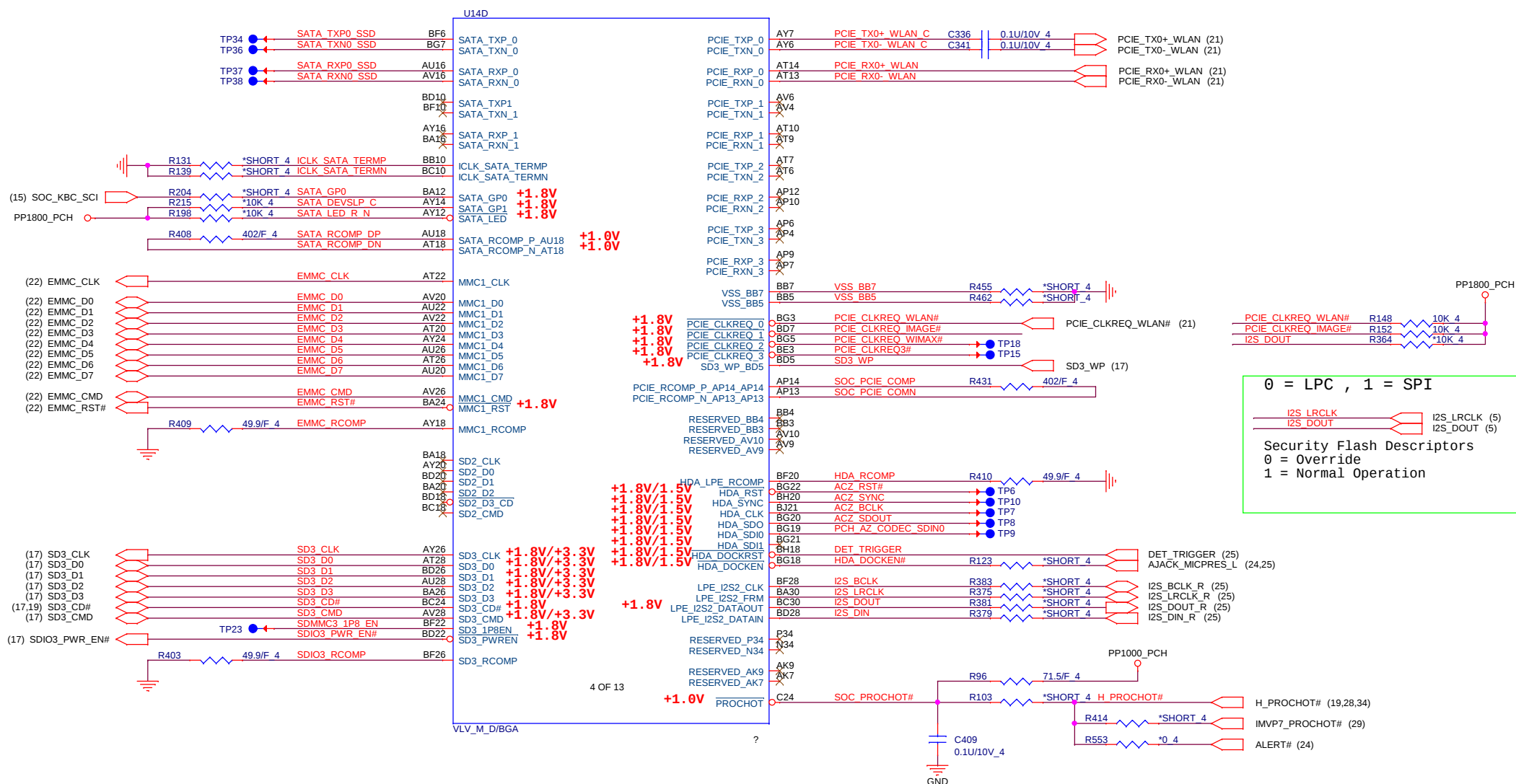


BQ24715 Battery Charger	TPS51216 PP1350
TPS51225 PP3300_DS0WPP5000	NB671GQ-Z PP1000_PCH
ISL95833HRTZ-T +VCC_CORE+VCC_GFX	Thermal Protection Discharger

BOM value option:
 SX@ => SOiX
 NSX@=>none SOiX
 HUB@=>USB HUB
 3G@ => LTE
 GD@ =>Google debug



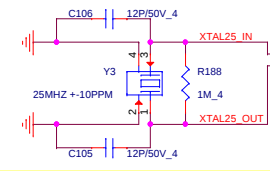
Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is unchanged 1 = Top address bit is inverted	
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC 1 = SPI	
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override 1 = Normal operation	
DDI0_DDCDATA	DDI0 Detect	PWROK	0 = DDI0 not detected 1 = DDI0 detected	
DDI1_DDCDATA	DDI1 Detect	PWROK	0 = DDI0 not detected 1 = DDI0 detected	
GPIO_SO_NC_13				



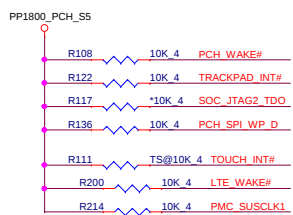
Quanta Computer Inc.
PROJECT : ZHS

Size	Document Number	Rev
	Valley 4/9 (SD/PCIe/SATA)	1A
Date:	Monday, August 10, 2015	Sheet 6 of 42

CRYSTAL 25MHZ



2nd BG625000121(HHE)



(21) CLK_PCIE_WLANN

(21) CLK_PCIE_WLANNP

(25) I2S_MCLK

(28) KBD_IRQ#

(12) SRT_CRST#

(12) XDP_H_TCK

(12) XDP_H_TRST#

(12) XDP_H_TMS

(12) XDP_H_TDI

(12) XDP_H_TDO

(12) XDP_H_PRODY#

(12) XDP_H_FREQ#_C

(28) PCH_WAKE_L

(27) TRACKPAD_INT#

(16) TOUCH_INT#

(15) SOC_KBC_SMI

(25) MUX_AUD_INT1#

(16) WIFI_DISABLE#

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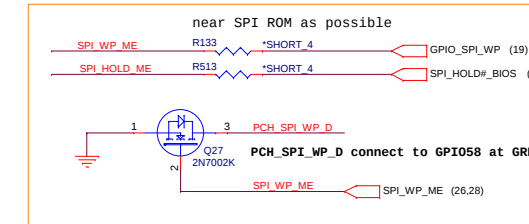
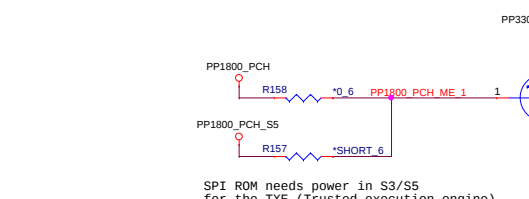
(16) WIFI_DISABLE#

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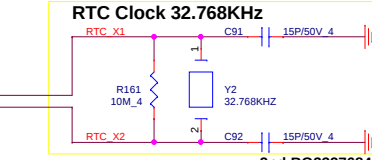
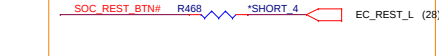
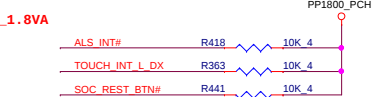
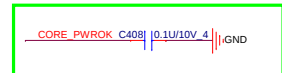
SPI_FLASH



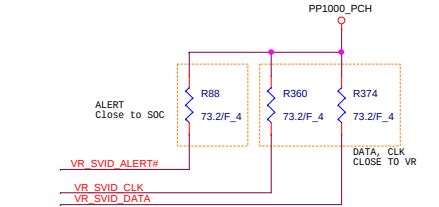
To debug header

To PCH

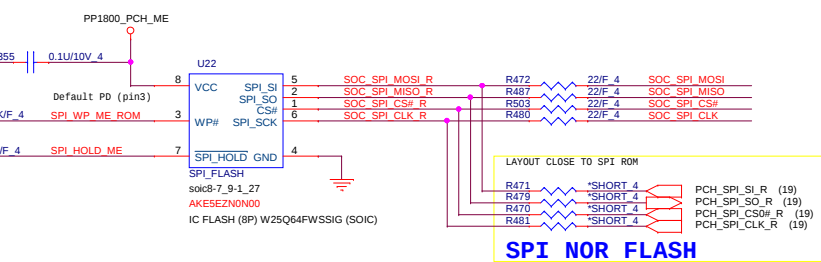
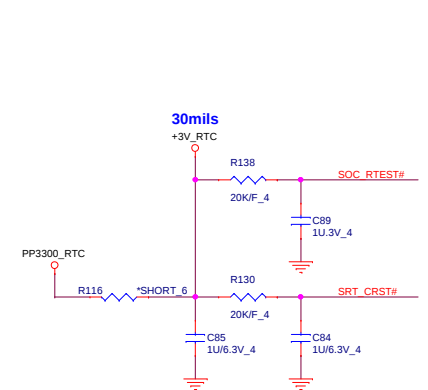
From Screw/EC



2nd BG332768453

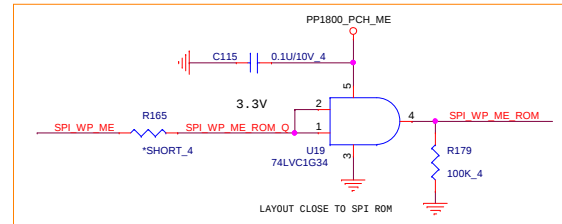


RTC Circuitry(RTC)



LAYOUT CLOSE TO SPI ROM

SPI NOR FLASH



LAYOUT CLOSE TO SPI ROM

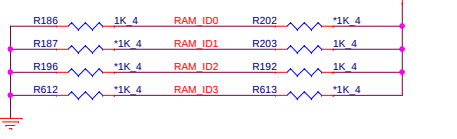
5/19 Update RAM ID for ZHQ and ZHS use.

Vender	RAM_ID	Q P/N	Mfr. PN	Freq.	Size	Pice
Samsang	0x000	AKD5PGST514	K4B4G1646Q-HYK0	1600MHZ	4GB	8
Hynix	0x001	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHZ	4GB	8
Micron	0x010	AKD5DGLT07	MT41K128M16JT-125H:K	1600MHZ	2GB	8
Hynix	0x011	AKD5PGSTW03	H5TC4G63MFR-PBA	1600MHZ	2GB	4
Hynix	0x100	AKD5PGSTW13	H5TC4G63CFR-PBA	1600MHZ	2GB	4
Hynix	0x101	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHZ	2GB	4
Hynix	0x110	AKD5PGSTW13	H5TC4G63CFR-PBA	1600MHZ	4GB	8
Hynix	0x111	AKD5PGSTW03	H5TC4G63MFR-PBA	1600MHZ	4GB	8

C2 SKU1

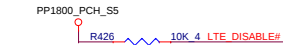
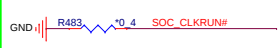
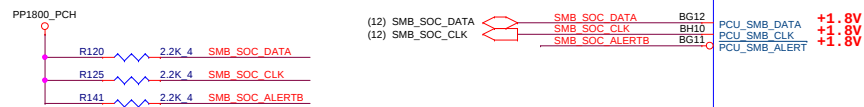
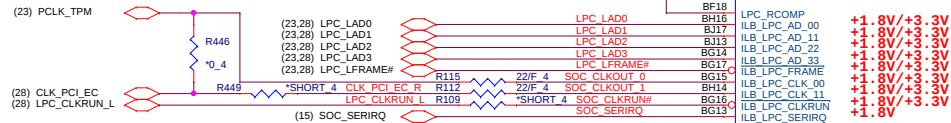
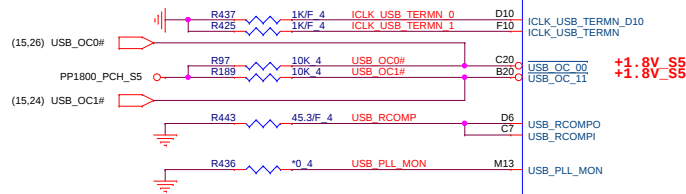
C2 SKU2

RAM ID



PORT 1 USB CONN
PORT 2 LTE
PORT 3 NA
PORT 4 NA

MB USB3.0
HUB1
CCD
BT



C2

GPIO_S5_31

GPIO_S5_32

GPIO_S5_33

GPIO_S5_34

GPIO_S5_35

GPIO_S5_36

GPIO_S5_37

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GPIO_S5_310

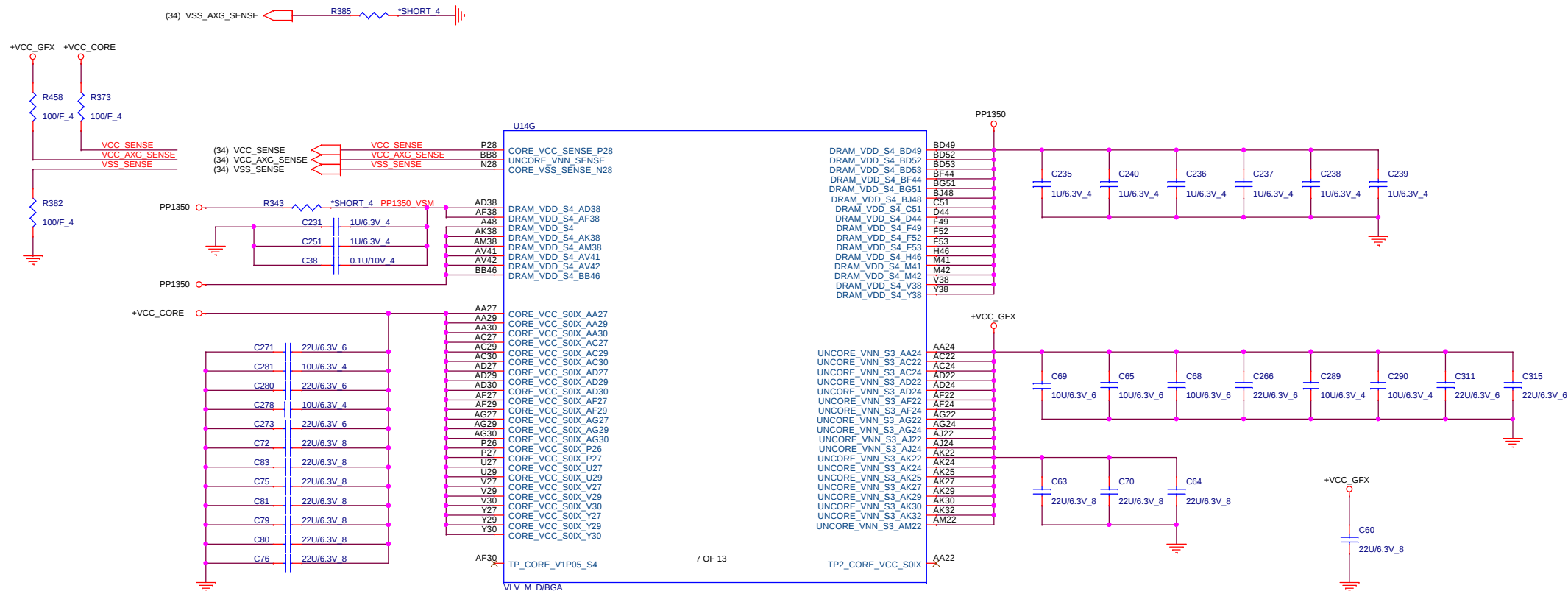
GPIO_S5_311

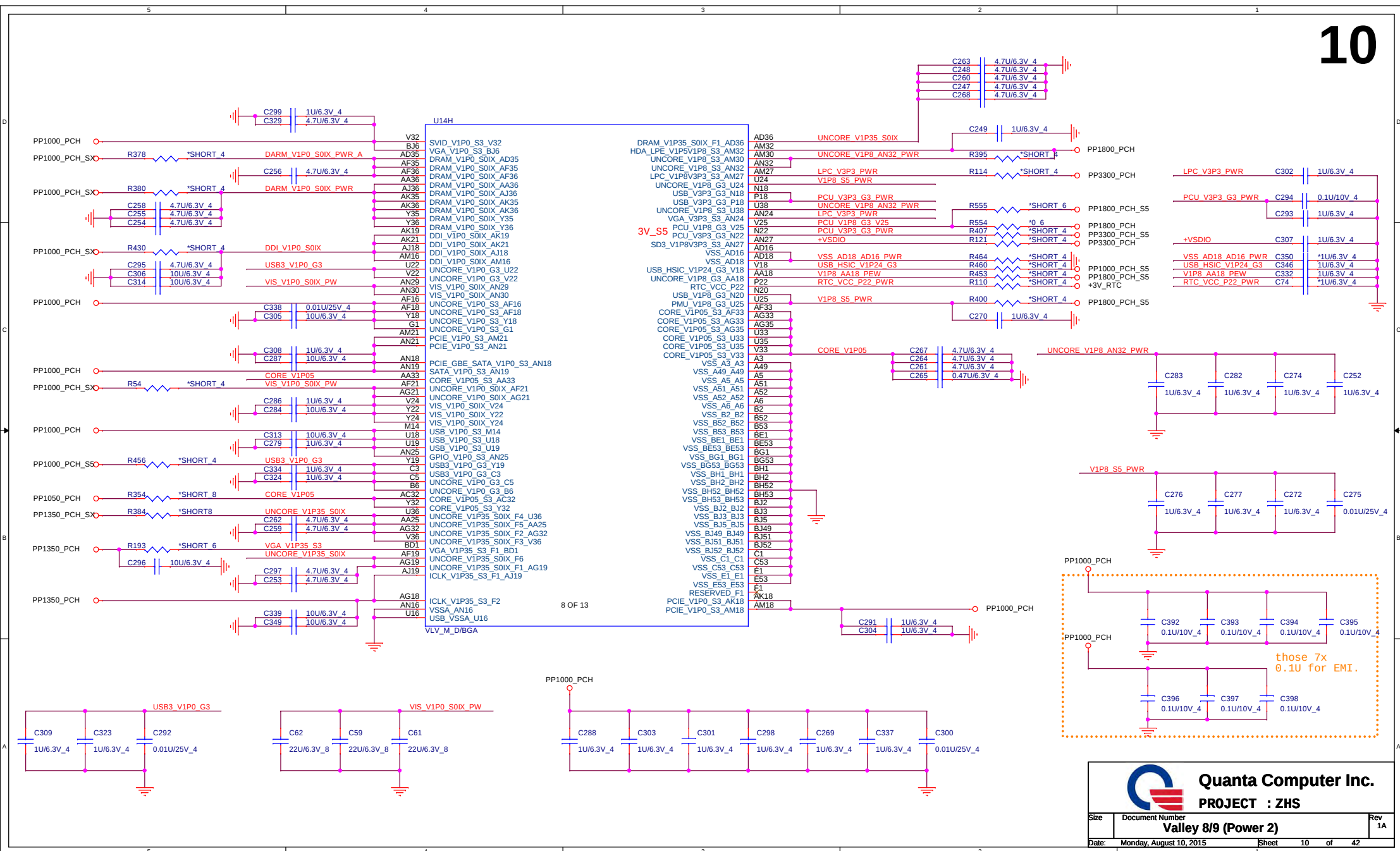
GPIO_S5_312

GPIO_S5_313

GPIO_S5_314

GPIO_S5_315





12

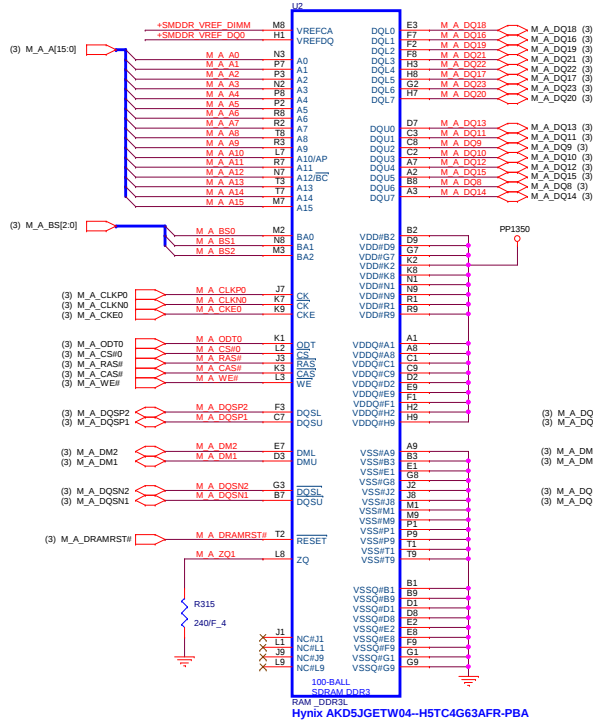


Size	Document Number	Rev
	CPU XDP / APS	1A
Date:	Monday, August 10, 2015	Sheet 12 of 42

<DDR>

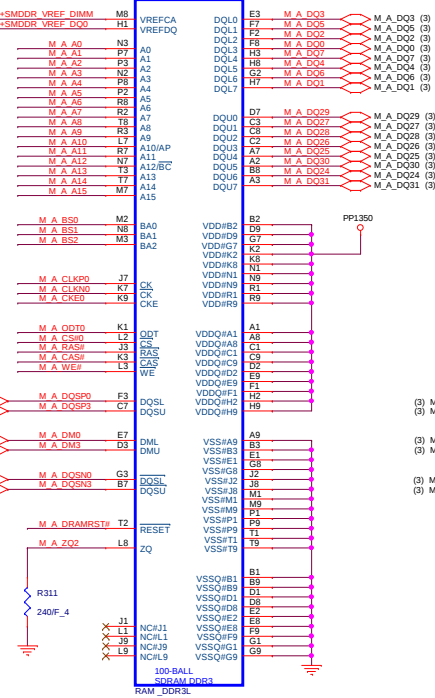
BYTE2_16-23

BYTE1_8-15



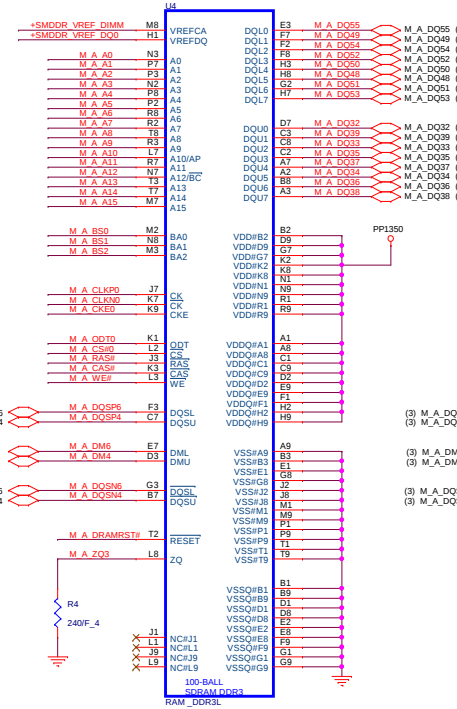
BYTE0_0-7

BYTE3_24-31



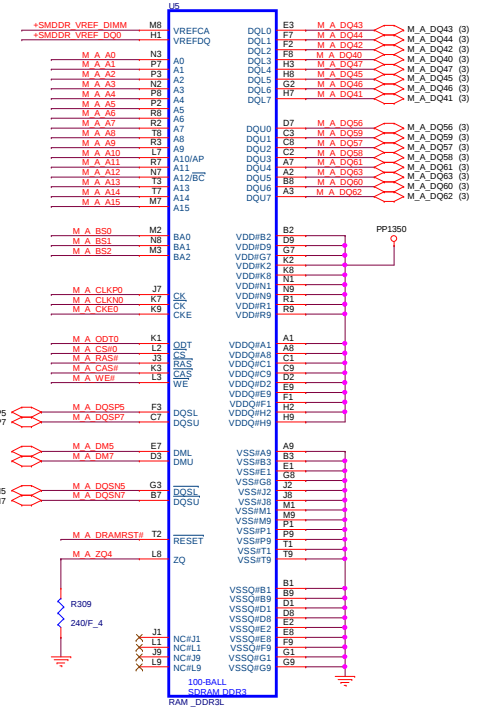
BYTE4_32-39

BYTE6_48-55



BYTE5_40-47

BYTE7_56-63

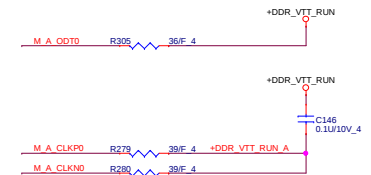


Distributed around all DRAM devices (CHA and CHB)

Place these Caps near each X16 Memory Down

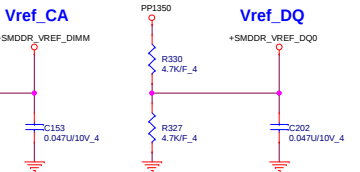
C325/C326 are for EMI request

Place these Caps near Memory Down CA & DQ pin



M1 solution

M1 solution



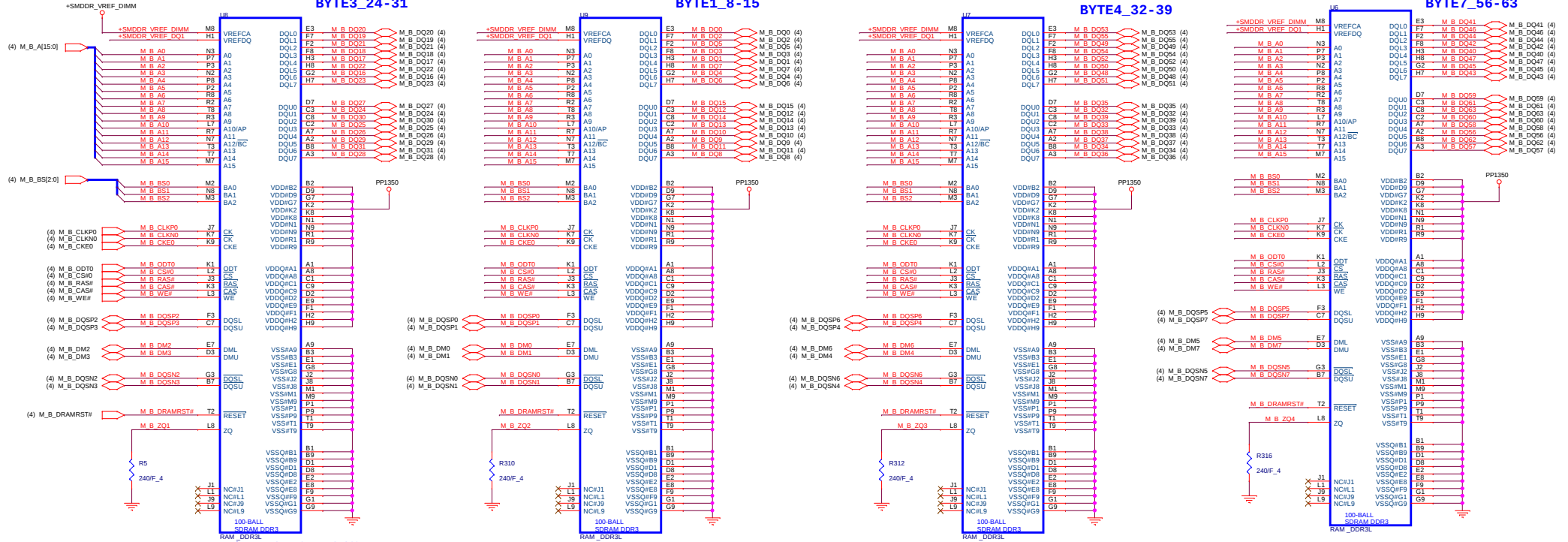
<DDR>

BYTE16_23
BYTE24_31

BYTE0_7
BYTE18_15

BYTE6_48-55
BYTE4_32-39

BYTE5_40-47
BYTE7_56-63

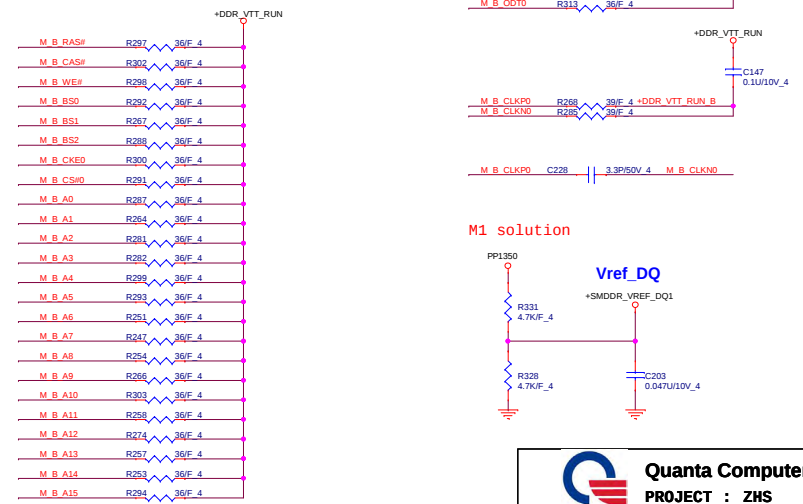
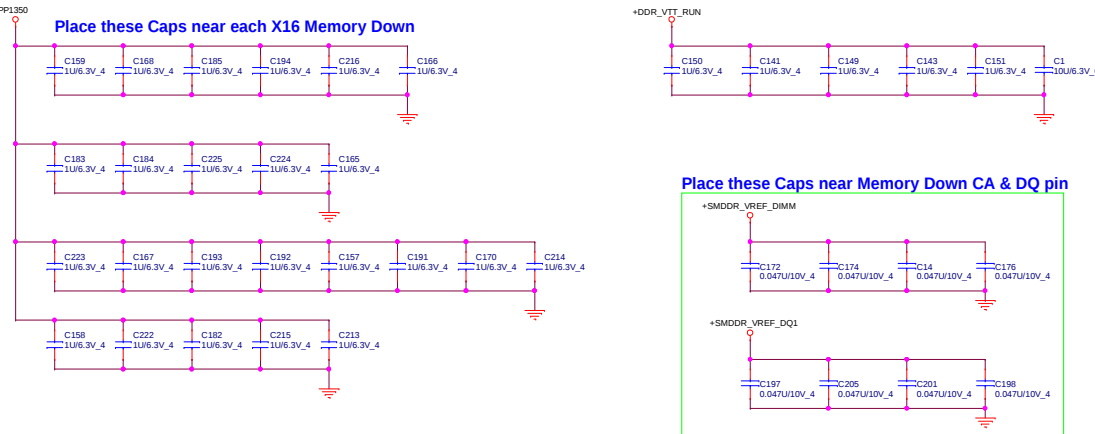


Hynix AKD5JGETW04-H5TC4G63AFR-PBA

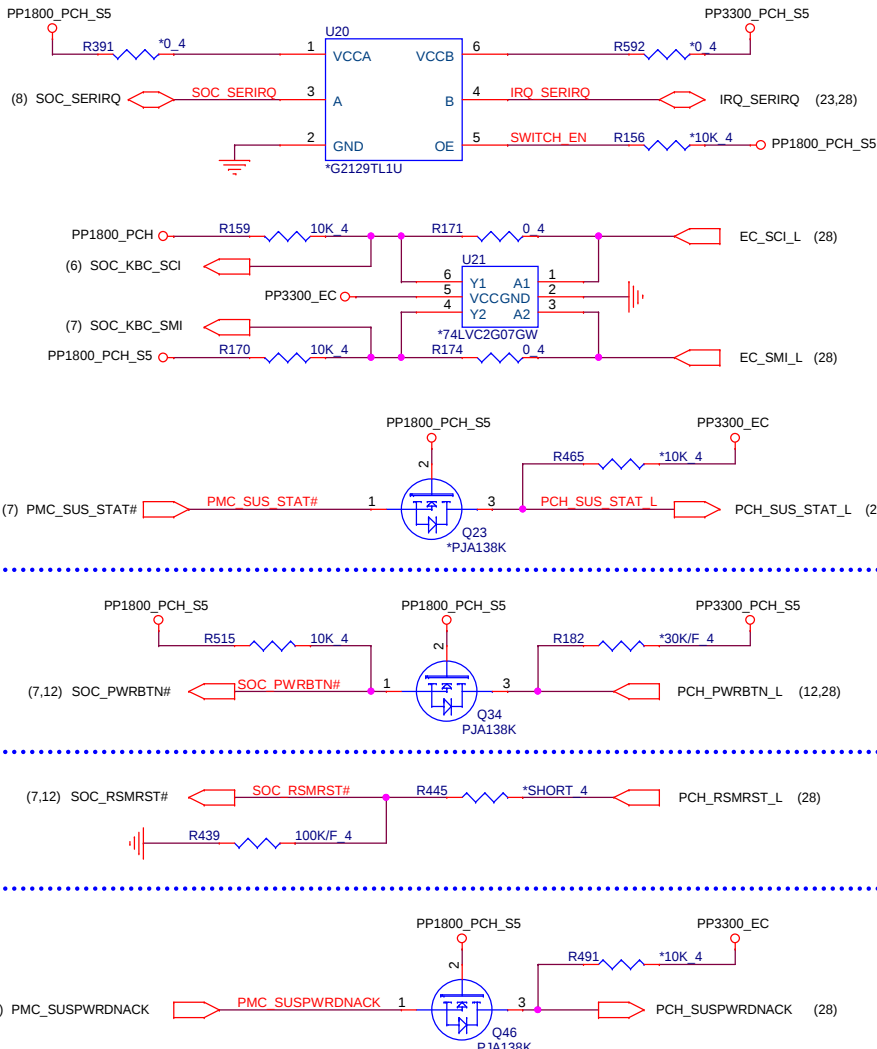
Vendor	P/N	
Hynix	AKD5JGETW04	DDR3L 1600MHz 4Gb
Elpida	AKD5JGST400	DDR3L 1333MHz 4Gb
	AKD5JGST404	DDR3L 1333MHz 4Gb

Place these Caps near each X16 Memory Down

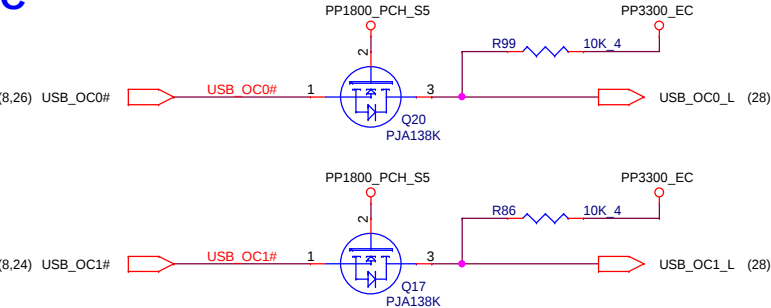
Place these Caps near Memory Down CA & DQ pin



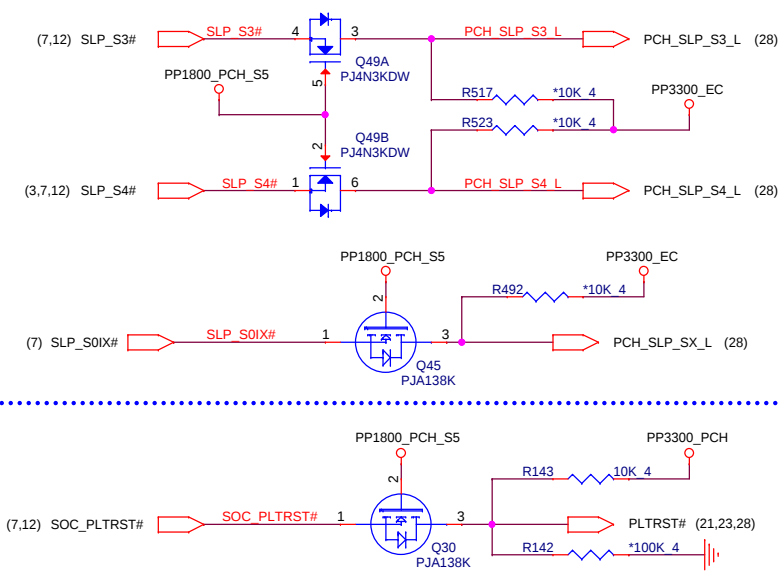
PWRON SEQUENCE



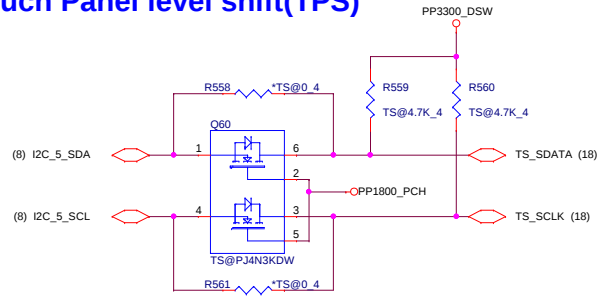
USB OC



PWRON SEQUENCE

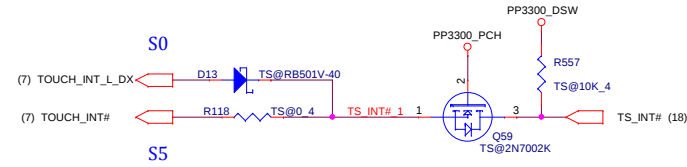


Touch Panel level shift(TPS)

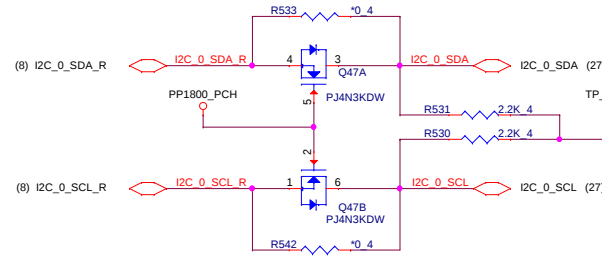


LTE

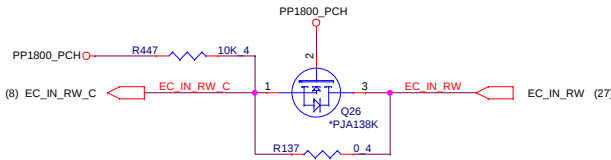
Touch Screen(TPS)



Track Pad

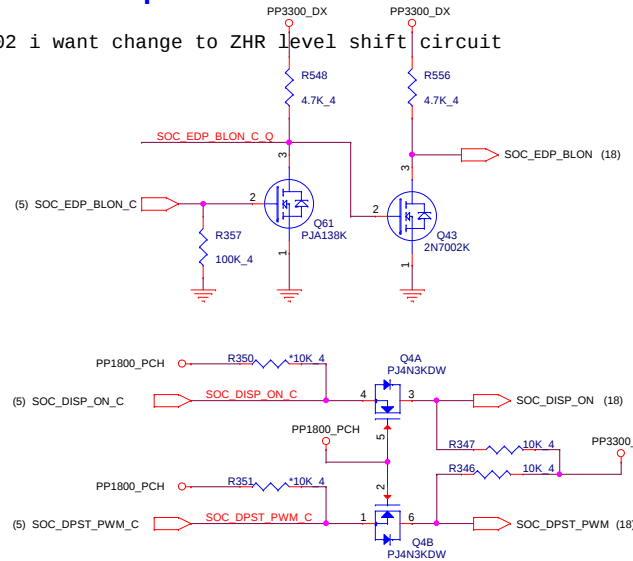


HW RESET

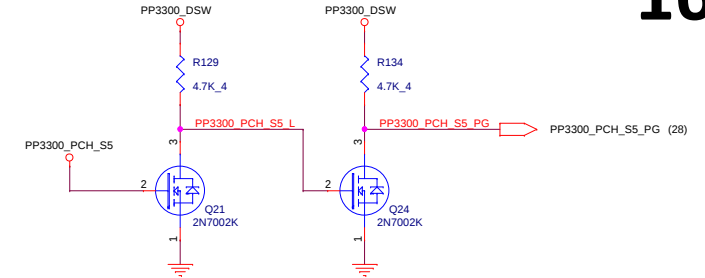


eDP control pin

0402 i want change to ZHR level shift circuit

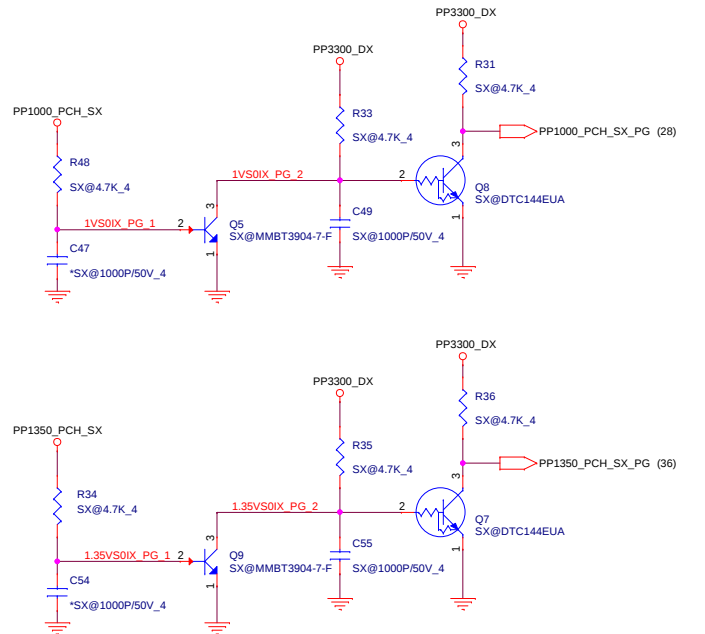


S5 Power Good(+3V_S5)

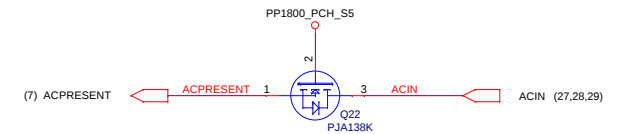


S0iX Power Good

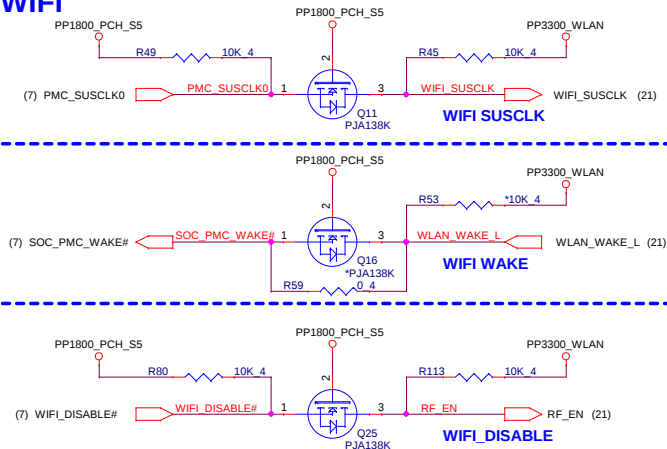
for proto type only, can remove at MP stage if S0ix is not needed



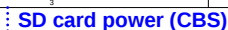
AC Detect



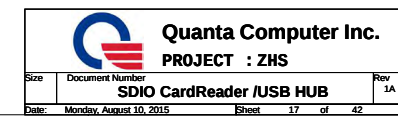
WIFI



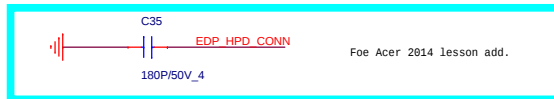
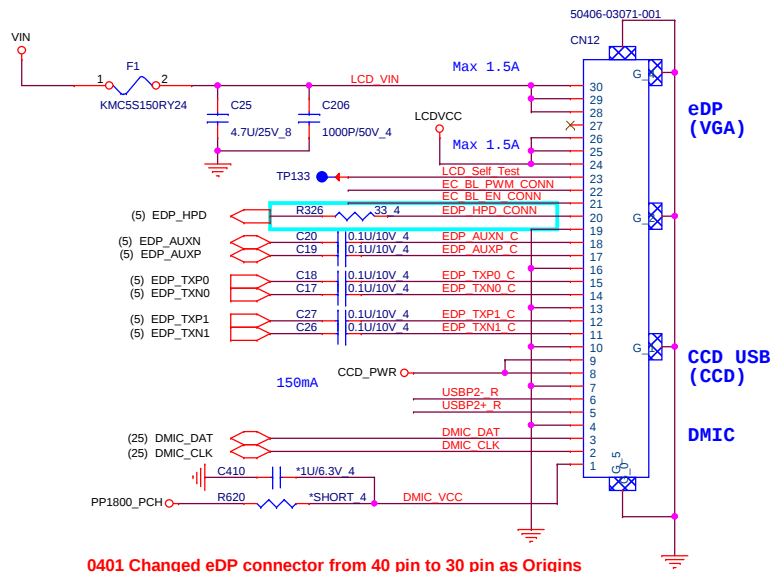
**This is full size SD card
(push-push type)**



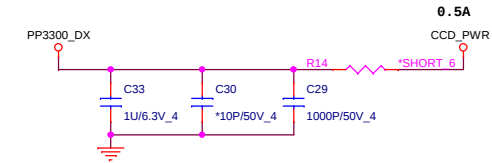
17



LCD CONN



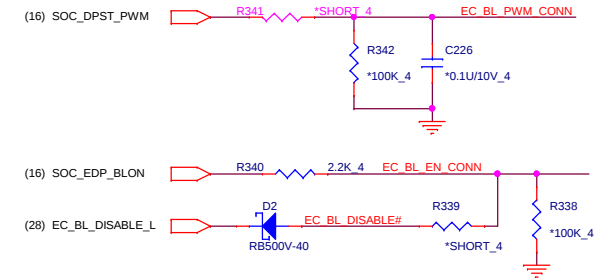
CCD Power(CCD)



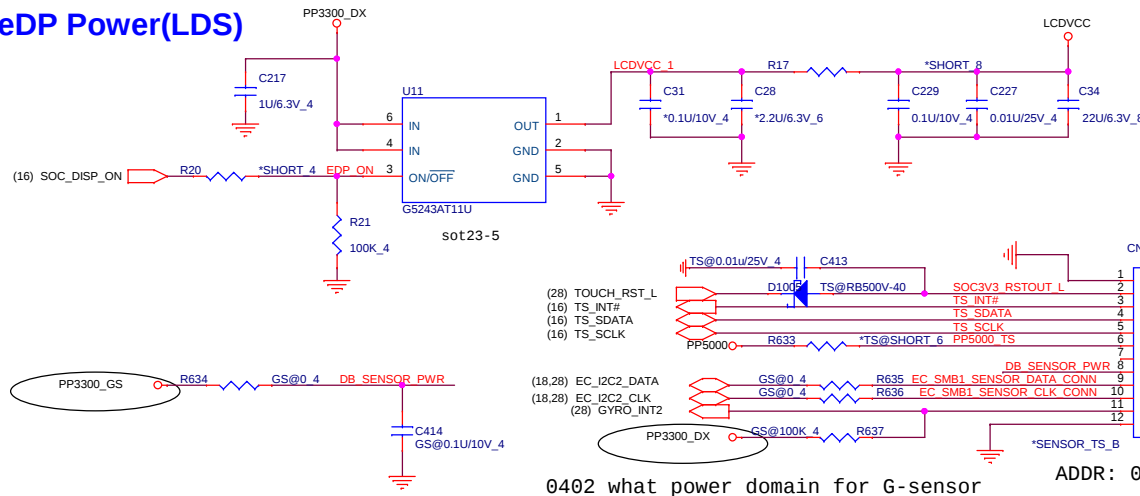
CCD USB(CCD)



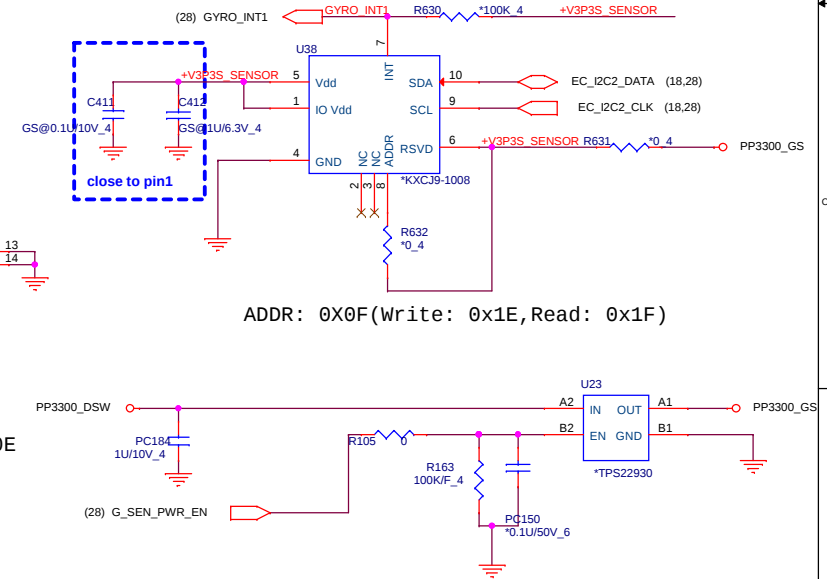
eDP panel control(LDS)



eDP Power(LDS)



0402 added G-sensor / TS-DB

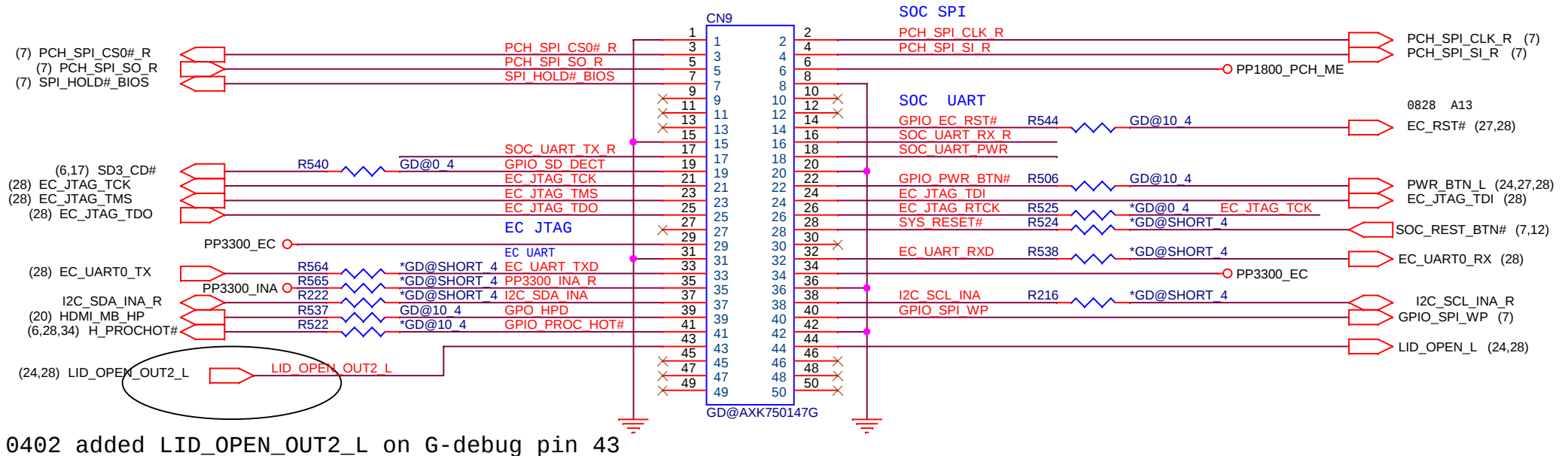


GOOGLE Debug Port(MPC)

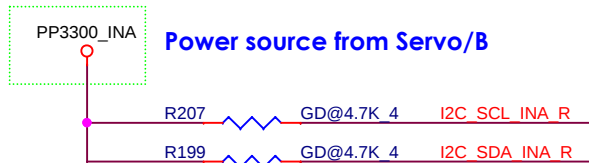
50 pin BTB is MUST, don't use 42 pin
Socket part number AXK750147G

PIN7	OD	PIN39	OD	PIN49	OD
PIN14	OD	PIN41	OD	PIN50	OD
PIN19	OD	PIN43	OD		
PIN22	OD	PIN44	OD		
PIN28	OD	PIN45	OD		
PIN30	OD	PIN46	OD		
PIN37	OD	PIN47	OD		
PIN38	OD	PIN48	OD		

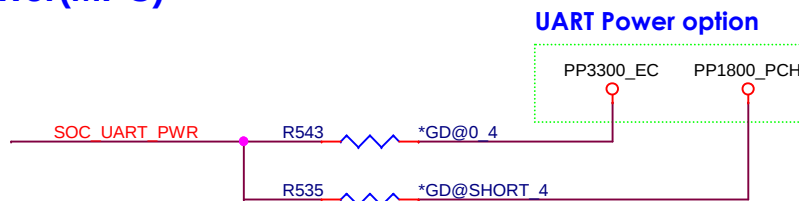
19



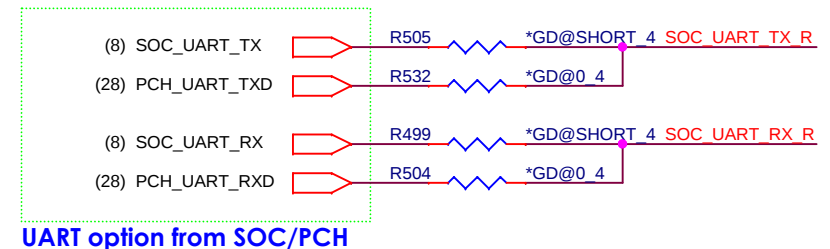
Servo/B I2C Power(MPC)



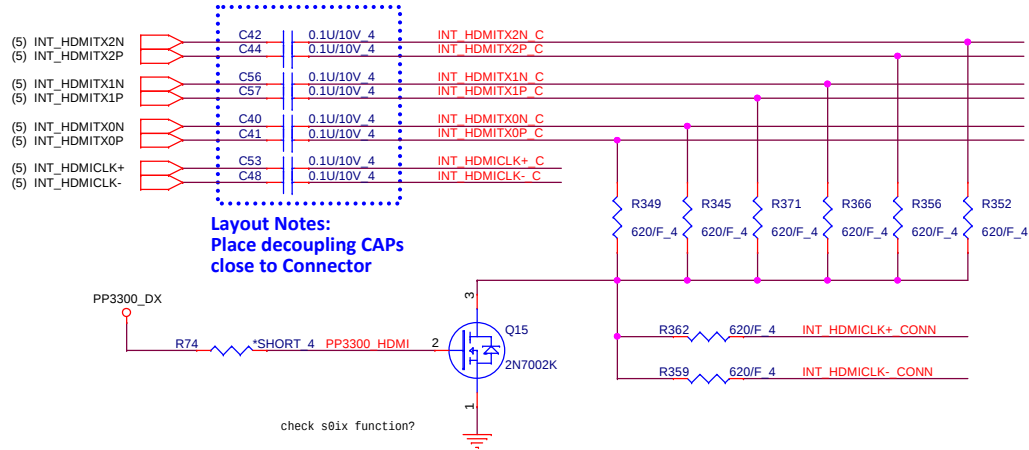
UART Power(MPC)



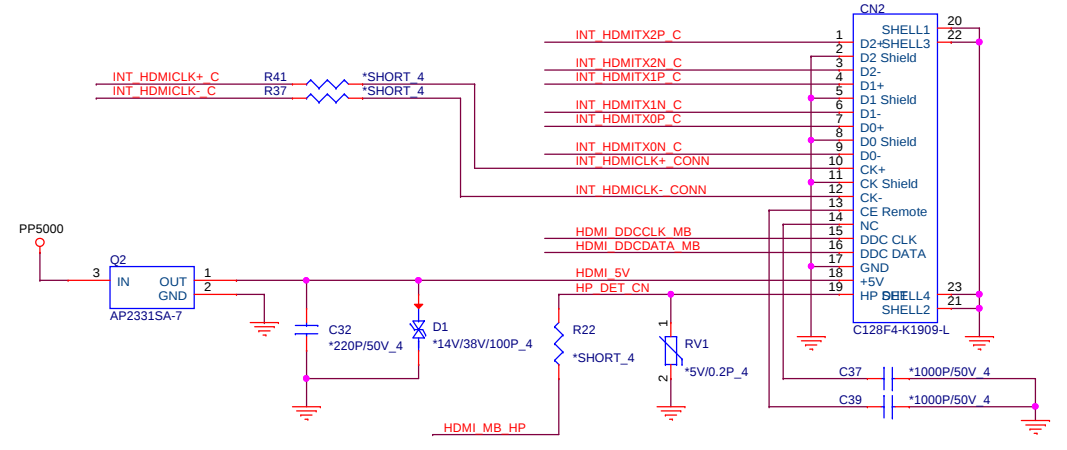
UART(MPC)



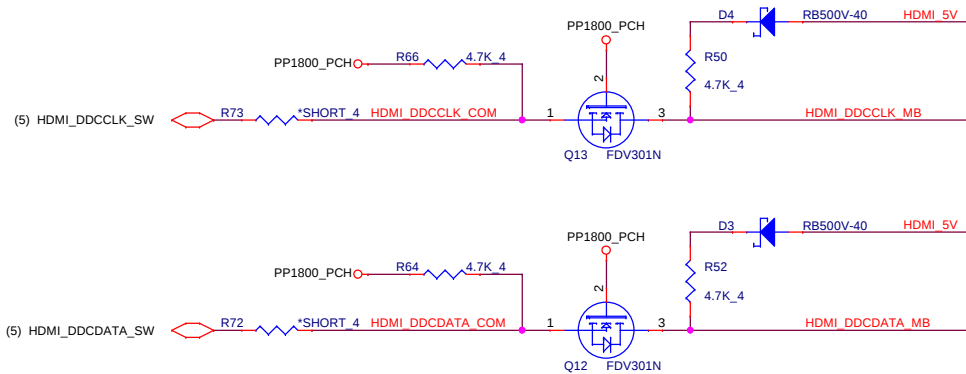
HDMI Cost Reduced level shift (HDM)



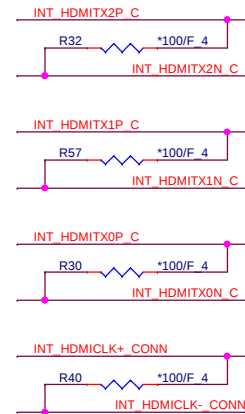
HDMI connector (HDM)



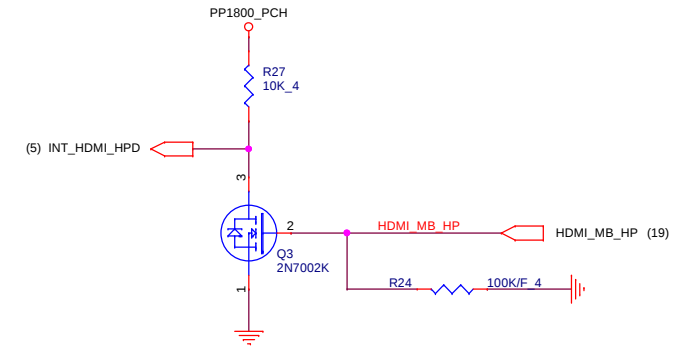
HDMI DDC (HDM)



EMI



HDMI-detect (HDM)



Quanta Computer Inc.
PROJECT : ZHS

Size	Document Number	Rev
	HDMI	1A

Date: Monday, August 10, 2015 Sheet 20 of 42

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BT



Quanta Computer Inc.
PROJECT : ZHS

Size	Document Number	Rev
	WIFI / BT	1A
Date:	Monday, August 10, 2015	Sheet 21 of 42

H



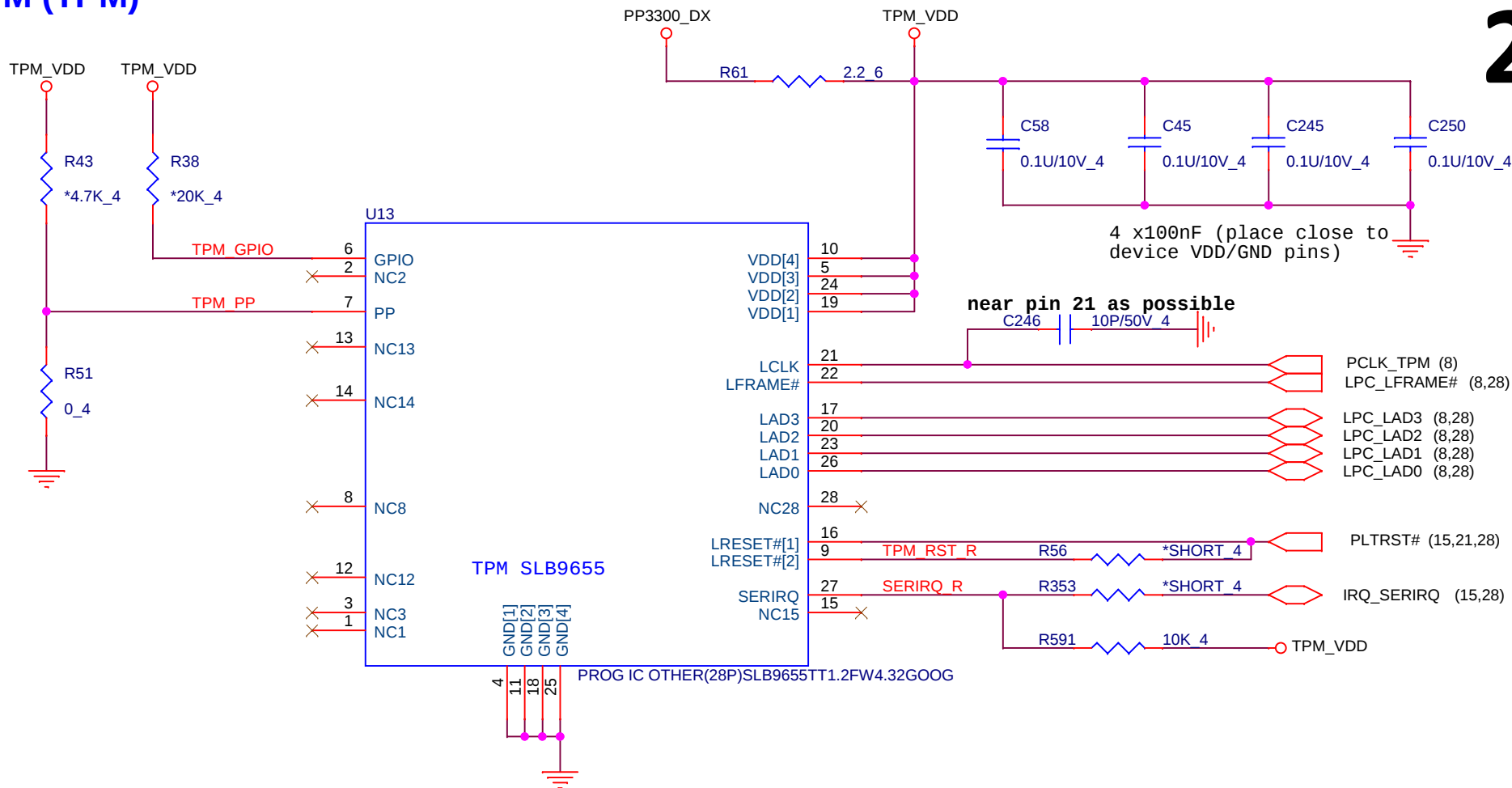
B

A



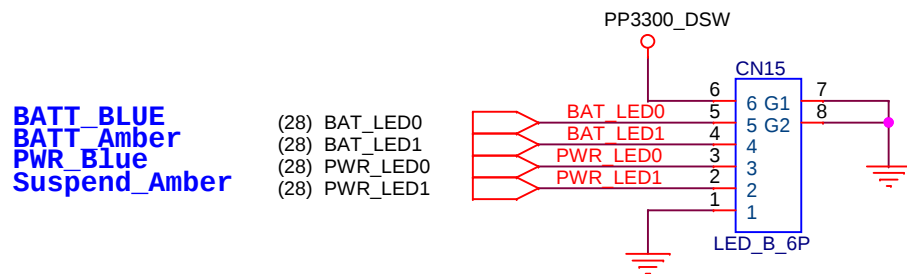
TPM (TPM)

23



LED board(UIF)

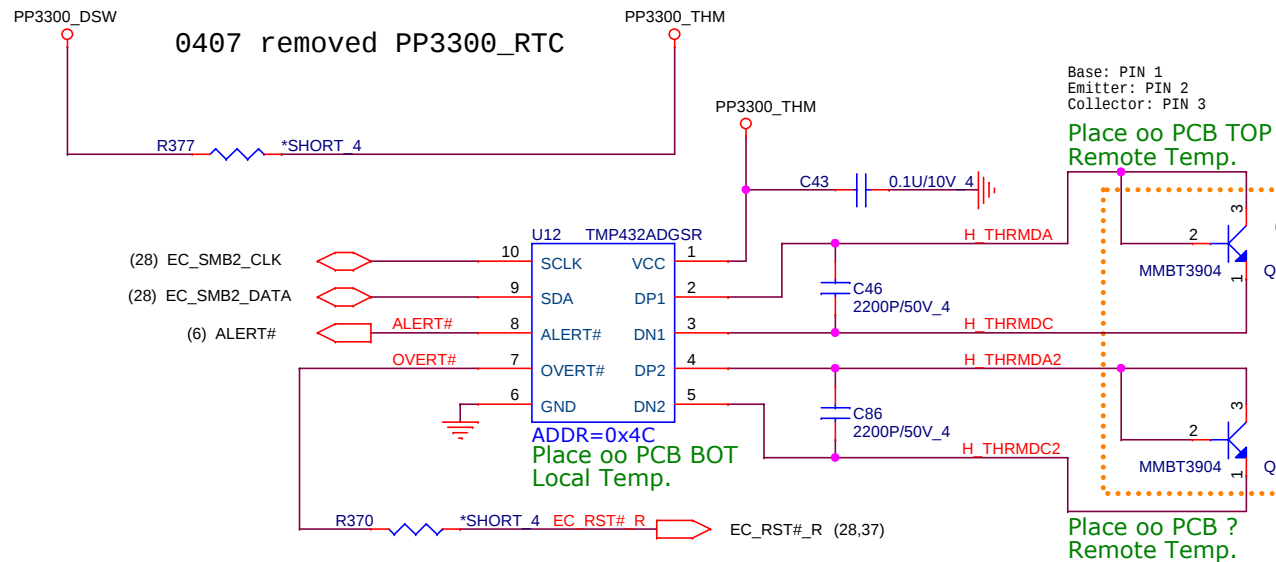
0402 Changed LED board connector as Origins use



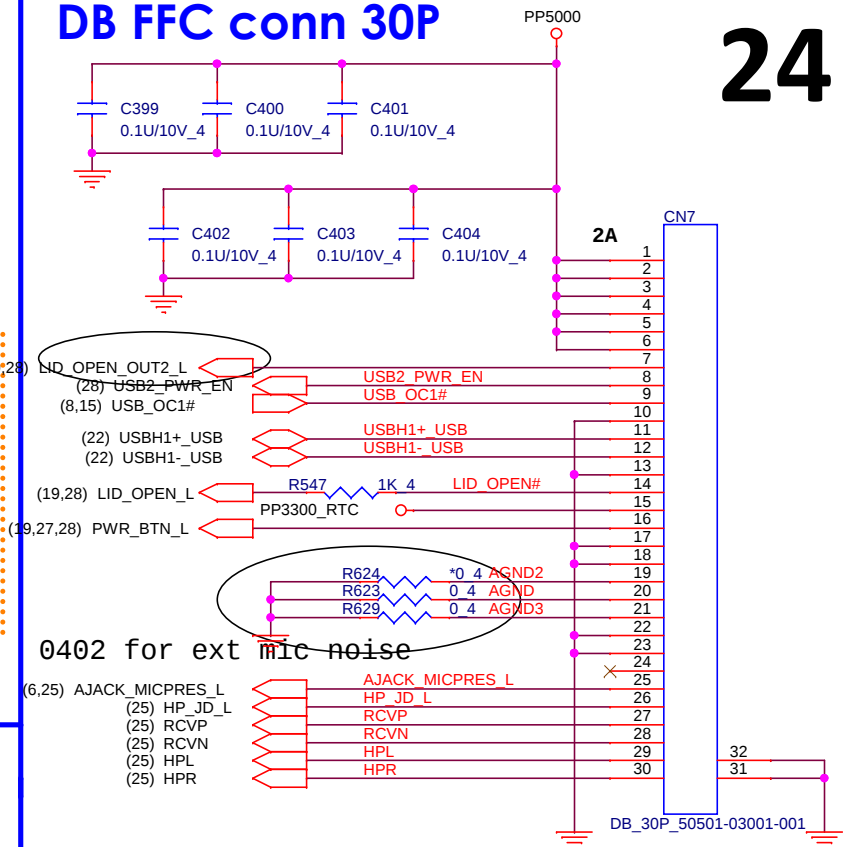
Quanta Computer Inc.
PROJECT : ZHS

Size	Document Number	Rev
	TPM SLB9655 / LED	1A
Date:	Monday, August 10, 2015	Sheet 23 of 42

Thermal Sensor(THM)



DB FFC conn 30P



USB 2.0_ILIM_SEL (USB)

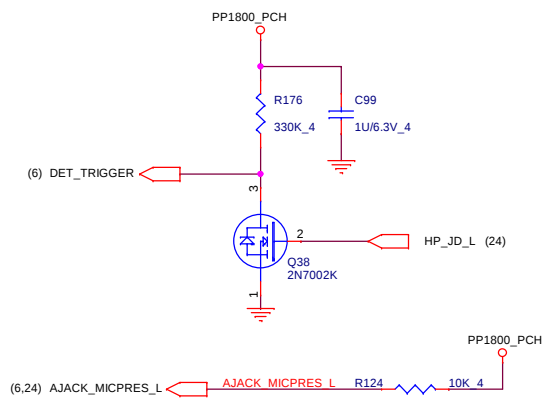
 Quanta Computer Inc. PROJECT : ZHS		Size	Document Number	Rev
			DB/Thermal sensor/LTE PWR	1A
Date: Monday, August 10, 2015		Sheet 24 of 42		

24

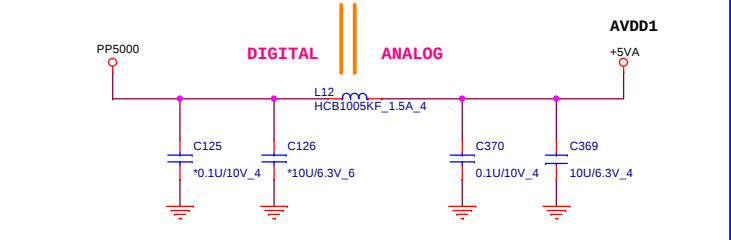
AUDIO CODEC (ADO)

25

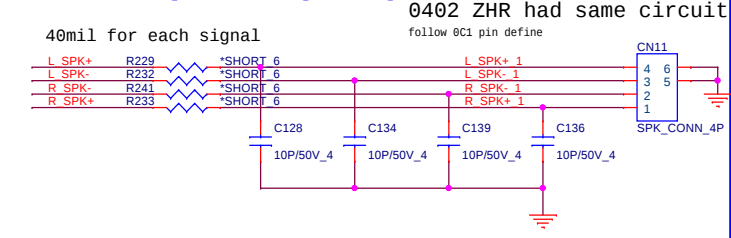
SOC DET (ADO)



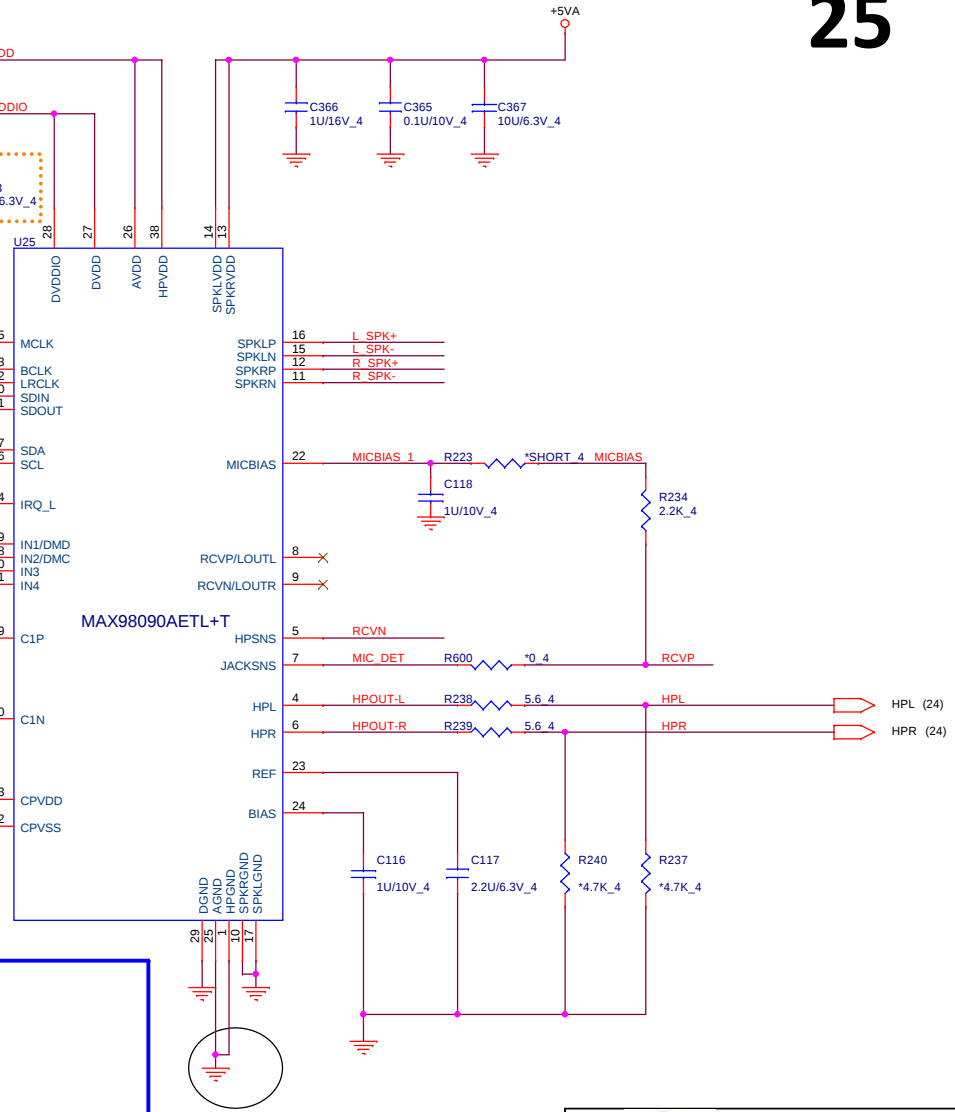
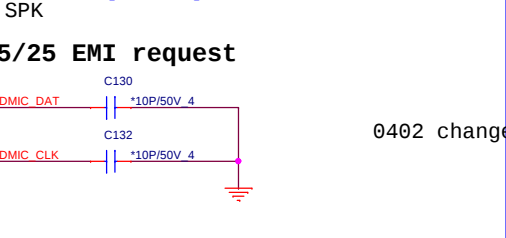
Codec PWR 5V (ADO)



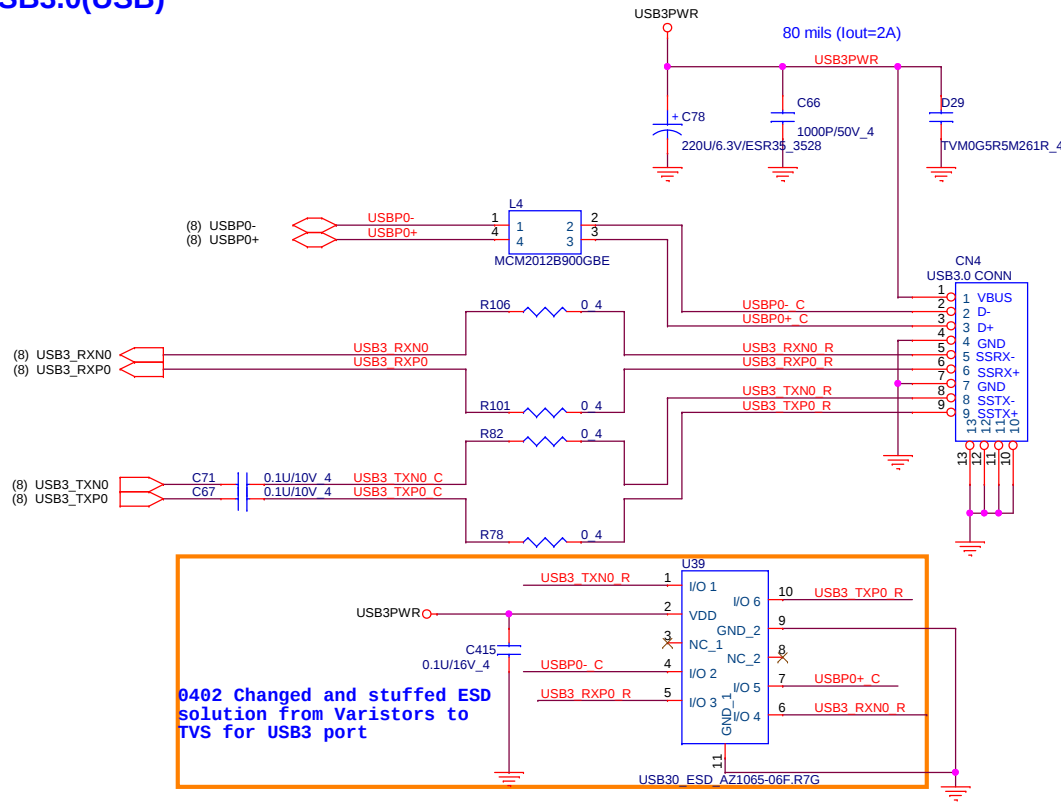
Internal Speaker (ADO)



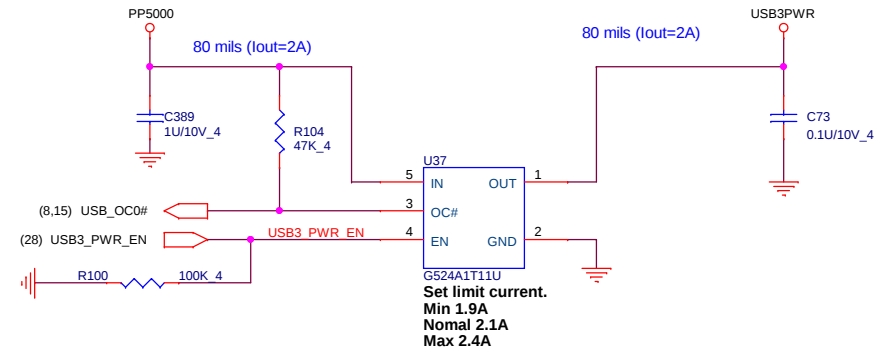
DMIC(ADO)



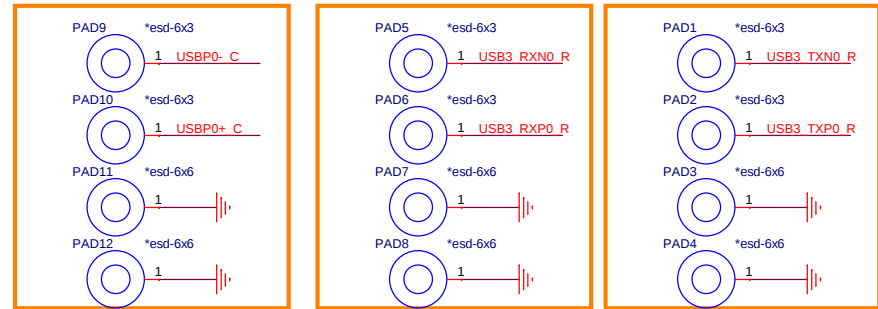
USB3.0(USB)



USB Switch

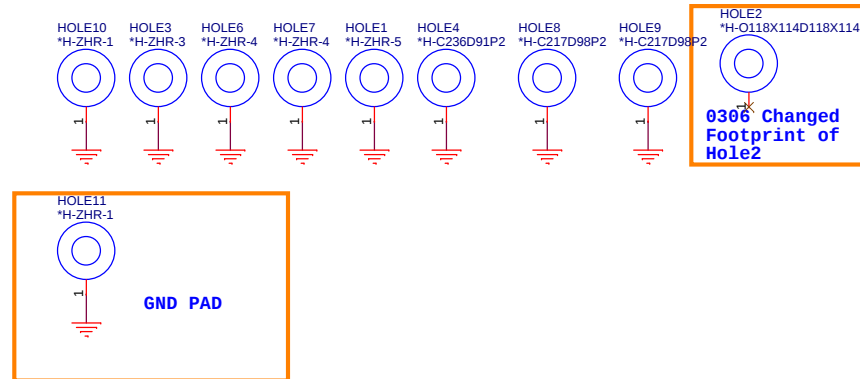
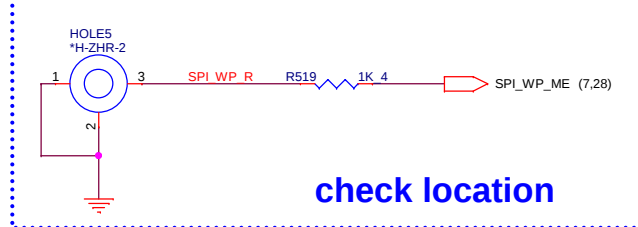


0804 Added PAD1-12
as ESD protection



HOLE(OTH)

ROM WP#

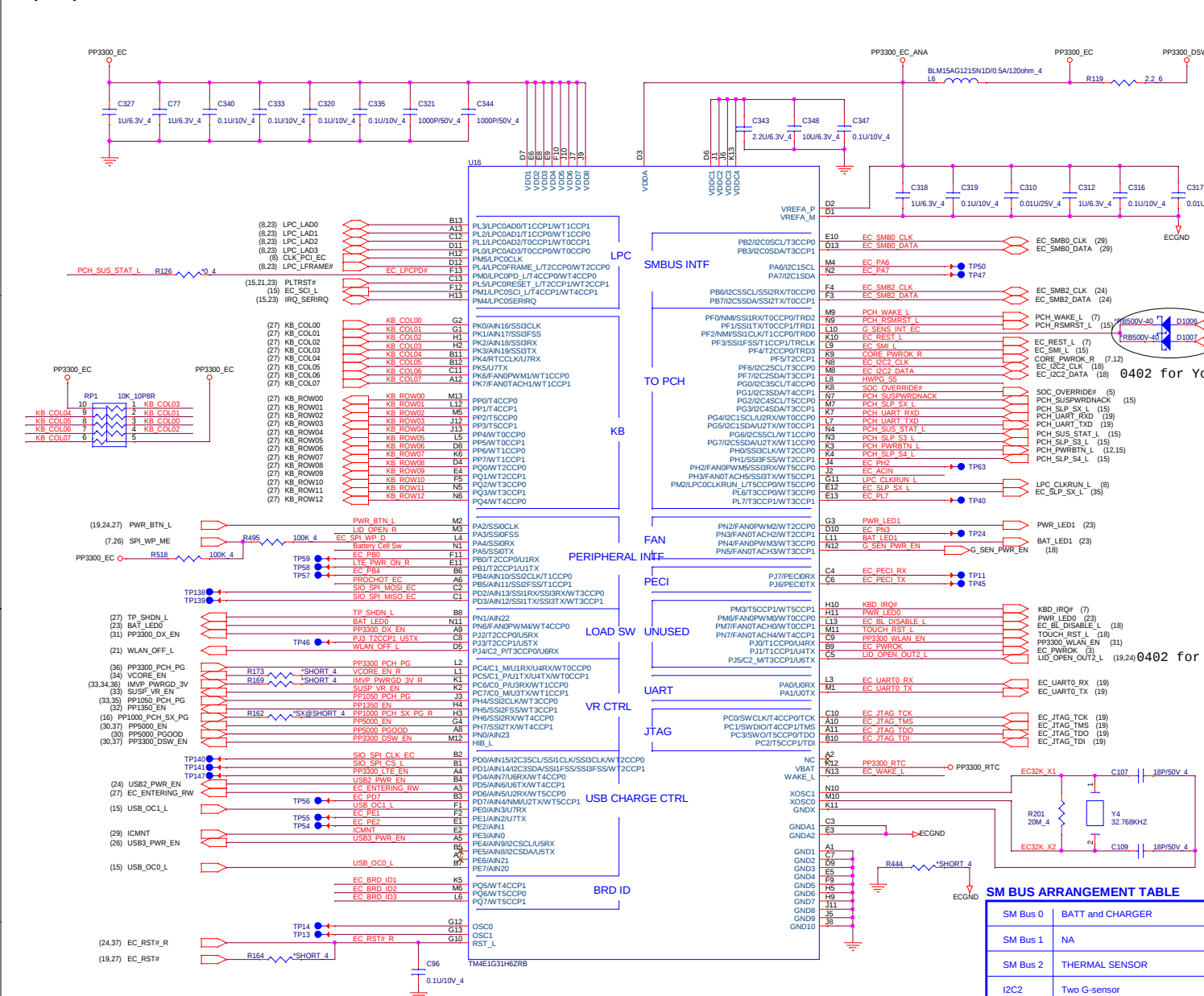


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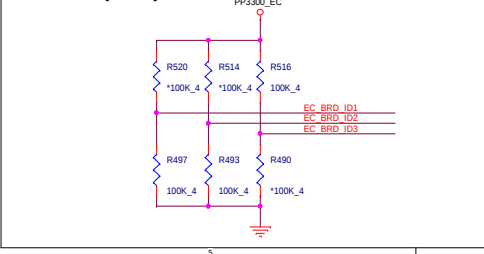
PROJECT : ZHS

Size	Document Number	Rev
	USB3/Hole	1A
Date:	Monday, August 10, 2015	Sheet 26 of 42

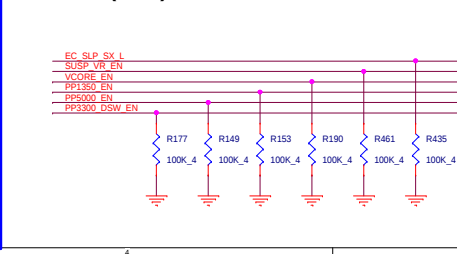
EC(KBC)



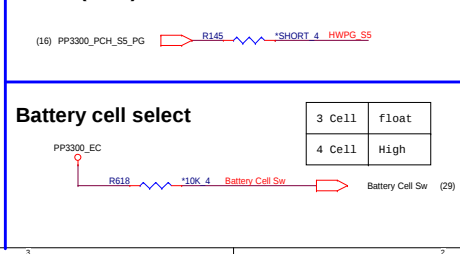
Board_ID(KBC)



Pull-down(KBC)



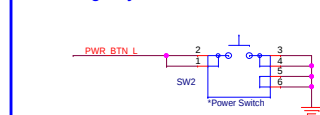
HWPG(KBC)



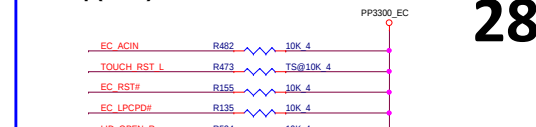
OD pin list	
-------------	--

EC_REST_L
BAT_LED0
BAT_LED1
PCH_RSMRST_L
SMBUS
IRQ_SERIRQ
EC_BL_DISABLE_L

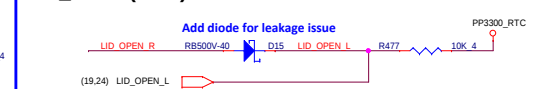
For testing only



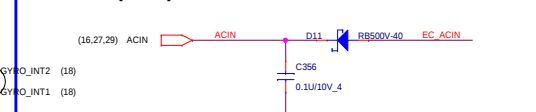
Pull-up(KBC)



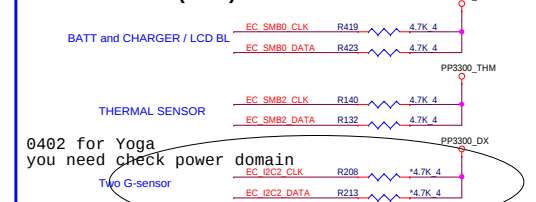
LID_OPEN(KBC)



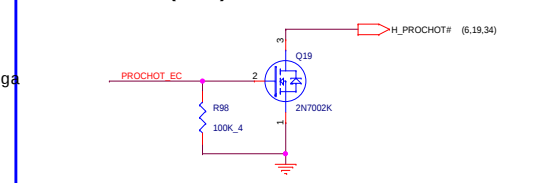
ACIN_EC(KBC)



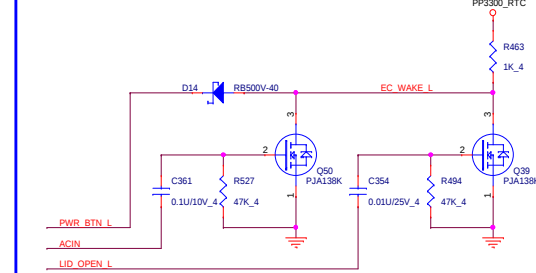
SM BUS/I2C PU(KBC)

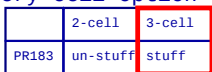


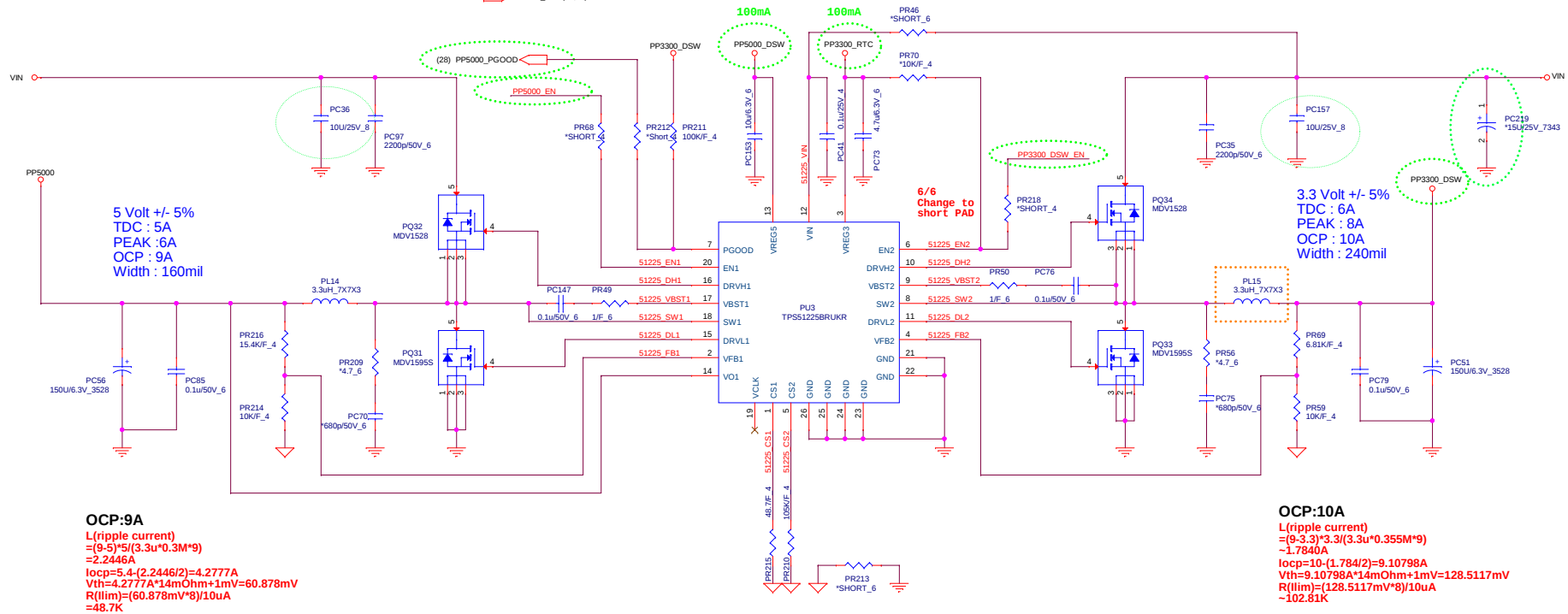
PROCHOT_EC(KBC)



EC HIB WAKE SOURCES

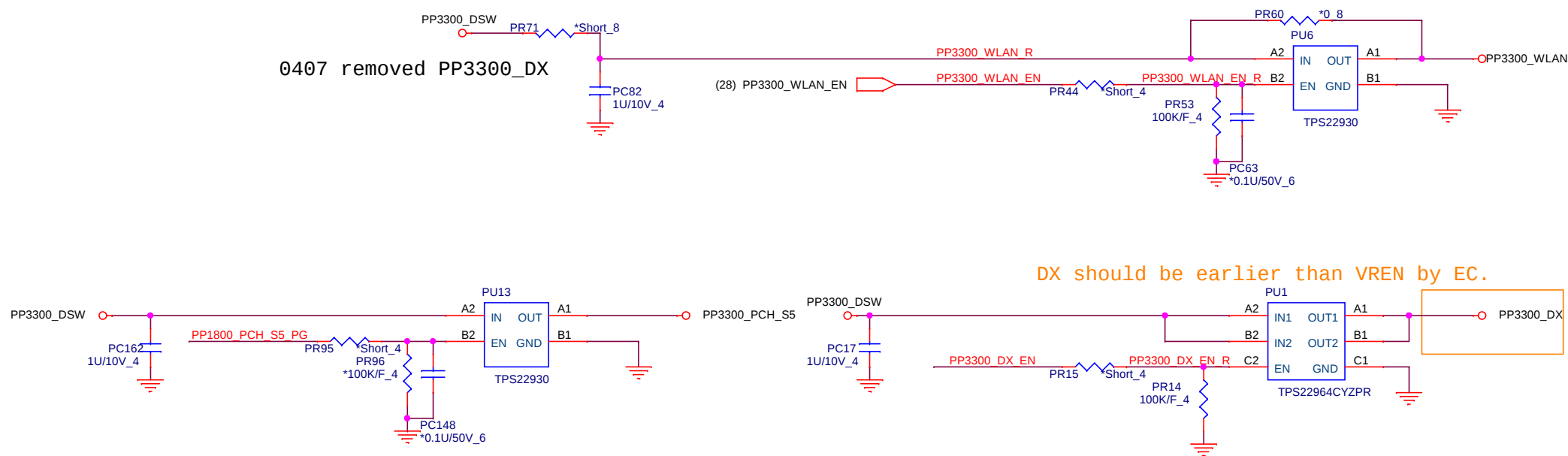


[illegible]



(36) PP1800_PCH_S5_PG PP1800_PCH_S5_PG
 (28) PP3300_DX_EN PP3300_DX_EN

0407 removed PP3300_DX



DX should be earlier than VREN by EC.

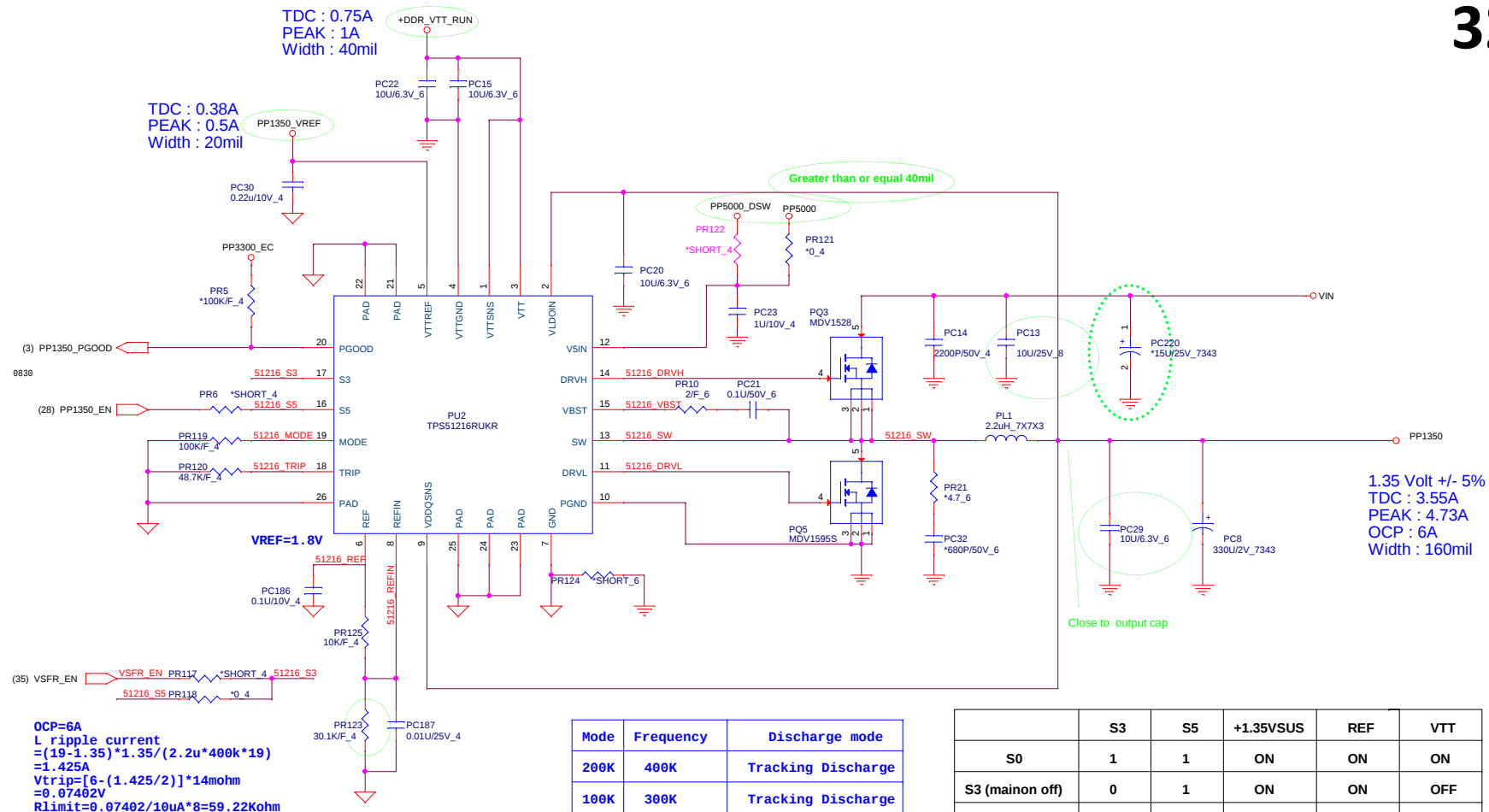


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PROJECT :

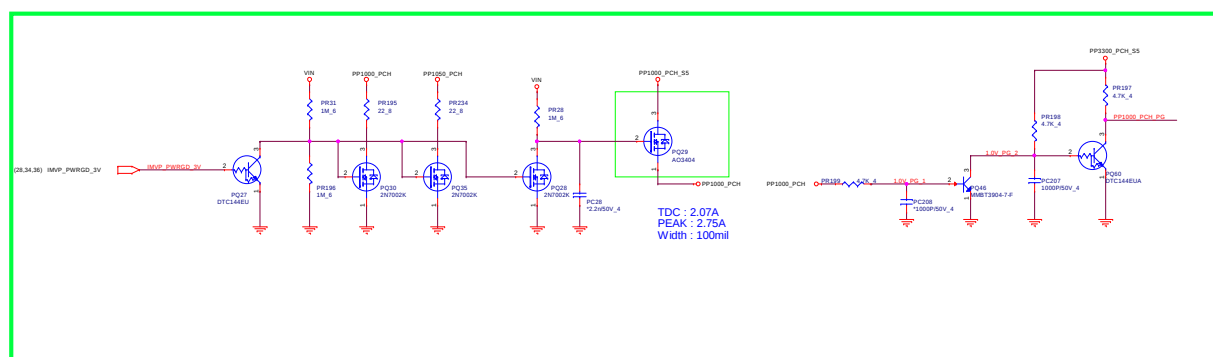
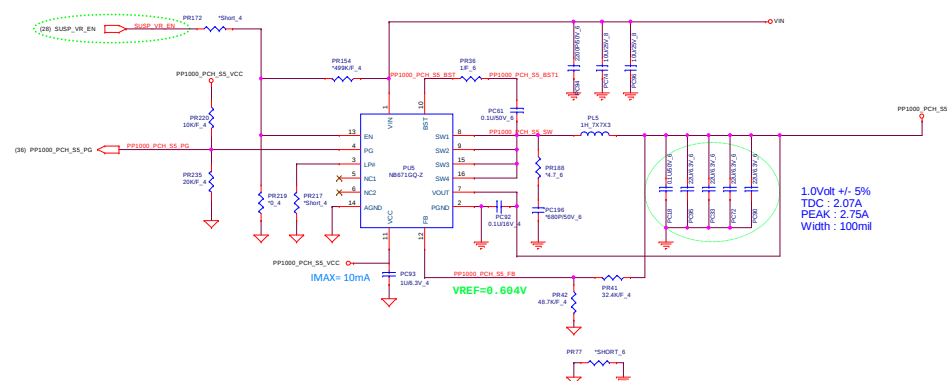
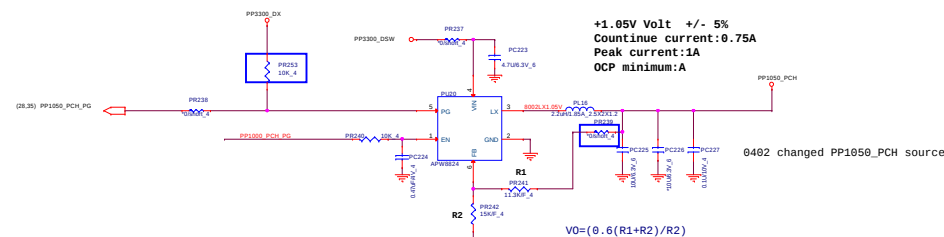
Size	Document Number	Rev
	Load Switch	1A

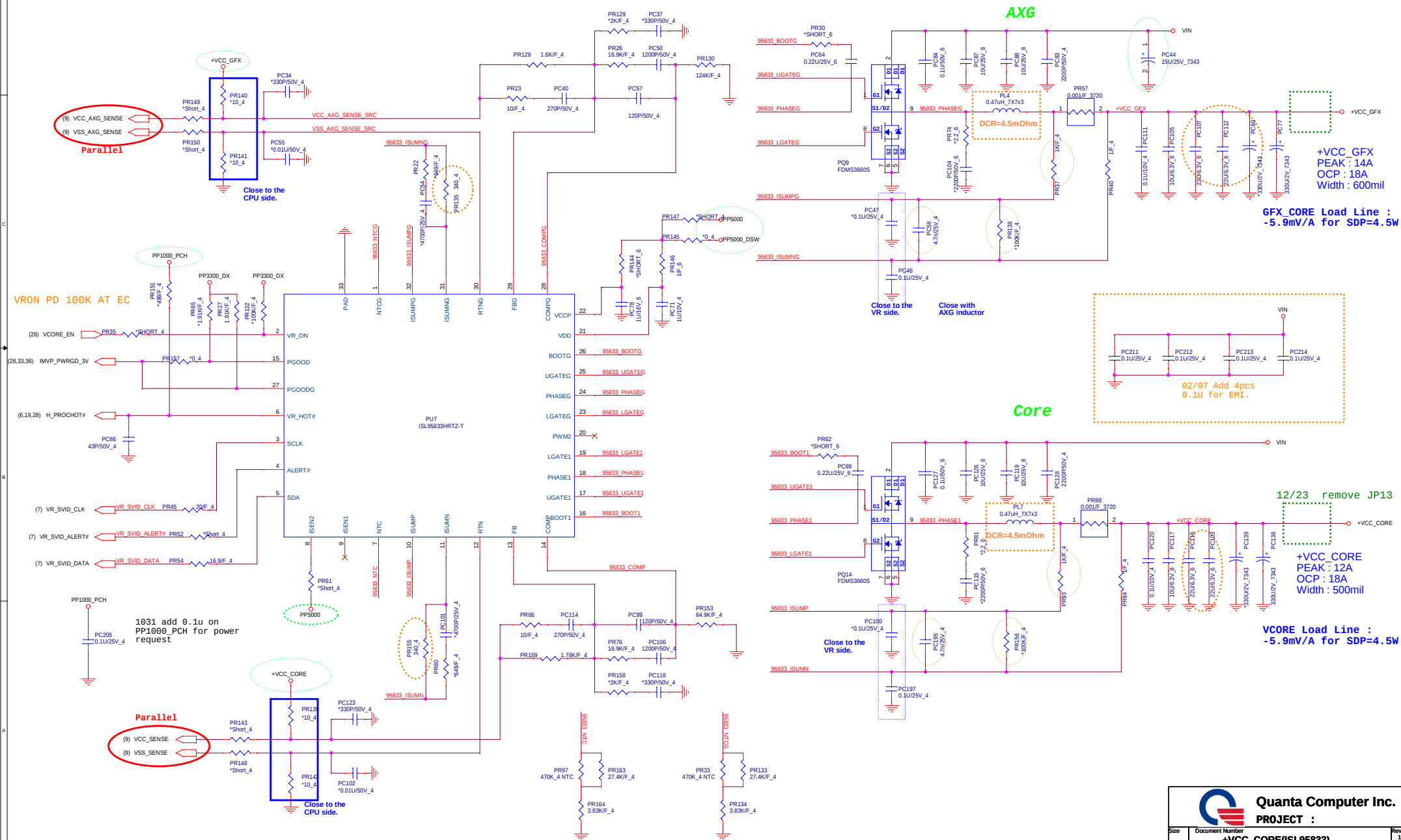
Date: Monday, August 10, 2015 Sheet 31 of 42

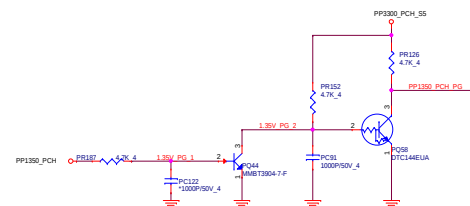
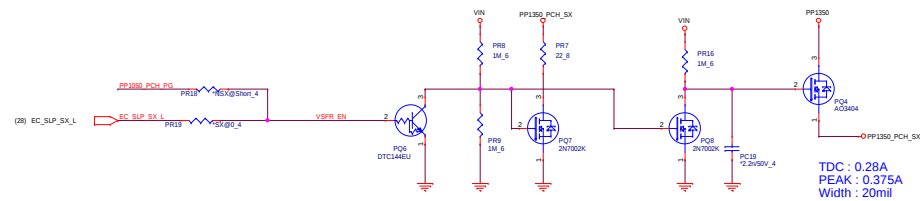


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PROJECT :

+1.05V Volt +/- 5%
Continue current:0.75A
Peak current:1A
OCP minimum:A

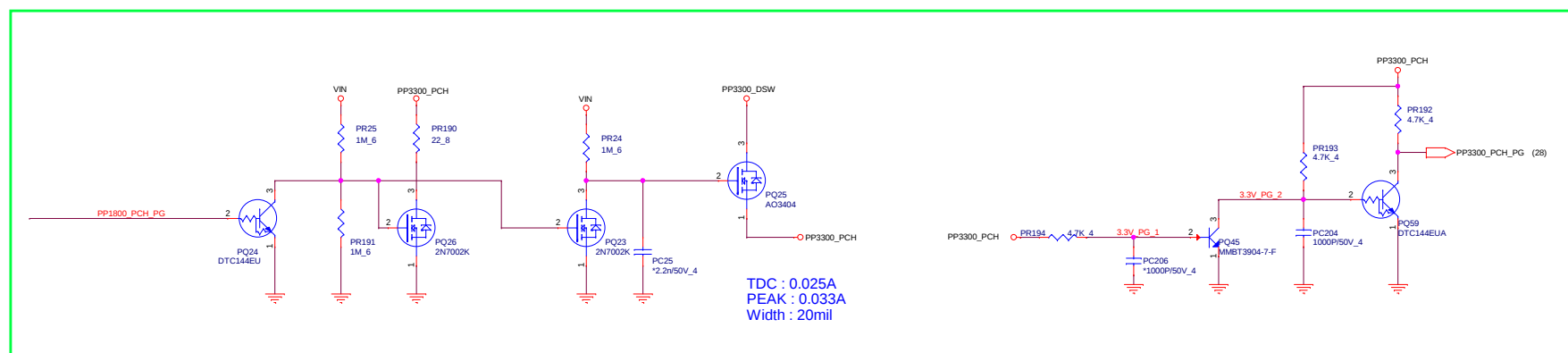
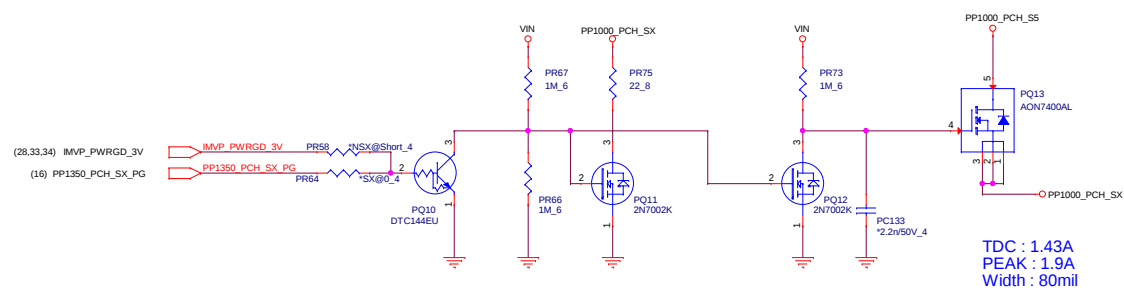
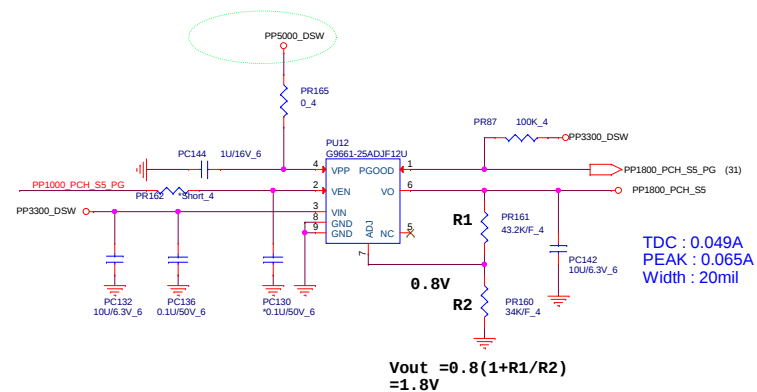






(35) PP1800_PCH_PG

(33) PP1000_PCH_S5_PG



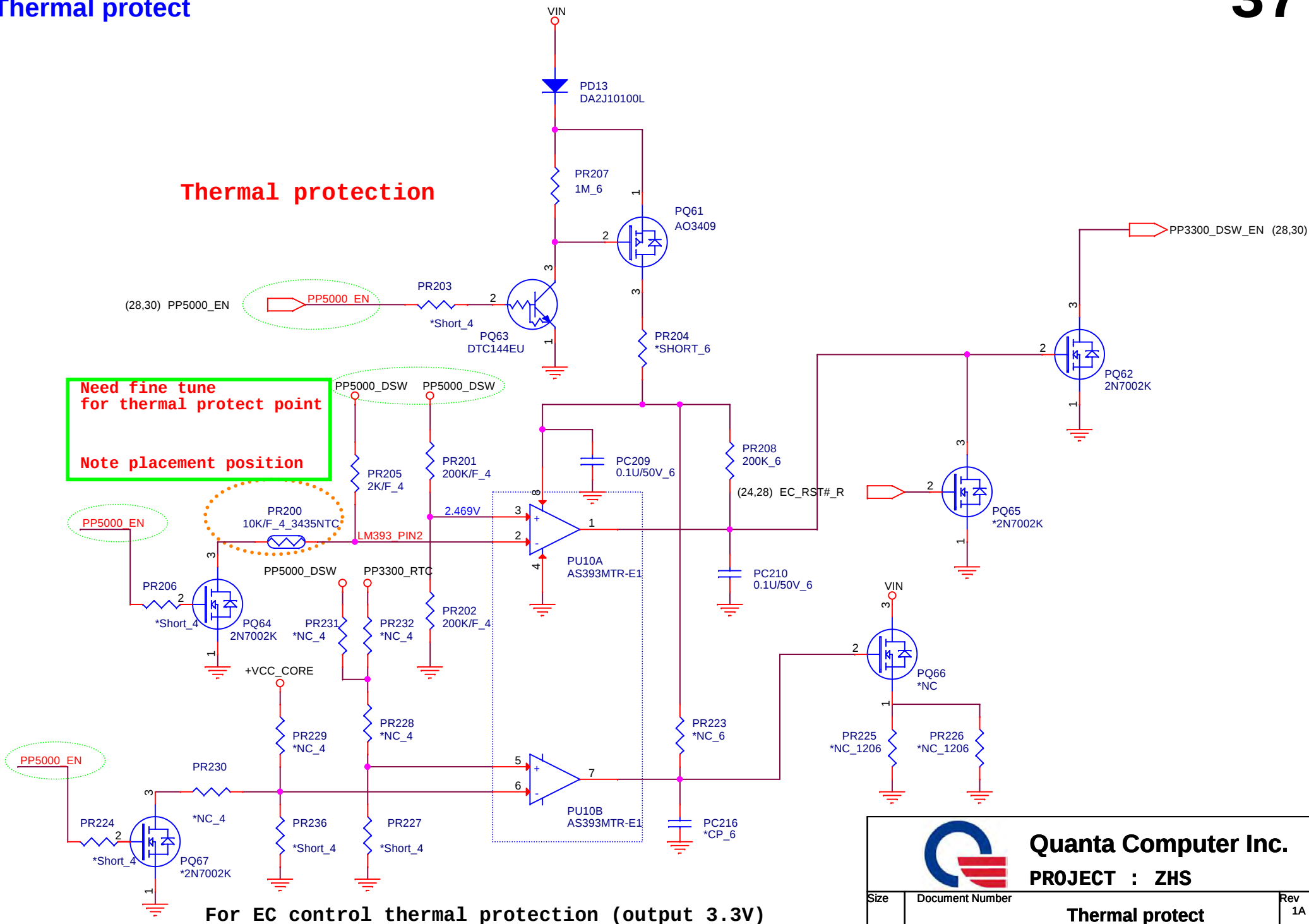
Thermal protect

37

Thermal protection

Need fine tune
for thermal protect point

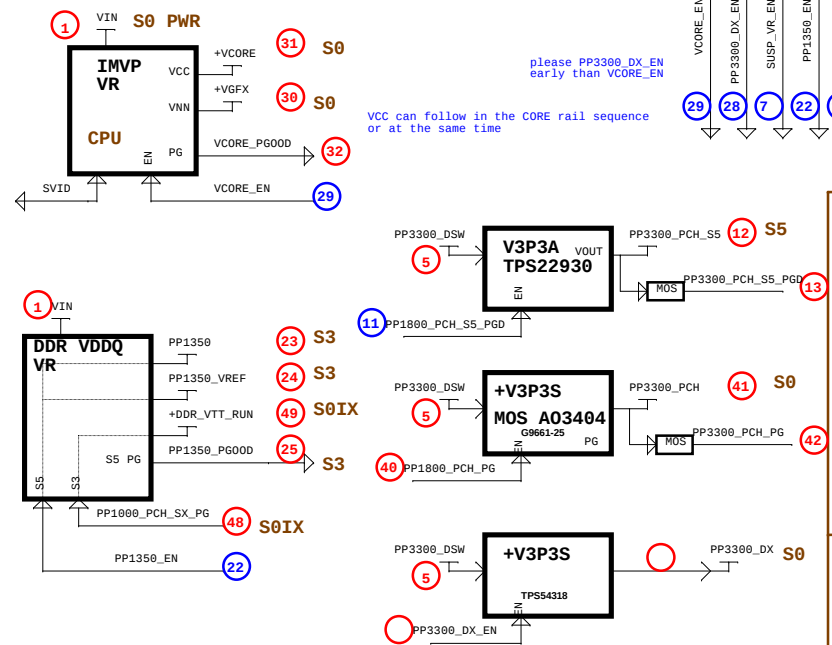
Note placement position



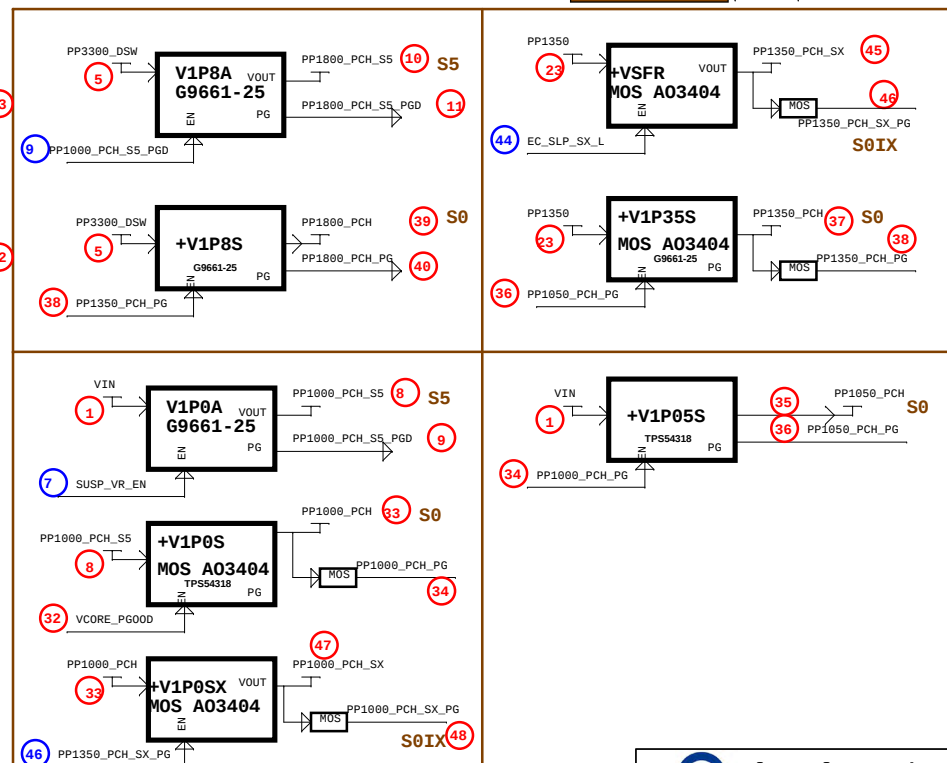
Quanta Computer Inc.

PROJECT : ZHS

Size	Document Number	Thermal protect	Rev 1A
Date:	Monday, August 10, 2015	Sheet 37 of 42	



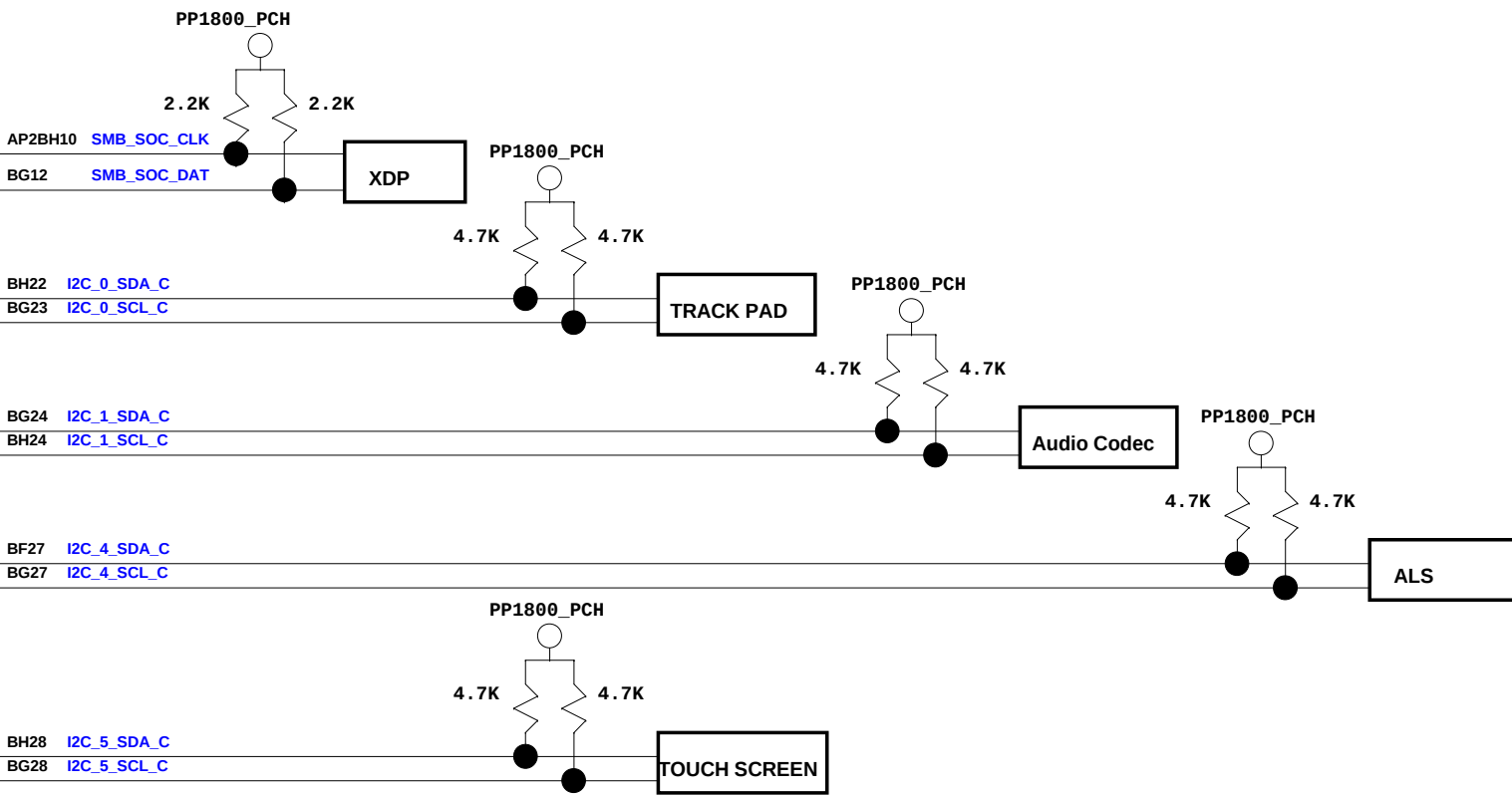
- a 10us to 2000us delay is required between rails to avoid inrush current caused by multiple loads turning on simultaneously and fast charging of VR output decoupling



SMBUS

Bay-trail M

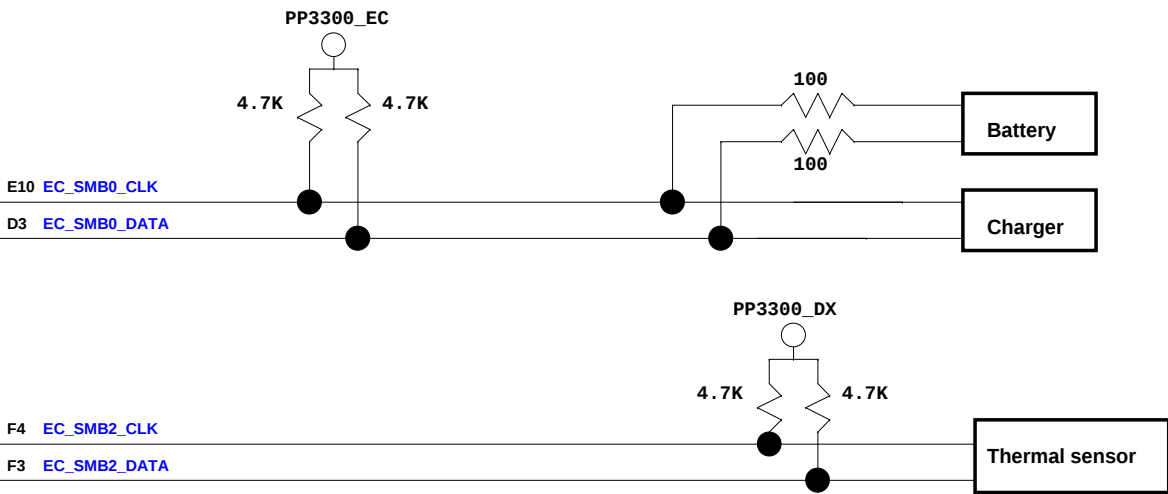
I2C



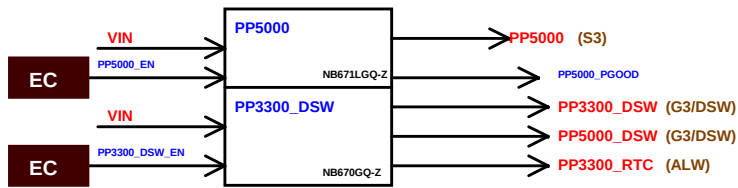
KBC

TI

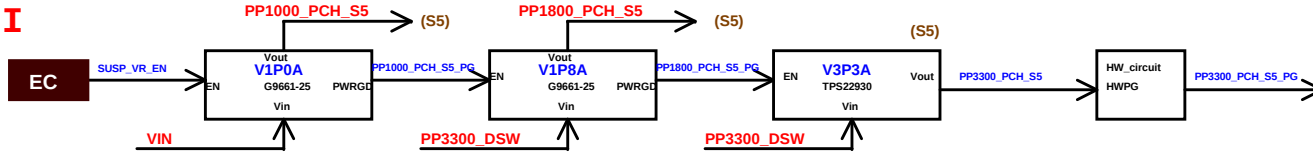
SMBUS



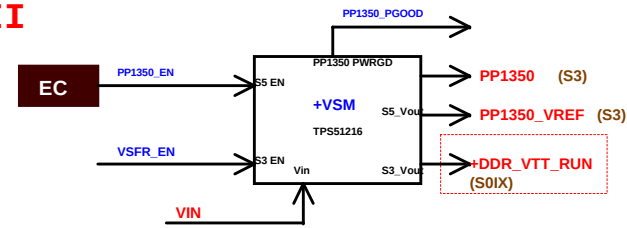
I



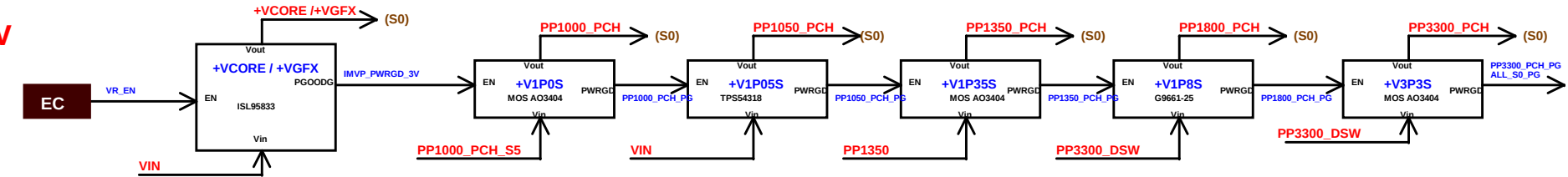
II



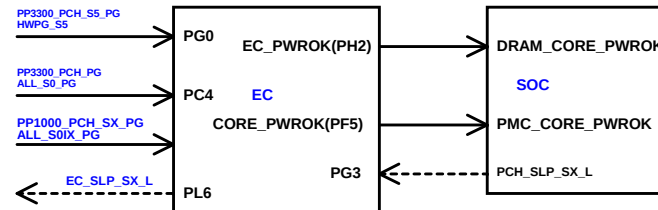
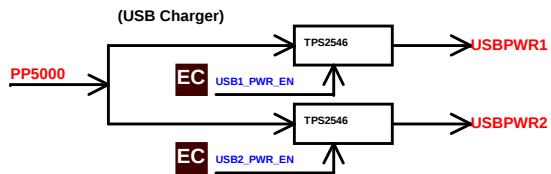
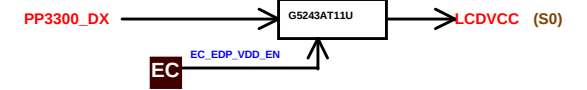
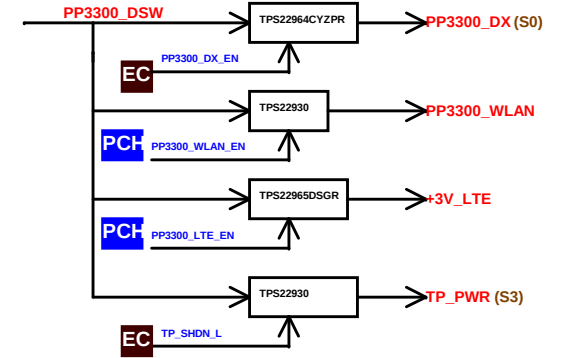
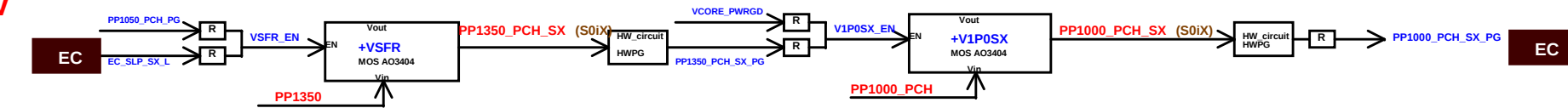
III



IV



V



		CHANGE LIST				41
Model	Version					
ZHS M/B	1A	1. 2015/05/19 :Update RAM ID for ZHQ and ZHS use.(page8) 2. 2015/05/19 : add R200 and R214 LTE_WAKE# and PMC_SUSCLK1 pull high to PP1800_PCH_S5 for can't into S3 issue (Page7) 3. 2015/05/19 : add R426 LTE_DISABLE# Pull-High to PP1800_PCH_S5 for can't into S3 issue.(Page 8) 4. 2015/05/19 : add R603/R609/Q62/R167/R607/Q63 FOR SD Card can't work issue. (page 17) 5. 2015/05/19 : add PR523 10k Pull-high to PP3300_DX for can't power on issue (Page 41) 6. 2015/05/19 : add PR234 and PQ35 for PP1050_PCH 放電線路 (Page 41) 7. 2015/05/19 : EMI request add PC189 for EMI issue. (Page 39) 8. 2015/05/19 : EMI request add C112 for EMI issue. (page22) 9. 2015/05/19 : EMI request add C130/C132 DMIC CLK/DAT for EMI issue(Page22)				
		1. 2015/06/19 : Add C35 and Change R326 to 33 ohm for Acer ESD request (page18) 2. 2015/06/19 : Add Pad1-Pad12 for Acer ESD request (page26) 3. 2015/06/19 : Add R427 33 ohm Acer ESD request (page27) 4. 2015/06/19 : Del R490 , Add R516 for SANYO battery 5. 2015/06/19 : Change 0 ohm to Short Pad: R14,R17,R39,R217 6. 2015/08/10 : Change 0 ohm to Short Pad: PR46,PR218,PR68,PR248,PR244,PR247,PR243,PR249,PR245,PR122,PR6,PR117,PR250,PR246				
DOC NO.	PROJECT MODEL :	Chrome	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISION:	
		Quanta Computer Inc. PROJECT : ZHS Change list				

