MODEL NAME : Marble Falls/ Discrete
PROJECT CODE : ZAL50, ZAL60
PCB NO : LA-B072P

ZZZ R1@
PCB 14B LA-B072P REV0 M/B

UC1
CPU

UV17	UV18	UV19	UV20	RV59	ZZZ
VRAM	VRAM	VRAM	VRAM	20K	X7653531L01
X76_HYX@	X76_HYX@	X76_HYX@	X76_HYX@	X76_HYX@	X76_HYX_R@

UV17	UV18	UV19	UV20	RV59	ZZZ
VRAM	VRAM	VRAM	VRAM	24.9K	X7653531L51
X76_MIC@	X76_MIC@	X76_MIC@	X76_MIC@	X76_MIC@	X76_MIC_R@

UV17	UV18	UV19	UV20	RV59	ZZZ
VRAM	VRAM	VRAM	VRAM	30.1K	X7653531L02
X76_SAM@	X76_SAM@	X76_SAM@	X76_SAM@	X76_SAM@	X76_SAM_R@

For Post RTS

Dell / Compal Confidential

Schematic Document

Intel Broadwell ULT
Marble Falls 14"/15" Value
DIS

2013-10-03 Rev: 0.1

Security Classification	Compal Secret Data		
Issued Date	2013/08/01	Deciphered Date	2014/07/31

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Title: *SCHEAMTICS,MB AB072*

Size | Document Number: *4019RU* | Rev: A

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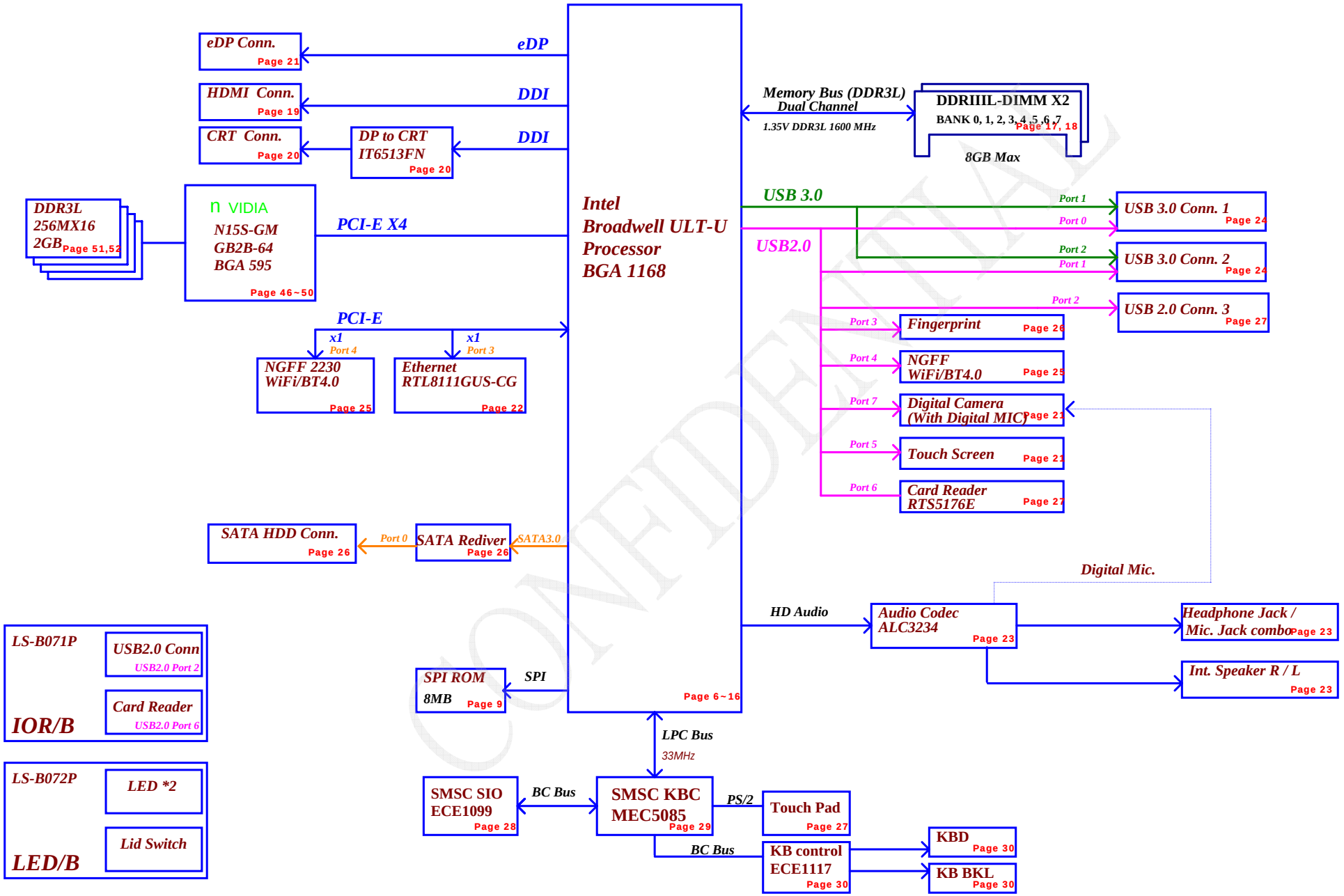

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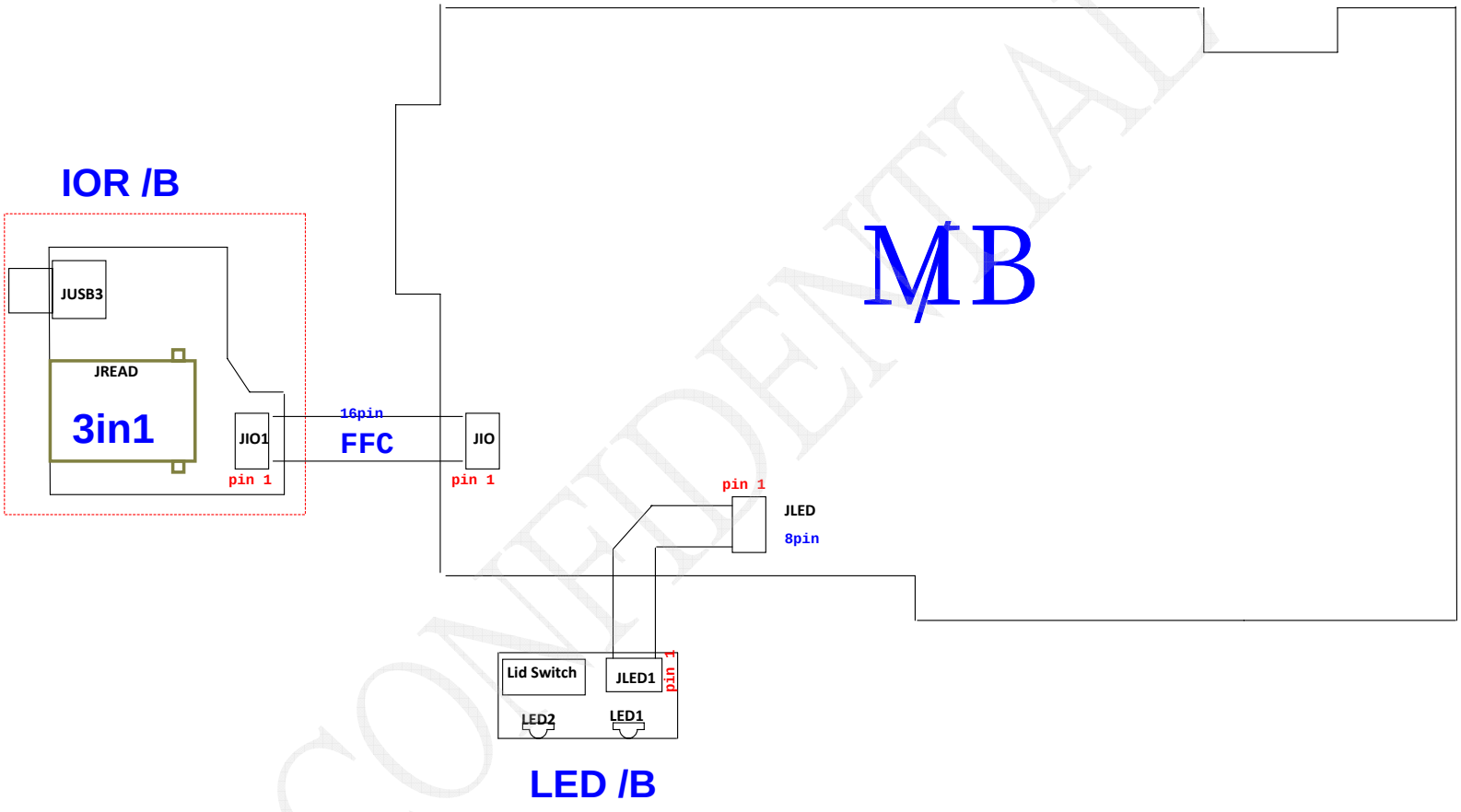

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Board ID Table

Phase ID

RE79	CE54	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	A00
4.3K	4700p	
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

Config ID

RE89	RE90	Config
De-Pop	Pop	Discrete
Pop	De-Pop	UMA

SMBUS Control Table

	SOURCE	BATT	Charger	DDR3L	XDP	WLAN NGFF	Touch pad	VGA
CHARGER_SMBCLK CHARGER_SMBDAT	MEC5085		V					
PBAT_SMBCLK PBAT_SMBDAT	MEC5085	V						
GPU_SMBCLK GPU_SMBDAT	MEC5085							V
SML1_SMBCLK SML1_SMBDATA	MEC5085							
SMBCLK SMBDATA	ULT			V	V	V	V	
SML0CLK SML0DATA	ULT							
SML1CLK SML1DATA	ULT							

Link

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100/1000 LAN
CLKOUT_PCIE3	NGFF (BT + WLAN)
CLKOUT_PCIE4	
CLKOUT_PCIE5	

Symbol Note :

: means Digital Ground

: means Analog Ground

ULT		
	USB3.0	
	Port1	USB connector 1
	Port2	USB connector 2
	Port3	
	Port4	
	USB2.0	
	Port0	USB connector 1
	Port1	USB connector 2
	Port2	USB connector 3 (IO/B)
	Port3	Finger print
	Port4	NGFF (BT + WLAN)
	Port5	Touch Screen Panel
	Port6	Card Reader
	Port7	Camera
	PCI EXPRESS	
	Lane 1	
	Lane 2	
	Lane 3	10/100/1000 LAN
	Lane 4	NGFF (BT + WLAN)
	Lane 5	PEG (N15S)
	Lane 6	
	SATA	
	SATA0	HDD
	SATA1	
	SATA2	
	SATA3	
	DDI	
	DDI1	HDMI
	DDI2	DP to CRT

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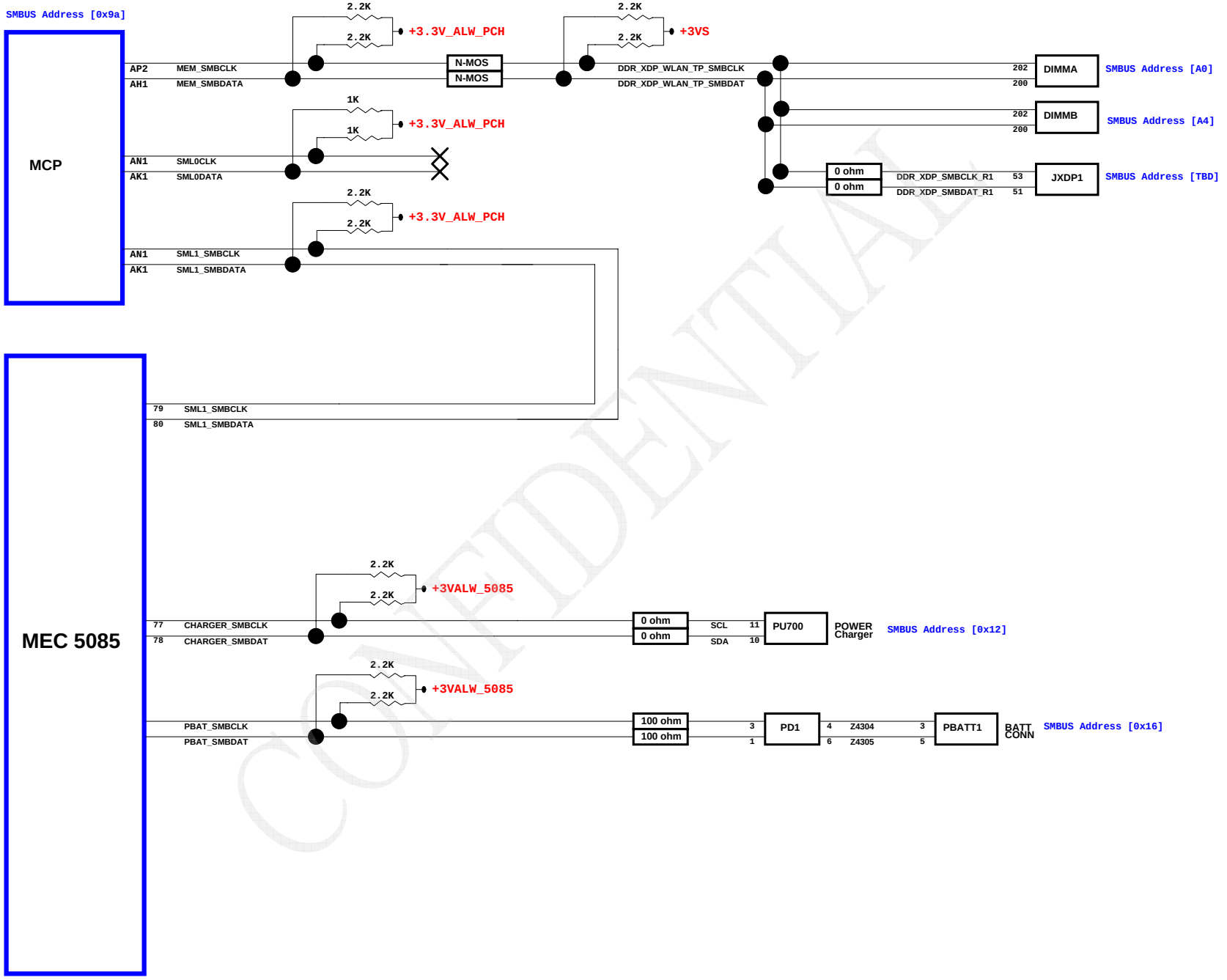

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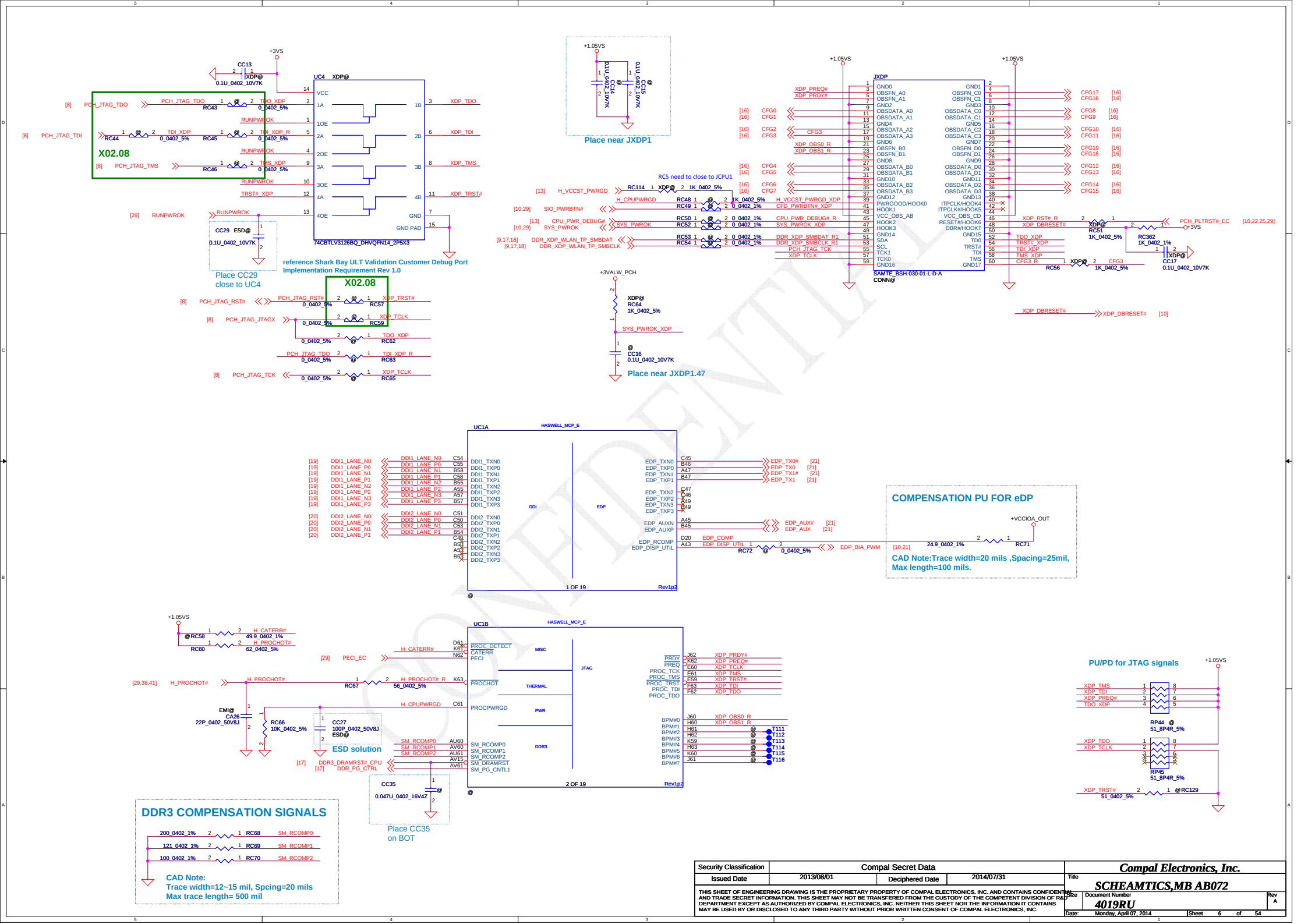

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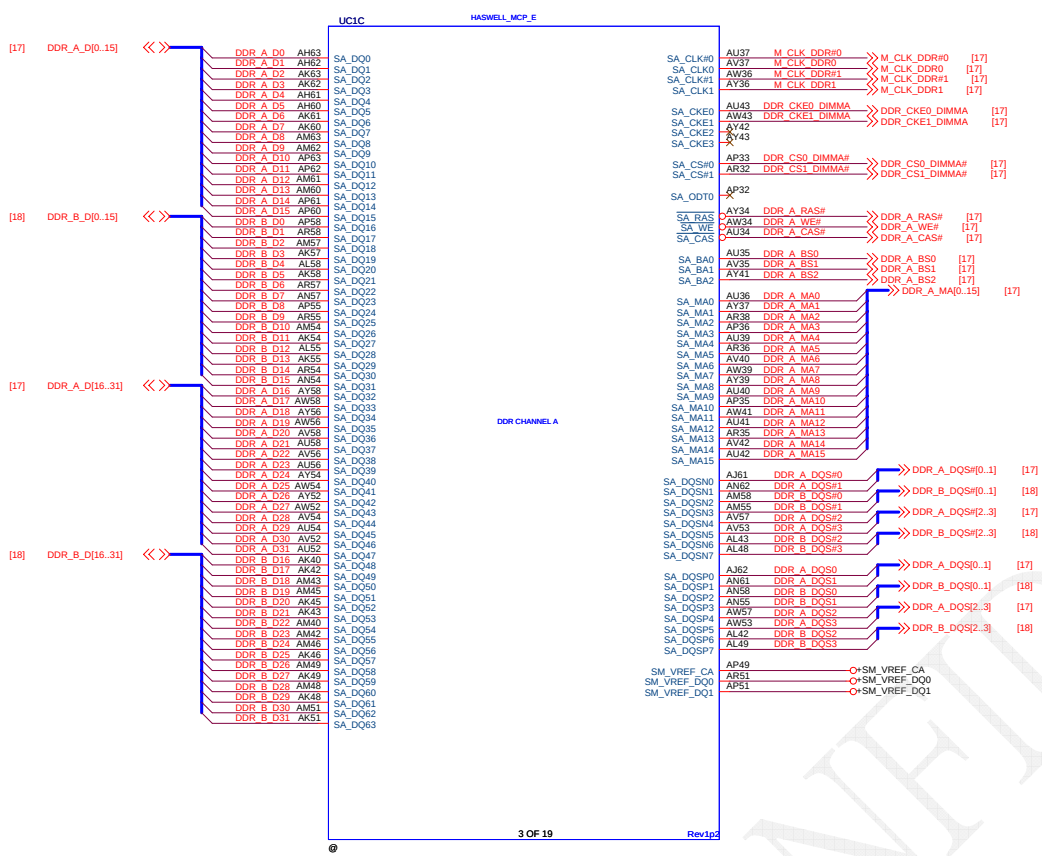
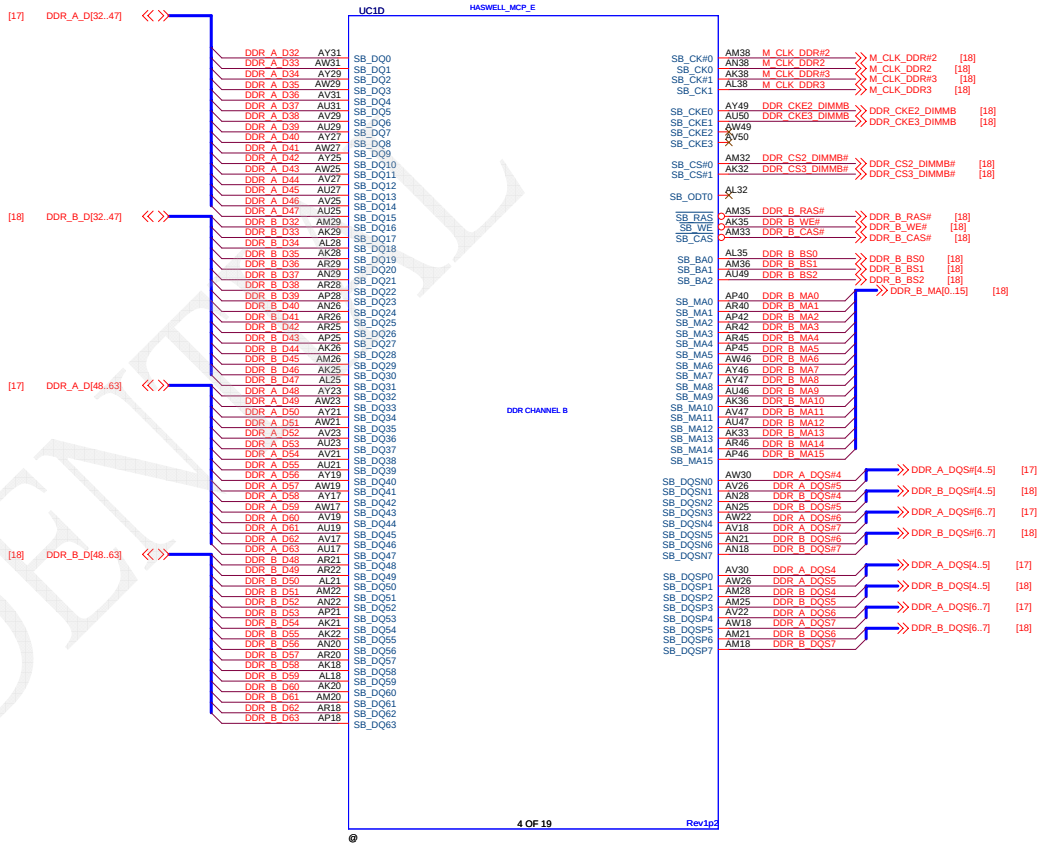
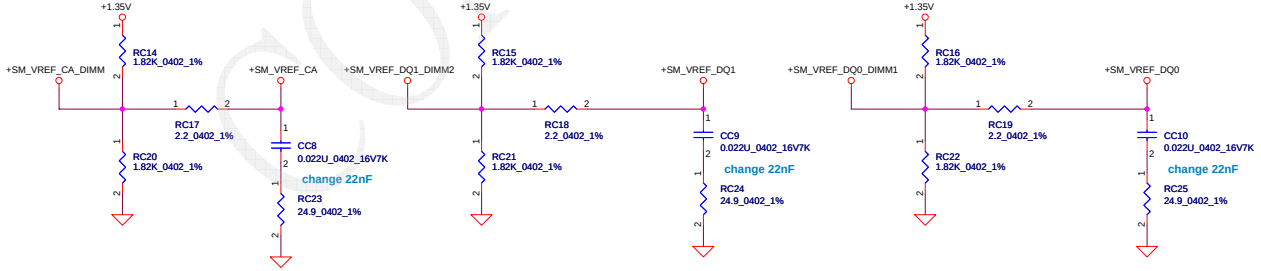
Interleaved Memory







confirm by intel request PDG P141

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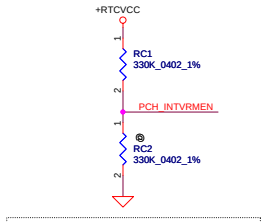
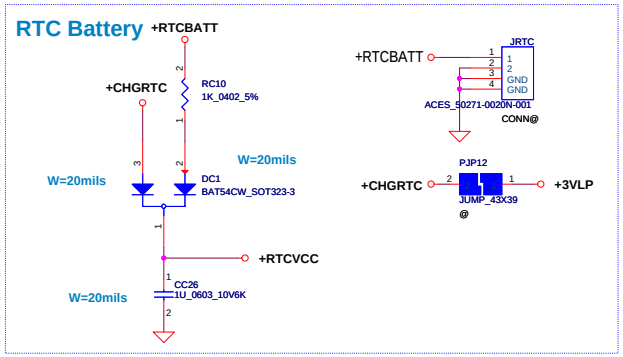
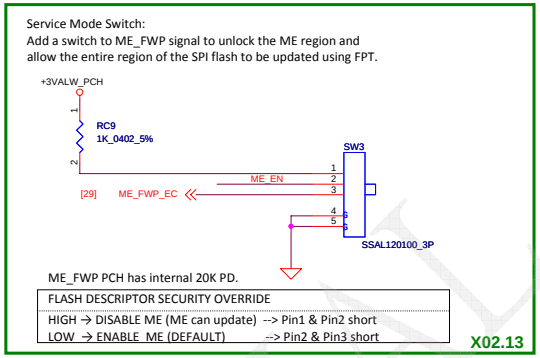
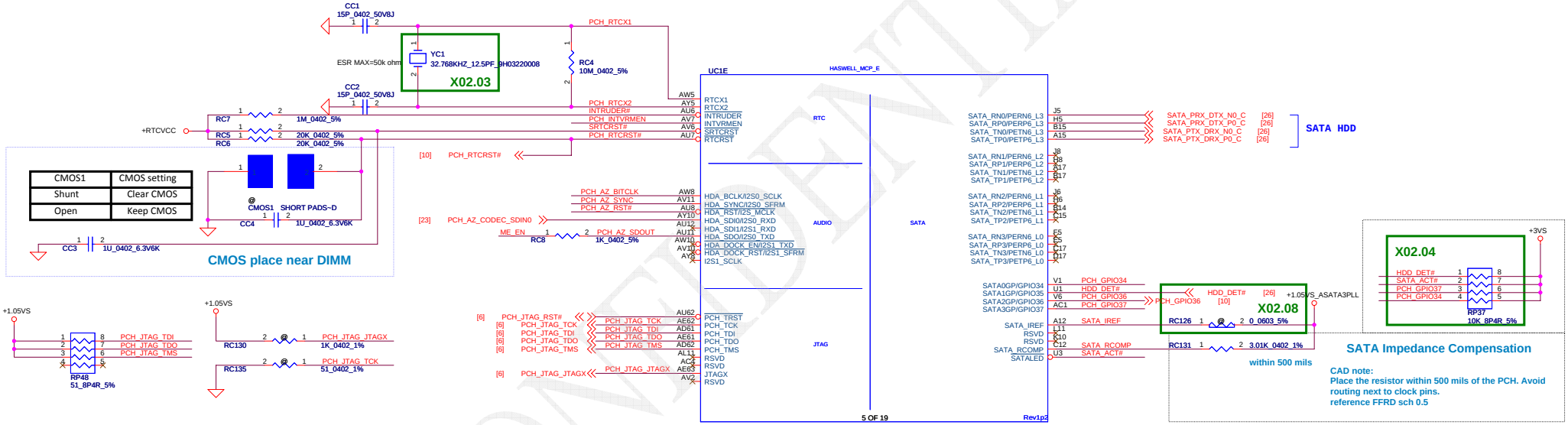


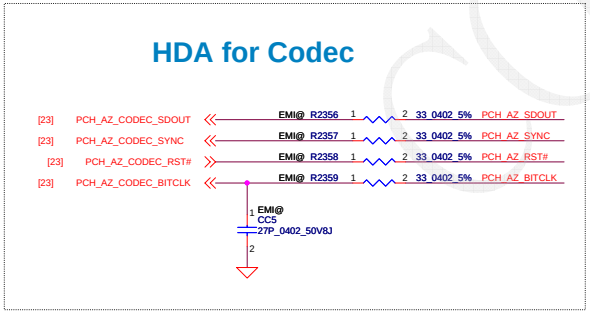
INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs





COMPRESSED IMAGE





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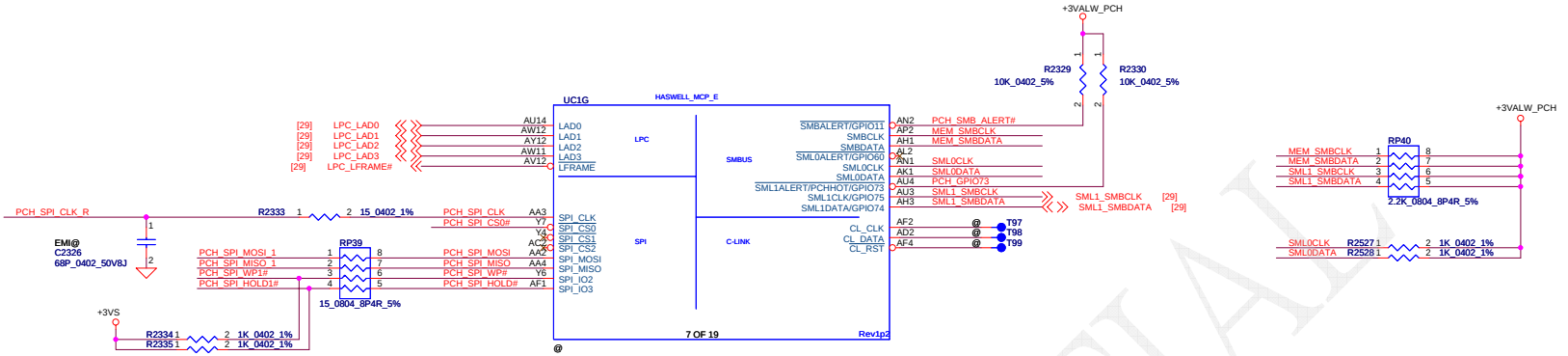
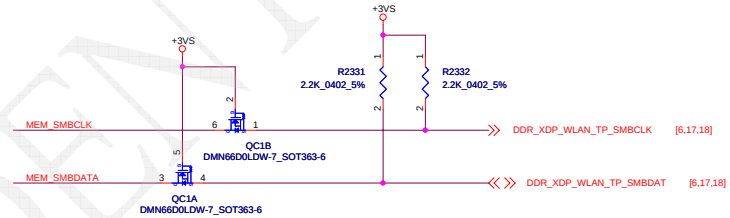
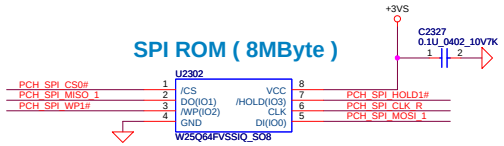


MEM Bus : DDR/XDP/WLAN/TP



SPI ROM (8MByte)



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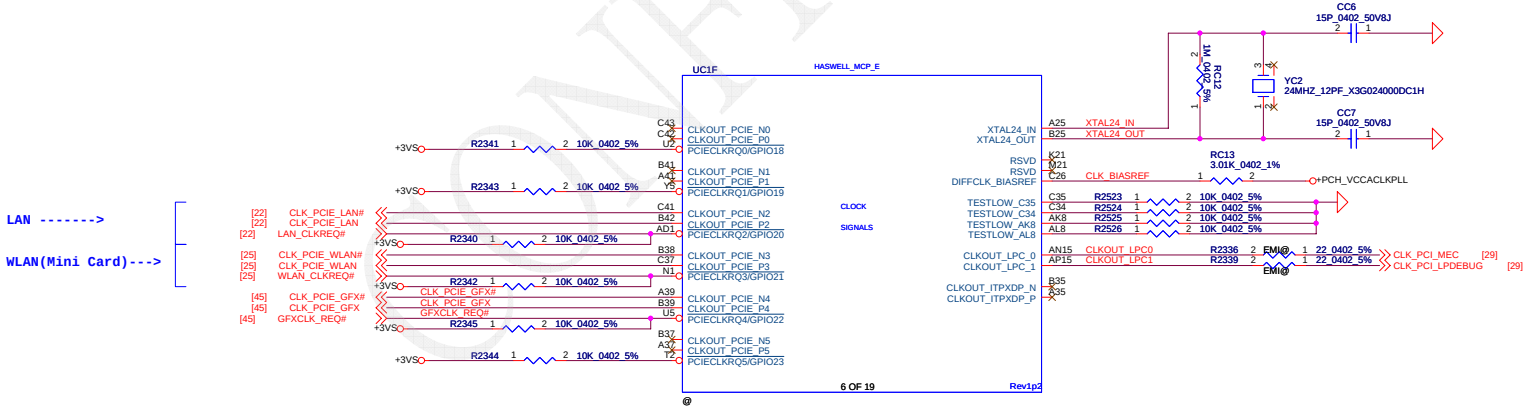

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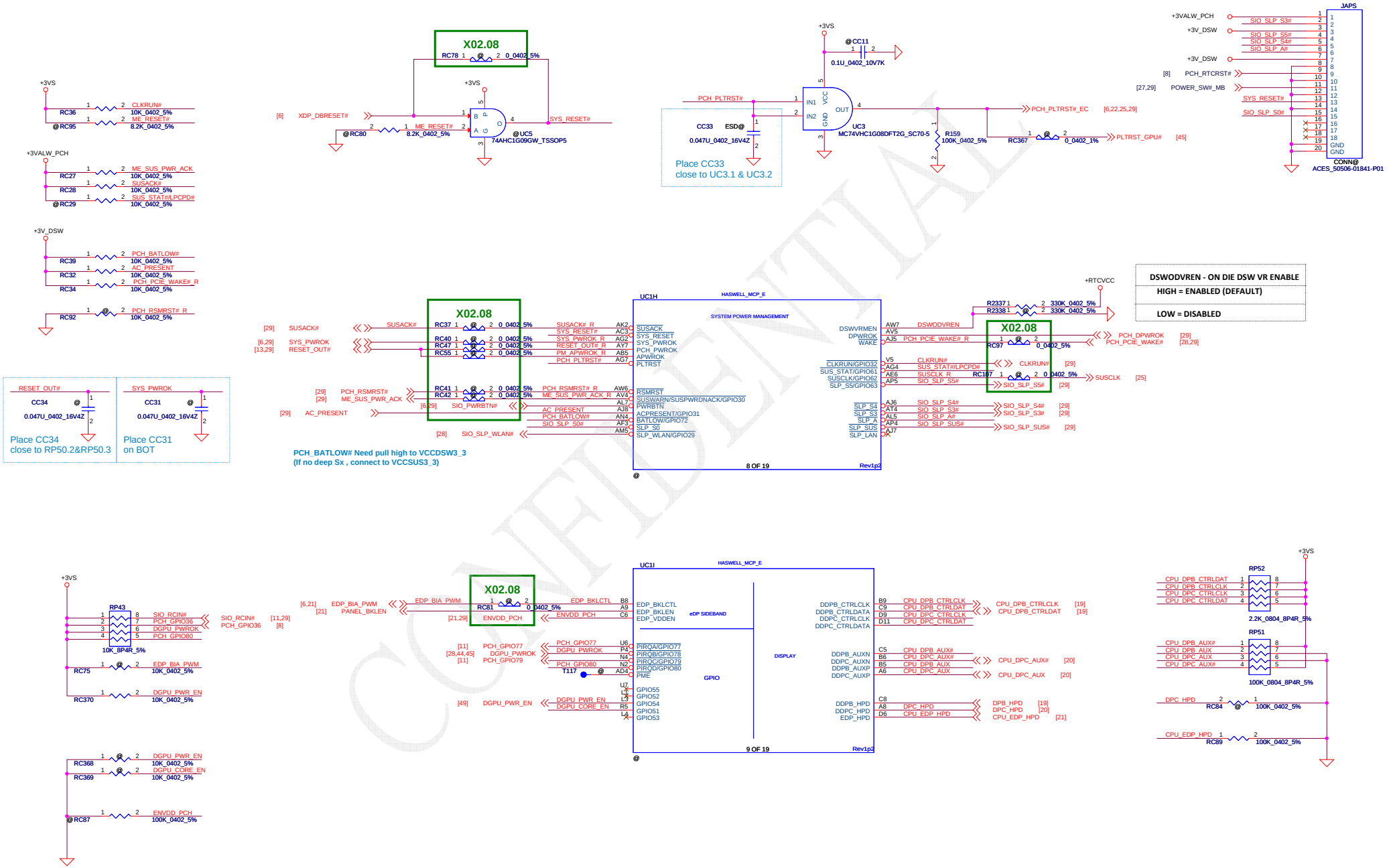

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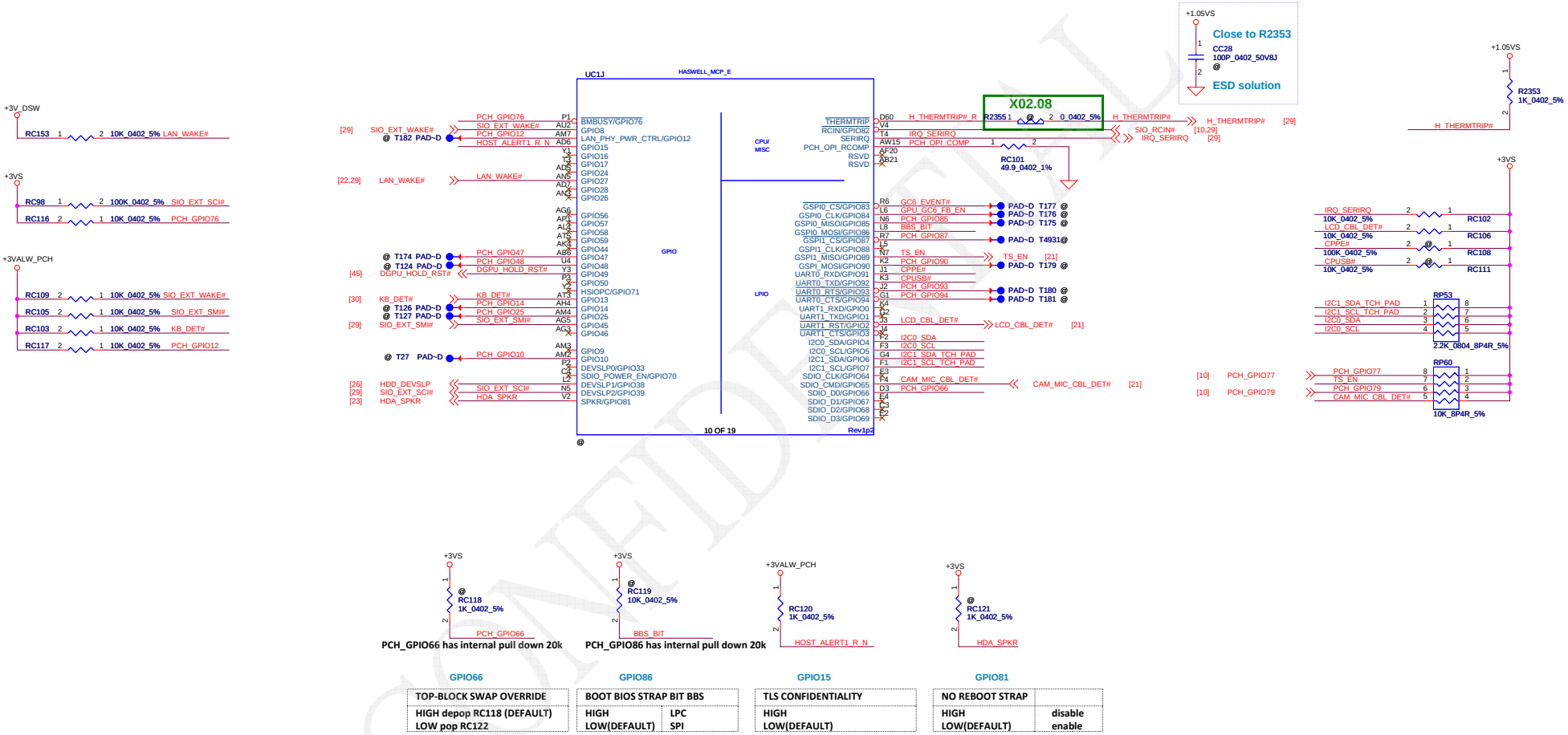

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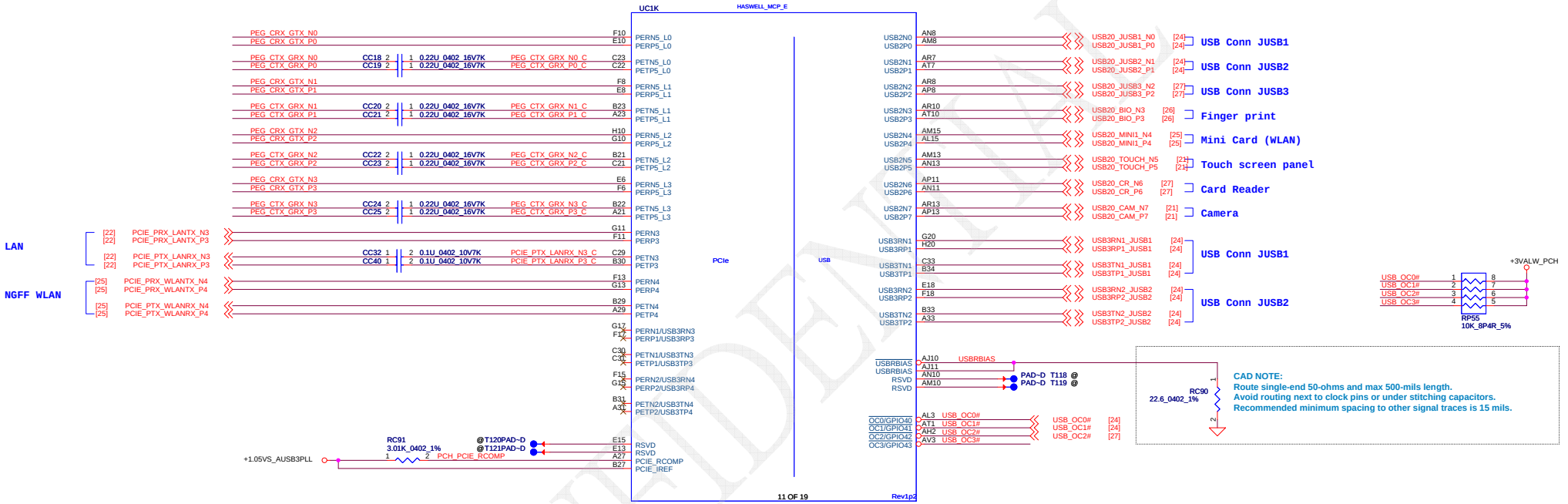
[45] PEG_CTX_GRX_P[0..3] → PEG_CTX_GRX_P[0..3]
[45] PEG_CTX_GRX_N[0..3] → PEG_CTX_GRX_N[0..3]
[45] PEG_CRX_GTX_P[0..3] → PEG_CRX_GTX_P[0..3]
[45] PEG_CRX_GTX_N[0..3] → PEG_CRX_GTX_N[0..3]



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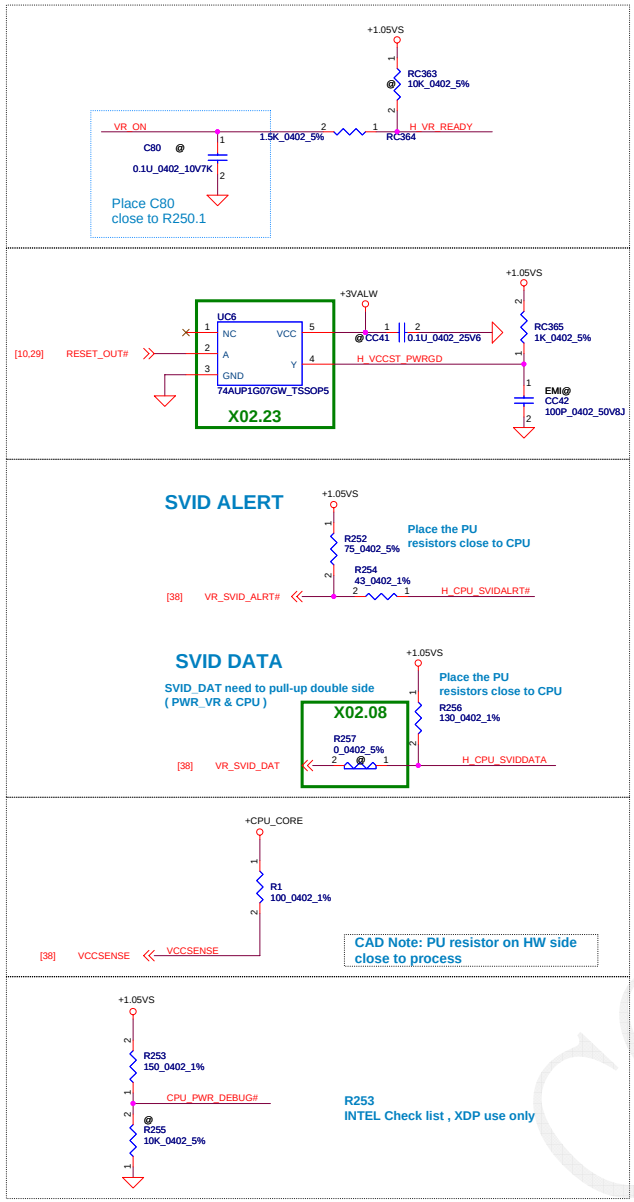

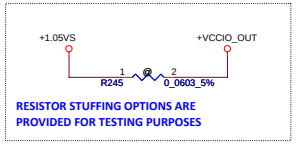

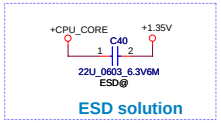

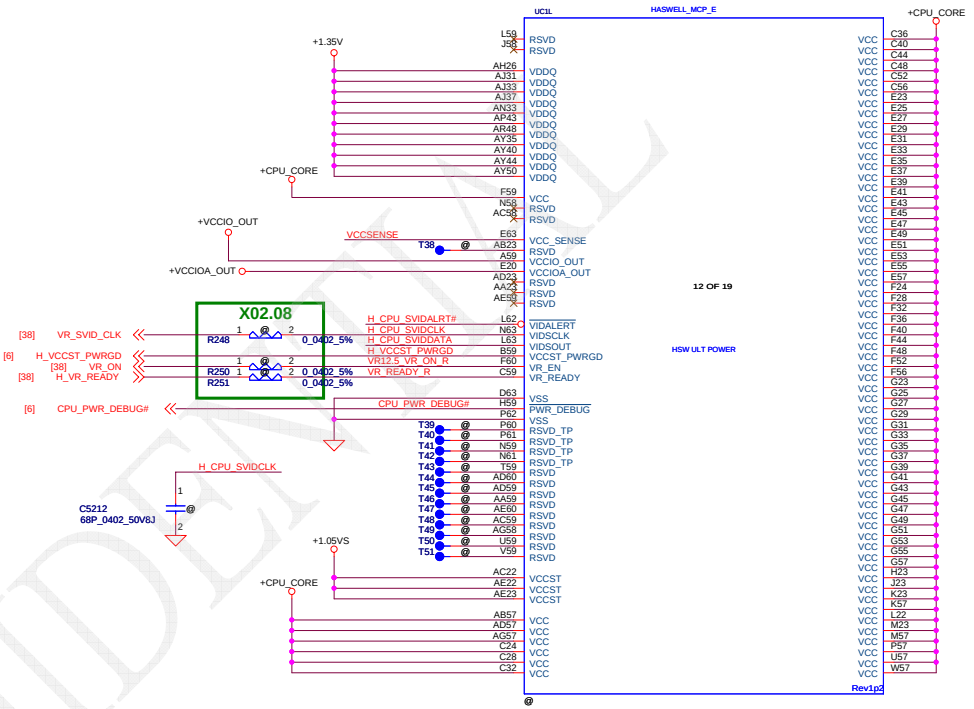

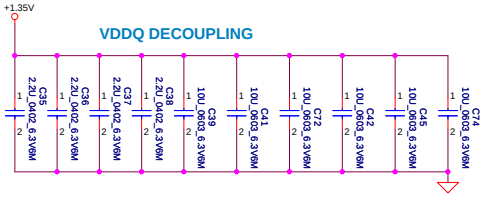

+1.35V : 470UF/2V/7343 *2 (PWR)
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

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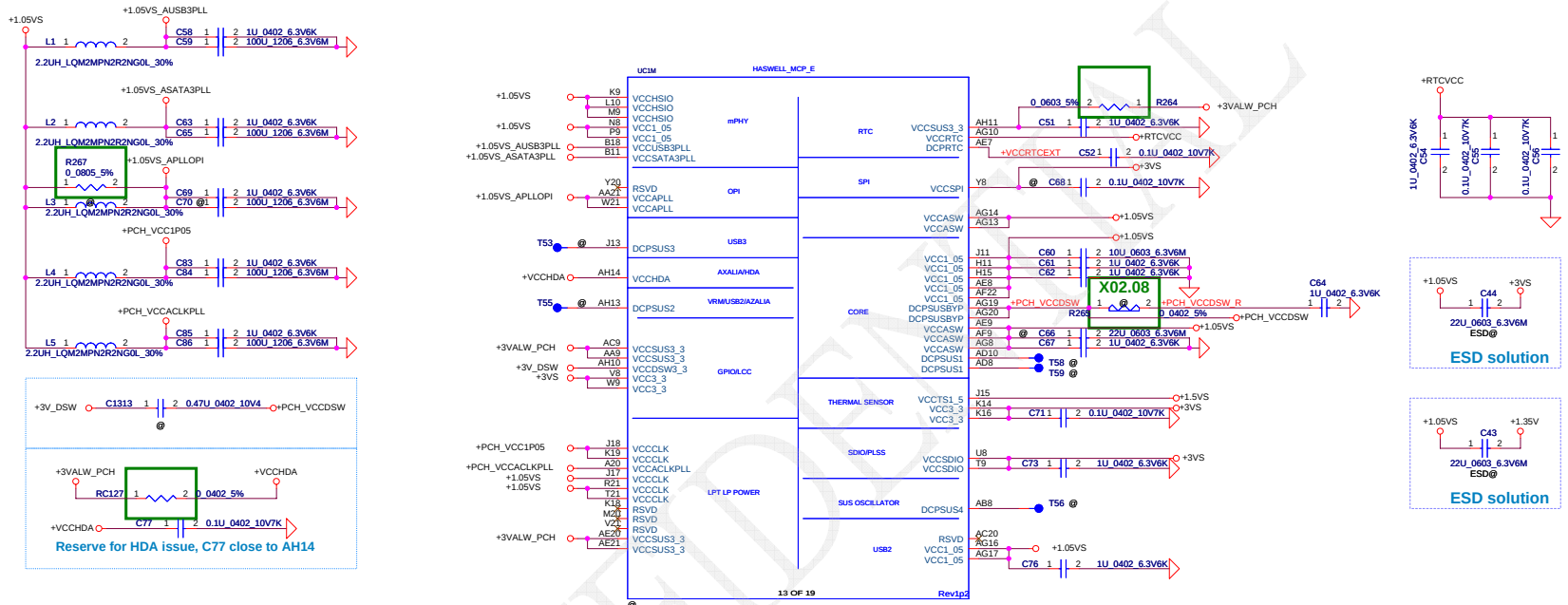

+1.05VS — C50 1U_0402_6.3V6K, C53 1U_0402_6.3V6K — Close to K9,M9

+3VALW_PCH — C81 @ 0.1U_0402_10V7K — Close to AH10

+3VALW_PCH — C78 22U_0603_6.3V6M — Close to AC9/AA9/AE20/AE21

+3VS — C82 22U_0603_6.3V6M — Close to V8

+1.05VS — C87 1U_0402_6.3V6K — Close to J17

+1.05VS — C88 1U_0402_6.3V6K — Close to R21

+1.05VS — C57 @ 1U_0402_6.3V6K — Close to N8

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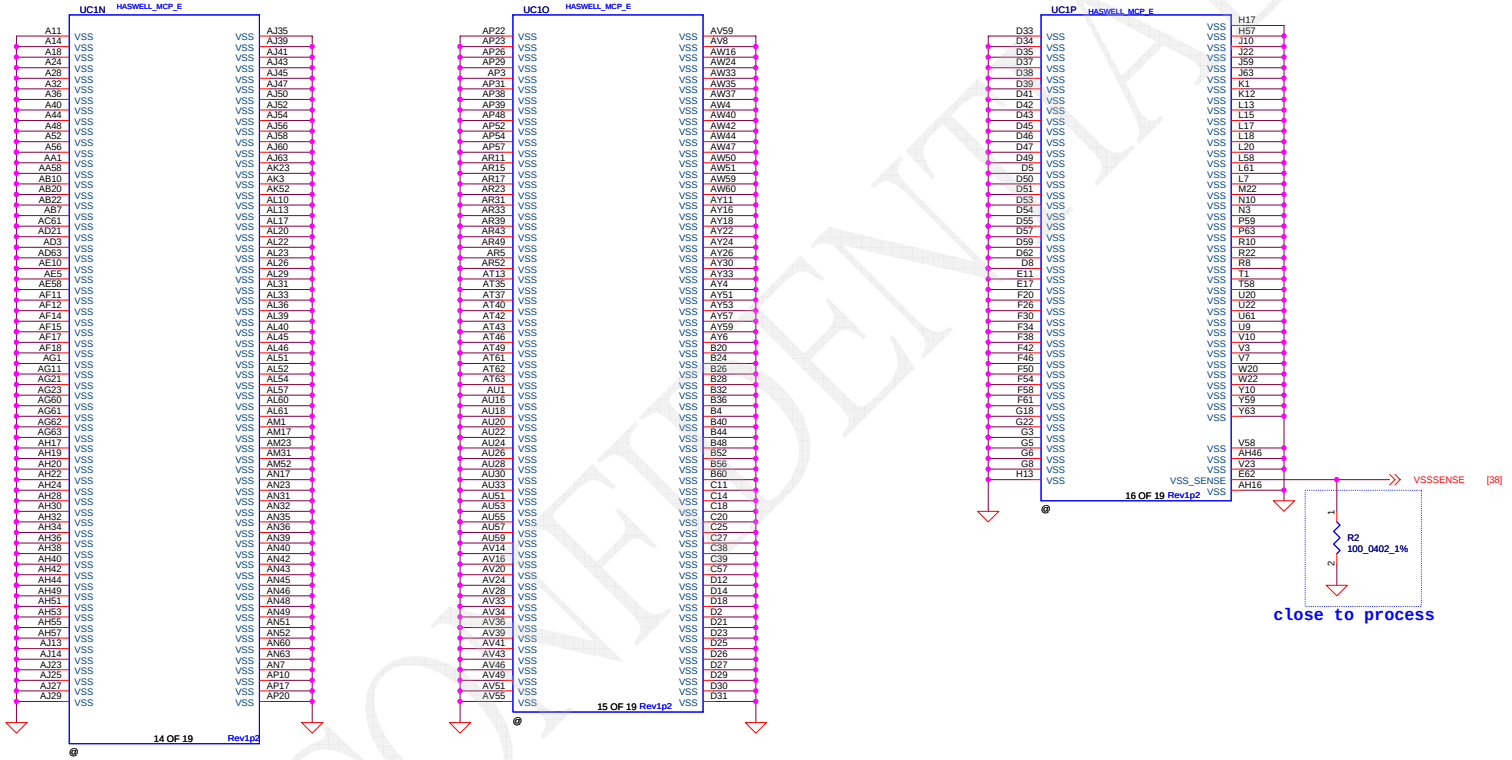

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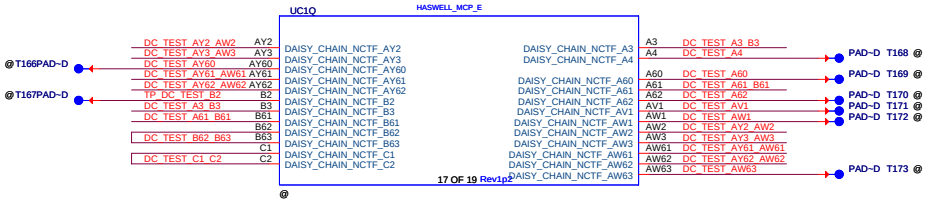
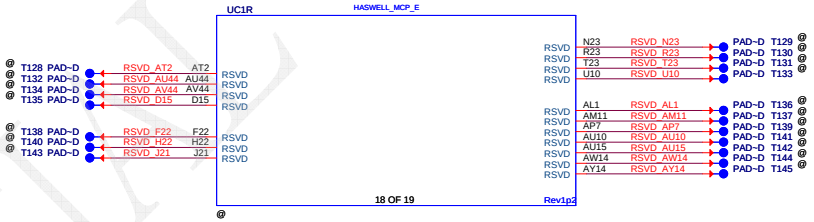
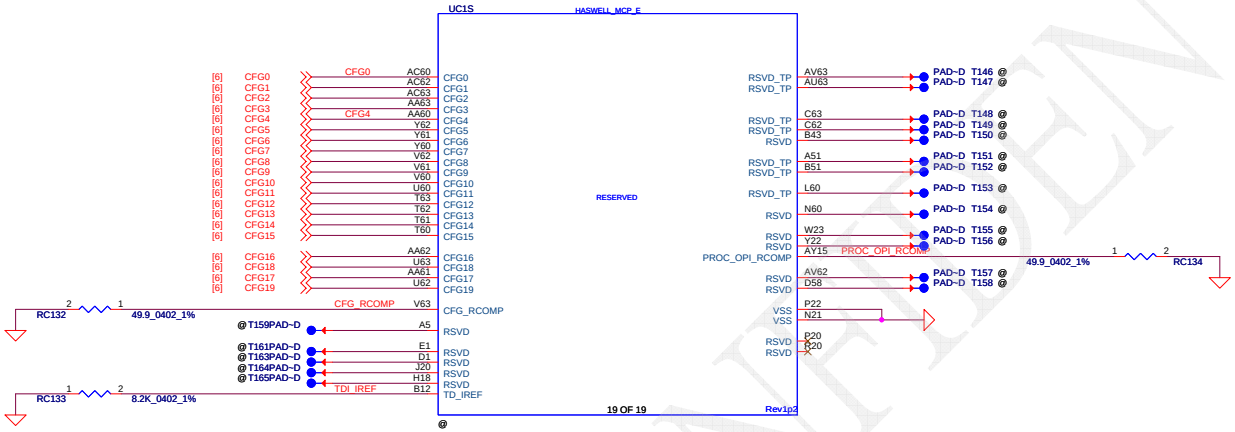
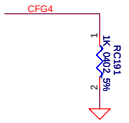


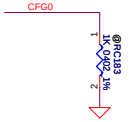




CFG STRAPS for CPU



	Display Port Presence Strap
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

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H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM1

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMM1.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

DDR3L SODIMM ODT GENERATION

Place CC31 between QD2 and R2349

ESD solution

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H=4mm

2-3A to 1 DIMMs/channel

Populate RD4, De-Populate RD8 for Intel DDR3 VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

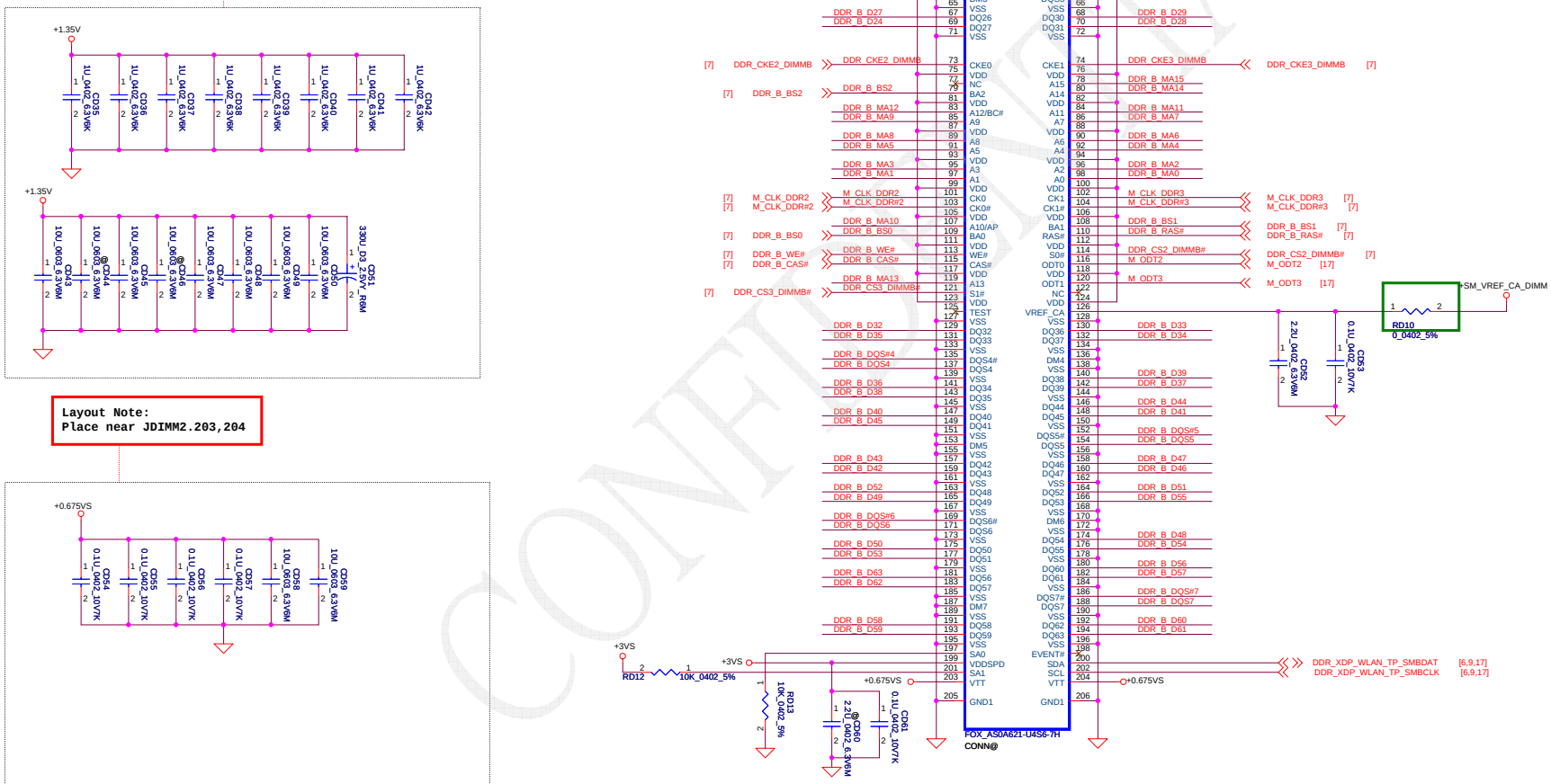
Layout Note: Place near JDIMM2

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMM2.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

JDIMM2
FOX_AS0A621-U4S6-7H
CONN@



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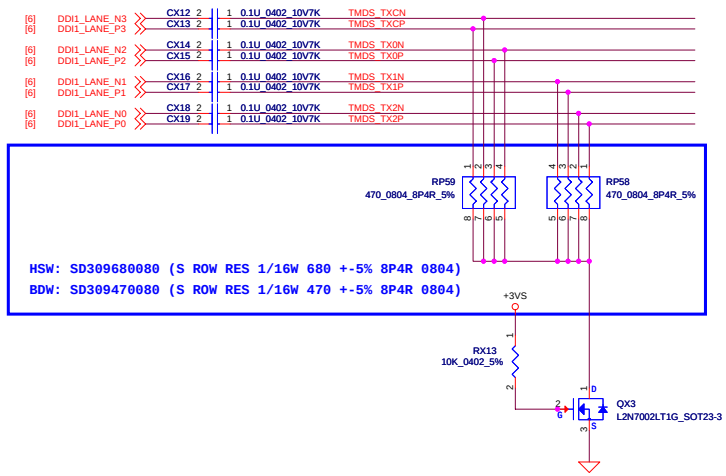

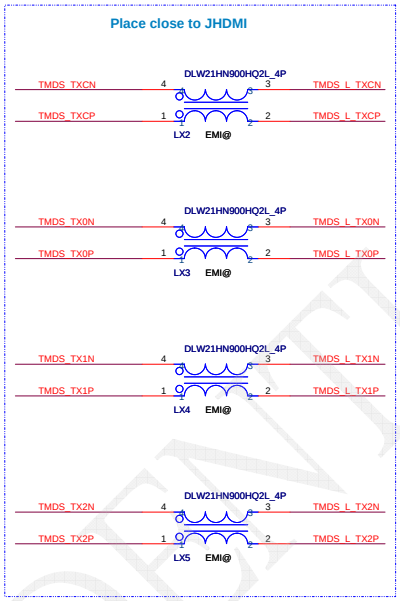

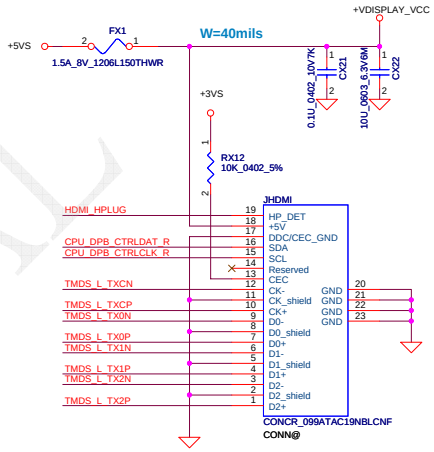

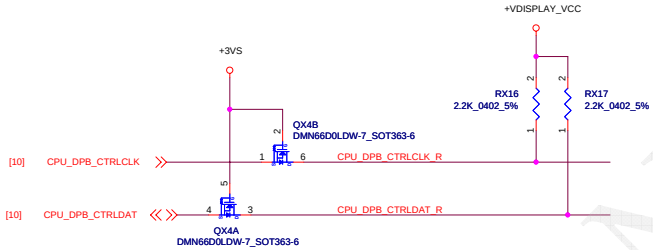

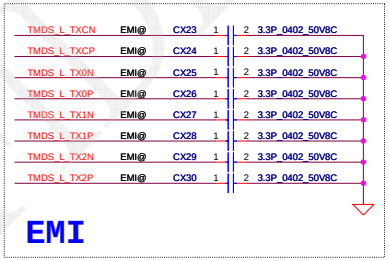

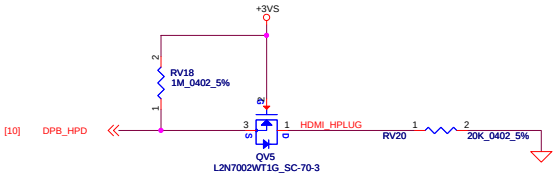

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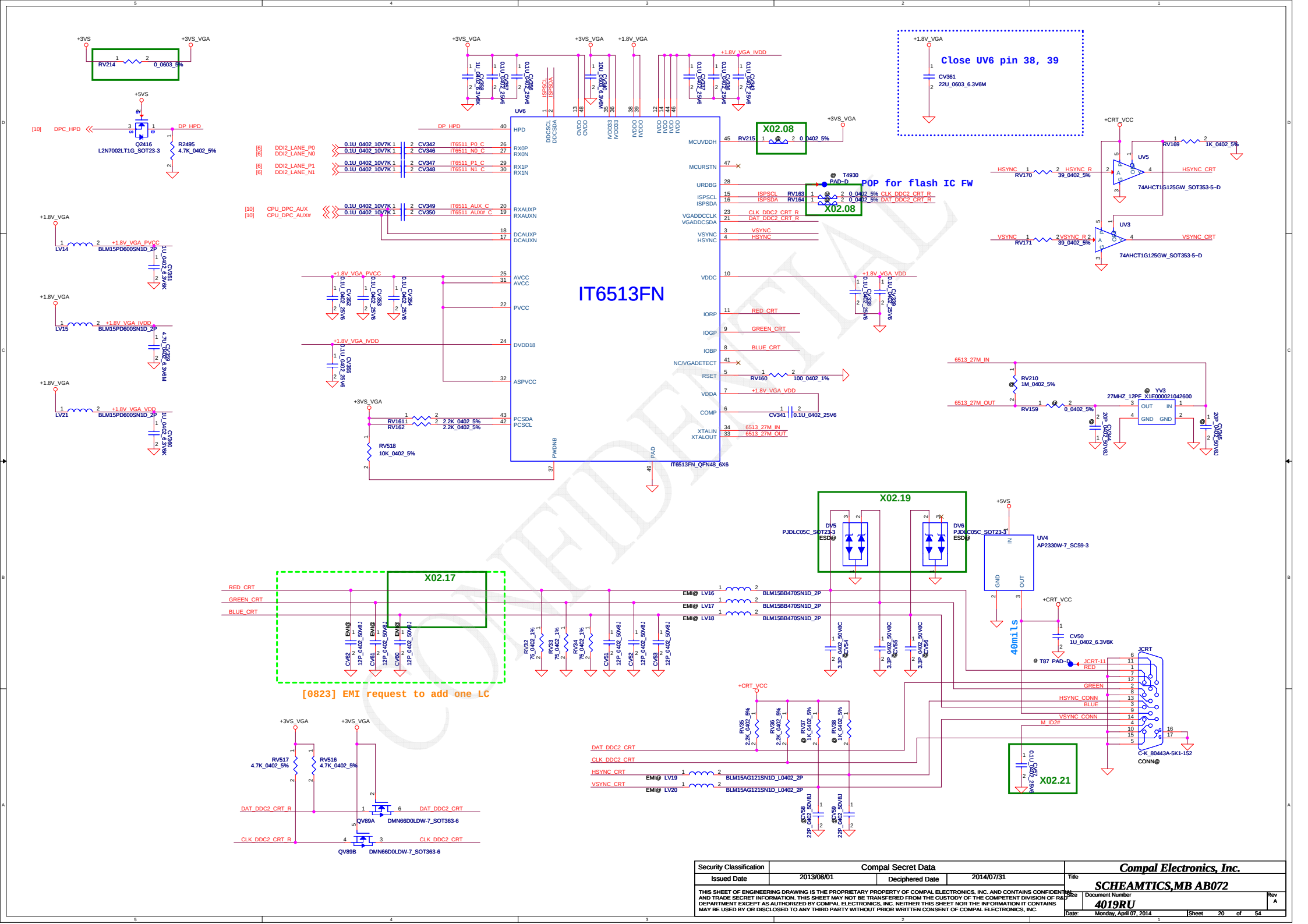
IT6513FN
Close UV6 pin 38, 39
POP for flash IC FW
X02.08
X02.19
X02.17
X02.21
[0823] EMI request to add one LC
40mils
Compal Electronics, Inc.
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2013/08/01
2014/07/31
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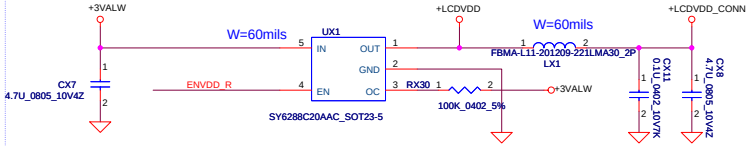
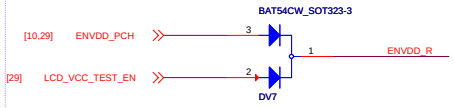
CONFIDENTIAL

LCD PWR CTRL

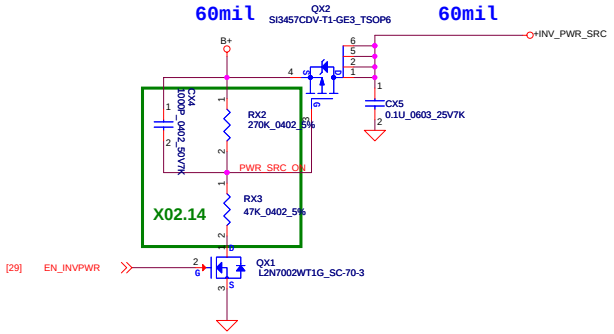




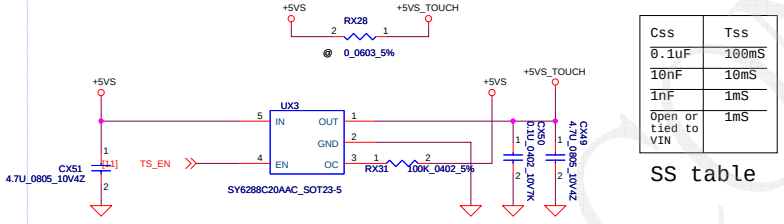
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

SS table

LCD backlight PWR CTRL



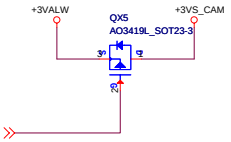
* Touch Screen Panel

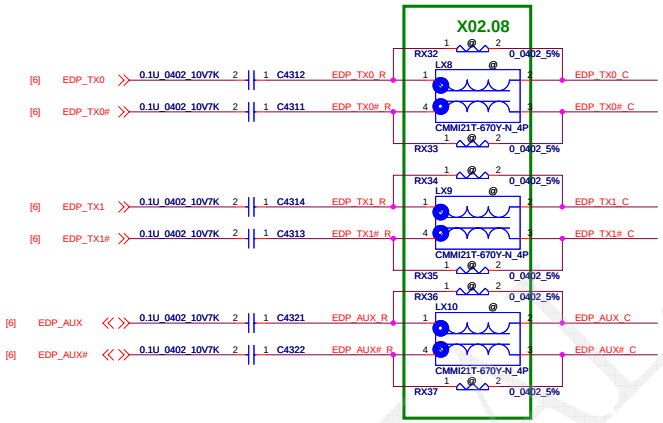


Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

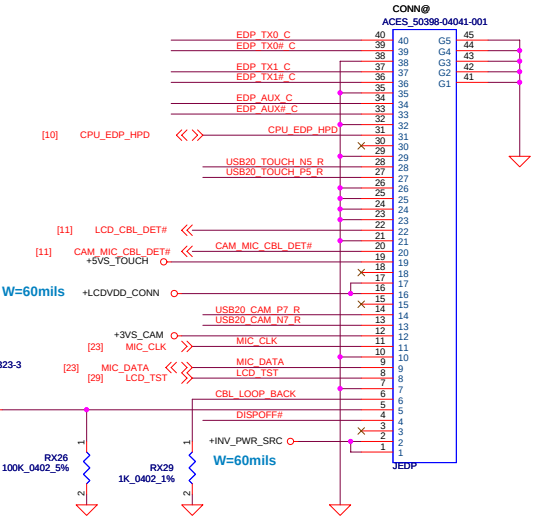
SS table

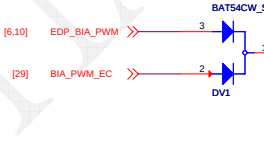
Webcam PWR CTRL

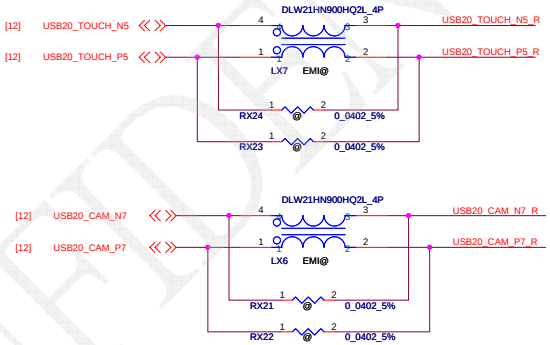


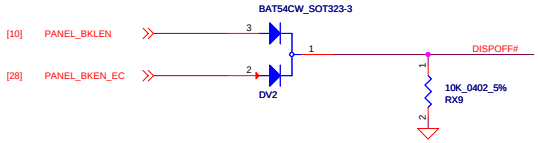


eDP Connector

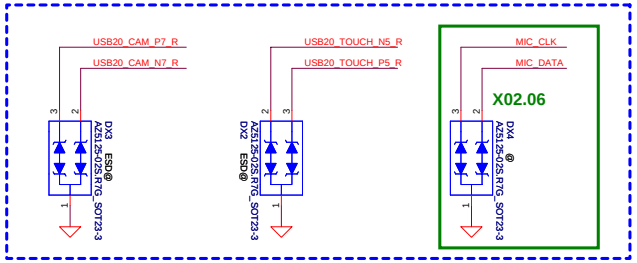


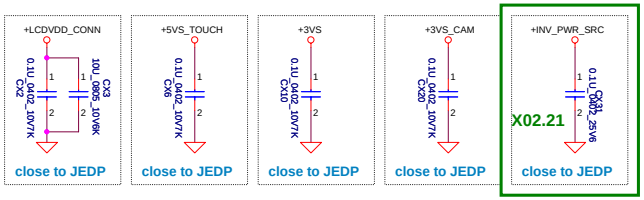






close to JEDP





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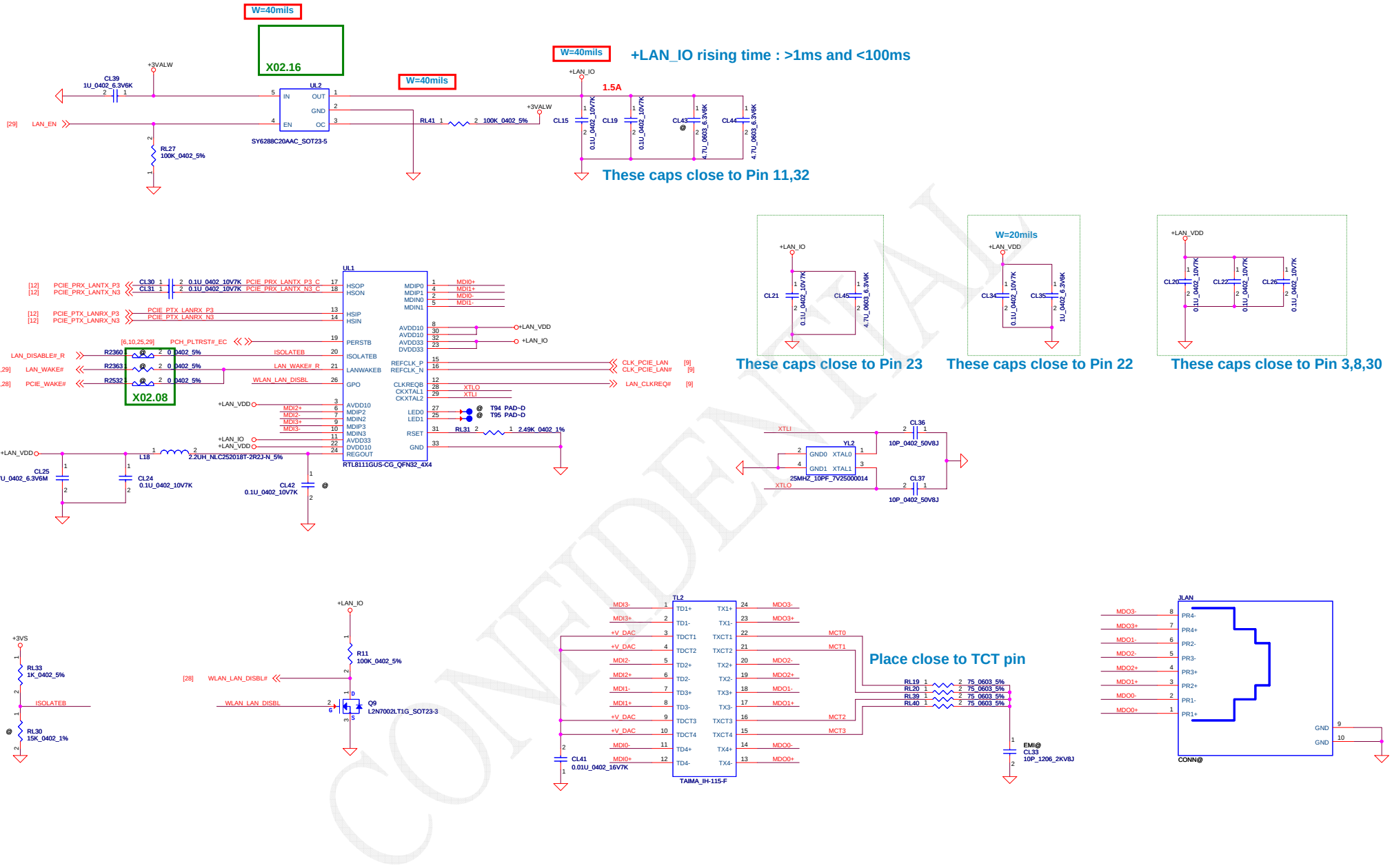

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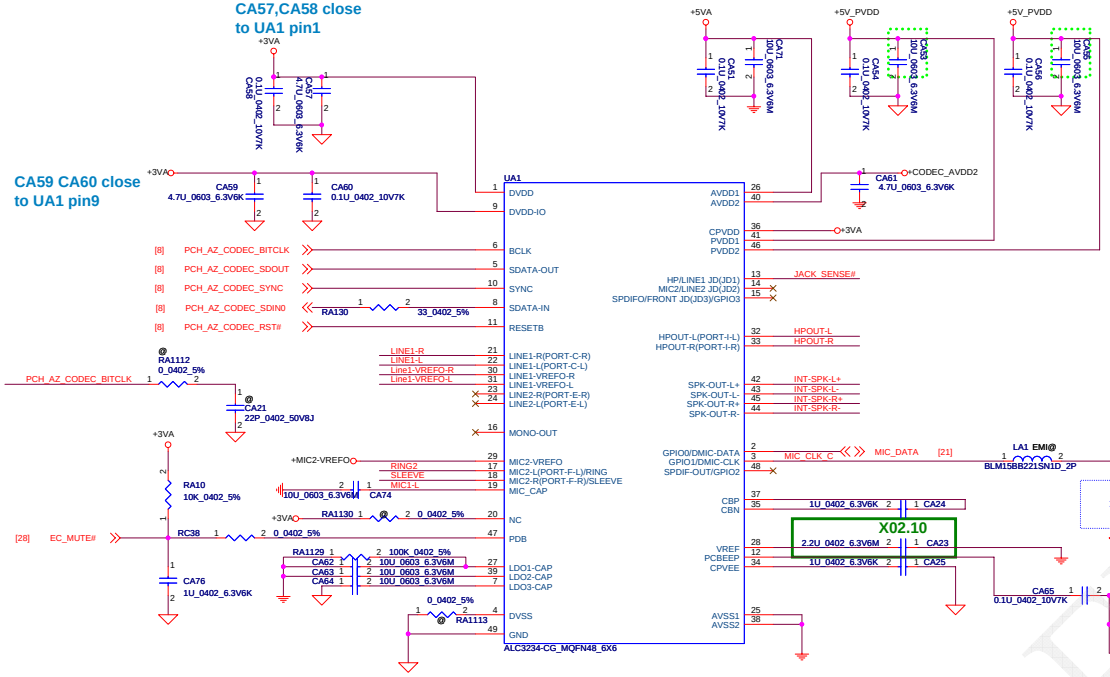
CA71, CA51 place close to Pin 26

CA53, CA55 change Value from 10U_0603_6.3V6M~D to 4.7U_0603_6.3V6K

CA57,CA58 close to UA1 pin1

CA59 CA60 close to UA1 pin9



close PIN36

close PIN3

X02.10

X02.08

Place on the moat between GND & GNDA.

GNDA GND

EC Beep

MCU Beep

PC Beep

Close to UA1 Pin11,13,14,16

close to Codec

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

iPhone and Nokia type Combo Jack

normal open

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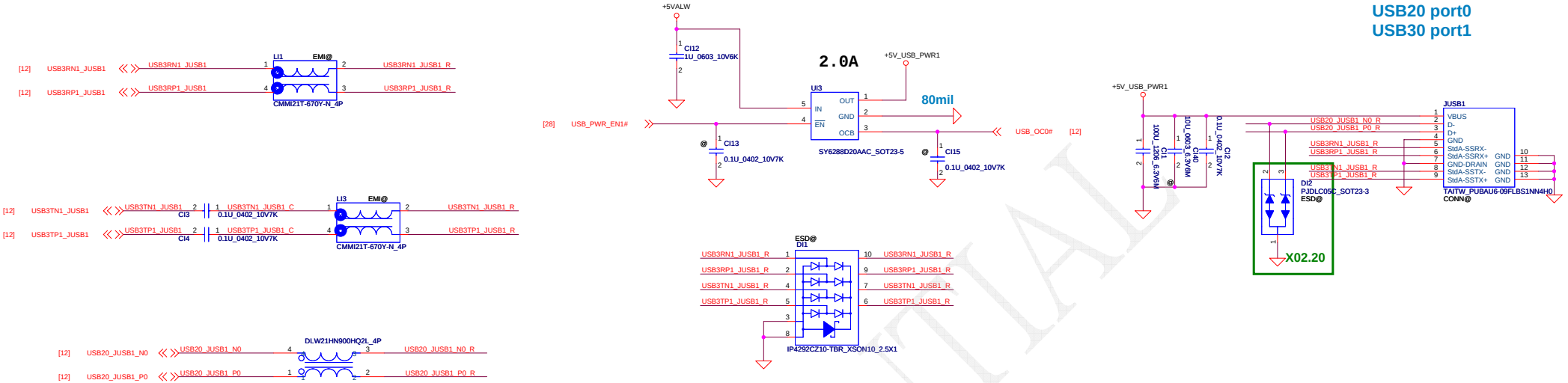
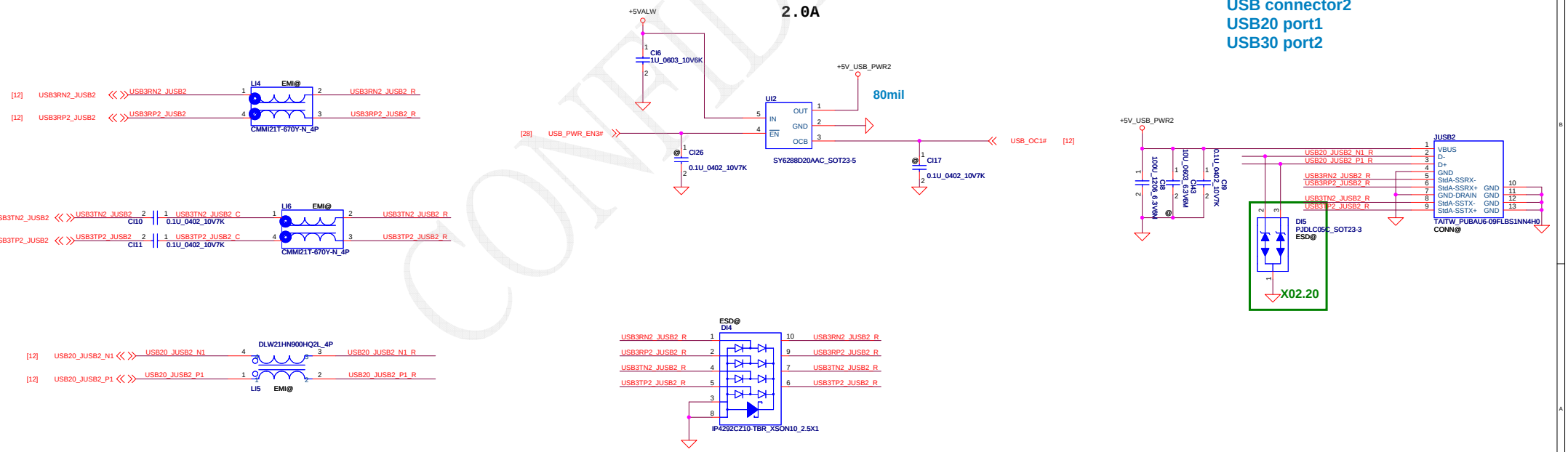
USB connector1
USB20 port0
USB30 port1



USB connector2
USB20 port1
USB30 port2



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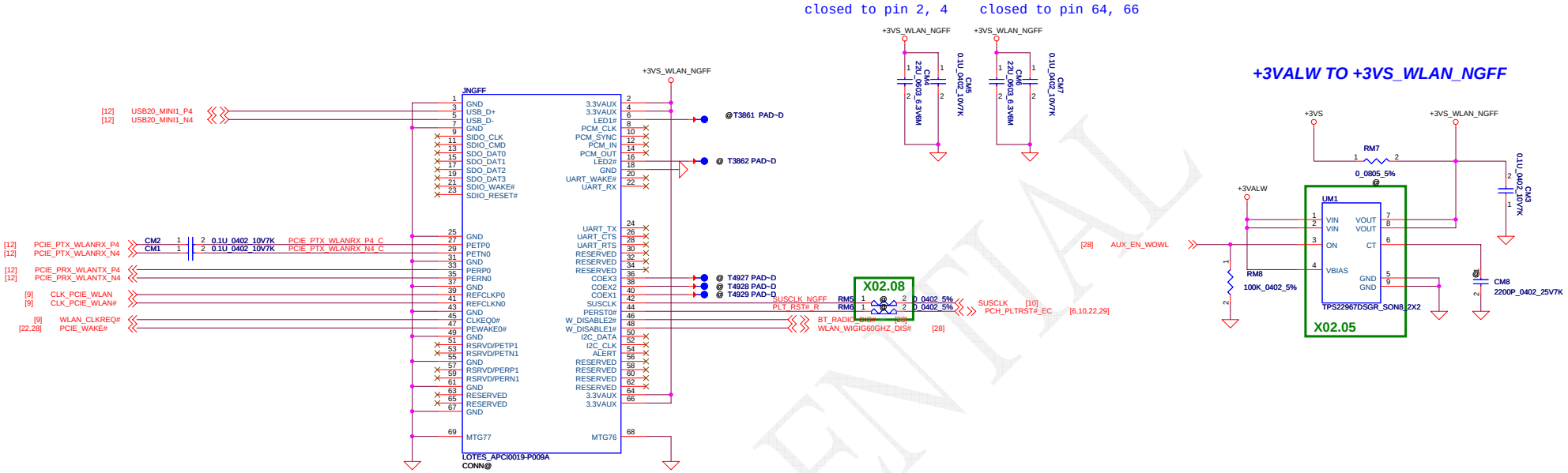

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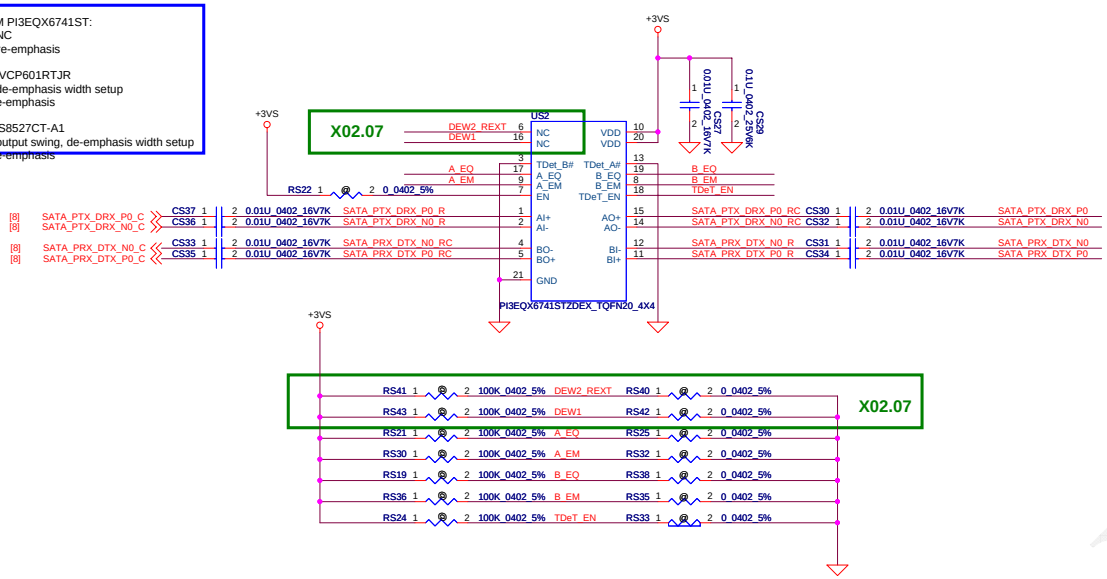
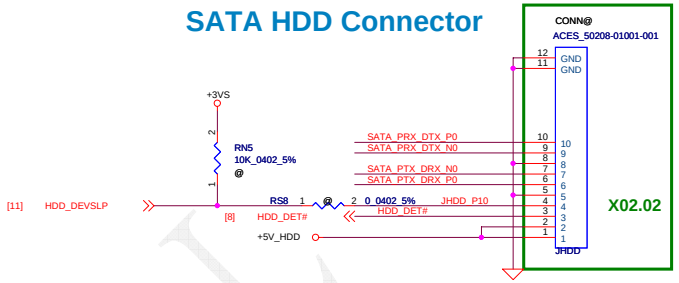
PERICOM PI3EQX6741ST:
Pin6/16, NC
Pin8/9, Pre-emphasis

TI SN75LVCP601RTJR
Pin6/16, de-emphasis width setup
Pin8/9, de-emphasis

Parade PS8527CT-A1
Pin6/16, output swing, de-emphasis width setup
Pin8/9, de-emphasis



SATA HDD Connector



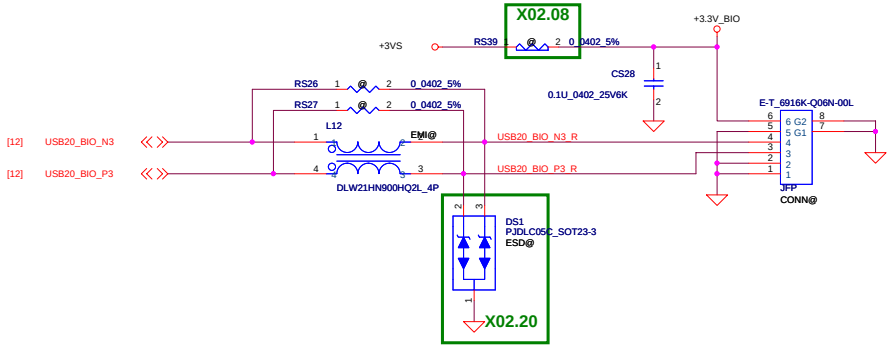
+5V_HDD Source

	DEW2 PIN6	B_EM PIN8	A_EM PIN9	TDeT_A PIN13	DEW1 PIN16	A_EQ PIN17	TDeT_EN PIN18	B_EQ PIN19
Pericom PI3EQX6741ST	NC	PD (RS35)	NC (IPU)	PD	NC	NC	PU (RS24)	PD (RS38)
TI SN75LVCP601	NC (IPU)	PD (RS35)	PD (RS32)	PD	NC (IPU)	PD (RS25)	PD (RS33)	NC
Parade PS8527C	PD (RS40)	PD (RS35)	PU (RS30)	PD	NC	PD (RS25)	PD (RS33)	NC

			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0	3dB	3dB	0	0dB	0dB
		NC	6dB	6dB	NC		
		1	9dB	9dB	1	1.5dB	1.5dB
2nd	TI	0	7dB	7dB	0	0dB	0dB
		NC	0dB	0dB	NC	-6dB	-6dB
		1	14dB	14dB	1	-3dB	-3dB
3rd	Parade	EQ2 EQ1 (M = VDD/2)	A_EQ	B_EQ		A_EM	B_EM
		0 M	2.4dB	2.4dB			
		0 0	7.4dB	7.4dB			
		0 1	14.4dB	14.4dB	0	0dB	0dB
		M M	12.2dB	12.2dB	M	-3.5dB	-3.5dB
		M 0	9.4dB	9.4dB	1	-1.5dB	-1.5dB
		M 1	13.3dB	13.3dB			
		1 M	6.2dB	6.2dB			
		1 0	11.2dB	11.2dB			
		1 1	5dB	5dB			

* red color is current setting

Finger print



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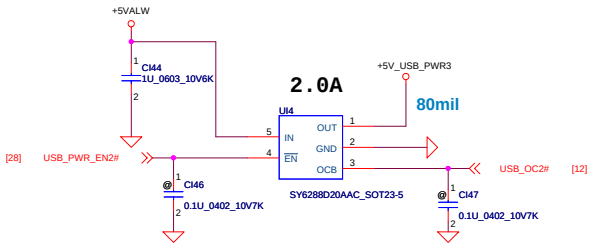
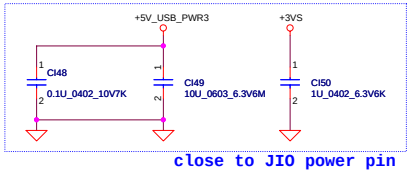
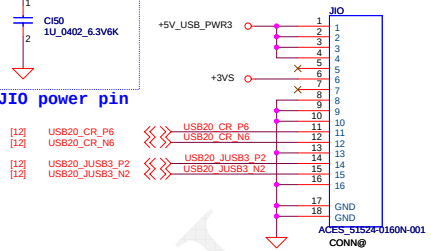


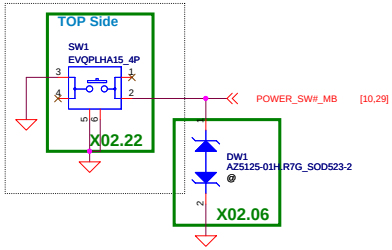


close to JIO power pin

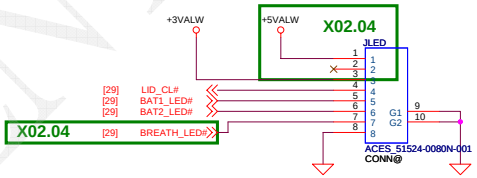
IO to MB CONN

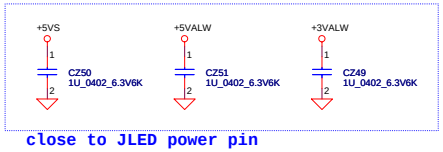


ON/OFF switch



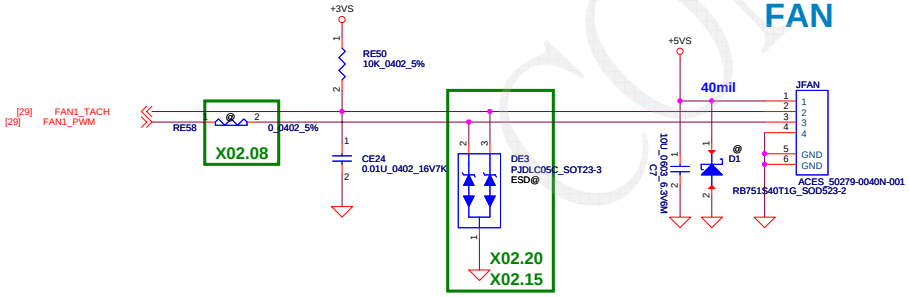
LED/B TO M/B



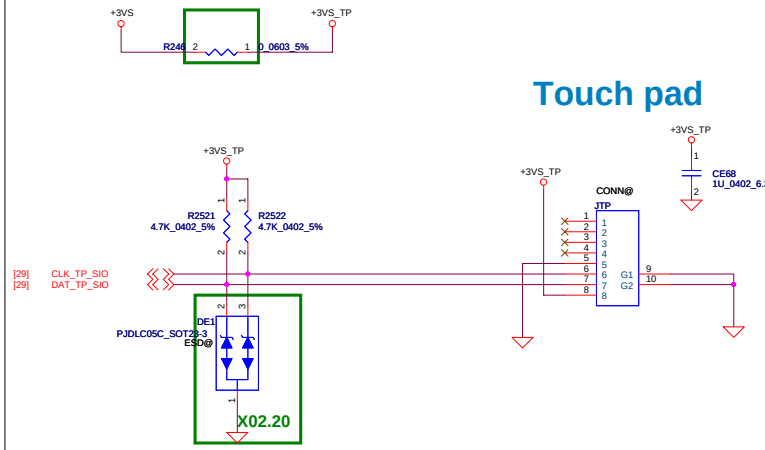


close to JLED power pin

FAN



Touch pad



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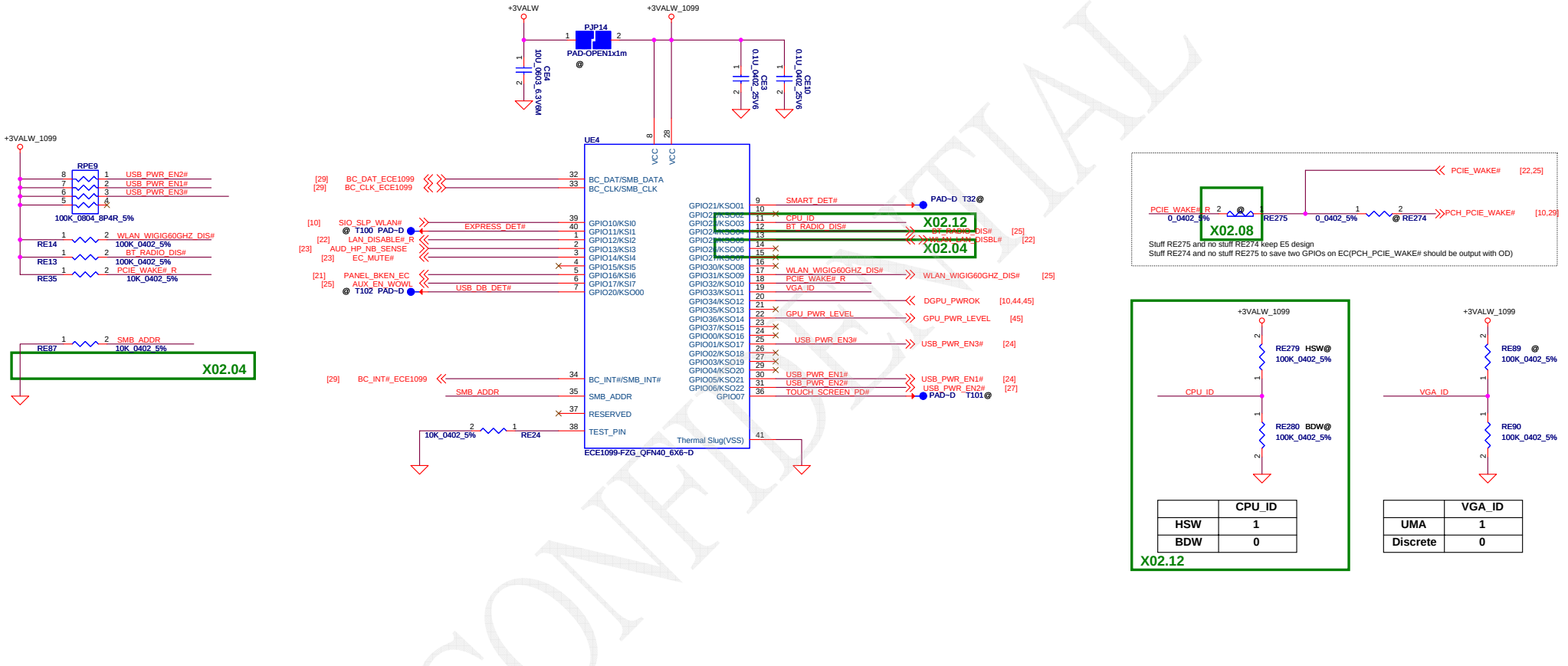

	CPU_ID
HSW	1
BDW	0

	VGA_ID
UMA	1
Discrete	0

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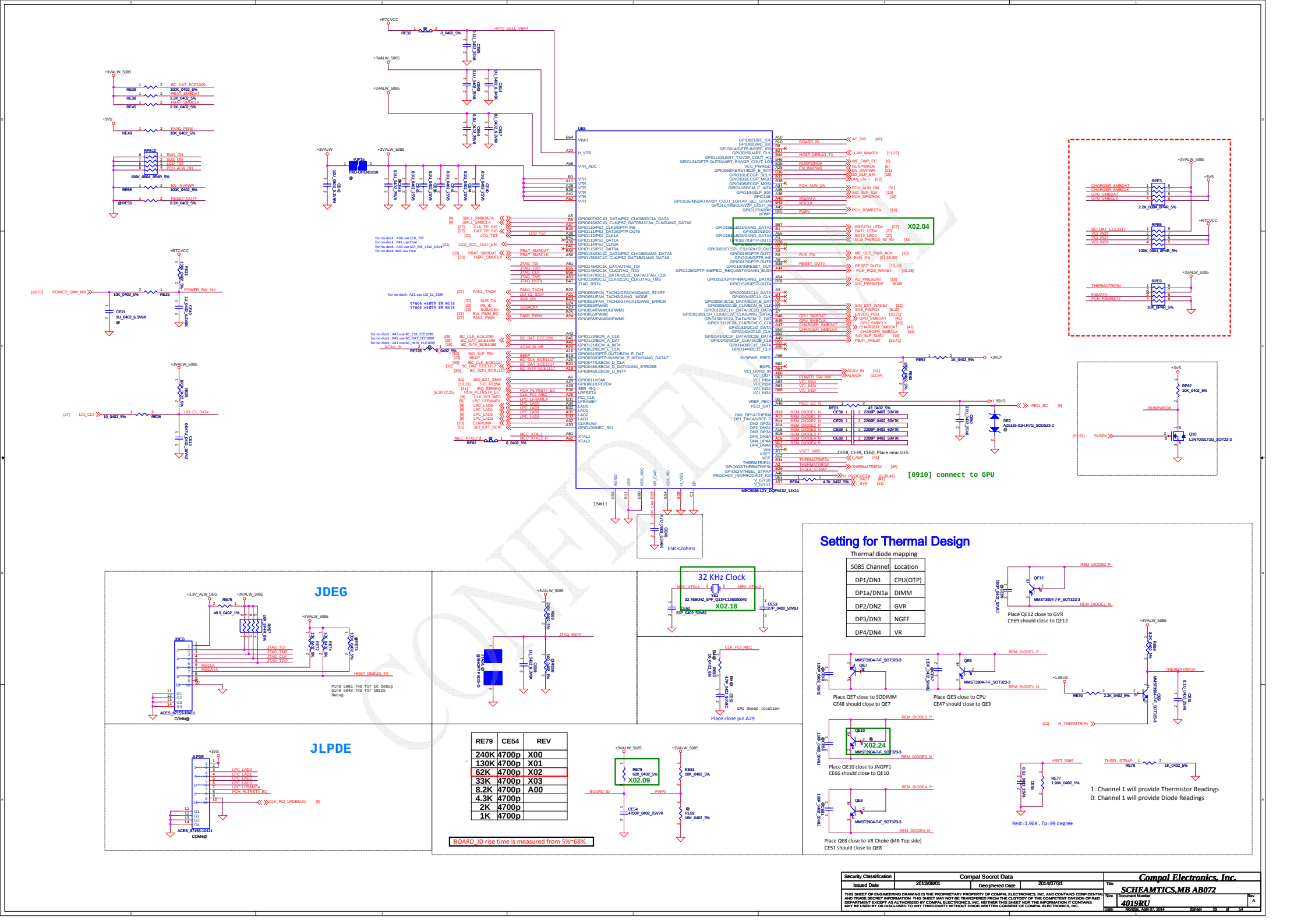
UE5
MEC5085-LZY_DQFN132_11X11
X02.04
[0910] connect to GPU
Setting for Thermal Design
Thermal diode mapping
5085 Channel | Location
DP1/DN1 | CPU(OTP)
DP1a/DN1a | DIMM
DP2/DN2 | GVR
DP3/DN3 | NGFF
DP4/DN4 | VR
Place QE12 close to GVR
CE69 should close to QE12
Place QE7 close to SODIMM
CE48 should close to QE7
Place QE3 close to CPU
CE47 should close to QE3
Place QE10 close to JNGFF1
CE66 should close to QE10
Place QE8 close to VR Choke (MB Top side)
CE51 should close to QE8
Rest=1.96K , Tp=99 degree
1: Channel 1 will provide Thermistor Readings
0: Channel 1 will provide Diode Readings
JDEG
JLPDE
32 KHz Clock
X02.18
X02.24
X02.09
RE79 | CE54 | REV
240K | 4700p | X00
130K | 4700p | X01
62K | 4700p | X02
33K | 4700p | X03
8.2K | 4700p | A00
4.3K | 4700p
2K | 4700p
1K | 4700p
BOARD_ID rise time is measured from 5%~68%.
ESR <2ohms
Place close pin A29
EMI depop location
Pin9 5085_TXD for EC Debug
pin9 5848_TXD for 5851DS debug
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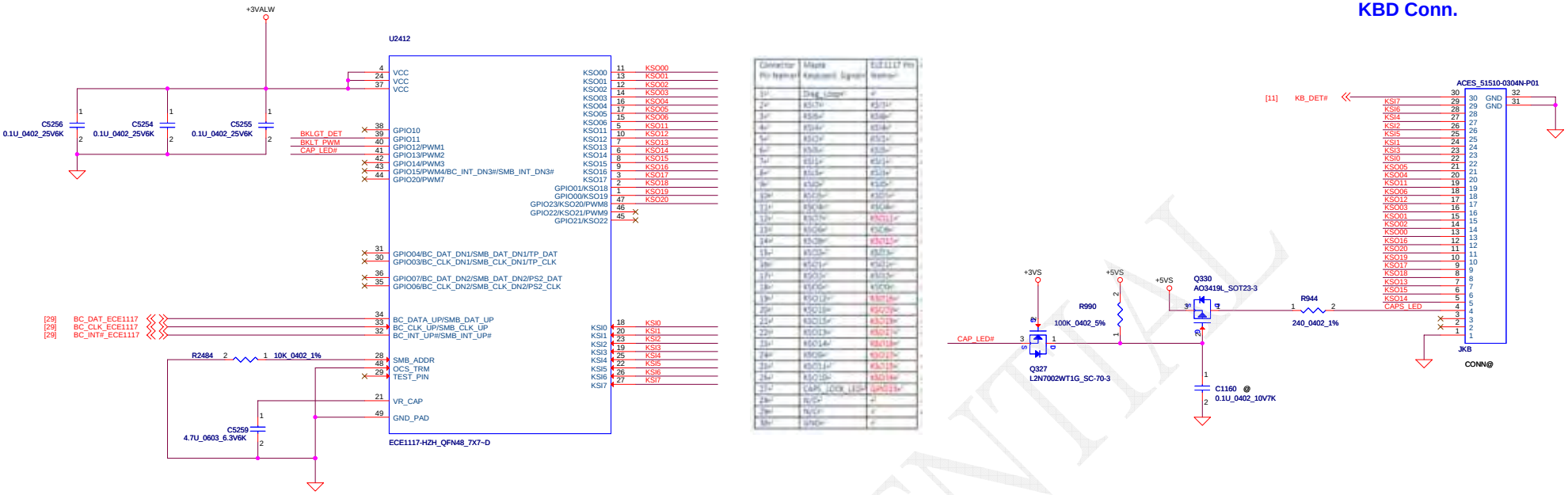
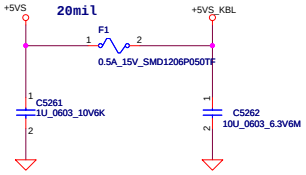
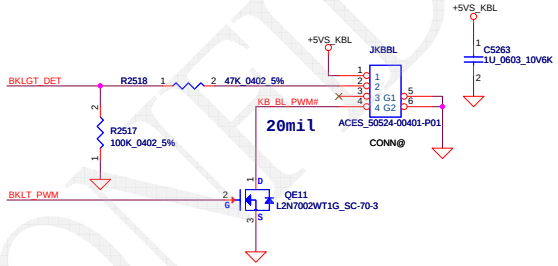
KBD Conn.







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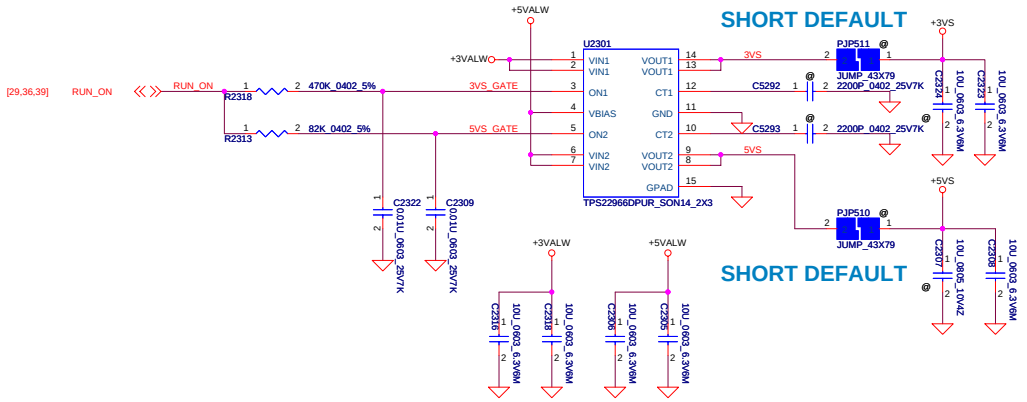
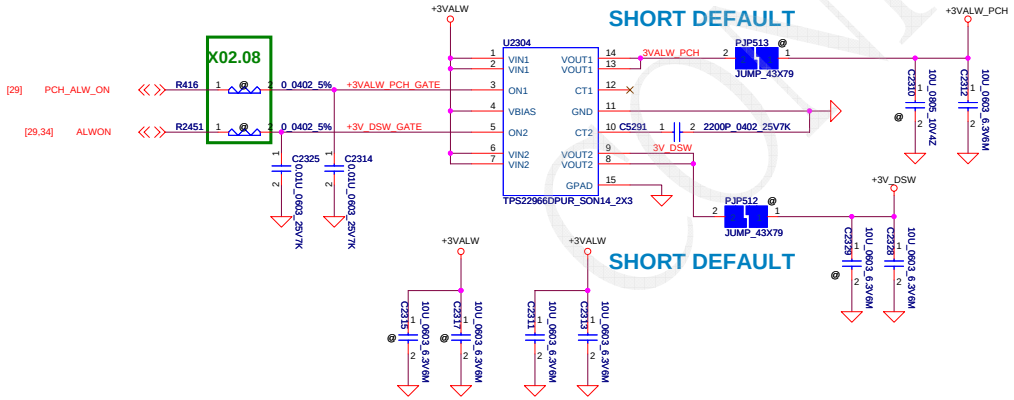
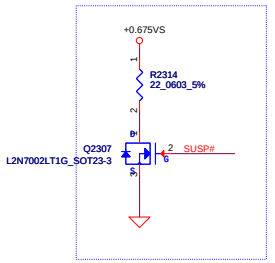
+5VS and +3VS switch

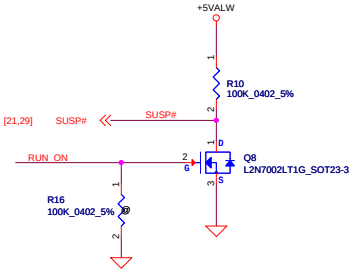


+3VALW_PCH switch





For Intel S3 Power Reduction



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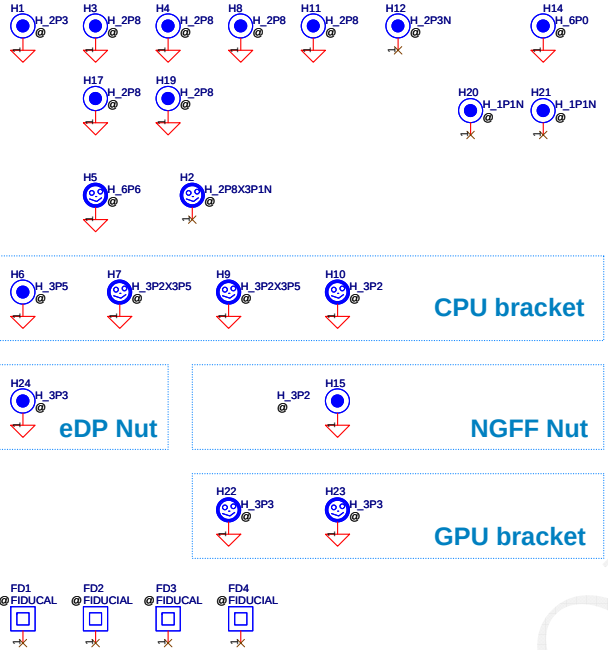
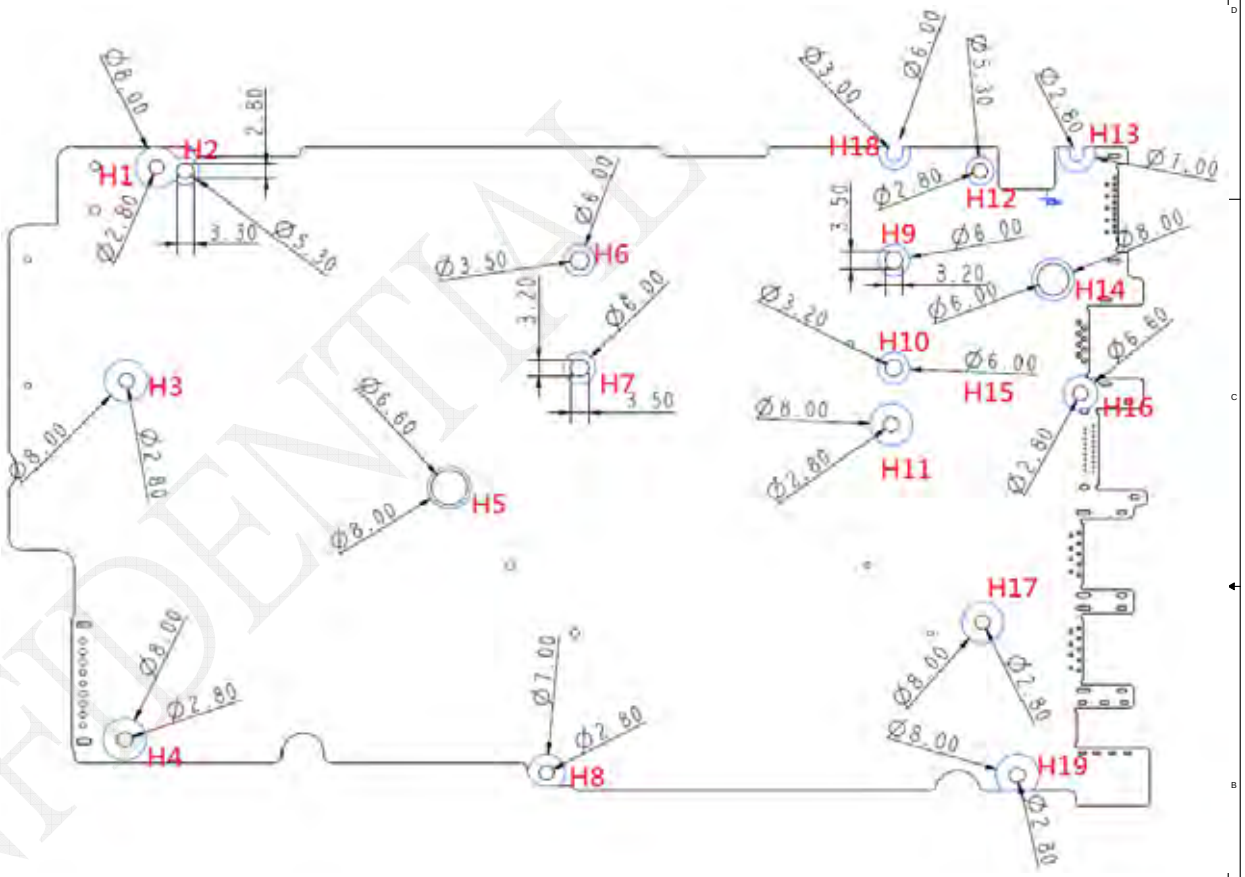
Screw Hole





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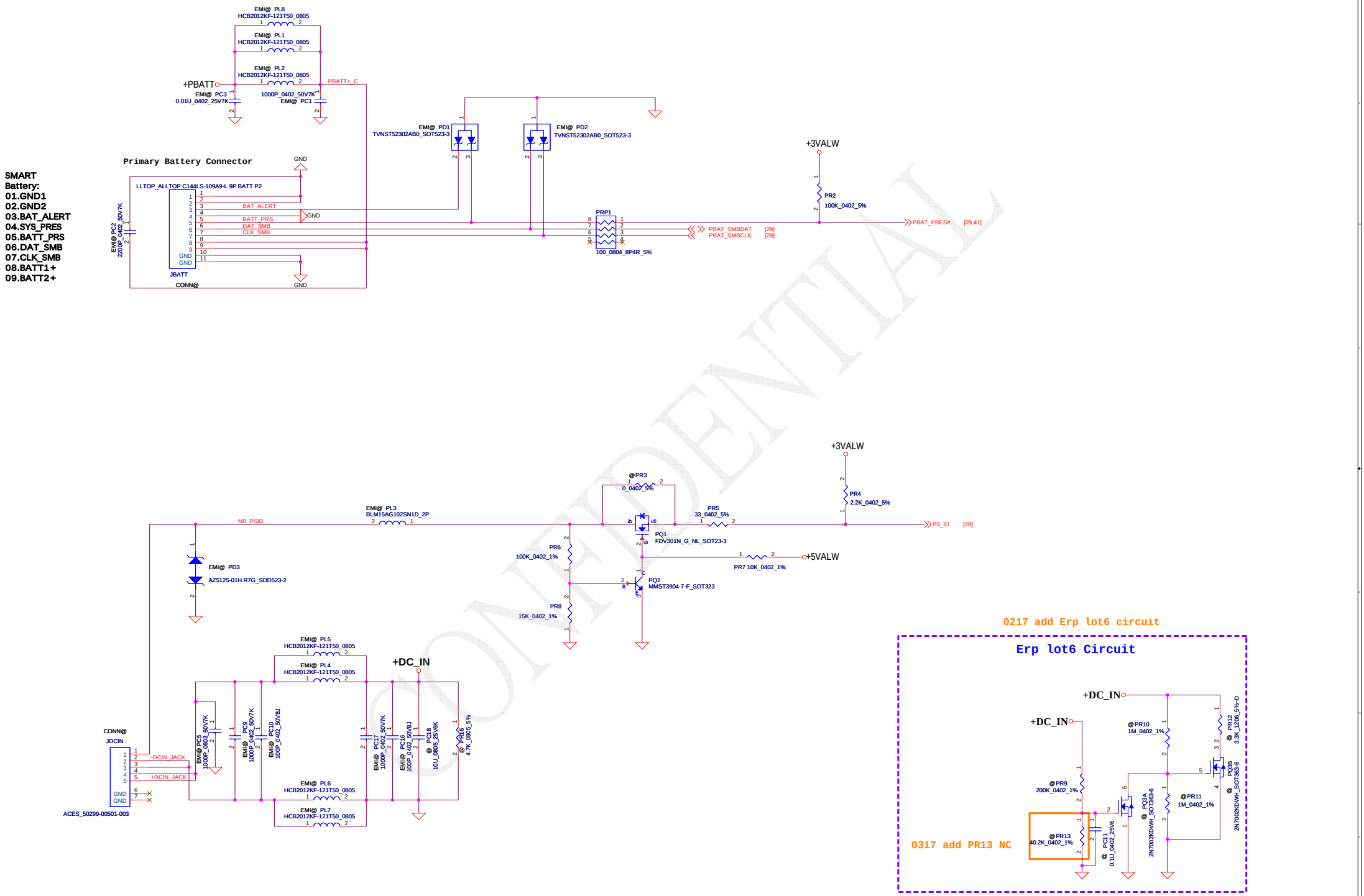

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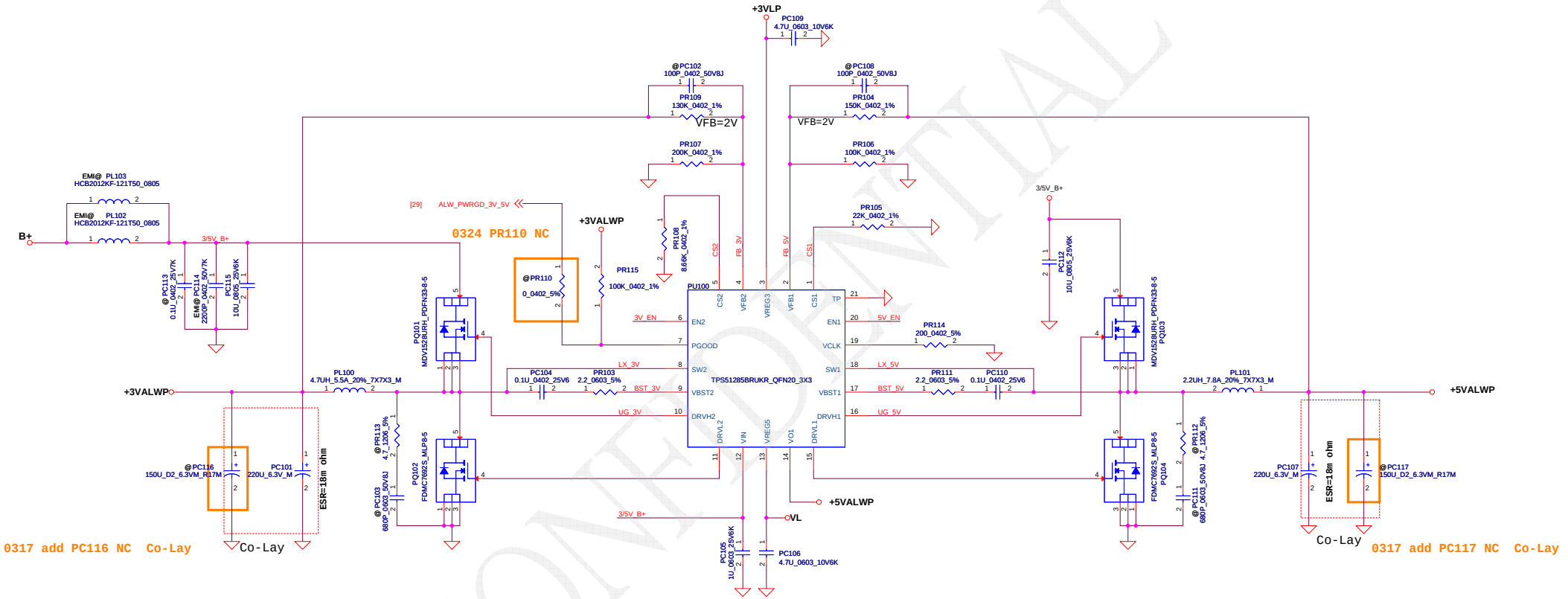
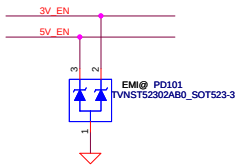
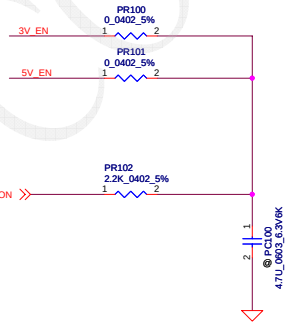


3VALWP
TDC 2.76A
Peak Current 3.95A
OCP current 4.6A

	TYP	MAX
H/S Rds(on):	23.2mohm ,	27.8mohm
L/S Rds(on):	10.8mohm ,	13.6mohm



Place PD101 close to PU100



5VALWP
TDC 6.86A
Peak Current 9.8A
OCP current 11.43A

	TYP	MAX
H/S Rds(on):	23.2mohm ,	27.8mohm
L/S Rds(on):	10.8mohm ,	13.6mohm

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[0823] change DP to VGA solution, delet this design

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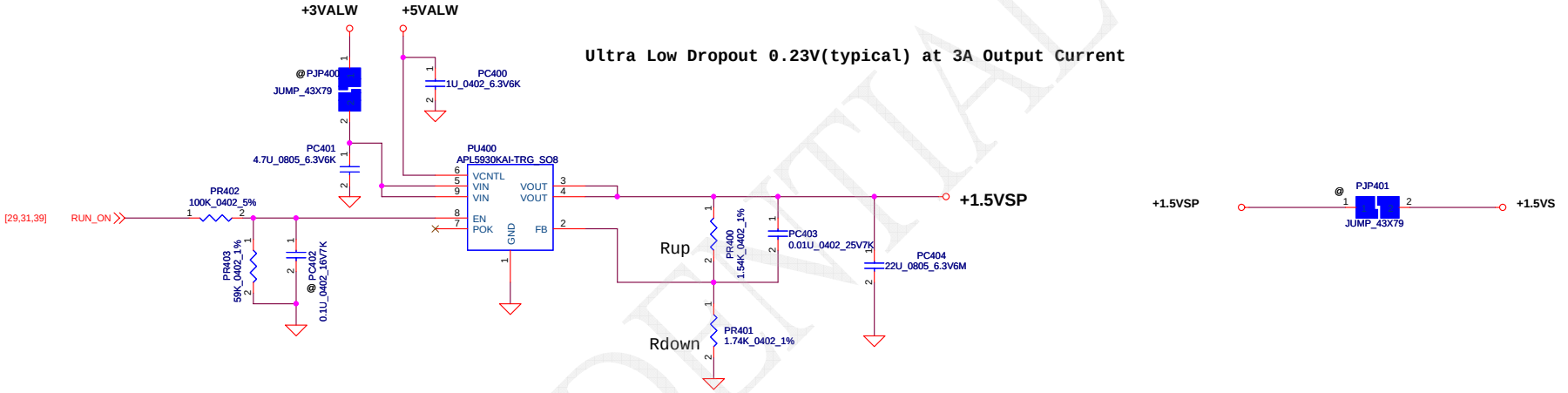
Module model information

APL5930_V1.mdd



1.5VS
TDC 0.014A
Peak Current 0.2A
OCP current 5.7A

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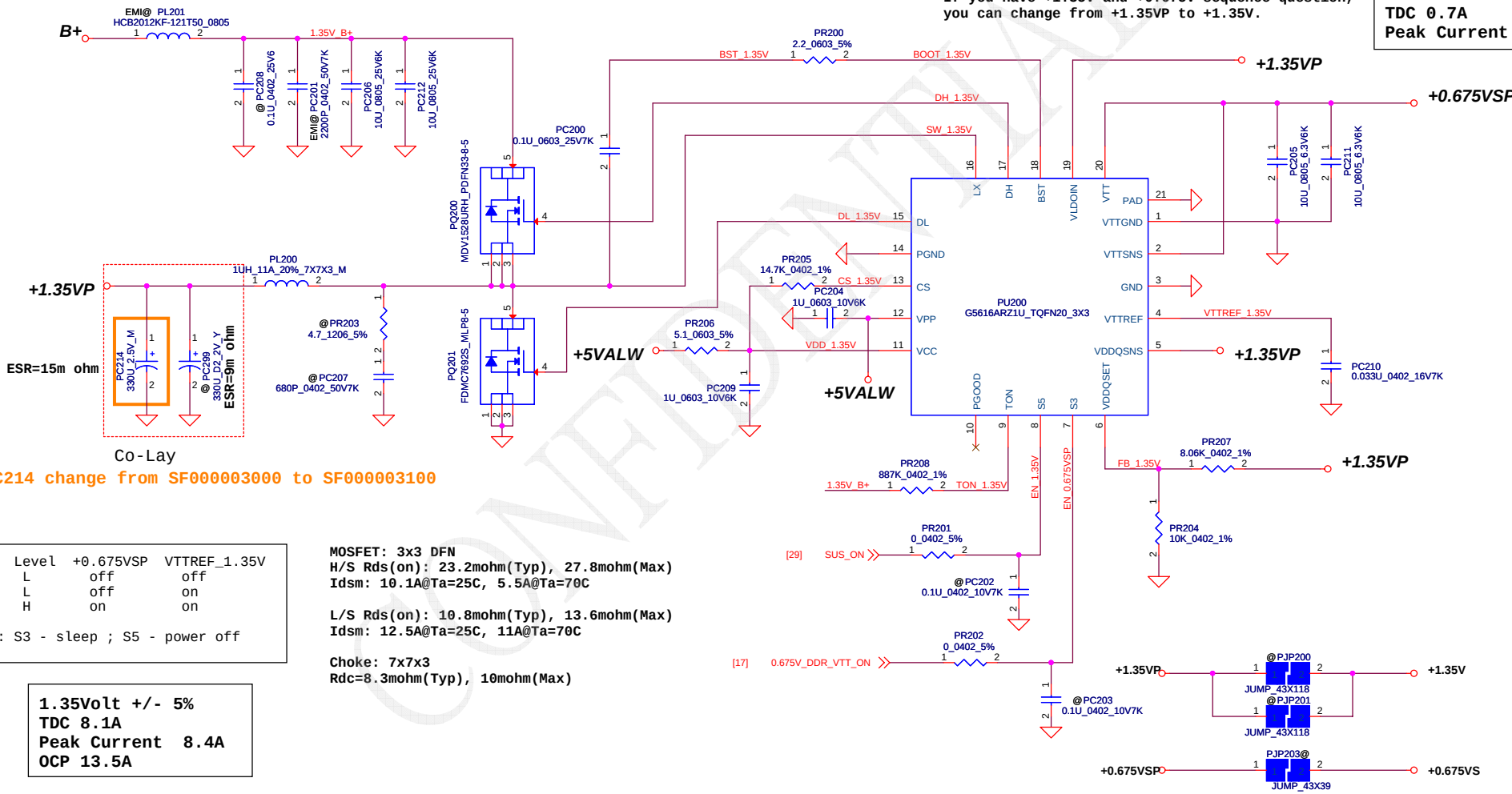
Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35V.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



Co-Lay

0314 PC214 change from SF000003000 to SF000003100

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

1.35Volt +/- 5%
TDC 8.1A
Peak Current 8.4A
OCP 13.5A

MOSFET: 3x3 DFN
H/S Rds(on): 23.2mohm(Typ), 27.8mohm(Max)
Idsm: 10.1A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 10.8mohm(Typ), 13.6mohm(Max)
Idsm: 12.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

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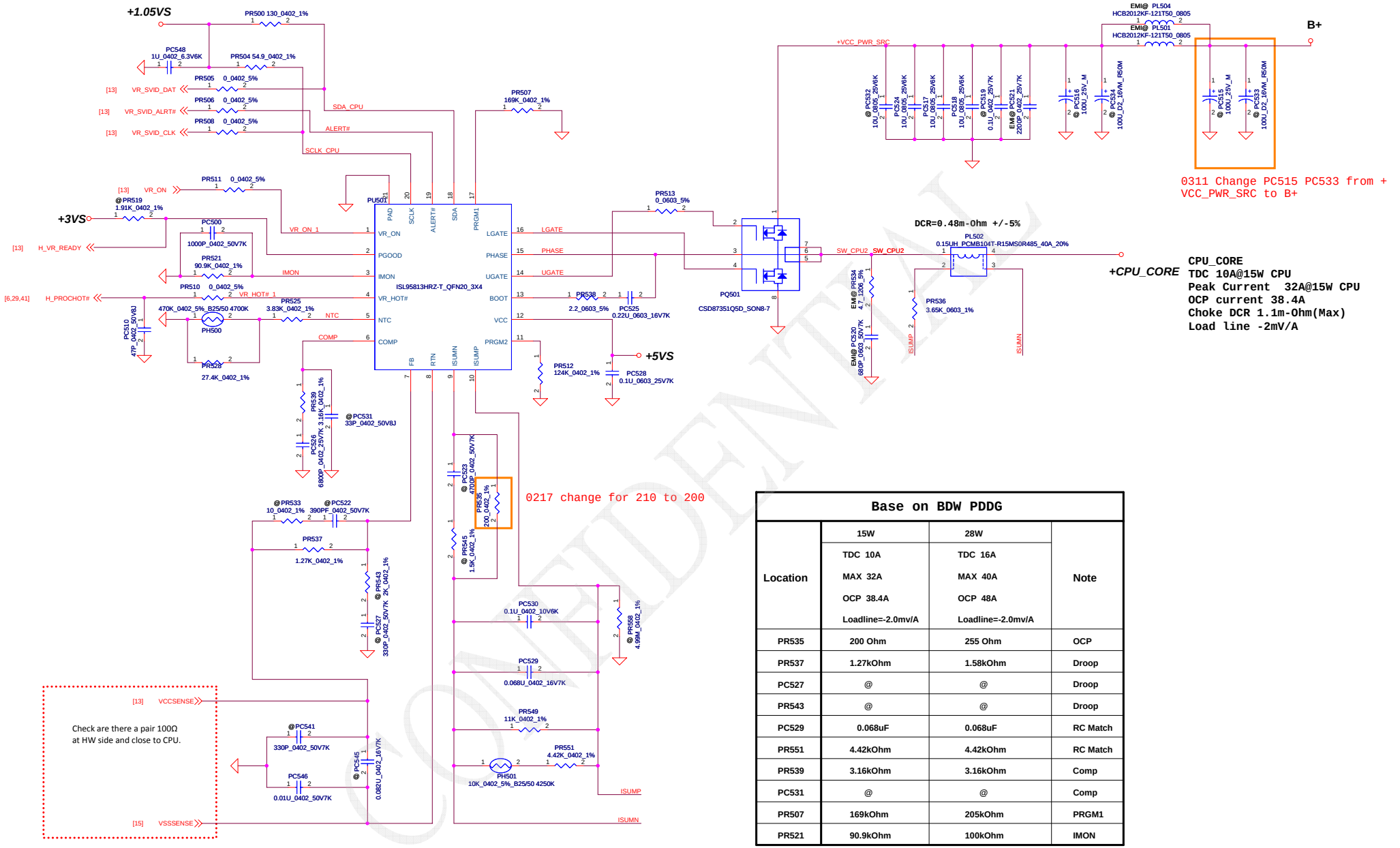

Base on BDW PDDG

Location	15W	28W	Note
	TDC 10A MAX 32A OCP 38.4A Loadline=-2.0mv/A	TDC 16A MAX 40A OCP 48A Loadline=-2.0mv/A	
PR535	200 Ohm	255 Ohm	OCP
PR537	1.27kOhm	1.58kOhm	Droop
PC527	@	@	Droop
PR543	@	@	Droop
PC529	0.068uF	0.068uF	RC Match
PR551	4.42kOhm	4.42kOhm	RC Match
PR539	3.16kOhm	3.16kOhm	Comp
PC531	@	@	Comp
PR507	169kOhm	205kOhm	PRGM1
PR521	90.9kOhm	100kOhm	IMON

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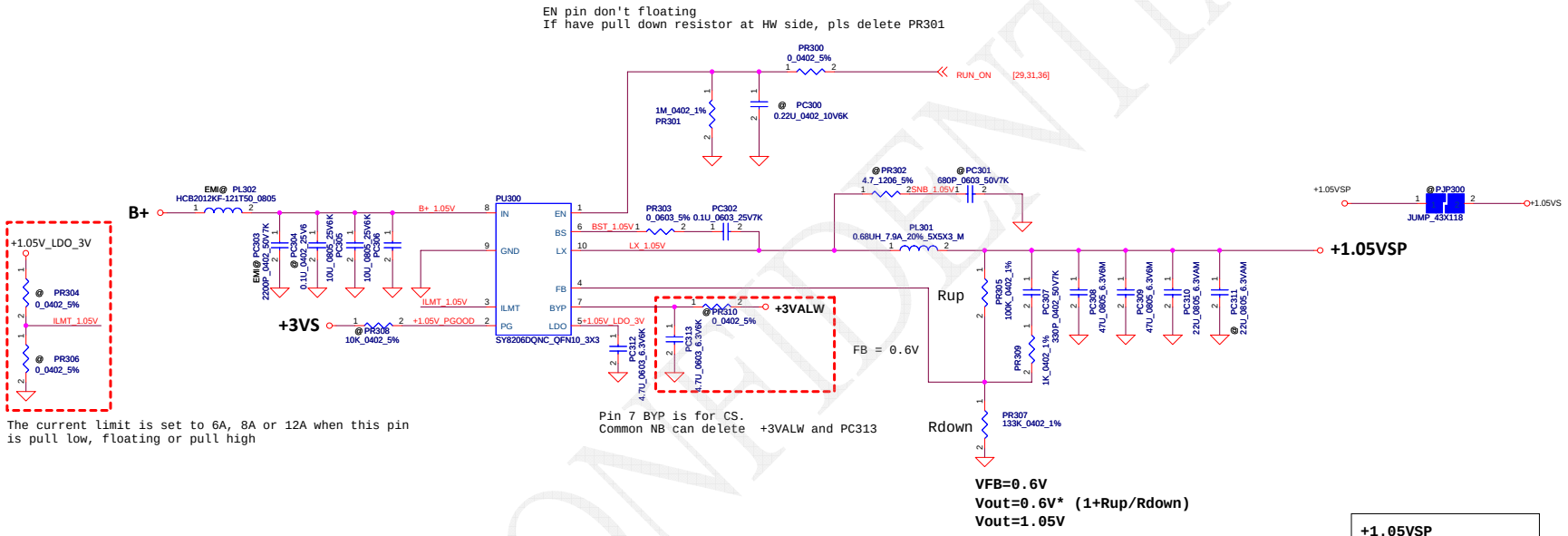

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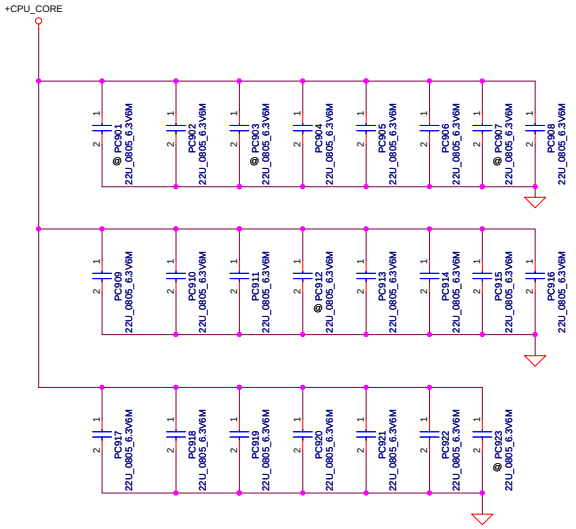
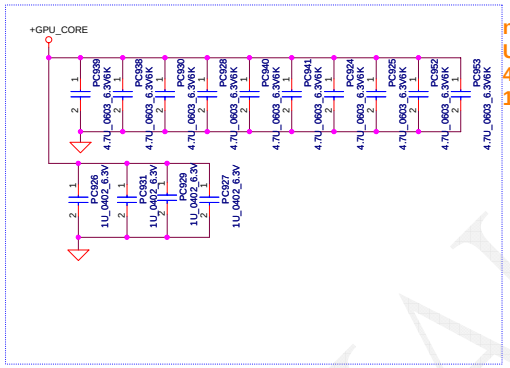
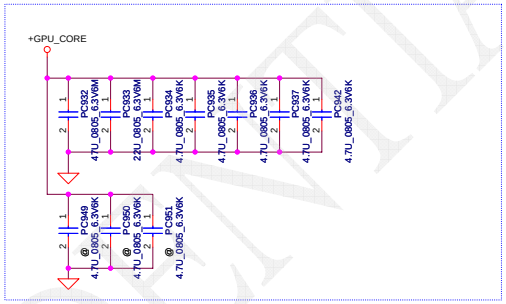




nVidia GB2B-64 package
Under GPU
4.7uF 0603 * 10
1uF 0402 * 4



nVidia GB2B-64 package
Near GPU
47uF 0805 *1
22uF 0805 *1
4.7uF 0805 *5

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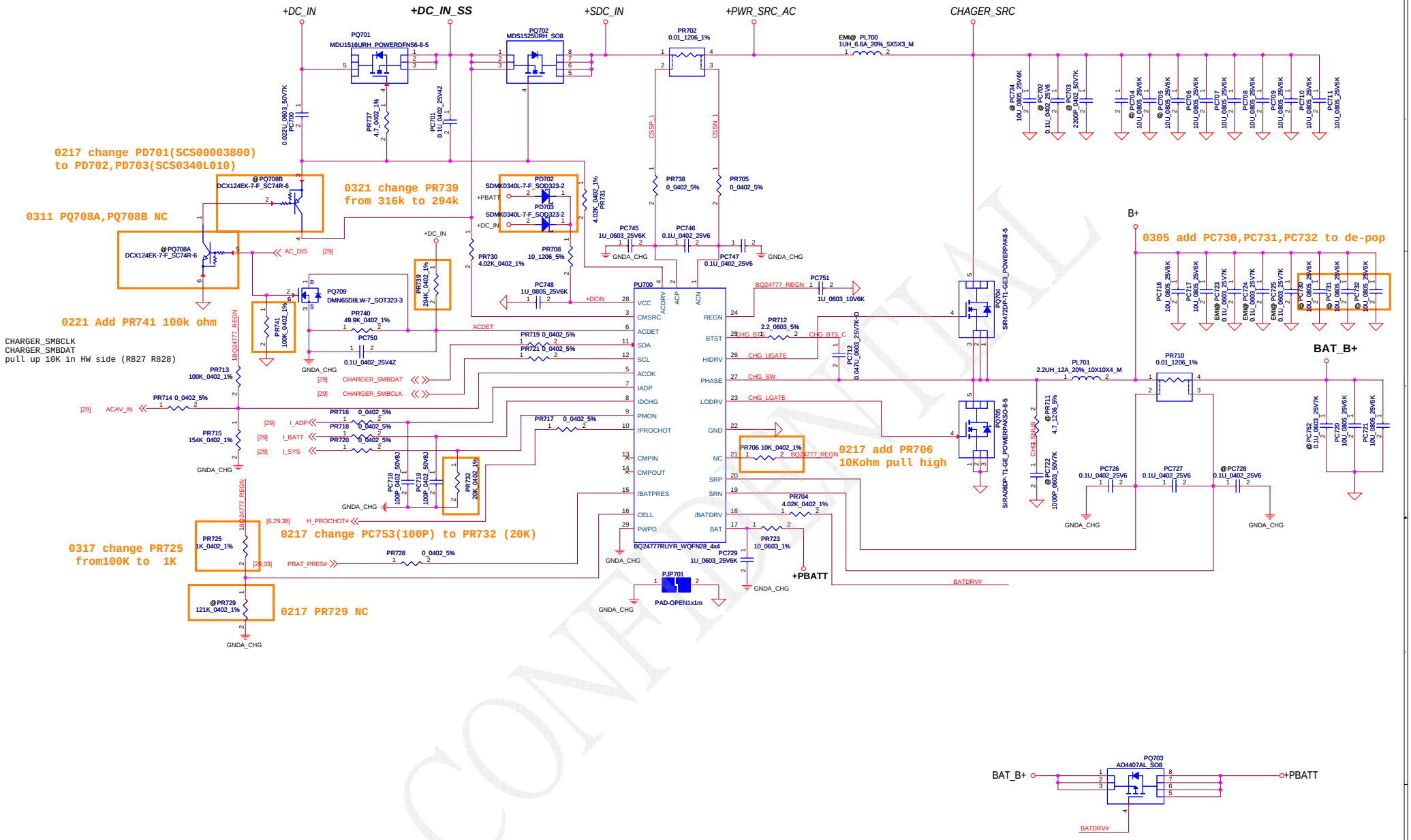

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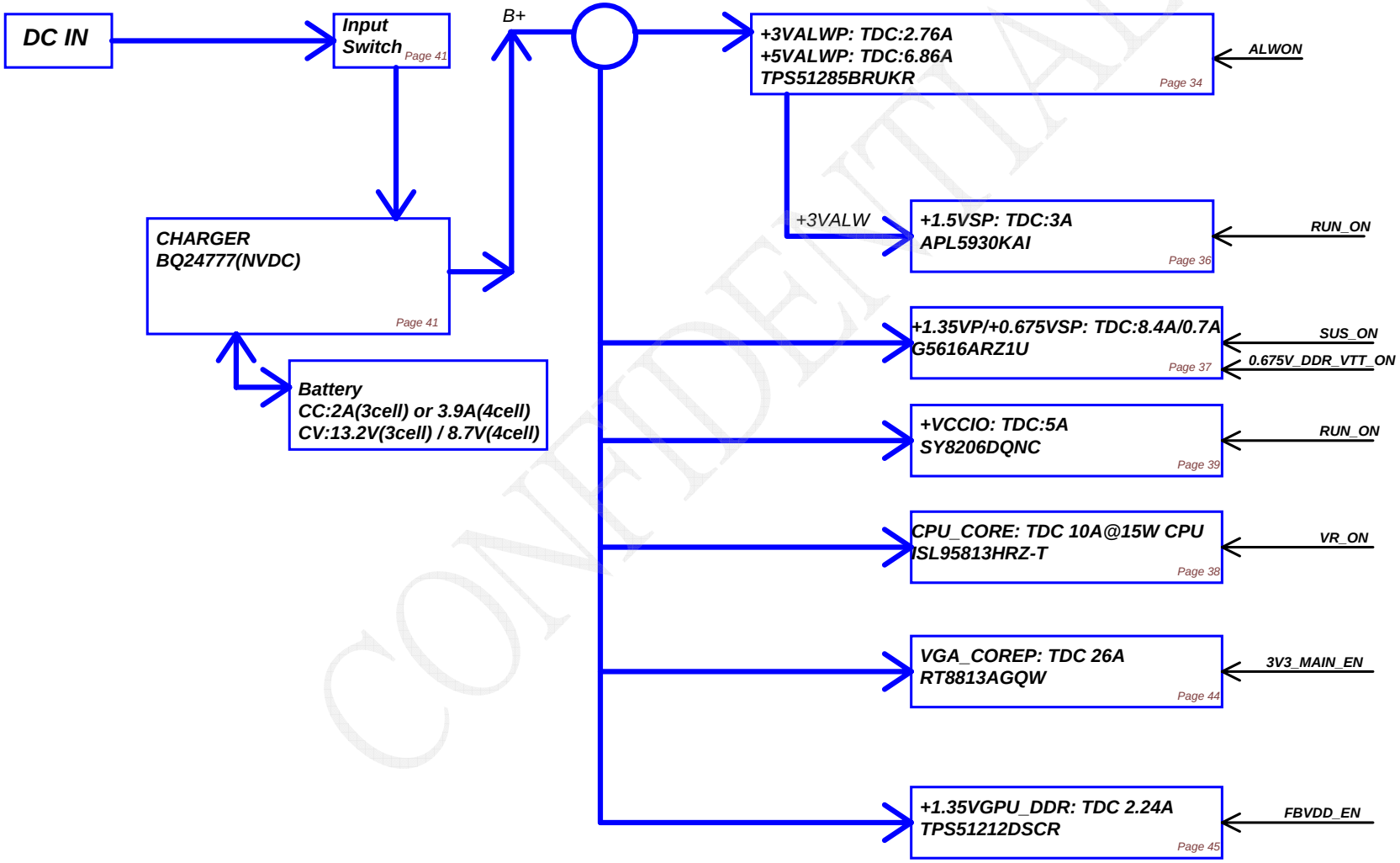
Power block



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Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

PWM-VID Spec and component Values

PWM-VID Spec		Config A	Config B	Config C
Vmin		0.6V	0.6V	0.65V
Vmax		1.2V	1.2V	1.15V
Vboot		0.875V	0.9V	0.9V
Voltage step		6.25mV	6.25mV	25mV
N of Voltage level		96	96	20
Rrefadj	PR604	39K	20K	39K
Rref1	PR602	39K	20K	30K
Rboot	PR603	1.5K	2K	3K
Rref2=PR607+PR610	PR607	30K	18K	24K
	PR610	1.5K	0	3K
C	PC607	1.5nf	2.7nf	1.8nf

H-side MOS:MDU1516URH
Rds(on):
11.7mohm@Vgs=4.5V
Id :18.6A@Ta=25 degC

L-side MOS:MDU1511RH
Rds(on):
2.7mohm@Vgs=4.5V
Id :36.1A@Ta=25 degC

Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N15S-GM
OpenVReg Configurations	Config B
Rated TDP Power at Tj=102C	18W
Boosted GPU Total at Tj=102C	20W
EDP-Continuous at Tj=102C	22A
EDP-Peak at Tj=102C	48.11 A
Istep max (Evaluation)	29.22 A
OCP Setting Current	66A
Rocset	13K
Recommendation	2phase 1H1L
Polymer Cap (330uF)	9mohm * 3
Or OSCON (390uF)	NULL

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

PSI Pull high on HW side

Pull high on HW side

Reserve Location

0217 PC604 change from pop to de-pop
PC627 change from de-pop to pop

+VGA_CORE
EDP-Continuous 22A
EDP-Peak 48.11A
OCP min 66A

1. VSNS Soft-Start time (Internal) is 0.7ms (PC616 un-pop)
Tss=(Css*Vrefin)/Iss+2.3ms
=0.01U*0.9V/5uA+2.3ms=4.1ms (PC616 pop)

2. Switching frequency setting:
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=304.89Khz

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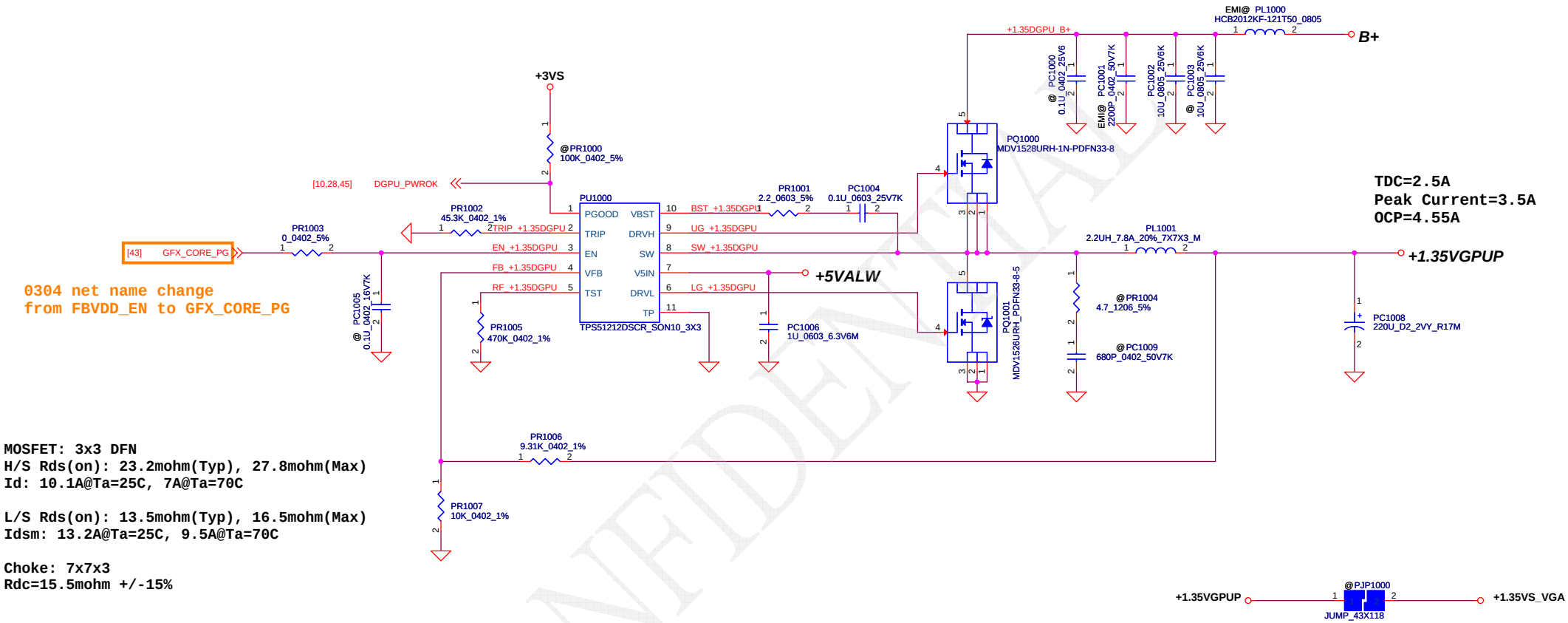

0304 net name change
from FBVDD_EN to GFX_CORE_PG

TDC=2.5A
Peak Current=3.5A
OCP=4.55A

MOSFET: 3x3 DFN
H/S Rds(on): 23.2mohm(Typ), 27.8mohm(Max)
Id: 10.1A@Ta=25C, 7A@Ta=70C

L/S Rds(on): 13.5mohm(Typ), 16.5mohm(Max)
Idsm: 13.2A@Ta=25C, 9.5A@Ta=70C

Choke: 7x7x3
Rdc=15.5mohm +/-15%

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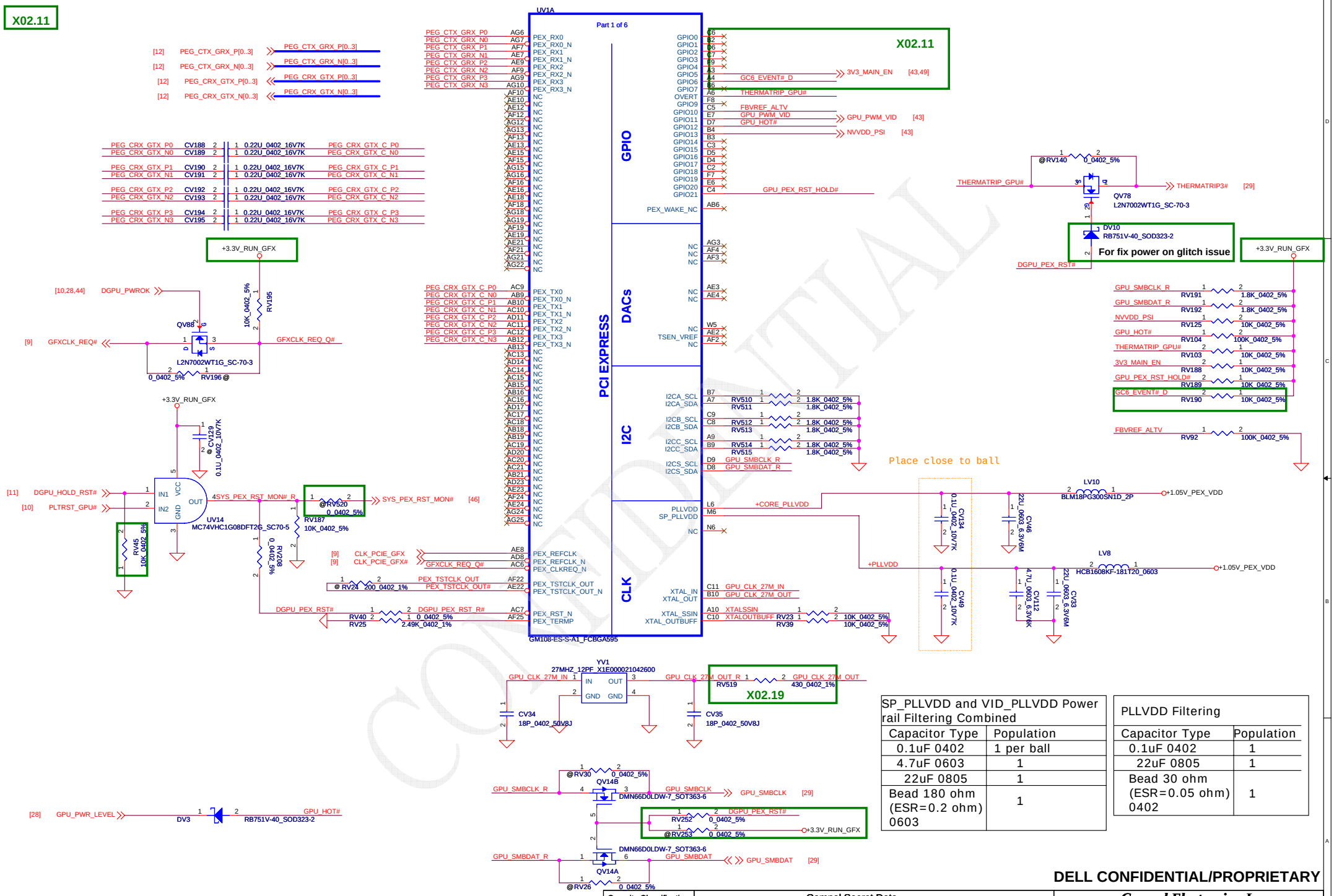

SP_PLLVDD and VID_PLLVDD Power rail Filtering Combined	
Capacitor Type	Population
0.1uF 0402	1 per ball
4.7uF 0603	1
22uF 0805	1
Bead 180 ohm (ESR=0.2 ohm) 0603	1

PLLVDD Filtering	
Capacitor Type	Population
0.1uF 0402	1
22uF 0805	1
Bead 30 ohm (ESR=0.05 ohm) 0402	1

GPU_PWR_LEVEL	
LOW	Low Performace
HIGH	High Performace

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X02.11

I2CS Slave Address

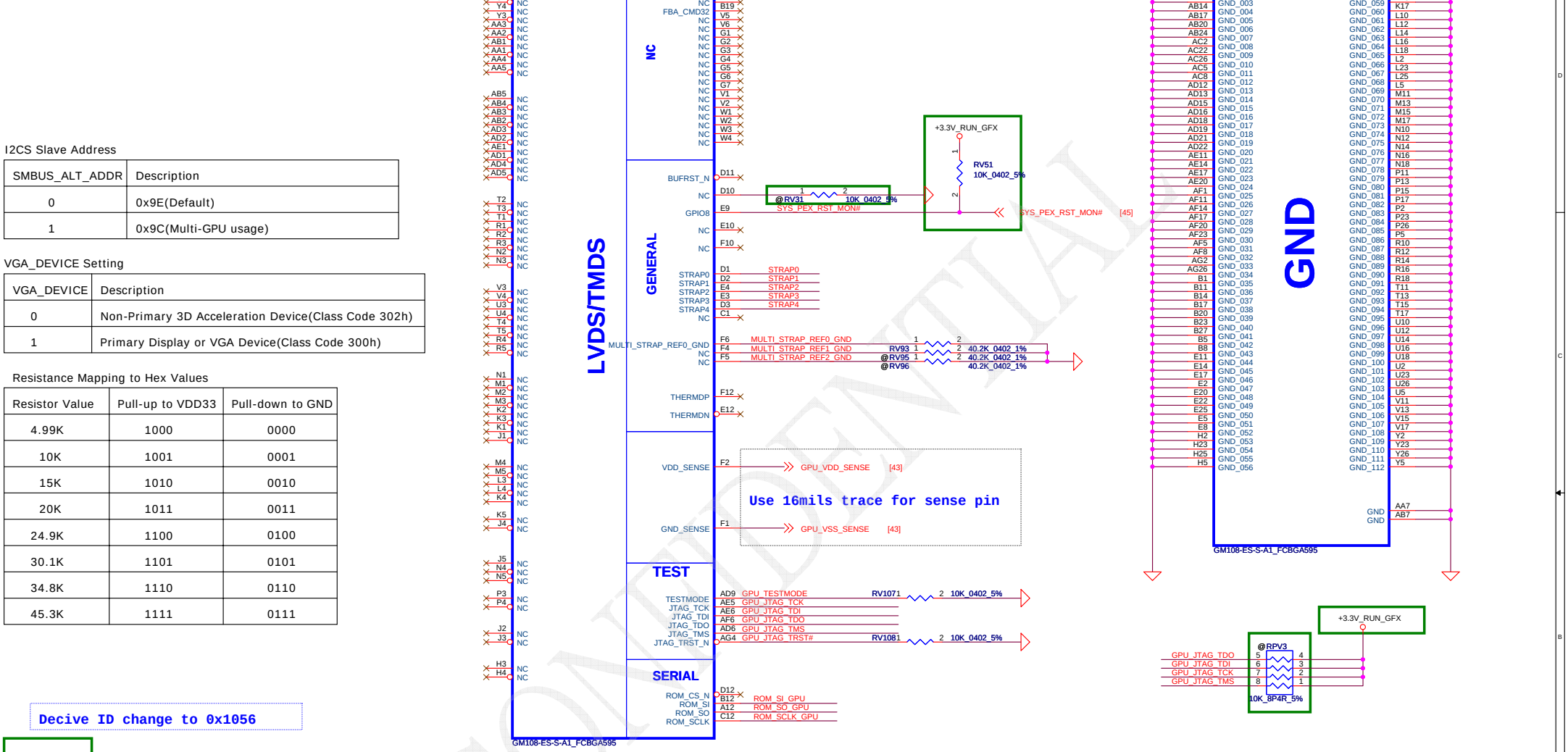
SMBUS_ALT_ADDR	Description
0	0x9E(Default)
1	0x9C(Multi-GPU usage)

VGA_DEVICE Setting

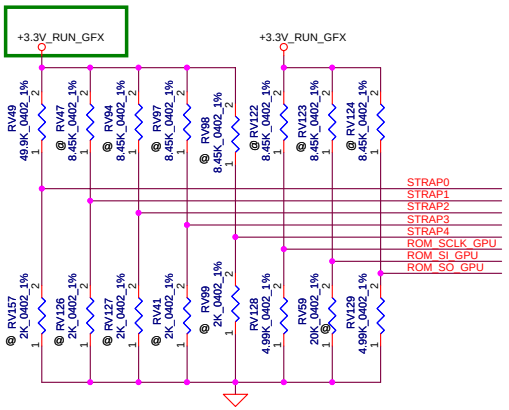
VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device(Class Code 302h)
1	Primary Display or VGA Device(Class Code 300h)

Resistance Mapping to Hex Values

Resistor Value	Pull-up to VDD33	Pull-down to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111



Decive ID change to 0x1056



Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0	Note
ROM_SCLK	SOR3_EXPOSED->0	SOR2_EXPOSED->0	SOR1_EXPOSED->0	SOR0_EXPOSED->0	ROM_SCLK pull-down 4.99k to GND
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	ROM_SI pull-down 20k to GND
ROM_SO	DEVID_SEL->0(default)	PCIE_CFG->0(defual)	SMB_ALT_ADDR->0(default)	VGA_DEVICE->0	ROM_SO pull-down 4.99k to GND
STRAP0	Keep pull up to 3V3_AON and pull-down to GND footprint and stuff 50k ohm pull up				STRAP0 pull up 50k to +3.3V_GFX_AON
STRAP1 STRAP2 STRAP3 STRAP4	Reserve				

DEVID_SEL/PCIE_CFG defaul set 0, need refer Platform Update Notification for the latest configuration

VENDER	STRAP	Part Number	Note(ROM_SI)
Hynix	0x3	H5TC4G63AFR-11C	20k PD
Micron	0x4	MT41J256M16HA-093G:E	24.9k PD
Samsung	0x5	K4W4G1646D-BC1A	30.1k PD

Base on RVL RVL-06891-001_v03_secured.pdf

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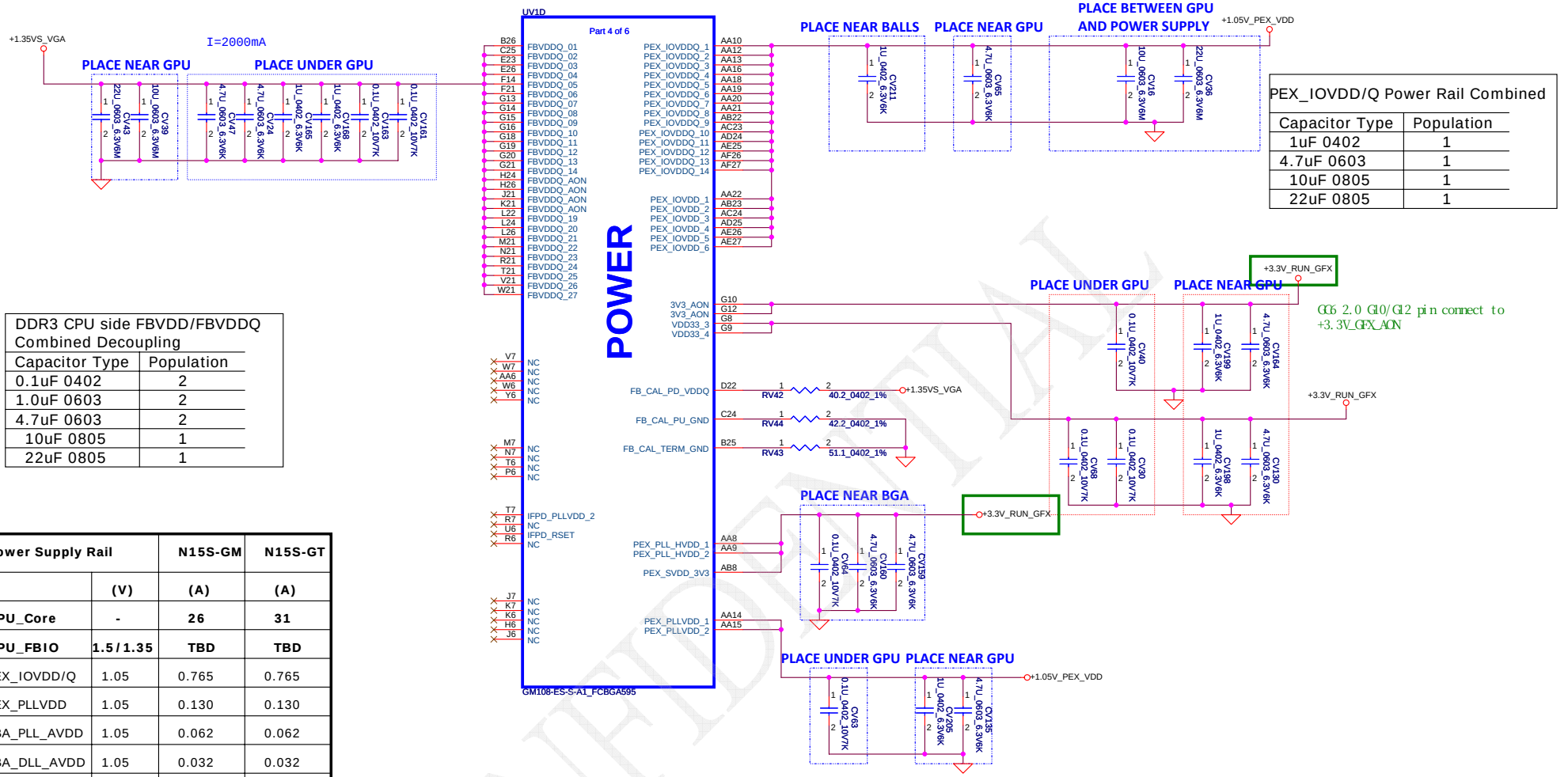

DDR3 CPU side FBVDD/FBVDDQ Combined Decoupling	
Capacitor Type	Population
0.1uF 0402	2
1.0uF 0603	2
4.7uF 0603	2
10uF 0805	1
22uF 0805	1

PEX_IOVDD/Q Power Rail Combined	
Capacitor Type	Population
1uF 0402	1
4.7uF 0603	1
10uF 0805	1
22uF 0805	1

Power Supply Rail		N15S-GM	N15S-GT
	(V)	(A)	(A)
GPU_Core	-	**26**	**31**
GPU_FBIO	**1.5/1.35**	**TBD**	**TBD**
PEX_IOVDD/Q	1.05	0.765	0.765
PEX_PLLVDD	1.05	0.130	0.130
FBA_PLL_AVDD	1.05	0.062	0.062
FBA_DLL_AVDD	1.05	0.032	0.032
PLL_VDD	1.05	0.058	0.058
SP_PLLVDD	1.05	0.030	0.030
1.05V Total	**1.05**	**1.060**	**1.060**
VDD33+3V3AON	3.3	0.036	0.036
PEX_SVDD_3V3	3.3	0.167	0.167
PEX_PLL_HVDD	3.3	0.022	0.022
3.3V Total	**3.3**	**0.225**	**0.025**

PEX_PLLVDD Decoupling	
Capacitor Type	Population
0.1uF 0402	1
1uF 0603	1
4.7uF 0805	1

PEX_SVDD/PEX_PLL_HVDD Decoupling	
Capacitor Type	Population
0.1uF 0402	1
4.7uF 0603	2

3V3_MAIN Decoupling	
Capacitor Type	Population
0.1uF 0402	2
1uF 0603	1
4.7uF 0603	1

3V3_AON Decoupling	
Capacitor Type	Population
0.1uF 0402	1
1uF 0603	1
4.7uF 0603	1

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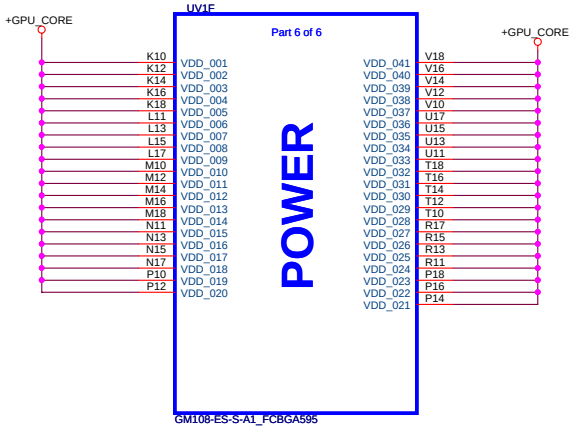
X02.11

Caps on Power Side
1UX4 4.7UX10 under GPU
4.7UX5 22UX1 47UX2 330UX2 near GPU



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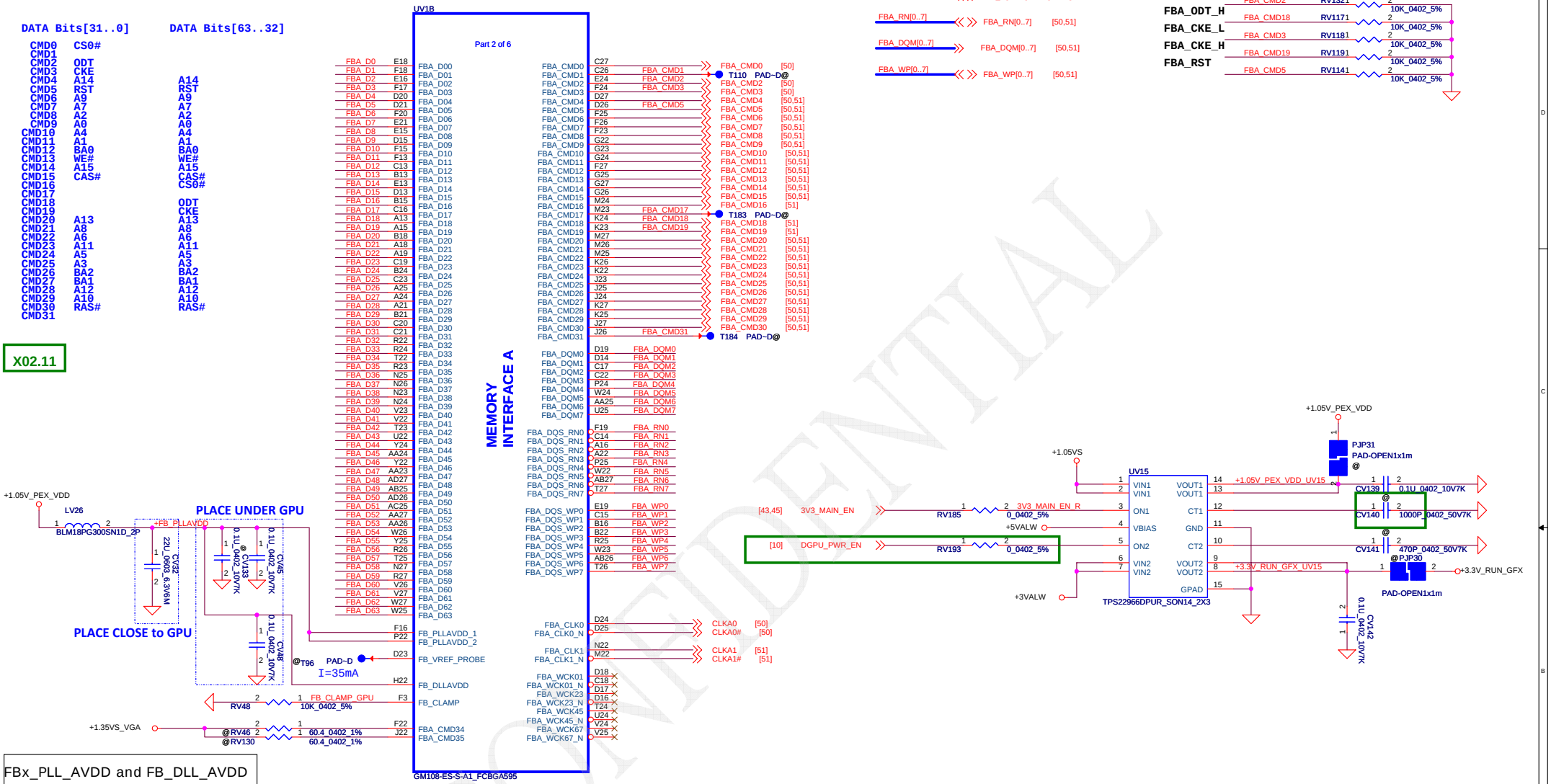
GDDR3L CMD Mapping Table

DATA Bits[31..0]	DATA Bits[63..32]
CMD0 CS0#	
CMD1	
CMD2 ODT	
CMD3 CKE	
CMD4 A14	A14
CMD5 RST	RST
CMD6 A9	A9
CMD7 A7	A7
CMD8 A2	A2
CMD9 A0	A0
CMD10 A4	A4
CMD11 A1	A1
CMD12 BA0	BA0
CMD13 WE#	WE#
CMD14 A15	A15
CMD15 CAS#	CAS#
CMD16	CS0#
CMD17	
CMD18	ODT
CMD19	CKE
CMD20 A13	A13
CMD21 A8	A8
CMD22 A6	A6
CMD23 A11	A11
CMD24 A5	A5
CMD25 A3	A3
CMD26 BA2	BA2
CMD27 BA1	BA1
CMD28 A12	A12
CMD29 A10	A10
CMD30 RAS#	RAS#
CMD31	

X02.11



FBx_PLL_AVDD and FB_DLL_AVDD Combined	
Capacitor Type	Population
0.1uF 0402	2
22uF 0805	1
Bead 30 ohm (ESR=0.01 ohm) 0603	1

Security Classification	Compal Secret Data		
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Memory Partition A - Upper 16 bits

256x16 DDR3L

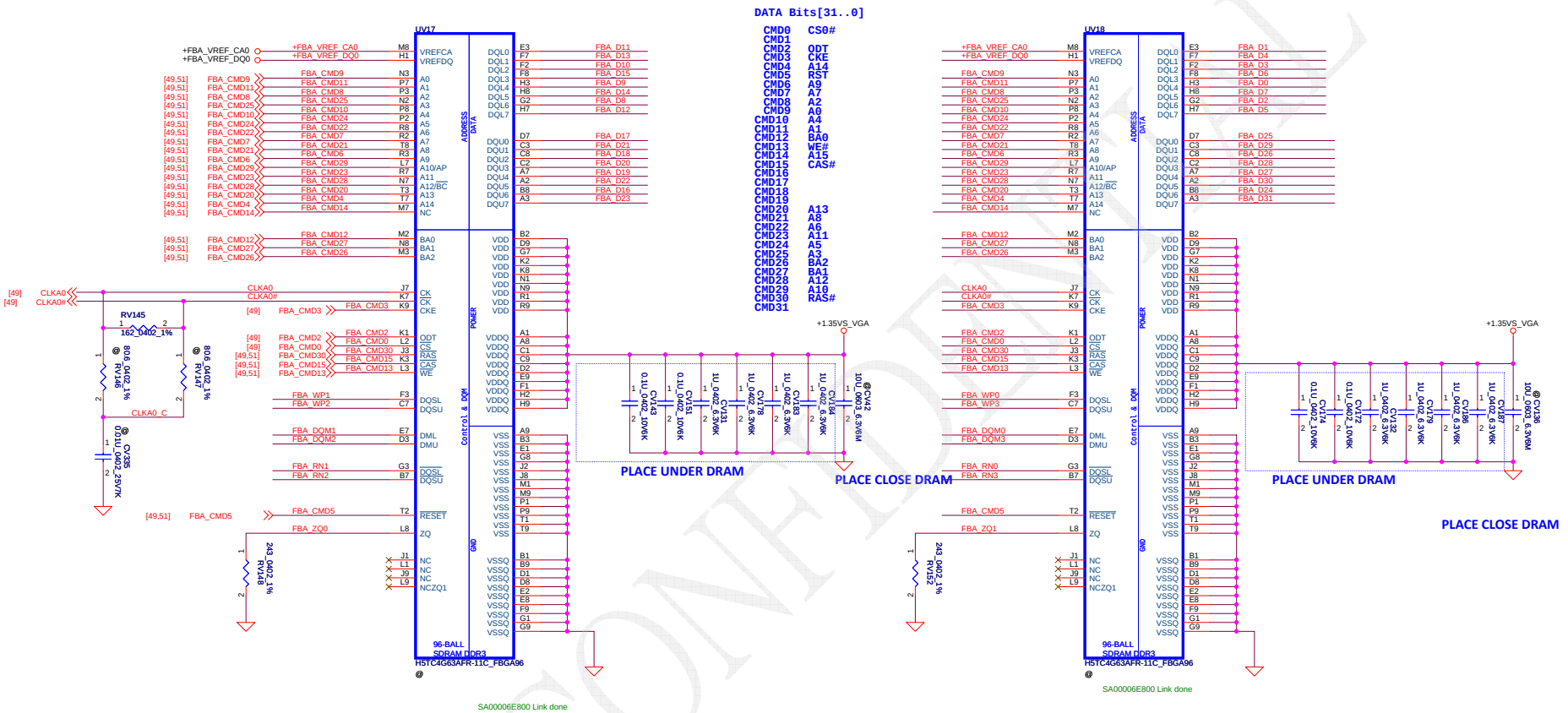
FBA_D[0..31] <<>> FBA_D[0..31] [49]

FBA_WP[0..3] <<>> FBA_WP[0..3] [49]

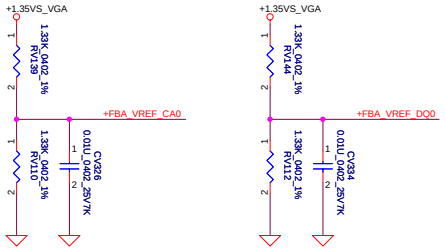
FBA_DQM[0..3] <<>> FBA_DQM[0..3] [49]

FBA_RN[0..3] <<>> FBA_RN[0..3] [49]

X02.11



DDR3 per Memory FBVDD/Q Decoupling	
FBVDD/Q Combined	
Capacitor Type	Population
0.1uF 0402	2
1.0uF 0603	4
10uF 0805	0



Security Classification	Compal Secret Data		
Issued Date	2013/07/25	Deciphered Date	2014/07/24

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Memory Partition A - Lower 16 bits

256x16 DDR3L

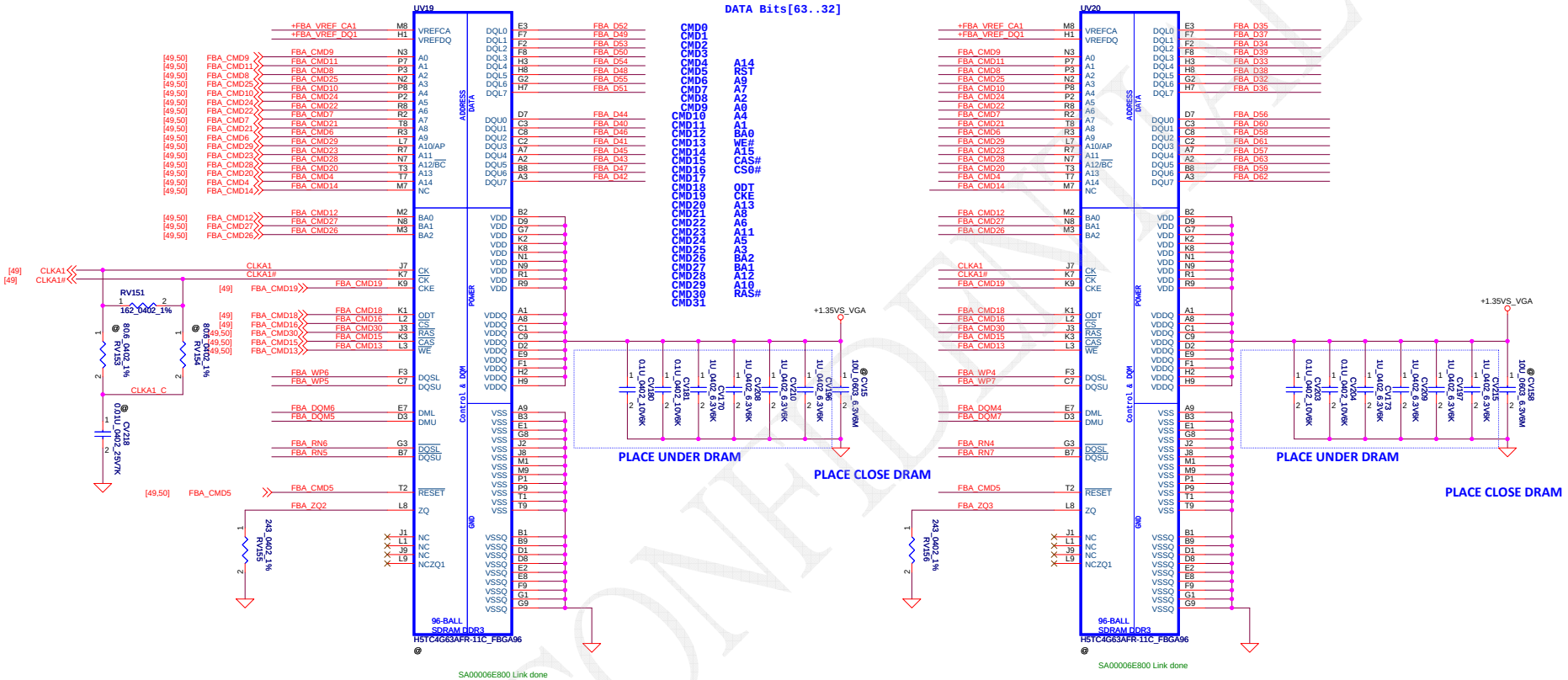
FBA_D[32..63] <<>> FBA_D[32..63] [49]

FBA_WP[4..7] <<>> FBA_WP[4..7] [49]

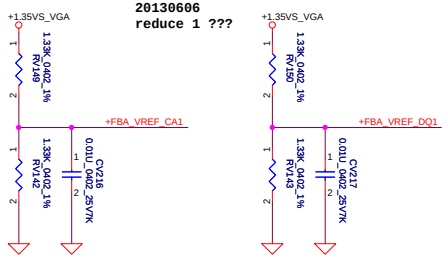
FBA_DQM[4..7] <<>> FBA_DQM[4..7] [49]

FBA_RN[4..7] <<>> FBA_RN[4..7] [49]

X02.11



20130606
reduce 1 ???



Security Classification	Compal Secret Data		
Issued Date	2013/07/25	Deciphered Date	2014/07/24

Compal Electronics, Inc.

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Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	31	KB control	2013/10/21	EE	Change Fuse package for sales suggestion	Change F1 From SP040003E00 to SP040003A00	X01
2	23	Audio Codec ALC3234	2013/10/21	EE	fix POP noise issue	Add RA1129 from 100K to UA1 pin 27, and NC RC366	X01
3	ALL	ALL	2013/10/21	EE	Re-name part of connector	JCRT1 --> JCRT, JAPS1 --> JAPS, JDEG1 --> JDEG, JLPDE1 --> JLPDE, JKB1 --> JKB, JNGFF1 --> JNGFF JXDP1 --> JXDP, JRTC1 --> JRTC, PJPDC1 --> JDCIN, PBATT1 --> JBATT	X01
4	ALL	ALL	2013/10/21	EE	Re-name part of jump	PJ200 --> PJP200, PJ201 --> PJP201, PJ203 --> PJP203, PJ400 --> PJP400, PJ401 --> PJP401, JP12 --> PJP12 JP13 --> PJP13, J510 --> PJP510, J511 --> PJP511, J512 --> PJP512, J513 --> PJP513, PJ1000 --> PJP1000	
5	23	Audio Codec ALC3234	2013/10/23	EE	Update P/N for X1 code issue	Change LA8, LA9 form SM010018110 to SM01000EI00	
6	1	Cover page	2013/10/28	EE	Add Micron sku for X76 level	Add UV17, UV18, UV19, UV20 for SA000077K0L, RV59 for 24.9K	X01
7	27	LED/DB	2013/10/29	EE	delete circuit for EC control LED blink issue	Delete Q2417	
8	29	KBC & GPIO MEC5085	2013/10/31	EE	Depop item by EC request	Depop RE278	
9	22	LAN RTL8111GUS-CG	2013/10/31	EE	Change Power switch for cost down plan	Change UL2 from SA00003AR00 to SA000079400, Delete CL38, Add RL41	X01
10	21	eDP/webcam/touch	2013/10/31	EE	Change Power switch for cost down plan	Change UX1, UX3 from SA00003AR00 to SA000079400, Delete CX9, CX52, Add RX30, RX31 to 100K	X01
11	31	DC/DC interface	2013/10/31	EE	Change Load switch for cost down plan	Change U2301, U2304 from SA00004MM00 to SA00006FD00	X01
12	50	N15S-MEM Interface A	2013/10/31	EE	Change Load switch for cost down plan	Change UV15 from SA00004MM00 to SA00006FD00	X01
13	25	NGFF_WLAN	2013/10/31	EE	Change Power switch for cost down plan	Change UM1 from SA00005XM00 to SA000070L00, Add CM8 to 2200P	X01
14	22	LAN RTL8111GUS-CG	2013/10/31	EE	Change Transformer for cost down plan	Change TL2 from SP050007Q00 to SP050006P00	X01
15	20	DP to CRT	2013/11/05	EE	Add cap for reduce power ripple by vendor confirm	Add CV361 to 22uF and close UV6 pin 38	X01
16	23	Audio Codec ALC3234	2013/11/05	EE	Add capacitor for codec stable	Add CA77 to 4.7uF_0603 and close UA1 pin36	
17	19,24, 26,27	Common mode Choke	2013/11/12	EE	Change Common mode choke for X1 code	Change L12,LX2,LI2,LX3,LX4,LX5,LI5,LX6,LX7,LI9,LI10 from SM070001S00 to SM070003Y00 Change LI1, LI3, LI4, LI6 from SM070001R00 to SM070003Q00	X01
18	27	LED/DB	2013/11/12	EE	Delete MB common mode choke by EA measure	Delete LI9, LI10	X01
19	46	N15S-PCIE	2013/11/13	EE	change bead for X1 code	Change LV8 from SM010028480 to SM010004700	X01
20	24, 27	USB	2013/11/13	EE	Change USB I/O power switch for Cost down	Change UI2, UI3, UI4 from SA00003XM00 to SA00007AO00, Delete CI7, CI14, CI18, CI45, Change CI6, CI12, CI44 from 4.7U_0805 to 1U_0603	
21	13, 17	Buffer output	2013/11/13	EE	change buffer output for cost down	Change UC6, U2303 from SA00005U600 to SA00007KJ00	X01
22	46	N15S-PCIE	2013/11/14	EE	change AND gate for cost down	Change UV14 from SA007080120 to SA00000OH00	X01
23	17, 27, 30	DDR & LED & KB	2013/11/14	EE	change MOSFET for cost down	Change Q12, QE11, Q327 from SB00000UO00 to SB00000ST00, Change QD2 from SB501380050 to SB00000ST00	X01
24	23	Audio Codec ALC3234	2013/11/15	EE	modify by EMC request	Change RA1126, RA1127 to SM01000FG00, Change CA38, CA40 from 100p to 680p	X01
25	46, 50	N15S-PCIE	2013/11/15	EE	modify for GPU power sequence	Change RV45 from pull high to 45.3K pull down, Depop CV141, Change CV140 from 470P to 1000P	
26	23	Audio Codec ALC3234	2013/11/18	EE	Change EMI solution	Change RA1121, RA1122, RA1123, RA1124 from 0 ohm to SM01000NO00	X01
27	29	KBC & GPIO MEC5085	2013/11/18	EE	Add ESD diode by EMC request	Add DE2 for PECI_EC net	
28	26	HDD/Finger print	2013/11/19	EE	Rename Location	Re-name U2413 to DS1	
29	08, 29	Crystal	2013/11/20	EE	Crystal fine tune	Change CE53 from 22P to 27P	
30	20	DP to CRT	2013/11/21	EE	Add Power pin connect to power by vendor	Add RV518 10K to +3VS_VGA	
31	21	eDP/ HDD / PAD	2013/11/21	EE	change connector & PAD by ME	Change JEDP to SP010013I00, JHDD to SP02000TR00, H1, H2, H15, H24 update footprint	
32	23, 26	Audio & Finger	2013/11/21	EE	modify by EMC request	Change LA8, LA9 from SM010018110 to SM01000MJ00, Change RS39 from 0603 to 0402	
33	27	ESD	2013/11/21	EE	ESD BOM slim plan	Change DE1, DV5, DV6 to SCA00001L00,	
34	21	Camera	2013/11/21	EE	Camera voltage drop	Delete RX27, Add QX5 and Change +3VS to +3VALW	
35	23	Audio	2013/11/25	EE	Change ESD diode by EMC request	Change DA12 to SC400007Q00, Add DA14 to SC400007Q00	
36	46	N15S-PCIE	2013/11/26	EE	Add diode for prevent leakage	Add DV9 for GC6_EVENT#	
37	32	Screw Hole	2013/11/26	EE	Modify Screw hole by ME update DXF	Delete H13, H18, Add H24	
38	29	KBC & GPIO MEC5085	2013/11/27	EE	Change Connector for ME issue	Change JDEG from SP01001FP00 to SP01001L100, Change JLPDE from SP01001FP00 to SP01000HE00	
39	21	eDP	2013/11/27	EE	Add EMI solution for eDP	Add LX8, LX9, LX10, for SM070003Q00, Add RX32, RX33, RX34, RX35, RX36, RX37 for 0 ohm	
40	29	KBC & GPIO MEC5085	2013/11/27	EE	Change Resistor for Thermal request	Change RE77 from 1.58K to 1.96K	
41	46	N15S-PCIE	2013/11/28	EE	GPU circuit modify by vendor feedback	Add RV519 for GPU_CLK_27M_OUT, pop DV8, RV29, reserve RV208, Change power for ROM_SO_GPU/ROM_SI_GPU/ROM_SCLK_GPU	

Security Classification	Compal Secret Data		
Issued Date	2013/04/10	Deciphered Date	2014/05/01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
42	24	USB3.0	2013/11/28	EE	Rename by EC request	Delete RI1, connect UI2 to UE4 by USB_PWR_EN3#	X01
43	32	Screw Hole	2013/11/29	EE	Modify Screw hole by ME update DXF	Delete H16, Update H12 & H15	X01
44	23	Audio	2013/12/02	EE	Change EMC bead by EMC request	Change RA1126, RA1127 to LA10, LA11, P/N from SM01000FG00 to SM01000NA00, RC366 rename to RA1130	X01
45	19	HDMI	2013/12/02	EE	Update HDMI connector	Change JHDMI from DC232001500 to DC232001K00	X01
46	46	N15S-PCIE	2013/12/03	EE	fine tune crystal capacitor	Change CV34, CV35 from 10P to 18P	X01
47	22	LAN RTL8111GUS-CG	2013/12/03	EE	Change Wake on LAN fnction GPIO by EC request	Add R2532 for PCIE_WAKE# to LAN_WAKE#	X01
48	27	LED/DB	2013/12/04	EE	Change Tough PAD pin define for vendor request	Delete R2529, R2530, R2531 pull high, and change net CLK_TP_SIO/DAT_TP_SIO from pin1, pin2 to pin6, pin7	X01
49	26	HDD/Finger print	2013/12/04	EE	Update footprint by DFB request	Update JFP connector footprint	X01
50	27	LED/DB	2013/12/06	EE	Change Power button design for SMT issue	delete net from SW1 pin1 & pin4	X01
01	22	LAN	2014/02/10	EE	Update Jump name	Change JP3 to PJP3	X02
02	26	HDD	2014/02/10	EE	Update connector footprint for ME	Update JHDD connector	X02
03	08	RTC	2014/02/10	EE	Change crystal by Intel SPEC	Change YC1 from SJ100001K00 to SJ10000LT00	
04	27	LED	2014/02/10	EE	Change design by Dell request	Delete RZ24,Q12,RE21, change LED signal from SATA_ACT# to BREATH_LED#, SATA_ACT# connect to RP37	
05	25	NGFF	2014/02/11	EE	Update CIS symbol for pin define correct.	Change UM1 from SA000070L00 to SA000070S00	
06	21,27	MIC/Power Switch	2014/02/11	EE	Add ESD solution by EMC	Add DX4, DW1 for MIC_CLK/MIC_DATA, POWER_SW#_MB	
07	26	HDD	2014/02/25	EE	update circuit for 2nd source plan	Add RS40, RS41, RS42, RS43 for US2	
08	ALL	0 ohm to short pad	2014/02/25	EE	change footprint for 0 ohm cost down	Change RC43,RC44,RC45,RC46,RC57,RC59,RC126,RC37,RC40,RC41,RC42,RC47,RC55,RC78,RC81,RC97,RC107,R2355,R248,R250,R251,R257,R265,RV163,RV164,RV215,R2360,R2632,RM5,RM6,RS39,RE58,RE275,R416,R2451,RX32,RX33,RX34,RX35,RX36,RX37,RA1114,RA1115,RA1116,RA1117	
09	29	EC	2014/02/26	EE	Update EC Reversion resistor	Change RE79 from 130K to 62K	
10	23	AUDIO	2014/03/12	EE	Change footprint for cost down	Change CA23 from 0603 to 0402	
11	45-51	GPU	2014/03/04	EE	1. Update GPU circuit for GC6 feature change to pure Optimus function. 2. fine tune GPU power sequence	GC6 Function Changes: Delete DV8,RV29,DV9,DV8,RV29,DV9,QV86,CV363,RV181,QV87, Reserve RV520, Add RV51 pull high for SYS_PEX_RST_MON#. Use DGPU_PWR_EN to replace 3V3_MAIN_EN for +3V_RUN_GFX turn on time tuning. Delete DV4 and use GFX_CORE_PG to replace FBVDD_EN turn on +1.35VS_VGA. Change net name +3.3V_GFX_AON to +3.3V_RUN_GFX. Other Changes: Chang RV45 from 45K to 10K, De-pop RV31 as FAE recommend no use. Add DV10 solve DGPU_PEX_RST# turn on glitch issue. reserve CV140 for fine tune GPU turn on timing	
12	28	EC	2014/03/05	EE	Add CPU_ID for HSW & BDW sku by EC request	Add RE279,RE280 for CPU_ID pin	
13	08	ME	2014/03/05	EE	Change ME switch for layout placemant	Change SW3 from SN200003E00 to SN200002Y00	
14	21	eDP	2014/03/07	EE	Fine tune B+ range	Change RX2 from 100K to 270K, Change RX3 from 100K to 47K	
15	27	FAN	2014/03/10	EE	Add ESD by EMC request	Add DE3 on FAN1_TACH/FAN1_PWM	
16	22	LAN	2014/03/12	EE	Remove jump for layout placement	Delete PJP3	
17	20	CRT	2014/03/12	EE	Remove 0 ohm for EMC request	Delete RV211,RV212,RV213	
18	29	EC	2014/03/12	EE	Update crystal for measure result	Change YE1 from CL=12.5pF(SJ100001K00) to 9pF(SJ10000IA00)	
19	45	GPU	2014/03/12	EE	Update Resistor for measure result	Change RV519 form 0 ohm to 430 ohm	
20	20,24,26,27	ESD	2014/03/13	EE	Update ESD diode footprint for ME height limit	Change DI2,DI5,DS1,DE1,DV5,DV6,DE3 from SCA00001L00 to SCA00001100	
21	21	eDP	2014/03/14	EE	Change Capacitor for measure result	Change CX31 from 10V(SE102104K00) to 25V(SE00000G880), Change CV57 from Y5V(SE070104Z80) to X5R(SE00000G880)	
22	27	PWR Button	2014/03/17	EE	Change Footprint for layout require	Change SW1 footprint (the same P/N)	
23	13,17	MCP & DDR buffer	2014/03/18	EE	Change main source for IC issue	Change UC6, U2303 from SA00007KJ00 to SA00005U600	
24	29	Thermal	2014/03/18	EE	Reserve NGFF thermal sensor by Thermal team request	Reserve QE10	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P40	PROCESSOR DECOUPLING	2013/11/12	PWR	SSI verify , Vcore keep 18 keep	PC901,PC907,PC923,PC912,PC903 change from pop to de-pop	
2	P41	Charger_BQ24777	2013/11/12	PWR	EMI requirement	Pc723,PC724,PC725 change from de-pop to pop	
3	P33	DCIN/BATT CONN/OTP	2013/11/12	PWR	EMI requirement	**Add PL5/PL7(SM01000C000)**	
4	P33	DCIN/BATT CONN/OTP	2013/11/12	PWR	EMI requirement	**Add PL8(SM01000C000), PL1/PL2/PL5/PL6 change from SM010009C80 to SM01000C000 for finding 2nd source easily**	
5	P33	VCORE	2013/11/12	PWR	EMI requirement	**PL502 change from 0.22uH to 0.15uH**	
6	P38	VCORE	2013/11/12	PWR	Vcore test result abjustmet value	PR521 change from 97.6k to 95.3k	
7	P38	VCORE	2013/11/12	PWR	change to Vendor (CYNTEC)	PL502 change to SH00000PQ00	
8	P38	VCORE	2013/11/12	PWR	EMI requirement	**add PL504(SM01000C000)**	
9	P38	VCORE	2013/11/12	PWR	for common part	PL501 change from SM010009C80 to SM01000C000	
10	P34	3.3VALWP/5VALWP	2013/11/13	PWR	for common part	PL100 change from SH00000MS00 to SH00000YC00	
11	P37	+1.35VP/0.675VSP	2013/11/13	PWR	for common part	PL200 change from SH00000KS00 to SH00000YE00	
12	P45	+1.35VGPU_DDR	2013/11/13	PWR	for common part	PL1001 change from SH00000MR00 to SH00000YV00	
13	P38	VCORE	2013/11/14	PWR	Vcore test result abjustmet value	PR521 change from 95.3k to 90.9k	
14	P39	+VCCIO	2013/11/15	PWR	for common part	PL302 change form SM010009C80 to SM01000C000	
15	P33	DCIN/BATT CONN/OTP	2013/11/21	PWR	ESD requirement	**add PD3 (AZ5125-01H.R7G_SOD523-2)**	
16	P34	3.3VALWP/5VALWP	2013/11/21	PWR	change to same material	PD101 change from SCA00002A00 to SCA00001W00	
17	P41	Charger_BQ24777	2013/11/21	PWR	peak shift issue	Add PQ709	
18	P44	VGA_COREP	2013/11/21	PWR	ocp modify to 66A	PR615 change from 10.7k to 13k	
19	P38	VCORE	2013/11/25	PWR	current rating issue	PC520 change from 0402 to 0603	
20	P41	Charger_BQ24777	2013/11/26	PWR	check circuit modify error	PQ708A swap pin1 and pin6	
21	P39	+VCCIO	2013/11/28	PWR	for buyer suggest change material	PR303 chang from SD00001FX00 to SD013000080	
22	P43	Charger_BQ24777	2013/11/28	PWR	Vendor spec BQ24777_REGN modify to 5.4V	R715 change from 121k to 154k	
23	P38	VCORE	2013/12/04	PWR	DFB issue	remove PL503	
24	P41	Charger_BQ24777	2014/2/17	PWR	peak shift issue	PR729 NC	
25	P41	Charger_BQ24777	2014/2/17	PWR	PIN21 change from NC to input current limit mode	add PR706 10Kohm and pull high	
26	P41	Charger_BQ24777	2014/2/17	PWR	leakage current issue	change PD701(SCS000003800) to PD702,PD703(SCS0340L010)	
27	P41	Charger_BQ24777	2014/2/17	PWR	PIN9 change from Voltage monitor to current monitor	change PC753(100P) to PR732 (20K)	
28	P38	VCORE	2014/2/17	PWR	Vcore test result abjustmet value	PR535 change from 210 to 200	
29	P43	VGA_COREP	2014/2/17	PWR	ME Z-High issue	PC604 change from pop to de-pop,PC627 change from de-pop to pop	
30	P33	DCIN/BATT CONN/OTP	2014/2/17	PWR	hiccup mode issue	add Erp lot 6 circuit	
31	P41	**Charger_BQ24777**	**2014/2/21**	PWR	**plug Adapter system no work issue**	**add PR741 connect PQ709 Gate to GND**	
32	P44	+1.35VGPU_DDR	**2014/3/4**	PWR	**for EE suggest**	**net name change from FBVDD_EN to GFX_CORE_PG**	
33	P41	**Charger_BQ24777**	**2014/3/5**	PWR	**acoustic noise**	**add PC730,PC731,PC732 to de-pop**	
34	P41	**Charger_BQ24777**	**2014/3/11**	PWR	**Follow Houston test summary solution NC**	**PQ708A,PQ708B NC**	
34	P38	VCORE	**2014/3/11**	PWR	**acoustic noise**	**Change PC515 PC533 from VCC_PWR_SRC to B+**	
35	P37	**+1.35VP/0.675VSP**	**2014/3/14**	PWR	select the correct voltage to 2.5V	**PC214 change from SF000003000 to SF000003100**	
36	P33	DCIN/BATT CONN/OTP	**2014/3/17**	PWR	hiccup mode issue	**add PR13 NC**	
37	P34	3.3VALWP/5VALWP	**2014/3/17**	PWR	Co-Lay	**add PC116 PC117 NC**	
38	P41	**Charger_BQ24777**	**2014/3/17**	PWR	follow TI solution	**change PR725 from 100K to 1K**	
39	P41	**Charger_BQ24777**	**2014/3/21**	PWR	hiccup mode issue	**change PR739 from 316K to 294K**	
40	P34	3.3VALWP/5VALWP	**2014/3/24**	PWR	follow EC solution	PR110 NC	

Security Classification	Compal Secret Data		
Issued Date	2013/07/25	Deciphered Date	2014/07/24

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