Compal Confidential

EA50_HWS M/B Schematics Document

Intel Shark Bay SV (Haswell+ Lynx point)

Nvidia N15S-GT / N15V-GM

2014-05-27

REV:1.0

DAX

Part Number	Description
DAZ17F00100	PCB Z5WAW LA-B702P LS-B161P/B162P

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.			
Title: Cover Sheet			
Size: Custom	Document Number: Z5WAW M/B LA-B702		Rev: 0.2
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eDP

LVDS

LVDS-Translator RTD2132R page 30

page 31

Fan Control page 42

Nvidia N15x with DDR3 x4 page 23~29

HDMI Conn.

HDMI

page 32

eDP

PCIe 3.0 x4 (x8) 8GT/s

HDMI x 4 lanes

DDI

PEG

Intel Processor Haswell SV

rPGA946 37.5mm x 37.5mm P.4~10

Memory BUS Dual Channel

1.35V DDR3L 1333/1600

204pin DDR3L-SO-DIMM X1 BANK 0, 1, 2, 3 page 11

204pin DDR3L-SO-DIMM X1 BANK 4, 5, 6, 7 page 12

USB 3.0 conn x1 USB port 0

USB 2.0 conn x2 USB/B (port 1,2)

CMOS Camera USB port 7

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Touch screen page 31

TP Bridge page 40

Port 4

Port 5

page 36

MINI Card WLAN USB port 4

PCIe 2.0 5GT/s port 4

VGA

page 33

FDII x2 100MHz 2.7GT/s

DMI x4 100MHz 5GB/s

Flexible IO

Intel PCH Lynx Point

FCBGA 695Balls 20mm x 20mm P.13~22

48MHz

USBx8

HD Audio 3.3V 24MHz

Touch Pad PS2 / I2C

page 40

PCIe 2.0 5GT/s port 3

SATA3.0 6.0 Gb/s port 4

SATA3.0 6.0 Gb/s port 2

LAN(GbE)/ Card Reader Realtek 8411B page 34

SATA HDD Conn.

SATA CDROM Conn.

page 37

page 37

HDA Codec ALC283 page 41

SPI

Card Reader 2 in 1 (SD)

page 35

RJ45 conn.

page 35

LPC BUS CLK=24MHz

SPI ROM x2 page 17

Int. Speaker page 41

Combo Jack page 41

Int. MIC page 41

ENE KB9012/9022 page 39

Int.KBD

page 40

RTC CKT. page 13

Power On/Off CKT. page 40

DC/DC Interface CKT. page 43

Power Circuit DC/DC page 44~56

Sub Board

LSB161 PWR/B page 38

LSB162 USB/B (port 1,2) page 38

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.675VS	+0.675VS power rail for DDR3L terminator	ON	OFF	OFF
+1.05VS	+1.05V power rail for CPU	ON	OFF	OFF
+1.05VSDGPU	+1.05VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+1.5VSDGPU	+1.5VSDGPU power rail for GPU	ON	OFF	OFF
+1.5VS	+1.5V power rail for CPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X

EC SM Bus2 address

Device	Address
On Board Thermal Senser	0100 110x
VGA Internal Thermal Senser	0100 000x

PCH SM Bus address

Device		Address	
ChannelA	DIMM0	1010 0000	JDIMM1
ChannelB	DIMM1	1010 0010	JDIMM2

USB Port Table

USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port(Left 3.0)
	1	USB Port(Right 2.0)
	2	USB Port(Right 2.0)
	3	Finger Printer
	4	Touch Screen
	5	USB/I2C Bridge
	6	WLAN
	7	Webcam
USB 3.0	Port	
XHCI	0	USB Port(Left 3.0)
	1	
	2	
	3	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD
0	0	0 V	0 V	0 V	0x00-0x0B
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C-0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D-0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27-0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31-0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C-0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47-0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55-0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65-0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77-0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88-0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97-0xA3
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA4-0xAD
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xAE-0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8-0xC0
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC1-0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA-0xD3
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD4-0xDC
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDD-0xE6
19	NC	3.000 V	3.300 V		0xE7-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	-
3	0.3
4	1.0
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
EC 9022	9022@
EC 9012	9012@
UMA Component	UMAO@
GPU	VGA@
EDP panel	EDP@
eDP to LVDS	LVDS@
EMC Component	EMC@
EMC Reserve	XEMC@
DGPU_IDEN VGM-820M;SGT-840M	VGM@, SGT@
GC6 2.0	GC6@
non GC6	NGC6@
VRAM Selection	X76@
Digital MIC	1Dmic@/2Dmic@
USB/I2C BRI	TPBRI@
Touch Screen	TS@

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		Title	Notes List

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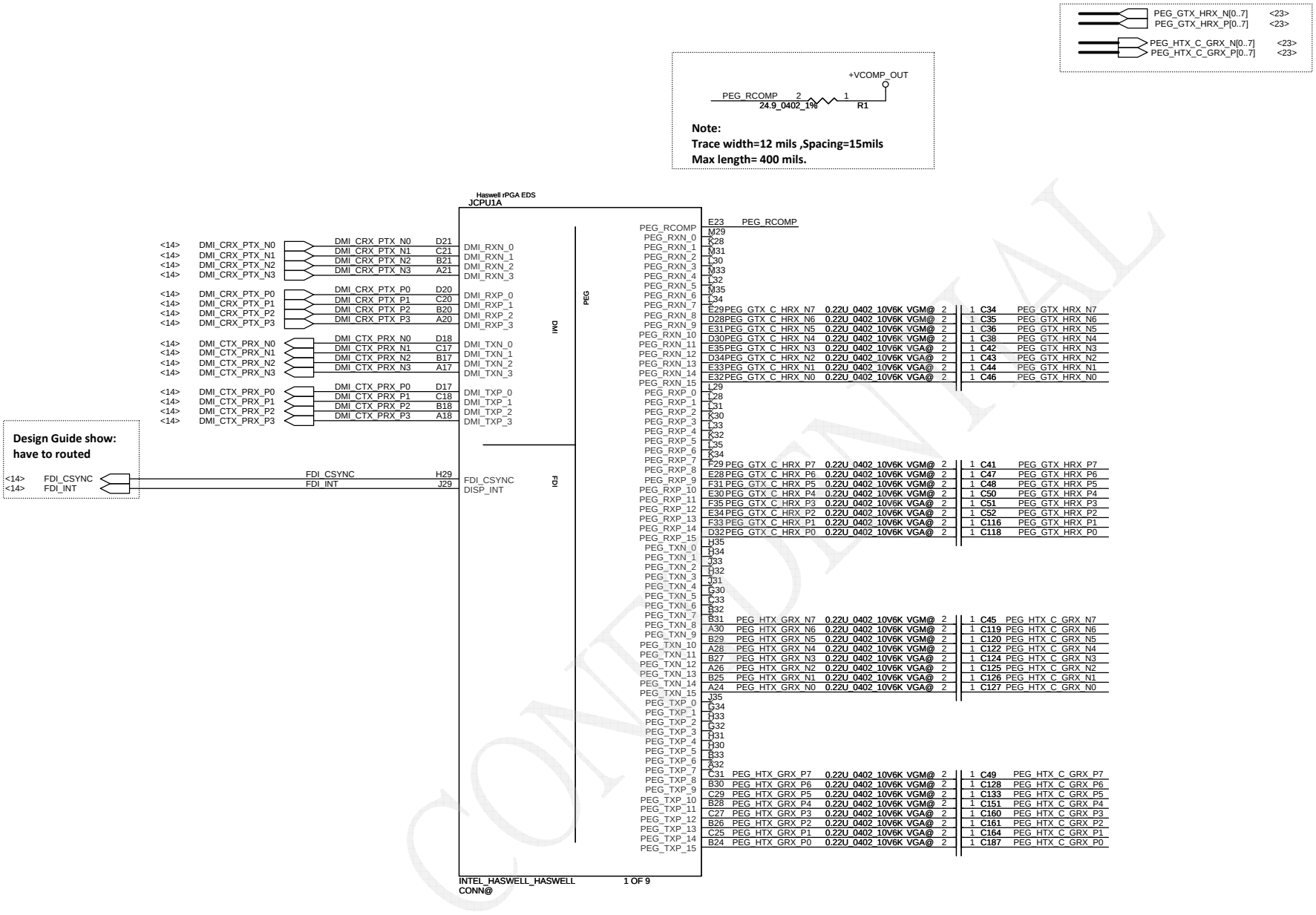

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Title: ***PROCESSOR(1/7) DMI,FDI,PEG***

Size	Document Number	Rev
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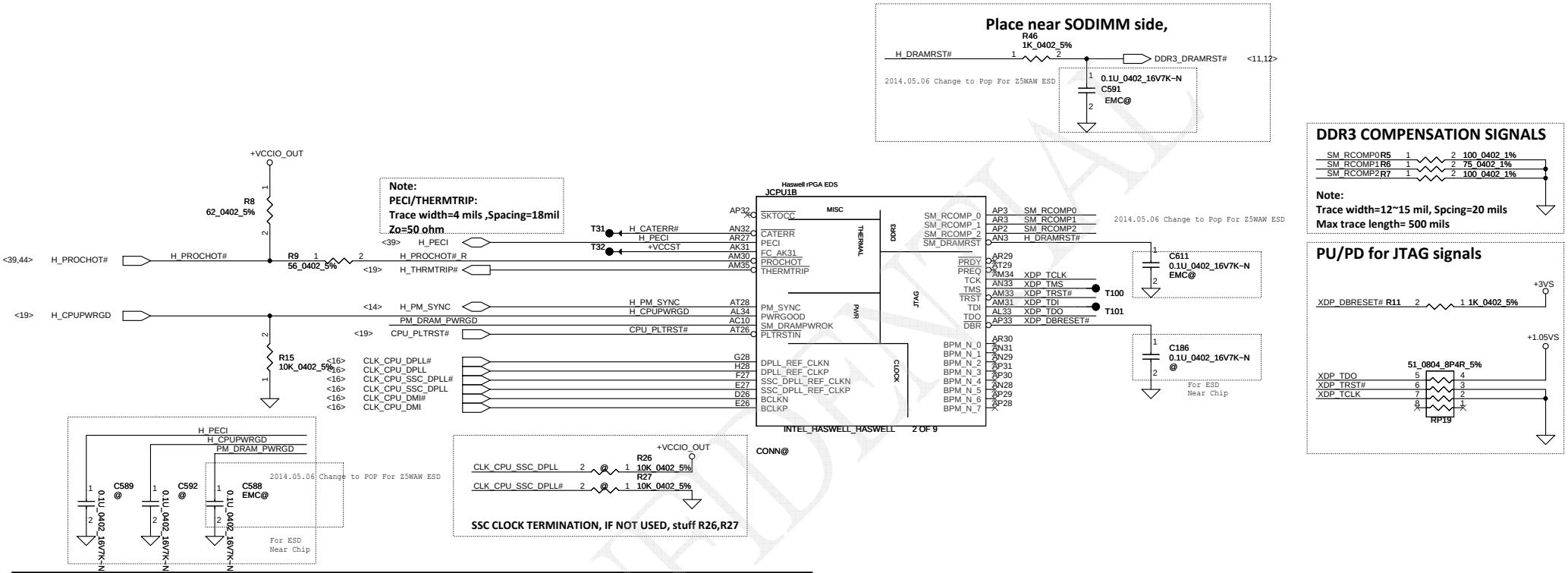

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Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

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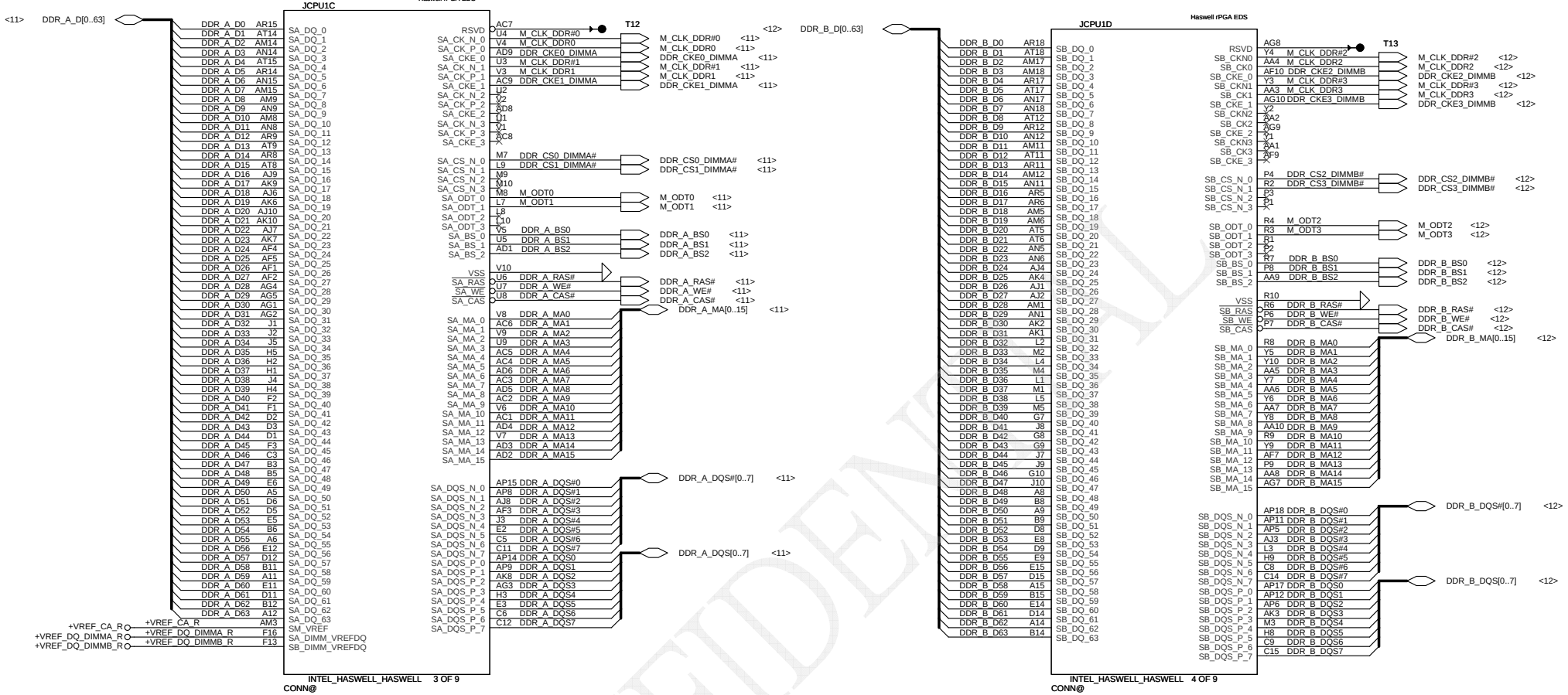

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Issued Date	2013/12/26	Deciphered Date	2014/12/26

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	Z5WAW M/B LA-B702	0.2

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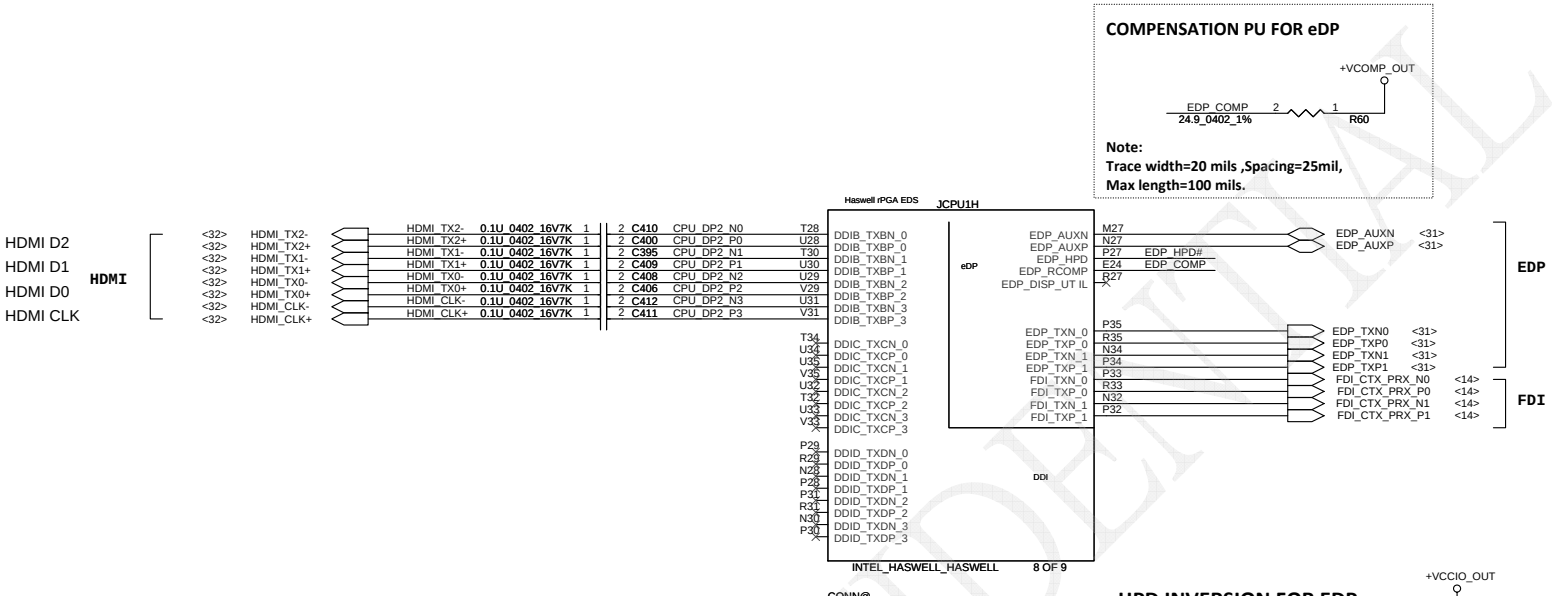

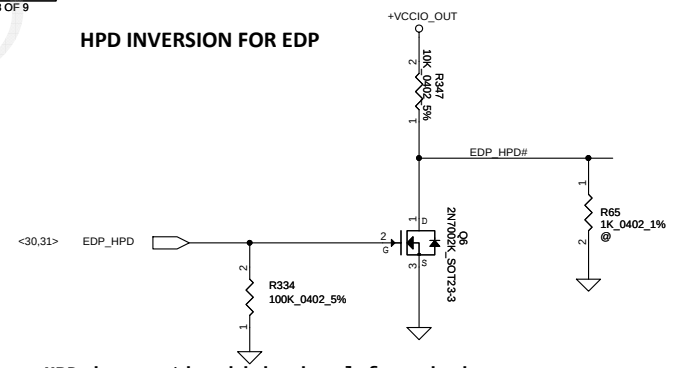

HPD is a active high signal from device. The HPD processor input is a low voltage active signal.

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Compal Electronics, Inc.			
Title	PROCESSOR(4/7) PM,XDP,CLK		
Size: Custom	Document Number: Z5WAW M/B LA-B702		Rev: 0.2
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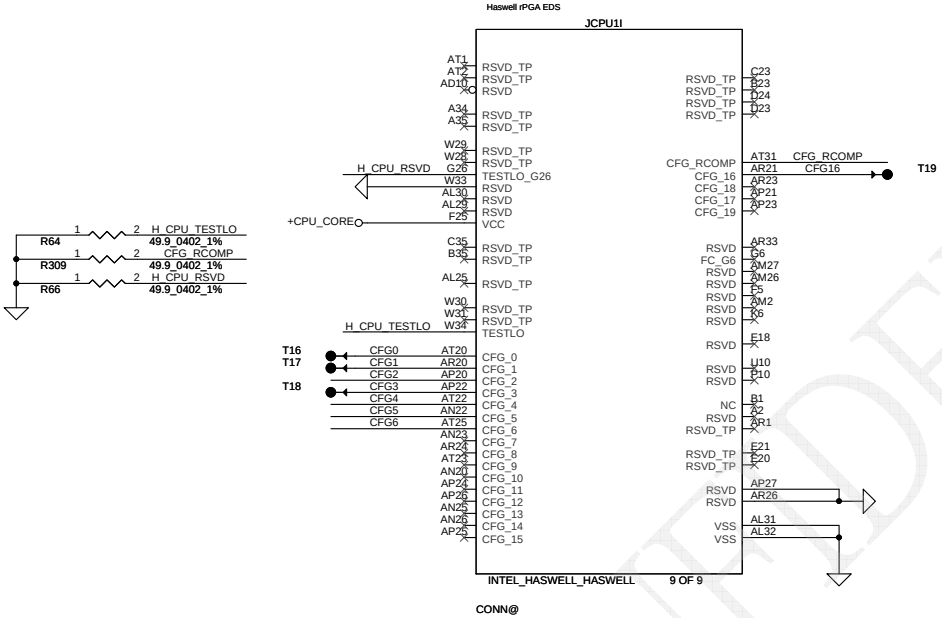
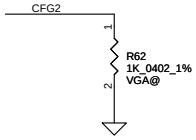
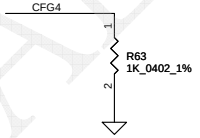
CFG Straps for Processor

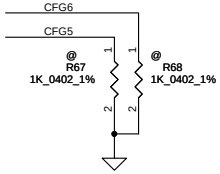




PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Embedded Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(5/7) RSVD,CFG			
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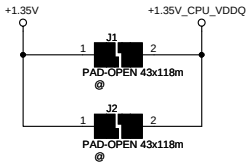
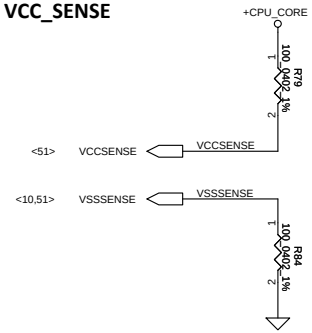
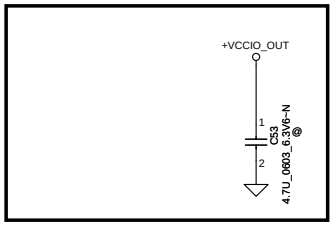
+1.35V_CPU_VDDQ Source

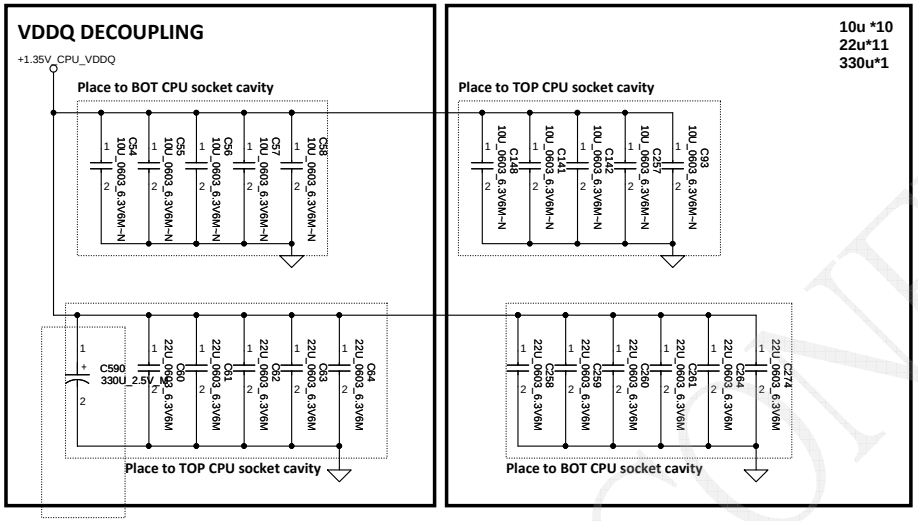


VCC_SENSE

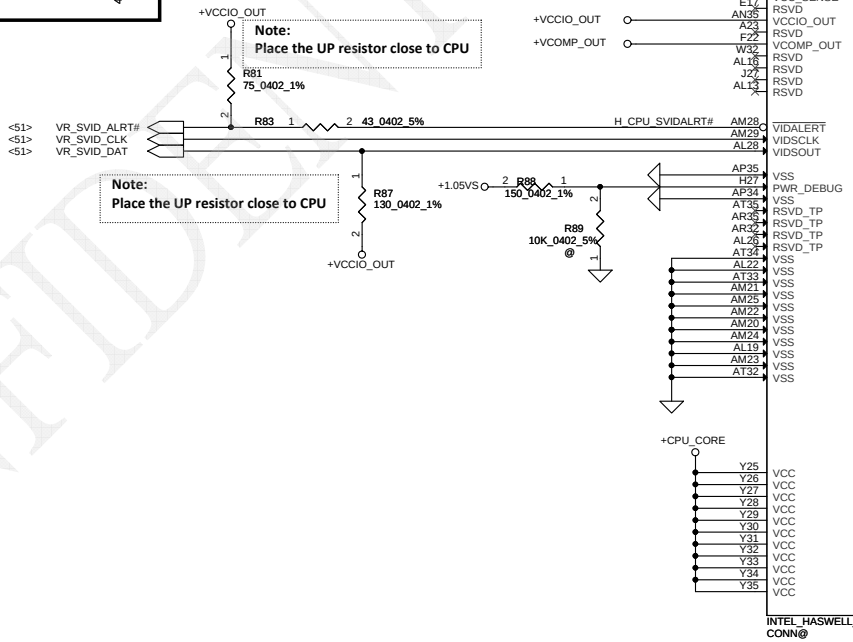




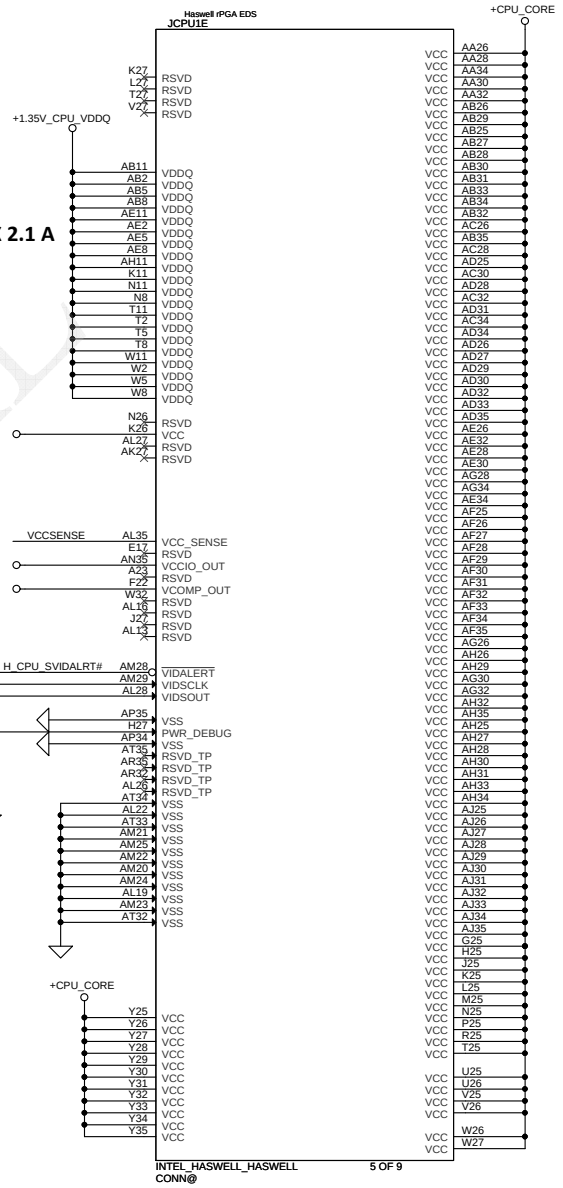
VDDQ DECOUPLING



SF000006S00
330U 2.5V H4.2
17mohm OSCON



VDDQ MAX 2.1 A



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Title: **PROCESSOR(6/7) PWR**

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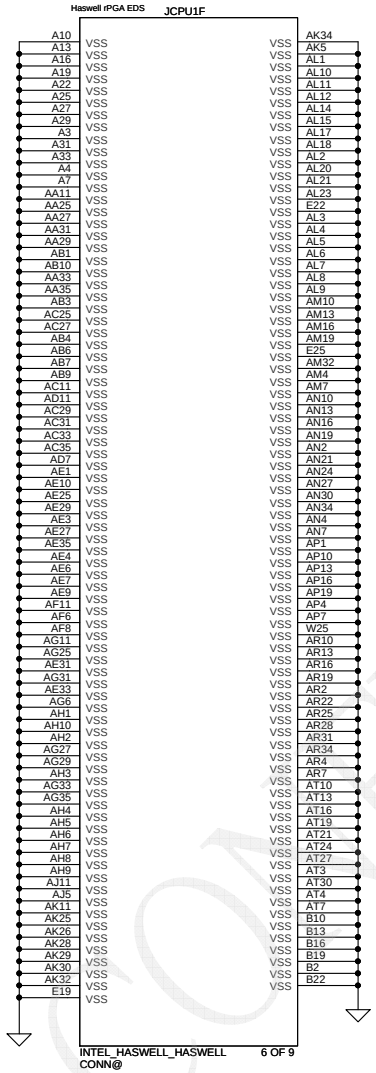

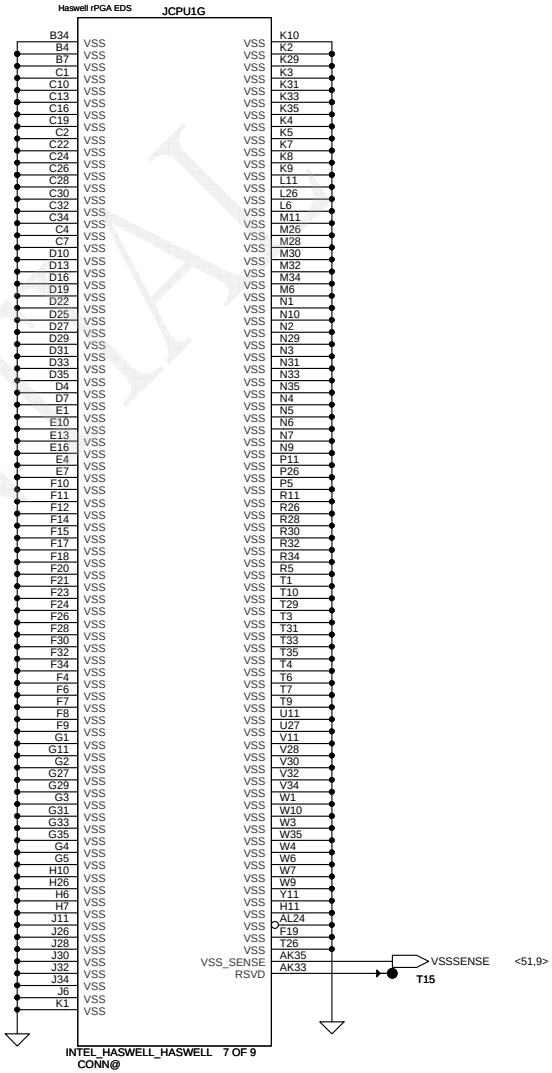

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Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size: Custom | Document Number: Z5WAW M/B LA-B702 | Rev: 0.2

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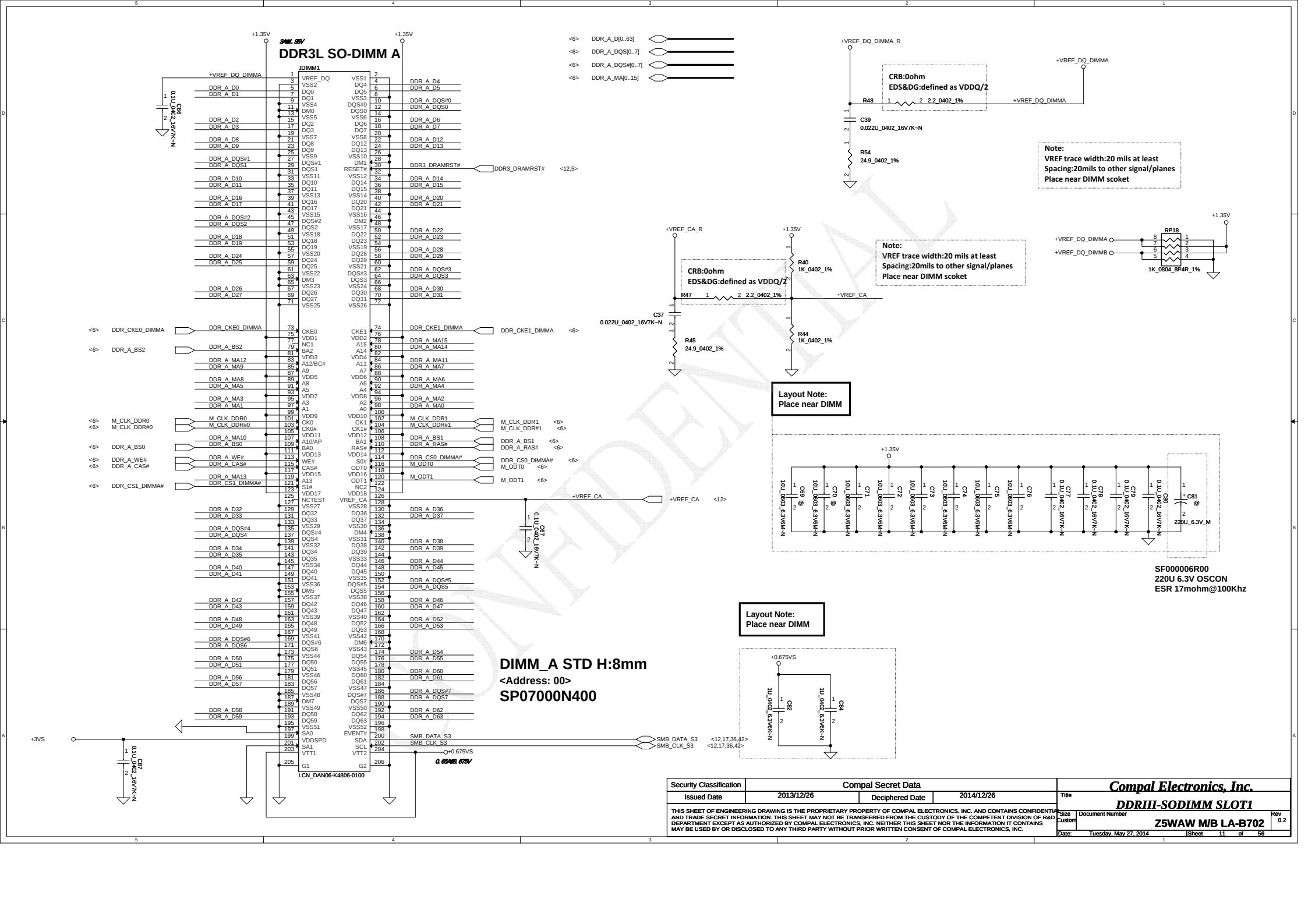
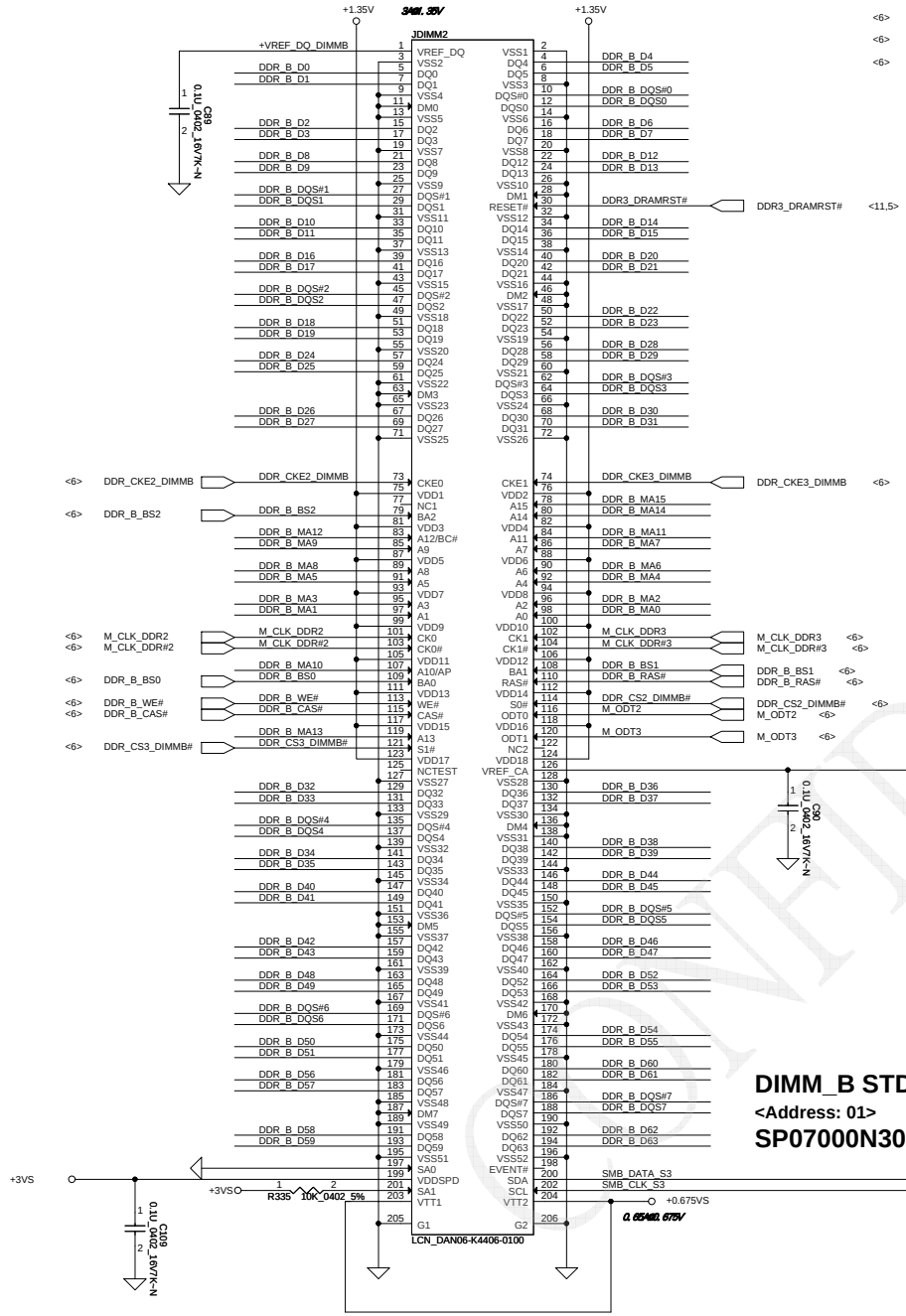
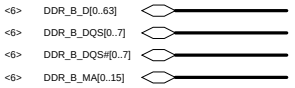
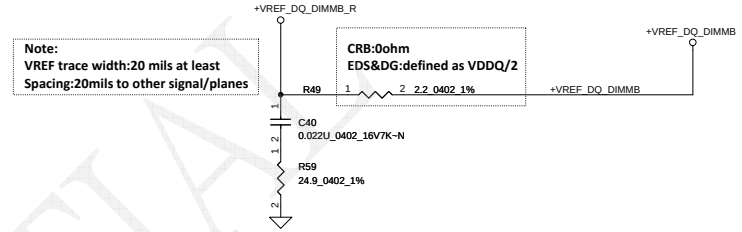
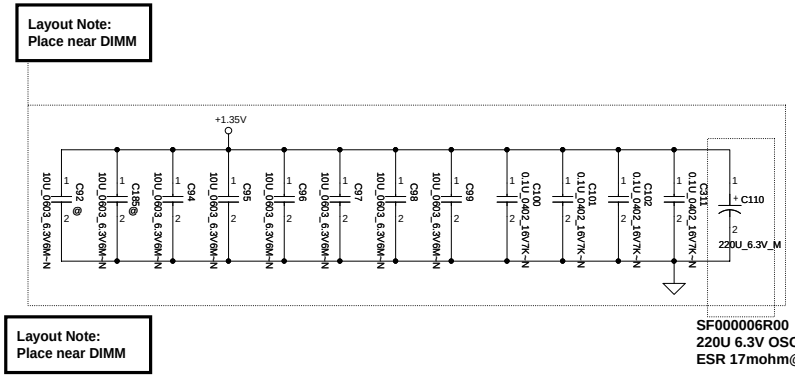


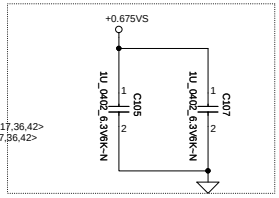








SF000006R00
220U 6.3V OSCON
ESR 17mohm@100Khz



DIMM_B STD H:4mm
<Address: 01>
SP07000N300

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Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

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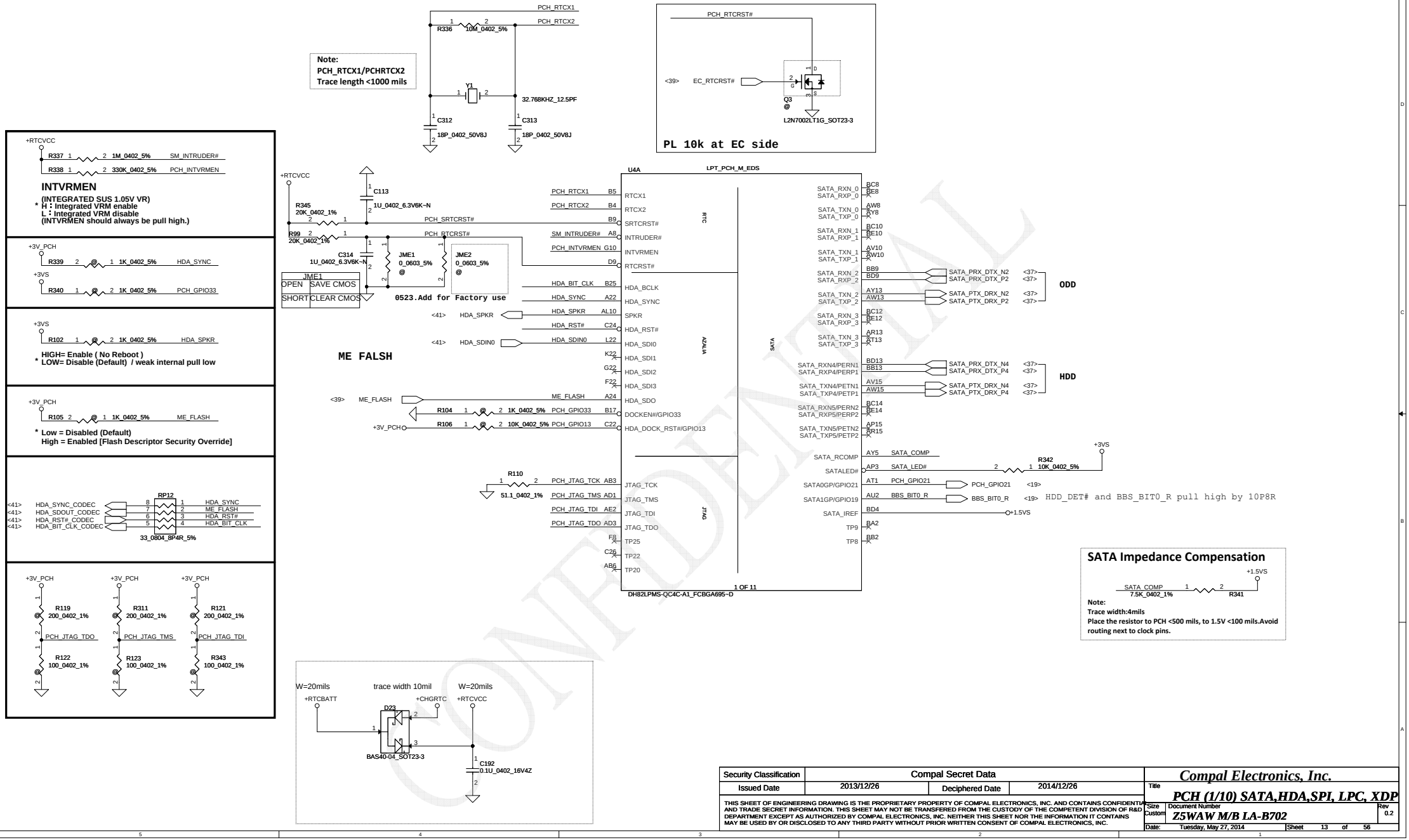

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: PCH (1/10) SATA,HDA,SPI, LPC, XDP

Size	Document Number	Rev
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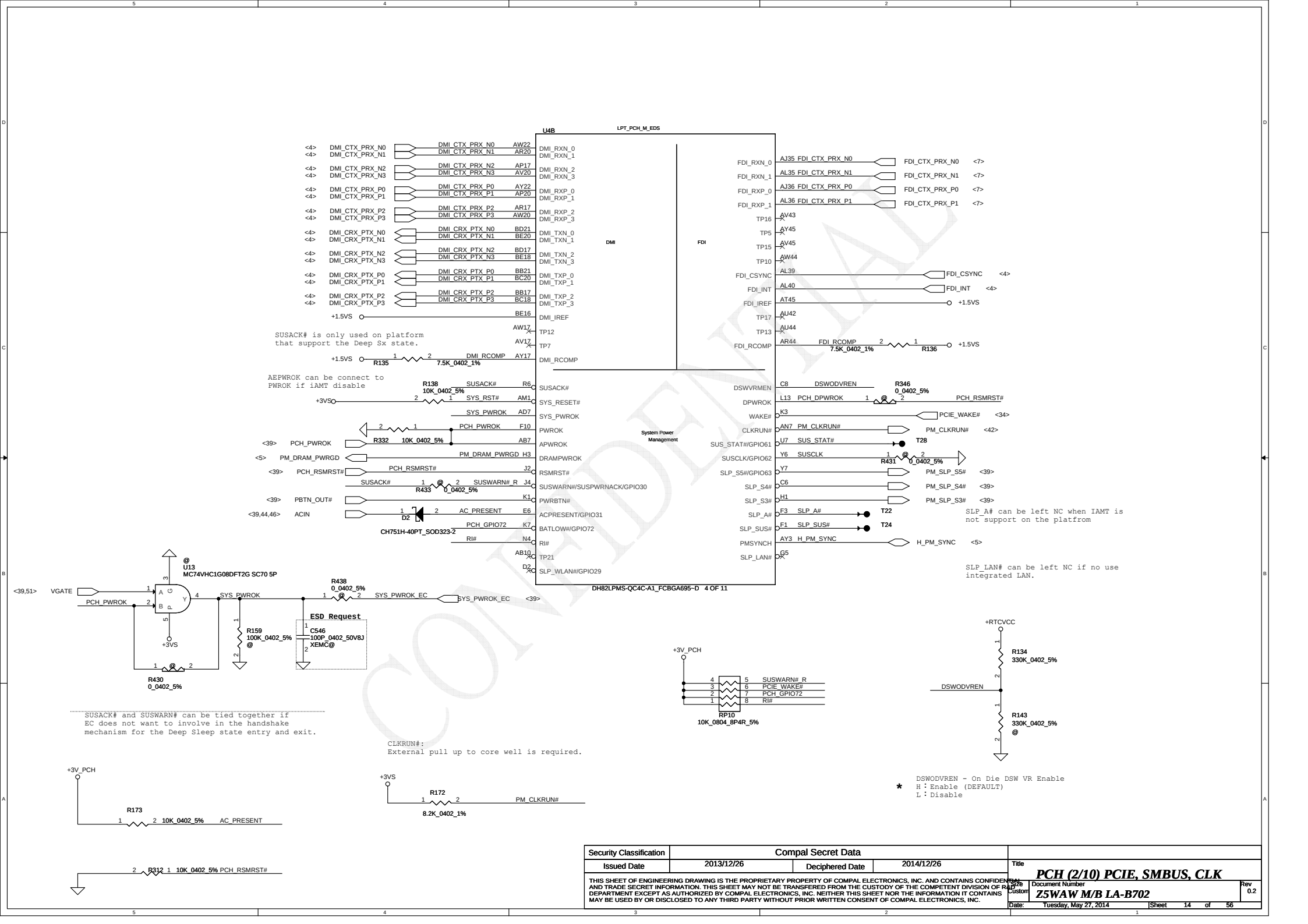

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Title	PCH (2/10) PCIE, SMBUS, CLK		
Size	Document Number		Rev
Custom	Z5WAW M/B LA-B702		0.2
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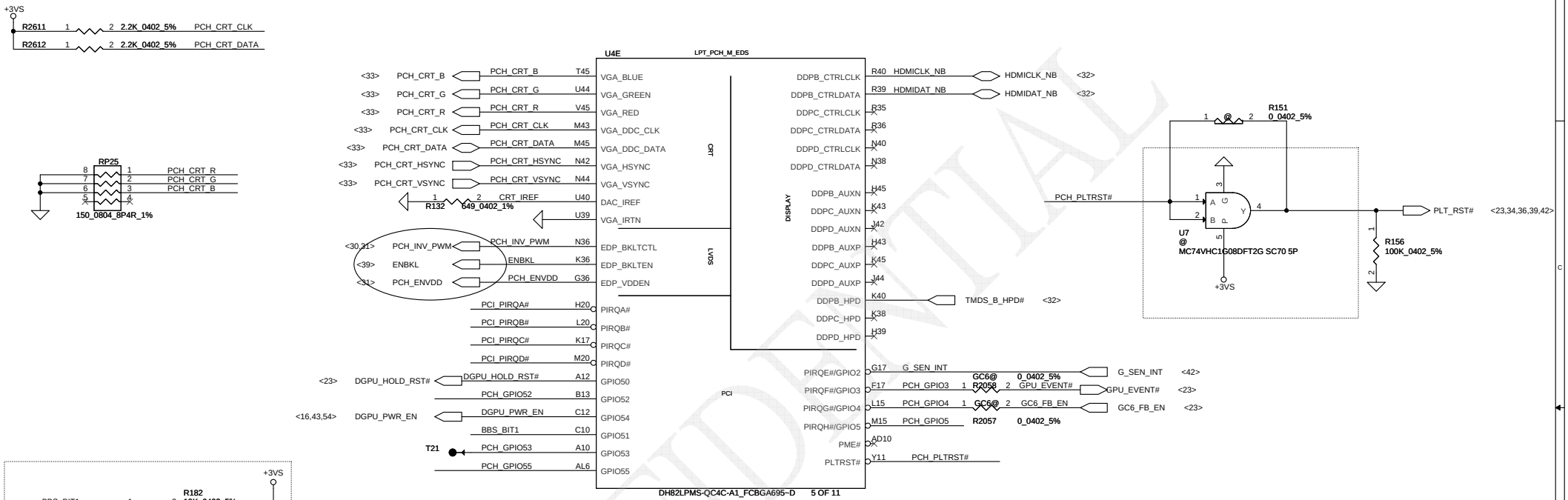

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: P14-PCH (3/10)DP,CRT

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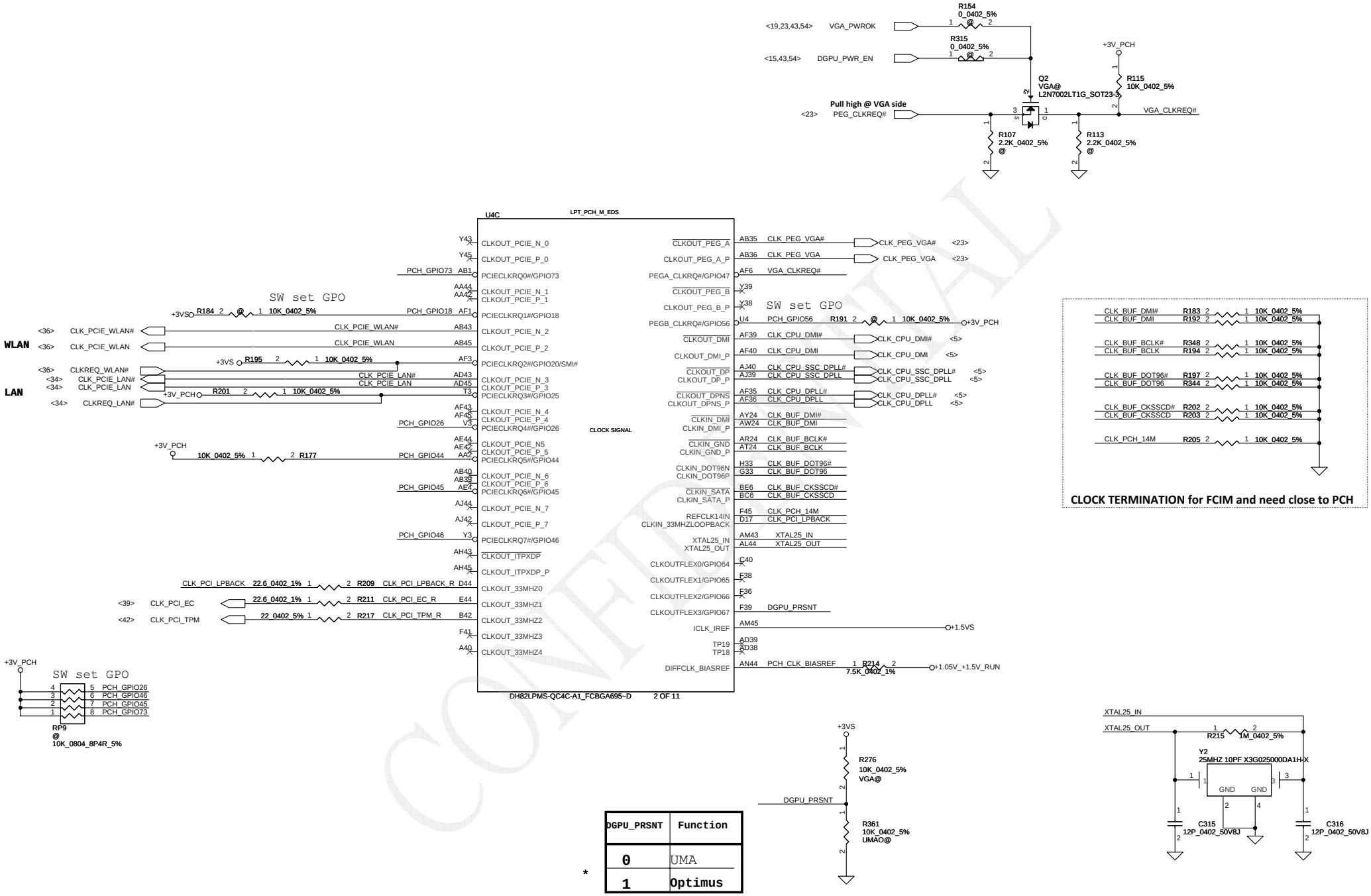

DGPU_PRSNT	Function
0	UMA
* 1	Optimus

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Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: PCH (4/10) DMI,FDI,PM,

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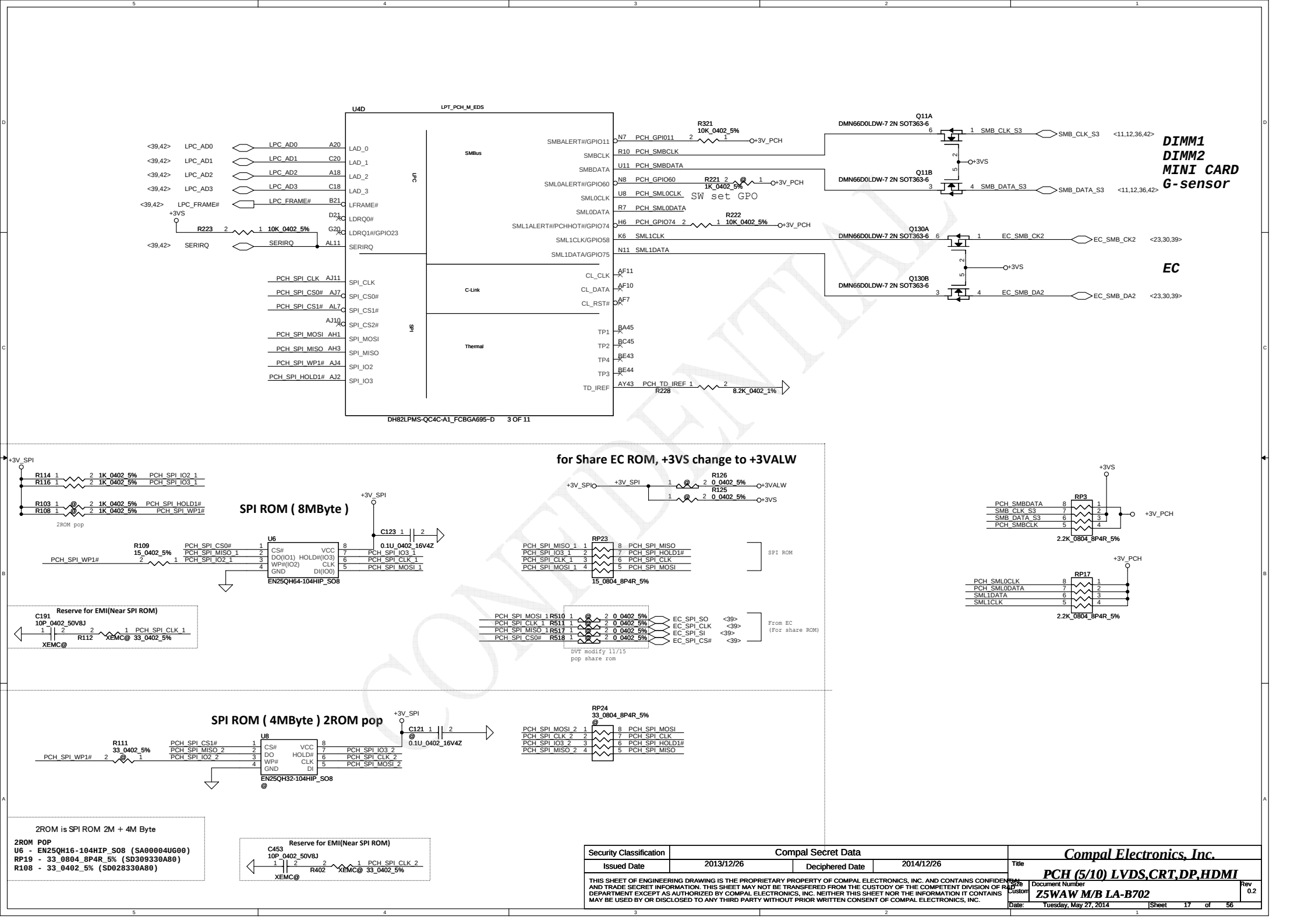

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: PCH (5/10) LVDS,CRT,DP,HDMI

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Custom	Z5WAW M/B LA-B702	0.2

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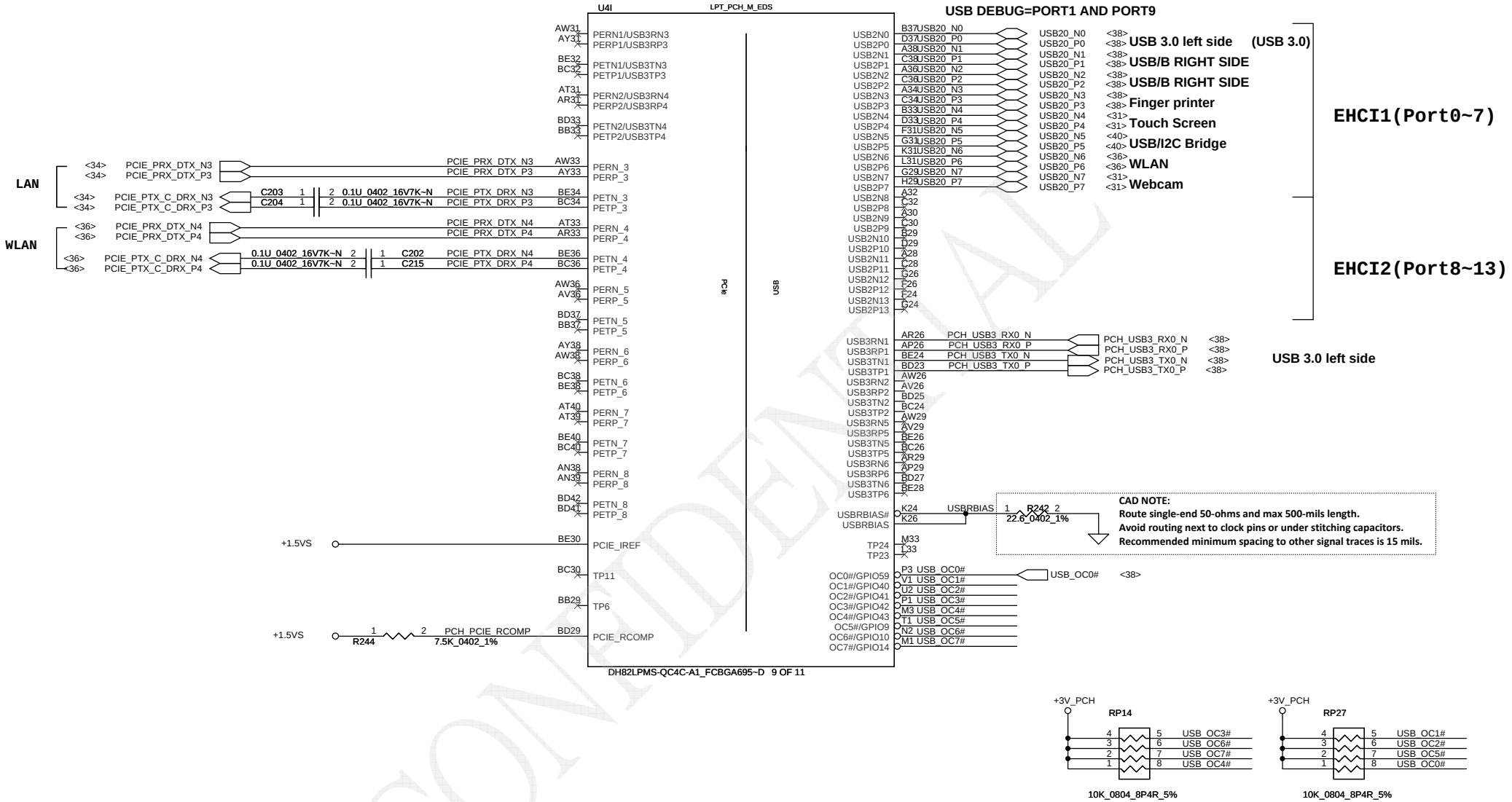


Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Title: **PCH (6/10) PCI, USB**

Size: Custom | Document Number: **Z5WAW M/B LA-B702** | Rev: 0.2

Date: Tuesday, May 27, 2014 | Sheet 18 of 56

SW set GPO

GPIO8 Weak internal pull-high but requires an external pull down.

Remove strap description
inform SW set GPO

PU at Page15

PU on power side

BIOS Request SKU ID

SW set GPO

PCH_GPIO68	PCH_GPIO69	Function
0	0	Z5WAW
0	1	Reserved
1	0	Reserved
1	1	Reserved

Config	GPIO16 & 49
USB3.0 x4, PCIE x8, SATA x6	11
USB3.0 x6, PCIE x8, SATA x4	01

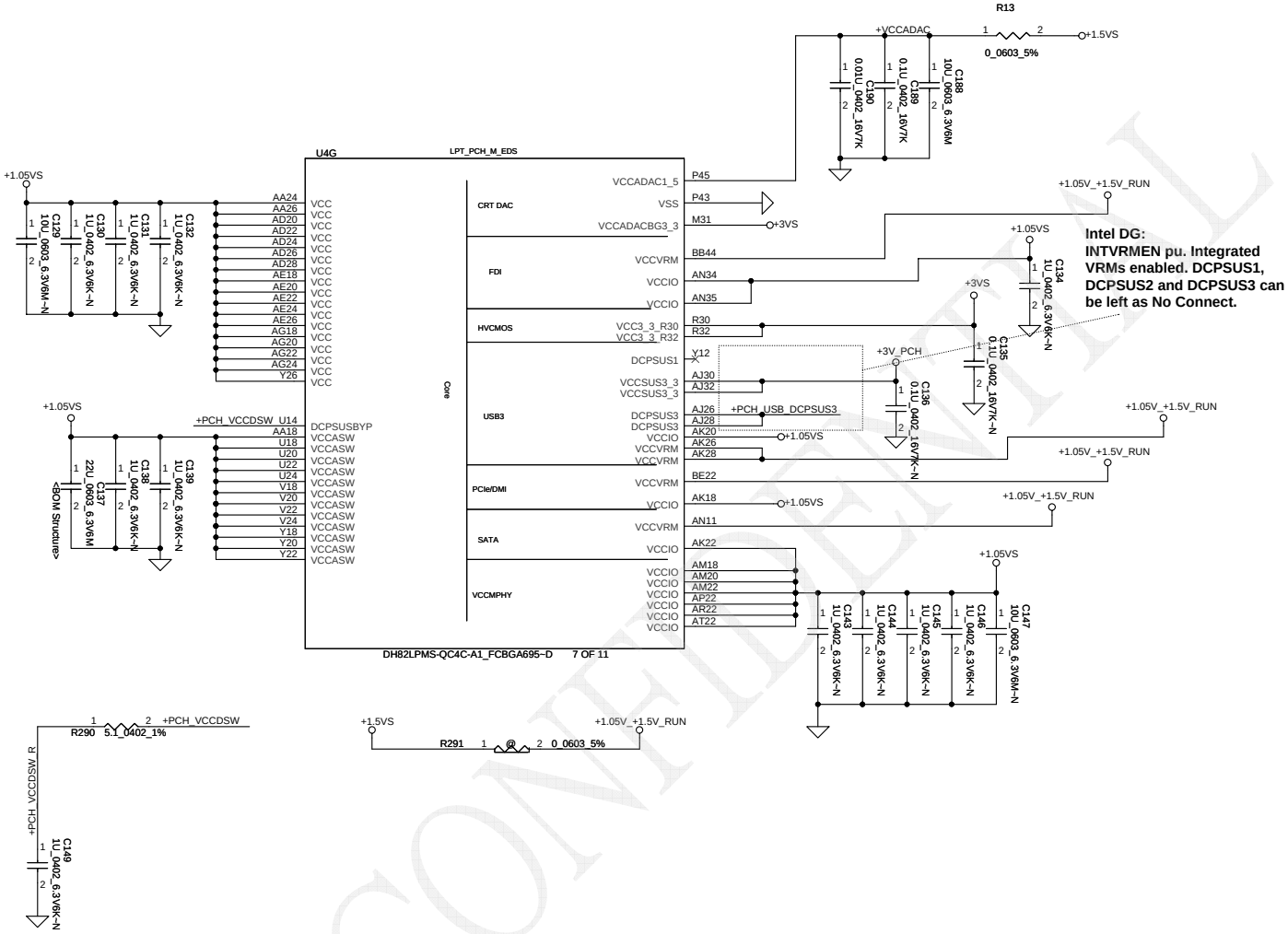
Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: PCH (7/10) GPIO, CPU, MISC

Size: Custom | Document Number: Z5WAW M/B LA-B702 | Rev: 0.2

Date: Tuesday, May 27, 2014 | Sheet 19 of 56



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

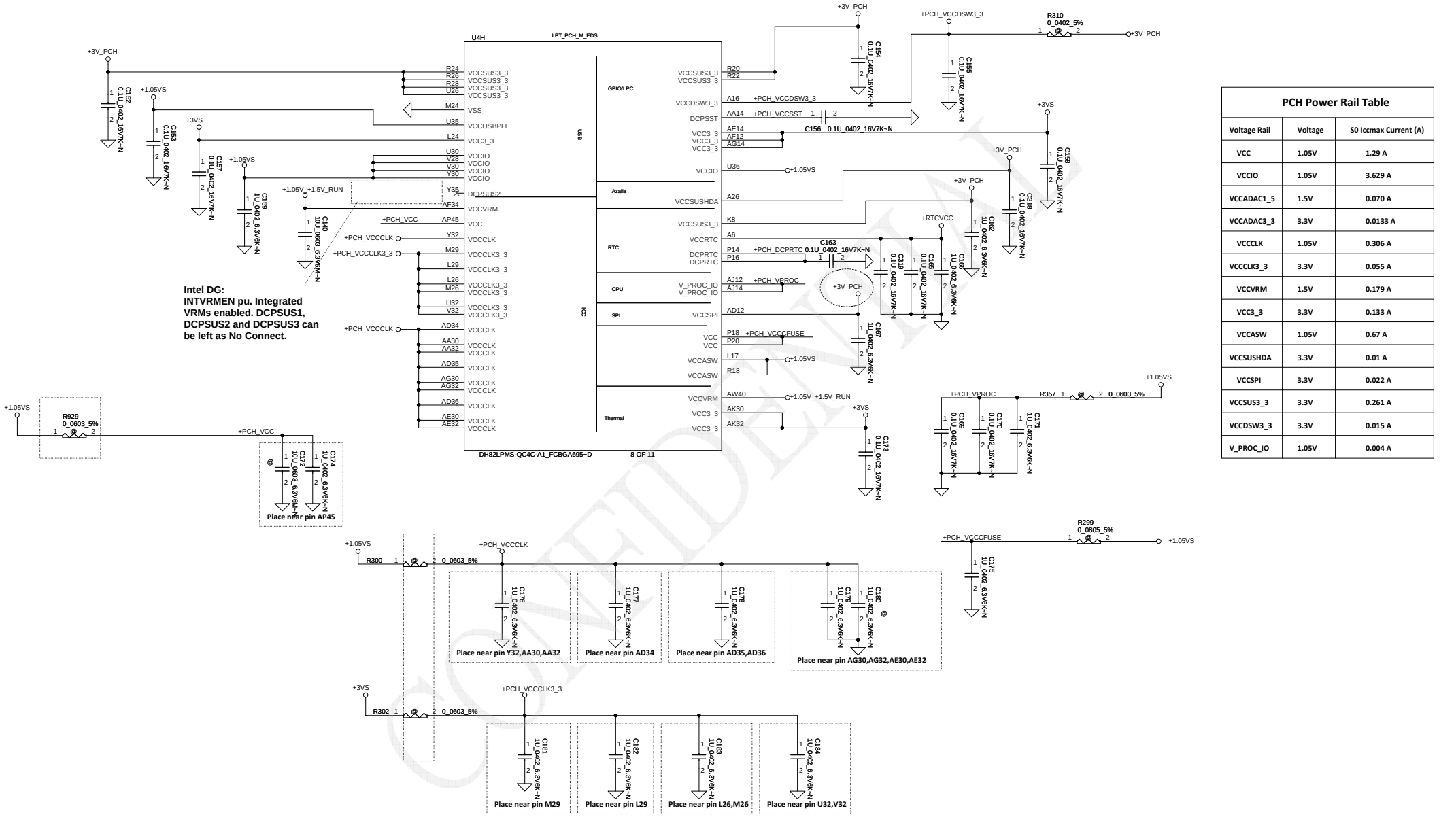
Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: PCH (8/10) PWR

Size: Custom | Document Number: Z5WAW M/B LA-B702 | Rev: 0.2

Date: Tuesday, May 27, 2014 | Sheet 20 of 56



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.			
Title: PCH (9/10) PWR			
Size: Custom	Document Number: Z5WAW M/B LA-B702		Rev: 0.2
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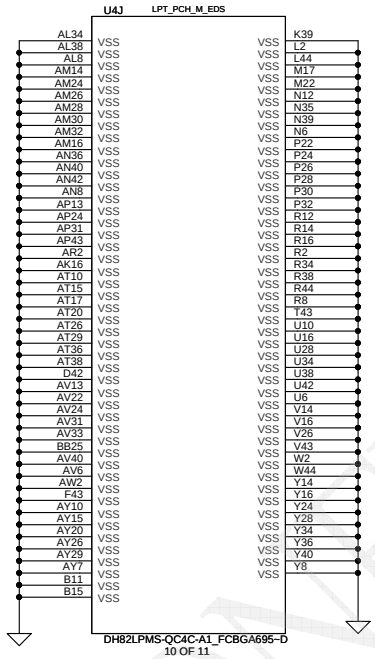

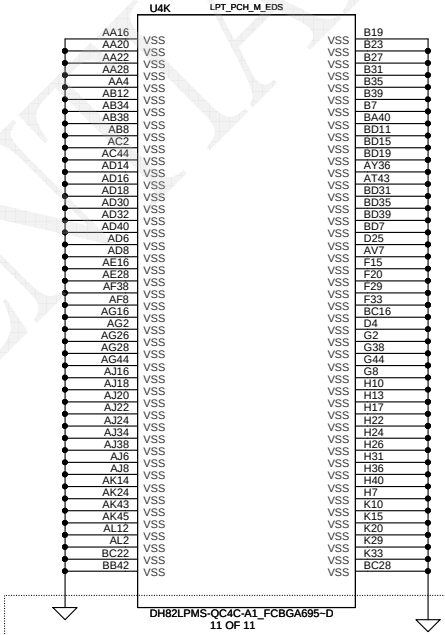

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: PCH (10/10) VSS

Size: Custom | Document Number: Z5WAW M/B LA-B702 | Rev: 0.2

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GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		

UGPU1A — Part 1 of 6 — PCI EXPRESS / GPIO / DACs / I2C / CLK

N15S-GT-S-A2_BGA_595P SGT@ SA00007GJ10

N15V-GM-S-A2_BGA_595P VGM@ SA00007BR20

GM108-ES-S-A1_FCBGA595 @

GC6 2.0 function

D2001 GC6@ BAV70W_SOT323-3

R2016 0_0402_5% NGC6@

R2014 10K_0402_5% GC6@

U2001 VGA@ MC74VHC1G08DFT2G_SC70-5

R2019 0_0402_5% NGC6@

R2017 10K_0402_5% VGA@

R2055 10K_0402_5% GC6@

D2002 BAT54A-7-F_SOT23-3 GC6@

DVT modify 11/20
use diode need to pull high
use AND gate need to pull down

PLL_VDD
0.1Ux1, 22Ux1
33ohm(ESR0.05)x1

SP_PLLVDD+VID_PLLVDD
0.1Ux2, 4.7Ux1,22Ux1
180ohm(ESR0.2)x1

SM010019400 3000ma 33ohm@100mhz DCR 0.05

38mA

L2000 CHILISIN PBY160808T-330Y-N

C2003 VGA@ 22U_0603_6.3V6M

Near GPU

SM010028480 1500ma 180ohm@100mhz DCR 0.18

17mA

L2001 BLM18PG181SN1D_2P

C2006 VGA@ 4.7U_0603_6.3V6K

C2007 VGA@ 22U_0603_6.3V6M

Near GPU

X2000 VGA@ 27MHZ_10PF_7V27000023

C2004 VGA@ 10P_0402_50V8J

C2005 VGA@ 10P_0402_50V8J

Crystals must have a max ESR of 80 ohm

DVT modify 11/27
TXC recommend from 18P change to 10P
X2000 from SJ100009700 change to SJ10000G300

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Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: N15X PEG 1/7

Size: Custom | Document Number: Z5WAW M/B LA-B702 | Rev: 0.2

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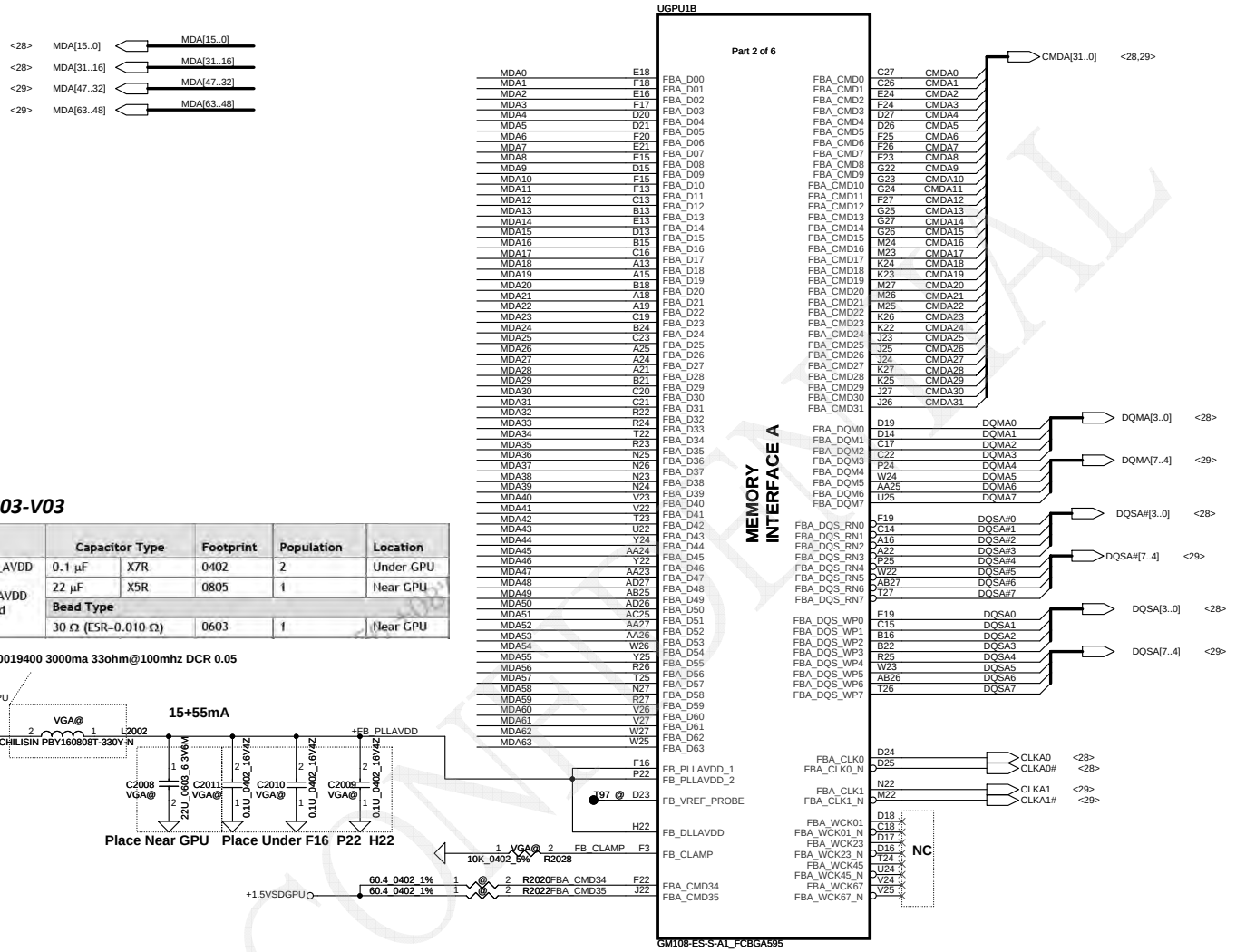
VRAM Interface



GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.			
Title: N15X VRAM 2/7			
Size: Custom	Document Number: Z5WAW M/B LA-B702		Rev: 0.2
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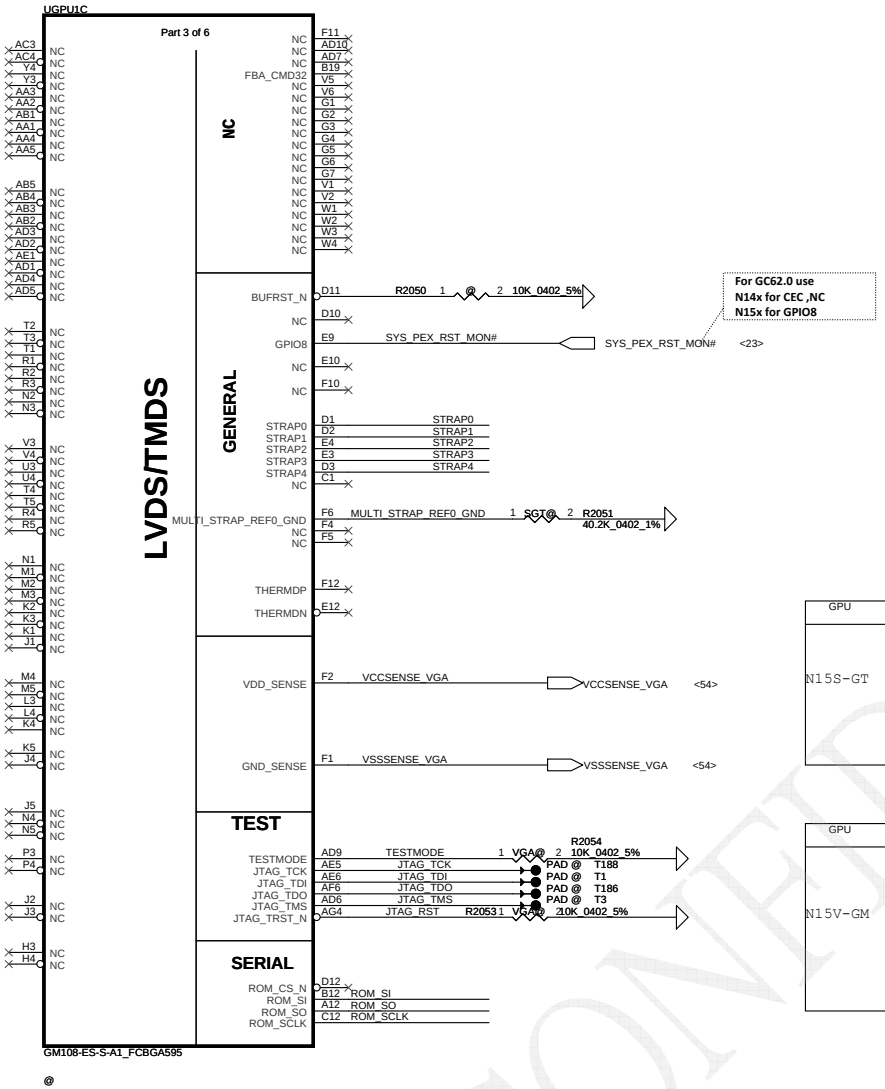
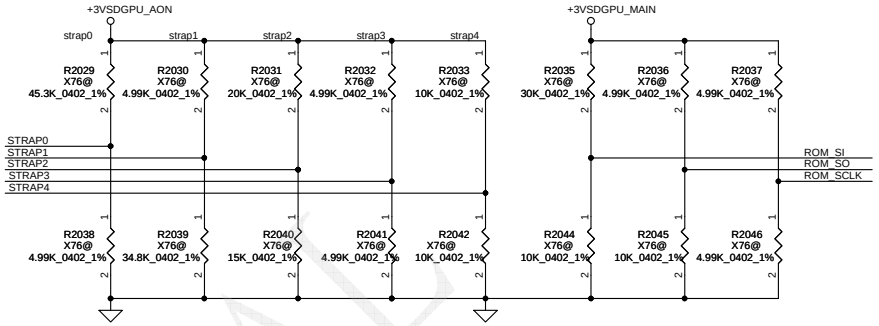


MULTI LEVEL STRAPS



For N15S-GT Multilevel strap table — Decive ID : 0x1341

GPU	X76	Size	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N15S-GT		1G	128Mx16x4		PU 50K	NC	NC	NC	NC		PD 4.99K	PD 4.99K
	X76550BOLA0	2G	256Mx16x4	0x4 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 24.9K		
	X76550BOLA1			0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30.1K		
	X76550BOLA2			0x3 (SA00006E840) Hynix H5TC4G63AFR-11C						PD 20K		

For N15V-GL/GM Binary strap table — Decive ID : 0x1140

GPU	X76	Size	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N15V-GM	X76550BOLA3	1G	128Mx16x4	0x1 (SA000067550) Micron MT41J128M16JT-093G:K	PU 10K	PD10K	PD 10K	PD 10K				
	X76550BOLA4			0x5 (SA000068U00) Samsung K4W2G1646E-BC1A	PU 10K	PD10K	PU 10K	PD 10K				
	X76550BOLA5			0xC (SA00006H430) Hynix H5TC2G63FFR-11C	PD 10K	PD10K	PU 10K	PD 10K				
										PD 10K	PD 10K	PD 10K	PD 10K
	X76550BOLA6	2G	256Mx16x5	0xD (SA000077K20) MT41J256M16HA-093G:E	PU 10K	PD10K	PU 10K	PD 10K				
	X76550BOLA7			0x9 (-) K4W4G1646D-BC1A	PU 10K	PD10K	PD 10K	PD 10K				
	X76550BOLA8			0x4 (-) H5TC4G63AFR-11C	PD 10K	PD 10K	PU 10K	PD 10K				

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Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: N15X LVDS 3/7

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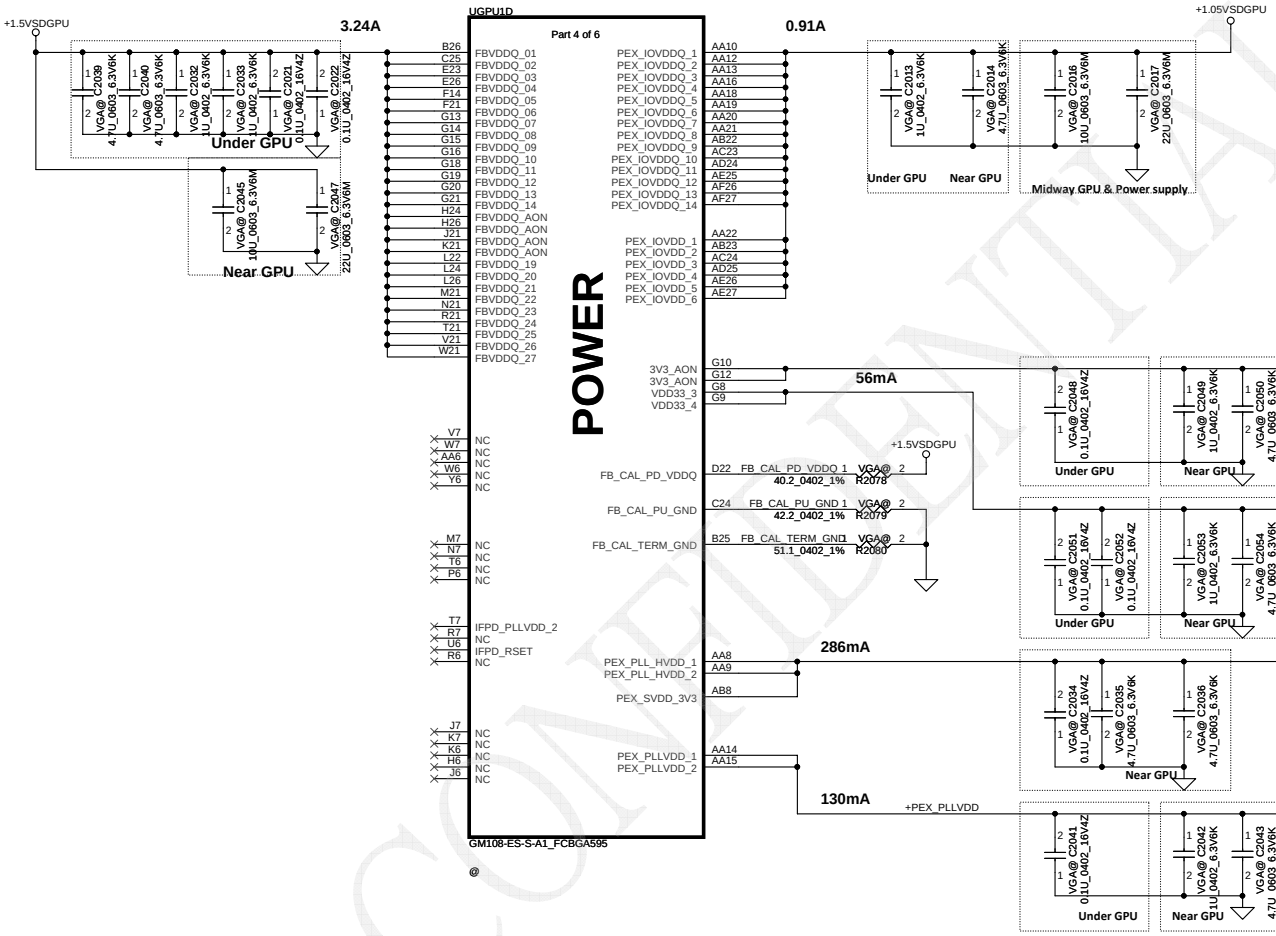
NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64 DDR3	0.1μF	X7R	0402	2	2	Under GPU
	1 μF	X7R	0603	2	2	Under GPU
	4.7 μF	X6S	0603	2	2	Under GPU
	10 μF	X5R	0805	1	1	Near GPU
	22 μF	X5R	0805	1	1	Near GPU

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 μF	X6S	0402	1	Under GPU
	4.7 μF	X6S	0603	1	Near GPU
	10 μF	X5R	0805	1	Midway between GPU and Power Supply
	22 μF	X5R	0805	1	Midway between GPU and Power Supply



GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1μF	X6S	0402	2	2	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1μF	X6S	0402	1	1	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X5R	0402	1	Near GPU
4.7 μF	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X6S	0402	1	Under GPU
1.0 μF	X5R	0603	1	Near GPU
4.7 μF	X5R	0805	1	Near GPU

SM01000BW00 3000ma 120ohm@100mhz DCR 0.04

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Title: N15X POWER & GND 4/9

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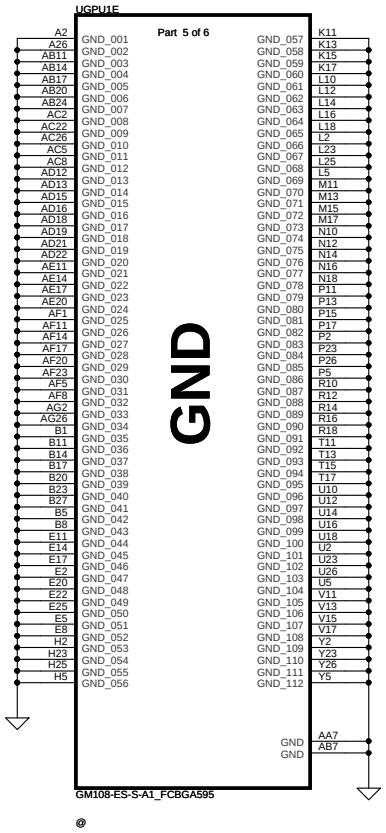

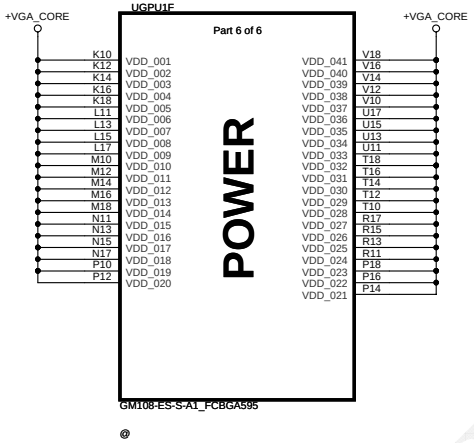

NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core — (A)	FB Total 1.5/1.35V (A)	1.05V Total 1.05V (A)
~~N15S-GM~~	~~DDR3/L~~	~~48.11~~	~~4.23~~	~~0.91~~
N15S-GT	DDR3/L	60.07	4.26	0.91

DA-06925-V05

Table 6. EDP-Peak at T_J = 102°C

Power Supply Rail	N15V-GM-S DDR3/L
(V)	(A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

DA07075-V01

Table 7. EDP-Peak at T_J = 102°C

Power Supply Rail	N15V-GL DDR3
(V)	(A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

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Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.			
Title: N15X POWER & GND 5/7			
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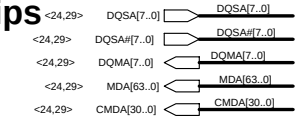
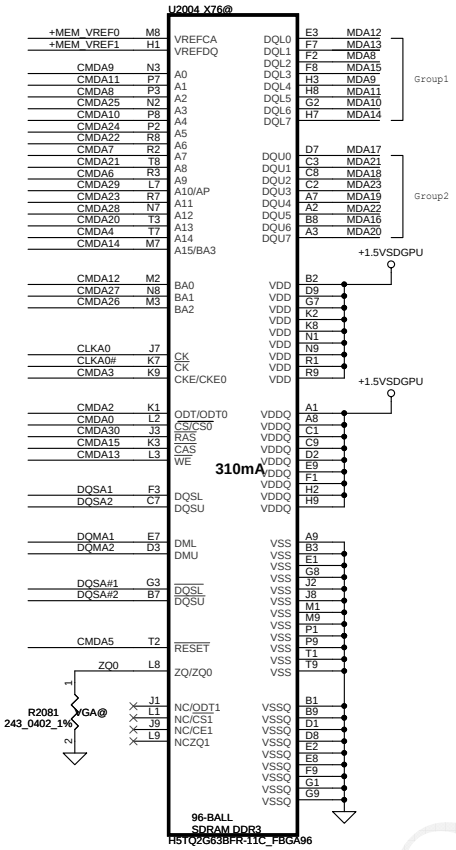
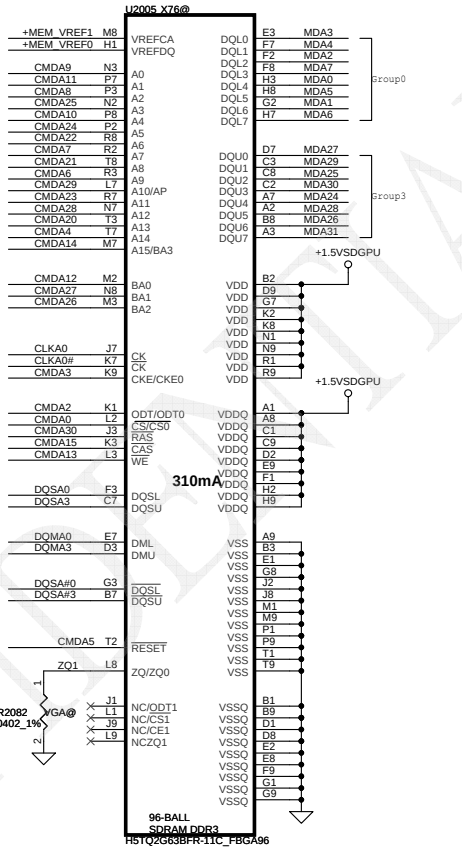
VRAM DDR3 chips

Upper 32

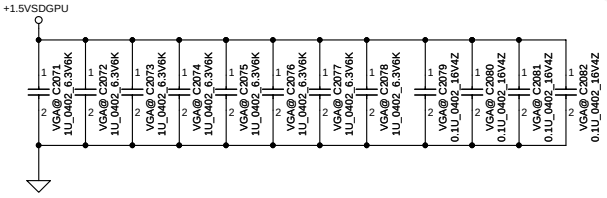


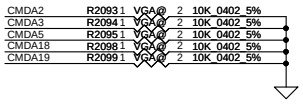


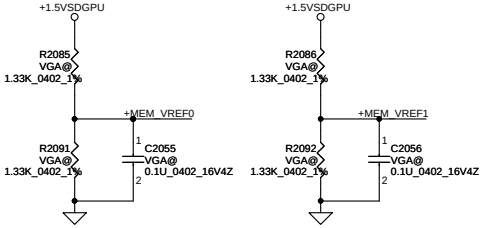


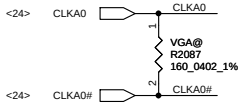
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination









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Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.			
Title: N15X DDR3 6/7			
Size: Custom	Document Number: Z5WAW M/B LA-B702		Rev: 0.2
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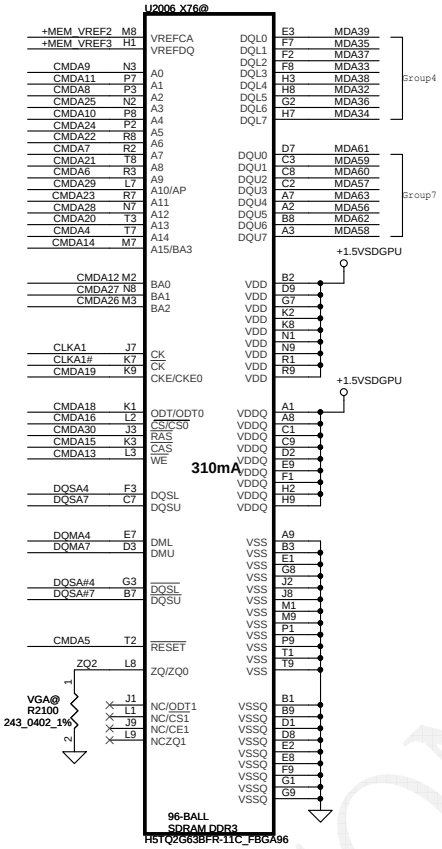
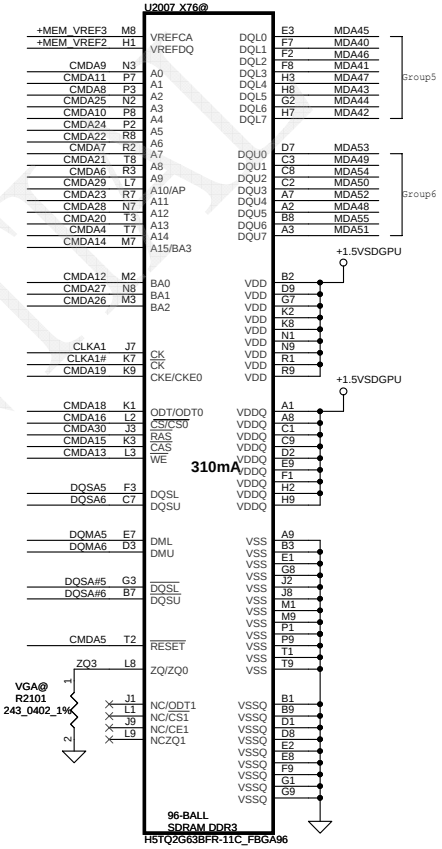
VRAM DDR3 chips

<24,28> DQSA[7..0] DQSA[7..0]
<24,28> DQSA#[7..0] DQSA#[7..0]
<24,28> DQMA[7..0] DQMA[7..0]
<24,28> MDA[63..0] MDA[63..0]
<24,28> CMDA[30..0] CMDA[30..0]

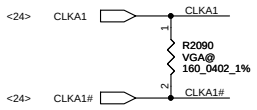
Lower 32

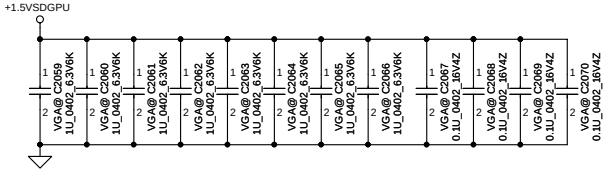


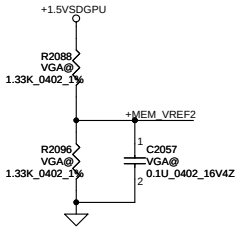


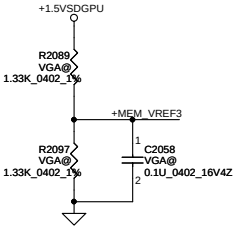
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination









Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

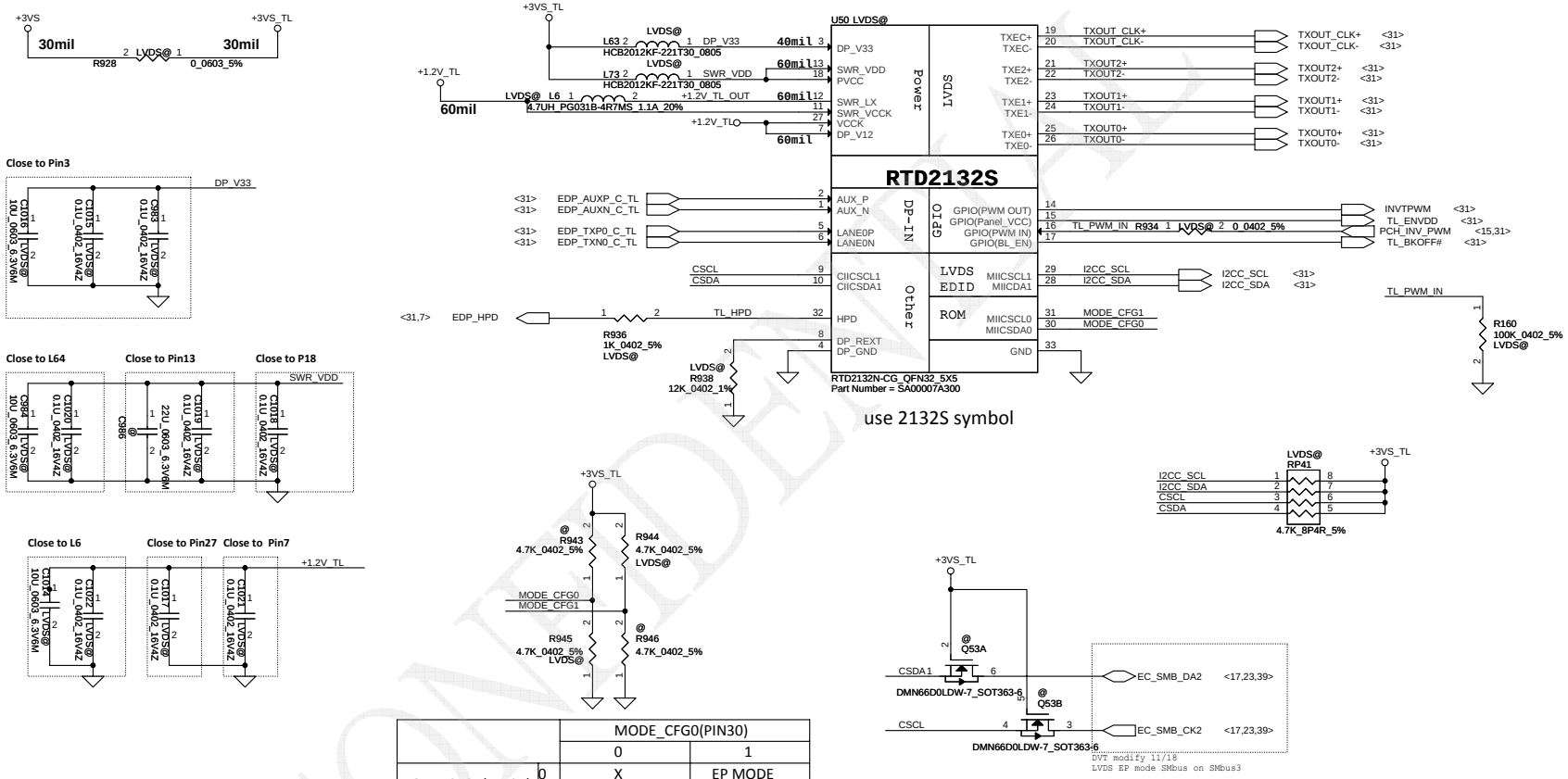
Compal Electronics, Inc.

Title: N15X DDR3 7/7

Size: Custom | Document Number: Z5WAW M/B LA-B702 | Rev: 0.2

Date: Tuesday, May 27, 2014 | Sheet 29 of 56

LVDS Translator - RTD2132R



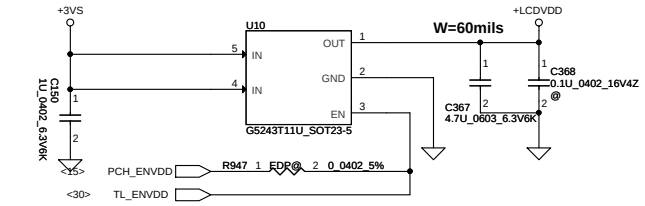
		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE*	EEPROM MODE

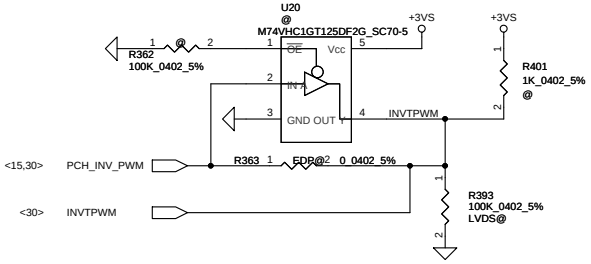
Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

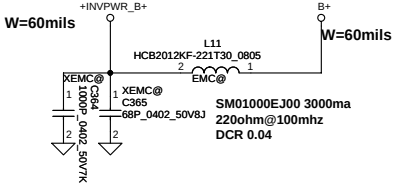
Title	LVDS Translator - RTD2132R		
Size: Custom	Document Number: Z5WAW M/B LA-B702		Rev: 0.2
Date: Tuesday, May 27, 2014	Sheet 30 of 56		

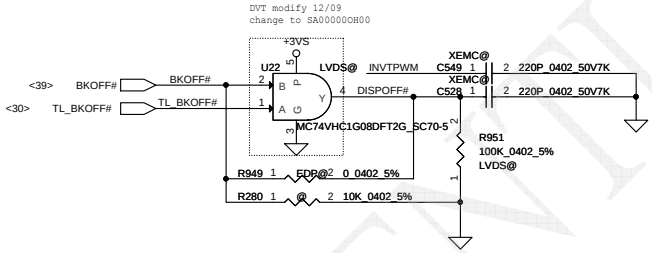
EDP / LVDS conn.

LCD POWER CIRCUIT

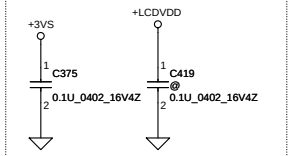




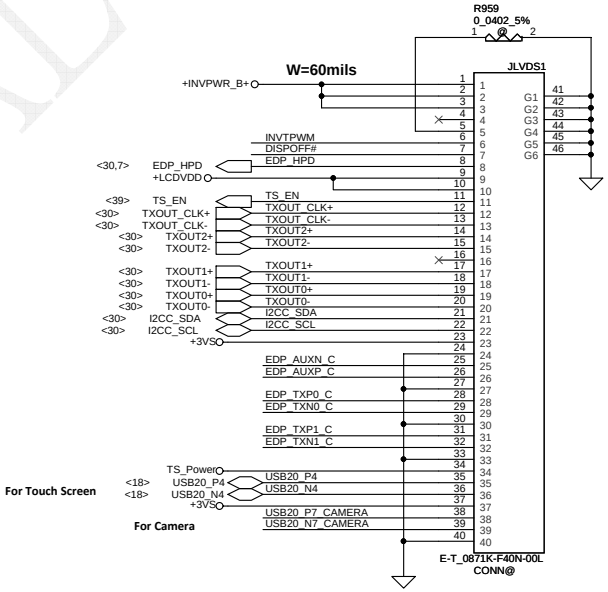




Place closed to JLVDS1

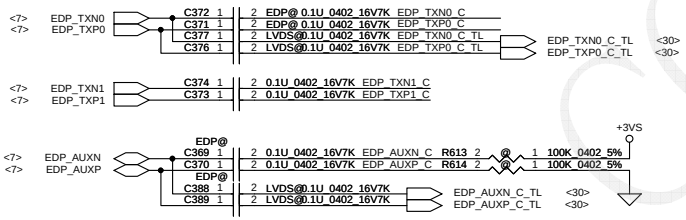


LCD/ LED PANEL Conn.

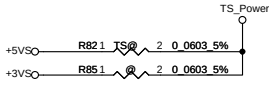


SP010011Z00

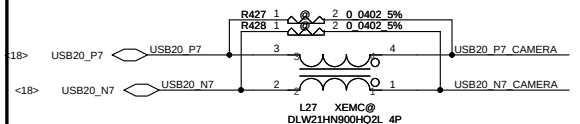
eDP

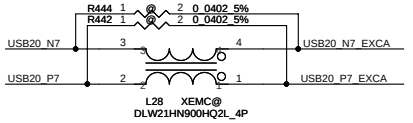


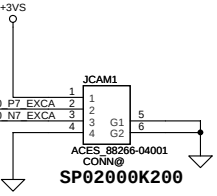
Touch Screen



Camera







SP02000K200

NEAR EDP CONNECTOR

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: eDP Connector

Size	Document Number	Rev
Custom	Z5WAW M/B LA-B702	0.2

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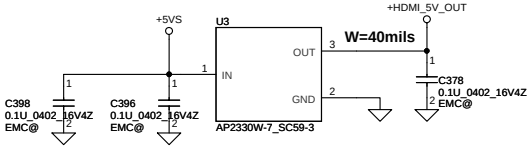
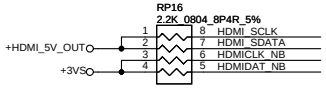
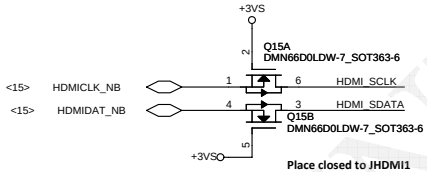
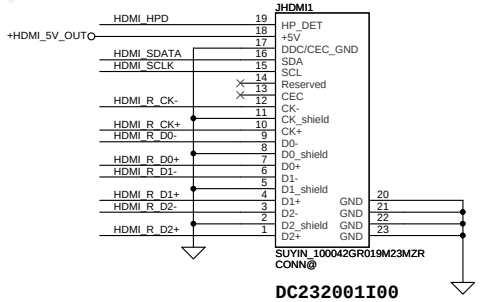
HDMI conn.

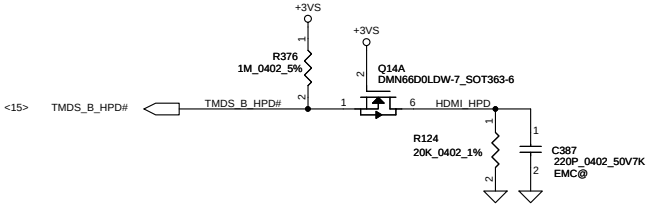


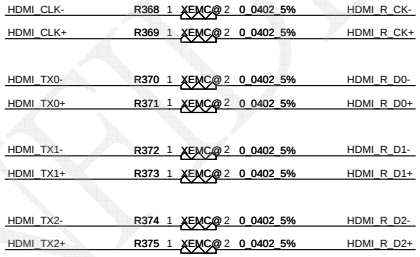


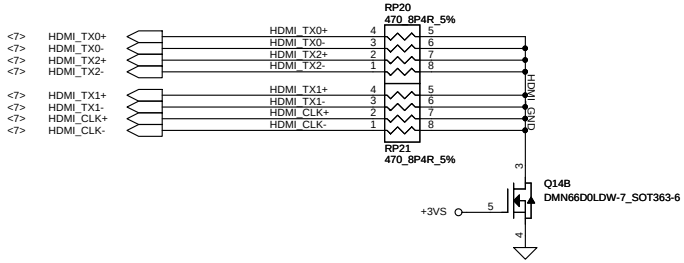


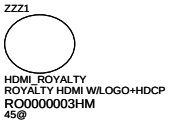
HDMI connector











Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: HDMI Conn

Size	Document Number	Rev
Custom	Z5WAW M/B LA-B702	0.2

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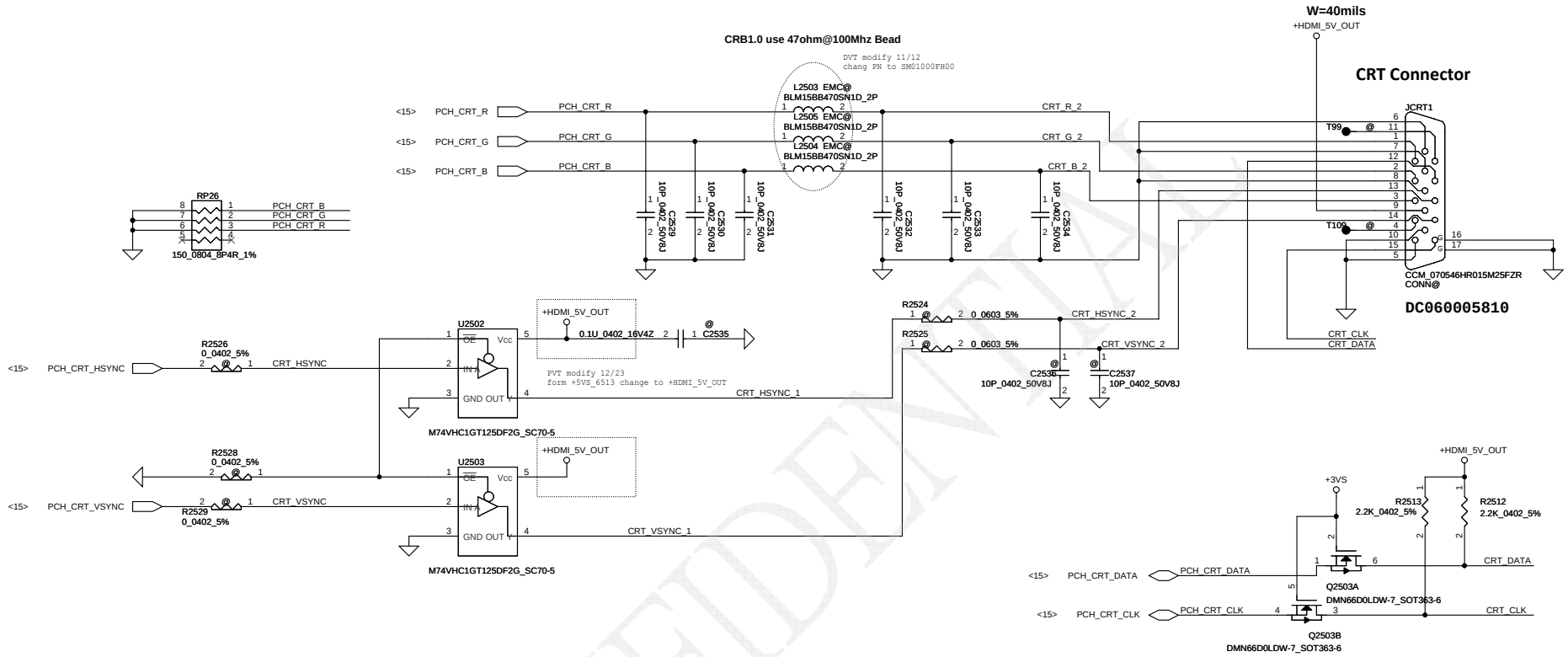
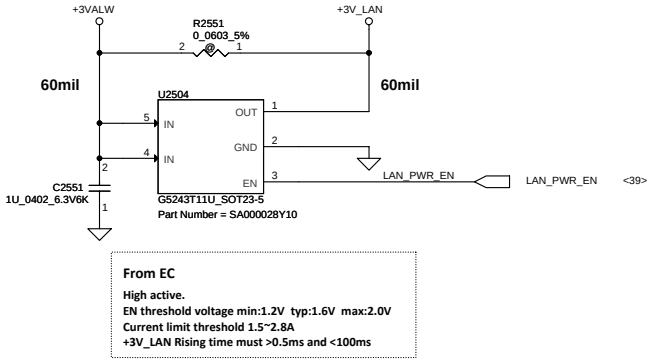
CRT conn.

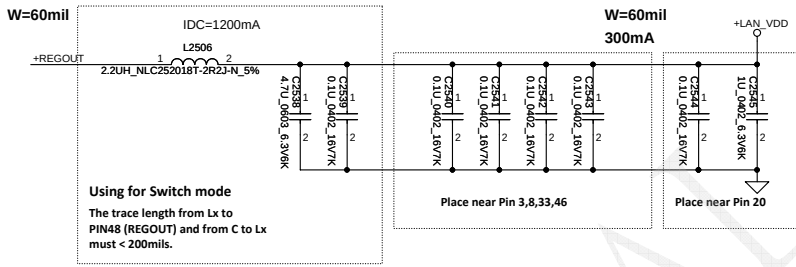


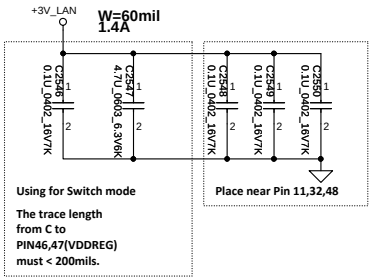
Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

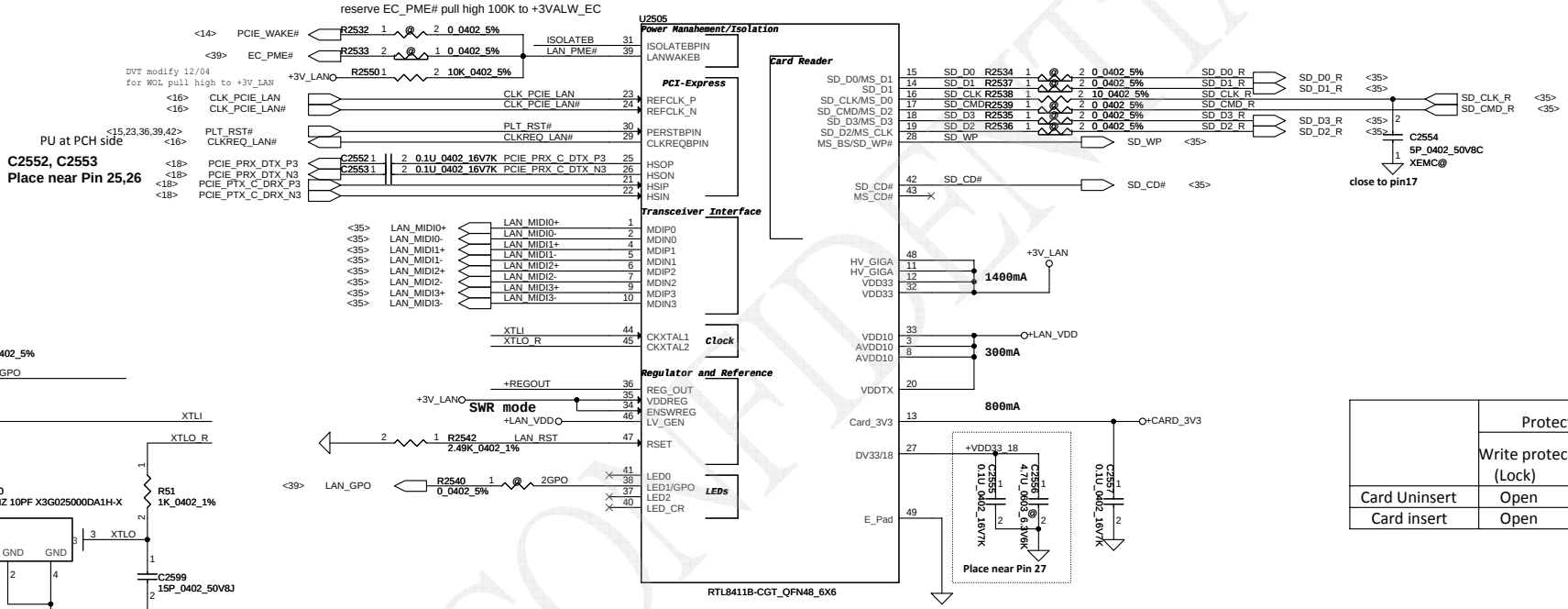
Compal Electronics, Inc.		
Title: CRT Connector		
Size: Custom	Document Number: Z5WAW M/B LA-B702	Rev: 0.2
Date: Tuesday, May 27, 2014	Sheet 33 of 56	

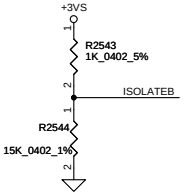
LAN-RTL8411B











	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

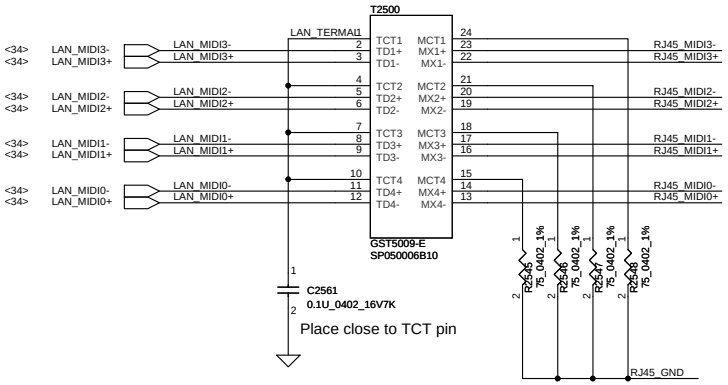
Compal Electronics, Inc.

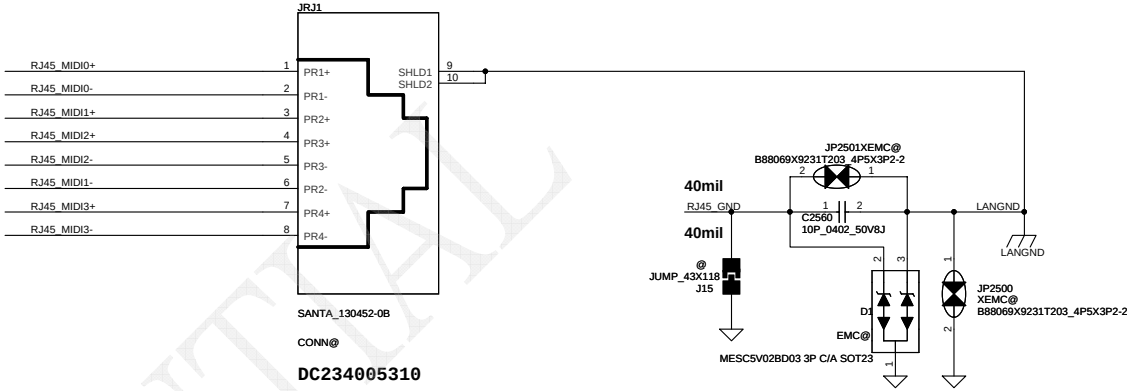
Title: LAN RTL8411-CG

Size: Custom | Document Number: Z5WAW M/B LA-B702 | Rev: 0.2

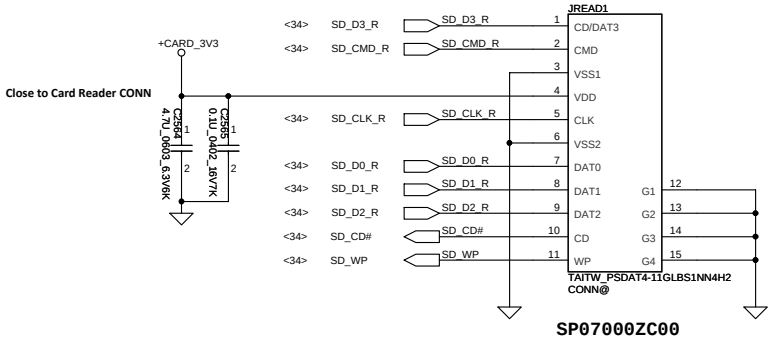
Date: Tuesday, May 27, 2014 | Sheet 34 of 56

RJ45 / Card Reader conn.





Card Reader Connector



Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: LAN RJ45/CR SD Connector

Size	Document Number	Rev
Custom	Z5WAW M/B LA-B702	0.2

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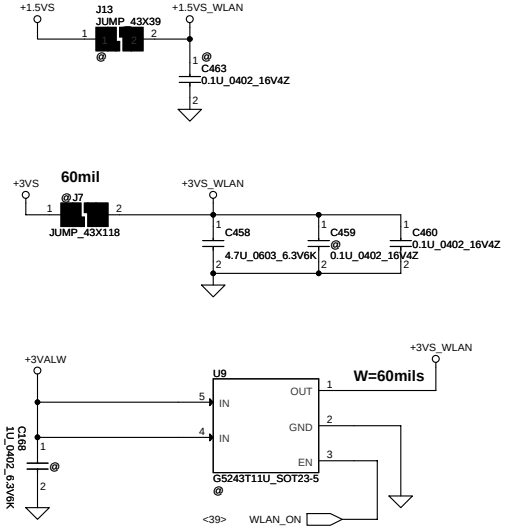
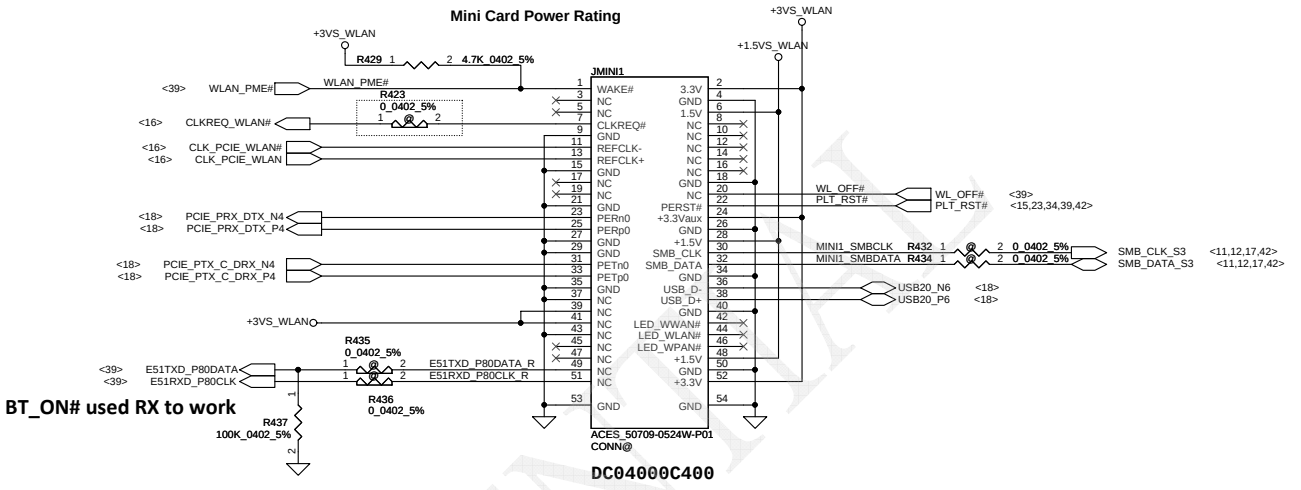
Wireless LAN





Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

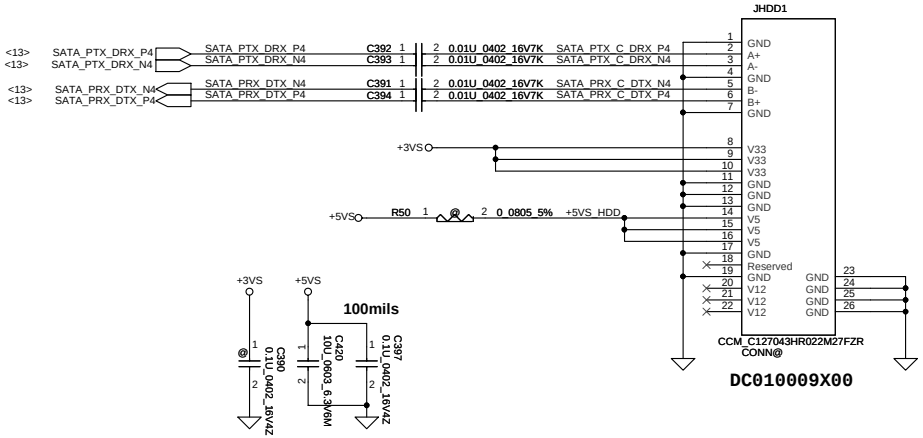
Compal Electronics, Inc.

Title: MINI CARD (WLAN)

Size	Document Number	Rev
Custom	Z5WAW M/B LA-B702	0.2

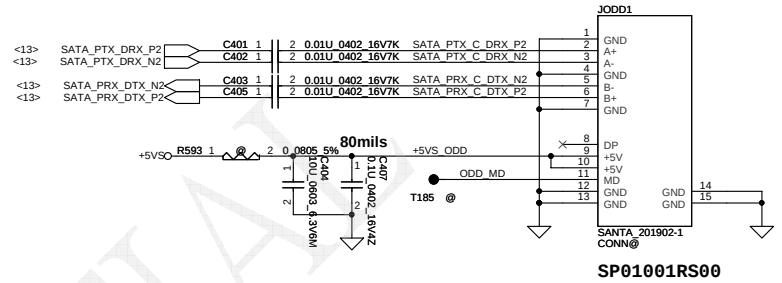
Date: Tuesday, May 27, 2014 | Sheet 36 of 56

SATA HDD1 Conn.



DC010009X00

SATA ODD Conn.



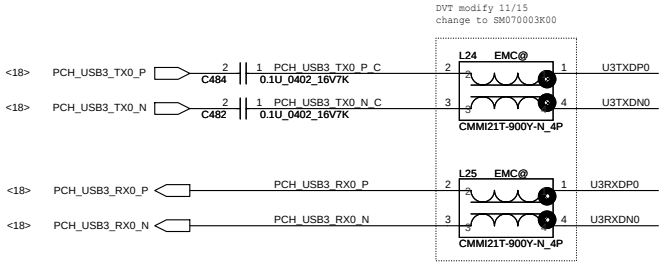
SP01001RS00

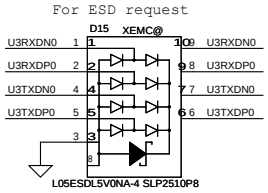
Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

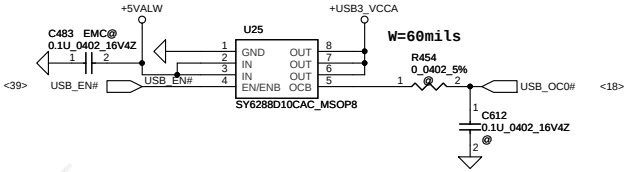
Compal Electronics, Inc.

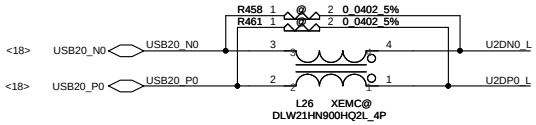
Title	HDD/ODD	
Size: Custom	Document Number: Z5WAW M/B LA-B702	Rev: 0.2
Date: Tuesday, May 27, 2014	Sheet 37 of 56	

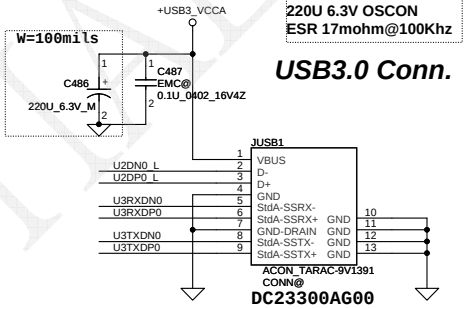
USB3.0 (Port 0)







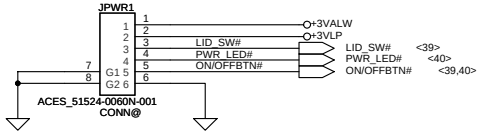




SF000006R00
220U 6.3V OSCON
ESR 17mohm@100Khz

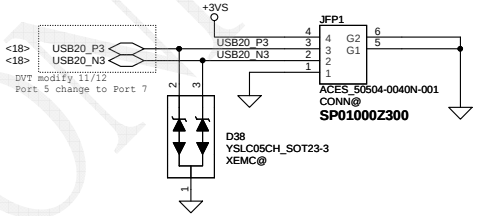
USB3.0 Conn.

PWR/B



SP010014M10

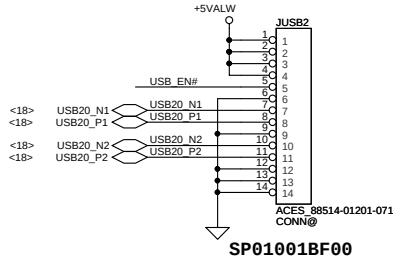
Finger Print /B for BA50



USB/B (USB Port 1, Port2)

USB/B Conn.

W=100mils



SP01001BF00

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: USB3.0 Conn/USB_B/PWR_B

Size	Document Number	Rev
Custom	Z5WAW M/B LA-B702	0.2

Date: Tuesday, May 27, 2014 | Sheet 38 of 56

C501 XEMC@ 22P_0402_50V8J
R477 33_0402_5%
CLK_PCI_EC

+3VALW_EC
R480 9012@ 47K_0402_5%
EC_RST#
C509 9012@ 0.1U_0402_16V4Z

9022: ECRST# is internally pull-up to VCC via 40Kohm resistor, so can remove external pull-up resistor and capacitor.

+3VALW_EC
R484 @ 100K_0402_5% EC_PME#

+3VALW_EC
RP22 2.2K_0804_8P4R_5%
EC_SMB_CK1
EC_SMB_DA1
EC_SMB_CK2
EC_SMB_DA2
+3VS

C511 EMC@ 0.01U_0402_16V7K PLT_RST#
ESD request

+3VS
R492 @ 10K_0402_5% EC_SMI# SCI#

9022:Change control method from push-pull to open-drain, so EC_SCI# must be pull high. *PU on PCH side
(Pull high in PCH side)

For abnormal shutdown

D27 RB751V-40 SOD-323
SPOK
PCH_RSMRST#
D26 RB751V-40 SOD-323 @
PCH_PWROK

+3VALW_EC
Board ID
Analog Board ID definition, Please see page 3.
Ra
R503 100K_0402_5%
AD_BID0
Rb
R506 27K_0402_1%
C517 @ 0.1U_0402_16V4Z

reserve for LVDS EP mode
R491 @ 10K_0402_5% EC_GPIO0D
DVT modify 11/18

+3VLP
R236 0_0805_5%
+3VALW_EC
DVT modify 11/12 change to SM010009U00
L31 BLM15BD121SN1D_2P
SM010030010 200ma 120ohm@100mhz DCR 0.2
+EC_VCCA
C502 C503 C504 C505 C506 C507 0.1U_0402_16V4Z 1000P_0402_50V7K XEMC@
C508 0.1U_0402_16V4Z
ECAGND <45>

U28
EC_VDD/VCC 9 22 36 111 125 67
EC_VDD/AVCC

LPC & MISC
<19> GATEA20 GATEA20/GPIO00 1
<19> KBRST# KBRST#/GPIO01 2
SERIRQ SERIRQ 3
<17,42> LPC_FRAME# LPC_FRAME# 4
<17,42> LPC_AD3 LPC_AD3 5
<17,42> LPC_AD2 LPC_AD2 7
<17,42> LPC_AD1 LPC_AD1 8
<17,42> LPC_AD0 LPC_AD0 10
<16> CLK_PCI_EC CLK_PCI_EC 12
<15,23,34,36,42> PLT_RST# PCIRST#/GPIO05 13
EC_RST# EC_RST# 37
<15,19> EC_SMI# SCI# EC_SCI#/GPIO0E 20
<36> WLAN_ON GPIO1D 38

PWM Output
GPIO0F 21 KBL_EN# KBL_EN# <40>
BEEP#/GPIO10 23 BEEP# BEEP# <41>
GPIO12 26 USB_EN# USB_EN# <38>
ACOFF/GPIO13 27 WLAN_PME# WLAN_PME# <36>

AD Input
BATT_TEMP/GPIO38 63 BATT_TEMP BATT_TEMP <44,45>
GPIO39 64 VCIN1_BATT_DROP VCIN1_BATT_DROP <45>
ADP_I/GPIO3A 65 ADP_I ADP_I <45,46>
GPIO3B 75 ADP_BID0
GPIO42 76
IMON/GPIO43
C510 2 100P_0402_50V8J ECAGND

DA Output
DAC_BRIG/GPIO3C 68
EN_DFAN1/GPIO3D 70 EN_DFAN1 EN_DFAN1 <42>
IREF/GPIO3E 71 TP_PWR_EN TP_PWR_EN <40>
CHGVADJ/GPIO3F 72 TP_SENOFF# TP_SENOFF# <40>

PS2 Interface
EC_MUTE#/GPIO4A 83 EC_MUTE# EC_MUTE# <41>
USB_EN#/GPIO4B 84 LAN_PWR_EN LAN_PWR_EN <34>
CAP_INT#/GPIO4C 85 EC_I2C_TPCLK R131 2.2K_0402_5% EC_SCLK1_TP <40>
EAPD/GPIO4D 86 EC_I2C_TPDAT R137 2.2K_0402_5% EC_SDATA1_TP <40>
TP_CLK/GPIO4E 87 TP_CLK TP_CLK <40>
TP_DATA/GPIO4F 88 TP_DATA TP_DATA <40>

Int. K/B Matrix
<40> KSI[0..7] KSI[0..7]
<40> KSO[0..17] KSO[0..17]
KSI0 55 KSI0/GPIO30
KSI1 56 KSI1/GPIO31
KSI2 57 KSI2/GPIO32
KSI3 58 KSI3/GPIO33
KSI4 59 KSI4/GPIO34
KSI5 60 KSI5/GPIO35
KSI6 61 KSI6/GPIO36
KSI7 62 KSI7/GPIO37
KSO0 39 KSO0/GPIO20
KSO1 40 KSO1/GPIO21
KSO2 41 KSO2/GPIO22
KSO3 42 KSO3/GPIO23
KSO4 43 KSO4/GPIO24
KSO5 44 KSO5/GPIO25
KSO6 45 KSO6/GPIO26
KSO7 46 KSO7/GPIO27
KSO8 47 KSO8/GPIO28
KSO9 48 KSO9/GPIO29
KSO10 49 KSO10/GPIO2A
KSO11 50 KSO11/GPIO2B
KSO12 51 KSO12/GPIO2C
KSO13 52 KSO13/GPIO2D
KSO14 53 KSO14/GPIO2E
KSO15 54 KSO15/GPIO2F
KSO16 81 KSO16/GPIO48
KSO17 82 KSO17/GPIO49

SPI Device Interface
CPU1.5V_S3_GATE/GPXIOA00 97 VGATE VGATE <14,51>
WOL_EN/GPXIOA01 98 GPU_ALERT GPU_ALERT <23>
HDA_SDO/GPXIOA02 99 ME_FLASH ME_FLASH <13>
VCIN0_PH/GPXIOD00 109 VCIN0_PH_R

SPI Flash ROM
Reserve for Share ROM EC
SPIDI/GPIO5B 119 EC_SPI_SI EC_SPI_SI <17>
SPIDO/GPIO5C 120 EC_SPI_SO EC_SPI_SO <17>
SPICLK/GPIO5B 126 EC_SPI_CLK EC_SPI_CLK <17>
SPICS#/GPIO5A 128 EC_SPI_CS# EC_SPI_CS# <17>

GPIO
R691 2 100K_0402_5%
ENBKL/GPIO40 73 ENBKL ENBKL <15>
PECI_KB930/GPIO41 74 GPU_OVERT GPU_OVERT <23>
FSTCHG/GPIO50 89 EC_I2C_ALERT#
BATT_CHG_LED#/GPIO52 90 BATT_BLUE_LED# BATT_BLUE_LED# <40>
CAPS_LED#/GPIO53 91
PWR_LED#/GPIO54 92 PWR_LED PWR_LED <40>
BATT_LOW_LED#/GPIO55 93 BATT_AMB_LED# BATT_AMB_LED# <40>
SYSON/GPIO56 95 SYSON SYSON <43,48>
VR_ON/GPIO57 121 VR_ON VR_ON <51>
PM_SLP_S4#/GPIO59 127
R1683 @ 0_0402_5%
TP_I2C_INT# <40>

SM Bus
<45,46> EC_SMB_CK1 EC_SMB_CK1 77
<45,46> EC_SMB_DA1 EC_SMB_DA1 78
<17,23,30> EC_SMB_CK2 EC_SMB_CK2 79
<17,23,30> EC_SMB_DA2 EC_SMB_DA2 80
EC_SMB_CK1/GPIO44
EC_SMB_DA1/GPIO45
EC_SMB_CK2/GPIO46
EC_SMB_DA2/GPIO47

GPIO
<14> PM_SLP_S3# PM_SLP_S3# 6
<14> PM_SLP_S5# PM_SLP_S5# 14
15
<23> DGPU_AC_DETECT DGPU_AC_DETECT 16
TS_EN TS_EN 17
<31> EC_GPIO0D 18
<36> WL_OFF# WL_OFF# 19
<47> SPOK SPOK 25
FAN_SPEED1 28
<42> FAN_SPEED1 EC_PME# 29
<34> EC_PME#
<36> E51TXD_P80DATA E51TXD_P80DATA 30
<36> E51RXD_P80CLK E51RXD_P80CLK 31
<14> PCH_PWROK PCH_PWROK 32
<40> PWR_SUSP_LED# PWR_SUSP_LED# 34
<13> EC_RTCRST# EC_RTCRST# 36
PM_SLP_S3#/GPIO04
PM_SLP_S5#/GPIO07
EC_SMI#/GPIO08
GPIO0A
GPIO0B
GPIO0C
GPIO0D
EC_INVT_PWM/GPIO11
FAN_SPEED1/GPIO14
EC_PME#/GPIO15
EC_TX/GPIO16
EC_RX/GPIO17
PCH_PWROK/GPIO18
SUSP_LED#/GPIO19
NUM_LED#/GPIO1A

GPO
EC_RSMRST#/GPXIOA03 100 PCH_RSMRST# PCH_RSMRST# <14>
EC_LID_OUT#/GPXIOA04 101
PROCHOT_IN/GPXIOA05 102 VCIN1_PROCHOT
H_PROCHOT#_EC/GPXIOA06 103 H_PROCHOT#_EC H_PROCHOT#_EC <45>
VCOUT0_PH/GPXIOA07 104 MAINPWON MAINPWON <45,47>
BKOFF#/GPXIOA08 105 BKOFF# BKOFF# <31>
PBTN_OUT#/GPXIOA09 106 PBTN_OUT# PBTN_OUT# <14>
PCH_APWROK/GPXIOA10 107 PCH_PWR_EN PCH_PWR_EN <43>
SA_PGOOD/GPXIOA11 108

GPI
AC_IN/GPXIOD01 110 EC_ACIN
EC_ON/GPXIOD02 112 EC_ON EC_ON <47>
ON/OFF/GPXIOD03 114 ON/OFFBTN# ON/OFFBTN# <38,40>
LID_SW#/GPXIOD04 115 LID_SW# LID_SW# <38>
SUSP#/GPXIOD05 116 SUSP# SUSP# <43,48,49,50>
GPXIOD06 117 SYS_PWROK_EC SYS_PWROK_EC <14>
PECI_KB9012/GPXIOD07 118 9012_PECI

<34> LAN_GPO LAN_GPO 122
<14> PM_SLP_S4# PM_SLP_S4# 123
XCLKI/GPIO5D
XCLKO/GPIO5E

V18R 124 +V18R
R507 9022@ 0_0402_5% +3VALW_EC
C515 4.7U_0603_6.3V6K 9012@

GND/GND 11 24 34 94 113
AGND/AGND 69
9022@ KB9022QC-A3_LQFP128_14X14
20mil L32 BLM15BD121SN1D_2P
ECAGND 1 2
SM010030010 200ma 120ohm@100mhz DCR 0.2
DVT modify 11/12 change to SM010009U00

EC_RTCRST# R490 1 2 10K_0402_5%

U28
KB9012QF-A3_LQFP128_14X14
9012@
SA00004OB30

LID_SW# R476 100K_0402_5% +3VALW_EC
0326 PU +TP_VCC at TP side
TP_CLK R485 @ 4.7K_0402_5%
TP_DATA R483 @ 4.7K_0402_5% +3VS
EC_MUTE# R481 @ 10K_0402_5% +3VS
GPU_ALERT R486 10K_0402_5% +3VS
GPU_OVERT R487 10K_0402_5% +3VS
9012_PECI R498 43_0402_5% H_PECI <5>

R509 0_0402_5%
ACIN <14,44,46>
EC_ACIN C512 100P_0402_50V8J

KB9022&9012 Co-Layout Item
R499 0_0402_5%
H_PROCHOT# EC 9022@
<51> VR_HOT# R496 0_0402_5%
H_PROCHOT# <44,5>
H_PROCHOT# EC
Q50 L2N7002LT1G_SOT23-3 9012@
Latest design guide suggest change to 74LVC1G06.

+3VALW_EC
R697 @ 10K_0402_5%
R696 @ 10K_0402_5%
R501 0_0402_5%
VCIN0_PH_R
VCIN1_PROCHOT
VCIN0_PH <45>
VCIN1_PROCHOT <45>
PU will disable PH function

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

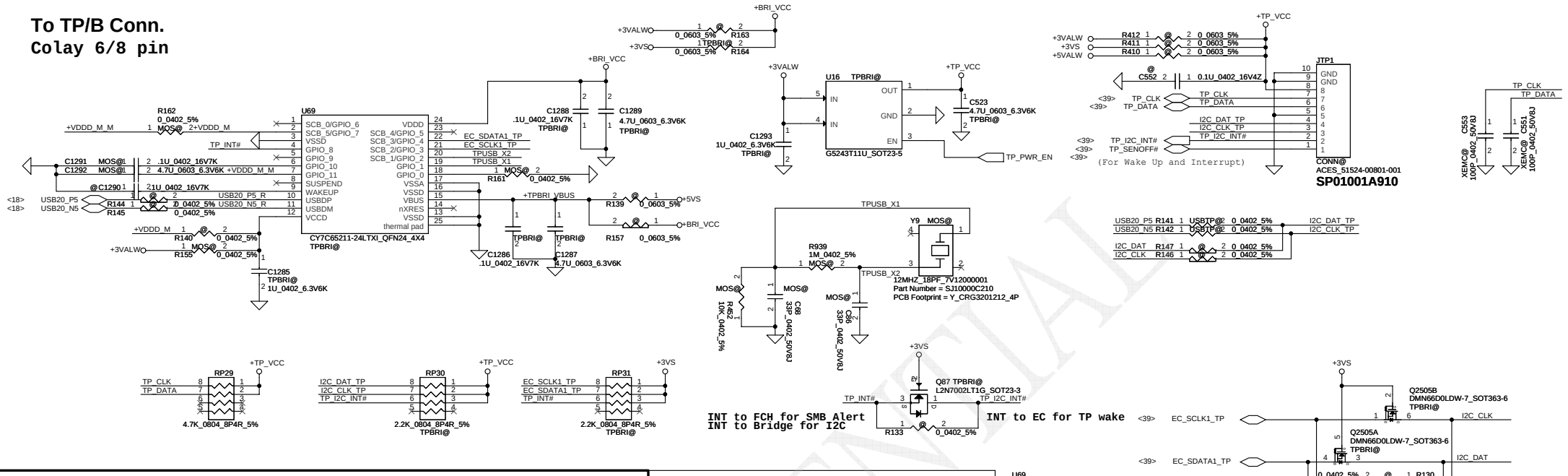
Compal Electronics, Inc.

Title: EC ENE-KB9012

Size: Custom | Document Number: Z5WAW M/B LA-B702 | Rev: 0.2

Date: Wednesday, May 28, 2014 | Sheet 39 of 56

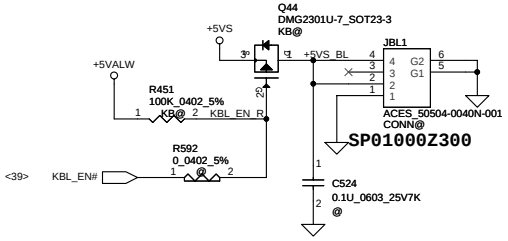
To TP/B Conn.
Colay 6/8 pin



INT to FCH for SMB_Alert
INT to Bridge for I2C

INT to EC for TP wake

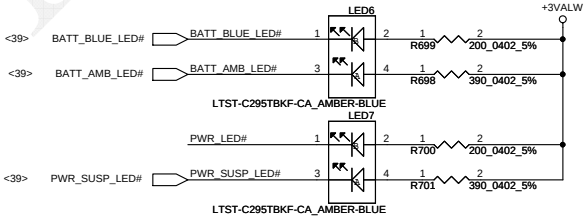
KB BackLight Conn. Reserve

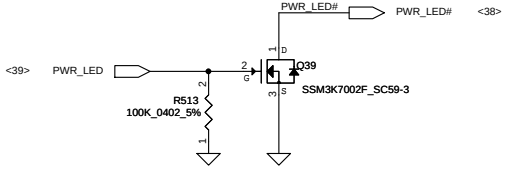


NOTE :
Cypress pop : TPBRI@
MOSART pop : TPBRI@ , MOS@ (default flash type)
EC I2C pop : R128,R129,R132,RP19
USBTP pop : USBTP@, (Q87 or R132, R130 option)

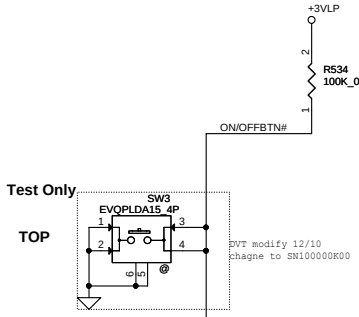
U69
MOSART Bridge
SA00007PR00
MOS@

LED

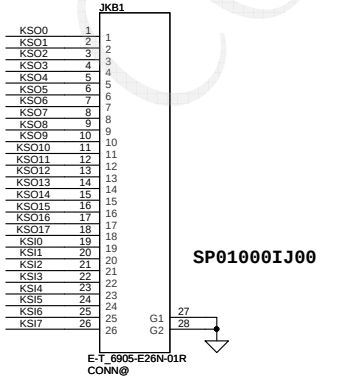




ON/OFF BTN



KB Conn.



Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: KB & TP & TPM Connector & LED

Size	Document Number	Rev
Custom	Z5WAW M/B LA-B702	0.2

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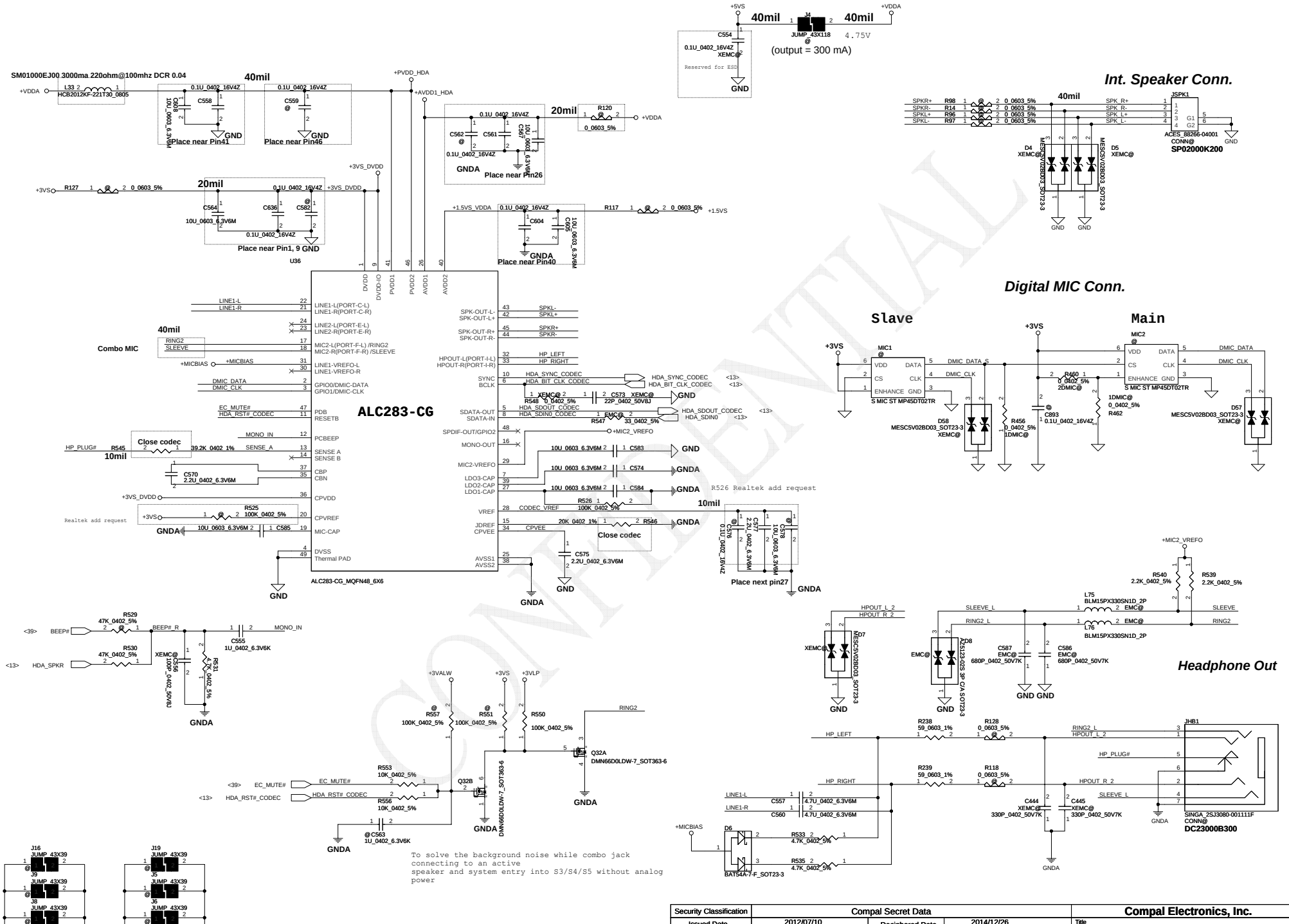
HD Audio Codec



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/07/10	Deciphered Date	2014/12/26
Title	HD Audio Codec ALC283		
Size C	Document Number Z5WAW M/B LA-B702		Rev 0.2
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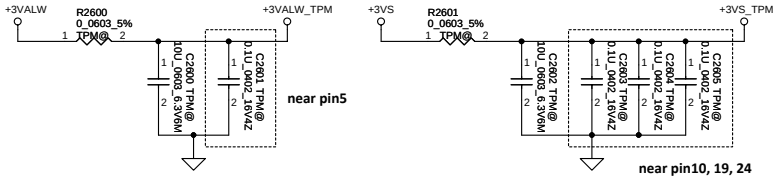
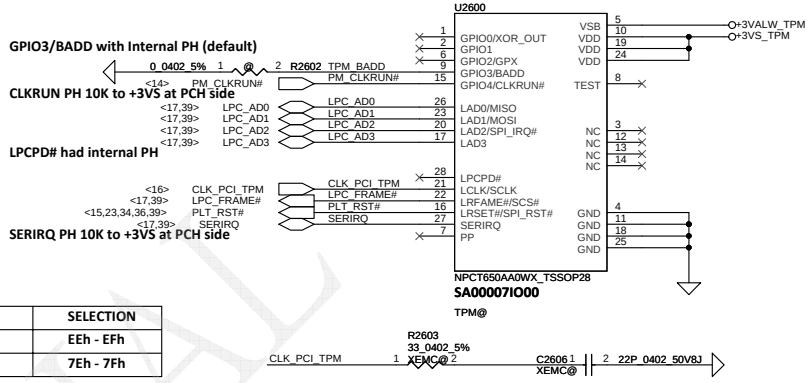
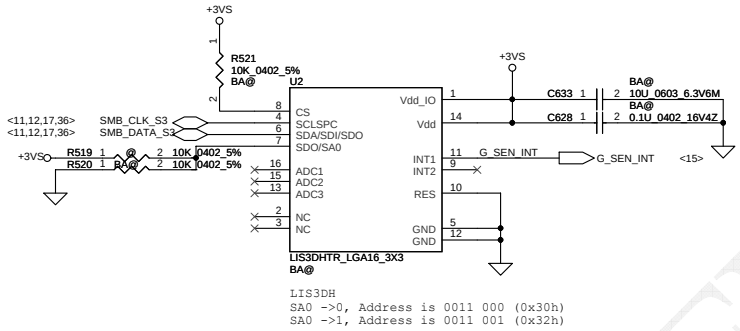
TPM Board for 2015



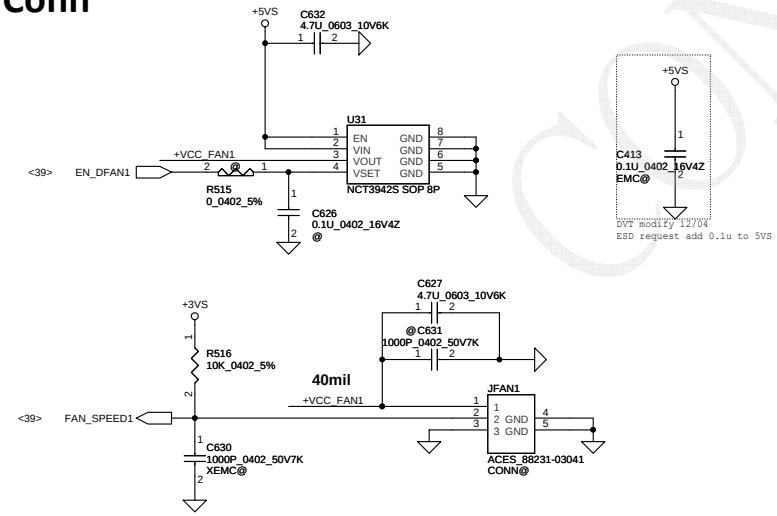


BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh

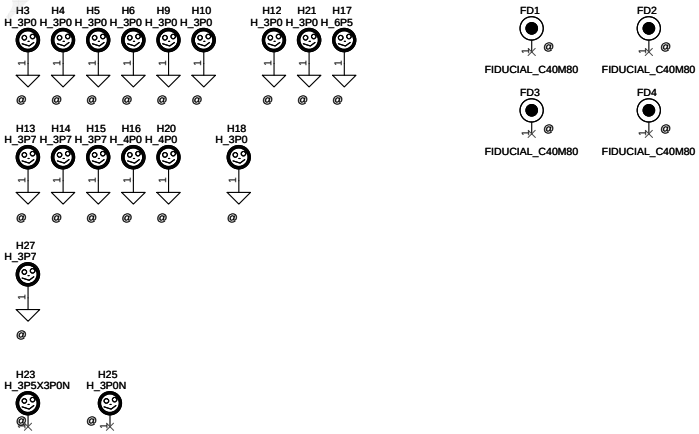
G-Sensor for BA50



FAN1 Conn



Screw Hole



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/12/26	Deciphered Date	2014/12/26	Title: FAN & Screw Hole & G-Sensor
Size: Custom	Document Number: Z5WAW M/B LA-B702			Rev: 0.2
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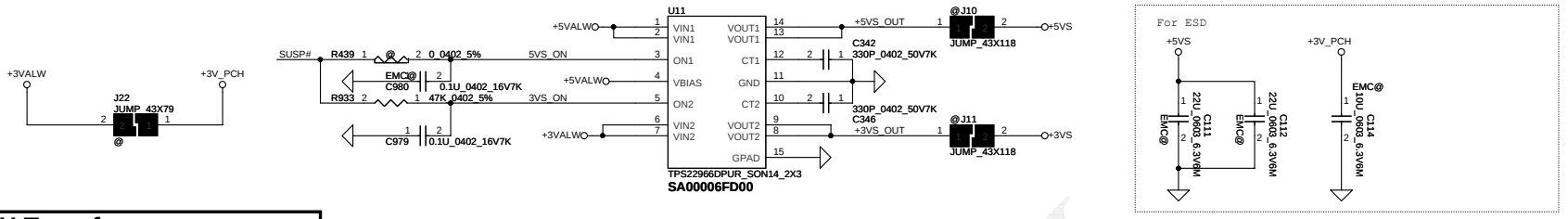
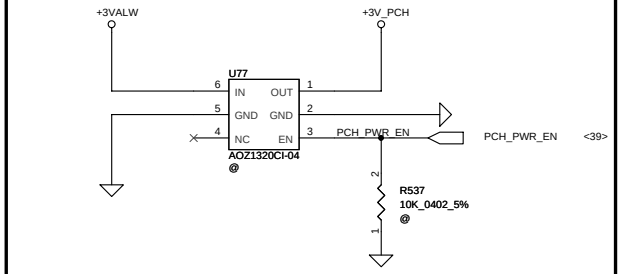
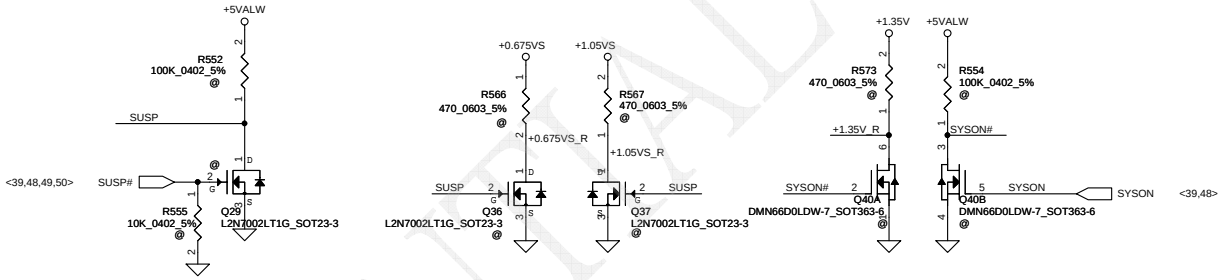
DC & VGA Interface

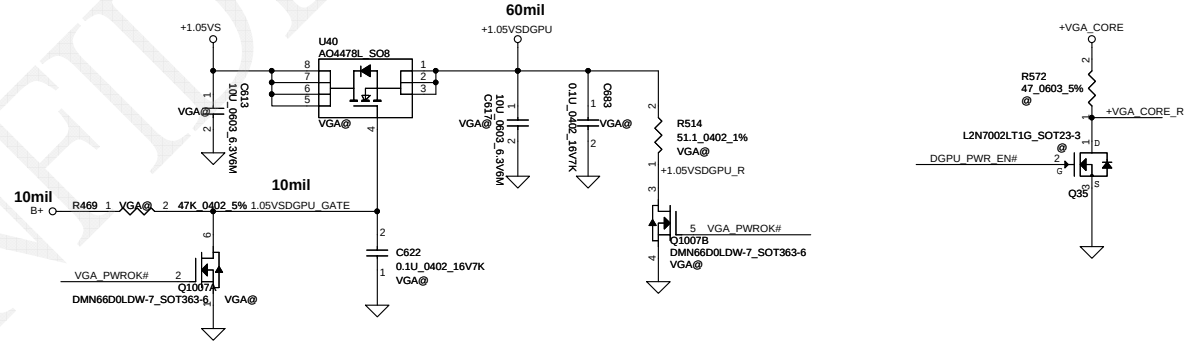


+3VALW to +3V_PCH Transfer

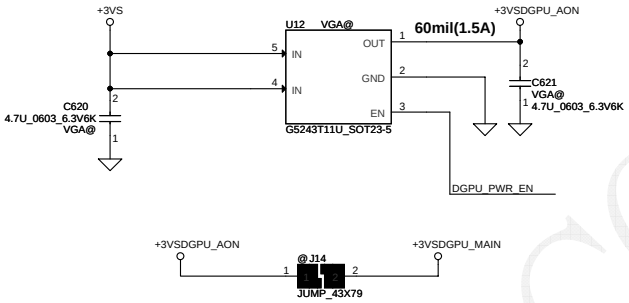




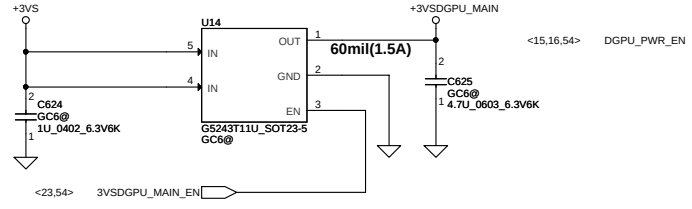
+1.05VS to +1.05VSDGPU



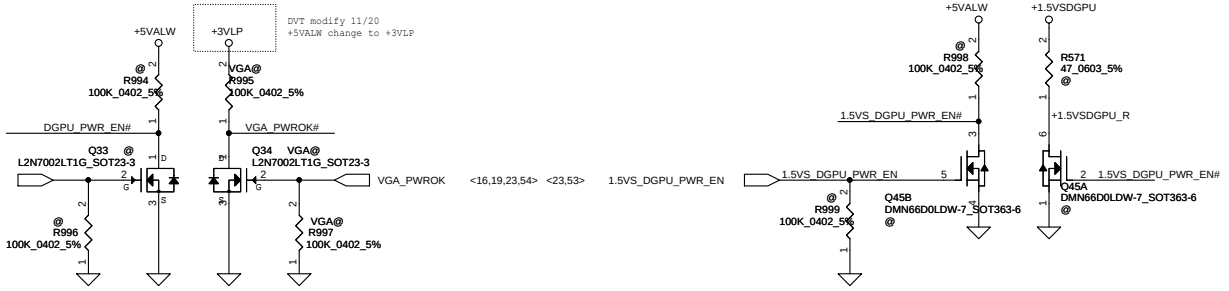
+3VS to +3VSDGPU_AON for GPU



+3VS to +3VSDGPU_MAIN for GC6-2.0



3VSDGPU_MAIN_EN From GPU



Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: DC Interface

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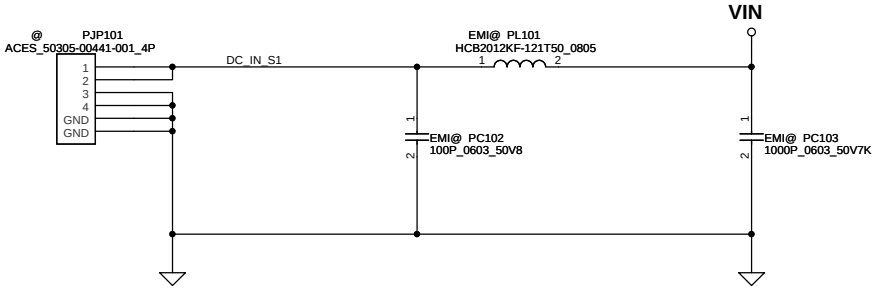

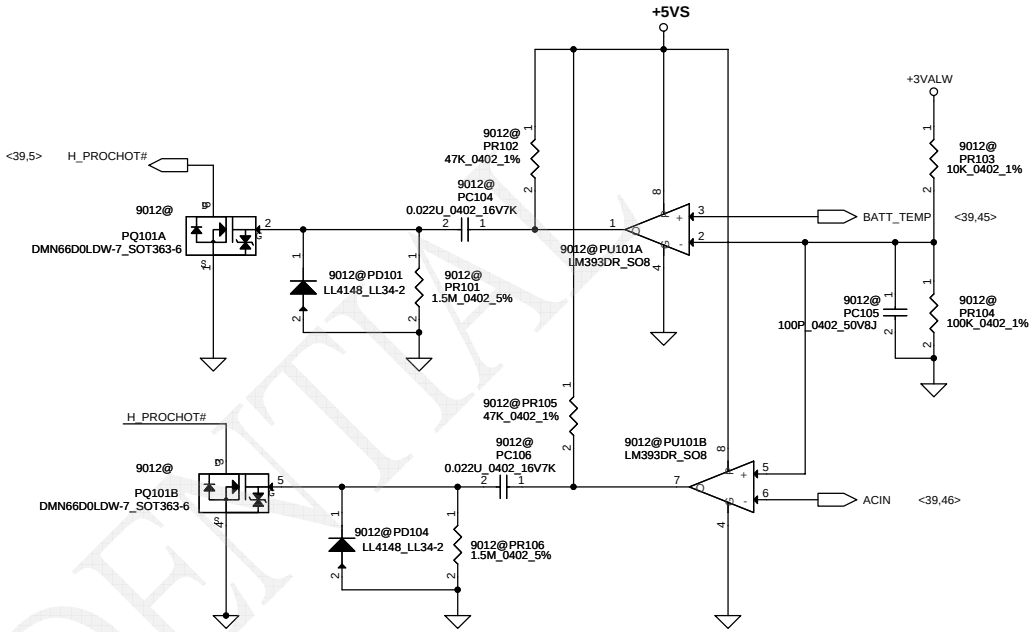

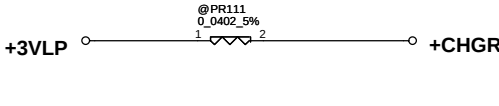

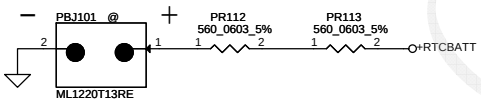

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: ***DCIN***

Size	Document Number	Rev
Custom		0.1

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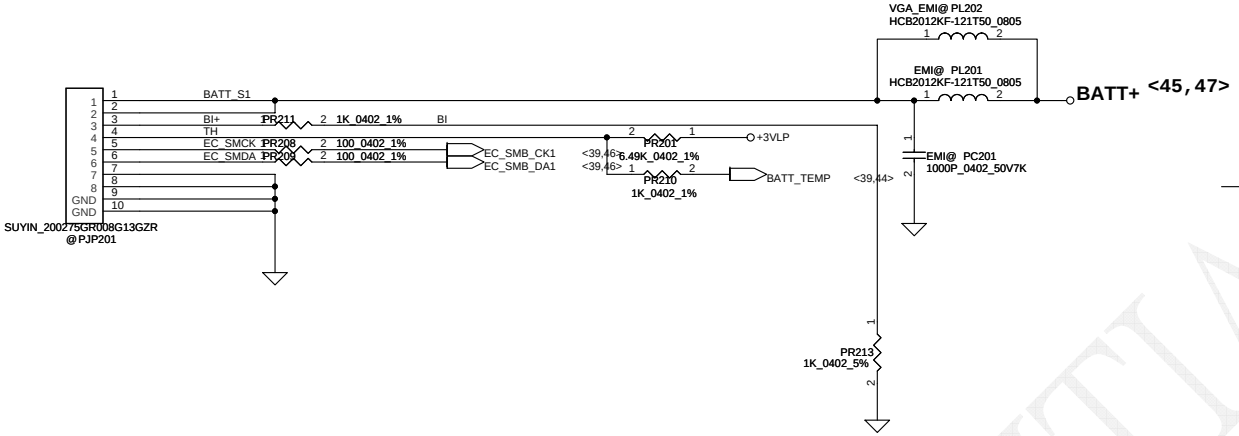
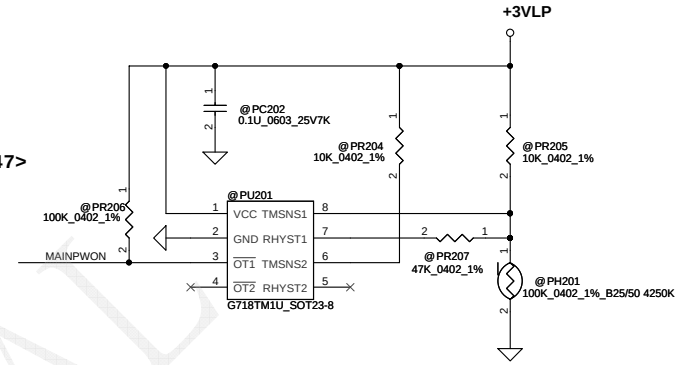
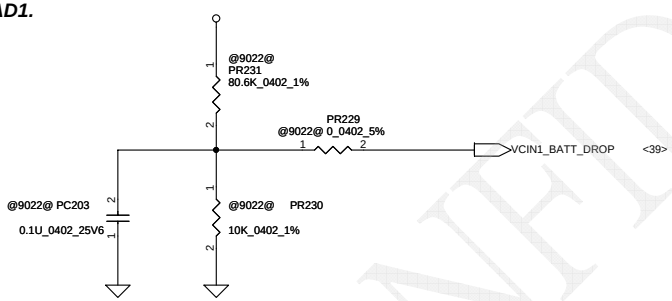




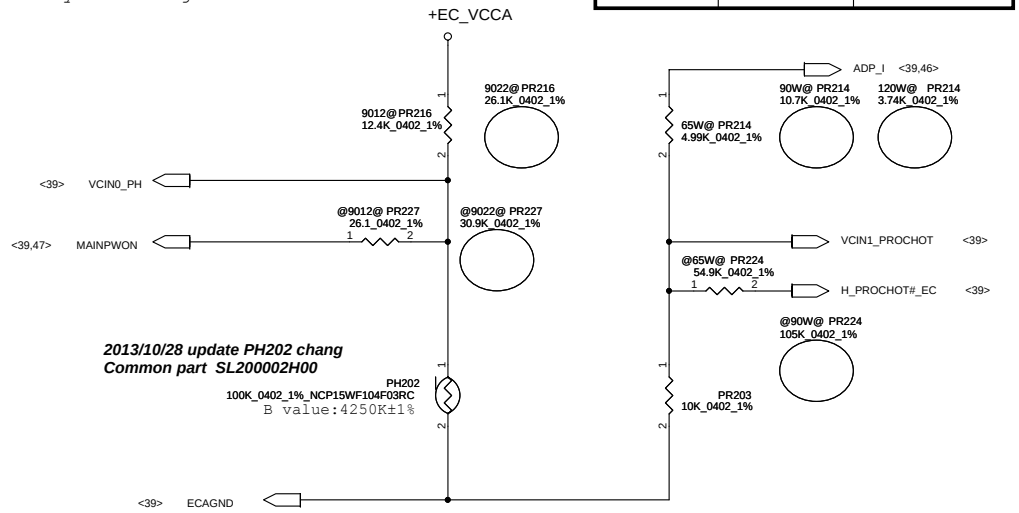
2013/10/02
Add for ENE9022 Battery Voltage drop detection. B+
Connect to ENE9022 pin64 AD1.

Battery is 3-cell design.
B+=9V



PH202 under CPU botton side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C

For KB9012 sense 20mΩ	Active	Recovery
65W	85W, 1.2V	65W, 0.913V
90W	117W, 1.2V	90W, 0.915V
120W	156W, 1.2V	120W, 0.919V



Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: ***BATTERY CONN / OTP***

Size	Document Number	Rev
Custom		0.1

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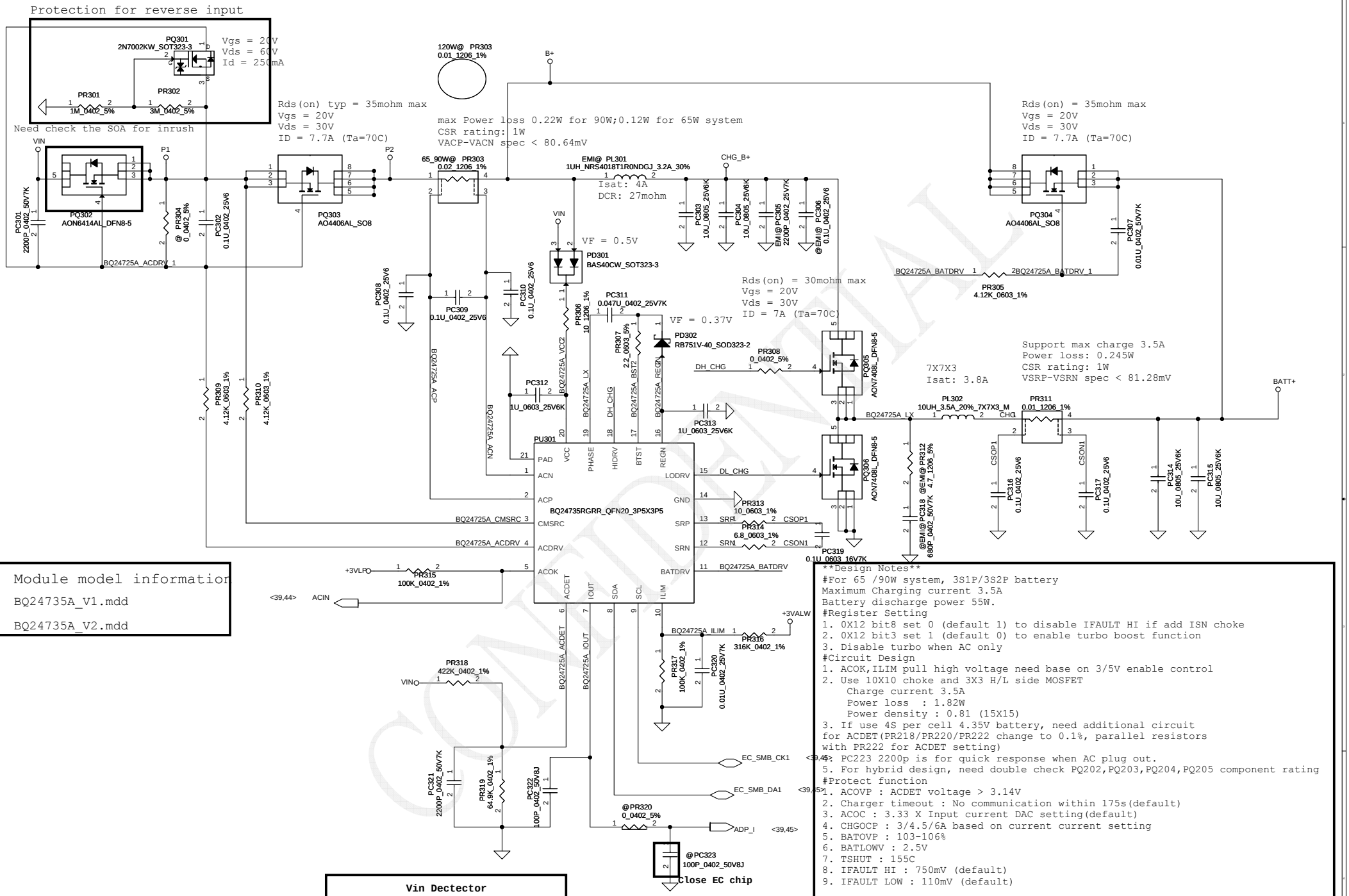

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
	Common Circuit	0.1

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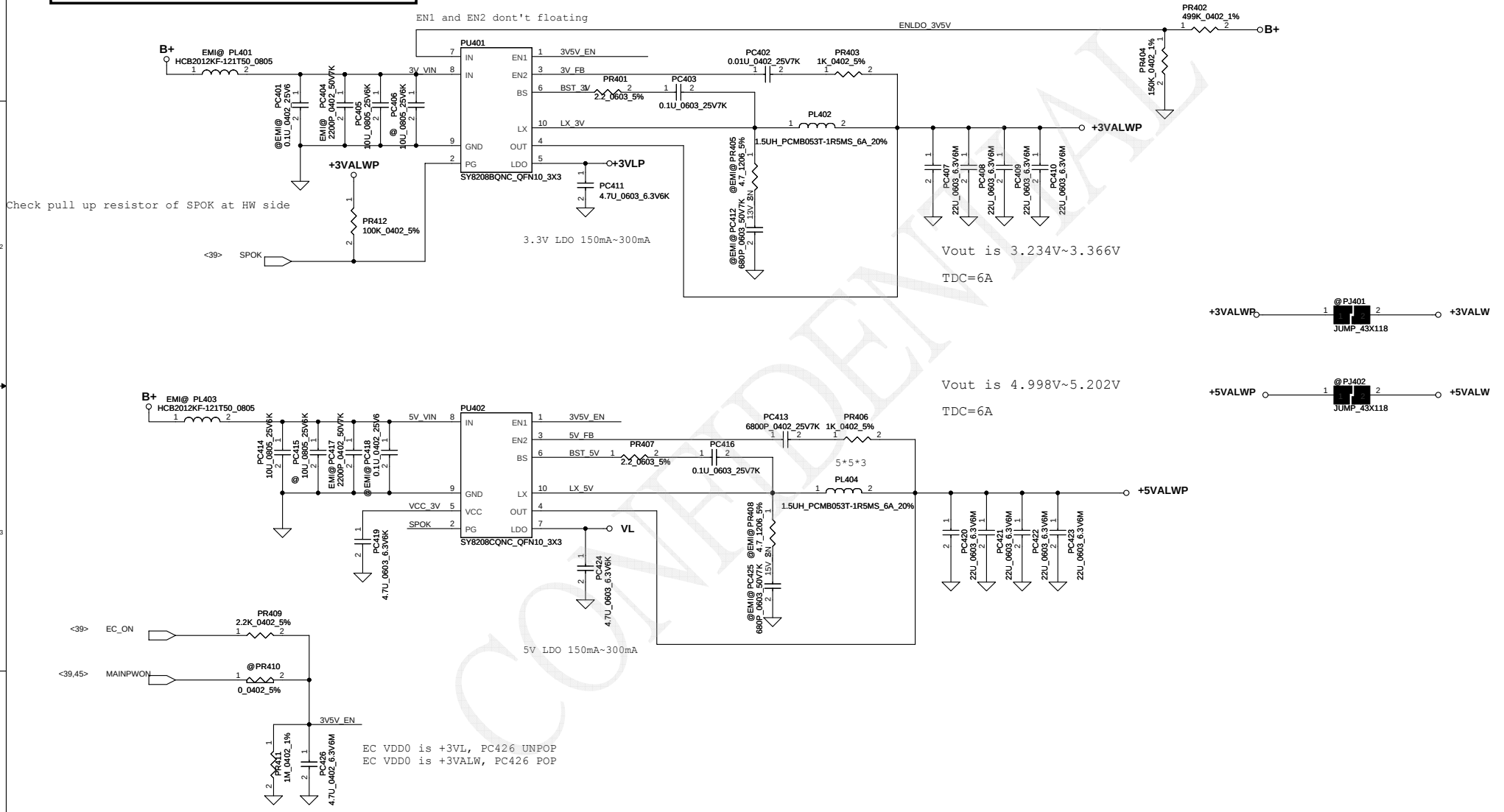
Module model information

SY8208B_V2.mdd

SY8208C_V2.mdd



Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

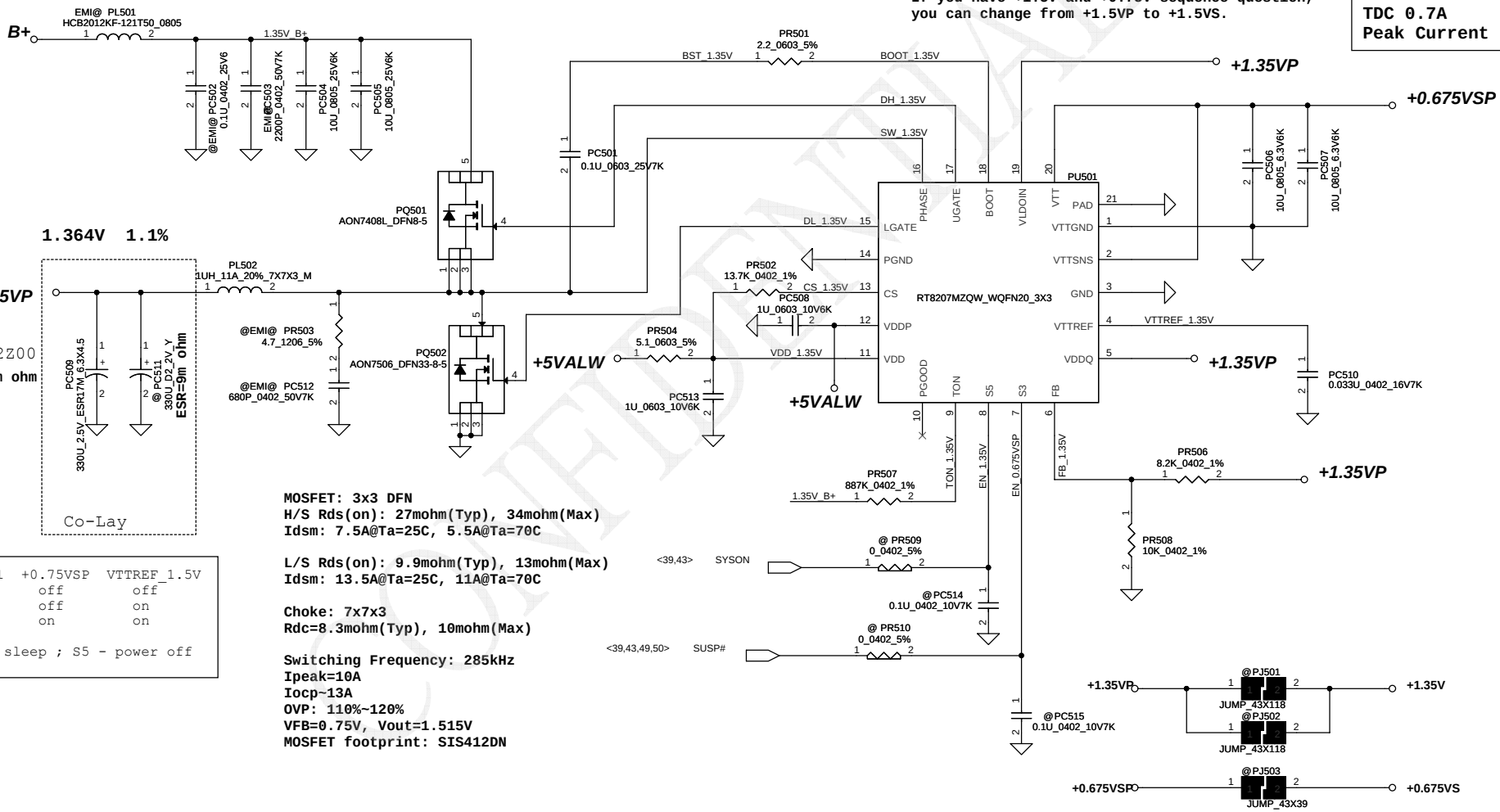
Compal Electronics, Inc.			
Title: +3VALW/+5VALW			
Size: Custom	Document Number		Rev: 0.1
Date: Tuesday, May 27, 2014	Sheet 47 of 56		

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
VFB=0.75V, Vout=1.515V
MOSFET footprint: SIS412DN

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: +1.35VP/+0.675VSP

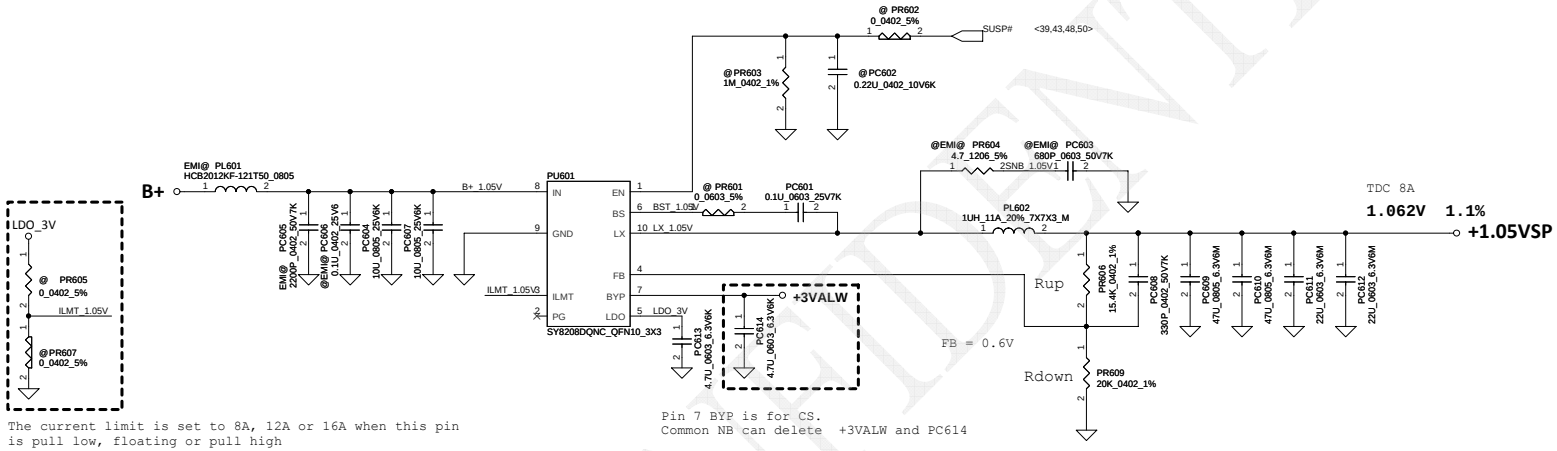
Size: Custom | Document Number | Rev: 0.1

Date: Tuesday, May 27, 2014 | Sheet 48 of 56

Module model information

SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR603



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC614

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)

Vout=1.05V

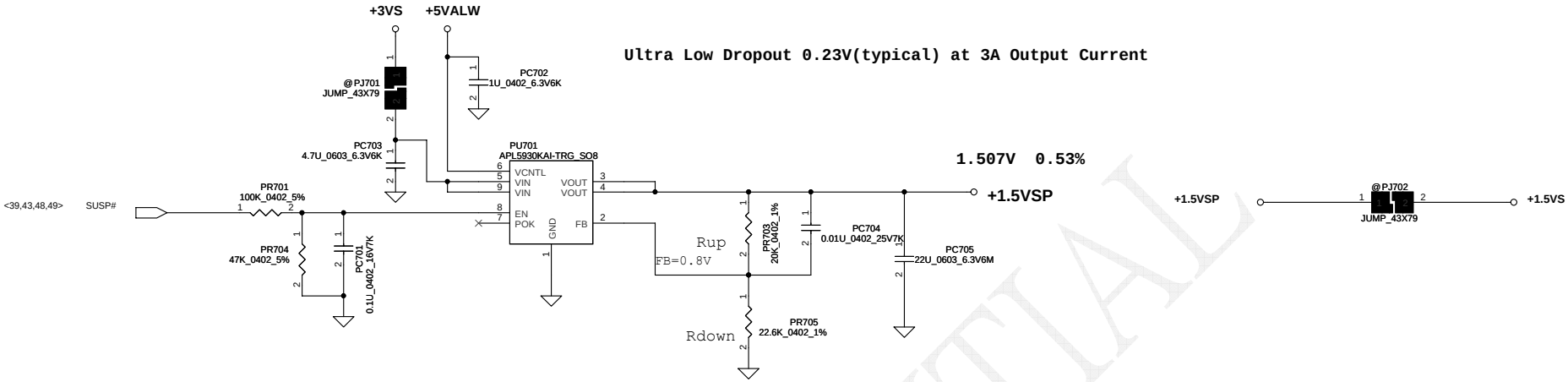
Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: +1.05VSP

Size	Document Number	Rev
C		0.1

Date: Tuesday, May 27, 2014 Sheet 49 of 56



Ultra Low Dropout 0.23V(typical) at 3A Output Current

Vout=0.8V* (1+Rup/Rdown)

Ultra Low Dropout 0.23V(typical) at 3A Output Current

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: ***+1.5VSP***

Size: Custom | Document Number | Rev: 0.1

Date: Tuesday, May 27, 2014 | Sheet 50 of 56

Module design of ISL95812 VR
For 47W/37W processor

PROG1(PR810) set 102K ohm to IccMAX 3 phase 84A/ 2 phase 56A
PROG2(PR805) set 49.9K ohm to Vboot 1.7V / 600KHz
PROG3(PR808) set 3.24K ohm to 12mV/us (2-ch CCM)

+VCCIO_OUT
PR801 130_0402_1%
PC801 1U_0402_6.3V6K
PR804 54.9_0402_1%
<9> VR_SVID_DAT
<9> VR_SVID_ALRT#
<9> VR_SVID_CLK
PR805 49.9K_0402_1%
PR808 3.24K_0402_1%
PR810 102K_0402_1%
VR_ON
@ PR809 0_0402_5%
+3VS
PR815 1.91K_0402_1%
<39> VGATE
PC809 680P_0402_50V7K
PR818 97.6K_0402_1%
<39> VR_HOT#
Place close to phase 1 MOSFET
PH801 470K_0402_5%_B25/50 4700K
NTC_PH2
PR819 5.62K_0402_1%
PC809 47P_0402_50V8J
PR821 27.4K_0402_1%
PR822 6.04K_0402_1%

VRHOT Assert Threshold : 0.92V
TSENSE Bias Current : 60uA
PH801=17.926K, 100C active
Reset Threshold: 0.96V, 94C active
100C Assert Threshold: PR821=27.4K
110C Assert Threshold: PR821=66.5K

PU801 ISL95812HRZ-T_QFN32_4x4
SCLK VR_ON PGOOD IMON VR_HOT# NTC COMP FB PAD
VR_EN
SDA ALERT#
SLOPE/PROG1 PROG3 PROG2 BOOT2 UGATE2 PHASE2
LGATE2 VDDP PWM3 LGATE1 PHASE1 UGATE1 BOOT1 VIN
FB2/VSEN FB/VSEN ISEN2 ISEN1 RTN ISUMN ISUMP VDD

@PR816 0_0402_5%
PC807 1U_0603_10V6K
37W: INSTALL
47W: @
37W@ PR817 0_0402_5%
@ PR820 0_0402_5%
PC810 0.22U_0603_25V7K
PR824 1_0402_5%
+5VS
PC814 1U_0603_10V6K

PR825 1K_0402_1%
PC815 220P_0402_50V7K FB_PR1040
37W: PR829=1.65K
47W: PR829=2.55K
47W@ PR829 2.55K_0402_1%
PR832 1.82K_0402_1%
PC819 56P_0402_50V8J
PR833 2K_0402_1%
37W@ PR829 1.65K_0402_1%
PC820 8200P_0402_25V7K
PC821 330P_0402_50V7K
PC816 2200P_0402_25V7K
47W@ PR830 511_0402_1%
PR834 1.5K_0402_1%
37W: PR830=470
47W: PR830=511
37W@ PR830 470_0402_1%
PR822 set 6.04K ohm to slope
PR830 set 665 ohm to OCP 102A
PR829 set 2.55K ohm to LL 1.5m

47W@ PC822 0.15U_0402_10V
37W: PC822=0.10U
47W: PC822=0.15U
37W@ PC822 0.1U_0402_10V7K
PC824 0.1U_0603_25V7K
@ PC830 0.033U_0603_16V7K
PR838 0_0402_5%
PR841 11K_0402_1%
PH802 10K_0402_5%_ERTJ0ER103J
PR845 2.61K_0402_1%
Place close to phase 1 inductor
ISUMP
ISUMN

ISEN3
ISEN2
ISEN1
PC831 0.022U_0402_25V7K
PC832 0.022U_0402_25V7K
ISUMN
47W@ PC833 0.022U_0402_25V7K
PC836 0.1U_0402_16V7K
<9> VCCSENSE
@ PC834 330P_0402_50V7K
PC837 @ 0.082U_0402_16V7K
PC838 0.01U_0402_25V7K
<10,9> VSSSENSE

Local sense put on HW site

+5VS
47W@ PU802
VCC UGATE FCCM BOOT PWM PHASE GND LGATE TP
ISL6208BCRZ-T_QFN8_2X2
PWM3
UGATE3
BOOT3
CPU_PHASE3
LGATE3
47W@ PC803 1U_0603_10V6K
47W@ PR802 2.2_0603_5%
47W@ PC802 0.22U_0603_25V7K
47W@ PR803 0_0603_5%
47W@ PQ802 AON6552_DFN5X6-8-5
47W@ PQ804 AON6554_DFN5X6-8-5
@EMI@ PR806 4.7_1206_5%
@EMI@ PC806 680P_0603_50V7K
SNB_CPU_P3
47W@ PR811 3.65K_0603_1%
47W@ PL802 0.22UH 20% PCME064T-R22MS0R985 28A
+CPU_CORE
P3_SW P3_VO
47W@PR807 100K_0603_1%
ISEN3
@47W@ PR813 100K_0402_1%
@47W@ PR814 100K_0402_1%
47W@ PR812 10_0402_1%
ISUMP ISUMN

Vboot=1.7V
FSW: 400KHz

		IccTDC	IccMax	OCP	R_DC_LL
47W	TDC	TDC at PL2 for 40 seconds starting from idle state	Max Current in Turbo Mode		
	27A	33A	85A	102A	-1.5 mV/A
37W	21A	26A	55A	66A	

Power Dissipation: H/S 1.0974W
L/S 0.4311W
with one L/S 1.586W

0.22UH 20% PCME064T-R22MS0R985 28A
DCR=0.98m ohm
SH00000OY00_7*7*4_600KHz

CPU_B+
EMI@ PL803 HCB2012KF-121T50_0805
@EMI@ PL805 HCB2012KF-121T50_0805
B+
PC811 10U_0805_25V6K
PC812 10U_0805_25V6K
PC813 10U_0805_25V6K
UGATE2
PR823 0_0603_5%
PQ805 AON6552_DFN5X6-8-5
PHASE2
PR826 2.2_0603_5%
PC817 0.22U_0603_25V7K
BOOT2
LGATE2
PQ806 AON6554_DFN5X6-8-5
@EMI@ PR827 4.7_1206_5%
@EMI@ PC818 680P_0603_50V7K
SNB_CPU_P2
PR828 3.65K_0603_1%
PL804 0.22UH 20% PCME064T-R22MS0R985 28A
+CPU_CORE
P2_SW P2_VO
PR831 100K_0603_1%
ISEN2
@ PR836 100K_0402_1%
@47W@ PR837 100K_0402_1%
PR835 10_0402_1%
ISUMP ISUMN

PQ801 AON6552_DFN5X6-8-5
PC825 10U_0805_25V6K
PC826 10U_0805_25V6K
PC827 10U_0805_25V6K
@EMI@ PC828 0.01U_0402_25V6
EMI@ PC829 470P_0402_50V7K
Max Height: PC823:8mm
PC823 100U_25V_M
UGATE1
PR839 0_0603_5%
PL801 0.22UH 20% PCME064T-R22MS0R985 28A
+CPU_CORE
P1_SW P1_VO
PHASE1
PR840 2.2_0603_5%
PC835 0.22U_0603_25V7K
BOOT1
LGATE1
PQ808 AON6554_DFN5X6-8-5
@EMI@ PR842 4.7_1206_5%
@EMI@ PC839 680P_0603_50V7K
SNB_CPU_P1
PR843 3.65K_0603_1%
PR844 100K_0603_1%
ISEN1
@ PR846 100K_0402_1%
@47W@ PR848 100K_0402_1%
PR847 10_0402_1%
ISUMP ISUMN

Module model information
ISL95812_V1A.mdd for IC portion
ISL95812_V1B.mdd for SW portion

Compal Electronics, Inc.
Title: CPU_CORE/GFX_CORE
Size: Document Number: Rev 0.1
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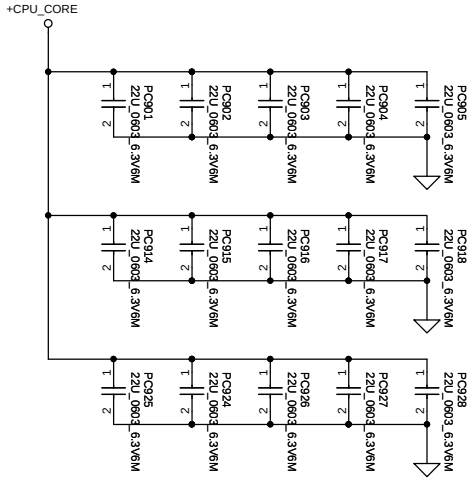
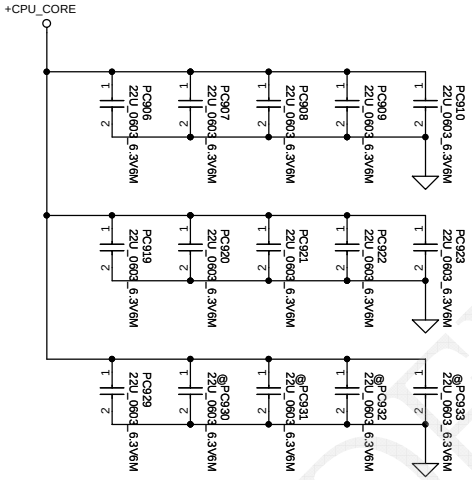
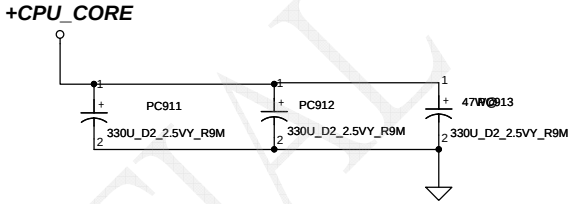
PWR Rule
需確認最新SPEC.
Modify 8/6.

3 X 330u/9m(47W)
2 X 330u/9m(37W)
24 pcs 22uF and reserve 4 pcs
2013/08/16

2 X 330u/9m(47W)
26 pcs 22uF
2013/08/28





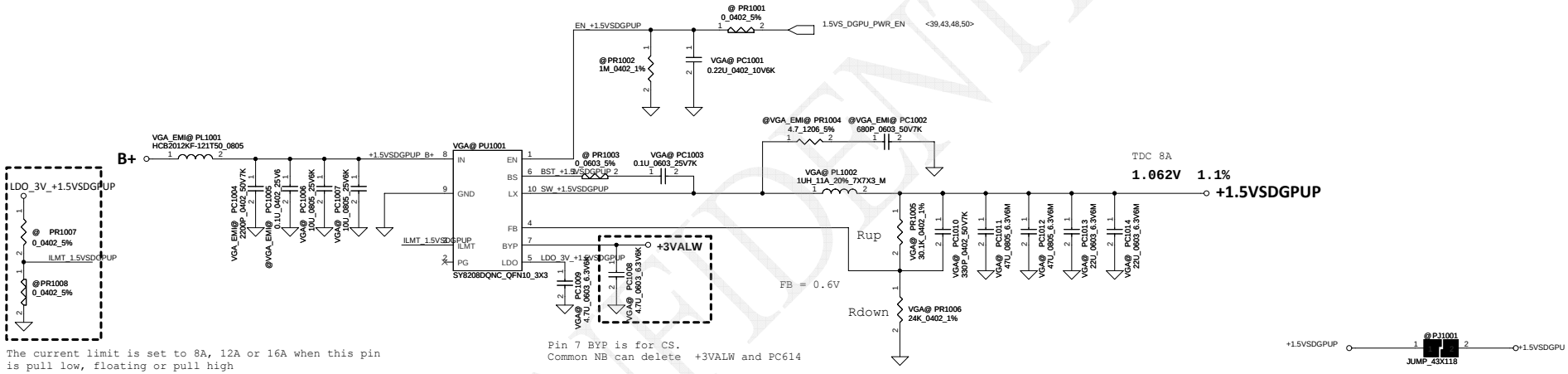


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/12/26	Deciphered Date	2014/12/26
Title	CPU_CORE_CAP		
Size: Custom	Document Number		Rev: 0.1
Date: Tuesday, May 27, 2014	Sheet 52 of 56		

Module model information

SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR1002



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC614

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)

Vout=1.05V

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: *+1.5VSDGPUP*

Size	Document Number	Rev
C		0.1

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Module model information:
RT8813A_V1A for IC module
RT8813A_V1B for SW module

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA

I_ripple=(19-0.9)*0.9/
(304.89Khz*0.36u*19)=7.811A

OCP=54A/2=27A per phase
Ivalley=27A-7.811A/2=23.1A

H-side MOS:AON6552
Rds(on):
5.6mohm@Vgs=10V
6.7mohm@Vgs=4.5V
Id :20A@Ta=25 degC

L-side MOS:AON6554
Rds(on):
3.2mohm@Vgs=10V
3~3.8mohm@Vgs=4.5V
Id :85A@Ta=25 degC

Choke: 0.36uH (Size:10*10*4)
Rdc=0.82mohm +-5%
Heat Rating Current=37A
Saturation Current=40A

C=3*330uF (9mohm)=990uF
Vripple=Iripple*ESR(min)=7.811A*3mohm=23.4mV

PWM-VID Spec and component Values

PWM-VID Spec		Config A	Config B	Config C	Config D
Vmin		0.6V	0.6V	0.65V	0.9V
Vmax		1.2V	1.2V	1.15V	1.15V
Vboot		0.875V	0.9V	0.9V	1.028V
Voltage step		6.25mV	6.25mV	25mV	12.5mV
N of Voltage level		96	96	20	20
PWM Frequency		1.125	1.125	0.676	0.676
Rrefadj	PR1206	39K	20K	39K	27K
Rref1	PR1204	39K	20K	30K	7.5K
Rboot	PR1205	1.5K	2K	3K	0
Rref2=PR1209 +PR1212	PR1209	30K	18K	24K	6.2K
	PR1212	1.5K	0	3K	1.74K
C	PC1209	1.5nf	2.7nf	1.8nf	5.6nf

Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT	N15S-GT	N15V-GM
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config D
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W	18W	18.16W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W	25W	24.72W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A	31A	29.2A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A	60A	44.3A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A		
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A	72A	54A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K	13K	10.2K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L	2phase 1H1L	2phase 1H1L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)		
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL	GT@	GM@

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

PSI Pull high on HW side

Pull high on HW side

Reserve Location

+VGA_CORE
EDP-Continuous 31A
EDP-Peak 60A
OCP min 72A

0.36uH_SH000000L400_10*10*4 (common: SH000011O00)

1. VSNS Soft-Start time (Internal) is 0.7ms (PC1213 un-pop)
   Tss=(Css*Vrefin)/Iss+2.3ms
   =0.01U*0.9V/5uA+2.3ms=4.1ms (PC1213 pop)

2. Switching frequency setting:
   Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=304.89Khz

3. Thermal monitoring:
   (VGPU_VREF-VTSNS)/PR23=VTSNS/Rth

	T_min	T_typical	T_max
PR1221=18.7K	96.73C	100C	103.1C
PR1221=13K	106.38C	110C	113.4C

2013/10/28 update PH1201 chang Common part SL200002E00

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: **RT8813**

Size | Document Number | Rev 0.1

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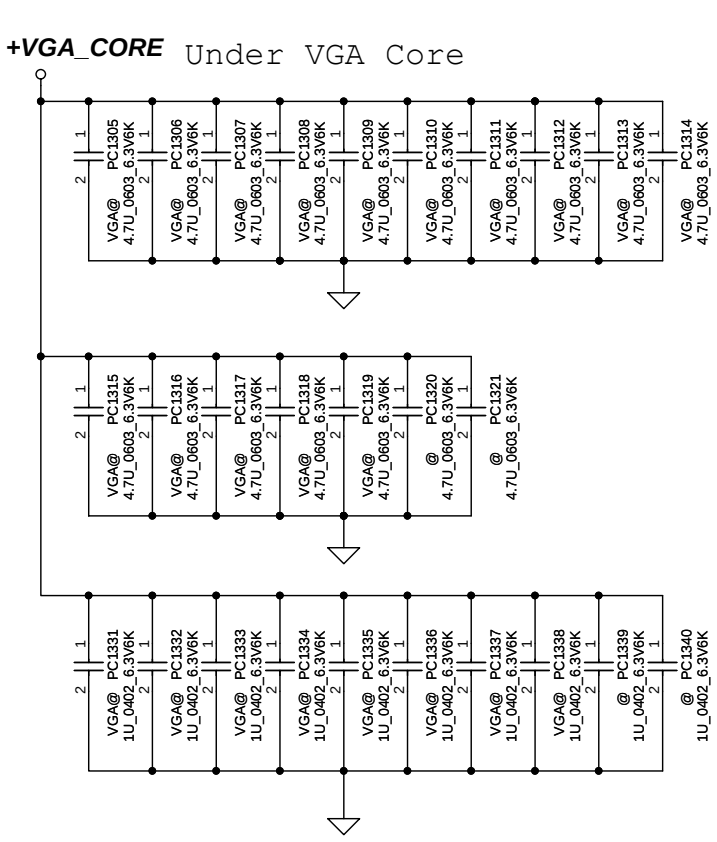
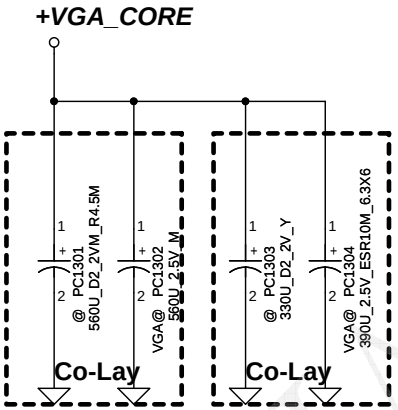
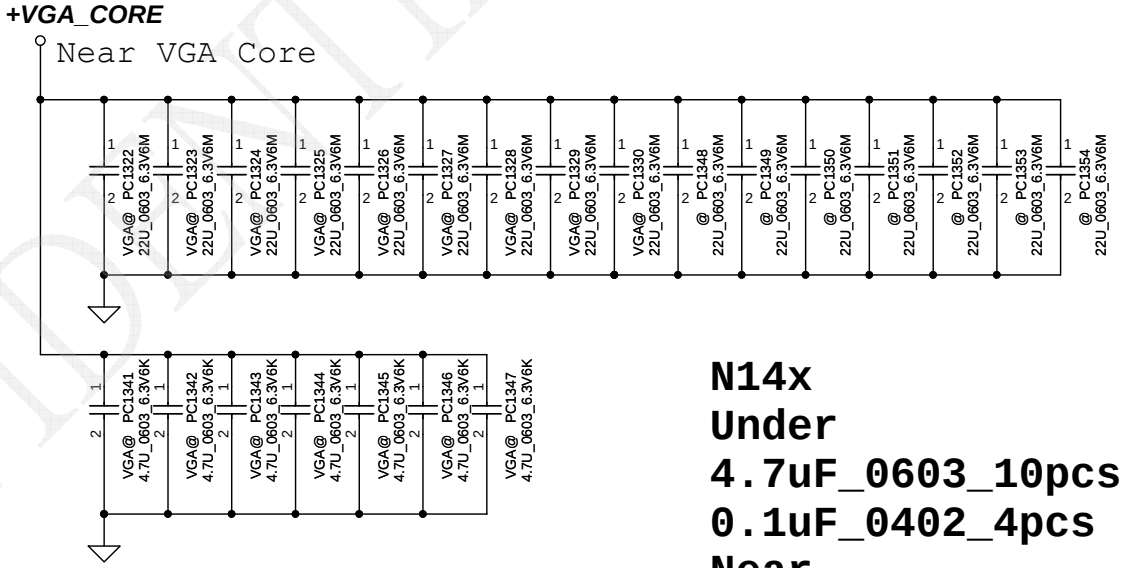




N15x
Under
4.7uF_0603_15pcs stuff 2
1uF_0402_8pcs stuff 2
Near
47uF_0805_0pcs
22uF_0805_14pcs stuff 7
4.7uF_0805_5pcs stuff 2



N14x
Under
4.7uF_0603_10pcs
0.1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0805_1pcs
4.7uF_0805_5pcs

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Title	*VGA_CORE CAP*		
Size: Custom	Document Number		Rev: 0.1
Date: Tuesday, May 27, 2014	Sheet 55 of 56		

Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1		Reduce 0 ohm count		Change PR510, PR602, PR607, PR809, PR816, PR820 to R-short	4/1	DVT
2	HW request	Change VRAM voltage to raise VRAM sequence	53	Change PR1006 to SD034240280	4/1	DVT
3		Improve CPU transient	51	Change PR818 to SD034976280	4/1	DVT
4		Reduce 0 ohm count		Change PR601, PR1001, PR1003, PR1008 to R-short	5/2	PVT
5		Component PN from M0 to 80	51	Change PC820 PN from SE0000006M0 to SE000000680	5/5	PVT
6		CPU low-side MOS selete	51	PQ804, PQ806, PQ808 from AON6414 change to AON6508	5/5	PVT
7		CPU TAT show VR thermal Alrt	51	change PR819 from 3.42K to 5.62K (active from 96'C to 106'C)	5/12	PVT
8		slewrate from ULV change to SV	51	PR808 from 16.9K to 3.24K (from 53mV/us to 12mV/us)	5/12	PVT
9		CPU low-side MOS selete	51	PQ804, PQ806, PQ808 from AON6508 change to AON6554	5/15	PVT MEMO
10		Thermal team change PH1 setting	45	PR216 from 16.9K to 26.1K (92'C active change to 85'C active)	5/15	PVT MEMO
12						
13						
14						
15						
16						
17						

Security Classification	Compal Secret Data		
Issued Date	2013/12/26	Deciphered Date	2014/12/26

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number | Rev: 0.1

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