Compal Confidential

Model Name : AIZY0
File Name : LA-B921PR10
BOM P/N:43xxxxxxxx

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AIZY0 M/B Schematics Document

Intel Broadwell Y Processor

2014-09-30

REV:1.0

Security Classification	Compal Secret Data		
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Title: *Cover Page*		
Size: Custom	Document Number: *LA-B921PR10*	Rev: 1.0
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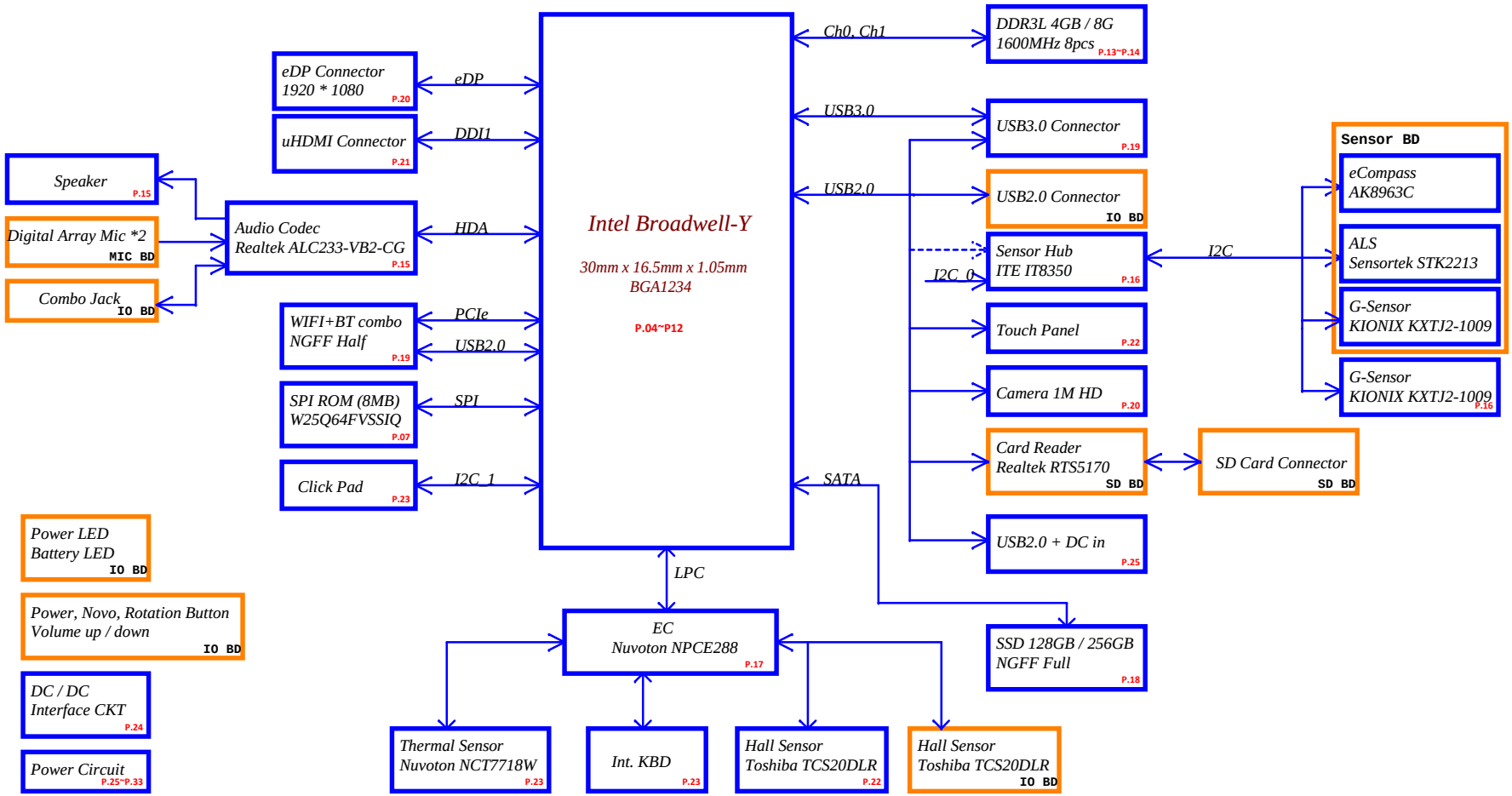
Model Name: AIZY0
File Name: LA-B921PR10

AIZY0 Intel Broadwell Y Block Diagram



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Issued Date	2014/04/10	Deciphered Date 2017/04/10	Title: MB Block Diagram
Size: Custom	Document Number		Rev: 1.0
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Voltage Rails

State \ power plane	B+	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +0.675VS
S0	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
76 LEVEL	X76@
UNPOP	@
CPU OPTION	CPU1@ ~ CPU8@
DRAM Option	H4G@ E4G@ S4G@ M4G1@ S8G@ E8G@ H8G@ M8G@ M4G2@
EMI POP	EMI@
ESD POP	ESD@
EMI UNPOP	@EMI@
ESD UNPOP	@ESD@
WLAN Support ISCT	ISCT@
WLAN No Support ISCT	NoISCT@

EC SM Bus1 address

Device	Address
Smart Battery	
Charger	
Home Key Button(TS)	8bit:0x60, 7bit:0x30

EC SM Bus2 address

Device	Address
Thermal Sensor NCT7718W	1001100x
Broadwell ULT SML1	

CPU SM Bus address

Device	Address
NA	

CPU SML0 Bus address

Device	Address
NA	

USB 2.0 Port Table

USB 2.0 Port	3 External USB Port
0	USB 2.0 Port (I/O Board)
1	USB 3.0/2.0 Port (MB)
2	DCIN USB COMBO
3	Card Reader
4	Touch Screen
5	Camera
6	Mini Card (WLAN/BT)
7	Sensor Fusion

USB 3.0 Port Table

Port	
1	
2	USB 3.0 Port (MB)
3	
4	

SATA Port Table

Port	
3	
2	
1	NGFF SSD(SATA)
0	

PCIE Port Table

Port	Lane	
1		
2		
3		
4		NGFF WLAN
5	0	
	1	
	2	
	3	
6	0	
	1	
	2	
	3	

HDMI Logo

ZZZ 45@ — HDMI Logo RO0000003HM

08/11, Add HDMI Logo P/N

CPU part

UCPU1 CPU1@	UCPU1 CPU2@	UCPU1 CPU3@	UCPU1 CPU4@	UCPU1 CPU5@	UCPU1 CPU6@	UCPU1 CPU7@	UCPU1 CPU8@
QGGY 1333/0.6G SA00007TL00	QGGZ 1333/0.8G SA00007TM00	QGGX 1600/0.8G SA00007TK00	QH1Y F0 0.8G SA00007YZ60	QH0U E0 1.1G SA000084N20	QH33 F0 0.8G SA00008BP00	QH2V F0 1.1G SA00008BU00	QH2R F0 1.2G SA00008BI00

07/01, Add QS SA00007YZ40 08/11, Add QS SA000084N00

PCB part

ZZZ003 — PCB 19O LA-B921P REV1 M/B 1 DA80011R110

09/30, Change PCB P/N to Rev.1.0

PCB Rev.1A P/N: DA80011R11A PCB 19O LA-B921P REV1A M/B 1

DRAM

ZZZ3 H4G@	ZZZ4 M4G2@	ZZZ7 S4G@	ZZZ8 M4G1@	ZZZ9 S8G@	ZZZ10 E8G@	ZZZ5 M8G@	ZZZ6 H8G@
HYNIX X7658138L02	MICRON X7658138L03	SAMSUNG X7658138L01	MICRON X7658138L04	SAMSUNG X7658138L05	ELPIDA X7658138L07	MICRON X7658138L08	HYNIX X7658138L06
H5TC4G63AFR-PBA SA00005AV70	MT41K256M16LY-107 SA000081200	K4B4G1646Q-HYK0 SA00005JC60	MT41K256M16HA-125:E SA00005WD60	K4B8G1646Q-MYK0 SA00006AT20	EDJ8416E6MB-GN-F SA00006AU30	MT41K512M16TNA-125E SA00006AV20	H5TC8G63AMR-PBA SA00006WZ20

07/01, SA00005HTB0 change to SA000081200

SMBUS Control Table

	HOST	Changer	BATT	NPCE288	CPU	HomeKey	Thermal sensor NCT7718W
EC_SMB_CK1 EC_SMB_DA1	NPCE288 +3VLP	V +3VLP	V +3VLP	X	X	V +3VALW	X
EC_SMB_CK2 EC_SMB_DA2	NPCE288 +3VS	X	X	X	V +3VS	X	V +3VS
SMBCLK SMBDATA	CPU +3VALW	X	X	X	X	X	X
SML0CLK SML0DATA	CPU +3VALW	X	X	X	X	X	X
SML1CLK SML1DATA	CPU +3VS	X	X	V +3VS	X	X	V +3VS

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Title: Note List

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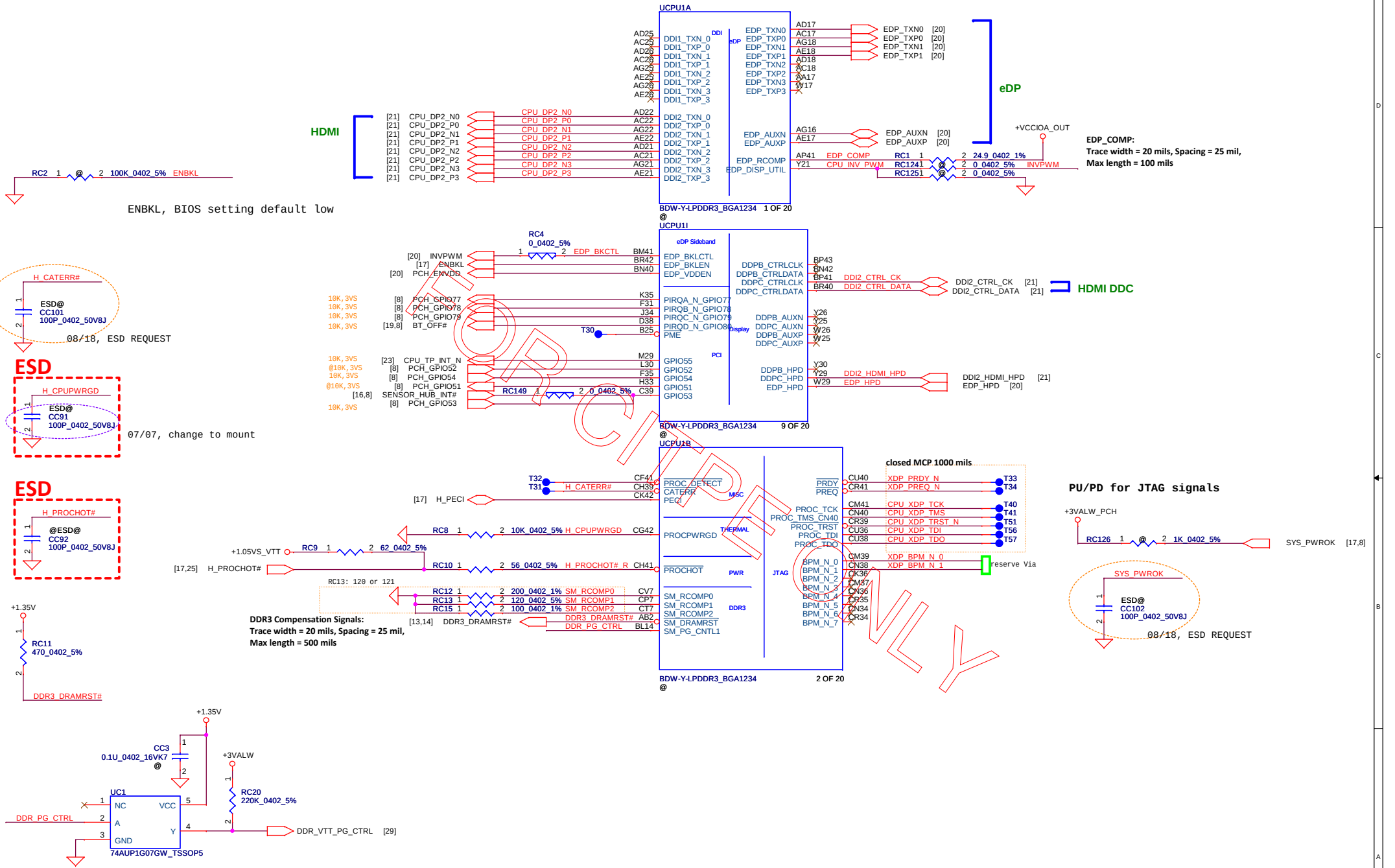

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Compal Electronics, Inc.			
Title	BDW MCP(1/9) DDI,eDP,PM,XDP		
Size	Document Number		Rev
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[13] DDR_A_D[0..63]
[13] DDR_A_MA[0..15]
[13] DDR_A_DQS#[0..7]
[13] DDR_A_DQS[0..7]

[14] DDR_B_D[0..63]
[14] DDR_B_MA[0..15]
[14] DDR_B_DQS#[0..7]
[14] DDR_B_DQS[0..7]

UCPU1C

DDR Channel A

DDR_A_D0	CT17	SA_DQ0	SA_CLK_N_0	CG4	M_CLK_A_DDR#0 [13]
DDR_A_D1	CV17	SA_DQ1	SA_CLK0	CG2	M_CLK_A_DDR0 [13]
DDR_A_D2	CN14	SA_DQ2	SA_CLK_N_1	CC4	
DDR_A_D3	CP15	SA_DQ3	SA_CLK1	CC6	
DDR_A_D4	CN16	SA_DQ4			
DDR_A_D5	CR16	SA_DQ5	SA_CKE0	CH11	DDR_A_CKE0 [13]
DDR_A_D6	CM13	SA_DQ6	SA_CKE1	CH9	DDR_A_CKE1 [13]
DDR_A_D7	CV15	SA_DQ7	SA_CKE2	CA12	
DDR_A_D8	CT13	SA_DQ8	SA_CKE3	CA10	
DDR_A_D9	CP13	SA_DQ9			
DDR_A_D10	CP10	SA_DQ10	SA_CS_N_0	CA4	DDR_A_CS0# [13]
DDR_A_D11	CM10	SA_DQ11	SA_CS_N_1	CA2	DDR_A_CS1# [13]
DDR_A_D12	CN12	SA_DQ12	SA_ODT0	CA6 DDRA_ODT0	T42
DDR_A_D13	CV13	SA_DQ13			
DDR_A_D14	CV10	SA_DQ14	SA_CAB3	CE2	DDR_A_RAS# [13]
DDR_A_D15	CT10	SA_DQ15	SA_CAB2	CE4	DDR_A_WE# [13]
DDR_A_D16	CT25	SA_DQ16	SA_CAB1	CC8	DDR_A_CAS# [13]
DDR_A_D17	CP25	SA_DQ17			
DDR_A_D18	CN22	SA_DQ18	SA_CAB4	CB5	DDR_A_BS0 [13]
DDR_A_D19	CP23	SA_DQ19	SA_CAB6	CC2	DDR_A_BS1 [13]
DDR_A_D20	CN24	SA_DQ20	SA_CAA5	CF11	DDR_A_BS2 [13]
DDR_A_D21	CV25	SA_DQ21			
DDR_A_D22	CV23	SA_DQ22	SA_CAB9	CE8 DDR_A_MA0	
DDR_A_D23	CT23	SA_DQ23	SA_CAB8	CE12 DDR_A_MA1	
DDR_A_D24	CN20	SA_DQ24	SA_CAB5	CF5 DDR_A_MA2	
DDR_A_D25	CN18	SA_DQ25	NOTUSED4	CE10 DDR_A_MA3	
DDR_A_D26	CT21	SA_DQ26	NOTUSED3	CG8 DDR_A_MA4	
DDR_A_D27	CT19	SA_DQ27	SA_CAA0	CG6 DDR_A_MA5	
DDR_A_D28	CP19	SA_DQ28	SA_CAA2	CH3 DDR_A_MA6	
DDR_A_D29	CP21	SA_DQ29	SA_CAA4	CE6 DDR_A_MA7	
DDR_A_D30	CV19	SA_DQ30	SA_CAA3	CB9 DDR_A_MA8	
DDR_A_D31	CV21	SA_DQ31	SA_CAA1	CC12 DDR_A_MA9	
DDR_A_D32	BU2	SA_DQ32	SA_CAB7	CF3 DDR_A_MA10	
DDR_A_D33	BW2	SA_DQ33	SA_CAA7	CG12 DDR_A_MA11	
DDR_A_D34	BW6	SA_DQ34	SA_CAA6	CH5 DDR_A_MA12	
DDR_A_D35	BU4	SA_DQ35	SA_CAB0	CB3 DDR_A_MA13	
DDR_A_D36	BW4	SA_DQ36	SA_CAA9	CF9 DDR_A_MA14	
DDR_A_D37	BT3	SA_DQ37	SA_CAA8	CG10 DDR_A_MA15	
DDR_A_D38	BU6	SA_DQ38			
DDR_A_D39	BT5	SA_DQ39	SA_DQSN0	CU16 DDR_A_DQS#0	
DDR_A_D40	BN2	SA_DQ40	SA_DQSN1	CR12 DDR_A_DQS#1	
DDR_A_D41	BR2	SA_DQ41	SA_DQSN2	CR24 DDR_A_DQS#2	
DDR_A_D42	BN6	SA_DQ42	SA_DQSN3	CR20 DDR_A_DQS#3	
DDR_A_D43	BN4	SA_DQ43	SA_DQSN4	BV3 DDR_A_DQS#4	
DDR_A_D44	BR6	SA_DQ44	SA_DQSN5	BP3 DDR_A_DQS#5	
DDR_A_D45	BR4	SA_DQ45	SA_DQSN6	BV9 DDR_A_DQS#6	
DDR_A_D46	BM5	SA_DQ46	SA_DQSN7	BP9 DDR_A_DQS#7	
DDR_A_D47	BM3	SA_DQ47			
DDR_A_D48	BT11	SA_DQ48	SA_DQSP0	CT15 DDR_A_DQS0	
DDR_A_D49	BU10	SA_DQ49	SA_DQSP1	CU12 DDR_A_DQS1	
DDR_A_D50	BW12	SA_DQ50	SA_DQSP2	CU24 DDR_A_DQS2	
DDR_A_D51	BW10	SA_DQ51	SA_DQSP3	CU20 DDR_A_DQS3	
DDR_A_D52	BW8	SA_DQ52	SA_DQSP4	BV5 DDR_A_DQS4	
DDR_A_D53	BU8	SA_DQ53	SA_DQSP5	BP5 DDR_A_DQS5	
DDR_A_D54	BU12	SA_DQ54	SA_DQSP6	BV11 DDR_A_DQS6	
DDR_A_D55	BT9	SA_DQ55	SA_DQSP7	BP11 DDR_A_DQS7	
DDR_A_D56	BN8	SA_DQ56			
DDR_A_D57	BR8	SA_DQ57	SM_VREF_CA	AP13	+V_DDR_VREFCA [13]
DDR_A_D58	BN12	SA_DQ58	SM_VREF_DQ0	AU14	+V_DDR_VREFDQ0 [13]
DDR_A_D59	BN10	SA_DQ59	SM_VREF_DQ1	AT13	+V_DDR_VREFDQ1 [14]
DDR_A_D60	BR12	SA_DQ60	SM_VCCDDQG	CC14	T44
DDR_A_D61	BR10	SA_DQ61			10 mil trace width
DDR_A_D62	BM11	SA_DQ62			
DDR_A_D63	BM9	SA_DQ63			

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UCPU1D

DDR Channel B

DDR_B_D0	BK3	SB_DQ0	SB_CK_N_0	AW6	M_CLK_B_DDR#0 [14]
DDR_B_D1	BK5	SB_DQ1	SB_CK0	AW4	M_CLK_B_DDR0 [14]
DDR_B_D2	BG6	SB_DQ2	SB_CK_N_1	AP11	
DDR_B_D3	BJ2	SB_DQ3	SB_CK1	AP9	
DDR_B_D4	BJ4	SB_DQ4			
DDR_B_D5	BJ6	SB_DQ5	SB_CKE0	BA2	DDR_B_CKE0 [14]
DDR_B_D6	BG2	SB_DQ6	SB_CKE1	BA4	DDR_B_CKE1 [14]
DDR_B_D7	BG4	SB_DQ7	SB_CKE2	AR8	
DDR_B_D8	BF3	SB_DQ8	SB_CKE3	AP5	
DDR_B_D9	BF5	SB_DQ9			
DDR_B_D10	BC6	SB_DQ10	SB_CS_N_0	AR10	DDR_B_CS0# [14]
DDR_B_D11	BE2	SB_DQ11	SB_CS_N_1	AT11	DDR_B_CS1# [14]
DDR_B_D12	BE4	SB_DQ12			
DDR_B_D13	BE6	SB_DQ13	SB_ODT0	AU10 DDRB_ODT0	T43
DDR_B_D14	BC2	SB_DQ14			
DDR_B_D15	BC4	SB_DQ15	SB_CAB3	BA10	DDR_B_RAS# [14]
DDR_B_D16	BE10	SB_DQ16	SB_CAB2	AW12	DDR_B_WE# [14]
DDR_B_D17	BC10	SB_DQ17	SB_CAB1	AW10	DDR_B_CAS# [14]
DDR_B_D18	BE8	SB_DQ18			
DDR_B_D19	BC8	SB_DQ19	SB_CAB4	AY11	DDR_B_BS0 [14]
DDR_B_D20	BF11	SB_DQ20	SB_CAB6	BA12	DDR_B_BS1 [14]
DDR_B_D21	BC12	SB_DQ21	SB_CAA5	AU2	DDR_B_BS2 [14]
DDR_B_D22	BE12	SB_DQ22			
DDR_B_D23	BF9	SB_DQ23	SB_CAB9	AT9 DDR_B_MA0	
DDR_B_D24	BJ12	SB_DQ24	SB_CAB8	AR4 DDR_B_MA1	
DDR_B_D25	BG12	SB_DQ25	SB_CAB5	AU8 DDR_B_MA2	
DDR_B_D26	BJ8	SB_DQ26	NOTUSED	AR6 DDR_B_MA3	
DDR_B_D27	BJ10	SB_DQ27	NOTUSED	AT5 DDR_B_MA4	
DDR_B_D28	BG8	SB_DQ28	SB_CAA0	AT3 DDR_B_MA5	
DDR_B_D29	BG10	SB_DQ29	SB_CAA2	BA8 DDR_B_MA6	
DDR_B_D30	BK9	SB_DQ30	SB_CAA4	AY3 DDR_B_MA7	
DDR_B_D31	BK11	SB_DQ31	SB_CAA3	AW2 DDR_B_MA8	
DDR_B_D32	AM1	SB_DQ32	SB_CAA1	AY5 DDR_B_MA9	
DDR_B_D33	AH2	SB_DQ33	SB_CAB7	AY9 DDR_B_MA10	
DDR_B_D34	AJ3	SB_DQ34	SB_CAA7	AU4 DDR_B_MA11	
DDR_B_D35	AM5	SB_DQ35	SB_CAA6	AU6 DDR_B_MA12	
DDR_B_D36	AM3	SB_DQ36	SB_CAB0	AW8 DDR_B_MA13	
DDR_B_D37	AJ1	SB_DQ37	SB_CAA9	BA6 DDR_B_MA14	
DDR_B_D38	AJ5	SB_DQ38	SB_CAA8	AR2 DDR_B_MA15	
DDR_B_D39	AH4	SB_DQ39			
DDR_B_D40	AG3	SB_DQ40	SB_DQSN0	BH5 DDR_B_DQS#0	
DDR_B_D41	AG1	SB_DQ41	SB_DQSN1	BD5 DDR_B_DQS#1	
DDR_B_D42	AD2	SB_DQ42	SB_DQSN2	BD11 DDR_B_DQS#2	
DDR_B_D43	AE3	SB_DQ43	SB_DQSN3	BH11 DDR_B_DQS#3	
DDR_B_D44	AE1	SB_DQ44	SB_DQSN4	AK2 DDR_B_DQS#4	
DDR_B_D45	AG5	SB_DQ45	SB_DQSN5	AF2 DDR_B_DQS#5	
DDR_B_D46	AD4	SB_DQ46	SB_DQSN6	AK8 DDR_B_DQS#6	
DDR_B_D47	AE5	SB_DQ47	SB_DQSN7	AF8 DDR_B_DQS#7	
DDR_B_D48	AM9	SB_DQ48			
DDR_B_D49	AM7	SB_DQ49	SB_DQSP0	BH3 DDR_B_DQS0	
DDR_B_D50	AH8	SB_DQ50	SB_DQSP1	BD3 DDR_B_DQS1	
DDR_B_D51	AJ9	SB_DQ51	SB_DQSP2	BD9 DDR_B_DQS2	
DDR_B_D52	AM11	SB_DQ52	SB_DQSP3	BH9 DDR_B_DQS3	
DDR_B_D53	AJ7	SB_DQ53	SB_DQSP4	AK4 DDR_B_DQS4	
DDR_B_D54	AJ11	SB_DQ54	SB_DQSP5	AF4 DDR_B_DQS5	
DDR_B_D55	AH10	SB_DQ55	SB_DQSP6	AK10 DDR_B_DQS6	
DDR_B_D56	AE11	SB_DQ56	SB_DQSP7	AF10 DDR_B_DQS7	
DDR_B_D57	AG7	SB_DQ57			
DDR_B_D58	AE7	SB_DQ58			
DDR_B_D59	AE9	SB_DQ59			
DDR_B_D60	AG11	SB_DQ60			
DDR_B_D61	AG9	SB_DQ61			
DDR_B_D62	AD8	SB_DQ62			
DDR_B_D63	AD10	SB_DQ63			

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Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.

Title: BDW MCP(2/9) DDRIII

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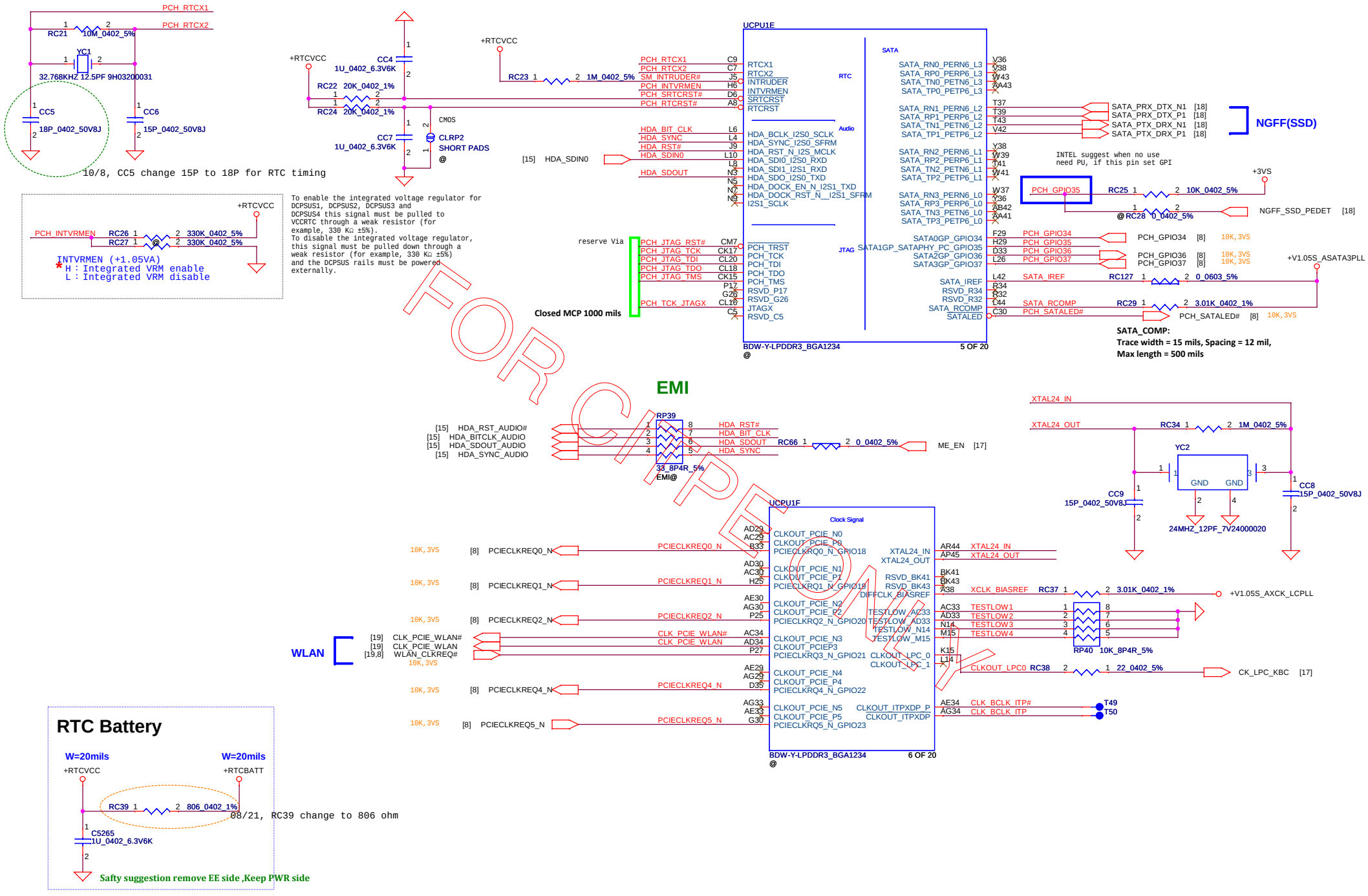

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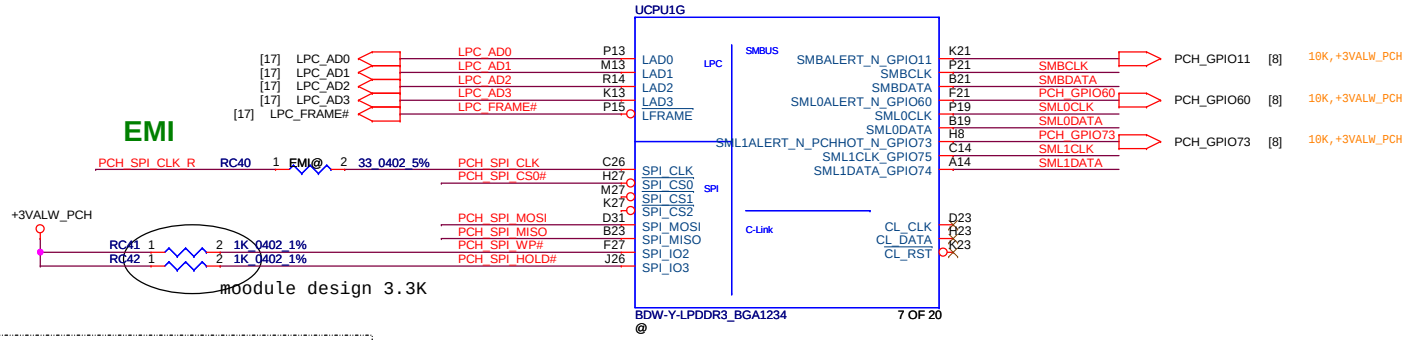
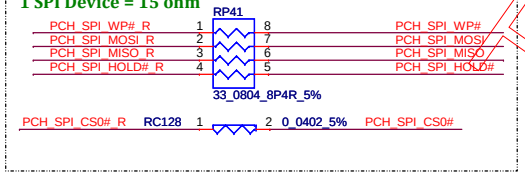
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.			
Title: BDW MCP(3/9) SATA,HDA,CLK			
Size: Custom	Document Number: LA-B921PR10		Rev: 1.0
Date: Thursday, October 23, 2014	Sheet 6 of 36		

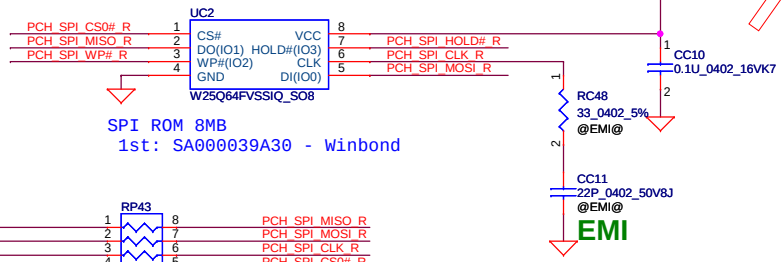


Closed to ROM

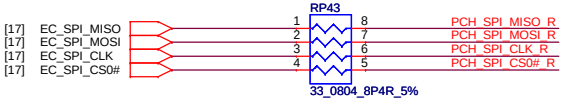
CHKLIST1.0
2 SPI Device = 33 ohm
1 SPI Device = 15 ohm



SPI ROM FOR ME (8MByte)
ROM is Quad SPI



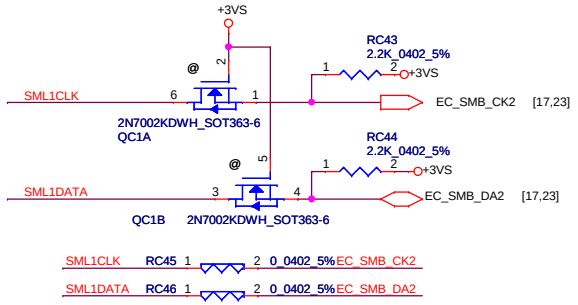
SPI ROM 8MB
1st: SA000039A30 - Winbond

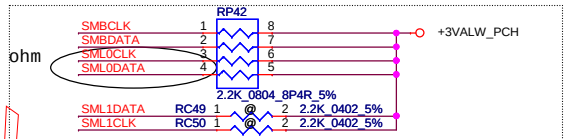


SML1 Bus BIOS set Native,
it's OD pin

SML1 Bus :EC/Thermal Sensor

FootPrint :DMN66D0LDW-7_SOT363-6





moodule design 499 ohm
CRB 2.2K

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Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.			
Title: BDW MCP(4/9) LPC,SPI,SMBUS			
Size: Custom	Document Number: LA-B921PR10		Rev: 1.0
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Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit CAN be NC ,if not support Deep Sx

DPWROK: Tired toghter with RSMRST# that do not support Deep Sx

DSWODVREN - On Die DSW VR Enable
* H : Enable(DEFAULT)
L : Disable

DPWROK can be tied to RSMRST# for platforms that do not support the Deep Sx state.

ESD

H_PLT_RST#
@ESD@ CC93 100P_0402_50V8J

07/07, change to mount

+3VS

RC53 1 2 0_0402_5%

@ UC3 MC74VHC1G08DFT2G_SC70-5

H_PLT_RST# → PLT_RST# [17,19]

RC59 100K_0402_5%

+RTCVCC

RC52 1 2 330K_0402_5%

RC56 1 @ 2 330K_0402_5%

RC54 1 2 0_0402_5% EC_RSMRST#

1K, +3VALW_PCH

UCPU1H

System Power Management

BDW-Y-LPDDR3_BGA1234 @

8 OF 20

SUSACK#	SUSACK# R	D19
SYS_RESET#	SYS_RESET#	E26
SYS_PWROK	SYS_PWROK	A22
PCH_PWROK	PCH_PWROK	F9
APWROK	APWROK_R	J22
PLTRST	H_PLT_RST#	M23
RSMRST	EC_RSMRST#	F7
SUSWARN_N_SUSPWRDNACK_GPIO30	PCH_GPIO30	D8
PWRBTN	PBTN_OUT#	M21
ACPRESENT_GPIO31	AC_PRESENT	M17
BATLOW_N_GPIO72	PCH_GPIO72	H17
SLP_S0	SLP_S0_N	G22
SLP_WLAN_N_GPIO29	PCH_GPIO29	J18
DSWVRMEN	DSWODVREN	G14
DPWROK	DPWROK	J7
WAKE	PCH_PCIE_WAKE#	F19
GPIO32_CLKRUN	PCH_GPIO32	B35
SUS_STAT_N_GPIO61	PCH_GPIO61	D25
SUSCLK_GPIO62		B27
SLP_S5_N_GPIO63	PM_SLP_S5#	A18
SLP_S4	PM_SLP_S4#	H19
SLP_S3	PM_SLP_S3#	N22
SLP_A	PM_SLP_A#	G18
SLP_SUS	SLP_SUS_N	D27
SLP_LAN	SLP_LAN_N	K19

SUSCLK_WLAN [19]
PM_SLP_S5# [17]
PM_SLP_S4# [17]
PM_SLP_S3# [17]

T52 T54 T55

10K, 3VS @10K, +3VALW_PCH

T58 T53

ESD

PCH_PWROK
@ESD@ CC95 100P_0402_50V8J

ESD

EC_RSMRST#
CC96 1000P_0402_50V7K ESD@

08/18, change to mount

ESD

SYS_RESET#
@ESD@ CC97 100P_0402_50V8J

ESD

H_THERMTRIP#
@ESD@ CC94 100P_0402_50V8J

UCPU1J

BDW-Y-LPDDR3_BGA1234 @

10 OF 20

BMBUSY_N_USB3PHY_PC_GPIO76	PCH_GPIO76	J30
GPIO8	PCH_GPIO8	C18
LAN_PHY_PWR_CTRL_GPIO12	PCH_GPIO12	J14
GPIO15	PCH_GPIO15	K25
GPIO16	PCH_GPIO16	N26
GPIO17	PCH_GPIO17	H31
GPIO24	PCH_GPIO24	C22
GPIO27	PCH_GPIO27	K17
GPIO28	PCH_GPIO28	M25
GPIO26	PCH_GPIO26	B15
GPIO56	RAM_ID0	E25
GPIO57	RAM_ID1	F23
GPIO58	RAM_ID2	F16
GPIO59	RAM_ID3	D15
GPIO44	PCH_GPIO44	L18
GPIO47	DDR_ID	B29
GPIO48	PCH_GPIO48	K28
GPIO49	PCH_GPIO49	B31
GPIO50	PCH_GPIO50	F33
GPIO71	PCH_GPIO71	D29
GPIO13	PCH_GPIO13	E14
GPIO45	SENSOR_HUB_INT# R	M19
GPIO25	PCH_GPIO25	F17
GPIO45	PCH_GPIO45	P23
GPIO46	SENSOR_HUB_RST#	L22
GPIO9	PCH_GPIO9	D17
GPIO10	PCH_GPIO10	B17
DEVSLP0_GPIO33	PCH_GPIO33	E30
SDIO_POWER_EN_GPIO70	PCH_GPIO70	R36
DEVSLP1_GPIO38	PCH_GPIO38	K31
DEVSLP2_GPIO39	EC_SCI#	J41
SPKR_GPIO81	SPKR	A34

CPU/MISC

THERMTRIP	H_THERMTRIP#	CG40
RCIN_N_GPIO82		C34
SERIRQ	SERIRQ	E34
PCH_OPI_RCOMP	PCH_OPIRCOMP	AB4
RSVD_AJ14		AJ14
RSVD_AL18		AL18

KB_RST# [17]
SERIRQ [17]

RC60 1K_0402_1%

RC61 49.9_0402_1%

+1.05VS_VTT

LPIO

GSPI0_CS_N_GPIO83	PCH_GPIO83	D40
GSPI0_CLK_GPIO84	PCH_GPIO84	G34
GSPI0_MISO_GPIO85	PCH_GPIO85	L36
GSPI0_MOSI_GPIO86	PCH_GPIO86	K33
GSPI1_CS_N_GPIO87	PCH_GPIO87	L34
GSPI1_CLK_GPIO88	PCH_GPIO88	M31
GSPI1_MISO_GPIO89	PCH_GPIO89	F37
GSPI_MOSI_GPIO90	PCH_GPIO90	H35
UART0_RTS_N_GPIO91	PCH_GPIO91	M35
UART0_RXD_GPIO91	PCH_GPIO92	F39
UART0_TXD_GPIO92	PCH_GPIO93	N43
UART0_CTS_N_GPIO94	PCH_GPIO94	N41
UART1_RXD_GPIO0	PCH_GPIO0	P29
UART1_TXD_GPIO1	PCH_GPIO1	H38
UART1_RST_N_GPIO2	PCH_GPIO2	N39
UART1_CTS_N_GPIO3	PCH_GPIO3	N30
I2C0_SDA_GPIO4	I2C0_SDA_SEN	N36
I2C0_SCL_GPIO5	I2C0_SCL_SEN	R42
I2C1_SDA_GPIO6	I2C1_SDA_TP	J37
I2C1_SCL_GPIO7	I2C1_SCL_TP	M33
SDIO_CLK_GPIO64	PCH_GPIO64	N34
SDIO_CMD_GPIO65	PCH_GPIO65	H40
SDIO_D0_GPIO66	PCH_GPIO66	R40
SDIO_D1_GPIO67	PCH_GPIO67	R38
SDIO_D2_GPIO68	PCH_GPIO68	J39
SDIO_D3_GPIO69	PCH_GPIO69	P31

T59

I2C0_SDA_SEN [16]
I2C0_SCL_SEN [16]
I2C1_SDA_TP [23]
I2C1_SCL_TP [23]

10K, 3VS

GSPI0_MOSI / GPIO86 : Boot BIOS Strap

1: LPC BUS
* 0: SPI BUS (Have internal PD)

PCH_GPIO86 RC1101 @ 2 1K_0402_1% RC1111 2 1K_0402_1%

SDIO_D0 / GPIO66 : Top-Block Swap Override

* 0: DISABLED (Have internal PD)
1: ENABLED

PCH_GPIO66 RC112 1 @ 2 4.7K_0402_5%

GPIO15 : TLS Confidentiality

1: Intel ME TLS with confidentiality
* 0: Intel ME TLS with no confidentiality (Have internal PD)

PCH_GPIO15 RC113 2 @ 1 1K_0402_1%

06/30, RC130~RC133 change value to 2.2K ohm

I2C1_SDA_TP RC130 1 2 2.2K_0402_5%
I2C1_SCL_TP RC131 1 2 2.2K_0402_5%
I2C0_SDA_SEN RC132 1 2 2.2K_0402_5%
I2C0_SCL_SEN RC133 1 2 2.2K_0402_5%

RP65 10K_8P4R_5% — PCH_GPIO64, PCH_GPIO68, PCH_GPIO69, SYS_RESET#

RP64 10K_8P4R_5% — PCH_GPIO0, PCH_GPIO1, PCH_GPIO2, PCH_GPIO3 (08/21, change to unpop)

RC51 200K_0402_5% — +3VALW_PCH — AC_PRESENT

RP63 10K_8P4R_5% — PCH_GPIO91, PCH_GPIO92, PCH_GPIO93, PCH_GPIO94 (08/21, change to unpop)

RP62 10K_8P4R_5% — PCH_GPIO84, PCH_GPIO85, PCH_GPIO89, PCH_GPIO90 (08/21, change to unpop)

RP45 10K_8P4R_5% — PCH_GPIO48; PCIECLKREQ4_N [6]; WLAN_CLKREQ# [19,6]; PCIECLKREQ2_N [6]

RP46 10K_8P4R_5% — PCH_GPIO32, KB_RST#; PCIECLKREQ1_N [6]; PCH_GPIO36 [6]

RP47 10K_8P4R_5% — PCH_GPIO67, PCH_GPIO65, EC_SCI#; PCH_GPIO53 [4]

RP48 10K_8P4R_5% — PCH_GPIO78 [4] [16], PCH_GPIO77 [4], PCH_GPIO79 [4], BT_OFF# [19,4]

RP49 10K_8P4R_5% — PCH_GPIO38; PCH_GPIO52 [4], PCH_GPIO51 [4]

RP50 10K_8P4R_5% — SERIRQ; PCH_GPIO37 [6]; PCIECLKREQ5_N [6]; PCIECLKREQ0_N [6]

RP51 10K_8P4R_5% — PCH_GPIO71, PCH_GPIO16; PCH_SATALED# [6], PCH_GPIO34 [6]

RP52 10K_8P4R_5% — PCH_GPIO33, PCH_GPIO50, PCH_GPIO76, PCH_GPIO49 (08/21, change to unpop)

RC65 1 2 10K_0402_5% — PCH_GPIO54 [4]

RP54 10K_8P4R_5% — +3VALW_PCH; RC1361 2 1K_0402_5% PCH_PCIE_WAKE#; PCH_GPIO12, PCH_GPIO8; PCH_GPIO30; PCH_GPIO73 [7]

RP55 10K_8P4R_5% — PCH_GPIO61, PCH_GPIO29

RP57 10K_8P4R_5% — SENSOR_HUB_RST#, PCH_GPIO13, SENSOR_HUB_INT# R, PCH_GPIO25

RP59 10K_8P4R_5% — PCH_GPIO28, PCH_GPIO9, PCH_GPIO10; PCH_GPIO60 [7]

RC62 1 @ 2 0_0402_5% — NGFF_SSD_PRESENT# [18]

RC1381 1 @ 2 0_0402_5% — SENSOR_HUB_INT# [16,4]

RC63 1 2 0_0402_5% — DEVSLP1 [18]; EC_SCI# [17]; SPKR [15]

RP61 10K_8P4R_5% — +3VS; PCH_GPIO87, PCH_GPIO17, PCH_GPIO83, PCH_GPIO70

RP58 10K_8P4R_5% — +3VS; PCH_GPIO44, PCH_GPIO26, PCH_GPIO45, PCH_GPIO24 (08/21, change to unpop)

+3VALW_PCH

RC64 1 2 10K_0402_5% PCH_GPIO72
RC1461 2 10K_0402_5% PCH_GPIO27
RC67 1 2 10K_0402_5% PCH_GPIO11 [7]
RC1471 2 10K_0402_5% DDR_ID
RC1481 @ 2 10K_0402_5%

DDR_ID
PU 10K to +3VALW_PCH (DDR3L)
PU down 10K (LP-DDR3)

+3VS

RC1371 @ 2 1K_0402_5% SPKR

+3VALW_PCH

RC116 10K_0402_5% X76@ RAM_ID3 — RC120 10K_0402_5% X76@
RC117 10K_0402_5% X76@ RAM_ID2 — RC121 10K_0402_5% X76@
RC118 10K_0402_5% X76@ RAM_ID1 — RC122 10K_0402_5% X76@
RC119 10K_0402_5% X76@ RAM_ID0 — RC123 10K_0402_5% X76@

RAM_ID3 GPI059	RAM_ID2 GPI058	RAM_ID1 GPI057	RAM_ID0 GPI056	RAM P/N
0	0	0	0	HYNIX H5TC4G63AFR-PBA
0	0	0	1	SAMSUNG K4B4G1646Q-HYK0
0	0	1	0	MICRON MT41K256M16HA-125:E
0	0	1	1	ELPIDA EDJ4216EFBG-GN-F
0	1	0	0	SAMSUNG K4B8G1646Q-MYK0
0	1	0	1	ELPIDA EDJ8416E6MB-GN-F
0	1	1	0	MICRON MT41K512M16TNA-125:E
0	1	1	1	HYNIX H5TC8G63AMR-PBA
1	0	0	0	MT41K256M16LY-107
1	0	0	1	TBD
1	0	1	0	TBD
1	0	1	1	TBD
1	1	0	0	TBD
1	1	0	1	TBD
1	1	1	0	TBD
1	1	1	1	TBD

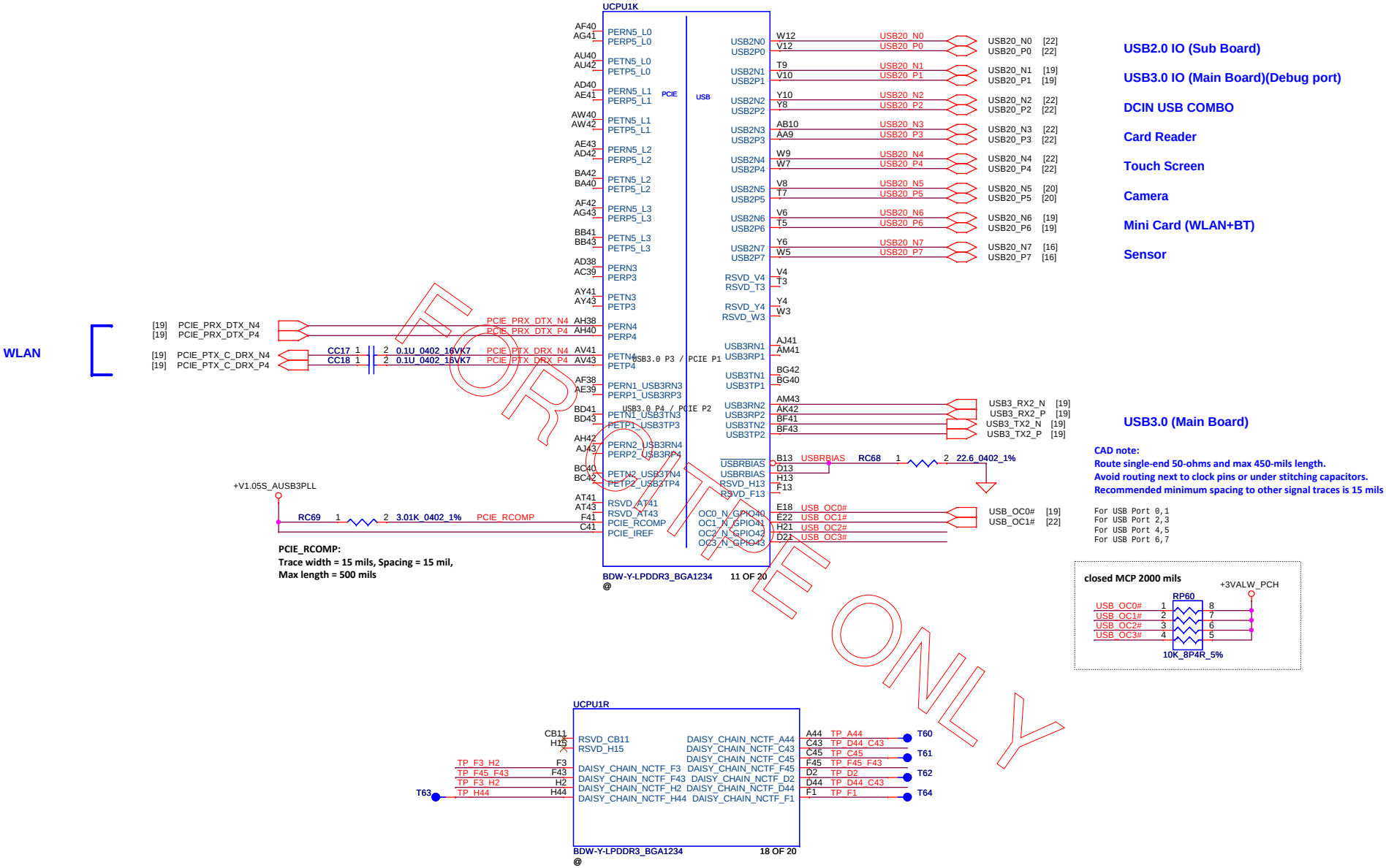
Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.

Title: P08-BDW MCP(5/9) PM,GPIO,I2C

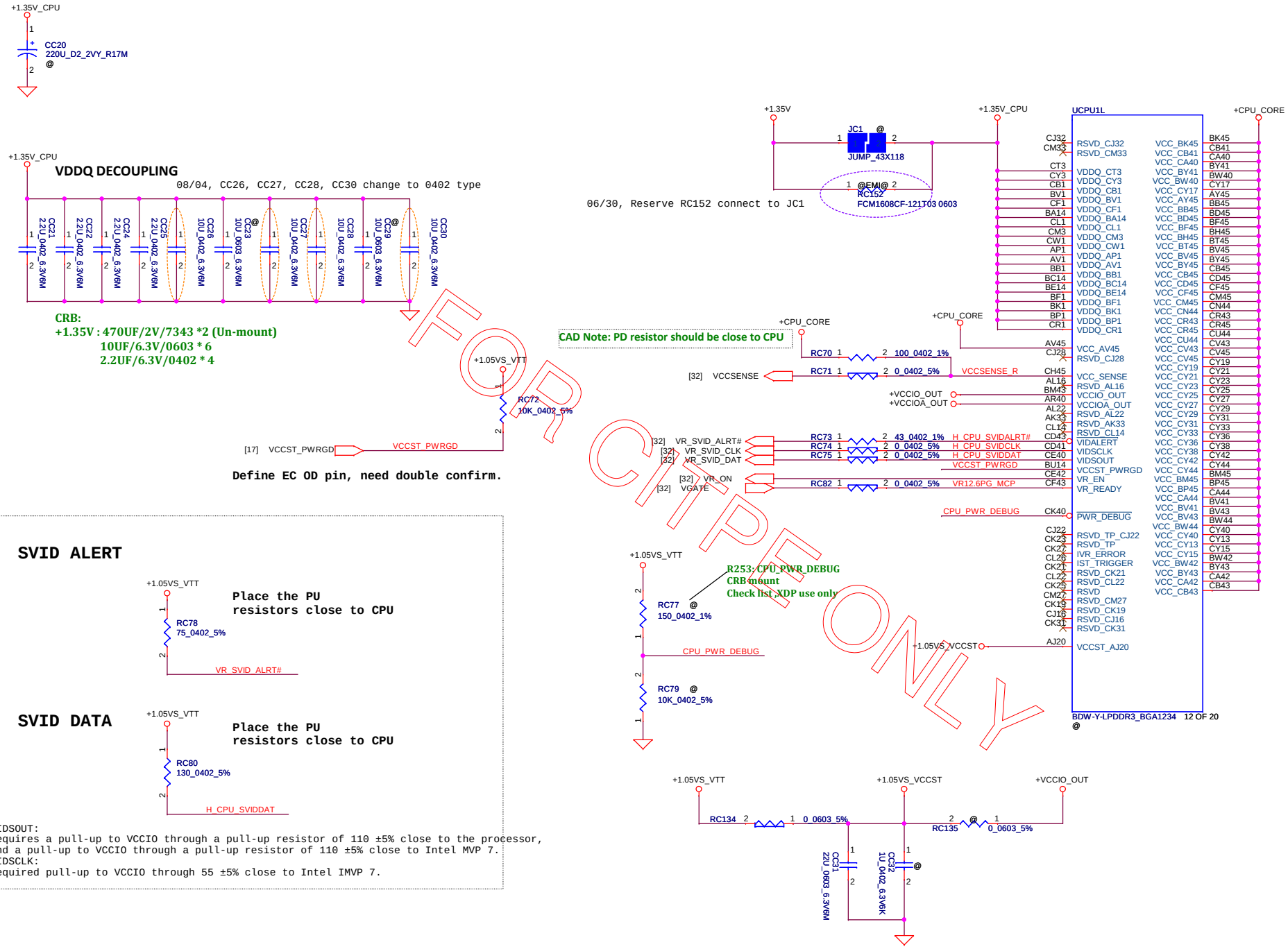
Size: Custom | Document Number: LA-B921PR10 | Rev: 1.0

Date: Friday, October 17, 2014 | Sheet 8 of 36



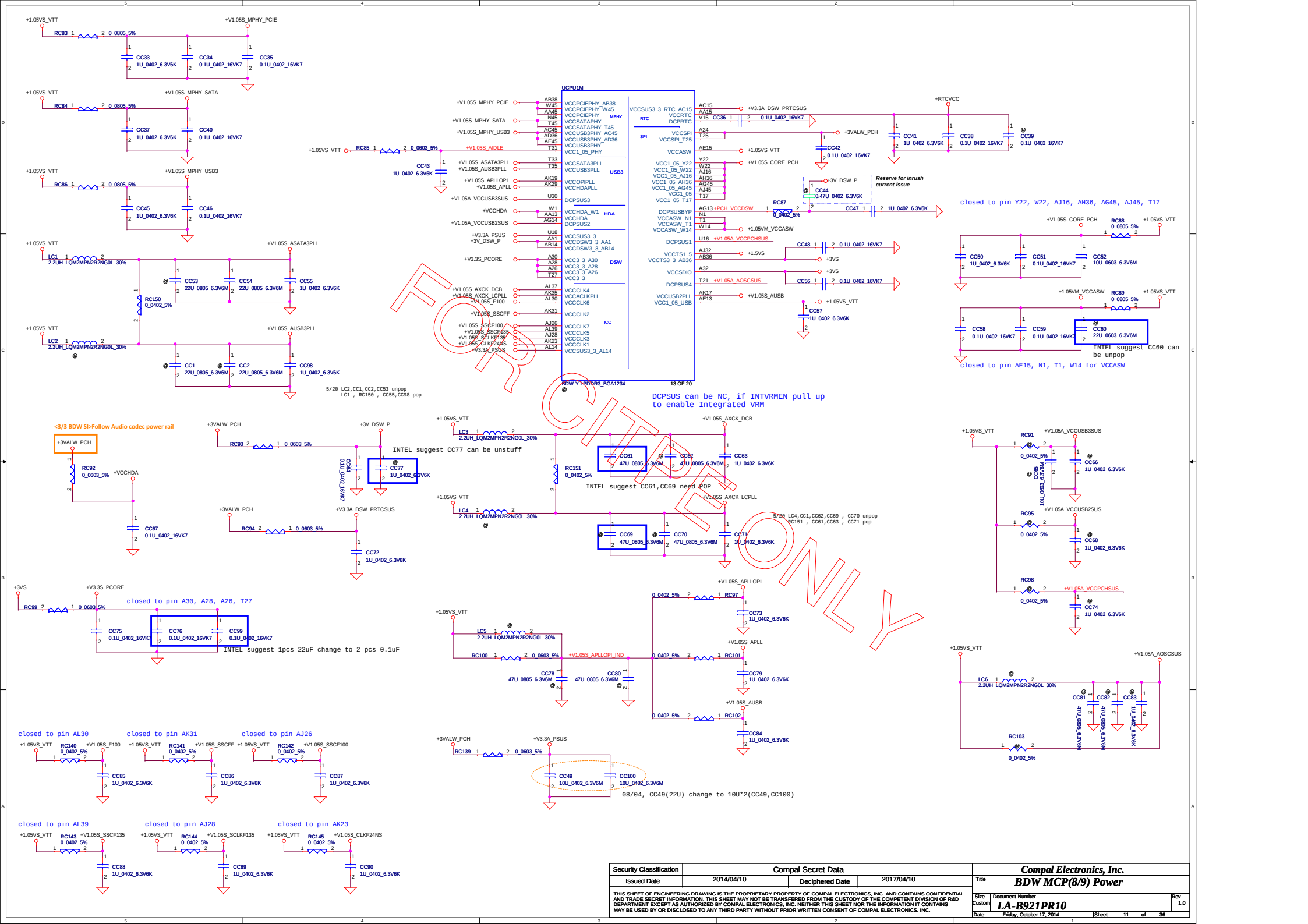
Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.			
Title	P09-BDW MCP(6/9) PCIe,USB		
Size	Document Number		Rev
Custom	LA-B921PR10		1.0
Date:	Friday, October 17, 2014	Sheet 9 of 36	



Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.	
Title	P10-BDW MCP(7/9) Power
Size: Custom	Document Number: LA-B921PR10
Rev	1.0
Date: Friday, October 17, 2014	Sheet 10 of 36



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Issued Date	2014/04/10	Deciphered Date	2017/04/10

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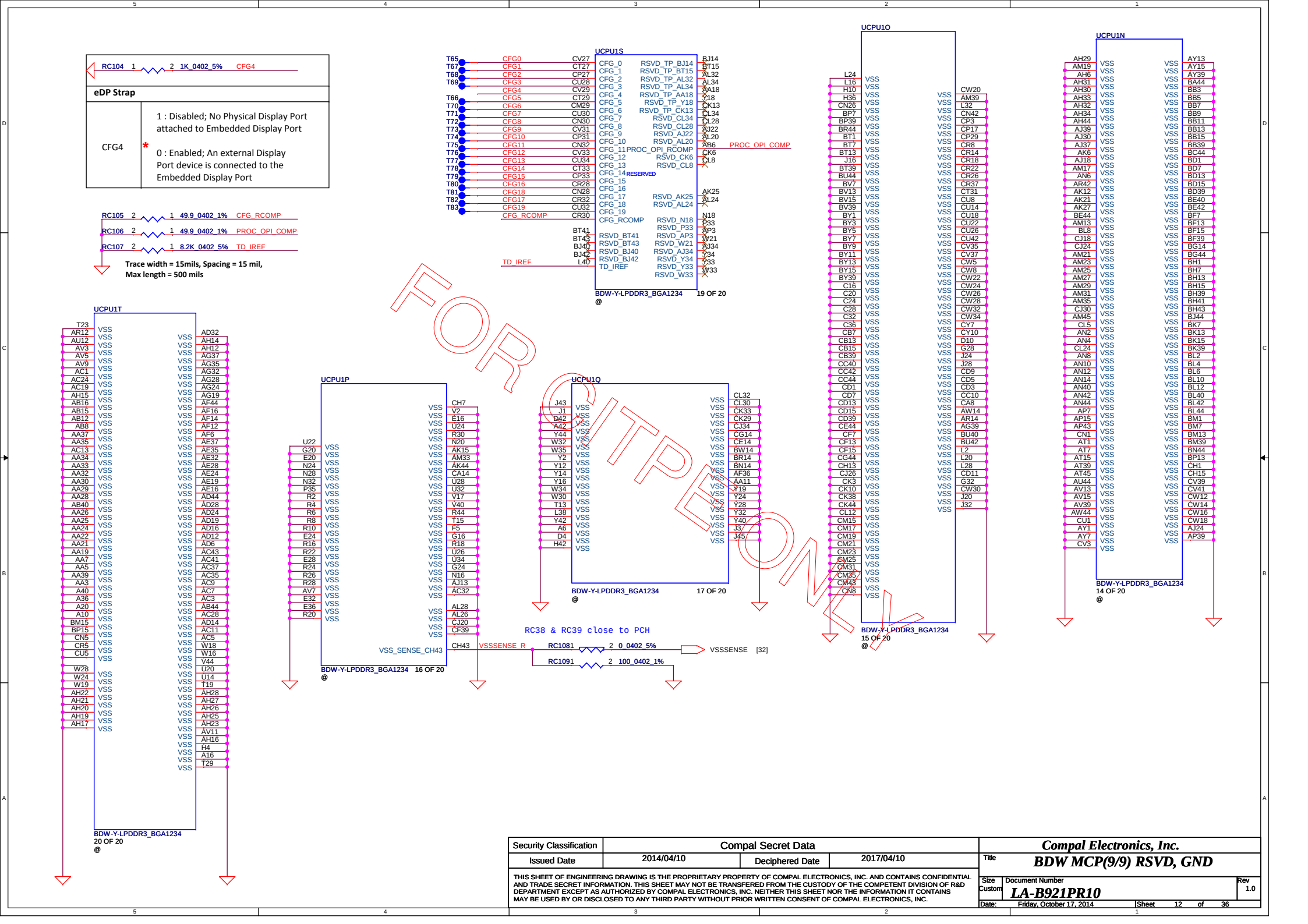
Title: BDW MCP(8/9) Power			
Size: Custom	Document Number: LA-B921PR10		Rev: 1.0
Date: Friday, October 17, 2014		Sheet 11 of 36	



Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.			
Title	BDW MCP(9/9) RSVD, GND		
Size: Custom	Document Number: LA-B921PR10		Rev: 1.0
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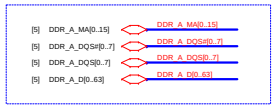
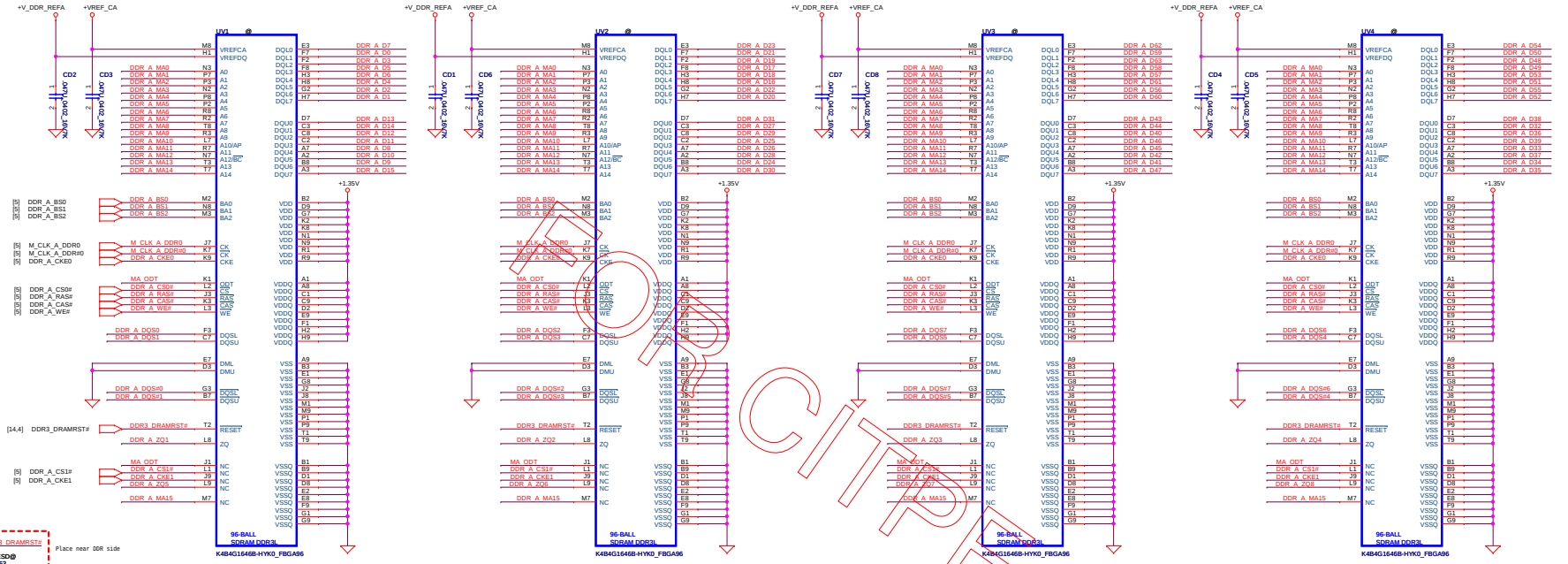
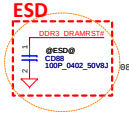
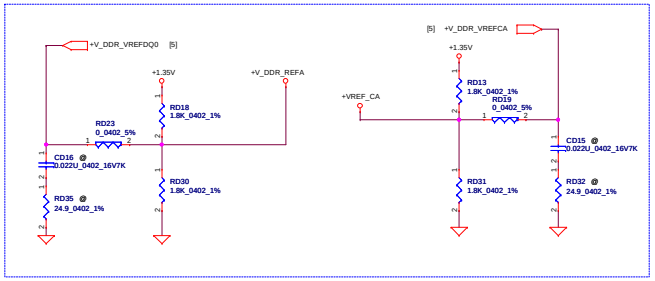
On Board A

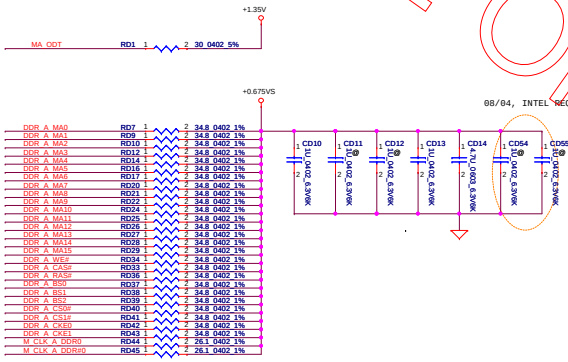




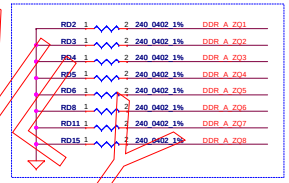


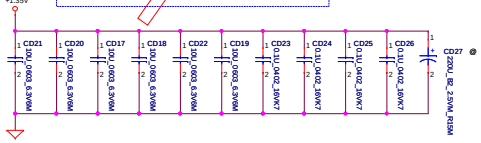
08/18, ESD REQUEST, place near CPU side



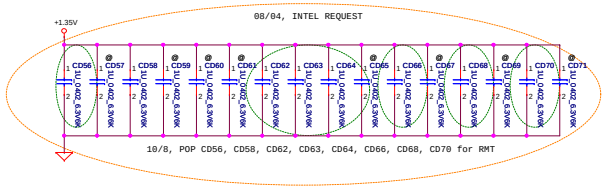


08/04, INTEL REQUEST





08/04, INTEL REQUEST



10/8, POP CD56, CD58, CD62, CD63, CD64, CD66, CD68, CD70 for RMT

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Issued Date	2014/04/10	Deciphered Date	2017/04/10
Title	DDRIII ON BOARD		
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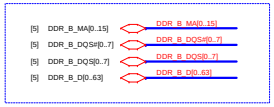
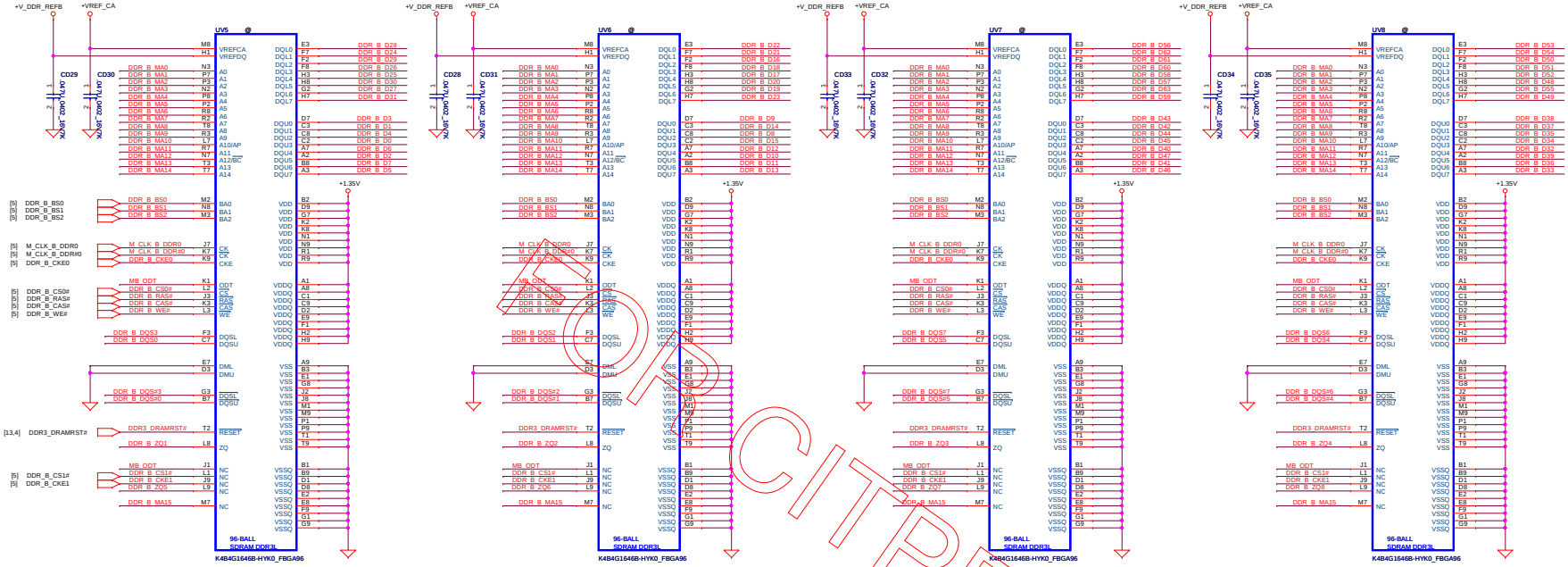
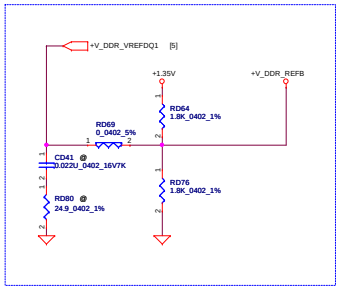
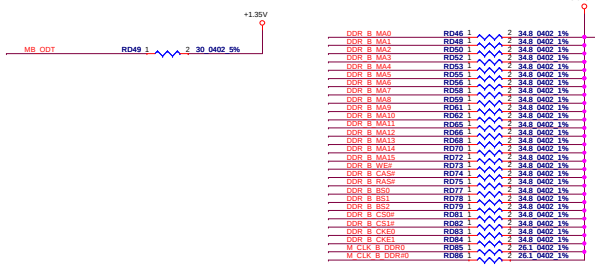
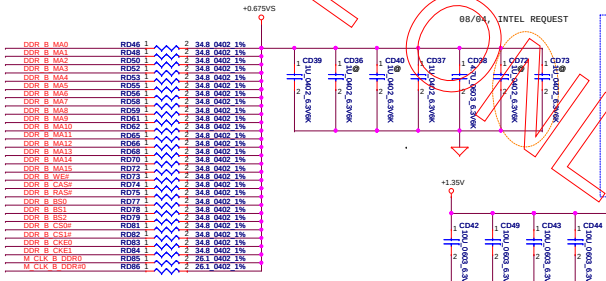
On Board B

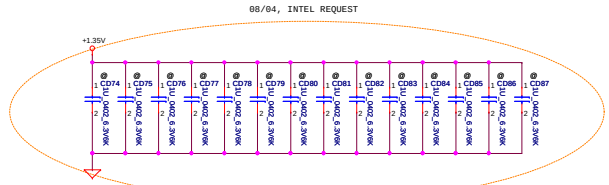












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Issued Date	2014/04/10	Deciphered Date	2017/04/10
Title	DDRIII ON BOARD		
Size: Custom	Document Number: LA-B921PR10		Rev: 1.0
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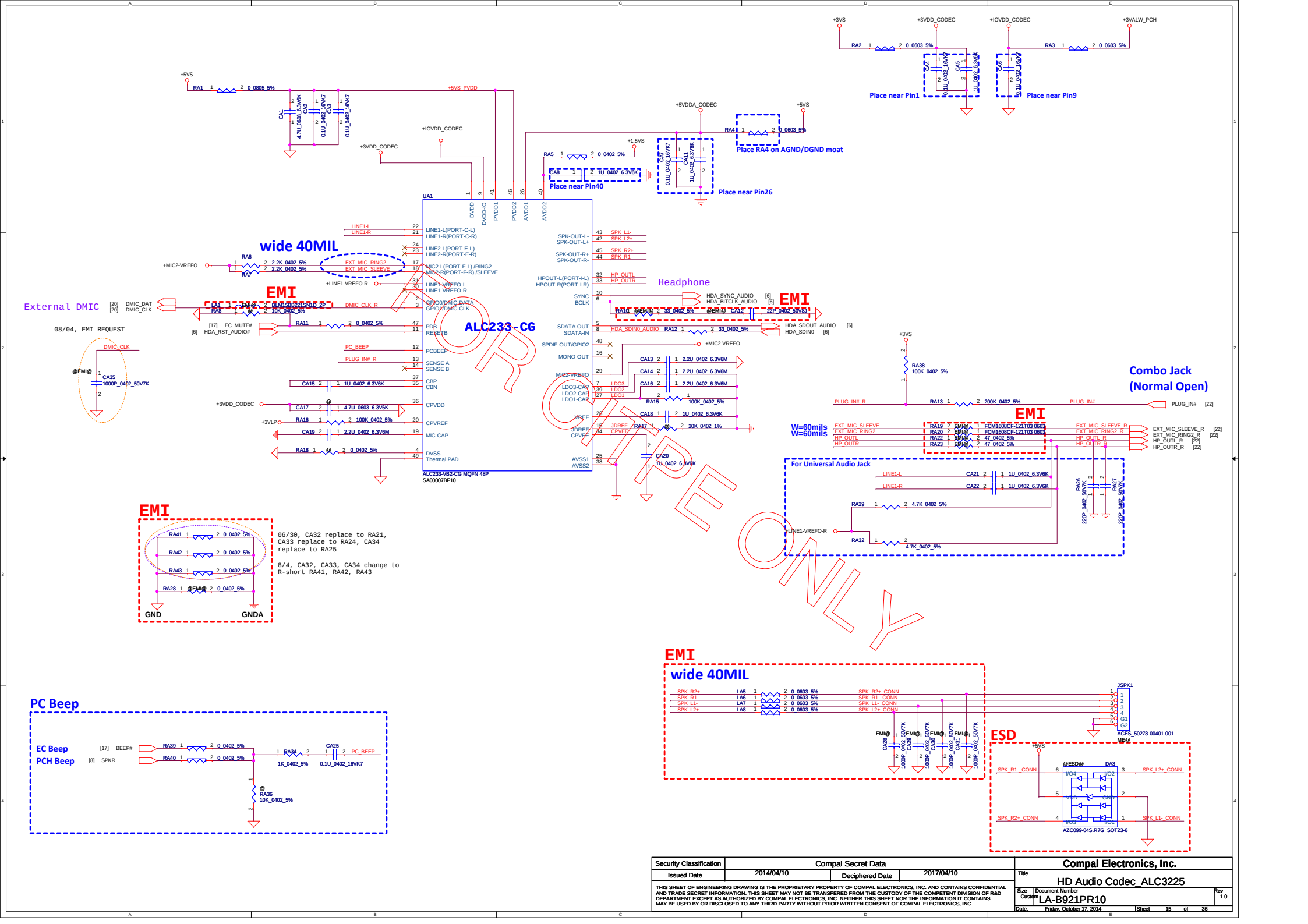
wide 40MIL
EMI
ALC233-CG
External DMIC
08/04, EMI REQUEST
Headphone
Combo Jack
(Normal Open)
W=60mils
W=60mils
For Universal Audio Jack
Place near Pin1
Place near Pin9
Place near Pin40
Place near Pin26
Place RA4 on AGND/DGND moat
PC Beep
EC Beep
PCH Beep
ESD
wide 40MIL
06/30, CA32 replace to RA21, CA33 replace to RA24, CA34 replace to RA25
8/4, CA32, CA33, CA34 change to R-short RA41, RA42, RA43
GND
GNDA
ALC233-VB2-CG MQFN 48P
SA00007BF10
AZC099-04S.R7G_SOT23-6
ACES_50278-00401-001
JSPK1
Security Classification
Compal Secret Data
Issued Date
2014/04/10
Deciphered Date
2017/04/10
Compal Electronics, Inc.
HD Audio Codec_ALC3225
LA-B921PR10
Rev 1.0
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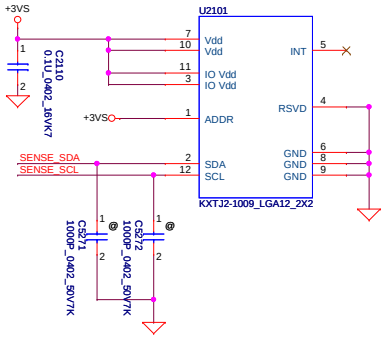
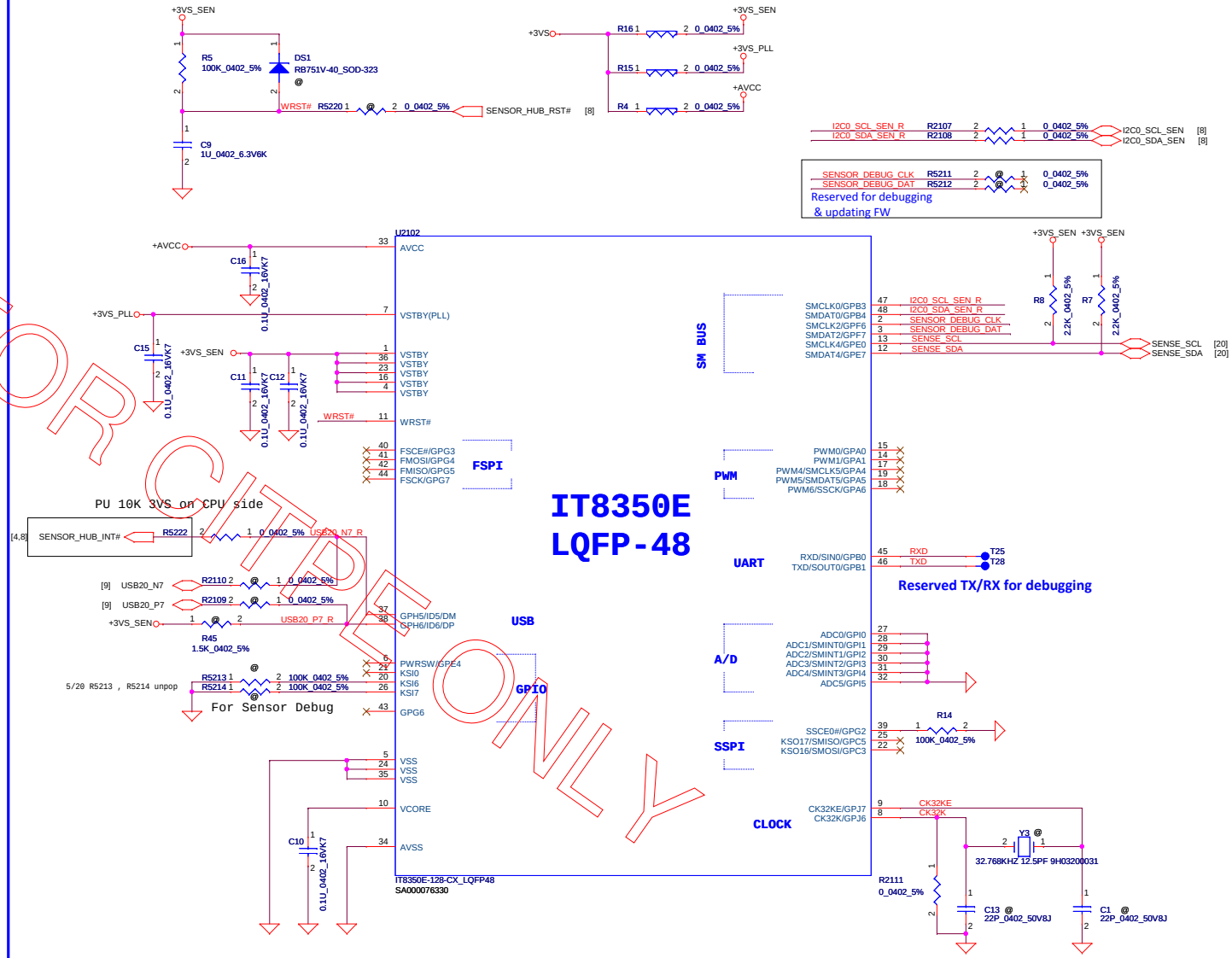
2nd G-sensor



Sensor Hub



Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.

Title: Sensor Fusion

Size	Document Number	Rev
Custom	LA-B921PR10	1.0

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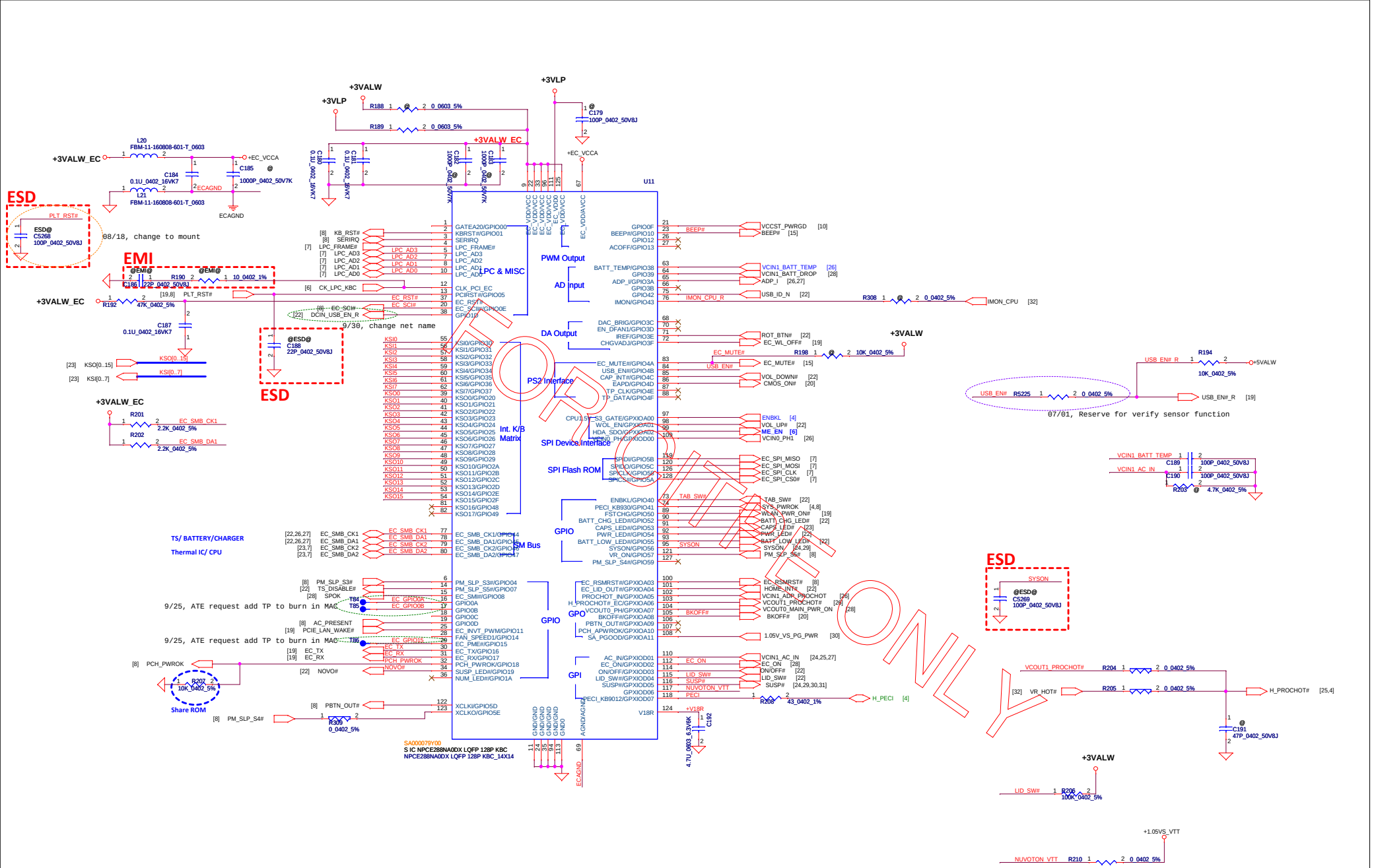

Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.	
Title	BIOS & EC I/O Port
Size: C	Document Number: LA-B921PR10
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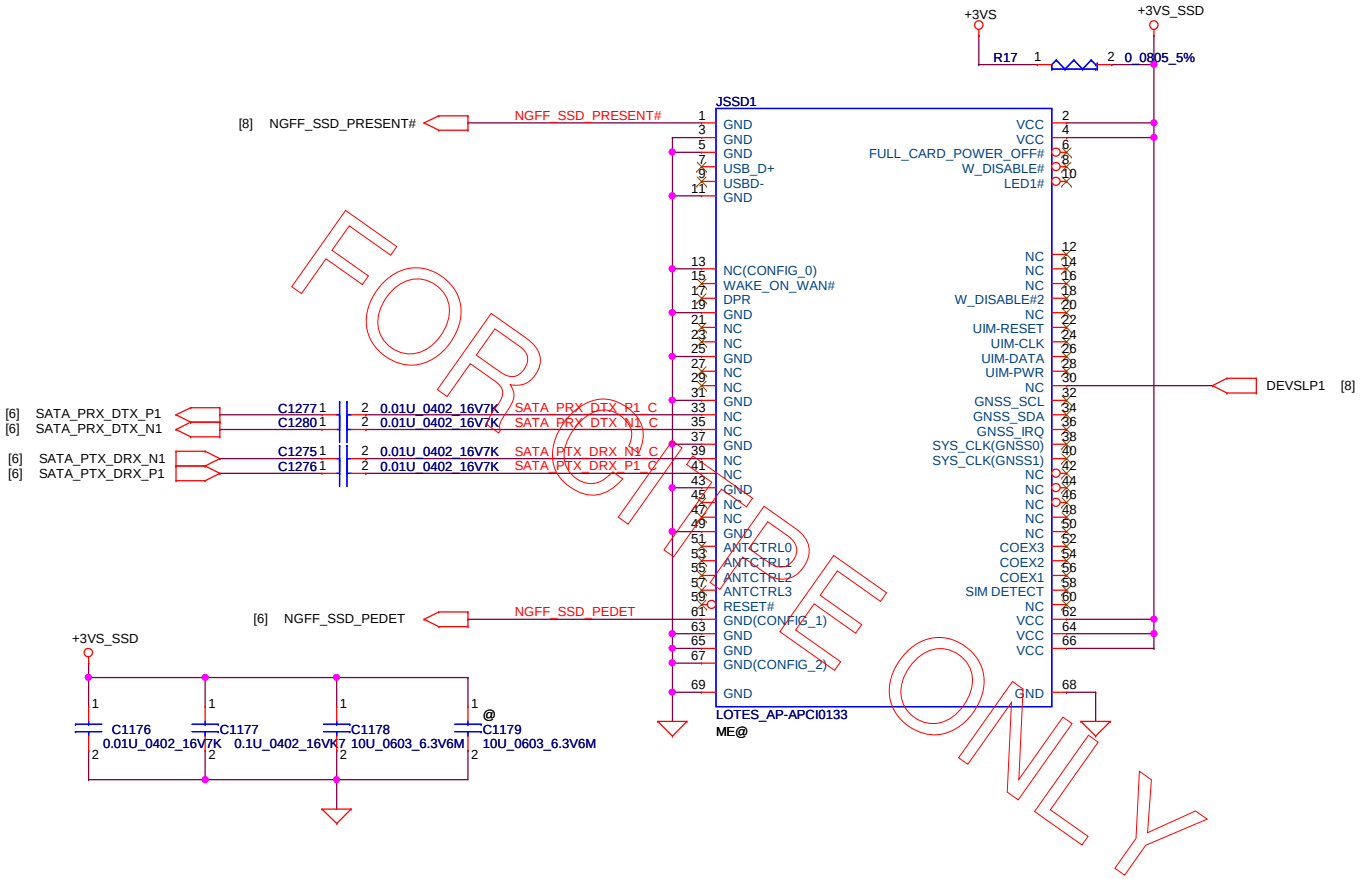
NGFF for SSD(Key B)



Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.

Title: **SSD**

Size	Document Number	Rev
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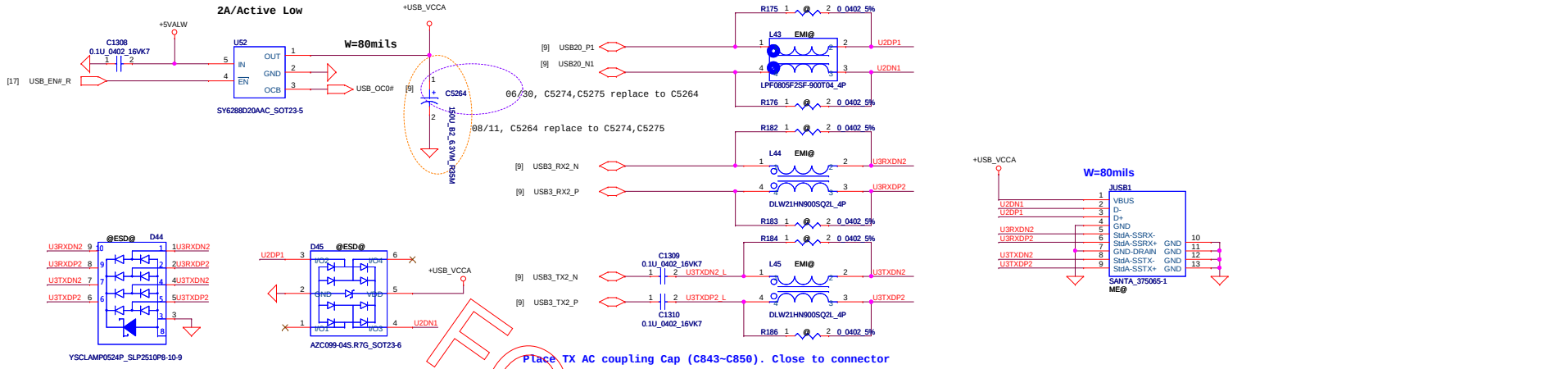
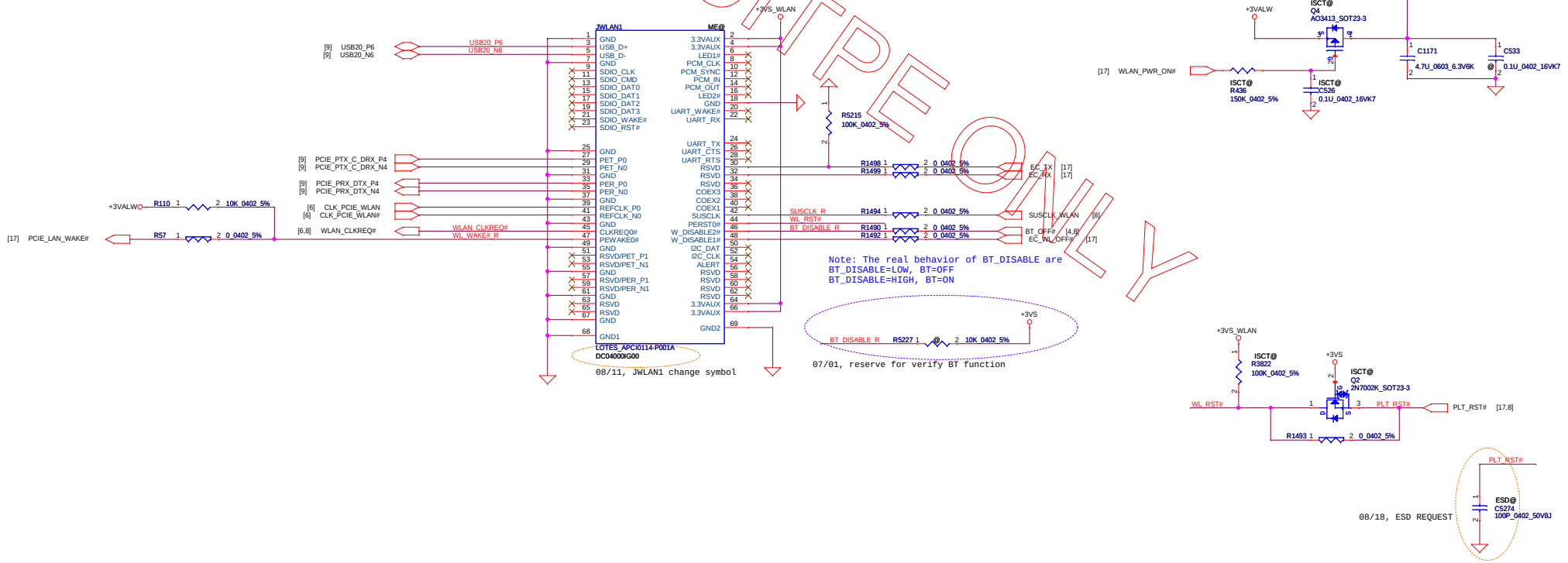
USB 3.0 Conn.



NGFF for WLAN(Key E)



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Issued Date	2014/04/10	Deciphered Date	2017/04/10

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Title	USB3.0/WLAN		
Size	Document Number		Rev
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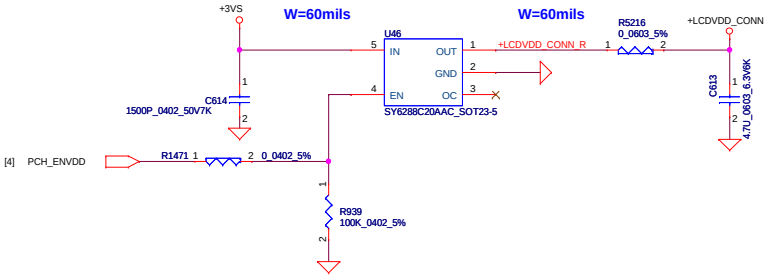
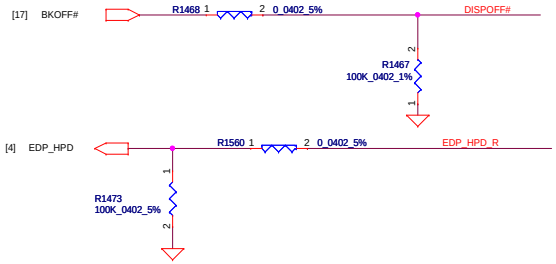
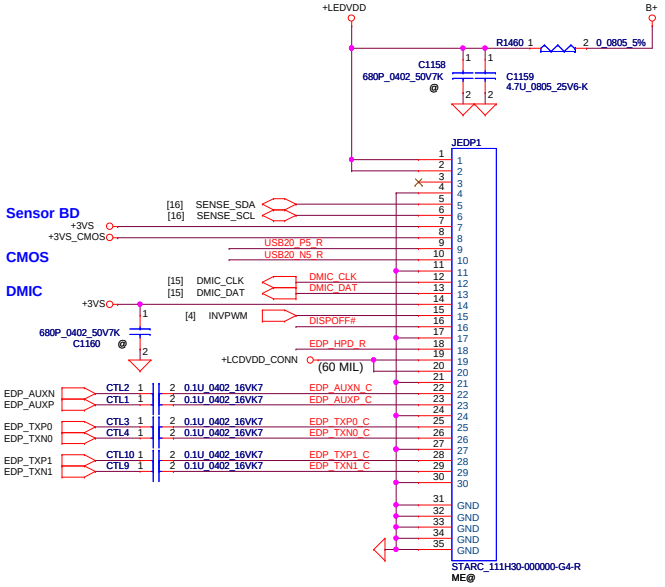
Date:	Friday, October 17, 2014	Sheet	19 of 36

LCD POWER CIRCUIT

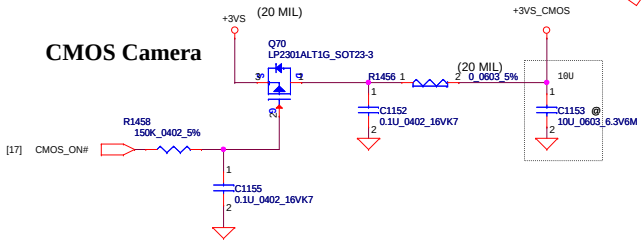


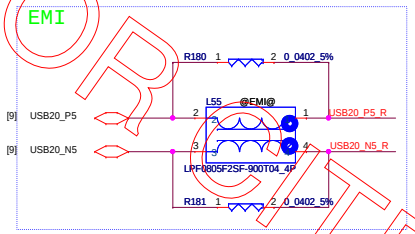


eDP PANEL/DMIC/COMS/SENSOR. Conn.



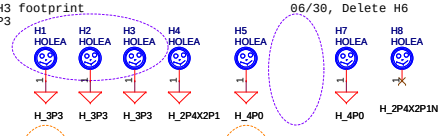
CMOS Camera

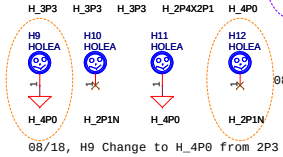




06/30, H1,H2,H3 footprint
change to H_3P3

06/30, Delete H6





08/18, Add H12

08/18, H9 Change to H_4P0 from 2P3

Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.

Title: **eDP /DMIC/COMS/HOLE**

Size	Document Number	Rev
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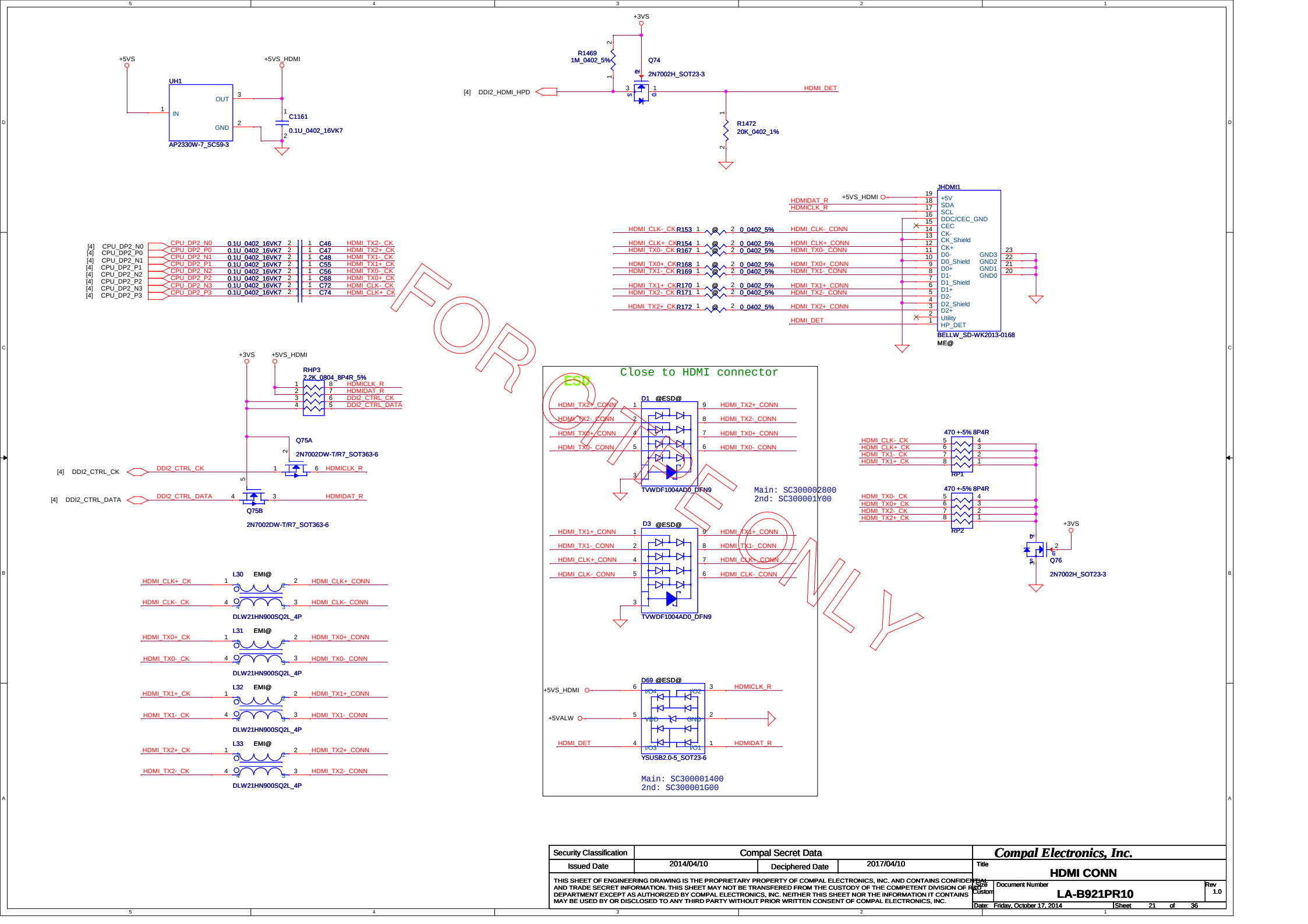

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **HDMI CONN**

Size: Custom	Document Number: LA-B921PR10	Rev: 1.0
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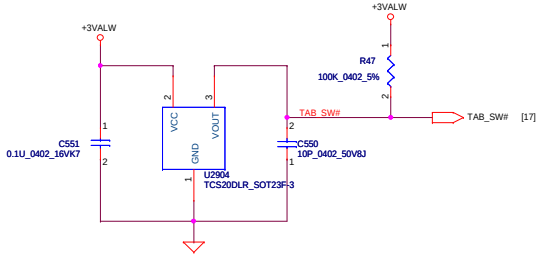
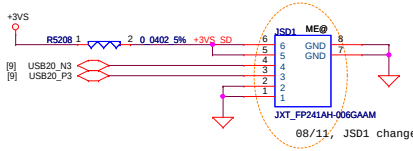
Lid SW(Tablet Mode)

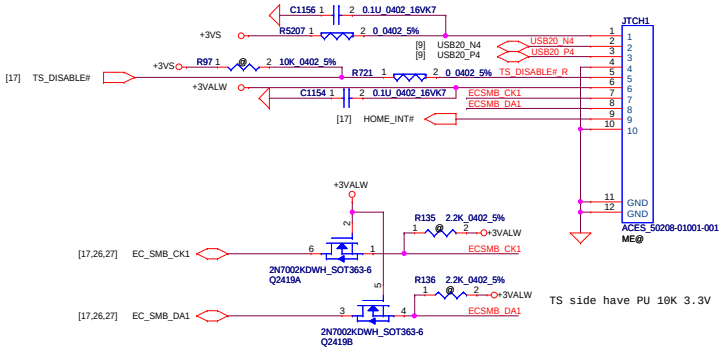


SD Board



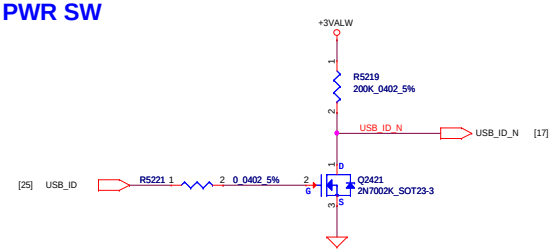
08/11, JSD1 change to 6pin, add one power and gnd pin

Touch Panel



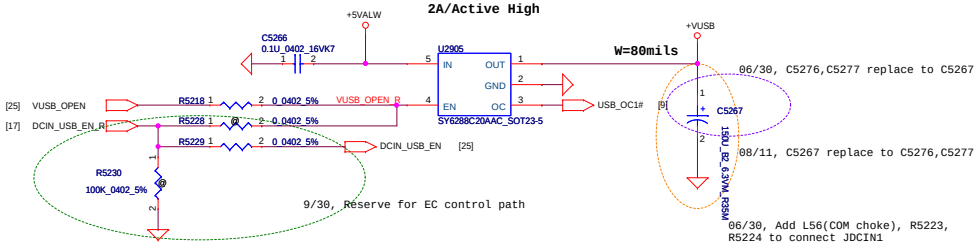
TS side have PU 10K 3.3V

DCIN-USB PWR SW



For DCIN-USB Combo port only

2A/Active High

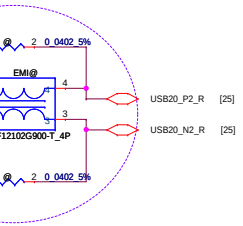


06/30, C5276,C5277 replace to C5267

08/11, C5267 replace to C5276,C5277

9/30, Reserve for EC control path

06/30, Add L56(COM choke), R5223, R5224 to connect JDCIN1

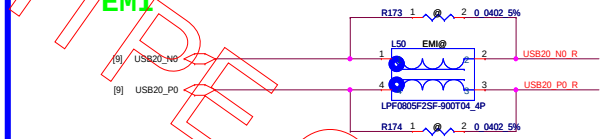


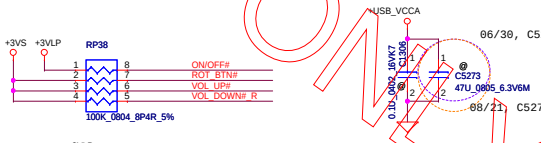
	AC S0	AC S3	AC S5
USB_ID_N	L	L	L
DCIN_USB_EN	L	L	L
VUSB_OPEN	L	L	L
	DC S0	DC S3	DC S5
USB_ID_N	H	H	L
DCIN_USB_EN	H	L	L
VUSB_OPEN	H	H	L
	DC to AC S0	DC to AC S3	DC to AC S5
USB_ID_N	H-->L	H-->L	L-->L
DCIN_USB_EN	H-->L	L-->L	L-->L
VUSB_OPEN	H-->L	H-->L	L-->L
	AC to DC S0	AC to DC S3	AC to DC S5
USB_ID_N	L-->H	L-->H	L-->L
DCIN_USB_EN	L-->H	L-->L	L-->L
VUSB_OPEN	L-->H	L-->H	L-->L

AC to DC S0
When EC get USB_ID_N L--> H, then
DCIN_USB_EN need delay 2's then L-->H

I/O Board

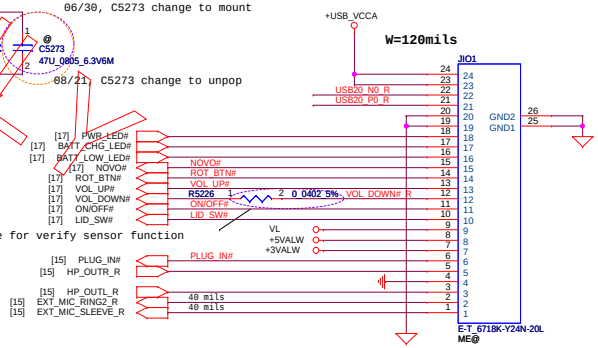
EMI





06/30, C5273 change to mount

08/21, C5273 change to unpop



07/01, Reserve for verify sensor function

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	IO BD/ SD BD/TOUCH/LED/LID		
Size C	Document Number LA-B921PR10		Rev 1.0
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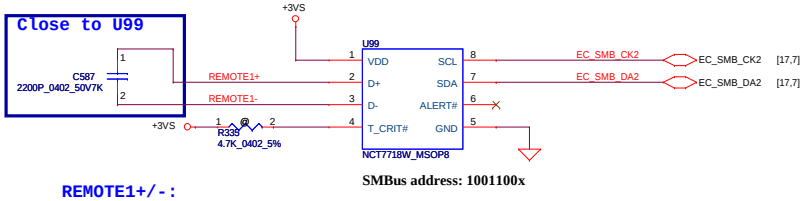
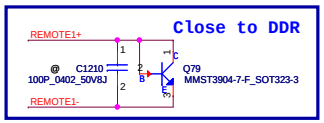
Thermal Sensor

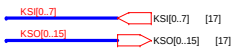


SMBus address: 1001100x

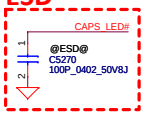
REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"

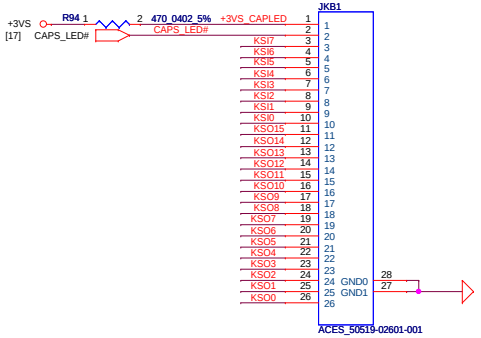


Keyboard



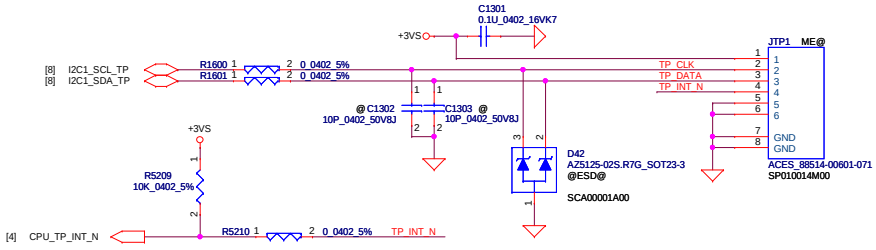
ESD





PIN1	+3VALW
PIN2	CAP_LED
PIN3	KSI7
PIN4	KSI6
PIN5	KSI5
PIN6	KSI4
PIN7	KSI3
PIN8	KSI2
PIN9	KSI1
PIN10	KSI0
PIN11	KSO15
PIN12	KSO14
PIN13	KSO13
PIN14	KSO12
PIN15	KSO11
PIN16	KSO10
PIN17	KSO9
PIN18	KSO8
PIN19	KSO7
PIN20	KSO6
PIN21	KSO5
PIN22	KSO4
PIN23	KSO3
PIN24	KSO2
PIN25	KSO1
PIN26	KSO0

Click Pad



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **KB/TP/Thermal Sensor**

Size: Custom	Document Number: LA-B921PR10	Rev: 1.0
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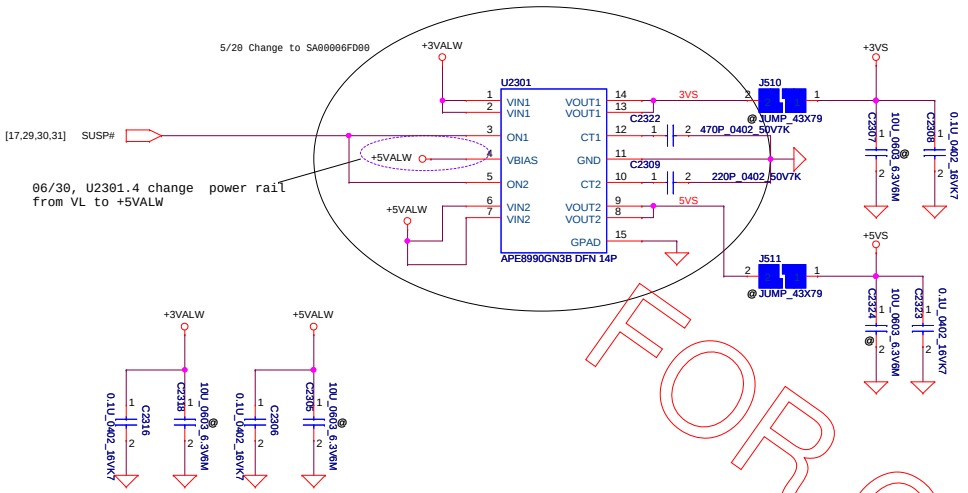
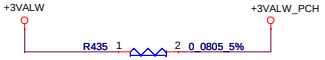
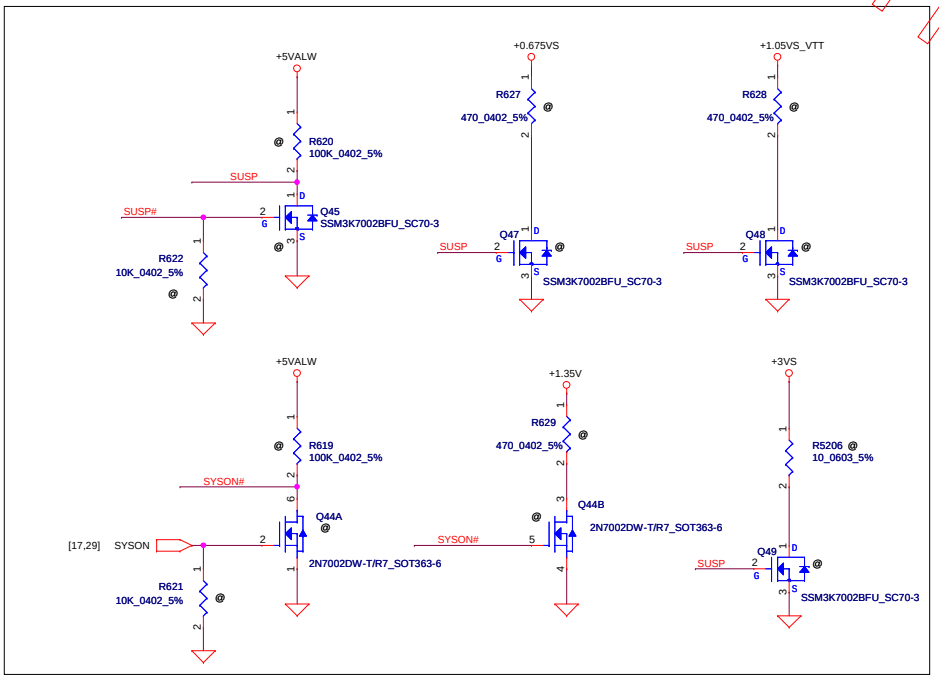
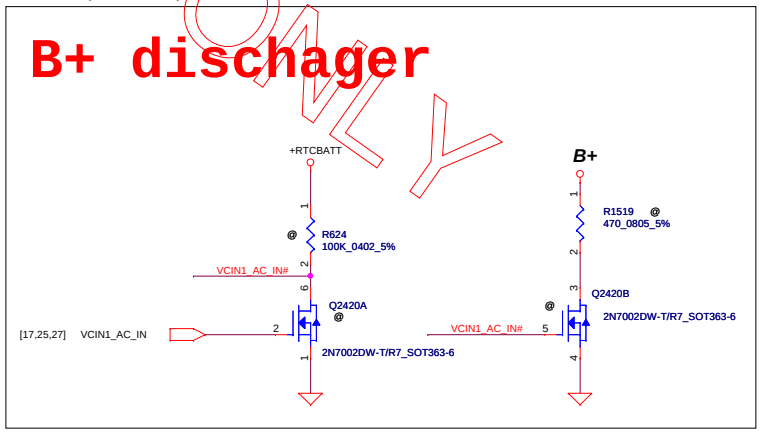
+5VALW TO +5VS
+3VALW TO +3VS







Use for panel sequence



Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.

Title: **DC V TO VS INTERFACE**

Size	Document Number	Rev
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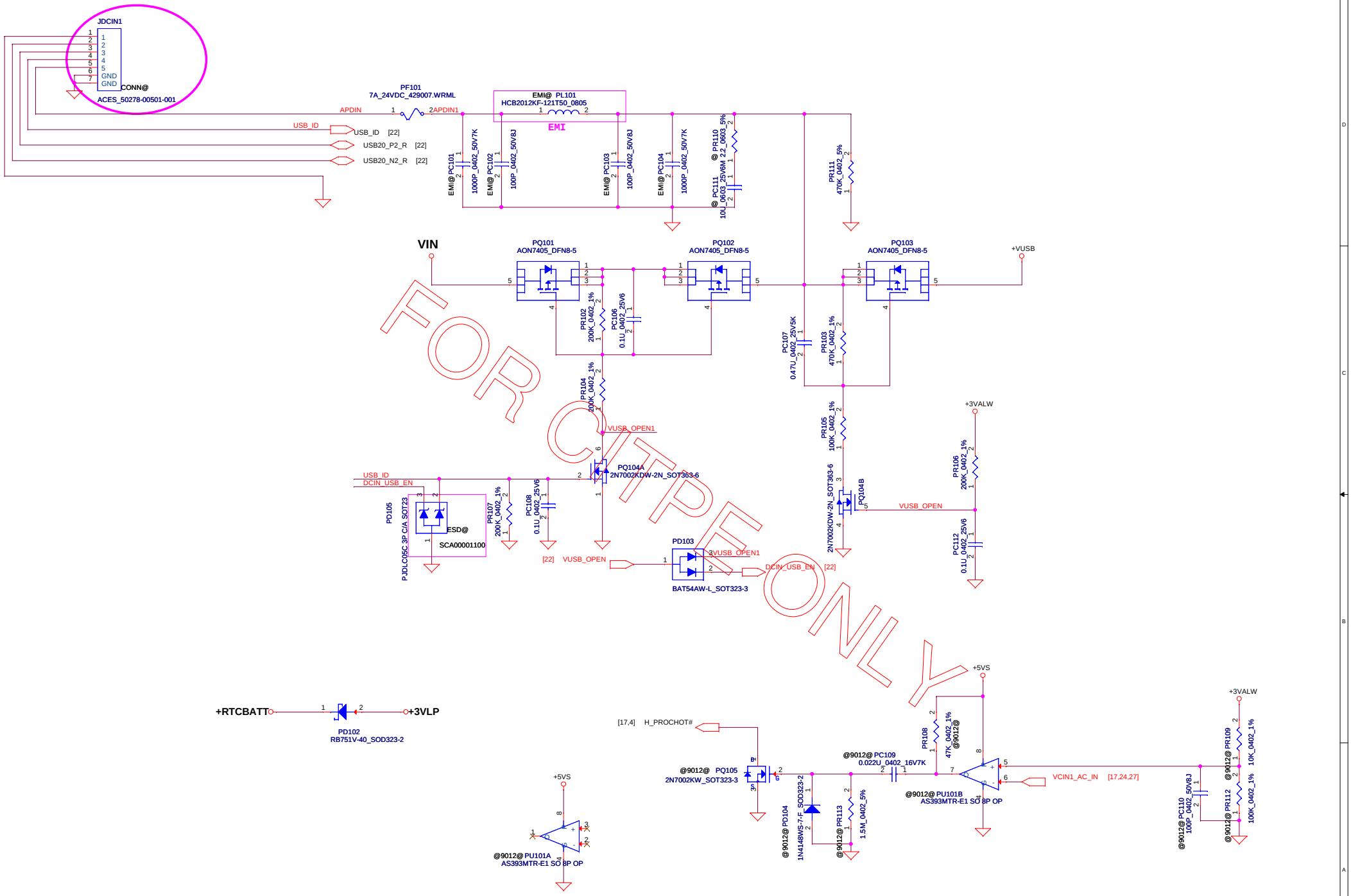


Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.

Title: PWR-DCIN / Vin Detector

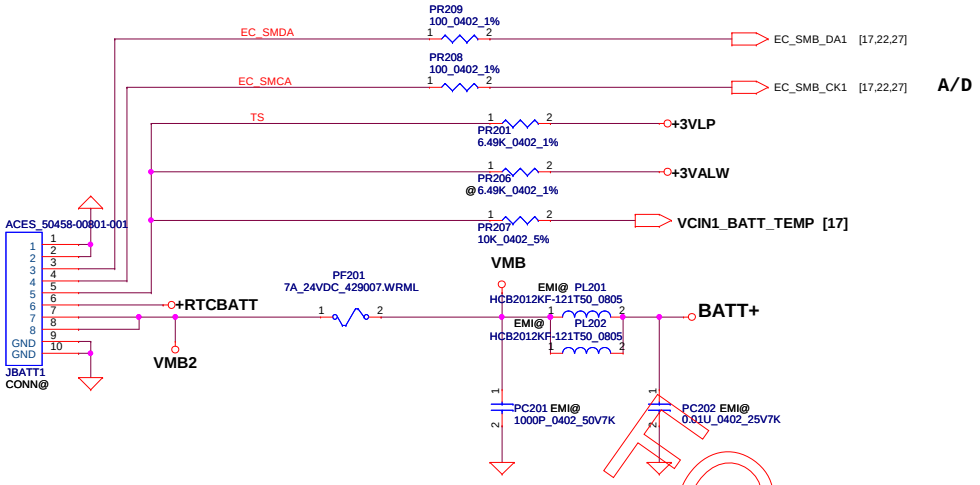
Size: Custom | Document Number: YOGA Paganini | Rev: 1.0

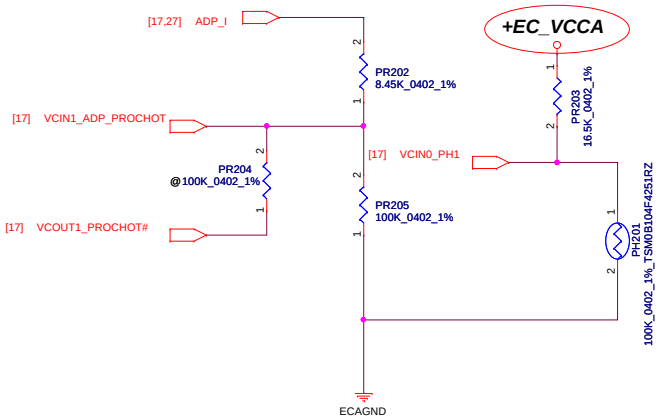
Date: Friday, October 17, 2014 | Sheet 25 of 36

PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

65W(UMA): 85W active W recovery

20120314
Change to +EC_VCCA from +3VLP





Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: YOGA Paganini | Rev: 1.0

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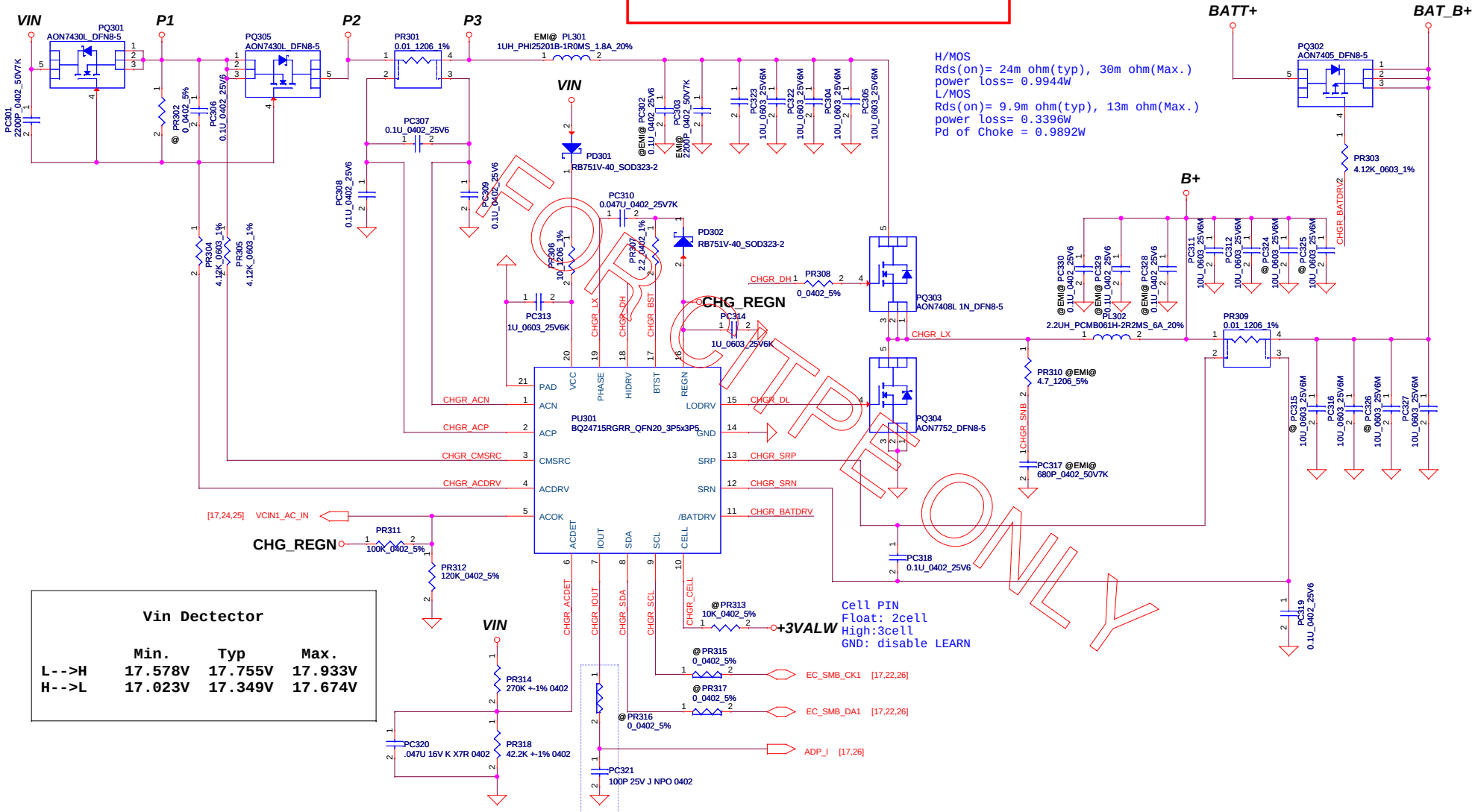
Module model information

BQ24715_V2.mdd

65W adapter support NVDC
BQ24715 support 2, 3 cell
BQ24717 for 4 cell



Vin Dectector

	Min.	Typ	Max.
L-->H	17.578V	17.755V	17.933V
H-->L	17.023V	17.349V	17.674V

Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.	
Title	PWR-CHARGER
Size	Document Number: YOGA Paganini
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Date:	Friday, October 17, 2014
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Module model information

SYX196B_V4.mdd

EN1 and EN2 dont't floating

3.3V LDO 150mA~300mA

PU401 SYX196BQNC_QFN10_3X3

Check pull up resistor of SPOK at HW side

Vout is 3.234V~3.366V

TDC=6A

[17] EC_ON

[17] VCOUT0_MAIN_PWR_ON

EN1 and EN2 dont't floating

Vout is 4.998V~5.202V

TDC=6A

PU402 SYX196C1QNC_QFN10_3X3

5V LDO 150mA~300mA

Module model information

SYX196C_V4.mdd

Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.

Title: PWR-3VALW/5VALW

Size: Custom | Document Number: YOGA Paganini | Rev: 1.0

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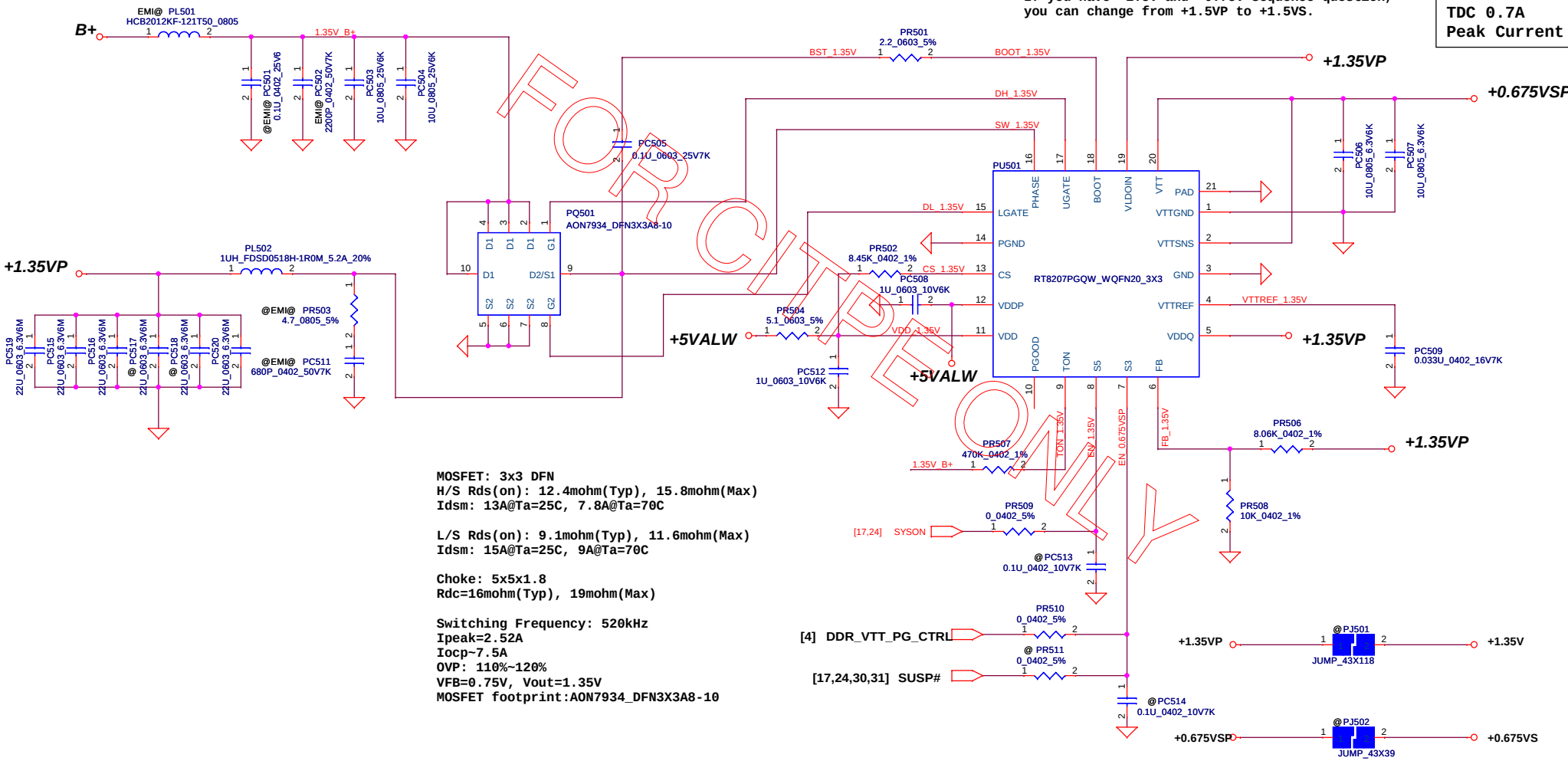
Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



MOSFET: 3x3 DFN
H/S Rds(on): 12.4mohm(Typ), 15.8mohm(Max)
Idsm: 13A@Ta=25C, 7.8A@Ta=70C

L/S Rds(on): 9.1mohm(Typ), 11.6mohm(Max)
Idsm: 15A@Ta=25C, 9A@Ta=70C

Choke: 5x5x1.8
Rdc=16mohm(Typ), 19mohm(Max)

Switching Frequency: 520kHz
Ipeak=2.52A
Iocp~7.5A
OVP: 110%~120%
VFB=0.75V, Vout=1.35V
MOSFET footprint:AON7934_DFN3X3A8-10

Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.

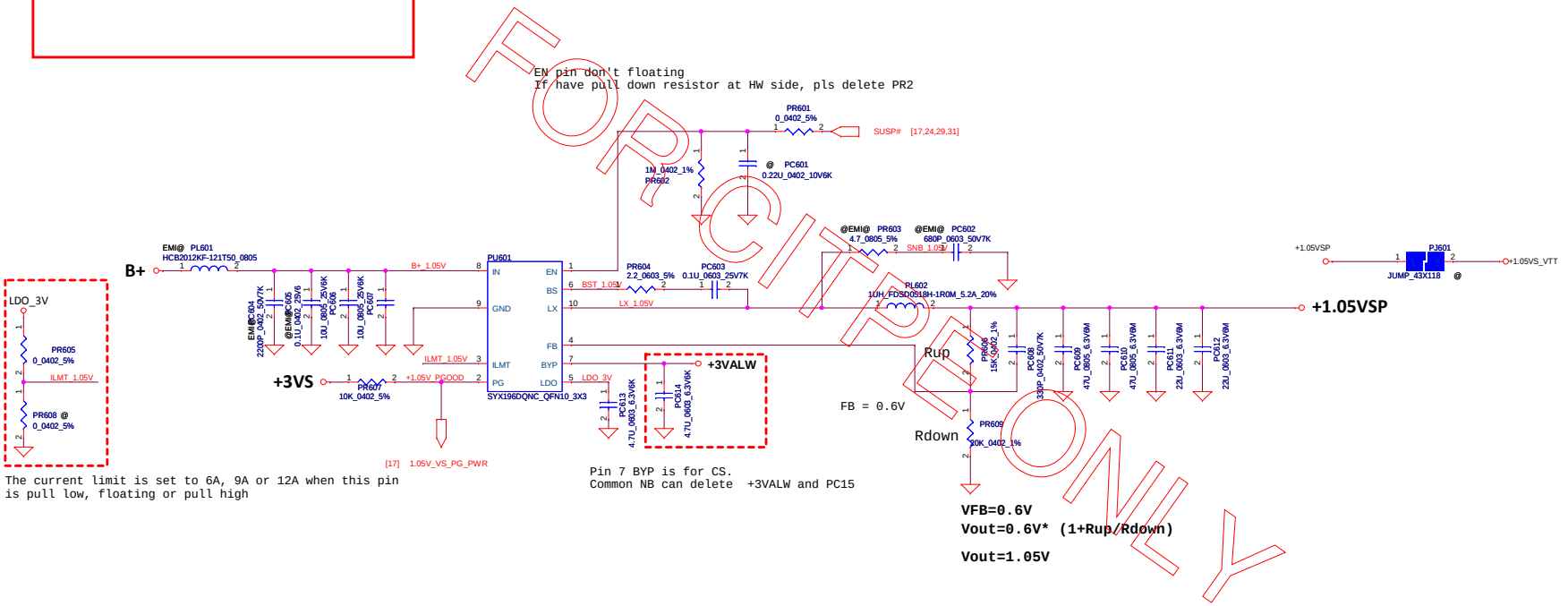
Title: PWR-1.35V/0.675VS

Size: Custom | Document Number: YOGA Paganini | Rev: 1.0

Date: Friday, October 17, 2014 | Sheet 29 of 36

Module model information

SYX196D_V3.mdd



Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.

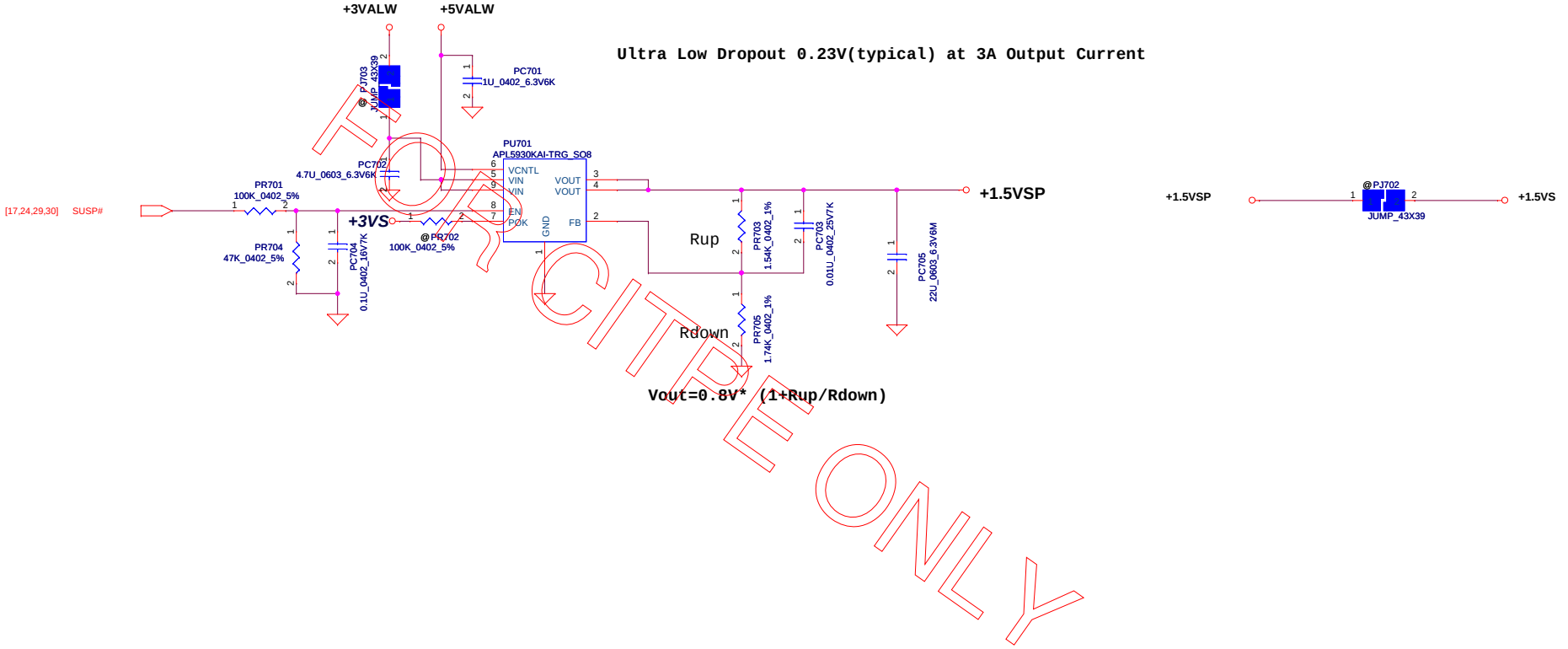
Title: PWR-1.05VS

Size: C | Document Number: YOGA Paganini | Rev: 1.0

Date: Friday, October 17, 2014 | Sheet 30 of 36

Module model information

APL5930_V2.mdd



Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.			
Title	PWR-1.5VS		
Size: Custom	Document Number: YOGA Paganini		Rev: 1.0
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Module model information:
ISL95813_V1A for IC module
ISL95813_V1B for SW module

Base on BDW PDDG Rev_1.2		
Location	4.5W TDC 8A MAX 18A OCP 27A Loadline=-2.0mv/A	Note
PR820	1.27K Ohm	OCP
PR816	909 Ohm	Droop
PC816	0.047uF	RC Match
PR803	73.2kOhm	PROG1
PR806	102kOhm	IMON
PC817	@	RC Filter

Dual MOS: AON6932A
Rds(on):
@Vgs=10V
Q1=4.1mohm
Q2=1.7mohm
@Vgs=4.5V
Q1=6.7mohm
Q2=2.4mohm

Choke: 0.22UH (Size:7*7*1.8)
Rdc=4.3m ohm +-5%
Heat Rating Current=14A

+1.05VS_VTT
Follow intel guideline
PR801 130_0402_1%
PR802 54.9_0402_1%
PC801 1U_0402_6.3V6K

Note:
VR_SVID_ALRT# Pull high on HW side

[10] VR_SVID_DAT
[10] VR_SVID_ALRT#
[10] VR_SVID_CLK
[10] VR_ON
[10] VGATE
[17] IMON_CPU
[17] VR_HOT#
[10] VCCSENSE
[12] VSSSENSE

PR803 73.2K_0402_1%
Note:
PR803=73.2K
=>Icc(max)=18A
fsw=700KHz

PR804 1.5K_0402_1%
PC807 1000P_0402_50V7K
PR806 102K_0402_1%
Note:
VR_HOT# Pull high on HW side

PU801
ISL95813HRZ-T_QFN20_3X4
PAD, SCLK, ALERT#, SDA, PRGM1
VR_ON, PGOOD, IMON, VR_HOT#, NTC, COMP
LGATE, PHASE, UGATE, BOOT, VCC, PRGM2
FB, RTN, ISUMN, ISUMP

PR805 0_0603_5%
PQ801 AON6932A_DFN5X6-8-7
PR807 2.2_0603_5%
PC808 0.22U_0603_16V7K
PC810 0.1U_0402_25V6
PR811 124K_0402_1%
Note:
PR512=124K
=>Slew rate=53mV/us
Vboot = 1.7V

CPU_B+
EMI@ PL801 HCB2012KF-121T50_0805
B+
PC802 10U_0603_25V6M
PC803 10U_0603_25V6M
@EMI@ PC804 0.1U_0402_25V6
EMI@ PC805 220P_0402_50V7K
PC806 100U_D2_16VM_R50M

PL802 0.22UH_PCMB061H-R22MS4R305_14A_20%
+CPU_CORE
+5VS
PR812 3.65K_0603_1%
@EMI@ PR810 4.7_0805_5%
@EMI@ PC811 680P_0603_50V7K

PH801 470K_0402_5%_B25/50 4700K
PR808 3.83K_0402_1%
PR809 27.4K_0402_1%
PC809 47P_0402_50V8J

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92v, recovery

PR813 3.65K_0402_1%
PC812 33P_0402_50V8J
PC813 6800P_0402_25V7K
@ PR815 10_0402_1%
@ PC815 390P_0402_50V7K
PR816 909_0402_1%
Droop

@ PR817 4.99M_0402_1%
RC Match
PC816 0.047U_0402_25V7K
PC817 @ 0.1U_0402_16V4Z
PR818 2.61K_0402_1%
PR819 11K_0402_1%
PH802 10K_0402_5%_B25/50 4250K

@PC818 330P_0402_50V7K
@ PC819 0.082U_0402_16V7K
PC820 0.01U_0402_50V7K

OCP Setting
PR820 1.27K_0402_1%

@PC821 4700P_0402_25V7K
@PR821 1.5K_0402_1%

Local sense put on HW site

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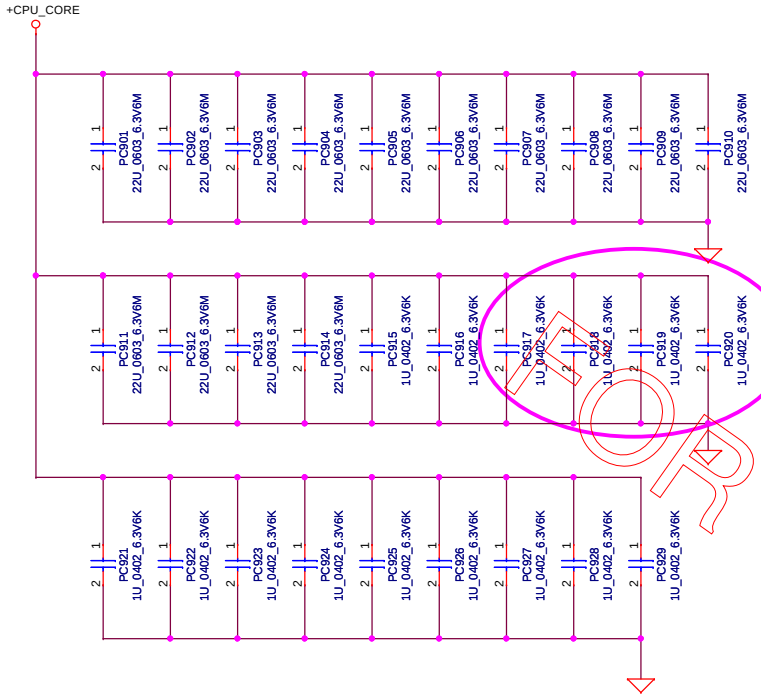
CPU_CORE output cap-->36.4



30 X 22uF 0805
2012/10/23
check the output cap Qty!!!
2012/10/24
23 pcs 22uF and reserve 7 pcs
2013/01/14
22uF*15; reserve 22uF*5

2013/09/6 22U_0603x17 + 22U_0805x2

Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.

Title: ***PROCESSOR DECOUPLING***

Size | Document Number: YOGA Paganini | Rev: 1.0

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Version change list (P.I.R. List)

Item	Reason for change	PAGE	Modify List	Date	Phase

Security Classification	Compal Secret Data		
Issued Date	2014/04/10	Deciphered Date	2017/04/10

Compal Electronics, Inc.

Title: **PWR-PIR**

Size: Custom | Document Number: YOGA Paganini | Rev: 1.0

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase	Verify
1	ME Request	P.20	H1,H2,H3 footprint change to H_3P3, Delete H6	2014-06-30	EVT-DVT	Pass
2	EMI request, for DCIN-USB port USB signal	P.22	Add L56(COM choke), R5223, R5224 to connect JDCIN1	2014-06-30	EVT-DVT	EA Pass
3	EMI request	P.15	CA32 replace to RA21, CA33 replace to RA24, CA34 replace to RA25	2014-06-30	EVT-DVT	Pass
4	EMI request	P.10	Reserve RC152 connect to JC1	2014-06-30	EVT-DVT	Pass
5	For fine tune I2C interface driving	P.8	RC130~RC133 change value to 2.2K ohm	2014-06-30	EVT-DVT	EA Pass
6	For ME Z-height limitation	P.19	C5274,C5275 replace to C5264	2014-06-30	EVT-DVT	EA Pass
7	For ME Z-height limitation	P.22	C5276,C5277 replace to C5267, C5273 change to mount	2014-06-30	EVT-DVT	EA Pass
8	For S5 power saving	P.24	U2301.4 change power rail from VL to +5VALW	2014-06-30	EVT-DVT	Pass
9	Reserve path for verify sensor function	P.22	Add 0 ohm R5226 to connect JIO1.12 and U11.85	2014-07-01	EVT-DVT	Pass
10	Reserve path for verify sensor function	P.17	Add 0 ohm R5225 to connect U52.4 and U11.84	2014-07-01	EVT-DVT	Pass
11	Reserve path for verify BT function	P.19	Add PU R5227 to connect BT_DISABLE_R and +3VS	2014-07-01	EVT-DVT	Pass
12	Follow Intel design guide	layout	Voiding the GND plane underneath the SATA signals pad of JSSD1	2014-07-01	EVT-DVT	EA Pass

Item	Reason for change	PG#	Modify List	Date	Phase	Verify
1	Z-high impact for thermal plate	P.11	CC49(22U)(0603) change to 10U*2(CC49,CC100)(0402)	2014-08-13	DVT-PVT	Pass
2	Z-high impact for thermal plate	P.10	CC26, CC27, CC28, CC30 change to 0402 type	2014-08-13	DVT-PVT	Pass
3	Reserve for Intel request	P.13 P.14	ADD CD54, CD55, CD72, CD73 connect to +0.675VS	2014-08-13	DVT-PVT	
4	Reserve for Intel request	P.13 P.14	ADD CD56~CD71,CD74~CD87 connect to +1.35V	2014-08-13	DVT-PVT	
5	Reserve For EMI request	P.15	ADD CA35 connect to DMIC_CLK	2014-08-13	DVT-PVT	
6	solve plug in/out USB device auto shutdown issue	P.19 P.22	C5264 replace to C5274,C5275; C5267 replace to C5276,C5277	2014-08-13	DVT-PVT	Pass
7	For EMI/Audio request, solve audio noise issue	P.15	CA32, CA33, CA34 change to RA41, RA42, RA43	2014-08-13	DVT-PVT	Pass
8	ME request, for FFC 夾持力 issue	P.22	JSD1 connector change symbol 4pin to 6pin	2014-08-13	DVT-PVT	Pass
9	For DFB request	P.19	JWLAN1 change symbol	2014-08-13	DVT-PVT	Pass
10	Reserve For ESD request		Add C5274, CC101, CC102, CD88, PC328, PC329, PC330, PC428,PC429	2014-08-18	DVT-PVT	
11	For ME request	P.20	Fix hole H9 Change to H_4P0, Add H12	2014-08-18	DVT-PVT	
12	For ME request	layout	JEDP1 change location placement	2014-08-18	DVT-PVT	Pass

Item	Reason for change	PG#	Modify List	Date	Phase	Verify
1	ATE request reserve Test point to burn in MAC	P.17	Add T84,T85,T86	2014-09-25	PVT-SOVP	
2	For ME request	layout	JEDP1 change location placement(move down 2mm)	2014-09-25	PVT-SOVP	Verify on SOVP
3	Reserve DCIN USB power SW EC control path	P.22	Add R5228,R5229,R5230 to connect U2905, U11, PD103	2014-09-30	PVT-SOVP	
4	Reserve for ESD protect	P.25	Add DCIN_USB_EN connect to PD105	2014-09-30	PVT-SOVP	

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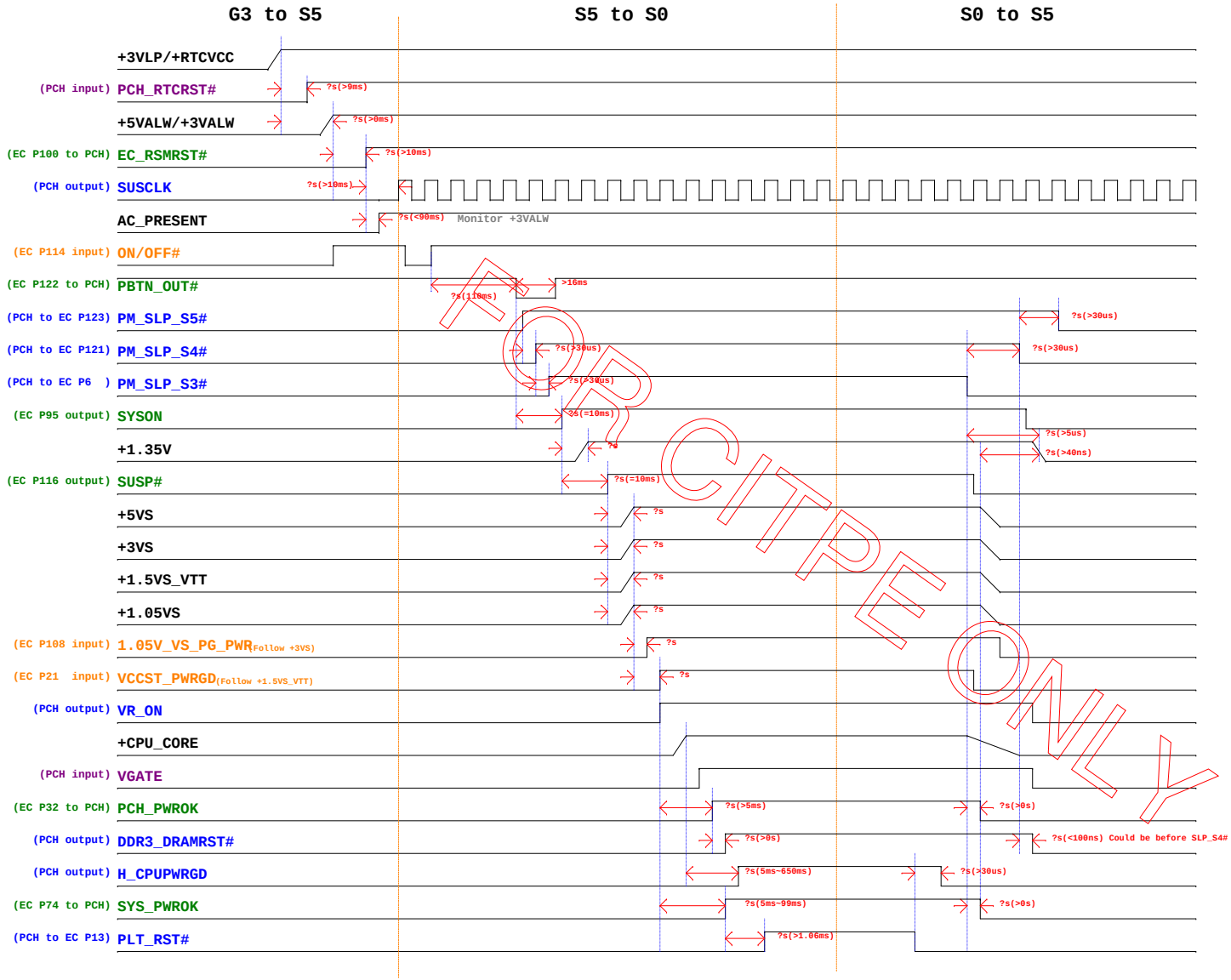
Paganini Power Sequence



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