Compal Confidential

AIWZ0/AIWZ1
DIS M/B Schematics Document

Intel Boardwell U Processor with DDR3L
AMD Meso XT / Tropo XT2

2015-02-02

LA-C281P

REV：1.0

Security Classification	Compal Secret Data		
Issued Date	2014/09/01	Deciphered Date	2015/09/01

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Title: *Cover Page*

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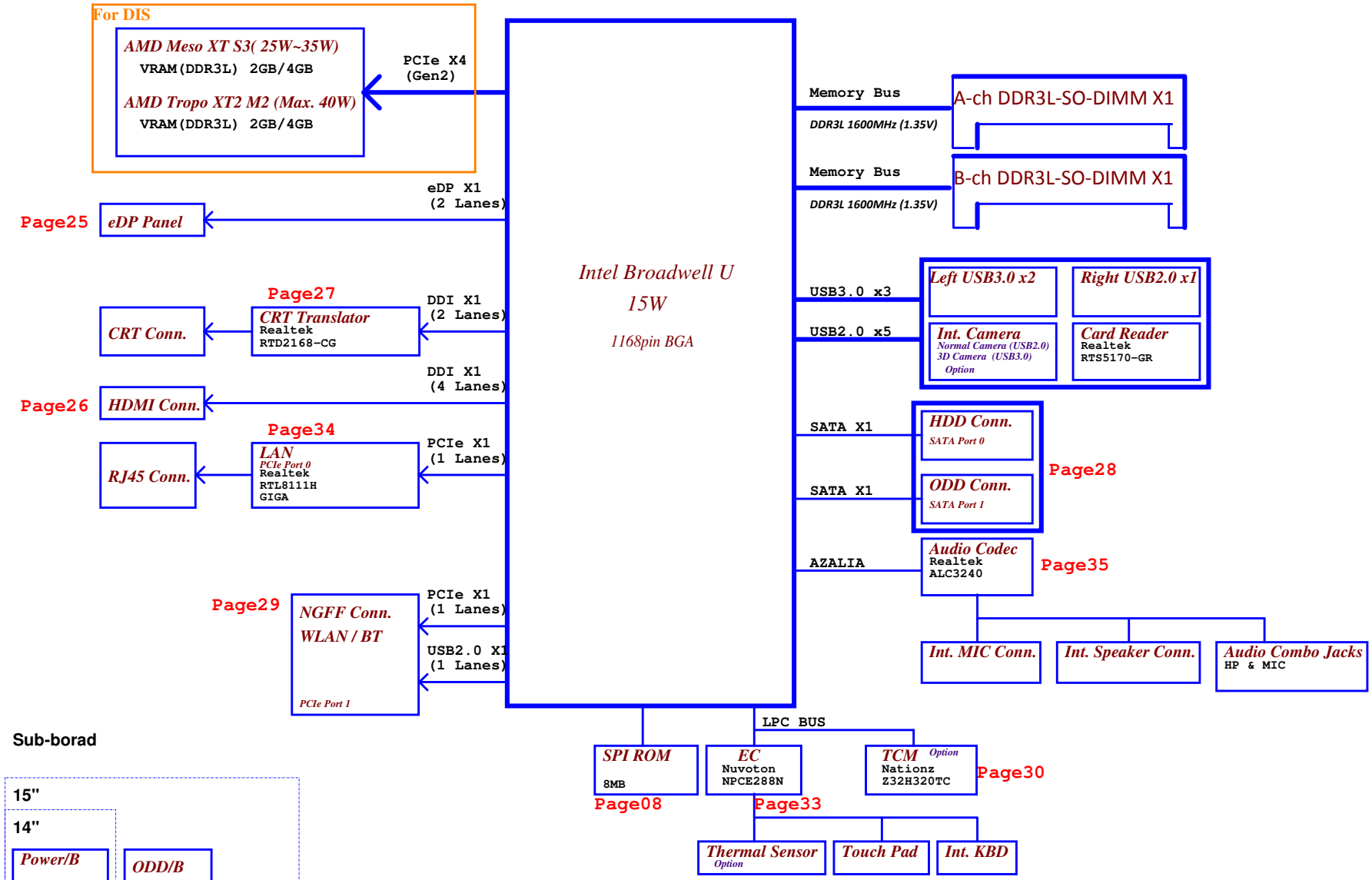

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Title: **MB Block Diagram**

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Voltage Rails

power plane / State	B+	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS +VCC_CORE +VGA_CORE +1.8VS +0.675VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

EC SM Bus2 address

Device	Address
Thermal Sensor	0100 1100

PCH SM Bus address

Device	Address	
DDR_JDIMM1	1010 000x	A0h
DDR_JDIMM2	1010 010x	A4h

AMD-GPU SM Bus address

Device	Address	
Internal thermal sensor	0100 0001	41h

SMBUS Control Table

	SOURCE	CRT	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
EC_SMB_CK1 EC_SMB_DA1	NPCE288 +3VALW	X	V +3VALW	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	NPCE288 +3VS	V +3VS	X	X	X	X	V +3VS	V +3VALW
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	V +3VS	X	X	X
PCH_SML0CLK PCH_SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VGS	X

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
	UHCI1	2	Sub Board
		3	CardReader
	UHCI2	4	Touch Screen
		5	Camera
	UHCI3	6	Bluetooth (NGFF)
		7	
EHCI1	UHCI4	8	
		9	
	UHCI5	10	
		11	
	UHCI6	12	
		13	

BDW_CPU

UC1
SA000089A60 I7-5500U
S IC FH8065801620004 SR23W F0 2.4G C38!
I7_5500@

UC1
SA000089970 I5-5200U
S IC FH8065801620204 SR23Y F0 2.2G C38!
I5_5200@

UC1
SA000089880 I3-5010U
S IC FH8065801620406 SR23Z F0 2.1G C38!
I3_5010@

UC1
SA000083EH0 I3-5005U
S IC FH8065801884006 SR244 F0 2G C38!
I3_5005@

PCB

ZZZ
DAZ1BK00101
PCB AIWZ0 LA-C281P LS-C281P/C282P 02
Z14@
PCB AIWZ0 LA-C281P LS-C281P/C282P 02

ZZZ
DAZ1BJ00101
PCB AIWZ1 LA-C281P LS-C281P/C282P/C283P/C285P/C286P 02
Z15@
PCB AIWZ1 LA-C281P LS-C281P/C282P/C283P/C285P/C286P 02

BOM Structure Table

Item	BOM Structure
AIWZ0 (14")	Z14@
AIWZ1 (15")	Z15@
AIWZ0 (17")	Z17@
LAN Switch mode	SWITCH@
LAN RTL8111GS-CG	8111GLDO@
WLAN Support ISCT	ISCT@
WLAN No Support ISCT	NOISCT@
For Green CLK	GCLK@
For No Green CLK	NOGCLK@
Green CLK IC For DIS	GCLKDIS@
Green CLK IC For UMA	GCLKUMA@
For system DIS	PX@
For TROPO DIS pop	DIS@
For TROPO DIS unpop	@DIS@
For UMA	UMA@
3D Camera	3DCMOS@
Camera	CMOS@
HDMI	HDMI@
NO keyboard backlight	NOKBL@
Keyboard backlight	KBL@
HDMI Royalty	45@
Connector	ME@
Un-pop component for EMI	@EMI@
Un-pop component for ESD	@ESD@
pop component for EMI	EMI@
pop component for ESD	ESD@
Un-pop for TPM	TPM@
pop for TPM	NOTPM@
VRAM indentify	X76@
For TROPO function	TROPO@
ADB function	ADB@
NO ADB function	NOADB@
CPU_SA000083E30	QGZ3@
CPU_SA000083C10	QH17@
CPU_SA00007AM00	QFSY@
CPU_SA000083A10	QH15@
CPU_SA000083D30	QH18@
CPU_SA00007UG00	QGHA@
CPU_SA00007UH00	QGHB@
CPU_SA00007U900	QGH9@

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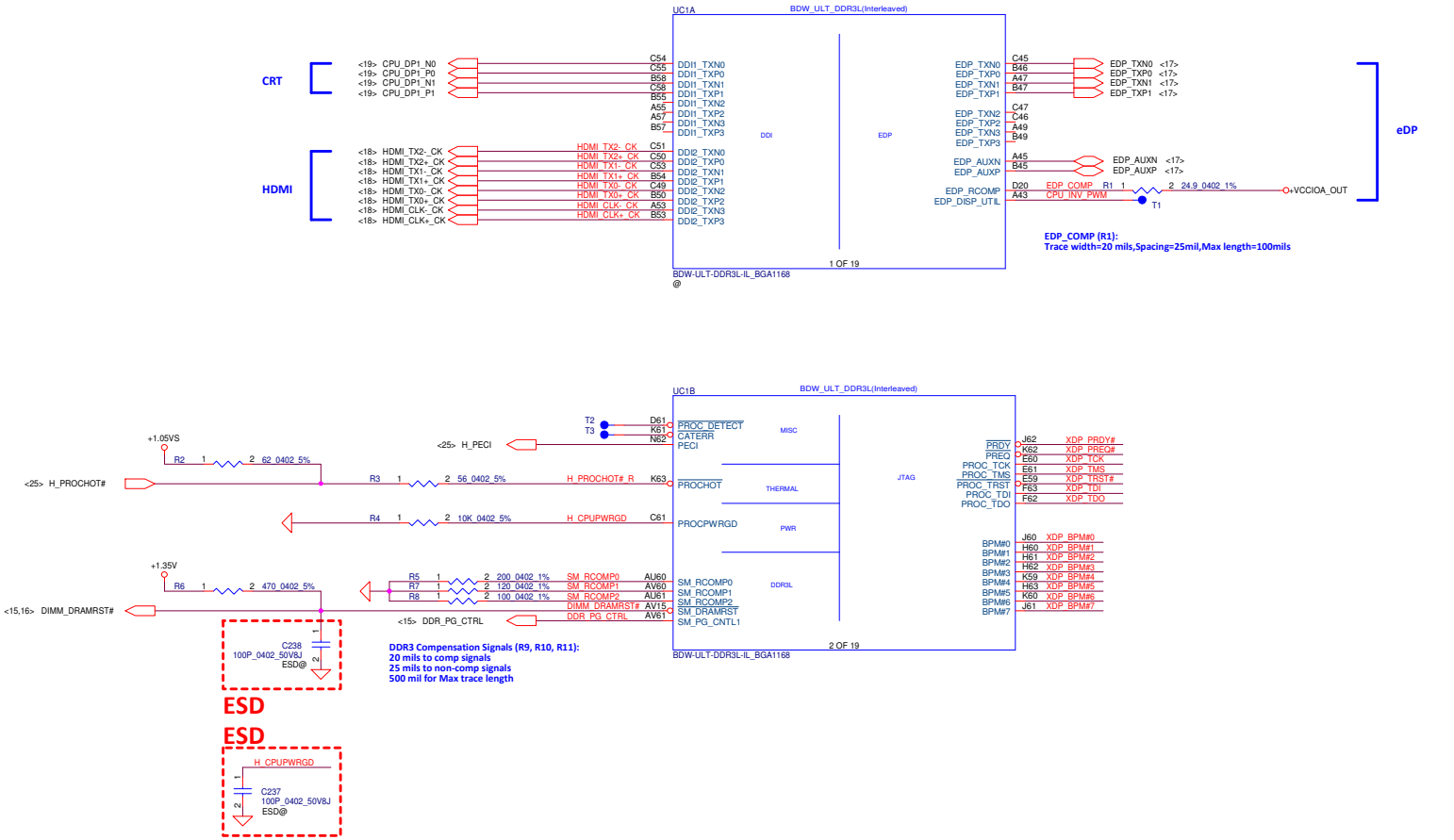

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/09/01	Deciphered Date	2015/09/01	Title: BDW MCP(1/11) DDI,MSIC,XDP
				Size: C; Document Number: LA-C281; Rev: 1.0
				Date: Friday, February 06, 2015; Sheet 4 of 50

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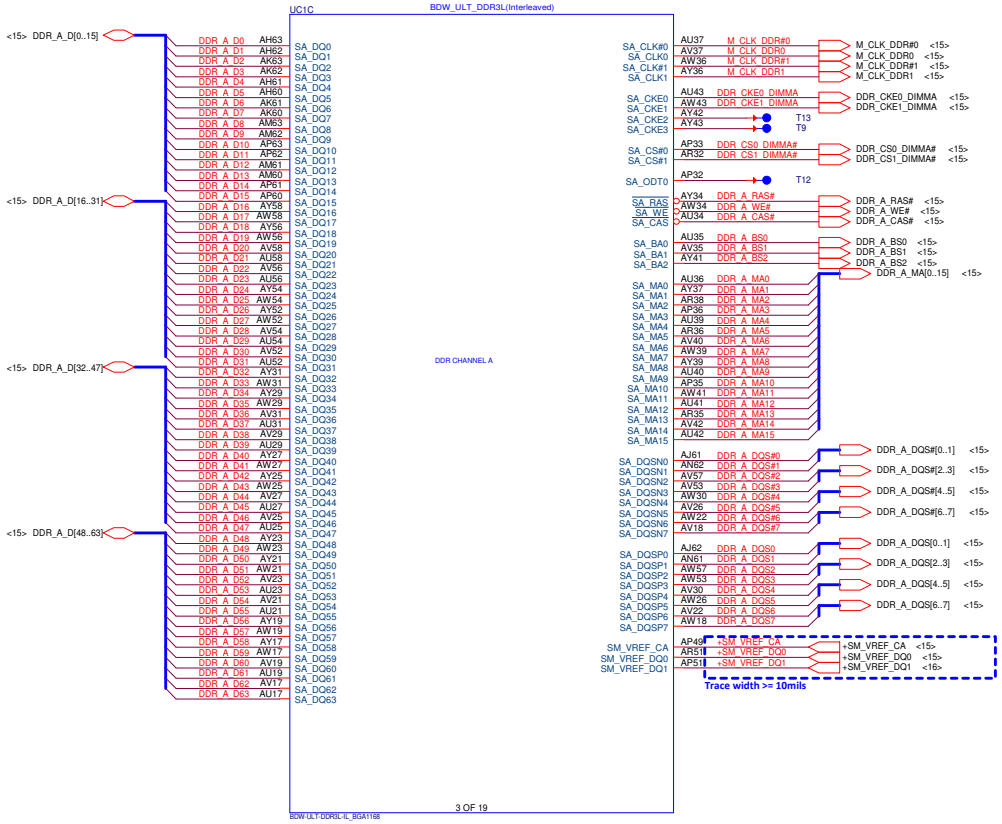
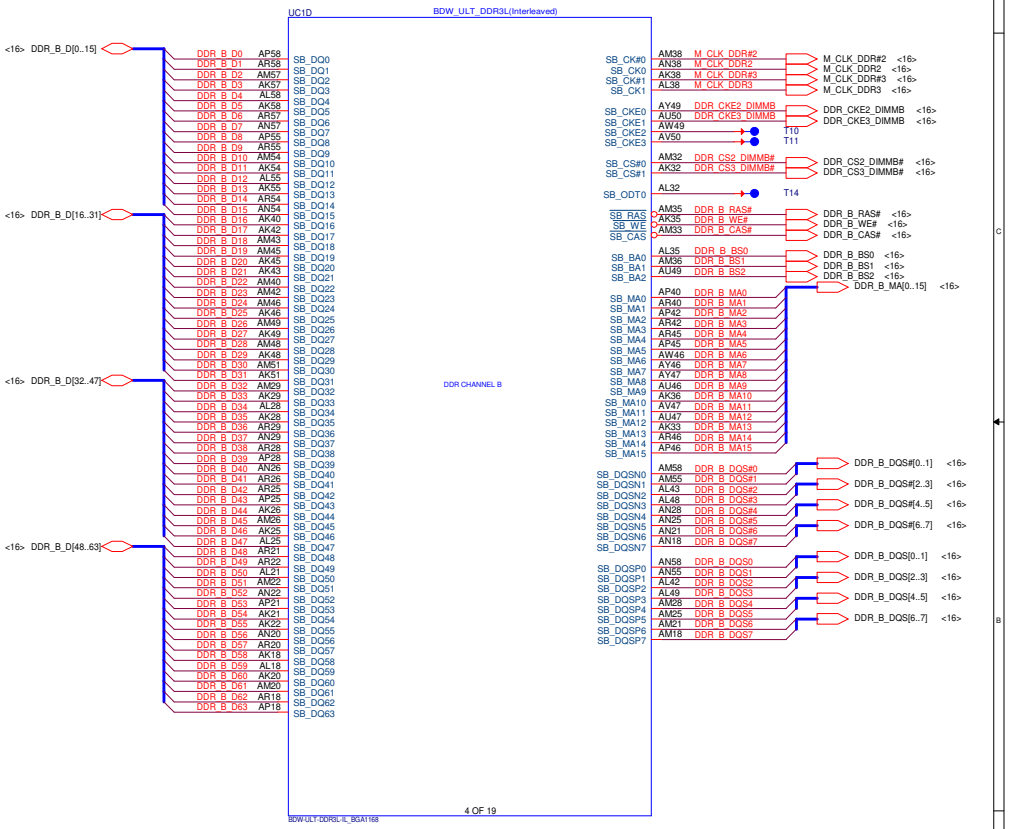
Interleaved Memory





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Issued Date	2014/09/01	Deciphered Date	2015/09/01	Title: BDW MCP(2/11) DDRIII
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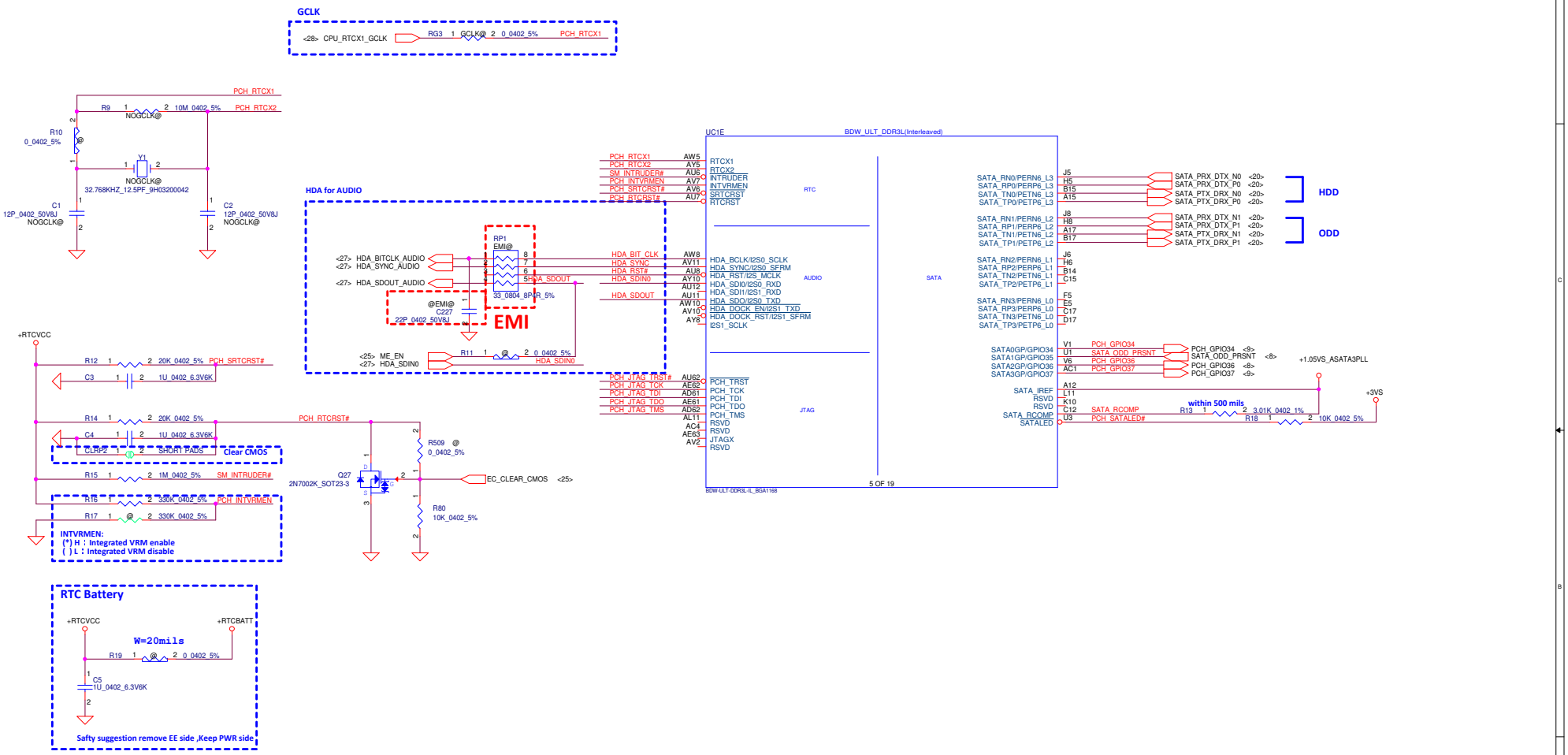

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Issued Date	2014/09/01	Deciphered Date	2015/09/01	Title: BDW MCP(3/11) RTC,SATA,XDP
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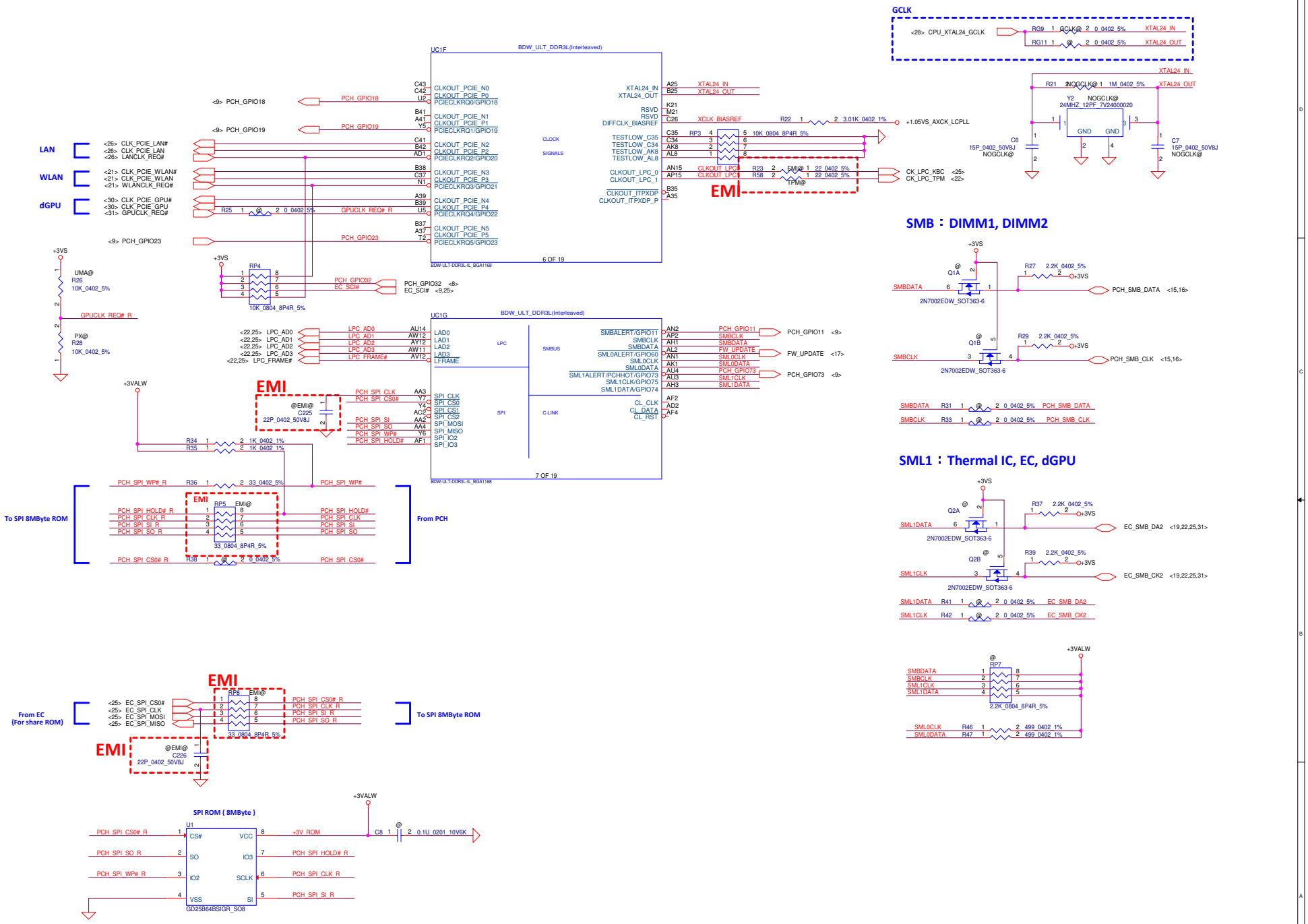

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Title: **BDW MCP(4/11) CLK,SPI,SMBUS**

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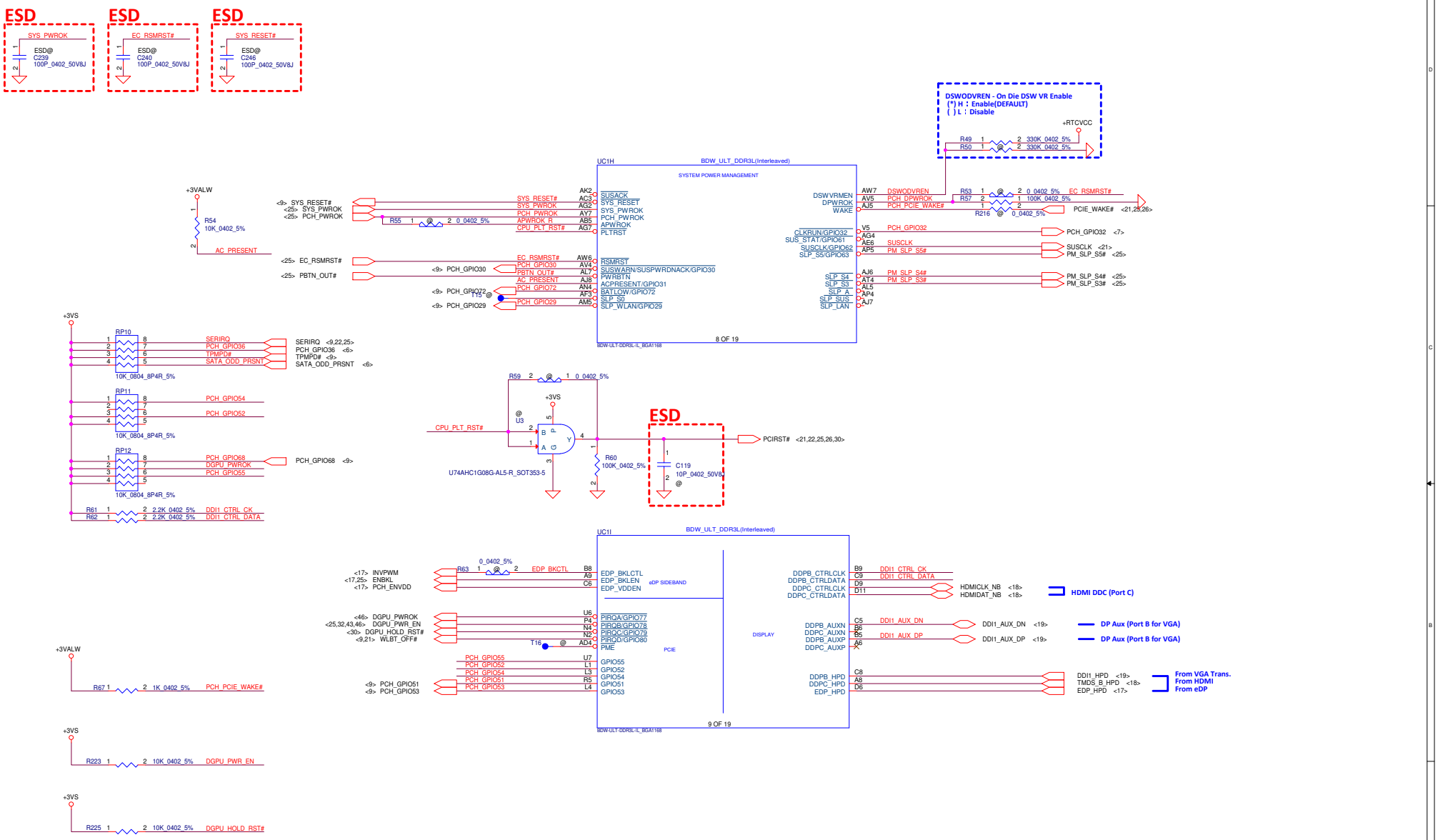

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Issued Date	2014/09/01	Deciphered Date	2015/09/01	Title: BDW MCP(5/11) PM,GPIO,DDI
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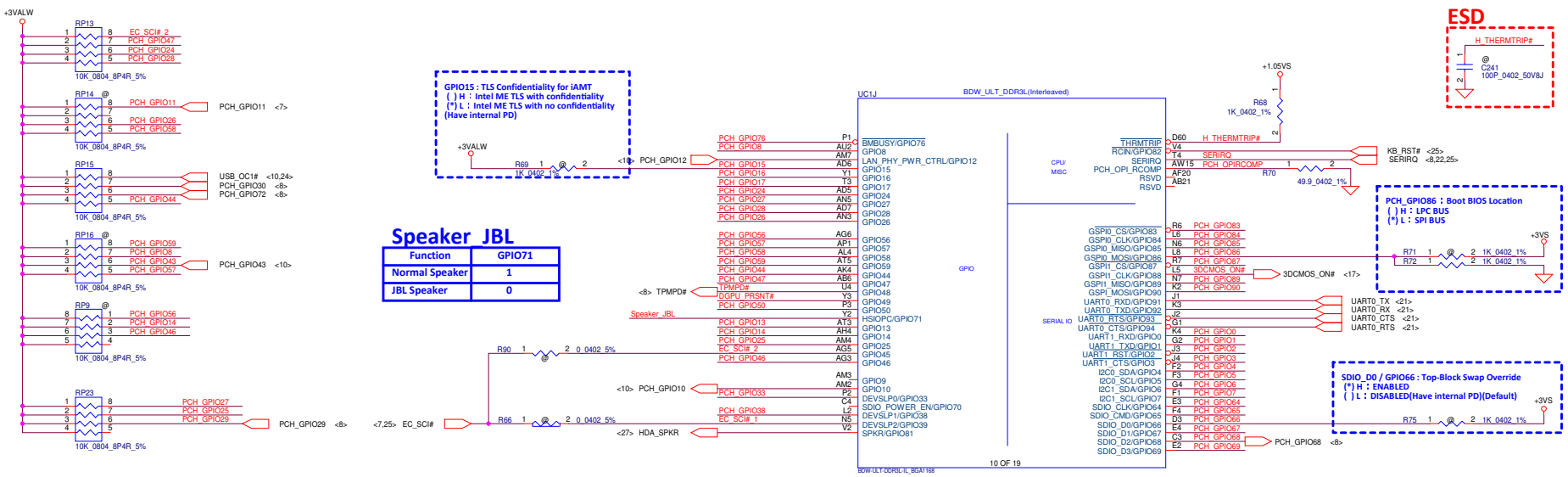

Speaker JBL

Function	GPIO71
Normal Speaker	1
JBL Speaker	0

BIOS Strap Pin

Function	GPIO13
No ISCT	1
ISCT	0

Function	DGPU_PRSNT#(GPIO49)
UMA Only	1
SG	0

Function	GPIO73
3DCMOS@	1
CMOS@	0

Function	GPIO1
14 inch	1
15 inch	0

Function	GPIO38
TPM@	1
NOTPM@	0

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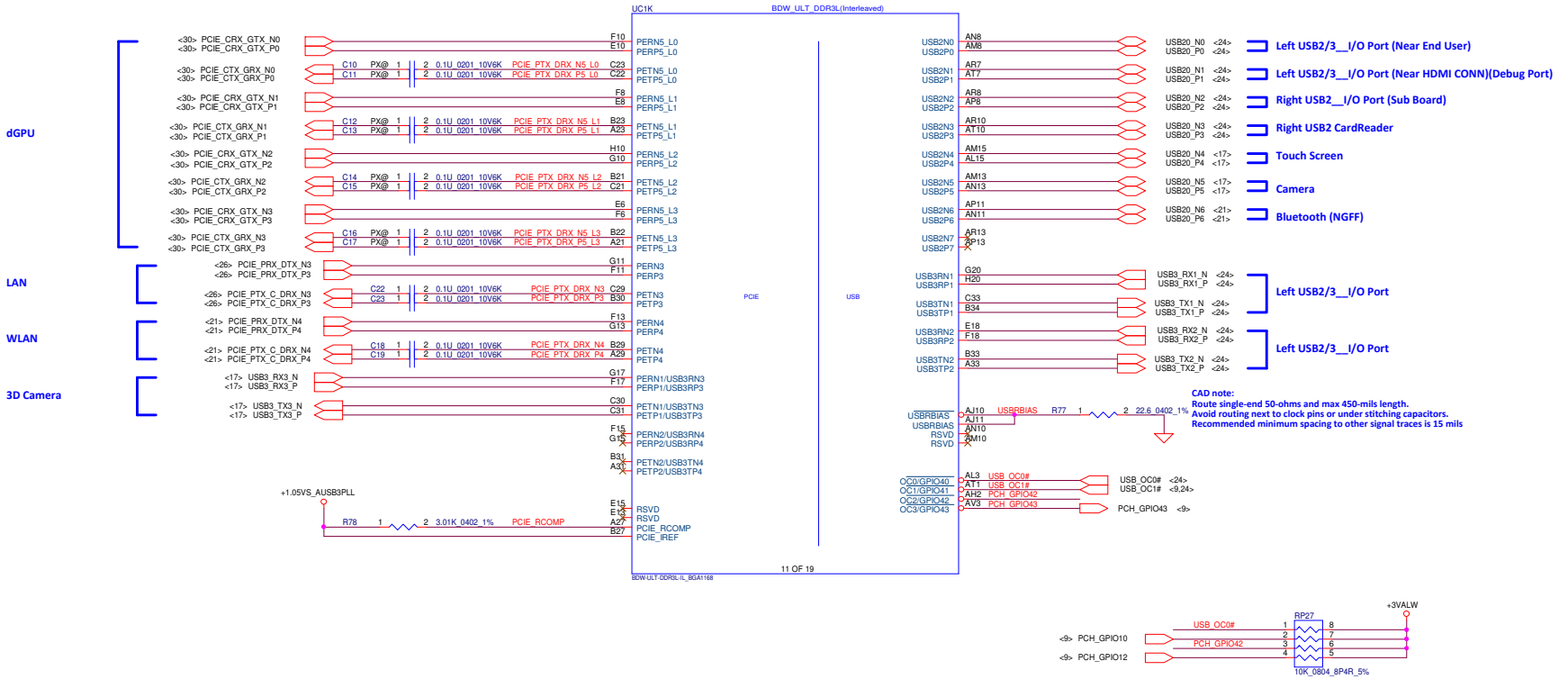

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Title: **BDW MCP(7/11) PCIE,USB**

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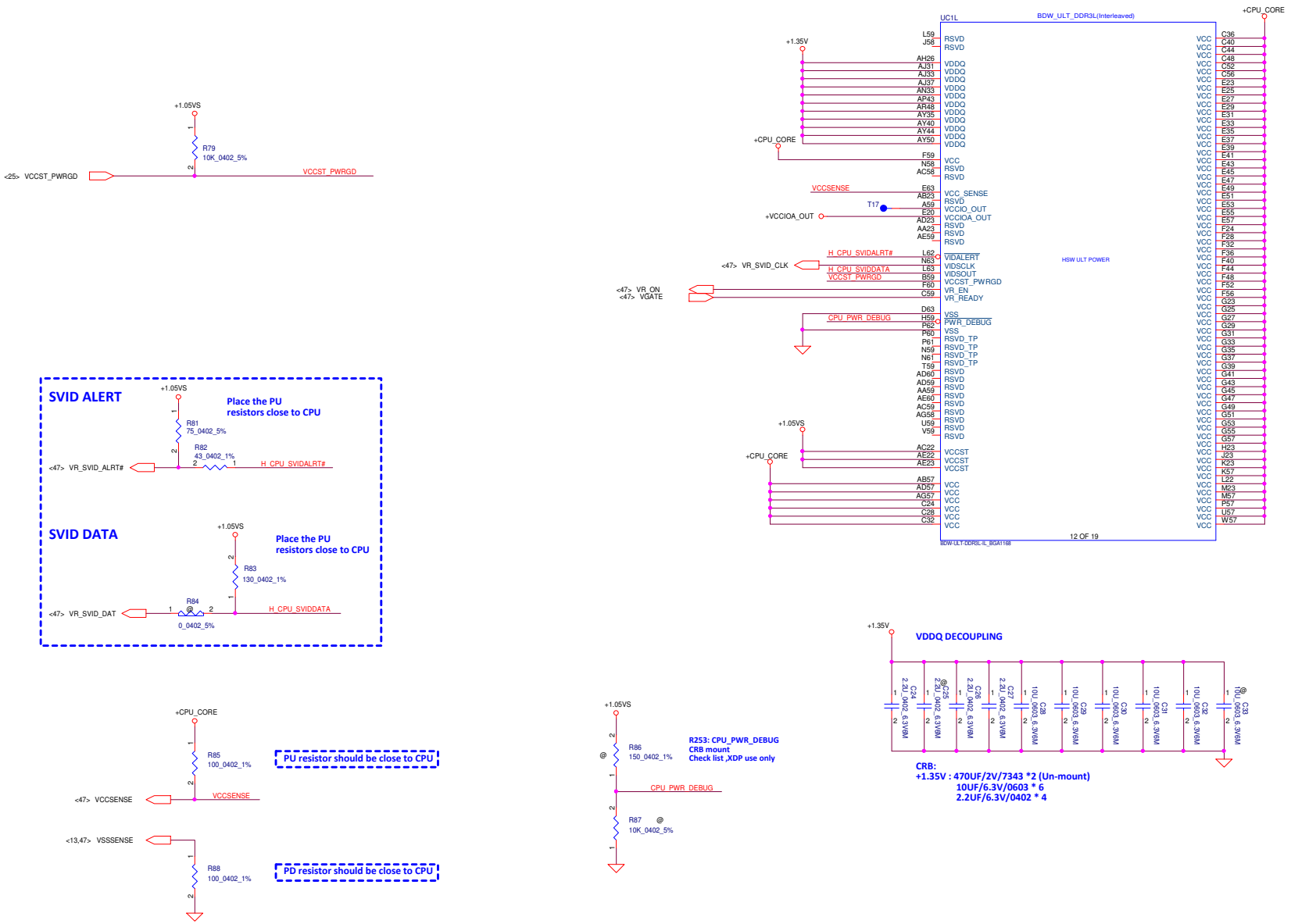

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Title: **BDW MCP(8/11) Power**

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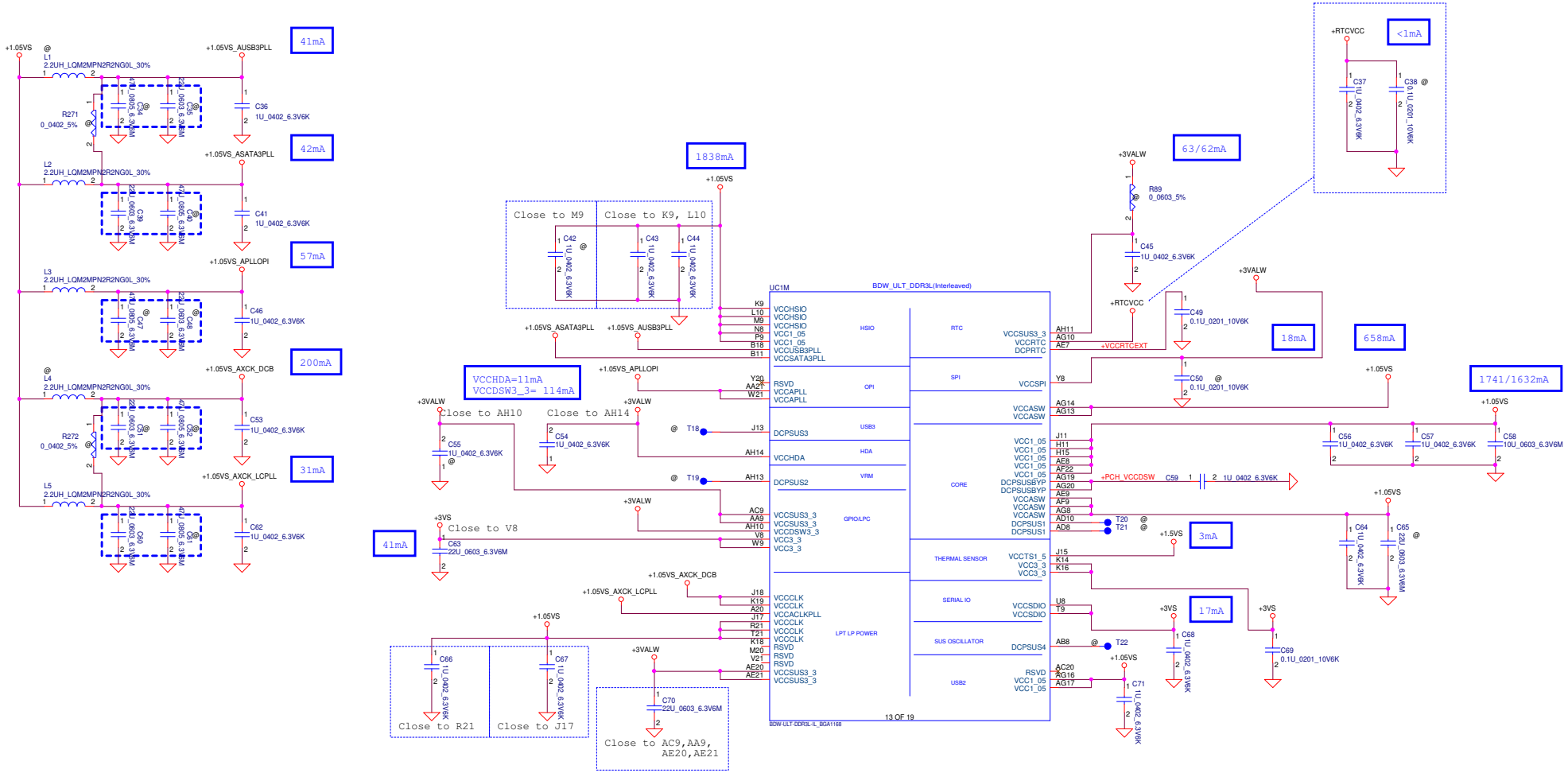

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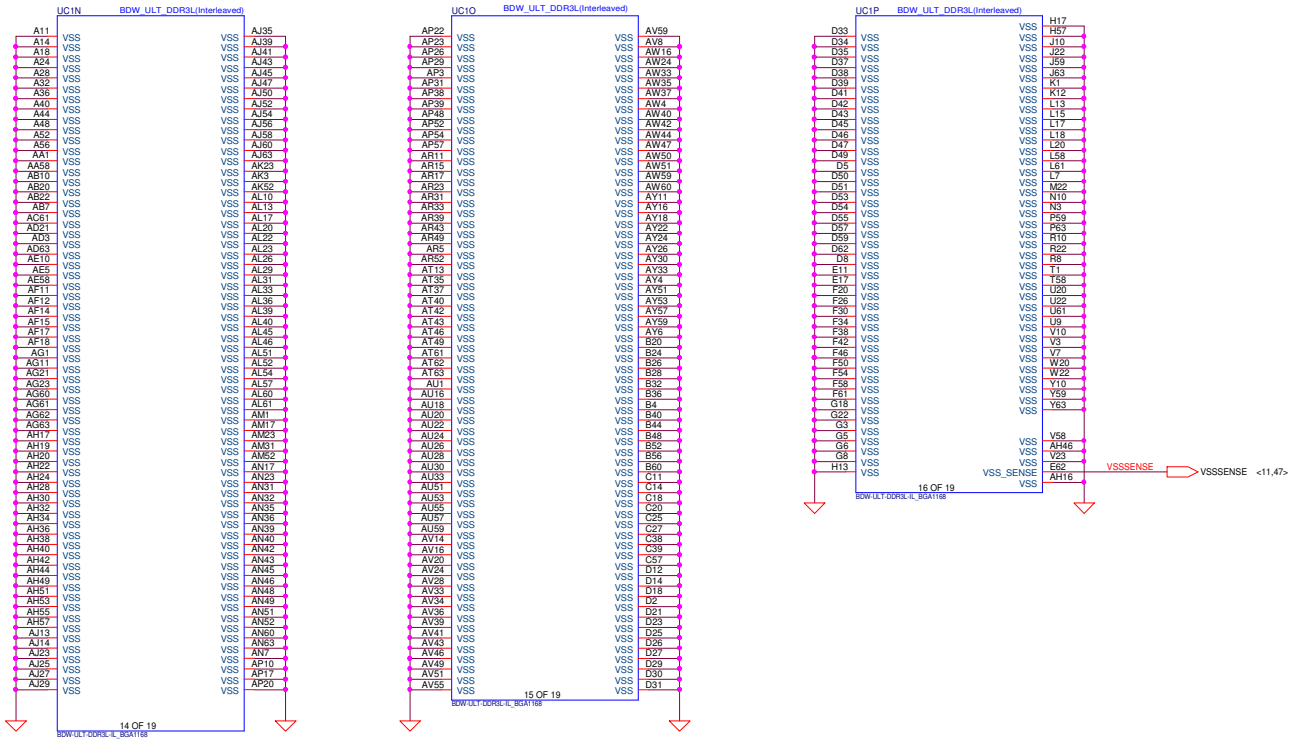

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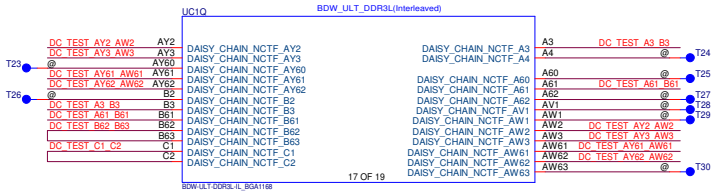
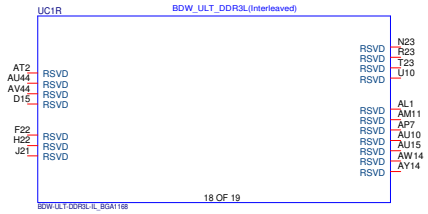
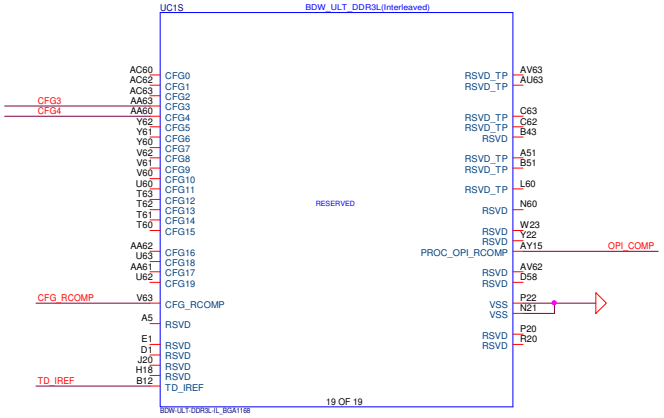
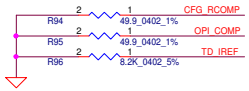
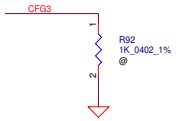




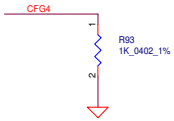




CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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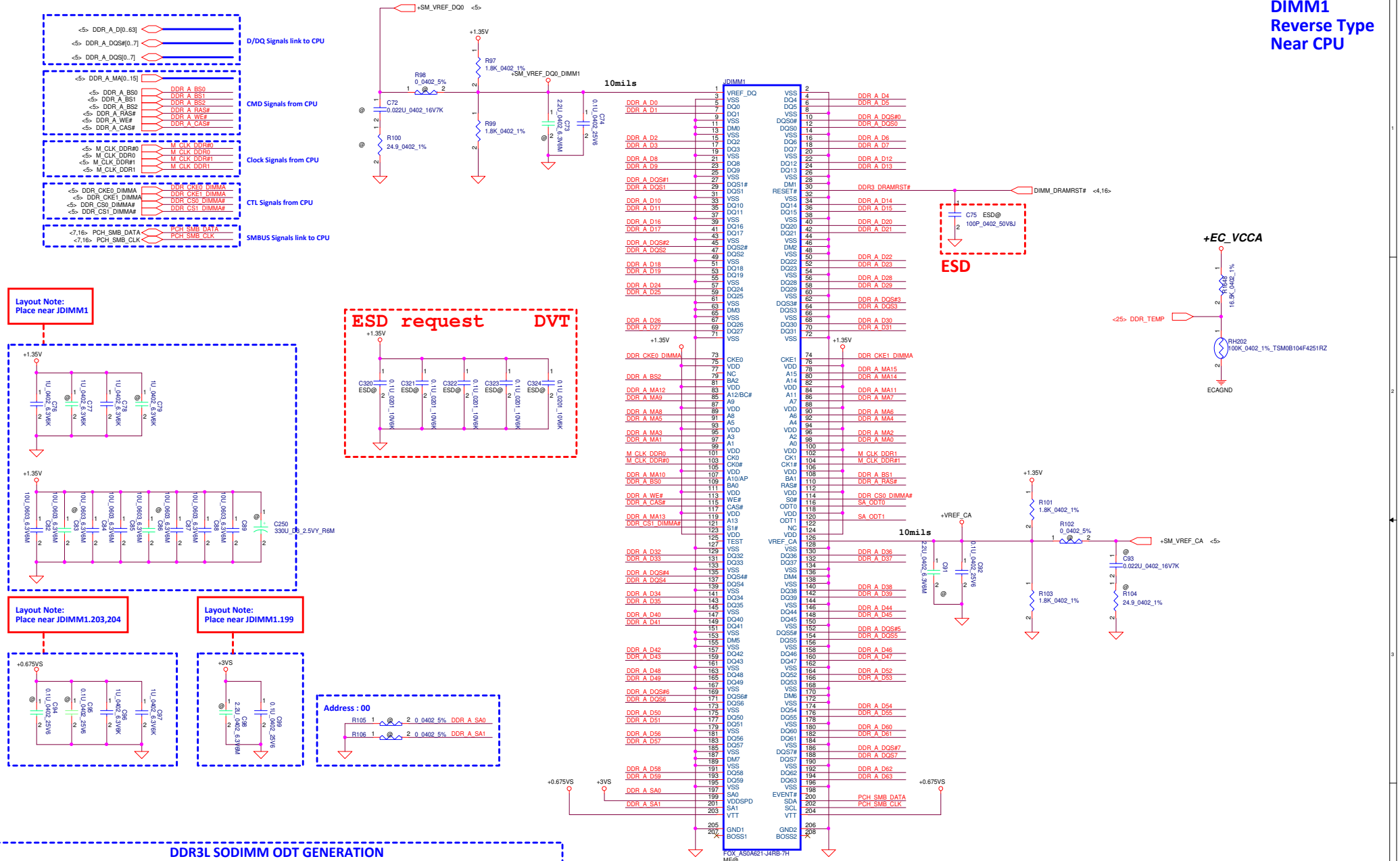
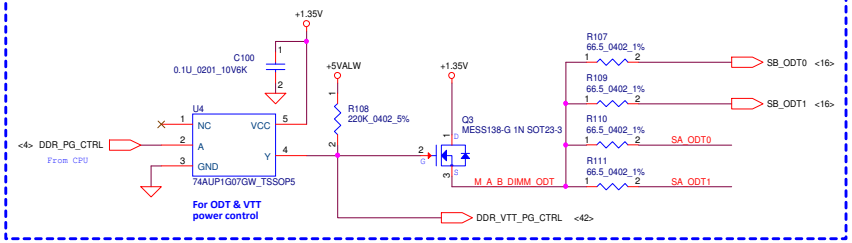
DIMM1 Reverse Type Near CPU



DDR3L SODIMM ODT GENERATION



Interleaved Memory

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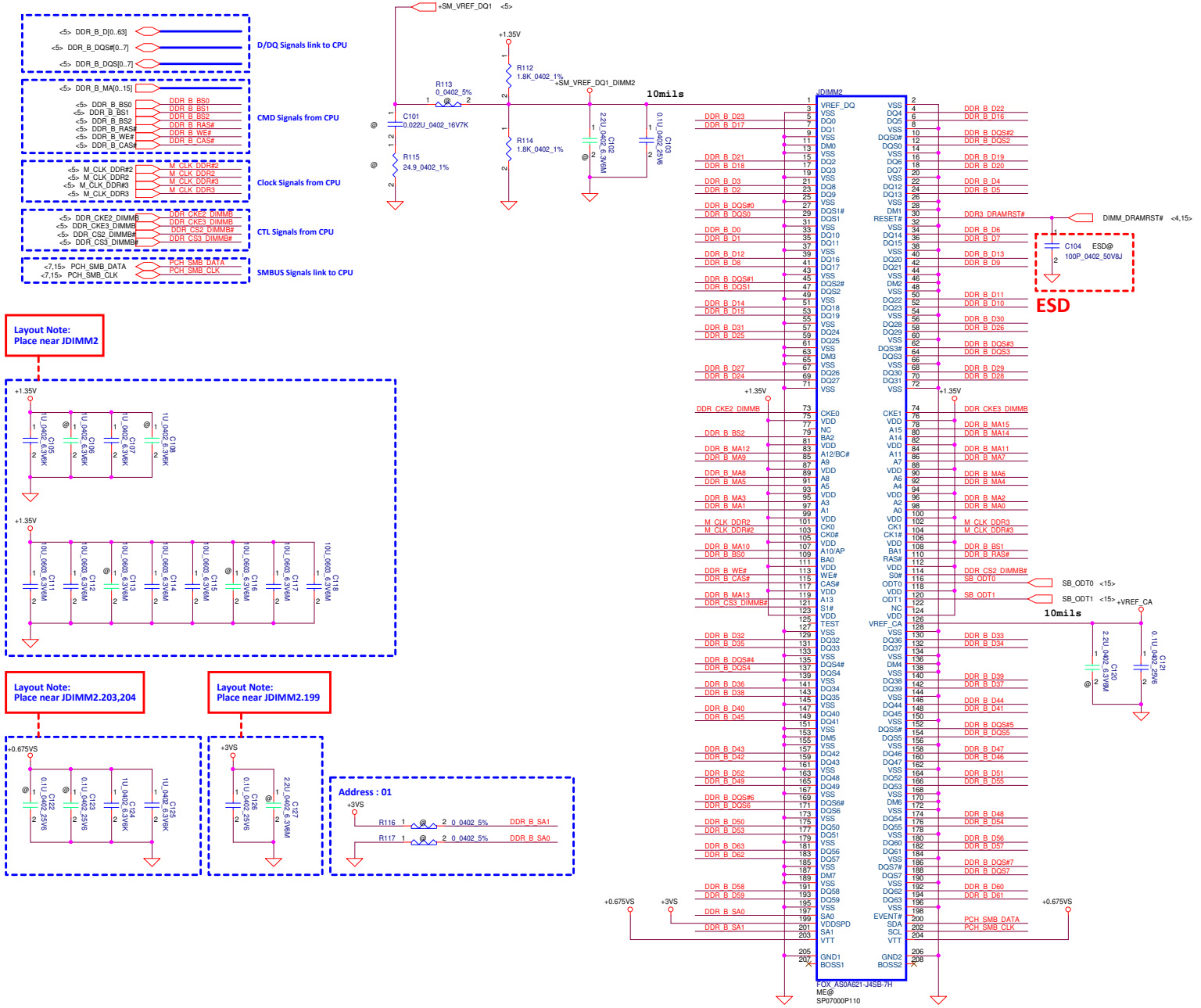
Compal Electronics, Inc.

Title: DDR3L DIMMA

Size: C | Document Number: LA-C281 | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 15 of 50

DIMM2
Standard Type
Near User



Interleaved Memory

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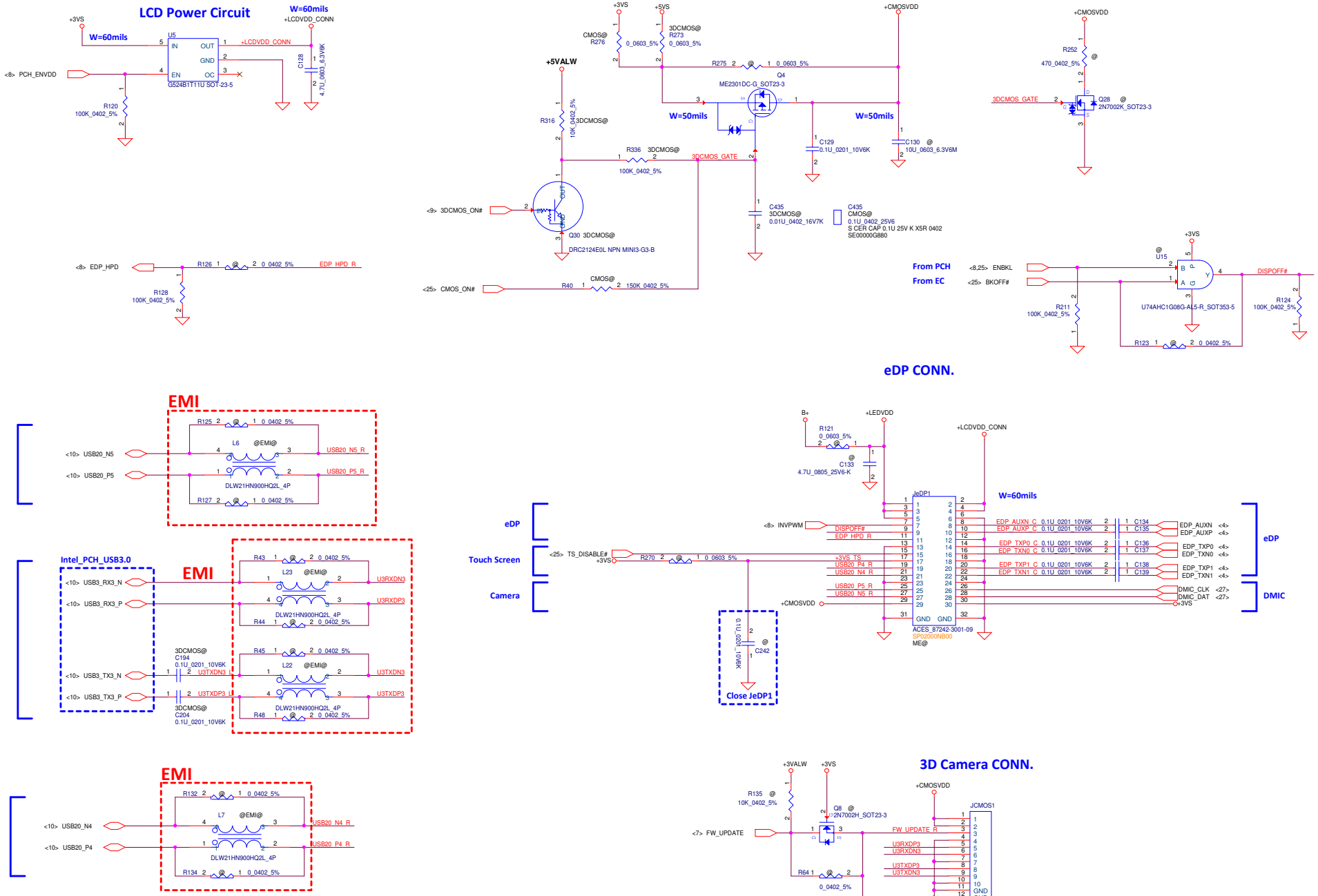
Compal Electronics, Inc.

Title: DDR3L DIMMB

Size: C | Document Number: LA-C281 | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 16 of 50



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Issued Date	2014/09/01	Deciphered Date	2015/09/01

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Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size	Document Number	Rev
C	LA-C281	1.0

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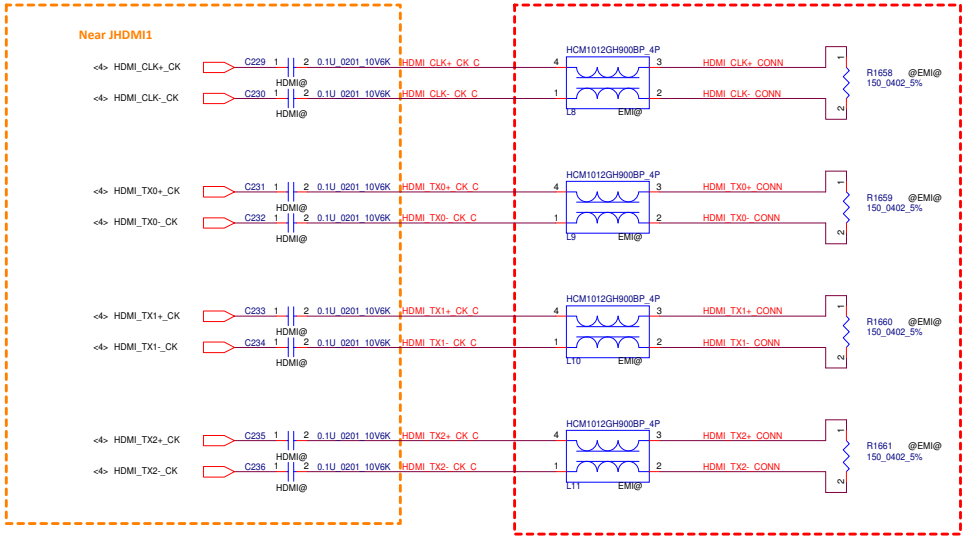
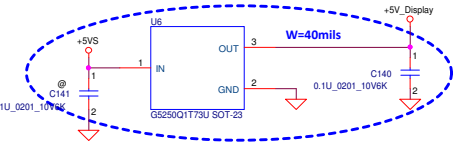
EMI

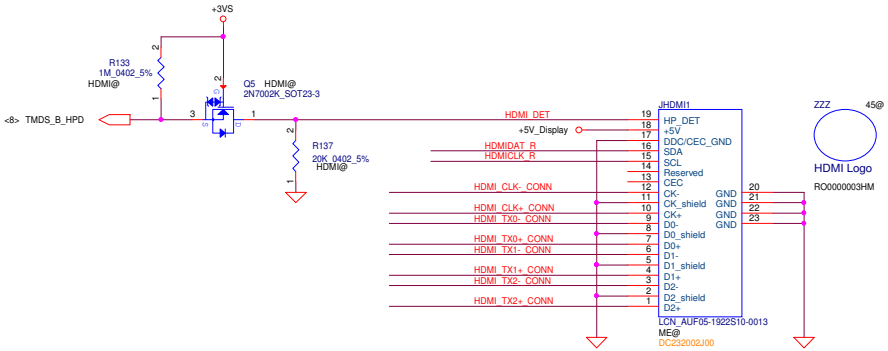
Near JHDMI1

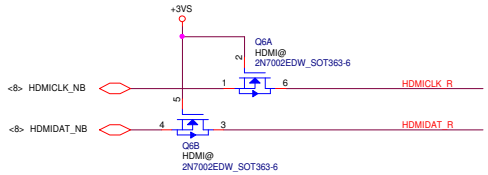


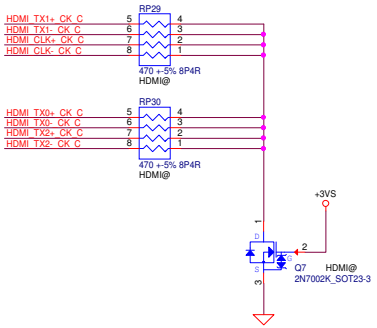
Only change P/N and value



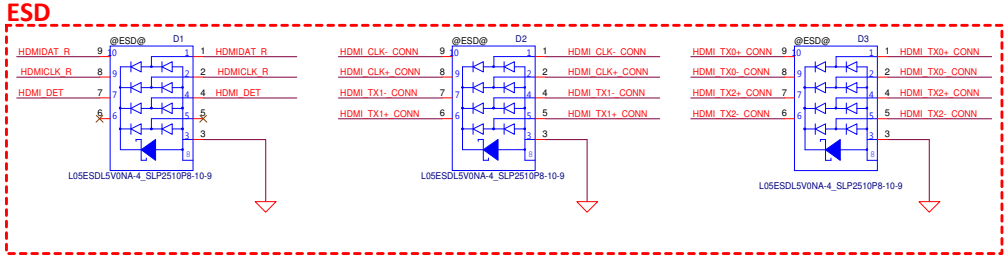
For CRT and HDMI







ESD



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Issued Date	2014/09/01	Deciphered Date	2015/09/01	Title: HDMI CONN
				Size: C; Document Number: LA-C281; Rev: 1.0
				Date: Friday, February 06, 2015; Sheet 18 of 50

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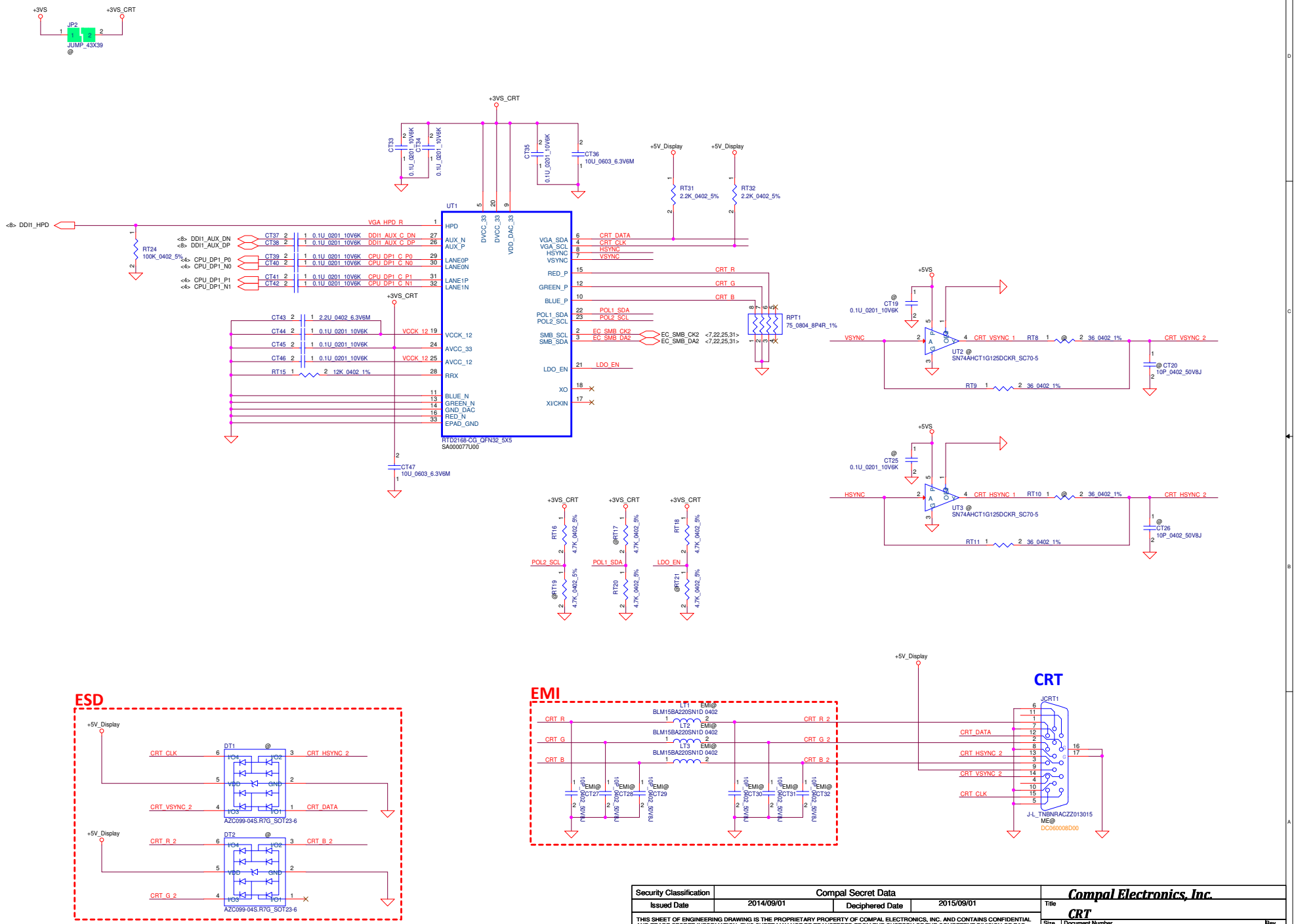

Security Classification	Compal Secret Data		
Issued Date	2014/09/01	Deciphered Date	2015/09/01

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Compal Electronics, Inc.

Title: CRT

Size	Document Number	Rev
C	LA-C281	1.0

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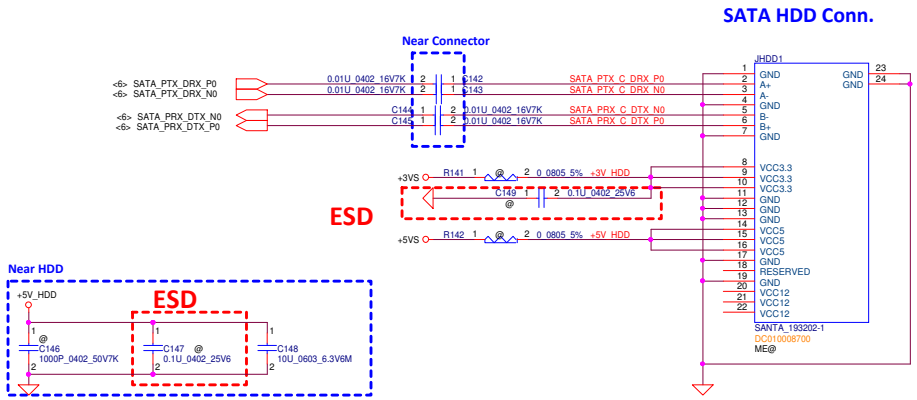
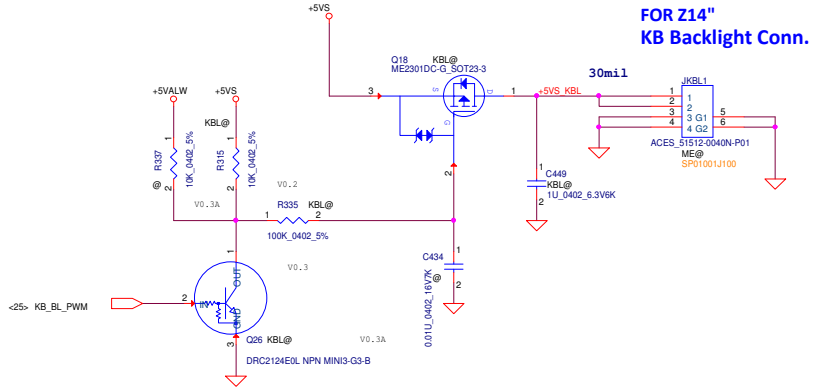
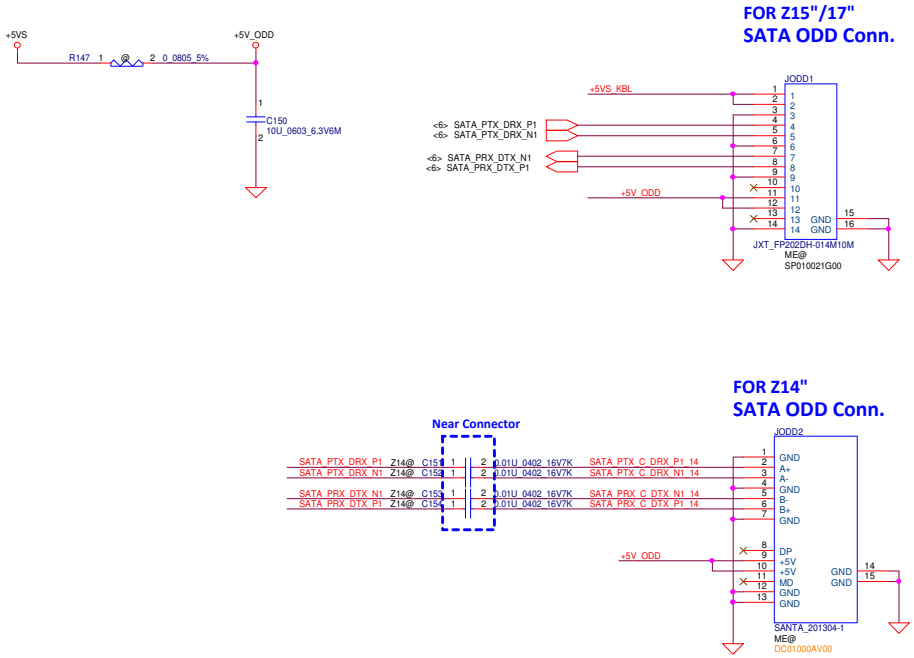
HDD



KB Backlight



ODD



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Compal Electronics, Inc.

Title: HDD/ODD/KB_BL Connector

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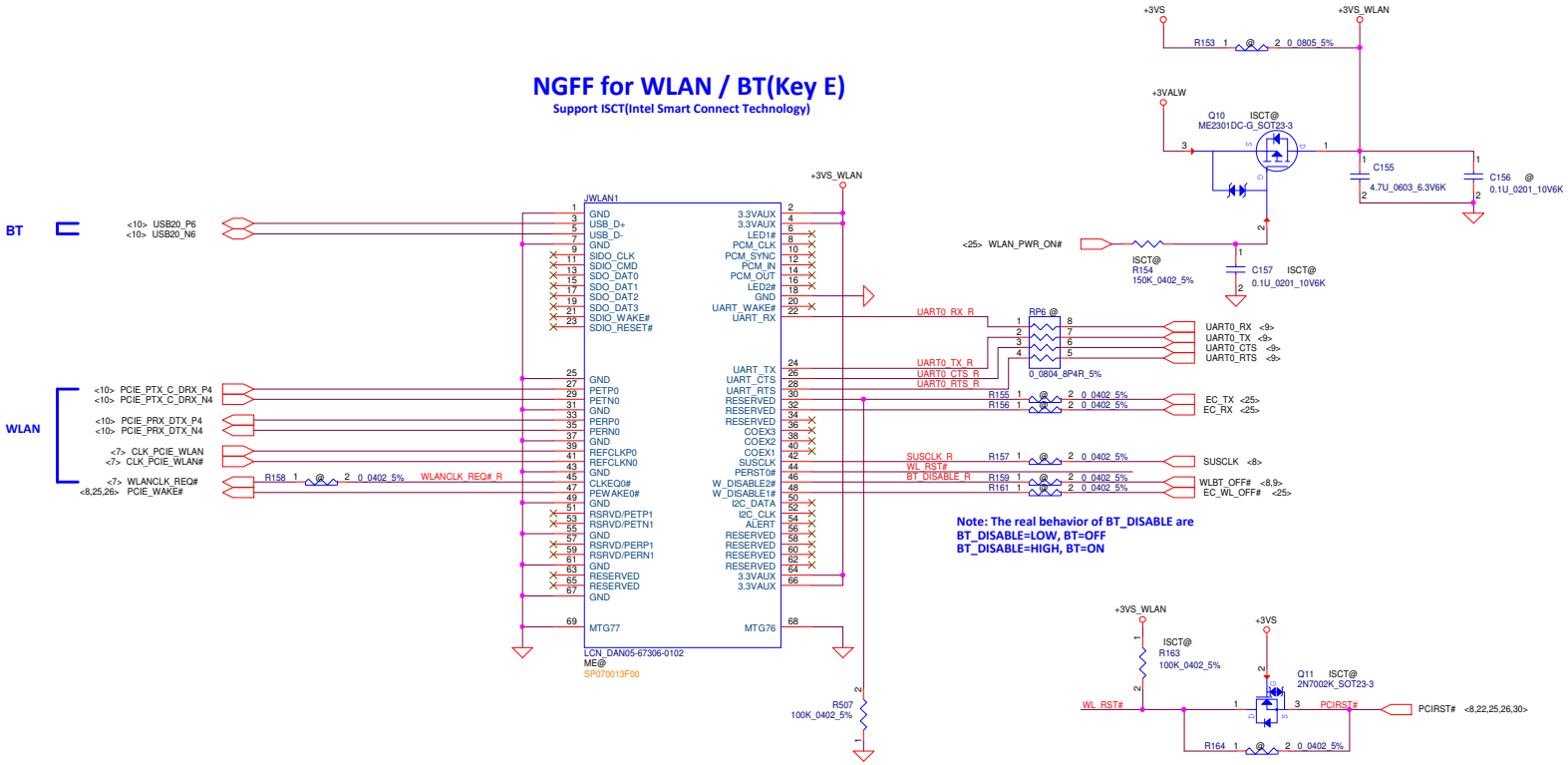
NGFF for WLAN / BT(Key E)

Support ISCT(Intel Smart Connect Technology)



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Issued Date	2014/09/01	Deciphered Date	2015/09/01

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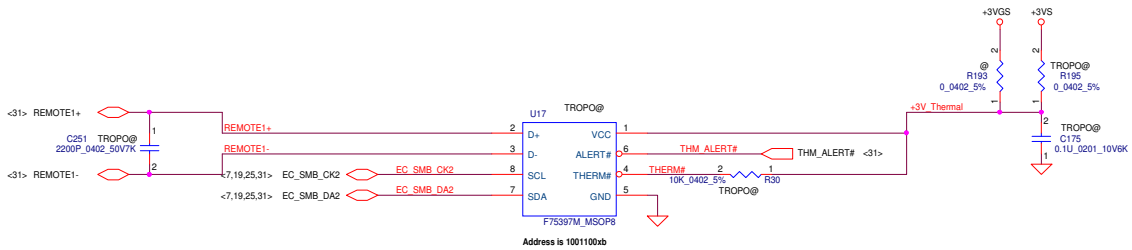
Compal Electronics, Inc.

Title: **Mini-Card/NEW Card/SIM**

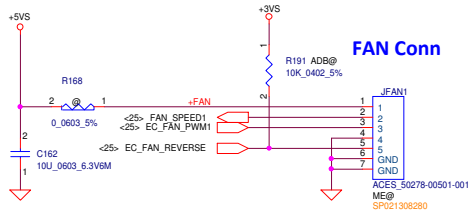
Size | Document Number: **LA-C281** | Rev 1.0

Date: Friday, February 06, 2015 | Sheet 21 of 50

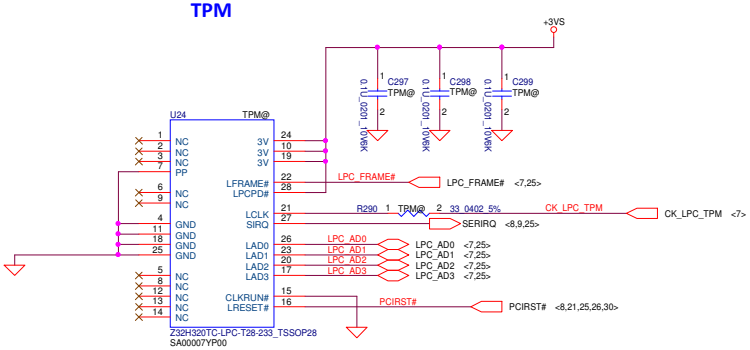
2 Channel

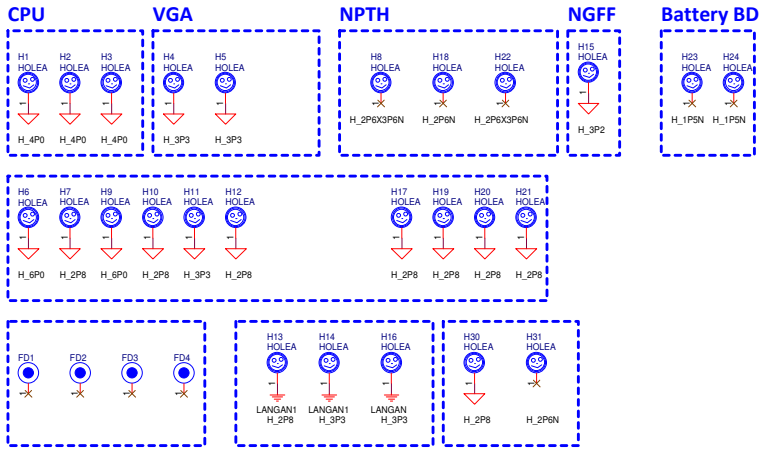


FAN Conn



TPM





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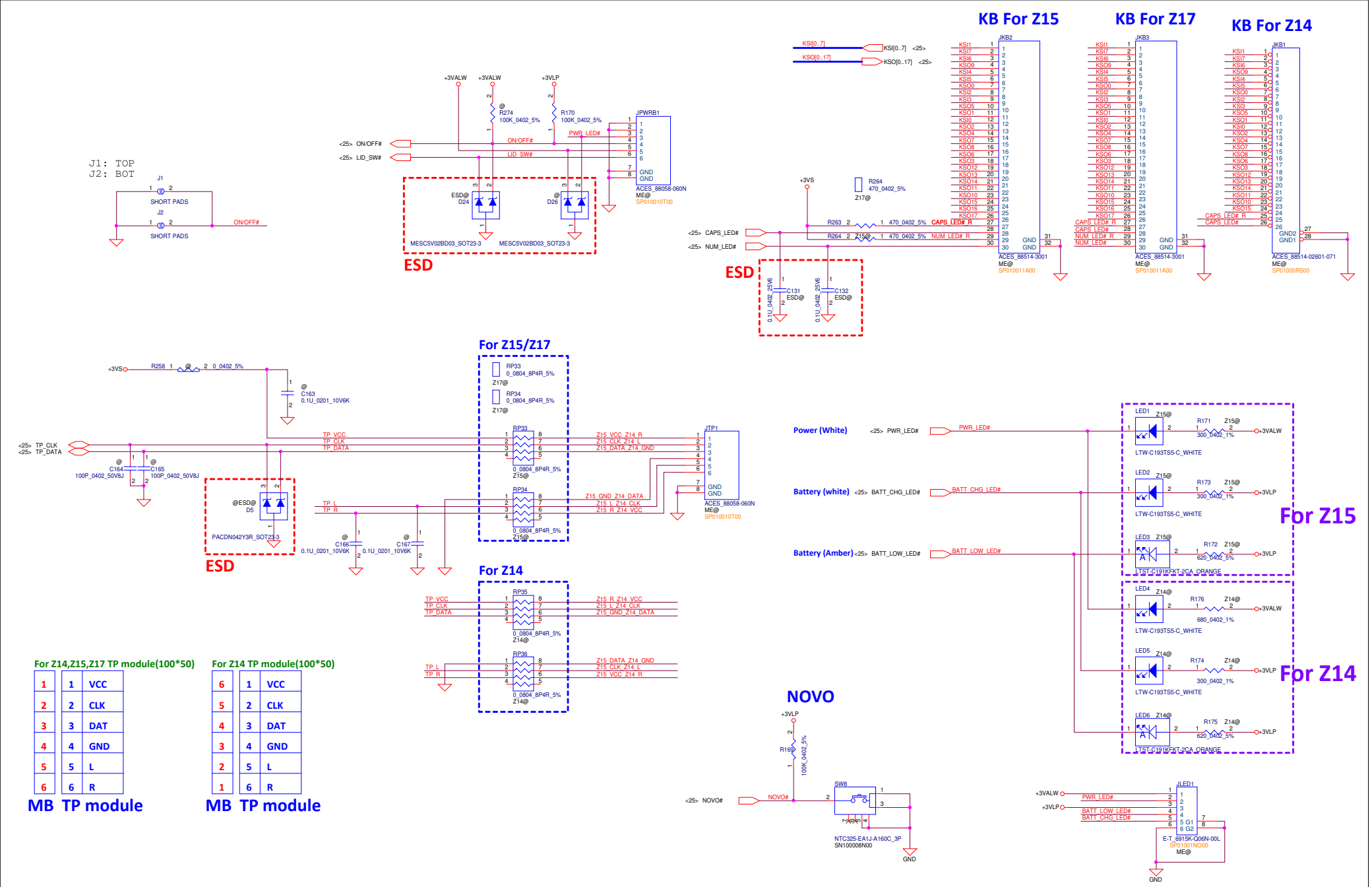
Compal Electronics, Inc.

Title: **Fintek-Thermal IC/FAN/screw**

Size: C | Document Number: **LA-C281** | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 22 of 50



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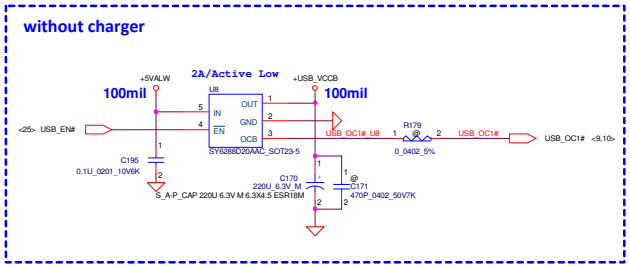
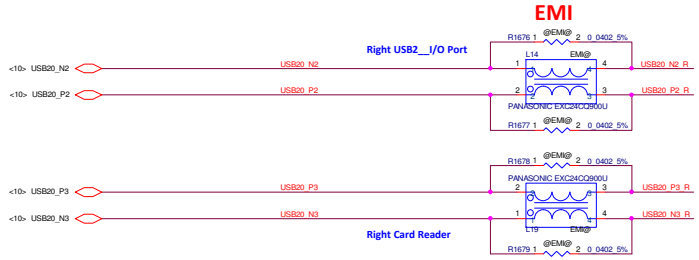
Compal Electronics, Inc.

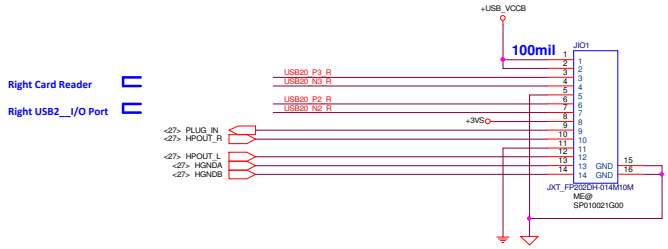
Title: ROM/KBD/PWR/CR/LED/TP Conn.

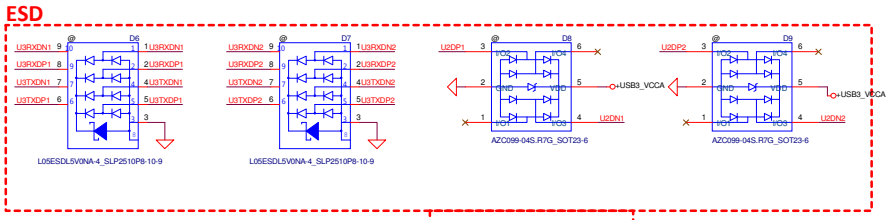
Size: C | Document Number: LA-C281 | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 23 of 50

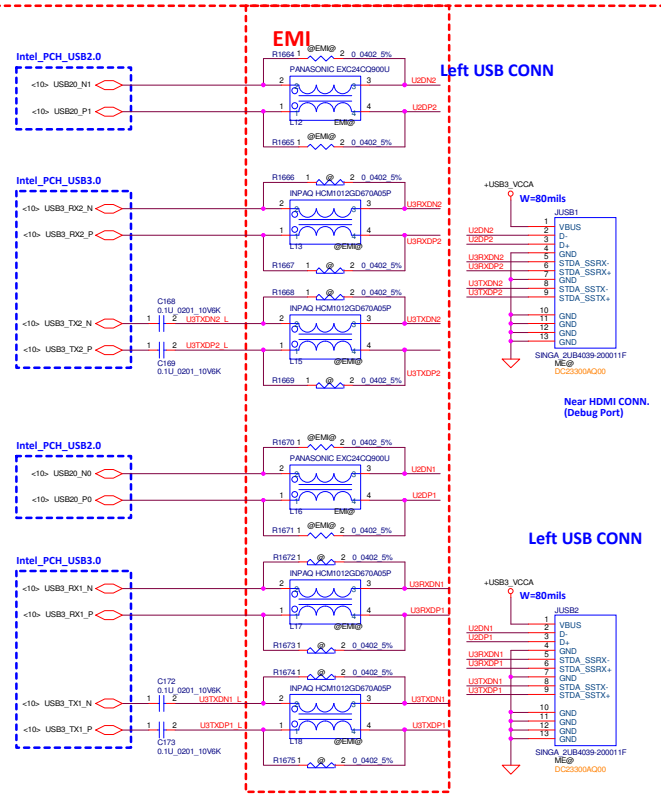








USB3.0_Port



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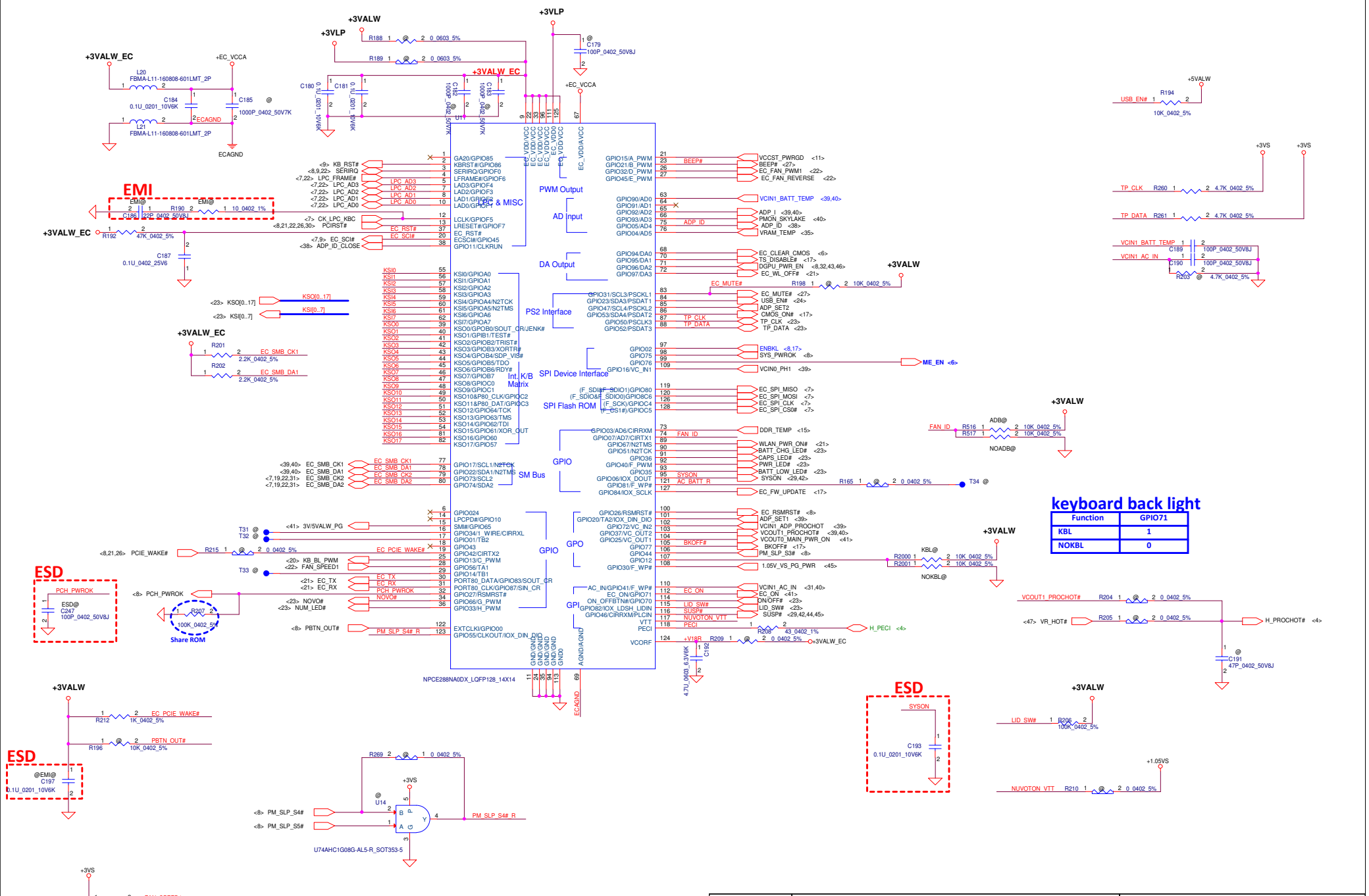
Compal Electronics, Inc.

Title: USB3.0/Left USB Ports

Size: Custom | Document Number | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 24 of 50



keyboard back light

Function	GPIO71
KBL	1
NOKBL	0

Security Classification	Compal Secret Data		
Issued Date	2014/09/01	Deciphered Date	2015/09/01

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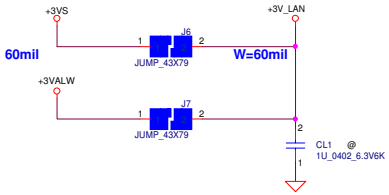
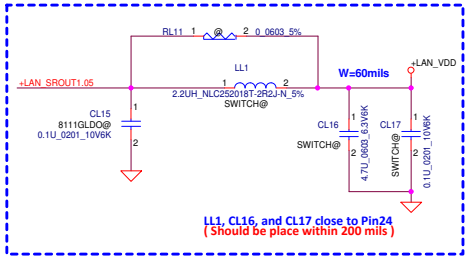
Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size: C | Document Number: **LA-C281** | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 25 of 50





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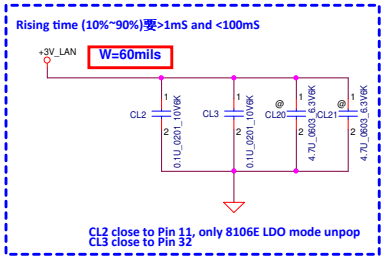
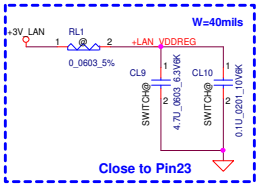
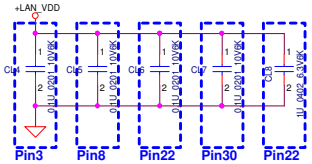
SA00005V700	RTL8111G	LDO	X	X	X	O	O
	~~RTL8111G~~	~~External~~	~~X~~	~~X~~	~~X~~	~~X~~	~~O~~
	RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X	X
SA000065Y00	RTL8106E	LDO	X	X	X	X	X

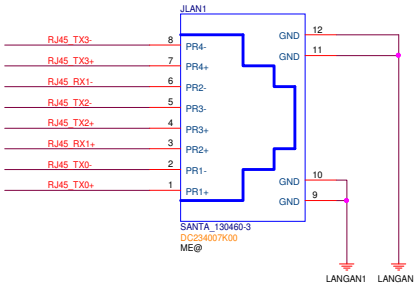
Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.

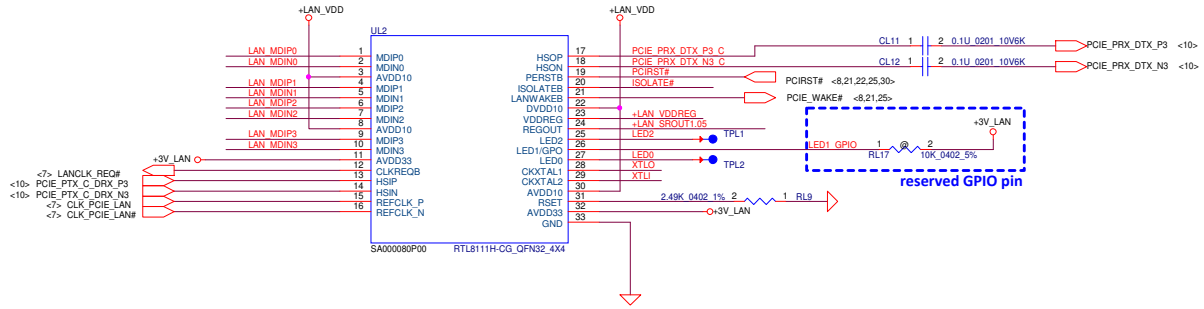


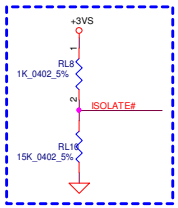


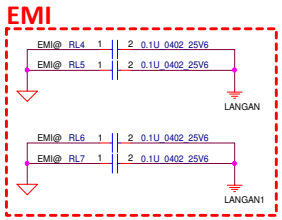


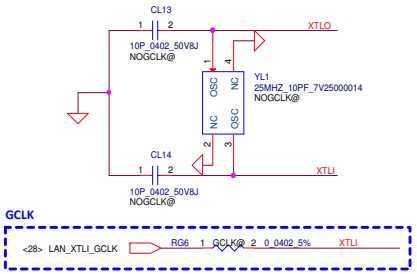
RJ-45 CONN.

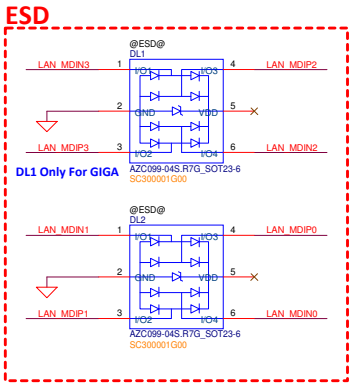


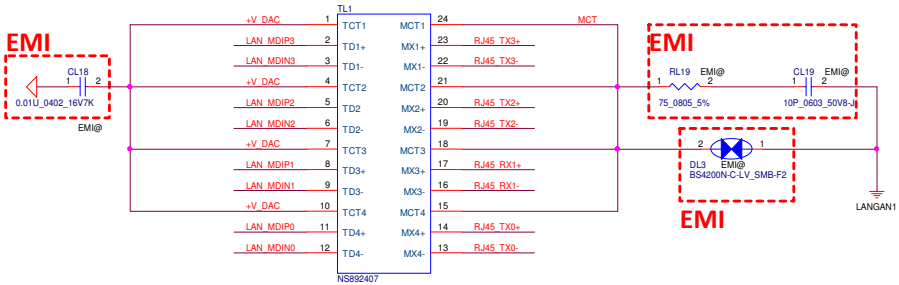












Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/09/01	Deciphered Date	2015/09/01	Title: LAN RTL8111/8106
				Size: C; Document Number: LA-C281; Rev: 1.0
				Date: Friday, February 06, 2015; Sheet 26 of 50

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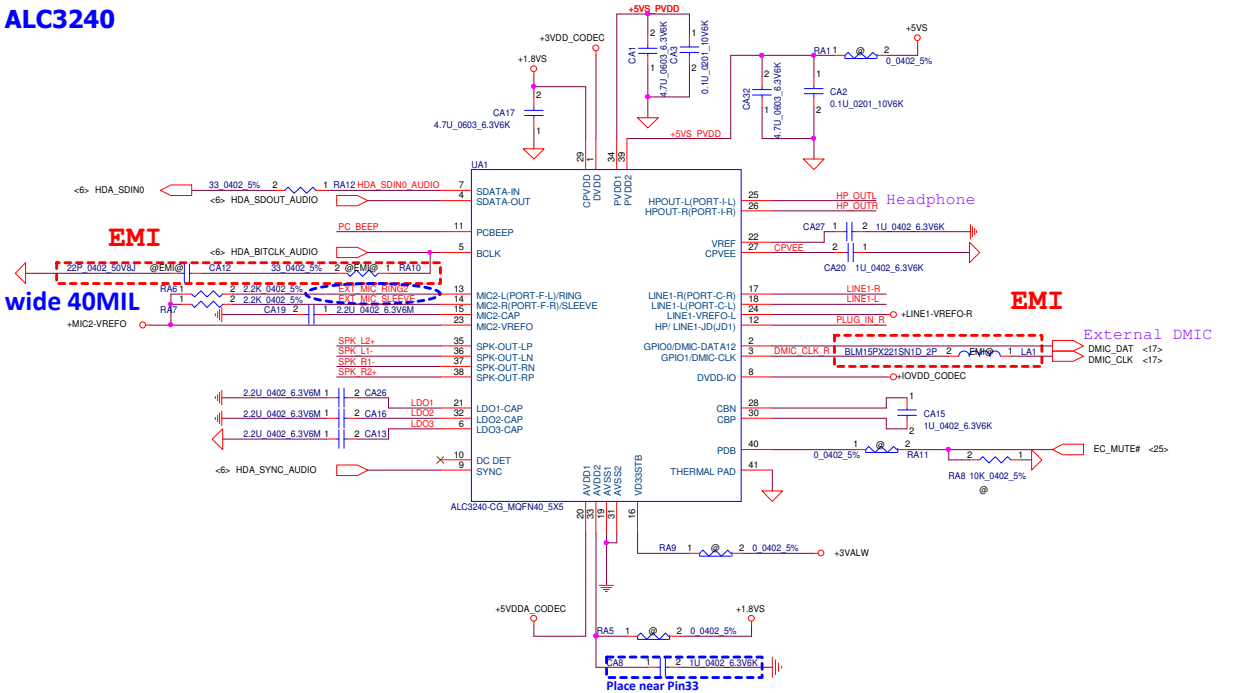
ALC3240



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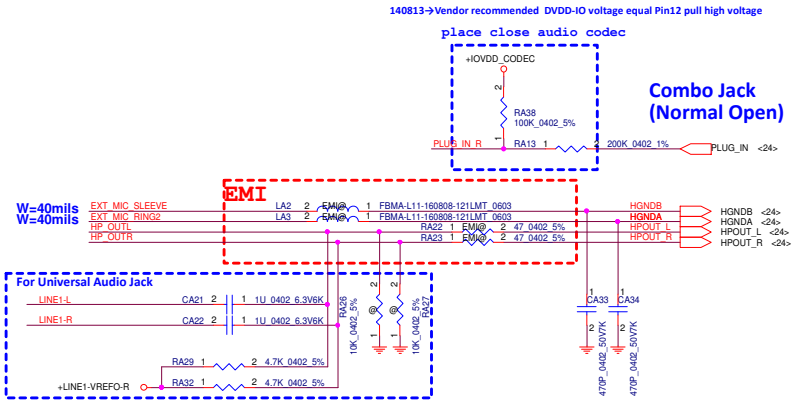

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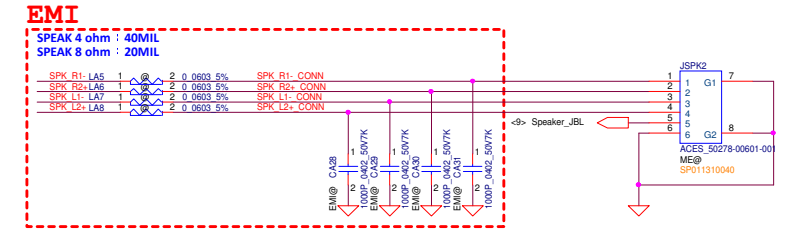
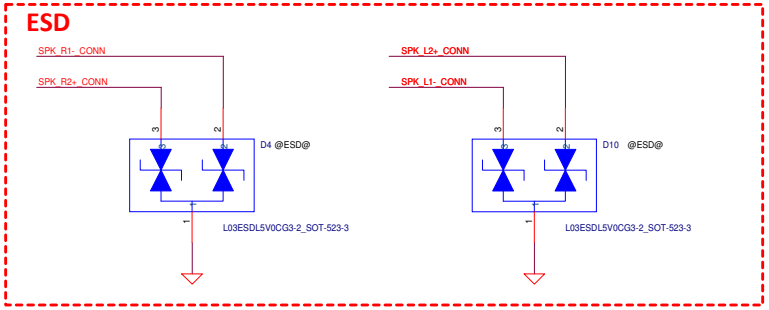
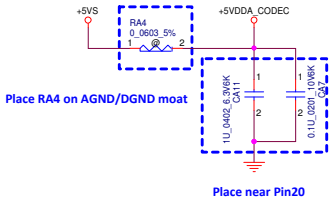


ESD protection needs to be placed near connector side



+5VS → +5VDDA_CODEC



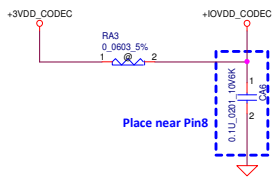
Each Platform Power Net Support List：

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0~S5)
AMD Carrizo	V	V	V	V	V
AMD Carrizo-L	V	V	V	V	V
Intel Broadwell	V		V	V	V
Intel Braswell	V	V	V	V	V
Intel Skylake	V	V	V	V	V
Intel Bay trail-M	V	V	V	V	V

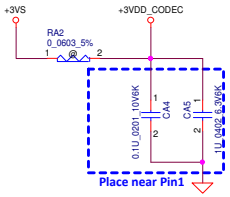
Each Platform HDA Link Voltage Support (Pin 8)：

	3.3V	1.5V
AMD Carrizo		V
AMD Carrizo-L		V
Intel Broadwell	V	V
Intel Braswell		V
Intel Skylake	V	V
Intel Bay trail-M		V

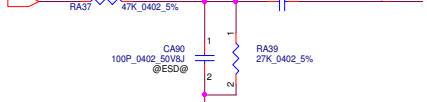
+3VDD_CODEC → +IOVDD_CODEC



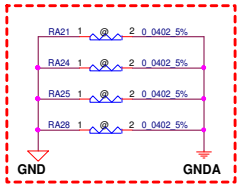
+3VS → +3VDD_CODEC



PC Beep



EMI



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Issued Date	2014/09/01	Deciphered Date	2015/09/01

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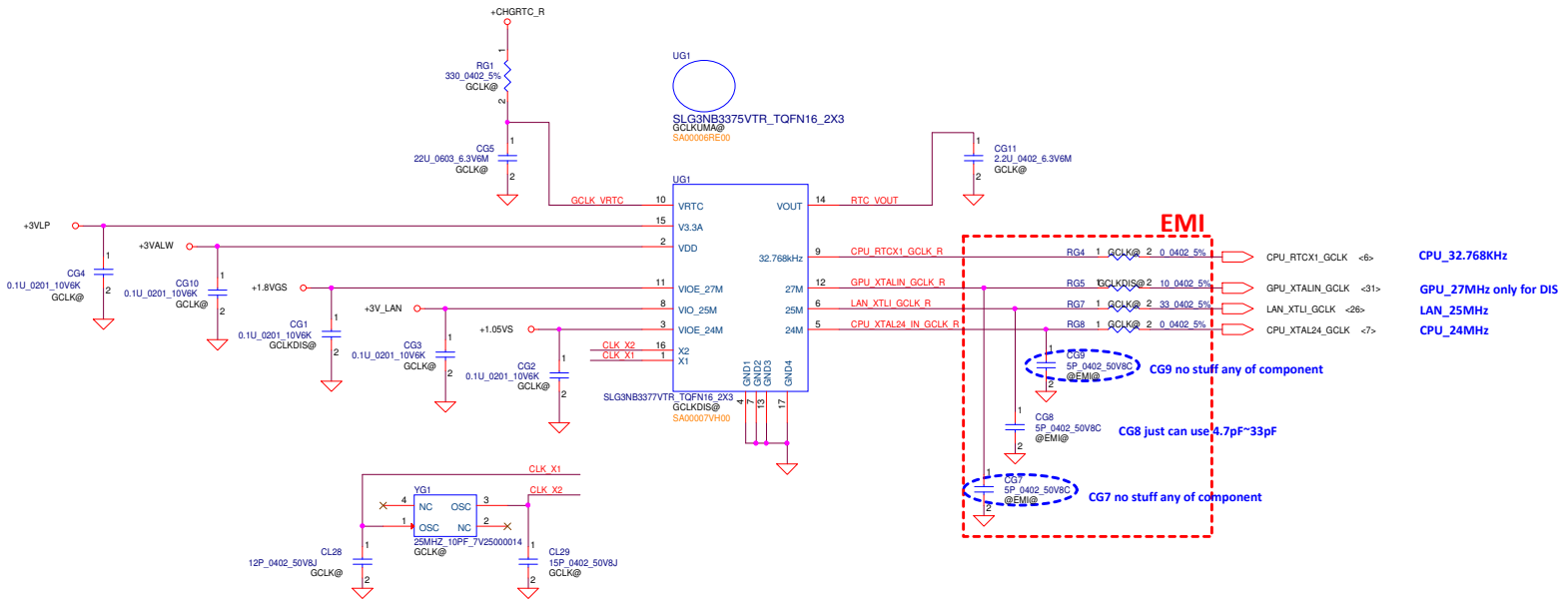
Compal Electronics, Inc.

Title: HD Audio Codec_ALC3240

Size: C | Document Number: LA-C281 | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 27 of 50



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Issued Date	2014/09/01	Deciphered Date	2015/09/01

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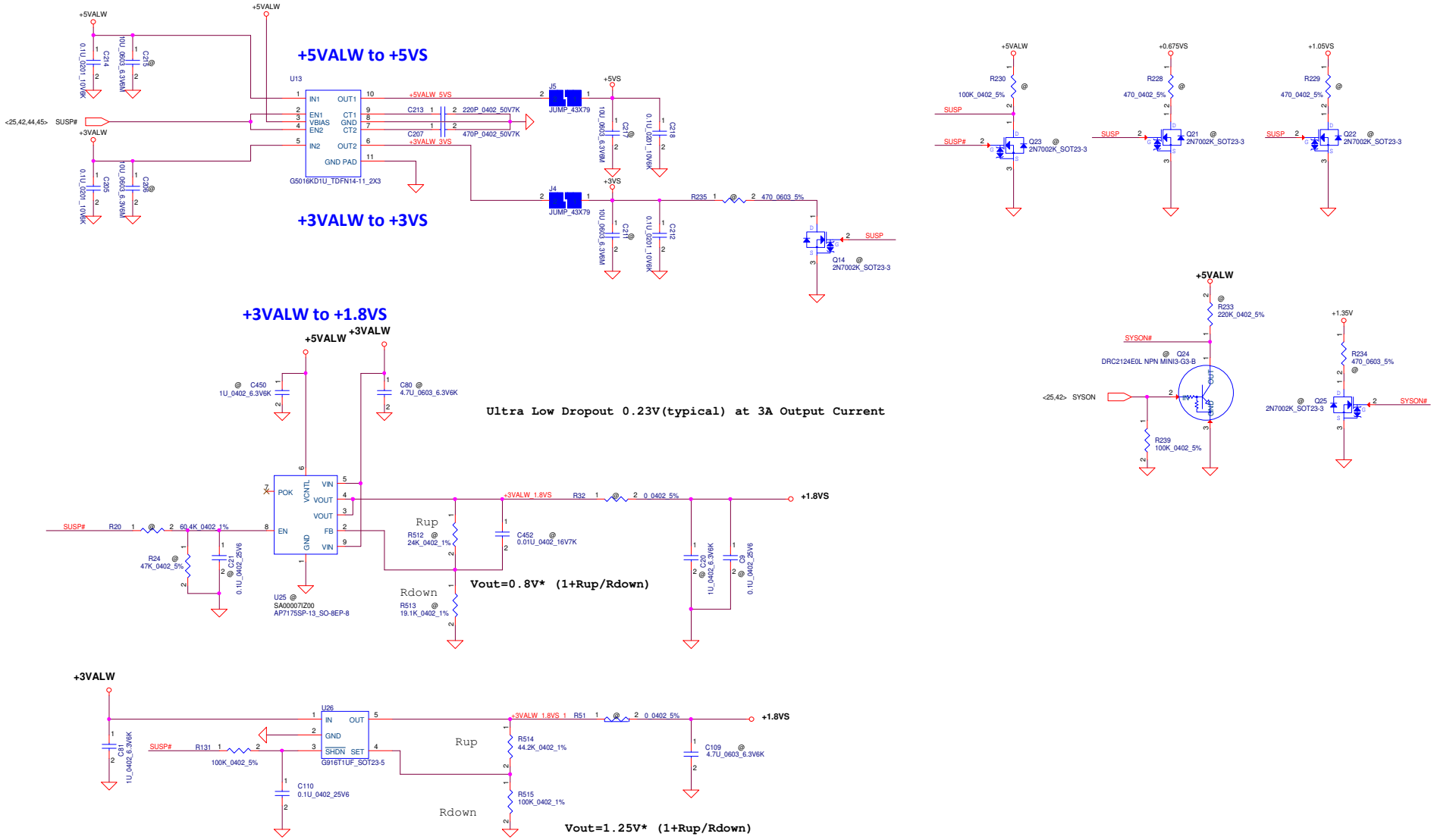
Compal Electronics, Inc.

Title: **GCLK**

Size: | Document Number: **LA-C281** | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 28 of 50



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/09/01	Deciphered Date	2015/09/01	Title: DC Interface
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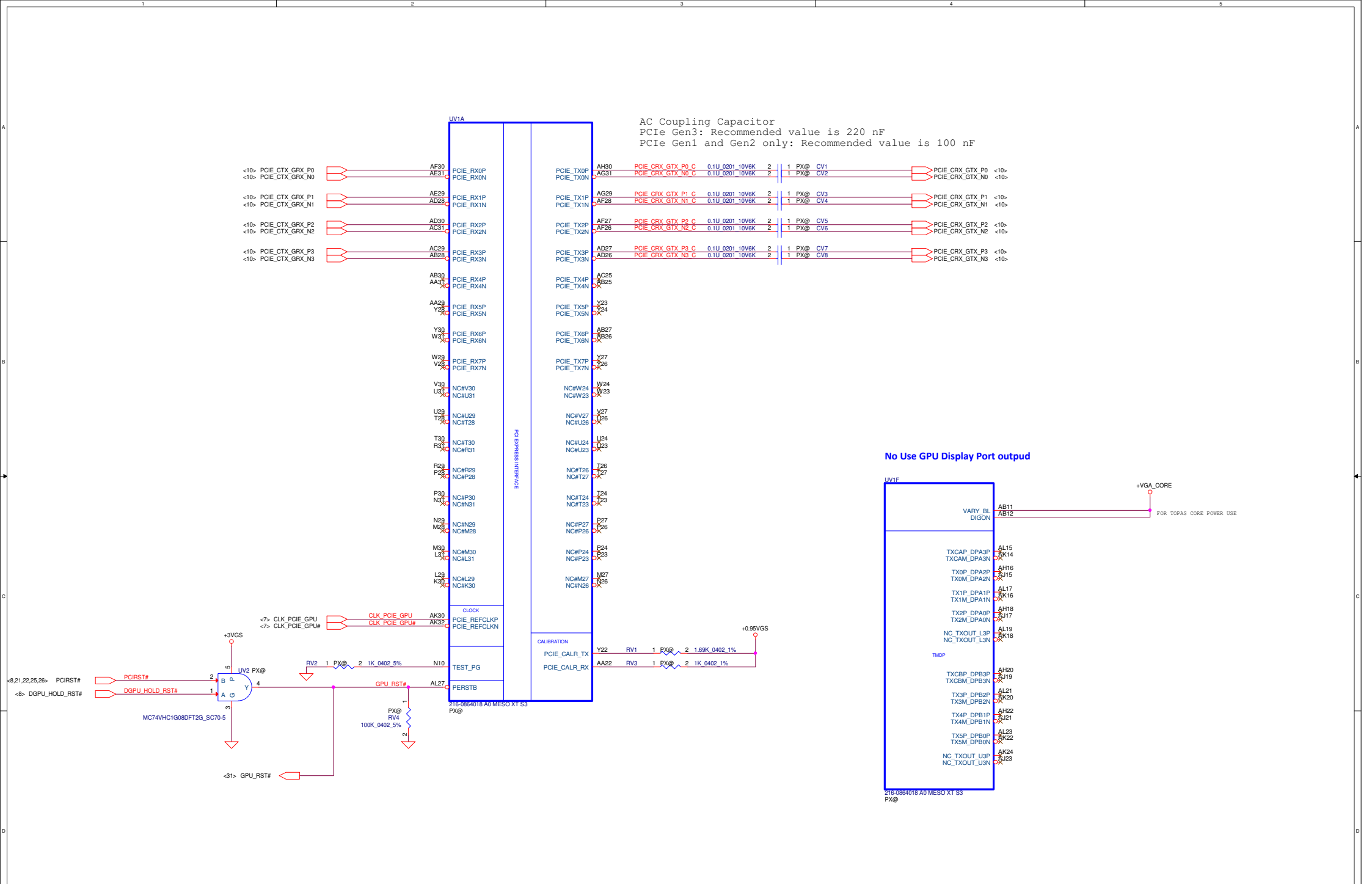
				Date: Friday, February 06, 2015; Sheet 29 of 50



Security Classification	Compal Secret Data		
Issued Date	2014/09/01	Deciphered Date	2015/09/01

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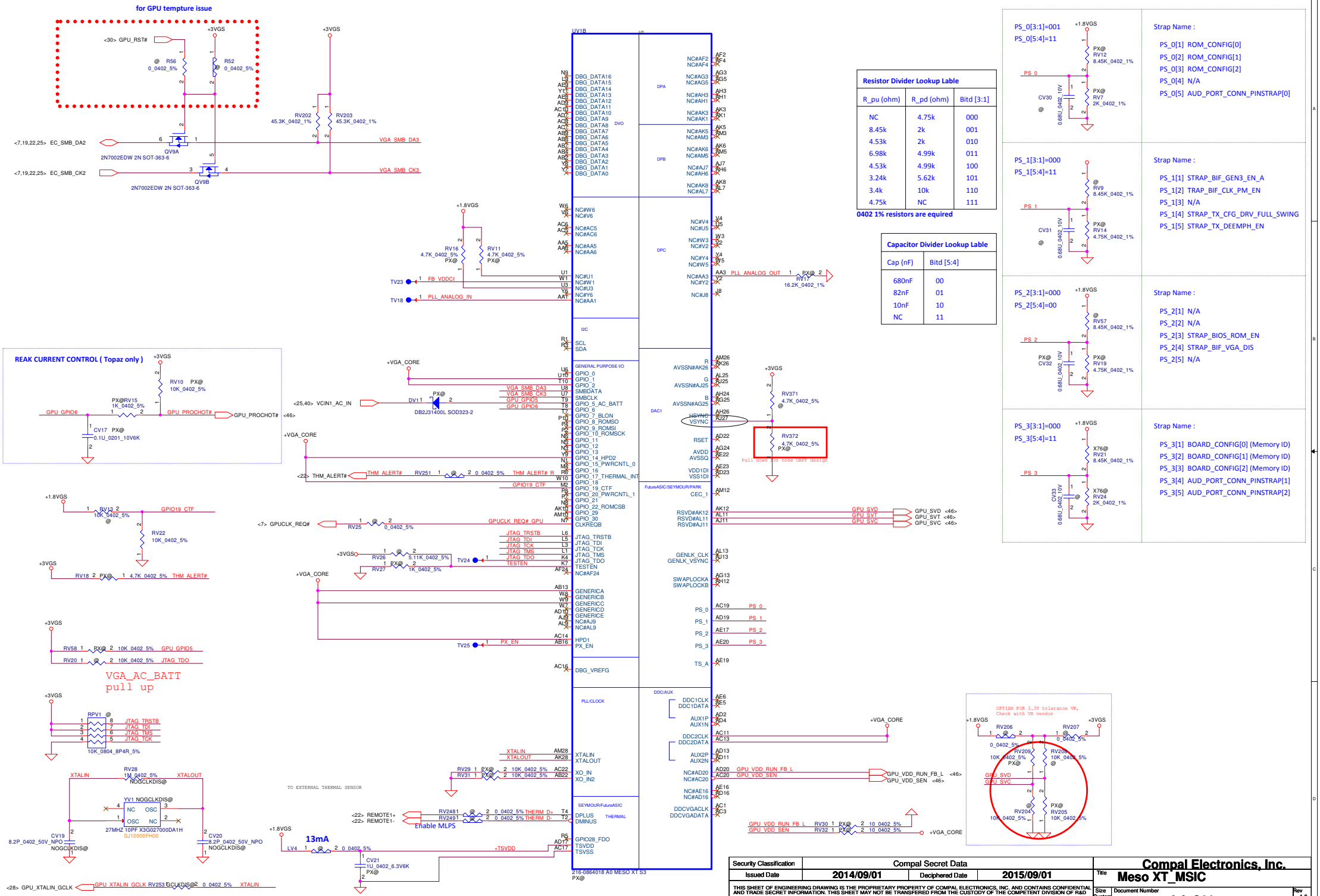
Compal Electronics, Inc.

Title: **Meso XT_PCIE/DP**

Size: Custom | Document Number: **LA-C281** | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 30 of 50



Resistor Divider Lookup Lable		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :
- PS_0[1] ROM_CONFIG[0]
- PS_0[2] ROM_CONFIG[1]
- PS_0[3] ROM_CONFIG[2]
- PS_0[4] N/A
- PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[3:1]=000
PS_1[5:4]=11

Strap Name :
- PS_1[1] STRAP_BIF_GEN3_EN_A
- PS_1[2] TRAP_BIF_CLK_PM_EN
- PS_1[3] N/A
- PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
- PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=00

Strap Name :
- PS_2[1] N/A
- PS_2[2] N/A
- PS_2[3] STRAP_BIOS_ROM_EN
- PS_2[4] STRAP_BIF_VGA_DIS
- PS_2[5] N/A

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
- PS_3[1] BOARD_CONFIG[0] (Memory ID)
- PS_3[2] BOARD_CONFIG[1] (Memory ID)
- PS_3[3] BOARD_CONFIG[2] (Memory ID)
- PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
- PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

Security Classification	Compal Secret Data		
Issued Date	2014/09/01	Deciphered Date	2015/09/01

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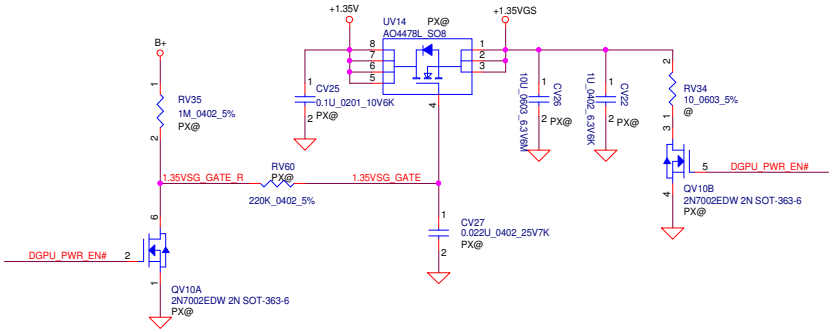
Compal Electronics, Inc.

Title: Meso XT_MSIC

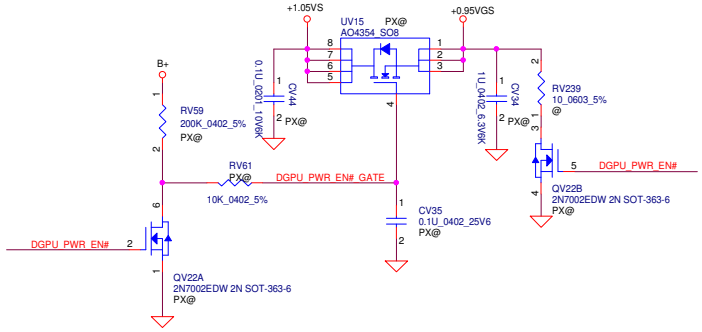
Size: Custom | Document Number: LA-C281 | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 31 of 50

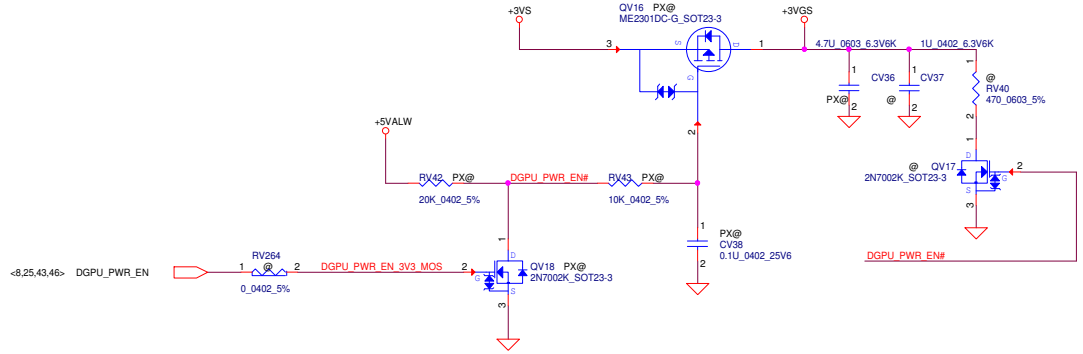
+1.35VS to +1.35VGS (6.234A)



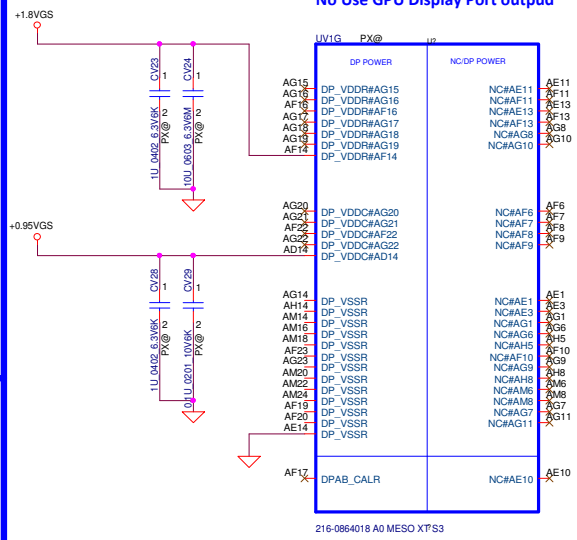
+1.05VS to +0.95VGS

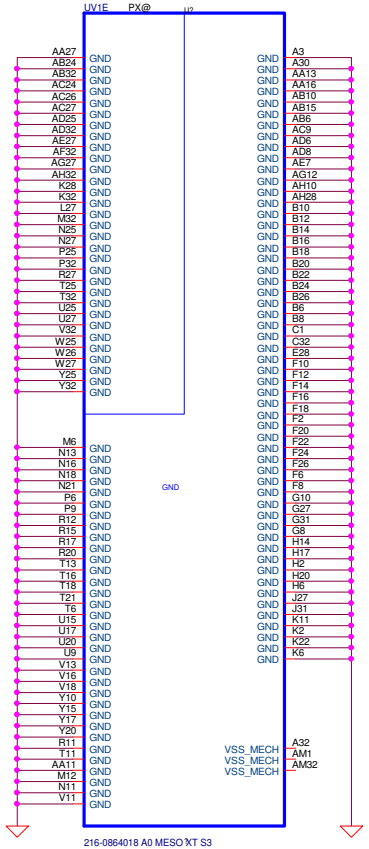


+3VS to +3VS_VGA (25mA)



No Use GPU Display Port outpud





Security Classification	Compal Secret Data		
Issued Date	2014/09/01	Deciphered Date	2015/09/01

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Compal Electronics, Inc.

Title: **Meso XT_Power/GND**

Size: Custom | Document Number: **LA-C281** | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 32 of 50

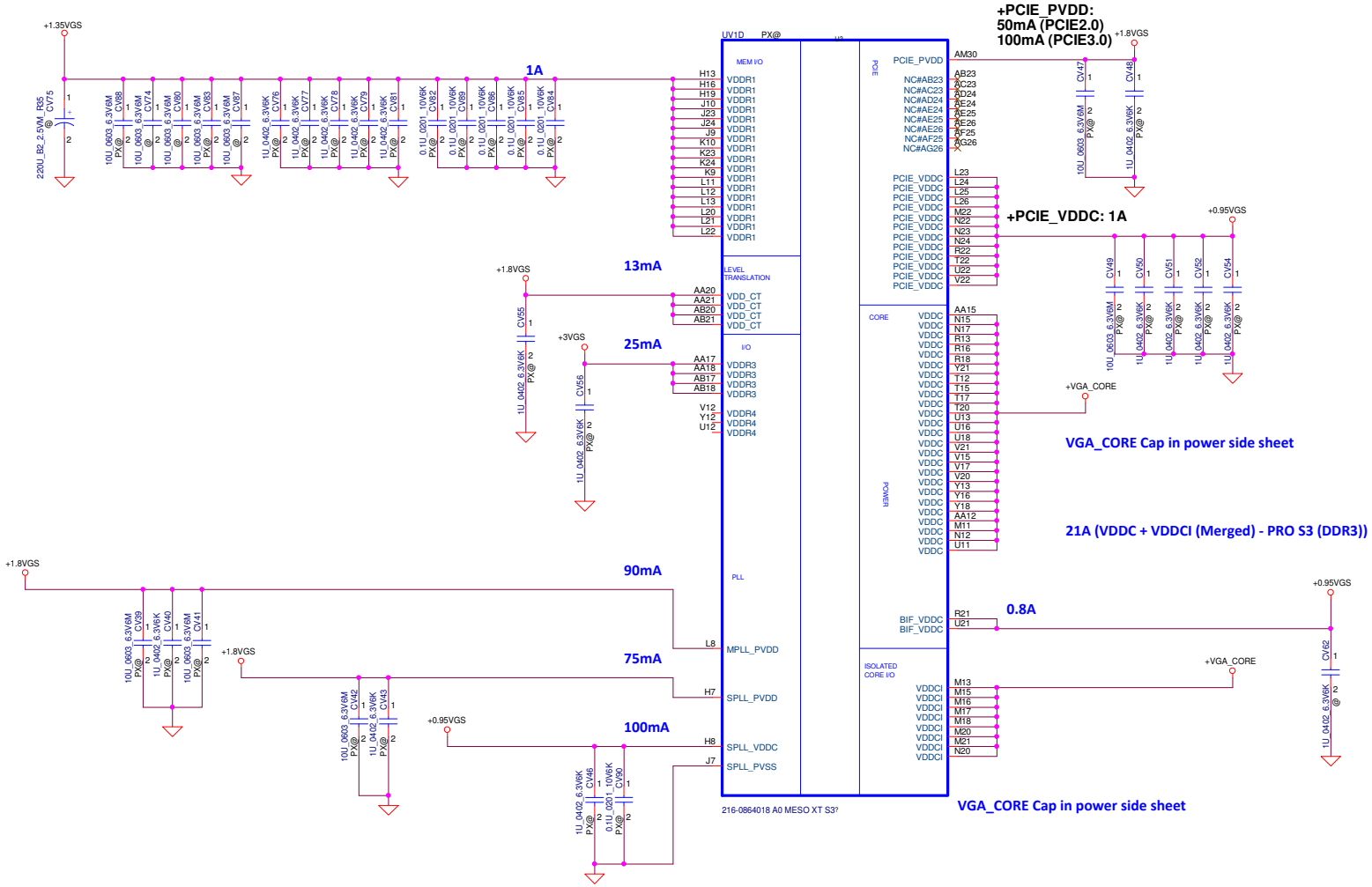
+VGA_CORE		10uF	2.2uF	1uF	0.1uF
VDDC	TBD	7	16	4	3
VDDCI	3.5A				

+0.95VGS		10uF	1uF	0.1uF
PCIE_VDDC	1A	1	5(1@)	0
BIF_VDDC	0.8A	0	1(1@)	0
SPLL_VDDC	100mA	0	1	1

+1.35VGS		10uF	1uF	0.1uF	0.01uF
VDDR1	1.5A	5(3@)	5	5	0

+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	0
MPLL_PVDD	130mA	2	1	0
SPLL_PVDD	75mA	0	1	0
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	0	1	0
+TSVDD	13mA	0	1	0
+DP_VDDR		1	1	0
+DP_VDDC		0	1	1

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	1	0



Security Classification	Compal Secret Data		
Issued Date	2014/09/01	Deciphered Date	2015/09/01

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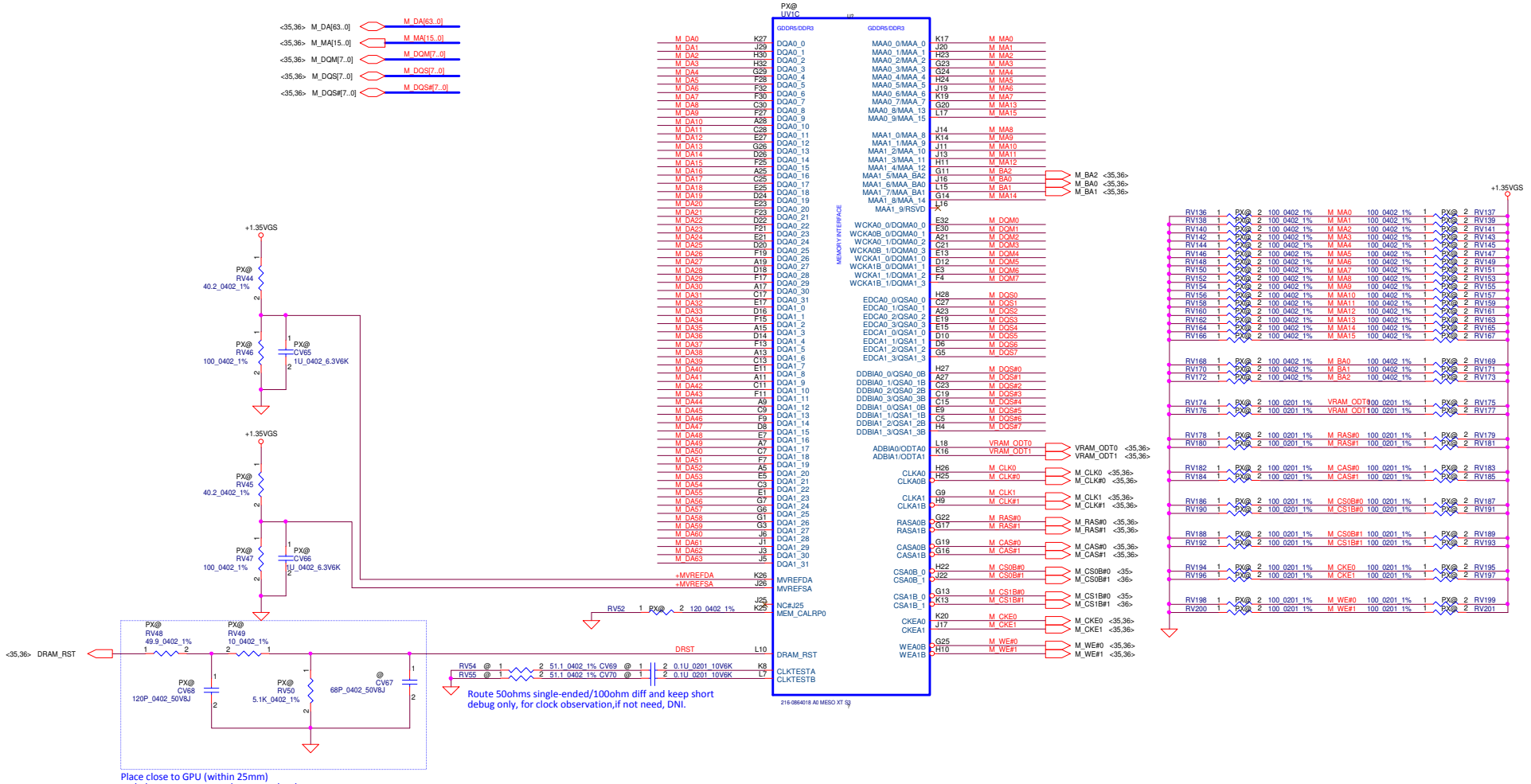
Compal Electronics, Inc.

Title: **Meso XT_Power**

Size: Custom | Document Number: **LA-C281** | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 33 of 50



Security Classification	Compal Secret Data		
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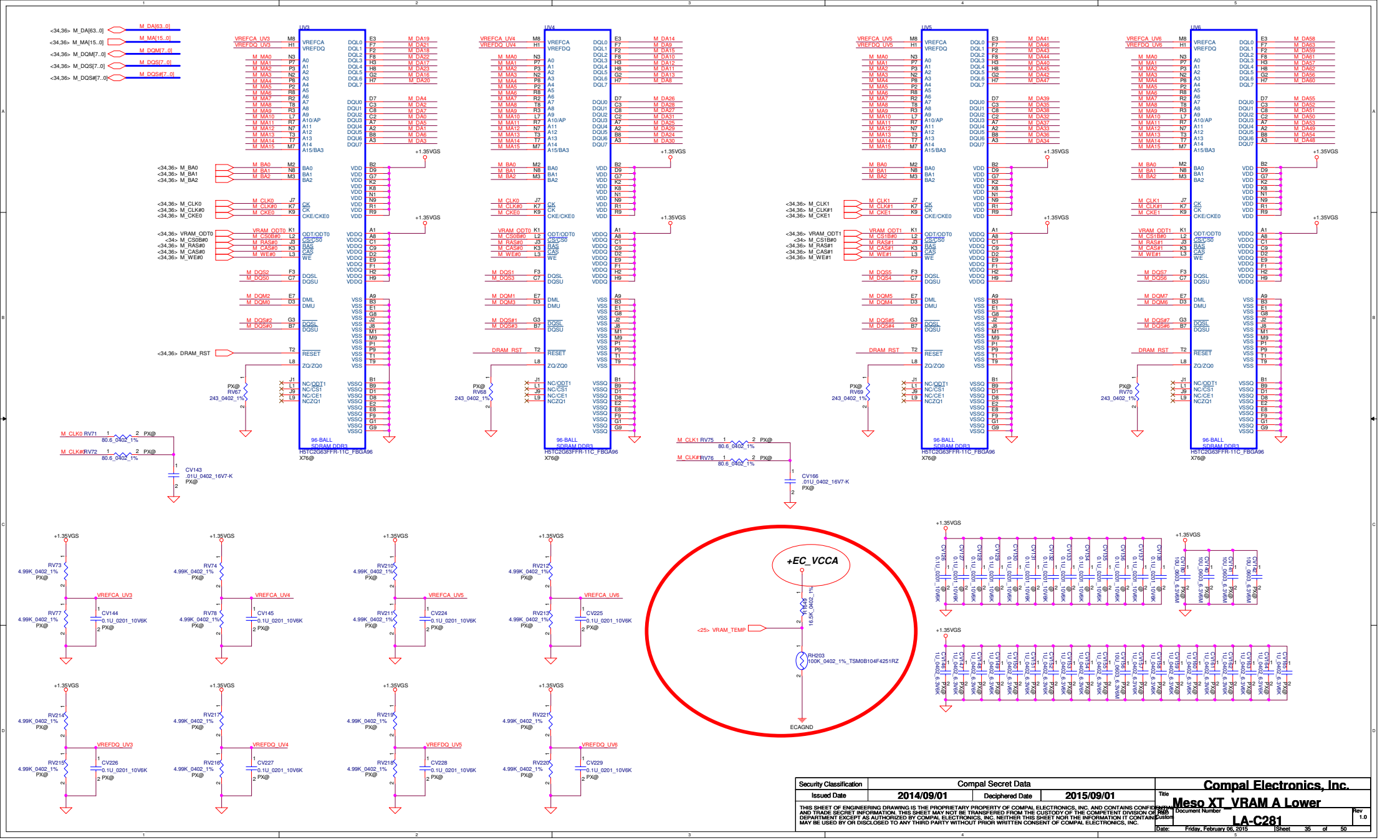
Compal Electronics, Inc.

Title: **Meso XT _MEM**

Size: C | Document Number: **LA-C281** | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 34 of 50



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Issued Date	2014/09/01	Deciphered Date	2015/09/01

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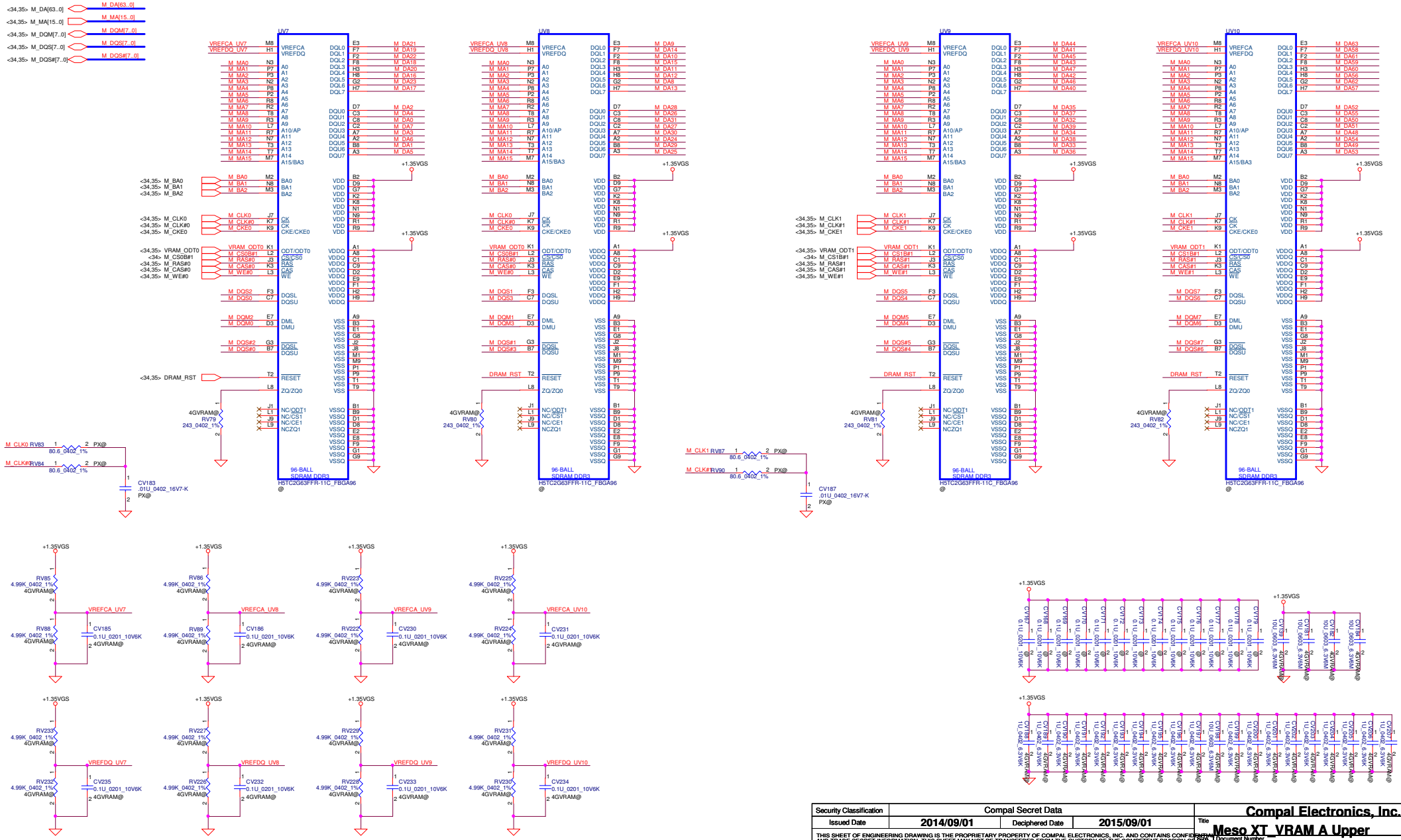
Compal Electronics, Inc.

Title: **Meso XT_VRAM A Lower**

Document Number: **LA-C281**

Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 35 of 50



Security Classification	Compal Secret Data		
Issued Date	2014/09/01	Deciphered Date	2015/09/01

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Compal Electronics, Inc.

Title: **Meso XT_VRAM A Upper**

Document Number: **LA-C281**

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Date: Friday, February 06, 2015 | Sheet 36 of 50

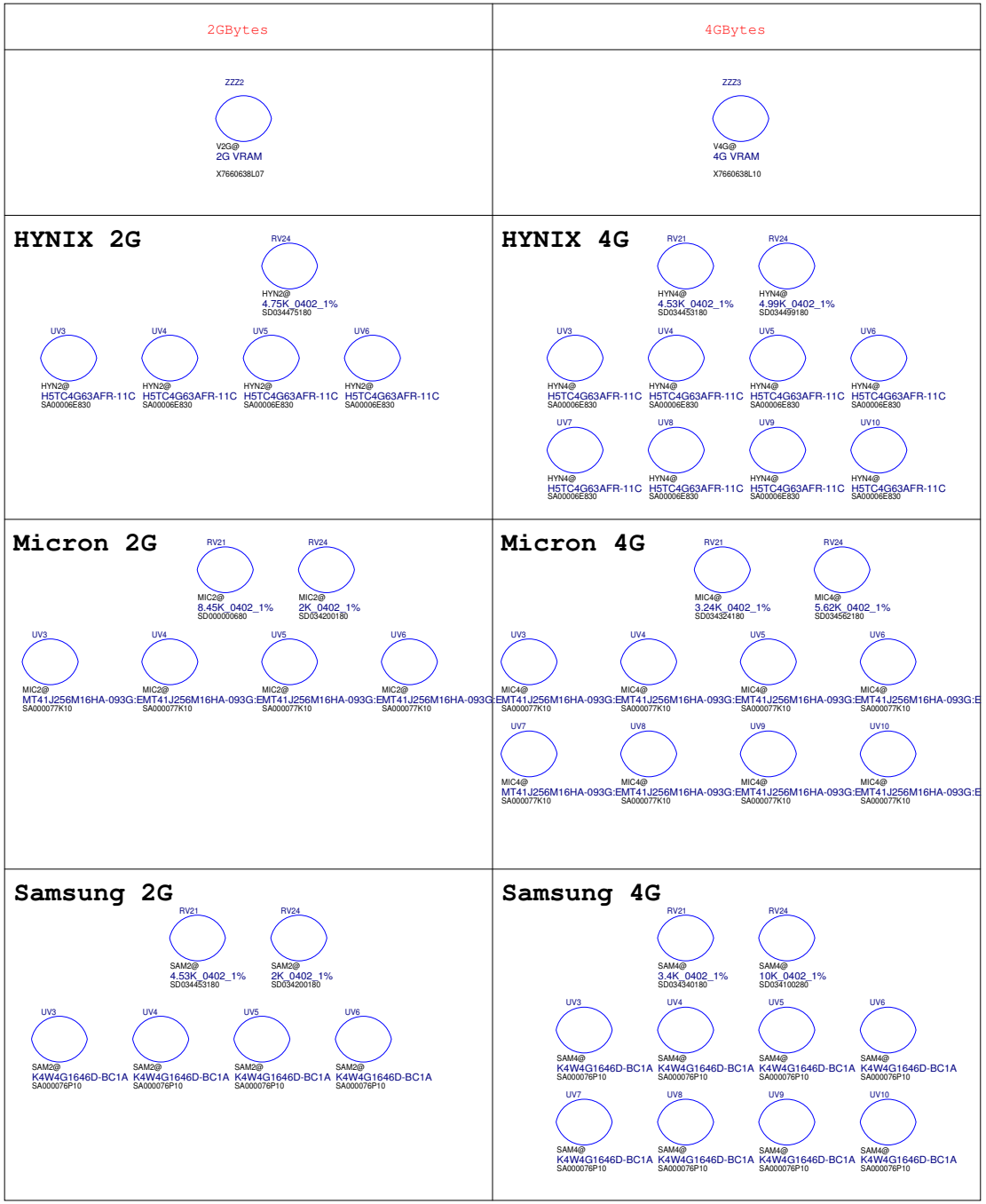
Meso XT_VRAM_STRAP

X76@ X76@

		Vendor UV3, UV4, UV5, UV6, UV7, UV8, UV9, UV10	ID	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV21	R_pd RV24
2GBytes	HYN2@	Hynix 2G SA00006E830 256Mx16 H5TC4G63AFR-11C	0	0	0	0	NC	4.75K
2GBytes	MIC2@	Micron 2G SA000077K10 256Mx16 MT41J256M16HA-093G:E	1	0	0	1	8.45K	2K
2GBytes	SAM2@	Samsung 2G SA000076P10 256Mx16 K4W4G1646D-BC1A	2	0	1	0	4.53K	2K
			3	0	1	1	6.98K	4.99K
4GBytes	HYN4@	Hynix 4G SA00006E830 256Mx16 H5TC4G63AFR-11C	4	1	0	0	4.53K	4.99K
4GBytes	MIC4@	Micron 4G SA000077K10 256Mx16 MT41J256M16HA-093G:E	5	1	0	1	3.24K	5.62K
4GBytes	SAM4@	Samsung 4G SA000076P10 256Mx16 K4W4G1646D-BC1A	6	1	1	0	3.4K	10K
			7	1	1	1	4.75K	NC

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.



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Issued Date	2014/09/01	Deciphered Date	2015/09/01

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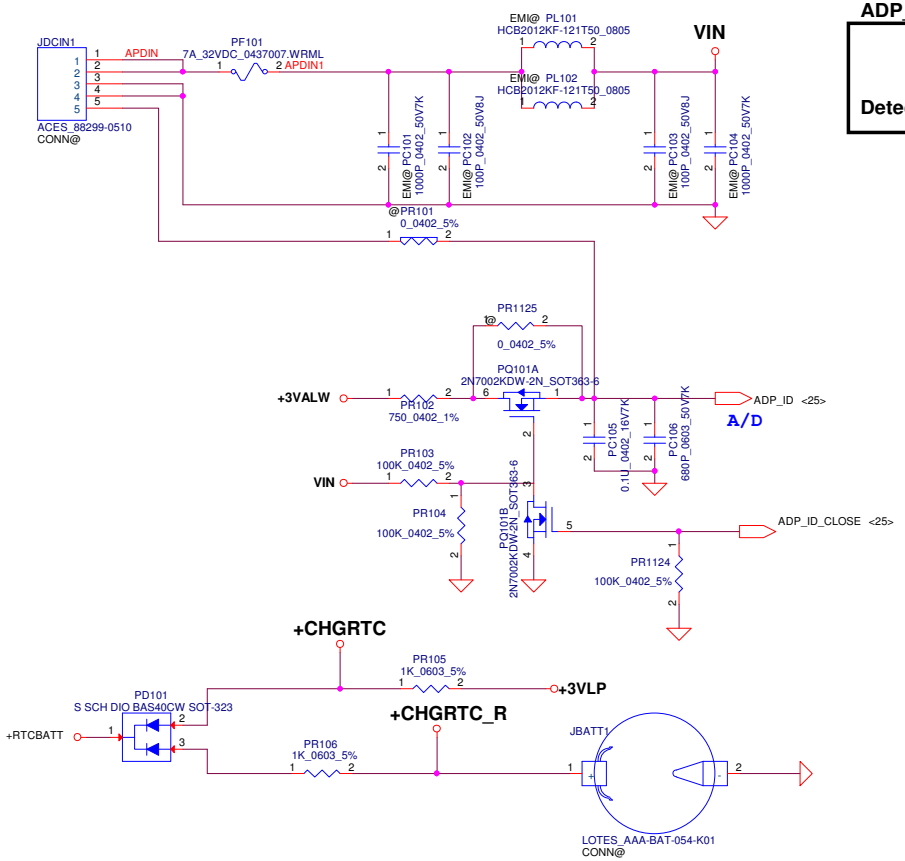
Compal Electronics, Inc.

Title: VGA Notes List

Size: C | Document Number: LA-C281 | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 37 of 50



ADP_ID

AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98

RTC Battery

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: **PWR DCIN / RTC Battery**

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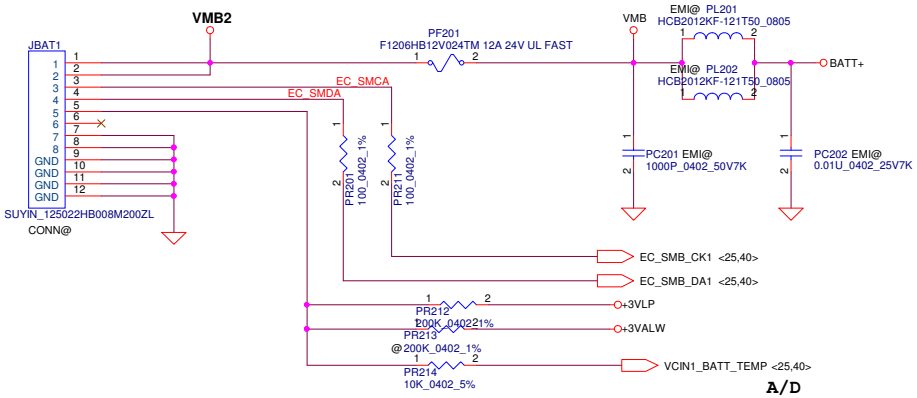
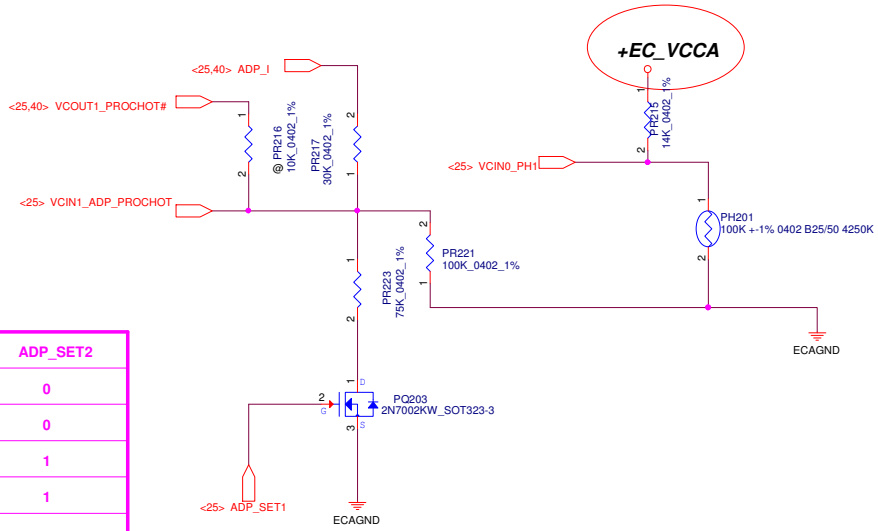
Date: Friday, February 06, 2015 | Sheet 38 of 50



A/D

PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

20120314
Change to +EC_VCCA from +3VLP



	ADP_SET1	ADP_SET2
45W adapter	0	0
65W adapter	1	0
90W adapter	0	1
135W adapter	1	1

135W: 150W active, 135W recovery
90W : 120W active, 90W recovery
65W : 85W active, 65W recovery
45W : 65W active, 45W recovery

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Compal Electronics, Inc.

Title: **PWR-BATTERY CONN/OTP**

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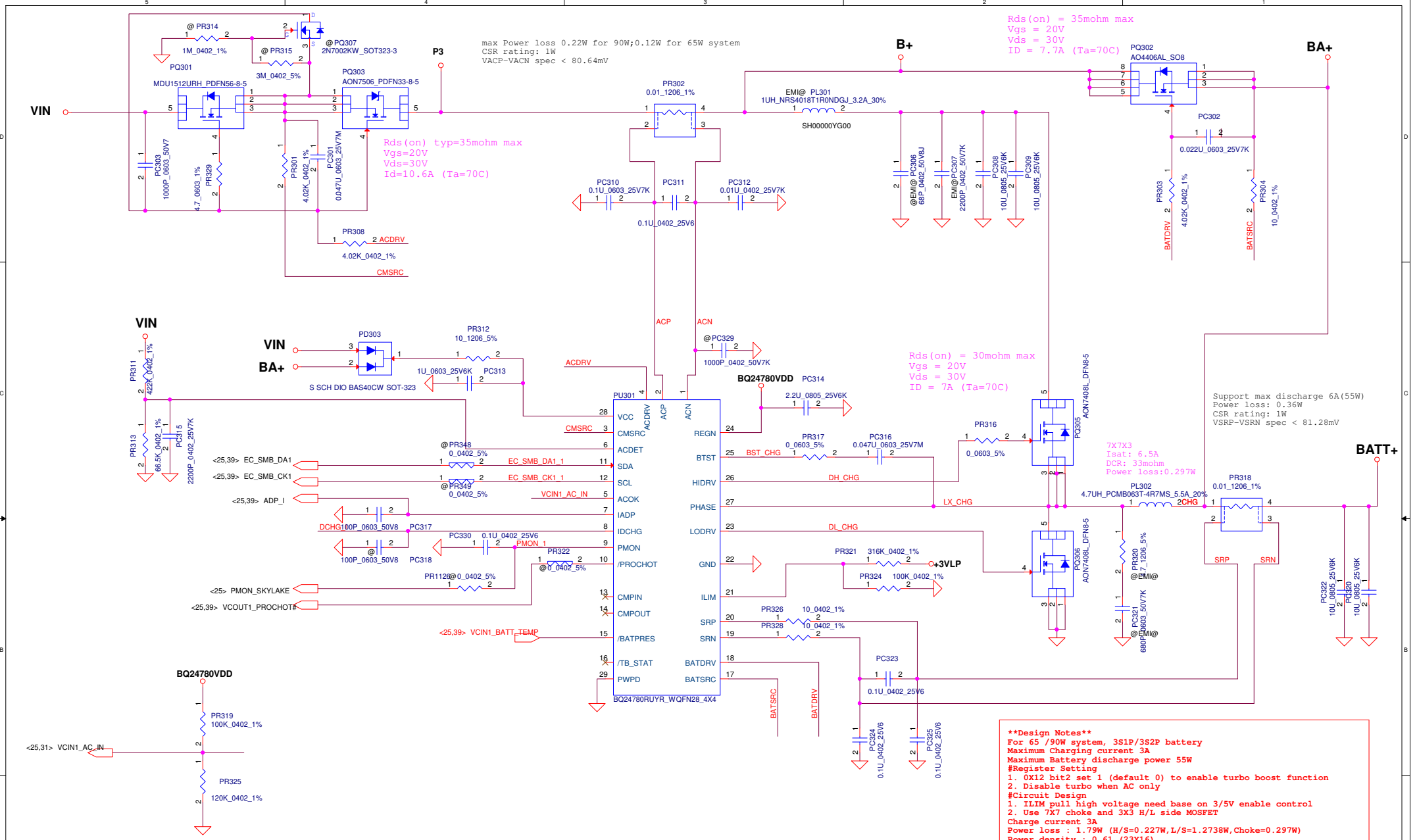
Date: Friday, February 06, 2015 | Sheet 39 of 50



Vin Dectector	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(316+100)/20/0.01
= 3.966 A

Design Notes
For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3A
Maximum Battery discharge power 55W
#Register Setting
1. 0X12 bit2 set 1 (default 0) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ILIM pull high voltage need base on 3/5V enable control
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOVP : VCC voltage > 24V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting (default:Disable)
4. CHGOCP : based on charge current setting
5. BATOVP : 103-106%
6. BATLOWV : 2.6V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default:Disable)
9. IFAULT LOW : 230mV (default)

Security Classification	Compal Secret Data		
Issued Date	2013/11/05	Deciphered Date	2015/11/05

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Compal Electronics, Inc.

Title: BQ24780

Size: Custom | Document Number: Z_BDW | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 40 of 50

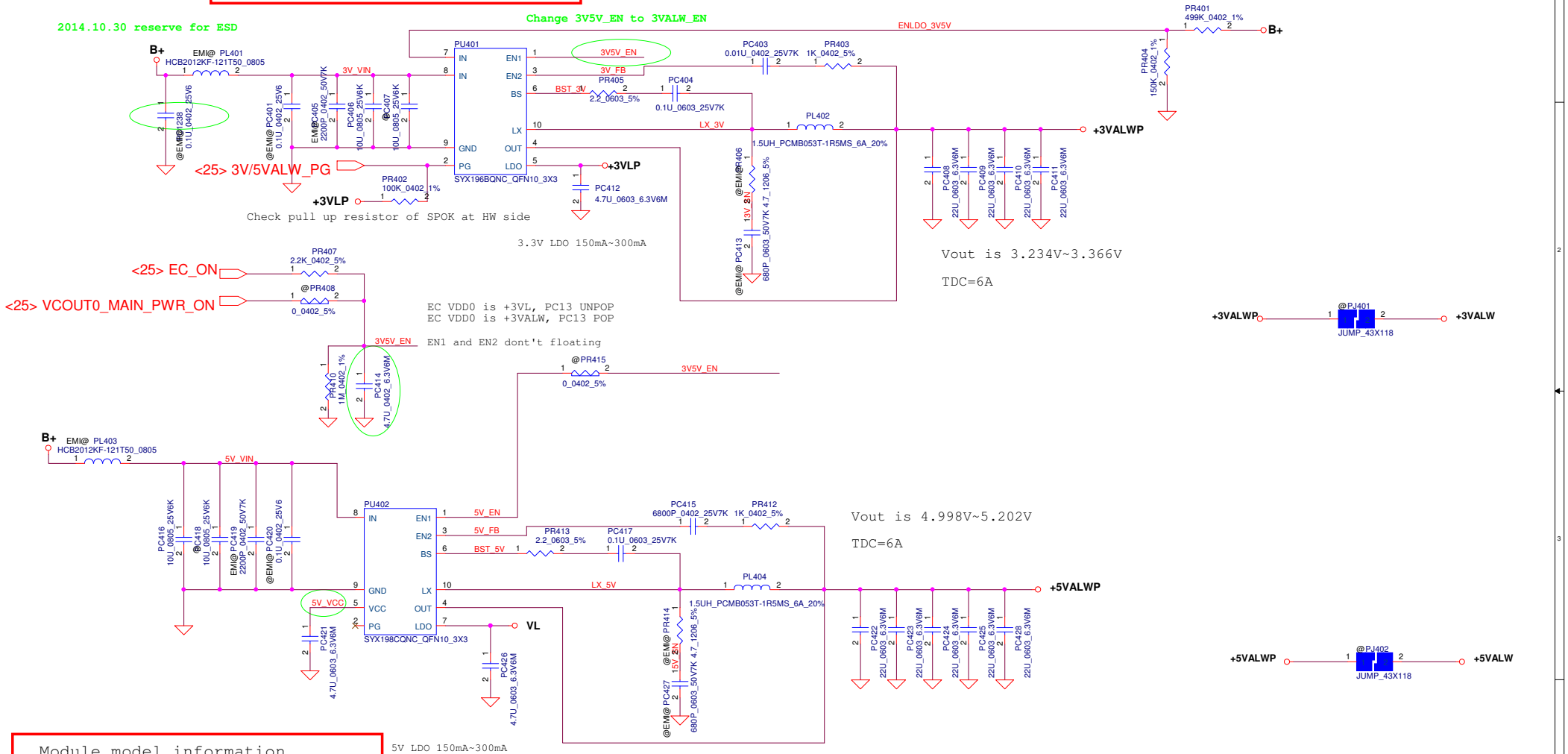
Module model information

SY8208B_V2.mdd

EN1 and EN2 dont't floating

2014.10.30 reserve for ESD

Change 3V5V_EN to 3VALW_EN



Module model information

SY8208C_V2.mdd

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number: Z_BDW | Rev: 1.0

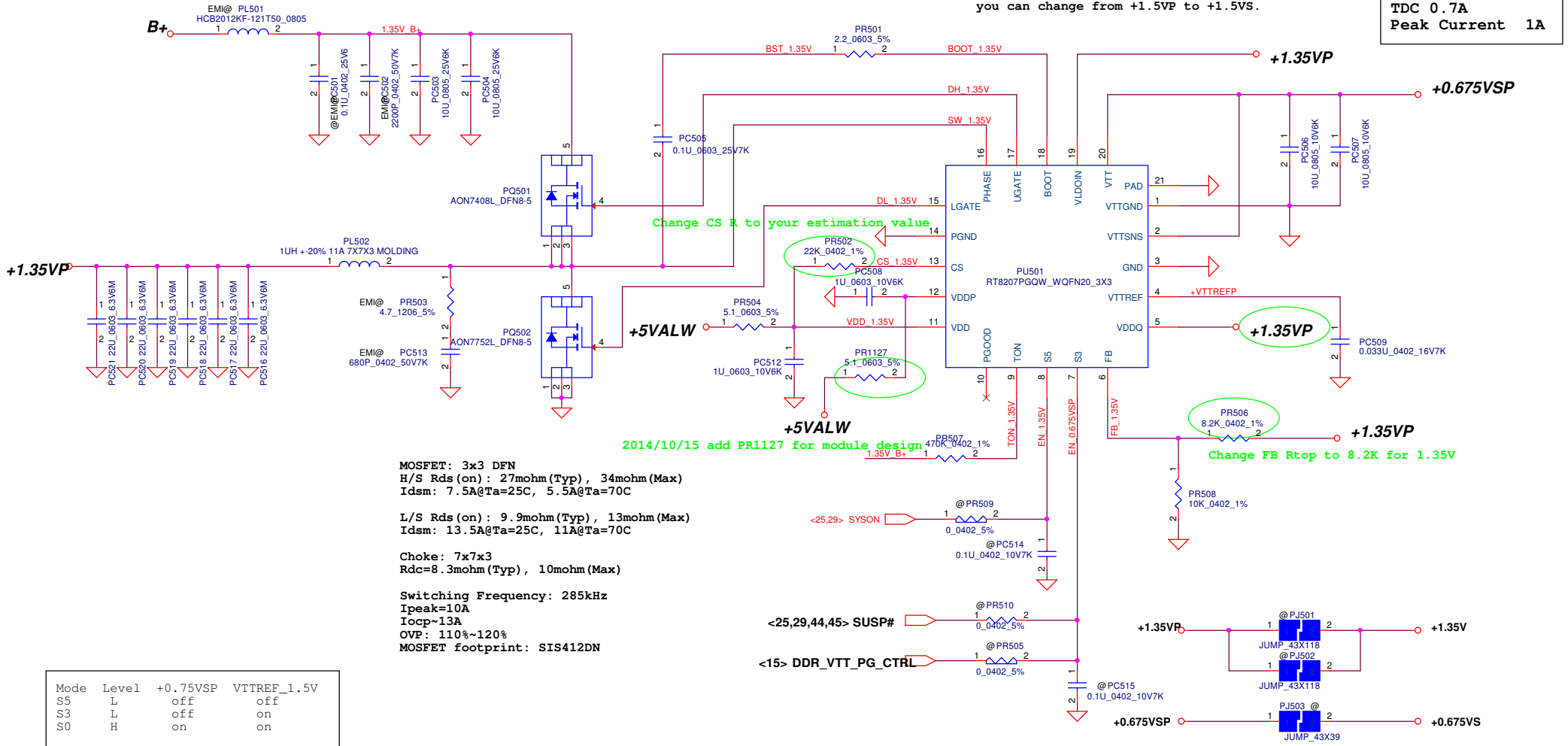
Date: Friday, February 06, 2015 | Sheet 41 of 50

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
MOSFET footprint: SIS412DN

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

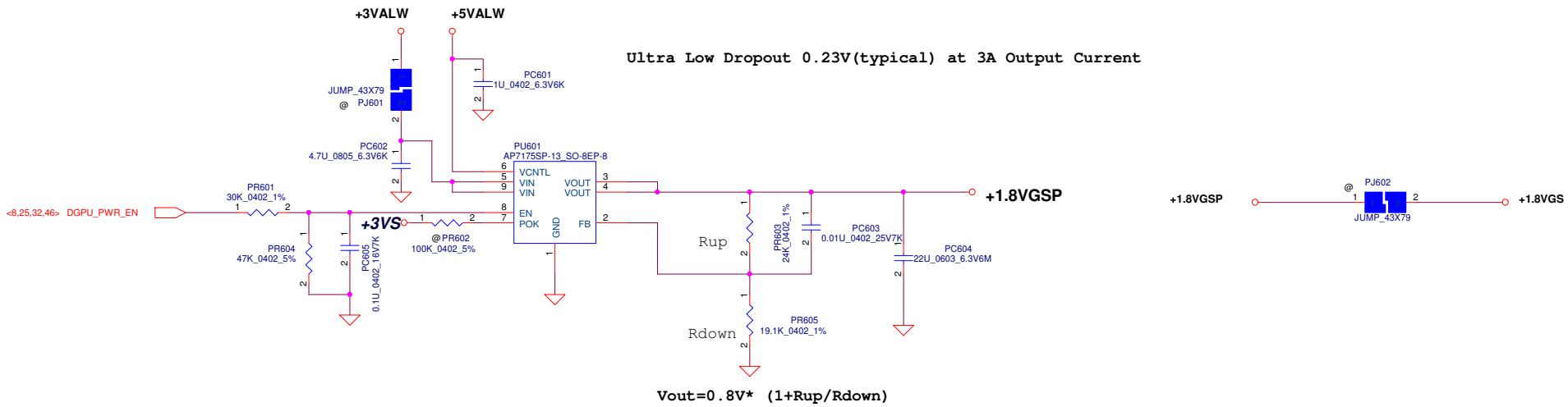
Title: RT8207M

Size: Custom | Document Number: Z_BDW | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 42 of 50

Module model information

APL5930_V1.mdd



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title: +1.8VGS-+0.95VVGS
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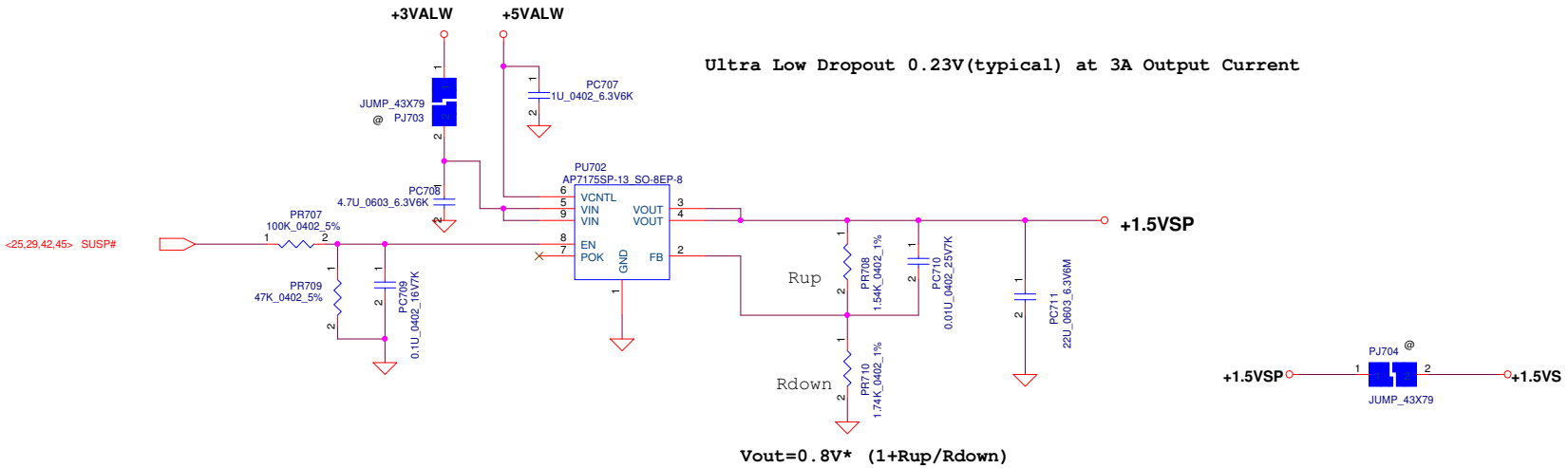

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title: +1.5VS
				Size: Custom; Document Number: Z_BDW; Rev: 1.0
				Date: Friday, February 06, 2015; Sheet 44 of 50

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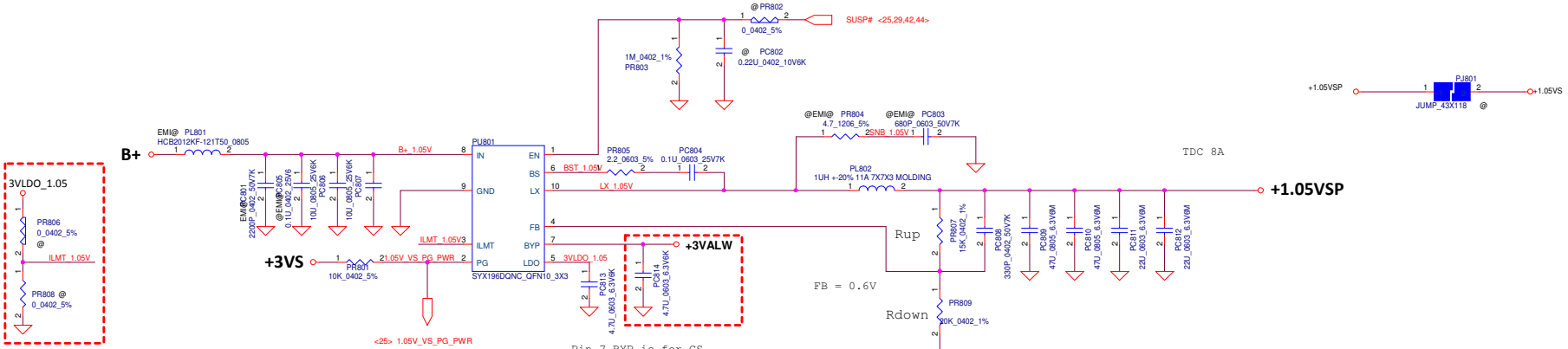
Module model information

SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 8A, 12A or 16A when this pin
is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)

Vout=1.05V

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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title: +1.05VS
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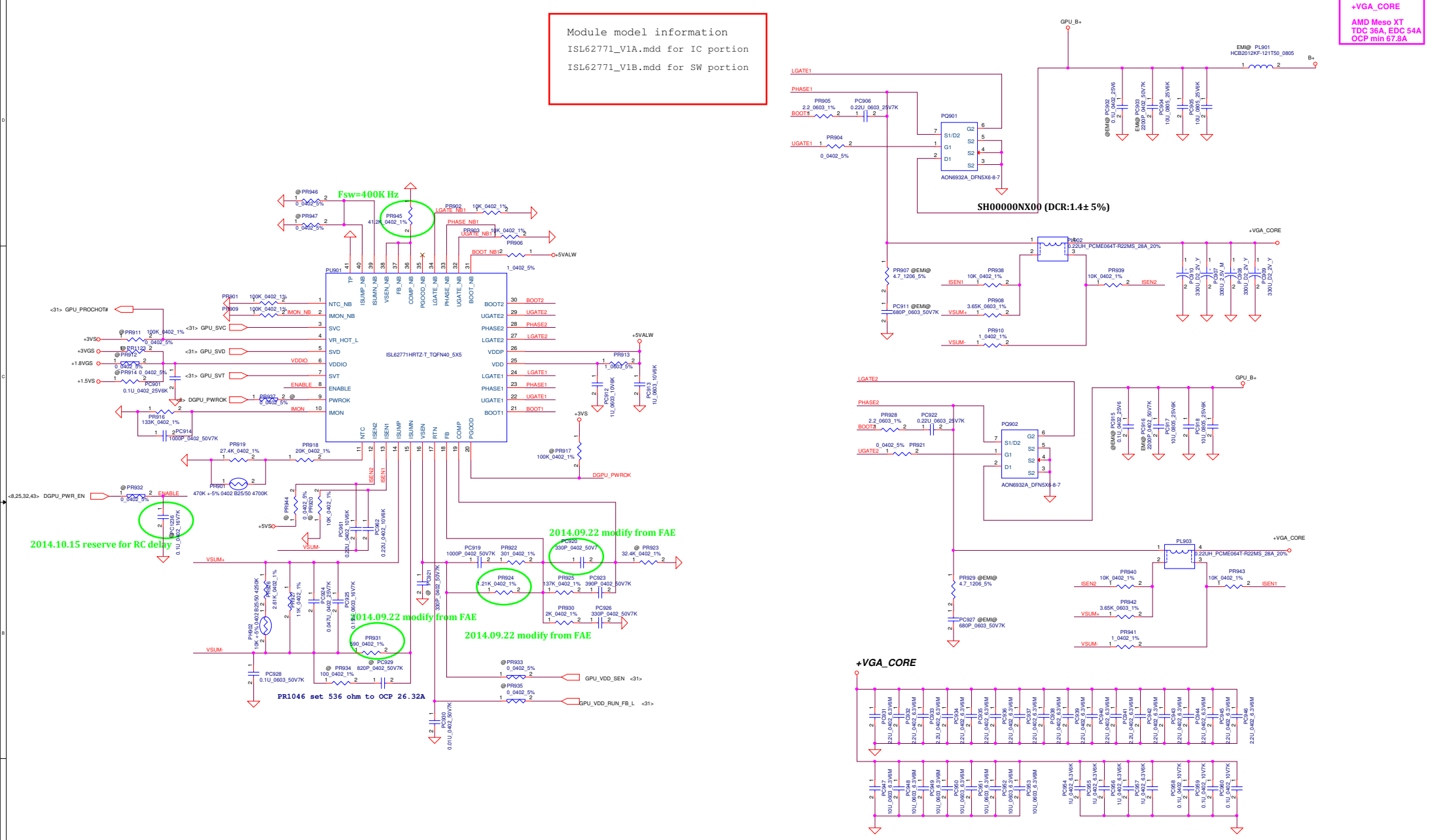
Module model information
ISL62771_V1A.mdd for IC portion
ISL62771_V1B.mdd for SW portion

+VGA_CORE
AMD Meso XT
TDC 36A, EDC 54A
OCP min 67.8A



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Compal Electronics, Inc.

Title: PWR-+VGA_CORE

Size: Custom | Document Number: Z_BDW | Rev: 1.0

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Module model information:
ISL95813 (for 15W & 28W CPU)

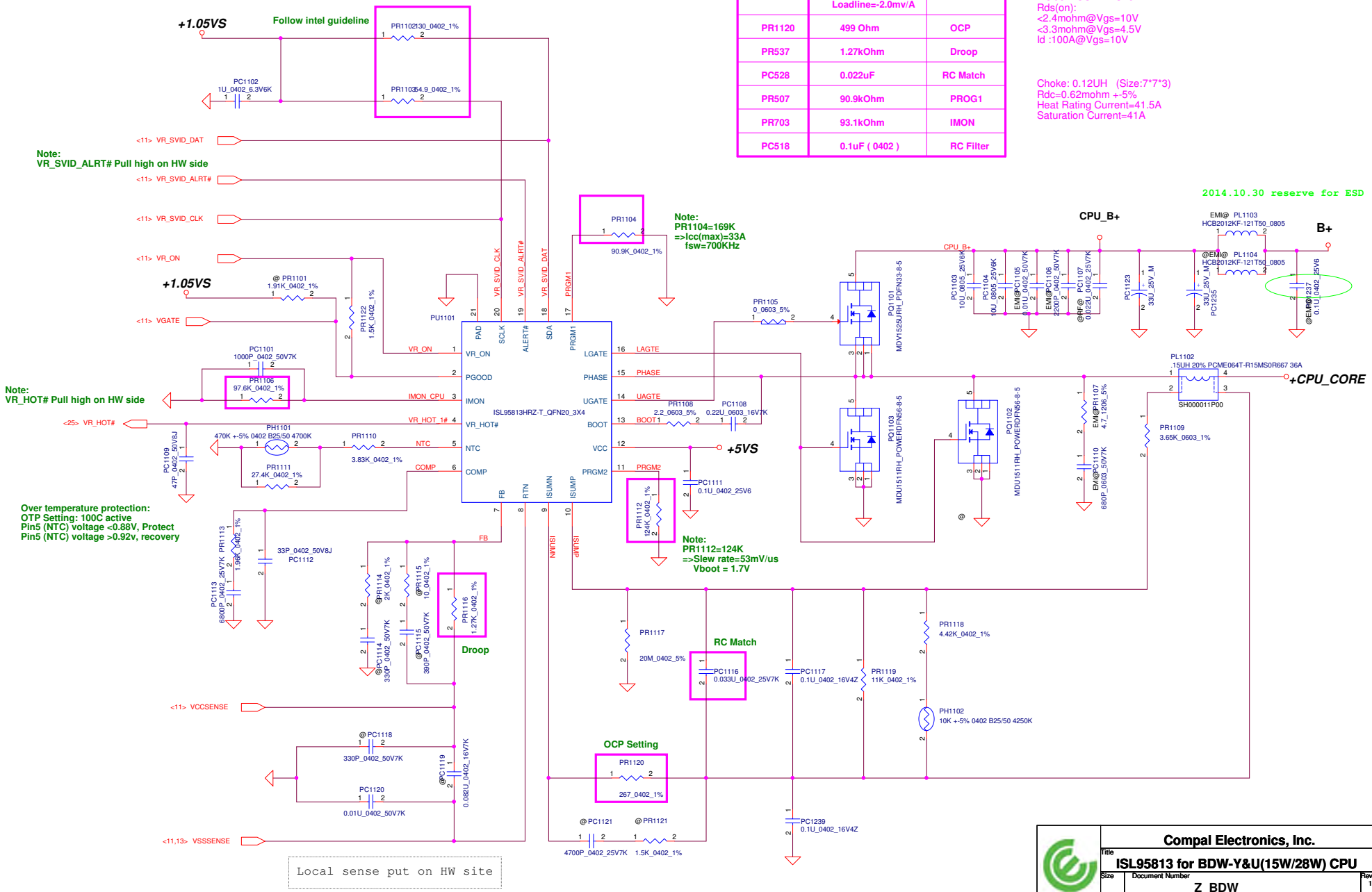
Base on BDW PDDG Rev_0_73		
Location	15W TDC 14A MAX 32A OCP 39A Loadline=-2.0mv/A	Note
PR1120	499 Ohm	OCP
PR537	1.27kOhm	Droop
PC528	0.022uF	RC Match
PR507	90.9kOhm	PROG1
PR703	93.1kOhm	IMON
PC518	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.12UH (Size:7*7*3)
Rdc=0.62mohm +-5%
Heat Rating Current=41.5A
Saturation Current=41A

2014.10.30 reserve for ESD

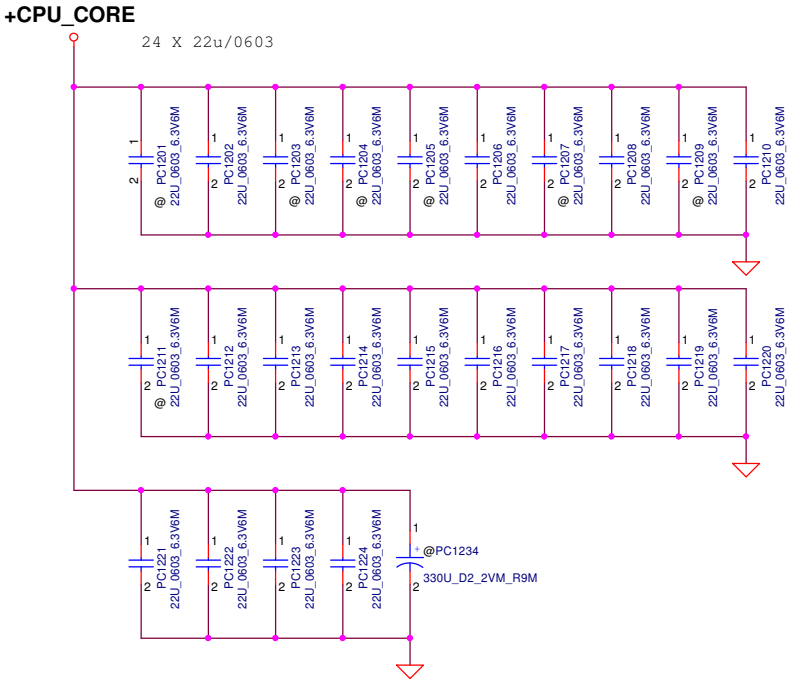


Compal Electronics, Inc.

Title: ISL95813 for BDW-Y&U(15W/28W) CPU

Size | Document Number: Z_BDW | Rev 1.0

Date: Friday, February 06, 2015 | Sheet 47 of 50



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Compal Electronics, Inc.

Title: **PWR-PROCESSOR DECOUPLING**

Size: Custom | Document Number: **Z_BDW** | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 48 of 50

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	reserve VGA_CORE RC delay	P46	add PC1236	2014.10.15	SIV
2	reserve 0.1uF for ESD	P41/P47	add PC1237,PC1238	2014.10.30	SIV
3					
4					
6					
7					
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17					

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Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Friday, February 06, 2015 | Sheet 49 of 50

Version change list (P.I.R. List) for HW

Item	Reason for change	PG#	Modify List		Phase
1	Reserve clean CMOS circuit	P06	reserve R80,Q27	2014.10.28	SIV
2	HDMI Design	P18	add R1650,R1651,R1652,R1653,R1654,R1655,R1656,R1657,R1658,R1659,R1660,R1661	2014.10.28	SIV
3	USB2.0 design for EMI request	P24	add R1676 and R1677	2014.10.28	SIV
4	Change commom chock symbol for EMI request	P24	change L12~L18	2014.10.28	SIV
5	Add FAN_ID for EC request	P25	add R516 and R517	2014.10.29	SIV
6	Audio design for EMI request	P36	add CA28,CA29,CA30,CA31	2014.10.29	SIV
7	Audio design for EMI request	P36	change from RA19,RA20 to LA2,LA3	2014.10.29	SIV
8	Audio design for EMI request	P36	add LA1	2014.10.29	SIV
9	+1.35V design for EMI request	P15	add C320~C324	2014.10.29	SIV
10	modify +MEM_GFX power sequence	P32	change C901 from 0.01uF to 0.1uF	2014.10.30	SIV
11	LAN design change for wake on lan	P26	delete RL18, add J6,J7	2014.11.13	SIT
12	Change pcb foot print by DFX request	P20,P24	change JIO1,JODD1,JHDMI pcb footprint	2014.12.08	SIT
13	Change for VGA power sequence	P32	change CV35 value	2014.12.08	SIT
14	Change Audio PCBEEP SCH by verdor suggestion	P27	add RA35,RA37,CA90,CA91,RA39 / DELETE CA23,CA24,RA36,RA34,CA25	2014.12.15	SIT
15	Modify LED BOM setting	P27	modify LED1,LED2,LED3,LED4,LED5,LED6 BOM setting	2014.12.15	SIT
16					
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Security Classification: Compal Secret Data
Issued Date: 2011/06/15 Deciphered Date: 2012/07/11

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Compal Electronics, Inc.

Title: HW-PIR1

Size: C | Document Number: LA-C281P | Rev: 1.0

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