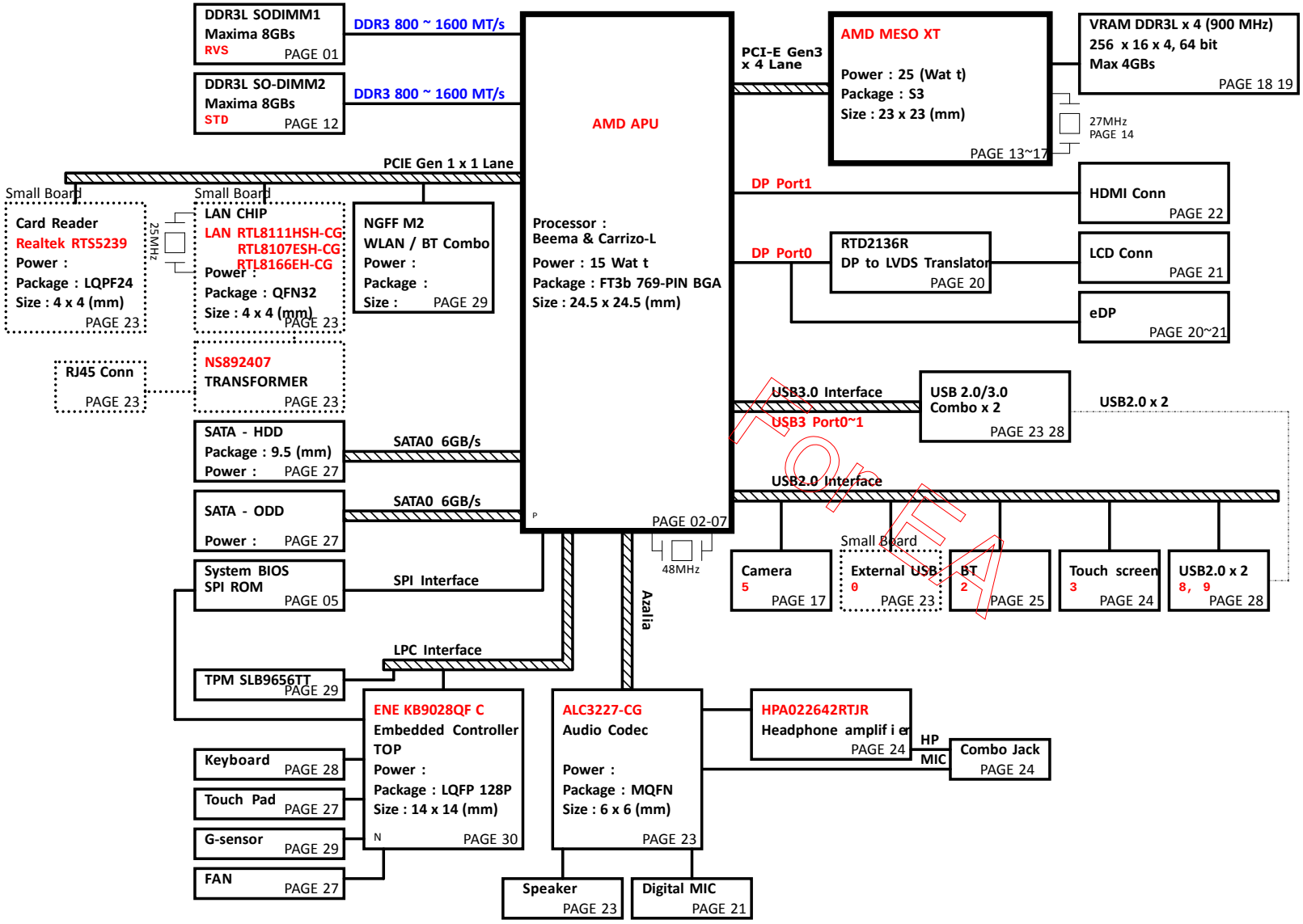
Chocolate AMD Beema DIS/UMA (14.0"/15.6"/17.3")

01



PCB 10L STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1 (HIGH)
- LAYER 4 : IN2 (LOW)
- LAYER 5 : SVCC
- LAYER 6 : GND
- LAYER 7 : IN3 (HIGH)
- LAYER 1 : IN4 (HIGH)
- LAYER 1 : GND
- LAYER 1 : BOT

Power Source

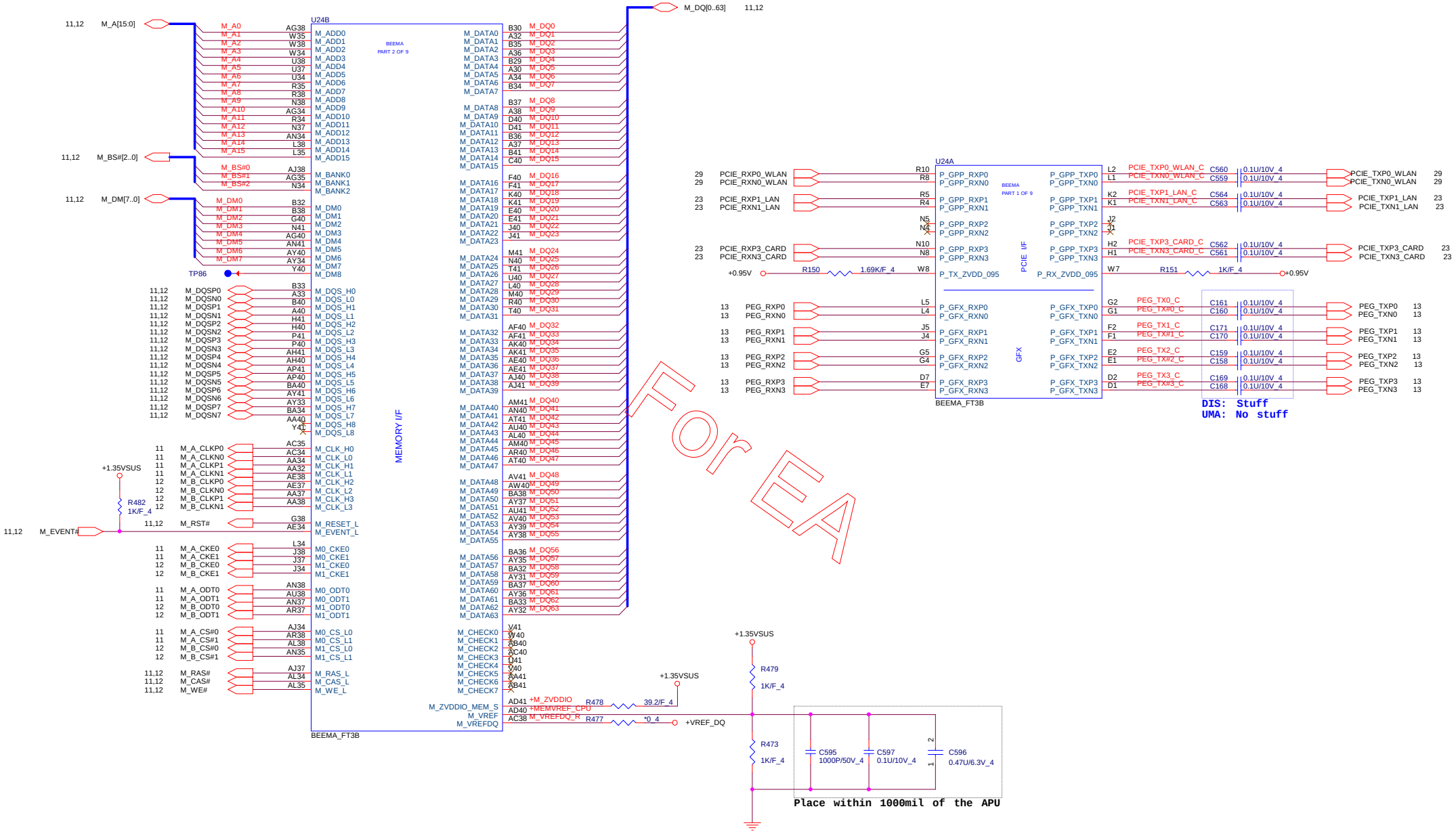
- BQ24728H — System Charge Power (+BATCHG) — PAGE 31
- RT7238B / RT7238C — System Power (+3VPCU/+5VPCU/ +3VS5/+5VS5) — PAGE 32
- RT8231BGQW — System Memory Power (+1.35VSUS/ +0.65V_DDR_VTT) — PAGE 33
- APW8824 / APW8824 — Processor Power (+0.95VS5/+1.5VS5) — PAGE 34
- AOZ1267QI-02 / RT8068AZQW — Processor Power (+0.95V/+1.8VS5) — PAGE 35
- ISL62771 — Processor Power (+VCC_CORE/+VDDNB_CORE) — PAGE 36 37
- APL3523A * 3 — Load switch (+3V/+3VLANVCC/+5V/+3VSUS/+1.5V/+1.8V) — PAGE 38
- RT8899AGQW — DGPU Power (+VGA_CORE/+1.35V_VGA) — PAGE 38 40
- RT8068A / APL3523A — DGPU Power (+0.95V_VGA/+1.8V_VGA/+3V_VGA) — PAGE 41

PROJECT : X22
Quanta Computer Inc.

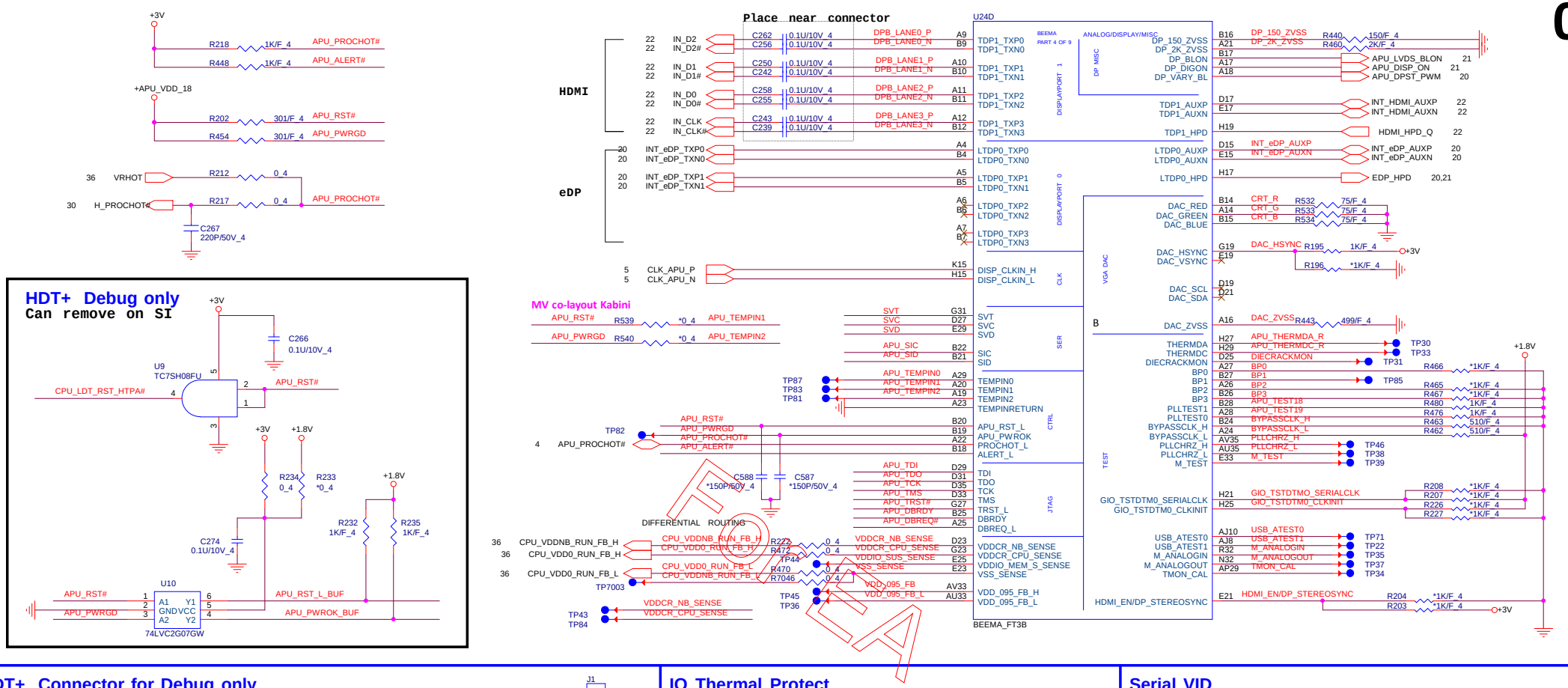
Size	Document Number	Rev
	Block Diagram	1A

NB5/RD3

Date: Tuesday, November 18, 2014 | Sheet 1 of 41



PROJECT :	Y2x
Quanta Computer Inc.	
NB5/RD3	
Size	Document Number: MEM/PCIE (1/6) — Rev 1A
Date: Tuesday, November 18, 2014	Sheet 2 of 41

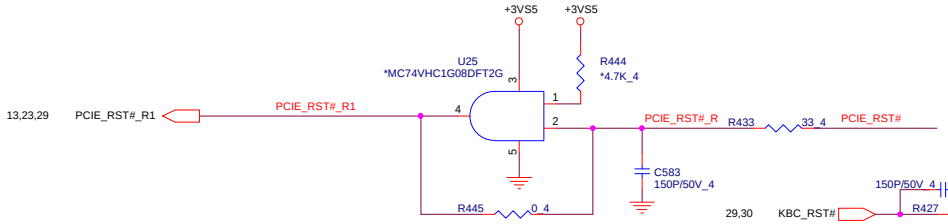


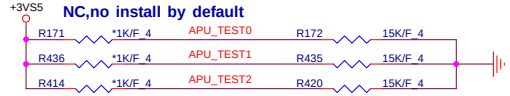
PROJECT : Y2x
Quanta Computer Inc.

Size	Document Number	Rev
	DIS/MI (2/6)	1A

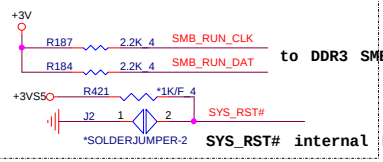
NB5/RD3

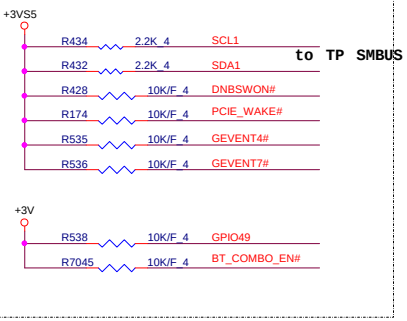
Date: Tuesday, November 18, 2014 Sheet 3 of 41

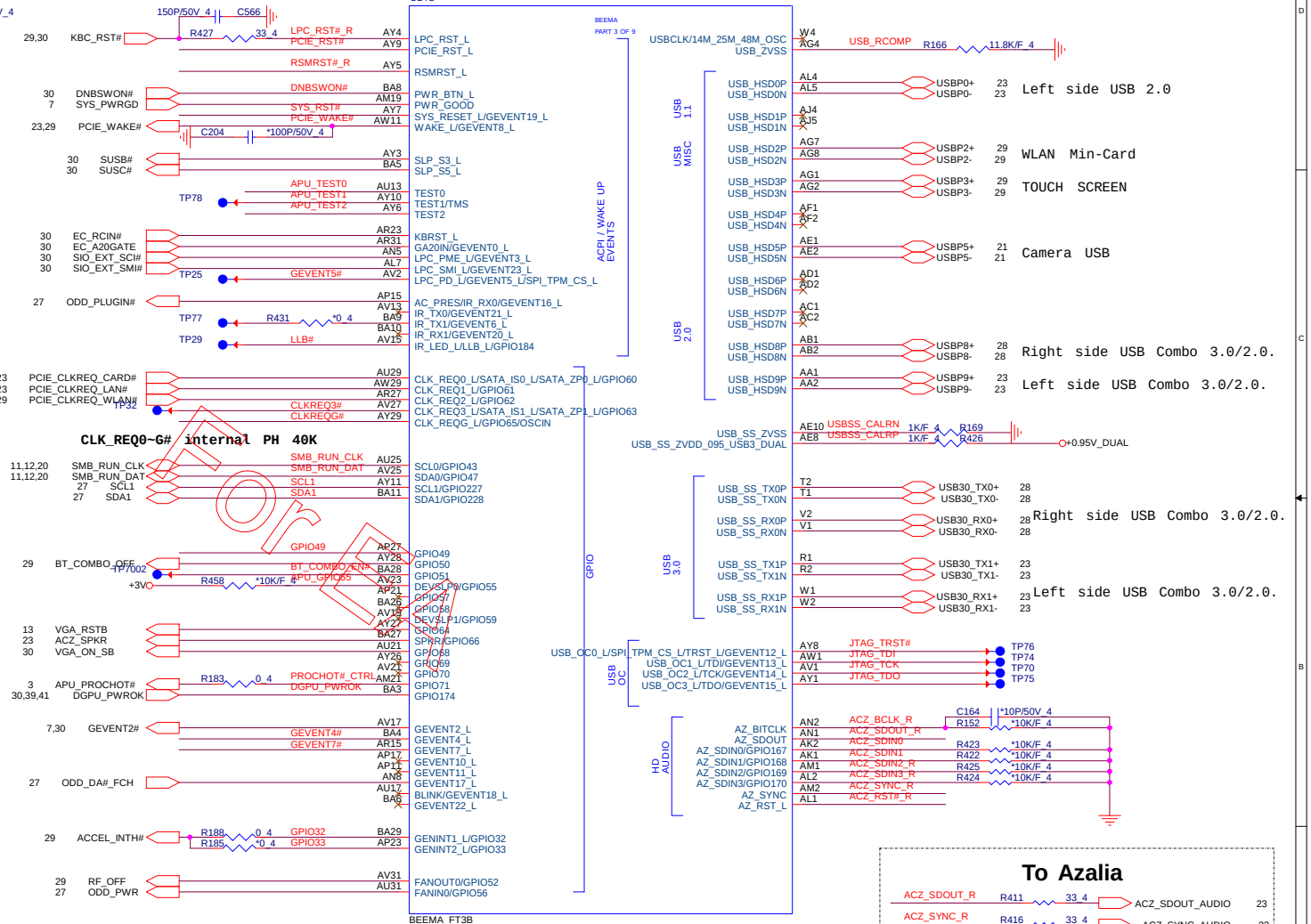




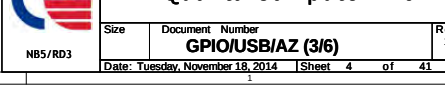
TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled

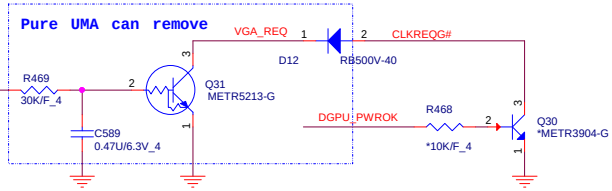


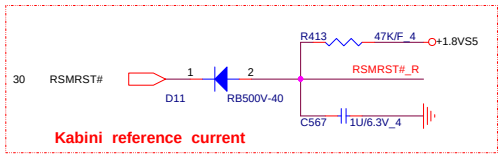




To Azalia







PROJECT : Y2x
Quanta Computer Inc.

Size	Document Number	Rev
NB5/RD3	GPIO/USB/AZ (3/6)	1A
Date: Tuesday, November 18, 2014	Sheet 4 of 41	

BOARD ID SETTING

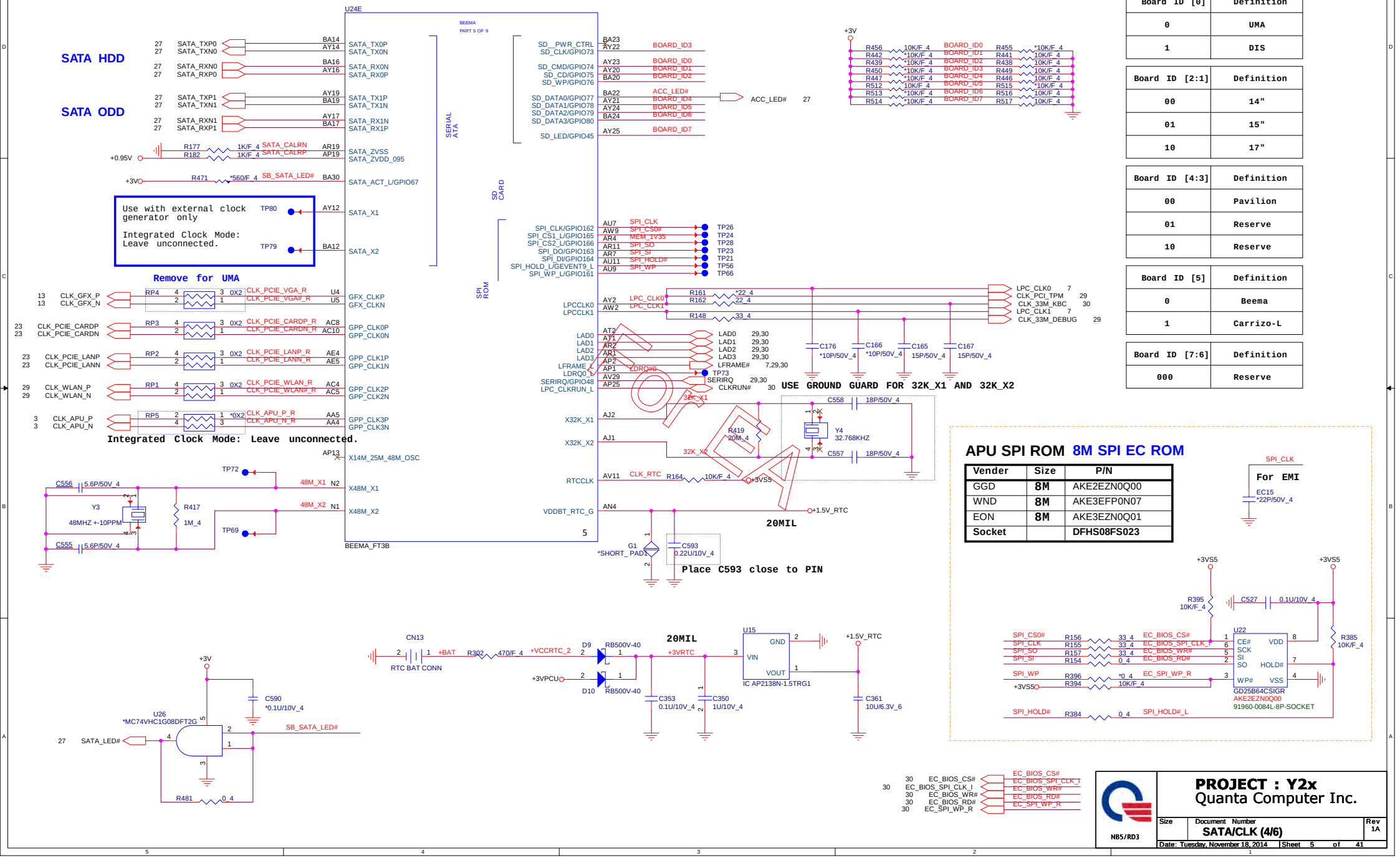
Board ID [0]	Definition
0	UMA
1	DIS

Board ID [2:1]	Definition
00	14"
01	15"
10	17"

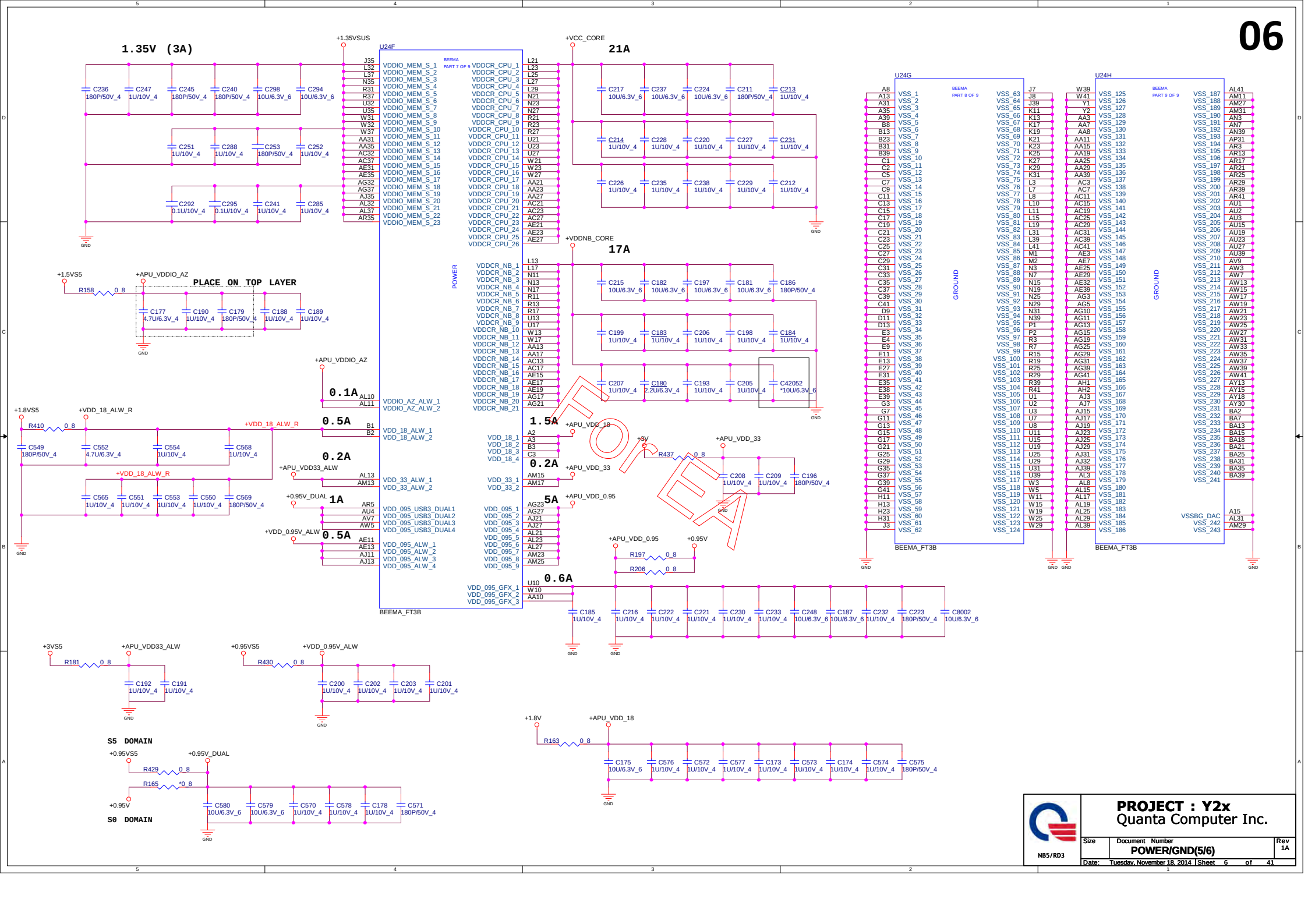
Board ID [4:3]	Definition
00	Pavilion
01	Reserve
10	Reserve

Board ID [5]	Definition
0	Beema
1	Carrizo-L

Board ID [7:6]	Definition
000	Reserve



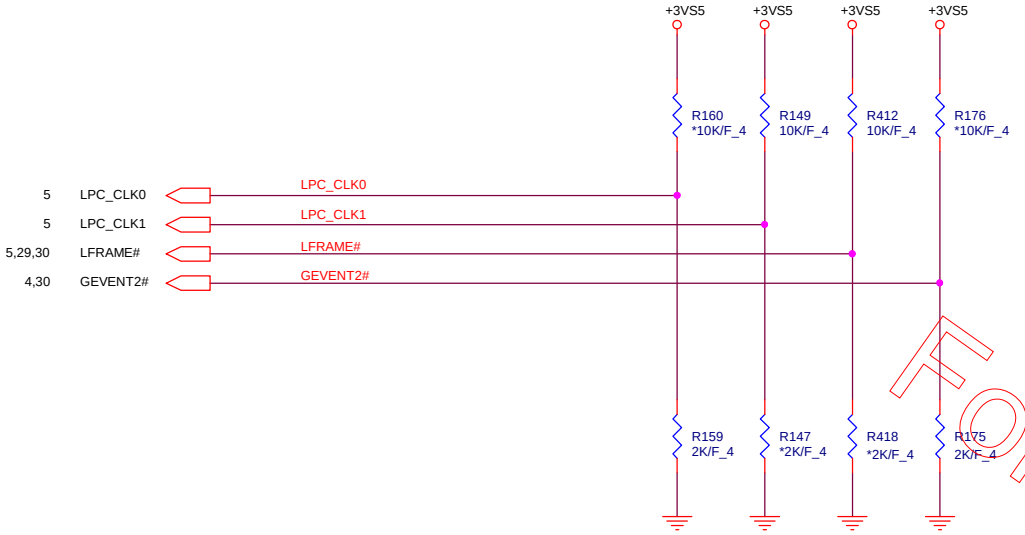
PROJECT :	Y2x
	Quanta Computer Inc.
Size	Document Number: SATA/CLK (4/6) — Rev 1A
NB5/RD3	Date: Tuesday, November 18, 2014 — Sheet 5 of 41



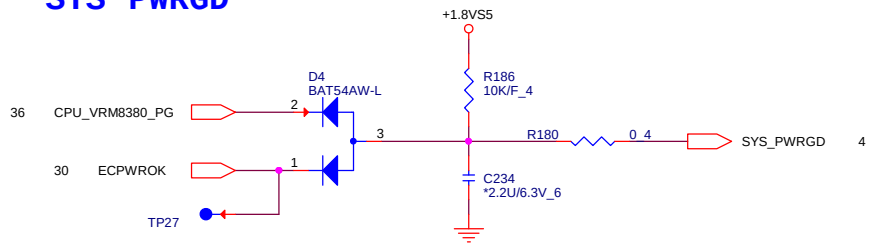
PROJECT : Y2x			
Quanta Computer Inc.			
NB5/RD3	Size	Document Number: POWER/GND(5/6)	Rev: 1A
	Date: Tuesday, November 18, 2014	Sheet 6 of 41	

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



SYS PWRGD



REQUIRED STRAPS

	LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH	BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW	BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

NB5/RD3

PROJECT : Y2x
Quanta Computer Inc.

Size	Document Number	Rev
	STRAP (6/6)	1A

Date: Tuesday, November 18, 2014 Sheet 7 of 41

NB5

PROJECT : Y71
Quanta Computer Inc.

Size	Document Number	Rev
B	**Reserved**	1A

Date: Tuesday, November 18, 2014 | Sheet 8 of 41

09

For EA

NB5

PROJECT : Y71
Quanta Computer Inc.

Size	Document Number	Rev
B	**Reserved**	1A

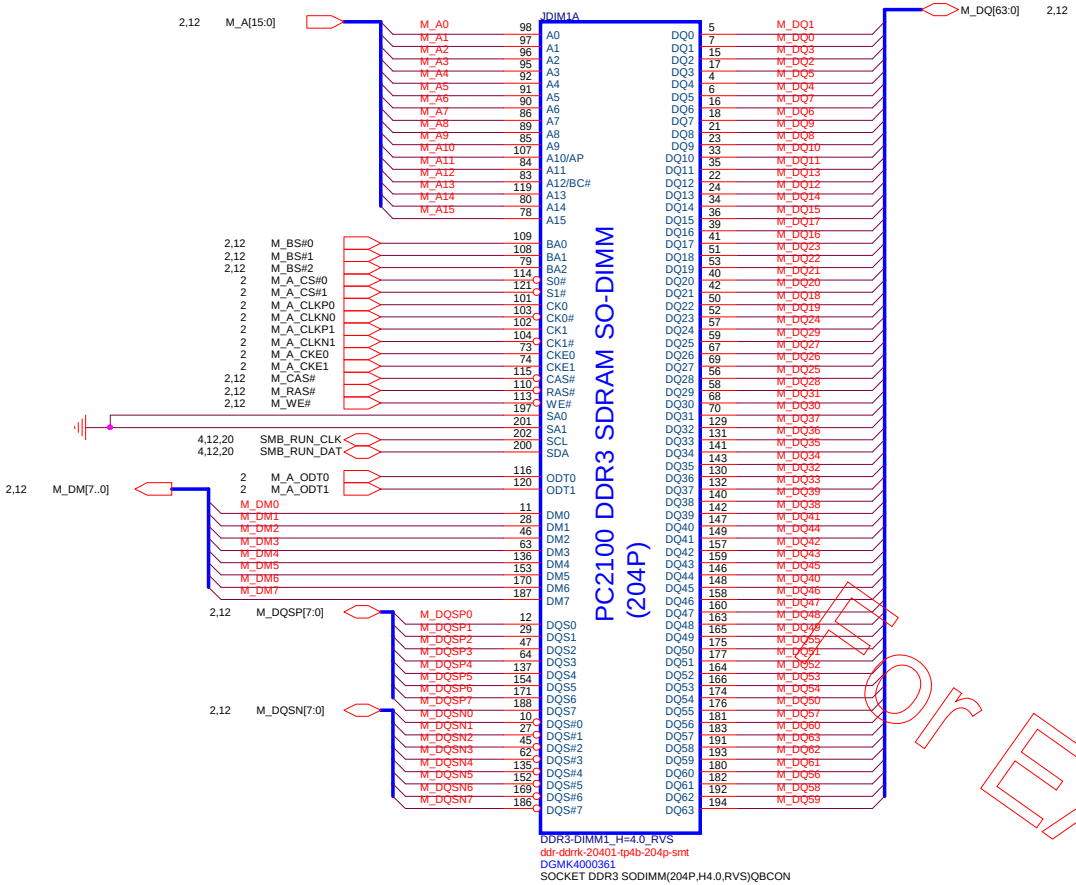
Date: Tuesday, November 18, 2014 Sheet 9 of 41

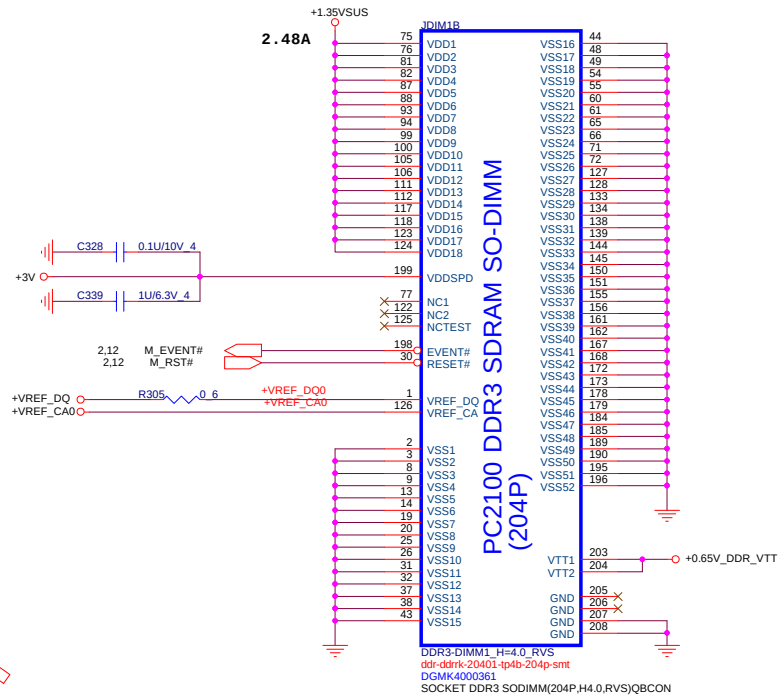
NB5

PROJECT : Y71
Quanta Computer Inc.

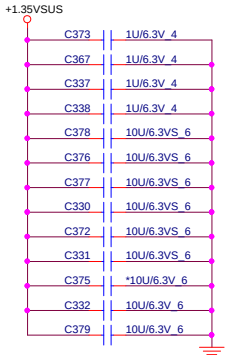
Size	Document Number	Rev
B	**Reserved**	1A

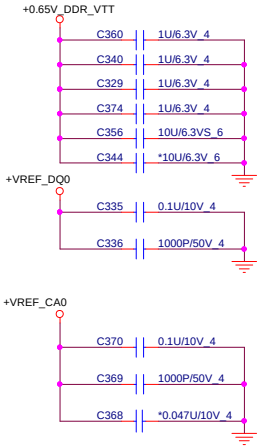
Date: Tuesday, November 18, 2014 | Sheet 10 of 41

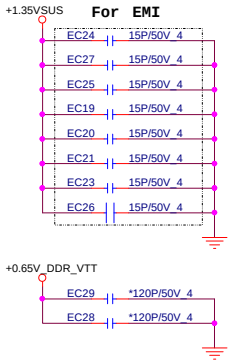




Place these Caps near So-Dimm0.

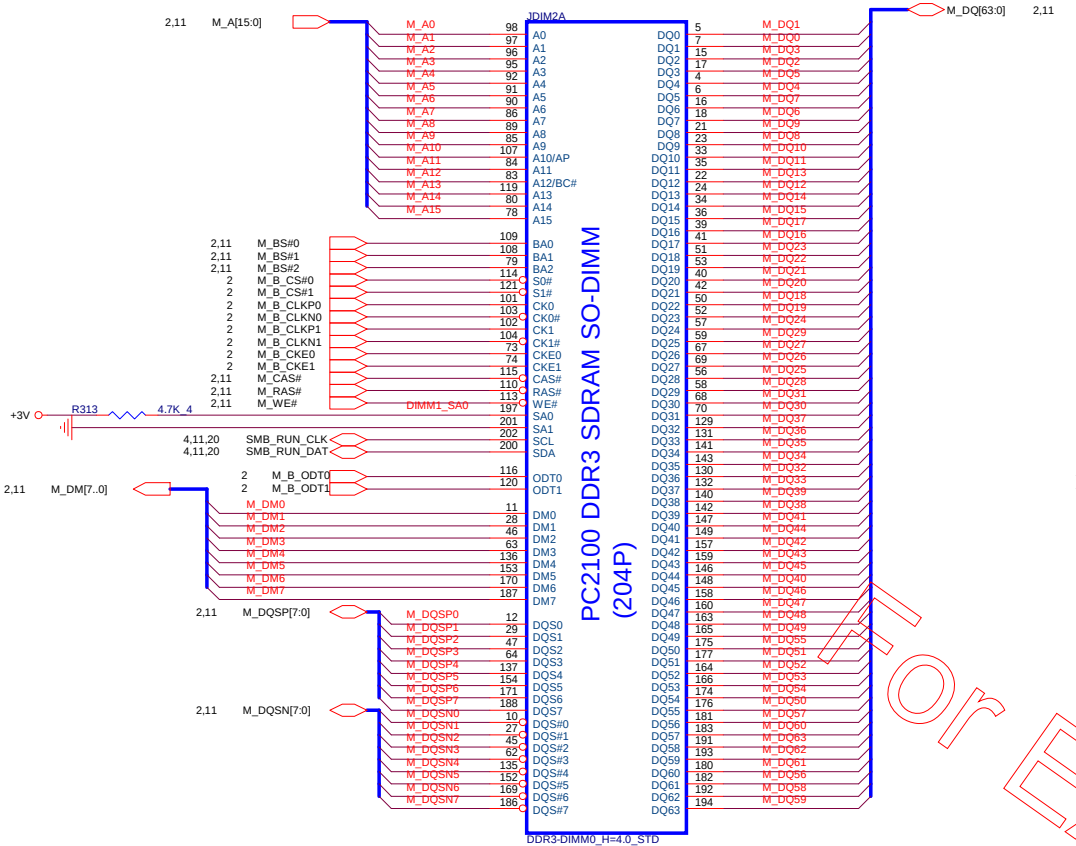


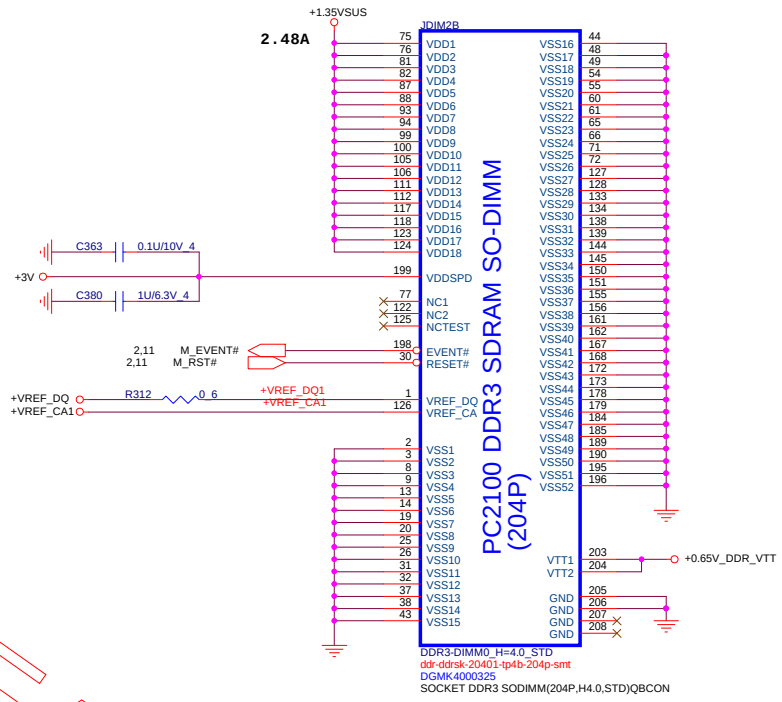




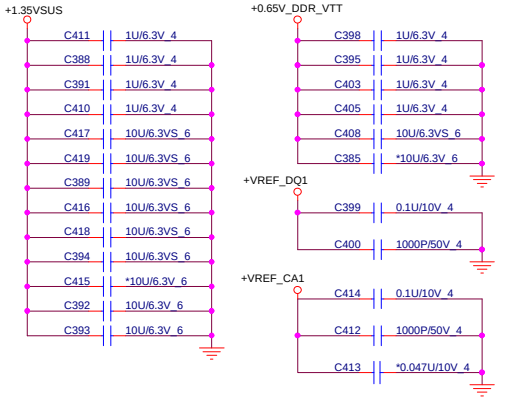
PROJECT : Y2x
Quanta Computer Inc.

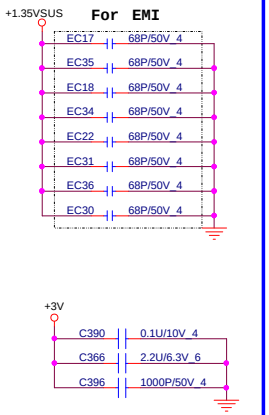
Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (4.0H)	1A
NB5/RD3	Date: Tuesday, November 18, 2014	Sheet 11 of 41

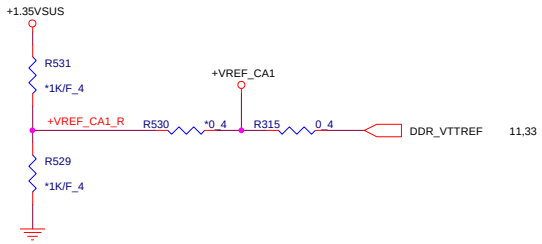




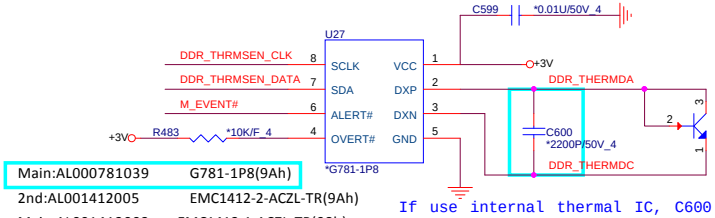
Place these Caps near So-Dimm1.





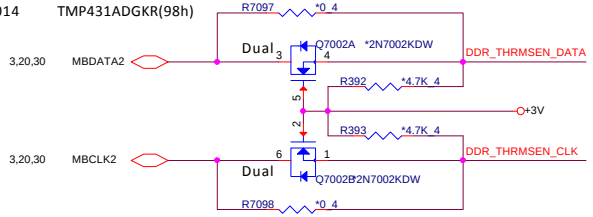


Local Thermal Sensor For DDR3



Main:AL000781039	G781-1P8(9Ah)
2nd:AL001412005	EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003	EMC1412-1-ACZL-TR(98h)
2nd:AL000431014	TMP431ADGKR(98h)

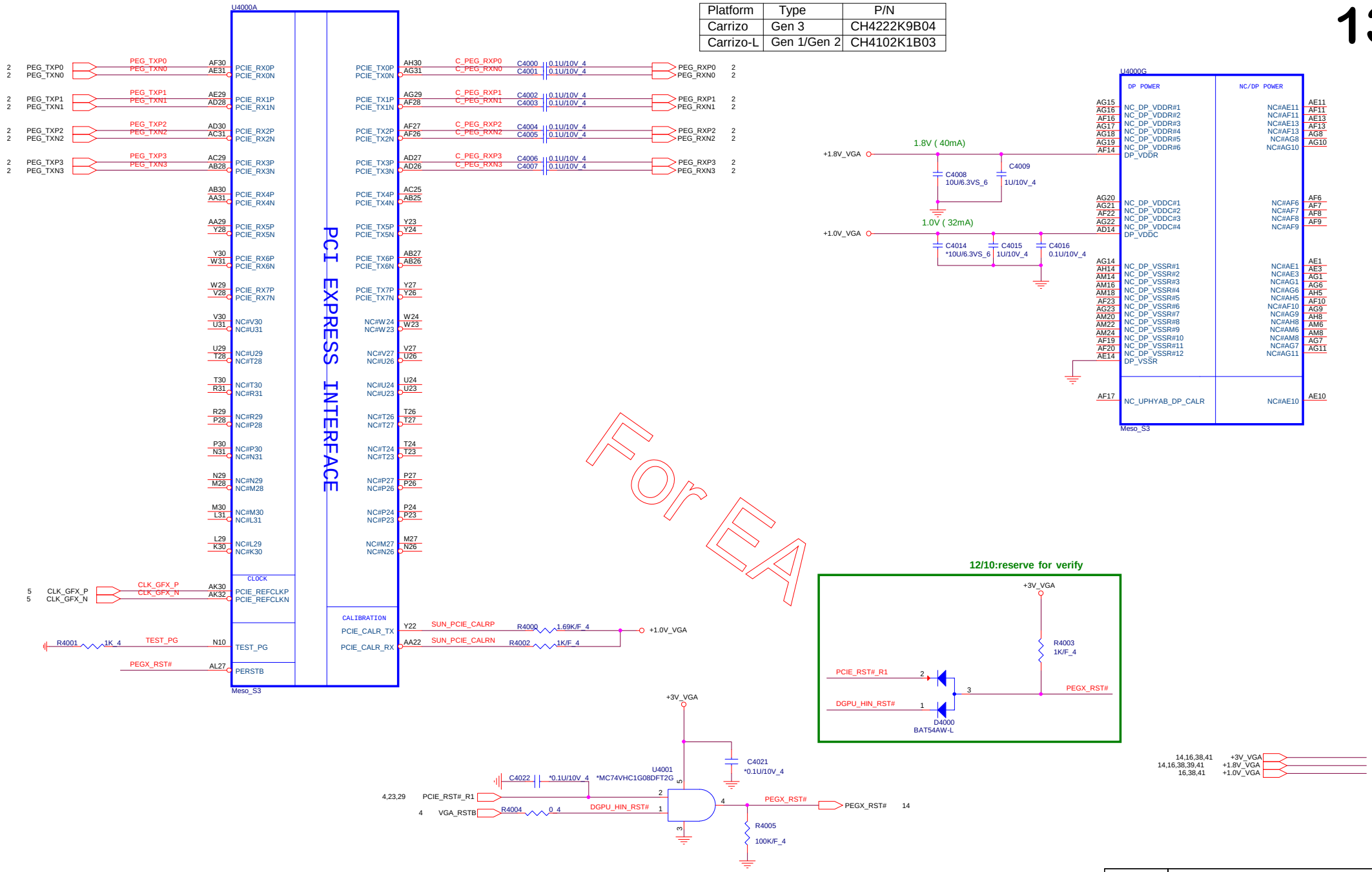
If use internal thermal IC, C600 use 0ohm.



PROJECT : Y2x
Quanta Computer Inc.

Size: Custom	Document Number: DDR3 DIMM1-STD (4.0H)	Rev: 1A
NB5/RD3	Date: Tuesday, November 18, 2014	Sheet 12 of 41

Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4102K1B03



PROJECT : X22
Quanta Computer Inc.

Size	Document Number	Rev
	MESO_S3 PCIE/DP power	1A

NB5/RD3
Tuesday, November 18, 2014
Sheet 13of 43

Thermal Solution(Close to GPU)

Main:AL000781039 G781-1P8(9Ah)

9/2: modify to +3V_VGA

10/2 : remove TP for no use

9/11: follow CRB change to 10K

9/4: change to 47K ohm for CRB

9/4: follow CRB design by FAE

10/1 : Gen 3 support or not
Carrizo : PU 8.45K ; PD 2K
Carrizo-L : PU NC ; PD 4.75K
Beema : PU NC ; PD 4.75K

MLPS Implementation
- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

BIT5 => BIT0

PS0 => 11001
PS1 => 11000
PS2 => 11000
PS3 => 11000

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 29).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	N/A	Reserved.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4]	N/A	Reserved.	1
PS_3[5]	N/A	Reserved.	1

AMD recommend

9/9: follow AMD CRB design

11/19: follow TXC Crystal vendor test report

9/11: Add for SR Tool review result
11/11: Change to unstuff by AMD confirm

Reserved. Do not connect on the PCB

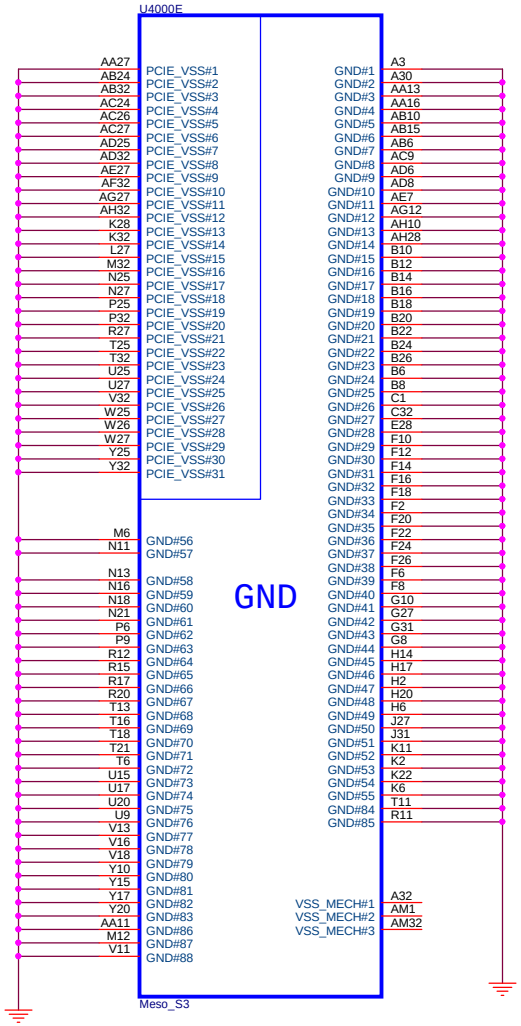
For AMD tuning timing purpose

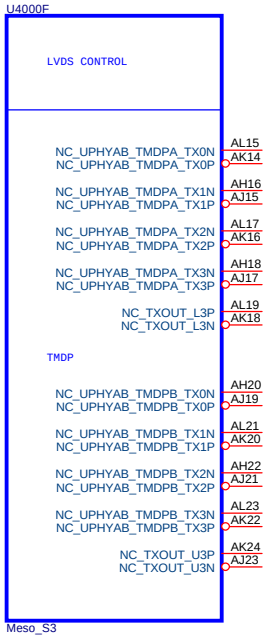
PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD
000	Hynix	256Mx16 *4, 900Mhz	H5TC4G63CFR-N0C	NC	4.75K
001	Samsung	256Mx16 *4, 900Mhz	K4W4G1646E-BC1A	8.45K	2K
010	Micron	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	4.53K	2K
011					
100					
101					

PROJECT : X22
Quanta Computer Inc.

NB5/RD3

Size	Document Number	Rev
	MESO_S3_Main	1A
Date: Wednesday, November 19, 2014	Sheet 14of 43	





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

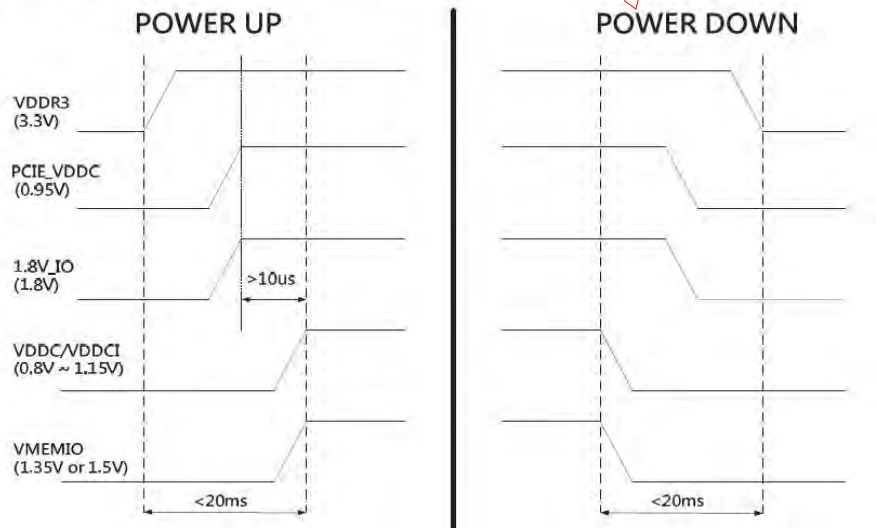
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

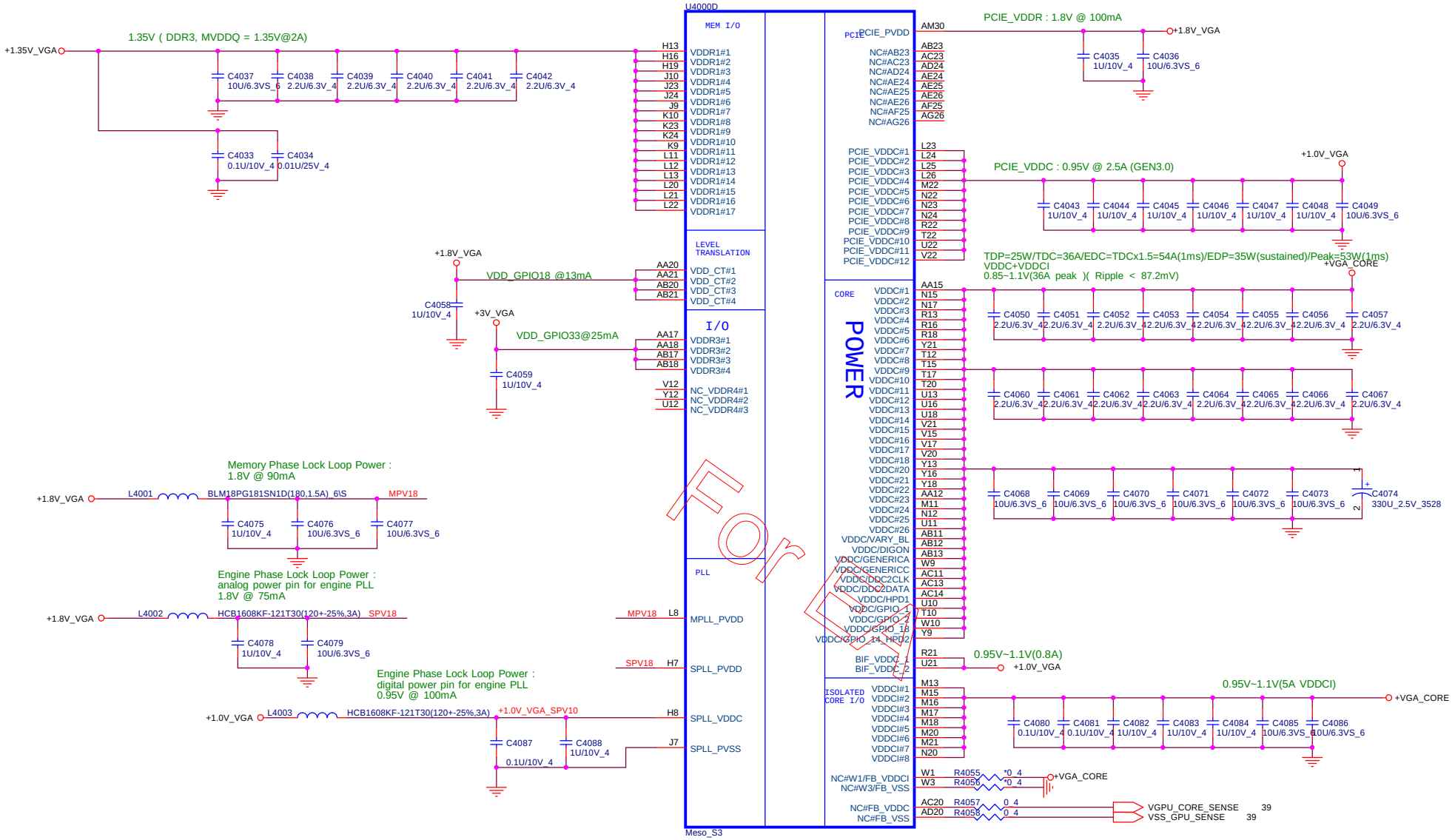


NB5/RD3

PROJECT : X22
Quanta Computer Inc.

Size	Document Number	Rev
	MESO_S3_GND/LVDS/Strap	1A

Date: Tuesday, November 18, 2014 Sheet 15 of 43

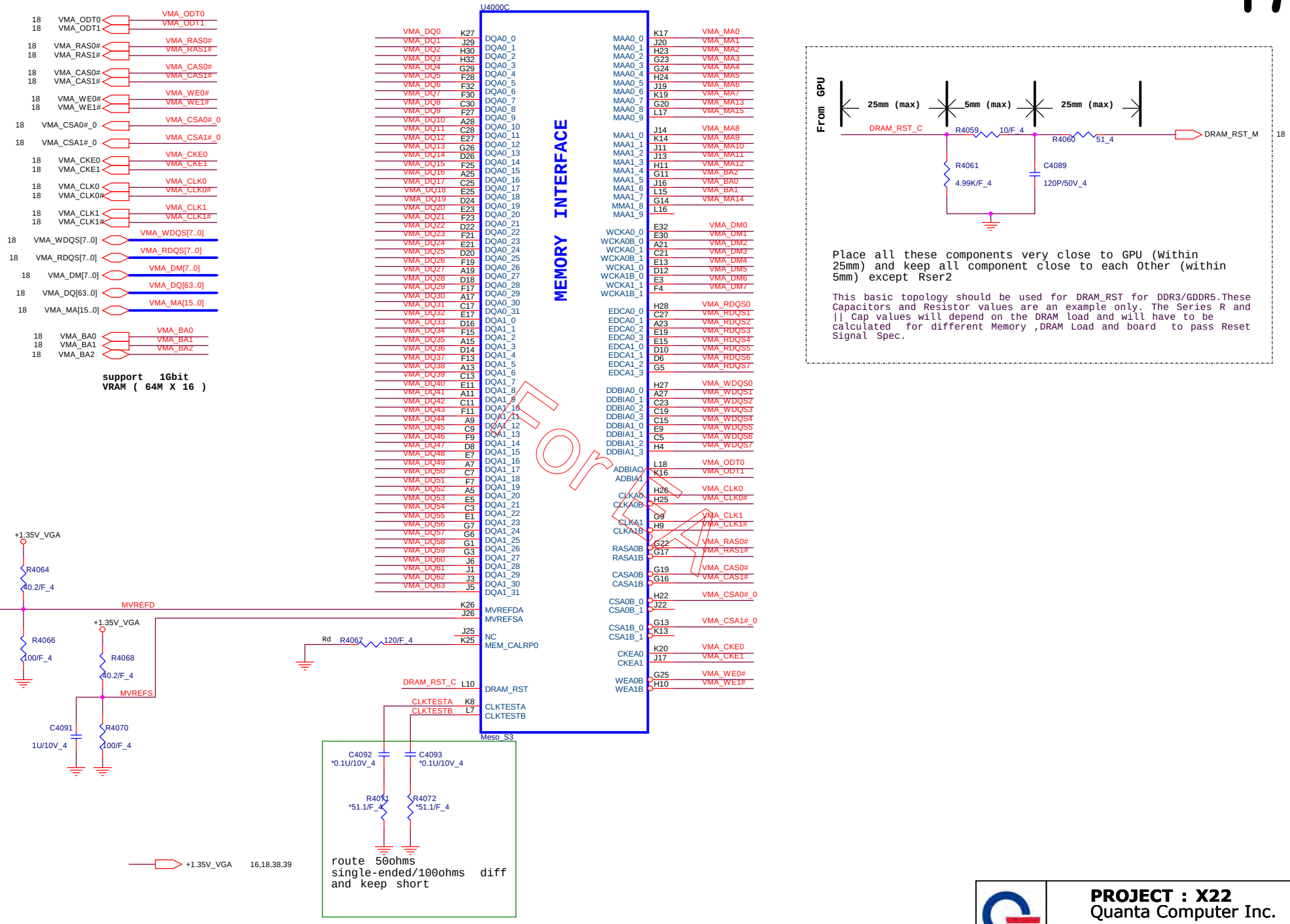


+1.35V_VGA 17,18,38,39
+1.8V_VGA 13,14,38,39,41
+1.0V_VGA 13,38,41
+VGA_CORE 38,39,40

NB5/RD3

PROJECT : X22
Quanta Computer Inc.

Size	Document Number	Rev
	MESO_S3 Power	1A
Date: Tuesday, November 18, 2014	Sheet 16 of 43	

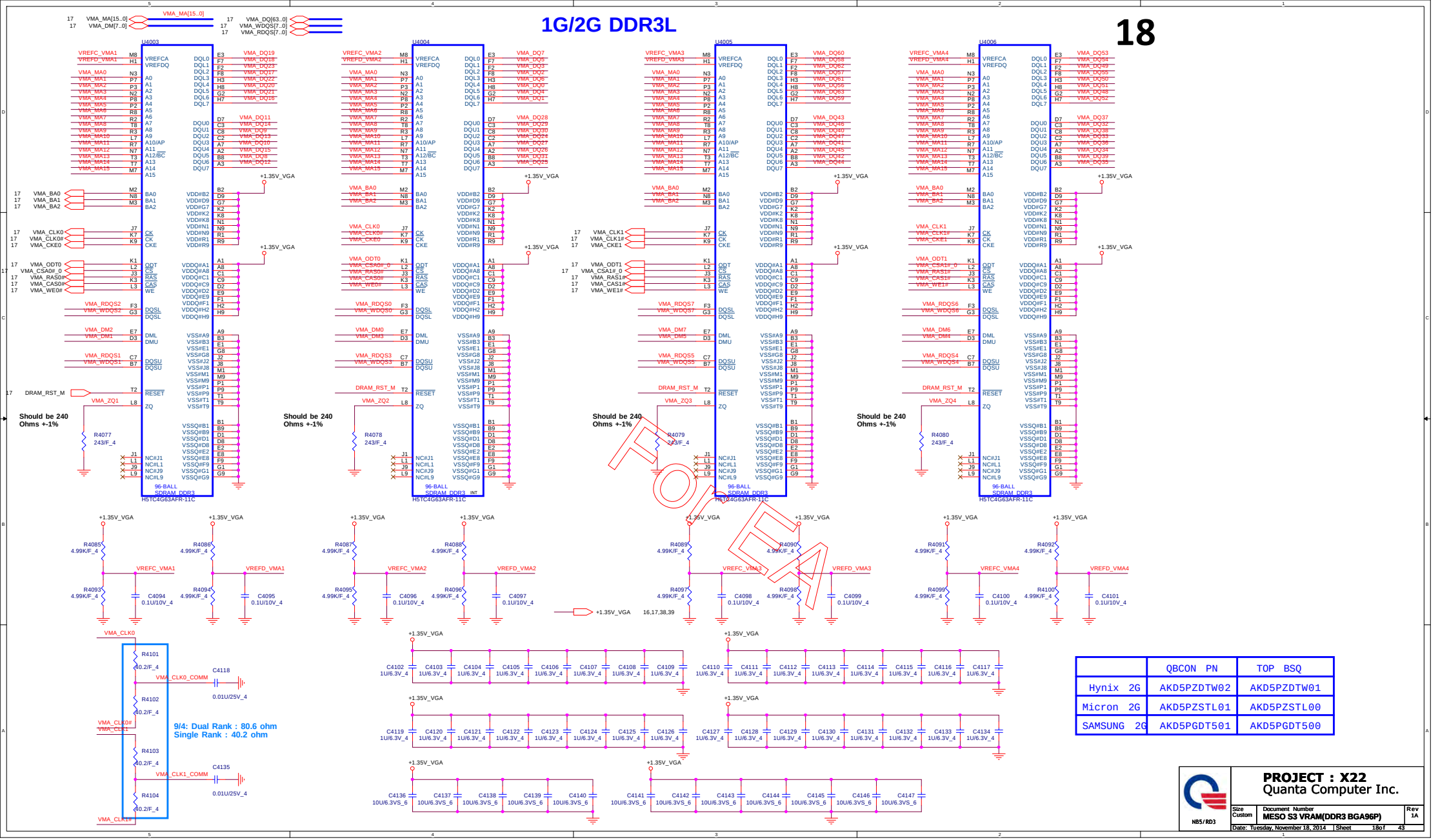


Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

NB5/RD3	PROJECT : X22 Quanta Computer Inc.	
Size	Document Number MESO_S3_MEM_Interface	Rev 1A
Date: Tuesday, November 18, 2014	Sheet 17 of 43	

1G/2G DDR3L



	QBCON PN	TOP BSQ
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01
Micron 2G	AKD5PZSTL01	AKD5PZSTL00
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500

PROJECT : X22
Quanta Computer Inc.

NB5/RD3

Size: Custom | Document Number: MESO S3 VRAM(DDR3 BGA96P) | Rev: 1A

Date: Tuesday, November 18, 2014 | Sheet 18 of 43

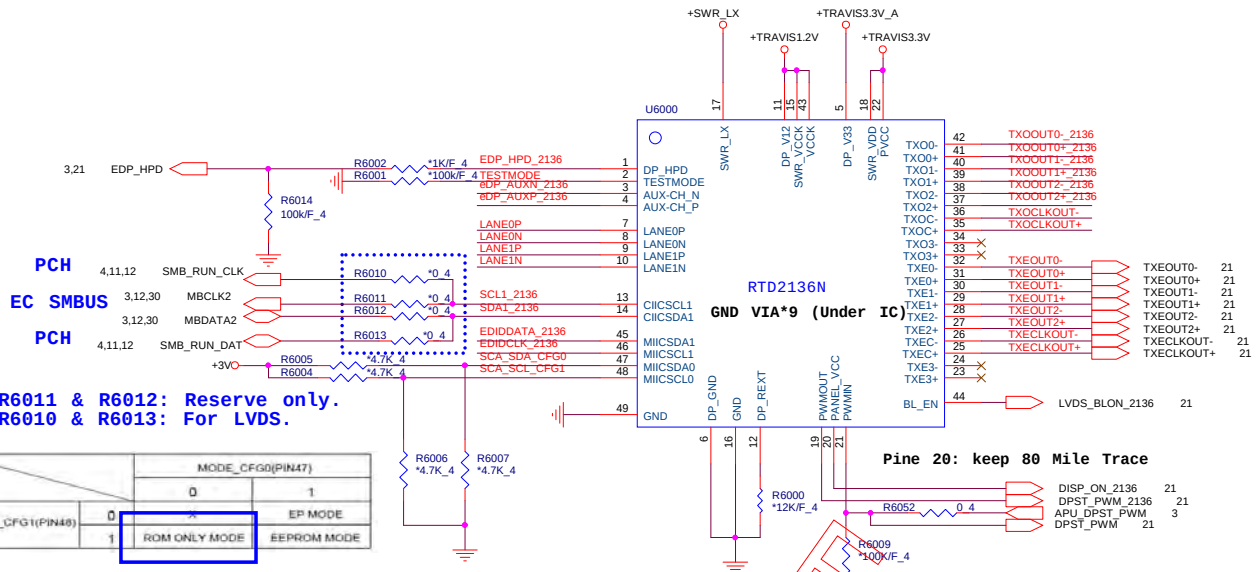
NB5/RD3

PROJECT : X22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MESO S3 VRAM(DDR3 BGA96P)	1A

Date: Tuesday, November 18, 2014 | Sheet 19of 43

Pine 15/17: keep 20 Mile Trace
Pine 18: keep 80 Mile Trace



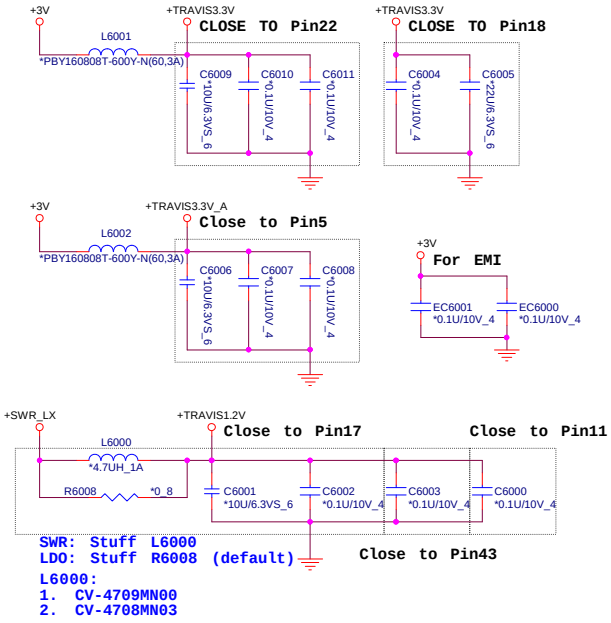
R6011 & R6012: Reserve only.
R6010 & R6013: For LVDS.

MODE_CFG0(PIN47)		
MODE_CFG1(PIN46)	0	1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

R6006 & R6005: Reserve only.
R6004 & R6007: For LVDS.

Pine 20: keep 80 Mile Trace

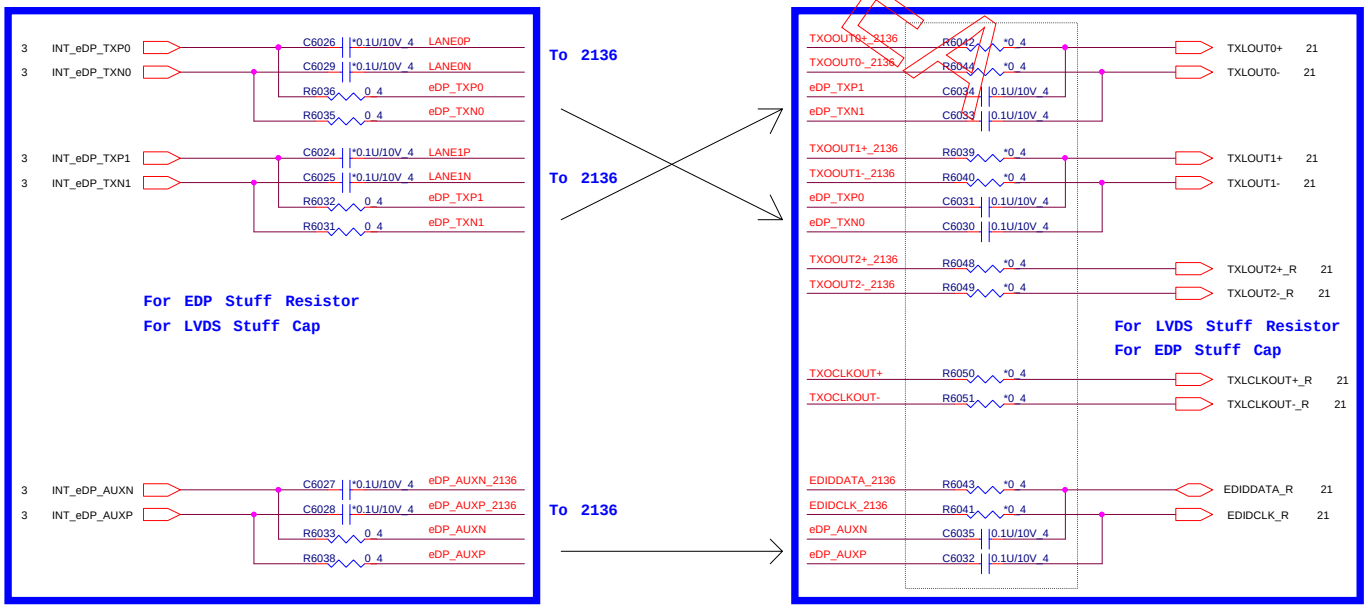
keep 80 Mile Trace



SWR: Stuff L6000
LDO: Stuff R6008 (default)

L6000:
1. CV-4709MN00
2. CV-4708MN03

Close to LVDS CONN



Note.
14" & 15" only eDP panel.
17" have both LVDS & eDP panel.

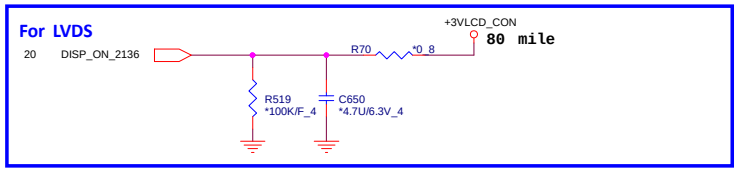
NB5/RD3

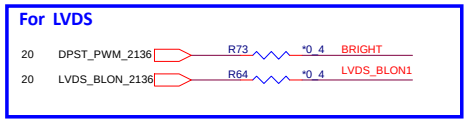
PROJECT : Y2x
Quanta Computer Inc.

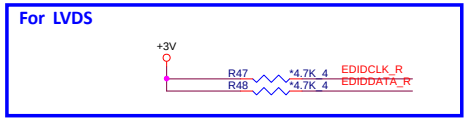
Size	Document Number	Rev
Custom	LVDS Converter RTD2136	1A
Date: Tuesday, November 18, 2014	Sheet 20 of 41	

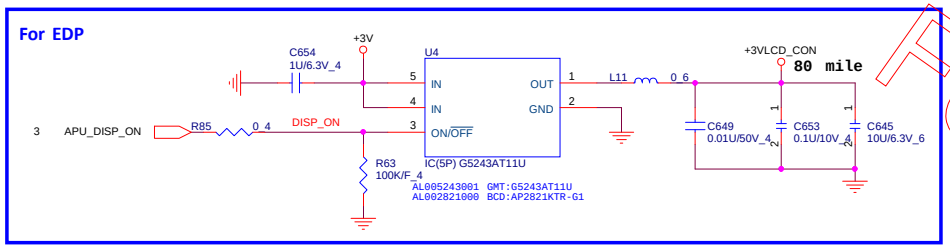
LVDS CONN.

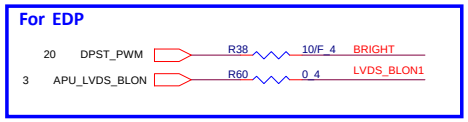
Note.
14" & 15" only eDP panel.
17" have both LVDS & eDP panel.

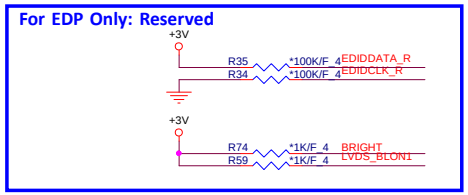






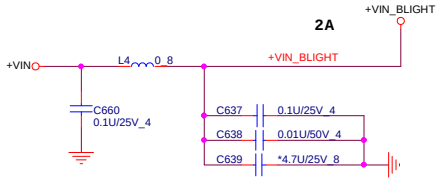


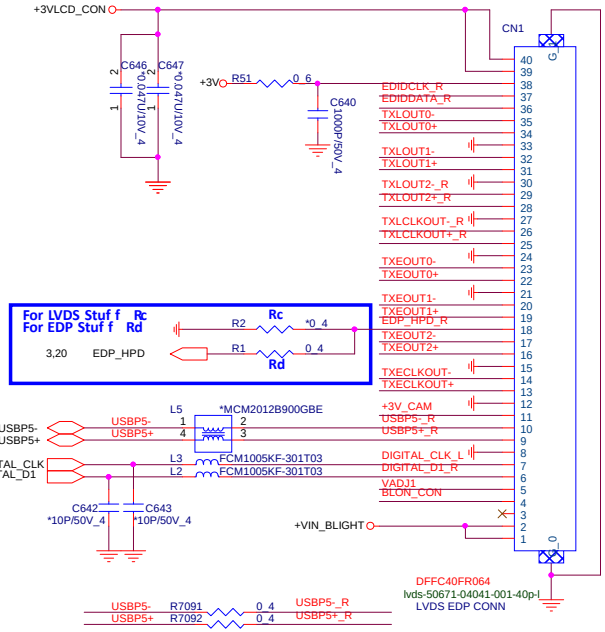


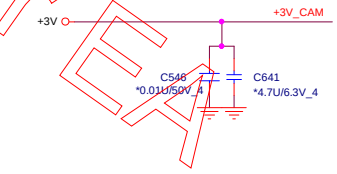


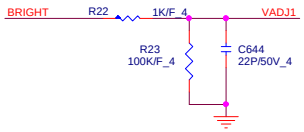
20 TXLOUT0+ TXLOUT0+
20 TXLOUT0- TXLOUT0-
20 TXLOUT1+ TXLOUT1+
20 TXLOUT1- TXLOUT1-
20 TXLOUT2+_R TXLOUT2+_R
20 TXLOUT2-_R TXLOUT2-_R
20 TXLCLKOUT+_R TXLCLKOUT+_R
20 TXLCLKOUT-_R TXLCLKOUT-_R
20 EDIDDATA_R EDIDDATA_R
20 EDIDCLK_R EDIDCLK_R

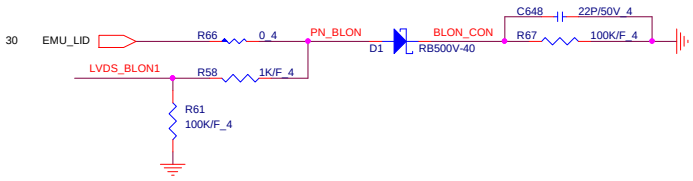
20 TXEOUT0+ TXEOUT0+
20 TXEOUT0- TXEOUT0-
20 TXEOUT1+ TXEOUT1+
20 TXEOUT1- TXEOUT1-
20 TXEOUT2+ TXEOUT2+
20 TXEOUT2- TXEOUT2-
20 TXECLKOUT+ TXECLKOUT+
20 TXECLKOUT- TXECLKOUT-

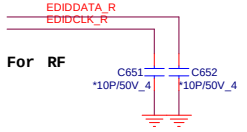






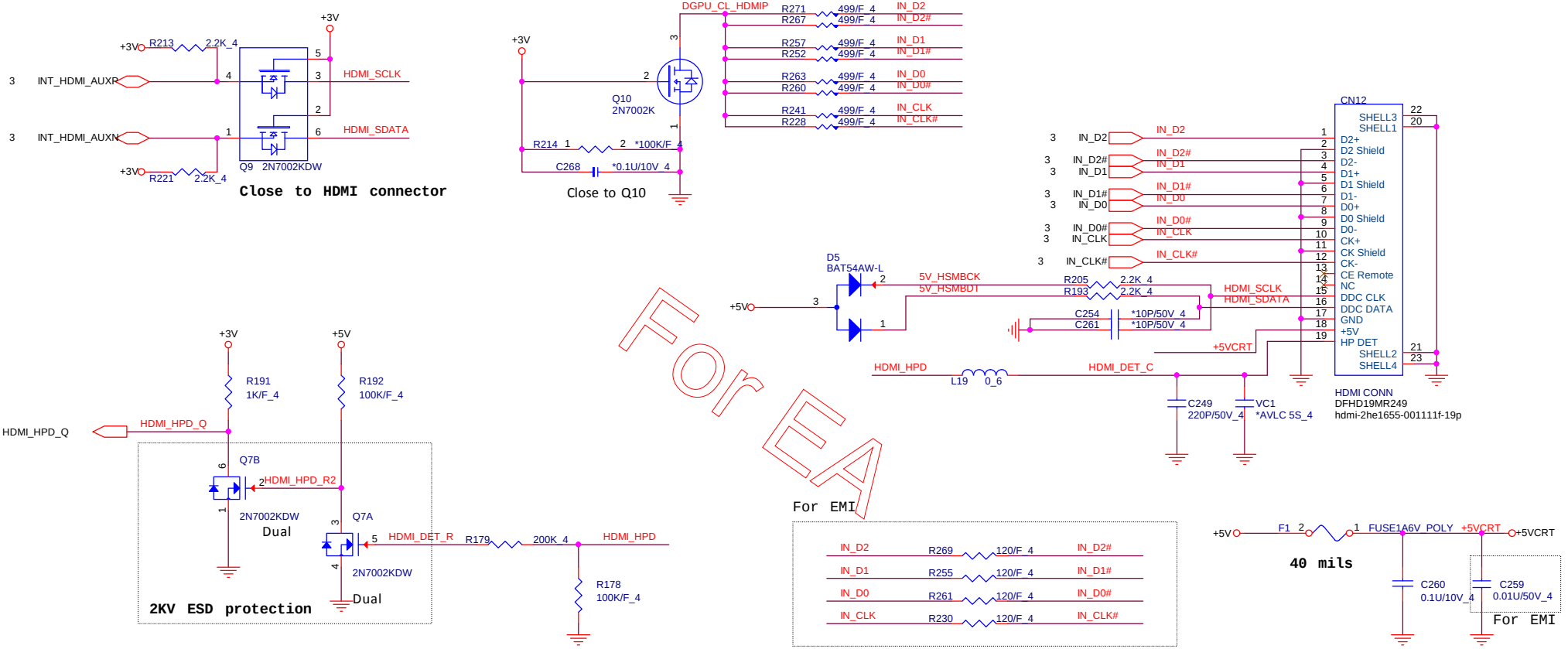




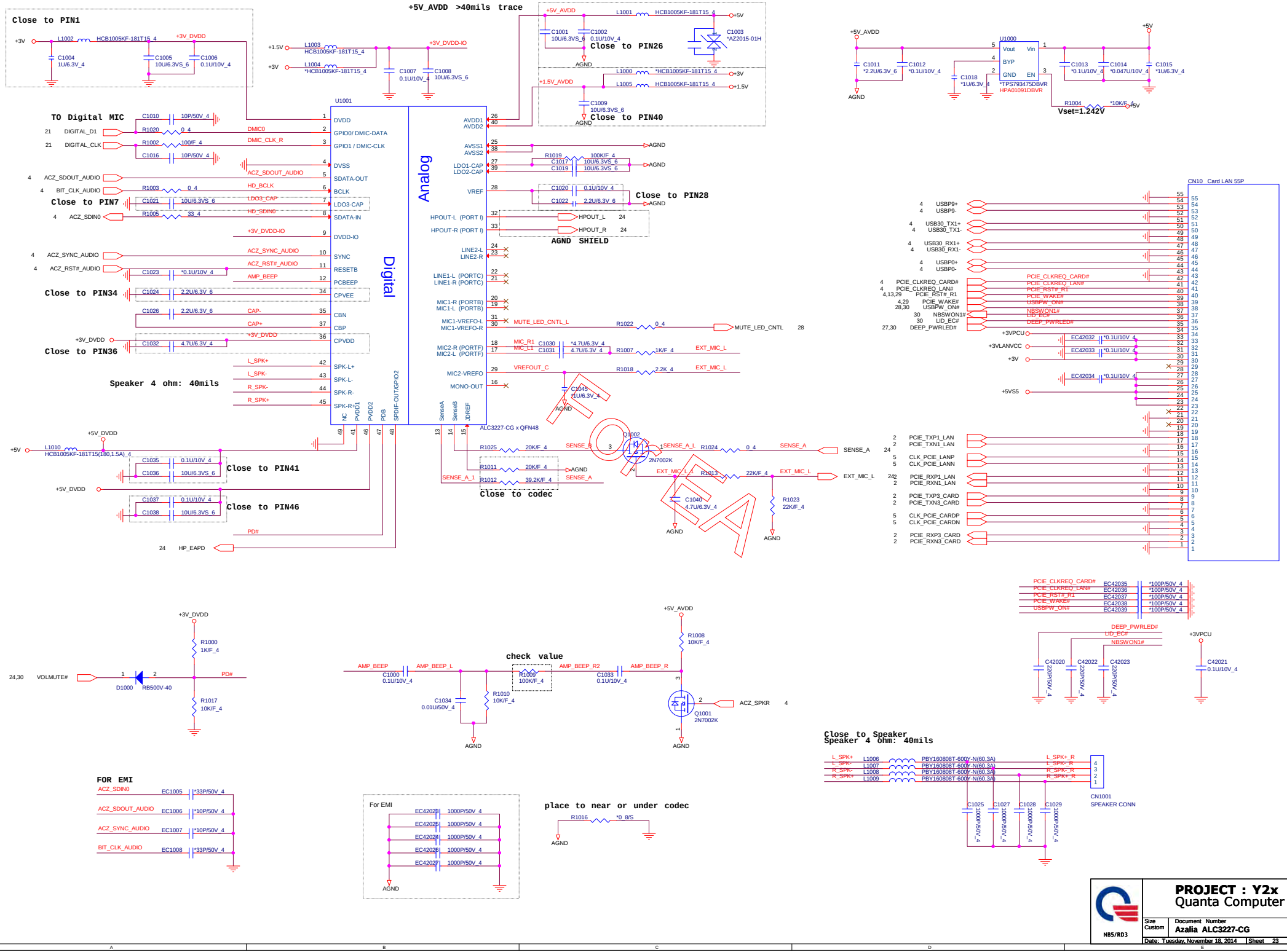


NB5/RD3	**PROJECT : Y2x** Quanta Computer Inc.	
Size Custom	Document Number LCD CONN/Camera/D-MIC	Rev 1A
Date: Tuesday, November 18, 2014	Sheet 21 of 41	

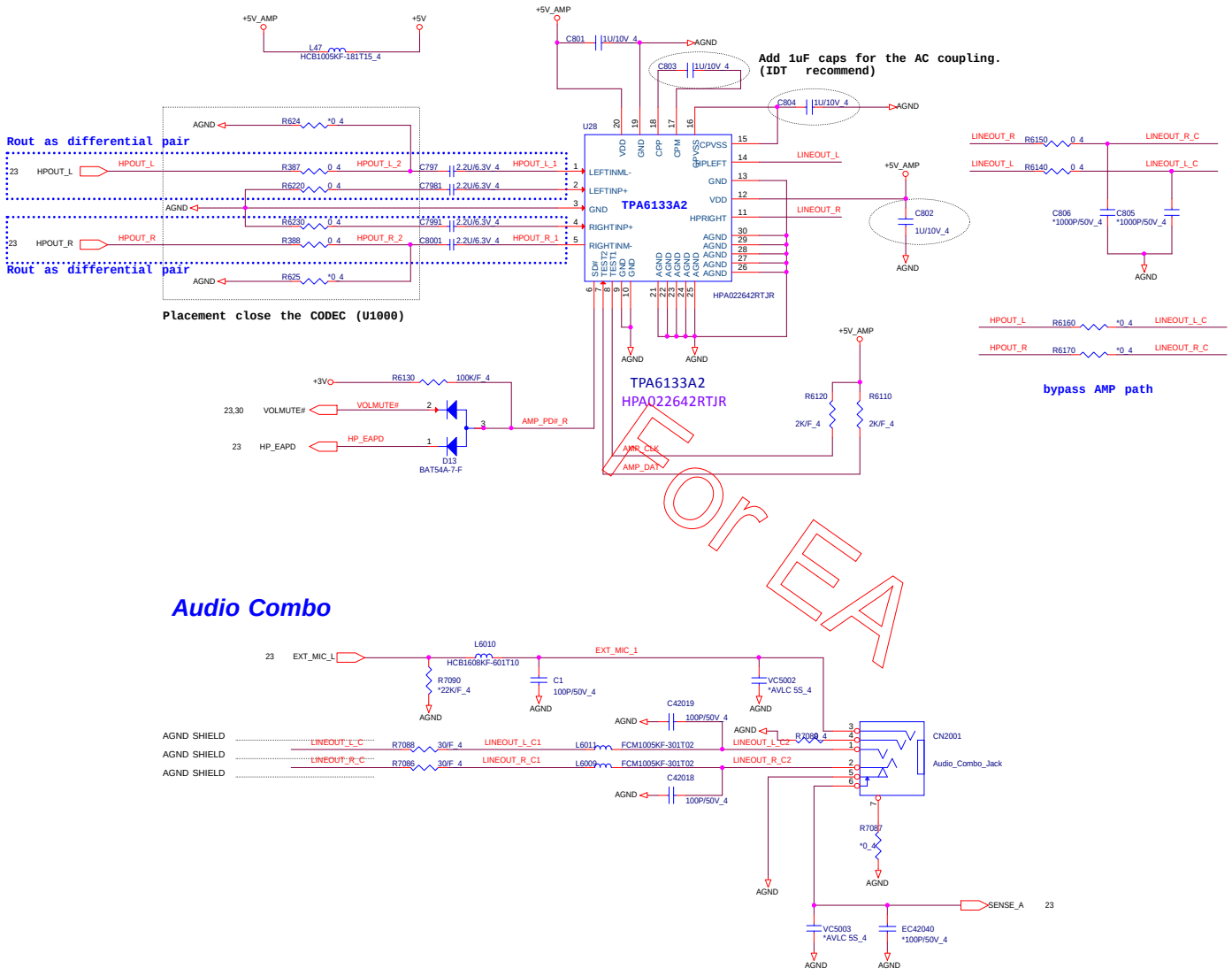
HDMI CONN



NB5/RD3	PROJECT : Y2x Quanta Computer Inc.	
	Size B Document Number HDMI	Rev 1A
	Date: Tuesday, November 18, 2014	Sheet 22 of 41


Close to PIN1
+5V_AVDD >40mils trace
Close to PIN26
Close to PIN40
Close to PIN28
AGND SHIELD
TO Digital MIC
Close to PIN7
Close to PIN34
Close to PIN36
Speaker 4 ohm: 40mils
Close to PIN41
Close to PIN46
Close to codec
Vset=1.242V
CN10 Card LAN 55P
check value
Close to Speaker
Speaker 4 ohm: 40mils
FOR EMI
For EMI
place to near or under codec
PROJECT : Y2x
Quanta Computer Inc.
Azalia ALC3227-CG
Date: Tuesday, November 18, 2014
Sheet 23 of 41

Head Phone out



Audio Combo

NB5	PROJECT : Y11C Quanta Computer Inc.	
Size C	Document Number HP AMP/Subwoofer	Rev 1A
Date: Tuesday, November 18, 2014	Sheet 24 of 41	

Holes

H1 *O-Y16X-4

H2 *H-TC236BC315D110P2

H4 *H-TC236BC276D118P2

H5 *H-TC236BC315D118P2

H6 *H-TC236BC315D118P2

H7 *H-TC315BC276D157P2

H12 *H-C315D157P2

H13 *H-TC236BC315D110P2

H16 *H-C98D98NP

GPU HOLEs

H14 *H-TC294BC197D146P2

H15 *H-TC294BC197D146P2

WLAN NUT

H3 H-TC197BC102D102P2

APU HOLEs

H8 *H-TC216BC197D146P2

H9 *H-TC216BC197D146P2

H10 *H-TC216BC197D146P2

H11 *H-TC216BC197D146P2

Metal ESD

PAD4 *SPAD-RE315X158

R337 *0_6

C634 *Clamp-Diode

EMI

PAD5 *SPAD-Y23X-1

PAD6 *O-Y16X-3

PAD7 *SPAD-Y23X-1

PAD8 *SPAD-Y23X-1

For EA

Place on +VIN path

+VIN — C42031 0.1U/25V_4 — C42032 0.1U/25V_4 — C42033 0.1U/25V_4 — C42034 0.1U/25V_4 — C42035 0.1U/25V_4 — C42036 0.1U/25V_4 — C42037 0.1U/25V_4 — C42038 0.1U/25V_4 — C42039 0.1U/25V_4 — C42040 0.1U/25V_4

+VIN — C42041 0.1U/25V_4 — C42042 0.1U/25V_4 — C42043 0.1U/25V_4 — C42044 0.1U/25V_4 — C42045 0.1U/25V_4 — C42046 0.1U/25V_4 — C42047 0.1U/25V_4 — C42048 0.1U/25V_4 — C42049 0.1U/25V_4 — C42050 0.1U/25V_4

+1.35VSUS — C42051 180P/50V_4

11/17 EMI request

NB5/RD3

PROJECT : Y2x
Quanta Computer Inc.

Size	Document Number	Rev
B	Holes / EMI	1A

Date: Tuesday, November 18, 2014 Sheet 25 of 41

NB5/RD3

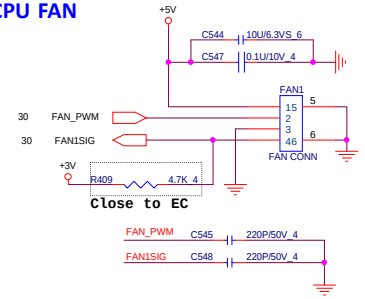
PROJECT : Y2x
Quanta Computer Inc.

Size	Document Number	Rev
B	**Reserved**	1A

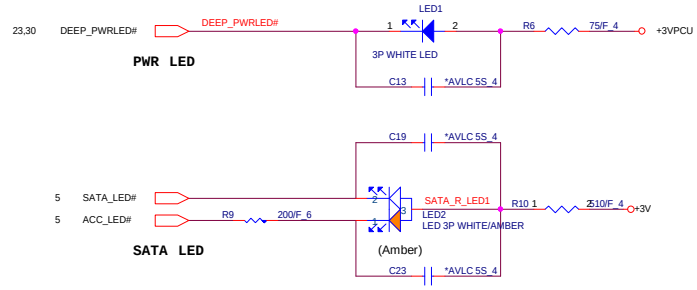
Date: Tuesday, November 18, 2014 | Sheet 26of 41

Power But t on Connect or (Mov et o DB)

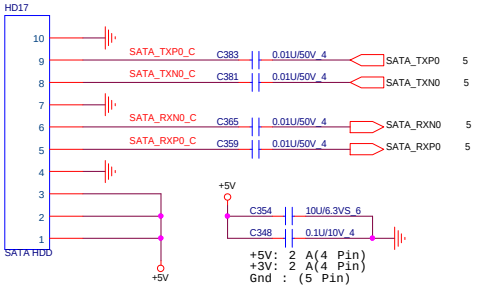
CPU FAN



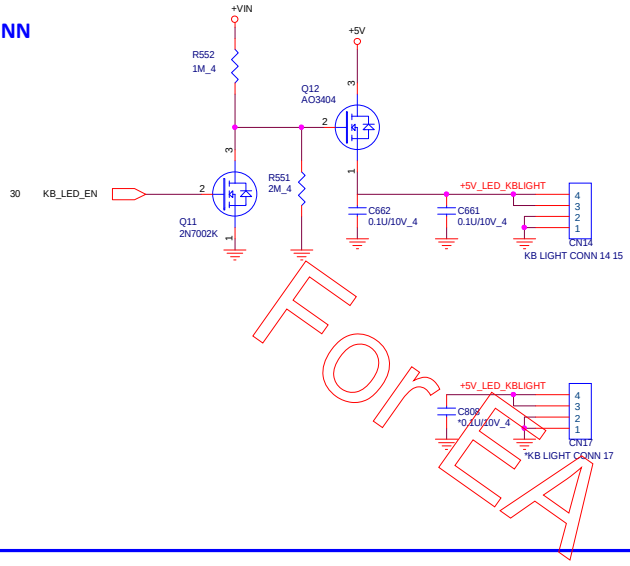
LED



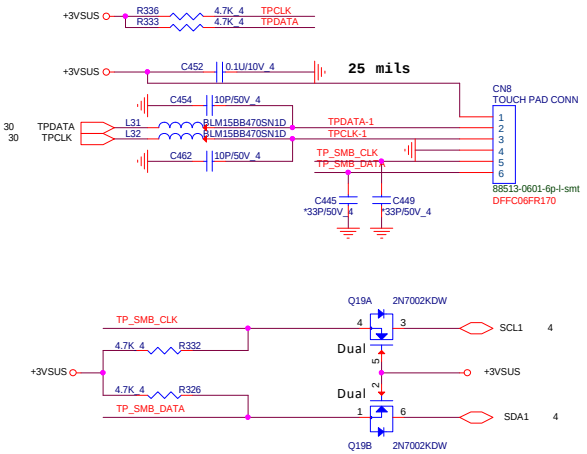
SATA HDD CONN (Cable type)



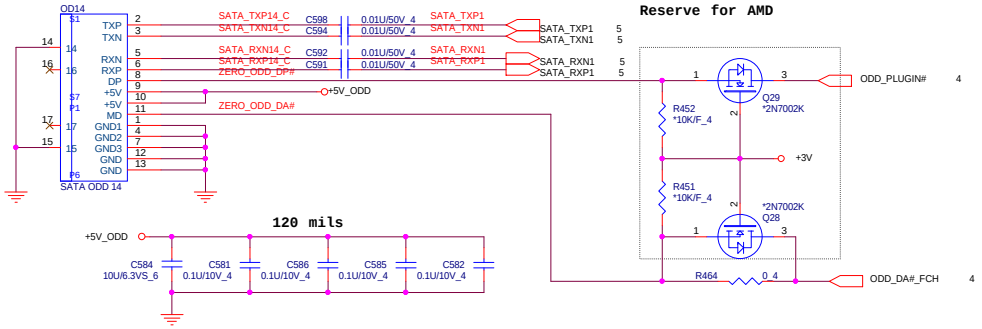
KB LIGHT CONN



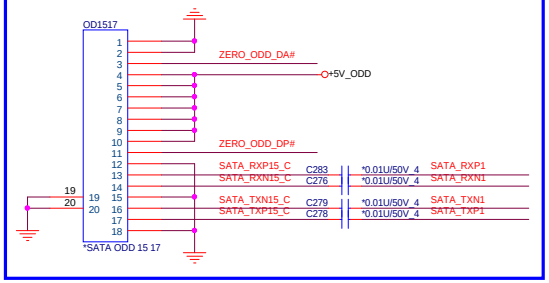
Touch Pad

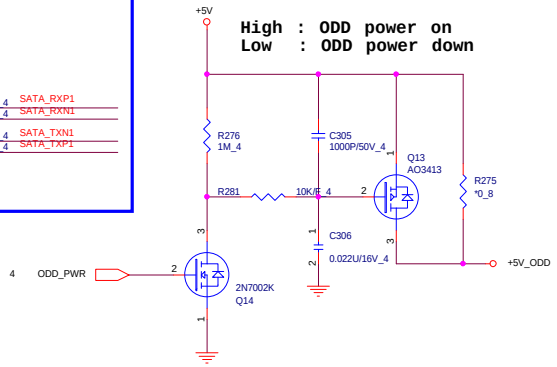


14" SATA ODD CONN



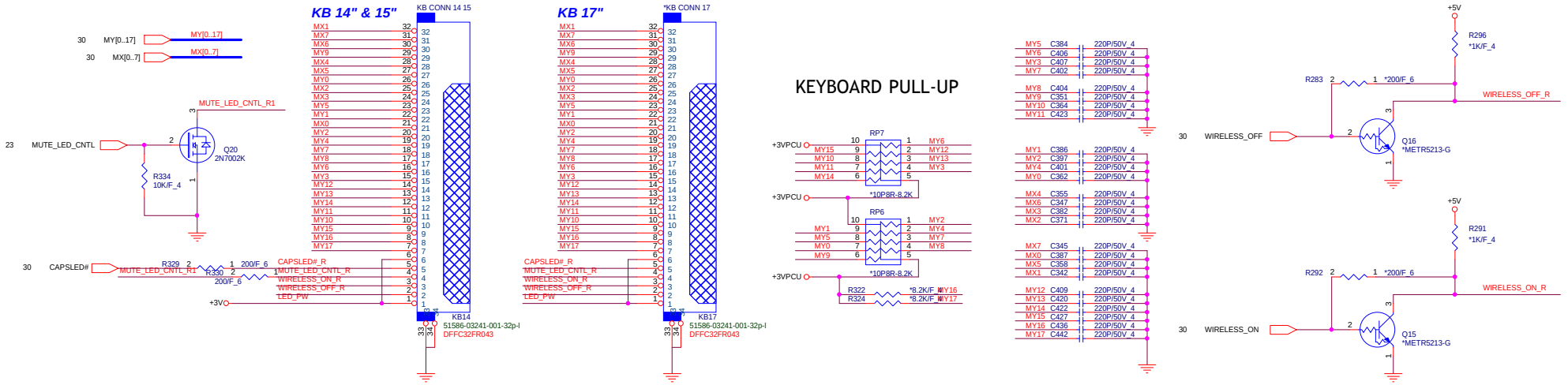
15" & 17" SATA ODD CONN



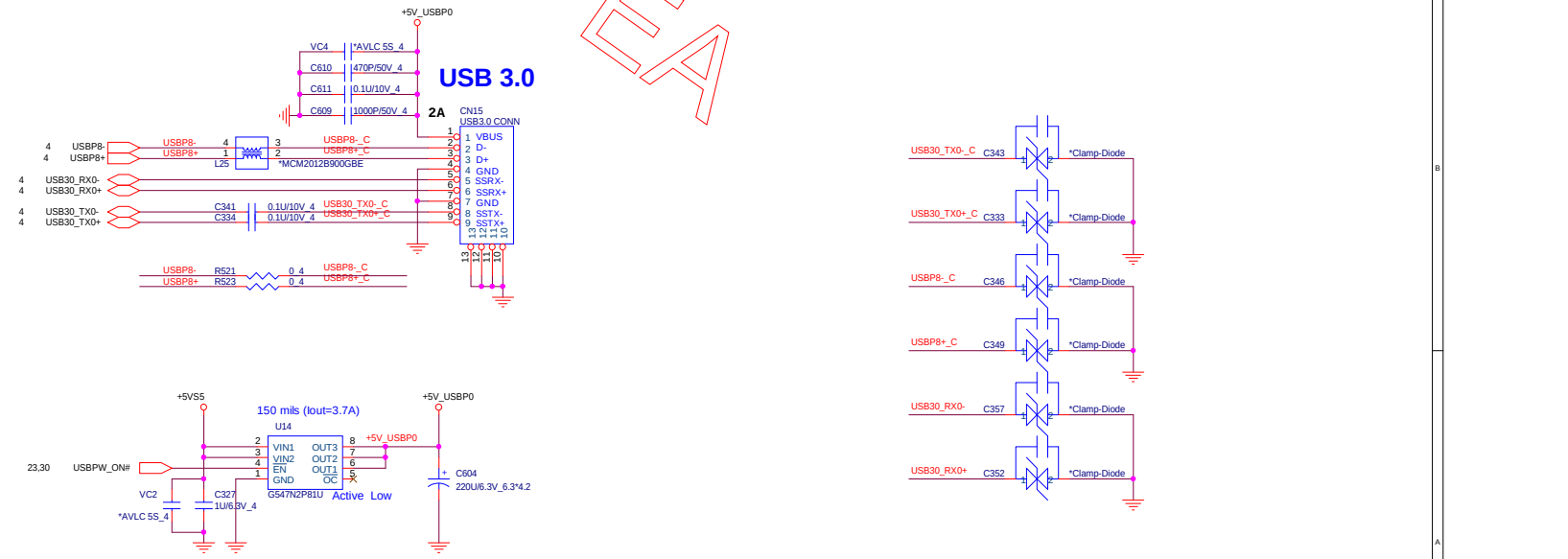


NB5/RD3	PROJECT : Y2x Quanta Computer Inc.	
Size: Custom	Document Number: HDD/ODD/TP/FAN/LID/LED	Rev: 1A
Date: Tuesday, November 18, 2014	Sheet 27 of 41	

KEYBOARD CONN.

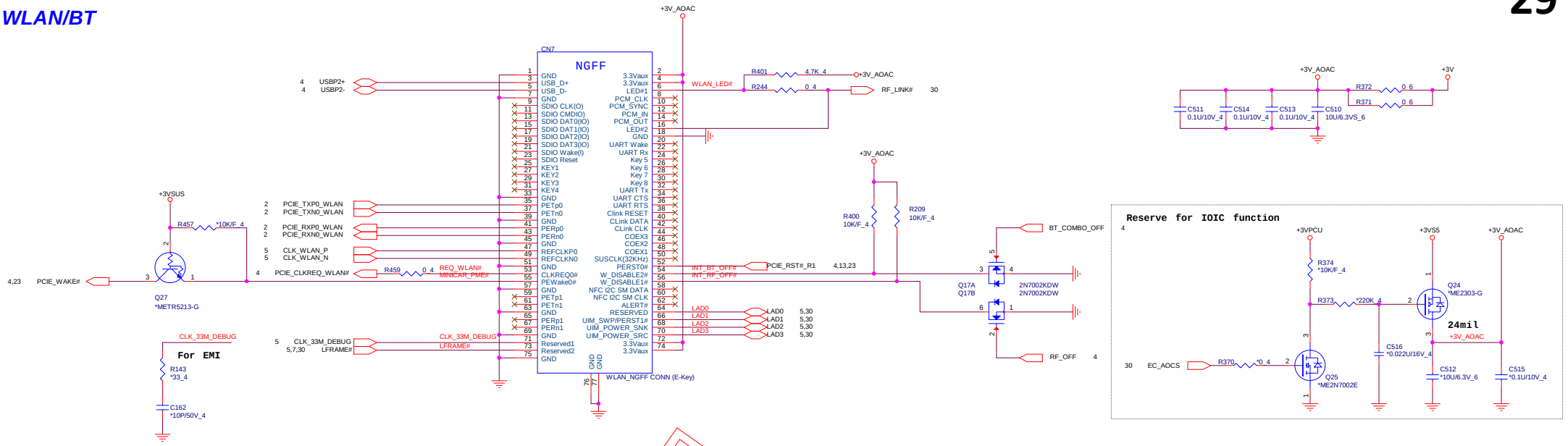


Left USB 2.0/3.0 Combo

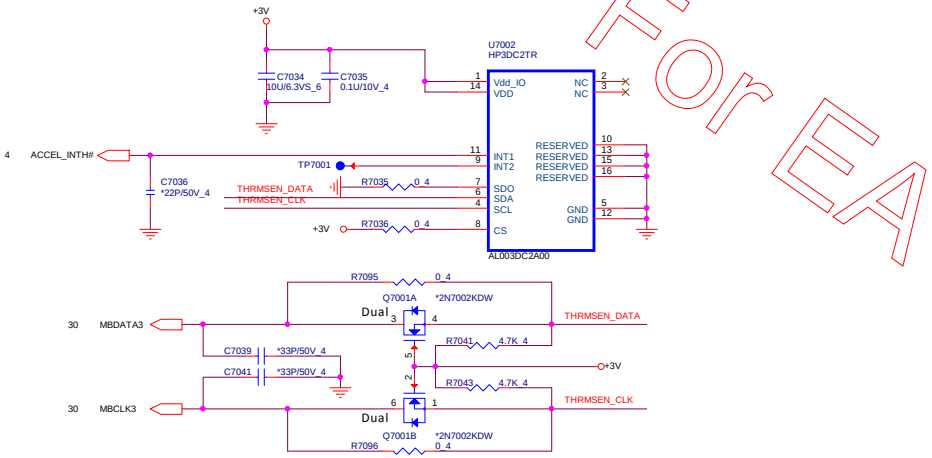


Quanta Computer Inc.	PROJECT : Y2x		
NB5/RD3	Size: Custom	Document Number: USB3.0/KB	Rev: 1A
	Date: Tuesday, November 18, 2014	Sheet 28 of 41	

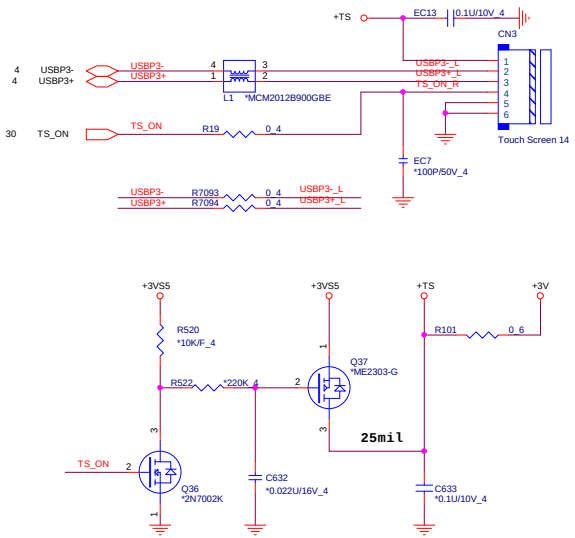
WLAN/BT



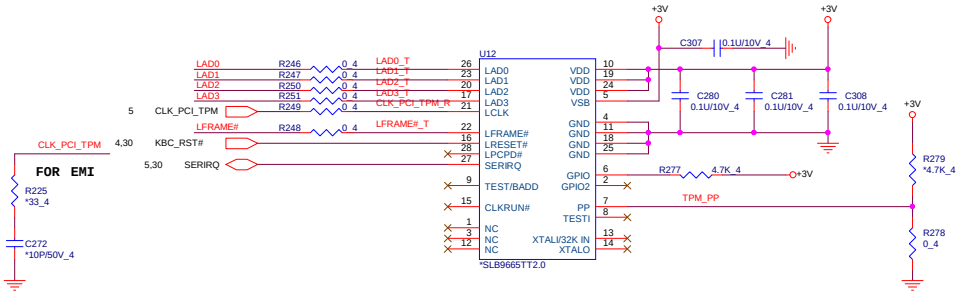
Accelerometer Sensor



Touch screen

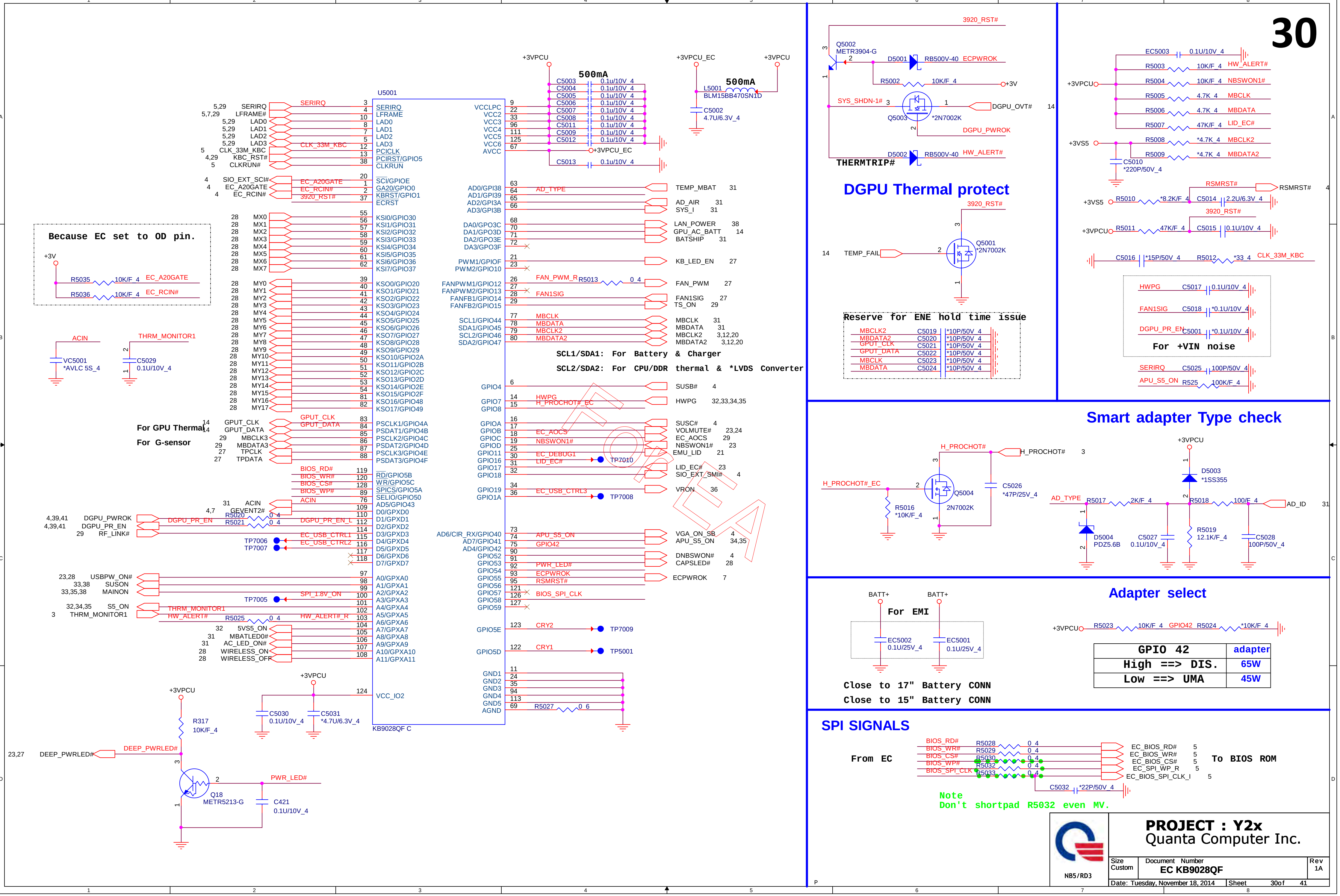


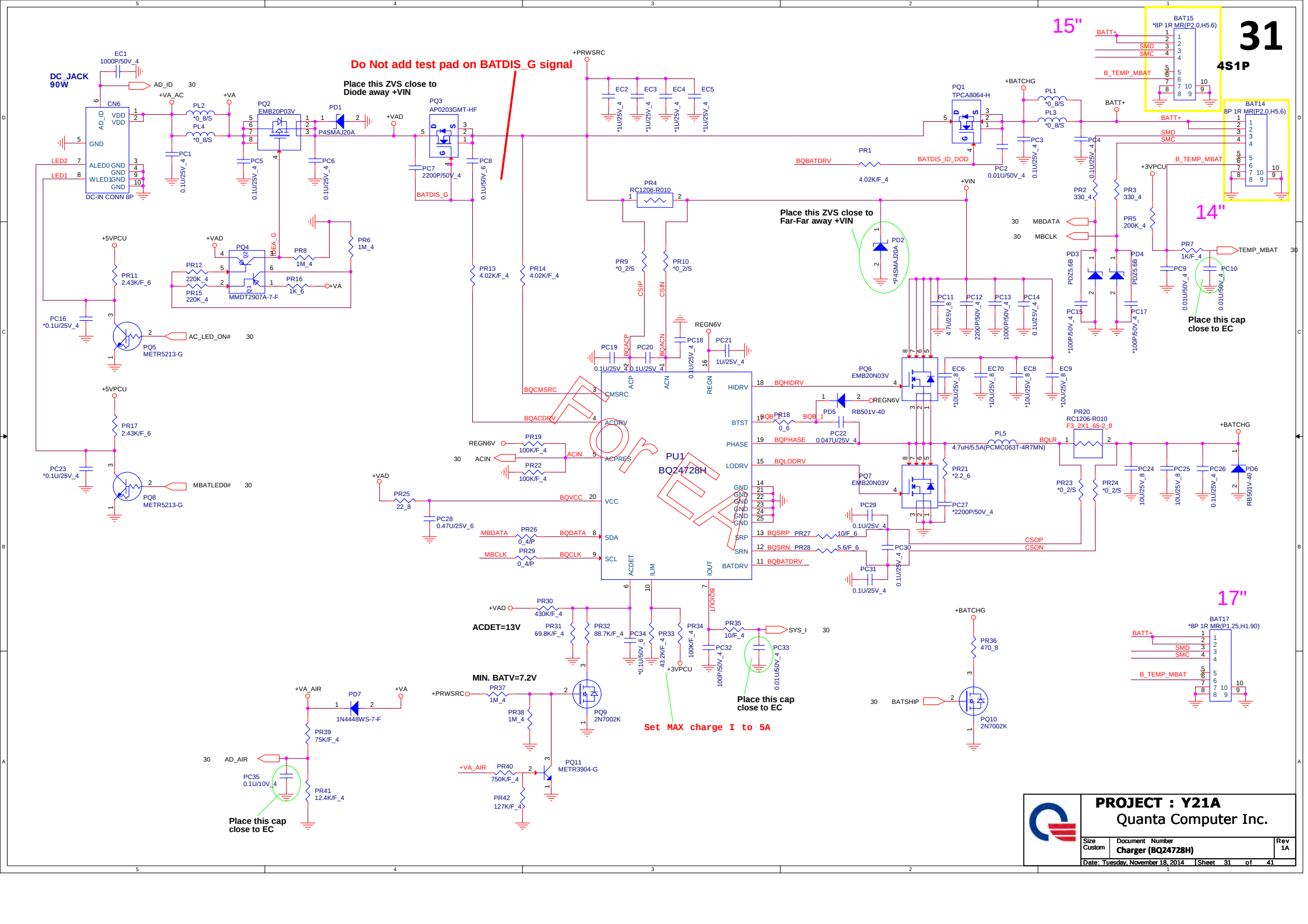
TPM (2.0)



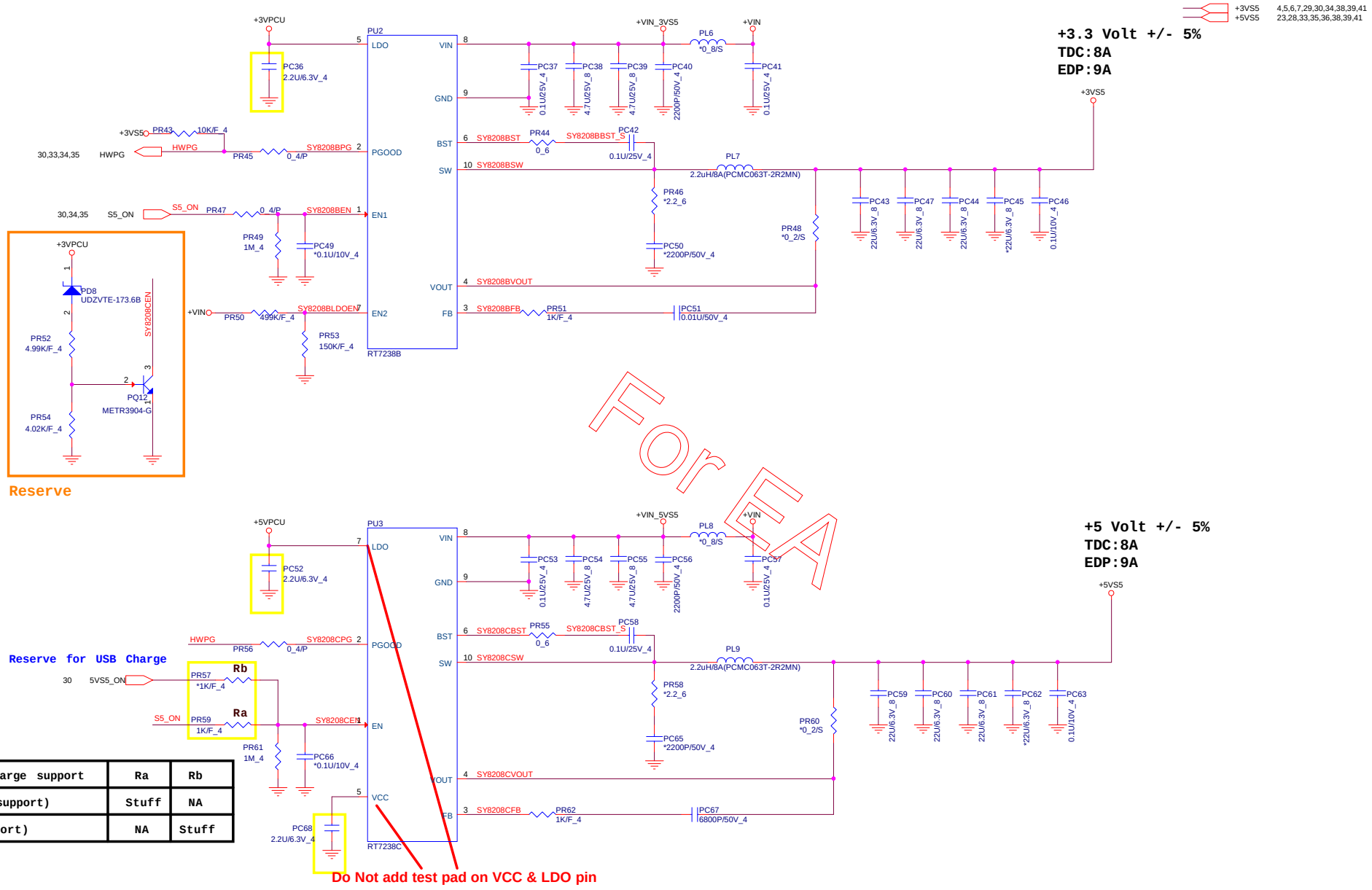
PROJECT : Y2x	
Quanta Computer Inc.	
Size: Custom	Document Number: WLAN/G Sensor/TPM/TS
Rev: 1A	
Date: Tuesday, November 18, 2014	Sheet 29 of 41

NB5/RD3


30
U5001
KB9028QF C
Because EC set to OD pin.
For GPU Thermal
For G-sensor
500mA
SCL1/SDA1: For Battery & Charger
SCL2/SDA2: For CPU/DDR thermal & *LVDS Converter
DGPU Thermal protect
THERMTRIP#
Reserve for ENE hold time issue
For +VIN noise
Smart adapter Type check
Adapter select
For EMI
Close to 17" Battery CONN
Close to 15" Battery CONN
GPIO 42 | adapter
High ==> DIS. | 65W
Low ==> UMA | 45W
SPI SIGNALS
From EC
To BIOS ROM
Note
Don't shortpad R5032 even MV.
NB5/RD3
PROJECT : Y2x
Quanta Computer Inc.
Size Custom
Document Number EC KB9028QF
Rev 1A
Date: Tuesday, November 18, 2014
Sheet 30 of 41


15"
31
4S1P
Do Not add test pad on BATDIS_G signal
Place this ZVS close to Diode away +VIN
Place this ZVS close to Far-Far away +VIN
Place this cap close to EC
14"
17"
DC_JACK 90W
DC-IN CONN 8P
PU1 BQ24728H
ACDET=13V
MIN. BATV=7.2V
Set MAX charge I to 5A
PROJECT : Y21A
Quanta Computer Inc.
Charger (BQ24728H)
Date: Tuesday, November 18, 2014
Sheet 31 of 41

DC/DC +3VS5/+5VS5

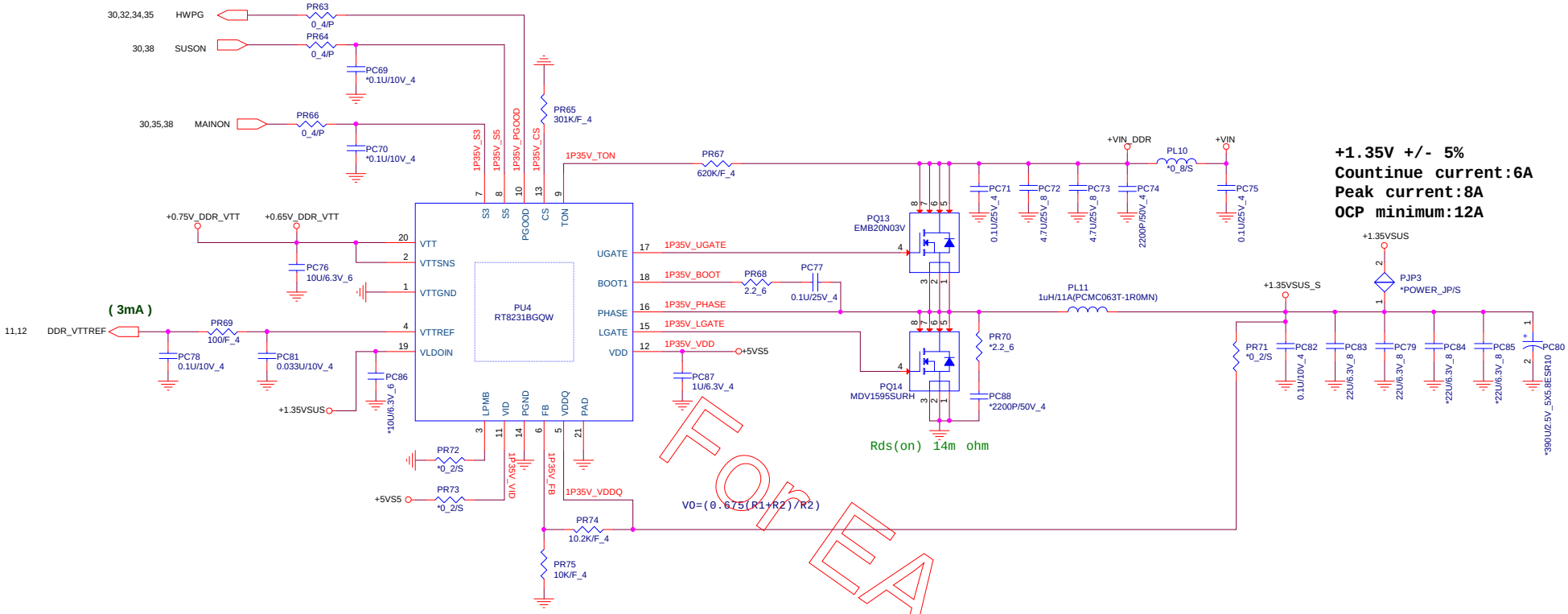


USB Charge support	Ra	Rb
(No support)	Stuff	NA
(Support)	NA	Stuff

PROJECT : Y21A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VPCU(SY8208B/SY8208C)	1A

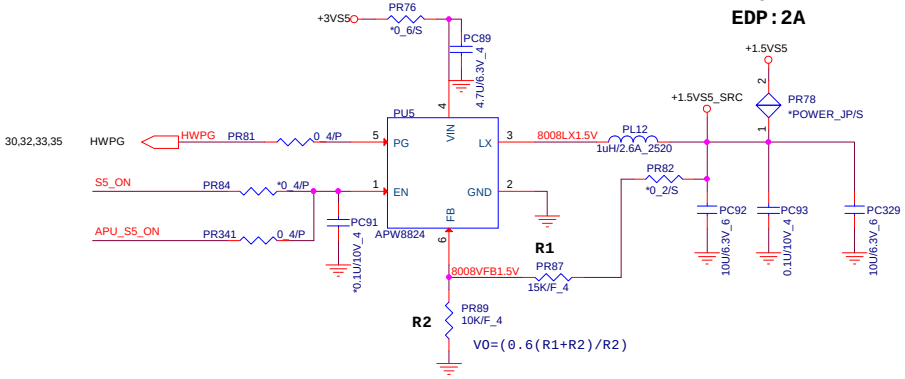
Date: Tuesday, November 18, 2014 Sheet 32 of 41



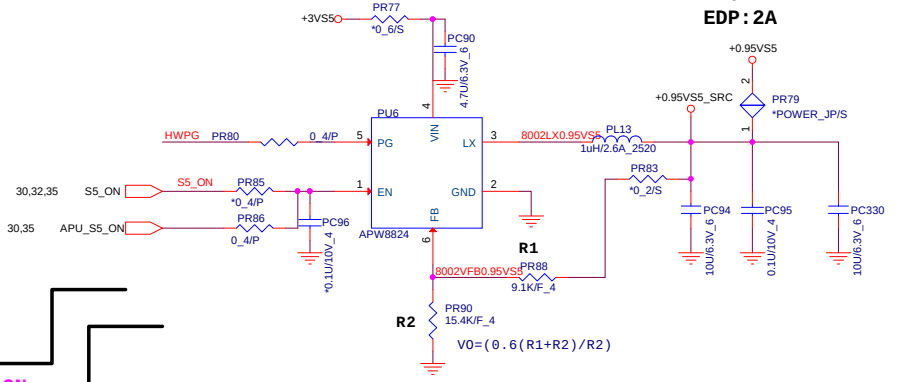
PROJECT : Y12A-BTM
Quanta Computer Inc.

Document Number	Rev
DDR3 (RT8231B)/1.8VS5	1A
Date: Tuesday, November 18, 2014	Sheet 33 of 41

+1.5V +/- 5%
TDC:1A
EDP:2A



+0.95VS5 +/- 5%
TDC:1A
EDP:2A



S5_ON

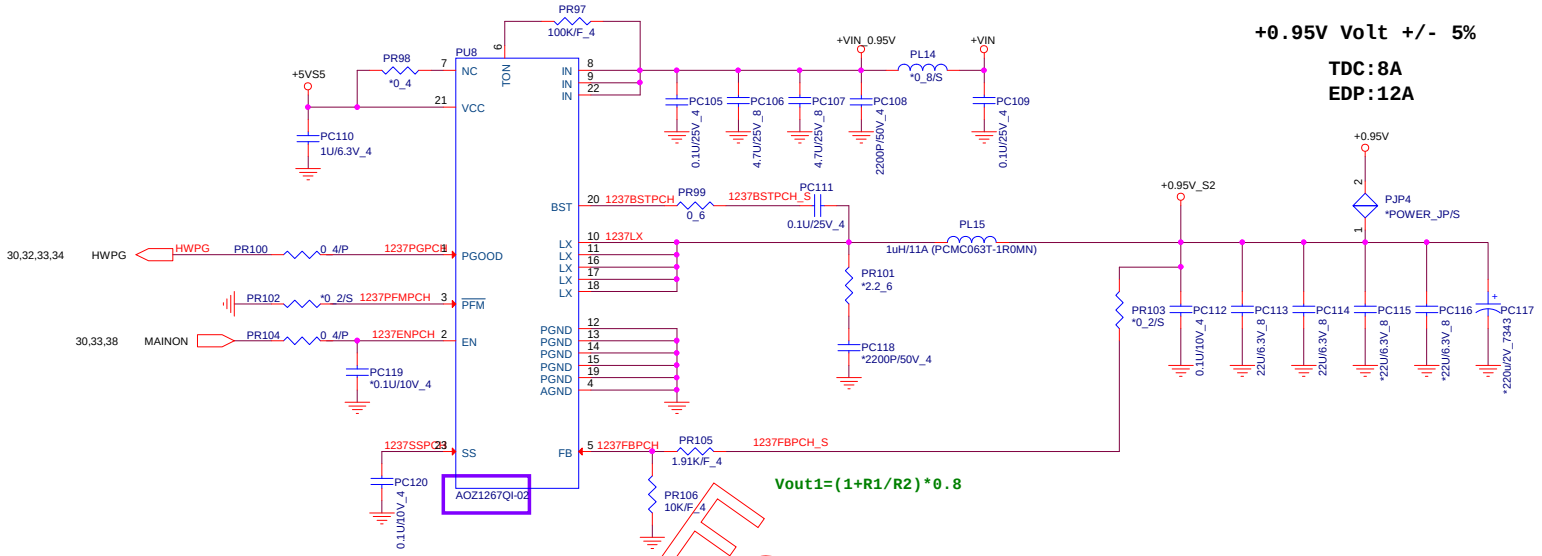
APU_S5_ON

	PROJECT : Y21A Quanta Computer Inc.	
Size Custom	Document Number **+1.1VS5 (RT8228)/2.5V**	Rev 1A
Date: Tuesday, November 18, 2014	Sheet 34 of 41	

+0.95V Volt +/- 5%

TDC:8A

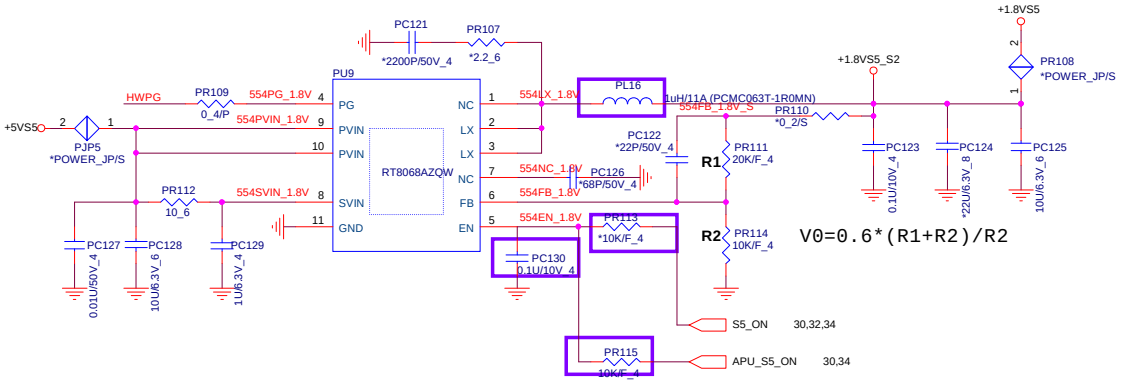
EDP:12A



1.8VS5 +/- 3%

TDC:3A

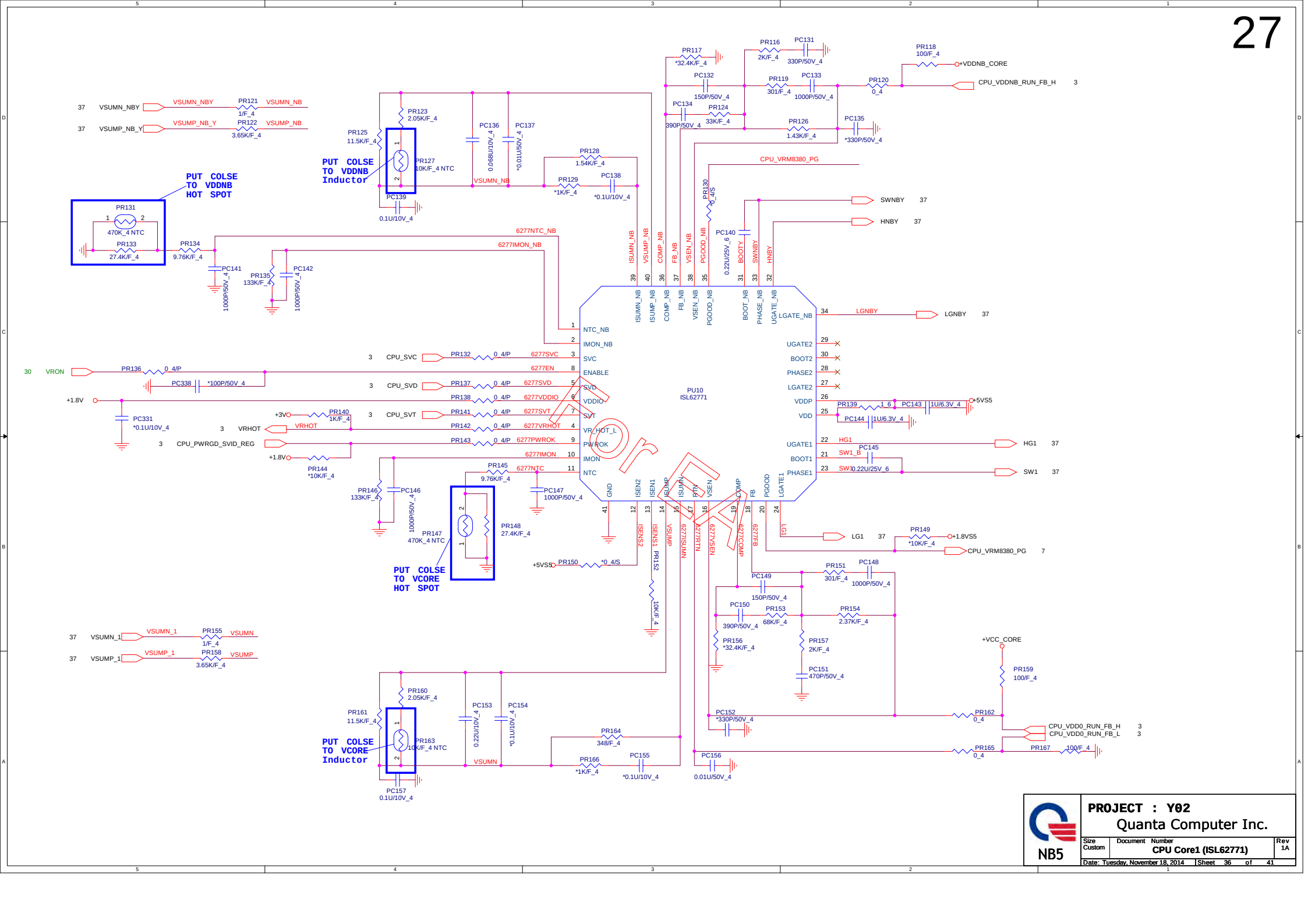
EDP:4A



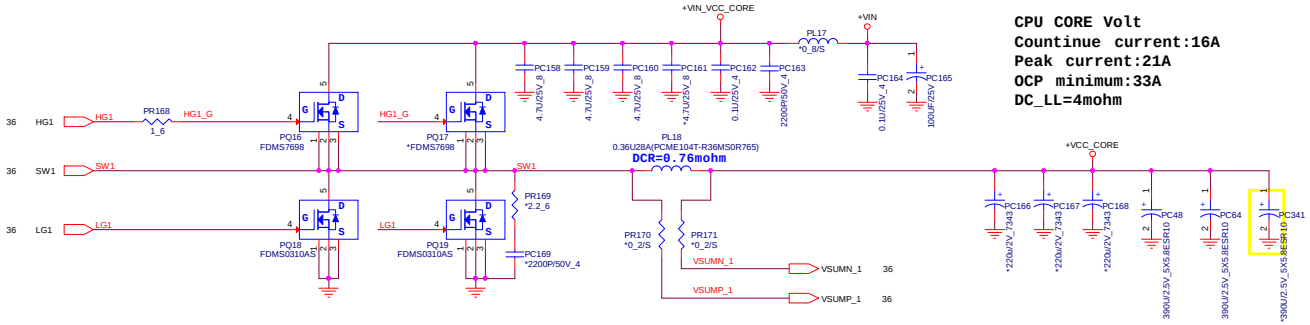
PROJECT : Y21A

Quanta Computer Inc.

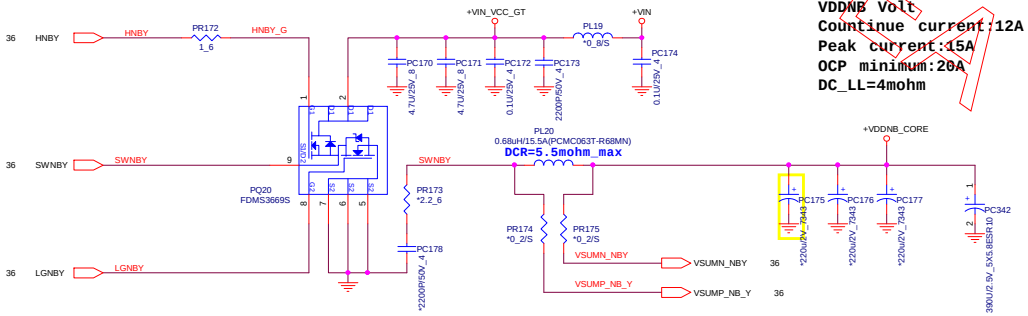
Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A
Date: Tuesday, November 18, 2014	Sheet 35 of 41	



PROJECT : Y02	
Quanta Computer Inc.	
Size: Custom	Document Number: CPU Core1 (ISL62771)
Rev: 1A	
NB5	Date: Tuesday, November 18, 2014 Sheet 36 of 41



CPU CORE Volt
Countinue current:16A
Peak current:21A
OCP minimum:33A
DC_LL=4mohm



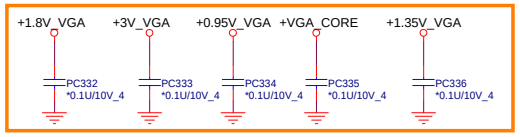
VDDNB Volt
Countinue current:12A
Peak current:15A
OCP minimum:20A
DC_LL=4mohm

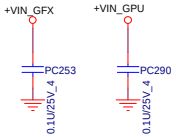
NB5

PROJECT : Y02
Quanta Computer Inc.

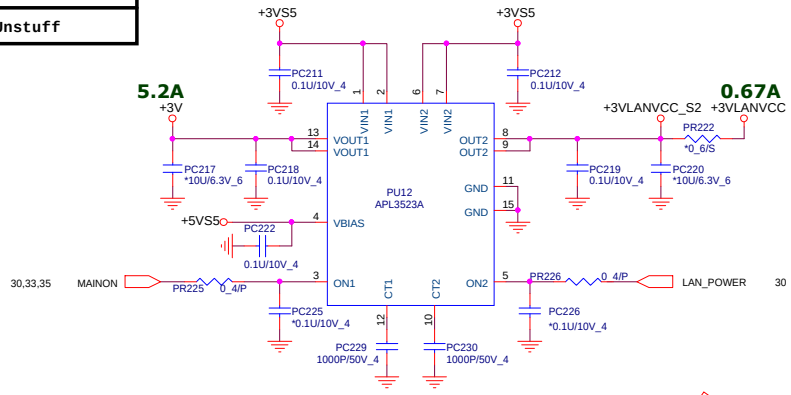
Size	Document Number	Rev
Custom	CPU Core2	1A

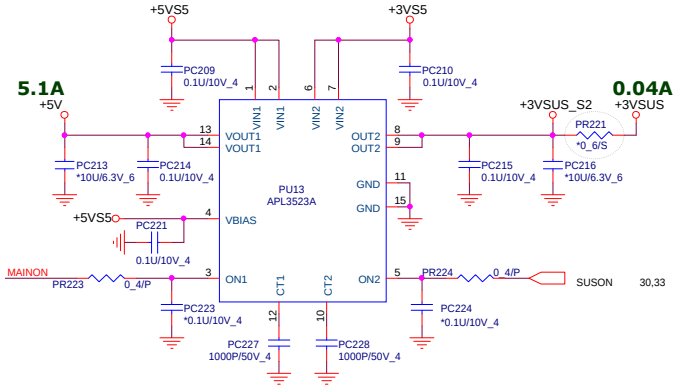
Date: Tuesday, November 18, 2014 | Sheet 37 of 41

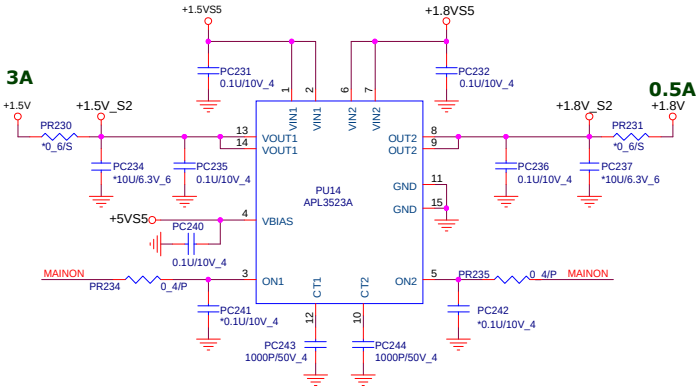




UMA only	Stuff
discrete	Unstuff







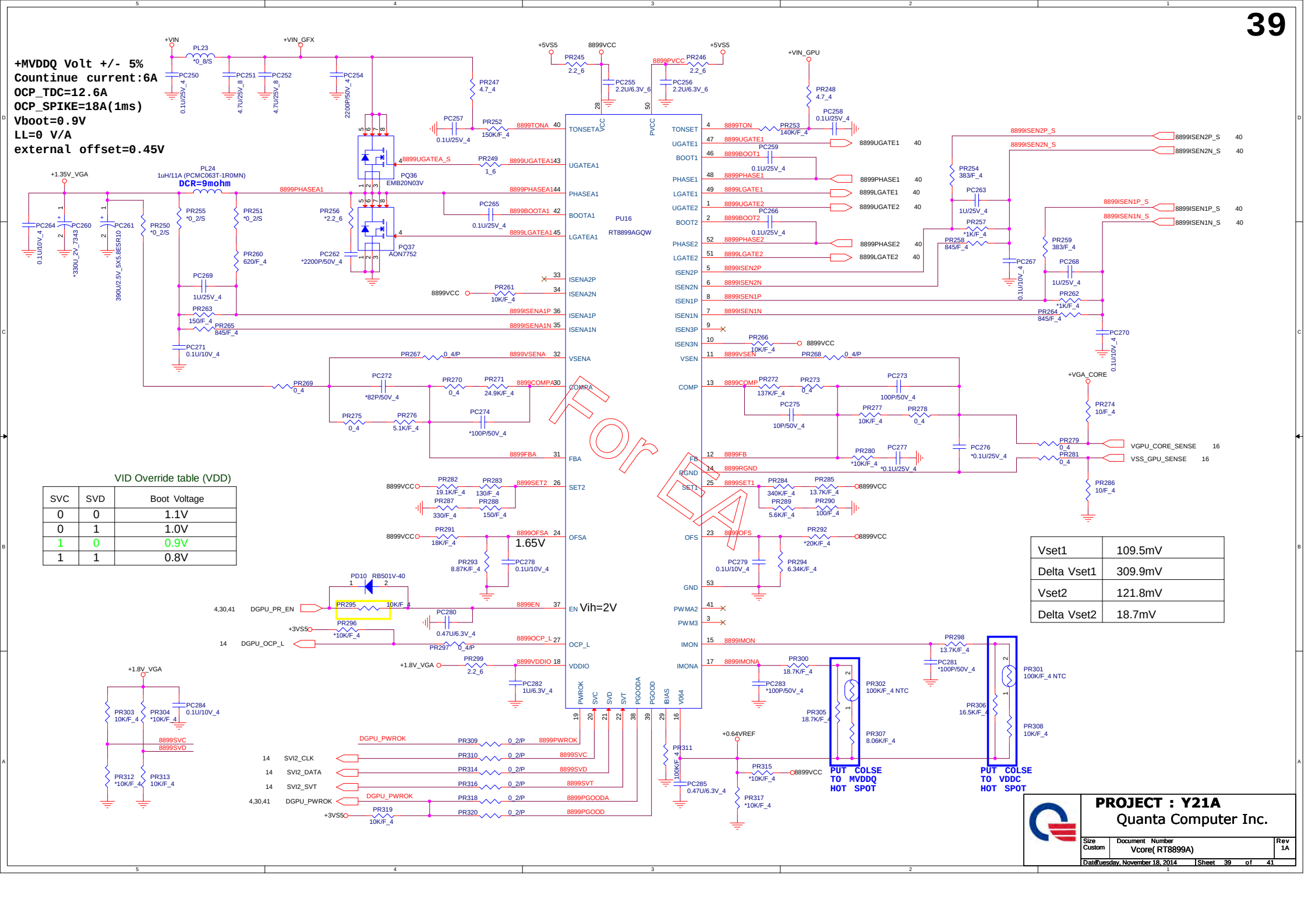
NB5/RD3

PROJECT : Y2x
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448)	1A

Date: Tuesday, November 18, 2014 | Sheet 38 of 41

+MVDDQ Volt +/- 5%
Countinue current:6A
OCP_TDC=12.6A
OCP_SPIKE=18A(1ms)
Vboot=0.9V
LL=0 V/A
external offset=0.45V



VID Override table (VDD)

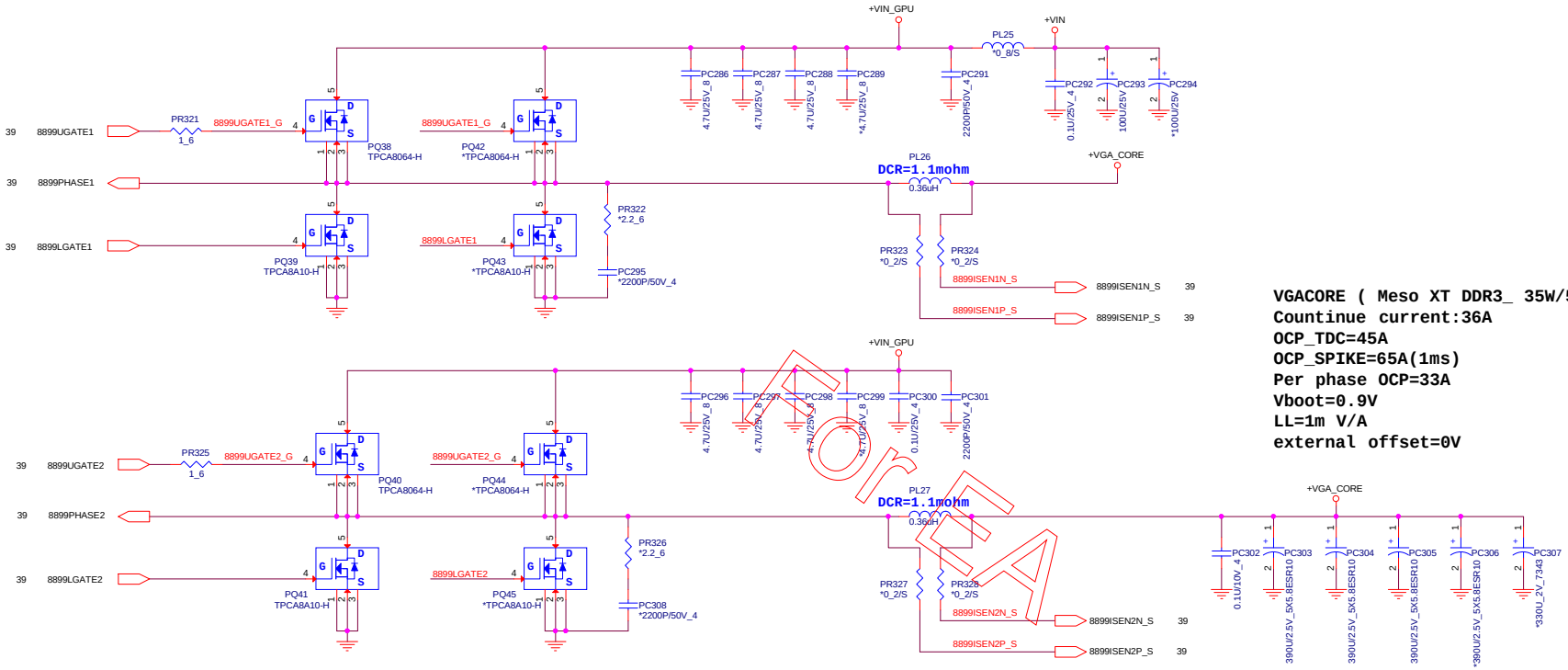
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

Vset1	109.5mV
Delta Vset1	309.9mV
Vset2	121.8mV
Delta Vset2	18.7mV

PROJECT : Y21A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Vcore(RT8899A)	1A

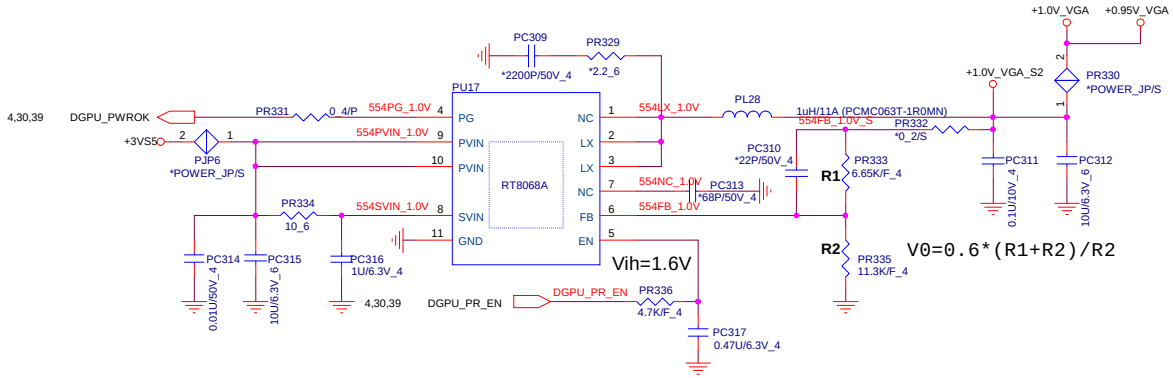
Date: Tuesday, November 18, 2014 Sheet 39 of 41

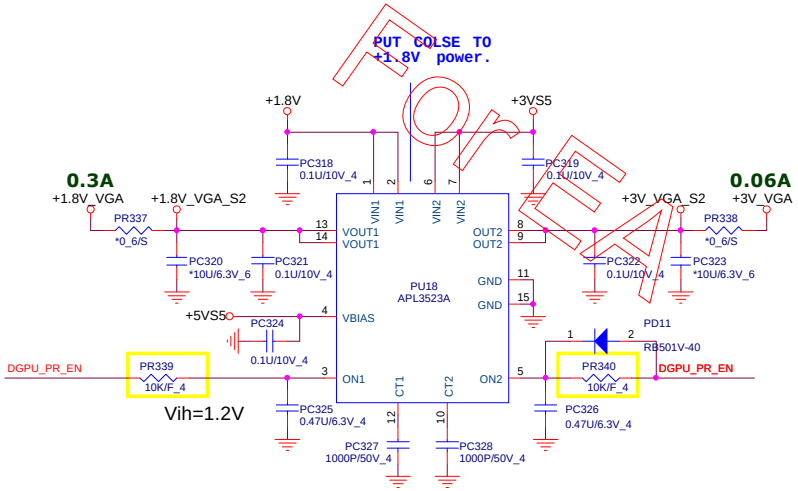


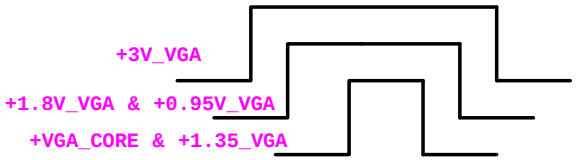
VGACORE (Meso XT DDR3_ 35W/53W(1ms))
Countinue current:36A
OCP_TDC=45A
OCP_SPIKE=65A(1ms)
Per phase OCP=33A
Vboot=0.9V
LL=1m V/A
external offset=0V

PROJECT : Y21A Quanta Computer Inc.		
Size: Custom	Document Number: CPU Core2	Rev: 1A
Date: Tuesday, November 18, 2014	Sheet 40 of 41	

+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A







+3V_VGA 13,14,16,38
+1.0V_VGA 13,16,38
+1.8V_VGA 13,14,16,38,39

PROJECT : Y21A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGA POWER	1A
Date: Tuesday, November 18, 2014	Sheet 41 of 41	