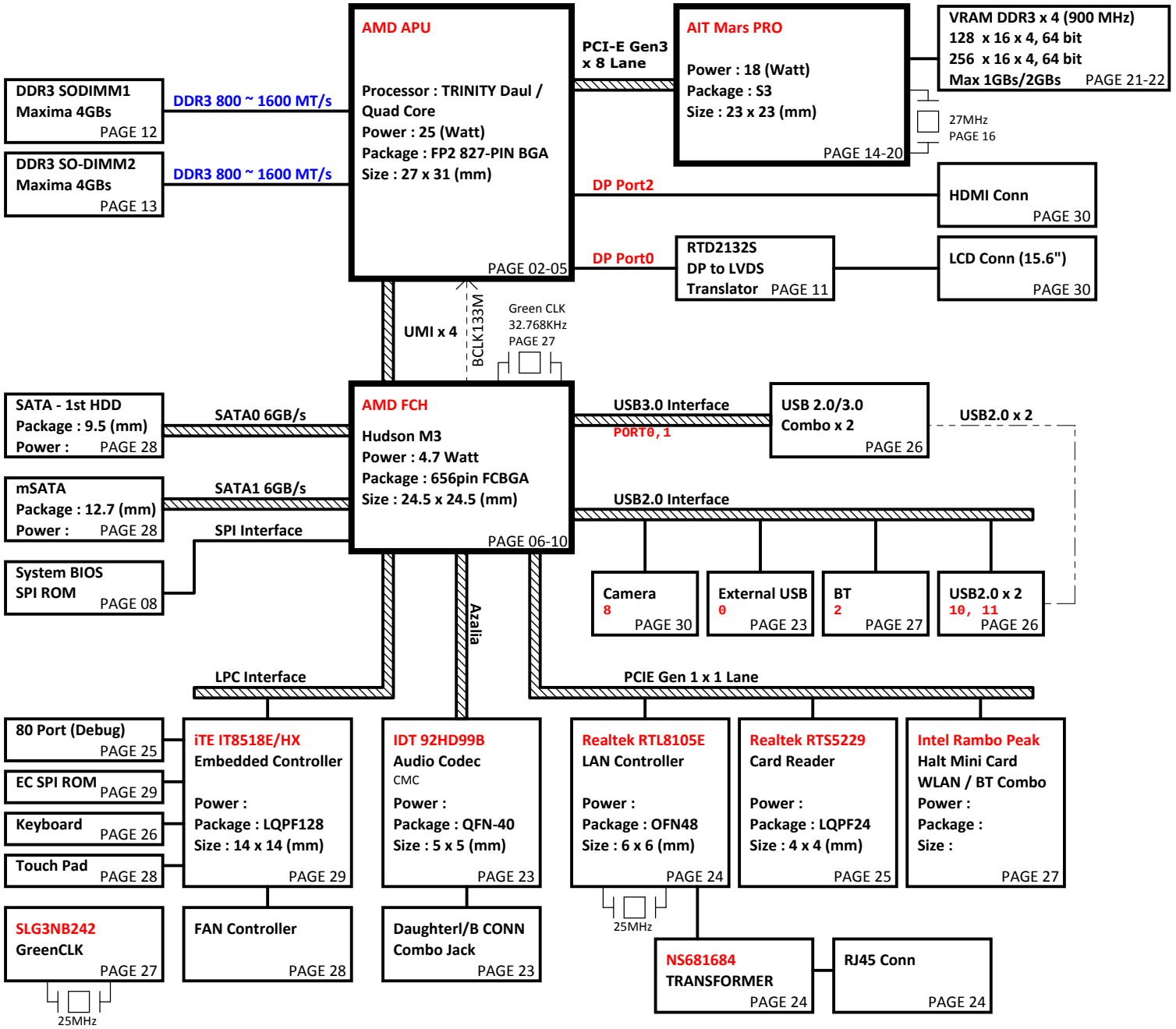
Tiguan1.0_AMD Comal DIS/UMA (15.6") Ultra/Slim

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24728
System Charge Power (+BATCHG)

G5934RZ1U
System Discharge Power
(+1.5V/+3V/+5V)
(+3VSUSV/+3VLANVCC/+1.1V)

Ricktek RT8223PZ
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

ISL6277/RT8228AZ/AP3407A/ISL6208BCRZ
Processor Power (+VCC_CORE/
+1.2V/+2.5V/+VDDNB_CORE)

Richtek RT8207L
System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)

Richtek RT8228AZ
PCH Power (+1.1VS5)

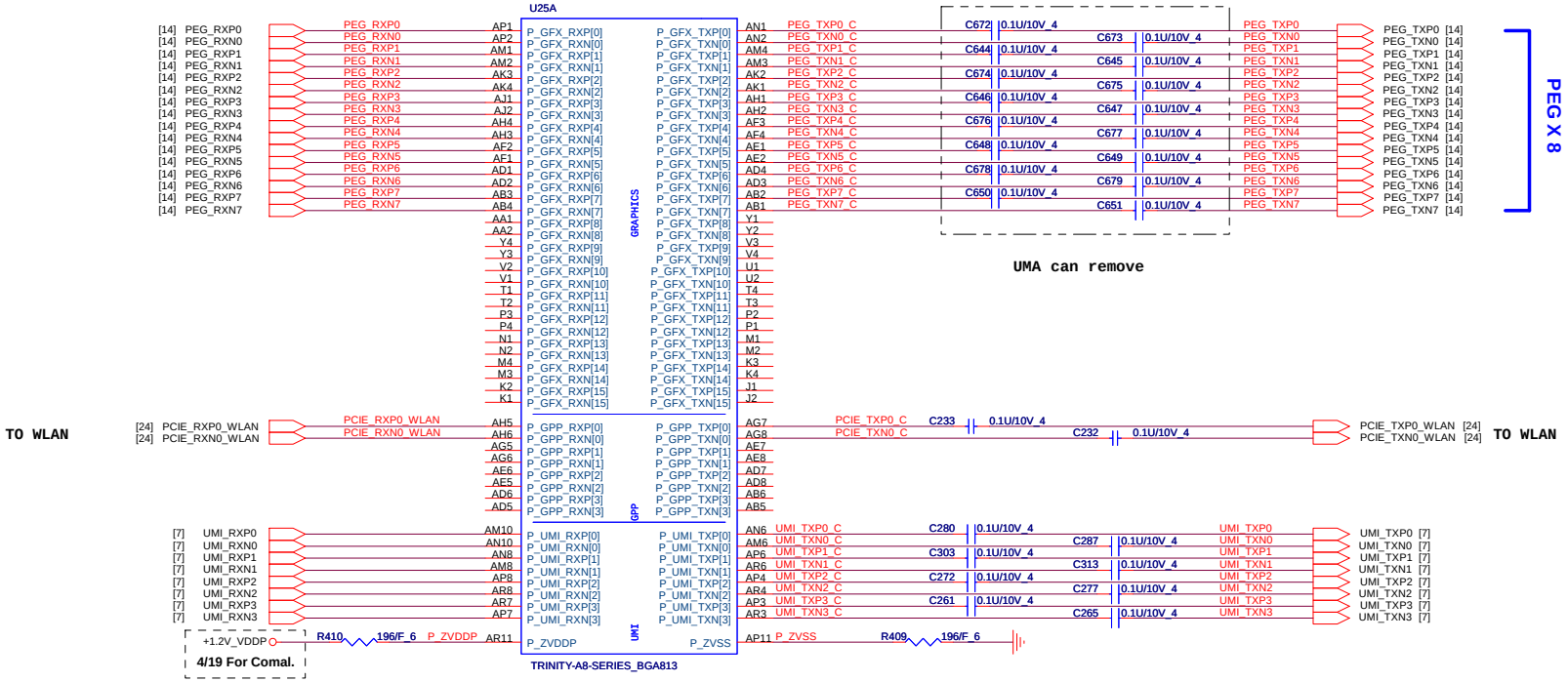
RT8152E/G5193/G5193R41U/NB650
DGPU Power (+VGA_CORE/+1.0V_VGA/+3V_VGA/
+1.5V_VGA/+1.8V_VGA/+VDDCI)

NB5

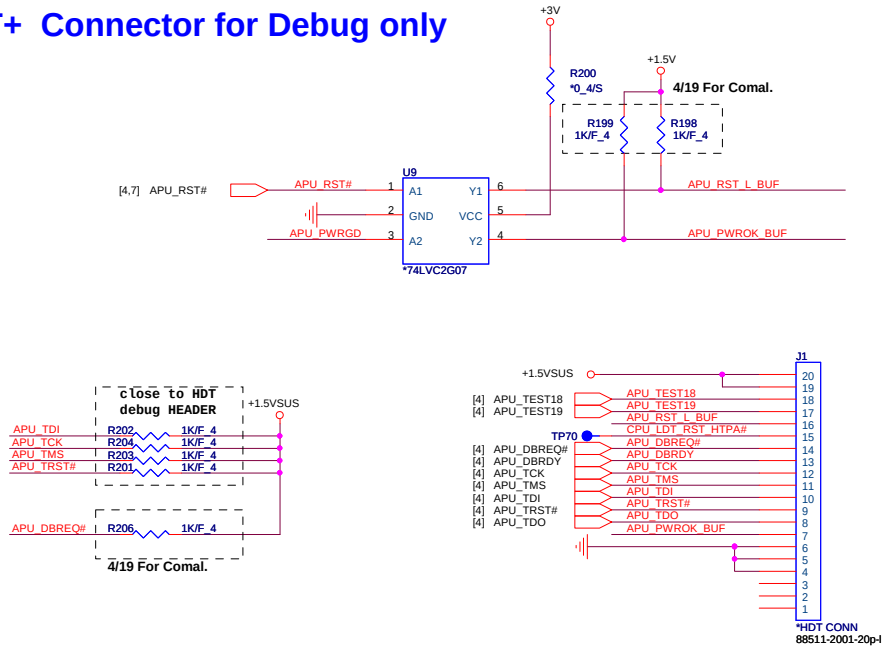
PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
A3	Block Diagram	1A

Date: Thursday, August 09, 2012 | Sheet 1 of 39



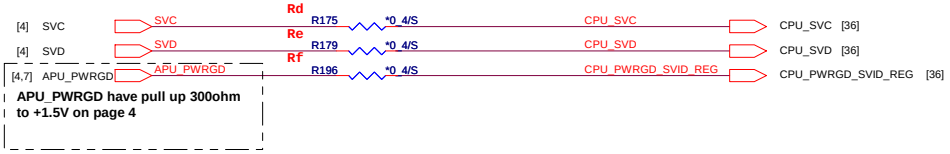
HDT+ Connector for Debug only



VID Override Circuit

	BOOT VOLTAGE		
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

Note:
To override VID,Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.

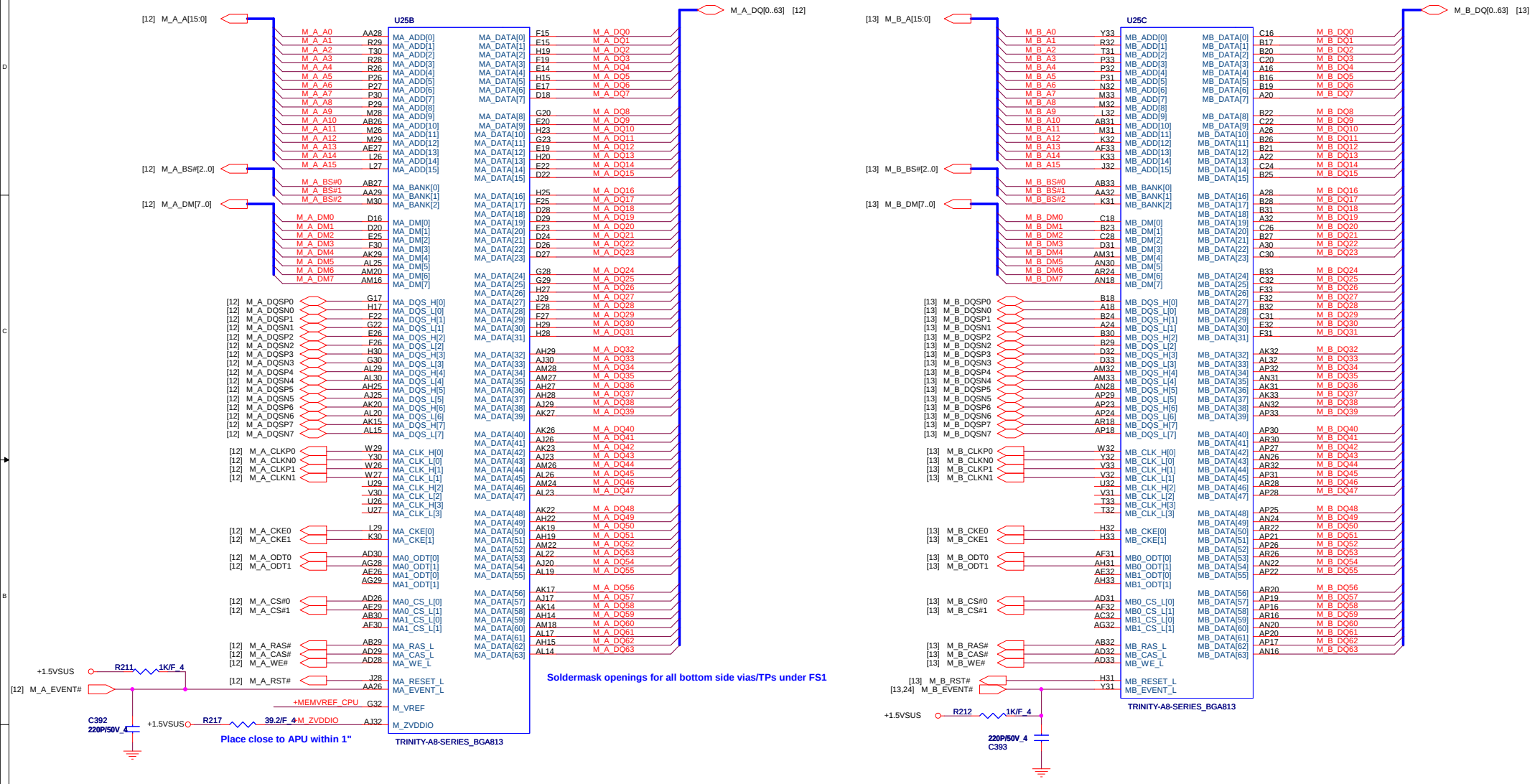


NB5

PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Llano PCIE/UMI/GPP	1A

Date: Tuesday, August 07, 2012 Sheet 2 of 39


U25B
TRINITY-A8-SERIES_BGA813
M_A_DQ[0..63] [12]
Soldermask openings for all bottom side vias/TPs under FS1
Place close to APU within 1"
U25C
TRINITY-A8-SERIES_BGA813
M_B_DQ[0..63] [13]
Reserved for AMD suggest

Place caps with APU < 1 inch
route PCIE as 85ohm +/- 10%

DP0 output to
eDP to LVDS converter

Display port power 1.5V min 1.2v max : 1.65v

4/19 HDMI change to DP2 for Comal.

DP2 output to
HDMI connector

note --HDMI P&N can not swap

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

DMAACTIVE_L controls
entry and exit from the
sleep and power states

7/8 For Comal.

TEST35 PU FOR INTERNAL
TEST35 PD FOR CUSTOMER

4/19 For Comal,
close to APU.

THERMTRIP# shutdown temperature 125度C

ADD VGA TEMP_ FAIL function is active Hi

over 120 degree C= Low

When 100K-NTC 100 C=6.164K
Thermal Trip = 120 C

Thermal

PROJECT : U56	
Quanta Computer Inc.	
NB5	
Size	Document Number: Llano Display/Misc
Rev	1A
Date: Tuesday, August 07, 2012	Sheet 4 of 39

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

EMI suggestion

+VCC_CORE

C357 470P/50V_4 | C328 *470P/50V_4 | C356 *470P/50V_4

U25E

+VCC_CORE

36A

Maximum IDDspike 50A

C333 22U/6.3VS_8 | C335 22U/6.3VS_8 | C346 22U/6.3VS_8 | C359 22U/6.3VS_8 | C315 22U/6.3VS_8 | C706 22U/6.3VS_8 | C345 22U/6.3VS_8 | C317 22U/6.3VS_8

C330 22U/6.3VS_8 | C331 22U/6.3VS_8 | C309 22U/6.3VS_8 | C285 *22U/6.3VS_8 | C316 *22U/6.3VS_8 | C693 *22U/6.3VS_8 | C323 *22U/6.3VS_8

C319 0.22U/10V_4 | C369 0.22U/10V_4 | C332 180P/50V_4 | C338 180P/50V_4 | C358 180P/50V_4 | C360 0.01U/25V_4 | C347 0.01U/25V_4 | C349 0.01U/25V_4

+VDDNB_CORE

C728 22U/6.3VS_8 | C743 22U/6.3VS_8 | C729 22U/6.3VS_8 | C734 22U/6.3VS_8

C291 0.22U/10V_4 | C292 0.22U/10V_4 | C290 180P/50V_4 | C288 180P/50V_4 | C289 180P/50V_4

+VDDNB_CAP

C297 22U/6.3VS_8 | C294 22U/6.3VS_8 | C295 22U/6.3VS_8 | C296 22U/6.3VS_8 | C286 180P/50V_4

+VDDP_CAP

C298 22U/6.3VS_8 | C299 *22U/6.3VS_8

+VDDNB_CORE

+VDDNB_CORE

25A

Maximum IDDNBspike 33A

+VDDNB_CAP

DECOUPLING between PROCESSOR and DIMMs

Across VDDIO and VSS split

+1.5VSUS

C425 4.7U/6.3V_6 | C493 4.7U/6.3V_6 | C365 4.7U/6.3V_6 | C422 4.7U/6.3V_6 | C412 0.22U/10V_4 | C477 0.22U/10V_4 | C756 0.22U/10V_4 | C757 0.22U/10V_4

If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

+1.5VSUS

2.8A Up to DDR3-1333 @ 1.50V VDDIO

C448 0.22U/10V_4 | C414 0.22U/10V_4 | C450 0.22U/10V_4 | C418 0.22U/10V_4 | C468 0.22U/10V_4 | C361 0.22U/10V_4

C390 180P/50V_4 | C471 180P/50V_4 | C445 180P/50V_4 | C464 180P/50V_4 | C368 180P/50V_4

C362 22U/6.3VS_8 | C363 22U/6.3VS_8 | C421 4.7U/6.3V_6 | C426 4.7U/6.3V_6 | C415 4.7U/6.3V_6 | C366 4.7U/6.3V_6

+1.2V_VDDP

VDDP = 5A

+1.2V | R413 *0_8/S | +1.2V_VDDP

C723 22U/6.3VS_8 | C727 0.22U/10V_4 | C720 0.22U/10V_4 | C724 22U/6.3VS_8

C725 180P/50V_4 | C730 180P/50V_4 | C731 *22U/6.3VS_8

+VDDP_CAP

TP66

VDDR = 3.3A (Up to DDR3-1333 @ 1.5V)

+1.2V_VDDR_B

C740 0.22U/10V_4 | C732 0.22U/10V_4 | C738 1000P/50V_4 | C735 180P/50V_4 | C733 180P/50V_4

R414 *0_8/S | +1.2V

TRINITY-A8-SERIES_BGA813

VDDA= 0.75A

+2.5V | L32 PBY160808T-221Y-N(220,2A) | +2.5V_VDDA

C348 4.7U/6.3V_6 | C343 0.22U/10V_4 | C344 3300P/50V_4

U25F

TRINITY-A8-SERIES_BGA813

PROJECT : U56

Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Llano POWER/GND	1A

Date: Wednesday, July 11, 2012 | Sheet 5 of 39

+3VS5 NC,no install by default
R166 *2.2K_4 FCH_TEST0
R173 *2.2K_4 FCH_TEST1
R169 *2.2K_4 FCH_TEST2

+3V
R192 2.2K_4 SMB_RUN_CLK
R193 2.2K_4 SMB_RUN_DAT
to DDR3 SMBUS
+3VS5
R168 *1K_4 SYS_RST#
SYS_RST# internal 10K pull up

GEVENT0# internal pull Hi 8.2K to +3V
GEVENT1# internal pull Hi 8.2K to +3V
GEVENT23# internal pull Hi 8.2K to +3V
GEVENT5# internal pull Hi 8.2K to +3VS5
PCIE_WAKE# no need to pull
Hi resistor from check list

+3VS5
R134 10K/F_4 SCL3
R136 10K/F_4 SDA3
R128 10K/F_4 SCL2
R132 10K/F_4 SDA2
R156 2.2K_4 SCL1
R155 2.2K_4 SDA1
R160 *4.7K_4 FCH_THERMTRIP#
C271 *0.01U/25V_4
R353 10K/F_4 DNBSWON#

CLK_REQ2# internal pull Hi 8.2K to +3V
CLK_REQ3# internal pull Hi 8.2K to +3V
CLK_REQ4# internal pull Hi 8.2K to +3V
GEVENT16# internal pull Hi 8.2K to +3VS5
GEVENT15# internal pull Hi 8.2K to +3VS5

This pin is used to power down VGA DAC regulators when CRT no connected

4/19 For Comal.
For Zero ODD

HD audio interface is +3V_S5 voltage

To Azalia

ACZ_SDOUT_R R399 33_4 ACZ_SDOUT_AUDIO [20]
ACZ_SYNC_R R400 33_4 ACZ_SYNC_AUDIO [20]
ACZ_BCLK_R R403 33_4 BIT_CLK_AUDIO [20]
ACZ_RST#_R R411 33_4 ACZ_RST#_AUDIO [20]
ACZ_SDIN0 ACZ_SDIN0 [20]
C273 *33P/50V_4
C278 33P/50V_4
6/21/2012 for EMI

Pure UMA can remove
CLK_REQ# already internal pull up 8.2K
[34] VGA_REQ 1 D20 RB501V-40 2 CLKREQ1#
R421 10K/F_4
[33,34,35] DGPU_PWROK
Q21 *MMBT3904-7-F

TP106 TP101 PCIE_RST2# RI#
[26] SUSB# [26] SUSC# [26] DNBSWON# [10] FCH_PWRGD
TP44 TP42 FCH_TEST0 FCH_TEST1 FCH_TEST2 EC_A20GATE EC_RCIN# FCH_PME# SIO_EXT_SMI# SIO_EXT_SCI# SYS_RST# PCIE_WAKE# FCH_THERMTRIP#
[26] EC_A20GATE [26] EC_RCIN# [26] SIO_EXT_SMI# [26] SIO_EXT_SCI# [21,24] PCIE_WAKE# [4] FCH_THERMTRIP#
R394 *0_4/S GEVENT5#
C690 *100P/50V_4
R189 10K/F_4 WD_PWRGD
[26] RSMRST#
[22] PCIE_CLKREQ_CR# [21] PCIE_CLKREQ_LAN#
R415 *0_4/S FCH_GPIO66
[20] SPKR [12,13] SMB_RUN_CLK [12,13] SMB_RUN_DAT [11,25] SCL1 [11,25] SDA1 [24] PCIE_CLKREQ_WLAN#
[24] RF_OFF1#
TP62 TP45 SMARTVOLT2 VGA_PD
TP46 GBE_LED0
TP52
TP90 TP103 ODD_PLUGIN#
TP35 TP100 TP89 TP43 FCH_JTAG_TCK FCH_JTAG_TDI FCH_JTAG_RST#
R404 R396 R391 R397 R390 *10K/F_4 ACZ_BCLK_R ACZ_SDOUT_R ACZ_SDIN0 ACZ_SDIN1 ACZ_SDIN2_R ACZ_SDIN3_R ACZ_SYNC_R ACZ_RST#_R
TP36 TP34
[24] BT_COMBO_OFF#
[14] VGA_RSTB [26] VGA_ON_SB

U23A
HUDSON-M3
Part 4 of 5
Hudson-M3-A14

PCIE_RST2#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
GPIO

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
HD AUDIO

PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/XDB0/GPIO223
KSO_15/XDB1/GPIO224
KSO_16/XDB2/GPIO225
KSO_17/XDB3/GPIO226
EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB MISC
USB 1.1

USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USB 2.0

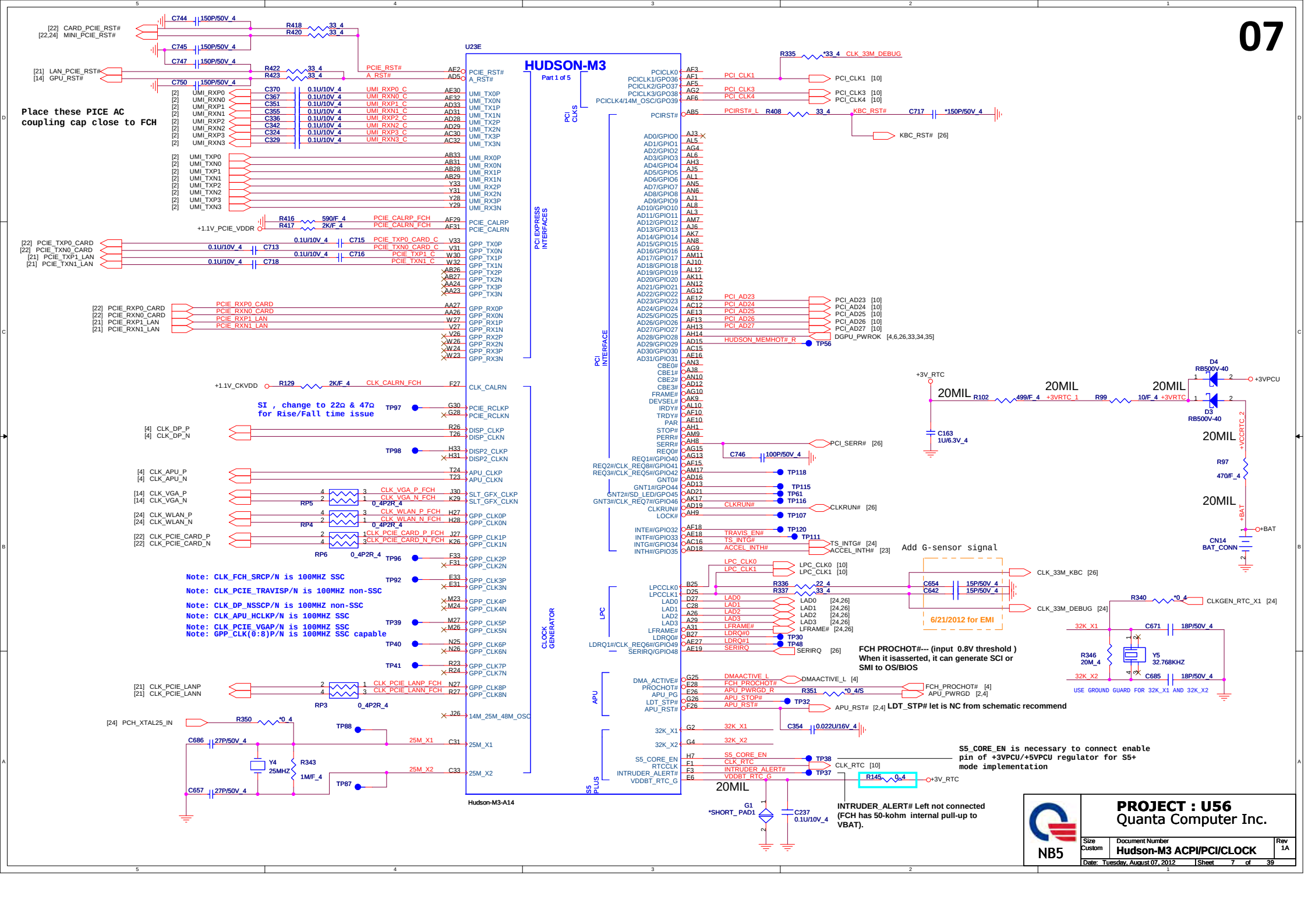
USBSS_CALRP
USBSS_CALRN
USB_SS_TX3P
USB_SS_TX3N
USB_SS_RX3P
USB_SS_RX3N
USB_SS_TX2P
USB_SS_TX2N
USB_SS_RX2P
USB_SS_RX2N
USB_SS_TX1P
USB_SS_TX1N
USB_SS_RX1P
USB_SS_RX1N
USB_SS_TX0P
USB_SS_TX0N
USB_SS_RX0P
USB_SS_RX0N
USB 3.0

SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208

USB_RCOMP_SB R348 11.8K/F_6
USBP11+ USBP11- [23] USB Combo 3.0/2.0.
USBP10+ USBP10- [23] USB Combo 3.0/2.0.
USBP8+ USBP8- [27] CAMERA
USBP3+ USBP3- [24] Touch screen
USBP2+ USBP2- [24] WLAN Min-Card
EXternal MIC
LEFT side USB 2.0 Connector
USBSS_CALRP R349 1K/F_4
USBSS_CALRN R342 1K/F_4
+FCH_VDD_11_SSUSB_S
USB 3.0 Not Implemented: left unconnected.
USB30_TX1+ USB30_TX1- [23]
USB30_RX1+ USB30_RX1- [23]
USB30_TX0+ USB30_TX0- [23]
USB30_RX0+ USB30_RX0- [23]
SCL2 SDA2 SCL3 SDA3
EC_PWM2 [10]
No need for GPIO200

SCL3 of a TSI-capable APU's thermal bus,Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.

NB5
PROJECT : U56
Quanta Computer Inc.
Size Custom | Document Number Hudson-M3 GPIO/USB/AZ/RGMII | Rev 1A
Date: Tuesday, August 07, 2012 | Sheet 6 of 39


HUDSON-M3
Part 1 of 5
U23E
Hudson-M3-A14
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
APU
S5 PLUS
Place these PICE AC coupling cap close to FCH
SI , change to 22Ω & 47Ω for Rise/Fall time issue
Note: CLK_FCH_SRCP/N is 100MHZ SSC
Note: CLK_PCIE_TRAVISP/N is 100MHZ non-SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_PCIE_VGAP/N is 100MHZ SSC
Note: GPP_CLK(0:8)P/N is 100MHZ SSC capable
Add G-sensor signal
6/21/2012 for EMI
FCH PROCHOT#--- (input 0.8V threshold) When it isasserted, it can generate SCI or SMI to OS/BIOS
LDT_STP# let is NC from schematic recommend
S5_CORE_EN is necessary to connect enable pin of +3VPCU/+5VPCU regulator for S5+ mode implementation
INTRUDER_ALERT# Left not connected (FCH has 50-kohm internal pull-up to VBAT).
USE GROUND GUARD FOR 32K_X1 AND 32K_X2
PROJECT : U56
Quanta Computer Inc.
NB5
Hudson-M3 ACPI/PCI/CLOCK
Size Custom
Document Number
Rev 1A
Date: Tuesday, August 07, 2012
Sheet 7 of 39

U23D

HUDSON-M3

Part 5 of 5

GROUND

A3	VSS_1	VSS_65	T25		
A33	VSS_2	VSS_66	T27		
B7	VSS_3	VSS_67	U6		
B13	VSS_4	VSS_68	U14		
D9	VSS_5	VSS_69	U17		
D13	VSS_6	VSS_70	U20		
E5	VSS_7	VSS_71	U21		
E12	VSS_8	VSS_72	U30		
E16	VSS_9	VSS_73	U32		
E29	VSS_10	VSS_74	V11		
F7	VSS_11	VSS_75	V16		
F9	VSS_12	VSS_76	V18		
F11	VSS_13	VSS_77	W4		
F13	VSS_14	VSS_78	W6		
F16	VSS_15	VSS_79	W25		
F17	VSS_16	VSS_80	W28		
F19	VSS_17	VSS_81	Y14		
F23	VSS_18	VSS_82	Y16		
F25	VSS_19	VSS_83	Y18		
F29	VSS_20	VSS_84	AA6		
G6	VSS_21	VSS_85	AA12		
G16	VSS_22	VSS_86	AA13		
G32	VSS_23	VSS_87	AA14		
H12	VSS_24	VSS_88	AA16		
H15	VSS_25	VSS_89	AA17		
H29	VSS_26	VSS_90	AA25		
J6	VSS_27	VSS_91	AA28		
J9	VSS_28	VSS_92	AA30		
J10	VSS_29	VSS_93	AA32		
J13	VSS_30	VSS_94	AB25		
J28	VSS_31	VSS_95	AC6		
J32	VSS_32	VSS_96	AC18		
K7	VSS_33	VSS_97	AC28		
K16	VSS_34	VSS_98	AD27		
K27	VSS_35	VSS_99	AE6		
K28	VSS_36	VSS_100	AE15		
L6	VSS_37	VSS_101	AE21		
L12	VSS_38	VSS_102	AE28		
L13	VSS_39	VSS_103	AF8		
L15	VSS_40	VSS_104	AF12		
L16	VSS_41	VSS_105	AF16		
L21	VSS_42	VSS_106	AF33		
M13	VSS_43	VSS_107	AG30		
M16	VSS_44	VSS_108	AG32		
M21	VSS_45	VSS_109	AH5		
M25	VSS_46	VSS_110	AH11		
N6	VSS_47	VSS_111	AH18		
N11	VSS_48	VSS_112	AH19		
N13	VSS_49	VSS_113	AH21		
N23	VSS_50	VSS_114	AH23		
N24	VSS_51	VSS_115	AH25		
P12	VSS_52	VSS_116	AH27		
P18	VSS_53	VSS_117	AJ18		
P20	VSS_54	VSS_118	AJ28		
P21	VSS_55	VSS_119	AJ29		
P31	VSS_56	VSS_120	AK21		
P33	VSS_57	VSS_121	AK25		
R4	VSS_58	VSS_122	AL18		
R11	VSS_59	VSS_123	AM21		
R25	VSS_60	VSS_124	AM25		
R28	VSS_61	VSS_125	AN1		
T11	VSS_62	VSS_126	AN18		
T16	VSS_63	VSS_127	AN28		
T18	VSS_64	VSS_128	AN33		
N8	VSSAN_HWM	VSSPL_DAC	T21		
		VSSAN_DAC	L28		
K25	VSSXL	VSSANQ_DAC	K33		
		VSSIO_DAC	N28		
H25	VSSPL_SYS				
		EFUSE	R6		

Hudson-M3-A14

PLACE SATA AC COUPLING
CAPS CLOSE TO HUDSON-M2/M3

SATA HDD

MINISATA

[25] SATA_TXP0	SATA_TXP0	AK19	SATA_TX0P
[25] SATA_TXN0	SATA_TXN0	AM19	SATA_TX0N
[25] SATA_RXN0		AL20	SATA_RX0N
[25] SATA_RXP0		AN20	SATA_RX0P
[25] SATA_TXP1	SATA_TXP1	AN22	SATA_TX1P
[25] SATA_TXN1	SATA_TXN1	AL22	SATA_TX1N
[25] SATA_RXN1		AH20	SATA_RX1N
[25] SATA_RXP1		AJ20	SATA_RX1P
		AJ22	SATA_TX2P
		AH22	SATA_TX2N
		AM23	SATA_RX2N
		AK23	SATA_RX2P
		AH24	SATA_TX3P
		AJ24	SATA_TX3N
		AN24	SATA_RX3N
		AL24	SATA_RX3P
		AL26	SATA_TX4P
		AN26	SATA_TX4N
		AJ26	SATA_RX4N
		AH26	SATA_RX4P
		AN29	SATA_TX5P
		AL28	SATA_TX5N
		AK27	SATA_RX5N
		AM27	SATA_RX5P
		AL29	NC6
		AN31	NC7
		AL31	NC8
		AL33	NC9
		AH33	NC10
		AH31	NC11
		AJ33	NC12
		AJ31	NC13
	SATA_CALRP	AF28	SATA_CALRP
	SATA_CALRN	AF27	SATA_CALRN
		AD22	SATA_ACT#/GPIO67
		AF21	SATA_X1
		AG21	SATA_X2

[25] SATA_LED# — R187 *0_4/S — SB_SATA_LED#

PV , change
to short pad

PLACE SATA_CAL RES VERY
CLOSE TO BALL OF
HUDSON-M2/M3

+1.1V_AVDD_SATA — R181 1K/F_4 — R177 931/F_4

4/19 For Comal.

+3V — R194 *220/F_6 — SB_SATA_LED#

Integrated Clock Mode:
Leave unconnected.

GPIO52 internal pull Hi 8.2K to +3V
GPIO53 internal pull Hi 8.2K to +3V
GPIO54 internal pull Hi 8.2K to +3V
GPIO56 internal pull Hi 8.2K to +3V
GPIO57 internal pull Hi 8.2K to +3V
GPIO58 internal pull Hi 8.2K to +3V

[24] RF_OFF#	RF_OFF#	AH16	FANOUT0/GPIO52
TP105	BT_OFF#	AM15	FANOUT1/GPIO53
TP63	BT_COMBO_EN#	AJ16	FANOUT2/GPIO54
[25] ACC_LED#		AK15	FANIN0/GPIO56
		AN16	FANIN1/GPIO57
[27] LCD_BK	LCD_BK	AL16	FANIN2/GPIO58
	TEMPIN0	K6	TEMPIN0/GPIO171
	TEMPIN1	K5	TEMPIN1/GPIO172
	TEMPIN2	K3	TEMPIN2/GPIO173
	TEMPIN3	M6	TEMPIN3/TALERT#/GPIO174

R142 10K/F_4 R143 10K/F_4 R358 10K/F_4 R144 10K/F_4

TEMP(0 - 3)
Temp Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

U23B

HUDSON-M3

Part 2 of 5

SERIAL ATA

SD CARD

SD_CLK/SCLK_2/GPIO73	AL14
SD_CMD/SLOAD_2/GPIO74	AN14
SD_CD#/GPIO75	AJ12
SD_WP/GPIO76	AH12
SD_DATA0/SDATI_2/GPIO77	AK13
SD_DATA1/SDATO_2/GPIO78	AM13
SD_DATA2/GPIO79	AH15
SD_DATA3/GPIO80	AJ14

GBE LAN

GBE_COL	AC4
GBE_CRS	AD3
GBE_MDCK	AD9
GBE_MDIO	W10
GBE_RXCLK	AB8
GBE_RXD3	AH7
GBE_RXD2	AE7
GBE_RXD1	AD7
GBE_RXD0	AG8
GBE_RXCTL/RXDV	AD1
GBE_RXERR	AB7
GBE_TXCLK	AF9
GBE_TXD3	AG6
GBE_TXD2	AE8
GBE_TXD1	AD8
GBE_TXD0	AB9
GBE_TXCTL/TXEN	AC2
GBE_PHY_PD	AA7
GBE_PHY_RST#	W9
GBE_PHY_INTR	

GBE_PHY_INTR — R167 10K/F_4 — +3VS5

+3VS5 — R427 10K/F_4

SPI ROM

SPI_DI/GPIO164	V6	SPI_SI
SPI_DO/GPIO163	V5	SPI_SO
SPI_CLK/GPIO162	V3	SPI_CLK
SPI_CS1#/GPIO165	T6	SPI_CS0#
ROM_RST#/SPI_WP#/GPIO161	V1	FCH_SPI_WP

TP110 TP109 TP113 TP114 TP104

SPI_CS0# *0_4/S R428 — EC_BIOS_CS# [26]
SPI_CLK *0_4/S R426 — EC_BIOS_SPI_CLK_I [26]
SPI_SO *0_4/S R425 — EC_BIOS_WR# [26]
SPI_SI *0_4/S R429 — EC_BIOS_RD# [26]

VGA DAC

VGA_RED	L30	
VGA_GREEN	L32	
VGA_BLUE	M29	
VGA_HSYNC/GPO68	M28	
VGA_VSYNC/GPO69	N30	
VGA_DDC_SDA/GPO70	M33	
VGA_DDC_SCL/GPO71	N32	
VGA_DAC_RSET	K31	TP99

VGA MAINLINK

AUX_VGA_CH_P	V28	
AUX_VGA_CH_N	V29	
AUXCAL	U28	TP102
ML_VGA_L0P	T31	
ML_VGA_L0N	T33	
ML_VGA_L1P	T29	
ML_VGA_L1N	T28	
ML_VGA_L2P	R32	
ML_VGA_L2N	R30	
ML_VGA_L3P	P29	
ML_VGA_L3N	P28	
ML_VGA_HPD/GPO229	C29	TP33

HW MONITOR

VIN0/GPIO175	N2	SIDE_PORT_ID0
VIN1/GPIO176	M3	SIDE_PORT_ID1
VIN2/SDATI_1/GPIO177	L2	SIDE_PORT_ID2
VIN3/SDATO_1/GPIO178	N4	BOARD_ID0
VIN4/SLOAD_1/GPIO179	P1	BOARD_ID1
VIN5/SCLK_1/GPIO180	P3	BOARD_ID2
VIN6/GBE_STAT3/GPIO181	M1	BOARD_ID3
VIN7/GBE_LED3/GPIO182	M5	BOARD_ID4
NC1	AG16	
NC2	AH10	
NC3	A28	
NC4	G27	
NC5	L4	

VIN (0 - 7)
Voltage Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

Hudson-M3-A14

Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

+3VS5 — R380 10K/F_4 BOARD_ID0 R381 *10K/F_4
R384 *10K/F_4 BOARD_ID1 R385 10K/F_4
R387 *10K/F_4 BOARD_ID2 R388 10K/F_4
R366 *10K/F_4 BOARD_ID3 R367 10K/F_4
R370 *10K/F_4 BOARD_ID4 R371 10K/F_4
R374 10K/F_4 SIDE_PORT_ID0 R375 *10K/F_4
R363 10K/F_4 SIDE_PORT_ID1 R364 *10K/F_4
R359 *10K/F_4 SIDE_PORT_ID2 R360 10K/F_4

NB5

PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hudson-M3 SATA/HWM/SPI	1A
Date: Tuesday, August 07, 2012	Sheet 8 of 39	

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

U23C

HUDSON-M3 Part 3 of 5

Hudson-M3-A14

POWER

VDDQ--3.3V I/O power 102mA

VDDCR-- S/B CORE power

1007mA for M3
902mA for M2

VDDAN_11_CLK-- Internal clock Generator I/O power 340mA

VDDAN_11_PCIE --PCIE/UMI analog power 1088mA

VDDAN_11_ML -- UMI 1.1V analog power

VDDPL_11_SYS_S : System Clock Gen PLLs analog power

VDDAN_11_SATA--SATA PHY analog/IO power 1337mA

VDDPL_33_USB_S : USB PHY PLL analog power

VDDAN_33_USB_S : USB PHY I/O analog power 470mA

VDDAN_11_USB_S : USB PHY PLL analog power 140mA

VDDCR_11_USB_S : USB PHY core power 42mA

VDDIO_33_S-- 3.3v S5 I/O power 59mA

VDDXL_33_S-- 25MHZ XTAL IO power 5mA

VDDCR_1.1_S-- 1.1V S5 Core power 187mA

VDDAN_11_SSUSB_S : USB3.0 PHY PLL analog power 282mA

VDDCR_11_SSUSB_S : USB3.0 PHY core power 424mA

M3 chipset need to stuff for support USB3.0

SI , AMD SR tool review

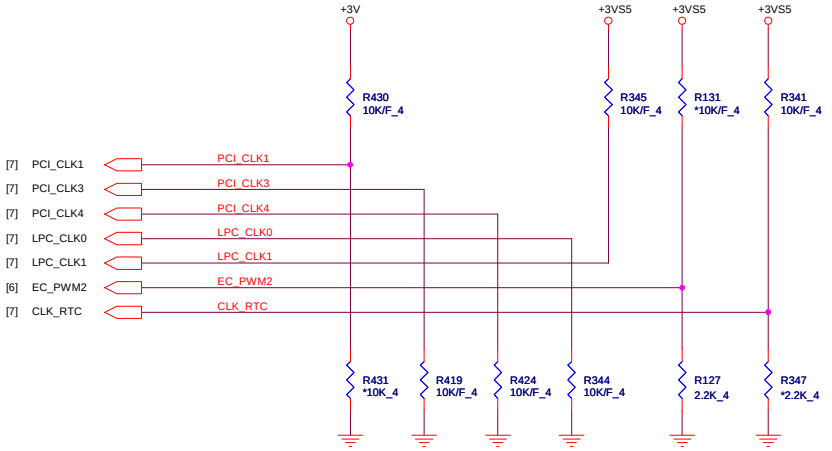
if support USB 3.0 wake up should be change pull hi to S5 power

if support Modem wake up should be change pull hi to S5 power

PROJECT : U56	Quanta Computer Inc.
NB5	Size: Custom; Document Number: Hudson-M3 POWER/GND; Rev: 1A
	Date: Tuesday, August 07, 2012; Sheet 9 of 39

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

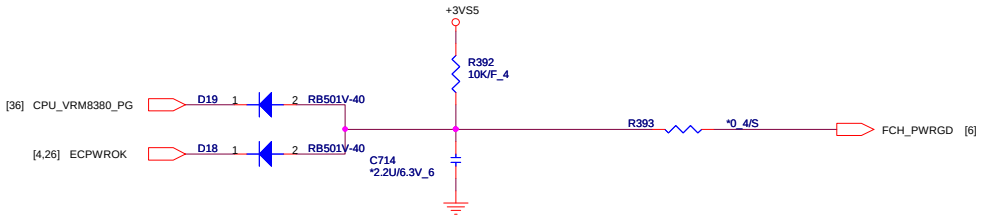
	--------	PCI_CLK1	--------	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD

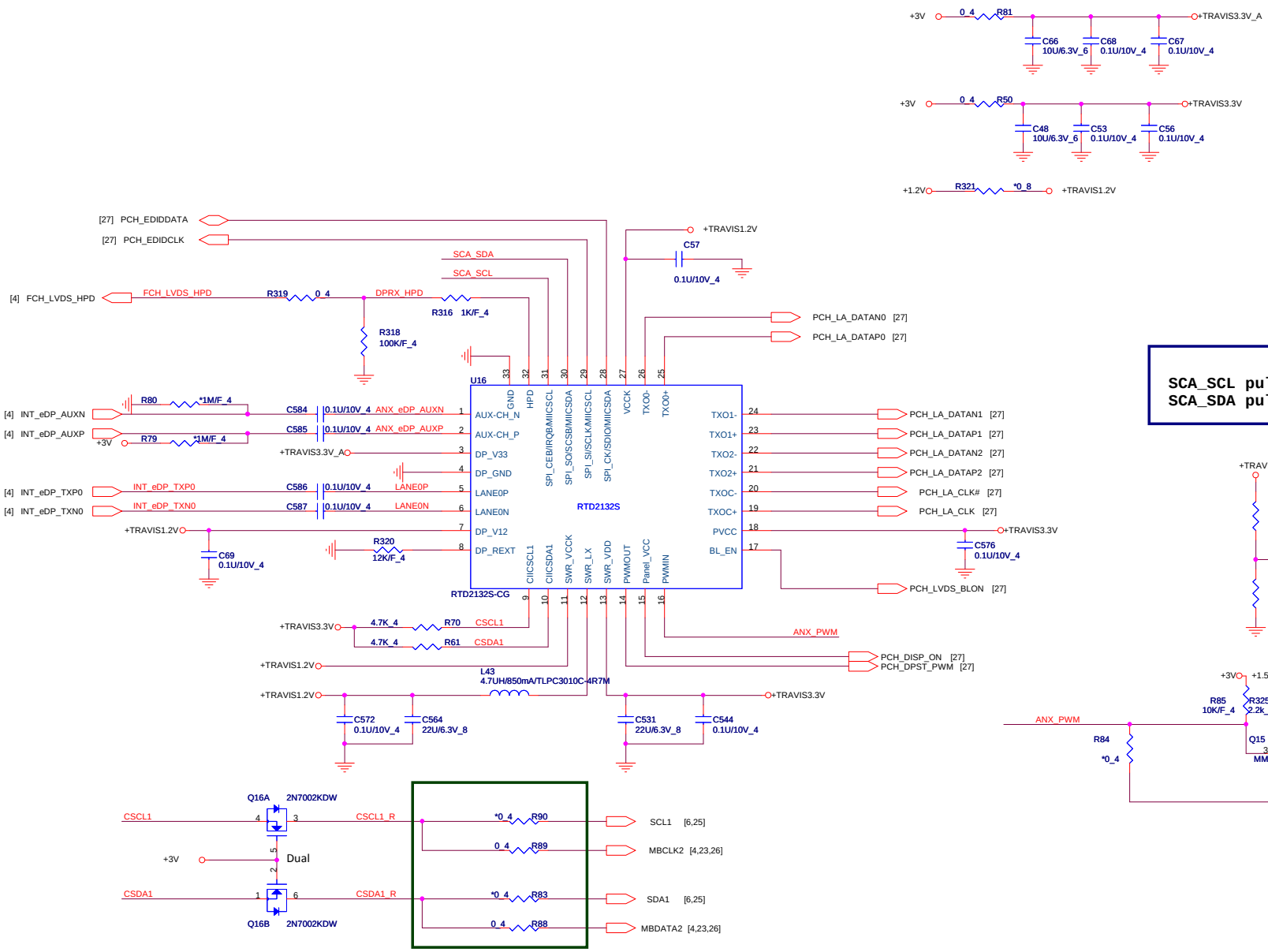


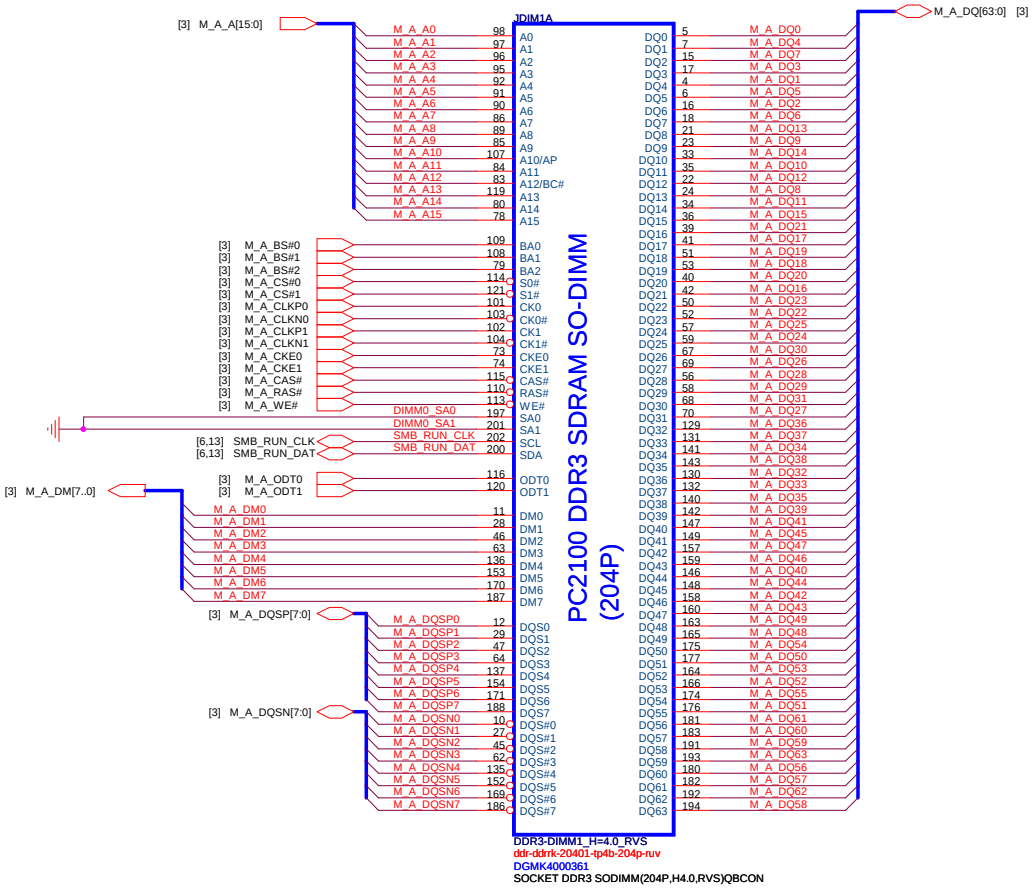
NB5

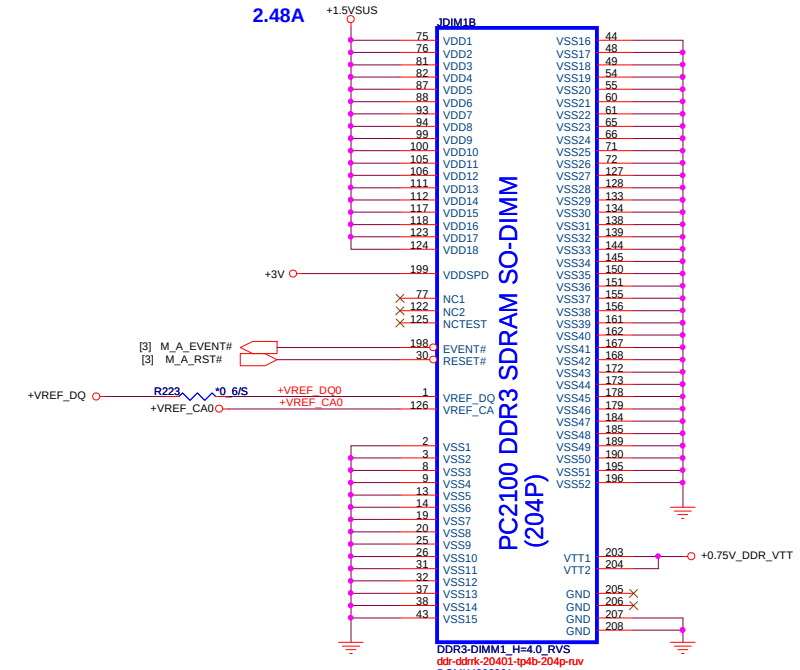
PROJECT : U56
Quanta Computer Inc.

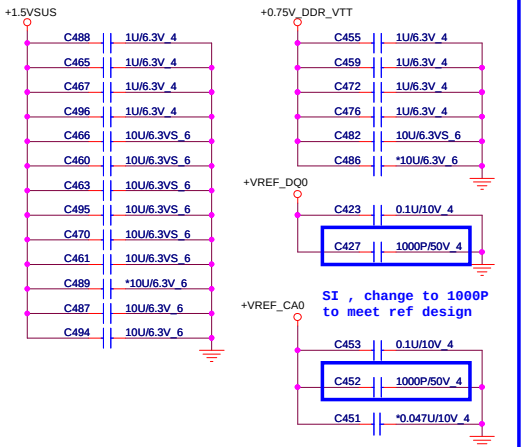
Size	Document Number	Rev
Custom	Hudson-M3 STRAP/PWRGD	1A

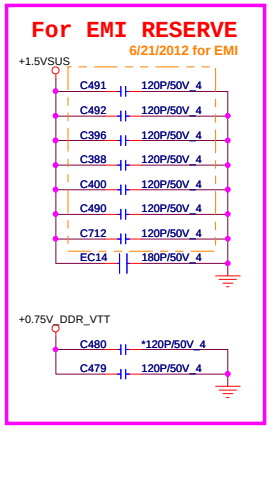
Date: Tuesday, August 07, 2012 Sheet 10 of 39

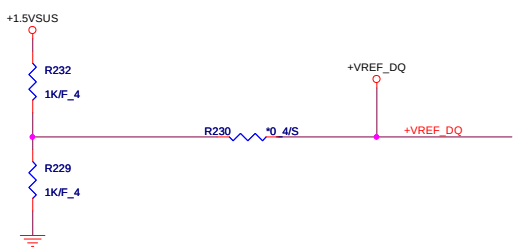

+3V
0_4
R81
+TRAVIS3.3V_A
C66 10U/6.3V_6
C68 0.1U/10V_4
C67 0.1U/10V_4
+3V
0_4
R50
+TRAVIS3.3V
C48 10U/6.3V_6
C53 0.1U/10V_4
C56 0.1U/10V_4
+1.2V
R321
*0_8
+TRAVIS1.2V
[27] PCH_EDIDDATA
[27] PCH_EDIDCLK
SCA_SDA
SCA_SCL
[4] FCH_LVDS_HPD
FCH_LVDS_HPD
R319 0_4
DPRX_HPD
R316 1K/F_4
R318 100K/F_4
+TRAVIS1.2V
C57 0.1U/10V_4
PCH_LA_DATAN0 [27]
PCH_LA_DATAP0 [27]
U16
RTD2132S
AUX-CH_N
AUX-CH_P
DP_V33
DP_GND
LANE0P
LANE0N
DP_V12
DP_REXT
TXO1-
TXO1+
TXO2-
TXO2+
TXOC-
TXOC+
PVCC
BL_EN
PCH_LA_DATAN1 [27]
PCH_LA_DATAP1 [27]
PCH_LA_DATAN2 [27]
PCH_LA_DATAP2 [27]
PCH_LA_CLK# [27]
PCH_LA_CLK [27]
+TRAVIS3.3V
PCH_LVDS_BLON [27]
[4] INT_eDP_AUXN
[4] INT_eDP_AUXP
R80 *1M/F_4
R79 *1M/F_4
+3V
C584 0.1U/10V_4 ANX_eDP_AUXN
C585 0.1U/10V_4 ANX_eDP_AUXP
+TRAVIS3.3V_A
[4] INT_eDP_TXP0
[4] INT_eDP_TXN0
INT_eDP_TXP0
INT_eDP_TXN0
C586 0.1U/10V_4 LANE0P
C587 0.1U/10V_4 LANE0N
+TRAVIS1.2V
C69 0.1U/10V_4
R320 12K/F_4
C576 0.1U/10V_4
RTD2132S-CG
+TRAVIS3.3V
4.7K_4 R70 CSCL1
4.7K_4 R61 CSDA1
+TRAVIS1.2V
L43 4.7UH/850mA/TLPC3010C-4R7M
ANX_PWM
PCH_DISP_ON [27]
PCH_DPST_PWM [27]
+TRAVIS1.2V
+TRAVIS3.3V
C572 0.1U/10V_4
C564 22U/6.3V_8
C531 22U/6.3V_8
C544 0.1U/10V_4
Q16A 2N7002KDW
CSCL1
CSCL1_R
+3V
Dual
CSDA1
CSDA1_R
Q16B 2N7002KDW
*0_4 R90
0_4 R89
*0_4 R83
0_4 R88
SCL1 [6,25]
MBCLK2 [4,23,26]
SDA1 [6,25]
MBDATA2 [4,23,26]
CMC
SCA_SCL pull high => EEPROM mode
SCA_SDA pull low = > EEPROM Free mode
Address=0xA8
+TRAVIS3.3V
+TRAVIS3.3V
+TRAVIS3.3V
R310 *4.7K/F_4
R303 4.7K/F_4
U17
VCC
SDA
SCL
GND
WP
A2
A1
A0
*SGT-M24C64-WMN6TP
C610 *0.1U/10V_4
SCA_SDA
SCA_SCL
R305 4.7K/F_4
Close to Pin8
+3V
+1.5V
R85 10K/F_4
R325 2.2k_4
ANX_PWM
R84 *0_4
Q15 MMBT3904
APU_BLPWM [4]
PWM_VADJ [26]
EE PROM R3054,R3056
EC OPTION R3055,R3057
PROJECT : U56
Quanta Computer Inc.
NB5
Size Custom
Document Number RTD2132S
Rev 1A
Date: Thursday, August 09, 2012
Sheet 11 of 39







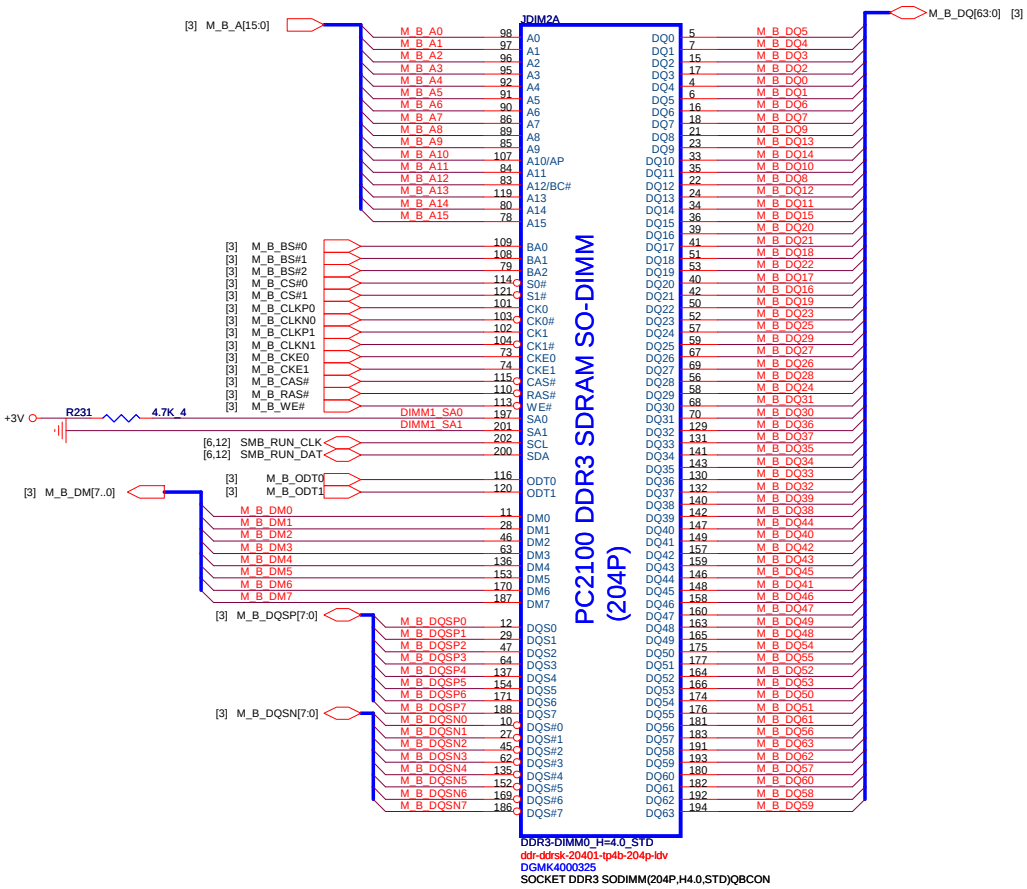


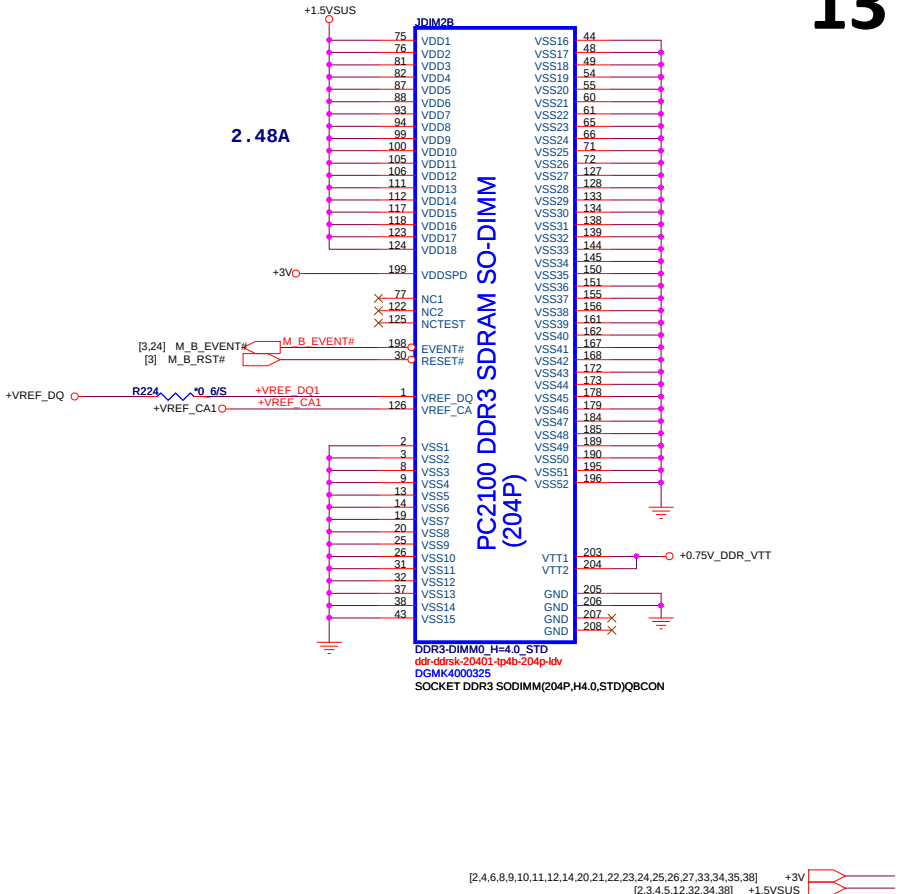


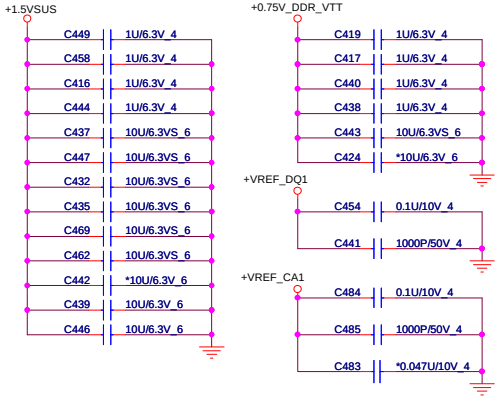
PROJECT : U56
Quanta Computer Inc.

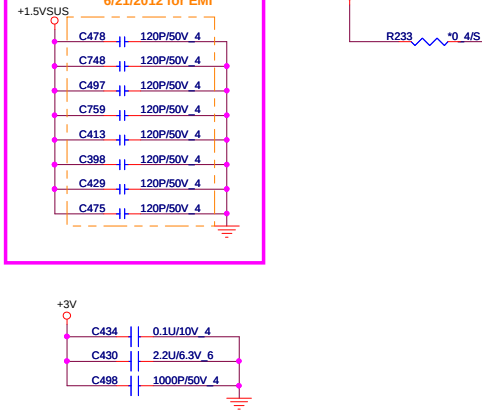
NB5

Size	Document Number	Rev
Custom	System Memory 1/2 (5.2H)	1A
Date: Wednesday, August 08, 2012	Sheet 12of 39	



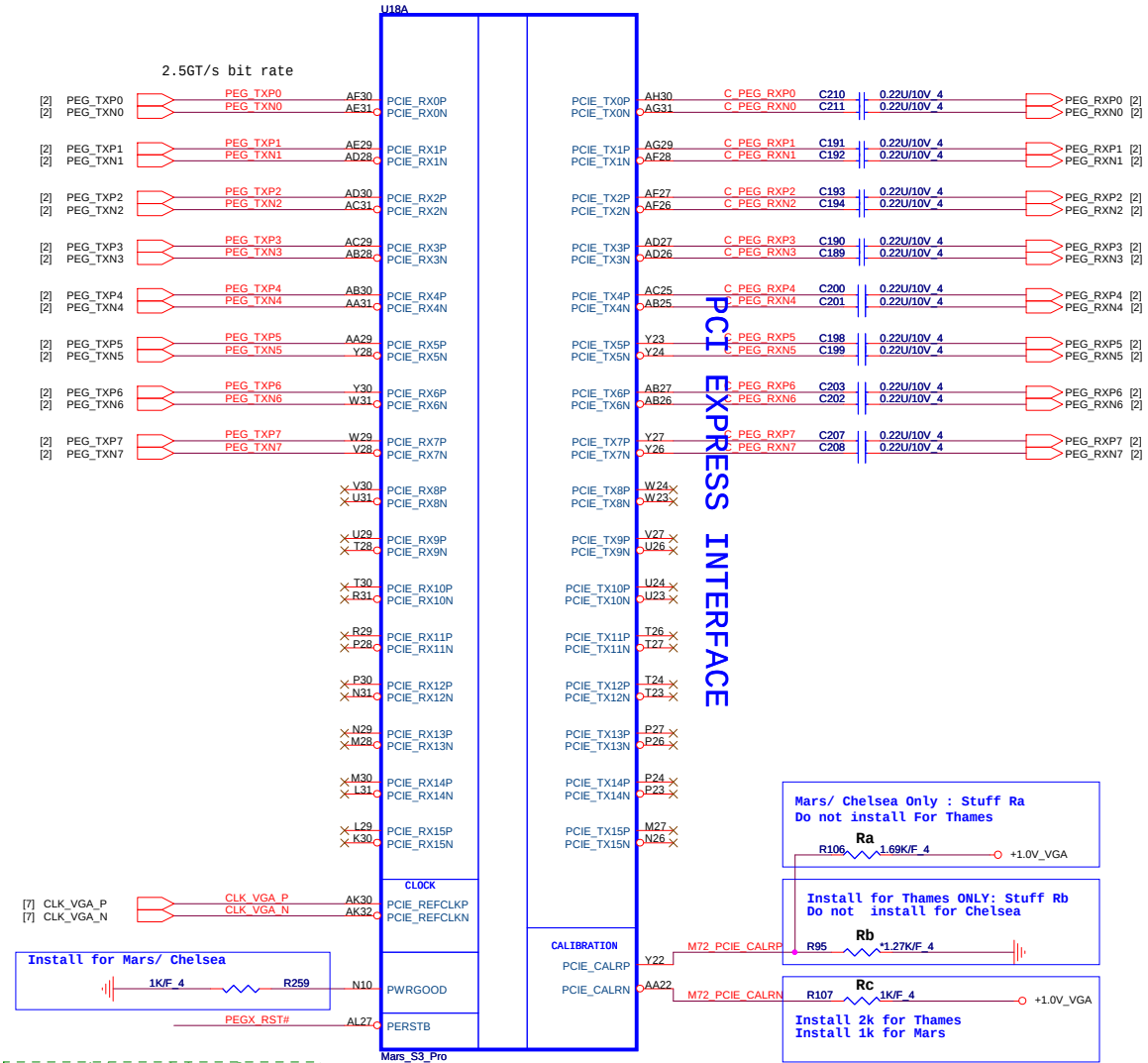




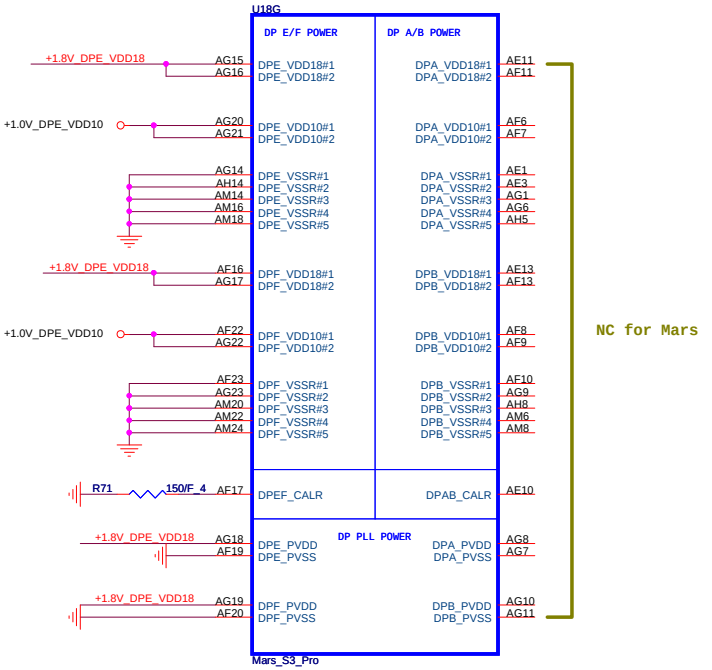


NB5	PROJECT : U56 Quanta Computer Inc.		
	Size: Custom	Document Number: System Memory 2/2 (9.2H)	Rev: 1A
	Date: Tuesday, August 07, 2012	Sheet 13 of 39	

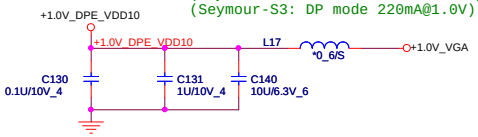
PCI EXPRESS INTERFACE



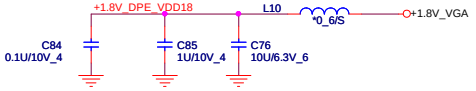
	Chelsea/MARS	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K



(Seymour-S3: LVDS mode 240mA@1.0V)
(Seymour-S3: DP mode 220mA@1.0V)



(Seymour-S3: LVDS mode 300mA@1.8V)
(Seymour-S3: DP mode 300mA@1.8V)



+1.0V_VGA [15,17,34]
+1.8V_VGA [15,17,35]

NB5	PROJECT : U56 Quanta Computer Inc.	
Size: Custom	Document Number: Mars S3 PCIE_Interface	Rev: 1A
Date: Tuesday, August 07, 2012	Sheet 14 of 39	

Thermal Solution(Close to GPU)

Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

GPIO30	GPIO12	GPIO16	GPIO20	GPIO15	Thames XT
PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	PWRCNTL0	V-CORE
0	0	0	0	0	1.0V
0	0	0	0	1	0.9V
0	0	0	1	0	0.875V
0	0	0	1	1	0.85V
0	0	1	0	0	0.8V
0	0	1	0	1	0.75V

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

PS_3[3:1]	Vendor	Type	Vendor P/N	R68	R76
000	Hynix- D (VEGA)	128Mx16 *4, 900Mhz	H5TQ1G63DFR-11C	NC	4.75K
001	Micron- G die	128Mx16 *4, 900Mhz	MT41J64M16JT-107:G	8.45K	2K
010	Samsung- G die	128Mx16 *4, 900Mhz	K4W1G1646G-BC11	4.53K	2K

BIT5 => BIT0

PS0	=>	11001
PS1	=>	01000
PS2	=>	00000
PS3	=>	11000

Fo Mars/ Chelsea
Change La, Lb
Bead to 0 ohm

For Thems: La,Lb:
CX8PG471000/BLM18PG471SN1D/1A_6

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

NC for Mars

SI , add R298 for PP table update

GPIO29, 30 are NC on Thems/ whistler/ Seymour

Mars / Chelsea : AVSSN must be short to gnd

Thames INSTALL Ra,Rb.
Do not install for Mars/ Chelsea
PS_0 should be tied to GND on Thames

For AMD tuning timing purpose

For Int Clk 27Mhz

Reserve for Power Play

For Mars: Stuff Ra only=> VDDC 1.1V
For Thems: Stuff Ra, Rb=> VDDC 1.0V

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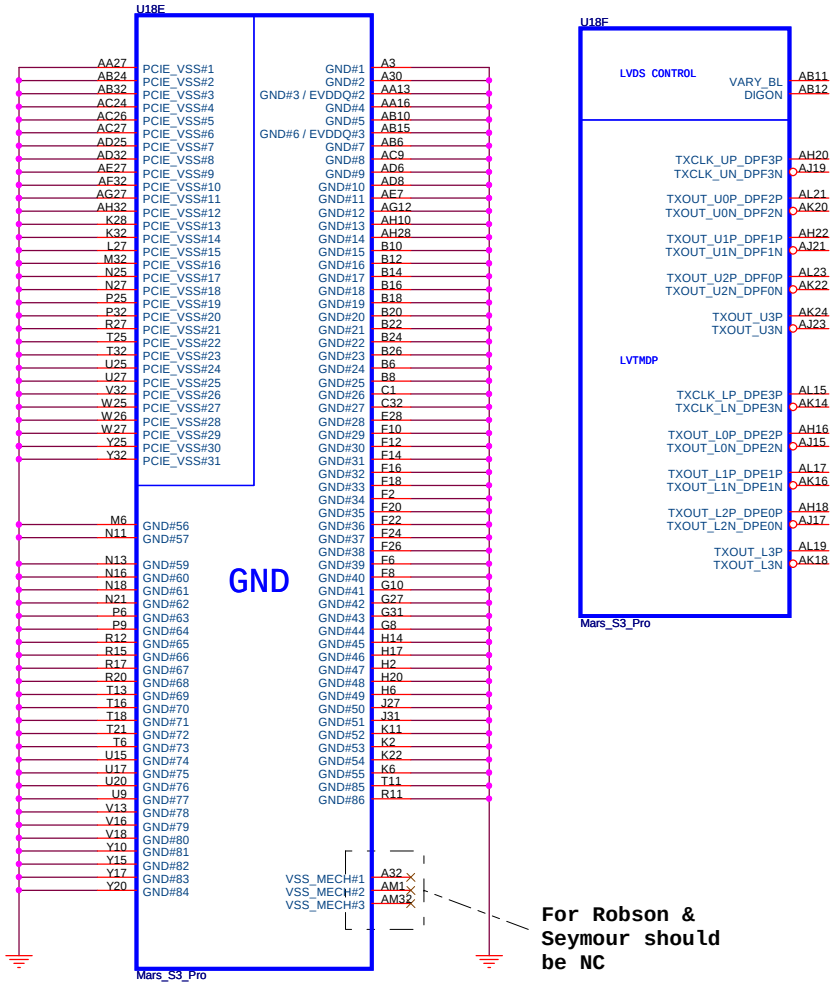


For Robson & Seymour should be NC

CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

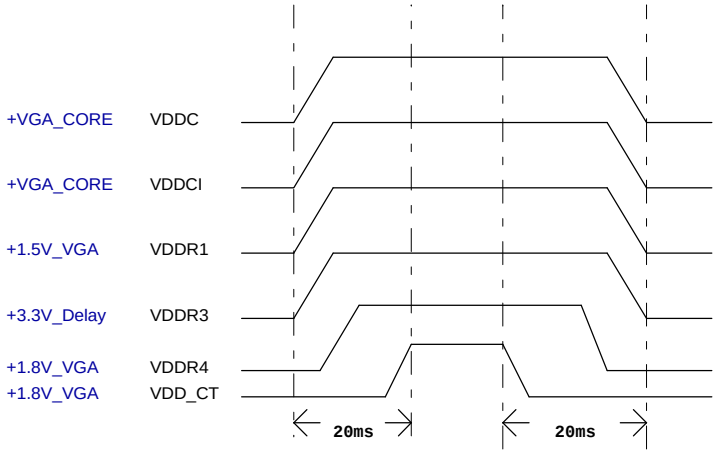
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0 X
RSVD RSVD	GPIO2 GPIO8	RESERVED RESERVED	0 0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

Power Up/Down Sequence

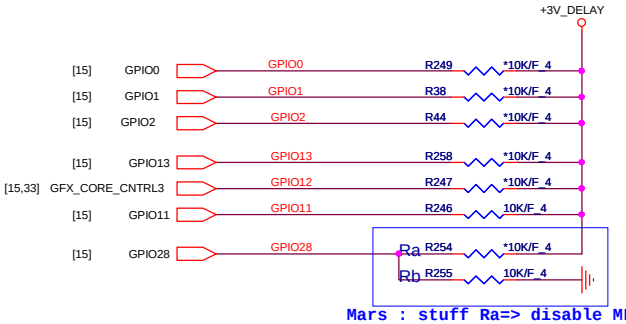


Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

+3V_DELAY [15,17]



Mars : stuff Ra=> disable MLPS
stuff Rb=> enable MLPS

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+1.5V_VGA [18,19,34]
+1.8V_VGA [14,15,35]
+1.0V_VGA [14,15,34]
+VGA_CORE [33,34]
+3V [2,4,6,8,9,10,11,12,13,14,20,21,22,23,24,25,26,27,33,34,35,38]
+5V [20,22,23,24,25,27,38]

U18D

MEM I/O
LEVEL TRANSLATION
M93-S3/M92-S2 I/O
MEM CLK
PLL
BACK BIAS
Mars_S3_Pro

PCIE
CORE
POWER
ISOLATED CORE I/O

+1.5V_VGA
1.5V (DDR3, MVDDQ = 1.5V@1.2A)
C60 2.2U/6.3V_4
C87 2.2U/6.3V_4
C137 2.2U/6.3V_4
C101 2.2U/6.3V_4
C143 2.2U/6.3V_4
C75 2.2U/6.3V_4
C638 10U/6.3VS_6
C59 10U/6.3VS_6
C538 10U/6.3VS_6
C533 10U/6.3VS_6
C552 10U/6.3VS_6
C184 0.1U/10V_4
C92 0.1U/10V_4
C129 0.1U/10V_4
C141 0.1U/10V_4

+1.8V_VGA
VDDC_CT: 1.8V @250mA
L45 0_6
+1.8V_VDD_CT
C596 10U/6.3VS_6
C598 1U/10V_4
C139 1U/10V_4
C597 1U/10V_4
C138 0.1U/10V_4
+3V_DELAY

+3V_VGA
VDDR3 : 3.3V @ 60mA
L16 *0_6/S
C113 1U/10V_4
C102 1U/10V_4
C123 1U/10V_4
C521 10U/6.3VS_6

+1.8V_VGA
VDDR4 : 1.8V @ 300mA
+VDDR4
L7 0_6
C35 10U/6.3VS_6
C86 1U/10V_4
C77 0.1U/10V_4
TP17

For Seymour,PCIE_PVDD is PCIE_VDDR

1.8V(75mA MPV18)
+1.8V_VGA
L38 BLM18PG181SN1D(180,1.5A)_6
MPV18
C519 1U/10V_4
C522 0.1U/10V_4

1.8V(50mA SPV18)
+1.8V_VGA
L9 PBY160808T-121Y-N(120,2.5A)
SPV18
C45 1U/10V_4
C41 0.1U/10V_4

1.0V_VGA(100mA SPV10)
+1.0V_VGA
L8 PBY160808T-121Y-N(120,2.5A)
+1.0V_VGA_SPV10
C39 10U/6.3VS_6
C46 0.1U/10V_4
C42 1U/10V_4

PCIE_PVDD → +1.8V_VGA
Mars NC

+1.0V_PCIE_VDDC
1.0V(2.0A)
L19 *0_8/S
C144 1U/10V_4
C146 1U/10V_4
C147 1U/10V_4
C145 1U/10V_4
C149 1U/10V_4
C167 1U/10V_4
C171 1U/10V_4
C169 10U/6.3VS_6

+1.0V_VGA

VDDC+VDDCI
0.85~1.1V(14.2A peak)(Ripple < 87.2mV)
+VGA_CORE
C526 1U/10V_4
C549 1U/10V_4
C88 1U/10V_4
C105 1U/10V_4
C577 1U/10V_4
C98 1U/10V_4
C93 1U/10V_4
C530 10U/6.3VS_6
C78 1U/10V_4
C94 2.2U/6.3V_4
C63 1U/10V_4
C599 10U/6.3V_8
C568 1U/10V_4
C89 1U/10V_4
C103 1U/10V_4
C121 330U_2.5V_3528
C104 1U/10V_4
C64 2.2U/6.3V_4
C96 1U/10V_4
C573 1U/10V_4
C62 1U/10V_4
C91 1U/10V_4
C764 *330U_2.5V_3528

+1.0V_PCIE_VDDC
C527 10U/6.3VS_6
C540 10U/6.3VS_6
C583 10U/6.3VS_6
C557 10U/6.3VS_6
C537 10U/6.3VS_6
C566 10U/6.3VS_6

R21 and U21
Must always be connected to PCIE_VDDC for Mars

+VGA_CORE R462 *0_8 +VDDCI

0.95V~1.1V(2A VDDCI)
+VDDCI
C111 1U/10V_4
C126 1U/10V_4
C118 1U/10V_4
C97 10U/6.3VS_6
C115 10U/6.3VS_6
C116 10U/6.3VS_6

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[19] VMA_ODT0 → VMA_ODT0
[19] VMA_ODT1 → VMA_ODT1
[19] VMA_RAS0# → VMA_RAS0#
[19] VMA_RAS1# → VMA_RAS1#
[19] VMA_CAS0# → VMA_CAS0#
[19] VMA_CAS1# → VMA_CAS1#
[19] VMA_WE0# → VMA_WE0#
[19] VMA_WE1# → VMA_WE1#
[19] VMA_CS0# → VMA_CS0#
[19] VMA_CS1# → VMA_CS1#
[19] VMA_CKE0 → VMA_CKE0
[19] VMA_CKE1 → VMA_CKE1
[19] VMA_CLK0 → VMA_CLK0
[19] VMA_CLK0# → VMA_CLK0#
[19] VMA_CLK1 → VMA_CLK1
[19] VMA_CLK1# → VMA_CLK1#
[19] VMA_WDQS[7..0] → VMA_WDQS[7..0]
[19] VMA_RDQS[7..0] → VMA_RDQS[7..0]
[19] VMA_DM[7..0] → VMA_DM[7..0]
[19] VMA_DQ[63..0] → VMA_DQ[63..0]
[19] VMA_MA[13..0] → VMA_MA[13..0]
[19] VMA_BA0 → VMA_BA0
[19] VMA_BA1 → VMA_BA1
[19] VMA_BA2 → VMA_BA2

support 1Gbit VRAM (64M X 16)

U18C

MEMORY INTERFACE

VMA_DQ0	K27	DQA_0	MAA_0	K17	VMA_MA0
VMA_DQ1	J29	DQA_1	MAA_1	J20	VMA_MA1
VMA_DQ2	H30	DQA_2	MAA_2	H23	VMA_MA2
VMA_DQ3	H32	DQA_3	MAA_3	G23	VMA_MA3
VMA_DQ4	G29	DQA_4	MAA_4	G24	VMA_MA4
VMA_DQ5	F28	DQA_5	MAA_5	H24	VMA_MA5
VMA_DQ6	F32	DQA_6	MAA_6	J19	VMA_MA6
VMA_DQ7	F30	DQA_7	MAA_7	K19	VMA_MA7
VMA_DQ8	C30	DQA_8	MAA_8	J14	VMA_MA8
VMA_DQ9	F27	DQA_9	MAA_9	K14	VMA_MA9
VMA_DQ10	A28	DQA_10	MAA_10	J11	VMA_MA10
VMA_DQ11	C28	DQA_11	MAA_11	J13	VMA_MA11
VMA_DQ12	E27	DQA_12	MAA_12	H11	VMA_MA12
VMA_DQ13	G26	DQA_13	MAA_13/BA2	G11	VMA_BA2
VMA_DQ14	D26	DQA_14	MAA_14/BA0	J16	VMA_BA0
VMA_DQ15	F25	DQA_15	MAA_15/BA1	L15	VMA_BA1
VMA_DQ16	A25	DQA_16			
VMA_DQ17	C25	DQA_17	DQMA_0	E32	VMA_DM0
VMA_DQ18	E25	DQA_18	DQMA_1	E30	VMA_DM1
VMA_DQ19	D24	DQA_19	DQMA_2	A21	VMA_DM2
VMA_DQ20	E23	DQA_20	DQMA_3	C21	VMA_DM3
VMA_DQ21	F23	DQA_21	DQMA_4	E13	VMA_DM4
VMA_DQ22	D22	DQA_22	DQMA_5	D12	VMA_DM5
VMA_DQ23	F21	DQA_23	DQMA_6	E3	VMA_DM6
VMA_DQ24	E21	DQA_24	DQMA_7	F4	VMA_DM7
VMA_DQ25	D20	DQA_25			
VMA_DQ26	F19	DQA_26	RDQSA_0	H28	VMA_RDQS0
VMA_DQ27	A19	DQA_27	RDQSA_1	C27	VMA_RDQS1
VMA_DQ28	D18	DQA_28	RDQSA_2	A23	VMA_RDQS2
VMA_DQ29	F17	DQA_29	RDQSA_3	E19	VMA_RDQS3
VMA_DQ30	A17	DQA_30	RDQSA_4	E15	VMA_RDQS4
VMA_DQ31	C17	DQA_31	RDQSA_5	D10	VMA_RDQS5
VMA_DQ32	E17	DQA_32	RDQSA_6	D6	VMA_RDQS6
VMA_DQ33	D16	DQA_33	RDQSA_7	G5	VMA_RDQS7
VMA_DQ34	E15	DQA_34			
VMA_DQ35	A15	DQA_35	WDQSA_0	H27	VMA_WDQS0
VMA_DQ36	D14	DQA_36	WDQSA_1	A27	VMA_WDQS1
VMA_DQ37	F13	DQA_37	WDQSA_2	C23	VMA_WDQS2
VMA_DQ38	A13	DQA_38	WDQSA_3	C19	VMA_WDQS3
VMA_DQ39	C13	DQA_39	WDQSA_4	C15	VMA_WDQS4
VMA_DQ40	E11	DQA_40	WDQSA_5	E9	VMA_WDQS5
VMA_DQ41	A11	DQA_41	WDQSA_6	C5	VMA_WDQS6
VMA_DQ42	C11	DQA_42	WDQSA_7	H4	VMA_WDQS7
VMA_DQ43	F11	DQA_43			
VMA_DQ44	A9	DQA_44	ODTA0	L18	VMA_ODT0
VMA_DQ45	C9	DQA_45	ODTA1	K16	VMA_ODT1
VMA_DQ46	F9	DQA_46			
VMA_DQ47	D8	DQA_47	CLKA0	H26	VMA_CLK0
VMA_DQ48	E7	DQA_48	CLKA0B	H25	VMA_CLK0#
VMA_DQ49	A7	DQA_49			
VMA_DQ50	C7	DQA_50	CLKA1	G9	VMA_CLK1
VMA_DQ51	F7	DQA_51	CLKA1B	H9	VMA_CLK1#
VMA_DQ52	A5	DQA_52			
VMA_DQ53	E5	DQA_53	RASA0B	G22	VMA_RAS0#
VMA_DQ54	C3	DQA_54	RASA1B	G17	VMA_RAS1#
VMA_DQ55	E1	DQA_55			
VMA_DQ56	G7	DQA_56	CASA0B	G19	VMA_CAS0#
VMA_DQ57	G6	DQA_57	CASA1B	G16	VMA_CAS1#
VMA_DQ58	G1	DQA_58			
VMA_DQ59	G3	DQA_59	CSA0B_0	H22	VMA_CS0#
VMA_DQ60	J6	DQA_60	CSA0B_1	J22	
VMA_DQ61	J1	DQA_61			
VMA_DQ62	J3	DQA_62	CSA1B_0	G13	VMA_CS1#
VMA_DQ63	J5	DQA_63	CSA1B_1	K13	
	K26	MVREFDA	CKEA0	K20	VMA_CKE0
	J26	MVREFSA	CKEA1	J17	VMA_CKE1
			WEA0B	G25	VMA_WE0#
	J25	MEM_CALRN0	WEA1B	H10	VMA_WE1#
	K7	NC/TESTEN#2			
	J8	MEM_CALRP1/DPC_CALR	PX_EN	AB16	PX_EN → TP86
	K25	MEM_CALRP0	RSVD#2	G14	
			RSVD#3	G20	VMA_MA13
DRAM_RST	L10	DRAM_RST			
CLKTESTA	K8	CLKTESTA			
CLKTESTB	L7	CLKTESTB			

Mars_S3_Pro

+1.5V_VGA
R111 40.2/F_4
MVREFD
C177 0.1U/10V_4
R112 100/F_4
+1.5V_VGA
R113 40.2/F_4
MVREFS
C179 0.1U/10V_4
R114 100/F_4

+1.5V_VGA
Ra R108 *243/F_4
Rb R248 1K/F_4
Rc R35 *150/F_4 Note 2
Rd R109 120/F_4 Note 1

Ra non-stuff
Rb 1K ohm
Rc non-stuff
Rd 120 ohm
for Mars

C44 *0.1U/10V_4
C524 *0.1U/10V_4
R39 *51.1/F_4
R262 *51.1/F_4

route 50ohms
single-ended/100ohms diff
and keep short

From GPU
25mm (max) 5mm (max) 25mm (max)
DRAM_RST R20 10/F_4 R21 51/F_4 DRAM_RST_M → DRAM_RST_M [19]
R13 4.99K/F_4
C25 120P/50V_4

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

+1.5V_VGA [17,19,34]

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512M/1G DDR3

[18] VMA_MA[13..0]
[18] VMA_DM[7..0]
VMA_MA[13..0]
[18] VMA_DQ[63..0]
[18] VMA_WDQS[7..0]
[18] VMA_RDQS[7..0]

U5 / U19 / U3 / U13 — 100-BALL SDRAM DDR3 — H5TQ4G63MFR-11C

Should be 240 Ohms +-1%

R115 243/F_4 (U5) · R326 243/F_4 (U19) · R63 243/F_4 (U3) · R242 243/F_4 (U13)

+1.5V_VGA

R338 4.99K/F_4 · R328 4.99K/F_4 · R339 4.99K/F_4 · R327 4.99K/F_4 · C670 0.1U/10V_4 · C617 0.1U/10V_4 · VREFC_VMA1 · VREFD_VMA1

R330 4.99K/F_4 · R119 4.99K/F_4 · R329 4.99K/F_4 · R118 4.99K/F_4 · C619 0.1U/10V_4 · C662 0.1U/10V_4 · VREFC_VMA2 · VREFD_VMA2

R62 4.99K/F_4 · R23 4.99K/F_4 · R64 4.99K/F_4 · R22 4.99K/F_4 · C70 0.1U/10V_4 · C26 0.1U/10V_4 · VREFC_VMA3 · VREFD_VMA3

R243 4.99K/F_4 · R308 4.99K/F_4 · R244 4.99K/F_4 · R307 4.99K/F_4 · C517 0.1U/10V_4 · C571 0.1U/10V_4 · VREFC_VMA4 · VREFD_VMA4

+1.5V_VGA [17,18,34]

VMA_CLK0 · R117 56.2/F_4 · VMA_CLK0_COMM · C187 0.01U/25V_4 · R116 56.2/F_4 · VMA_CLK0# · VMA_CLK1 · R25 56.2/F_4 · VMA_CLK1_COMM · C27 0.01U/25V_4 · R24 56.2/F_4 · VMA_CLK1#

+1.5V_VGA: C578 1U/6.3V_4 · C47 1U/6.3V_4 · C606 1U/6.3V_4 · C183 1U/6.3V_4 · C72 1U/6.3V_4 · C582 1U/6.3V_4 · C38 1U/6.3V_4 · C666 1U/6.3V_4

+1.5V_VGA: C616 1U/6.3V_4 · C570 1U/6.3V_4 · C614 1U/6.3V_4 · C514 1U/6.3V_4 · C513 1U/6.3V_4 · C669 1U/6.3V_4 · C512 1U/6.3V_4 · C615 1U/6.3V_4

+1.5V_VGA: C569 1U/6.3V_4 · C136 1U/6.3V_4 · C135 1U/6.3V_4 · C133 1U/6.3V_4 · C515 1U/6.3V_4 · C516 1U/6.3V_4 · C132 1U/6.3V_4 · C134 1U/6.3V_4

+1.5V_VGA: C661 1U/6.3V_4 · C667 1U/6.3V_4 · C668 1U/6.3V_4 · C663 1U/6.3V_4 · C664 1U/6.3V_4 · C665 1U/6.3V_4 · C186 1U/6.3V_4 · C185 1U/6.3V_4

+1.5V_VGA: C43 10U/6.3VS_6 · C40 10U/6.3VS_6 · C643 10U/6.3VS_6 · C120 10U/6.3VS_6 · C563 10U/6.3VS_6

+1.5V_VGA: C23 10U/6.3VS_6 · C612 10U/6.3VS_6 · C611 10U/6.3VS_6 · C51 10U/6.3VS_6 · C639 10U/6.3VS_6 · C24 10U/6.3VS_6 · C641 10U/6.3VS_6

	QCI PN
SAM 2G	AKD5MGWT500
HYU 2G	AKD5MGWTW00
SAMSUNG	AKD5EGGT500
HYNIX	AKD5LZWTW02

NB5

PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Mars S3 VRAM(DDR3 BGA96)	1A

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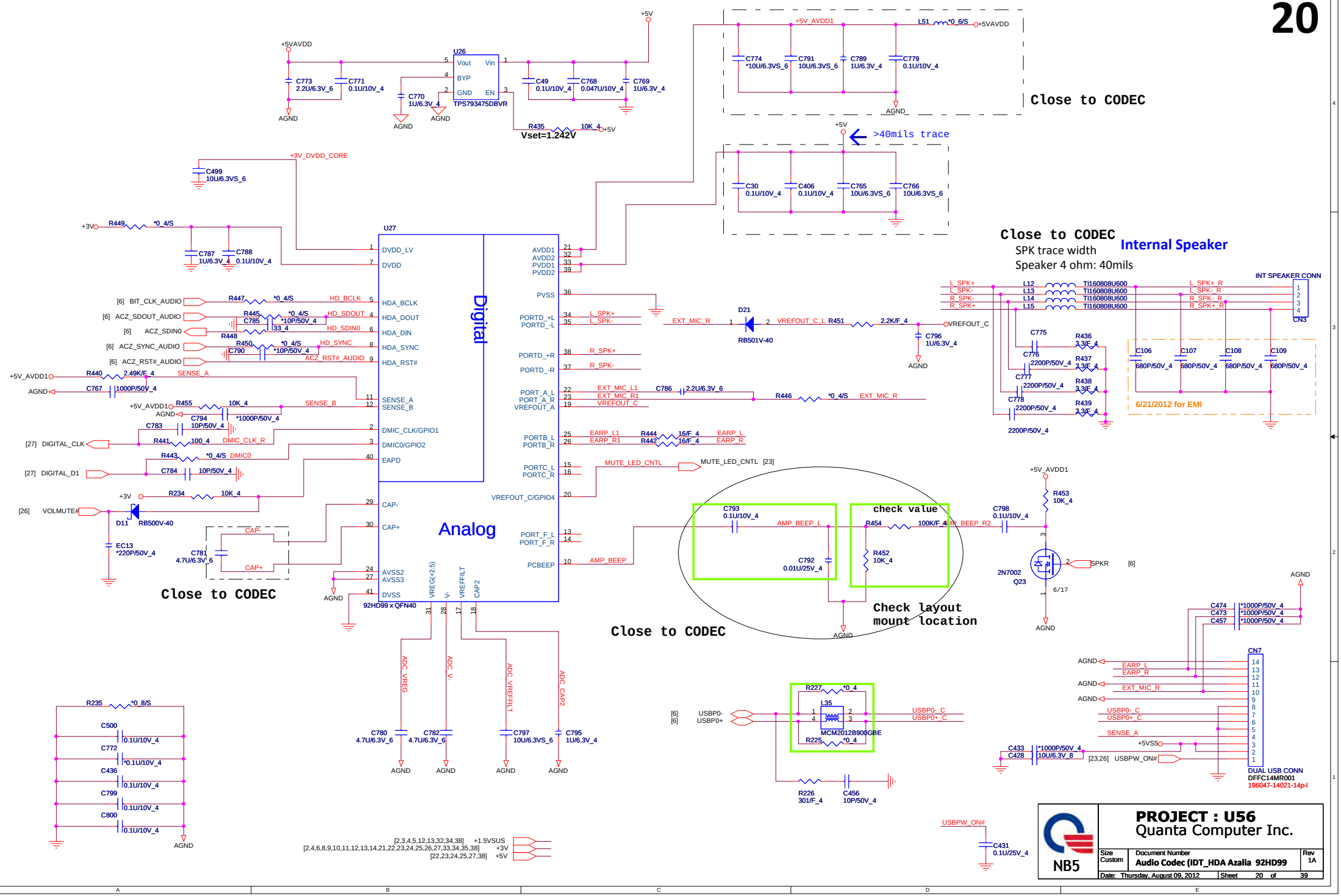
U26
TPS793475DBVR
Vset=1.242V
+5V
+5VAVDD
+5V_AVDD1
+3V_DVDD_CORE
>40mils trace
Close to CODEC
U27
92HD99 x QFN40
Digital
Analog
Close to CODEC
SPK trace width
Speaker 4 ohm: 40mils
Internal Speaker
INT SPEAKER CONN
6/21/2012 for EMI
check value
Check layout
mount location
Close to CODEC
DUAL USB CONN
DFFC14MR001
196047-14021-14p-l
PROJECT : U56
Quanta Computer Inc.
NB5
Audio Codec (IDT_HDA Azalia 92HD99
Date: Thursday, August 09, 2012
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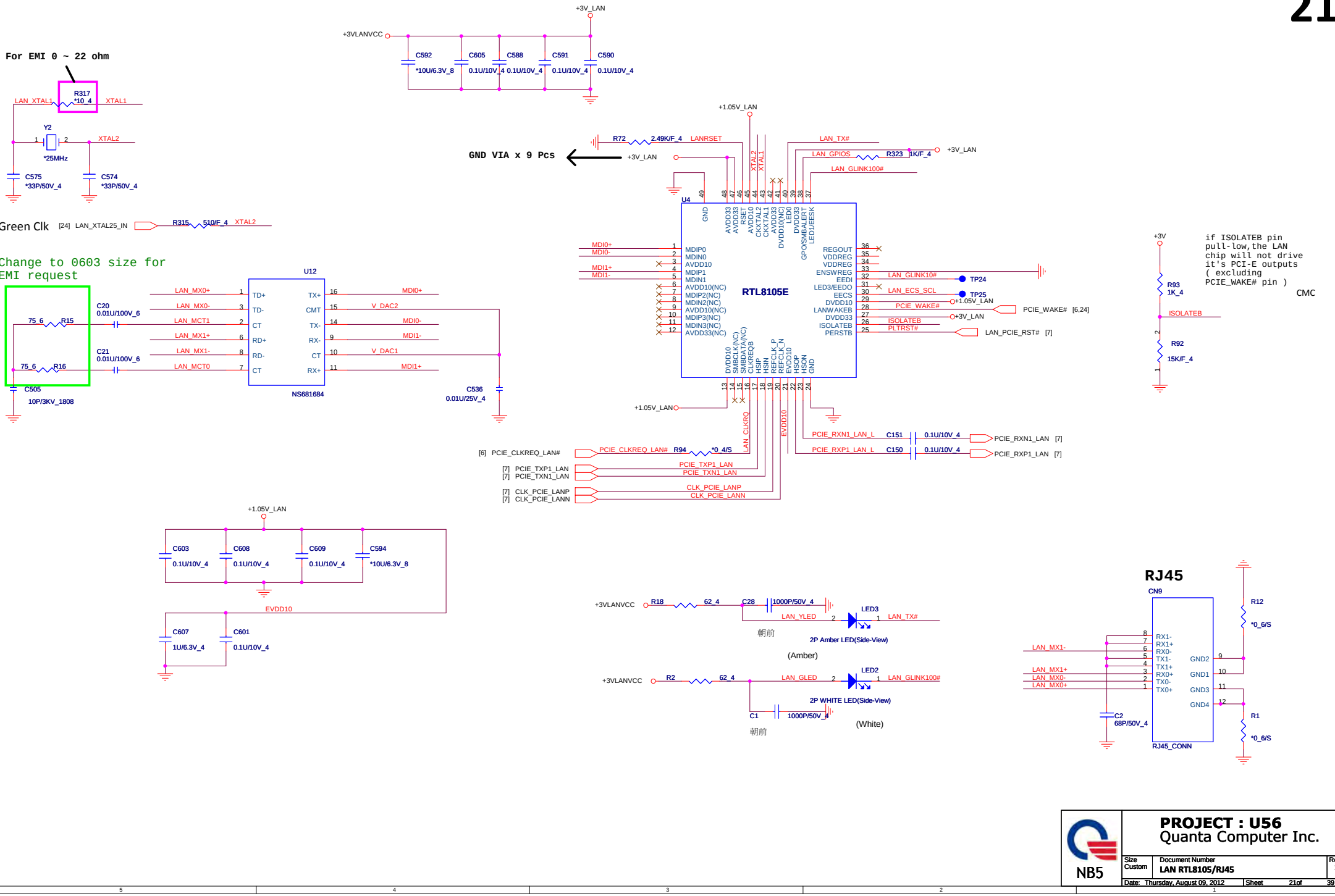

NB5	PROJECT : U56 Quanta Computer Inc.	
Size: Custom	Document Number: LAN RTL8105/RJ45	Rev: 1A
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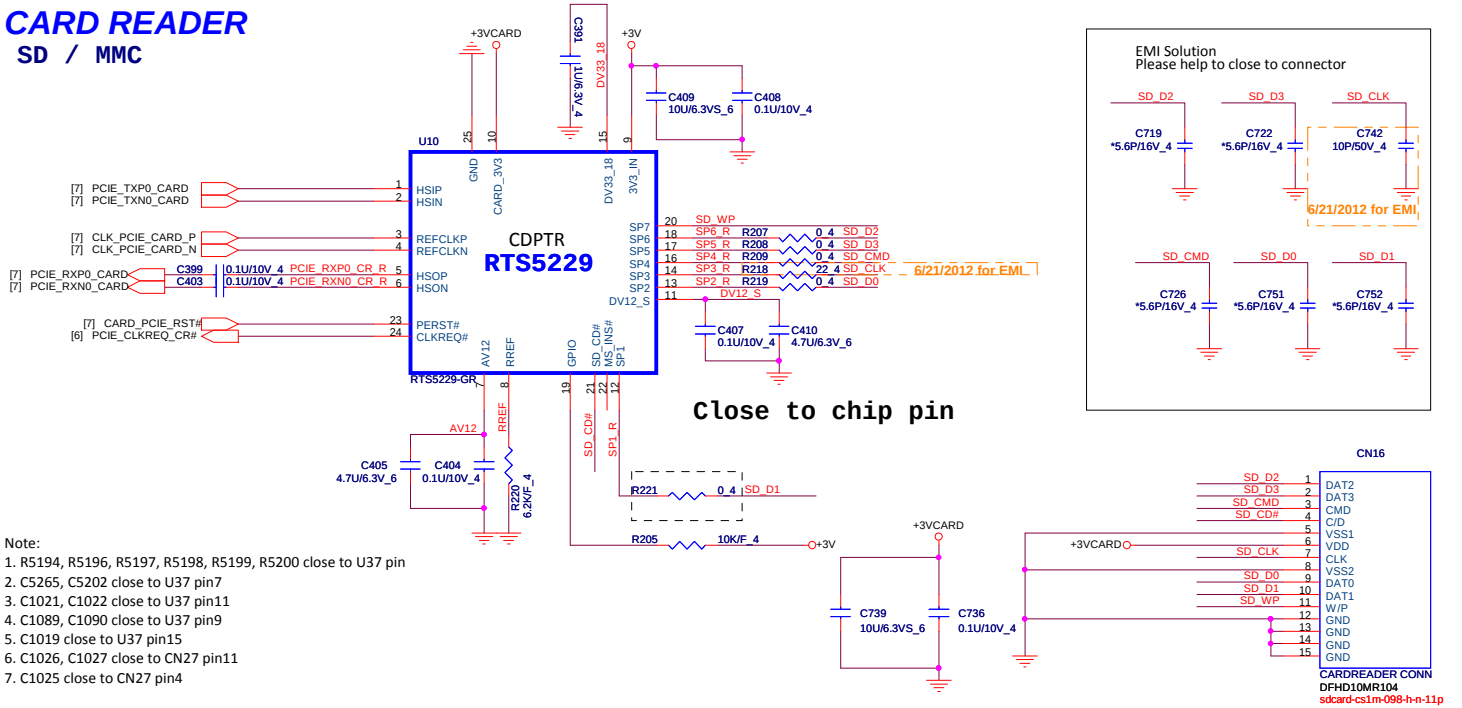
CARD READER
SD / MMC



Note:
1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4

Stitching Cap(each 1" place one cap) EMI/ESD

CPU
H10 *H-TC280BI217D150P2 | H11 *H-TC280BI217D150P2 | H13 *H-TC280BI217D150P2 | H14 *H-TC280BI217D150P2

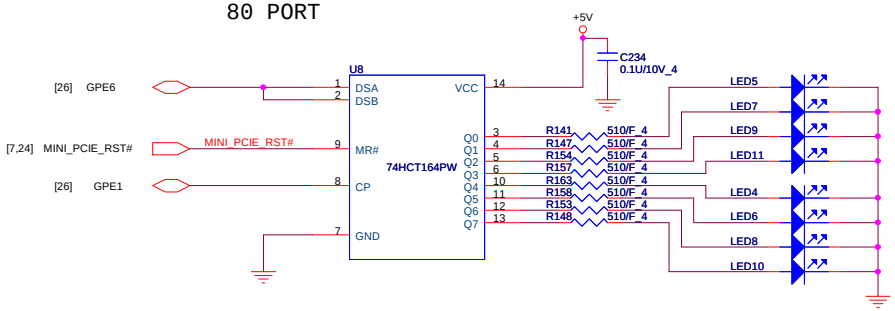
VGA
H4 *H-TC280BI217D150P2 | H8 *H-TC280BI217D150P2 | H9 *H-TC280BI217D150P2

FCH
H28 H-TC217BC122D122PT | H26 H-TC217BC122D122PT

mSATA
H25 *h-tc138bc104d104pt | H24 *h-tc138bc104d104pt

H2 *h-tc315bc118d118p2 | H5 *H-C315D118P2 | H6 *H-TBC315I158D118P2 | H1 *H-C315D106P2
H22 *H-C315D110P2 | H15 *h-c315ic150d110p2 | H23 *H-C315D110P2 | H16 *H-C315D110P2
H12 *SPAD-C315NP | H27 *SPAD-C315NP | H3 *h-tc217bc98d98pt
H19 *H-TSBC315D110P2 | H17 *h-tsbc315ic190d110p2 | H7 *H-TSBC315D106P2 | H18 *h-tc315bsic160d110p2
H21 *H-C158D158N | H20 *H-O142X110D142X110N

80 PORT

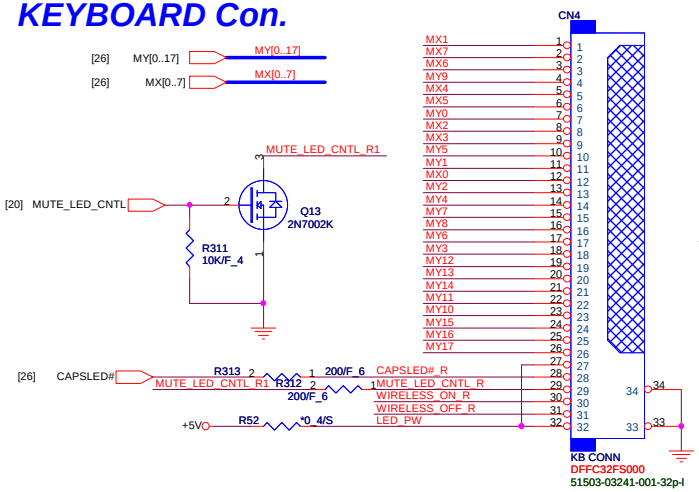


PROJECT : U56
Quanta Computer Inc.

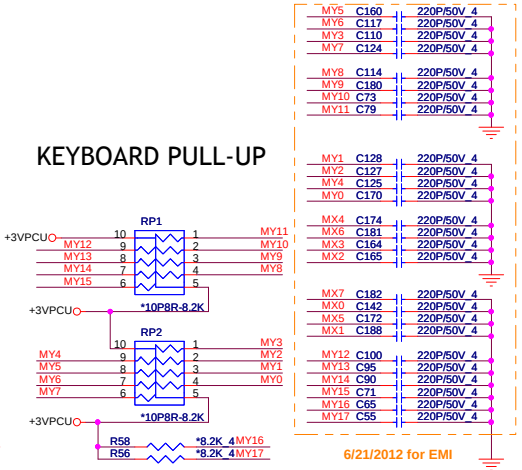
Size	Document Number	Rev
Custom	Card Reader control (RTS5229-GR)	1A
Date: Tuesday, August 07, 2012	Sheet 22of 39	

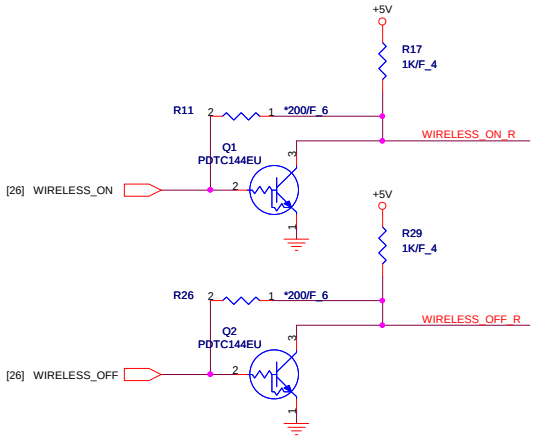
NB5

KEYBOARD Con.

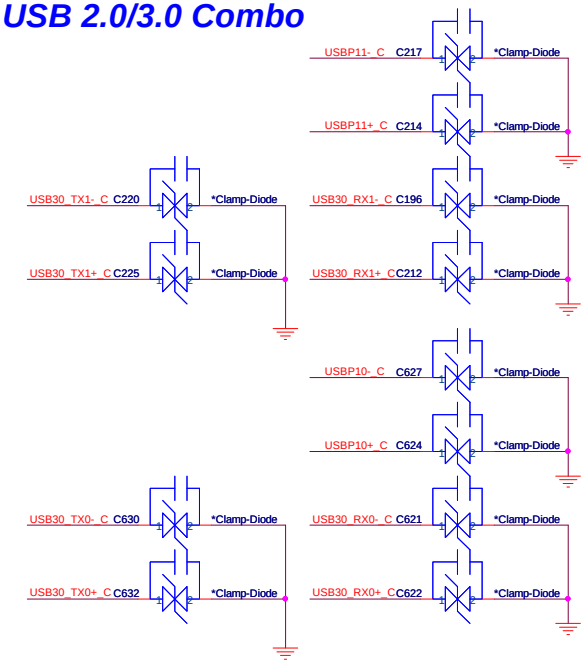


KEYBOARD PULL-UP

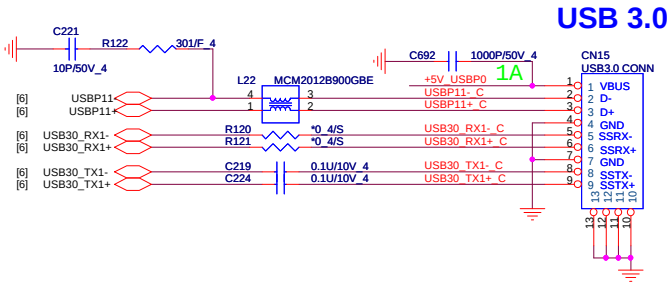




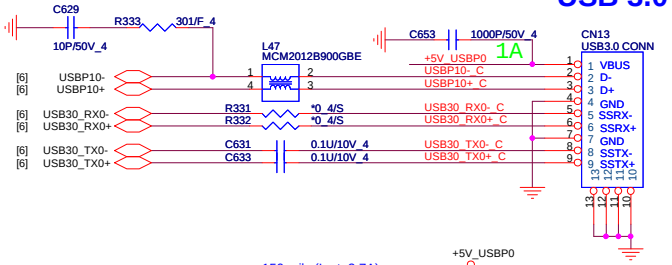
USB 2.0/3.0 Combo

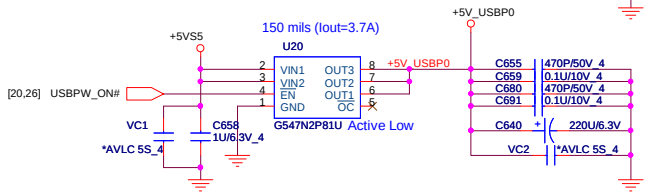


USB 3.0

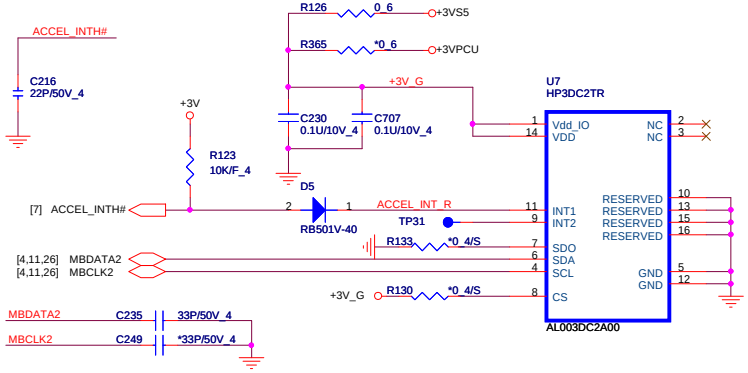


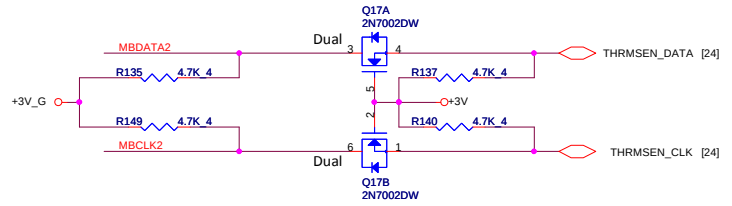
USB 3.0





Accelerometer Sensor





[20,22,29,30,31,32,33,35,36,37,38] +5VS5
[4,7,24,25,26,27,28,29] +3VPCU

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Size	Document Number	Rev
Custom	USB 3.0/KB/Green CLK	1A
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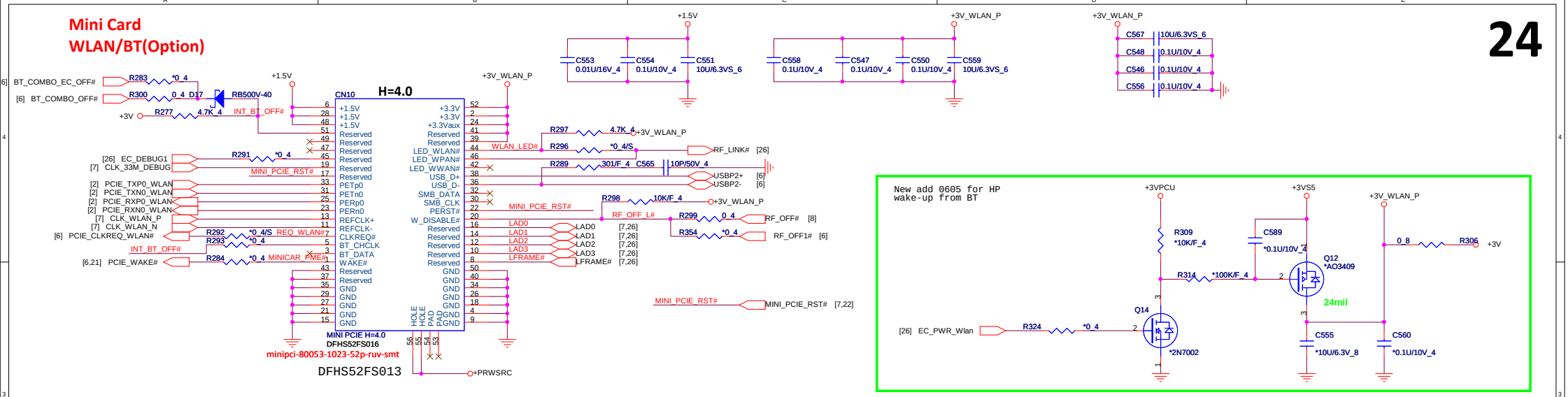
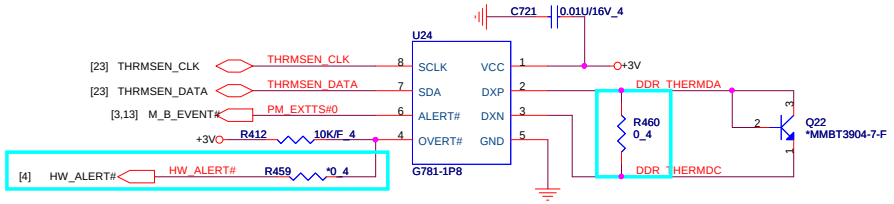
Mini Card
WLAN/BT(Option)



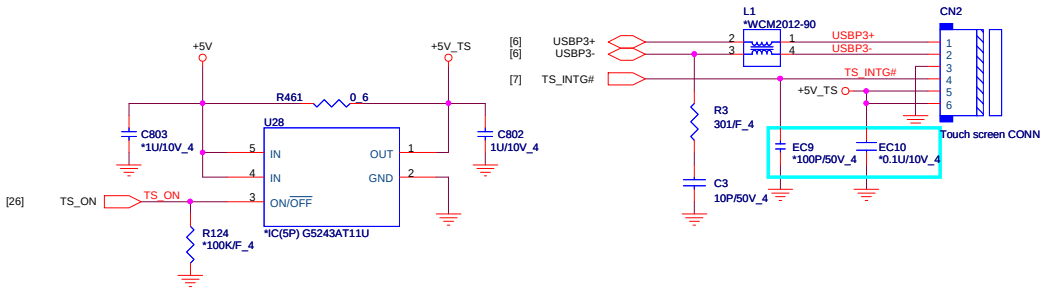
Local Thermal Sensor

DDR3 Thermal Sensor

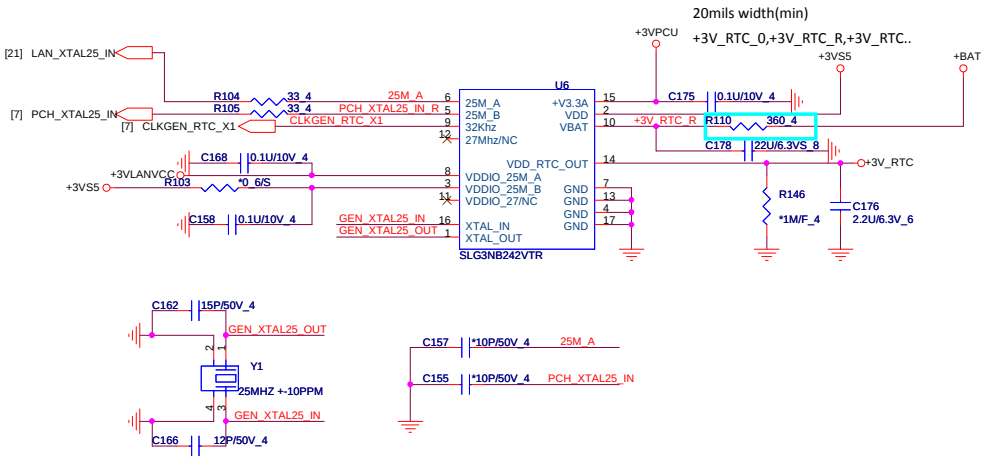


Main:AL000781039	G781-1P8(9Ah)
2nd:AL001412005	EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003	EMC1412-1-ACZL-TR(98h)
2nd:AL000431014	TMP431ADGKR(98h)

Touch screen



Green CLK Circuitry



[6,8,9,10,22,23,26,29,31,33,34,38] +3VS5
[2,4,6,8,9,10,11,12,13,14,20,21,22,23,25,26,27,33,34,35,38] +3V
[20,22,23,25,27,38] +5V
[4,7,23,25,26,27,28,29] +3VPCU
[2,4,11,25,36,38] +1.5V

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Custom	MINI-PCIE/LED	1A
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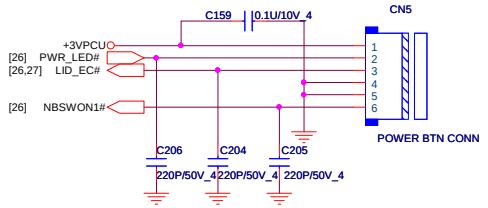
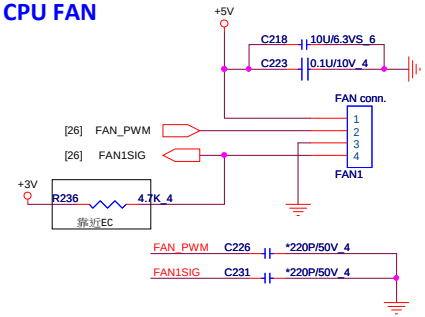
Power Botton Connector

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

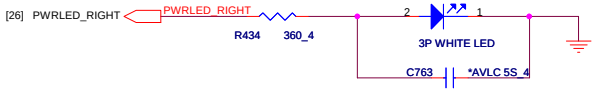


CPU FAN

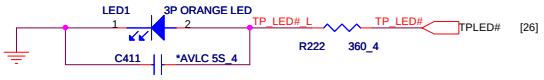


LED Status

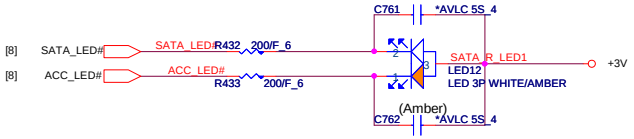
PWR LED



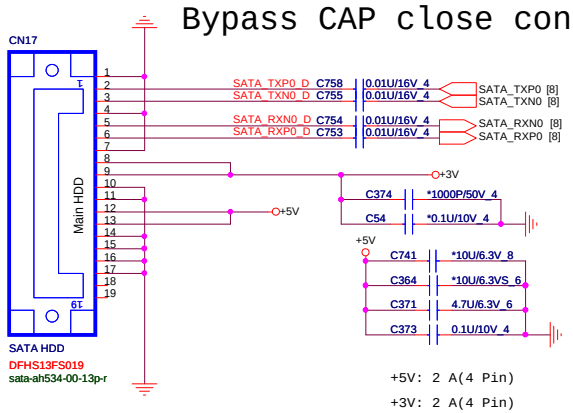
14 "TP LED

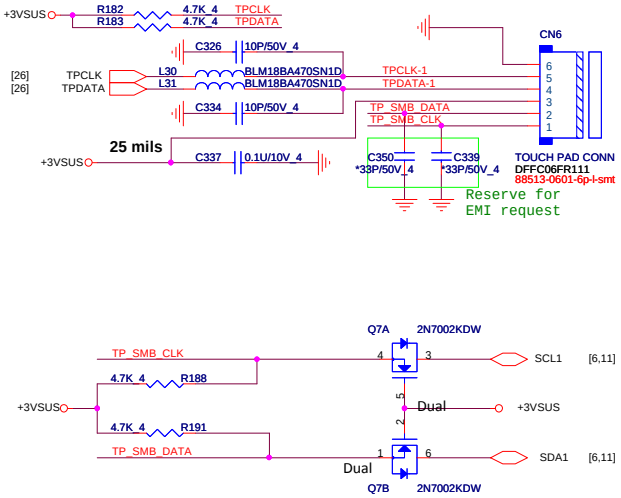


SATA LED

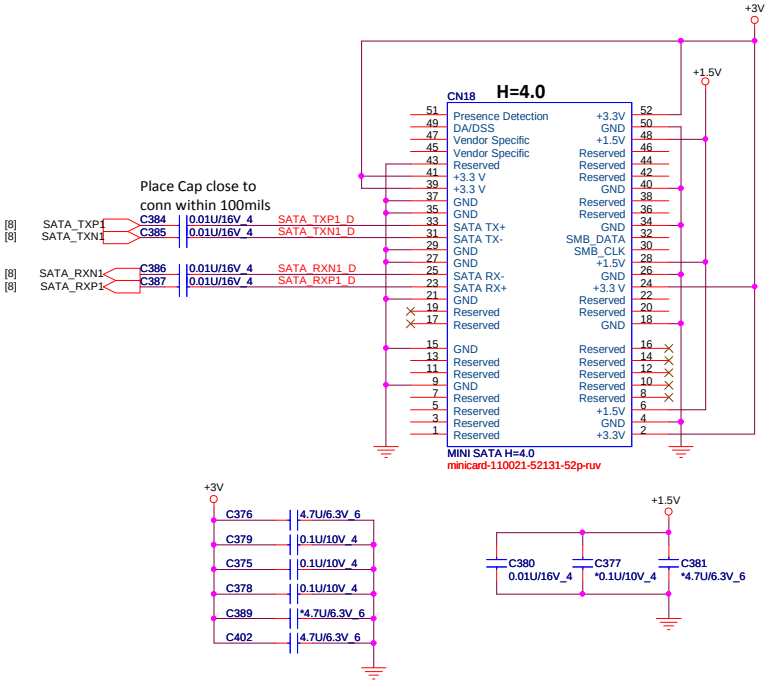


SATA HDD Connector(Cable type)

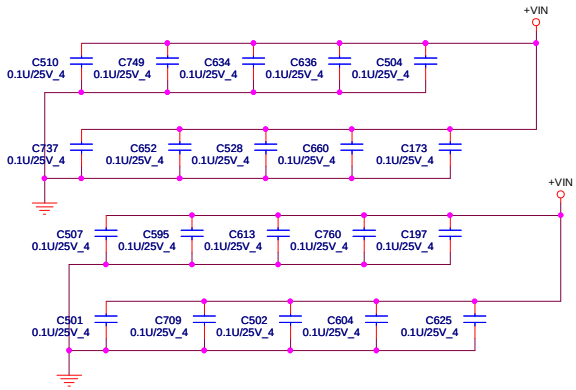




Mini PCI-E Card 2- Full size
mSATA



+VIN Cap



[2,4,6,8,9,10,11,12,13,14,20,21,22,23,24,26,27,33,34,35,38] +3V
[20,22,23,24,27,38] +5V
[4,7,23,24,26,27,28,29] +3VPCU
[2,4,11,24,36,38] +1.5V
[28,34,38] +12VALW

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Quanta Computer Inc.

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Size	Document Number	Rev
Custom	SATA HDD/ODD/MSATA CONN	1A
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ITE pin 100 , 104 , 106 default can not pull up to +3VPCU it will cause chip into test mode

+3VPCU CAP close to EC pin

CAPS LED

CAPSLED# → CAPSLED# [23]

CAPSLED# OUT — Q8 2N7002K

+3VPCU_AC L36 FCM1608KF-121T04

+3VPCU_EC L6 FCM1608KF-121T04

500mA

Change to RB500 as Current loss

SCI1# D13 RB501V-40 → SIO_EXT_SCI# [6]

DNBSWON1# D12 RB501V-40 → DNBSWON# [6]

KBSMI#1 D14 RB501V-40 → SIO_EXT_SMI# [6]

HWPG C511 *0.1U/10V_4

FAN1SIG C503 *0.1U/10V_4

DGPU_PR_EN C534 *0.1U/10V_4

For +VIN noise

SERIRQ C804 100P/50V_4

Vender	Size	P/N
AMIC	4M	AKE39F-0800
EON	4M	AKE39ZN0Q02
Socket		DFHS08FS023

4M SPI EC ROM

U14 A25LQ32AM-F/Q AKE39F-0800 SOIC8-8-1_27

BIOS_CS# BIOS_SPI_CLK_I BIOS_WR# BIOS_RD# SPI_3P SPI_7P

128K byte SPI EC ROM

U15 *W25X40AVSSIG DFHS08FS023 SOIC8-6-1_27

TP84 ICT need TP2675 size test point

TP79 TP76 TP82 TP81 TP83

R278 33_4 EMI C532 22P/50V_4

R287 10K/F_4 SPI_3P

R286 *100K/F_4

TP place on top lay for ICT request

C541 0.1U/10V_4

R285 10K/F_4

PWR_LED

0424 Fix PWR_LED

+3VS5 R295 10K/F_4 PWR_LED# I — Q10 MMBT3904 → PWR_LED# [25]

Adapter select

+3VPCU R240 *10K/F_4 GPIO42 R241 10K/F_4

Hi ==> DIS/SG
Low ==>UMA

Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

IT8518E/HX

U11 — AJ085180F04 — IT8518E/HX

LPC: LAD0–LAD3, LFRAME#, LPCRST#/WUI4/GPD2, LPCCLK, LPCPD#/WUI6/GPE6, GA20/GPB5, SERIRQ, ECSMI#/GPD4, ECSCI#/GPD3, WRST#, KBRST#/GPB6, PWUREQ#/BBO/GPC7

GPIO: EGCLK/WUI27/GPE3, EGCS#/WUI26/GPE2, EGAD/WUI25/GPE1, KSO16/SMOSI/GPC3, KSO17/SMISO/GPC5, L80HLAT/BAO/WUI24/GPE0, L80LLAT/WUI7/GPE7, SBUSY/GPG1/ID7, HMOSIGPH6/ID6, HMISO/GPH5/ID5, HSCK/GPH4/ID4, HSCE#/WUI19/GPH3/ID3, CTX1/WUI18/GPH2/SMDAT3/ID2, CRX1/WUI17/GPH1/SMCLK3/ID1, CLKRUN#/WUI16/GPH0/ID0

GPC0 TMA0/GPB2

PS/2: PS2DAT0/TMB1/GPF1, PS2CLK0/TMB0/GPF0, PS2DAT2/WUI21/GPF5, PS2CLK2/WUI20/GPF4

SM_BUS: SMCLK2/WUI22/GPF6/PECI, SMDAT2/WUI23/GPF7, SMCLK0/GPB3, SMDAT0/GPB4, SMCLK1/GPC1, SMDAT1/GPC2

UART: DAC4/DCD0#/GPJ4, DSR0#/GPG6, GINT/CTS0#/GPD5, PS2DAT1/RTS0#/GPF3, DAC5/RIG0#/GPJ5, PS2CLK1/DTR0#/GPF2, RXD/SIN0/GPB0, TXD/SOUT0/GPB1

FLASH: GPG0 FSCK, FMISO FMOSI FSCE# SSCE0#/GPG2

PWM: PWM0/GPA0, PWM1/GPA1, PWM2/GPA2, PWM3/GPA3, PWM4/GPA4, PWM5/GPA5, PWM6/SSCK/GPA6, PWM7/GPA7, TACH0/GPD6, TACH1/TMA1/GPD7, TMR0/WUI2/GPC4, TMR1/WUI3/GPC6

KBMX: KSO0/PD0, KSO1/PD1, KSO2/PD2, KSO3/PD3, KSO4/PD4, KSO5/PD5, KSO6/PD6, KSO7/PD7, KSO8/ACK#, KSO9/BUSY, KSO10/PE, KSO11/ERR#, KSO12/SLCT, KSO13, KSO14, KSO15, KSI0/STB#, KSI1/AFD#, KSI2/INIT#, KSI3/SLIN#, KSI4, KSI5, KSI6, KSI7

WAKE UP: PWRSW/GPE4, RI1#/WUI0/GPD0, RI2#/WUI1/GPD1, WUI5/GPE5, RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7

A/D D/A: ADC0/GPI0, ADC1/GPI1, ADC2/GPI2, ADC3/GPI3, ADC4/WUI28/GPI4, ADC5/WUI29/GPI5, ADC6/WUI30/GPI6, ADC7/WUI31/GPI7

CLOCK: CK32K, CK32KE

DAC0/GPJ0, DAC1/GPJ1, DAC2/GPJ2, DAC3/GPJ3

VCC VSTBY VBAT AVCC AVSS VCORE VSS

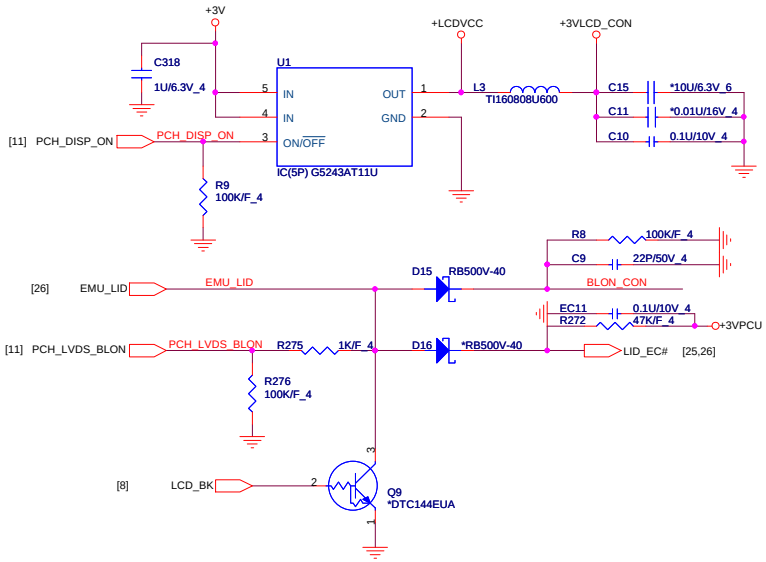
C33 0.1U/10V_4 · R273 *0_4/S · C34 0.1U/10V_4 · C518 0.1U/10V_4 · L37 BK1608HS121-T

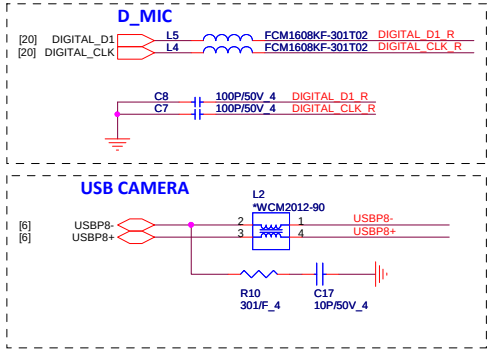
IT8518_AGND

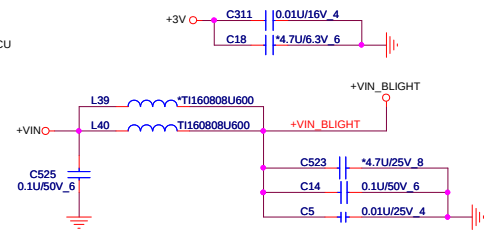
For GPU thermal
for Battery charge/discharge
for CPU themal

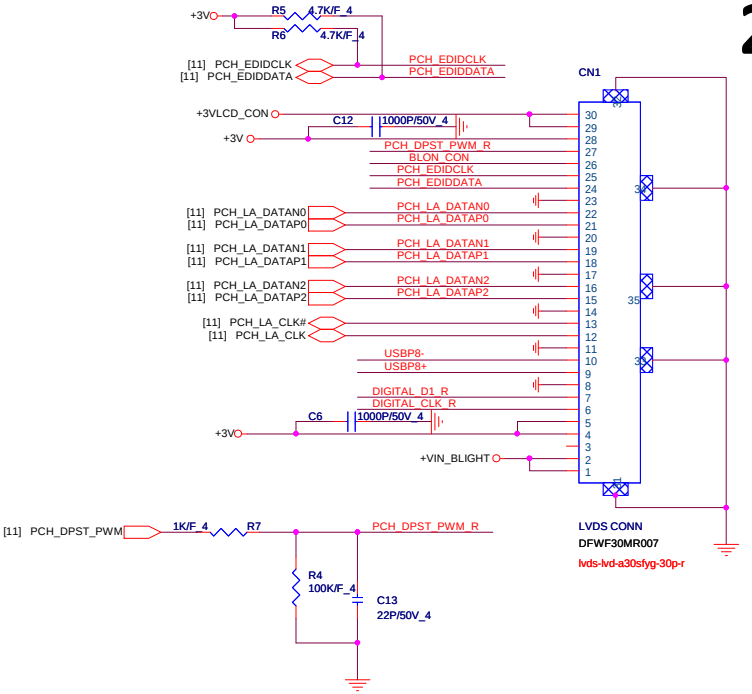
from power button

LVDS Conn.

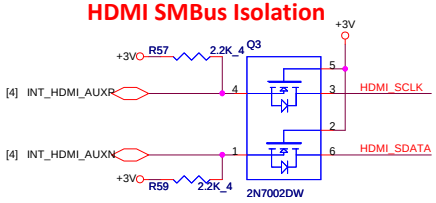


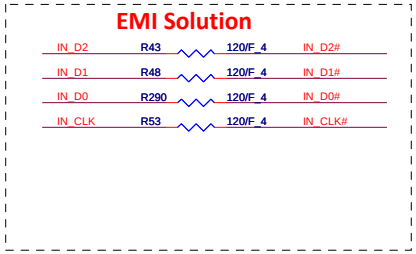


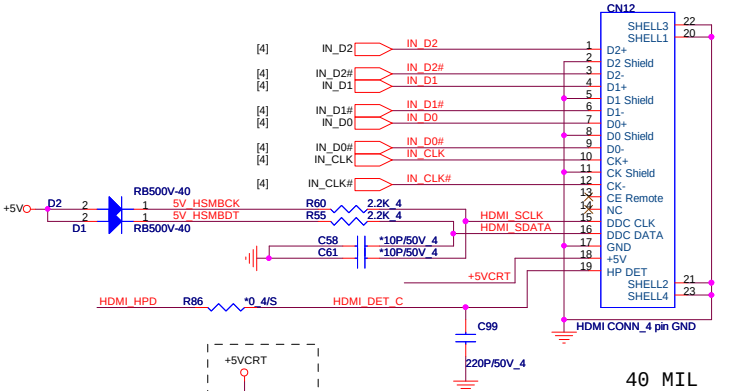


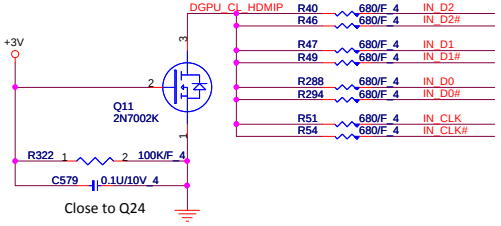


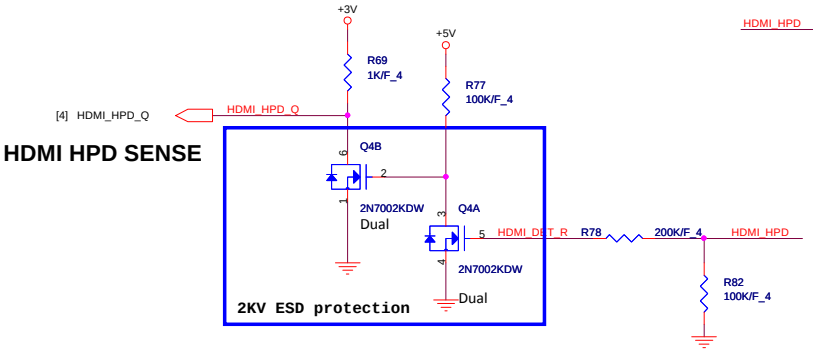
HDMI Conn.

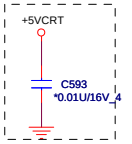


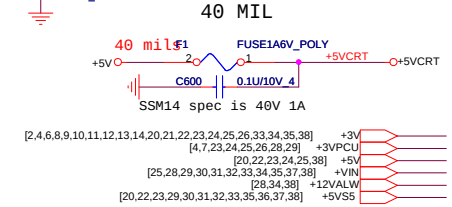












NB5

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Size	Document Number	Rev
Custom	LCD Connector (LVDS)	1A
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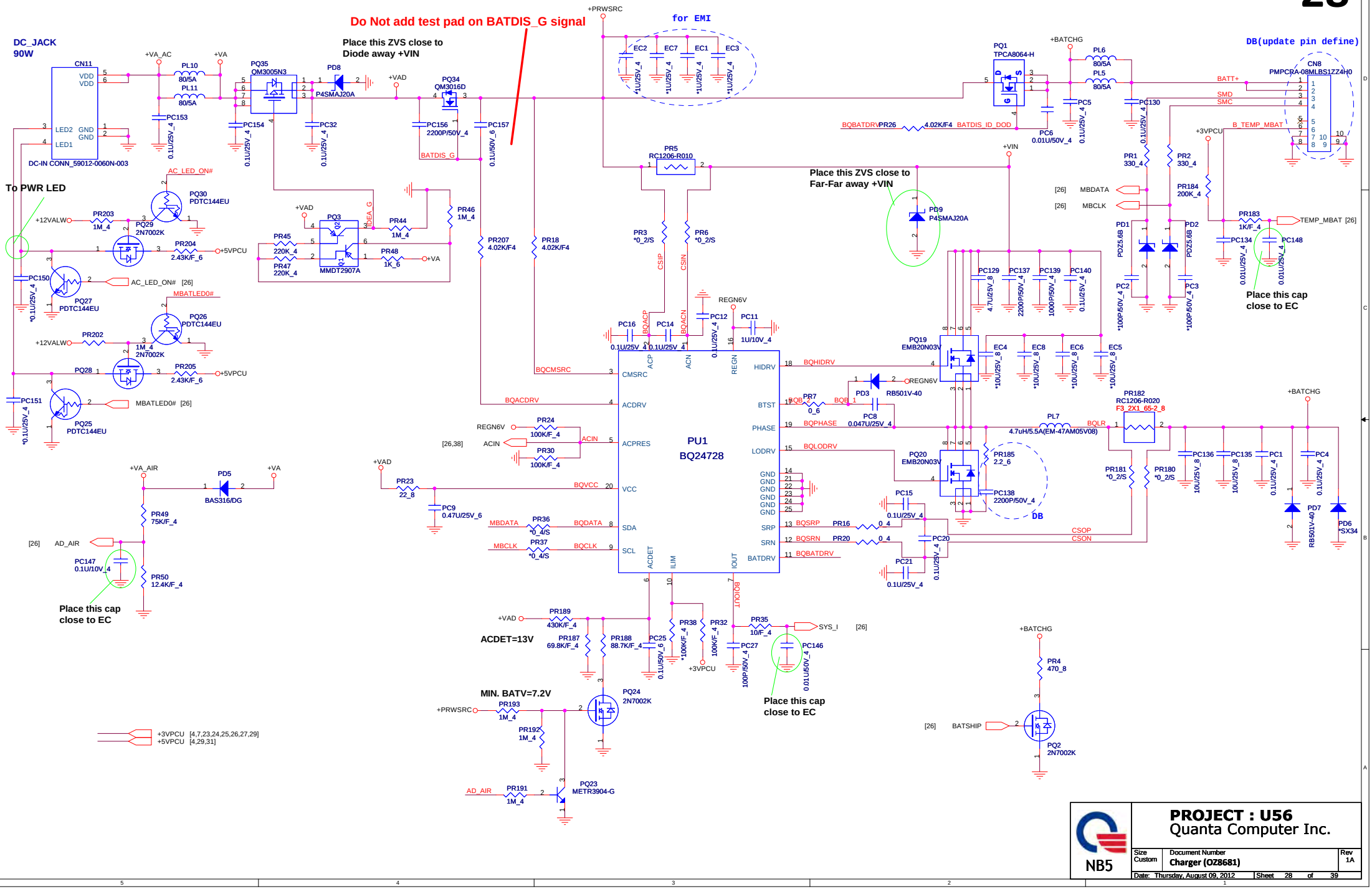

NB5	**PROJECT : U56** Quanta Computer Inc.		
	Size: Custom	Document Number: Charger (OZ8681)	Rev: 1A
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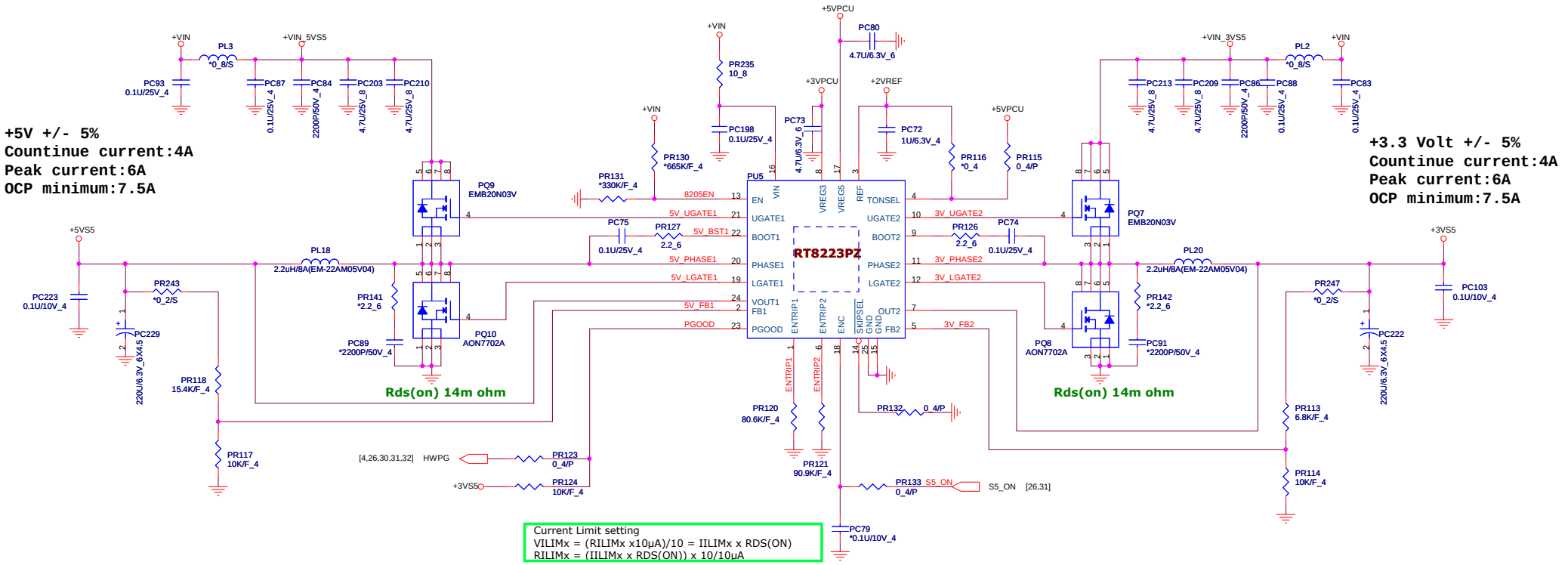
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



[25,27,28,30,31,32,33,34,35,37,38]	+VIN
[6,8,9,10,22,23,24,26,31,33,34,38]	+3VS5
[20,22,23,30,31,32,33,35,36,37,38]	+5VS5
[4,7,23,24,25,26,27,28]	+3VPCU

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Custom	3/5VS5 (RT8223P)	1A

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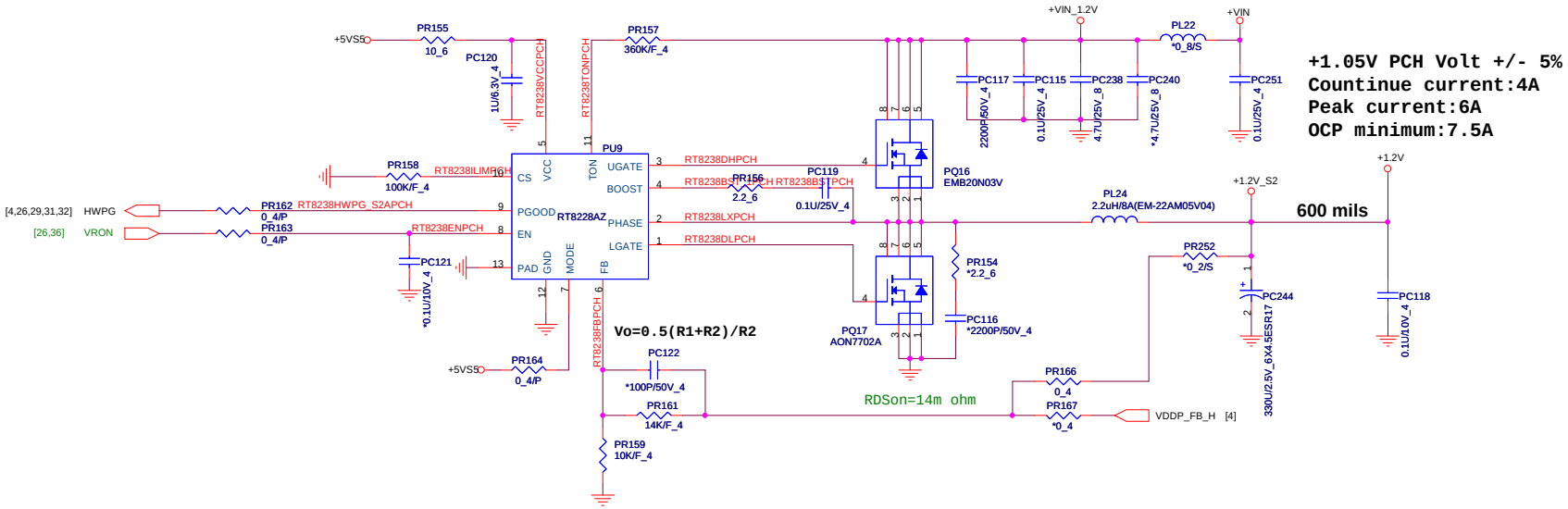

NB5	**PROJECT : U56** Quanta Computer Inc.	
Size: Custom	Document Number: +1.2V (RT8228)	Rev: 1A
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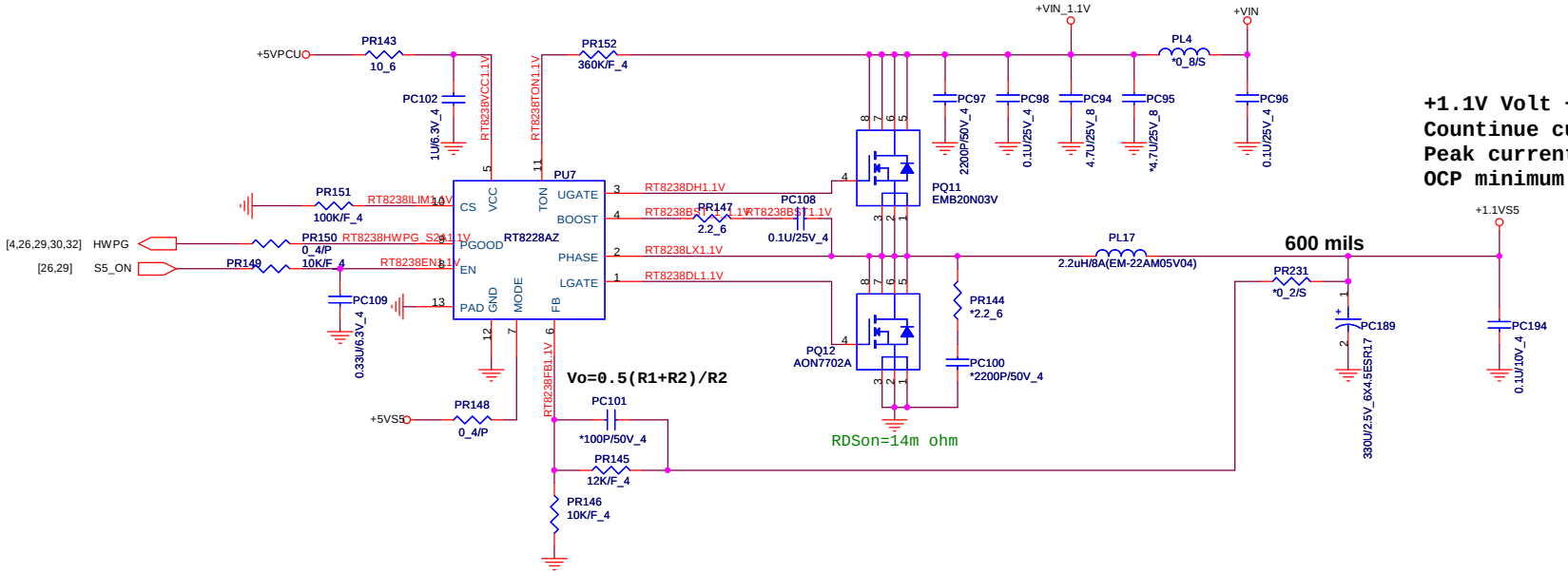
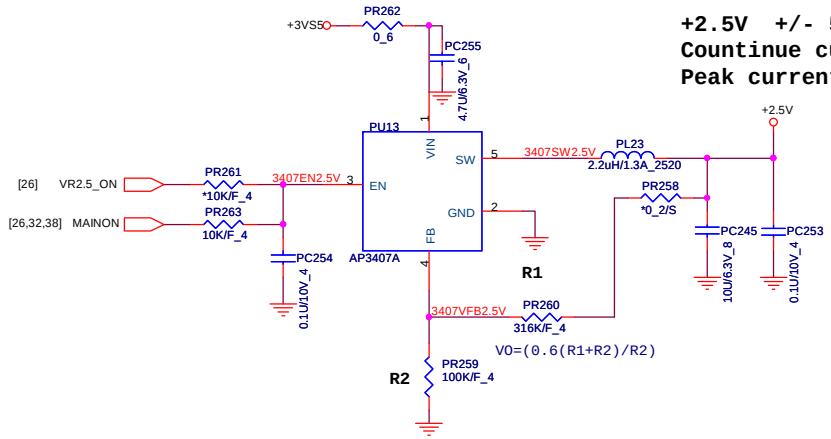


+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 6.5A
OCP minimum:7.5A



+2.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A

NB5	**PROJECT : U56** Quanta Computer Inc.	
Size: Custom	Document Number: **+1.1VS5 (RT8228)/2.5V**	Rev: 1A
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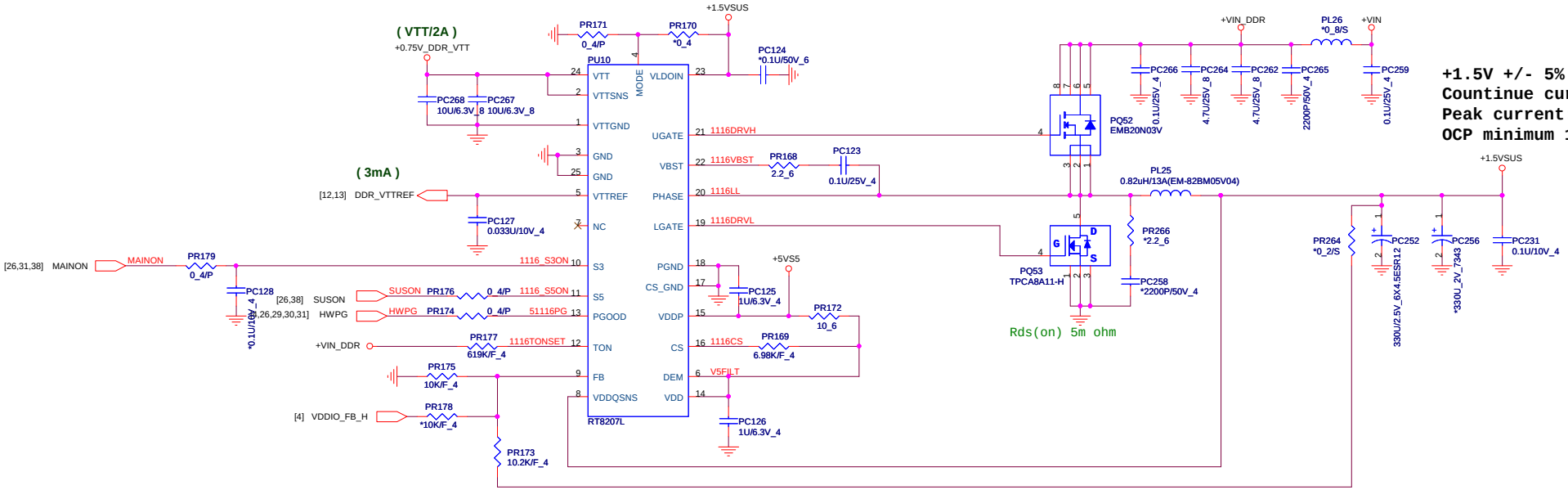

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Size: Custom	Document Number: **DDR3 (RT8207)**	Rev: 1A
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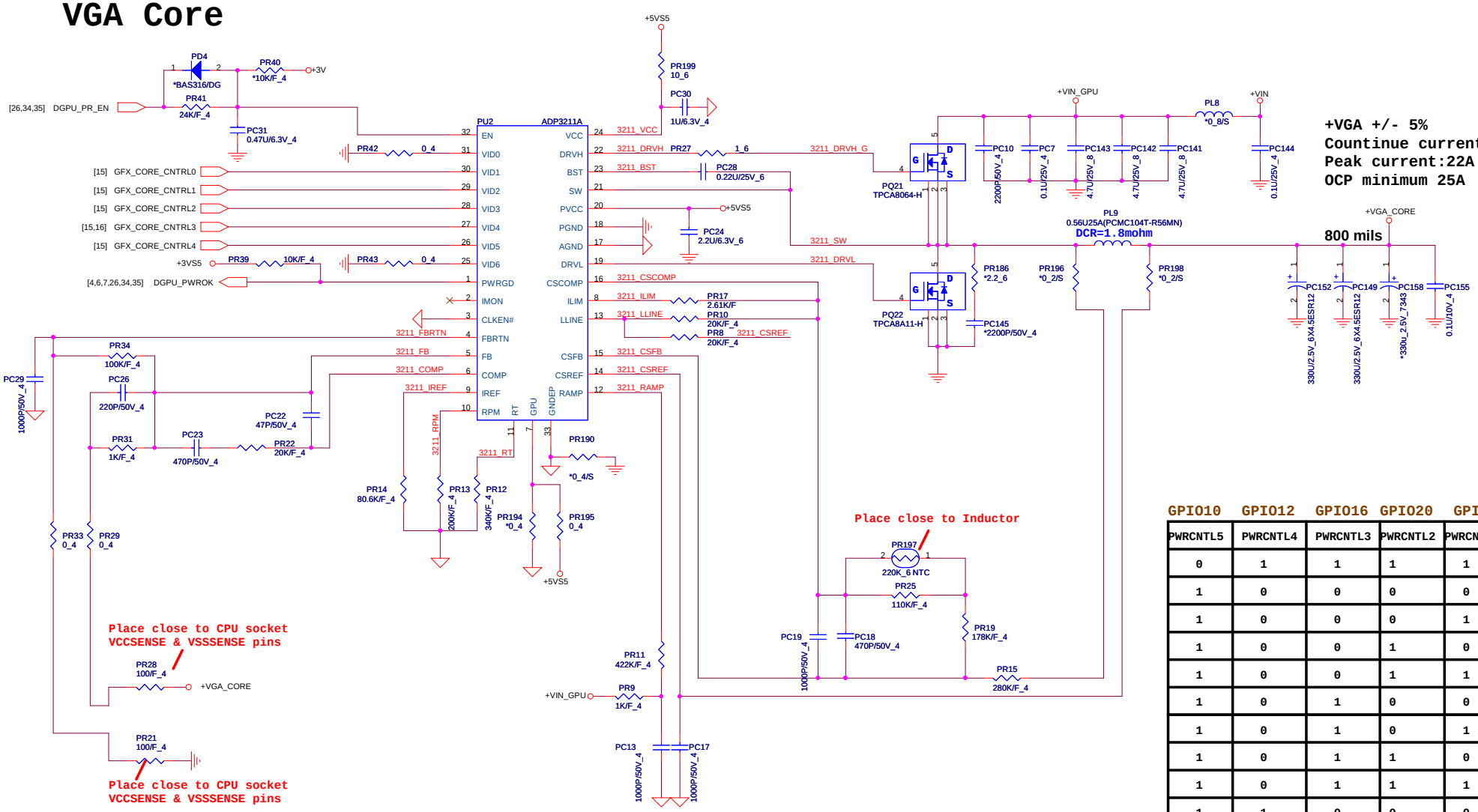
VGA Core



+VGA +/- 5%
Countinue current:18A
Peak current:22A
OCP minimum 25A

GPIO10	GPIO12	GPIO16	GPIO20	GPIO15	Mars XT	
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	Default
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	

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Size	Document Number	Rev
Custom	+VGACORE NCP3218G)	1A
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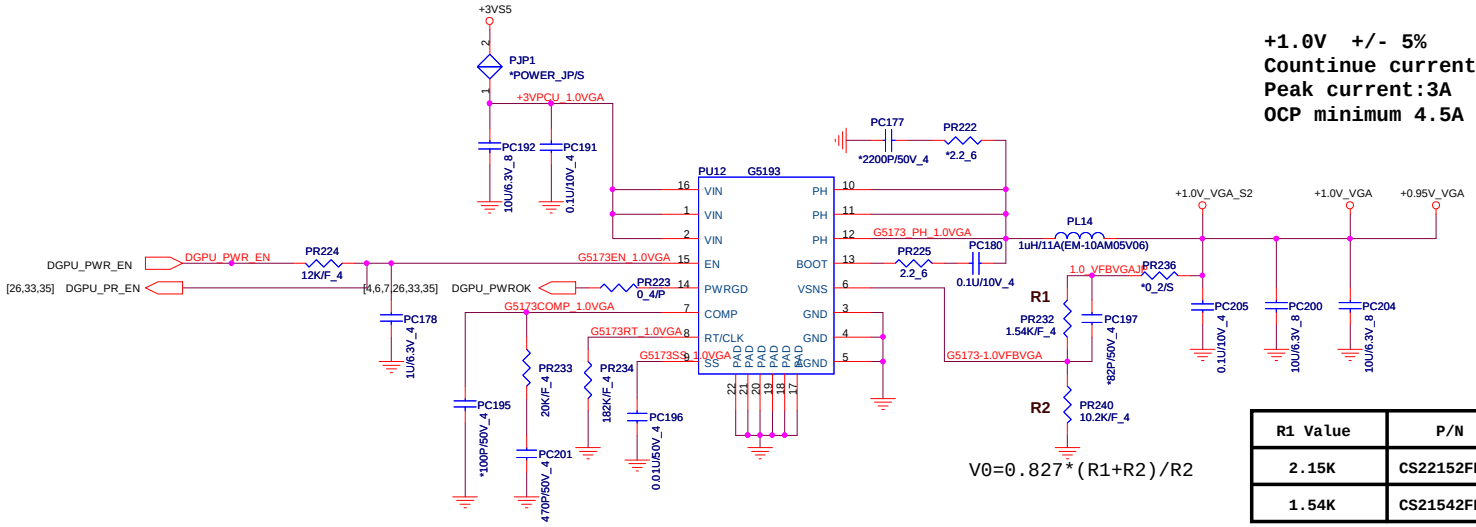


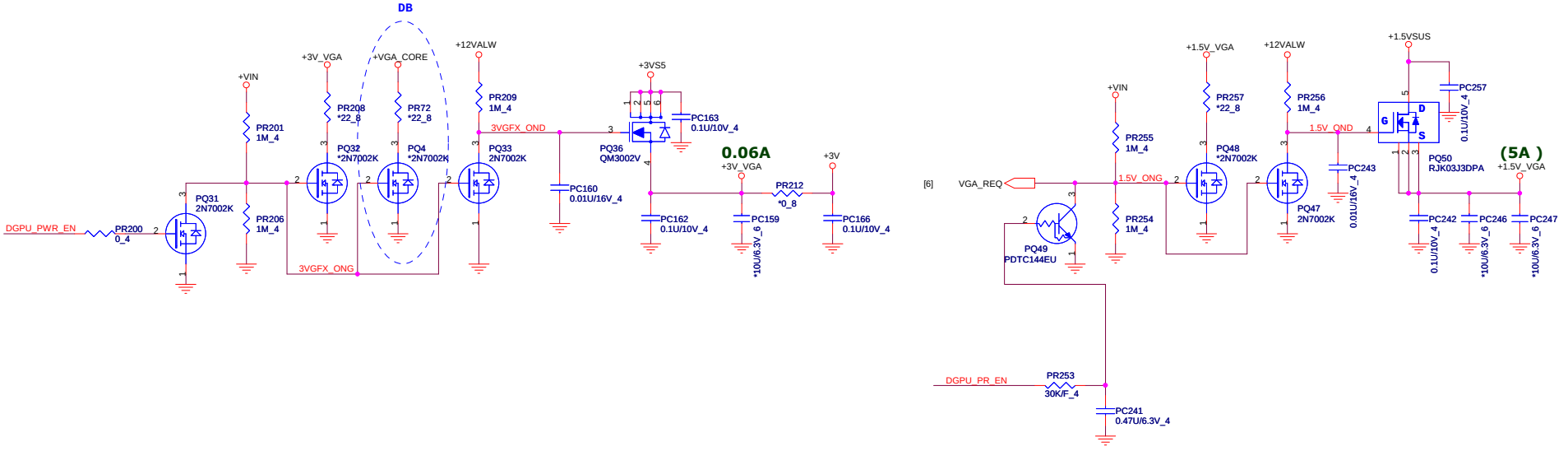
+1.0V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

R1 Value	P/N	1.0V_VGA
2.15K	CS22152FB07	1.0V
1.54K	CS21542FB00	0.95V

$$V0=0.827*(R1+R2)/R2$$

+3V [2,4,6,8,9,10,11,12,13,14,20,21,22,23,24,25,26,27,33,35,38]
+VIN [25,27,28,29,30,31,32,33,35,37,38]

+3VS5 [6,8,9,10,22,23,24,26,29,31,33,38]
+5VS5 [20,22,23,29,30,31,32,33,35,36,37,38]
+3V_VGA [17]
+12VALW [28,38]
+1.5VSUS [2,3,4,5,12,13,32,38]
+1.5V_VGA [17,18,19]
+1.8V_VGA [14,15,17,35]
+3V_DELAY [15,16,17]
+VGA_CORE [17,33]



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Size	Document Number	Rev
Custom	+VGA POWER	1A

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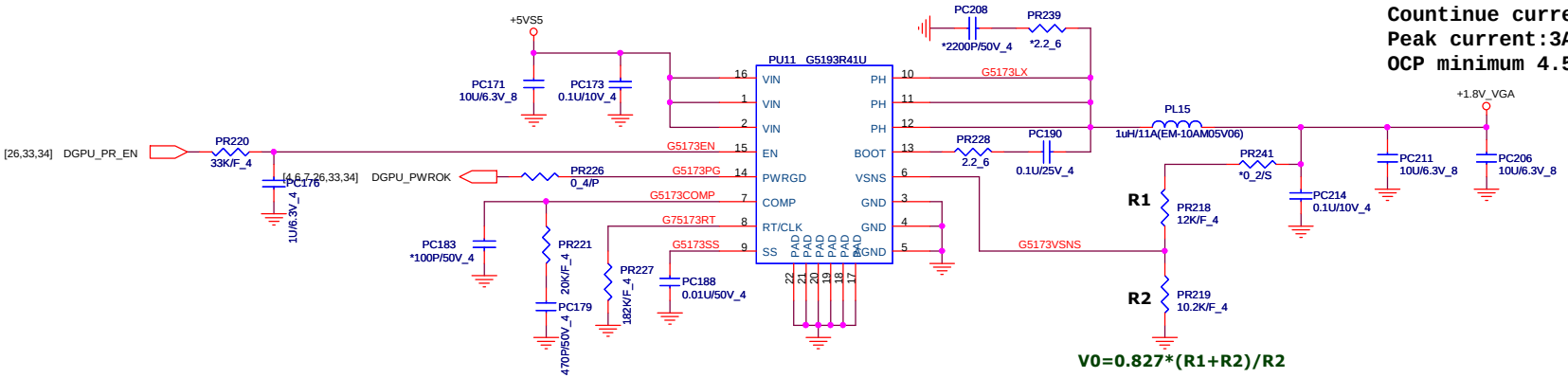
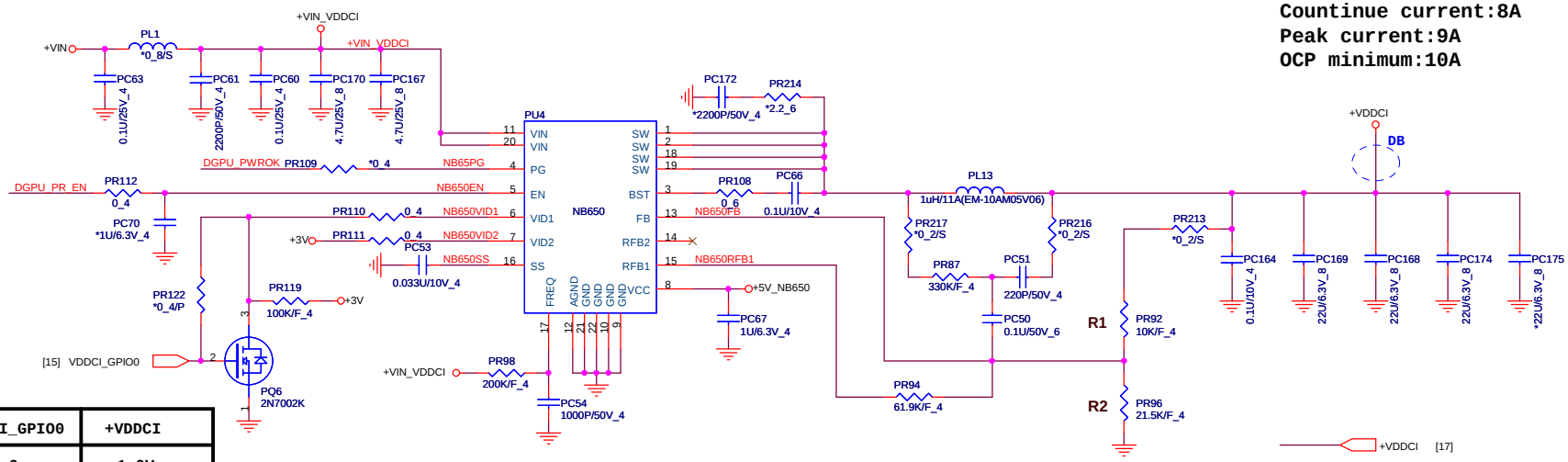
+1.8V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A



V0=0.827*(R1+R2)/R2

+VDDCI +/- 5%
Countinue current:8A
Peak current:9A
OCP minimum:10A



VDDCI_GPIO1	VDDCI_GPIO0	+VDDCI
X	0	1.0V
X	1	0.9V
X	X	X
X	X	X

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Size	Document Number	Rev
Custom	+1.8V_VGA (G5193)	1A
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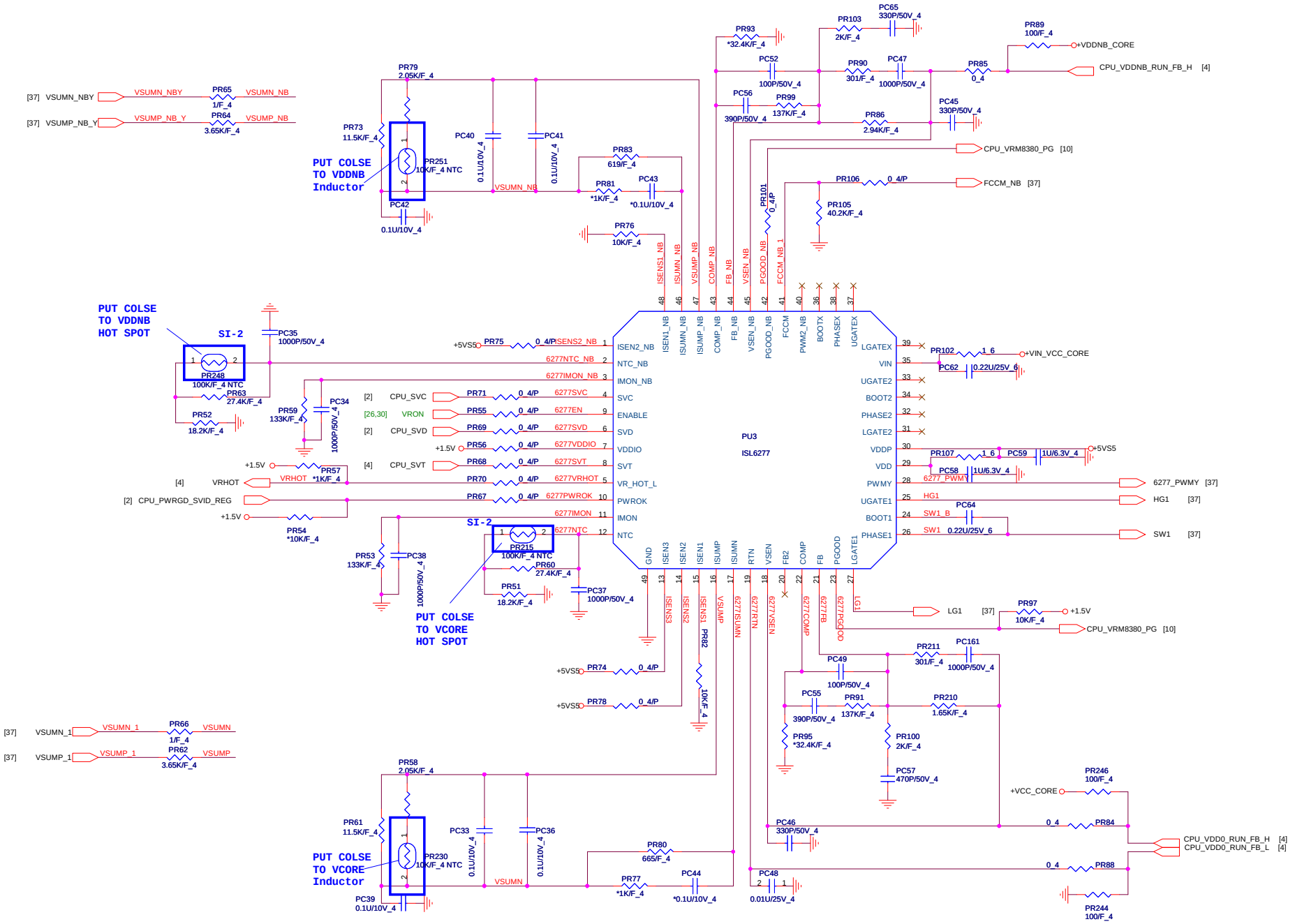

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Custom	ISL6277	1A

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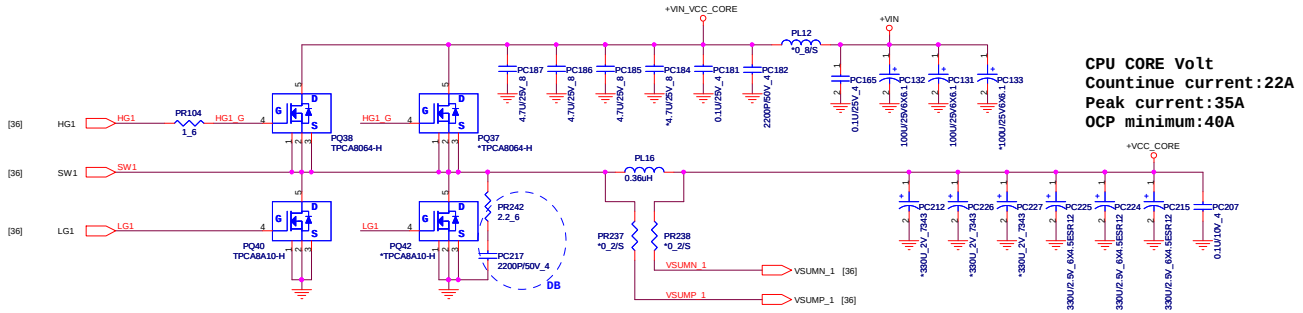
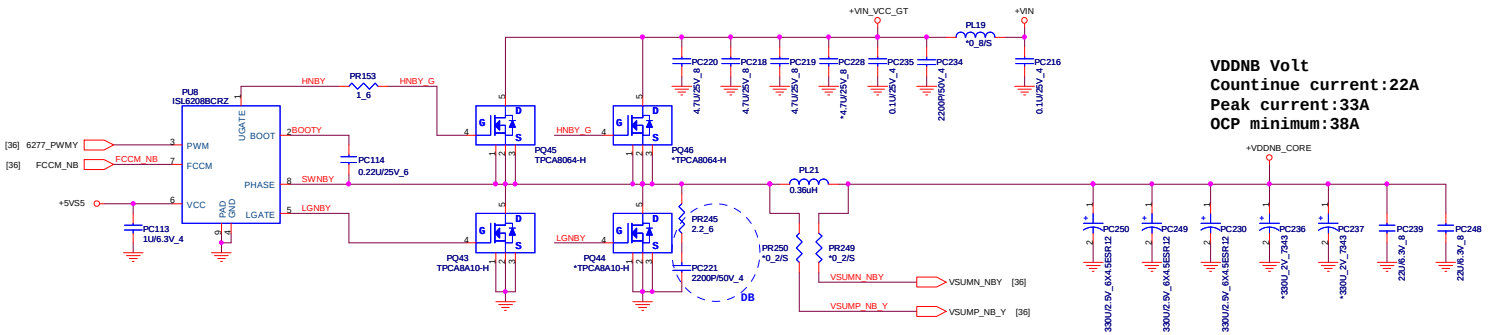


CPU CORE Volt
Countinue current:22A
Peak current:35A
OCP minimum:40A



VDDNB Volt
Countinue current:22A
Peak current:33A
OCP minimum:38A

NB5

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Custom	ISL6208	1A

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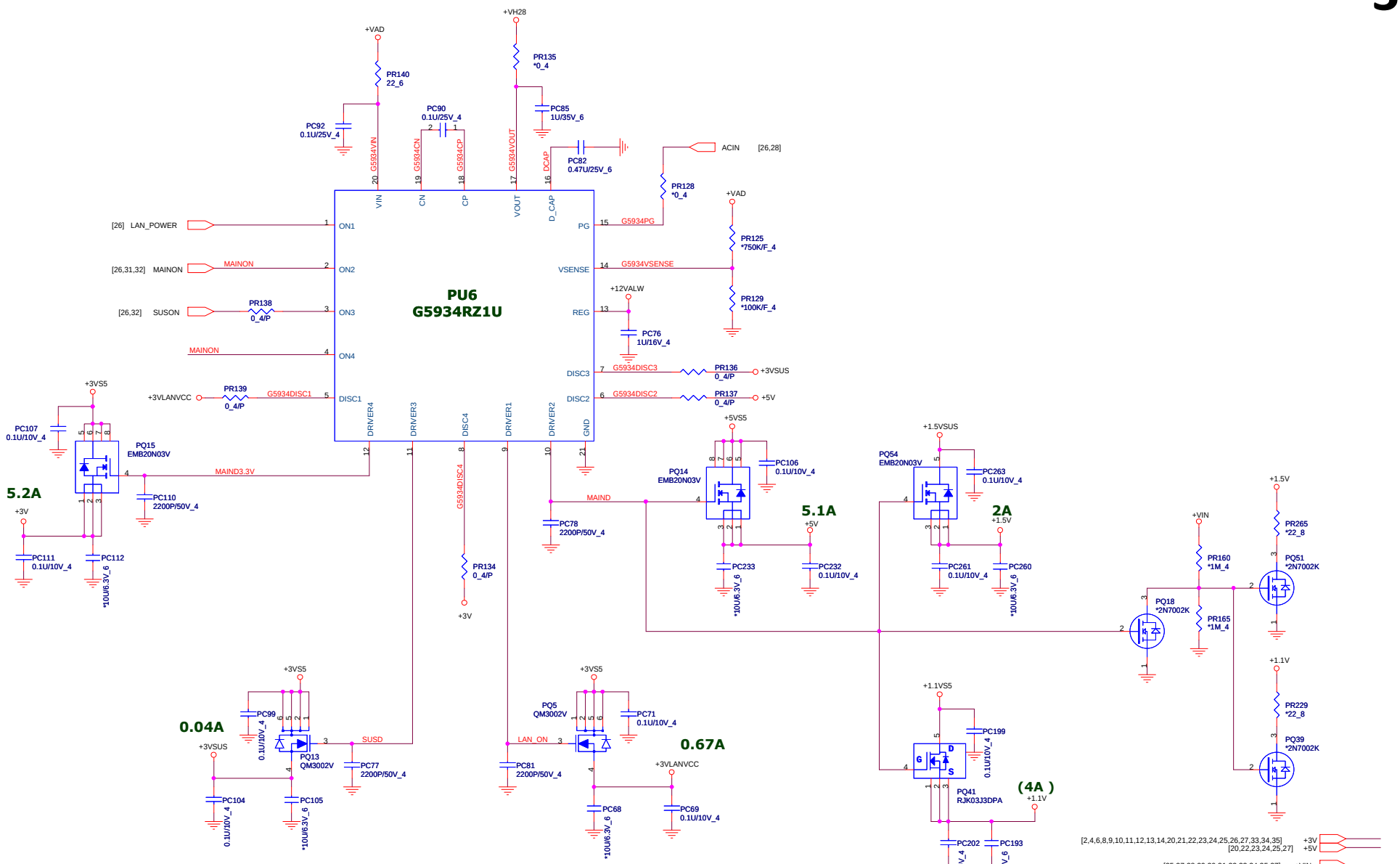

NB5

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Size	Document Number	Rev
C	History	1A

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