

COMPAL CONFIDENTIAL

MODEL NAME : VALA0

PCB NO : LA-9411P

GPIO P/N: 2012.12.20 Rev 3.0C

BOM P/N :

4319L231L01 SMT MB A9411 VALA0 DSC TPM R1

4319L231L02 SMT MB A9411 VALA0 DSC DTP R1

4319L231L03 SMT MB A9411 VALA0 DSC TPM WO EXP R1

4319L231L04 SMT MB A9411 VALA0 DSC DTP WO EXP R1

4319L231L05 SMT MB A9411 VALA0 DSC TPM R1

4319L231L06 SMT MB A9411 VALA0 DSC DTP R1

4319L231L07 SMT MB A9411 VALA0 DSC TPM WO EXP R1

4319L231L08 SMT MB A9411 VALA0 DSC DTP WO EXP R1

SALADO 15 HSW

HASWELL + LYNX POINT

2013_04_10

REV : 1.0 (A00)

@ : Nopop Component

CONN@ : Connector Component

	L01/L02/L5/L6	L03/L04/L7/L8
15MDC@ : MDC	V	V
15G@ : Only for 15 Discrete	V	V
PXDP@ : PCH XDP		
EMC@ : EMI/ESD/RF	V	V
EXP@ : Express Card	V	V
CXDP@ : CPU XDP		

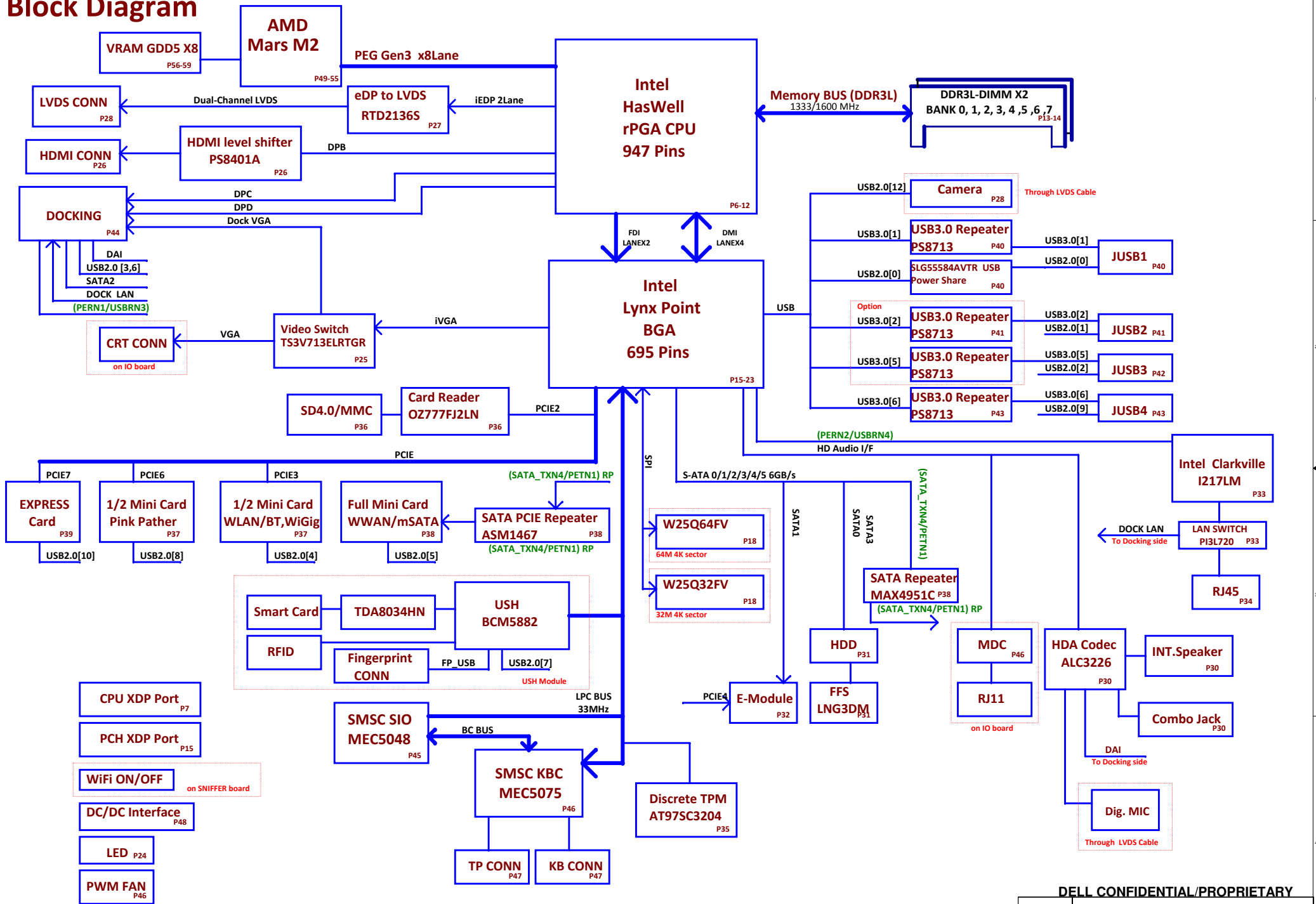
Part Number	Description
DAA00005Q00	PCB 0LH LA-9411P REV0 M/B DSC

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Block Diagram



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Block Diagram

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+PWR_SRC +PWR_SRC_S +5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +VCC_CORE +1.05V_RUN +GPU_CORE +1.35V_MEM_GFX +1.8V_RUN_GFX +VGA_PCIE +3.3V_RUN_GFX +VDDCI	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB 2.0 PORT#	USB 3.0 PORT#	DESTINATION
	0	1	Right Side Top (JUSB1)
	1	2	Right Side Middle (JUSB2)
	2	5	Right Side bottom (JUSB3)
	3	3 (PERN1/USBRN3)	DOCKING (JDOCK1)
	4		WLAN (JMINI2)
	5		WWAN (JMINI1)
	6		DOCKING (JDOCK1)
	7		USH (JUSH1)
	8		Pink Pather (JMINI3)
	9	6	Left Side (JUSB4)
	10		Express card (JEXP1)
	11		None
	12		CAMERA (JCAM1)
	13		None

PCI EXPRESS	DESTINATION
Lane 1 (SATA_TXN4/PETN1)	WWAN (JMINI1) SATA by default
Lane 2 (SATA_RXN5/PERN2)	None
Lane 2 (PERN2/USBRN4)	10/100/1G LOM
Lane 3	WLAN (JMINI2)
Lane 4	E3 Module Bay (JSATA2)
Lane 5	None
Lane 6	Pink Pather (JMINI3)
Lane 7	Express card (JEXP1)
Lane 8	MMI

SATA	DESTINATION
SATA 0	HDD (JSATA1)
SATA 1	ODD (JSATA2)
SATA 2	Dock (JDOCK1)
SATA 3	NA
SATA 4 (SATA_TXN4/PETN1)	WWAN (JMINI1) SATA by default

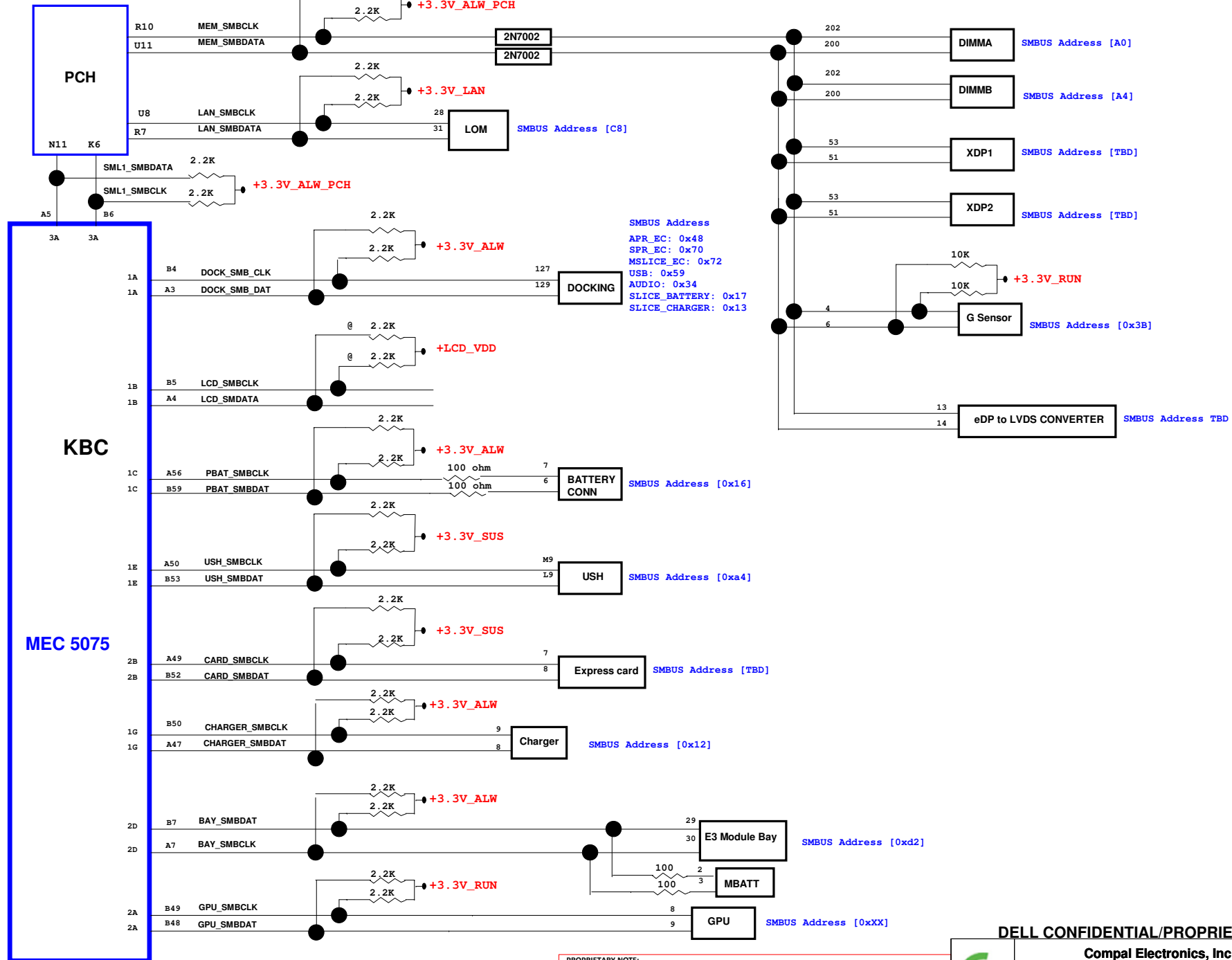
DISPLAY Ports On CPU	Connetion
DDIB	MB HDMI (JHDMI1)
DDIC	Dock DP port 1
DDID	Dock DP port 2

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SMBUS Address [0x9a]



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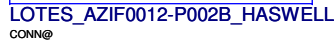
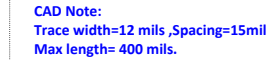
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SMBus block diagram

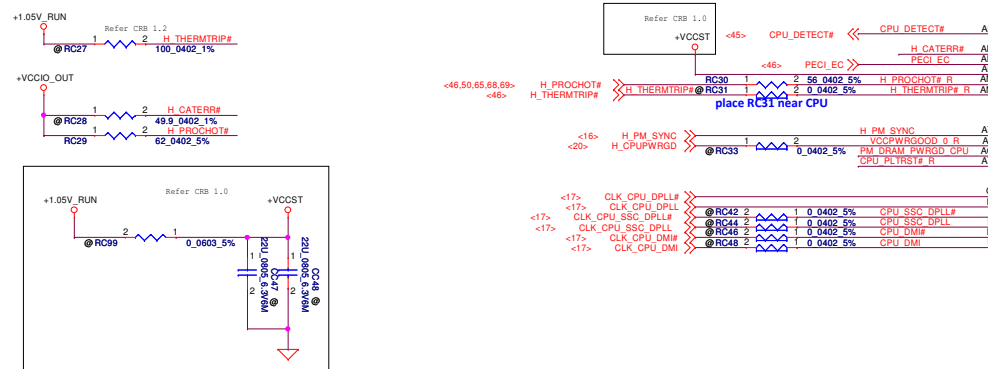
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[illegible]

Buffered reset to CPU

CAD Note:
PLACE PULL-UP RESISTOR WITHIN 2 INCH OF THE CPU

CAD Note:
Avoid stub in the PWRGD path while placing resistors RC33 & RC56

DDR3 COMPENSATION SIGNALS

CAD Note:
 Trace width=12~15 mil, Spacing=20 mils
 Max trace length= 500 mil

CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

PU/PD for JTAG signals

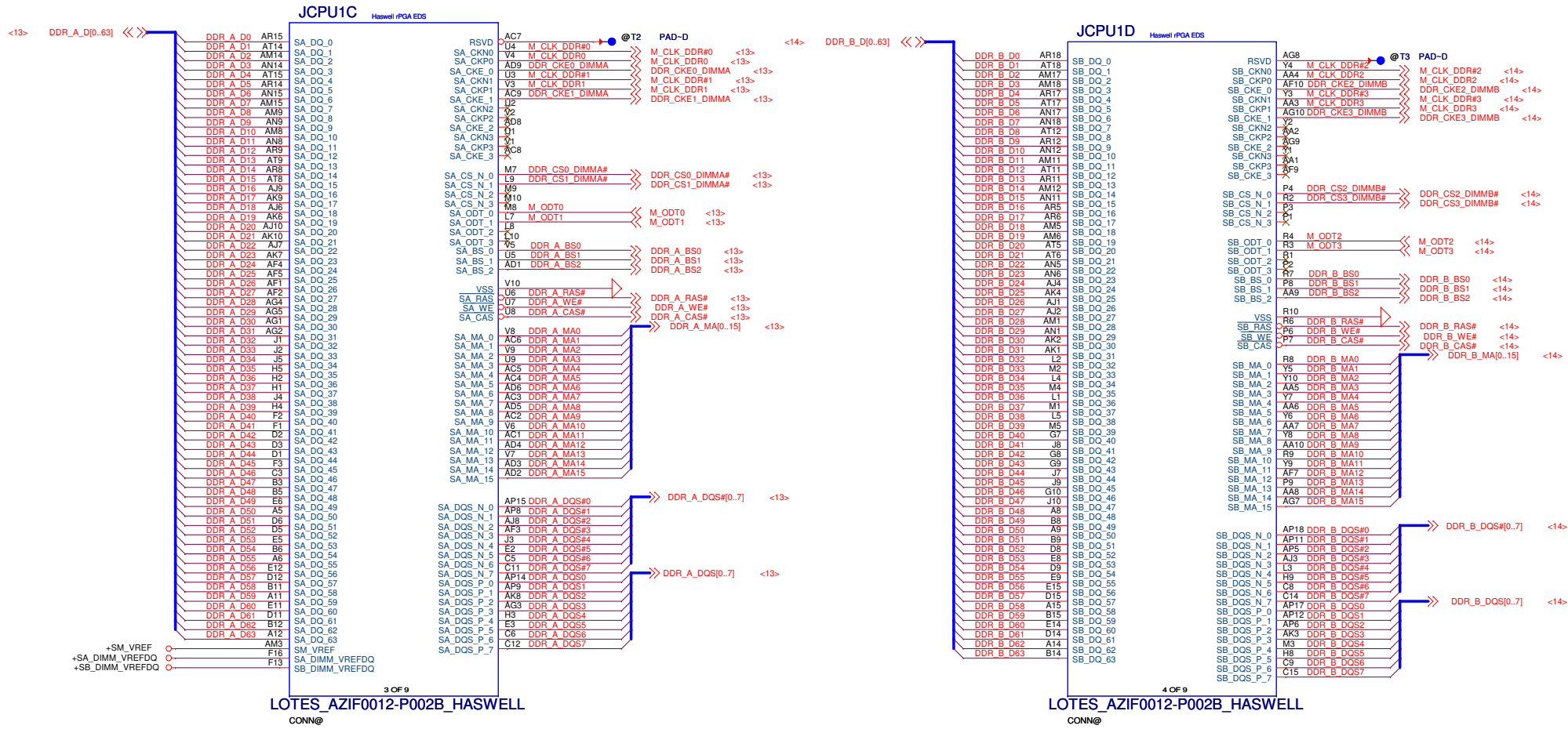
The diagram illustrates the power-up and power-down (PU/PD) for JTAG signals. It shows several signals connected to resistors (RC52, RC54, RC55, RC62) and power sources (+3.3V_RUN, +1.05V_RUN). The signals are:

- XDP DBRESET#**: Connected to RC52 2, 1 51 0402 1%.
- XDP TMS**: Connected to RC53 2, 1 51 0402 1%.
- XDP TDI**: Connected to RC54 2, 1 51 0402 1%.
- XDP PREQ#**: Connected to RC55 2, 1 51 0402 1%.
- XDP TDO**: Connected to RC57 2, 1 51 0402 1%.
- XDP TCLK**: Connected to RC59 2, 1 51 0402 1%.
- XDP TRST#**: Connected to RC62 2, 1 51 0402 1%.

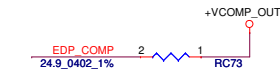
Power sources are +3.3V_RUN and +1.05V_RUN. A CXPD@ symbol is also present.

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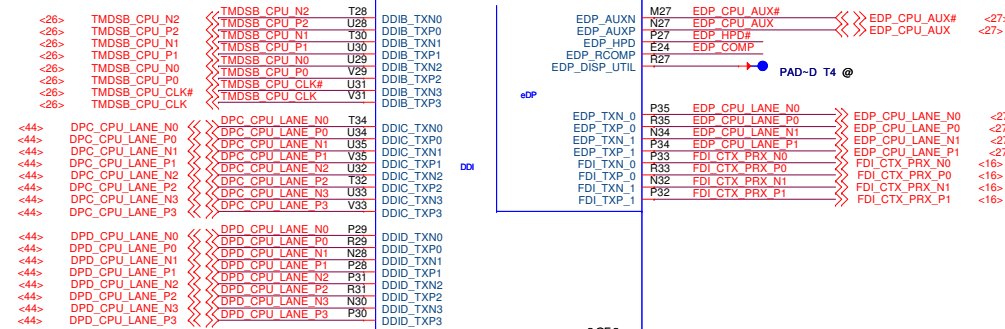


COMPENSATION PU FOR eDP



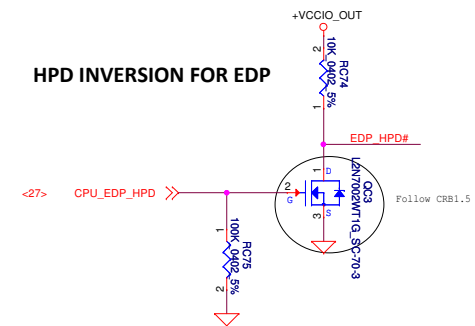
CAD Note: Trace width=20 mils, Spacing=25mil, Max length=100 mils.

JCPU1H Haswell PGA EDS



OTES_AZIF0012-P002B_HASWELL CONN@

HPD INVERSION FOR EDP



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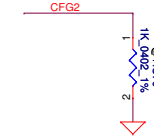
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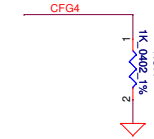
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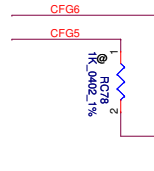
CFG STRAPS for CPU



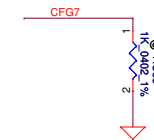
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



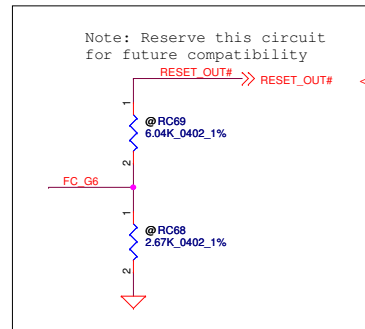
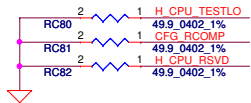
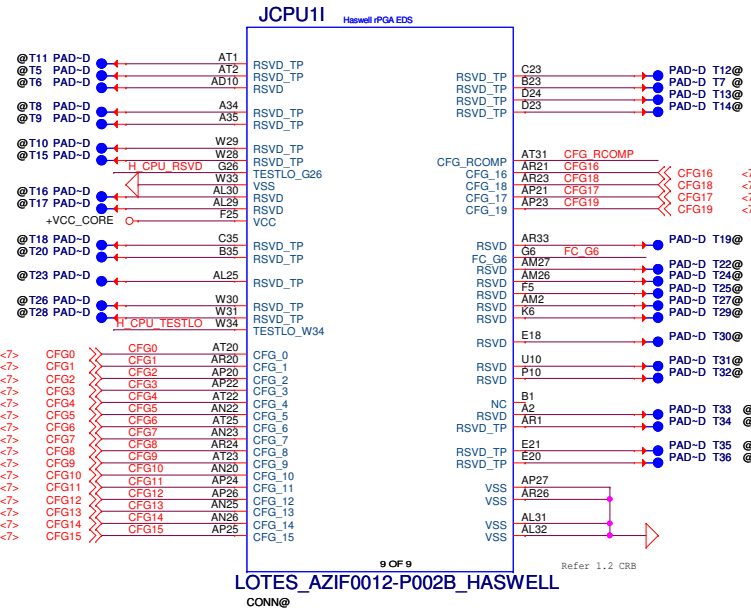
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



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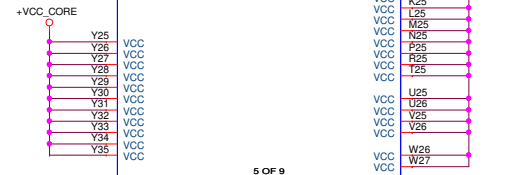
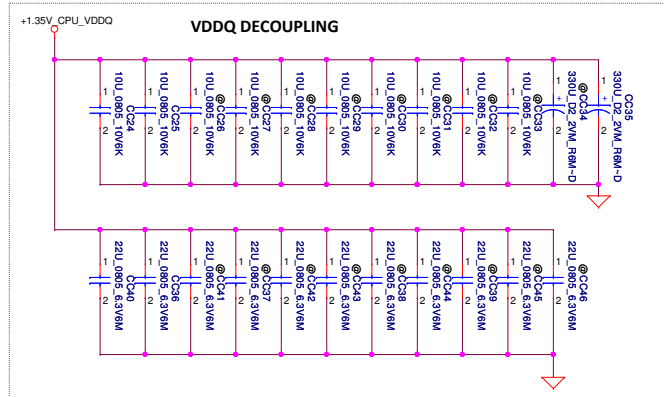
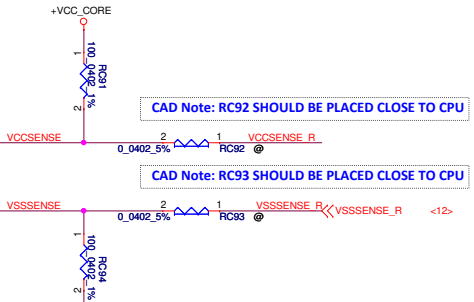
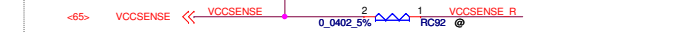
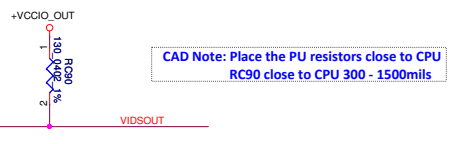
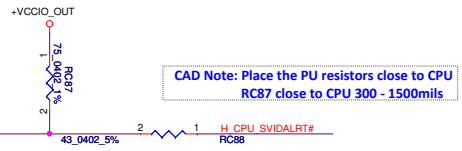
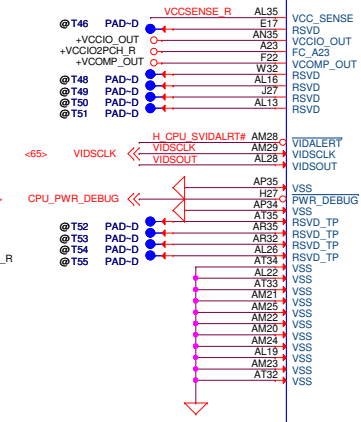
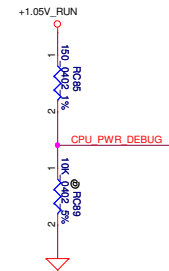
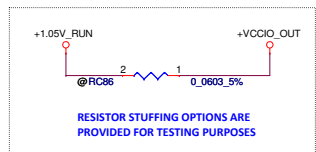
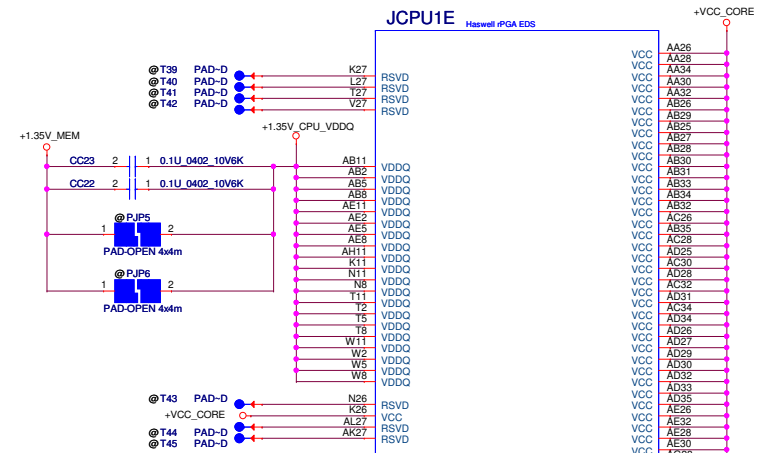
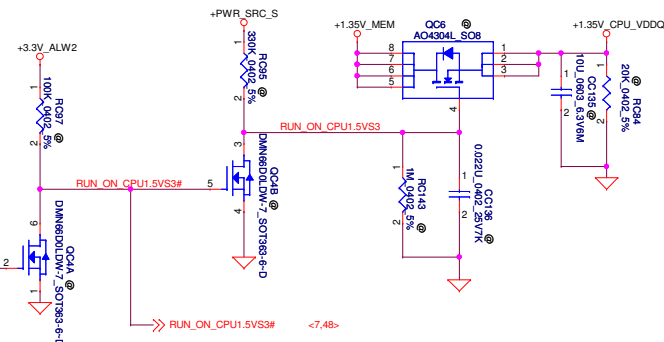
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16,35,39,40,45,48,64,66> SIO_SLP_S3# >> 0_0402_5%

<46> CPU1.5V_S3_GATE >> 0_0402_5%



CONING@

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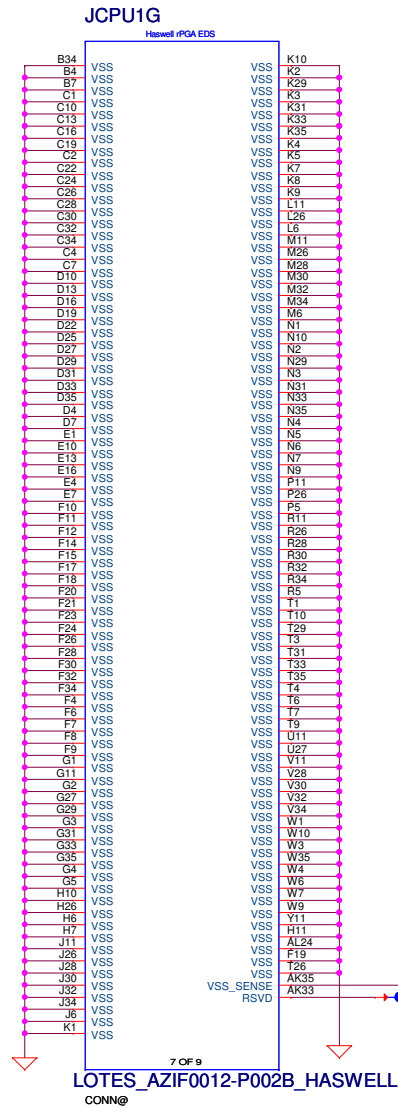
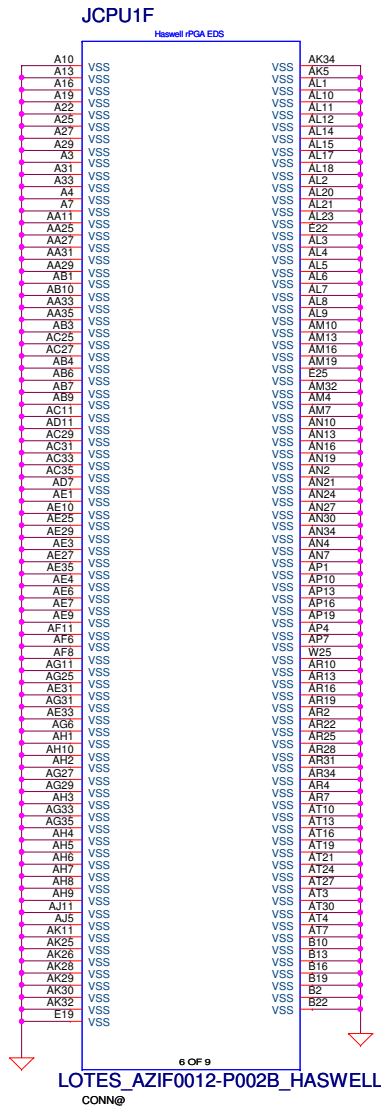
CPU (6/7)

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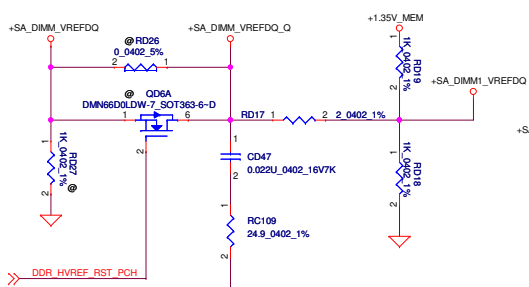


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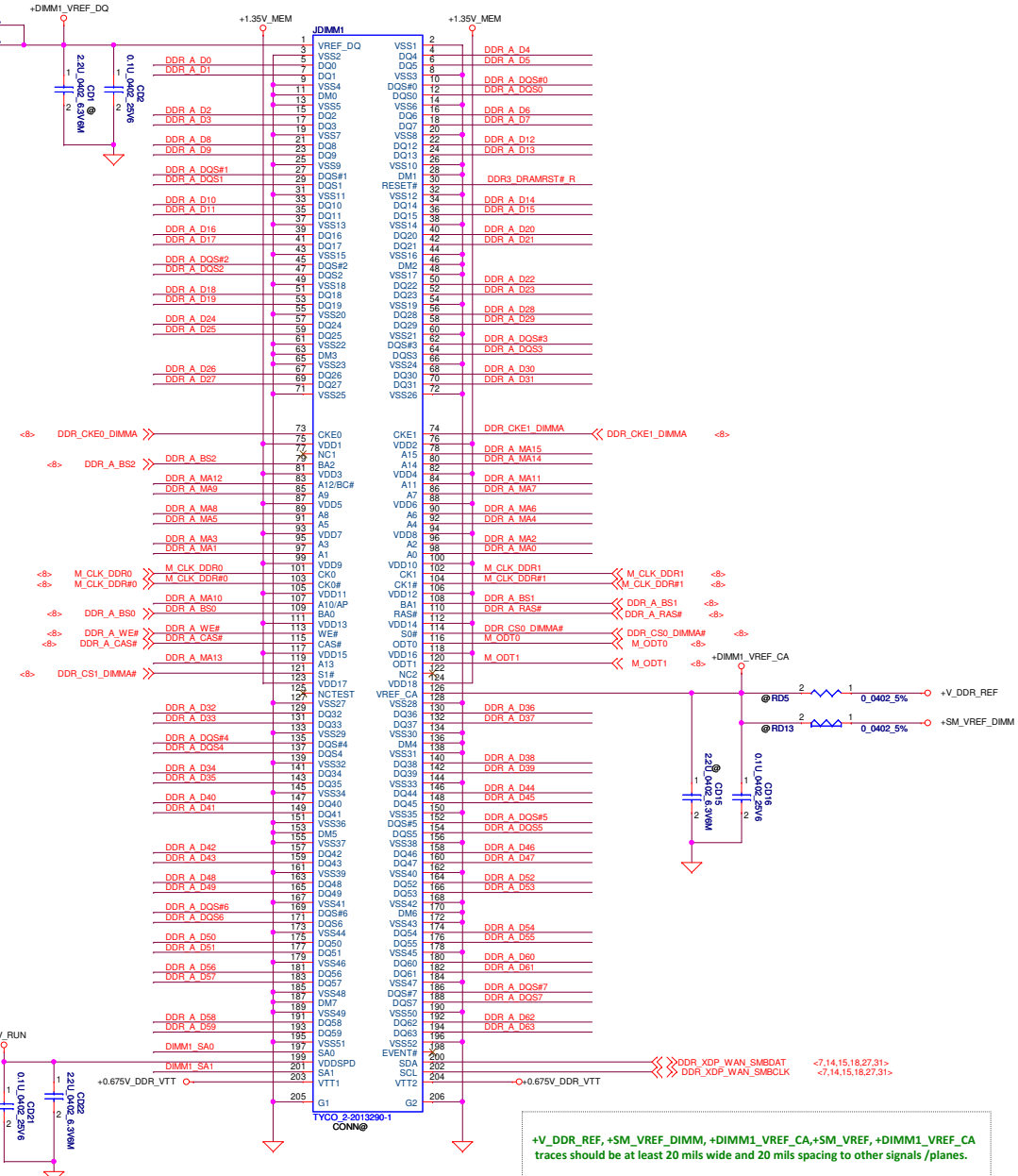


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Populate RD1, De-Populate RD3 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

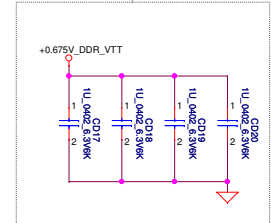
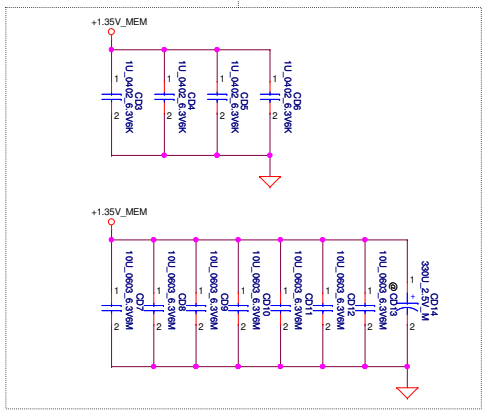
JDIMM1 H=5.2mm



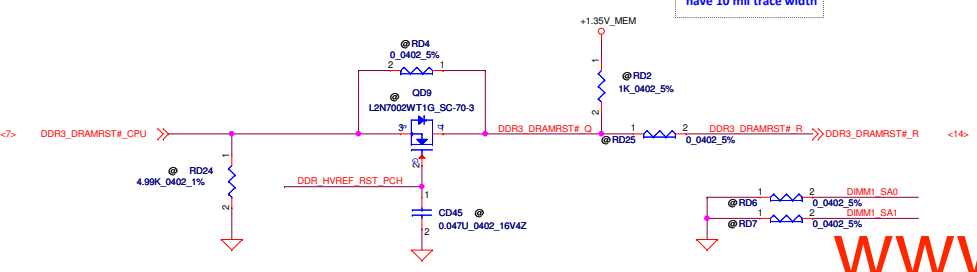
+V_DDR_REF, +SA_DIMM1_VREFDQ, +SA_DIMM_VREFDQ, +DIMM1_VREF_DQ traces should be at least 20 mils wide and 20 mils spacing to other signals /planes.

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204



All VREF traces should have 10 mil trace width



+V_DDR_REF, +SM_VREF_DIMM, +DIMM1_VREF_CA, +SM_VREF, +DIMM1_VREF_CA traces should be at least 20 mils wide and 20 mils spacing to other signals /planes.

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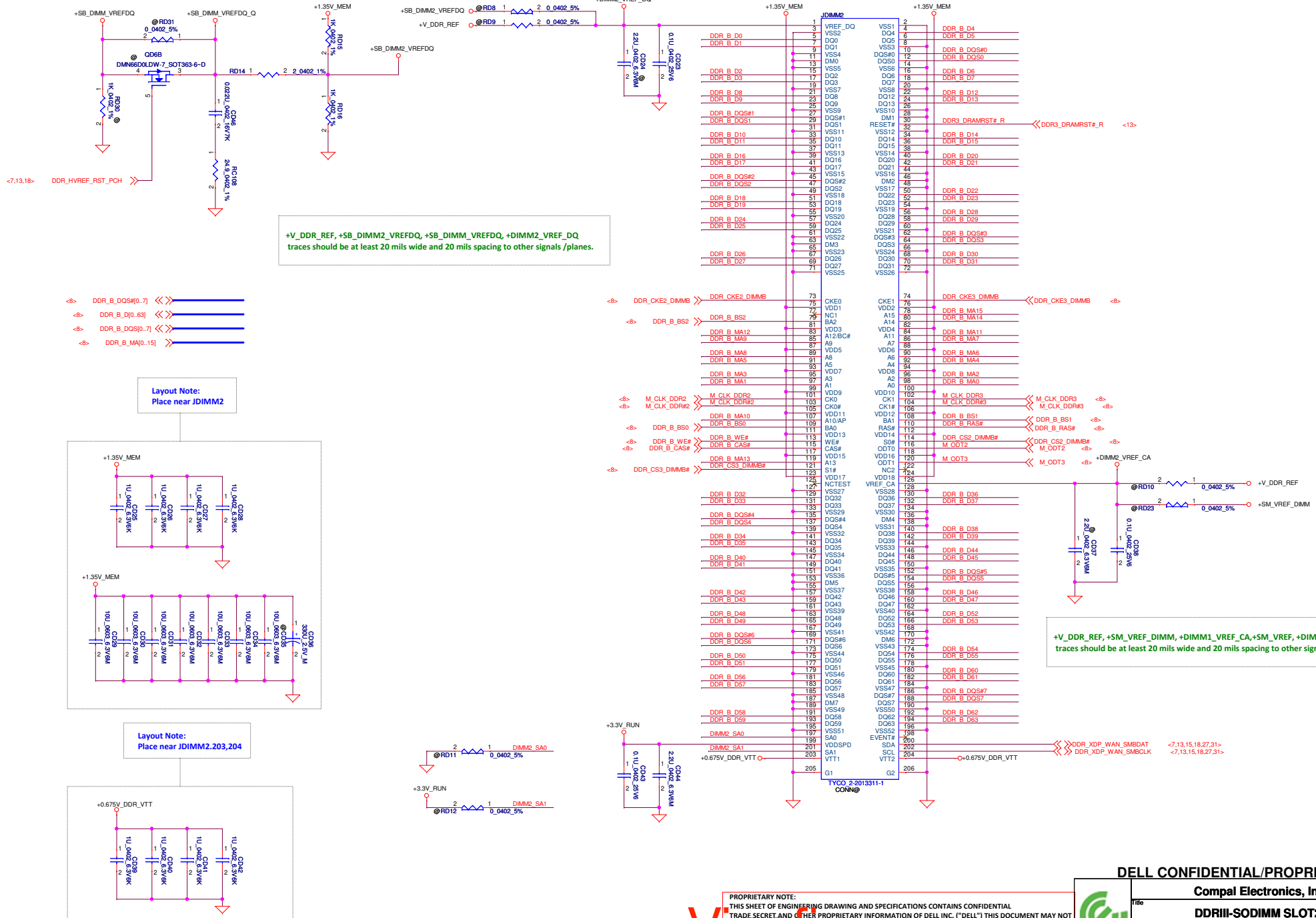
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DDR3-SODIMM SLOT1			
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Populate RD4, De-Populate RD9 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M3

JDIMM2 H=9.2mm



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DDRIII-SODIMM SLOT2

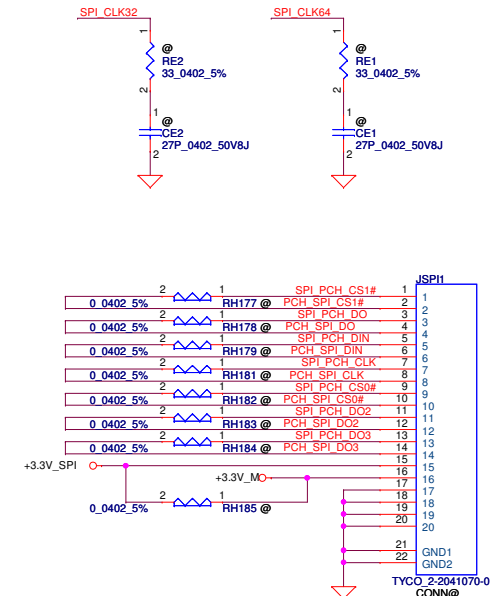
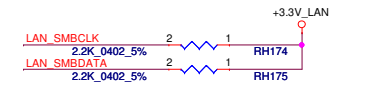
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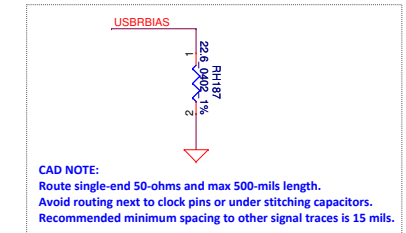
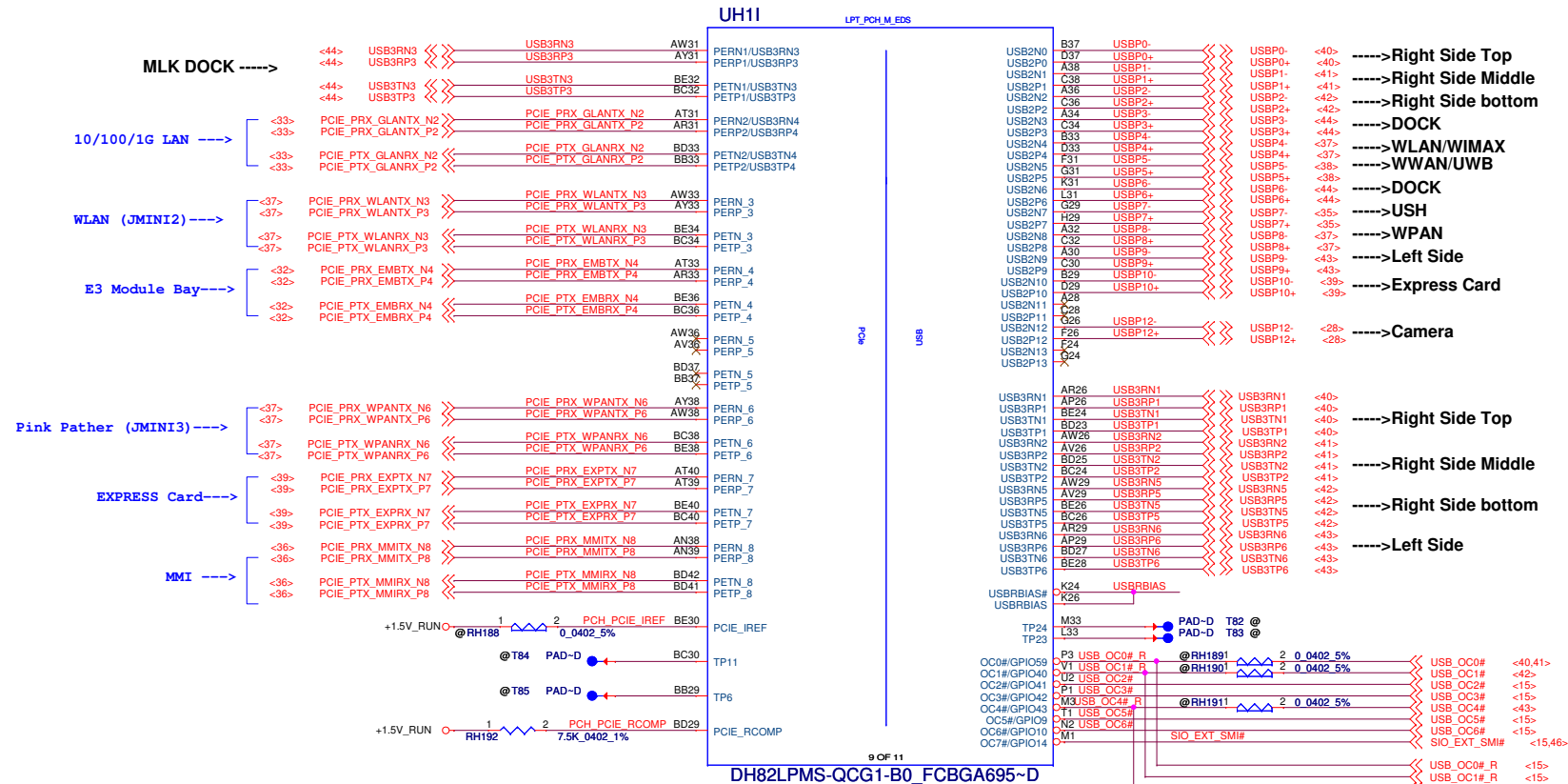
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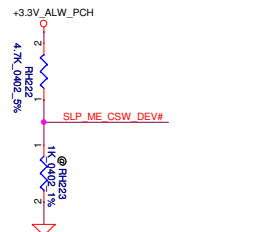
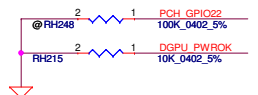
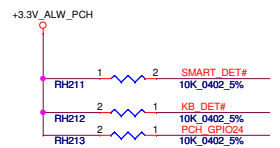
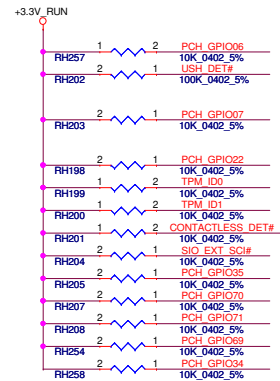
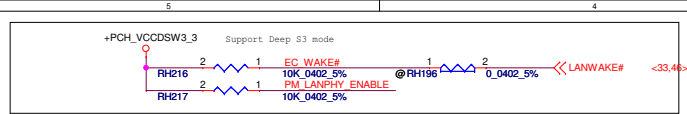


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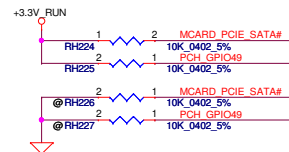
Compal Electronics, Inc.	
Title PCH (5/9)	
Size	Document Number
LA-9411P	
Date: Wednesday, April 10, 2013	Sheet 19 of 77

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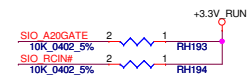
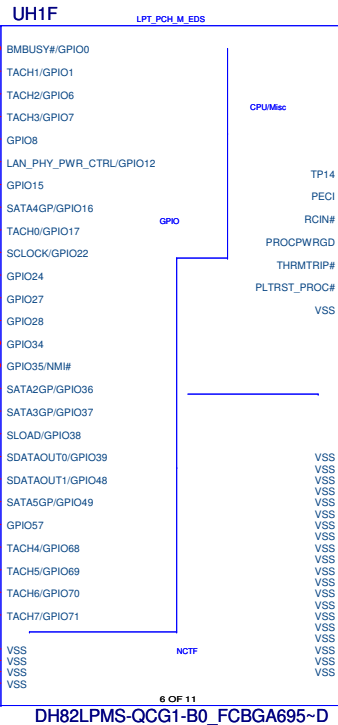
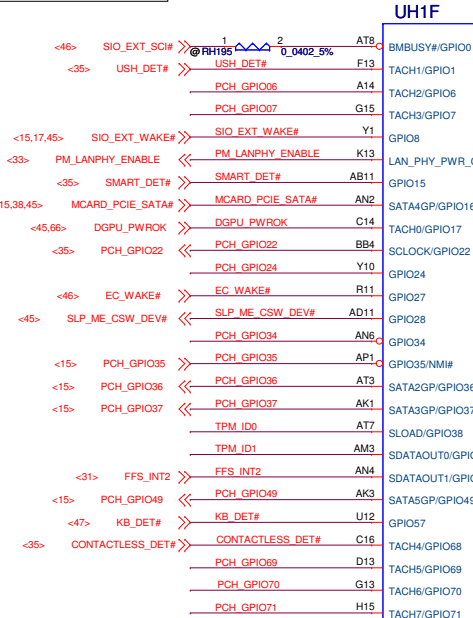
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PLL ON DIE VR ENABLE
ENABLED - HIGH(DEFAULT)
DISABLED - LOW

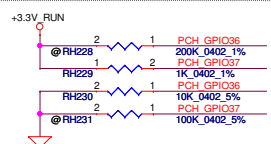


Config	GPIO16,49
USB X4,PCIEX8,SATAx6	11
* USB X6,PCIEX8,SATAx4	01



CRB1.2 already change to GND directly at UH1.A44, B45, BD1 pins

PCH_GPIO37
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.



SATA2GP/GPIO36, SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER PLRST_N DE-ASSERTS).
NOTE: THIS SIGNAL SHOULD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals					
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3		
				(00)	(00)							(00)	(00)						
				USB3 3	USB3 4							PCIE 1	PCIE 2						
				(01)	(01)							(01)	(01)						

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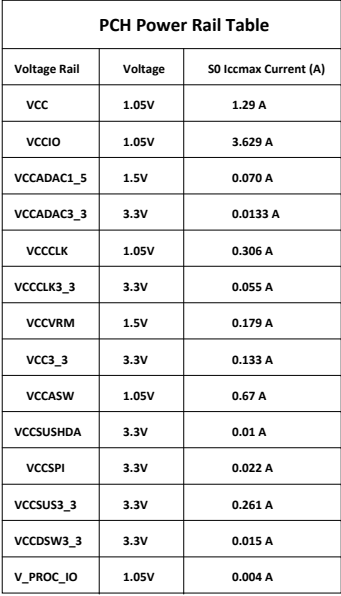
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Title			
PCH (6/9)			
Size	Document Number		Rev
	LA-9411P		1.0
Wednesday, April 10, 2013 10:20 AM			

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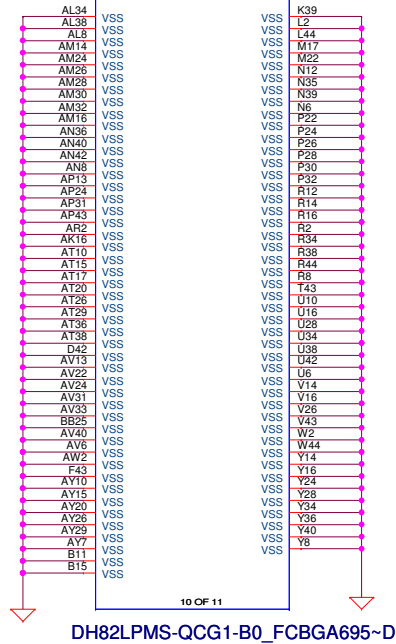
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Size		Document Number						Rev	
		LA-9411P						1.0	
Date:			Wednesday, April 10, 2013			Sheet		21 of 77	

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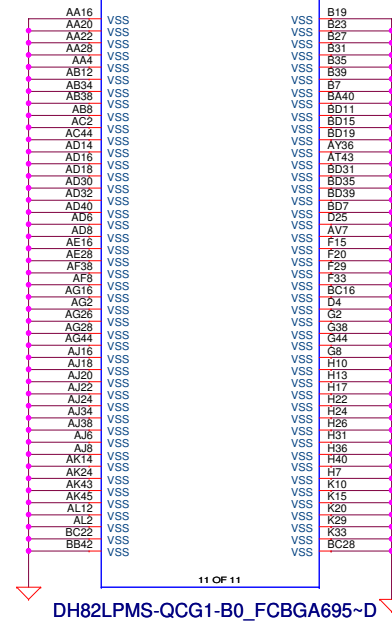
UH1J

LPT_PCH_M_EDS



UH1K

LPT_PCH_M_EDS



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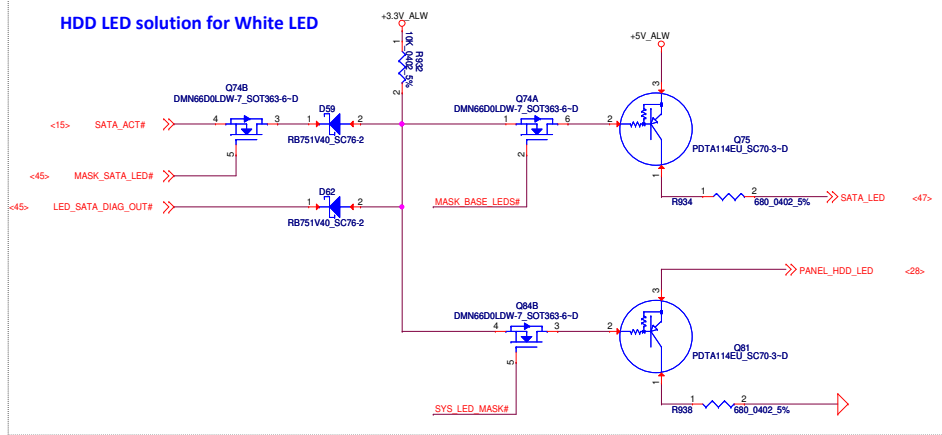
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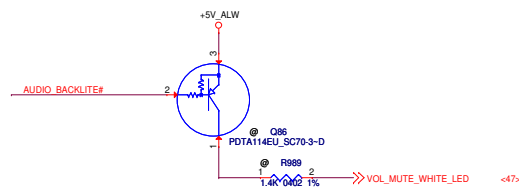
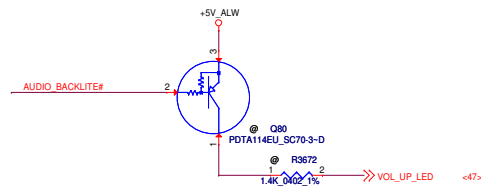
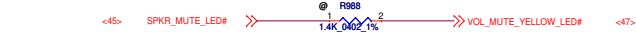
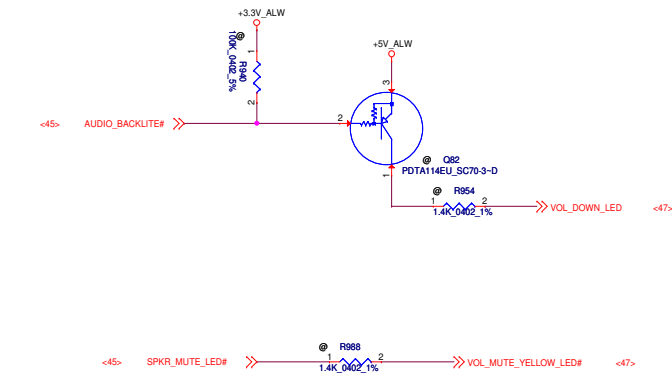
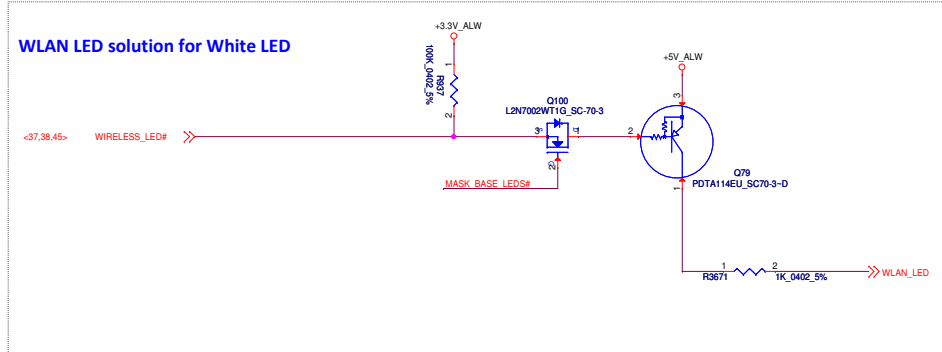
Compal Electronics, Inc.

Title			
PCH (9/9)			
Size	Document Number		Rev
	LA-9411P		1.0
Date:	Wednesday, April 10, 2013		Sheet 23 of 77

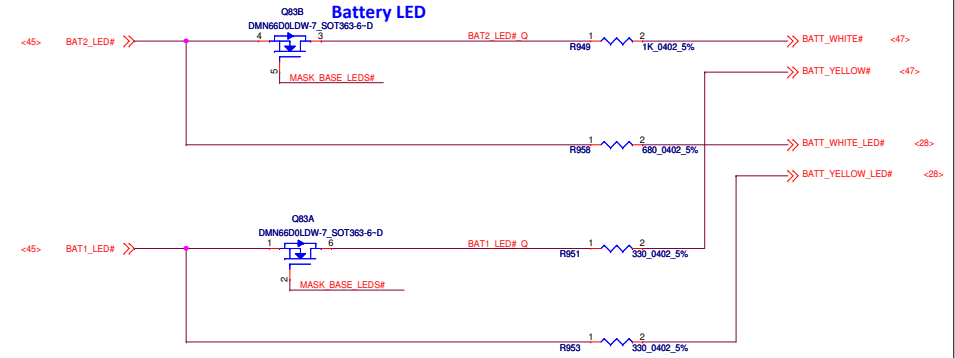
HDD LED solution for White LED



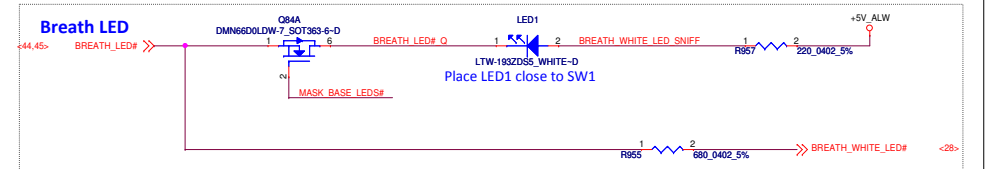
WLAN LED solution for White LED



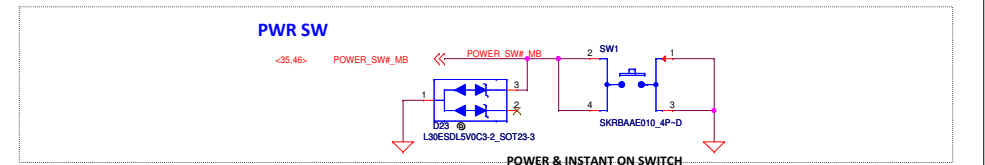
Battery LED



Breath LED



PWR SW

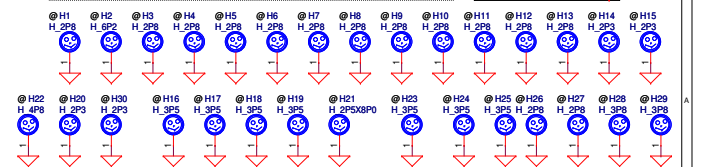
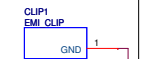


LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark



EMI CLIP



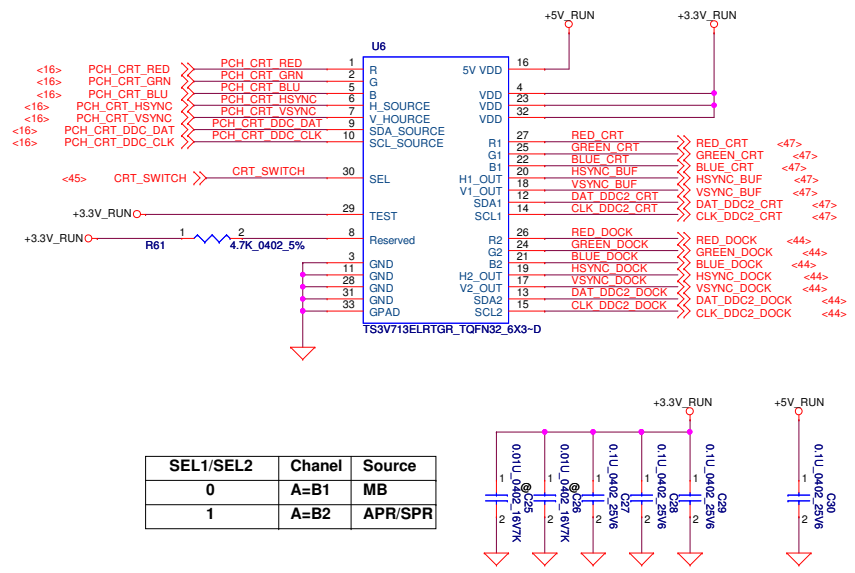
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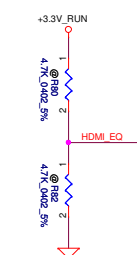
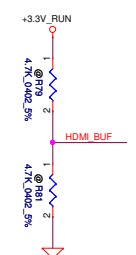
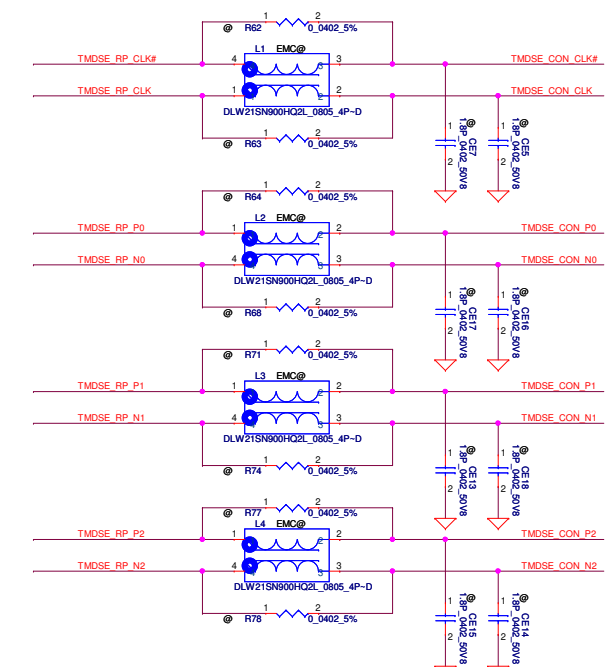
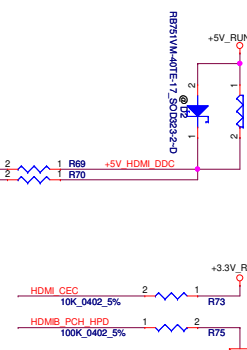
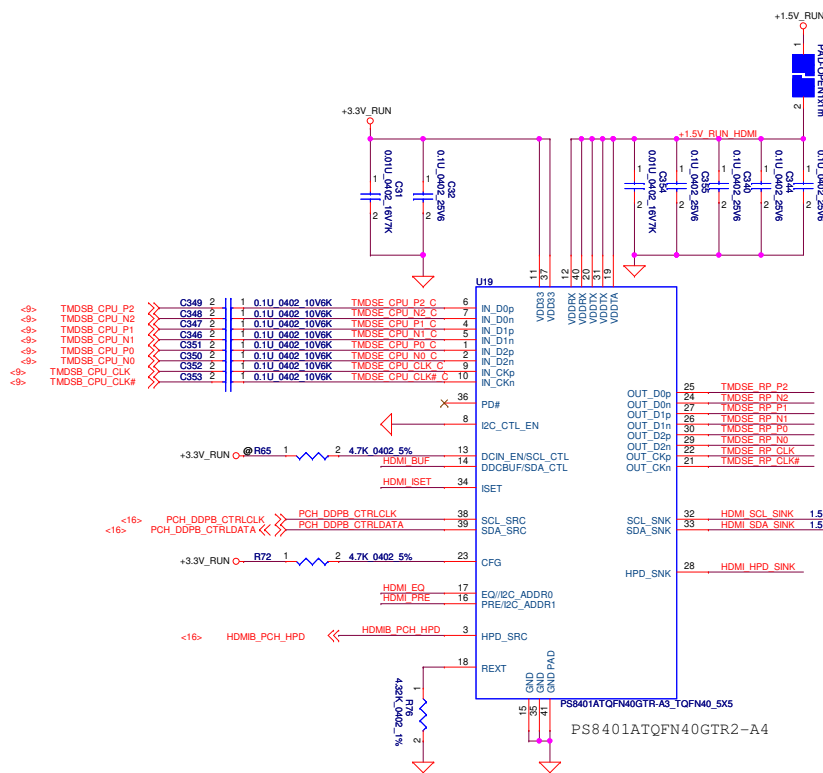
Compal Electronics, Inc.	
Title: PWR SW/LED/PAD/ME	
Size: Document Number	Rev: 1.0
LA-9411P	
Date: Wednesday, April 10, 2013	Sheet 24 of 77

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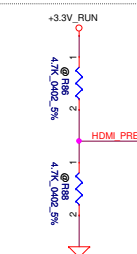
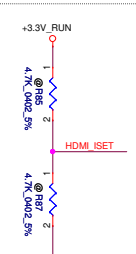
SW for MB/DOCK





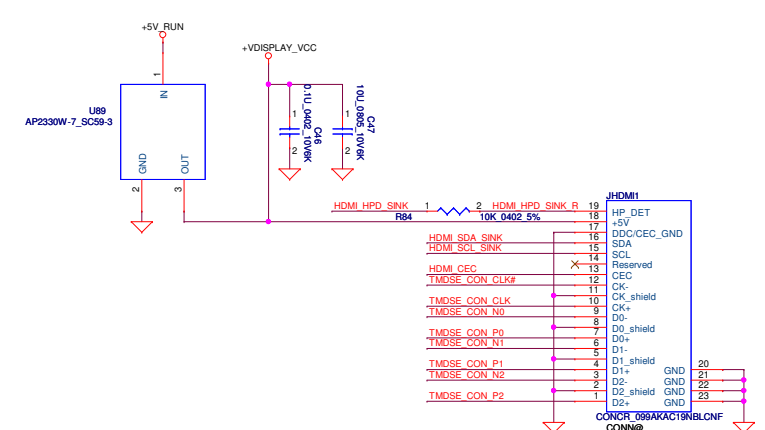
Enable active DDC buffer; Internal pull up at ~150kΩ, 3.3V I/O
 L: default, passive DDC pass-through
 H: active DDC buffer with default threshold
 M: passive DDC pass-through with internal ~10KΩ pull up

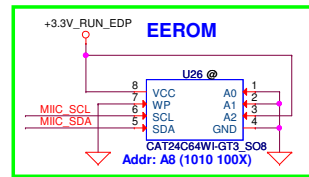
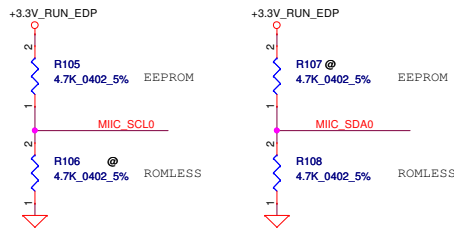
Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
 L: programmable EQ for channel loss up to 5.3dB
 H: programmable EQ for channel loss up to 10dB
 M: programmable EQ for channel loss up to 14dB



TMDs output swing adjustment; Internal pull down at ~150kΩ, 3.3V I/O.
 L: default
 H: increase +13%
 M: reduce -13%

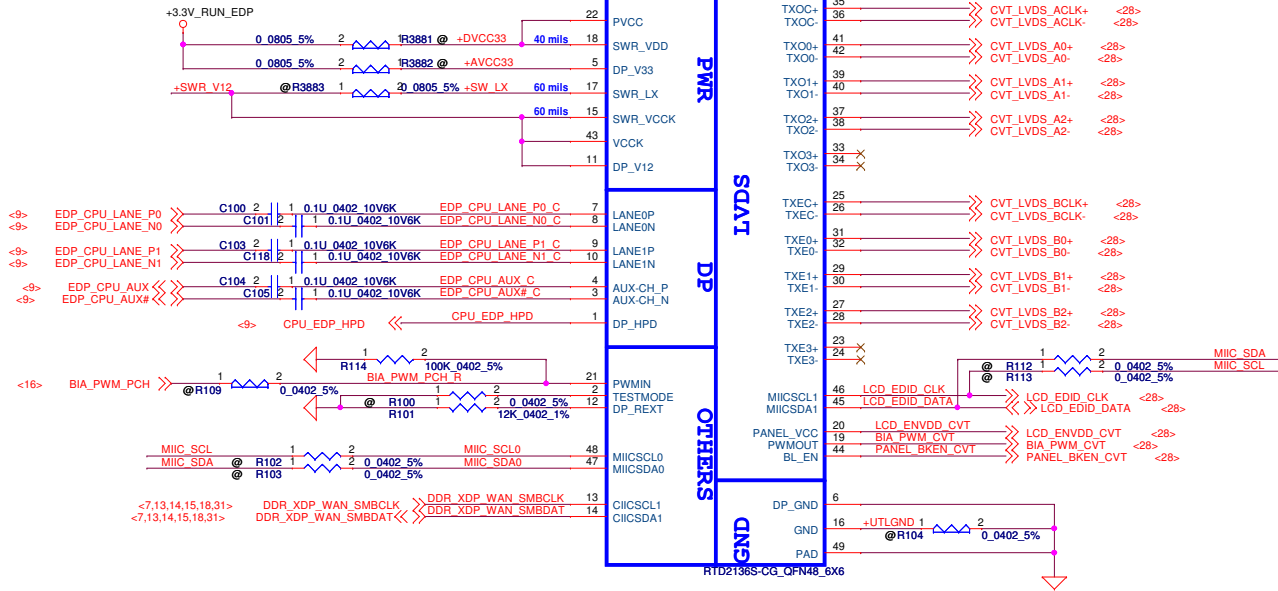
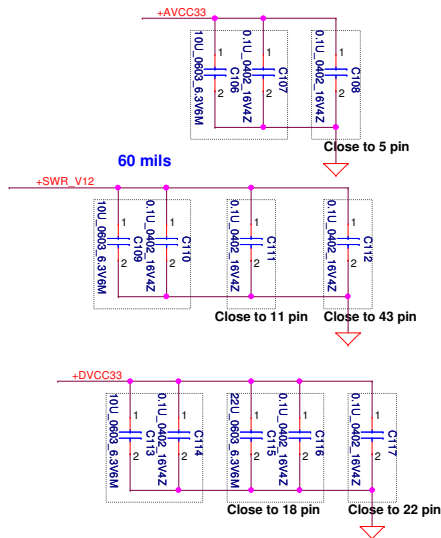
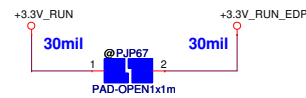
Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
 L: no pre-emphasis
 H: 1.6dB pre-emphasis
 M: 3.0dB pre-emphasis





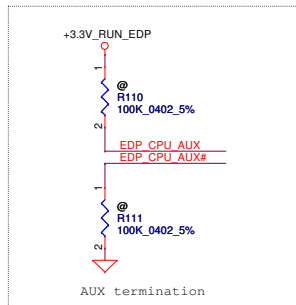
Power Consumption:

Pin5 (DPV33) < 20mA
 Pin 11 (DPV12) < 100mA
 Pin 15 (SWR_VCC) < 100mA (layout trace > 60 mil)
 Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
 Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
 Pin 22 (PVCC) < 50 mA
 Pin 43 (VCC) < 50mA



Symbol need to update

1. RTD2136S:SA00004NW10 Populated R102, R103, R107; De-populated R108
- *** 2. RTD2136R SA000067100 : De-Populated R102, R103, R107; Populate R108;



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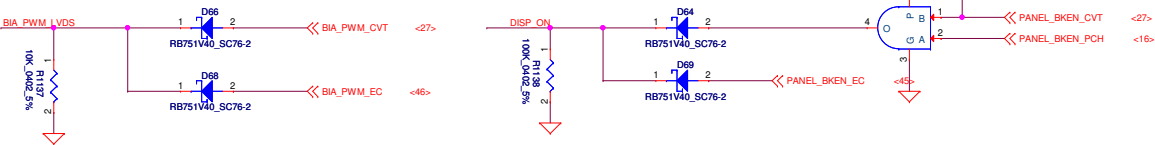
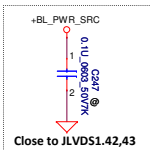
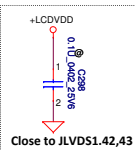
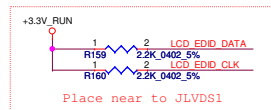
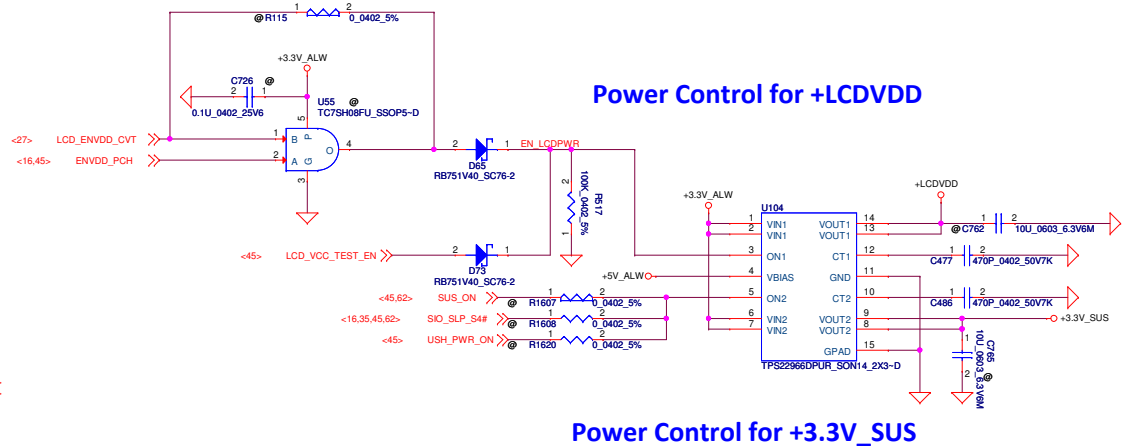
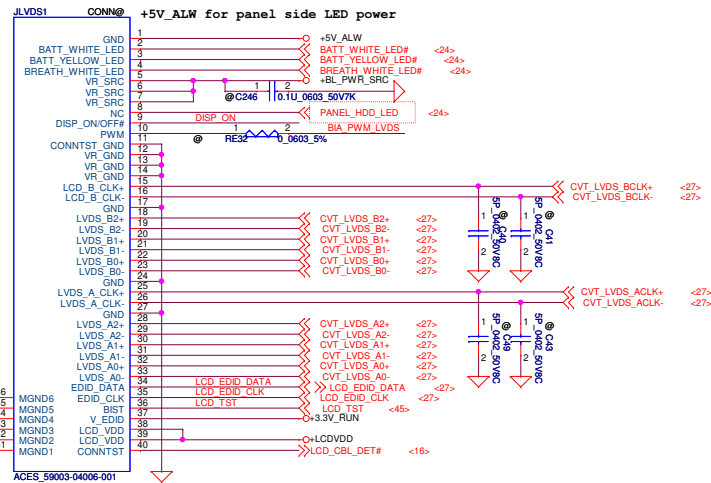
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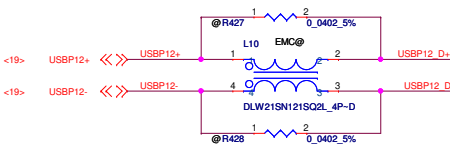
eDP to LVDS CONVERTER			
Title	Document Number	Rev	1.0
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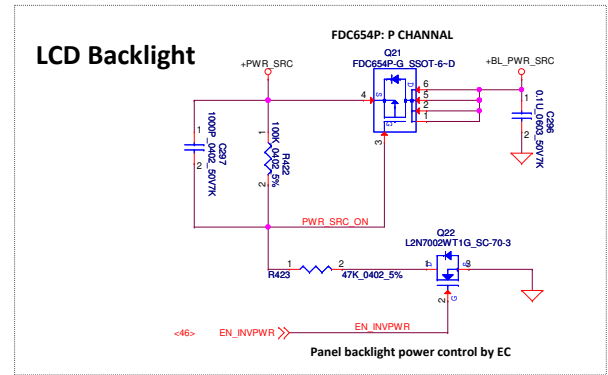
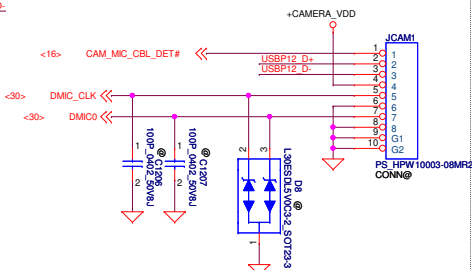
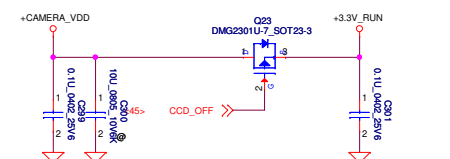
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For Webcam



Webcam PWR CTRL

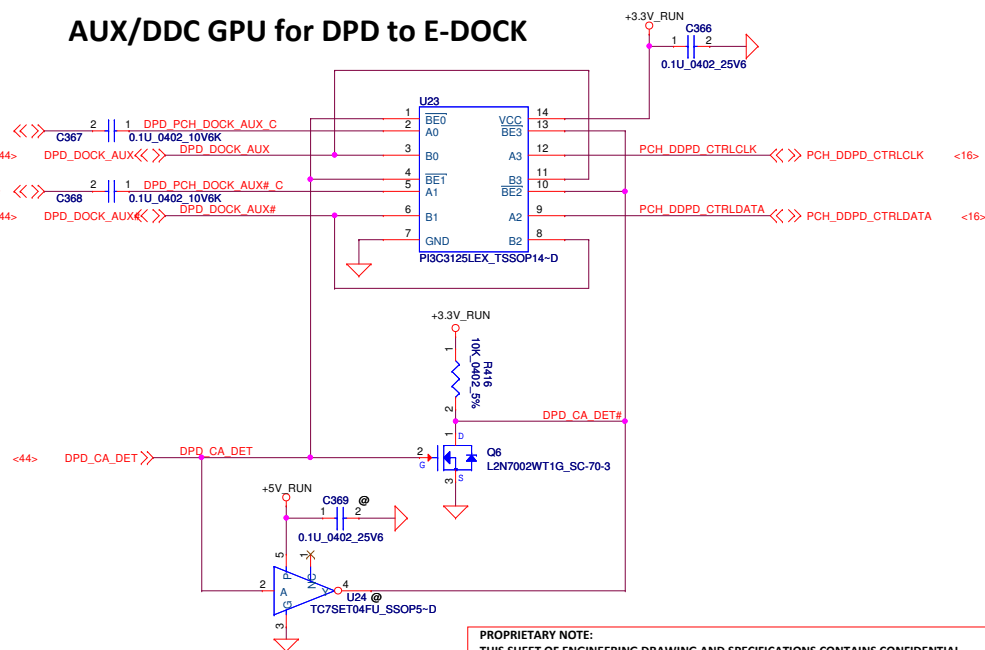


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Size	Document Number	LA-9411P	
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AUX/DDC GPU for DPD to E-DOCK

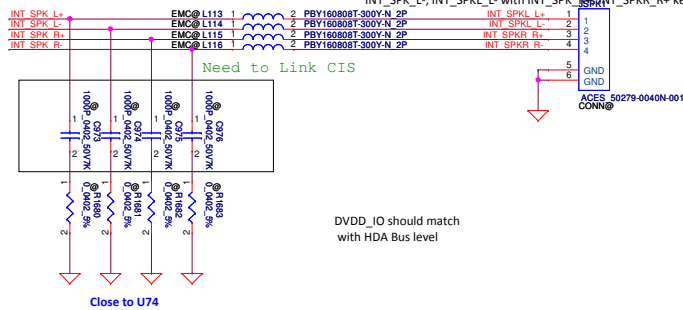


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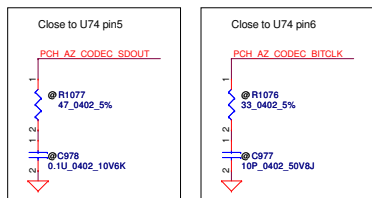
Sheet 29 of 77

Internal Speakers Header

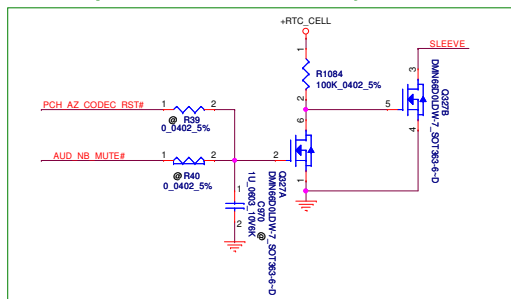
INT_SPK_L+, INT_SPK_L- :40 mils trace, keep 10mils spacing
INT_SPK_L+, INT_SPK_L- :40 mils trace, keep 10mils spacing
INT_SPK_R+, INT_SPK_R- :40 mils trace, keep 10mils spacing
INT_SPK_L-, INT_SPK_L- with INT_SPK_R+ keep 20mils spacing



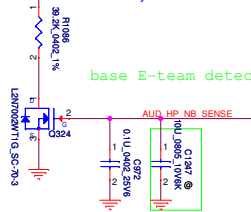
DVDD_IO should match with HDA Bus level



When no external power, it Sleeve will be floating mode and no reference GND.

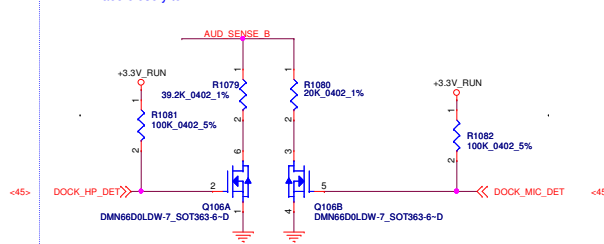


Place closely to Pin 13.



Add for solve pop noise and detect issue

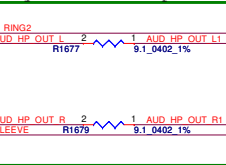
Place closely to Pin 14



RING2_L, RING2, AUD_HP_OUT_L2, AUD_HP_OUT_L1, AUD_HP_OUT_L, AUD_HP_OUT_R2, AUD_HP_OUT_R1, AUD_HP_OUT_R, EXT_MIC, SLEEVE Trace width to 15mils.

Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

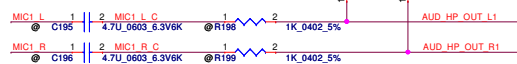
Symbol need update



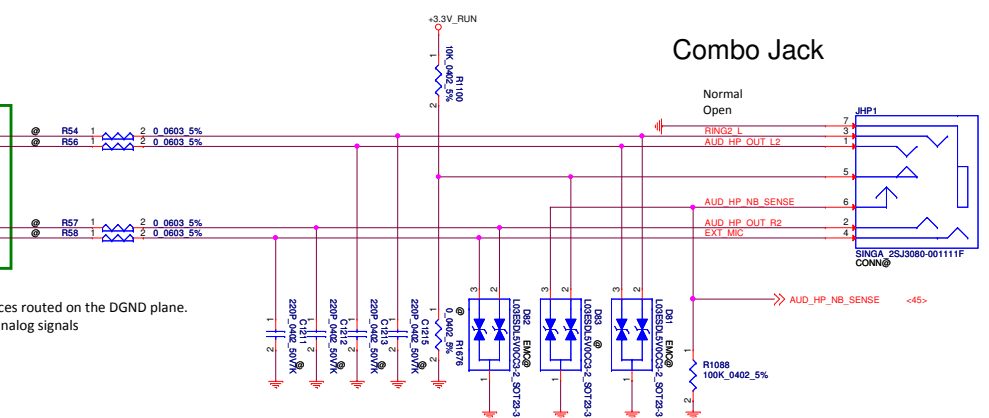
Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK

support universal Jack



Combo Jack



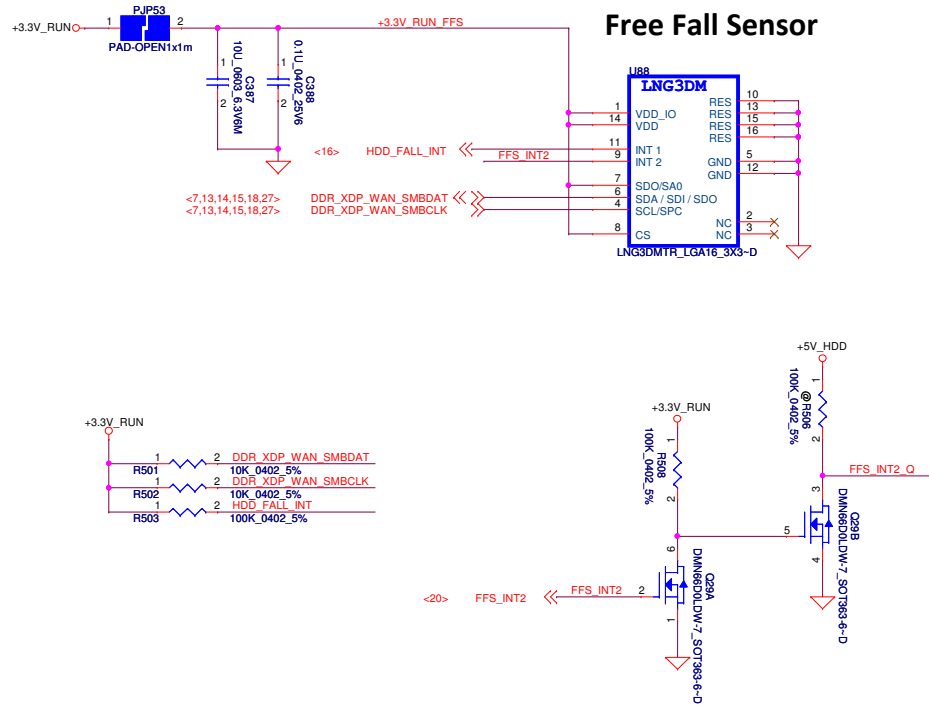
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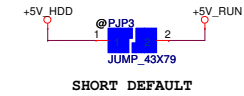
Codec

LA-9411P

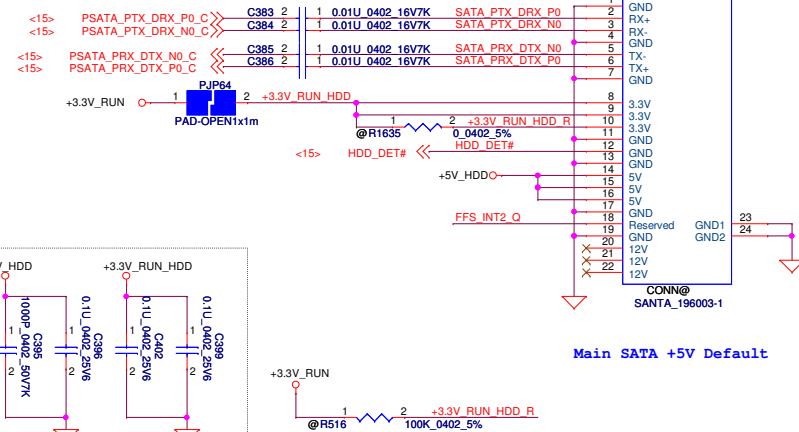
Date: Wednesday, April 10, 2013 Sheet 30 of 77



HDD PWR



HDD CONN



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HDD

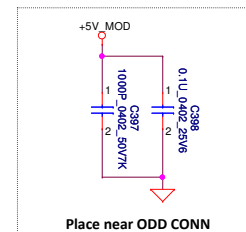
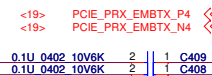
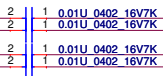
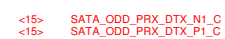
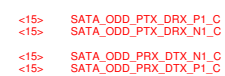
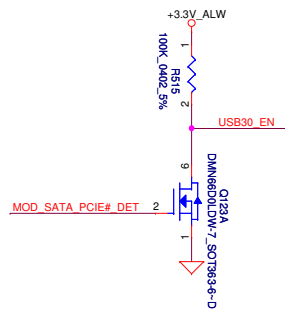
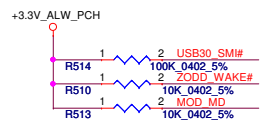
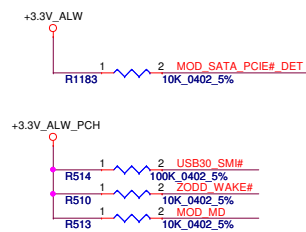
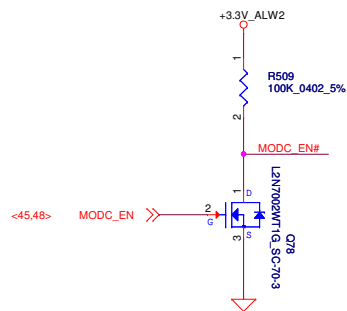
LA-9411P

Rev 1.0

Date: Wednesday, April 10, 2013 Sheet 31 of 77

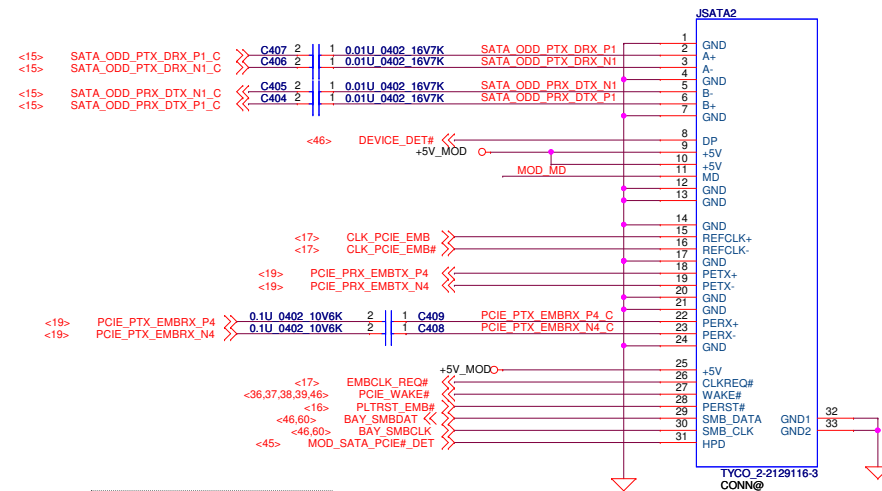
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Place near ODD CONN

ODD CONN



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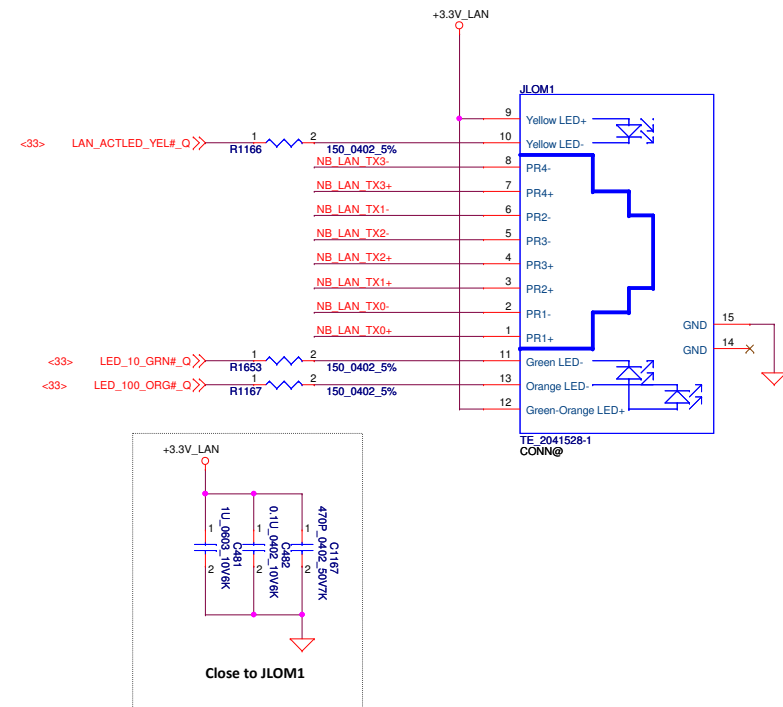
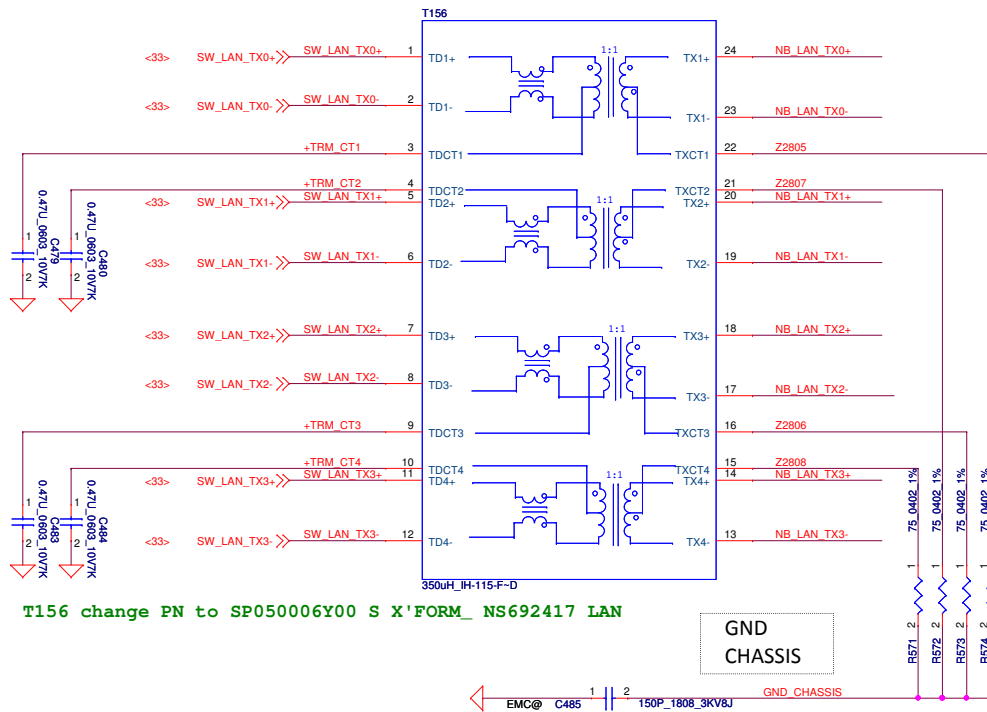
ODD

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Rev
1.0

Date: Wednesday, April 10, 2013 Sheet 32 of 77

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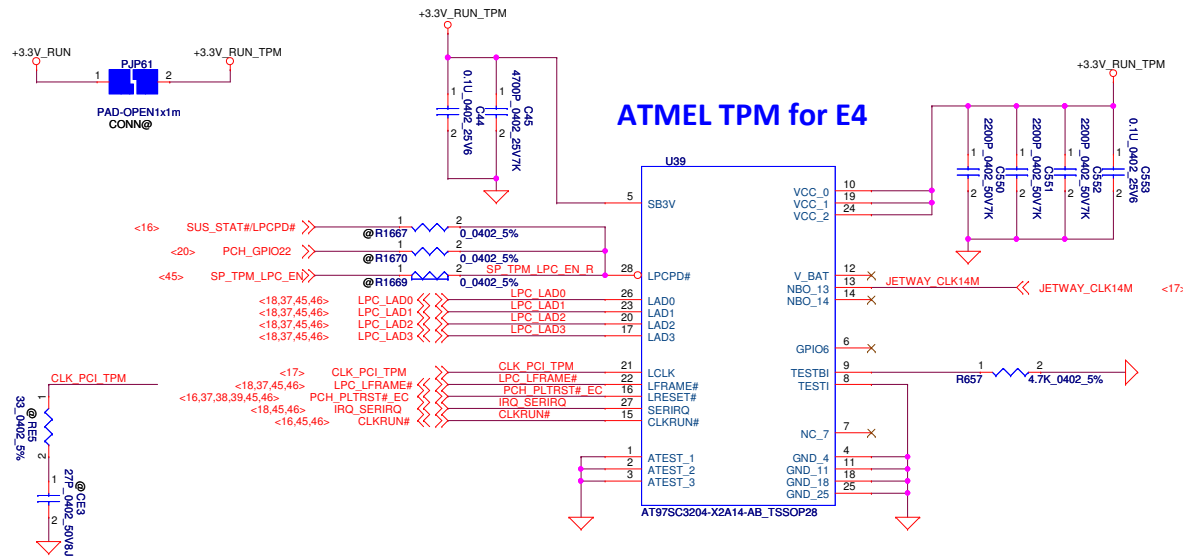


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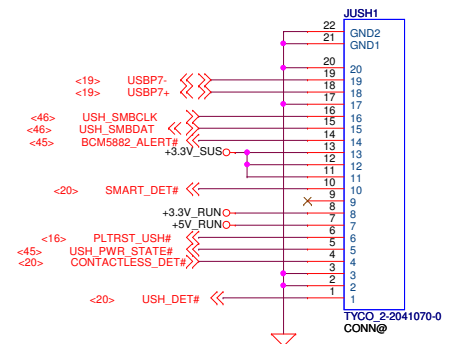
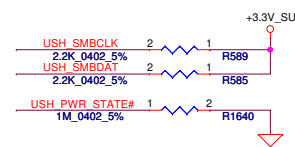
	Compal Electronics, Inc.		
	Title		
	RJ45 Conn		
	Size	Document Number	Rev
		LA-9411P	1.0
	Date: Wednesday, April 10, 2013	Sheet 34 of 77	

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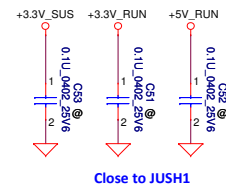
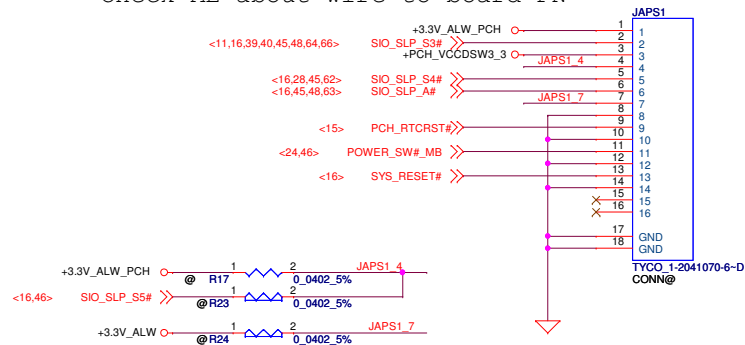
www.vinafix.vn



USH CONN



Check ME about wire to board PN

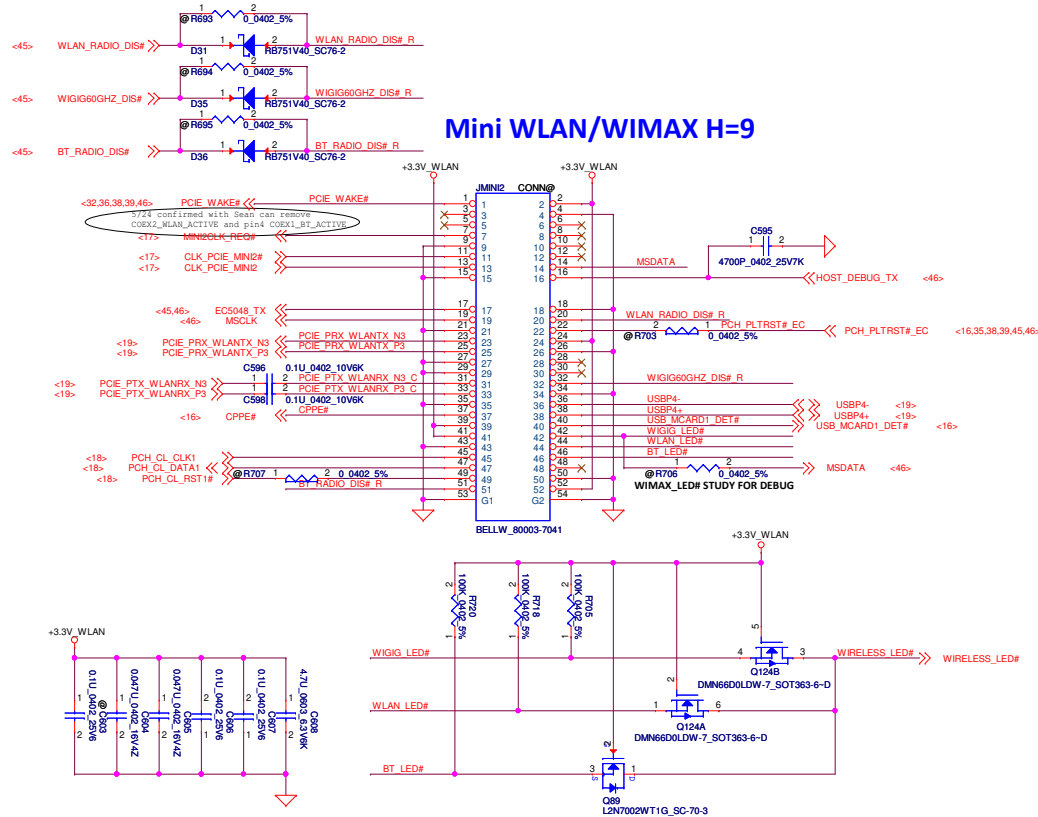


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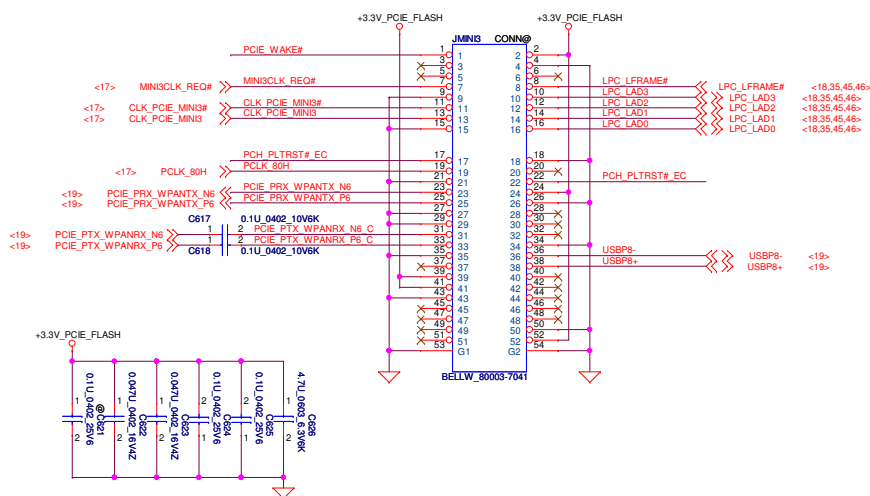
Compal Electronics, Inc.	
Title	
Size	
Document Number	Rev
LA-9411P	1.0
Date: Wednesday, April 10, 2013	Sheet 35 of 77

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1/2 Minicard Pink Pather/60GHz Card H=9



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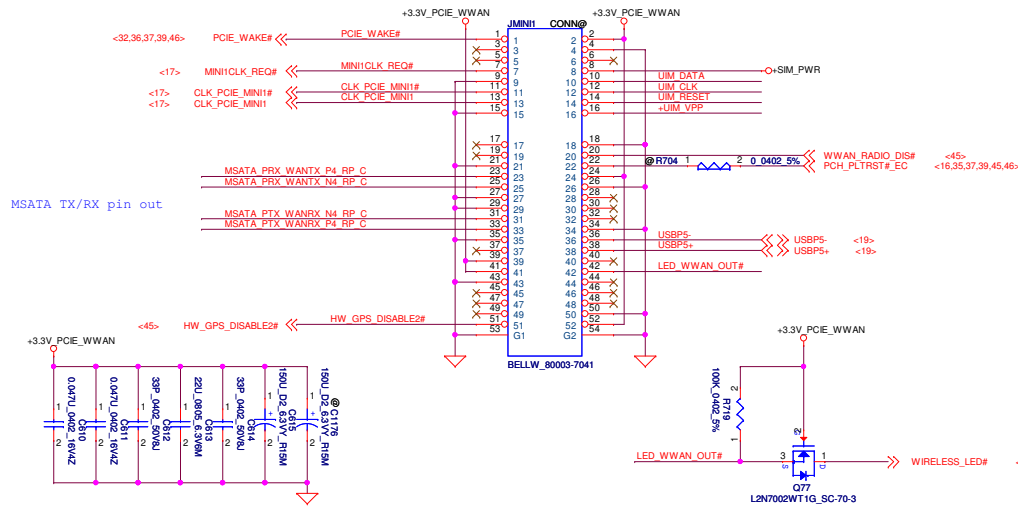
Compal Electronics, Inc.



Title	WLAN/Pink Pather Mini Card		
Size	Document Number	LA-9411P	
Date	Wednesday, April 10, 2013	Sheet	37 of 77
Rev	1.0		

www.Victor.com

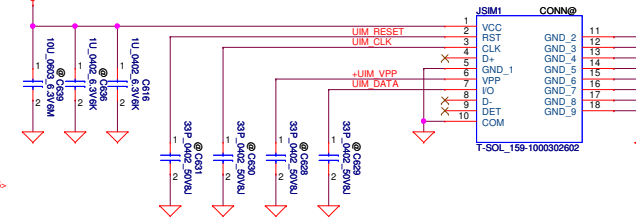
Mini WWAN/GPS/LTE/UWB H=9



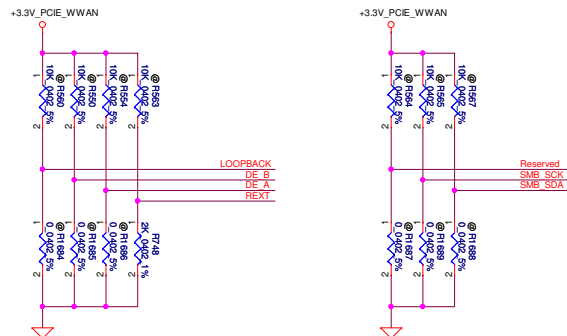
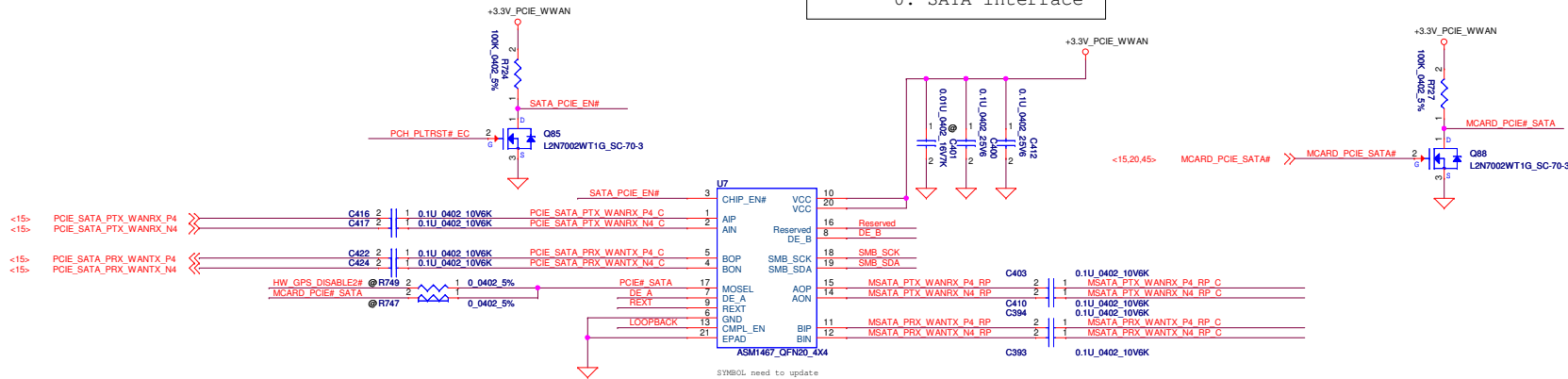
- (1) Wake Enabled and Active
(2) Wake NOT Enabled nor Active

PWR Rail	Voltage Tolerance	D0-D2&D3 hot Power		D3 cold Power	
		Peak (mA)	Typ (mA)	Peak (mA)	Typ (mA)
+3.3V_PCIE_WWAN	+/-9%	2750	800	800 (1) 5 (2)	150 (1) 5 (2)

SIM Card Push-Push



MOSEL 1: PCIE interface
0: SATA interface



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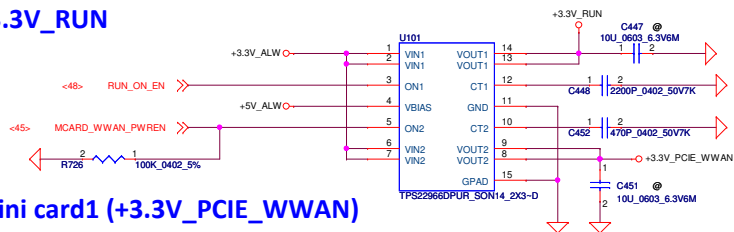
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WWAN Mini Card

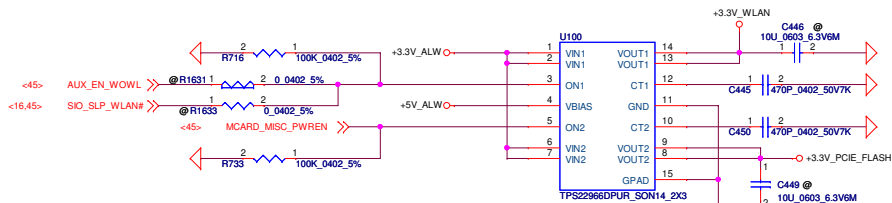
Title	Document Number	Rev
LA-9411P	1.0	1.0
Date: Wednesday, April 10, 2013	Sheet 38 of 77	

Power Control for +3.3V_RUN



Power Control for Mini card1 (+3.3V_PCIE_WWAN)

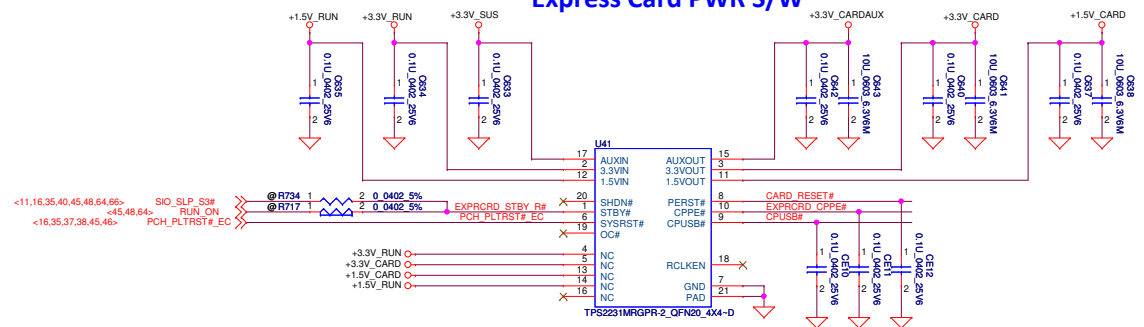
Power Control for Mini card2 (+3.3V_WLAN)



Power Control for Mini card3 (+3.3V_PCIE_FLASH)

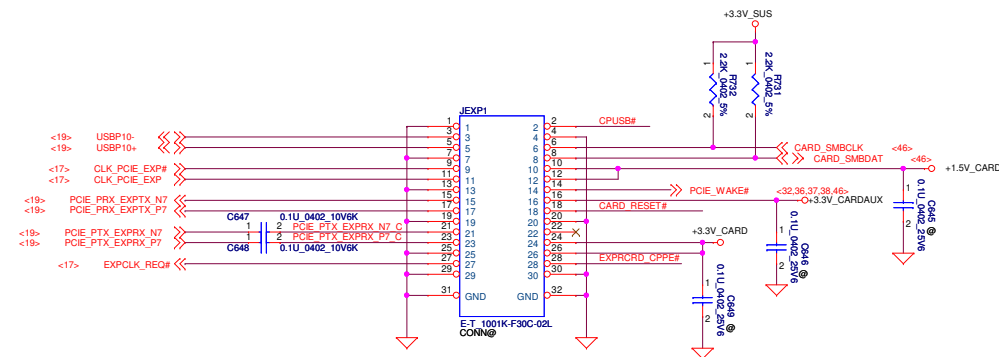


Express Card PWR S/W



Express Card Conn.

Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part



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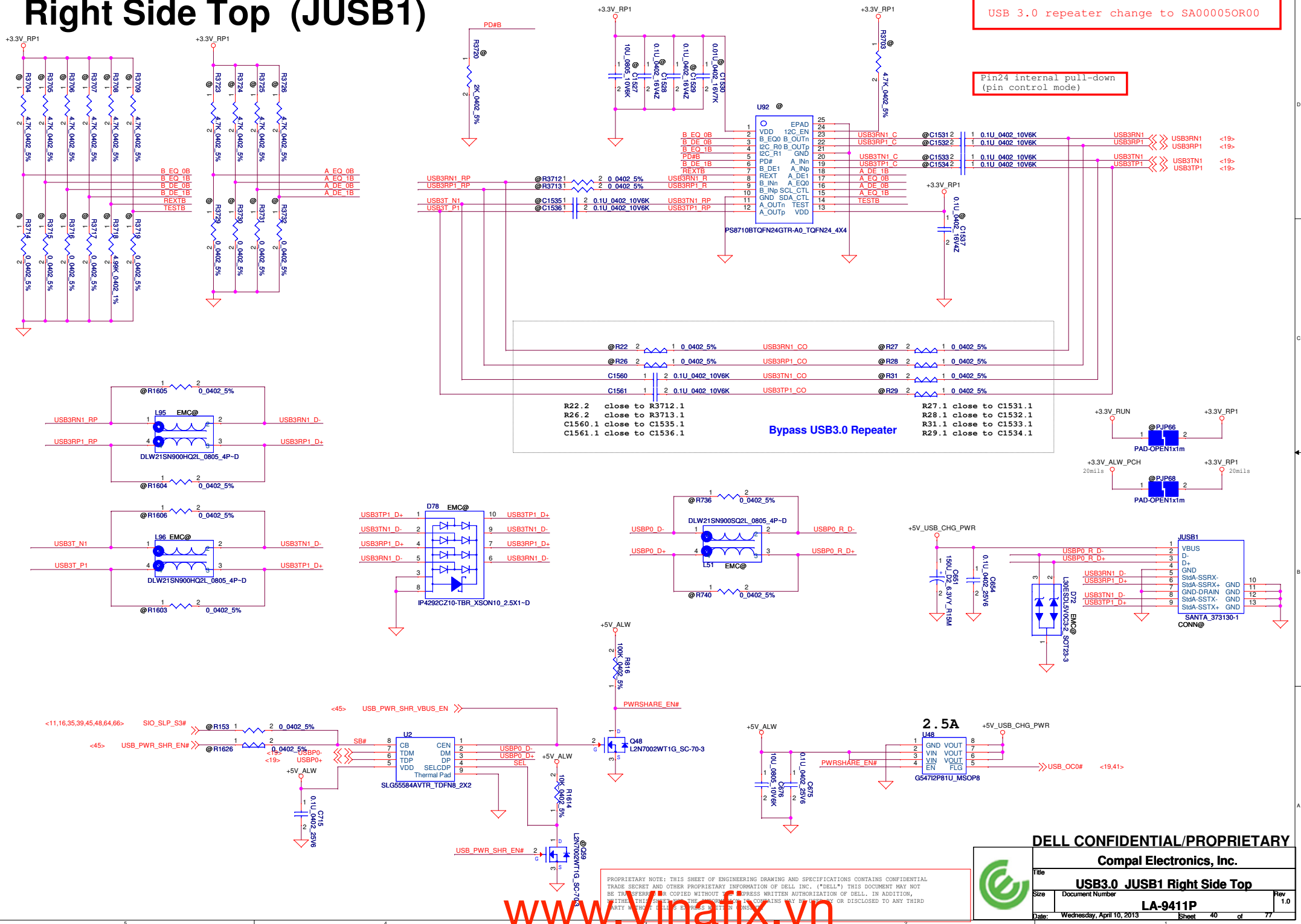
PCIE-SATA SW / PCIE PWR

Size Document Number LA-9411P Rev 1.0

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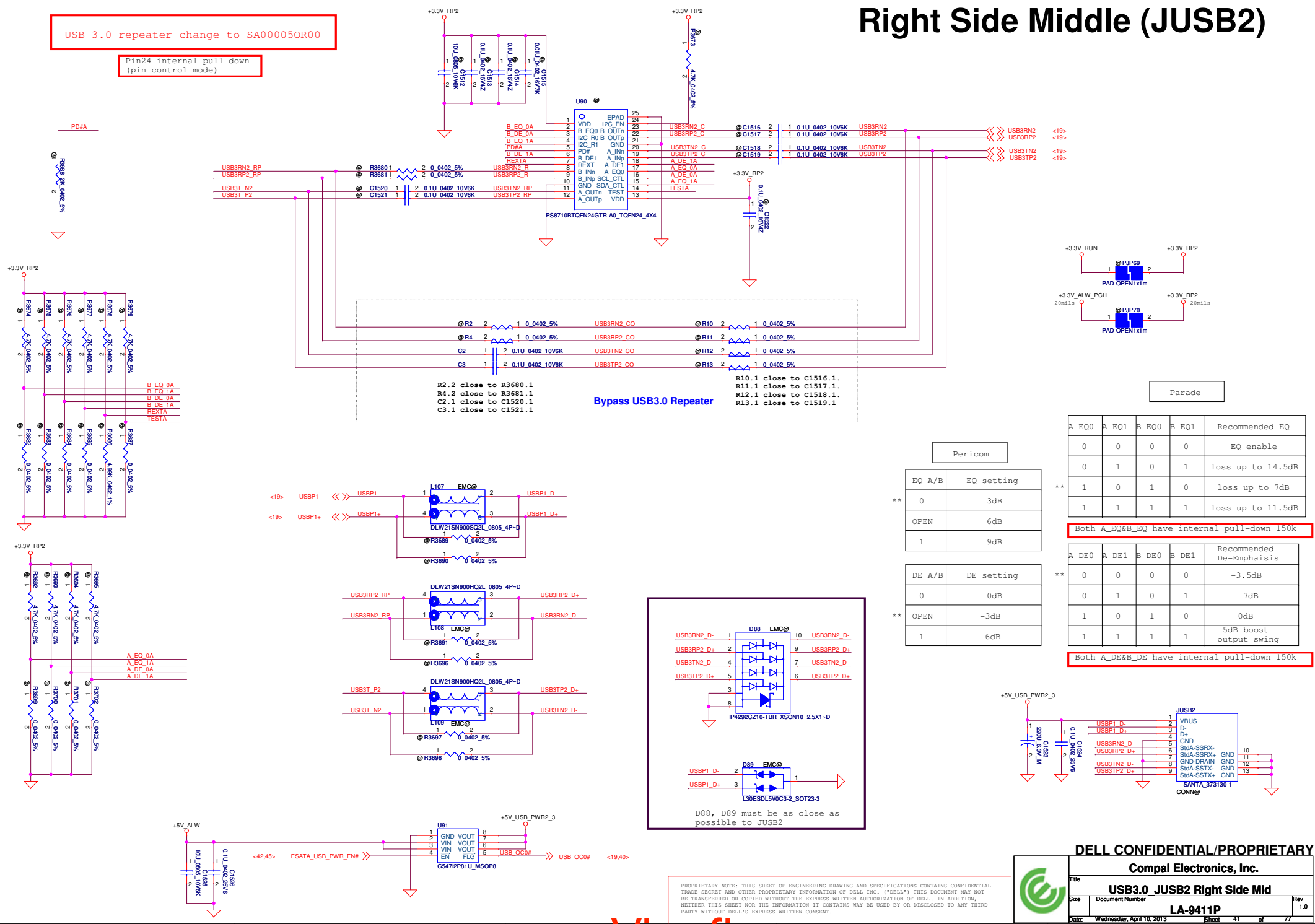
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Right Side Top (JUSB1)



USB 3.0 repeater change to SA000050R00

Pin24 internal pull-down
(pin control mode)



USB 3.0 repeater change to SA000050R00

Pin24 internal pull-down
(pin control mode)



USB3.0 JUSB3 Right Side bot

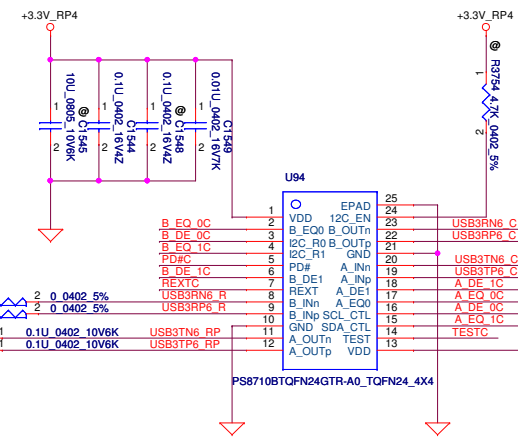
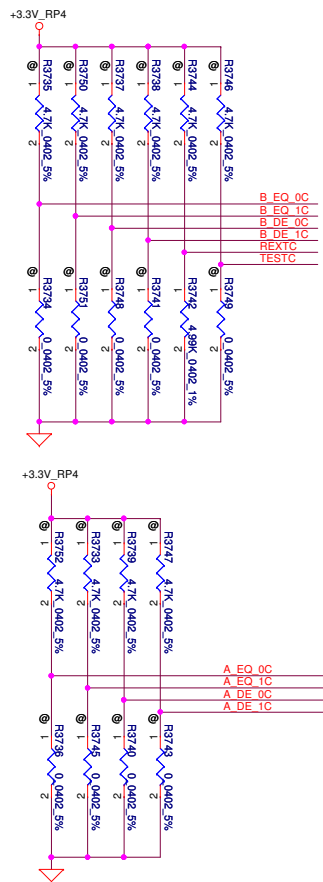
LA-9411B

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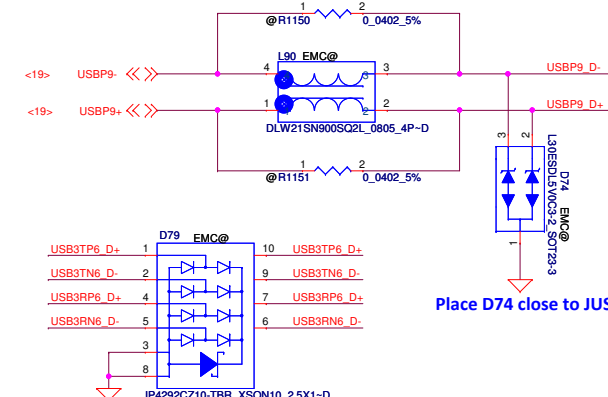
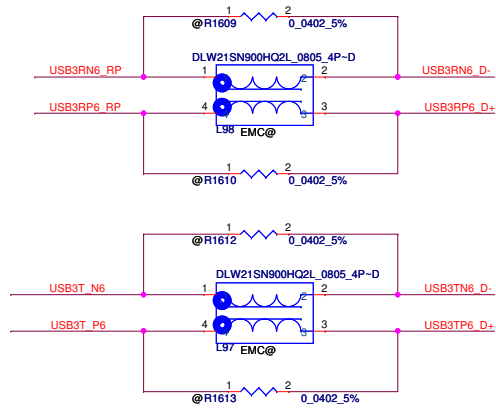
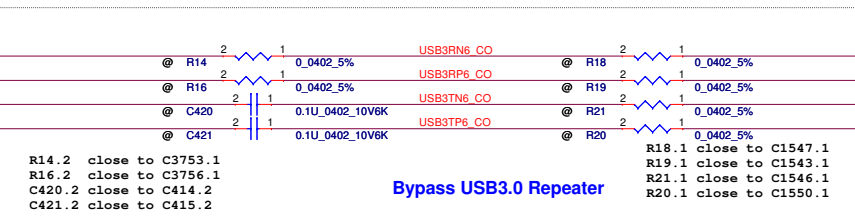
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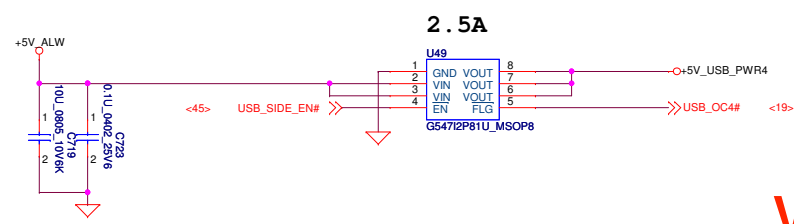
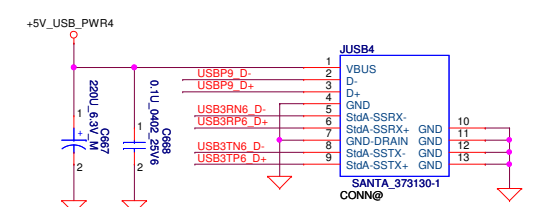


USB 3.0 repeater change to SA00005OR00

Pin24 internal pull-down (pin control mode)



JUSB4



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USB3.0_JUSB4 Left Side

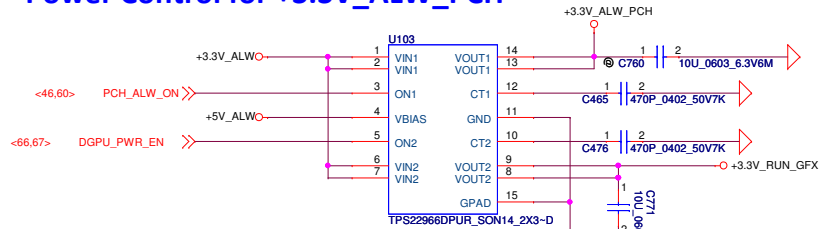
LA-9411P

Date: Wednesday, April 10, 2013 Sheet 43 of 77

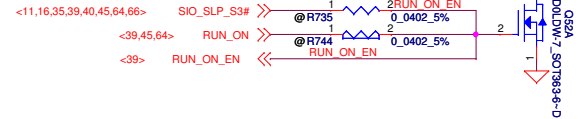
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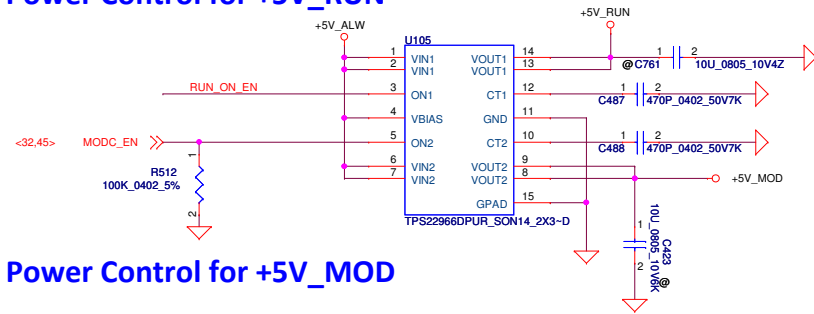
Power Control for +3.3V_ALW_PCH



Power Control for +3.3V_RUN_GFX

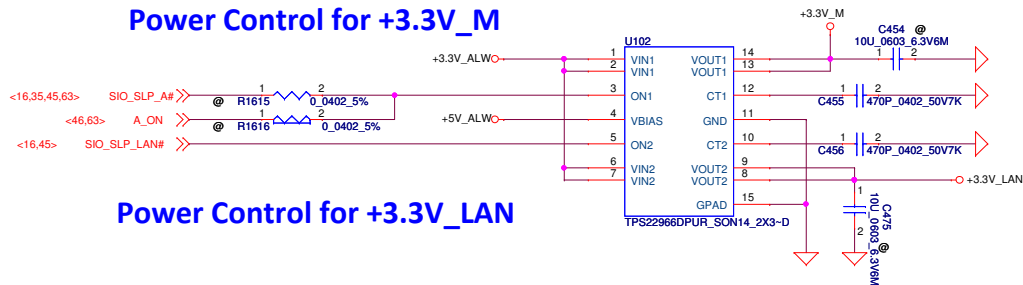


Power Control for +5V_RUN



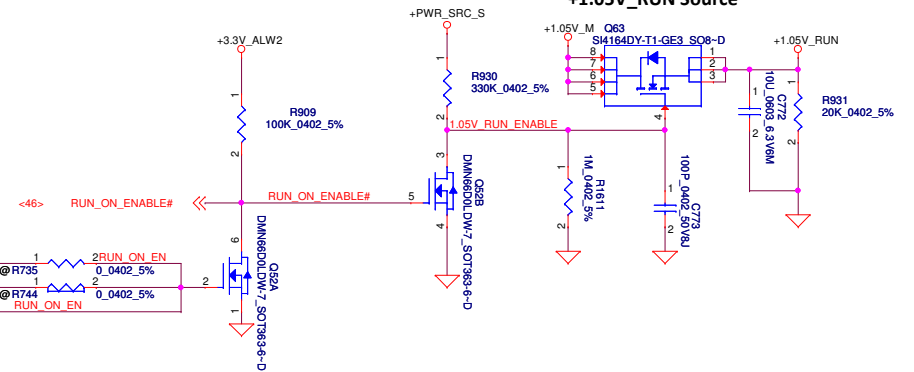
Power Control for +5V_MOD

Power Control for +3.3V_M



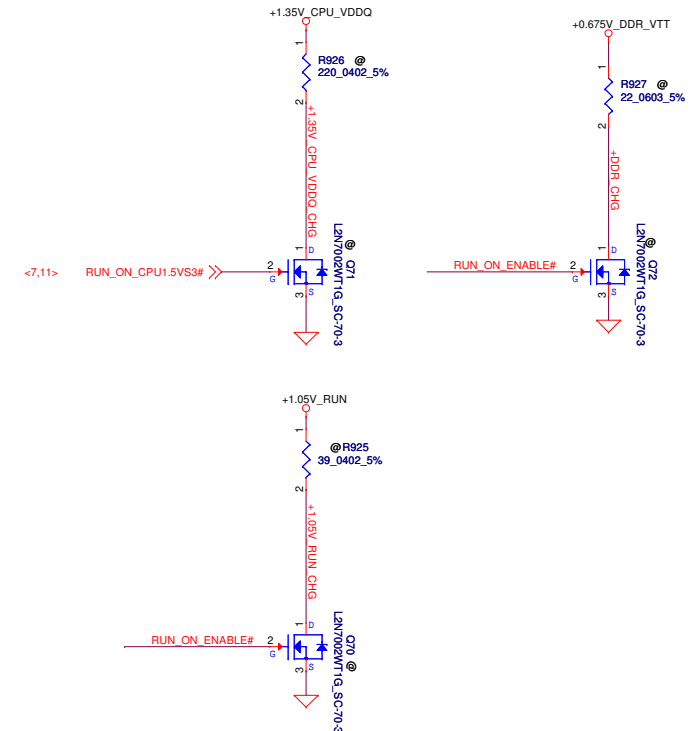
Power Control for +3.3V_LAN

DC/DC Interface



+1.05V_RUN Source

Discharge Circuit



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POWER CONTROL

LA-9411P

Wednesday, April 10, 2013

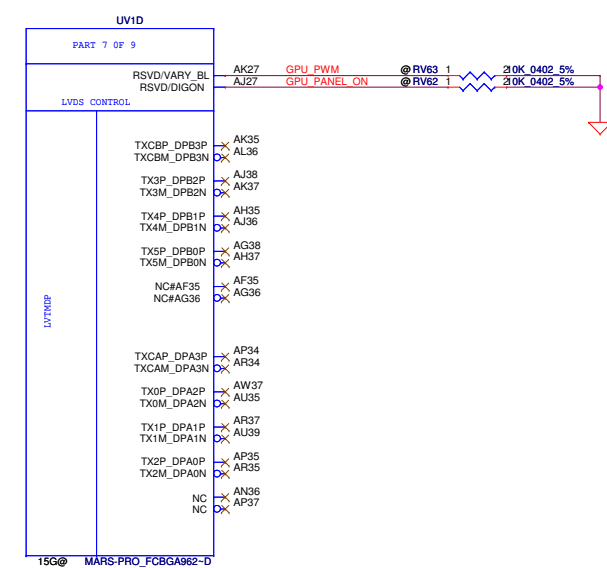
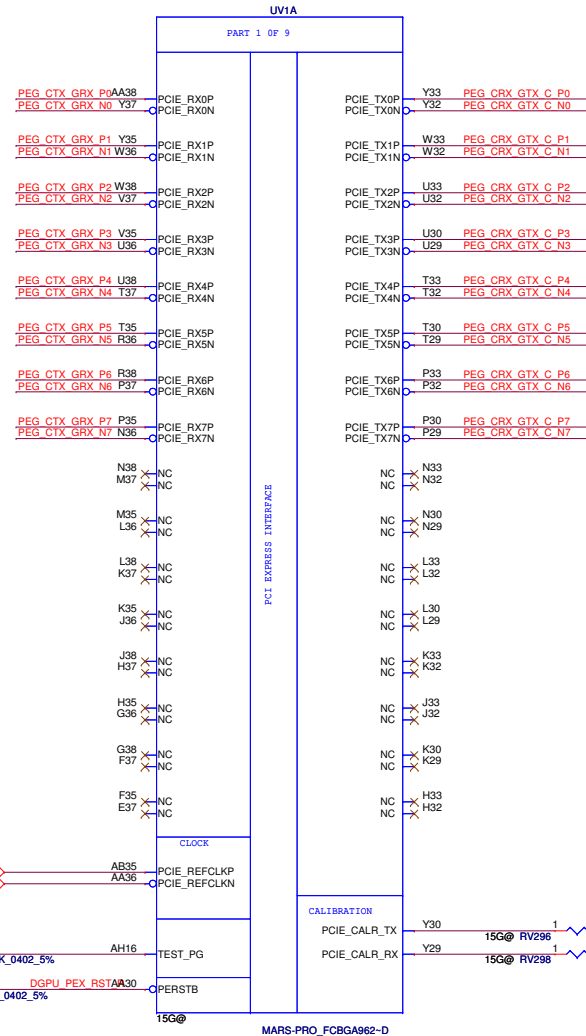
Sheet 48 of 77

Rev 1.0

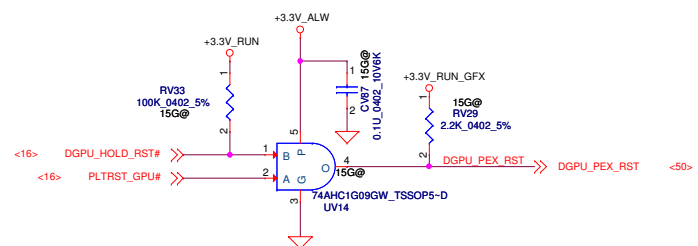
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PEG_CRX GTX_P0	15G@ CV1	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_P0
PEG_CRX GTX_N0	15G@ CV2	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_N0
PEG_CRX GTX_P1	15G@ CV4	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_P1
PEG_CRX GTX_N1	15G@ CV3	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_N1
PEG_CRX GTX_P2	15G@ CV5	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_P2
PEG_CRX GTX_N2	15G@ CV6	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_N2
PEG_CRX GTX_P3	15G@ CV7	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_P3
PEG_CRX GTX_N3	15G@ CV8	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_N3
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PEG_CRX GTX_P5	15G@ CV11	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_P5
PEG_CRX GTX_N5	15G@ CV12	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_N5
PEG_CRX GTX_P6	15G@ CV14	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_P6
PEG_CRX GTX_N6	15G@ CV15	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_N6
PEG_CRX GTX_P7	15G@ CV16	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_P7
PEG_CRX GTX_N7	15G@ CV17	2	1	0.22U 0402 16V7K	PEG_CRX GTX_C_N7



don't connect to PCH



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Compal Electronics, Inc.			
Title	MARX-PCIE		
Size	Document Number	LA-9411P	
Date	Wednesday, April 10, 2013	Sheet	49 of 77

CONFIGURATION STRAPS

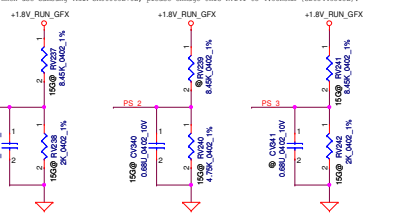
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE
GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 10K RESISTOR
X= DESIGN DEPENDANT
NA= NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	POE FULL TX OUTPUT SWING	0: 50% swing 1: full swing	X
TX_DEEMPH_EN	GPIO1	POE TRANSMITTER DE-EMPHASIS	0: enable 1: disable	X
RSVD	GPIO2	Advertises PCIe speed when compliance test	0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED		0
BF_VGA_EN	GPIO9	VGA ENABLED		0
RSVD	GPIO21	RESERVED		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X
ROMIDCFG(2)	GPIO(13:11)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX
VP_DEVICE_STRAP_ENA	VS2SYNC	IGNORE VIP DEVICE STRAPS		0
RSVD	HS2SYNC			0
RSVD	GENERICC			0
ALUD[1]	HS2NC	AD[0][1] AD[0][0] 0: 0 No audio function 1: 1 Audio for DisplayPort and HDMI if dongle is detected 2: 2 Audio for DisplayPort only 3: 3 Audio for both DisplayPort and HDMI		11
ALUD[0]	VS2NC			

AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL
RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND
NOT CONFLICT DURING RESET

PS_3_1(3:2:1) for MEMB	RV241_PU	RV242_PU	CV341
001: Nanya R502H24MP (1.35V)	8.45K	2K	NC
010: Samsung K4D2032SPD (1.35V)	4.53K	2K	NC

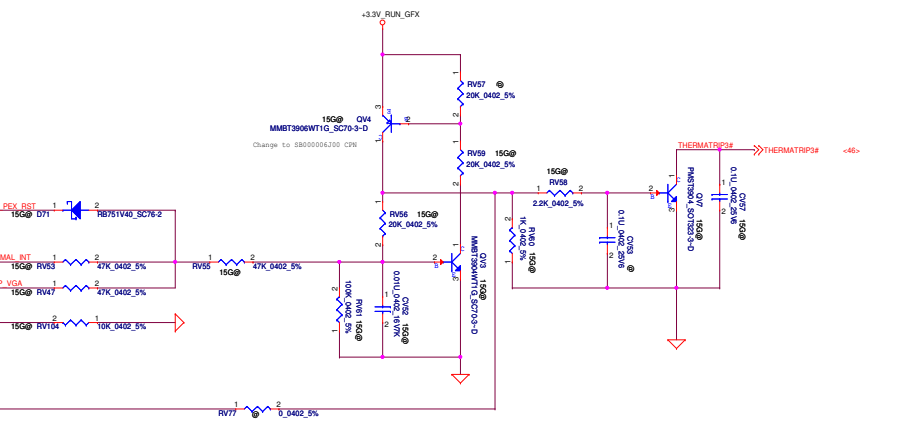


TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)

GPU_PWR_LEVEL	
LOW	Low Performance
HIGH	High Performance



Change to 58000006300 CPU

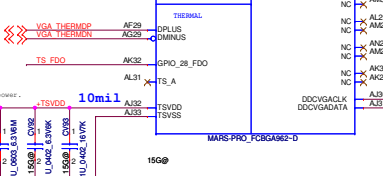
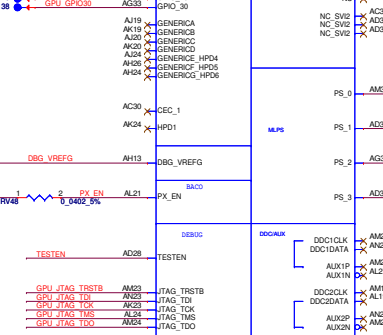
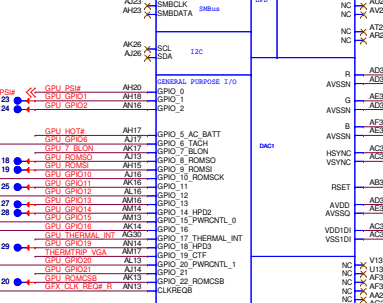
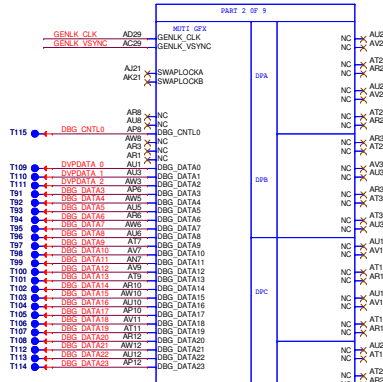
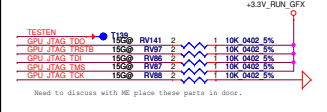
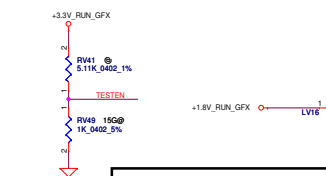
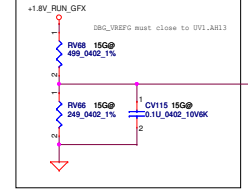
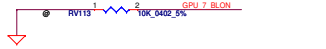
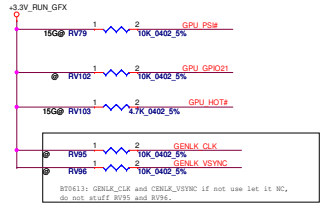


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MARX-GPIO,HDMI,DP,DAC
LA-9411P
Date: Wednesday, April 10, 2013 Sheet 80 of 77

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STRAPS

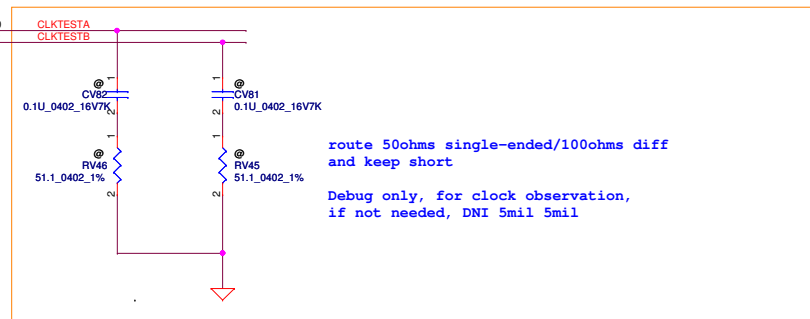
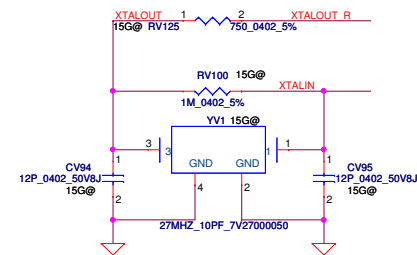
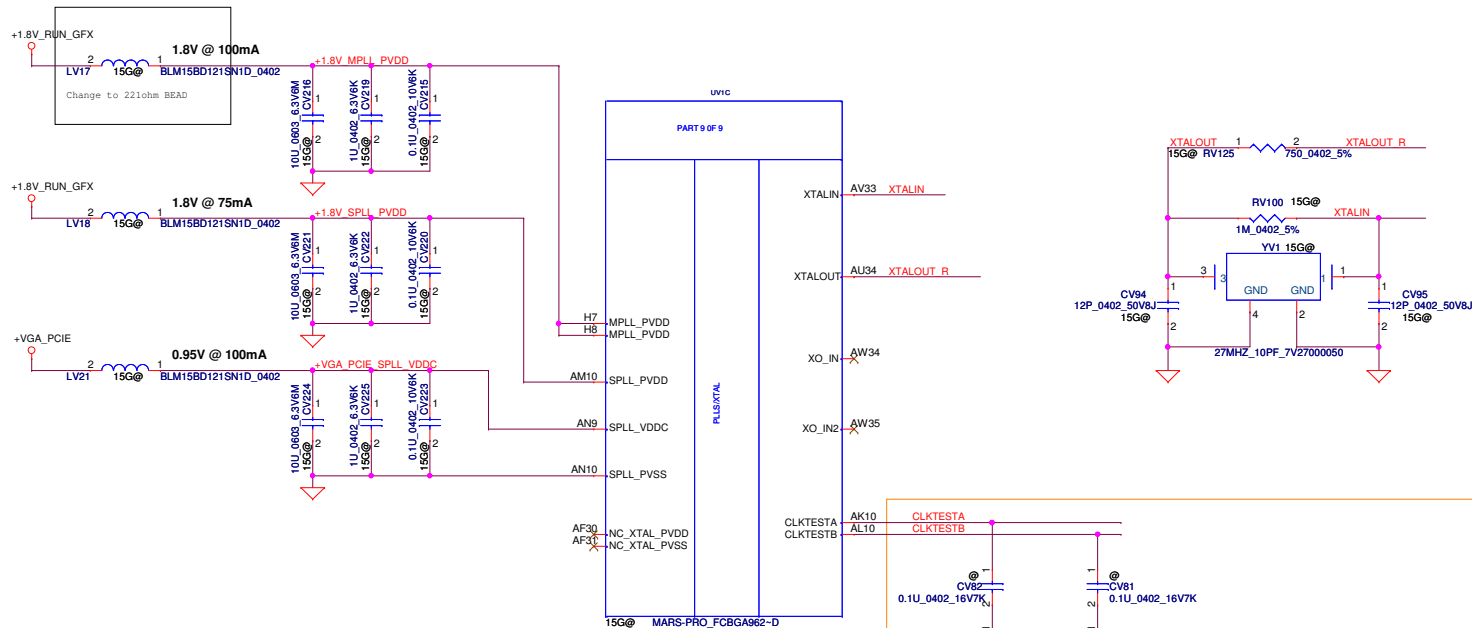




MLFS Bit	AMD recommended setting			
	strap	R_FU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

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MARX-PLL Power

Document Number

LA-9411P

Date: Wednesday, April 10, 2013

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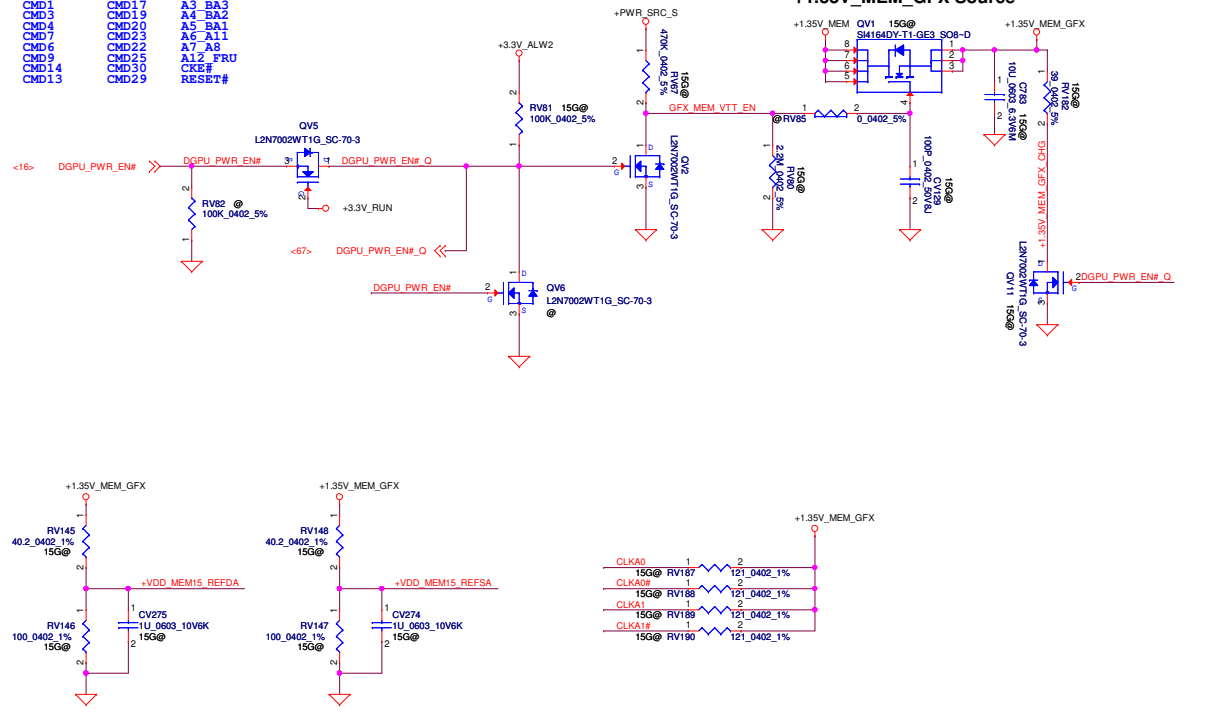
www.Vinafix.vn

GDDR5 CMD Mapping Table

LVNH			PART 3 OF 9		
GDDR5/DMA3			GDDR5/DMA3		
DOA0 [0..31]	<<>>	DOA0_0..31	<56>	DOA0_0	C37
DOA1 [0..31]	<<>>	DOA1_0..31	<57>	DOA0_1	C38
MAA0 [0..8]	<<>>	MAA0_0..8	<56>	DOA0_2	A38
MAA1 [0..8]	<<>>	MAA1_0..8	<57>	DOA0_3	E34
EDCA0 [0..3]	<<>>	EDCA0_0..3	<56>	DOA0_4	C39
EDCA1 [0..3]	<<>>	EDCA1_0..3	<57>	DOA0_5	D33
DOA0_0	<<>>	DOA0_0	<56>	DOA0_6	P32
DOA0_1	<<>>	DOA0_1	<57>	DOA0_7	E32
DOA0_2	<<>>	DOA0_2	<56>	DOA0_8	D31
DOA0_3	<<>>	DOA0_3	<57>	DOA0_9	F30
DOA0_4	<<>>	DOA0_4	<56>	DOA0_10	C30
DOA0_5	<<>>	DOA0_5	<57>	DOA0_11	A30
DOA0_6	<<>>	DOA0_6	<56>	DOA0_12	P28
DOA0_7	<<>>	DOA0_7	<57>	DOA0_13	C28
DOA0_8	<<>>	DOA0_8	<56>	DOA0_14	A28
DOA0_9	<<>>	DOA0_9	<57>	DOA0_15	E28
DOA0_10	<<>>	DOA0_10	<56>	DOA0_16	D27
DOA0_11	<<>>	DOA0_11	<57>	DOA0_17	P26
DOA0_12	<<>>	DOA0_12	<56>	DOA0_18	C26
DOA0_13	<<>>	DOA0_13	<57>	DOA0_19	A26
DOA0_14	<<>>	DOA0_14	<56>	DOA0_20	P24
DOA0_15	<<>>	DOA0_15	<57>	DOA0_21	C24
DOA0_16	<<>>	DOA0_16	<56>	DOA0_22	A24
DOA0_17	<<>>	DOA0_17	<57>	DOA0_23	E24
DOA0_18	<<>>	DOA0_18	<56>	DOA0_24	C22
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DOA0_24	<<>>	DOA0_24	<56>	DOA0_30	D19
DOA0_25	<<>>	DOA0_25	<57>	DOA0_31	E18
DOA0_26	<<>>	DOA0_26	<56>	DOA0_1	A18
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DOA0_30	<<>>	DOA0_30	<56>	DOA0_5	F15
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DOA0_16	<<>>	DOA0_16	<56>	DOA0_23	K10
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DOA0_18	<<>>	DOA0_18	<56>	DOA0_25	A8
DOA0_19	<<>>	DOA0_19	<57>	DOA0_26	C8
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DOA0_22	<<>>	DOA0_22	<56>	DOA0_29	C8
DOA0_23	<<>>	DOA0_23	<57>	DOA0_30	E8
DOA0_24	<<>>	DOA0_24	<56>	DOA0_31	A8
DOA0_25	<<>>	DOA0_25	<57>	DOA0_0	A8
DOA0_26	<<>>	DOA0_26	<56>	DOA0_1	A8
DOA0_27	<<>>	DOA0_27	<57>	DOA0_2	A8
DOA0_28	<<>>	DOA0_28	<56>	DOA0_3	A8
DOA0_29	<<>>	DOA0_29	<57>	DOA0_4	A8
DOA0_30	<<>>	DOA0_30	<56>	DOA0_5	A8
DOA0_31	<<>>	DOA0_31	<57>	DOA0_6	A8

<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD21	WE#
CMD0	CMD16	CS#
CMD8	CMD24	AB1#
CMD10	CMD26	A0 A10
CMD11	CMD27	A1 A9
CMD2	CMD18	A2 BA0
CMD4	CMD17	A3 BA3
CMD7	CMD23	A6 A11
CMD6	CMD22	A7 A8
CMD25	CMD25	A12 FRU
CMD30	CMD30	CKE#
CMD13	CMD29	RESET#

SI4164DY	RDS(on)	ID(A)
VDS	30 0.0032ohm at VGS=10V	30A
	30 0.0039ohm at VGS=4.5V	26.3A



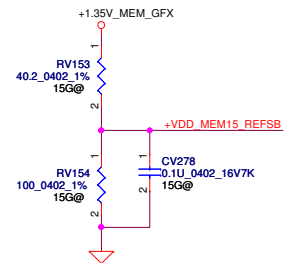
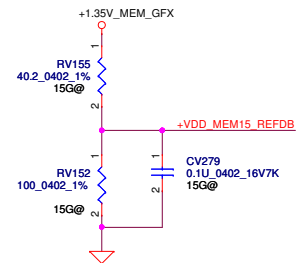
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Title	MARX-MEM Interface A
Size	Document Number
	LA-9411P
Date	Wednesday, April 10, 2013
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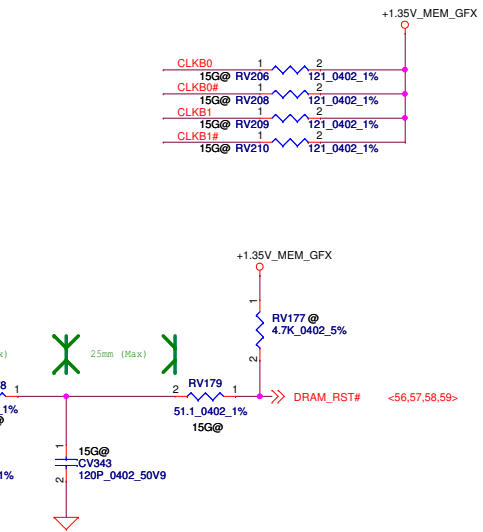
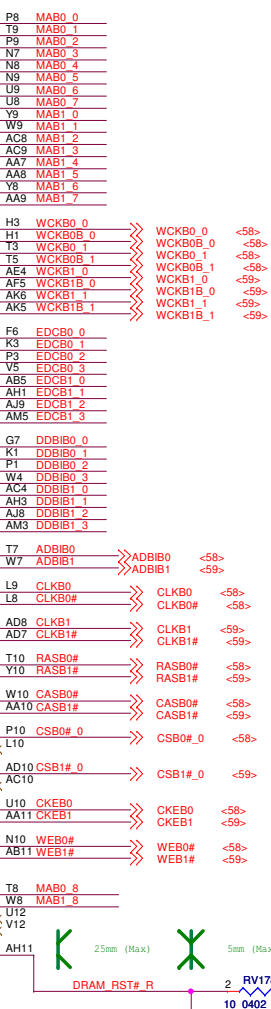
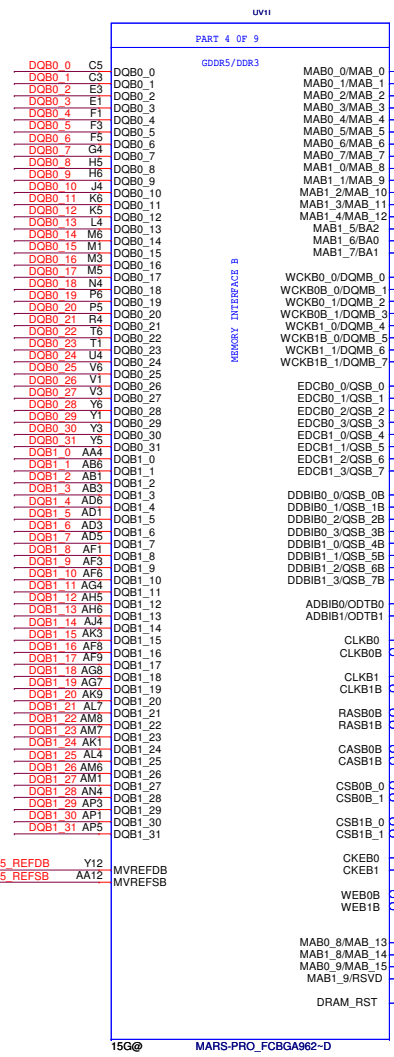
www.ViaChip.com

For Mars DNI RV28, RV31, RV32, RV34, RV35

DOB0 [0..31] <<>> DOB0 [0..31] <-58>
DOB1 [0..31] <<>> DOB1 [0..31] <-59>
MAB0 [0..8] <<>> MAB0 [0..8] <-58>
MAB1 [0..8] <<>> MAB1 [0..8] <-59>
EDCB0 [0..3] <<>> EDCB0 [0..3] <-58>
EDCB1 [0..3] <<>> EDCB1 [0..3] <-59>
DDBIB0 [0..3] <<>> DDBIB0 [0..3] <-58>
DDBIB1 [0..3] <<>> DDBIB1 [0..3] <-59>



+VDD MEM15 REFDB Y12
+VDD MEM15 REFSB AA12
MVRREFDB
MVRREFSB



This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | | Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

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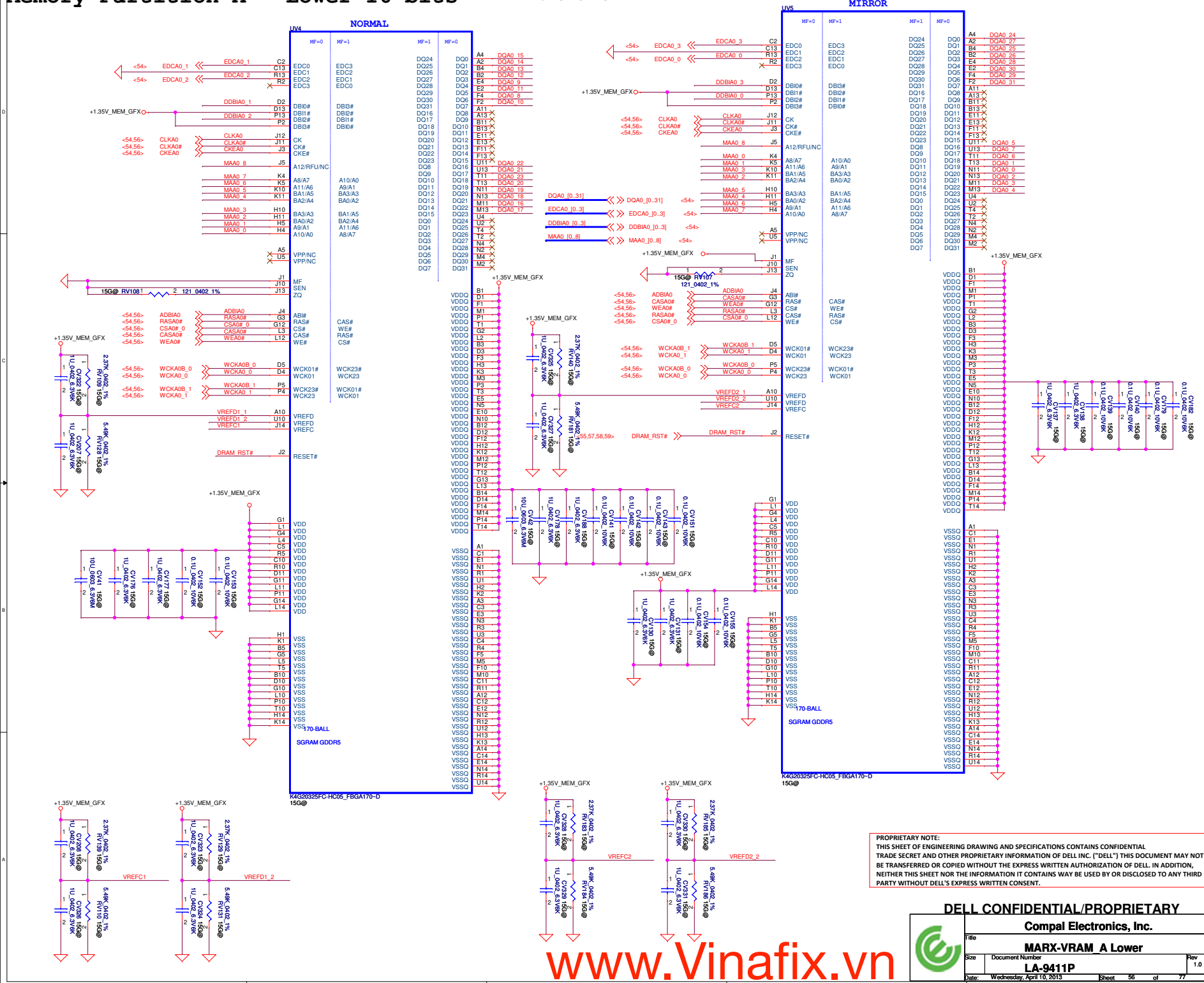
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Title		
MARX-MEM Interface B		
Size	Document Number	Rev
	LA-9411P	1.0
Date:	Wednesday, April 10, 2013	Sheet 55 of 77

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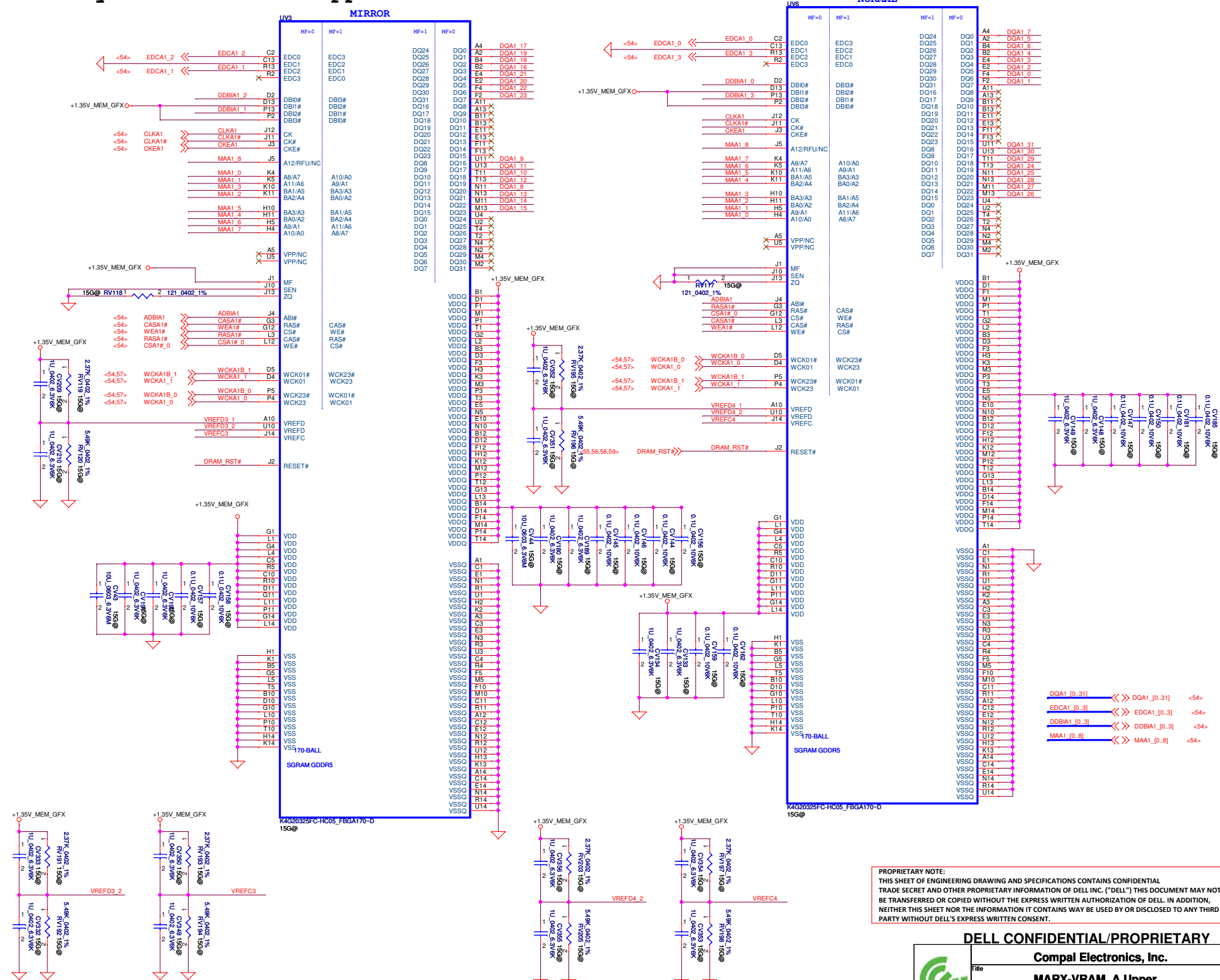
Memory Partition A - Lower 16 bits

64X32 GDDR5



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Memory Partition A - Upper 16 bits



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MARX-VRAM A Upper

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Rev
1.0

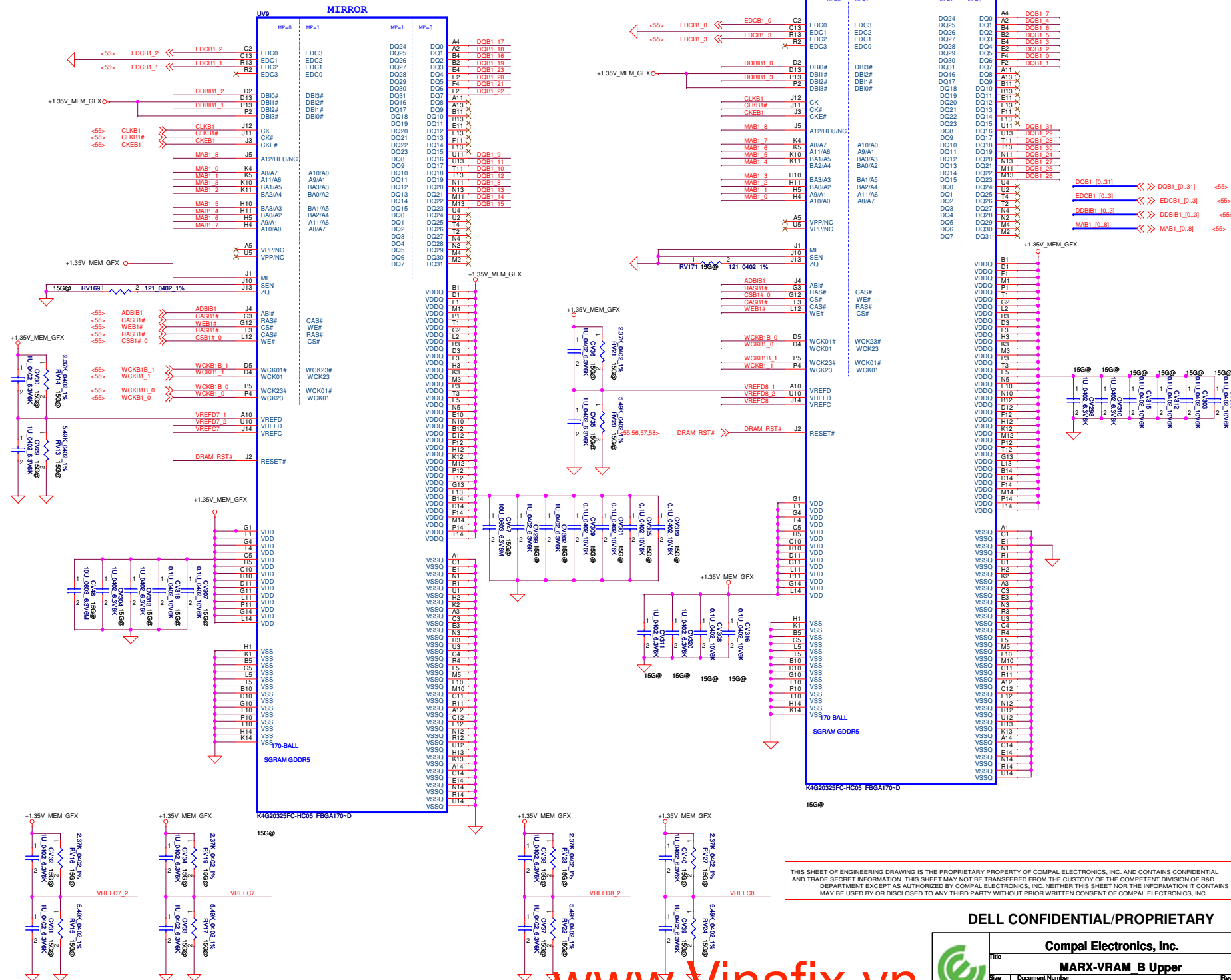
Date: Wednesday, April 10, 2013 Sheet 57 of 77

DOB0 [0..31]	<< >>	DOB0_0..31	<55>
EDCB0 [0..3]	<< >>	EDCB0_0..3	<55>
DDIB0 [0..3]	<< >>	DDIB0_0..3	<55>
MAB0 [0..8]	<< >>	MAB0_0..8	<55>



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Memory Partition B - Upper 16 bits



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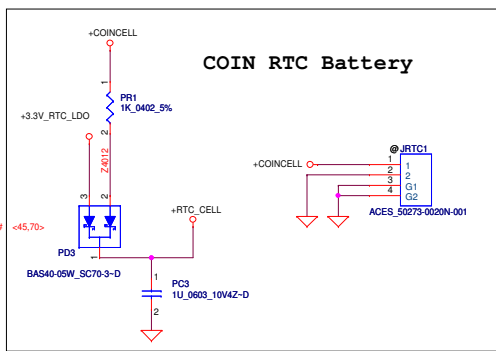
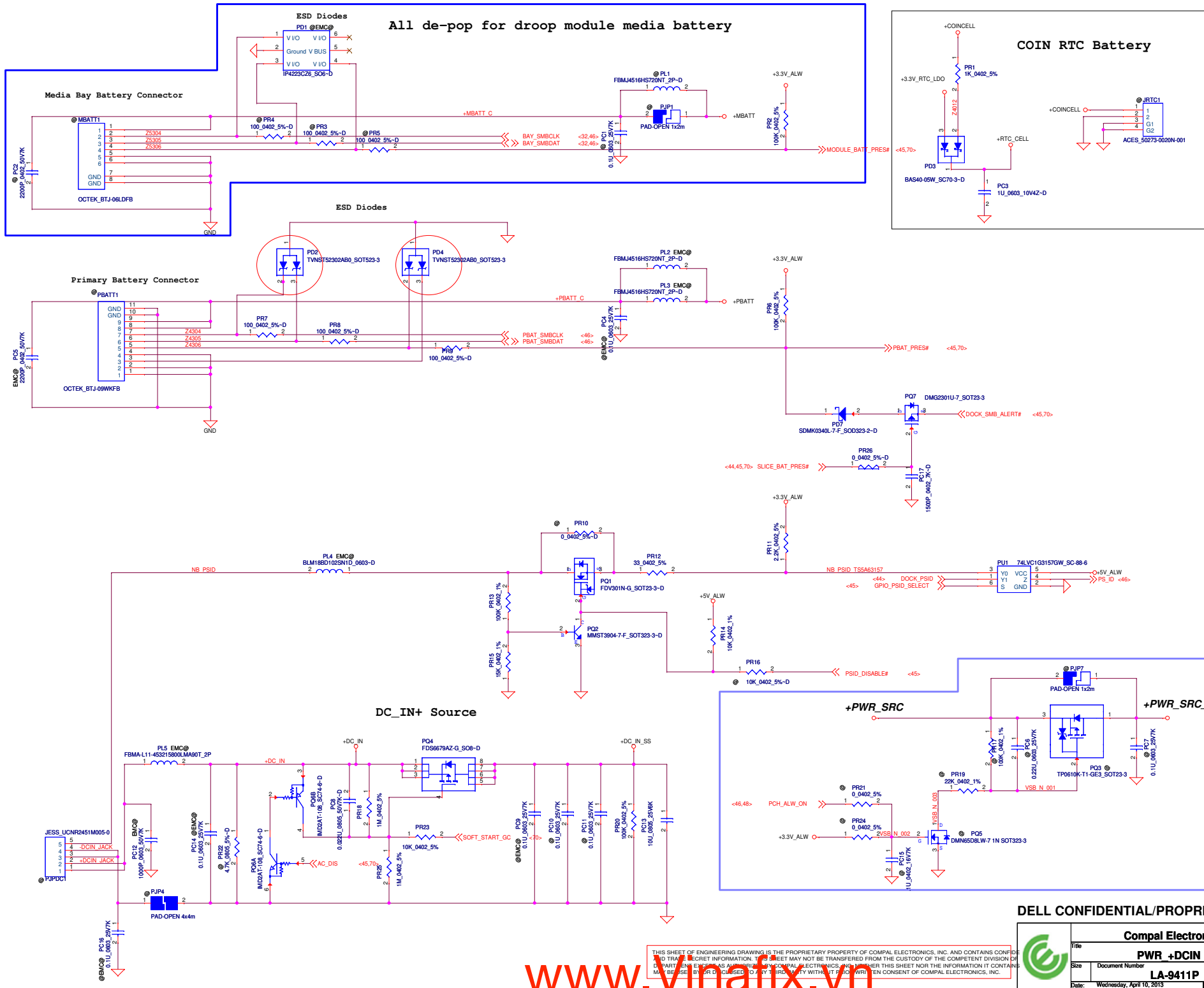
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MARX-VRAM B Upper

LA-9411P

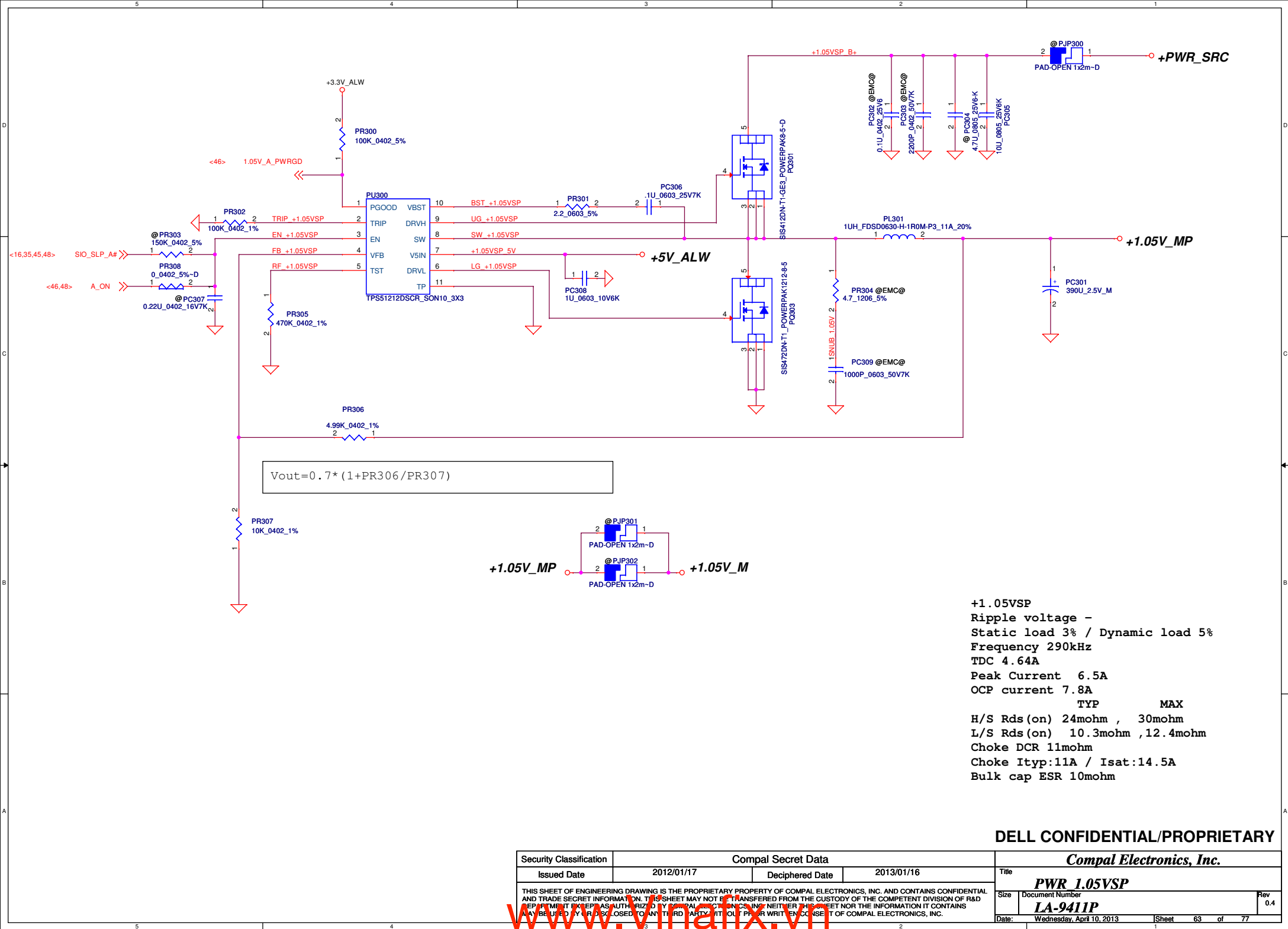
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Compal Electronics, Inc.			
PWR +DCIN			
Size	Document Number	LA-9411P	Rev 0.4
Date	Wednesday, April 10, 2013	Sheet 60	of 77

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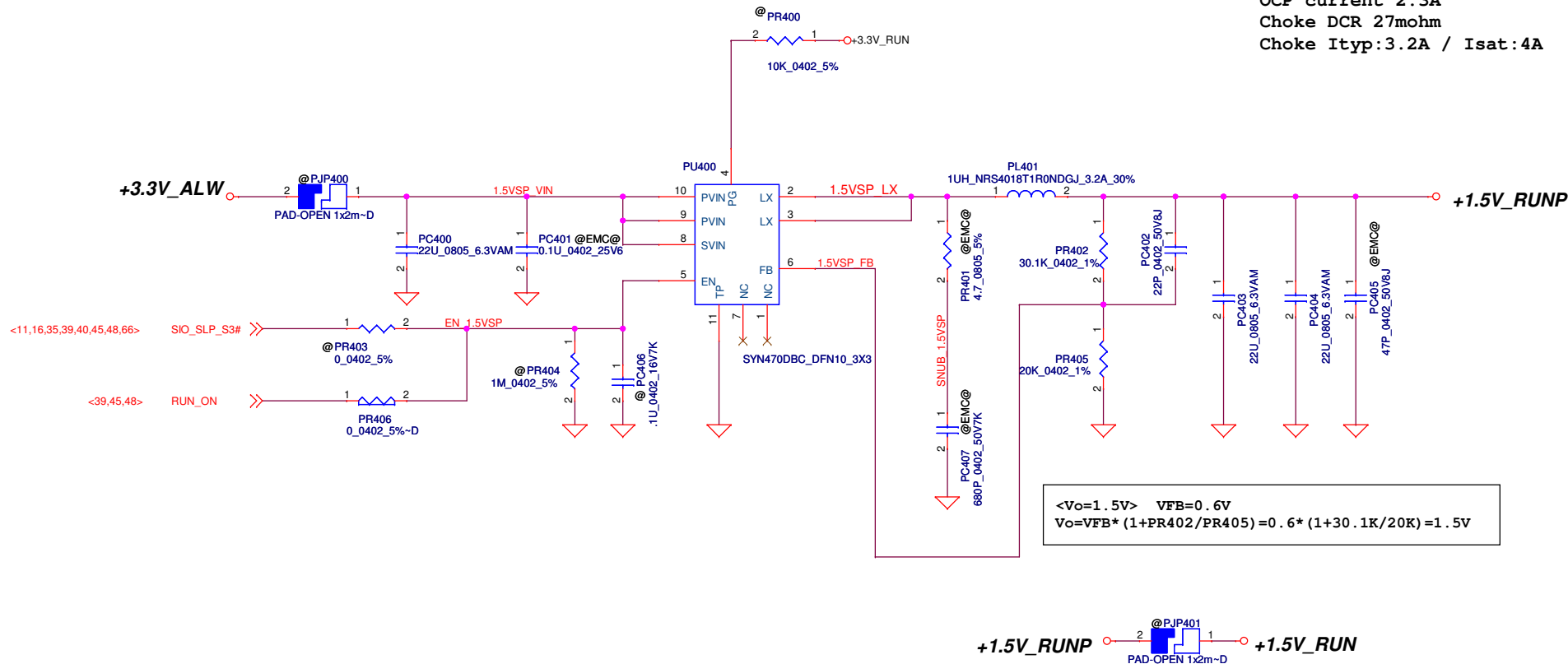
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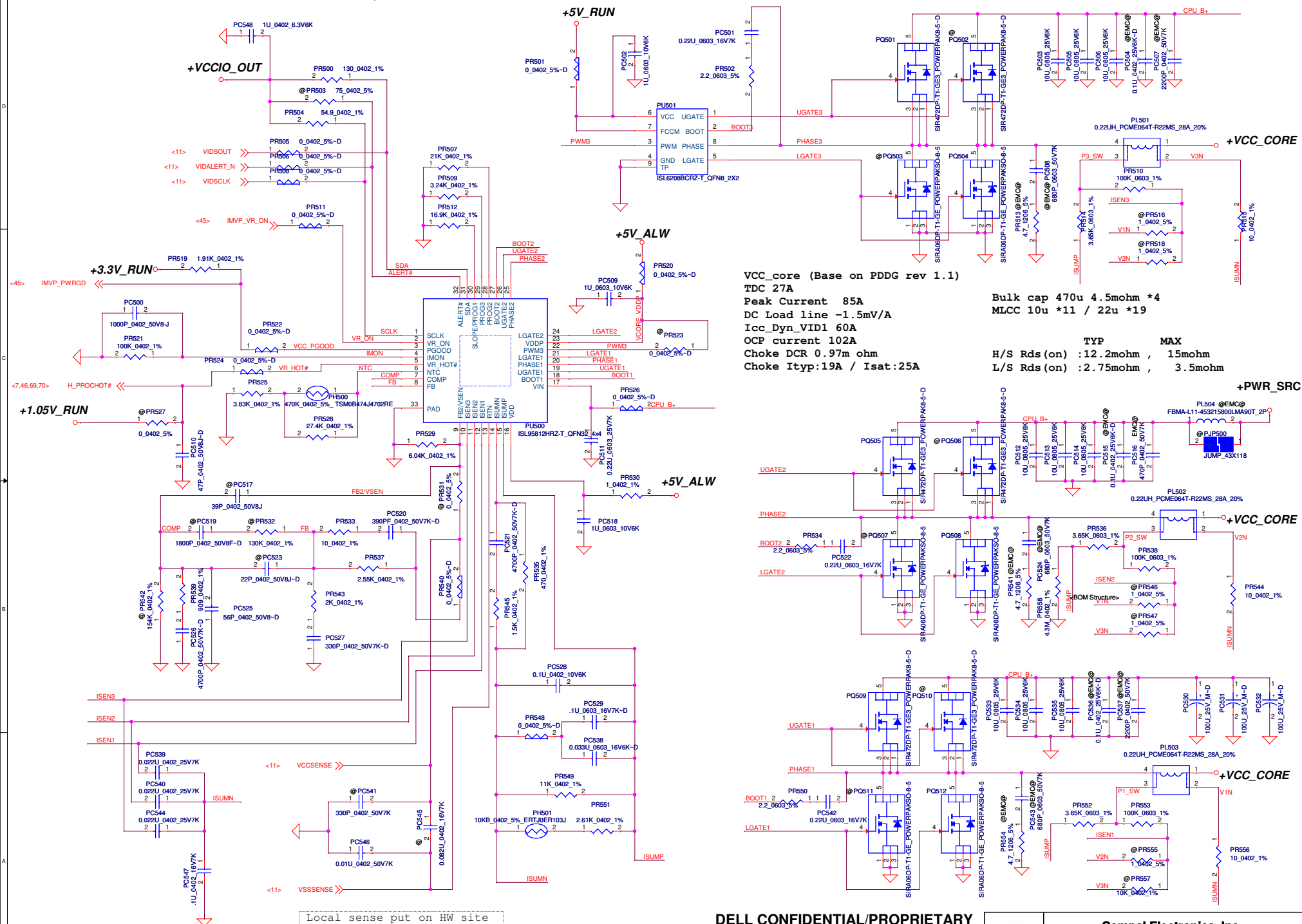
+1.5VSP
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 Frequency 1MHz
 TDC 1.329A
 Peak Current 1.9A
 OCP current 2.3A
 Choke DCR 27mohm
 Choke Ityp:3.2A / Isat:4A



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Title			
PWR_+1.5VSP			
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VCC_core (Base on PDDG rev 1.1)
TDC 27A
Peak Current 85A
DC Load line -1.5mV/A
Icc_Dyn_VID1 60A
OCP current 102A
Choke DCR 0.97m ohm
Choke Ityp:19A / Isat:25A

Bulk cap 470u 4.5mohm *4
MLCC 10u *11 / 22u *19

	TYP	MAX
H/S Rds(on)	:12.2mohm	15mohm
L/S Rds(on)	:2.75mohm	3.5mohm

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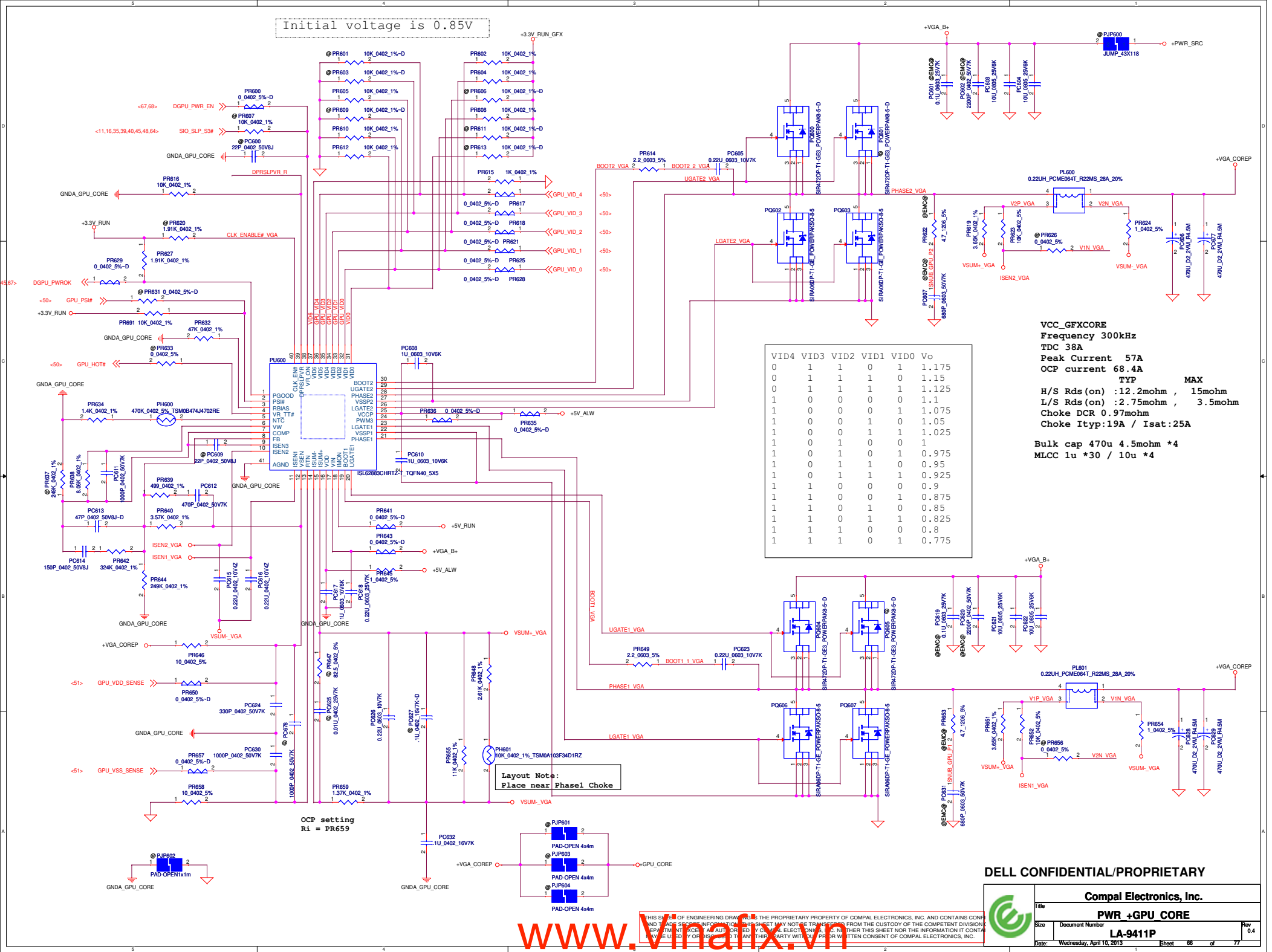
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PWR_VCORE_ISL95812 for QC

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Date	Sheet	of
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Initial voltage is 0.85V



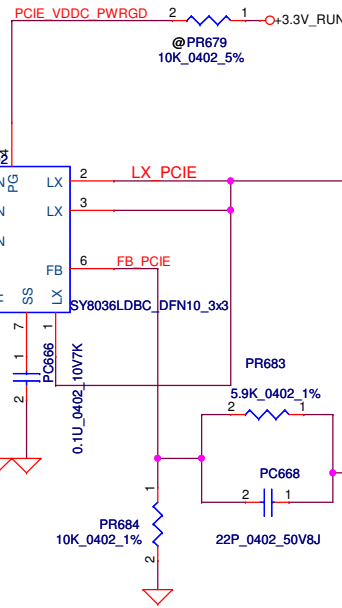
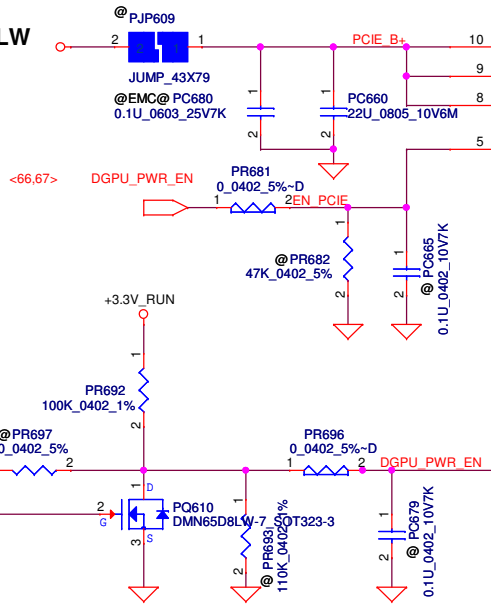
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PWR +GPU CORE	
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$$VFB=0.6V \quad V_O=VFB*(1+PR683/PR684)=0.6*(1+5.9K/10K)=0.95V$$

+5V_ALW



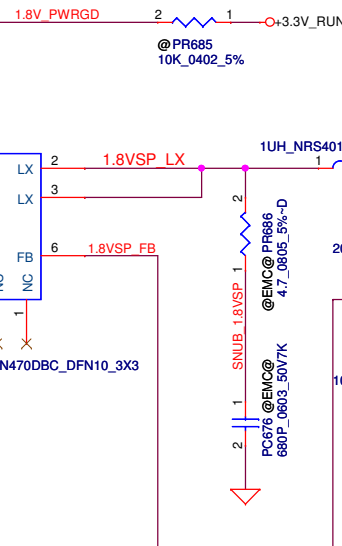
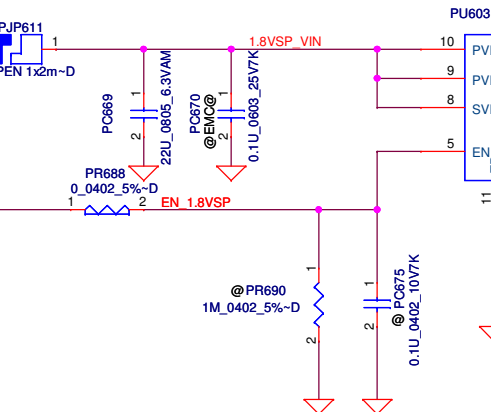
+VGA_PCIE

+VGA_PCIE (0.95V)
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 Frequency 1MHz
 TDC 3.2A
 Peak Current 4.56A
 OCP current 5.47A
 Choke DCR 29mohm
 Choke Ityp:4.9A / Isat:9A

+VGA_PCIE

1.8Volt
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 Frequency 1MHz
 TDC 1.43A
 Peak Current 2A
 OCP current 2.46A
 Choke DCR 27mohm
 Choke Ityp:3.2A / Isat:4A

+3.3V_ALW



+1.8V_RUN

+1.8V_RUN

+1.8V_RUN_GFX

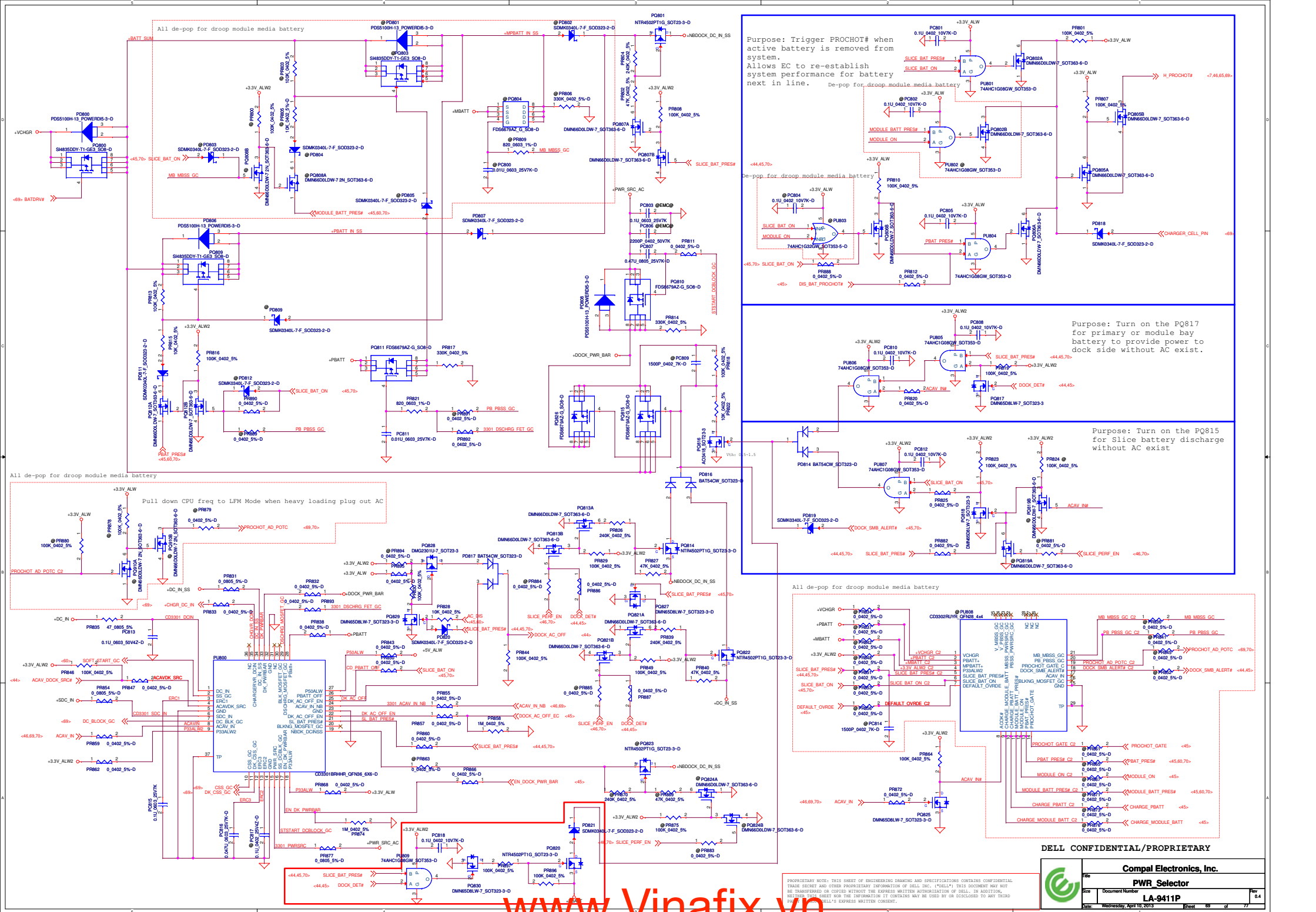
$$VFB=0.6V \quad V_O=VFB*(1+PR687/PR689)=0.6*(1+20K/10K)=1.8V$$

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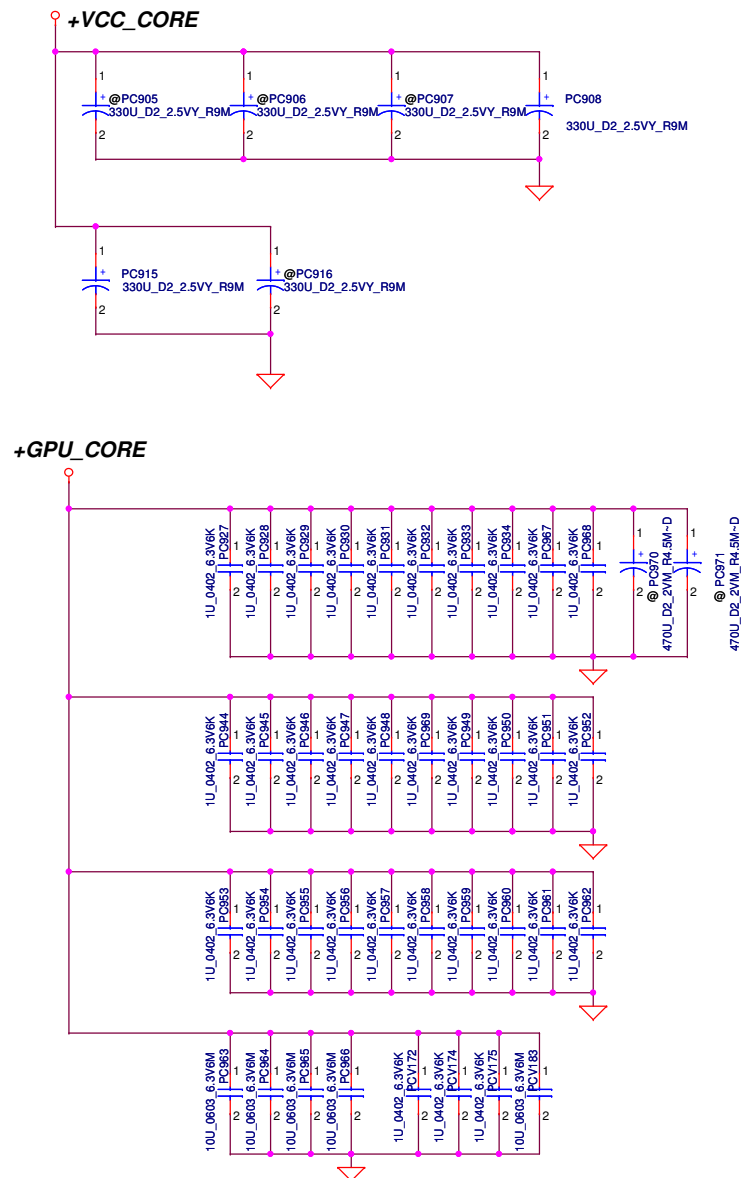
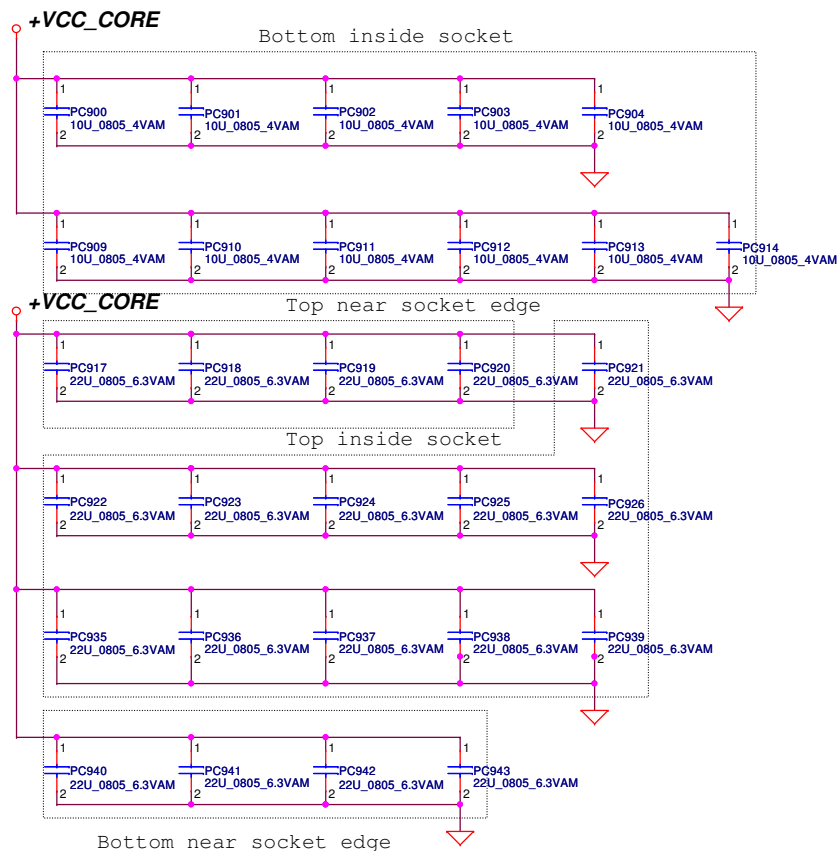
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Based on PDDG rev 1.1 Table 5-1.



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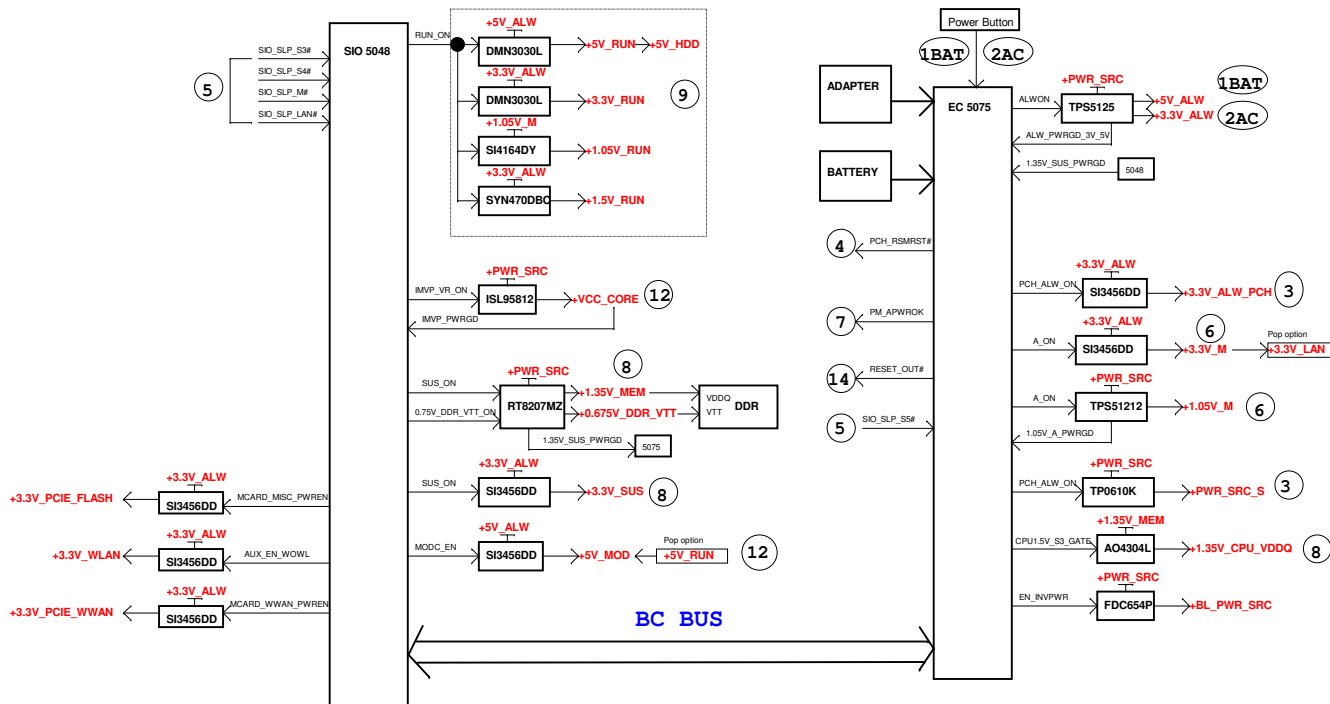
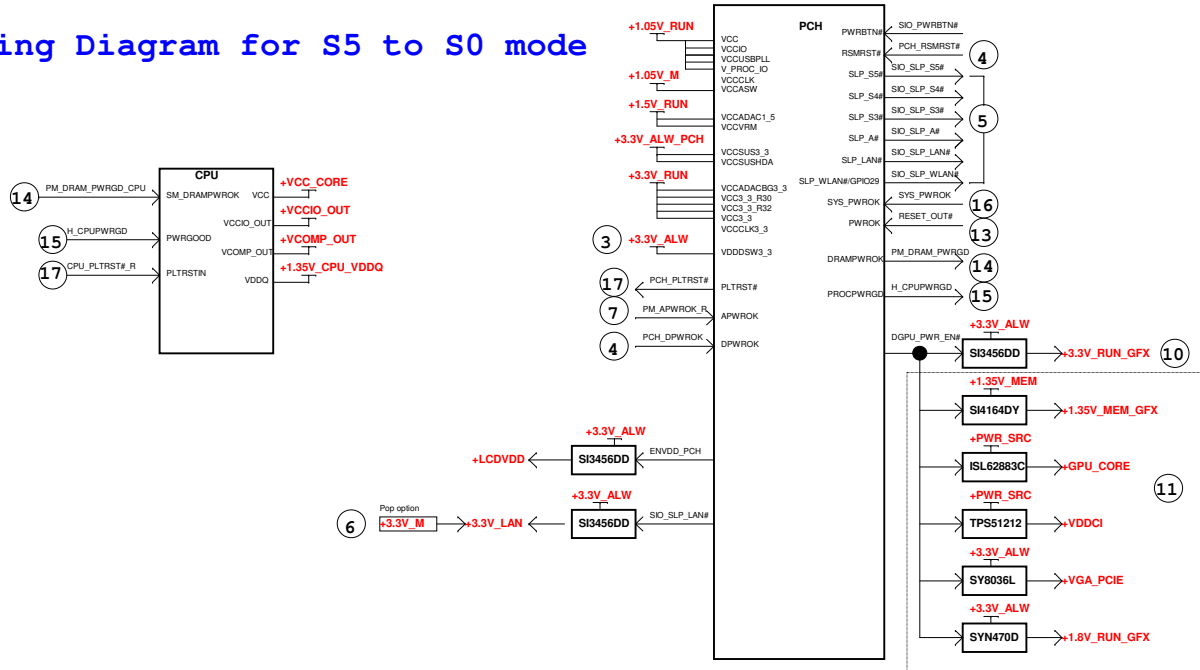
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Timing Diagram for S5 to S0 mode



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1	7	HW	8/24/2012	COMPAL	Change DRAMPWROK Pull up Power rail to Suspend	Base on EDS 1.0 (page124) . Change RC4 PM_DRAM_PWRGD pull up power rail to +3.3V_ALW_PCH.	X00(0.2)
2	16	HW	8/24/2012	COMPAL	Remove DGPU_HOLD_RST# double pull up.	Remove RH74 DGPU_HOLD_RST# pull up.	X00(0.2)
3	20	HW	8/24/2012	COMPAL	Remove mCARD_PCIE_SATA# double pull up.	Remove RH196 mCARD_PCIE_SATA# pull up.	X00(0.2)
4	48	HW	8/27/2012	COMPAL	Correct DC to DC interface Pull up power rail to +PWR_SRC_S	R905.1, R911.1, R917.1, R930.1, R906.1 and R912.1 change to +PWR_SRC_S	X00(0.2)
5	13,14	HW	8/27/2012	COMPAL	Follow DG DDR3L VREF_DQ Control as page120. it pull up power rail should be +1.35V_MEM	Modify RD19.1, RD22.1, RD15.1 net name to +1.35V_MEM.	X00(0.2)
6	46,16	HW	8/30/2012	COMPAL	Follow EDS page 131 as DSW rail	Modify AC_PRESENT R835.1 to +PCH_VCCDSW3_3 Add PCH_PCIE_WAKE# RH92.1 to +PCH_VCCDSW3_3 De-populate RH78 with +3.3V_ALW_PCH power rail	X00(0.2)
7	46	HW	8/27/2012	COMPAL	Correct GPU_SMBDAT,GPU_SMBCLK Pull up power rail to +3.3V_RUN	Modify GPU_SMBDAT R829,1,GPU_SMBCLK R822.1 to +3.3V_RUN	X00(0.2)
8	33	HW	8/27/2012	COMPAL	Change LANWAKE#_R Pull up power rail to +3.3V_LAN	Modify R558.1 power rail to +3.3V_LAN	X00(0.2)
9	46	HW	8/29/2012	COMPAL	Modify THERMATRIP2# control by +VCCIO_OUT	Modify Q4.2 to +VCCIO_OUT.	X00(0.2)
10	47	HW	8/27/2012	COMPAL	Back E4 RSMRST RESET IC solution and add pull up at PCH_RSMRST#_Q	Modify U8 to RT9818A-44GU3 Add Pull up 8.2Kohm to +3.3V_ALW_PCH on PCH_RSMRST#_Q	X00(0.2)
11	35	HW	8/27/2012	COMPAL	Back E4 JUSH pin out	JUSH1 back to 20pins.	X00(0.2)
12	51	HW	8/27/2012	AMD	Modify GPU power net	+VDDCI change to +GPU_CORE power net	X00(0.2)
13	48	HW	8/27/2012	COMPAL	Correct +1.35V_CPU_VDDQ Discharge net name	Modify R926.2 Net name to +1.35V_CPU_VDDQ	X00(0.2)
14	36	HW	8/27/2012	COMPAL	Update OZ777 ES2 symbol	U38 OZ777FJ2LN_QFN48P_6X6 symbol updated	X00(0.2)
15	38	HW	8/27/2012	COMPAL	Replace U7 SATA Repeater and U95 SATA/PCIE SW by U7 ASM1467 SATA/PCIE Repeater.	Modify U7 circuit	X00(0.2)
16	33,34	HW	9/4/2012	COMPAL	LAN LED support unobtrusive mode on System board	Modify Q325,Q326 LAN LED control circuit between LAN SW MB and MB CONN.	X00(0.2)
17	16	HW	8/27/2012	COMPAL	Base on EDS 1.0 Page 124 Modify SIO_SLP_LAN# to DSW Power rail	Modify SIO_SLP_LAN# RH80.1 to +PCH_VCCDSW3_3	X00(0.2)
18	37	HW	8/27/2012	COMPAL	Modify CPPE#, USB_MCARD1_DET# Pull up power rail to +3.3V_RUN	Modify CPPE# R737.2, USB_MCARD1_DET# R739.2 net name to +3.3V_RUN	X00(0.2)
19	29	HW	8/28/2012	DELL	Cost Down Concept	Replace(U21,U24)NOT Gate by(Q5, Q6)N-Channel MOSFET with Pull high resistor on CA_DET#	X00(0.2)
20	30	HW	8/28/2012	REALTEK	Codec AGND to DGND modify	Replace C981, C982, C983 0.1uf by R5,R6,R15 0ohm	X00(0.2)
21	50	ESD	8/29/2012	COMPAL	Reserve GPU_HOT# control by H_PROCHOT#	Reserve H_PROCHOT# with level shift circuit to control GPU_HOT#	X00(0.2)

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22	24	ME	8/30/2012	COMPAL	ME request	Change SW1 power switch to SN11100580L SKRBAAE010_4P~D	X00 (0.2)
23	45	HW	9/3/2012	DELL	GPIO MAP2.4	1.Assign ECE5048_TX at 5048 GPIOE1/TXD 2.Remove 1.8V_RUN_PWRGD across X5 at 5048 GPIOK2 pin B10. 3.Move USB_PWR_SHR_EN# to GPIOK2 pin B10 4.Free up 5048 GPIOG3 (DYN_TURB_PWR_ALRT#),de-populate R796	X00 (0.2)
24	35	HW	9/4/2012	COMPAL	Follow INTEL Check list 1.0 reserve JAPS1 pin4, 7 connection	1.Reserve JAPS1 PIN4 of R23 SIO_SLP_S5# and R17 +3.3V_ALW_PCH 2.Reserve JAPS1 PIN7 of R24 +3.3V_ALW	X00 (0.2)
25	46	HW	9/18/2012	COMPAL	Added a 0ohm at U51 VTR_ADC pin.	Added R839 0ohm between +3.3V_ALW and U51.A58 pin.	X01 (0.3)
26	47	HW	9/19/2012	INTEL	Stuff RTC cell can't power on issue	Reserve R1636 pull down resistor on PCH_RSMRST#_Q.	X01 (0.3)
27	20,46	HW	9/24/2012	COMPAL	GPIO MAP2.5	1.Remove POA_WAKE# at 5075 VCI_INT3# pin B68 2.Remove FP_POA_EN at 5048 GPIOI7/PWM5 pin A44. 3.Rename LANWAKE# to EC_WAKE# at 5048 GPIOI5/PWM2 pin B1. 4.Add LANWAKE# connect to 5075 pin B27 5.Reserve 0ohm between LANWAKE# and EC_WAKE#	X01 (0.3)
28	11	HW	9/24/2012	COMPAL	HSW will internally power gate the VDDQ rail (+1.35V_CPU_VDDQ)	1.De-populated the +1.35V_CPU_VDDQ DC to DC circuit 2.add these two PJP5, PJP6 4x4mm Jumper between +1.35V_CPU_VDDQ and +1.35V_MEM power net.	X01 (0.3)
29	46	HW	9/24/2012	COMPAL	Follow CRB1.2 Peci circuit	De-populate Peci_EC_R C290 CAP.	X01 (0.3)
30	36	HW	9/24/2012	COMPAL	O2 Request	Add C802 0.1uF cap on SD_CD#.	X01 (0.3)
31	30	HW	10/03/2012	COMPAL	When no external power, it Sleeve will be floating mode and no reference GND.	Add AUD_NB_MUTE# to control Sleeve pin.	X01 (0.3)
32	16	HW	9/26/2012	COMPAL	Follow CRB, PCH_DPWROK circuit	Add RH120 100Kohm PD and close to PCH site.	X01 (0.3)
33	32	HW	9/26/2012	COMPAL	Follow EDS, Change USB30_SMI# (GPIO13) pull up power rail to +3.3V_ALW_PCH.	Change R514.1 to +3.3V_ALW_PCH	X01 (0.3)
34	38	HW	10/02/2012	Asmedia	Asmedia ASM1467 spec modify	1.Pin7 GND chage DE_A 2.Pin6 Reserved change to GND 3.Pin16 MOSEL change to Reserved 4.Pin17 DE_A change to MOSEL	X01 (0.3)
35	27	HW	9/26/2012	COMPAL	Change EDP to LVDS converter solution to RTD2136R	1.Change U27 P/N:SA000067100(S IC RTD2136R-CG QFN 48P DP/LVDS CTRL) 2.Remove R102,R103 0ohms 3.Remove R107 4.7Kohm 4.Add R108 4.7Kohm 5.Remove U26 CAT24C64WI-GT3_S08_EEROM	X01 (0.3)
36	28	HW	10/02/2012	COMPAL	Fix LCD T3 timing issue	Add R115 0ohm between LCD_ENVDD_CVT and U55.4 net to control +LCD_VDD power net.	X01 (0.3)
37	30	HW	10/04/2012	COMPAL	Reserve Support universal jack	1.C195,C196 4.7U_0603_6.3V6K~D 2.R198,R199 1K_0402_5% 3.R209,R210 4.7K_0402_5%~D 4.D11,D12 RB751VM-40TE-17_SOD323-2~D	X01 (0.3)
38	20,35	HW	10/05/2012	COMPAL	GPIO MAP2.6	1.Add SMART_DET# on PCH GPIOI5 and JUSH1 pin11. 2.Move EC_WAKE# from ECE5048[L]5 to MEC5075 GPIOI52. 3.Add ECE5048_PWRGD to MEC5075 GPIOI02 4.Add AND Gate of ECE5048_PWRGD, RUNPWROK to AND_PWRGD on ECE5048 A4 pin 5.Remove R842 pull up resistor	X01 (0.3)

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39	30	HW	10/08/2012	COMPAL	Remove IDT& TI Audio codec co-lay circuit	Remove IDT& TI Audio codec co-lay circuit	X01 (0.3)
40	37	HW	10/08/2012	COMPAL	Remove +1.5V_RUN power rail on JMINI3 card	1.Remove +1.5V_RUN power rail on JMINI3 card of pin6, 28 and 48 2.Remove C619, C620 cap	X01 (0.3)
41	54	HW	10/11/2012	COMPAL	Correct DGPU_PWR_EN# behavior	Add QV5	X01 (0.3)
42	30	HW	10/11/2012	REALTEK	Follow Realtek recommend circuit	1.Change L91,92,93,94 to R41,42,43,44 0_0603_5%~D 2.Change C973,974,975,76 1000P_0402_50V8-J 3.Change R1680,1681,1682,1683 0_0402_5%~D	X01 (0.3)
43	11	HW	10/25/2012	COMPAL	Follow CRB1.5 design	1. De-populate 10UF CC26,CC27,CC28,CC29,CC30,CC31,CC32,CC33 2. De-populate 22UF CC41,CC37,CC42,CC43,CC38,CC44,CC39,CC45.CC46 3. De-populate 330UF CC34	X01 (0.3)
44	11	HW	10/25/2012	COMPAL	Support Deep SX mode	1. De-populate RH79 0_0402 2. Populate R802 0_0402	X01 (0.3)
45	30	HW	12/25/2012	COMPAL	Follow Realtek recommend circuit	1.Change R1658,R1095 to jump 2.Change R1119 ,R1120 to 100K 3.Change R1677 R1679 to 9.1 ohm 4.Remove R25	X02 (0.4)
46	50	HW	12/25/2012	COMPAL	Follow AMD recommend	Change GPU_HOT# pull high fomr 100K to 4.7K	X02 (0.4)
47	28	HW	12/25/2012	COMPAL	Samsnug PANEL issue	Add pull down R1139 100K	X02 (0.4)
48	20	HW	12/25/2012	COMPAL	TLS issue	Change RH229 fomr 200K to 1K	X02 (0.4)
49	46	HW	12/25/2012	COMPAL	Follow DELL recommend	add 0ohm to short RUNPWROK and AND_PWRGD	X02 (0.4)
50	36	HW	12/25/2012	COMPAL	Follow GPIO map rev 3.0C	SP_TPM_LPC_EN reserve PCH GPIO22 to control	X02 (0.4)
51	13,14	HW	12/25/2012	COMPAL	Follow CRB1.5 DDR RAM M1&M3 circuit	Reserve circuit to control 1.+SA_DIMM1_VREFDQ ,+SA_DIMM2_VREFDQ 2.+SM_VREF_DIMM 3.DDR3_DRAMRST#_R	X02 (0.4)
52	30	HW	12/25/2012	COMPAL	Follow ESD	Remove D83,D23,D8,D37,DE1&DE2	X02 (0.4)
53	36	HW	03/28/2013	COMPAL	Follow O2 recommend	add R493 on SD_CD#	A00 (1.0)

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1	66	+GPU_CORE	8/29	AMD	GPU_CORE merged with one of AMD Chip power rail - VDDCI	Delete VDDCI Power rail page	X00 (0.2)
2	60	+DC_IN	8/29	Compal	ESD Team change solution	Change PD1 PD2 Solution	X00 (0.2)
3	68	Charger for DSC	8/29	Compal	SMBus connection is wrong	Swap net CHARGER_SMBDAT and CHARGER_SMBCLK	X00 (0.2)
4	67	+VGA_PCIE/ +1.8V_RUN_GFX	8/29	Compal	DGPU_PWR_EN signal pull high voltage net is wrong	Change PR692 Pin1 net from +3.3V_ALW to +3.3V_RUN	X00 (0.2)
5	61	3VALWP/5VALWP	8/29	Compal	Find tune 3V/5V OCP setting	Change PR105 from 110k to 115k for 3.3V Change PR106 from 82.5k to 86.6k for 5V	X00 (0.2)
6	62	1.35V/0.675VSP	8/29	Compal	Change Enable signal from SIO_SLP_S4# to SUS_ON by HW request	Pop PR210 and depop PR206	X00 (0.2)
7	63	1.05VSP	8/29	Compal	Fint tune 1.05VSP OCP setting	Change PR302 from 64.9k to 68.1k	X00 (0.2)
8	65	VCORE_ISL95812 for QC	8/29	Compal	Fint tune DC loadline	Change PR537 from 2.55k to 2.37k	X00 (0.2)
9	66	+GPU_CORE	8/29	AMD	Adjust OCP setting for +GPU_CORE merge with VDDCI	Change PR659 from 787 to 1.37k	X00 (0.2)
10	66	+GPU_CORE	8/29	AMD	Adjust initial voltage from 1.125V to 0.85V	Pop PR602 PR604 PR608 PR605 PR610 PR612 Depop PR606 PR611 PR613 PR601 PR603 PR609	X00 (0.2)
11	65	VCORE_ISL95812 for QC	9/25	Compal	Fint tune DC loadline	Change PR535 from 475ohm to 511ohm Change PR537 from 2.37k to 2.55k	X01 (0.3)
12	65	VCORE_ISL95812 for QC	9/25	INTERSIL	Change schematic setting for new version IC (Rev3p0)	Change PR529 from 0 to 6.04k Change PR512 from 21k to 16.9k Change PR507 from 49.9k to 21k Change PR509 from 34k to 3.24k	X01 (0.3)
13	65	VCORE_ISL95812 for QC	9/25	Compal	Fint tune IMON	Change PR521 from 90.9k to 100k	X01 (0.3)
14	68	Charger for DSC	9/28	TI	Schematic setting for charger IC	Change PR722 from 0 to 4.02k	X01 (0.3)
15	69	Selector	9/28	Compal	Can not power on with only slice battery	Add PD819 and DOCK_SMB_ALERT# control signal	X01 (0.3)
16	69	Selector	9/28	Compal	Turn on DOCK_PWR_BAR NVDC blocking MOSFET(PQ815) to charge and discharge slice battery	Add PR882 and SLICE_BAT_PRES# control signal to replace SLICE_PREF_EN EC signal	X01 (0.3)
17	69	Selector	9/28	Compal	Turn off DOCK_PWR_BAR NVDC blocking MOSFET(PQ815) when AC connect to other NB or DOCK	Add PR886 PR887 and DOCK_DET# control signal to replace SLICE_PREF_EN EC signal	X01 (0.3)
18	60	+DC_IN	10/8	Compal	Reserve circuit for droop module battery function	Reserve PQ7 PD7 PR26 PC17 location	X01 (0.3)
19	69	Selector	10/8	Compal	Reserve circuit for droop module battery function	Reserve PR888 PR890 PR892 location	X01 (0.3)

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20	69	Selector	10/8	Compal	Abnormal waveform in PBAT_PRES# when remove battery	Change PD811 and PD804 location	X01 (0.3)
21	69	Selector	10/8	Compal	Avoid voltage appearing at the docking connector when either slice battery or E-Dock is not connected to notebook	Add PQ826	X01 (0.3)
22	65	VCORE_ISL95812 for QC	10/8	Compal	Remove the 1.05V_0.8V_PWROK connection by HW request	Delete PR517	X01 (0.3)
23	63	1.05VSP	10/8	Compal	Remove the 1.5V_RUN_PWRGD connection by HW request	Delete net 1.5V_RUN_PWRGD	X01 (0.3)
24	68	Charger for DSC	10/11	Compal	Reserve circuit for system throttling switching from AC to DC if droop module battery function	Reserve PU704 PC733 PR748 PQ710 PQ708 location	X01 (0.3)
25	60	+DC_IN	11/20	Dell	Reserve module battery connector circuit for droop module battery function	De-pop MBATT1 PC2 PR4 PR3 PR5 PL1 PR2 PD1 PC1 PJP1	X02 (0.4)
26	60	+DC_IN	11/20	Dell	Add Main battery control signal circuit for droop module battery function	Pop PQ7 (DMG2301U-7) PD7 (SDMK0340L-7-F) PC17 (1500pF) PR26 (0 ohm)	X02 (0.4)
27	60	+DC_IN	11/20	Compal	Reserve +PWR_SRC to +PWR_SRC_S Circuit by HW request	De-pop PQ3 PQ5 PR21 PC15 PR24 PR19 PR17 PC6 PC7	X02 (0.4)
28	60	+DC_IN	11/20	Compal	Change EMI solution by EMI request	Delete PL6 PD6 and add PJP4	X02 (0.4)
29	68	Charger for DSC	11/20	Dell	Add circuit for CPU freq to LFM mode when heavy loading plug out AC, because this function is built in module battery function controller IC - CD3302, droop module battery will not use CD3302 controller.	Pop PU704 (74AHC1G08GW) PC733 (0.1uF) PQ710 (DMN65D8LW-7) PR748 (100K)	X02 (0.4)
30	68	Charger for DSC	11/20	Compal	Use one dual N package part to replace two NPN Mosfet	Change PQ707 PQ708 from DMN65D8LW-7 to DMN66D0LDW-7 (PQ707A PQ707B)	X02 (0.4)
31	69	Selector	11/20	Dell	Reserve module battery circuit about trigger PROCHOT# when active battery is removed from system.	De-pop PU802 PC802 PU803 PC804 Pop PR888 (0 ohm)	X02 (0.4)
32	69	Selector	11/20	Dell	Reserve controller - CD3302 solution for droop module battery circuit	De-pop PU808 PR834 PR837 PR842 PR848 PR851 PR853 PR856 PC814 PR861 PR865 PR867 PR871 PR873 PR876 PR836 PR841 PR845 PR852 PQ910 PR880 PR878 PR879	X02 (0.4)
33	69	Selector	11/20	Dell	Reserve module battery charging and discharging path circuit	De-pop PQ808 PD803 PR800 PR803 PR805 PD804 PD805 PQ803 PD801 PQ804 PR809 PC800 PR806 PD802 PD809	X02 (0.4)
34	69	Selector	11/20	Dell	Change battery control signal for droop module battery function	De-pop PD812 PR889 PR891 Pop PR890 (0 ohm) PR892 (0 ohm)	X02 (0.4)
35	69	Selector	11/20	Compal	Change Main source for EOL issue.	Change PQ801 PQ814 PQ822 PQ823 from FDN338P_G to NTR4502PT1G	X02 (0.4)

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36	69	Selector	11/20	Compal	Use one dual diode package part to replace two discrete diode part	Change PD810 PD814 PD813 PD816 PD815 PD817 from SDMK0340L-7-F to BAT54CW (PD814 PD816 PD817)	X02 (0.4)
37	70	PROCESSOR DECOUPLING	11/20	Compal	Move GPU Core output MLCC cap to power side by HW request	Change CV172 CV174 CV175 CV183 location to PCV172 PCV174 PCV175 PCV183	X02 (0.4)
38	68	Charger for DSC	11/20	Compal	Change bootstrap resistor size	Change PR715 size from 0402 to 0603	X02 (0.4)
39	69	Selector	11/20	Compal	Use one package part to replace dual n package part	Change PQ802 from DMN66D0LDW-7 to DMN65D8LW-7	X02 (0.4)
40	65	VCORE_ISL95812 for QC	12/25	Compal	VCCIO_OUT 6KHz noise issue. Request by H.W.	Add PC548 (1uF)	X02 (0.4)
41	65	VCORE_ISL95812 for QC	12/25	INTERSIL	Fine tune Iout accuracy	Change PR535 from 511 Ohm to 470 Ohm. Change PR521 from 100kOhm to 100kOhm. Change PC500 from 0.01uF to 1000pF. Change PC539,PC540,PC544 from 0.22uF to 0.022uF. Change PR510,PR538,PR553 from 10kOhm to 100kOhm. Add PR558 (4.3M Ohm)	X02 (0.4)
42	68	Charger for DSC	12/25	TI	For Input current sense stabilize	Change PC703 from 0.1uF to 1uF	X02 (0.4)
43	68	Charger for DSC	12/25	TI	Change cell pin pull high reference voltage from +3.3V_ALW to BQ24715_REGN	Depop PR720 and pop PR746	X02 (0.4)
44	60	+DC_IN	12/25	Compal	GPIO net - AC_DIS# is high active. Corrent net name.	Change PQ6A pin.5 net name from AC_DIS# to AC_DIS.	X02 (0.4)
45	69	Selector	12/25	Compal	GPIO net - AC_DIS# is high active. Corrent net name.	Change PR828 pin1 net name from AC_DIS# to AC_DIS.	X02 (0.4)
46	68	Charger for DSC	1/7	Compal	Reserve input cap location for input voltage overshoot issue. This issue fix in PGI.3	Reserve PC734 PC735	X02 (0.4)
47	68	Charger for DSC	1/7	Compal	IAC peaks with VCORE EMI bead (PL504). reaches 8 A, triggers PROCHOT	Reserve PC736 PC737 PC738	X02 (0.4)
48	68	Charger for DSC	1/7	DELL	AC+ E5 Battery will not active H_PROCHOT funtion	Add PR749 and EC signal	X02 (0.4)
49	60	+DC_IN	2/6	Compal	Change PD2 material by ESD team request.	Change PD2 material and add PD4.	X02 (0.5)
50	69	Selector	2/6	Compal	To avoid +DOCK_PWR_BAR leakage voltage when system only with main battery	Add PD821 PQ820 PR896 PR897 PQ830 PC818 PU809	X02 (0.5)

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