

FIRENZE-R

CPU : Yonah 667
Chip Set : CALISTOGA & ICH7-M
Remarks : Mobility Platform

Model Name : FIRENZE-R
PBA Name : MAIN
PCB Code : BA41-00655A/B
Dev. Step : SR
Revision : 1.0
T.R. Date : 2006.03.09

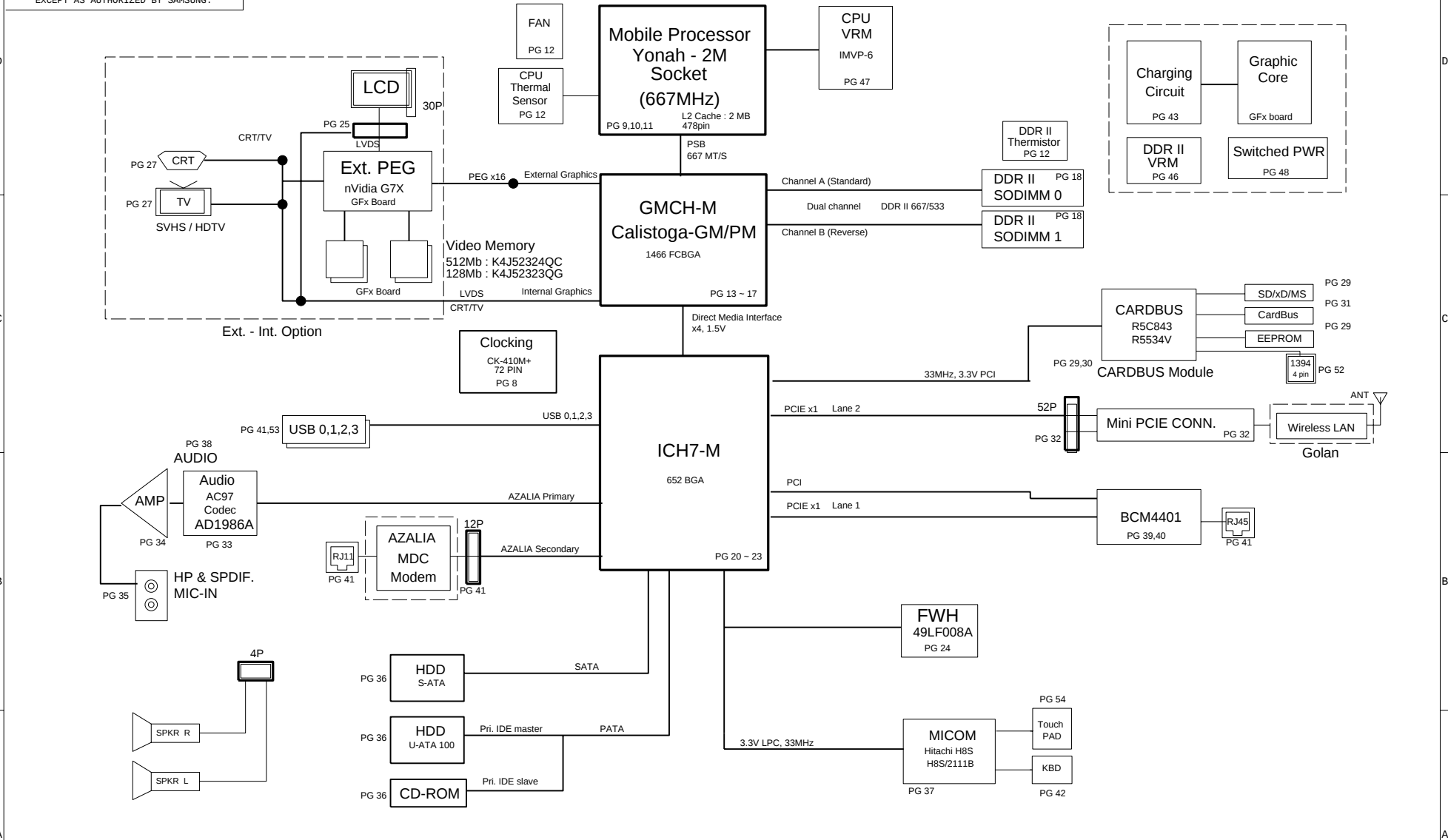
DRAW	CHECK	APPROVAL
SON,C.W	YUN,C.Y	LIM,J.G

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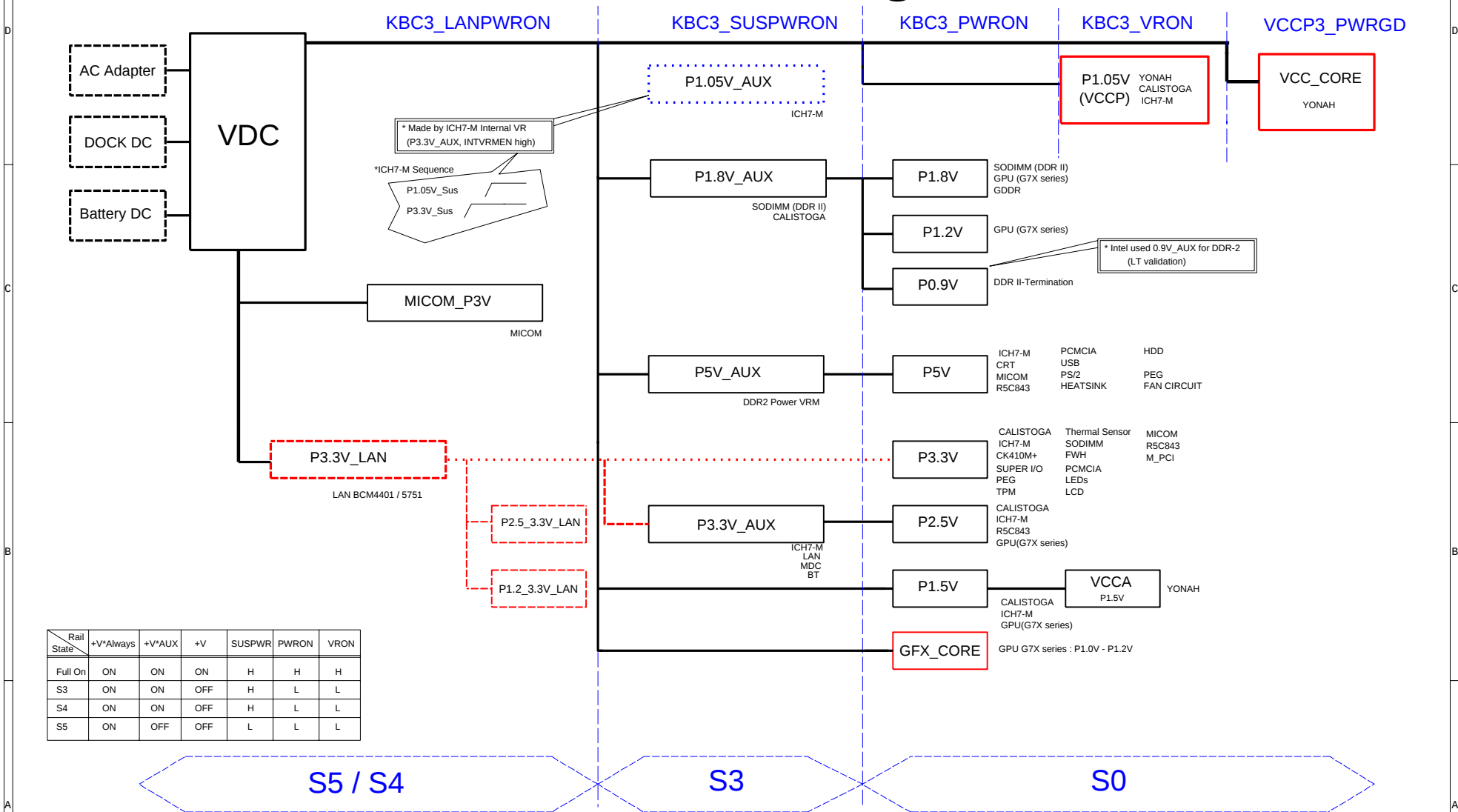
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APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	1 OF 55	

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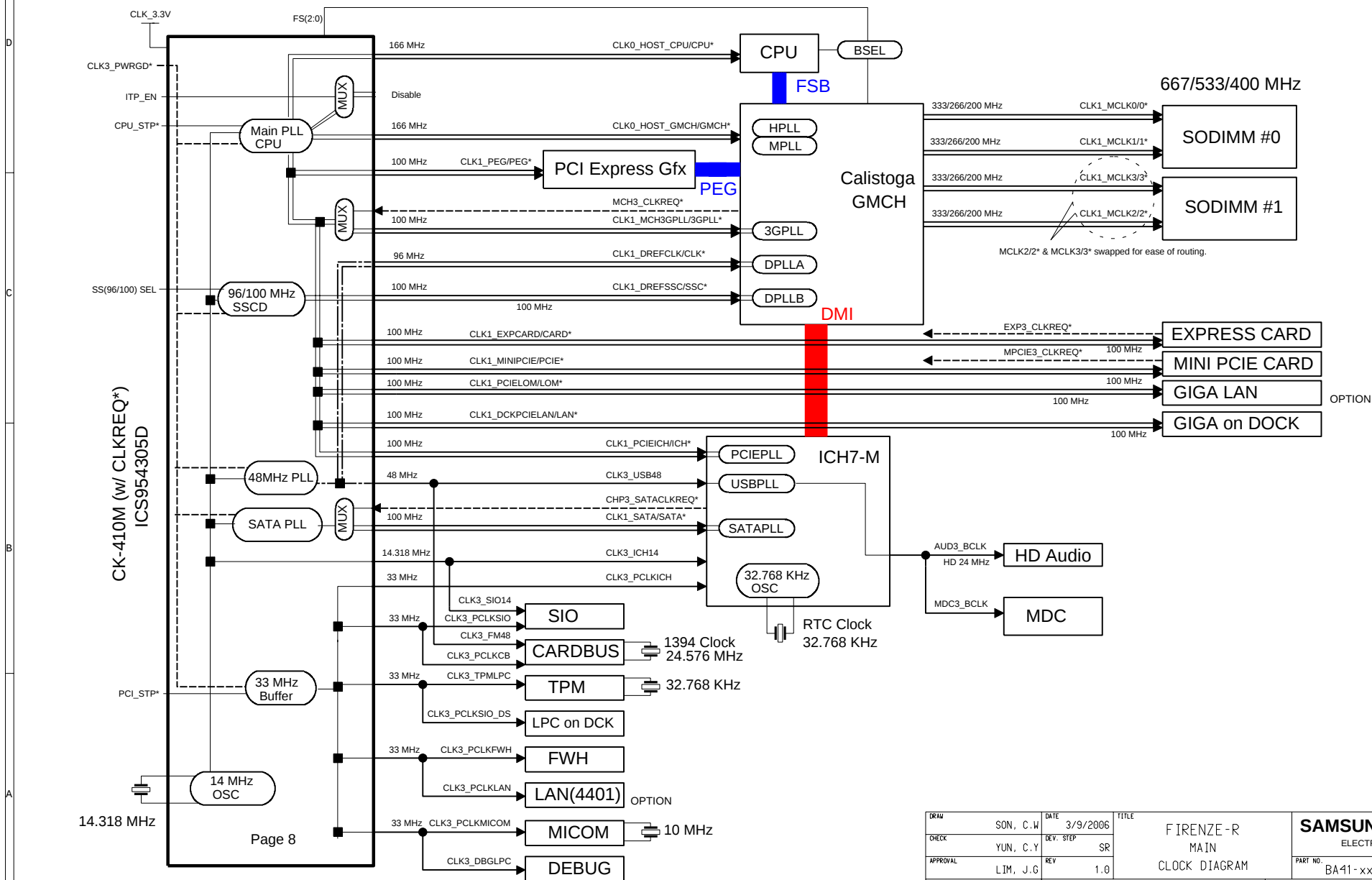


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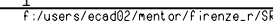
Power Diagram



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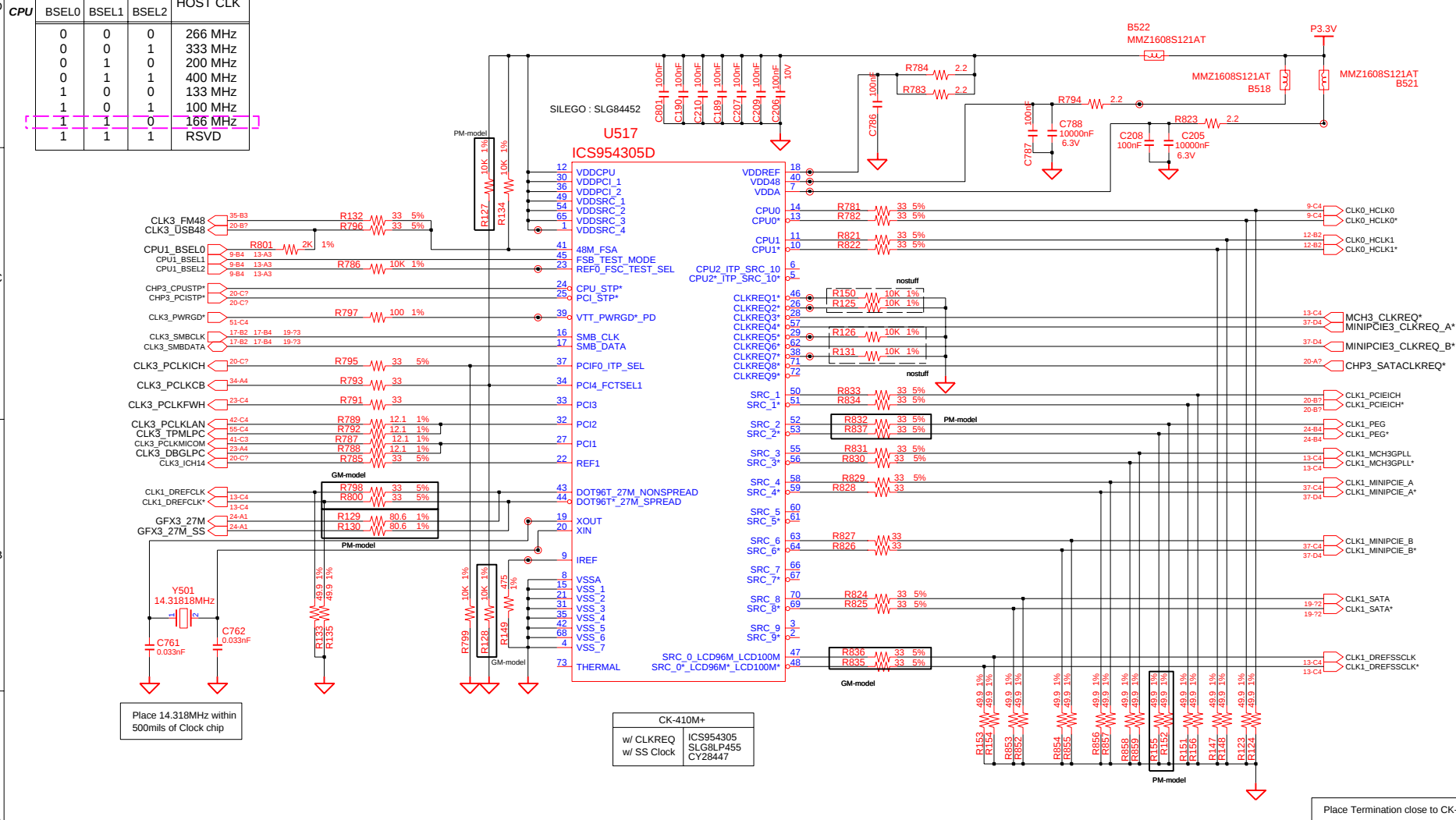
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APPROVAL	LIM, J.G	REV	1.0			
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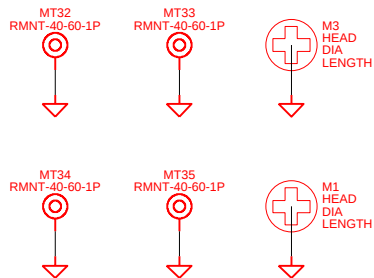
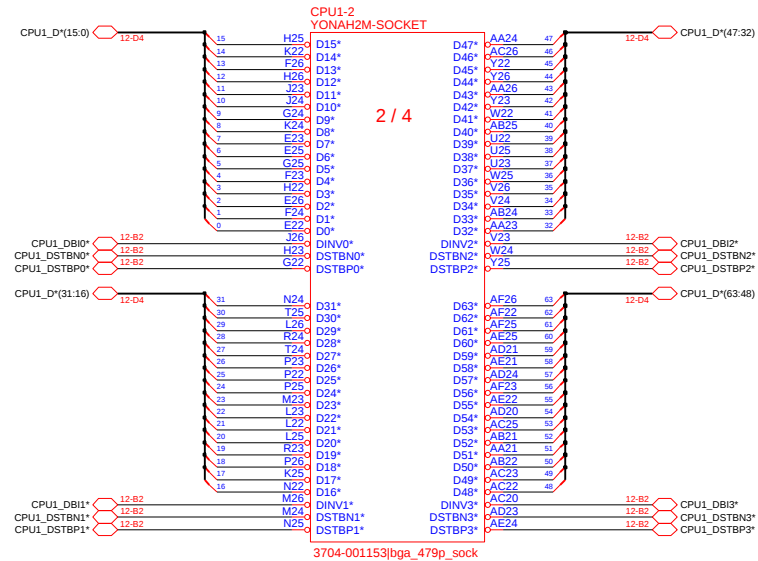
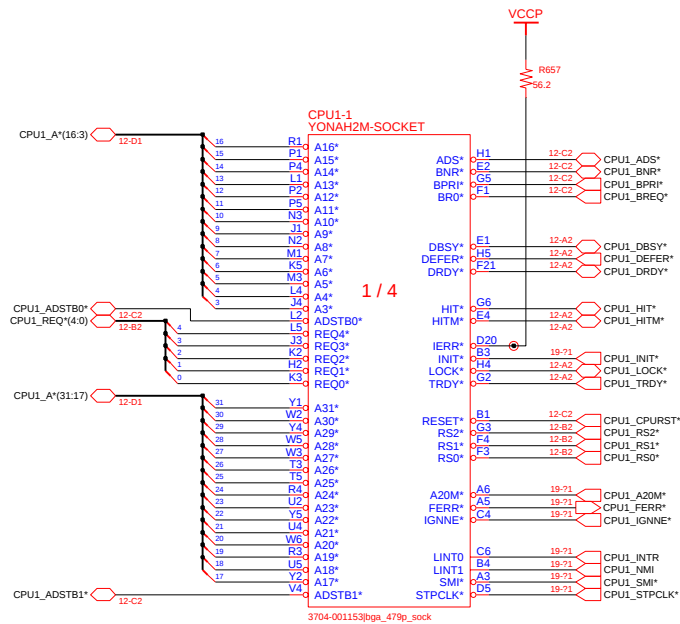
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FCTSEL1(43,44,47,48)	1: 27M & SRC0	0: DOT96 & LCD100
ITP_EN (5,6)	1: CPU_1TP pair	0: SRC pair

FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

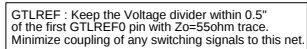


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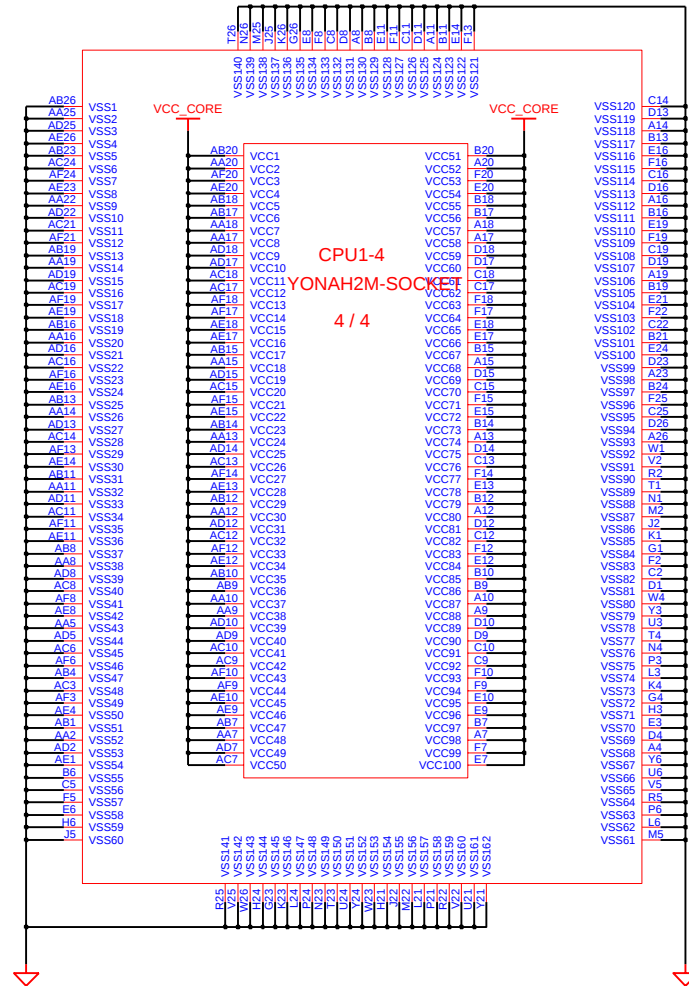
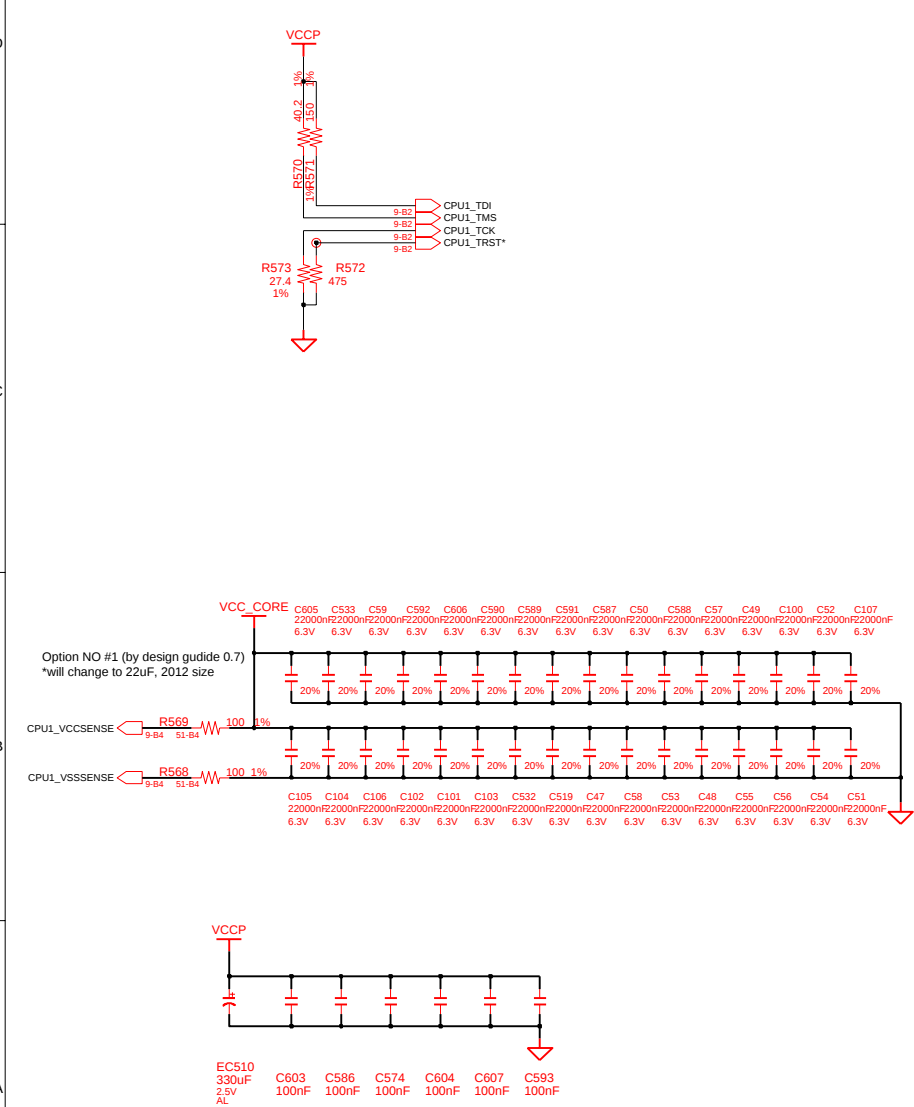
3 / 4

IMVP-6

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

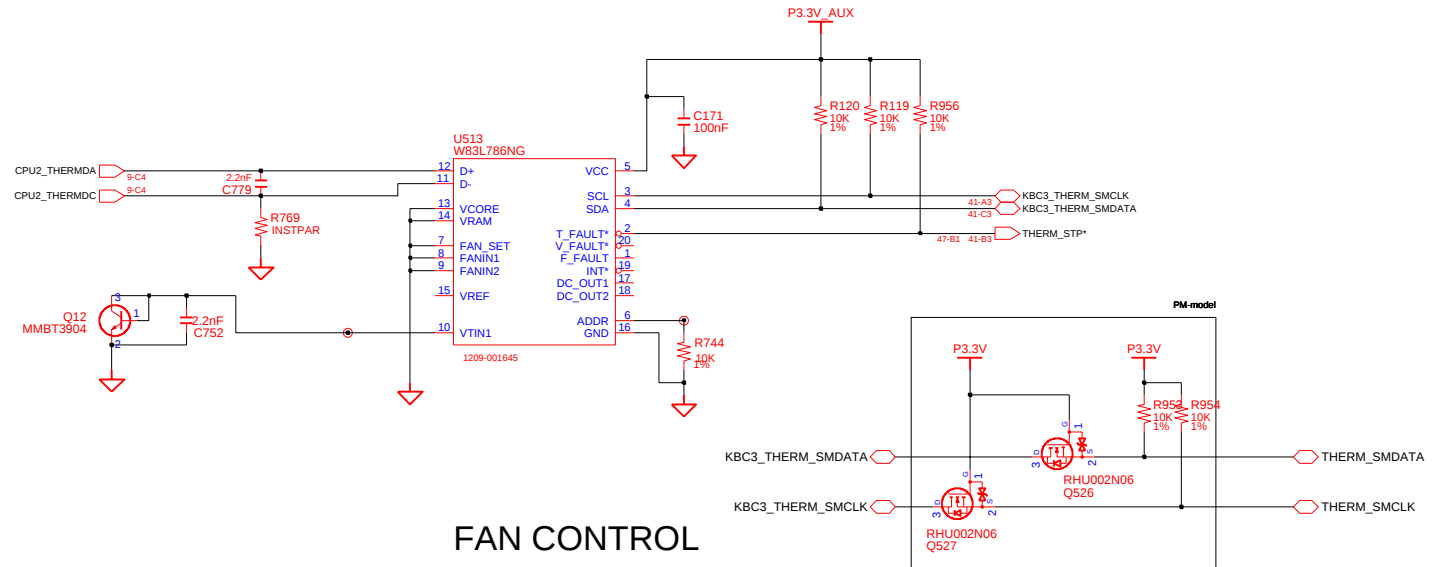
COM-22C-015(1996.6.5) REV. 3

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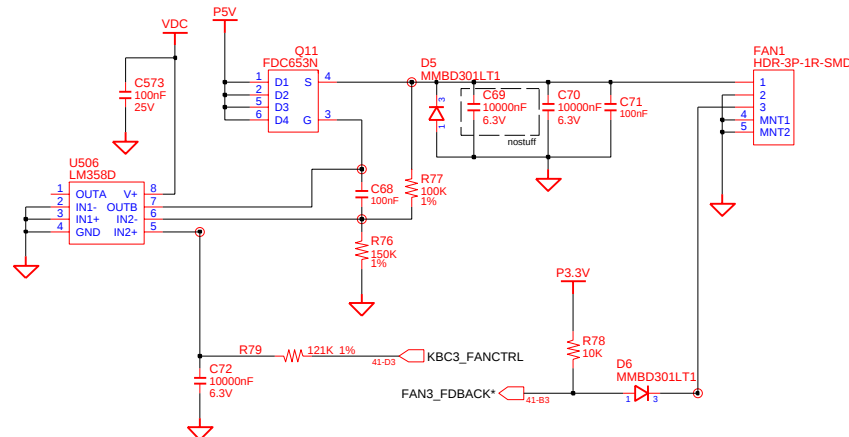


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR	MAIN	MAIN	
APPROVAL	LIM, J.G	REV	1.0	CPU(3/3)		
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	10 OF 55	

CPU/GFX Thermal Sensor

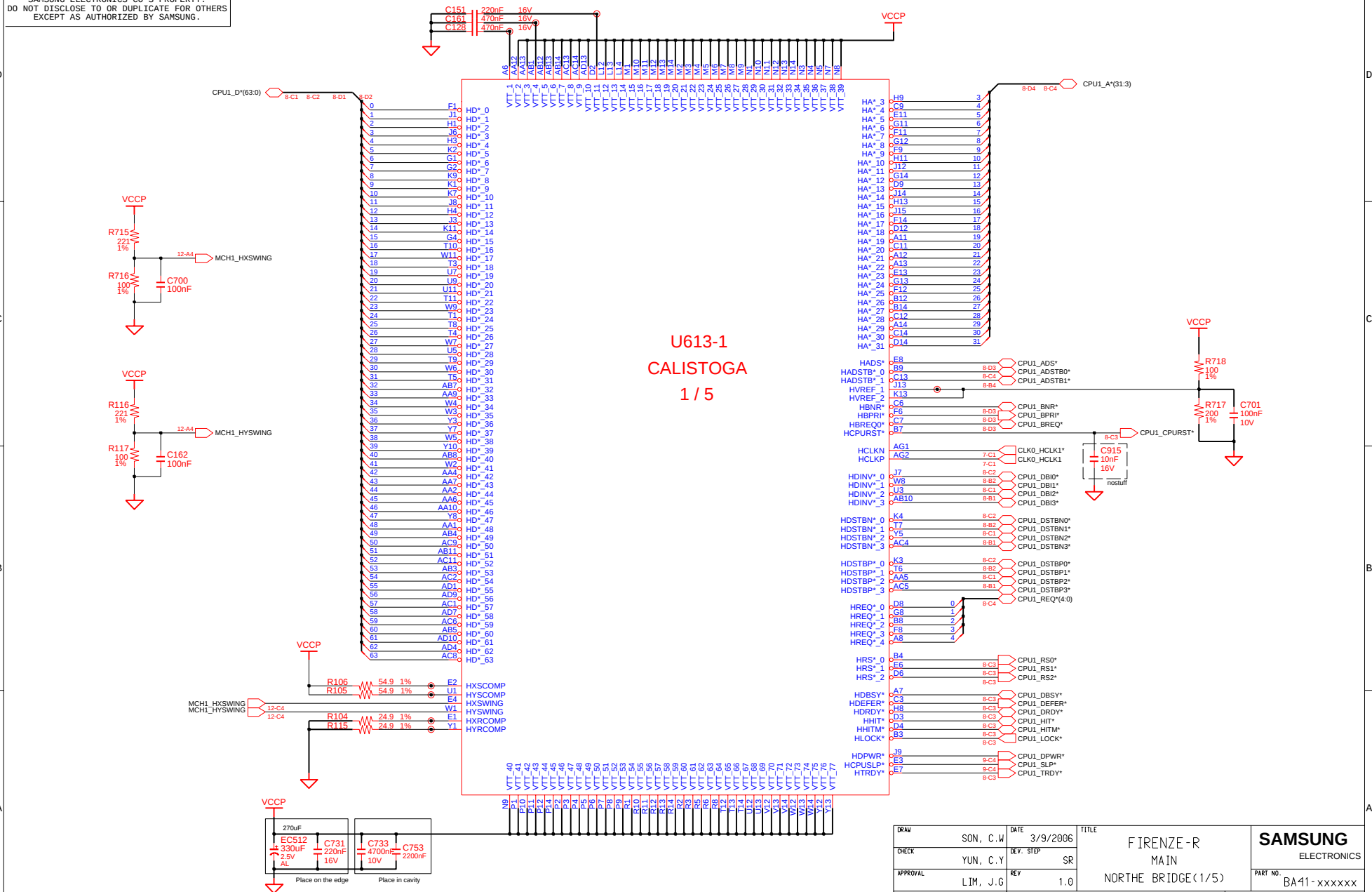


FAN CONTROL



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN THERMAL SENSOR/FAN CTRL	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR	REV	1.0	
APPROVAL	LIM, J.G	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	11	OF 55
MODULE CODE	undefined					

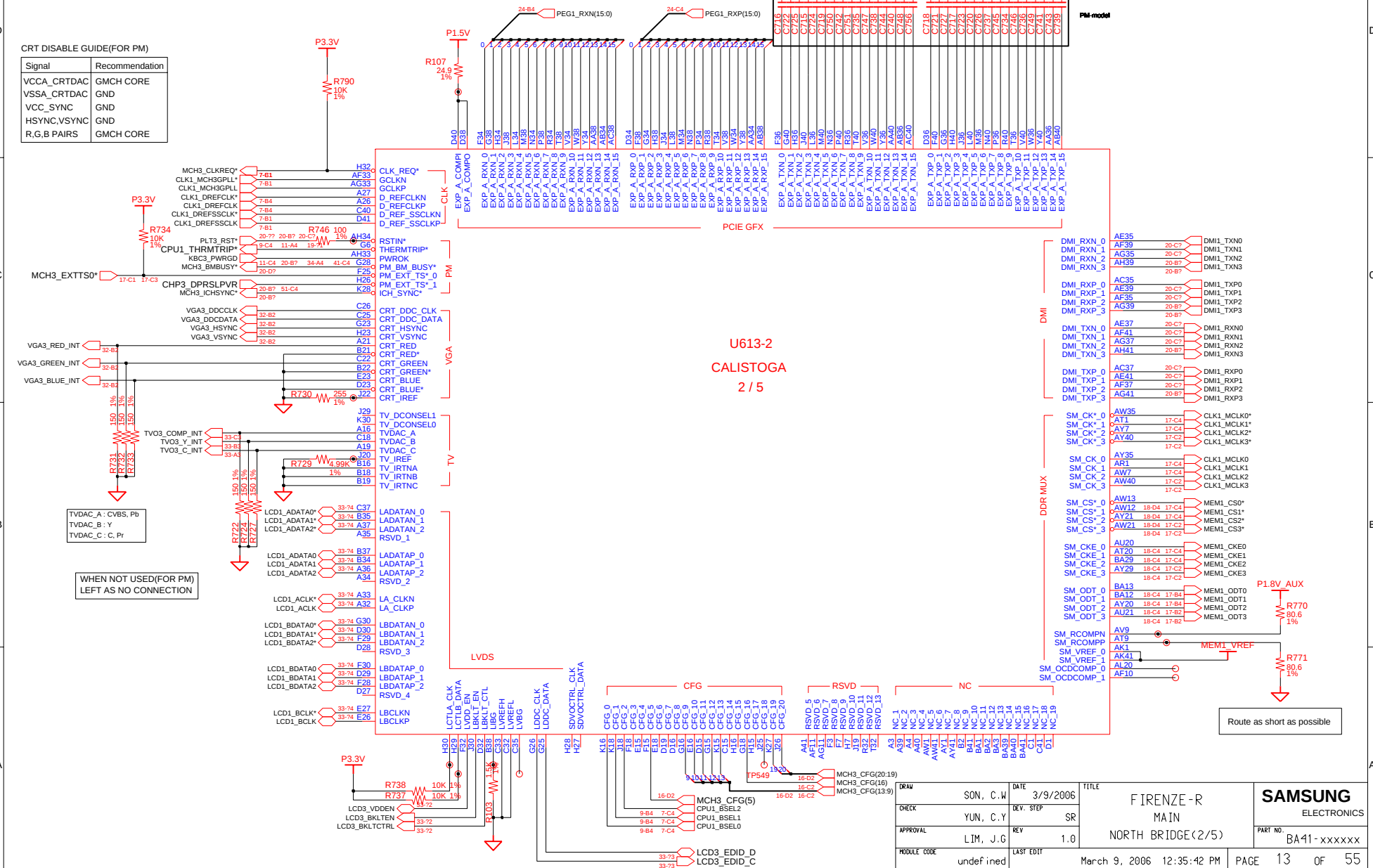
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CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
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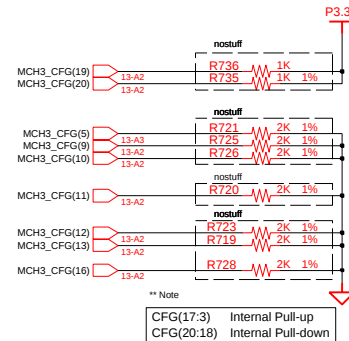
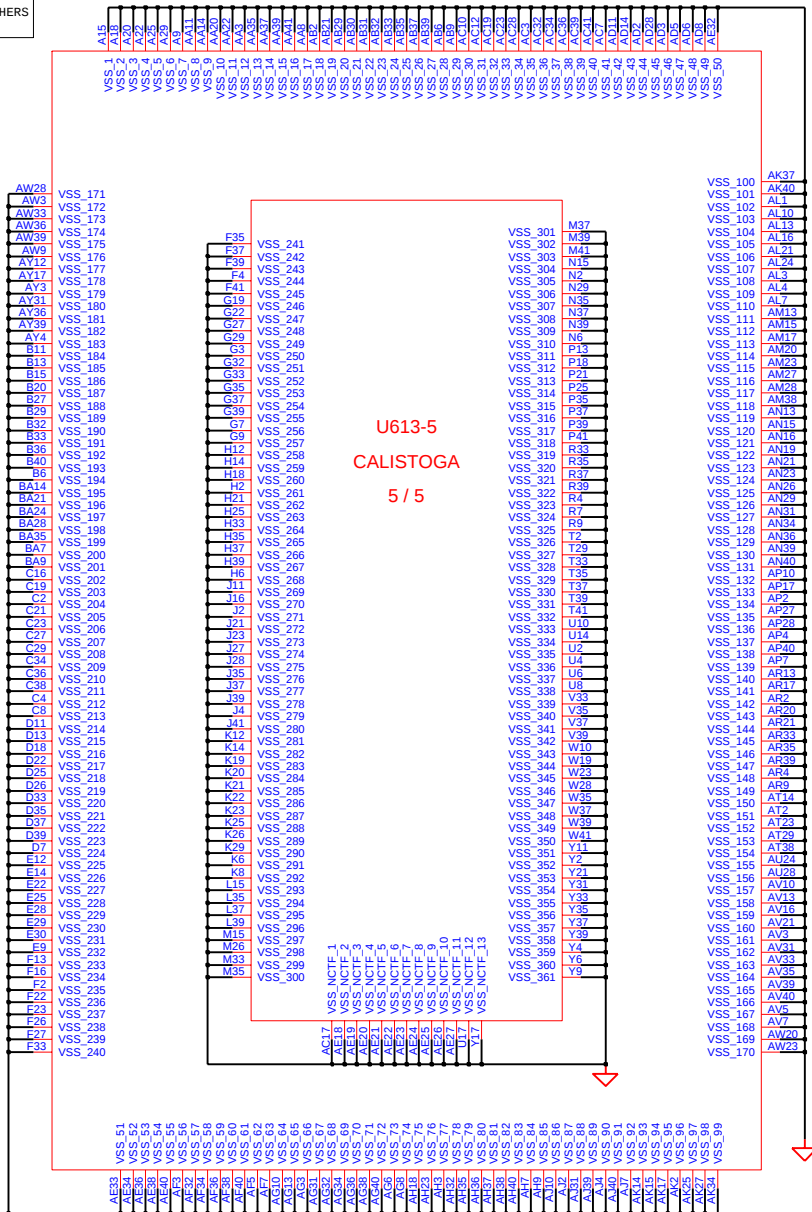
Signal	Recommendation
VCCA_CRTDAC	GMCH CORE
VSSA_CRTDAC	GND
VCC_SYNC	GND
HSYNC,VSYNC	GND
R,G,B PAIRS	GMCH CORE



SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED*	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN*	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE*	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK*	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOC_ALPHA*	
SDVOC_RED	EXP_TXP_4
SDVOC_ALPHA	
SDVOC_GREEN*	EXP_TXN_5
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_6
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_7
SDVOC_CLK*	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

COM-22C-015(1996.6.5) REV. 3



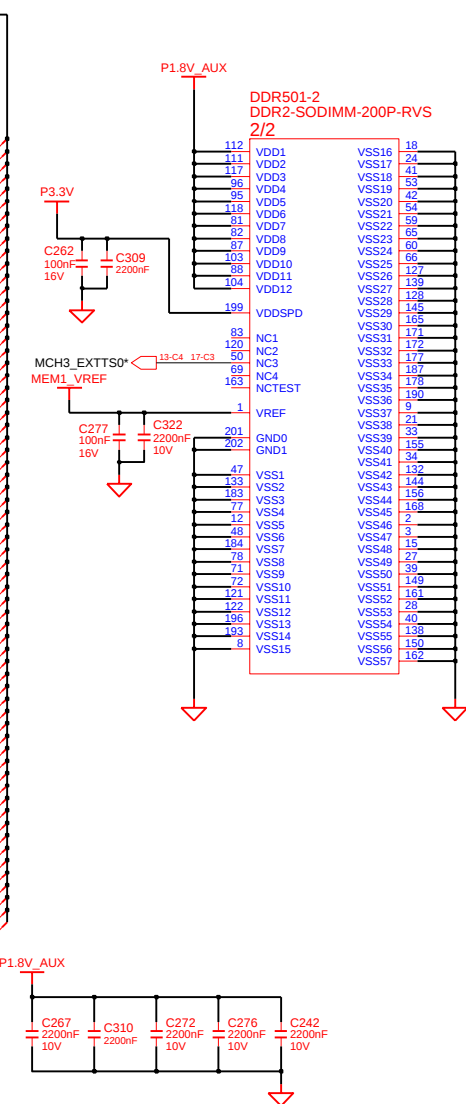
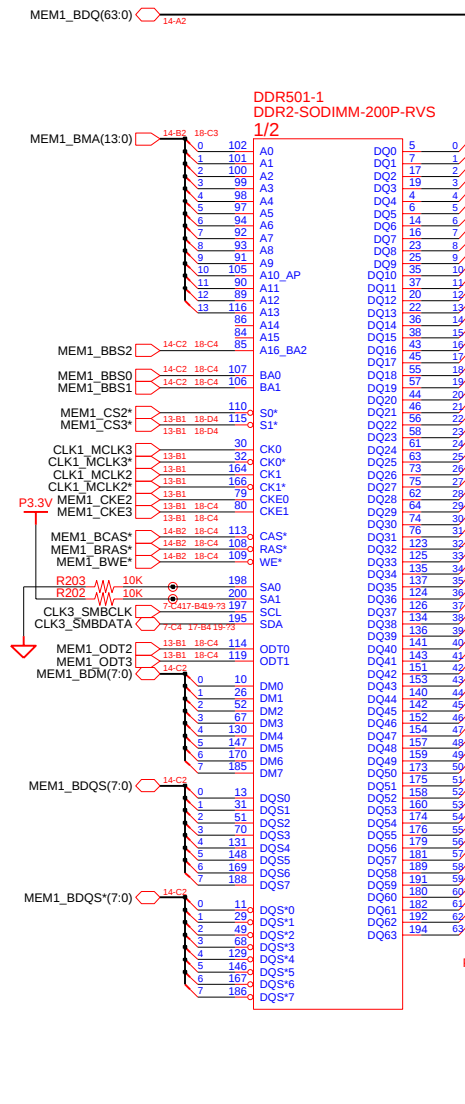
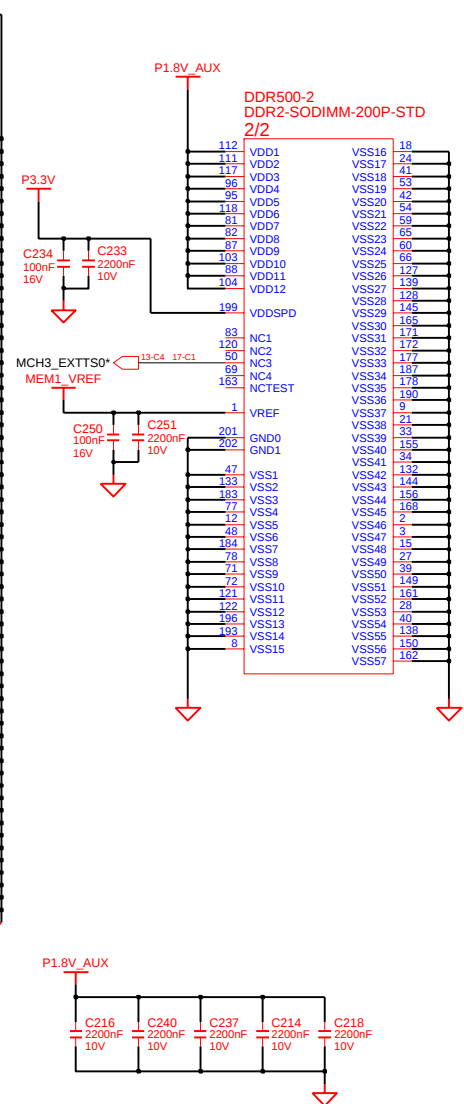


** Note *POCAFEH-10 Only (Remove in MP Model)

Current Setting (def.: default Option)		
CFG#	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	Reserved	DDR-II (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT	Dynamic ODT
	Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneously

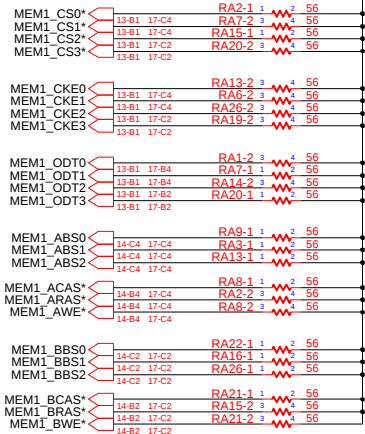
When CFG 13:12 are pulled down to '00', certain clocks within Calistoga will become free-running clocks. This will lead to a rise in avg. power, but eliminates any possible clock-timing marginalities involved in clock power-up/power-down. Intel strongly recommends leaving CFG 13:12 = NC (Internal PU to '11') to ensure low avg.power.

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APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	16	OF 55



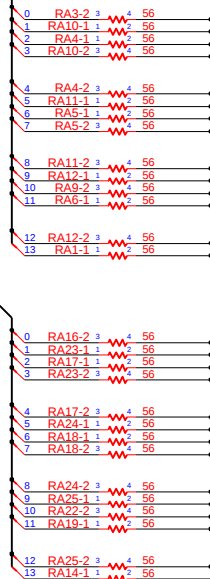
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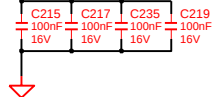


MEM1_AMA(13:0) 14-B4 17-D4

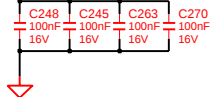
MEM1_BMA(13:0) 14-B2 17-D2



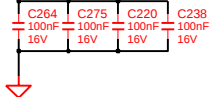
P1.8V_AUX



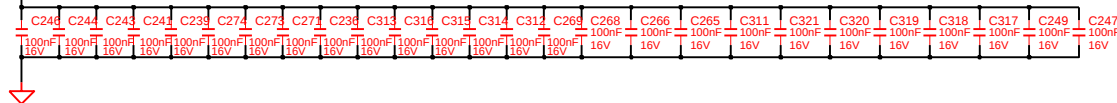
P1.8V_AUX



P1.8V_AUX

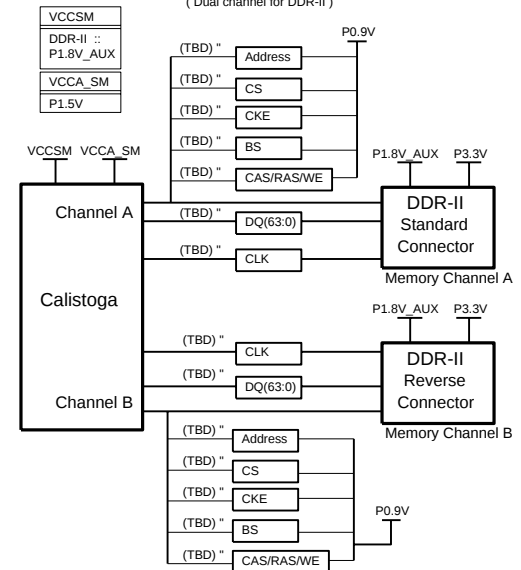


P0.9V



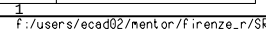
Memory Topology

(Dual channel for DDR-II)



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CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	18	OF 55

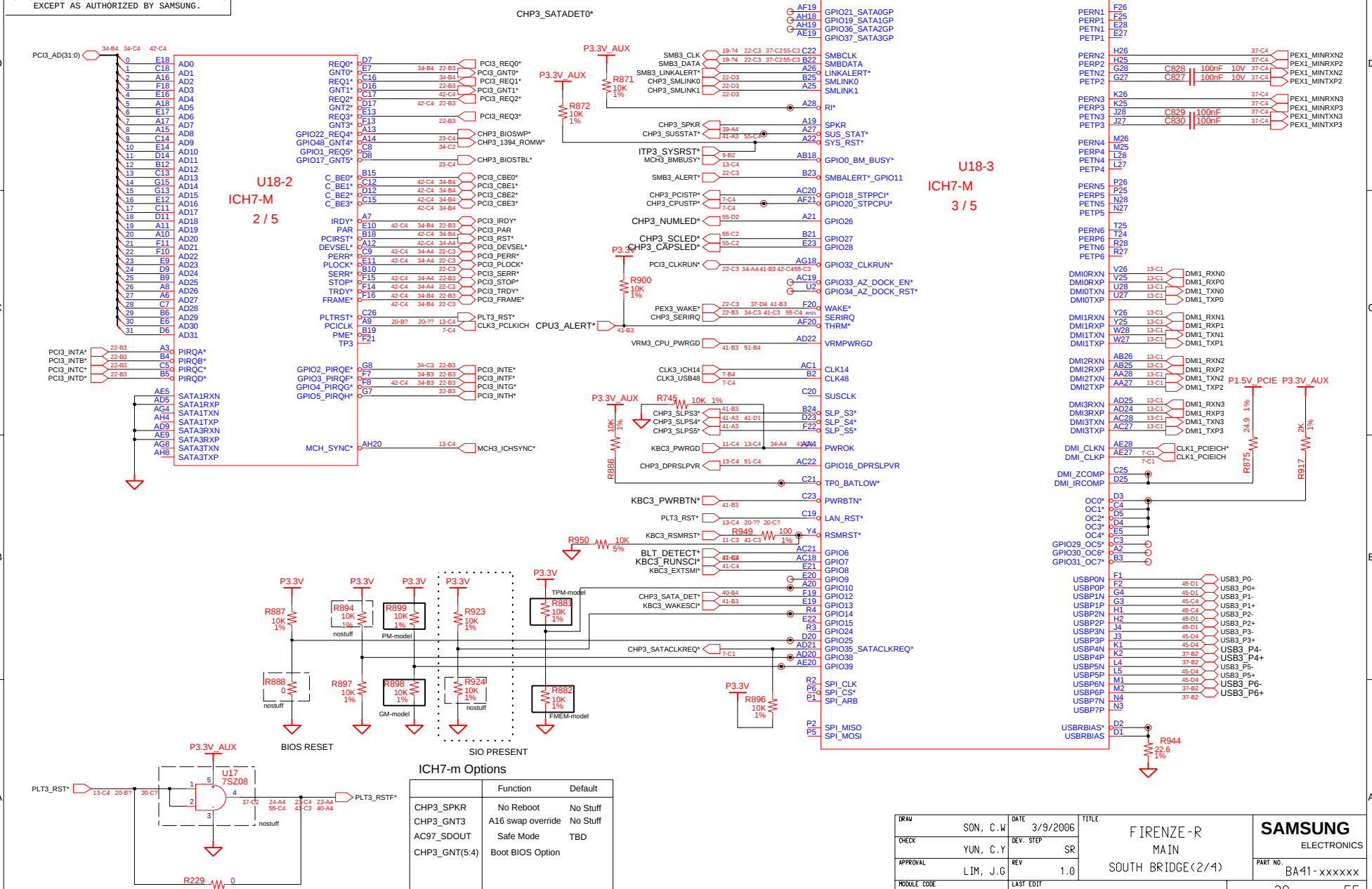
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DATE	3/9/2006	TITLE FIRENZE-R MAIN SOUTH BRIDGE(1/4)		SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx	
DRAW	SON, C.W.				
CHECK	YUN, C.Y.				
APPROVAL	LIM, J.G.	REV	1.0		
MODULE CODE		LAST EDIT		March 9, 2006 12:35:42 PM PAGE 19 OF 55	

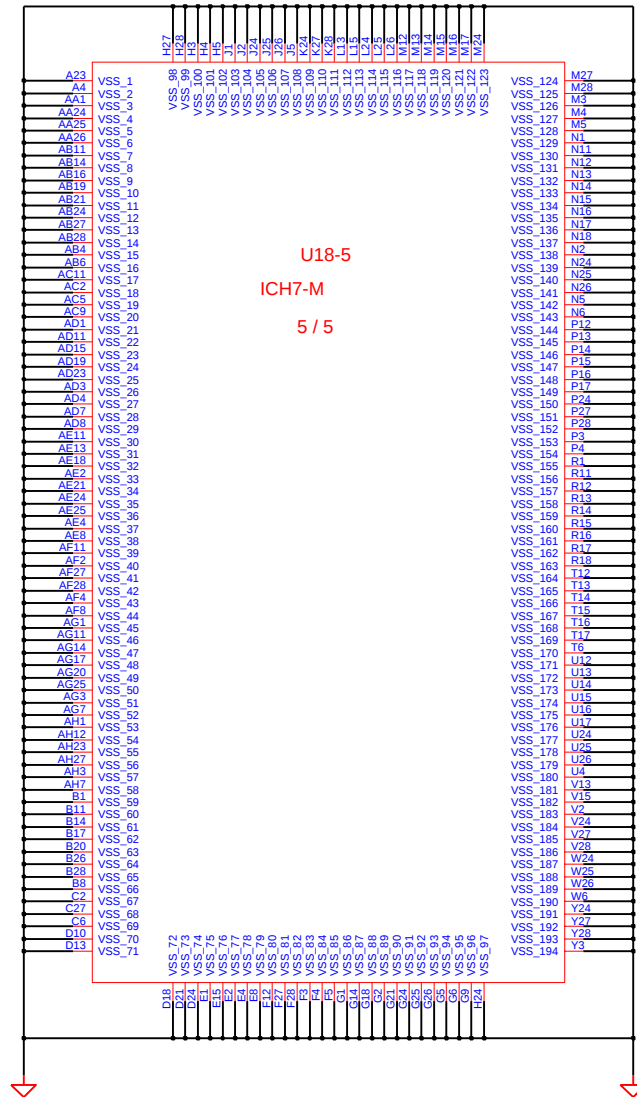
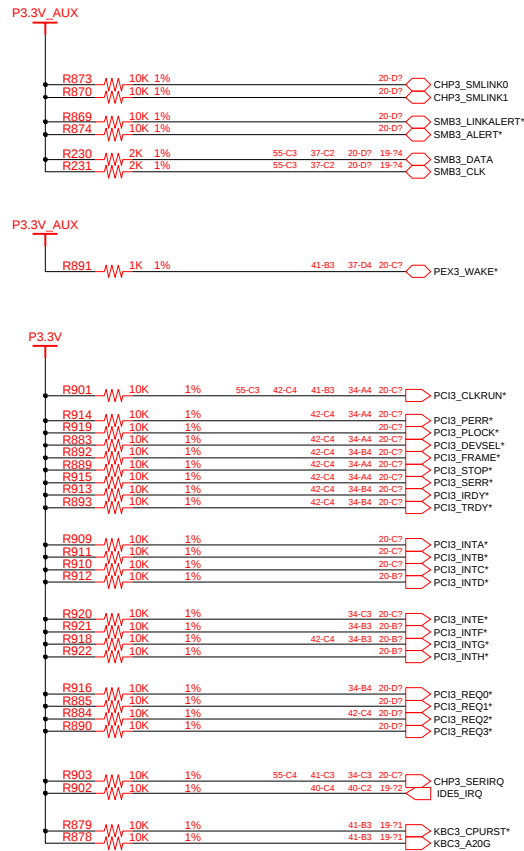
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AC caps : PCIe need to be within 250mils of the driver
Resistor for Test : Place Stuffing Option to minimize stubs

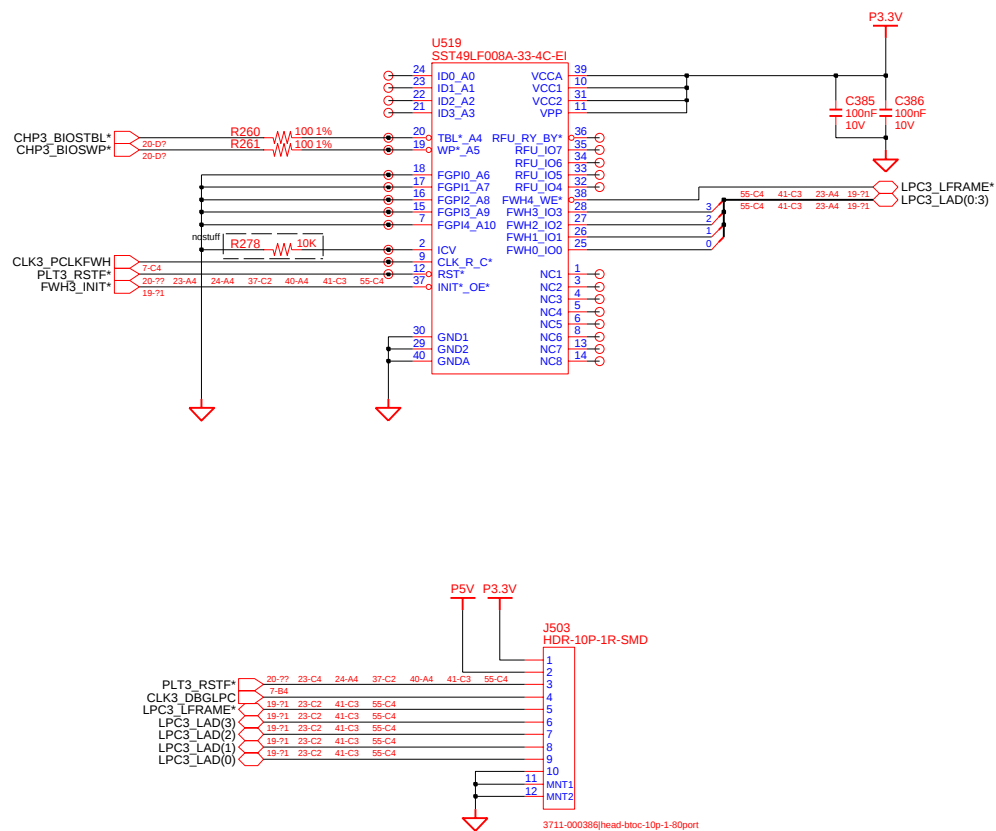




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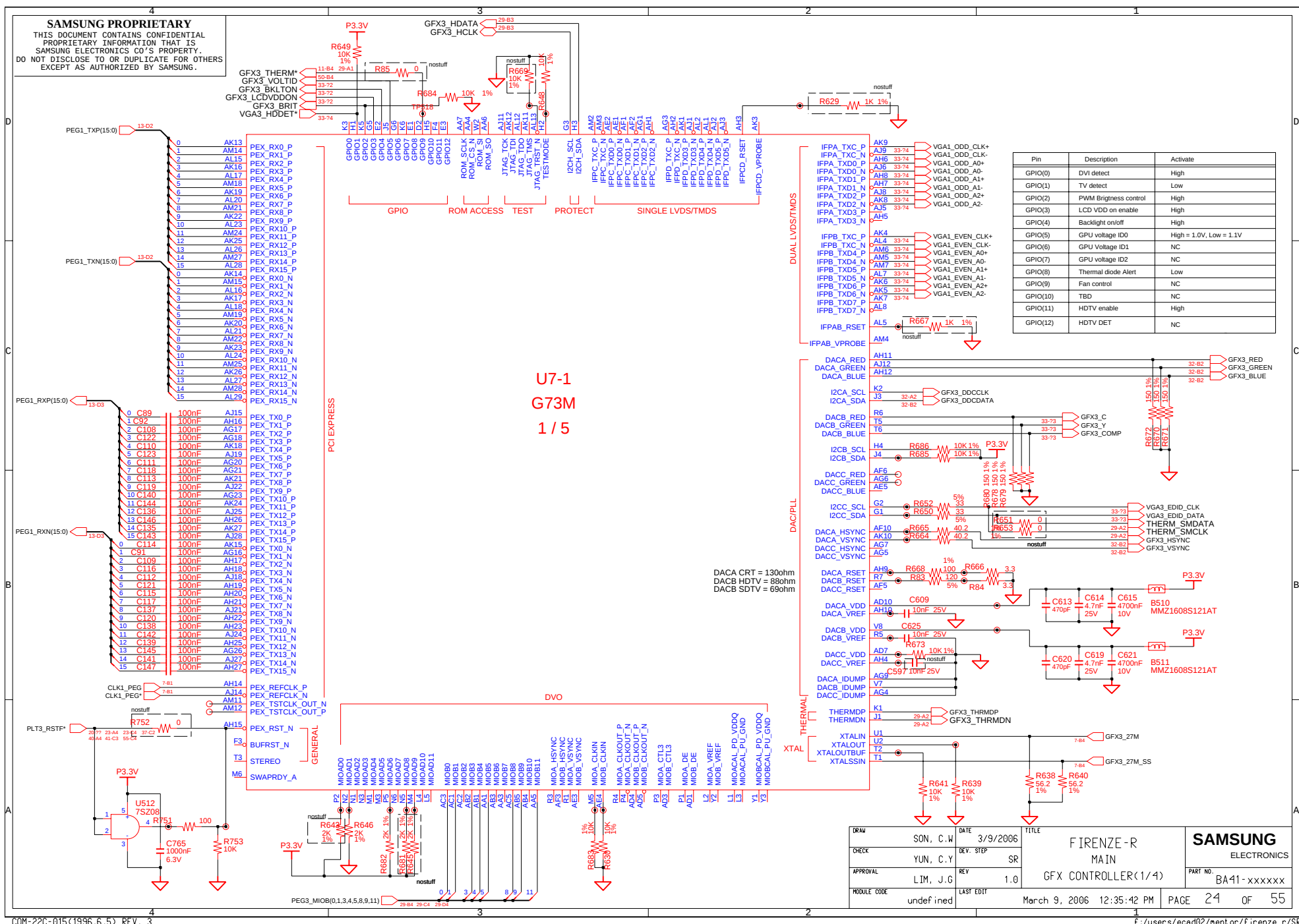
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- | | | | |
|----|------------------------------------|----|---------------------------------|
| 02 | VERIFY REAL MODE | 66 | CONFIGURE ADVANCE CACHE REG. |
| 03 | DISABLE NMI | 6A | DISPLAY EXTERNAL CACHE SIZE |
| 04 | GET CPU TYPE | 6C | DISPLAY SHADOW MESSAGE |
| 06 | INIT. SYSTEM H/W | 6E | DISPLAY NON-DISPOSABLE SEGMENT |
| 08 | INIT. CHIPSET REG. | 70 | DISPLAY ERROR MESSAGE |
| 09 | SET IN POST FLAG | 72 | CHECK FOR CONFIGURATION ERROR |
| 0A | INIT CPU.REG | 74 | TEST REAL-TIME CLOCK |
| 0B | CPU CACHE ON | 76 | CHECK FOR KEYBOARD ERROR |
| 0C | INIT.CACHE TO POST | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| 0E | INIT. I/O VALUE | 7E | TEST COPROCESSER IF PRESENT |
| 0F | ENABLE THE L-BUS IDE | 80 | DISABLE ON-BOARD I/O PORT |
| 10 | INIT. POWER MANAGER | 82 | DETECT AND INSTALL EXT.RS232C |
| 11 | LOAD ALTERNATE REG. | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET | 86 | RE-INIT. ON-BOARD I/O PORT |
| | WITH INITIAL POST VALUE | 88 | INIT. BIOS DATA ROM |
| 14 | INIT. KEYBOARD CONTROLLER | 8A | INIT.EXTENDED BIOS DATA AREA |
| 16 | CHECK CHECKSUM | 8C | INIT. FDD CONTROLLER |
| 18 | 8254 TIMER INIT. | 9A | SHADOW OPTION ROMS |
| 1A | 8237 DMA CONTROLLER INIT. | 9C | SETUP POWER MANAGEMENT |
| 1C | RESET INTERRUPT CONTROLLER | 9E | ENABLE H/W INTERRUPT |
| 20 | TEST DRAM REFRESH | A0 | SET TIME OF DAY |
| 22 | TEST 8742 KEYBOARD CONTROLLER | A4 | INIT. TYPEMATIC RATE |
| 24 | SET ES SEGMENT REG. TO 4GB | A8 | ERASE F2 PROMPT |
| 26 | ENABLE A20 | AA | SCAN FOR F2 KEY STROKE |
| 28 | AUTO SIZING DRAM | AC | ENTER SETUP |
| 32 | COMPUTE THE CPU SPEED | AE | CLEAR IN POST FLAG |
| 34 | TESET CMOS RAM | B0 | CHECK FOR ERRORS |
| 38 | SHADOW SYSTEM BIOS ROM | B2 | POST DONE-PREPARE TO BOOT O/S |
| 3A | AUTO SIZING CACHE | B4 | ONE BEEP |
| 3C | CONFIGURE ADVANCED CHIPSET REG. | B6 | CHECK PASSWORD (OPTION) |
| 3D | LOAD ALTER REG. WITH CMOS VALUE | B7 | ACPI INIT |
| 42 | INIT. INTERRUPT VECTOR | BA | DMI INIT |
| 44 | INIT. BIOS INTERRUPT | BE | CLEAR SCREEN |
| 46 | CHECK ROM COPYRIGHT NOTICE | C0 | TRY BOOT WITH INT19 |
| 47 | INIT. I20 SUPPORT IF INSTALLED | D0 | INTERRUPT HANDLER ERROR |
| 48 | CHECK VIDEO CONFIGURE AGAINST CMOS | D2 | UNKNOWN INTERRUPT ERROR |
| 49 | INIT. PCI BUS AND DEVICE | D4 | PENDING INTERRUPT ERROR |
| 4A | INIT. ALL VIDEO BIOS ROM | D6 | SHUTDOWN 5 |
| 4C | SHADOW VIDEO BIOS ROM | D8 | SHUTDOWN ERROR |
| 50 | DISPLAY CPU TYPE AND SPEED | DA | EXTENDED BLOCK MOVE |
| 52 | TEST KEYBOARD | DC | SHUTDOWN 10 |
| 54 | SET KEYCLICK IF ENABLED | 89 | ENABLE NMI |
| 56 | ENABLE KEYBOARD | 90 | INIT. HDD CONTROLLER |
| 58 | TEST FOR UNEXPECTED INTERRUPTS | 91 | INIT. LOCAL BUS HDD CONTROLLER |
| 5A | DISPLAY "PRESS SETUP" | 92 | JUMP TO USER PATCH 2 |
| 5C | TEST RAM BETWEEN 512K AND 640K | 94 | DISABLE A20 ADDRESS LINE |
| 60 | TEST EXTENDED MEMORY | 96 | CLEAR HUGE ES SEGMENT REG. |
| 62 | TEST EXTENDED MEMORY ADDRESS LINE | 98 | SEARCH FOR OPTION ROMS |
| 64 | JUMP TO USER PATCH 1 | | |

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG
CHECK	YUN, C.Y	DEV. STEP	SR		MAIN	ELECTRONICS
APPROVAL	LIM, J.G	REV	1.0		FWH	PART NO.
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM			BA41-xxxxxx
				PAGE	23	OF 55

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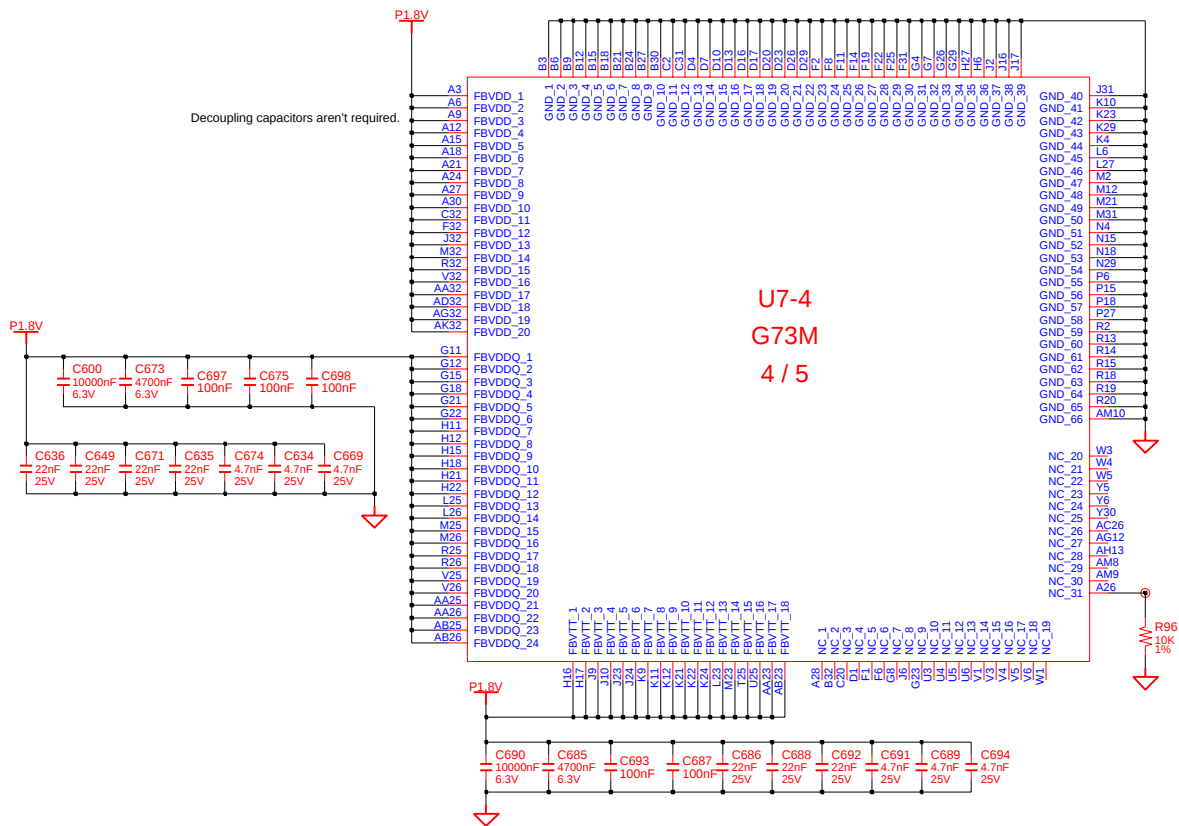


Pin	Description	Activate
GPIO(0)	DVI detect	High
GPIO(1)	TV detect	Low
GPIO(2)	PWM Brightness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU voltage ID0	High = 1.0V, Low = 1.1V
GPIO(6)	GPU Voltage ID1	NC
GPIO(7)	GPU voltage ID2	NC
GPIO(8)	Thermal diode Alert	Low
GPIO(9)	Fan control	NC
GPIO(10)	TBD	NC
GPIO(11)	HDTV enable	High
GPIO(12)	HDTV DET	NC

2 / 5

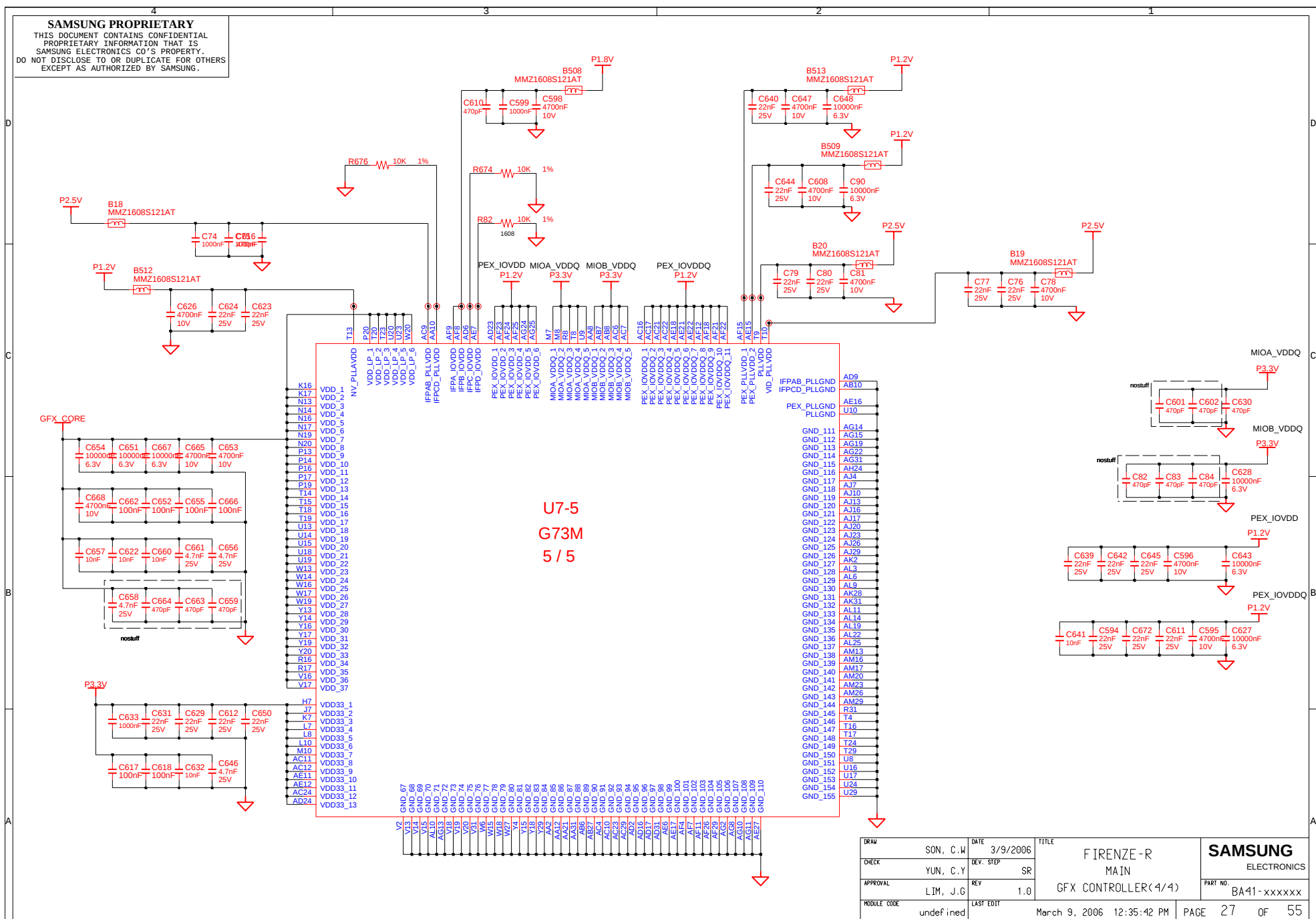
3 / 5

COM-22C-015(1996.6.5) REV. 3

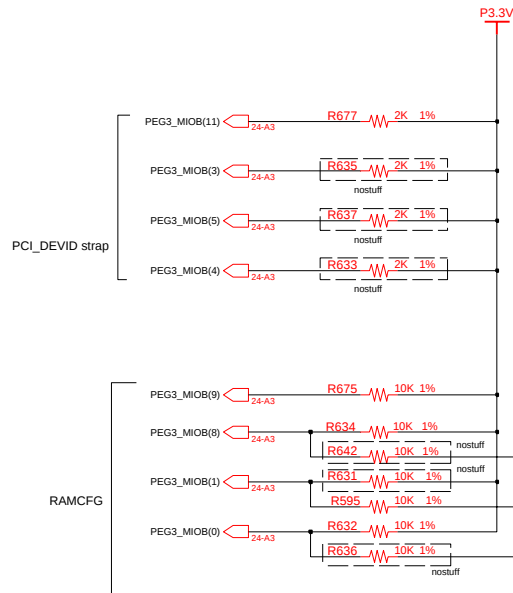


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN GFX CONTROLLER(3/4)	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	26	OF 55

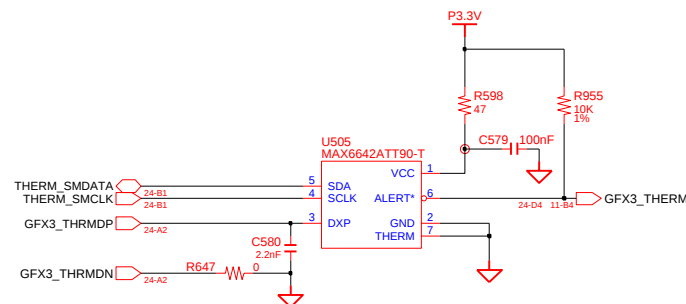
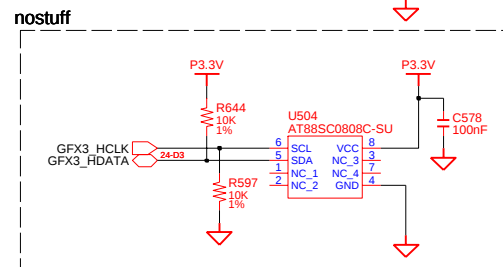
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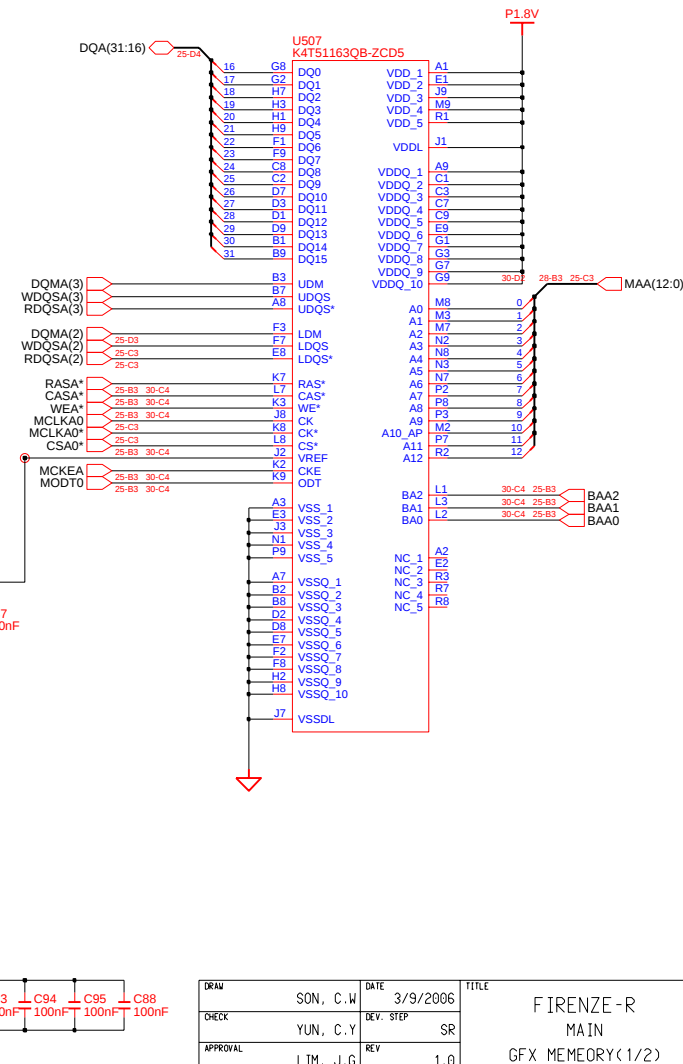
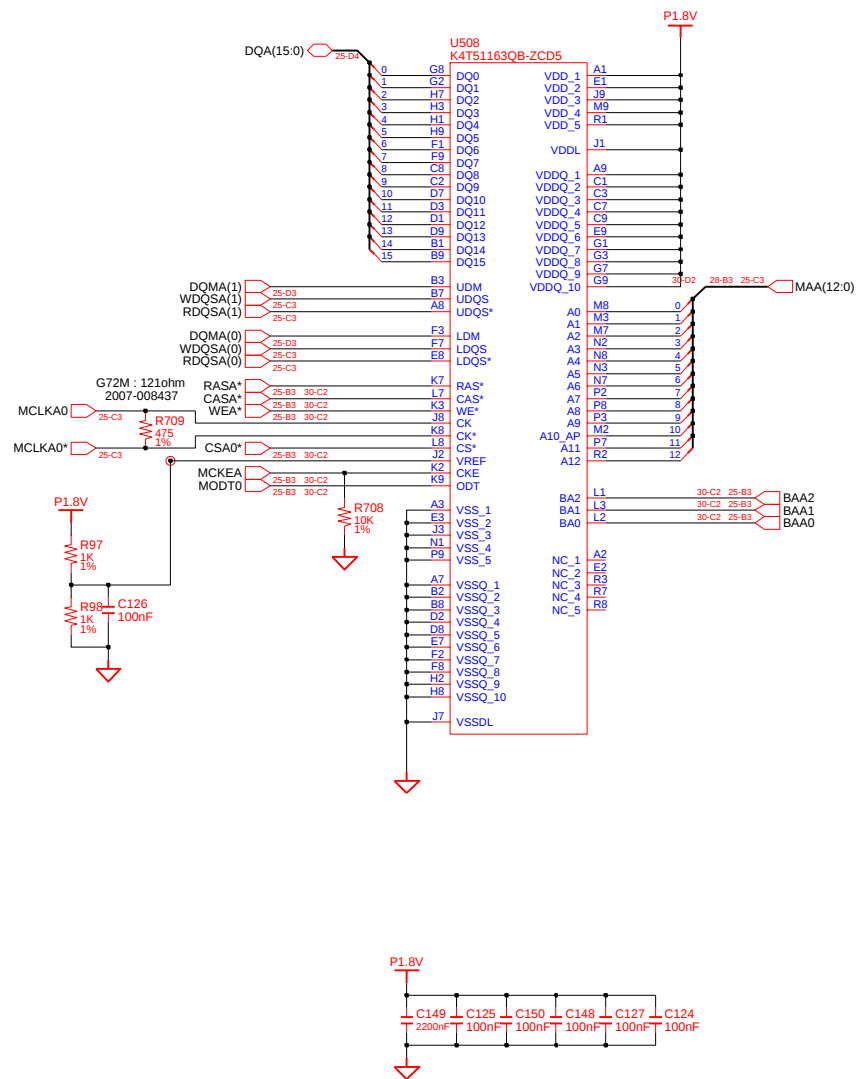
Straps	Pin # (Rev.A02)	Descriptions
SUB_VENDOR	MIOAD(1)	0 : No BIOS 1 : Read from BIOS(Default)
RAMCFG(3:0) [9,8,1,0]	MIOB(9) MIOB(8) MIOB(1) MIOB(0)	1001 : samsung GDDR2 256Mbit 1010 : infineon GDDR2 256Mbit 1101 : samsung GDDR2 512Mbit 1110 : infineon GDDR2 512Mbit
CRYSTAL(1:0)	MIOB(2) MIOB(6)	01 : 14.318 MHz 10 : 27 MHz (Default) 11 : Unknown 00 : 13.5 MHz
TV_MODE(1:0)	MIOAD(7) MIOAD(10)	00 : SECAM 01 : NTSC (Default) 10 : PAL 11 : CRT
PCI_DEVID(3:0) [11,3,5,4]	MIOB(11) MIOB(3) MIOB(5) MIOB(4)	72M : 0X01D8 72M-V : 0X01D7 73M : 0X0398
ROM_TYPE(1:0)	MIOB(10) MIOBVSNC	No ROM (NC)
USER STRAP	MIOAD(2:5)	EDID



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN GFX THERMAL SENSOR	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	28	OF 55

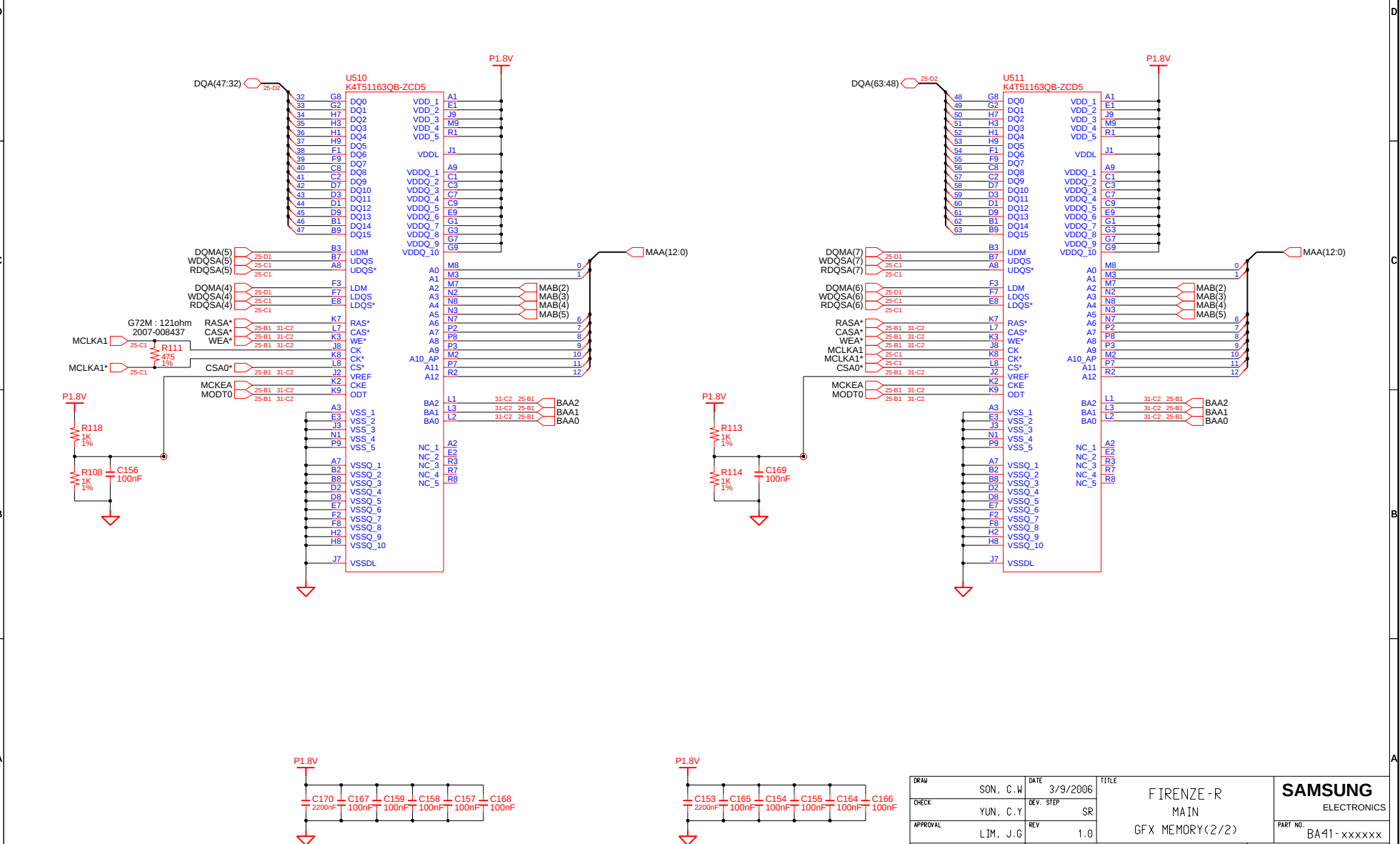
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A-channel



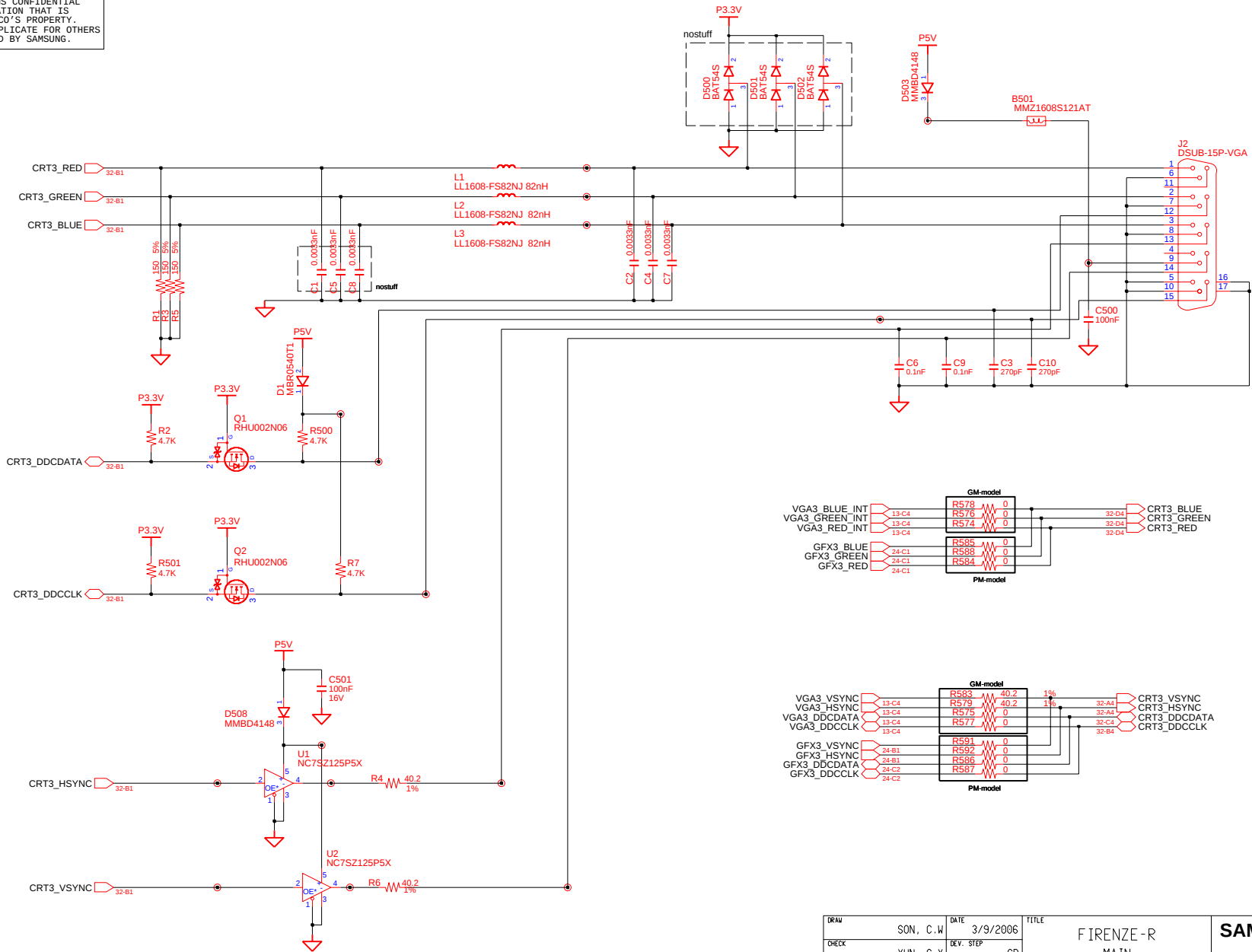
DATE	3/9/2006	TITLE FIRENZE-R MAIN GFX MEMEORY(1/2)			SAMSUNG ELECTRONICS				
CHECK	DEV: STEF							SR	
APPROVAL	REV							1.0	
MODULE CODE		undefined	LAST EDIT		March 9, 2006 12:35:42 PM	PAGE	29	OF	55

A-channel



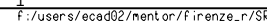
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN GFX MEMORY(2/2)	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	30 OF 55	

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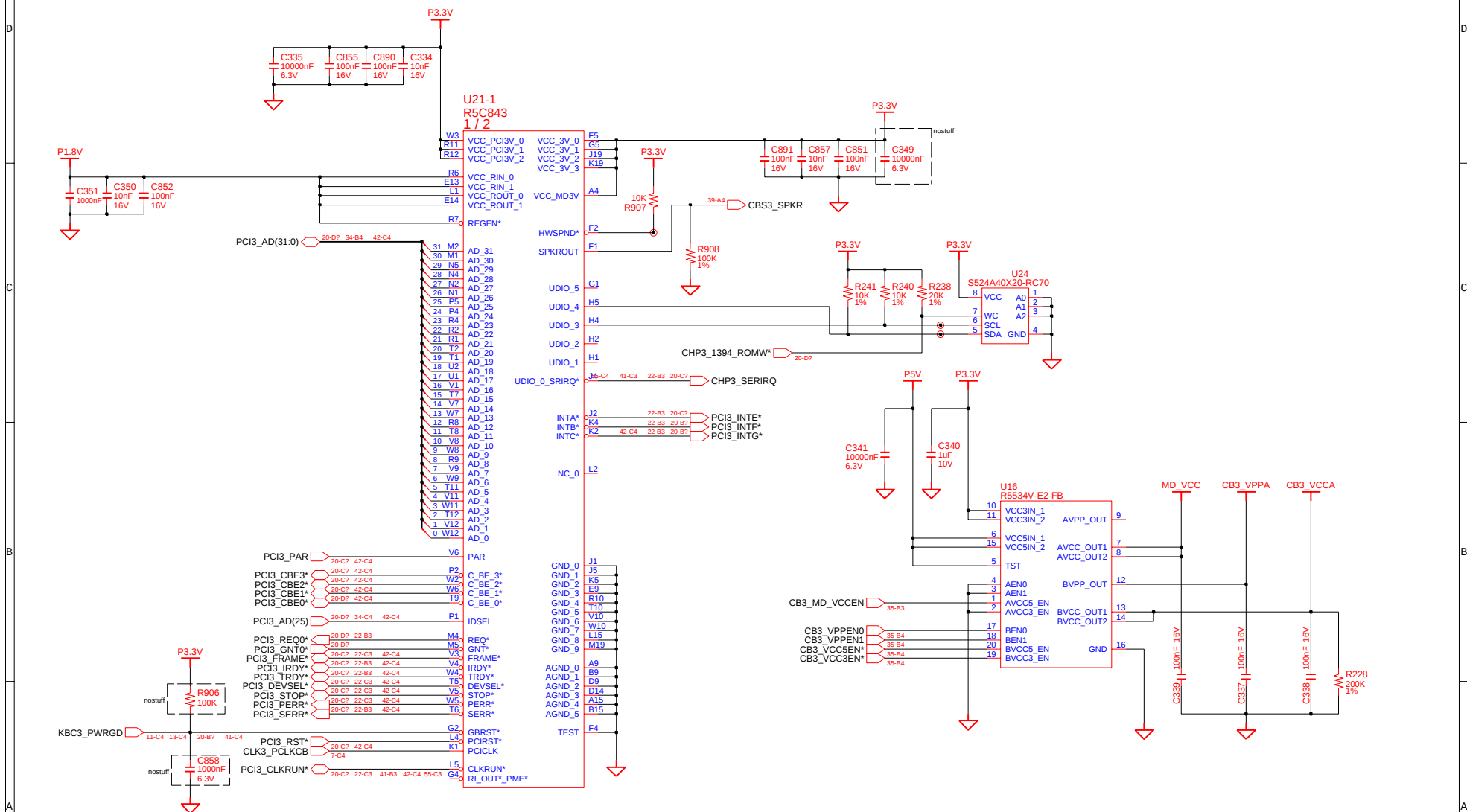


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CRT PORT	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	31	OF 55

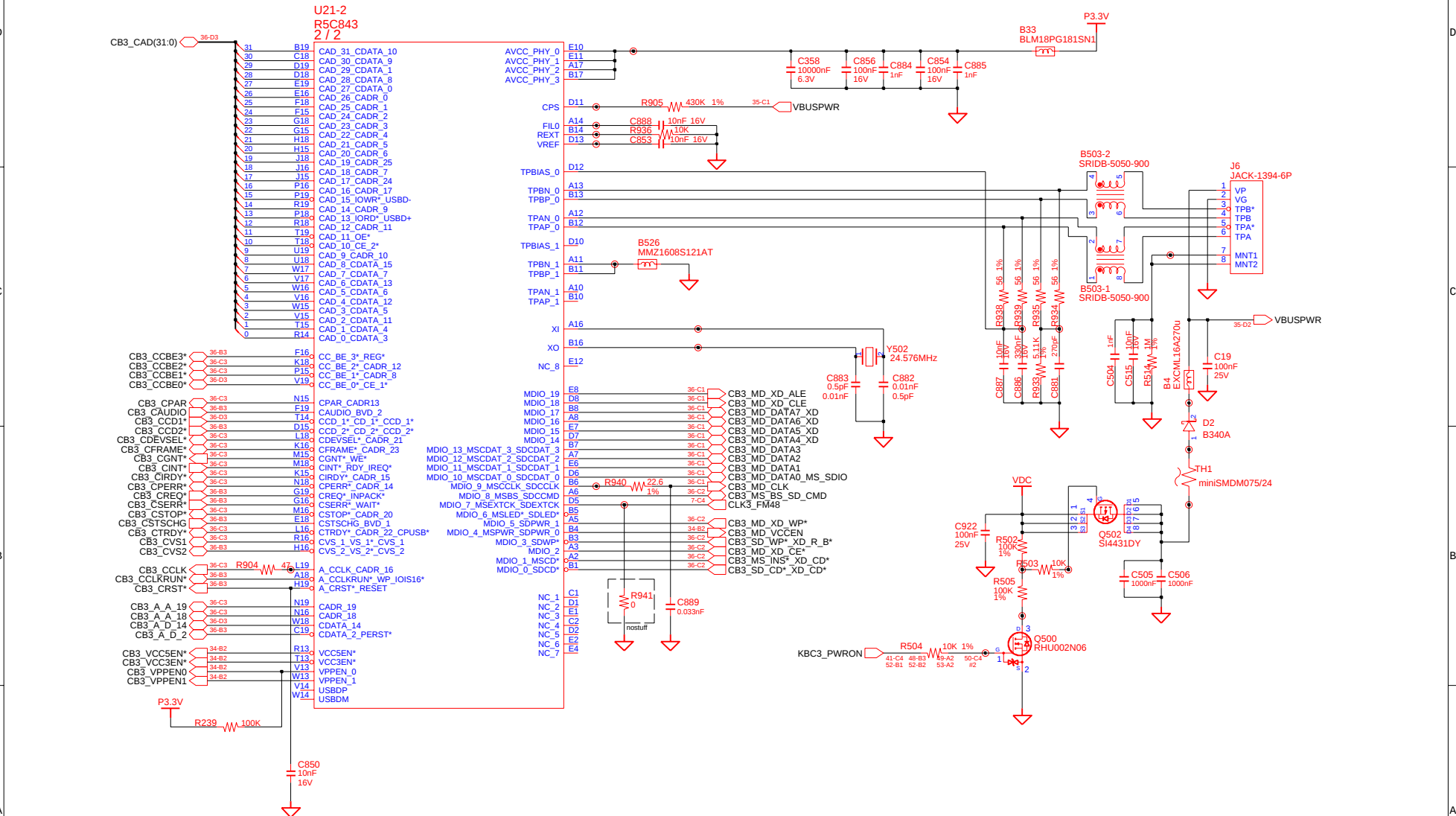
LCD CONNECTOR



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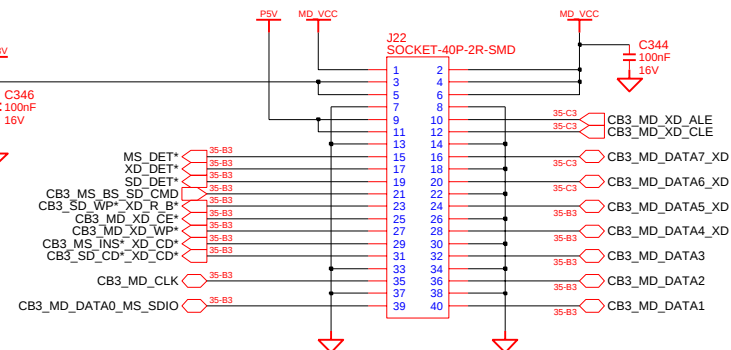
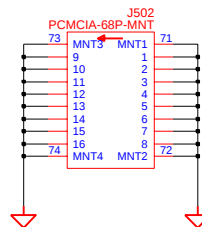
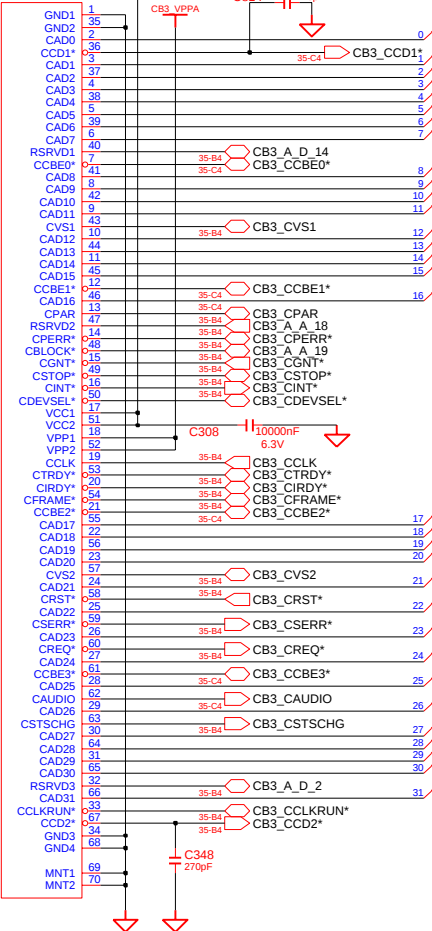
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CARDBUS(1/2)	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	33	OF 55



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR		MAIN	
APPROVAL	LIM, J.G	REV	1.0		CARDBUS(2/2)	
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	34	OF 55

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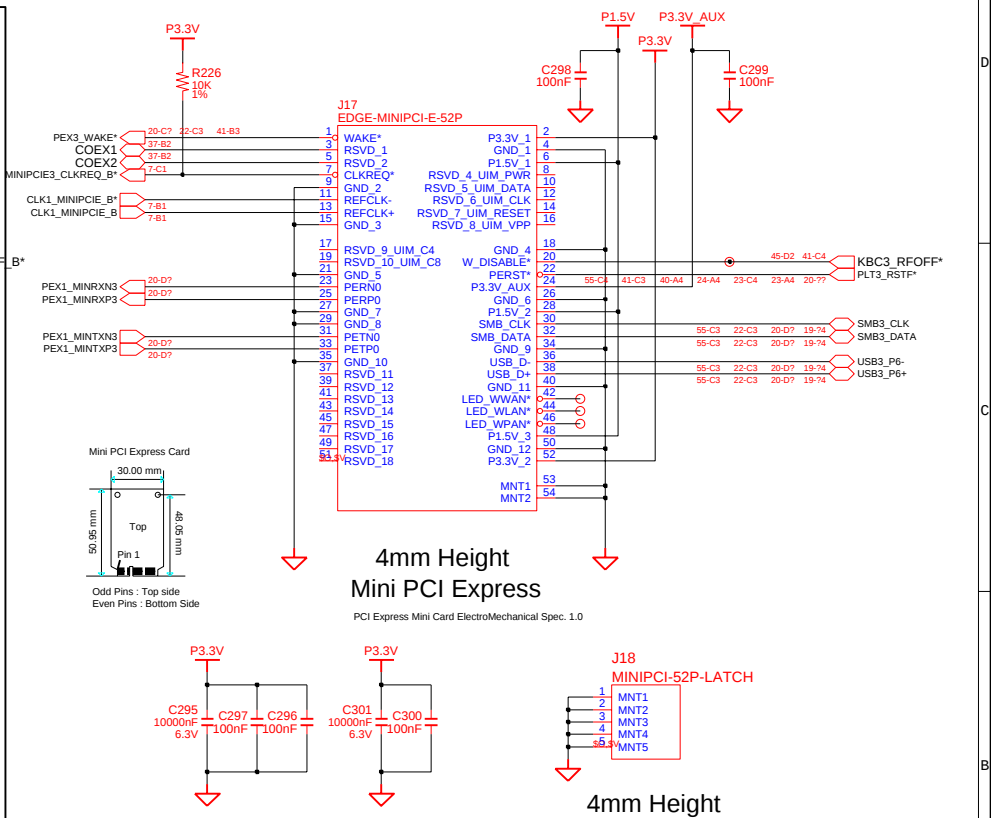
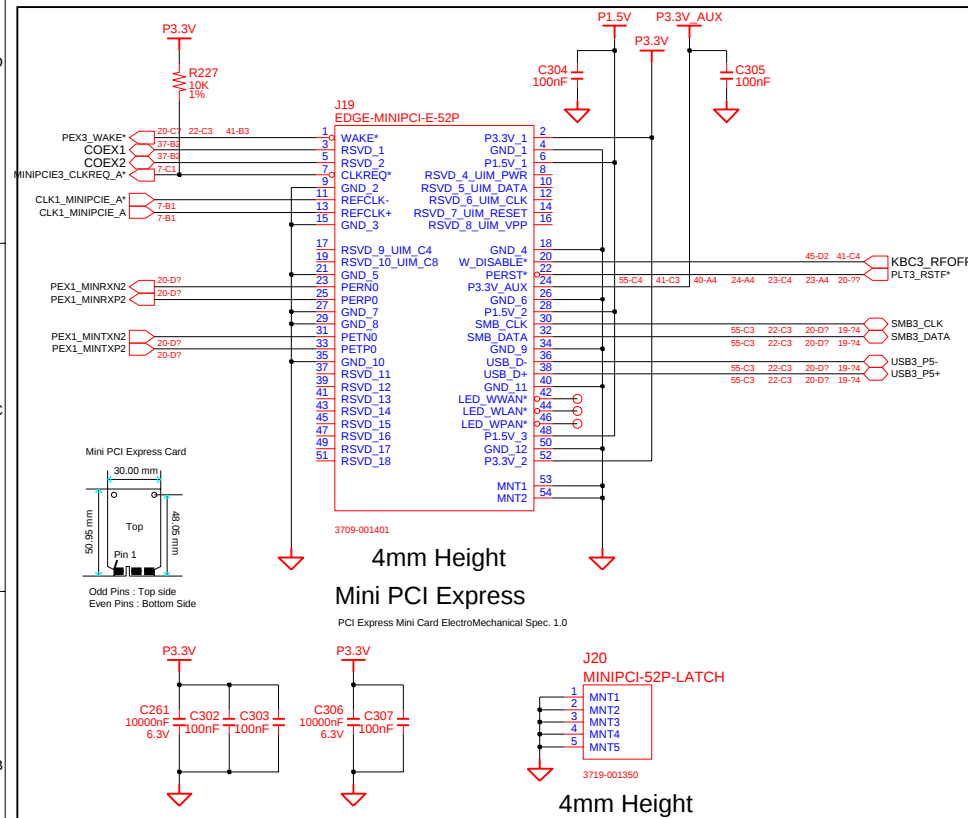
J501
PCMCIA-68P-REVERSE



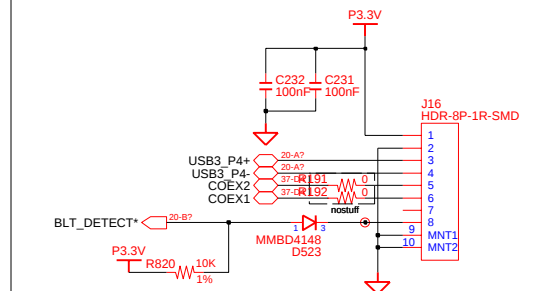
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CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0		CARDBUS CONN/MEDIA CARD	
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	35	OF 55

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nostuff

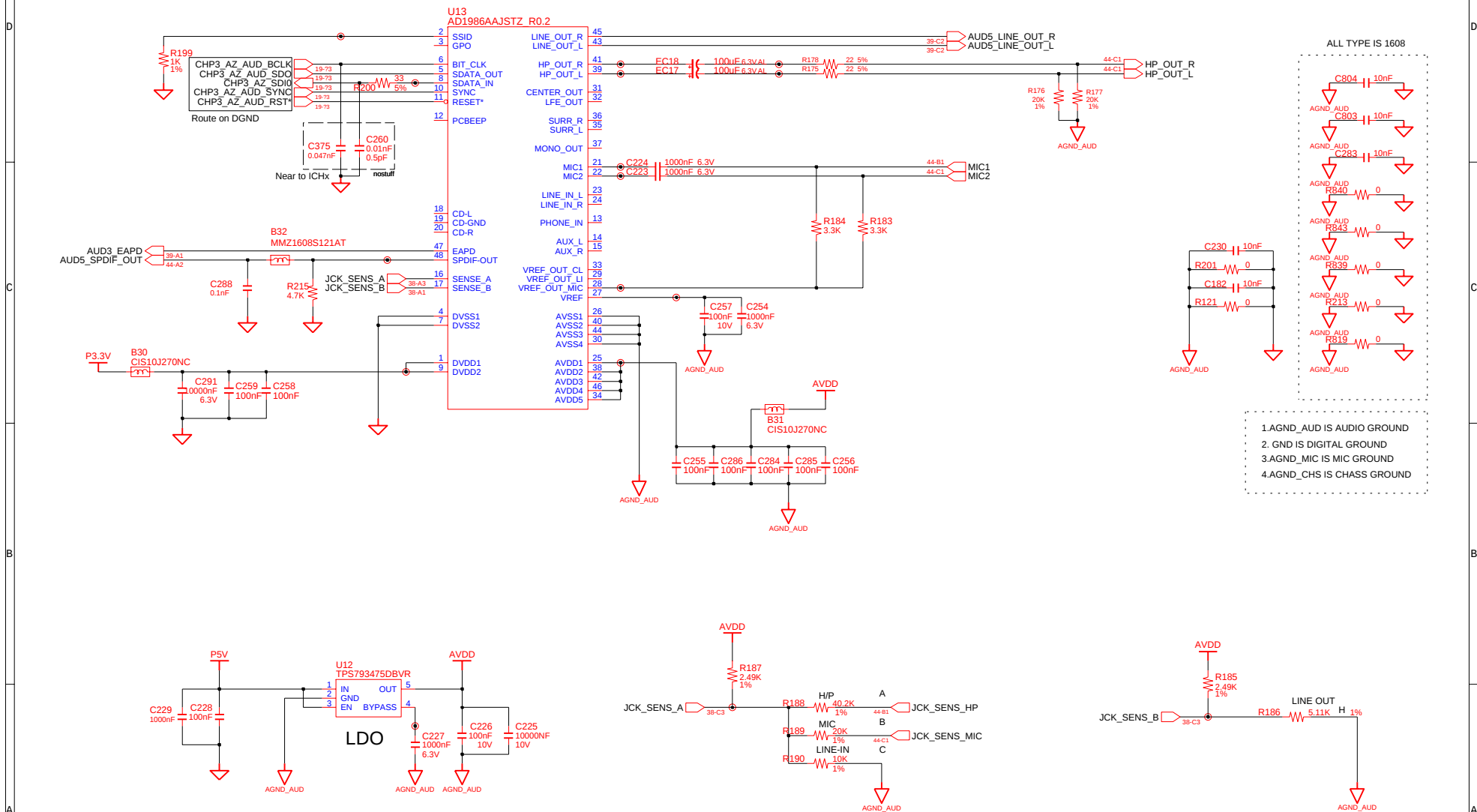


Bluetooth Interface



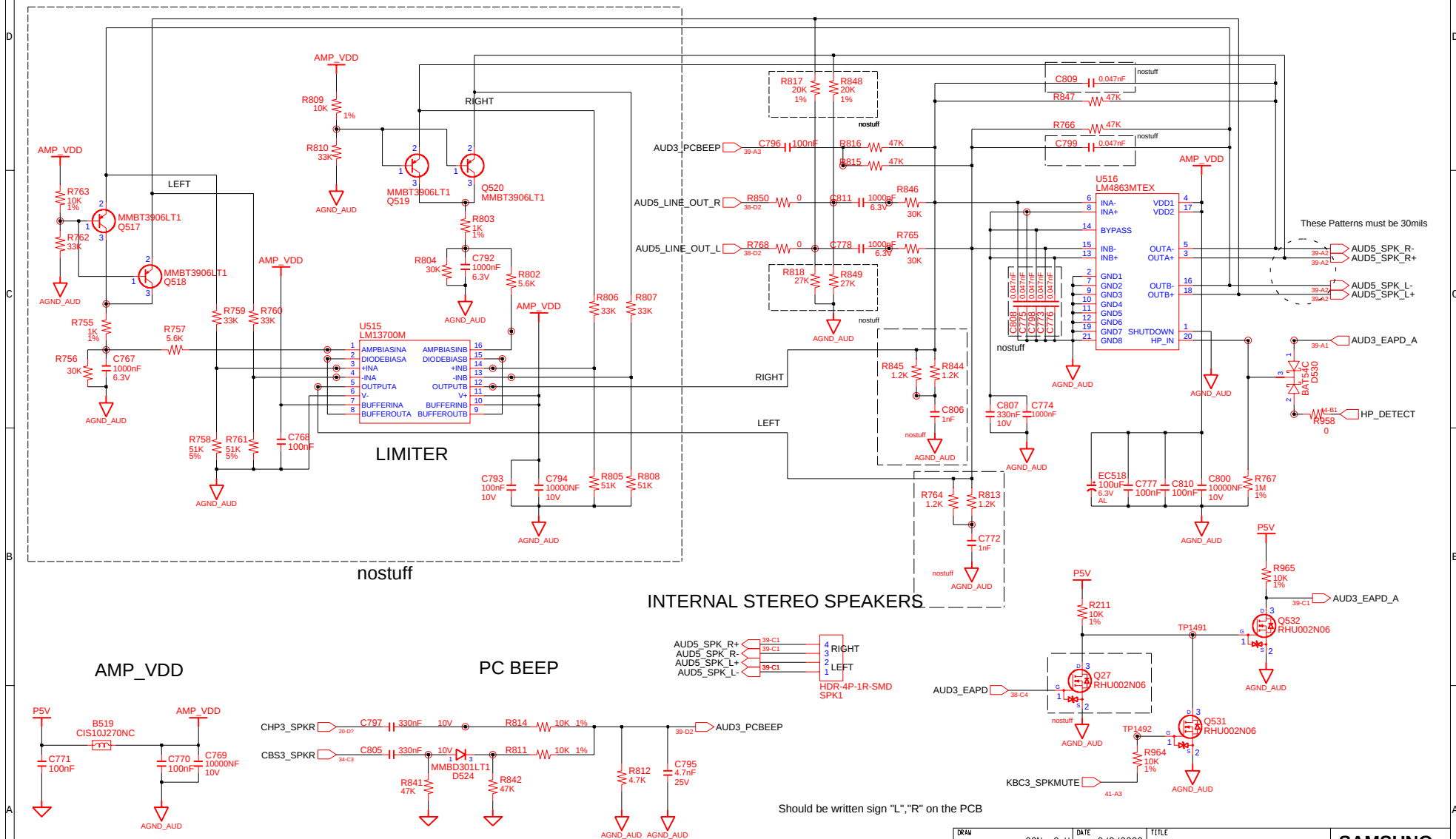
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN MINI CARD	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	36	OF 55

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DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN AUDIO CODEC	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	37 OF 55	

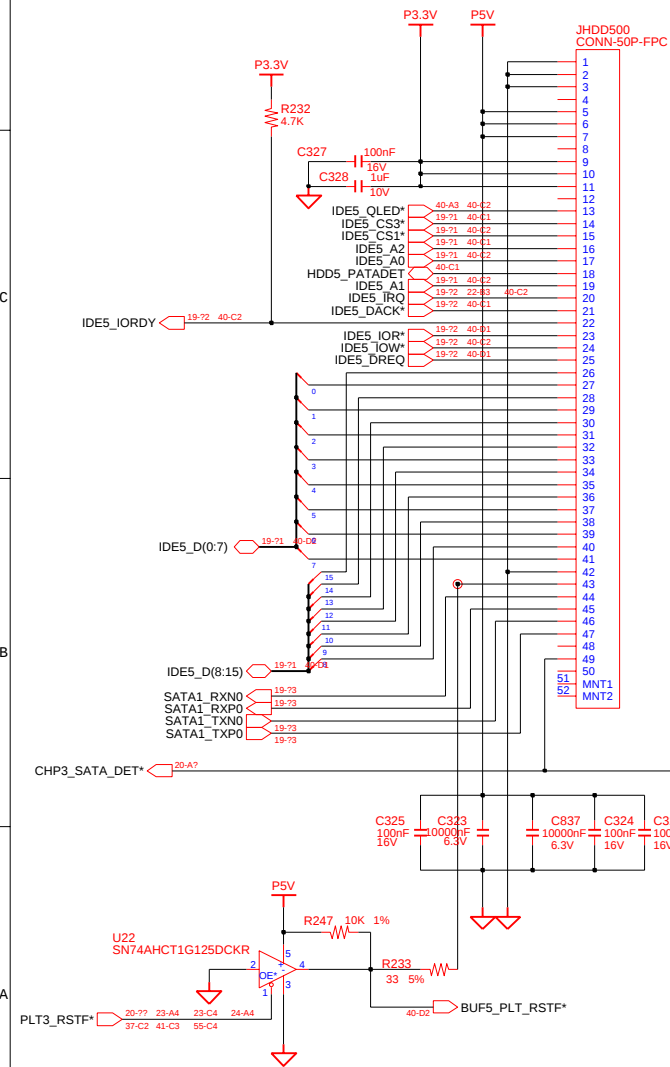
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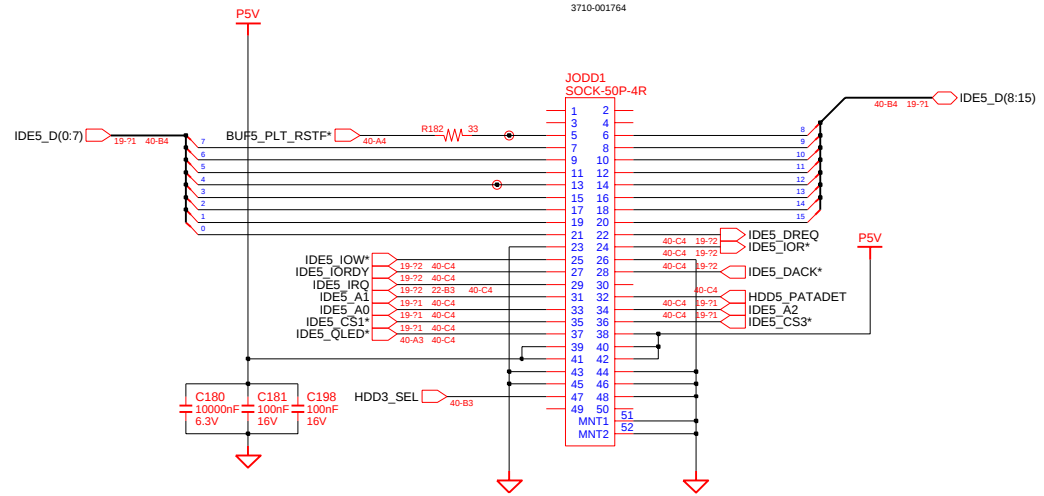
DRAM	SON, C. W.	DATE	3/9/2006	TITLE	FIRENZE-R MAIN AUDIO AMP	SAMSUNG ELECTRONICS		
CHECK	YUN, C. Y.	DEV. STEP	SR					
APPROVAL	LIM, J. G.	REV	1.0				PART NO.	BA41-xxxxxx
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM				PAGE	38 OF 55

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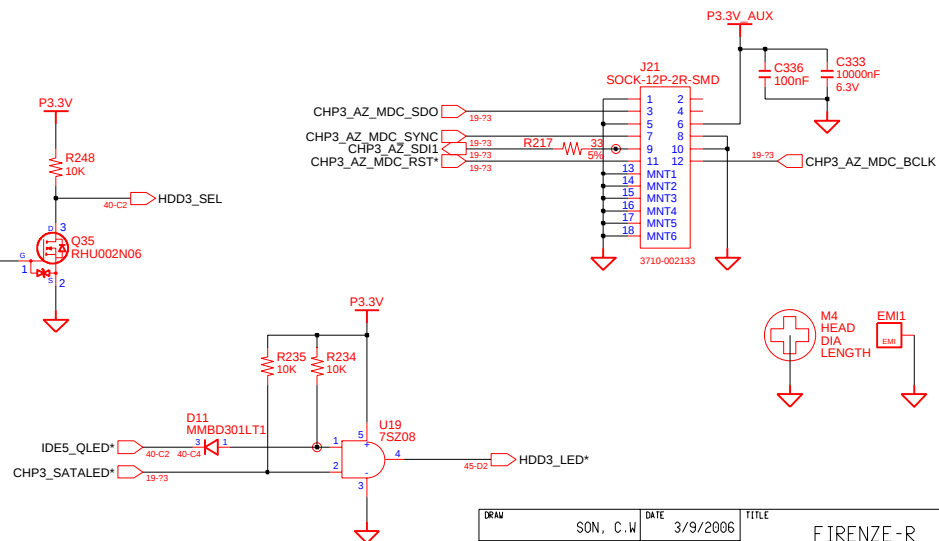
MAIN TO HDD



MAIN TO ODD

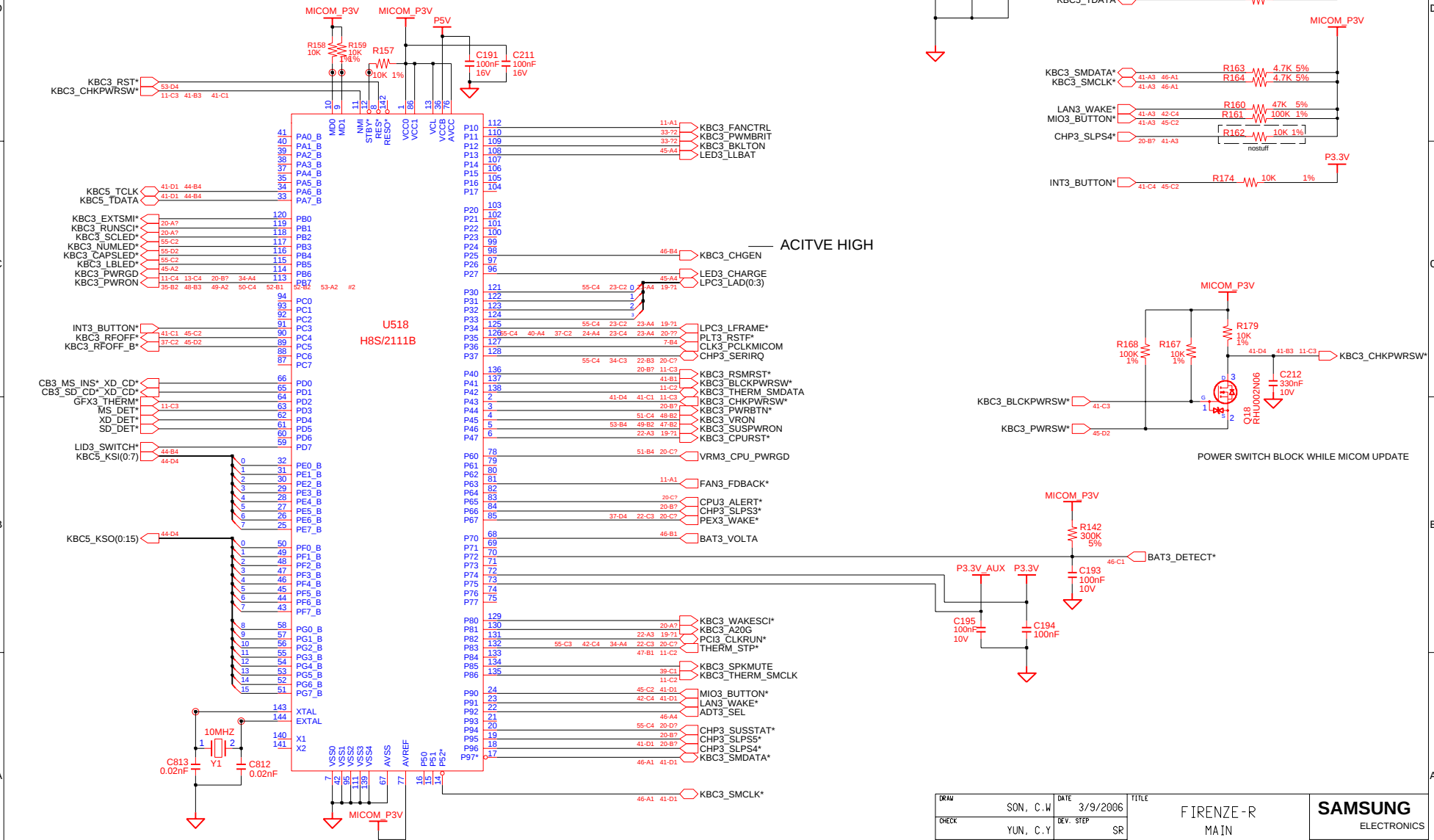


MDC Connector

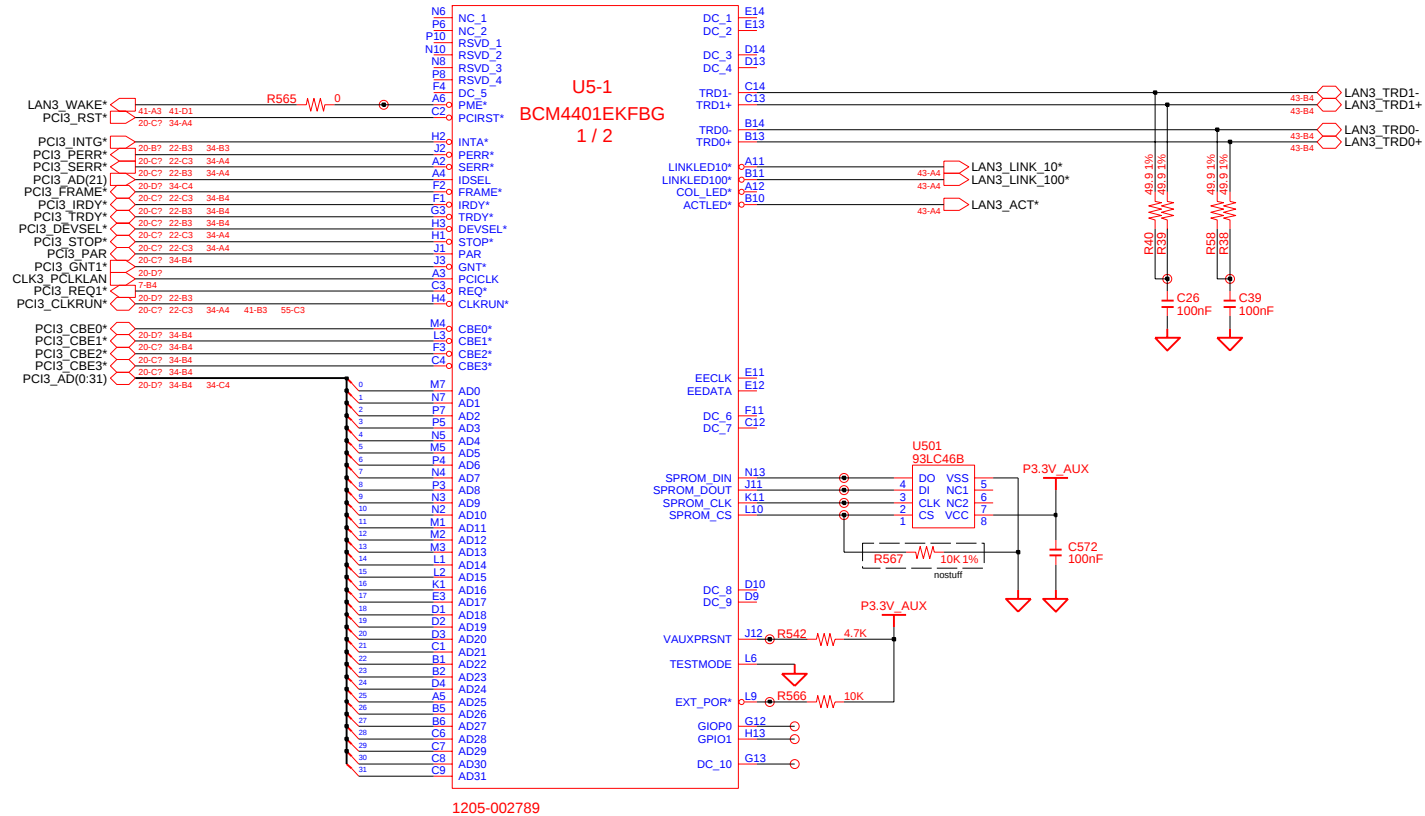


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN HDD/ODD/MDC CONN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	39	OF 55

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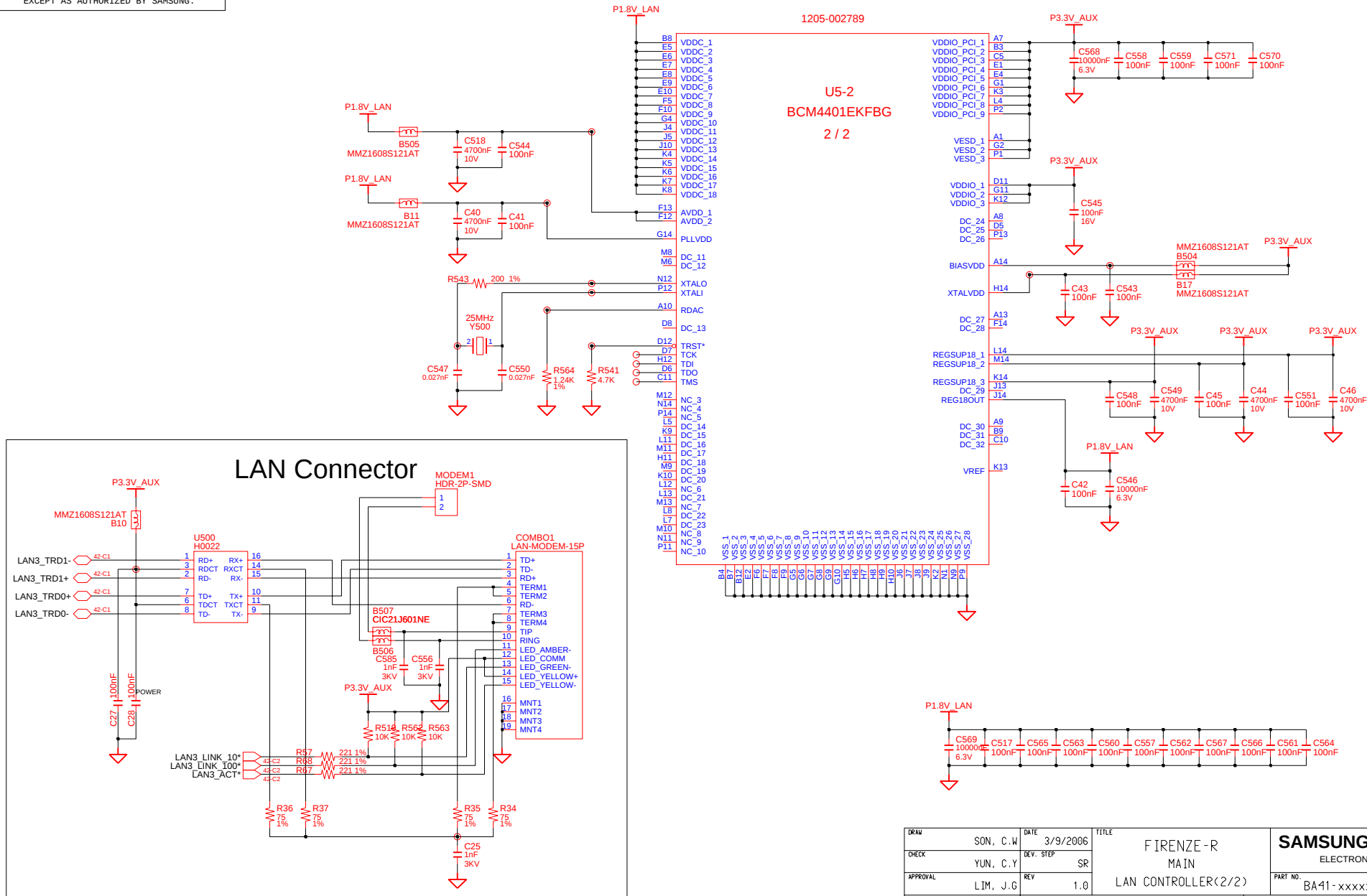
LAN Controller (Only 10/100M)



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN LAN CONTROLLER(1/2)	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	41	OF 55

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LAN Controller (Only 10/100M)



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN LAN CONTROLLER(2/2)	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	43	OF 56

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OPTICAL SPDIF OUTPUT & HEADPHONE

KEYBOARD

KBC5_KSI(0:7) 41-64

KBC5_KSO(0:15) 41-64

JKBD1 CONN-24P-FPC

MNT1 MNT2

TOUCH PAD

P5V

J13 SOCK-8P-1R-SMD

LED5_AMBER LED5_GREEN LID3_SWITCH* LB3_LED KBC5_TCLK KBC5_TDATA

PCB10J0603NR PCB10J0603NF

D52 D53

C179 100nF 16V C178 100nF 16V ZD500-1 SM05

MNT1 MNT2

SPDIF DETECT

P5V

AUD5_SPDIF_OUT 38-C4

JCK_SENS 44-C1

U8 NC7SZ125P5X

R145 1M 1%

C200 100nF

SPDIF BUFFER

P5V

AUD5_SPDIF 44-D1

JCK_SENS 44-C1

Q15 RHU002N06

HP_DETECT 39-C1

JCK_SENS_HP 38-A2

JACK-PHONE-9P-LED

P5V

J15 JACK-PHONE-9P-LED

VCC VIN GND RCH A_LCH GROUND SENSE MNT1 MNT2

B523 MMZ1608S121AT

R838 10K 1% B29 B524 B520

C791 100nF C802 0.1nF C790 0.1nF

AGND_AUD Connect to Mount-hole.

AUD5_SPDIF JCK_SENS

JACK-PHONE-6P-PINK

P5V

J14 JACK-PHONE-6P-PINK

TPS13 MMZ1608S121AT

R754 0 C789 0.1nF C766 0.1nF

AGND_AMGND_AUD Connect to Mount-hole.

JCK_SENS_MIC MIC2 MIC1

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OPTICAL SPDIF OUTPUT & HEADPHONE

KEYBOARD

KBC5_KSI(0:7) 41-64

KBC5_KSO(0:15) 41-64

JKBD1 CONN-24P-FPC

MNT1 MNT2

TOUCH PAD

P5V

J13 SOCK-8P-1R-SMD

LED5_AMBER LED5_GREEN LID3_SWITCH* LB3_LED KBC5_TCLK KBC5_TDATA

PCB10J0603NR PCB10J0603NF

D52 D53

C179 100nF 16V C178 100nF 16V ZD500-1 SM05

MNT1 MNT2

SPDIF DETECT

P5V

AUD5_SPDIF_OUT JCK_SENS

U8 NC7SZ125P5X

R145 1M 1%

C200 100nF

SPDIF BUFFER

P5V

AUD5_SPDIF JCK_SENS

Q14 RHU002N06 Q15 RHU002N06

R146 10K 1% R143 47K

HP_DETECT JCK_SENS_HP

DEFAULTL: HIGH JACK INSERT : LOW

AGND_AUD

JACK-PHONE-9P-LED

P5V

J15 JACK-PHONE-9P-LED

VCC VIN GND RCH A_LCH GROUND SENSE MNT1 MNT2

B523 B524 B520

MMZ1608S121AT

C802 0.1nF C790 0.1nF C199 0.1nF

AGND_AUD

Connect to Mount-hole.

JACK-PHONE-6P-PINK

P5V

J14 JACK-PHONE-6P-PINK

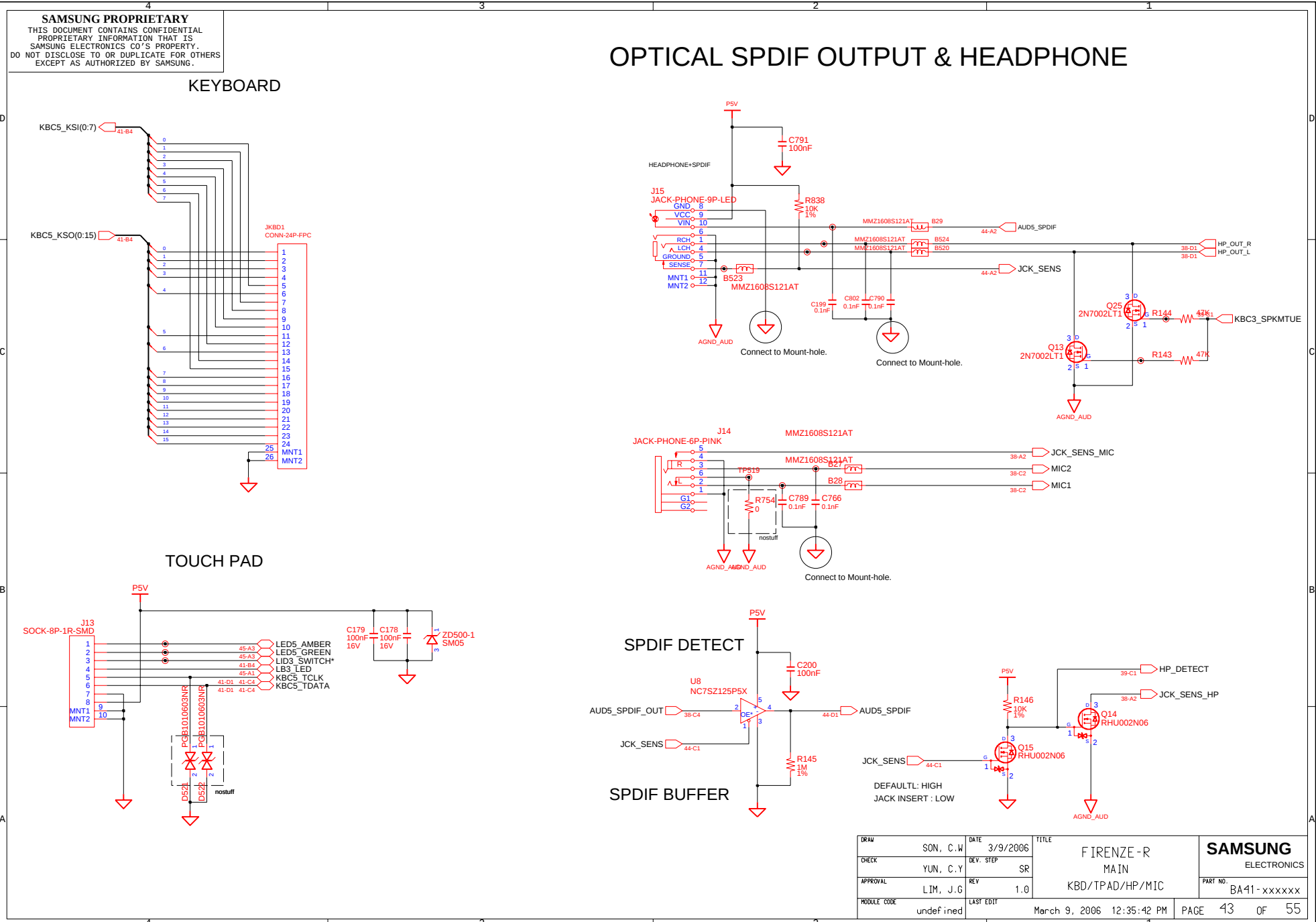
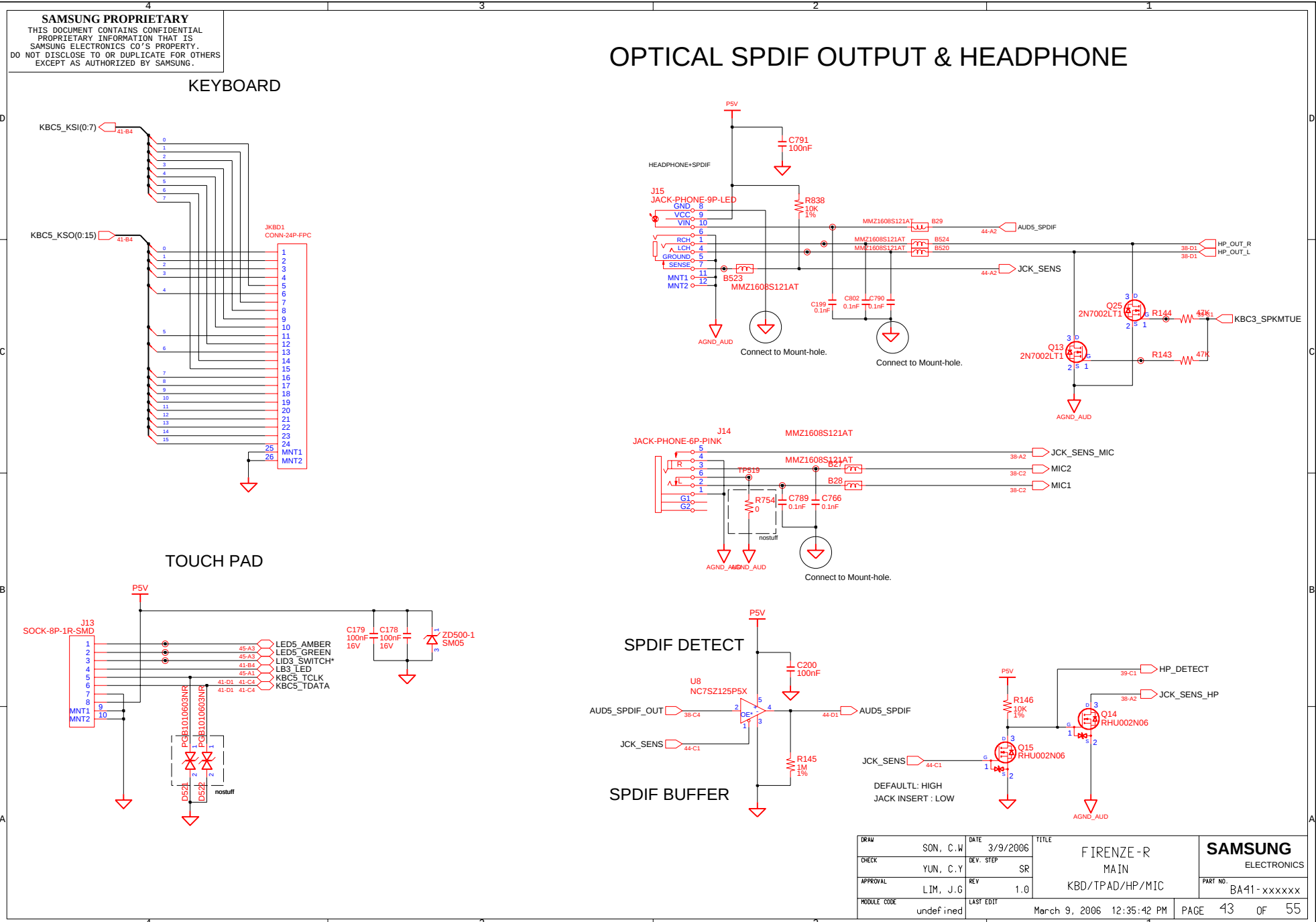
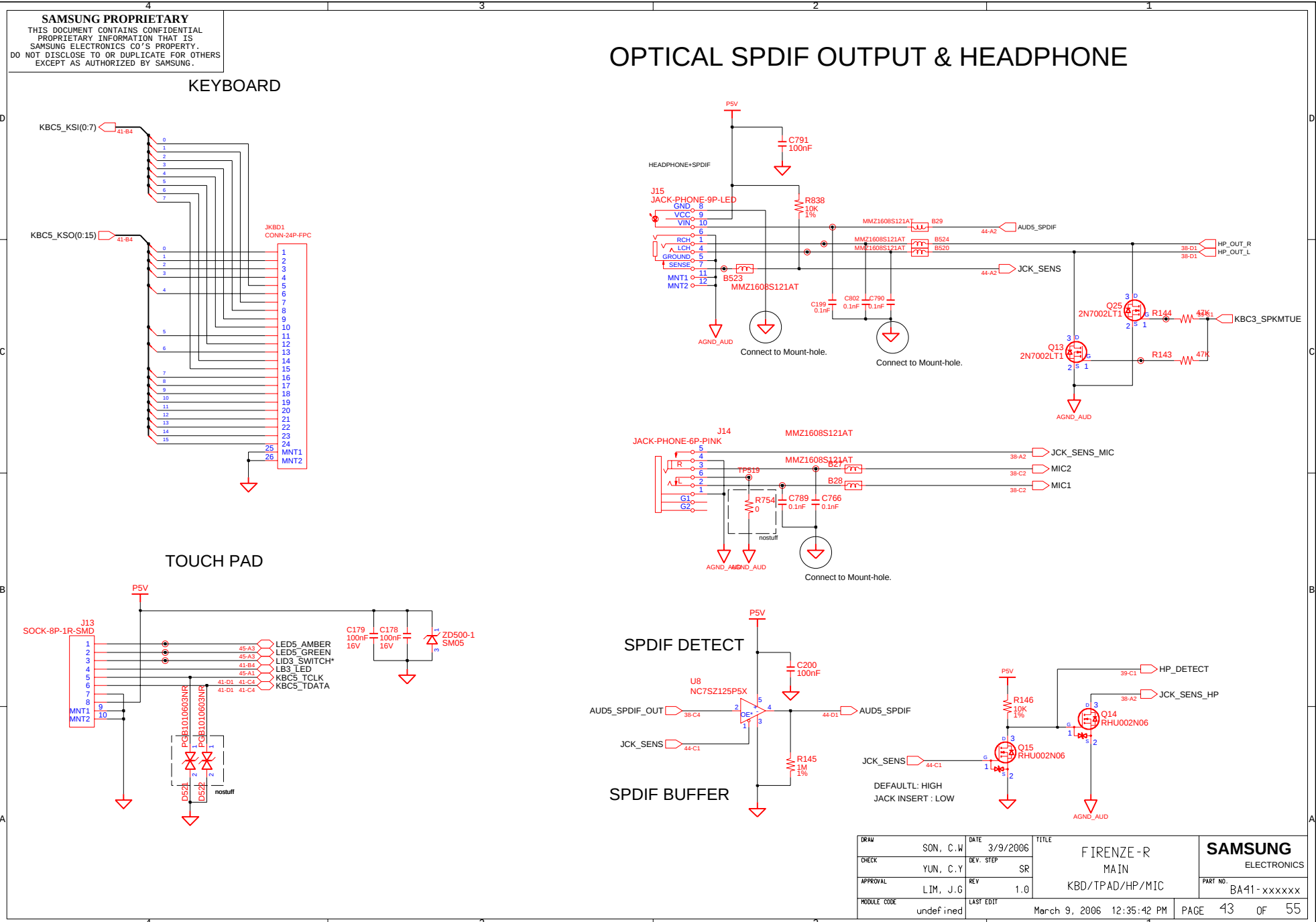
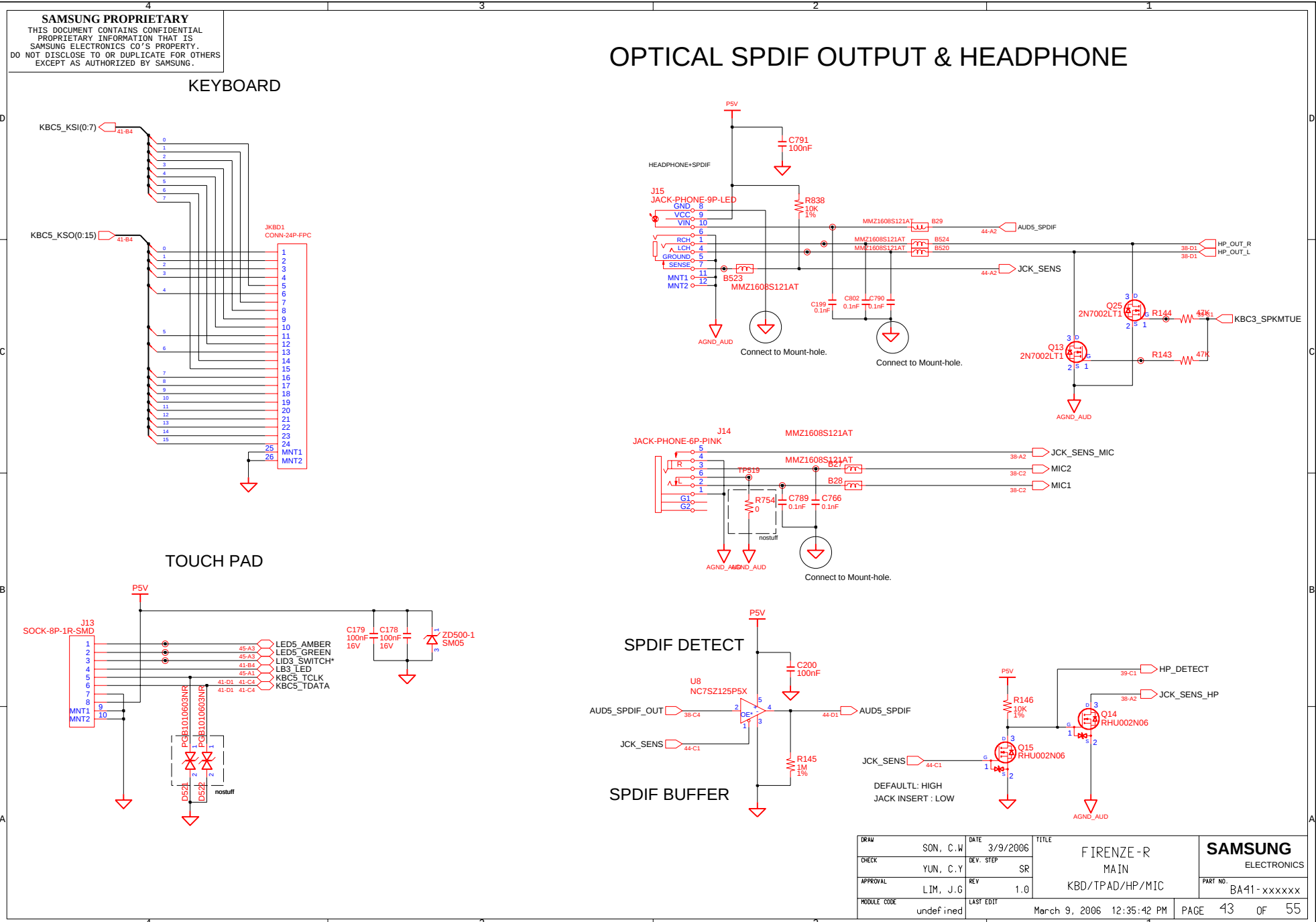
TPS13 MMZ1608S121AT

B27 B28

C789 0.1nF C766 0.1nF

AGND_AUD

Connect to Mount-hole.

[illegible][illegible][illegible]

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KEYBOARD

KBC5_KSI(0:7)

KBC5_KSO(0:15)

JKB01
CONN-24P-FPC

TOUCH PAD

J13
SOCK-8P-1R-SMD

MNT1
MNT2

LED5_AMBER
LED5_GREEN
LID3_SWITCH*
LB3_LED
KBC5_TCLK
KBC5_TDATA

P5V

C179 100nF 16V
C178 100nF 16V

ZD500-1
SM05

D52
D53

nostuff

OPTICAL SPDIF OUTPUT & HEADPHONE

PSV

C791 100nF

R838 10K 1%

J15 JACK-PHONE-9P-LED

VCC 9
VIN 10
GND 8
RCH 1
A_LCH 4
GROUND 5
SENSE 7
MNT1 11
MNT2 12

B523

MMZ1608S121AT

AGND_AUD

Connect to Mount-hole.

C802 0.1nF
C790 0.1nF

MMZ1608S121AT

B29

B524

B520

AUD5_SPDIF

JCK_SENS

HP_OUT_R
HP_OUT_L

Q25 2N7002LT1

Q13 2N7002LT1

R144 47K

R143 47K

KBC3_SPKMTUE

AGND_AUD

J14 JACK-PHONE-6P-PINK

TP513

MMZ1608S121AT

B27

B28

AGND_AMERG_AUD

JCK_SENS_MIC

MIC2

MIC1

Connect to Mount-hole.

SPDIF DETECT

U8 NC7SZ125P5X

C200 100nF

R145 1M 1%

AUD5_SPDIF_OUT

JCK_SENS

AUD5_SPDIF

SPDIF BUFFER

P5V

R146 10K 1%

Q14 RHU002N06

Q15 RHU002N06

JCK_SENS

HP_DETECT

JCK_SENS_HP

AGND_AUD

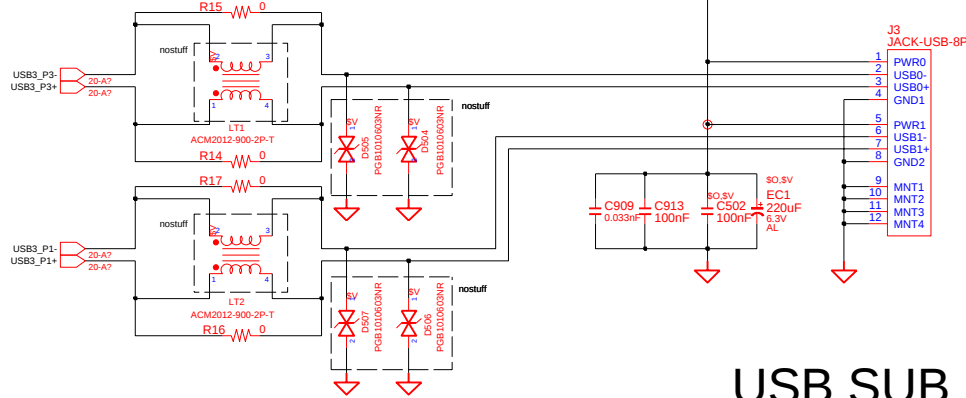
DEFAULTL: HIGH
JACK INSERT : LOW

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R
CHECK	YUN, C.Y	DEV. STEP	SR	MAIN	
APPROVAL	LIM, J.G	REV	1.0	KBD/TPAD/HP/MIC	
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	43 OF 55

SAMSUNG
ELECTRONICS
PART NO.: BA41-xxxxxx

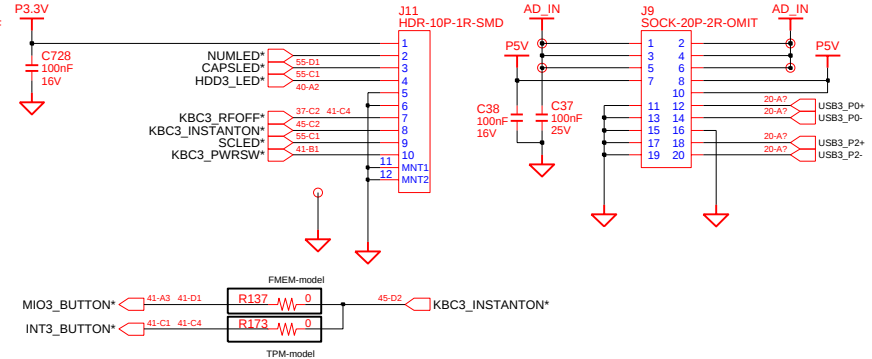
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USB PORT

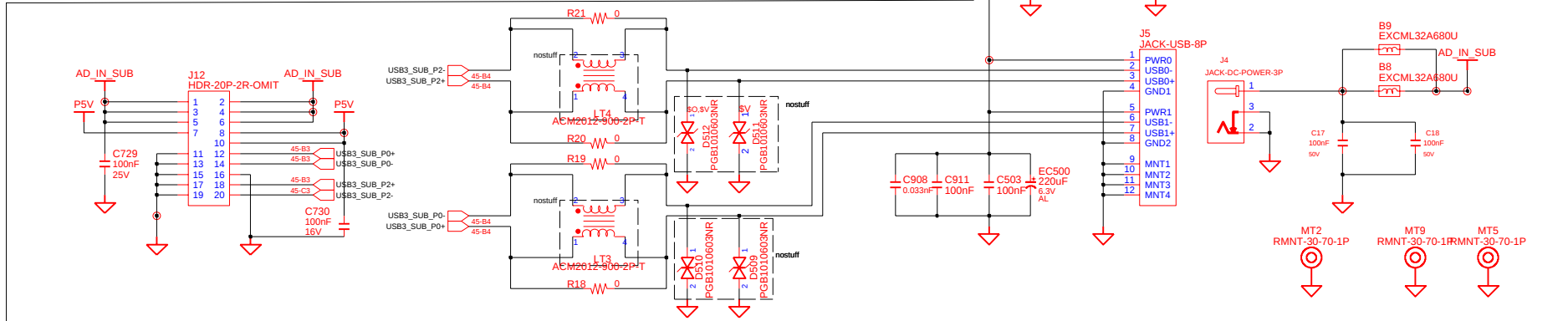


MAIN TO ON-TOP

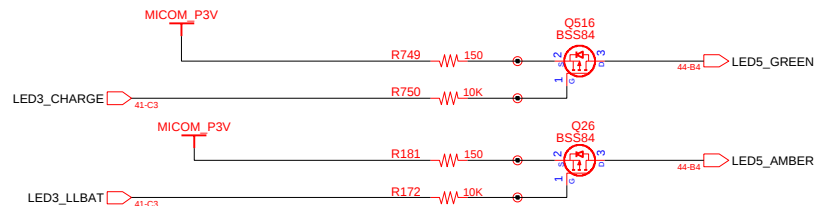
MAIN TO USB



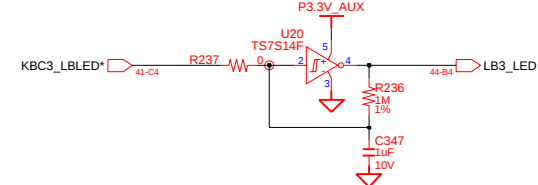
USB SUB B'D



ADAPTER IN / CHARGER LED



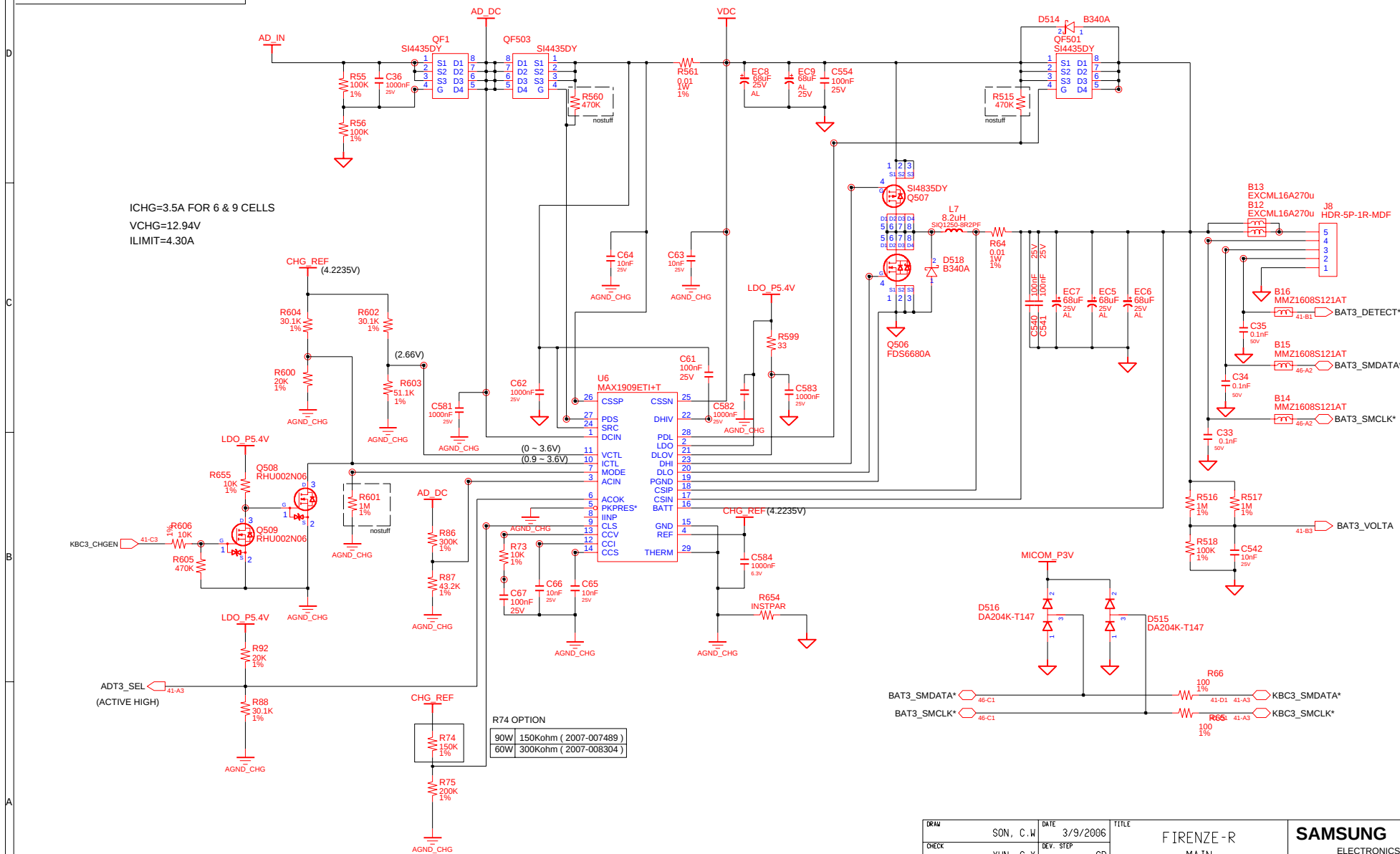
POWER ON / LB LED



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN USB PORT/LED/ON-TOP	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	44	OF 55

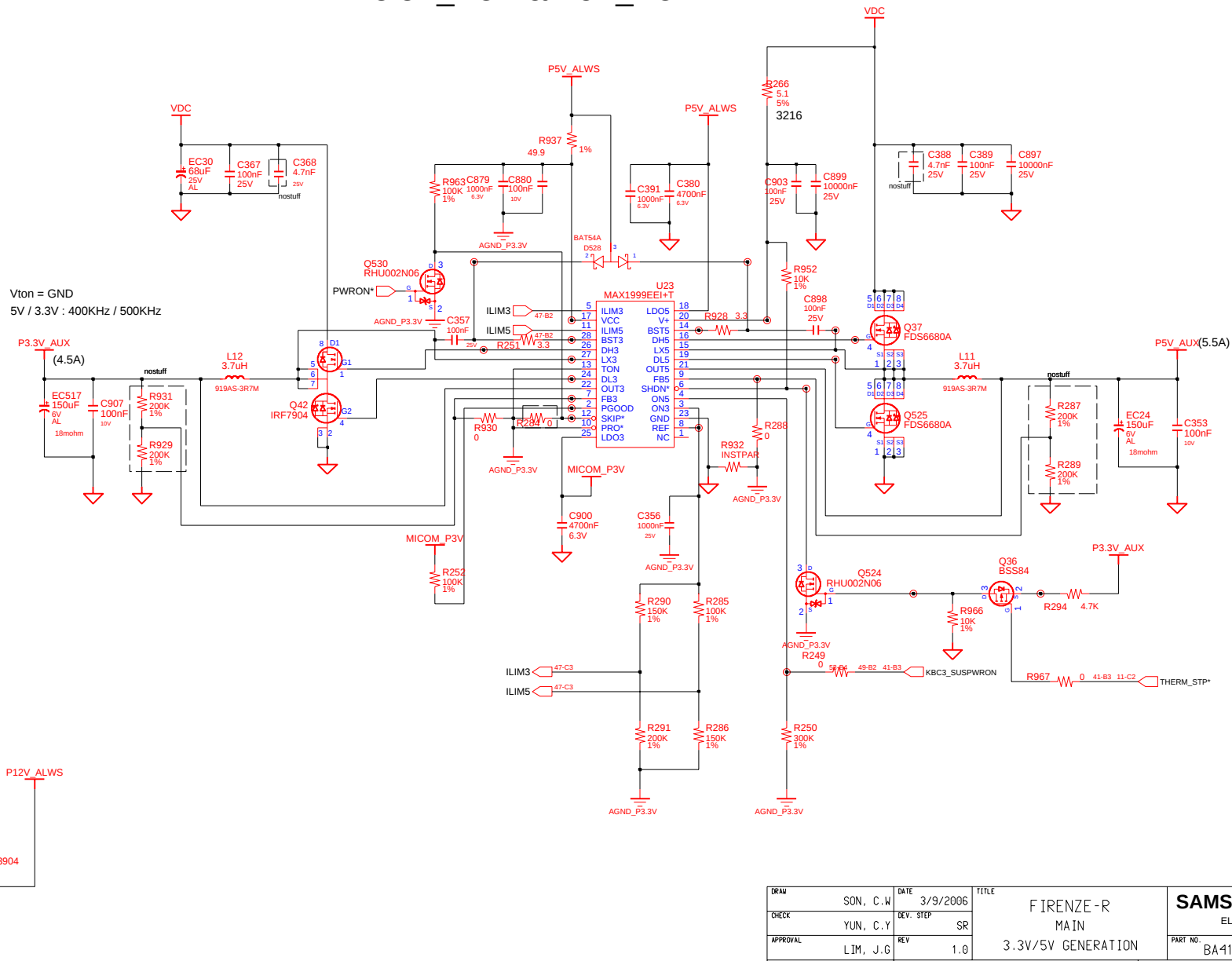
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CHARGER & POWER MANAGEMENT



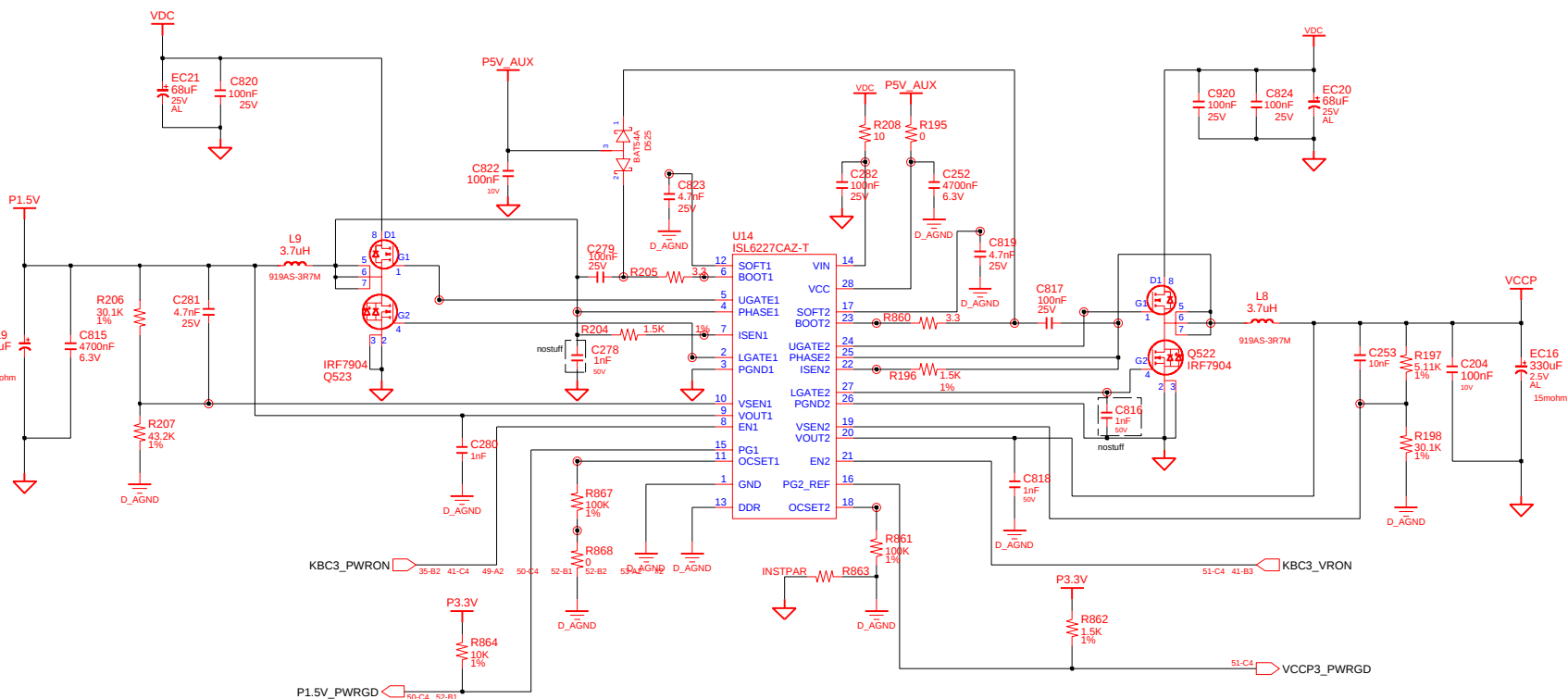
DRAW	SON, C.W	DATE	3/9/2006	FIRENZE-R MAIN CHARGER		SAMSUNG ELECTRONICS	
CHECK	YUN, C.Y	DEV. STEP	SR				
APPROVAL	LIM, J.G	REV	1.0				
MODULE CODE		LAST EDIT		March 9, 2006 12:35:42 PM	PAGE	45	OF 55

P3.3V_AUX & P5V_AUX



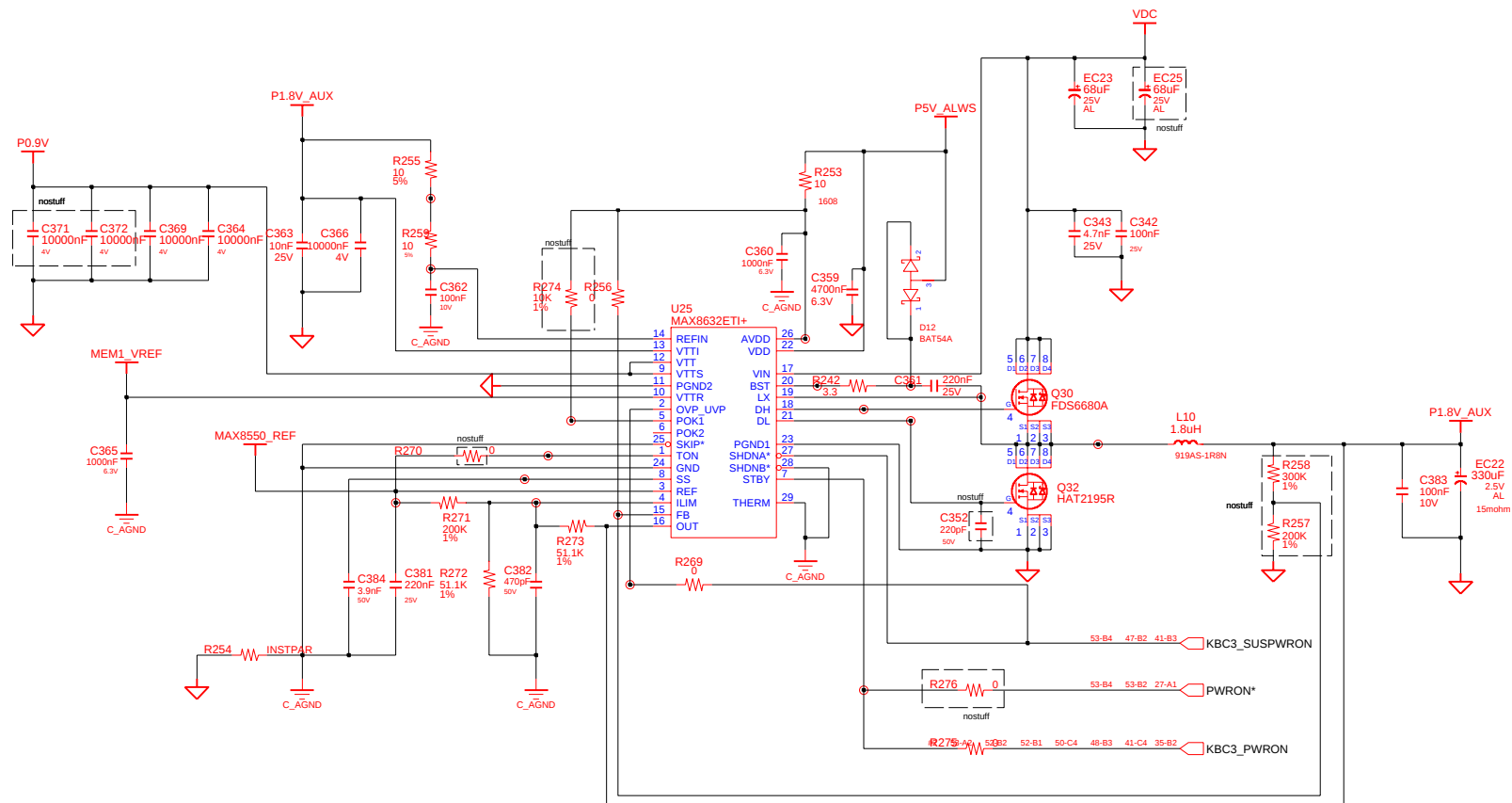
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN 3.3V/5V GENERATION	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	46	OF 55

P1.5V & VCCP (1.05V)



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN 1.5V_AUX/VTT	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	47 OF 55	

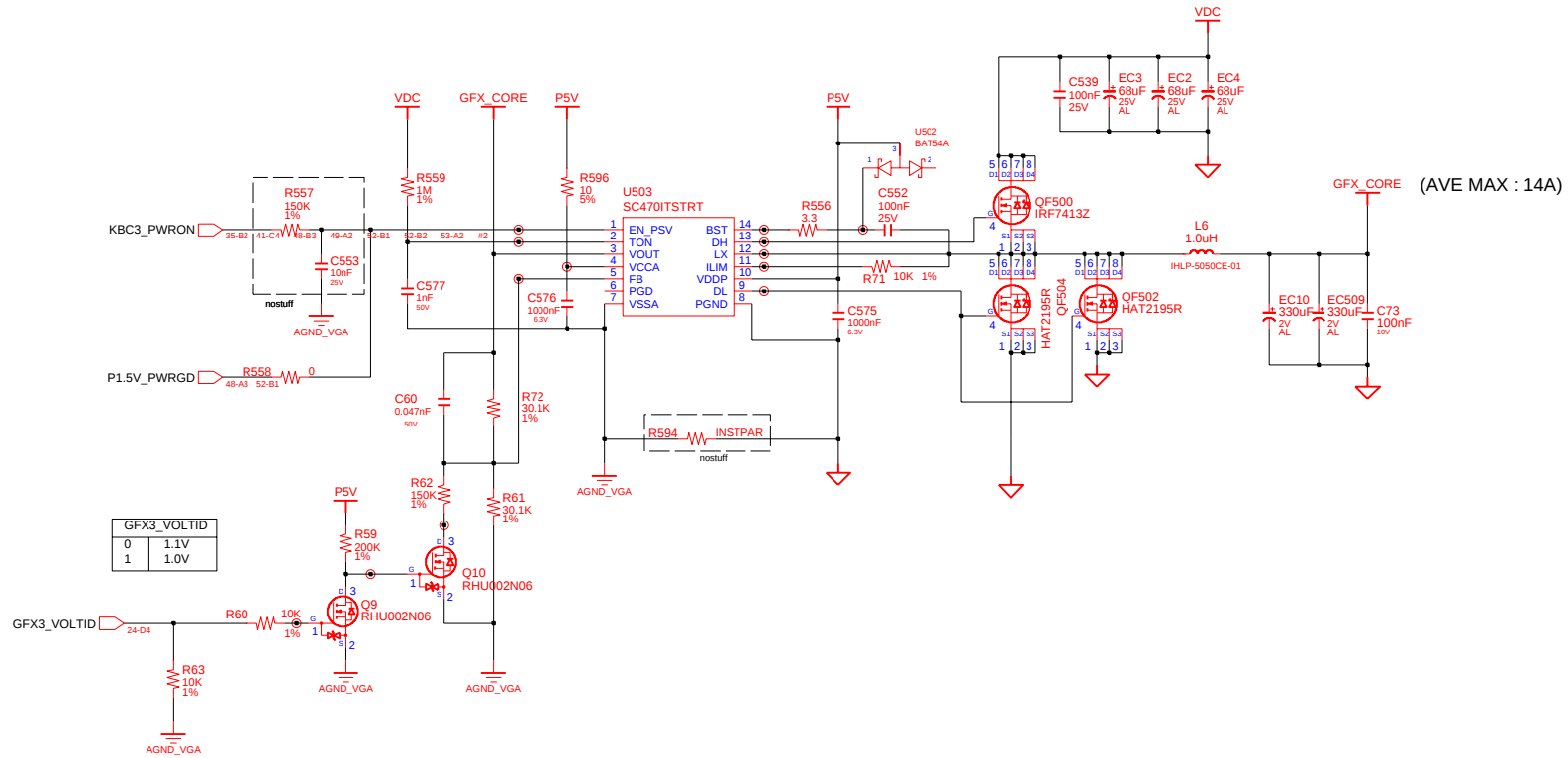
DDR2 Power



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN DDR2 POWER	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	48	OF 55

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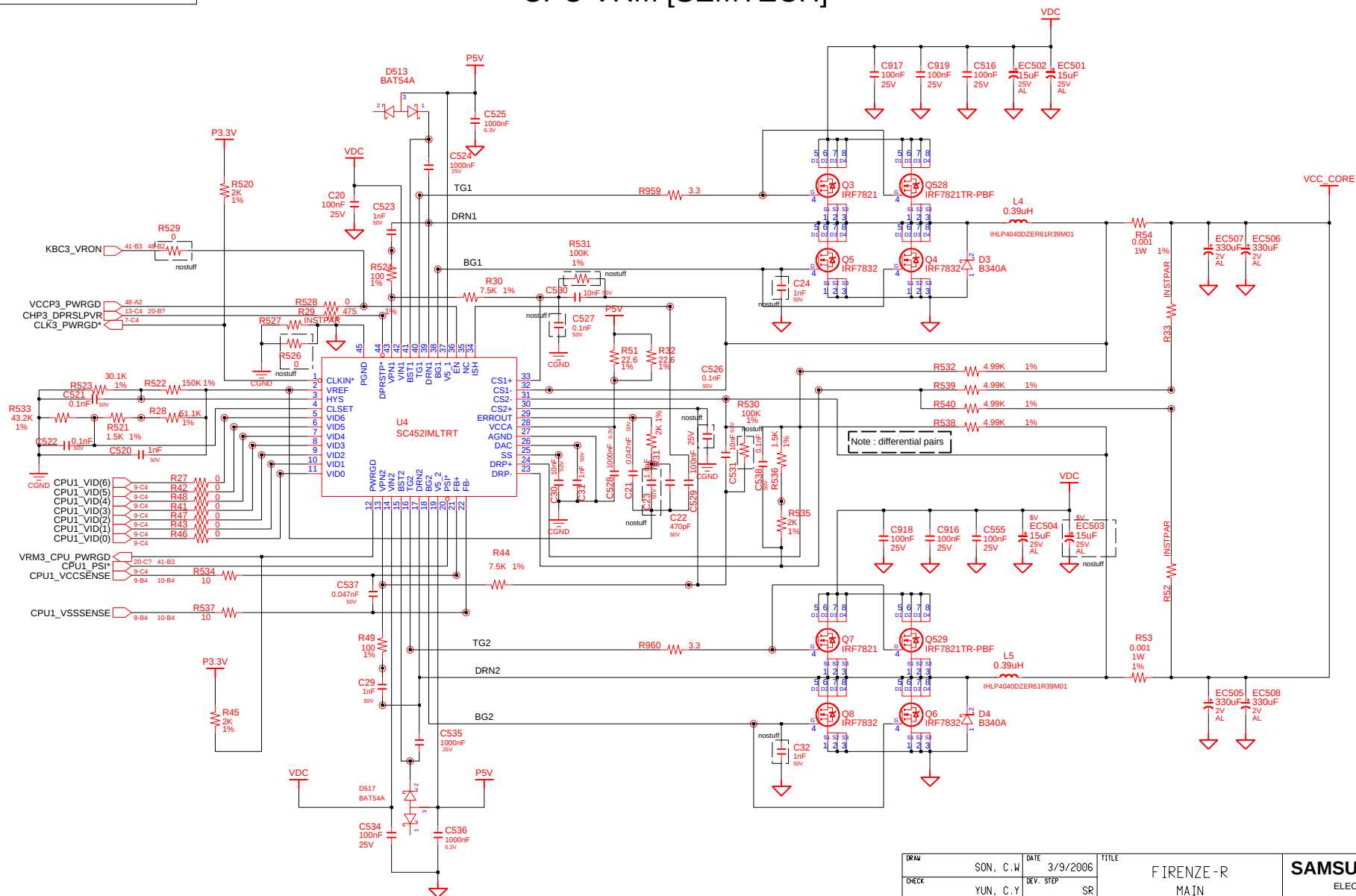
Graphic Core Power



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN GRAPHIC CORE POWER	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	49	OF 55

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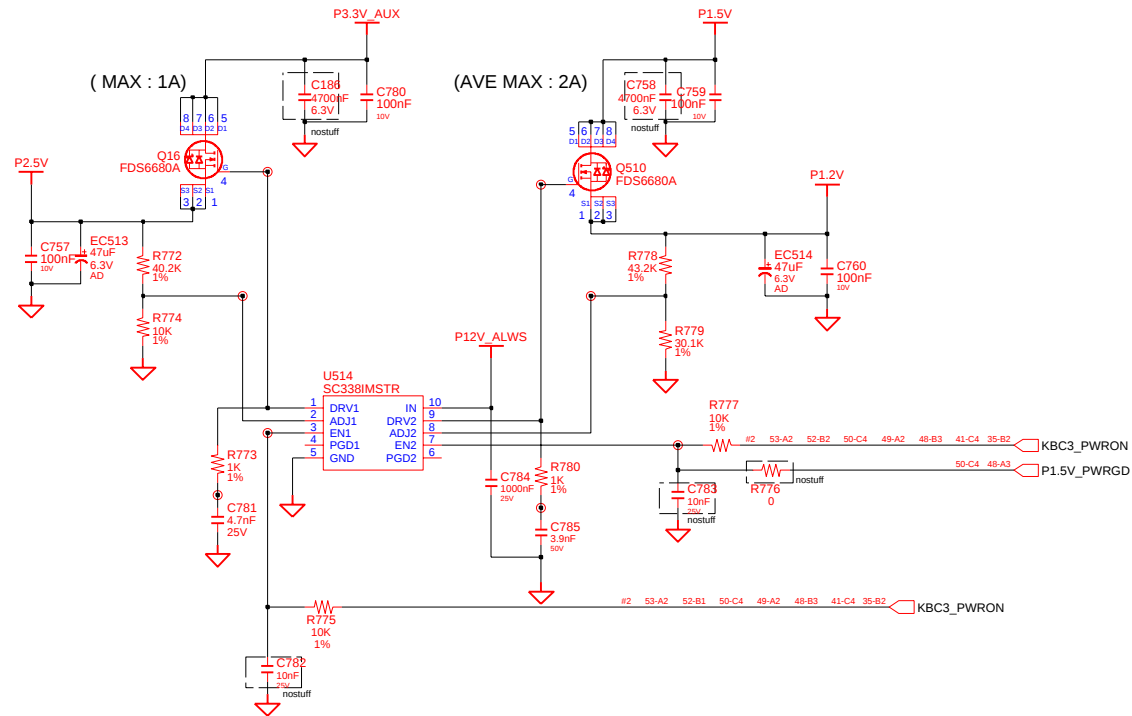
CPU VRM [SEMTECH]



DRAW	SON, C.W.	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CPU POWER	SAMSUNG ELECTRONICS	
CHECK	YUN, C.Y.	DEV. STEP	SR				
APPROVAL	LIM, J.G.	REV	1.0				
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM				PAGE
				PART NO.	BA41-xxxxxx		

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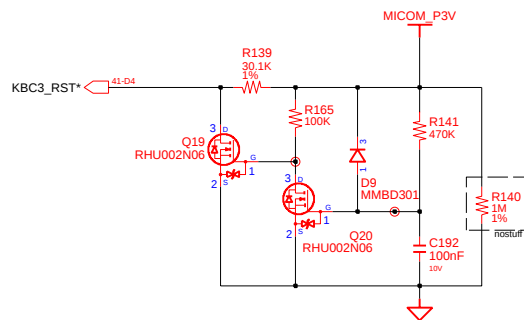
P1.2V / P2.5V POWER



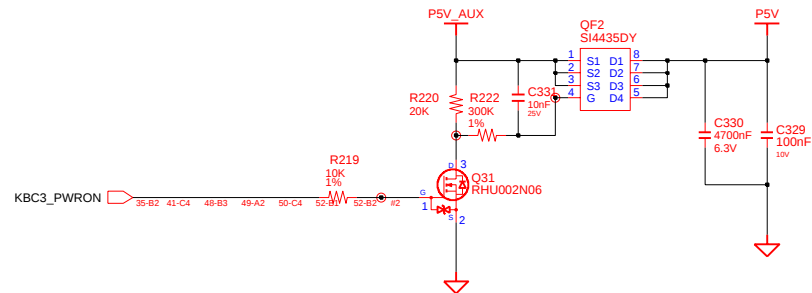
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN 1.2V/2.5V POWER	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	51 OF 55	

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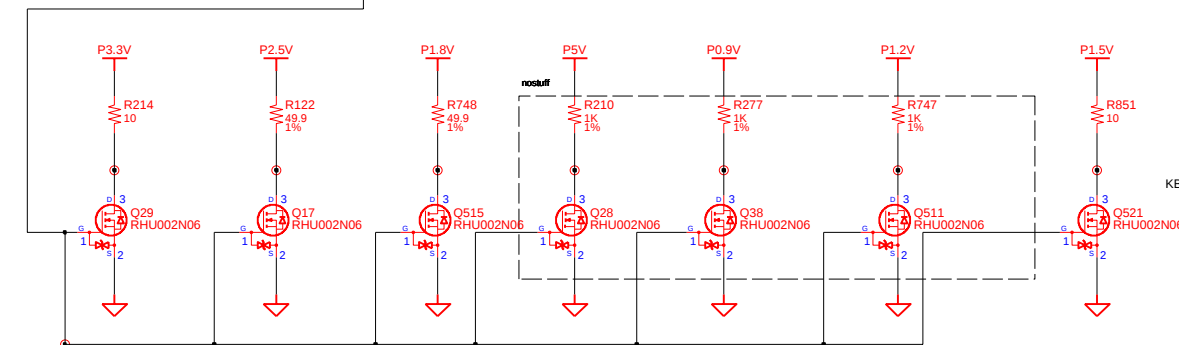
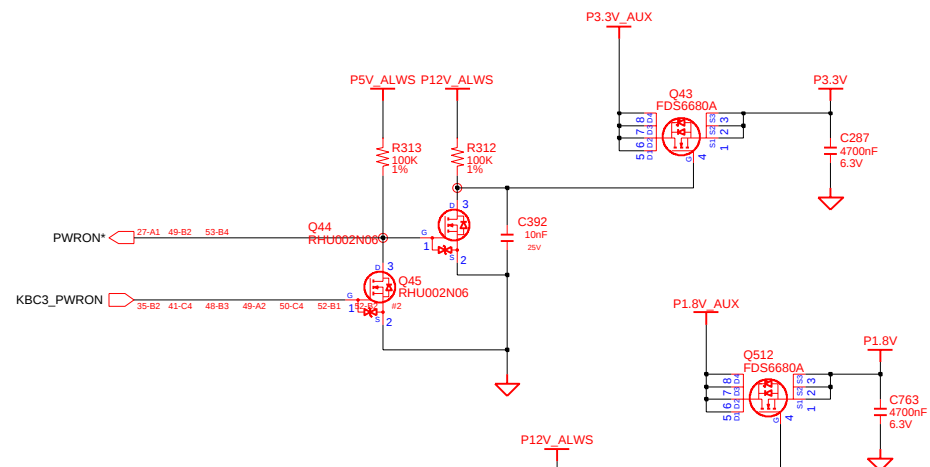
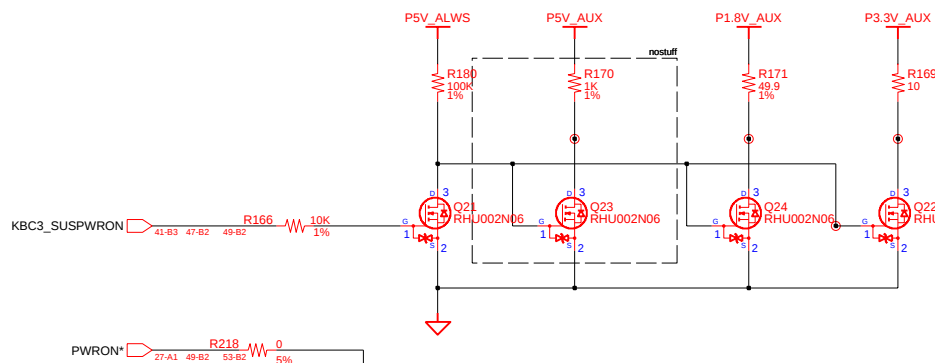
MICOM RESET



Switched Power On (P5V)



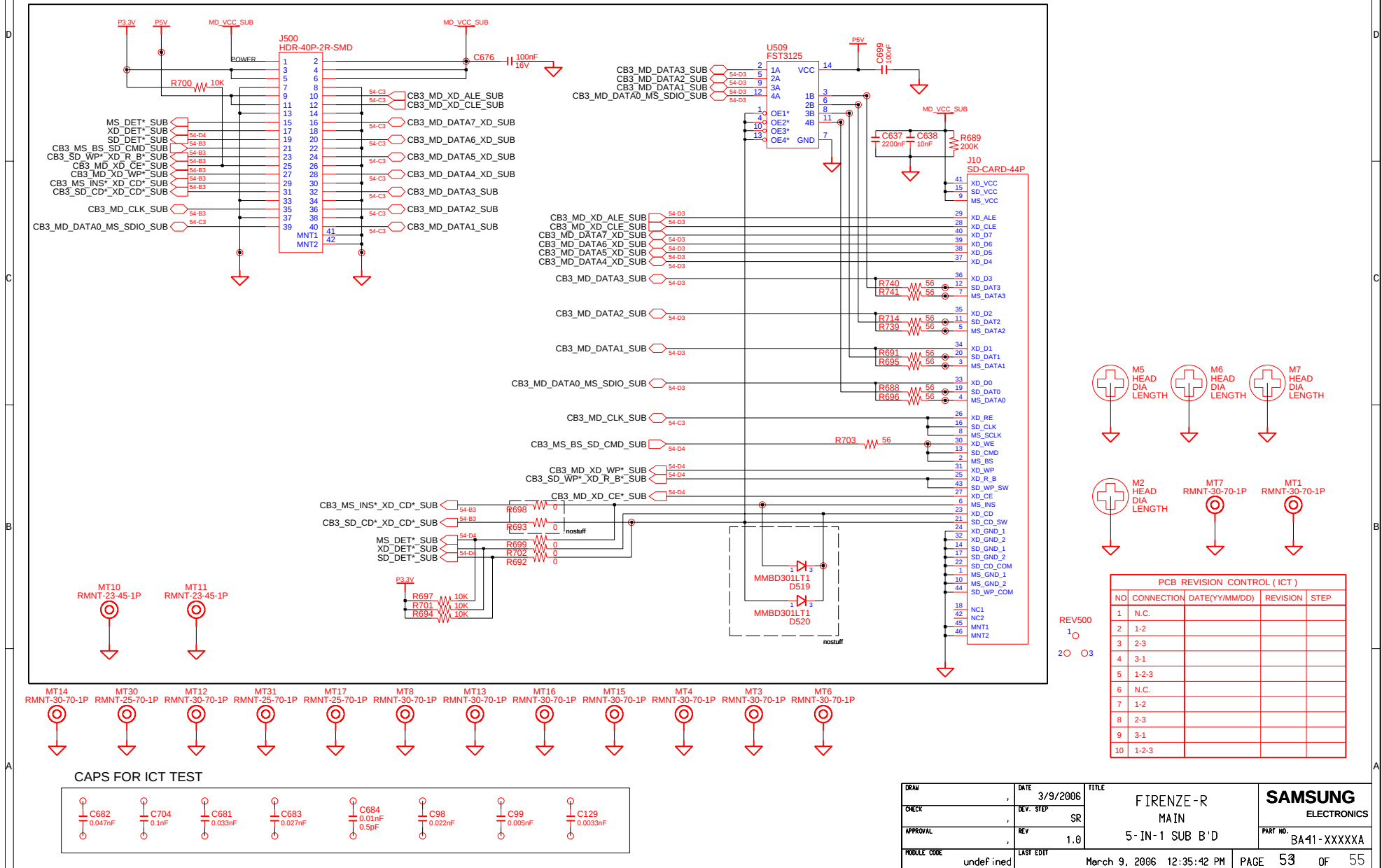
Switched Power On (P3.3V & 1.8V)



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN MICOM&SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	52	OF 55

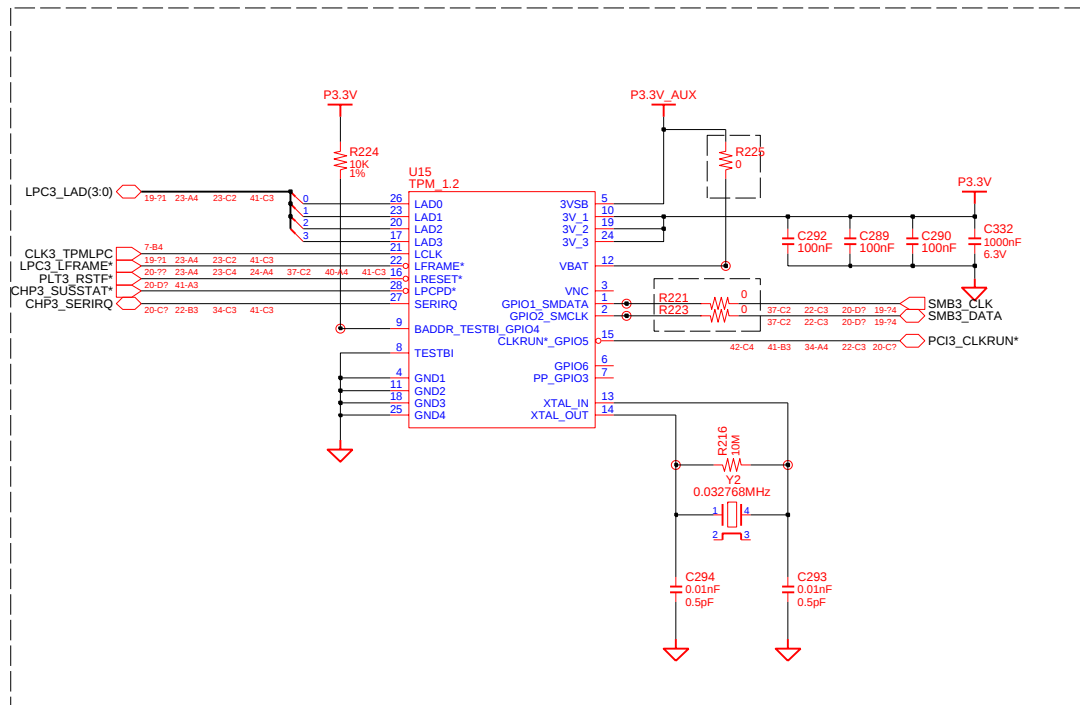
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5-IN-1 SUB B'D

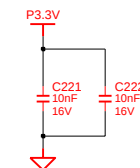
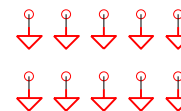
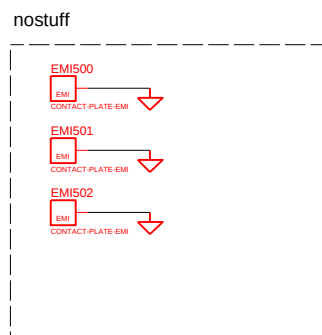
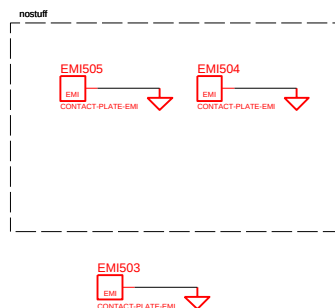
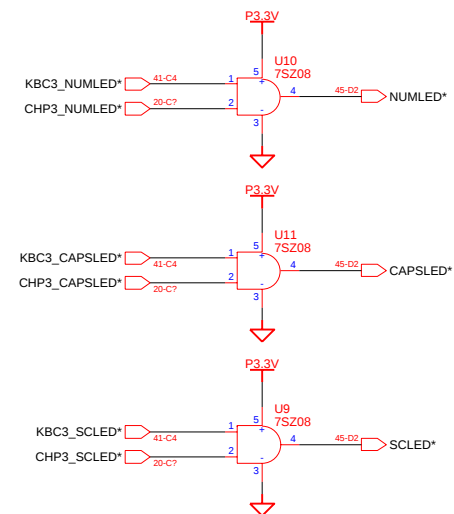


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nostuff



LED SIGNAL



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR		MAIN	
APPROVAL	LIM, J.G	REV	1.0		TPM	
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	54 OF 55	

4			3			2			1																																																														
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TP913○MIC1 TP914○MIC2 TP919○COEX1 TP920○COEX2 TP923○ILIM3 TP924○ILIM5 TP925○MCCKEA TP911○GF3X_C TP912○GF3X_Y TP907○SCLED* TP908○TV03_C TP909○TV03_Y TP890○IDES_A0 TP891○IDES_A1 TP892○IDES_A2 TP893○LB3_LED TP898○CMS_DET* TP873○NUMLED* TP874○SD_DET* TP875○VBUSPWR TP876○XD_DET* TP877○ADPT3_SEL TP878○CAPSLED* TP879○CB3_CCLK TP880○CB3_CPAR TP881○CB3_CVS1 TP882○CB3_CVS2 TP884○CPUL_NMI TP885○CPUL_TCK TP886○CPUL_TDI TP887○CPUL_TMS TP888○CRT3_RED TP889○GF3X_27M TP826○GF3X_RED TP827○HDD03_SEL TP828○HP_OUT_L TP829○HP_OUT_R TP830○IDES_IRQ TP831○JCK_SENS TP712○PC13_PAR TP729○SMB3_CLK TP698○CB3_A_D_2 TP699○CB3_CCD1* TP700○CB3_CCD2* TP701○CB3_CGNT* TP702○CB3_CINT* TP703○CB3_CREQ* TP704○CB3_CRS1* TP705○CB33_SPKR TP706○CHP3_SPKR TP691○CRT3_BLUE TP692○GF3X_BLUE TP693○GF3X_BRIT TP694○GF3X_COMP TP695○GF3X_HCLK TP696○HDD03_LED* TP697○IDES_CSI* TP627○IDES_CSI* TP628○IDES_D(0) TP629○IDES_D(1) TP630○IDES_D(2) TP631○IDES_D(3) TP632○IDES_D(4) TP633○IDES_D(5) TP634○IDES_D(6) TP635○IDES_D(7) TP636○IDES_D(8) TP637○IDES_D(9) TP638○IDES_DREQ TP639○IDES_IOR* TP640○IDES_IOW* TP641○KBC3_A206 TP642○KBC3_RST* TP643○KBC3_VRON TP644○KBC3_TCLK TP645○LAN3_ACT* TP646○LCD03_BRIT TP605○PC13_RST* TP606○PLT3_RST* TP607○SMB3_DATA TP608○TV03_COMP TP610○AUD5_SPDIF TP611○BAT3_VOLTA TP612○CB3_A_A_18 TP613○CB3_A_A_18 TP614○CB3_A_D_14 TP615○CB3_CAD(0) TP616○CB3_CAD(1) TP617○CB3_CAD(2)												TP618○CB3_CAD(3) TP619○CB3_CAD(4) TP620○CB3_CAD(5) TP621○CB3_CAD(6) TP622○CB3_CAD(7) TP623○CB3_CAD(8) TP624○CB3_CAD(9) TP625○CB3_CAUDIO TP626○CB3_CCBE0* TP627○CB3_CCBE1* TP591○CB3_CCBE2* TP592○CB3_CCBE3* TP593○CB3_CIRDY* TP594○CB3_CPERP* TP595○CB3_CSERR* TP596○CB3_CSTOP* TP597○CB3_CTRDY* TP598○CB3_MD_CLK TP599○CB3_VPPEN0 TP600○CB3_VPPEN1 TP601○CB3_GREEN TP585○PWR3_INIT* TP586○GF3X_GREEN TP587○GF3X_HDATA TP588○GF3X_HSYNC TP589○GF3X_VSYNC TP550○IDES_D(0) TP551○IDES_D(1) TP552○IDES_D(2) TP553○IDES_D(3) TP554○IDES_D(4) TP555○IDES_D(5) TP556○IDES_D(6) TP557○IDES_IORDY TP558○IDES_QUEP* TP559○KBC3_CHGEN TP560○KBC3_PWRGD TP561○KBC3_PWRON TP562○KBC5_TDATA TP567○LAN3_WAKE* TP568○LCD3_VDDEN TP571○LED3_LLBAT TP576○PC13_AD(0) TP577○PC13_AD(1) TP578○PC13_AD(2) TP579○PC13_AD(3) TP580○PC13_AD(4) TP581○PC13_AD(5) TP1146○PC13_AD(6) TP1147○PC13_AD(7) TP1148○PC13_AD(8) TP1149○PC13_AD(9) TP1150○PC13_CBE0* TP1151○PC13_CBE1* TP1152○PC13_CBE2* TP1153○PC13_CBE3* TP1154○PC13_GNT0* TP1155○PC13_GNT1* TP1156○PC13_INTA* TP1157○PC13_INTB* TP1158○PC13_INTC* TP1159○PC13_INTD* TP1160○PC13_INTE* TP1161○PC13_INTF* TP1162○PC13_INTG* TP1164○PC13_IRQ* TP1165○PC13_PERR* TP1166○PC13_REQ0* TP1167○PC13_REQ1* TP1168○PC13_REQ2* TP1170○PC13_SERR* TP1171○PC13_STOP* TP1172○PC13_TRDY* TP1173○PEX3_WAKE* TP1114○THERM_STP* TP1115○TV03_C_INT TP1116○TV03_Y_INT TP1117○VGA3_HSYNC TP1118○VGA3_VSYNC TP1119○AUD3_EAPD_A TP1120○AUD3_PCBEEP TP1121○AUD5_SPK_L+ TP1122○AUD5_SPK_L- TP1123○AUD5_SPK_R+ TP1124○AUD5_SPK_R- TP1125○BAT3_SMCLK TP1126○BLT3_DETECT* TP1127○CB3_CAD(0) TP1128○CB3_CAD(1) TP1129○CB3_CAD(2) TP1130○CB3_CAD(3) TP1131○CB3_CAD(4) TP1132○CB3_CAD(5) TP1133○CB3_CAD(6) TP1134○CB3_CAD(7)												TP1135○CB3_CAD(18) TP1136○CB3_CAD(19) TP1137○CB3_CAD(20) TP1138○CB3_CAD(21) TP1139○CB3_CAD(22) TP1140○CB3_CAD(23) TP1141○CB3_CAD(24) TP1142○CB3_CAD(25) TP1143○CB3_CAD(26) TP1144○CB3_CAD(27) TP1145○CB3_CAD(28) TP1095○CB3_CAD(29) TP1096○CB3_CAD(30) TP1097○CB3_CAD(31) TP1098○CB3_CFRAME* TP1099○CB3_CSTSCHG TP1100○CB3_VCC3EN* TP1101○CB3_VCC5EN* TP1102○CHP3_SCLED* TP1103○CHP3_SERRIQ TP1104○CHP3_SLPS3* TP1105○CHP3_SLPS5* TP1106○CHP3_SLPS5* TP1109○CLK3_DBGCLPC TP1110○CLK3_PCLKCB TP1111○CLK3_PWRGD* TP1112○CLK3_SMBCLK TP1113○CLK3_TPMCLPC TP1075○CPU3_ALERT* TP1076○CRT3_DDCCLK TP1077○GF3X_27M_SS TP1078○GF3X_BKLTON TP1079○GF3X_DDCCLK TP1080○GF3X_THERM* TP1081○GF3X_THRMND TP1082○GF3X_THRMCP TP1083○GF3X_VOLTD TP1084○JCK_SENS_HP TP1085○KBC3_BKLTON TP1086○KBC3_LBLEDET TP1087○KBC3_PWR5W* TP1088○KBC3_RFOFF* TP1089○KBC3_SCLED* TP1090○KBC3_SMCLK* TP1091○KBC5_KSI(0) TP1092○KBC5_KSI(1) TP1093○KBC5_KSI(2) TP1094○KBC5_KSI(3) TP1095○KBC5_KSI(4) TP1045○KBC5_KSI(5) TP1046○KBC5_KSI(6) TP1047○KBC5_KSI(7) TP1048○KBC5_KSO(0) TP1049○KBC5_KSO(1) TP1050○KBC5_KSO(2) TP1051○KBC5_KSO(3) TP1052○KBC5_KSO(4) TP1053○KBC5_KSO(5) TP1054○KBC5_KSO(6) TP1055○KBC5_KSO(7) TP1056○KBC5_KSO(8) TP1057○KBC5_KSO(9) TP1064○LCD3_BKLTEN TP1065○LCD3_BKLTEN TP1066○LCD3_EDID_C TP1067○LCD3_EDID_D TP1068○LCD3_CHARGE TP1069○OLPC3_LAD(0) TP1070○OLPC3_LAD(1) TP1071○OLPC3_LAD(2) TP1072○OLPC3_LAD(3) TP1038○CMS_DET*_SUB TP1039○CP13_PSW_PWRGD TP1037○CP13_AD(10) TP1038○CP13_AD(11) TP1039○CP13_AD(12) TP1040○CP13_AD(13) TP1041○CP13_AD(14) TP1042○CP13_AD(15) TP1043○CP13_AD(16) TP1018○CP13_AD(17) TP1019○CP13_AD(18) TP1020○CP13_AD(19) TP1021○CP13_AD(20) TP1022○CP13_AD(21) TP1023○CP13_AD(22) TP1024○CP13_AD(23) TP1025○CP13_AD(24) TP1026○CP13_AD(25) TP1027○CP13_AD(26) TP1028○CP13_AD(27) TP1029○CP13_AD(28) TP1030○CP13_AD(29) TP1031○CP13_AD(30) TP1032○CP13_AD(31)												TP1033○PC13_FRAME* TP999○SD_DET*_SUB TP1001○THERM_SMCLK TP1002○VCCP3_PWRGD TP1003○VGA3_DDCCLK TP1004○SD_DET*_SUB TP1005○BAT3_DETECT* TP1006○BAT3_SMDATA* TP1007○CB3_CCLKRUN* TP1008○CB3_CDEVSEL* TP1009○CB3_MD_DATA1 TP1010○CB3_MD_DATA2 TP1011○CB3_MD_DATA3 TP1012○CB3_MD_VCCEN TP1013○CHP3_AZ_SDIO TP1014○CHP3_AZ_SDI1 TP1015○CHP3_BIOSWP* TP1016○CHP3_NUMLED* TP1017○CHP3_PCISTP* TP983○CHP3_SMLINK0 TP984○CHP3_SMLINK1 TP987○CLK3_PCLKICH TP988○CLK3_PCLKLAN TP989○CLK3_SMBDATA TP990○CPUL_THERMDA TP991○CPUL_THERMDC TP992○CRT3_DDCDATA TP993○FAN3_FDBACK* TP994○GF3X_DDCDATA TP995○HDD03_PATADET TP996○INT3_BUTTON* TP1079○GF3X_BKLTON TP998○JCK_SENS_MIC TP951○KBC3_CPURST* TP952○KBC3_EXTSM* TP953○KBC3_FANCTRL TP954○KBC3_NUMLED* TP955○KBC3_PWMBRIT TP956○KBC3_PWRBTN* TP957○KBC3_RSMRST* TP958○KBC3_RUNSCI* TP959○KBC3_SMDATA* TP960○KBC3_SPMKUTE TP961○KBC5_KSO(10) TP962○KBC5_KSO(11) TP963○KBC5_KSO(12) TP964○KBC5_KSO(13) TP965○KBC5_KSO(14) TP966○KBC5_KSO(15) TP967○PC13_LFRAME* TP974○MCH1_HXSWING TP975○MCH1_HXSWING TP976○MCH3_BMBUSY* TP977○MCH3_CLKREQ* TP950○MCH3_EXTTS0* TP945○MIO3_BUTTON* TP946○PC13_CLKRUN* TP947○PC13_DEVSSEL* TP948○PC13_MIOB(3) TP949○PEG3_MIOB(3) TP941○PEG3_MIOB(4) TP942○PEG3_MIOB(5) TP943○PEG3_MIOB(8) TP1267○P1.8V TP1268○P1.8V TP1269○P1.8V TP1270○P2.5V TP1271○P2.5V TP1272○P2.5V TP1273○P3.3V TP1274○P3.3V TP1275○P3.3V TP1036○CP13_PSW_PWRGD TP1277○PSV_ALWS TP1279○PSV_ALWS TP1280○PSV_ALWS TP1281○PSV_ALWS TP1282○PRTT_BAT TP1223○PRTT_BAT TP1224○P1.8V_AU TP1225○P1.8V_AU TP1019○CP13_AD(18) TP1227○P1.8V_LAN TP1228○P1.8V_LAN TP1229○P1.8V_LAN TP1231○P12V_ALWS TP1232○P12V_ALWS TP1233○P3.3V_AU TP1234○P3.3V_AU TP1235○P3.3V_AU TP1028○CP13_AD(27) TP1236○P1.5V_PCIE TP1238○P1.5V_PCIE TP1239○TV_DND TP1265○P1.5V TP1266○P1.5V												TP1380○THERM_SMDATA TP1391○VGA3_DDCDATA TP1392○VGA3_RED_INT TP1393○CB3_MD_XD_ALE TP1394○CB3_MD_XD_CE* TP1395○CB3_MD_XD_CLE TP1396○CB3_MD_XD_WP* TP1397○CHP3_BIODEL* TP1398○CHP3_CCLKRUN* TP1399○CHP3_DPRSLPVR TP1400○CHP3_SATALED* TP1404○CPUL1_PWRGDGPU TP1405○CPUL_VCCSENSE TP1406○CPUL_VSSSENSE TP1407○GF3X_LCDVDDDD TP1408○KBC3_CAPSLED* TP1409○KBC3_SUSPWON* TP1410○KBC3_WAKESCI* TP1220○LCD3_BKLTCTRL TP1221○MCH3_IHSYNCR* TP1204○PEG3_MIOB(11) TP1205○TV03_COMP_INT* TP1214○VGA3_BLUE_INT TP1215○VGA3_EDID_CLK TP1216○AUD5_SPDIF_OUT TP1217○UBUF5_PLT_RST* TP1218○CB3_MD_CLK_SUB TP1197○CHP3_SATA_DET* TP1202○CPUL_THRMTRIP* TP1200○LAN3_LINK_100* TP1079○GF3X_BKLTON TP1186○VGA3_GREEN_INT TP1187○VRM3_CPU_PWRGD TP1188○AUD5_LINE_OUT_L TP1189○AUD5_LINE_OUT_R TP1190○CB3_MD_DATA4_XD TP1191○CB3_MD_DATA5_XD TP1192○CB3_MD_DATA6_XD TP1193○CB3_MD_DATA7_XD TP1194○CHP3_1304_ROMW* TP1195○CHP3_AZ_AUD_SDO TP1196○CHP3_AZ_MDC_SDO TP1179○KBC3_BLKPRWSW* TP1178○KBC3_INSTANTON* TP1177○SMB3_LINKALERT* TP1176○CB3_MD_DATA1_SUB TP1175○CB3_MD_DATA2_SUB TP1174○CB3_MD_DATA3_SUB TP1347○CB3_MS_BS_SDO_CMD TP1348○CHP3_AZ_AUD_BCLK TP1349○CHP3_AZ_AUD_RST* TP1350○CHP3_AZ_AUD_SYNC TP1351○CHP3_AZ_MDC_BCLK TP1352○CHP3_AZ_MDC_RST* TP1353○CHP3_AZ_MDC_SYNC TP1354○CHP3_SATACLKREQ* TP1357○KBC3_THERM_SMCLK TP1358○CB3_MD_XD_ALE_SUB TP1359○CB3_MD_XD_CE*_SUB TP1360○CB3_MD_XD_CLE_SUB TP1361○CB3_MD_XD_WP*_SUB TP1362○CB3_SD_CD*_XD_CD* TP1363○KBC3_THERM_SMDATA TP1364○CB3_MS_IN*_XD_CD* TP1365○CB3_SD_WP*_XD_R_B* TP1366○CB3_MD_DATA4_XD_SUB TP1367○CB3_MD_DATA5_XD_SUB TP1368○CB3_MD_DATA6_XD_SUB TP1369○CB3_MD_DATA7_XD_SUB TP1370○MINIPCIES_CLKREQ_A* TP1371○MINIPCIES_CLKREQ_B* TP1372○CB3_MD_DATA5_SDO TP1373○CB3_MS_BS_SDO_CMD TP1374○CB3_SD_CD*_XD_CD*_SUB TP1375○CB3_MS_IN*_XD_CD*_SUB TP1376○CB3_SD_WP*_XD_R_B*_SUB TP1377○CB3_MD_DATA0_MS_SDO_SUB												TP1320○AVDD TP1321○CB3_MD_XD_CE* TP1322○AVDD TP1323○AMP_VDD TP1324○AMP_VDD TP1325○AMP_VDD TP1326○AGND_AUD TP1327○AGND_AUD TP1328○AGND_AUD TP1329○AGND_CHG TP1330○AGND_CHG TP1331○AGND_CHG TP1332○AGND_VGA TP1333○AGND_VGA TP1334○AGND_VGA TP1335○AD_IN_SUB TP1336○AD_IN_SUB TP1337○AD_IN_SUB TP1338○AGND_P3.3V TP1340○AGND_P3.3V TP1341○CGND TP1342○CGND TP1343○CGND TP1344○C_AGNND TP1345○C_AGNND TP1346○C_AGNND TP1283○CHG_REF TP1285○CHG_REF TP1287○CB3_VCCA TP1288○CB3_VCCA TP1289○CB3_VPPA TP1290○CB3_VPPA TP1292○D_AGNND TP1293○D_AGNND TP1294○D_AGNND TP1295○GFX_CORE TP1296○GFX_CORE TP1297○GFX_CORE TP1298○INV_VDC TP1242○VDC TP1243○VDC TP1244○VDC TP1245○VCCP TP1246○VCCP TP1247○VCCP TP1248○VCC_CORE TP1249○VCC_CORE TP1250○VCC_CORE TP1303○LCD_VDD3V TP1305○LDDO_P5.4V TP1306○LDDO_P5.4V TP1308○MID_VCC TP1309○MID_VCC TP1310○MEM1_VREF TP1311○MEM1_VREF TP1312○MEM1_VREF TP1313○MICOM_P3V TP1314○MICOM_P3V TP1251○MICOM_P3V TP1252○MID_VCC_SUB TP1253○MID_VCC_SUB TP1254○MID_VCC_SUB TP1255○PSV TP1256○PSV TP1257○PSV TP1258○P0.9V TP1259○P0.9V TP1260○P0.9V TP1261○P1.2V TP1262○MID_VCC_SUB TP1263○P1.2V TP1264○P1.5V											
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