1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Sully

M9 MLB
3/3/2006

DVT
(6.0.0)

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

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3	3	Power Block Diagram	(MASTER)	(MASTER)
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6	6	Signal Aliases	(M1_MLB)	(11/11/2005)
7	7	CPU 1 OF 2-FSB	M1_MLB	02/10/2006
8	8	CPU 2 OF 2-PWR/GND	M1_MLB	02/10/2006
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10	10	CPU MISC1-TEMP SENSOR	M1_MLB	02/10/2006
11	11	CPU ITP700FLEX DEBUG	M1_MLB	02/10/2006
12	12	NB CPU Interface	M1_MLB	02/10/2006
13	13	NB PEG / Video Interfaces	M1_MLB	02/10/2006
14	14	NB Misc Interfaces	M1_MLB	02/10/2006
15	15	NB DDR2 Interfaces	M1_MLB	02/10/2006
16	16	NB Power 1	M1_MLB	02/10/2006
17	17	NB Power 2	M1_MLB	02/10/2006
18	18	NB Grounds	M1_MLB	02/10/2006
19	19	NB (GM) Decoupling	M1_MLB	02/08/2006
20	20	NB Config Straps	M1_MLB	02/10/2006
21	21	SB: 1 OF 4	M1_MLB	02/10/2006
22	22	SB: 2 of 4	M1_MLB	02/10/2006
23	23	SB: 3 OF 4	M1_MLB	02/10/2006
24	24	SB: 4 OF 4	M1_MLB	02/10/2006
25	25	SB Decoupling	M1_MLB	02/10/2006
26	26	SB Misc	M1_MLB	02/10/2006
27	27	M1 SMBus Connections	M1_MLB	01/04/2006
28	28	DDR2 SO-DIMM Connector A	M1_MLB	02/10/2006
29	29	DDR2 SO-DIMM Connector B	M1_MLB	02/10/2006
30	30	Memory Active Termination	(M1_MLB)	(11/07/2006)
31	31	Memory Vtt Supply	M1_MLB	02/10/2006
32	32	DDR2 VRef	M1_MLB	12/19/2005
33	33	CLOCKS	M1_MLB	02/10/2006
34	34	Clock Termination	M1_MLB	02/10/2006
35	37	Mobile Clocking	M1_MLB	02/10/2006
36	38	PATA Connector	M1_MLB	02/10/2006
37	39	FireWire Link (TSB83AA22)	(MASTER)	(MASTER)
38	40	FireWire PHY (TSB83AA22)	(MASTER)	(MASTER)
39	41	ETHERNET CONTROLLER	M1_MLB	02/10/2006
40	42	Ethernet Connector	M1_MLB	02/10/2006
41	43	Yukon Power Control	M1_MLB	02/10/2006
42	44	FW PHY Power Supply	(MASTER)	(MASTER)
43	45	FireWire Port Power	(M1_MLB)	(11/03/2005)
44	46	FireWire Ports	(MASTER)	(MASTER)
45	49	Internal USB Connections	M1_MLB	02/10/2006
46	52	External USB Connector	M1_MLB	02/10/2006
47	55	Left I/O Board Connector	(MASTER)	(MASTER)
48	56	Current & Thermal Sensors	(MASTER)	(MASTER)
49	57	PCI-E Connections	M1_MLB	02/10/2006
50	58	SMC	M1_MLB	02/10/2006
51	59	SMC Support	M1_MLB	02/10/2006
52	60	LPC+ Debug Connector	M1_MLB	02/10/2006
53	61	Thermal Sensors	M1_MLB	02/10/2006
54	62	Current & Voltage Sensing	M1_MLB	01/05/2006
55	63	SPI BOOTROM	M1_MLB	02/10/2006
56	64	ALS Support	M1_MLB	02/10/2006
57	65	Fan Connectors	M1_MLB	02/10/2006
58	66	Sudden Motion Sensor (SMS)	M1_MLB	02/10/2006
59	67	TPM	M1_MLB	02/10/2006
60	75	IMVP6 CPU VCore Regulator	M1_MLB	02/08/2006
61	76	5V / 1.5V Power Supply	M1_MLB	02/10/2006
62	77	2.5V & 1.2V Regulators	M1_MLB	02/10/2006
63	78	1.8V Supply	M1_MLB	02/10/2006
64	79	3.3V / 1.05V Power Supplies	M1_MLB	02/10/2006
65	80	3.3V G3Hot Supply & Power Control	M1_MLB	02/10/2006
66	81	Power Aliases	M1_MLB	12/19/2005
67	82	DC-In & Battery Connectors	(MASTER)	(MASTER)
68	83	PBus Supply & Batt. Charger	M1_LIO	12/19/2005
69	84	ATI M56 PCI-E	M1_MLB	02/10/2006
70	85	GPU (M56) Core Supplies	M1_MLB	02/10/2006
71	86	ATI M56 Core Power	M1_MLB	02/10/2006
72	87	ATI M56 Frame Buffer I/F	M1_MLB	02/10/2006
73	88	GPU Straps	M1_MLB	02/10/2006
74	89	GDDR3 Frame Buffer A	M1_MLB	02/10/2006
75	90	GDDR3 Frame Buffer B	M1_MLB	02/10/2006
76	91	ATI M56 GPIO/DVO/Misc	M1_MLB	02/10/2006
77	93	ATI M56 Video Interfaces	M1_MLB	02/10/2006
78	94	Internal Display Connectors	M1_MLB	01/09/2006
79	97	External Display Connector	M1_MLB	11/18/2005
80	98	M9 Specific Connectors	(MASTER)	(MASTER)
81	99	LVDS Interface Pull-downs	M1_MLB	12/19/2005
82	100	Revision History	(MASTER)	(MASTER)
83	101	Napa Platform Constraints	M1_MLB	02/10/2006
84	102	More System Constraints	M1_MLB	02/10/2006
85	103	M1 Spacing & Physical Constraints	M1_MLB	02/10/2006
86	104	M1 Net Properties	M1_MLB	02/10/2006

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7023	1	SCHEM,SULLY,M9	SCH	CRITICAL	
820-2023	1	PCBF,SULLY,FINAL,M9	PCB	CRITICAL	

DRAWING
TITLE=SULLY
ABBREV=DRAWING
LAST_MODIFIED=Fri Mar 3 17:59:45 2006

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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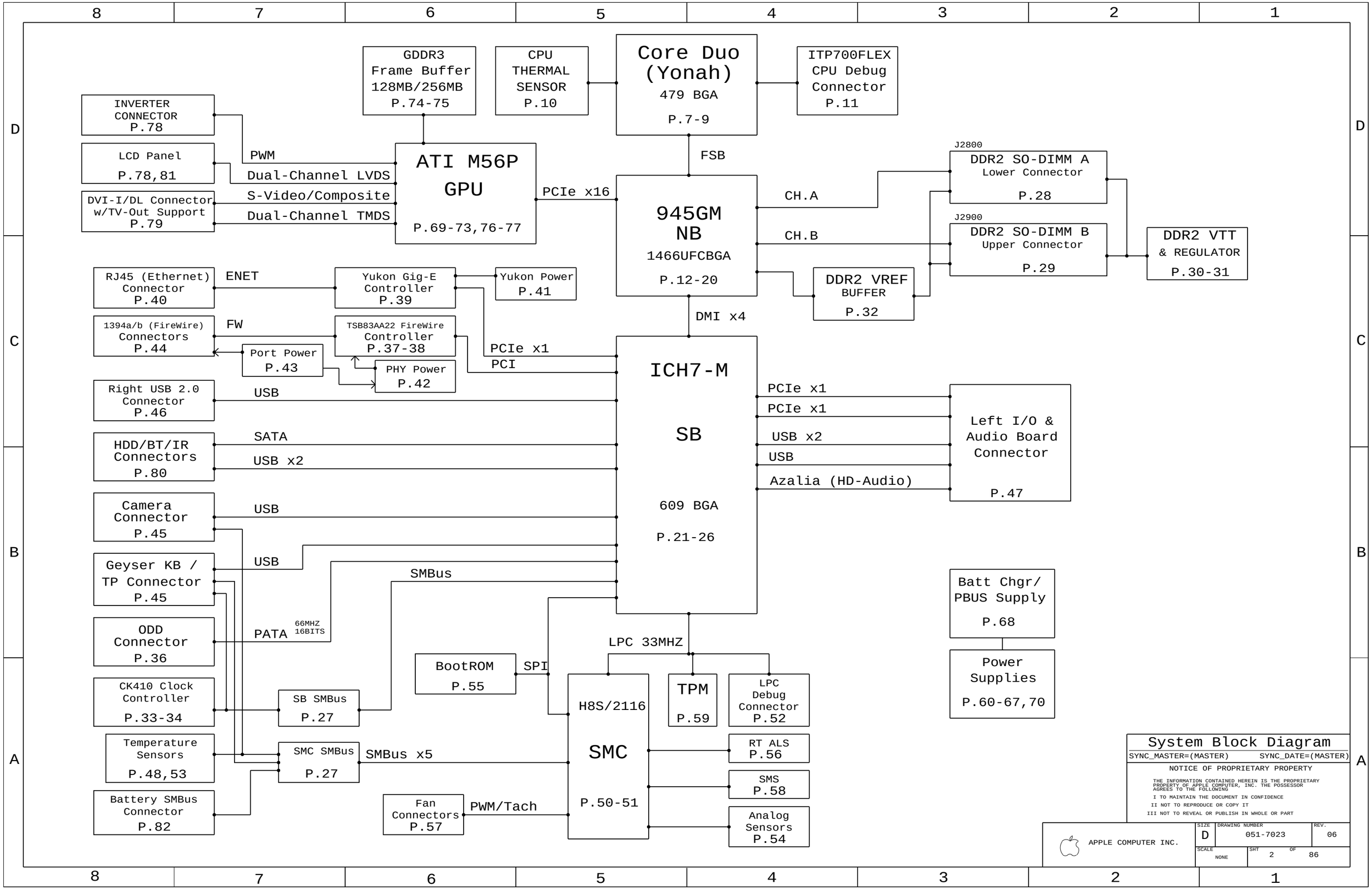
TITLE
SCHEM,SULLY,M9

DRAWING NUMBER 051-7023 REV. 06

SHT 1 OF 86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CPU THERMAL SENSOR P.10
Core Duo (Yonah) 479 BGA P.7-9
ITP700FLEX CPU Debug Connector P.11
INVERTER CONNECTOR P.78
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PCIe x1
USB x2
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USB x2
Camera Connector P.45
USB
Geyser KB / TP Connector P.45
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Batt Chgr/ PBUS Supply P.68
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ODD Connector P.36
PATA
66MHZ 16BITS
LPC 33MHZ
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H8S/2116 SMC P.50-51
TPM P.59
LPC Debug Connector P.52
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SMC SMBus P.27
SMBus x5
RT ALS P.56
SMS P.58
Analog Sensors P.54
Battery SMBus Connector P.82
Fan Connectors P.57
PWM/Tach
System Block Diagram
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
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REV. 06
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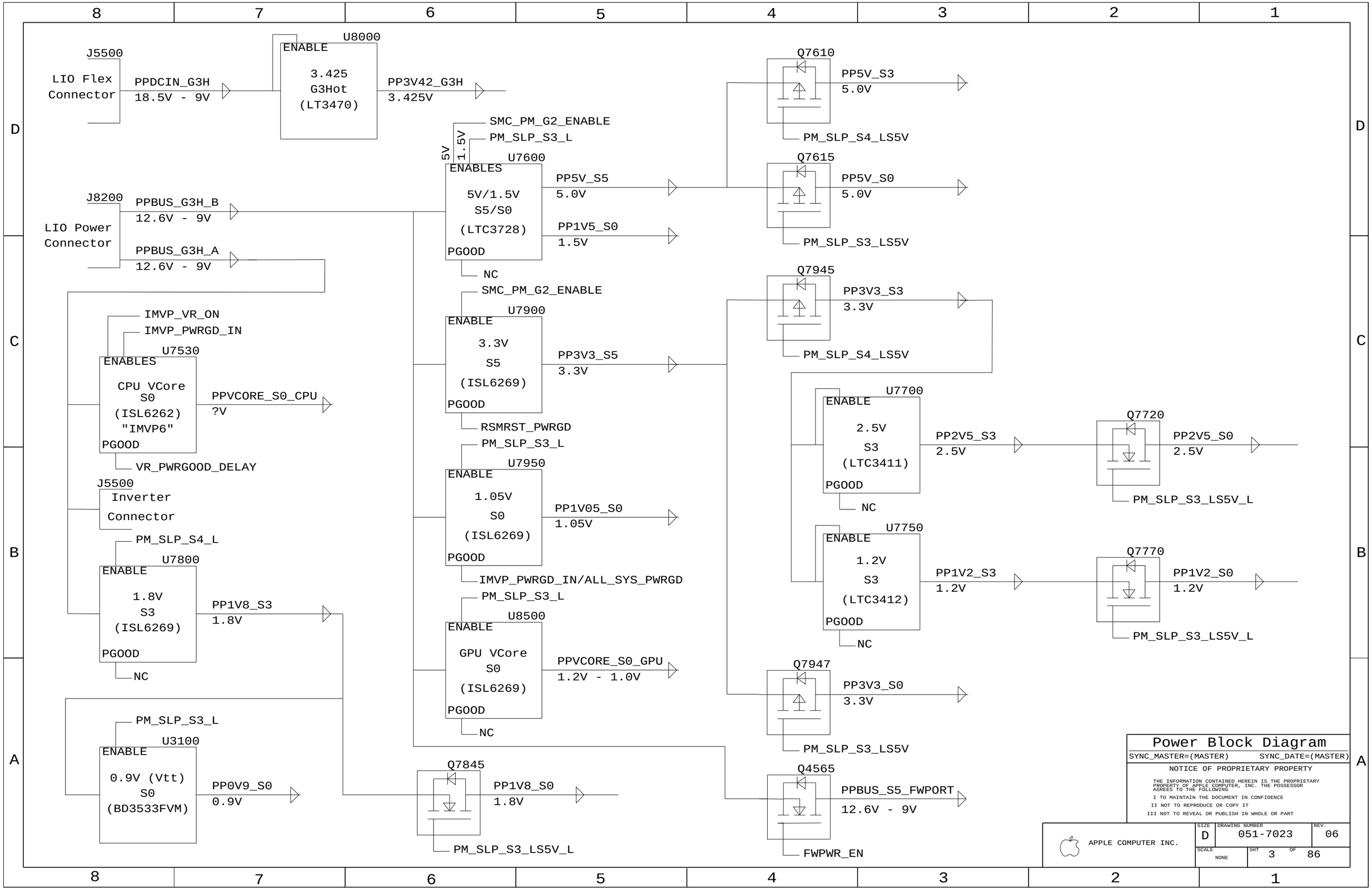
SHT 2 OF 86


J5500
LIO Flex Connector
PPDCIN_G3H
18.5V - 9V
U8000
ENABLE
3.425 G3Hot (LT3470)
PP3V42_G3H
3.425V
J8200
LIO Power Connector
PPBUS_G3H_B
12.6V - 9V
PPBUS_G3H_A
12.6V - 9V
SMC_PM_G2_ENABLE
PM_SLP_S3_L
5V
1.5V
U7600
ENABLES
5V/1.5V S5/S0 (LTC3728)
PGOOD
PP5V_S5
5.0V
PP1V5_S0
1.5V
NC
Q7610
PP5V_S3
5.0V
PM_SLP_S4_LS5V
Q7615
PP5V_S0
5.0V
PM_SLP_S3_LS5V
SMC_PM_G2_ENABLE
U7900
ENABLE
3.3V S5 (ISL6269)
PGOOD
PP3V3_S5
3.3V
RSMRST_PWRGD
Q7945
PP3V3_S3
3.3V
PM_SLP_S4_LS5V
IMVP_VR_ON
IMVP_PWRGD_IN
U7530
ENABLES
CPU VCore S0 (ISL6262) "IMVP6"
PGOOD
PPVCORE_S0_CPU
?V
VR_PWRGOOD_DELAY
J5500
Inverter Connector
PM_SLP_S3_L
U7950
ENABLE
1.05V S0 (ISL6269)
PGOOD
PP1V05_S0
1.05V
IMVP_PWRGD_IN/ALL_SYS_PWRGD
U7700
ENABLE
2.5V S3 (LTC3411)
PGOOD
NC
PP2V5_S3
2.5V
Q7720
PP2V5_S0
2.5V
PM_SLP_S3_LS5V_L
PM_SLP_S4_L
U7800
ENABLE
1.8V S3 (ISL6269)
PGOOD
NC
PP1V8_S3
1.8V
U7750
ENABLE
1.2V S3 (LTC3412)
PGOOD
NC
PP1V2_S3
1.2V
Q7770
PP1V2_S0
1.2V
PM_SLP_S3_LS5V_L
PM_SLP_S3_L
U8500
ENABLE
GPU VCore S0 (ISL6269)
PGOOD
NC
PPVCORE_S0_GPU
1.2V - 1.0V
Q7947
PP3V3_S0
3.3V
PM_SLP_S3_LS5V
PM_SLP_S3_L
U3100
ENABLE
0.9V (Vtt) S0 (BD3533FVM)
PP0V9_S0
0.9V
Q7845
PP1V8_S0
1.8V
PM_SLP_S3_LS5V_L
Q4565
PPBUS_S5_FWPORT
12.6V - 9V
FWPWR_EN
Power Block Diagram
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
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06
SCALE
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SHT
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OF
86

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7404	PCBA,SULLY,2.0GHz,M9	VRAM_256SAM,M9_COMMON,CPU_2_0GHZ,EEE_UNZ
630-7406	PCBA,SULLY,2.16GHz,M9	VRAM_256SAM,M9_COMMON,CPU_2_16GHZ,EEE_UP1

BOM GROUP	BOM OPTIONS
VRAM_128SAM	VRAM_128_SAMSUNG
VRAM_256SAM	GPU_MEM_256M,VRAM_256_SAMSUNG
VRAM_128HY	GPU_MEM_HYNIX,VRAM_128_HYNIX
VRAM_256HY	GPU_MEM_HYNIX,GPU_MEM_256M,VRAM_256_HYNIX

BOM GROUP	BOM OPTIONS
M9_COMMON	ALTERNATE,COMMON,M9_COMMON1,M9_COMMON2,M9_COMMON3,M9_COMMON4,M9_DEBUG
M9_COMMON1	ENET_LOM_DISABLE,ENETPWR_S3AC,GPUTHM_A_GPU,GPU_BB_CTL,HSTHMSNS_HAS,INVERTER_BUF,ONEWIRE_PU
M9_COMMON2	KBDLED_HAS,MEMVREF_S3,MEMVTT_EN_PU,RTUSB_ESD,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
M9_COMMON3	LVDS_PD,M56_REV_B24_LP,FW_B_BILINGUAL,FW_A_DS_ONLY,FW_PORT_FAULT_PU,FW_PLTRST_UNGATED
M9_COMMON4	LIO_TEMP,BOOTROM_DEVEL,SMC_DEVEL
M9_DEBUG	ITP,ITPCONN,LPCPLUS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1876	1	IC,SMC,PRGRM,M9	U5800	CRITICAL	SMC_DEVEL
341S1876	1	IC,SMC,PRGRM,M9	U5800	CRITICAL	SMC_FINAL
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6301	CRITICAL	BOOTROM_BLANK
341S1828	1	IC,EFI,BOOTROM DEVELOPMENT,M9	U6301	CRITICAL	BOOTROM_DEVEL
341S1829	1	IC,EFI,BOOTROM FINAL,M9	U6301	CRITICAL	BOOTROM_FINAL
353S1235	1	IC,CPU VOLTAGE REGULATOR,IMVP,TWO PHASE	U7530	CRITICAL	
359S0101	1	IC,CY28445-5,CLOCK GEN,68PIN QFN	U3301	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3282	1	IC,CPU,479 BGA	U0700	CRITICAL	CPU_1_83GHZ
337S3267	1	IC,CPU,479 BGA	U0700	CRITICAL	CPU_2_0GHZ
337S3268	1	IC,CPU,479 BGA	U0700	CRITICAL	CPU_2_16GHZ
338S0269	1	IC,945GM,SOUTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UNZ]	CRITICAL	EEE_UNZ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UP0]	CRITICAL	EEE_UP0
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UP1]	CRITICAL	EEE_UP1
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UP2]	CRITICAL	EEE_UP2
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UYU]	CRITICAL	EEE_UYU

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0266	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	M56_REV_B24_LL
338S0302	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	M56_REV_B24_HL
338S0309	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	M56_REV_B24_LP
338S0315	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	M56_REV_B26_LP
338S0316	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	M56_REV_B26_P
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0309	338S0266	M56_REV_B24_LL	U8400	LP is alt to LL
338S0266	338S0309	M56_REV_B24_LP	U8400	LL is alt to LP
338S0315	338S0309	M56_REV_B24_LP	U8400	B26_LP is alt to B24_LP
376S0448	376S0445		ALL	Vishay 2nd source
128S0083	128S0073		C2516	1.86 max alt to 1.9 max
128S0093	128S0092		ALL	Kemet is alt to Sanyo
128S0060	128S0094		ALL	Sanyo is alt to Panasonic
128S0095	128S0094		ALL	330uF,2V,6MOHM,D2
128S0081	128S0061		ALL	C2 package is alt to C3

M9 Specific Aliases

64 63 61 60 54 47 43 41 5 4 78 70 68 66	PPBUS_G3H	PPBUS_G3H	4 5 41 43 47 54 60 61 63 64 66 68 70 78
68 67 66 65 4	PPDCIN_G3H	PPDCIN_G3H	4 65 66 67 68
		PPDCIN_G3H	4 65 66 67 68
50 37 4	SMC_RSTGATE_L MAKE_BASE=TRUE	SMC_RSTGATE_L	4 37 50
44 43 4	PPFW_PORTA_VP_UF MAKE_BASE=TRUE	PPFW_PORTA_VP_UF	4 43 44
44 43 4	PPFW_PORTB_VP_UF MAKE_BASE=TRUE	PPFW_PORTB_VP_UF	4 43 44
64 60 59 57 56 53 51 48 43 23 22 21 20 19 17 14 10 5 4 37 36 34 33 29 28 27 26 25 22 78 70 70 70 66 65	PP3V3_S0	PP3V3_S0	48 51 53 56 57 59 60 64 65 66 4 5 10 14 17 19 20 21 22 23 24 25 26 27 28 29 33 34 36 37 43 70 70 70
		PP3V3_S0	48 51 53 56 57 59 60 64 65 66 4 5 10 14 17 19 20 21 22 23 24 25 26 27 28 29 33 34 36 37 43 70 70 70
		PP3V3_S0	48 51 53 56 57 59 60 64 65 66 4 5 10 14 17 19 20 21 22 23 24 25 26 27 28 29 33 34 36 37 43 70 70 70
50 48 27 10 4	SMBUS_SMC_B_S0_SCL	SMBUS_SMC_B_S0_SCL	4 10 27 48 50
50 48 27 10 4	SMBUS_SMC_B_S0_SDA	SMBUS_SMC_B_S0_SDA	4 10 27 48 50
37 22	PCI_AD<19> MAKE_BASE=TRUE	=FW_PCI_IDSEL	37
56 54 52 47 42 36 31 25 5 4 80 79 78 70 67 66 65 61 60 57	PP5V_S0	PP5V_S0	4 5 25 31 36 42 47 57 54 56 57 60 61 65 66 67 70 78 79 80
66 43 42 38 4	PPBUS_S5_FW_FET	PPBUS_S5_FW_FET	4 38 42 43 66
		PPBUS_S5_FW_FET	4 38 42 43 66
		PPBUS_S5_FW_FET	4 38 42 43 66
44 43 42 38 5 4 PP3V3_FWPHY 44 43 42 38 5 4	PP3V3_FWPHY VOLTAGE=3.3V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm MAKE_BASE=TRUE	PP3V3_FWPHY	4 5 38 42 43 44
		PP3V3_FWPHY	4 5 38 42 43 44
		PP3V3_FWPHY	4 5 38 42 43 44
		PP3V3_FWPHY	4 5 38 42 43 44
		PP3V3_FWPHY	4 5 38 42 43 44
42 38 5 4 PP1V95_FWPHY 42 38 5 4	PP1V95_FWPHY VOLTAGE=1.95V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm MAKE_BASE=TRUE	PP1V95_FWPHY	4 5 38 42
		PP1V95_FWPHY	4 5 38 42
37 32 31 29 28 19 16 14 5 4 66 63 54	PP1V8_S3	PP1V8_S3	4 5 14 16 19 28 29 31 32 37 54 63 66
47 22 5 4	LT2USB_OC_L MAKE_BASE=TRUE	LT2USB_OC_L	4 5 22 47
37 22 4	PCI_GNT3_L MAKE_BASE=TRUE	PCI_GNT3_L	4 22 37
37 26 22 4	PCI_REQ3_L MAKE_BASE=TRUE	PCI_REQ3_L	4 22 26 37

BOM Configuration

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7023	06

SCALE NONE

Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	60
TRUE		P5VS5_RUNSS	61 65
TRUE		P1V5S0_RUNSS	61 65
TRUE		P2V5S3_MODE	62
TRUE		P2V5S3_SHDNRT	62
TRUE		P1V2S3_RT	62
TRUE		P1V2S3_RUNSS	41 62
TRUE		P1V8S3_COMP	63
TRUE		P1V8S3_FSET	63
TRUE		P3V3S5_COMP	64
TRUE		P3V3S5_FSET	64
TRUE		P1V05S0_COMP	64
TRUE		P1V05S0_FSET	64
TRUE		P3V42G3H_FB	65
TRUE		GPUVCORE_COMP	70
TRUE		GPUVCORE_FSET	70
TRUE		GPUBBP_ADJ	70

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7 12 86
TRUE		FSB_ADS_L	7 12 86
TRUE	TRUE	FSB_ADSTB_L<1..0>	7 12 86
TRUE		FSB_BNR_L	7 12 86
TRUE		FSB_BREQ0_L	7 12 86
TRUE		FSB_D_L<63..0>	7 12 86
TRUE		FSB_DBSY_L	7 12 86
TRUE	TRUE	FSB_DINV_L<3..0>	7 12 86
TRUE		FSB_DRDY_L	7 12 86
TRUE	TRUE	FSB_DSTBN_L<3..0>	7 12 86
TRUE	TRUE	FSB_DSTBP_L<3..0>	7 12 86
TRUE		FSB_HIT_L	7 12 86
TRUE		FSB_HITM_L	7 12 86
TRUE		FSB_LOCK_L	7 12 86
TRUE		FSB_REQ_L<4..0>	7 12 86

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14 22
TRUE	DMI_N2S_N<1..0>	14 22
TRUE	SB_CLK100M_SATA_P	21 34
TRUE	SB_CLK100M_SATA_N	21 34

Power Nets

FUNC_TEST			
TRUE	PP0V9_S0		30 31 65 66
TRUE	PP1V05_S0		5 7 8 9 11 12 13 16 17 19 21 24 29 33 54 64 66
TRUE	PP1V2_S0		62 65 66 69 76
TRUE	PP1V2_S3		5 39 62 66
TRUE	PP1V5_S0		5 8 9 13 16 17 19 24 25 47 65 66
TRUE	PP1V8_S0		63 65 66
TRUE	PP1V8_S3		4 5 24 16 19 28 29 31 32 37 54 63 66
TRUE	PP2V5_S0		17 19 62 65 66 76 77
TRUE	PP2V5_S3		39 62 66
TRUE	PP3V3_S0		70 78 79 48 51 53 56 57 59 60 64 65 66 4 5 10 14 17 19 20 21 22 23 24 25 26 27 28 29 33 34 36 37 43
TRUE	PP3V3_S3		27 32 37 41 45 51 56 58 59 62 63 64 66 80
TRUE	PP3V3_S5		11 22 23 24 25 26 55 62 64 65 66 78
TRUE	PP5V_S0		78 79 80 4 5 29 31 36 42 47 52 54 56 57 60 61 65 66 67 70
TRUE	PP5V_S3		5 45 51 61 66 80
TRUE	PP5V_S5		5 25 46 51 61 63 64 65 66 67 70
TRUE	PPBUS_G3H		4 5 21 43 47 54 60 61 63 64 65 68 70 78
TRUE	GND		

Request for at least 10 GND TPs

Characterization TPs

FUNC_TEST		
TRUE	IMVP_VR_ON	50 60
TRUE	IMVP_DPRSLPVR	60 86
TRUE	PM_SLP_S3_L	23 32 39 43 50 54 64 65
TRUE	PM_SLP_S3BATT	41
TRUE	PM_SLP_S4_L	5 23 41 46 47 50 63 65
TRUE	PM_SLP_S5_L	23 50 51
TRUE	P1V5P1V05S0_PGOOD	60 64 65
TRUE	CPU_DPRSTP_L	7 21 60
TRUE	IMVP6_VID<6..0>	9 60
TRUE	FSB_CLK_CPU_N	7 34
TRUE	FSB_CLK_CPU_P	7 34
TRUE	PLT_RST_L	5 14 22 26
TRUE	PLT_RST_L	5 14 22 26
TRUE	PEG_RESET_L	26 69
TRUE	SMC_LRESET_L	26 50
TRUE	TPM_LRESET_L	26 59
TRUE	CPU_STPCLK_L	7 21 86
TRUE	FSB_CLK_NB_P	12 34
TRUE	FSB_CLK_NB_N	12 34
TRUE	CLK_NB_OE_L	14 33
TRUE	NB_CLK100M_GCLKIN_P	14 34
TRUE	NB_CLK100M_GCLKIN_N	14 34
TRUE	GND	
TRUE	GND	
TRUE	GND	
TRUE	GND	
TRUE	CPU_THERMTRIP_R	21
TRUE	TP_SB_SUS_CLK	6 23

MAC-1 TPs

FUNC_TEST			
TRUE	CPU_PWRGD		7 21 86
TRUE	TP_CPU_CPUSLP_L		21
TRUE	PM_DPRSLPVR		14 23 60 86
TRUE	CPU_DPSLP_L		7 21 86
TRUE	PM_LAN_ENABLE		23 50
TRUE	PCI_RST_L		22 37
TRUE	PM_RSMRST_L		23 50
TRUE	PM_SB_PWROK		23 26
TRUE	SB_RTC_RST_L		21 26
TRUE	PM_STPCPU_L		23 33
TRUE	PM_STPPCI_L		23 33
TRUE	VR_PWRGD_CK410		23 26
TRUE	VR_PWRGOOD_DELAY		14 26 60
TRUE	FSB_CPURST_L		7 11 12 86
TRUE	FSB_SLPCPU_L		7 12
TRUE	FSB_DPWR_L		7 12 86
TRUE	NB_SB_SYNC_L		14 22
TRUE	PP2V5_S0_GPU_TPVDD		77
TRUE	PP2V5_S0_GPU_TXVDDR		77
TRUE	PP2V5_S0_GPU_AVDD		77
TRUE	PP2V5_S0_GPU_A2VDD		77
TRUE	PP2V5_S0_GPU_LPVDD		77
TRUE	PP2V5_S0_GPU_LVDDR		59 60 64 65 66 70 78 79
TRUE	PP3V3_S0		23 26 29 33 4 5 10 14 17 19 20 21 22 23 24 25 26 27 34 36 37 43 48 51 53 56 57 (=PP3V3_S0_CK410)
TRUE	PP3V3_S0_CK410_VDD48		33
TRUE	PP3V3_S0_CK410_VDD_PCI		33
TRUE	PP3V3_S0_CK410_VDD_REF		33
TRUE	PP3V3_S0_CK410_VDD_CPU_SRC		33
TRUE	PP3V3_S0_CK410_VDDA		33
TRUE	PP3V3_FWPHY		4 38 42 43 44
TRUE	PP3V3_FWPHY_AVDD		38
TRUE	PP3V3_FWPHY_PLLVDD		38
TRUE	PP1V95_FWPHY		4 38 42
TRUE	PP1V95_FWPHY_PLLVDD		38
TRUE	PP1V2_S3		5 39 62 66 (=PP1V2_S3_ENET)
TRUE	PP3V3_S3AC		39 41 66 (=PP3V3_S3_ENET)
TRUE	PP2V5_S3		5 39 62 66 (=PP2V5_S3_ENET)
TRUE	PP2V5_S3_ENET_AVDD		39 40

Fan Connectors

FUNC_TEST		
TRUE	PP5V_S0	66 67 70 78 79 80 4 5 29 31 36 42 47 52 54 56 57 60 61 65
TRUE	FAN_LT_PWM	57
TRUE	FAN_LT_TACH	57
TRUE	FAN_RT_PWM	57
TRUE	FAN_RT_TACH	57

LPC+ Debug Connector

FUNC_TEST		
TRUE	PP3V42_G3H	68 5 26 27 35 45 50 51 52 54 65 66
TRUE	PP5V_S0	66 67 70 78 79 80 4 5 29 31 36 42 47 52 54 56 57 60 61 65
TRUE	LPC_AD<0>	21 50 52 59
TRUE	LPC_AD<1>	21 50 52 59
TRUE	LPC_FRAME_L	21 50 52 59
TRUE	PM_CLKRUN_L	23 50 52 59
TRUE	BOOT_LPC_SPI_L	22 50 52
TRUE	SMC_TMS	50 51 52
TRUE	DEBUG_RST_L	26 52
TRUE	SMC_TRST_L	50 52
TRUE	SMC_TDO	50 51 52
TRUE	SMC_MD1	50 52
TRUE	SMC_TX_L	50 51 52
TRUE	FWH_INIT_L	21 50 51 52
TRUE	PCI_CLK_PORT80_LPC	34 52
TRUE	LPC_AD<2>	21 50 52 59
TRUE	LPC_AD<3>	21 50 52 59
TRUE	INT_SERIRQ	23 50 52 59
TRUE	PM_SUS_STAT_L	23 50 51 52 59
TRUE	SMC_TDI	50 51 52
TRUE	SMC_TCK	50 51 52
TRUE	SMC_RST_L	50 51 52
TRUE	SMC_NMI	50 52
TRUE	SMC_RX_L	50 51 52
TRUE	SV_SET_UP	23 52

Resistor Calibration

FUNC_TEST			
TRUE	PP5V_S0		66 67 70 78 79 80 4 5 29 31 36 42 47 52 54 56 57 60 61 65
TRUE	PP1V8_S3		4
TRUE	PP1V05_S0		64 66 5 7 8 9 11 12 13 16 17 19 21 24 25 33 54
TRUE	PPVCORE_S0_CPU		8 9 54 60 66
TRUE	PPVCORE_S0_GPU		54 66 70 71 76
TRUE	ISENSE_CAL_EN		50 54
TRUE	GND		

Request for at least 2 GND TPs per resistor

Camera Connector

FUNC_TEST		
TRUE	PP5V_S3	5 45 51 61 66 80
TRUE	USB2_CAMERA_N	6 22 45
TRUE	USB2_CAMERA_P	6 22 45
TRUE	SMBUS_SMC_0_S0_SDA	27 45 50 53
TRUE	SMBUS_SMC_0_S0_SCL	27 50 53

Thermal Sensors

FUNC_TEST		
TRUE	HSTHMSNS_DX_P	53
TRUE	HSTHMSNS_DX_N	53
TRUE	RSFSTHMSNS_D_P	53
TRUE	RSFSTHMSNS_D_N	53

SMC TPs

FUNC_TEST		
TRUE	PM_SYSRST_L	23 26 50
TRUE	SMC_ONOFF_L	45 50 51 54

Battery Connector

FUNC_TEST		
TRUE	BATT_POS	67 68
TRUE	BATT_NEG	67 68
TRUE	SMC_BS_ALRT_L	50 51 67
TRUE	SMBUS_SMC_BSA_SCL	27 50 67
TRUE	SMBUS_SMC_BSA_SDA	27 50 67

Left I/O Data Connector

FUNC_TEST		
TRUE	PP1V5_S0	25 47 65 66 5 8 9 13 16 17
TRUE	PPBUS_G3H	68 70 78 79 19 24 4 5 41 43 47 54 60 61 63 64 66
TRUE	PP3V42_G3H	5 26 27 35 45 50 51 52 54 65 66
TRUE	PP5V_S0_AUDIO	67
TRUE	GND_AUDIO	47
TRUE	ALS_GAIN	6 47 50
TRUE	LTALS_OUT	47 56
TRUE	ACZ_SDATAIN<0>	21 47 86
TRUE	ACZ_SDATAOUT	21 47 86
TRUE	ACZ_BITCLK	21 47 86
TRUE	ACZ_RST_L	21 47 86
TRUE	EXCARD_OC_L	6 22 47 51
TRUE	LTUSB_OC_L	6 22 47
TRUE	LT2USB_OC_L	4 22 47
TRUE	PM_SLP_S3_LS5V	47 61 65
TRUE	PM_SLP_S4_L	5 23 41 46 47 50 63 65
TRUE	SYS_ONEWIRE	47 50 51
TRUE	MINI_CLKREQ_L	33 34 47
TRUE	SMC_EXCARD_CP	47 50 51
TRUE	EXCARD_CLKREQ_L	33 34 47
TRUE	SMC_EXCARD_PWR_EN	47 50
TRUE	LIO_PLT_RESET_L	26 47
TRUE	ACZ_SYNC	21 47 86
TRUE	USB2_LT_N	6 22 47
TRUE	USB2_LT_P	6 22 47
TRUE	USB2_EXCARD_N	6 22 47
TRUE	USB2_EXCARD_P	6 22 47
TRUE	PCIE_EXCARD_R2D_C_N	47 49
TRUE	PCIE_EXCARD_R2D_C_P	47 49
TRUE	PCIE_EXCARD_D2R_N	22 47 49
TRUE	PCIE_EXCARD_D2R_P	22 47 49
TRUE	PCIE_CLK100M_EXCARD_P	34 47
TRUE	PCIE_CLK100M_EXCARD_N	34 47
TRUE	USB2_LT2_N	6 22 47
TRUE	USB2_LT2_P	6 22 47
TRUE	PCIE_MINI_R2D_C_N	47 49
TRUE	PCIE_MINI_R2D_C_P	47 49
TRUE	PCIE_MINI_D2R_N	22 47 49
TRUE	PCIE_MINI_D2R_P	22 47 49
TRUE	PCIE_CLK100M_MINI_P	34 47
TRUE	PCIE_CLK100M_MINI_N	34 47
TRUE	SMBUS_SB_SCL	23 27 28 29 33 48 47
TRUE	SMBUS_SB_SDA	23 27 28 29 33 48 47
TRUE	PCIE_WAKE_L	23 39 47
TRUE	SMC_BC_ACOK	47 50 51 67 68

Left I/O Power Connector

FUNC_TEST		
TRUE	PP18V5_DCIN	67
TRUE	PP5V_S5	5 25 46 51 61 63 64 65 66 67 70
TRUE	PP5V_S0_AUDIO_PWR	67
TRUE	GND_AUDIO_PWR	67
TRUE	GND	

Request for at least 10 GND test points

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NC_CPU_A32_L	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_A32_L	7 6 → 6 7
NC_CPU_A33_L	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_A33_L	7 6 → 6 7
NC_CPU_A34_L	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_A34_L	7 6 → 6 7
NC_CPU_A35_L	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_A35_L	7 6 → 6 7
NC_CPU_A36_L	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_A36_L	7 6 → 6 7
NC_CPU_A37_L	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_A37_L	7 6 → 6 7
NC_CPU_A38_L	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_A38_L	7 6 → 6 7
NC_CPU_A39_L	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_A39_L	7 6 → 6 7
NC_CPU_APM0_L	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_APM0_L	7 6 → 6 7
NC_CPU_APM1_L	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_APM1_L	7 6 → 6 7
NC_CPU_EXTBREF	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_EXTBREF	7 6 → 6 7
NC_CPU_HFPLL	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_HFPLL	7 6 → 6 7
NC_CPU_SPARE0	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_SPARE0	7 6 → 6 7
NC_CPU_SPARE1	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_SPARE1	7 6 → 6 7
NC_CPU_SPARE2	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_SPARE2	7 6 → 6 7
NC_CPU_SPARE4	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_CPU_SPARE4	7 6 → 6 7

28 NC_MEM_A_A<15..14>	MAKE_BASE=TRUE, NO_TEST=TRUE	MEM_A_A<15..14>	
29 NC_MEM_B_A<15..14>	MAKE_BASE=TRUE, NO_TEST=TRUE	MEM_B_A<15..14>	
TP_NB_CFG<4..3>	MAKE_BASE=TRUE	NB_CFG<4..3>	14
TP_NB_CFG<6>	MAKE_BASE=TRUE	NB_CFG<6>	14
TP_NB_CFG<8>	MAKE_BASE=TRUE	NB_CFG<8>	14
TP_NB_CFG<11..10>	MAKE_BASE=TRUE	NB_CFG<11..10>	14
14 TP_NB_CFG<15..14>	MAKE_BASE=TRUE	NB_CFG<15..14>	14
TP_NB_CFG<17>	MAKE_BASE=TRUE	NB_CFG<17>	14

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12>	MAKE_BASE=TRUE	NB_CFG<13..12>	14
23 6 5 TP_SB_SUS_CLK	MAKE_BASE=TRUE	TP_SB_SUS_CLK	5 6 23

R0600
0
5%
1/16W
MF-LF
402

50 47 5 ALS_GAIN		RTALS_GAIN (MAKE_BASE=TRUE)	RTALS_GAIN 6 56
39 6 NC_ENET_CTRL12	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_ENET_CTRL12	6 39
39 6 NC_ENET_CTRL25	MAKE_BASE=TRUE, NO_TEST=TRUE	NC_ENET_CTRL25	6 39

Ethernet Powr Management Support

ENET_LOM_DISABLE

R0690
0
5%
1/16W
MF-LF
402

22 SB_GPIO30 — ENET_LOM_DIS_L 39

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOM_DISABLE" are mutually-exclusive.

USB Port "A" (Debug Port) = Right USB 2.0 Port

46 22 6 USB2_RT_P	46 22 6	USB2_RT_P (MAKE_BASE=TRUE)	USB2_RT_P 6 22 46
46 22 6 USB2_RT_N	46 22 6	USB2_RT_N (MAKE_BASE=TRUE)	USB2_RT_N 6 22 46
46 22 6 RTUSB_OC_L	46 22 6	RTUSB_OC_L (MAKE_BASE=TRUE)	RTUSB_OC_L 6 22 46

USB Port "B" = Trackpad (Geyser)

45 22 6 USB_TRACKPAD_P	45 22 6	USB_TRACKPAD_P (MAKE_BASE=TRUE)	USB_TRACKPAD_P 6 22 45
45 22 6 USB_TRACKPAD_N	45 22 6	USB_TRACKPAD_N (MAKE_BASE=TRUE)	USB_TRACKPAD_N 6 22 45
22 6 UNUSED_USB_B_OC_L (MAKE_BASE=TRUE)			UNUSED_USB_B_OC_L 6 22

USB Port "C" = Left USB 2.0 Port

47 22 6 5 USB2_LT_P	47 22 6 5	USB2_LT_P (MAKE_BASE=TRUE)	USB2_LT_P 5 6 22 47
47 22 6 5 USB2_LT_N	47 22 6 5	USB2_LT_N (MAKE_BASE=TRUE)	USB2_LT_N 5 6 22 47
47 22 6 5 LTUSB_OC_L (MAKE_BASE=TRUE)			LTUSB_OC_L 5 6 22 47

USB Port "D" = Camera

45 22 6 5 USB2_CAMERA_P	45 22 6 5	USB2_CAMERA_P (MAKE_BASE=TRUE)	USB2_CAMERA_P 5 6 22 45
45 22 6 5 USB2_CAMERA_N	45 22 6 5	USB2_CAMERA_N (MAKE_BASE=TRUE)	USB2_CAMERA_N 5 6 22 45
22 6 UNUSED_USB_D_OC_L (MAKE_BASE=TRUE)			UNUSED_USB_D_OC_L 6 22

USB Port "E" = ExpressCard

47 22 6 5 USB2_EXCARD_P	47 22 6 5	USB2_EXCARD_P (MAKE_BASE=TRUE)	USB2_EXCARD_P 5 6 22 47
47 22 6 5 USB2_EXCARD_N	47 22 6 5	USB2_EXCARD_N (MAKE_BASE=TRUE)	USB2_EXCARD_N 5 6 22 47
51 47 22 6 5 EXCARD_OC_L (MAKE_BASE=TRUE)			EXCARD_OC_L 5 6 22 47 51

USB Port "F" = IR Receiver

80 22 6 USB_IR_P	80 22 6	USB_IR_P (MAKE_BASE=TRUE)	USB_IR_P 6 22 80
80 22 6 USB_IR_N	80 22 6	USB_IR_N (MAKE_BASE=TRUE)	USB_IR_N 6 22 80

USB Port "G" = Bluetooth (M13P)

80 22 6 USB_BT_P	80 22 6	USB_BT_P (MAKE_BASE=TRUE)	USB_BT_P 6 22 80
80 22 6 USB_BT_N	80 22 6	USB_BT_N (MAKE_BASE=TRUE)	USB_BT_N 6 22 80

USB Port "H" = 2nd Left USB 2.0 Port

47 22 6 5 USB2_LT2_P	47 22 6 5	USB2_LT2_P (MAKE_BASE=TRUE)	USB2_LT2_P 5 6 22 47
47 22 6 5 USB2_LT2_N	47 22 6 5	USB2_LT2_N (MAKE_BASE=TRUE)	USB2_LT2_N 5 6 22 47

Chassis connection to be made at the fan cutout near the right ALS

SH0601
EMI-SPRING
0G-502620R

GND_CHASSIS_FANFRAME (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)

R0601
0
5%
1/16W
MF-LF
402

Chassis connection to be made at the mounting hole northwest of the DVI connector

ZT0600
HOLE-VIA-P5RP25

GND_CHASSIS_DVI_TOP (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)

- GND_CHASSIS_DVI_TOP 6 79
- GND_CHASSIS_DVI_TOP 6 79
- GND

Chassis connection to be made on FW shell

ZT0603
HOLE-VIA-P5RP25

GND_CHASSIS_DVI_BOT (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)

- GND_CHASSIS_DVI_BOT 6 40 44 79
- GND_CHASSIS_DVI_BOT 6 40 44 79
- GND_CHASSIS_DVI_BOT 6 40 44 79
- GND_CHASSIS_DVI_BOT 6 40 44 79
- GND_CHASSIS_DVI_BOT 6 40 44 79

Chassis connection to be made at the mounting hole southwest of the USB connector

ZT0601
HOLE-VIA-P5RP25

GND_CHASSIS_USB (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)

- GND_CHASSIS_USB 6 44 46
- GND_CHASSIS_USB 6 44 46
- GND_CHASSIS_USB 6 44 46

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602
HOLE-VIA-P5RP25

GND_CHASSIS_LVDS (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)

- GND_CHASSIS_LVDS 6 78
- GND_CHASSIS_LVDS 6 78
- GND_CHASSIS_LVDS 6 78
- GND_CHASSIS_LVDS 6 78

SH0600
OG-503040
SHLD-SM-LF

GND_CHASSIS_INVERTER (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE) — GND_CHASSIS_INVERTER 6 78

Signal Aliases

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/11/2005)

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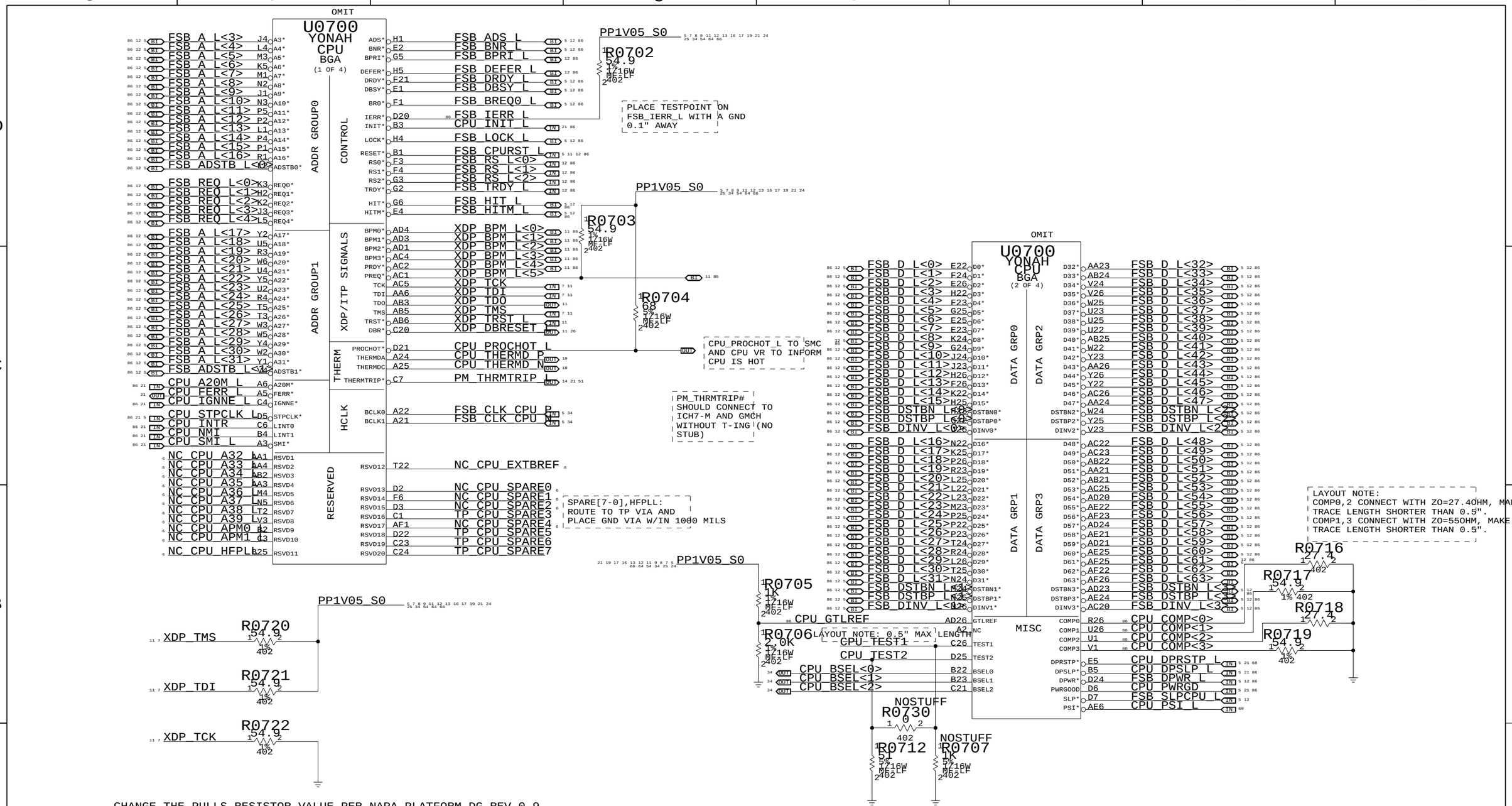

CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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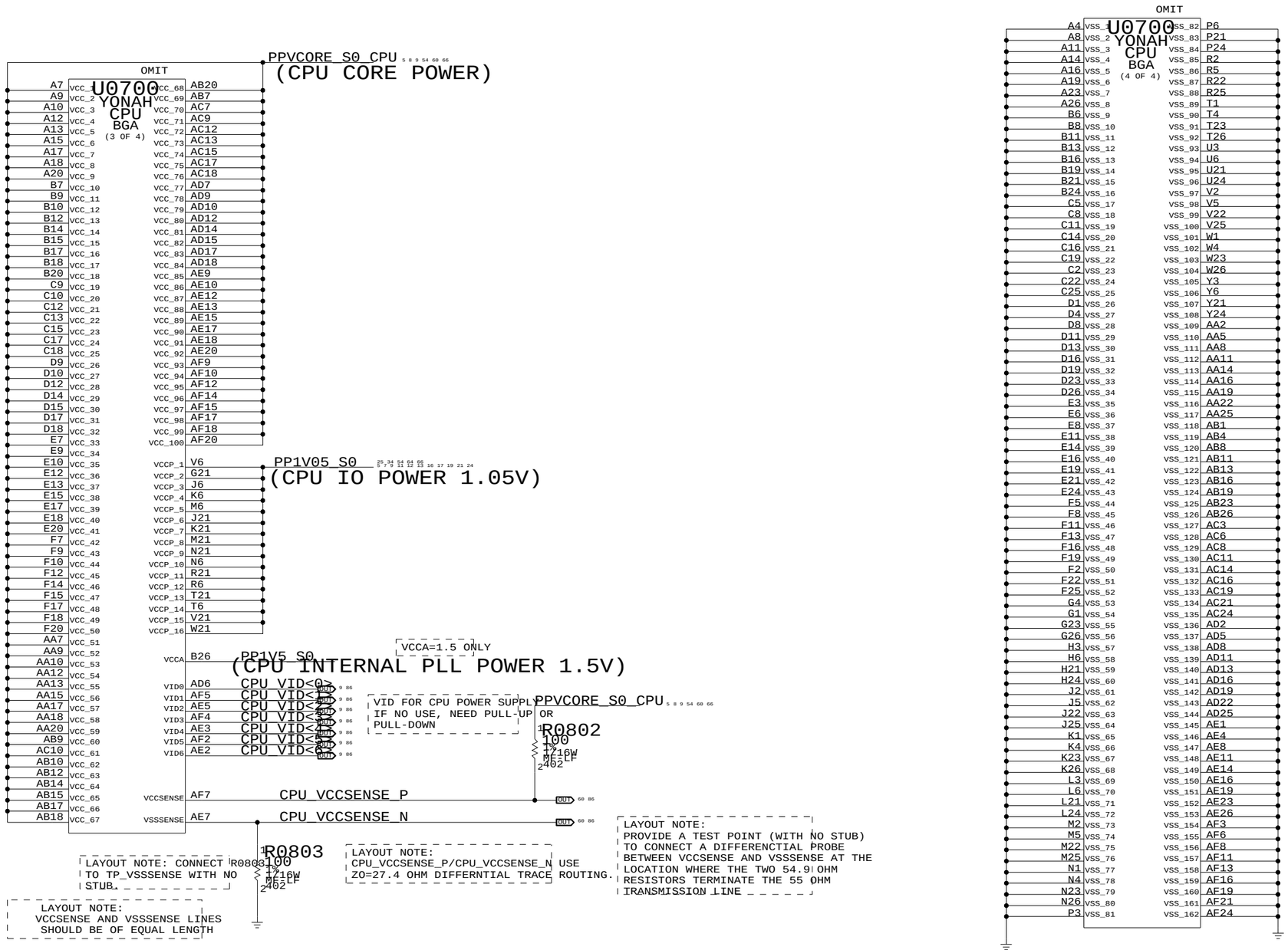
SCALE NONE SHT 7 OF 86



CPU 2 OF 2-PWR/GND

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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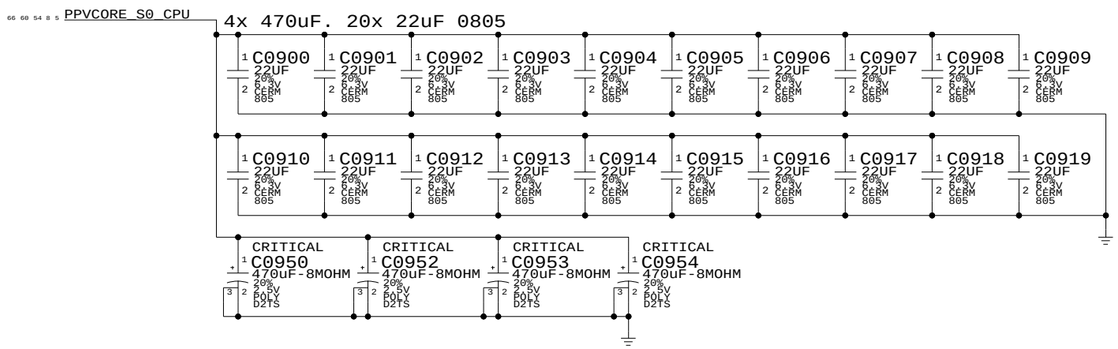
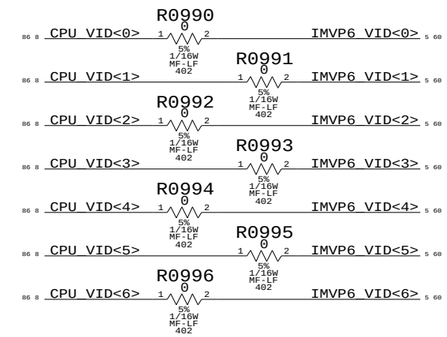
SCALE NONE	SHT 8 OF 86	

CPU VCORE HF AND BULK DECOUPLING

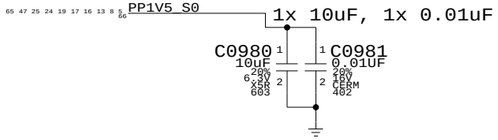


CPU VCORE VID Connections

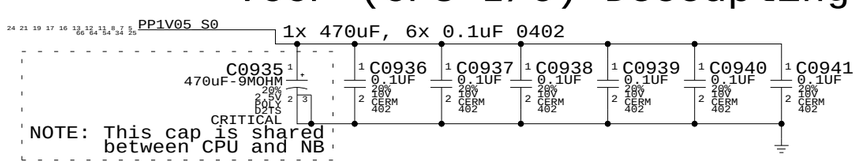
Resistors to allow for override of CPU VID
Will probably be removed before production



VCCA (CPU AVdd) Decoupling



VCCP (CPU I/O) Decoupling



CPU Decoupling & VID

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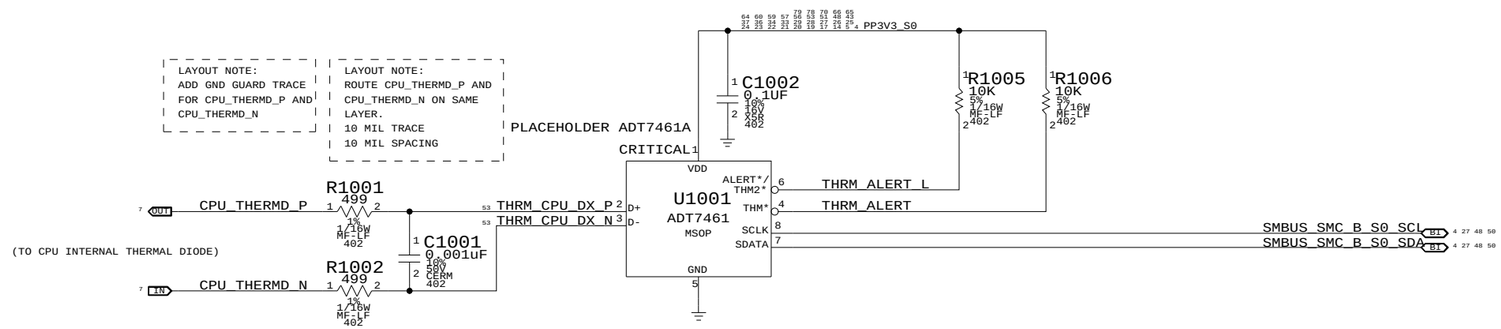
SCALE NONE	SHT 9 OF 86	

CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

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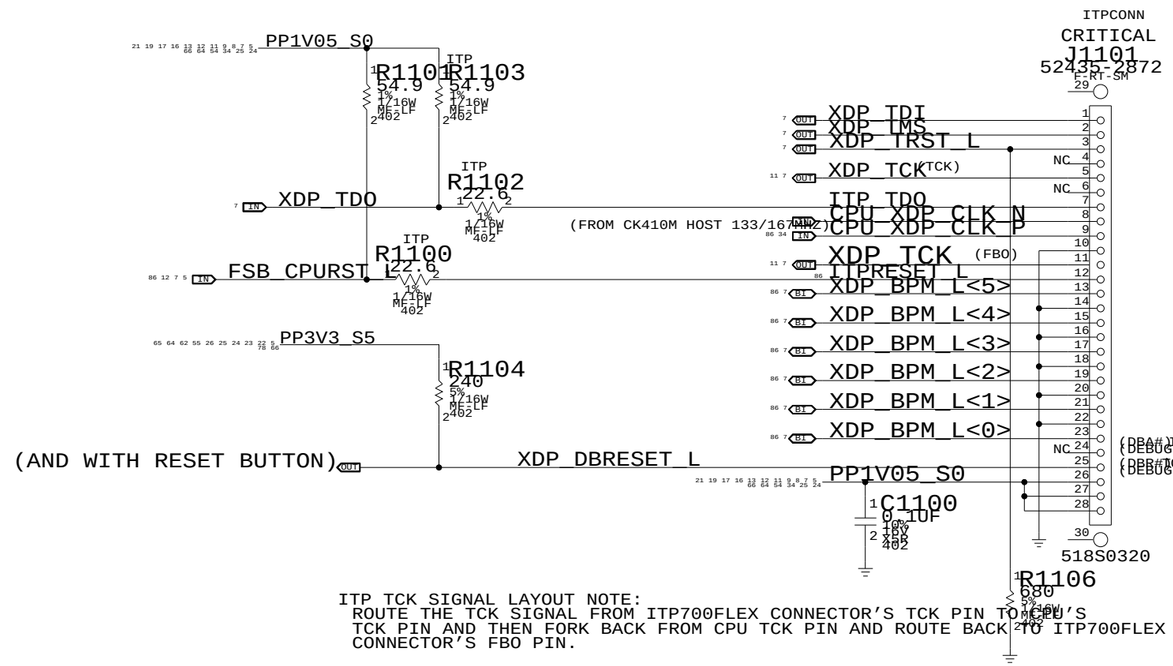
SCALE NONE

SHT 10 OF 86

CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=MSYNCB SYNC_DATE=02/10/2006

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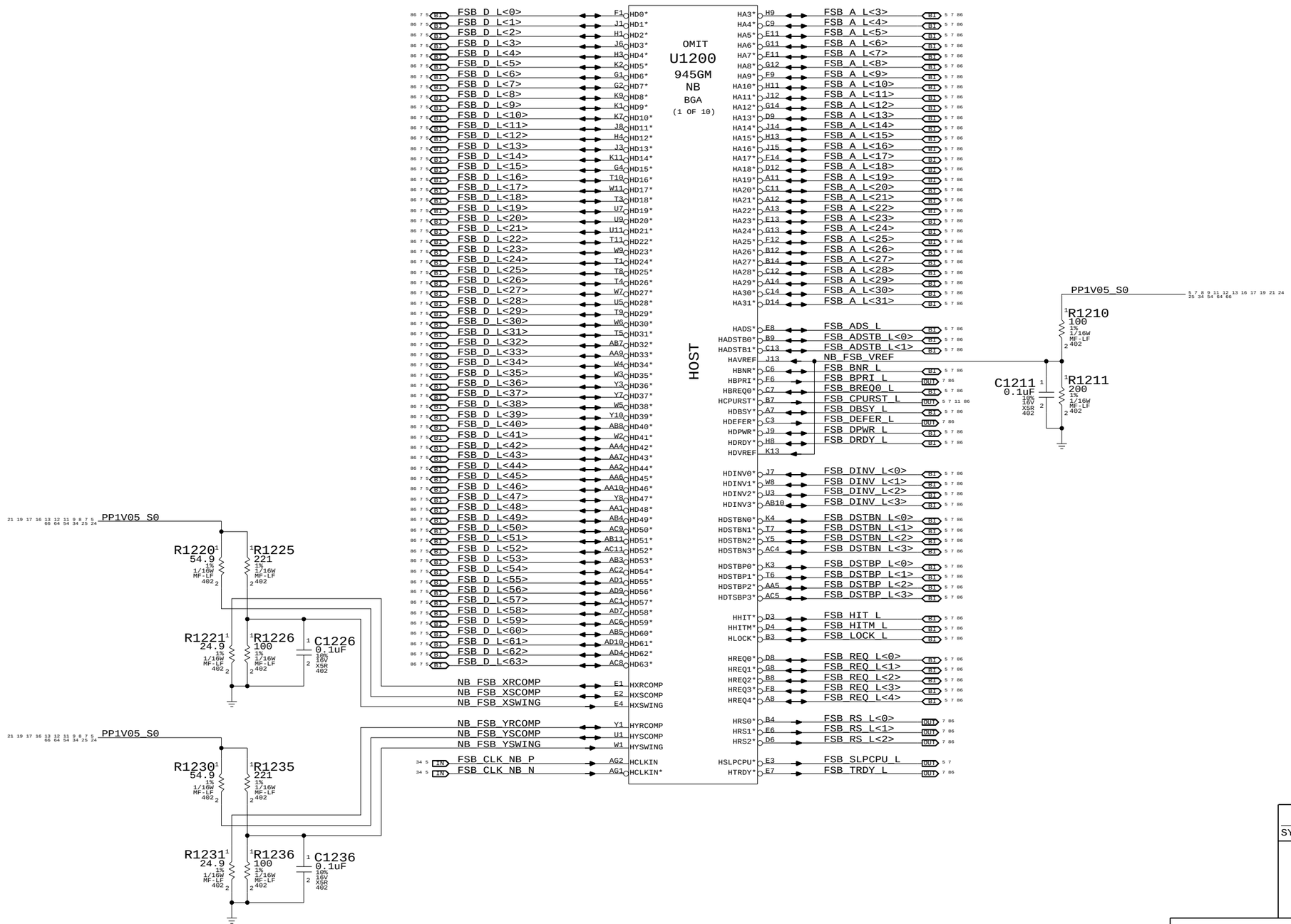

NB CPU Interface

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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

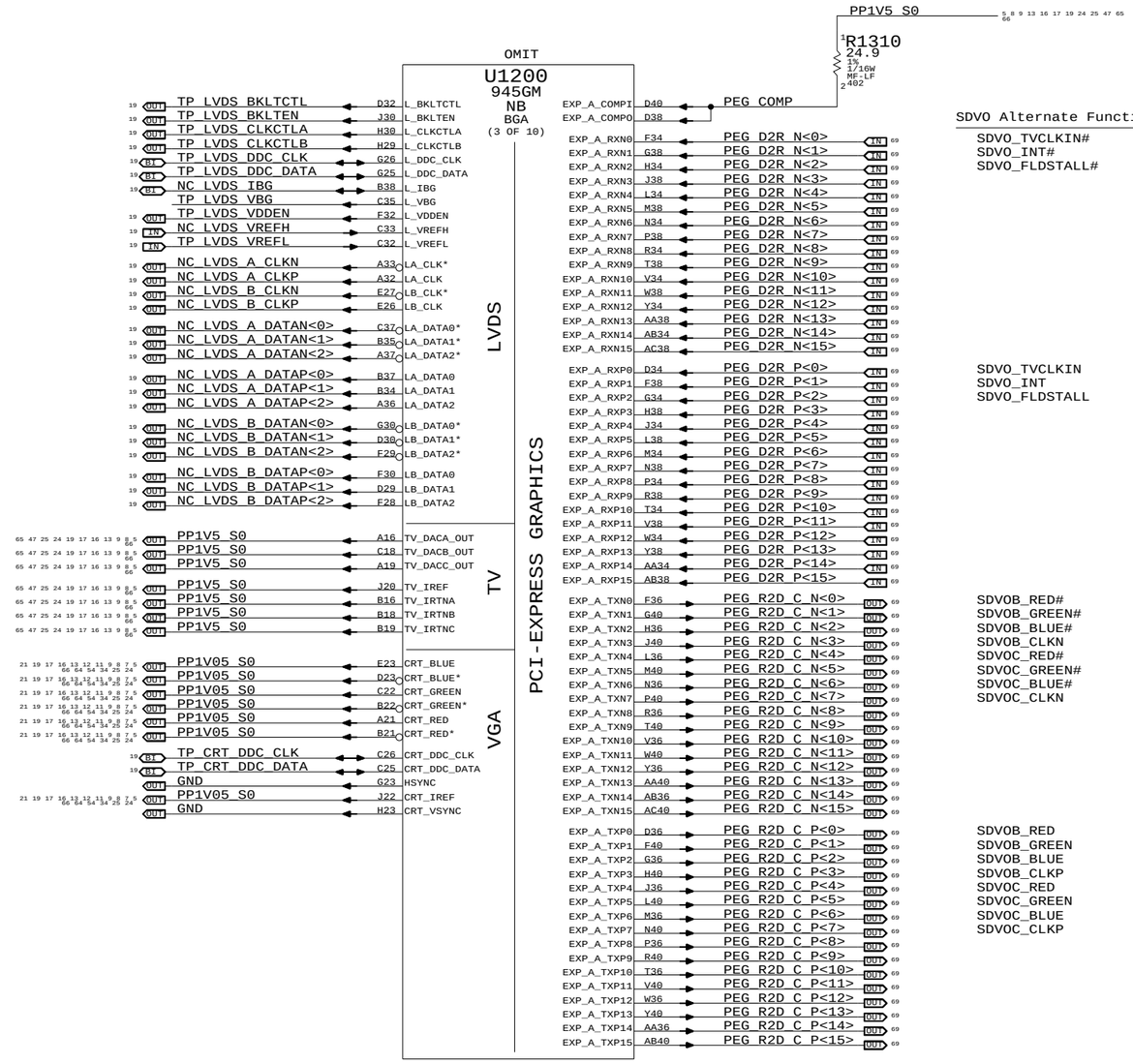
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



NB PEG / Video Interfaces

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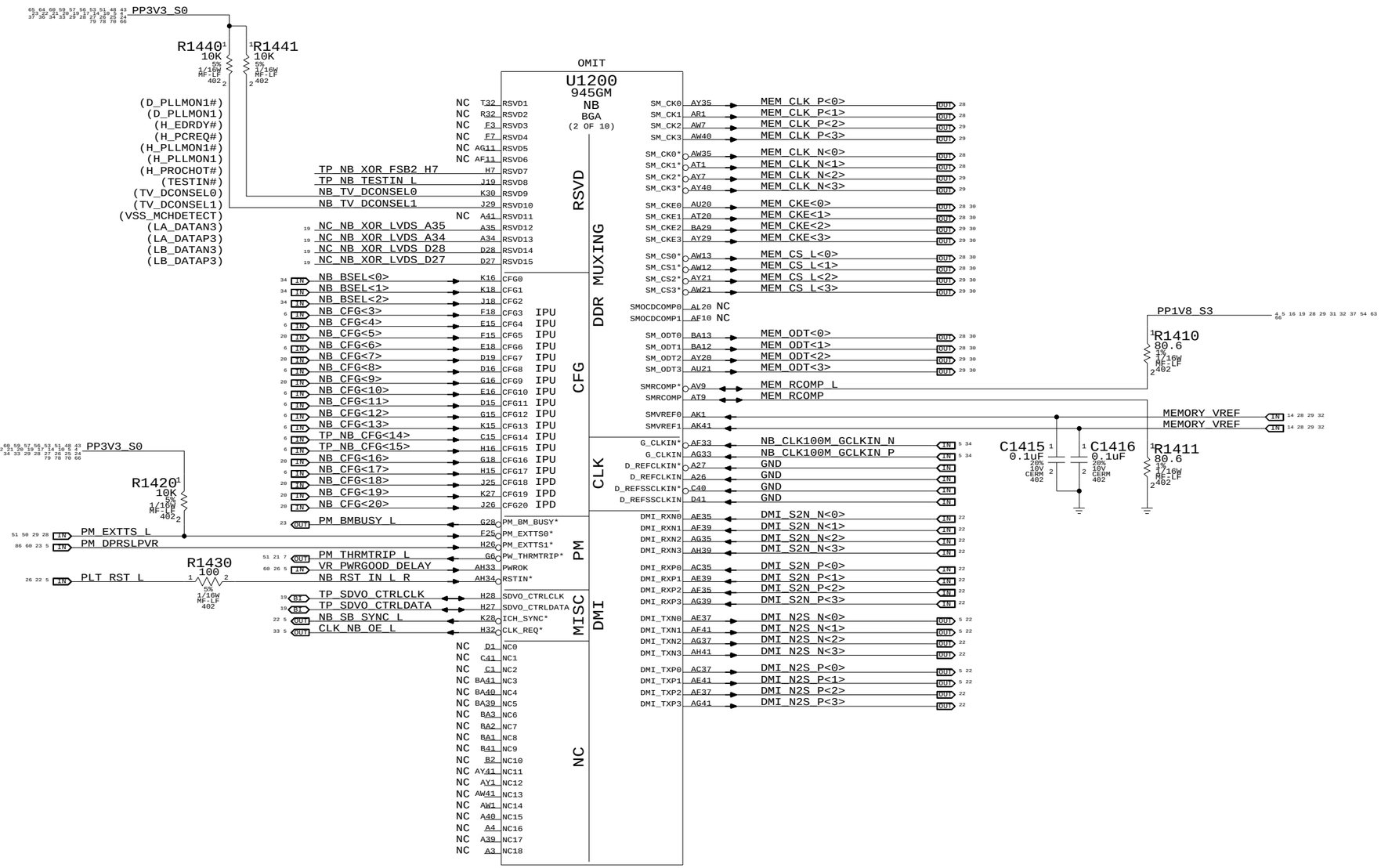
SCALE NONE



NB Misc Interfaces

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SIZE	DRAWING NUMBER	REV.
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SCALE NONE SHT 14 OF 86

OMIT

U1200
945GM
NB
BGA
(4 OF 10)

DDR SYSTEM MEMORY A

MEM_A_DQ<0>	AJ35	SA_DQ0	
MEM_A_DQ<1>	AJ34	SA_DQ1	
MEM_A_DQ<2>	AM31	SA_DQ2	
MEM_A_DQ<3>	AM33	SA_DQ3	
MEM_A_DQ<4>	AJ36	SA_DQ4	
MEM_A_DQ<5>	AK35	SA_DQ5	
MEM_A_DQ<6>	AJ32	SA_DQ6	
MEM_A_DQ<7>	AH31	SA_DQ7	
MEM_A_DQ<8>	AN35	SA_DQ8	
MEM_A_DQ<9>	AP33	SA_DQ9	
MEM_A_DQ<10>	AR31	SA_DQ10	
MEM_A_DQ<11>	AP31	SA_DQ11	
MEM_A_DQ<12>	AN38	SA_DQ12	
MEM_A_DQ<13>	AM36	SA_DQ13	
MEM_A_DQ<14>	AM34	SA_DQ14	
MEM_A_DQ<15>	AN33	SA_DQ15	
MEM_A_DQ<16>	AK26	SA_DQ16	
MEM_A_DQ<17>	AL27	SA_DQ17	
MEM_A_DQ<18>	AM26	SA_DQ18	
MEM_A_DQ<19>	AN24	SA_DQ19	
MEM_A_DQ<20>	AK28	SA_DQ20	
MEM_A_DQ<21>	AL28	SA_DQ21	
MEM_A_DQ<22>	AM24	SA_DQ22	
MEM_A_DQ<23>	AP26	SA_DQ23	
MEM_A_DQ<24>	AP23	SA_DQ24	
MEM_A_DQ<25>	AL22	SA_DQ25	
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MEM_A_DQ<33>	AR14	SA_DQ33	
MEM_A_DQ<34>	AP13	SA_DQ34	
MEM_A_DQ<35>	AP12	SA_DQ35	
MEM_A_DQ<36>	AT13	SA_DQ36	
MEM_A_DQ<37>	AT12	SA_DQ37	
MEM_A_DQ<38>	AL14	SA_DQ38	
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MEM_A_DQ<40>	AK9	SA_DQ40	
MEM_A_DQ<41>	AN7	SA_DQ41	
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MEM_A_DQ<58>	AG4	SA_DQ58	
MEM_A_DQ<59>	AF6	SA_DQ59	
MEM_A_DQ<60>	AG9	SA_DQ60	
MEM_A_DQ<61>	AH6	SA_DQ61	
MEM_A_DQ<62>	AF4	SA_DQ62	
MEM_A_DQ<63>	AF8	SA_DQ63	

SA_BS0	AU12	MEM_A_BS<0>	OUT
SA_BS1	AV14	MEM_A_BS<1>	OUT
SA_BS2	BA20	MEM_A_BS<2>	OUT
SA_CAS*	AY13	MEM_A_CAS_L	OUT
SA_DM0	AJ33	MEM_A_DM<0>	OUT
SA_DM1	AM35	MEM_A_DM<1>	OUT
SA_DM2	AL26	MEM_A_DM<2>	OUT
SA_DM3	AN22	MEM_A_DM<3>	OUT
SA_DM4	AM14	MEM_A_DM<4>	OUT
SA_DM5	AL9	MEM_A_DM<5>	OUT
SA_DM6	AR3	MEM_A_DM<6>	OUT
SA_DM7	AH4	MEM_A_DM<7>	OUT
SA_DQS0	AK33	MEM_A_DQS_P<0>	BI
SA_DQS1	AT33	MEM_A_DQS_P<1>	BI
SA_DQS2	AN28	MEM_A_DQS_P<2>	BI
SA_DQS3	AM22	MEM_A_DQS_P<3>	BI
SA_DQS4	AN12	MEM_A_DQS_P<4>	BI
SA_DQS5	AN8	MEM_A_DQS_P<5>	BI
SA_DQS6	AP3	MEM_A_DQS_P<6>	BI
SA_DQS7	AG5	MEM_A_DQS_P<7>	BI
SA_DQS0*	AK32	MEM_A_DQS_N<0>	BI
SA_DQS1*	AU33	MEM_A_DQS_N<1>	BI
SA_DQS2*	AN27	MEM_A_DQS_N<2>	BI
SA_DQS3*	AM21	MEM_A_DQS_N<3>	BI
SA_DQS4*	AM12	MEM_A_DQS_N<4>	BI
SA_DQS5*	AL8	MEM_A_DQS_N<5>	BI
SA_DQS6*	AN3	MEM_A_DQS_N<6>	BI
SA_DQS7*	AH5	MEM_A_DQS_N<7>	BI
SA_MA0	AY16	MEM_A_A<0>	OUT
SA_MA1	AU14	MEM_A_A<1>	OUT
SA_MA2	AW16	MEM_A_A<2>	OUT
SA_MA3	BA16	MEM_A_A<3>	OUT
SA_MA4	BA17	MEM_A_A<4>	OUT
SA_MA5	AU16	MEM_A_A<5>	OUT
SA_MA6	AV17	MEM_A_A<6>	OUT
SA_MA7	AU17	MEM_A_A<7>	OUT
SA_MA8	AW17	MEM_A_A<8>	OUT
SA_MA9	AT16	MEM_A_A<9>	OUT
SA_MA10	AU13	MEM_A_A<10>	OUT
SA_MA11	AT17	MEM_A_A<11>	OUT
SA_MA12	AV20	MEM_A_A<12>	OUT
SA_MA13	AV12	MEM_A_A<13>	OUT
SA_RAS*	AW14	MEM_A_RAS_L	OUT
SA_RCVENIN*	AK23	NC	
SA_RCVENOUT*	AK24	NC	
SA_WE*	AY14	MEM_A_WE_L	OUT

OMIT

U1200
945GM
NB
BGA
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DDR SYSTEM MEMORY B

MEM_B_DQ<0>	AK39	SB_DQ0	
MEM_B_DQ<1>	AJ37	SB_DQ1	
MEM_B_DQ<2>	AP39	SB_DQ2	
MEM_B_DQ<3>	AR41	SB_DQ3	
MEM_B_DQ<4>	AJ38	SB_DQ4	
MEM_B_DQ<5>	AK38	SB_DQ5	
MEM_B_DQ<6>	AN41	SB_DQ6	
MEM_B_DQ<7>	AP41	SB_DQ7	
MEM_B_DQ<8>	AT40	SB_DQ8	
MEM_B_DQ<9>	AV41	SB_DQ9	
MEM_B_DQ<10>	AU38	SB_DQ10	
MEM_B_DQ<11>	AV38	SB_DQ11	
MEM_B_DQ<12>	AP38	SB_DQ12	
MEM_B_DQ<13>	AR40	SB_DQ13	
MEM_B_DQ<14>	AW38	SB_DQ14	
MEM_B_DQ<15>	AY38	SB_DQ15	
MEM_B_DQ<16>	BA38	SB_DQ16	
MEM_B_DQ<17>	AV36	SB_DQ17	
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MEM_B_DQ<23>	AP34	SB_DQ23	
MEM_B_DQ<24>	AY33	SB_DQ24	
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MEM_B_DQ<27>	AU29	SB_DQ27	
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MEM_B_DQ<29>	AW31	SB_DQ29	
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MEM_B_DQ<60>	AT4	SB_DQ60	
MEM_B_DQ<61>	AK5	SB_DQ61	
MEM_B_DQ<62>	AJ5	SB_DQ62	
MEM_B_DQ<63>	AJ3	SB_DQ63	

SB_BS0	AT24	MEM_B_BS<0>	OUT
SB_BS1	AV23	MEM_B_BS<1>	OUT
SB_BS2	AY28	MEM_B_BS<2>	OUT
SB_CAS*	AR24	MEM_B_CAS_L	OUT
SB_DM0	AK36	MEM_B_DM<0>	OUT
SB_DM1	AR38	MEM_B_DM<1>	OUT
SB_DM2	AT36	MEM_B_DM<2>	OUT
SB_DM3	BA31	MEM_B_DM<3>	OUT
SB_DM4	AL17	MEM_B_DM<4>	OUT
SB_DM5	AH8	MEM_B_DM<5>	OUT
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SB_DQS0	AM39	MEM_B_DQS_P<0>	BI
SB_DQS1	AT39	MEM_B_DQS_P<1>	BI
SB_DQS2	AU35	MEM_B_DQS_P<2>	BI
SB_DQS3	AR29	MEM_B_DQS_P<3>	BI
SB_DQS4	AR16	MEM_B_DQS_P<4>	BI
SB_DQS5	AR10	MEM_B_DQS_P<5>	BI
SB_DQS6	AR7	MEM_B_DQS_P<6>	BI
SB_DQS7	AN5	MEM_B_DQS_P<7>	BI
SB_DQS0*	AM40	MEM_B_DQS_N<0>	BI
SB_DQS1*	AU39	MEM_B_DQS_N<1>	BI
SB_DQS2*	AT35	MEM_B_DQS_N<2>	BI
SB_DQS3*	AP29	MEM_B_DQS_N<3>	BI
SB_DQS4*	AP16	MEM_B_DQS_N<4>	BI
SB_DQS5*	AT10	MEM_B_DQS_N<5>	BI
SB_DQS6*	AT7	MEM_B_DQS_N<6>	BI
SB_DQS7*	AP5	MEM_B_DQS_N<7>	BI
SB_MA0	AY23	MEM_B_A<0>	OUT
SB_MA1	AW24	MEM_B_A<1>	OUT
SB_MA2	AY24	MEM_B_A<2>	OUT
SB_MA3	AR28	MEM_B_A<3>	OUT
SB_MA4	AT27	MEM_B_A<4>	OUT
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SB_MA7	AV28	MEM_B_A<7>	OUT
SB_MA8	AV27	MEM_B_A<8>	OUT
SB_MA9	AW27	MEM_B_A<9>	OUT
SB_MA10	AV24	MEM_B_A<10>	OUT
SB_MA11	BA27	MEM_B_A<11>	OUT
SB_MA12	AY27	MEM_B_A<12>	OUT
SB_MA13	AR23	MEM_B_A<13>	OUT
SB_RAS*	AU23	MEM_B_RAS_L	OUT
SB_RCVENIN*	AK16	NC	
SB_RCVENOUT*	AK18	NC	
SB_WE*	AR27	MEM_B_WE_L	OUT

NB DDR2 Interfaces

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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D	051-7023	06

SCALE NONE

SHT 15 OF 86

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

OMIT

PP1V05_S0 (21 19 17 16 13 12 11 9 8 7 5 / 66 64 54 34 25 24)

U1200 945GM NB BGA (7 OF 10) NCTF

AD27	VCC_NCTF0	VSS_NCTF0	AE27
AC27	VCC_NCTF1	VSS_NCTF1	AE26
AB27	VCC_NCTF2	VSS_NCTF2	AE25
AA27	VCC_NCTF3	VSS_NCTF3	AE24
Y27	VCC_NCTF4	VSS_NCTF4	AE23
W27	VCC_NCTF5	VSS_NCTF5	AE22
V27	VCC_NCTF6	VSS_NCTF6	AE21
U27	VCC_NCTF7	VSS_NCTF7	AE20
T27	VCC_NCTF8	VSS_NCTF8	AE19
R27	VCC_NCTF9	VSS_NCTF9	AE18
AD26	VCC_NCTF10	VSS_NCTF10	AC17
AC26	VCC_NCTF11	VSS_NCTF11	Y17
AB26	VCC_NCTF12	VSS_NCTF12	U17
AA26	VCC_NCTF13		
Y26	VCC_NCTF14		
W26	VCC_NCTF15		
V26	VCC_NCTF16		
U26	VCC_NCTF17		
T26	VCC_NCTF18		
R26	VCC_NCTF19		
AD25	VCC_NCTF20		
AC25	VCC_NCTF21		
AB25	VCC_NCTF22		
AA25	VCC_NCTF23		
Y25	VCC_NCTF24		
W25	VCC_NCTF25		
V25	VCC_NCTF26		
U25	VCC_NCTF27		
T25	VCC_NCTF28		
R25	VCC_NCTF29		
AD24	VCC_NCTF30		
AC24	VCC_NCTF31		
AB24	VCC_NCTF32		
AA24	VCC_NCTF33		
Y24	VCC_NCTF34		
W24	VCC_NCTF35		
V24	VCC_NCTF36		
U24	VCC_NCTF37		
T24	VCC_NCTF38		
R24	VCC_NCTF39		
AD23	VCC_NCTF40		
V23	VCC_NCTF41		
U23	VCC_NCTF42		
T23	VCC_NCTF43		
R23	VCC_NCTF44		
AD22	VCC_NCTF45		
V22	VCC_NCTF46		
U22	VCC_NCTF47		
T22	VCC_NCTF48		
R22	VCC_NCTF49		
AD21	VCC_NCTF50		
V21	VCC_NCTF51		
U21	VCC_NCTF52		
T21	VCC_NCTF53		
R21	VCC_NCTF54		
AD20	VCC_NCTF55		
V20	VCC_NCTF56		
U20	VCC_NCTF57		
T20	VCC_NCTF58		
R20	VCC_NCTF59		
AD19	VCC_NCTF60		
V19	VCC_NCTF61		
U19	VCC_NCTF62		
T19	VCC_NCTF63		
AD18	VCC_NCTF64		
AC18	VCC_NCTF65		
AB18	VCC_NCTF66		
AA18	VCC_NCTF67		
Y18	VCC_NCTF68		
W18	VCC_NCTF69		
V18	VCC_NCTF70		
U18	VCC_NCTF71		
T18	VCC_NCTF72		

PP1V5_S0 (25 47 65 / 5 9 9 13 / 17 19 24 / 66)

		VCCAUX_NCTF0	AG27
		VCCAUX_NCTF1	AF27
		VCCAUX_NCTF2	AG26
		VCCAUX_NCTF3	AF26
		VCCAUX_NCTF4	AG25
		VCCAUX_NCTF5	AF25
		VCCAUX_NCTF6	AG24
		VCCAUX_NCTF7	AF24
		VCCAUX_NCTF8	AG23
		VCCAUX_NCTF9	AF23
		VCCAUX_NCTF10	AG22
		VCCAUX_NCTF11	AF22
		VCCAUX_NCTF12	AG21
		VCCAUX_NCTF13	AF21
		VCCAUX_NCTF14	AG20
		VCCAUX_NCTF15	AF20
		VCCAUX_NCTF16	AG19
		VCCAUX_NCTF17	AF19
		VCCAUX_NCTF18	R19
		VCCAUX_NCTF19	AG18
		VCCAUX_NCTF20	AF18
		VCCAUX_NCTF21	R18
		VCCAUX_NCTF22	AG17
		VCCAUX_NCTF23	AF17
		VCCAUX_NCTF24	AE17
		VCCAUX_NCTF25	AD17
		VCCAUX_NCTF26	AB17
		VCCAUX_NCTF27	AA17
		VCCAUX_NCTF28	W17
		VCCAUX_NCTF29	V17
		VCCAUX_NCTF30	T17
		VCCAUX_NCTF31	R17
		VCCAUX_NCTF32	AG16
		VCCAUX_NCTF33	AF16
		VCCAUX_NCTF34	AE16
		VCCAUX_NCTF35	AD16
		VCCAUX_NCTF36	AC16
		VCCAUX_NCTF37	AB16
		VCCAUX_NCTF38	AA16
		VCCAUX_NCTF39	Y16
		VCCAUX_NCTF40	W16
		VCCAUX_NCTF41	V16
		VCCAUX_NCTF42	U16
		VCCAUX_NCTF43	T16
		VCCAUX_NCTF44	R16
		VCCAUX_NCTF45	AG15
		VCCAUX_NCTF46	AF15
		VCCAUX_NCTF47	AE15
		VCCAUX_NCTF48	AD15
		VCCAUX_NCTF49	AC15
		VCCAUX_NCTF50	AB15
		VCCAUX_NCTF51	AA15
		VCCAUX_NCTF52	Y15
		VCCAUX_NCTF53	W15
		VCCAUX_NCTF54	V15
		VCCAUX_NCTF55	U15
		VCCAUX_NCTF56	T15
		VCCAUX_NCTF57	R15

1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.5V, Internal Graphics: 5500mA Max

PP1V05_S0 (64,66 / 17 9 8 11 12 13 16 / 17 19 21 24 29 34 54)

1.05V or 1.5V

U1200 945GM NB BGA (6 OF 10) OMIT VCC

AU41	VCC_SM0	VCC_0	AA33
AT41	VCC_SM1	VCC_1	W33
AM41	VCC_SM2	VCC_2	P33
AU40	VCC_SM3	VCC_3	N33
BA34	VCC_SM4	VCC_4	L33
AY34	VCC_SM5	VCC_5	J33
AW34	VCC_SM6	VCC_6	AA32
AV34	VCC_SM7	VCC_7	Y32
AU34	VCC_SM8	VCC_8	W32
AT34	VCC_SM9	VCC_9	V32
AR34	VCC_SM10	VCC_10	P32
BA30	VCC_SM11	VCC_11	N32
AY30	VCC_SM12	VCC_12	M32
AW30	VCC_SM13	VCC_13	L32
AV30	VCC_SM14	VCC_14	J32
AU30	VCC_SM15	VCC_15	AA31
AT30	VCC_SM16	VCC_16	W31
AR30	VCC_SM17	VCC_17	V31
AP30	VCC_SM18	VCC_18	T31
AN30	VCC_SM19	VCC_19	R31
AM30	VCC_SM20	VCC_20	P31
AM29	VCC_SM21	VCC_21	N31
AL29	VCC_SM22	VCC_22	M31
AK29	VCC_SM23	VCC_23	AA30
AJ29	VCC_SM24	VCC_24	Y30
AH29	VCC_SM25	VCC_25	W30
AJ28	VCC_SM26	VCC_26	V30
AH28	VCC_SM27	VCC_27	U30
AJ27	VCC_SM28	VCC_28	T30
AH27	VCC_SM29	VCC_29	R30
BA26	VCC_SM30	VCC_30	P30
AY26	VCC_SM31	VCC_31	N30
AW26	VCC_SM32	VCC_32	L30
AV26	VCC_SM33	VCC_33	AA29
AU26	VCC_SM34	VCC_34	Y29
AT26	VCC_SM35	VCC_35	W29
AR26	VCC_SM36	VCC_36	V29
AJ26	VCC_SM37	VCC_37	U29
AH26	VCC_SM38	VCC_38	P29
AJ25	VCC_SM39	VCC_39	R29
AH25	VCC_SM40	VCC_40	P29
AJ24	VCC_SM41	VCC_41	N29
AH24	VCC_SM42	VCC_42	L29
BA23	VCC_SM43	VCC_43	AB28
AJ23	VCC_SM44	VCC_44	AA28
BA22	VCC_SM45	VCC_45	Y28
AY22	VCC_SM46	VCC_46	V28
AW22	VCC_SM47	VCC_47	U28
AV22	VCC_SM48	VCC_48	T28
AU22	VCC_SM49	VCC_49	R28
AT22	VCC_SM50	VCC_50	P28
AR22	VCC_SM51	VCC_51	N28
AP22	VCC_SM52	VCC_52	M28
AK22	VCC_SM53	VCC_53	L28
AJ22	VCC_SM54	VCC_54	P27
AK21	VCC_SM55	VCC_55	N27
AK20	VCC_SM56	VCC_56	M27
BA19	VCC_SM57	VCC_57	L27
AY19	VCC_SM58	VCC_58	P26
AW19	VCC_SM59	VCC_59	N26
AV19	VCC_SM60	VCC_60	L26
AU19	VCC_SM61	VCC_61	M25
AT19	VCC_SM62	VCC_62	L25
AR19	VCC_SM63	VCC_63	P24
AP19	VCC_SM64	VCC_64	N24
AK19	VCC_SM65	VCC_65	M24
AJ19	VCC_SM66	VCC_66	AB23
AJ18	VCC_SM67	VCC_67	AA23
AH17	VCC_SM68	VCC_68	Y23
AJ16	VCC_SM69	VCC_69	P23
AH16	VCC_SM70	VCC_70	N23
BA15	VCC_SM71	VCC_71	M23
AY15	VCC_SM72	VCC_72	L23
AW15	VCC_SM73	VCC_73	AC22
AV15	VCC_SM74	VCC_74	AB22
AU15	VCC_SM75	VCC_75	AA22
AT15	VCC_SM76	VCC_76	Y22
AR15	VCC_SM77	VCC_77	W22
AJ15	VCC_SM78	VCC_78	P22
AJ14	VCC_SM79	VCC_79	N22
AJ13	VCC_SM80	VCC_80	M22
AH13	VCC_SM81	VCC_81	L22
AK12	VCC_SM82	VCC_82	AC21
AJ12	VCC_SM83	VCC_83	AA21
AH12	VCC_SM84	VCC_84	W21
AG12	VCC_SM85	VCC_85	N21
AK11	VCC_SM86	VCC_86	M21
BA8	VCC_SM87	VCC_87	L21
AY8	VCC_SM88	VCC_88	AC20
AW8	VCC_SM89	VCC_89	AB20
AV8	VCC_SM90	VCC_90	Y20
AU8	VCC_SM91	VCC_91	W20
AT8	VCC_SM92	VCC_92	P20
AR8	VCC_SM93	VCC_93	N20
AP8	VCC_SM94	VCC_94	L20
BA6	VCC_SM95	VCC_95	AB19
AW6	VCC_SM96	VCC_96	AA19
AV6	VCC_SM97	VCC_97	Y19
AU6	VCC_SM98	VCC_98	W19
AT6	VCC_SM99	VCC_99	N19
AR6	VCC_SM100	VCC_100	L19
AP6	VCC_SM101	VCC_101	N18
AN6	VCC_SM102	VCC_102	M18
AK6	VCC_SM103	VCC_103	L18
AJ6	VCC_SM104	VCC_104	P17
AV1	VCC_SM105	VCC_105	N17
AJ1	VCC_SM106	VCC_106	M17
	VCC_SM107	VCC_107	N16
		VCC_108	M16
		VCC_109	L16
		VCC_110	L16

1.8V Max Current

Speed	1 Channel	2 Channel
400MTs	1300mA	2400mA
533MTs	1500mA	2800mA
667MTs	1700mA	3200mA

NB_VCCSM_LF4
NB_VCCSM_LF5

C1614 0.47uF 20% 6.3V CERM-X5R 402 (1 – 2)

C1613 0.47uF 20% 6.3V CERM-X5R 402 (1 – 2)

C1615 0.47uF 20% 6.3V CERM-X5R 402 (1 – 2)
PP1V8_S3 (66 63 54 37 / 19 14 6 2 / 32 31 29 28)
Layout Note: Place near pin BA23

C1620 10uF 20% 6.3V X5R 603 (1 – 2)

C1621 10uF 20% 6.3V X5R 603 (1 – 2)

Layout Note: Place in cavity

C1610 0.47uF 20% 6.3V CERM-X5R 402 (1 – 2)
Layout Note: Place near pin BA15

C1612 0.47uF 20% 6.3V CERM-X5R 402 (1 – 2)

C1611 0.47uF 20% 6.3V CERM-X5R 402 (1 – 2)

NB_VCCSM_LF2
NB_VCCSM_LF1

NB Power 1

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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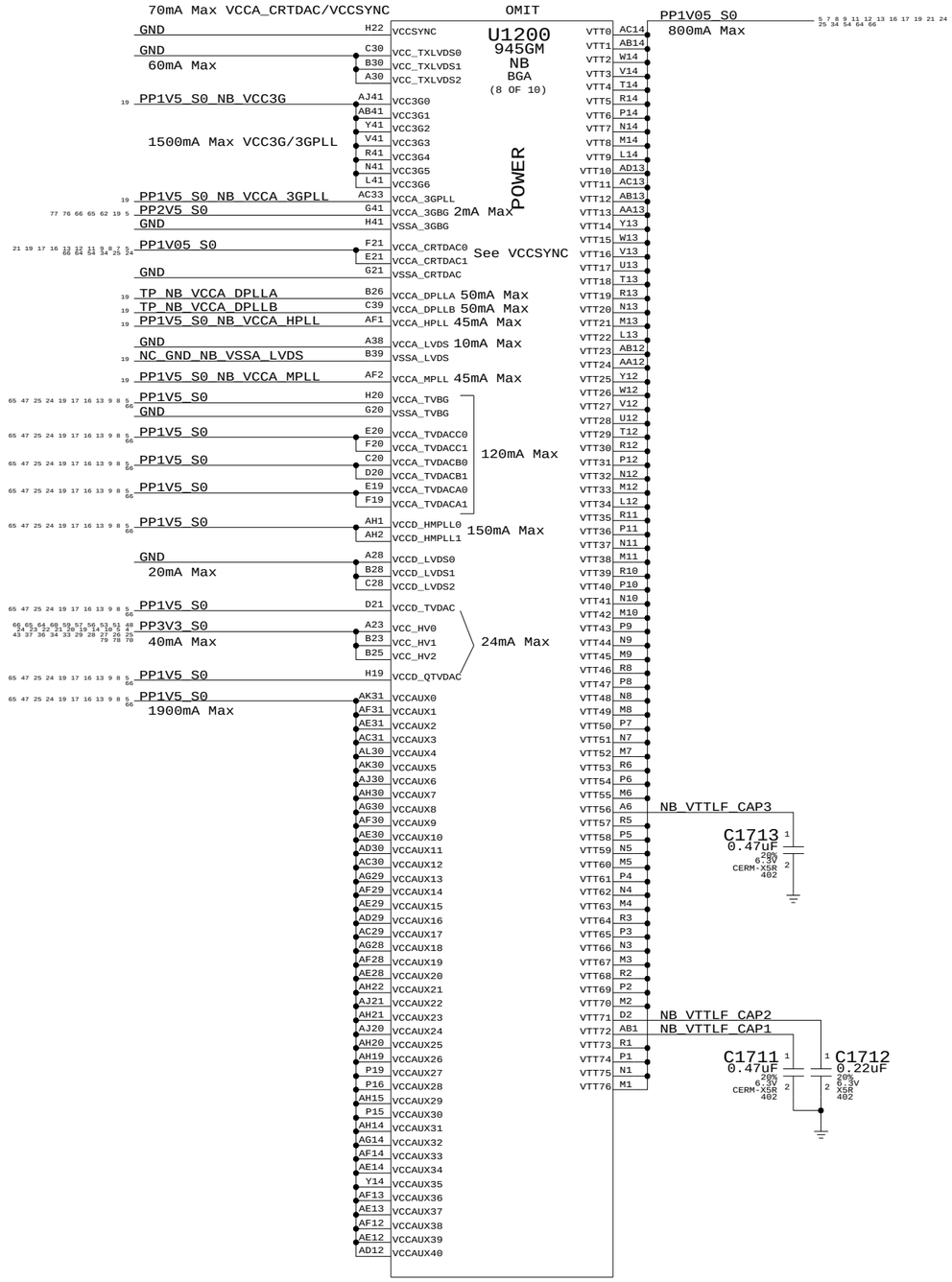
SIZE	DRAWING NUMBER	REV.
D	051-7023	06

SCALE NONE SHT 16 OF 86



NB Power 2

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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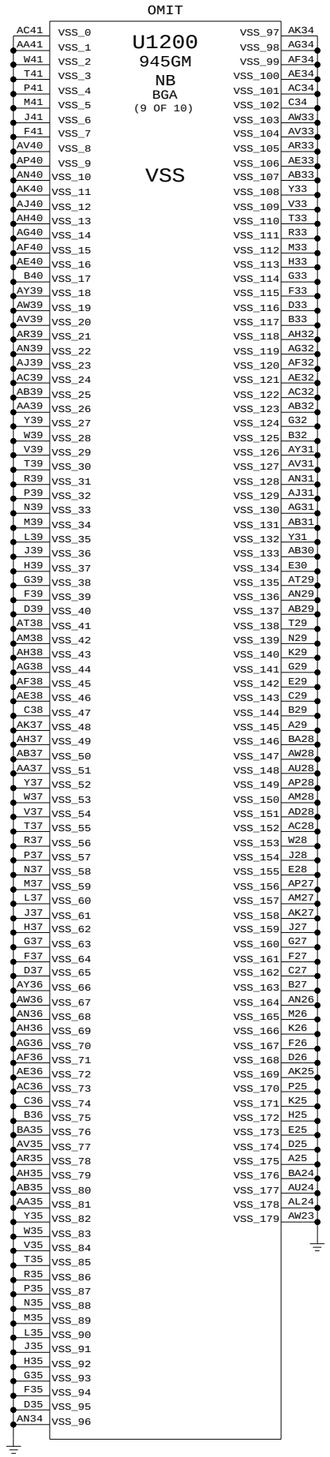
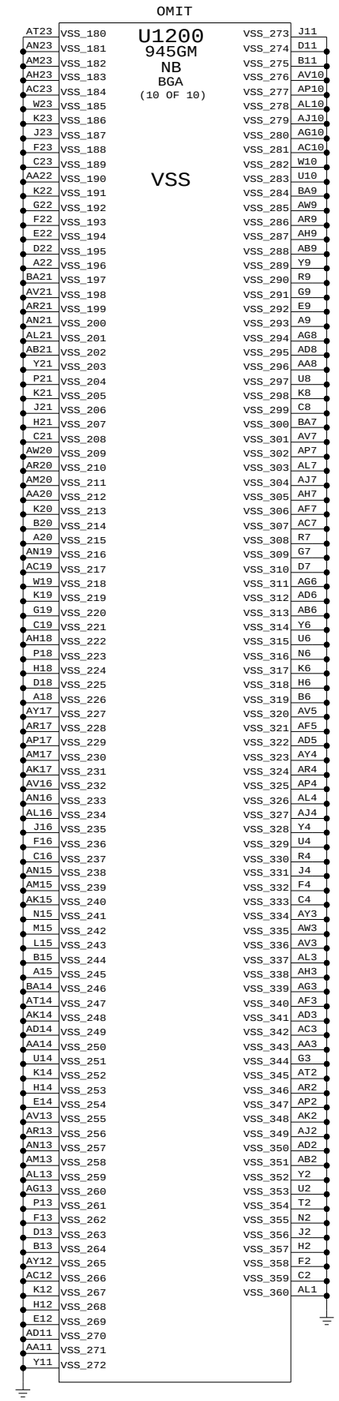
SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 17 OF 86	





NB Grounds

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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D	051-7023	06
SCALE NONE	SHT 18 OF 86	

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	PP1V05_S0	1500mA Max
	PP1V05_S0	10mA Max?
	PP1V05_S0	800mA Max
	PP1V05_S0	?mA Max
3674mA Max	PP1V5_S0	?mA Max
	PP1V5_S0	1500mA Max
	PP1V5_S0	?mA Max
	PP1V5_S0	100mA Max
	PP1V5_S0	24mA Max
	PP1V5_S0	150mA Max
	PP1V5_S0	1900mA Max
3200mA Max	PP1V8_S3	3200mA Max
132mA Max	GND	70mA Max
	GND	60mA Max
	PP2V5_S0	2mA Max
40mA Max?	PP3V3_S0	?mA Max
	PP3V3_S0	40mA Max

PP1V05_S0 → PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, GND, GND

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) → TP_CRT_DDC_CLK

TP_CRT_DDC_DATA (MAKE_BASE=TRUE) → TP_CRT_DDC_DATA

PP1V5_S0 → PP1V5_S0, PP1V5_S0, PP1V5_S0, PP1V5_S0, PP1V5_S0, PP1V5_S0, PP1V5_S0

TP_LVDS_BKLTCTL (MAKE_BASE=TRUE)	TP_LVDS_BKLTCTL
TP_LVDS_BKLTEN (MAKE_BASE=TRUE)	TP_LVDS_BKLTEN
TP_LVDS_CLKCTLA (MAKE_BASE=TRUE)	TP_LVDS_CLKCTLA
TP_LVDS_CLKCTLB (MAKE_BASE=TRUE)	TP_LVDS_CLKCTLB
TP_LVDS_DDC_CLK (MAKE_BASE=TRUE)	TP_LVDS_DDC_CLK
TP_LVDS_DDC_DATA (MAKE_BASE=TRUE)	TP_LVDS_DDC_DATA
NC_LVDS_IBG (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_IBG
TP_LVDS_VDDEN (MAKE_BASE=TRUE)	TP_LVDS_VDDEN
NC_LVDS_VREFH (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_VREFH
TP_LVDS_VREFL (MAKE_BASE=TRUE)	TP_LVDS_VREFL
NC_LVDS_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_A_CLKP
NC_LVDS_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_A_CLKN
NC_LVDS_A_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE)	LVDS_A_DATA_P<2..0>
NC_LVDS_A_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE)	LVDS_A_DATA_N<2..0>
NC_LVDS_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_B_CLKP
NC_LVDS_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_B_CLKN
NC_LVDS_B_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE)	LVDS_B_DATA_P<2..0>
NC_LVDS_B_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE)	LVDS_B_DATA_N<2..0>
NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_NB_XOR_LVDS_A34
NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_NB_XOR_LVDS_A35
NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_NB_XOR_LVDS_D27
NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_NB_XOR_LVDS_D28
TP_SDVO_CTRLCLK (MAKE_BASE=TRUE)	TP_SDVO_CTRLCLK
TP_SDVO_CTRLDATA (MAKE_BASE=TRUE)	TP_SDVO_CTRLDATA

(MCH LVDS DATA/CLK TX 2.5V PWR) GND

(MCH LVDS DIGITAL 1.5V PWR) GND

(MCH LVDS ANALOG 2.5V PWR) GND

NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE) — NC_GND_NB_VSSA_LVDS

(MCH CRTDAC ANALOG 2.5V PWR) PP1V05_S0 — PP1V05_S0, GND

(MCH H/V SYNC 2.5V PWR) GND

(MCH TVDAC DEDICATED PWR 1.5V) PP1V5_S0 — PP1V5_S0

(MCH TVDAC DIGITAL QUIET 1.5V PWR) PP1V5_S0 — PP1V5_S0

(MCH TV OUT CHANNEL A 3.3V PWR) PP1V5_S0 — PP1V5_S0

(MCH TV OUT CHANNEL B 3.3V PWR) PP1V5_S0 — PP1V5_S0

(MCH TV OUT CHANNEL C 3.3V PWR) PP1V5_S0 — PP1V5_S0

(MCH TV DAC BAND GAP 3.3V PWR) PP1V5_S0 — PP1V5_S0, GND

(MCH DISPLAY A PLL 1.5V PWR) TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE) — TP_NB_VCCA_DPLLA

(MCH DISPLAY B PLL 1.5V PWR) TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE) — TP_NB_VCCA_DPLLB

GND, GND, GND, GND

GMCH CORE PWR 1.05V BYPASS

PP1V05_S0 1500mA Max → C1900 (CRITICAL, 470uF-9MOHM, 20%, 2.5V, POLY, D2TS) | C1902 10uF 20% 6.3V X6S 603 | C1903 10uF 20% 6.3V X6S 603 | C1904 1uF 10% 6.3V CERM 402 | C1905 0.22uF 20% 6.3V X6S 402 | C1906 0.22uF 20% 6.3V X6S 402 | C1907 0.22uF 20% 6.3V X6S 402

MCH VTT BYPASS (MCH FSB 1.05V PWR)

PP1V05_S0 800mA Max → C1965 4.7uF 20% 6.3V CERM 603 | C1966 2.2uF 20% 6.3V CERM1 603

Layout Note: Place in cavity

(SHARE C0940 470UF) C1967 0.22uF 20% 6.3V X6S 402

Layout Note: Place on the edge

MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR)

PP3V3_S0 40mA Max → C1914 10uF 20% 6.3V X6S 603 | C1915 0.1uF 20% 10V CERM 402

MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)

PP2V5_S0 2mA Max → C1916 0.1uF 20% 10V CERM 402

GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

PP1V5_S0 1900mA Max → C1918 0.1uF 20% 10V CERM 402

GMCH VCCA_HPLL FILTER (HOST PLL 1.5V PWR)

PP1V5_S0 100mA Max → L1934 FERR-120-OHM-0.2A (0603) → PP1V5_S0_NB_VCCA_HPLL (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V) 45mA Max

C1934 22UF 20% 6.3V CERM 805 | C1935 0.1uF 20% 10V CERM 402

GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR)

PP1V5_S0 → L1936 FERR-120-OHM-0.2A (0603) → PP1V5_S0_NB_VCCA_MPLL (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V) 45mA Max

C1936 22UF 20% 6.3V CERM 805 | C1937 0.1uF 20% 10V CERM 402

GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR)

1500mA Max → PP1V5_S0 → L1970 91nH (1210)

Layout Note: Place L and C close to MCH

C1970 220UF 20% 2.5V POLY SMB2

C1971 10uF 20% 6.3V X6S 603 | C1972 10uF 20% 6.3V X6S 603

Layout Note: 10uF caps should be close to MCH on opposite side.

→ PP1V5_S0_NB_VCC3G (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V) → 1500mA Max

GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR)

1500mA Max → PP1V5_S0 → L1975 1.0UH-220MA-0.12-OHM (0805) → PP1V5_S0_NB_3GPLL_F (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.4 mm, VOLTAGE=1.5V) → R1975 0.51 1% 1/16W MF-LF 402 → PP1V5_S0_NB_VCCA_3GPLL (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V)

C1975 10uF 20% 6.3V X5R 603 | C1976 0.1uF 20% 10V CERM 402 — GND

Layout Note: 3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=M1_MLB SYNC_DATE=02/08/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7023	06

SCALE NONE SHT 19 OF 86

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

PP3V3_S0
48,51,53,56,57,59,60,64,65,66
4,5,10,14,17,19,20,21,22,23,24
25,26,27,28,29,33,34,36,37,43
70,78,79

NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

PP3V3_S0
37,43,48,51,53,56,57,59,60,64
4,5,10,14,17,19,20,21,22,23,24
25,26,27,28,29,33,34,36
65,66,70,78,79

NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

PP3V3_S0
78,79
4,5,10,37,43,48,51,53,56,57,59
14,17,19,20,21,22,23,24
25,26,27,28,29,33
60,64,65,66,70

NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

945 External Design Spec says reserved

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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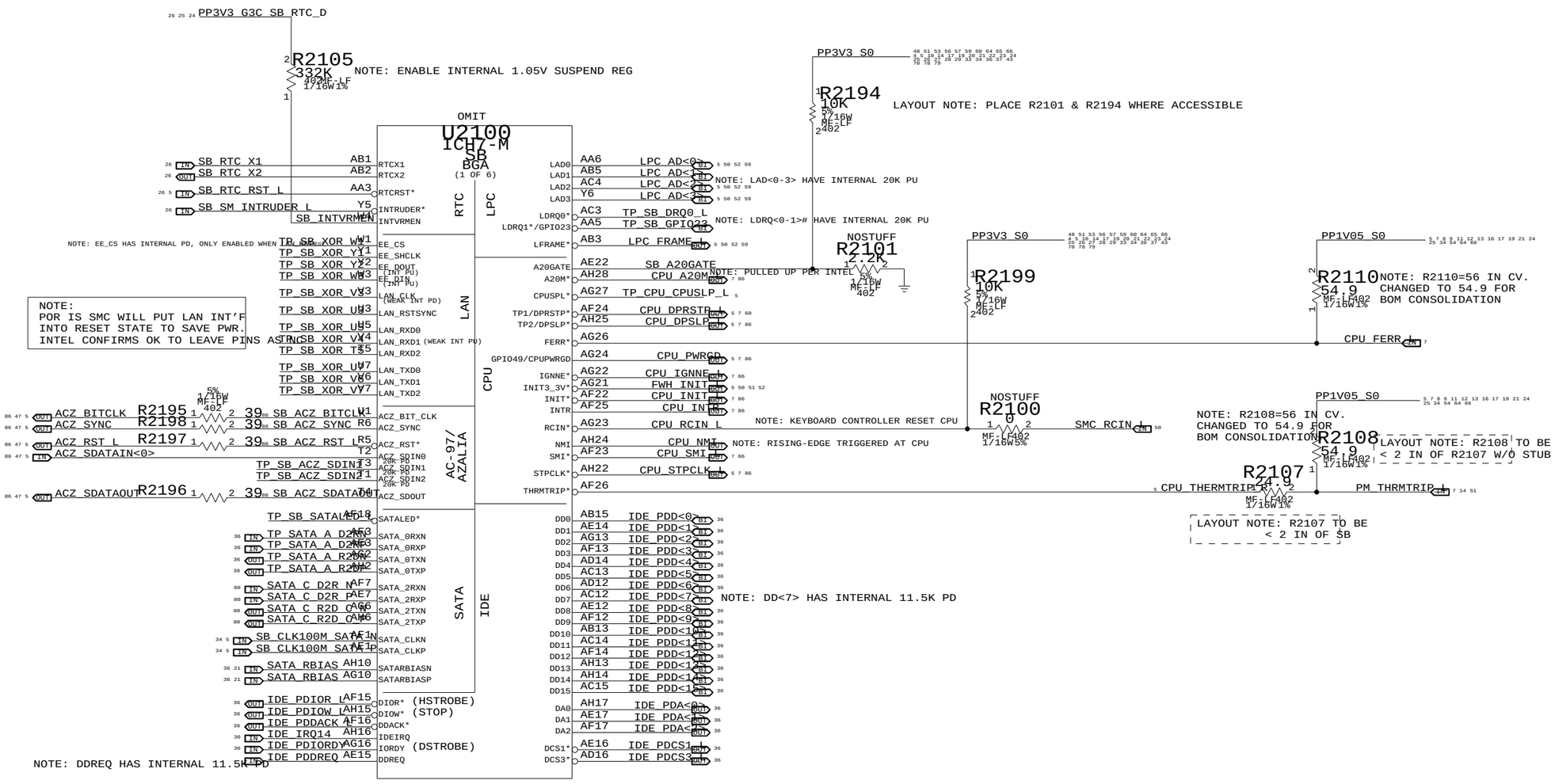
D	051-7023	06
SCALE NONE	SHT 20 OF 86	



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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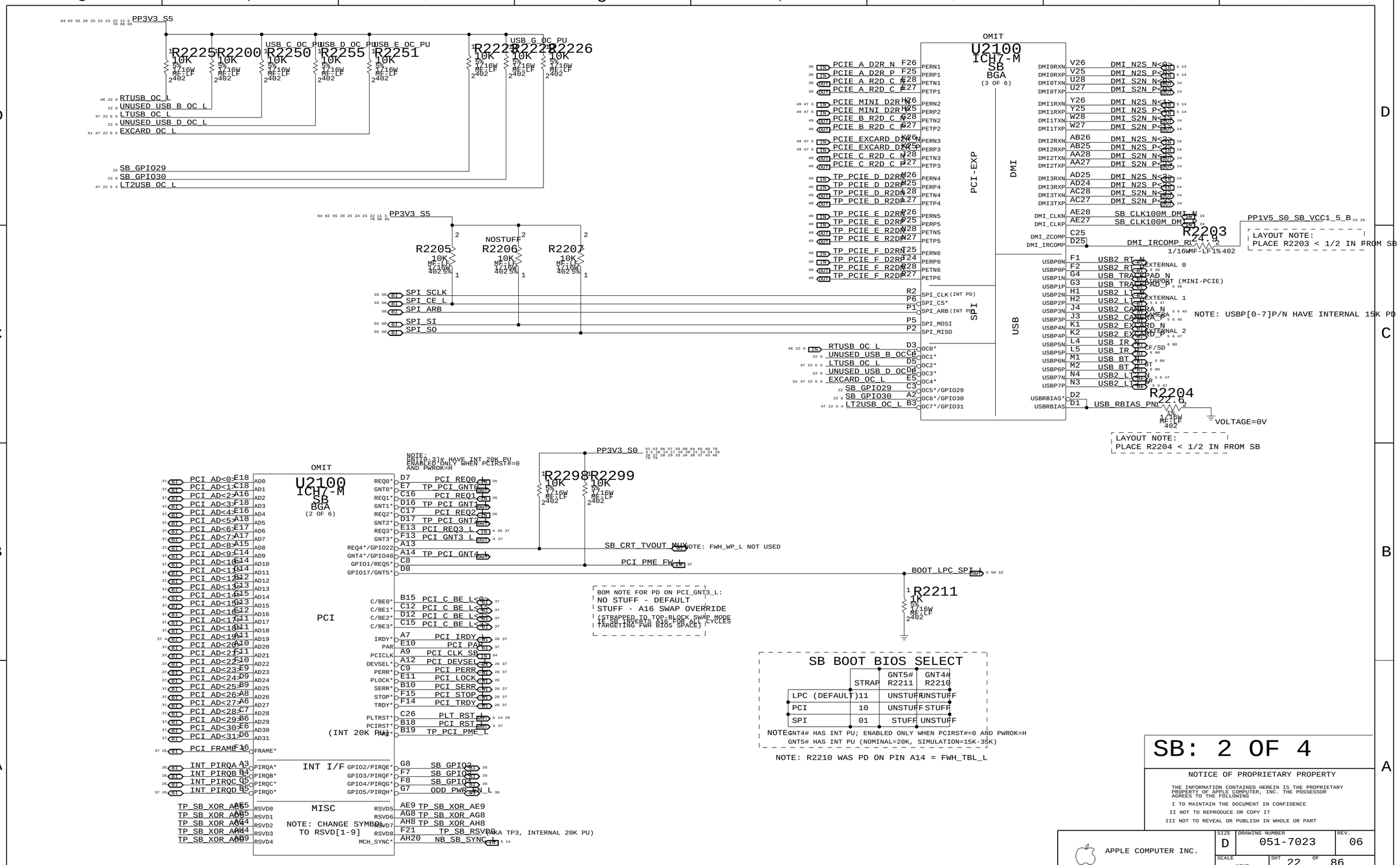
D	051-7023	06
SCALE NONE	SHT 21 OF 86	


PP3V3_S5
R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2227 10K 5% 1/16W MF-LF 402
R2228 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402
USB_C_OC_PU
USB_D_OC_PU
USB_E_OC_PU
USB_G_OC_PU
RTUSB_OC_L
UNUSED_USB_B_OC_L
LTUSB_OC_L
UNUSED_USB_D_OC_L
EXCARD_OC_L
SB_GPIO29
SB_GPIO30
LT2USB_OC_L
R2205 10K 5% 1/16W MF-LF 402
NOSTUFF
R2206 10K 5% 1/16W MF-LF 402
R2207 10K 5% 1/16W MF-LF 402
SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO
OMIT
U2100
ICH7-M
SB
BGA
(3 OF 6)
PCI-EXP
DMI
SPI
USB
PCIE_A_D2R_N
PCIE_A_D2R_P
PCIE_A_R2D_C_N
PCIE_A_R2D_C_P
PCIE_MINI_D2R_N
PCIE_MINI_D2R_P
PCIE_B_R2D_C_N
PCIE_B_R2D_C_P
PCIE_EXCARD_D2R_N
PCIE_EXCARD_D2R_P
PCIE_C_R2D_C_N
PCIE_C_R2D_C_P
TP_PCIE_D_D2RN
TP_PCIE_D_D2RP
TP_PCIE_D_R2DN
TP_PCIE_D_R2DP
TP_PCIE_E_D2RN
TP_PCIE_E_D2RP
TP_PCIE_E_R2DN
TP_PCIE_E_R2DP
TP_PCIE_F_D2RN
TP_PCIE_F_D2RP
TP_PCIE_F_R2DN
TP_PCIE_F_R2DP
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_N2S_N<0>
DMI_N2S_P<0>
DMI_S2N_N<0>
DMI_S2N_P<0>
DMI_N2S_N<1>
DMI_N2S_P<1>
DMI_S2N_N<1>
DMI_S2N_P<1>
DMI_N2S_N<2>
DMI_N2S_P<2>
DMI_S2N_N<2>
DMI_S2N_P<2>
DMI_N2S_N<3>
DMI_N2S_P<3>
DMI_S2N_N<3>
DMI_S2N_P<3>
DMI_CLKN
DMI_CLKP
SB_CLK100M_DMI_N
SB_CLK100M_DMI_P
DMI_ZCOMP
DMI_IRCOMP
DMI_IRCOMP_R
R2203 24.9 1/16W MF-LF 1% 402
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE:
PLACE R2203 < 1/2 IN FROM SB
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USB2_RT_N
USB2_RT_P
USB_TRACKPAD_N
USB_TRACKPAD_P
USB2_LT_N
USB2_LT_P
USB2_CAMERA_N
USB2_CAMERA_P
USB2_EXCARD_N
USB2_EXCARD_P
USB_IR_N
USB_IR_P
USB_BT_N
USB_BT_P
USB2_LT2_N
USB2_LT2_P
EXTERNAL 0
EXTERNAL 1
EXTERNAL 2
NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD
USBRBIAS*
USBRBIAS
USB_RBIAS_PN
R2204 22.6 1/16W MF-LF 402
VOLTAGE=0V
LAYOUT NOTE:
PLACE R2204 < 1/2 IN FROM SB
OC0*
OC1*
OC2*
OC3*
OC4*
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
SPI_CLK (INT PD)
SPI_CS*
SPI_ARB (INT PD)
SPI_MOSI
SPI_MISO
NOTE: GNT[0-3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
PP3V3_S0
R2298 10K 5% 1/16W MF-LF 402
R2299 10K 5% 1/16W MF-LF 402
SB_CRT_TVOUT_MUX
NOTE: FWH_WP_L NOT USED
PCI_PME_FW_L
BOOT_LPC_SPI_L
R2211 1K 5% 1/16W MF-LF 402
BOM NOTE FOR PD ON PCI_GNT3_L:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IF SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)
OMIT
U2100
ICH7-M
SB
BGA
(2 OF 6)
PCI
INT I/F
MISC
PCI_AD<0>
PCI_AD<1>
PCI_AD<2>
PCI_AD<3>
PCI_AD<4>
PCI_AD<5>
PCI_AD<6>
PCI_AD<7>
PCI_AD<8>
PCI_AD<9>
PCI_AD<10>
PCI_AD<11>
PCI_AD<12>
PCI_AD<13>
PCI_AD<14>
PCI_AD<15>
PCI_AD<16>
PCI_AD<17>
PCI_AD<18>
PCI_AD<19>
PCI_AD<20>
PCI_AD<21>
PCI_AD<22>
PCI_AD<23>
PCI_AD<24>
PCI_AD<25>
PCI_AD<26>
PCI_AD<27>
PCI_AD<28>
PCI_AD<29>
PCI_AD<30>
PCI_AD<31>
PCI_FRAME
INT_PIRQA
INT_PIRQB
INT_PIRQC
INT_PIRQD
TP_SB_XOR_AE5
TP_SB_XOR_AG5
TP_SB_XOR_AG4
TP_SB_XOR_AH4
TP_SB_XOR_AG9
REQ0*
GNT0*
REQ1*
GNT1*
REQ2*
GNT2*
REQ3*
GNT3*
REQ4*/GPIO22
GNT4*/GPIO48
GPIO1/REQ5*
GPIO17/GNT5*
PCI_REQ0_L
TP_PCI_GNT0
PCI_REQ1_L
TP_PCI_GNT1
PCI_REQ2_L
TP_PCI_GNT2
PCI_REQ3_L
PCI_GNT3_L
TP_PCI_GNT4_L
C/BE0*
C/BE1*
C/BE2*
C/BE3*
IRDY*
PAR
PCICLK
DEVSEL*
PERR*
PLOCK*
SERR*
STOP*
TRDY*
PLTRST*
PCIRST*
(INT 20K PU)
PCI_C_BE_L<0>
PCI_C_BE_L<1>
PCI_C_BE_L<2>
PCI_C_BE_L<3>
PCI_IRDY_L
PCI_PAR
PCI_CLK_SB
PCI_DEVSEL_L
PCI_PERR_L
PCI_LOCK_L
PCI_SERR_L
PCI_STOP_L
PCI_TRDY_L
PLT_RST_L
PCI_RST_L
TP_PCI_PME_L
GPIO2/PIRQE*
GPIO3/PIRQF*
GPIO4/PIRQG*
GPIO5/PIRQH*
SB_GPIO2
SB_GPIO3
SB_GPIO4
ODD_PWR_EN_L
RSVD0
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
MCH_SYNC*
TP_SB_XOR_AE9
TP_SB_XOR_AG8
TP_SB_XOR_AH8
TP_SB_RSVD20
(NOTE: TP3, INTERNAL 20K PU)
NB_SB_SYNC
NOTE: CHANGE SYMBOL TO RSVD[1-9]
SB BOOT BIOS SELECT
STRAP
GNT5# R2211
GNT4# R2210
LPC (DEFAULT) 11 UNSTUFF UNSTUFF
PCI 10 UNSTUFF STUFF
SPI 01 STUFF UNSTUFF
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L
SB: 2 OF 4
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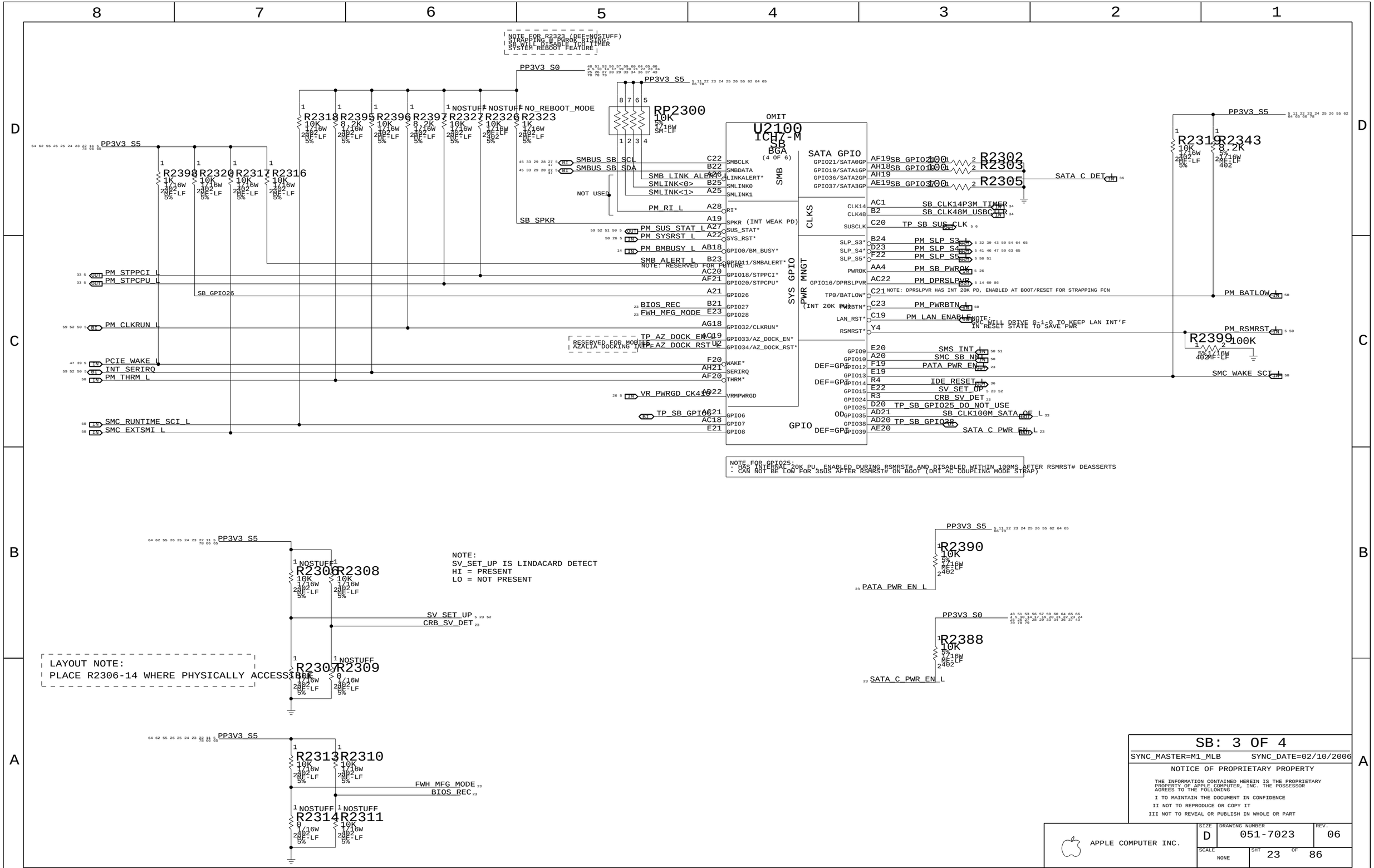
SIZE D
DRAWING NUMBER 051-7023
REV. 06
SCALE NONE
SHT 22 OF 86



SB: 3 OF 4	
SYNC_MASTER=M1_MLB	SYNC_DATE=02/10/2006

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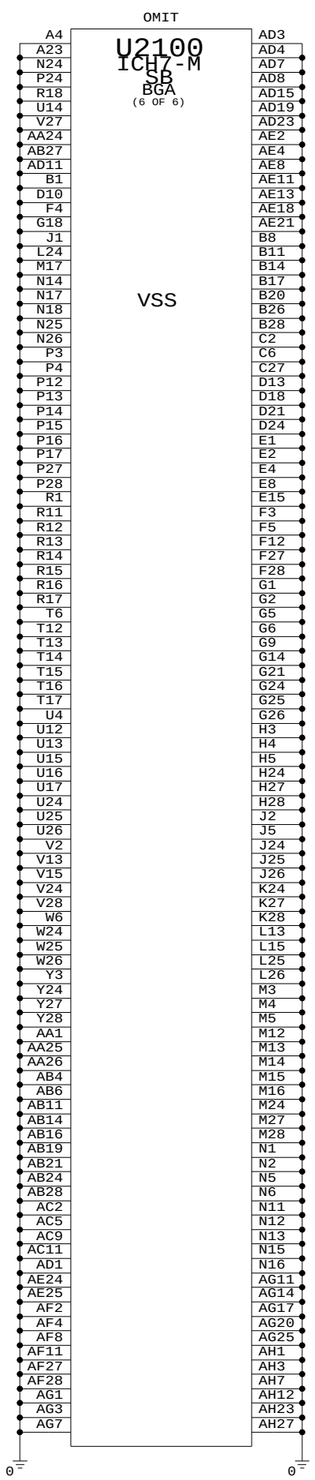
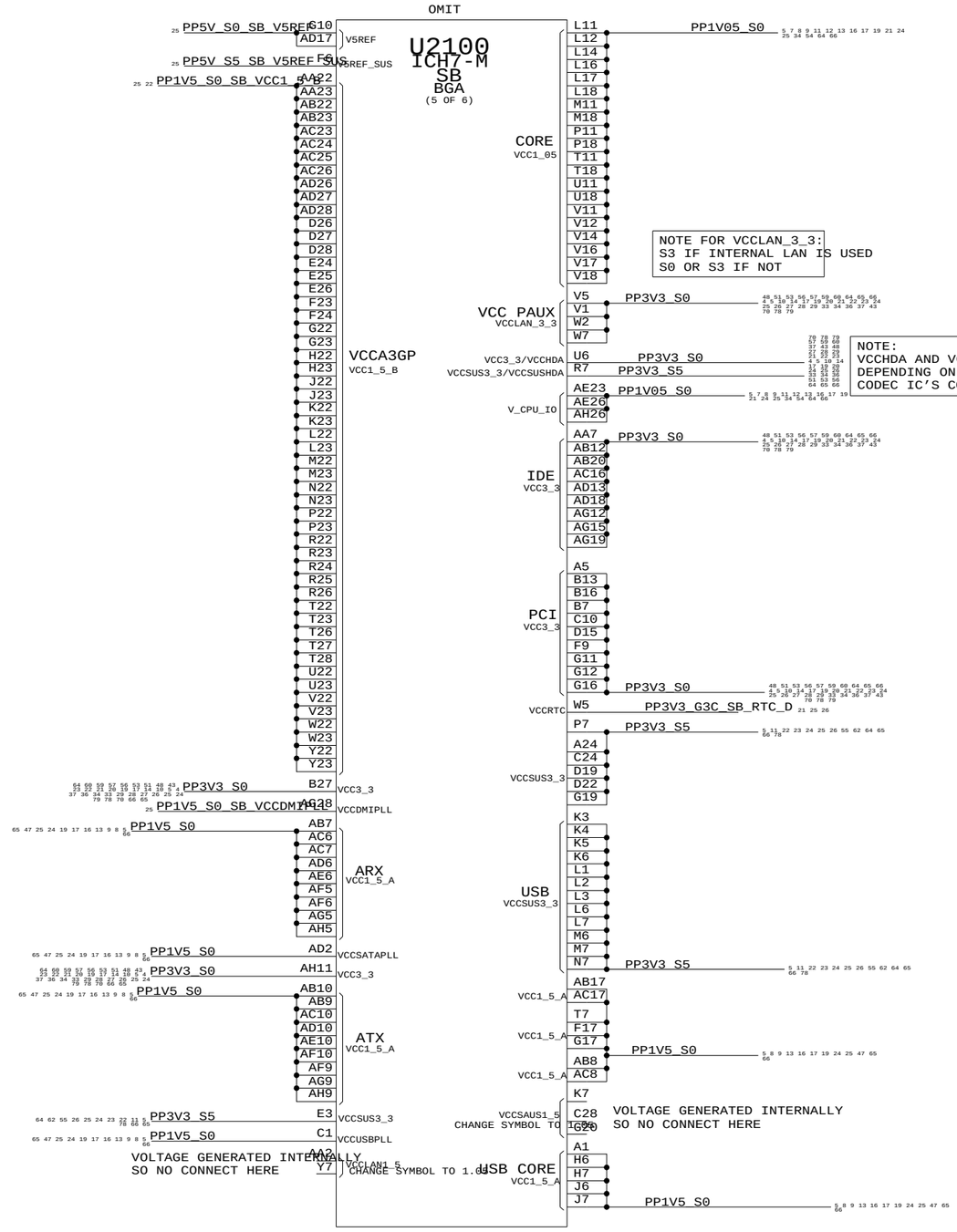
SCALE NONE	SHT 23 OF 86	





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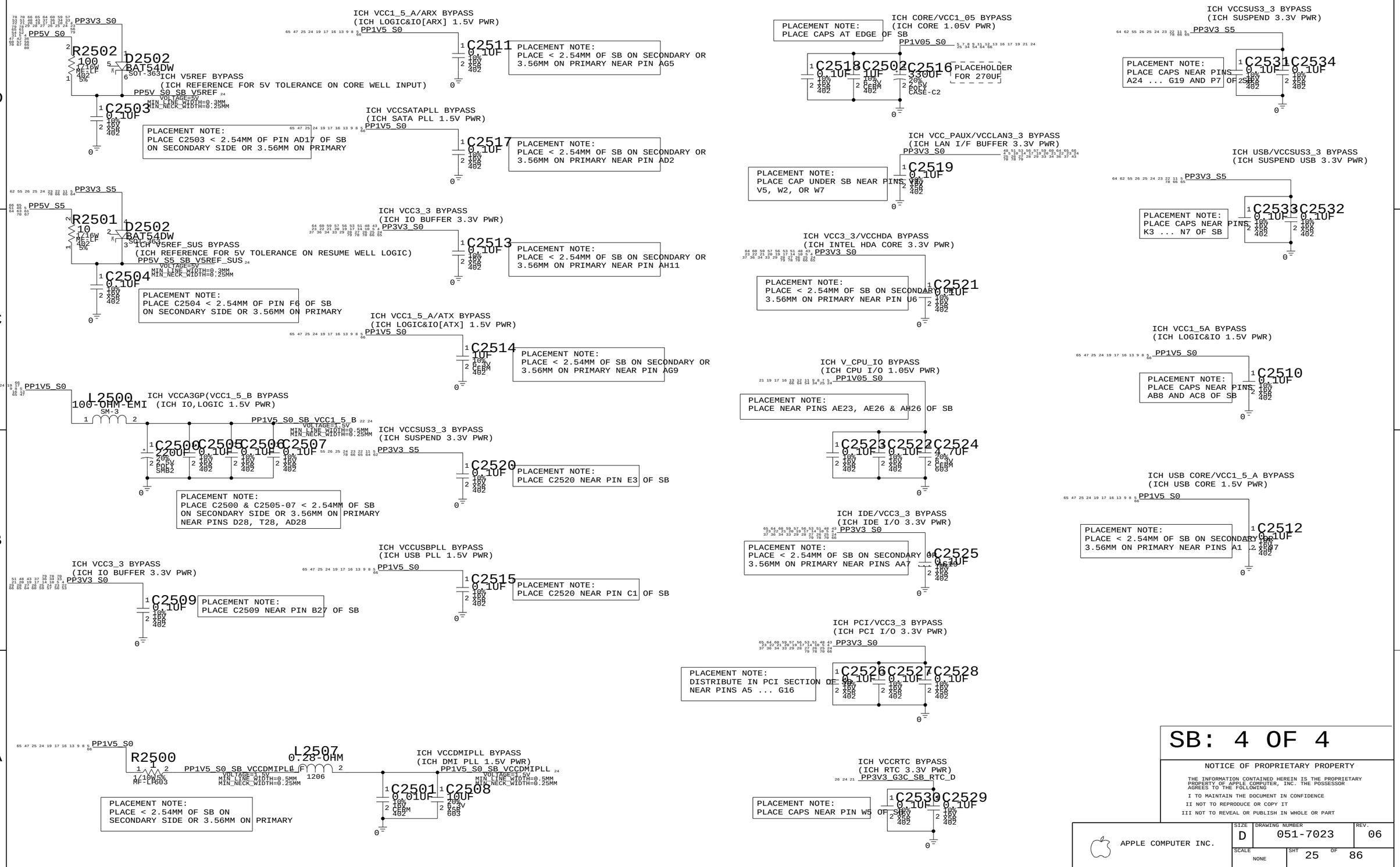
ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
PP1V5_S0
C2511
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG5
PP3V3_S0
PP5V_S0
R2502
100
D2502
BAT54DW
SOT-363
ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
PP5V_S0_SB_V5REF
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2503
0.1UF
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
PP1V5_S0
C2517
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AD2
PP3V3_S5
PP5V_S5
R2501
10
D2502
BAT54DW
SOT-363
ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
PP5V_S5_SB_V5REF_SUS
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2504
0.1UF
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PP3V3_S0
C2513
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
PP1V5_S0
C2514
1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG9
PP1V5_S0
L2500
100-OHM-EMI
SM-3
ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
PP1V5_S0_SB_VCC1_5_B
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2500
220UF
20%
2.5V
POLY
SMB2
C2505
0.1UF
C2506
0.1UF
C2507
0.1UF
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PP3V3_S5
C2520
0.1UF
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PP3V3_S0
C2509
0.1UF
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
PP1V5_S0
C2515
0.1UF
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB
PP1V5_S0
R2500
1/10W5%
MF-LF003
PP1V5_S0_SB_VCCDMIPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
L2507
0.28-OHM
1206
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
PP1V5_S0_SB_VCCDMIPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2501
0.01UF
10%
16V
CERM
402
C2508
10UF
20%
6.3V
X6S
603
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
PP1V05_S0
C2518
0.1UF
C2502
1UF
C2516
330UF
20%
2.5V
POSCAP
CASE-C2
PLACEHOLDER
FOR 270UF
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
PP3V3_S0
C2519
0.1UF
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS W4,
V5, W2, OR W7
ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
PP3V3_S0
C2521
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
PP1V05_S0
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB
C2523
0.1UF
C2522
0.1UF
C2524
4.7UF
20%
6.3V
CERM
603
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
PP3V3_S0
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7
C2525
0.1UF
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
PP3V3_S0
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16
C2526
0.1UF
C2527
0.1UF
C2528
0.1UF
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
PP3V3_G3C_SB_RTC_D
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB
C2530
0.1UF
C2529
0.1UF
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PP3V3_S5
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF SB
C2531
0.1UF
C2534
0.1UF
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
PP3V3_S5
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB
C2533
0.1UF
C2532
0.1UF
ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
PP1V5_S0
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB
C2510
0.1UF
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
PP1V5_S0
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1
C2512
0.1UF
SB: 4 OF 4
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REV.
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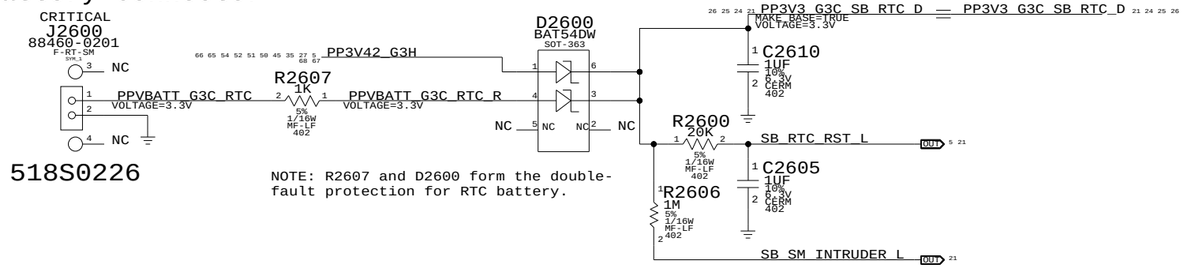
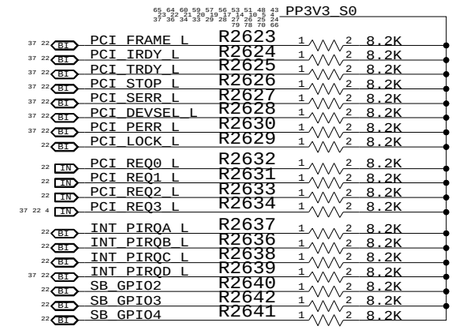
SHT
25
OF
86

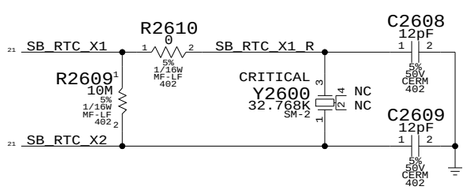
RTC Battery Connector

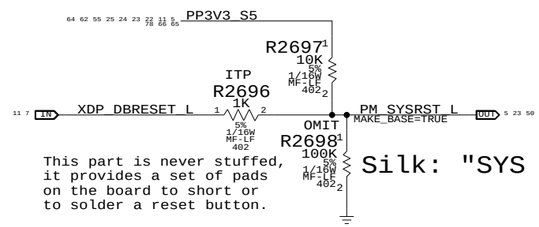


NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



SB RTC Crystal Circuit



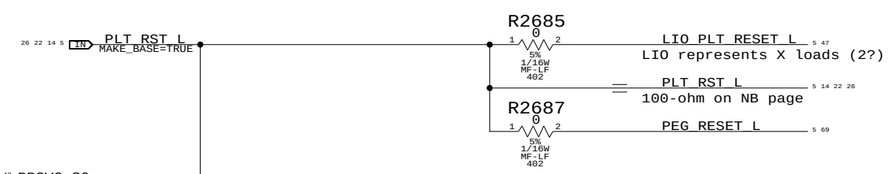


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

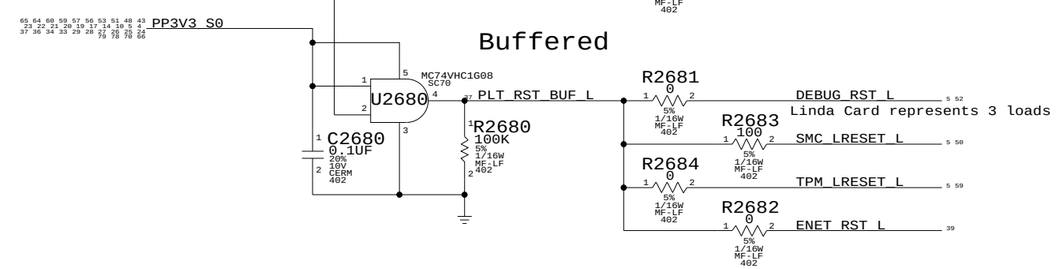
Silk: "SYS RST"

Platform Reset Connections

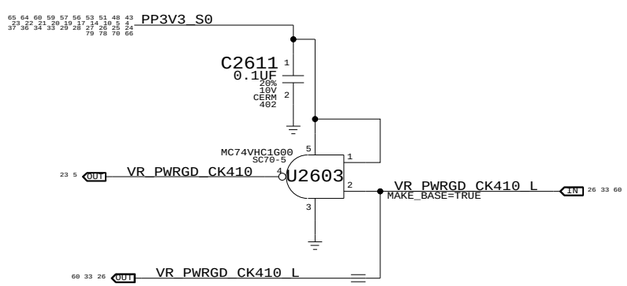
Unbuffered



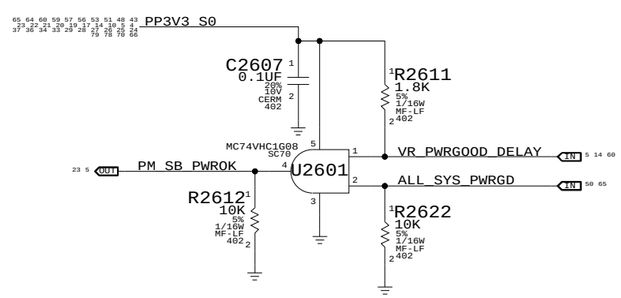
Buffered



Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter



SB Misc	
SYNC_MASTER=M1_MLB	SYNC_DATE=02/10/2006

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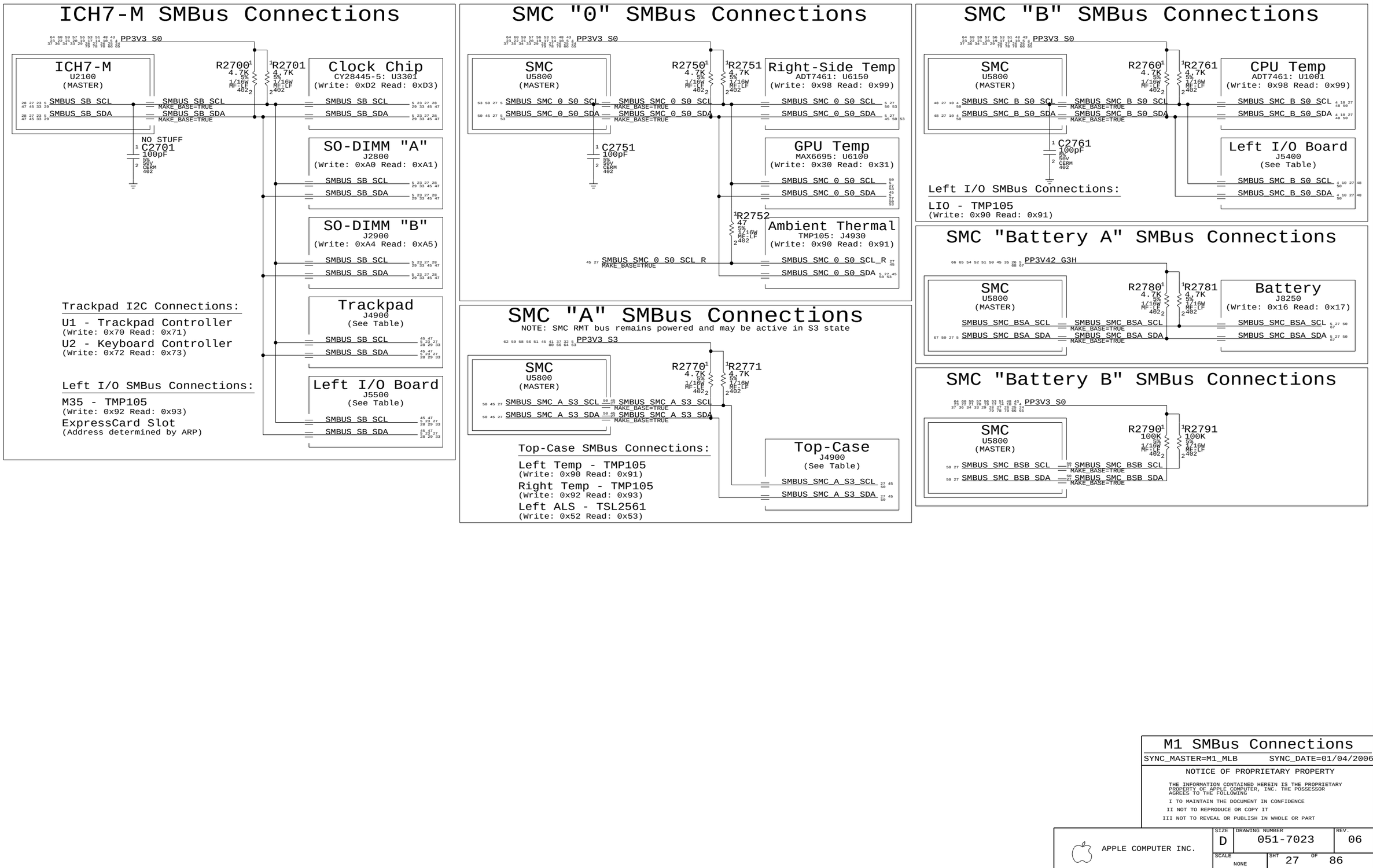
SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 26 OF 86	



M1 SMBus Connections

SYNC_MASTER=M1_MLB SYNC_DATE=01/04/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7023	06

SCALE NONE

SHT 27 OF 86

Page Notes

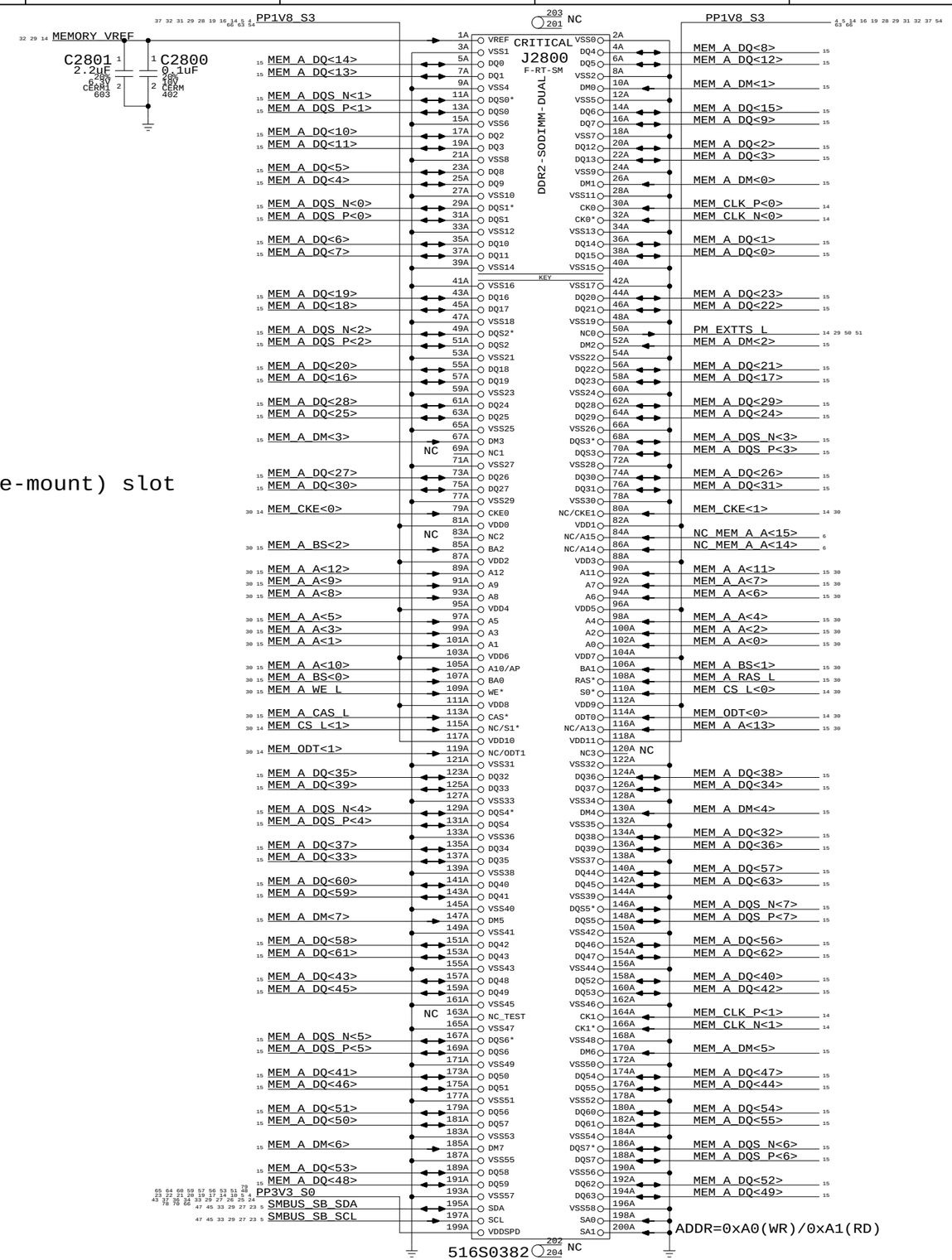
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

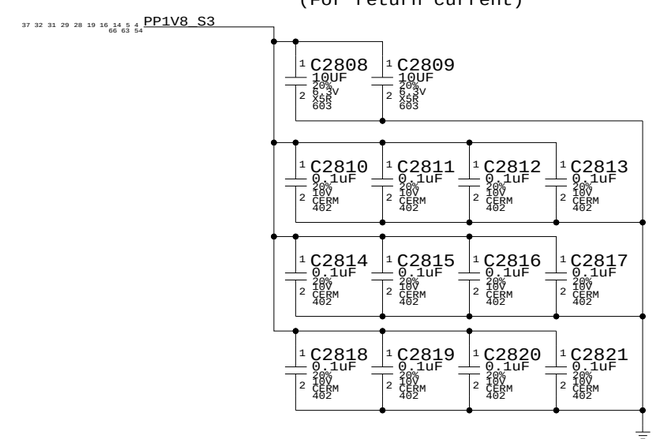
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Lower" (surface-mount) slot



DDR2 Bypass Caps
(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 28 OF 86	

Page Notes

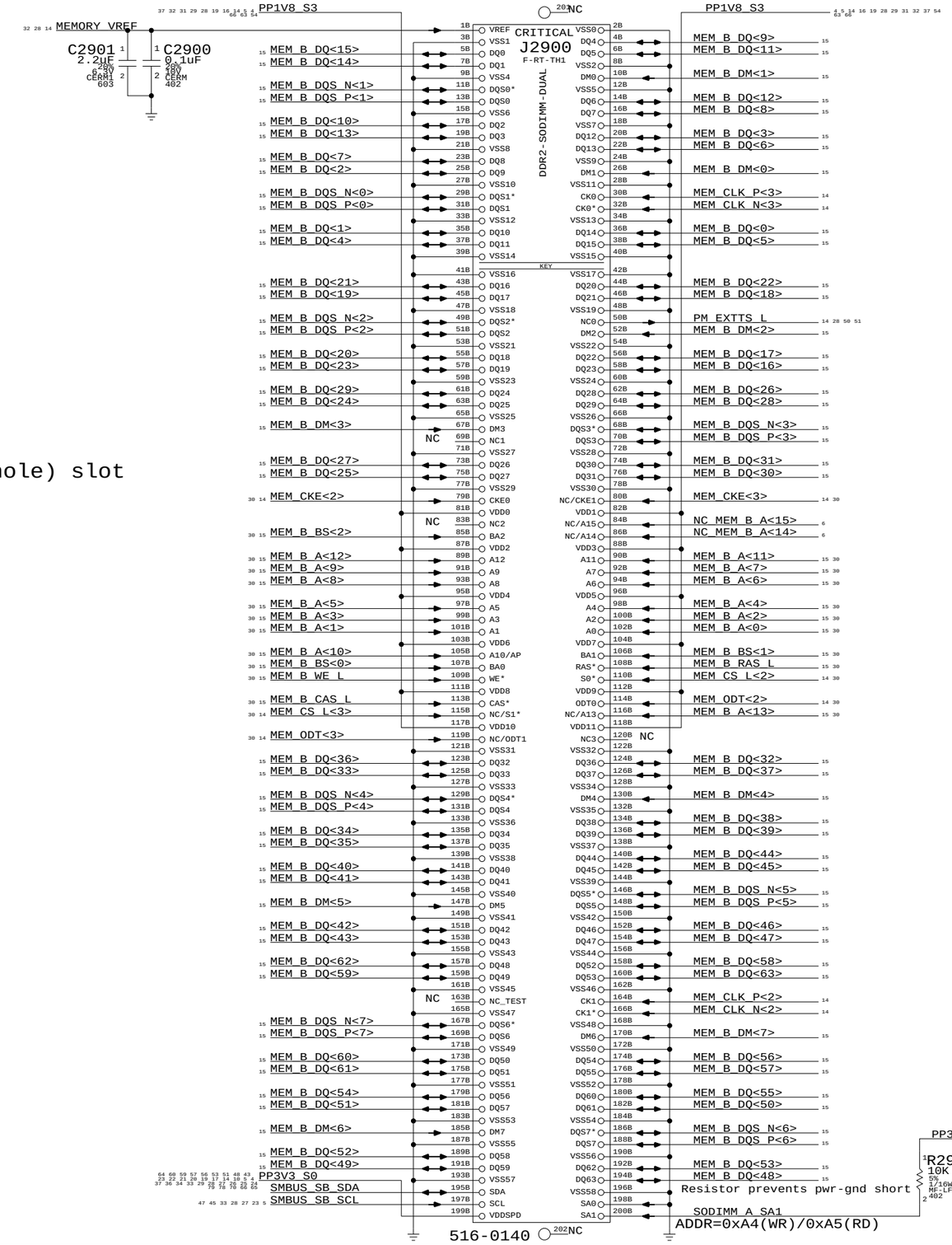
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

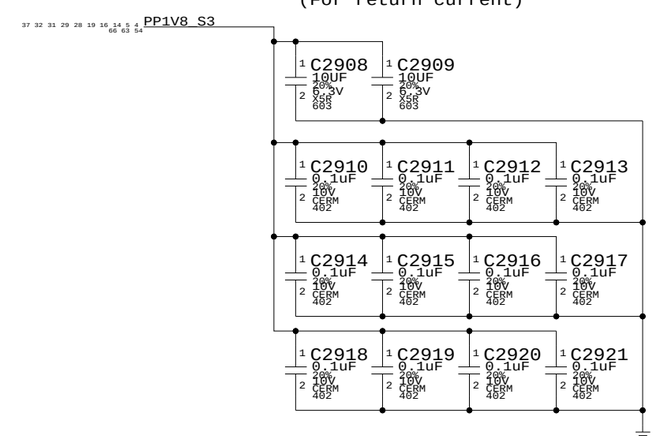
NOTE: This page does not supply VREF.
The reference voltage must be provided by another page.

"Upper" (thru-hole) slot



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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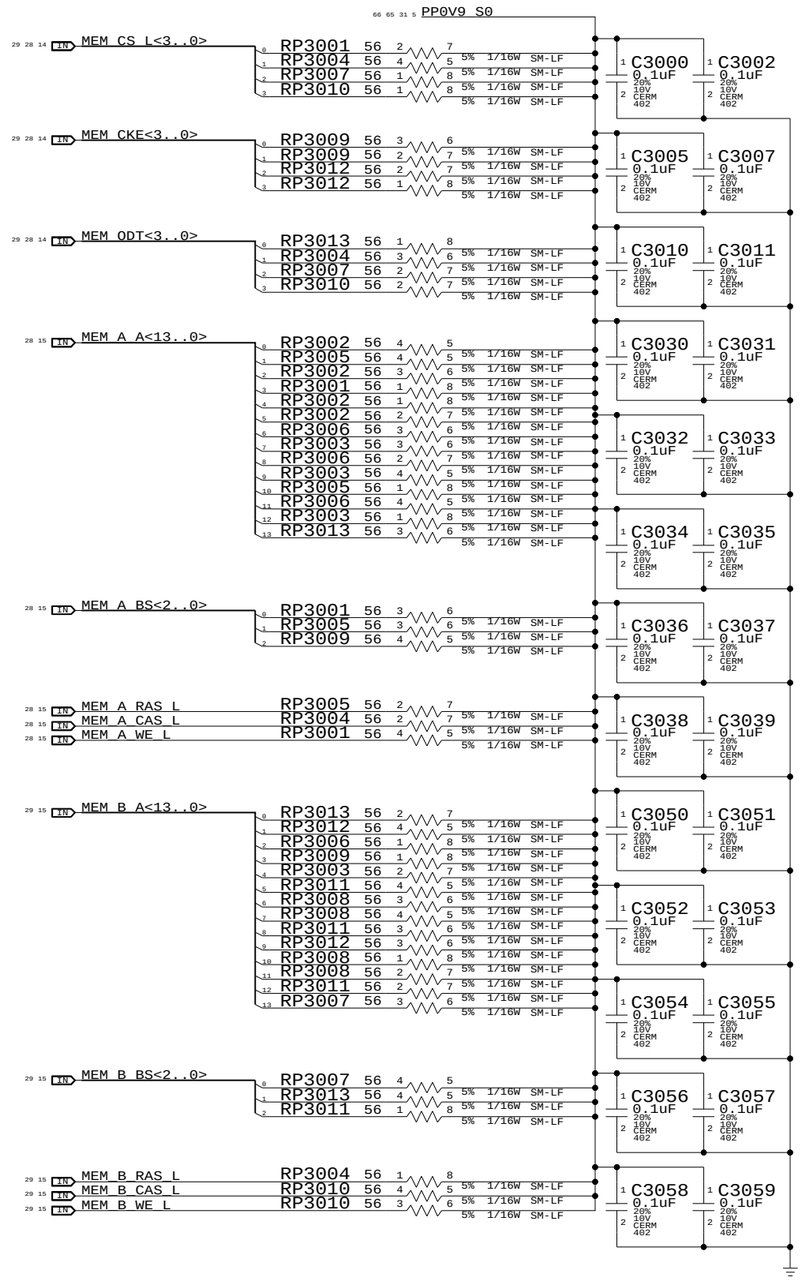
SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 29 OF 86	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/07/2006)

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SIZE	DRAWING NUMBER	REV.
D	051-7023	06

SCALE NONE

SHT 30 OF 86

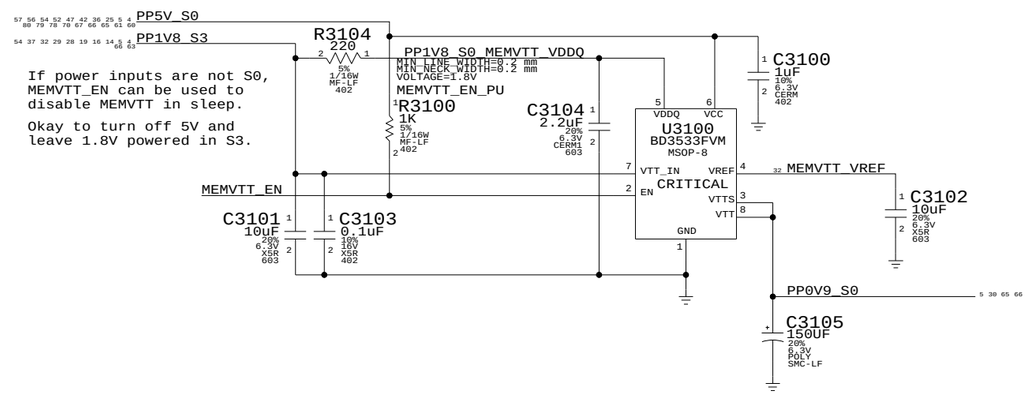
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

Okay to turn off 5V and leave 1.8V powered in S3.

Memory Vtt Supply

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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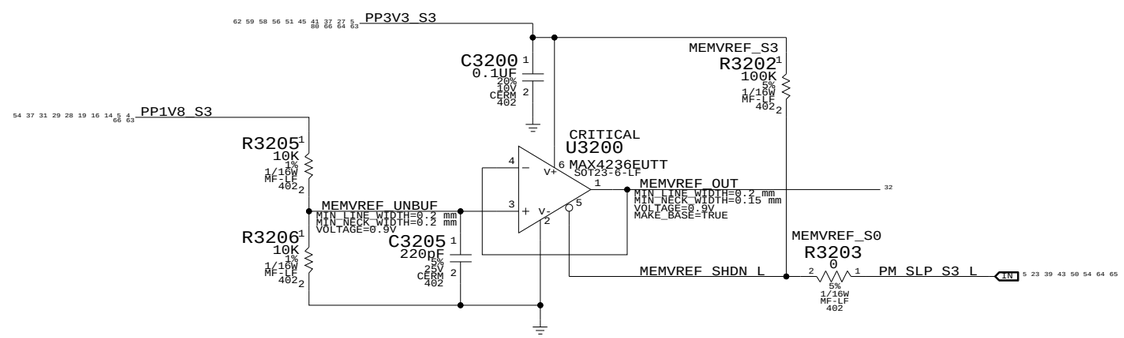
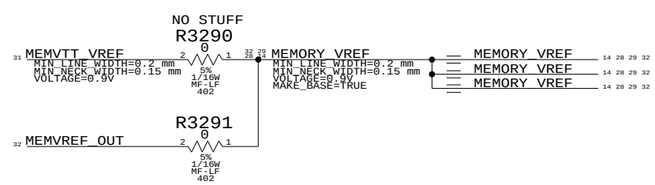
SIZE	DRAWING NUMBER	REV.
D	051-7023	06

SCALE NONE





DDR2 VRef

SYNC_MASTER=M1_MLB SYNC_DATE=12/19/2005

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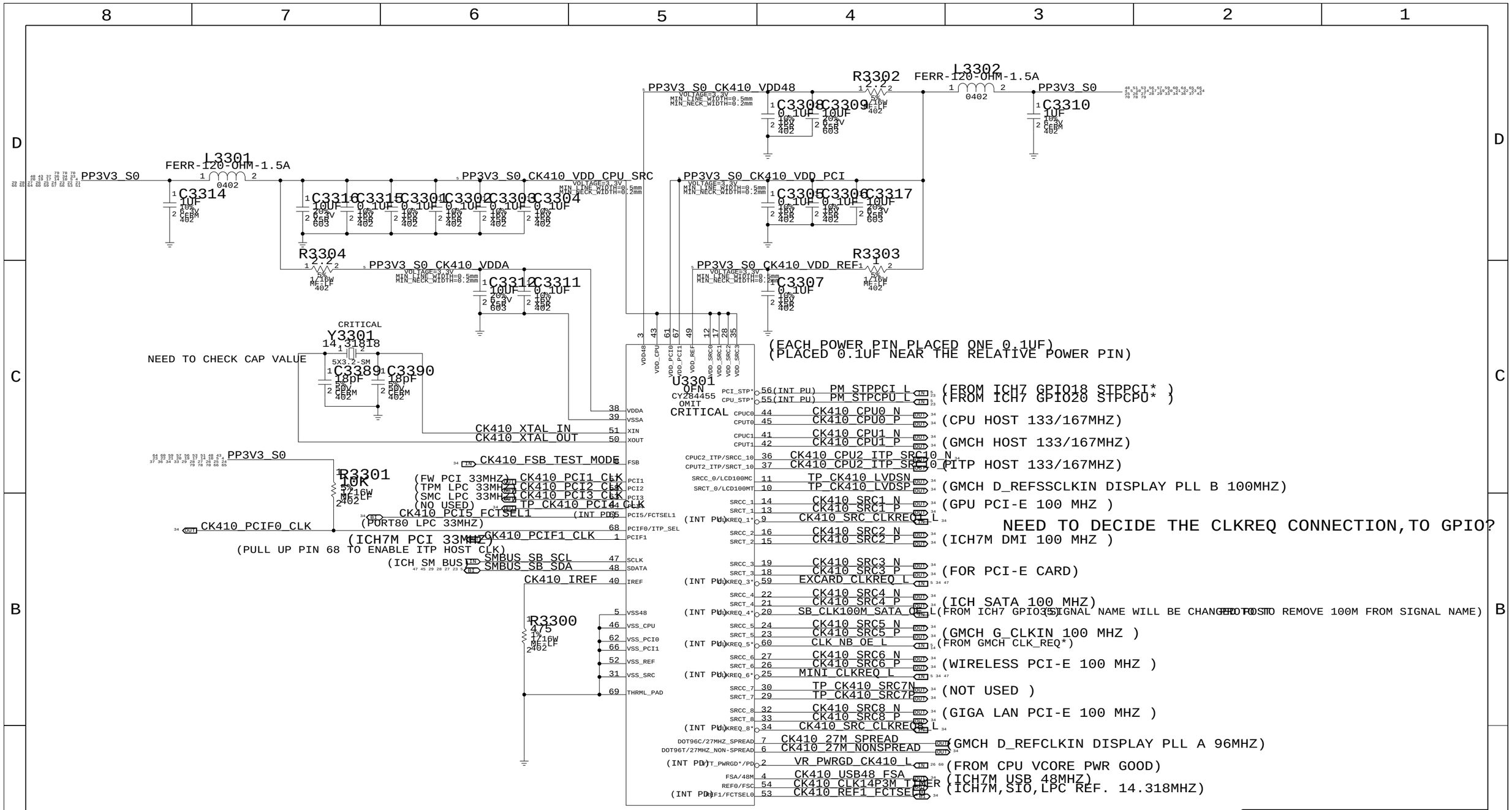
SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 32 OF 86	



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_S	ST100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=M1_MCB SYNC_DATE=02/10/2006

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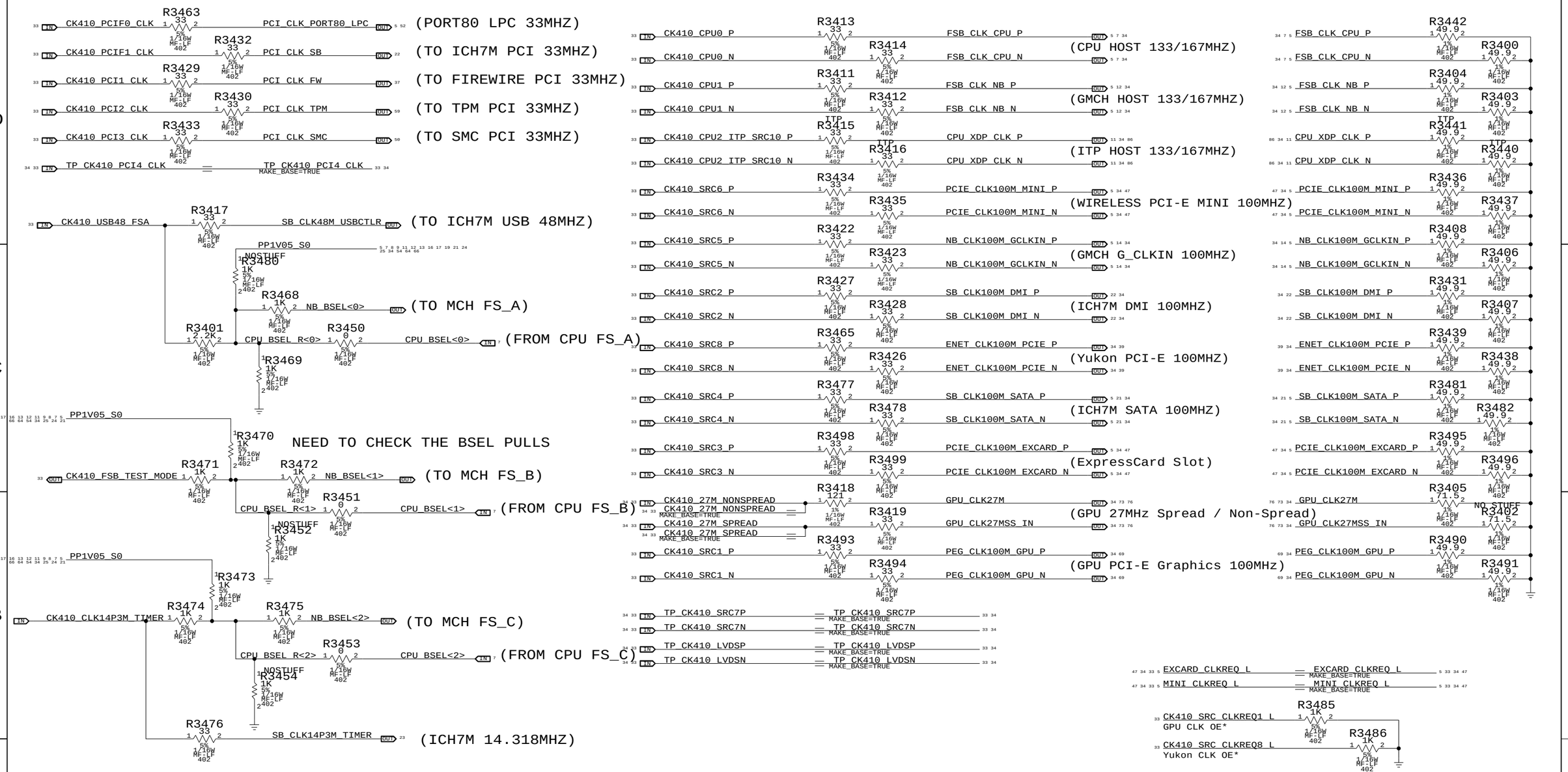
SIZE	DRAWING NUMBER	REV.
D	051-7023	06

SCALE NONE

SHT 33 OF 86



NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED

Clock Termination

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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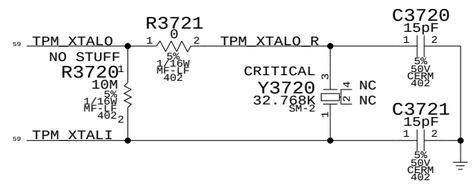
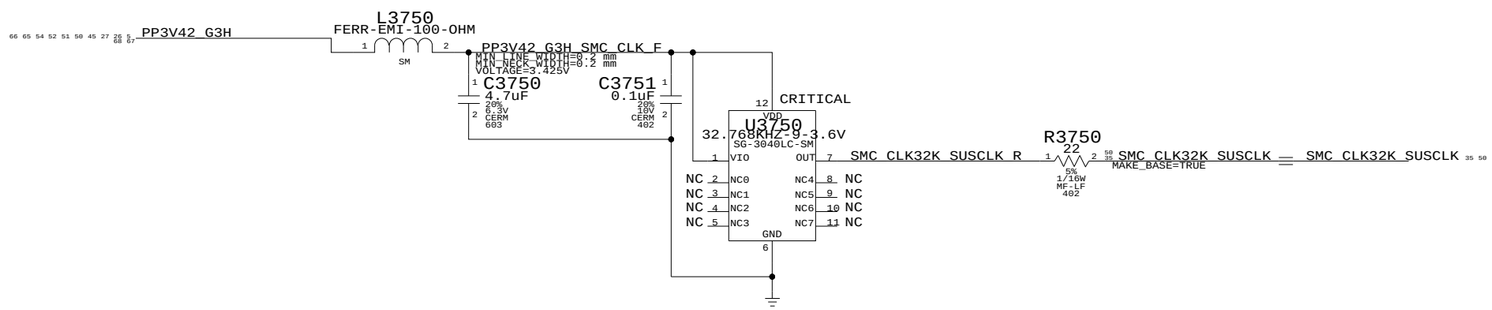
SIZE	DRAWING NUMBER	REV.
D	051-7023	06

SCALE NONE SHT 34 OF 86

TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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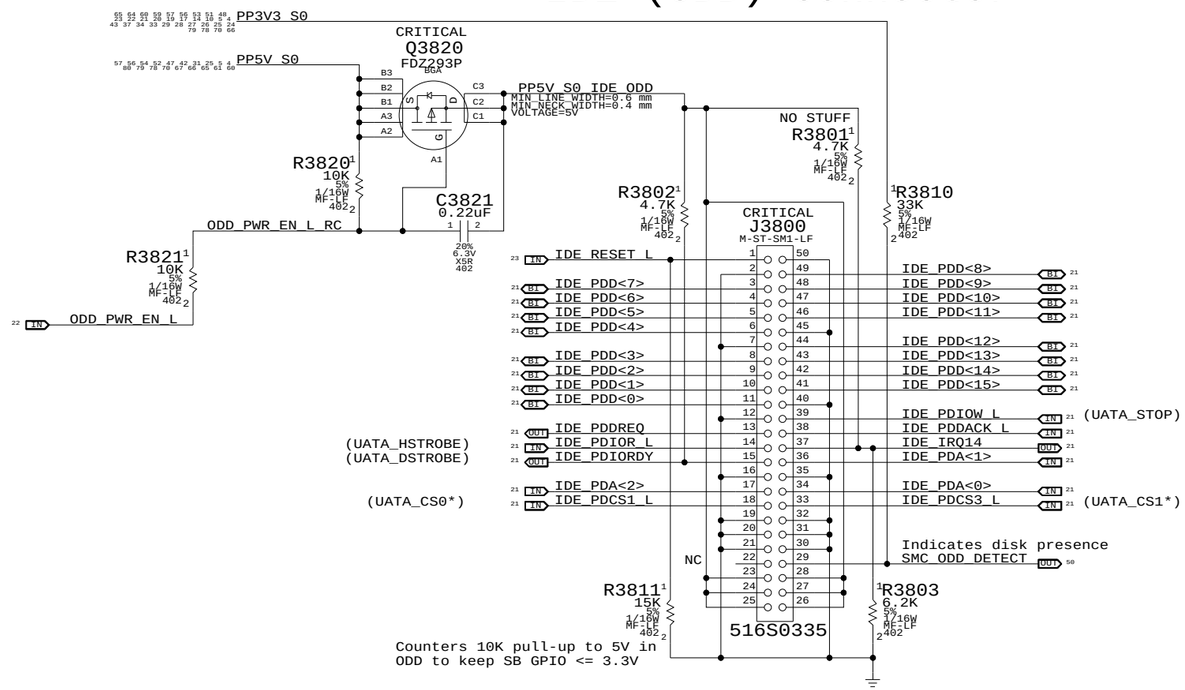
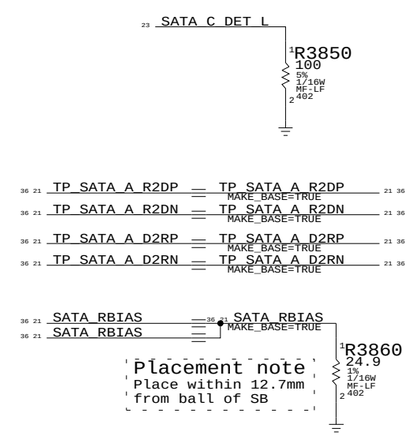
SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 35 OF 86	

IDE (ODD) Connector





PATA Connector

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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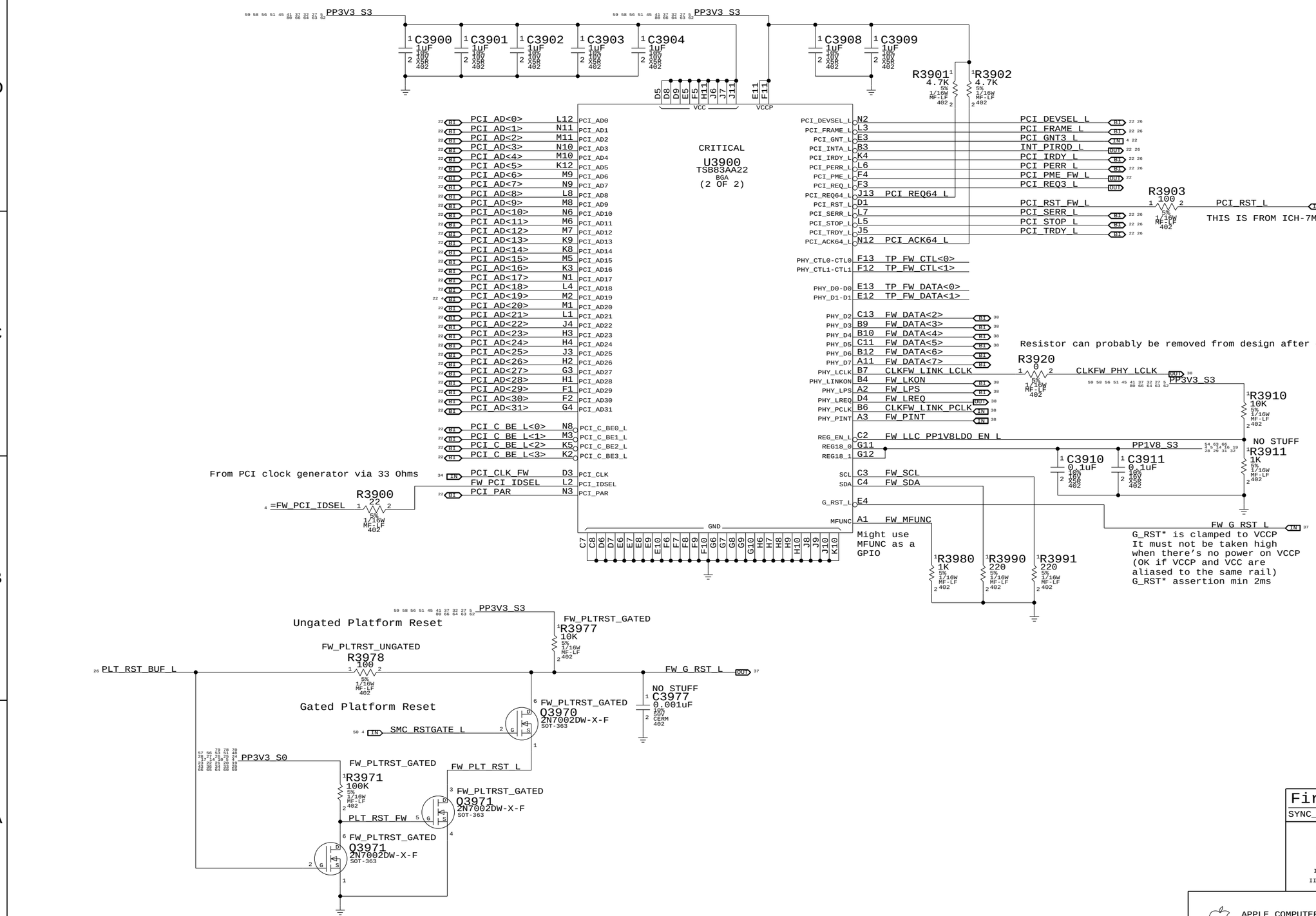
SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 36 OF 86	



FireWire Link (TSB83AA22)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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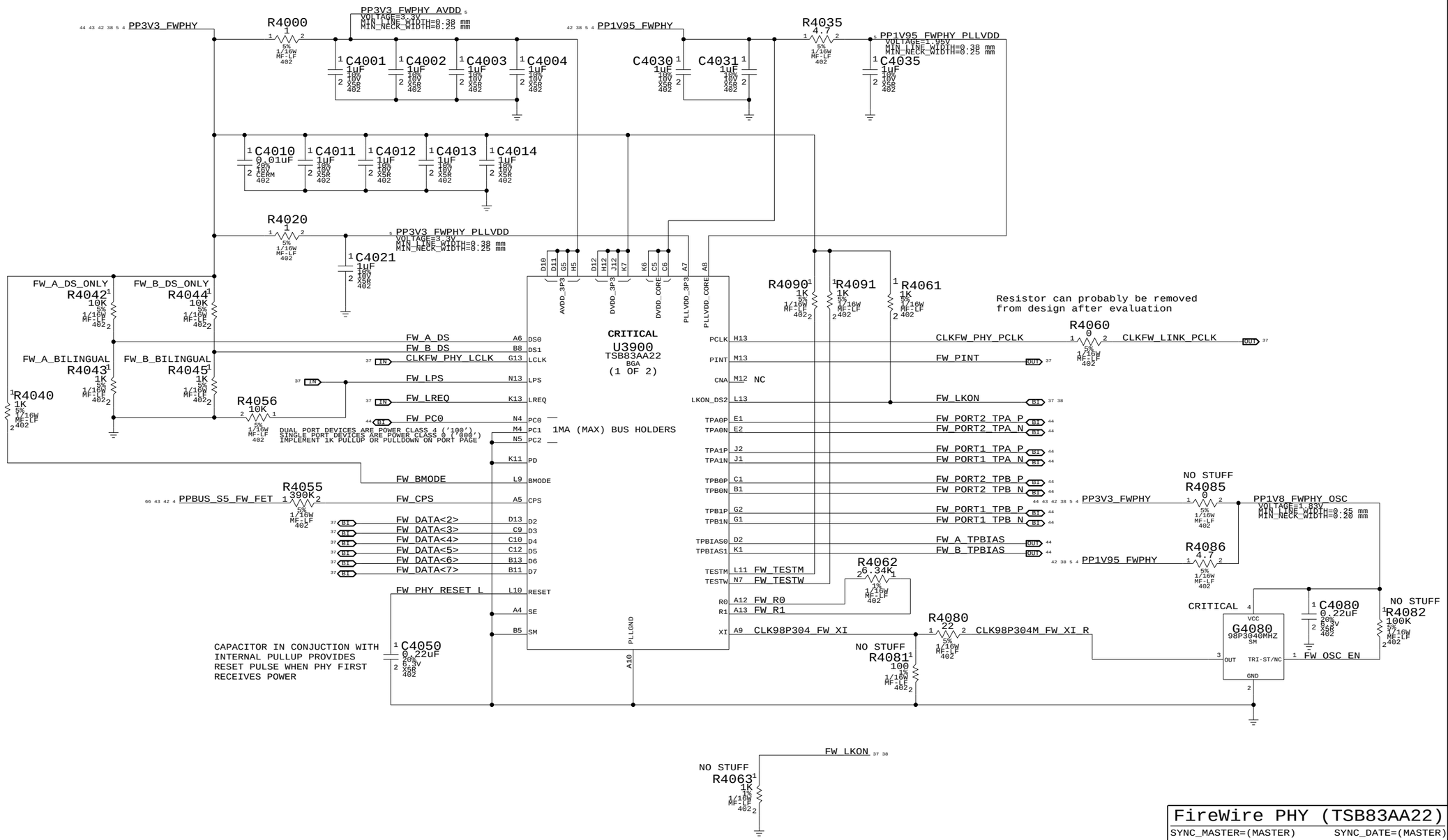
SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 37 OF 86	



FireWire PHY (TSB83AA22)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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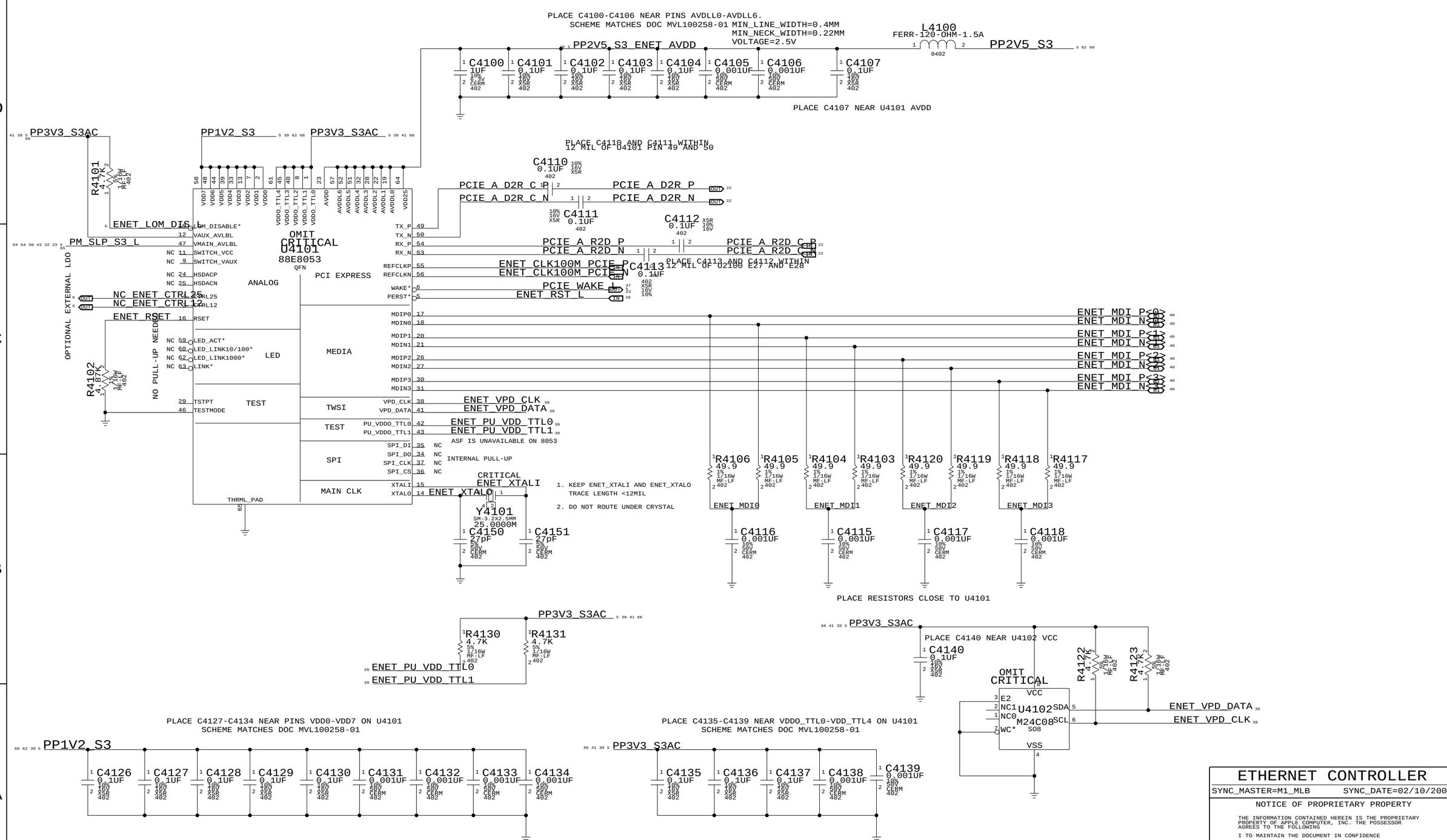
SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 38 OF 86	



ETHERNET CONTROLLER

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7023	06

SCALE NONE

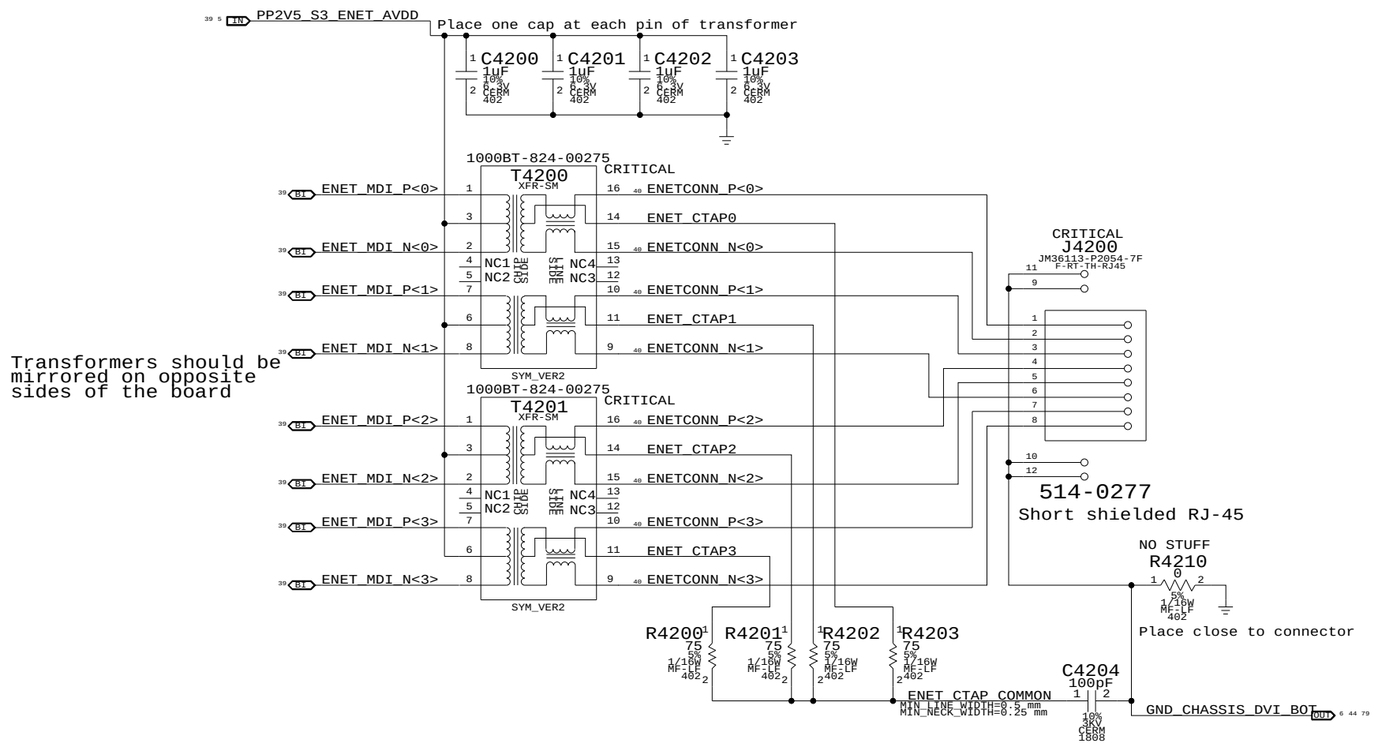
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0> 40
	ENETCONN	ENET_100D	ENETCONN_N<0> 40
	ENETCONN	ENET_100D	ENETCONN_P<1> 40
	ENETCONN	ENET_100D	ENETCONN_N<1> 40
	ENETCONN	ENET_100D	ENETCONN_P<2> 40
	ENETCONN	ENET_100D	ENETCONN_N<2> 40
	ENETCONN	ENET_100D	ENETCONN_P<3> 40
	ENETCONN	ENET_100D	ENETCONN_N<3> 40

Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Ethernet Connector

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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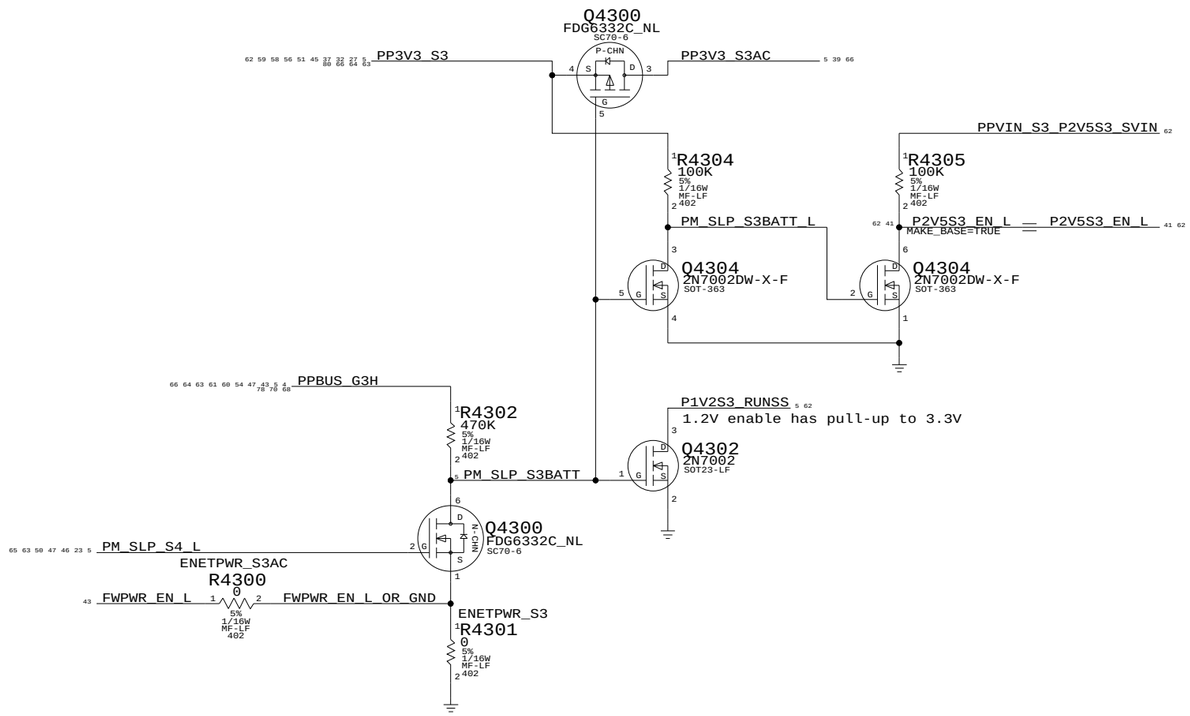
SIZE	DRAWING NUMBER	REV.
D	051-7023	06

SCALE NONE

SHT 40 OF 86

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	3.3V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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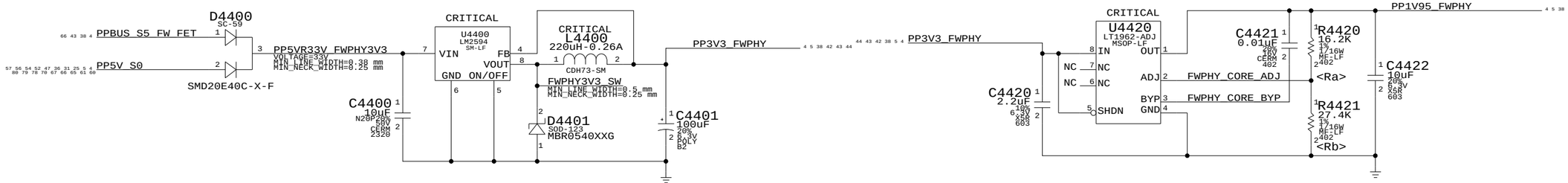
SCALE NONE SHT 41 OF 86

165MA MAX LOAD



Vout = 1.22V * (1 + Ra/Rb) + (Iadj * Ra)
Iadj = 30nA @ 25 deg C

FW PHY Power Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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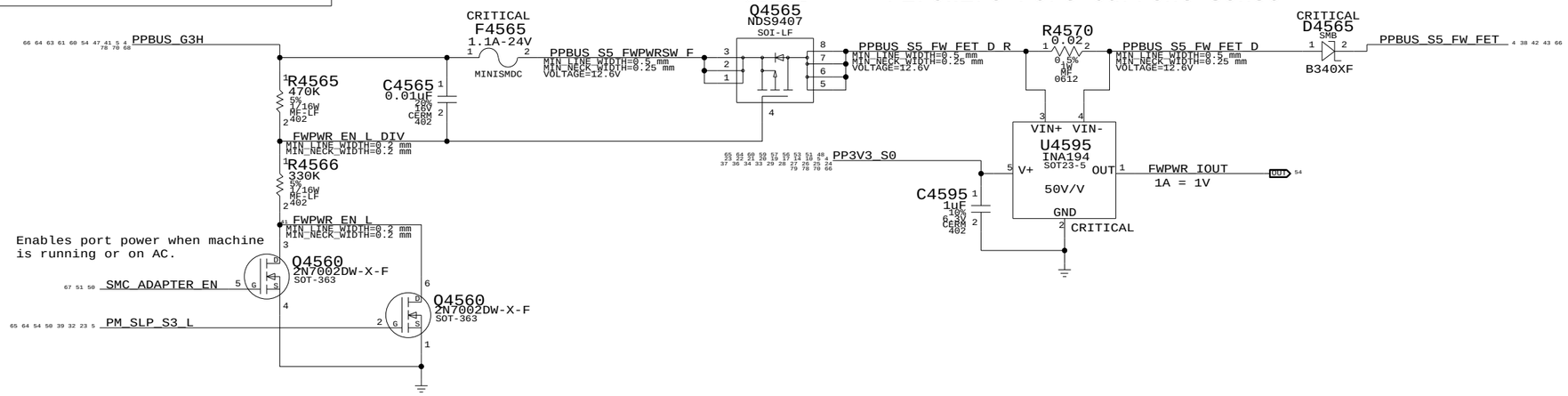
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

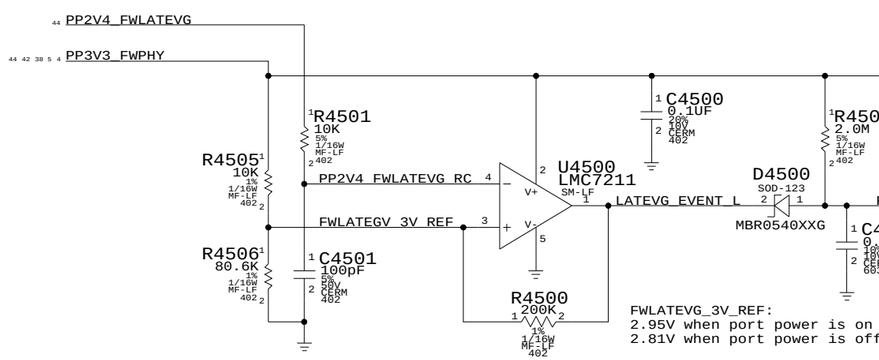
BOM options provided by this page:
(NONE)

Port Power Switch



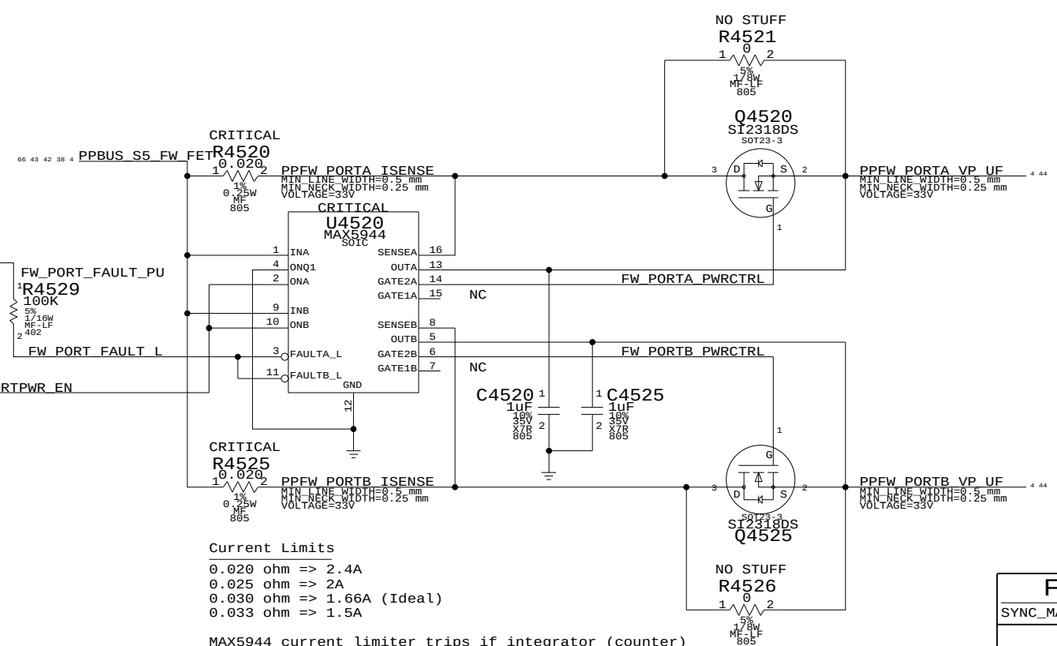
FireWire Port Current Sense

Late-VG Event Detection



FWLATEVG_3V_REF:
2.95V when port power is on
2.81V when port power is off

Current Limit/Active Late-VG Protection



Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/03/2005)

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SCALE NONE

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED	FW	FW_110D	FW_PORT1_TPA_FL_P 44
	FW	FW_110D	FW_PORT1_TPA_FL_N 44
BY	FW	FW_110D	FW_PORT1_TPB_FL_P 44
	FW	FW_110D	FW_PORT1_TPB_FL_N 44
PHY	FW	FW_110D	FW_PORT2_TPA_FL_P 44
	FW	FW_110D	FW_PORT2_TPA_FL_N 44
PAGE	FW	FW_110D	FW_PORT2_TPB_FL_P 44
	FW	FW_110D	FW_PORT2_TPB_FL_N 44

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

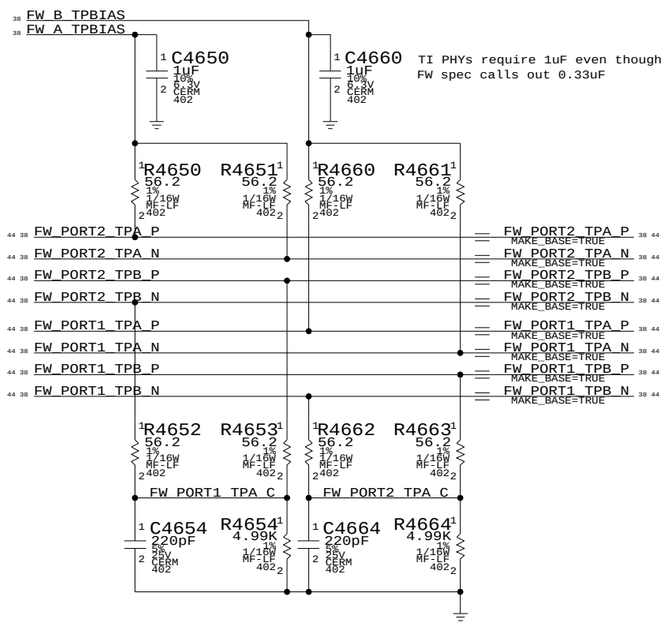
AREF needs to be isolated from all local grounds per 1394b spec

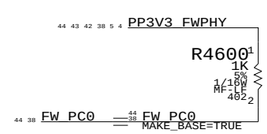
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

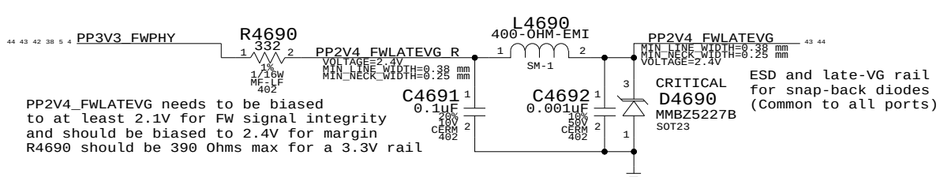
Termination

Place close to FireWire PHY





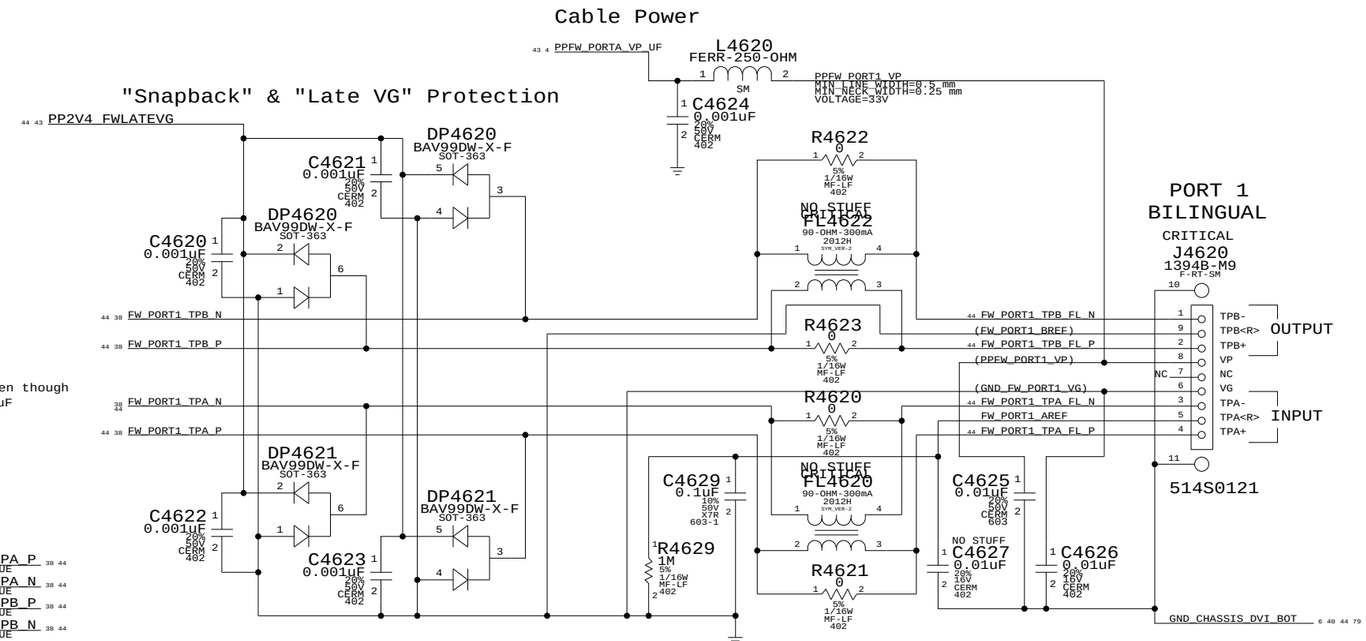
Late-VG Protection Power



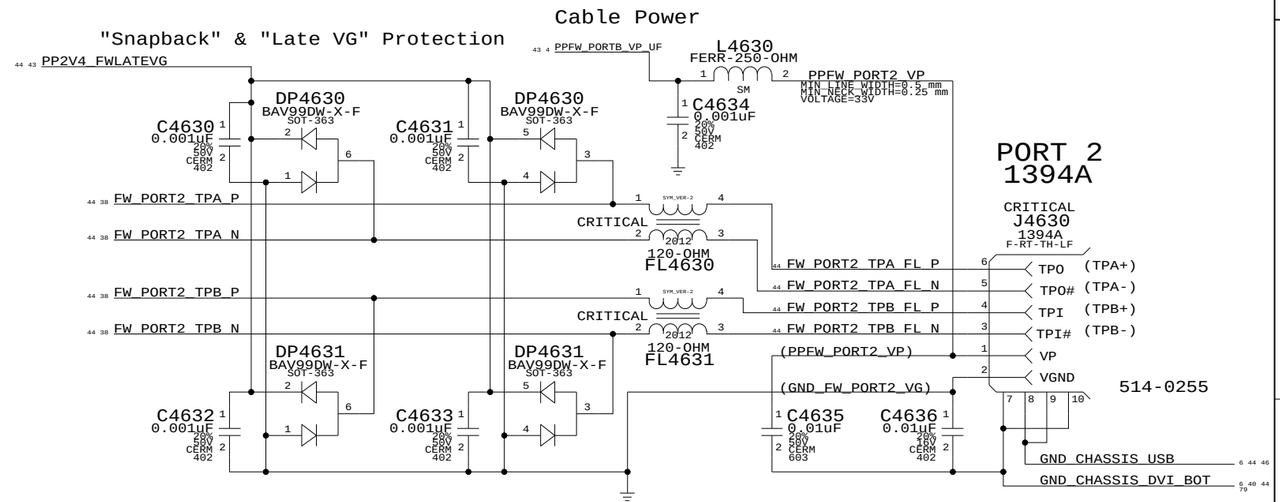
PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4690 should be 390 Ohms max for a 3.3V rail

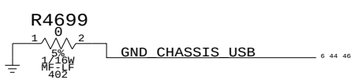
ESD and late-VG rail for snap-back diodes (Common to all ports)

"Snapback" & "Late VG" Protection



"Snapback" & "Late VG" Protection





FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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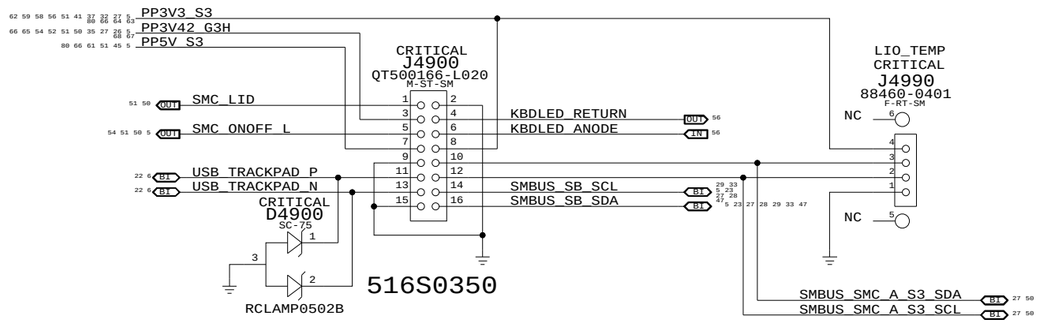
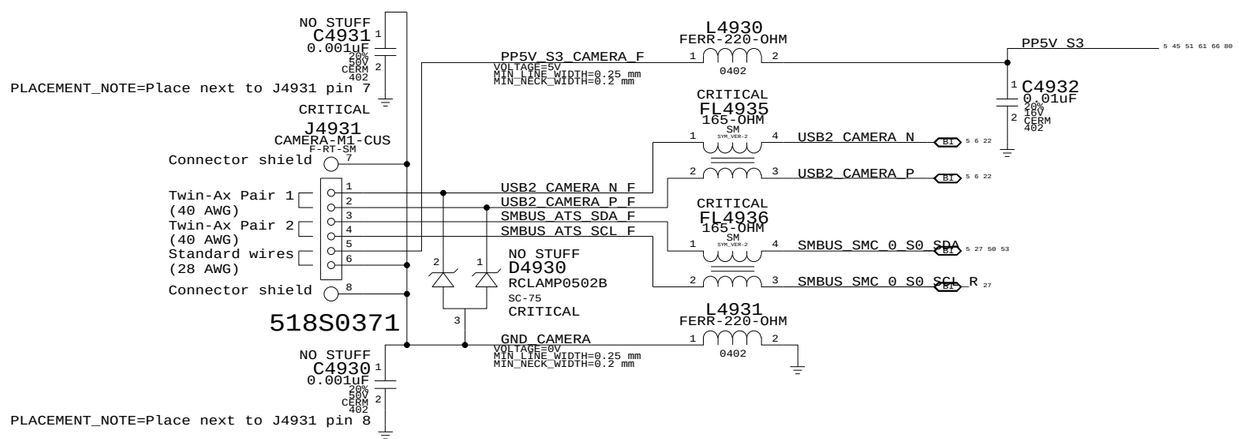
Top-Case Connector LIO Temp Sensor Connector



Camera Connector



Internal USB Connections

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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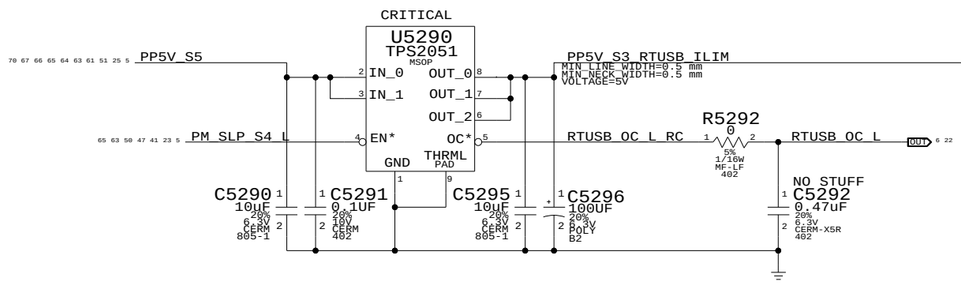
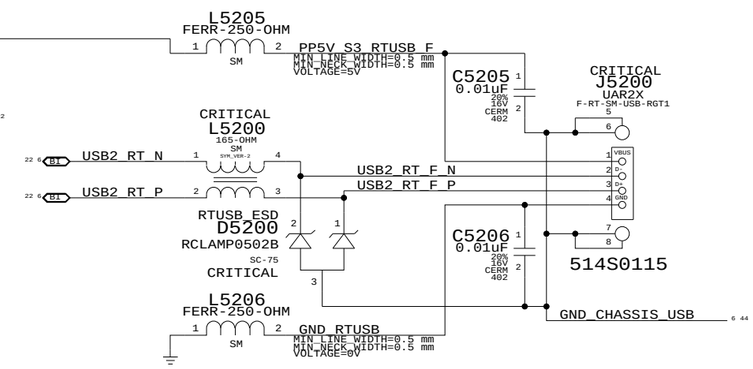
D	051-7023	06

SCALE NONE SHT 45 OF 86

Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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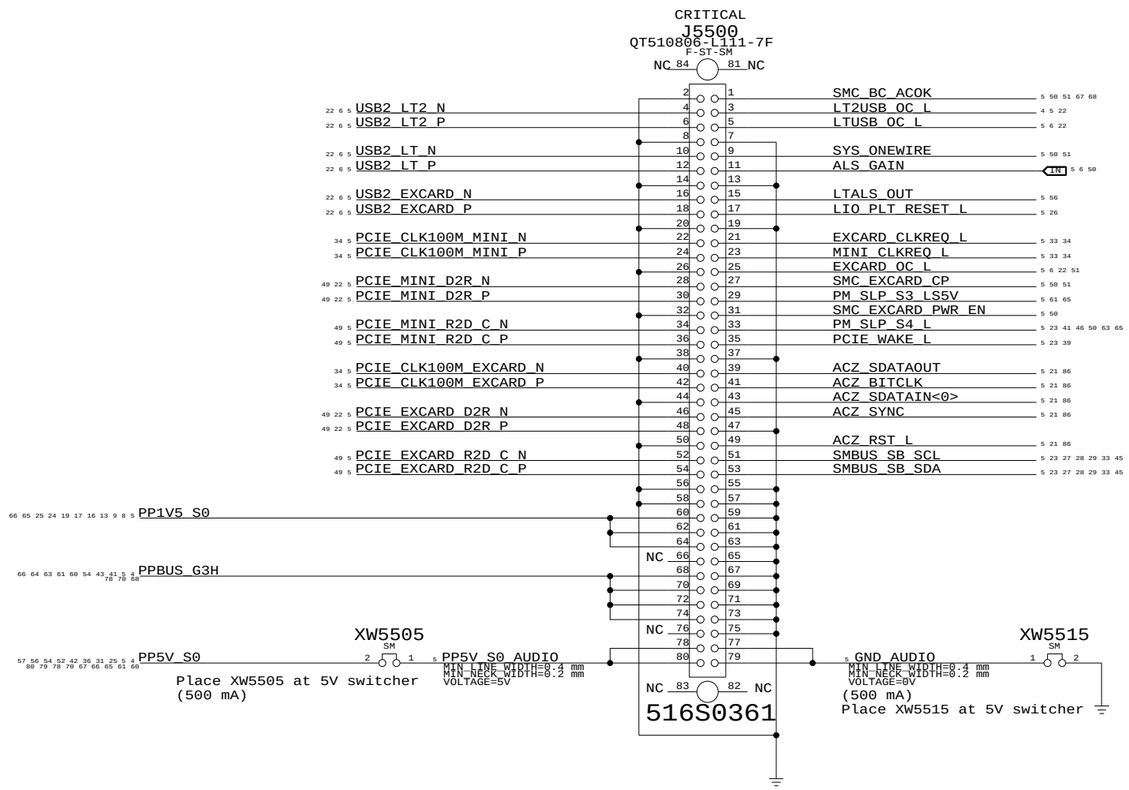
Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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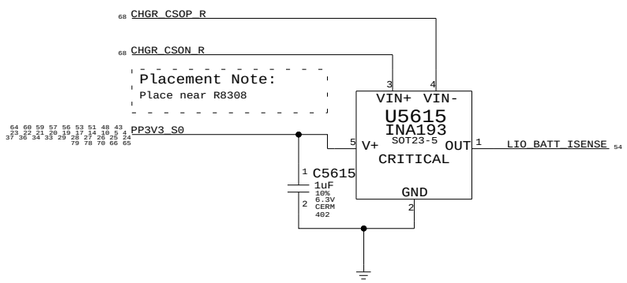
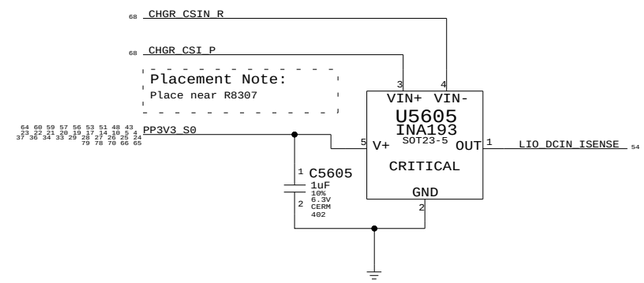
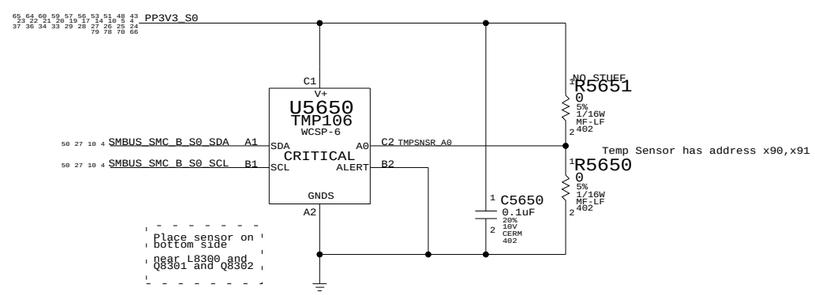
Battery Current Sense



DCIn Current Sense



TMP106 Thermal Sensor



Current & Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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PCI-E x1 Port "A" = Ethernet (Yukon)

PCI-E x1 Port "B" = PCI-E Mini Card

C5710 0.1uF 10% 16V X5R 402

C5711 0.1uF 10% 16V X5R 402

Place caps close to SB

49 47 5	PCIE_MINI_R2D_C_P	49 47 5 PCIE_MINI_R2D_C_P (MAKE_BASE=TRUE)		PCIE_B_R2D_C_P 22
49 47 5	PCIE_MINI_R2D_C_N	49 47 5 PCIE_MINI_R2D_C_N (MAKE_BASE=TRUE)		PCIE_B_R2D_C_N 22
49 47 22 5	PCIE_MINI_D2R_P	49 47 22 5 PCIE_MINI_D2R_P (MAKE_BASE=TRUE)		PCIE_MINI_D2R_P 5 22 47 49
49 47 22 5	PCIE_MINI_D2R_N	49 47 22 5 PCIE_MINI_D2R_N (MAKE_BASE=TRUE)		PCIE_MINI_D2R_N 5 22 47 49

PCI-E x1 Port "C" = ExpressCard

C5720 0.1uF 10% 16V X5R 402

C5721 0.1uF 10% 16V X5R 402

Place caps close to SB

49 47 5	PCIE_EXCARD_R2D_C_P	49 47 5 PCIE_EXCARD_R2D_C_P (MAKE_BASE=TRUE)		PCIE_C_R2D_C_P 22
49 47 5	PCIE_EXCARD_R2D_C_N	49 47 5 PCIE_EXCARD_R2D_C_N (MAKE_BASE=TRUE)		PCIE_C_R2D_C_N 22
49 47 22 5	PCIE_EXCARD_D2R_P	49 47 22 5 PCIE_EXCARD_D2R_P (MAKE_BASE=TRUE)		PCIE_EXCARD_D2R_P 5 22 47 49
49 47 22 5	PCIE_EXCARD_D2R_N	49 47 22 5 PCIE_EXCARD_D2R_N (MAKE_BASE=TRUE)		PCIE_EXCARD_D2R_N 5 22 47 49

PCI-E x1 Port "D" = Unused

49 22	TP_PCIE_D_R2DP	(MAKE_BASE=TRUE)		TP_PCIE_D_R2DP 22 49
49 22	TP_PCIE_D_R2DN	(MAKE_BASE=TRUE)		TP_PCIE_D_R2DN 22 49
49 22	TP_PCIE_D_D2RP	(MAKE_BASE=TRUE)		TP_PCIE_D_D2RP 22 49
49 22	TP_PCIE_D_D2RN	(MAKE_BASE=TRUE)		TP_PCIE_D_D2RN 22 49

PCI-E x1 Port "E" = Unused

49 22	TP_PCIE_E_R2DP	(MAKE_BASE=TRUE)		TP_PCIE_E_R2DP 22 49
49 22	TP_PCIE_E_R2DN	(MAKE_BASE=TRUE)		TP_PCIE_E_R2DN 22 49
49 22	TP_PCIE_E_D2RP	(MAKE_BASE=TRUE)		TP_PCIE_E_D2RP 22 49
49 22	TP_PCIE_E_D2RN	(MAKE_BASE=TRUE)		TP_PCIE_E_D2RN 22 49

PCI-E x1 Port "F" = Unused

49 22	TP_PCIE_F_R2DP	(MAKE_BASE=TRUE)		TP_PCIE_F_R2DP 22 49
49 22	TP_PCIE_F_R2DN	(MAKE_BASE=TRUE)		TP_PCIE_F_R2DN 22 49
49 22	TP_PCIE_F_D2RP	(MAKE_BASE=TRUE)		TP_PCIE_F_D2RP 22 49
49 22	TP_PCIE_F_D2RN	(MAKE_BASE=TRUE)		TP_PCIE_F_D2RN 22 49

PCI-E Connections

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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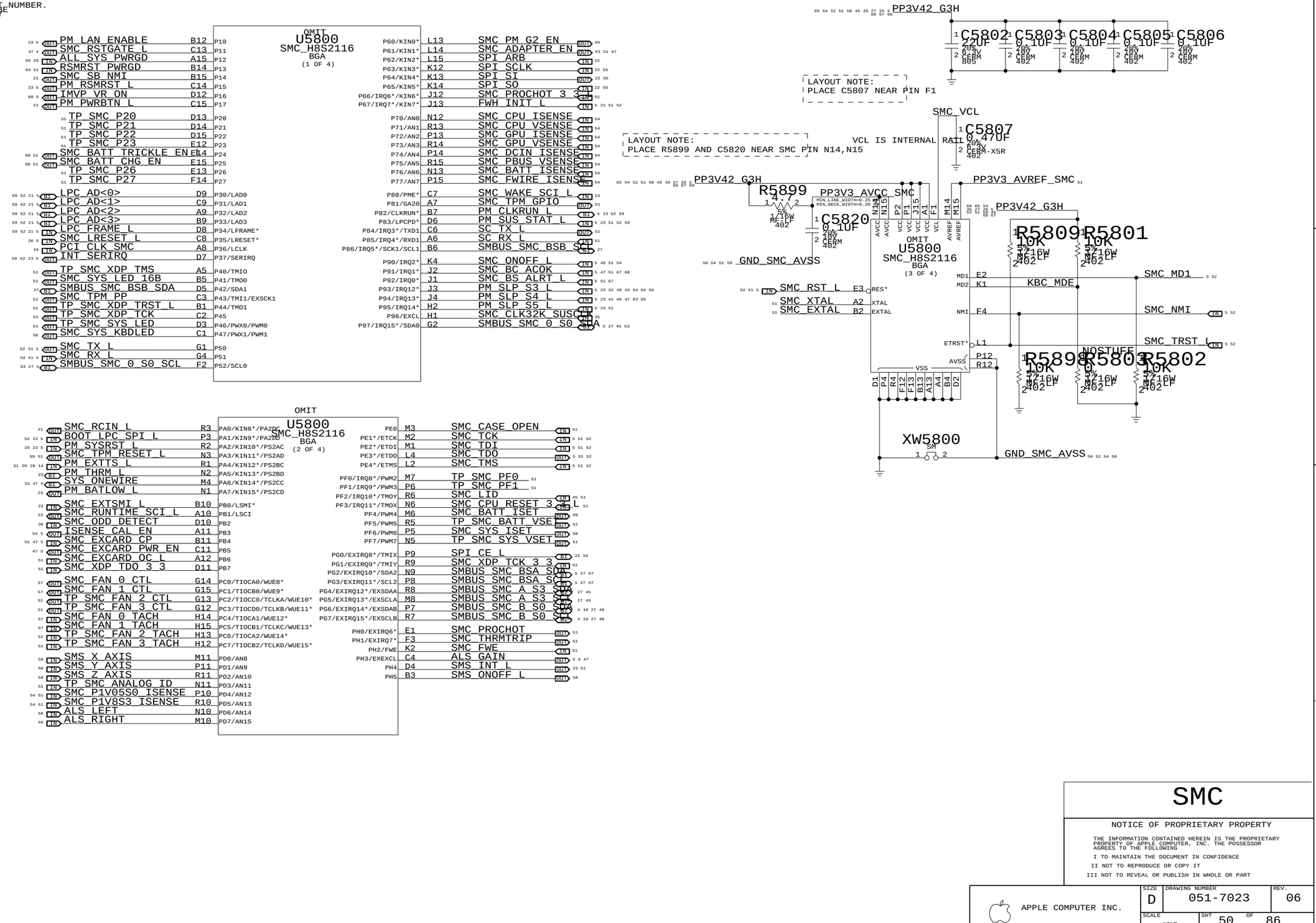
UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.



SMC

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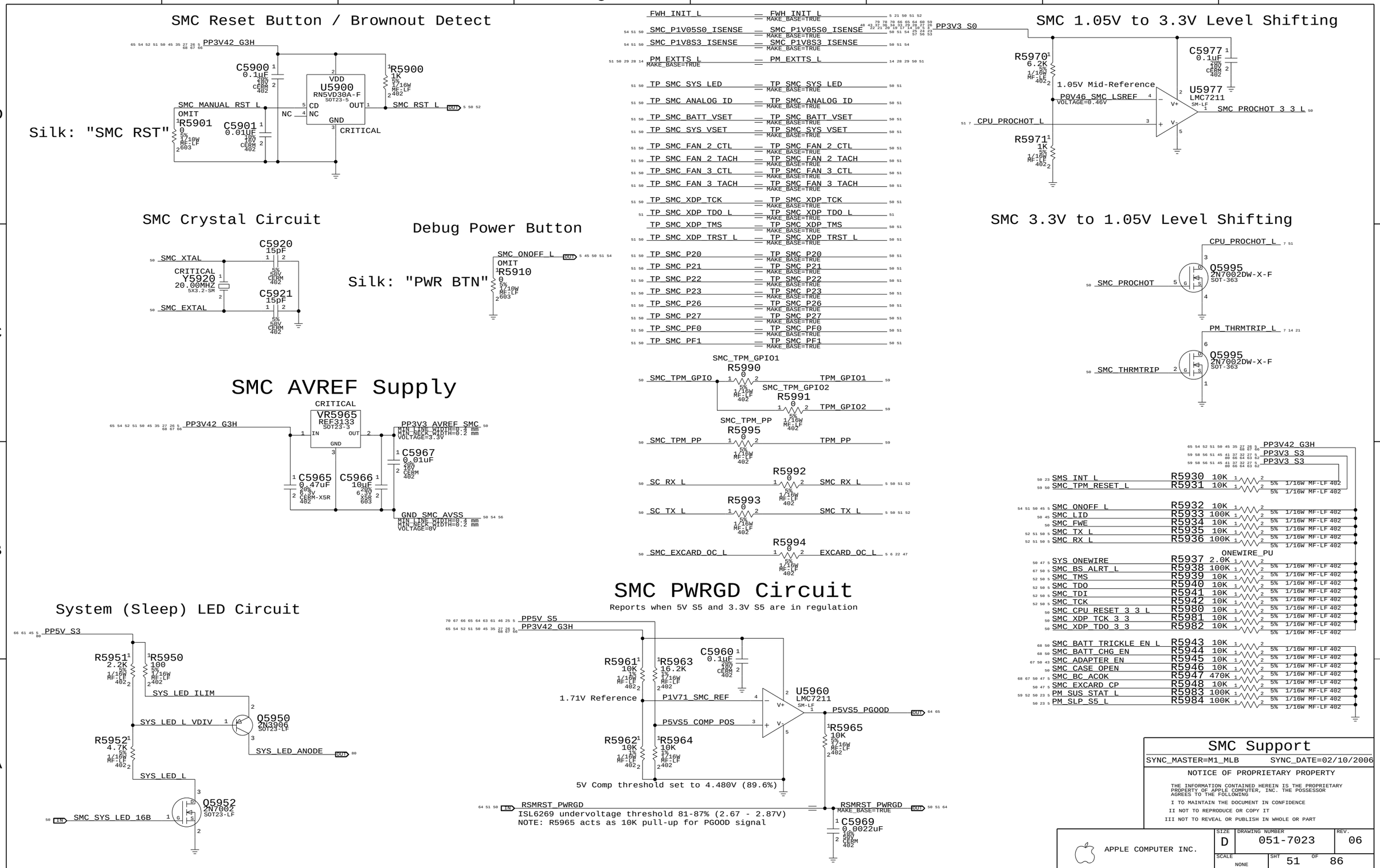
SMC Reset Button / Brownout Detect
PP3V42_G3H
C5900 0.1uF 20% 16V CERM 402
U5900 RN5VD30A-F SOT23-5
VDD CD NC OUT GND
R5900 1K 5% 1/16W MF-LF 402
SMC_MANUAL_RST_L
SMC_RST_L
CRITICAL
Silk: "SMC RST"
R5901 0 5% 1/10W MF-LF 603
C5901 0.01uF 10% 16V CERM 402
SMC 1.05V to 3.3V Level Shifting
PP3V3_S0
R5970 6.2K 5% 1/16W MF-LF 402
C5977 0.1uF 20% 16V CERM 402
1.05V Mid-Reference
P0V46_SMC_LSREF
VOLTAGE=0.46V
U5977 LMC7211 SM-LF
SMC_PROCHOT_3_3_L
CPU_PROCHOT_L
R5971 1K 5% 1/16W MF-LF 402
SMC Crystal Circuit
C5920 15pF 5% 50V CERM 402
SMC_XTAL
CRITICAL
Y5920 20.00MHZ 5X3.2-SM
C5921 15pF 5% 50V CERM 402
SMC_EXTAL
Debug Power Button
SMC_ONOFF_L
Silk: "PWR BTN"
R5910 0 5% 1/10W MF-LF 603
FWH_INIT_L
SMC_P1V05S0_ISENSE
SMC_P1V8S3_ISENSE
PM_EXTTS_L
TP_SMC_SYS_LED
TP_SMC_ANALOG_ID
TP_SMC_BATT_VSET
TP_SMC_SYS_VSET
TP_SMC_FAN_2_CTL
TP_SMC_FAN_2_TACH
TP_SMC_FAN_3_CTL
TP_SMC_FAN_3_TACH
TP_SMC_XDP_TCK
TP_SMC_XDP_TDO_L
TP_SMC_XDP_TMS
TP_SMC_XDP_TRST_L
TP_SMC_P20
TP_SMC_P21
TP_SMC_P22
TP_SMC_P23
TP_SMC_P26
TP_SMC_P27
TP_SMC_PF0
TP_SMC_PF1
MAKE_BASE=TRUE
SMC 3.3V to 1.05V Level Shifting
CPU_PROCHOT_L
Q5995 2N7002DW-X-F SOT-363
SMC_PROCHOT
PM_THRMTRIP_L
SMC_THRMTRIP
SMC_TPM_GPIO
SMC_TPM_GPIO1
R5990 0 5% 1/16W MF-LF 402
TPM_GPIO1
SMC_TPM_GPIO2
R5991 0 5% 1/16W MF-LF 402
TPM_GPIO2
SMC_TPM_PP
R5995 0 5% 1/16W MF-LF 402
TPM_PP
SC_RX_L
R5992 0 5% 1/16W MF-LF 402
SMC_RX_L
SC_TX_L
R5993 0 5% 1/16W MF-LF 402
SMC_TX_L
SMC_EXCARD_OC_L
R5994 0 5% 1/16W MF-LF 402
EXCARD_OC_L
SMC AVREF Supply
CRITICAL
VR5965 REF3133 SOT23-3
IN OUT GND
PP3V42_G3H
PP3V3_AVREF_SMC
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C5967 0.01uF 20% 16V CERM 402
C5965 0.47uF 20% 6.3V CERM-X5R 402
C5966 10uF 20% 6.3V X5R 603
GND_SMC_AVSS
VOLTAGE=0V
PP3V42_G3H
PP3V3_S3
SMS_INT_L R5930 10K 5% 1/16W MF-LF 402
SMC_TPM_RESET_L R5931 10K 5% 1/16W MF-LF 402
SMC_ONOFF_L R5932 10K 5% 1/16W MF-LF 402
SMC_LID R5933 100K 5% 1/16W MF-LF 402
SMC_FWE R5934 10K 5% 1/16W MF-LF 402
SMC_TX_L R5935 10K 5% 1/16W MF-LF 402
SMC_RX_L R5936 100K 5% 1/16W MF-LF 402
ONEWIRE_PU
SYS_ONEWIRE R5937 2.0K 5% 1/16W MF-LF 402
SMC_BS_ALRT_L R5938 100K 5% 1/16W MF-LF 402
SMC_TMS R5939 10K 5% 1/16W MF-LF 402
SMC_TDO R5940 10K 5% 1/16W MF-LF 402
SMC_TDI R5941 10K 5% 1/16W MF-LF 402
SMC_TCK R5942 10K 5% 1/16W MF-LF 402
SMC_CPU_RESET_3_3_L R5980 10K 5% 1/16W MF-LF 402
SMC_XDP_TCK_3_3 R5981 10K 5% 1/16W MF-LF 402
SMC_XDP_TDO_3_3 R5982 10K 5% 1/16W MF-LF 402
SMC_BATT_TRICKLE_EN_L R5943 10K 5% 1/16W MF-LF 402
SMC_BATT_CHG_EN R5944 10K 5% 1/16W MF-LF 402
SMC_ADAPTER_EN R5945 10K 5% 1/16W MF-LF 402
SMC_CASE_OPEN R5946 10K 5% 1/16W MF-LF 402
SMC_BC_ACOK R5947 470K 5% 1/16W MF-LF 402
SMC_EXCARD_CP R5948 10K 5% 1/16W MF-LF 402
PM_SUS_STAT_L R5983 100K 5% 1/16W MF-LF 402
PM_SLP_S5_L R5984 100K 5% 1/16W MF-LF 402
System (Sleep) LED Circuit
PP5V_S3
R5951 2.2K 5% 1/16W MF-LF 402
R5950 100 5% 1/16W MF-LF 402
SYS_LED_ILIM
SYS_LED_L_VDIV
Q5950 2N3906 SOT23-LF
SYS_LED_ANODE
R5952 4.7K 5% 1/16W MF-LF 402
SYS_LED_L
Q5952 2N7002 SOT23-LF
SMC_SYS_LED_16B
SMC PWRGD Circuit
Reports when 5V S5 and 3.3V S5 are in regulation
PP5V_S5
PP3V42_G3H
C5960 0.1uF 20% 16V CERM 402
R5961 10K 1% 1/16W MF-LF 402
R5963 16.2K 1% 1/16W MF-LF 402
1.71V Reference
P1V71_SMC_REF
U5960 LMC7211 SM-LF
P5VS5_PGOOD
P5VS5_COMP_POS
R5962 10K 1% 1/16W MF-LF 402
R5964 10K 1% 1/16W MF-LF 402
R5965 10K 5% 1/16W MF-LF 402
5V Comp threshold set to 4.480V (89.6%)
RSMRST_PWRGD
ISL6269 undervoltage threshold 81-87% (2.67 - 2.87V)
NOTE: R5965 acts as 10K pull-up for PGOOD signal
C5969 0.0022uF 10% 50V CERM 402
SMC Support
SYNC_MASTER=M1_MLB
SYNC_DATE=02/10/2006
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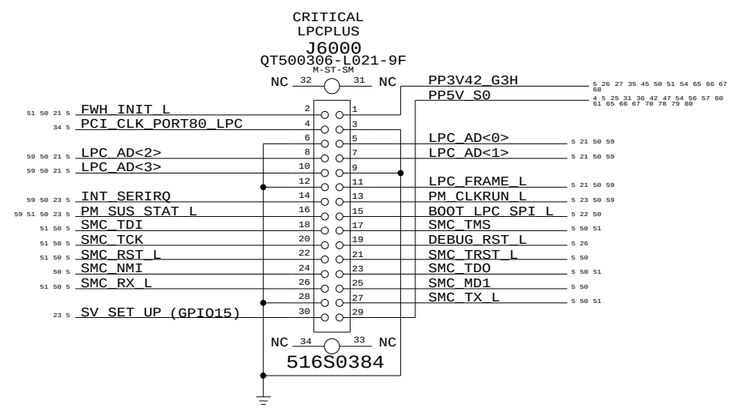
SIZE D
DRAWING NUMBER 051-7023
REV. 06
SCALE NONE
SHT 51 OF 86



LPC+ Debug Connector

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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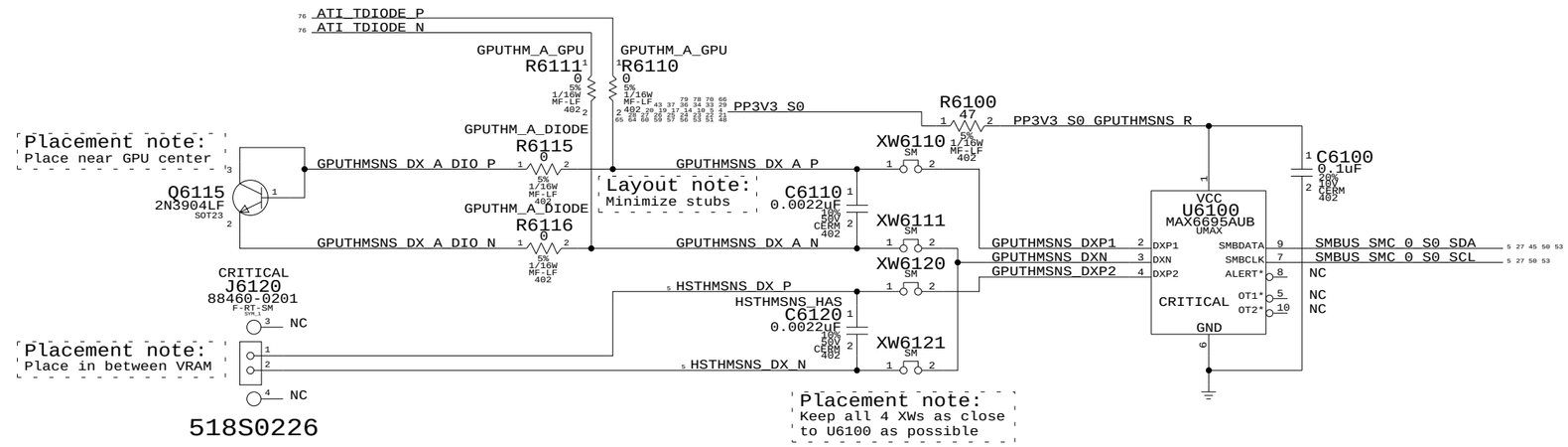
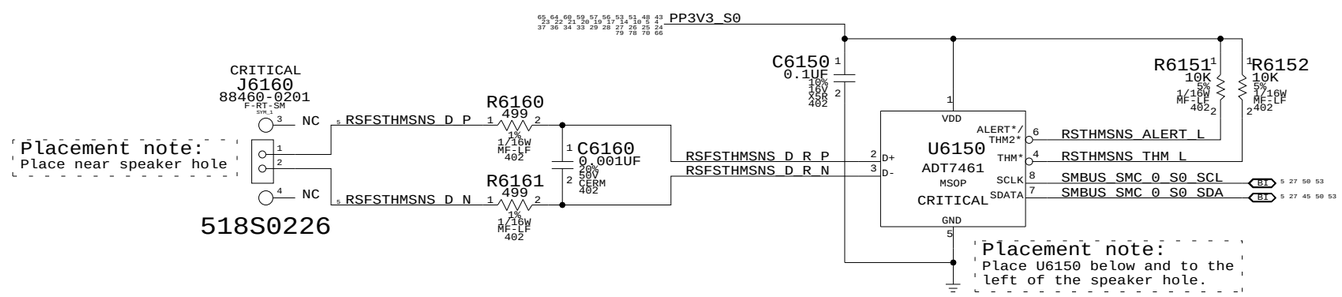
SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 52 OF 86	

GPU / Heat Pipe Thermal Sensor

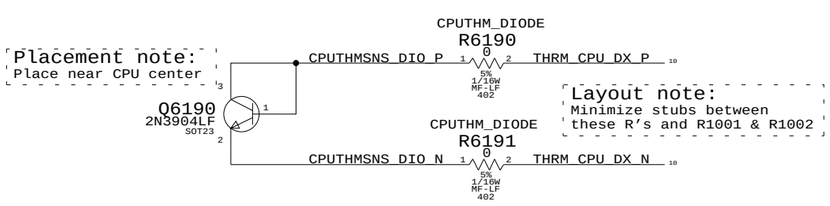


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

Thermal Sensors

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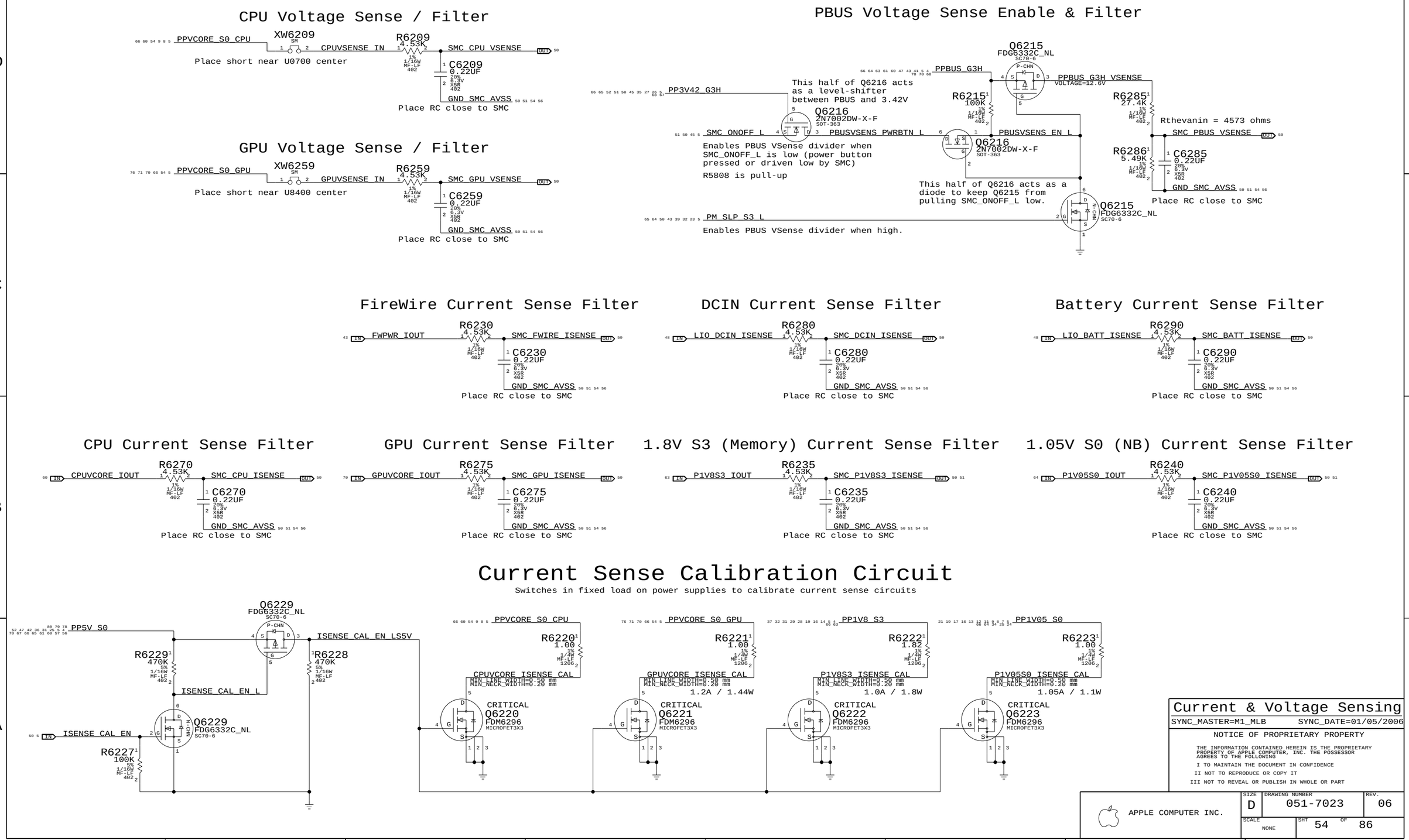
D	051-7023	06

SCALE NONE SHT 53 OF 86


CPU Voltage Sense / Filter
PPVCORE_S0_CPU
XW6209
CPUVSENSE_IN
R6209 4.53K
SMC_CPU_VSENSE
Place short near U0700 center
C6209 0.22UF
GND_SMC_AVSS
Place RC close to SMC
GPU Voltage Sense / Filter
PPVCORE_S0_GPU
XW6259
GPUVSENSE_IN
R6259 4.53K
SMC_GPU_VSENSE
Place short near U8400 center
C6259 0.22UF
GND_SMC_AVSS
Place RC close to SMC
PBUS Voltage Sense Enable & Filter
Q6215 FDG6332C_NL
PPBUS_G3H
PPBUS_G3H_VSENSE
VOLTAGE=12.6V
PP3V42_G3H
This half of Q6216 acts as a level-shifter between PBUS and 3.42V
Q6216 2N7002DW-X-F
R6215 100K
R6285 27.4K
Rthevanin = 4573 ohms
SMC_PBUS_VSENSE
SMC_ONOFF_L
PBUSVSENS_PWRBTN_L
PBUSVSENS_EN_L
Enables PBUS VSense divider when SMC_ONOFF_L is low (power button pressed or driven low by SMC)
R5808 is pull-up
R6286 5.49K
C6285 0.22UF
GND_SMC_AVSS
Place RC close to SMC
This half of Q6216 acts as a diode to keep Q6215 from pulling SMC_ONOFF_L low.
PM_SLP_S3_L
Enables PBUS VSense divider when high.
FireWire Current Sense Filter
FWPWR_IOUT
R6230 4.53K
SMC_FWIRE_ISENSE
C6230 0.22UF
GND_SMC_AVSS
Place RC close to SMC
DCIN Current Sense Filter
LIO_DCIN_ISENSE
R6280 4.53K
SMC_DCIN_ISENSE
C6280 0.22UF
GND_SMC_AVSS
Place RC close to SMC
Battery Current Sense Filter
LIO_BATT_ISENSE
R6290 4.53K
SMC_BATT_ISENSE
C6290 0.22UF
GND_SMC_AVSS
Place RC close to SMC
CPU Current Sense Filter
CPUVCORE_IOUT
R6270 4.53K
SMC_CPU_ISENSE
C6270 0.22UF
GND_SMC_AVSS
Place RC close to SMC
GPU Current Sense Filter
GPUVCORE_IOUT
R6275 4.53K
SMC_GPU_ISENSE
C6275 0.22UF
GND_SMC_AVSS
Place RC close to SMC
1.8V S3 (Memory) Current Sense Filter
P1V8S3_IOUT
R6235 4.53K
SMC_P1V8S3_ISENSE
C6235 0.22UF
GND_SMC_AVSS
Place RC close to SMC
1.05V S0 (NB) Current Sense Filter
P1V05S0_IOUT
R6240 4.53K
SMC_P1V05S0_ISENSE
C6240 0.22UF
GND_SMC_AVSS
Place RC close to SMC
Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits
PP5V_S0
Q6229 FDG6332C_NL
ISENSE_CAL_EN_LS5V
R6229 470K
R6228 470K
ISENSE_CAL_EN_L
ISENSE_CAL_EN
R6227 100K
PPVCORE_S0_CPU
R6220 1.00
CPUVCORE_ISENSE_CAL
MIN_LINE_WIDTH=0.50 mm
MIN_NECK_WIDTH=0.20 mm
CRITICAL
Q6220 FDM6296 MICROFET3X3
PPVCORE_S0_GPU
R6221 1.00
GPUVCORE_ISENSE_CAL
1.2A / 1.44W
Q6221 FDM6296 MICROFET3X3
PP1V8_S3
R6222 1.82
P1V8S3_ISENSE_CAL
1.0A / 1.8W
Q6222 FDM6296 MICROFET3X3
PP1V05_S0
R6223 1.00
P1V05S0_ISENSE_CAL
1.05A / 1.1W
Q6223 FDM6296 MICROFET3X3
Current & Voltage Sensing
SYNC_MASTER=M1_MLB
SYNC_DATE=01/05/2006
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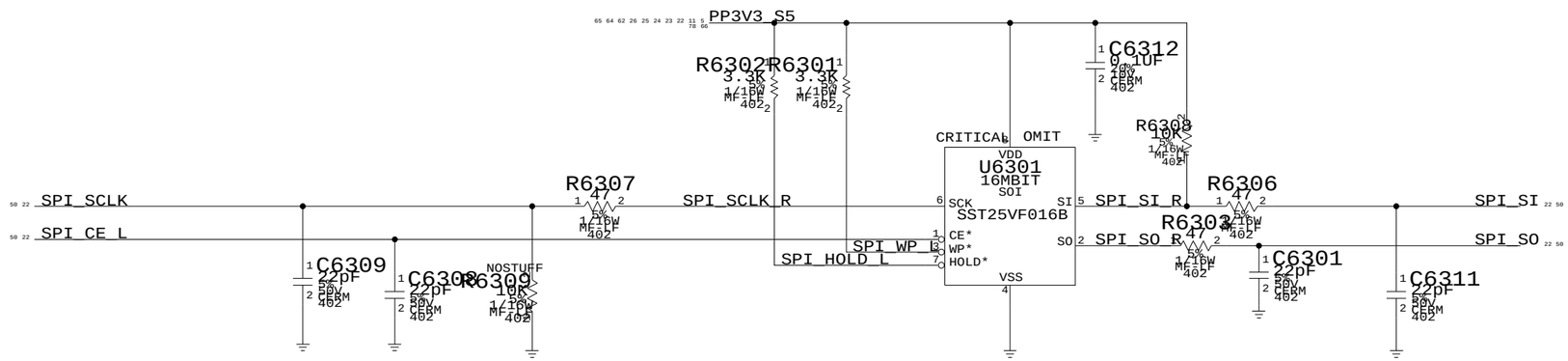
REV. 06
SCALE NONE
SHT 54 OF 86



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=M$YNC_DATE=02/10/2006

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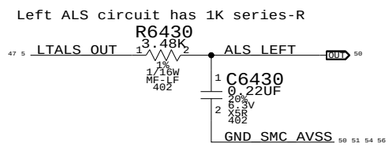
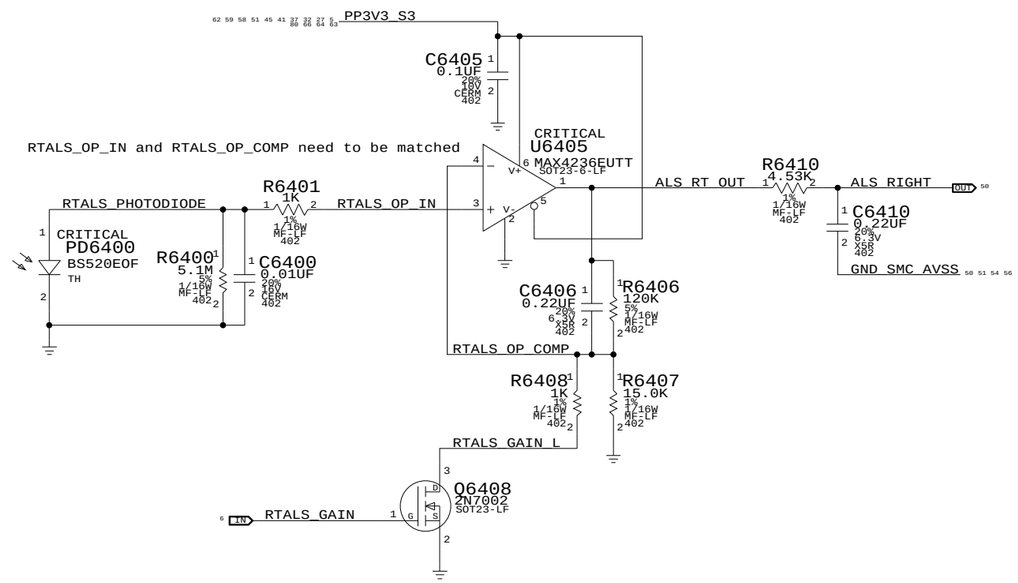
SCALE NONE

SHT 55 OF 86

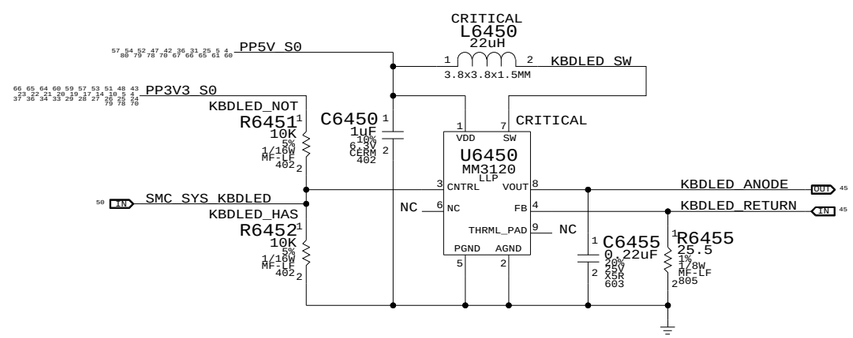
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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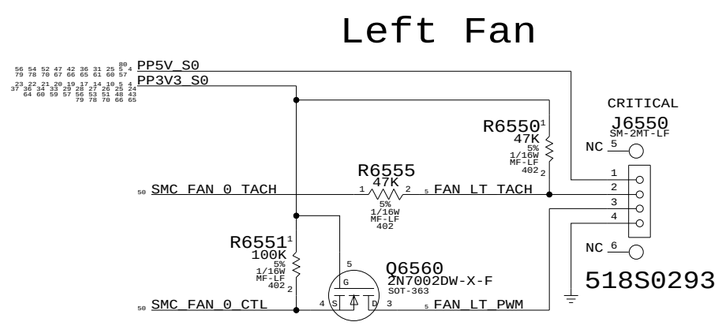
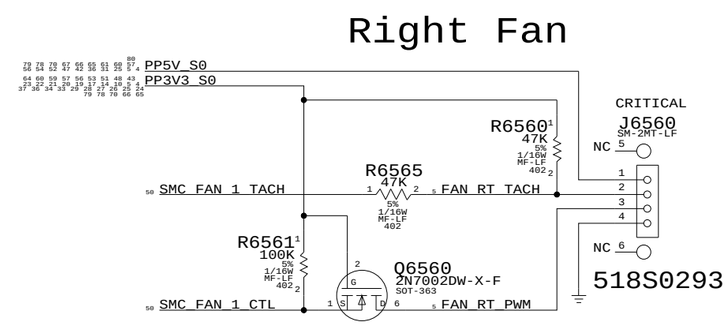
SCALE NONE	SHT 56 OF 86	





Fan Connectors

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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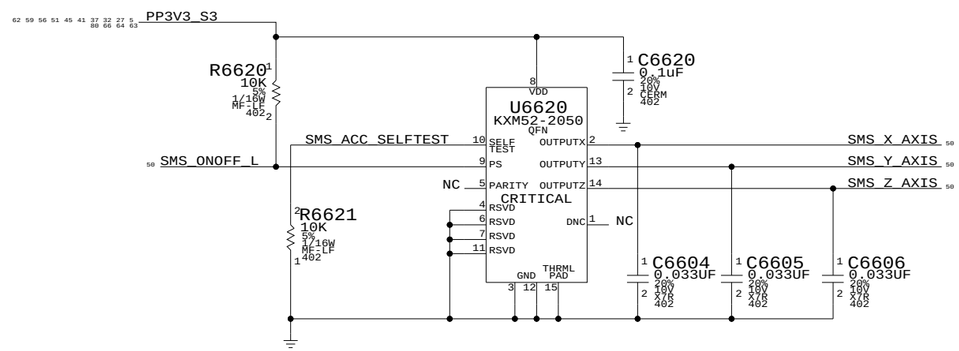
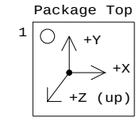
SCALE NONE	SHT 57 OF 86	



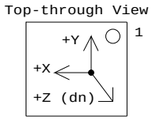
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



M1 placement: Bottom-side

Sudden Motion Sensor (SMS)

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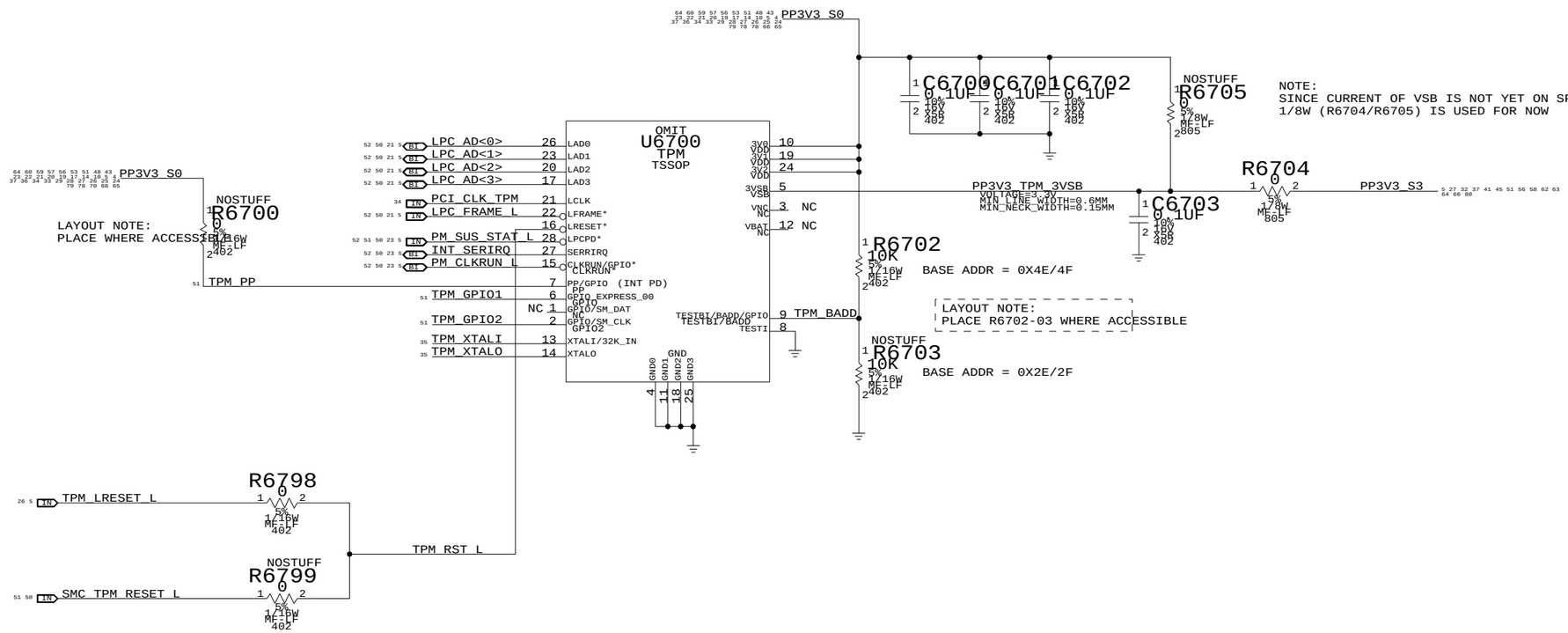
SCALE NONE

SHT 58 OF 86



TPM

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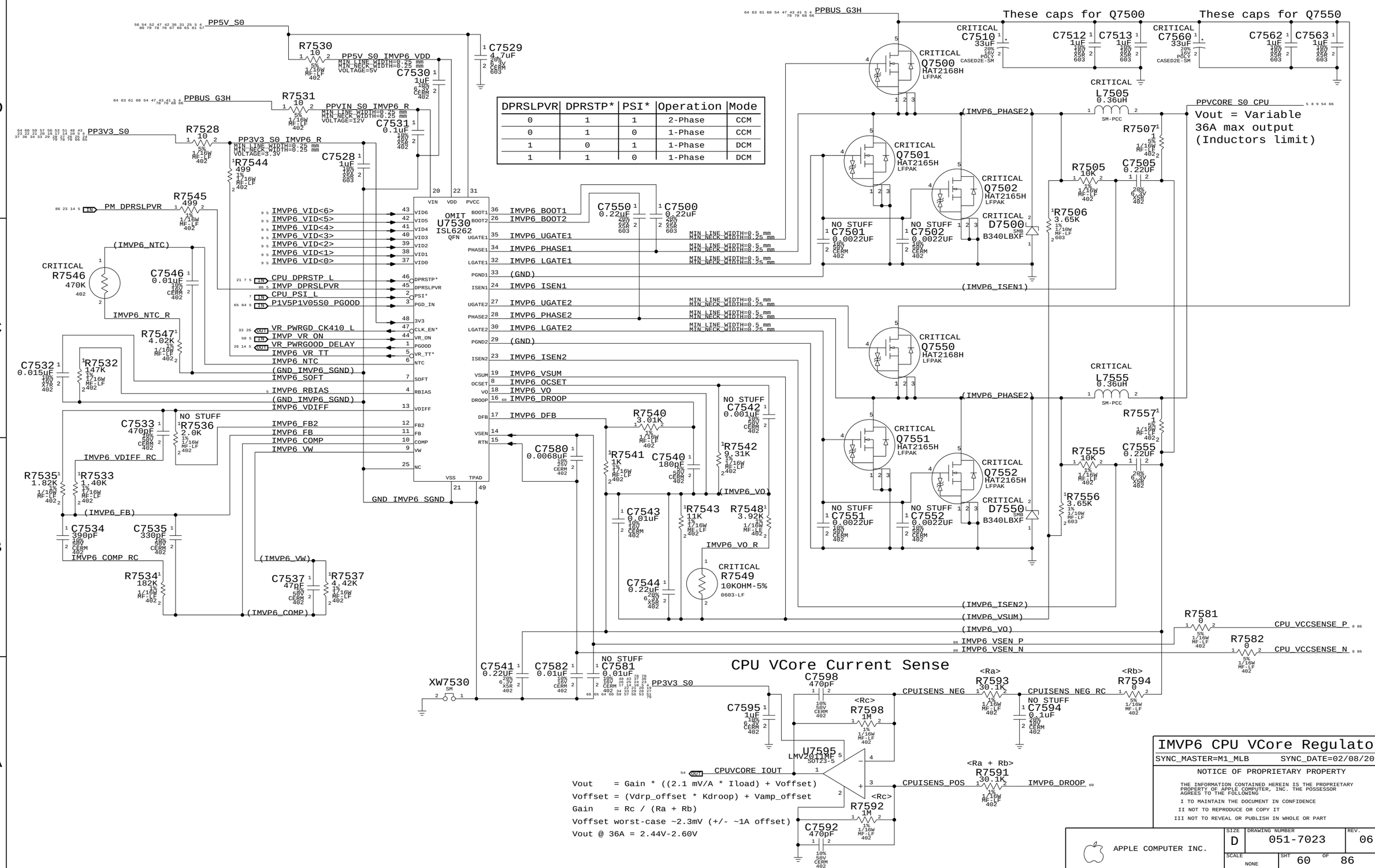
SCALE NONE

SHT 59 OF 86



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

IMVP6 CPU VCore Regulator

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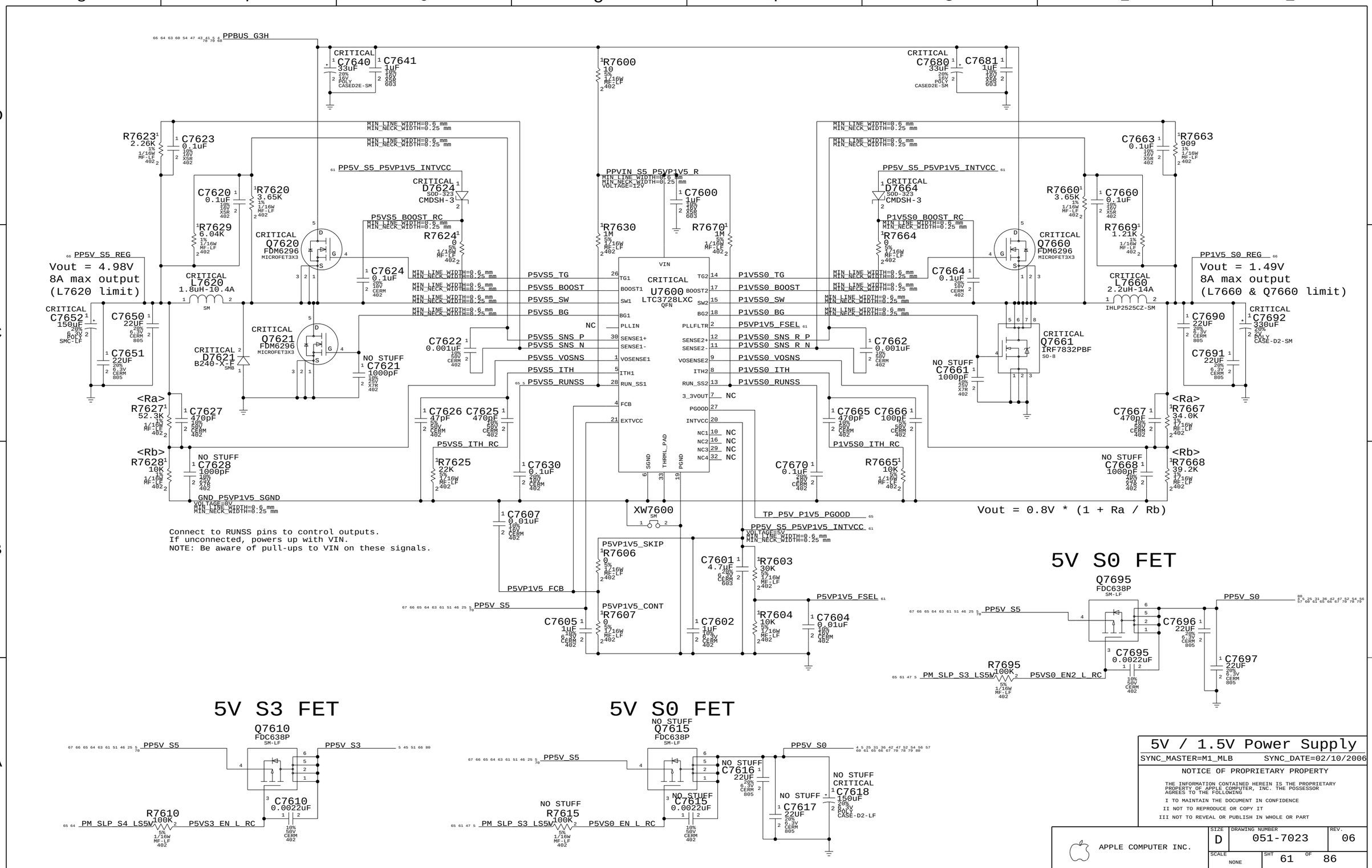
SCALE NONE SHT 60 OF 86


PPBUS_G3H
Vout = 4.98V
8A max output
(L7620 limit)
PP5V_S5_REG
Vout = 1.49V
8A max output
(L7660 & Q7660 limit)
PP1V5_S0_REG
U7600
LTC3728LXC
QFN
Vout = 0.8V * (1 + Ra / Rb)
Connect to RUNSS pins to control outputs.
If unconnected, powers up with VIN.
NOTE: Be aware of pull-ups to VIN on these signals.
5V S0 FET
5V S3 FET
5V S0 FET
5V / 1.5V Power Supply
SYNC_MASTER=M1_MLB
SYNC_DATE=02/10/2006
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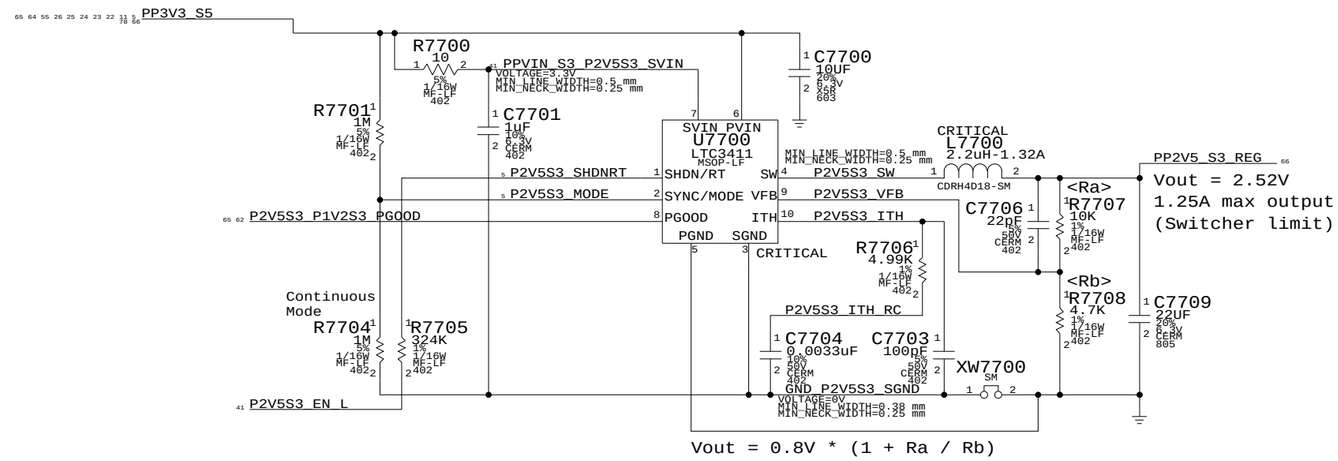
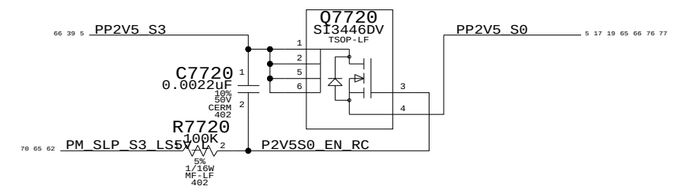
REV. 06
SCALE NONE
SHT 61 OF 86

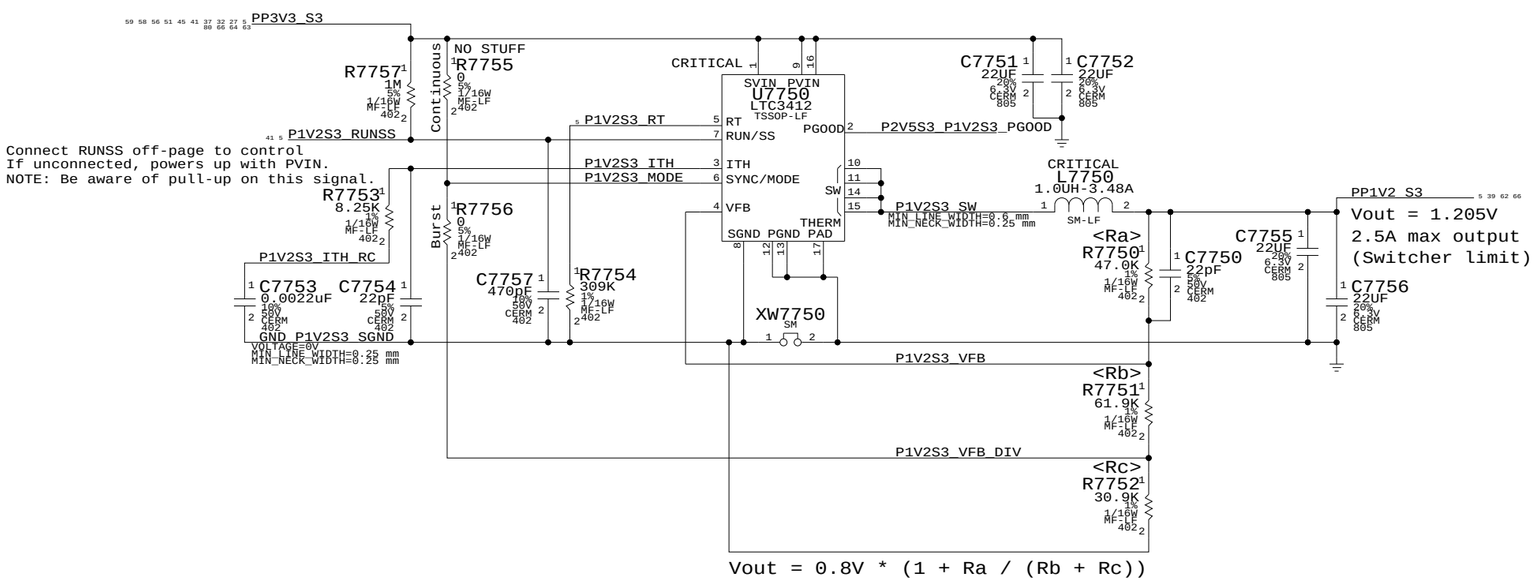
2.5V S3 Regulator



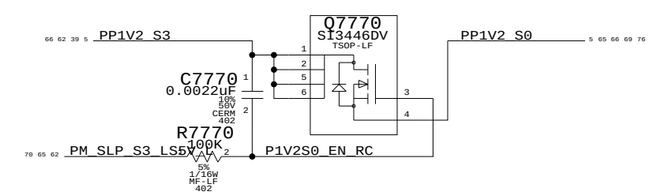
2.5V S0 FET



1.2V S3 Regulator



1.2V S0 FET



2.5V & 1.2V Regulators

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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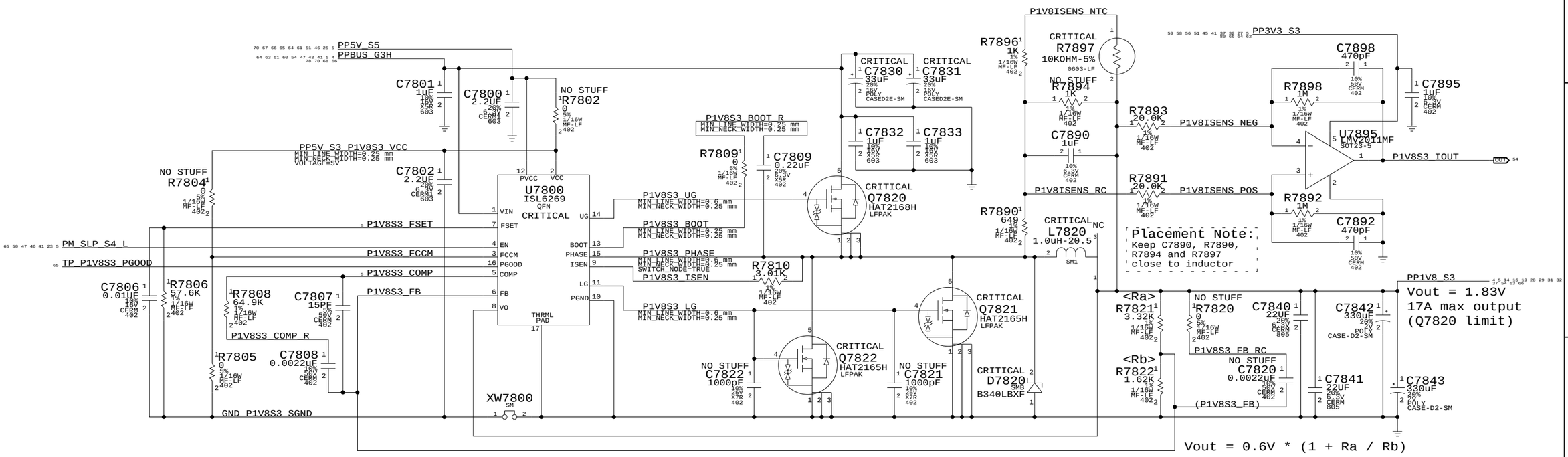
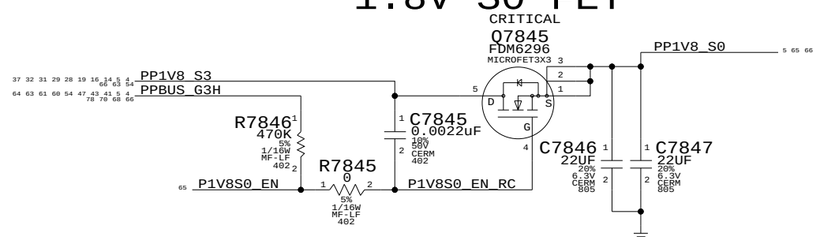
SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 62 OF 86	

1.8V S3 Current Sense



1.8V S0 FET



1.8V Supply

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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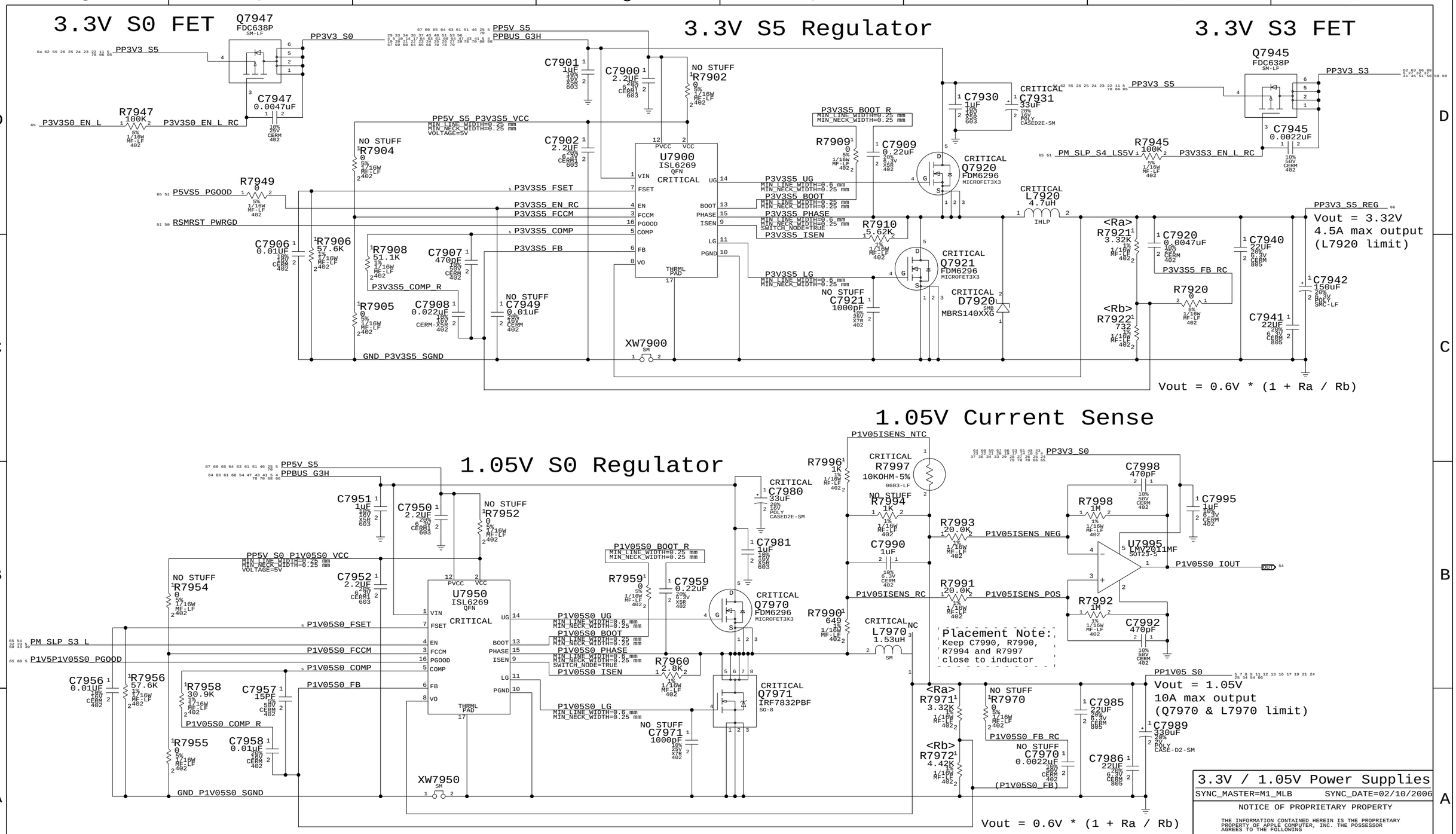
D	051-7023	06
SCALE NONE	SHT 63 OF 86	



3.3V / 1.05V Power Supplies

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 64 OF 86	

Power Control Signals

PP5V_S5

R8050 10K 5% 1/10W MF-LF 402
R8051 10K 5% 1/10W MF-LF 402
R8052 10K 5% 1/10W MF-LF 402

GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up.

PM_SLP_S3_LS5V_L (IN)

Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.

PM_SLP_S3_LS5V_L (MAKE_BASE=TRUE) — PM_SLP_S3_LS5V_L, PM_SLP_S3_LS5V_L
P3V3S0_EN_L (MAKE_BASE=TRUE) — P3V3S0_EN_L
P1V8S0_EN (MAKE_BASE=TRUE) — P1V8S0_EN

1.8V Enable has pull-up to PBUS

Q8055 2N7002DW-X-F SOT-363
Q8056 2N7002DW-X-F SOT-363
Q8050 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V (MAKE_BASE=TRUE) — PM_SLP_S3_LS5V, PM_SLP_S3_LS5V

PP3V42_G3H

Q8050 2N7002DW-X-F SOT-363
R8054 100K 5% 1/16W MF-LF 402

P1V5S0_RUNSS

1.5V Enable has pull-up to PBUS

Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3

Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3_L (IN)

R8056 100K 5% 1/10W MF-LF 402

PM_SLP_S3_L, PM_SLP_S3_L, PM_SLP_S3_L, PM_SLP_S3_L

(PM_SLP_S3_L) (MAKE_BASE=TRUE)

R8053 10K 5% 1/16W MF-LF 402

P2V5S3_P1V2S3_PGOOD (IN)
P2V5S3_P1V2S3_PGOOD (IN)

NO STUFF
R8060 0 5% 1/16W 402

P2V5S3_P1V2S3_PGOOD (MAKE_BASE=TRUE)

GPUVCORE_EN (MAKE_BASE=TRUE) — GPUVCORE_EN

Ensure 1.2V and 2.5V S3 supplies are up before enabling GPU VCore to support removing ethernet power in battery sleep.

PP5V_S5

R8055 10K 5% 1/10W MF-LF 402

PM_SLP_S4_LS5V (MAKE_BASE=TRUE) — PM_SLP_S4_LS5V, PM_SLP_S4_LS5V

Q8055 2N7002DW-X-F SOT-363

PM_SLP_S4_L (IN)

R8057 100K 5% 1/10W MF-LF 402

2.5V S3 and 1.2V S3 supplies are controlled by ethernet power control circuit.

(PM_SLP_S4_L) (MAKE_BASE=TRUE) — PM_SLP_S4_L, PM_SLP_S4_L, PM_SLP_S4_L

PP3V42_G3H

P5VS5_PGOOD (IN)

(P5VS5_PGOOD) (MAKE_BASE=TRUE) — P5VS5_PGOOD

R8059 470K 5% 1/10W MF-LF 402

P5VS5_RUNSS

5V Enable has pull-up to PBUS

SMC_PM_G2_EN_L — Q8059 2N7002DW-X-F SOT-363

Q8059 2N7002DW-X-F SOT-363

SMC_PM_G2_EN (IN)

R8058 100K 5% 1/10W MF-LF 402

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

PPDCIN_G3H

C8000 10uF 20% 20V CERM 1206

U8000 LT3470 TSOT23-8
VIN, BOOST, SHDN*, SW, BIAS, FB, GND, NC CRITICAL

P3V42G3H5_BOOST

C8005 0.22uF 20% 6.3V X5R 402

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

CRITICAL
L8010 33uH CDPH4D19F-SM

PP3V42_G3H

Vout = 3.425
200mA max output
(Switcher limit)

C8010 22pF 5% 50V CERM 402

<Ra>
R8010 348K 1% 1/16W MF-LF 402

<Rb>
R8011 200K 1% 1/16W MF-LF 402

C8015 22UF 20% 6.3V CERM 805

P3V42G3H_FB

Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

PP3V3_S5
PP1V5_S0

R8061 27.4K 1% 1/10W MF-LF 402
R8063 4.99K 1% 1/16W MF-LF 402

C8060 0.1uF 20% 16V CERM 402

0.89V Reference — P1V0_P1V5PG_REF

U8060 LMC7211 SM-LF
V+, V-, P1V5S0_PGOOD

P1V5S0_COMP_POS

R8062 10K 1% 1/10W MF-LF 402
R8064 10K 1% 1/16W MF-LF 402

R8065 10K 5% 1/16W MF-LF 402

1.5V Comp threshold set to 1.32V (88%)

P1V5P1V05S0_PGOOD (OUT)

P1V5P1V05S0_PGOOD (IN) — P1V5P1V05S0_PGOOD (MAKE_BASE=TRUE)

ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)
NOTE: R8065 acts as 10K pull-up for PGOOD signal

Unused PGOOD Signals

TP_P5V_P1V5_PGOOD — TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE)
TP_P1V8S3_PGOOD — TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation

PP5V_S0
PP3V3_S0
PP2V5_S0
PP1V8_S0
PP1V2_S0
PP0V9_S0

C8070 0.1uF 20% 16V CERM 402

U8070 LTC2908 LLP
V1, V2, V3, V4 CRITICAL, VADJ1, VADJ2, RST*, GND, THRML PAD

C8071 0.1uF 20% 16V CERM 402

R8074 68.1K 1% 1/10W MF-LF 402
R8072 124K 1% 1/16W MF-LF 402

S0PGOOD_1V2_DIV
S0PGOOD_0V9_DIV

S0PGOOD_PWROK

R8076 549K 1% 1/16W MF-LF 402

LTC2908 sources 6uA at 5.0V
R8076 serves as pull-down
and 3.3V level-shifter.

R8075 100K 5% 1/10W MF-LF 402
R8073 100K 1% 1/16W MF-LF 402

LTC2908 threshold is 95% (4.75V, 3.135V, 2.375V, 1.71V, 1.14V, 0.86V)

PP3V3_S0

MC74VHC1G08 SC70 U8080

ALL_SYS_PWRGD (OUT)

C8080 0.1uF 20% 16V CERM 402

3.3V G3Hot Supply & Power Control

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE NONE — SHT 65 OF 86

"S3AC" rail is ON in S3 on AC, OFF in S3 on battery

PP0V9_S0 — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE

PP1V05_S0 — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.05V, MAKE_BASE=TRUE

PP3V3_S5_REG — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE

XW8133 — JUMPER OPEN

PLACEMENT_NOTE=Place on top-side of board

PP1V2_S3 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.22 mm, VOLTAGE=1.2V, MAKE_BASE=TRUE

PP1V2_S0 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.2V, MAKE_BASE=TRUE

PP1V5_S0_REG — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.4 mm, VOLTAGE=1.5V, MAKE_BASE=TRUE

XW8115 — JUMPER OPEN

PLACEMENT_NOTE=Place on top-side of board

PP1V5_S0 — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V, MAKE_BASE=TRUE

PP1V8_S3 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.8V, MAKE_BASE=TRUE

PP1V8_S0 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.8V, MAKE_BASE=TRUE

XW8119 — JUMPER OPEN

PLACEMENT_NOTE=Place on top-side of board

PP2V5_S3_REG — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.3 mm, VOLTAGE=2.5V, MAKE_BASE=TRUE

XW8125 — JUMPER OPEN

PLACEMENT_NOTE=Place on top-side of board

PP2V5_S3 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V, MAKE_BASE=TRUE

PP2V5_S0 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0, MAKE_BASE=TRUE

PPVCORE_S0_GPU — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE

PPDCIN_G3H — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=18.5V, MAKE_BASE=TRUE

GND — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V

PP3V42_G3H — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.42V, MAKE_BASE=TRUE

PP3V3_S3 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE

PP3V3_S0 — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE

R8133 — 0, 5%, 1/8W, MF-LF, 805

PLACEMENT_NOTE=Place on top-side of board

PP3V3_S0GPU — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE

PP5V_S5_REG — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.3 mm, VOLTAGE=5V, MAKE_BASE=TRUE

XW8150 — JUMPER OPEN

PLACEMENT_NOTE=Place on top-side of board

PP3V3_S3AC — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.22 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE

PNBB_S0_GPU — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=-0.7V, MAKE_BASE=TRUE

PPBB_S0_GPU — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.8V, MAKE_BASE=TRUE

PPVCORE_S0_CPU — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.4V, MAKE_BASE=TRUE

PPBUS_G3H — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V, MAKE_BASE=TRUE

PPBUS_S5_FW_FET — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.3 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE

PP5V_S5 — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V, MAKE_BASE=TRUE

PP5V_S3 — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V, MAKE_BASE=TRUE

PP5V_S0 — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V, MAKE_BASE=TRUE

Power Aliases

SYNC_MASTER=M1_MLB SYNC_DATE=12/19/2005

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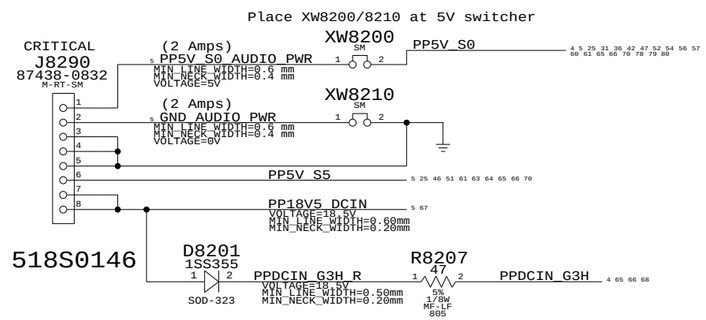
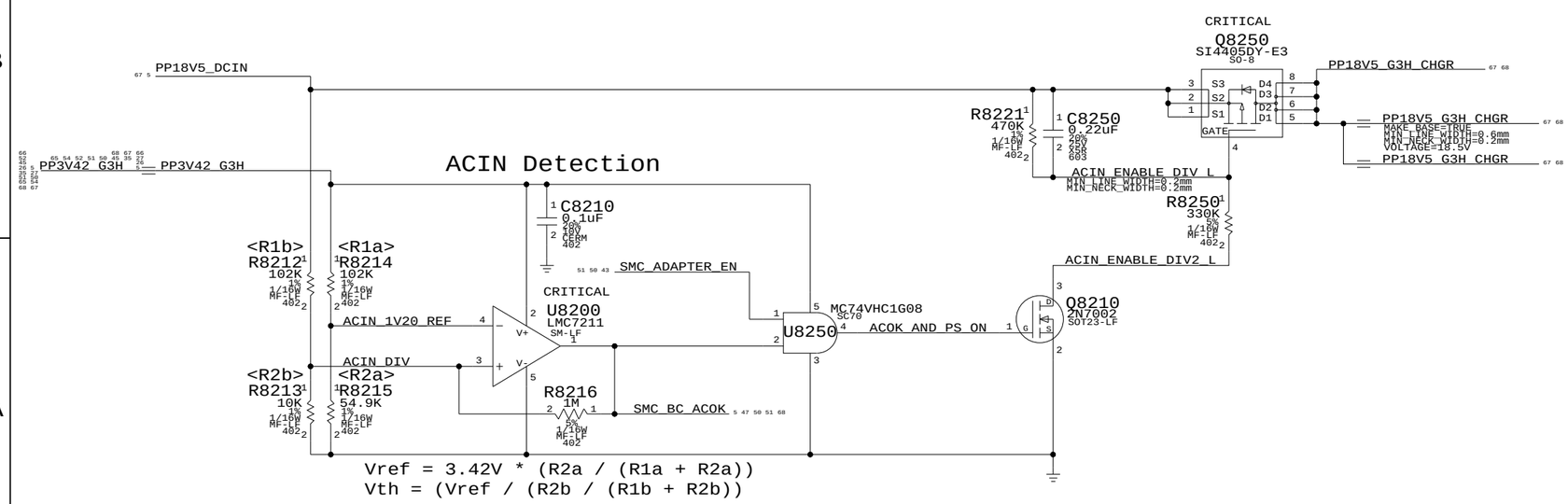
D	051-7023	06

SCALE NONE — SHT 66 OF 86

DC-In Connector



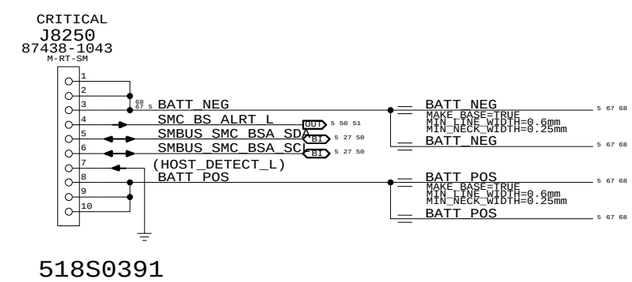
Inrush Limiter



Vref = 3.42V * (R2a / (R1a + R2a))
Vth = (Vref / (R2b / (R1b + R2b))

Vref = 1.20V
Vth = 13.4V

Battery Connector



518S0391

DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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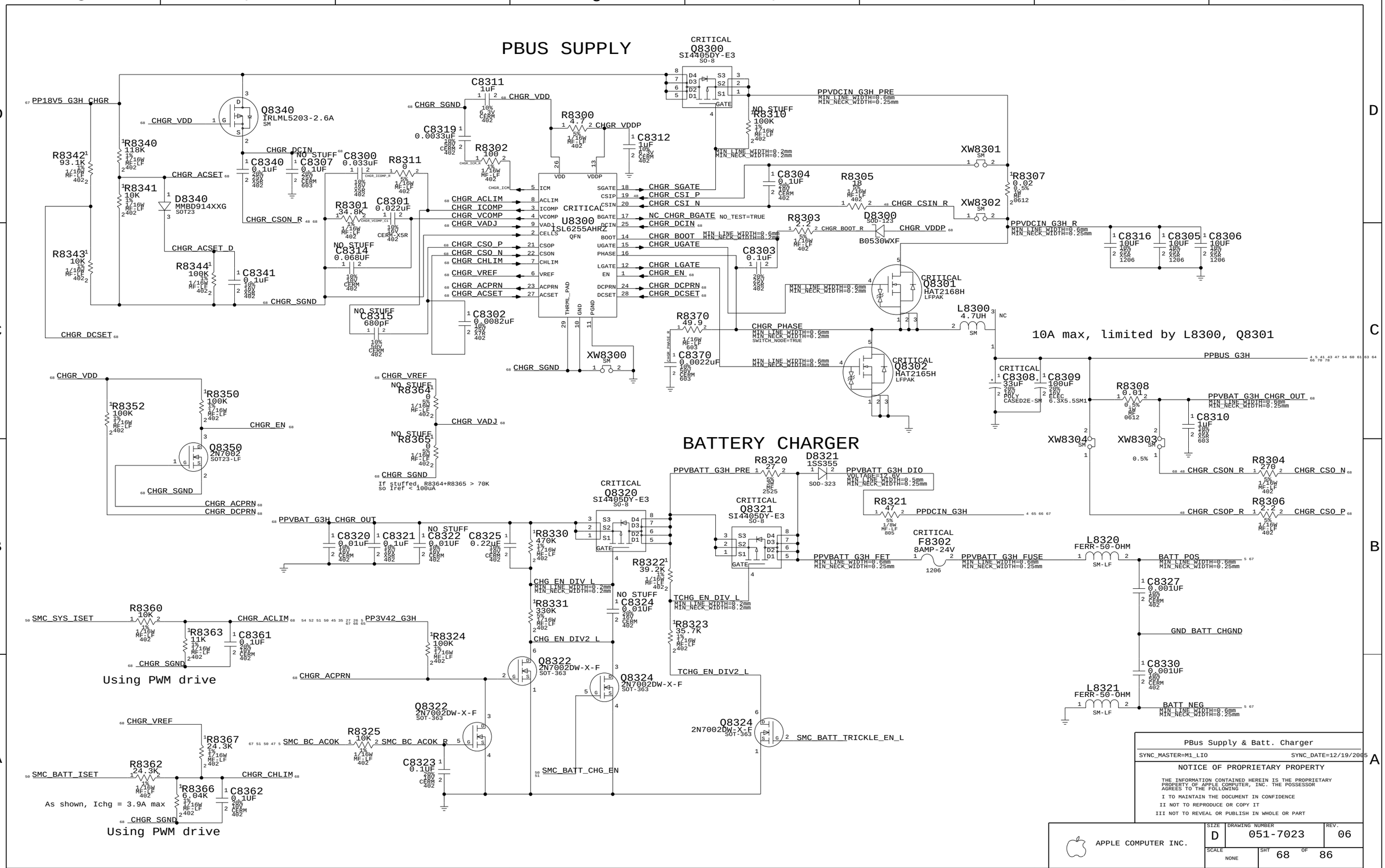
SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 67 OF 86	


PBUS SUPPLY
BATTERY CHARGER
Q8300 SI4405DY-E3 SO-8
U8300 ISL6255AHRZ QFN
Q8340 IRLML5203-2.6A SM
Q8350 2N7002 SOT23-LF
Q8320 SI4405DY-E3 SO-8
Q8321 SI4405DY-E3 SO-8
Q8322 2N7002DW-X-F SOT-363
Q8324 2N7002DW-X-F SOT-363
Q8301 HAT2168H LFPAK
Q8302 HAT2165H LFPAK
D8300 B0530WXF SOD-123
D8321 1SS355 SOD-323
D8340 MMBD914XXG SOT23
F8302 8AMP-24V 1206
L8300 4.7UH SM
L8320 FERR-50-OHM SM-LF
L8321 FERR-50-OHM SM-LF
10A max, limited by L8300, Q8301
Using PWM drive
Using PWM drive
As shown, Ichg = 3.9A max
If stuffed, R8364+R8365 > 70K so Iref < 100uA
PBus Supply & Batt. Charger
SYNC_MASTER=M1_LIO
SYNC_DATE=12/19/2005
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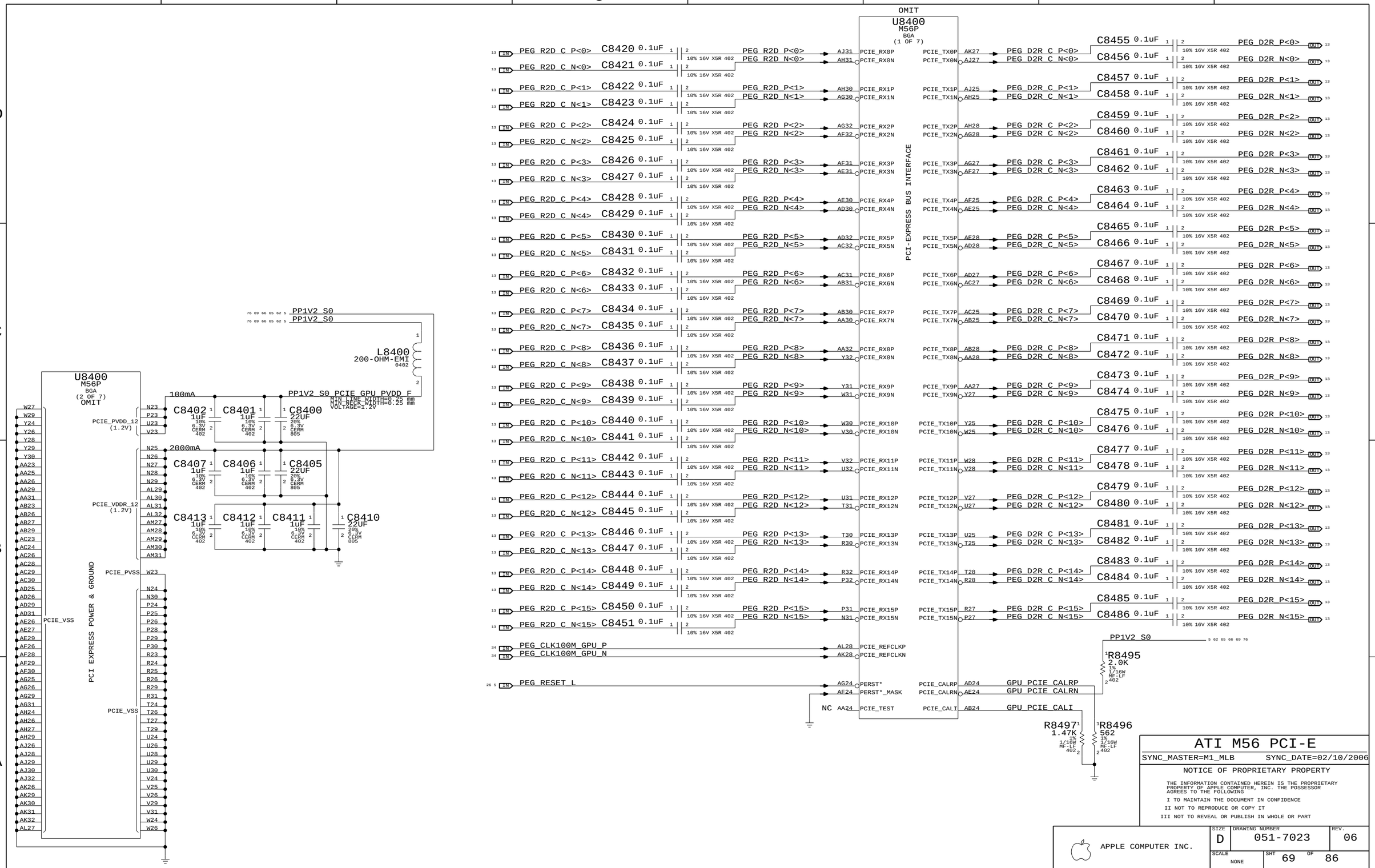
SIZE D
DRAWING NUMBER 051-7023
REV. 06
SCALE NONE
SHT 68 OF 86



ATI M56 PCI-E

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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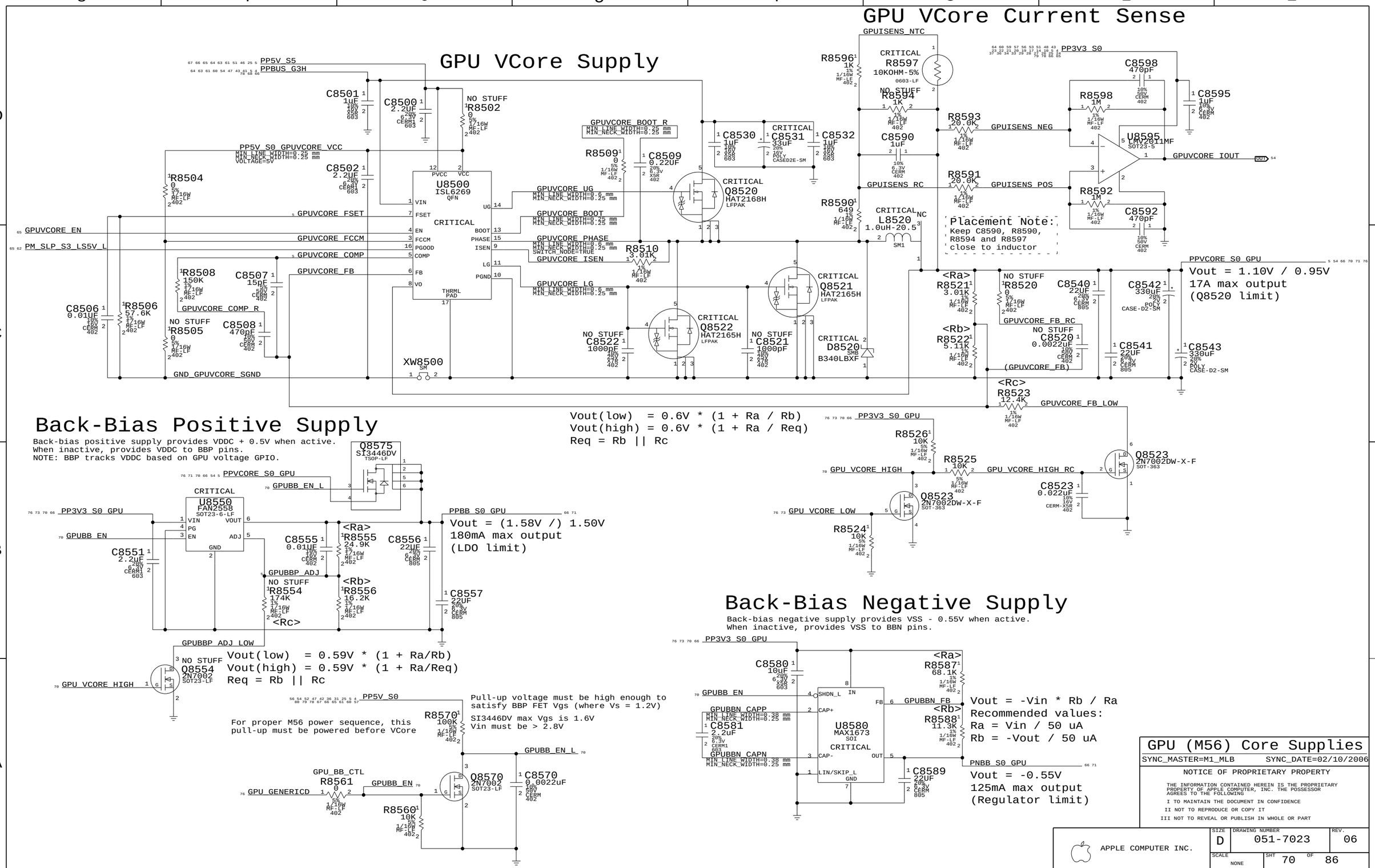
SCALE NONE	SHT 69 OF 86	



GPU (M56) Core Supplies

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7023	06

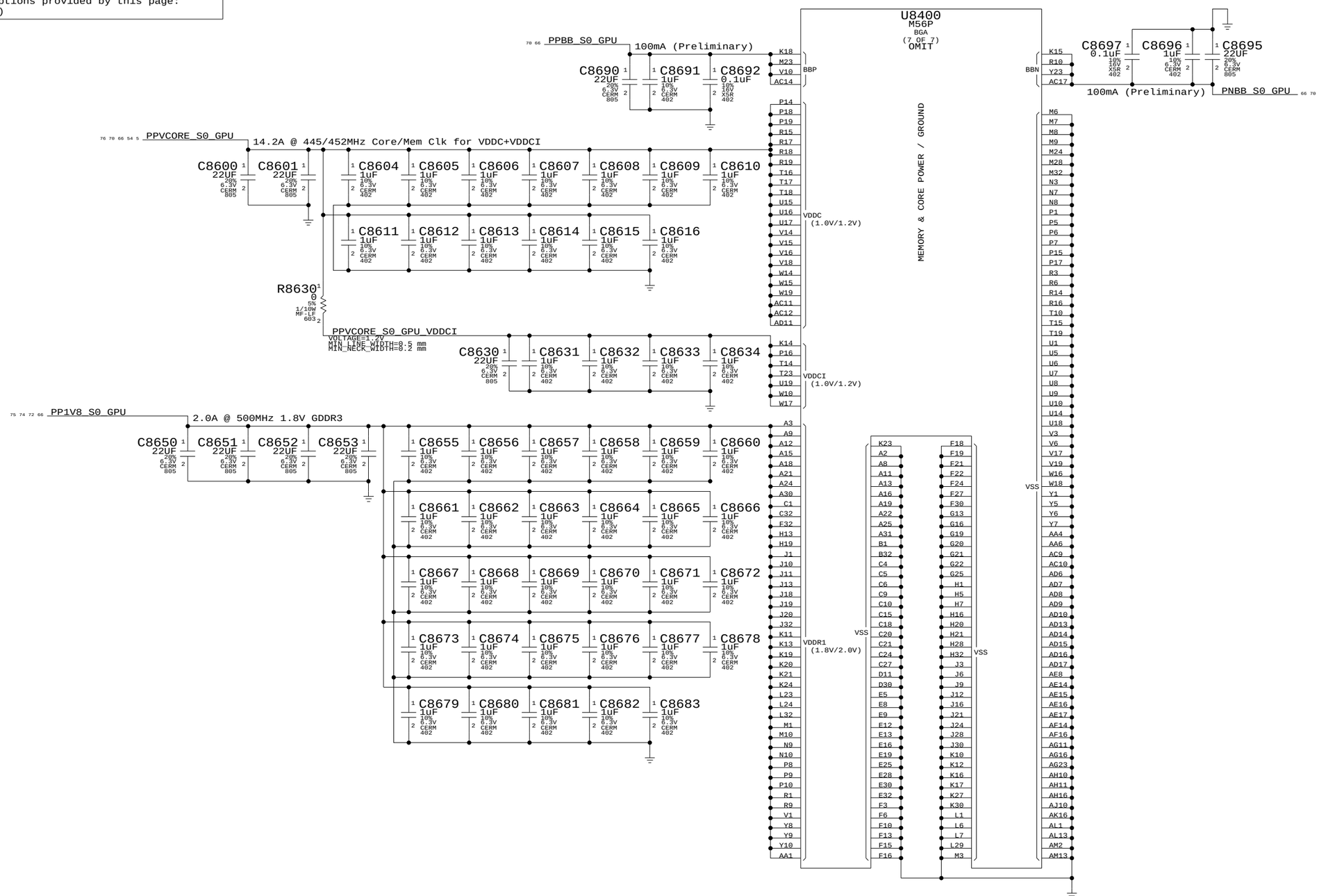
SCALE NONE SHT 70 OF 86

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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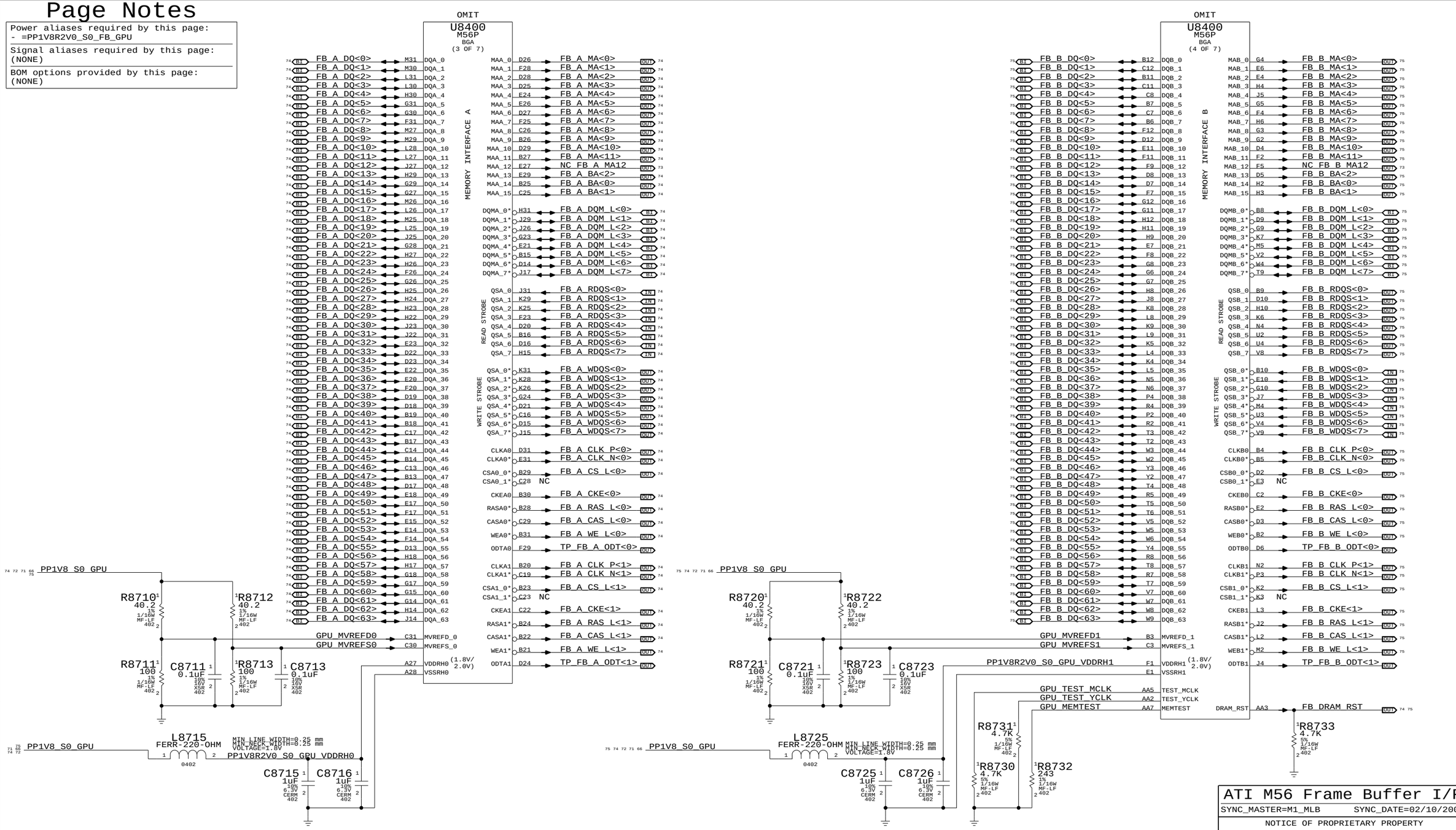
SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE NONE	SHT 71 OF 86	

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE NONE

ROMCFGID[3..0]

0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

76 73 70 66 PP3V3_S0_GPU

		Serial ROM	TestBus	Misc	Straps		
76 GPU_GPIO_0	IPD		TESTIN[0]		TX_PWRS_ENb	R8800[1] 10K 5% 1/16W MF-LF 402	
76 GPU_GPIO_1	IPD		TESTIN[1]		TX_DEEMPH_EN	R8801[1] 10K 5% 1/16W MF-LF 402	GPU_DEEPMH_EN
76 GPU_GPIO_2		VDD_VCL	TESTIN[2]		Reserved	R8802[1] 10K 5% 1/16W MF-LF 402	NO STUFF
76 GPU_GPIO_3			TESTIN[3]		Reserved	R8803[1] 10K 5% 1/16W MF-LF 402	NO STUFF
76 GPU_GPIO_4	IPD		TESTIN[4]		DEBUG_ACCESS	R8804[1] 10K 5% 1/16W MF-LF 402	NO STUFF
76 GPU_GPIO_5			TESTIN[5]		Reserved	R8805[1] 10K 5% 1/16W MF-LF 402	NO STUFF
76 GPU_GPIO_6			TESTIN[6]		Reserved	R8806[1] 10K 5% 1/16W MF-LF 402	NO STUFF
78 76 73 GPU_BLON		ENA_BL	TESTIN[7]			R8808[1] 10K 5% 1/16W MF-LF 402	NO STUFF
76 GPU_GPIO_8		ROMSO	TESTWR		Reserved	R8809[1] 10K 5% 1/16W MF-LF 402	NO STUFF
76 GPU_GPIO_9	IPD	ROMSI			ROMIDCFG[3]	R8812[1] 10K 5% 1/16W MF-LF 402	GPU_MEM_256M
76 73 TP_GPU_GPIO_10		ROMSCK	TESTOUT[8]			R8813[1] 10K 5% 1/16W MF-LF 402	GPU_MEM_64M
76 GPU_GPIO_11	IPD		TESTOUT[9]		ROMIDCFG[0]	R8824[1] 10K 5% 1/16W MF-LF 402	GPU_MEM_256M
76 GPU_GPIO_12	IPD		TESTOUT[10]		ROMIDCFG[1]	R8811[1] 10K 5% 1/16W MF-LF 402	NO STUFF
76 GPU_GPIO_13	IPD		TESTOUT[11]		ROMIDCFG[2]	R8827[1] 10K 5% 1/16W MF-LF 402	GPU_MEM_HYNIX
76 73 NC_GPU_GPIO_14			TESTIN[8]				
76 73 70 GPU_VCORE_LOW			TESTIN[9]	PWRCNTL			
76 73 34 GPU_CLK27MSS_IN				SS_IN			
76 73 NC_GPU_GPIO_17				Thm Mon Int			

GPU_BLON — MAKE_BASE=TRUE 73 76 78

TP_GPU_GPIO_10 — MAKE_BASE=TRUE 73 76

Required for debug access
Required for debug access
Required for debug access
Required for debug access

NC_GPU_GPIO_14 — MAKE_BASE=TRUE NO_TEST=TRUE 73 76

GPU_VCORE_LOW — MAKE_BASE=TRUE 70 73 76

GPU_CLK27MSS_IN — MAKE_BASE=TRUE 34 73 76

NC_GPU_GPIO_17 — MAKE_BASE=TRUE NO_TEST=TRUE 73 76

76 73 NC_GPU_GPIO_18	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_18 73 76
76 73 NC_GPU_GPIO_19	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_19 73 76
76 73 NC_GPU_GPIO_20	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_20 73 76
76 73 NC_GPU_GPIO_21	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_21 73 76
76 73 NC_GPU_GPIO_22	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_22 73 76
76 73 NC_GPU_GPIO_23	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_23 73 76
76 73 GPU_MEM_256M		76 73 GPU_MEM_256M — MAKE_BASE=TRUE
76 73 NC_GPU_GPIO_25	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_25 73 76
76 73 NC_GPU_GPIO_26	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_26 73 76
76 73 GPU_MEMID		76 73 GPU_MEMID — MAKE_BASE=TRUE
76 73 NC_GPU_GPIO_28	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_28 73 76
76 73 NC_GPU_GPIO_29	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_29 73 76
76 73 NC_GPU_GPIO_30	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_30 73 76
76 73 NC_GPU_GPIO_31	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_31 73 76
76 73 NC_GPU_GPIO_32	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_32 73 76
76 73 NC_GPU_GPIO_33	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_33 73 76
76 73 NC_GPU_GPIO_34	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GPIO_34 73 76

Renamed signals

76 73 34 GPU_CLK27M — MAKE_BASE=TRUE — GPU_CLK27M 34 73 76

Unused signals

76 73 NC_GPU_XTALOUT	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_XTALOUT 73 76
76 73 NC_ATI_ROMCS_L	MAKE_BASE=TRUE NO_TEST=TRUE	NC_ATI_ROMCS_L 73 76
73 72 NC_FB_A_MA12	MAKE_BASE=TRUE NO_TEST=TRUE	NC_FB_A_MA12 72 73
73 72 NC_FB_B_MA12	MAKE_BASE=TRUE NO_TEST=TRUE	NC_FB_B_MA12 72 73
76 73 NC_GPU_GENERICA	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GENERICA 73 76
76 73 NC_GPU_GENERICB	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GENERICB 73 76
76 73 NC_GPU_GENERICC	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_GENERICC 73 76
77 73 NC_GPU_VGA_R	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_VGA_R 73 77
77 73 NC_GPU_VGA_G	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_VGA_G 73 77
77 73 NC_GPU_VGA_B	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_VGA_B 73 77
77 73 TP_GPU_VGA_HSYNC	MAKE_BASE=TRUE	TP_GPU_VGA_HSYNC 73 77
77 73 TP_GPU_VGA_VSYNC	MAKE_BASE=TRUE	TP_GPU_VGA_VSYNC 73 77
77 73 NC_GPU_TV_Y	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_TV_Y 73 77
77 73 NC_GPU_TV_C	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_TV_C 73 77
77 73 NC_GPU_TV_COMP	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_TV_COMP 73 77
77 73 NC_LVDS_U_DATAP<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_U_DATAP<3> 73 77
77 73 NC_LVDS_U_DATAN<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_U_DATAN<3> 73 77
77 73 NC_LVDS_L_DATAP<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_L_DATAP<3> 73 77
77 73 NC_LVDS_L_DATAN<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_L_DATAN<3> 73 77
76 73 NC_ATI_DVPCLK	MAKE_BASE=TRUE NO_TEST=TRUE	NC_ATI_DVPCLK 73 76
76 NC_ATI_DVPCNTL<2..0>	MAKE_BASE=TRUE NO_TEST=TRUE	ATI_DVPCNTL<2..0>
76 NC_ATI_DVPDATA<15..0>	MAKE_BASE=TRUE NO_TEST=TRUE	ATI_DVPDATA<15..0>

Required for debug access

76 TP_ATI_DVPDATA<23..16> — MAKE_BASE=TRUE — ATI_DVPDATA<23..16>

Also required: GPIO10 - GPIO13

76 73 70 66 PP3V3_S0_GPU

R9390[1] 4.7K 5% 1/16W MF-LF 402 — 77 GPU_DDC_B_CLK

R9391[1] 4.7K 5% 1/16W MF-LF 402 — 77 GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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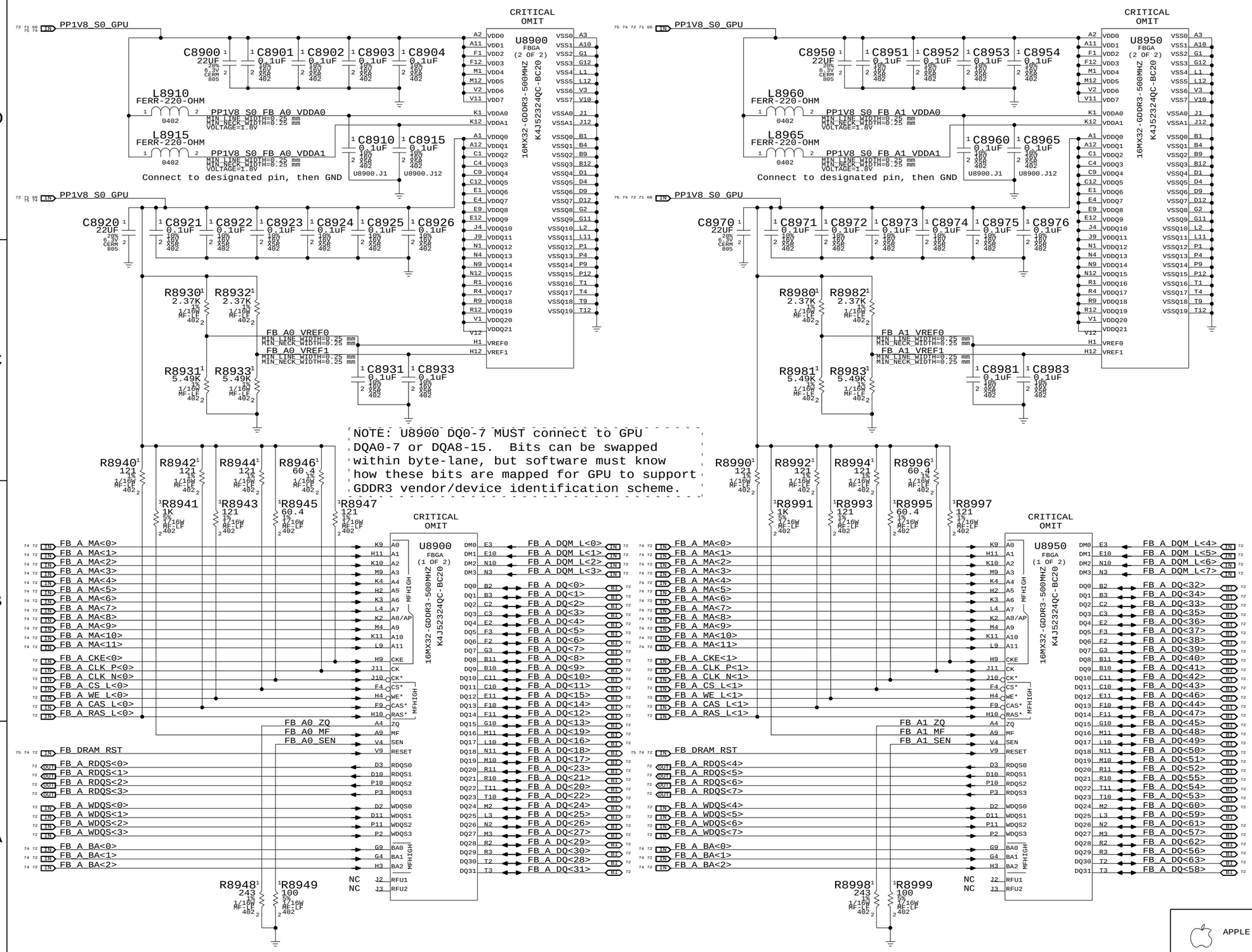
D	051-7023	06

SCALE NONE — SHT 73 OF 86



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer A

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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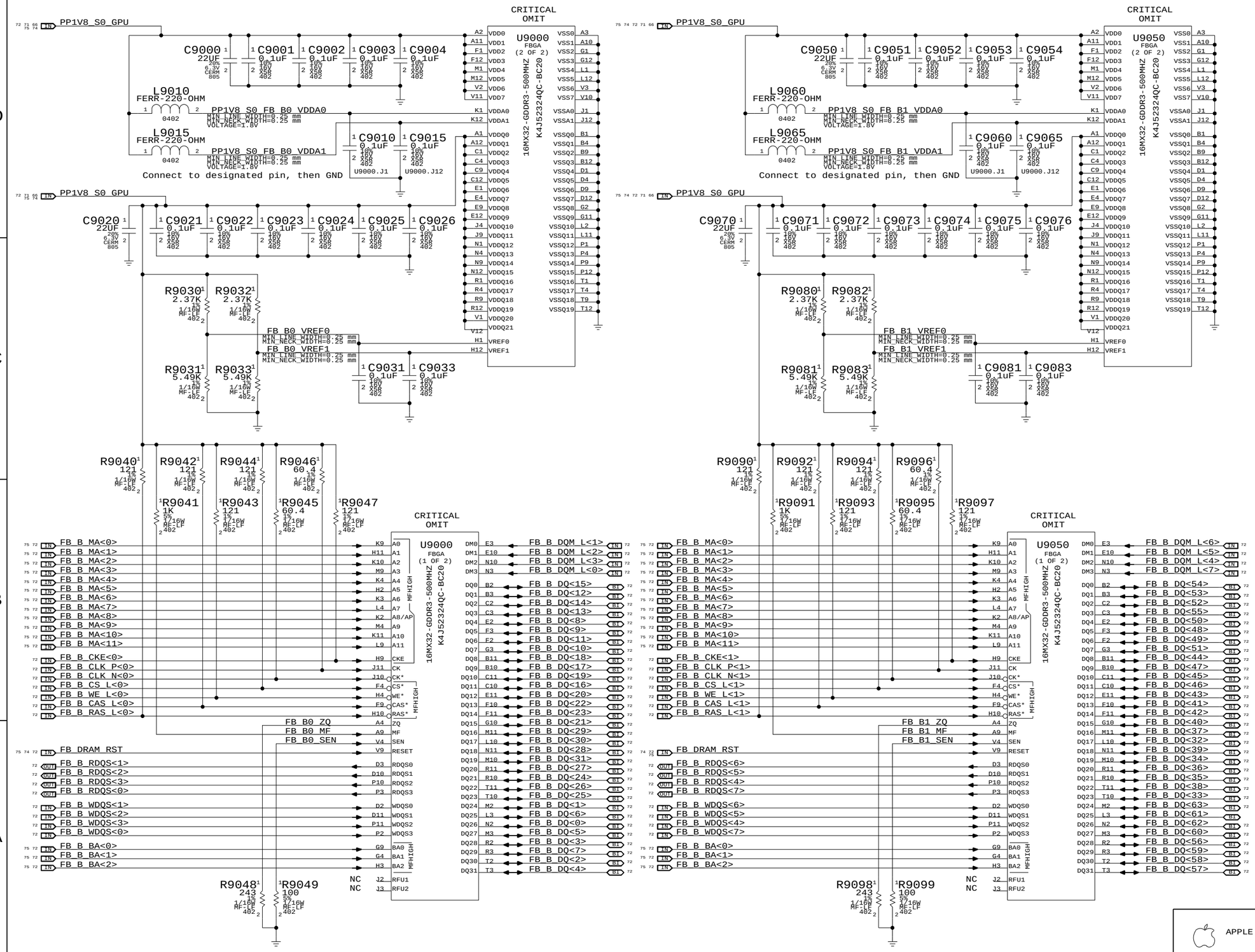
SCALE NONE SHT 74 OF 86



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

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SCALE NONE

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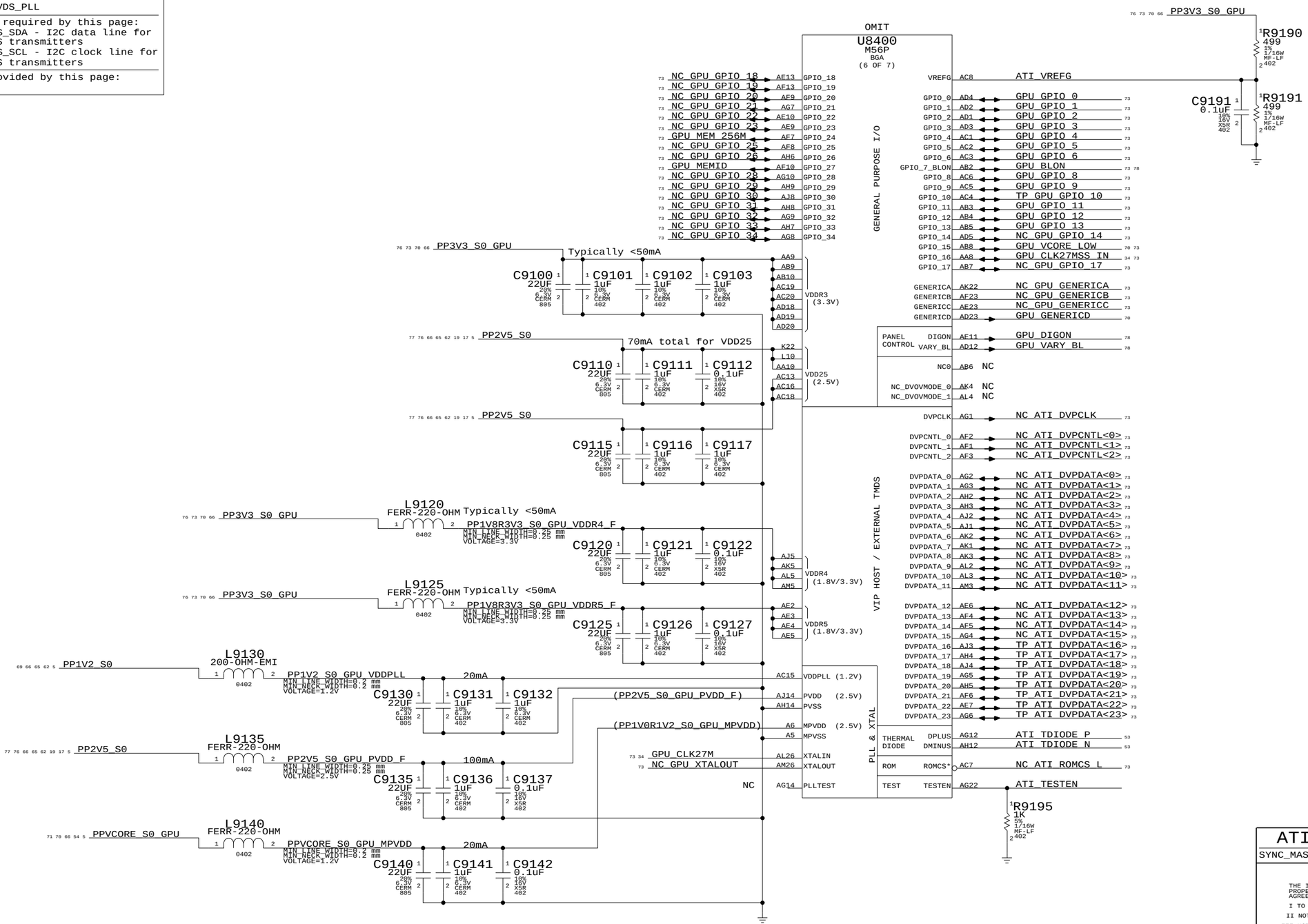
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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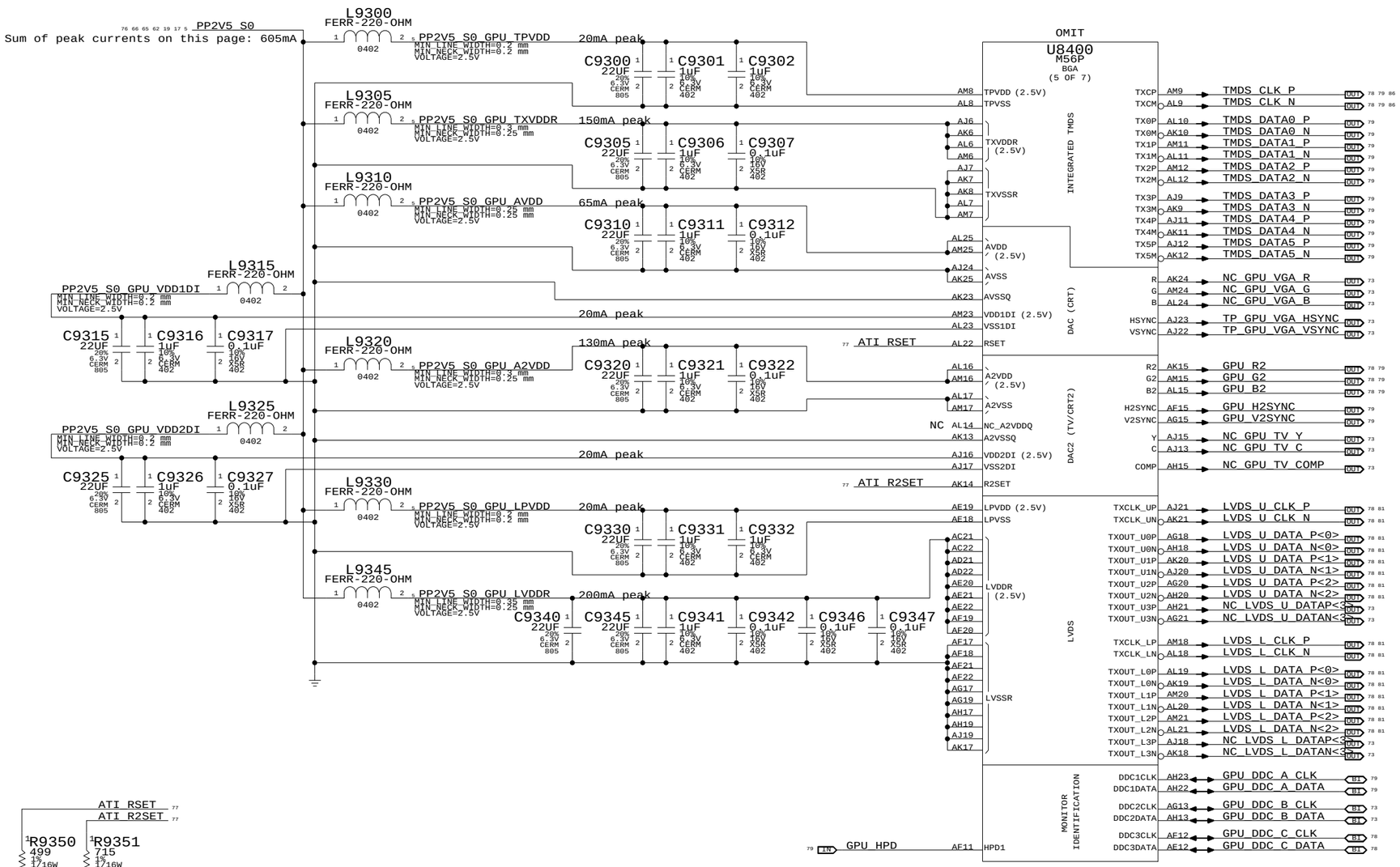
SCALE NONE

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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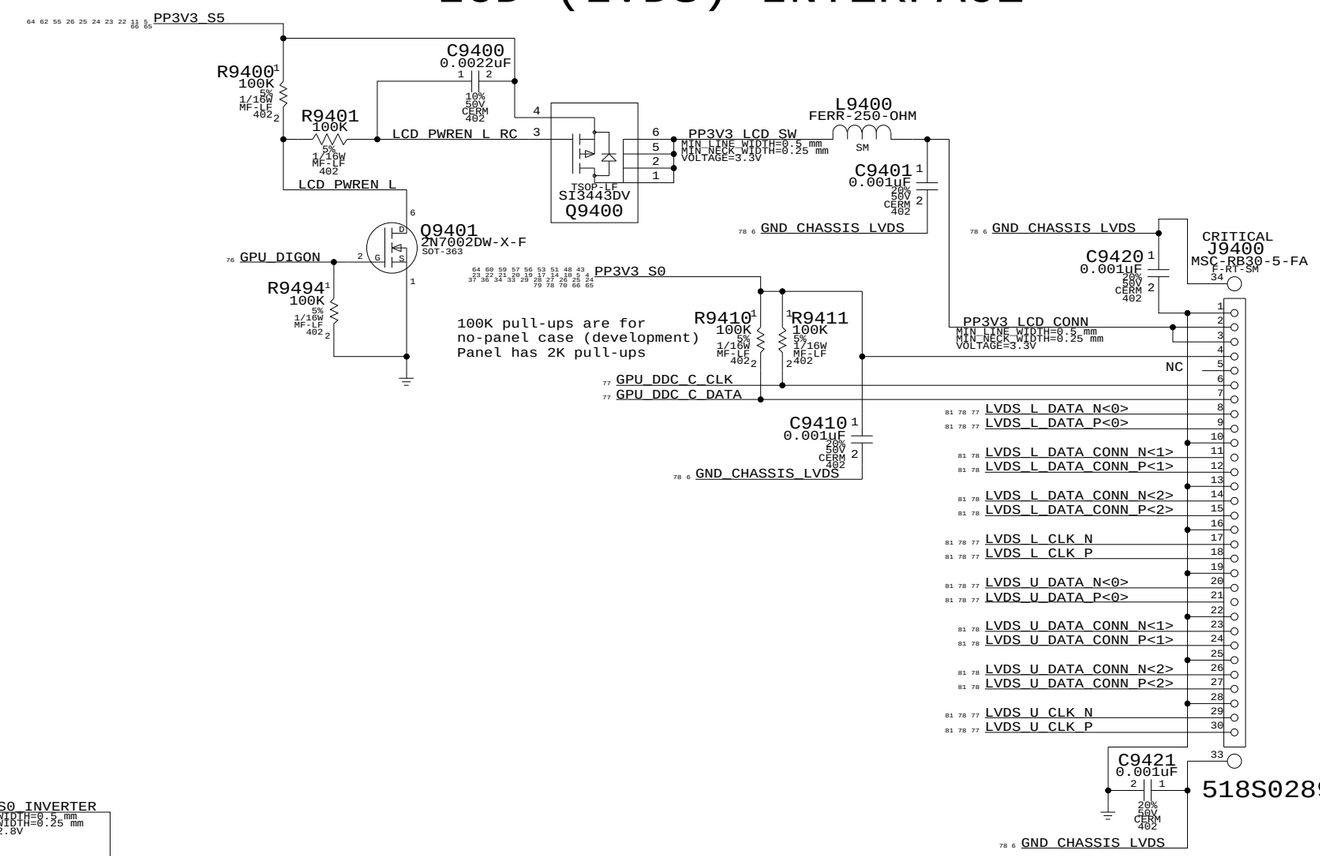
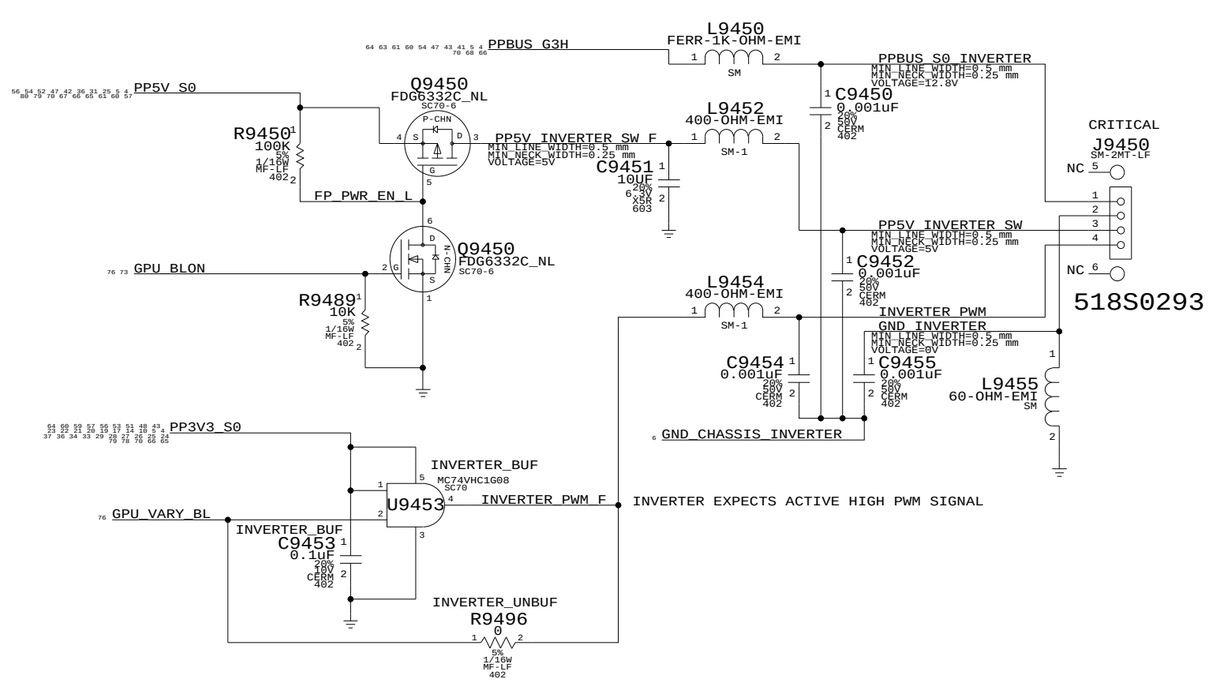
LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
	VGA	VGA	GPU_R2
	VGA	VGA	GPU_G2
	VGA	VGA	GPU_B2
	LVDS	LVDS	LVDS_U_CLK_P
	LVDS	LVDS	LVDS_U_CLK_N
	LVDS	LVDS	LVDS_U_DATA_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_P
	LVDS	LVDS	LVDS_L_CLK_N
	LVDS	LVDS	LVDS_L_DATA_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_N<2..0>
	LVDS	LVDS	LVDS_U_CLK_P
	LVDS	LVDS	LVDS_U_CLK_N
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_P
	LVDS	LVDS	LVDS_L_CLK_N
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>
	TMDS	TMDS	TMDS_CLK_P
	TMDS	TMDS	TMDS_CLK_N
	TMDS	TMDS	TMDS_DATA_P<5..3>
	TMDS	TMDS	TMDS_DATA_N<5..3>
	TMDS	TMDS	TMDS_DATA_P<2..0>
	TMDS	TMDS	TMDS_DATA_N<2..0>



INVERTER INTERFACE



Internal Display Connectors

SYNC_MASTER=M1_MLB SYNC_DATE=01/09/2006

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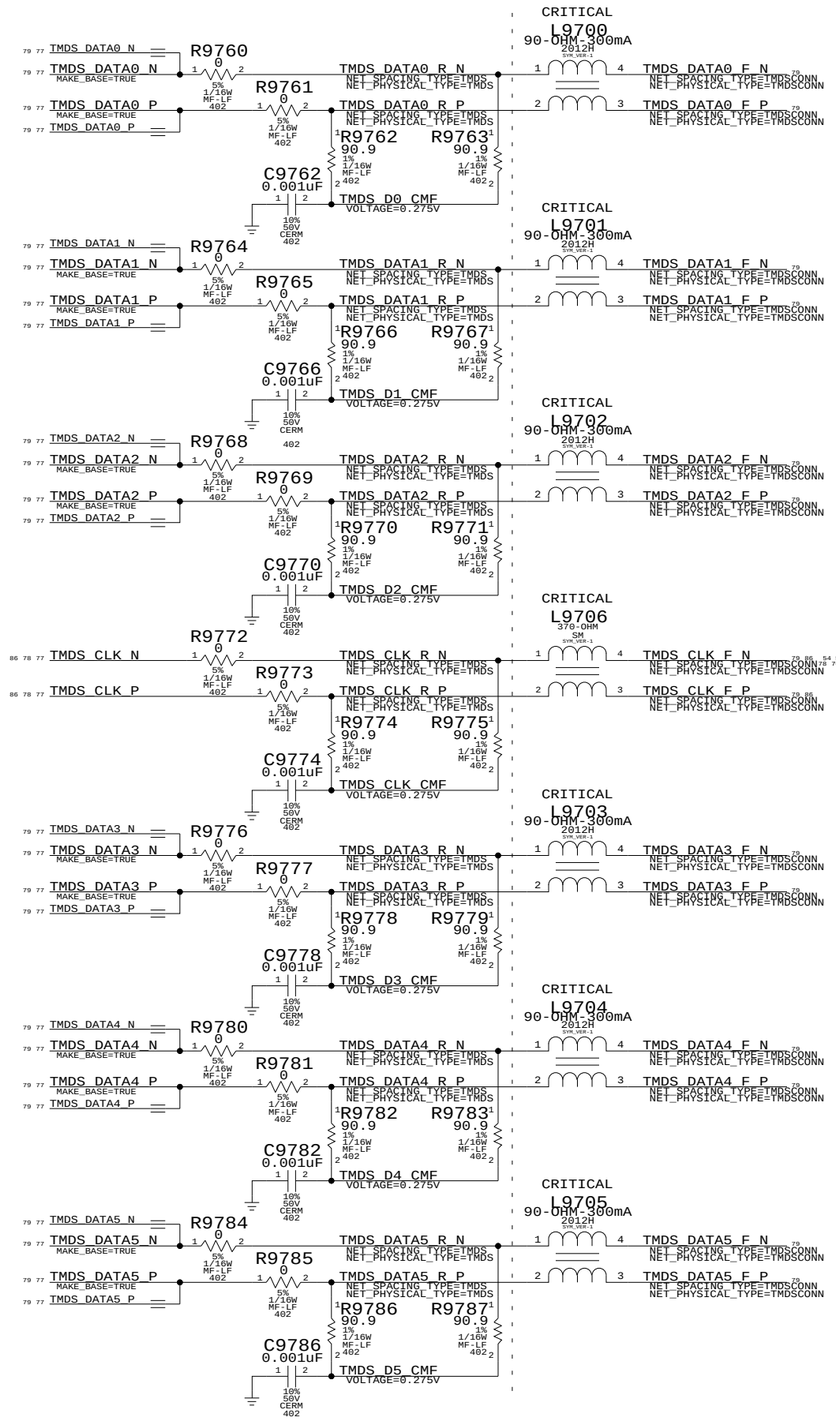
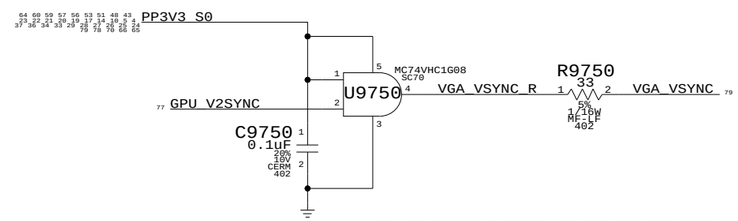
TMDS Filtering

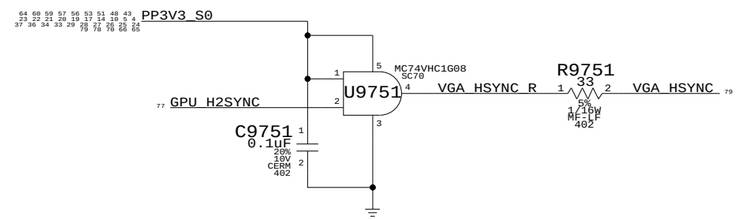
Place series R's and common-mode filtering close to GPU, common mode chokes near connector.



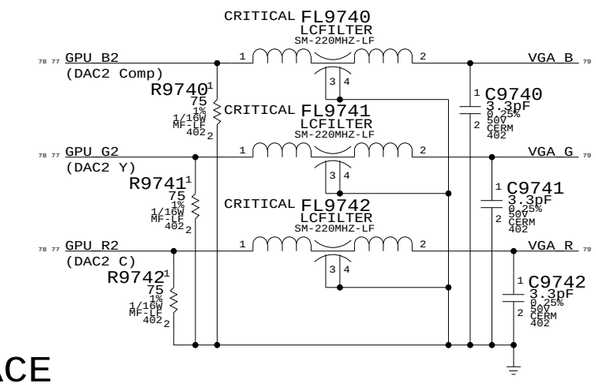
VGA SYNC BUFFERS



PLACE R9750 & R9751 CLOSE TO DVI CONNECTOR

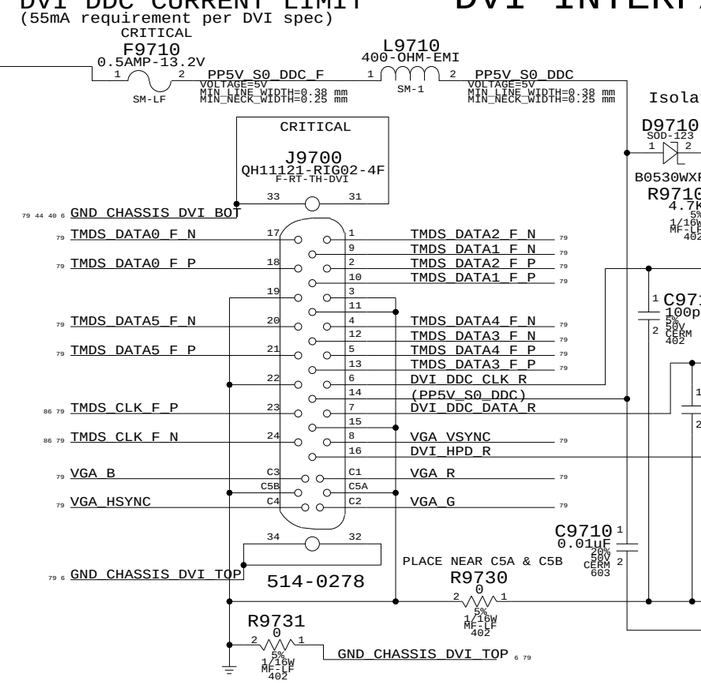


ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

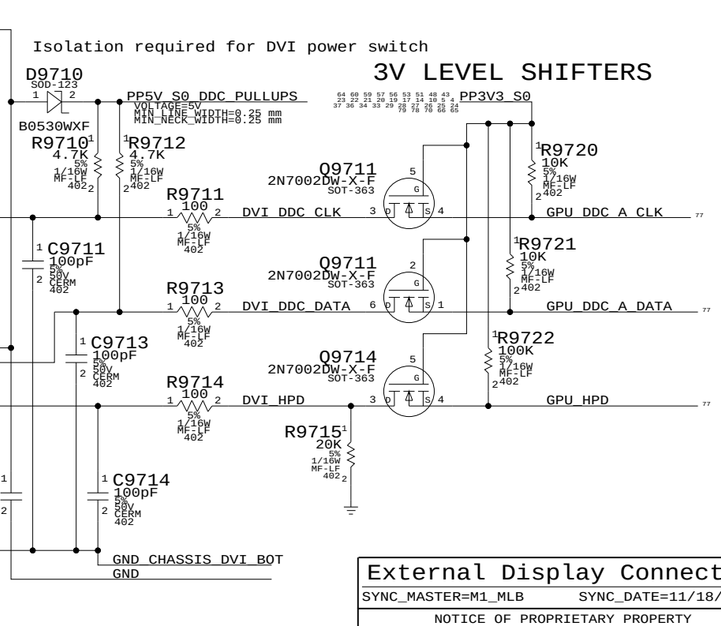


DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

DVI INTERFACE



Isolation required for DVI power switch



External Display Connector	
SYNC_MASTER=M1_MLB	SYNC_DATE=11/18/2005

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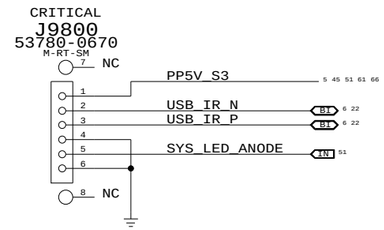
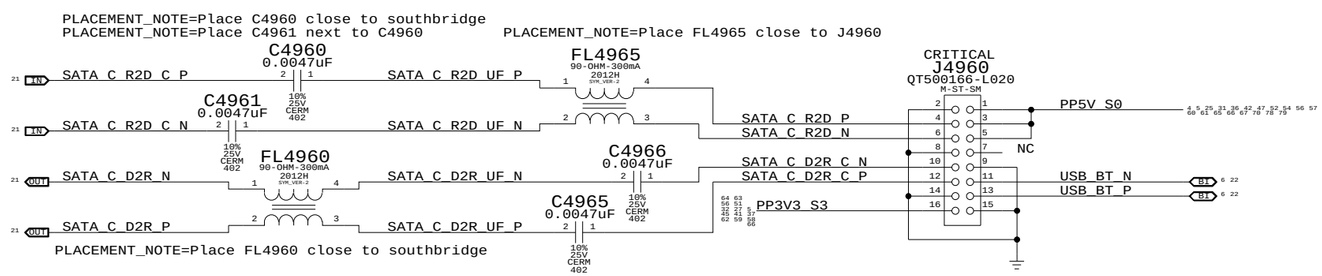
IR & Sleep LED Connector



518S0388

Bluetooth (M13P) & SATA HDD Flex Connector



516S0350

M9 Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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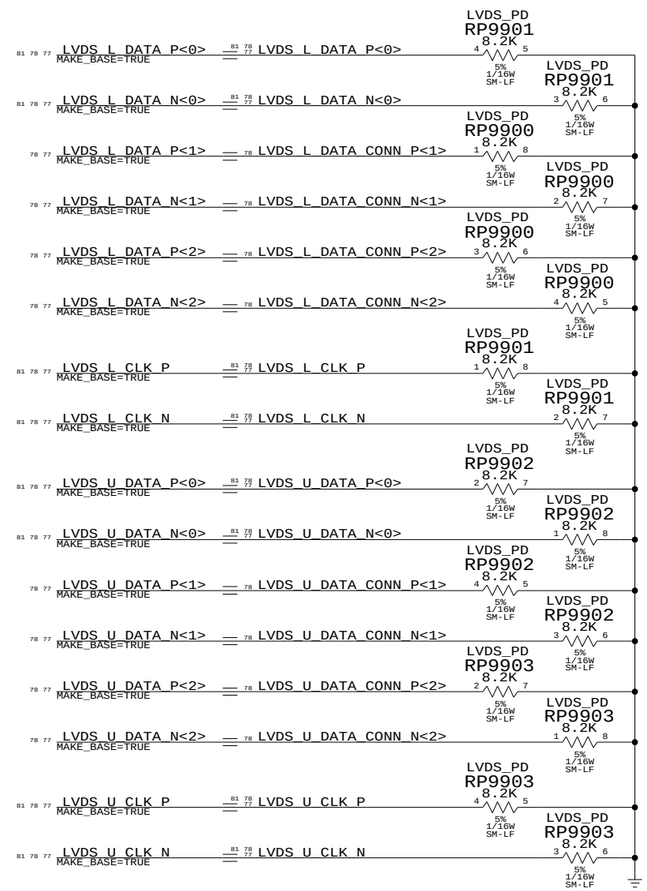
LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



LVDS Interface Pull-downs

SYNC_MASTER=M1_MLB SYNC_DATE=12/19/2005

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Revision History

Proto

11-29-05: -Release for Proto

11-30-05: -Turned on M56_REV_B24 BOMOPTION

12-01-05: -Added CRITICAL property to 3-pin caps, ESD diodes, and FW chokes
-Added TIPCONN_BOMOPTION
-RC value changes on CPU Core current sense
-Changed IDE reset pulldown to 15K

EVT

12-01-05: -Changed L1400 to Pb-free part
-Changed J4620 to M8 part
-Added ESD/EMI protection to camera connector
-Removed dual voltage support for trackpad
-Added PM_SOS_STAT_L and PM_SLP_S5_L pulldowns

Revision History

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	?
USB2_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

Napa Platform Constraints

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	?
FB_CLK	*	=2.5:1_SPACING	?
FB_DATA	*	=2.5:1_SPACING	?

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	=3:1_SPACING	?
TMDS	*	=3:1_SPACING	?
VGA	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS_PAIR2PAIR	*	25 MIL	?
TMDS_PAIR2PAIR	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET	*	=3:1_SPACING	?
FW	*	=3:1_SPACING	?

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

More System Constraints

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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M1 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2,ISL11	0.1 MM	?
1.8:1_SPACING	ISL2,ISL11	0.1 MM	?
2:1_SPACING	ISL2,ISL11	0.1 MM	?
2.5:1_SPACING	ISL2,ISL11	0.1 MM	?
3:1_SPACING	ISL2,ISL11	0.1 MM	?
4:1_SPACING	ISL2,ISL11	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2,ISL11	0.1 MM	?
CLK_PCIE	ISL2,ISL11	0.1 MM	?
CLK_MED	ISL2,ISL11	0.1 MM	?
CLK_SLOW	ISL2,ISL11	0.1 MM	?
CPU_COMP	ISL2,ISL11	0.1 MM	?
CPU_GTLREF	ISL2,ISL11	0.1 MM	?
CPU_VCCSENSE	ISL2,ISL11	0.1 MM	?
DMI	ISL2,ISL11	0.1 MM	?
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
MEM_2OTHER	ISL2,ISL11	0.1 MM	?
PCIE	ISL2,ISL11	0.1 MM	?
SATA	ISL2,ISL11	0.1 MM	?
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
VGA	ISL2,ISL11	0.1 MM	?

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	? OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M1 Spacing & Physical Constraints
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	5 7 11 12
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	5 7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	5 7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	5 7 21
	CPU_55S	CPU_2T01	CPU_THERMTRIP_L	
	CPU_55S	CPU_2T01	PM_DPRSLPVR	5 14 23 60
	CPU_55S	CPU_2T01	IMVP_DPRSLPVR	5 60
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2T01	CPU_VID<6..0>	8 9 86
	CPU_55S	CPU_2T01	CPU_VID<6..0>	8 9 86
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 60
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 60
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	60
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	60

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 47
AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
AUDIO_55S	AUDIO	ACZ_SYNC	5 21 47
AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
AUDIO_55S	AUDIO	ACZ_RST_L	5 21 47
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 47
AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 47

TMDS	TMDS	TMDS_CLK_P	77 78 79
TMDS	TMDS	TMDS_CLK_N	77 78 79
TMDS	TMDS	TMDS_DATA_P<5..3>	78
TMDS	TMDS	TMDS_DATA_N<5..3>	78
TMDS	TMDS	TMDS_DATA_P<2..0>	78
TMDS	TMDS	TMDS_DATA_N<2..0>	78
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	79
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	79
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	

M1 Net Properties

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