

CONFUCIUS

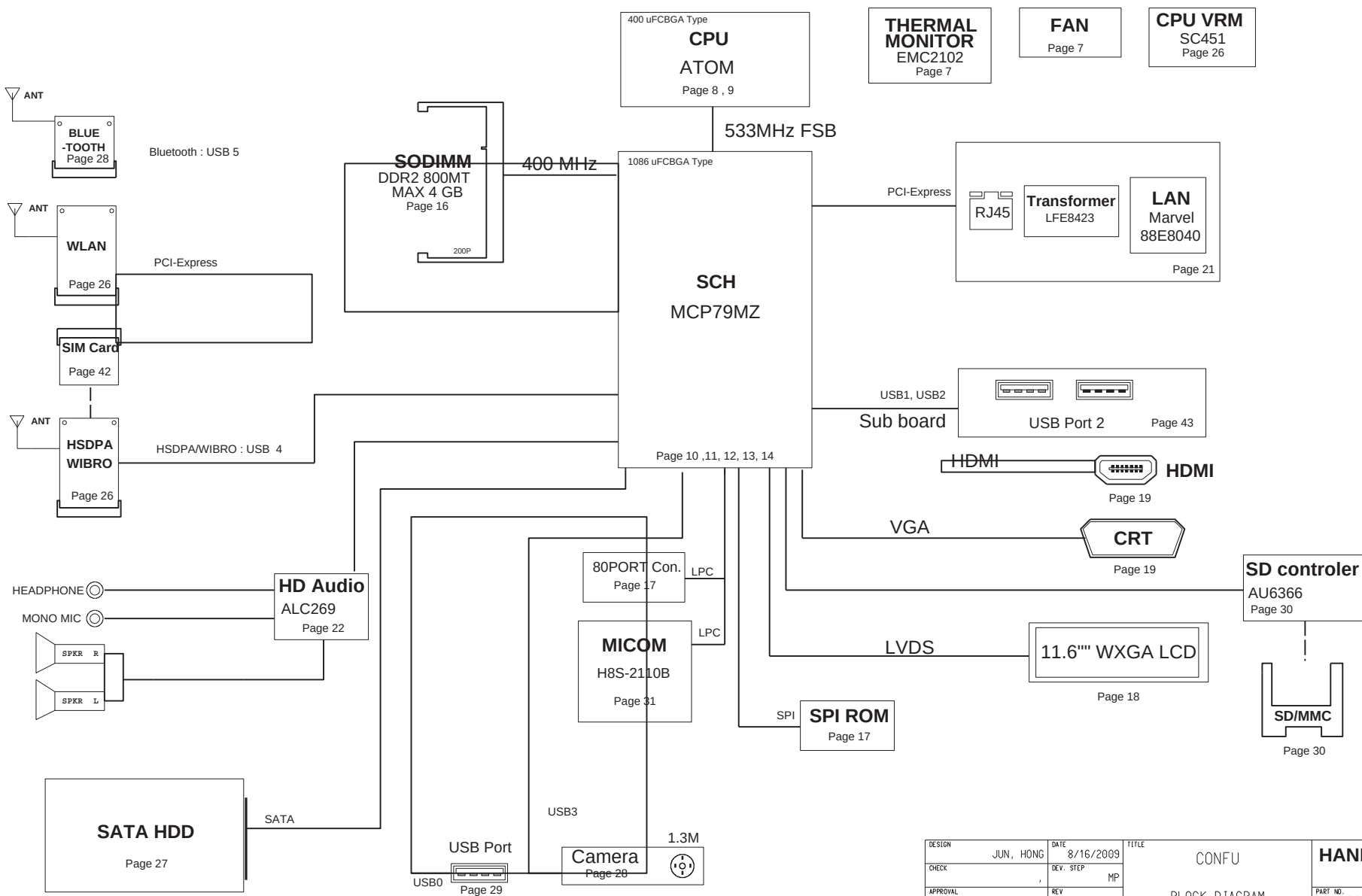
CPU :ATOM (N270)
Chip Set :MCP79MZ
Remarks :12.1"

Model Name : CONFU
PBA Name : PBA01-0010A
PCB Code : PCB01-0010A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2009.09.05

DESIGN	CHECK	APPROVAL

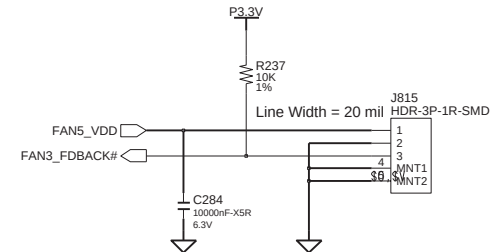
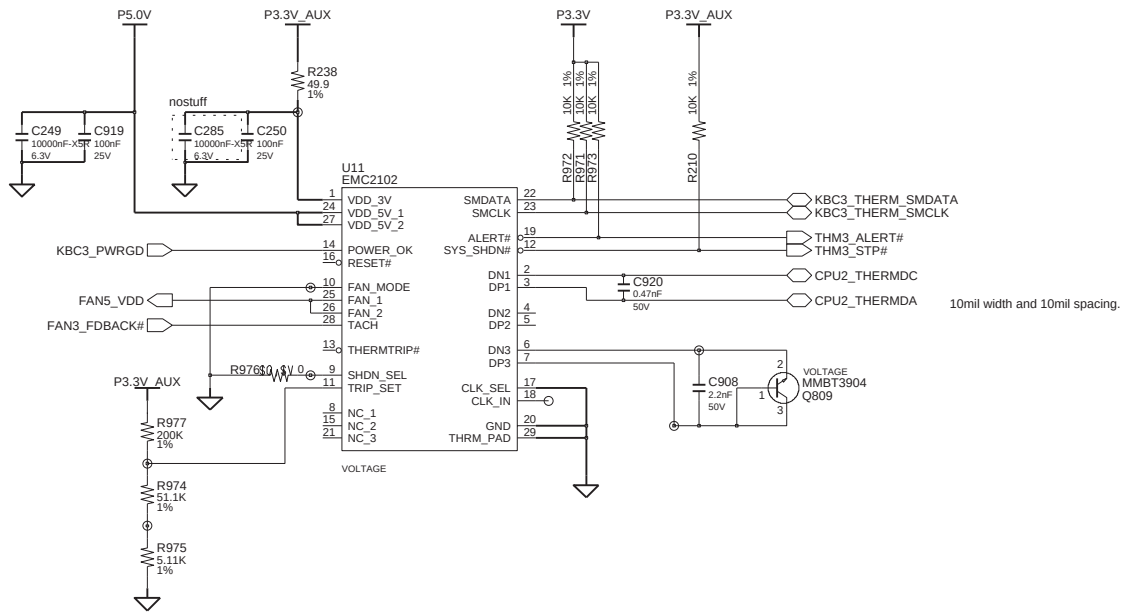
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CHECK	.	DEV. STEP	MP			TECH
APPROVAL	.	REV	1.0	TOC		PART NO. PCB01-0010A
MODULE CODE		LAST EDIT	August, 16, 2009 12:40:05 AM	PAGE	1 OF 40	

OPERATION BLOCK DIAGRAM

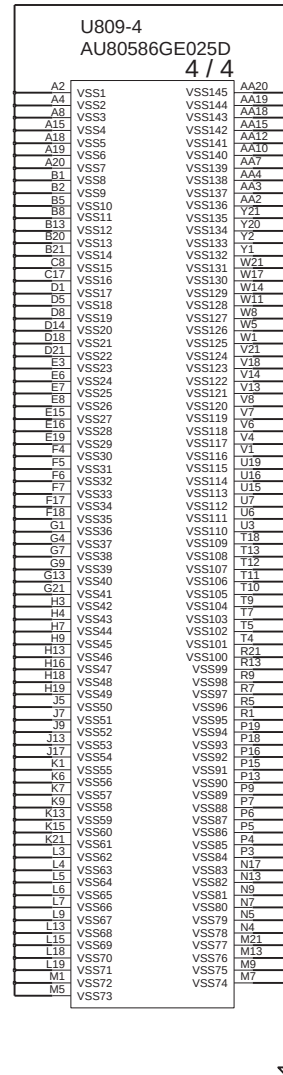
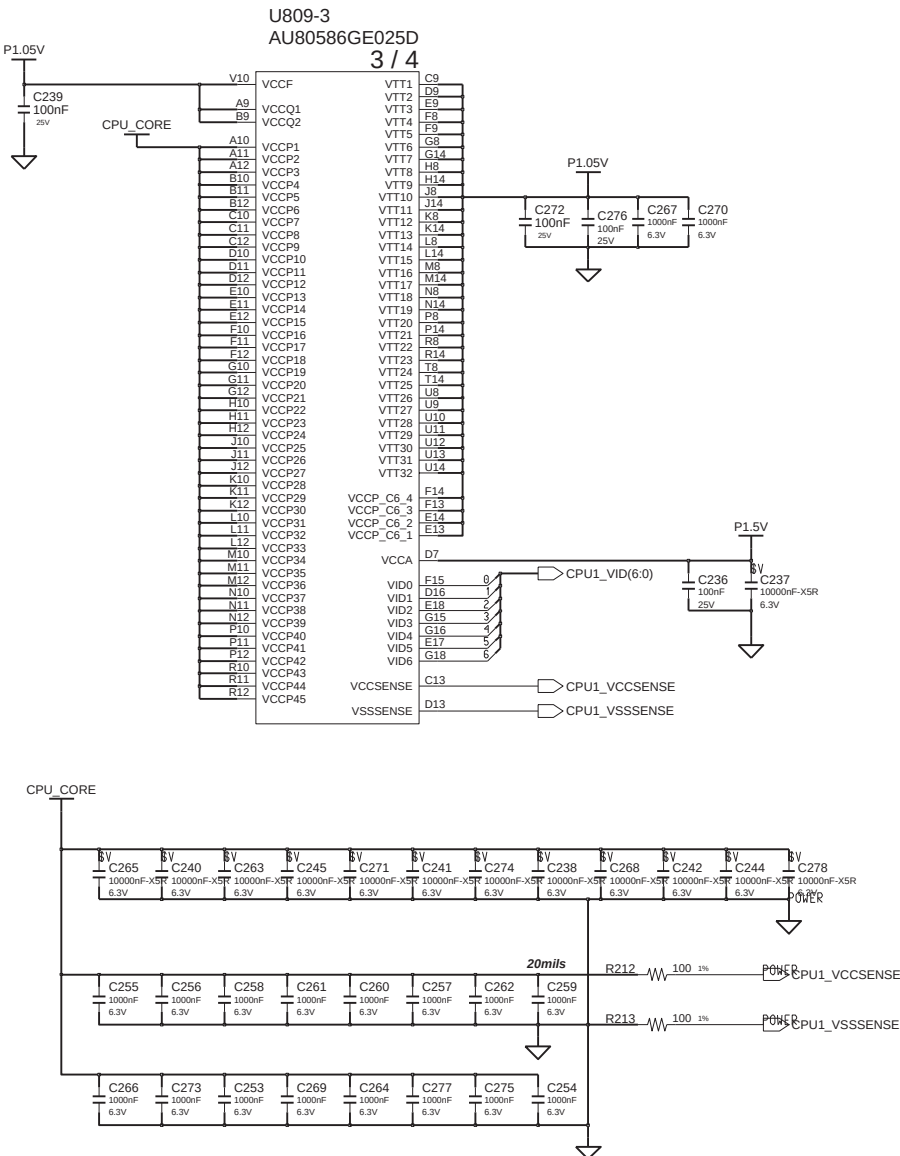


DESIGN	JUN, HONG	DATE	8/16/2009	TITLE CONFU BLOCK DIAGRAM	HANDBOOK TECH
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APPROVAL	,	REV	1.0		
MODULE CODE		LAST EDIT	August, 16, 2009 1:20:51 PM		
				PAGE	2 OF 40

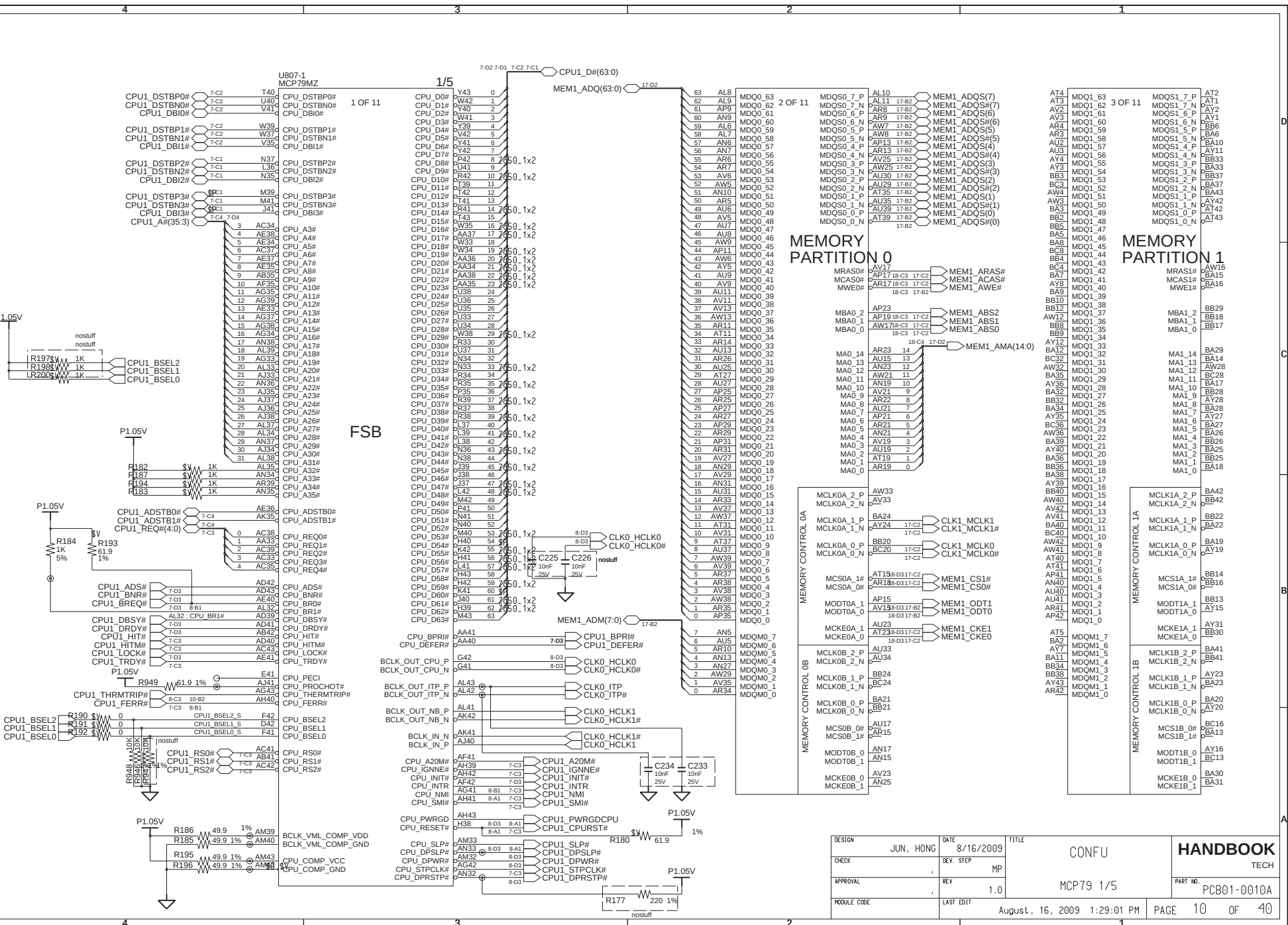
THERMAL IC



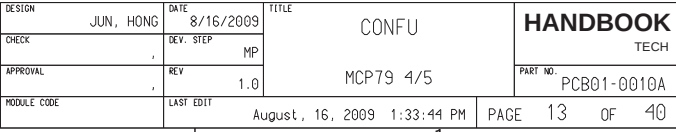
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CHECK		DEV. STEP	MP			TECH
APPROVAL		REV	1.0	THERMAL SENSOR & FAN CONTROL		PART NO. PCB01-0010A
MODULE CODE		LAST EDIT	August, 16, 2009 1:24:03 PM	PAGE	7	OF 40

DIAMONDVILLE (N270)

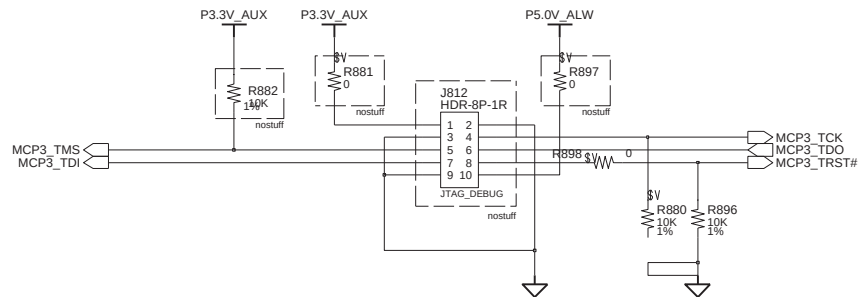
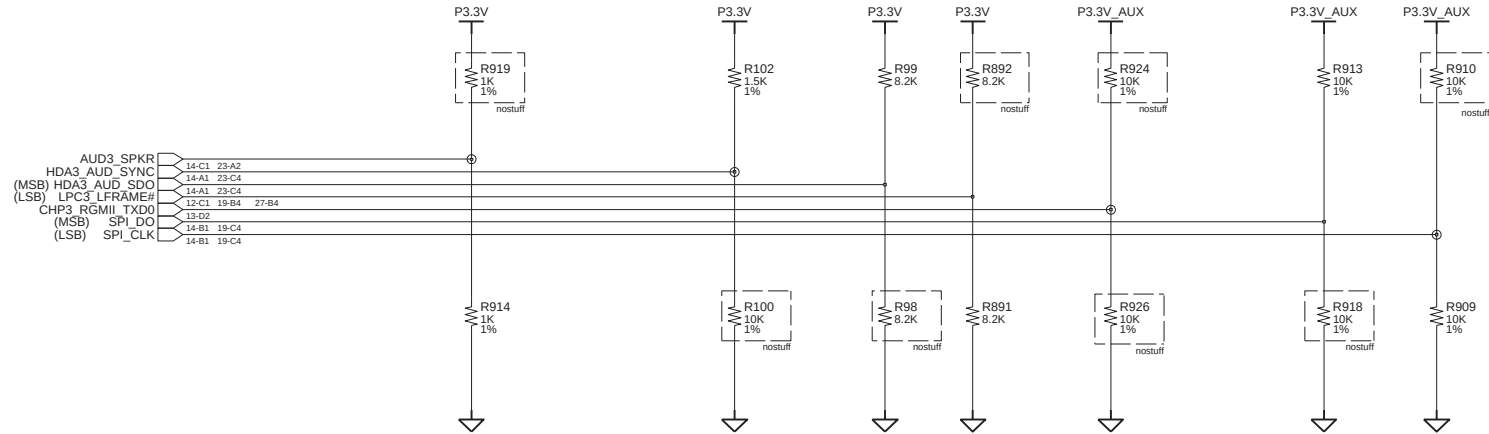
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APPROVAL	,	REV	1.0	CPU 2/2		PART NO.		PCB01-0010A	
MODULE CODE		LAST EDIT	August, 16, 2009 1:25:38 PM			PAGE	9	OF	40







REQUIRED SYSTEM STRAPS



DESIGN	JUN, HONG	DATE	8/16/2009	TITLE	CONFU	HANDBOOK
CHECK		DEV. STEP	MP			TECH
APPROVAL		REV	1.0	REQUIRED SYSTEM STRAPS	PART NO.	PCB01-0010A
MODULE CODE		LAST EDIT	August, 16, 2009 1:56:49 PM	PAGE	15	OF 40

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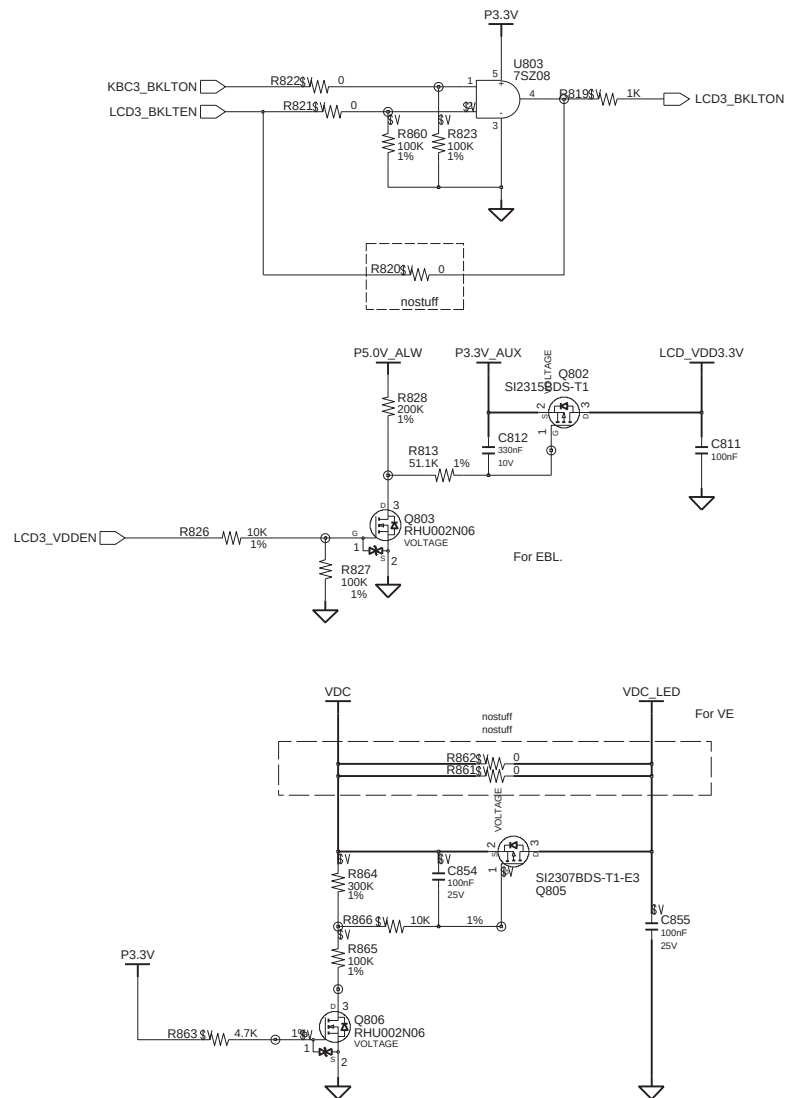
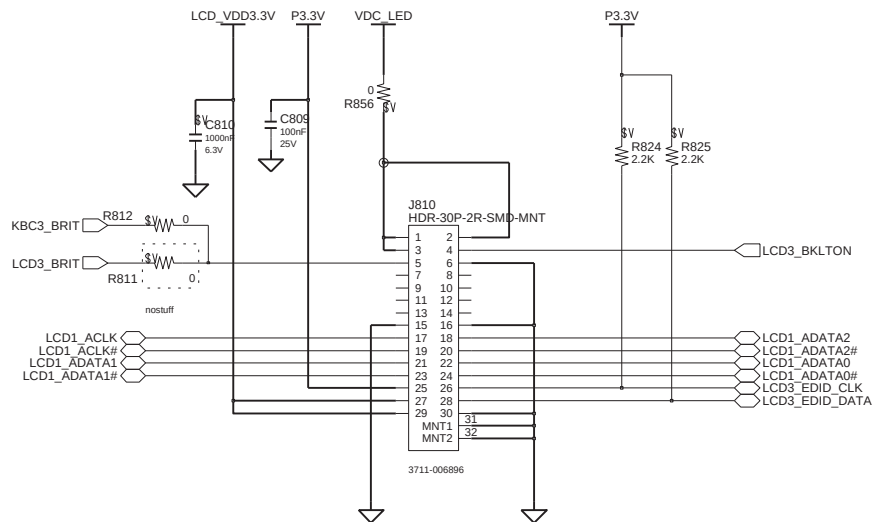
Pin connection diagram for the LPC3114 microcontroller. The diagram shows the microcontroller's pins connected to a P3.3V supply and a J819 HDR-10P-SMD connector. The connections are:

- LPC3_RST# to pin 1
- CLK3_DBG LPC to pin 2
- LPC3_LFRAME# to pin 3
- LPC3_LAD(3) to pin 4
- LPC3_LAD(2) to pin 5
- LPC3_LAD(1) to pin 6
- LPC3_LAD(0) to pin 7
- MNT1 to pin 10
- MNT2 to pin 11

A ground symbol is connected to the bottom of the connector.

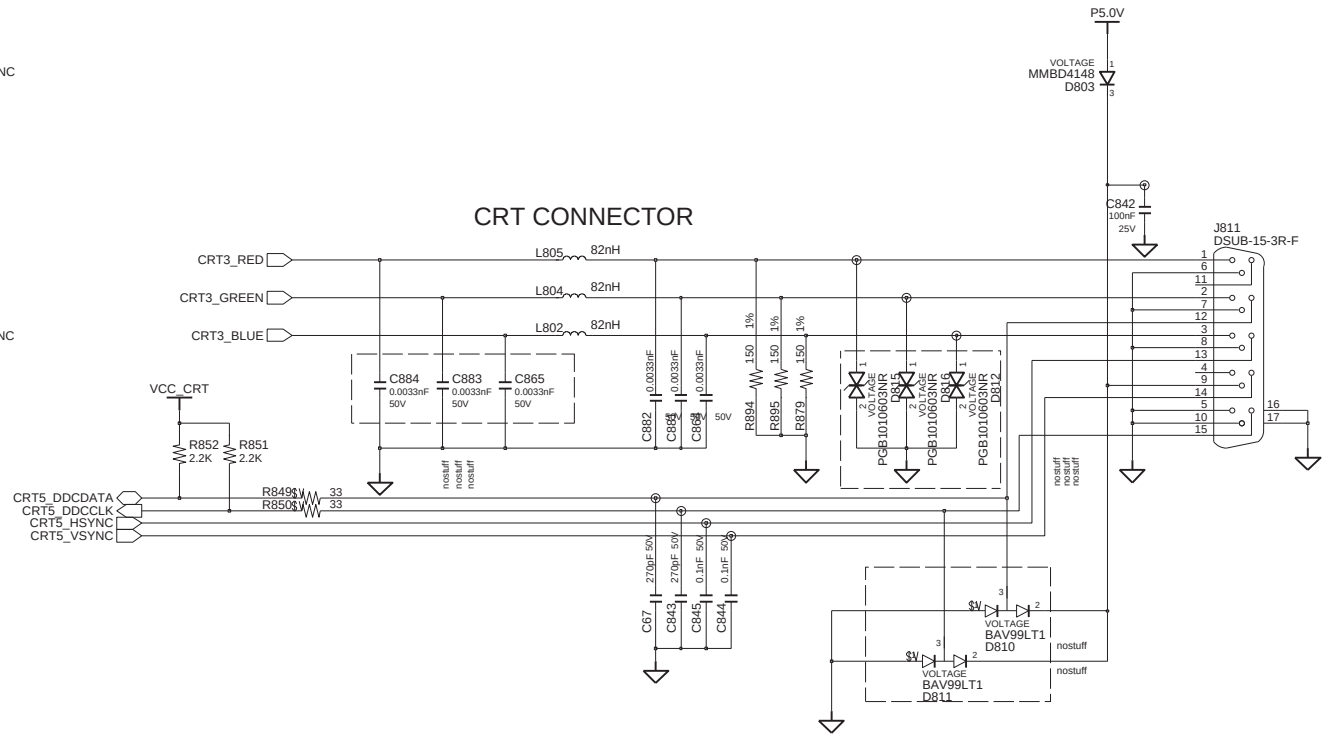
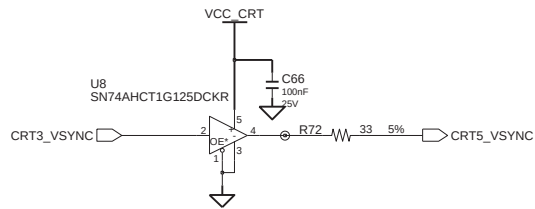
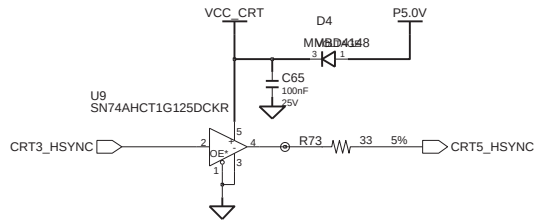
02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
	WITH INITIAL POST VALUE	88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TEST CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY "PRESS SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM BETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

DESIGN	JUN, HONG	DATE	8/16/2009	TITLE	CONFU BOIS	HANDBOOK	
CHECK		DEV. STEP	MP			TECH	
APPROVAL		REV	1.0			PART NO.	PCB01-0010A
MODULE CODE		LAST EDIT		August, 16, 2009 2:09:27 PM		PAGE	17 OF 40



DESIGN	JUN, HONG	DATE	8/16/2009	TITLE	CONFU	HANDBOOK
CHECK		DEV. STEP	MP			TECH
APPROVAL		REV	1.0		LCD CONN	PART NO. PCB01-0010A
MODULE CODE		LAST EDIT	August, 16, 2009 2:16:31 PM	PAGE	18	OF 40

CRT I/F



DESIGN	JUN, HONG	DATE	8/16/2009	TITLE		HANDBOOK
CHECK		DEV. STEP	MP			
APPROVAL		REV	1.0	CRT		PART NO.
		LAST EDIT		August, 16, 2009 3:02:05 PM		PCB01-0010A
MODULE CODE				PAGE	19	OF 40

HDMI

PEG3_TX2P_HDMI

PEG3_TX2N_HDMI

PEG3_TX1P_HDMI

PEG3_TX1N_HDMI

PEG3_TX0P_HDMI

PEG3_TX0N_HDMI

PEG3_TXCP_HDMI

PEG3_TXCN_HDMI

PEG3_TX2P_HDMI_B_MN

PEG3_TX2N_HDMI_B_MN

PEG3_TX1P_HDMI_B_MN

PEG3_TX1N_HDMI_B_MN

PEG3_TX0P_HDMI_B_MN

PEG3_TX0N_HDMI_B_MN

PEG3_TXCP_HDMI_B_MN

PEG3_TXCN_HDMI_B_MN

PEG5_HDMI_CLK

PEG5_HDMI_DATA

PEG3_HDMI_HPD

PEG5_HDMI_CLK_B_MN

PEG5_HDMI_DATA_B_MN

PEG3_HDMI_DATA

PEG5_HDMI_DATA

PEG3_HDMI_CLK

PEG5_HDMI_CLK

P3.3V

P3.3V

P3.3V

P5.0V

P5.0V_HDMI_TH_D_MN

VOLTAGE

D817

CRS06

C248

100nF

25V

HDMI

J814

HDMI-19P-FEMALE

TMDS_DATA2

TMDS_DATA2_SHIELD

TMDS_DATA2#

TMDS_DATA1

TMDS_DATA1_SHIELD

TMDS_DATA1#

TMDS_DATA0

TMDS_DATA0_SHIELD

TMDS_DATA0#

TMDS_CLOCK

TMDS_CLOCK_SHIELD

TMDS_CLOCK#

CEC

RESERVED

SCL

SDA

DDC_GROUND

5V_POWER

HOT_PLUG_DETECT

MNT1

MNT2

MNT3

MNT4

R966

R965

2.2K

2.2K

R964

0

R963

1K

R961

100K

1%

C917

0.01uF

50V

C918

0.01uF

50V

C916

100nF

25V

ESD

BAV99LT1

D5

BAV99LT1

D6

Q811

RHU002N06

R968

0

Q810

RHU002N06

R967

0

R970

10K

1%

R969

10K

1%

Q811

RHU002N06

R968

0

Q810

RHU002N06

R967

0

R970

10K

1%

R969

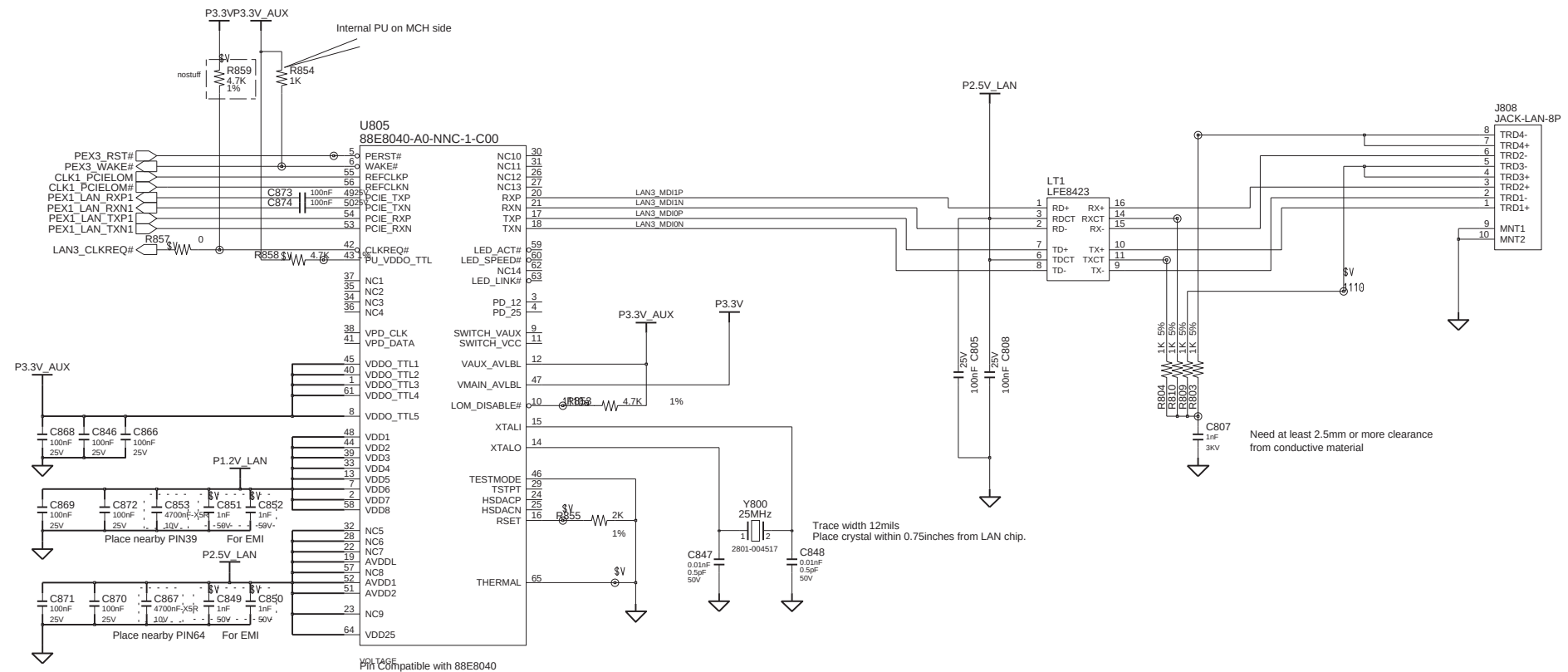
10K

1%

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CHECK		DEV. STEP	MP			
APPROVAL		REV	1.0			
MODULE CODE		LAST EDIT				PART NO. PCB01-0010A
August, 16, 2009 3:05:38 PM						PAGE 20 OF 40

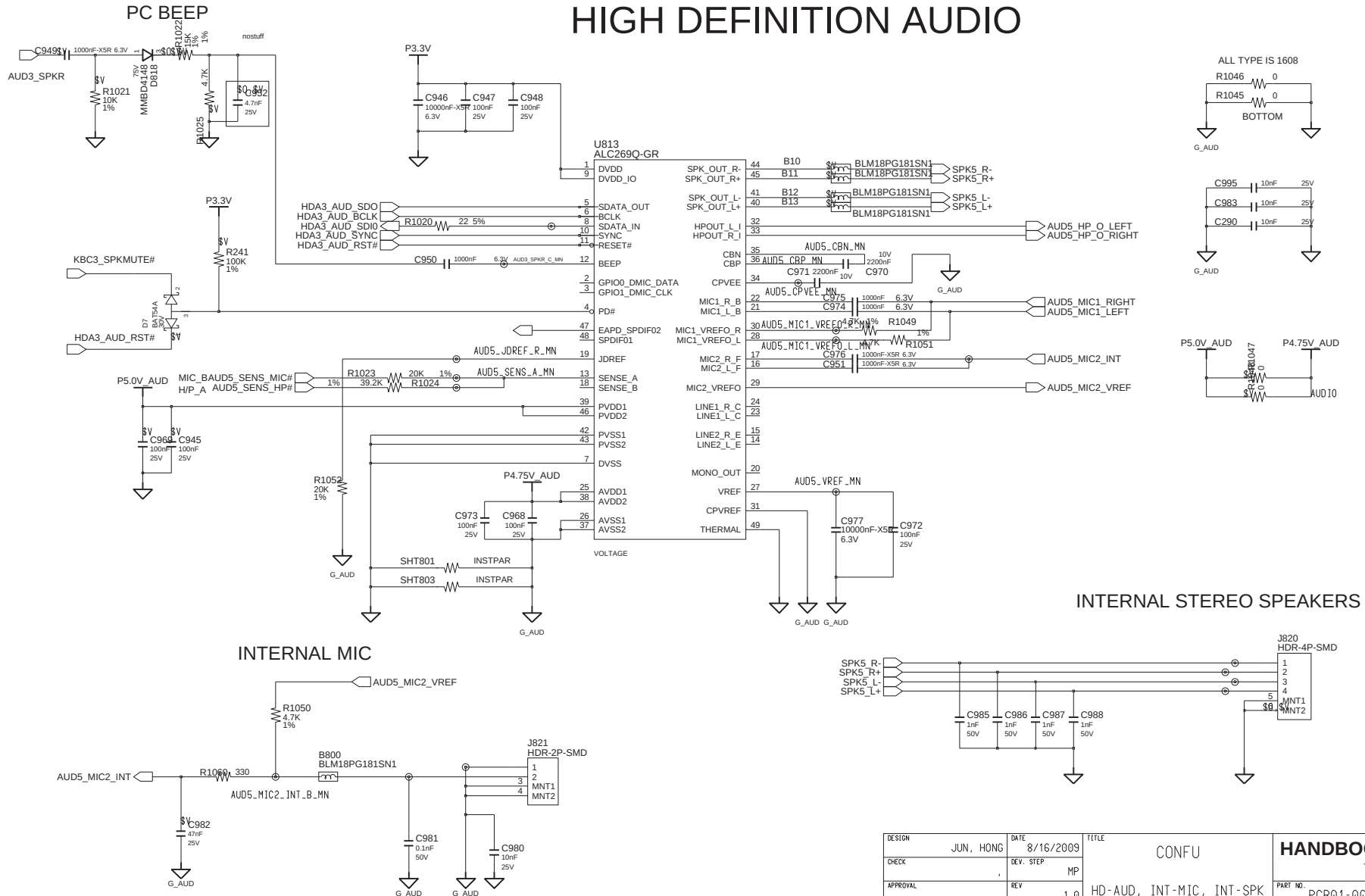
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MODULE CODE	LAST EDIT						

Marvell 88E8040 (WIRED LAN)



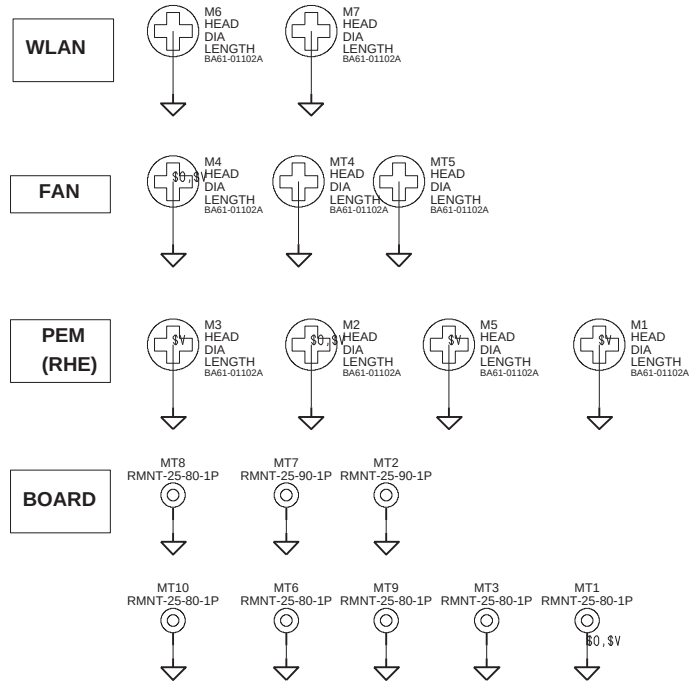
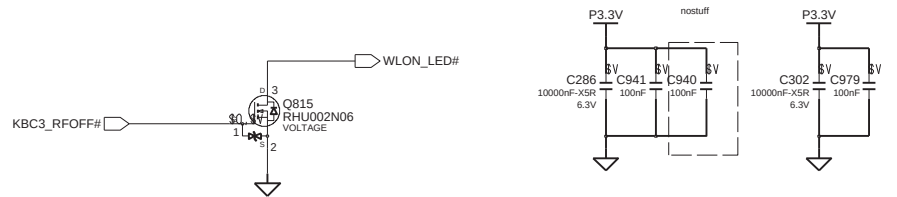
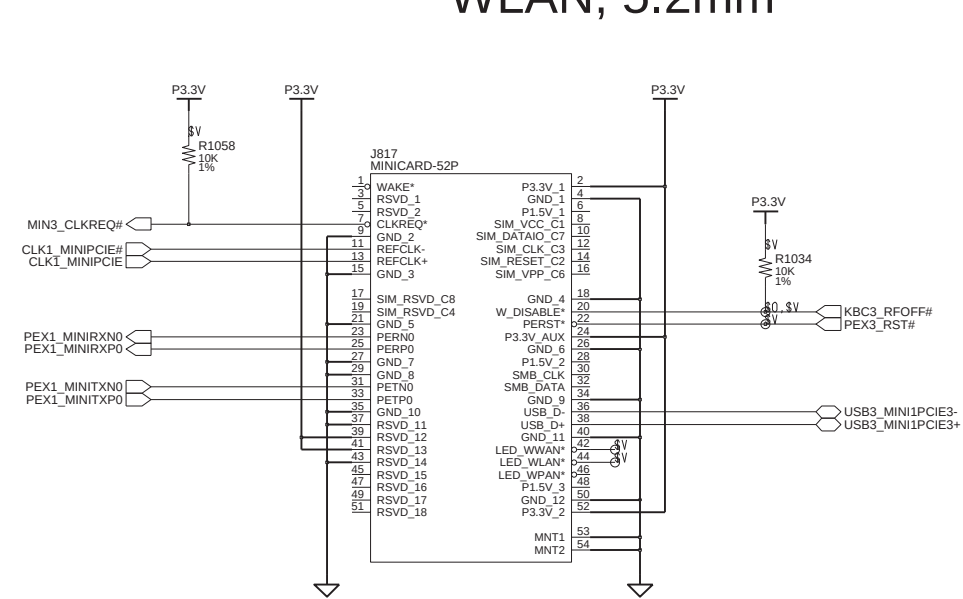
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MODULE CODE		LAST EDIT	August, 16, 2009 3:05:59 PM					

HIGH DEFINITION AUDIO

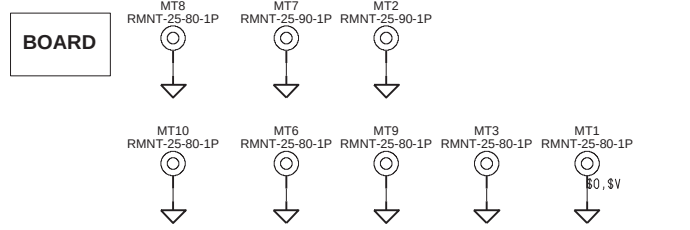
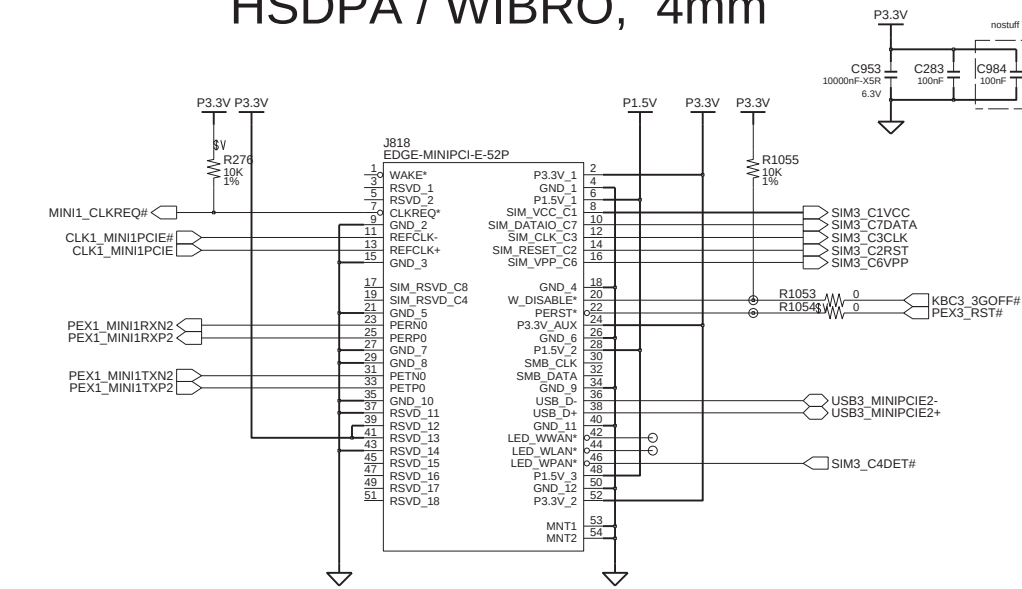


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APPROVAL		REV	1.0	HD-AUD, INT-MIC, INT-SPK	PART NO.	
MODULE CODE		LAST EDIT	August, 16, 2009 12:38:31 AM	PAGE	22 OF 40	

WLAN, 5.2mm

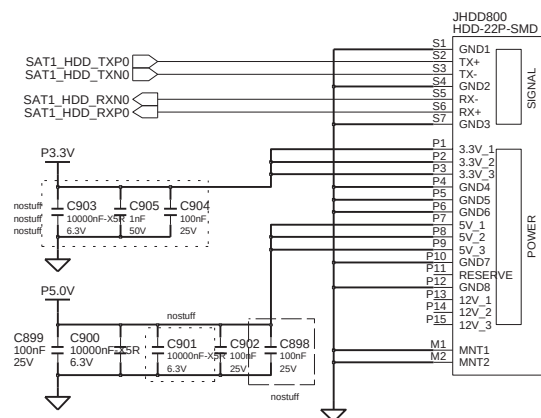


HSDPA / WIBRO, 4mm



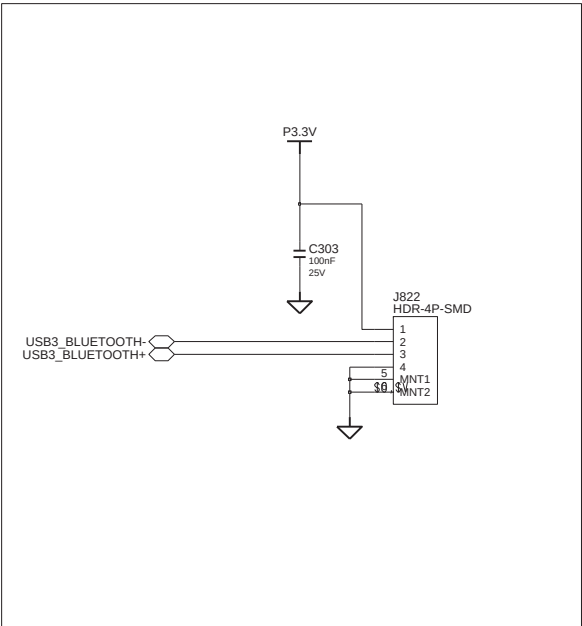
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MODULE CODE		LAST EDIT	August, 16, 2009 3:07:44 PM	PAGE	23	OF 40

A B C D

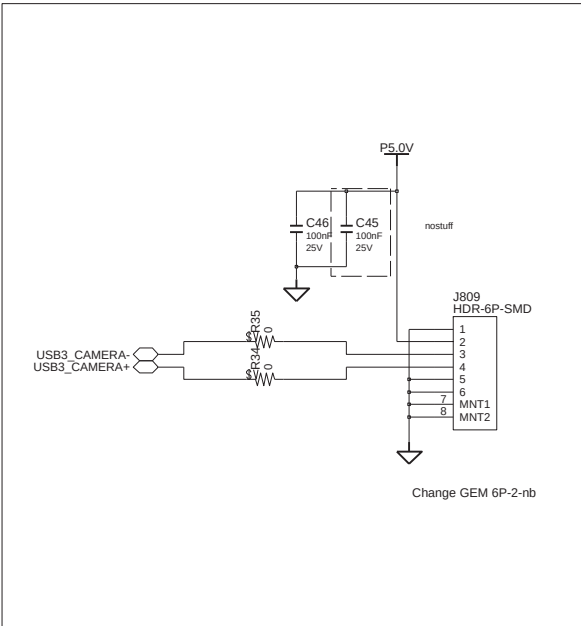
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USB I/F Devices

Bluetooth Interface

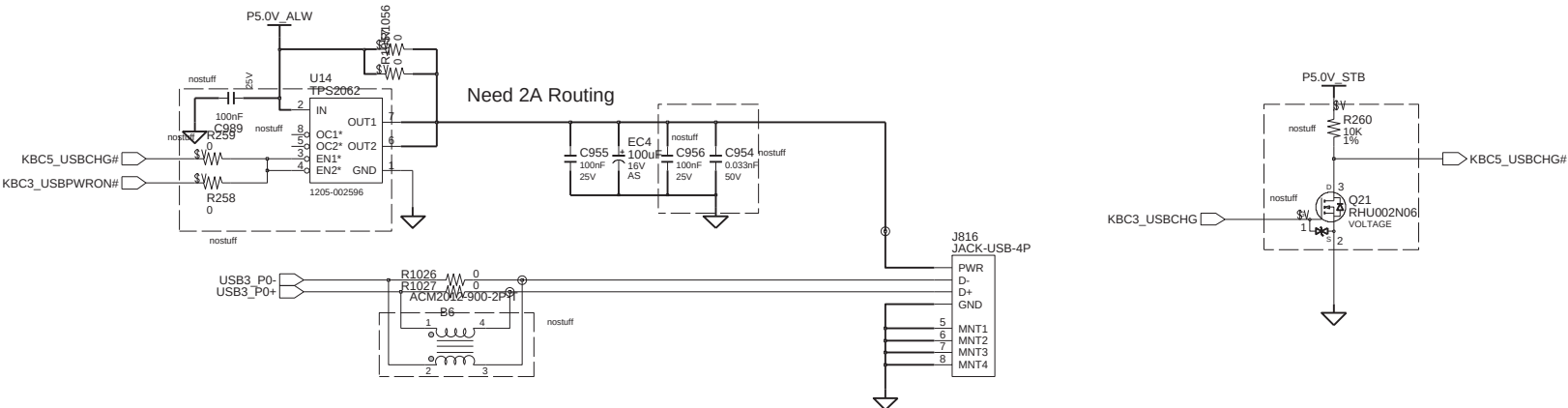


CAMERA

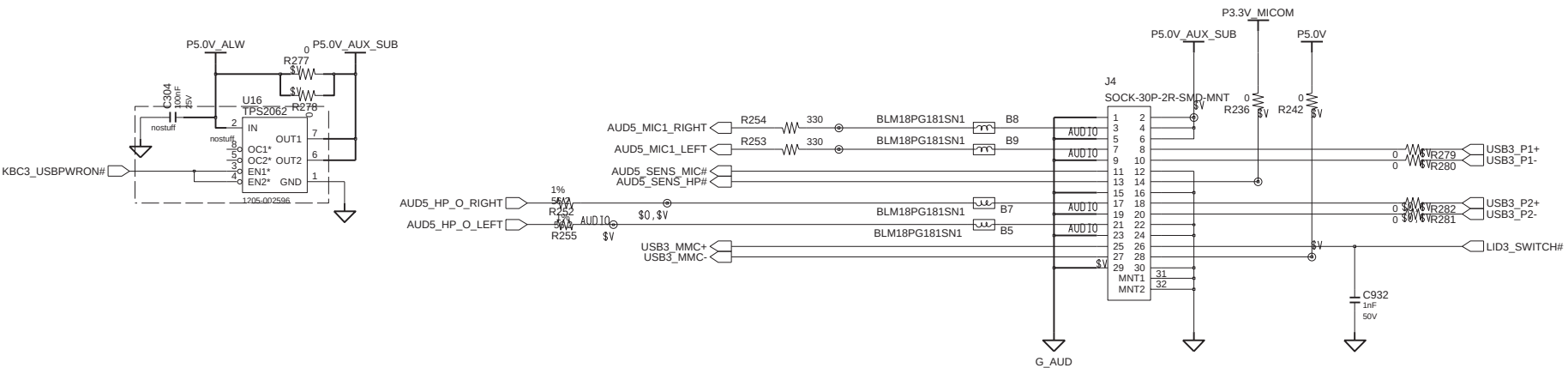


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MODULE CODE		LAST EDIT	August, 16, 2009 3:08:55 PM	PAGE	25	OF 40

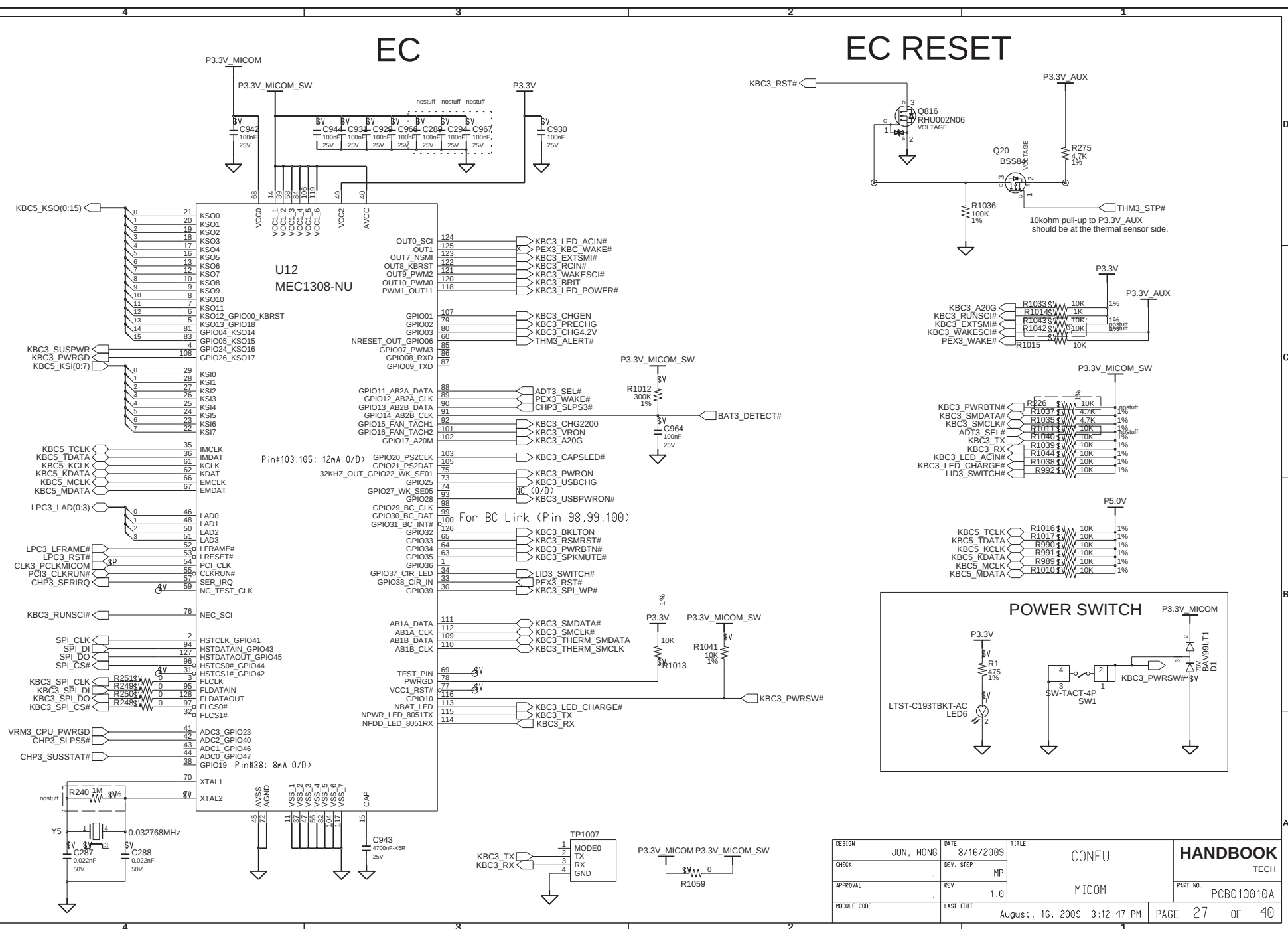
1 PORT USB CONNECTOR



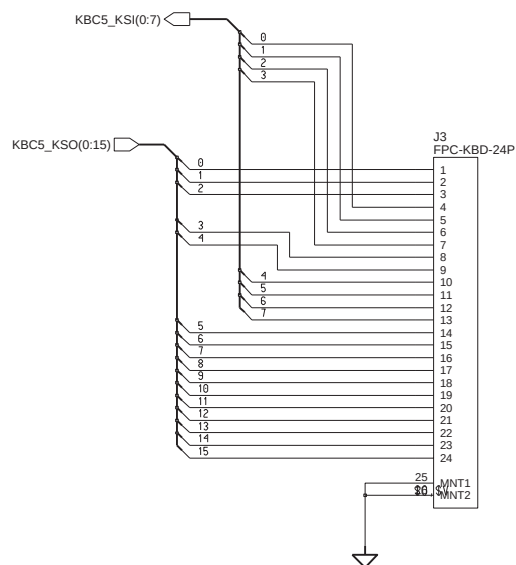
MAIN TO SUB CONN



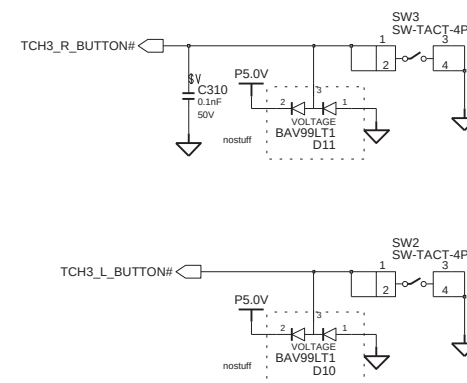
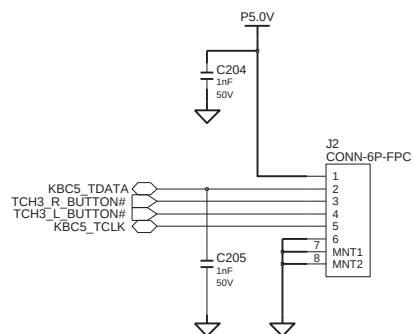
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CHECK		DEV. STEP	MP				
APPROVAL		REV	1.0	USB0, MB TO SUB CONN		PART NO.	PCB01-0010A
MODULE CODE		LAST EDIT		August, 16, 2009 3:09:49 PM		PAGE	26 OF 40



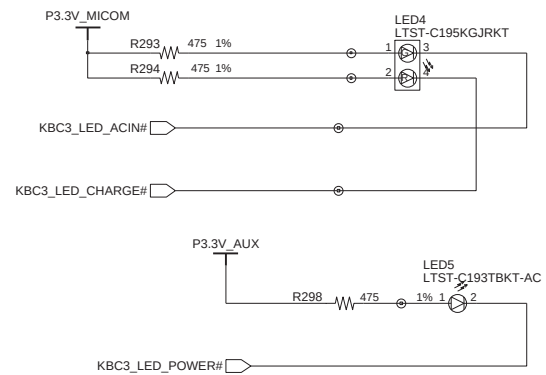
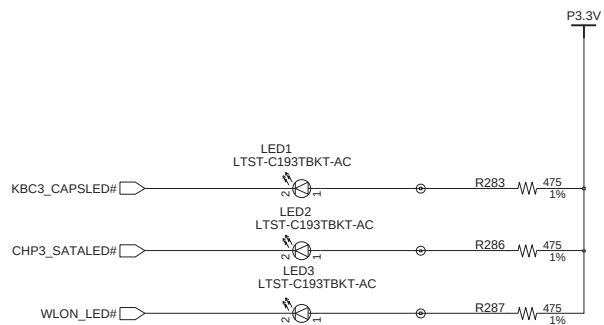
KEYBOARD



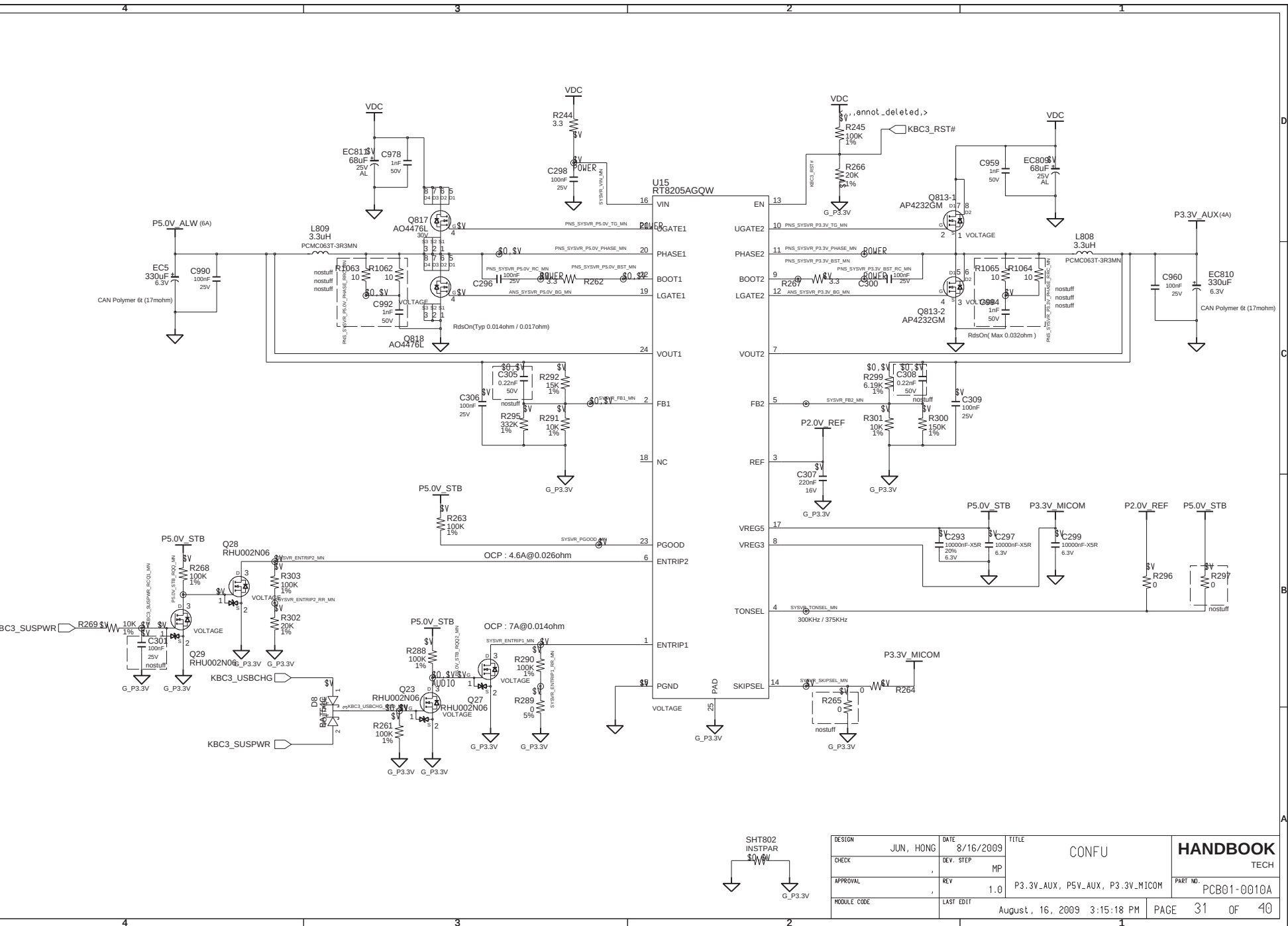
TOUCHPAD



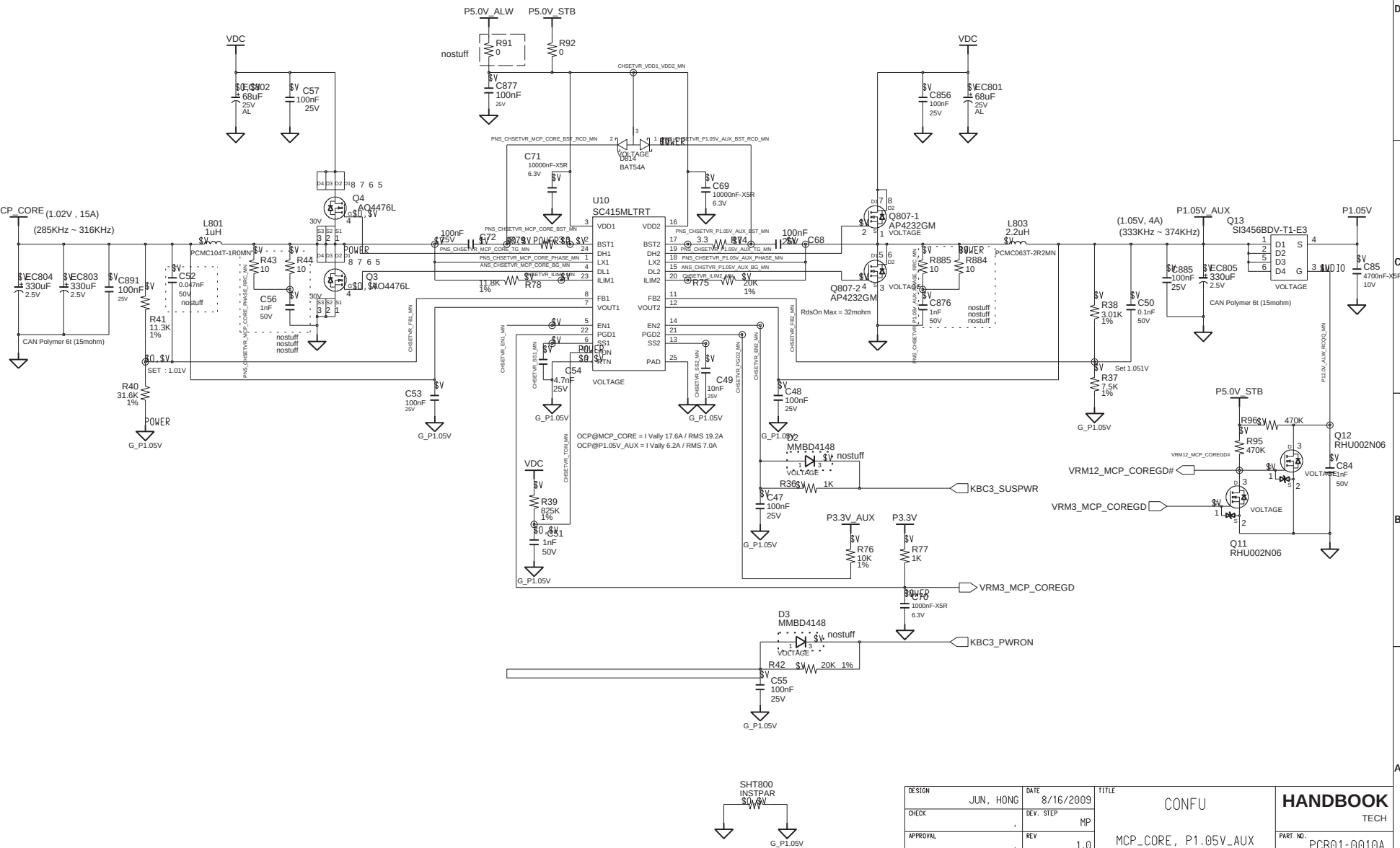
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CHECK		DEV. STEP	MP			TECH
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MODULE CODE		LAST EDIT	August, 16, 2009 3:13:12 PM	PAGE	28	OF 40



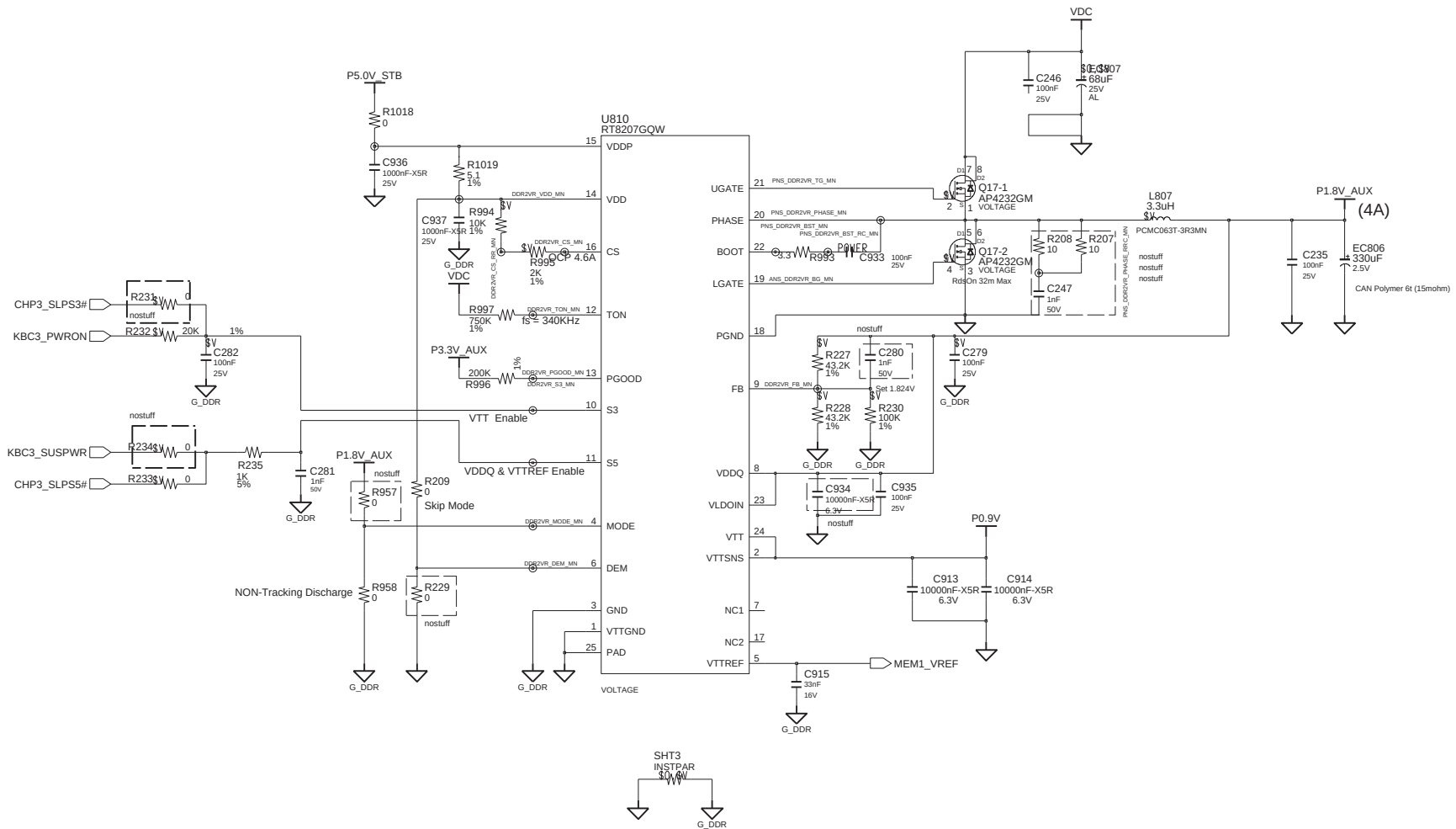
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CHECK	.	DEV. STEP	MP			TECH
APPROVAL	.	REV	1.0	LED		PART NO. PCB01-0010A
MODULE CODE		LAST EDIT	August, 16, 2009 3:13:53 PM	PAGE	29	OF 40



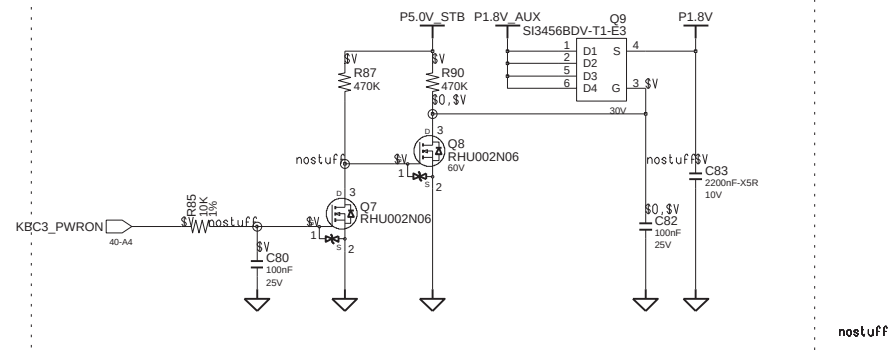
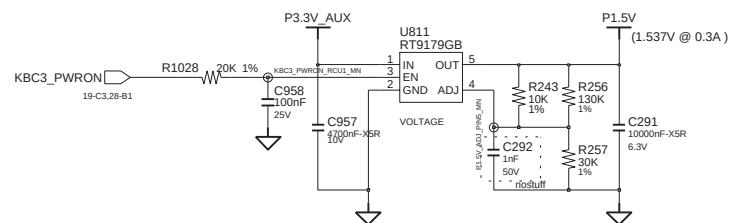
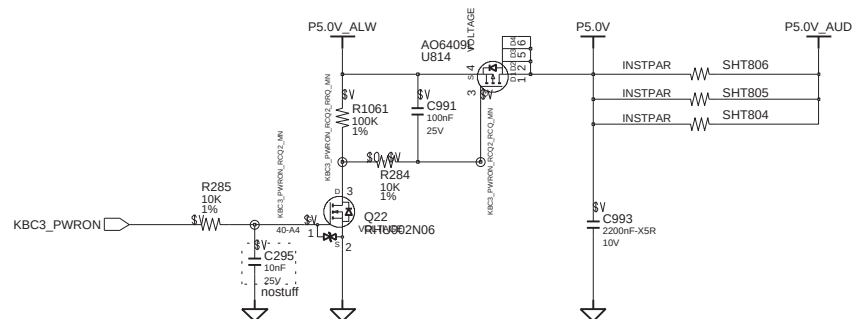
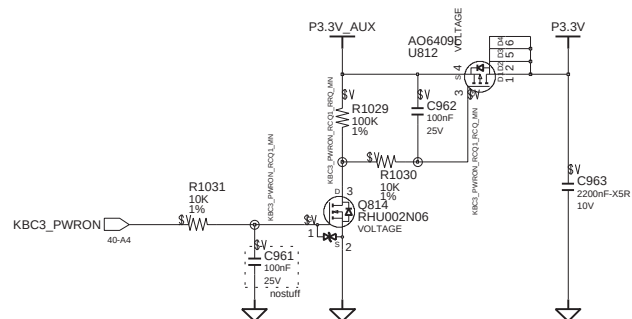
MCP_CORE & P1.05V_AUX



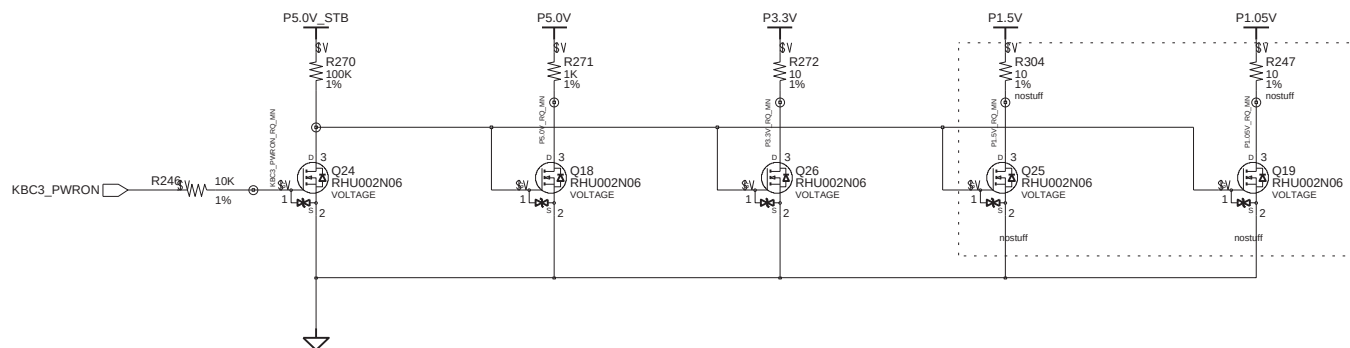
DDR2 Power



DESIGN	JUN, HONG	DATE	8/16/2009	TITLE	CONFU	HANDBOOK
CHECK		DEV. STEP	MP			TECH
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MODULE CODE		LAST EDIT	August, 16, 2009 3:16:06 PM	PAGE	33	OF 40

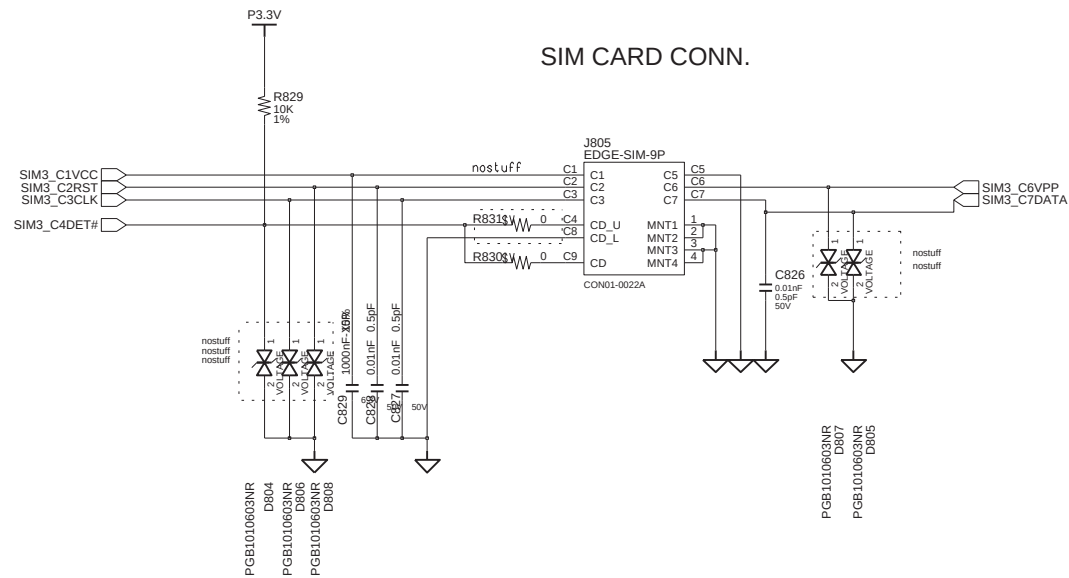


DESIGN	JUN, HONG	DATE	8/16/2009	TITLE	CONFU	HANDBOOK
CHECK		DEV. STEP	MP			TECH
APPROVAL		REV	1.0	LOAD SW CONTROL		PART NO. PCB01-0010A
MODULE CODE		LAST EDIT	August, 16, 2009 3:16:43 PM	PAGE	35	OF 40



DESIGN	JUN, HONG	DATE	8/16/2009	TITLE	CONFU	HANDBOOK
CHECK		DEV. STEP	MP			TECH
APPROVAL		REV	1.0		DISCHARGER	PART NO. PCB01-0010A
MODULE CODE		LAST EDIT	August, 16, 2009 3:17:00 PM	PAGE	36	OF 40

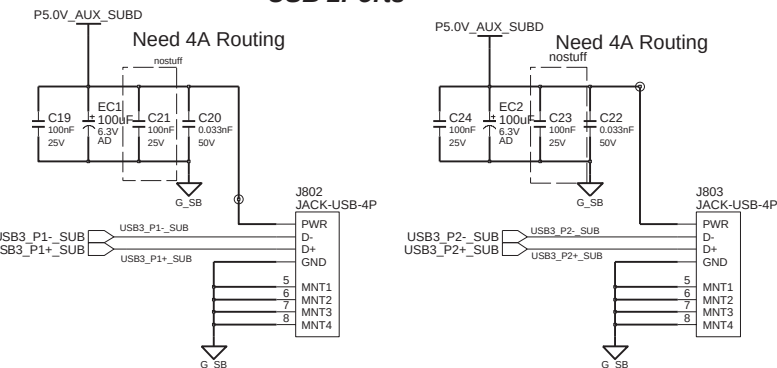
SIM Card



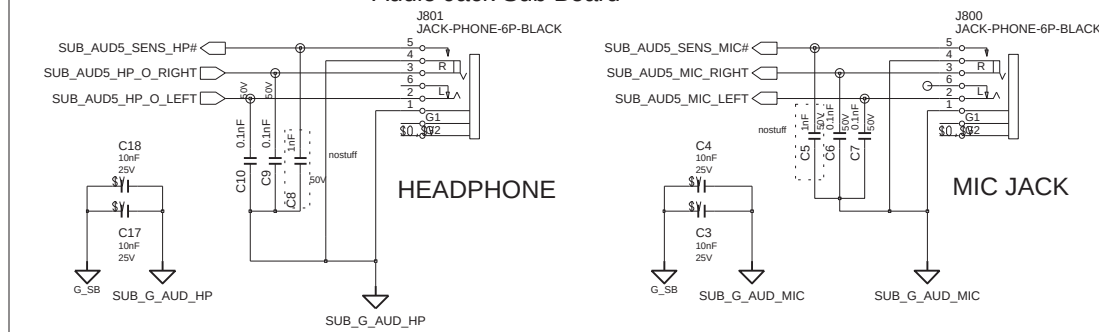
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CHECK		DEV. STEP	MP			
APPROVAL		REV	1.0	SIM CARD CONN		PART NO.
MODULE CODE		LAST EDIT	August, 16, 2009 3:17:23 PM			PAGE

SUB Board (USB 2Ports, Audio 2Ports, MMC)

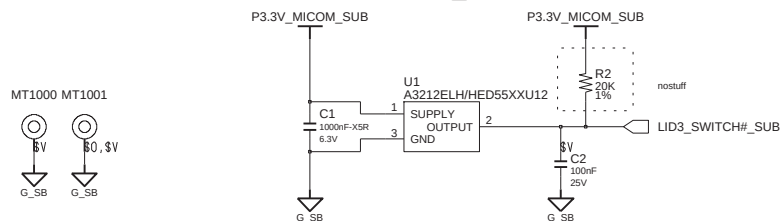
USB 2Ports



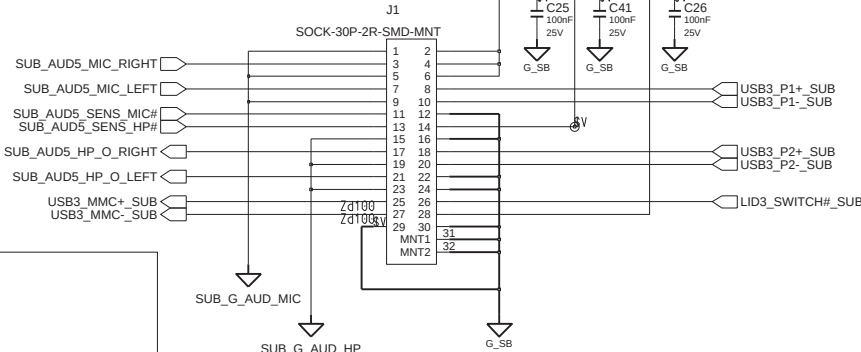
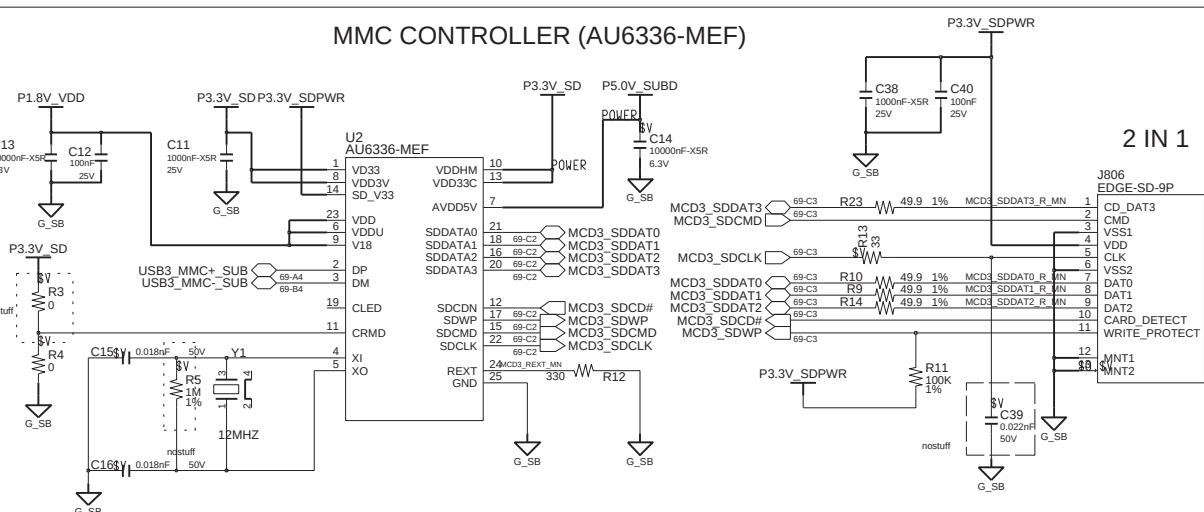
Audio Jack Sub Board



LID_SWITCH



MMC CONTROLLER (AU6336-MEF)



DESIGN	JUN, HONG	DATE	8/16/2009	TITLE		HANDBOOK TECH
CHECK		DEV. STEP	MP	CONFU		
APPROVAL		REV	1.0	SUB BRD		
MODULE CODE			LAST EDIT		PART NO.	
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			PAGE		38 OF 40	

