

COMPAL CONFIDENTIAL

MODEL NAME : VAL91

PCB NO : LA-9934P(eDP)

GPIO P/N: 2012.8.1 Rev 2.7

BOM P/N :

X76 of SPI:

X7650731L03

SA000039A30 (64M W25Q64FVSSIQ)

SA00003K820 (32M W25Q32FVSSIQ)

X7650731L04

SA00006N000 (32M MX25L3273EM2I-10G)

SA00006N100 (64M MX25L6473EM2I-10G)

X76 of VRAM:

X7650731L53 - SAMSUNG

SA00006EU1L (128M32 K4G41325FC-HC04)

SD034453180 (4.53K +-1% 0402)

X7650731L54 - HYNIX

SA00006O41L (128M32/2.5G H5GC4H24MFR-T2C)

SD000000680 (8.45K +-1% 0402)

SALADO 14 HSW DSC

HASWELL + LYNX POINT

2013-07-04

REV : 1.0 (A00)

@ : Nopop Component

CONN@ : Connector Component

SPI@ : For X76 SPI

VRAM@ : For X76 VRAM

14DSC

EMC@: EMI/RF/ESD ask to add

V

CXDP@ : CPU XDP

PXDP@ : PCH XDP

COMPRESSED IMAGE

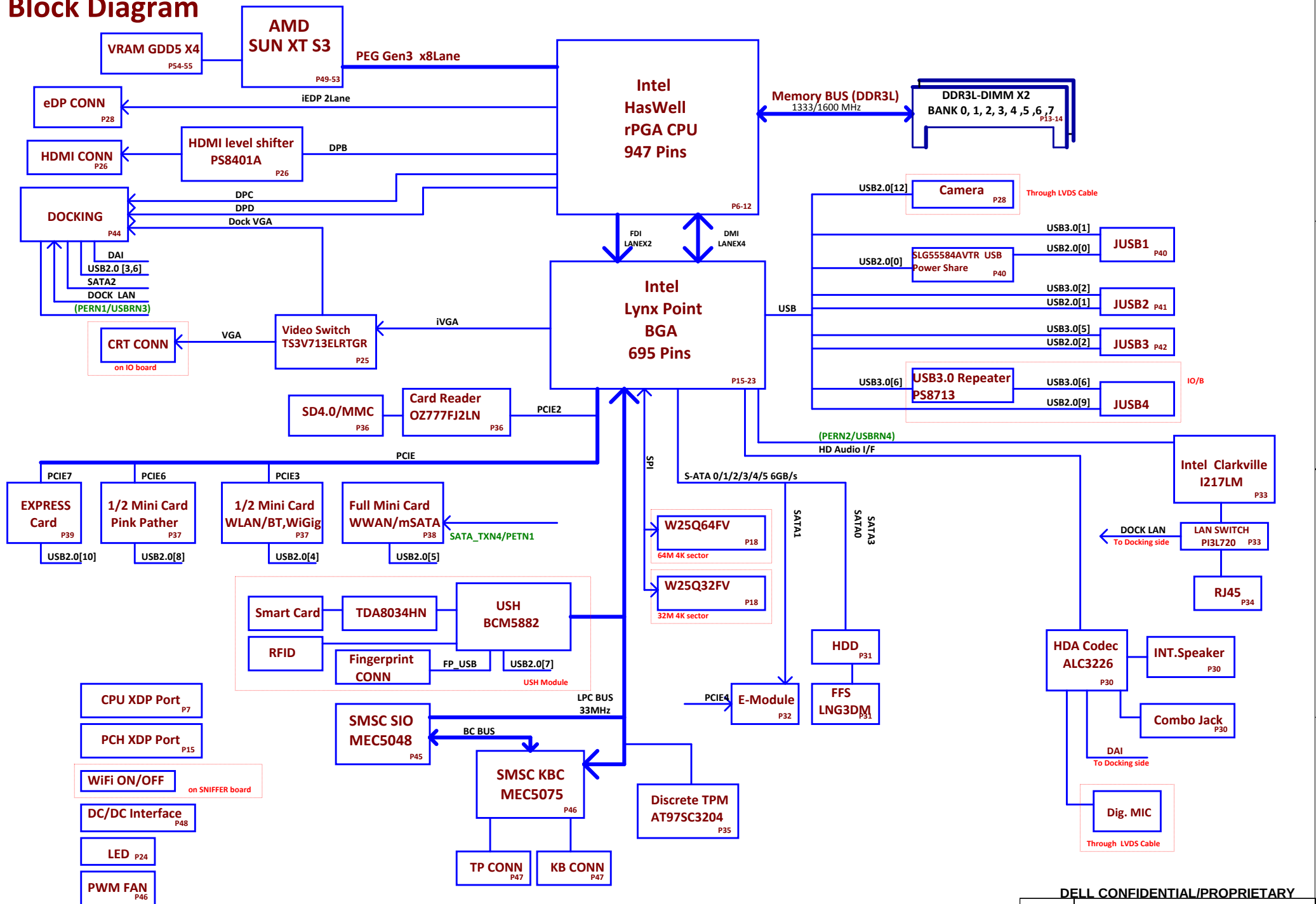
MB PCB	
Part Number	Description
DAA0006L000	PCB 0YH LA-9932P REV0 M/B DSC 6

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Block Diagram



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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+PWR_SRC +PWR_SRC_S +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +VCC_CORE +1.05V_RUN +GPU_CORE +1.35V_MEM_GFX +1.8V_RUN_GFX +VGA_PCIE +3.3V_RUN_GFX +VDDCI	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB 2.0 PORT#	USB 3.0 PORT#	DESTINATION
	0	1	Rear Side (JUSB1)
	1	2	Right Side TOP (JUSB2)
	2	5	Right Side bottom (JUSB3)
	3	3 (PERN1/USBRN3)	DOCKING (JDOCK1)
	4		WLAN (JMINI2)
	5		WWAN (JMINI1)
	6		DOCKING (JDOCK1)
	7		USH (JUSH1)
	8		Pink Pather (JMINI3)
	9	6	Left Side (JUSB4)
	10		Express card (JEXP1)
	11		None
	12		CAMERA (JCAM1)
	13		LCD Touch

PCI EXPRESS	DESTINATION
Lane 1 (SATA_TXN4/PETN1)	WWAN (JMINI1) SATA by default
Lane 2 (SATA_RXN5/PERN2)	None
Lane 2 (PERN2/USBRN4)	10/100/1G LOM
Lane 3	WLAN (JMINI2)
Lane 4	E3 Module Bay (JSATA2)
Lane 5	None
Lane 6	Pink Pather (JMINI3)
Lane 7	Express card (JEXP1)
Lane 8	MMI

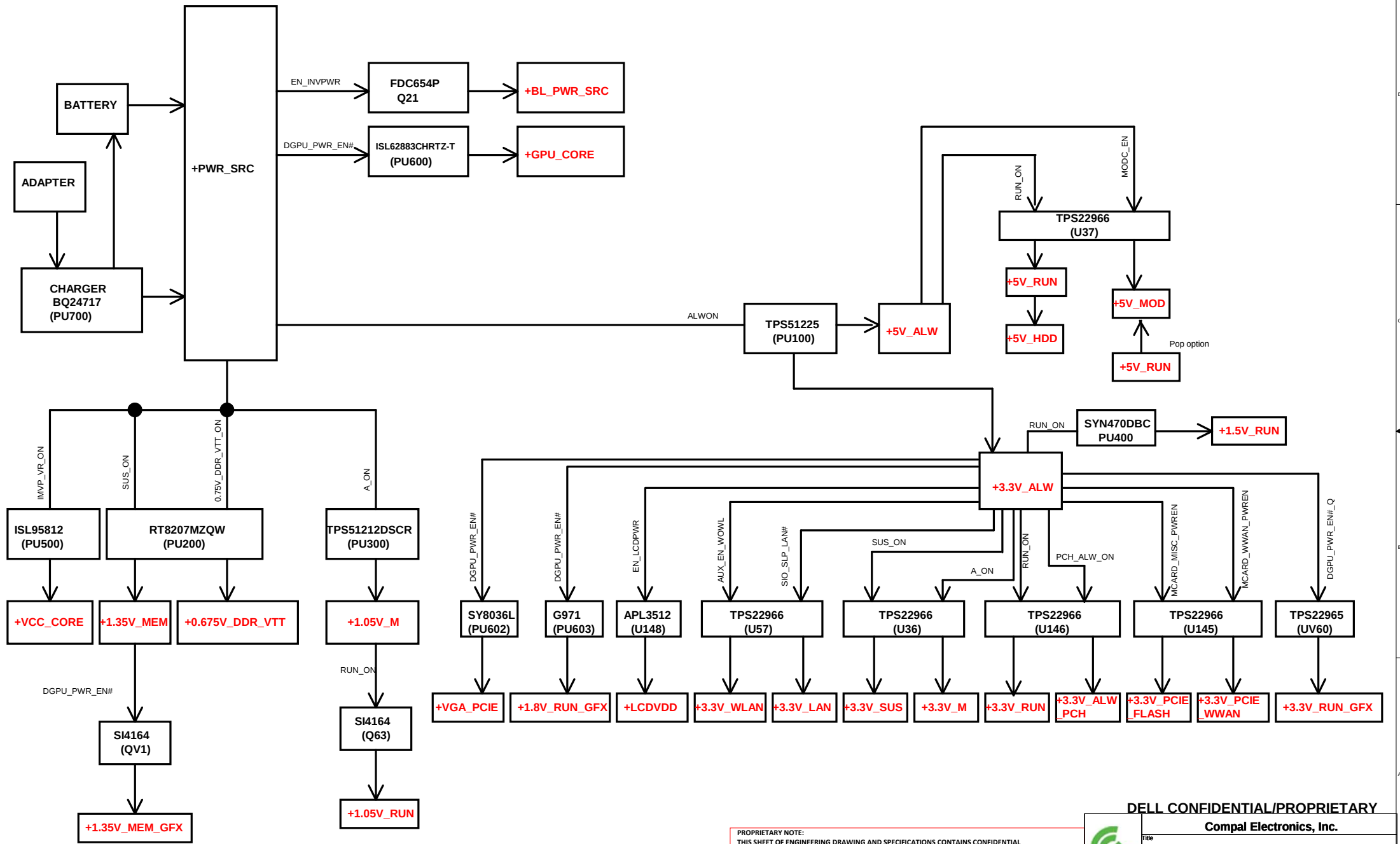
SATA	DESTINATION
SATA 0	HDD (JSATA1)
SATA 1	ODD (JSATA2)
SATA 2	Dock (JDOCK1)
SATA 3	NA
SATA 4 (SATA_TXN4/PETN1)	WWAN (JMINI1) SATA by default

DISPLAY Ports On CPU	Connetion
DDIB	MB HDMI (JHDMI1)
DDIC	Dock DP port 1
DDID	Dock DP port 2

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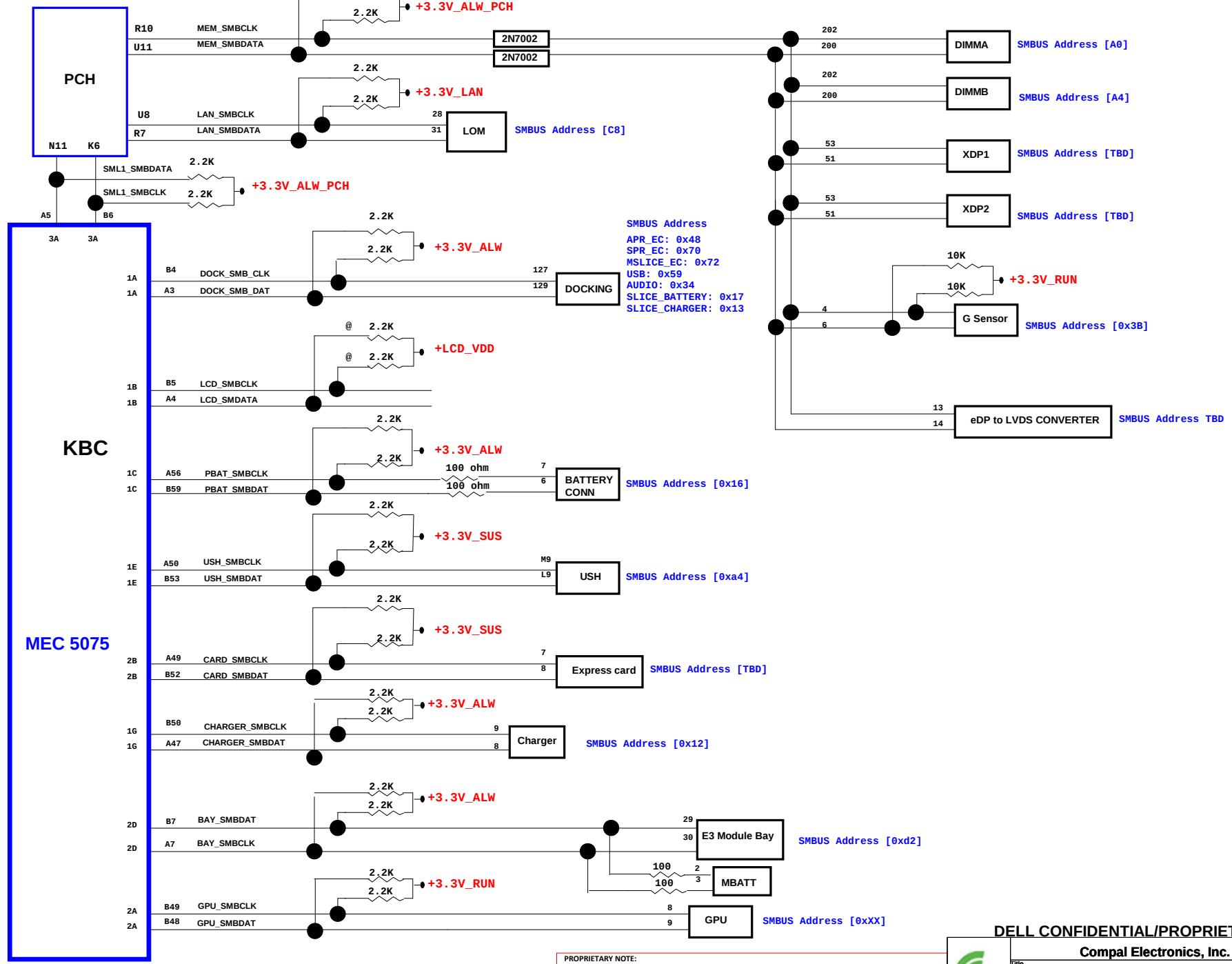
Power Rail

LA-9934P

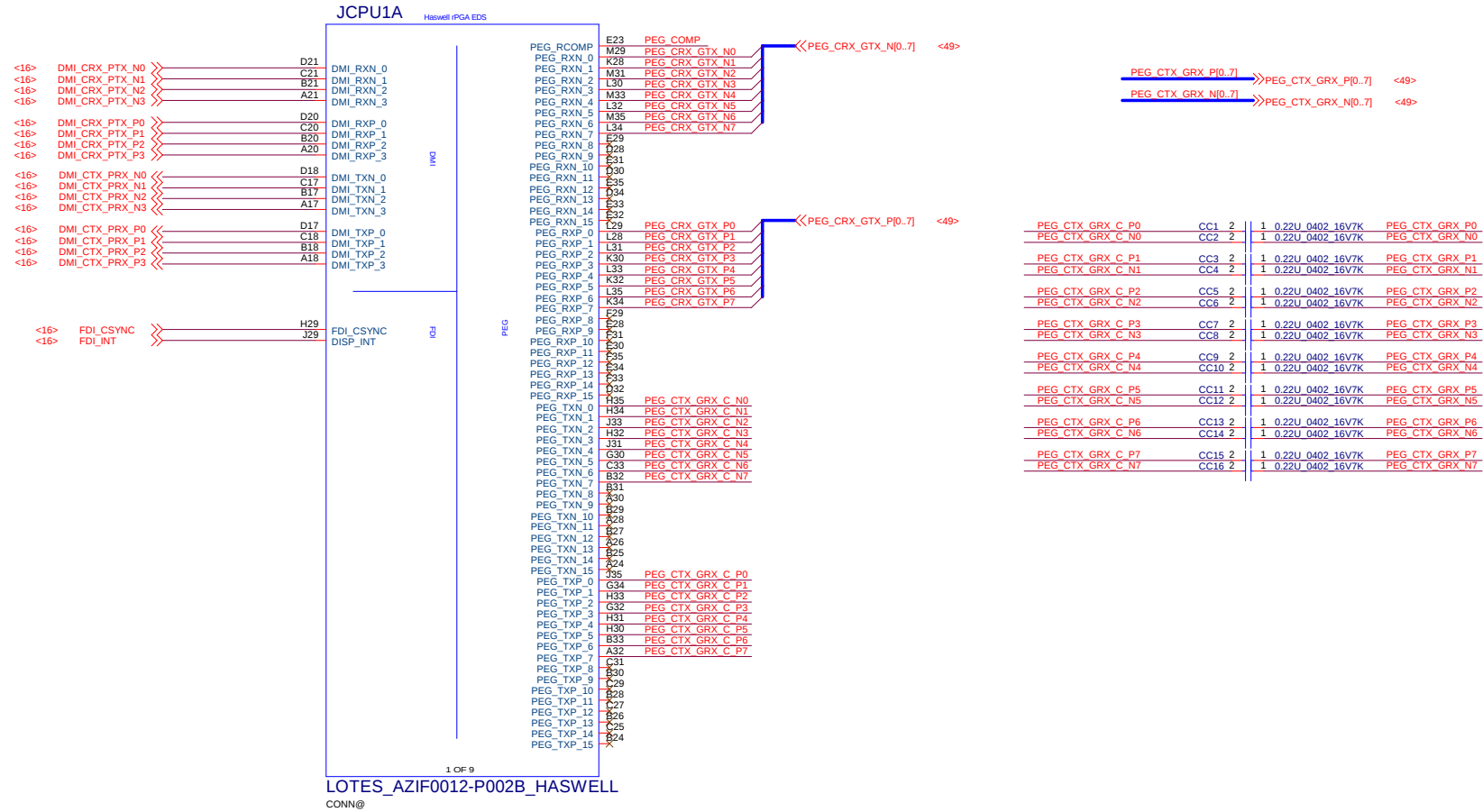
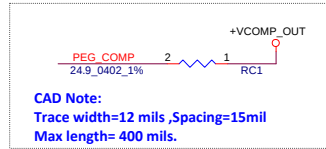
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SMBUS Address [0x9a]



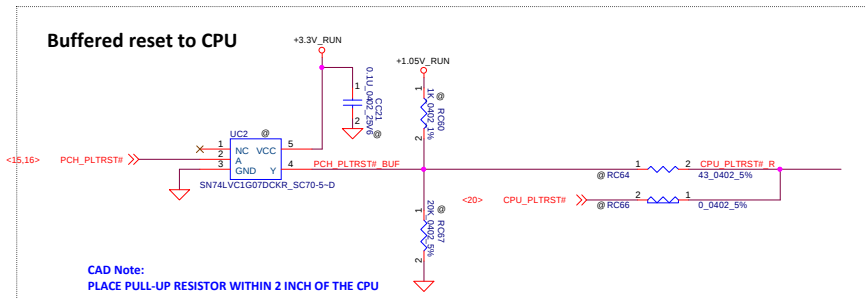
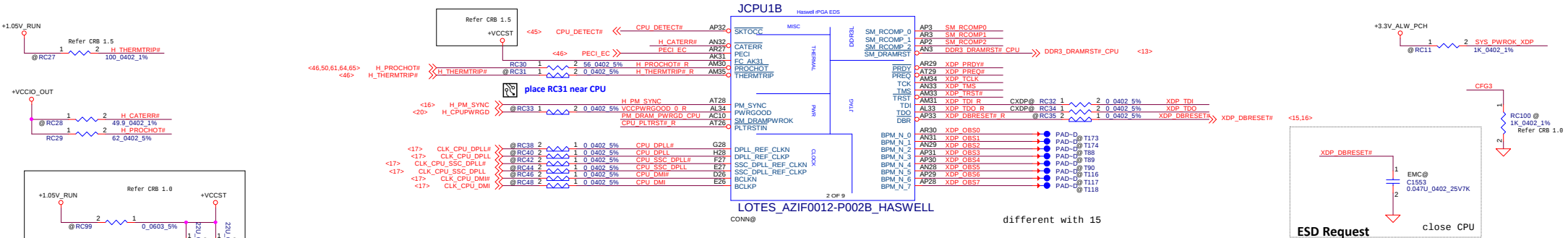
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[illegible]

PU/PD for JTAG signals

The diagram shows the power-up and power-down behavior for JTAG signals. The signals are represented by colored lines (red, blue, green, purple) with timing markers. The signals are:

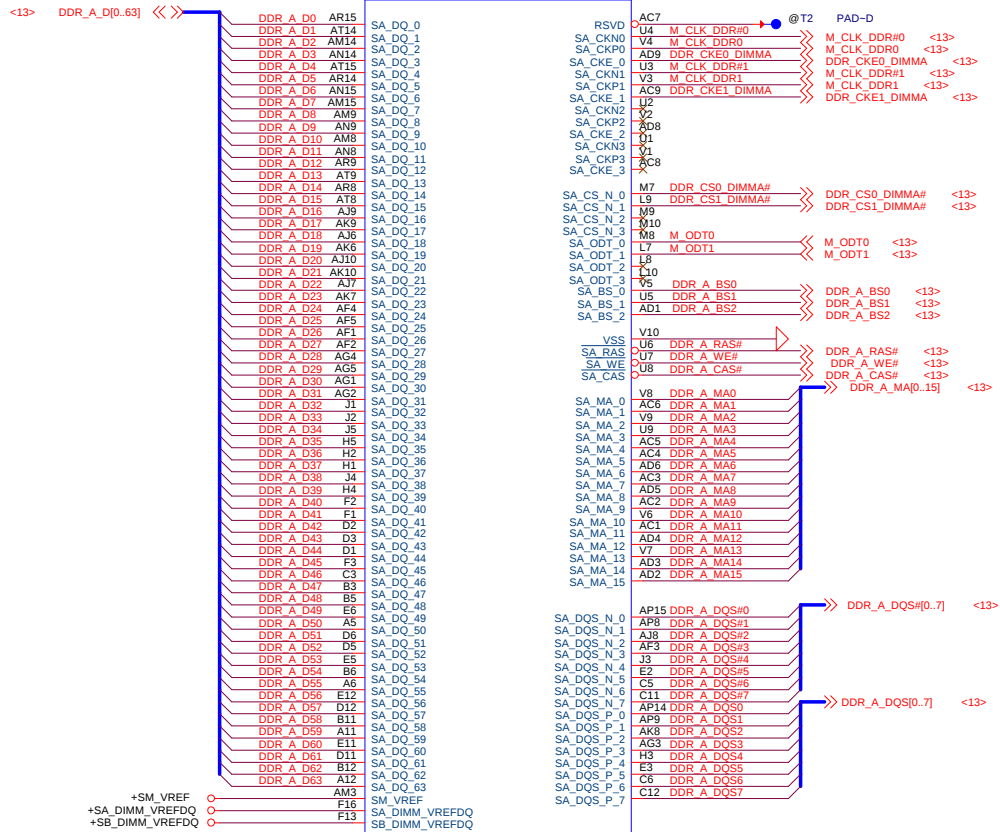
- XDP DBARESET#**: Red line, RC52 2, 1 K, 0402 1%, EMC0.
- XDP TMS**: Blue line, @ RC53 2, 1 51 0402 1%.
- XDP TDI**: Blue line, @ RC54 2, 1 51 0402 1%.
- XDP PREQ#**: Green line, @ RC55 2, 1 51 0402 1%.
- XDP TDO**: Purple line, CXDP0 RC57 2, 1 51 0402 1%.
- XDP TCLK**: Blue line, RC59 2, 1 51 0402 1%.
- XDP TRST#**: Purple line, RC62 2, 1 51 0402 1%.

The signals are connected to a +3.3V RUN supply and a +1.05V RUN supply. The signals are shown with a delay of 2 ns and a rise/fall time of 1 ns.

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JCPU1C Haswell (PGA) EDS



LOTES_AZIF0012-P002B_HASWELL
CONN@

JCPU1D Haswell (PGA) EDS

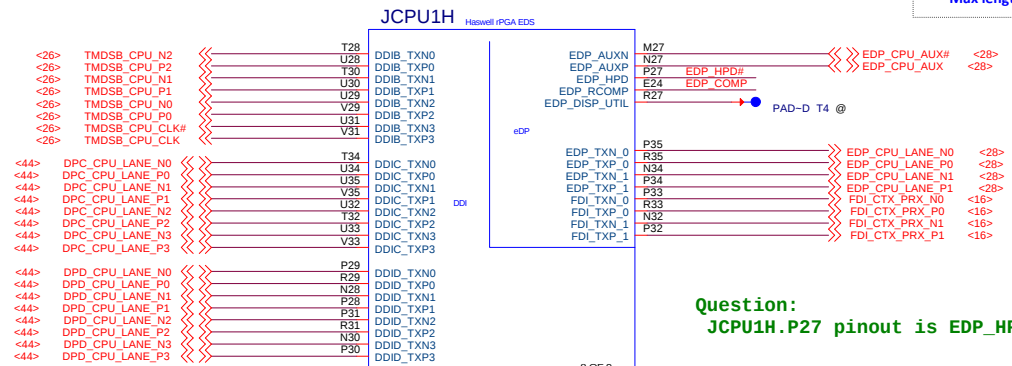


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CONN@

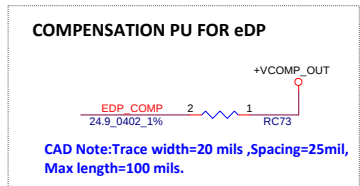
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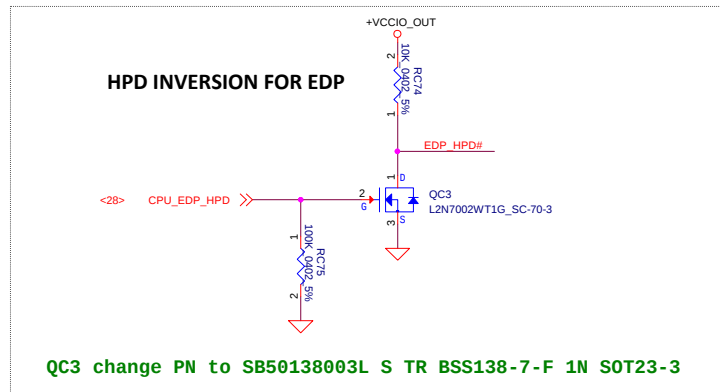
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LOTES_AZIF0012-P002B_HASWELL
CONN@



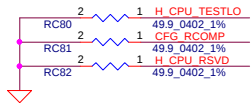
Question:
JCPU1H.P27 pinout is EDP_HPDI. is it high active when Plug in eDP device?



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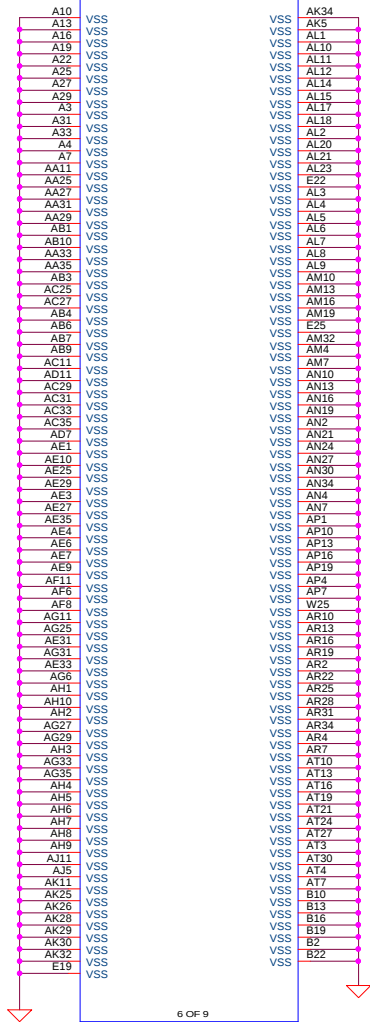
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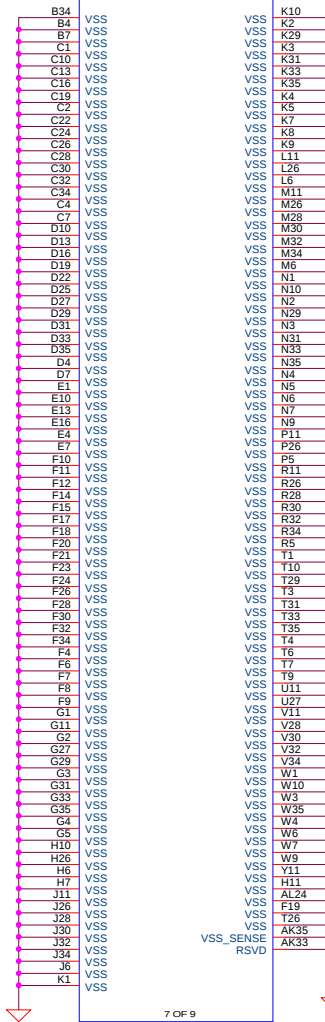
JCPU1F

Haswell iPGA EDS

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CONN@

JCPU1G

Haswell iPGA EDS

VSS_SENSE
RSVD
PAD-D T56@ <11>7 OF 9
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CONN@

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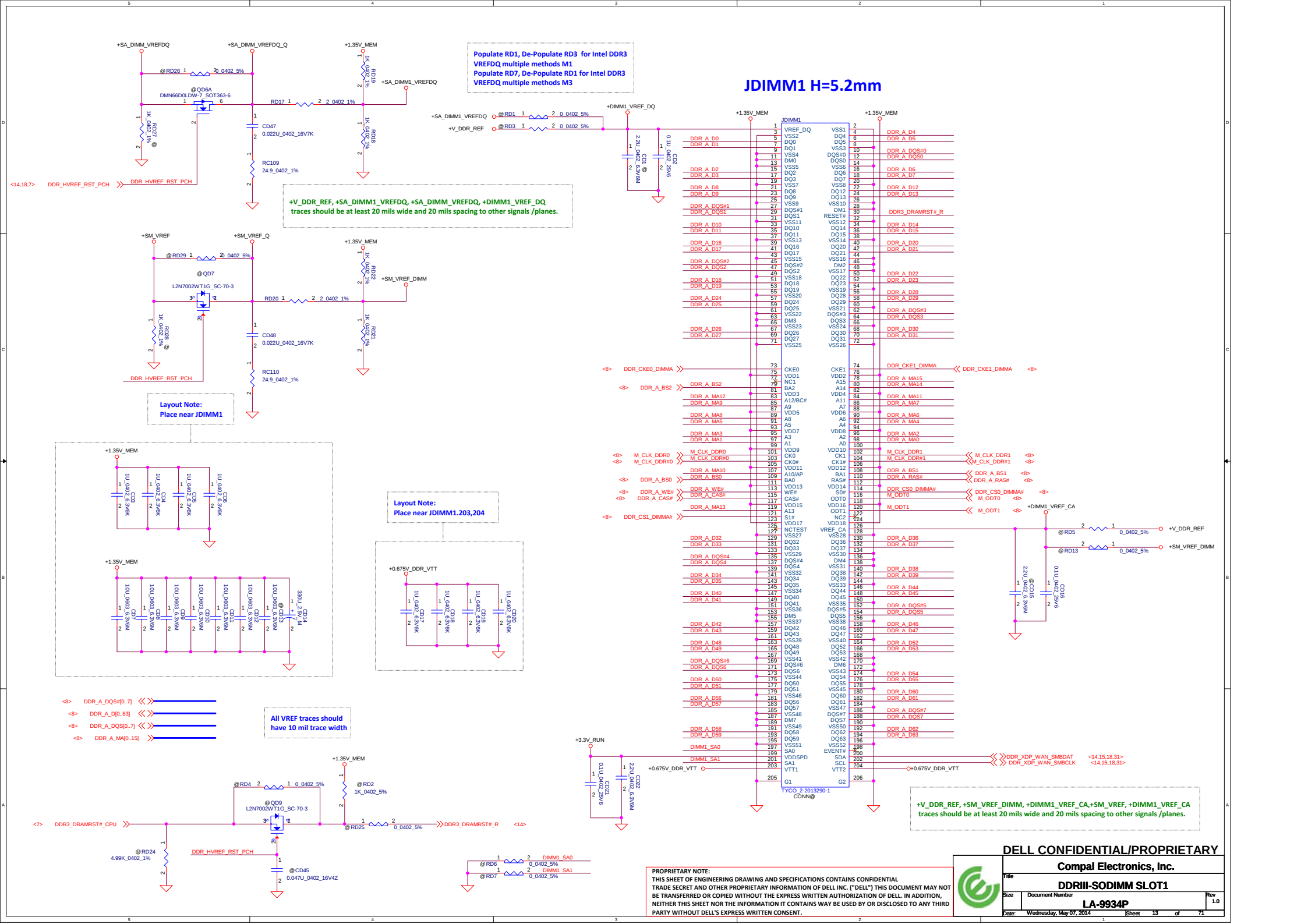


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CPU (7/7)

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Populate RD1, De-Populate RD3 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

JDIMM1 H=5.2mm

+V_DDR_REF, +SA_DIMM1_VREFDQ, +SA_DIMM_VREFDQ, +DIMM1_VREF_DQ traces should be at least 20 mils wide and 20 mils spacing to other signals /planes.

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

All VREF traces should have 10 mil trace width

+V_DDR_REF, +SM_VREF_DIMM, +DIMM1_VREF_CA, +SM_VREF, +DIMM1_VREF_CA traces should be at least 20 mils wide and 20 mils spacing to other signals /planes.

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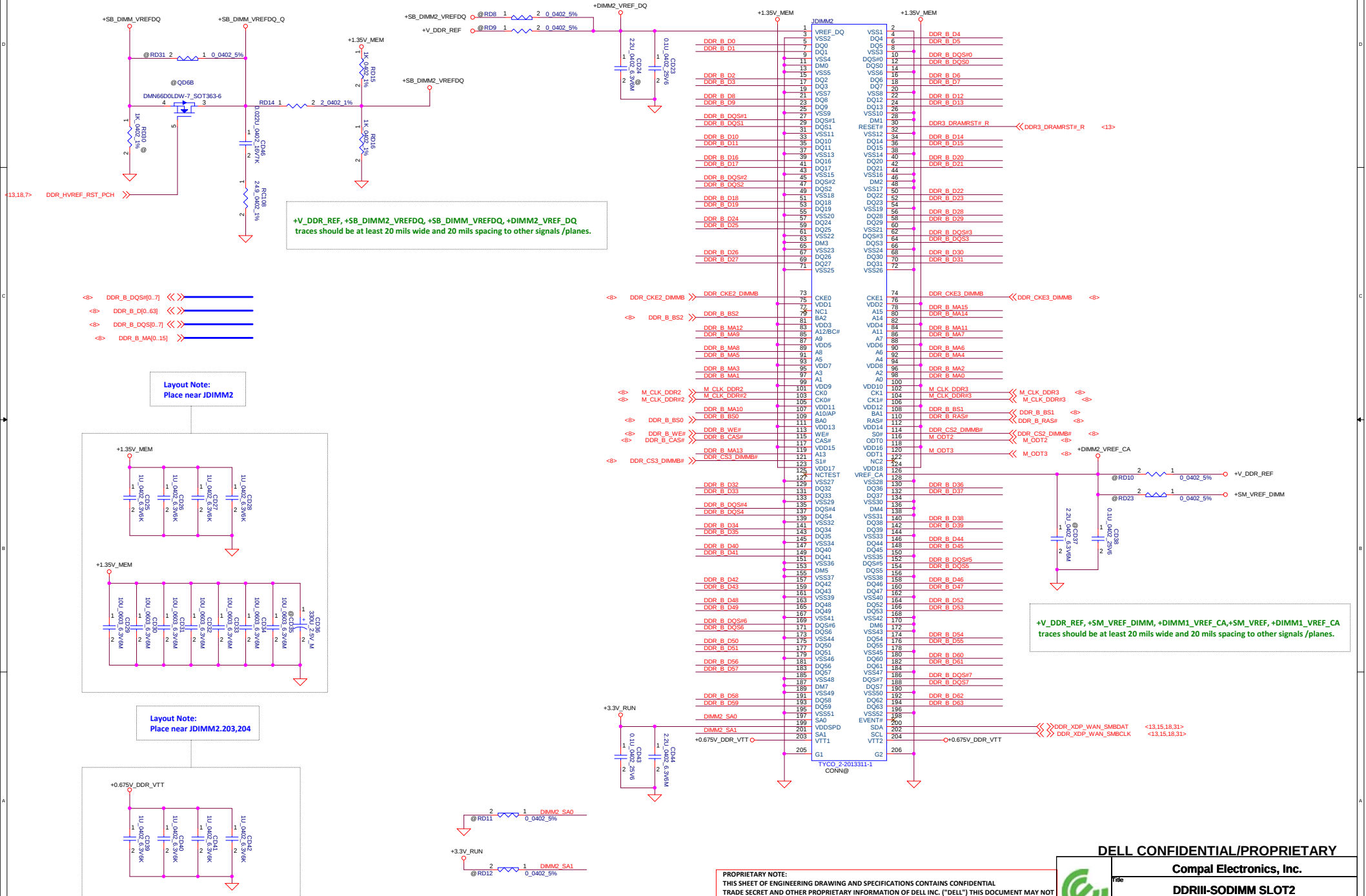
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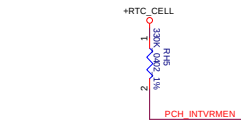
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JDIMM2 H=9.2mm

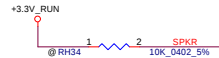


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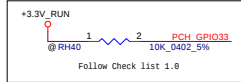




INTVSMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

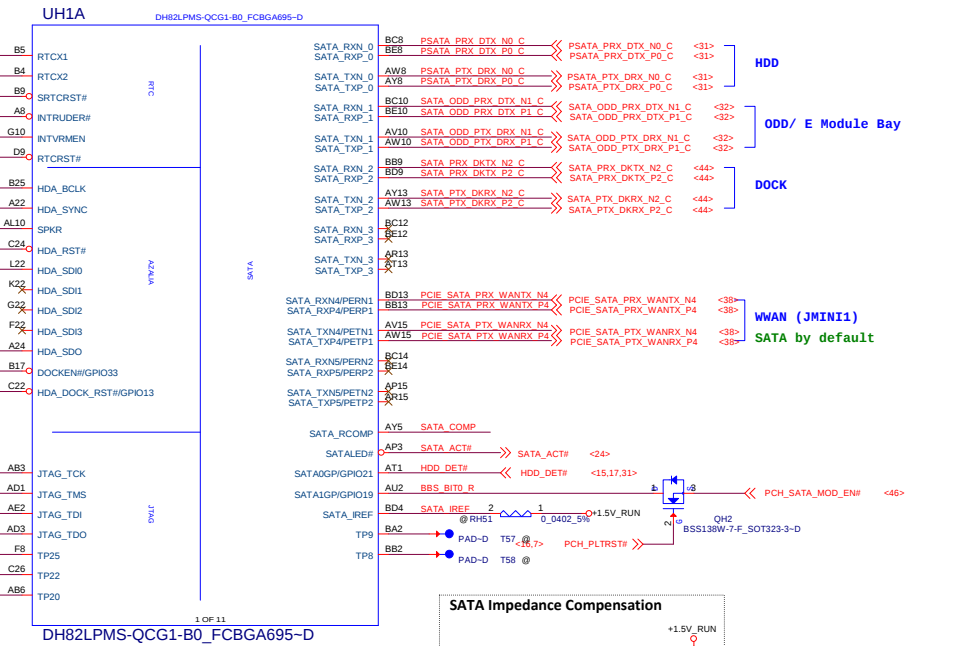
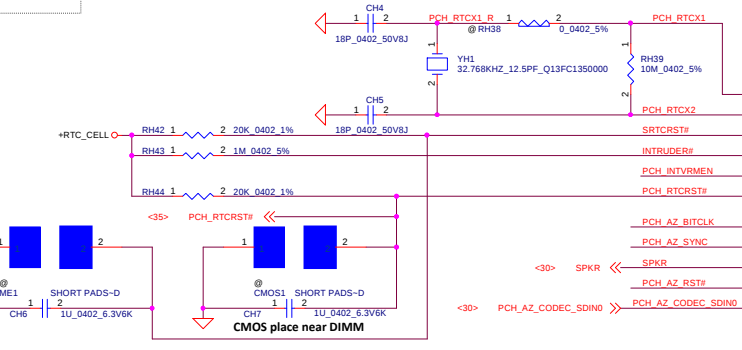
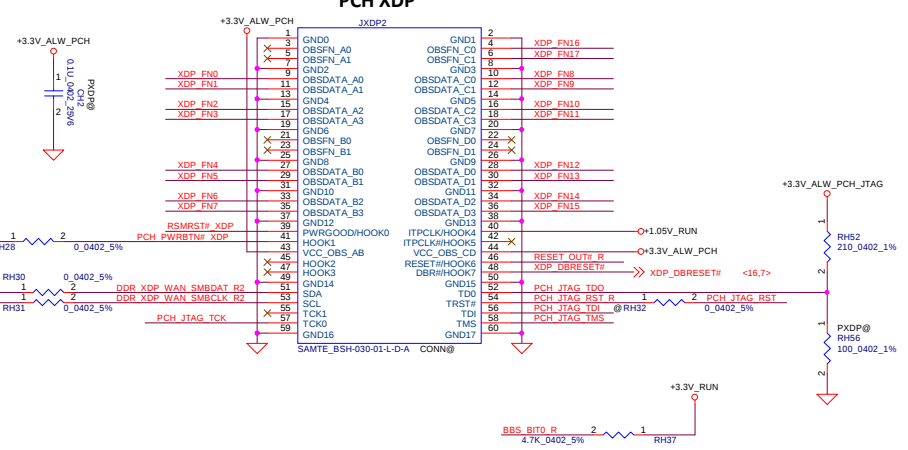
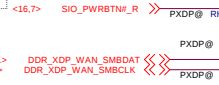
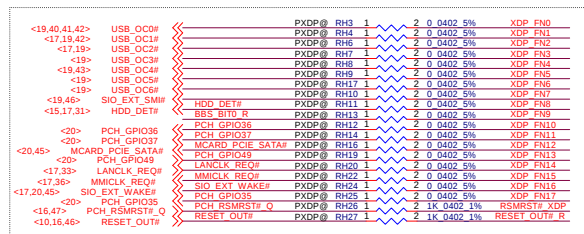
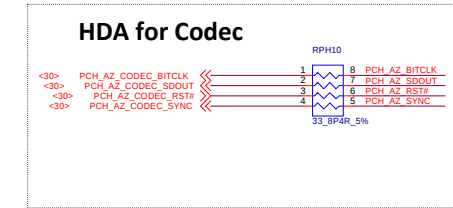


NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH

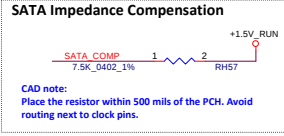


CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

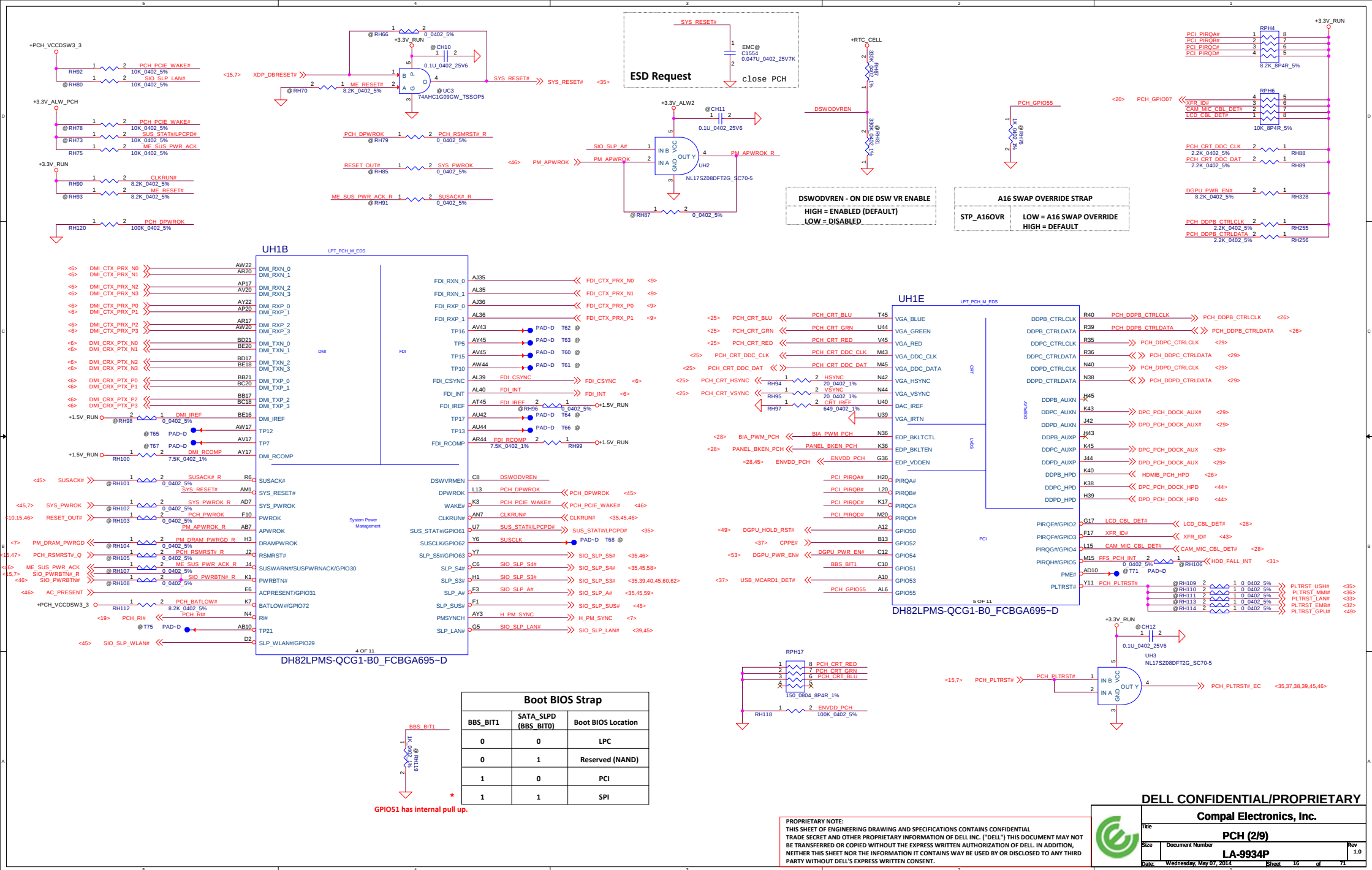


UH1 change PN to SA00005NE2L IC A31 DH82LPMS QCG1-B0 FCBGA 695P PCH



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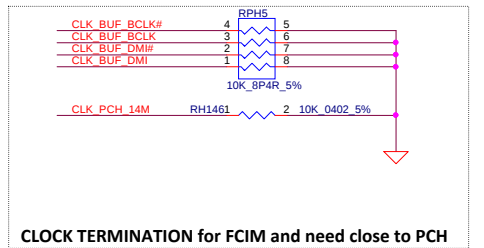
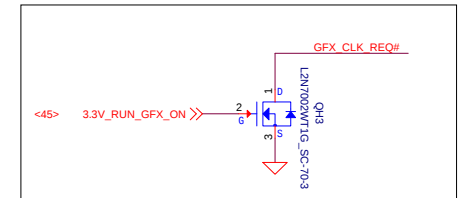
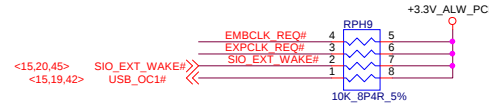
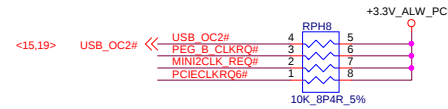
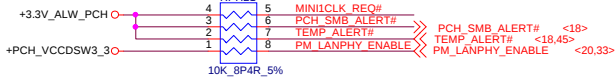
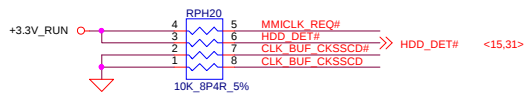
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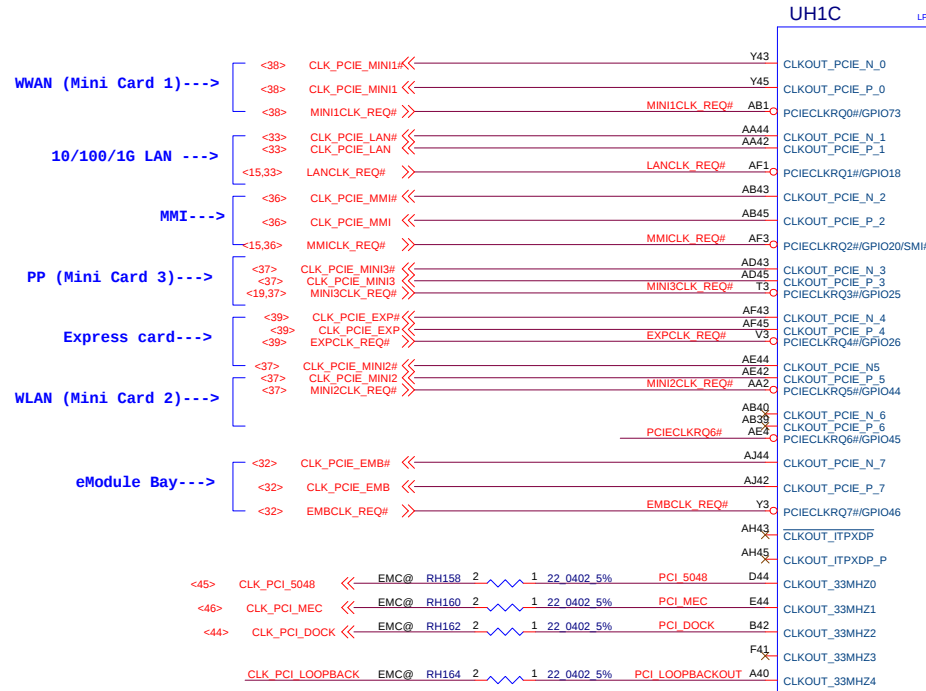
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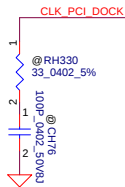
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CLOCK TERMINATION for FCIM and need close to PCH



PCIECLK REQ Pull UP Power Rail:
SUS Rail : 0 3 4 5 6 7
Core Rail: 1 2

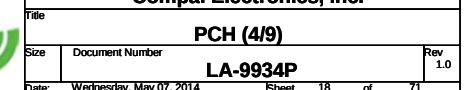
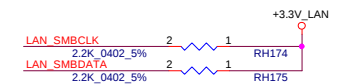


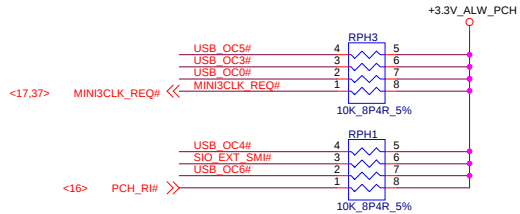
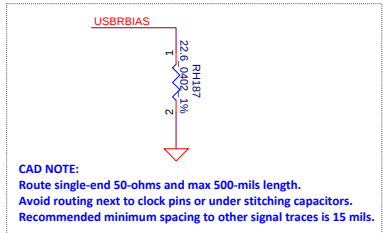
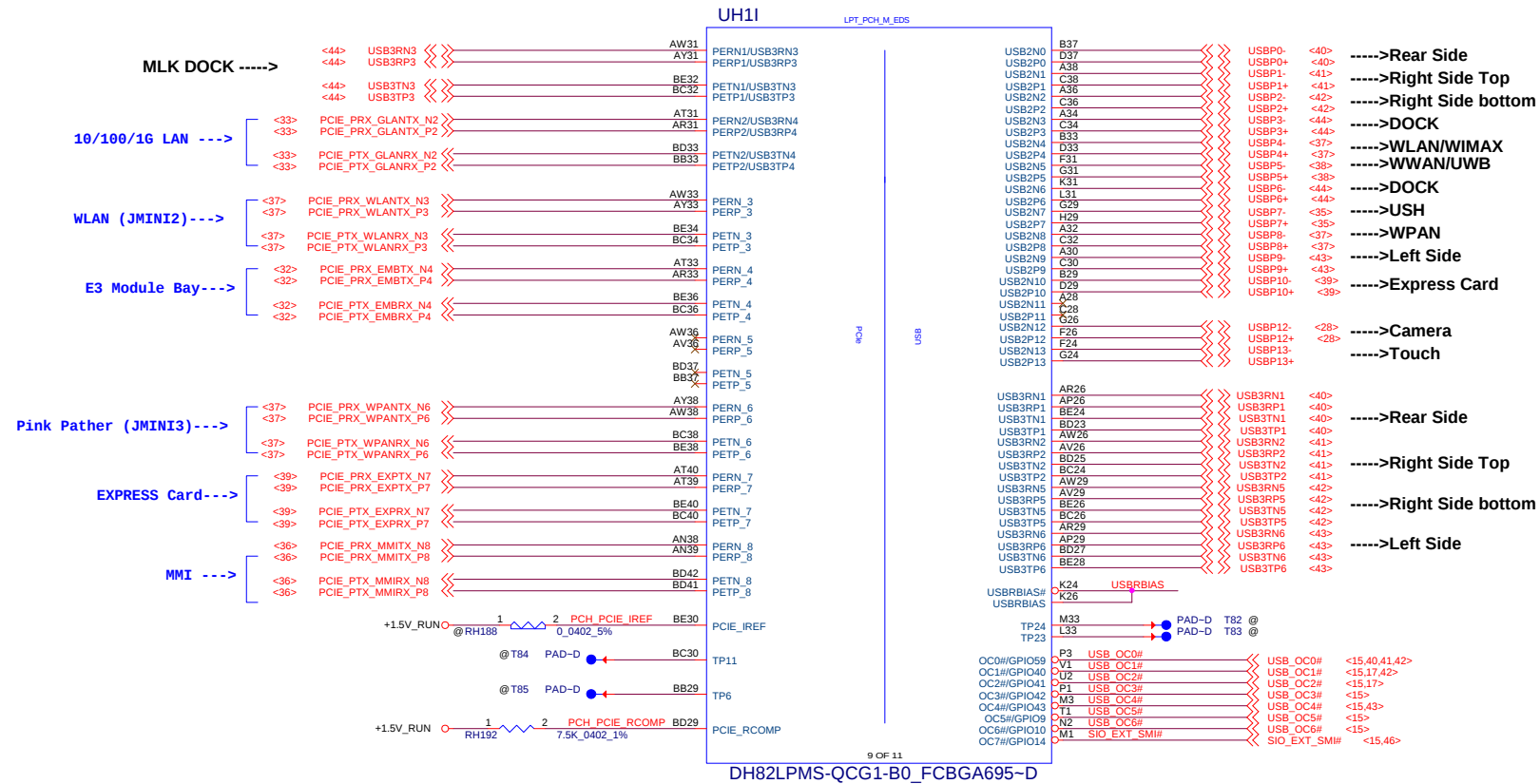
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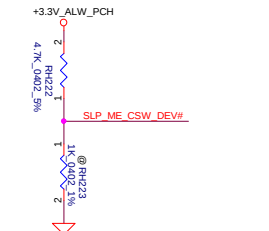
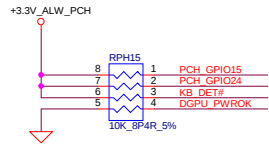
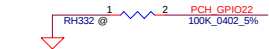
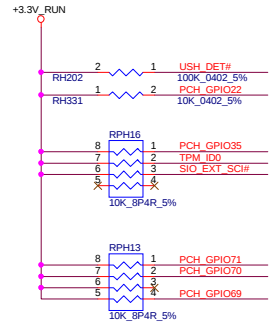
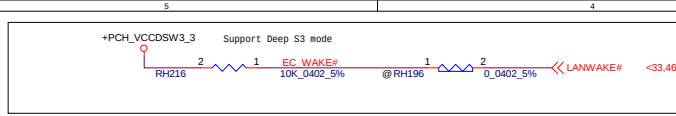
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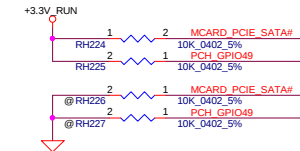
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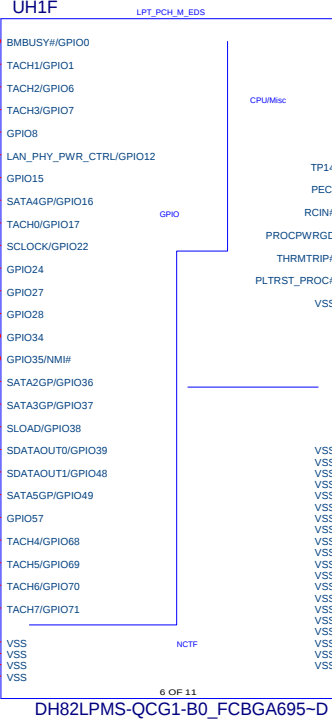
PLL ON DIE VR ENABLE
ENABLED - HIGH(DEFAULT)
DISABLED - LOW



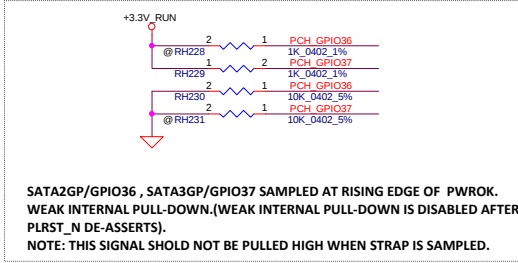
Config	GPIO16,49
USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01

*

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals					
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3		
				(00)	(00)							(00)	(00)						
				USB3 3	USB3 4							PCIE 1	PCIE 2						
				(01)	(01)							(01)	(01)						



CRB1.2 already change to GND directly at UH1.A44, B45, BD1 pins

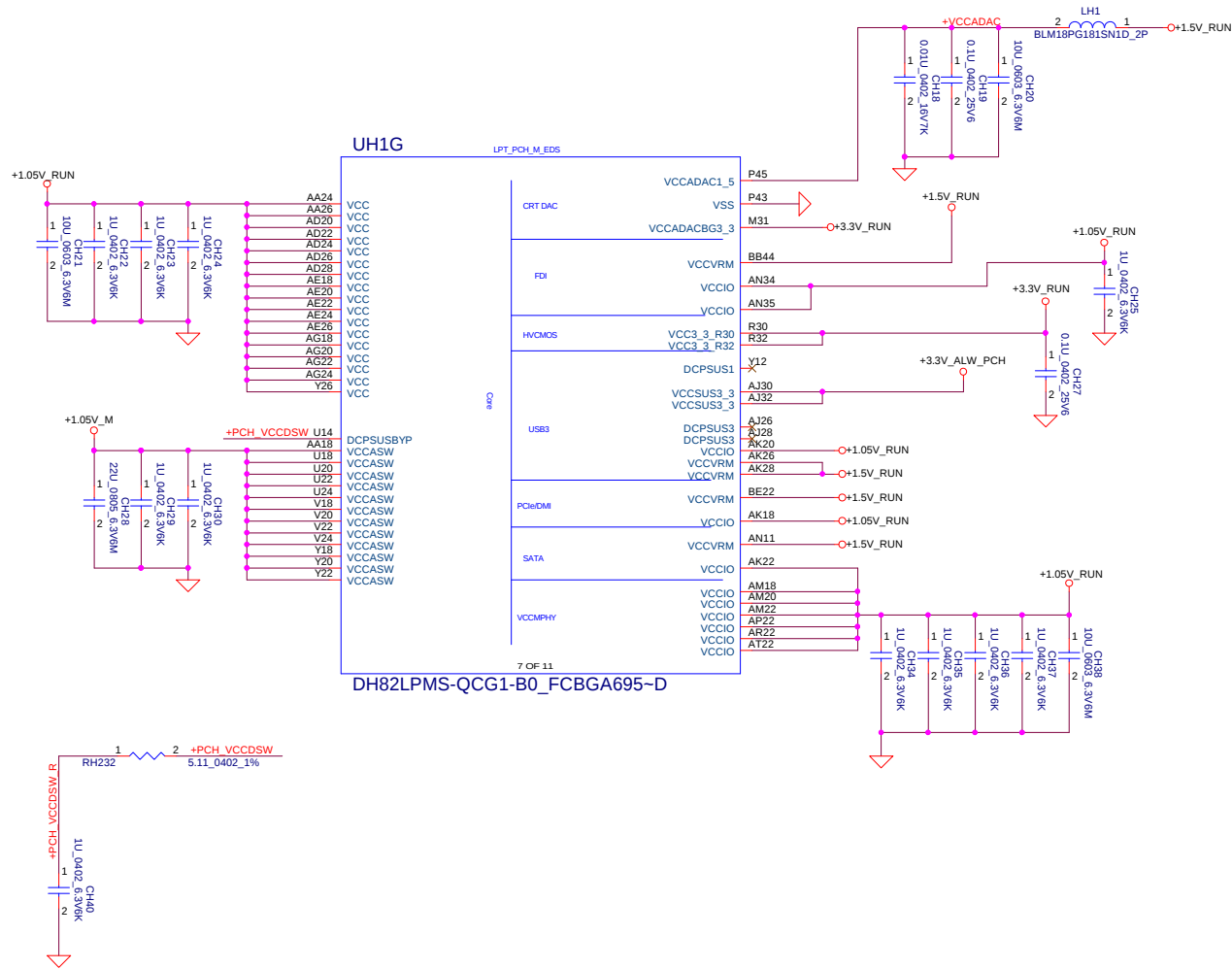


SATA2GP/GPIO36 , SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER PLRST_N DE-ASSERTS).
NOTE: THIS SIGNAL SHOULD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.

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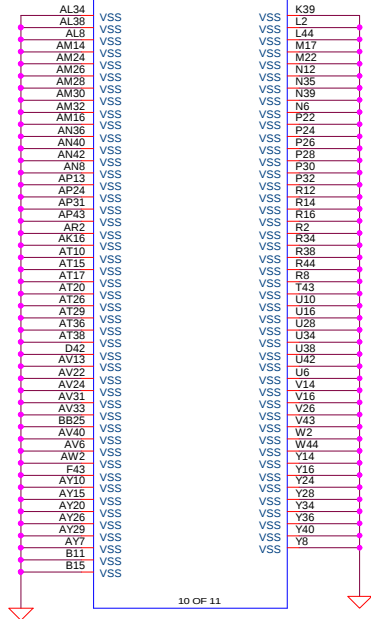
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.138 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.183 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

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UH1J

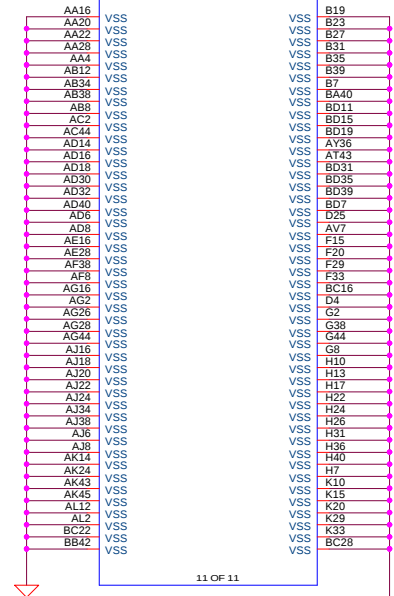
LPT_PCH_M_EDS



DH82LPMS-QCG1-B0_FCBGA695-D

UH1K

LPT_PCH_M_EDS



DH82LPMS-QCG1-B0_FCBGA695-D

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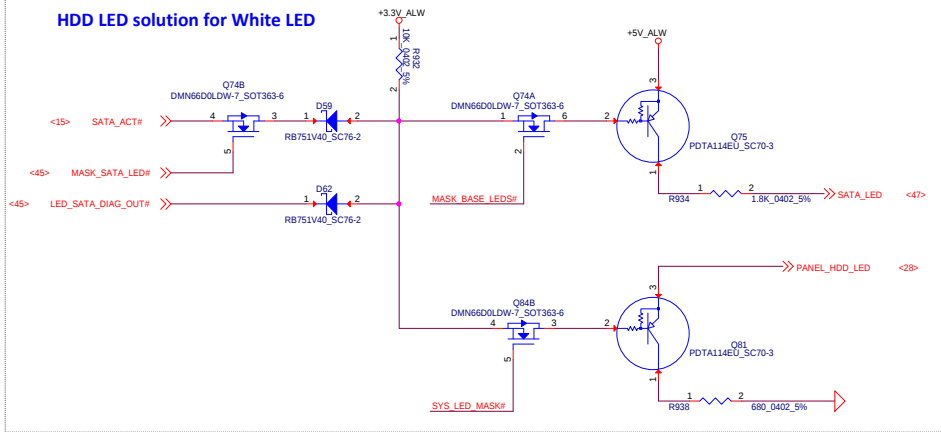


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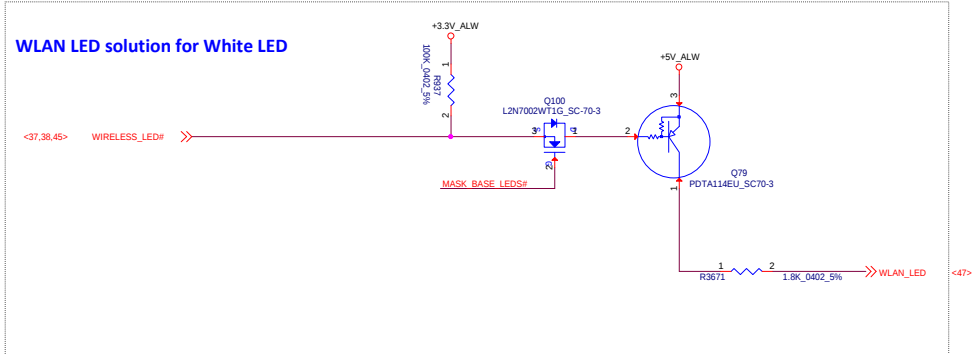
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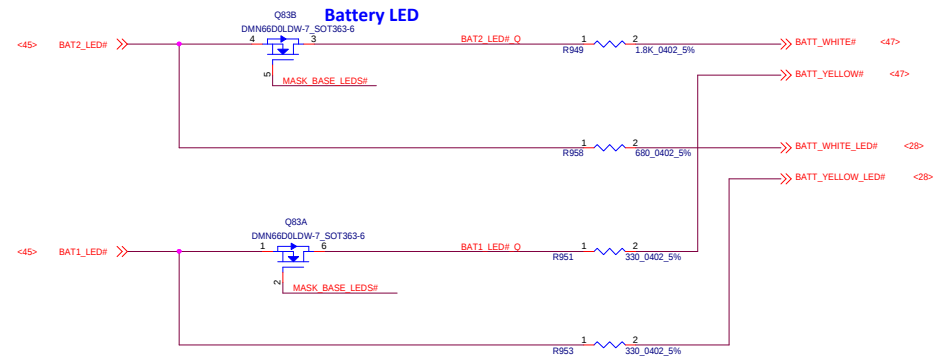
HDD LED solution for White LED



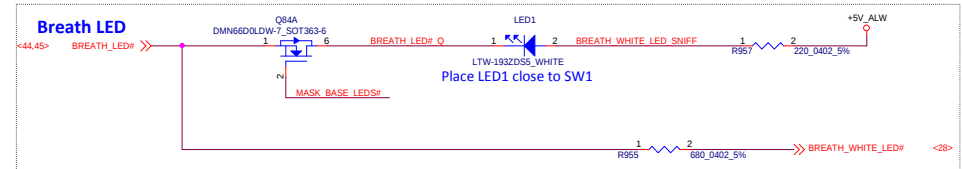
WLAN LED solution for White LED



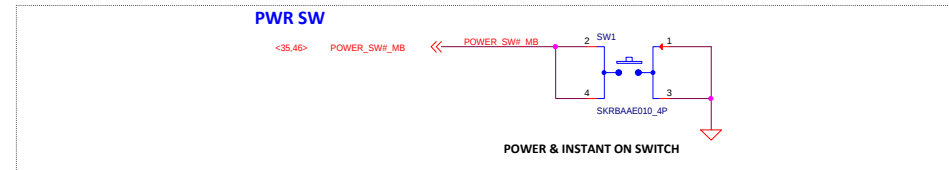
Battery LED



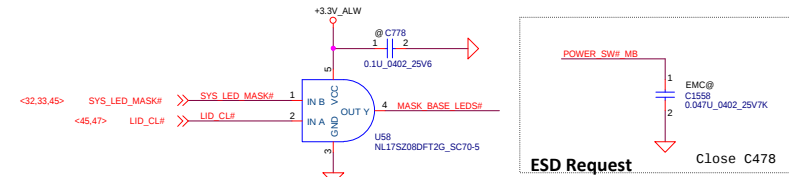
Breath LED



PWR SW

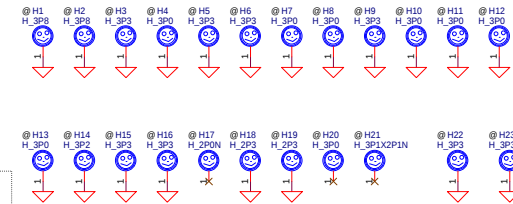


POWER & INSTANT ON SWITCH



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



Fiducial Mark



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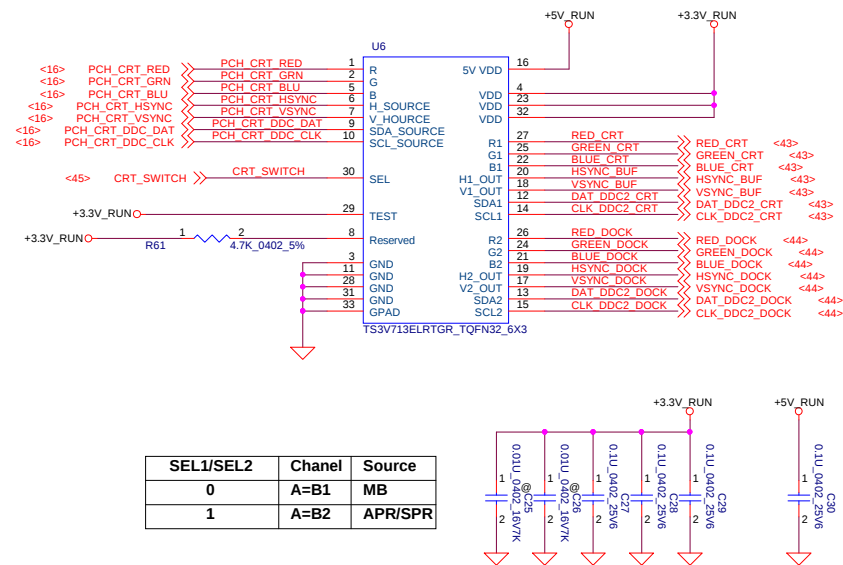
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PWR SW/LED/PAD/ME

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SW for MB/DOCK



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CRT SW

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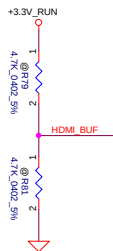
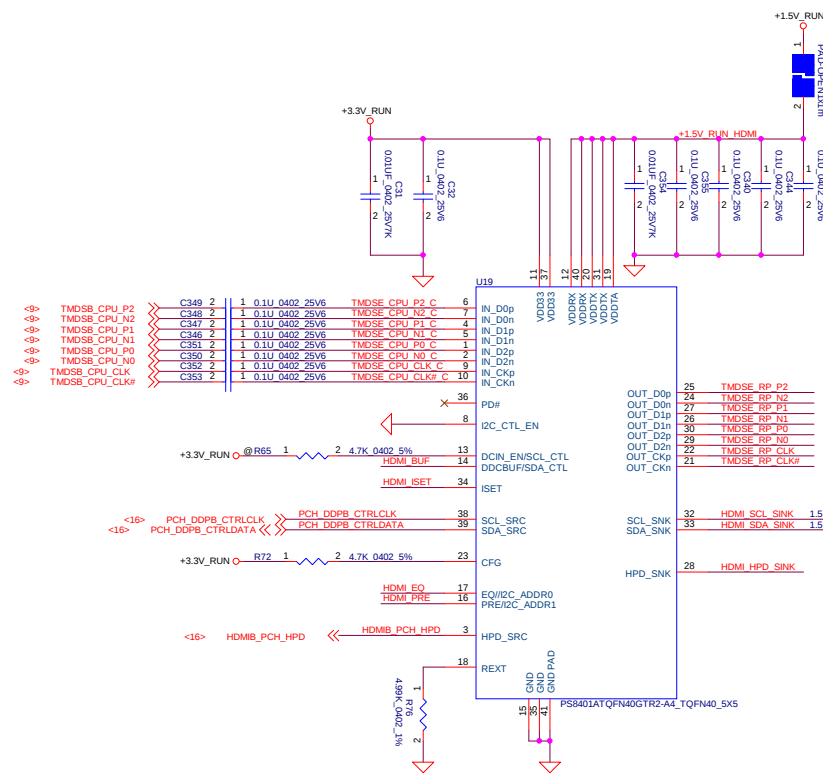
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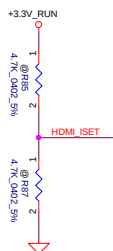
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Rev

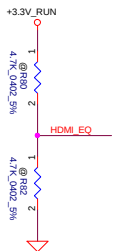
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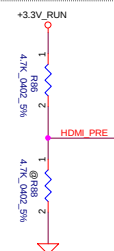
Enable active DDC buffer; Internal pull up at 150kΩ±20%, 3.3V I/O
 L: default, passive DDC pass-through
 H: active DDC buffer with default threshold
 M: active DDC buffer without internal pull up resistor



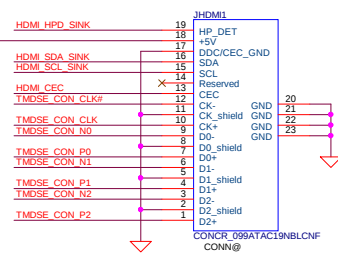
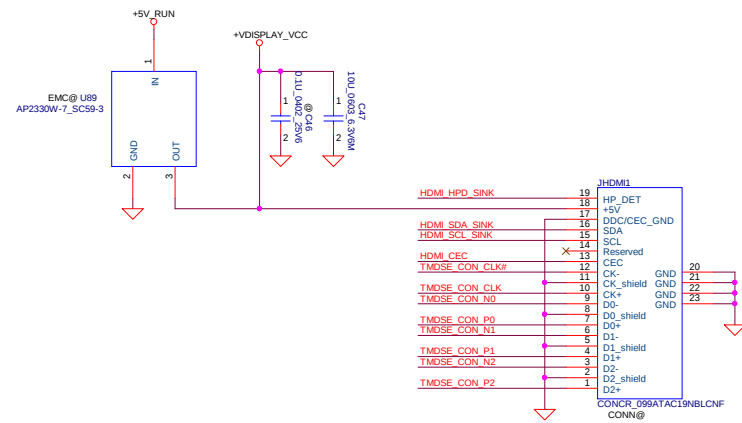
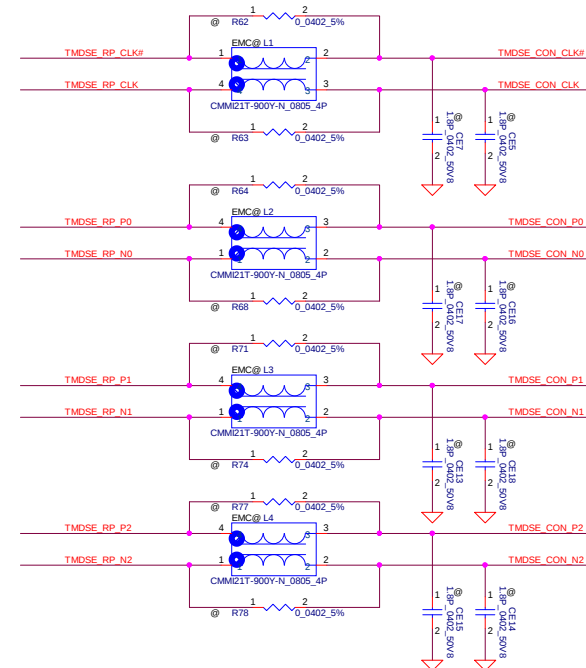
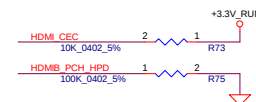
TMD5 output swing adjustment; Internal pull down at ~150kΩ, 3.3V I/O.
 L: default
 H: increase +13%
 M: reduce -13%



Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
 L: programmable EQ for channel loss up to 12.4dB
 H: programmable EQ for channel loss up to 4.3dB
 M: programmable EQ for channel loss up to 8.6dB



Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
 L: no pre-emphasis
 H: 1.6dB pre-emphasis
 M: 2.5dB pre-emphasis



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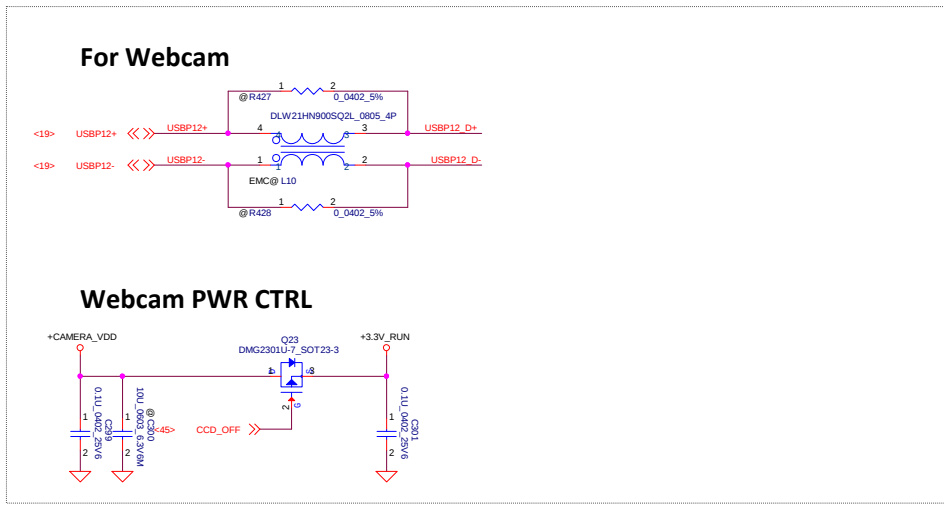
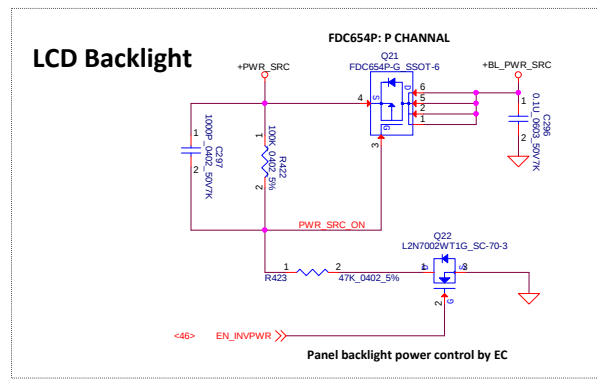
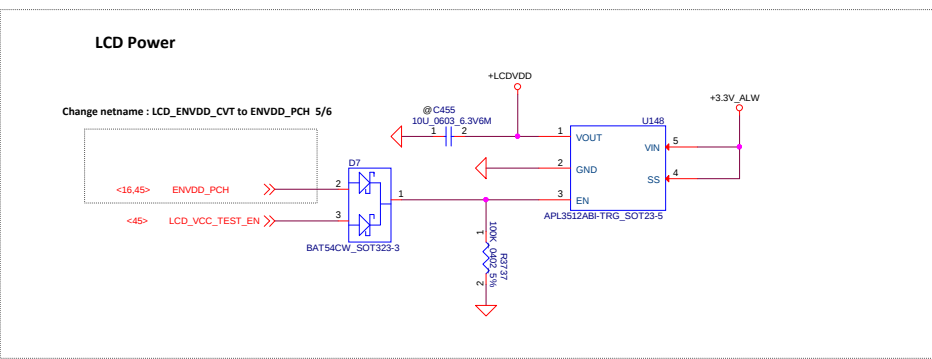
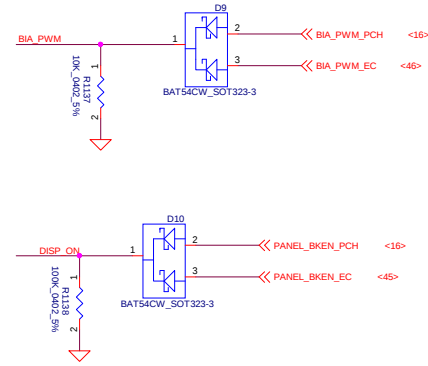
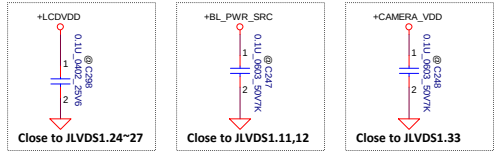
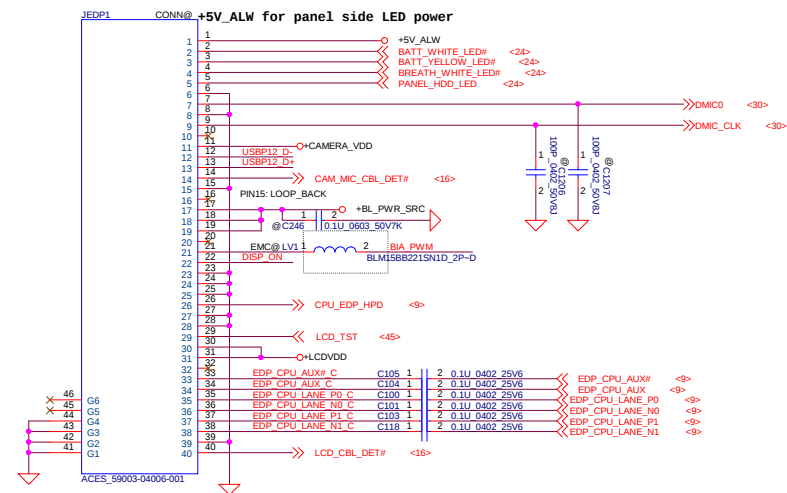
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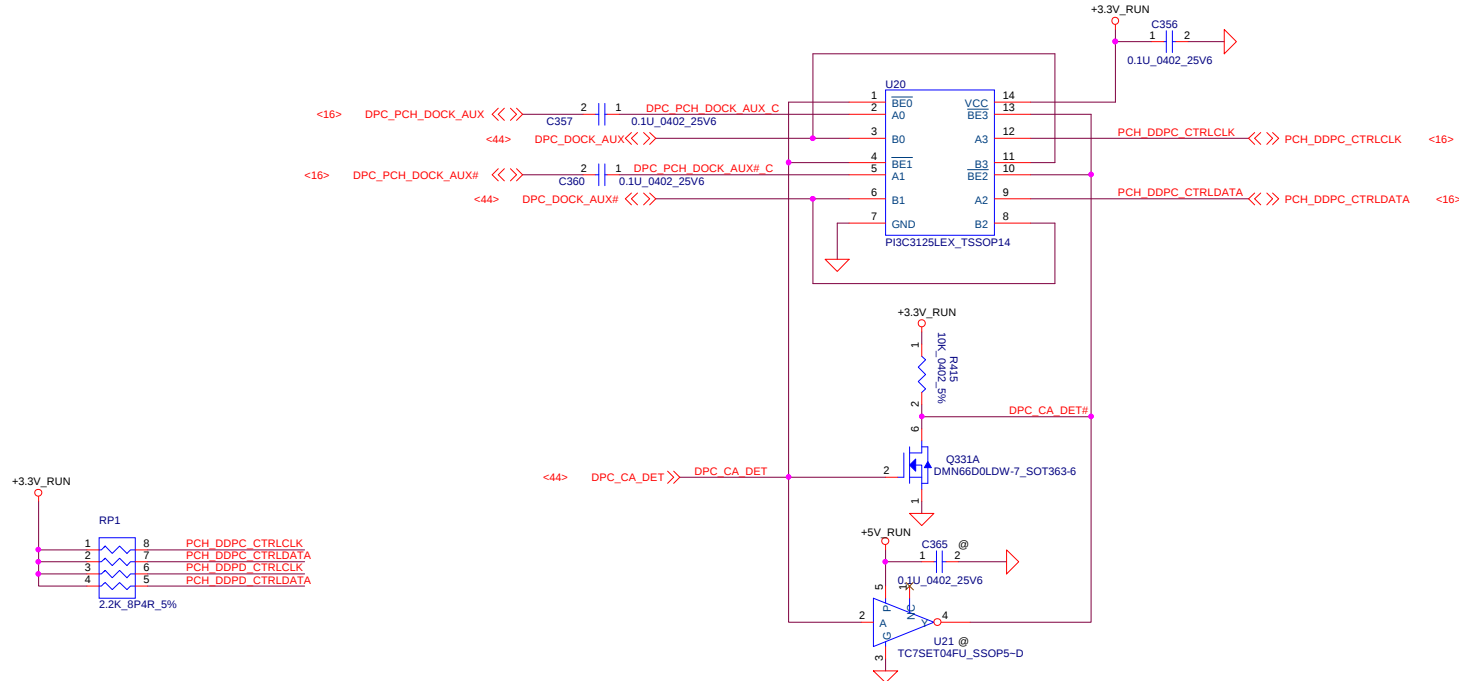
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Remove Touch Screen

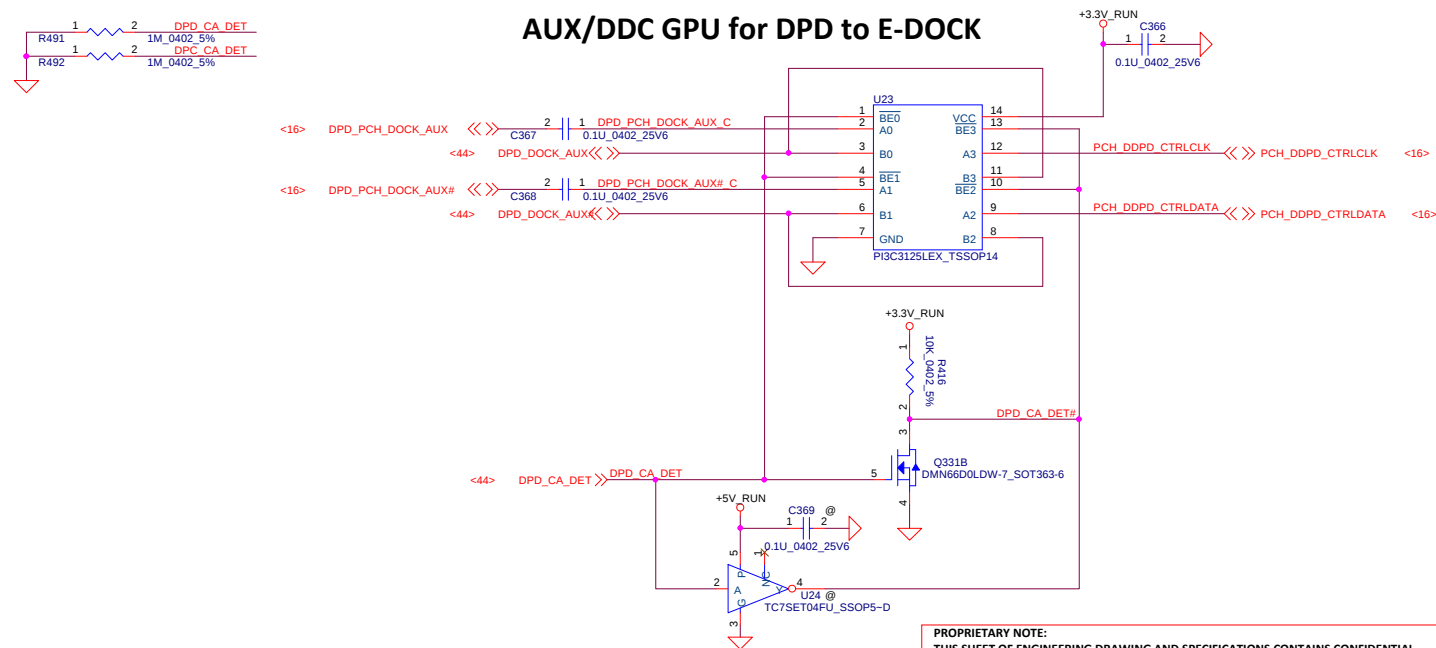
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AUX/DDC GPU for DPC to E-DOCK



Vinafix

AUX/DDC GPU for DPD to E-DOCK



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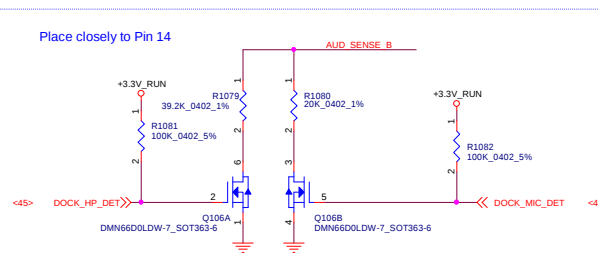
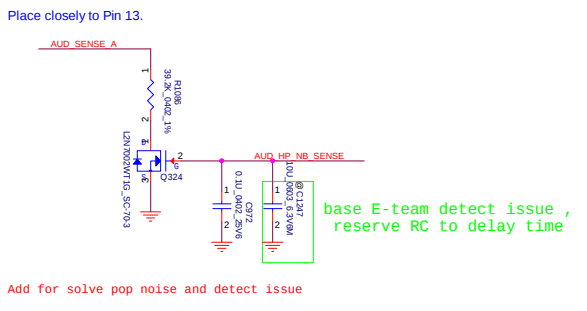
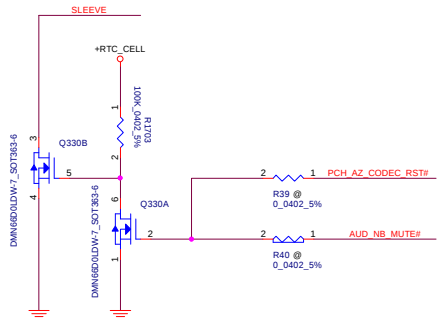
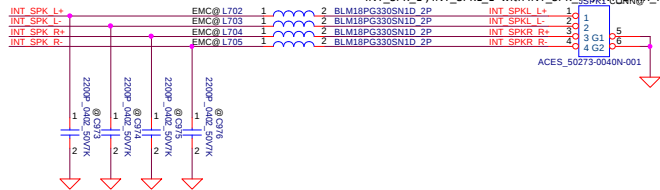
DP SW

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Internal Speakers Header

INT_SPK_L+, INT_SPKL_L+ :40 mils trace, keep 10mils spacing
 INT_SPK_R+, INT_SPKR_R+ :40 mils trace, keep 10mils spacing
 INT_SPK_L-, INT_SPKL_L- :40 mils trace, keep 10mils spacing
 INT_SPK_R-, INT_SPKR_R- :40 mils trace, keep 10mils spacing
 INT_SPK_L-, INT_SPKL_L- with INT_SPK_R+, INT_SPKR_R+ keep 20mils spacing

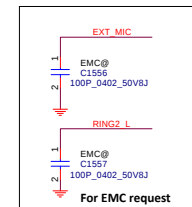
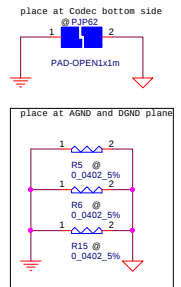
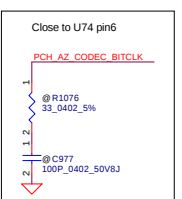
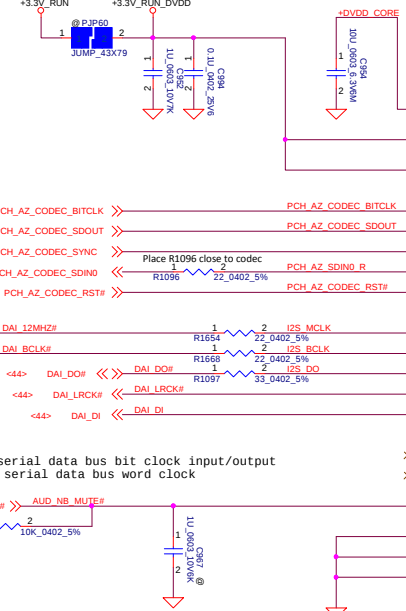


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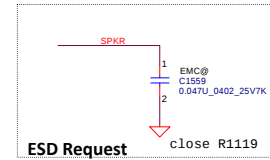
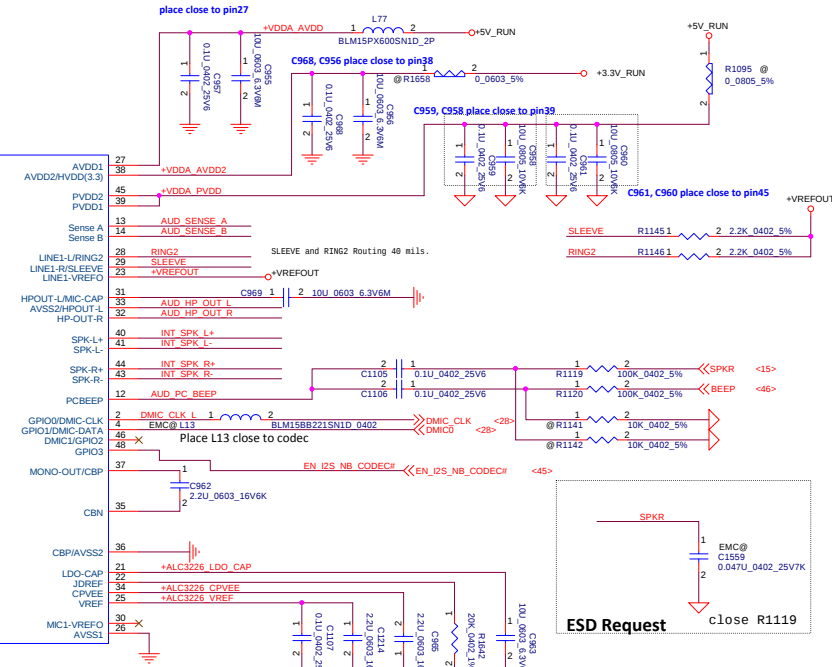
Keep PVDD supply and speaker traces routed on the DGND plane.
 Keep away from AGND and other analog signals

Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

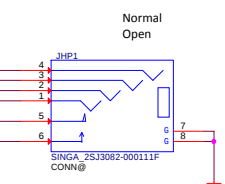
PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK



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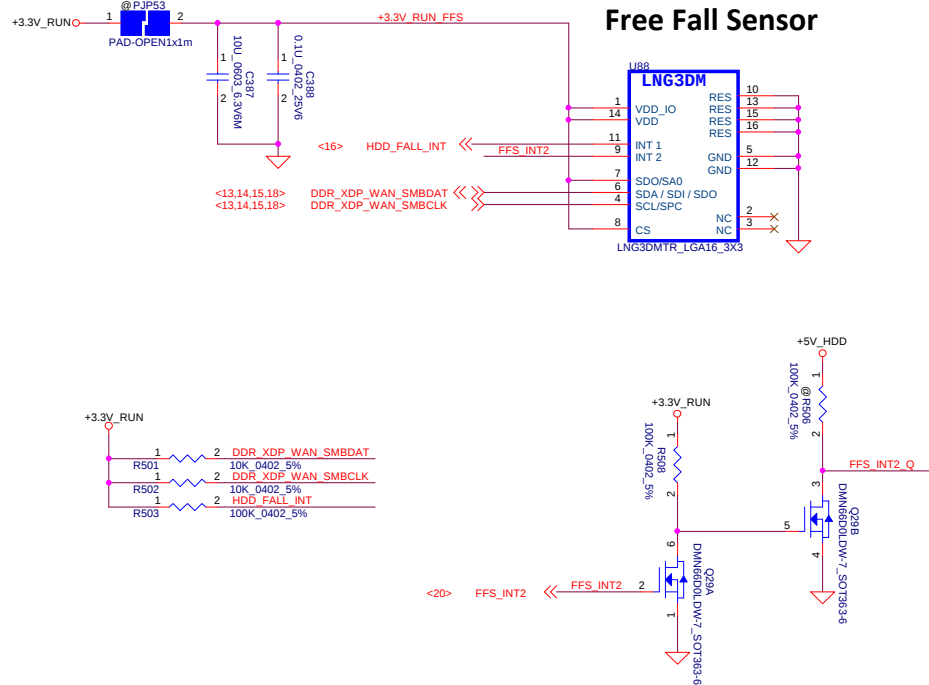


Combo Jack

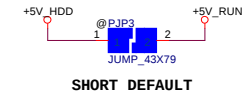


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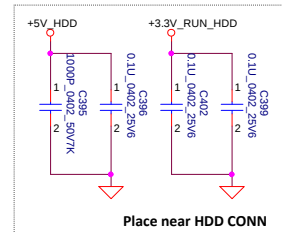
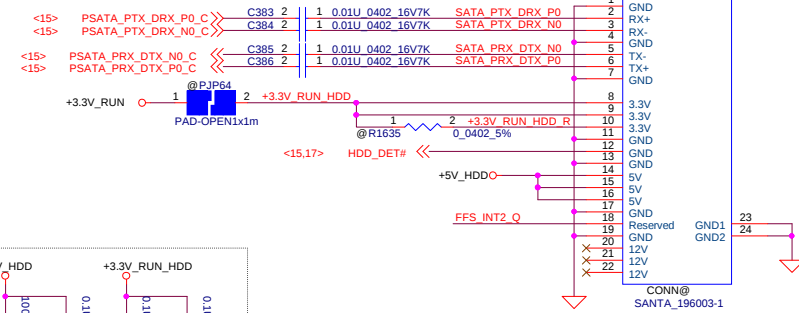
Compal Electronics, Inc.			
Title	Codec		
Size	Document Number	LA-9934P	Rev 1.0
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HDD PWR



HDD CONN



Main SATA +5V Default

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HDD		
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+5V_MOD/+5V_RUN source

MOD MD

+3.3V_ALW_PCH

+3.3V_ALW

Place near ODD CONN

ODD CONN

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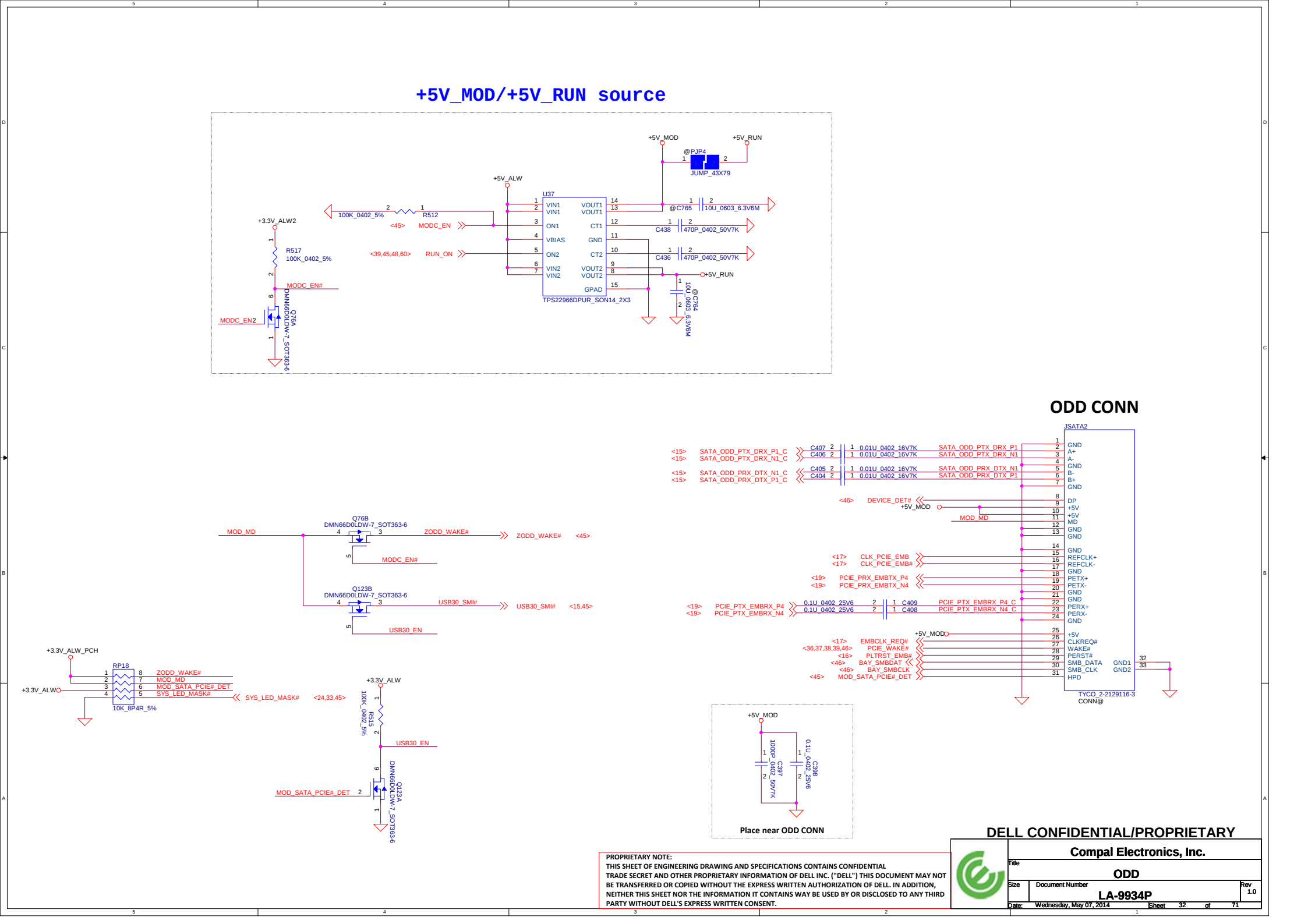
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+5V_MOD/+5V_RUN source

MOD MD

MOD SATA PCIE# DET

ODD CONN

Place near ODD CONN

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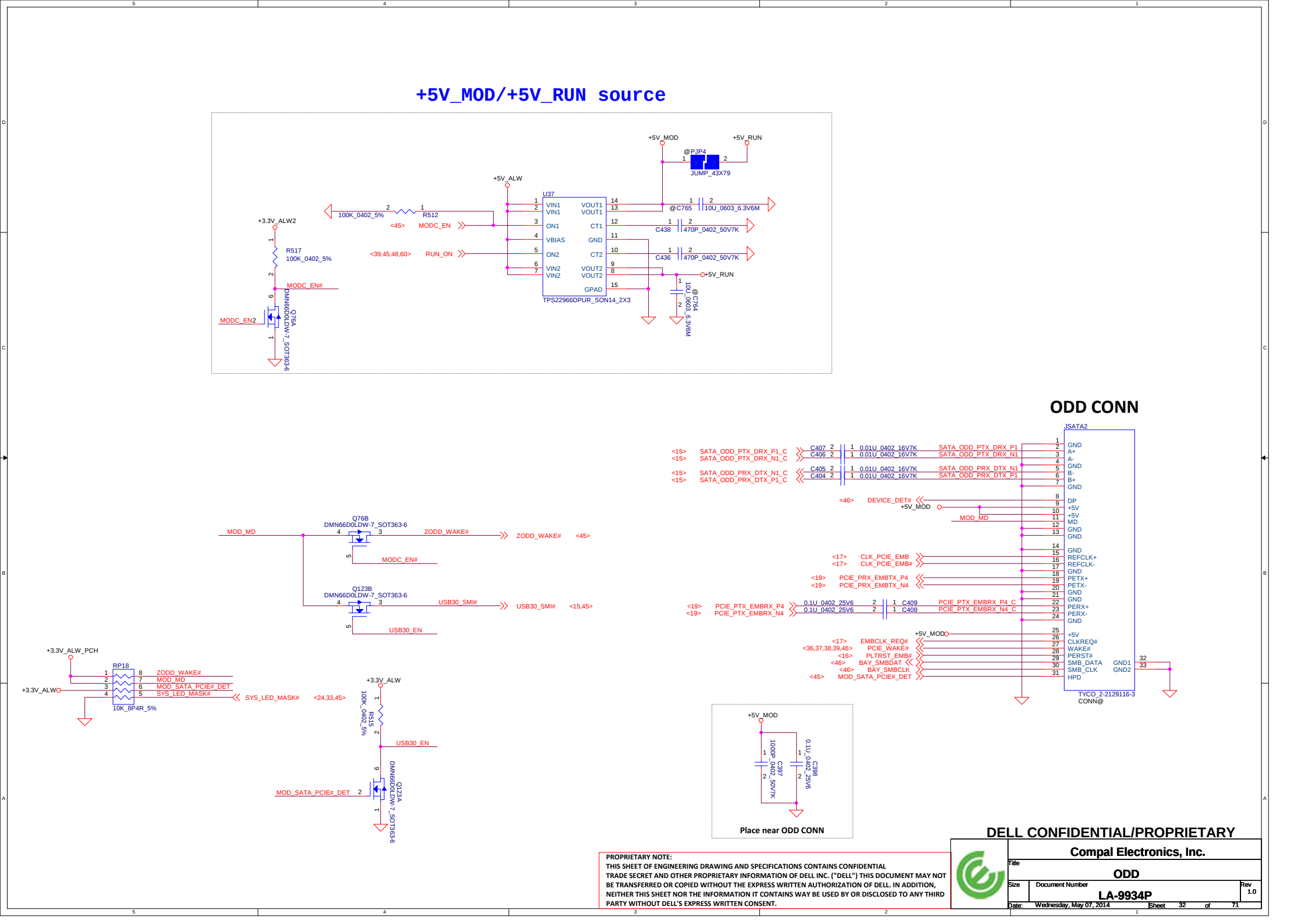
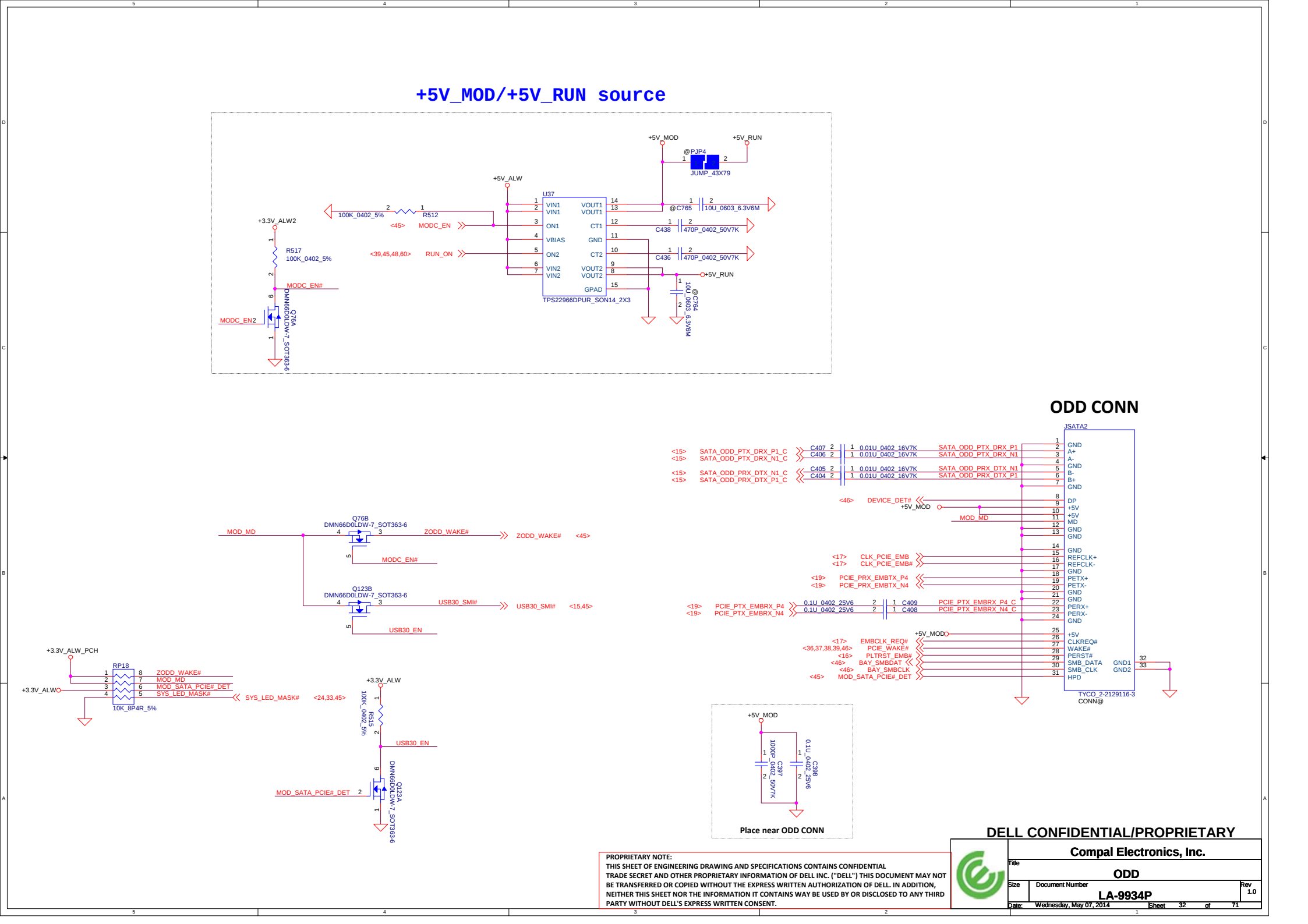
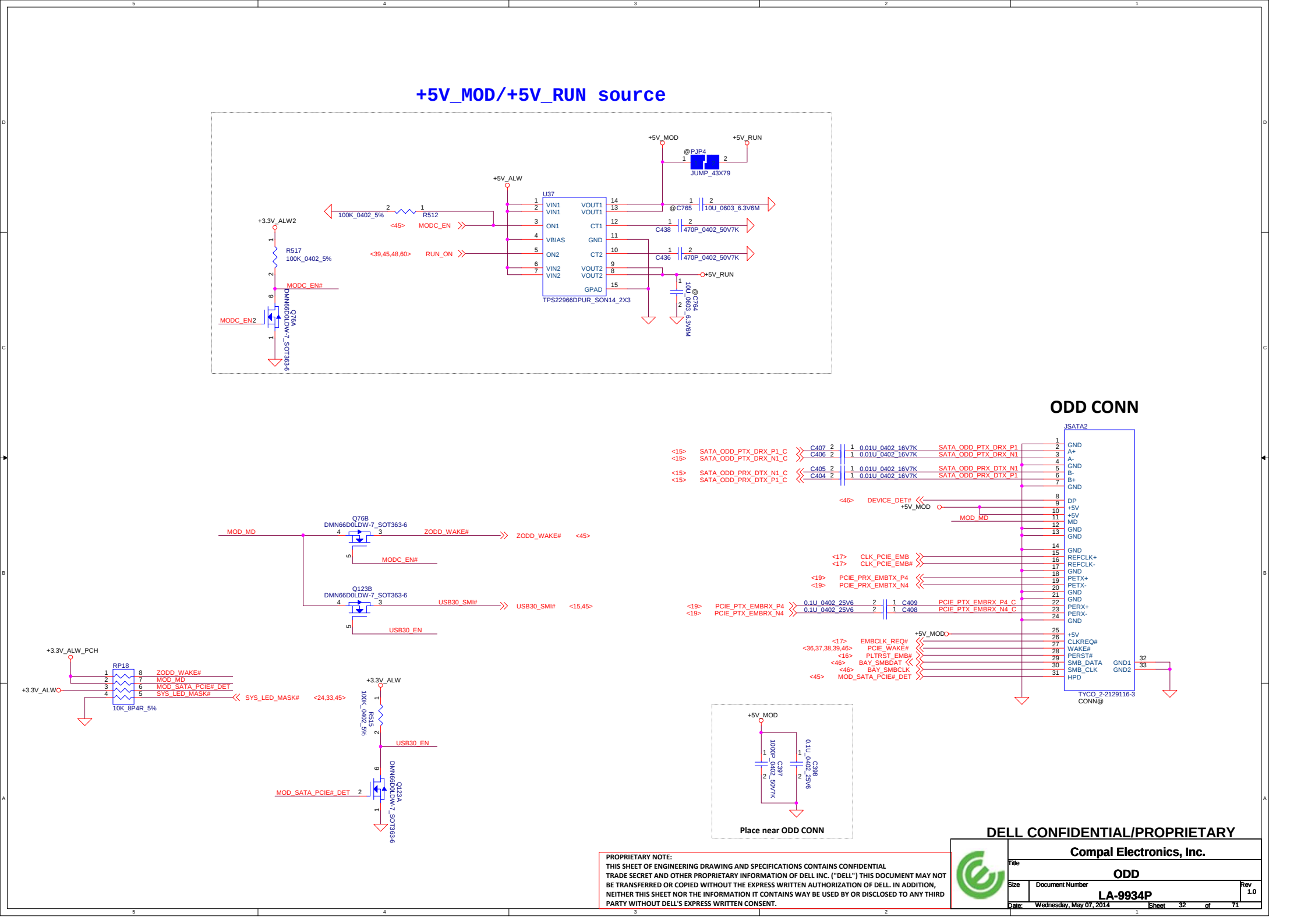
ODD

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+5V_MOD/+5V_RUN source

MOD MD

MOD SATA PCIE# DET

ODD CONN

Place near ODD CONN

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+5V_MOD/+5V_RUN source

MOD MD

+3.3V_ALW_PCH

Place near ODD CONN

ODD CONN

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+5V_MOD/+5V_RUN source

MOD MD

+3.3V_ALW_PCH

MOD SATA PCIE# DET

USB30 EN

JSATA2

Signal	Pin	Component	Value	Notes
SATA_ODD_PT_X_DRX_P1_C	C407	Resistor	0.01U 0402 16V7K	<15>
SATA_ODD_PT_X_DRX_N1_C	C406	Resistor	0.01U 0402 16V7K	<15>
SATA_ODD_PRX_DTX_N1_C	C405	Resistor	0.01U 0402 16V7K	<15>
SATA_ODD_PRX_DTX_P1_C	C404	Resistor	0.01U 0402 16V7K	<15>
PCIE_PT_X_EMBRX_P4_C	C409	Resistor	0.1U 0402 25V6	<19>
PCIE_PT_X_EMBRX_N4_C	C408	Resistor	0.1U 0402 25V6	<19>
EMBCLK_REQ#	C398	Capacitor	0.1U 0402 25V6	<17>
CLK_PCIE_EMB	C397	Capacitor	0.1U 0402 25V6	<17>
PLTRSTY_EMB#	C396	Capacitor	0.1U 0402 25V6	<16>
BAY_SMBCLK	C395	Capacitor	0.1U 0402 25V6	<45>
BAY_SMBCLK	C394	Capacitor	0.1U 0402 25V6	<45>

Place near ODD CONN

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ODD

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[illegible]

+5V_MOD/+5V_RUN source

MOD MD

+3.3V_ALW_PCH

USB30 EN

Place near ODD CONN

ODD CONN

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+5V_MOD/+5V_RUN source

MOD MD

USB30 EN

MOD SATA PCIE# DET

Place near ODD CONN

ODD CONN

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ODD

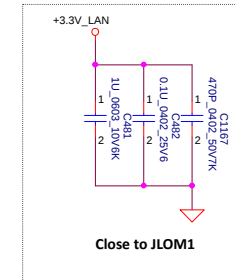
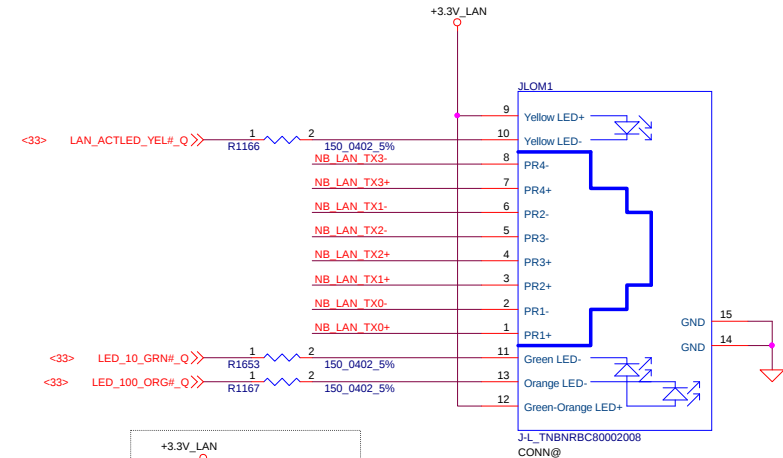
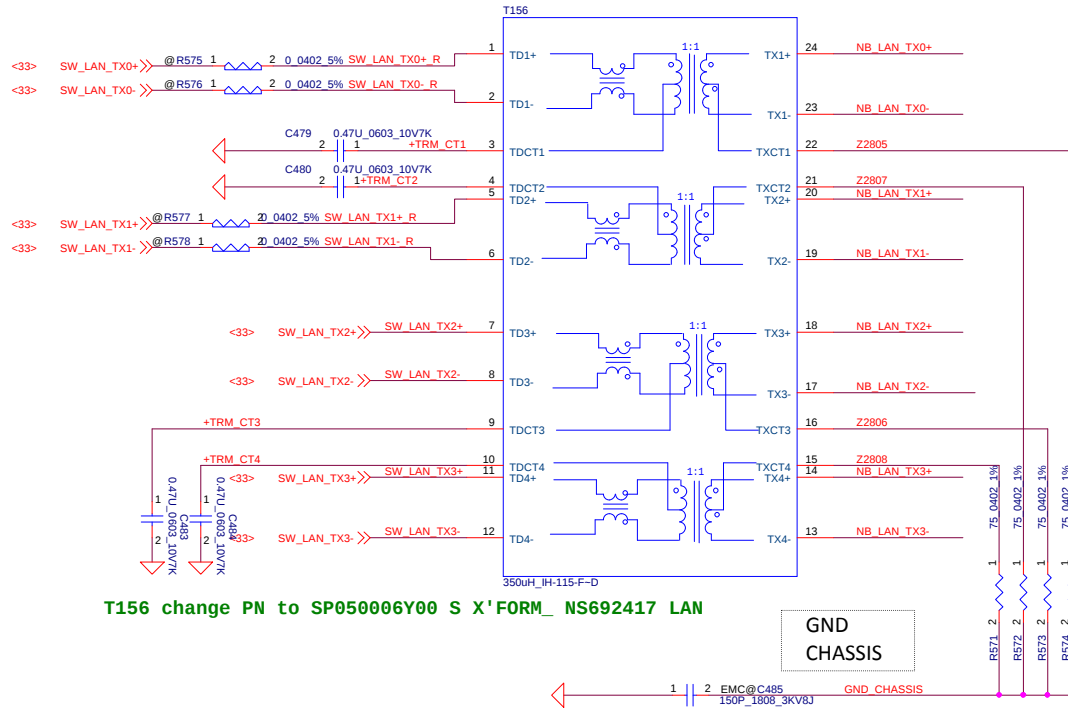
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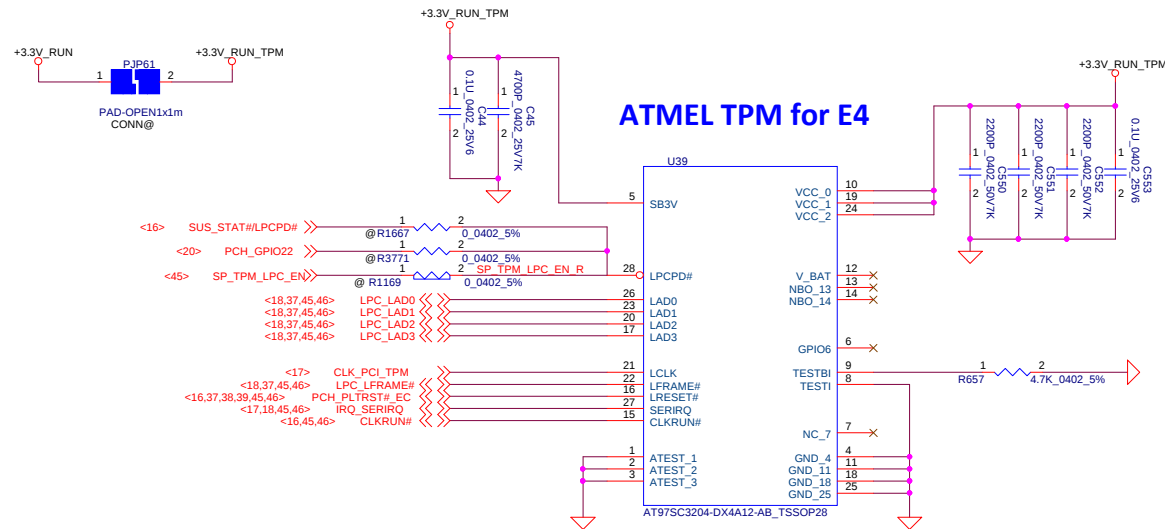
SW_LAN_TX0+ R 1 2 SW_LAN_TX0+ R
@C500 1 2 100P_0402_50V8J
SW_LAN_TX1+ R 1 2 SW_LAN_TX1+ R
@C501 1 2 100P_0402_50V8J



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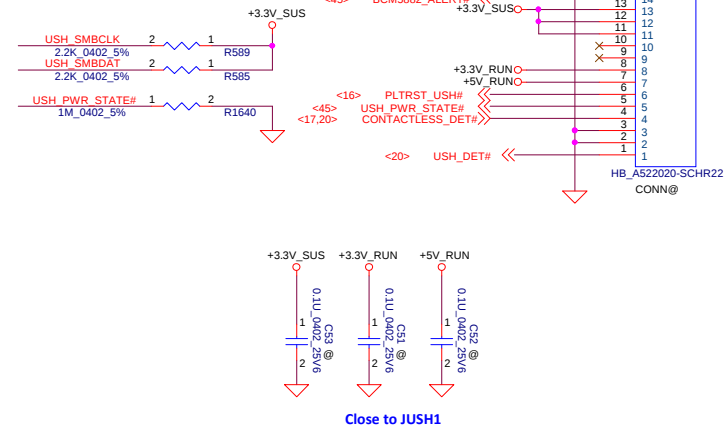
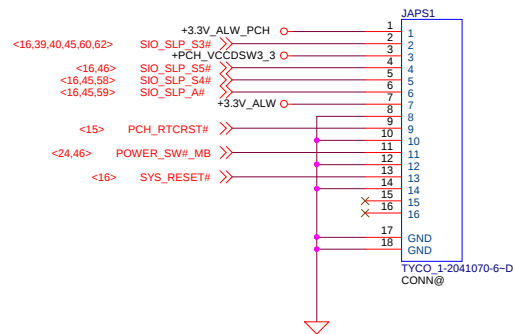
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	Title			
	RJ45 Conn			
	Size	Document Number		Rev
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JUSH1 pin reverse between IVY and HSW to support E4 13 USH board

USH CONN

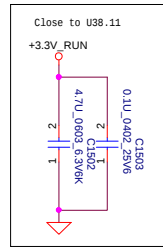
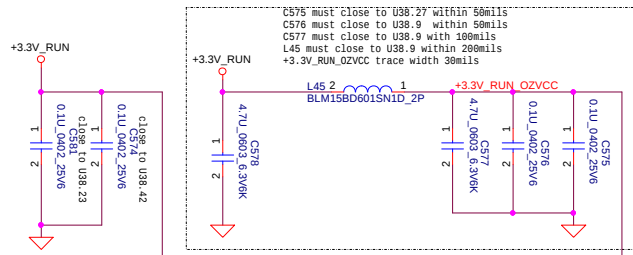


Close to JUSH1

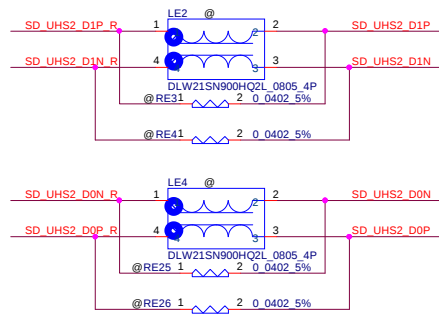
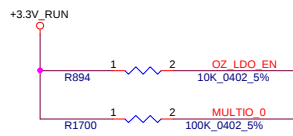
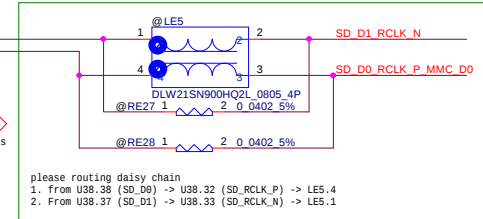
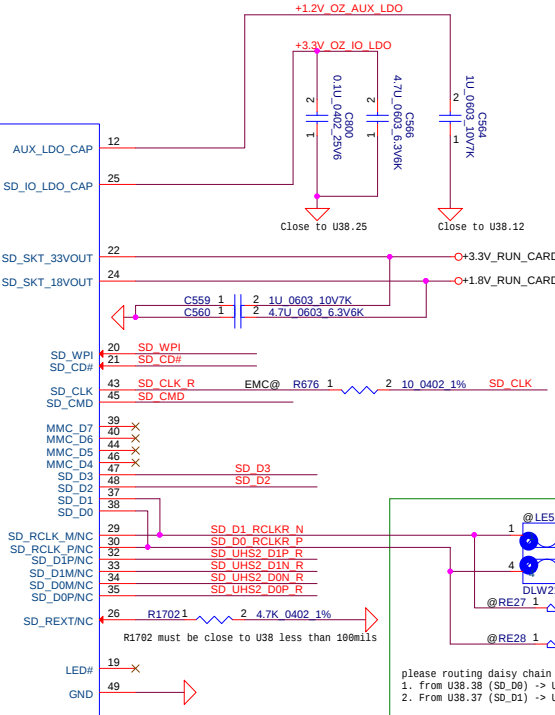
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Title			
USH board conn / TPM			
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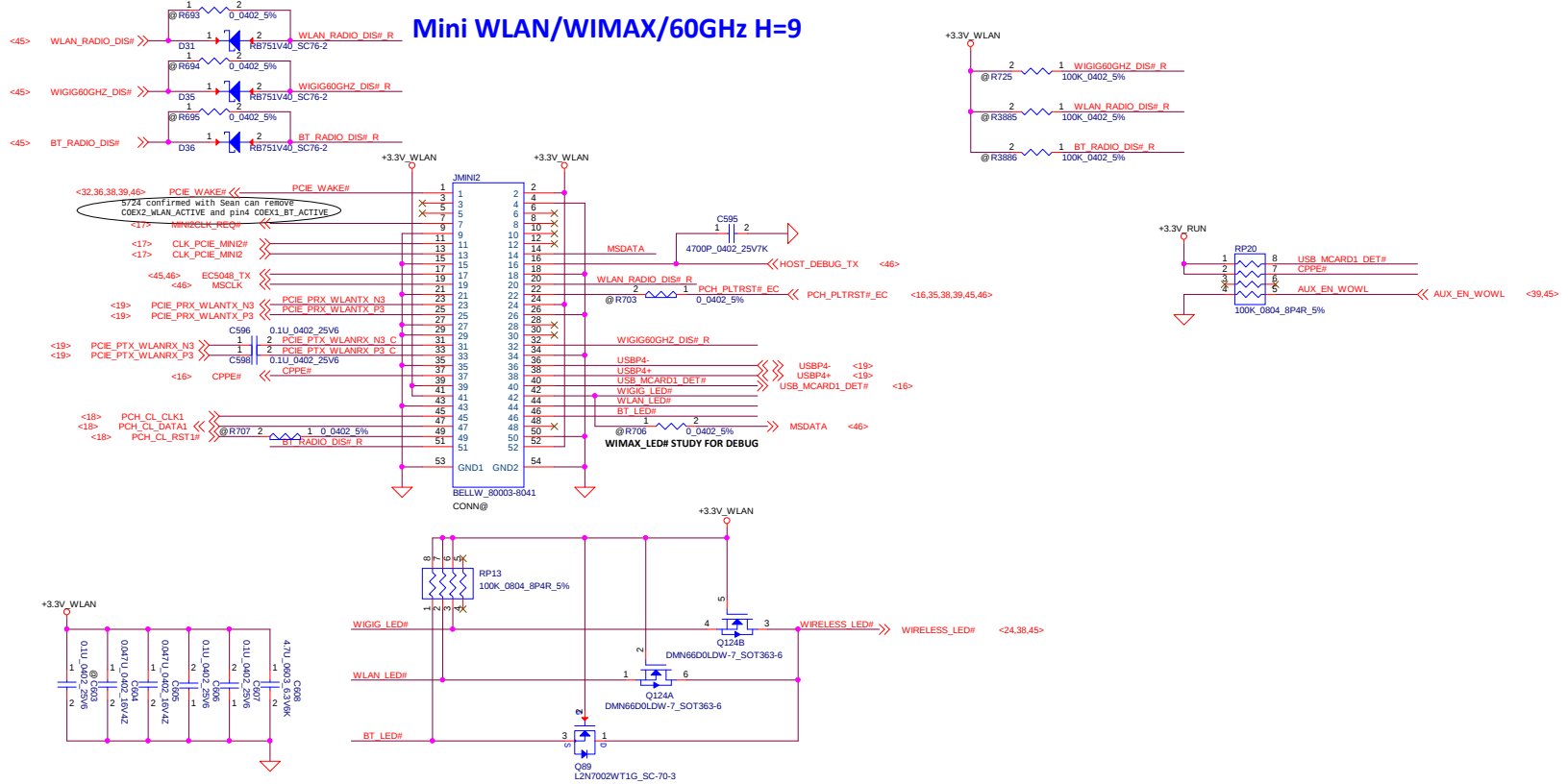
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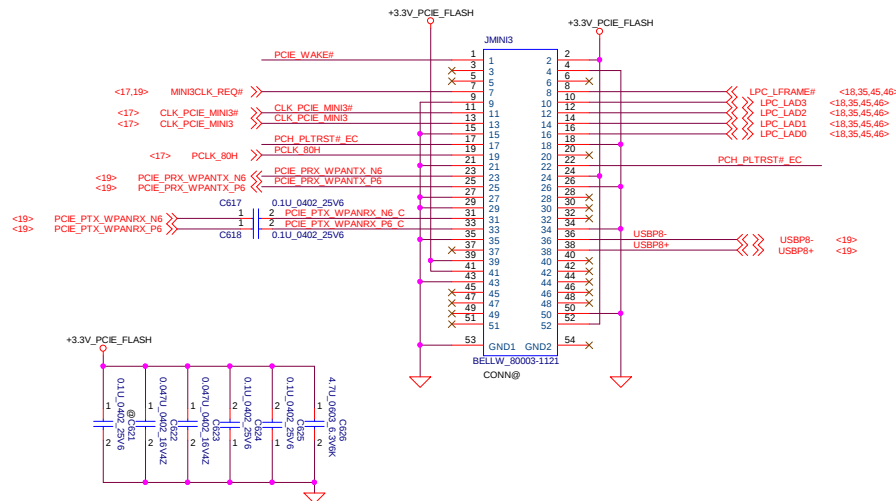
OZ777FJ2LN



Mini WLAN/WIMAX/60GHz H=9



1/2 Minicard Pink Pather Card H=9



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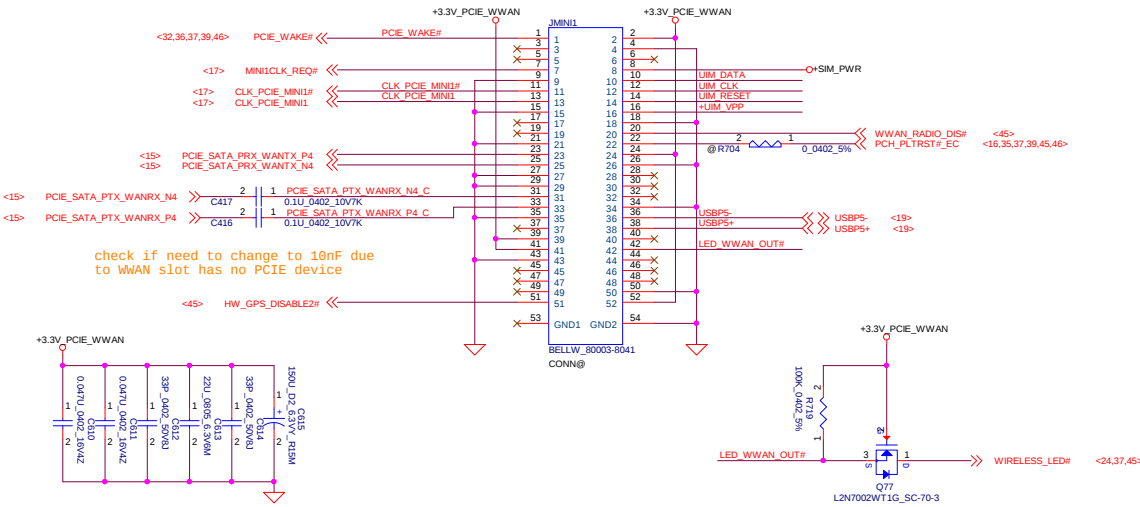
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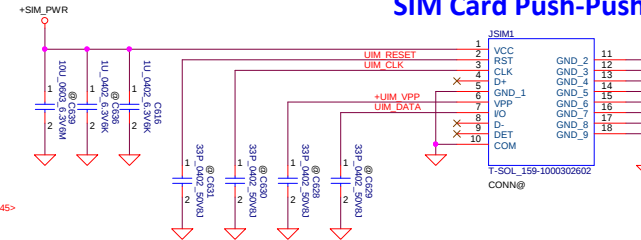
Mini WWAN/GPS/LTE/UWB H=9

- (1) Wake Enabled and Active
(2) Wake NOT Enabled nor Active

PWR Rail	Voltage Tolerance	D0-D2&D3 hot Power		D3 cold Power	
		Peak(mA)	Typ(mA)	Peak(mA)	Typ(mA)
+3.3V_PCIE_WWAN	+/-9%	2750	800	800 (1)	150 (1) 5 (2)



SIM Card Push-Push



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WWAN Mini Card

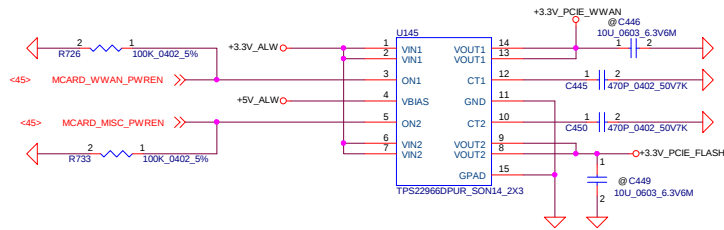
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Date: Wednesday, May 07, 2014

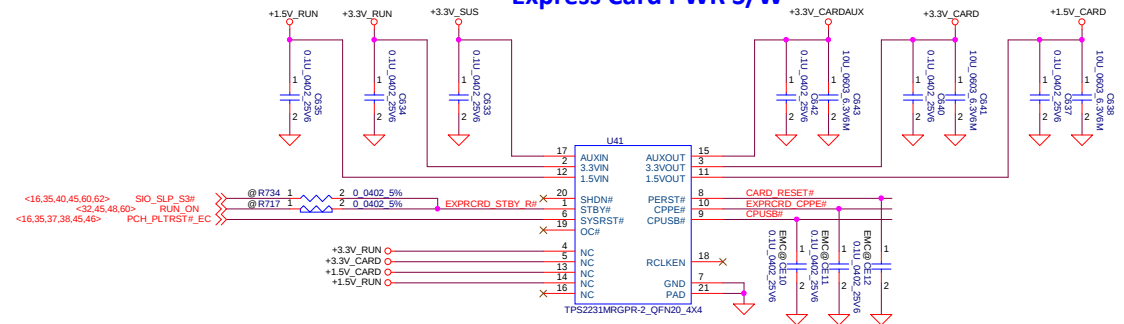
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+3.3V_PCIE_WWAN/+3.3V_PCIE_FLASH



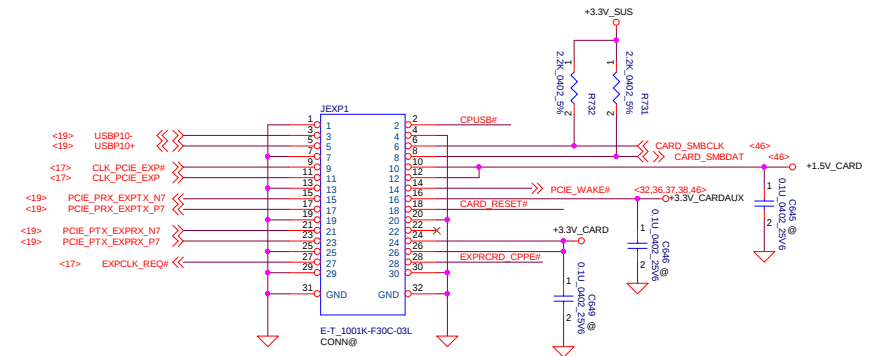
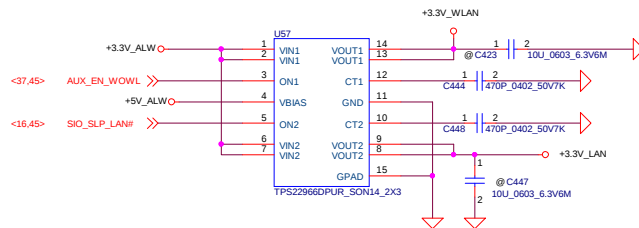
Express Card PWR S/W



Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part

Express Card Conn.

+3.3V_WLAN/+3.3V_LAN source



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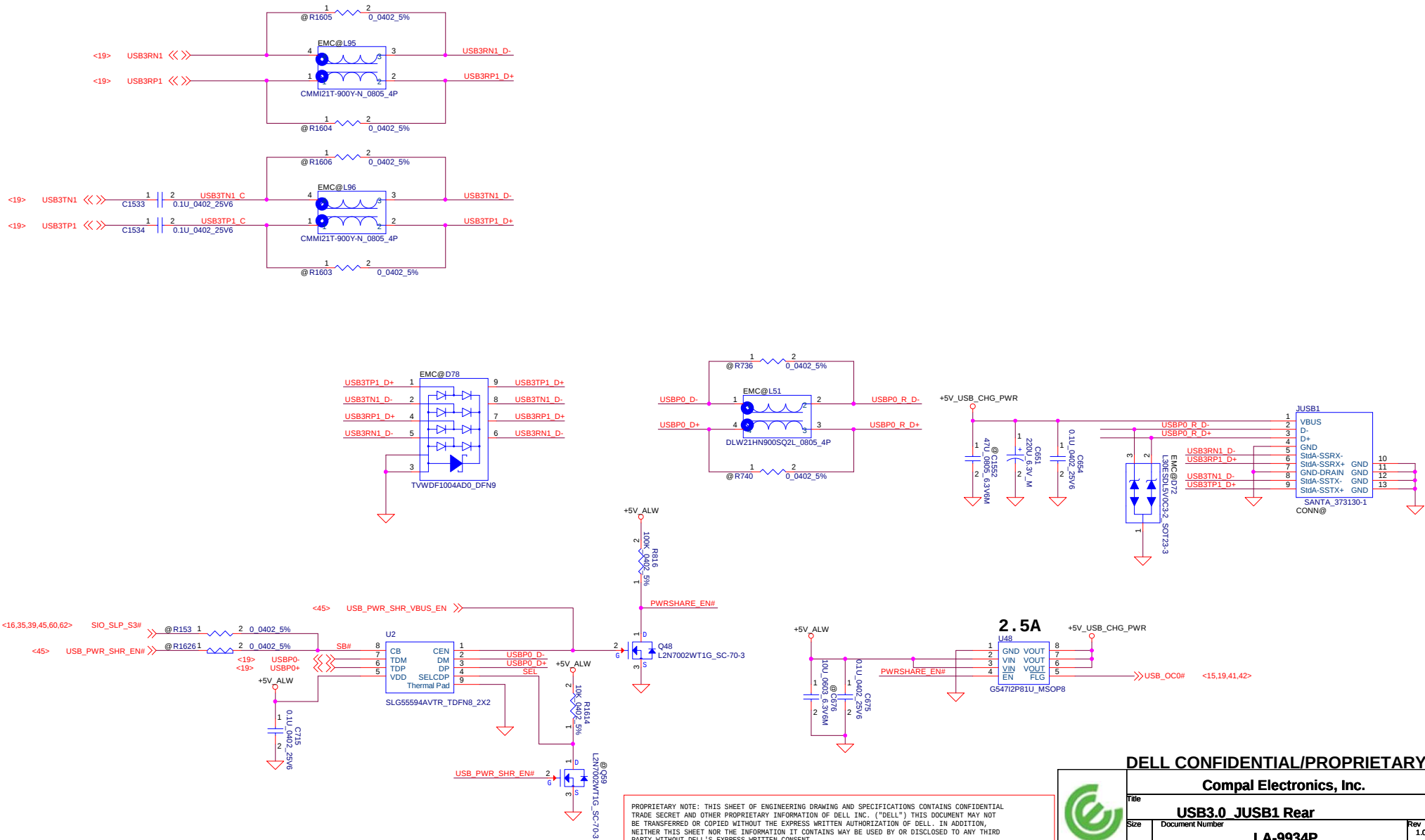
Compal Electronics, Inc.

PCIE-SATA SW / PCIE PWR

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Rear Side (JUSB1)



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USB3.0 JUSB1 Rear

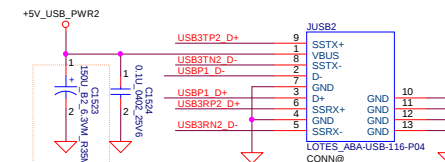
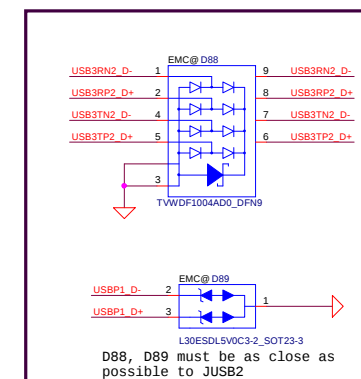
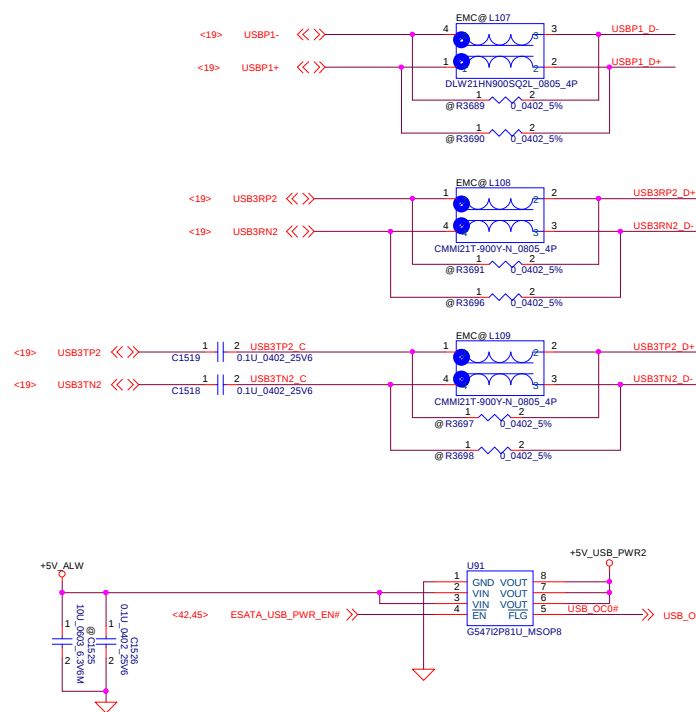
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Right Side Top (JUSB2)



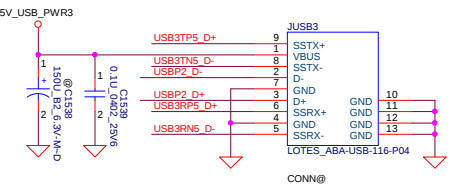
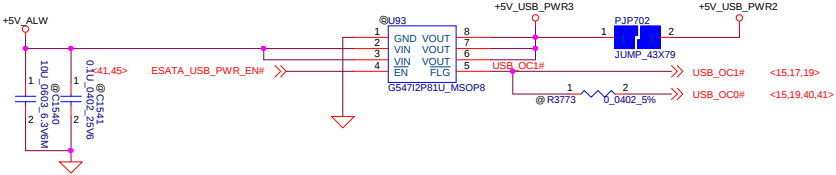
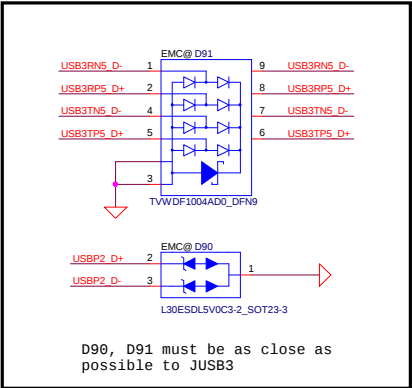
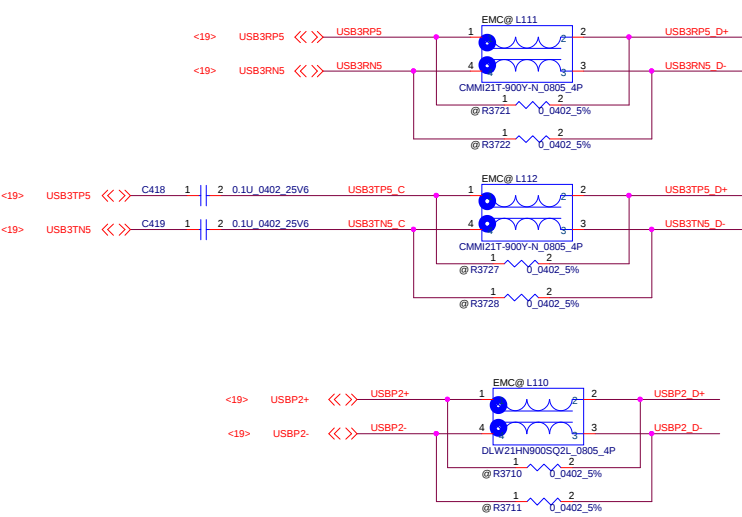
place C1523 between JUSB2 and JUSB3

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File	USB3.0 JUSB2 Right Side top
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Right Side bottom (JUSB3)

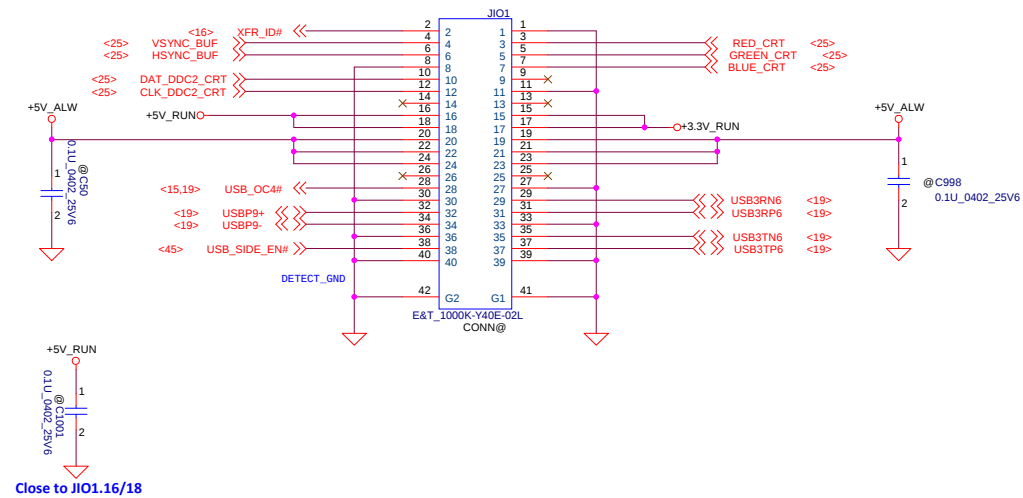


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		Compal Electronics, Inc.	
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I/O board CONN.



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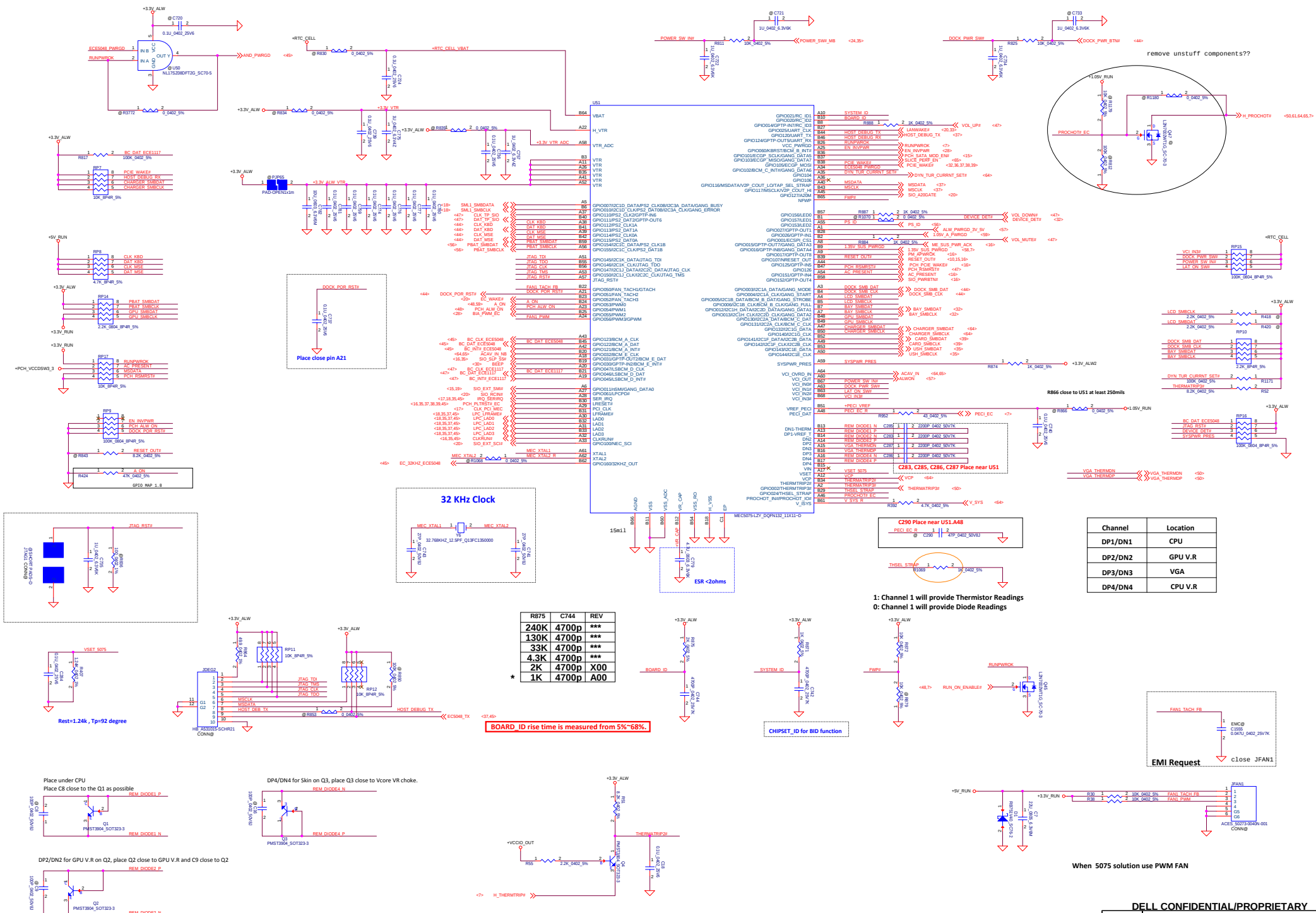


Compal Electronics, Inc.			
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USB3.0_JUSB4 Left Side			
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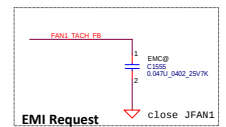
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Channel	Location
DP1/DN1	CPU
DP2/DN2	GPU V.R
DP3/DN3	VGA
DP4/DN4	CPU V.R

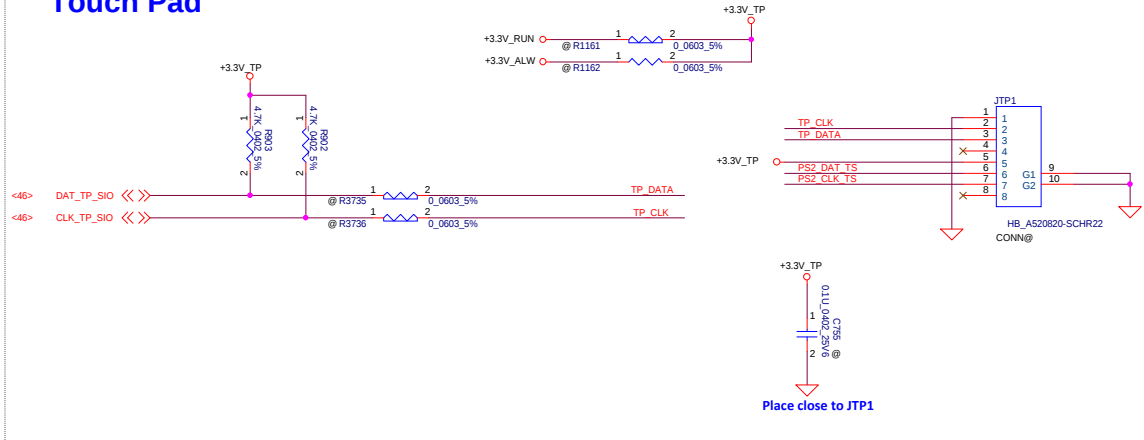
1: Channel 1 will provide Thermistor Readings
0: Channel 1 will provide Diode Readings



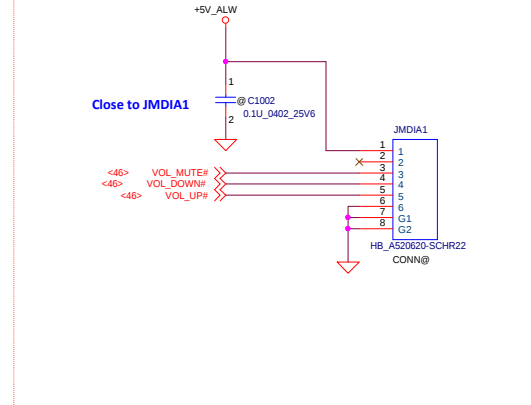
When 5075 solution use PWM FAN

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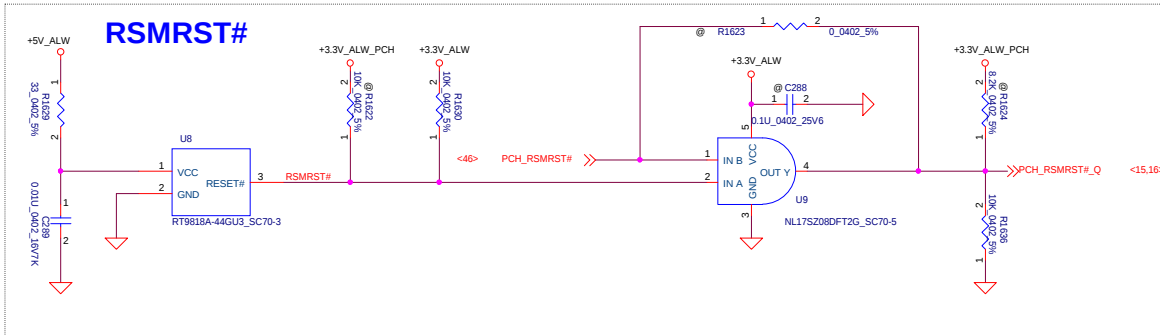
Touch Pad



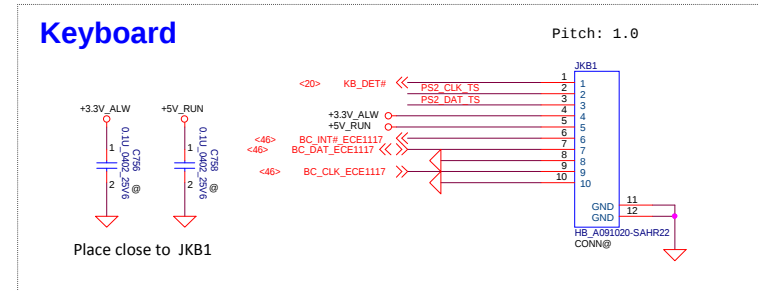
Media Board



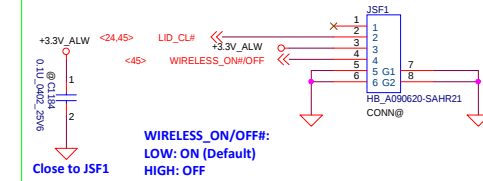
RSMRST#



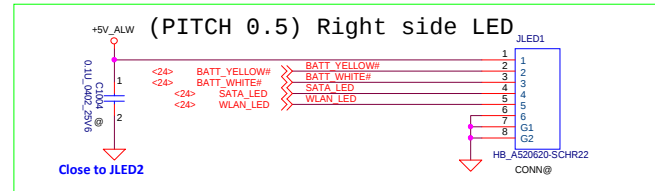
Keyboard



SNIFFER /Hall SENSOR BOARD



(PITCH 0.5) Right side LED

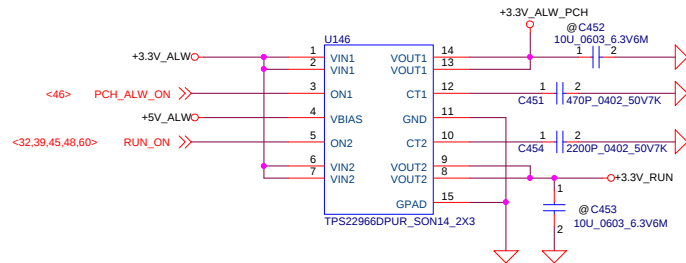


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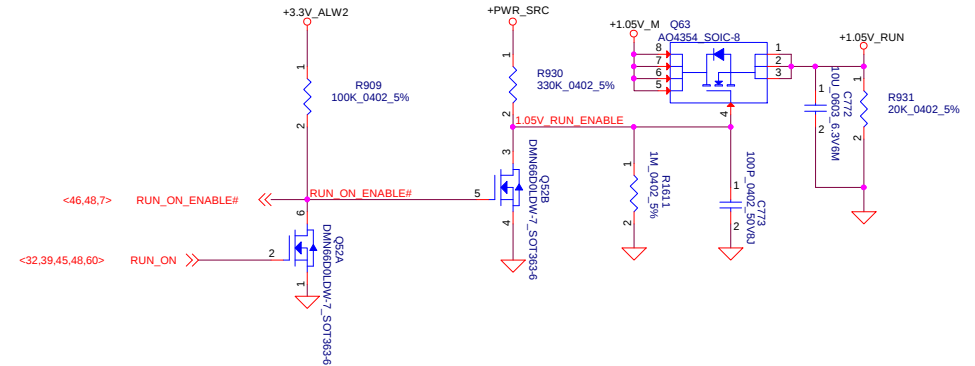
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	Title				
	Int KB/TP/BT/RSMRST				
	Size	Document Number		Rev	
		LA-9934P		1.0	
	Date: Wednesday, May 07, 2014	Sheet	47	of	71

+3.3V_ALW_PCH/+3.3V_RUN Source

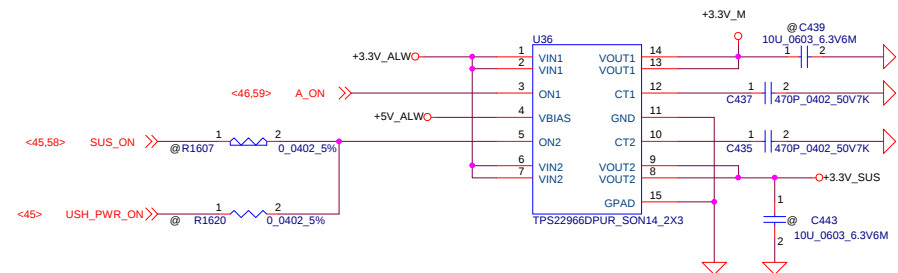


SI4164DY			
VDS	RDS(on)	ID(A)	
30	0.0032ohm at	VGS=10V	30A
30	0.0039ohm at	VGS=4.5V	26.3A

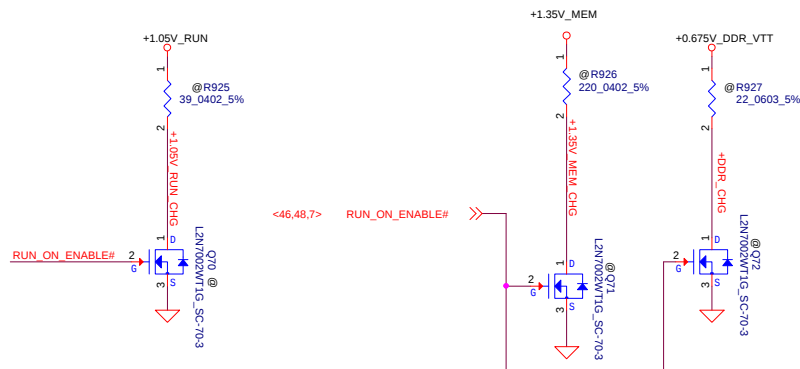
+1.05V_RUN Source



+3.3V_M/+3.3V_SUS source



Discharge Circuit



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POWER CONTROL

LA-9934P

Rev 1.0

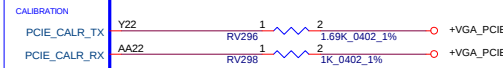
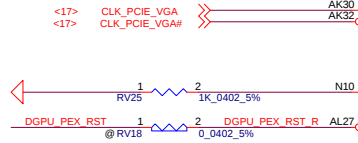
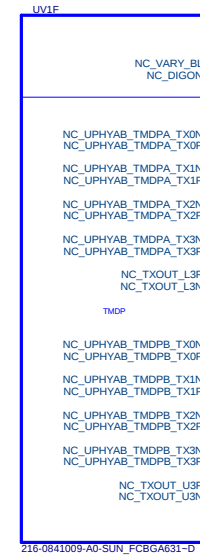
Date: Wednesday, May 07, 2014

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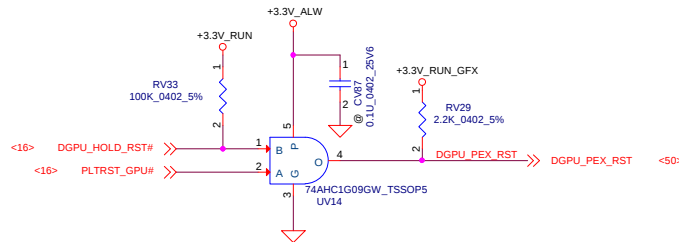
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PEG_CRX_GTX_N0	CV2	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N0
PEG_CRX_GTX_P1	CV4	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P1
PEG_CRX_GTX_N1	CV3	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N1
PEG_CRX_GTX_P2	CV5	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P2
PEG_CRX_GTX_N2	CV6	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N2
PEG_CRX_GTX_P3	CV7	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P3
PEG_CRX_GTX_N3	CV8	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N3
PEG_CRX_GTX_P4	CV9	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P4
PEG_CRX_GTX_N4	CV10	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N4
PEG_CRX_GTX_P5	CV11	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P5
PEG_CRX_GTX_N5	CV12	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N5
PEG_CRX_GTX_P6	CV14	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P6
PEG_CRX_GTX_N6	CV15	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N6
PEG_CRX_GTX_P7	CV16	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_P7
PEG_CRX_GTX_N7	CV17	2	1	0.22U	0402	16V7K	PEG_CRX_GTX_C_N7

PEG_CTX_GRX_P0	AF30	PCIE_RX0P
PEG_CTX_GRX_N0	AE31	PCIE_RX0N
PEG_CTX_GRX_P1	AE29	PCIE_RX1P
PEG_CTX_GRX_N1	AD28	PCIE_RX1N
PEG_CTX_GRX_P2	AD30	PCIE_RX2P
PEG_CTX_GRX_N2	AC31	PCIE_RX2N
PEG_CTX_GRX_P3	AC29	PCIE_RX3P
PEG_CTX_GRX_N3	AB28	PCIE_RX3N
PEG_CTX_GRX_P4	AB30	PCIE_RX4P
PEG_CTX_GRX_N4	AA31	PCIE_RX4N
PEG_CTX_GRX_P5	AA29	PCIE_RX5P
PEG_CTX_GRX_N5	Y28	PCIE_RX5N
PEG_CTX_GRX_P6	Y30	PCIE_RX6P
PEG_CTX_GRX_N6	W31	PCIE_RX6N
PEG_CTX_GRX_P7	W29	PCIE_RX7P
PEG_CTX_GRX_N7	V28	PCIE_RX7N

PCIE_TX0P	AH30	PEG_CRX_GTX_C_P0
PCIE_TX0N	AG31	PEG_CRX_GTX_C_N0
PCIE_TX1P	AG29	PEG_CRX_GTX_C_P1
PCIE_TX1N	AF28	PEG_CRX_GTX_C_N1
PCIE_TX2P	AF27	PEG_CRX_GTX_C_P2
PCIE_TX2N	AF26	PEG_CRX_GTX_C_N2
PCIE_TX3P	AD27	PEG_CRX_GTX_C_P3
PCIE_TX3N	AD26	PEG_CRX_GTX_C_N3
PCIE_TX4P	AC25	PEG_CRX_GTX_C_P4
PCIE_TX4N	AB25	PEG_CRX_GTX_C_N4
PCIE_TX5P	Y23	PEG_CRX_GTX_C_P5
PCIE_TX5N	Y24	PEG_CRX_GTX_C_N5
PCIE_TX6P	AB27	PEG_CRX_GTX_C_P6
PCIE_TX6N	AB26	PEG_CRX_GTX_C_N6
PCIE_TX7P	Y27	PEG_CRX_GTX_C_P7
PCIE_TX7N	Y26	PEG_CRX_GTX_C_N7
NC#W24	W24	
NC#W23	W23	
NC#V27	V27	
NC#V26	V26	
NC#U24	U24	
NC#U23	U23	
NC#T26	T26	
NC#T27	T27	
NC#T24	T24	
NC#T23	T23	
NC#P27	P27	
NC#P26	P26	
NC#P24	P24	
NC#P23	P23	
NC#M27	M27	
NC#M26	M26	



don't connect to PCH



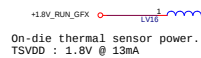
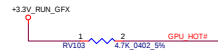
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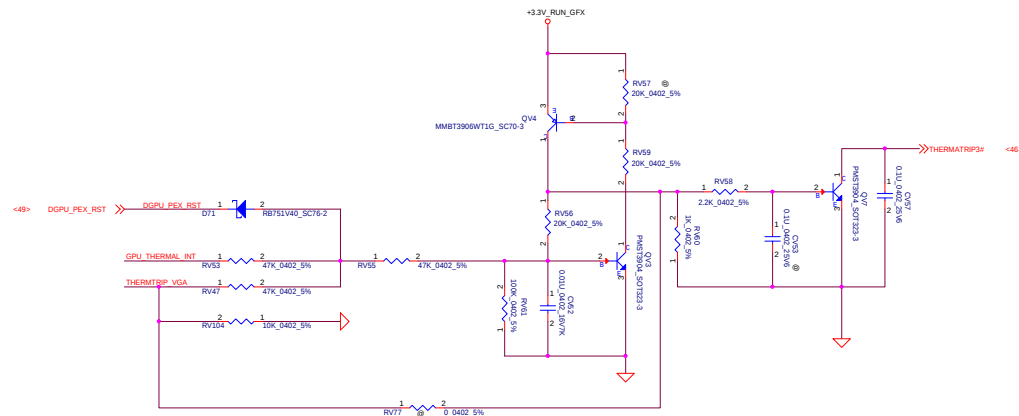
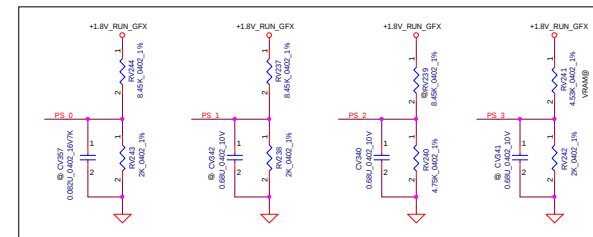


Title	SUN-PCIE	Rev	1.0
Size	Document Number	LA-9934P	
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Hynix VRAM: RV241 =8.45k
* Samsung VRAM: RV241 =4.53Kohm



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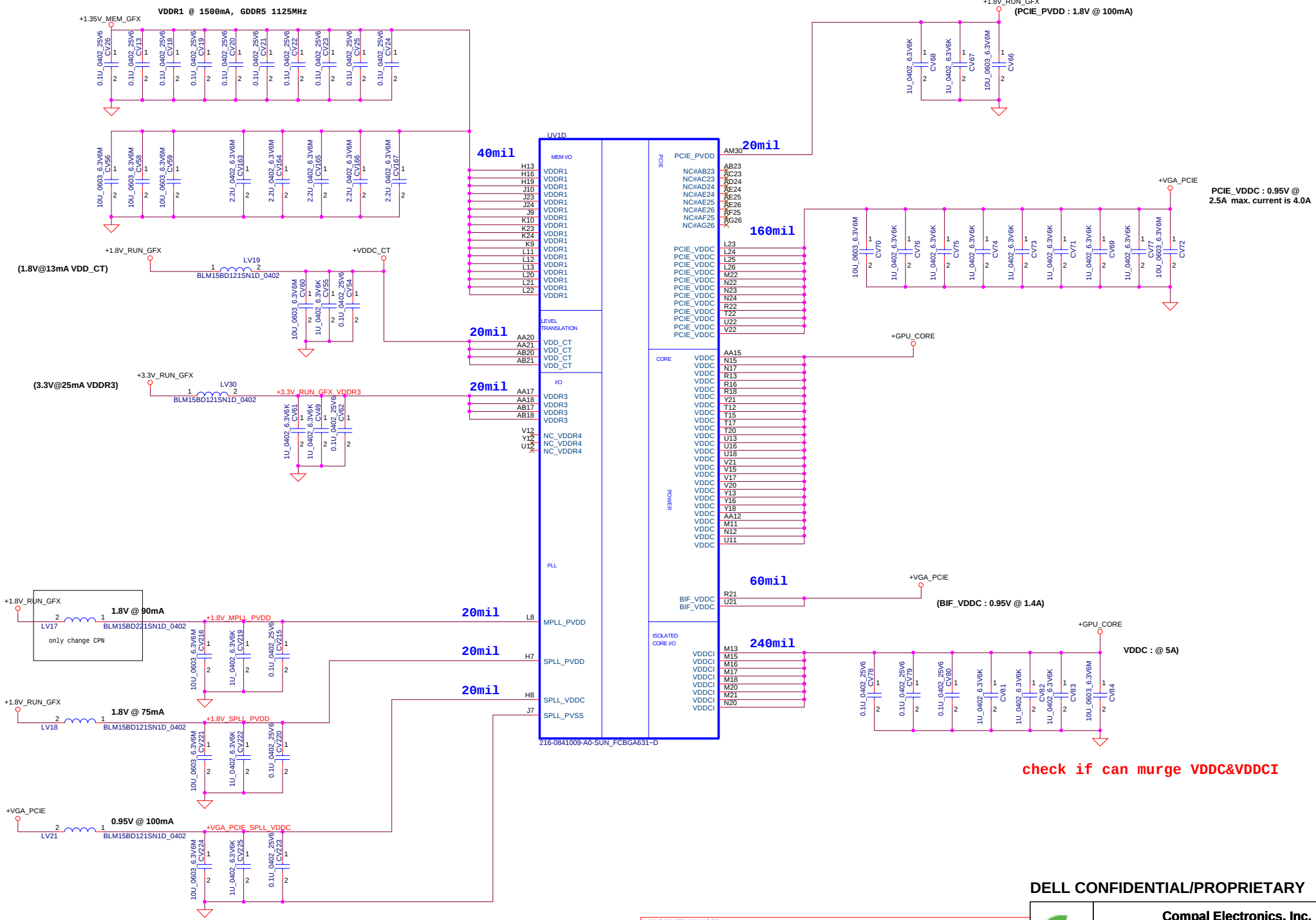
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SUN-GPIO,HDMI,DP,DAC

Size	Document Number
	LA 99245

LA-9934P
Date: Wednesday, May 07, 2014 Sheet 50 of 71

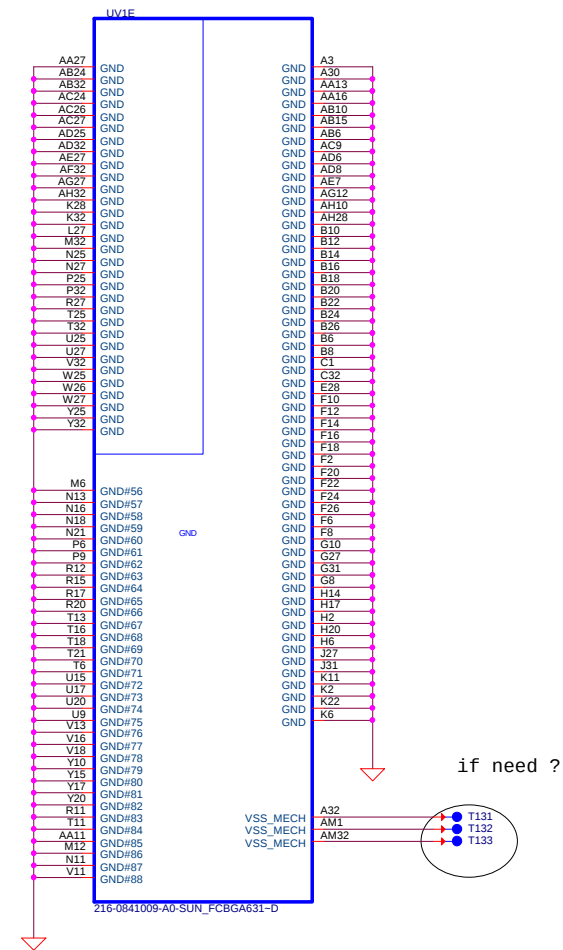
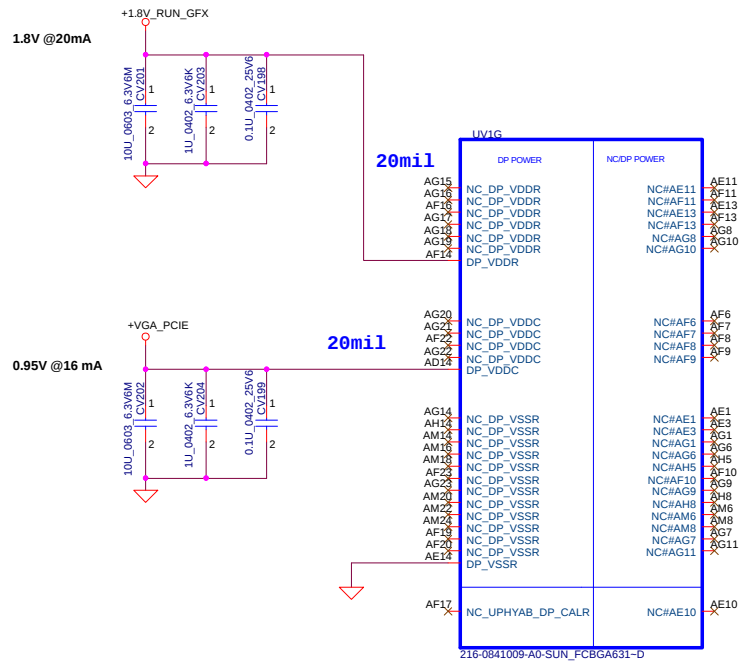
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MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

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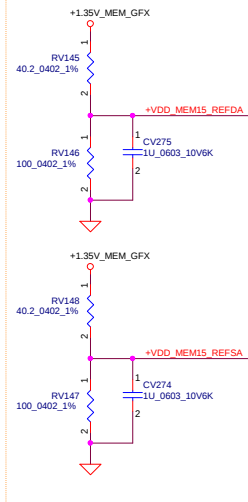
SUN-DP Power,GND

LA-9934P

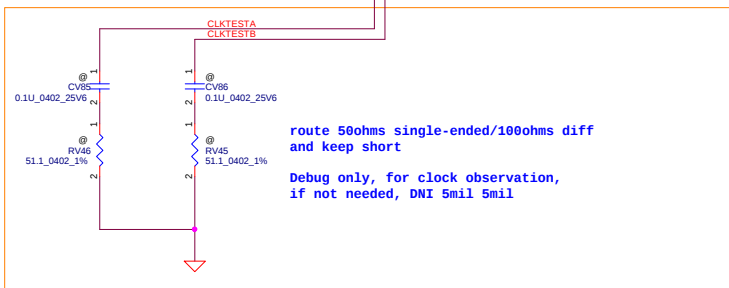
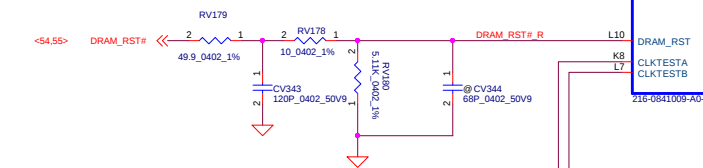
Date: Wednesday, May 07, 2014 Sheet 52 of 71

DQA0_0[0..31] <<>> DQA0_0[0..31] <S4>
 DQA1_0[0..31] <<>> DQA1_0[0..31] <S5>
 MAA0_0[0..8] <<>> MAA0_0[0..8] <S4>
 MAA1_0[0..8] <<>> MAA1_0[0..8] <S5>
 EDCA0_0[0..3] <<>> EDCA0_0[0..3] <S4>
 EDCA1_0[0..3] <<>> EDCA1_0[0..3] <S5>
 DOBIA0_0[0..3] <<>> DOBIA0_0[0..3] <S4>
 DOBIA1_0[0..3] <<>> DOBIA1_0[0..3] <S5>

Place close to UV1

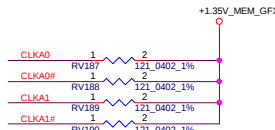


Place RV178-RV180, CV343, CV344 close to UV1 within 1000mil

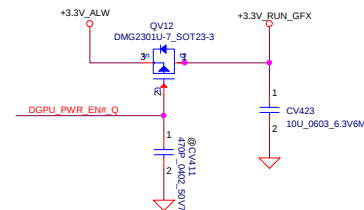


route 50ohms single-ended/100ohms diff and keep short

Debug only, for clock observation, if not needed, DNI 5mil 5mil

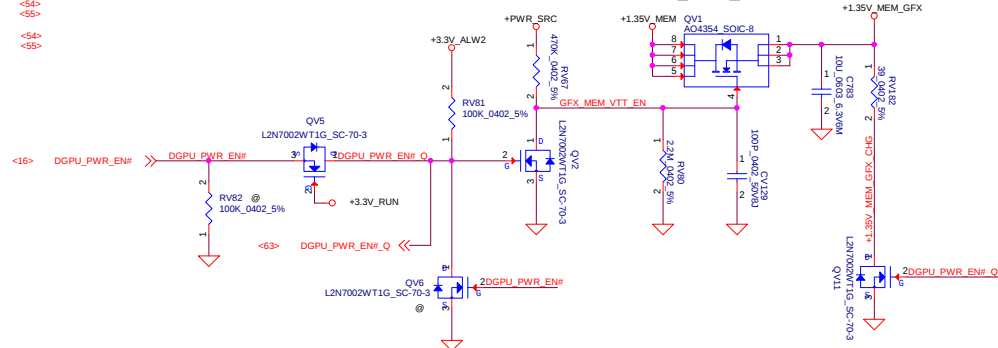


+3.3V_RUN_GFX Source



SI4164DY	RDS(on)	ID(A)
VDS	30	30
	0.0632ohm at VGS=10V	30A
	30	0.0639ohm at VGS=4.5V
		26.3A

+1.35V_MEM_GFX Source



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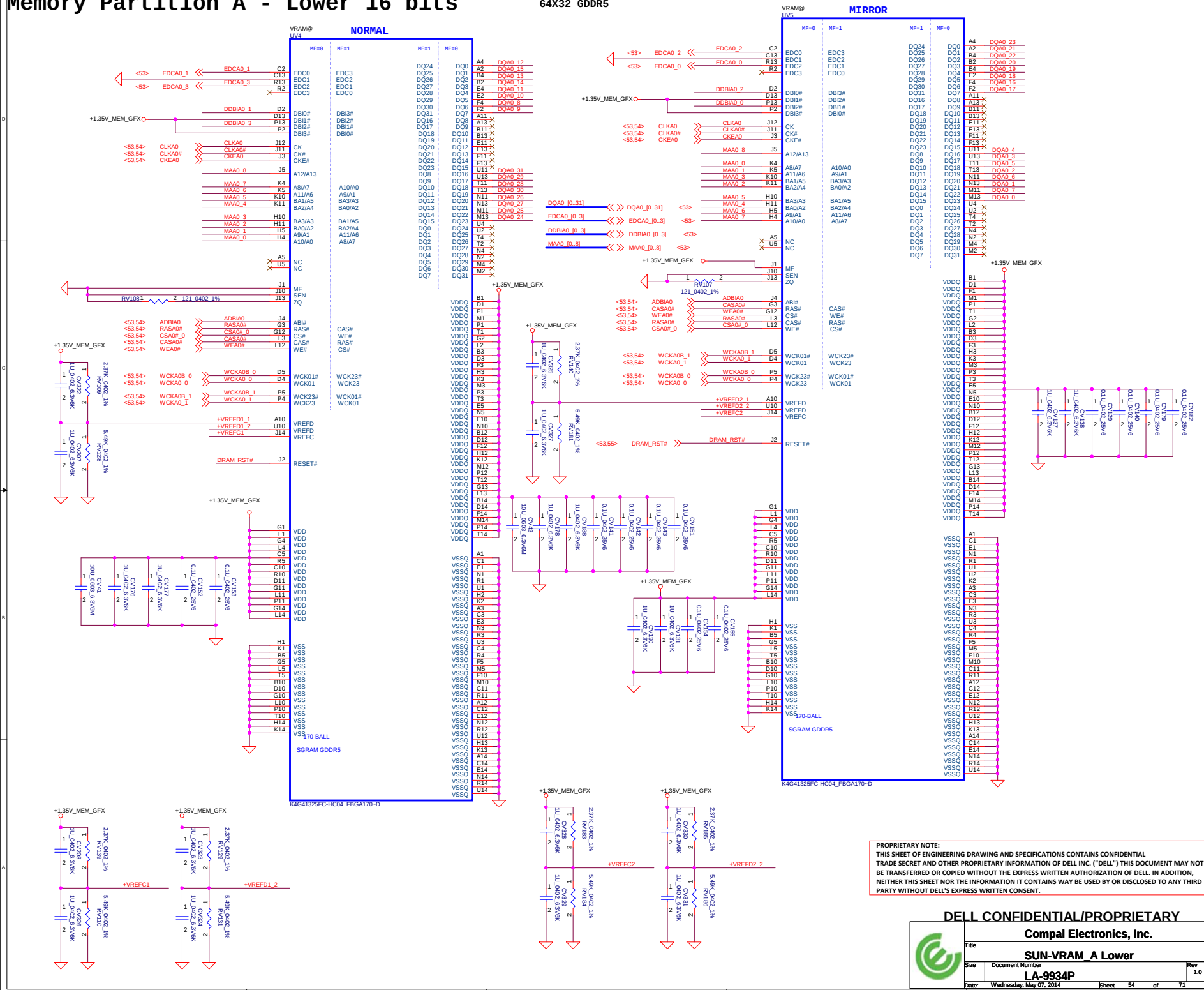
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Title	SUN-MEM Interface A	Rev	1.0
Size	Document Number		
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Memory Partition A - Lower 16 bits

64X32 GDDR5

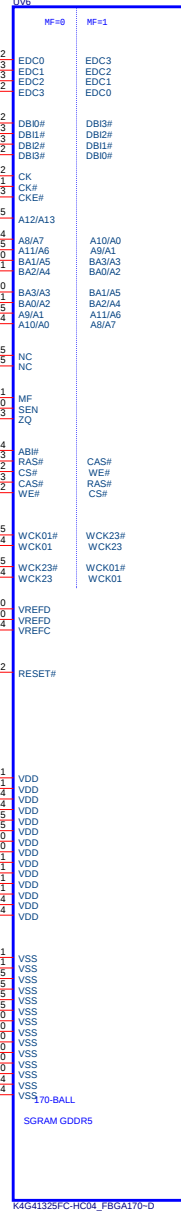
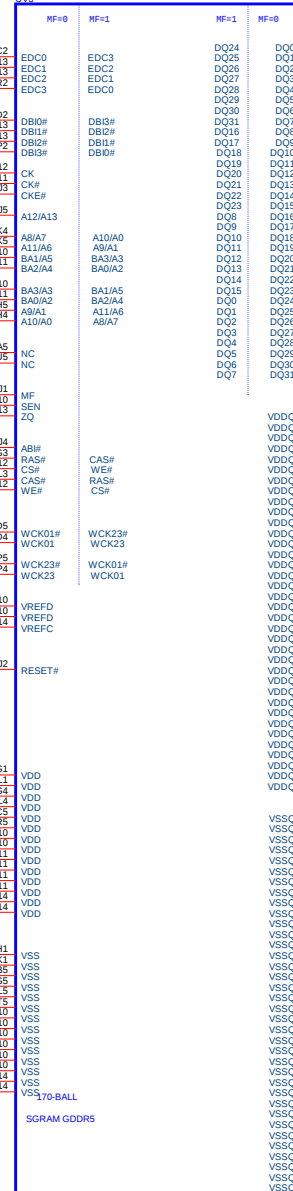


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File	SUN-VRAM_A Lower		
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Memory Partition A - Upper 16 bits



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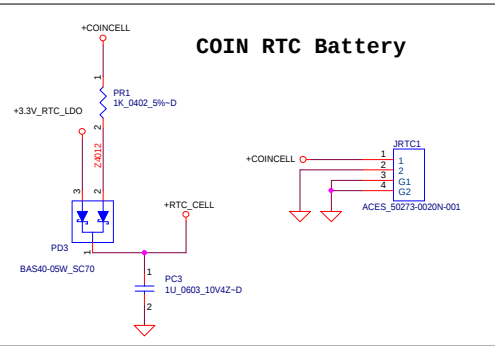
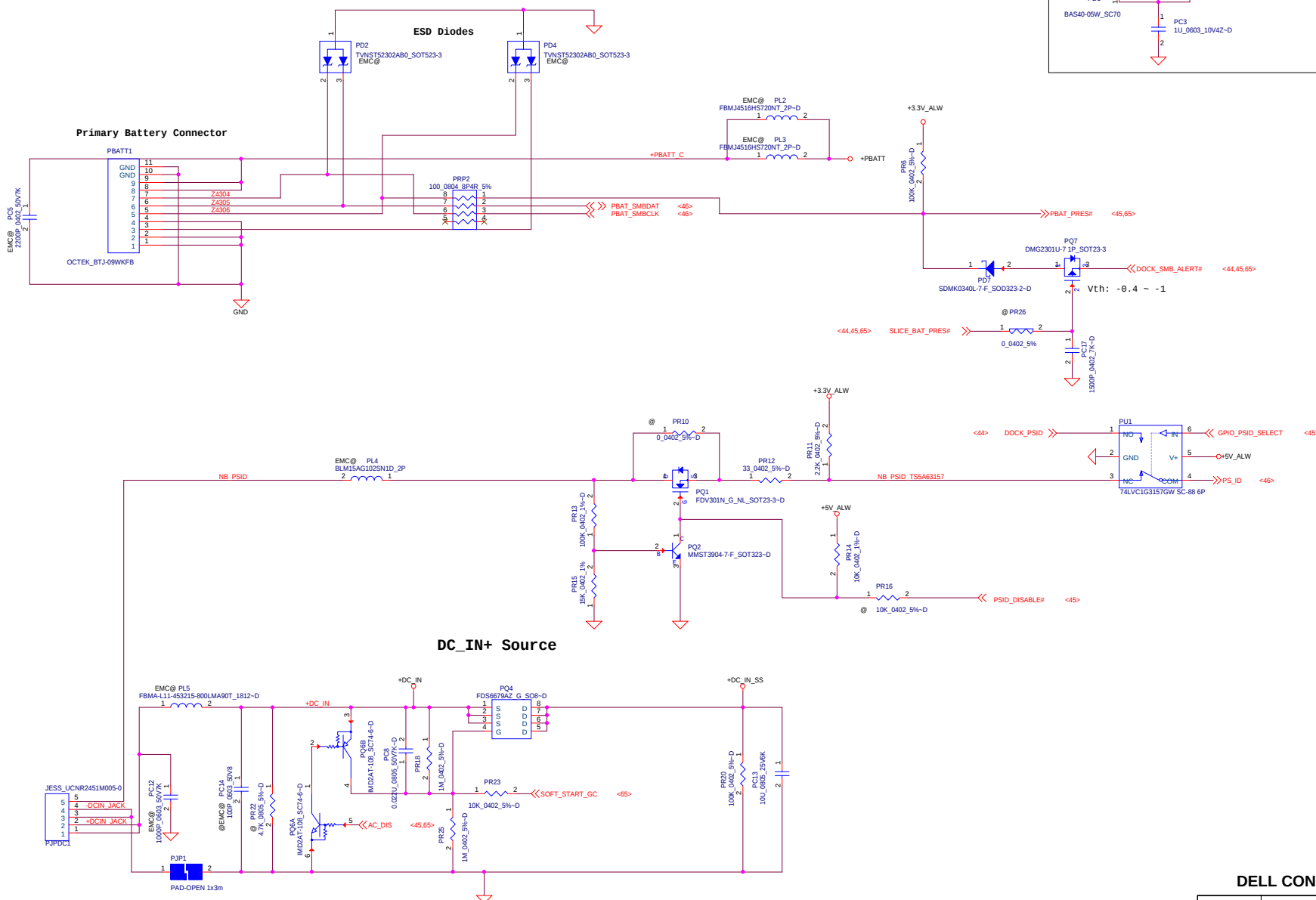
SUN-VRAM A Upper

ent Number
LA-9934P

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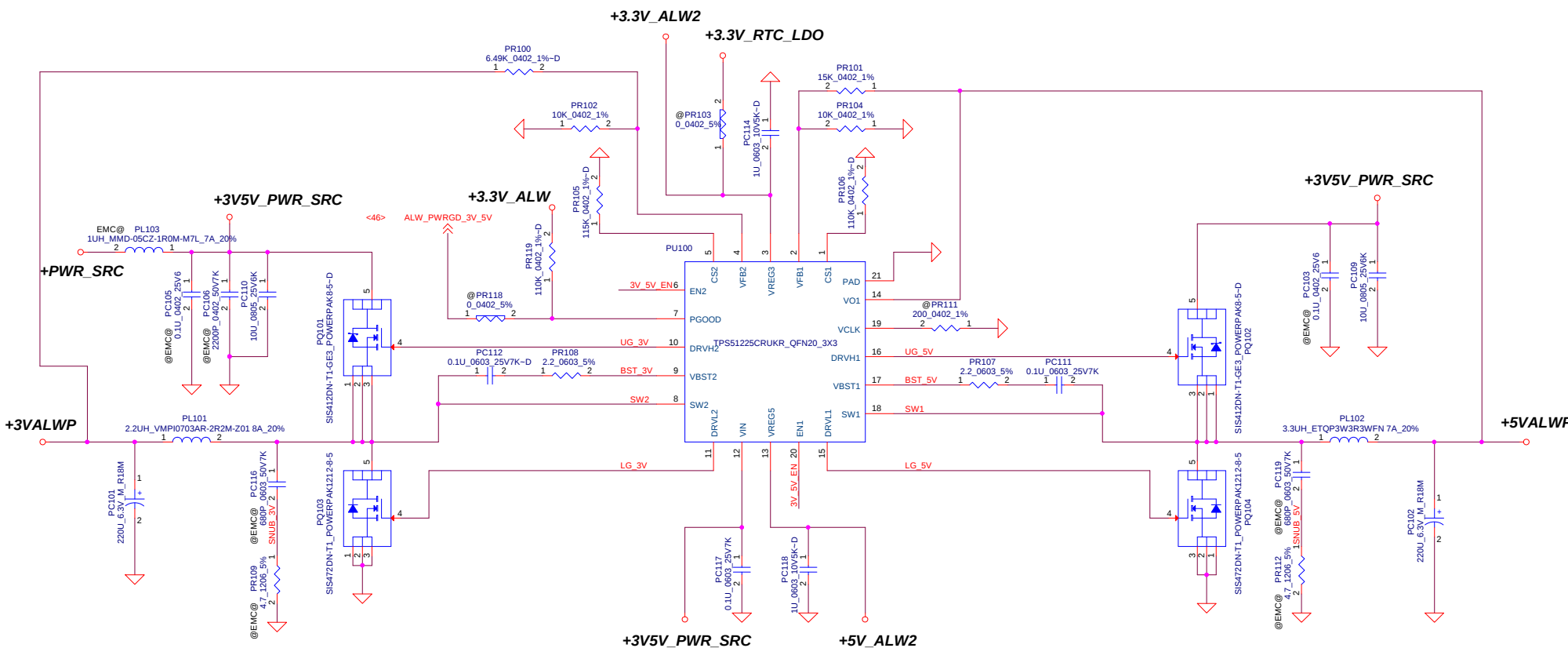




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		PWR +DCIN	
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+3VALWP
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 Frequency 350kHz
 TDC 6.48A
 Peak Current 9.25A
 OCP current 11.1A
 TYP MAX
 H/S Rds(on) 24mohm , 30mohm
 L/S Rds(on) 10.3mohm , 12.4mohm
 Choke DCR Max:17mohm

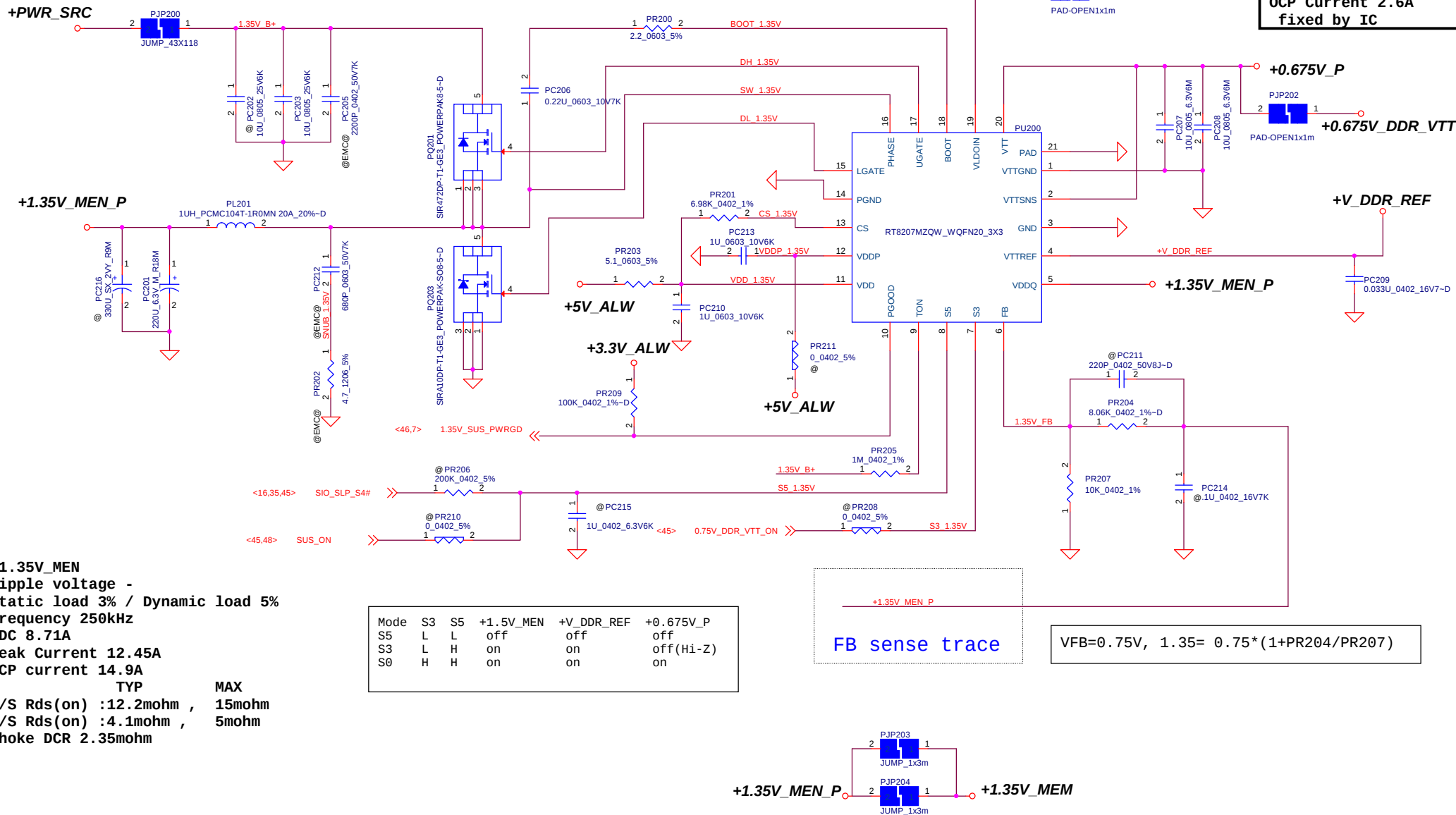
+5VALWP
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 Frequency 300kHz
 TDC 6.08A
 Peak Current 8.68A
 OCP current 10.4A
 TYP MAX
 H/S Rds(on) 24mohm , 30mohm
 L/S Rds(on) 10.3mohm , 12.4mohm
 Choke DCR Max:28mohm

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Title			
PWR_+3VALWP/5VALWP			
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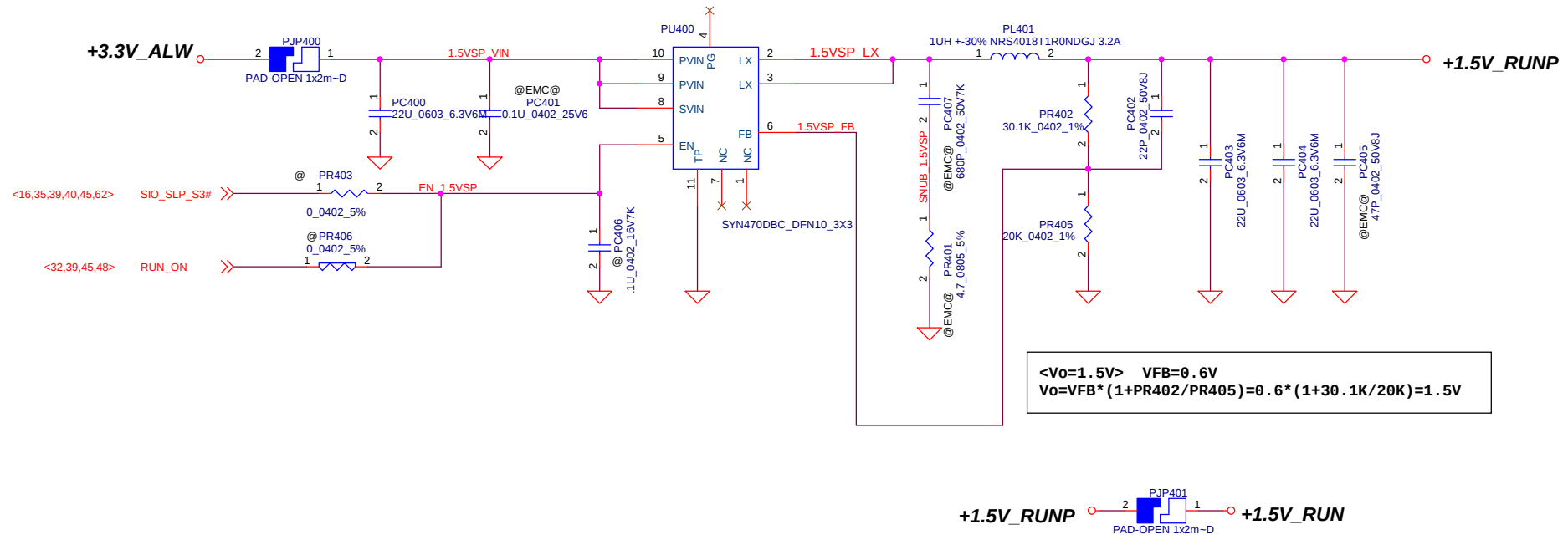
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Size: Document Number: **LA-9934P** Rev: 1.0

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+1.5V_RUN
 Ripple voltage -
 Static load 3% / Dynamic load 5%
 Frequency 1MHz
 TDC 0.63A
 Peak Current 0.9A
 OCP current 4A fixed by IC
 Choke DCR 27mohm

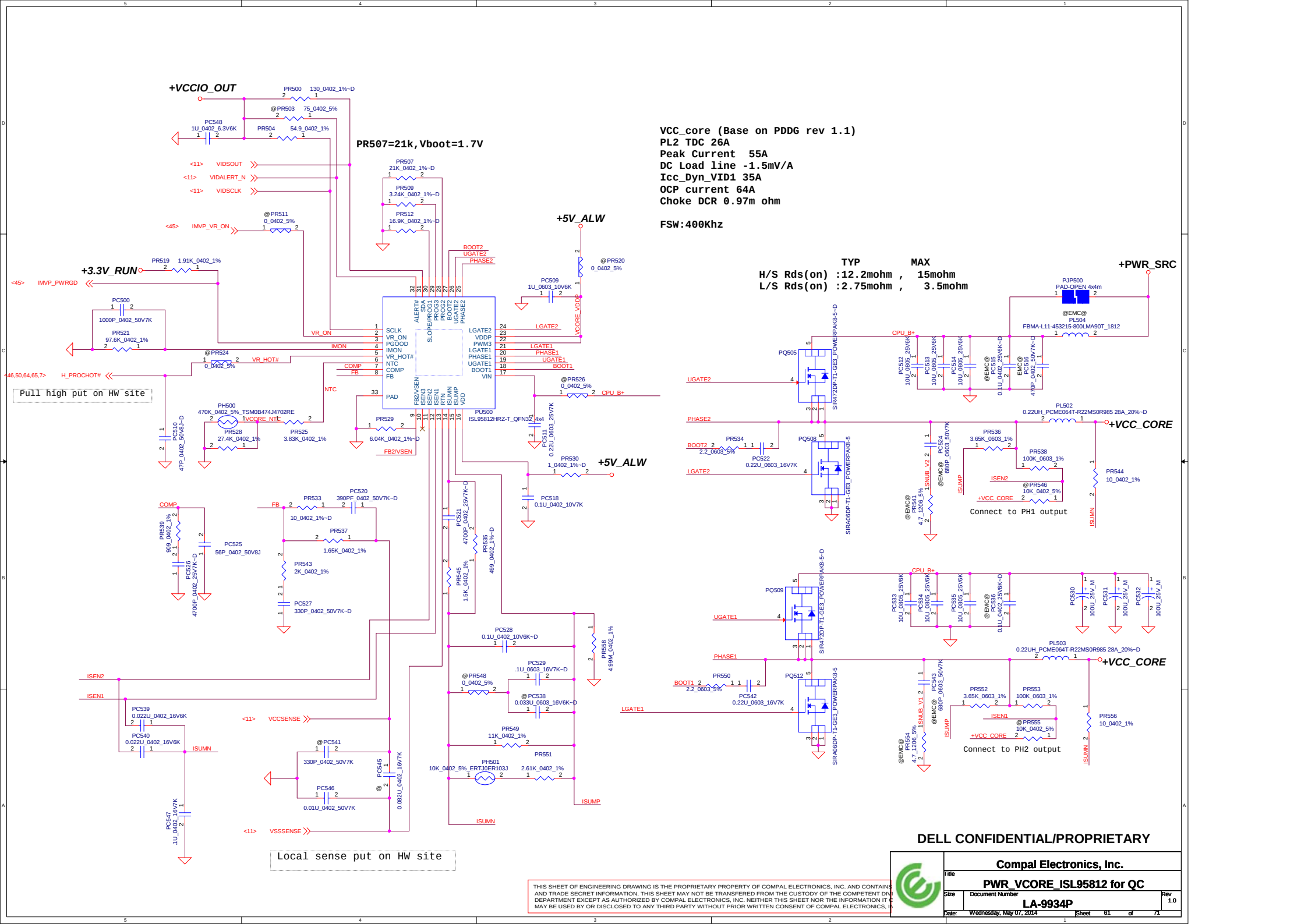


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Compal Electronics, Inc.			
Title			
PWR_+1.5V_RUNP			
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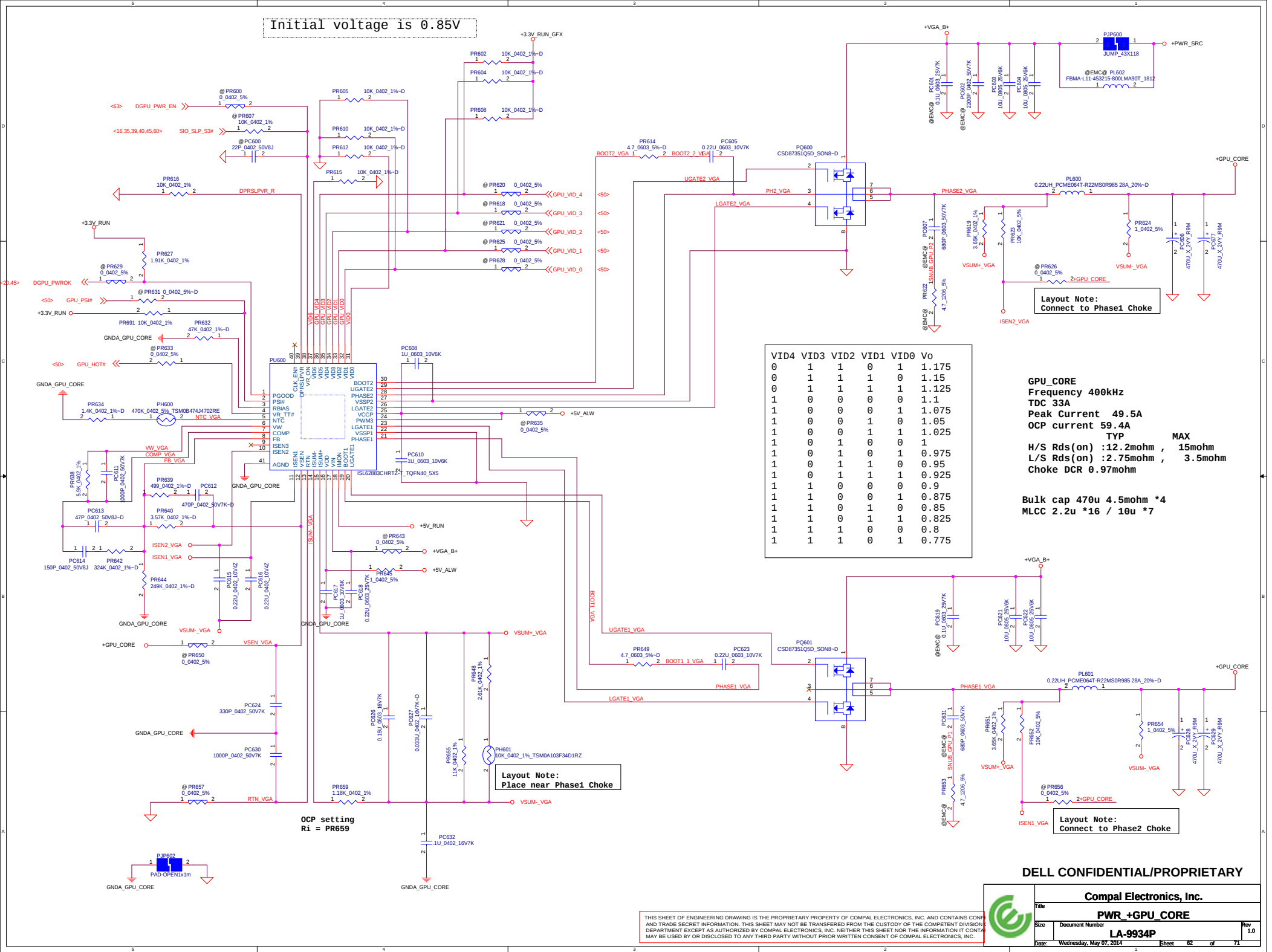
VCC_core (Base on PDDG rev 1.1)
PL2 TDC 26A
Peak Current 55A
DC Load line -1.5mV/A
Icc_Dyn_VID1 35A
OCP current 64A
Choke DCR 0.97m ohm
FSW:400Khz

TYP MAX
H/S Rds(on) :12.2mohm , 15mohm
L/S Rds(on) :2.75mohm , 3.5mohm

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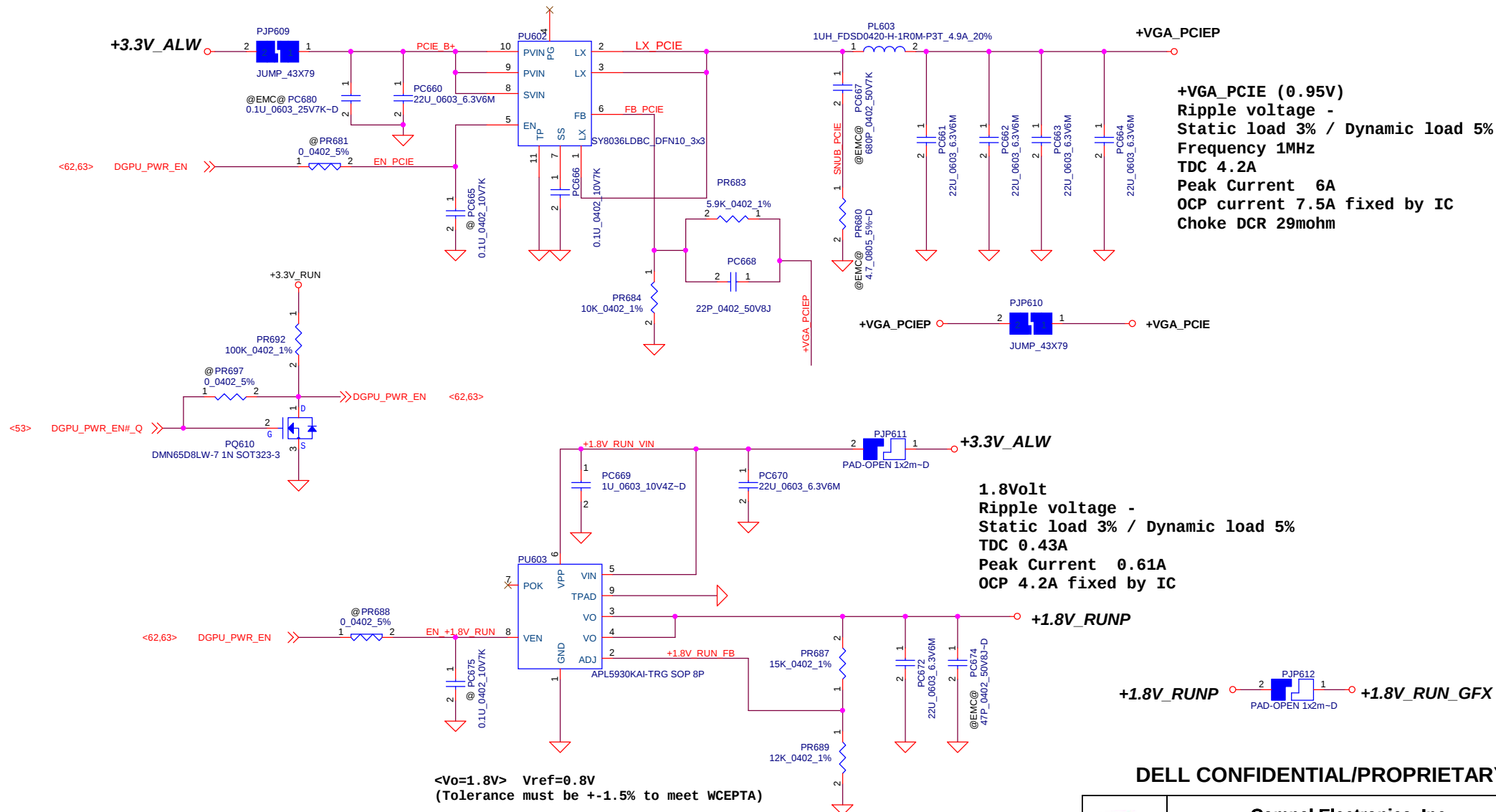
Compal Electronics, Inc.			
PWR_VCORE_ISL95812 for QC			
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Initial voltage is 0.85V



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$$V_{FB}=0.6V \quad V_0=V_{FB} \cdot (1+PR683/PR684)=0.6 \cdot (1+5.9K/10K)=0.95V$$



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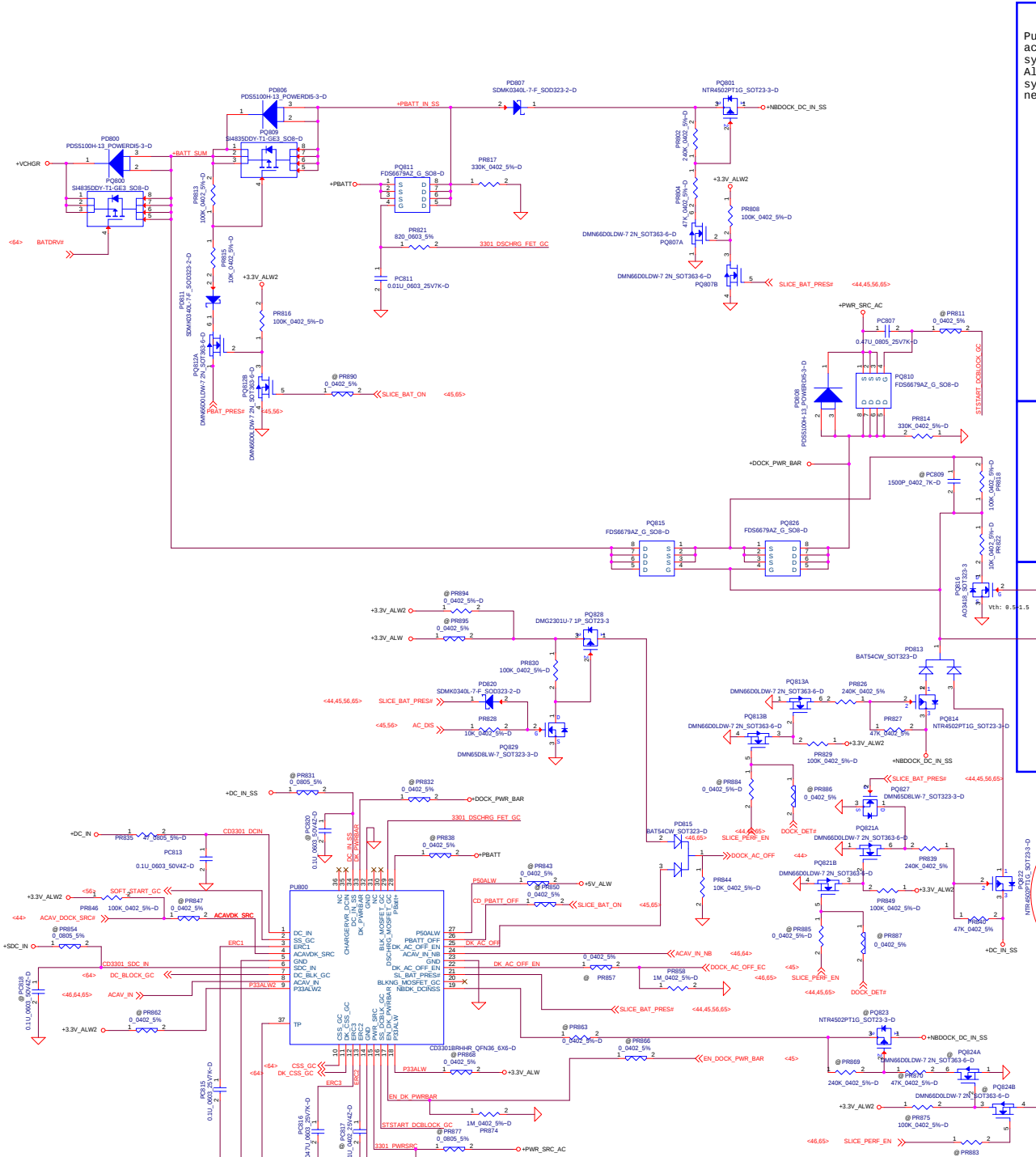
Title	PWR +VGA PCIE/+1.8V RUN GFX
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Size	Document Number	Rev
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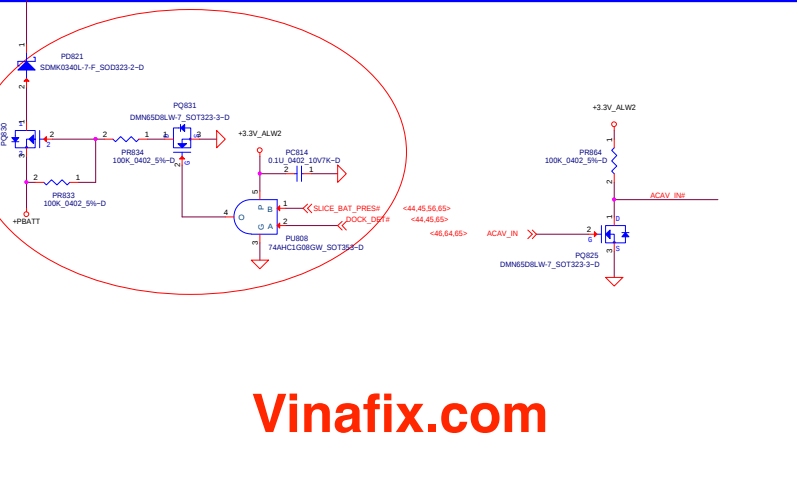
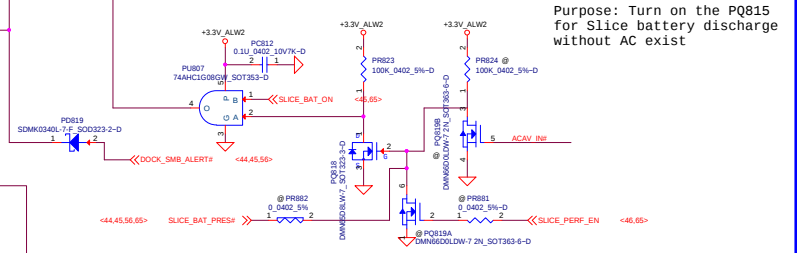
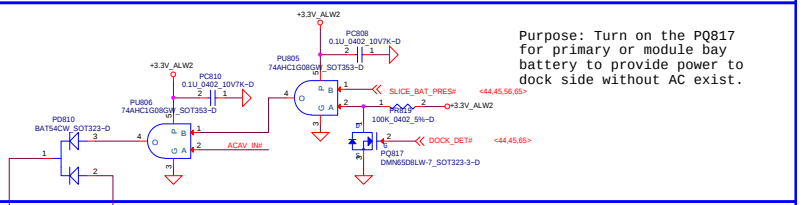
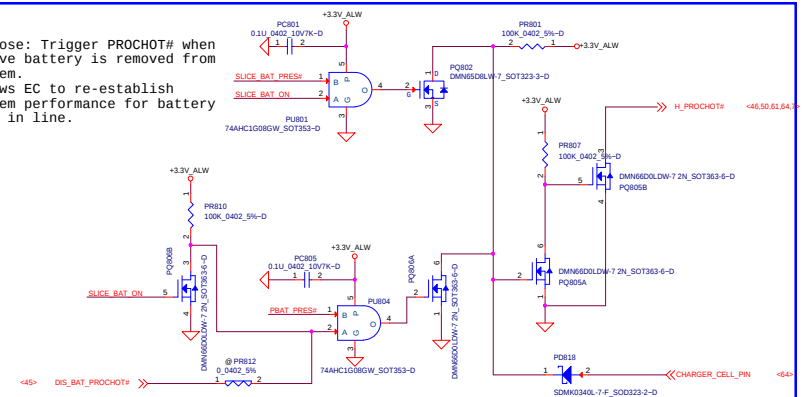
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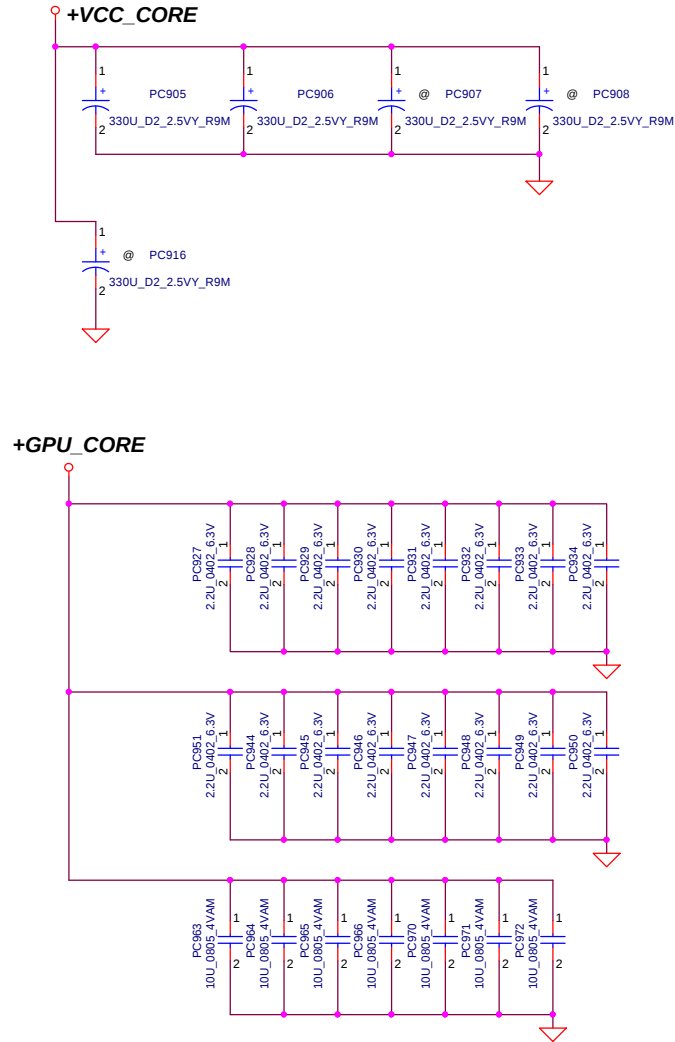
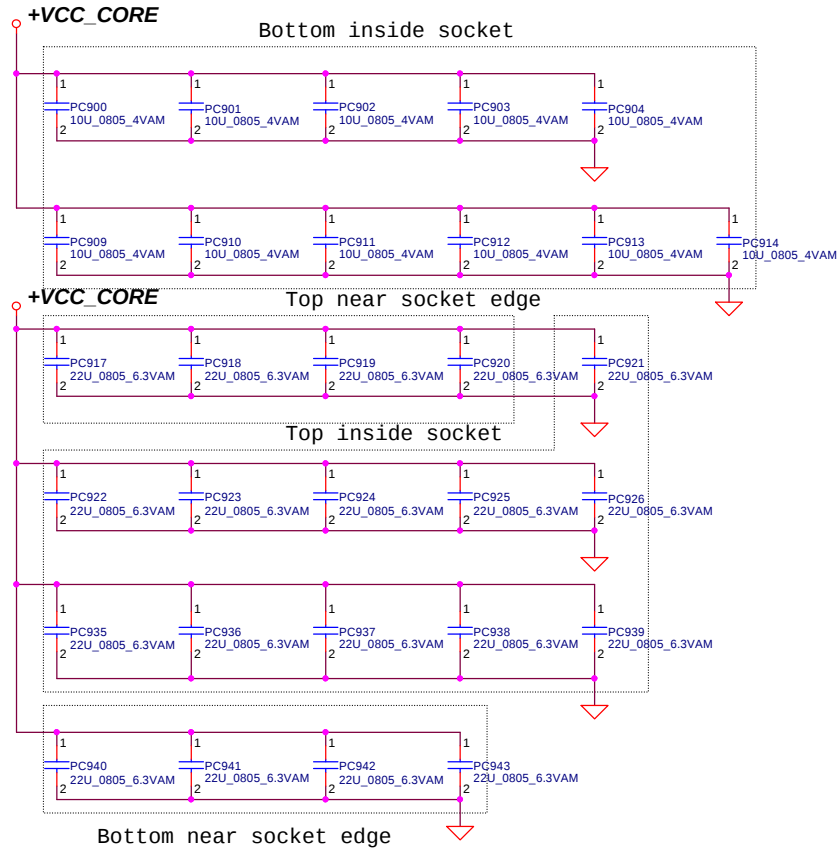
Purpose: Trigger PROCHOT# when active battery is removed from system.
Allows EC to re-establish system performance for battery next in line.



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Based on PDDG rev 1.1 Table 5-1.



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PWR_PROCESSOR DECOUPLING			
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	64	Charger	1/8	TI	Change cell pin pull high reference voltage from +3.3V_ALW to BQ24715_REGN	Depop PR720 and pop PR746	X01
2	64	Charger	1/8	Compal	Reduce adapter current ripple	PC714,PC728,PC712,PC713,PC714,PC734 pop 22uF cap	X01
3	61	VCC_CORE	1/8	Compal	Reduce adapter current ripple	Add input jump PJP500 and unpop PL504, PC516 pop 470pF	X01
4	64	Charger	1/8	Compal	Fine tune H_PROCHOT# response time.	Add 0402 cap PC736(1.2nF) on PU701 pin1	X01
5	64	Charger	1/8	Compal	Control H_PROCHOT# when AC removed.	Add PR727(0 ohm) and MODULE_BATT_PRES# connect to PU701 pin1	X01
6	61	VCC_CORE	1/8	Compal HW	Reduce noise on +VCCIO_OUT.	Add 1uF cap (PC548) on +VCCIO_OUT	X01
7	61	Charger	1/8	Compal	For Input current sense stabilize.	PC703 change from 0402 0.1uF to 0603 1uF	X01
8	65	Selector	1/8	Compal	For undock shutdown issue.	Add PQ827 and gate connect to SLICE_BAT_PRES#.	X01
9	64	Charger	1/8	Compal	To prevent charger into sleep mode when dual AC transient.	PC707 change from 1uF to 10uF.	X01
10	64	Charger	1/8	Compal	Improve ACAV_IN_NB ref voltage accuracy.	PR733 connect to +3.3V_ALW2. PR740 change from 12K to 10K PR733 change from 130k to 48.8k	X01
11	61	VCC_CORE	1/8	Intersil	Fine tune IMON, OCP, Iout offset.	Add PR558 4.99M on ISUMP to GND. PR535 change from 432 to 499. PR521 change from 95.3k to 97.6k. PC500 change from 0.01u to 1000p	X01
12	62	GPU_CORE	1/8	Compal HW	Change enable signal to DGPU_PWR_EN.	PC600 unpop, PR600 change from 10k to 0 ohm.	X01
13	64	Charger	1/9	Compal	Fine tune ACOK response time.	PC708 change from 0.01uF to 0.1uF	X01
14	56 65	DCIN selector	1/9	Compal	GPIO net - AC_DIS# is high active. Corrent net name.	AC_DIS# cahnge to AC_DIS.	X01
15	64	Charger	1/9	Compal	Improve current sense accuracy.	PR744=44.2ohm PR736=59ohm	X01
16	65	Selector	1/9	Compal	AC_DIS circuit modify to improve output voltage level.	Add PD820, PQ828, PQ829, PR895.	X01
17	59	1.05V_VM	1/11	Compal	Improve output ripple voltage.	Add 10uF(PC310) on output.	X01
18	62	GPU_CORE	1/11	Compal HW	DGPU_PWR_EN# has glitch when entry S3/S4/S5.	DGPU_PWR_EN# change to DGPU_PWR_EN#_Q.	X01
19	56	DCIN	1/14	Compal	To prevent PD2 damage issue, ESD team suggest pin5 connect to VCC.	PD2 pin5 connect to +3.3V_ALW, Add PR27 0 ohm PD2 change from NXP(SC300001100) to AMC(SC300001G00)	X01
20	61	GPU_CORE	1/15	AMD	Add GPU_VID_4.	Add GPU_VID_4 and 0ohm PR620.	X01
21	64	Charger	1/17	Compal	Adapter protect from rating+0.75A to 2A.	PR730 change from 150k to 249k PR731 change from 66.5K to 162K unpop PR727	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37, 45, 46	HW	12/10/2012	Compal	Change R-Pak package.	Change RP3,RP4,RP5,RP6,RP9,RP13 P/N to SD309100380 (Change Package from 1206 to 0804)	X01
2	46	HW	12/10/2012	Compal	Change R-Pak package.	Change RP8 P/N to SD309470180 (Change Package from 1206 to 0804)	X01
3	35	HW	12/10/2012	Compal	Change New TPM Chip	Change U39 P/N to SA00004WQ40 (AT97SC3204-DX4A12-ABF)	X01
4	28	HW	12/18/2012	Compal	Impact SMT DFX stilt and solder risk.	Change JLVDS1 P/N from SP01001BS00 to SP01001BT00	X01
5	20, 35	HW	12/21/2012	DELL	Update GPIO map to rev 3.0C	Reserve PCH GPIO 22 for moving SP_TPM_LPC_EN from OUT65 and add PD 100k(RH332)	X01
6	30	HW	12/21/2012	Compal	Remove non-pop item	Remove R3730	X01
7	46	HW	12/21/2012	DELL	Update GPIO map to rev 3.0C	Add a 0ohm resistor R3772 to short RUNPWROK and AND_PWRGD	X01
8	28	HW	12/21/2012	DELL	ATG droop	Remove ATG config 1@,2@	X01
9	40	HW	12/26/2012	Compal	Support Samsung Galaxy Tab charger in S3.	Change USB charger P/N from SLGC55584AVTR to SLG55594AVTR	X01
10	26	HW	12/27/2012	Compal	Inter-pair skew test issue, PS8401 design change from A3 to A4.	Change HDMI LV Shift P/N from PS8401ATQFN40GTR2-A3 to PS8401ATQFN40GTR2-A4.	X01
11	38	ME	01/02/2013	Compal	JSIM1 BOSS hole update from 3.55mm to 1.7mm.	Change JSIM1 P/N from 159-1000302600 to 159-1000302602	X01
12	47	ME	01/03/2013	Compal	JSF1 pitch change from 0.5mm to 1.0mm	Change JSF1 P/N from A520620-SCHR22 to A090620-SAHR21	X01
13	30	HW	01/03/2013	COMPAL	Follow Realtek recommend circuit	1.Change R1119 ,R1120 to 100K 2.Change R1677 R1679 to 9.1 ohm 3.Change C958,C960 from 0603 to 0805	X01
14	28	HW	01/04/2013	COMPAL	Import U148 of 2nd source	U148 pin4 connect to +3.3V_ALW and remove C33	X01
15	15, 17, 18, 20, 46	HW	01/04/2013	COMPAL	Import R-Pak	R820,R818,R829,R822 change to RP14 R1125,R810,R1156,R819 change to RP15 R814,R920,R870,R876 change to RP16 RH168,RH329,RH125 change to RPH18 R799,R835,R892,R869 change to RP17 RH138,RH136,RH257,RH201 change to RPH19 RH133,RH141,RH143,RH36 change to RPH20 RH122,RH166,RH171,RH217 change to RPH21 R1183,R513,R510,R775 change to RP18 R514,R767,R3,R805 change to RP19 R728,R739,R737,R716 change to RP20	X01
16	46	HW	01/07/2013	COMPAL	Change Board ID from X00 to X01	Change R875 from 240K to 130K	X01
 DELL CONFIDENTIAL/PROPRIETARY Compal Electronics, Inc. Title EE P.I.R (1/2) Size Document Number LA-9934P Date: Wednesday, May 07, 2014 Sheet 69 of 71							PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT. Rev 1.0

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
17	30	HW	01/08/2013	Compal	Follow EMI request	Change 0 ohm to 33 ohm bead for internal SPK (L702~L705)	X01
18	17, 33, 46, 50	HW	01/08/2013	Compal	Follow Crystal EA result.	Change C470,471 from 33pF to 27pF Change CH13,CH14 from 18pF to 12pF Change C743,C741 from 22pF to 27pF Change CV94,CV95 from 10pF to 6.8pF	X01
19	7, 16	HW	01/11/2013	Compal	Follow ESD result.	Change RC35 from 0ohm to 0ohm short Pop RC52 1K Add C1553 0.047u Add C1554 0.047u	X01
20	46	HW	01/11/2013	Compal	Follow EMI result.	Add C1555 0.047u	X01
21	28	HW	01/14/2013	Compal	To avoid +3.3V Camera inrush	De-populate C300 10U_0805 CAP	X01
22	27	HW	01/15/2013	Compal	The RTD2136R ripple is better than S version. The cap can be use small.	Change C109 from 22uF to 10uF.	X01
23	50	HW	01/16/2013	Compal	As Sun PowerPlay Clock PA request, Sun-XT VDDC range from 0.925 to 1.150V, so extra VDDC_VID4 is needed	Add GPU_VID_4 to control ~ 1.150V	X01
24	7	HW	03/11/2013	Compal	Follow Intel DG Rev.1.5	Change RC12 from 10k to 100k.	X01
25	6~45	HW	04/01/2013	Compal	For Vender recommend circuit	Change 0 ohm resistor to short pad Change Q63,QV1 P/N from SB00000RV00 to SB00000ZN00 Change L77 P/N from SM010022010 to SM01000M000	X02
26	27	HW	04/01/2013	Compal	Follow Realtek recommend circuit	L60,L61,L62 change to R3881,R3882,R3883(Short 0ohm)	X02
27	39	HW	04/01/2013	Dell	Dell don't want EXP@ config on MB.	Remove EXP@ config	X02
28	26	HW	04/01/2013	Compal	Follow HDMI EA result. Change repeter setting.	Pop R86	X02
29	24	HW	04/01/2013	Compal	Follow Icon Brightness result. Change LED resistance.	R955 from 1.8k to 680 ohm R938 from 1.8k to 680 ohm R958 from 620 to 680 ohm R934 from 1K to 1.8k ohm R3671 from 1.4k to 1.8k ohm R949 from 680 to 1.8k ohm	X02
30	36	HW	04/01/2013	Compal	OZ777FJ2 enters into test mode unexpectedly with SD card inserted incompletely.	Add R3884 1M ohm to GND on SD_CD#	X02
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
31	15~23, 33	HW	04/01/2013	Compal	Intel ChipSet update.	Change PCH C1 version to C2 version. P/N from SA00006P30L to SA00006P33L	X02
32	13, 14, 40	HW	04/01/2013	Compal	Update OSCON P/N for DFX issue	Change 330uF OSCON P/N from SF000002Z00 to SF000003100 (CD14, CD36) Change 220uF OSCON P/N from SF000002Y00 to SF000003000 (C651)	X02
33	7	HW	04/01/2013	Compal	No support CPU XDP JTAG PU/PD issue	Pop RC59, RC62, RH52 for Intel recommend	X02
34	50	HW	04/01/2013	Compal	GPU_HOT# voltage issue	Change RV103 from 100k to 4.7k for AMD recommend	X02
35	46	HW	04/01/2013	COMPAL	Change Board ID from X01 to X02	Change R875 from 130K to 33K	X02
36	37	HW	04/08/2013	COMPAL	Schematic synchronous	Change R725 PU Net from WIGIG60GHZ_DIS# to WIGIG60GHZ_DIS#_R Add R3885 to WLAN_RADIO_DIS#_R Add R3886 to BT_RADIO_DIS#_R	X02
37	30, 24	HW	04/11/2013	COMPAL	Sleeve / Ring2 have EMI noise.	Add L706, L707 (BLM15BD601SN1D) Add C1556, C1557 (100pF) H20 connect from GND to NC for ESD request. (EMI AGND and DGND noise)	X02
38	7, 16, 32	HW	04/19/2013	COMPAL	The system running DVD will hand when doing ESD test.	Add C1559 47nF cap on SPKR Add C1558 47nF cap on POWER_SW#_MB Pop C1553	X02
39	35	HW	04/23/2013	COMPAL	TPM Chip Update.	Change TMP version from DX4A12 to X4A12. P/N from SA00004WQ40 to SA00004WQ50	X02
37	15~23, 33, 49~55	HW	06/04/2013	COMPAL	Change chip P/N to R3	Change PCH from R1 to R3. P/N from SA00006P33L to SA00006P35L Change PHY from R1 to R3. P/N from SA00005003L to SA00005005L Change GPU from R1 to R3. P/N from SA00006ES0L to SA00006ES1L Change VRAM from R1 to R3. P/N from SA00006EU0L to SA00006EU1L	A00
38	46	HW	06/04/2013	COMPAL	Change Board ID from X02 to A00	Change R875 from 33K to 1K	A00
39	18	HW	06/04/2013	COMPAL	Change 0 0hm to short 0 ohm	Change RH177, RH178, RH179, RH181, RH182, RH183, RH184, RH185 to short 0 ohm	A00

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EE P.I.R (2/2)

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