Compal Confidential

Diner Braswell M/B LA-D702P Schematics Document

Intel Braswell + ATI R16M-M1-30/70

2015/12/12

Project Code : BDL50

Rev. 0.3 PV

Security Classification	Compal Secret Data		
Issued Date	2015/10/05	Deciphered Date	2015/10/05

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Title: *Cover Page*

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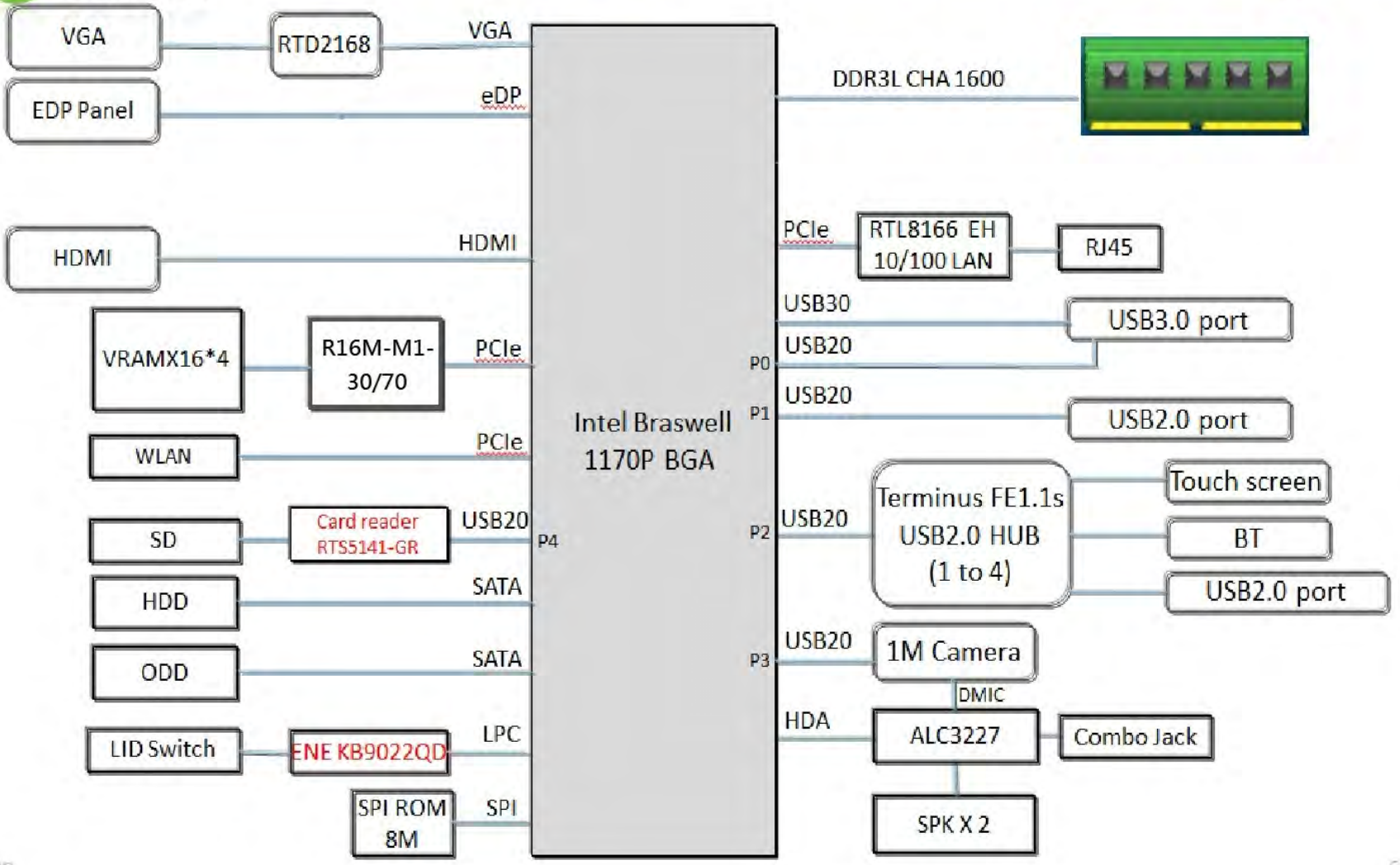
Intel Braswell 15” Hardware Block Diagram



Sub-borad

page34
CR+USB/B

page34
PWR BTN/B

page36
TP BTN/B

page24
HDD or SSD/B

page24
ODD/B

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Issued Date	2014/07/07	Deciphered Date 2015/07/07	Title: Block Diagrams
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			Date: Thursday, January 07, 2016; Sheet 2 of 50

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.2VALW	+1.2v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

<PCI-E,SATA,USB3.0>

Lane#	USB3.0	DESTINATION	
		UMA	DIS
0		USB3.0	USB3.0
1			

Lane#	SATA	DESTINATION	
		UMA	DIS
0		HDD	HDD
1		ODD	ODD

Lane#	PCIE	DESTINATION	
		UMA	DIS
0			GPU
1			GPU
2		WLAN	WLAN
3		LAN	LAN

<USB2.0 port>

USB2.0 port	UMA	Dis
0	USB 3.0 (MB)	USB 3.0 (MB)
1	USB 2.0 (MB)	USB 2.0 (MB)
2	Camera	Camera
3	Card Reader	Card Reader
4	USB 2.0 Hub	USB 2.0 Hub

<USB2.0 Hub>

USB2.0 port	UMA	Dis
0	Touch Screen	Touch Screen
1	USB 2.0 (SB)	USB 2.0 (SB)
2	BT	BT
3		
4		

EC SM Bus1 address

Device	Address
Charger	
Battery	

EC SM Bus2 address

CPU Thermal Sensor	4C	UC3
ATI GPU EXO Pro		U666

EC SM Bus3 address

GPU Thermal Sensor	4C	UV1

SOC SM Bus address

Device	Address	
ChannelA	A0	DDR DIMM1
ChannelB	A2	DDR DIMM2
Touch Pad		

BOM Structure Table

BOM Config	Description
@	Unpop
CONN@	Connector Part Control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD unpop component
PX@	For Discrete Sku
8166@	10/100 LAN
8151@	Giga LAN
UMA@	For UMA Sku
NAT@	EC Non Auto Load Code
AUTO@	EC Auto Load Code
TPM@	CPU to EC LPC use 3.3V level
NTPM@	CPU to EC LPC use 1.8V level
GCLK@	Pop Green Clock
GCUMA@	Pop Green Clock UMA
GCDIS@	Pop Green Clock DIS
XTAL@	For XTAL
TS@	Pop Touch Screen component
R30@	For R16M-M1-30 GPU
R70@	For R16M-M1-70 GPU
6U@	For 6U@ (Add CRT Component)
IND@	Pop for India Sku

DAX

PCB
Part Number = DA6001JC000
PCB LA-C811P REV0 M/B 4

ZZZ1

HDMI
Part Number = RO0000003HM
PCB 102 LA-B151P REV0 M/B 3
45@

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Issued Date	2014/07/07	Deciphered Date 2015/07/07	Title Notes List

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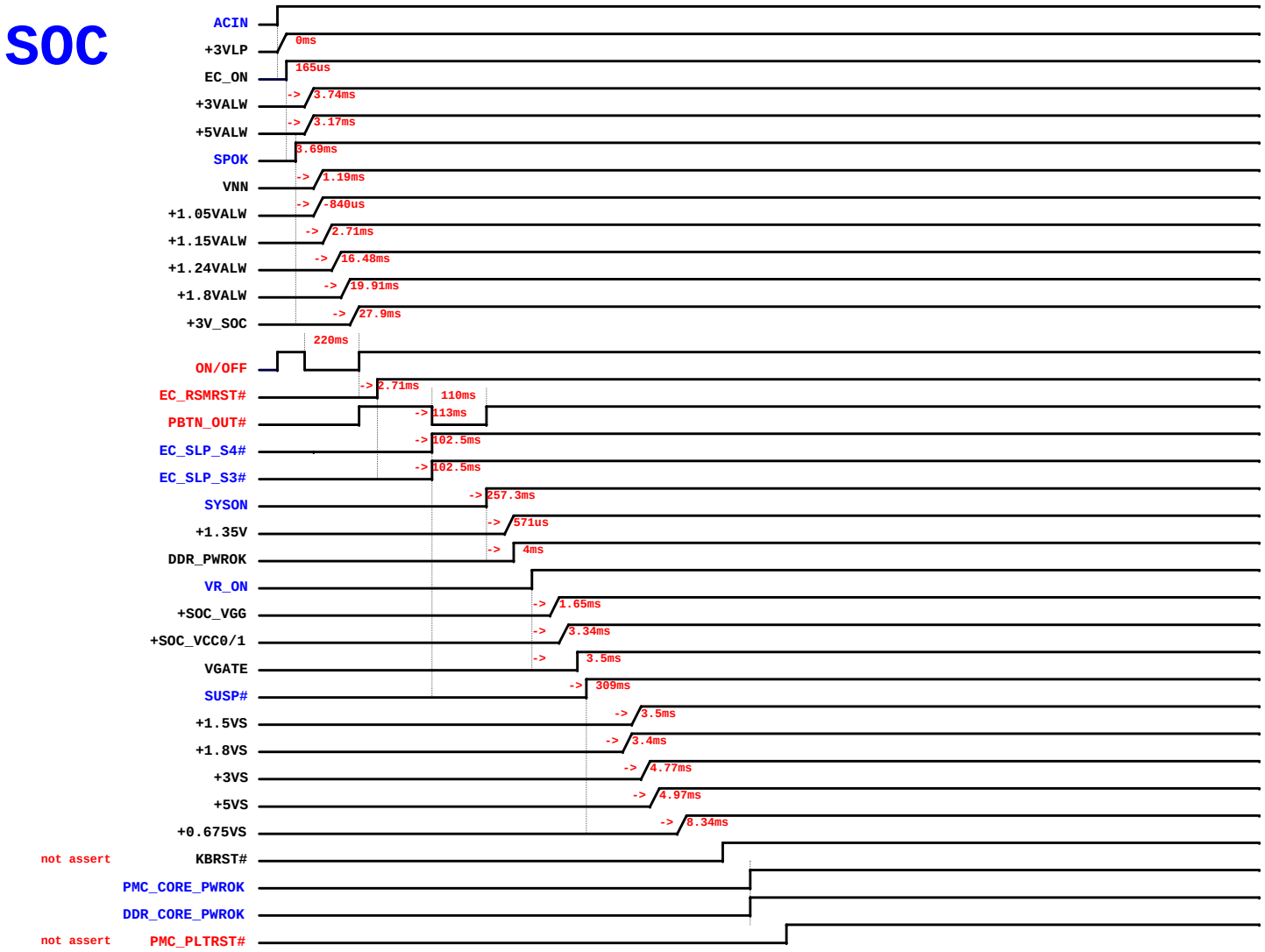
G3->S0



Dr-Bios.com

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Issued Date	2014/08/21	Deciphered Date	2015/08/21	Title: Power Sequence

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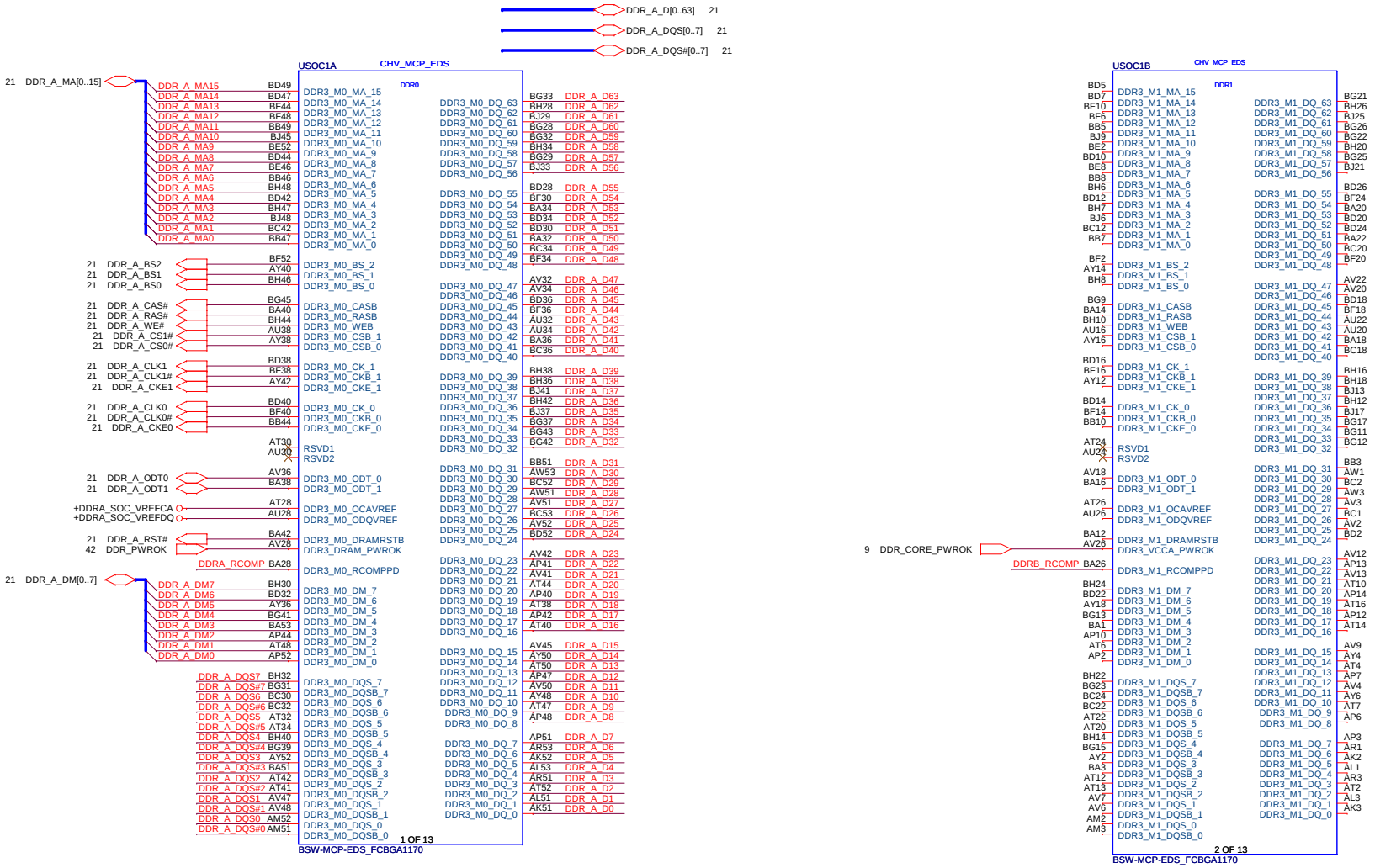

Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

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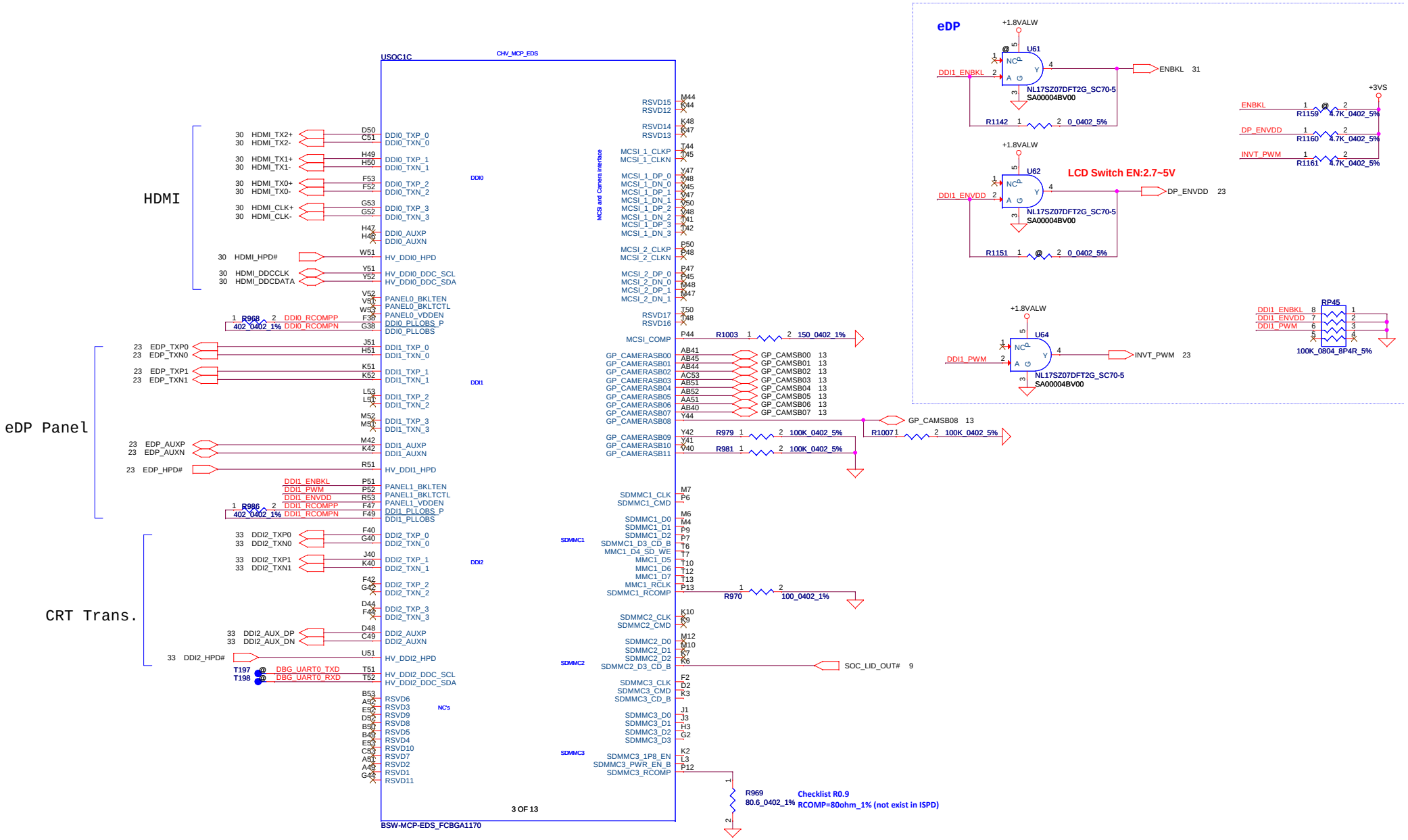
Title: **VLV-M SOC Memory DDR3L**

Size: Custom | Document Number: **LA-706P** | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 5 of 50



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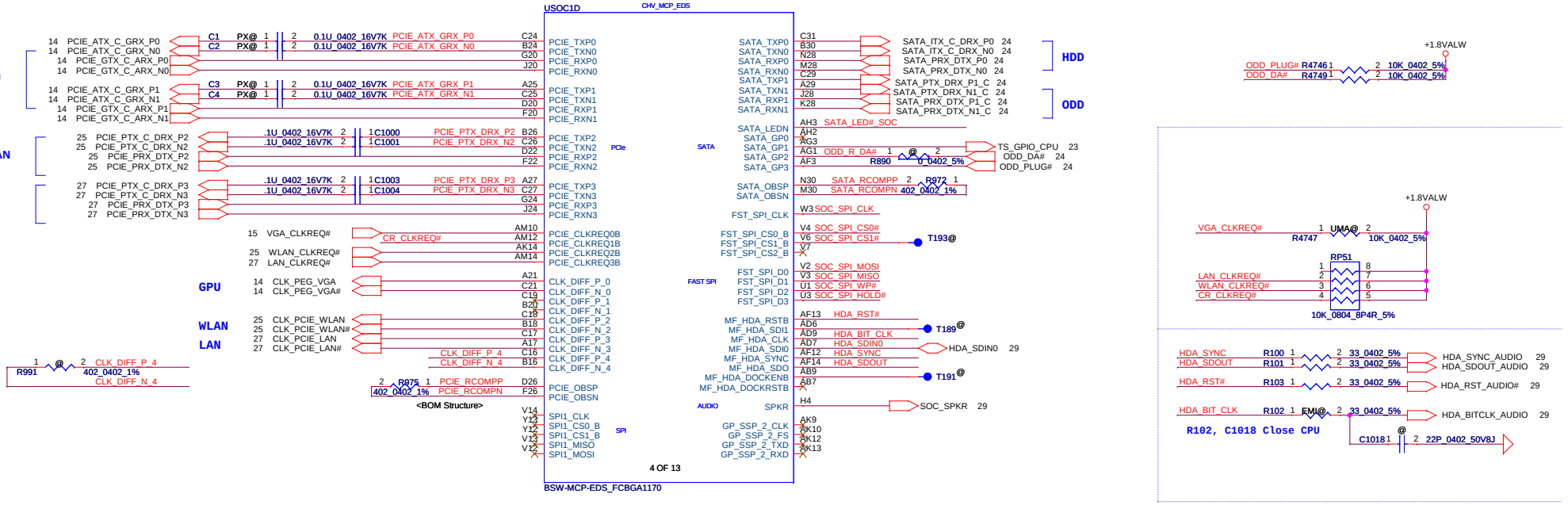

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Issued Date	2014/08/21	Deciphered Date	2015/08/21	Title: VLV-M SOC SATA/PCI-E/HDA
				Size: Custom; Document Number: LA-706P; Rev: 0.1
				Date: Thursday, January 07, 2016; Sheet 7 of 50

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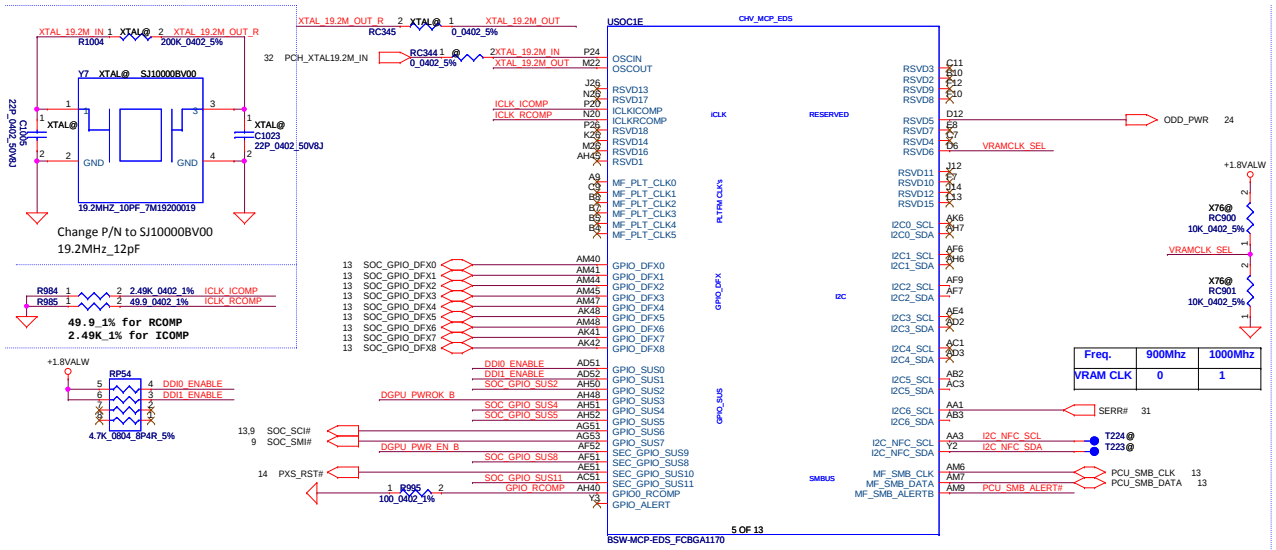
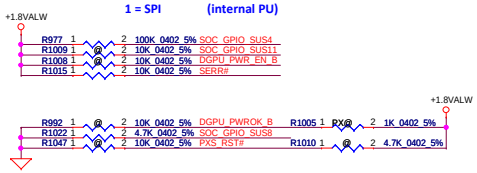
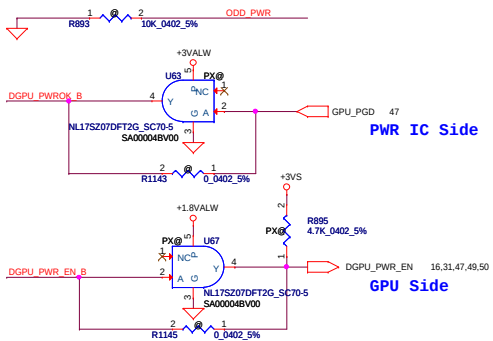


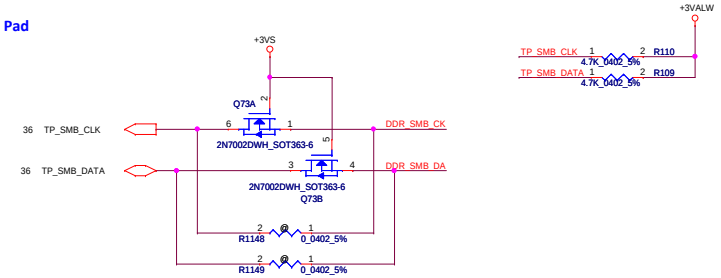
Freq.	900Mhz	1000Mhz
VRAM CLK	0	1

SOC_GPIO_SUS4:
BIOS Boot Selection
0 = LPC
1 = SPI (internal PU)



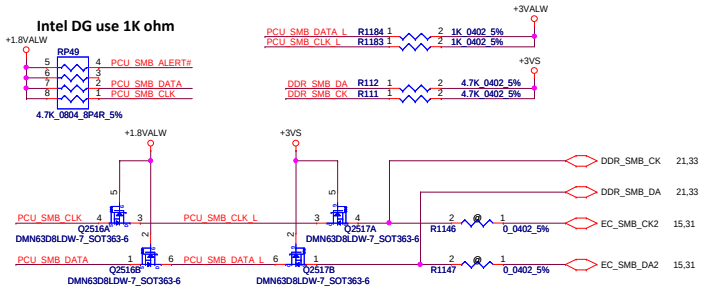


Touch Pad



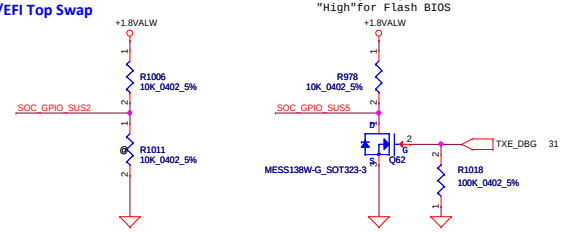
Hardware Strap				
Pin Name	**Purpose**	**PU/PD**	**Description**	**Default State**
GPIO_SUS0	DDI0 Detect	PU	1: DDI0 detected 0: DDI0 not detected	High
GPIO_SUS1	DDI1 Detect	PU	1: DDI1 detected 0: DDI1 not detected	High
GPIO_SUS2	A16 swap overdrive	PU	1: Normal operation 0: Change Boot Loader address	High
GPIO_SUS3	DSI Display Detect	NC	1: DSI detected 0: DSI not detected	Low
GPIO_SUS4	Boot BIOS Strap BBS	PU	1: Boot from SPI 0: Boot from LPC	High
GPIO_SUS5	Flash Descriptor Security Override	PU	1: Security enabled 0: Security disabled	High
GPIO_SUS6	DFX Boot Halt Strap, VISA Early POSM Debug Enable	PU	1: Normal operation 0: Halt boot enable	High
GPIO_SUS7	DFX Sus Debug Strap	PU	1: Normal operation 0: Sus Debug enabled	High
SEC_GPIO_SUS8	ICLK, USB2, DDI SFR Supply Select	PD	1: 1.35V supply 0: 1.25V supply	Low
SEC_GPIO_SUS9	ICLK, USB2, DDI SFR Bypass	NC	1: Bypass with 1.05V 0: No bypass	Low
SEC_GPIO_SUS10	POSM Select	NC	1: PMC 0: Fuse controller	Don't care, if GPIO_SUS6 is pulled high
GP_CAMERASB08	ICLK Xtal OSC Bypass	PD	1: Bypass 0: No bypass	Low
GP_CAMERASB09	CCU SUS RO Bypass	PD	1: Bypass 0: No bypass	Low
GP_CAMERASB11	RTC OSC Bypass	PD	1: Bypass 0: No bypass	Low

Intel DG use 1K ohm



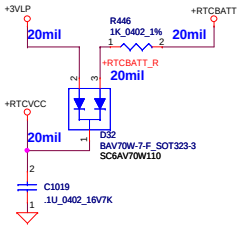
Q2516 change to SB000016K00
Vgs = 0.8V~1.1V

BIOS/EFI Top Swap

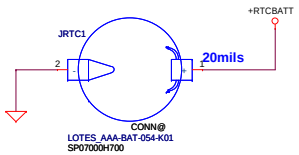


SOC_GPIO_SUS2: Top Swap(A16 Override)
0 = Change Boot Loader address
1 = Normal Operation
Reference EDS0.8 Page 73 (Internal PU)

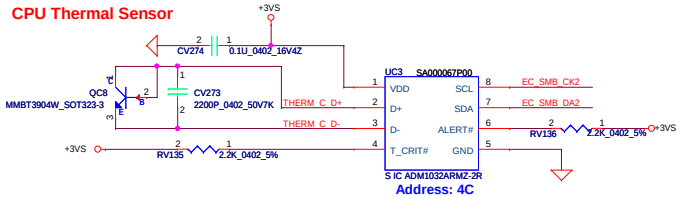
SOC_GPIO_SUS5:
Security Flash Descriptors
0 = Override
1 = Normal Operation (Internal PU)



11/18 RTC BAT conn



QC8/CV273 Place CPU TOP Side
CPU Thermal Sensor



Address: 4C

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Title: **VLV-M SOC CLK/PMU/SPI**

Size: C | Document Number: **LA-706P** | Rev: 0.1

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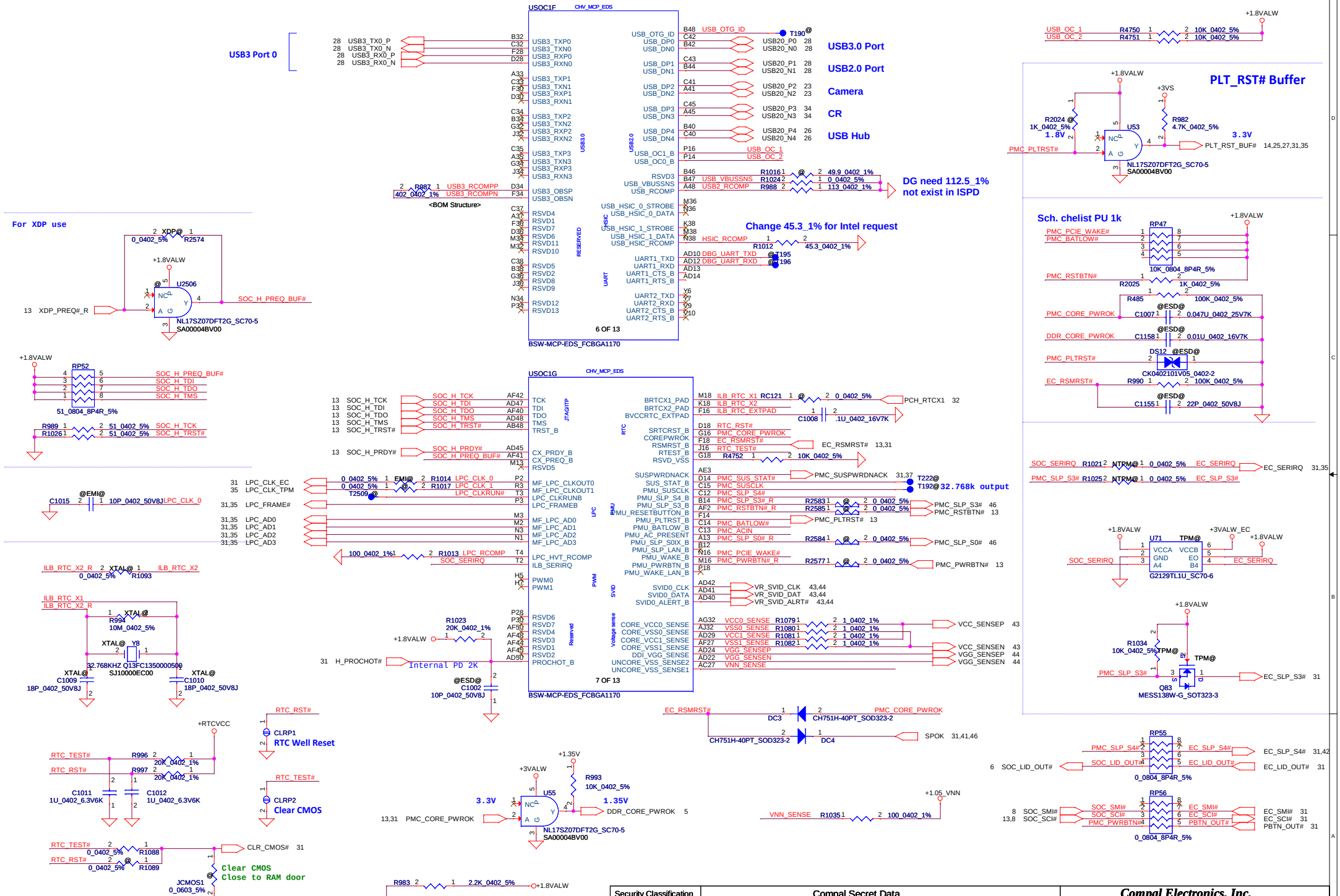

PDG v0.9 page291 : RTC_RST# -
When asserted, this signal resets register bits in the RTC well.

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Title: VLV-M SOC USB/LPC/SMBus

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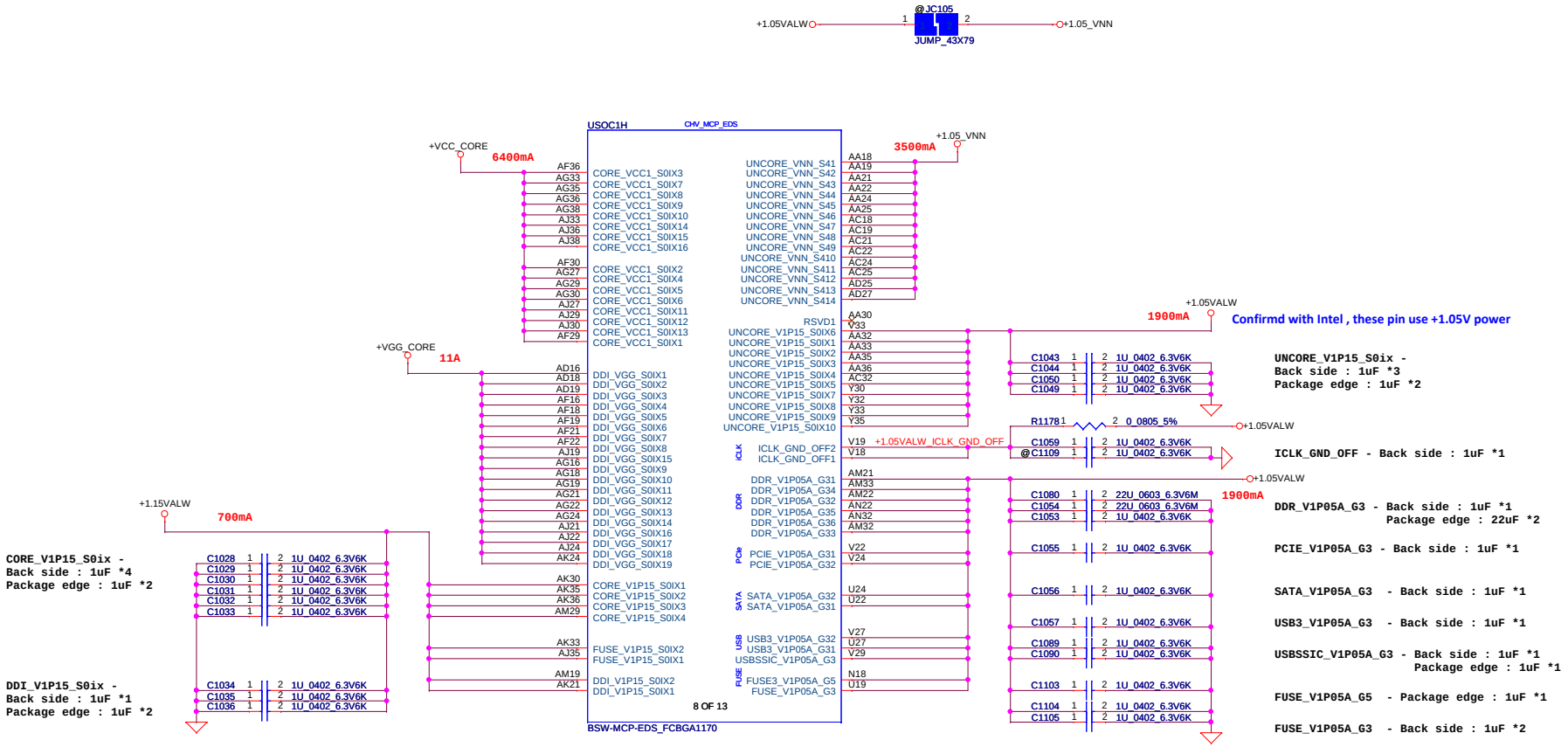

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Title: **VLV-M SOC Power**

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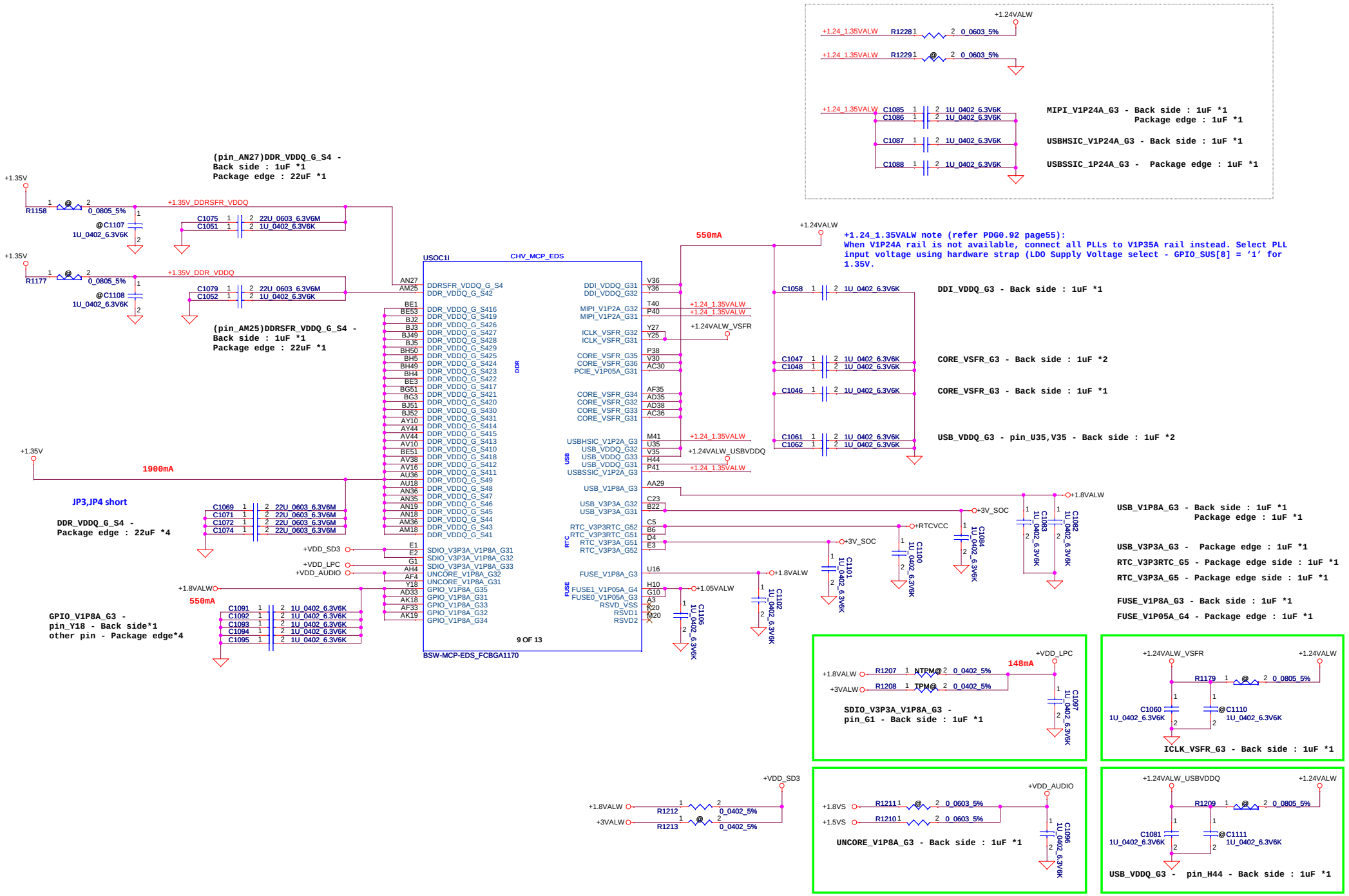

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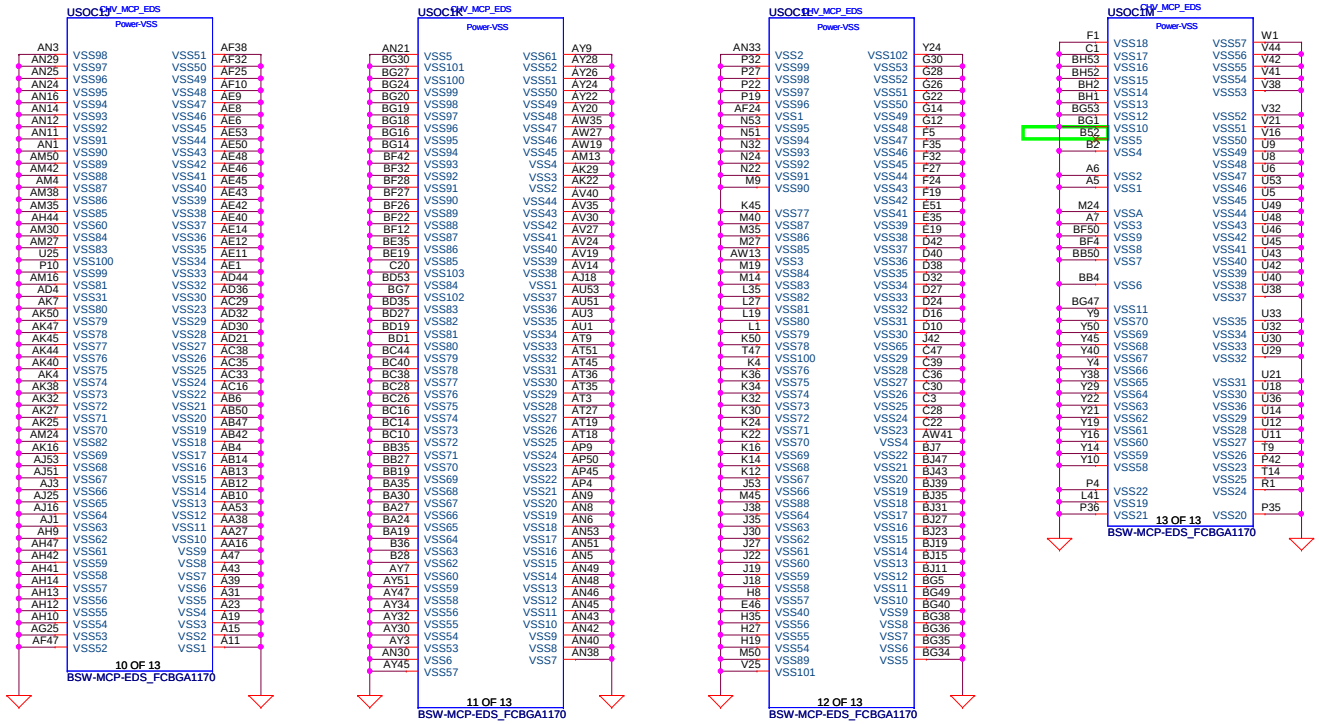

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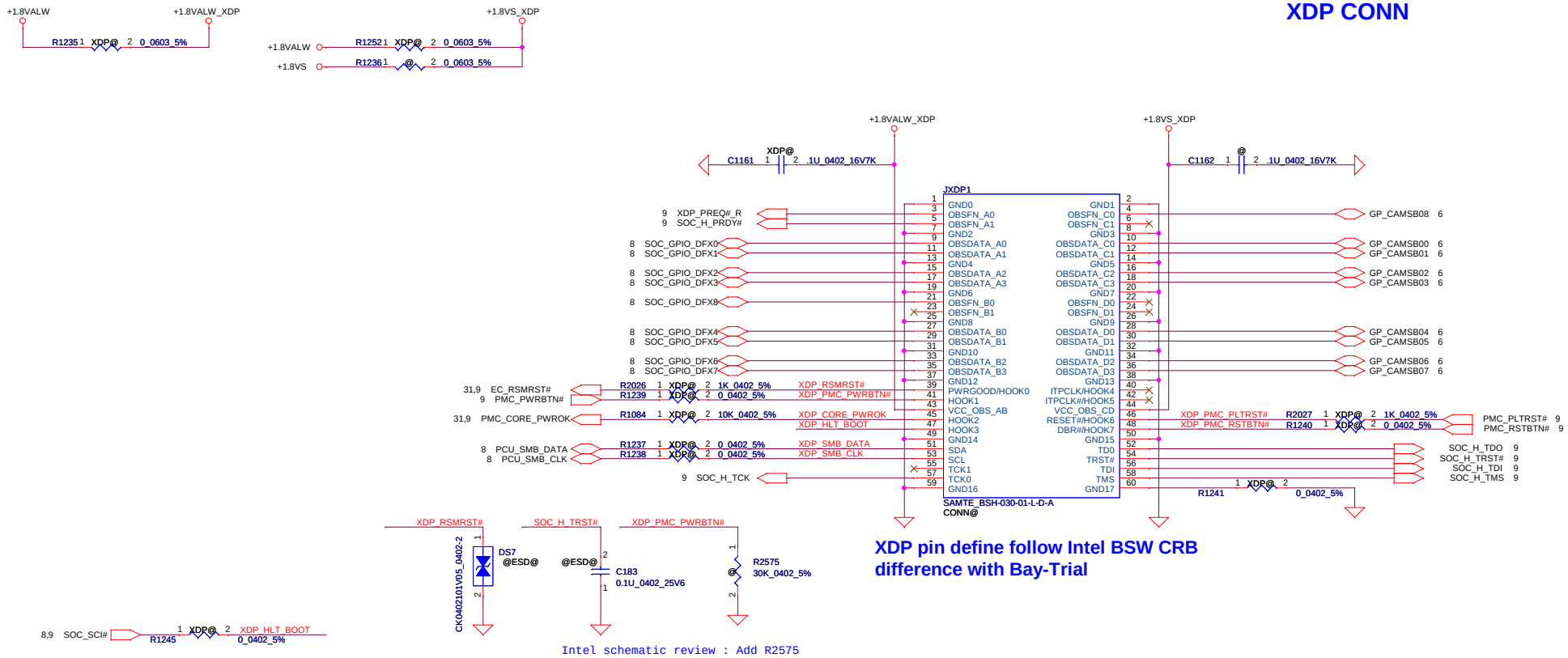
APS CONN

XDP CONN



XDP pin define follow Intel BSW CRB difference with Bay-Trial

Intel schematic review : Add R2575

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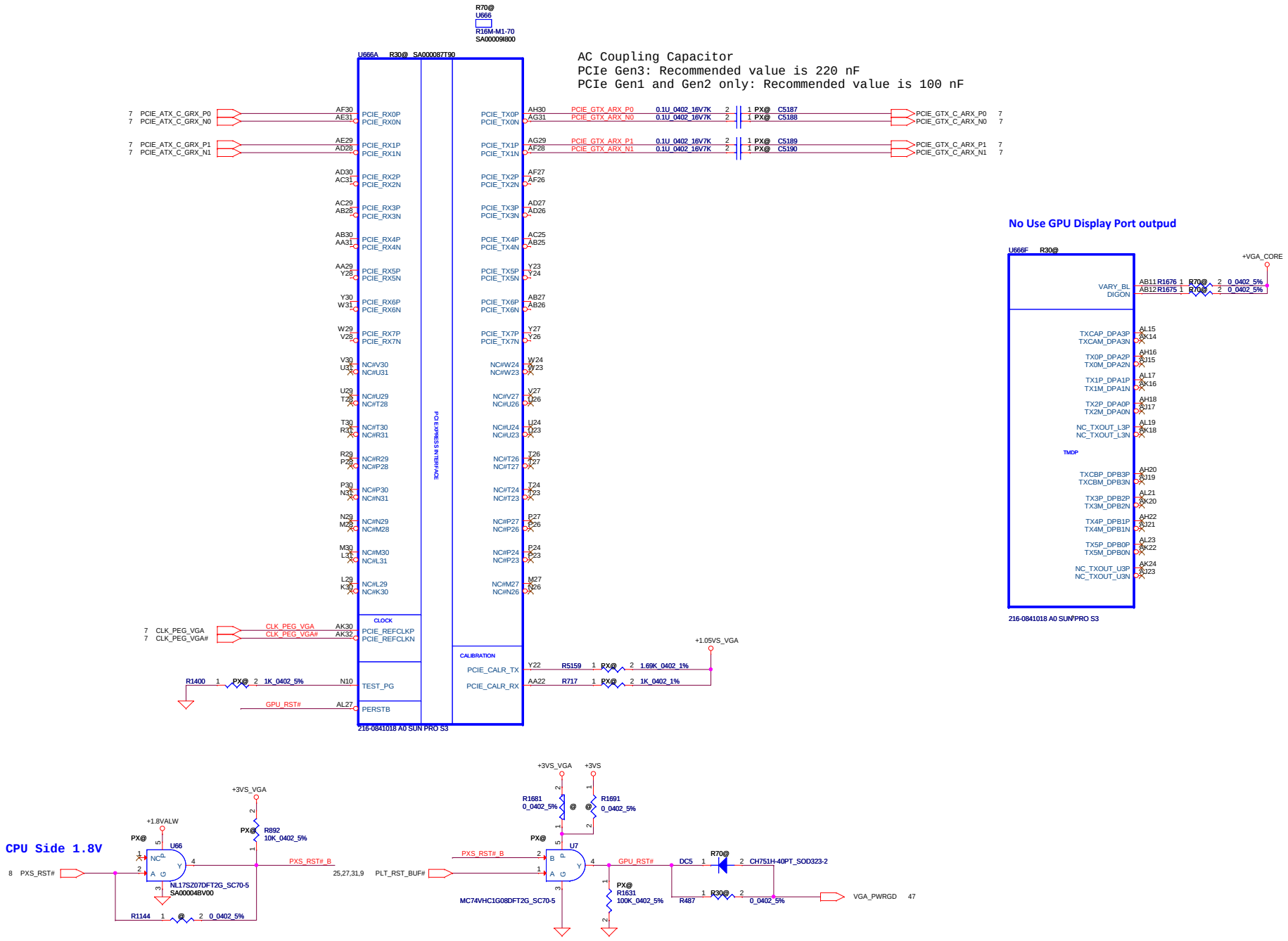
Title: **BDW MCP(1/11) DDI,MSIC,XDP**

Size: Custom | Document Number: **LA-706P** | Rev: 0.3

Date: Thursday, January 07, 2016 | Sheet 13 of 50



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Title: **SUN_PCIE/DP**

Size: Custom | Document Number: **LA-706P** | Rev: 0.1

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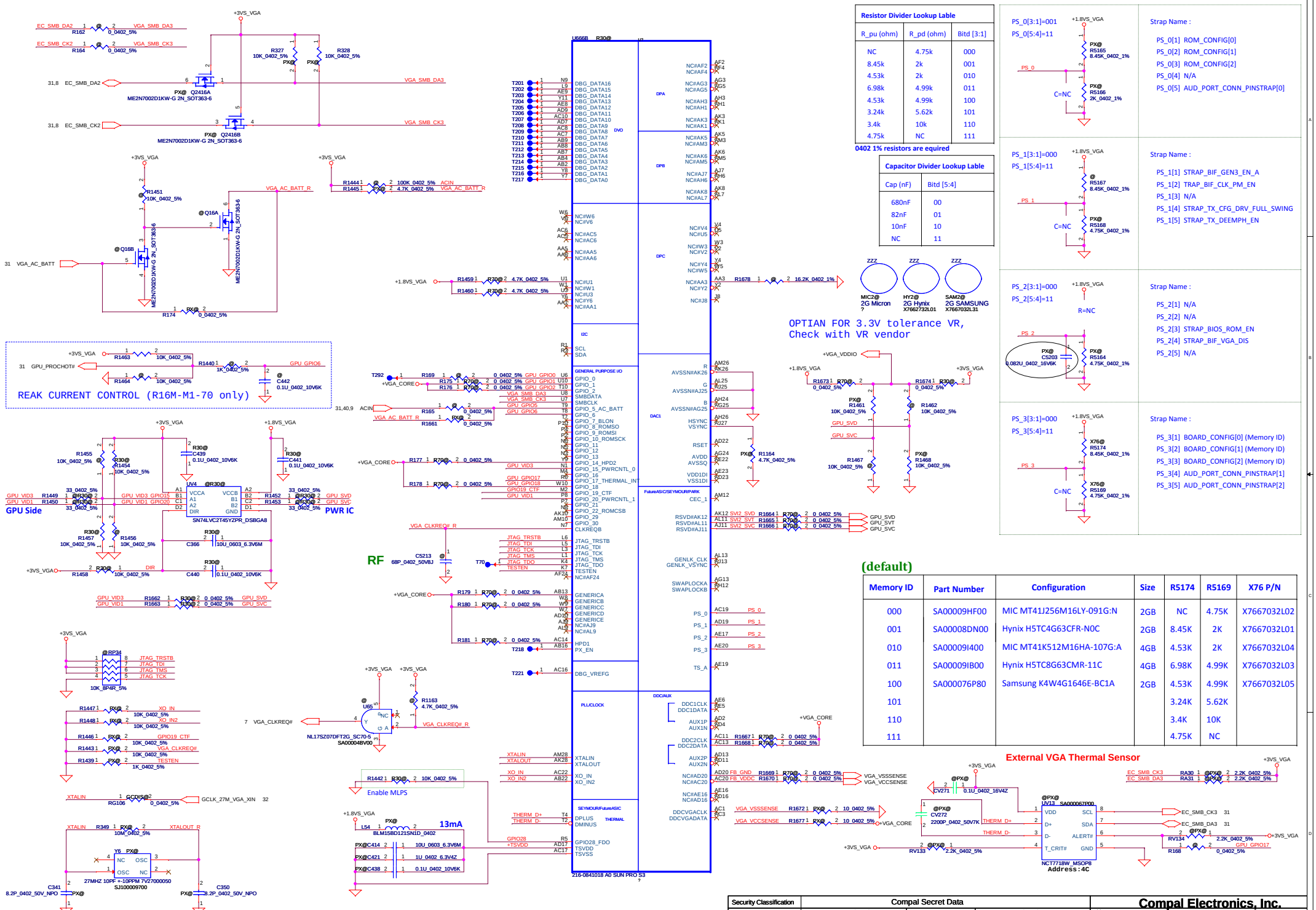

Resistor Divider Lookup Lable

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

(default)

Memory ID	Part Number	Configuration	Size	R5174	R5169	X76 P/N
000	SA00009HF00	MIC MT41J256M16LY-091G:N	2GB	NC	4.75K	X7667032L02
001	SA00008DN00	Hynix H5TC4G63CFR-N0C	2GB	8.45K	2K	X7667032L01
010	SA00009I400	MIC MT41K512M16HA-107G:A	4GB	4.53K	2K	X7667032L04
011	SA00009IB00	Hynix H5TC8G63CMR-11C	4GB	6.98K	4.99K	X7667032L03
100	SA000076P80	Samsung K4W4G1646E-BC1A	2GB	4.53K	4.99K	X7667032L05
101				3.24K	5.62K	
110				3.4K	10K	
111				4.75K	NC	

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Issued Date	2013/01/11	Deciphered Date	2013/12/31

Title: **Compal Electronics, Inc.** SUN_MSIC

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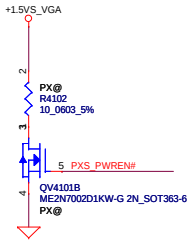
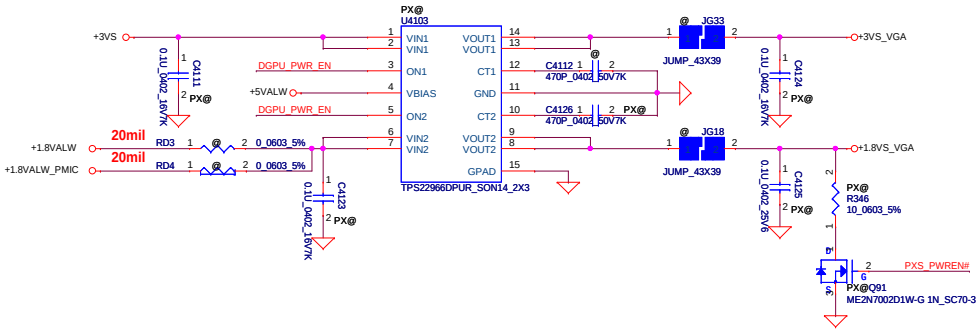
Date: Thursday, January 07, 2016 | Sheet 15 of 50

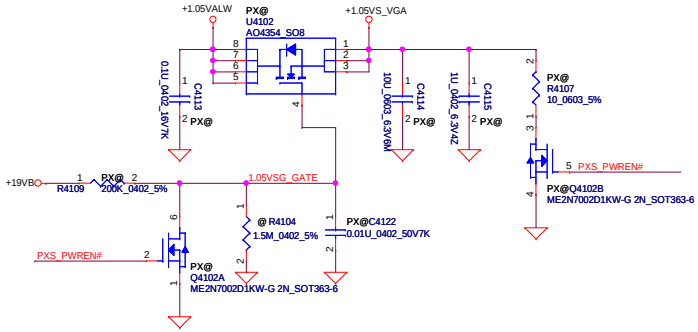
+1.5VS to +1.5VS_VGA (4A)



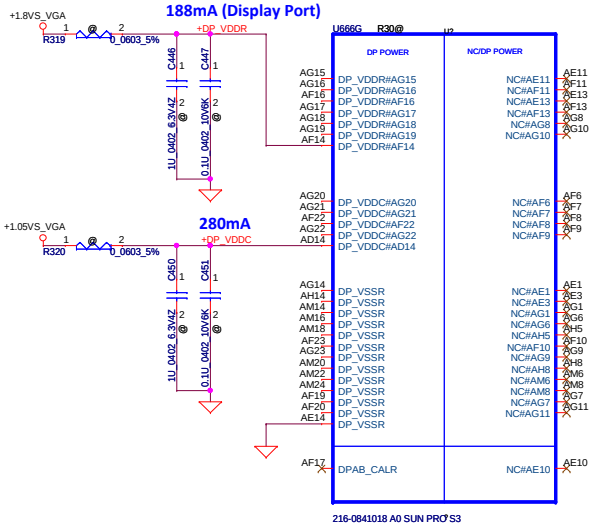
+3VS to +3VS_VGA (25mA)
+1.8VALW to +1.8VS_VGA (331mA)

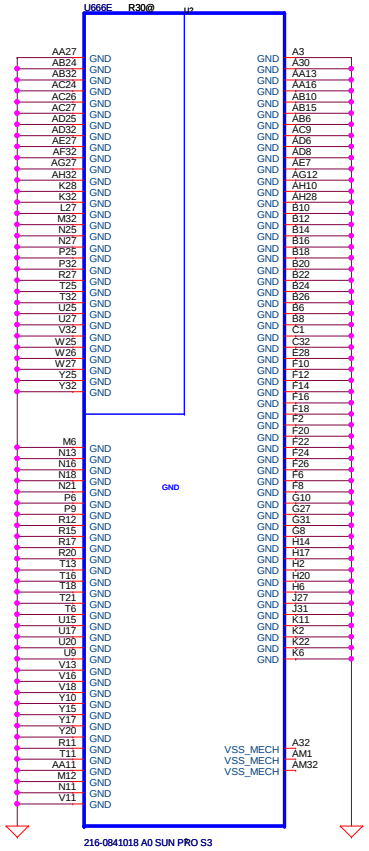


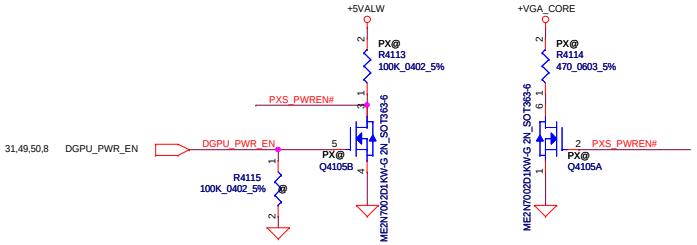
+1.05VALW to +1.05VGA (2A)



370mA (HDMI)
188mA (Display Port)
No Use GPU Display Port outpud







Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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Compal Electronics, Inc.

Title: **SUN_Power/GND**

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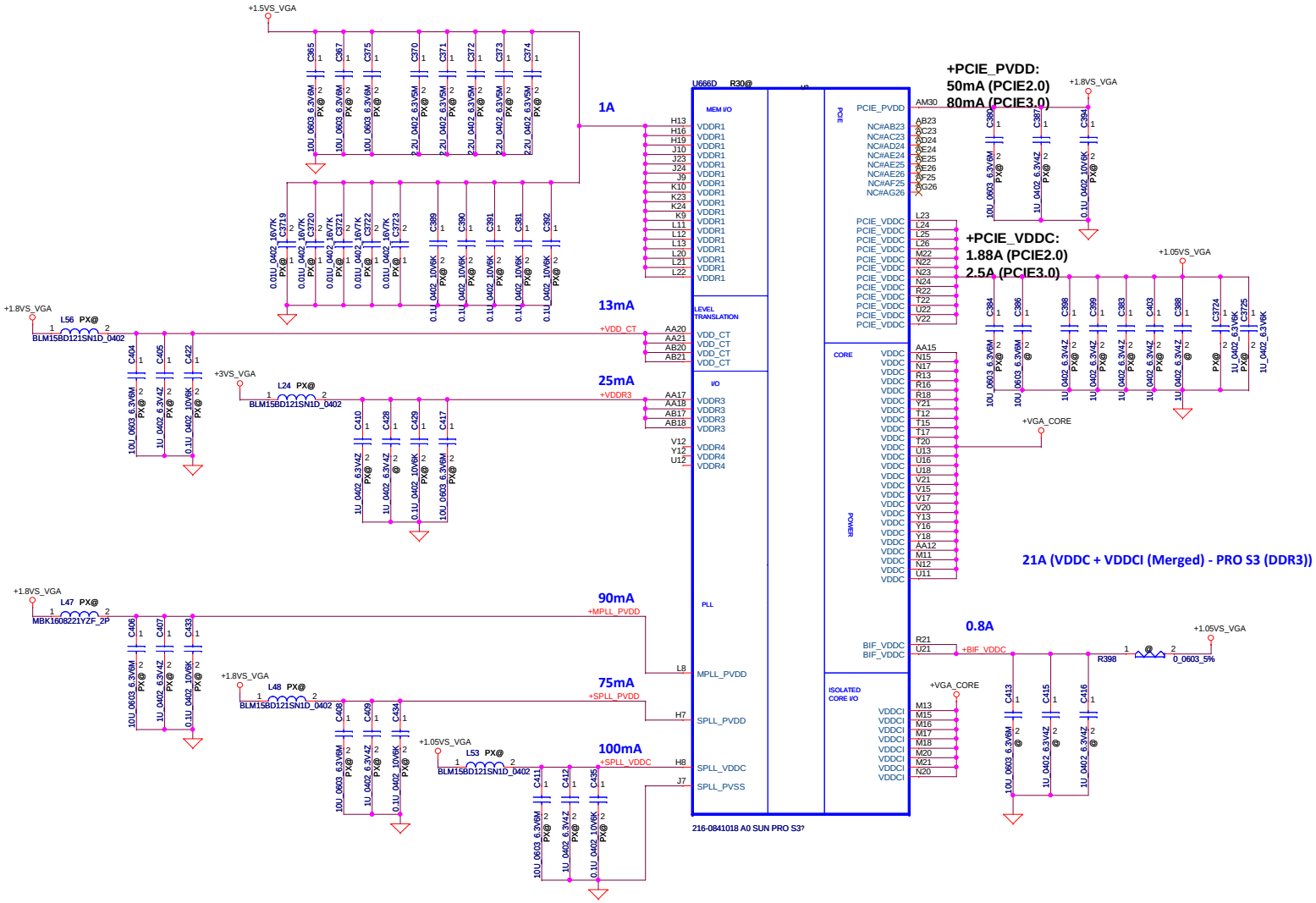
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+0.95VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



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Compal Electronics, Inc.

Title: SUN_Power

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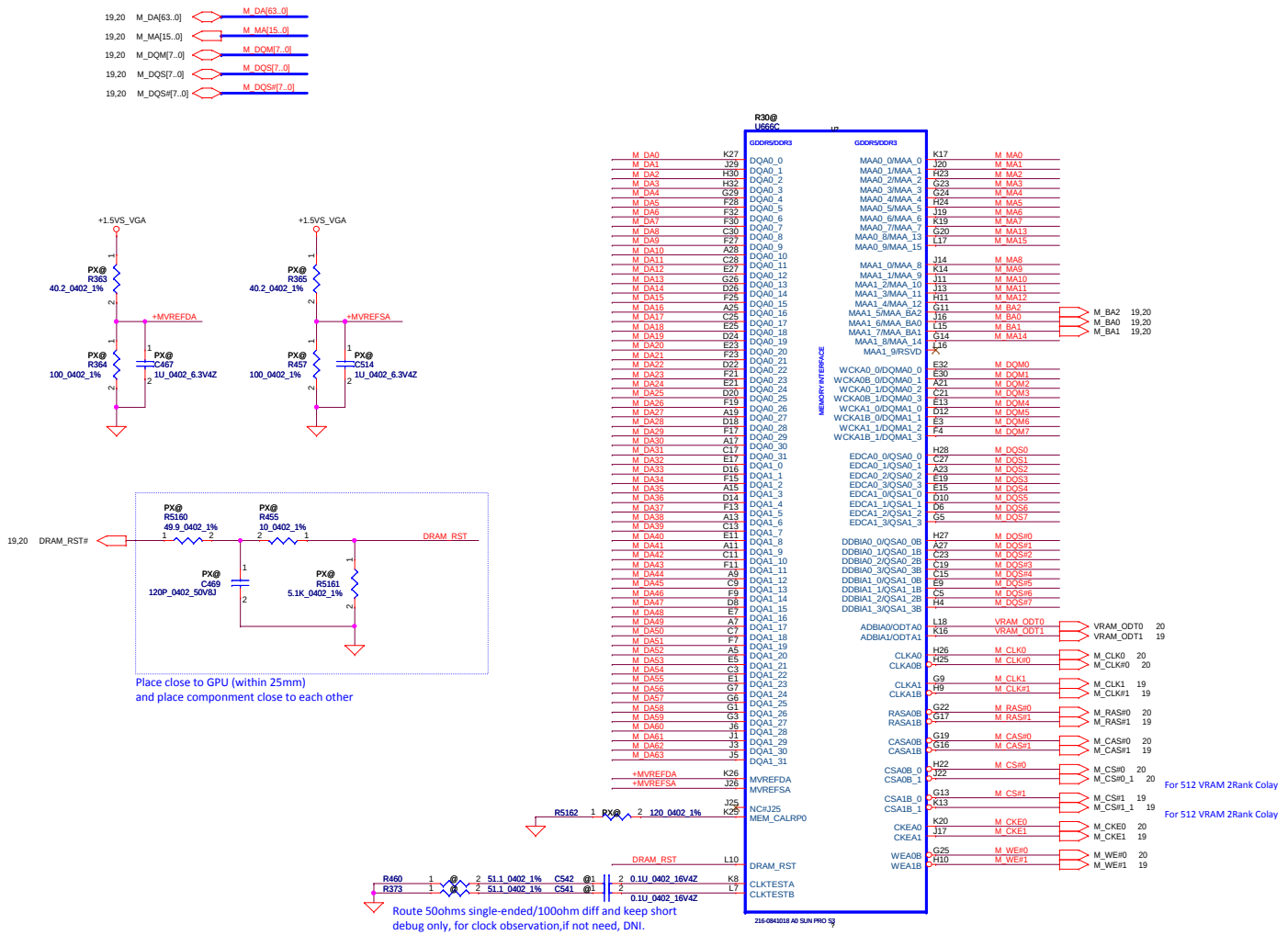

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Issued Date	2013/01/11	Deciphered Date	2013/12/31

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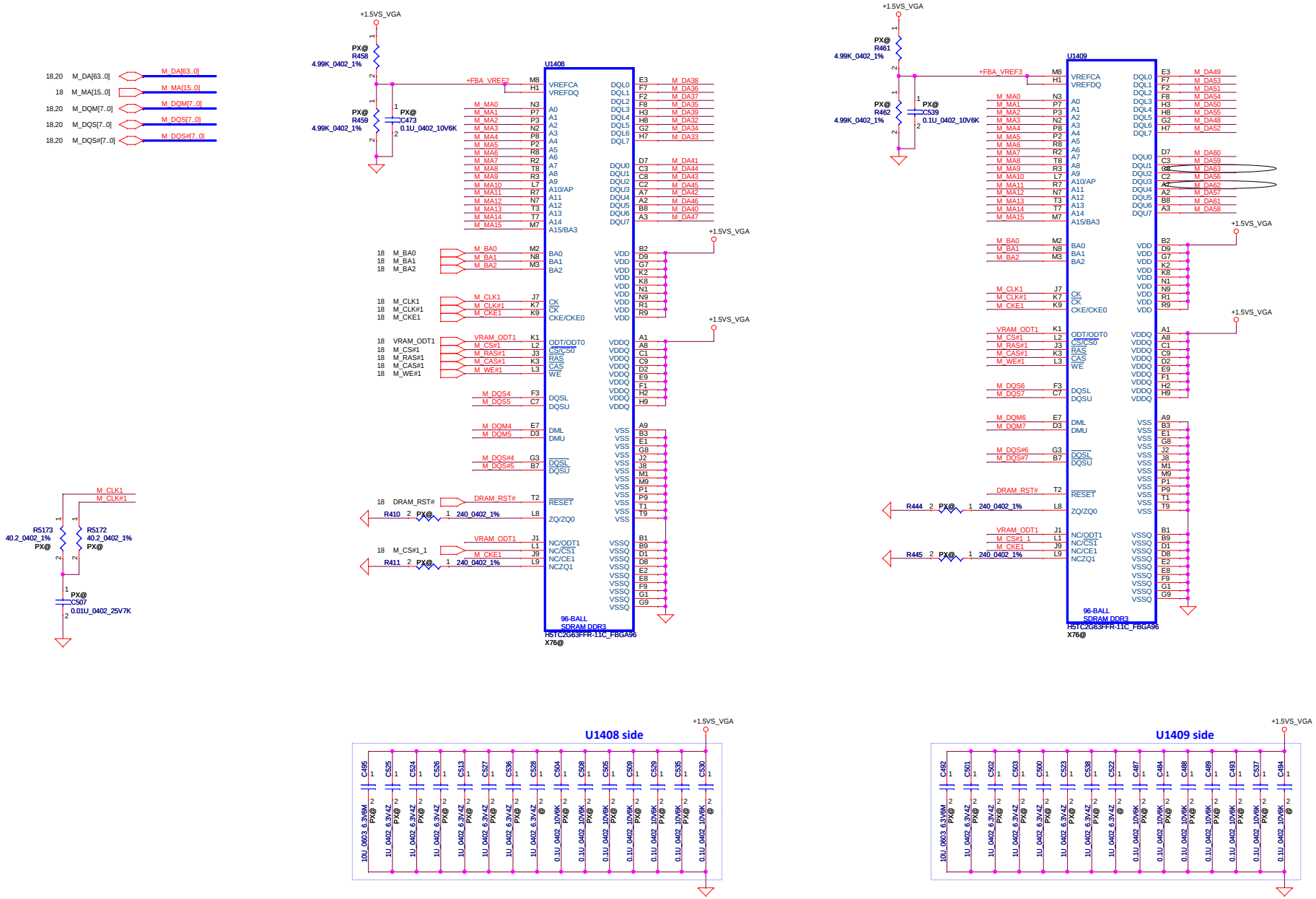
Compal Electronics, Inc.

Title: **SUN_MEM**

Size: C | Document Number: **LA-706P** | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 18 of 50

Memory Partition A - Upper 32 bits



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Issued Date	2013/01/11	Deciphered Date	2013/12/31

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Compal Electronics, Inc.

Title: **SUN_VRAM A Upper**

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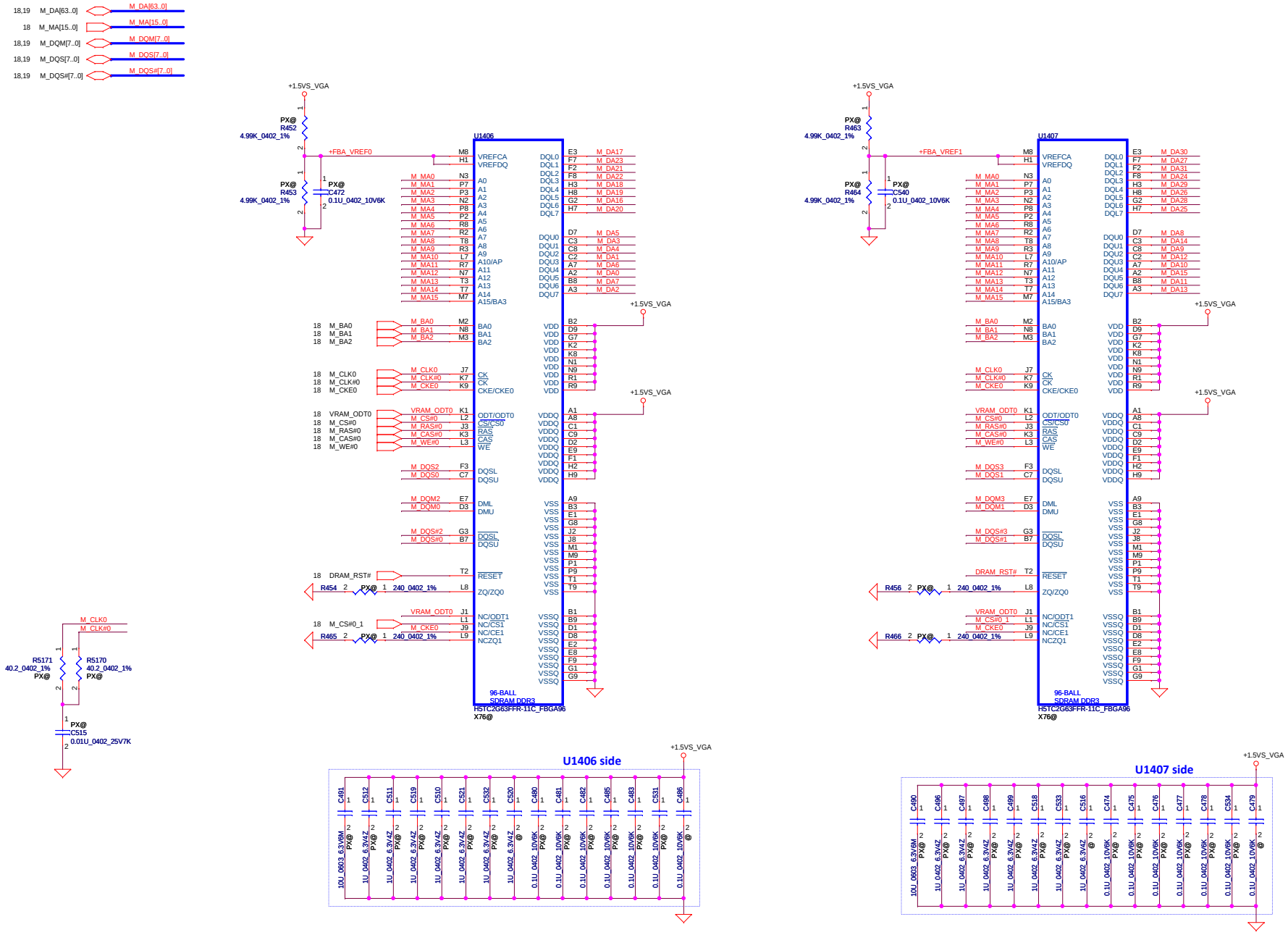
Date: Thursday, January 07, 2016 | Sheet 19 of 50

Memory Partition A - Lower 32 bits



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Issued Date	2013/01/11	Deciphered Date	2013/12/31

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Compal Electronics, Inc.

Title: **SUN_VRAM A Lower**

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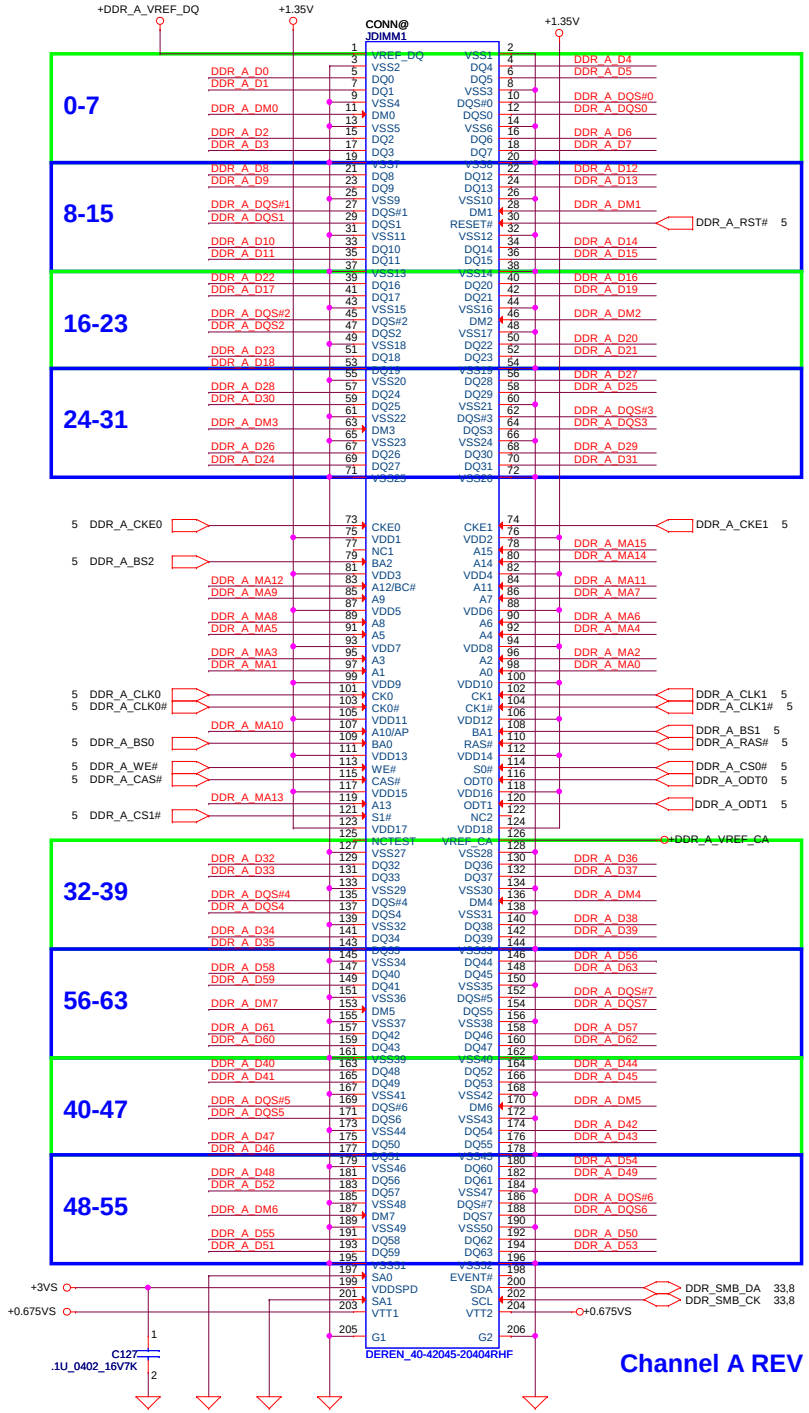


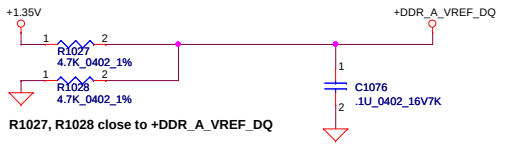
All VREF traces should have 10 mil trace width

Channel A REV

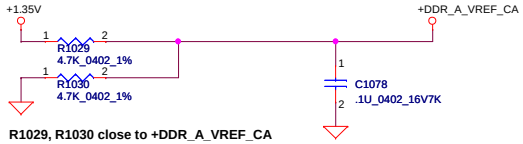
SA1: SA0 = 00
Address: A0h/10100000b

DDR_A_DQS#[0..7] 5
DDR_A_DQS[0..7] 5
DDR_A_D[0..63] 5
DDR_A_MA[0..15] 5
DDR_A_DM[0..7] 5

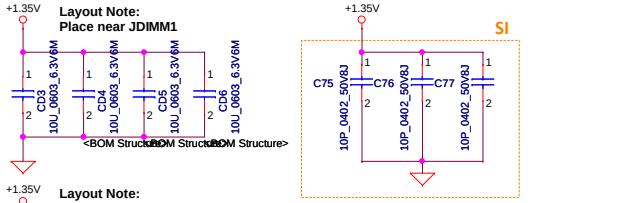
Signal voltage level = 0.675 V
PLACE TWO 4.7K RESISTORS CLOSE TO
DIMMS ON DIMM_VREF_CA / DIMM_VREF_DQ
Decoupling caps are needed; one 0.1 µF placed close to VREF pins of each DDR3 SODIMM.

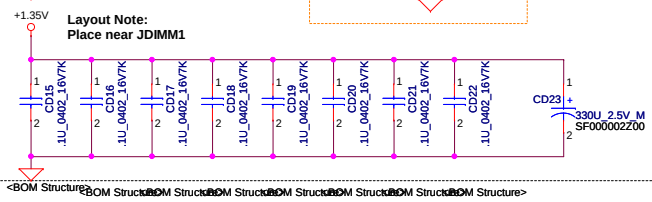


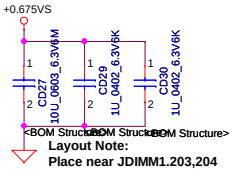
R1027, R1028 close to +DDR_A_VREF_DQ



R1029, R1030 close to +DDR_A_VREF_CA







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Issued Date	2014/07/07	Deciphered Date	2015/07/07	Title: DDR3L DIMMA
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				Date: Thursday, January 07, 2016 / Sheet 21 of 50

Channel B Rev

<Address: SA0:SA1=10 (A2H)>

DIMM_2 REV H:4mm

Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

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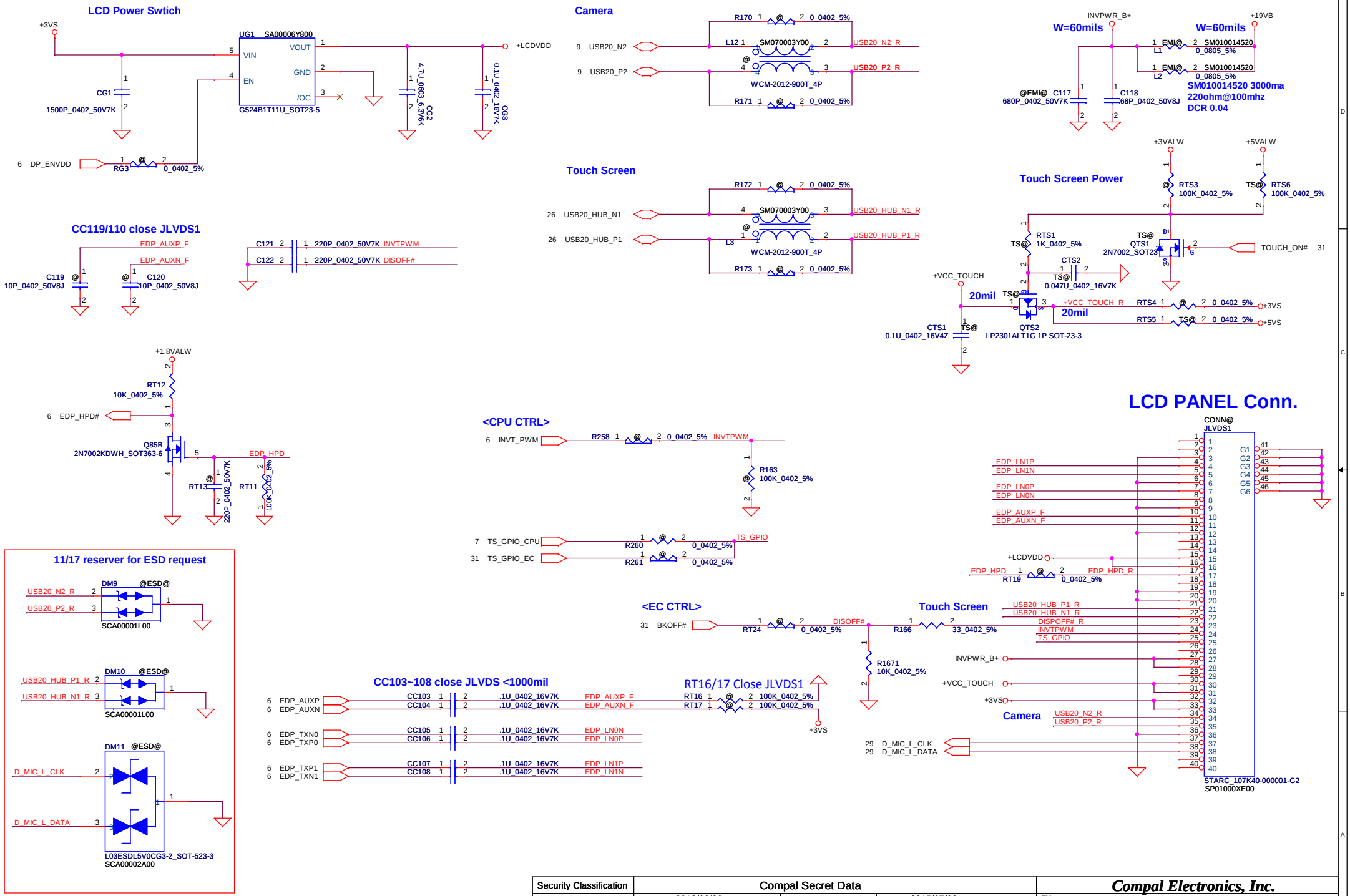
Compal Electronics, Inc.

Title: **DDR3L DIMMB**

Size: Custom | Document Number: **LA-706P** | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 22 of 50



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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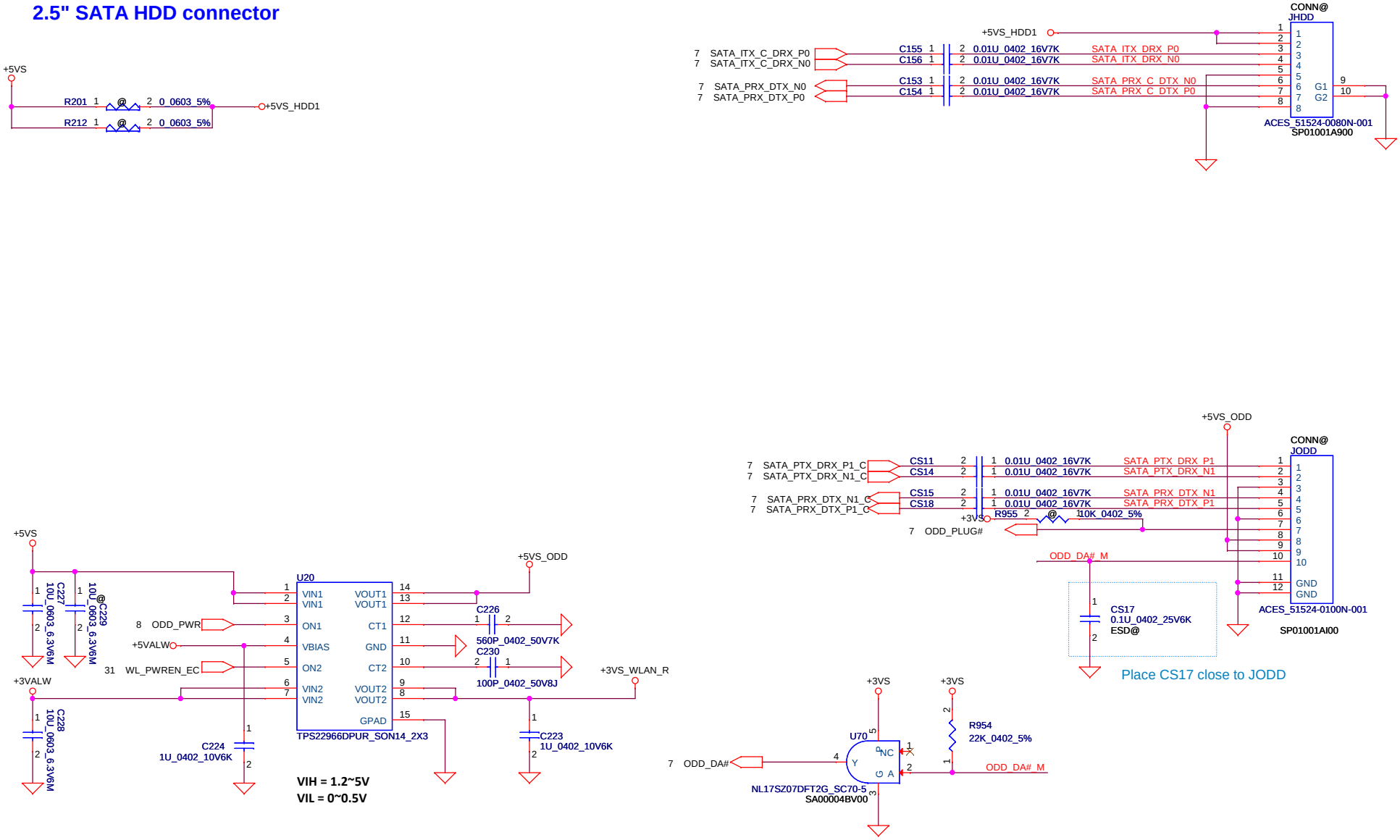
Compal Electronics, Inc.

Title: **LVDS Connector**

Size | Document Number | Rev 0.1

Date: Thursday, January 07, 2016 | Sheet 23 of 51

2.5" SATA HDD connector



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: ODD/SATA Conn

Size: B | Document Number: LA-706P | Rev: 0.1

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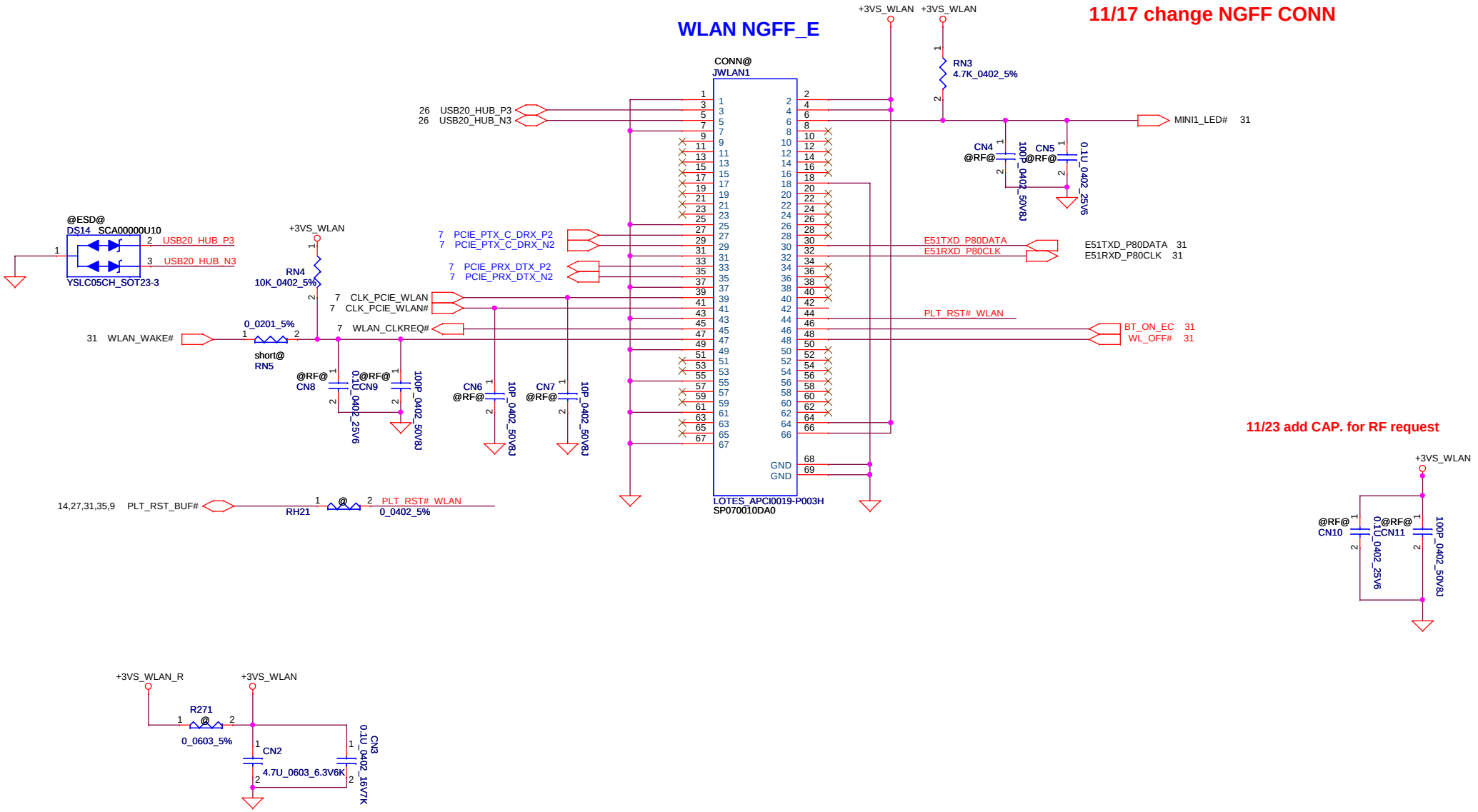

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: WLAN
				Size: Document Number: LA-706P — Rev: 0.1
				Date: Thursday, January 07, 2016 — Sheet 25 of 51

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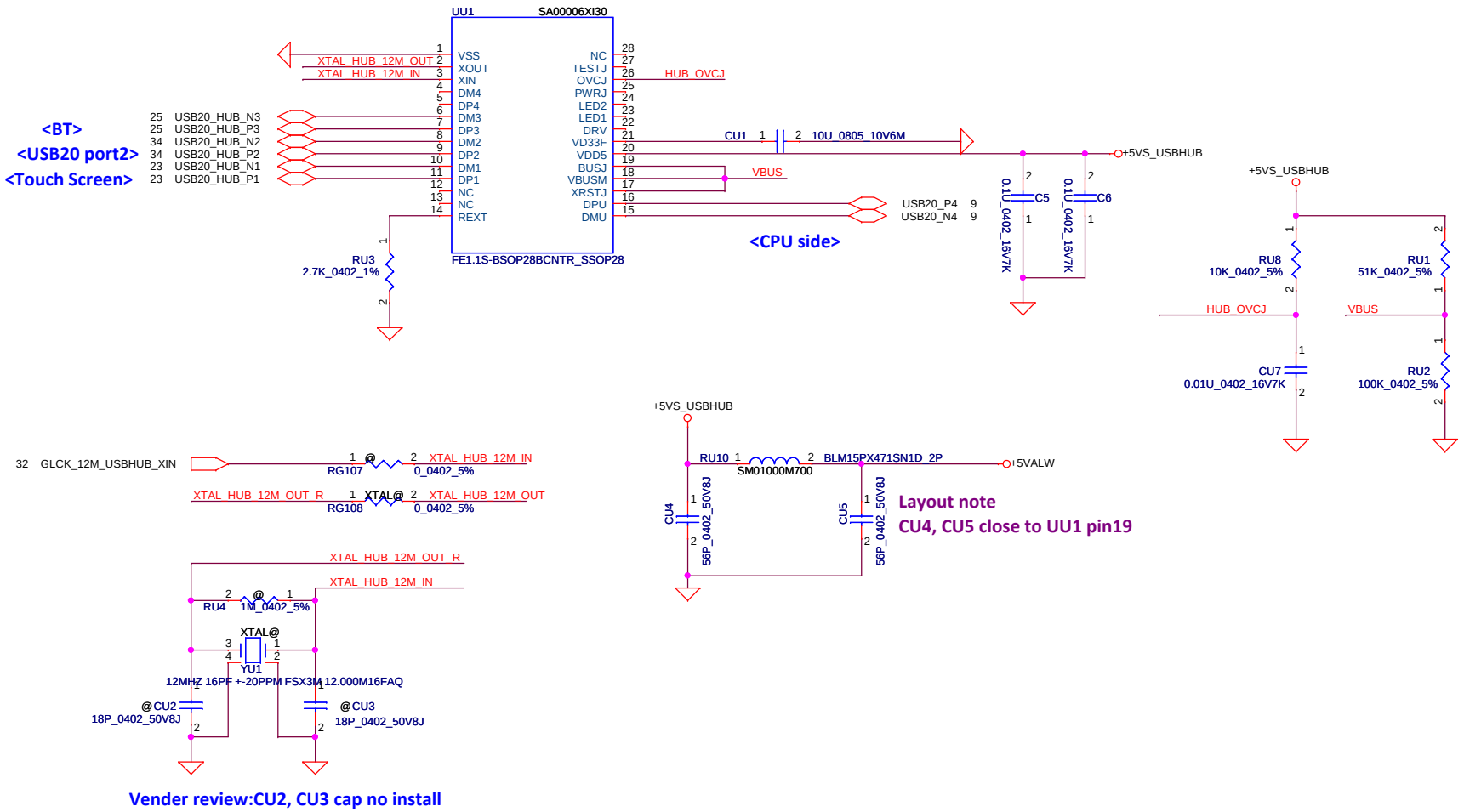

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: USB2.0 Hub
				Size: B; Document Number: LA-706P; Rev: 0.1
				Date: Thursday, January 07, 2016; Sheet 26 of 51

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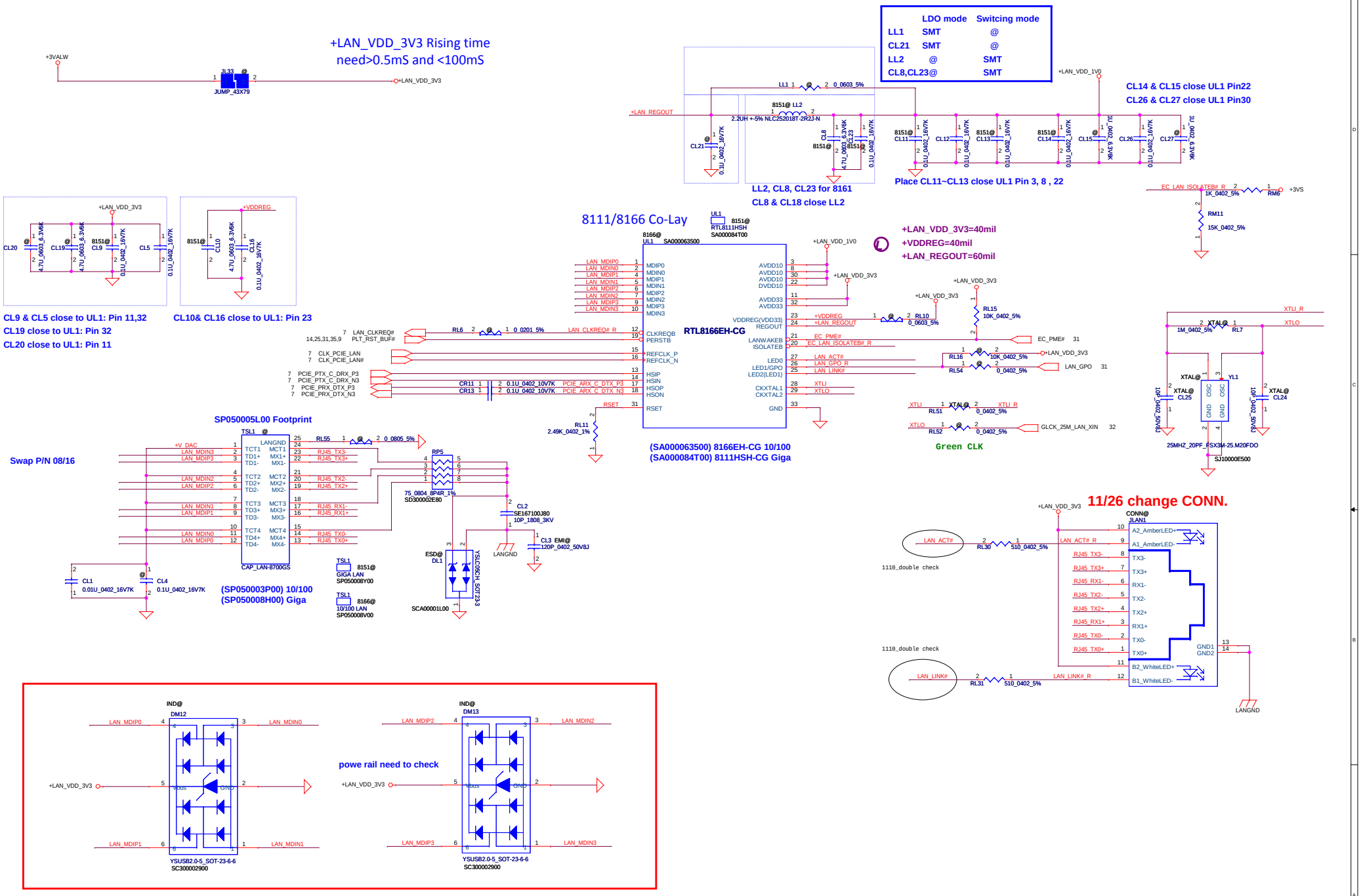

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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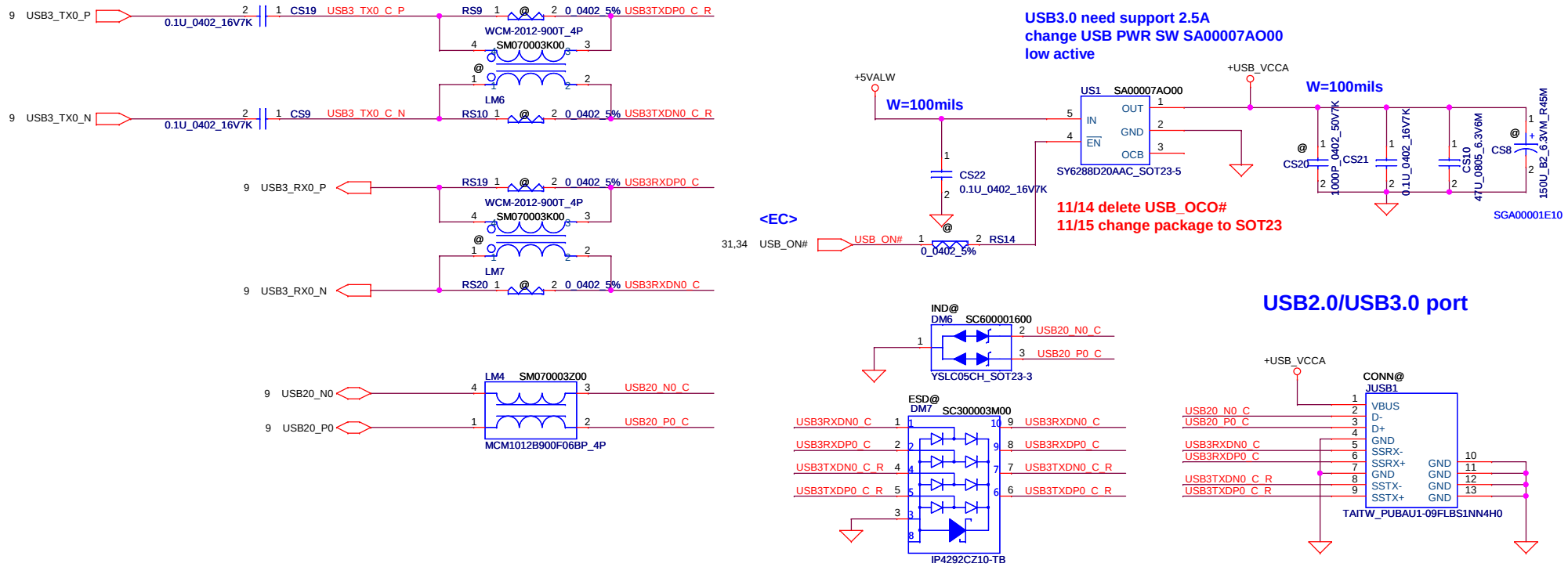
Compal Electronics, Inc.

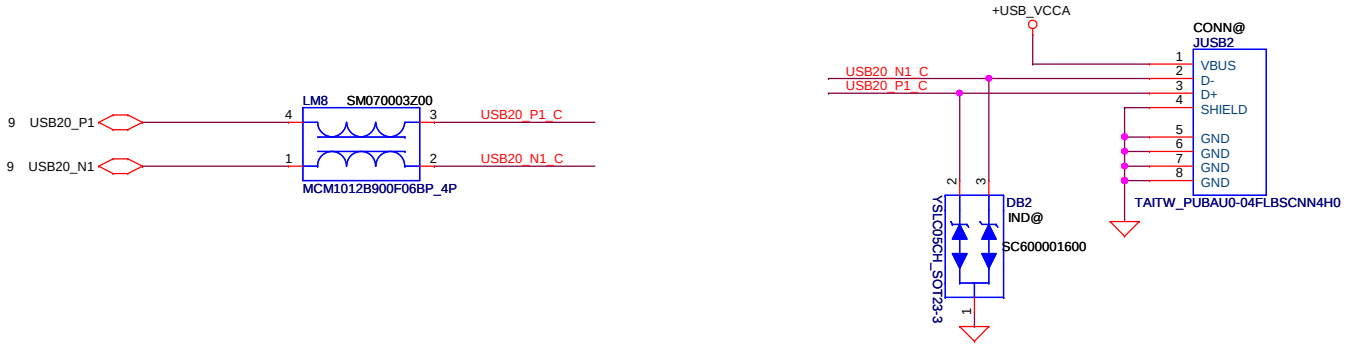
Title: **LAN 8111/8166**

Size	Document Number	Rev
	LA-706P	0.1

Date: Thursday, January 07, 2016 | Sheet 27 of 51



USB2.0 Port



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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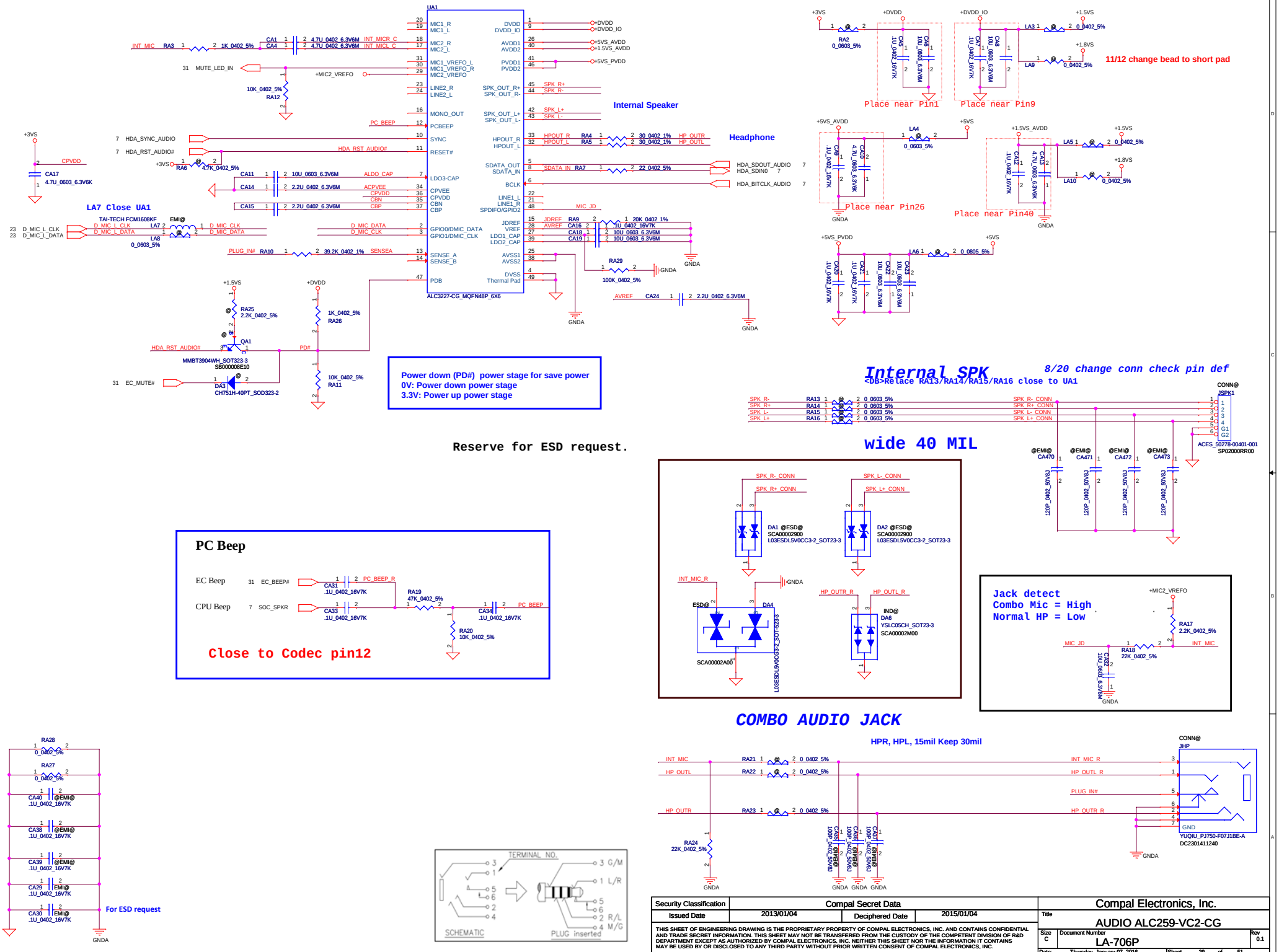
Compal Electronics, Inc.

Title: USB 3.0/2.0 conn

Size: B | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 28 of 51



Security Classification	Compal Secret Data		
Issued Date	2013/01/04	Deciphered Date	2015/01/04

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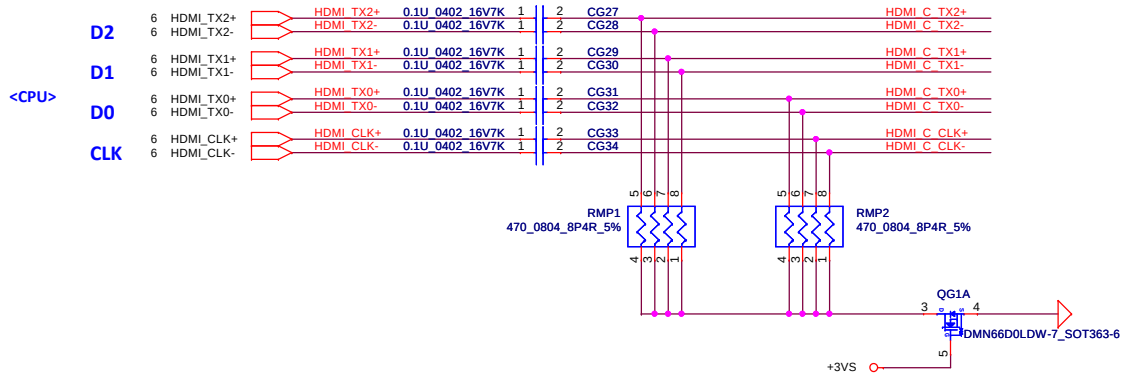
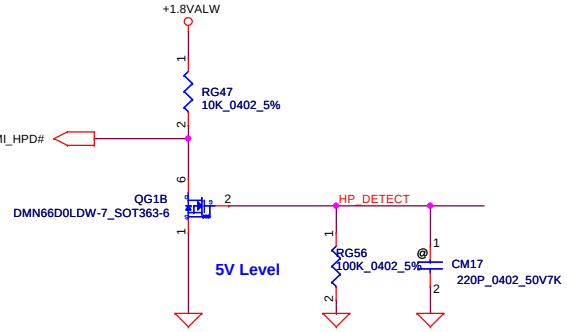
Compal Electronics, Inc.

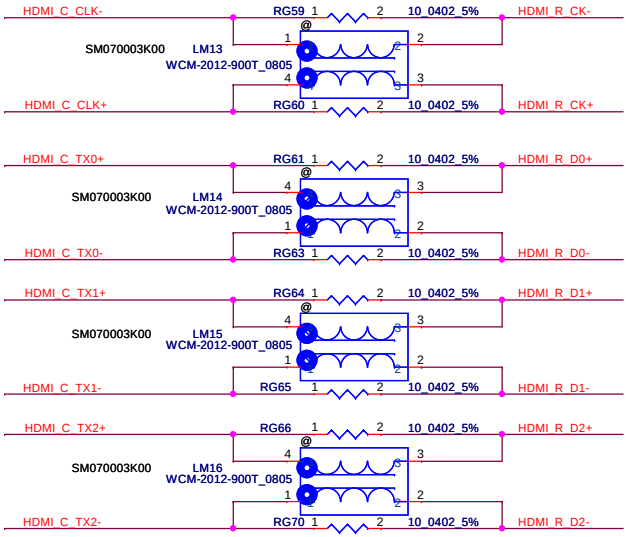
Title: AUDIO ALC259-VC2-CG

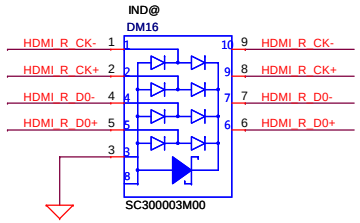
Size: C | Document Number: LA-706P | Rev: 0.1

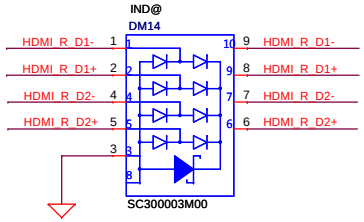
Date: Thursday, January 07, 2016 | Sheet 29 of 51

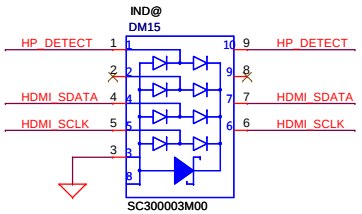


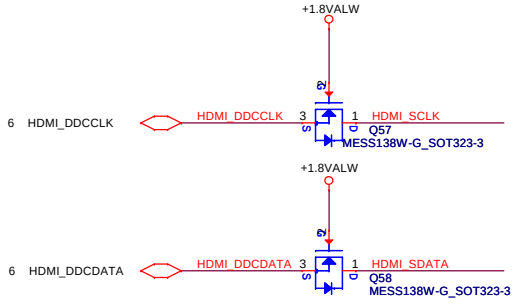


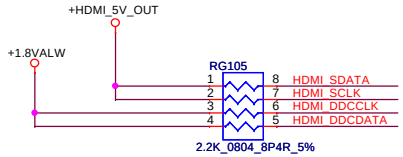




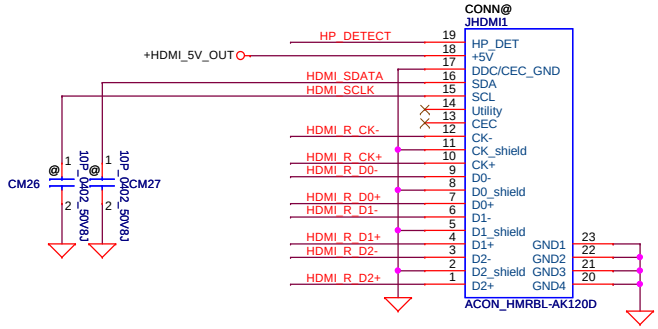


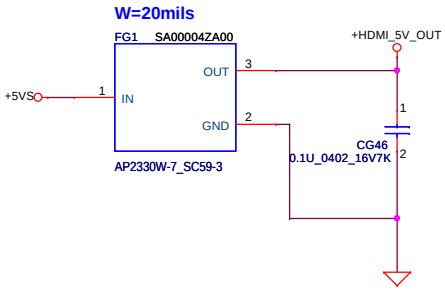






HDMI Conn.





Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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Compal Electronics, Inc.

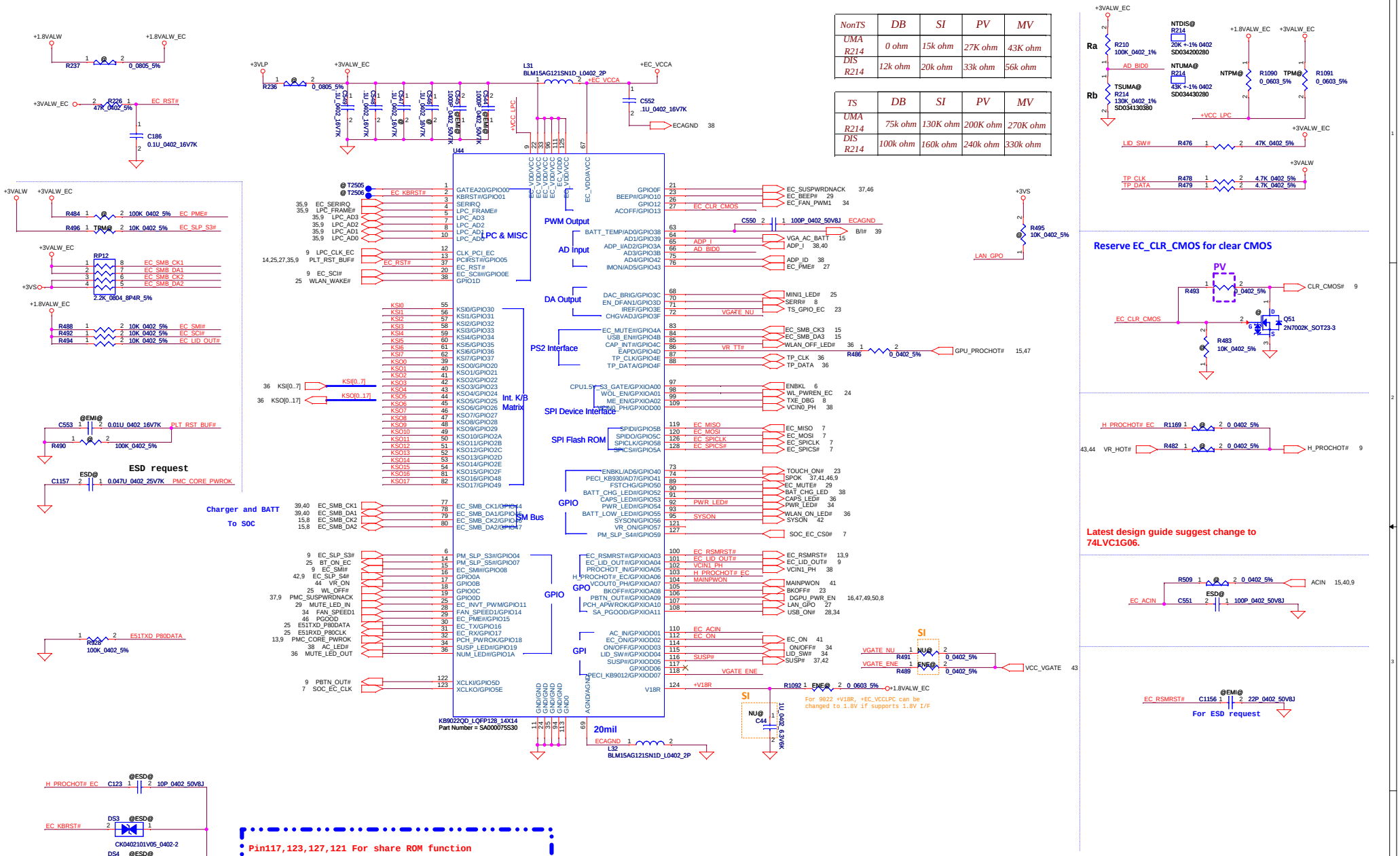
Title: **HDMI Conn/Level shift**

Size | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 30 of 51

NonTS	DB	SI	PV	MV
UMA R214	0 ohm	15k ohm	27K ohm	43K ohm
DIS R214	12k ohm	20k ohm	33k ohm	56k ohm

TS	DB	SI	PV	MV
UMA R214	75k ohm	130K ohm	200K ohm	270K ohm
DIS R214	100k ohm	160k ohm	240k ohm	330k ohm



Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

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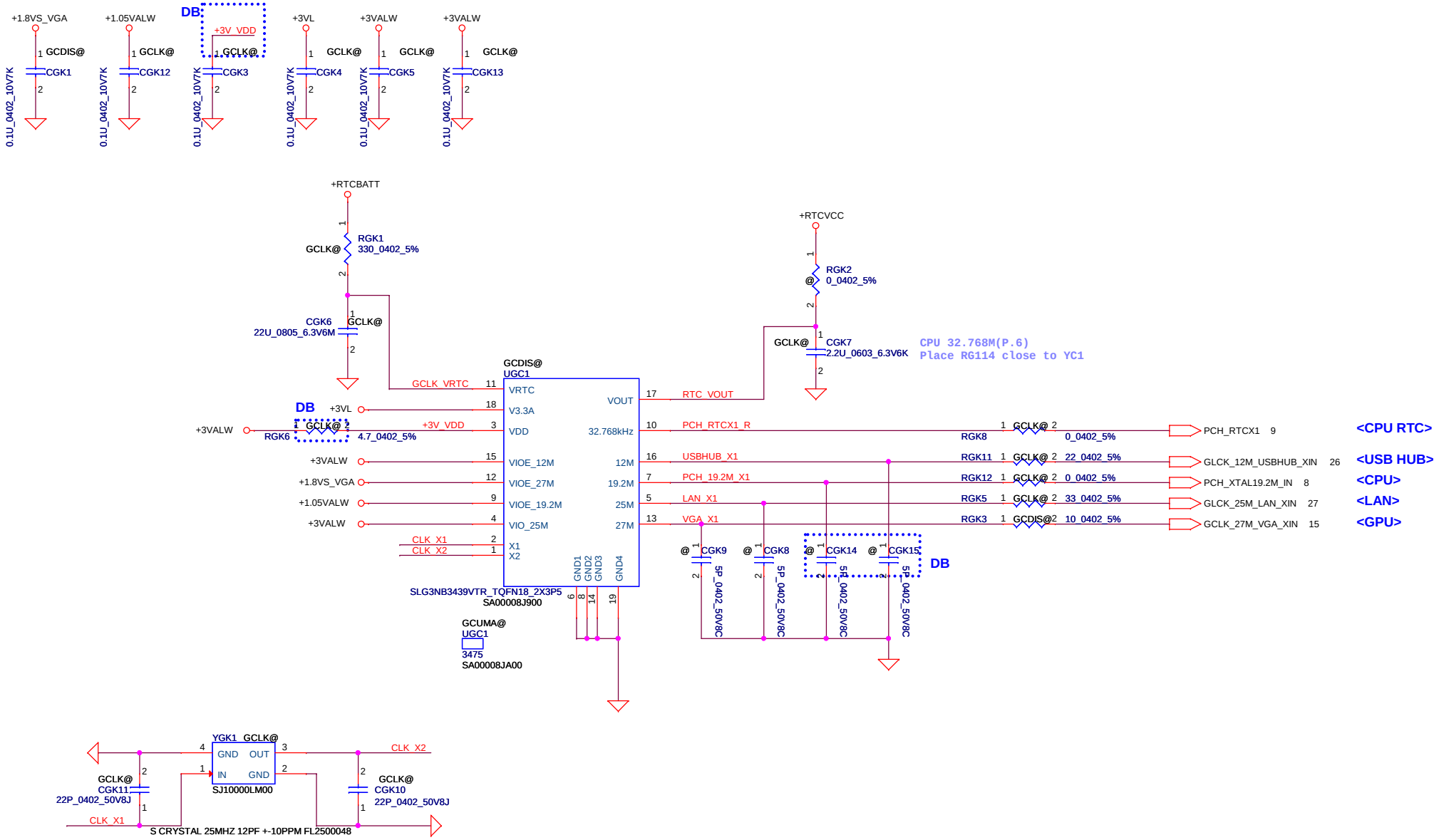
Compal Electronics, Inc.

Title: EC ENE KB9012/KB9022

Size: C | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 31 of 51



Security Classification	Compal Secret Data		
Issued Date	2013/06/10	Deciphered Date	2014/07/01

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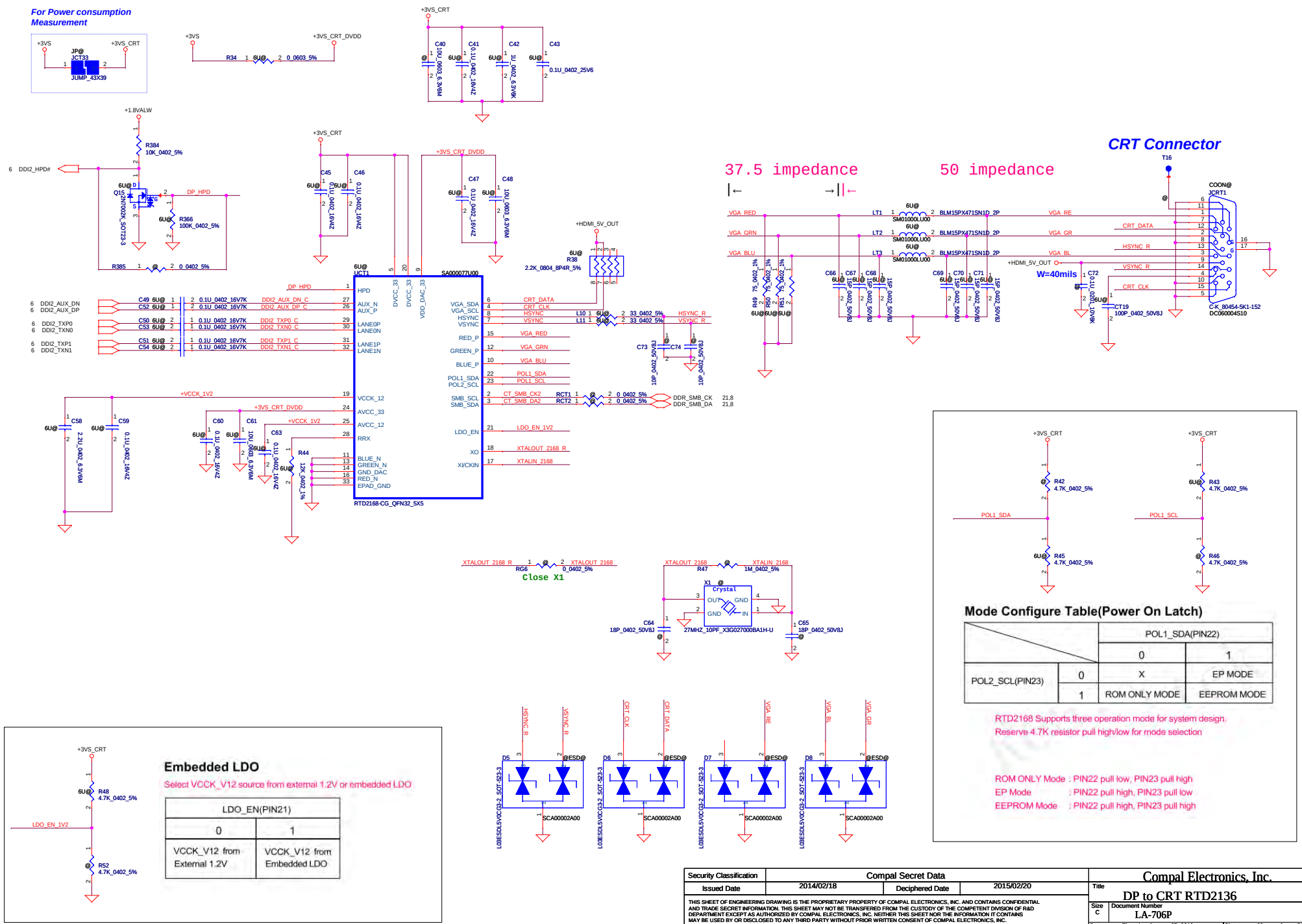
Compal Electronics, Inc.

Title: **GCLK**

Size: **LA-706P** | Document Number | Rev 0.1

Date: Thursday, January 07, 2016 | Sheet 32 of 51

DP to CRT converter



Security Classification	Compal Secret Data		
Issued Date	2014/02/18	Deciphered Date	2015/02/20

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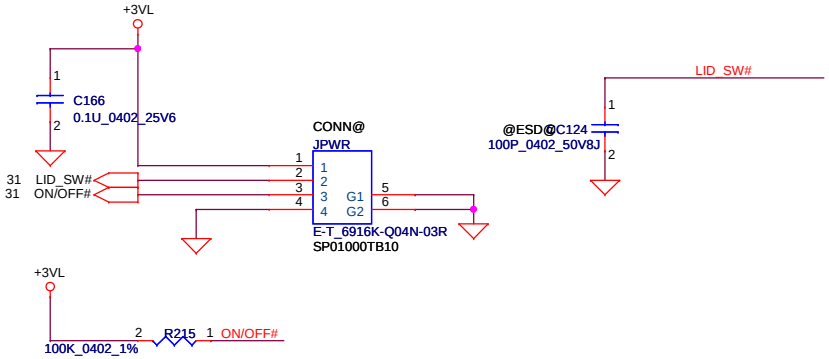
Compal Electronics, Inc.

Title: DP to CRT RTD2136

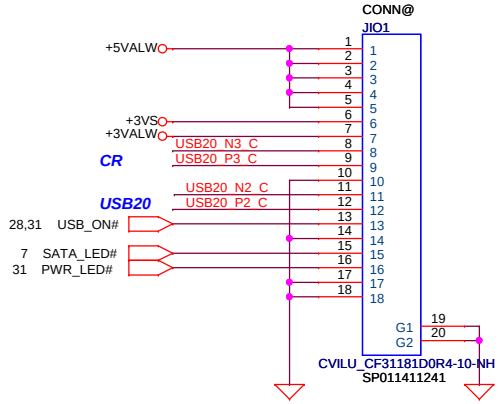
Size: C | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 33 of 51

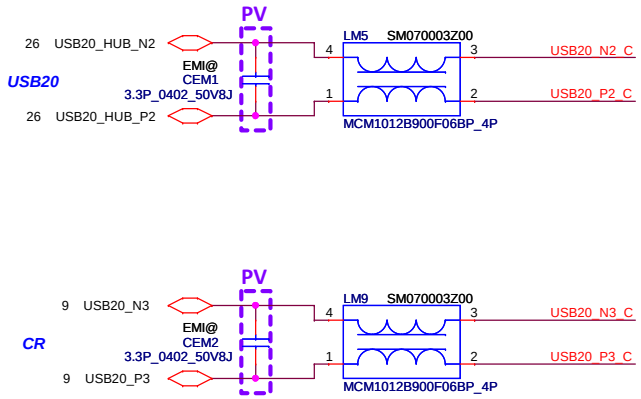
Powert Button Connector



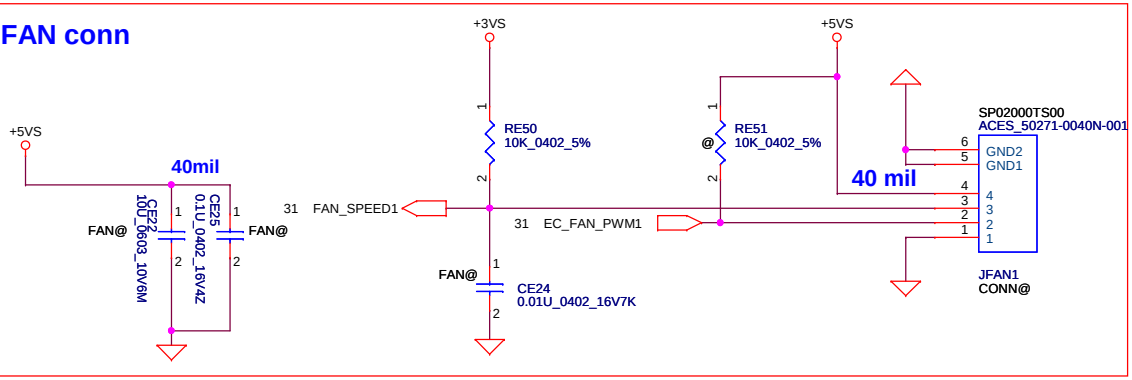
JIO S/B



CEM1,2 Close LM5/LM9



FAN conn



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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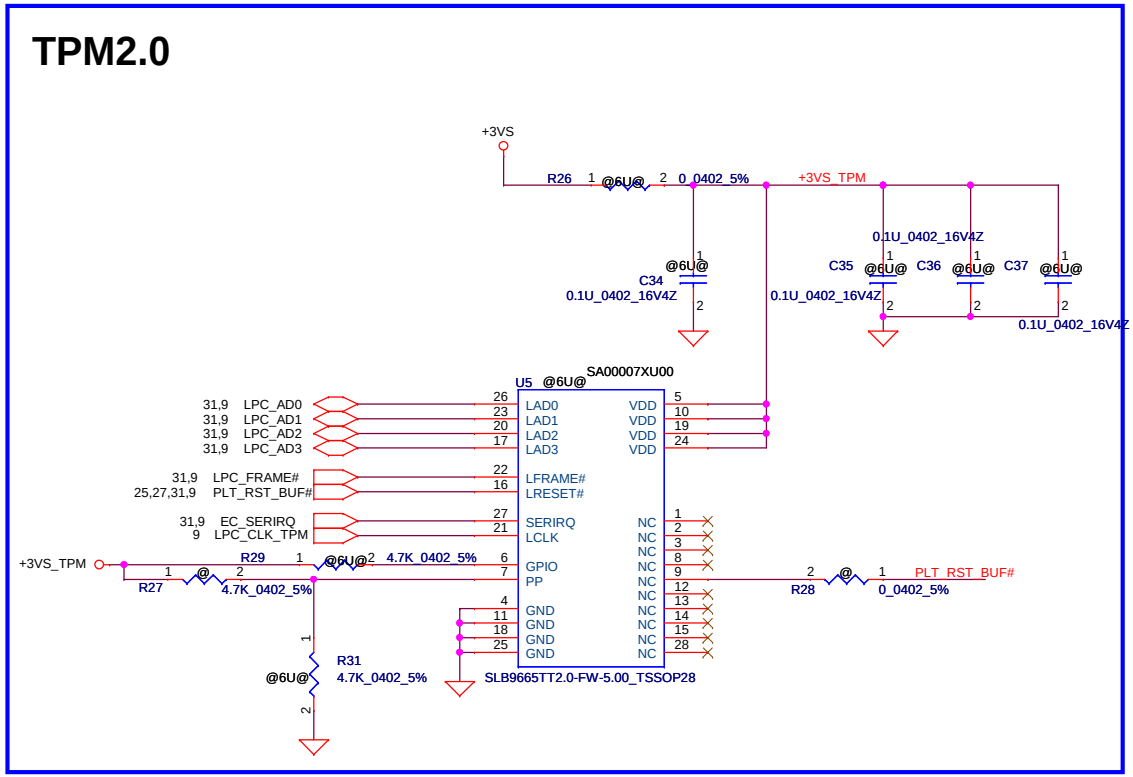
Compal Electronics, Inc.

Title: PWRBTN/FAN

Size: B | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 34 of 51

TPM2.0



H3 H_2P8 HOLEA
H4 H_2P5 HOLEA
H5 H_2P8 HOLEA
H6 H_2P5 HOLEA
H12 H_2P8 HOLEA
H8 H_2P5 HOLEA
H19 H_2P5 HOLEA
H20 H_2P5 HOLEA
H21 H_2P5 HOLEA
H24 H_2P4X3P0N HOLEA
H25 H_2P4X3P0N HOLEA
H26 H_2P4N HOLEA

VGA

H17 H_5P0 HOLEA
H18 H_5P0 HOLEA

CPU

H9 H_5P0 HOLEA
H10 H_5P0 HOLEA
H11 H_5P0 HOLEA
H13 H_5P0 HOLEA

FD1 FIDUCIAL_C40M80
FD2 FIDUCIAL_C40M80
FD3 FIDUCIAL_C40M80
FD4 FIDUCIAL_C40M80

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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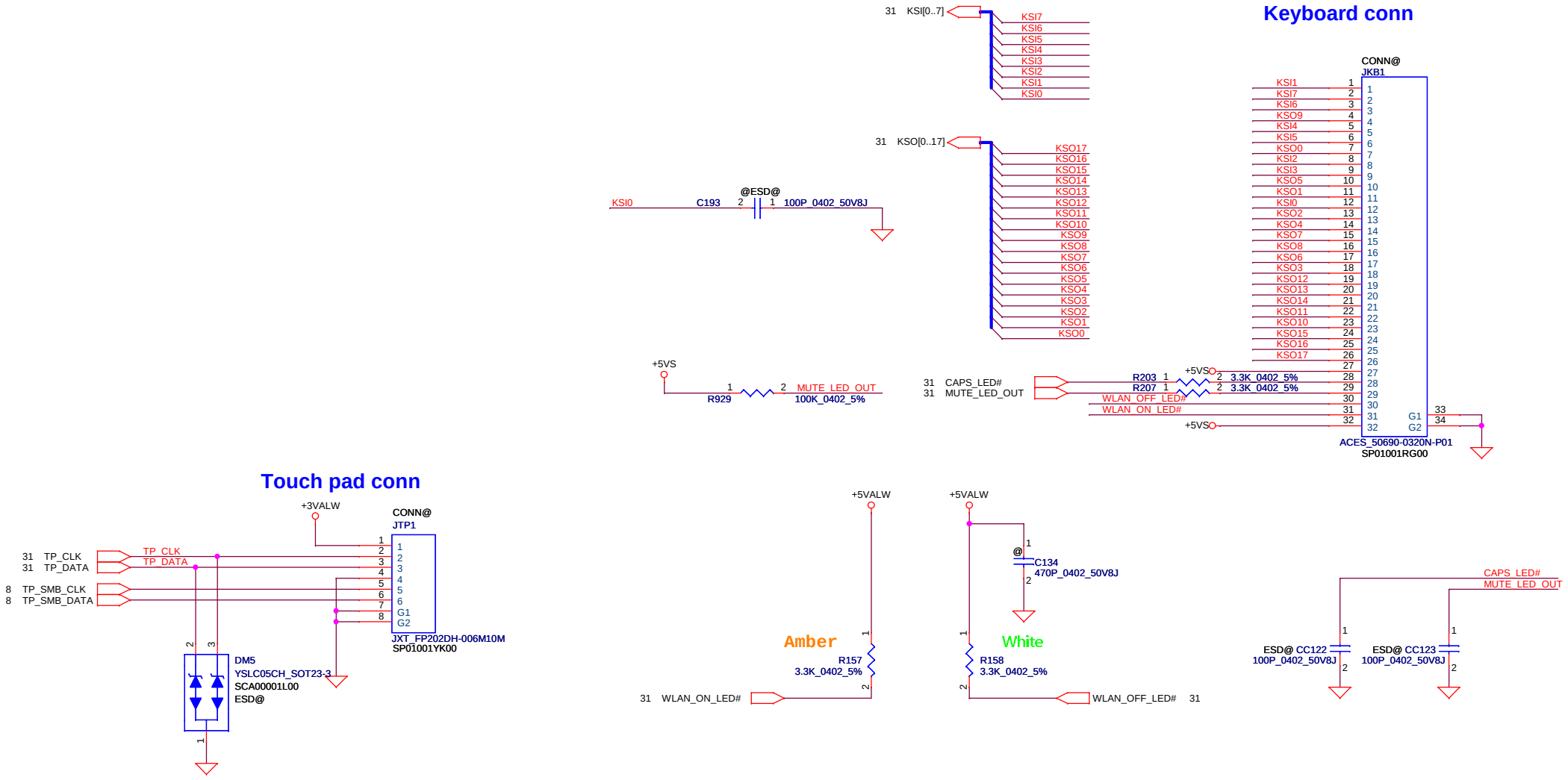
Compal Electronics, Inc.

Title: **LED/Screw hole**

Size: LA-706P | Document Number | Rev 0.1

Date: Thursday, January 07, 2016 | Sheet 35 of 51



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: KB/TP
				Size: B; Document Number: LA-706P; Rev: 0.1
				Date: Thursday, January 07, 2016; Sheet 36 of 51

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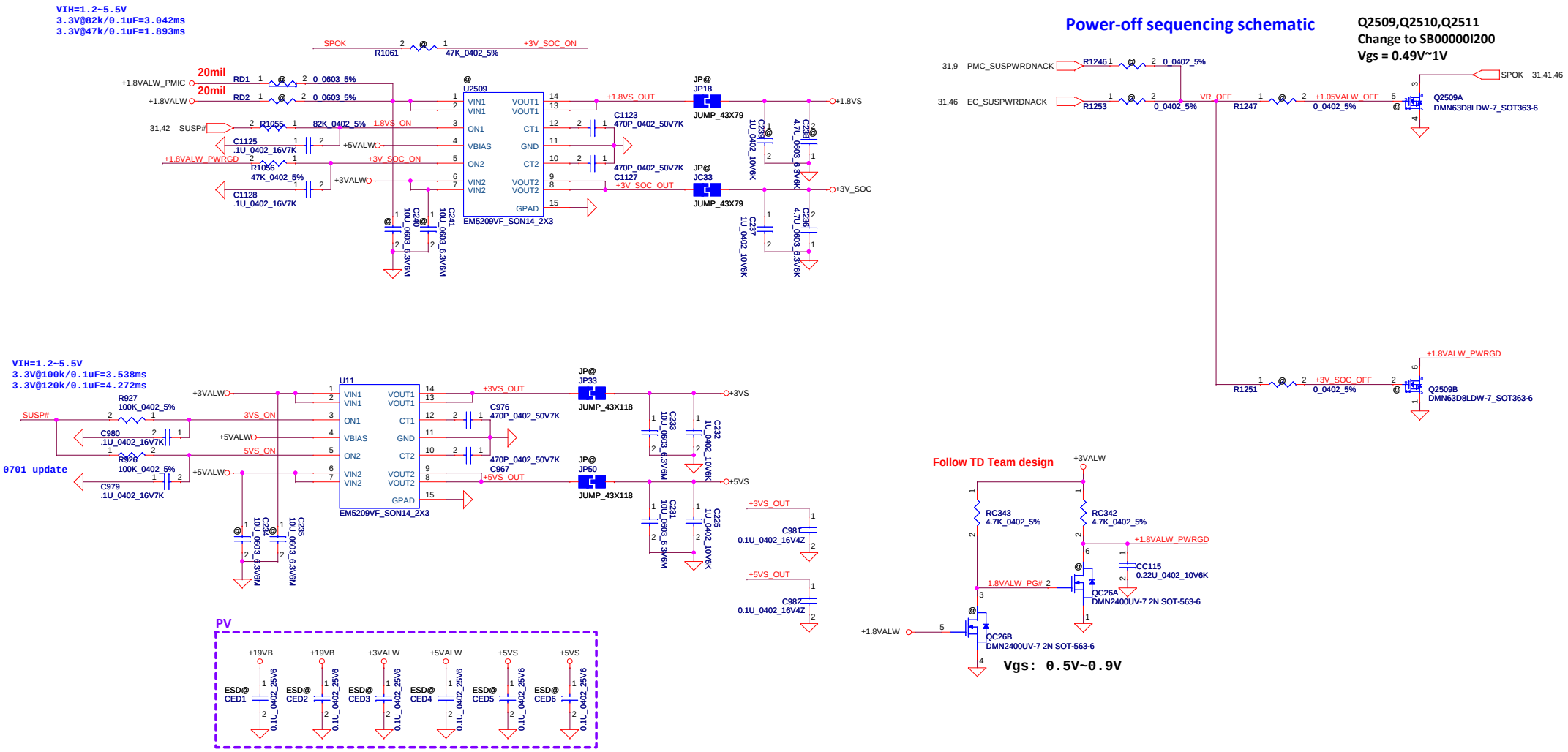

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/07/07	Deciphered Date	2015/07/07	Title: DC Interface
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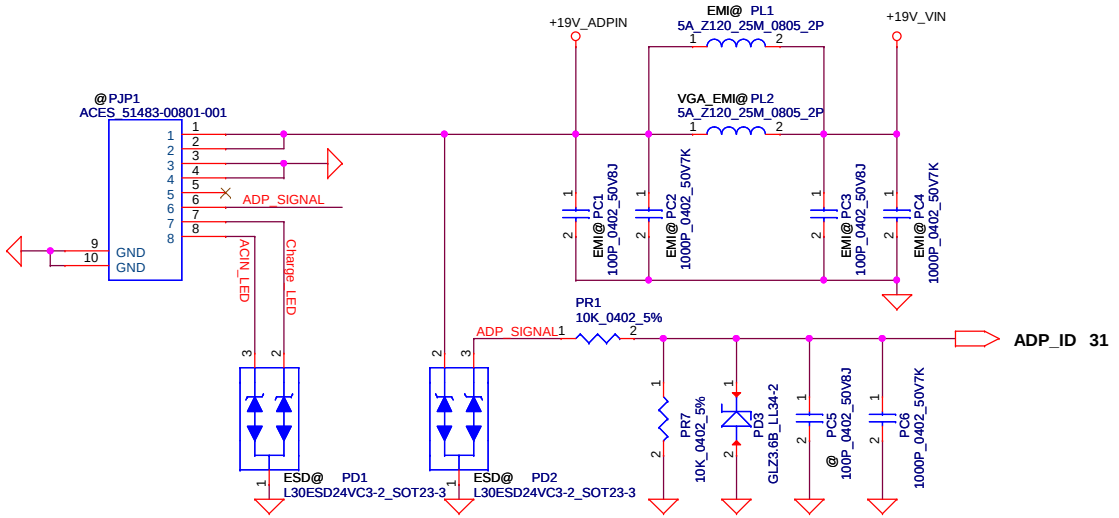
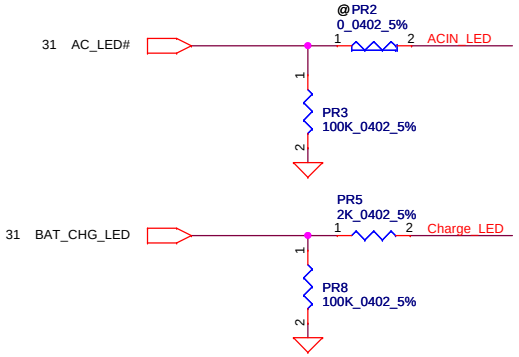
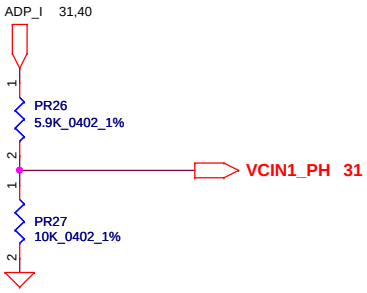
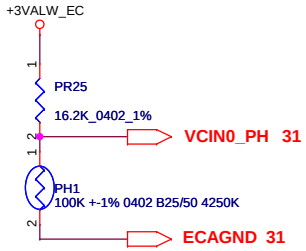
				Date: Thursday, January 07, 2016 / Sheet 37 of 51









Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2014/10/28

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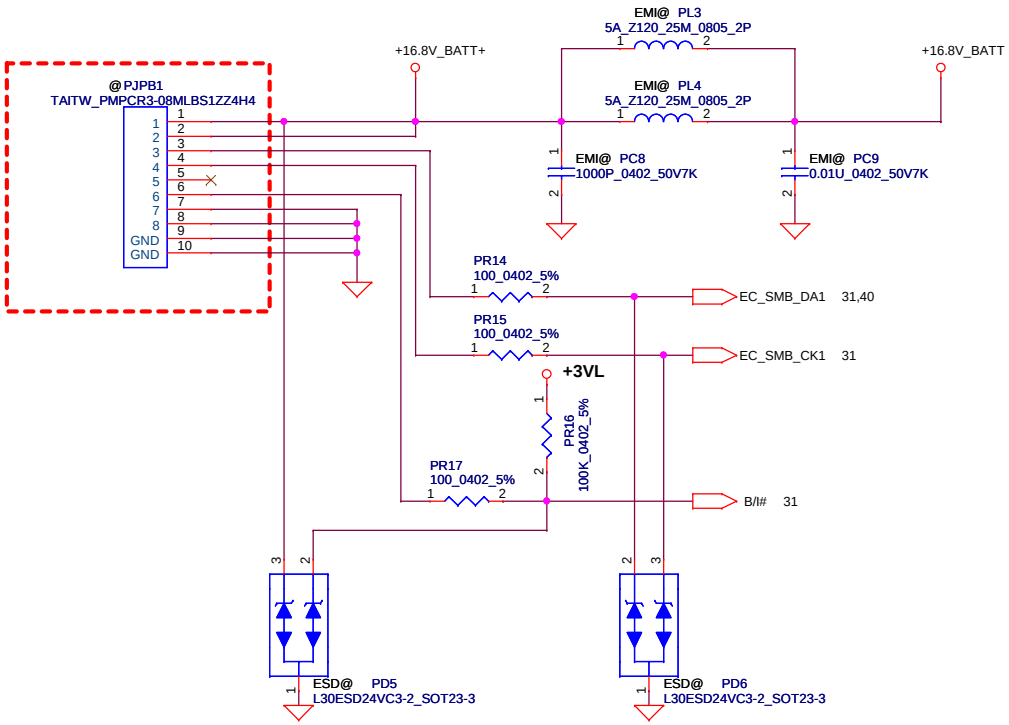
Compal Electronics, Inc.

Title: ***DC Conn***

Size | Document Number: **LA-C706P** | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 38 of 52



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2015/10/08	Deciphered Date	2016/08/06	Title: BATT Conn
				Size: Document Number: LA-C706P Rev: 0.1
				Date: Thursday, January 07, 2016 Sheet 39 of 52

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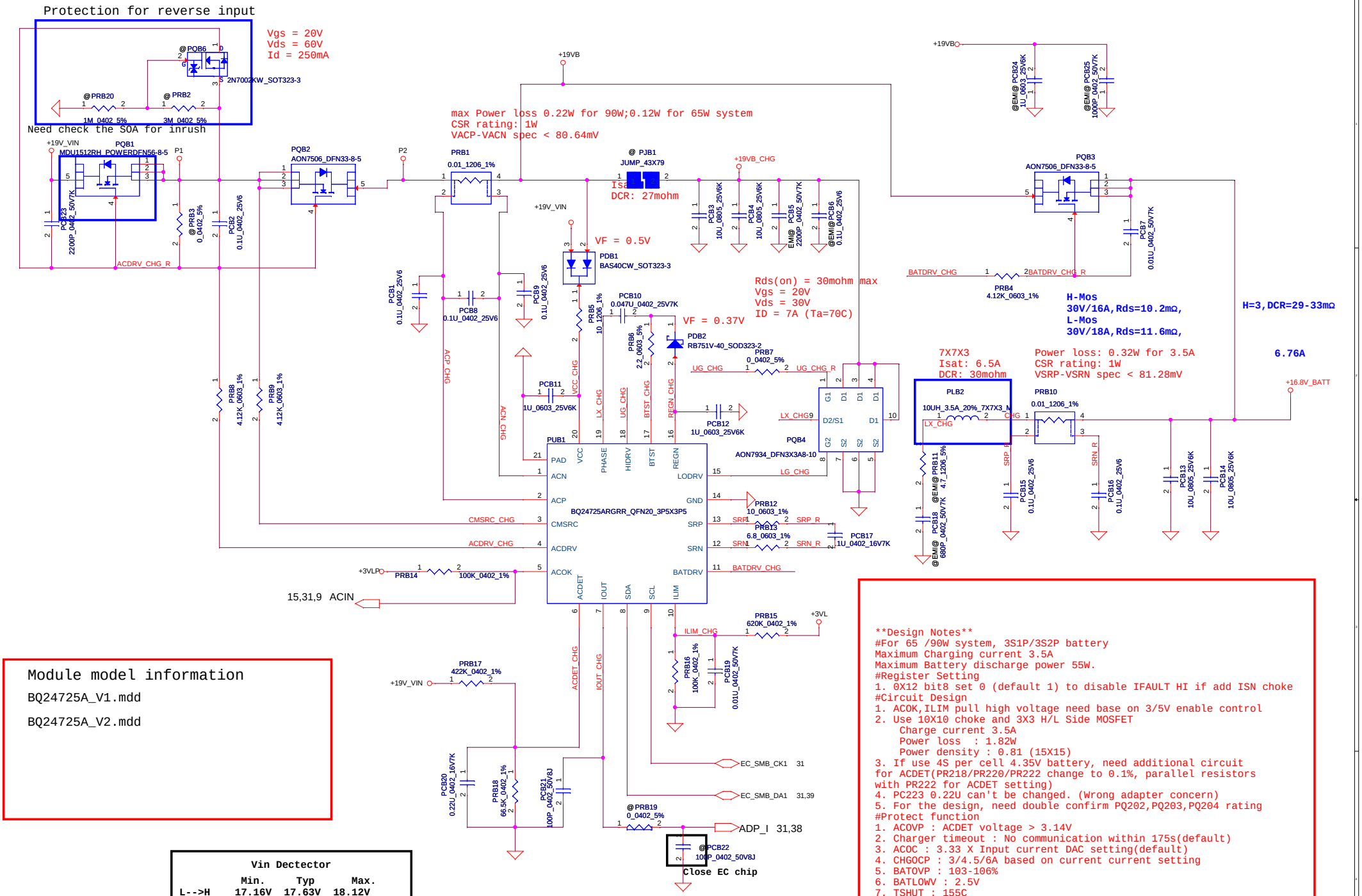

Module model information

BQ24725A_V1.mdd

BQ24725A_V2.mdd

Vin Dectector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+107)/20/0.02
= 3.986 A

```
**Design Notes**
#For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W.
#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
#Circuit Design
1. ACOK,ILIM pull high voltage need base on 3/5V enable control
2. Use 10X10 choke and 3X3 H/L Side MOSFET
    Charge current 3.5A
    Power loss  : 1.82W
    Power density : 0.81 (15X15)
3. If use 4S per cell 4.35V battery, need additional circuit
for ACDET(PR218/PR220/PR222 change to 0.1%, parallel resistors
with PR222 for ACDET setting)
4. PC223 0.22U can't be changed. (Wrong adapter concern)
5. For the design, need double confirm PQ202,PQ203,PQ204 rating
#Protect function
1. ACOVP : ACDET voltage > 3.14V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVP : 103-106%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 150mV (default)
```

Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2012/07/02

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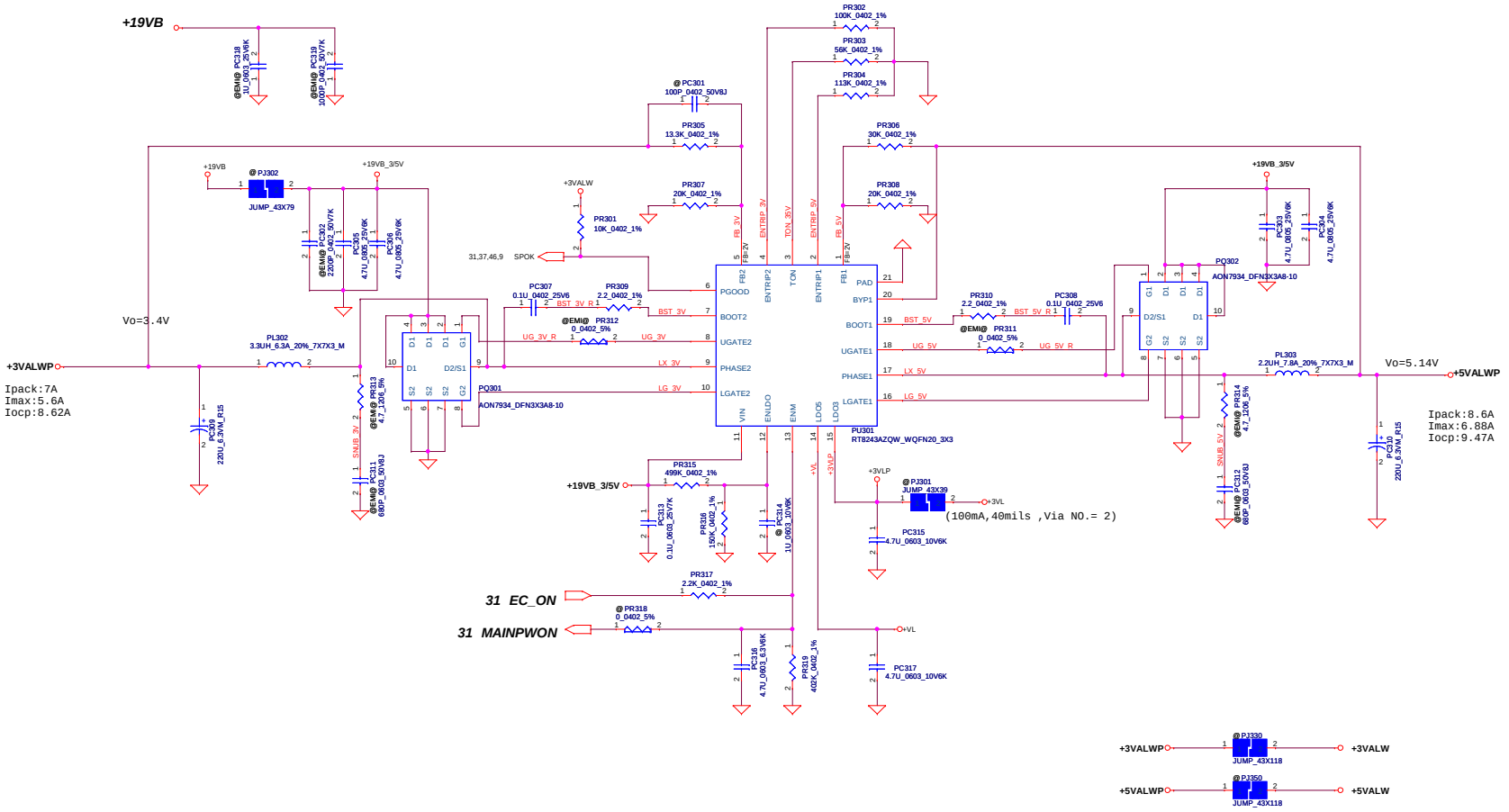
Compal Electronics, Inc.

Title: **CHARGER**

Size | Document Number: *Intel / Braswell* | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 40 of 52



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2015/10/08	Deciphered Date	2016/08/06	Title: 3VALW/5VALW
				Size: A2 · Document Number: Intel / Braswell · Rev: 0.1
				Date: · Sheet 41 of 52

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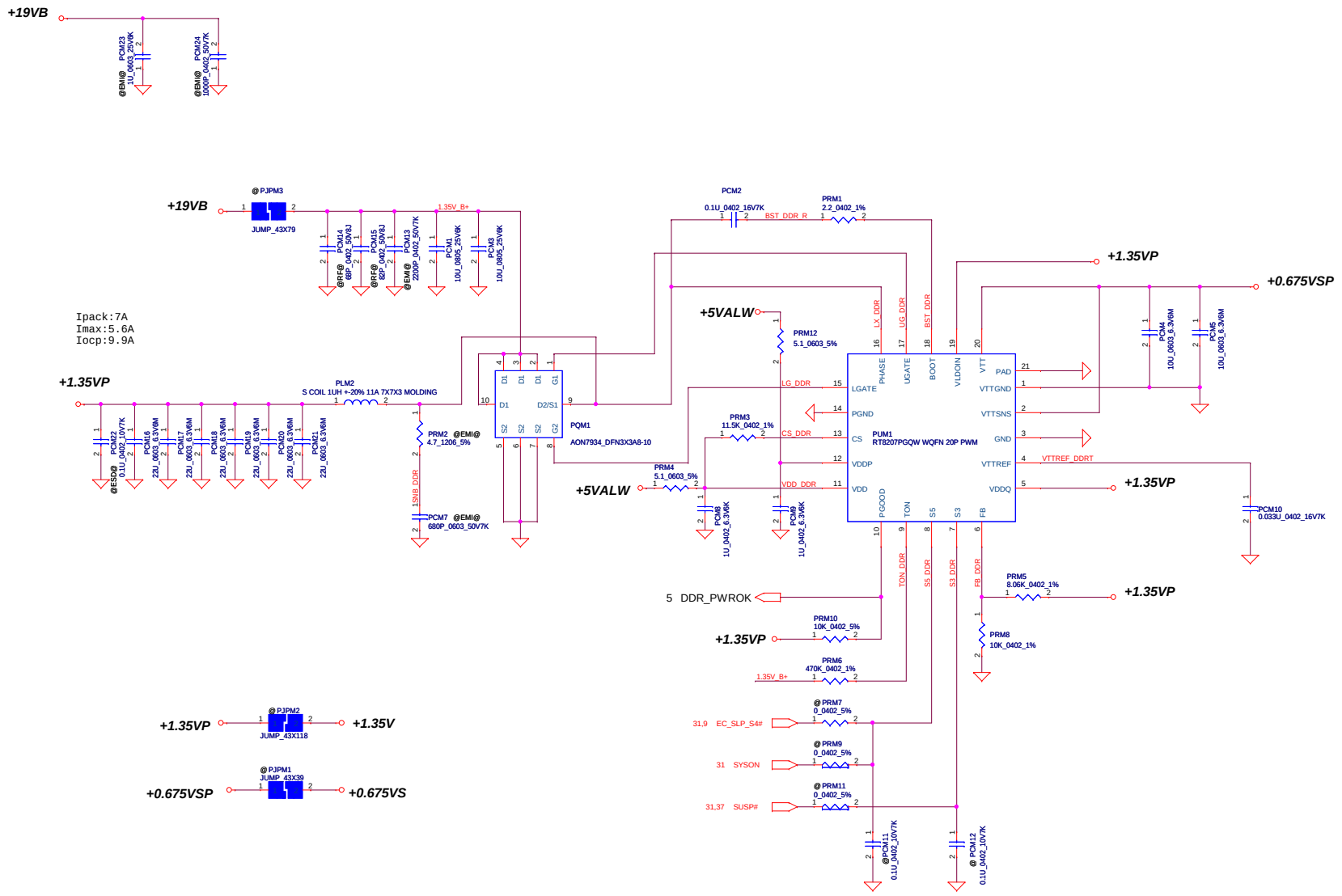

Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2014/10/28

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Compal Electronics, Inc.

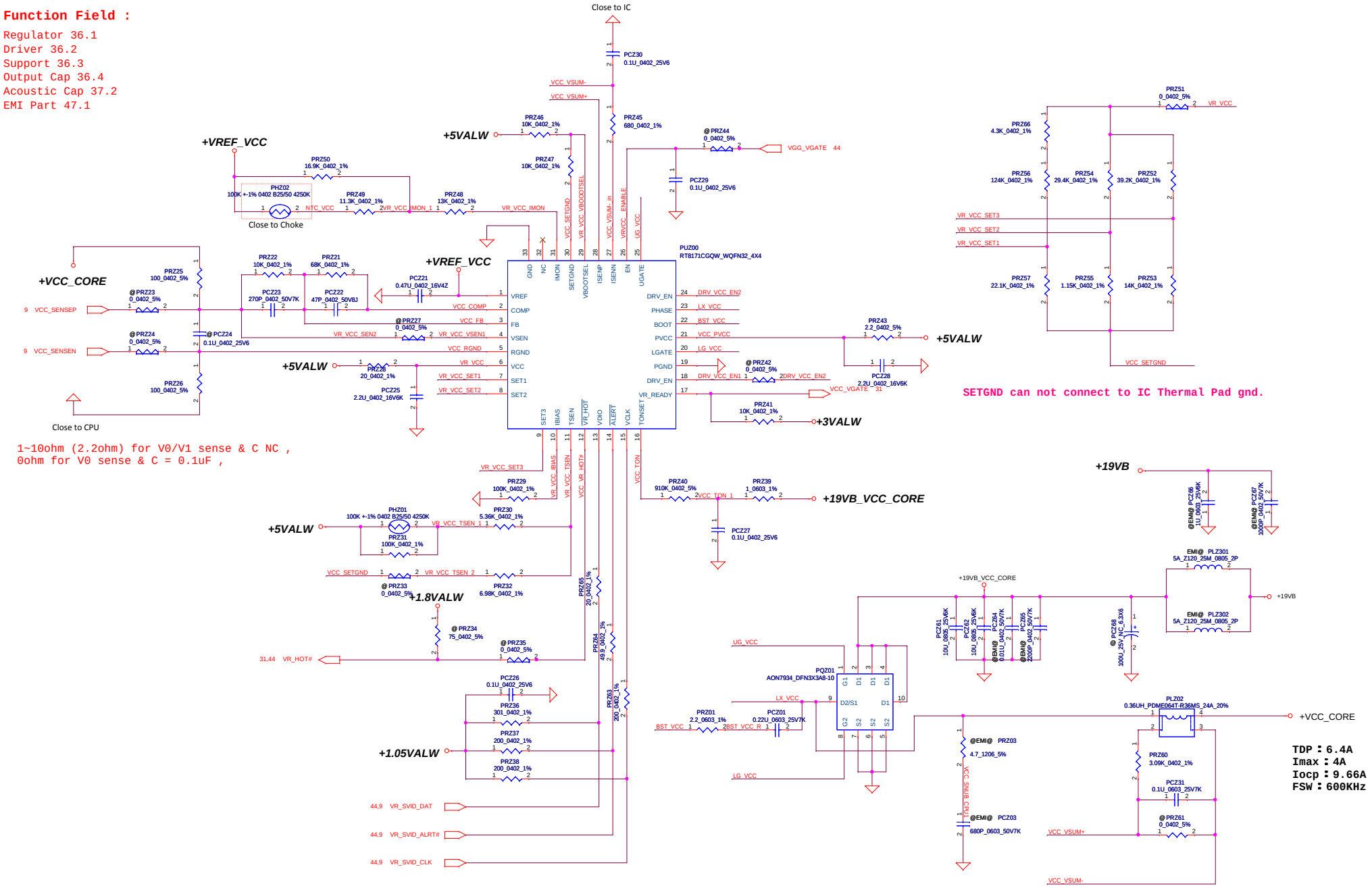
Title: **1.35V/0.675VS**

Size: C | Document Number: *Intel / Braswell* | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 42 of 52

Function Field :

Regulator 36.1
Driver 36.2
Support 36.3
Output Cap 36.4
Acoustic Cap 37.2
EMI Part 47.1



TDP : 6.4A
Imax : 4A
Iocp : 9.66A
FSW : 600KHz

Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2013/07/10

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Compal Electronics, Inc.

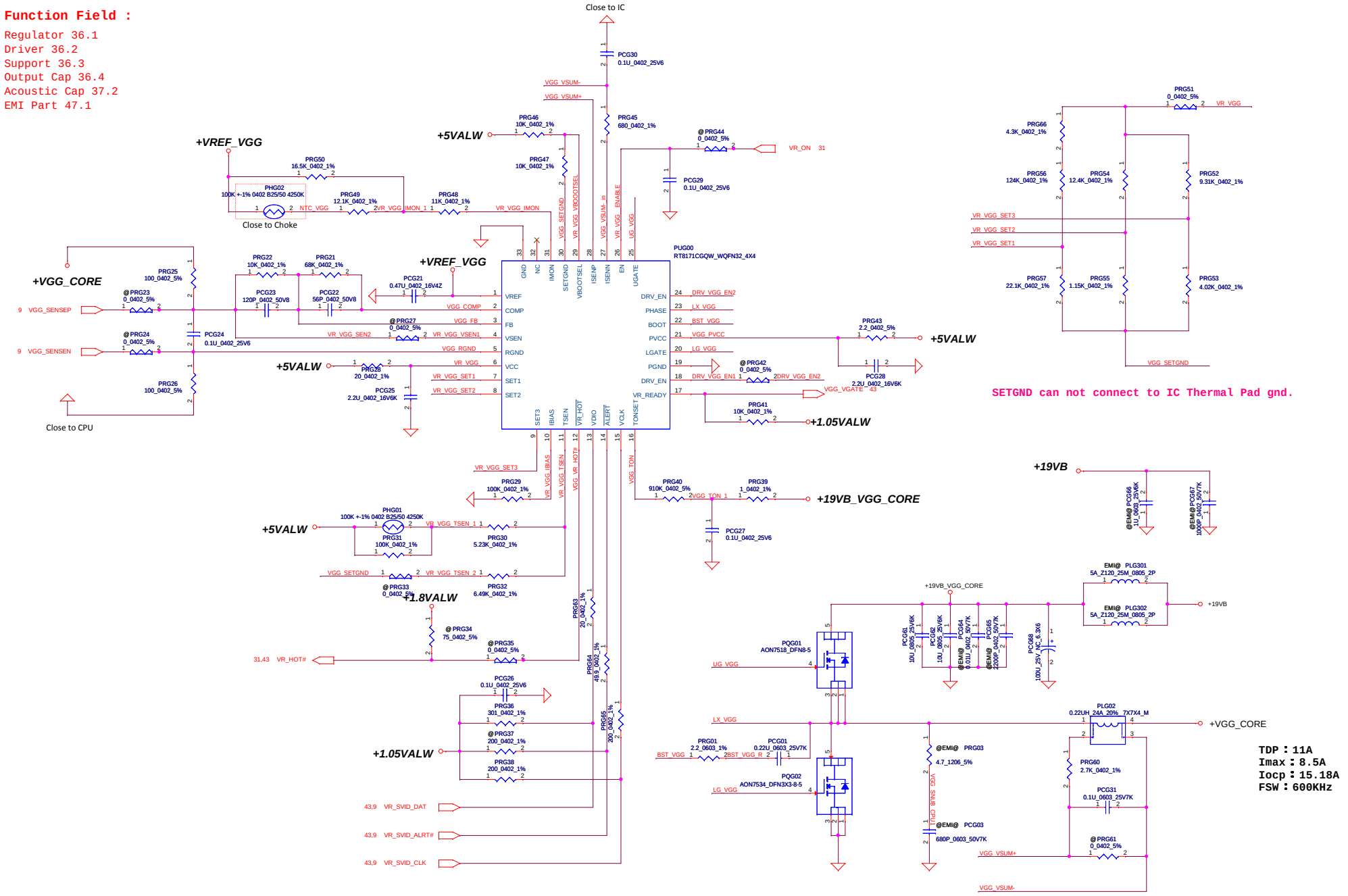
Title: *VCC_Core*

Size: C | Document Number: *Intel / Braswell* | Rev: 0.1

Date: | Sheet 43 of 52

Function Field :

Regulator 36.1
Driver 36.2
Support 36.3
Output Cap 36.4
Acoustic Cap 37.2
EMI Part 47.1



SETGND can not connect to IC Thermal Pad gnd.

TDP : 11A
Imax : 8.5A
Iocp : 15.18A
FSW : 600KHz

Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2013/07/10

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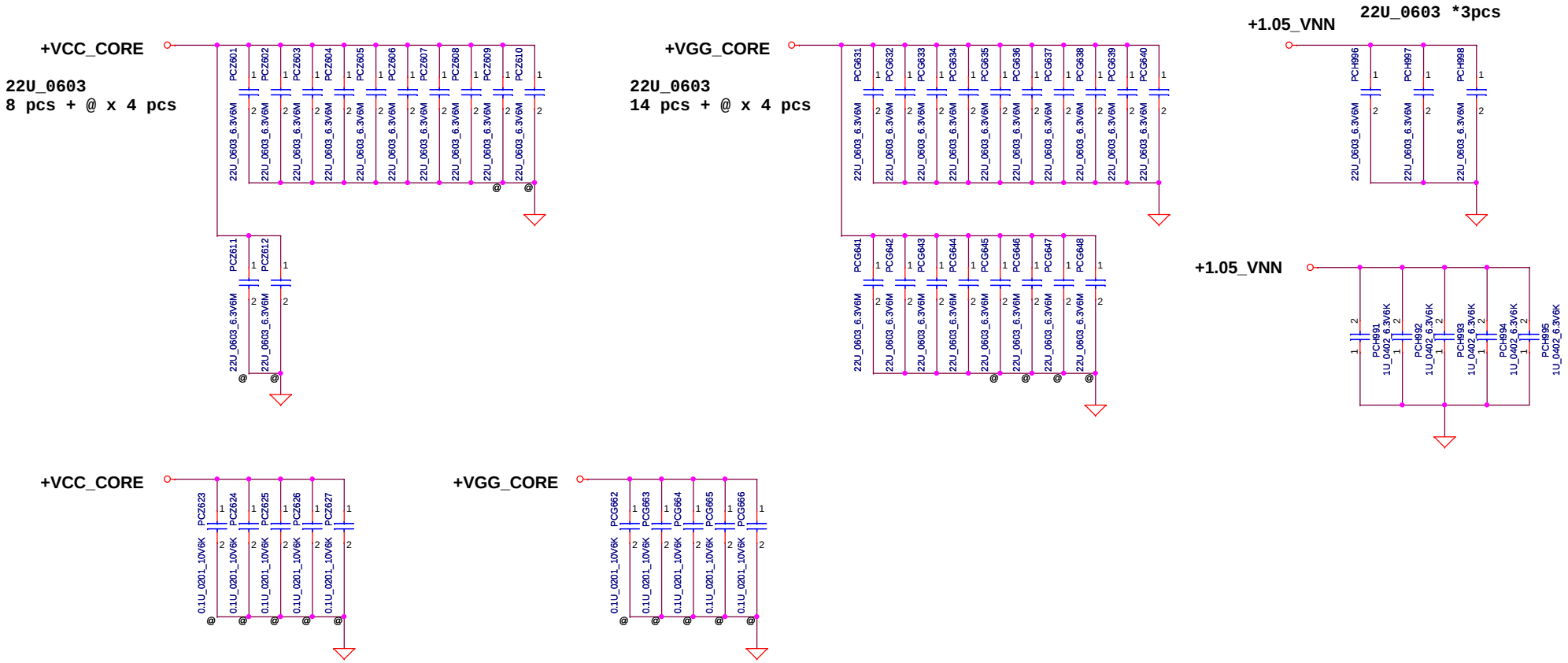
Compal Electronics, Inc.

Title: *VGG_Core*

Size: C | Document Number: *Intel / Braswell* | Rev: 0.1

Date: | Sheet 44 of 52



Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

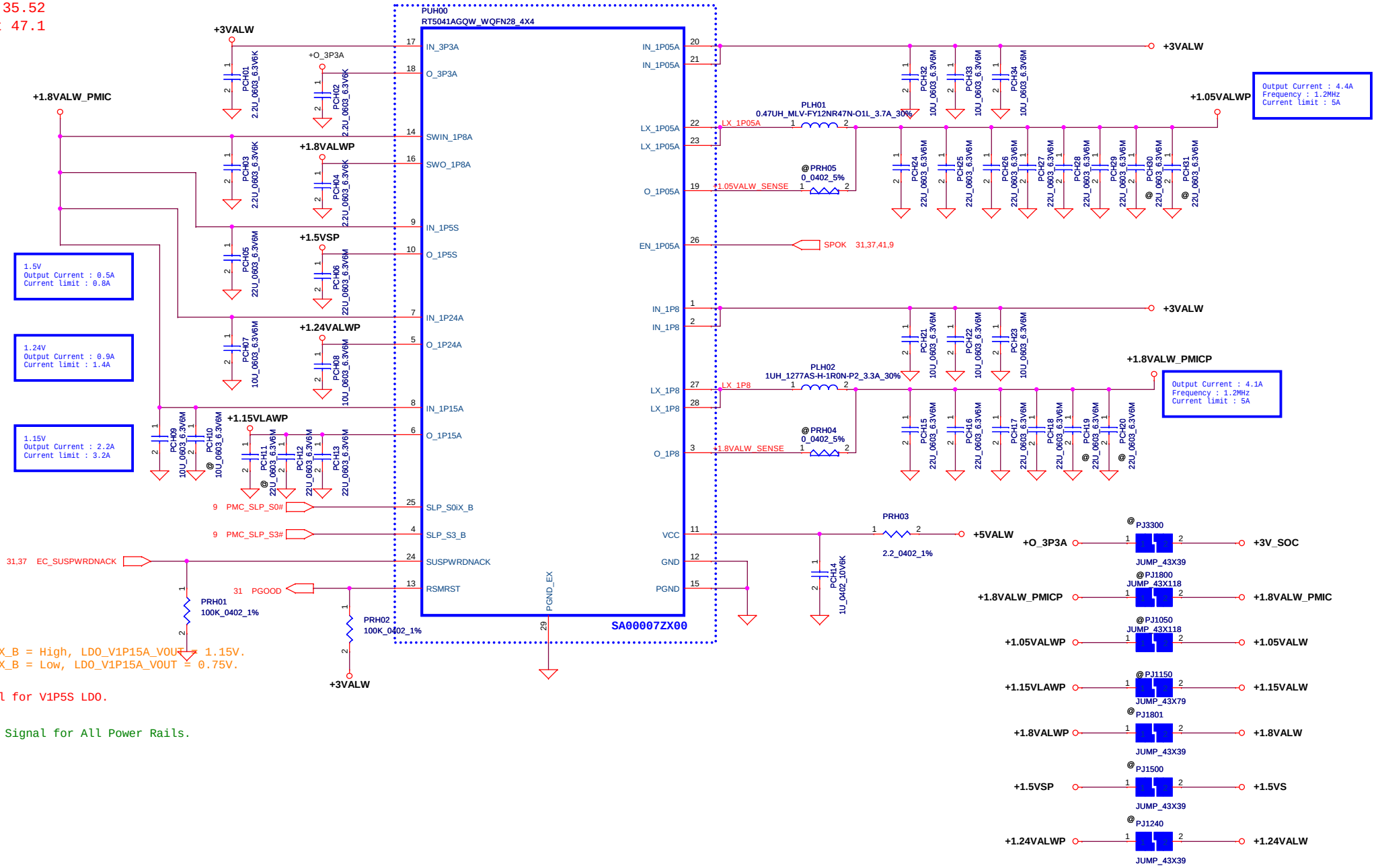
Title: PWR-PROCESSOR DECOUPLING

Size: A3 | Document Number: LA-C706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 45 of 52

Function Field :

Regulator 35.51
Support 35.52
EMI Part 47.1



SLP_S0iX_B
When SLP_S0iX_B = High, LDO_V1P15A_VOUT = 1.15V.
When SLP_S0iX_B = Low, LDO_V1P15A_VOUT = 0.75V.

SLP_S3_B
Enable Signal for V1P5S LDO.

SUSPWRDNACK
HIGH:Disable Signal for All Power Rails.

Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2013/09/17

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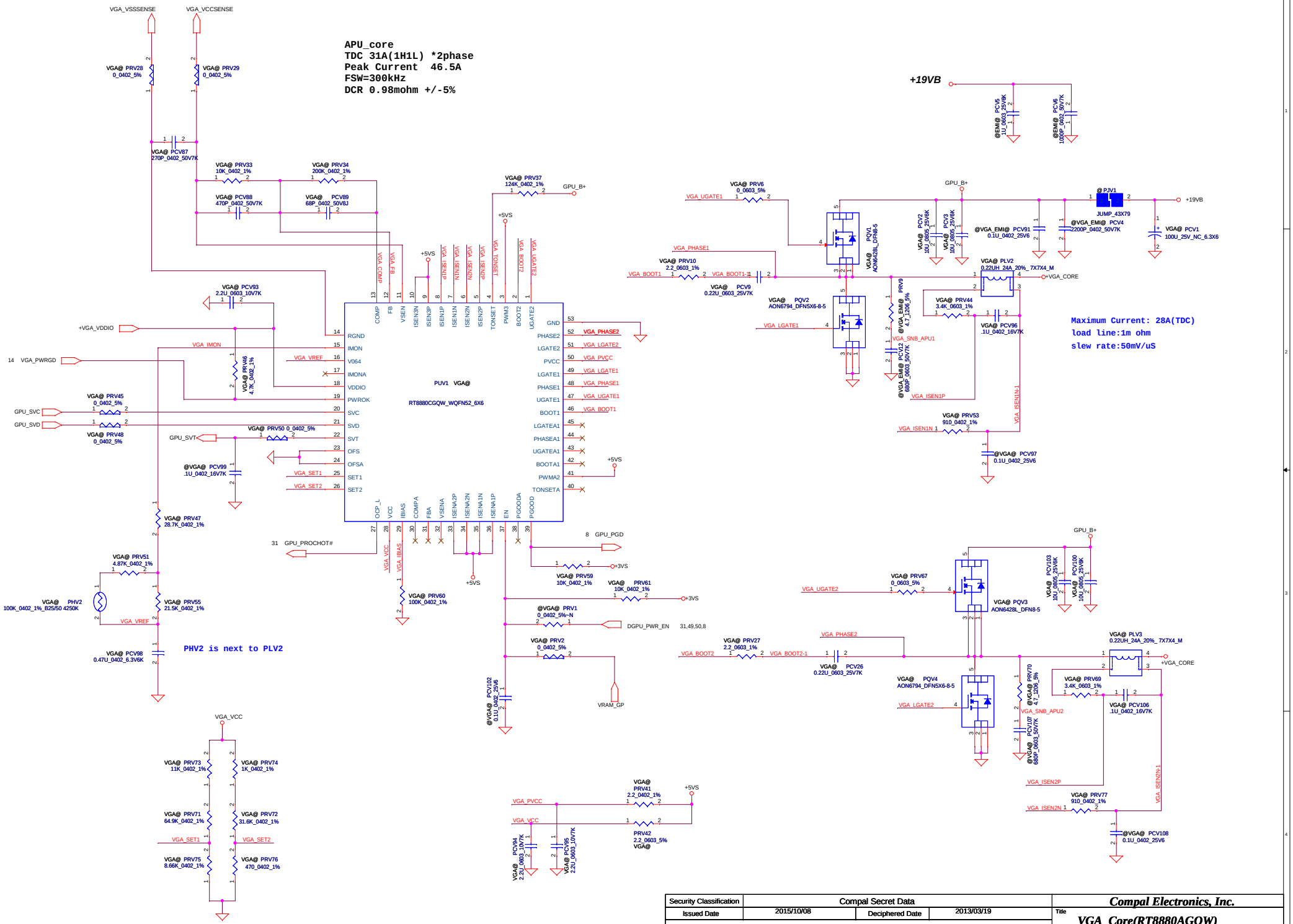
Compal Electronics, Inc.

Title: PWR-MOIC SYSTEM

Size: A3 | Document Number: LA-C706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 46 of 52



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Issued Date	2015/10/08	Deciphered Date	2013/03/19

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Compal Electronics, Inc.

Title: **VGA_Core(RT8880AGQW)**

Size	Document Number	Rev
		0.1

Date: Thursday, January 07, 2016 | Sheet 47 of 52

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2015/10/08	Deciphered Date	2016/09/30	Title: *VGA CHIP DECOUPLING*
				Size: Document Number: LA-C706P — Rev: 0.1
				Date: Thursday, January 07, 2016 — Sheet 48 of 52

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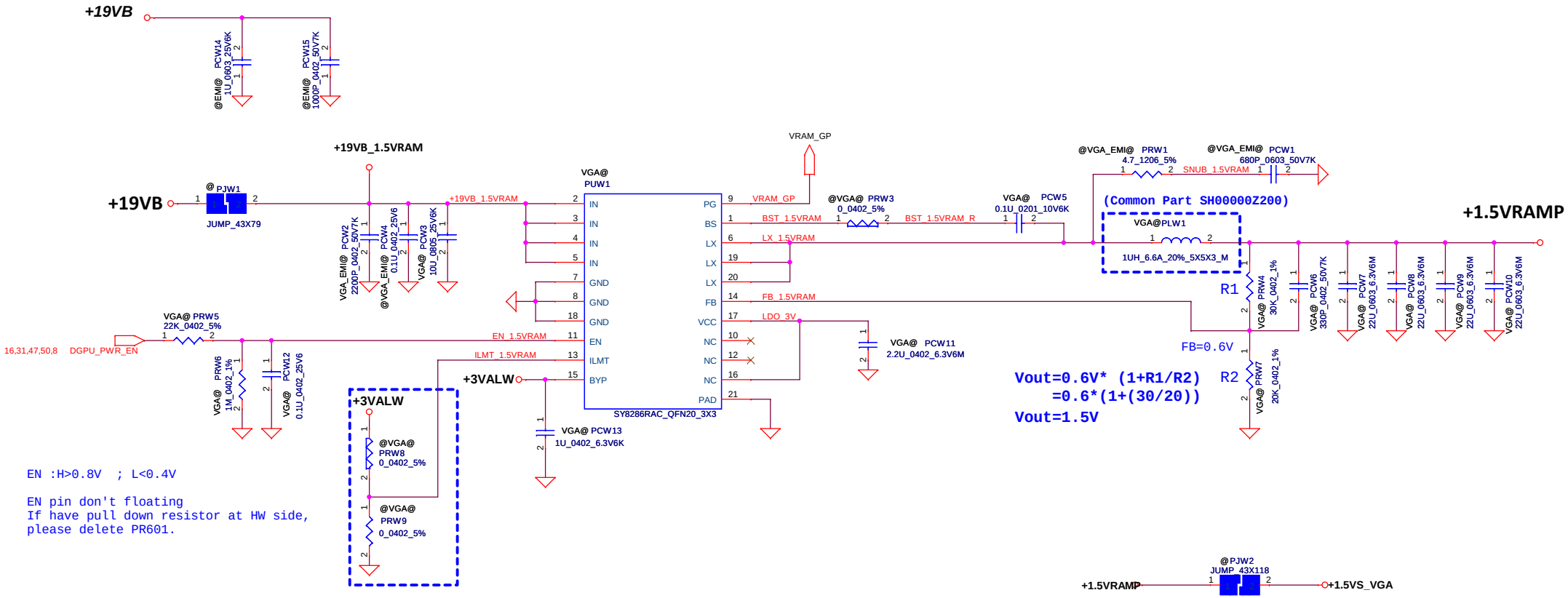
Module model information

SY8286_V1_single.mdd
SY8286_V1_dual.mdd



EN :H>0.8V ; L<0.4V

EN pin don't floating
If have pull down resistor at HW side,
please delete PR601.

The current limit is set to 6A, 9A or 12A when this pin
is pull low, floating or pull high.

Security Classification	Compal Secret Data			APS55 Compal Electronics, Inc.
Issued Date	2015/10/08	Deciphered Date	2014/05/26	Title: VRAM_1V5_GPU
				Size: A3 / Document Number: LA-C706P / Rev: 0.1
				Date: Thursday, January 07, 2016 / Sheet 49 of 52

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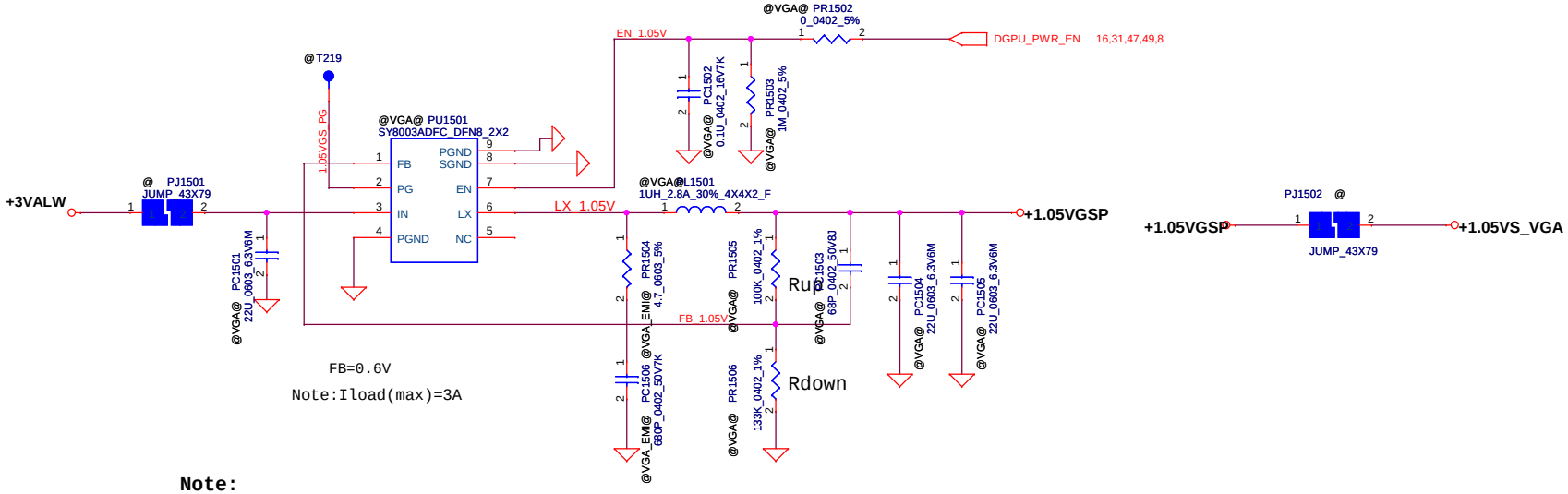
Module model information

SY8003_V2.mdd



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2012/06/13

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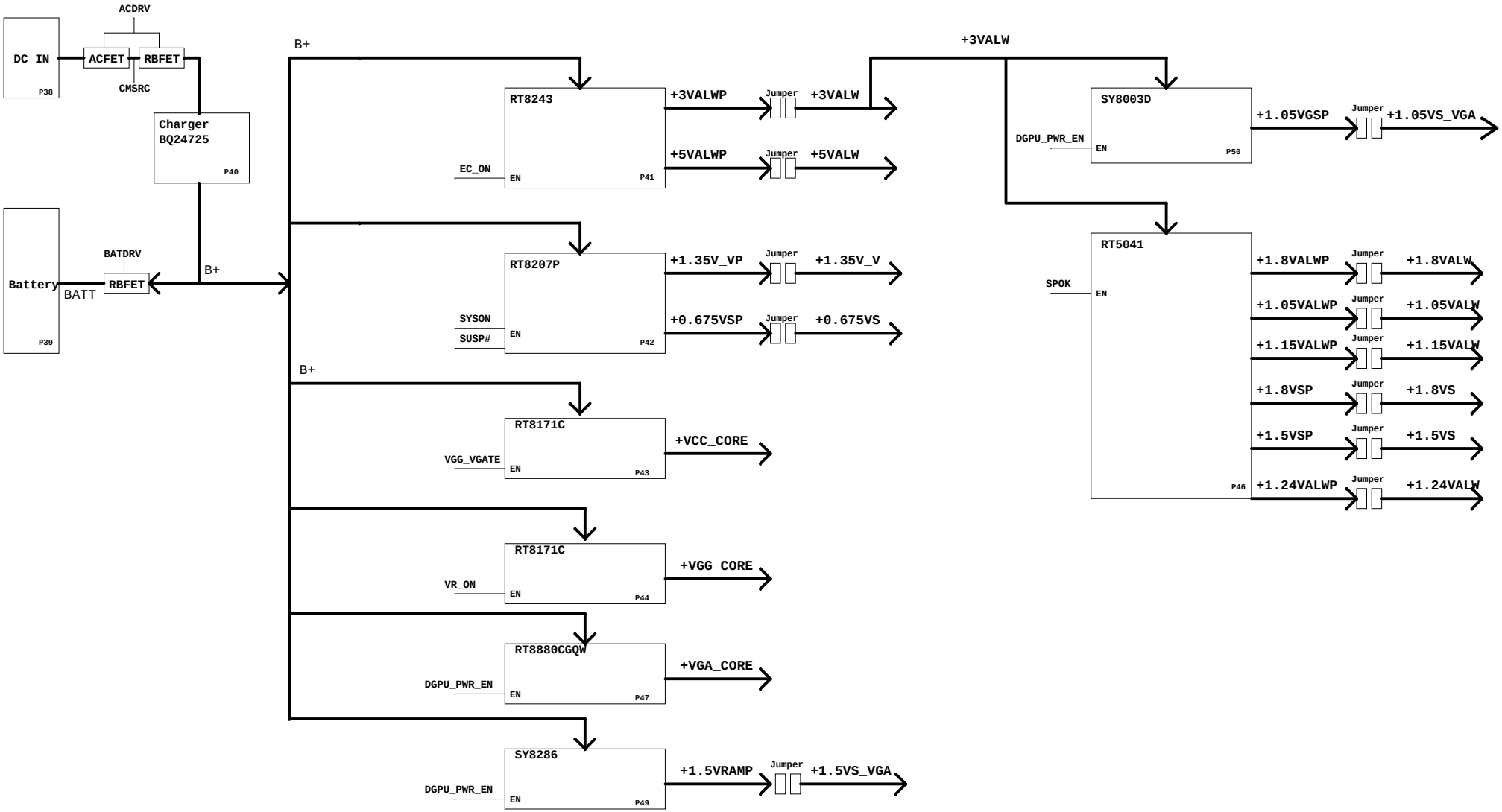
Title: **1.05V(SY8003)**

Size: A3 | Document Number: *Intel / Braswell* | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 50 of 52



Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2014/10/28

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Compal Electronics, Inc.

Title: ***Power Block Diagram***

Size | Document Number: **LA-C706P** | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 51 of 52

Version change list (P.I.R. List)

Item	Date	Page	Reason for change	Modify List	Phase
1	11/16	P47	EE request for VGA power debug	Change PRV61 to stuff & PRV1/PCV102 to Unpop	SI
2	11/16	P47	EE request for VGA power debug	Add PRV2 for EE debug sequence issue	SI
3	11/24	P44	EMI request for debug	remove PJG1 & add PLG301/ PLG302	SI
4	11/24	P52	EE request for VGA power debug	Change PRW5 0 ohm --> 22K & PCW12 0.1U to stuff	SI
5	11/24	P43	EMI request for debug	remove PJZ1 & add PLZ301/ PLZ302	SI
6	12/29	P47	Modify OCP value	Change PRV73 1K-->11K, PRV71 124K-->64.9K PRV75 2.8K-->8.66K	PV
7	12/29	P40,P42	Diner cost down item	Change PCB17, PCM4 0603 to 0402, PCM5 0805 to 0603	PV
8	12/30	P43, P44, P47	Change 0 ohm to short pad	PRZ51, PRG51, PRV28, PRV29, PRV45, PRV48, PRV50, PRV2	PV
9	1/7	P49	Change 0 ohm to short pad	PRW8	PV
10					
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Issued Date	Deciphered Date	Title: PIR List	
		Size: Custom	Document Number: Intel / Braswell	Rev: 0.1
		Date: Thursday, January 07, 2016	Sheet 52 of 52