

LCFC Confidential

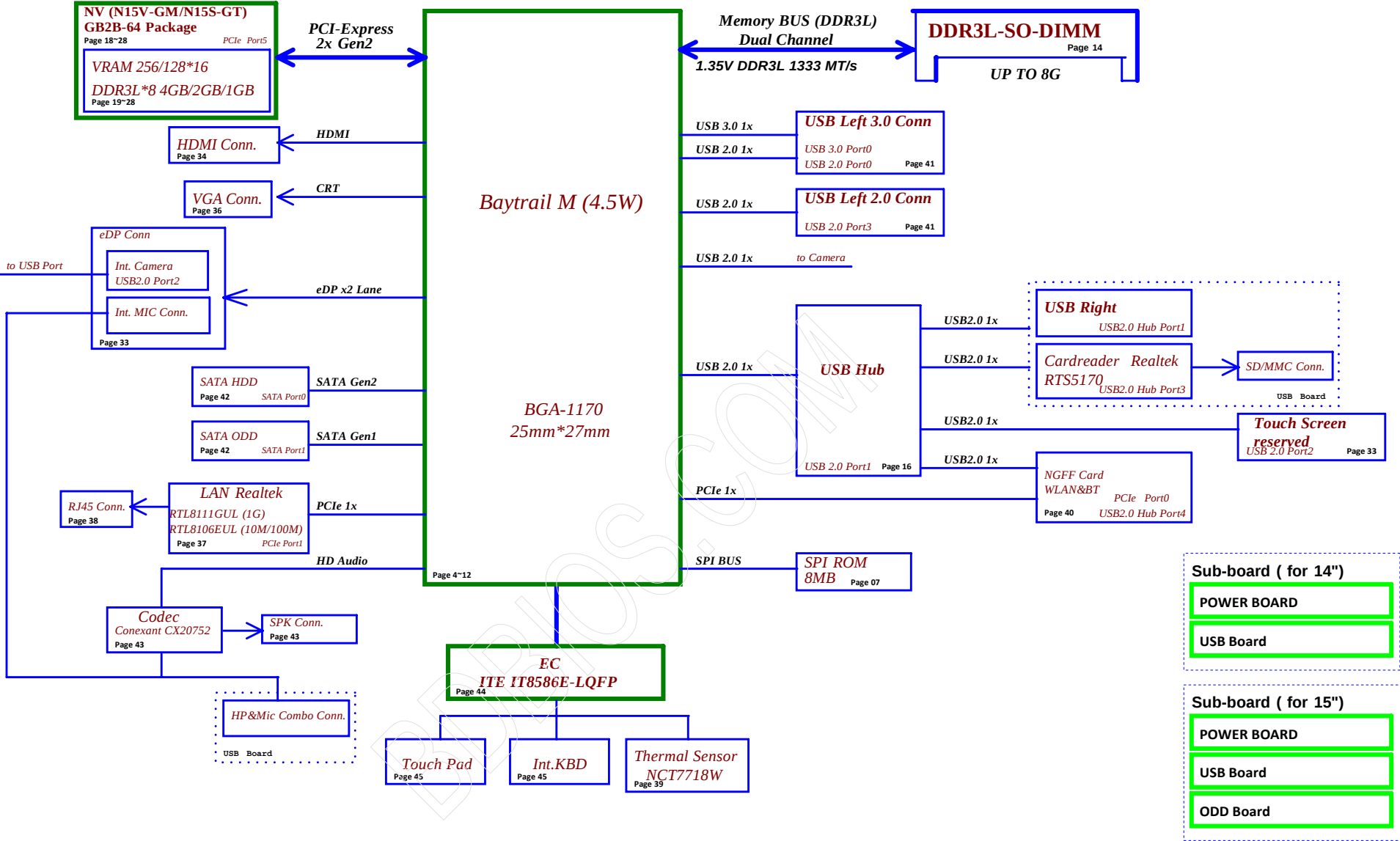
ACLU9 M/B Schematics Document

Intel BayTrail M-Processor with DDRIIL + NV (N15V-GM/N15S-GT) GPU

2013-12-22

REV: 0.2

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Cover Page	
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Power Plane State	B+	+3VALW	+3VALW_SOC +1.0VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS +0.68VS CPU_CORE GFX_CORE
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_PCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB 2.0	USB 3.0	Port	3 External USB Port
EHCI1	XHCI 1	0	USB Port (Left Side)
		1	USB Port (Right Side)
		2	USB Port (Left Side)
		3	USB HUB
USB HUB			
	1	Camera	
	2	Cardreader	
	3	BT(WLAN)	
	4	TOUCH PANEL	

[illegible]

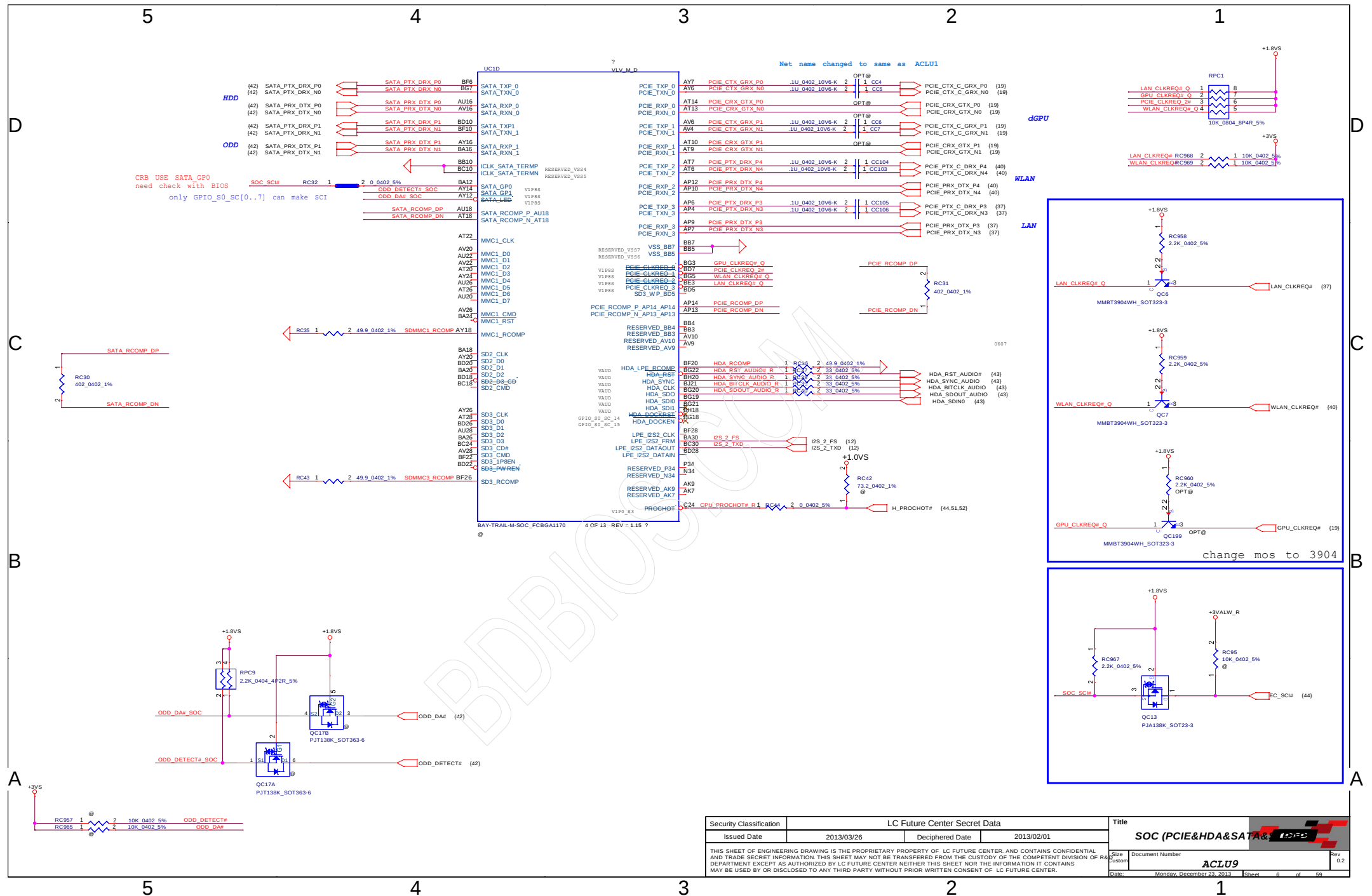
Port	Device
1	Discrete GPU
2	Discrete GPU
3	WLAN
4	LAN
5	
6	
7	
8	

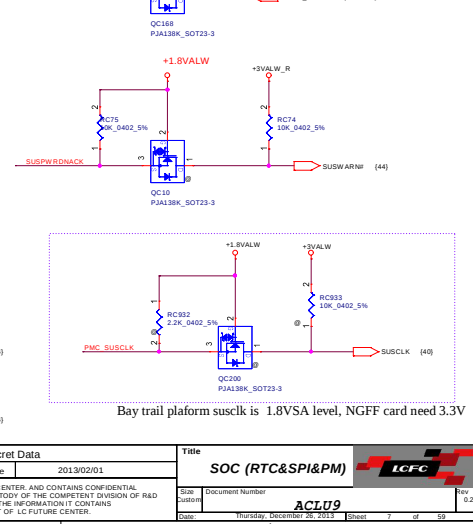
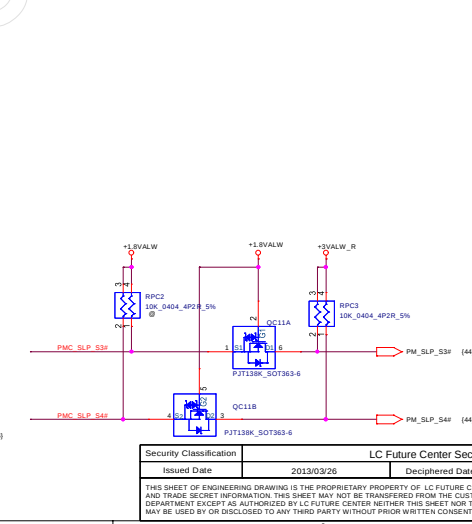
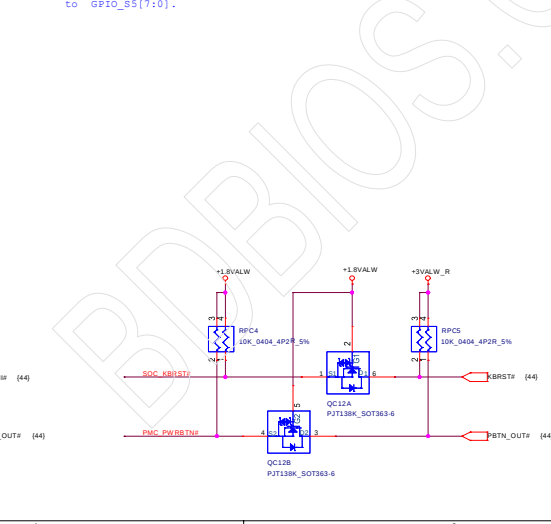
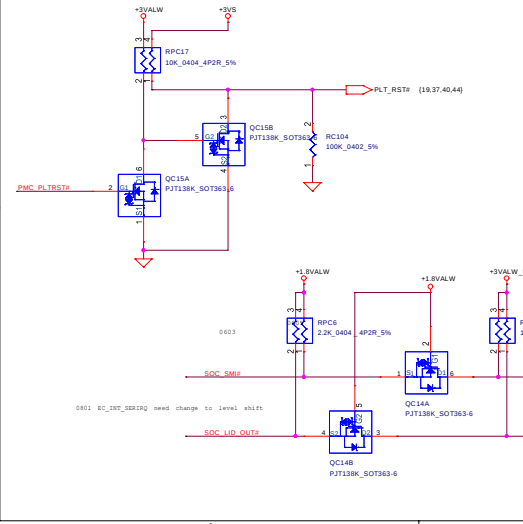
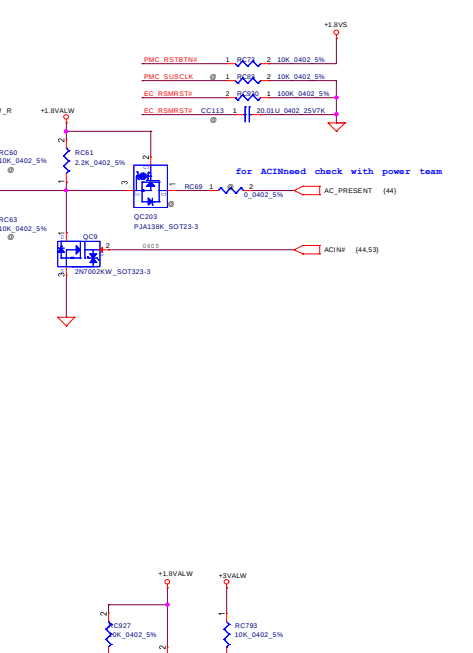
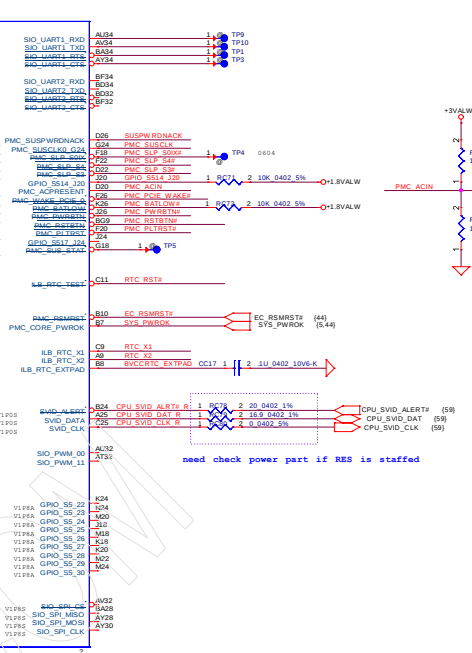
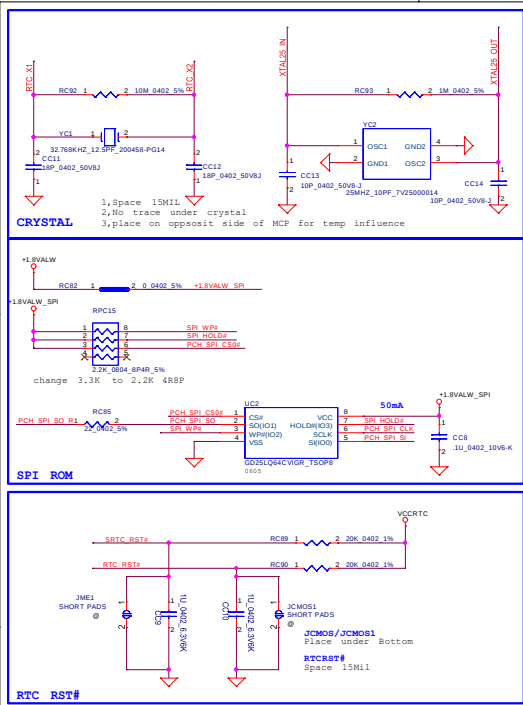
Device	Address
DDR DIMMA	1001 000Xb
Wlan	Rsvd
TP	need to update

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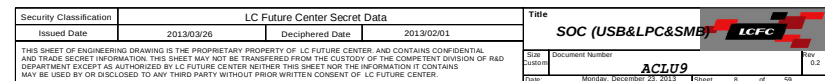
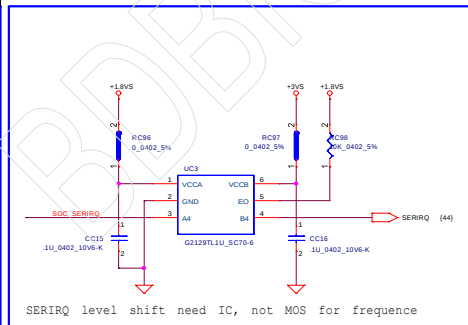


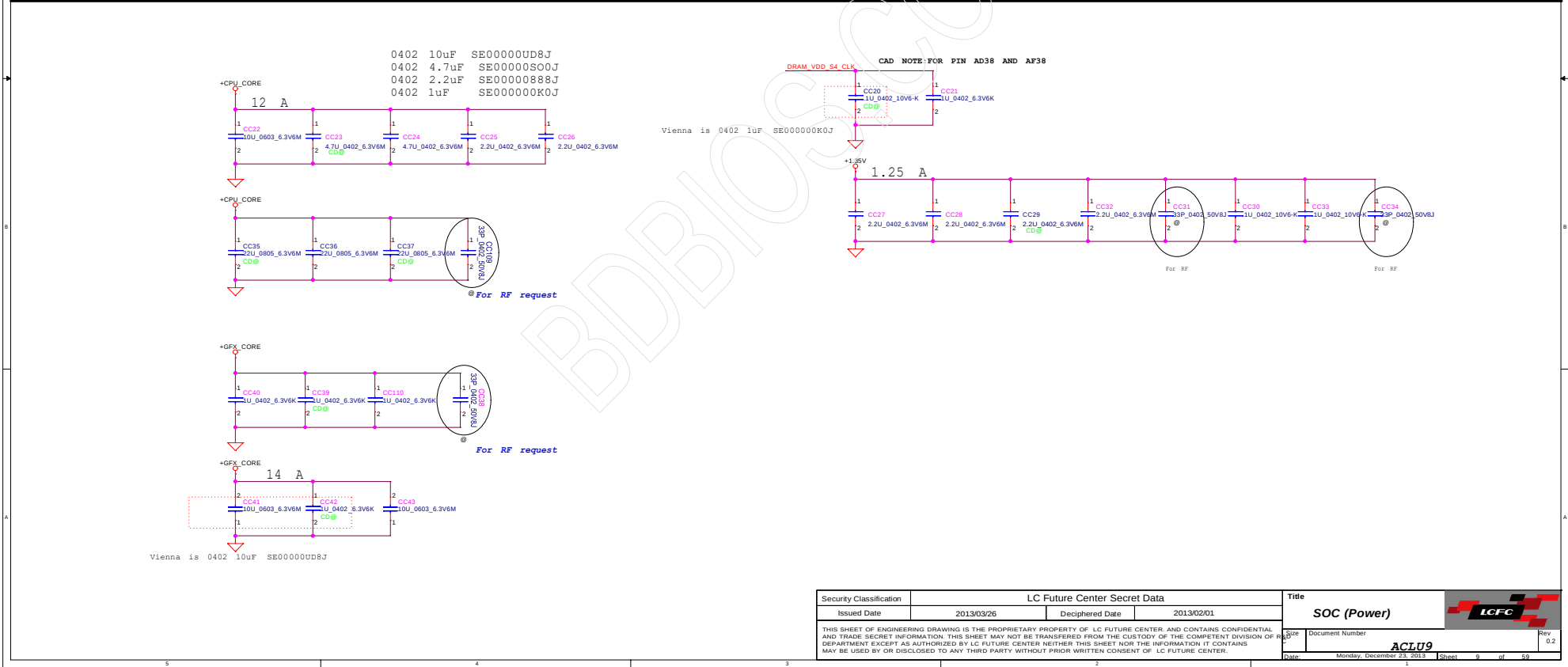
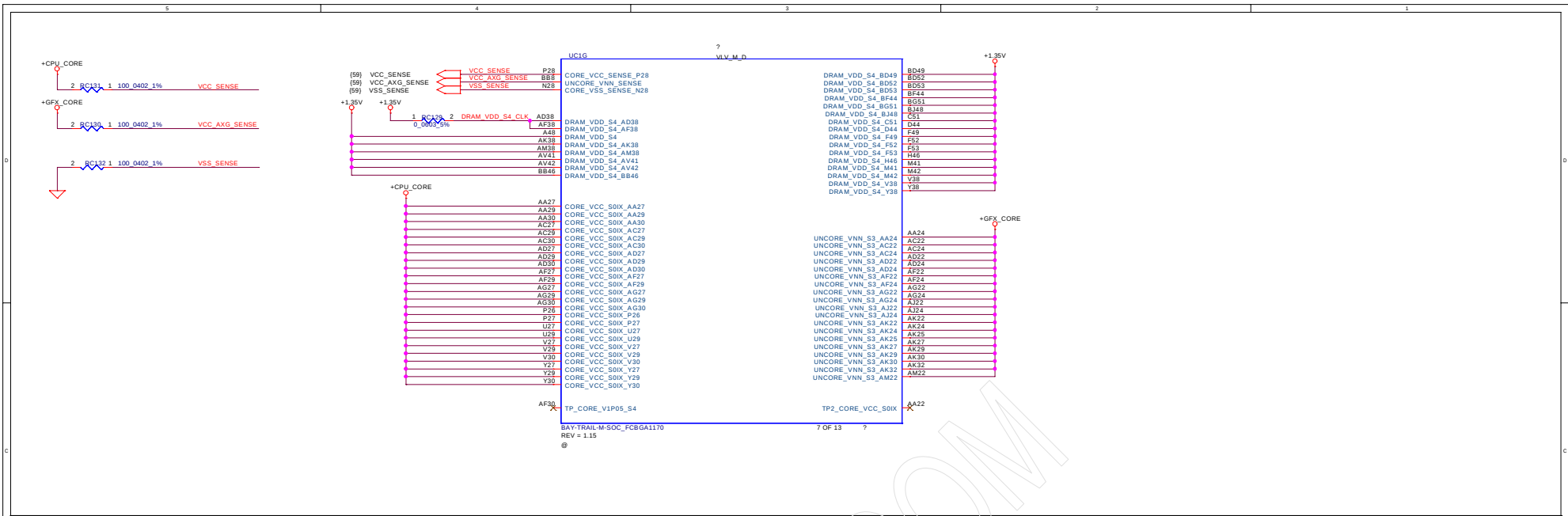


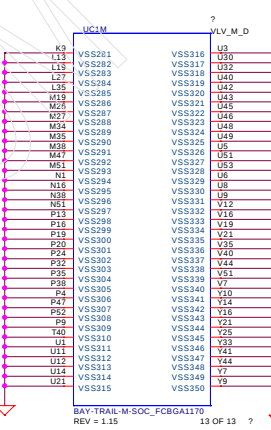
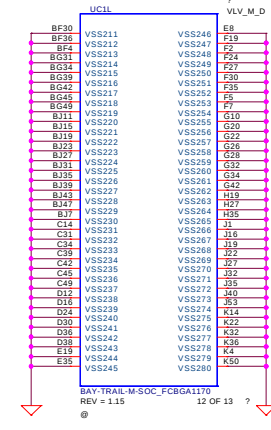
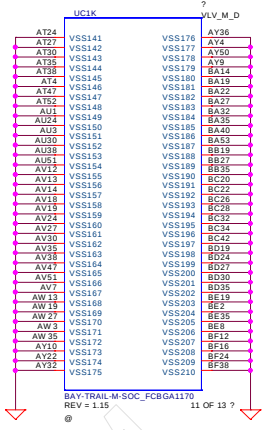
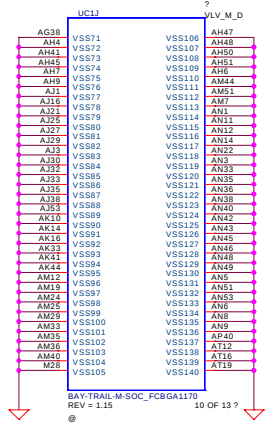
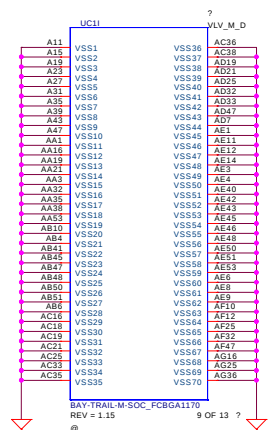


The ALT_GPIO_SMI.CORE_GPIO_SMI_STS[31:24] & ALT_GPIO_SMI.CORE_GPIO_SMI_STS[23:16] & ALT_GPIO_SMI.SUS_GPIO_SMI_STS[7:0] correspond to GPIO_S5[7:0].

Security Classification			LC Future Center Secret Data		Title	
Issued Date	2013/03/26	Deciphered Date	2013/02/01		SOC (RTC&SPI&PM)	
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Hardware STRAPS (Follow up CRB& VIENNA)

GPIO_NC13
GPIO_S0_SC_56
I2S_2_FS
I2S_2_TXD
PCH_HDMI_DDC_DAT
DDI0_DDCDATA

MDSI_DDCDATA(Checklist request 10K pull down)
GPIO_S0_SC_56(Internal Pull-up)
GPIO_S0_SC[063] (Internal Pull-up)
GPIO_S0_SC[065] (Internal Pull-up)
DDI1_DDCDATA
DDI0_DDCDATA

GPIO_S0_SC_56:

A16 Top Swap

0=Top address bit is unchanged

1=Top address bit is inverted

GPIO_S0_SC[063]

Multiplexed with Hardware Straps Pin LPE_I2S2_FRM

BIOS Boot selection

0=LPC

1=SPI

GPIO_S0_SC[065]

Multiplexed with LPE_I2S2_DATAOUT

Security Flash Descriptors

0=Override

1=Normal Operation

DDI0_DDCDATA:

DDI0 strap

0=DDI0 not detected

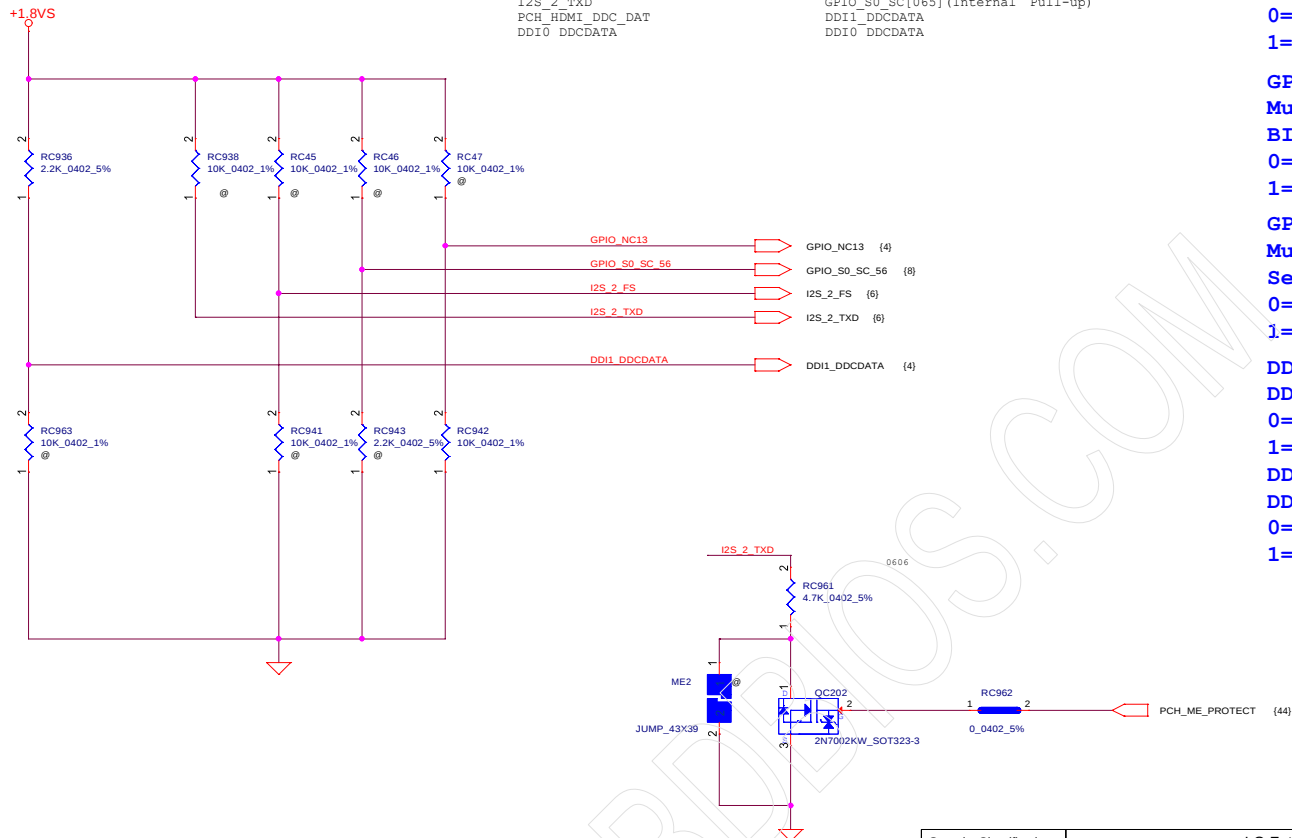
1=DDI0 detected

DDI1_DDCDATA:

DDI1 strap

0=DDI1 not detected

1=DDI1 detected



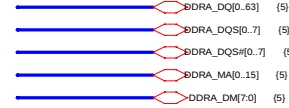
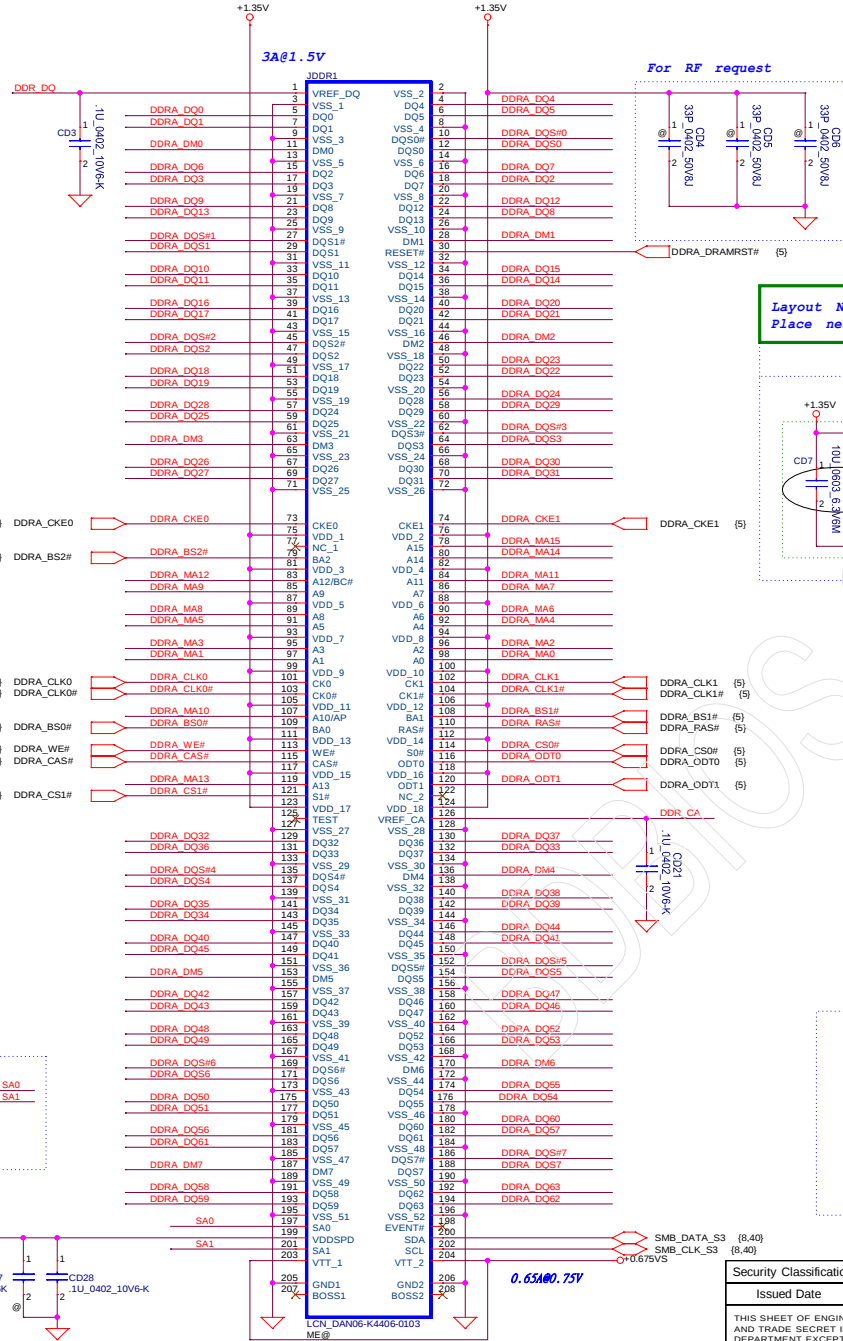
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DDR Mapping table

DDRA_DQ0---DQ0
 DDRA_DQ1---DQ1
 DDRA_DQ6---DQ2
 DDRA_DQ3---DQ3
 DDRA_DQ4---DQ4
 DDRA_DQ5---DQ5
 DDRA_DQ7---DQ6
 DDRA_DQ2---DQ7
 DDRA_DQ9---DQ8
 DDRA_DQ13---DQ9
 DDRA_DQ10---DQ10
 DDRA_DQ11---DQ11
 DDRA_DQ12---DQ12
 DDRA_DQ8---DQ13
 DDRA_DQ15---DQ14
 DDRA_DQ14---DQ15
 DDRA_DQ16---DQ16
 DDRA_DQ17---DQ17
 DDRA_DQ18---DQ18
 DDRA_DQ19---DQ19
 DDRA_DQ20---DQ20
 DDRA_DQ21---DQ21
 DDRA_DQ22---DQ22
 DDRA_DQ23---DQ23
 DDRA_DQ24---DQ24
 DDRA_DQ25---DQ25
 DDRA_DQ26---DQ26
 DDRA_DQ27---DQ27
 DDRA_DQ28---DQ28
 DDRA_DQ29---DQ29
 DDRA_DQ30---DQ30
 DDRA_DQ31---DQ31
 DDRA_DQ32---DQ32
 DDRA_DQ33---DQ33
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 DDRA_DQ36---DQ36
 DDRA_DQ37---DQ37
 DDRA_DQ38---DQ38
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 DDRA_DQ42---DQ42
 DDRA_DQ43---DQ43
 DDRA_DQ44---DQ44
 DDRA_DQ45---DQ45
 DDRA_DQ46---DQ46
 DDRA_DQ47---DQ47
 DDRA_DQ48---DQ48
 DDRA_DQ49---DQ49
 DDRA_DQ50---DQ50
 DDRA_DQ51---DQ51
 DDRA_DQ52---DQ52
 DDRA_DQ53---DQ53
 DDRA_DQ54---DQ54
 DDRA_DQ55---DQ55
 DDRA_DQ56---DQ56
 DDRA_DQ57---DQ57
 DDRA_DQ58---DQ58
 DDRA_DQ59---DQ59
 DDRA_DQ60---DQ60
 DDRA_DQ61---DQ61
 DDRA_DQ62---DQ62
 DDRA_DQ62---DQ63

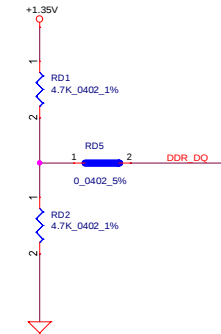
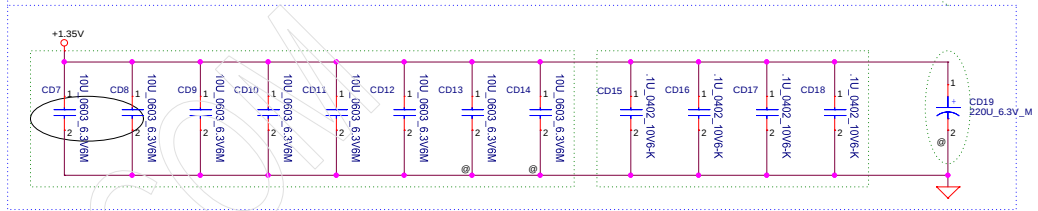
DDR3 SO-DIMM A



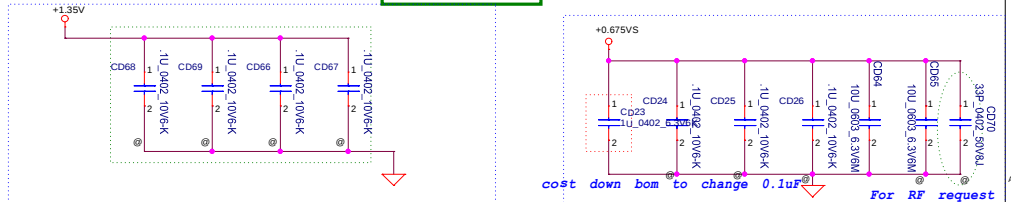
OSCON (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)

(10uF_0603_6.3V)*8
 (0.1uF_402_10V)*4

Layout Note: Place near DIMM

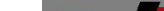


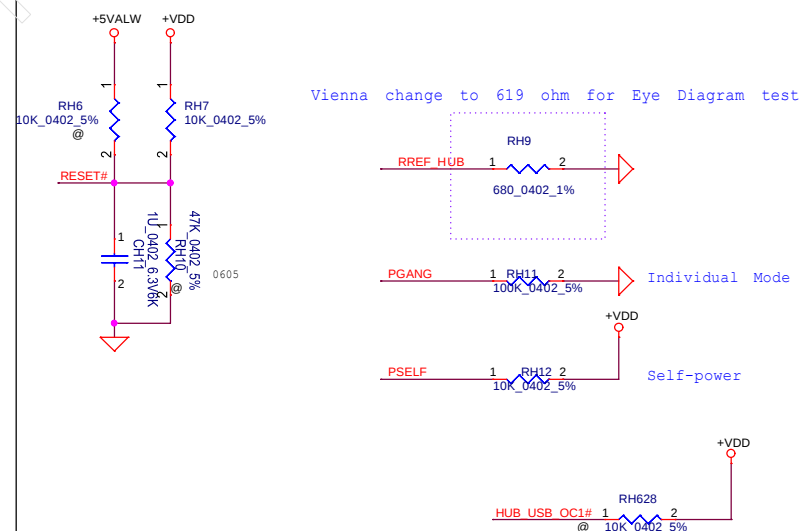
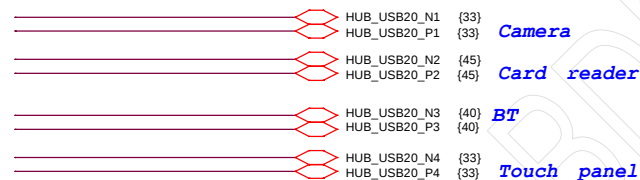
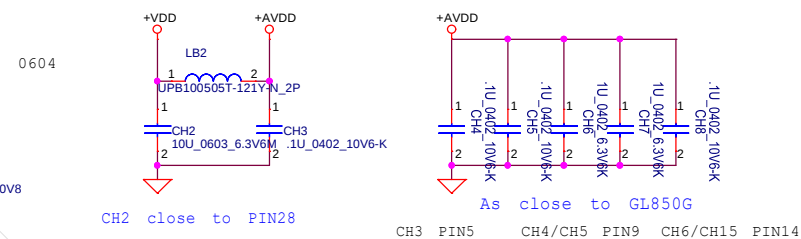
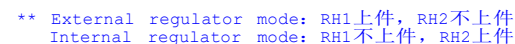
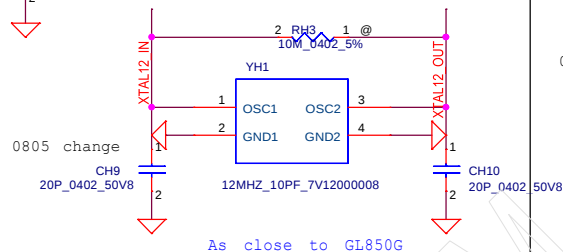
Layout Note: Place near DIMM



cost down bom to change 0.1uF For RF request

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						DDRIII SO-DIMM B	
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N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

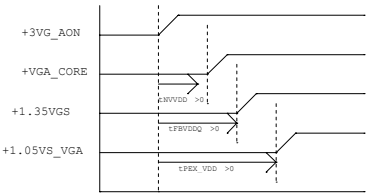
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

N15x Multi-level Straps

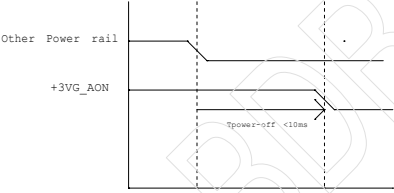
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15V-GM Power Sequence

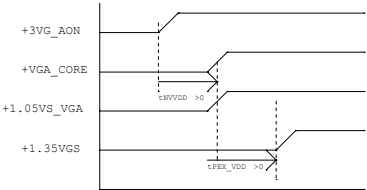


1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimum system VDD3 avoids drop down earlier than NVDD and FBVDDQ

N15S-GT Power Sequence

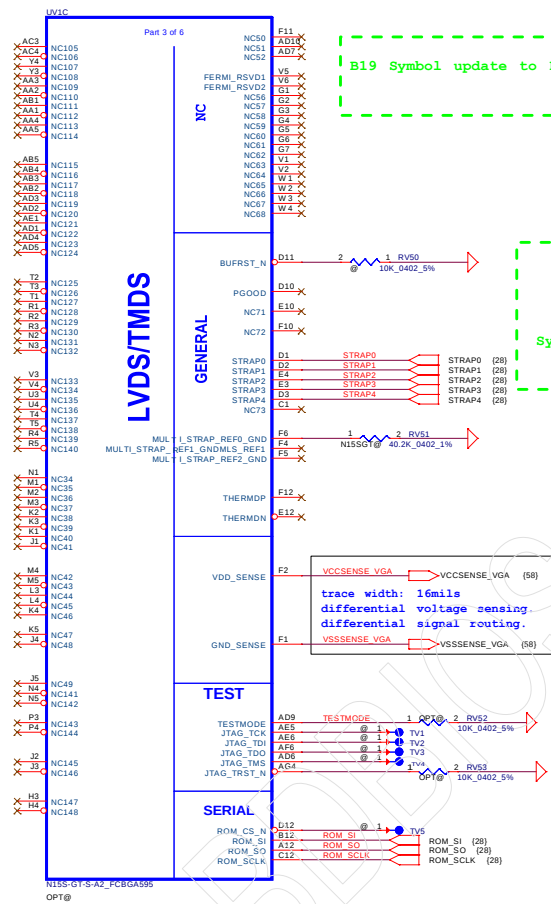


1. all power rail ramp up time should be larger than 40us

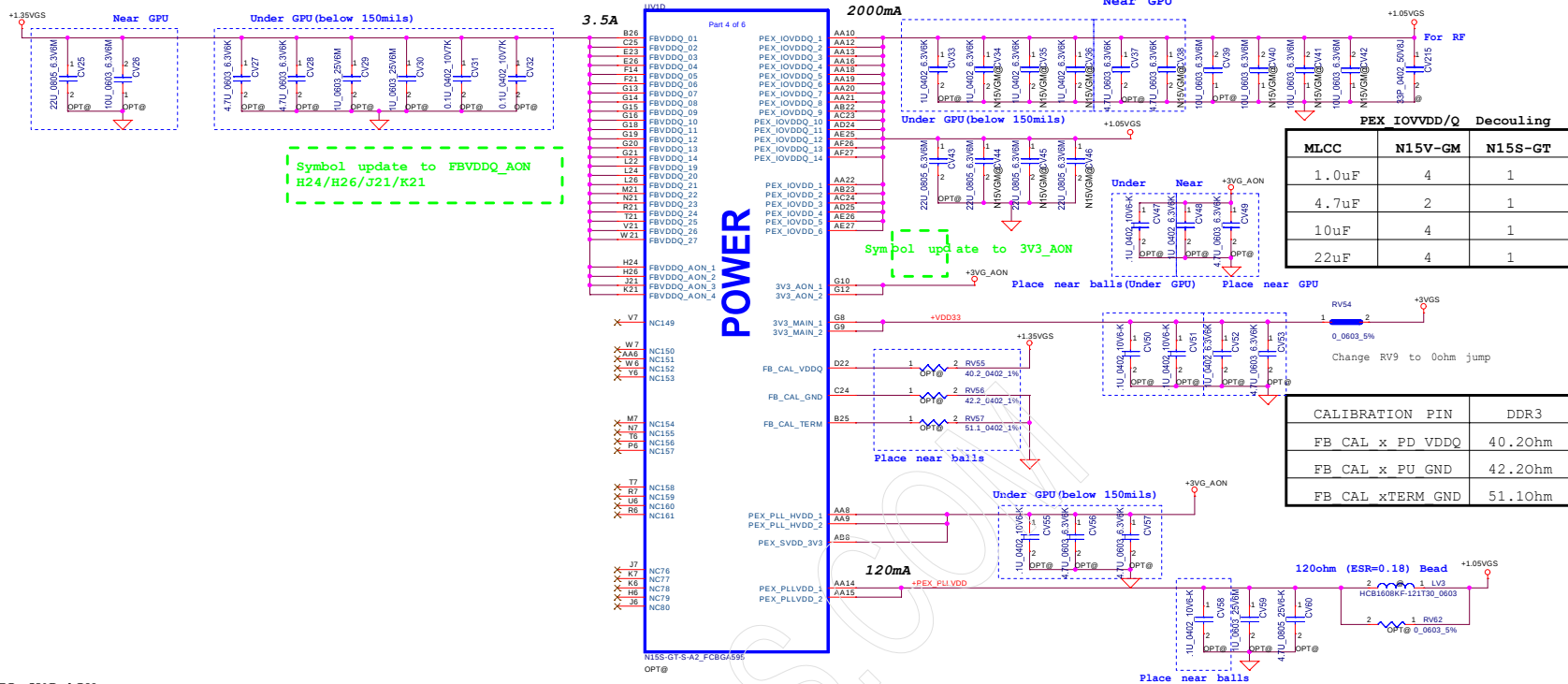
N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

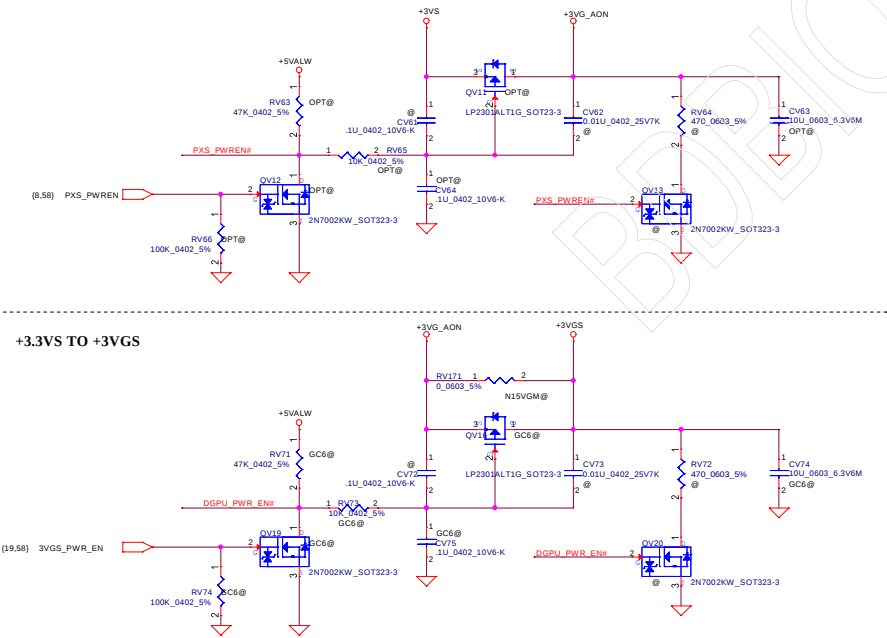
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	VGA Notes List	
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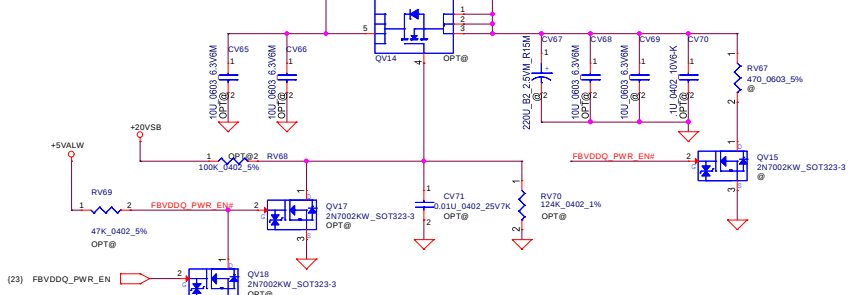
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Rev C		Document Number		ACLU9				Rev 0.2		
Date		Monday, December 23, 2013		Sheet		20		of 52		

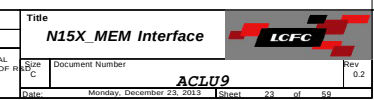


+3.3VS TO +3VGS_AON

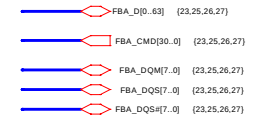
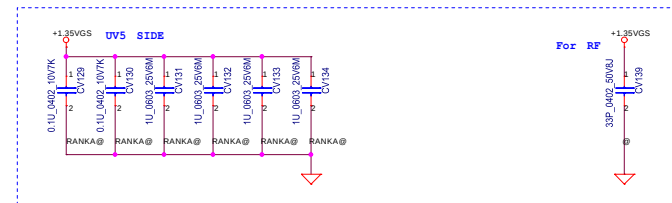
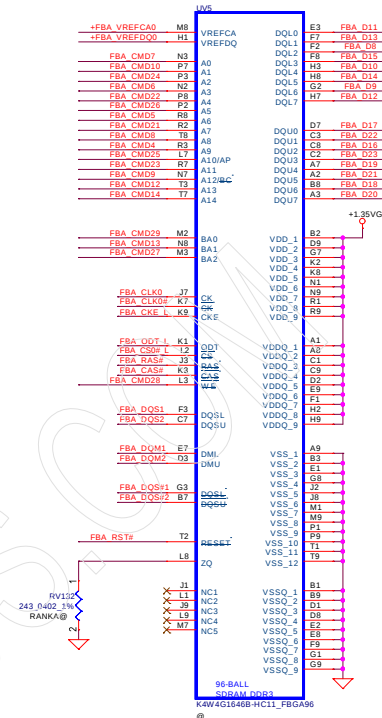
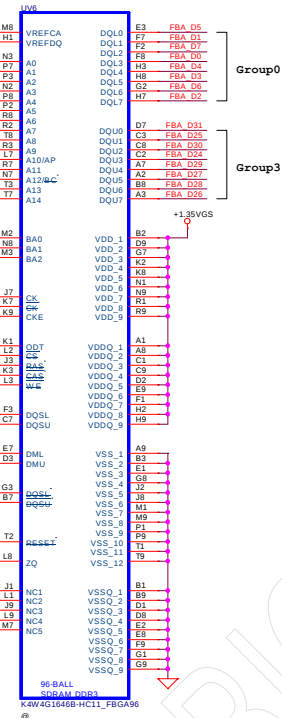
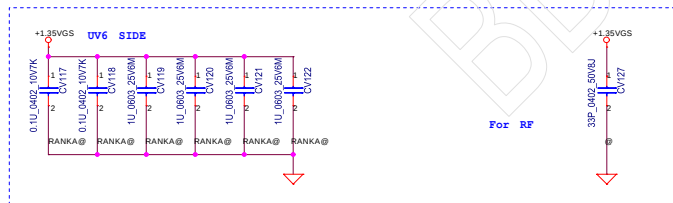
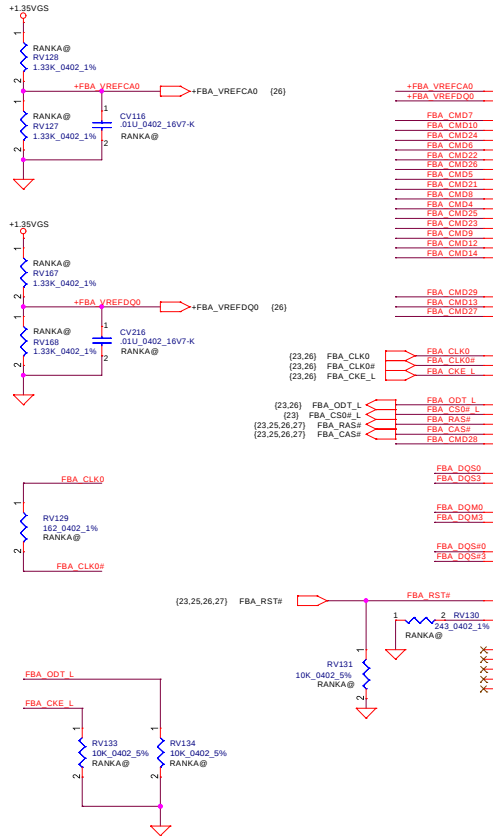


+1.35V TO +1.35VGS





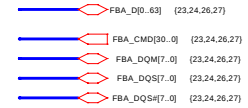
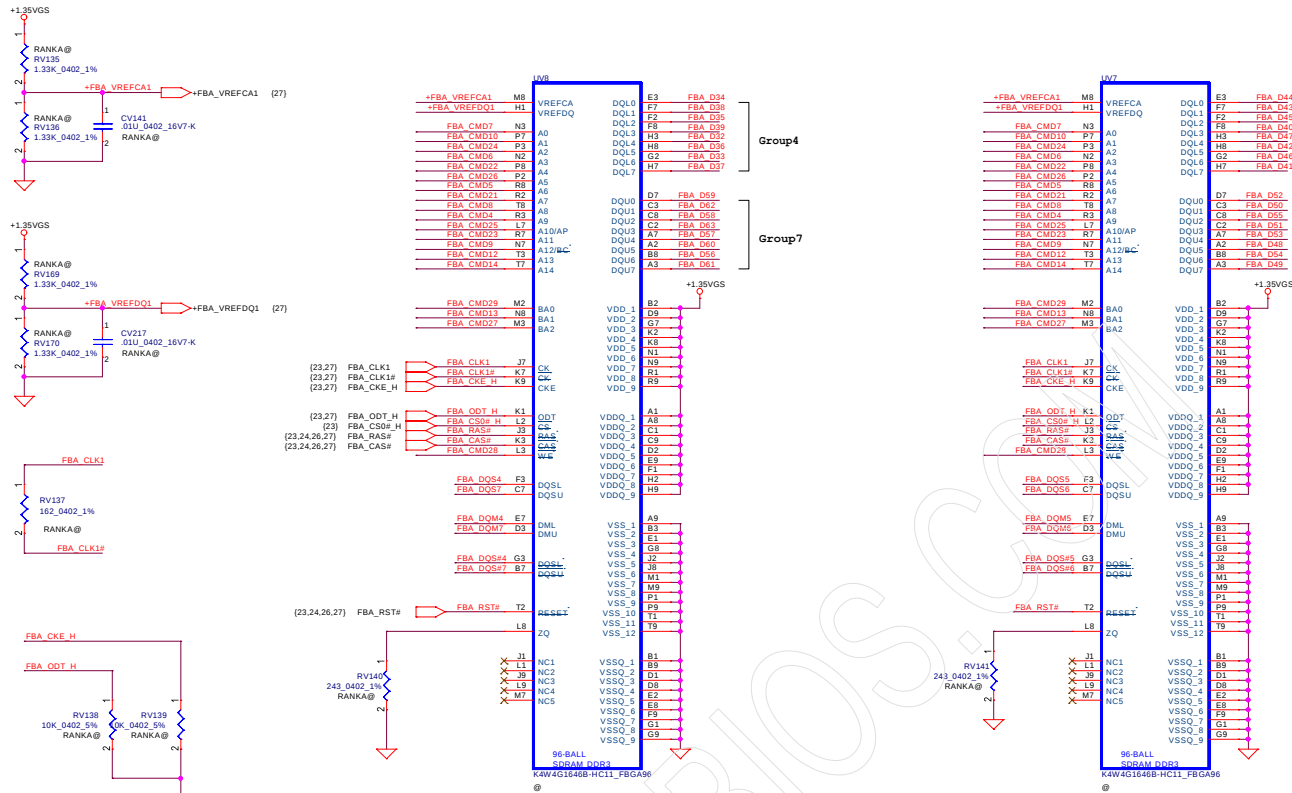
at least 16 mils width(optimal)
20 mils spacing to other signals /planes



CMD mapping mod Mode E

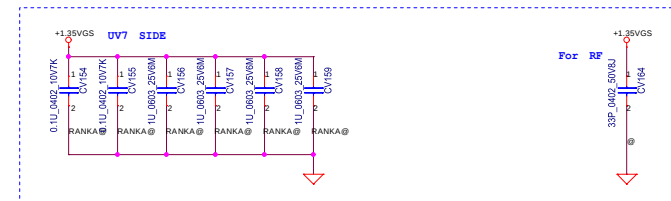
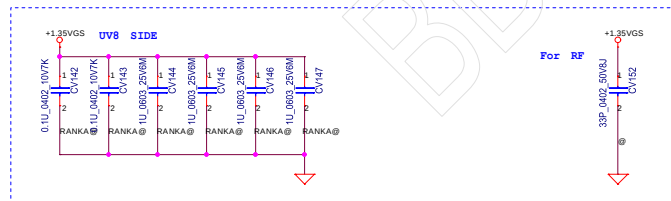
	Rank0	Rank1
Address	0..31	32..63
FBx_CMD0	ODT_L	ODT_L
FBx_CMD1		CS1#_L
FBx_CMD2	CS0#_L	
FBx_CMD3	CKE_L	CKE_L
FBx_CMD4	A9	A11
FBx_CMD5	A6	A7
FBx_CMD6	A3	BA1
FBx_CMD7	A0	A12
FBx_CMD8	A8	A8
FBx_CMD9	A12	A0
FBx_CMD10	A1	A2
FBx_CMD11	RAS#	RAS#
FBx_CMD12	A13	A14
FBx_CMD13	BA1	A3
FBx_CMD14	A14	A13
FBx_CMD15	CAS#	CAS#
FBx_CMD16	ODT_H	ODT_H
FBx_CMD17		CS1#_H
FBx_CMD18	CS0#_H	
FBx_CMD19	CKE_H	CKE_H
FBx_CMD20	RST	RST
FBx_CMD21	A7	A6
FBx_CMD22	A4	A5
FBx_CMD23	A11	A9
FBx_CMD24	A2	A1
FBx_CMD25	A10	WE#
FBx_CMD26	A5	A4
FBx_CMD27	BA2	
FBx_CMD28	WE#	A10
FBx_CMD29	BA0	BA0
FBx_CMD30		BA2

at least 16 mils width(optimal)
20 mils spacing to other signals/planes

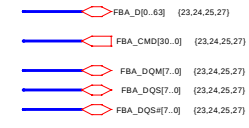
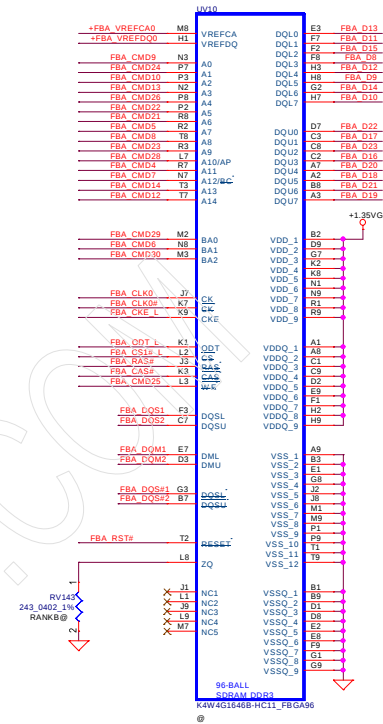
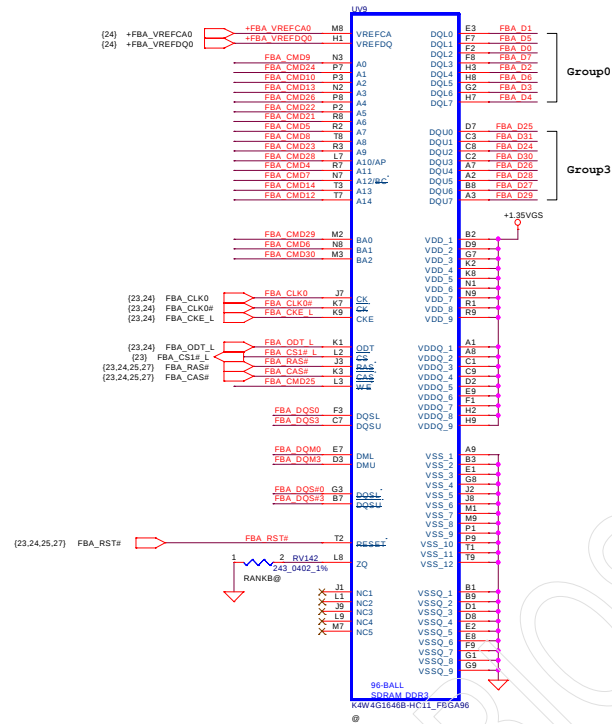


CMD mapping mod Mode E

Address	Rank0	Rank1
FBx_CMD0	0..31	0..31
FBx_CMD1	ODT_L	ODT_L
FBx_CMD2	CS0#_L	CS1#_L
FBx_CMD3	CKE_L	CKE_L
FBx_CMD4	A9	A11
FBx_CMD5	A6	A7
FBx_CMD6	A3	BA1
FBx_CMD7	A0	A12
FBx_CMD8	A8	A8
FBx_CMD9	A12	A0
FBx_CMD10	A1	A2
FBx_CMD11	RAS#	RAS#
FBx_CMD12	A13	A14
FBx_CMD13	BA1	A3
FBx_CMD14	A14	A13
FBx_CMD15	CAS#	CAS#
FBx_CMD16	ODT_H	ODT_H
FBx_CMD17		CS1#_H
FBx_CMD18	CS0#_H	
FBx_CMD19	CKE_H	CKE_H
FBx_CMD20	RST	RST
FBx_CMD21	A7	A6
FBx_CMD22	A4	A5
FBx_CMD23	A11	A9
FBx_CMD24	A2	A1
FBx_CMD25	A10	WE#
FBx_CMD26	A5	A4
FBx_CMD27	BA2	
FBx_CMD28	WE#	A10
FBx_CMD29	BA0	BA0
FBx_CMD30		BA2



at least 16 mils width(optimal)
20 mils spacing to other signals /planes

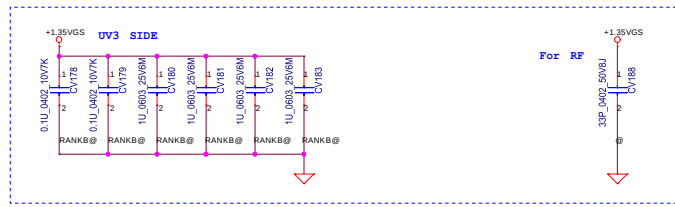
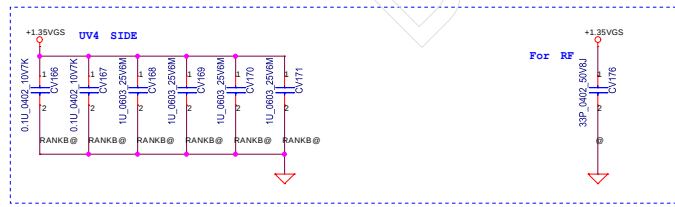


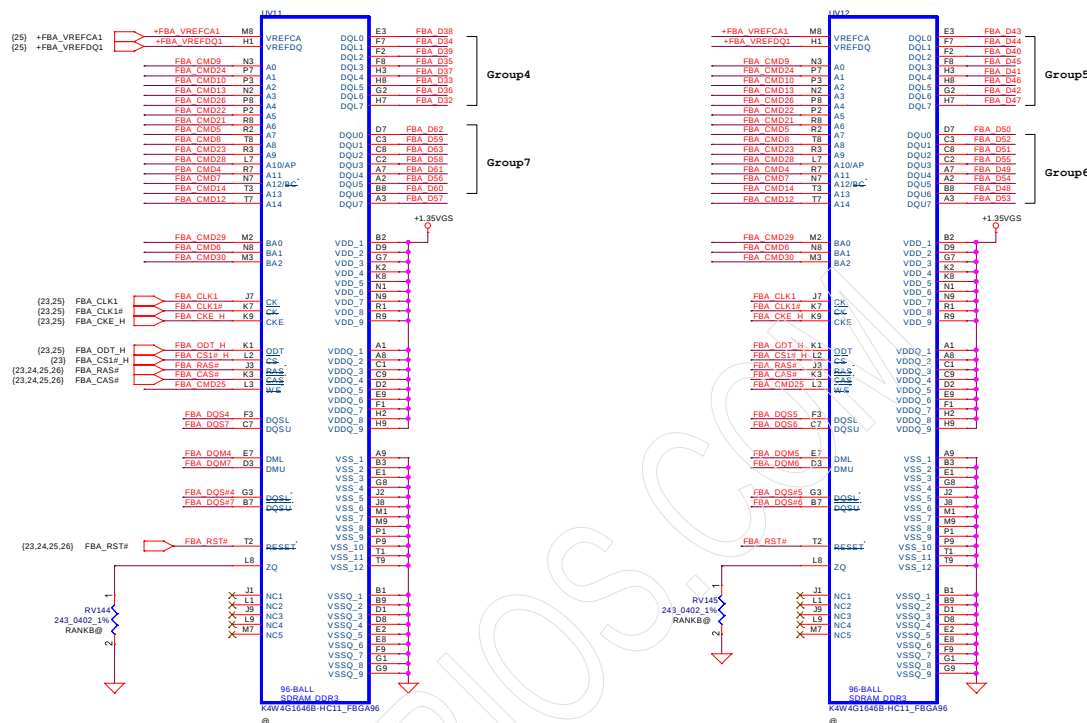
Group1

Group2

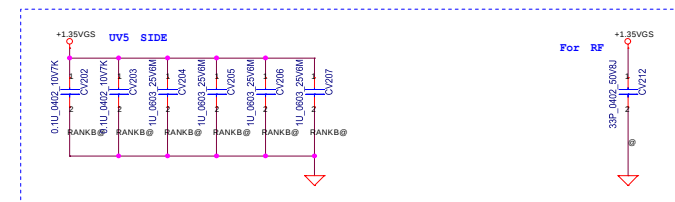
CMD mapping mod Mode E

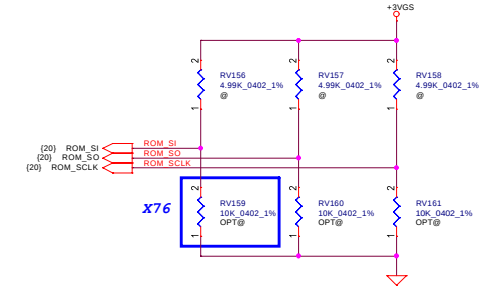
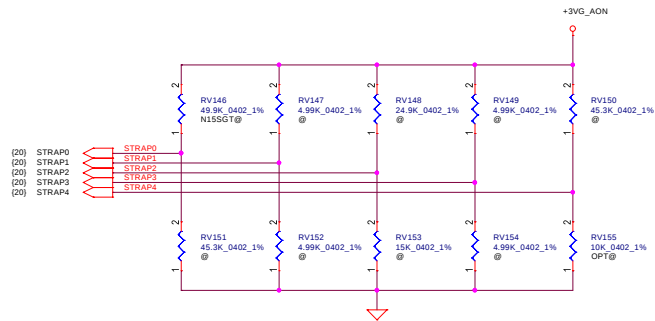
Address	Rank0	Rank1
FBx_CMD0	0..31	32..63
FBx_CMD1	ODT_L	ODT_L
FBx_CMD2	CS0#_L	CS1#_L
FBx_CMD3	CKE_L	CKE_L
FBx_CMD4	A9	A9
FBx_CMD5	A6	A6
FBx_CMD6	A3	A3
FBx_CMD7	A0	A0
FBx_CMD8	A8	A8
FBx_CMD9	A12	A12
FBx_CMD10	A1	A1
FBx_CMD11	RAS#	RAS#
FBx_CMD12	A13	A13
FBx_CMD13	BA1	BA1
FBx_CMD14	A14	A14
FBx_CMD15	CAS#	CAS#
FBx_CMD16	ODT_H	ODT_H
FBx_CMD17		CS1#_H
FBx_CMD18	CS0#_H	
FBx_CMD19	CKE_H	CKE_H
FBx_CMD20	RST	RST
FBx_CMD21	A7	A7
FBx_CMD22	A4	A4
FBx_CMD23	A11	A11
FBx_CMD24	A2	A2
FBx_CMD25	A10	A10
FBx_CMD26	A5	A5
FBx_CMD27	BA2	BA2
FBx_CMD28	WE#	WE#
FBx_CMD29	BA0	BA0
FBx_CMD30		





	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
FBX_CMD0	ODT_L		ODT_L	
FBX_CMD1			CS1#_L	
FBX_CMD2	CS0#_L			
FBX_CMD3	CKE_L		CKE_L	
FBX_CMD4	A9	A9	A11	A11
FBX_CMD5	A6	A6	A7	A7
FBX_CMD6	A3	A3	BA1	BA1
FBX_CMD7	A0	A0	A12	A12
FBX_CMD8	A8	A8	A8	A8
FBX_CMD9	A12	A12	A0	A0
FBX_CMD10	A1	A1	A2	A2
FBX_CMD11	RAS#	RAS#	RAS#	RAS#
FBX_CMD12	A13	A13	A14	A14
FBX_CMD13	BA1	BA1	A3	A3
FBX_CMD14	A14	A14	A13	A13
FBX_CMD15	CAS#	CAS#	CAS#	CAS#
FBX_CMD16		ODT_H		ODT_H
FBX_CMD17			CS1#_H	
FBX_CMD18	CS0#_H			
FBX_CMD19		CKE_H		CKE_H
FBX_CMD20	RST	RST	RST	RST
FBX_CMD21	A7	A7	A6	A6
FBX_CMD22	A4	A4	A5	A5
FBX_CMD23	A11	A11	A9	A9
FBX_CMD24	A2	A2	A1	A1
FBX_CMD25	A10	A10	WE#	WE#
FBX_CMD26	A5	A5	A4	A4
FBX_CMD27	BA2	BA2		
FBX_CMD28	WE#	WE#	A10	A10
FBX_CMD29	BA0	BA0	BA0	BA0
FBX_CMD30			BA2	BA2





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
SD03448918J		
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
SD03448928J		
30.1K	1101	0101
SD03440128J		
34.8K	1110	0110
SD03448928J		
45.3K	1111	0111
SD03445328J		

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

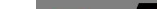
X76

GPU	FB Memory (DDR3)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N15S-GT	H5TC4G63AFR-11C	0x3	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
	256M x 16	PD 20K							
	MT41J256M16HA-093G:E	0x4							
	256M x 16	PD 24.9K							
	K4W4G1646D-BC1A	0x5							
	256M x 16	PD 30.1K							

GPU	FB Memory (DDR3)	STRAP3	STRAP2	STRAP1	STRAP0	STRAP4	ROM_SI	ROM_SO	ROM_SCLK
N15V-GM	H5TC4G63AFR-11C	PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
	256M x 16	0x4							
	MT41J256M16HA-093G:E	PU 10K	PU 10K	PD 10K	PU 10K				
	256M x 16	0xD							
	H5TC2G63FFR-11C	PU 10K	PU 10K	PD 10K	PD 10K				
	128M x 16	0xC							
	MT41J128M16JT-093G	PD 10K	PD 10K	PD 10K	PU 10K				
	128M x 16	0x1							
	K4W2G1646Q-BC1A	PU 10K	PU 10K	PU 10K	PD 10K				
	128M x 16	0xE							

VRAM	X76	VRAM P/N
Samsung	X7604112001	SA00005SH40
Micron	X7604012002	SA00005M120
Hynix	X7604012001	SA00005VS00

5					4					3					2					1				
D																								
C																								
B																								
A																								

Security Classification		LC Future Center Secret Data		Title			
Issued Date		Deciphered Date		Blank			
2013/08/08		2013/08/05		Size		Rev	
				Document Number		0.2	
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Date:				Monday, December 23, 2013		Sheet 30 of 59	

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Issued Date		2013/08/08		Deciphered Date		2013/08/05		Blank	
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				Date: Monday, December 23, 2013		Sheet 31 of 59		0.2	



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Security Classification				LC Future Center Secret Data				Title	
Issued Date		2013/08/08		Deciphered Date		2013/08/05		Blank	
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								Date: Monday, December 23, 2013	
								Sheet 32 of 59	
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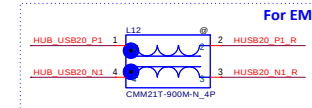
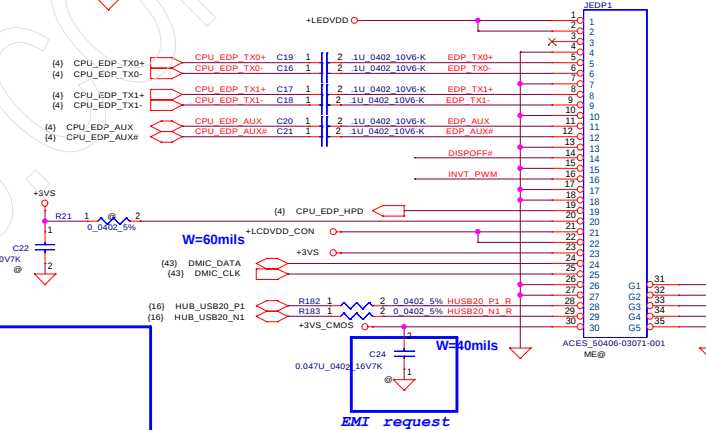
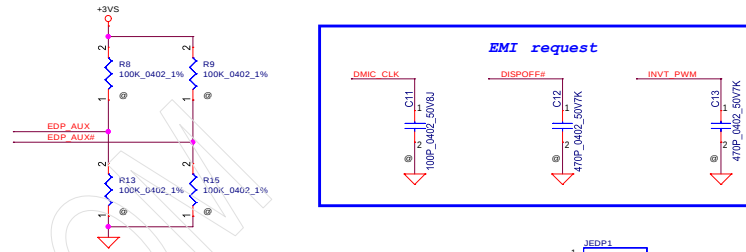
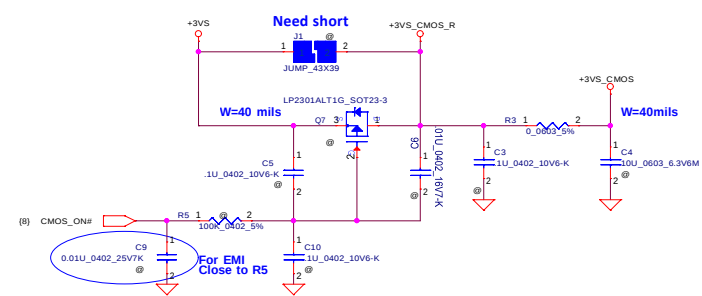


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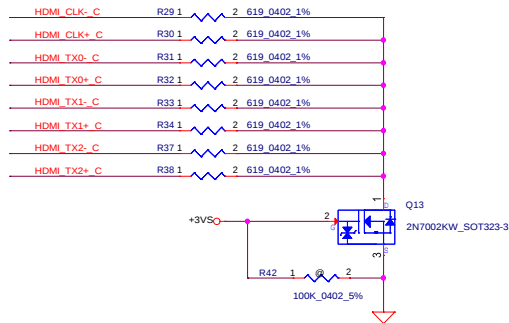
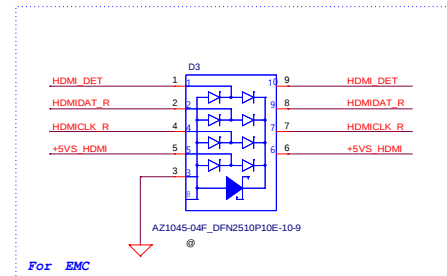
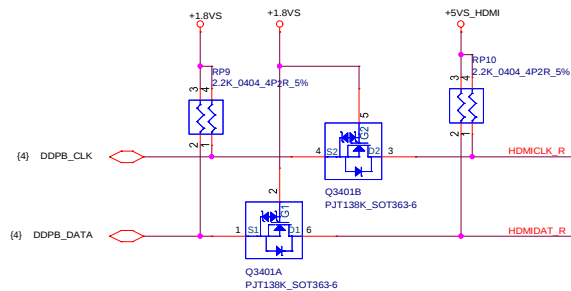
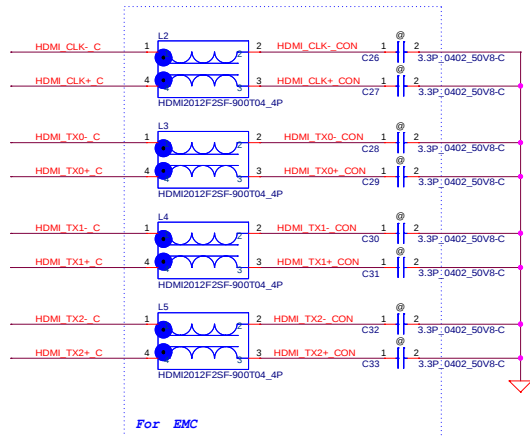
Rev

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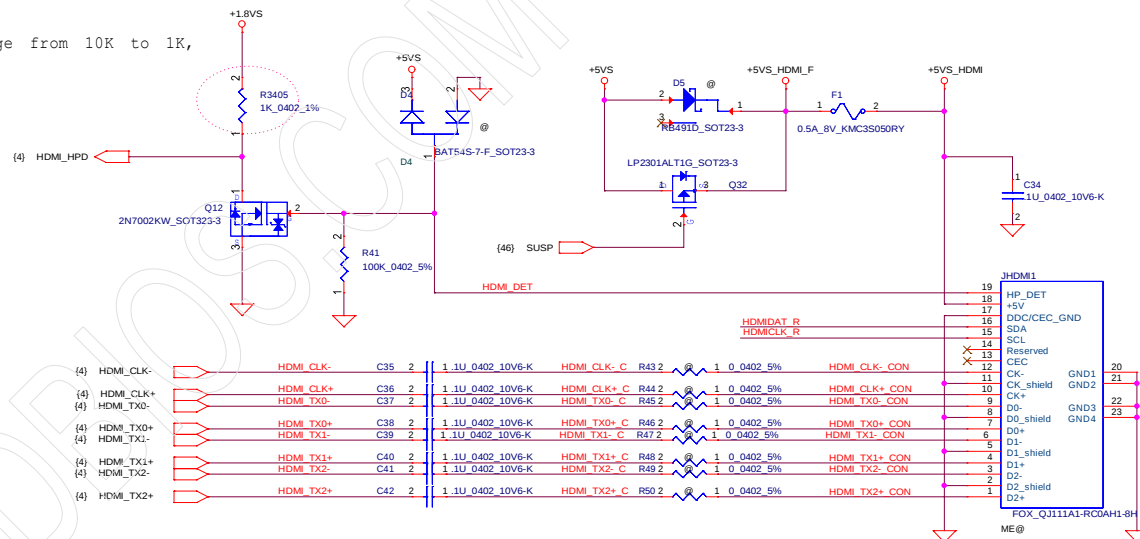
CMOS Camera



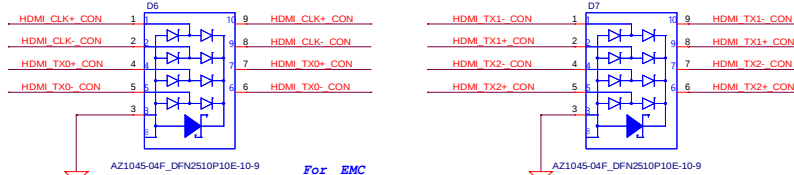
Security Classification	LC Future Center Secret Data			Title		
Issued Date	2013/08/08	Deciphered Date	2013/08/05	eDP/ CMOS/Touch screen		
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Date: Monday, December 23, 2013					Sheet 33 of 59	



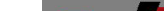
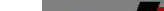
R4602 change from 10K to 1K, as Vienna

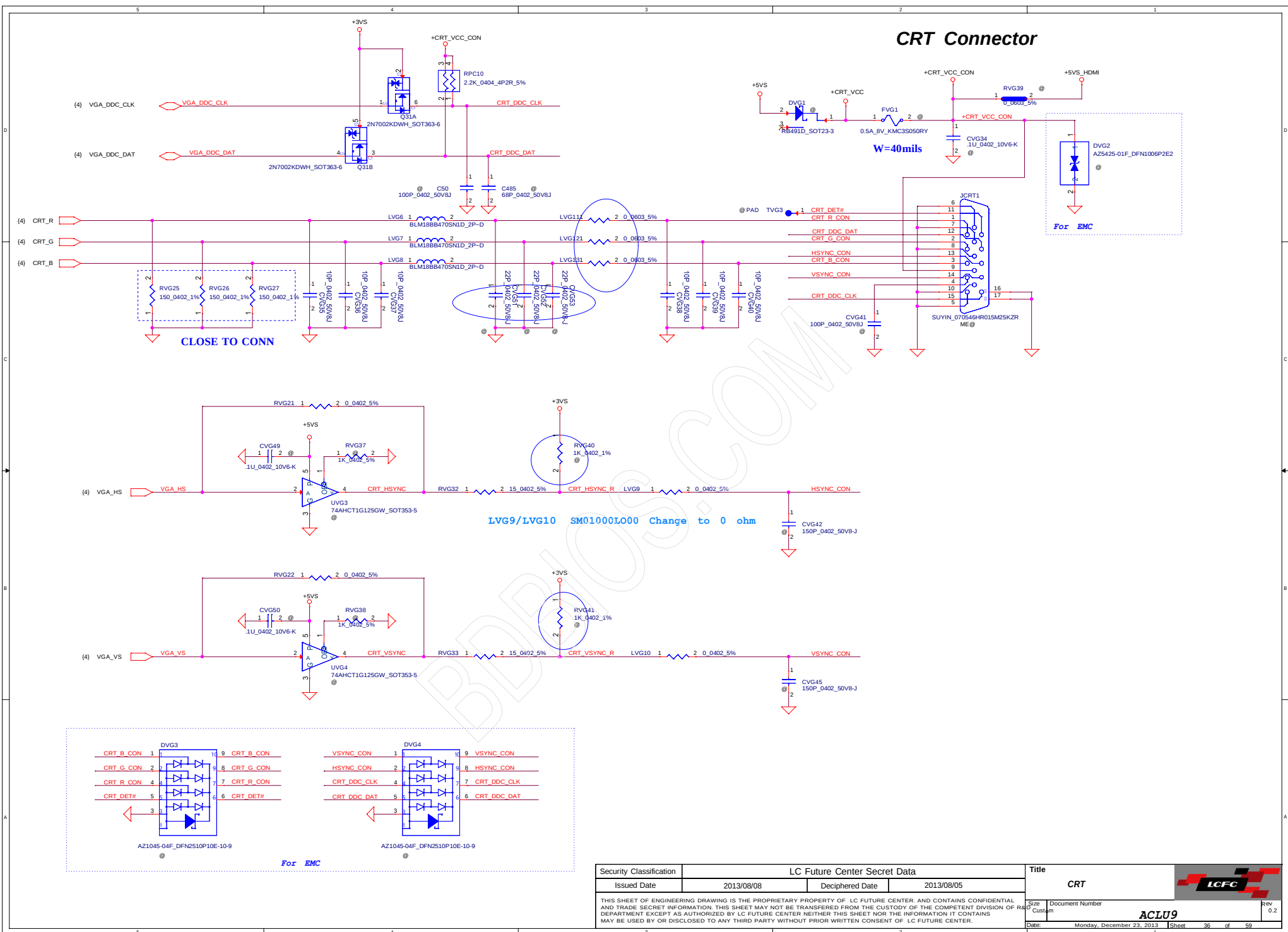


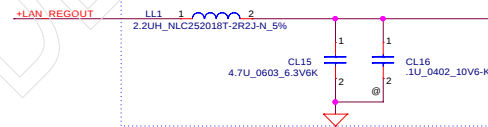
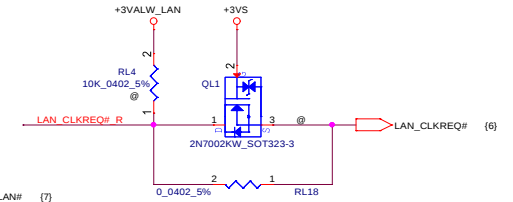
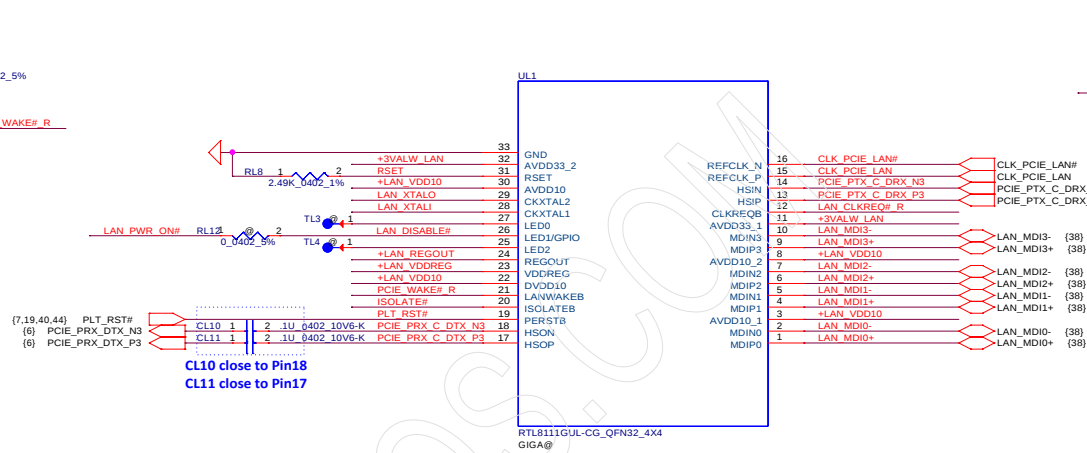
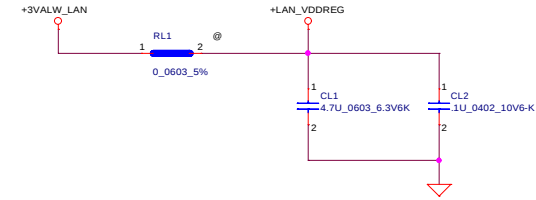
Close to JHDMI1



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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Size		
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Issued Date		2013/08/08		Deciphered Date			
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MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Date Monday, December 23, 2013		Sheet 35 of 59	
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LAN_VDD10

CL17 1uF 0402_10V6-K

CL18 1uF 0402_10V6-K

CL19 1uF 0402_10V6-K

CL20 1uF 0402_10V6-K

CL21 1uF 0402_6.3V6K

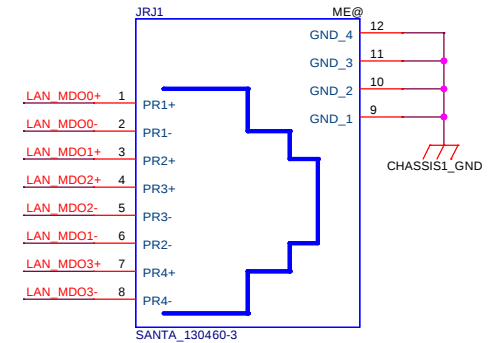
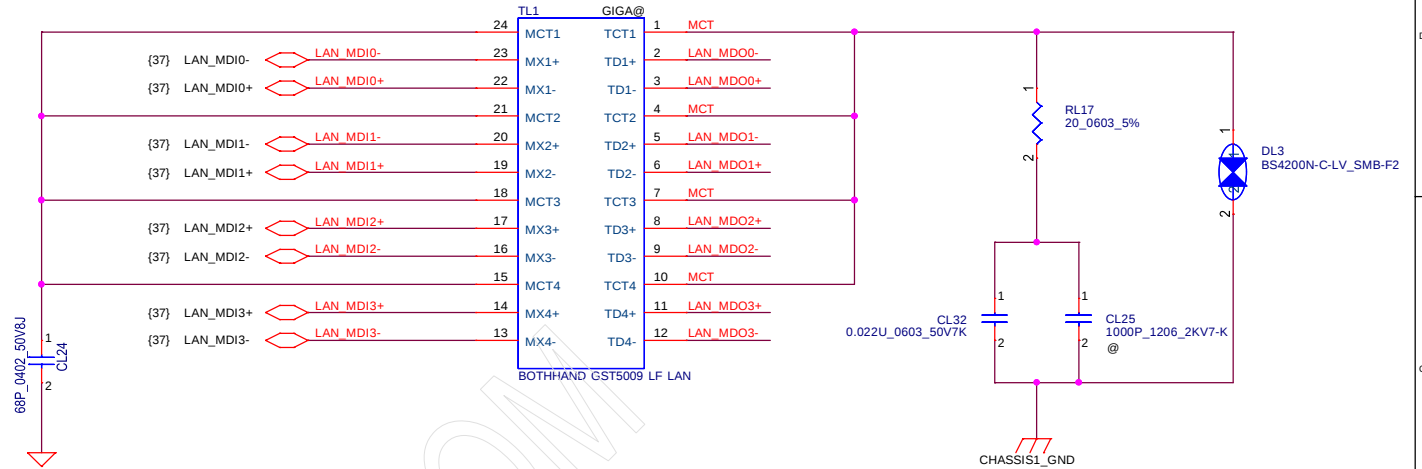
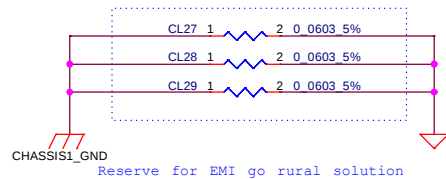
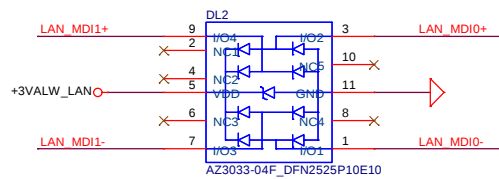
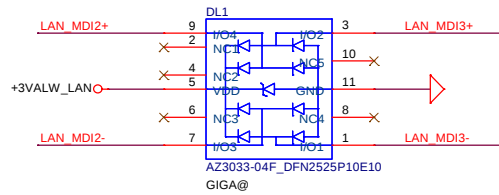
CL22 1uF 0402_10V6-K

Close to Pin3, 8, 22, 30

Close to Pin22(Reserved)

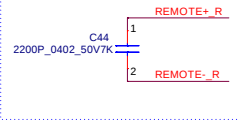
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Issued Date		Deciphered Date		LAN_RTL8111GUL/RTL8106E		0.2	
2013/08/08		2013/08/05					
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				Date: Monday, December 23, 2013		Sheet 37 of 59	

DL1/DL2 1'S PN:SC300003M00

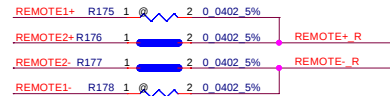
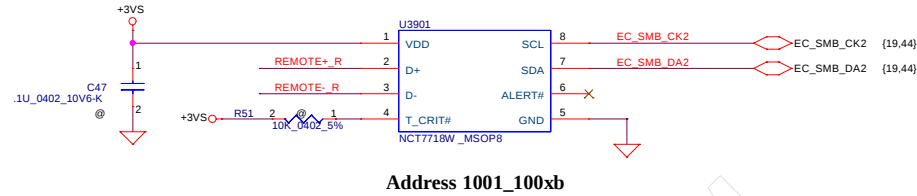


Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	LAN Transformer	
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				Date:	Monday, December 23, 2013
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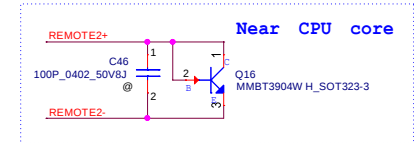
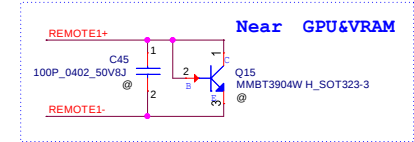
Close to U3901



SMSC thermal sensor placed near DIMM

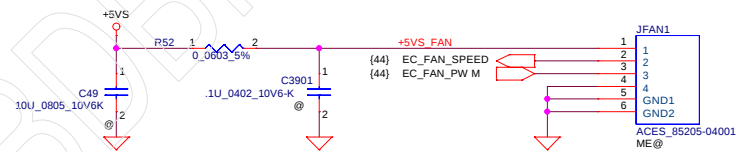


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



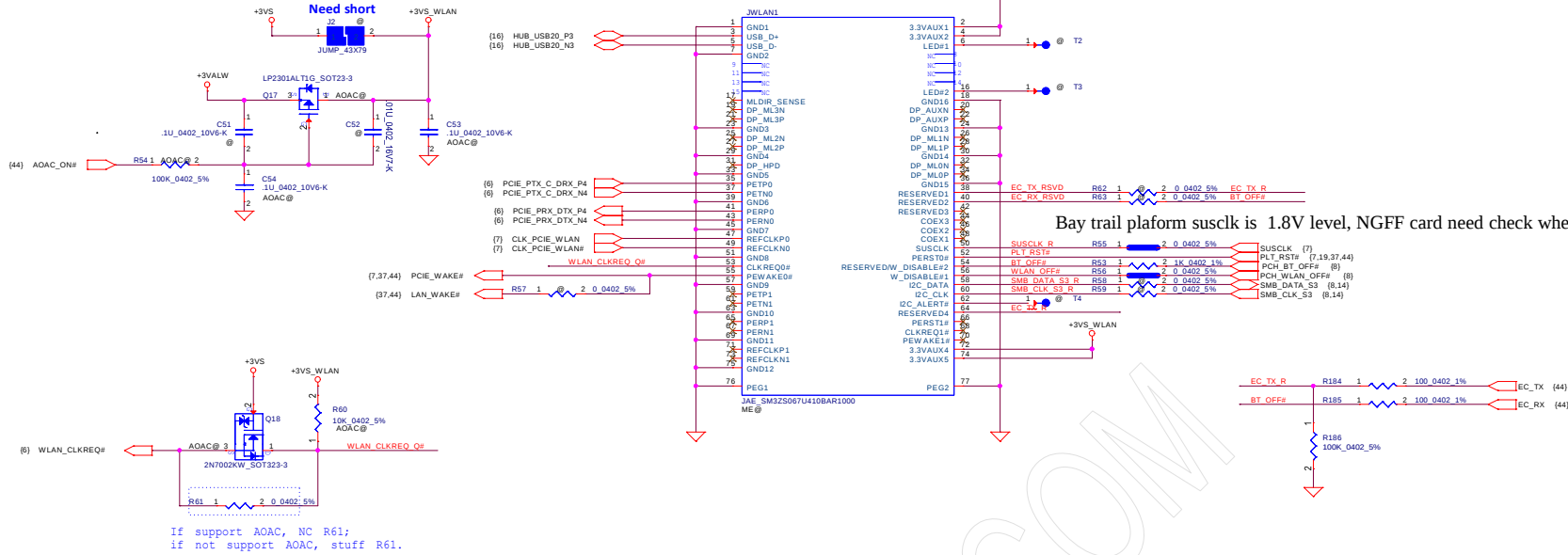
Baytrail SOC use thermal sensor to read the thermal,
Baytrail don't has PECI signal

FAN Conn



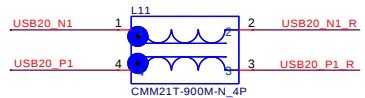
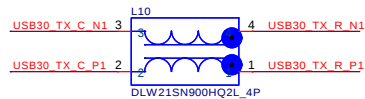
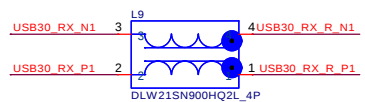
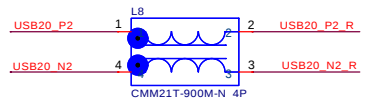
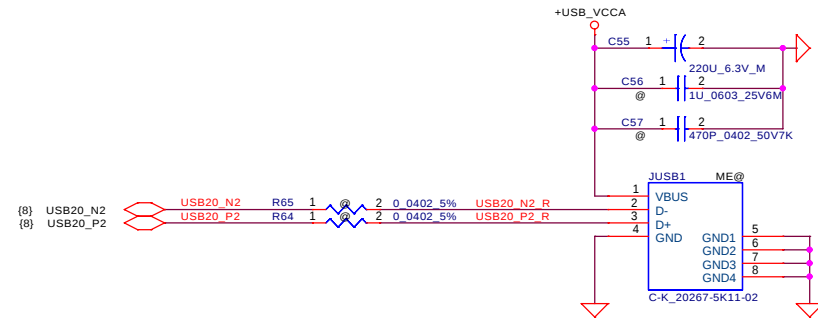
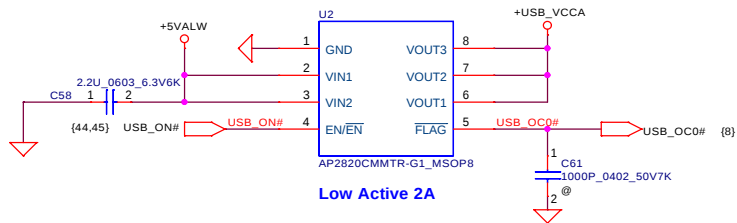
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Thermal sensor/FAN CONN	
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				Custom	0.2
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Mini-Express Card(WLAN/WiMAX)

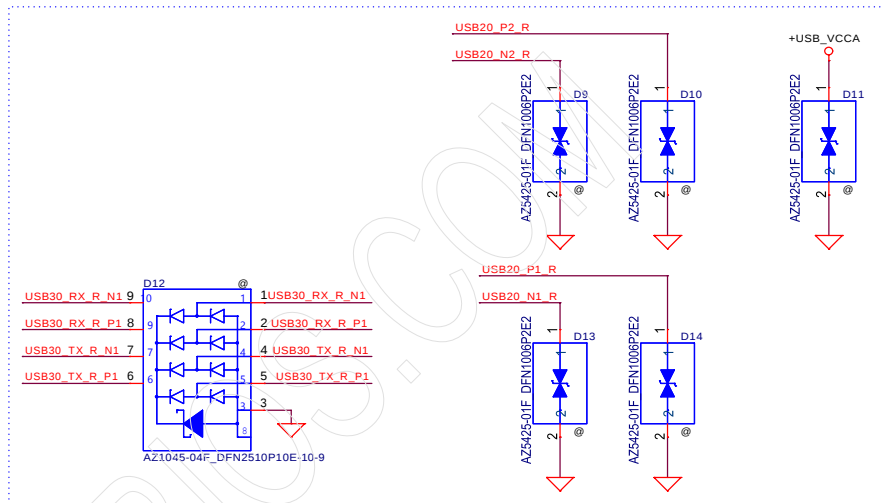


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	NGFF WLAN	
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				Date	Monday, December 23, 2013
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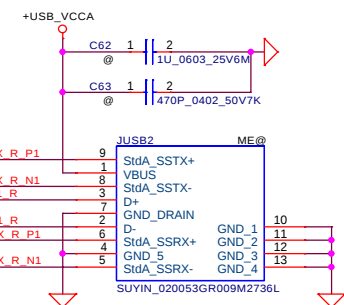
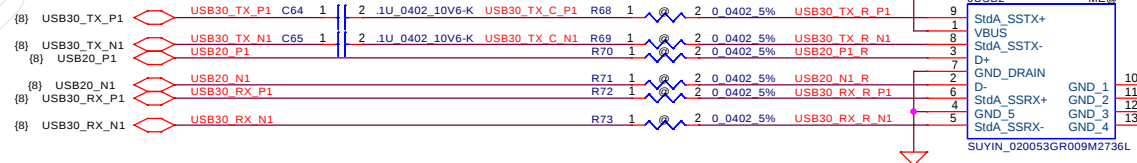
LEFT SIDE USB3.0 PORT X2



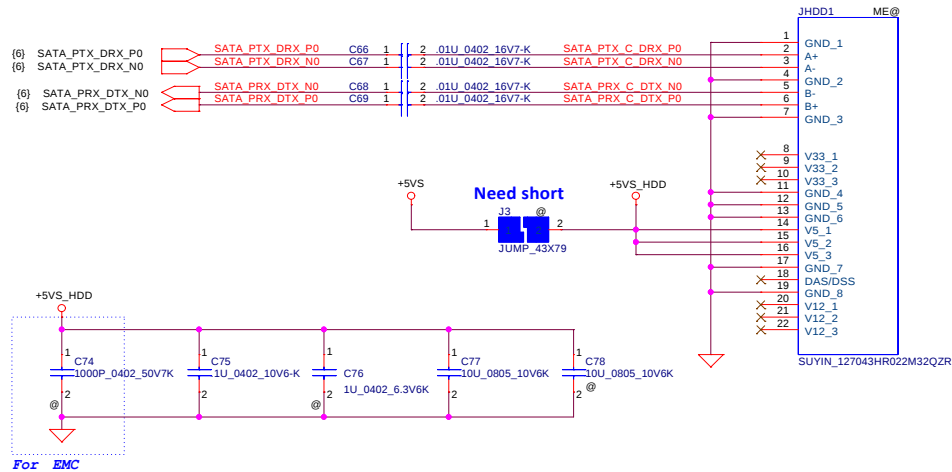
For EMC



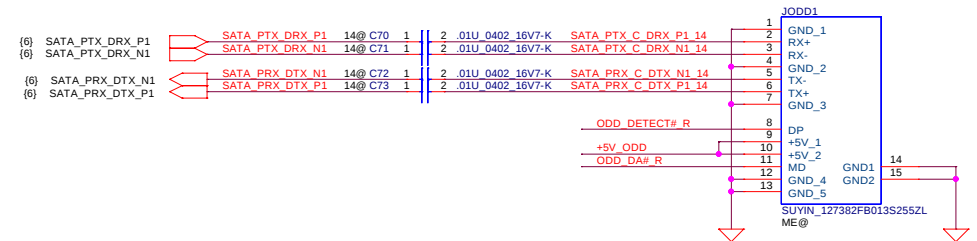
For EMC



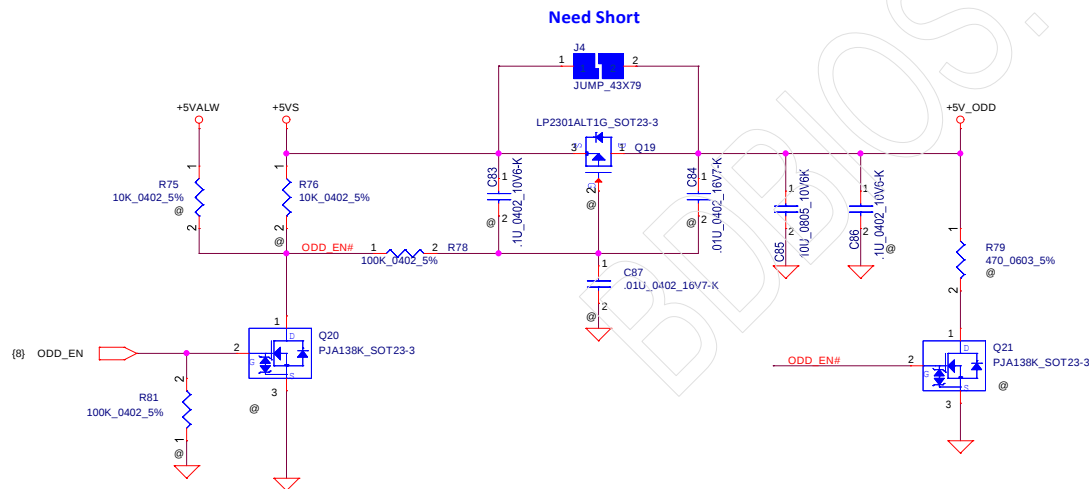
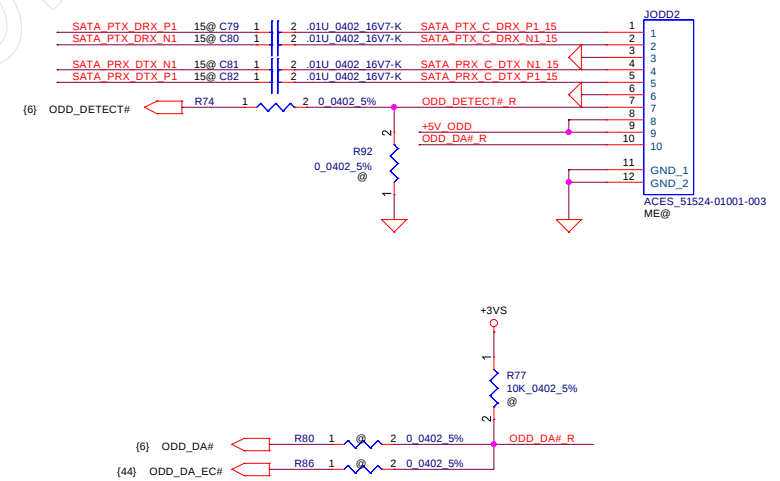
Security Classification	LC Future Center Secret Data			Title	USB2.0/USB3.0 PORT (LEFT)	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Size	Document Number	Rev
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SATA HDD Conn.

FOR 14"
SATA ODD Conn.

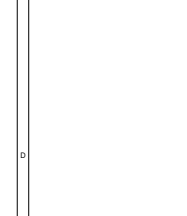
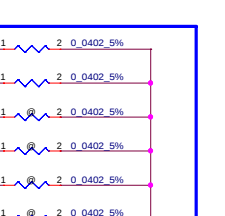
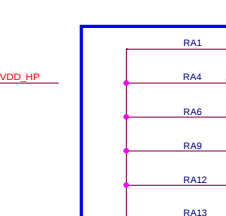
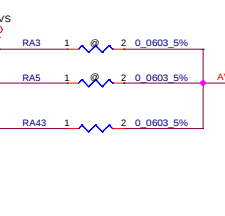
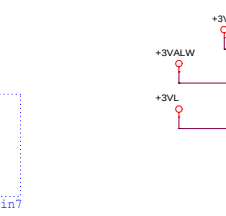
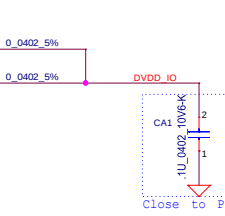
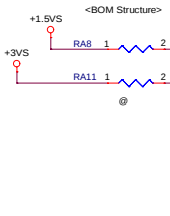
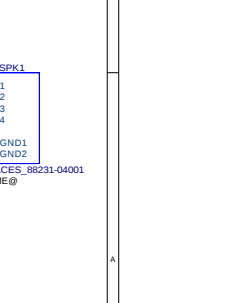
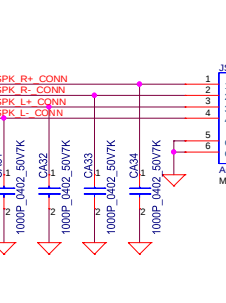
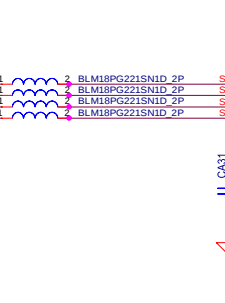
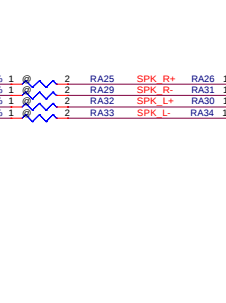
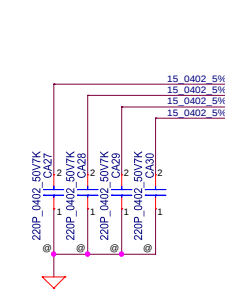
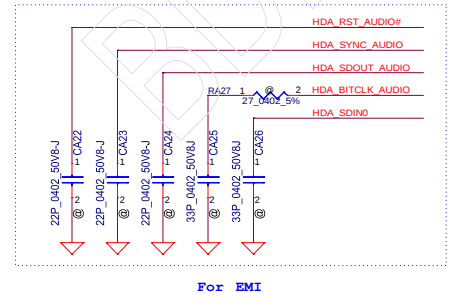
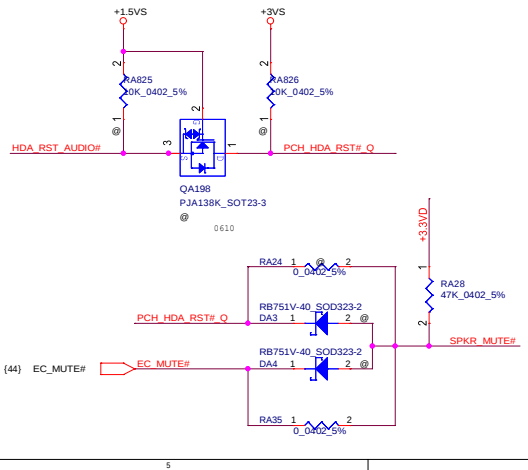
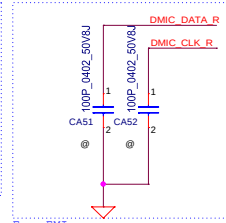
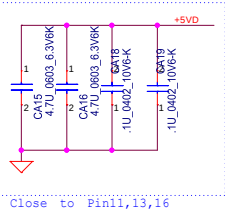
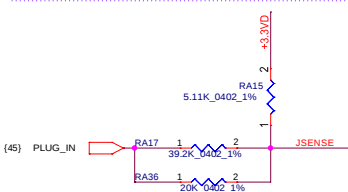
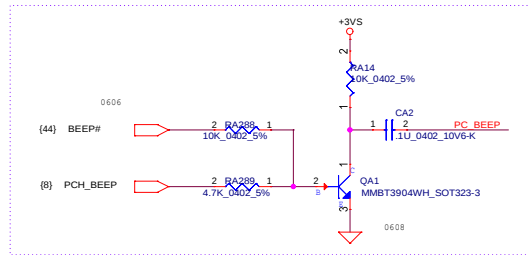


FOR 15"
SATA ODD FFC Conn



Security Classification		LC Future Center Secret Data		Title HDD/ODD CONN 	
Issued Date	2013/08/08	Deciphered Date	2013/08/05		
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Same as Vienna



CX20751-11Z

CX20752-21Z_QFN40_5X5

Security Classification

LC Future Center Secret Data

Issued Date

2013/08/08

Deciphered Date

2013/08/05

Title

Codec_CX20751

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Size

Document Number

ACLU9

Date

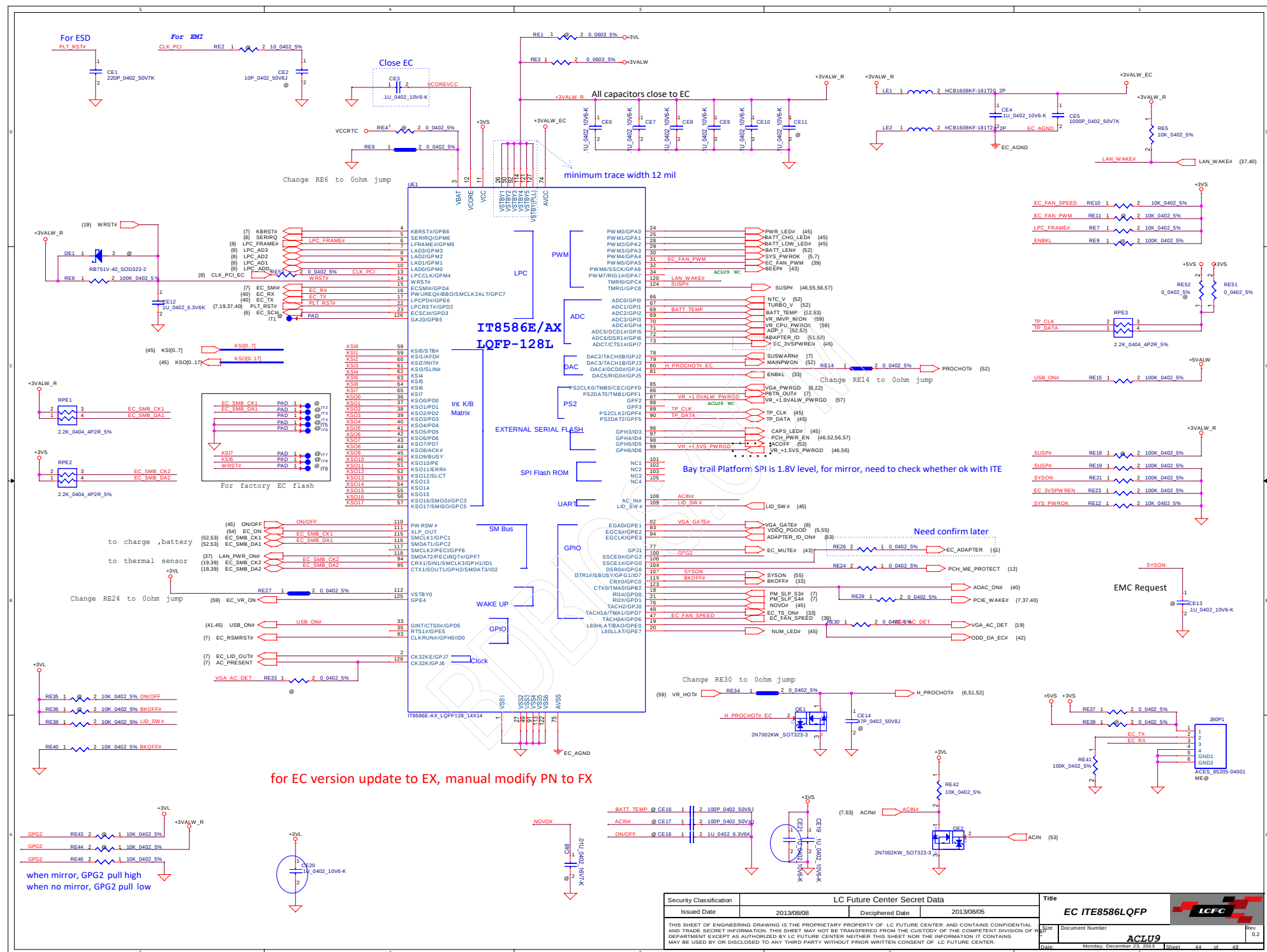
Monday, December 23, 2013

Sheet

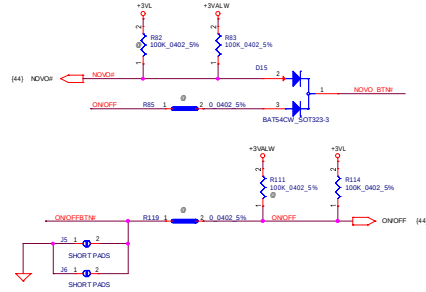
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Rev 0.2

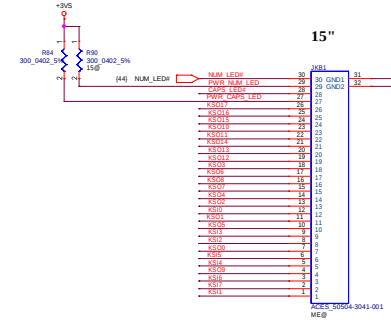
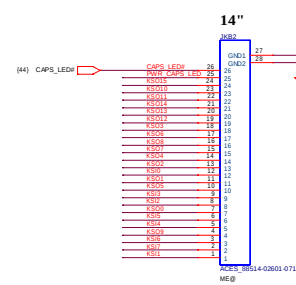
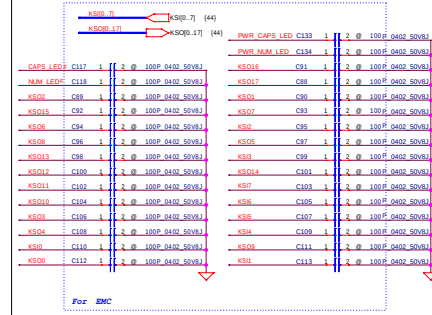


ON/OFF switch

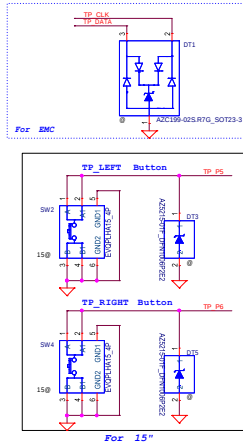
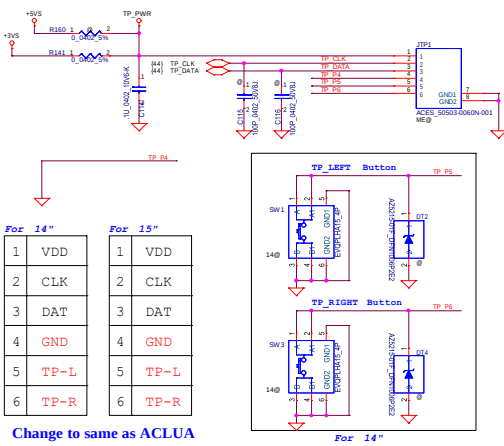


TP/B Connector

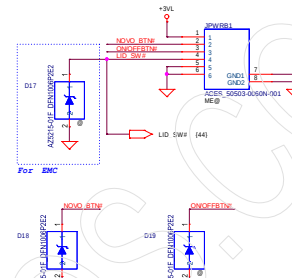
K/B Connector



14"	15"
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KB_2	KB17_14
KB_3	KB14_14
KB_4	KB09_14
KB_5	KB14_14
KB_6	KB15_14
KB_7	KB00_14
KB_8	KB12_14
KB_9	KB13_14
KB_10	KB05_14
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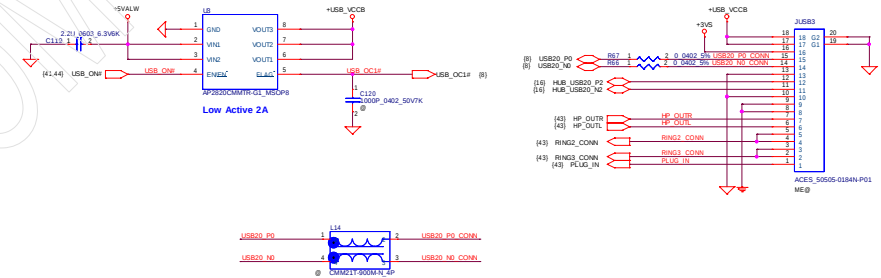


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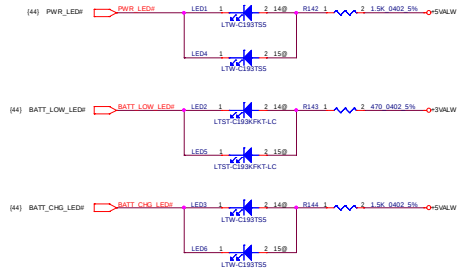


USB I/O Connector

Right Side USB2.0 Port X 1 (USB/B)

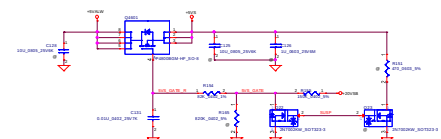


LED

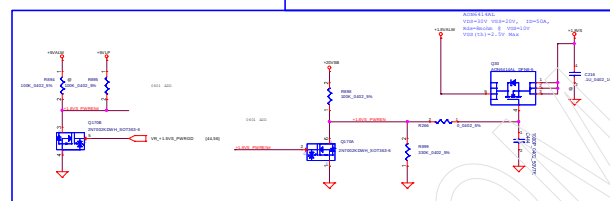
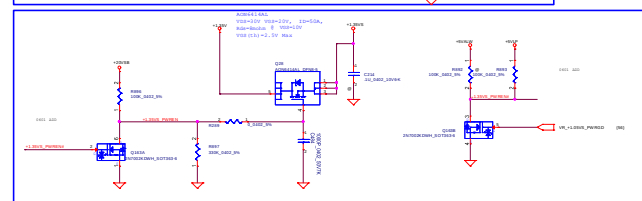
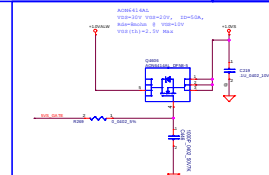
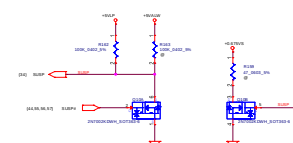
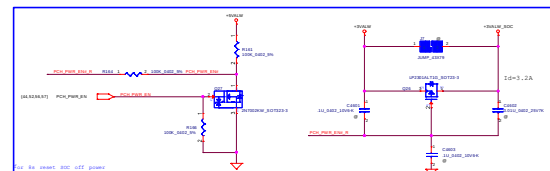
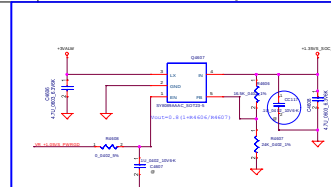
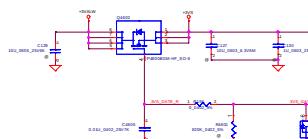


Security Classification	LC Future Center Secret Data	Title
Issued Date	2013/08/08	Deciphered Date
Deciphered Date	2013/08/05	
KBD/PWR/IO/LED/TP Conn.		LCFC
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Doc Control	Doc Number	Doc Date
Doc Control	Doc Number	Doc Date
Doc Control	Doc Number	Doc Date

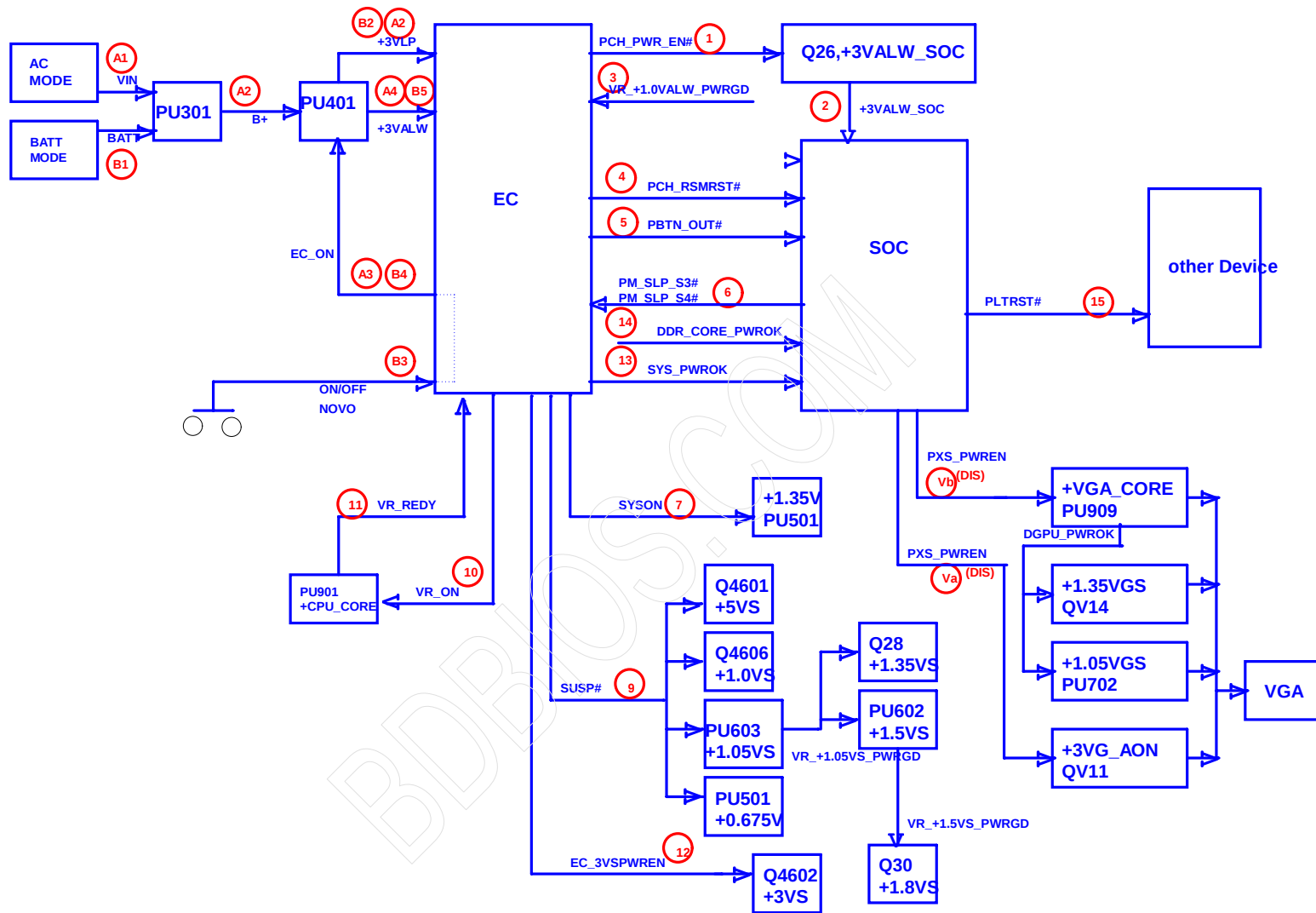
+5VALW to +5VS AP4800BDM
VGS=10V, ID=9A, Rds=18m ohm
VGS=-25V



+3VALW to +3VS AP4800BDM
VGS=10V, ID=9A, Rds=18m ohm
VGS=-25V



Security Classification	LC Future Center Secret Data		Rev	1
Report Date	20110805	Classification Code	TOP SECRET	
This report is classified SECRET because it contains information that is not generally known and its disclosure could be detrimental to the national defense. This report is classified SECRET because it contains information that is not generally known and its disclosure could be detrimental to the national defense. This report is classified SECRET because it contains information that is not generally known and its disclosure could be detrimental to the national defense.				
Form	REPORT NUMBER	ACT09	1	



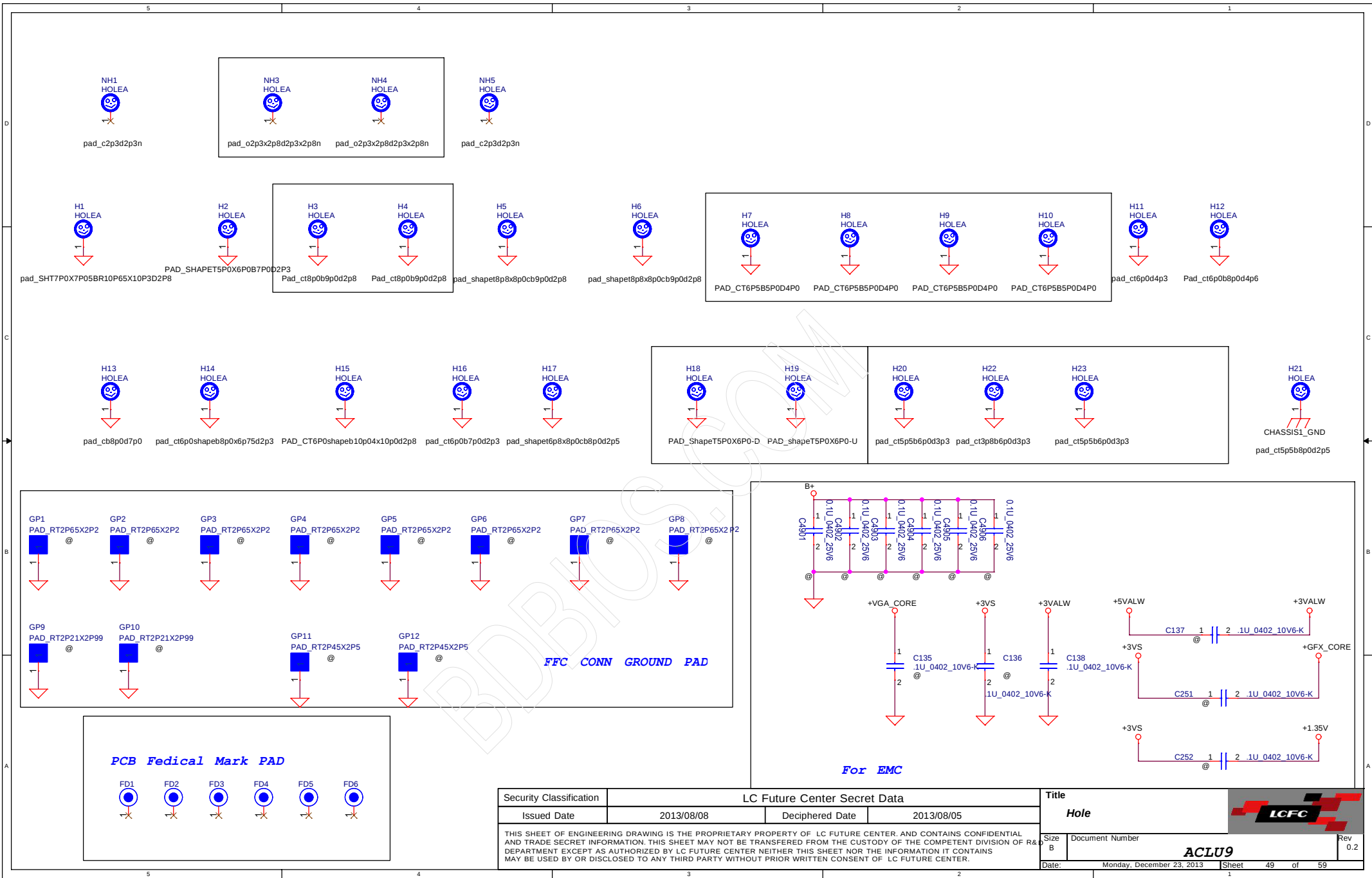
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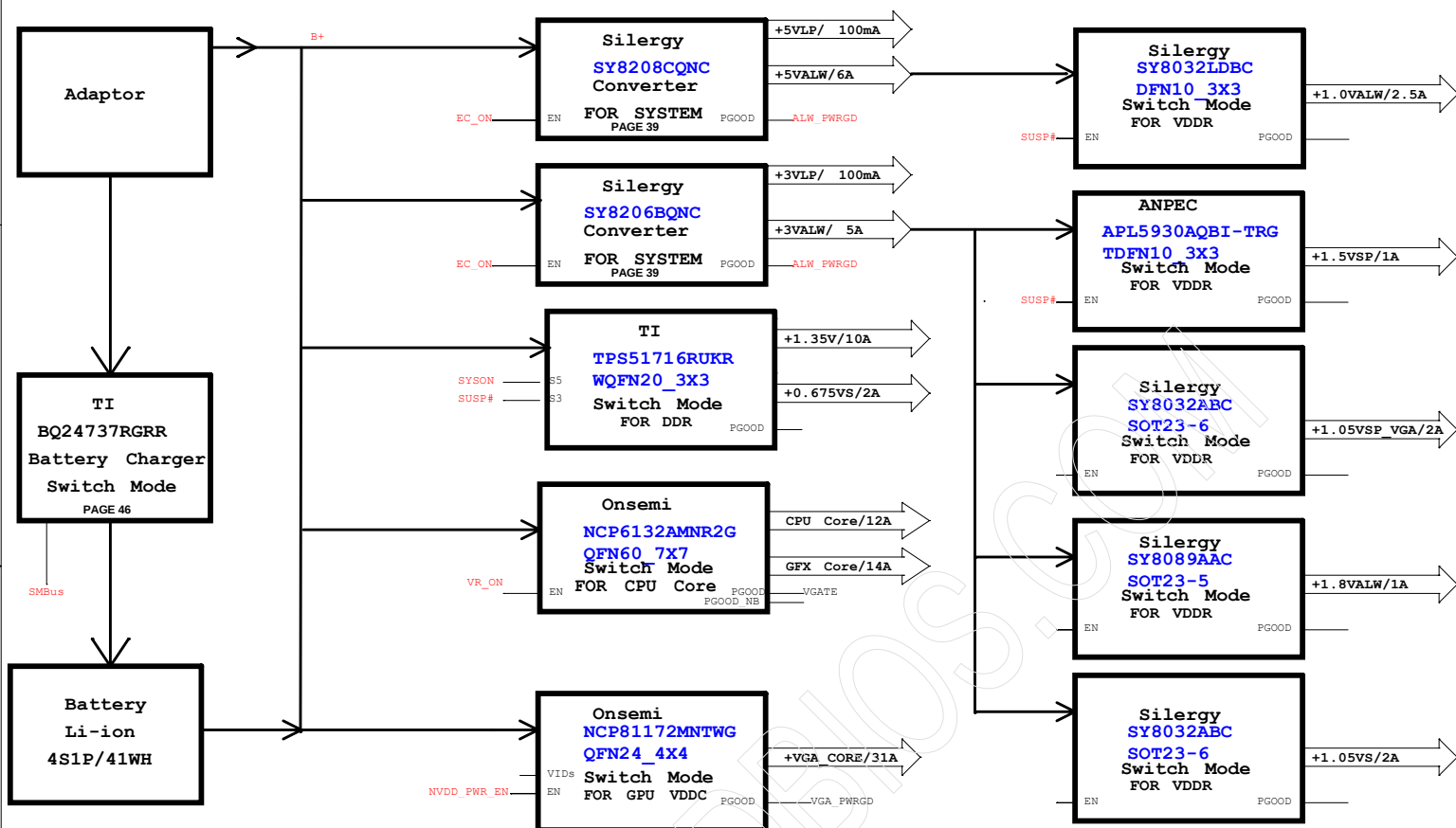
Title		Power sequence Block	
Size	Document Number	Rev	0.2
Custom	ACLU9		
Date:	Monday, December 23, 2013	Sheet	47 of 59

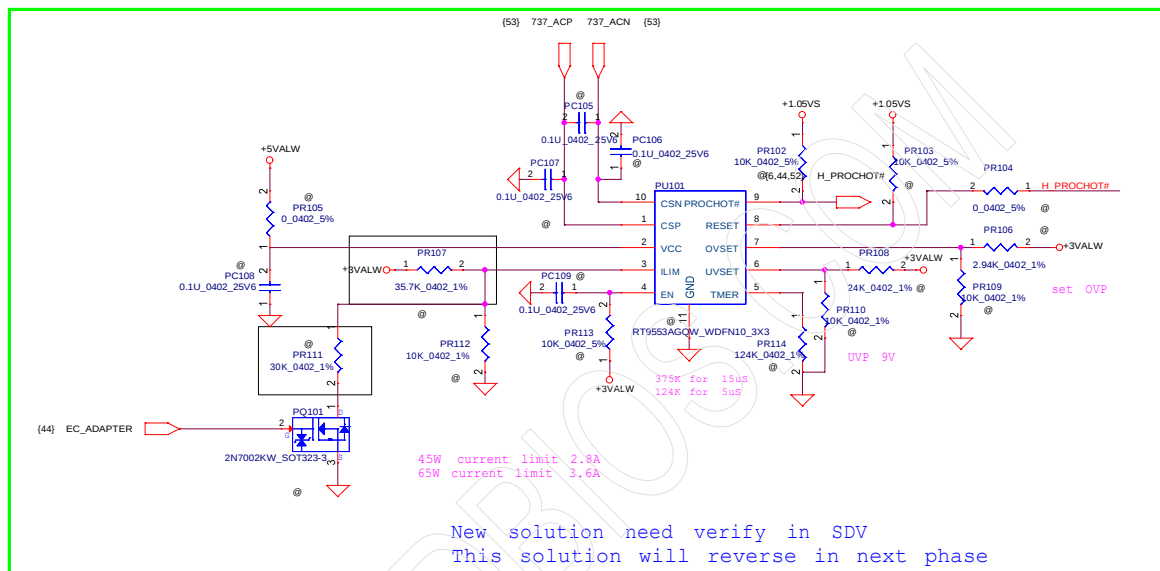
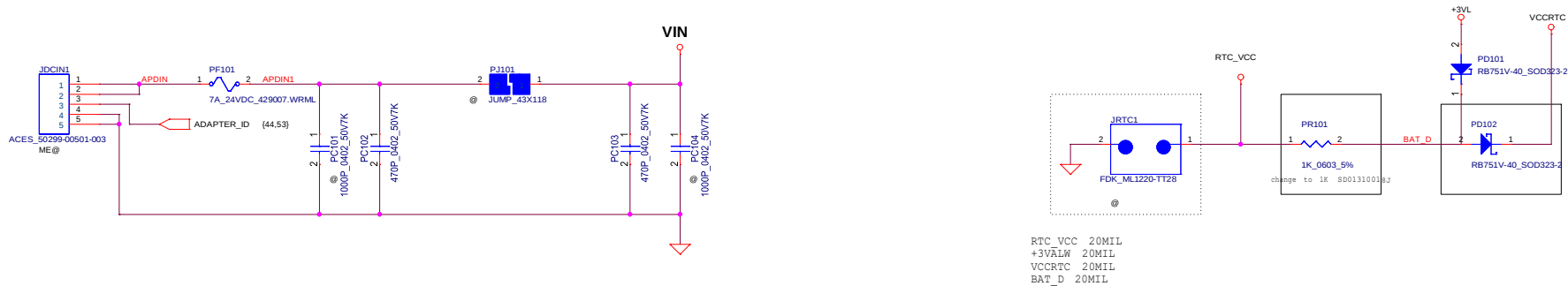
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C				C
B				B
A				A
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Security Classification	LC Future Center Secret Data			Title	
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				Date: Monday, December 23, 2013	Rev 0.2

Sheet	48	of	59
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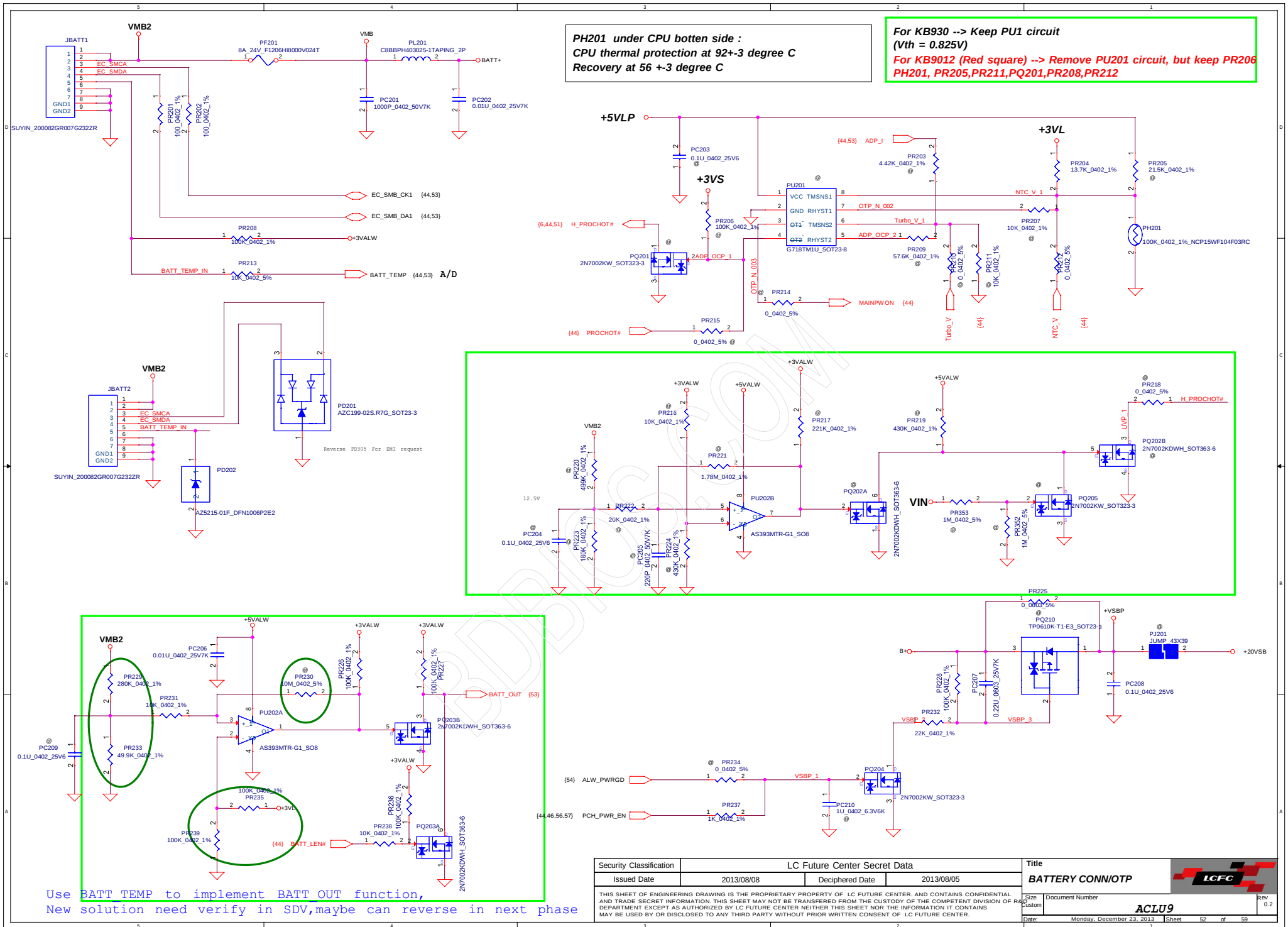




PH201 under CPU bottom side :
CPU thermal protection at 92+3 degree C
Recovery at 56 +3 degree C

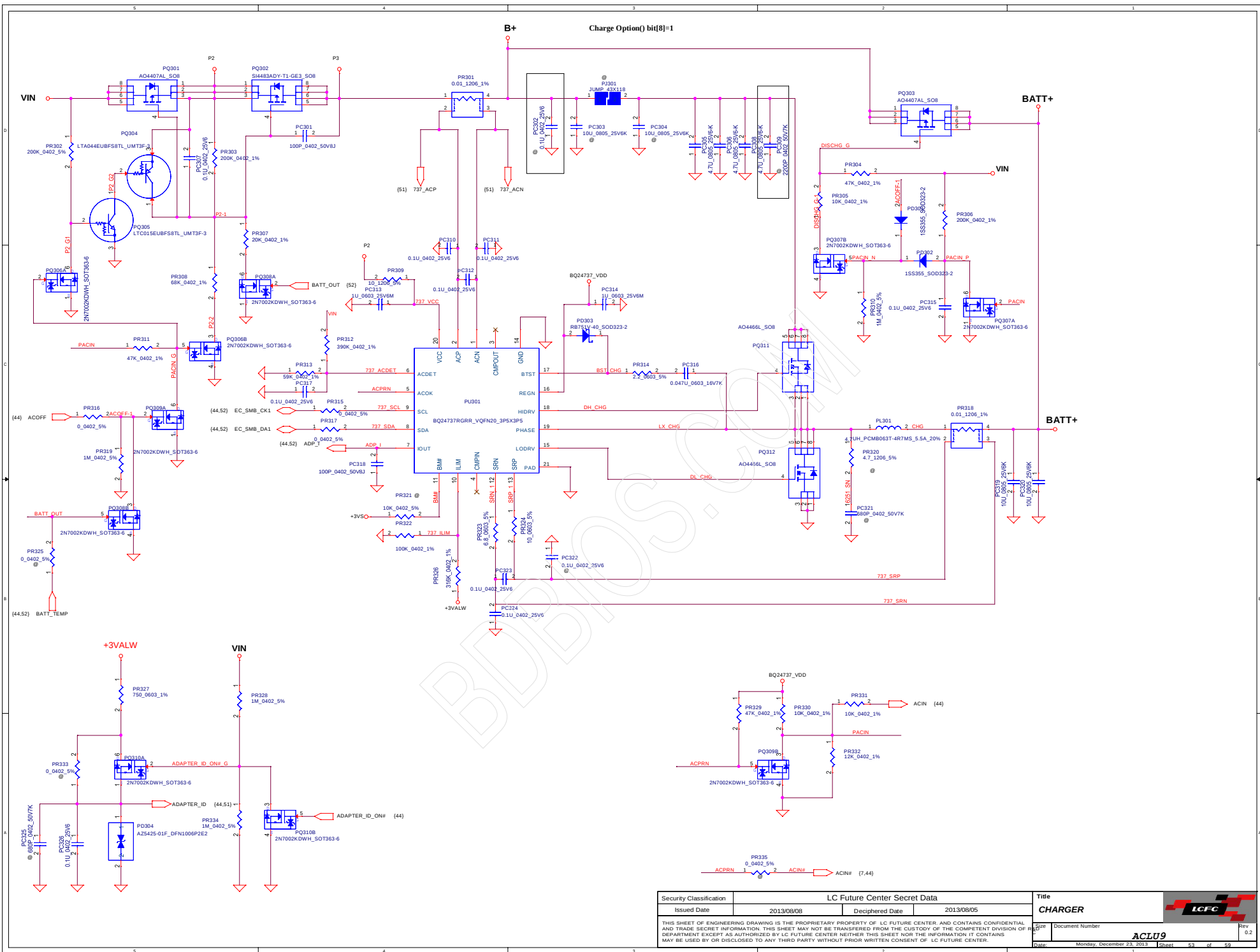
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212



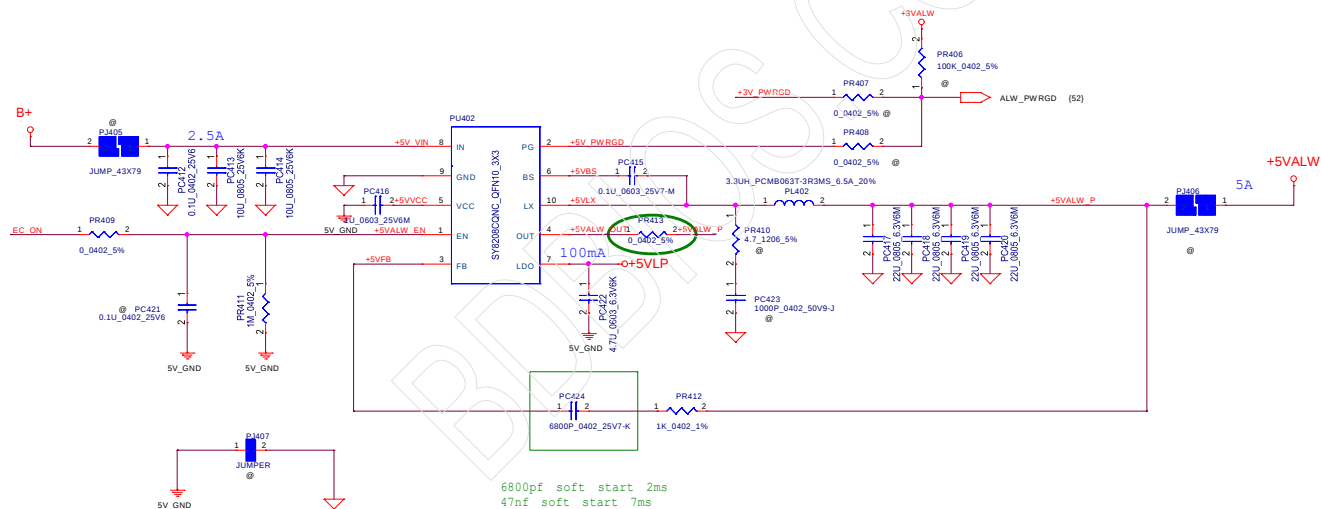
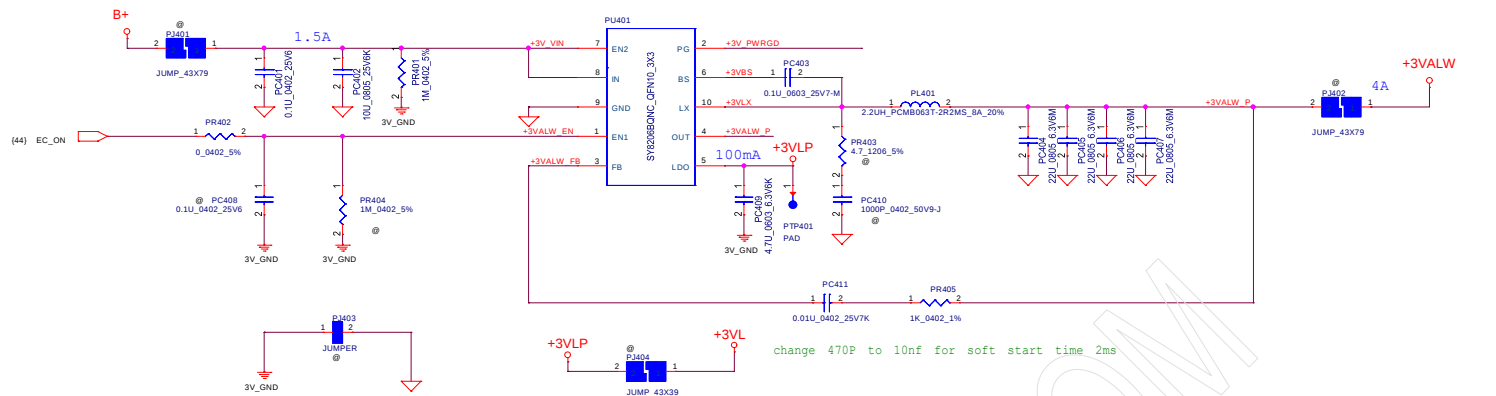
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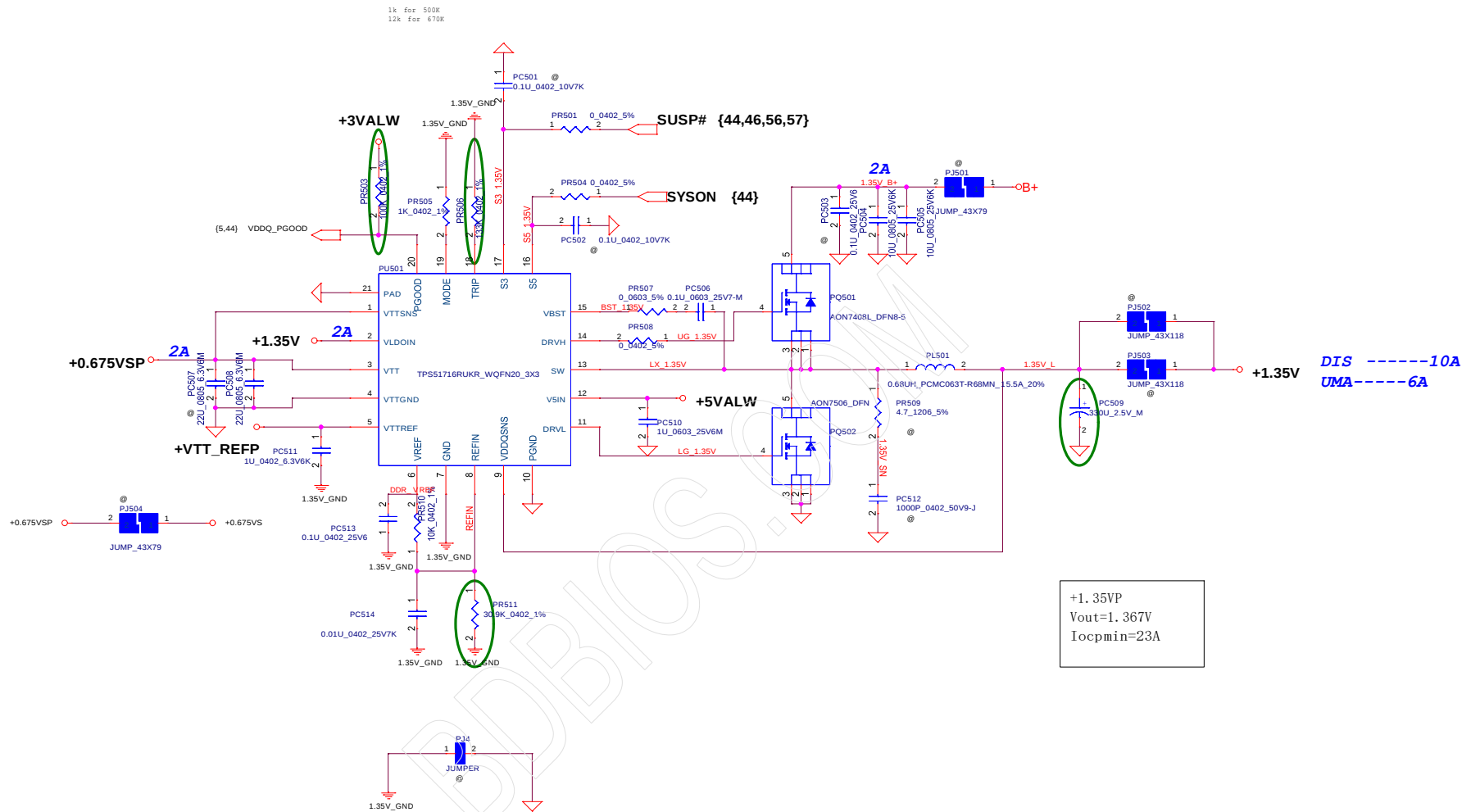
Title		CHARGER	
Rev	Document Number	ACLU9	
Date	Monday, December 23, 2013	Sheet	53 of 52



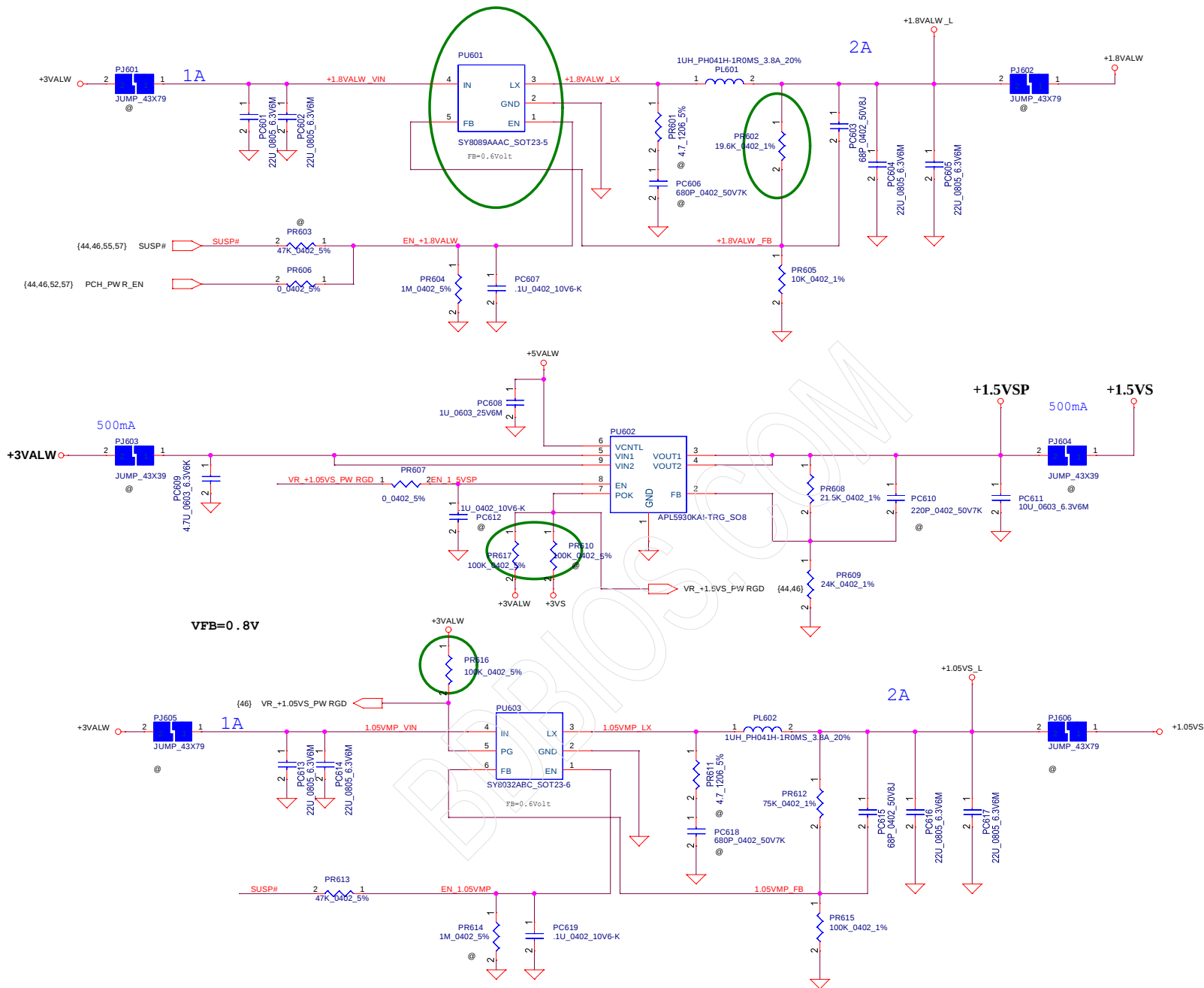
Security Classification		LC Future Center Secret Data	
Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Title		PWR_3VALW/5VALW	
Rev	Document Number	Rev	0.2
Date	Monday, December 23, 2013	Sheet	54 of 59





Security Classification	LC Future Center Secret Data		Title	1.35VS/+0.675VS	
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				ACL09	
				Date	Monday, December 23, 2013
				Sheet	55 of 59



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Size	Custom	Document Number	ACLU9
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