

Compal Confidential

Lotus M/B Schematics Document

14": Elise; 15.6" Exige

Intel Ivy Bridge ULV Processor with DDRIII + Panther Point

Date : 2011/10/27
Version 0.1

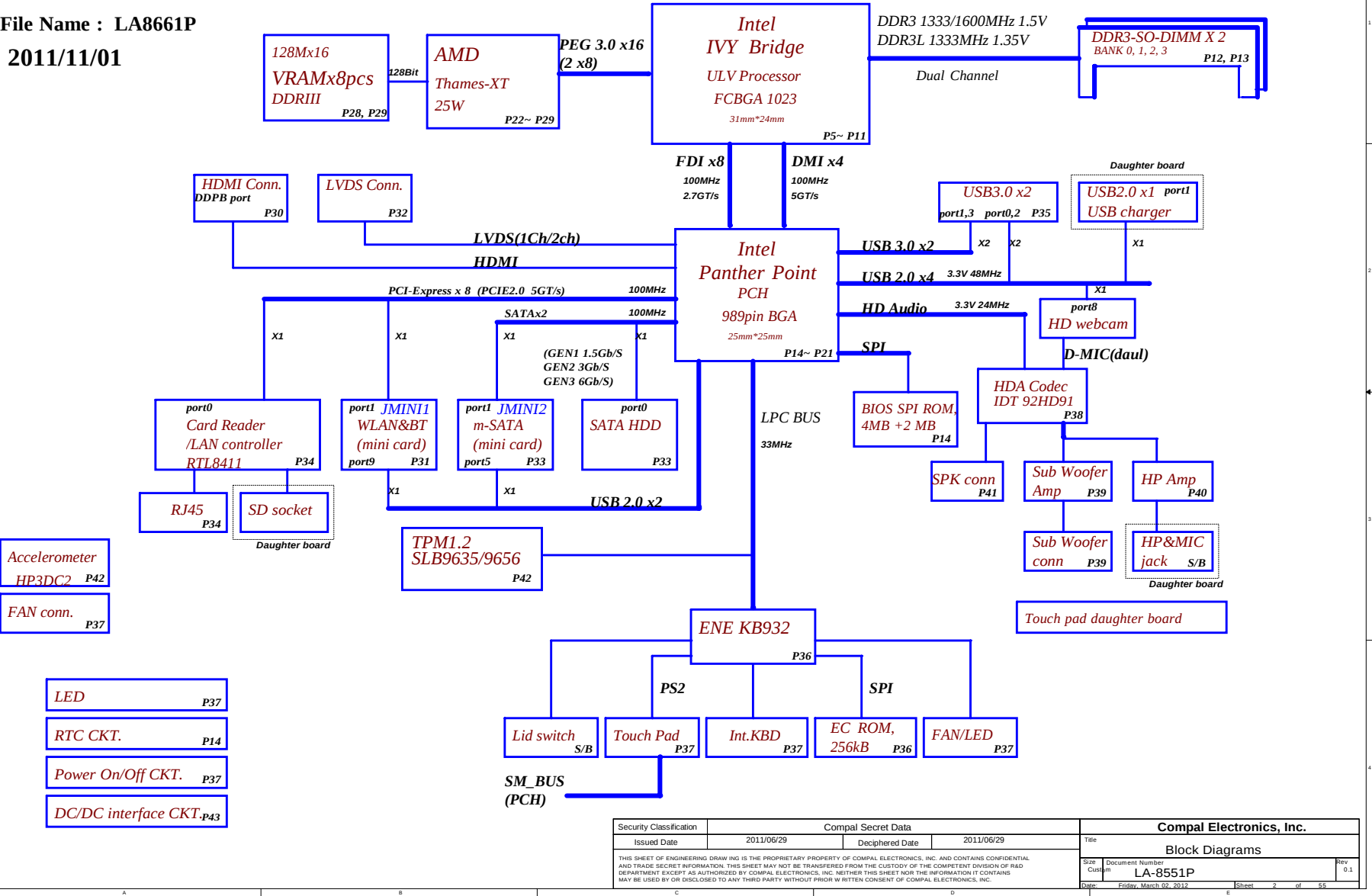
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				Block Diagrams		
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Compal Confidential

Model Name : Lotus

File Name : LA8661P

2011/11/01



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QAU30/50 (LA-8661P Ver:0.1)

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
		ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S1	S3	S5
+VGA_CORE	GPU power	PX	OFF	OFF
+3VGS	GPU power	PX	OFF	OFF
+1.8VGS	GPU power	PX	OFF	OFF
+1.5VGS	GPU power	PX	OFF	OFF
+1.0VGS	GPU power	PX	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	
G-sensor	0x50/0x52

PCH SM Bus address

Device	Address
DDR DIMM0	
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	

EC SM Bus2 address

Device	Address
PCH (Reserve)	

SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	BATT Charger	TP	SODIMM	EC_SMB_CK2 EC_SMB_DA2	PCH_SML1CLK PCH_SML1DATA	G-Sensor	GPU	HP AMP
EC_SMB_CK1 EC_SMB_DA1	KB930	V		V					V		
EC_SMB_CK2 EC_SMB_DA2	KB930							V		V	V
PCH_SMBCLK PCH_SMBDATA	PCH		@		V	V					
PCH_SML0CLK PCH_SML0DATA	PCH										
PCH_SML1CLK PCH_SML1DATA	PCH						V				

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	PCIE LAN CARD READER	CLKOUTFLEX0	None
			CLKOUTFLEX1	None
	CLKOUT_PCIE1	mini WLAN	CLKOUTFLEX2	None
	CLKOUT_PCIE2	None	CLKOUTFLEX3	DGPU_PRSENT#
	CLKOUT_PCIE3	None		
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :
: means Digital Ground
: means Analog Ground

Project ID	30UMA@	30DIS@	50UMA@	50DIS@
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PCB	LA-8661P	LA-8662P
	PX@	UMA@

BY SKU			
TPM	9635@	9656@	
CPU	CPUUMA1@		
	CPUUMA2@		
	CPUDIS@		
VRAM	X76@	H2G@	
	M2G@	S2G@	

Option	@	CONN@	USB30@	PX@	UMA@	DIS@	THA@
UMA	X	X	V	X	V	X	X
DIS	X	X	V	V	X	V	V

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

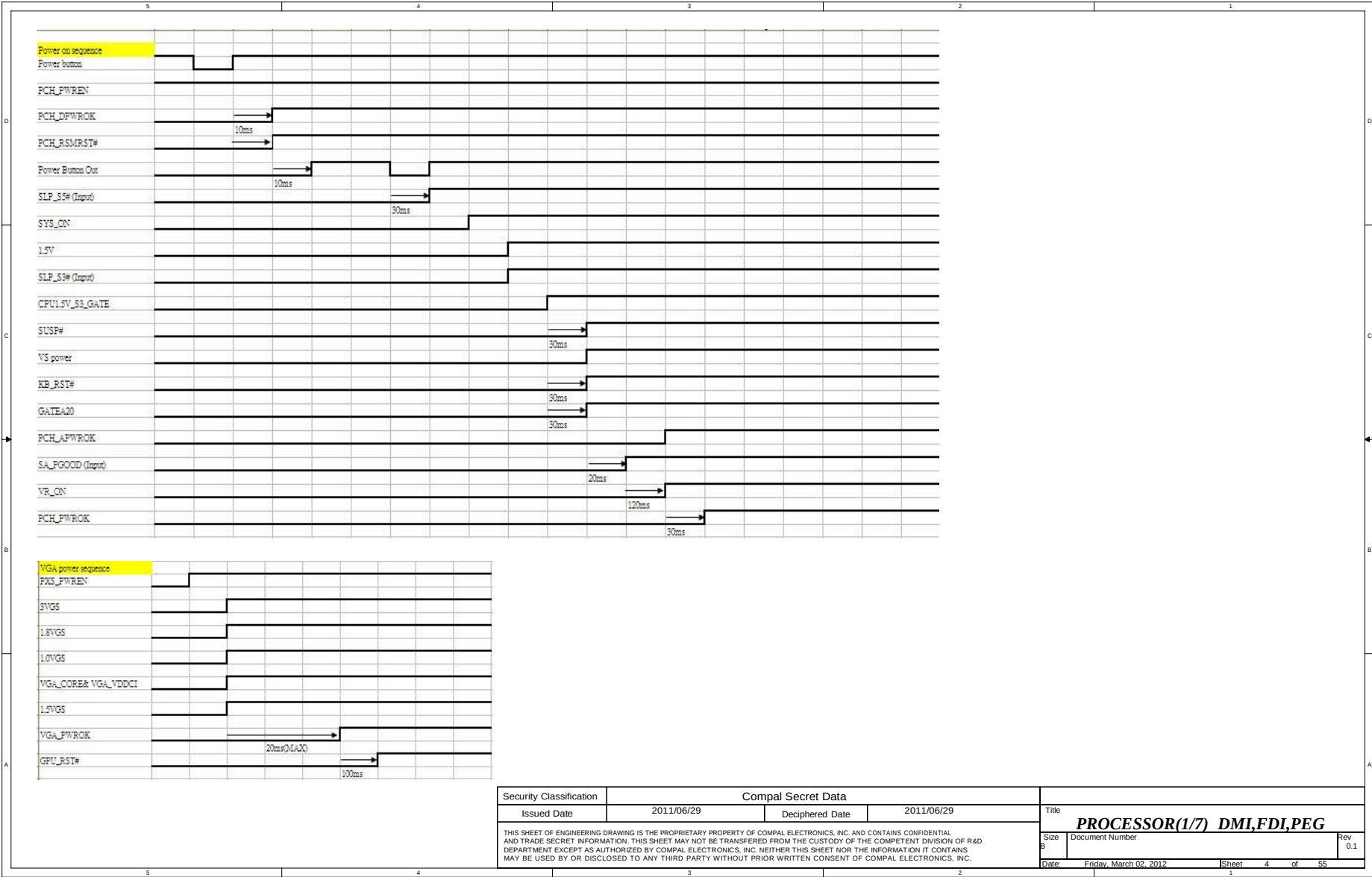
SATA	DESTINATION
SATA0	SATA, JHDD1
SATA1	m-SATA,JMINI2
SATA2	None
SATA3	None
SATA4	None
SATA5	None

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB2.0 (left Side)
		1	USB2.0 (right Side)
		2	USB2.0 (left Side)
	UHCI11	3	None
		4	None
		5	None
		6	None
EHCI2	UHCI3	7	None
		8	Camera
		9	Mini Card(WLAN& BT)
	UHCI4	10	None
		11	None
		12	None
		13	None

USB 3.0	Port	2 External USB Port
	1	USB3.0 (left Side)
	2	None
	3	USB3.0 (left Side)
	4	None

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UCPU1 CPU0IS01@
i5-2467M CPU
SA00004X000

UCPU1 CPU0IS02@
i5-2367M CPU
SA000051H20

UCPU1 CPU0IS03@
i5-2367M CPU
SA000051H20

UCPU1 CPU0IS04@
i5-3317U CPU
SA00005K600

UCPU1 CPUUMA3@
i5-2367M CPU
SA000051H20

UCPU1 CPUUMA4@
17W 1.7GHz GT2 ES2 QBP7
SA00005B010

UCPU1 CPUUMA5@
17W 1.7GHz no onlg ES2 QB7Q
SA00005B020

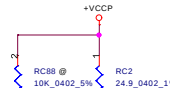
UCPU1 CPUUMA1@
17W 1.5GHz GT2 ES2 QBP8
SA00005AZ10

UCPU1 CPUUMA2@
17W 1.5GHz no onlg ES2 QB7P
SA00005AZ20

Sandy Bridge:
Intel Core i5-2467M: SA00004X000 (4619HY32L01)

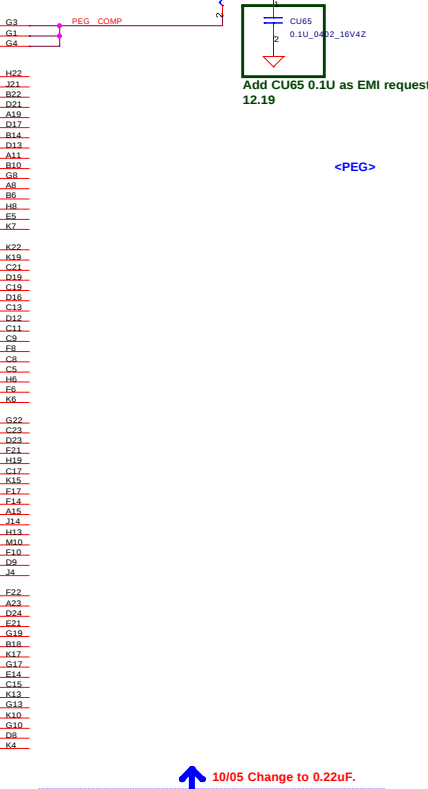
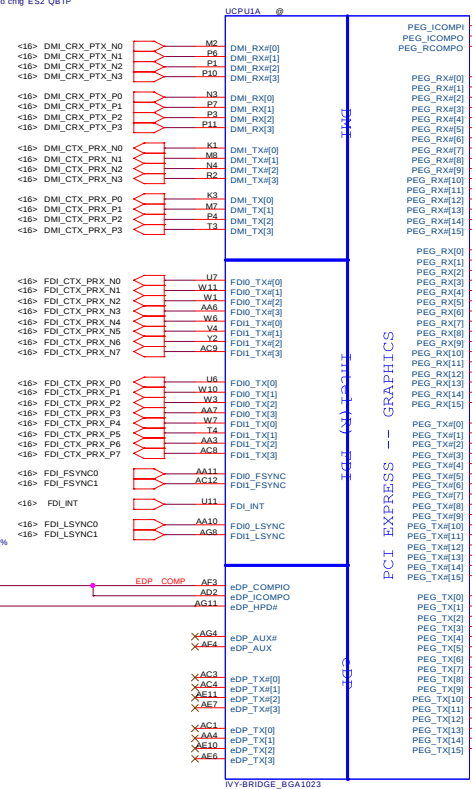
Ivy Bridge:
1.5GHz GT2 ES2 QBP8: SA00005AZ10 (4619HZ32L01)
1.5GHz ES2 QB7P: SA00005AZ20(4619HZ32L02)

PEG_ICOMPI and RCOMPO signals should be
shorted and routed
with - max length = 500 mils - typical
impedance = 43 mohms
PEG_ICOMPO signals should be routed with -
max length = 500 mils
- typical impedance = 14.5 mohms



eDP_COMP and ICOMPO signals
should be shorted near balls
and routed with typical
impedance <25 mohms

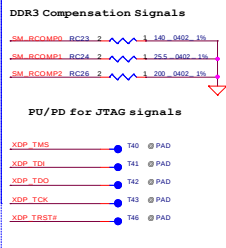
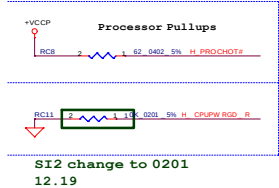
NOTE: eDP_COMP and eDP_ICOMPO
should not be left floating even if Internal
Graphic is disabled since they are shared
with other interfaces



10/05 Change to 0.22uF.

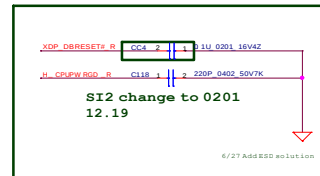
Typ- suggest 220nF. The change in AC capacitor
value from 180nF to 265nF is to enable
compatibility with future platforms having PCIe
Gen3 (8GT/s)

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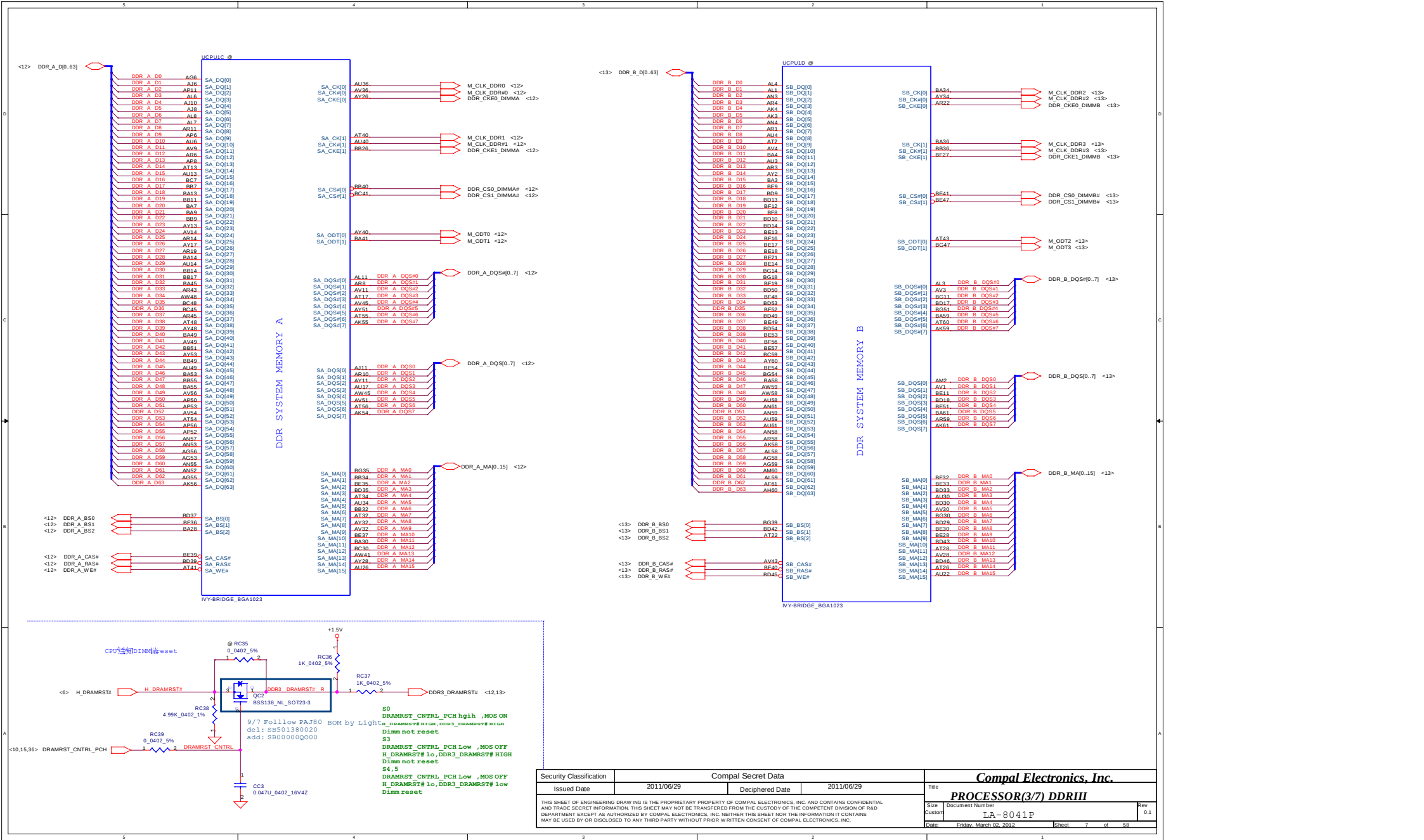


SI2 change to 0201
12.19

XDP_RST# 1 2
C264 220P_0402_50V7K
PLT_RST# 1 2
C265 100P_0402_50V8J
PM_SYS_PWRGD_BUF 1 2
C266 220P_0402_50V7K
BUF_CPU_RST# 1 2
C263 0.1U_0201_16V4Z



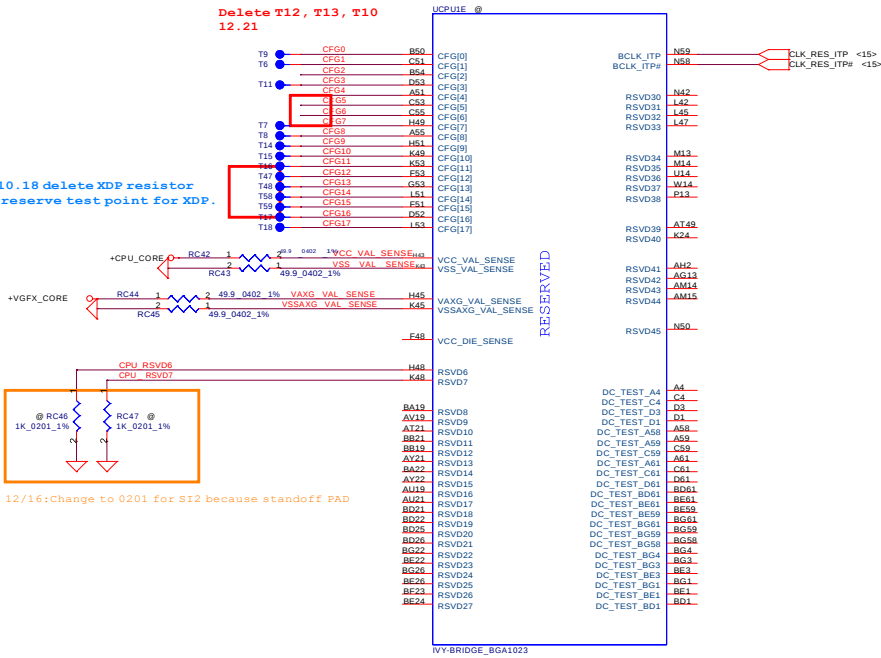
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Change to part G.

Delete T12, T13, T10
12.21

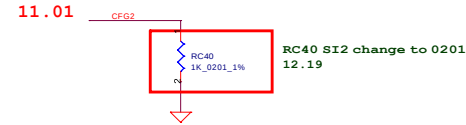
2011.10.18 delete XDP resistor
just reserve test point for XDP.



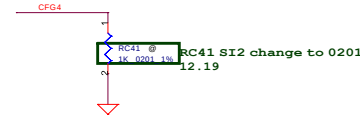
12/16:Change to 0201 for SI2 because standoff PAD

CFG Straps for Processor

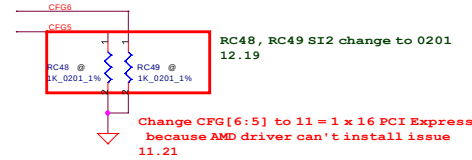
PEG bus is reversed, need to PD.



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	★ 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

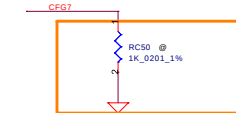


Display Port Presence Strap	
CFG4	★ 1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



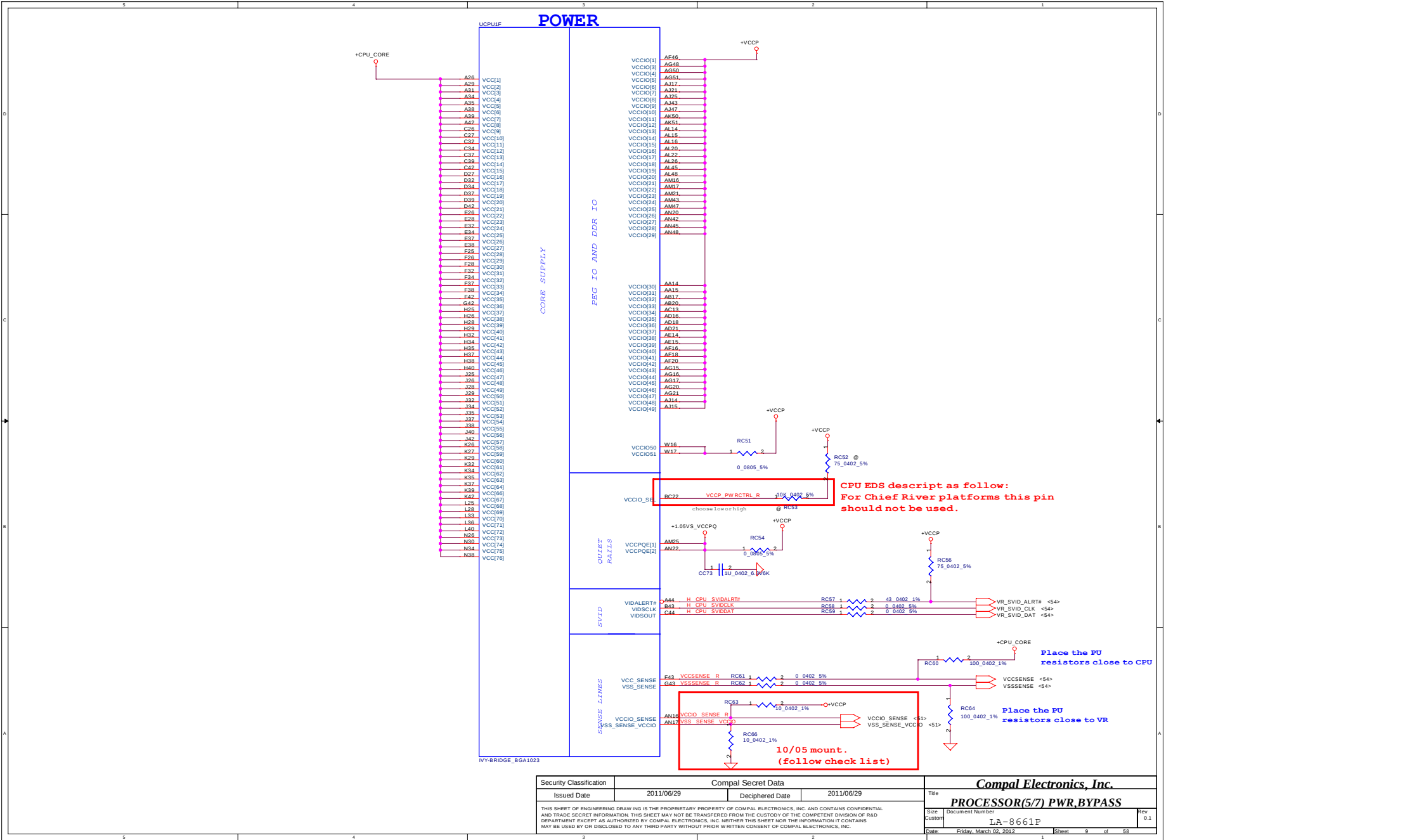
PCIe Port Bifurcation Straps	
CFG[6:5]	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express
★	

12/16:Change to 0201 for SI2 because standoff PAD

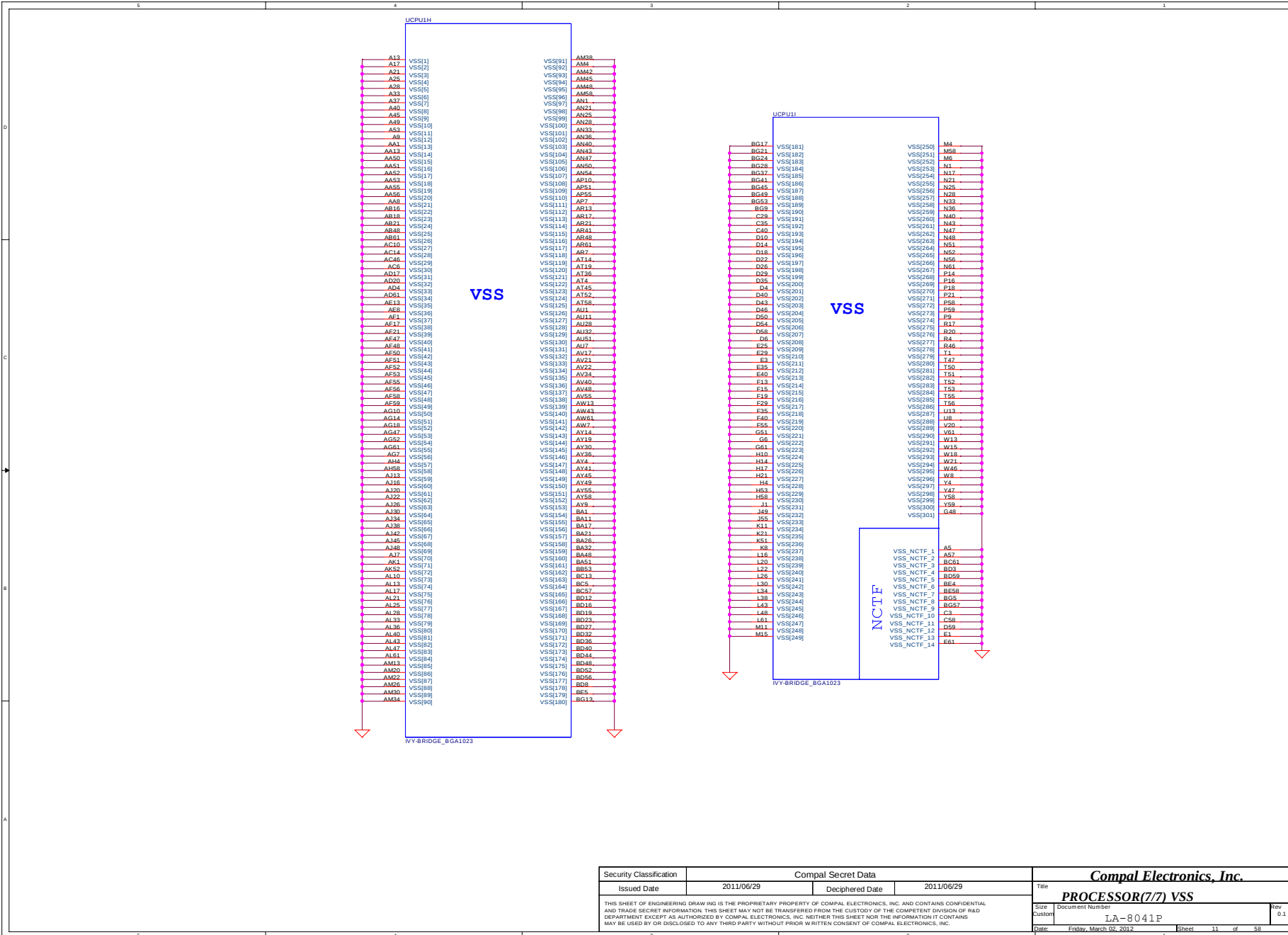


PEG DEFER TRAINING	
CFG7	★ 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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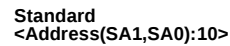


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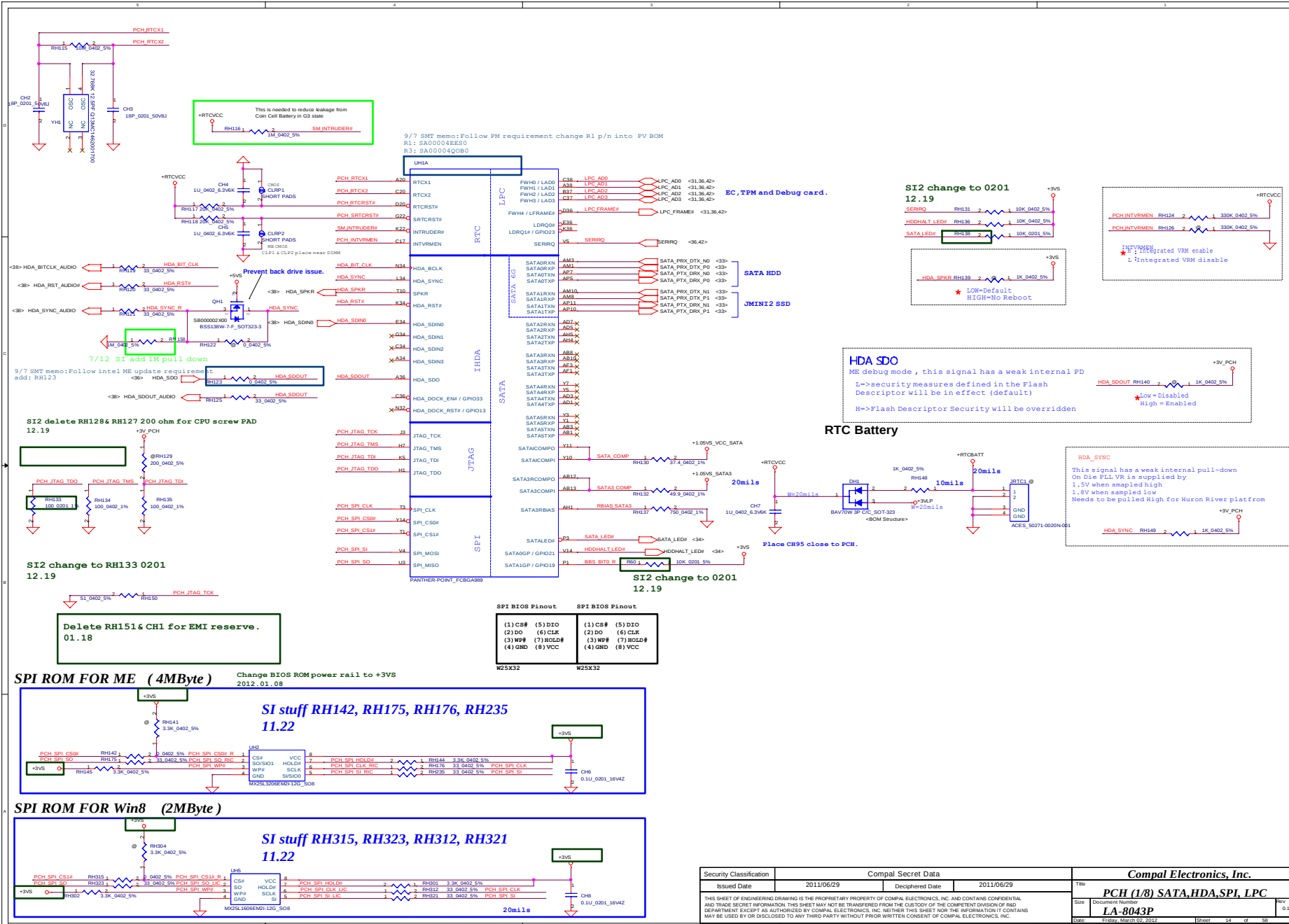


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10/03 change to +V_DDR_REFB



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[illegible]

PCIE LAN/Card Reader

<34> CLK_PCIE_LAN1 RH18 2 1 0 0402 5% PCB LAN1 Y40 CLKOUT_PCIEON
<34> CLK_PCIE_LAN1 RH19 2 1 0 0402 5% PCB LAN1 Y39 CLKOUT_PCIEOP
+3V_PCH RH173 1 1 0201 5% PCIECLKREQ0+ PCIECLKREQ0+ / GPI073
<34> LAN_CLKREQ0+ RH173 1 1 0201 5% PCIECLKREQ0+ PCIECLKREQ0+ / GPI073

MiniWLAN

<31> CLK_PCIE_MINI1 RH178 2 1 0 0402 5% PCB MINI1# AB49 CLKOUT_PCIEIN
<31> CLK_PCIE_MINI1 RH179 2 1 0 0402 5% PCB MINI1# AB47 CLKOUT_PCIEIP

+3V_PCH — RH177 10K 0.201 5% — L12 PCIECLKREQ# / GPIO26
 — V45 CLKOUT_PCIEN
 — V46 CLKOUT_PCIENP
 +3V_PCH — RH274 10K 0.402 5% — L14 PCIECLKREQ# / GPIO44

Change WL_OFF# to GPIO45 (pull-high) +3V_PCH
2012.01.04

CLK_PCH 14M

RH193

CH14

33.0402µs

22P_0201 25V8

Reserve for EMI please close to UH1

CLK_PCI_LPBK

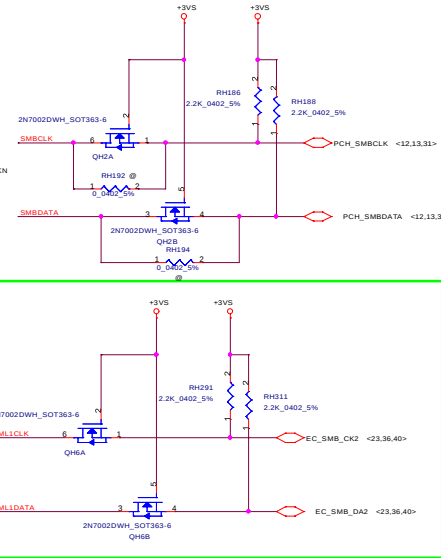
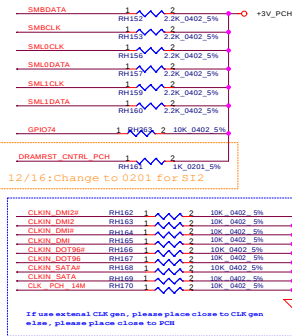
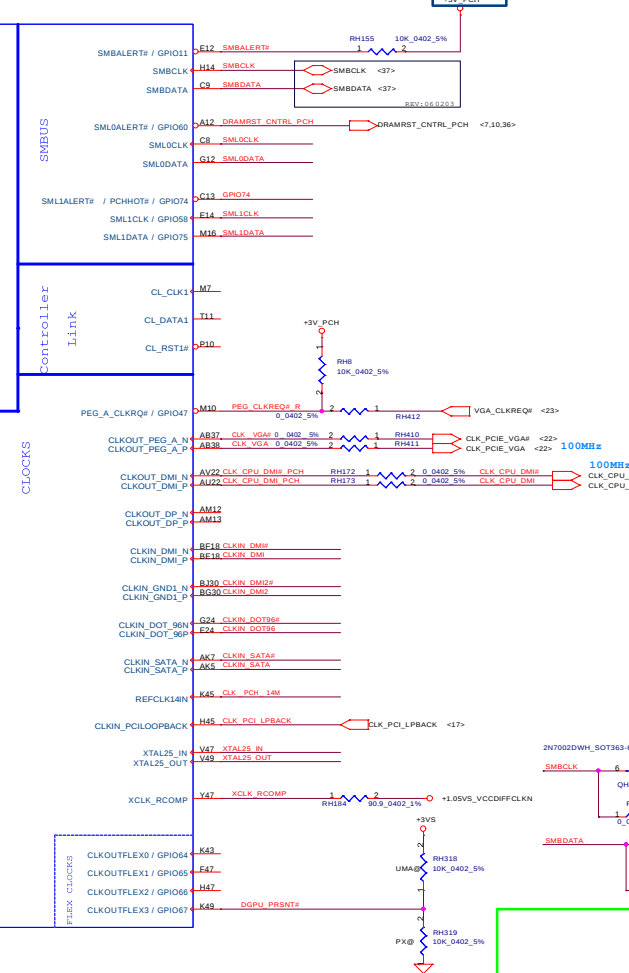
RH195

CH15

33.0402µs

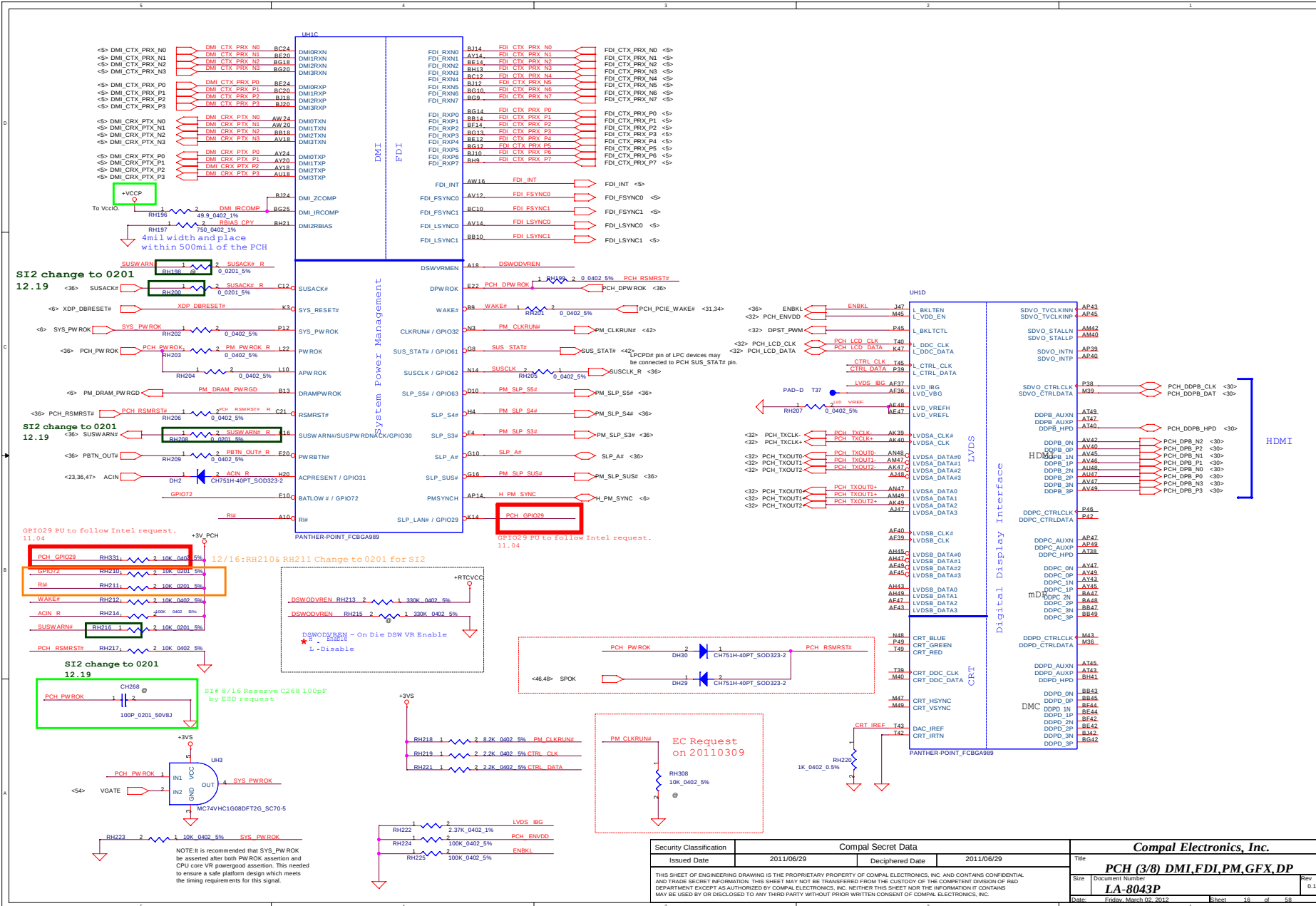
27P_0201 25V8

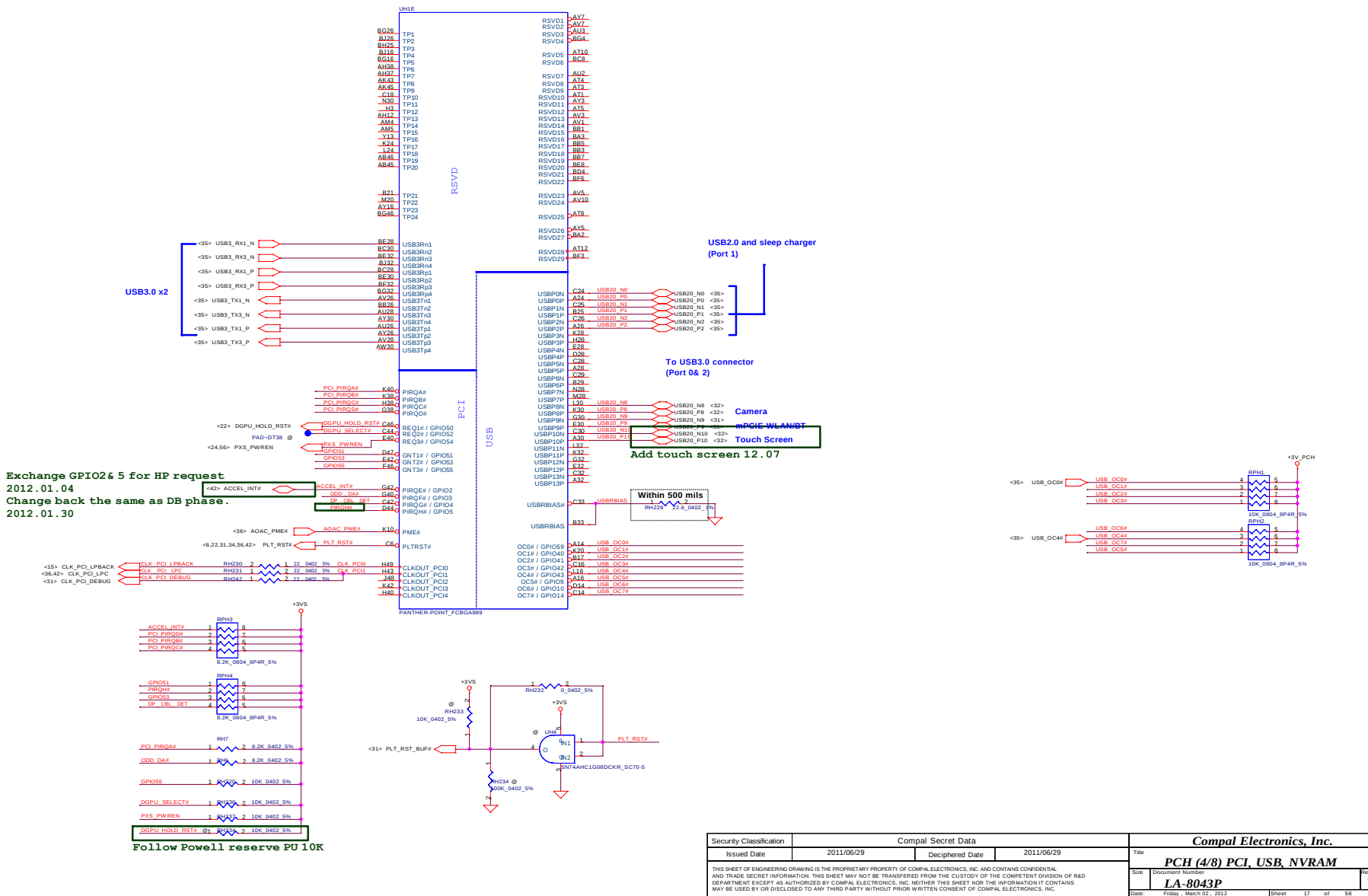
Reserve for EMI please close to UH1



SI# 8/8 Add SML1CLK/SML1DATA for EC detect Thermal

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		Size	Document Number LA-8043P

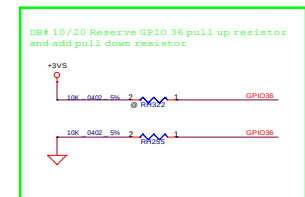
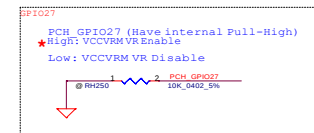
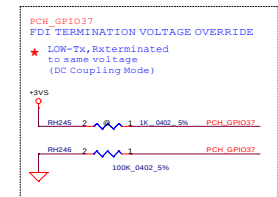
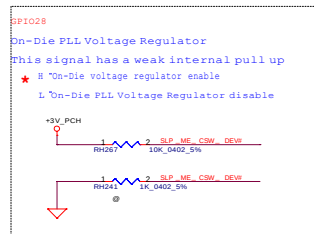




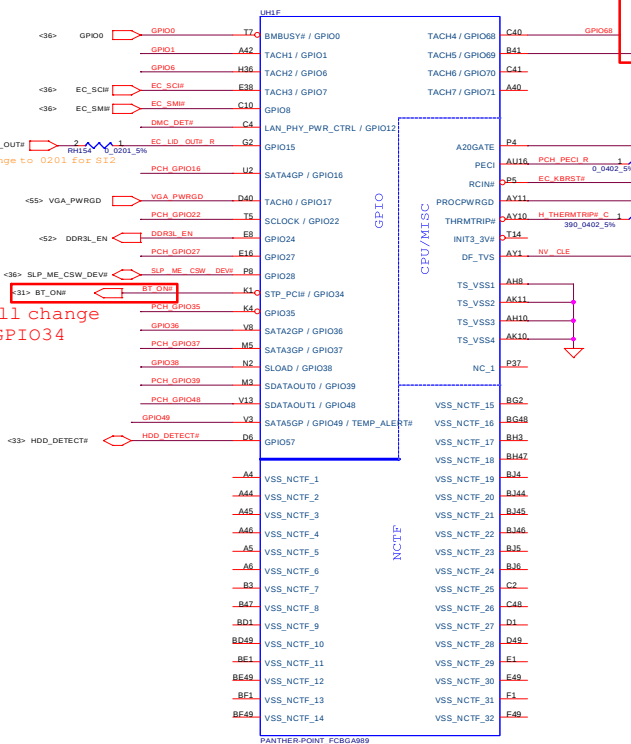
Exchange GPIO2 & 5 for HP request
2012.01.04
Change back the same as DB phase.
2012.01.30

Follow Powell reserve PU 10K

Security Classification	Compal Secret Data			Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	PCH (4/8) PCI, USB, NVRAM	
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Doc No.	Form - 0001.02 - 2012	Sheet	17	of	58

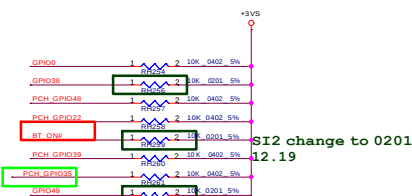
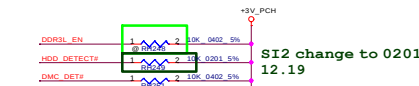
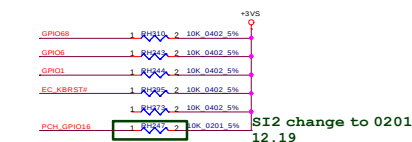


Refer Powell change
BT_ON to GPIO34
10.21



GPIO 69 follow Intel's request PU.
11.04

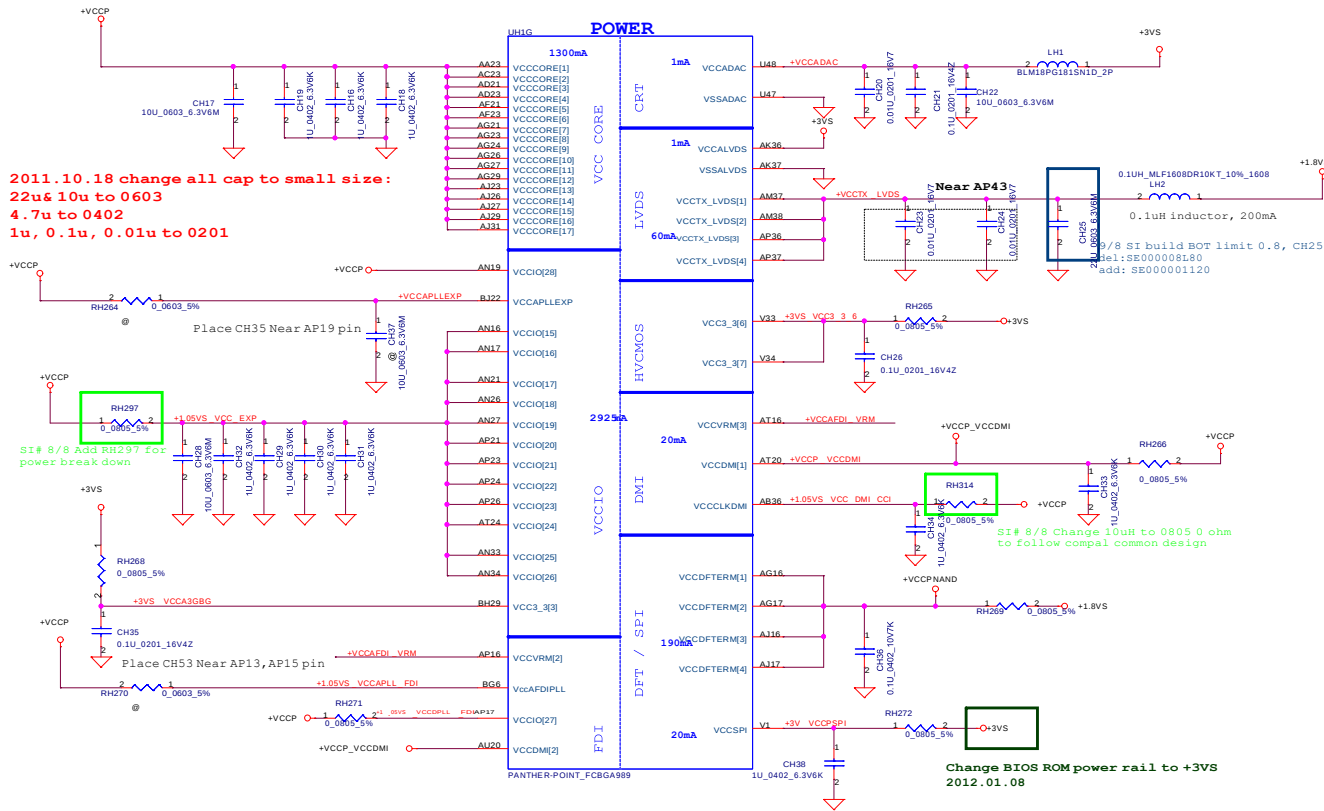
This signal should be connected to the processor's UNCOREPWGRD input to indicate when the processor power is valid.



Refer Powell change
BT_ON to GPIO34
10.21

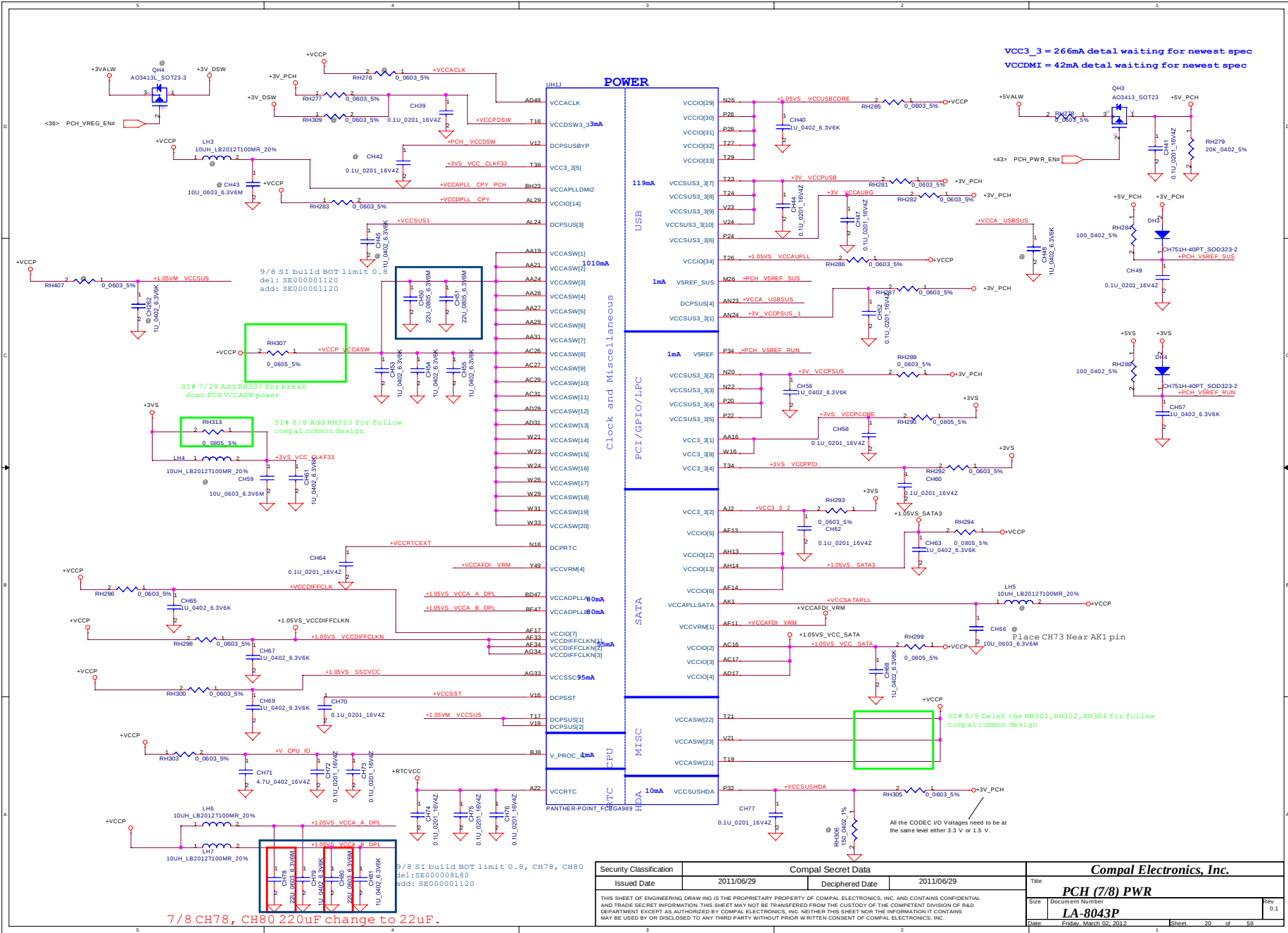
SI# 8/8 change PCH_WAN_RADIO_OFF# to PCH_GPIO35

Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	PCH (5/8) GPIO, CPU, MISC	
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				Doc#	LA-8043P
				Rev	0.1



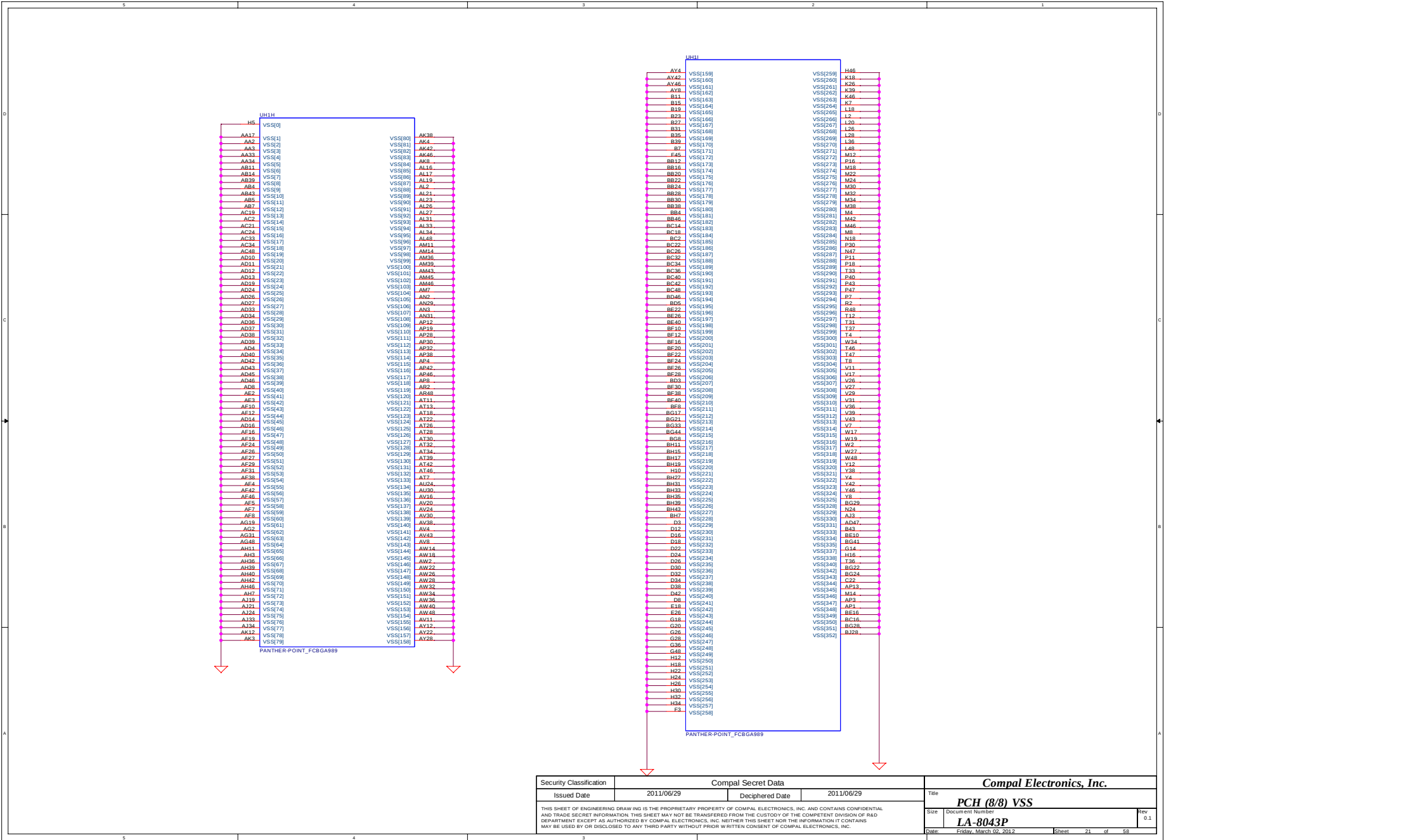
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iocmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	PCH (6/8) PWR
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Compal Secret Data			
Issued Date	2011/06/29	Deciphered Date	2011/06/29
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Compal Electronics, Inc.			
Title			
PCH (7/8) PWR			
Size	Document Number	Rev	
LA-8043P		0.1	
Date	Friday, March 02, 2012	Sheet	20 of 58



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	PCH (8/8) VSS	
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					LA-8043P	0.1
				Date	Friday, March 02, 2012	Sheet 21 of 58

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/30	Deciphered Date	2013/06/30	Title	ATI_SeymourXT_M2_PCIE/LVDS
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Date				Issued	Rev
March 02, 2012				22	01

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/30	Deciphered Date	2013/06/30	Title	ATI_SeymourXT_M2_Main_MSIC
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				C	LA7691P
Date				Issued	March 02, 2012
Page				23	of 58

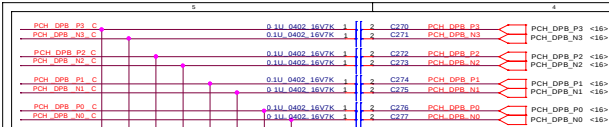
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/30	Deciphered Date	2013/06/30	Title	ATI SeymourXT M2 BACO POWER
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				C	LA7691P
Date				Issued	March 02, 2012
Rev				24	02 58

Security Classification		Compal Secret Data		Title		Compal Electronics, Inc.		
Issued Date	2011/06/30	Deciphered Date	2013/06/30	ATI SetmountXT M2 PWR GND				
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				LA7691P				
				Date	Friday, March 09, 2012	Entered	PS	of

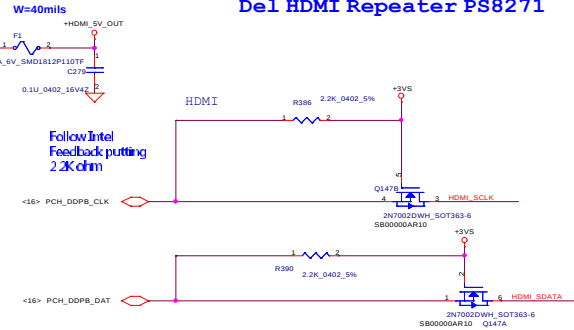
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/30	Deciphered Date	2013/06/30	Title	ATI SeymourXT M2 MEM IF	
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				LA7691P		
Date	Friday, March 09, 2012		Sheet	27 of 58		

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/30	Deciphered Date	2013/06/30	Title	ATI SevmourXT M2 VRAM A
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				C	LA7691P
Date				Friday, March 02, 2012	Sheet 26 of 50

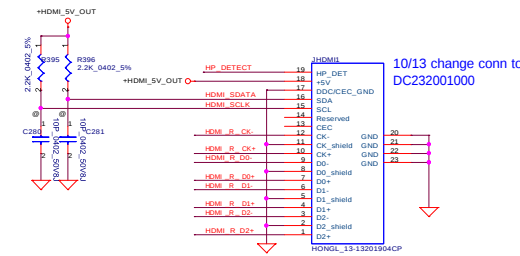
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/30	Deciphered Date	2013/06/30	Title	ATI SevmourXT M2 VRAM B
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				C	LA7691P
				Date	Friday, March 02, 2012 12:04:29 PM



Del HDMI Repeater PS8271



5V PULL UP IN CONNECTER SIDE



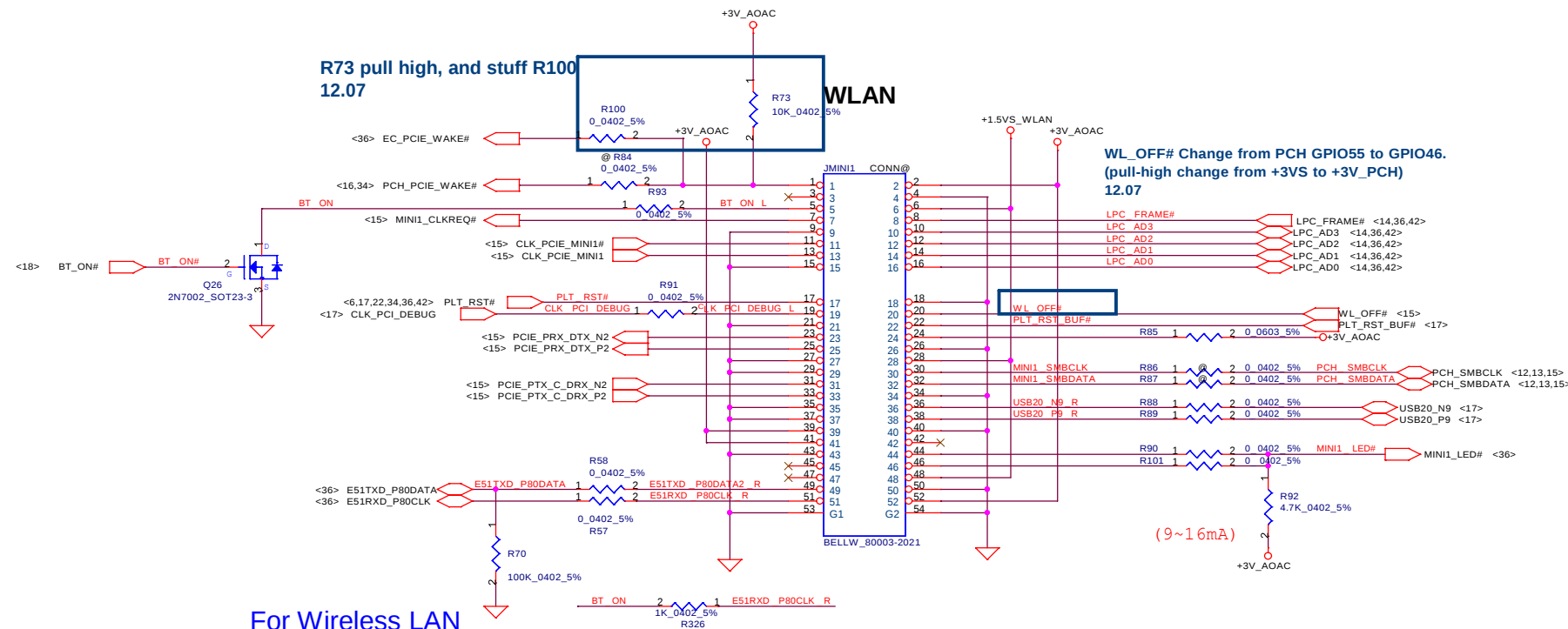
Follow EMI request add 33pF cap to GND .
11.02

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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	HDMI Conn
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DATE: 2011/06/29 2012					Page: 30 of 38

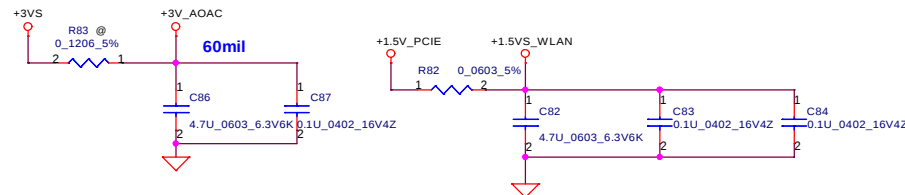
R73 pull high, and stuff R100
12.07

WLAN

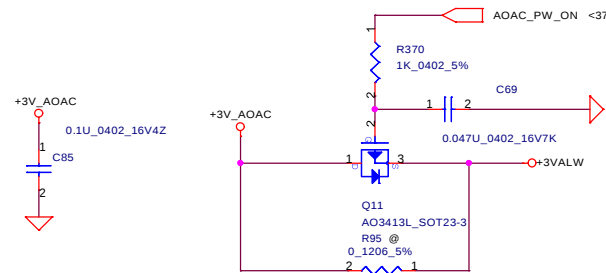
WL_OFF# Change from PCH GPIO55 to GPIO46.
(pull-high change from +3VS to +3V_PCH)
12.07



For Wireless LAN



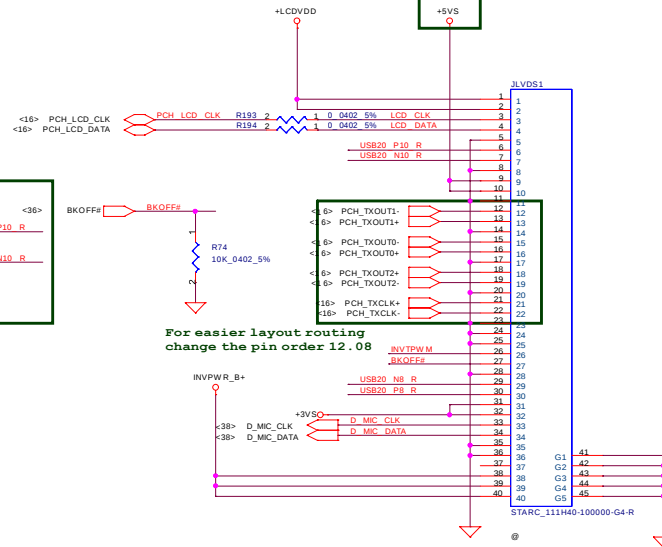
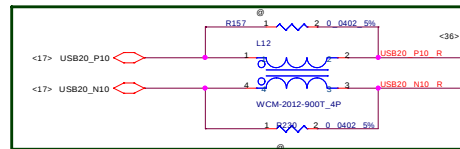
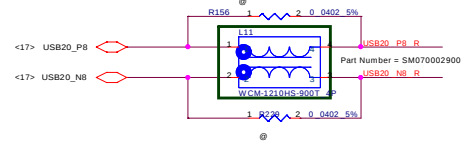
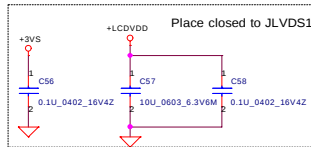
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



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						Size	Document Number			Rev		
						LA-8042P				0.1		
						Date	Friday, March 02, 2012			Sheet	31 of 58	

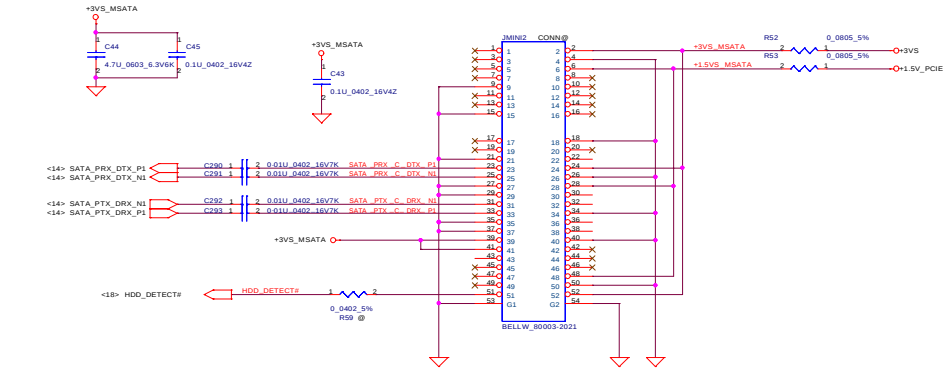


SI# 8/15 R62 change to +3VALW, R61 change to 10 ohm, R63 change to 200Kohm



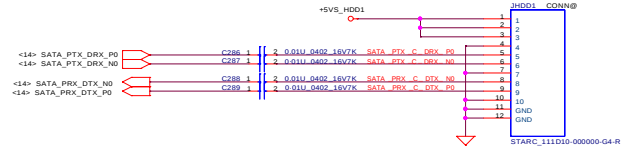
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mSATA Conn.

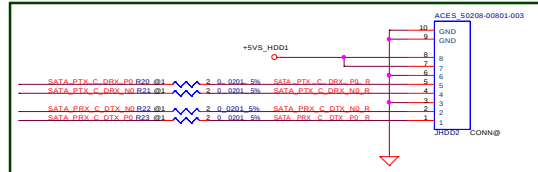
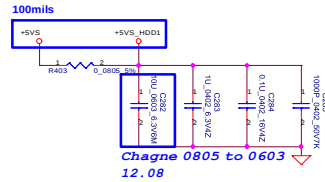


Exchange port 0 & port 1 for SI as customer request
11.30

Change footprint to Starconn (PAD is bigger)
11.30



SATA connector



Co-layout for wire type connector

01.16

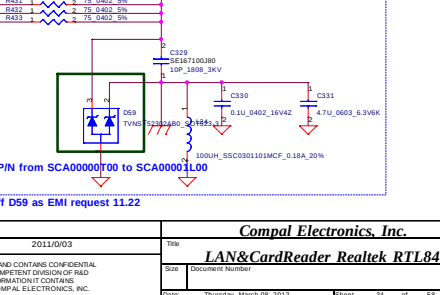
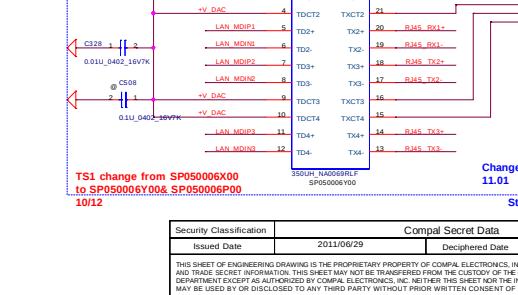
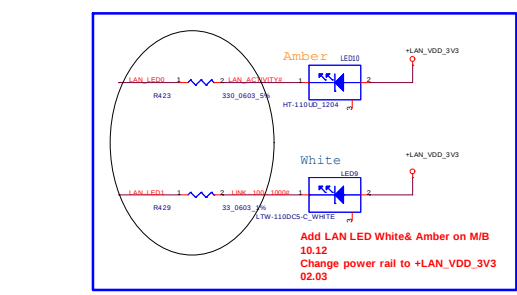
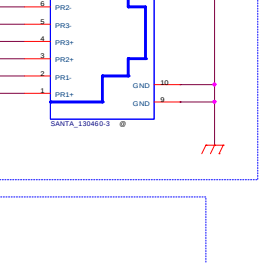
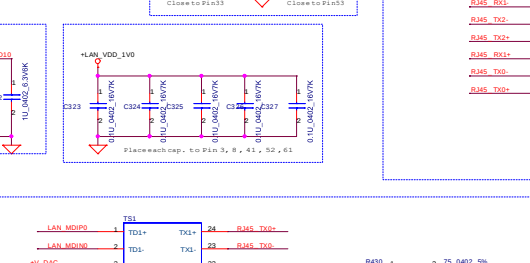
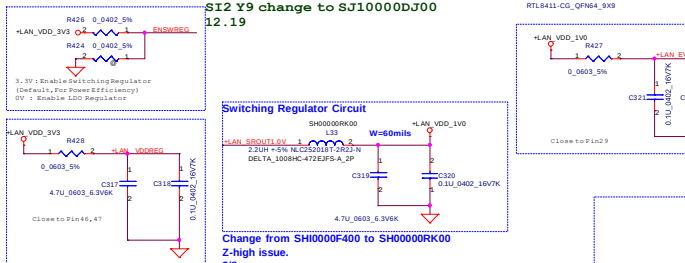
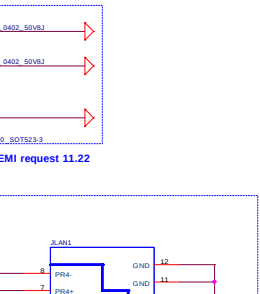
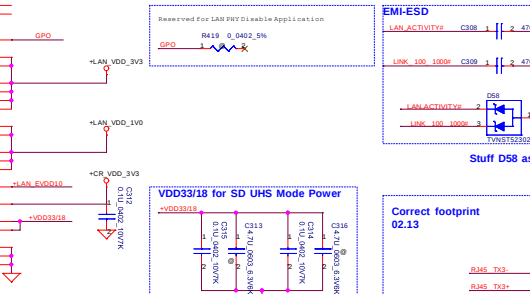
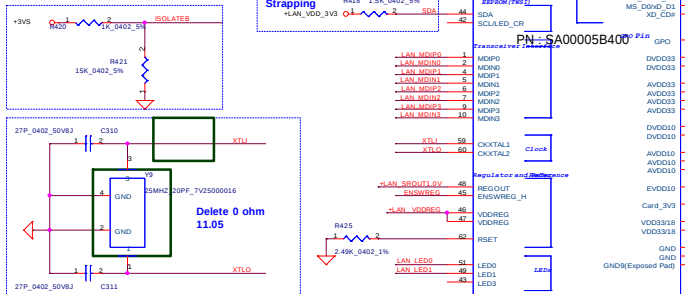
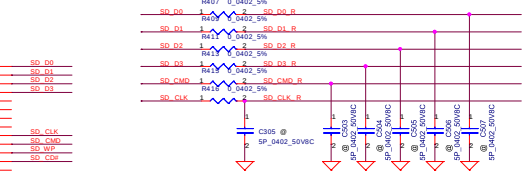
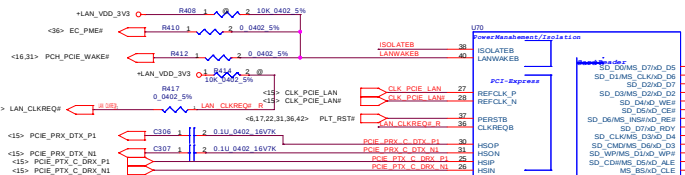
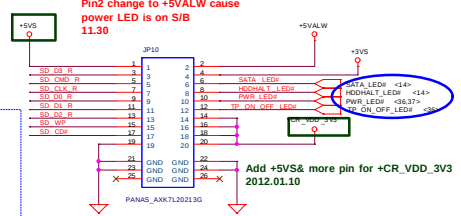
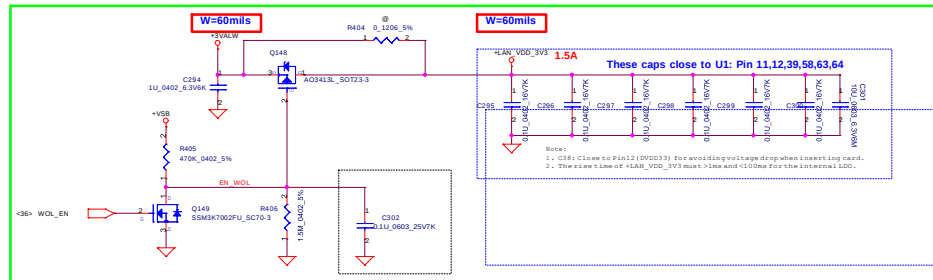
Change connector to ACES_50376

01.31

Change connector to ACES_50208 because current limit issue

02.06

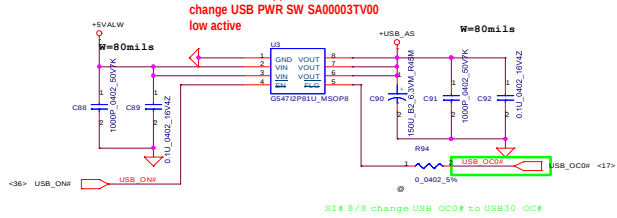
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	mSATA Connector
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Date				File	March 02, 2012
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Security Classification			Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/0/3		Title	LAN&CardReader Realtek RTL8411
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Date	Thursday, March 08, 2012	Drawn	34	df	68	

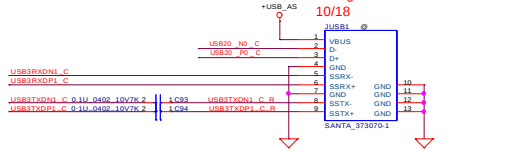
USB3.0

USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active

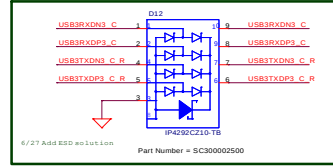
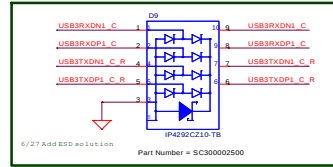
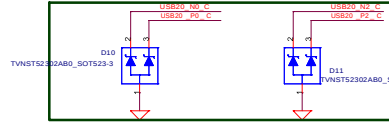


S1# 8/8 change USB OC0# to USB30_OC#

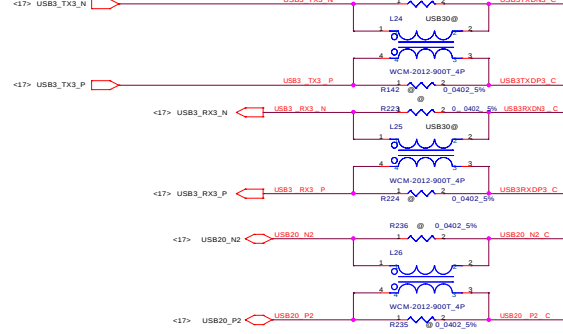
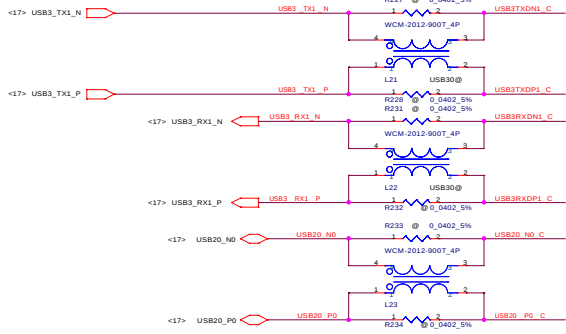
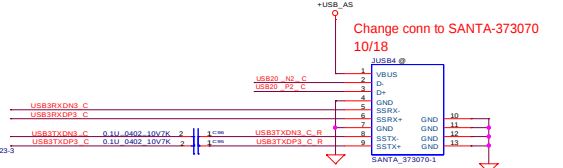
Change conn to SANTA-373070
10/18



Change P/N from SCA00000T00 to SCA00001L00
11.01
Change P/N to SCA00001W00 for smaller size, 10*10 choke
02.13

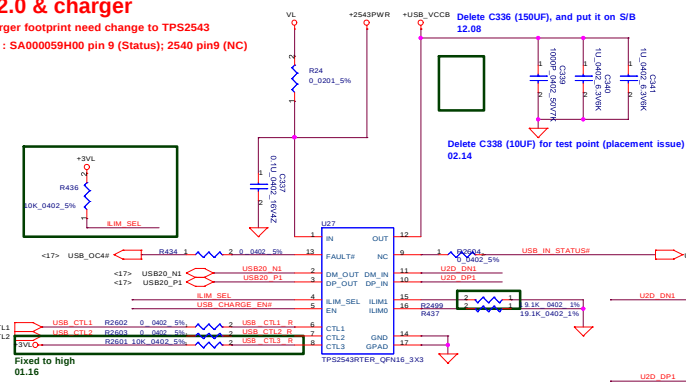


Change conn to SANTA-373070
10/18

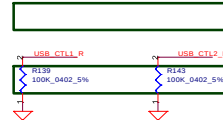


USB2.0 & charger

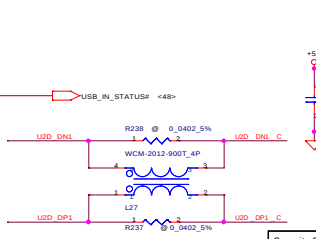
USB charger footprint need change to TPS2543
TPS2543 : SA000059H00 pin 9 (Status); 2540 pin9 (NC)



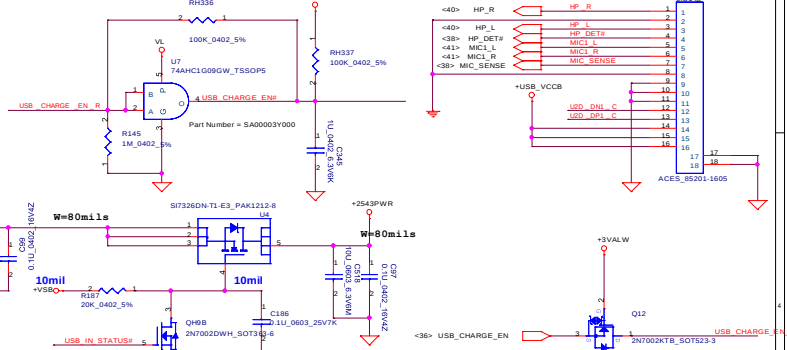
Delete pull-high resistors
01.16



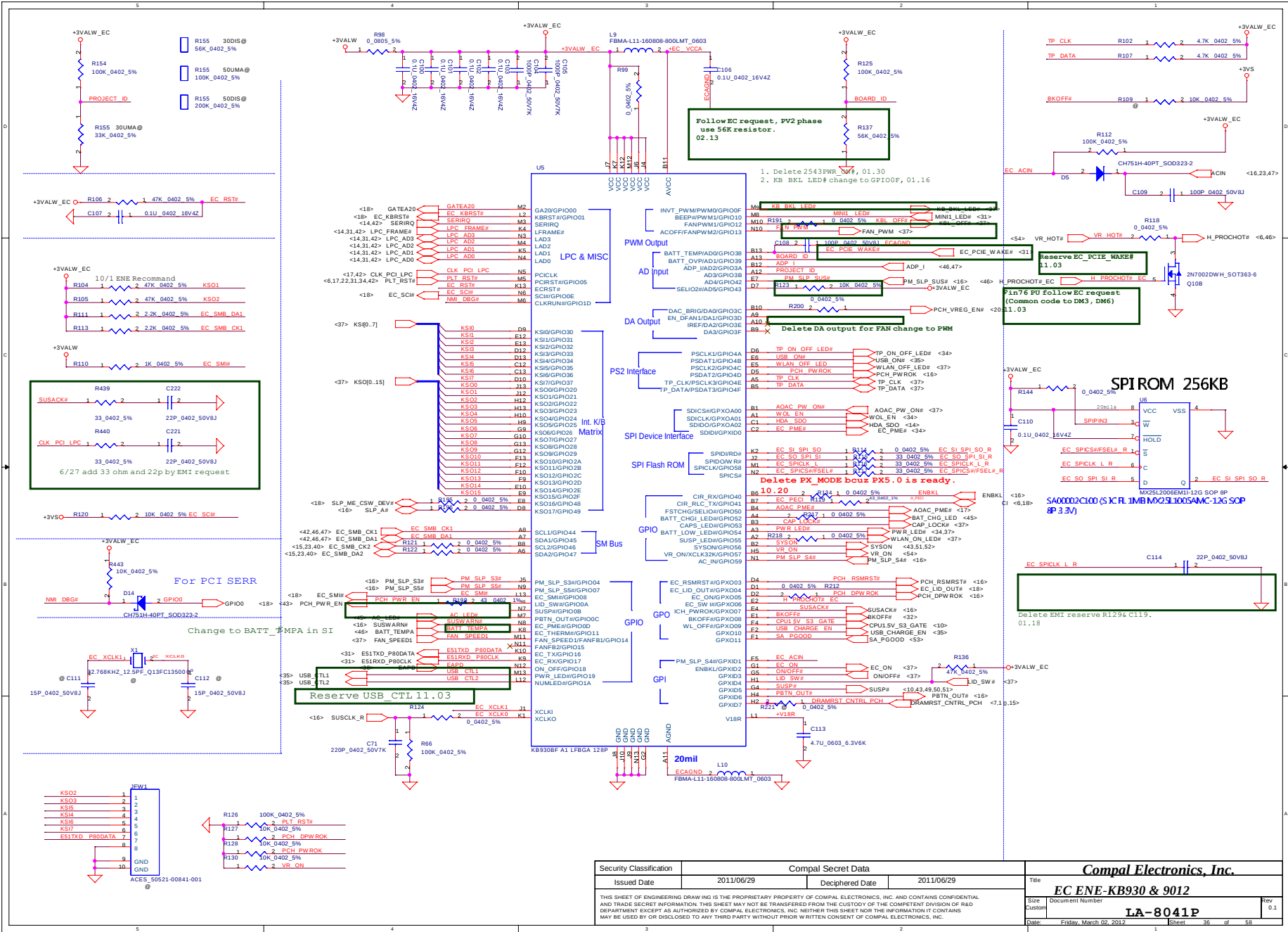
Delete C338 (10uF) for test point (placement issue)
02.14



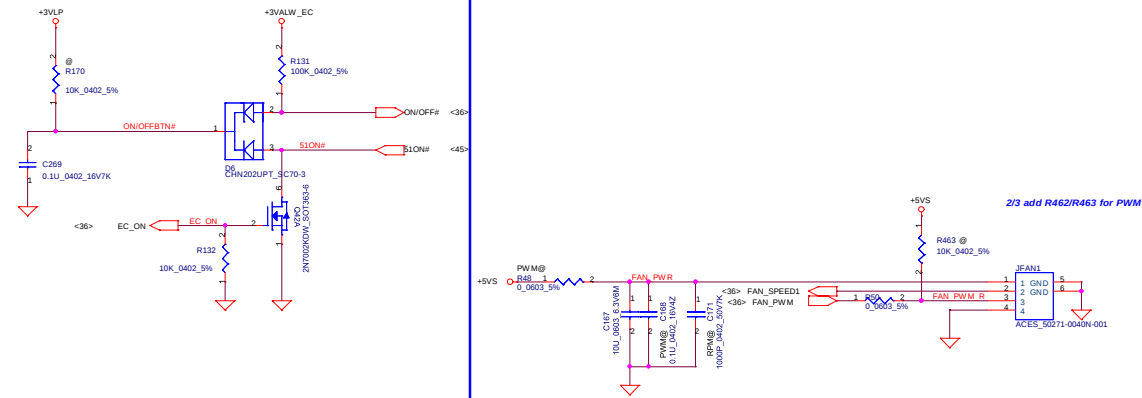
Follow EMI request add choke
11.08



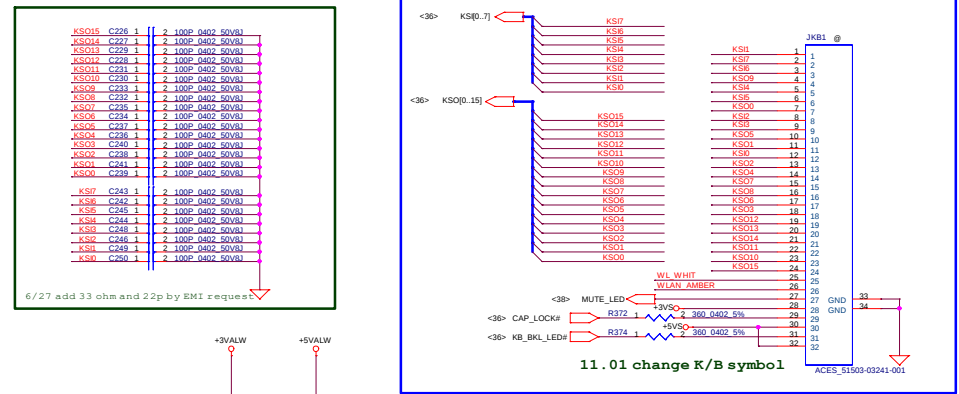
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	USB Con & Daughter Con
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				Date	Monday, March 09, 2012
				Sheet	35 of 38
				Rev	0.1



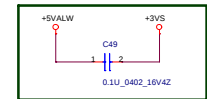
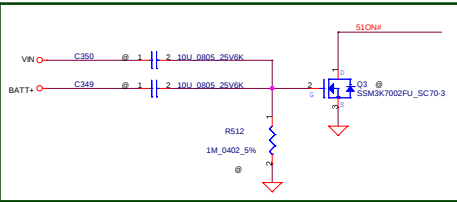
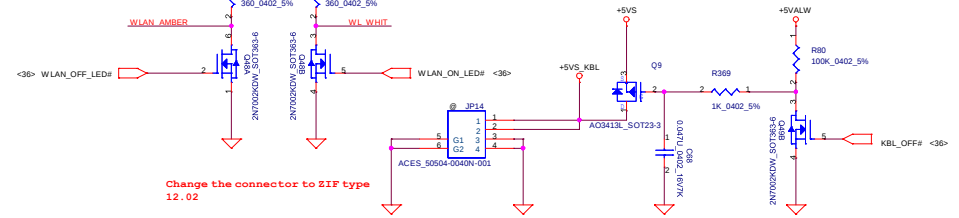
PWM Fan Control circuit



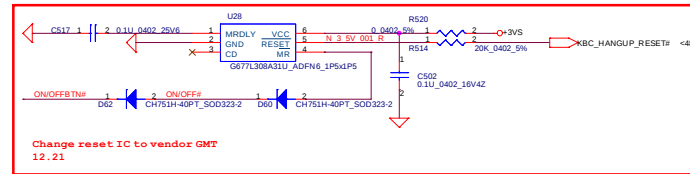
Follow thermal (FAN) design guide, pull-high 10K
12.05



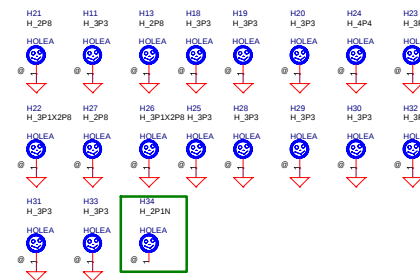
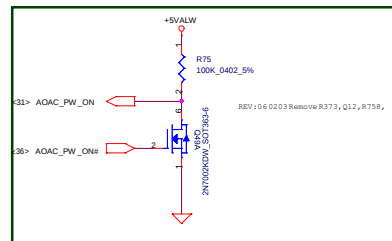
Keyboard backlight Conn



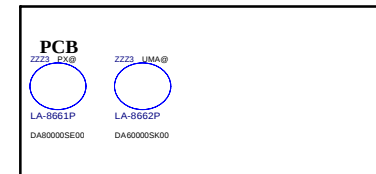
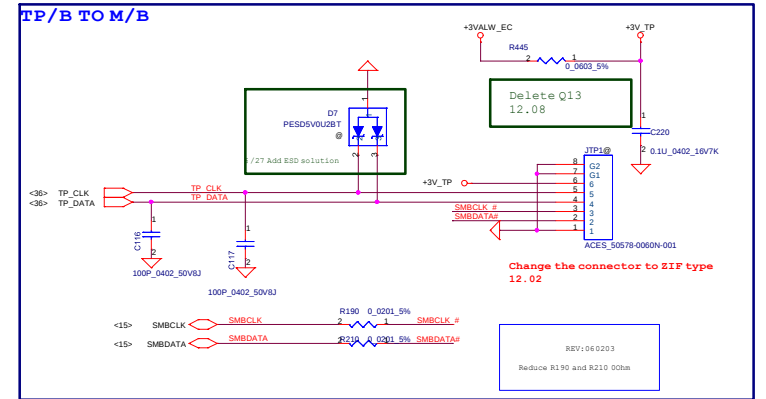
Add C49 as EMI request.
12.05



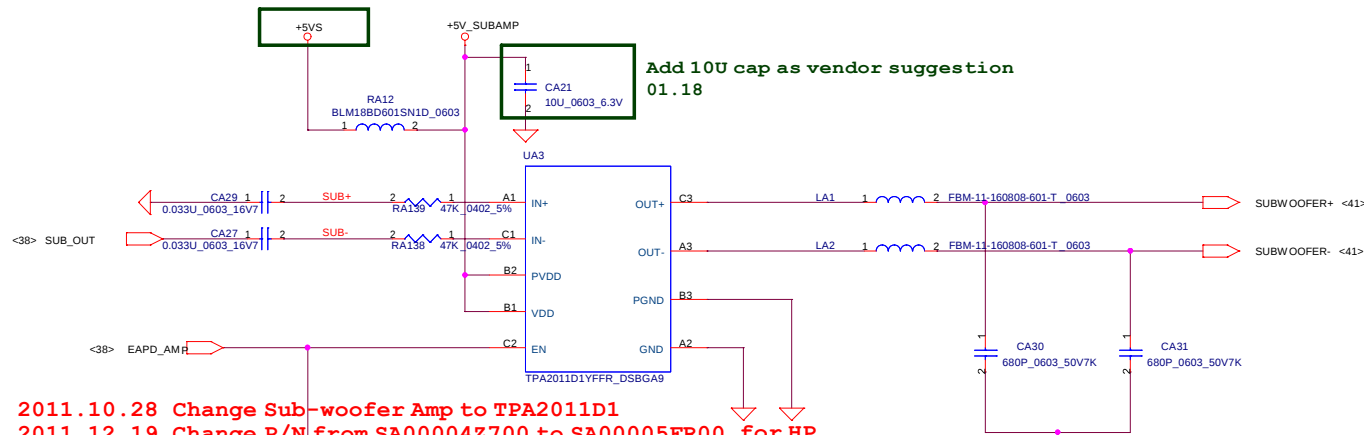
Change reset IC to vendor GMT
12.21



12/15: Add NPTH H34

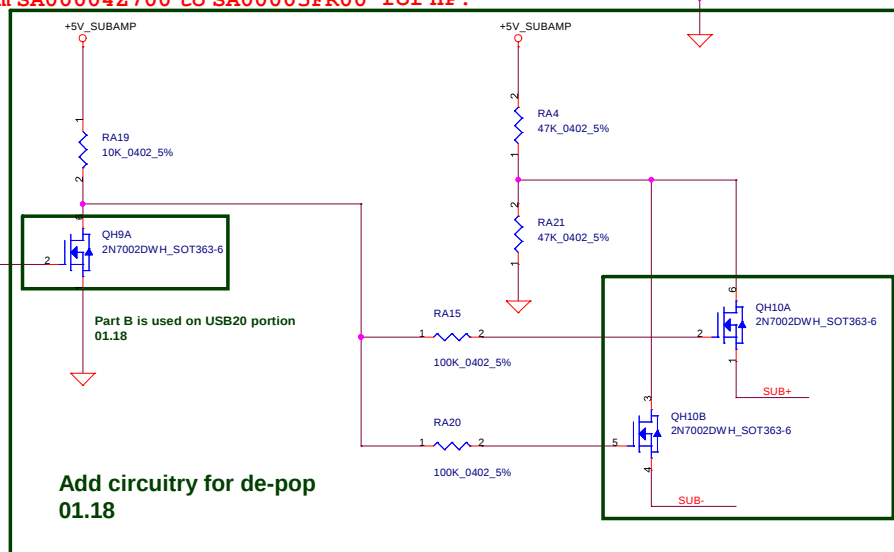


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	KB/TP/LED/FAN/Screw/Gsensor	
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				Custm	LA-8041P	
				Date	Saturday, March 03, 2012	Sheet



2011.10.28 Change Sub-woofer Amp to TPA2011D1

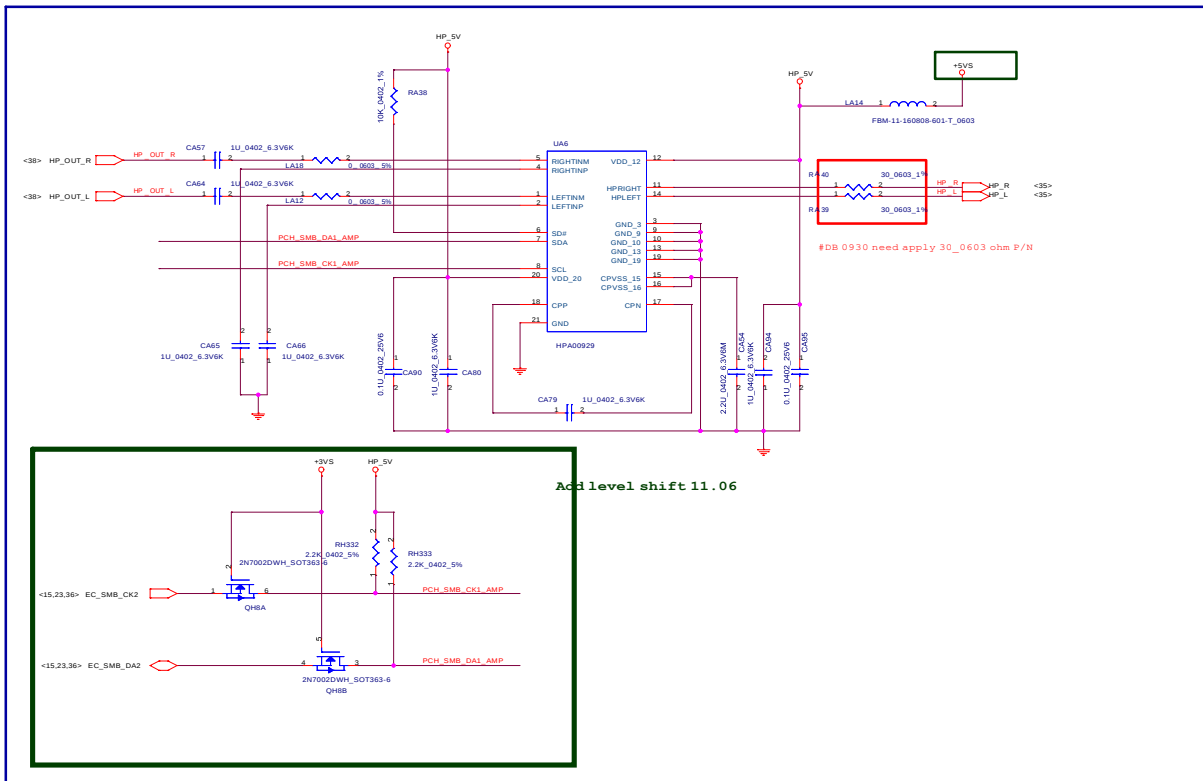
2011.12.19 Change P/N from SA00004Z700 to SA00005FR00 for HP.



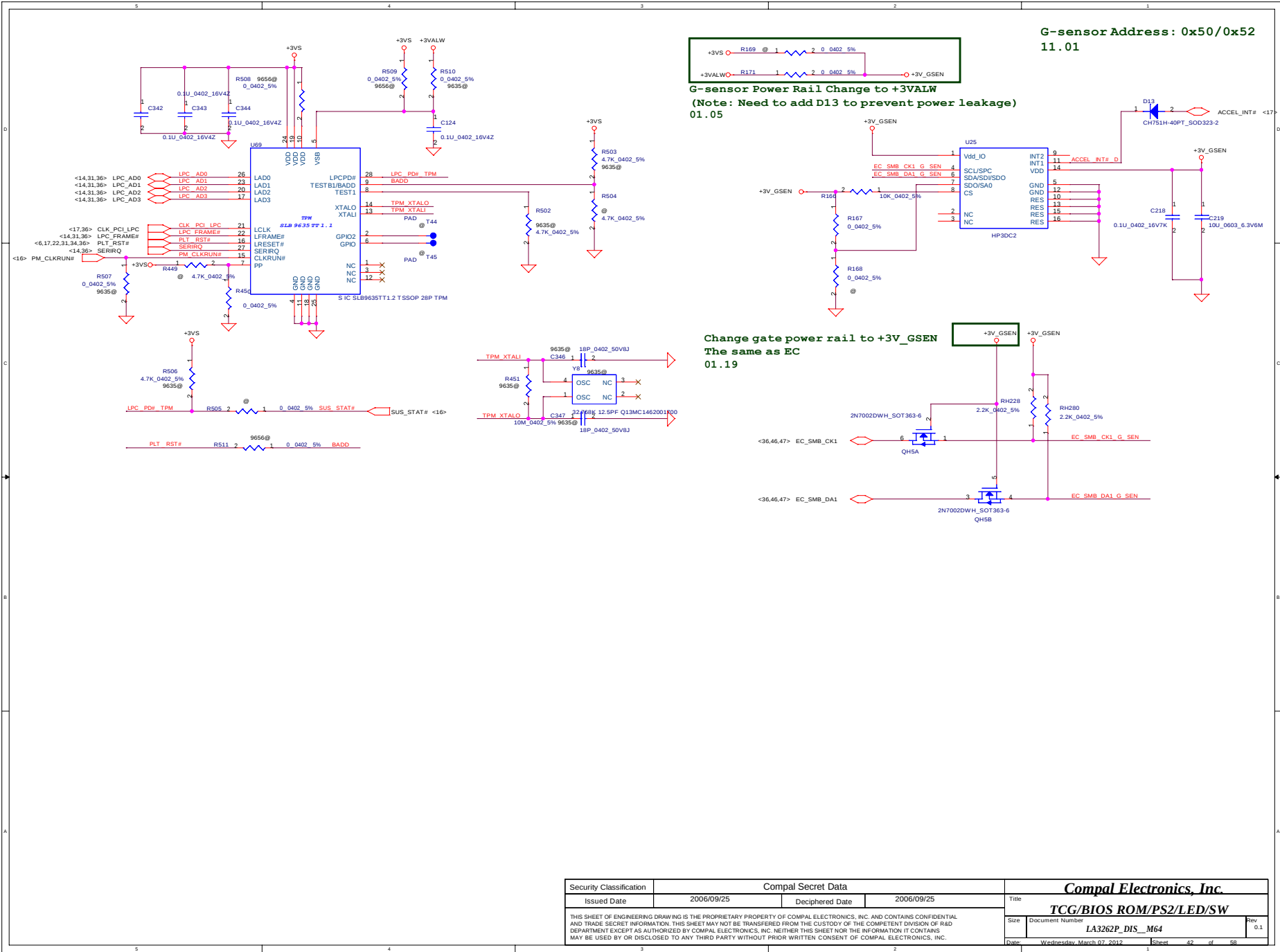
QH10 must change to BJT before SMT
(Footprint is compatible from BJT& MOTFET)
01.18
BJT P/N: SB00000VH00

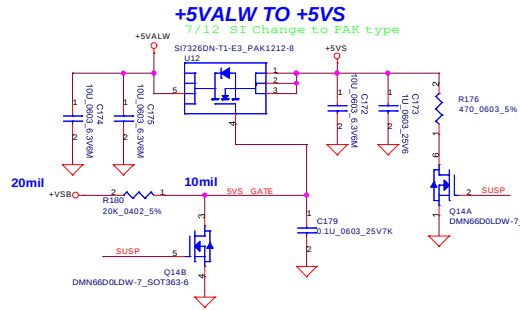
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title		
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				Size	Document Number	Rev
				B		0.1
				Date	Friday, March 02, 2012	Sheet 39 of 58

Headphone amplifier

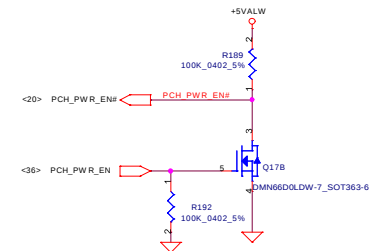
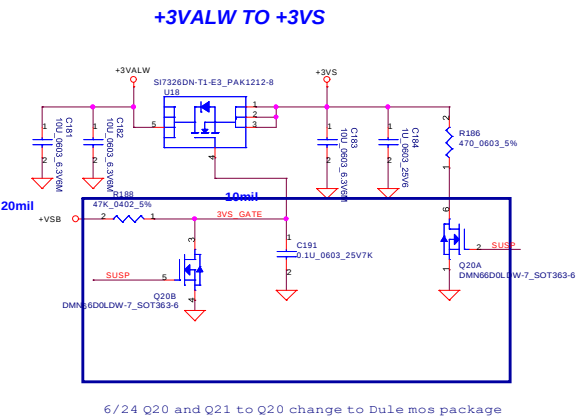
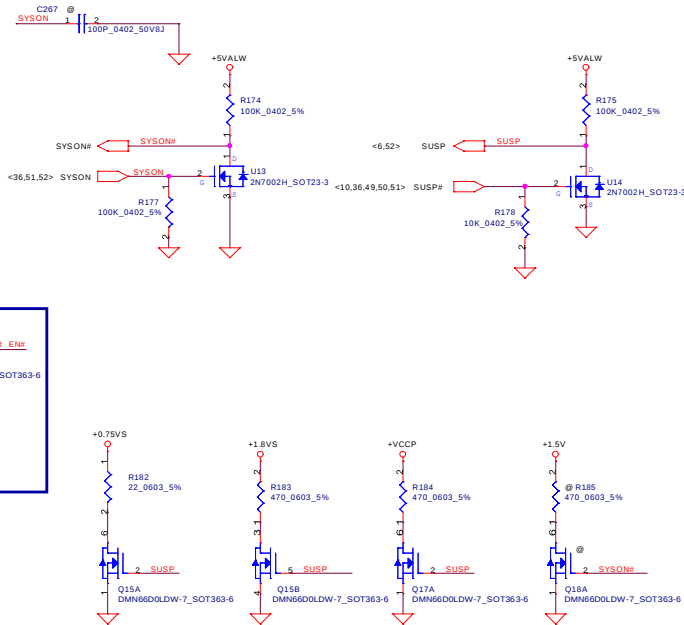
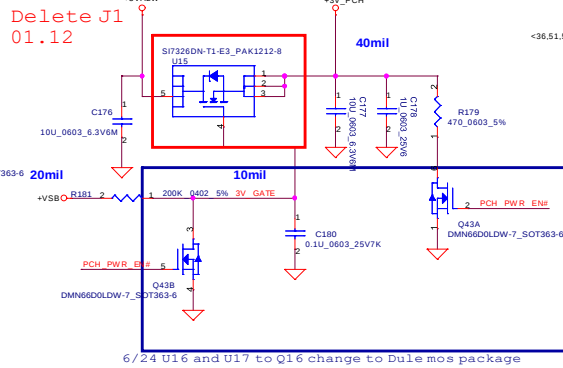


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Issued Date 2011/06/29	Deciphered Date 2011/06/29	Title Audio SPK/HP Amplifier
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		Date Wednesday, March 07, 2012 Sheet - 40 - of 58





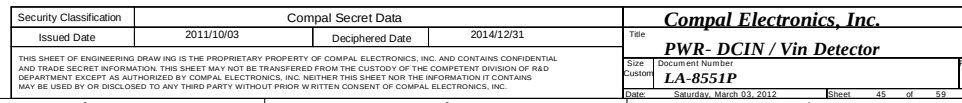
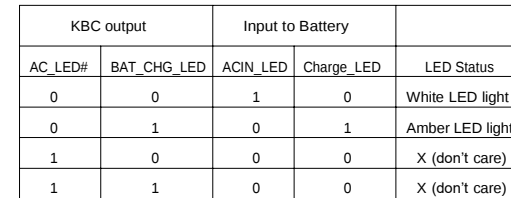
10.21 Change to PAK type
+3VALW TO +3VALW(PCH AUX Power)
Short J1 for PCH VCCSUS3.3



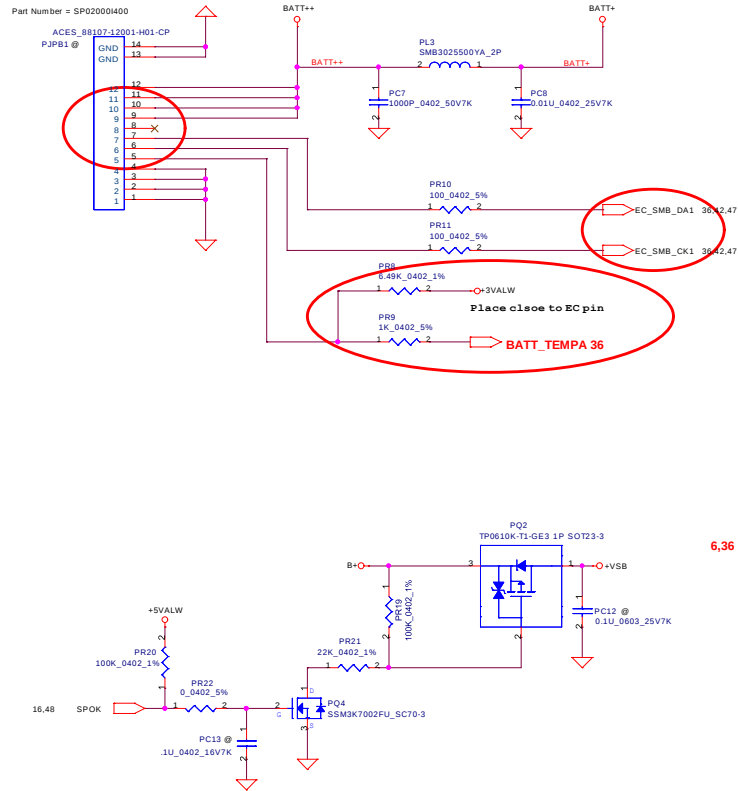
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	
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				Custom	LA-8661P
				Date	Friday, March 02, 2012
				Sheet	43 of 58
				Rev	0.1

	QA260 Strap pin Table		@:un_install	
	Netname	setting	BOM config	
CPU	CFG2	1	RC40 @	1: Normal Operation; Lane # definition matchessocket pin map definition 0: Lane Reversed
	CFG4	1	RC41 @	1 : Disabled; No Physical Display Portattached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
	CFG[6:5]	0 1	RC49 RC48 @	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
	CFG7	1	RC50 @	1: (Default) PEG Train immediately following xRESETB de assertion 0: PEG Wait for BIOS for training
PCH	PCH_INTVRMEN	H	RH124 RH126 @	H : Integrated VRM enable L : Integrated VRM disable
	HDA_SPKR	L	RH139 @	H:No Reboot L:Default
	HDA_SYNC	H	RH149	This signal has a weak internal pull-downOn Die PLL VR is supplied by H:1.5V when smapled high L:1.8V when sampled low Needs to be pulled High for Huron River platfrom
	HDA_SDOUT	L	RH140 @	ME debug mode , this signal has a weak internal PD L=>security measures defined in the Flash Descriptor will be in effect (default) H=>Flash Descriptor Security will be overridden
	DSWODVREN	H	RH213 RH215 @	On Die DSW VR Enable H : Enable L : Disable
	SLP_ME_CSW_DEV#	H	RH267 RH241 @	On-Die PLL Voltage Regulator This signal has a weak internal pull up H : On-Die voltage regulator enable L : On-Die PLL Voltage Regulator disable
	PCH_GPIO37	L	RH245 @ RH246	FDI TERMINATION VOLTAGE OVERRIDE L: Tx, Rx terminated to same voltage(DC Coupling Mode)
	GPIO27	H	RH250 @	PCH_GPIO27 (Have internal Pull-High) H: VCCVRM VR Enable L: VCCVRM VR Disable

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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Strap pin table	
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For KB930 --> Keep PU1 circuit
(Vth = 0.825V)



PH1 under CPU bottom side :
CPU thermal protection at 90 +/-3 degree C
Recovery at 56 +/-3 degree C

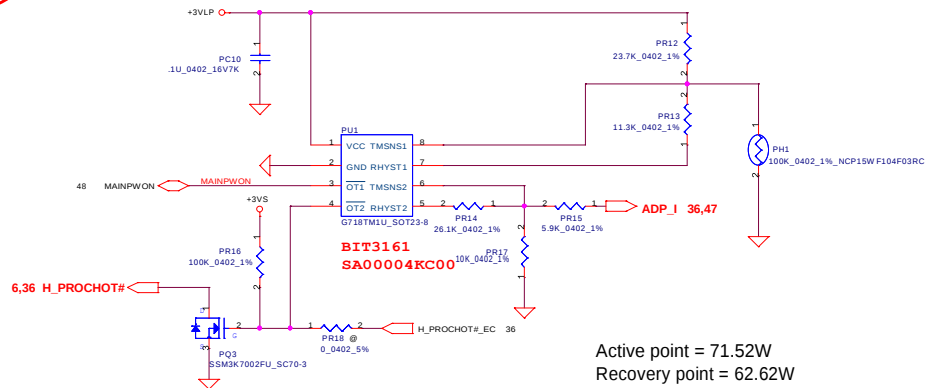
$$R_{set} = 3 * R_{tmh}$$

$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

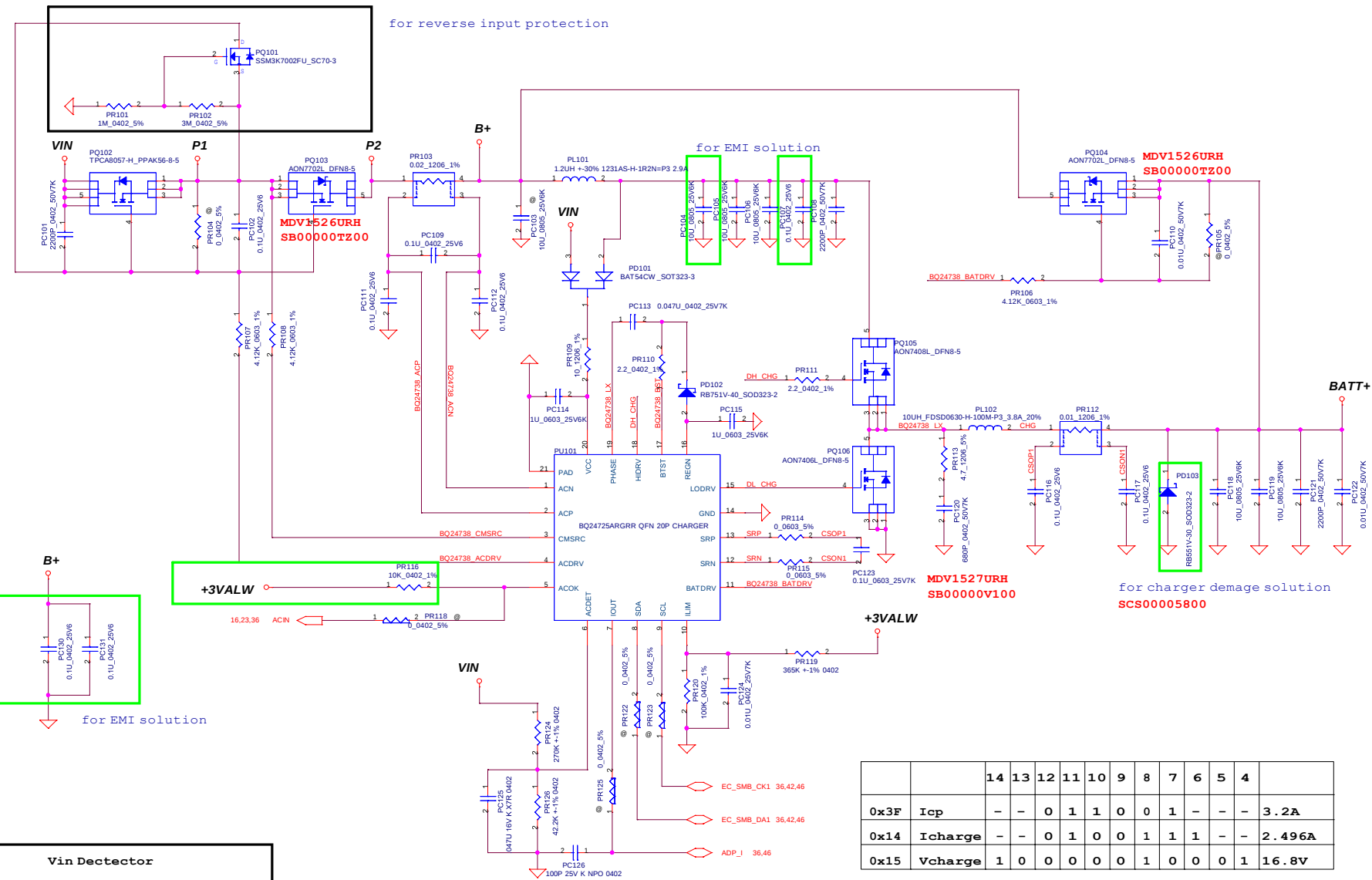
$$R_{tmh} \text{ at } 90C = 7.8K, R_{tml} \text{ at } 56C = 26.1K$$

$$R_{set} = 3 * 7.8K = 23.4K \Rightarrow 23.7K$$

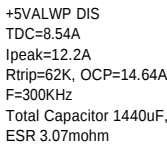
$$R_{hyst} = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K \Rightarrow 11.3K$$



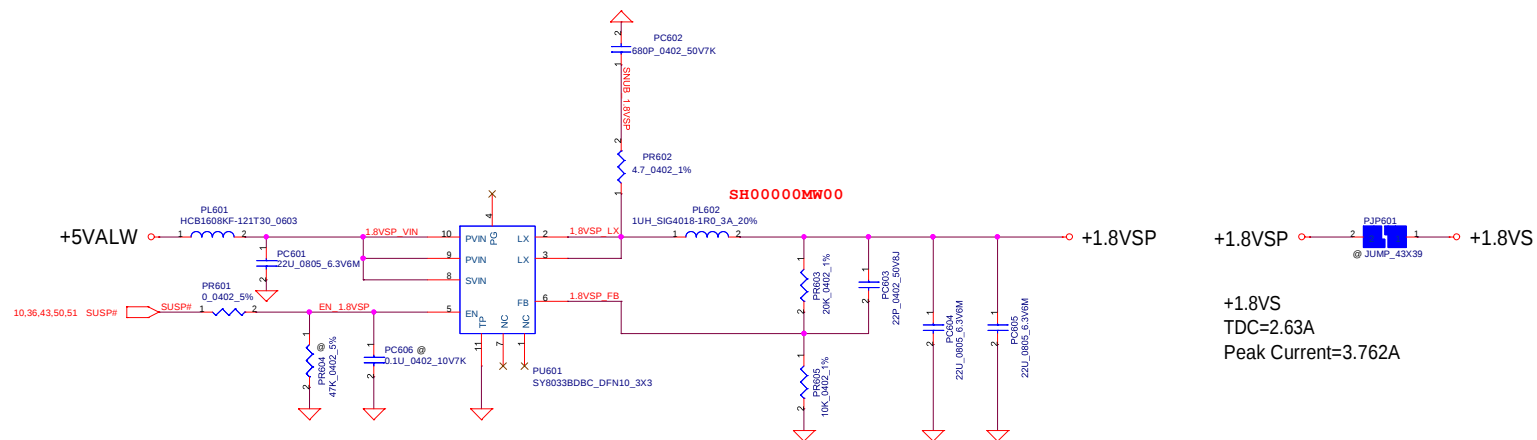
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Issued Date	2011/10/03	Deciphered Date	2014/12/31	Title
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				LA-8551P
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				Size	Document Number	Rev
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			Document Number	

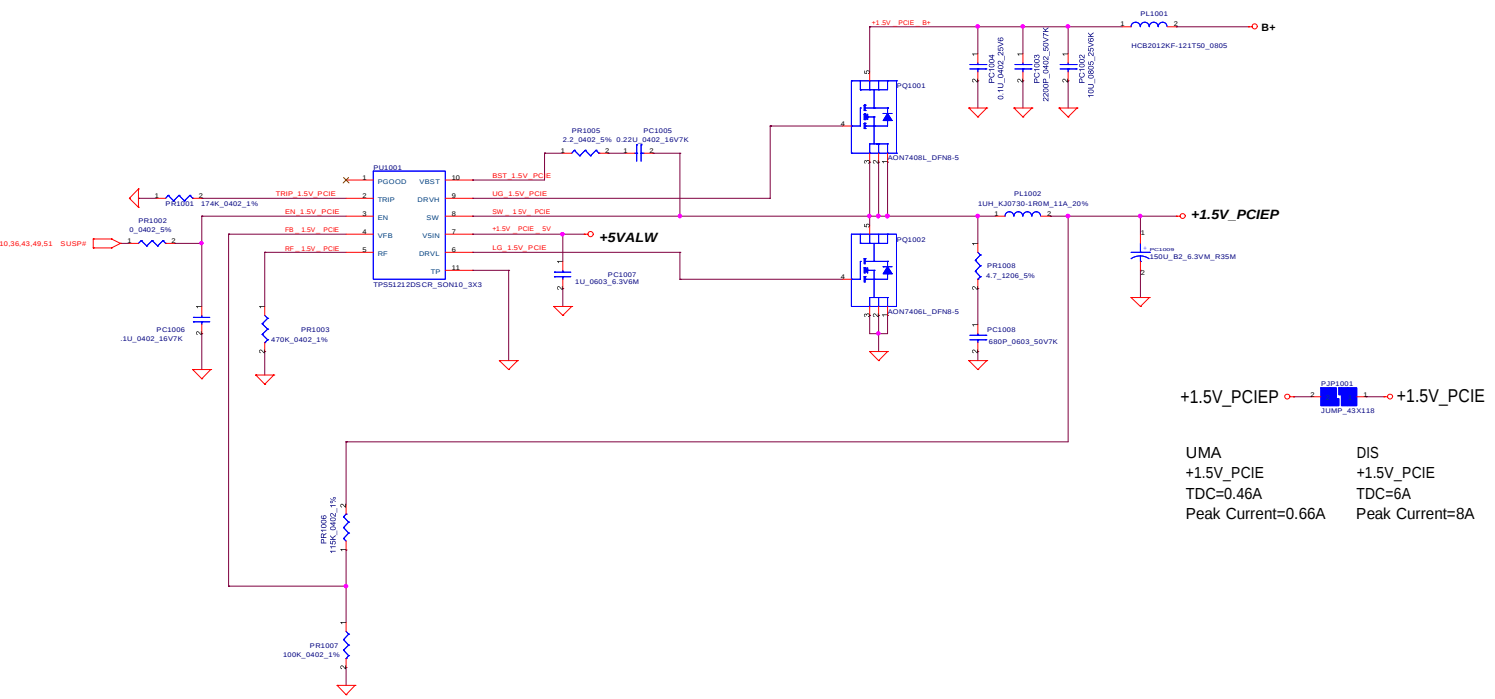


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Compal Electronics, Inc.

PWR- 1.8VS

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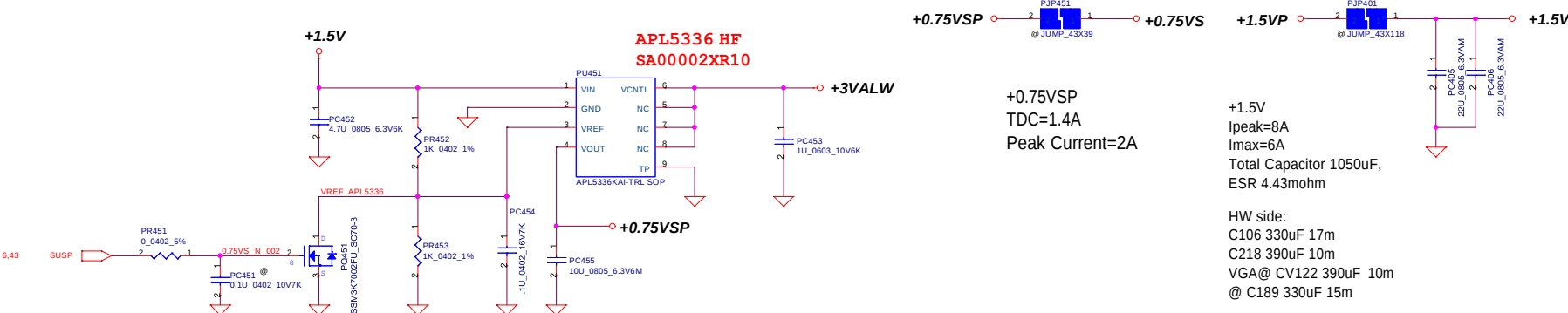
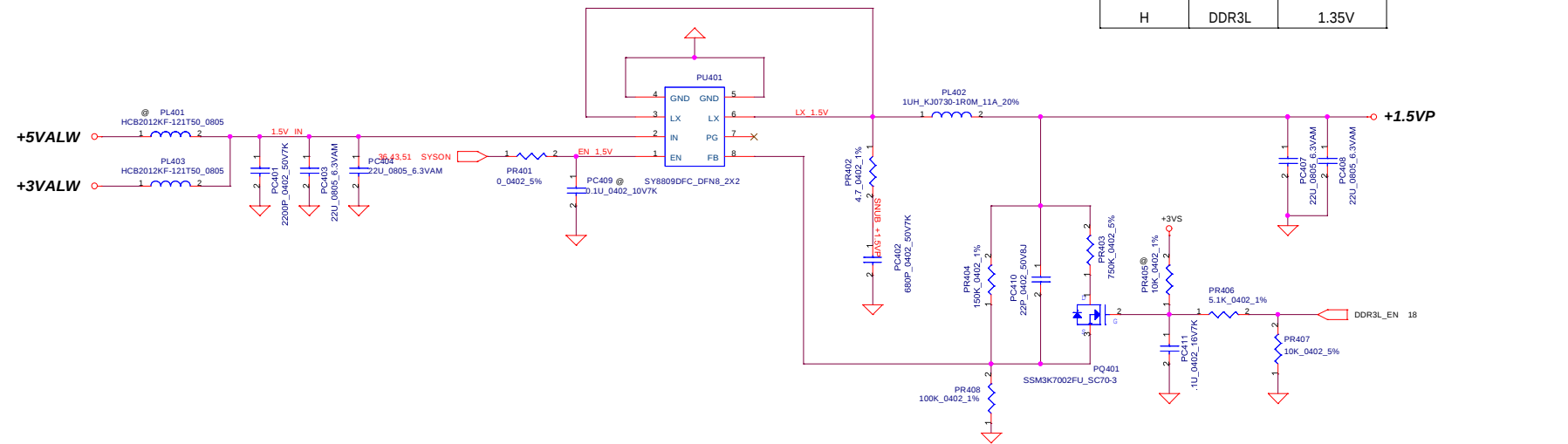
+1.5V_PCEP

UMA
+1.5V_PCE
TDC=0.46A
Peak Current=0.66A

DIS
+1.5V_PCE
TDC=6A
Peak Current=8A

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Sub C	Document Number					LA-8551P		Rev 0.1
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DDR3L_EN		1.5VP
L	DDR3	1.5V
H	DDR3L	1.35V



+0.75VSP

+0.75VS

+1.5VP

+1.5V

APL5336 HF
SA00002XR10

+3VALW

+0.75VSP

+0.75VSP

TDC=1.4A

Peak Current=2A

+1.5V

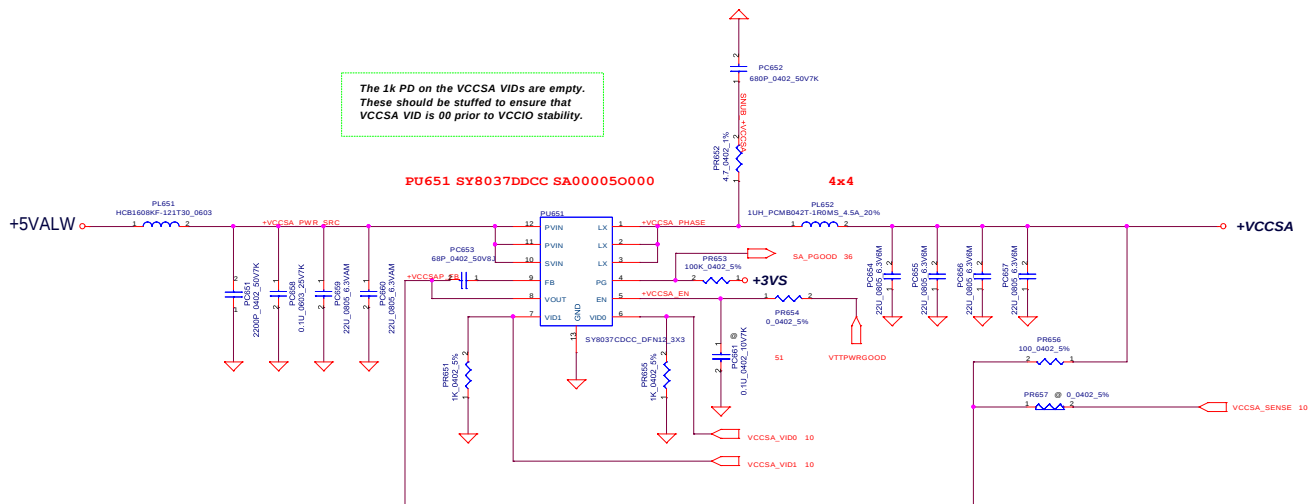
Ipeak=8A

I_{max}=6A

Total Capacitor 1050uF,
ESR 4.43mohm

HW side:
C106 330uF 17m
C218 390uF 10m
VGA@ CV122 390uF 10m
@ C189 330uF 15m

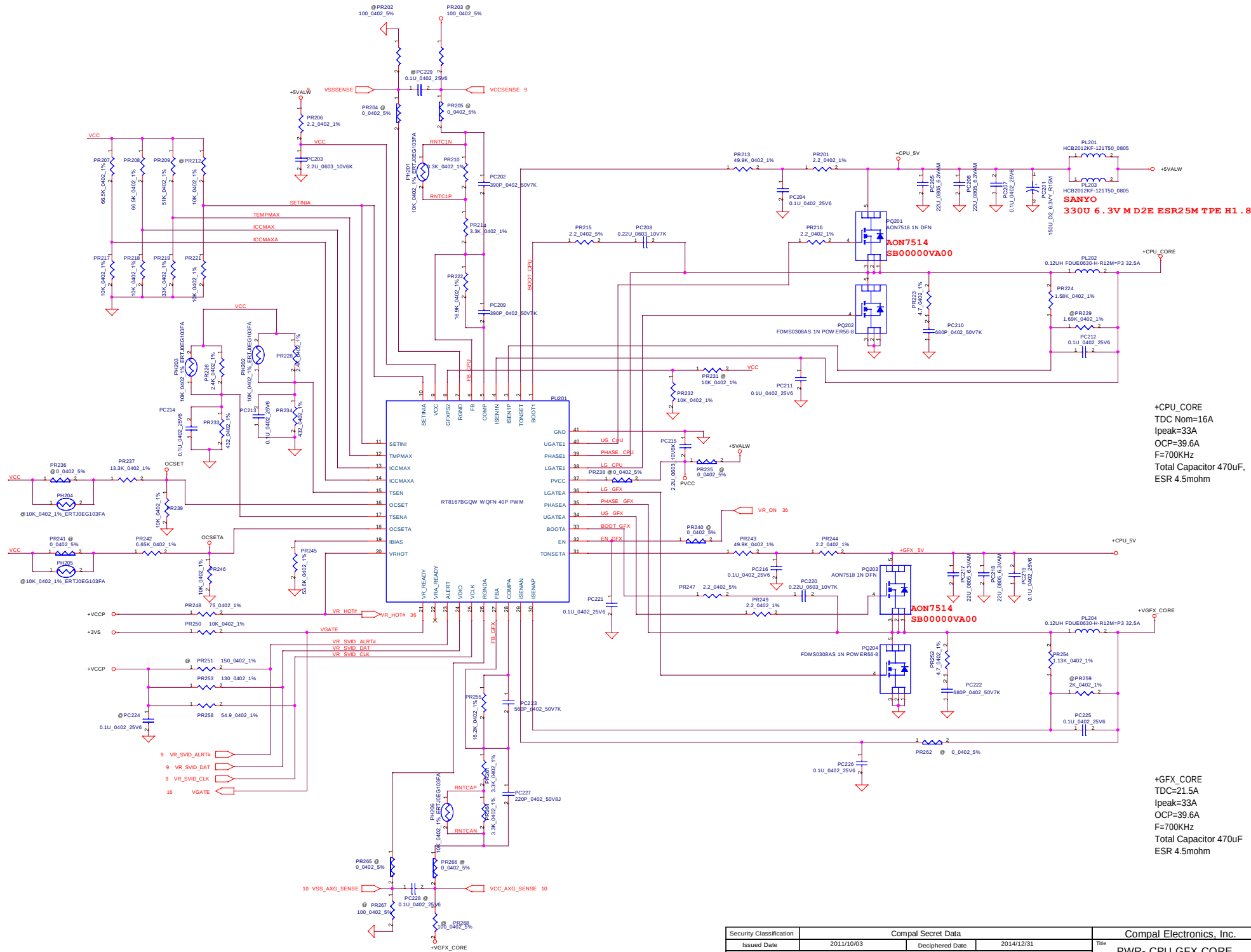
Security Classification	Compal Secret Data		Title	
Issued Date	2011/10/03	Deciphered Date	2014/12/31	
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				59



The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

+VCCSA
I_{tdc}=3A
I_{max}=4A

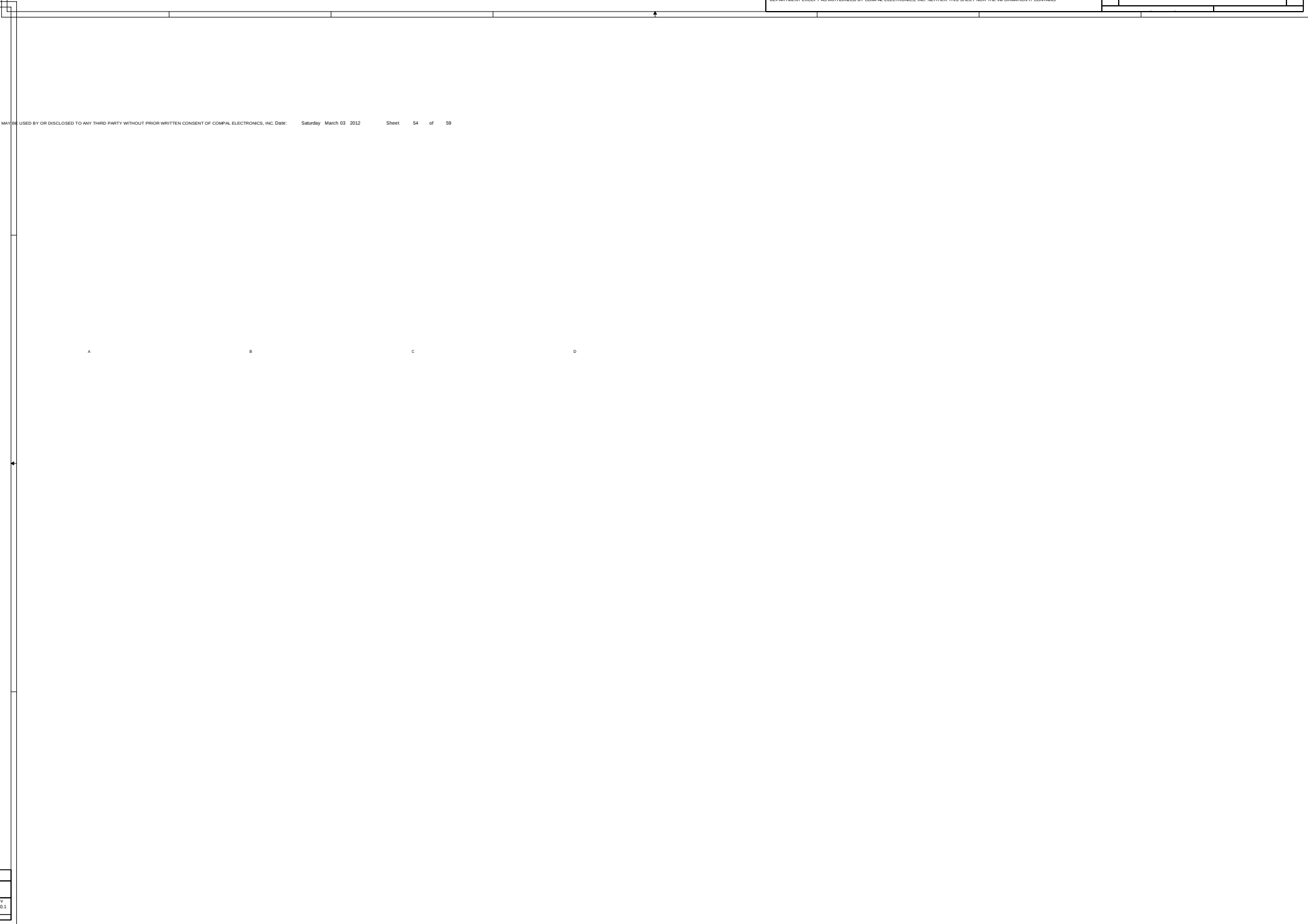
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+CPU_CORE
TDC Nom=16A
Ipeak=33A
OCP=39.6A
F=700KHz
Total Capacitor 470uF,
ESR 4.5mohm

+GFX_CORE
TDC=21.5A
Ipeak=33A
OCP=39.6A
F=700KHz
Total Capacitor 470uF
ESR 4.5mohm

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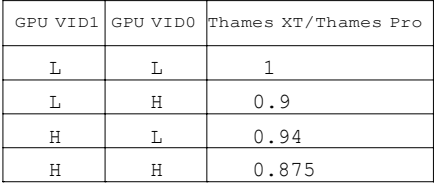


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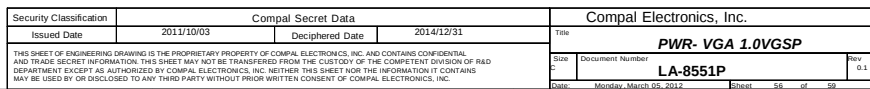
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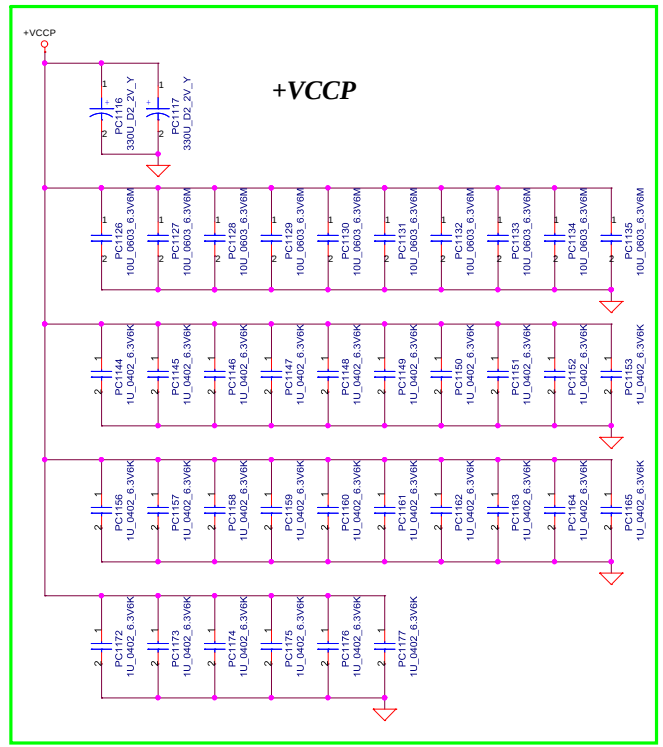
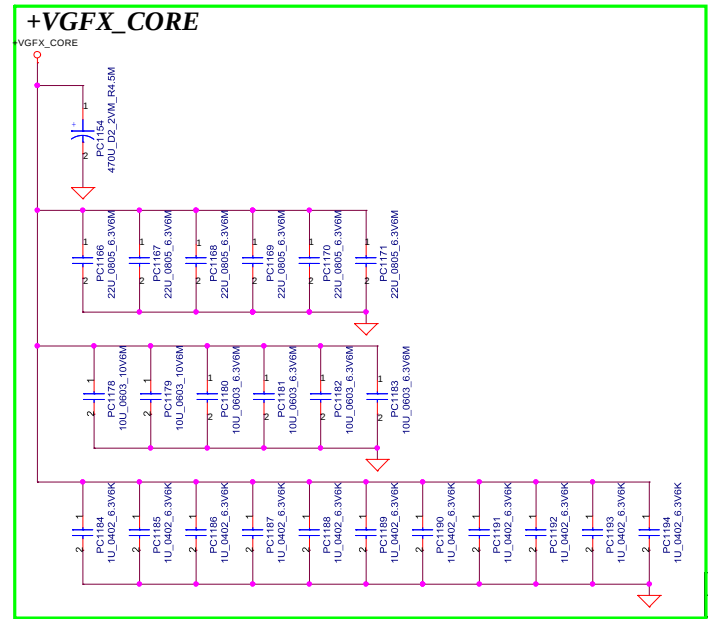
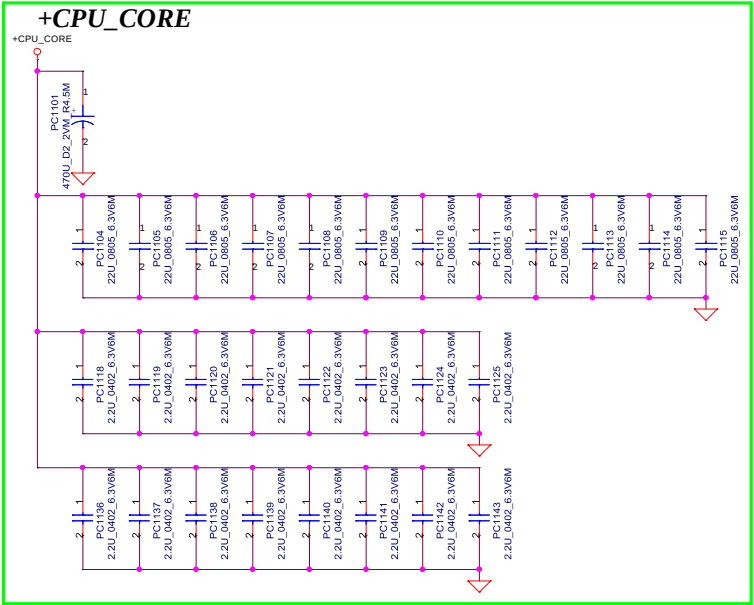
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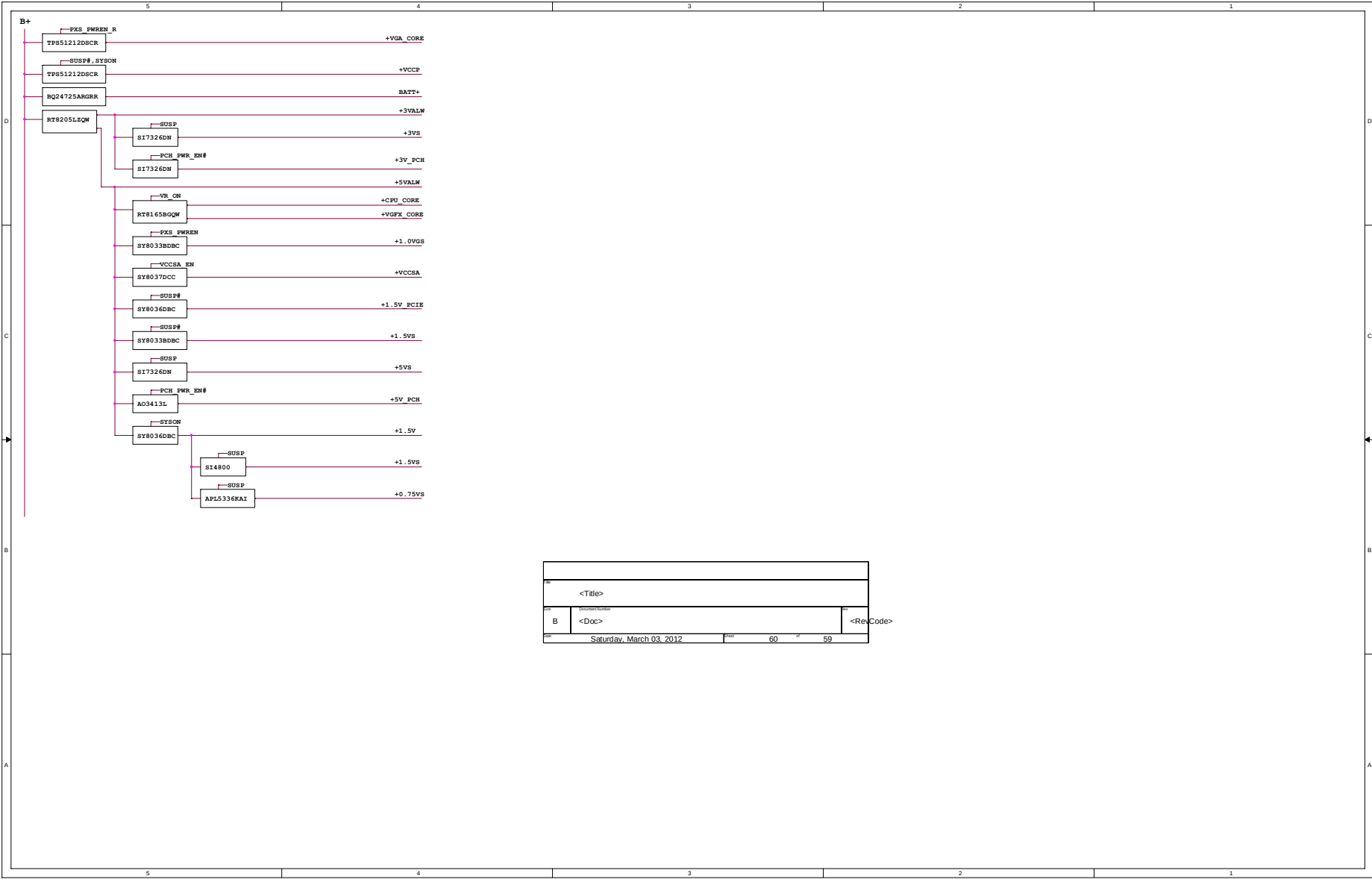


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2011/10/03		2014/12/31		Size	Rev
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1	47	change PC111 to 0402	2011/11/28		For layout space		
2	47	remove PR121	2011/11/28		0ohm, not needed		
3	47	change PR124 to 270K, PR126 to 42.2K	2011/11/28		change Vin detector setting		
4	47	change PC125 to 0.047uF	2011/11/28				
5	47	change PR125 to 0ohm, PC126 to 100pF	2011/11/28		FAE review recomment		
6	47	change PR119 to 365K	2011/11/28		modify charge I limit to 3.54A		
7	47	change PR111 to 0ohm	2011/11/28				
8	47	add PL101	2011/11/28				
9	46	delete PD5, PD6	2011/11/28		imbedded battery, ESD diode is not needed		
10	46	SMC, SMD exchange	2011/11/28				
11	46	delete pin8 and pin5, add battery temp sense at pin5.	2011/11/28		EC request to need one detect pin if SMB communication fail.		
12	47	change PQ302 to AON7518	2011/11/28				
13	50, 52	change PU1001, PU401 from SY8036HDBC to SY8036L	2011/11/28				
14	53	change PU651 from SY8037DCC to SY8037ADCC	2011/11/28				
15	52	add PQ401, PR406, PR407, PC411	2011/11/28				
16	56	change PR1055 to 28.7K	2011/11/28		for correct 1.0V voltage		
17	54	change PL202, PL204 to SH00000FP00, 0.12uH	2011/11/28				
18	54	change PU201 to RT8167, SA00005AU00	2011/11/28				
19	54	change PQ201, PQ203 to AON7518, SB00000U300	2011/11/28				
20	54	change PQ202, PQ204 to FDMS0308AS, SB00000U400	2011/11/28				
21	55	change PL802 to 0.36uH, SH00000HD00	2011/11/28				
22	52	change PU401 to SY8809DFC	2011/11/29				
23	45, 48	change PD2, PD301 DIO CD4148WN-1 1206	2011/11/29		For cost and layout space		
24	51	add PC511, PC512	2011/12/11				
25	54	change PL201 to 0805, and add PL203	2011/12/11				
26	48	add PR320	2011/12/11		tune frequency		
27	55	change PC813, PC814, PC815, PC816 tp 330uF 9m	2011/12/11				
28	47	change PQ101 to SB000009610	2011/12/11				
29	54	change PR210, PR214, PR261, PR264 to 3.3K; PR222 to 15.8K; PR255 to 10.5K; PC202, PC209 to 270p; PC223 to 220p; PC227 to 560p; PR224, PR254 to 1.82K; PR207 to 127K	2011/12/11		Fine tune CPU, GFX transient		
30	47, 54	change PR111, PR110, PR216, PR249 to 2.2 ohm	2011/12/12		For EMI solution		
31	53, 56	change PL602, PL1052 to SH00000MW00	2011/12/12		For crack issue		
32	55	change PL802 to SH00000HQ00	2011/12/12		For thermal solution		
33	48	change PL303 to SH00000ON00	2011/12/12		For thermal solution		
34	47	change PR114, PR115 to 0 ohm	2011/12/14		Prevent charger damaged by negative output voltage		
35	54	change PR207 to 66.5K	2011/12/14		For GFX GT2 current limit		
36	54	change PR237 to 23.7K +-1% 0402	2011/12/23				
37	54	change PR241 to 1/16W 0 +-5% 0402	2011/12/23				
38	54	change PR242 to 23.7K +-1% 0402	2011/12/23				
39	47	change PQ103, PQ104 to SB00000TZ00	2011/12/23				
40	47, 48	change PQ106, PQ303 to SB00000H700	2011/12/23				
41	54	change PR210, PR261, PR264 to 3.3K +-1% 0402	2011/12/23				
42	53	change PL651 to SY8037CDCC	2012/1/11		For latch mode		
43	57	change PC1180, PC1181, PC1182, PC1183 to SE000005T80	2012/1/11		For height limit		
44	46	Delete PC11	2012/1/12		For ME request		

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45	47	change PR114 to 10, PR115 to 6.8ohm, add PD103	2012/1/30		For Charger issue		
46	47	Add PC130, PC131, PC104, PC107	2012/1/30		For EMI solution		
47	48	Add PR321	2012/1/30		Choose working frequency to improve efficiency and thermal		
48	50	change 1.5VPCIE Circuit	2012/1/30		Change input voltage form 5V to 19V to slove thermal issue		
49	52	Add FL403	2012/1/30		Choose input voltage to slove thermal issue		
50	54	Change PR224 to 1.58Kohm, PC209 to 220PF, PC202 to 390PF, PR222 to 16.9Kohm, PR237 to 21.5K	2012/1/30		Base on SI layout, FAE review recommand value		
51	48	change PL303 to SH00000F600	2012/1/30		For thermal issue		
52	45	Delete PD2, PR2, PR3, PC6	2012/1/30		For Layout space		
53	47, 48, 54	Change PQ302, PQ201, PQ203 to AON7514	2012/1/30		For efficiency		
54	51	Delete PJP501	2012/1/30		For Layout space		
55	55	Change PC813, PC814, PC815 to 470uF, delete PC816 Change PL802 0.36uF to 13*13*3.5 size	2012/1/30		For thermal issue		
56	55	Add PC820, PC821, PC822	2012/1/30		For VGA transient voltage		
57	57	Change PC1180, PC1181, PC1182, PC1183 to SE000005780	2012/1/30		For ME request		
58	47	change PQ102 to TFCA8057	2012/1/30				
59	54	change PC223 to 560pF, PC227 to 220pF	2012/2/17		For FAE suggesstion		
60	48	change PQ302 to AON7518	2012/2/17		For efficiency		
61	55	change PL802 to 13*13*3 size	2012/2/17		For thermal solution		
62	47	change PR114, PR115 to 0 ohm, PD103 to SCS00005800	2012/2/17		For HP and soucer request		
63	54	change PC201 to 330uF	2012/2/17		For acoustic solution		
64	45	change LED circuit	2012/2/23				
65	48	change PL303 to 3.3uH 10*10*3H, PC313 to 150U_B2_6.3VM_R35M, remove 5V output jumper	2012/2/23		For thermal solution		
66	53	change PU651 to SY8037DDCC	2012/2/23		For ULV CPU and latch mode		
67	55	change PR812 and PR816 power to +3VGS	2012/2/23		For leakage issue		
68	45	change LED circuit	2012/2/29				
69	54	change PC209 to 390pF, PR237 to 13.3Kohm, PR254 to 1.13Kohm, PR255 to 16.2Kohm, PR242 to 6.65Kohm	2012/2/29		Base on PV layout		
70	45	change PL1, PL2 to 0603 size, add PL4	2012/2/29		EMI request		



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