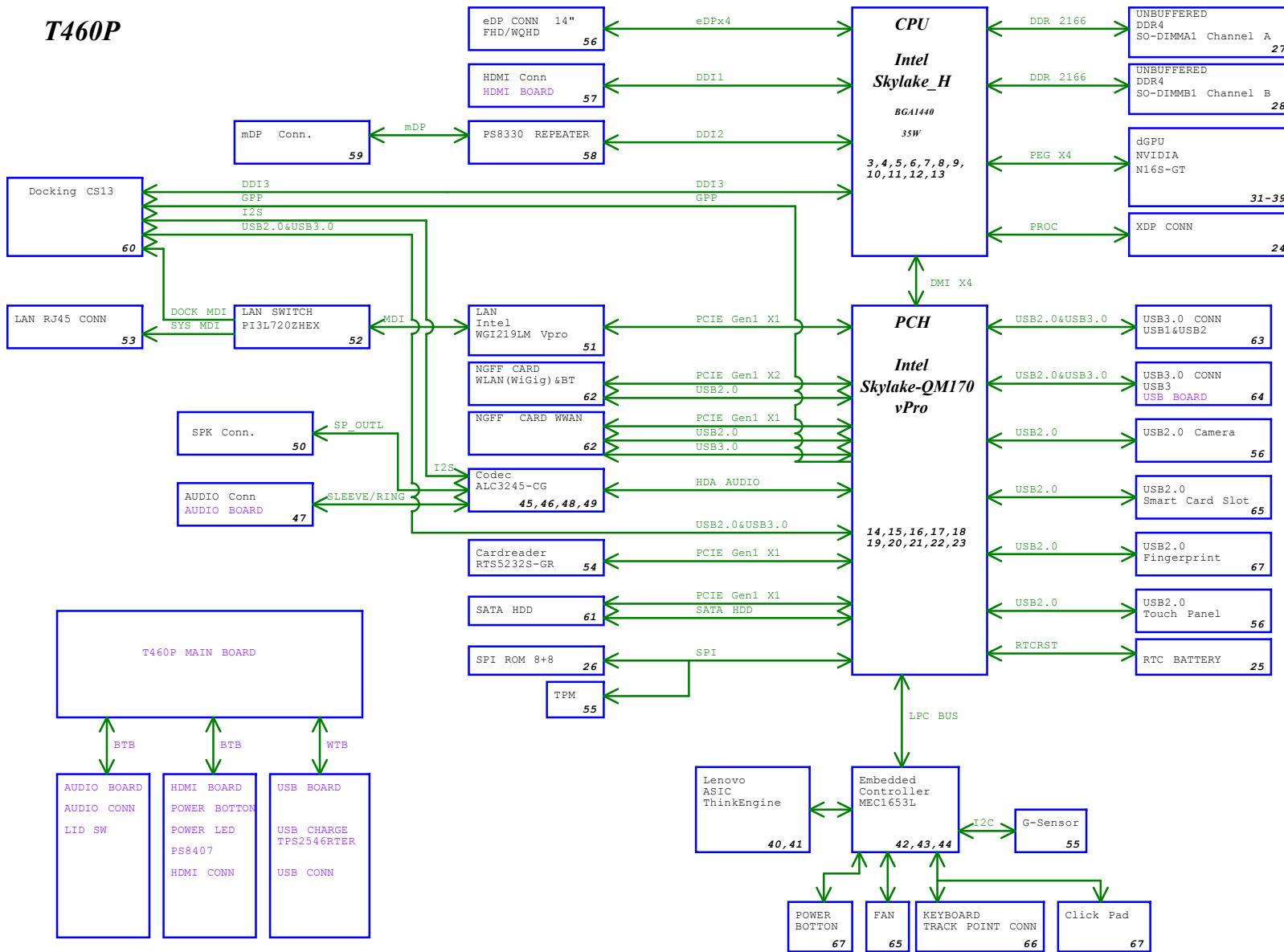


T460P



```

Page: 03~13==>CPU SKL-H
Page: 14~23==>PCH SKL-H
Page: 24=====>XDP CONNECTOR
Page: 25=====>RTC BATTERY
Page: 26=====>SPI FLASH
Page: 27~28==>DDR4 MEMORY
Page: 31~39==>N16S-GT
Page: 40~41==>THINK ENGINE
Page: 42~44==>MEC1653L
Page: 45~50==>AUDIO ALC3245-CG
Page: 51~53==>LAN WGI219LM
Page: 54=====>CARD READER RTS5232S-GR
Page: 55=====>THERMAL SENSOR/G SENSOR/TPM
Page: 56=====>eDP/CMOS/LOGO-LED CONN.
Page: 57=====>HDMI BTB CONN.
Page: 58=====>PS8330B REPEATER DP
Page: 59=====>MINI-DP CONN.
Page: 60=====>CS13 DOCKING CONN.
Page: 61=====>SATA HDD CONN.
Page: 62=====>WLAN/WWAN/SIM CONN.
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Page: 84=====>DC/DC IMVP8
Page: 85=====>DC/DC VCCPCORE
Page: 86=====>DC/DC VCCGFXCORE_I
Page: 87=====>DC/DC VCCSA
Page: 88=====>CPU PROCESSOR DECOUPLING
Page: 89=====>DC/DC VCCCPU10
Page: 90=====>DC/DC VCC1R0 SUS
Page: 91=====>DC/DC VCC1R2A/VCC0R6B
Page: 92=====>DC/DC VCC2R5A
Page: 93=====>DC/DC GFXCORE_D
Page: 94=====>DC/DC VCC1R5VIDEO
Page: 95=====>DC/DC VCC1R05VIDEO_PLL

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Security Classification	LC Future Center Secret Data			Title	
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TABLE: SYSTEM POWER STATE

Gx State (System State)	Sx State (System State)	Mx State (System State)	SW Power	M Power	SUS Power	AMT Power	A Power	B Power	User Observation	Chipset
G0	S0	M0	ON	ON	ON	ON	ON	ON	System Operating	Full On
G1	S3	M3	ON	ON	ON	ON	ON	OFF	Standby	Suspend-to-RAM (STR)
		M-OFF	ON	ON	ON	OFF	ON	OFF	Standby with USB wake enabled	
	Deep S3	M-OFF	ON	ON	OFF	OFF	ON	OFF	Standby	Suspend-to-Disk (STD)
	S4	M3	ON	ON	ON	ON	OFF	OFF	Hibernation with RTC wakeup	
G2	Deep S4	M-OFF	ON	ON	OFF	OFF	ON	OFF	Hibernation or Shutdown	Soft Off
	S5	M3	ON	ON	ON	ON	OFF	OFF		
	Deep S5	M-OFF	ON	ON	OFF	OFF	ON	OFF		
G3	S5 EC OFF	M-OFF	ON	OFF	OFF	OFF	OFF	OFF	No Power	Mechanical Off
	---	---	OFF	OFF	OFF	OFF	OFF	OFF		

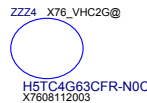
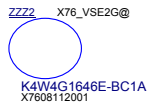
Schematics Mark Definition

Capacitor Naming Note

Ceramic Capacitors:

0.1U_0402_6.3VXX

Tolerance
Temperature Characteristics
Rated Voltage
Package Size



Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7	8	9	A
Code	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R	NPO	COG	X6S

B	C	D	E	F	G	H	I	J	K	L
BJ	CH	CJ	CK	SH	SJ	UJ	UK	SL	X5S	NOJ

Tolerance:

Symbol	A	B	C	D	F	G	H	J	K	M	N
Tolerance	+0.05PF	+0.1PF	+0.25PF	+0.5PF	+1%	+2%	+3%	+5%	+10%	+20%	+30%

Symbol	P	Q	V	X	Z	S	Y
Tolerance	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	+50,-20%	-30% ~ 10%

EC SMBus0 address

Device	Address
Smart Battery	0001 011X b

EC SMBus1 address

Device	Address
G-Senor (LIS3DH)	0011 000Xb
G-Senor (KX023)	0011 110Xb

EC SMBus2 address

Device	Address
Charge Controller	0001 0010

EC SMBus10 address

Device	Address
Master VGA	0x9E

PCH SM Bus address

Device	Address
CH-A DDR DIMM1	1001 0000b
CH-B DDR DIMM2	1001 0010b

PCH SM Bus0 address

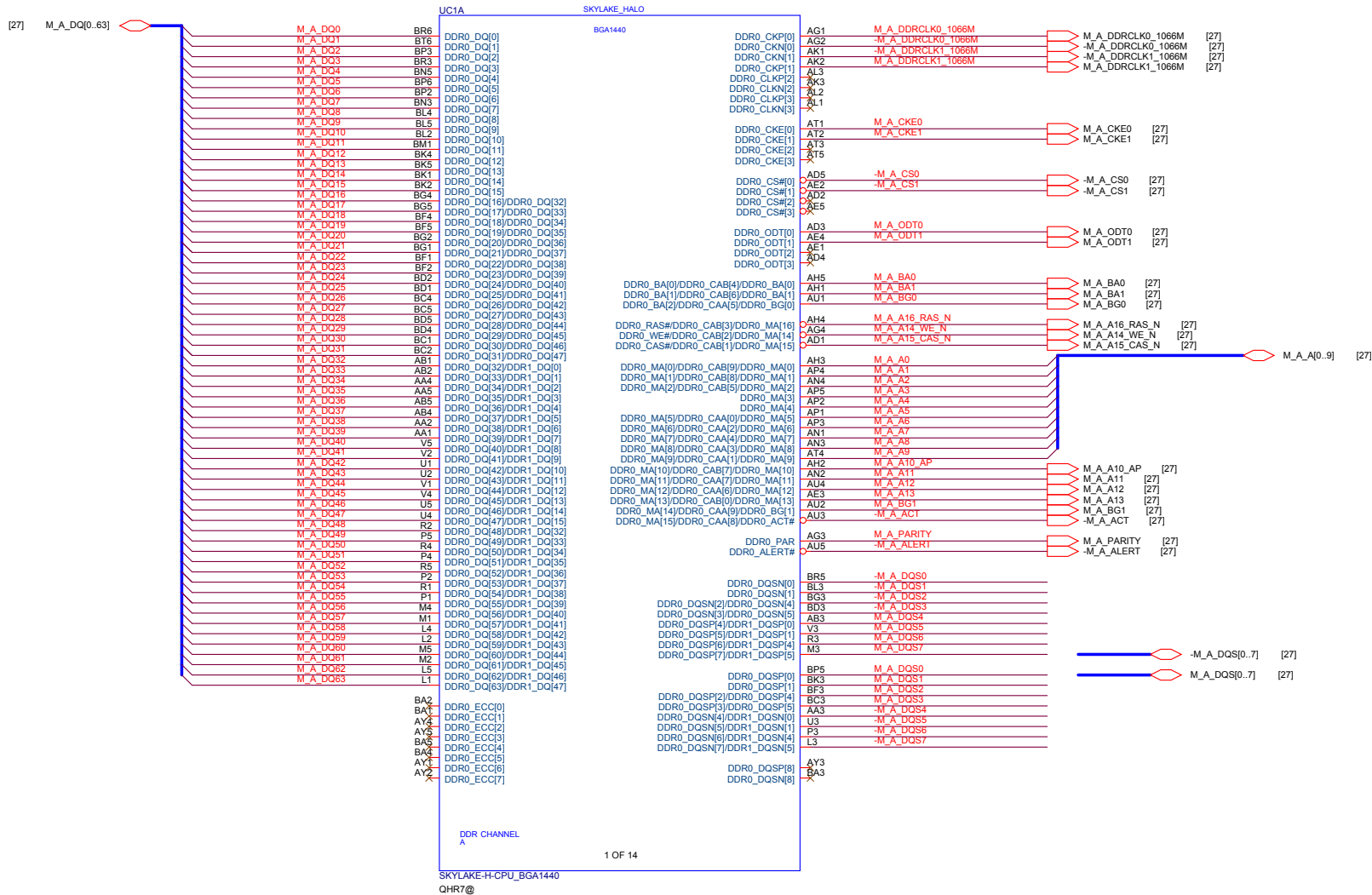
Device	Address
Intel Lan_I219	0XC8

BOM Structure Table

BOM Structure	NOTE
DEBUG@	For EE DEBUG
DPRE@	DP re-driver function
NODPRE@	Disable DP re-driver
GC6@	For GC6 function
NGC6@	NON GC6 function
ME@	ME Connector
EMC@	For EMI Solution
RF@	For RF Solution
VSE2G@	For SAMSUNG VRAM Setting
VME2G@	For Micron VRAM Setting
VHC2G@	For RF HYNIX VRAM Setting
X76_VSE2G@	K4W4G1646E-BC1A x4 + 24.9K
X76_VME2G@	MT41J256M16HA-093G x4 +10k
X76_VHC2G@	H5TC4G63CFR-N0C x4 +30.1k
CS@	For CURRENT SENSE
UMA@	For UMA
DIS@	For DIS
UC1@	For CPU

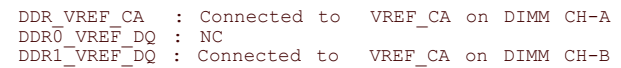
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DDR4 INTERLEAVE IMPLEMENTATION

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				Tuesday, November 03, 2015 Sheet 3 of 99	



[31] PEG_RXP[3:0] 
[31] PEG_RXN[3:0] 

 PEG_TXP[3:0] [31]
 PEG_TXN[3:0] [31]

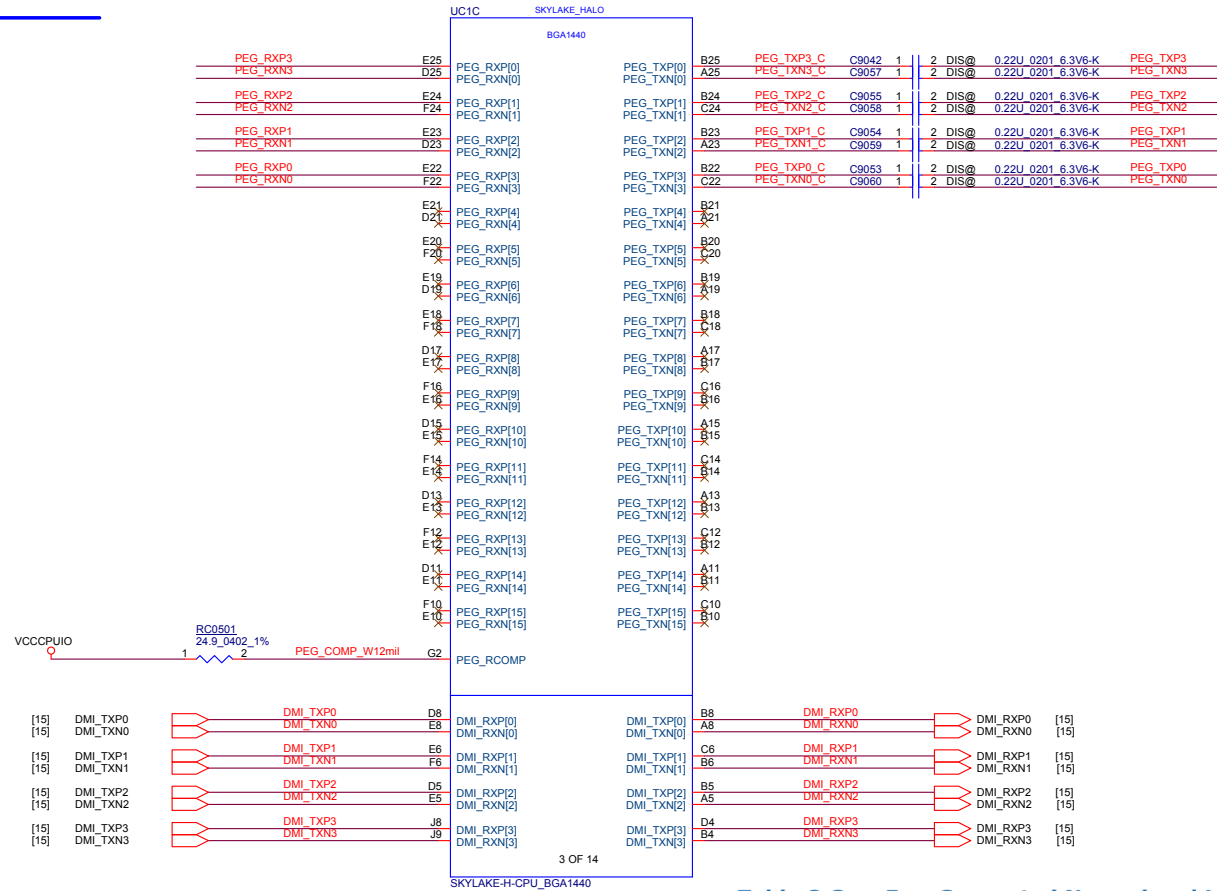
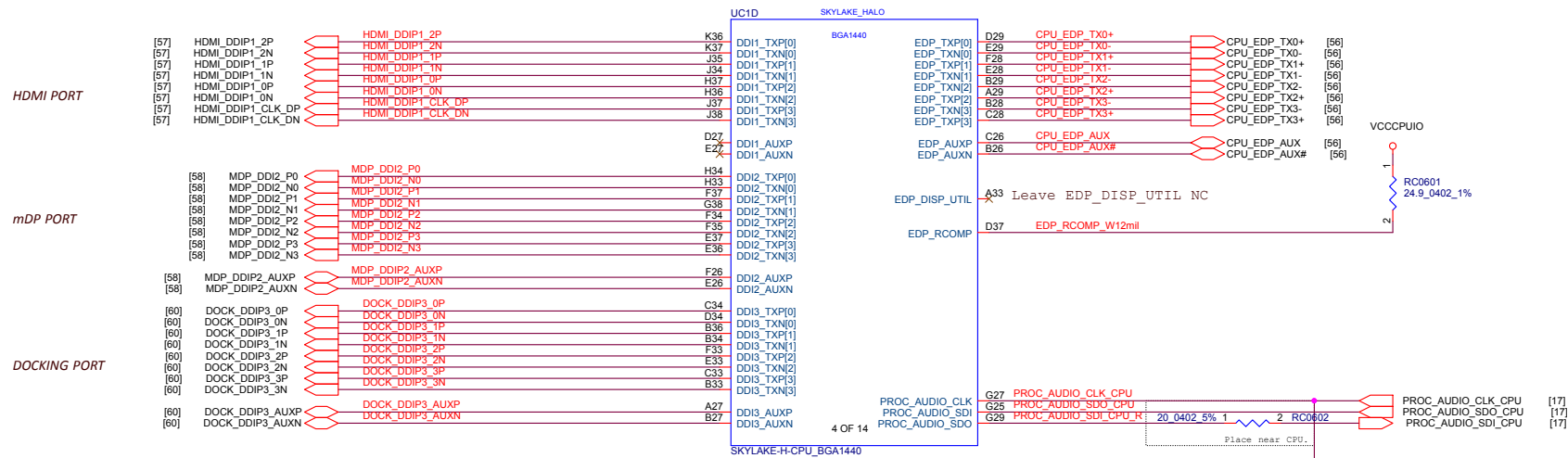
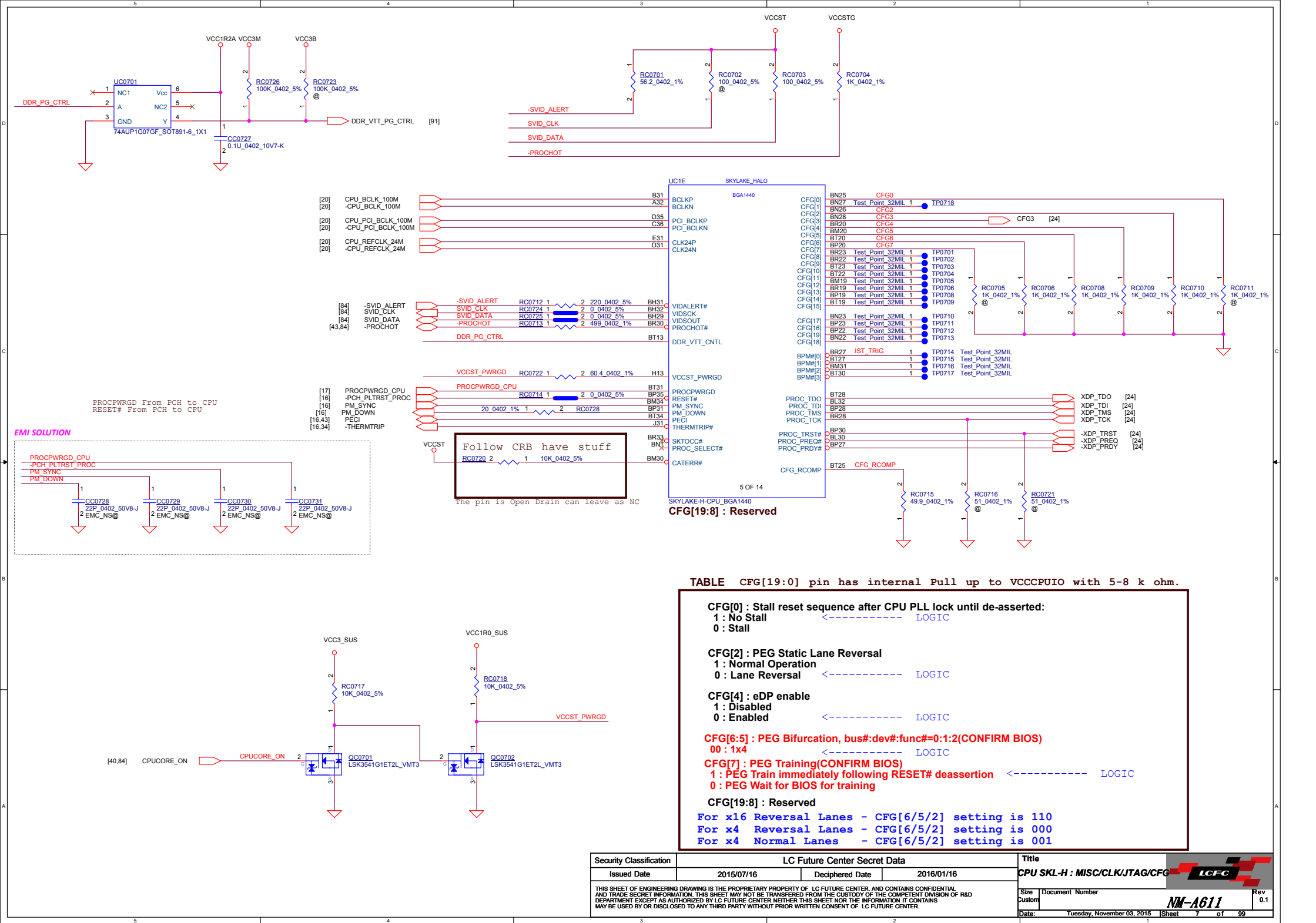
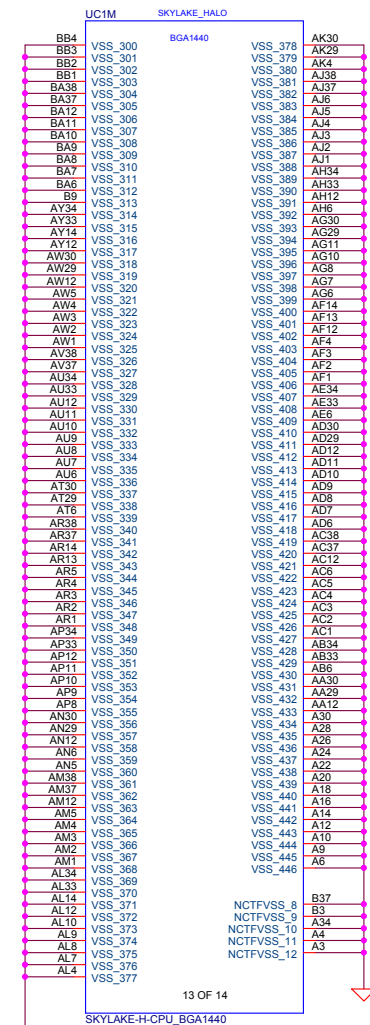
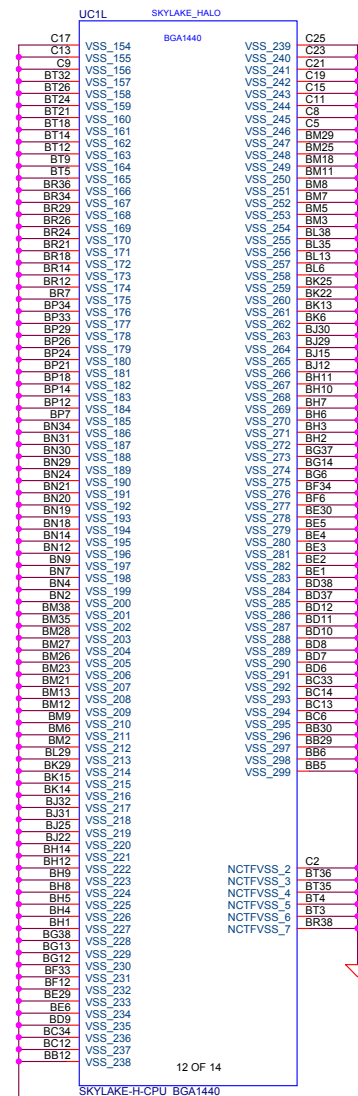
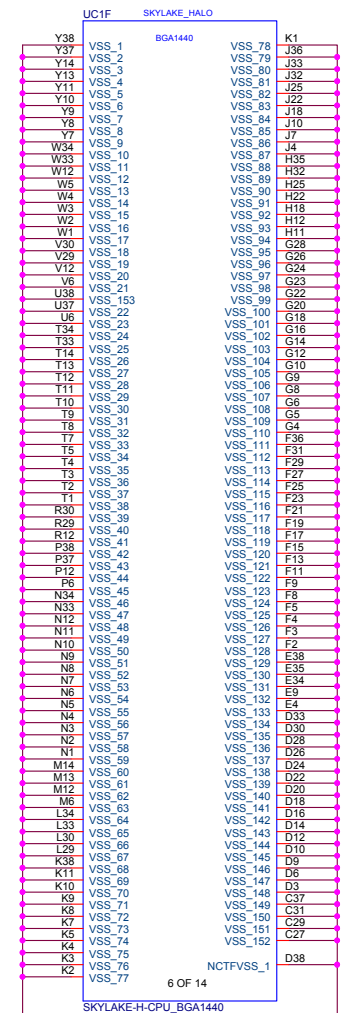


Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

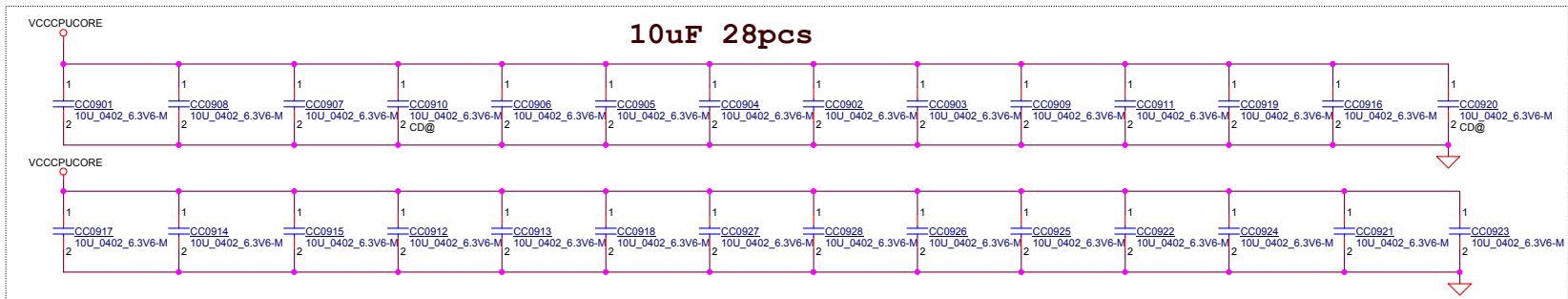
x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Pro- cessor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0
Notes: 1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported. 2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows: — Connect lane 0 of 1st device to lane 0. — Connect lane 0 of 2nd device to lane 8. — Connect lane 0 of 3rd device to lane 12. For example: a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7. b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9. c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane12.																			



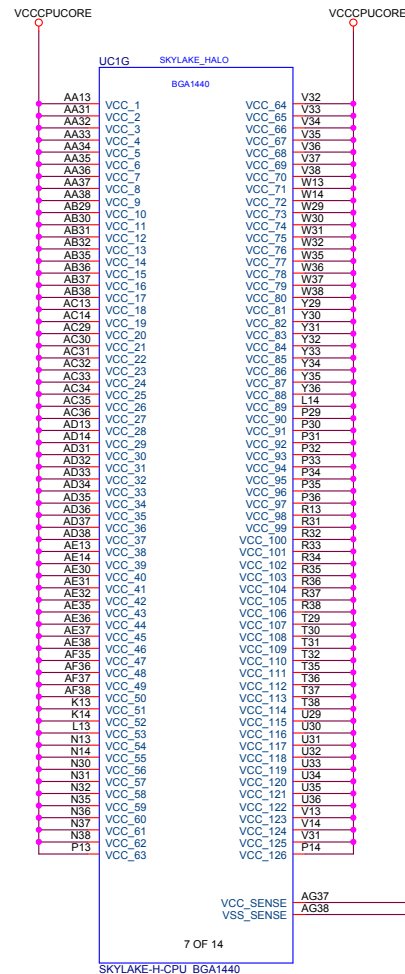
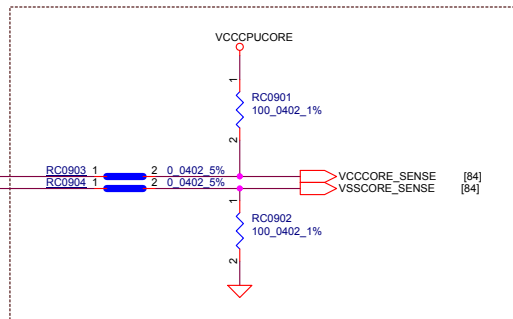




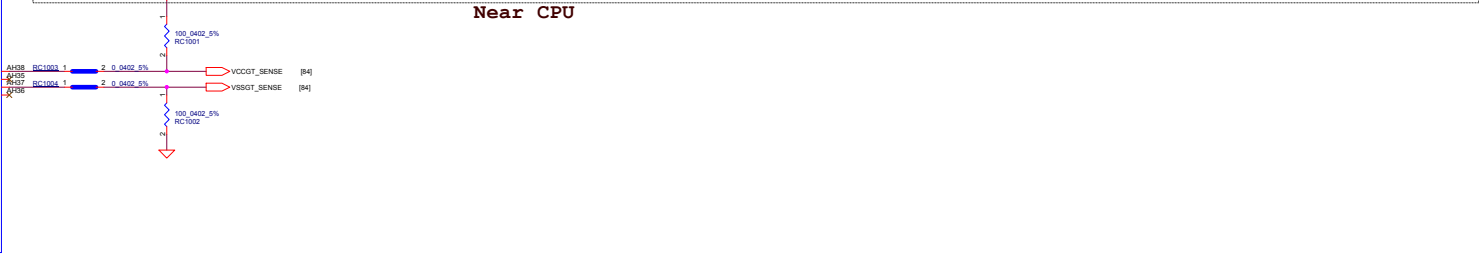
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NEAR PROCESSOR PINS

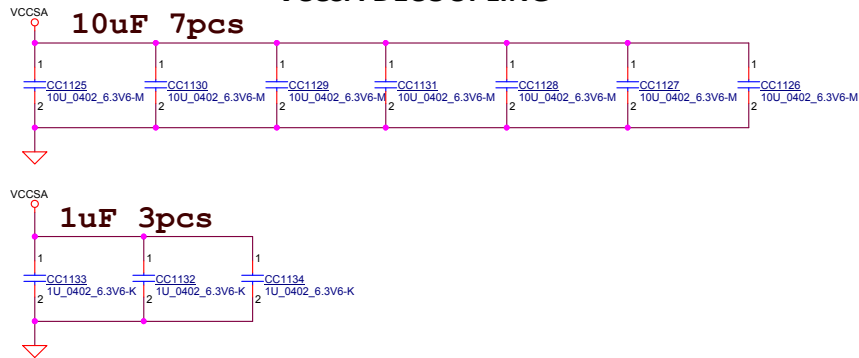


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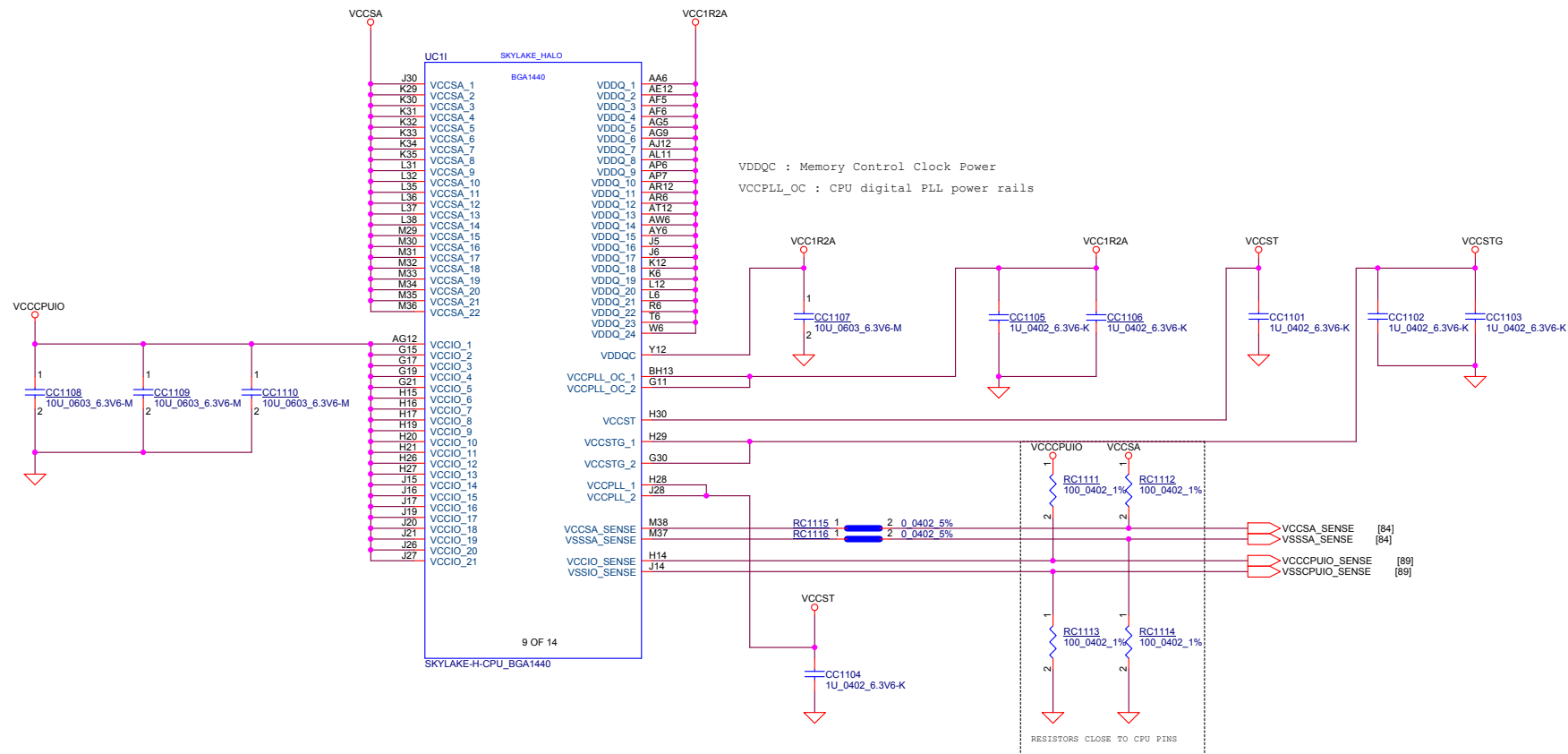
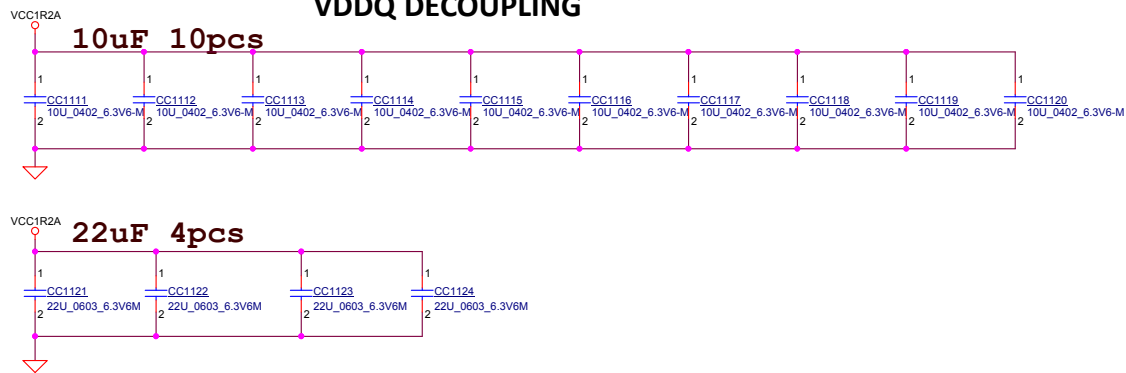


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VCCSA DECOUPLING



VDDQ DECOUPLING

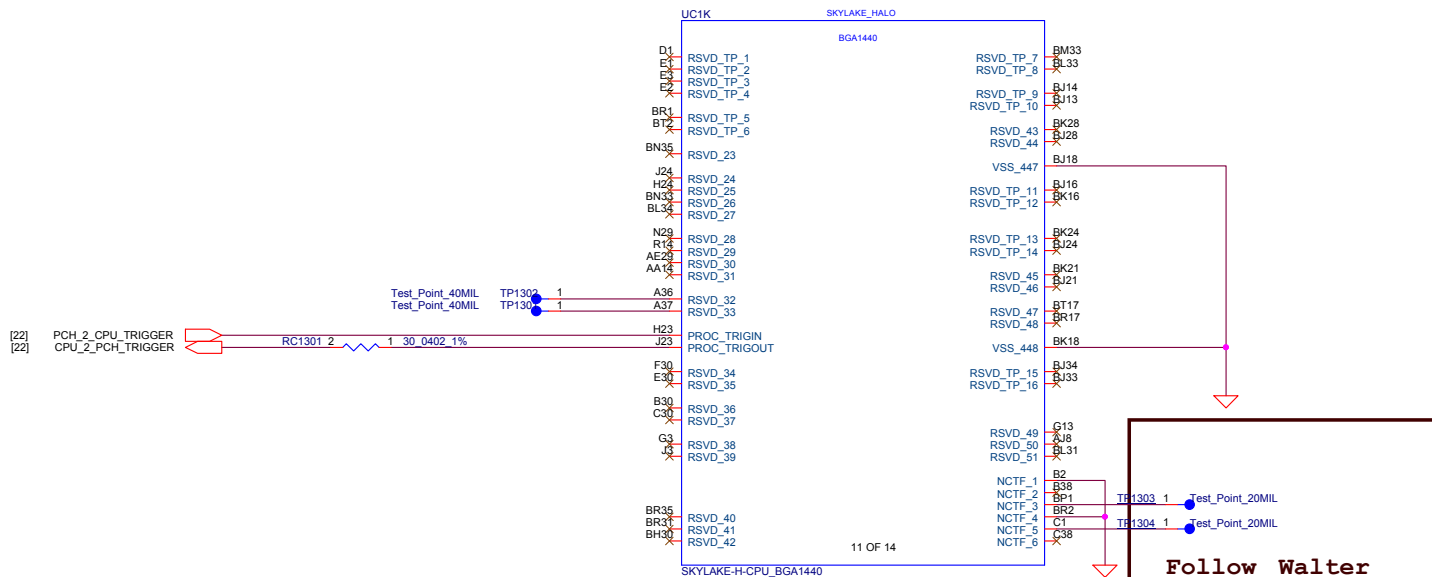


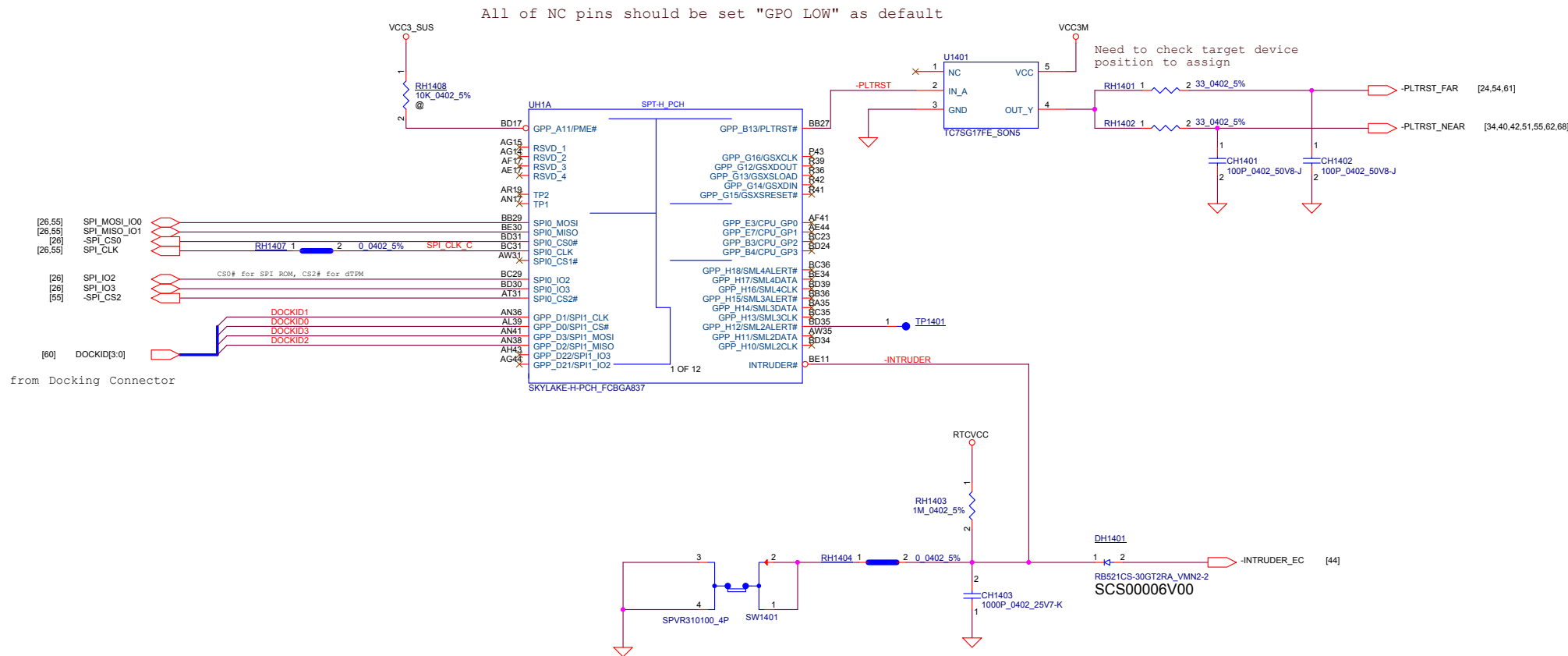
OPC_RCOM Support 4+4e
If not use can't conector

UC1J		SKYLAKE_HALO
		BGA1440
BJ17	VCCOPC_1	
BJ19	VCCOPC_2	
BJ20	VCCOPC_3	
BK17	VCCOPC_4	
BK19	VCCOPC_5	
BK20	VCCOPC_6	
BL18	VCCOPC_7	
BL19	VCCOPC_8	
BL20	VCCOPC_9	
BL21	VCCOPC_10	
BL22	VCCOPC_11	
BM17	VCCOPC_12	
BN17	VCCOPC_13	
	VCCOPC_14	
BJ23	RSVD_1	
BJ26	RSVD_2	
BJ27	RSVD_3	
BK23	RSVD_4	
BK26	RSVD_5	
BK27	RSVD_6	
BL23	RSVD_7	
BL24	RSVD_8	
BL25	RSVD_9	
BL26	RSVD_10	
BL27	RSVD_11	
BM23	RSVD_12	
	RSVD_13	
BL15	VCCOPC_SENSE	
BM16	VSSOPC_SENSE	
BL22	RSVD_14	
BM22	RSVD_15	
BP15	VCCEOPIO_1	
BR15	VCCEOPIO_2	
BT15	VCCEOPIO_3	
BP16	RSVD_16	
BR16	RSVD_17	
BT16	RSVD_18	
BN15	VCCEOPIO_SENSE	
BM15	VSSEOPIO_SENSE	
BP17	RSVD_19	
BN16	RSVD_20	
BM14	VCC_OPC_1P8_1	
BL14	VCC_OPC_1P8_2	
BJ35	RSVD_21	
BJ36	RSVD_22	
AT13	ZVM#	
AW13	MSM#	
AU13	ZVM2#	
AY13	MSM2#	
BT29	OPC_RCOMP	
BR29	OPCE_RCOMP	
BP29	OPCE_RCOMP2	

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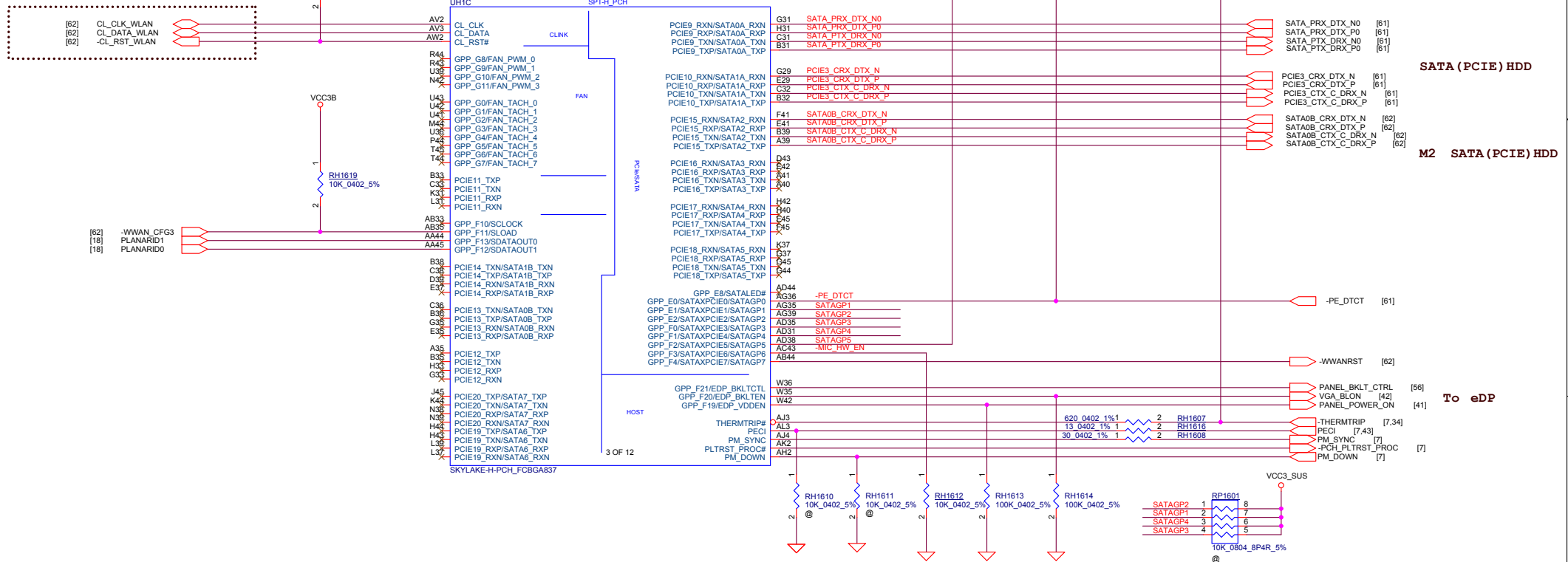
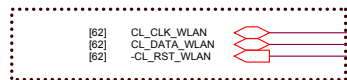
SKYLAKE-H-CPU_BGA1440





Flexible I/O	Port#	Configuration	Port Assignment
PCIe #20	26		
PCIe #19	25		
PCIe #18	24		
PCIe #17	23		
PCIe #16	22	SATA #3	M.2 Type B connector
PCIe #15	21	SATA #2	M.2 Type B connector
PCIe #14	20		
PCIe #13	19		
PCIe #12	18		
PCIe #11	17		
PCIe #10	16	PCIe #10	SATA-Express connector
PCIe #9	15	SATA #0/PCIe #9	SATA-Express connector
PCIe #8	14		
PCIe #7	13		
PCIe #6	12		
PCIe #5	11	PCIe #5	Cardreader
USB3 #10	10	PCIe #4	GbE PHY
USB3 #9	9		
USB3 #8	8		
USB3 #7	7	PCIe #1	WLAN
USB3 #6	6		
USB3 #5	5	USB3 #5	
USB3 #4	4	USB3 #4	Docking USB3.0 port
USB3 #3	3	USB3 #3	USB AOU port
USB3 #2	2	USB3 #2	USB Port 2
USB3 #1	1	USB3 #1	USB Port 1

from / to WLAN



Notes:

- The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
- SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
 - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
 - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs

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TABLE : Functional Strap

HDA_SDO	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

HDA_SDO is used to update the Descriptor and/or the ME Regions of the SPI after MFG Done bit is set.

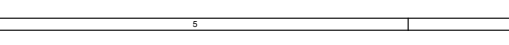
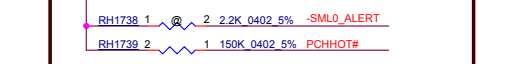
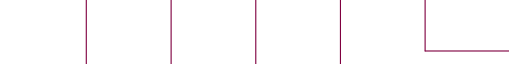
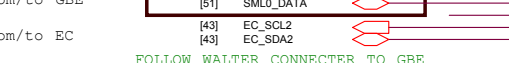
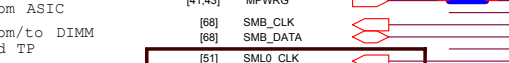
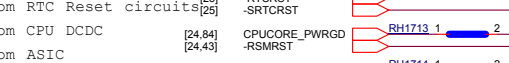
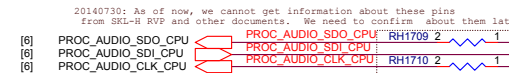
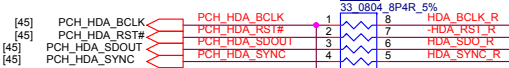
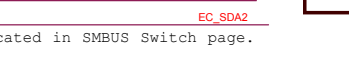
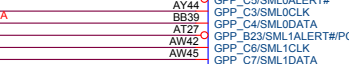
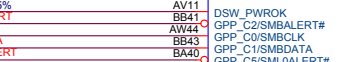
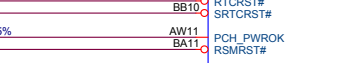
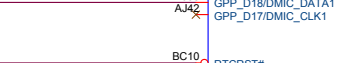
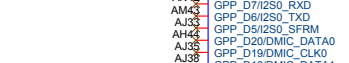
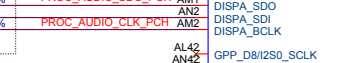
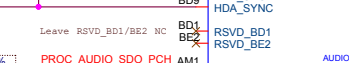
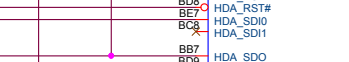
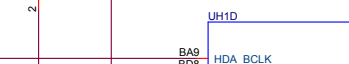
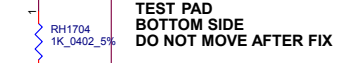
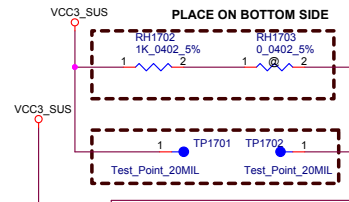


TABLE : Functional Strap

GPP_C5/SML0ALERT#(LPC or SPI)	
HIGH	eSPI is selected
LOW	LPC is selected(Default)

TABLE : Functional Strap

GPP_C5/SML0ALERT#(TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS(Default)



important

LPC is selected for EC. (Default)
This PD is insurance in case internal PD doesn't work well.

TABLE : Functional Strap

GPP_B14/SPKR(Top Swap Override)	
HIGH	Enable "TOP Swap" Mode
LOW	Disable "TOP Swap" Mode (Default by Internal PD)

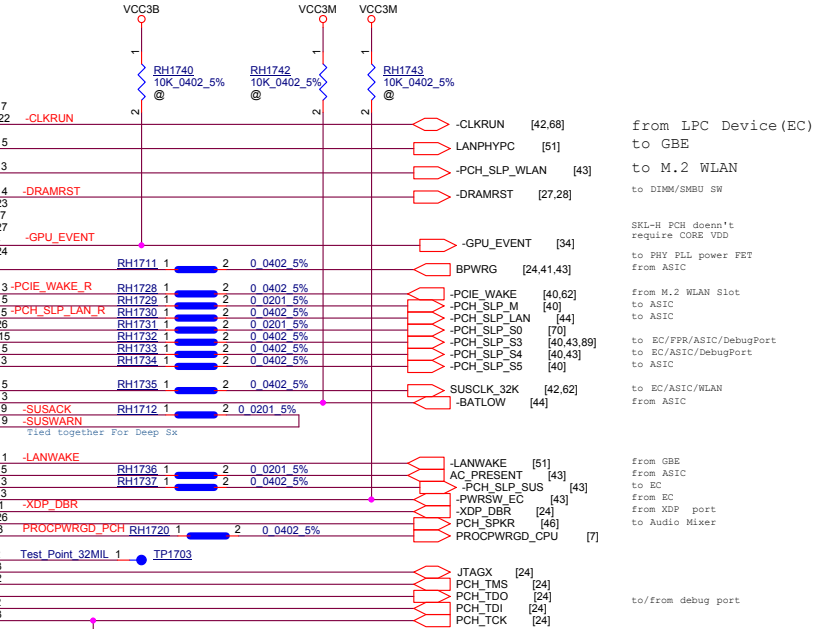
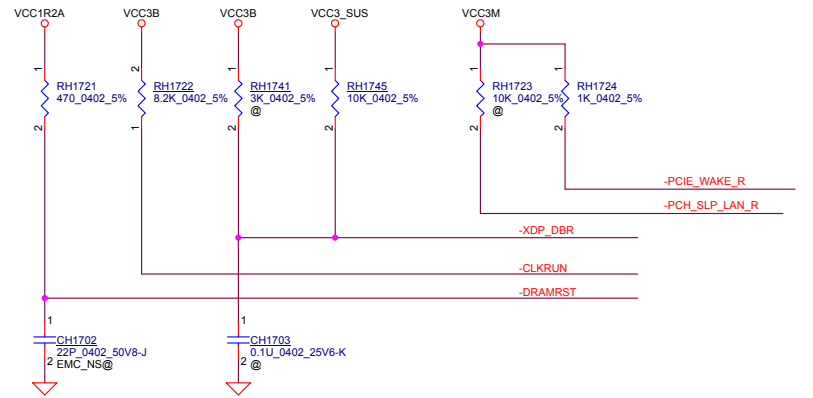


TABLE : Functional Strap

GPP_B14/SPKR(Top Swap Override)	
HIGH	Enable "TOP Swap" Mode
LOW	Disable "TOP Swap" Mode (Default by Internal PD)



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Title	
PCH SKL-H : AUDIO/SMBUS/JTAG	
Size	Document Number
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to be confirm on SDV

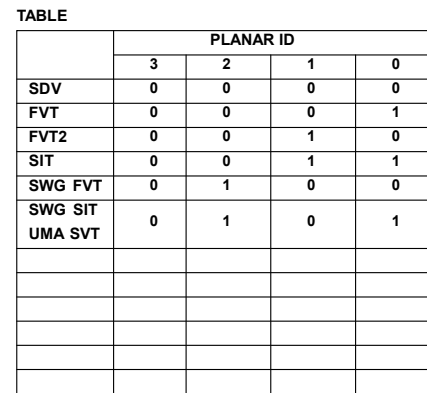
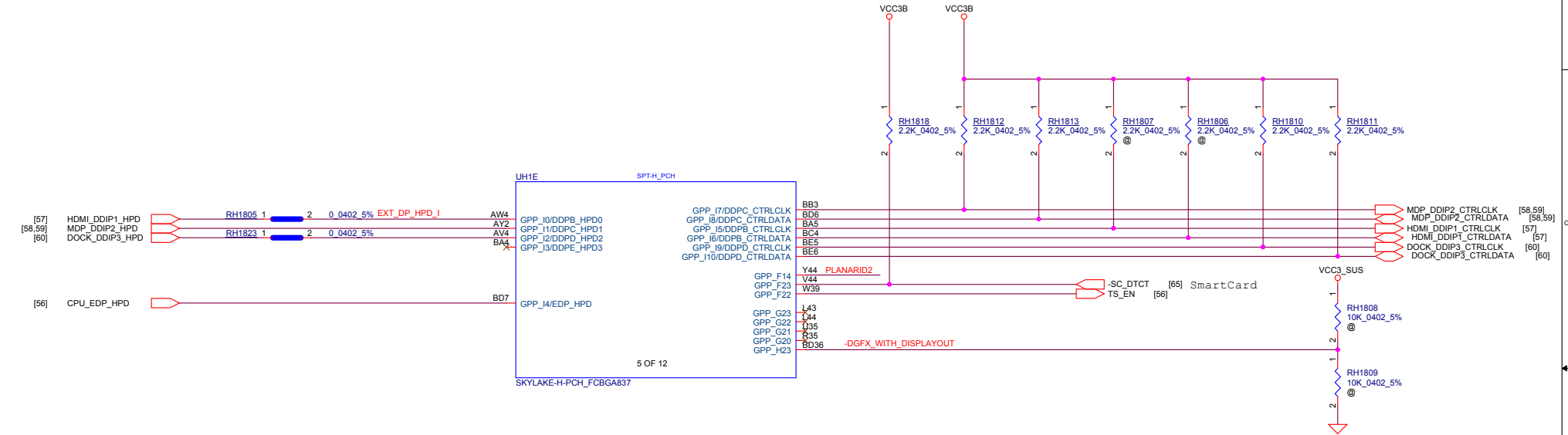
RH1816 1 2 100K_0402_5% HDMI_DDIP1_HPD

RH1814 NODPRE@1 2 100K_0402_5% MDP_DDIP2_HPD

RH1817 1 2 100K_0402_5% DOCK_DDIP3_HPD

RH1815 1 2 100K_0402_5% CPU_EDP_HPD

DDIP2_HPD : PS8330 has Int.PD 150K



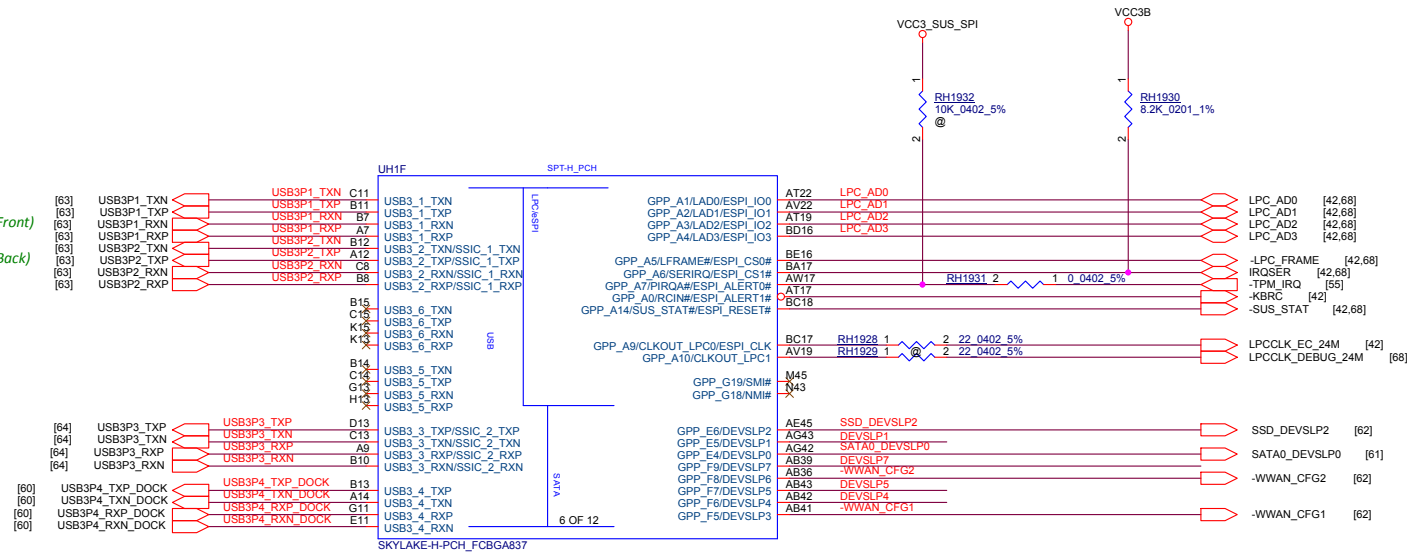
	PLANAR ID			
	3	2	1	0
SDV	0	0	0	0
FVT	0	0	0	1
FVT2	0	0	1	0
SIT	0	0	1	1
SWG FVT	0	1	0	0
SWG SIT				
UMA SVT	0	1	0	1

System Port 1 (Right-Front)

System Port 2 (Right-Back)

Small Board

DOCKING



[7] CPU_REFCLK_24M
[7] -CPU_REFCLK_24M
[7] CPU_BCLK_100M
[7] -CPU_BCLK_100M

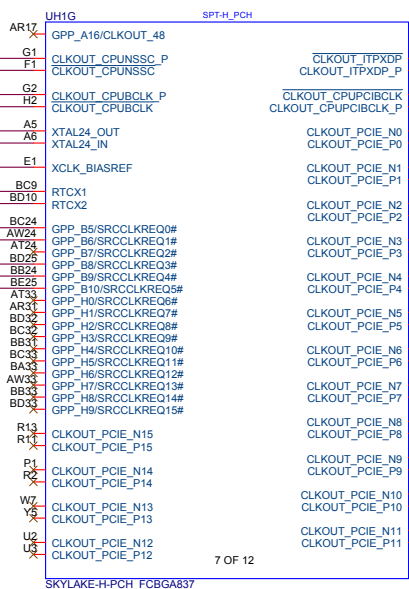
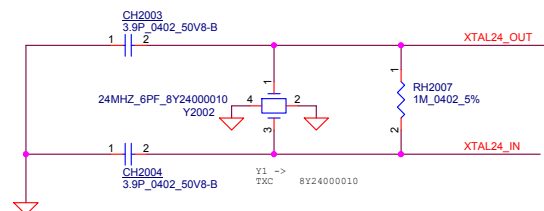
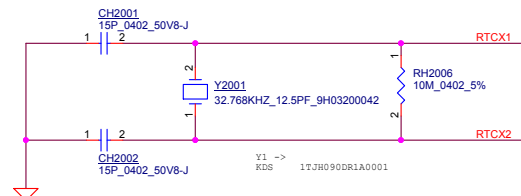
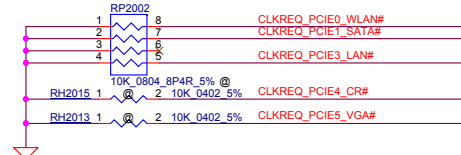
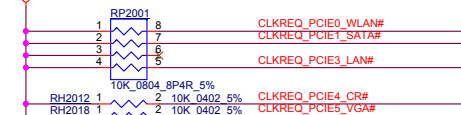
VCC1R0_SUS

RH2005

[62] CLKREQ_PCIE0_WLAN#
[61] CLKREQ_PCIE1_SATA#

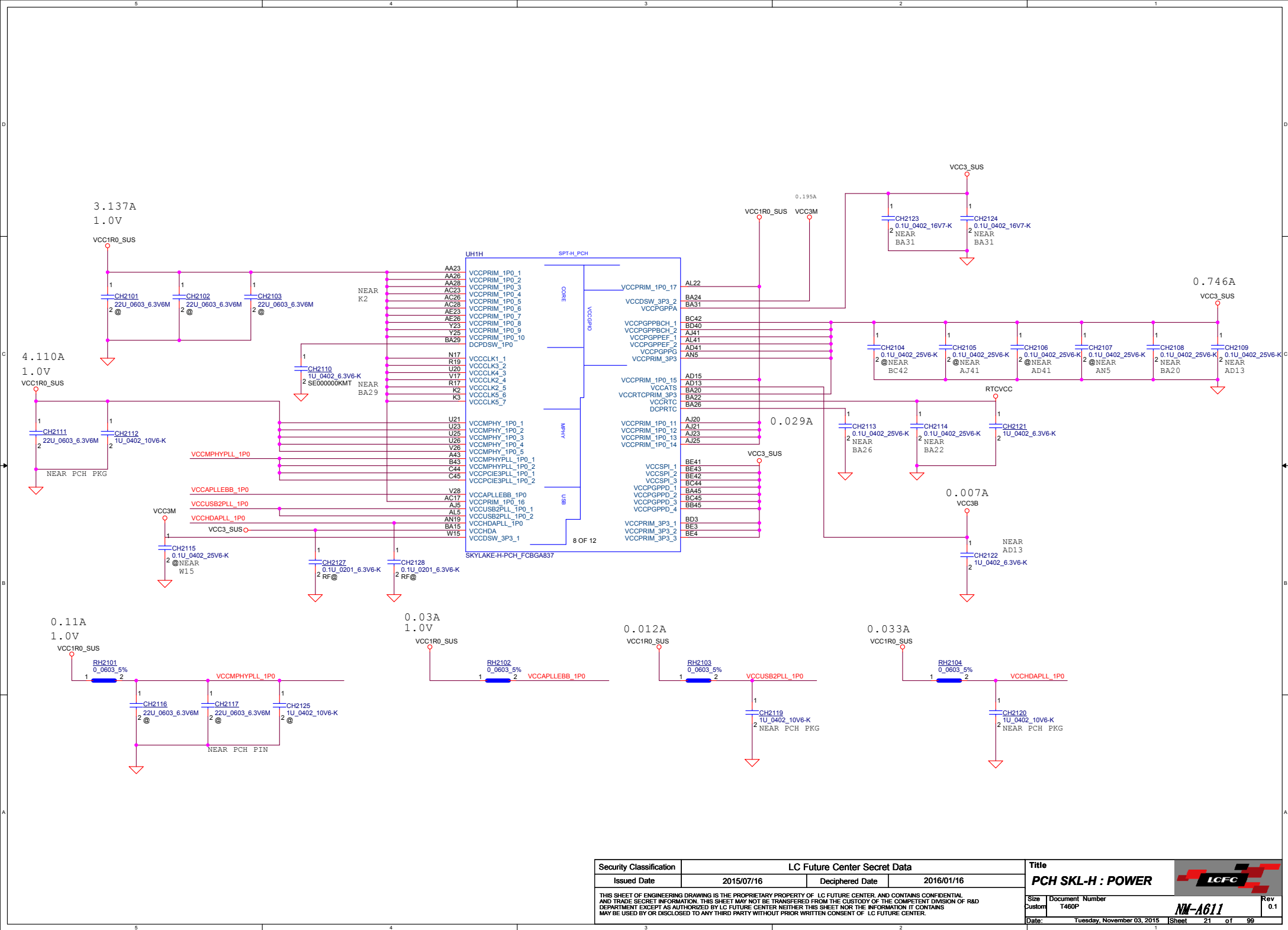
[51] CLKREQ_PCIE3_LAN#
[54] CLKREQ_PCIE4_CR#
[31] CLKREQ_PCIE5_VGA#

VCC3B

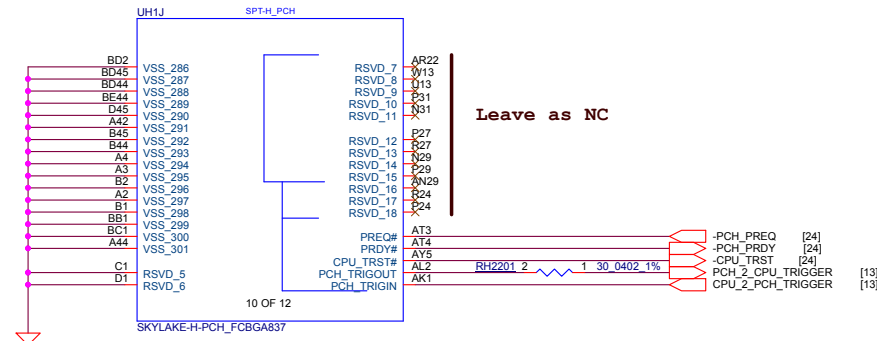
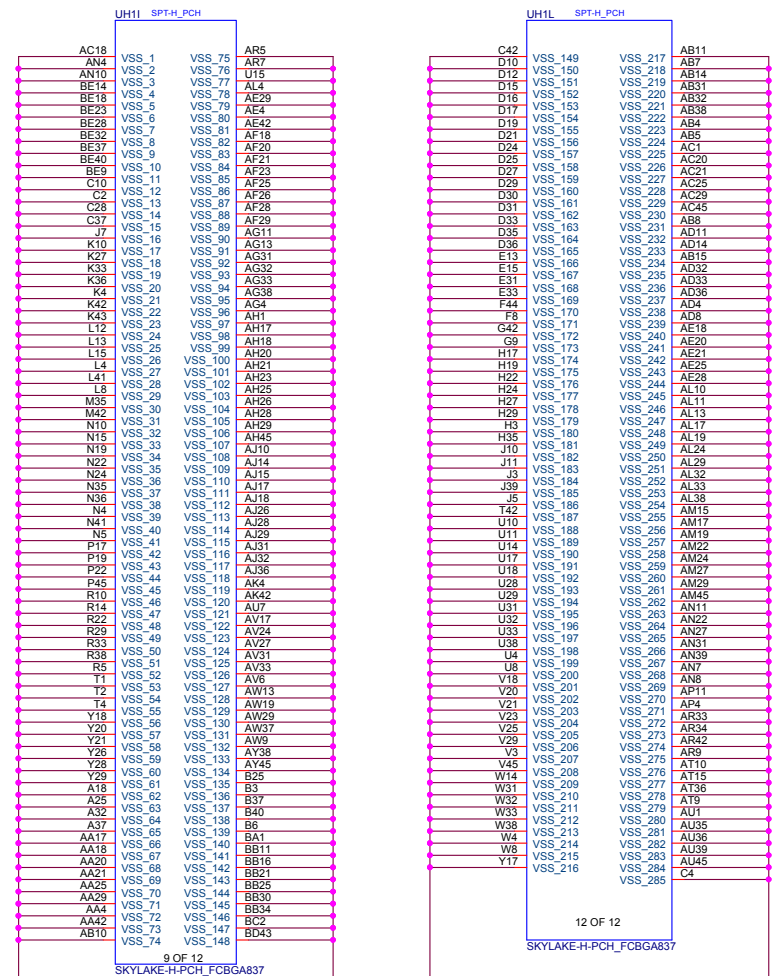


PCIE Clock Assignment
Clock 0 : WLAN
Clock 1 : SATA
Clock 3 : Giga LAN
Clock 4 : CARD READER
Clock 5 : GPU N16S-GT

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2015/07/16		2016/01/16		Size Document Number T460P		Rev 0.1 NW-A611	
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Leave as NC

[17]	JTAGX		JTAGX	R2407	1		2	0.0402 5%	XDP_TCK_R
[17]	PCH_TMS		PCH_TMS						
[17]	PCH_TDI		PCH_TDI						
[22]	-CPU_TRST		-CPU_TRST	R2410	1		2	0.0402 5%	-XDP_TRST_R
[22]	PCH_TDO		PCH_TDO						
[22]	-PCH_PRDY		-PCH_PRDY	R2413	1		2	0.0402 5%	-XDP_PRDY_R
[22]	-PCH_PREQ		-PCH_PREQ	R2415	1		2	0.0402 5%	-XDP_PREQ_R

VCC3_SUS

R2406
1K_0402_5%

Place near PCH

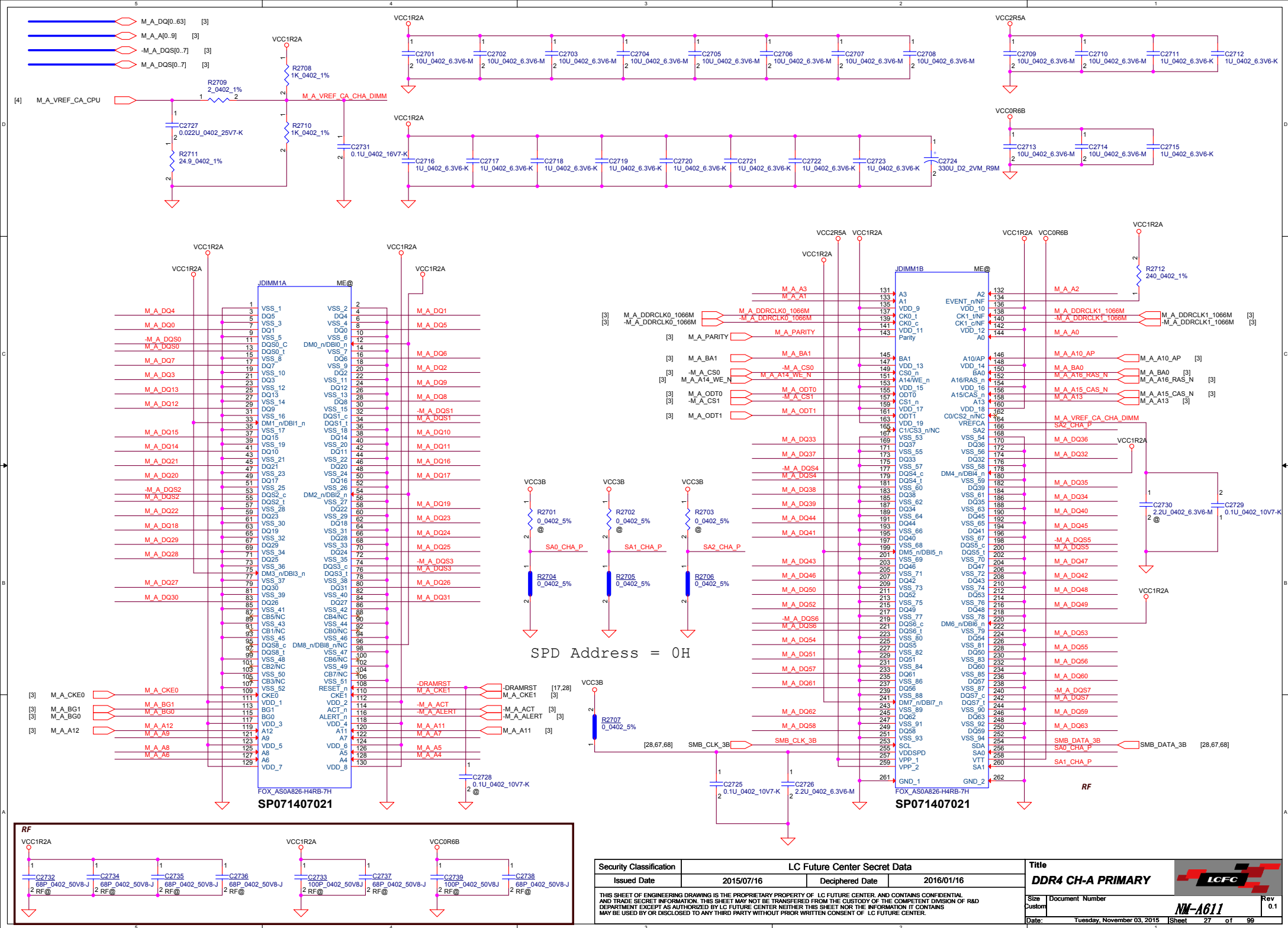
GPP_B18_NO_REBOOT

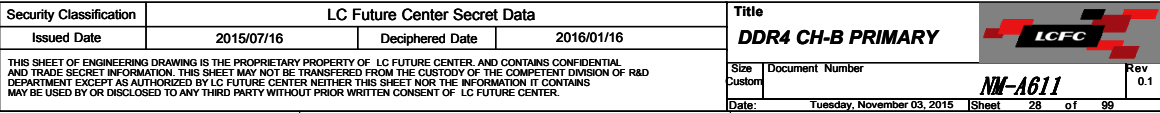
GPP B18 NO REBOOT [23]

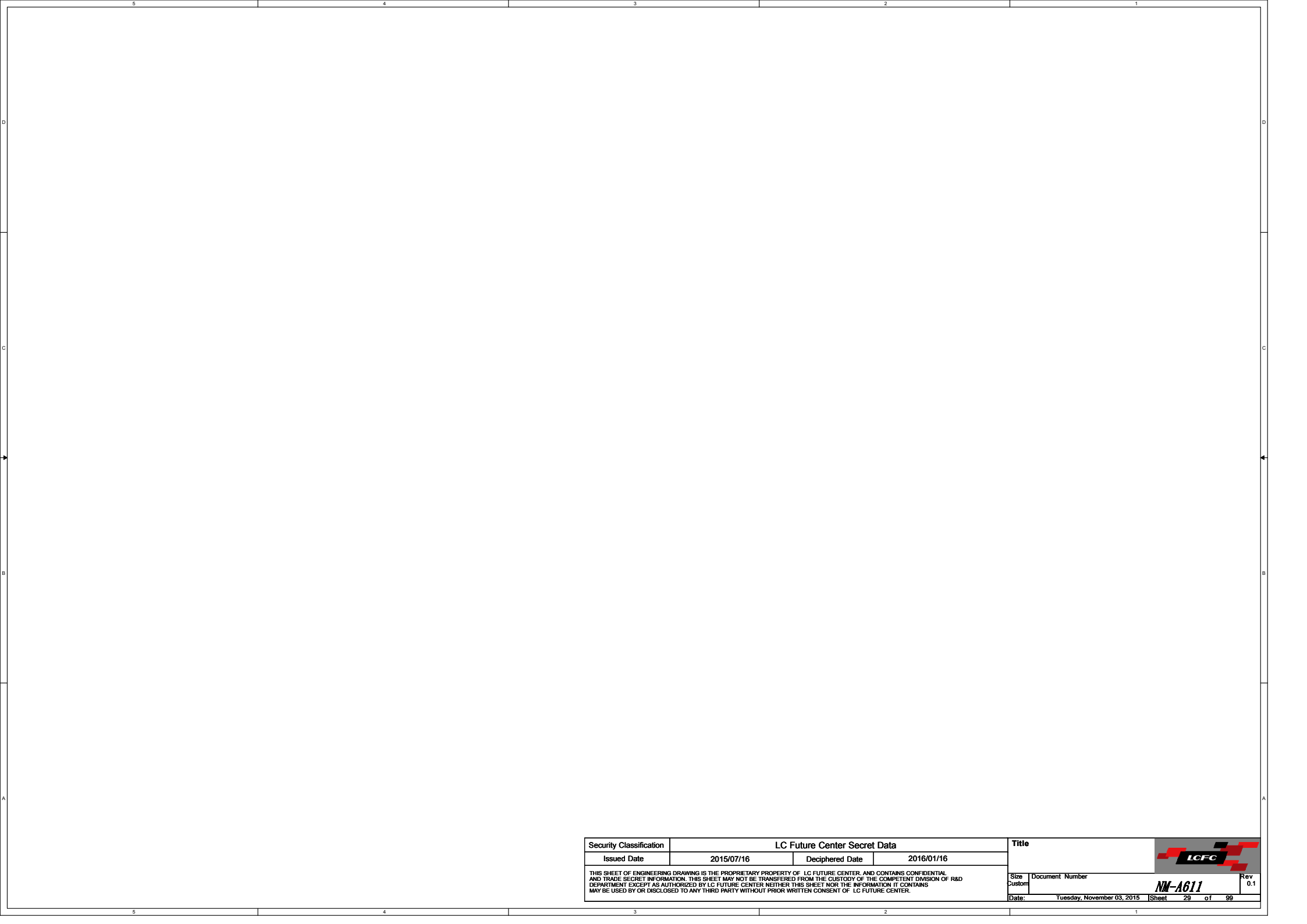
	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

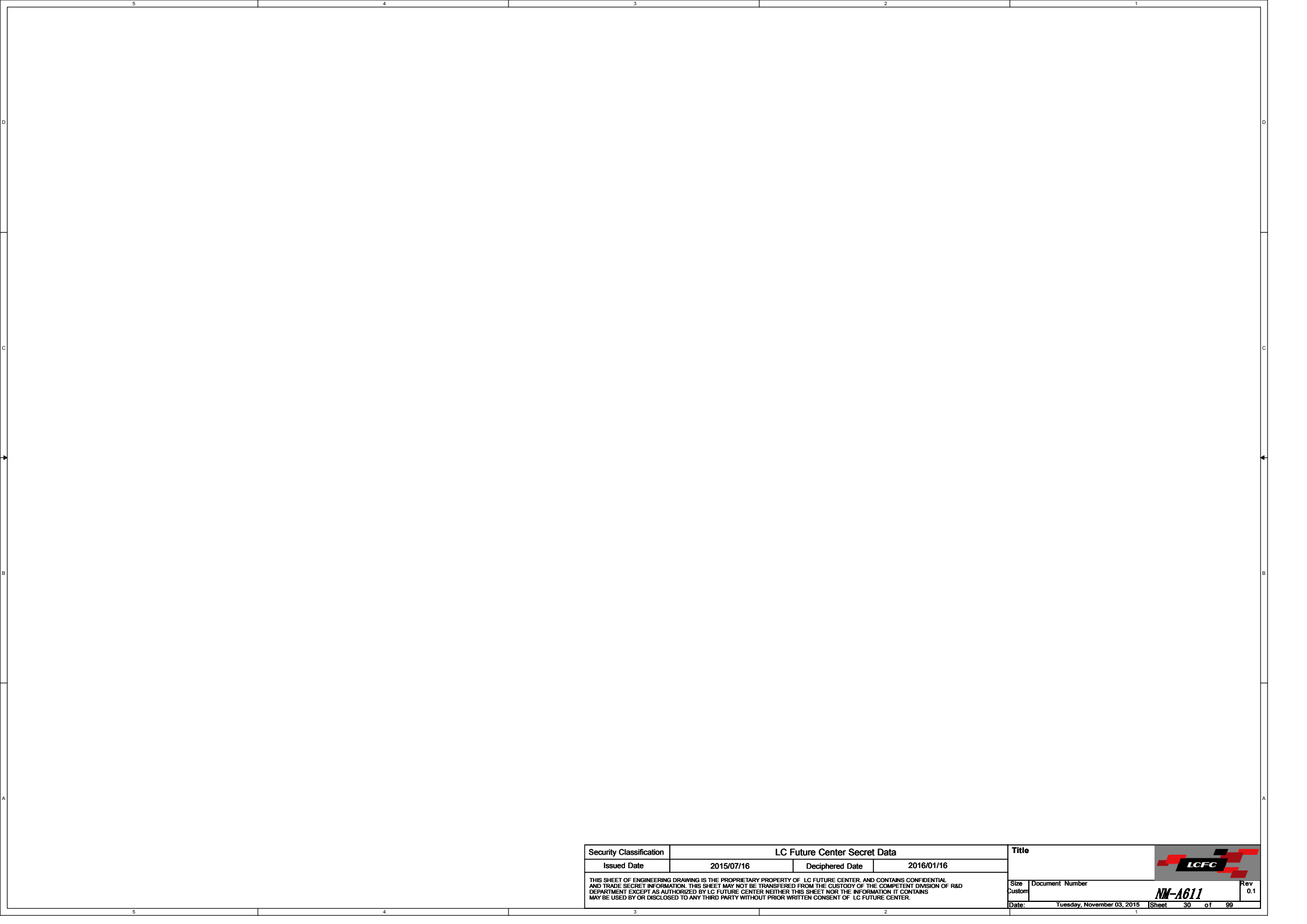
GPP_B18/GSPI0_MOSI (No Reboot)		R2406
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM



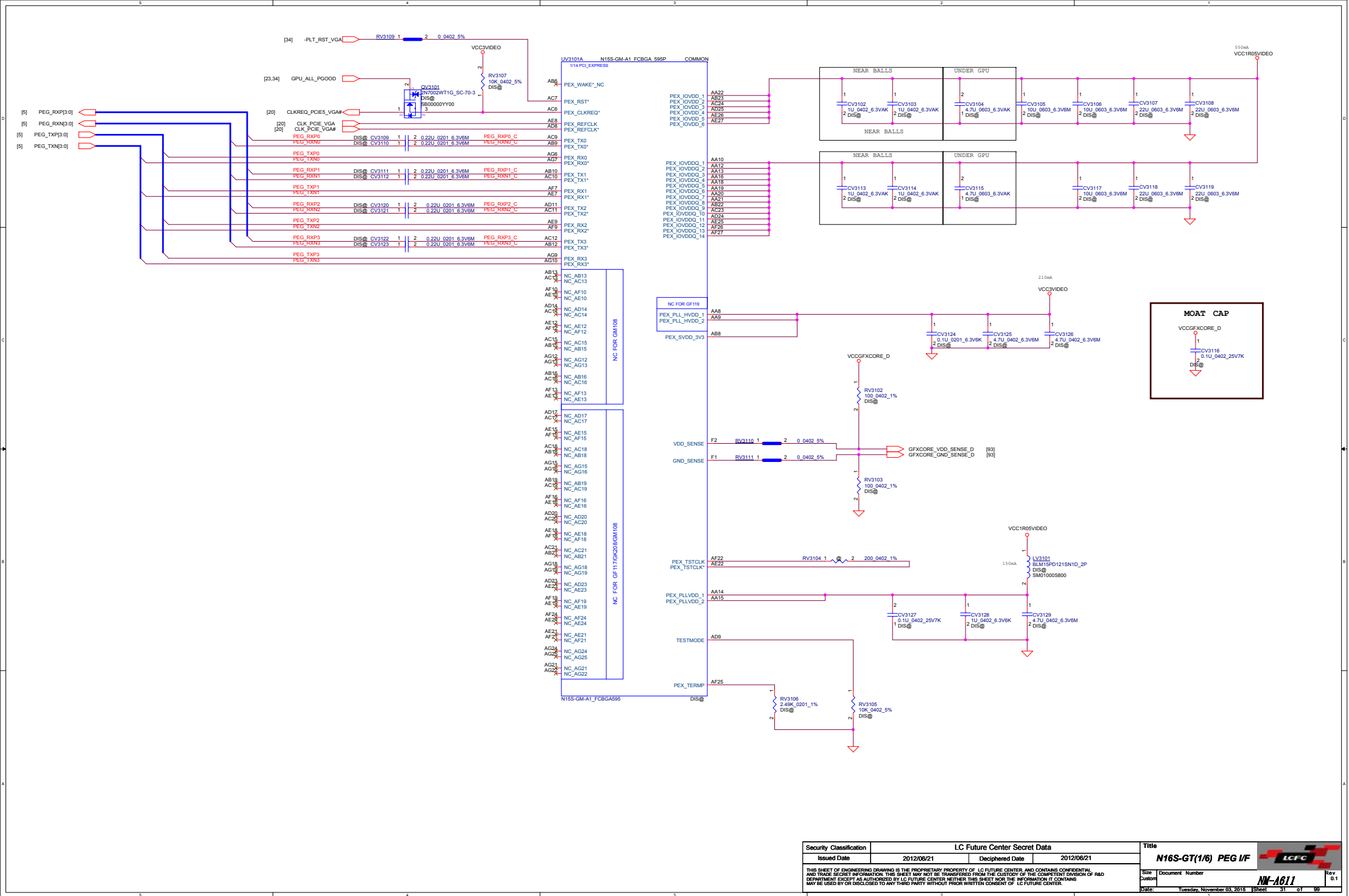


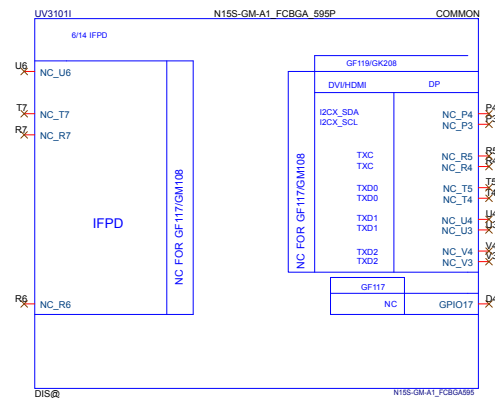
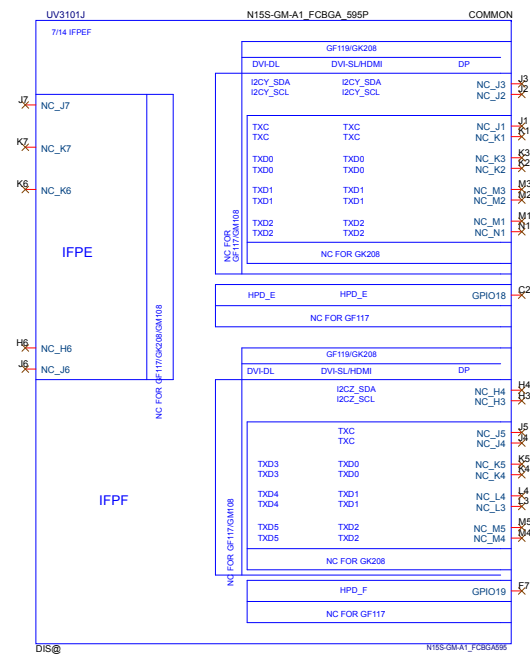
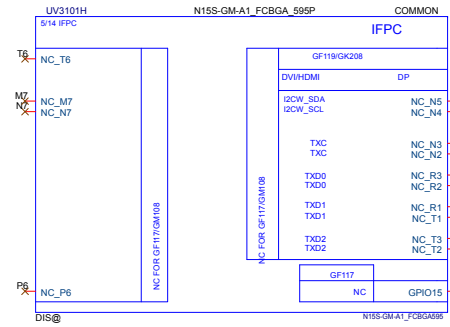
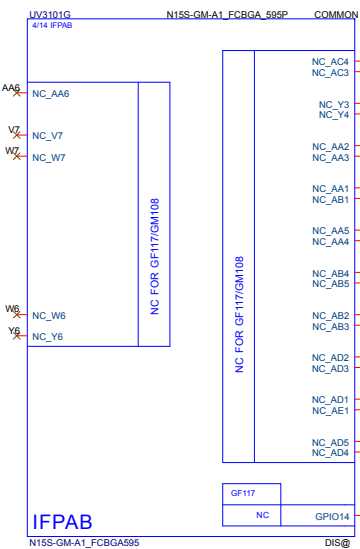


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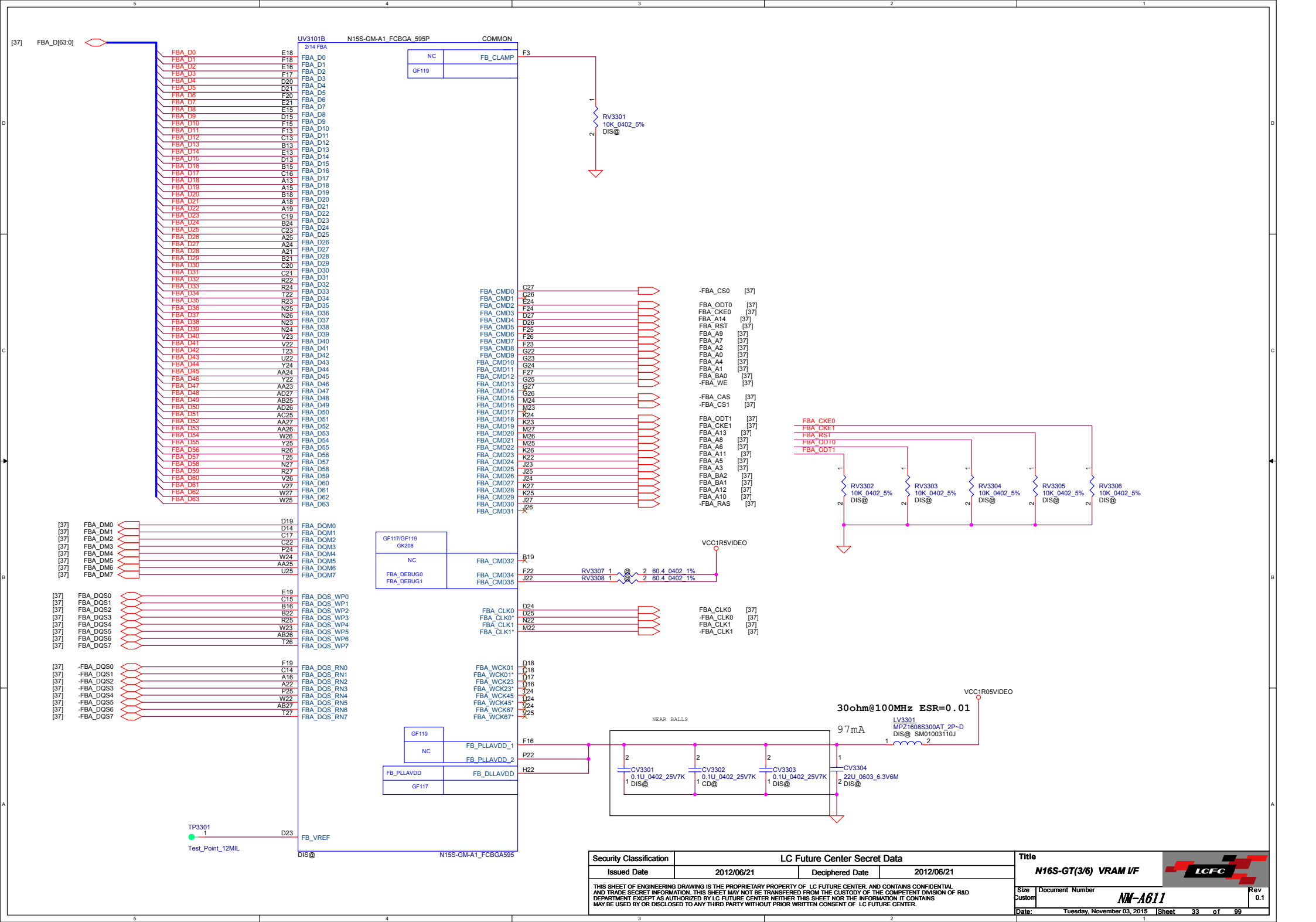


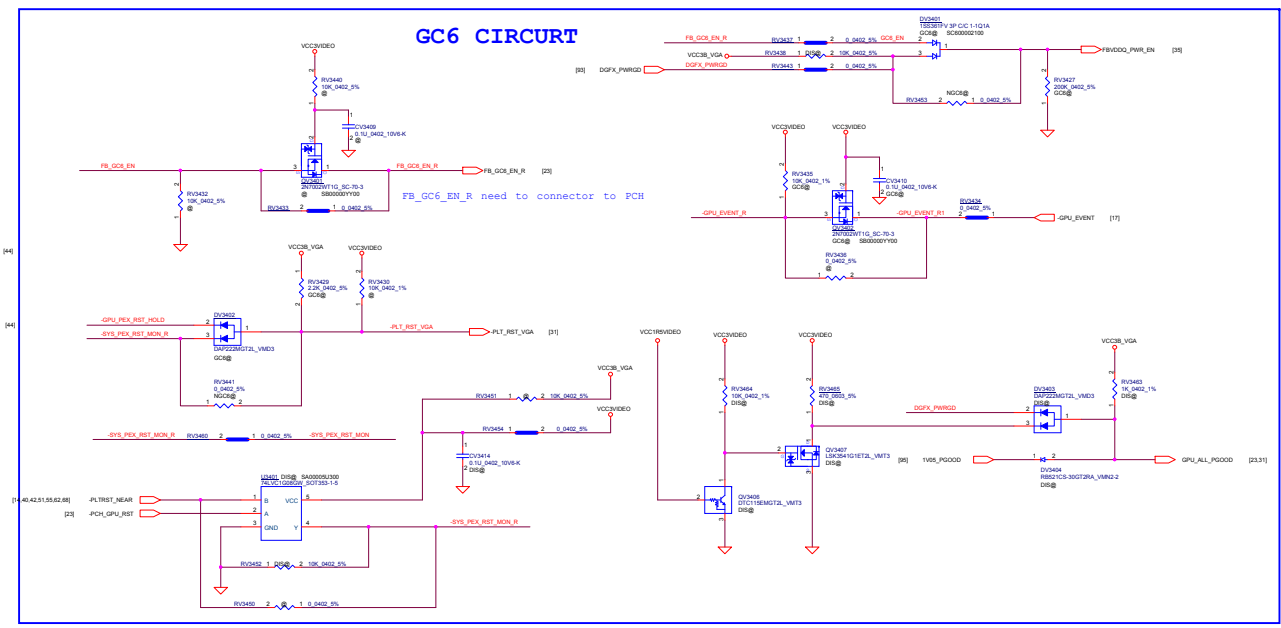
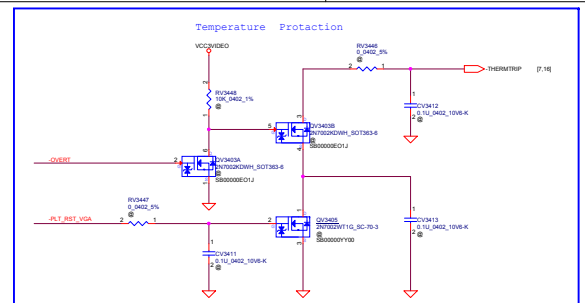
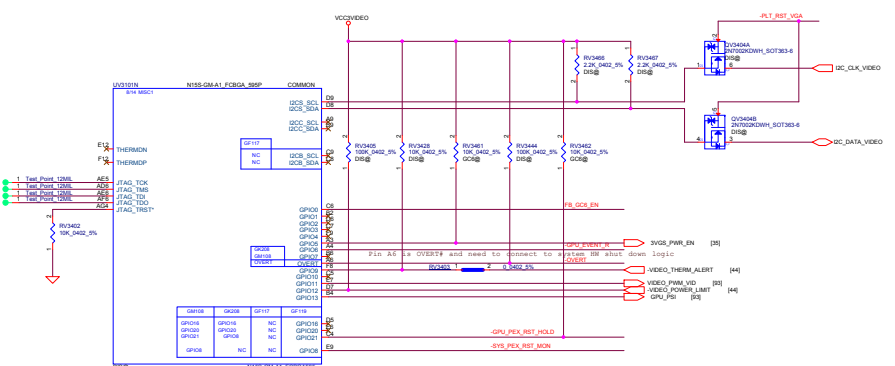
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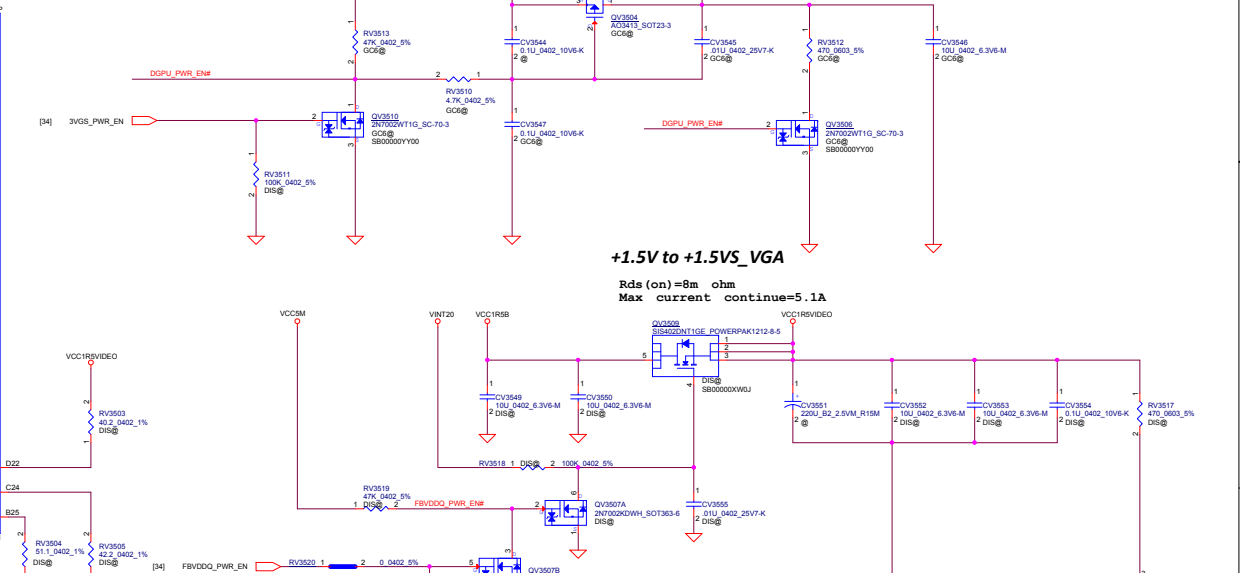
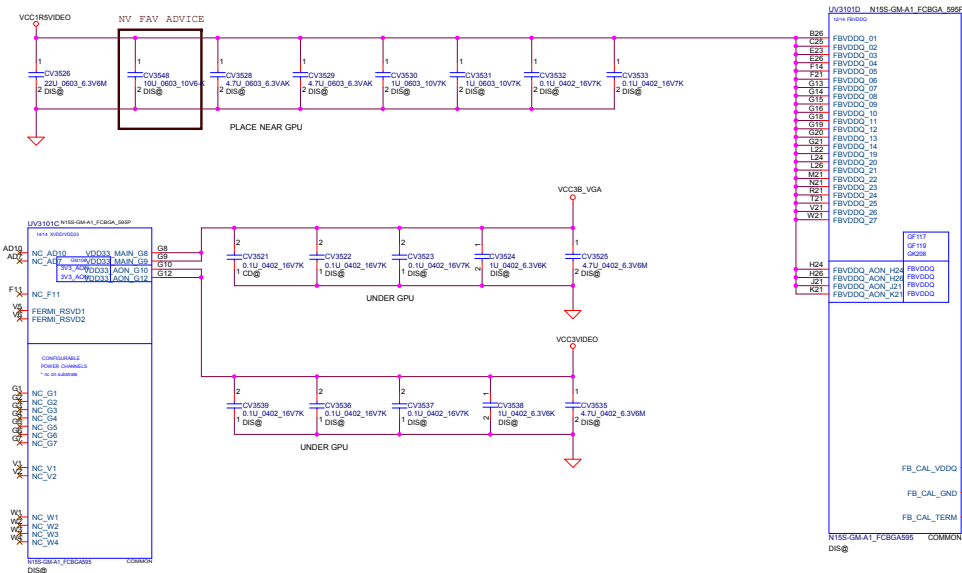
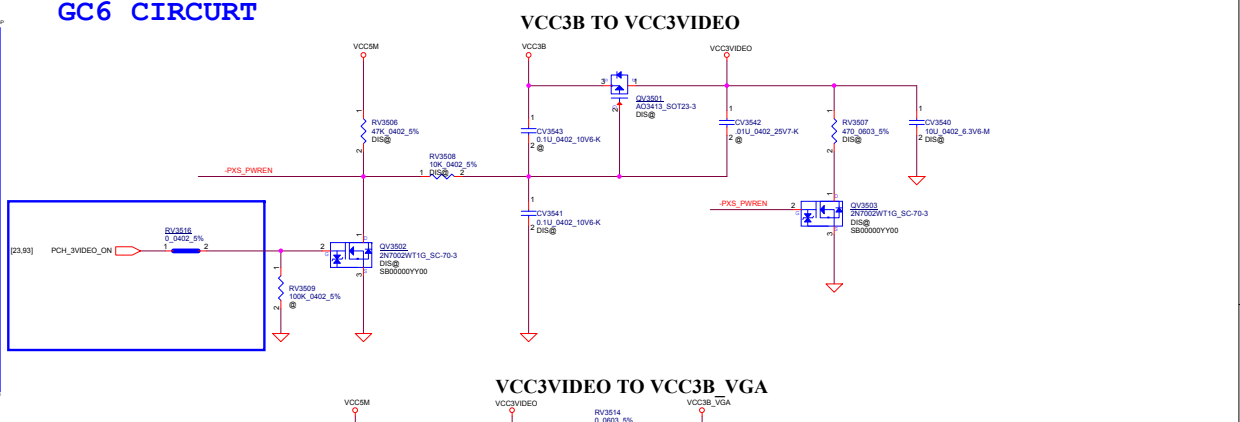
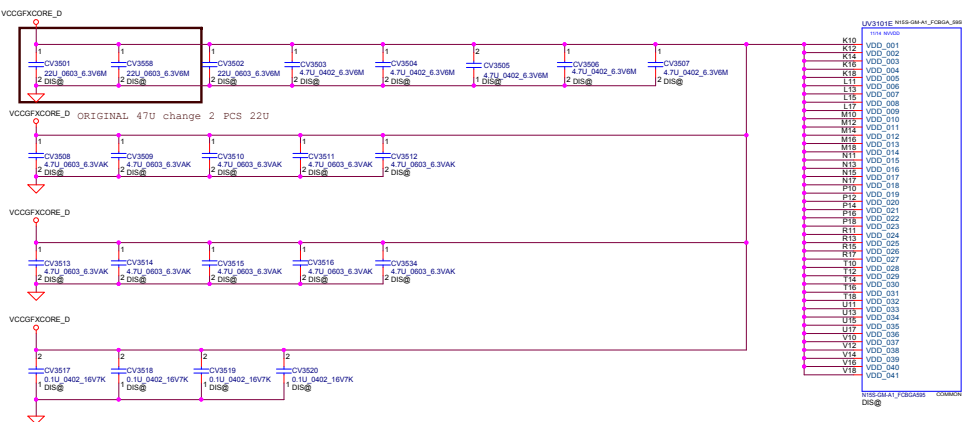


CB_1_SWG_SDV_EC006

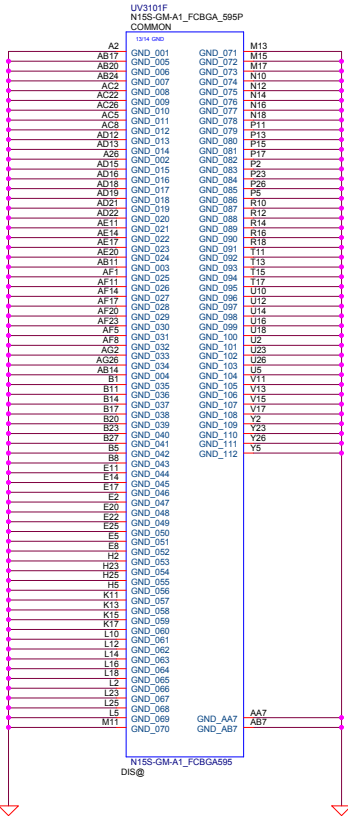




GC6 CIRCUIT



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FB CMD mapping Mode D-N14x

TABLE

DDR3 VIDEO MEMORY

	Micron 4GBITS (256Mx16)	HYNIX 4GBITS(256Mx16)	SAMSUNG 4GBITS(256Mx16)	SAMSUNG 4GBITS(256Mx16)	HYNIX 4GBITS(256Mx16)
UV3701 UV3702 UV3703 UV3704	MT41J256M16HA-093G:E(Die) 256Mx16 SA00006000	H5TC4G63AFR-11C (A-Die)256Mx16 SA00005Y1L10	K4W4G1646D-BC1A (D-Die)256Mx16 SA000063F00	K4W4G1646E-BC1A (D-Die)256Mx16(LFCF USE) SA000063F30	H5TC4G63CFR-N0C(C-Die) 256Mx16(LFCF USE) SA00007DU00
BOM Structure	VME2G@	VHA2G@	VSD2G@	VSE2G@	VHC2G@

* FOR DEV

[33] FBA_D[0:3]

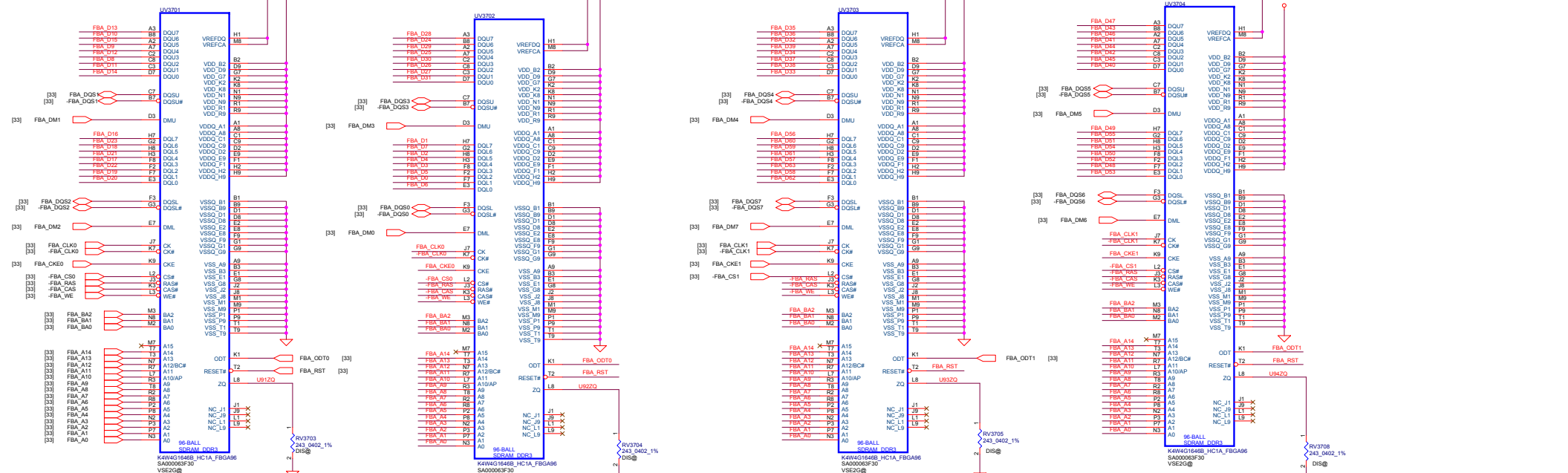


[39] FBA_VREF_0

FBA_VREF_0

[39] FBA_VREF_1

FBA_VREF_1



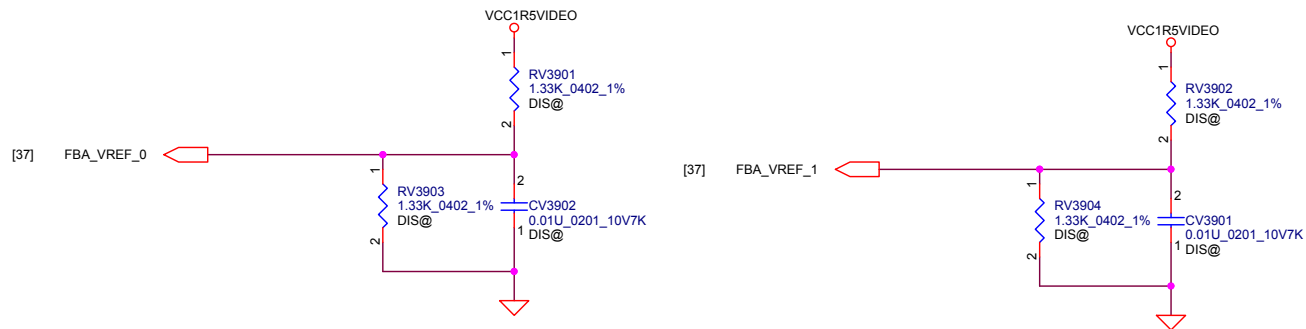
For UV3701
CLOSE TO THE MEMORY

For UV3702
CLOSE TO THE MEMORY

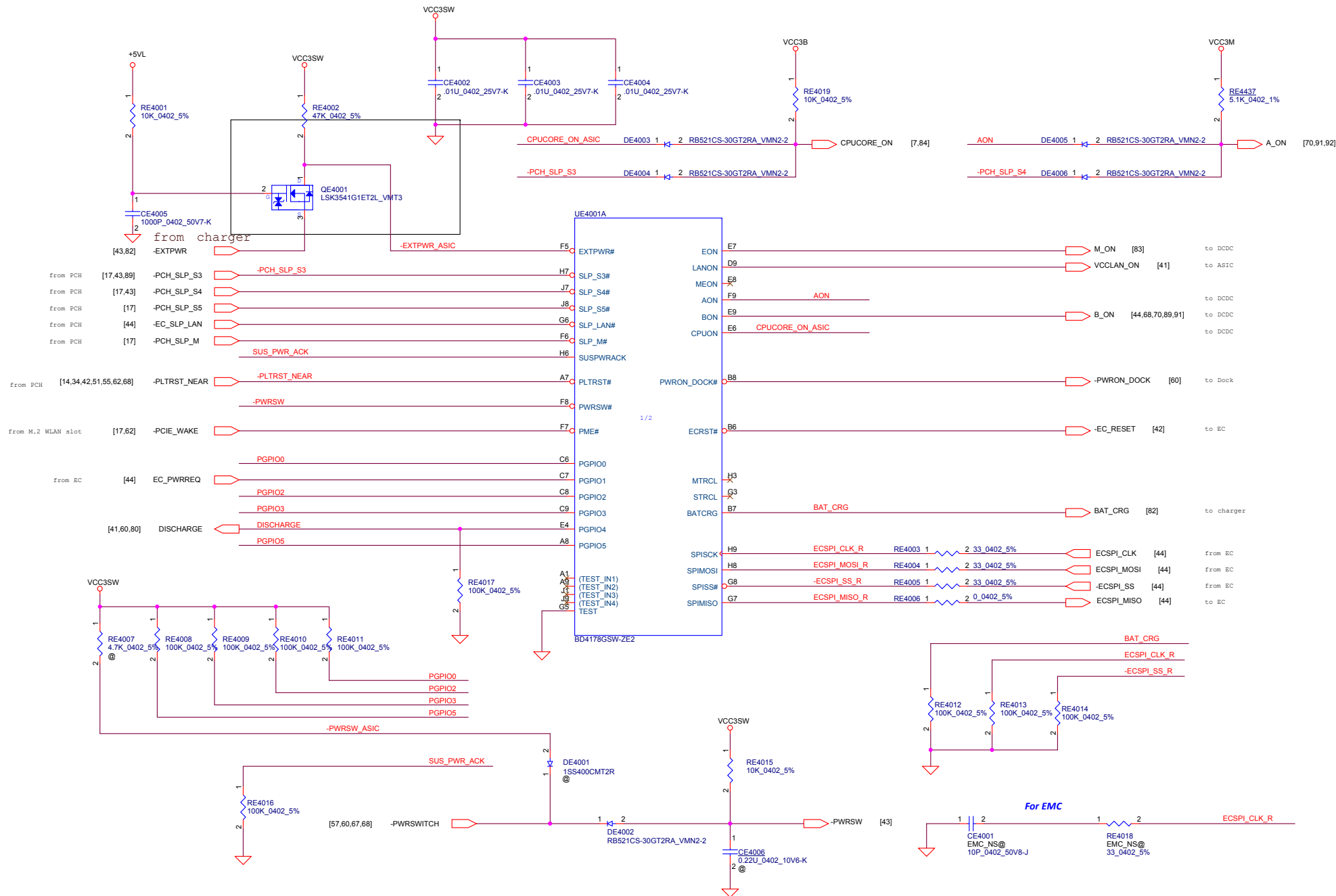
For UV3703
CLOSE TO THE MEMORY

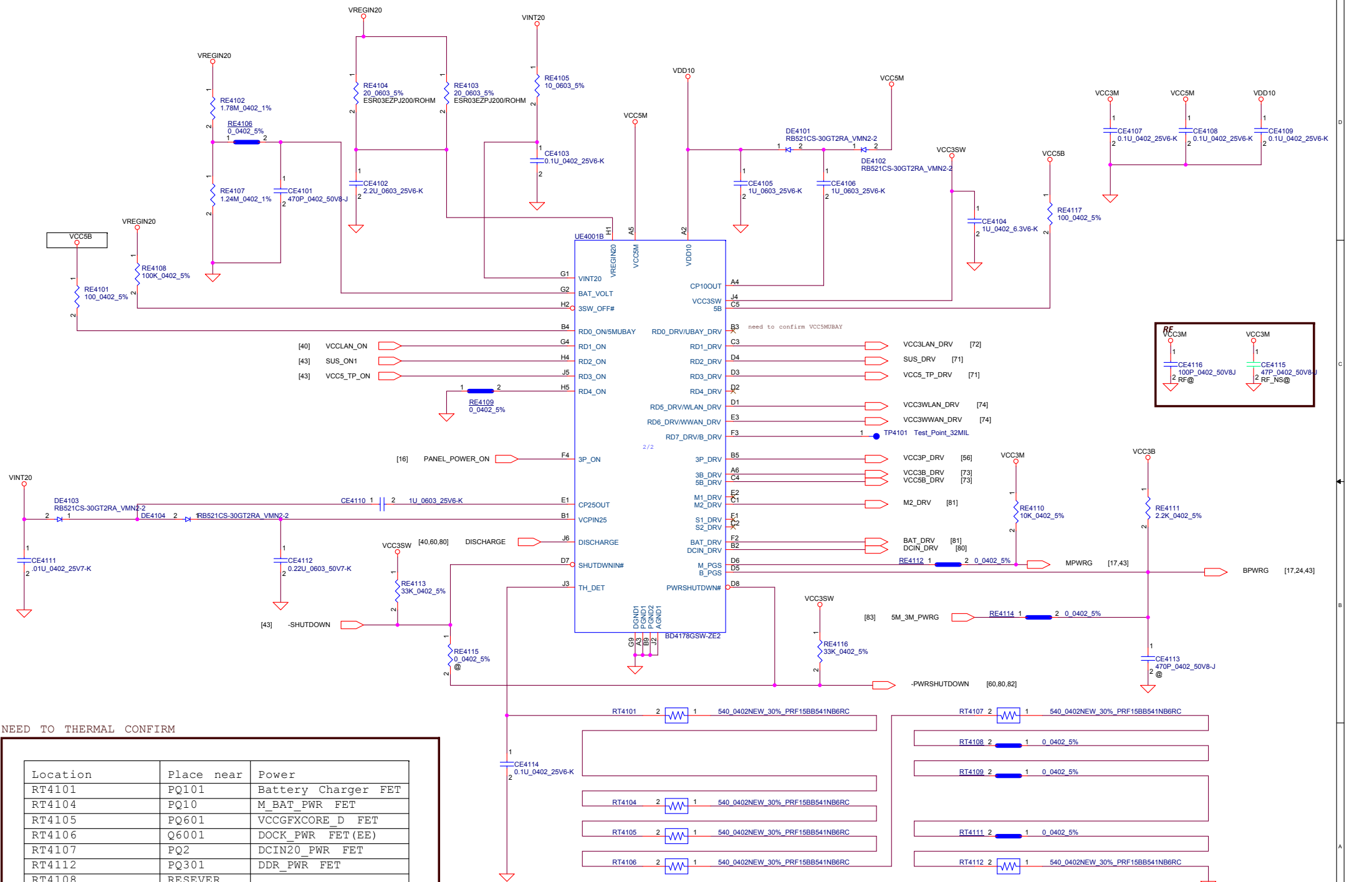
For UV3704
CLOSE TO THE MEMORY

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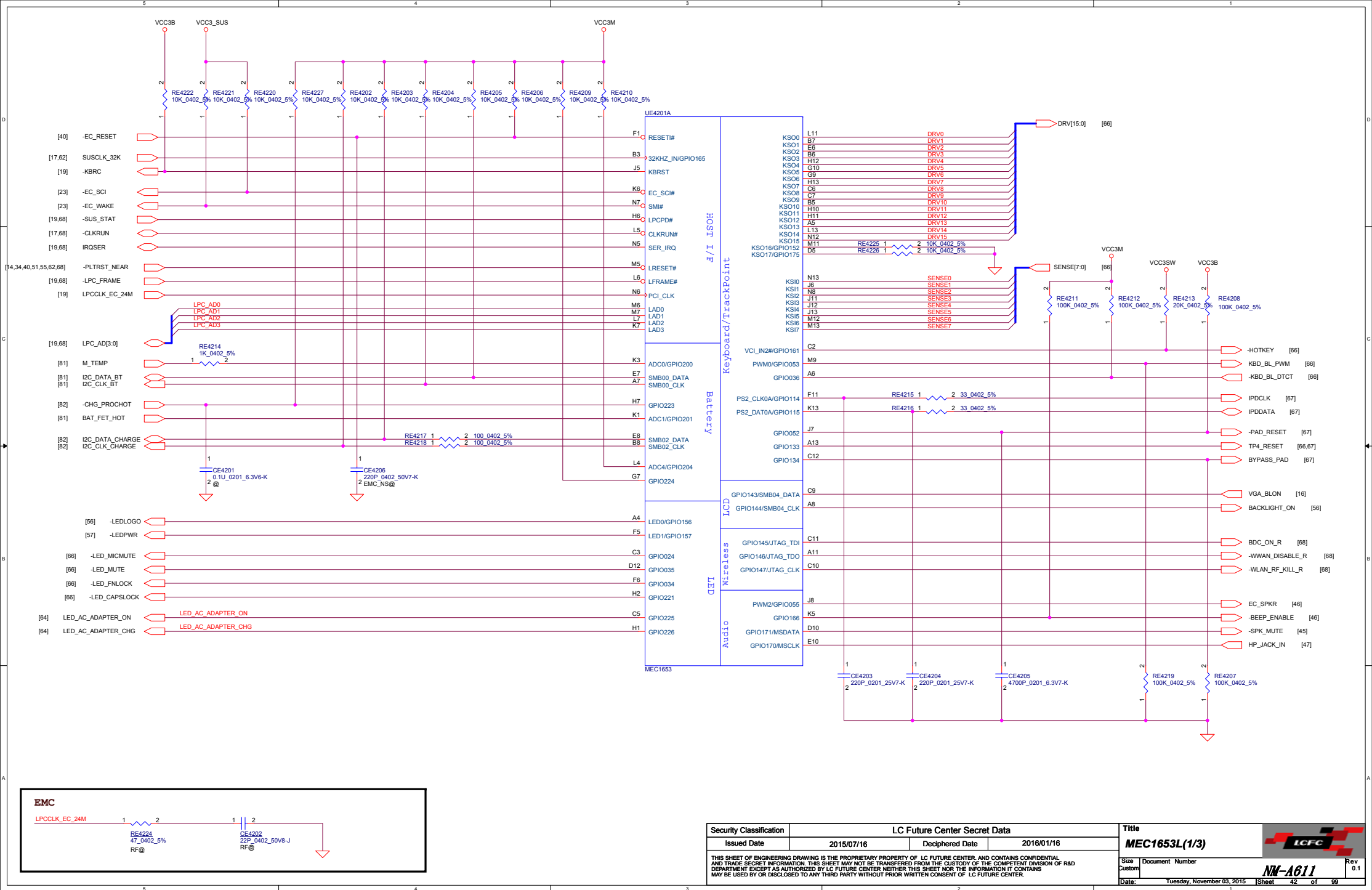
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				B	NM-A611	0.1
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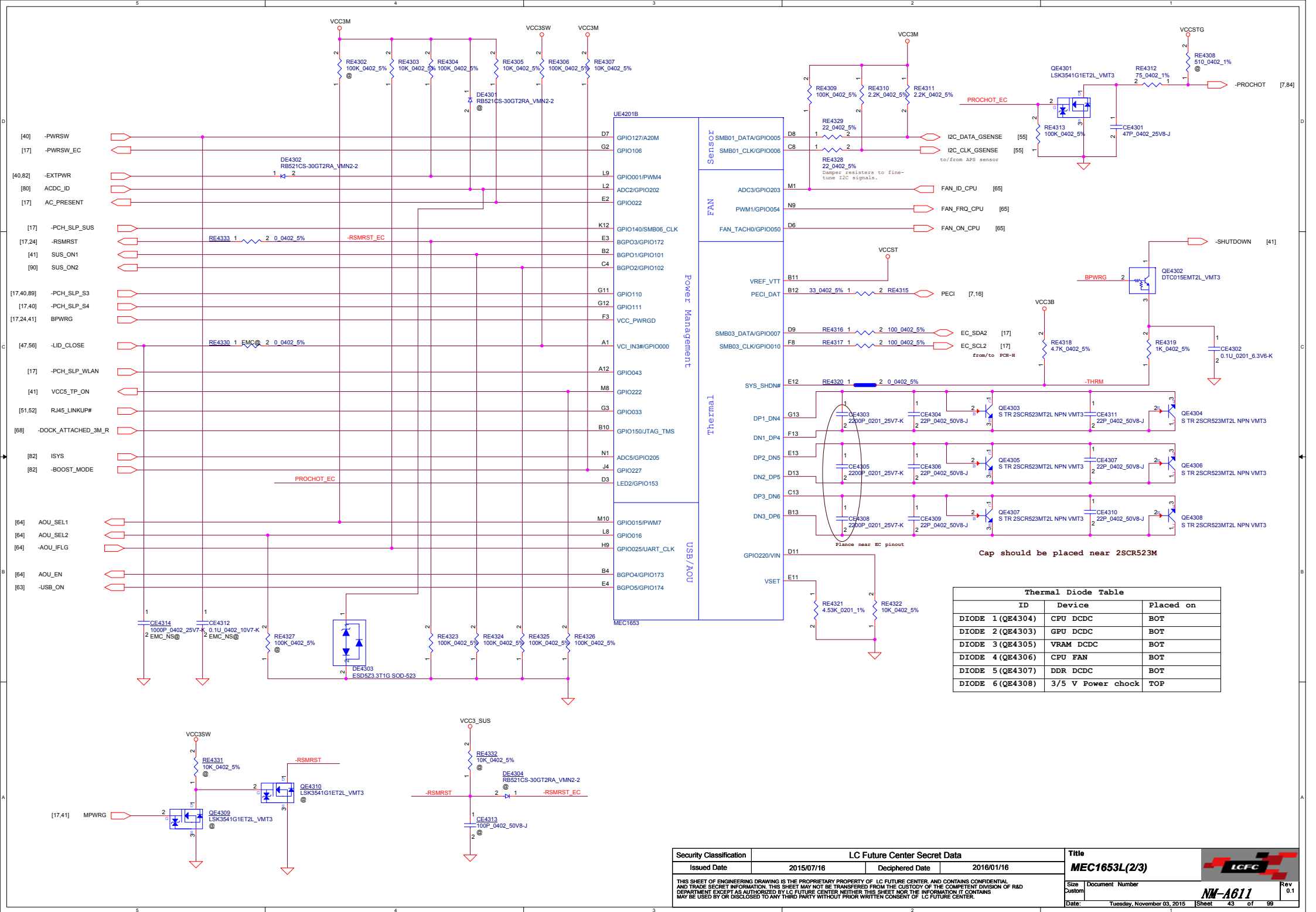




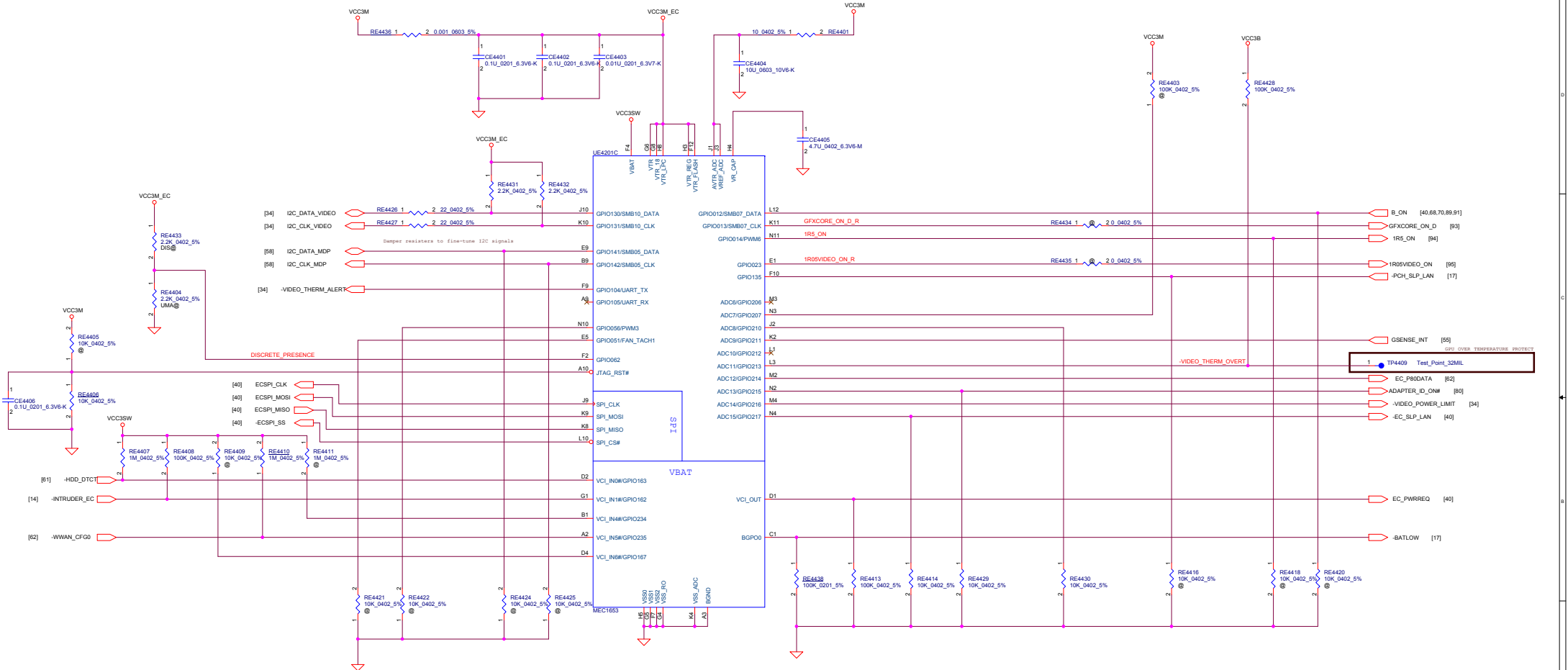
NEED TO THERMAL CONFIRM

Location	Place near	Power
RT4101	PQ101	Battery Charger FET
RT4104	PQ10	M_BAT_PWR FET
RT4105	PQ601	VCCGFXCORE_D FET
RT4106	Q6001	DOCK_PWR FET (EE)
RT4107	PQ2	DCIN20_PWR FET
RT4112	PQ301	DDR_PWR FET
RT4108	RESEVER	
RT4109	RESEVER	
RT4111	RESEVER	

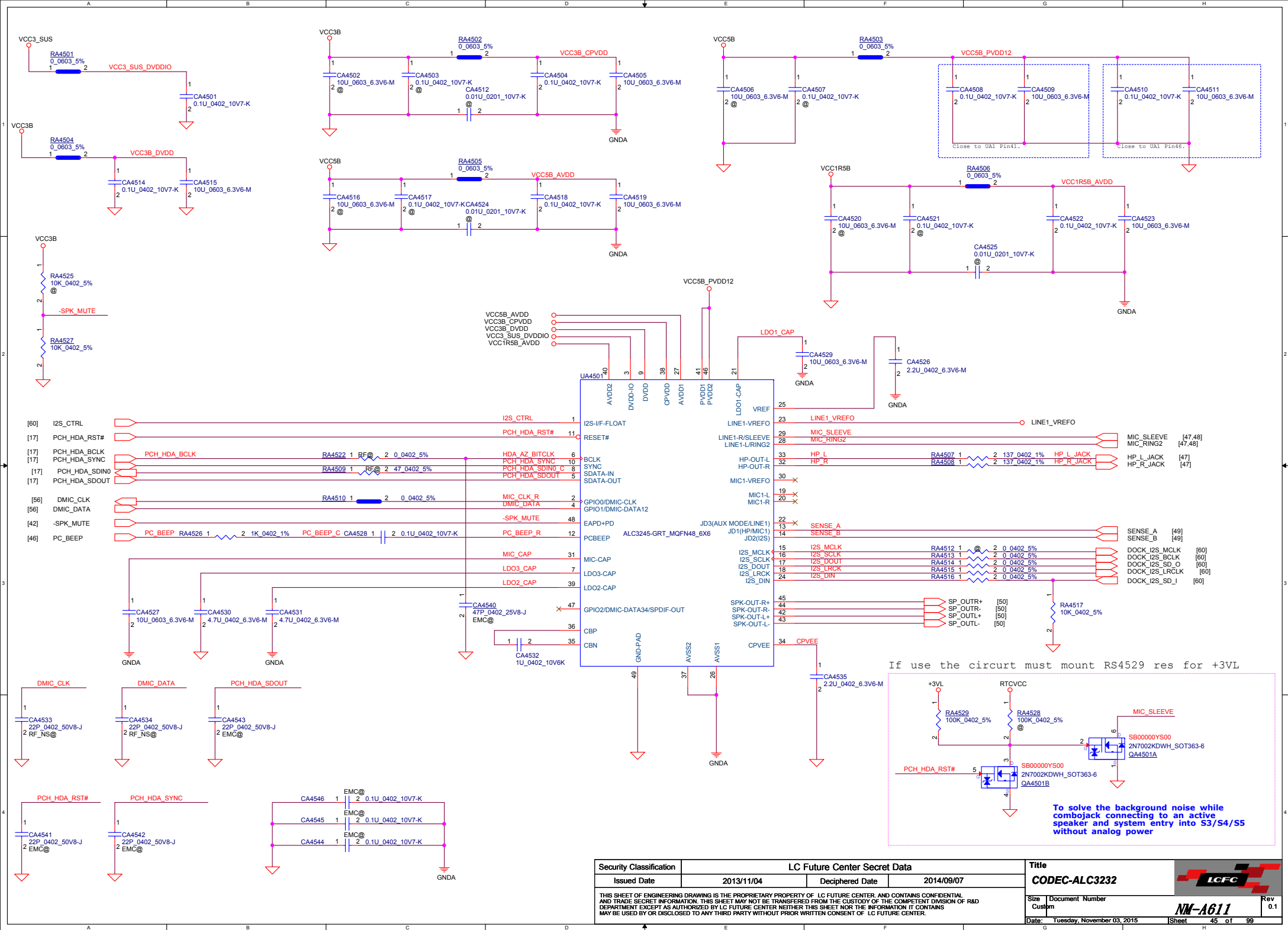




Thermal Diode Table		
ID	Device	Placed on
DIODE 1 (QE4304)	CPU DCDC	BOT
DIODE 2 (QE4303)	GPU DCDC	BOT
DIODE 3 (QE4305)	VRAM DCDC	BOT
DIODE 4 (QE4306)	CPU FAN	BOT
DIODE 5 (QE4307)	DDR DCDC	BOT
DIODE 6 (QE4308)	3/5 V Power chock	TOP

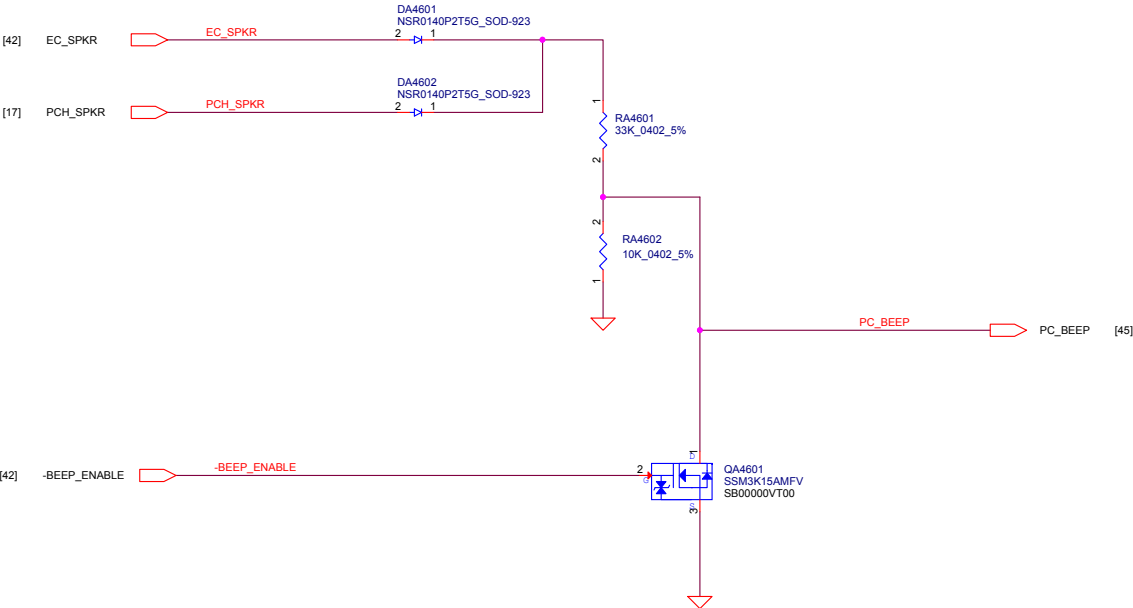


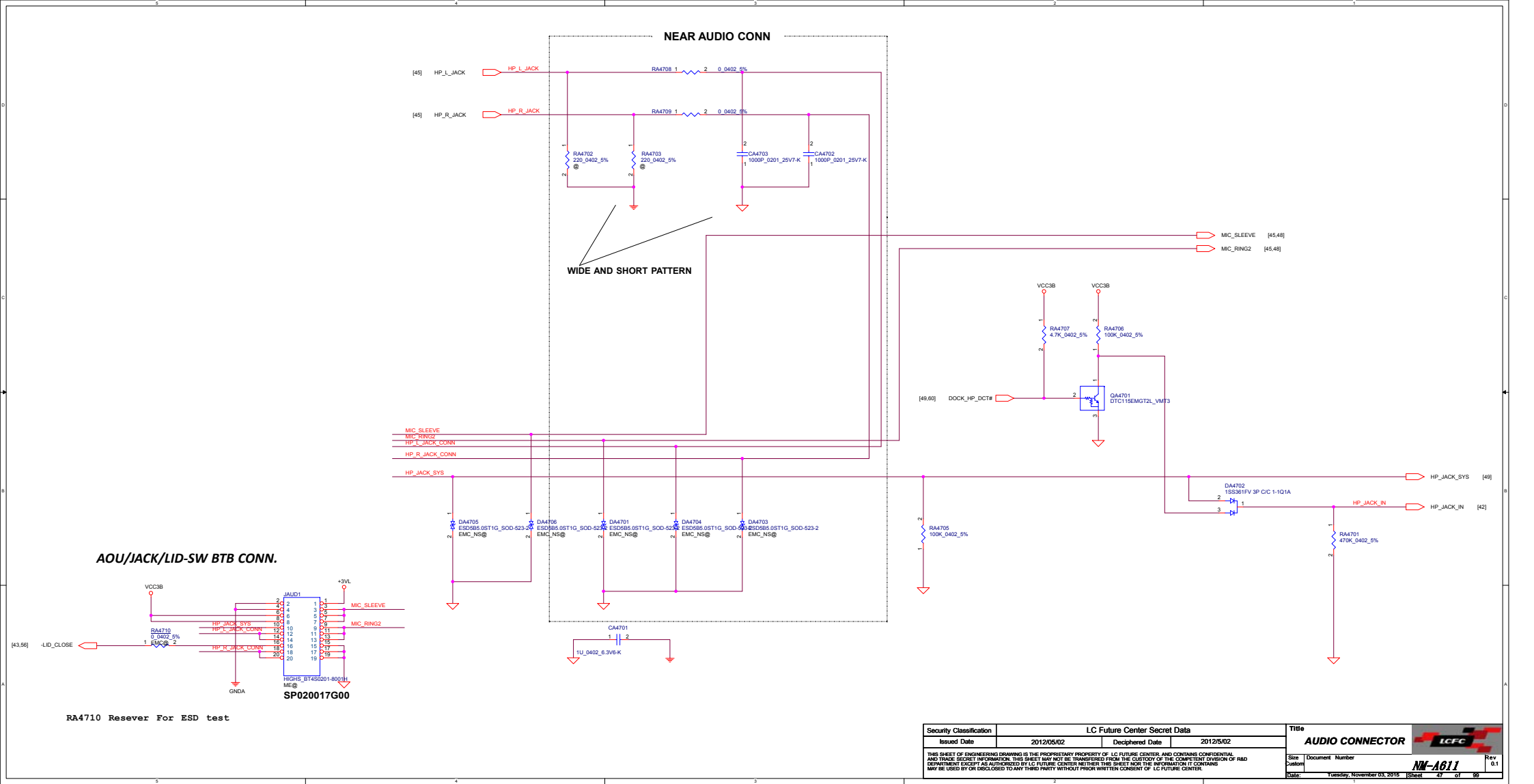
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/07/16	Deciphered Date	2016/01/16	MEC1653L(3/3)	
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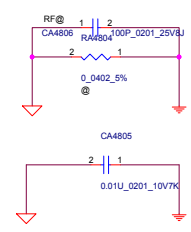
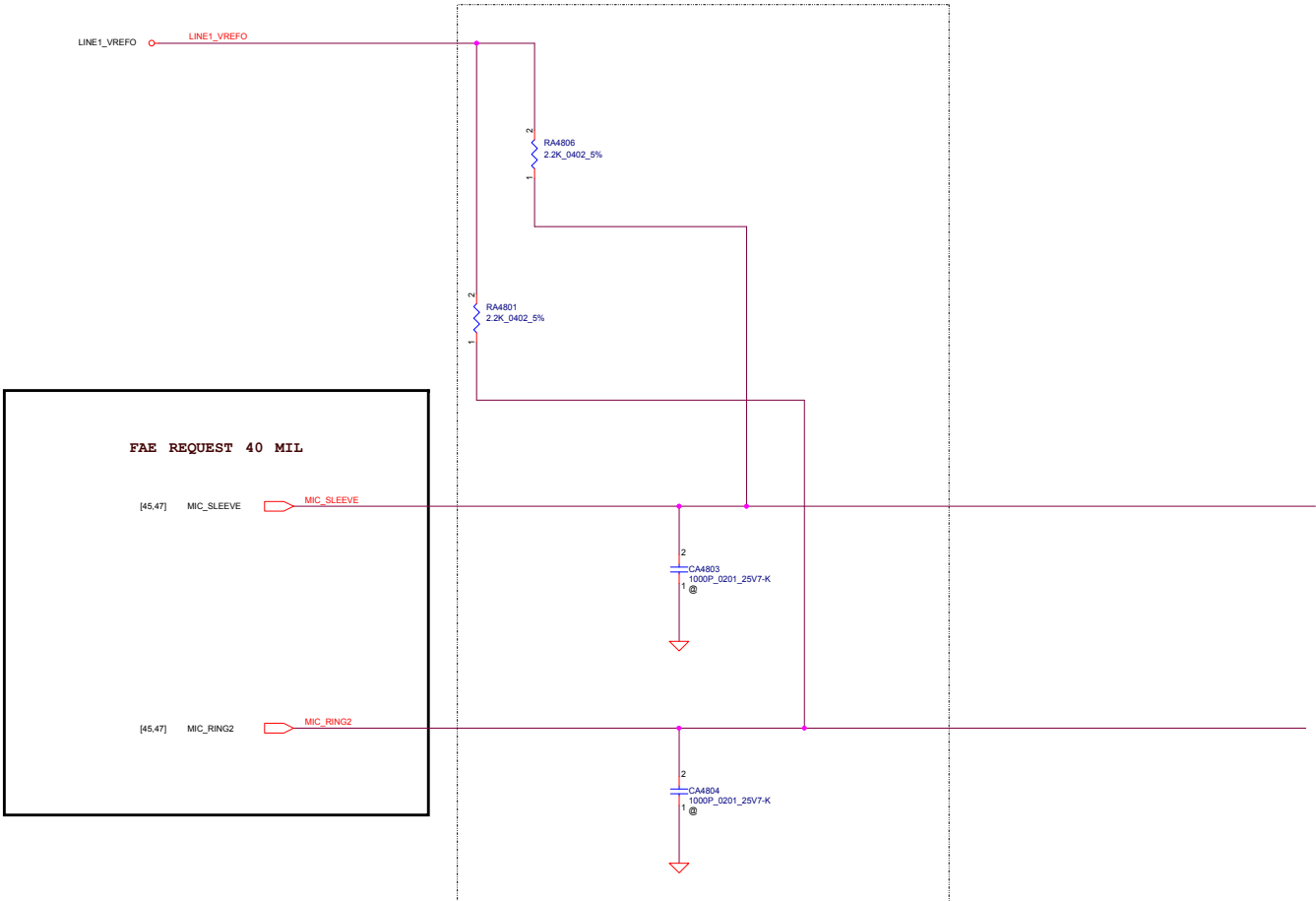


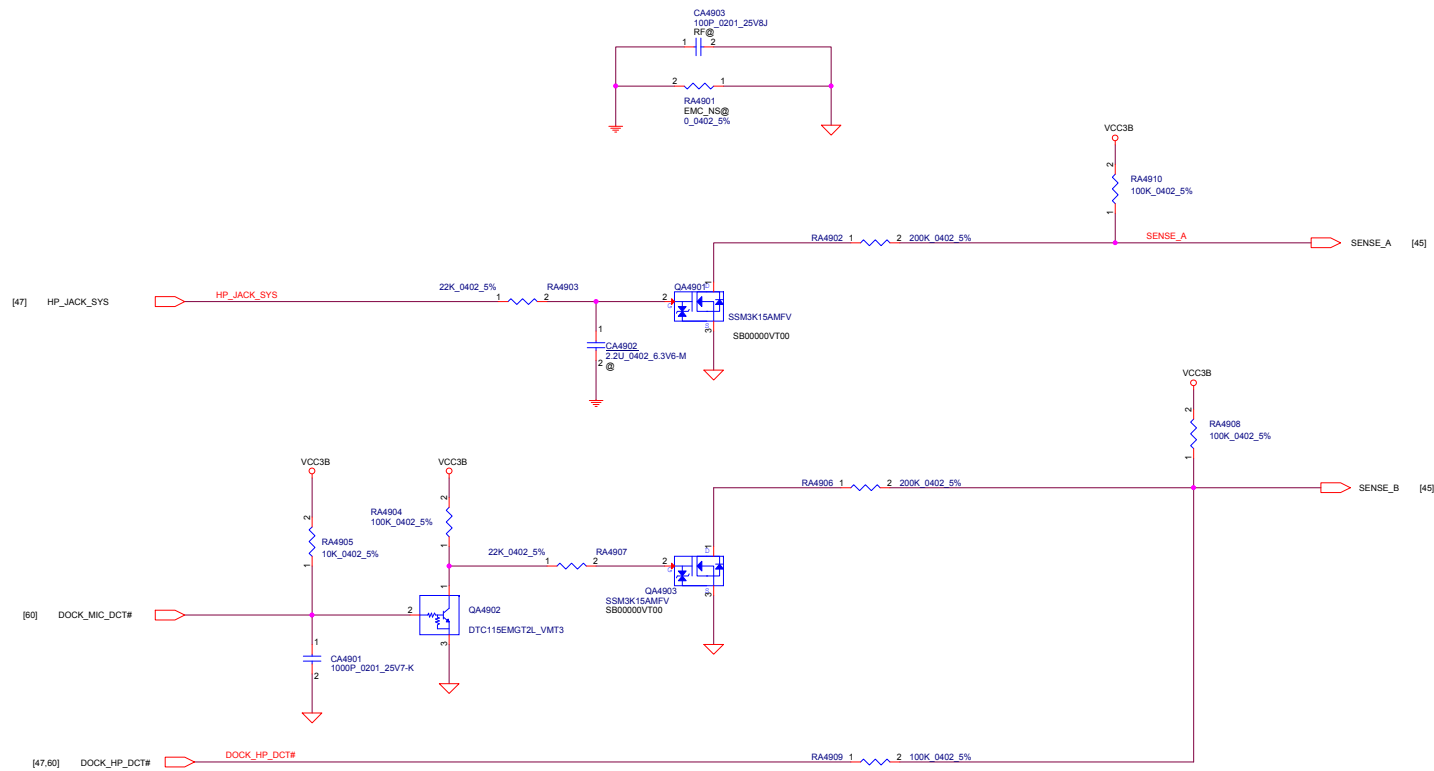
Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07
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PC-BEEP

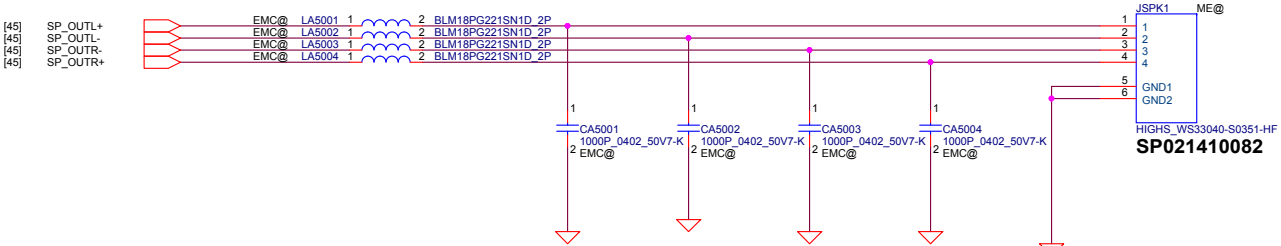




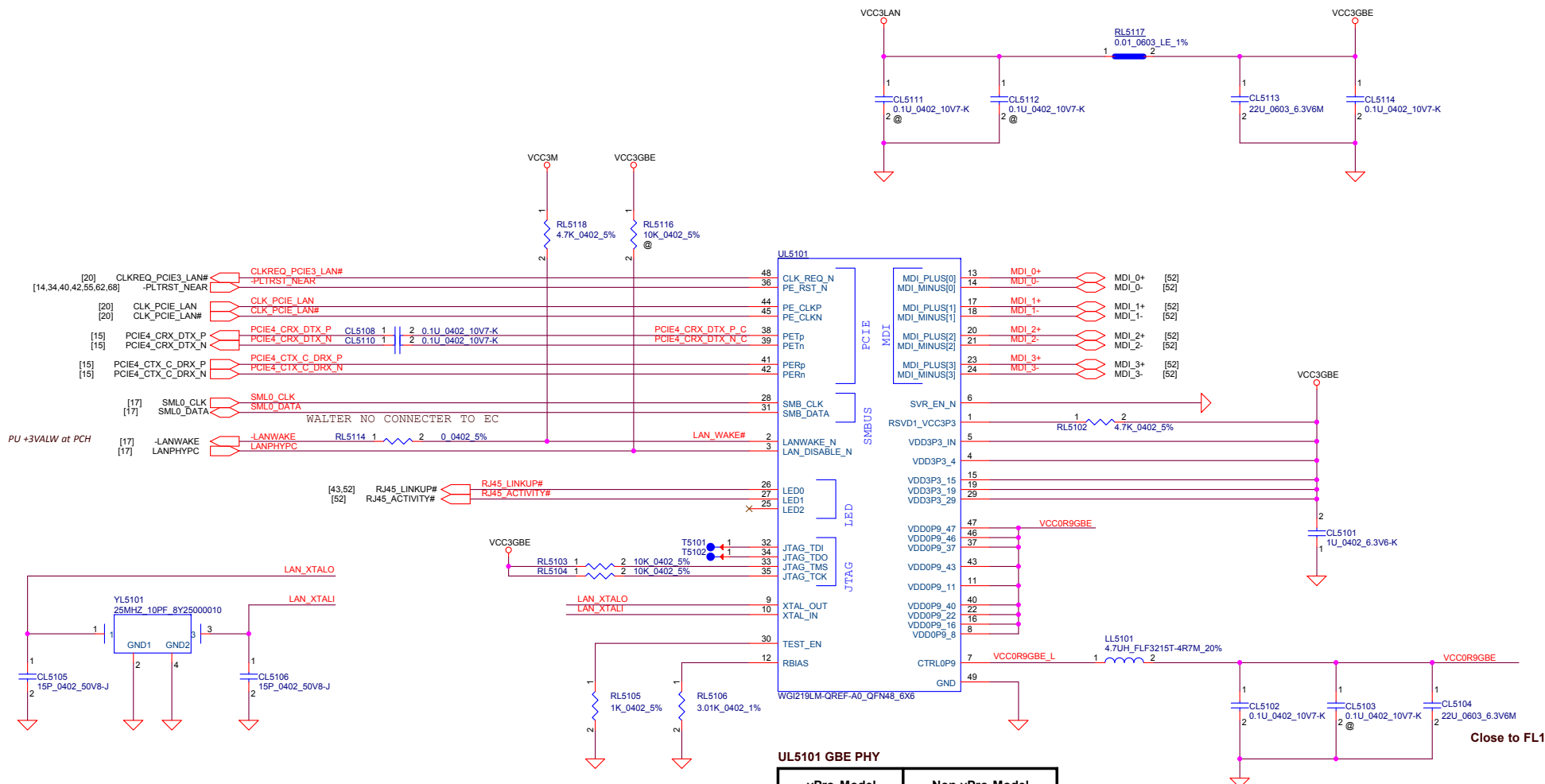




SPEAKER CONN.

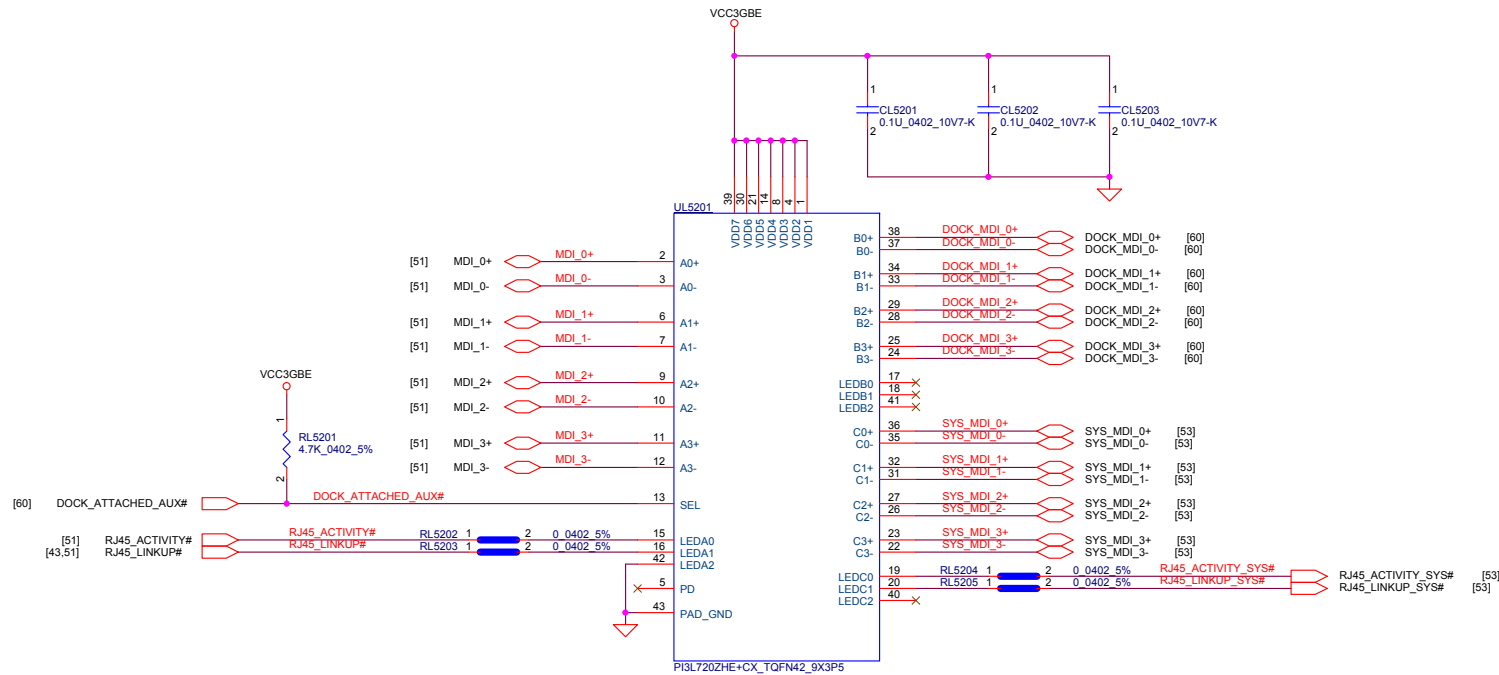


PLACE, NEAR SPEAKER CONNECTOR



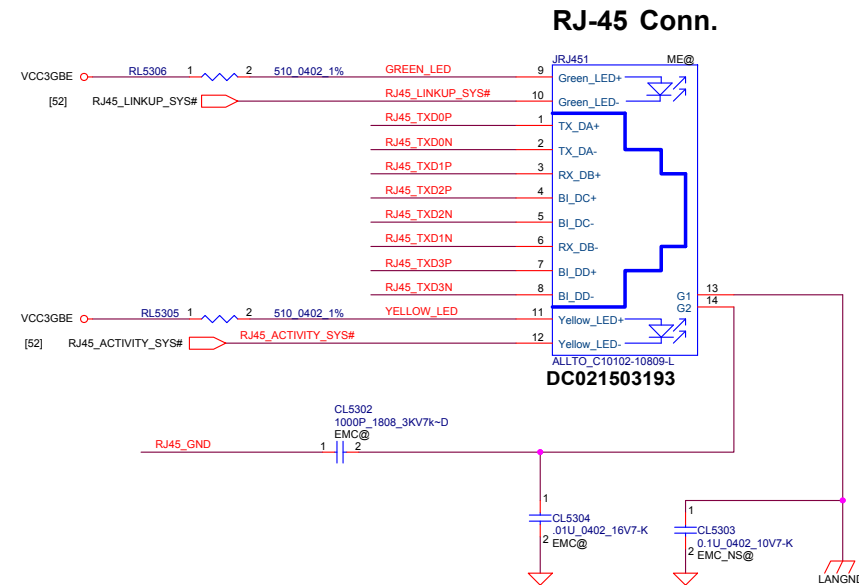
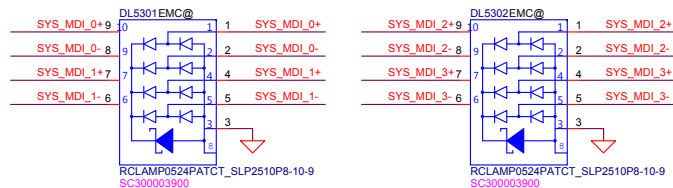
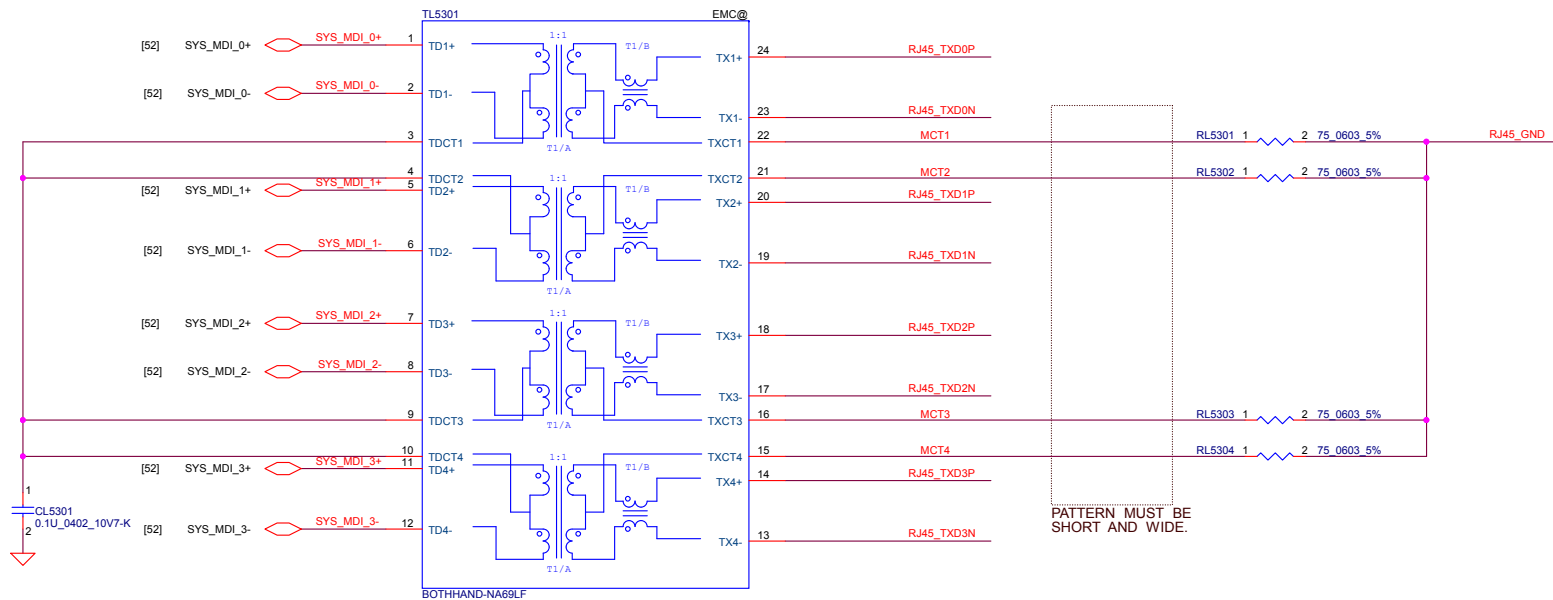
UL5101 GBE PHY

vPro Model	Non-vPro Model
WG1219LM	WG1219V
SA000073000	SA000072Z00

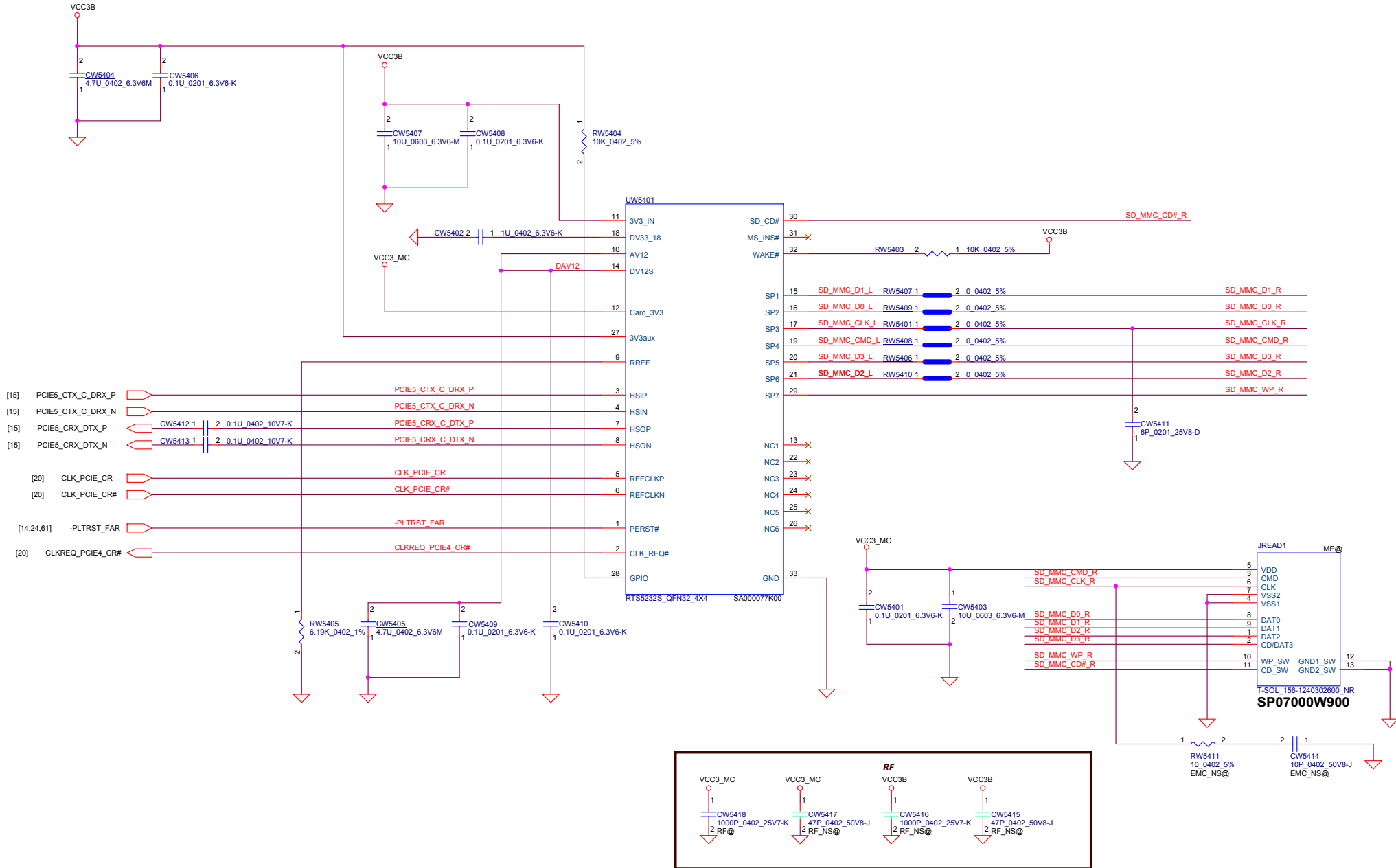


UL5201

Vendor	P/N	NOTE
Pericom	PI3L720ZHE, SA00003B20J	Main Source
ONsemi	NCN7201, SA00005TF00	2nd Source (FVT)



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APS G-Sensor

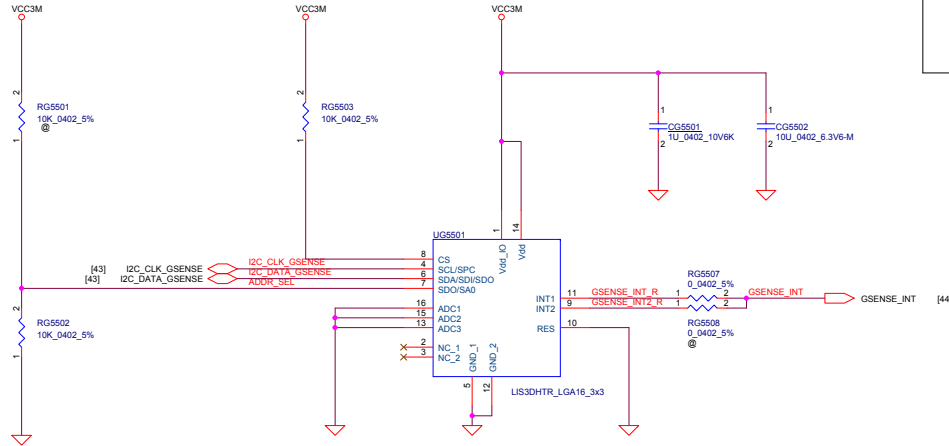
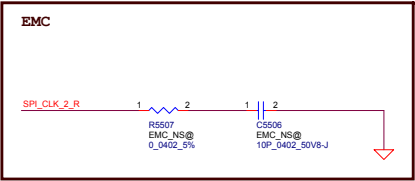
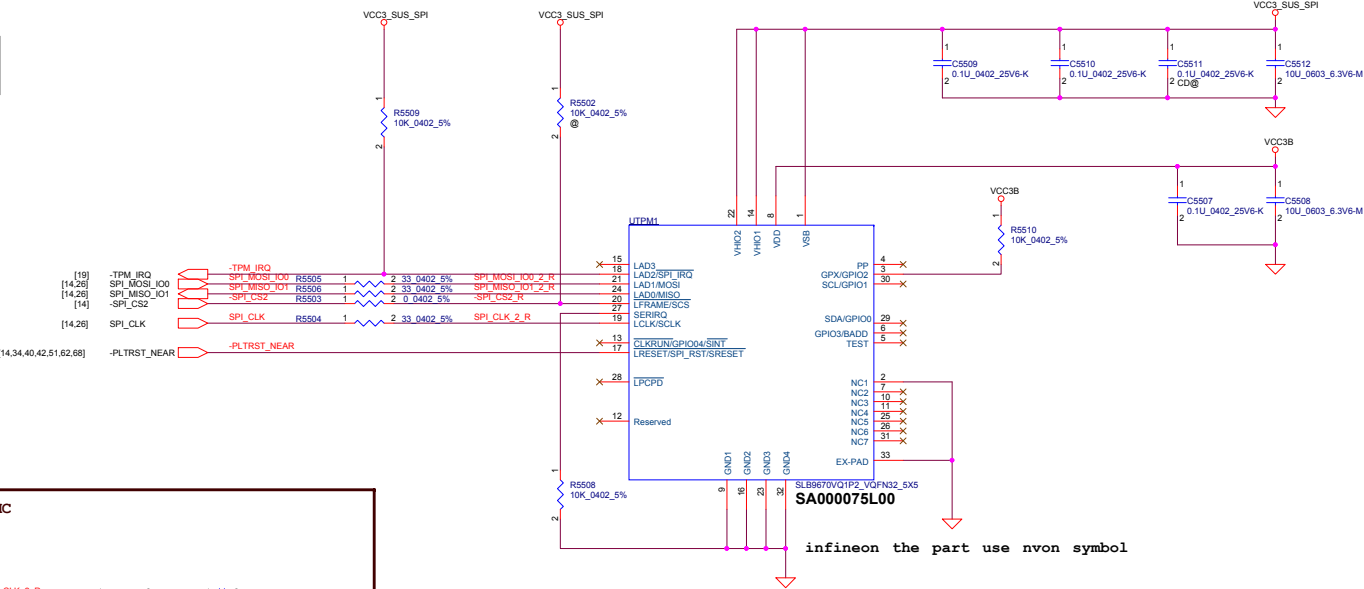


TABLE	
CS	Mode Selection
H	I2C Mode
L	SPI Mode

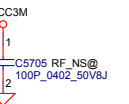
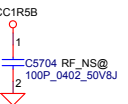
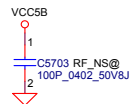
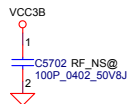
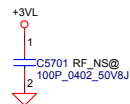
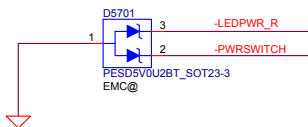
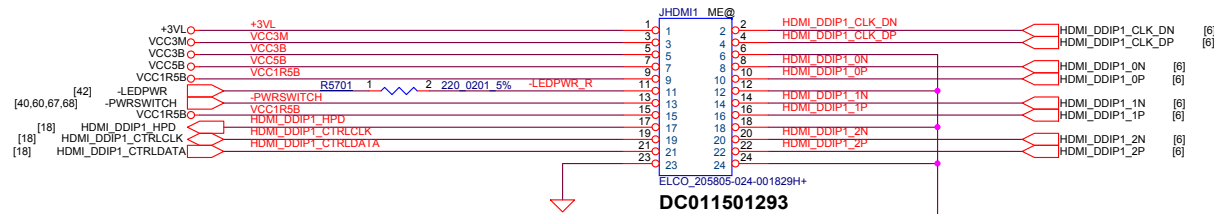
TPM IC

TPM Pin8	+3VS	VCC3_SUS_SPI
S3~S5 current	120uA	330uA



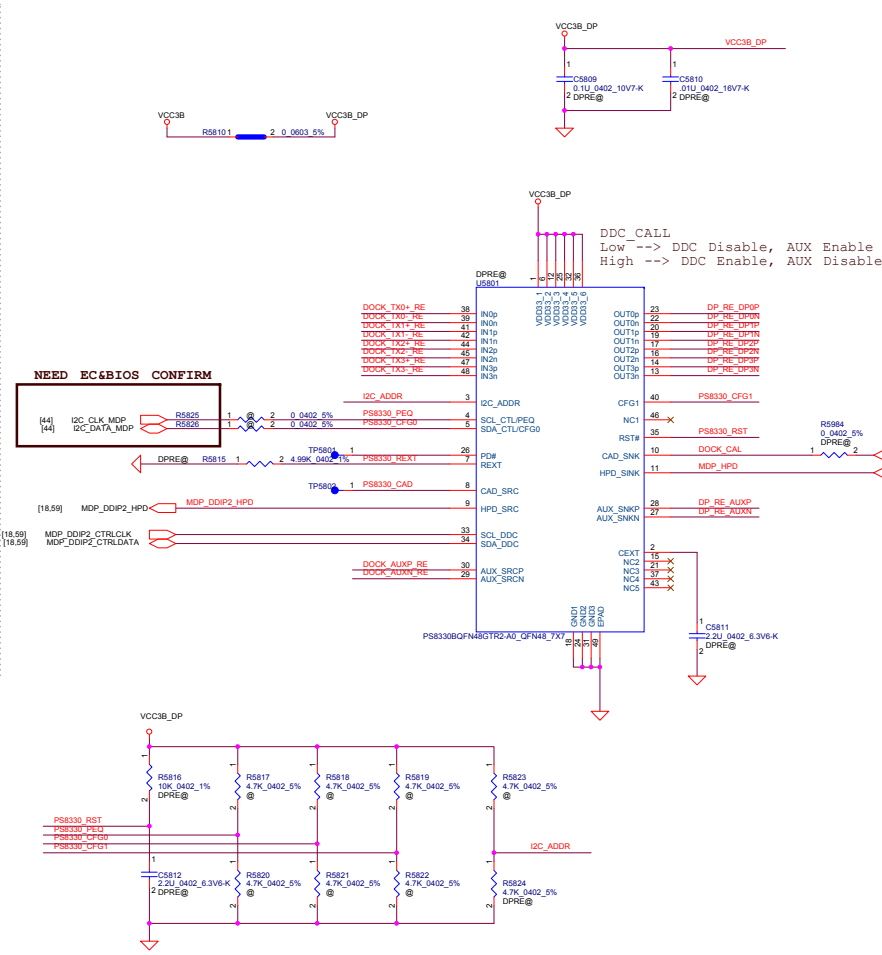
infineon the part use nvon symbol

M/B TO HDMI/B BTB CONN.

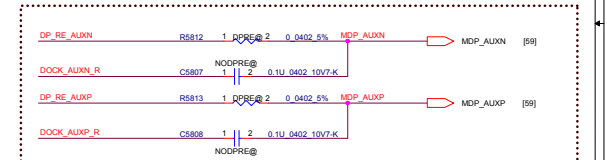




Cap.Pin1 and R.Pin1 Co-lay

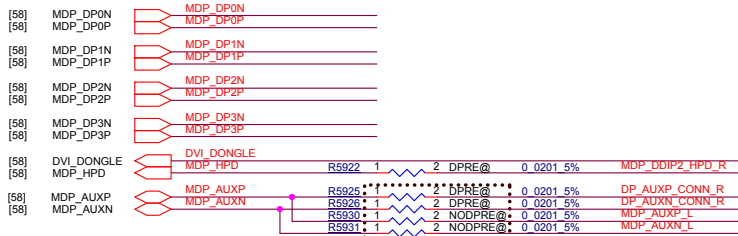


R.Pin2 and R.Pin2 Co-lay

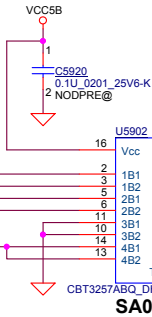
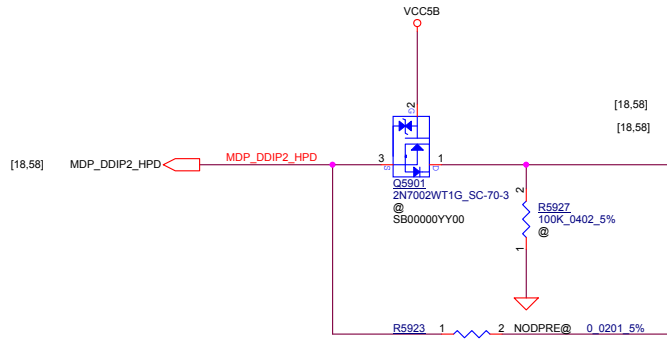


Cap.Pin2 and R.Pin2 Co-lay

DP AUX : From Repeater don't need cap, but PCH.

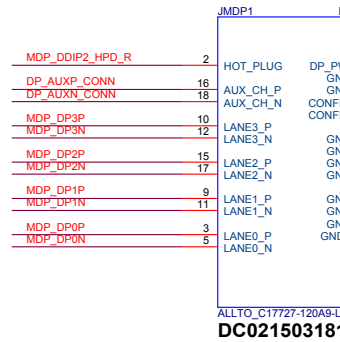


PIN1 COLAY

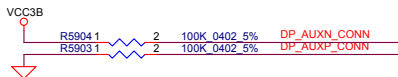


PIN2 COLAY

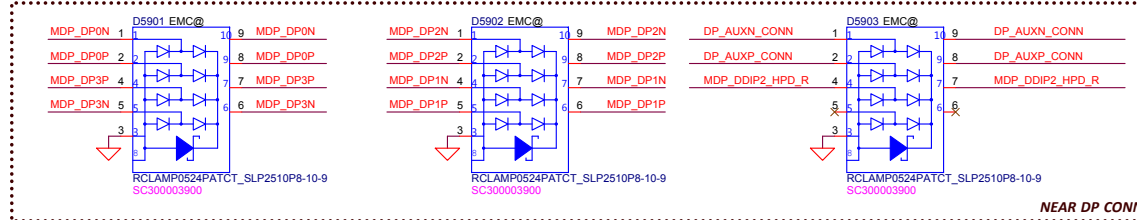
OE	S	Result
L	L	nA1 to nB1.
L	H	nA1 to nB2.
H	X	Switch off.



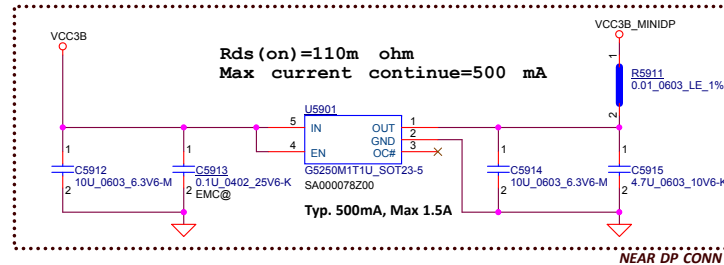
DC021503181



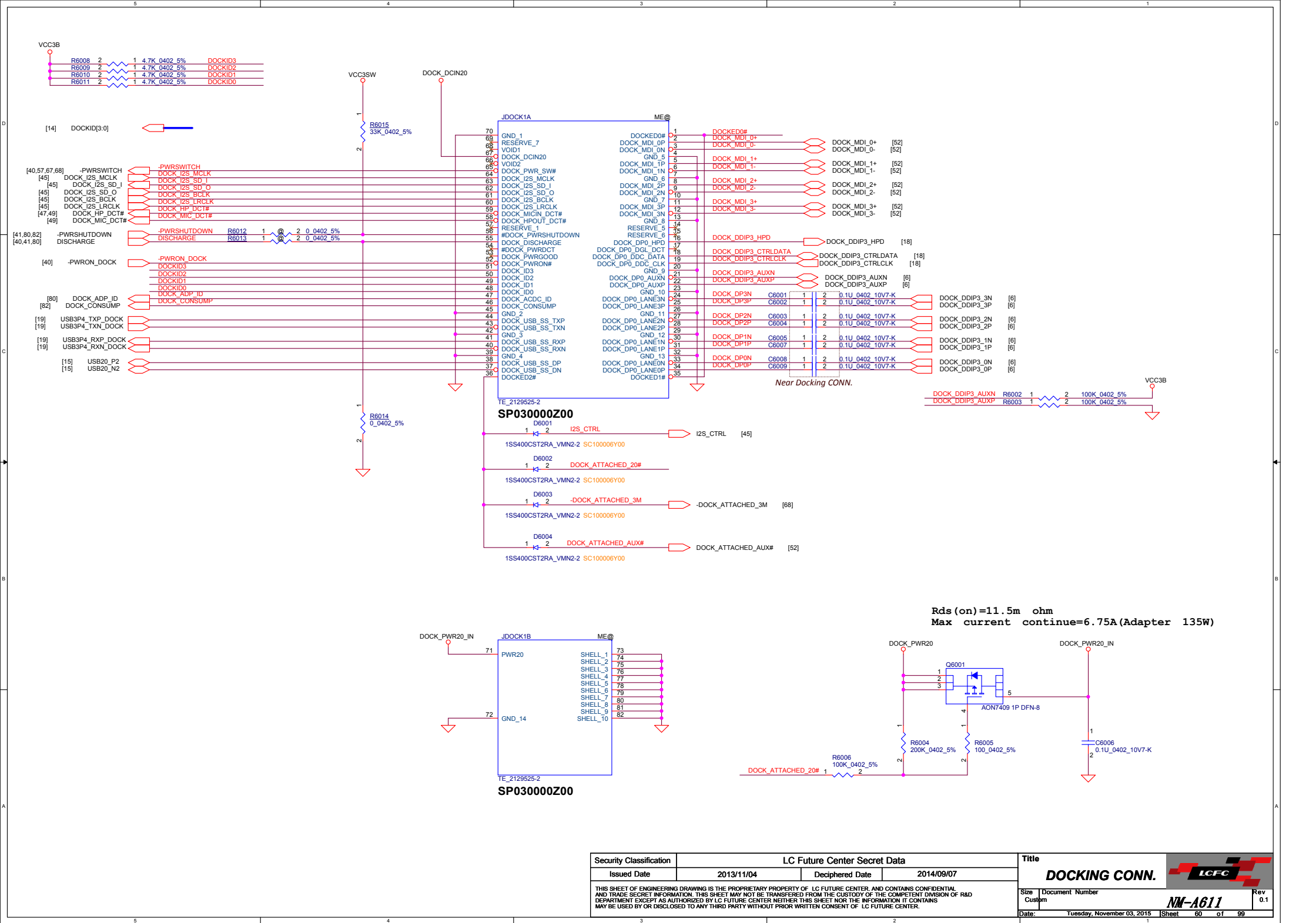
EMC (ESD soluti on)



NEAR DP CONN



NEAR DP CONN



AC coupling capacitors is not needed when use SATA-Express interface.

Input	Function
OE	Function
L	Disconnect
H	A port = B port

Security Classification: LC Future Center Secret Data

Issued Date: 2013/11/04

Deciphered Date: 2014/09/07

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Title: SATA HDD CONN.

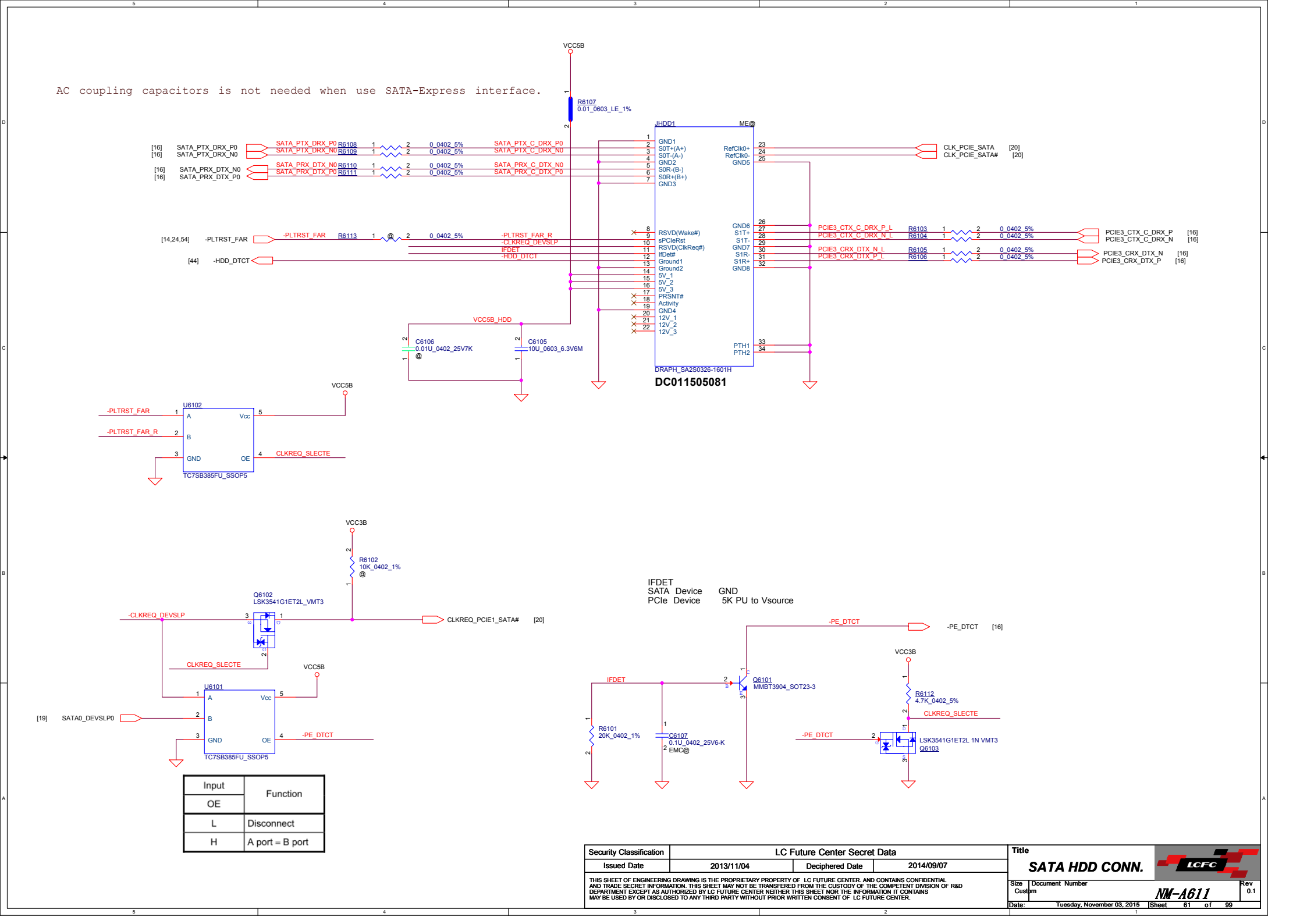
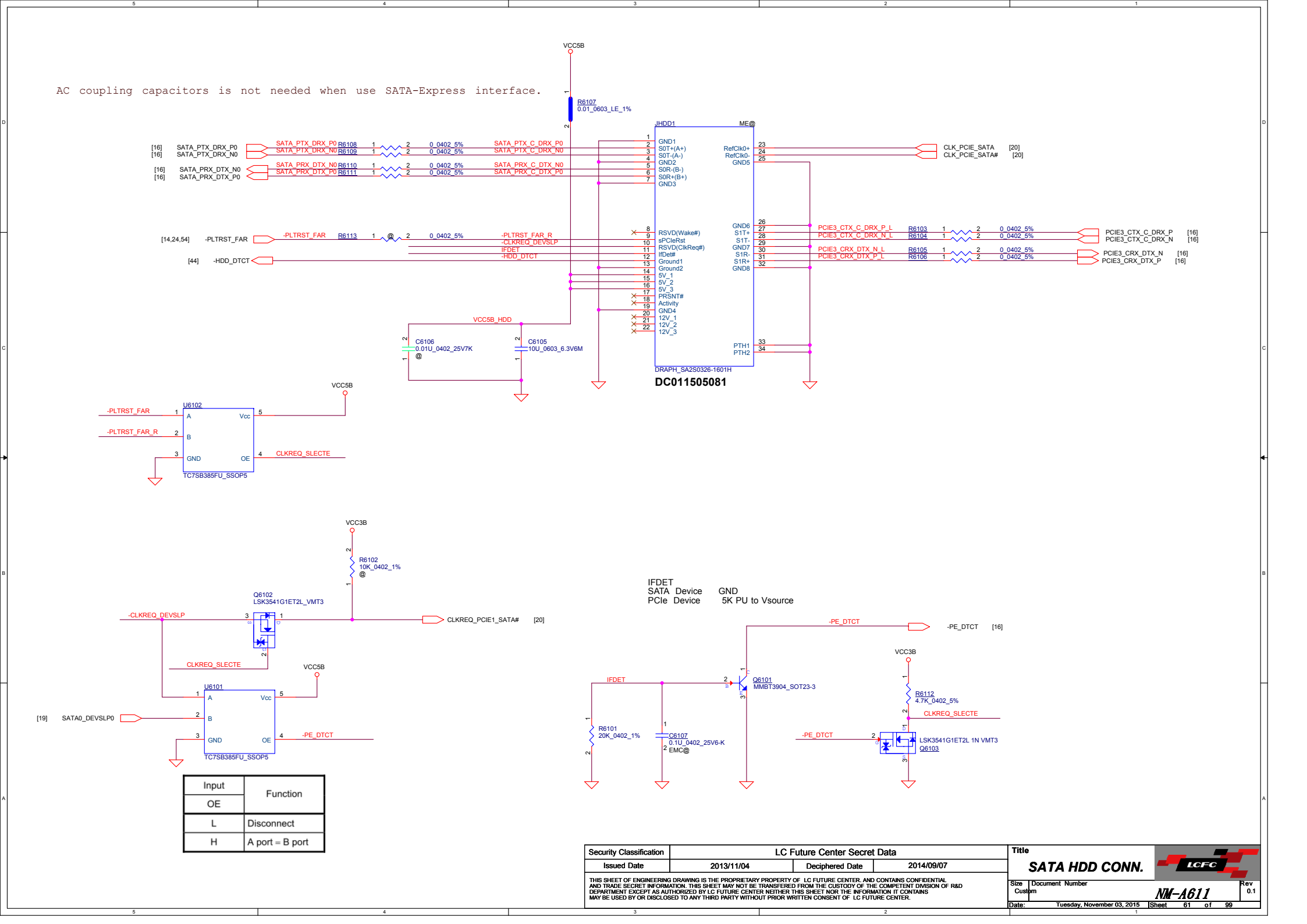
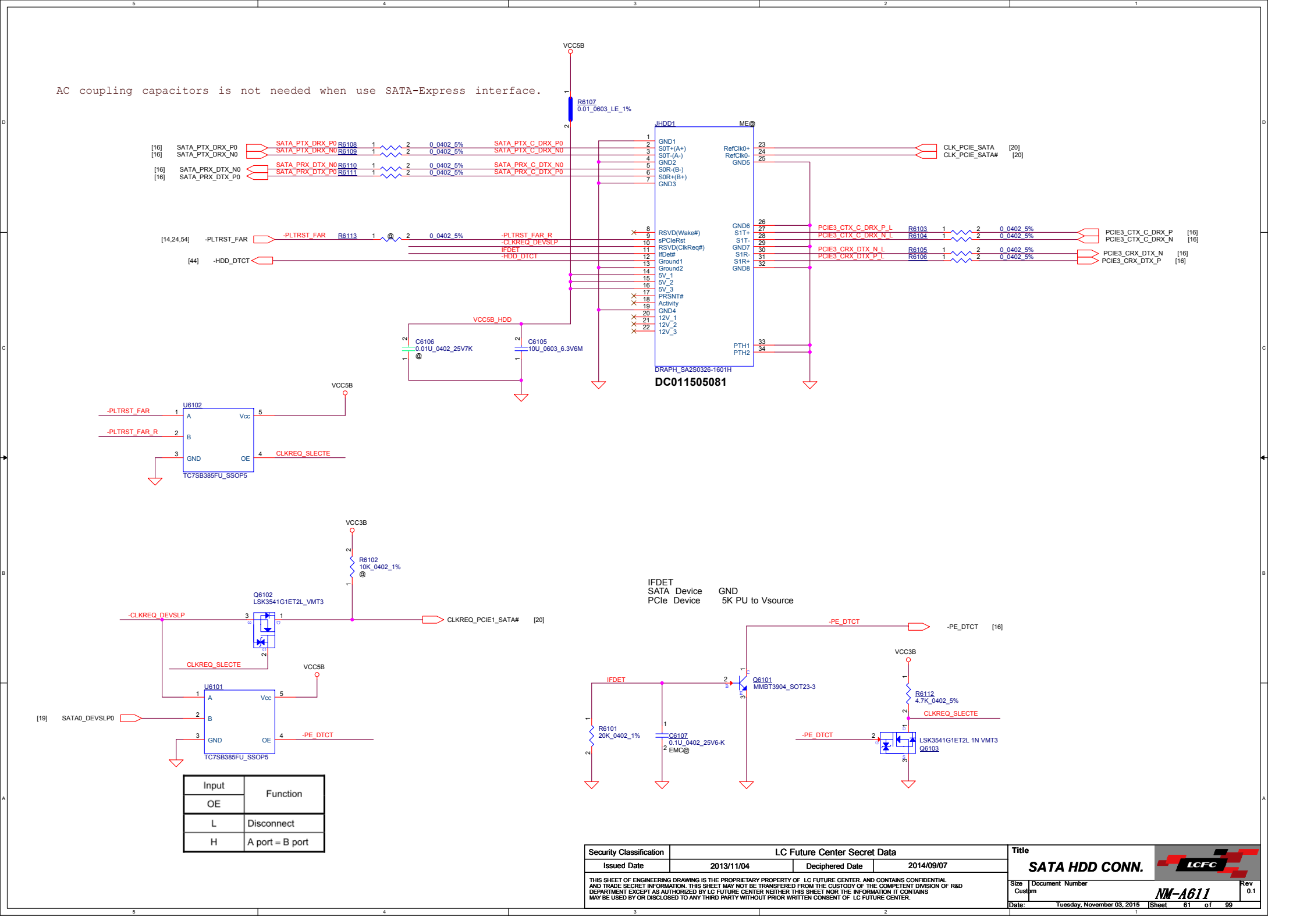
Size: Custom

Document Number: NM-A611

Date: Tuesday, November 03, 2015

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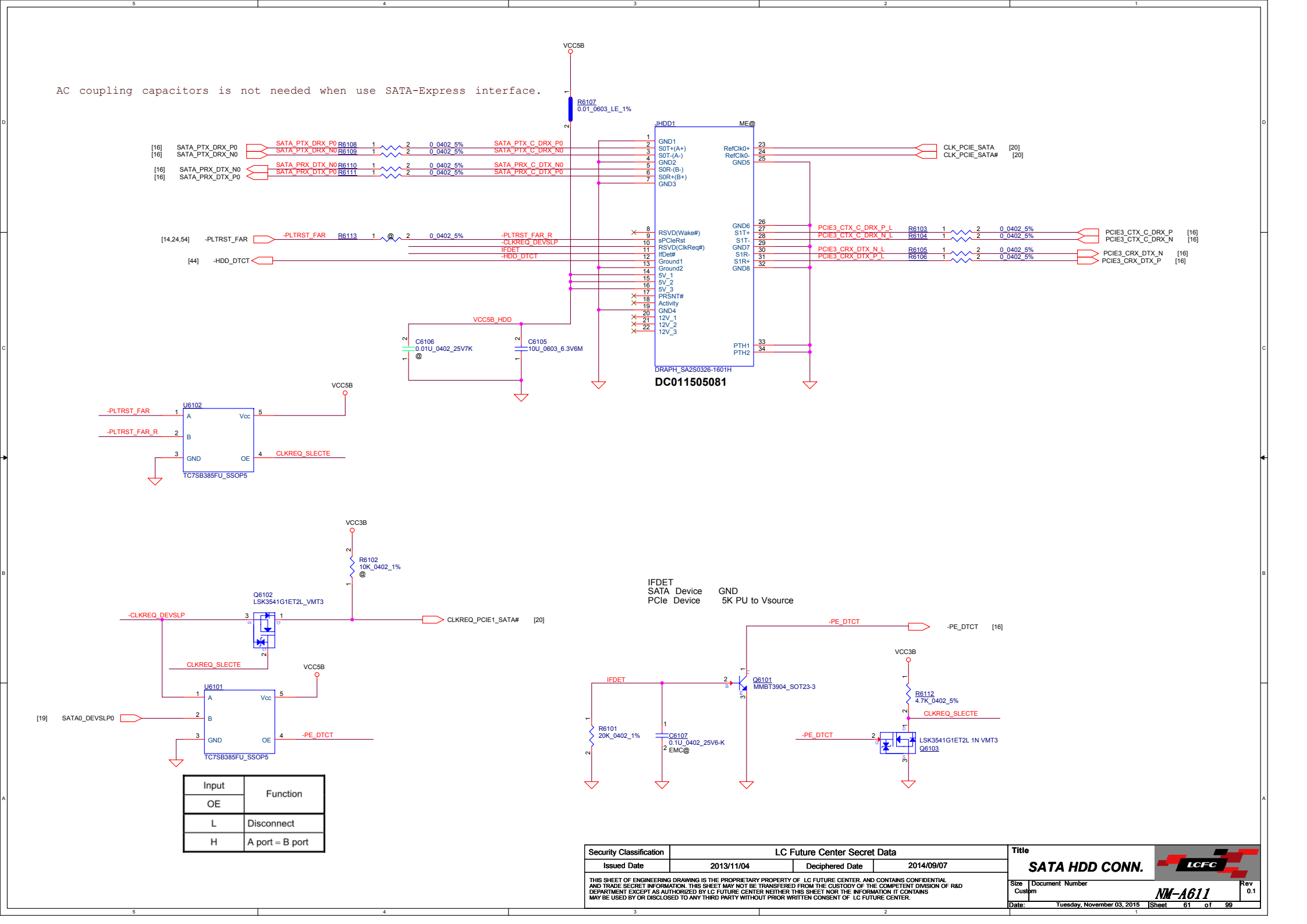
Rev: 0.1



AC coupling capacitors is not needed when use SATA-Express interface.

Input	Function
OE	
L	Disconnect
H	A port = B port

Security Classification	LC Future Center Secret Data		Title
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Date: Tuesday, November 03, 2015			Sheet 61 of 99



AC coupling capacitors is not needed when use SATA-Express interface.

Input	Function
OE	
L	Disconnect
H	A port = B port

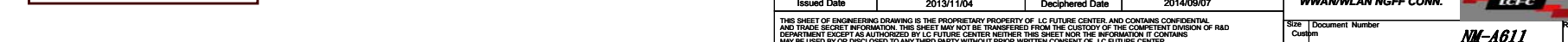
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AC coupling capacitors is not needed when use SATA-Express interface.

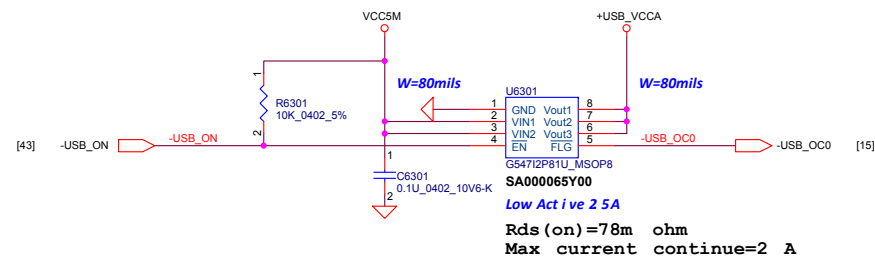
Input	Function
OE	
L	Disconnect
H	A port = B port

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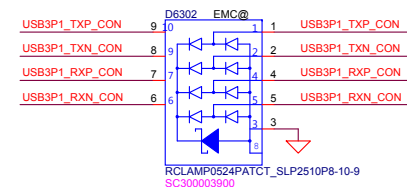
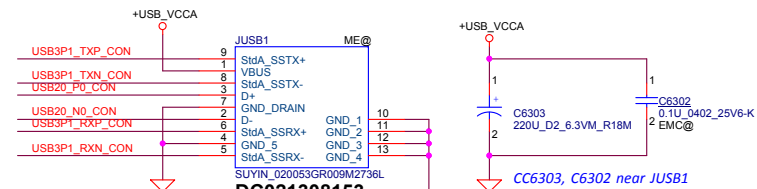
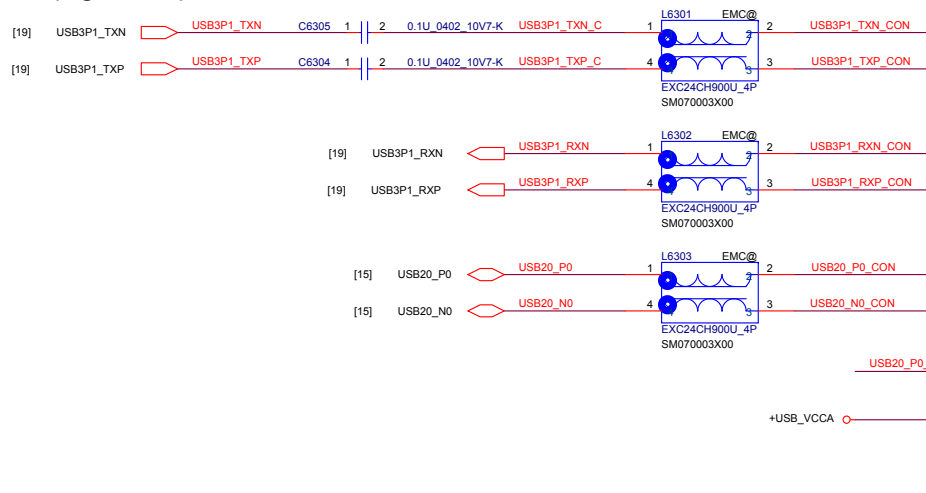
VCC3WLAN



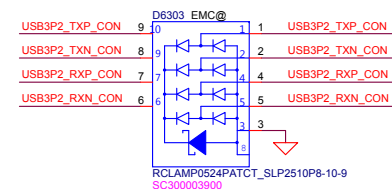
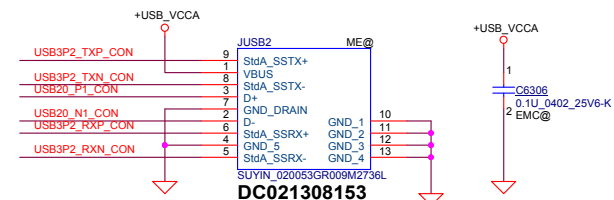
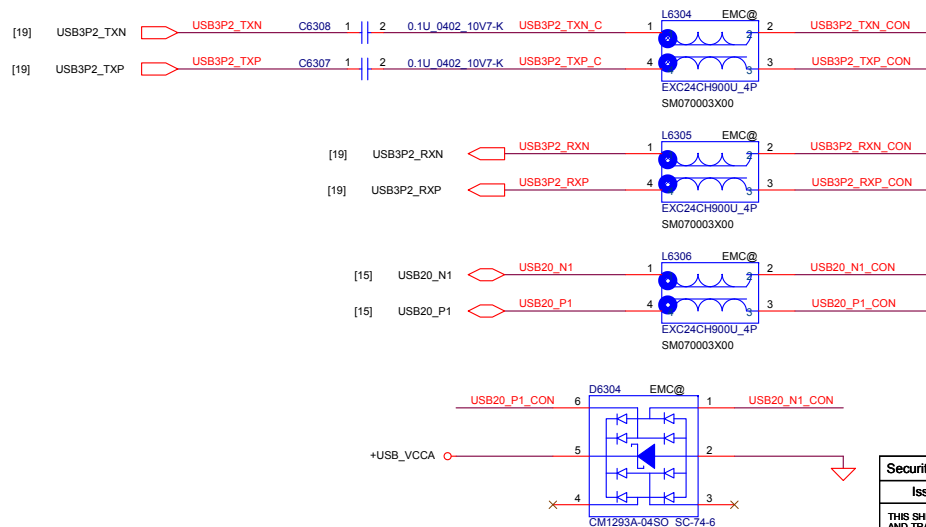
USB POWER SWITCH



On Board (Right-Front)



On Board (Right-Back)



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				Date:	Tuesday, November 03, 2015	Sheet 63 of 99 Rev 0.1

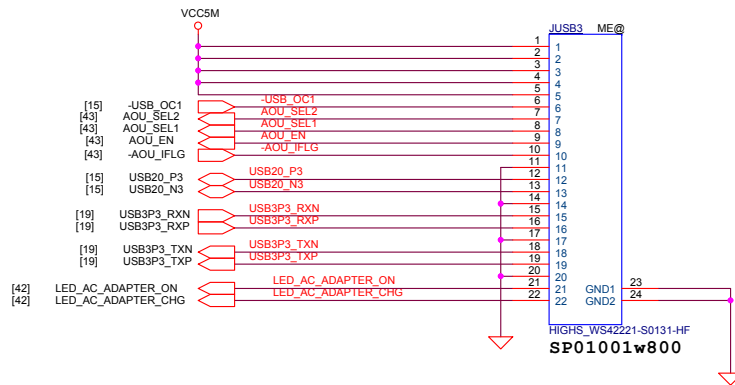
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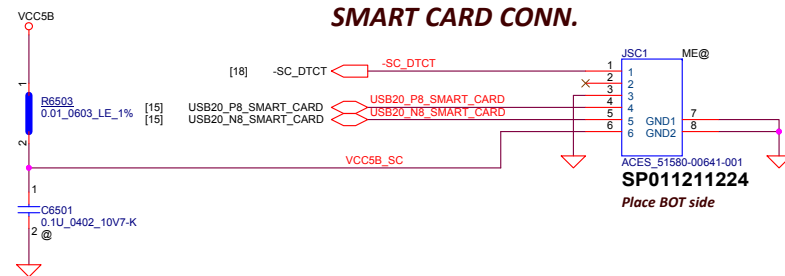
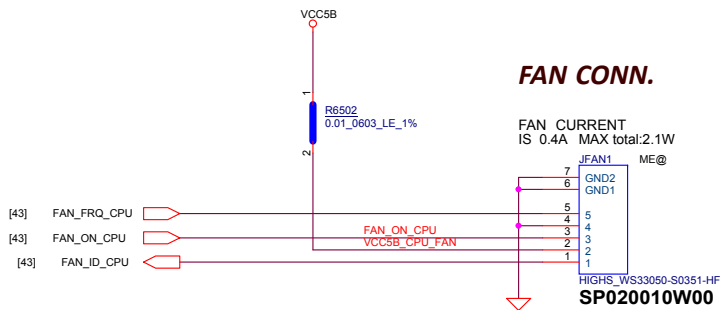
MB PIN number	MB PIN name	SB board pin name	SB PIN number
pin1~5	VCC5M	VCC5M	pin1~5
pin6	-USB_OC1	-USB_OC1	pin6
pin7	AOU_SEL2	AOU_SEL2	pin7
pin8	AOU_SEL1	AOU_SEL1	pin8
pin9	AOU_EN	AOU_EN	pin9
pin10	-AOU_IFLG	-AOU_IFLG	pin10
pin11	GND	GND	pin11
pin12	USB20_P3	USB20_P3	pin12
pin13	USB20_N3	USB20_N3	pin13
pin14	GND	GND	pin14
pin15	USB3P3_RXN	USB3P3_RXN	pin19
pin16	USB3P3_RXP	USB3P3_RXP	pin18
pin17	GND	GND	pin17
pin18	USB3P3_TXN	USB3P3_TXN	pin16
pin19	USB3P3_TXP	USB3P3_TXP	pin15
pin20	GND	GND	pin20
pin21	LED_AC_ADAPTER_ON	LED_AC_ADAPTER_ON	pin21
pin22	LED_AC_ADAPTER_CHG	LED_AC_ADAPTER_CHG	pin22

*

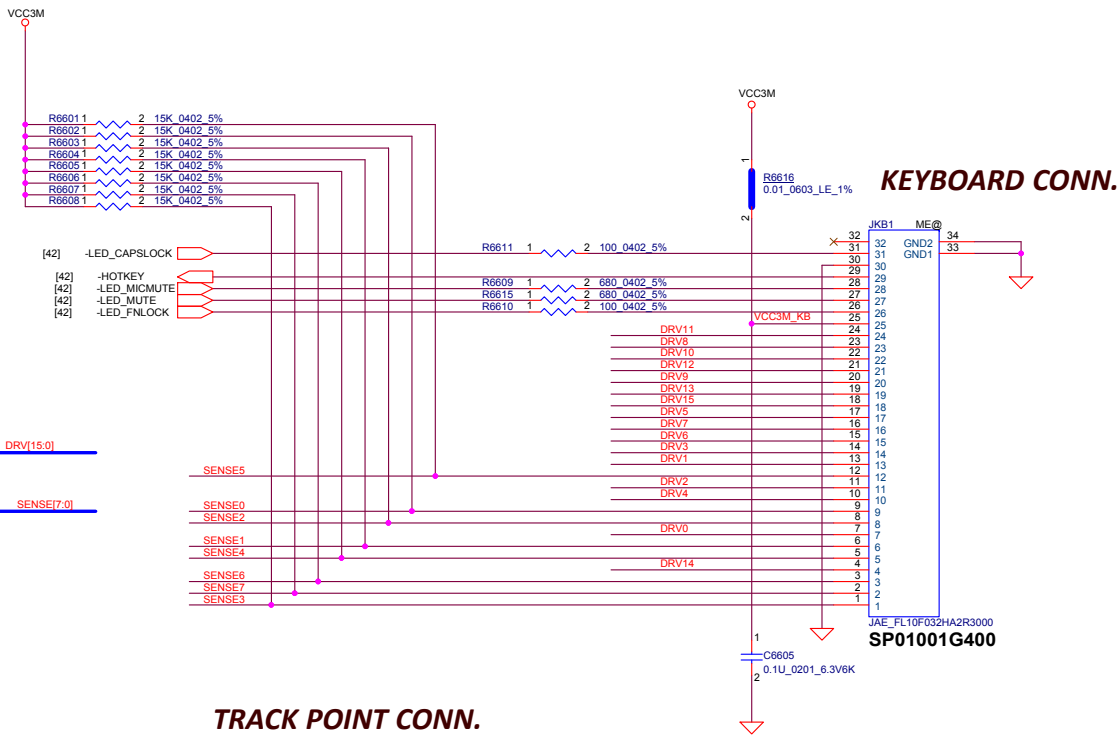
USB board and MB board is wire to board connector.
Due to USB board layout issue so pin define can* meet MB

USB LEFT PORT

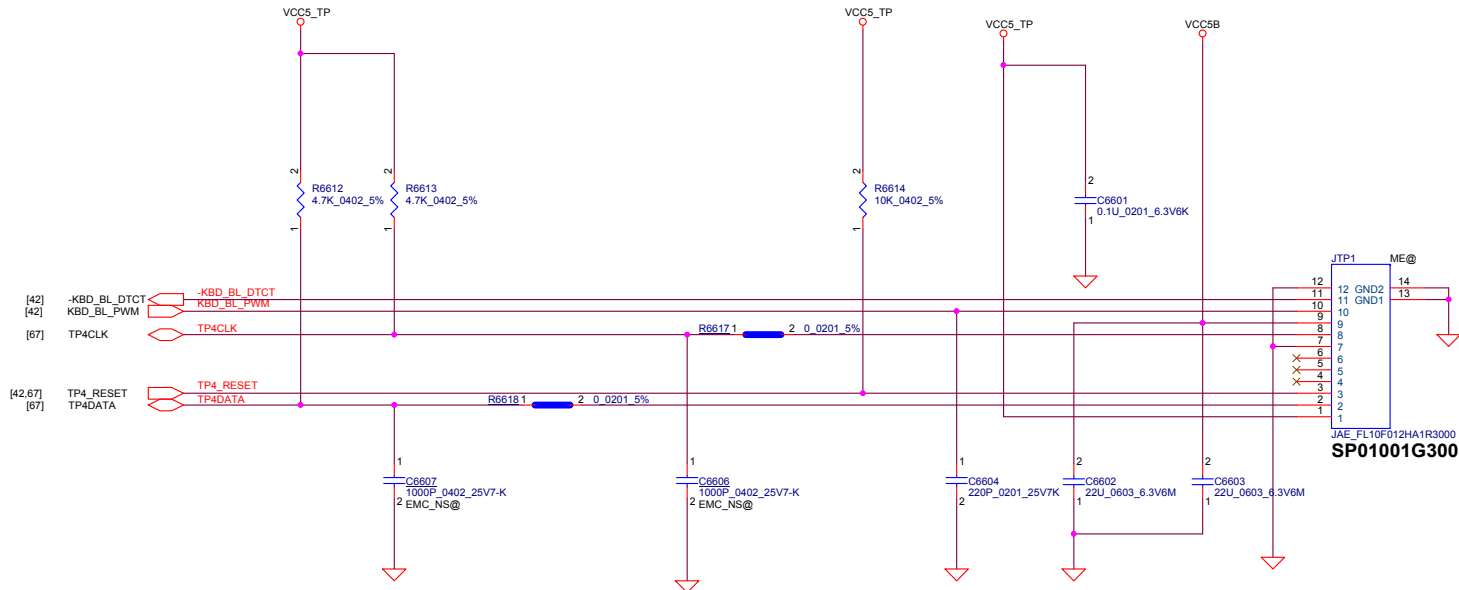




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				Date:	Tuesday, November 03, 2015
				Sheet	65 of 99
				Rev	0.1



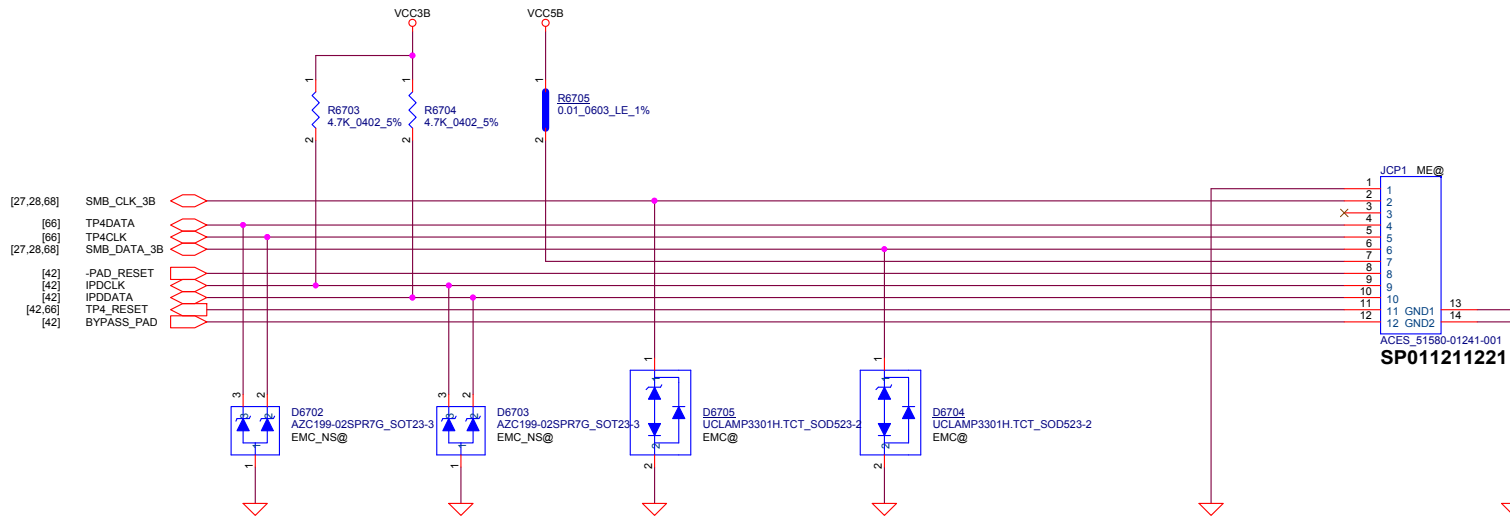
TRACK POINT CONN.



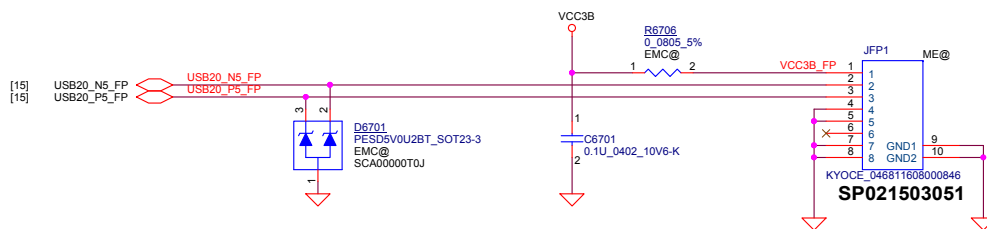
Security Classification		LC Future Center Secret Data		Title			Rev
Issued Date	2013/11/04	Deciphered Date	2014/09/07	KEYBOARD/TRACK POINT			
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				Date:	Tuesday, November 03, 2015	Sheet	66 of 99

NM-A611

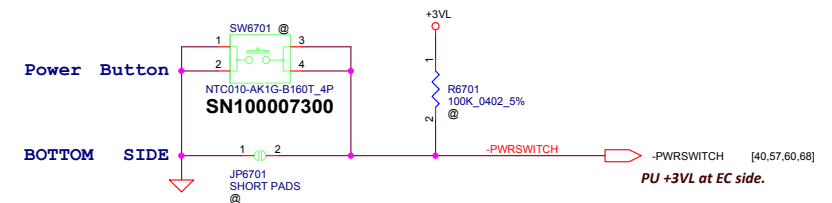
Click Pad



FingerPrint CONN.

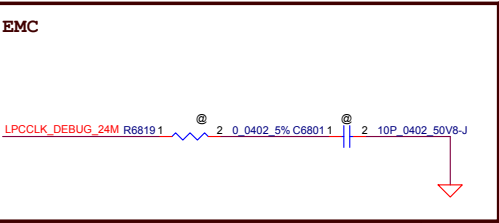
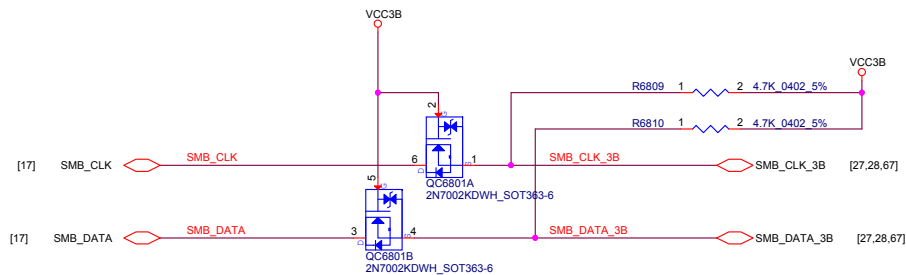
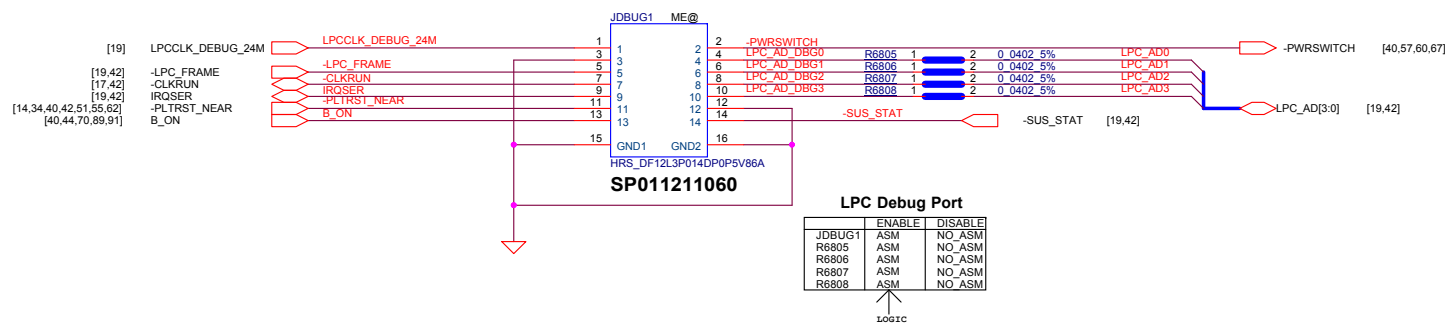
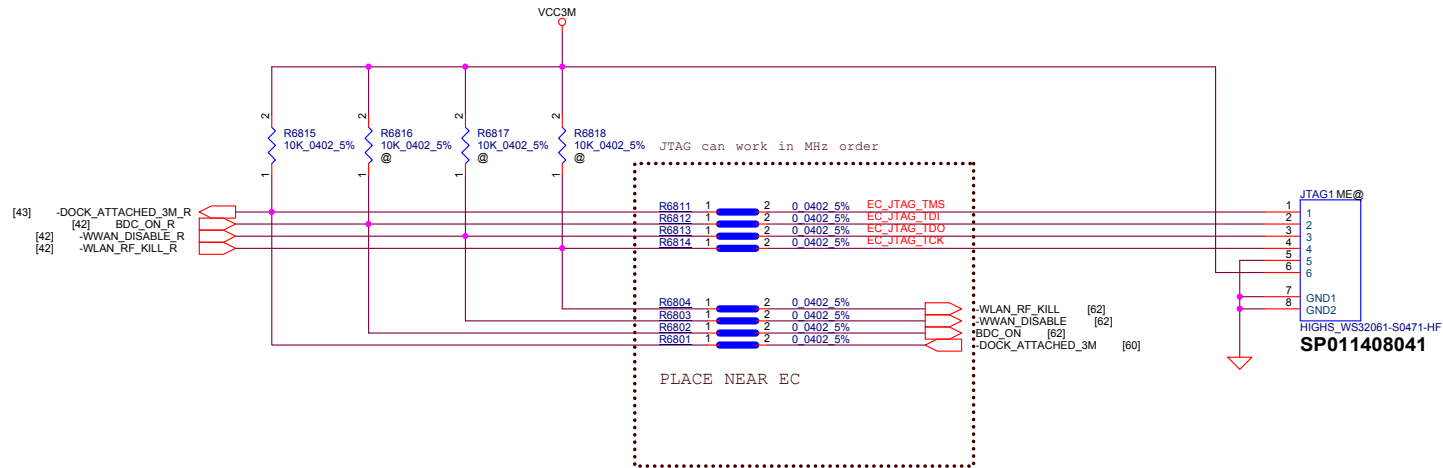


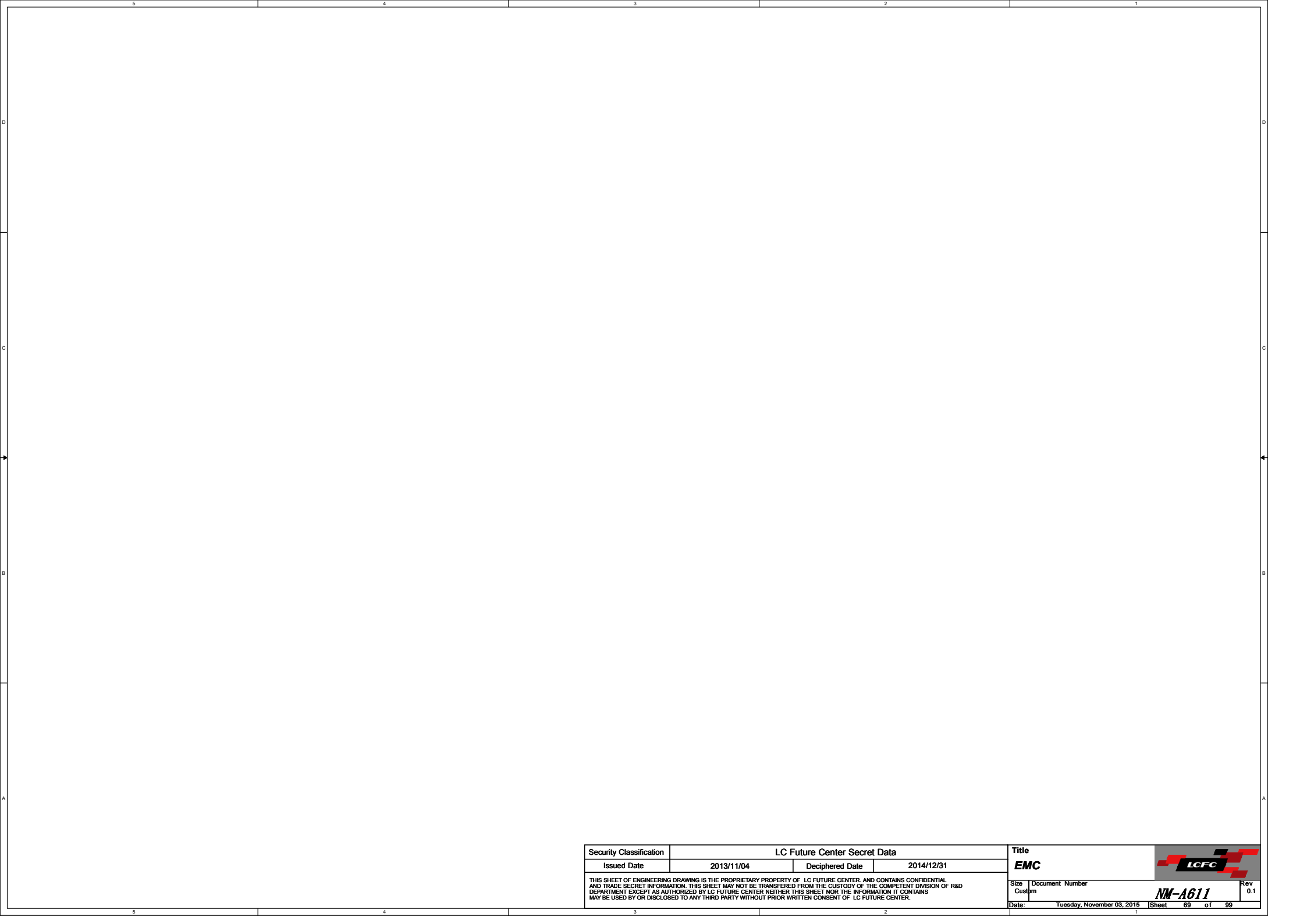
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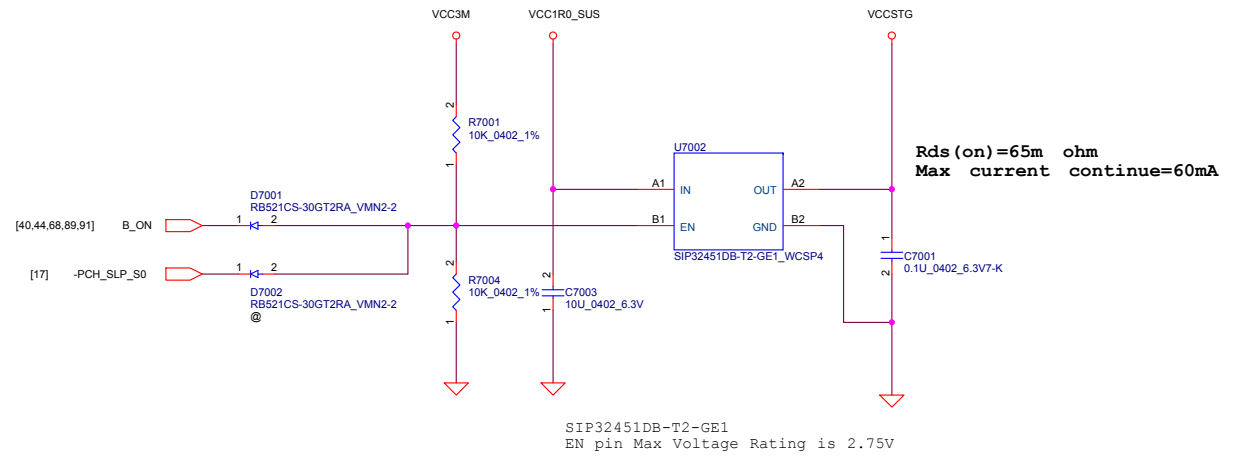
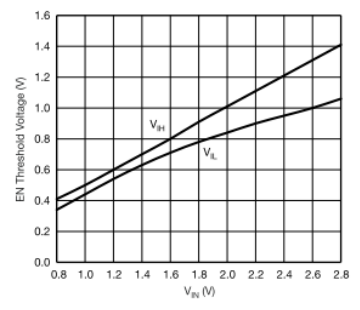
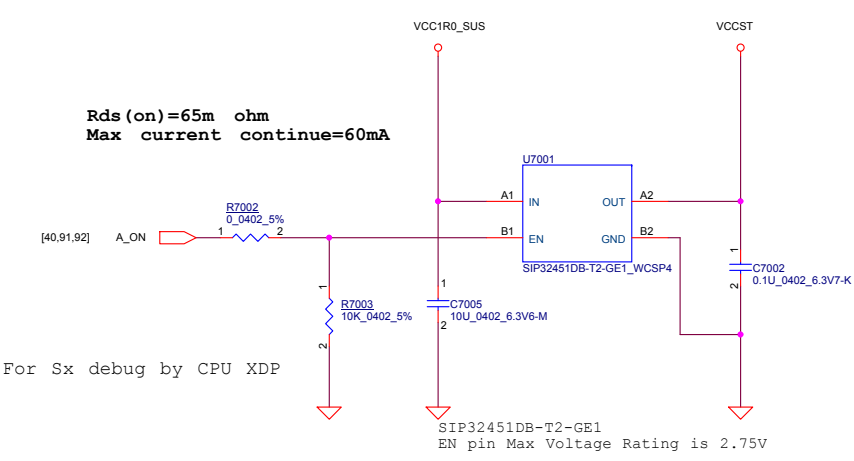
Security Classification			
LC Future Center Secret Data			
Issued Date	2013/11/04	Deciphered Date	2014/09/07
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Title		Rev	
Click Pad/FPR/PBTN		0.1	
Size	Document Number	NM-A611	
Custom			
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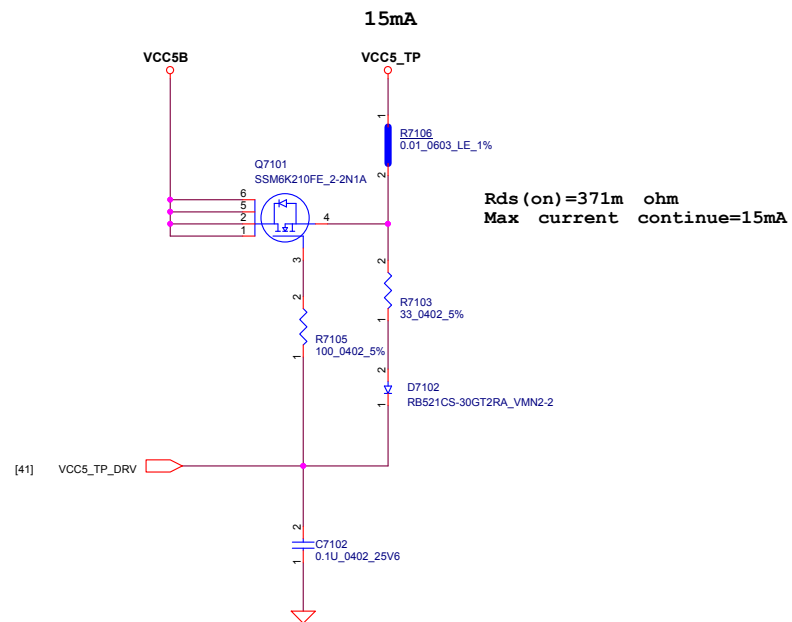
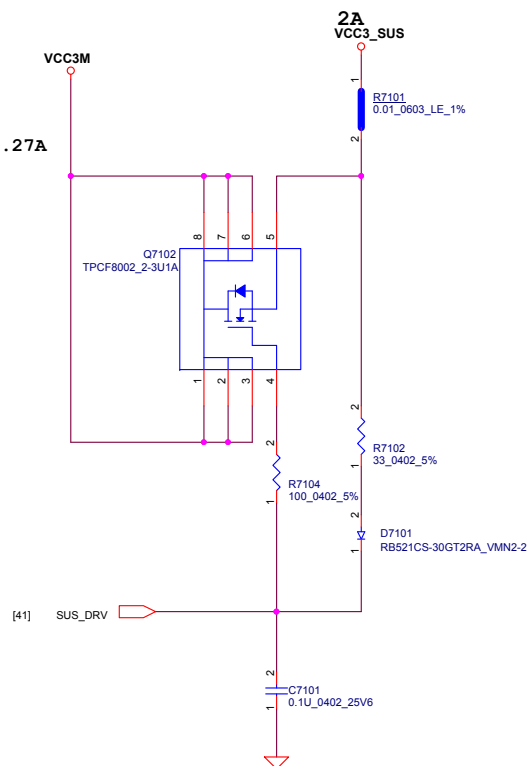


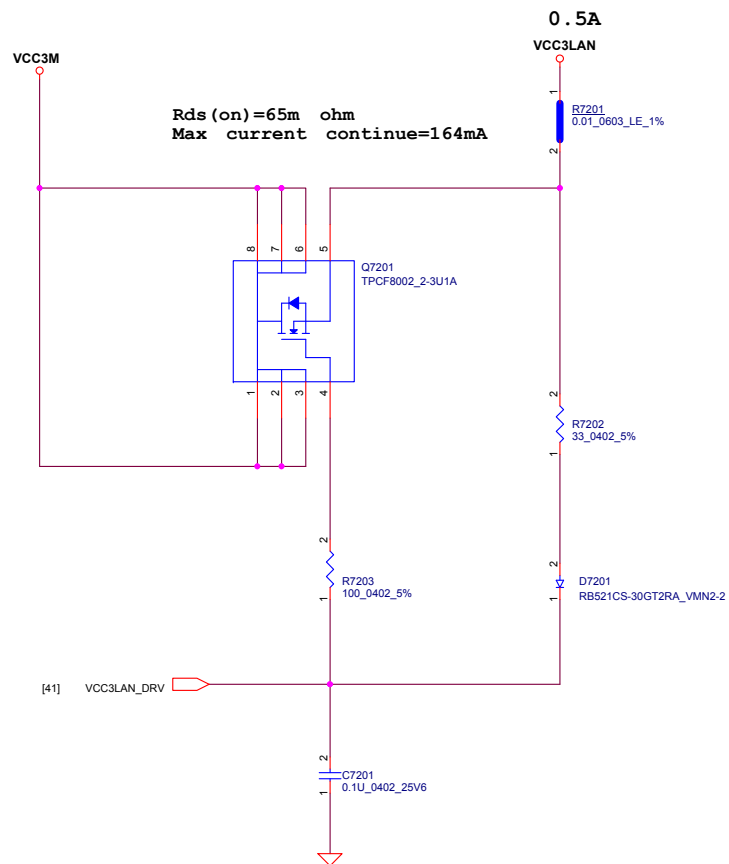


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Issued Date		2013/11/04		Deciphered Date		2014/12/31			
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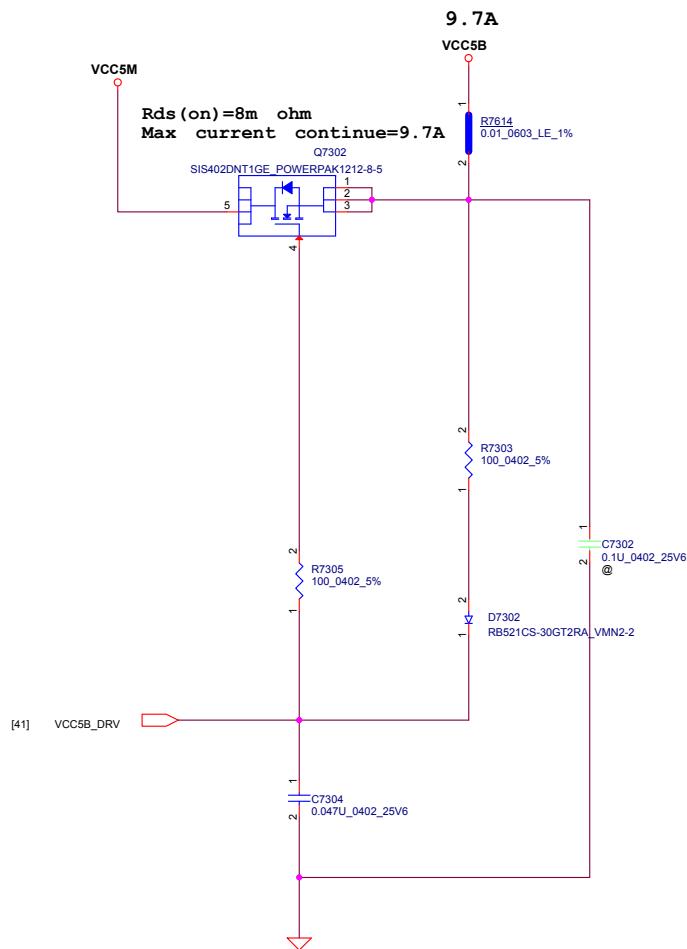
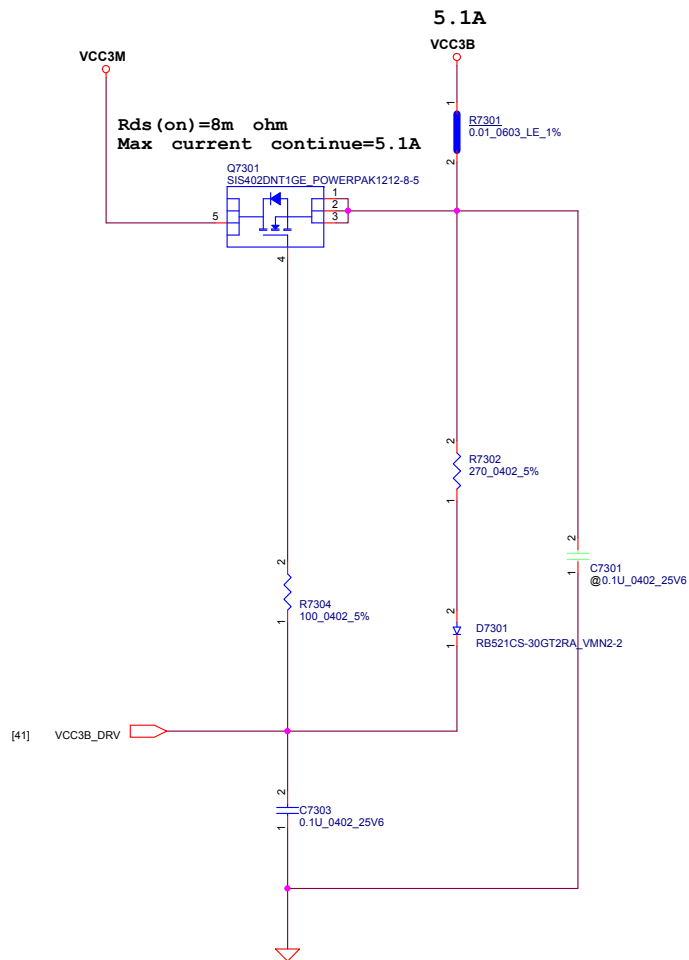


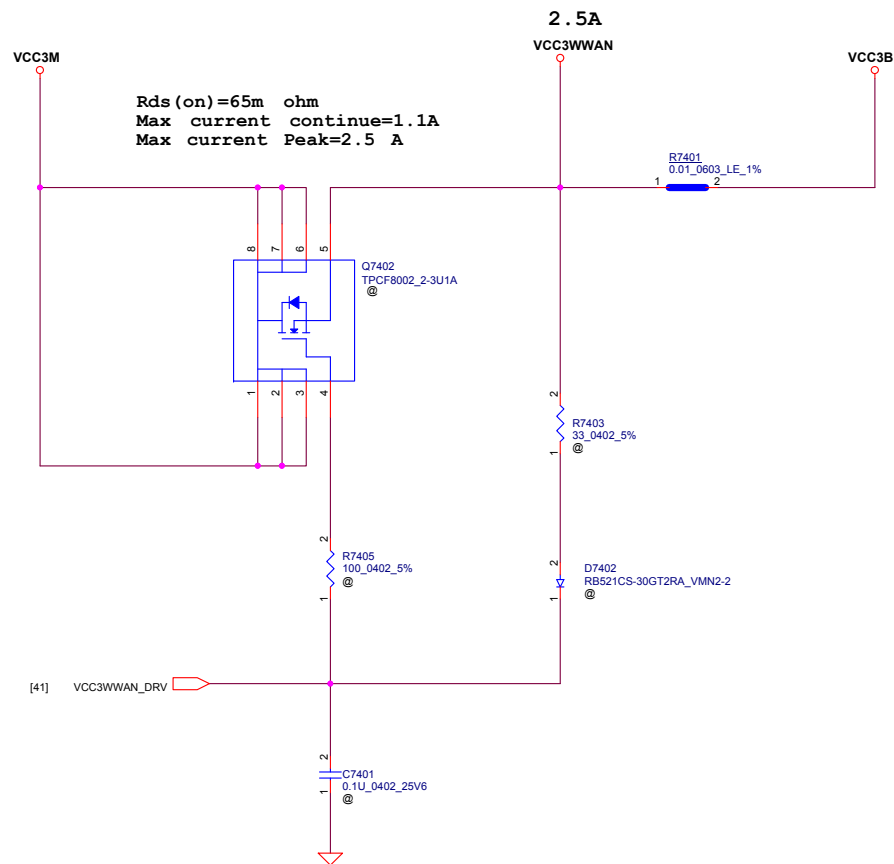
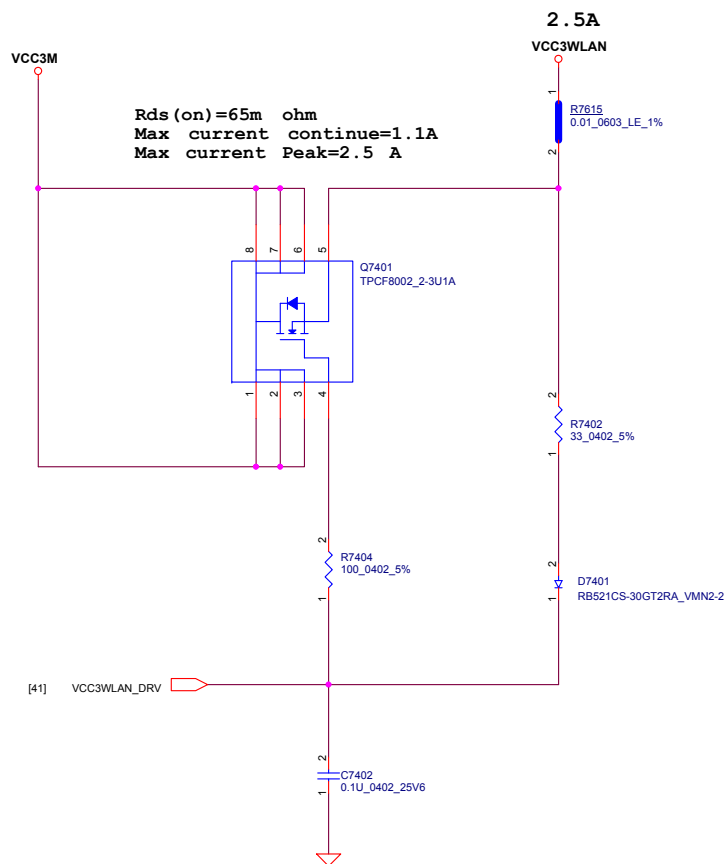
Rds (on)=65m ohm
Max current continue=4.27A

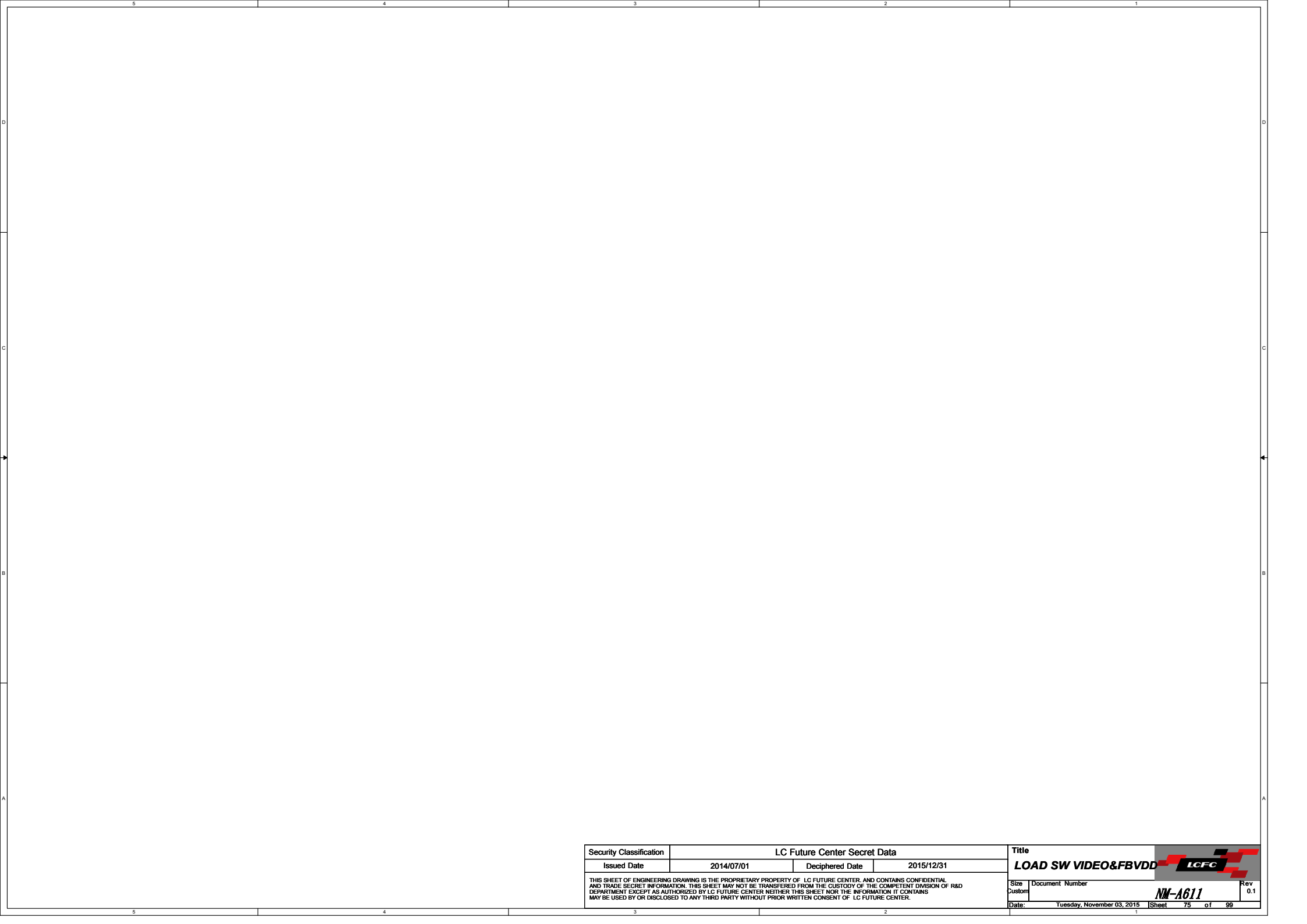




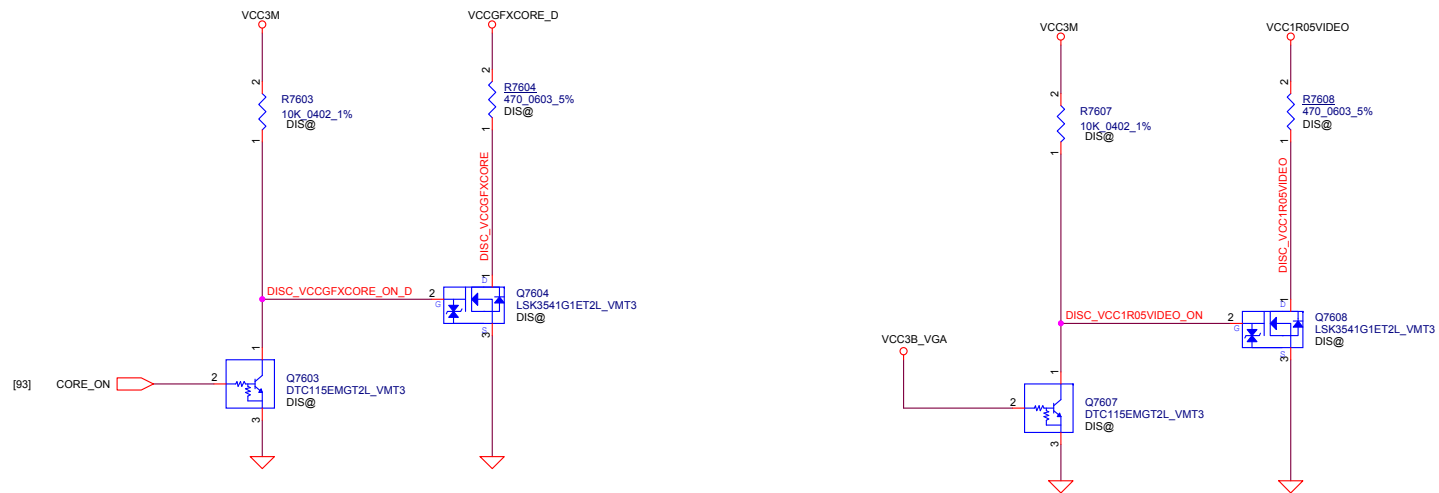
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Issued Date	2014/07/01	Deciphered Date	2015/12/31	LOAD SW LAN			
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				Custom		0.1	
				Date:	Tuesday, November 03, 2015	Sheet 72 of 99	



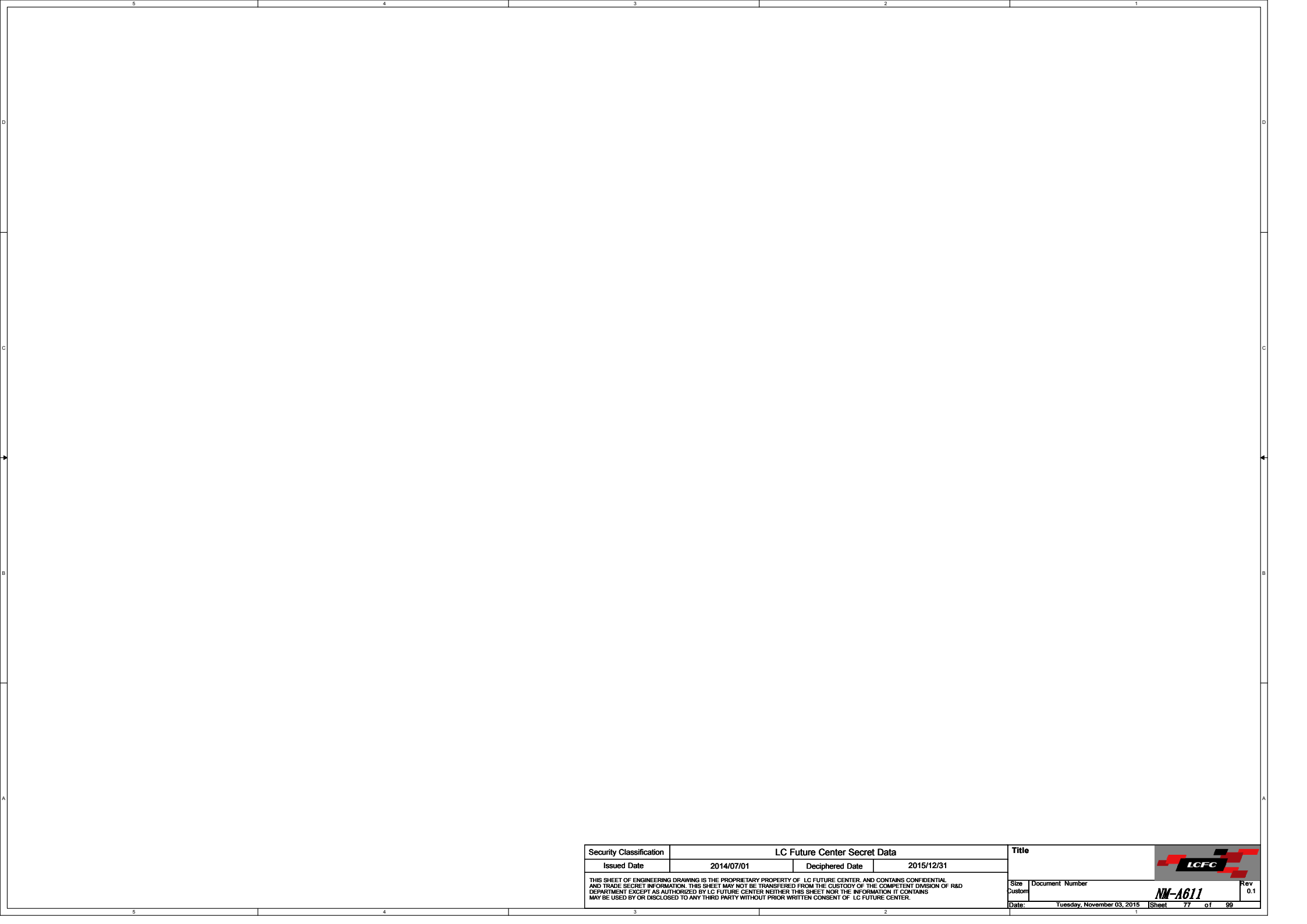




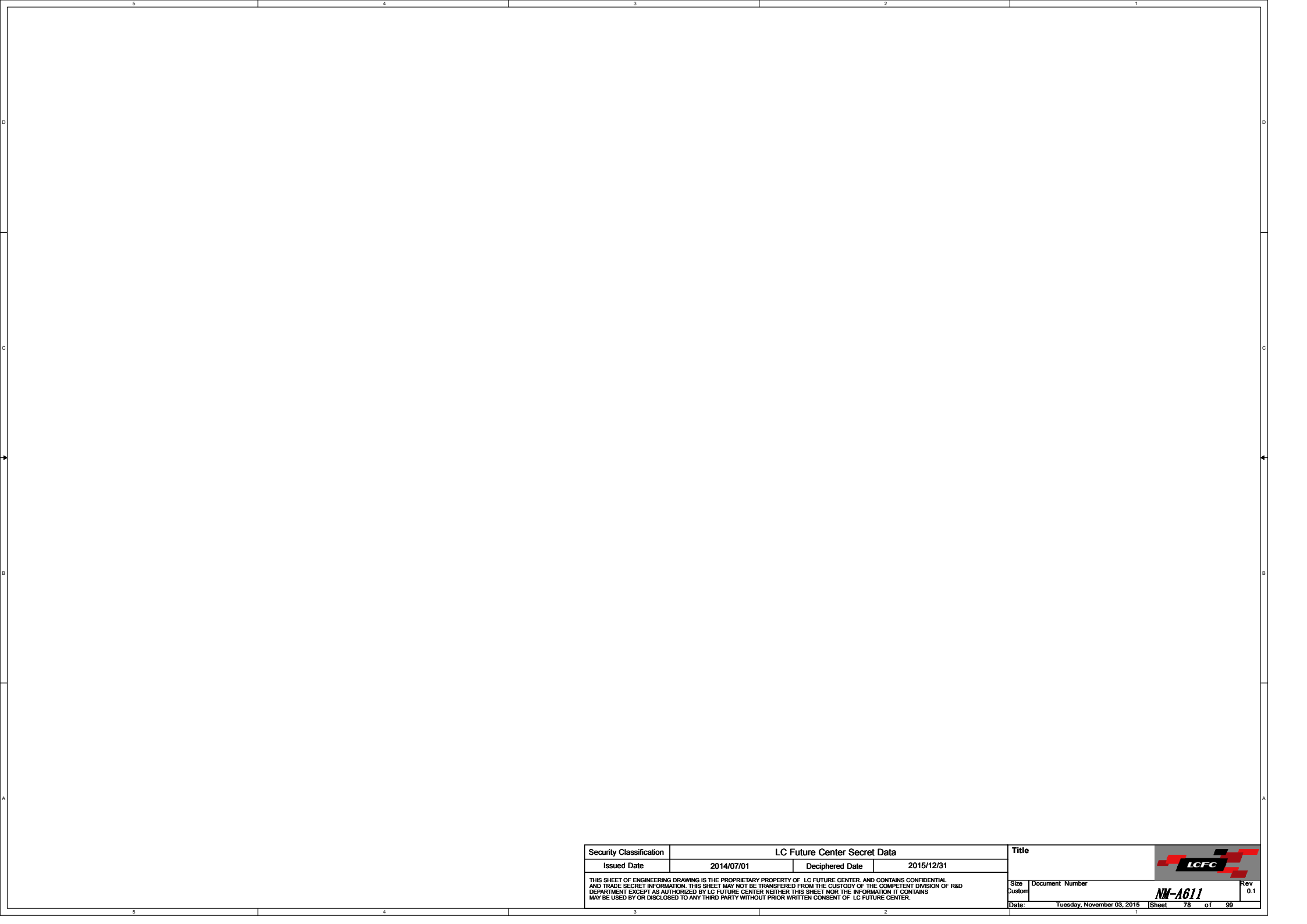
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/07/01	Deciphered Date	2015/12/31	LOAD SW VIDEO&FBVDD	
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Issued Date	2014/07/01	Deciphered Date	2015/12/31	DISCHARGE CIRCUIT VIDEO	
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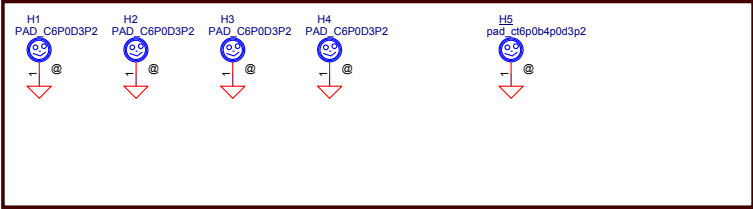
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Issued Date	2014/07/01	Deciphered Date	2015/12/31				
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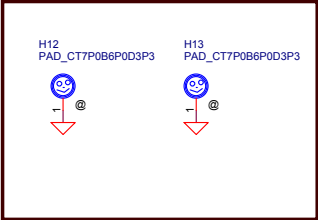
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Issued Date	2014/07/01	Deciphered Date	2015/12/31				
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Screw Hole

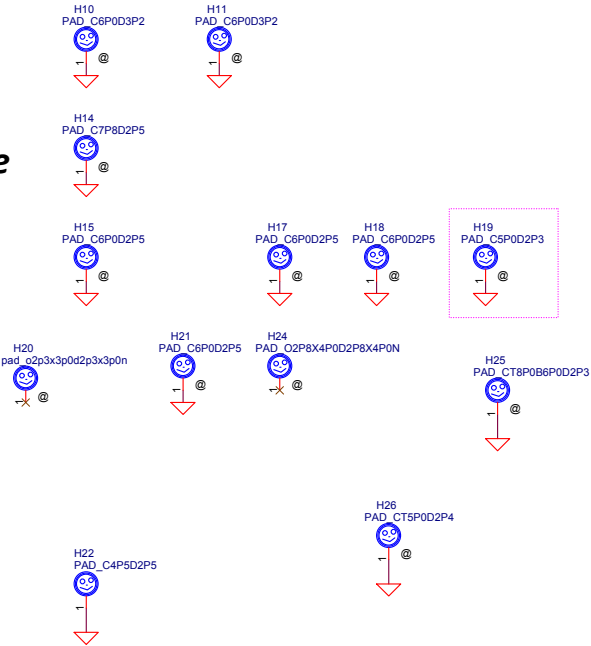
For CPU and GPU



AUDIO SCREW



For ME GND hole

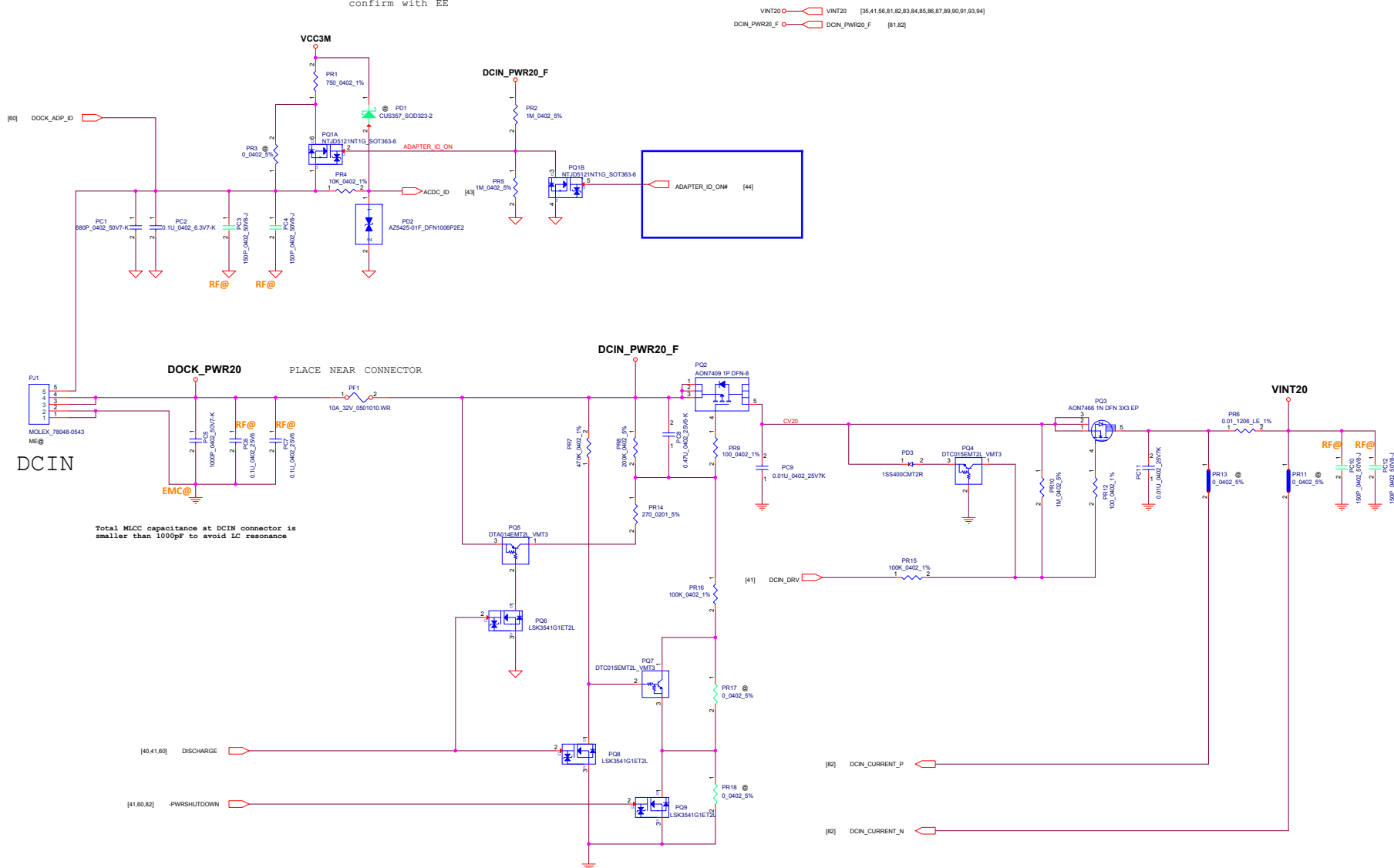


For ME hole

PCB Fedical Mark PAD



confirm with EE

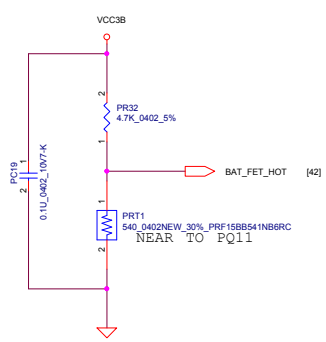
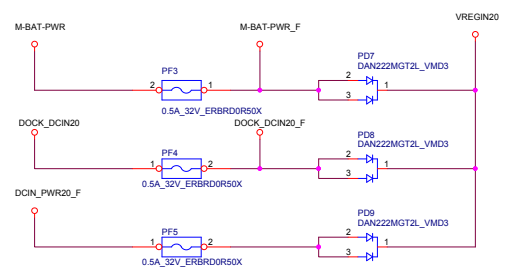
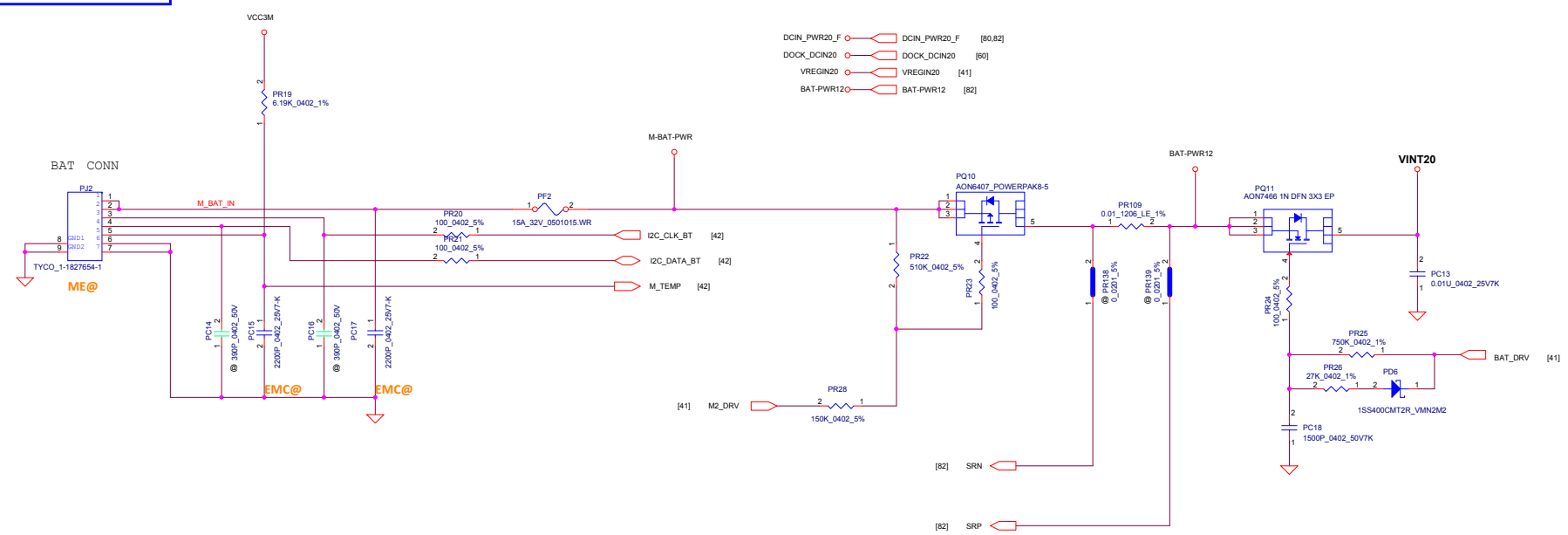


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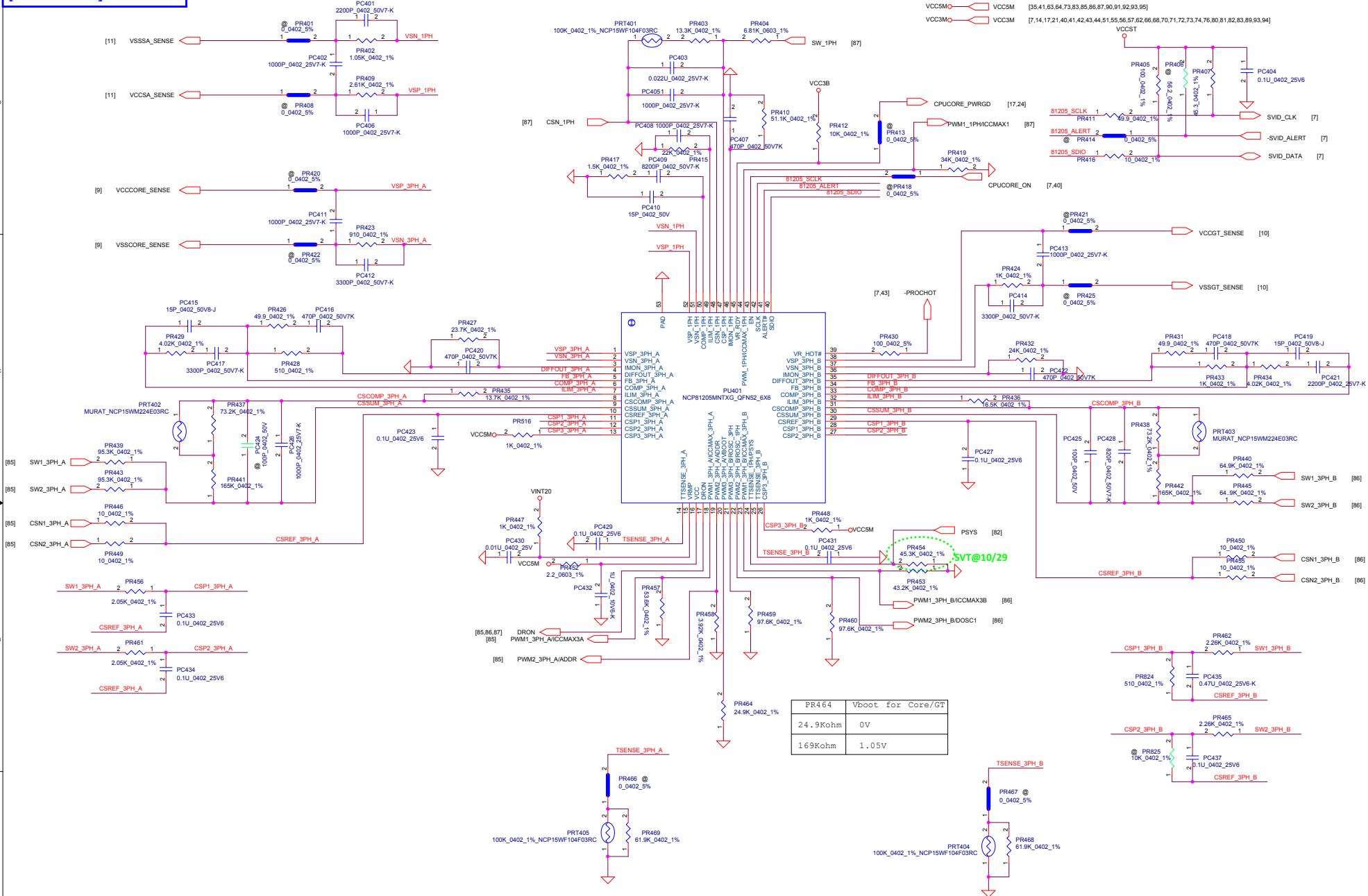
PEAK SHIFT	YES	NO
PR17	NO-ASM	ASM
PR7	ASM	NO-ASM
PQ8	ASM	NO-ASM
PQ7	ASM	NO-ASM

↑
LOGIC

Payton Common

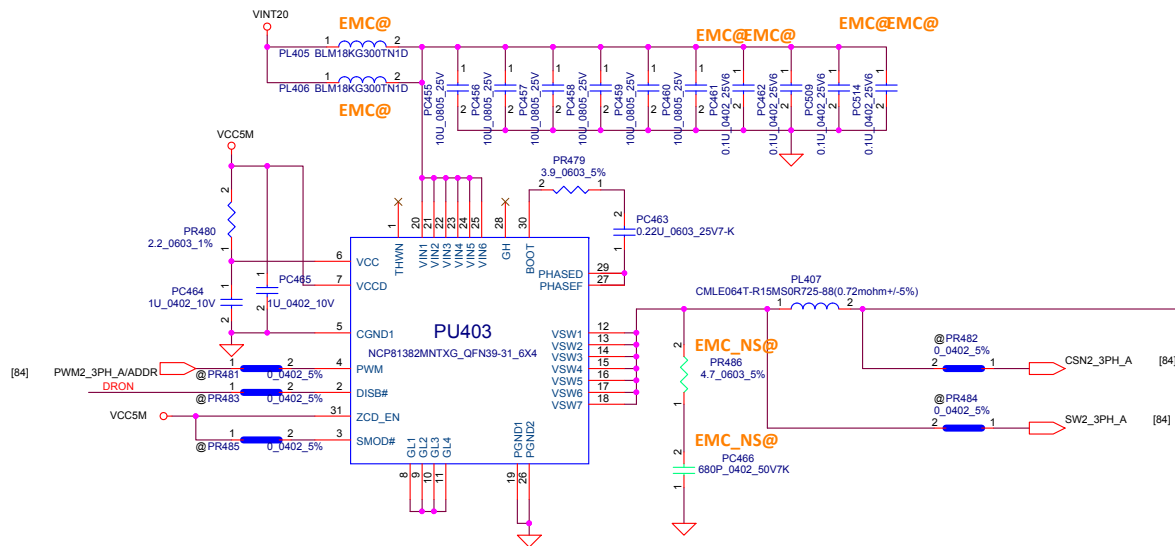
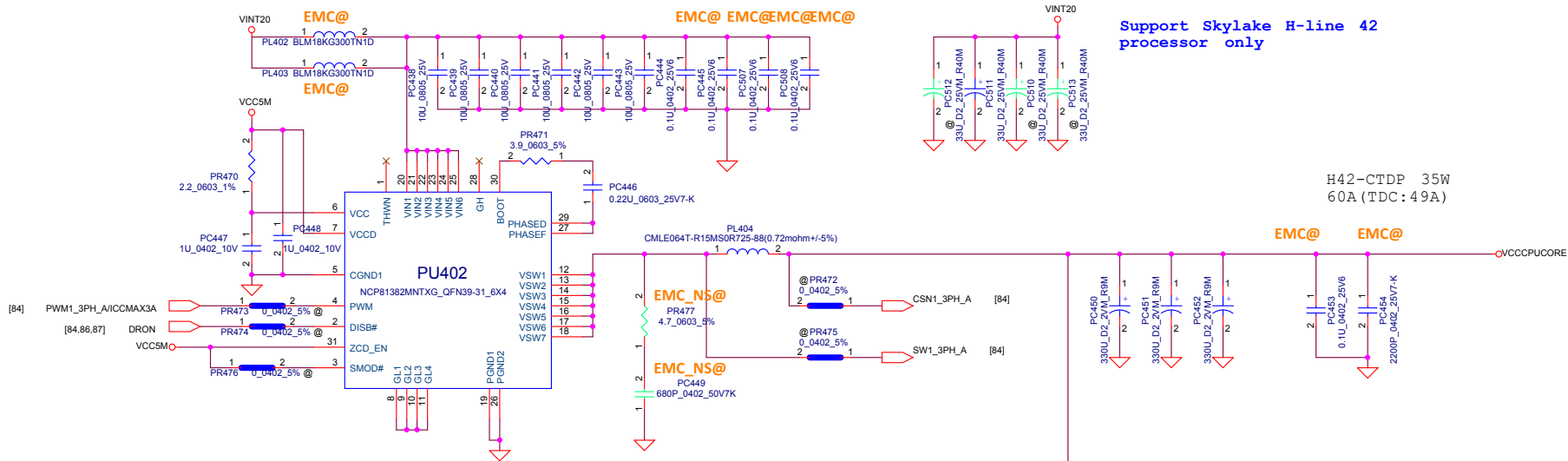


Support Skylake H-line 42 processor only



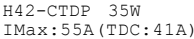
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Issued Date	2014/07/01	Deciphered Date	2015/12/31
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Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/07/01	Deciphered Date	2015/12/31	DC/DC VCCPUCORE	
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Size Custom	Document	Number	Rev		0.1
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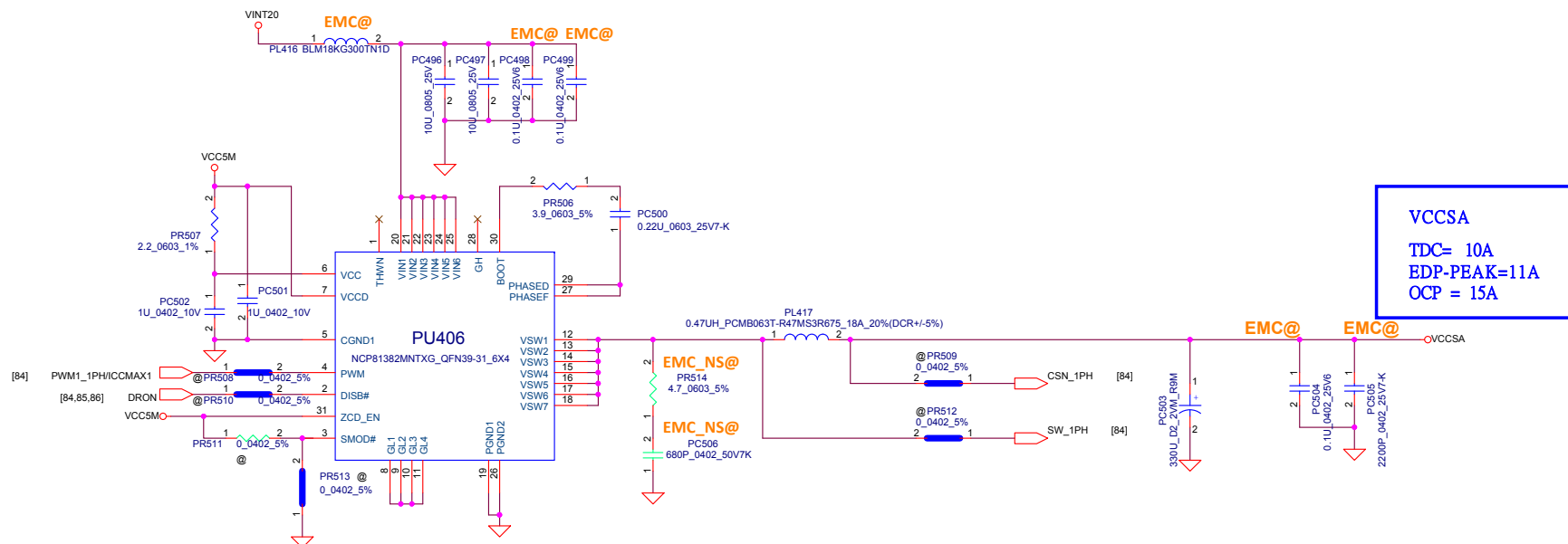
Support Skylake H-line 42
processor only



Security Classification	LC Future Center Secret Data			Title	
Issued Date	2014/07/01	Deciphered Date	2015/12/31	DC/DC VCCGFXCORE_I	
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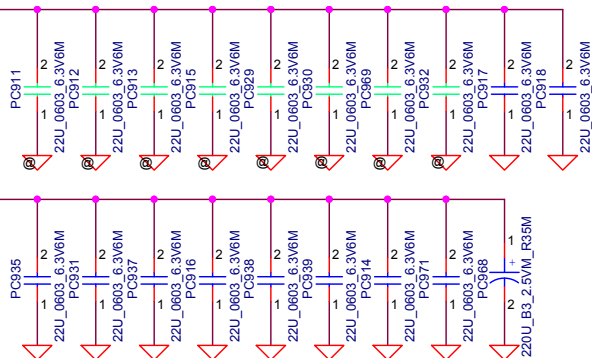
Walter Unique

Support Skylake H-line 42
processor only



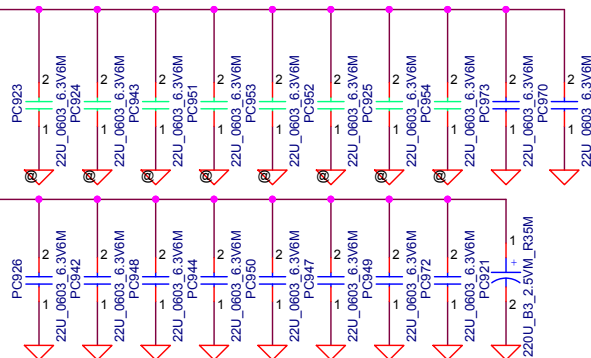
VCCCPUCORE

VCCCPUCORE
22uF 10pcs + 220uF/3528 1pcs



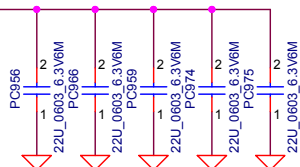
VCCGFXCORE_I

VCCGFXCORE_I
22uF 10pcs + 220uF/3528 1pcs

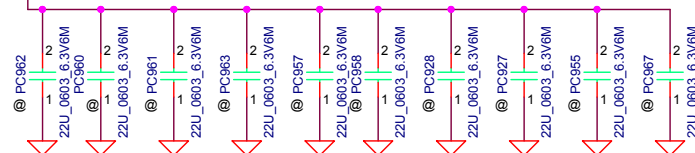


VCCSA

VCCSA
22uF 5pcs

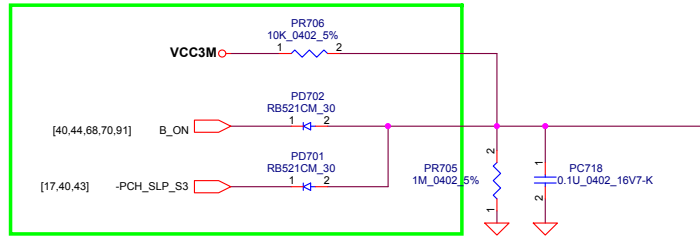


VCCSA

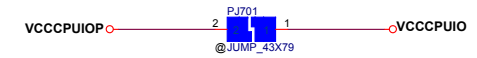


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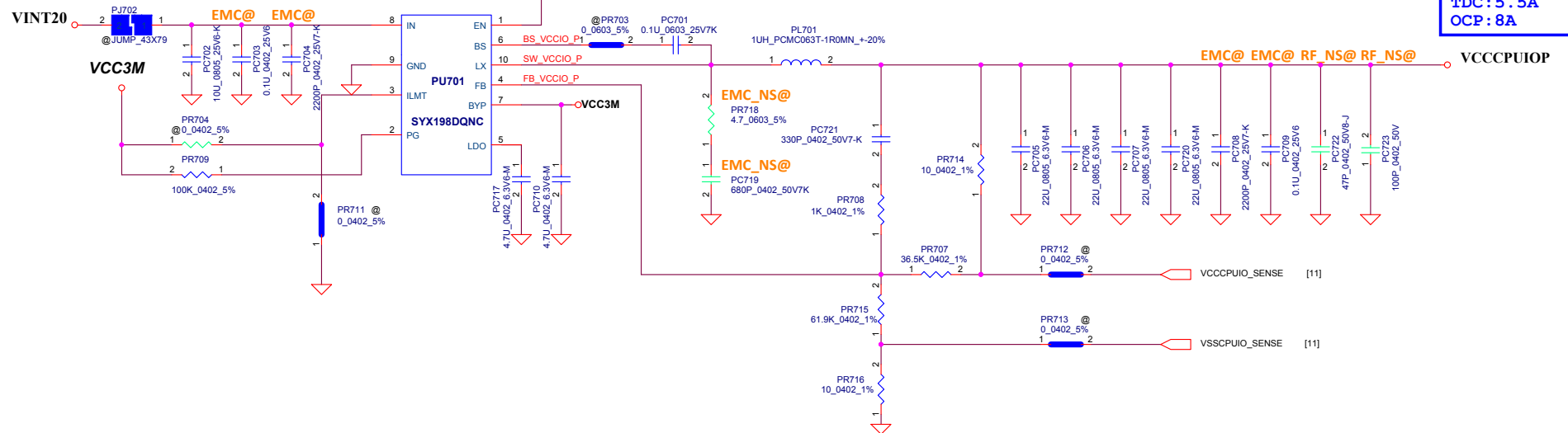
Title		Rev	
PROCESSOR DECOUPLING		0.1	
Size	Document Number	NM-A611	
Date:	Tuesday, November 03, 2015	Sheet	88 of 99

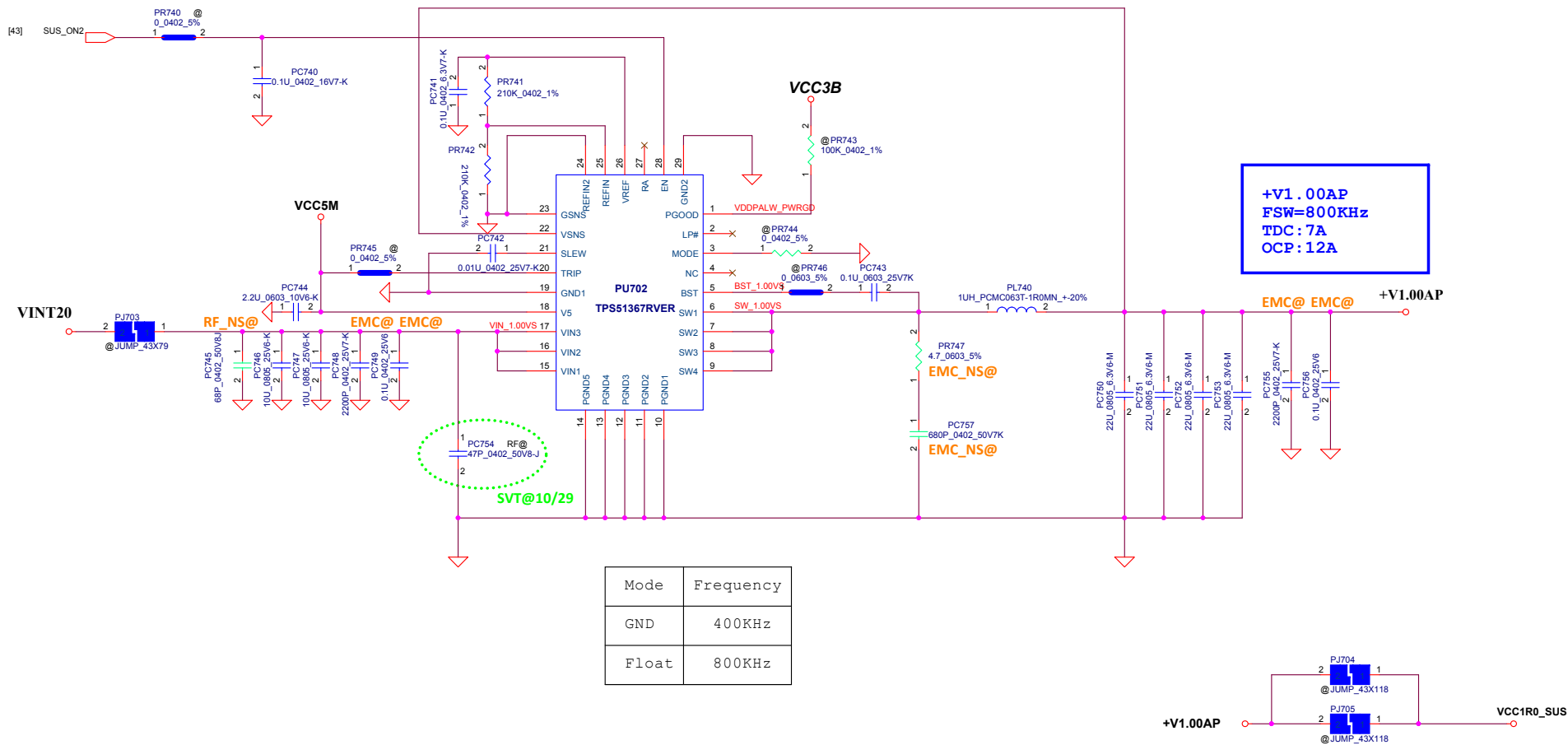


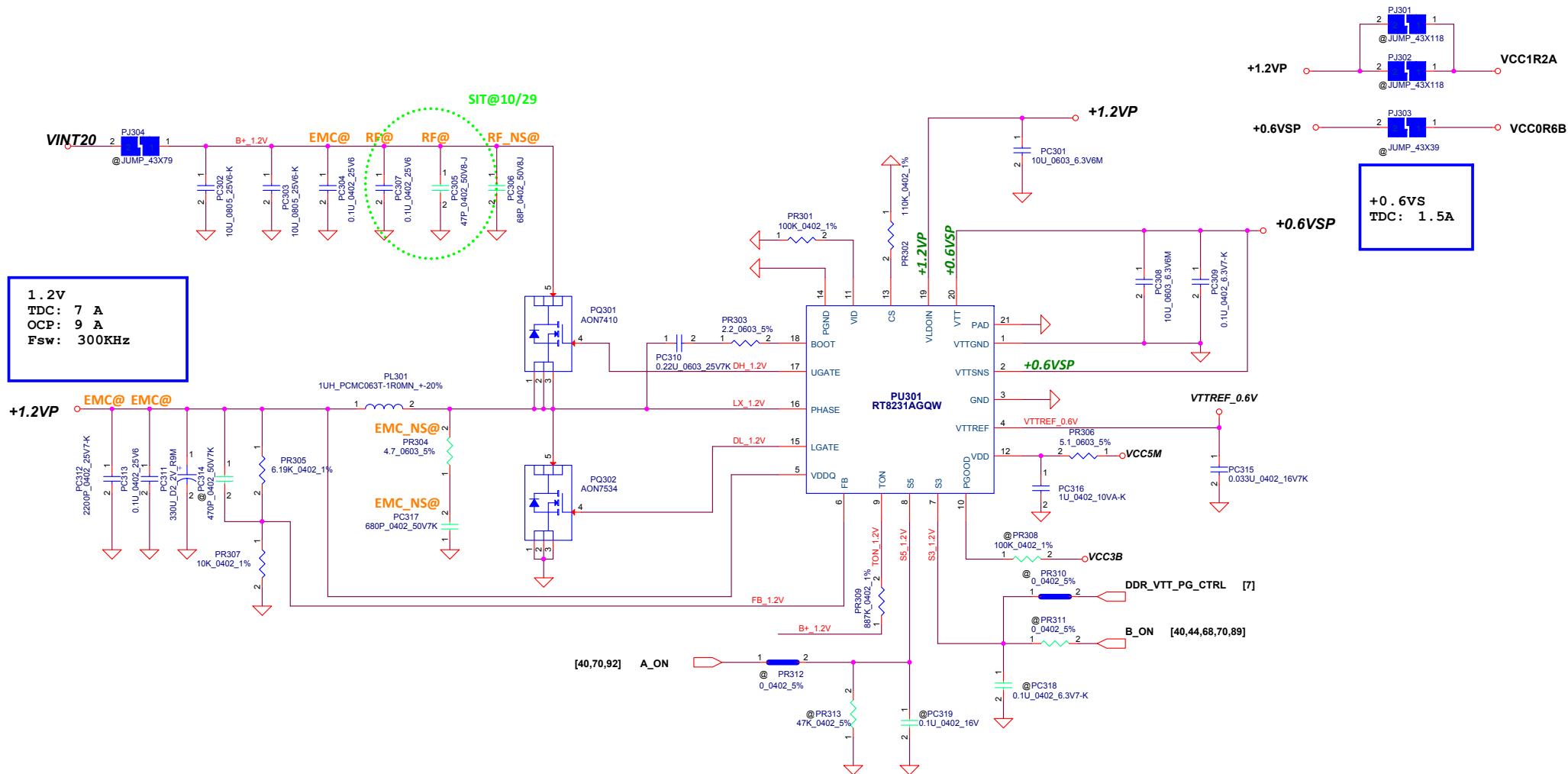
Follow Walter

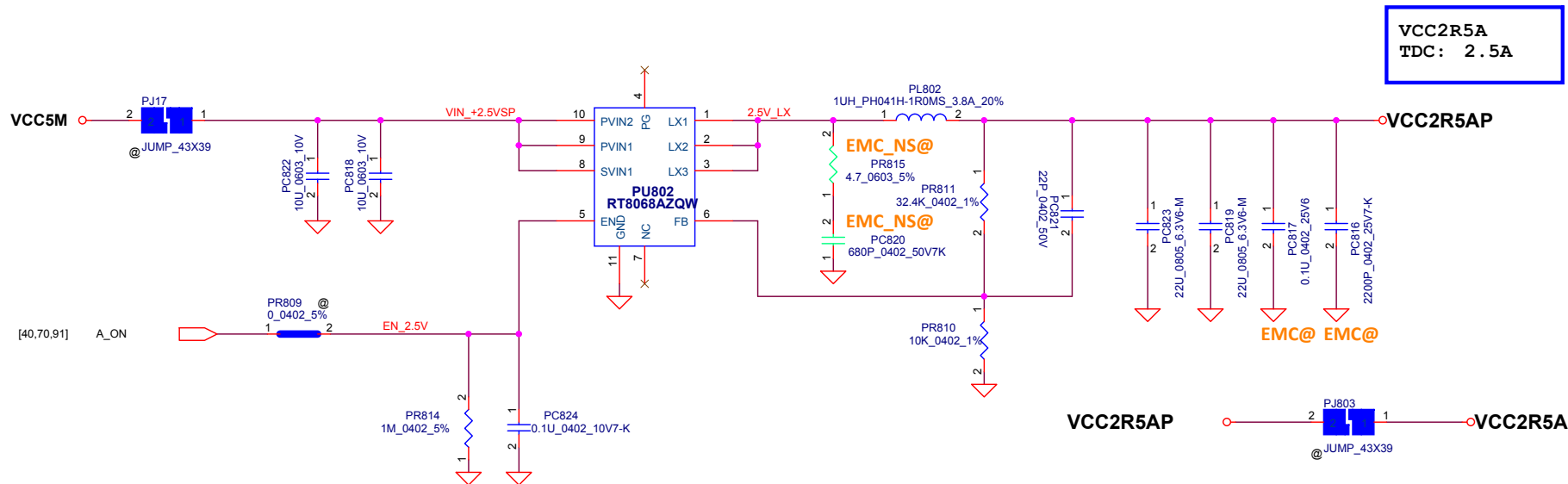


VCCCPUIOP
FSW=800KHz
TDC: 5.5A
OCF: 8A



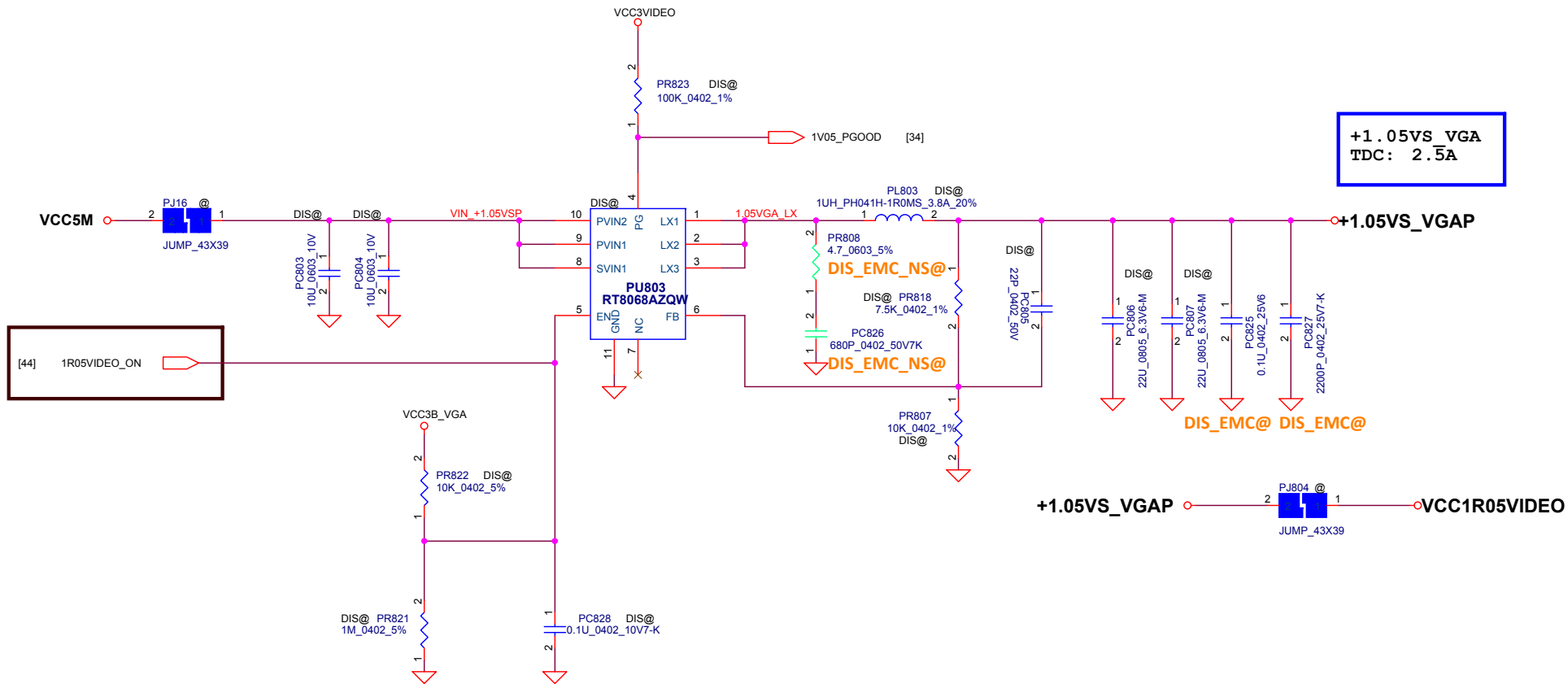






Security Classification		LC Future Center Secret Data	
Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Security Classification		LC Future Center Secret Data		Title			
Issued Date	2013/08/08	Deciphered Date	2013/08/05	PWR-+1.05ALW			
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				3		0.1	
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+0.6VSP		+0.6VSP	[91]	VINT20		VINT20	[35,41,56,80,81,82,83,84,85,86,87,89,90,91,93,94]	VCCGFXCORE_D		VCCGFXCORE_D	[31,35,76,93]	VCC3_SUS_SPI		VCC3_SUS_SPI	[19,26,55]
+1.05VS_VGAP		+1.05VS_VGAP	[95]	+3VL		+3VL	[45,47,57,67,83]	VCC3VIDEO		VCC3VIDEO	[31,34,35,93,95]	VCC5B_AVDD		VCC5B_AVDD	[45]
+1.2VP		+1.2VP	[91]	+5VL		+5VL	[40,83]	VCC3B_VGA		VCC3B_VGA	[34,35,76,93,95]	VCC5B_PVDD12		VCC5B_PVDD12	[45]
+1.5VSP		+1.5VSP	[94]	VCC3M		VCC3M	[7,14,17,21,40,41,42,43,44,51,55,56,57,62,66,68,70,71,72,73,74,76,80,81,82,83,89,93,94]	VCC1R05VIDEO		VCC1R05VIDEO	[31,33,34,76,95]	VCC3_SUS_DVDDIO		VCC3_SUS_DVDDIO	[45]
+V1.00AP		+V1.00AP	[90]	VCC3_SUS		VCC3_SUS	[7,14,15,16,17,18,21,23,24,26,42,43,45,71]	VCC1R5VIDEO		VCC1R5VIDEO	[33,34,35,37,39]	VCC3B_CPVDD		VCC3B_CPVDD	[45]
BAT-PWR12		BAT-PWR12	[81,82]	VCC3B		VCC3B	[7,16,17,18,19,20,21,23,24,27,28,35,40,41,42,43,44,45,47,49,54,55,56,57,58,59,60,61,62,67,68,73,74,81,84,90,91,94]				VCC3B_DVDD		VCC3B_DVDD	[45]	
DCIN_PWR20_F		DCIN_PWR20_F	[80,81,82]	VCC5M		VCC5M	[35,41,63,64,73,83,84,85,86,87,90,91,92,93,95]				VCC3B_DP		VCC3B_DP	[58]	
DOCK_DCIN20		DOCK_DCIN20	[60,81]	VCC5B		VCC5B	[41,45,57,59,61,65,66,67,71,73]				VCC3B_MINIDP		VCC3B_MINIDP	[59]	
DOCK_DCIN20_F		DOCK_DCIN20_F	[81]	VCCCPUCORE		VCCCPUCORE	[9,85,88]				VCC3GBE		VCC3GBE	[51,52,53]	
DOCK_PWR20		DOCK_PWR20	[60,80]	VCCGFXCORE_I		VCCGFXCORE_I	[10,86,88]				VCC3LAN		VCC3LAN	[51,72]	
M-BAT-PWR		M-BAT-PWR	[81]	VCCSA		VCCSA	[11,87,88]				VCC3M_EC		VCC3M_EC	[44]	
M-BAT-PWR_F		M-BAT-PWR_F	[81]	VCCST		VCCST	[7,11,16,24,43,70,84]				VCC3WWAN		VCC3WWAN	[62,74]	
VCC2R5AP		VCC2R5AP	[92]	VCCSTG		VCCSTG	[7,11,43,70]				VCC3WLAN		VCC3WLAN	[62,74]	
VCC3P		VCC3P	[56]	VCCCPUIO		VCCCPUIO	[5,6,11,89]				VCC5_TP		VCC5_TP	[66,71]	
VTTREF_0.6V		VTTREF_0.6V	[91]	RTCVCC		RTCVCC	[14,21,25,45]				VCC3_MC		VCC3_MC	[54]	
				VCC0R6B		VCC0R6B	[27,28,91]				VCC1R5B_AVDD		VCC1R5B_AVDD	[45]	
				VCC3SW		VCC3SW	[25,40,41,42,43,44,60,82]				+UIM_PWR		+UIM_PWR	[62]	
				VCC1R2A		VCC1R2A	[7,11,17,27,28,91]				+USB_VCCA		+USB_VCCA	[63]	
				VCC1R5B		VCC1R5B	[35,45,57,94]				LINE1_VREFO		LINE1_VREFO	[45,48]	
				VCC2R5A		VCC2R5A	[27,28,92]								
				VCC1R0_SUS		VCC1R0_SUS	[7,20,21,24,70,90]								
				VDD10		VDD10	[41]								

NOTE

1:NEED FIX SYMBOL
LV3301,LV3402,UL5201,U3401

2:NEED APPLY PART NUMBER
LV3101==>FROM BLM18PG121SN1D TO BLM15PD121SN1

3:10 OHM ALREADY CHANGE 470 OHM
RV3465,R7604,R7608