

Compal Confidential

STORM2 M/B Schematic

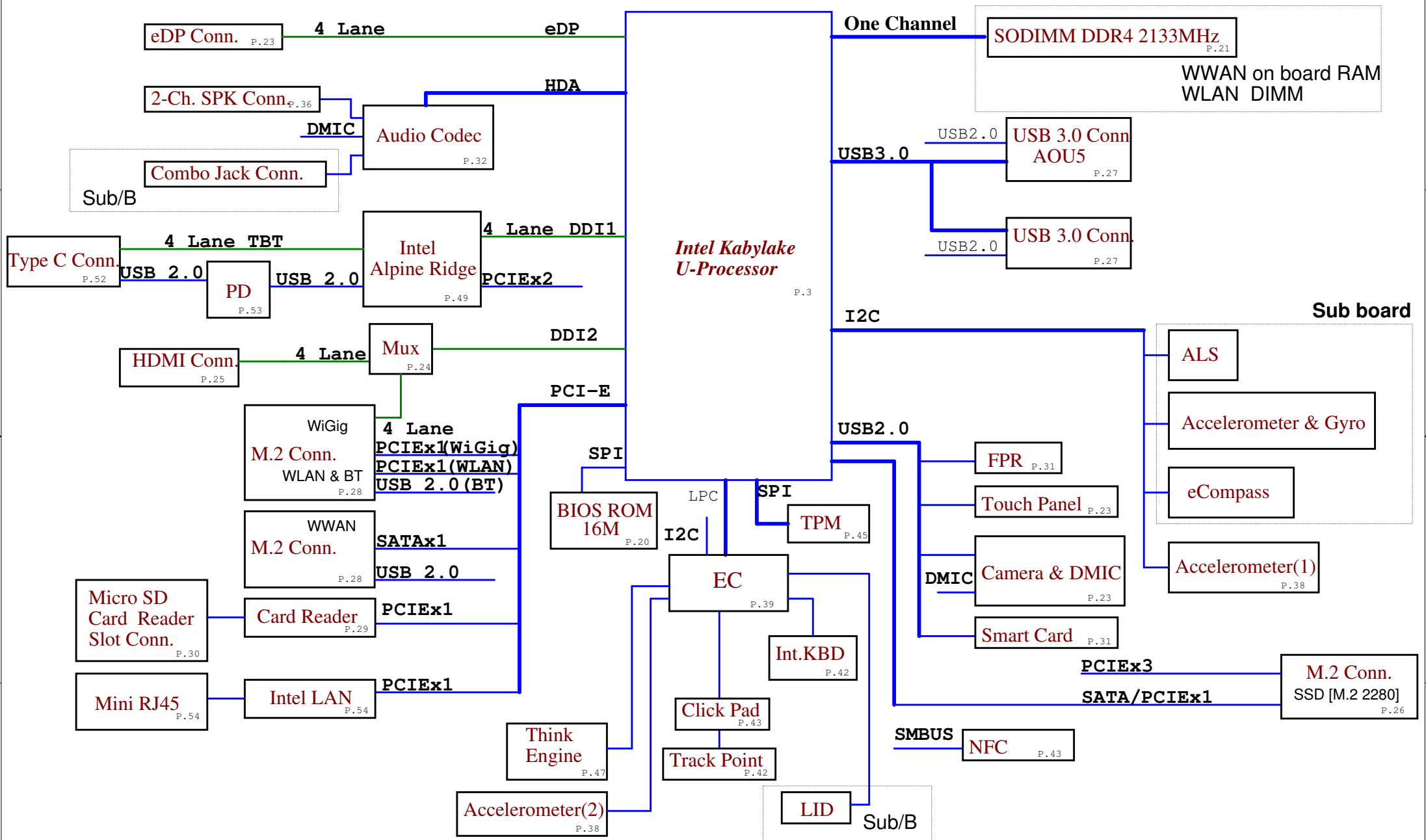
LA-E291P

Rev: 0.3_B

2016.09.01

Security Classification	Compal Secret Data		Title	<i>Compal Electronics, Inc.</i>	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	COVER PAGE	
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STORM 2 Block-Diagram



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	BLOCK DIAGRAM
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Sheet	2	Document Number	LA-E291P	Rev	0.3
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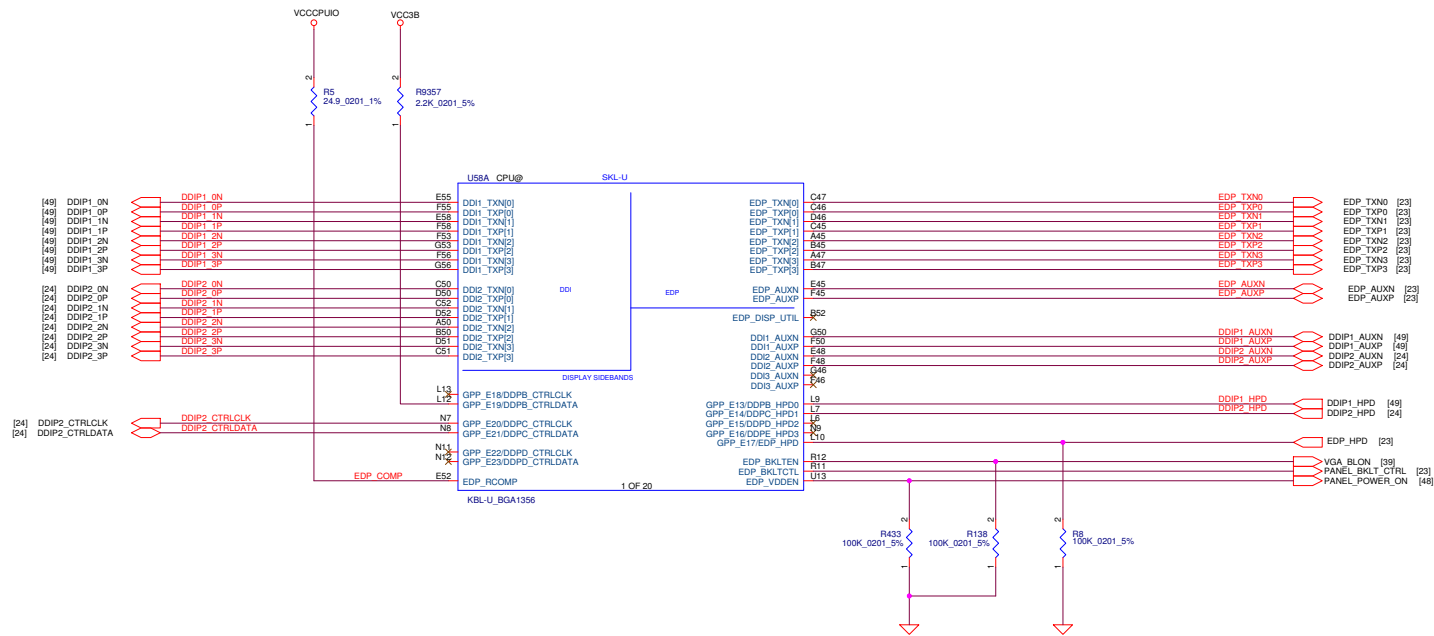


TABLE : Functional Strap

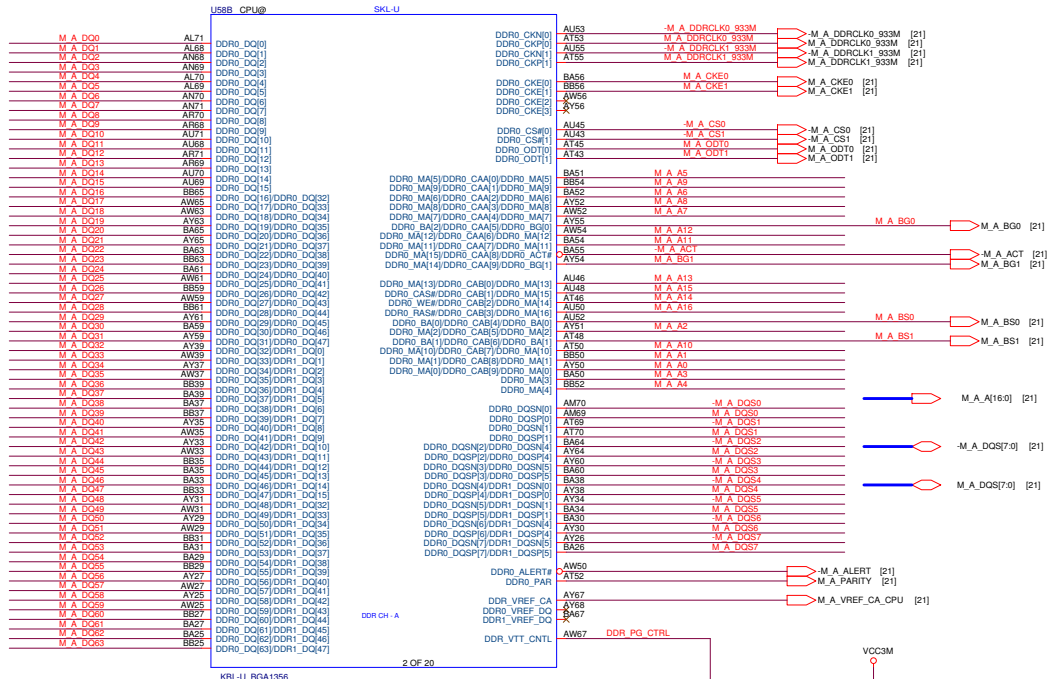
DDPB_CTRLDATA	
HIGH	Port B is detected.
LOW	Port B is not detected.
DDPC_CTRLDATA	
HIGH	Port C is detected.
LOW	Port C is not detected.

TABLE

Block	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
AU69	DDR0_DQ[15]	DDR0_DQ[15]	
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
	BA59	DDR0_DQ[30]	DDR0_DQ[46]
AY59	DDR0_DQ[31]	DDR0_DQ[47]	
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
BB33	DDR0_DQ[47]	DDR1_DQ[15]	
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
	BA25	DDR0_DQ[62]	DDR1_DQ[46]
BB25	DDR0_DQ[63]	DDR1_DQ[47]	

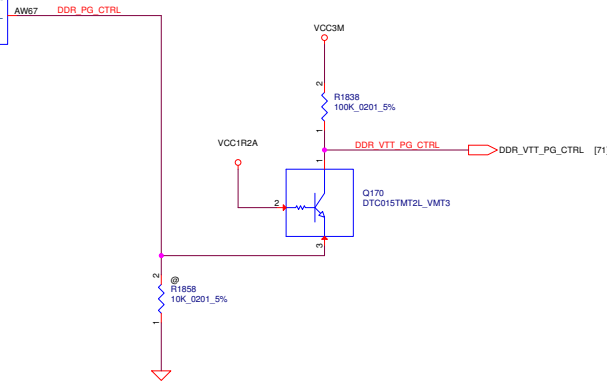
LOGIC

LOGIC



TABLE

Block	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]



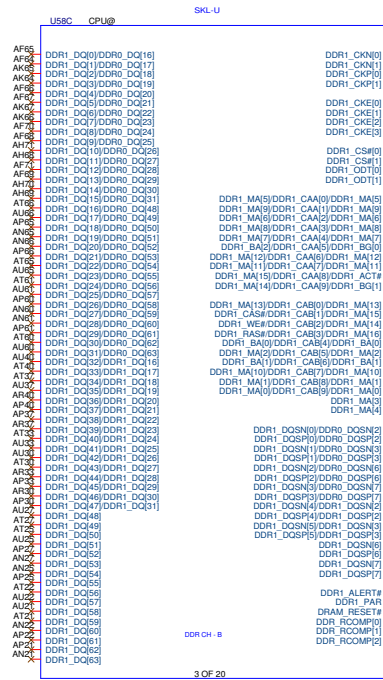
TABLE

Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_CAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

LOGIC

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
AH70	DDR1_DQ[14]	DDR0_DQ[30]	
AH69	DDR1_DQ[15]	DDR0_DQ[31]	
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
AT60	DDR1_DQ[30]	DDR0_DQ[62]	
AU60	DDR1_DQ[31]	DDR0_DQ[63]	
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
AR30	DDR1_DQ[46]	DDR1_DQ[30]	
AP30	DDR1_DQ[47]	DDR1_DQ[31]	
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
AP21	DDR1_DQ[62]	DDR1_DQ[62]	
AN21	DDR1_DQ[63]	DDR1_DQ[63]	

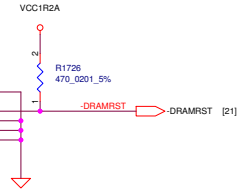


TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
AG70	DDR1_DQSP[1]	DDR0_DQSP[3]	
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

TABLE

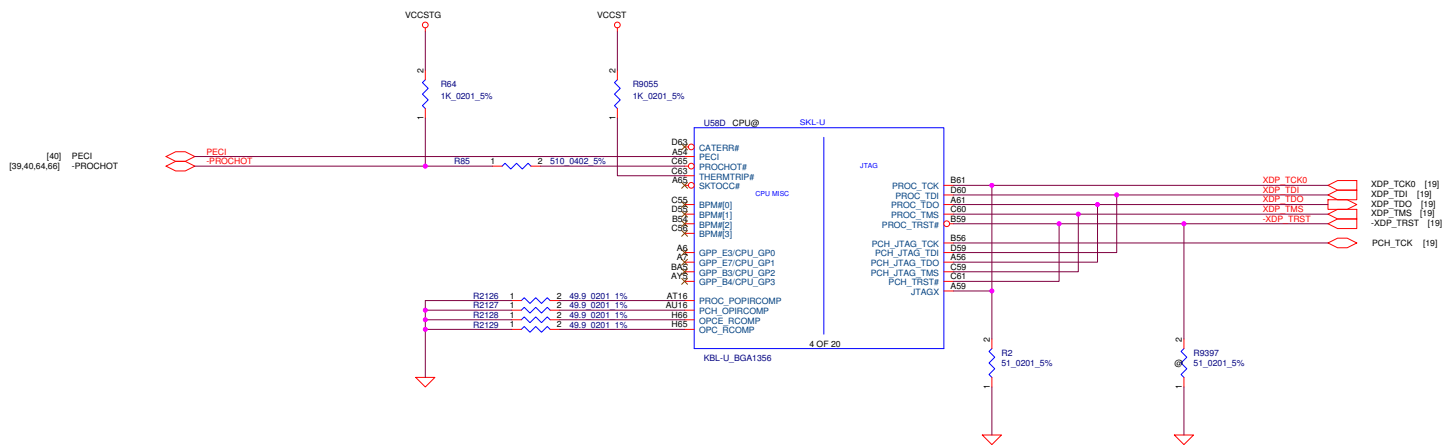
Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]



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[40] PECE
[39,40,64,66] -PROCHOT

Security Classification	Compal Secret Data		2016/12/31		Compal Electronics, Inc.	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title		CPUL(416) : MISC/JTAG
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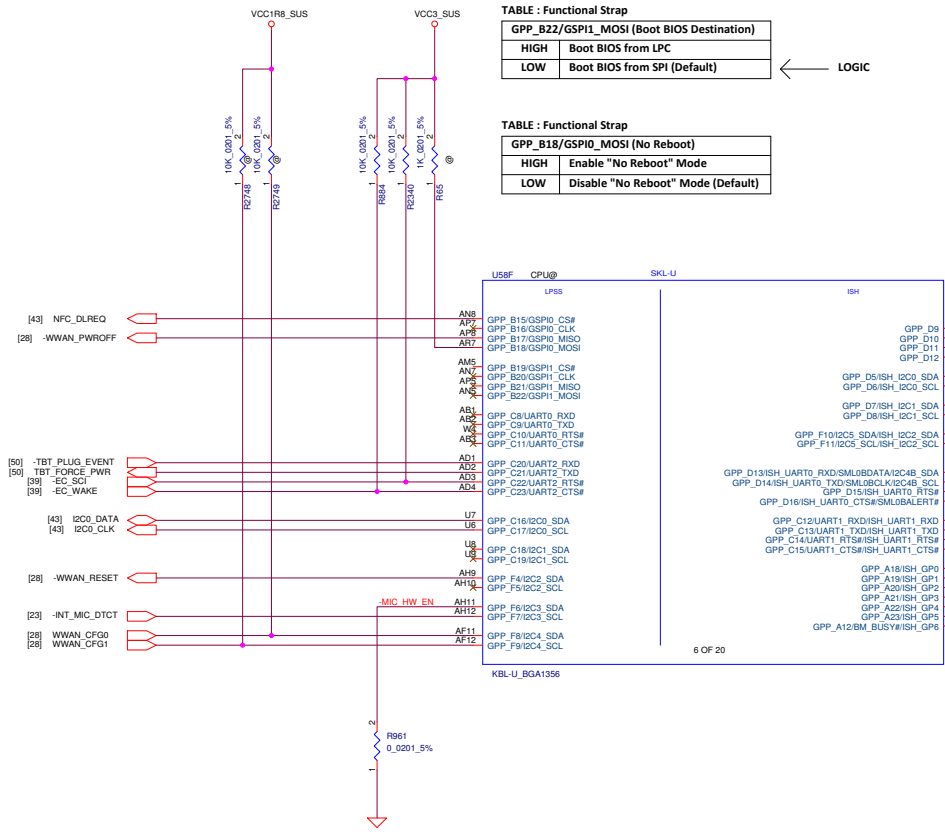


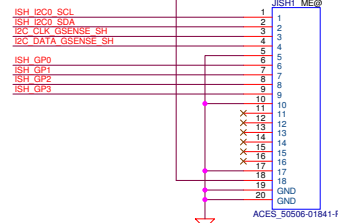
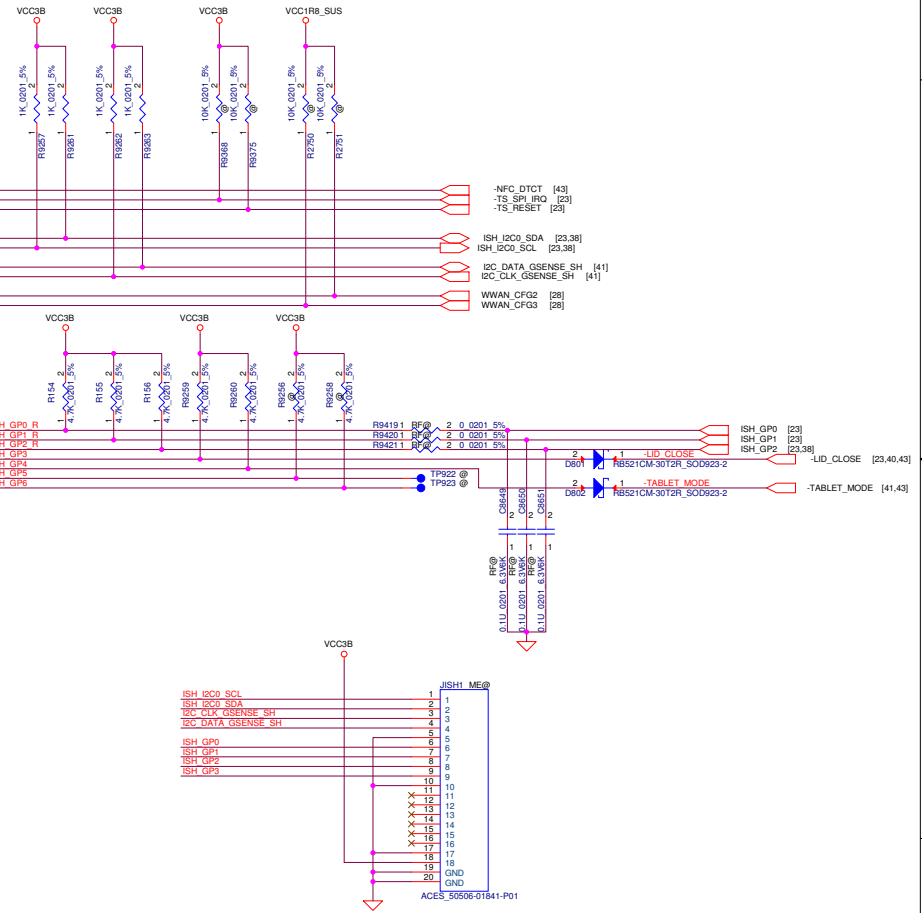
TABLE : Functional Strap

GPP_B22/GSP11_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI (Default)

← LOGIC

TABLE : Functional Strap

GPP_B18/GSP10_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)



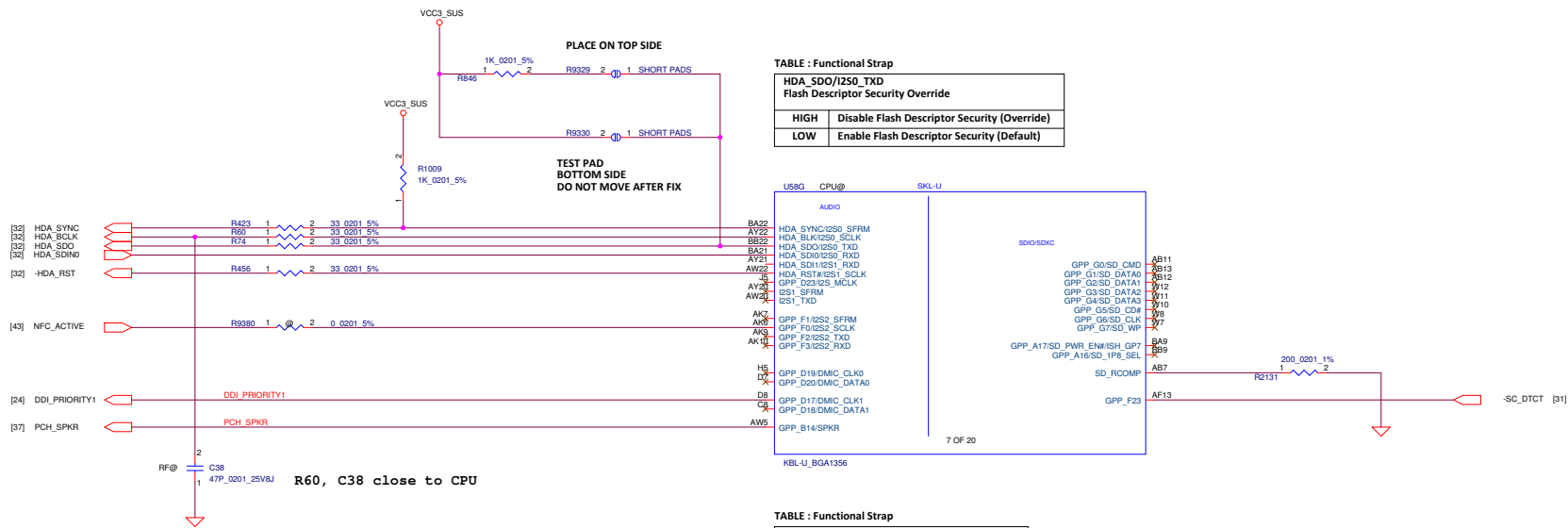


TABLE : Functional Strap

HDA_SDO/I2SD0_TXD Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

TABLE : Functional Strap

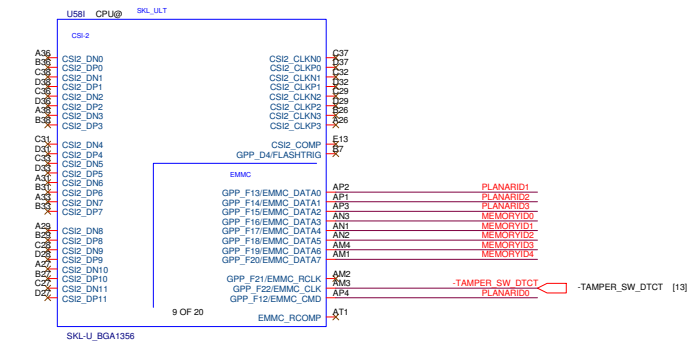
GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default)

← LOGIC

TABLE

MEMORY[4..0]	U125, U126, U127, U128		R7 (Rcomp0)
00000B	Micron MT40A512M16HA-083E:A	8Gbit SDP 4GB	200 1%
00001B	Micron MT40A1G16HBA-083E:A	16Gbit DDP 8GB	121 1%
00010B	Samsung K4A8G16SWB-BCP8	8Gbit SDP 4GB	200 1%
00011B	Reserved		
00100B	Reserved		
00101B	Samsung K4AAG16SWB-MCRC	16Gbit DDP 8GB	121 1%
00110B	Samsung K4AAG16SWB-MCRC	8Gbit SDP 4GB	200 1%
00111B	Micron MT40A512M16Y-083E:B	8Gbit SDP 4GB	200 1%
01000B	Micron MT40A1G16WBU-083E:B	16Gbit DDP 8GB	121 1%
01001B	Hynix H5AN8G6NAFR-UHC	8Gbit SDP 4GB	200 1%
01010B	Hynix T8D	16Gbit DDP 8GB	121 1%
01011B	Samsung K4AAG16SWB-MCRC	16Gbit DDP 8GB	121 1%
11111B	NO_ASM	No Soldered Memory	

Storm1 only

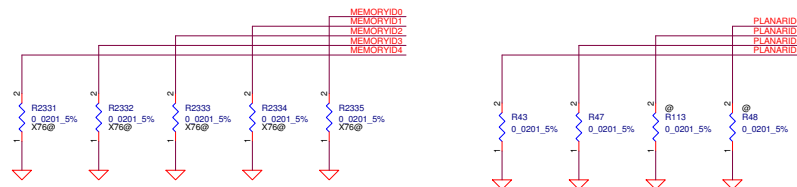


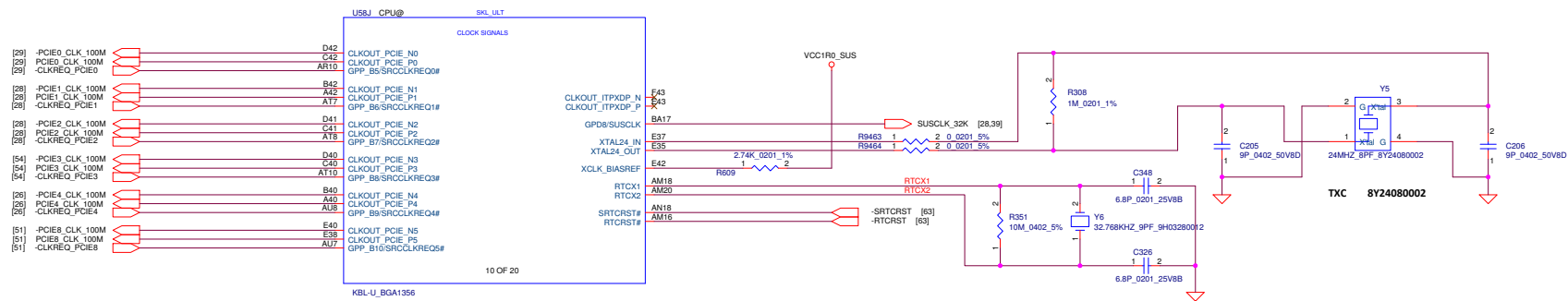
TABLE

LEVEL	PLANAR ID			
	3	2	1	0
	R43	R47	R113	R48
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

TABLE

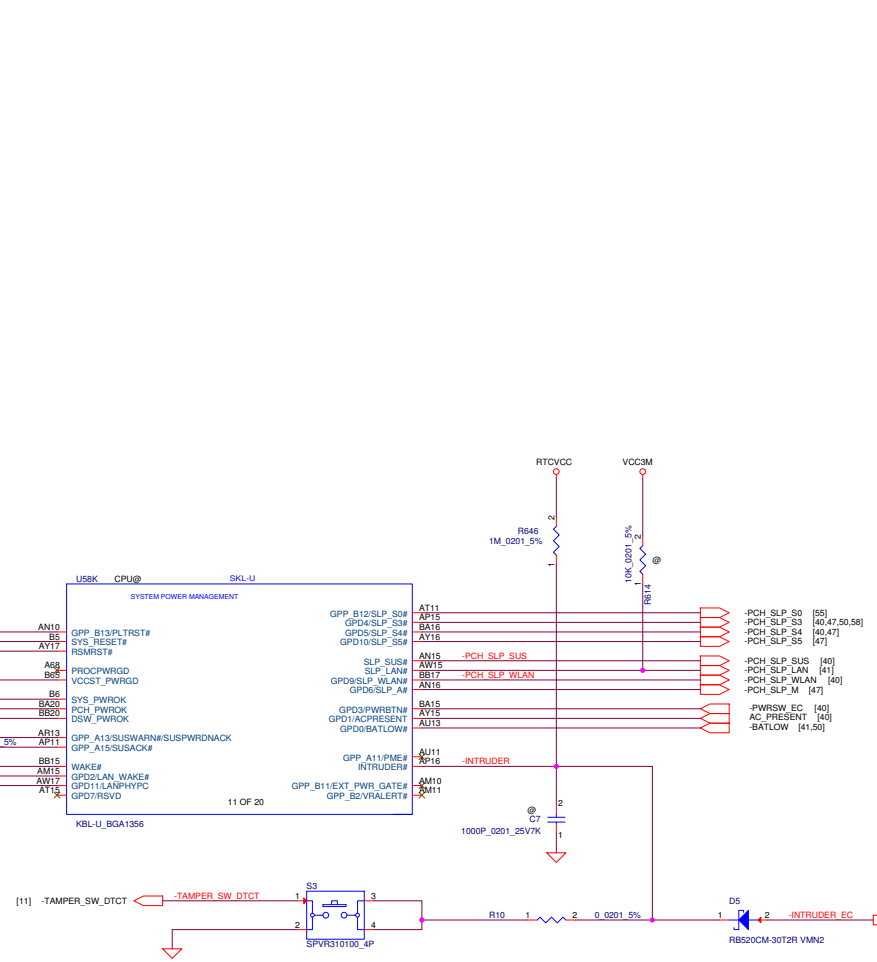
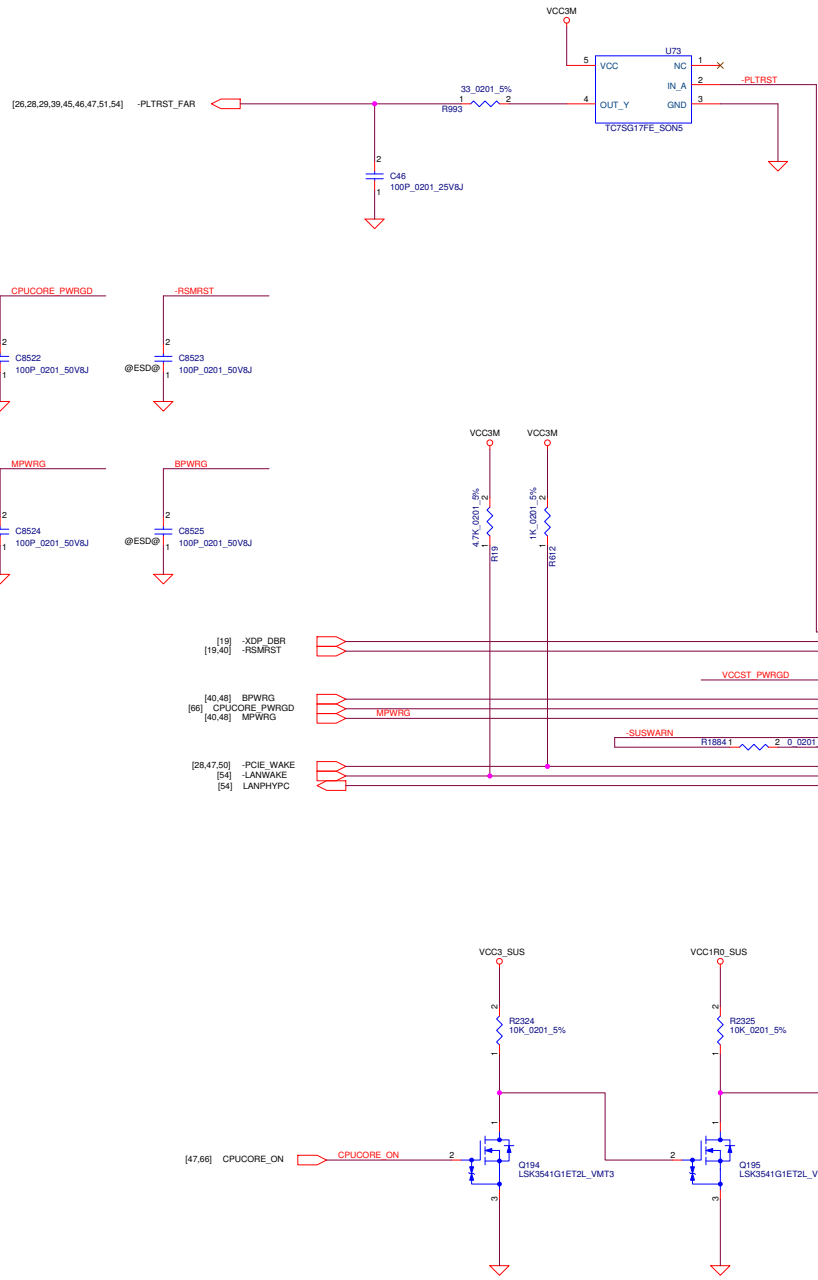
LEVEL	PLANARID[3..0]
SDV	0001B
FVT	0010B
SIT	0011B
SIT-R	0100B
SVT	0101B



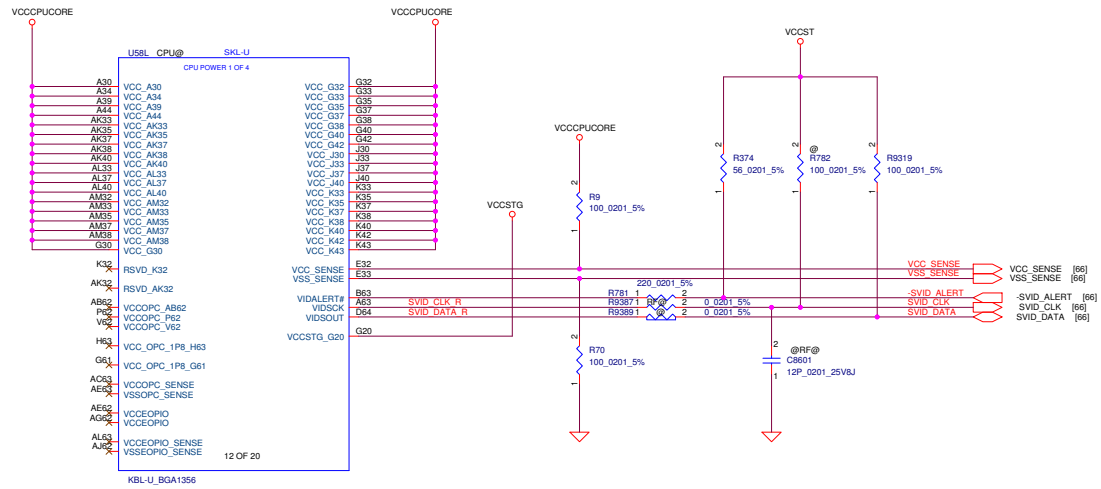


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KDS 1TJF090DJ1A000B

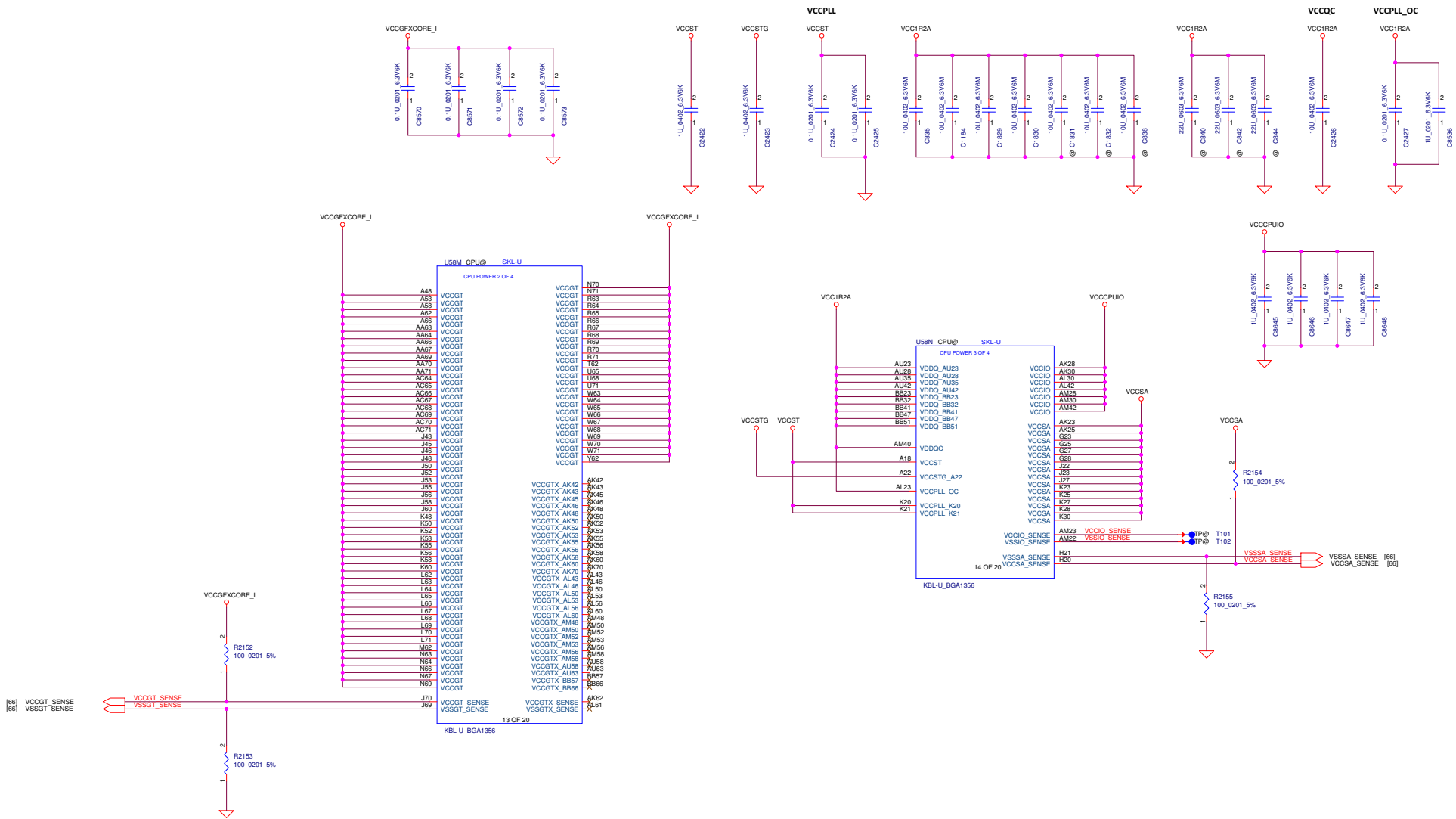
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			Date:	Thursday, September 01, 2016	Sheet 12 of 75



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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Compal Electronics, Inc.	
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				Date	Thursday, September 01, 2016
				Sheet	13 of 75



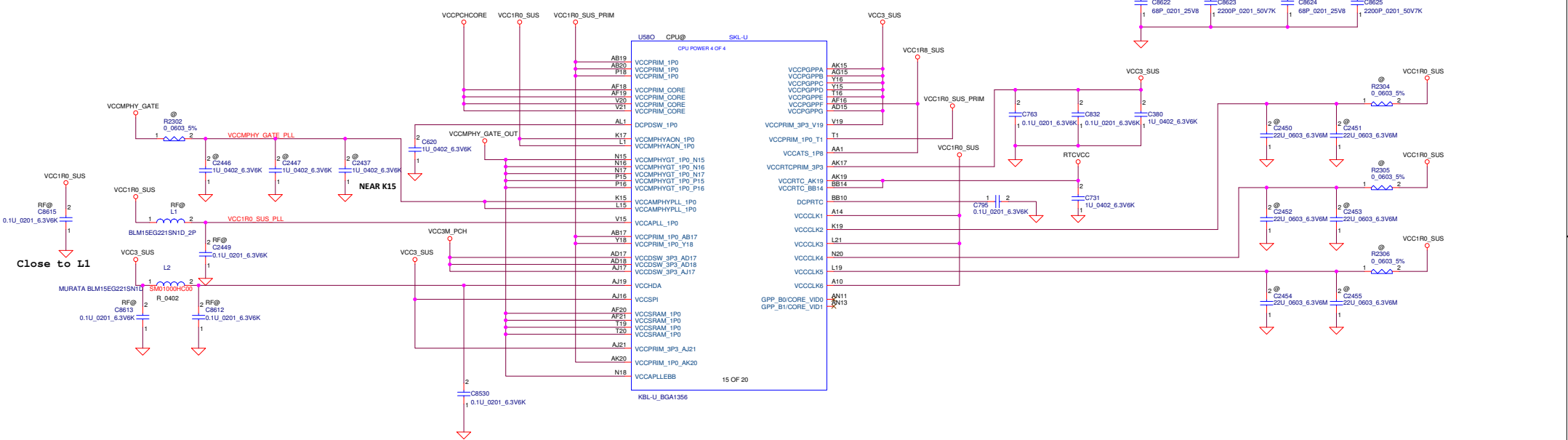
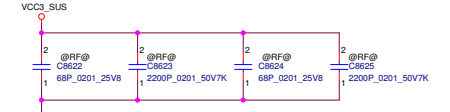
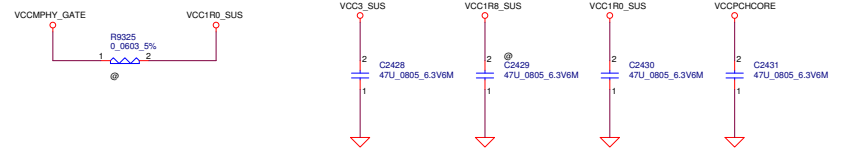
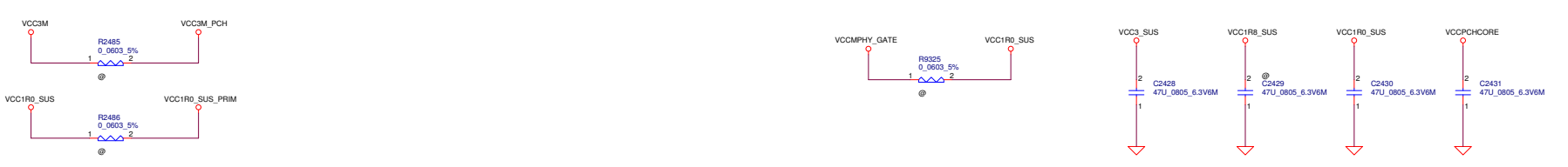
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DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Document Number LA-E291P Date: Thursday, September 01, 2016 Sheet 14 of 75
			Rev 0.3



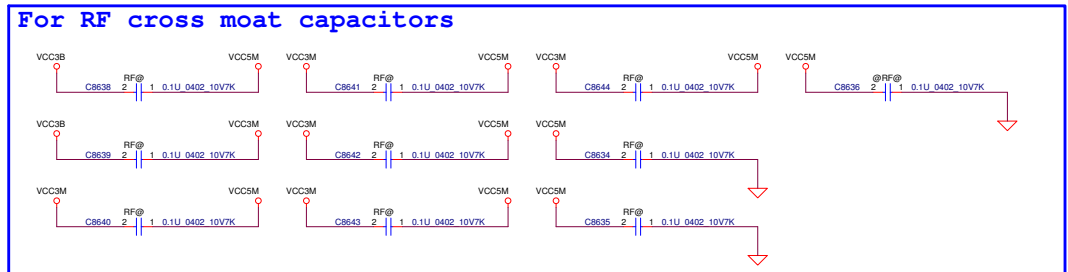
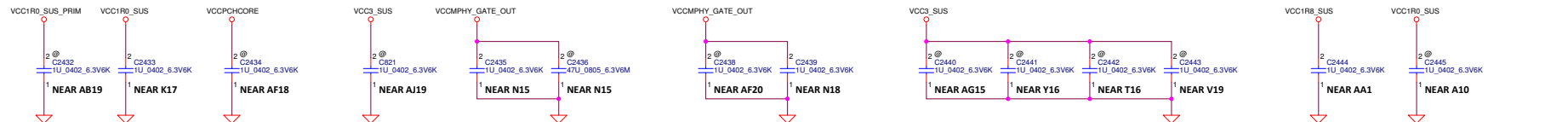
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[66] VSSGT SENSE

[66] VCCSA SENSE
[66] VSSSA SENSE

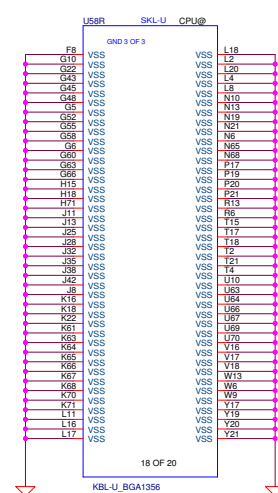
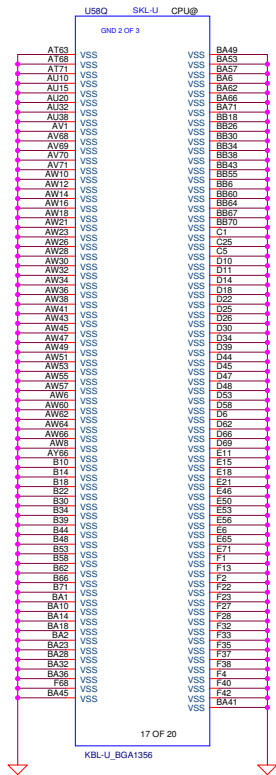
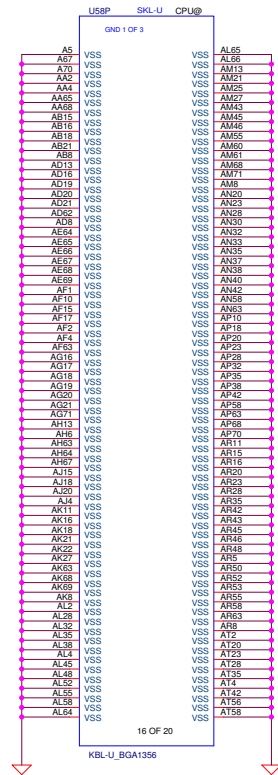
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	CPU : CPU POWER (2/2)	
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Close to L1

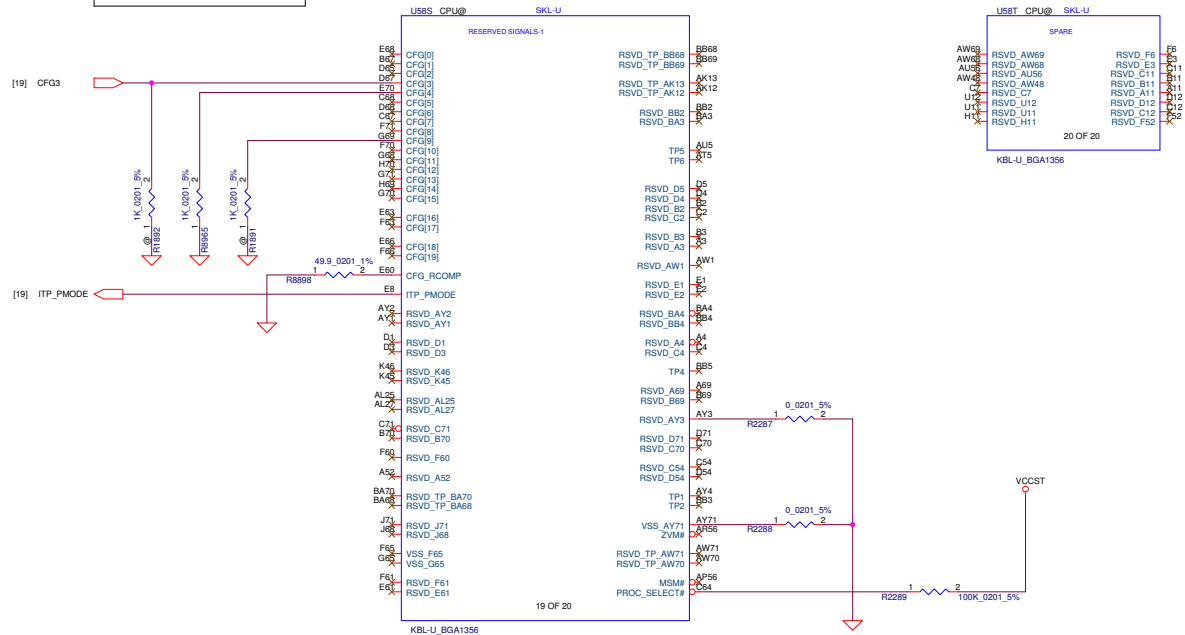


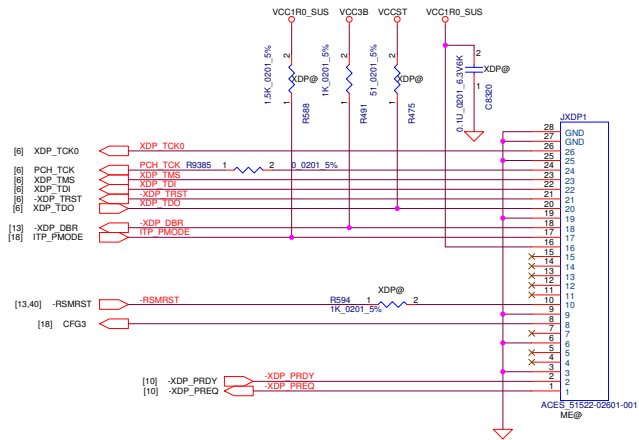
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Issued Date	2014/11/04		Deciphered Date		2016/12/31	Document Number		CPU : PCH POWER	
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						Date		Thursday, September 01, 2016	
						Sheet		16 of 75	



TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall
CFG3 : MSR Privacy Bit Feature 1 : MSR (C80h) bit[0] setting 0 : MSR (C80h) bit[0] overridden
CFG4 : eDP Enable 1 : Disabled 0 : Enabled
CFG9 : SVID Bus Communication 1 : Enabled 0 : Disabled

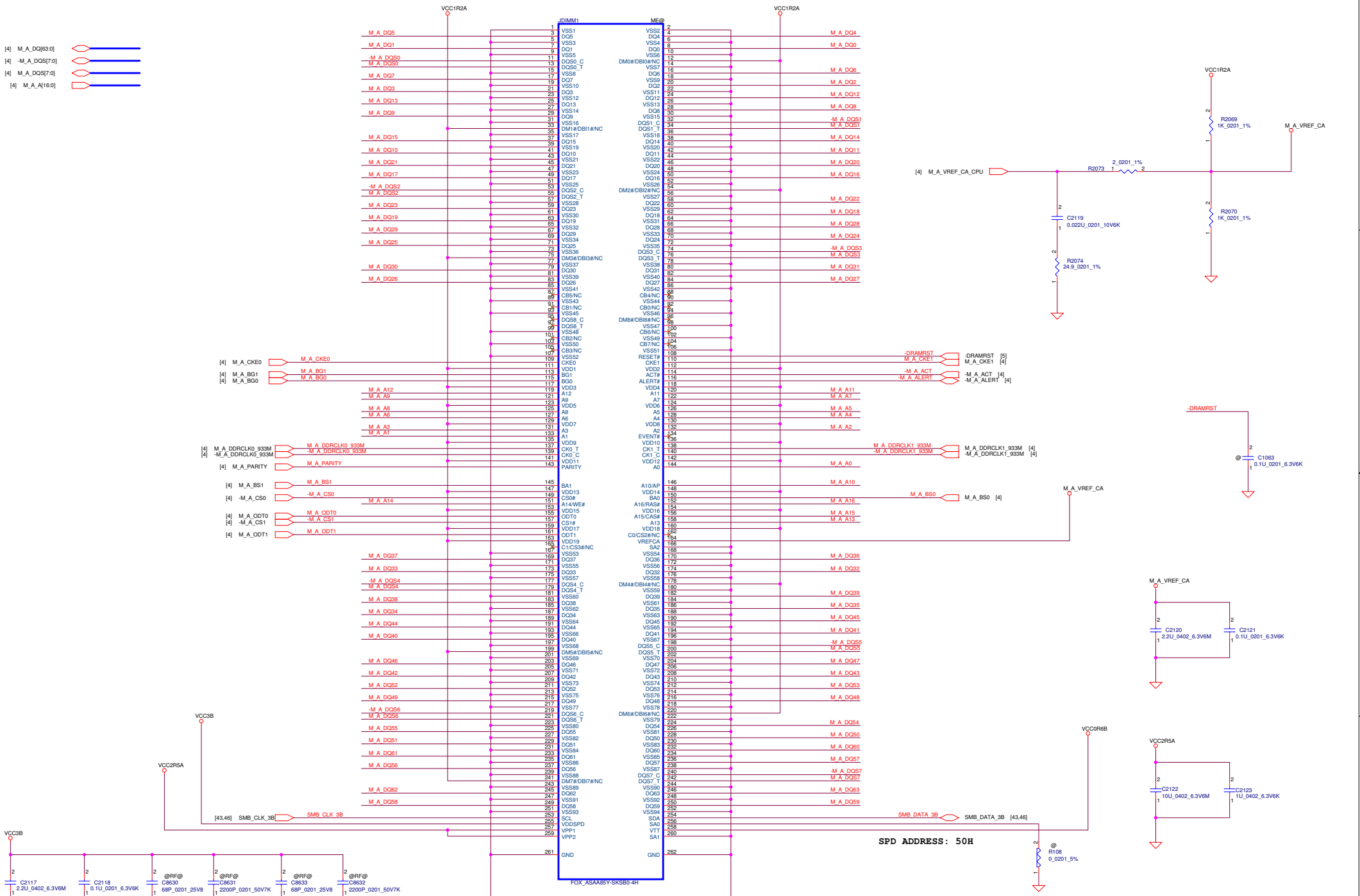




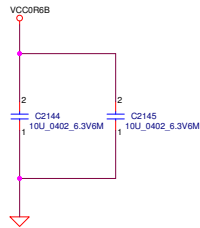
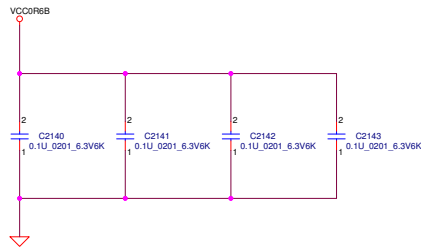
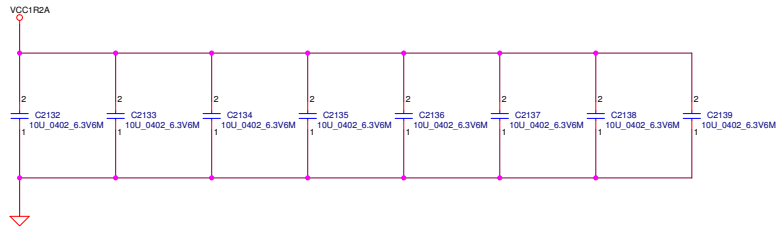
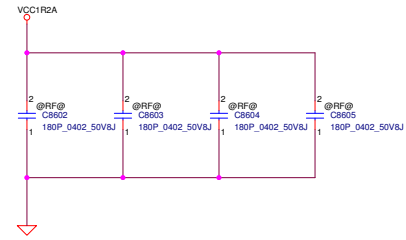
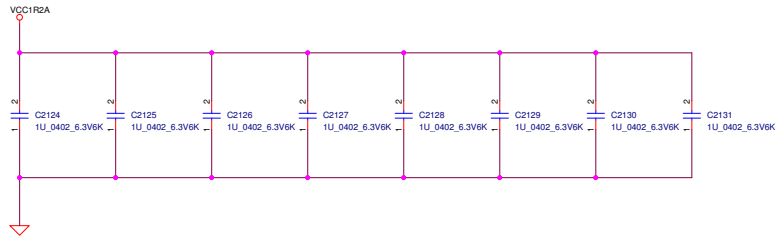
TABLE

Logic	Ref Des	Merged	DCI 2.0
Page 7	R2559	ASM	NO_ASM
Page 18	R1982	ASM	NO_ASM
Page 19	J8	ASM	NO_ASM
	C8320	ASM	NO_ASM
	R475	ASM	ASM
	R491	ASM	ASM
	R588	ASM	NO_ASM
	R594	ASM	NO_ASM
	R2494	ASM	NO_ASM

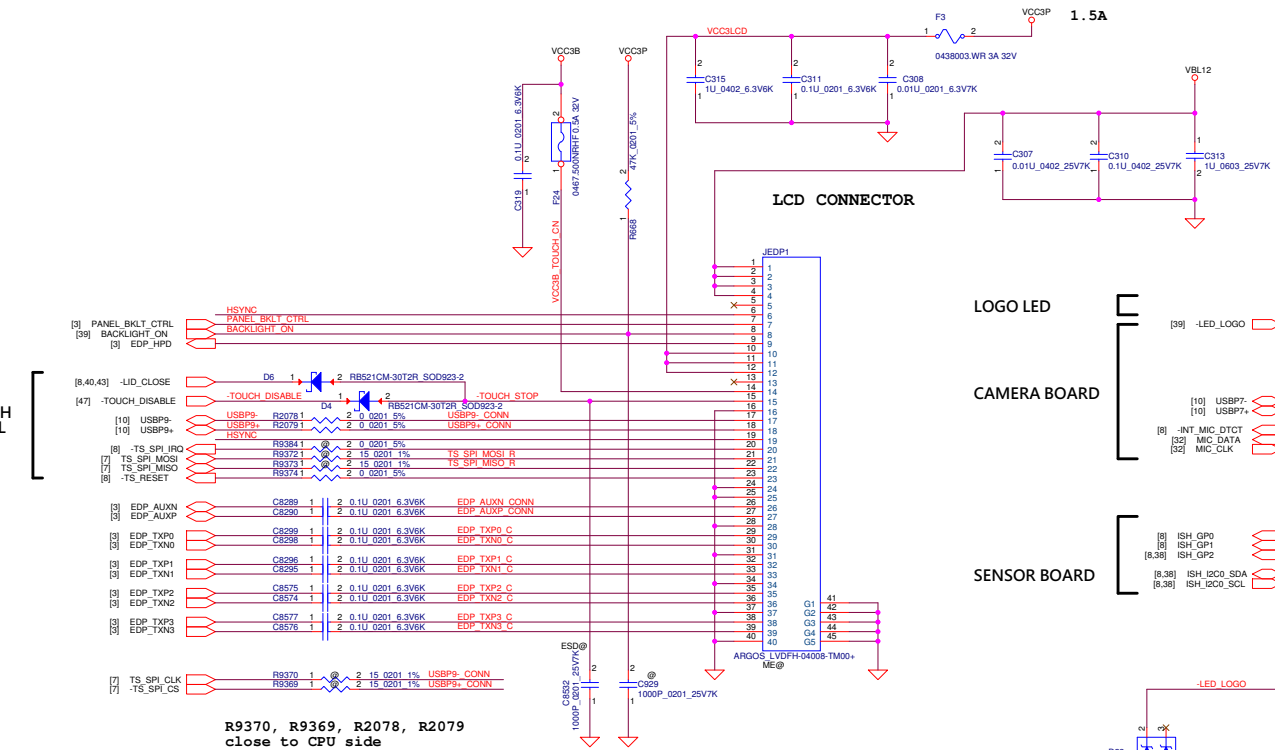
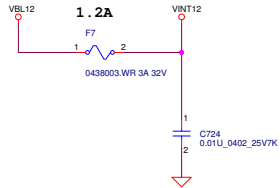
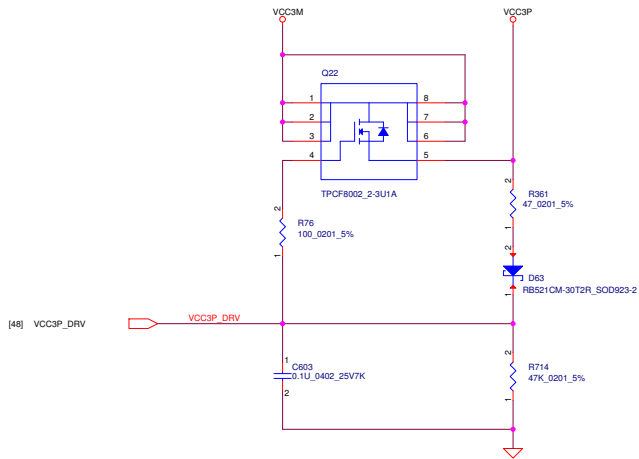
- [4] M_A_DQ[63:0]
- [4] -M_A_DQS[7:0]
- [4] M_A_DQS[7:0]
- [4] M_A_A[16:0]



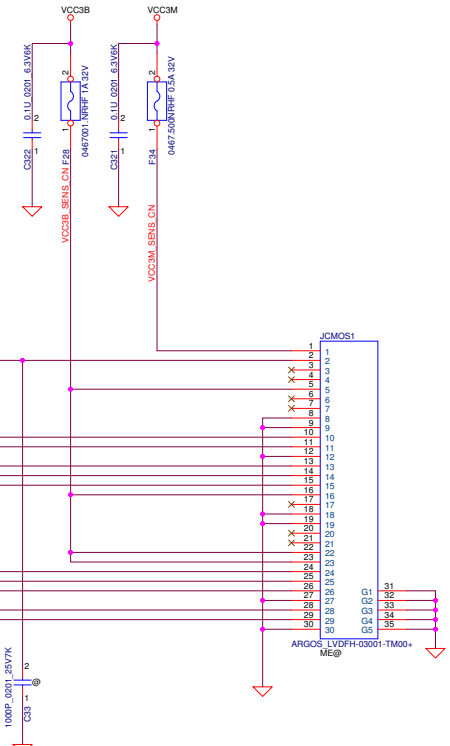
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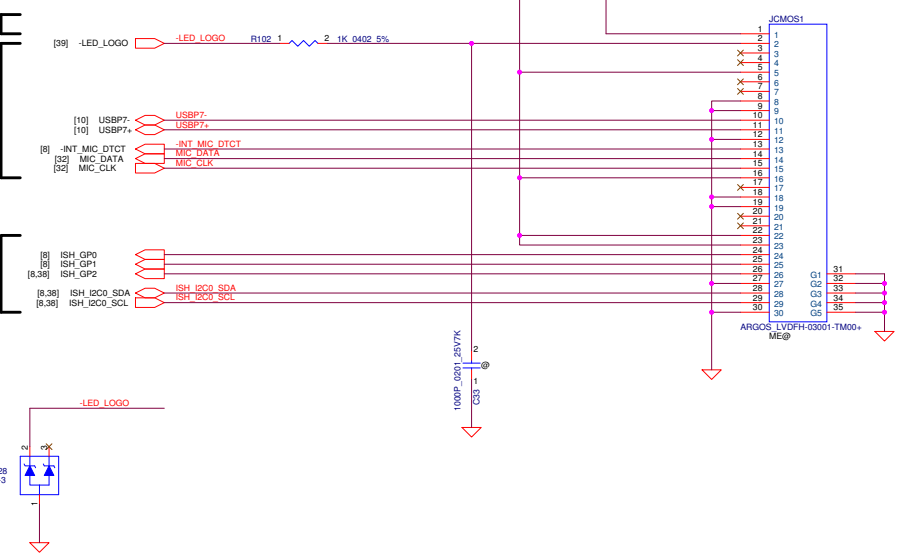
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				Rev 0.3
				Date: Thursday, September 01, 2016 Sheet 22 of 75



R9370, R9369, R2078, R2079
close to CPU side



LOGO LED
CAMERA BOARD
SENSOR BOARD



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Date: Thursday, September 01, 2016				1A-E791P
Sheet 23 of 75				0.3

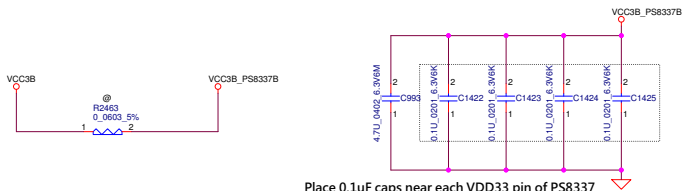
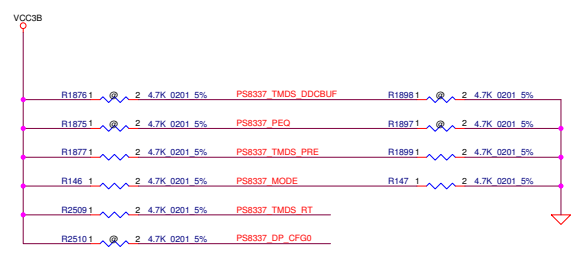
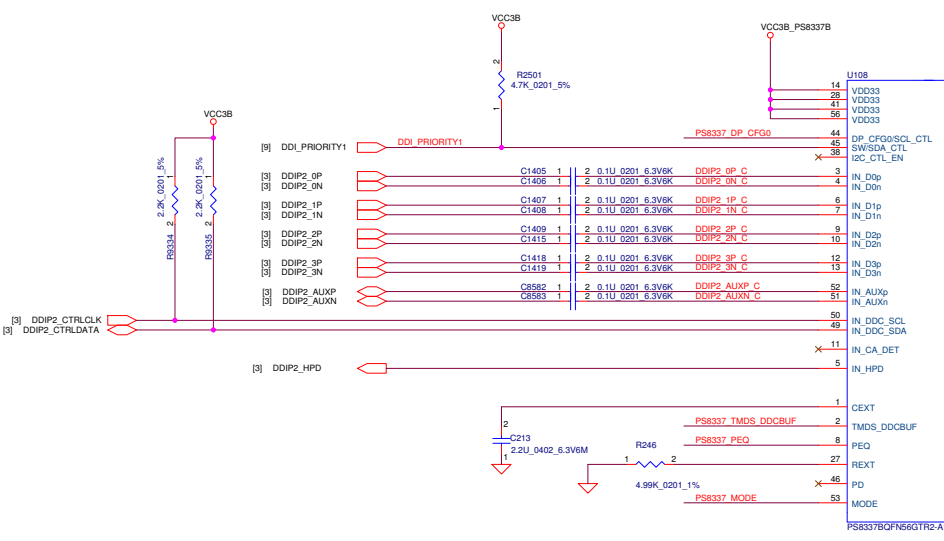


TABLE : Automatic Switching Mode (MODE = H, M)

SW (DDI_PRIORITY1)	
L	DP Port has higher priority when both ports are plugged
H	TMDS Port has higher priority when both ports are plugged



TMDS DDCBUF (INT PD)	R1876	R1898	
DDC Active Buffer	ASM	NO_ASM	
DDC Pass Through w/ PU	ASM	ASM	
DDC Pass Through w/o PU	NO_ASM	NO_ASM	← LOGIC



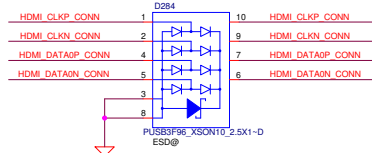
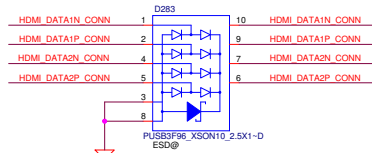
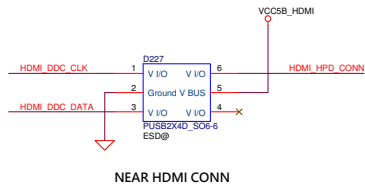
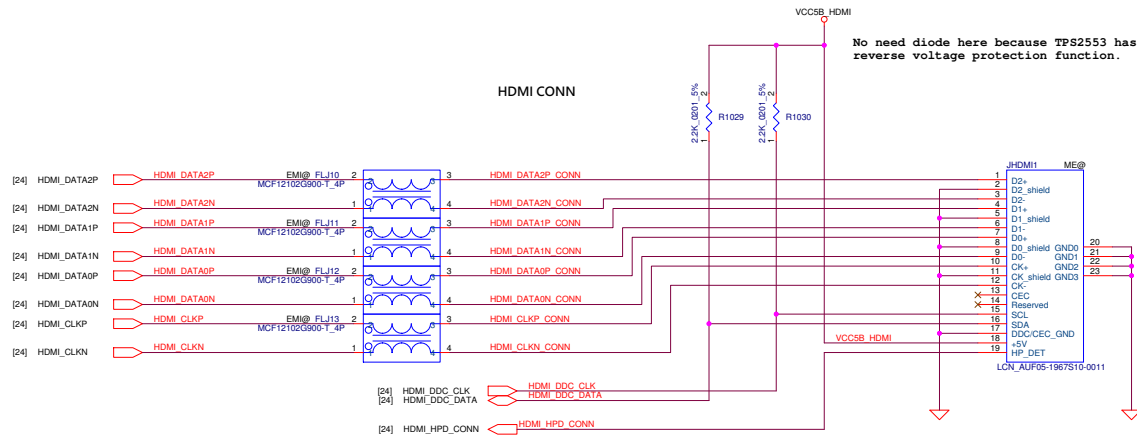
PEQ (INT PD)	R1875	R1897	
HEQ 15dB	ASM	NO_ASM	
LLEQ 5dB	ASM	ASM	
LLEQ 12dB	NO_ASM	NO_ASM	← LOGIC

TMDS PRE (INT PD)	R1877	R1899	
1.5dB	ASM	NO_ASM	
3.0dB	ASM	ASM	← LOGIC
0dB	NO_ASM	NO_ASM	

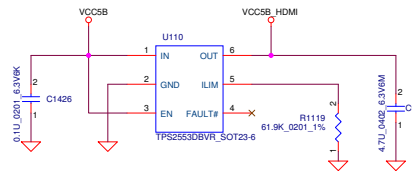
MODE (INT PD)	R146	R147	
Auto HDMI ID disable	ASM	NO_ASM	
Auto HDMI ID enable	ASM	ASM	← LOGIC
Control HDMI ID disable	NO_ASM	NO_ASM	

TMDS RT (INT PD)	R2509		
OD w/ termination	ASM		
OD	NO_ASM		← LOGIC

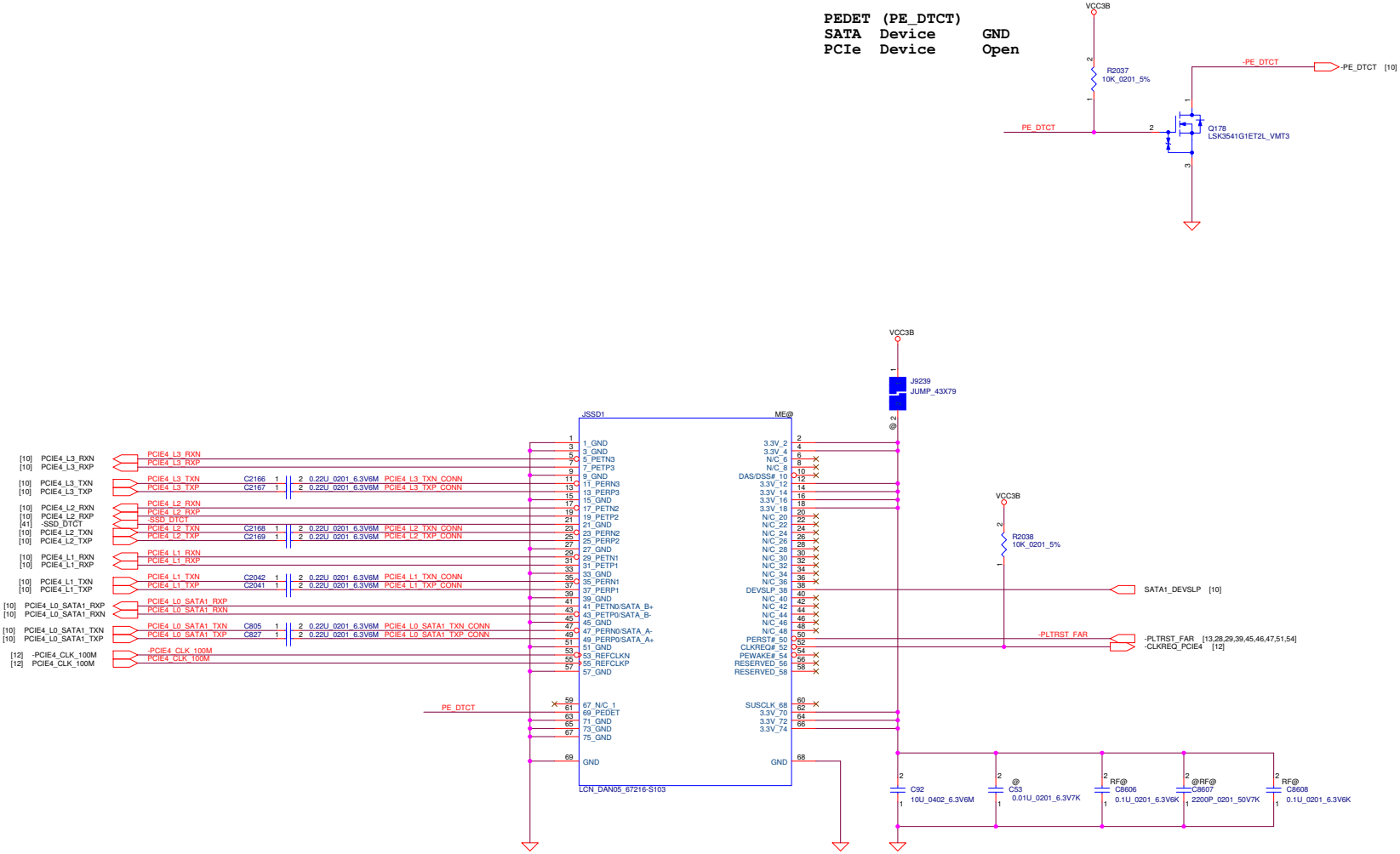
Vendor suggest to @



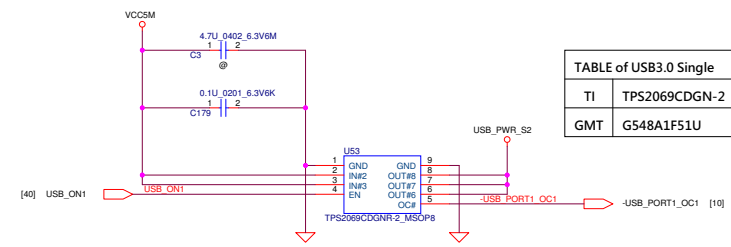
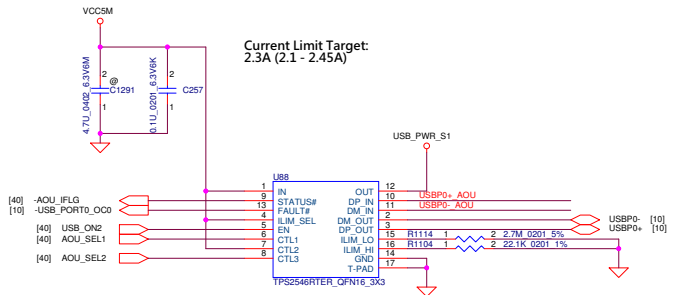
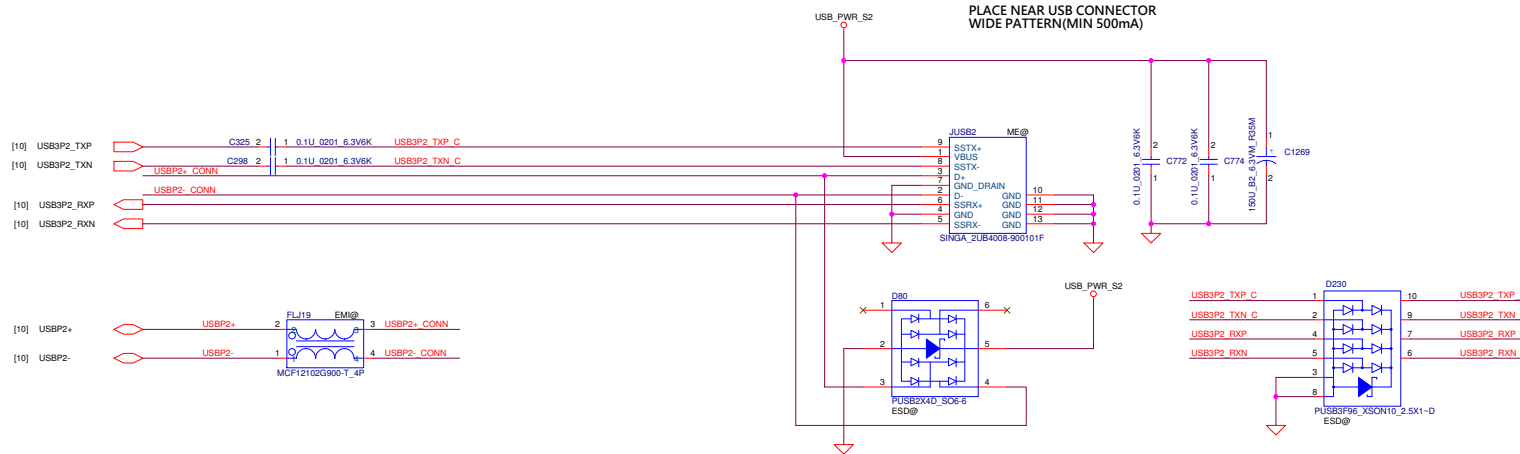
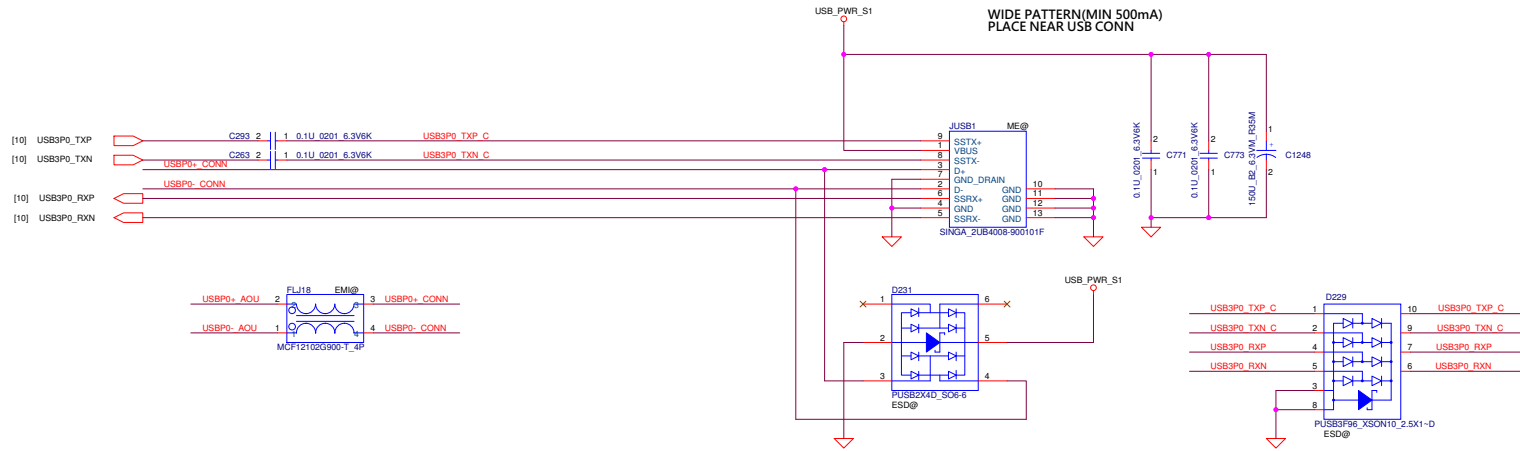
Current Limit Target : 400mA
 Requirement : 300mA
 HDMI Spec : 50mA - 500mA



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Date: Thursday, September 01, 2016				Sheet 25 of 75

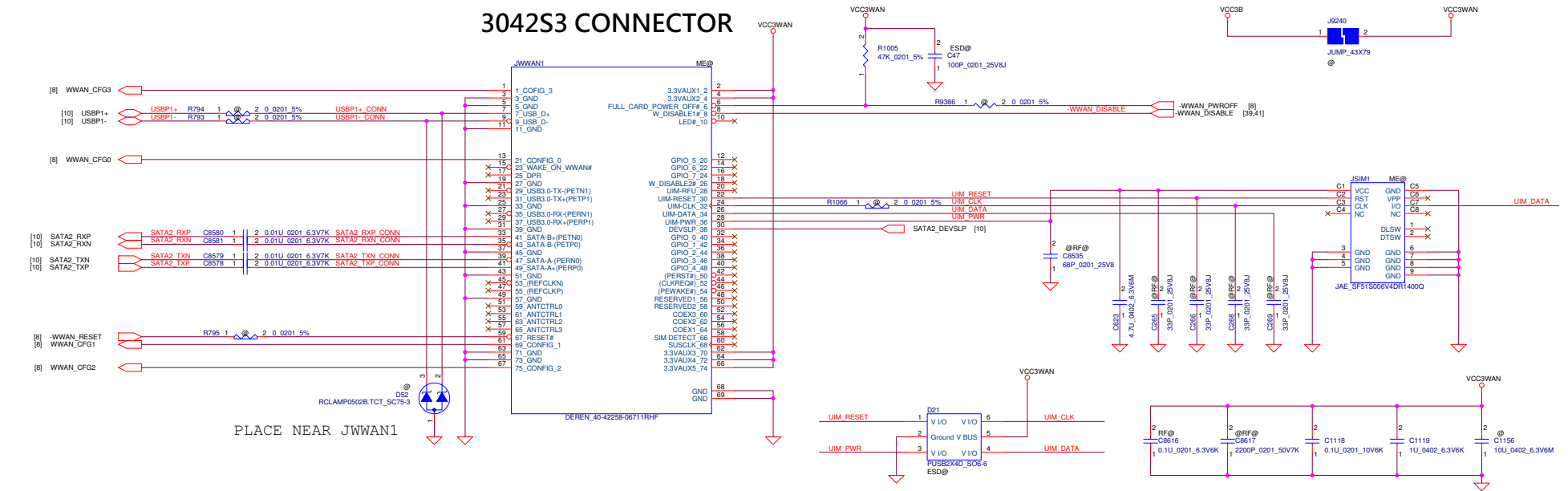


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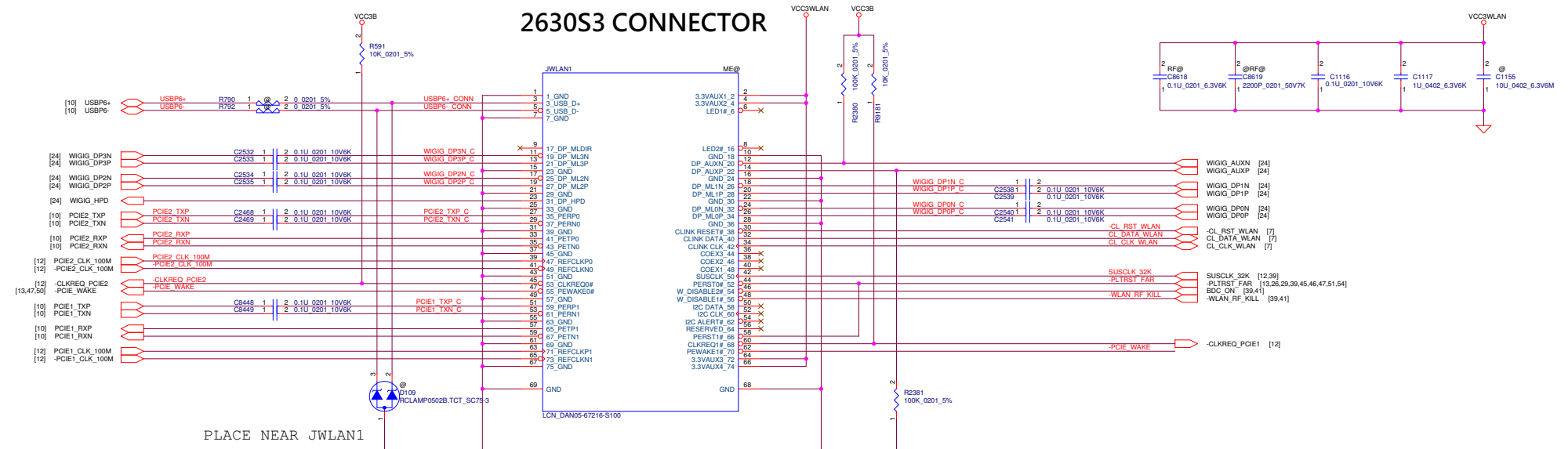
TYPE-B M.2 CARD FOR WWAN

3042S3 CONNECTOR

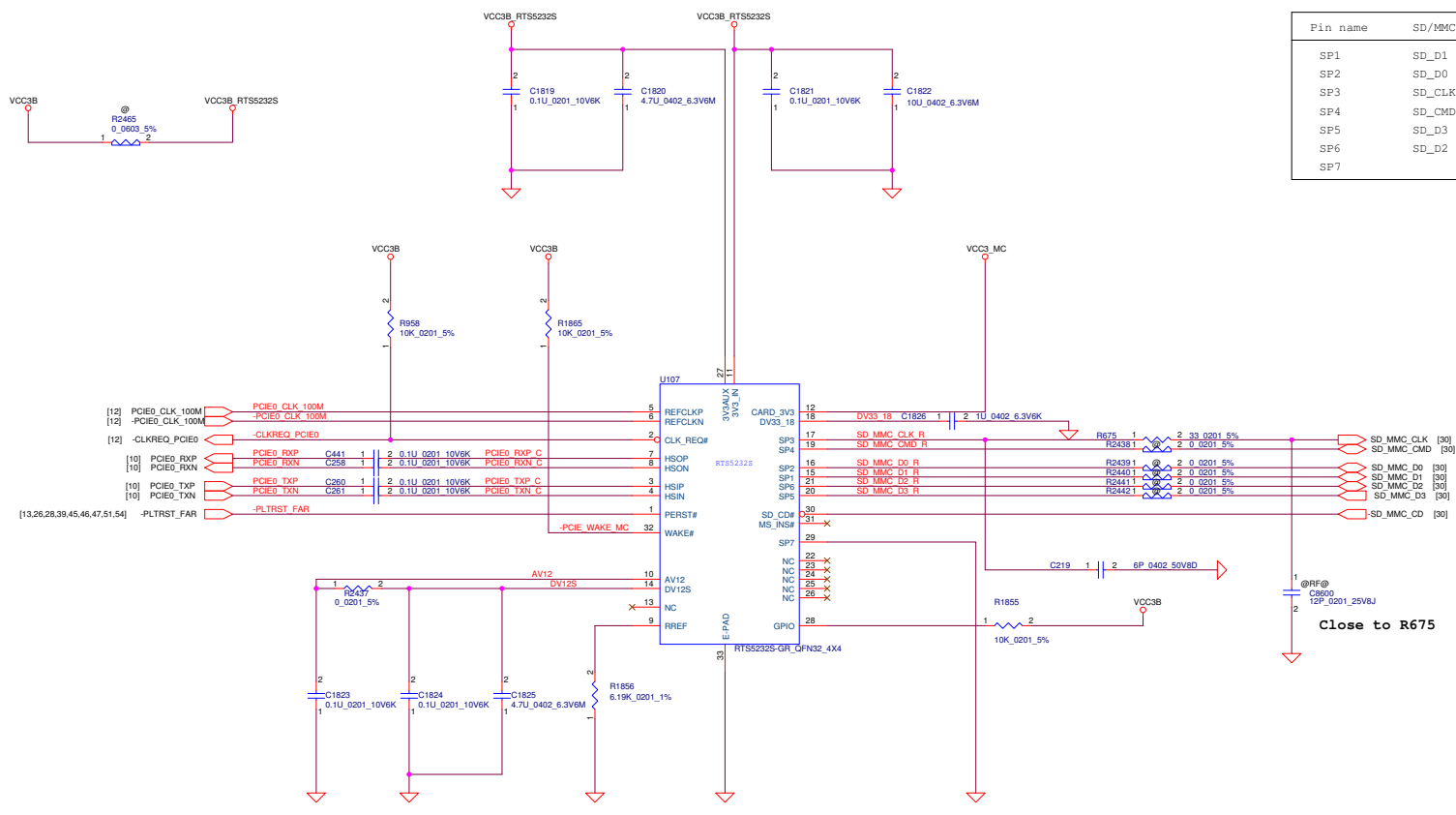


TYPE-A M.2 CARD FOR WLAN / Bluetooth / WiGig

2630S3 CONNECTOR



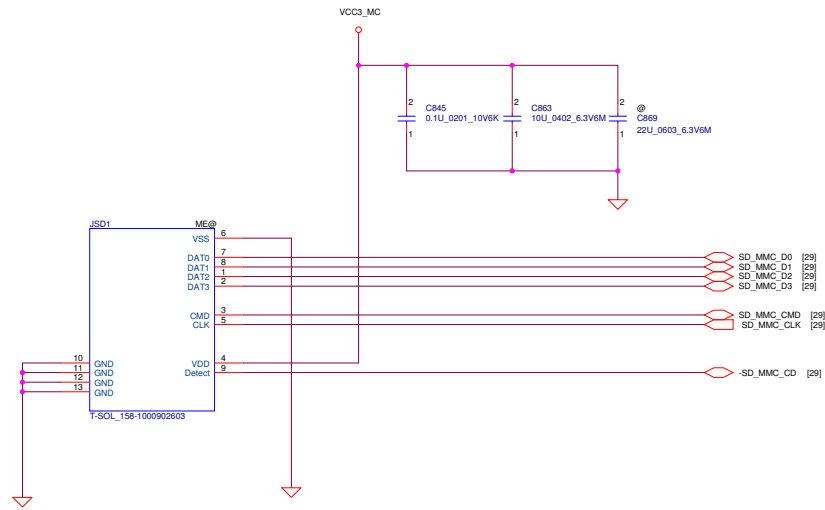
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	PCIE M.2 CARD SLOT
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Date: Thursday, September 01, 2016				Sheet 28 of 75



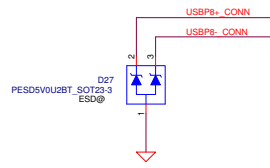
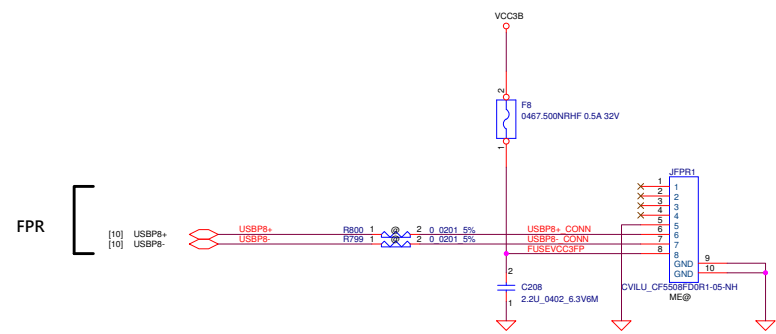
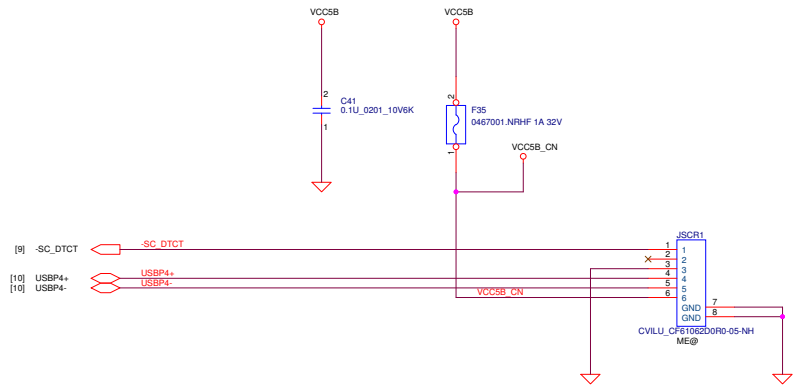
TABLE

Pin name	SD/MMC	MEMORSTICK
SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7		

Close to R675



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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title MEDIA CARD INTERFACE	
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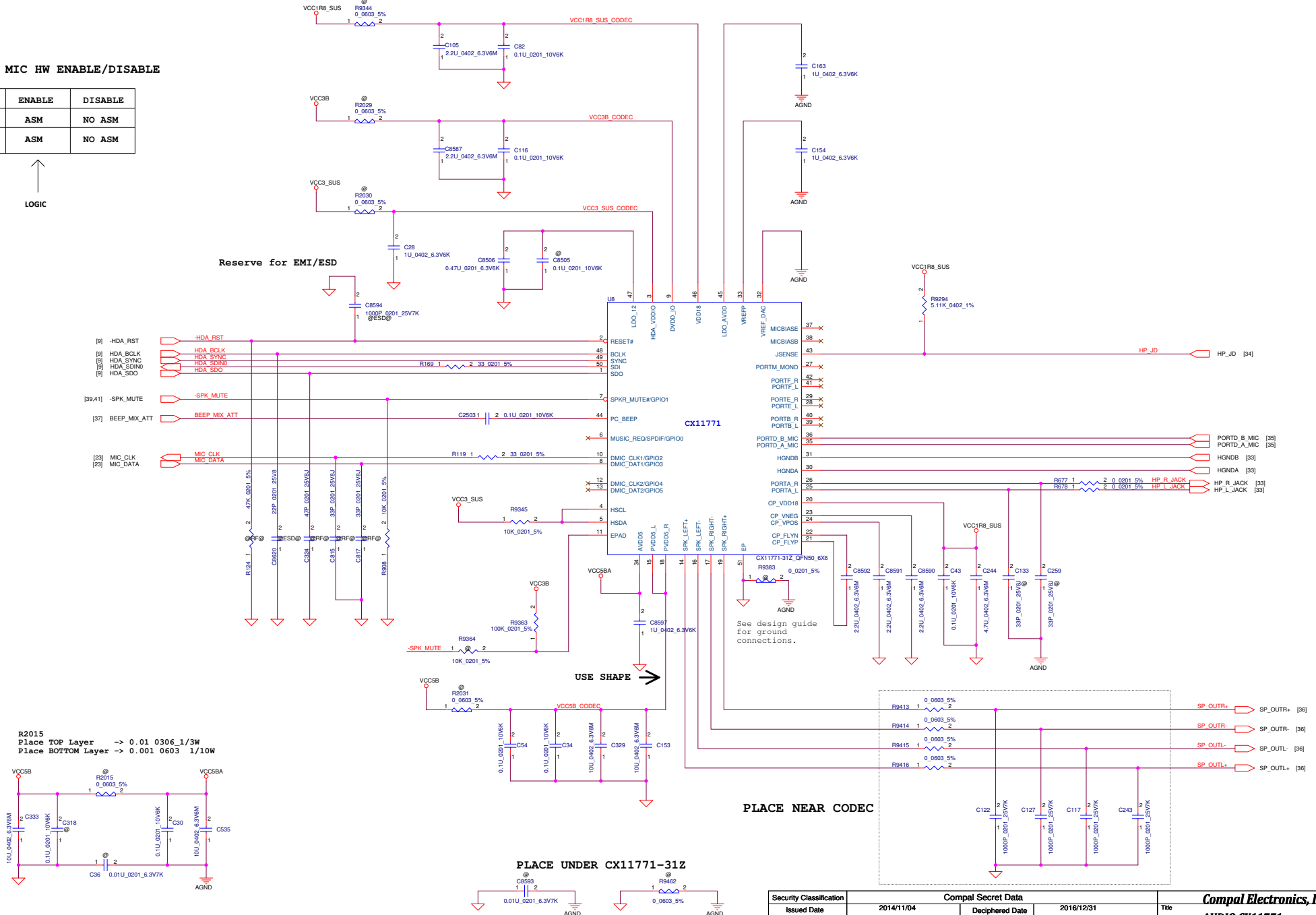


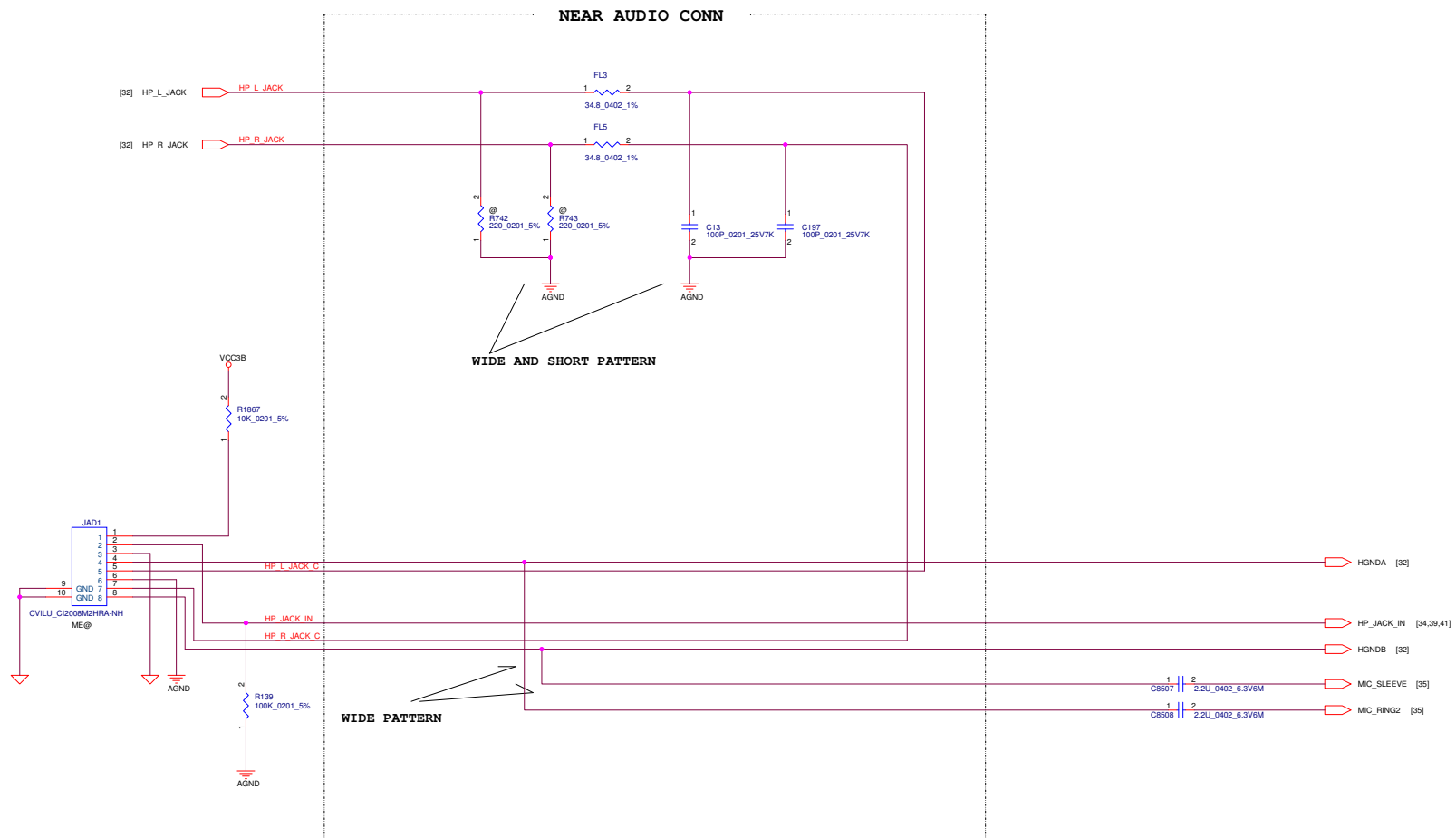
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	SMART CARD/FPR
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TABLE MIC HW ENABLE/DISABLE

	ENABLE	DISABLE
R961	ASM	NO ASM
R119	ASM	NO ASM

↑
LOGIC



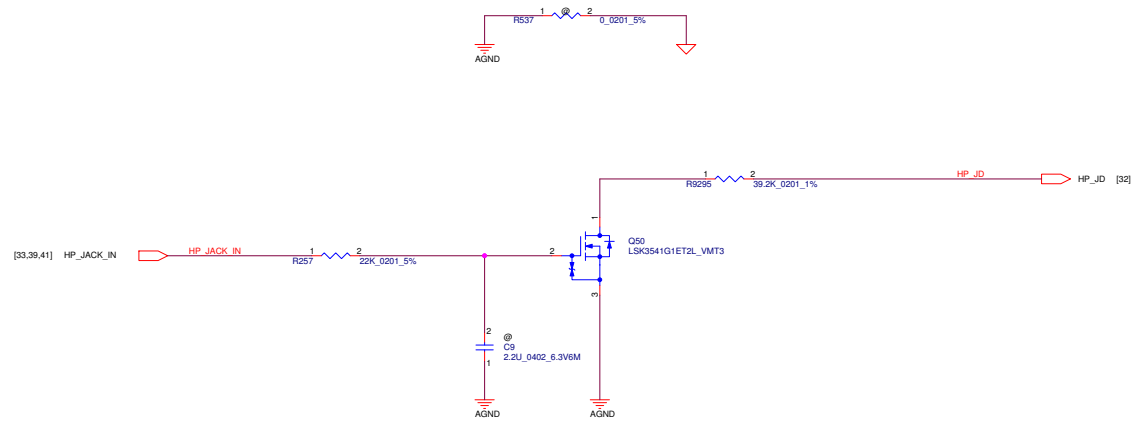


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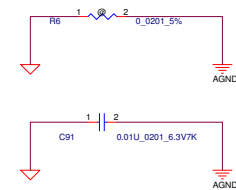
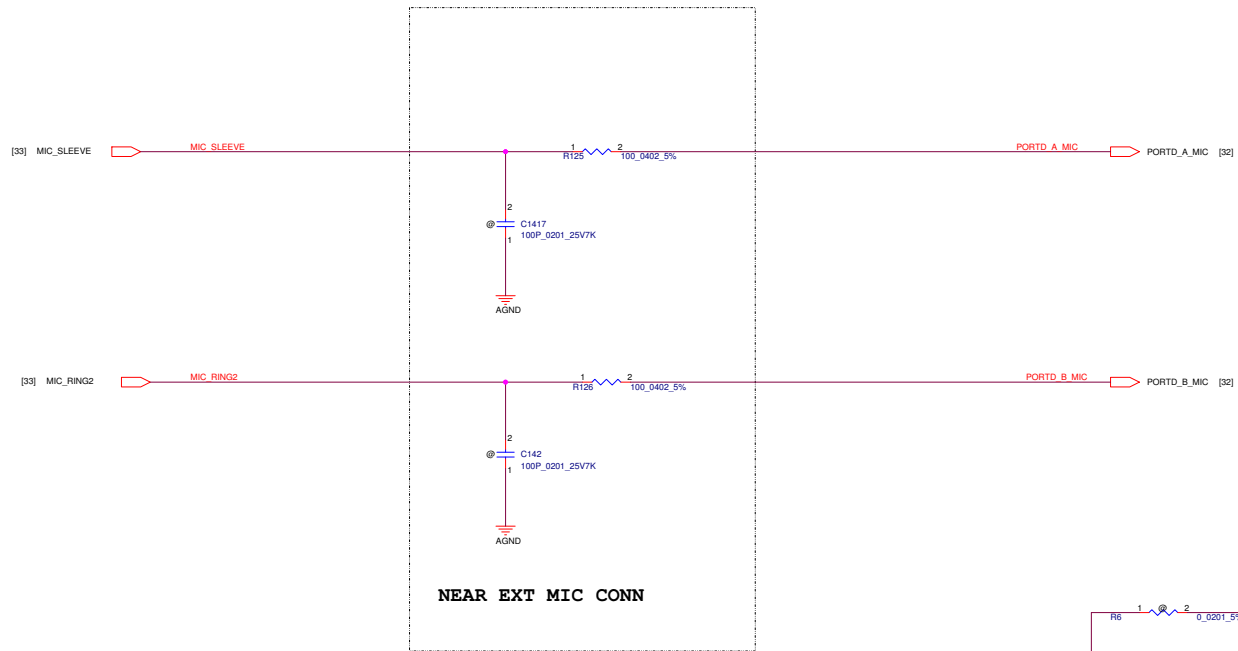
Compal Electronics, Inc.

AUDIO CONNECTOR

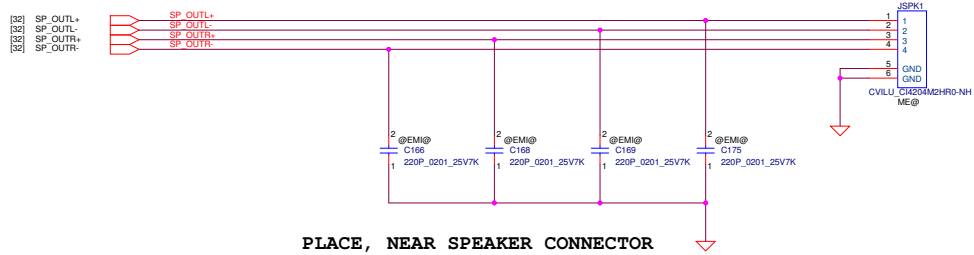
LA-E291P



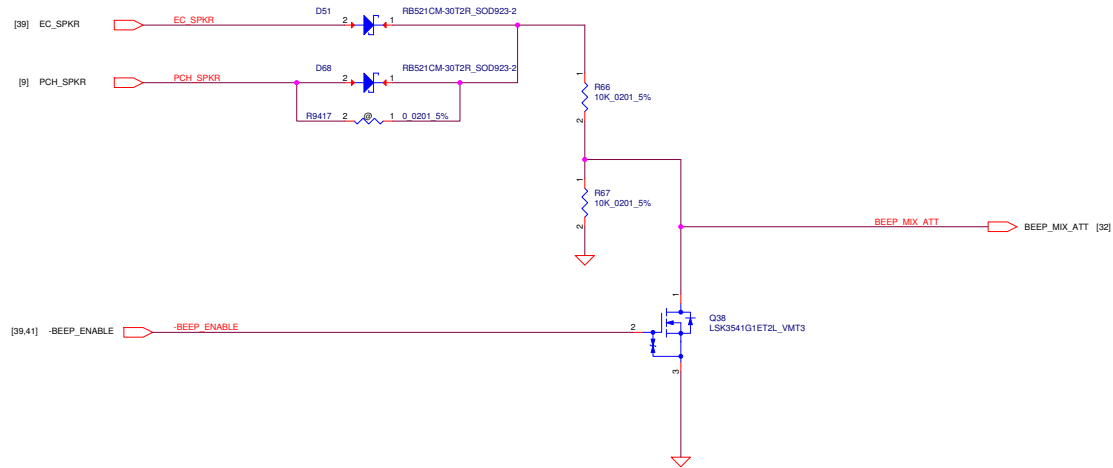
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	AUDIO JACK SENSE
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			Document Number LA-E291P	Compal Electronics, Inc.



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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Document Number		Rev
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				Date		Thursday, September 01, 2016
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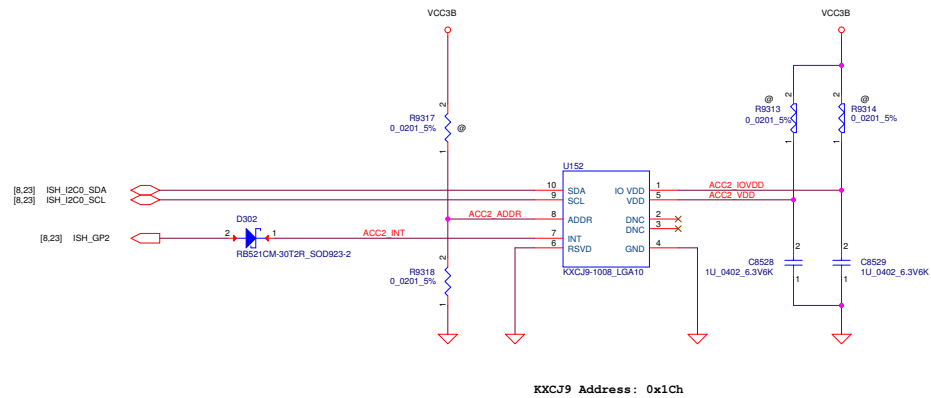
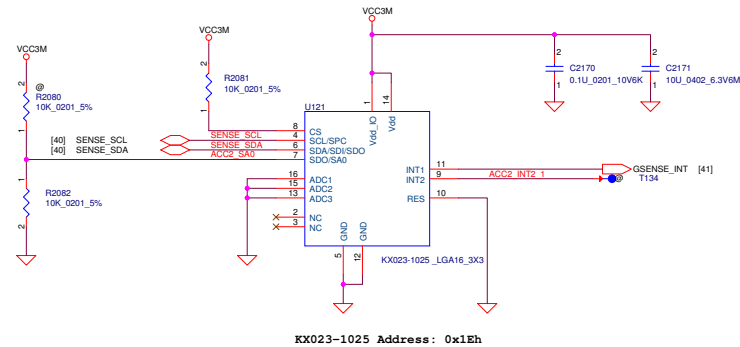
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				Date:	Thursday, September 01, 2016	Sheet 37 of 75

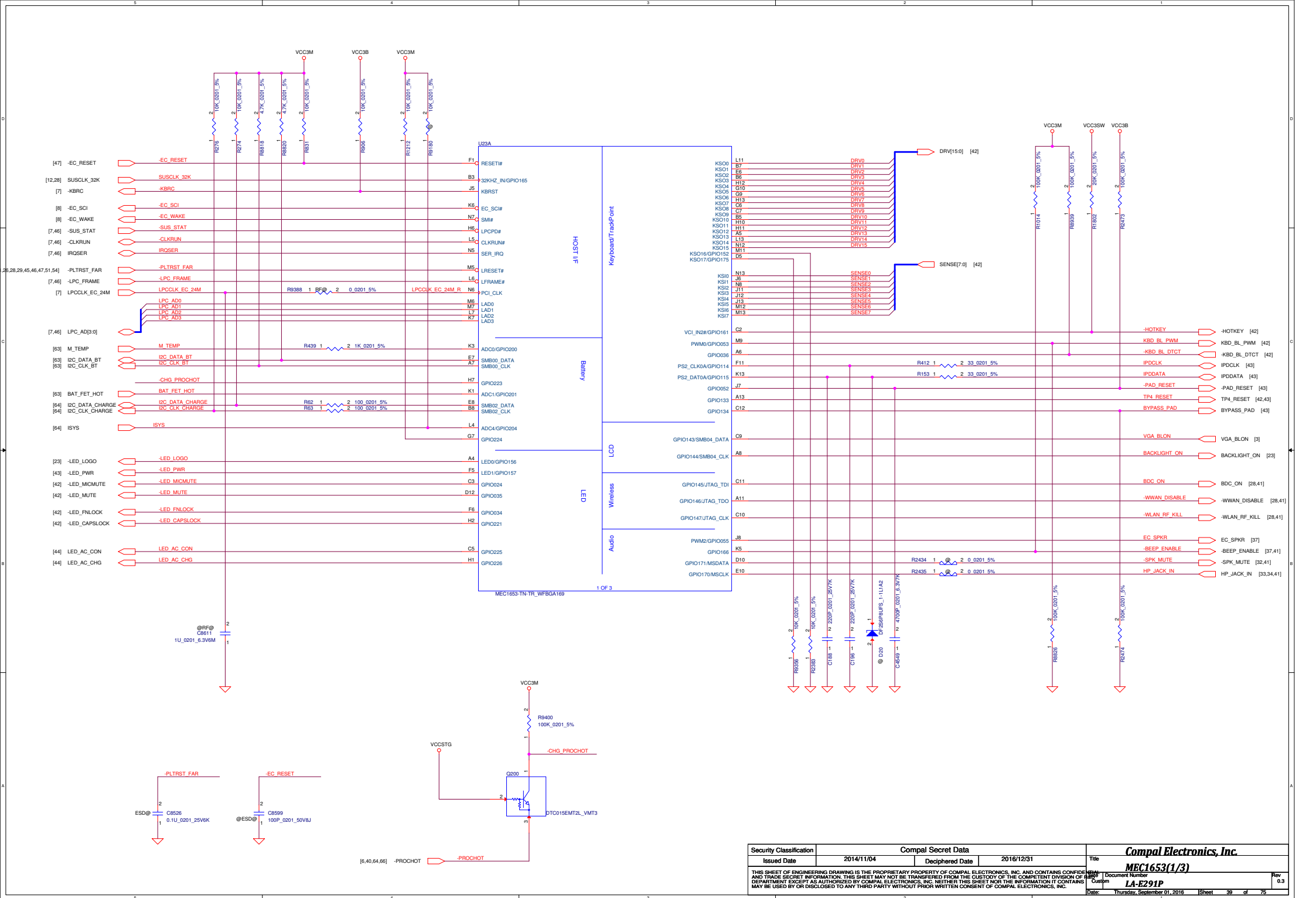
TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

TABLE

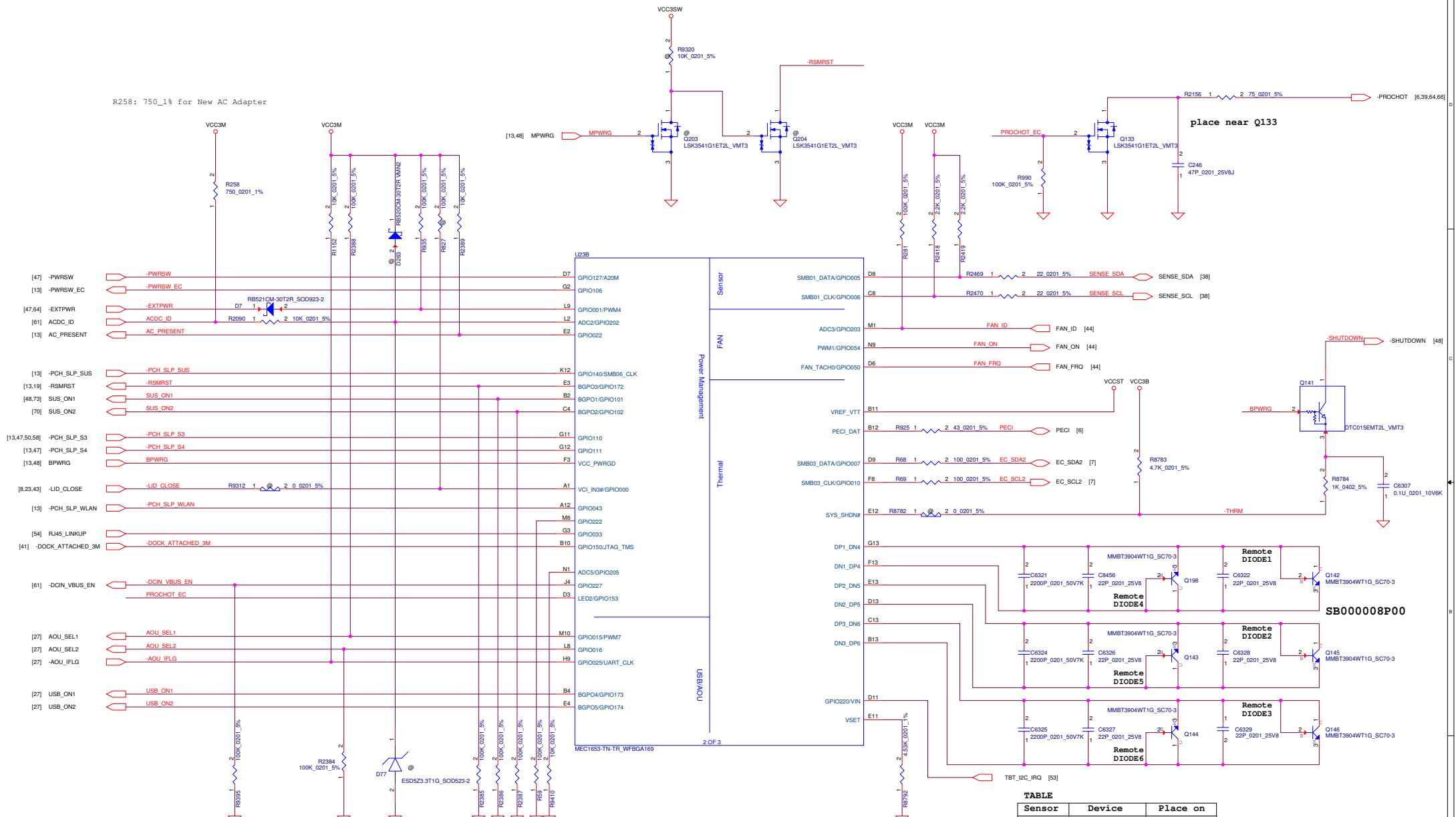
ACC2_SA0	Address Selection
H	32h (W) & 33h (R)
L	30h (W) & 31h (R)





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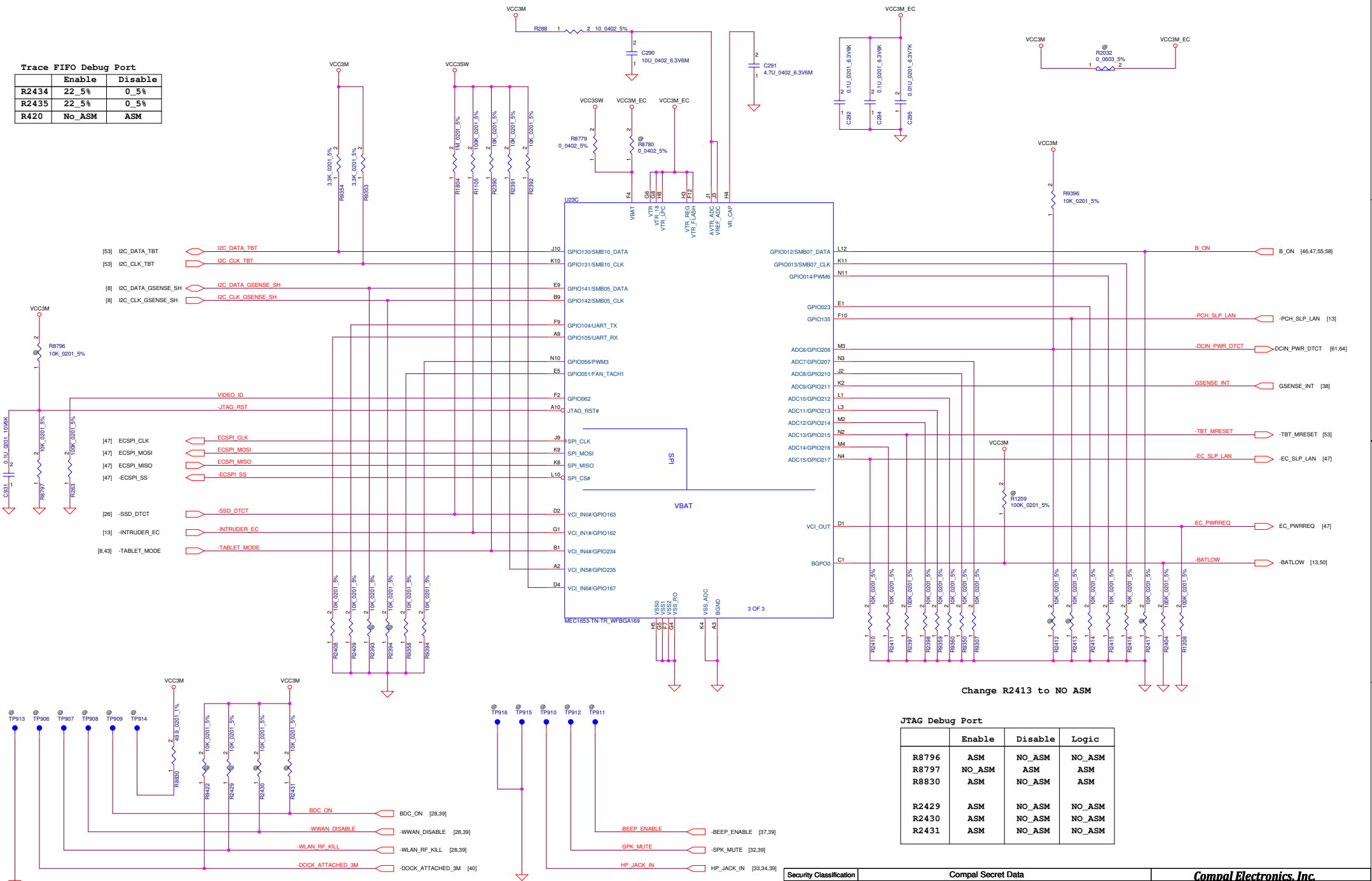
R258: 750_1% for New AC Adapter

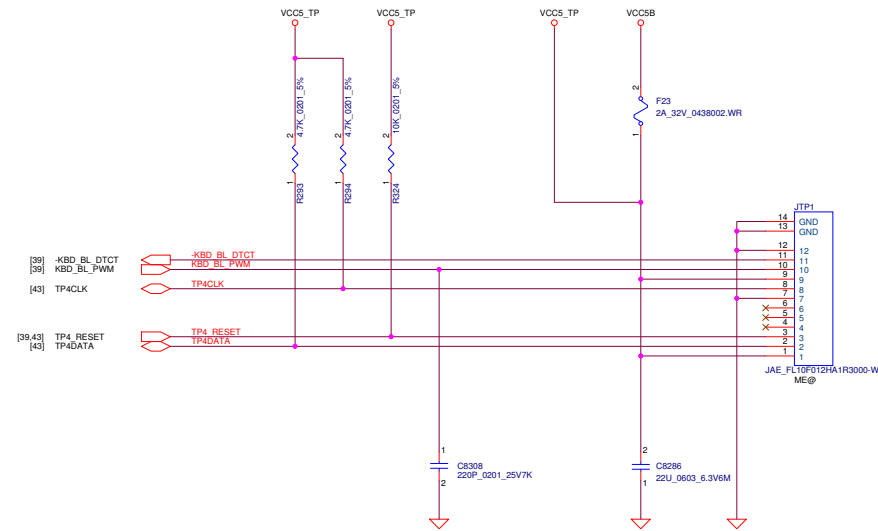
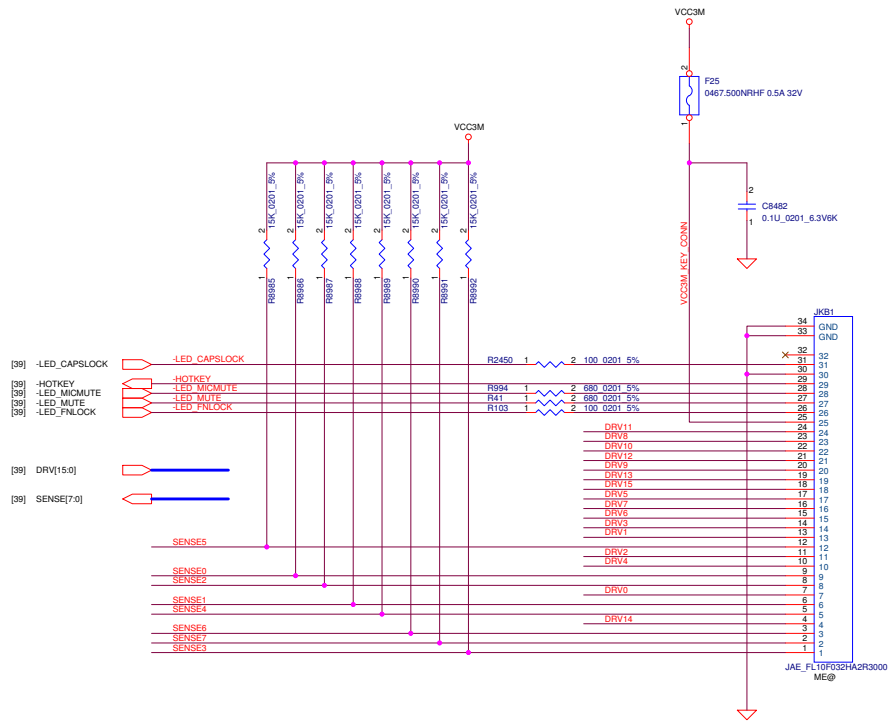


TABLE

Sensor	Device	Place on
DIODE0	EC internal	TOP
DIODE1	CPU DC/DC	BOTTOM
DIODE2	SSD	BOTTOM
DIODE3	DIMM	BOTTOM
DIODE4	FAN/HEATPIPE	BOTTOM
DIODE5	WLAN/WWAN	BOTTOM
DIODE6	CHARGER	BOTTOM

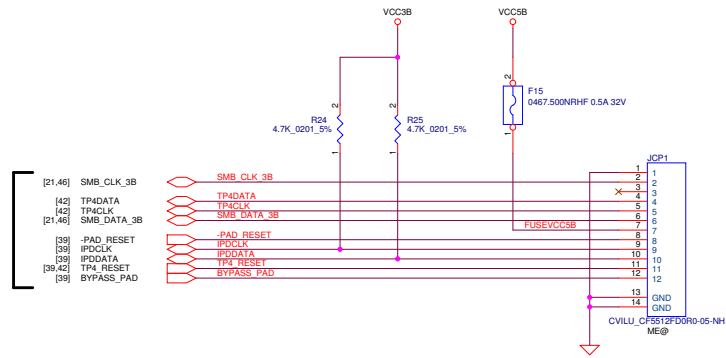
Trace FIFO Debug Port		
	Enable	Disable
R2434	22.5%	0.5%
R2435	22.5%	0.5%
R420	No_ASM	ASM



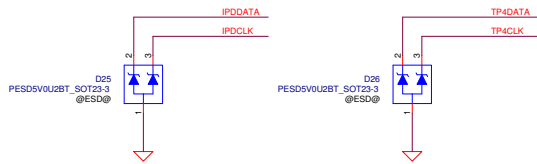
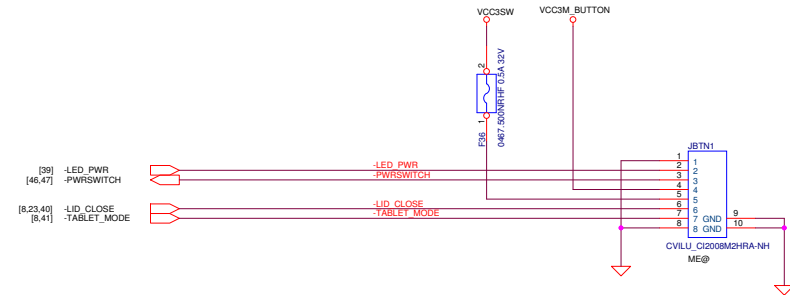
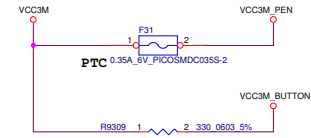


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				Date	Thursday, September 01, 2016
				Sheet	42 of 75

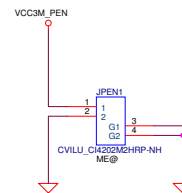
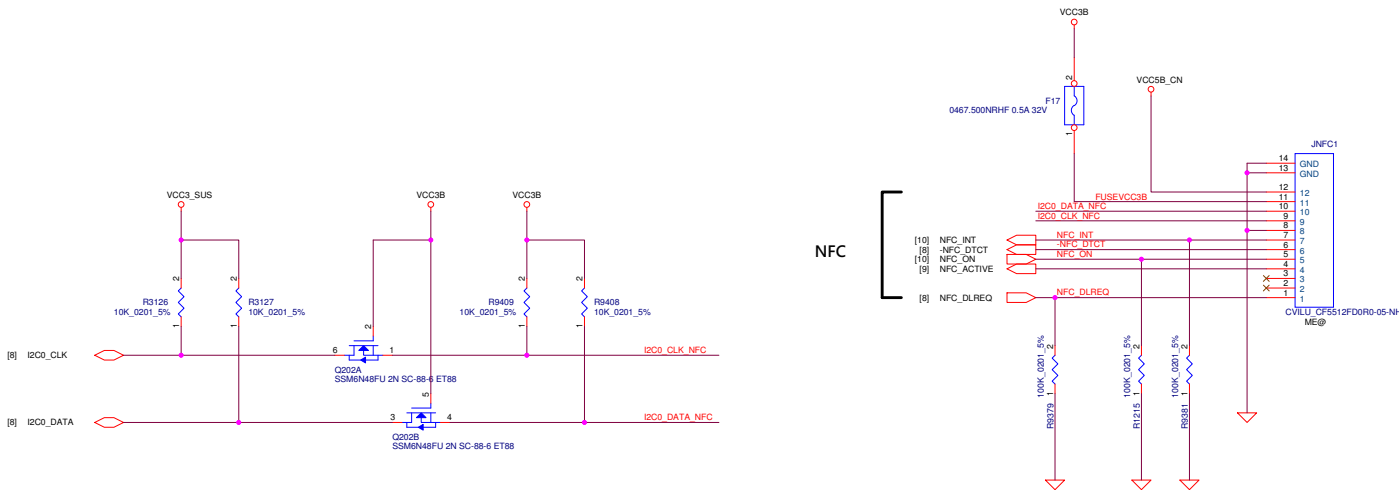
Clickpad



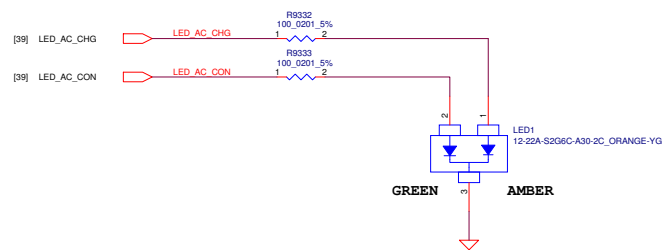
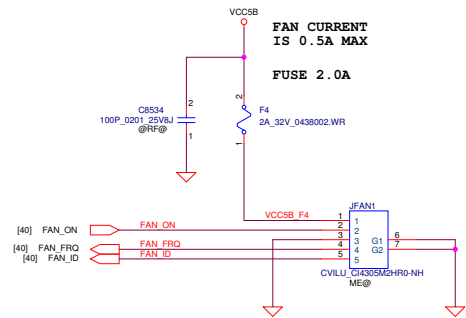
TO SUB BOARD



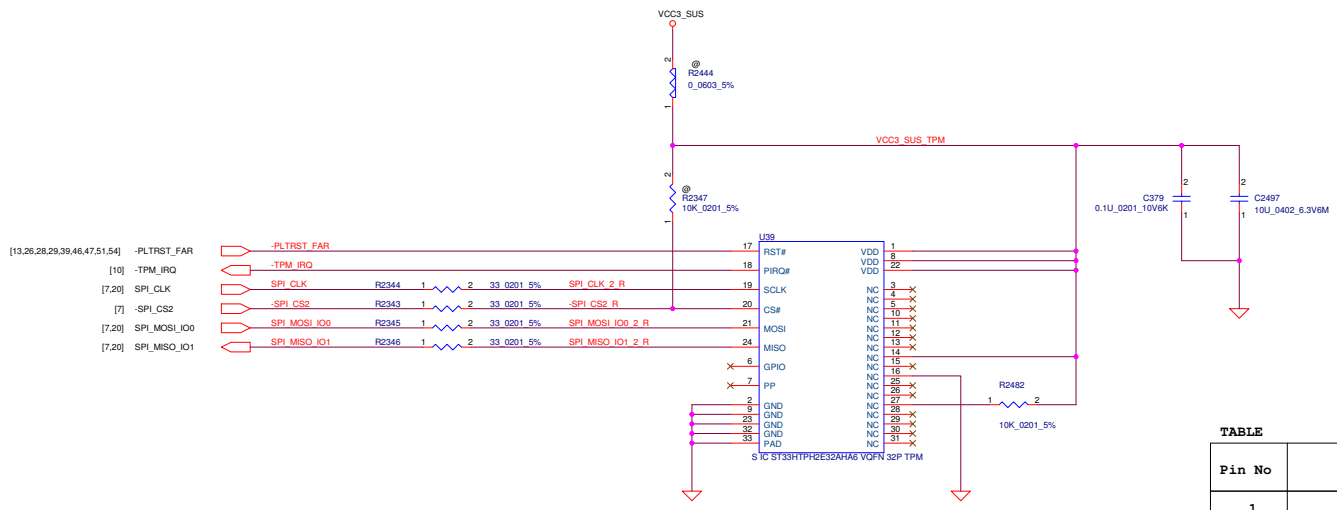
NFC



Security Classification	Compal Secret Data		Title	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	TOUCH PAD/NFC/BUTTON/PEN I
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Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Document Number		FAN CONNECTOR/LED
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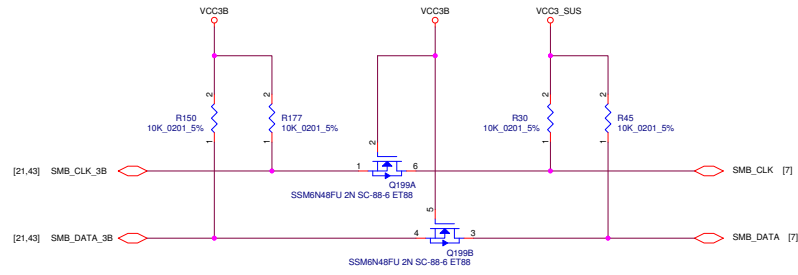
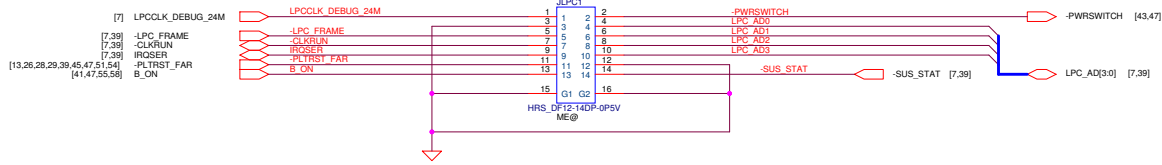
-Change TPM1.2 to TPM2.0
 -Infineon SLB9670VQ2.0 part number SA00009N210
 -ST ST33HTPH2E32AHA6 part number SA00009S010

TABLE

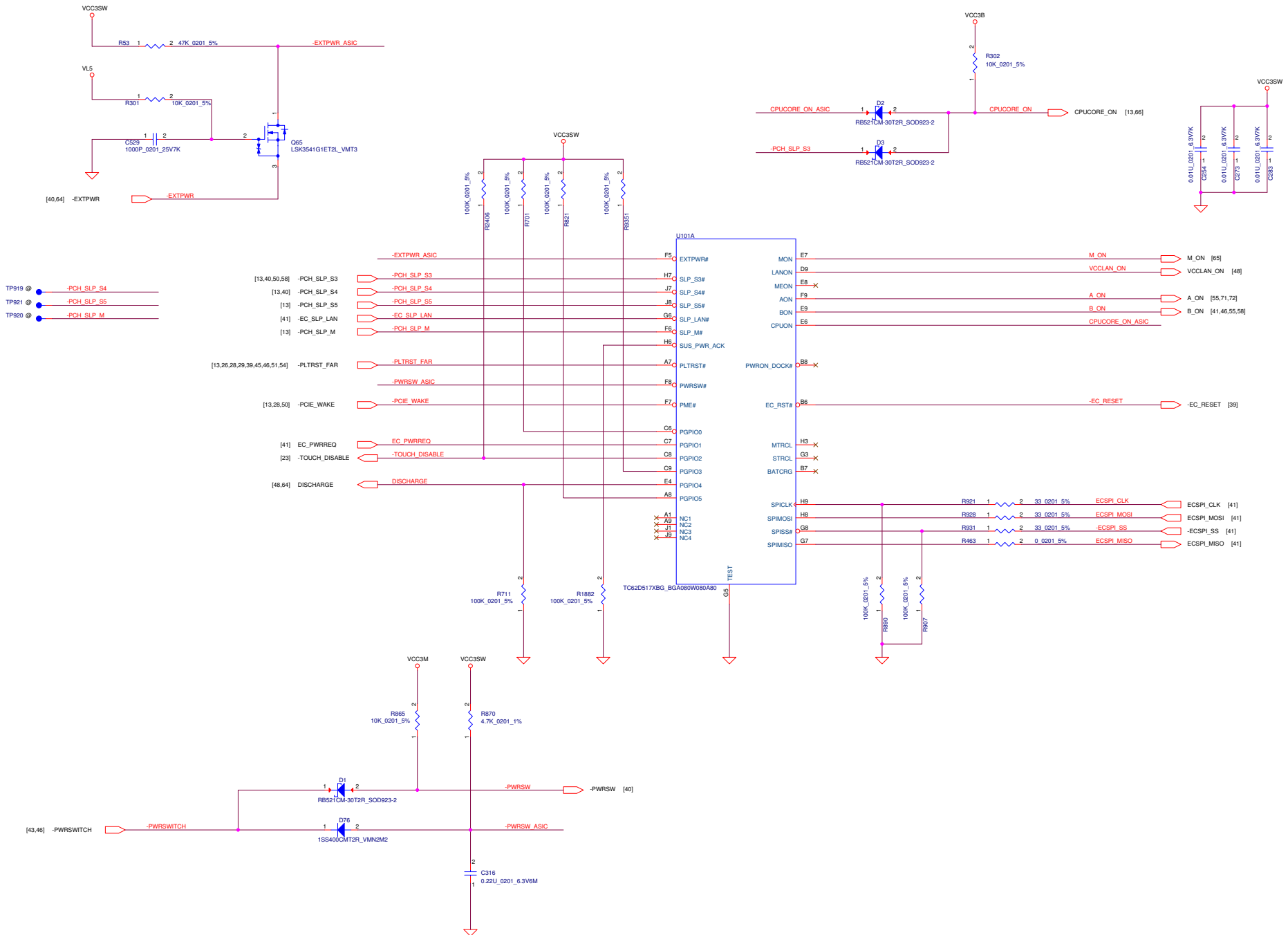
Pin No	ST ST33HTPH2E32AHA6	Infineon SLB9670VQ2.0 FW7.60
1	NC	VDD
2	GND	GND
3	NC	NC
4	NC	NC
5	NC	NC
6	NC	GPIO
7	PP	PP
8	NC	VDD
9	NC	GND
10	NC	NC
11	NC	NC
12	NC	NC
13	NC	NC
14	NC	VDD
15	NC	NC
16	NC	GND
17	SPI_RST#	RST#
18	SPI_PIRQ#	PIRQ#
19	SPI_CLK	SCLK
20	SPI_CS#	CS#
21	MOSI	MOSI
22	VDD	VDD
23	NC	GND
24	MISO	MISO
25	NC	NC
26	NC	NC
27	NC	NC
28	NC	NC
29	NC	NC
30	NC	NC
31	NC	NC
32	NC	GND

REF DES	ENABLE	DISABLE
JLPC1	ASM	NO_ASM
R220	ASM	NO_ASM

↑
LOGIC

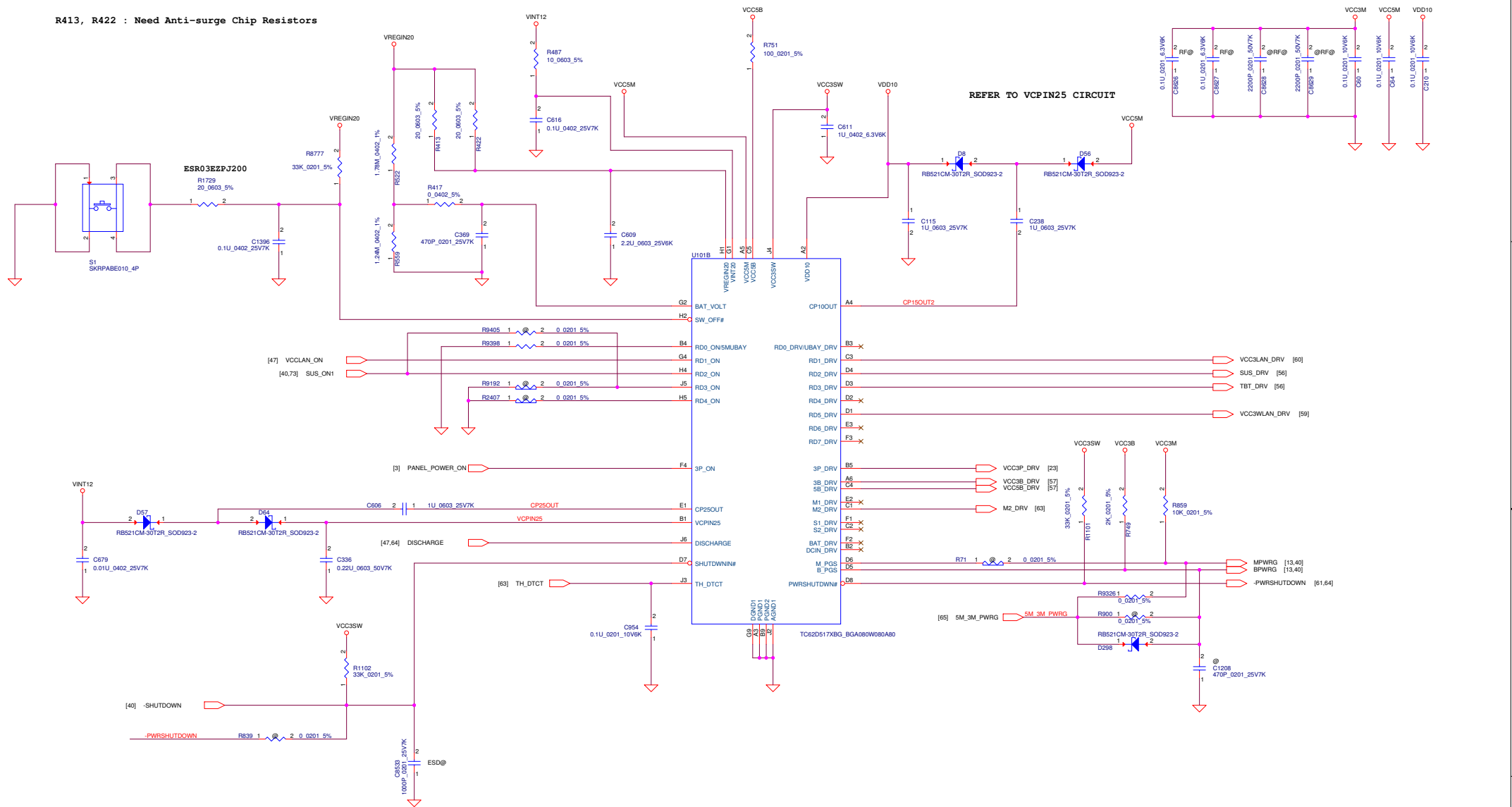


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Issued Date	2014/11/04	Deciphered Date	2016/12/31	THINK ENGINE(1/2)
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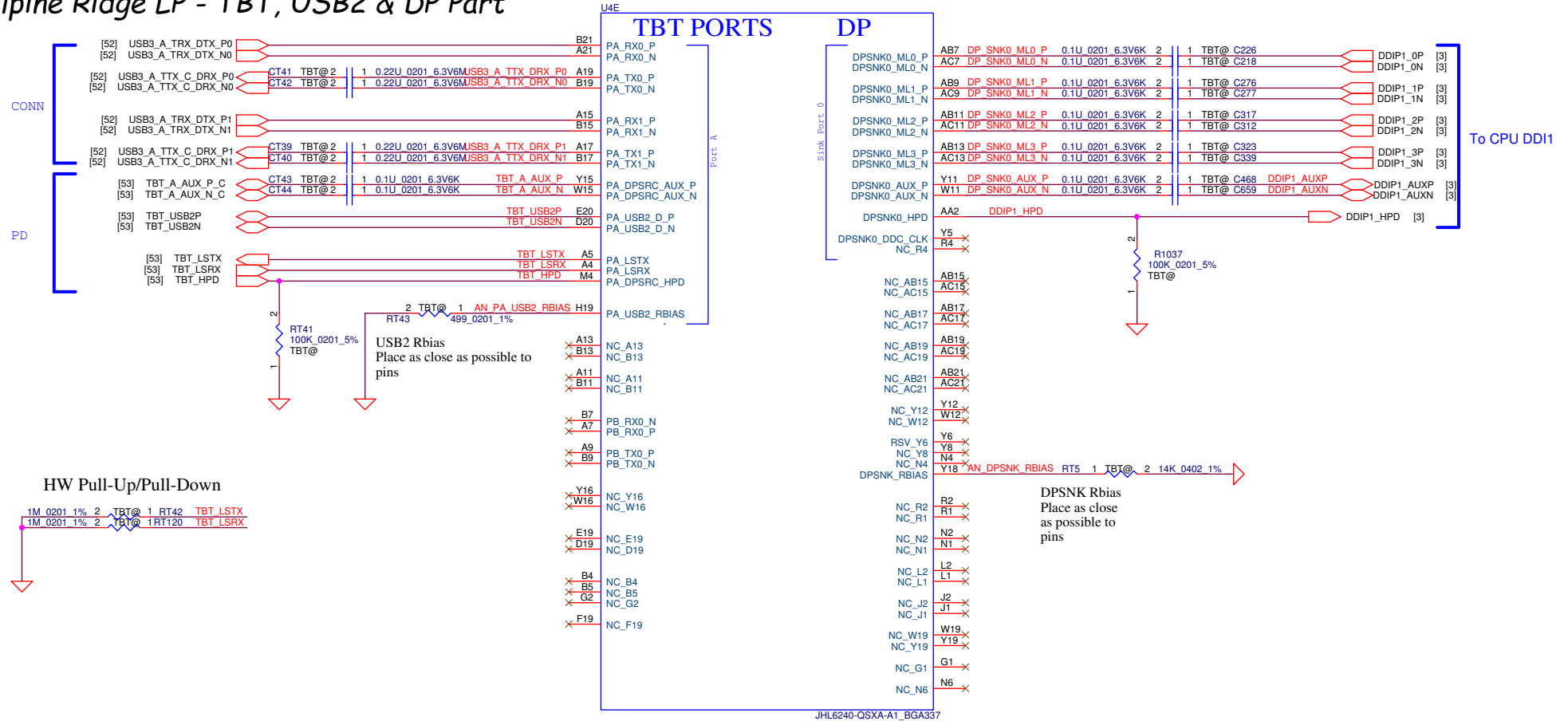
R413, R422 : Need Anti-surge Chip Resistors



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Alpine Ridge LP - TBT, USB2 & DP Part

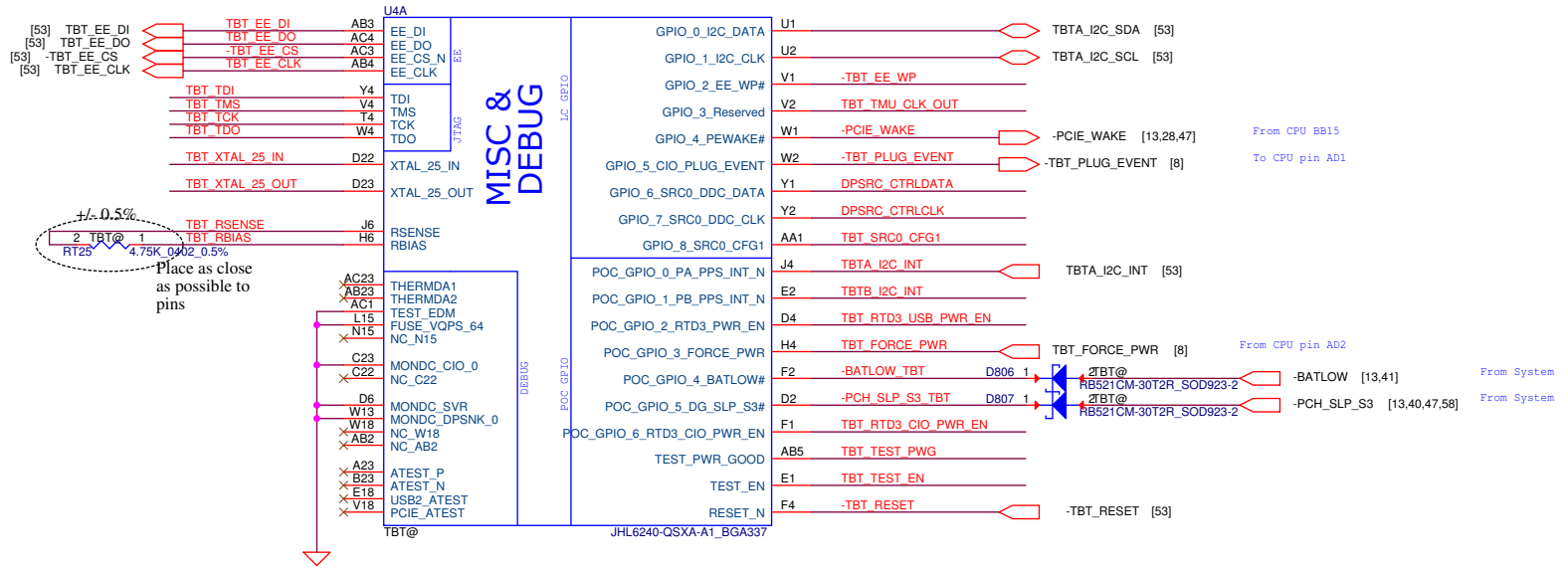
Alpine Ridge LP - TBT, USB2 & DP Part



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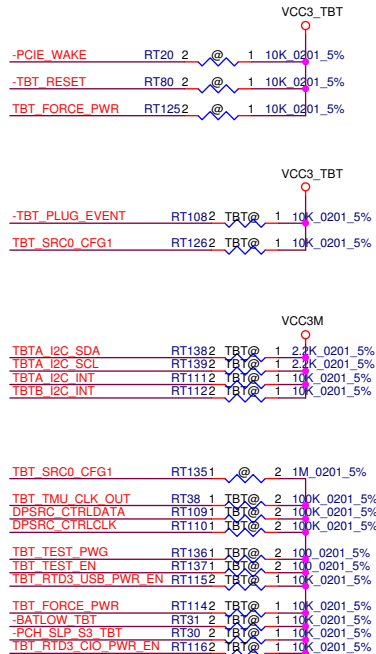
Alpine Ridge LP - Misc Part

Alpine Ridge LP - Misc
Symbol

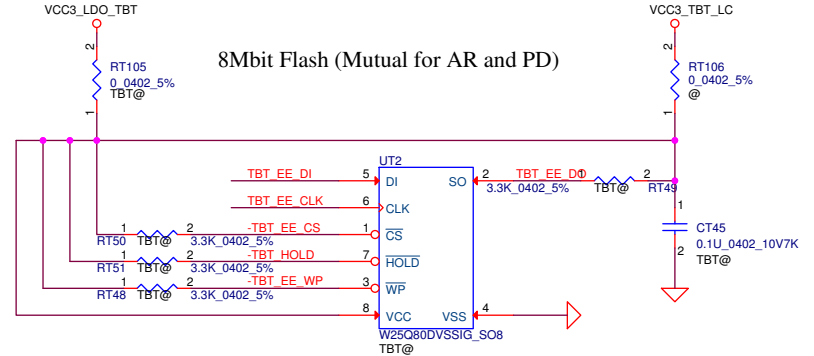


HW Pull-Up/Pull-Down

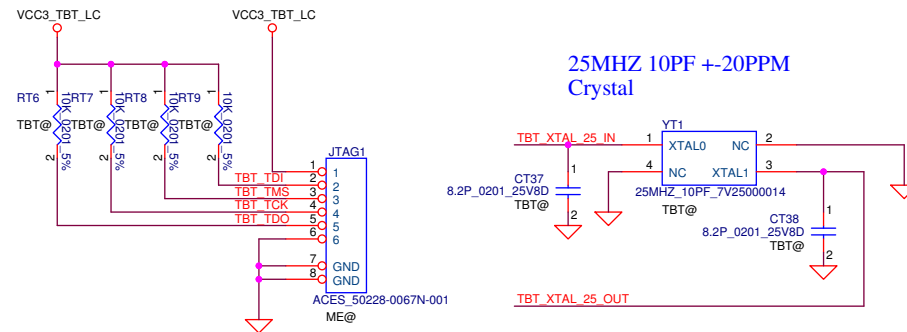
DG_SLP_S3#: PU should be on the Host side
DG_BATLOW#: PU should be on the Host side



8Mbit Flash (Mutual for AR and PD)



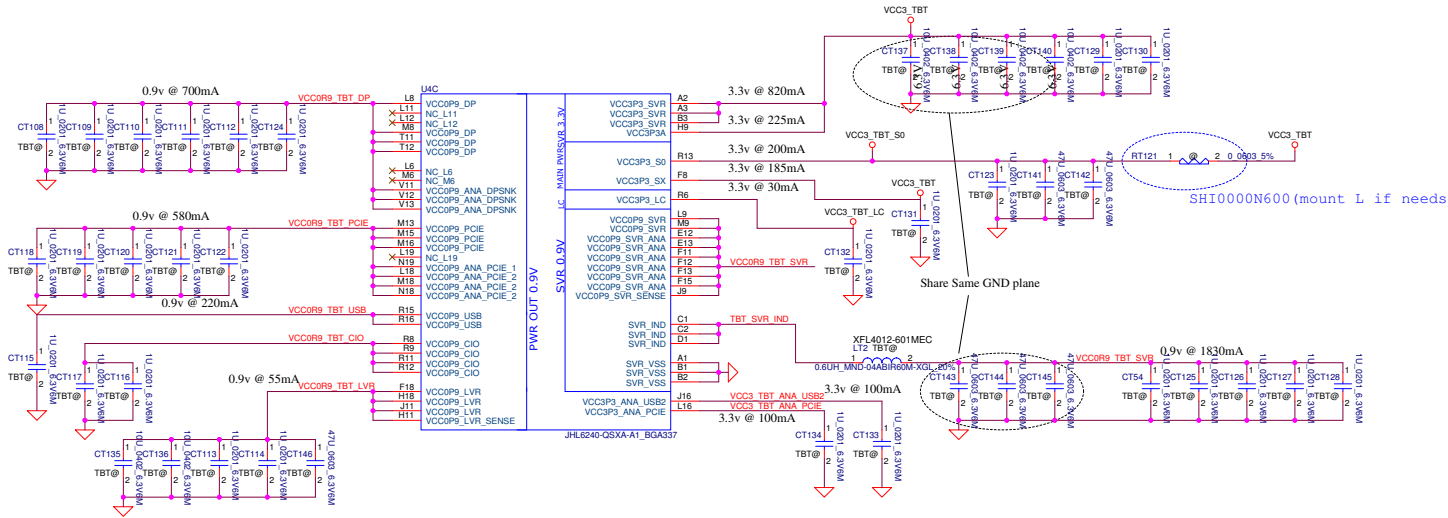
25MHZ 10PF +-20PPM Crystal



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Alpine Ridge LP - Power Supply

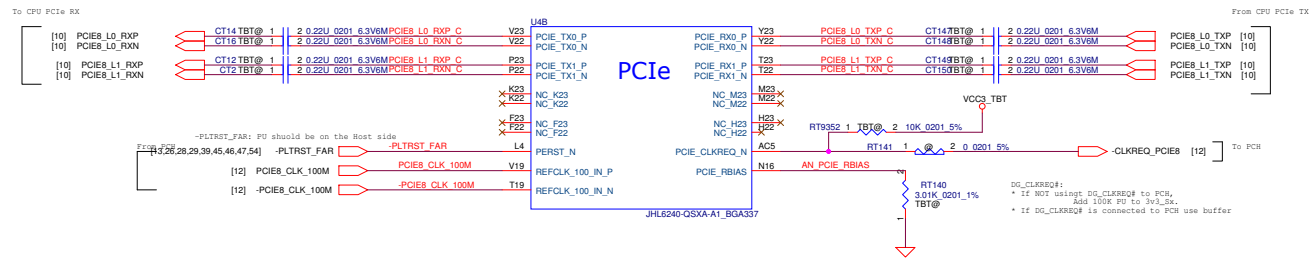
Alpine Ridge SP - VCC
Symbol



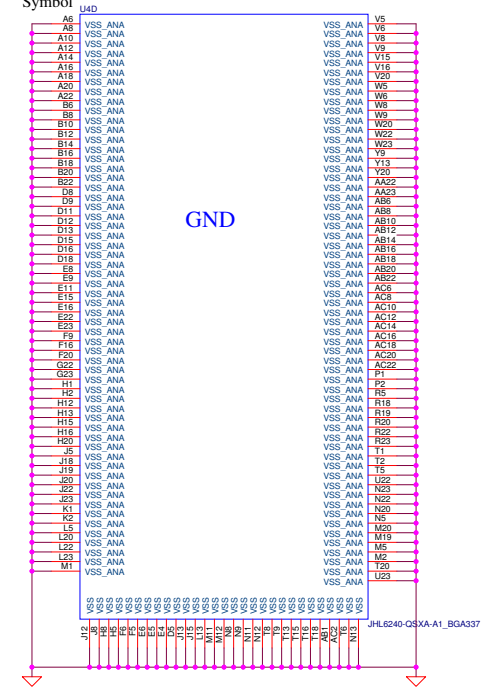
AR-LP Power & GND

AR-LP PCIE

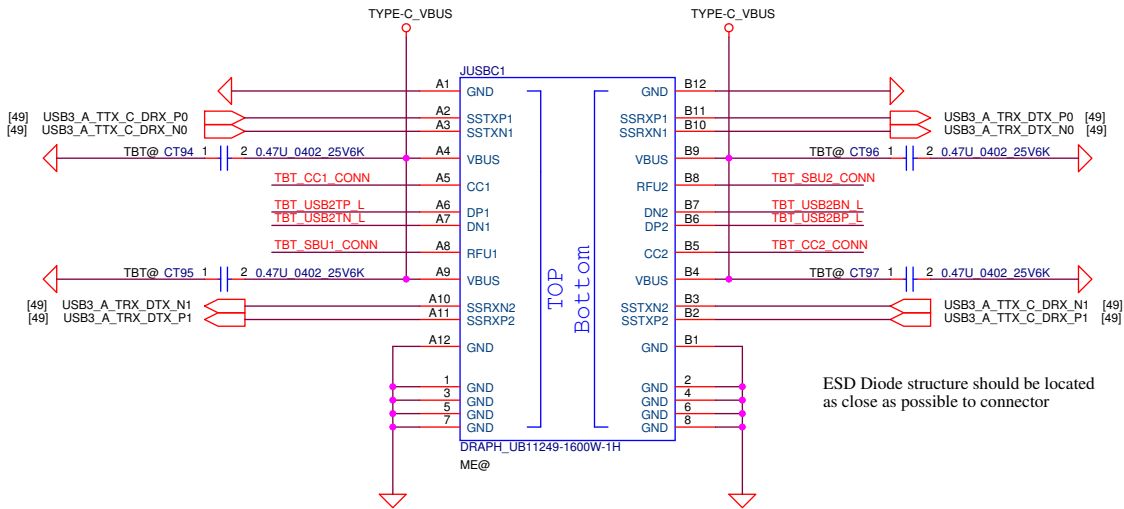
Alpine Ridge LP - PCIE Symbol



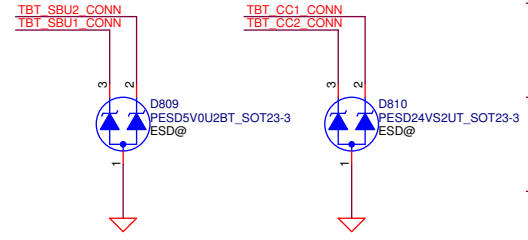
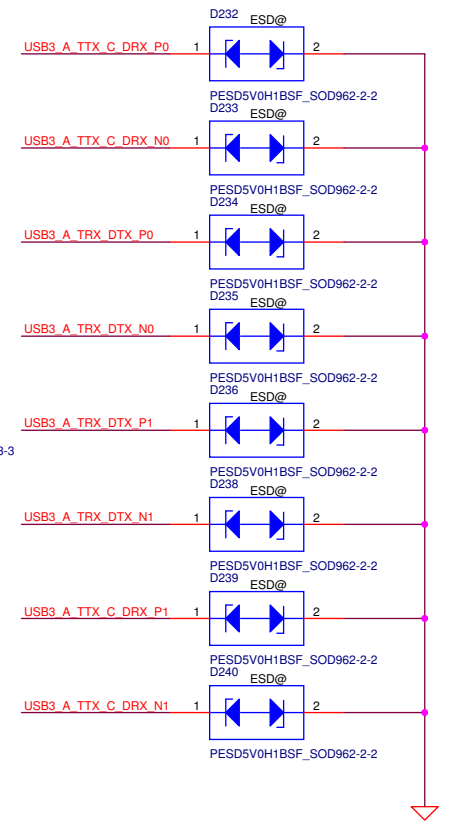
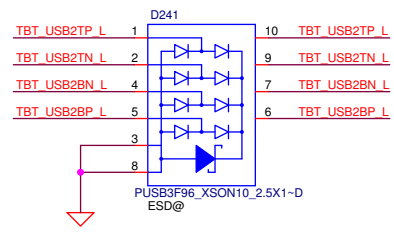
Alpine Ridge SP - GND Symbol



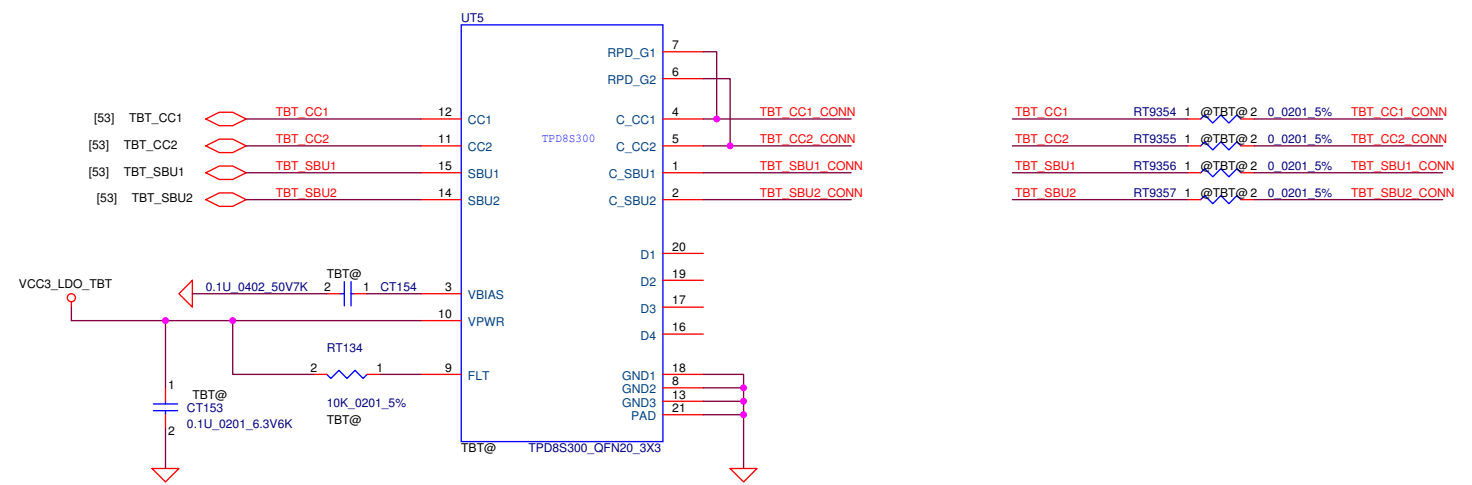
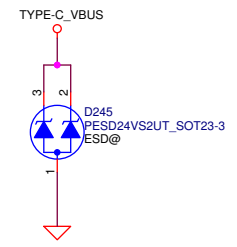
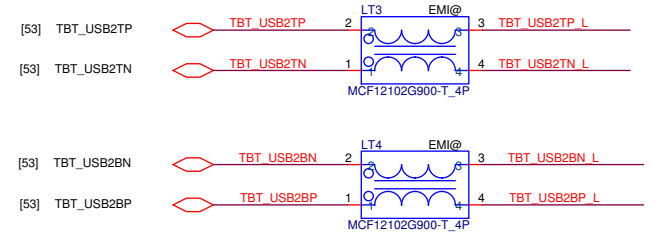
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	
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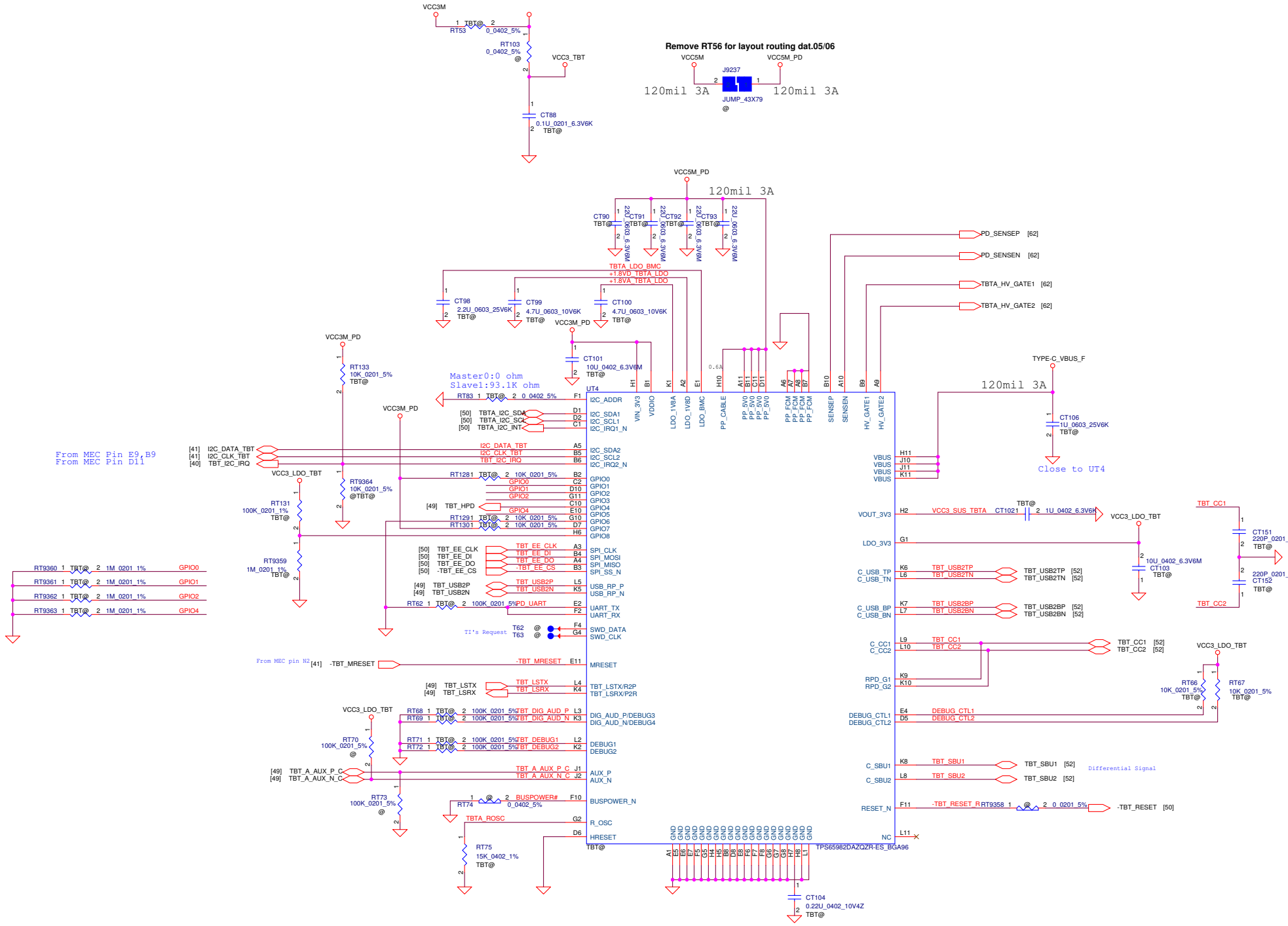
ESD for USB2 Lines and Control lines



ESD Diode structure should be located as close as possible to connector



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				Document Number	Rev
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From MEC Pin E9, B9
From MEC Pin D11

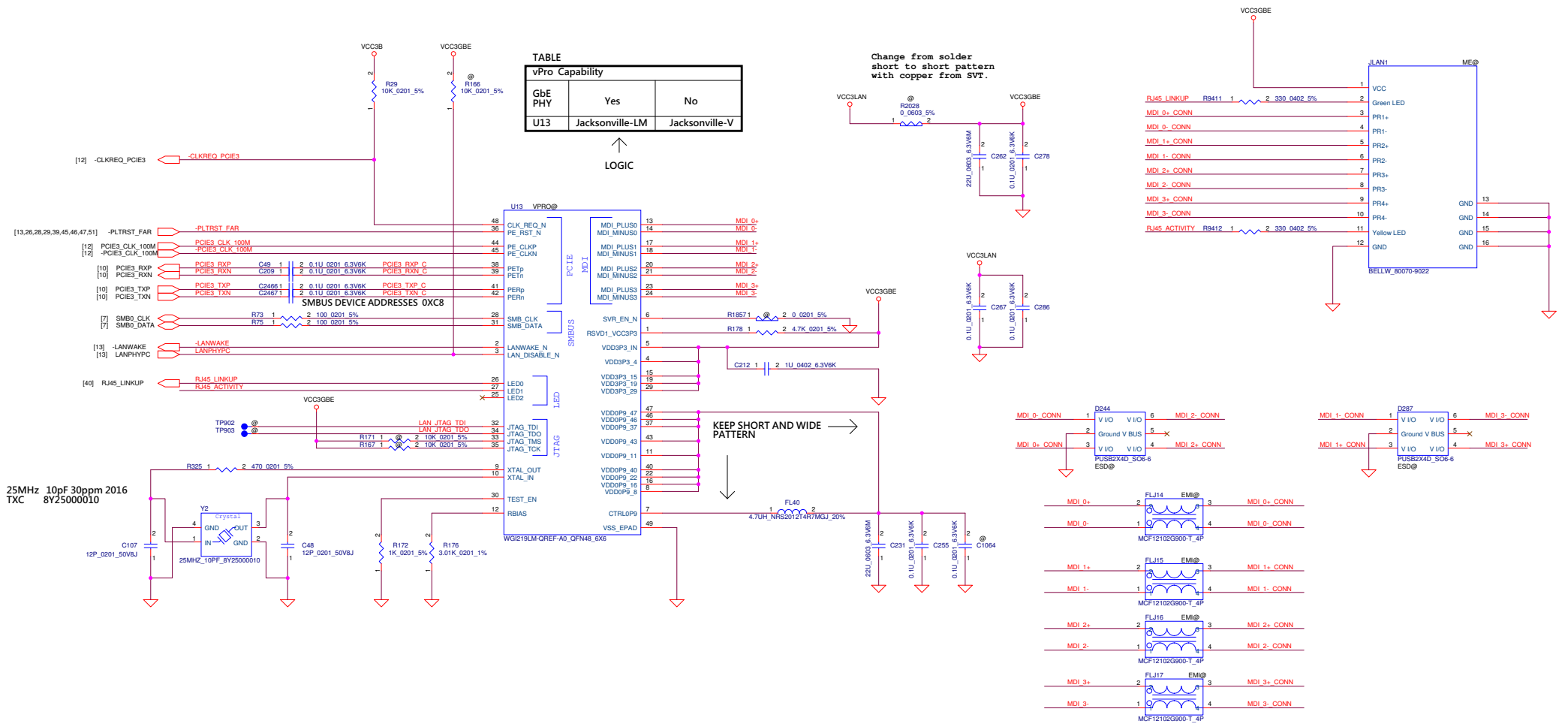
From MEC pin H2 [41] -TBT_MRESET

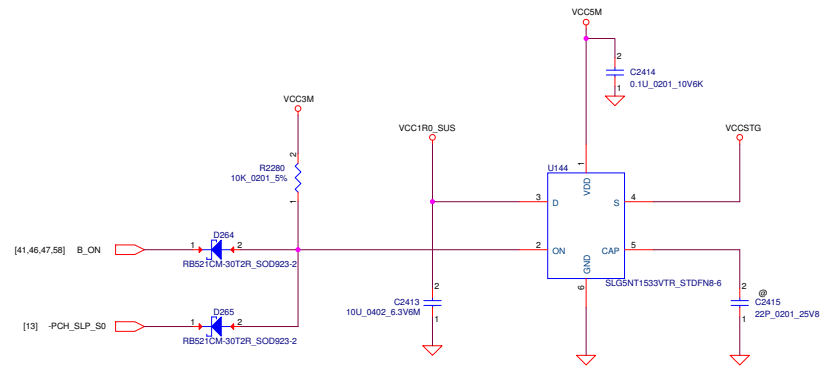
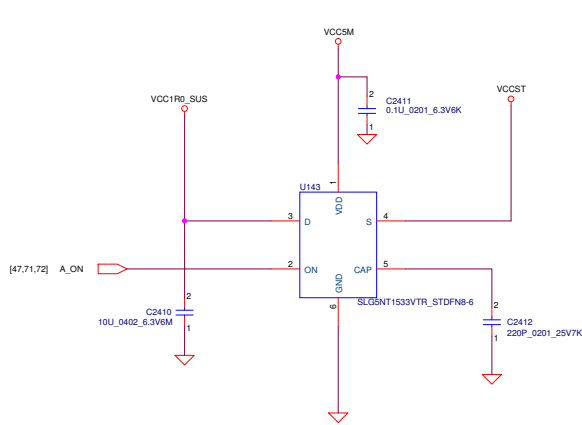
Security Classification		Compal Secret Data		Title	
Issued Date	2015/01/06	Deciphered Date	2016/01/06	Compal Electronics, Inc.	
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TPS65982D AZOZR-ES_BGA96				LA-E291P	0.3
Date:	Thursday, September 01, 2016	Sheet	53	of 75	

TABLE
vPro Capability

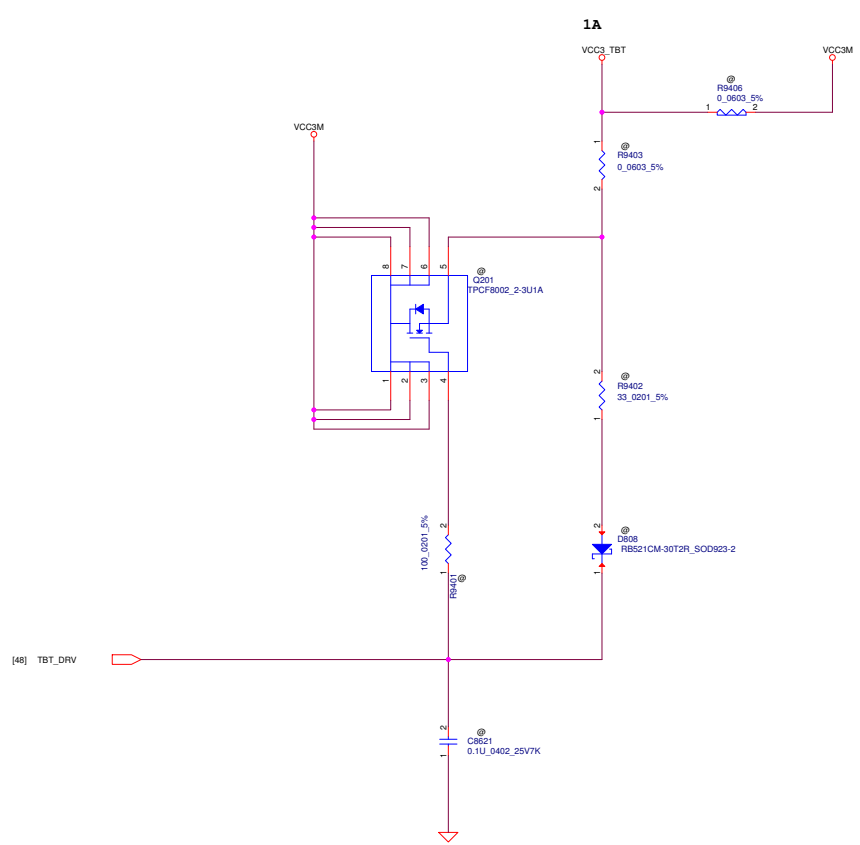
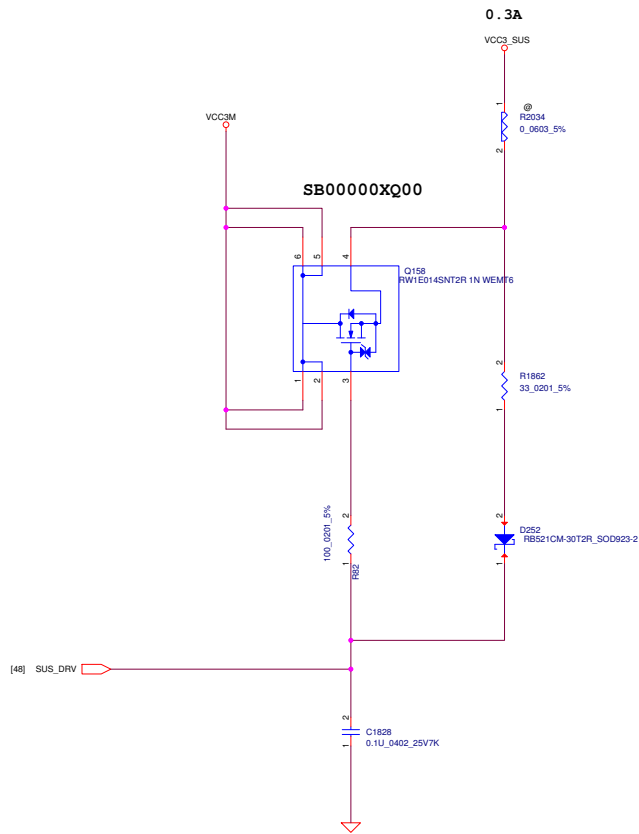
GBE PHY	Yes	No
U13	Jacksonville-LM	Jacksonville-V

↑
LOGIC

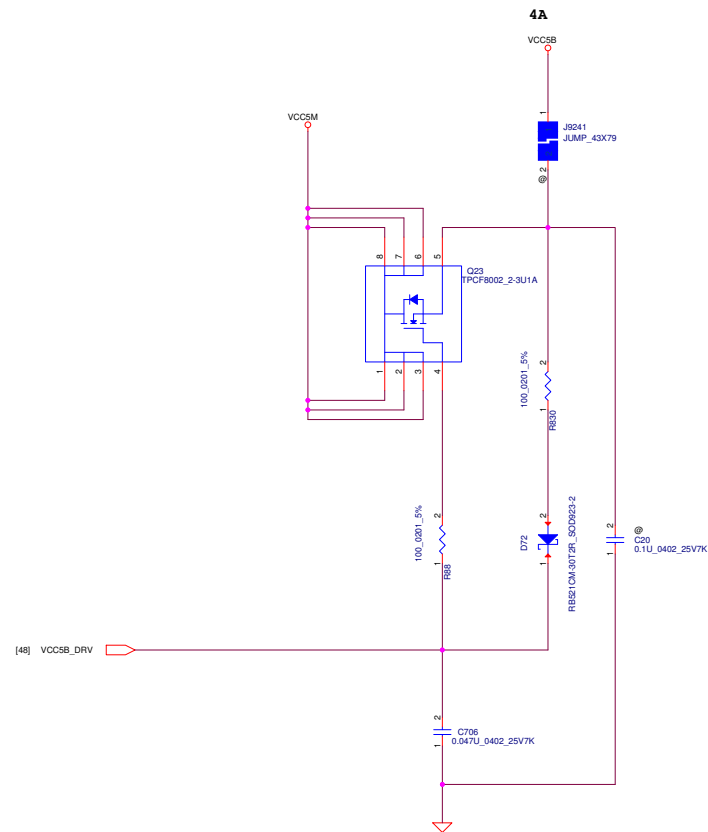
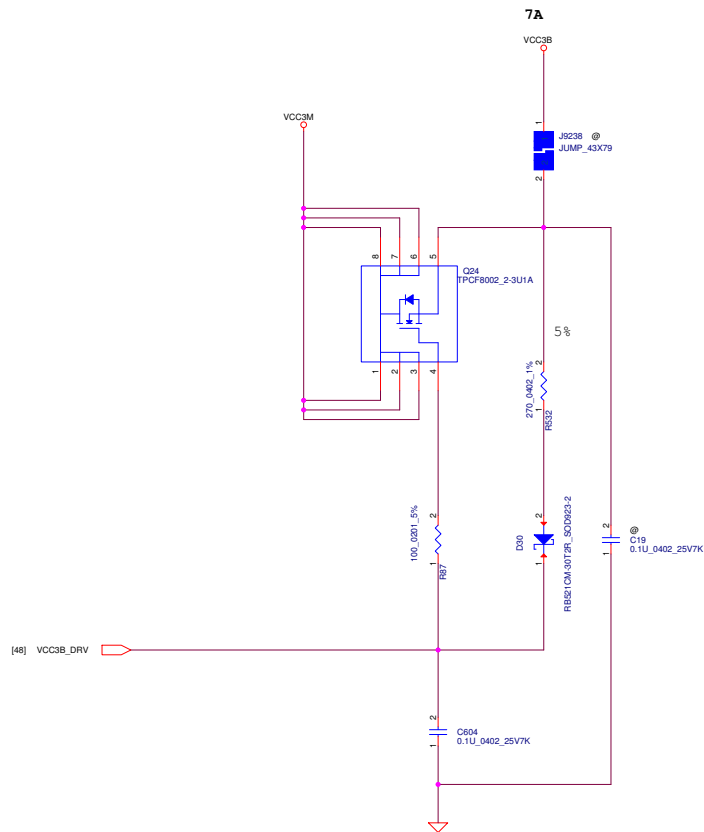




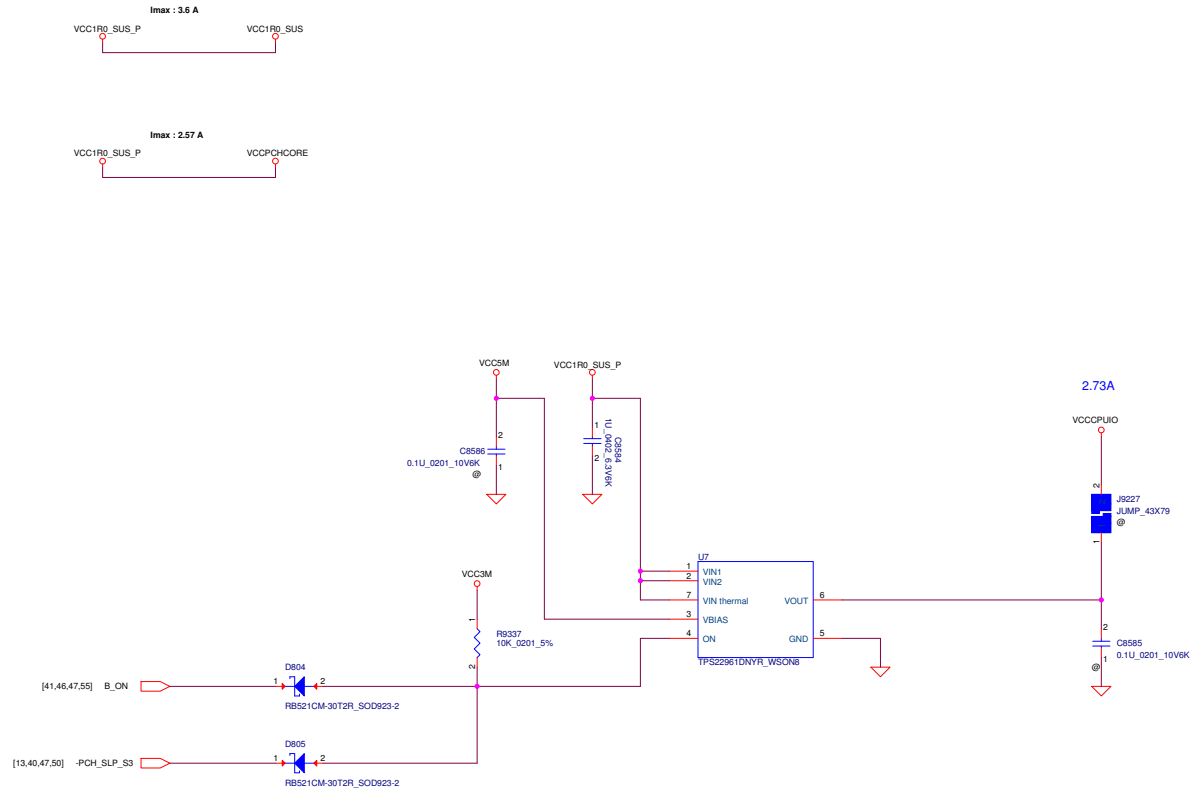
Security Classification	Compal Secret Data		Title	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	LOAD SW VCCST & VCCSTG
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<small>Document Number</small> LA-E291P			<small>Date</small> Thursday, September 01, 2016 <small>Sheet</small> 55 of 75	



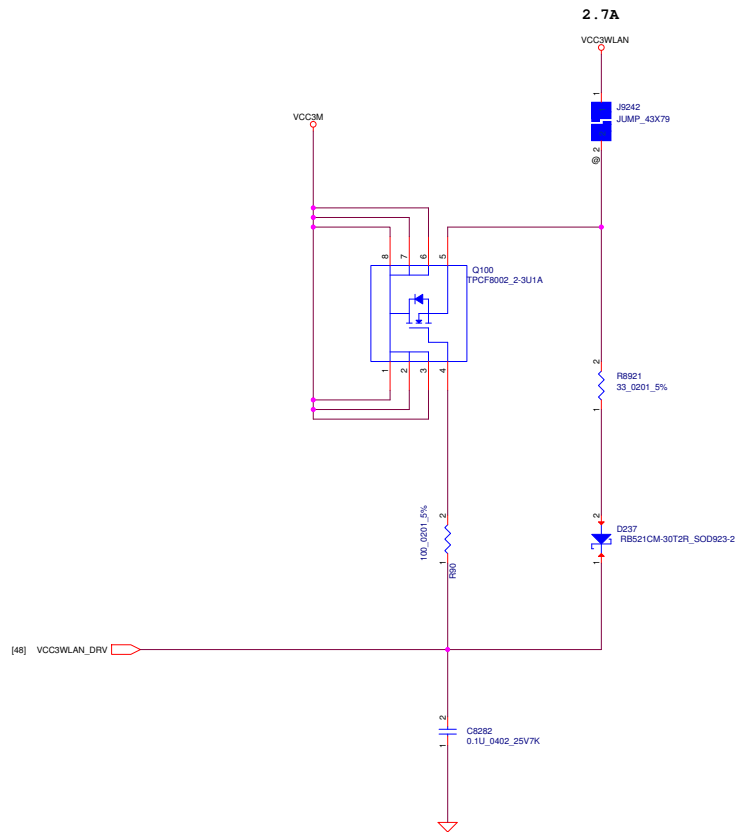
Security Classification	Compal Secret Data		Title	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	LOAD SW PCH SUS/TRACK POIN
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				<small>Document Number</small> LA-EZ91P <small>Rev</small> 0.3
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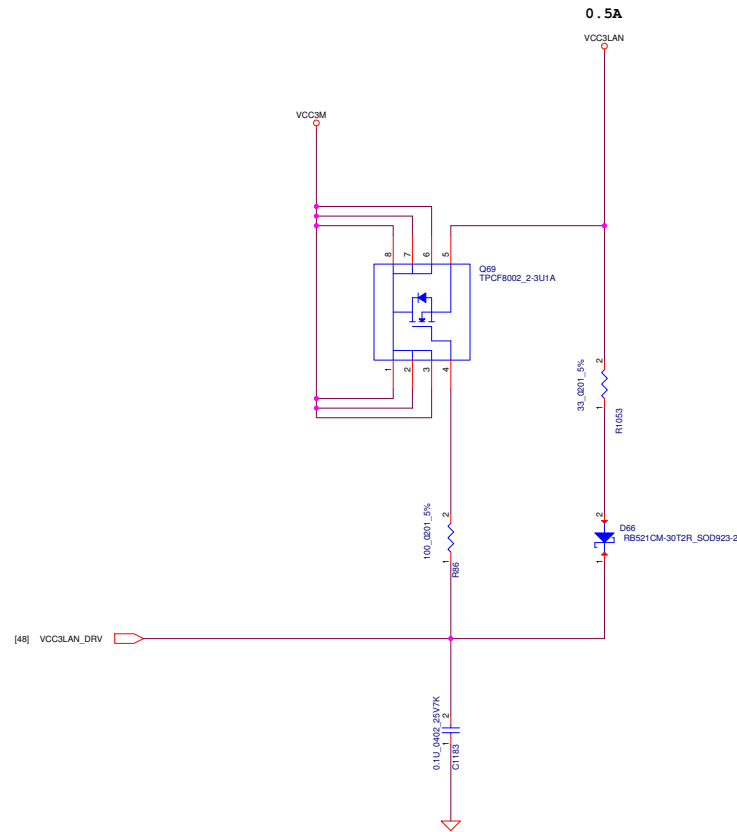
Security Classification	Compal Secret Data		Title	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	LOAD SW B
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev 0.3
Date: Thursday, September 01, 2016			Sheet 57 of 75	LA-E291P



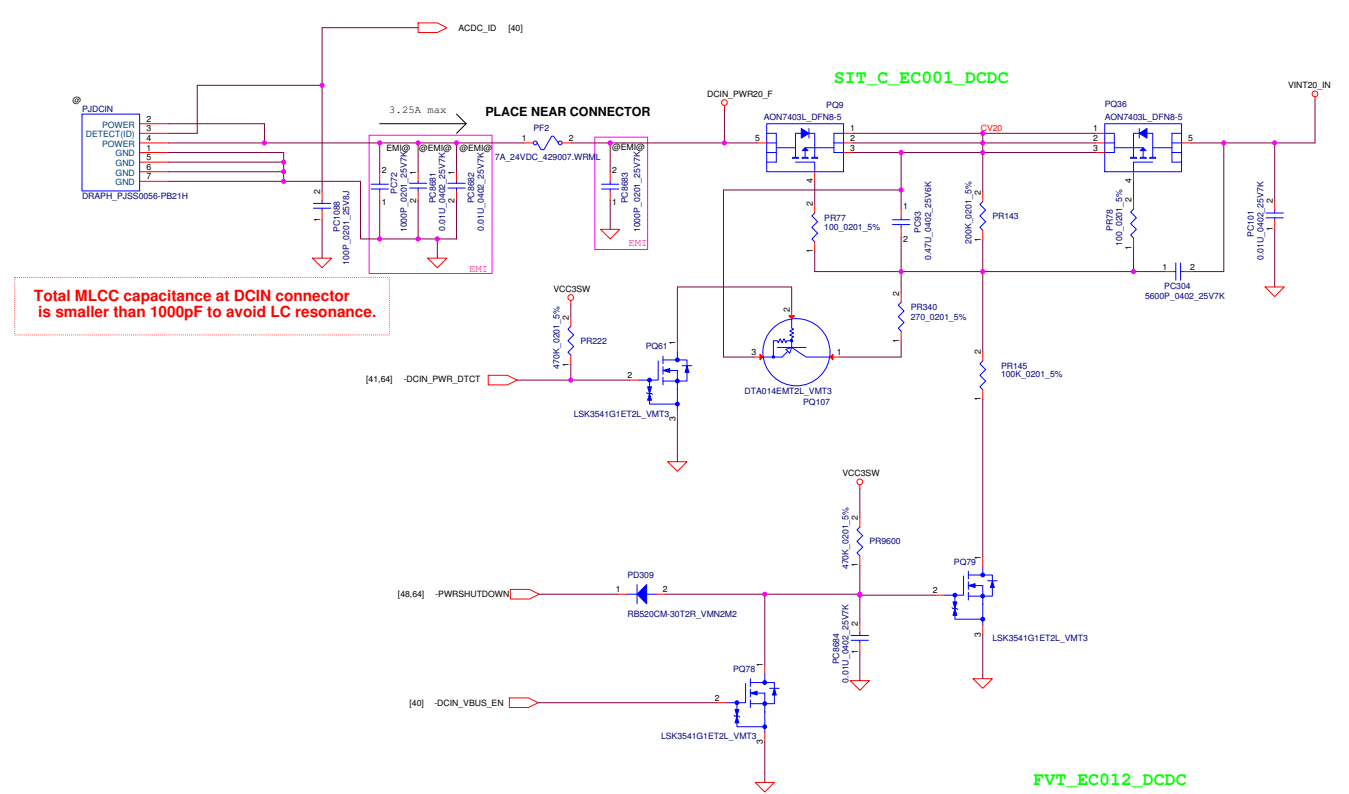
Security Classification	Compal Secret Data		Title	
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				Document Number	Rev
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				Date	Thursday, September 01, 2016



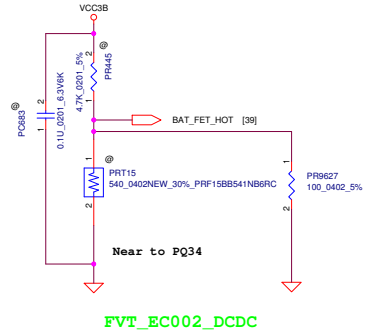
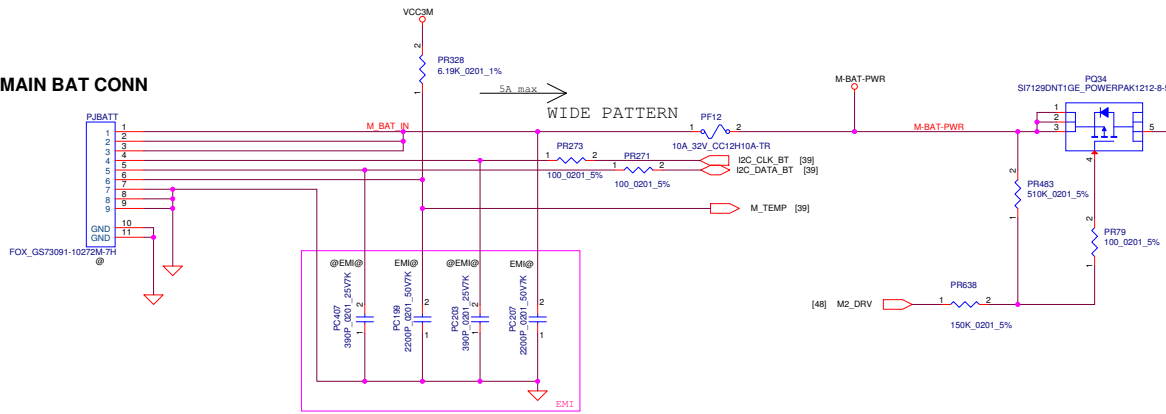
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	LOAD SW LAN
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				Date	Thursday, September 01, 2016
				Sheet	60 of 75



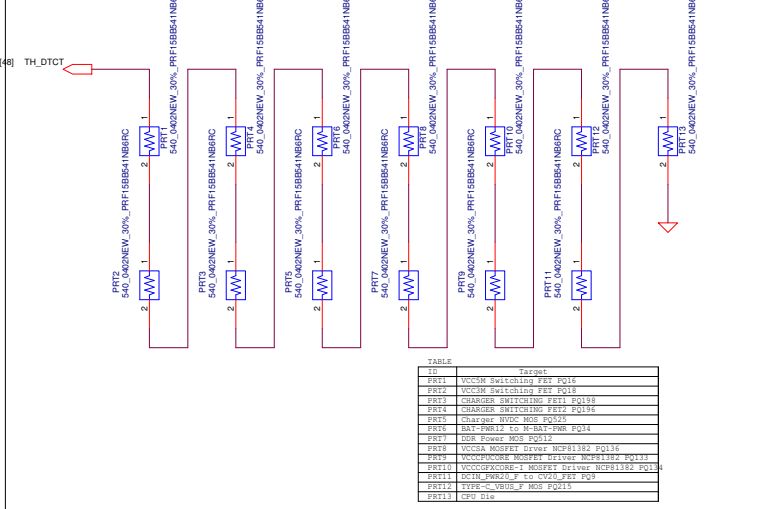
Total MLCC capacitance at DCIN connector is smaller than 1000pF to avoid LC resonance.

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Issued Date	2014/11/04	Deciphered Date	2016/12/31	DC-IN	
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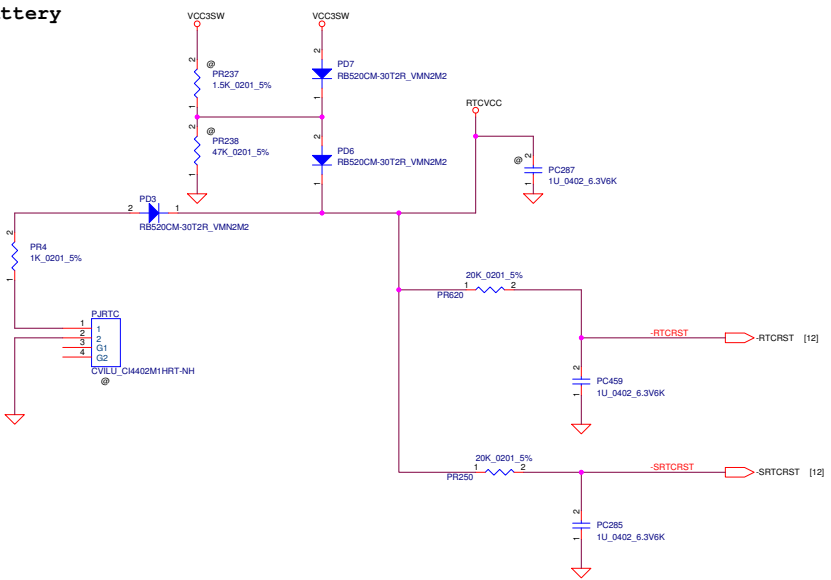
MAIN BAT CONN



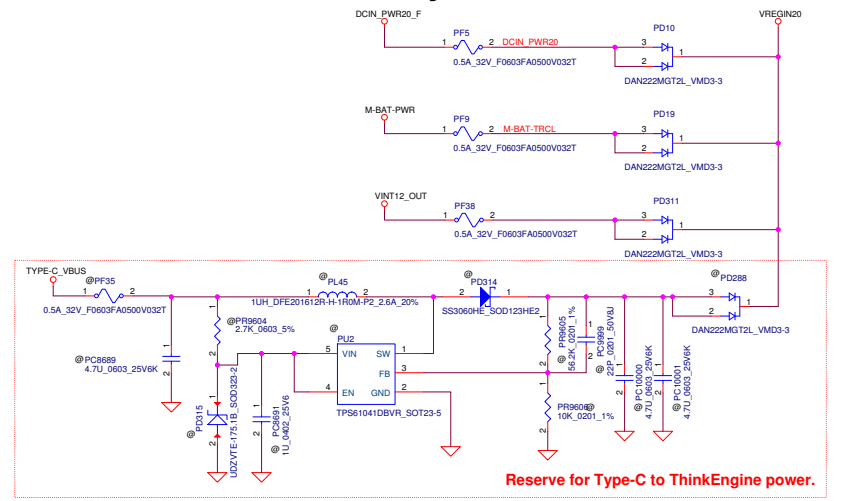
PTC function

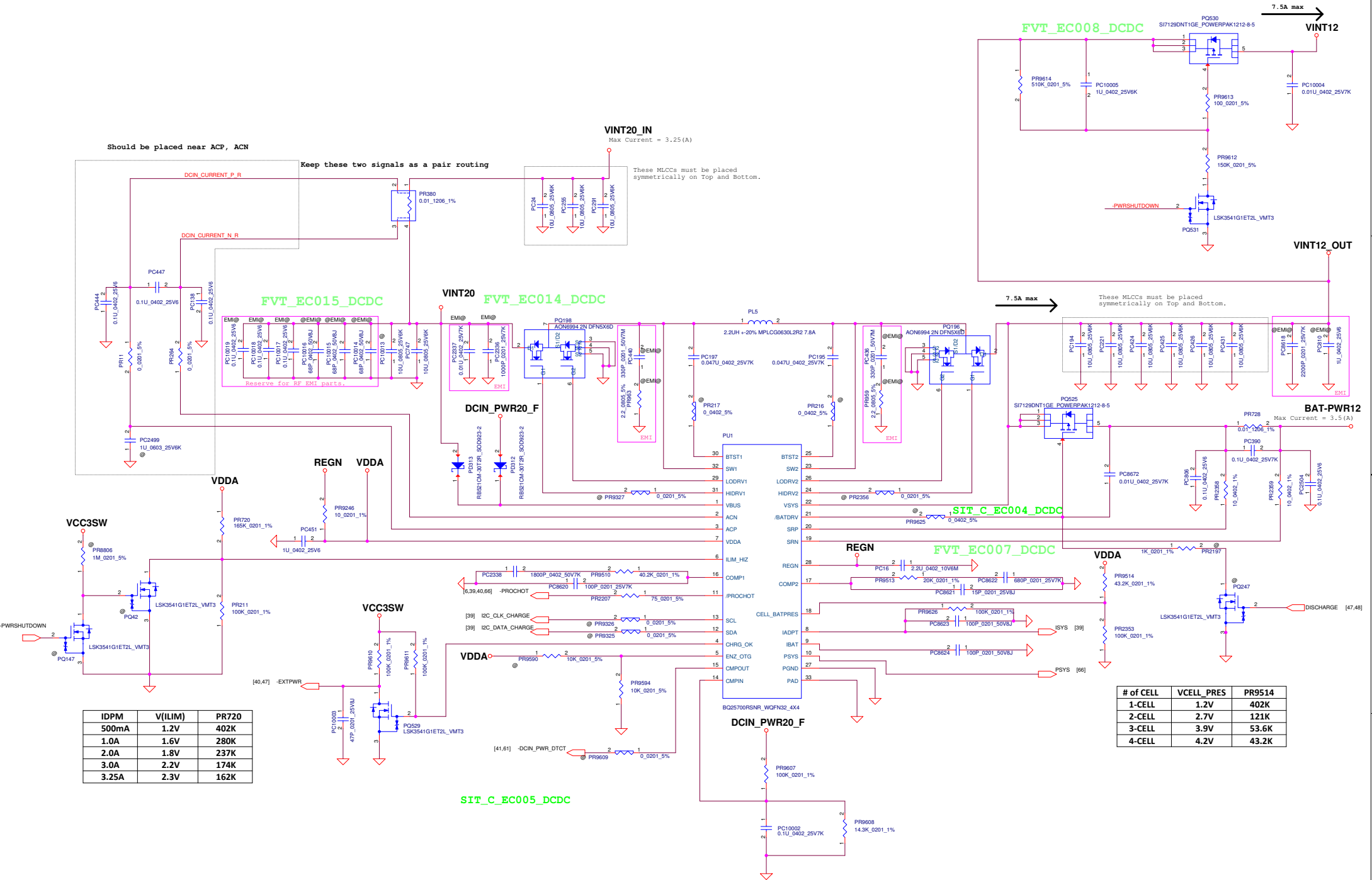


RTC Battery



FVT_EC003_DCDC Power to ThinkEngine



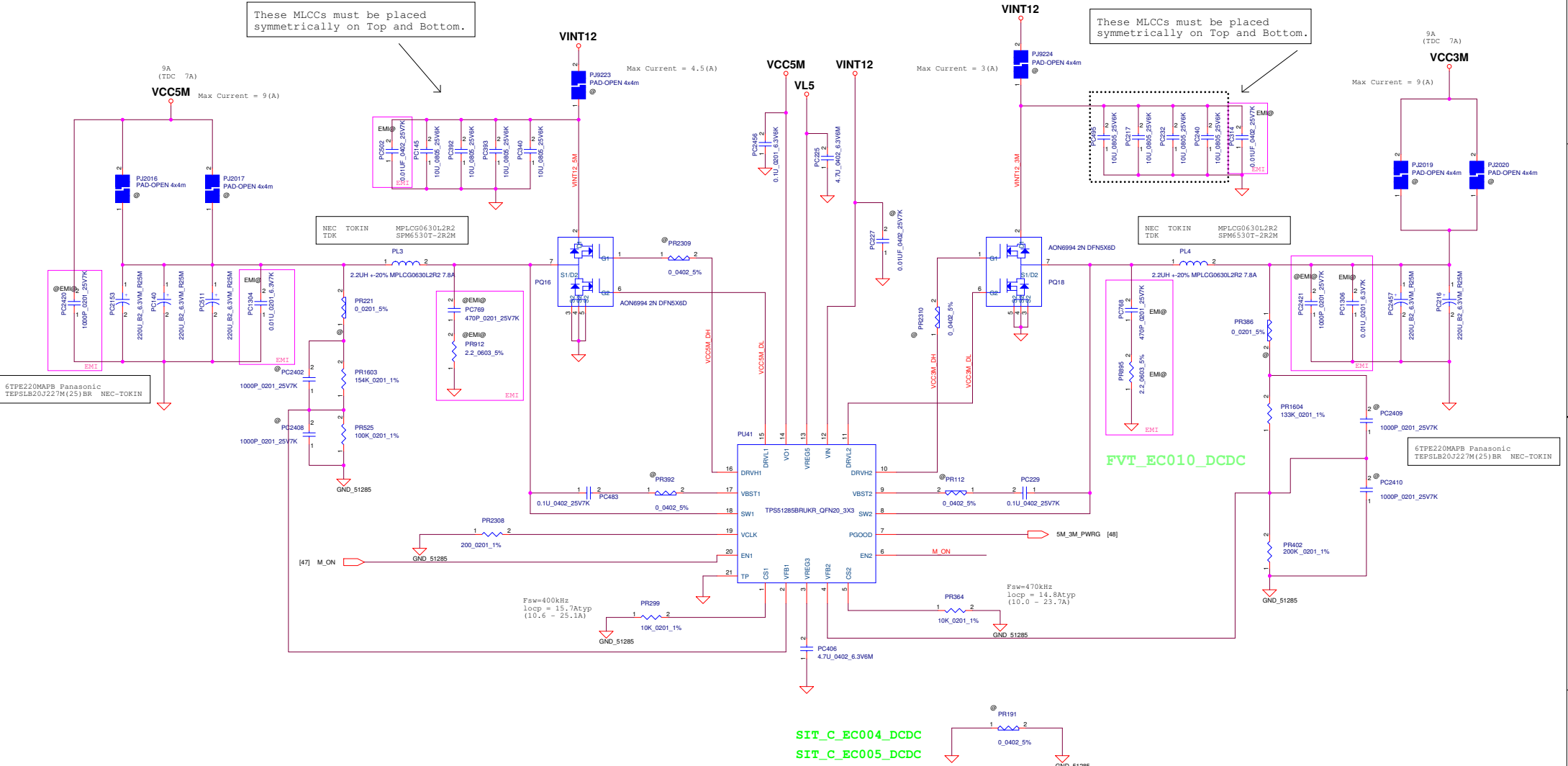


IDPM	V(ILIM)	PR720
500mA	1.2V	402K
1.0A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

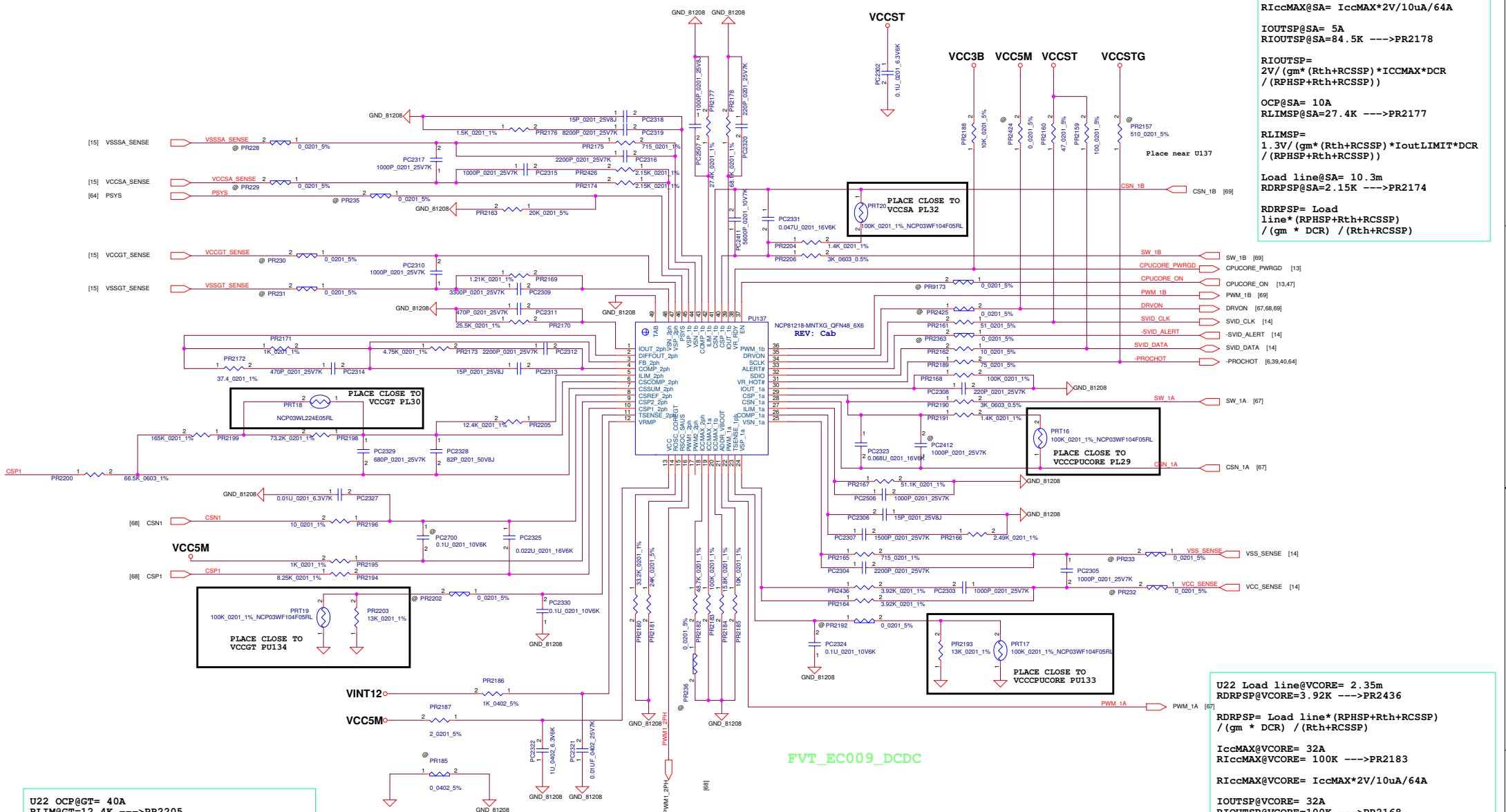
# of CELL	VCELL_PRES	PR9514
1-CELL	1.2V	402K
2-CELL	2.7V	121K
3-CELL	3.9V	53.6K
4-CELL	4.2V	43.2K

These MLCCs must be placed symmetrically on Top and Bottom.

These MLCCs must be placed symmetrically on Top and Bottom.



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IccMAX@SA= 5A
RiccMAX@SA= 15.8K ---->PR2184
RiccMAX@SA= IccMAX*2V/10uA/64A
IOUTSP@SA= 5A
RIOUTSP@SA=84.5K ---->PR2178
RIOUTSP=
 $2V / (gm * (Rth + RCSSP) * ICcMAX + DCR / (RPHSP + Rth + RCSSP))$
OCp@SA= 10A
RLIMSP@SA=27.4K ---->PR2177
RLIMSP=
 $1.3V / (gm * (Rth + RCSSP) * IoutLIMIT + DCR / (RPHSP + Rth + RCSSP))$
Load line@SA= 10.3m
RDRPSP@SA=2.15K ---->PR2174
RDRPSP= Load
 $line * (RPHSP + Rth + RCSSP) / (gm * DCR) / (Rth + RCSSP)$

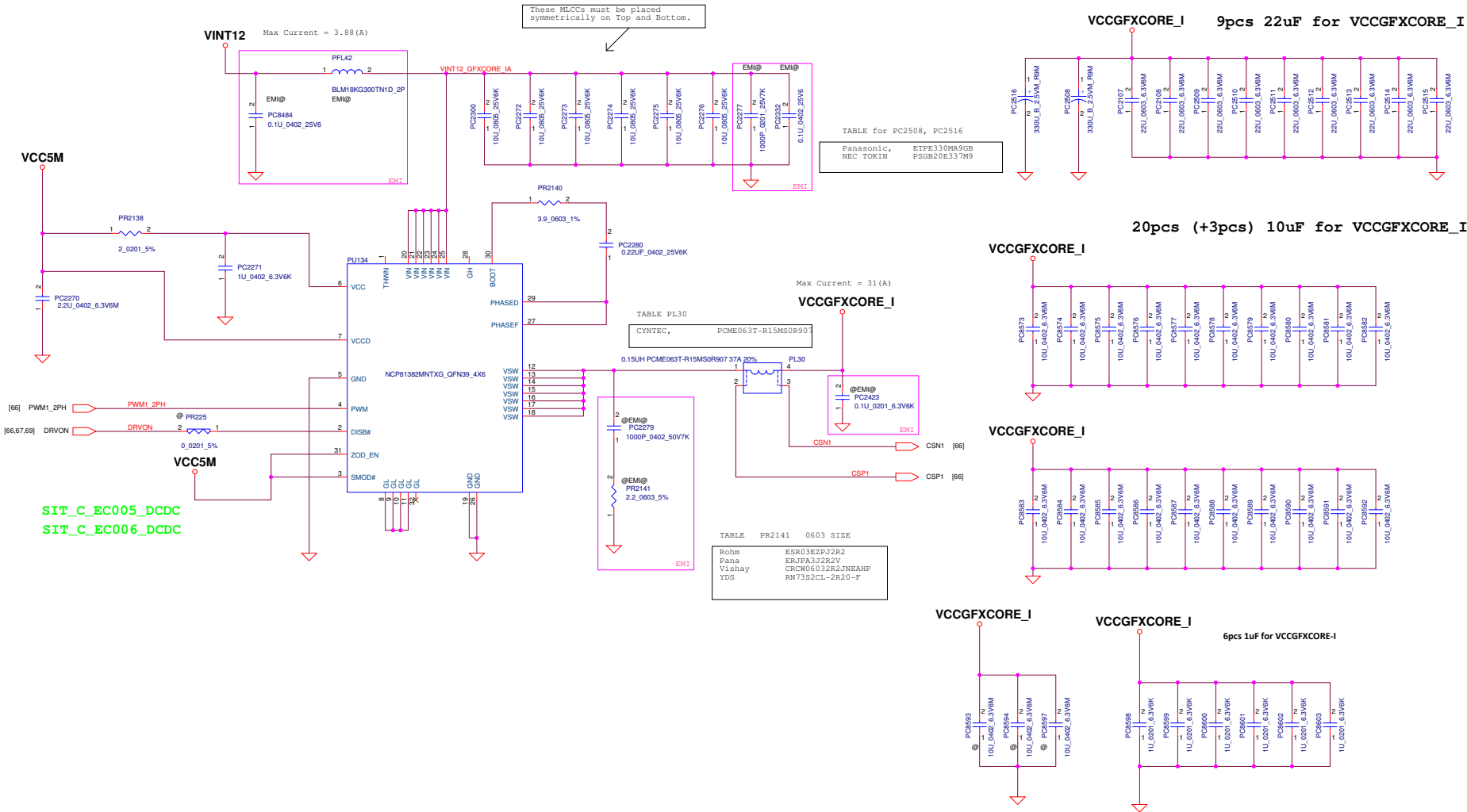
U22 Load line@VCORE= 2.35m
RDRPSP@VCORE=3.92K ---->PR2436
RDRPSP= Load line * (RPHSP + Rth + RCSSP)
 $/ (gm * DCR) / (Rth + RCSSP)$
IccMAX@VCORE= 32A
RiccMAX@VCORE= 100K ---->PR2183
RiccMAX@VCORE= IccMAX*2V/10uA/64A
IOUTSP@VCORE= 32A
RIOUTSP@VCORE=100K ---->PR2168
RIOUTSP= 2V / (gm * (Rth + RCSSP) * ICcMAX + DCR
 $/ (RPHSP + Rth + RCSSP))$
OCp@VCORE= 40A
RLIMSP@VCORE=51.1K ---->PR2167
RLIMSP= 1.3V / (gm * (Rth + RCSSP) * IoutLIMIT + DCR
 $/ (RPHSP + Rth + RCSSP))$

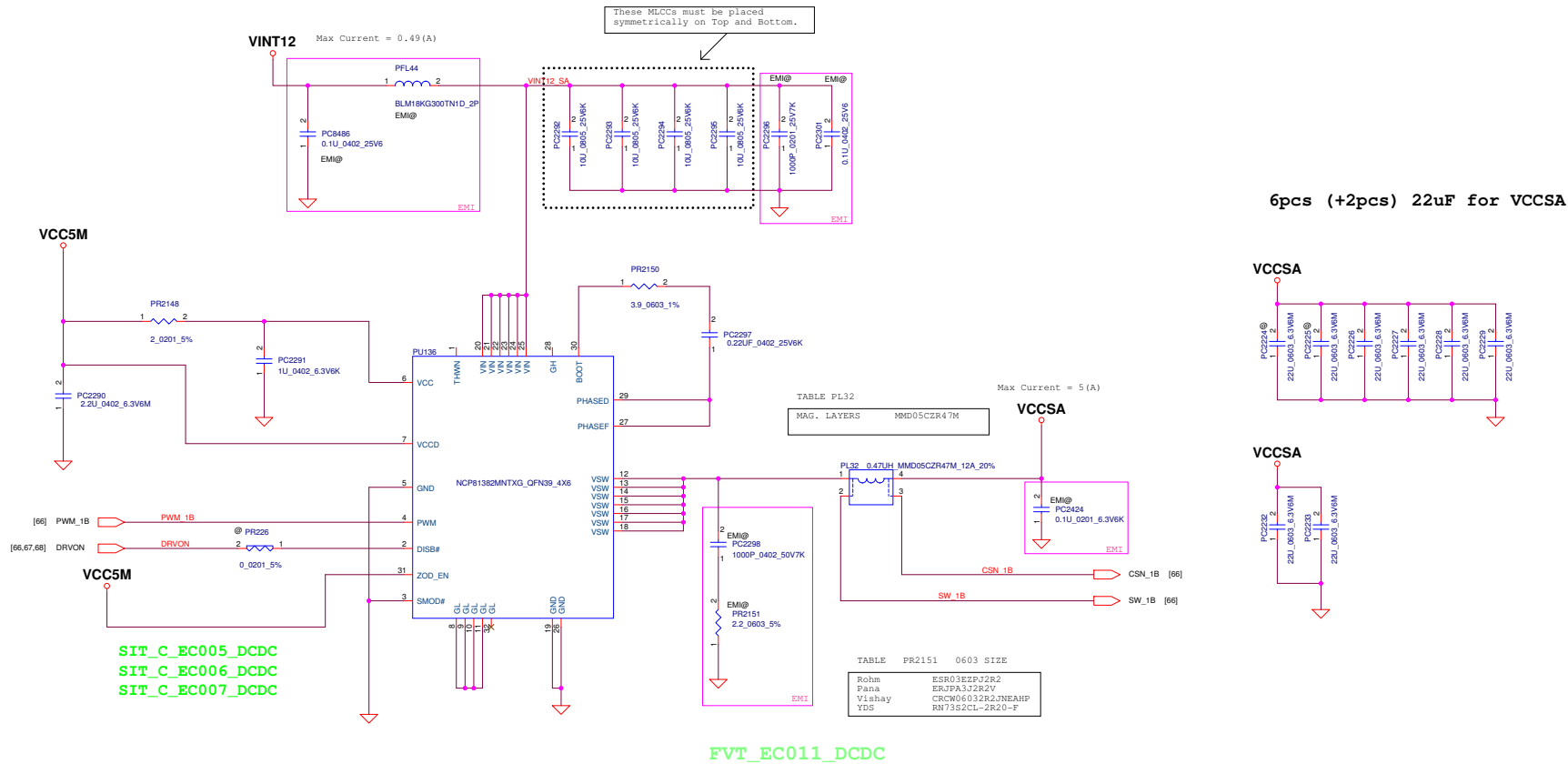
U22 OCP@GT= 40A
RLIM@GT=12.4K ---->PR2205
RLIM= IoutLIMIT * Load line/10
U22 IccMAX@GT= 31A
RiccMAX2ph= 48.7K ---->PR2182
RiccMAX2ph= (IccMAX2Ph+32) * 200K Ohn/ 127
U22 Iout@GT= 31A
RIOUT@GT=25.5K ---->PR2170
RIOUT= 2 * RLIM / (10 * IOUITCCMAX * Load line)
U22 Load line@GT= 3.1m
RPH@GT=84.5K ---->PRI30, PRI38
Load line= (RCS2 + RCS1 * Rth) / (RCS1 + Rth))
***IOUITOTAL * DCR/RPH**

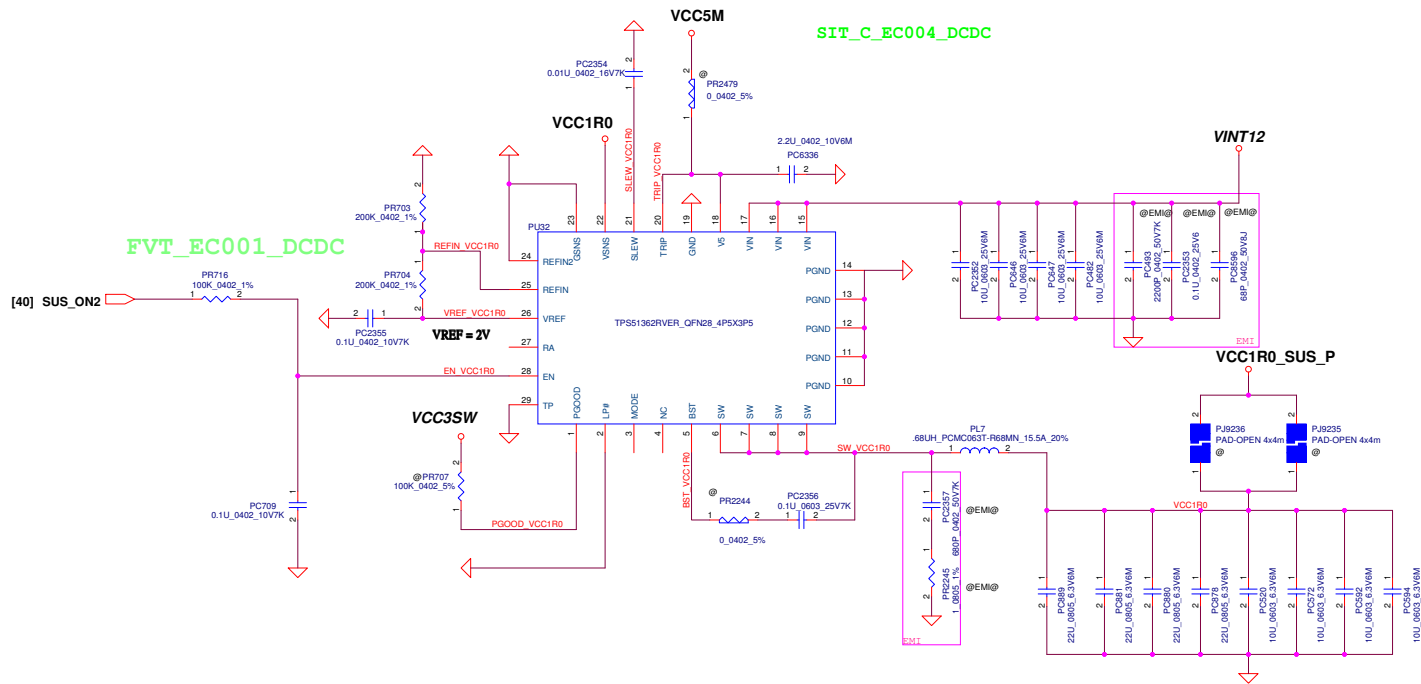
TABLE OCP

PR2167	51.1K	Ilim=40A	VCCUCORE
PR2205	12.4K	Ilim=40A	VCCGFXCORE
PR2177	27.4K	Ilim=10A	VCCSA

SIT_C_EC004_DCDC
SIT_C_EC005_DCDC







FVT_EC001_DCDC

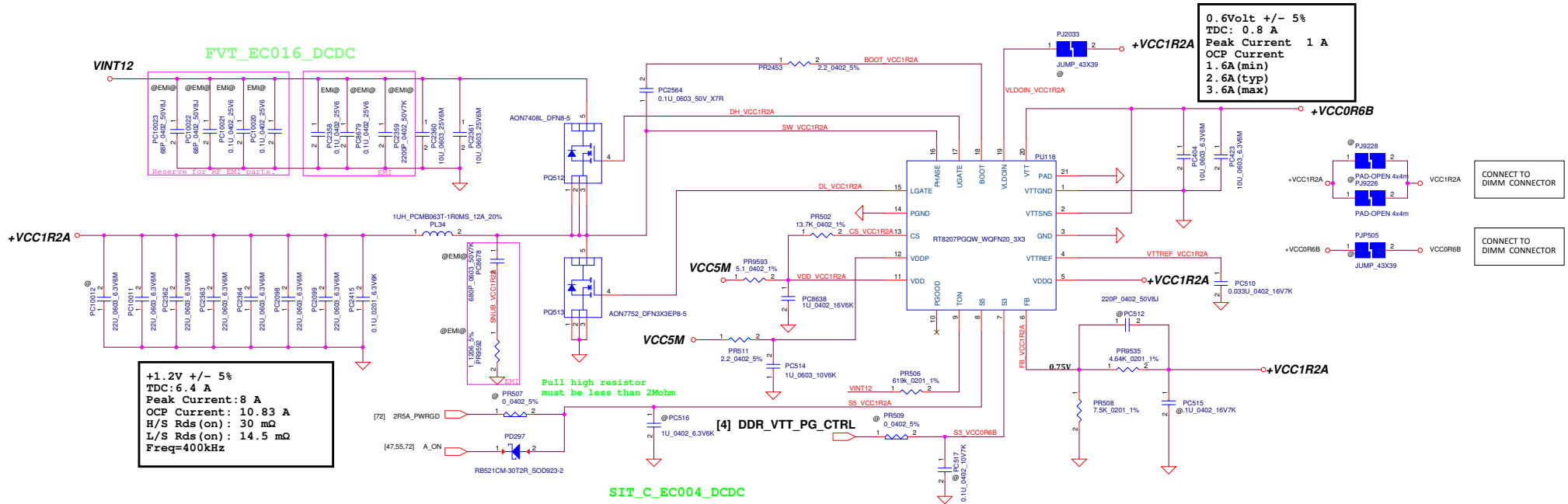
SIT_C_EC004_DCDC

1.0VS OCL = 8A (Trip = GND)
1.0VS OCL = 12A (Trip = 5V)

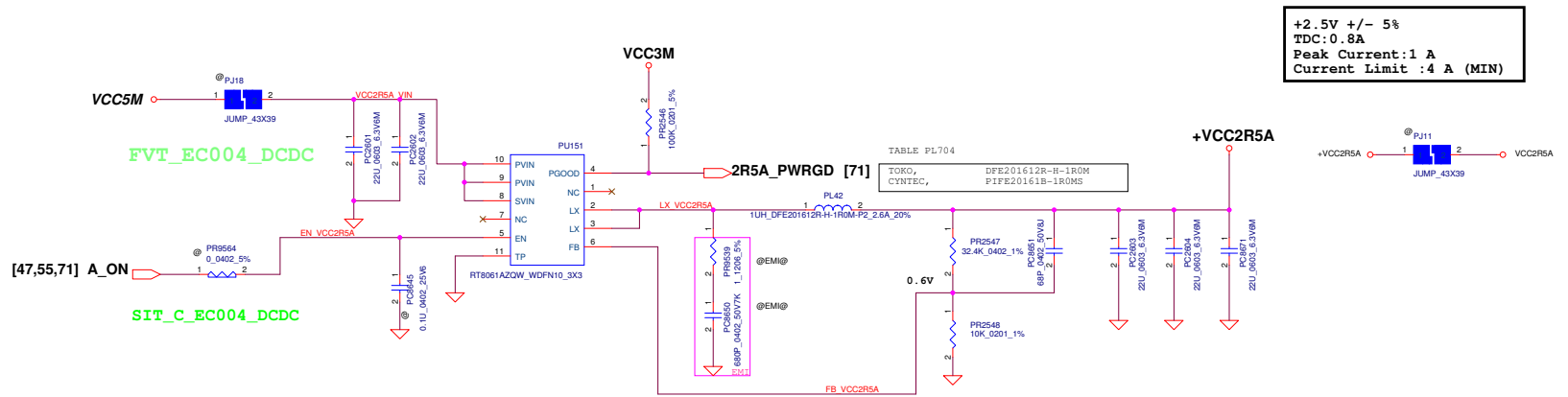
+1.0 V +/- 5%
TDC: 7.12 A
Peak Current: 8.9 A
OCP Current: 12 A

Output Voltage = 1.05V (REFIN Voltage = GND)
Output Voltage = 1.2V (REFIN Voltage = FLOAT)
Output Voltage Adj between = 0.6V-2V (REFIN Voltage = Resistor divider)

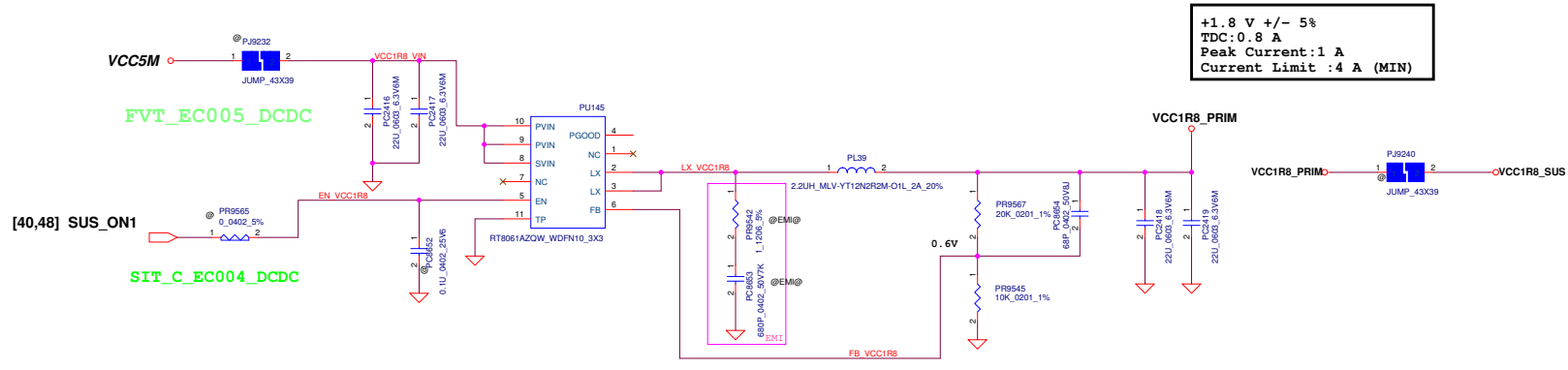
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Issued Date	2014/11/04	Deciphered Date	2016/12/31
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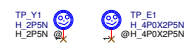
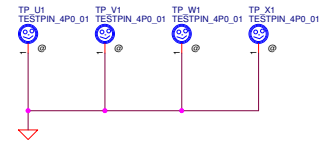
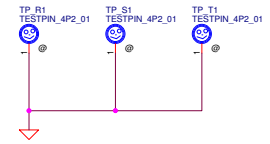
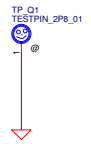
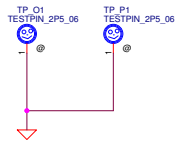
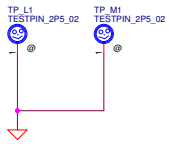
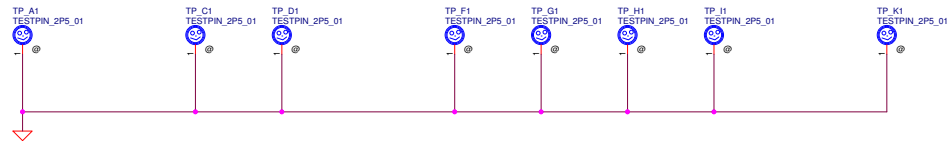


+1.8 V +/- 5%
 TDC: 0.8 A
 Peak Current: 1 A
 Current Limit: 4 A (MIN)

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PTH FOR SCREW HOLE

Value	Hole Dia	Pad Dia		QTY
		TOP	BOTTOM	
TESTPIN_2P5_01	2.5	6	6	9
TESTPIN_2P5_02	2.5	7.4	7.4	2
TESTPIN_2P5_03	2.5	Square	0	1
TESTPIN_2P5_06	2.5	5	5	2
TESTPIN_2P8_01	2.8	0	Square	1
TESTPIN_4P3_01	4.3	6.5	6.5	3
TESTPIN_4P0_01	4.0	6.1	6.1	4



FID
Board Area


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 ZZZ
 DAB001BL000
 DIMM


 ZZZ1
 DAB001BM000
 On board

 U58
 KBL_QKKS 2.4G
 CPU1@
 SA00009P140


 U58
 KBL_QKJW 2.6G
 CPU2@
 SA00009UR20


 U58
 KBL_QKDP 2.4G
 CPU3@
 SA0000A3840


 U58
 KBL_QKDN 2.7G
 CPU4@
 SA0000A3410

 U58
 KBL_QKDM 2.5G
 CPU5@
 SA0000A3740

 U58
 KBL_QKDU 2.6G
 CPU6@
 SA0000A3L00

 U58
 KBL_QLYG 2.6G
 CPU7@
 SA0000AD000

 U58
 KBL_QLYF 2.8G
 CPU8@
 SA0000ADP00

 U13
 Jacksonville WGI219V
 NVPRO@
 SA00009S410

 ZZZ
 Samsung 1G
 S1G@
 X7666239L24

 ZZZ
 Micron 1G
 M1G@
 X7666239L22

 ZZZ
 Samsung 2G
 S2G@
 X7666239L23

BOM Structure Table

BTO Item	BOM Structure	Remark
vPRO LAN chip	VPRO@	WGI219LM
non vPRO LAN chip	NVPRO@	WGI219V
Thunderbolt requirement	TBT@	
Thunderbolt reserve	@TBT@	
ESD requirement	ESD@	
ESD reserve	@ESD@	
EMI requirement	EMI@	
EMI reserve	@EMI@	
RF requirement	RF@	
RF reserve	@RF@	
XDP	XDP@	
On board RAM	X76@	