

Model Name : B5/B7W1A
File Name : LA-D641P

Compal Confidential

B5/B7W1A M/B Schematics Document

Intel Apollo lake
UMA

2016-07-22

REV:1.A

For 1A PCB

PCB15A@
ZZZ

Part Number	Description
DA6001K401A	PCB 1NU LA-D641P REV1A MB 1

PCB17A@
ZZZ3

Part Number	Description
DA6001K411A	PCB 1NU LA-D641P REV1A MB 2

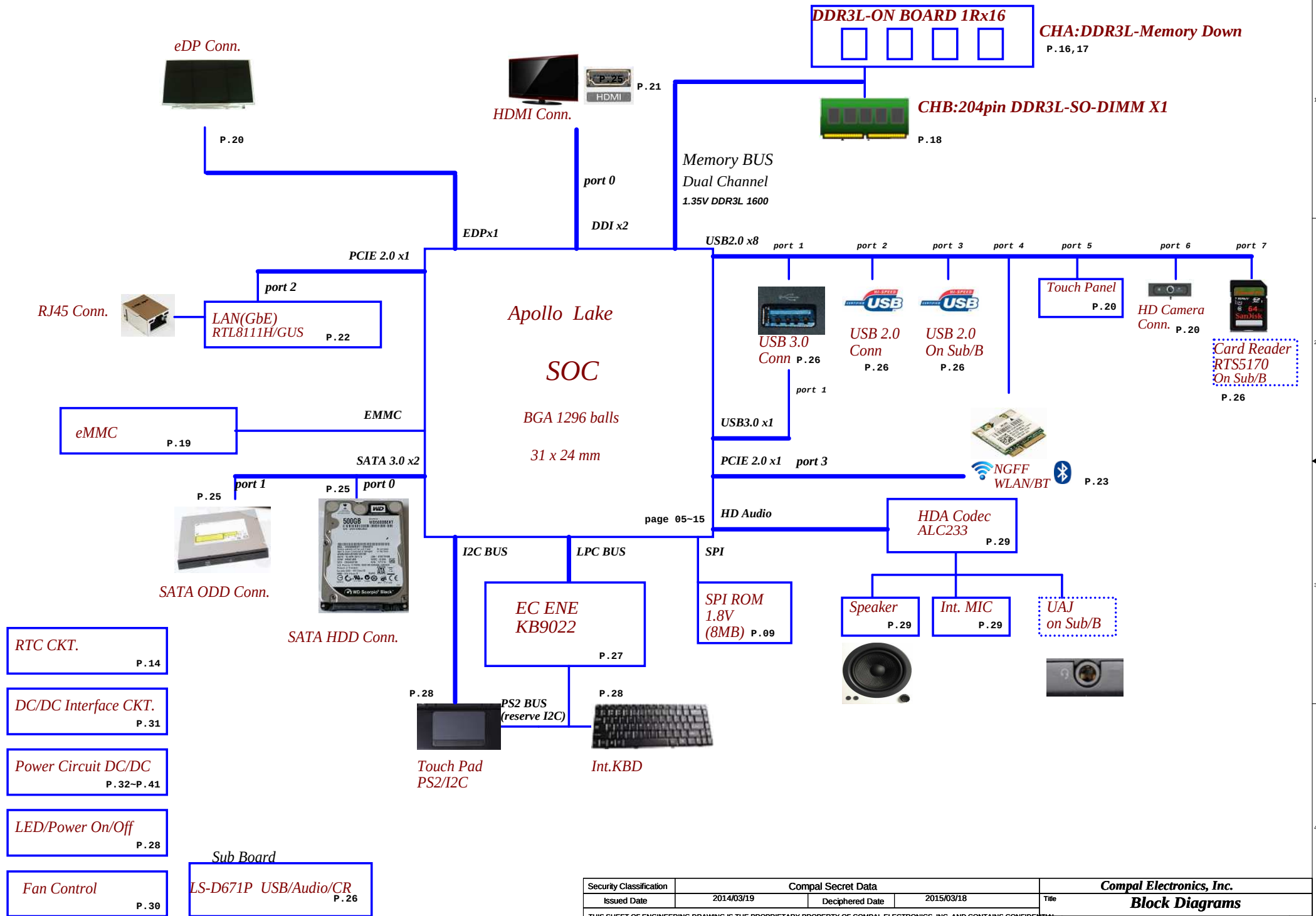
PCB15@
ZZZ

Part Number	Description
DA6001K4000	PCB 1NU LA-D641P REV0 MB 1

PCB17@
ZZZ

Part Number	Description
DA6001K4100	PCB 1NU LA-D641P REV0 MB 2

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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
+19VB	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.24VALW	+1.24v Always power rail	ON	ON	OFF
+1.8VALW	+1.8v Always power rail	ON	ON	OFF
+3V_SOC	+3v Always power rail for SOC	ON	ON	OFF
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	ON
+3V_PTP	+3.3V power rail for PTP	ON	ON	OFF
+VNN	other (non core) logic voltage for SOC	ON	OFF	OFF
+VCC_VCGI	Core & GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.05VS	+1.05v System power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				
Note : ON** dGPU optimus on				

Board ID / SKU ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00-0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14-0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F-0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26-0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31-0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B-0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46-0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55-0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65-0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77-0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88-0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97-0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5-0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0-0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8-0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0-0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA-0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5-0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE-0xFF
19	NC	3.000V	3.000V		0xF1-0xFF

BOARD ID Table_LA-D641P

Board ID	PCB Revision
01	EVT_LA-D641PR01
02	DVT_LA-D641PR02
03	PVT(DVT2)_LA-D641PR03
04	Pre MP_LA-D641PR10
05	Pre MP_LA-D641PR1A

43 level BOM table

43 Level	Description	BOM Structure
431A2BB0L07	SMT MB AD641 B5W1A QKT4 HDMI	233@/8111H@/NBYOC@/CMC@/PCB15@/QKT4@
431A2BB0L08	SMT MB AD641 B5W1A QKTY 2G HDMI	233@/8111H@/NBYOC@/CMC@/PCB15@/QKTY@/MD@
431A2BB0L09	SMT MB AD641 B5W1A QKTW 2G HDMI	233@/8111H@/NBYOC@/CMC@/PCB15@/QKTW@/MD@
431A2BB0L60	SMT MB AD641 B7W1A QKT4 HDMI	233@/8111H@/NBYOC@/CMC@/PCB17@/QKT4@
431A2BB0L61	SMT MB AD641 B7W1A QKT4 2G HDMI	233@/8111H@/NBYOC@/CMC@/PCB17@/QKT4@/MD@
431A2BB0L62	SMT MB AD641 B7W1A QKTY 2G HDMI	233@/8111H@/NBYOC@/CMC@/PCB17@/QKTY@/MD@
431A2BB0L63	SMT MB AD641 B7W1A QKTW 2G HDMI	233@/8111H@/NBYOC@/CMC@/PCB17@/QKTW@/MD@

EC SMBUS Routing Table

EC	Power	BAT	CHGR	NGFF
EC_SMB_CK1 EC_SMB_DA1	+3VALW	V	V	X
EC_SMB_CK2 EC_SMB_DA2	+3VS	X	X	V

SOC SMBUS Routing Table

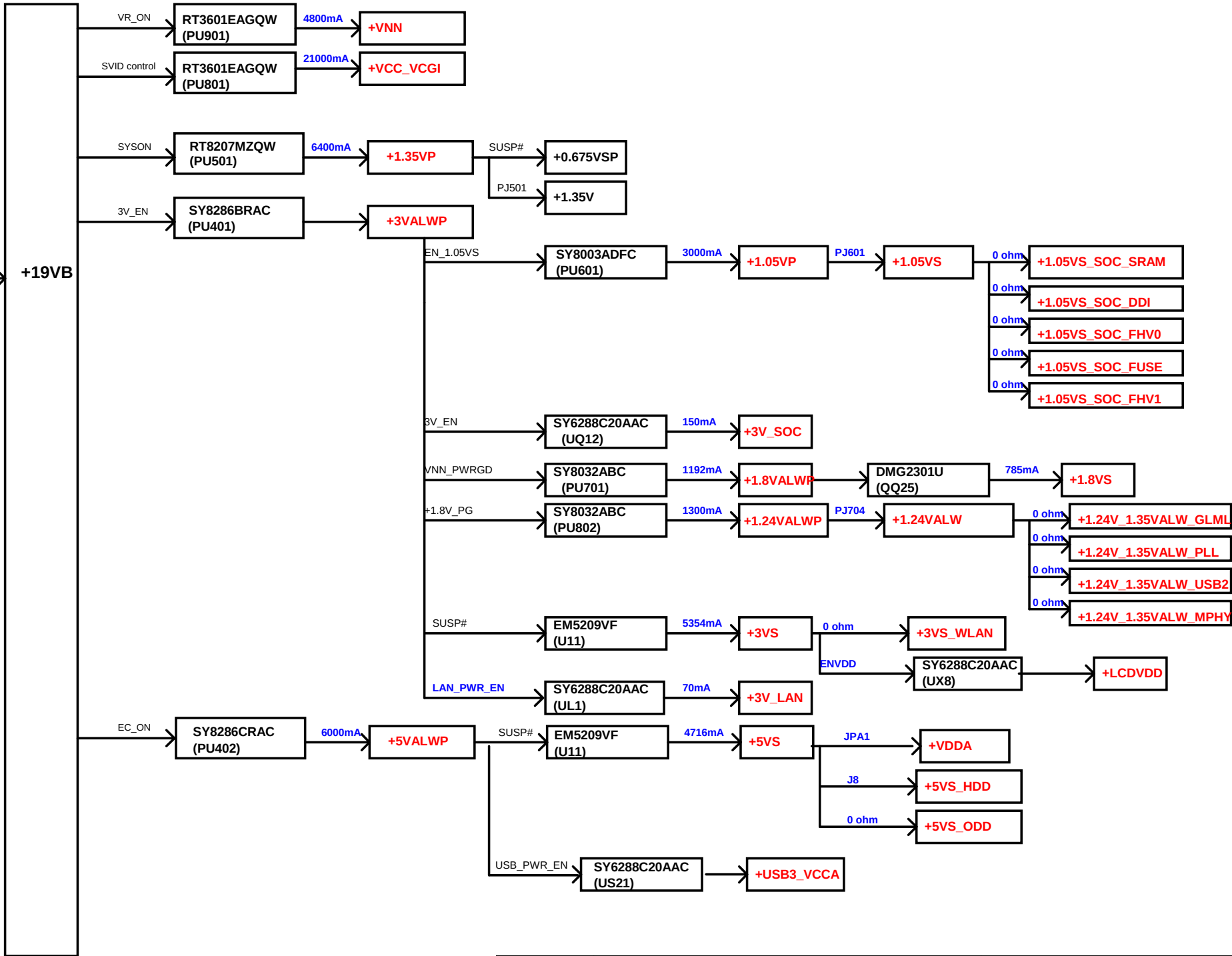
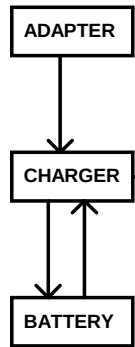
SOC	Power	DIMM1	DIMM2
SMB Address			
SOC_SMBCLK SOC_SMBDATA	+3VS	V	V

I2C Map

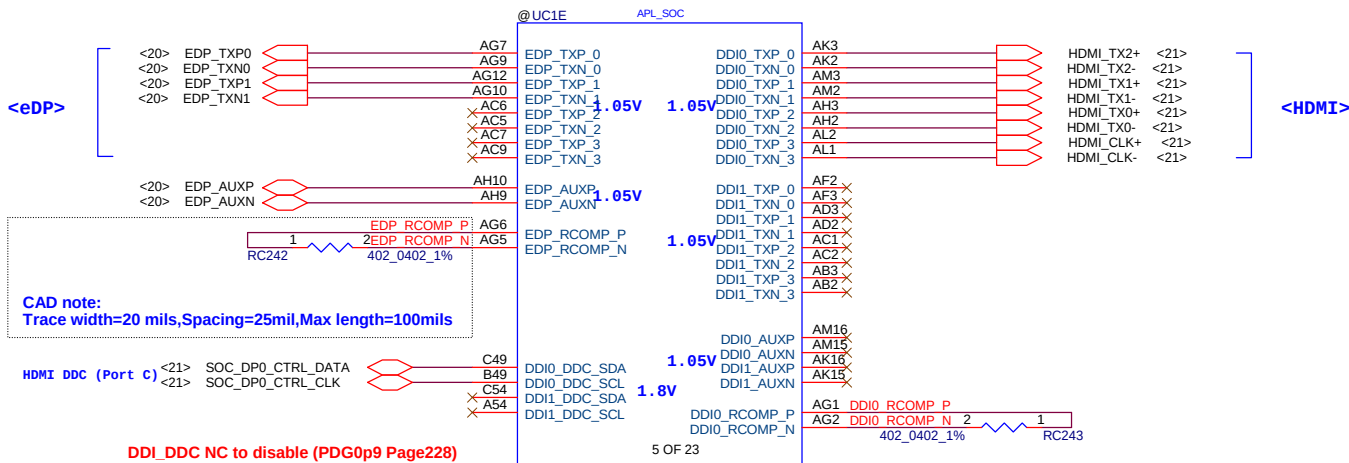
	Power	Touch PAD	Touch Panel
I2C Address		0xXX	0xXX
I2C Port3	+1.8VALW to +TS_PWR	X	V
I2C Port4	+1.8VALW to +3V_PTP	V	X

BOM Option Table		BOM Option Table	
Item	BOM Structure	Item	BOM Structure
Unpop	@	with BYOC	BYOC@
Connector	CONN@	without BYOC	NBYOC@
EMC requirement	EMC@	EMMC	EMMC@
EMC requirement depop	@EMC@	EMMC V5.0	EMMCV5@
Touch Screen I2C	TSI@	A0 Step need to stuff	A0S@
TPM	TPM@	Kingston 32G EMMC	KINGSTON32G@
NTPM	NTPM@	PRE QS CPU QLB5	QLB5@
Power Button	DBG@	PRE QS CPU QLB6	QLB6@
CODEC(ALC233)	233@	PRE QS CPU QLB8	QLB8@
CODEC(ALC255)	255@	15" PCB 1.0	PCB15@
RTL 8111H	8111H@	17" PCB 1.0	PCB17@
RTL8111GUS	8111GUS@	Memory down	MD@
Hynix DRAM on board	HYN@	15" PCB 1.A	PCB15A@
Samsung DRAM on board	SAM@	17" PCB 1.A	PCB17A@
intel CMC	CMC@	Micron DRAM on board	MCN@

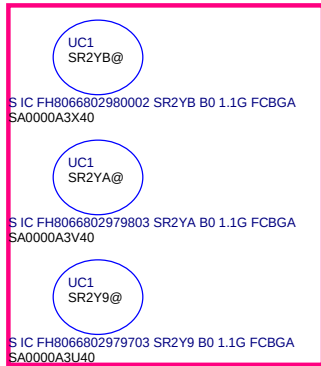
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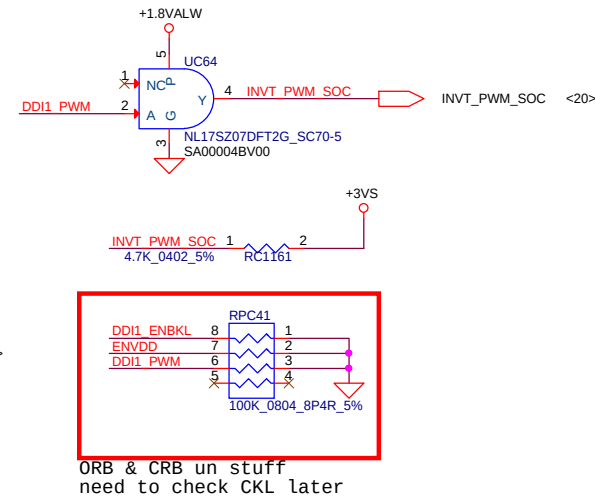
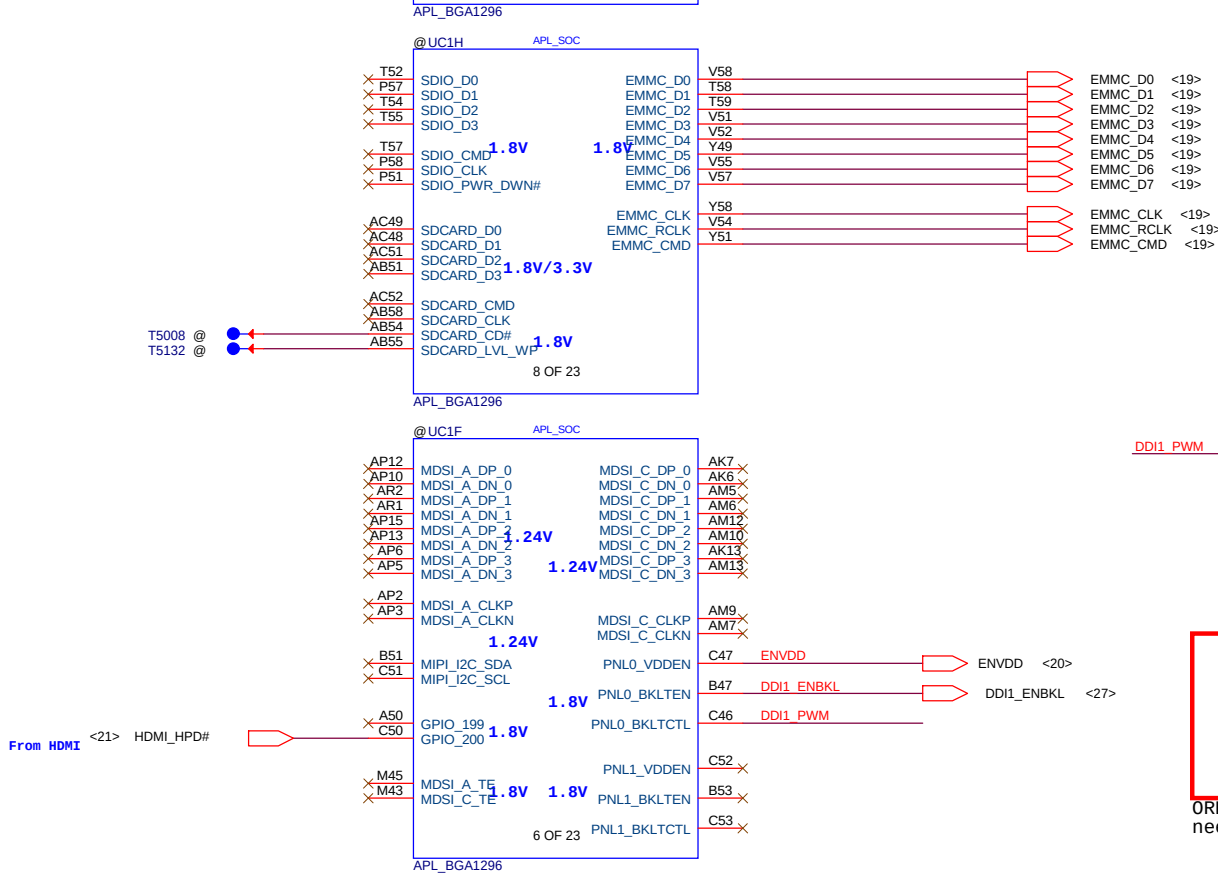
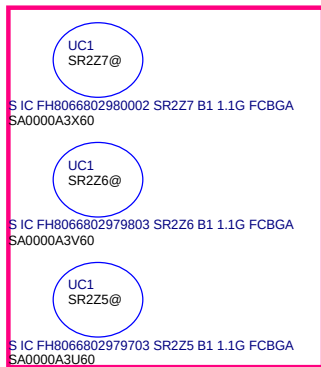
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PreMP modify B0 step

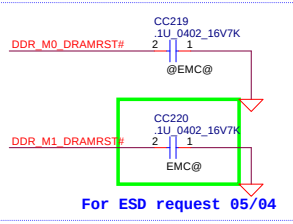
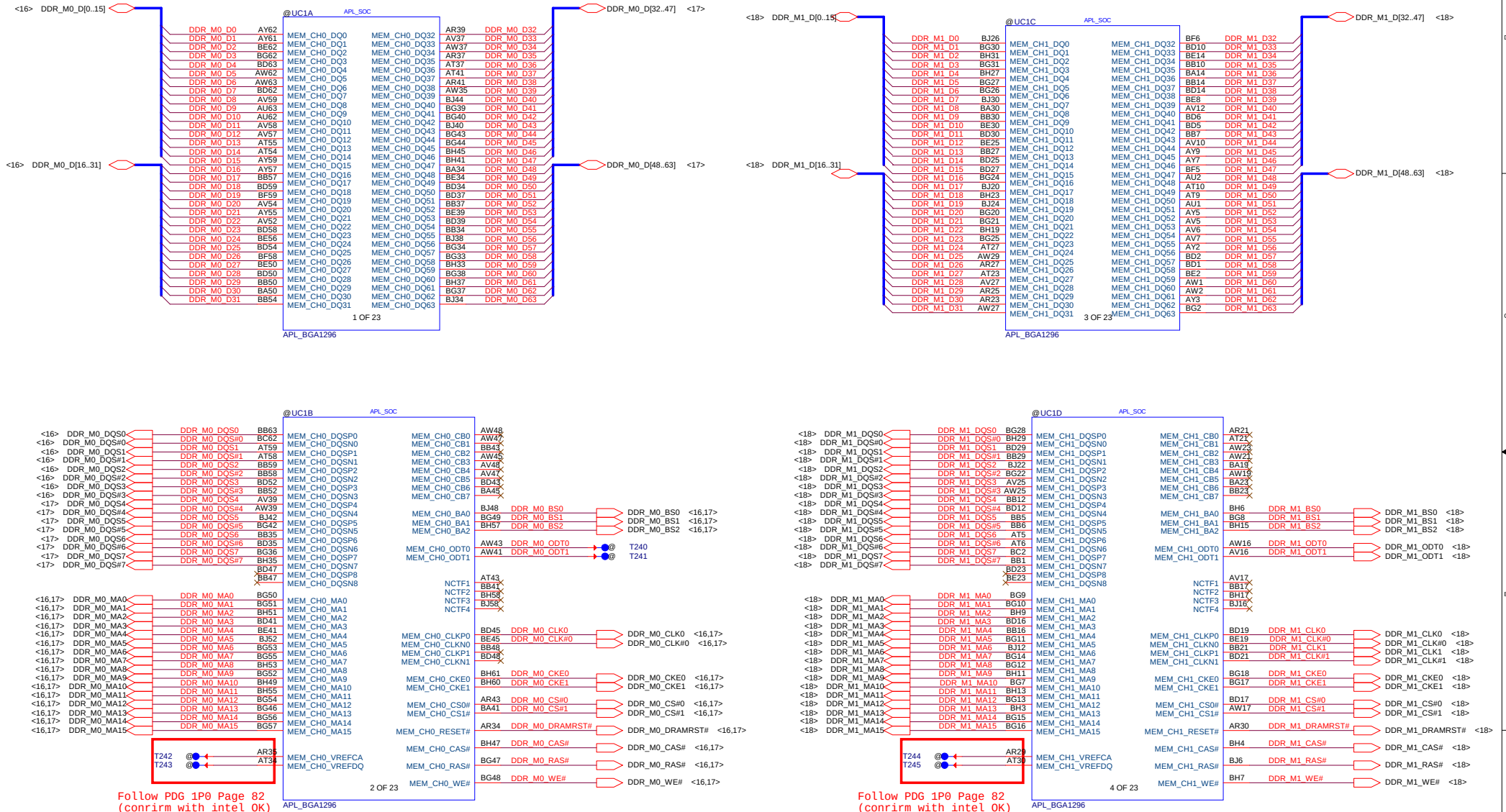


PreMP modify B1 step



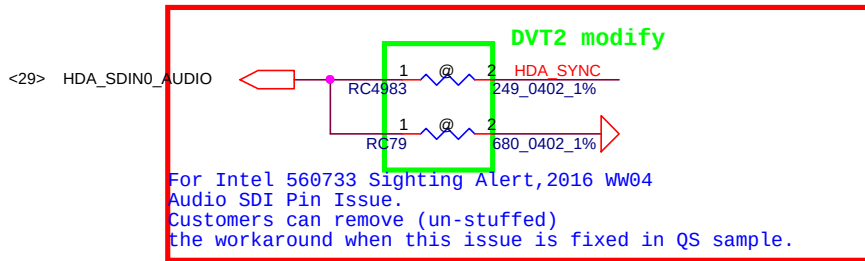
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Non-Interleaved Memory

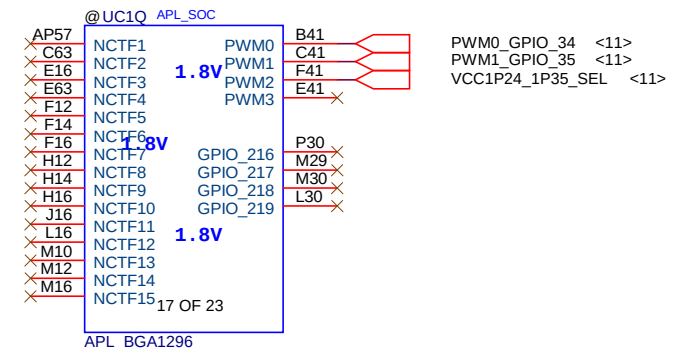
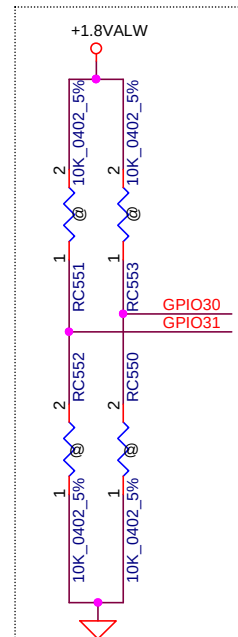
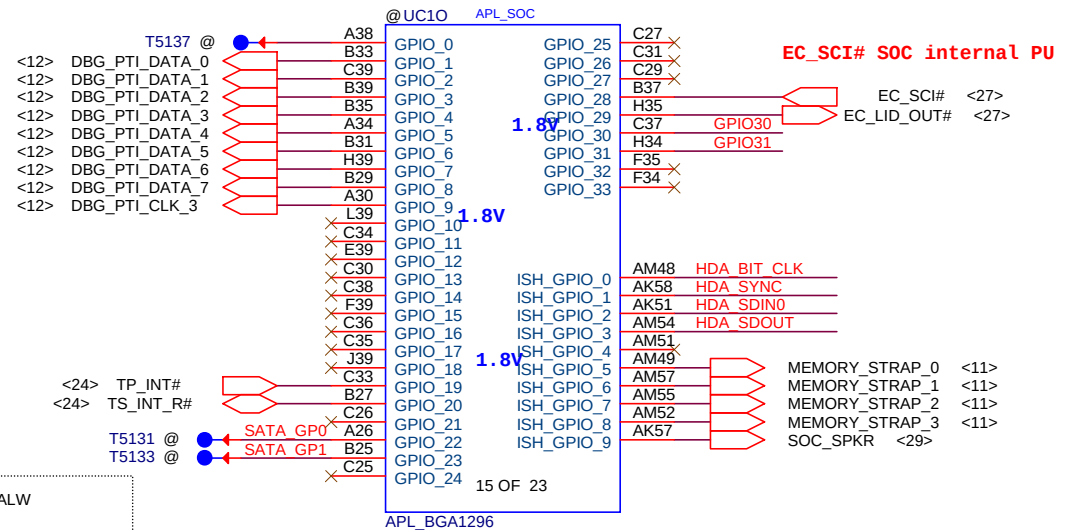
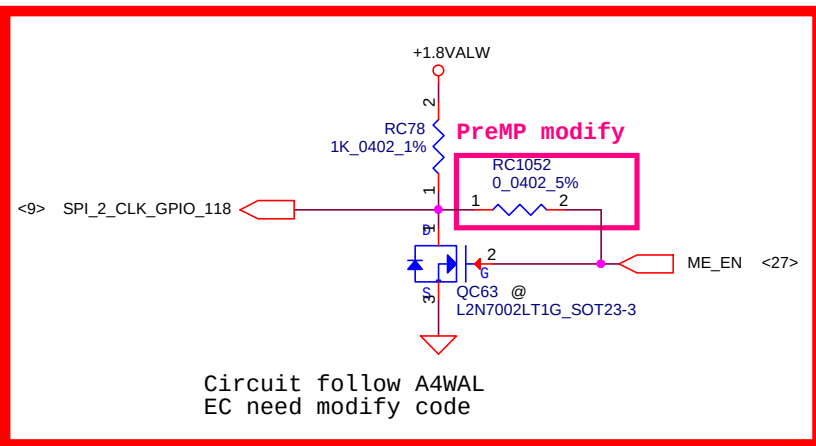
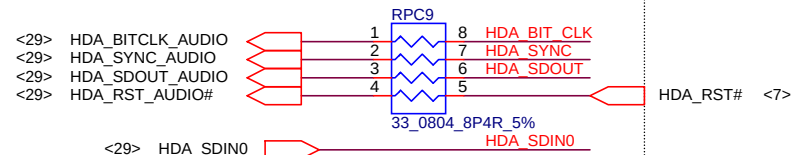


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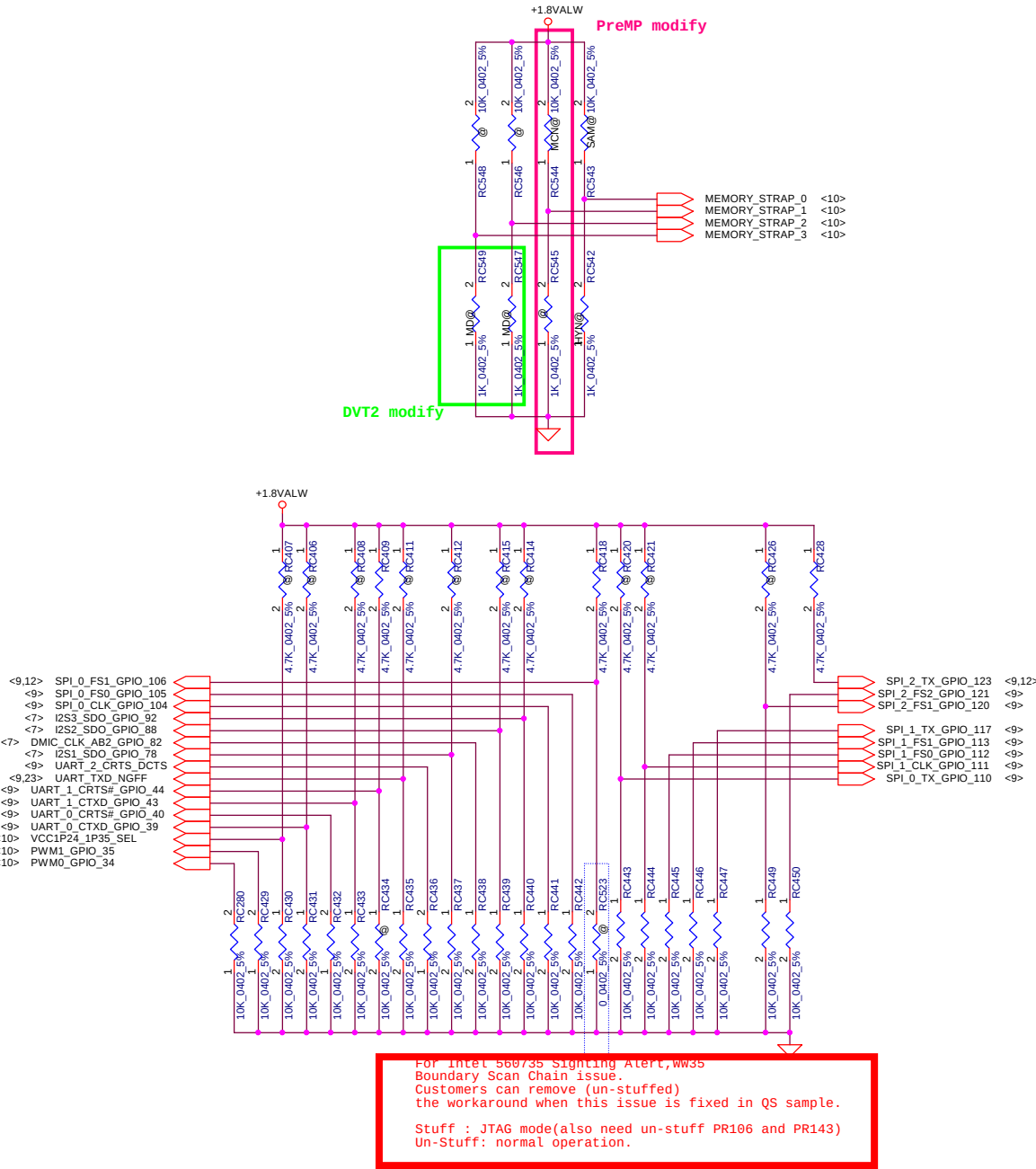
Intel HDA issue, Fix on QS sample 09/01



HDA for AUDIO



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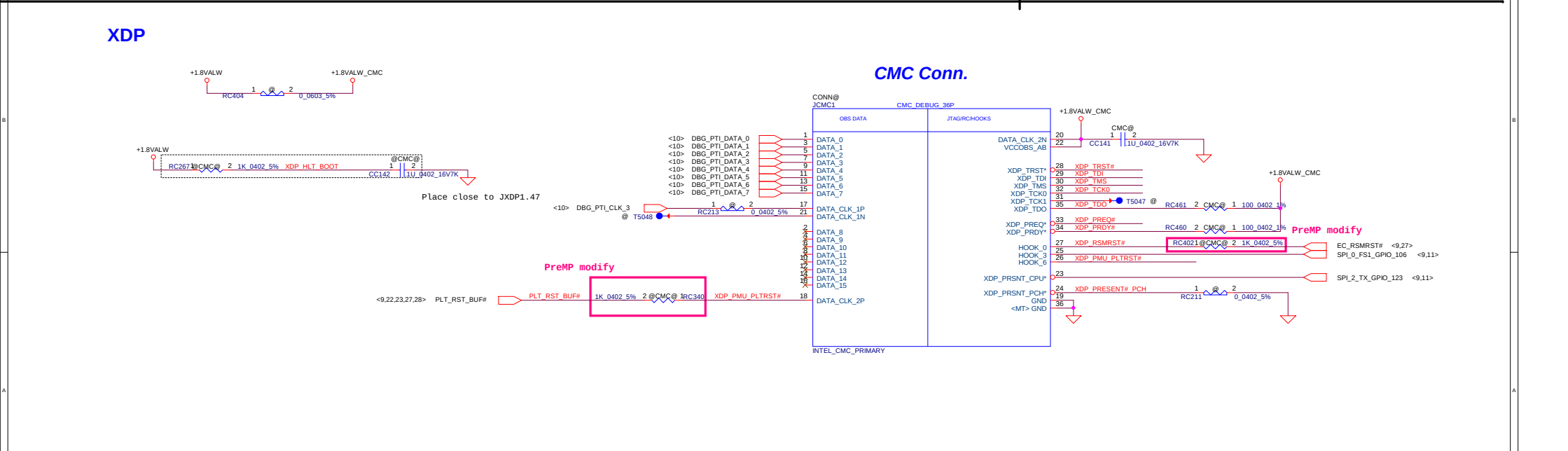
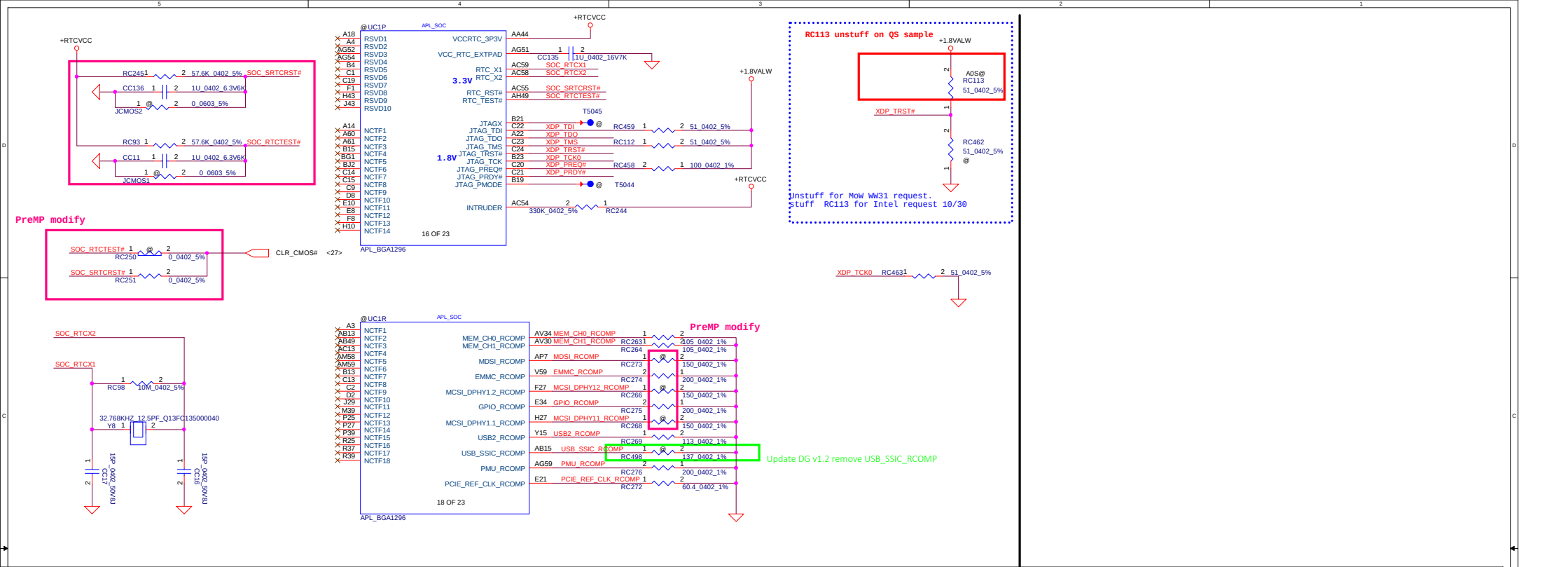
On Board Memory Strap Pin

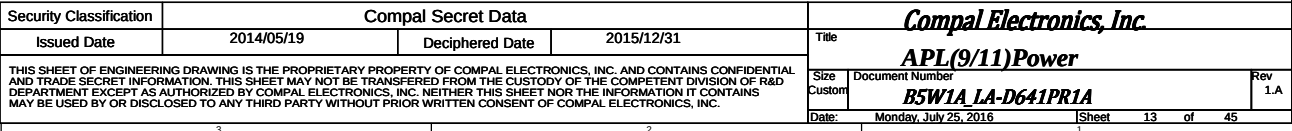
On Board RAM Configuration	RAM_ID3	RAM_ID2	RAM_ID1	RAM_ID0
DDR3L Hynix 256MX16/1600 H5TC4G63CFR-PBA (SA00005AVD0)	0	0	0	0
DDR3L Samsung 256MX16/1600 K4B4G1646E-BYK0 (SA000099X20)	0	0	0	1
DDR3L Micron 256MX16/1600 MT41K256M16TW(SA00009KQ30)	0	0	1	0
SODIMM only	1	1	1	1

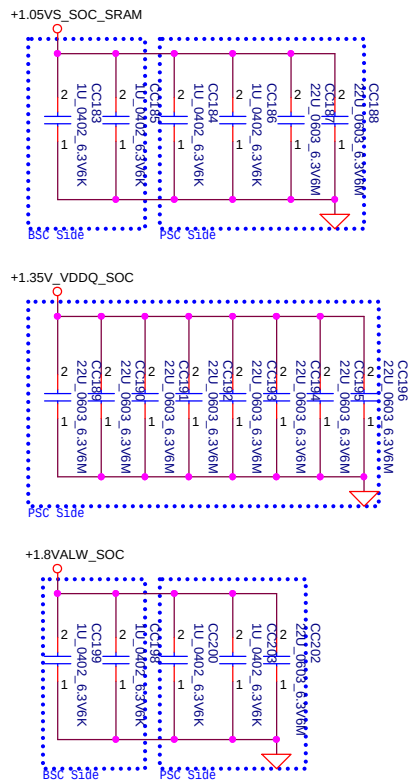
* stand for default value

Pin Name	PU/PD Function	External Termination	Strap pin Description
GPI034		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPI035		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPI036	0: 1.24V* 1: 1.35V	10KPD	VCC_1P24V_1P35V_A voltage selection
GPI039	0: Disable* 1: Enable	10KPD	Enable CSE ROM Bypass
GPI040		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPI043	0: Disable* 1: Enable	4.7KPU	Allow eMMC as a boot source
GPI044	0: Disable* 1: Enable	4.7KPU	Allow SPI as a boot source
GPI047	0: No Force* 1: Force	10KPD	Force DNX FW Load
GPI048		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPI078	0: 3.3V* 1: 1.8V	10KPD	SMBus 1.8V/3.3V mode select
GPI082		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPI088	0: 3.3V* 1: 1.8V	10KPD	PMU 1.8V/3.3V mode select
GPI092	0: Disable* 1: Enable	10KPD	SMBus No Re-Boot
GPI0104		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPI0105		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPI0106		4.7KPU	Pulled HIGH when RSM_RST_N de-asserts
GPI0110	0: 3.3V* 1: 1.8V	10KPD	LPC 1.8V/3.3V mode select
GPI0111	0: From SPI* 1: Don't	10KPD	Boot BIOS from SPI select
GPI0112		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPI0113		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPI0117		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPI0118	0: Don't* 1: Override	10KPD	Flash Descriptor Override
GPI0120	0: Enable* 1: Disable	10KPD	Top swap override
GPI0121		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPI0123		4.7KPU	Pulled HIGH when RSM_RST_N de-asserts

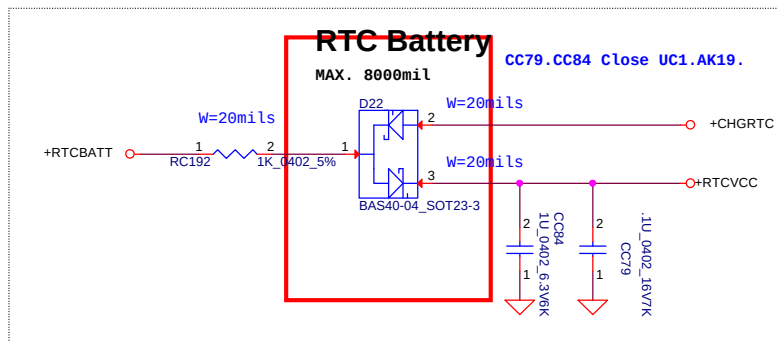
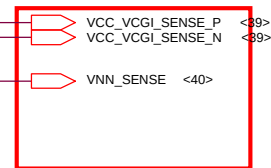
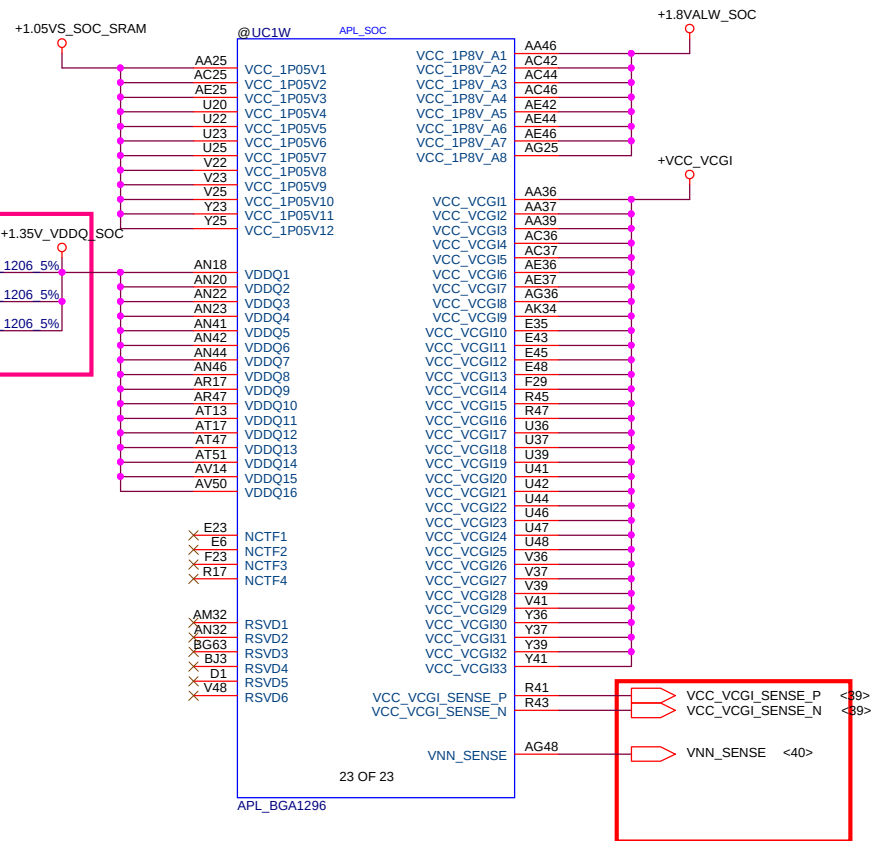
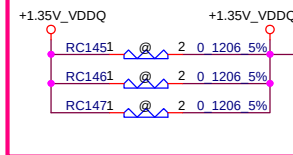
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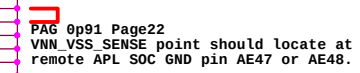




PreMP modify

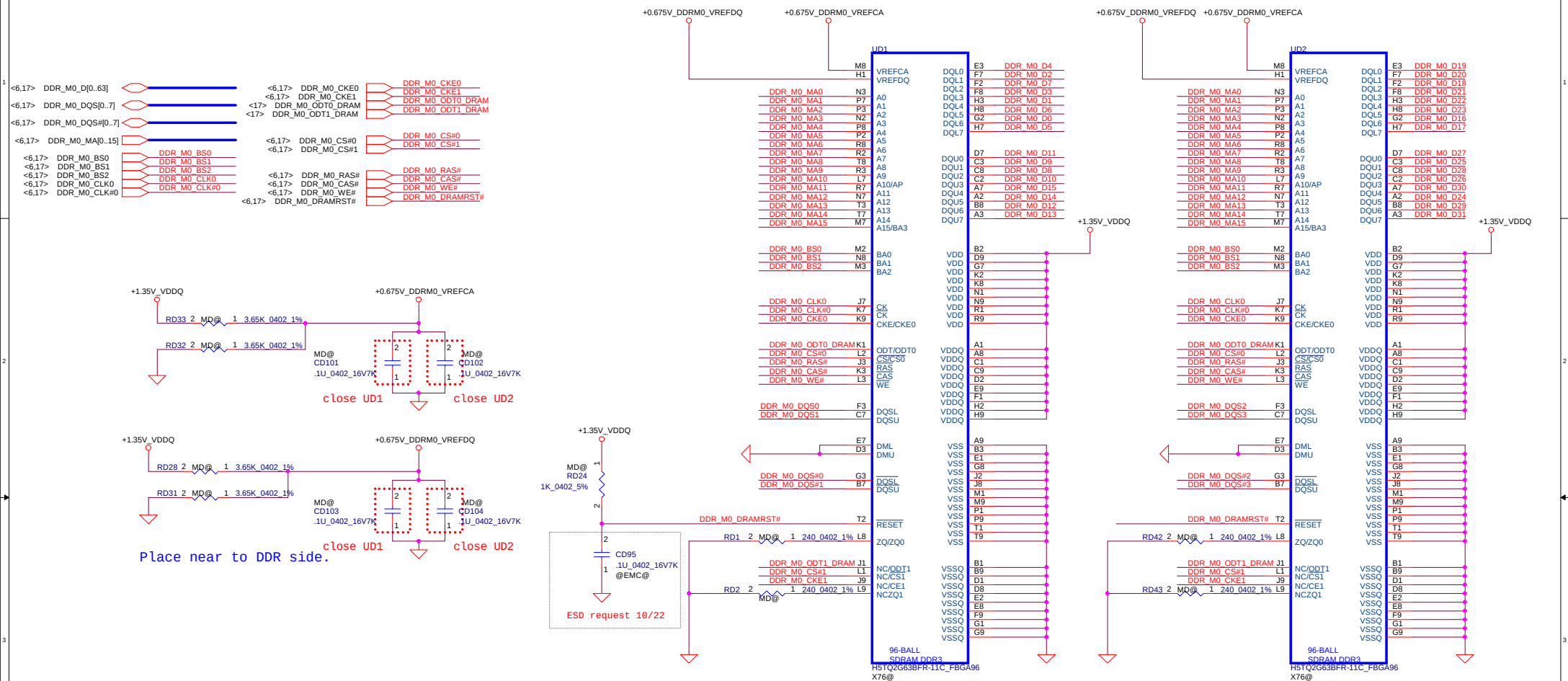


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								Document Number		
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CH0 DDR3L Memory Down Lower Bits

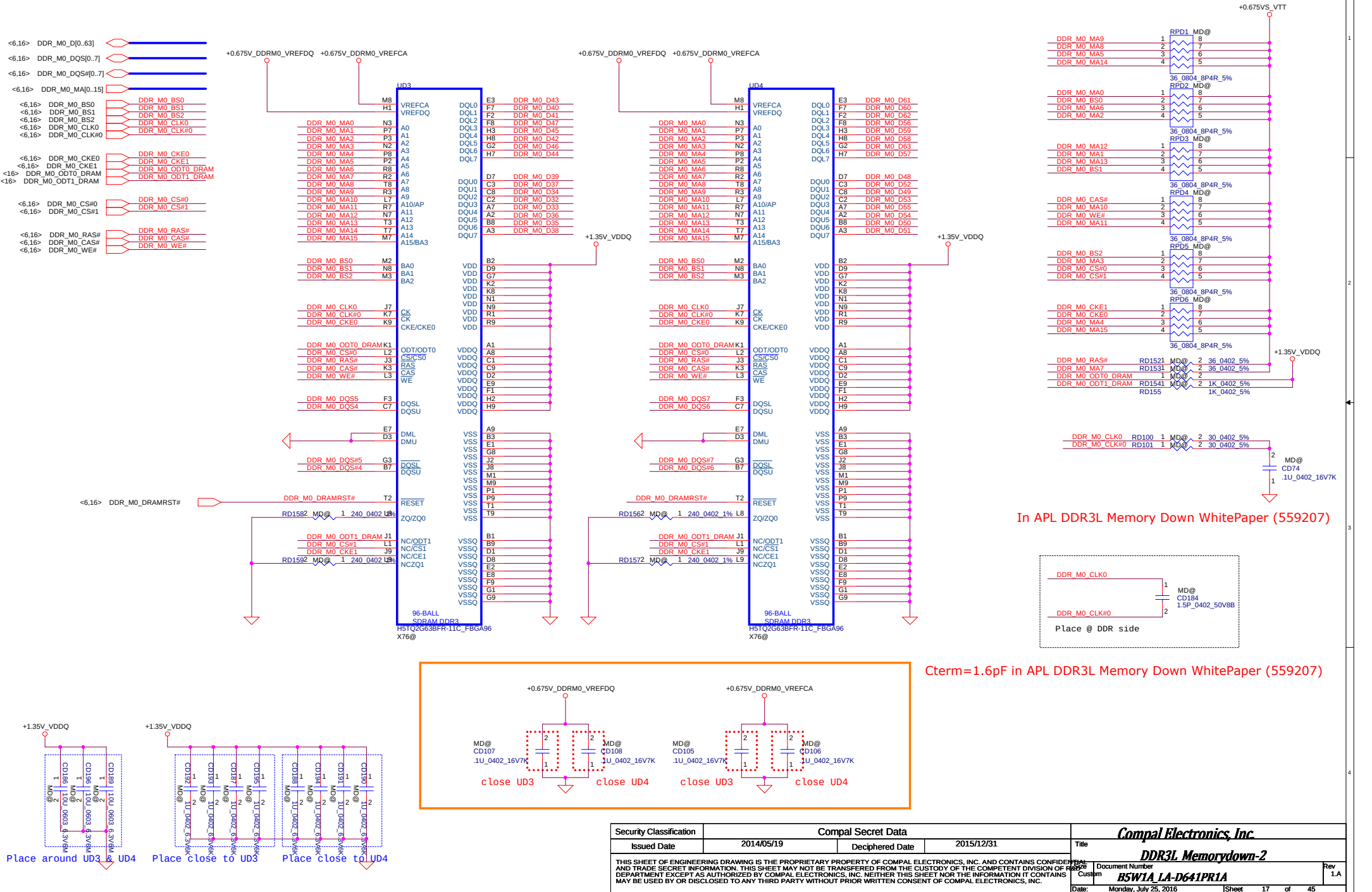


Non-Interleaved Memory

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Issued Date	2014/05/19	Deciphered Date	2015/12/31	Title	DDR3L Memory down-1
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Date: Monday, July 25, 2016				Sheet 16 of 45	

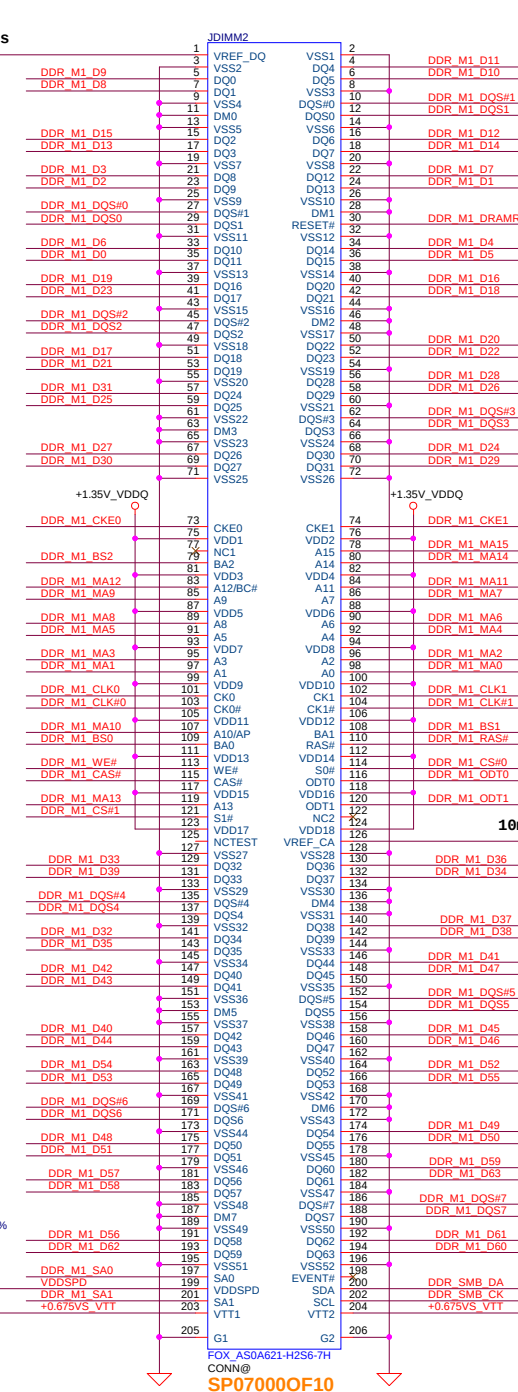
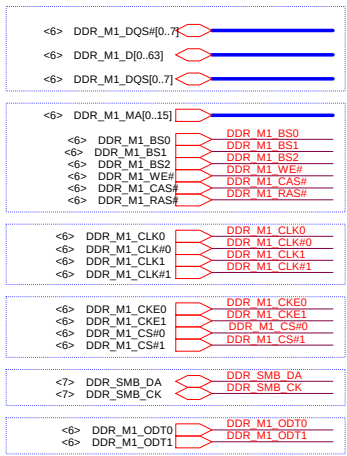
CH0 DDR3L Memory Down Upper Bits

Non-Interleaved Memory

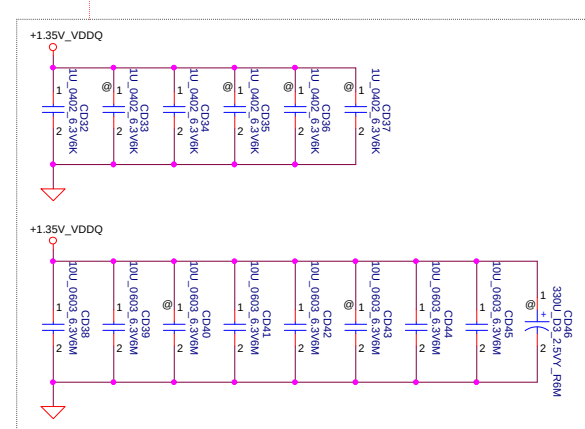


Normal Type

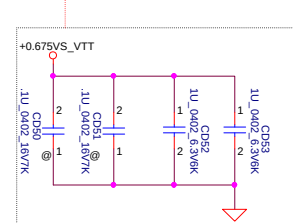
2-3A to 1 DIMMs/channel



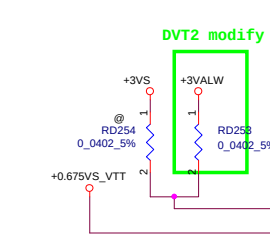
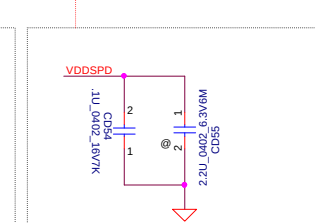
Layout Note:
Place near JDIMM2



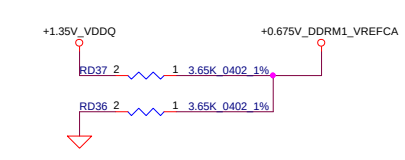
Layout Note:
Place near JDIMM2.203, 204



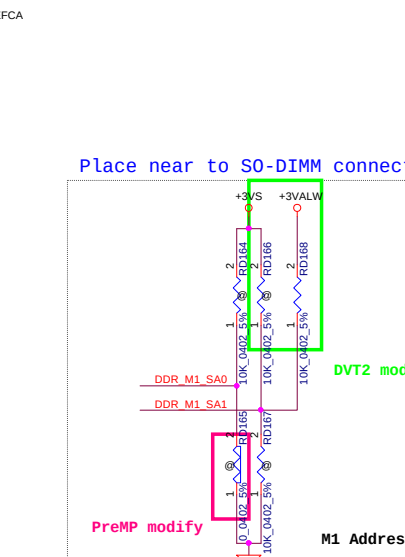
Layout Note:
Place near JDIMM2.199



Place near to S0-DIMM connector.



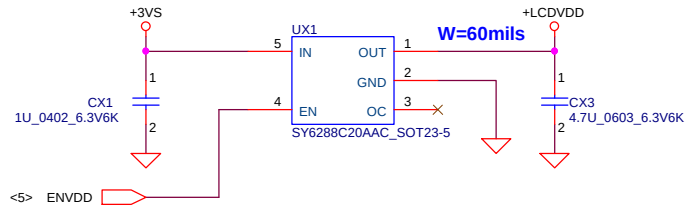
Place near to S0-DIMM connector.



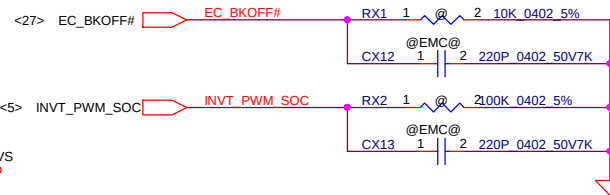
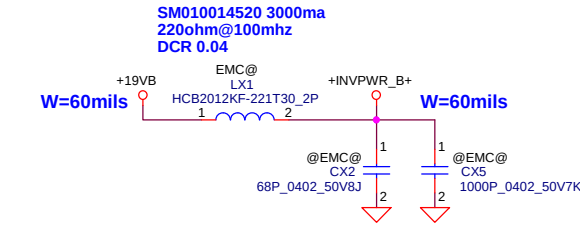
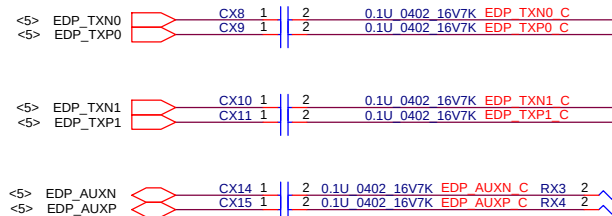
Non-Interleaved Memory

Security Classification	Compal Secret Data		Title	
Issued Date	2014/05/19	Deciphered Date	2015/12/31	Document Number
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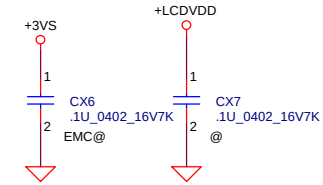
LCD POWER CIRCUIT



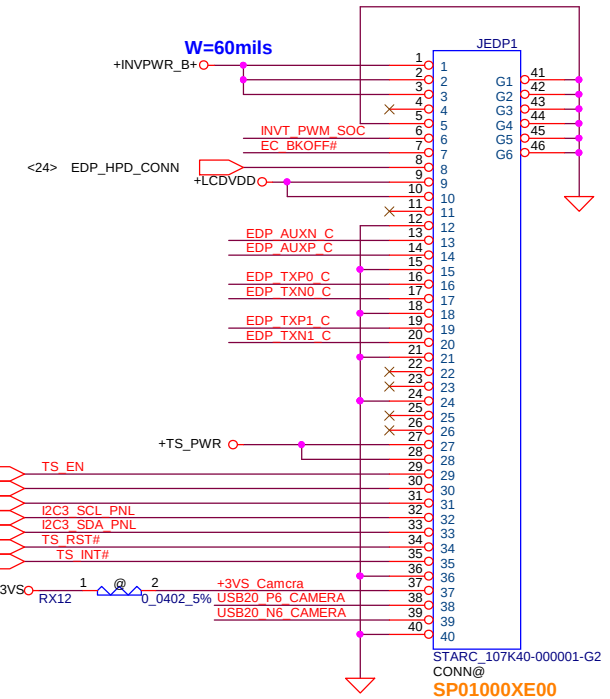
eDP



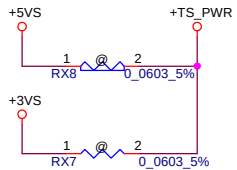
Place closed to JEDP1



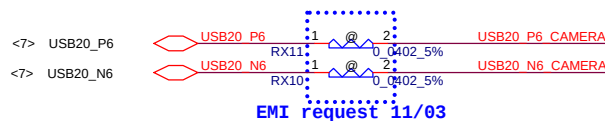
LCD/ LED PANEL Conn.



For Touch Panel



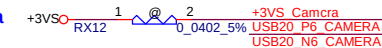
For Camera



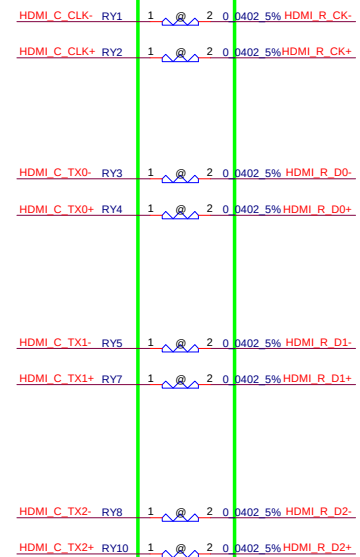
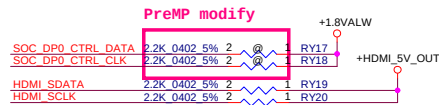
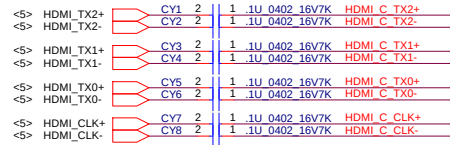
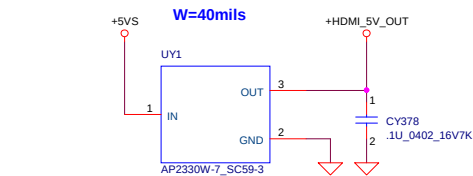
Touch Screen

- <27> TS_EN
- <7> USB20_P5
- <7> USB20_N5
- <9> I2C3_SCL_PNL
- <9> I2C3_SDA_PNL
- <27> TS_RST#
- <24> TS_INT#

For Camera

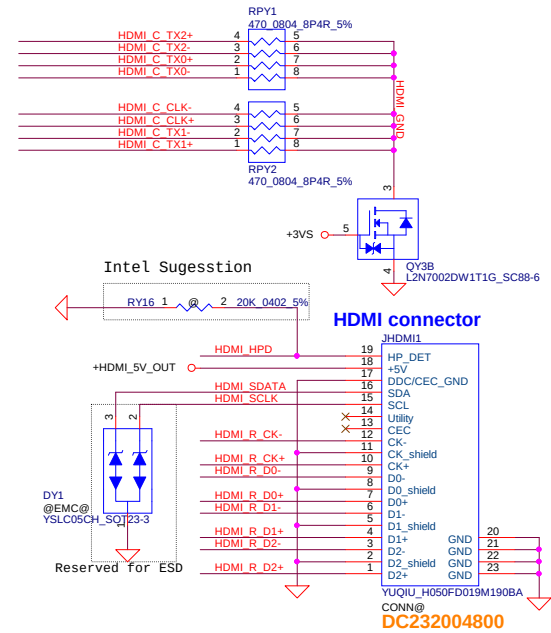
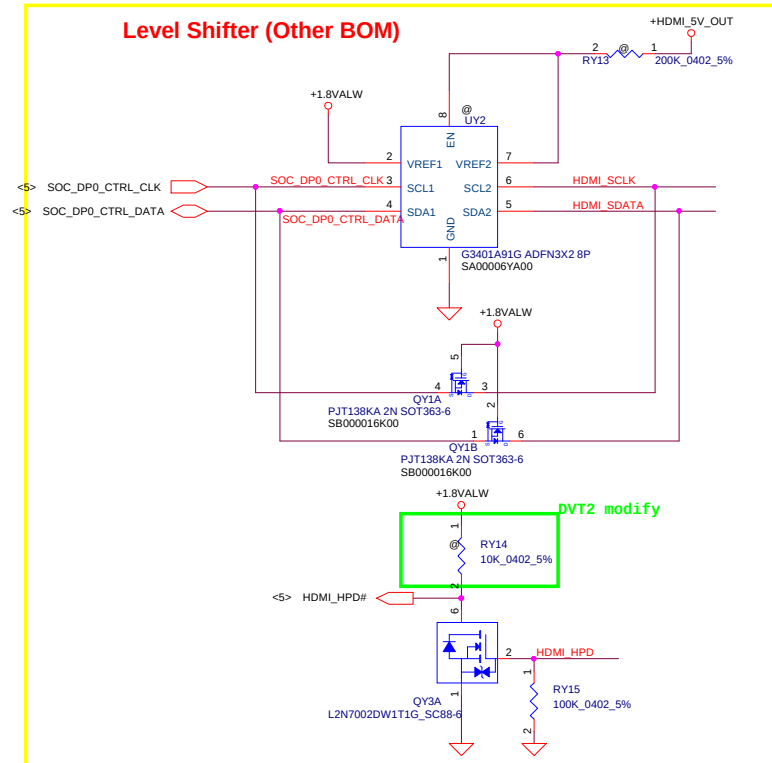


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/03/19	Deciphered Date	2015/03/18	Title		
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				Custom	B5W1A LA-D641PR1A	1.A
				Date:	Monday, July 25, 2016	Sheet 20 of 45



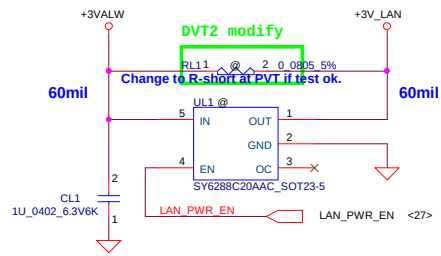
EMI 4/25 confirm OK
DVT2 modify

Level Shifter (Other BOM)



ZZZ1
HDMI ROYALTY
ROYALTY HDMI W/LOGO+HDCP
RO000003HM
45@

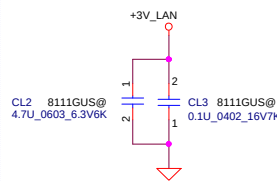
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2014/03/19				Deciphered Date			
2015/03/18				Title				HDMI CONN.			
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Date: Monday, July 25, 2016				B5W1A LA-D641PR1A				1A			
Sheet				21				of 45			



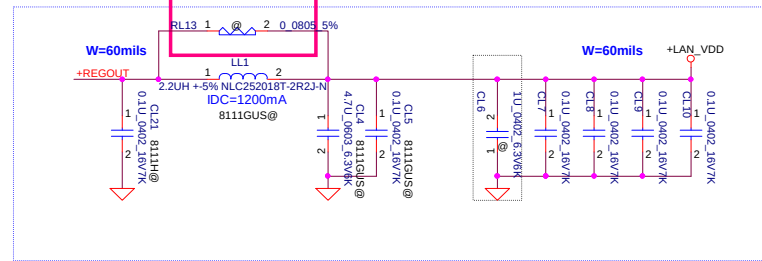
+3V_LAN Rising time request: 0.5~100mS

SA000028Y10
High active.
EN threshold voltage :1.2~2.0V
Current limit threshold :1.5~2.8A
Output turn-on rising time: 1.3~2.7ms

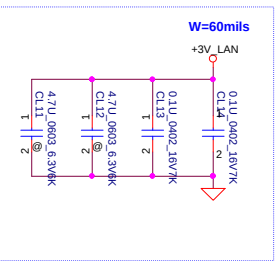
Close to U20
Pin23



(Should be place within 200 mils)
Close to Pin 24



0.1uF close to Pin 11,32



PU to +3VS at PCH
side

<8> LAN_CLKREQ#
<8> PCIE_PTX_C_DRX_P2
<8> PCIE_PTX_C_DRX_N2
<8> CLK_PCIE_LAN
<8> CLK_PCIE_LAN#

UL2
S.I.C RTL8111H-CG QFN 32P E-LAN CTRL
8111H@
SA000080P00

LAN_MIDIO+
LAN_MIDIO-
+LAN_VDD
LAN_MIDI1+
LAN_MIDI1-
LAN_MIDI2+
LAN_MIDI2-
+LAN_VDD
LAN_MIDI3+
LAN_MIDI3-
+3V_LAN

MDIP0
MDIN0
AVDD10
ISOLATEB
MDIP1
MDIN1
MDIP2
MDIN2
AVDD10
REGOUT
LED2
MDIP3
MDIN3
AVDD33
LED0
CLKREQB
HSIP
HSIN
REFCLK_P
REFCLK_N

close to Pin 17,

18

1CL15

1CL16

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

ISOLATEB

LAN_PME#

+LAN_VDD

+REGOUT

LAN_LED2

GPO

XTLO

XTLI

+LAN_VDD

LAN_RST

+3V_LAN

AVDD33

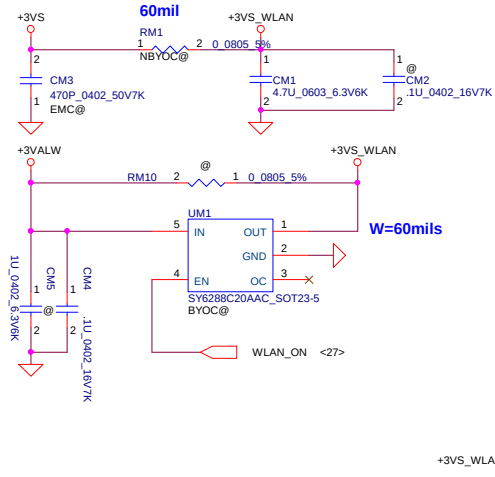
GND

PCIE_PRX_DTX_P2

PCIE_PRX_DTX_N2

PLT_RST_BUF#

For Wireless LAN



<7> USB20_P4
<7> USB20_N4

<8> PCIE_PTX_C_DRX_P3
<8> PCIE_PTX_C_DRX_N3
<8> PCIE_PRX_DTX_P3
<8> PCIE_PRX_DTX_N3
<8> CLK_PCIE_WLAN
<8> CLK_PCIE_WLAN#
<8> WLAN_CLKREQ#
<27> WLAN_PME#

+3VS_WLAN

JNGFF1

1 GND_1
2 3.3VAUX_2
3 USB_D+
4 3.3VAUX_4
5 USB_D-
6 LED1#
7 GND_7
8 PCM_CLK
9 SDIO_CLK
10 PCM_SYNC
11 SDIO_CMD
12 PCM_OUT
13 SDIO_DAT0
14 PCM_IN
15 SDIO_DAT1
16 LED2#
17 SDIO_DAT2
18 GND_18
19 SDIO_DAT3
20 UART_WAKE
21 SDIO_WAKE
22 UART_TX
23 SDIO_RST

25 GND_33
26 PET_RX_P0
27 PET_RX_N0
28 PET_RX_P0
29 PET_RX_N0
30 GND_39
31 PER_TX_P0
32 PER_TX_N0
33 GND_45
34 REFCLK_P0
35 REFCLK_N0
36 GND_51
37 CLKREQ#
38 PEWAKE#
39 W_DISABLE#
40 W_DISABLE1#
41 I2C_DAT
42 I2C_CLK
43 RSVD/PCIE_RX_P1
44 RSVD/PCIE_RX_N1
45 GND_63
46 RSVD/PCIE_TX_P1
47 RSVD/PCIE_TX_N1
48 GND_69
49 RSVD_71
50 RSVD_73
51 RSVD_75
52 GND_75
53 GND1

BELLW 80152-3221
CONN@
SP070013E00

P80CLK and BT_ON enable separate.

UART_RX
UART_RTS
UART_CTS
Clink_RST
Clink_DATA
Clink_CLK
COEX3
COEX2
COEX1
SUSCLK(32KHz)
PERST0#
W_DISABLE#
W_DISABLE1#
I2C_DAT
I2C_CLK
RSVD/PCIE_RX_P1
RSVD/PCIE_RX_N1
RSVD/PCIE_TX_P1
RSVD/PCIE_TX_N1
RSVD_68
RSVD_70
RSVD_72
RSVD_74
RSVD_76
GND1

24 3.3VAUX_2
25 3.3VAUX_4
26 LED1#
27 PCM_CLK
28 PCM_SYNC
29 PCM_OUT
30 PCM_IN
31 LED2#
32 GND_18
33 UART_WAKE
34 UART_TX
35 UART_RX
36 UART_RTS
37 UART_CTS
38 Clink_RST
39 Clink_DATA
40 Clink_CLK
41 COEX3
42 COEX2
43 COEX1
44 SUSCLK(32KHz)
45 PERST0#
46 W_DISABLE#
47 W_DISABLE1#
48 I2C_DAT
49 I2C_CLK
50 RSVD/PCIE_RX_P1
51 RSVD/PCIE_RX_N1
52 RSVD/PCIE_TX_P1
53 RSVD/PCIE_TX_N1
54 RSVD_68
55 RSVD_70
56 RSVD_72
57 RSVD_74
58 RSVD_76
59 GND1

ES1TXD_P80DATA_R 1
ES1RXD_P80CLK_R 1
ES1TXD_P80DATA <27>
ES1RXD_P80CLK <27>

BT_ON
WL_OFF#
MINI1_SMBDATA RM8 1
MINI1_SMBCLK RM9 1

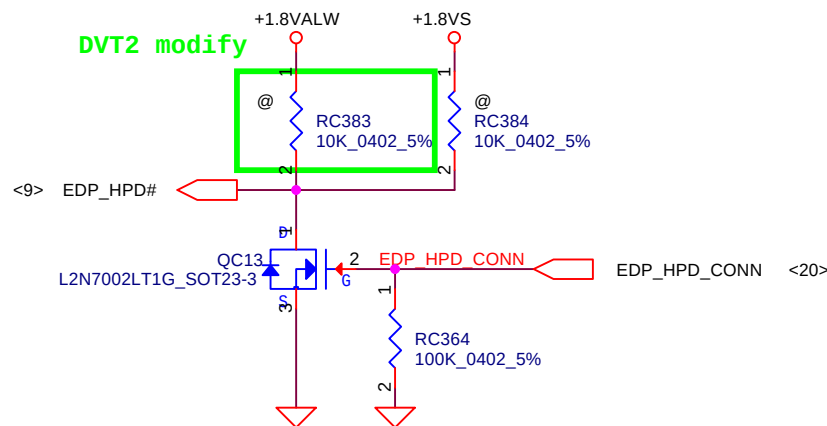
PLT_RST_BUF# <9,12,22,27,28>
BT_ON <27>
WL_OFF# <27>
EC_SMB_DA2 <27>
EC_SMB_CK2 <27>

NGFF WL+BT (KEY E)

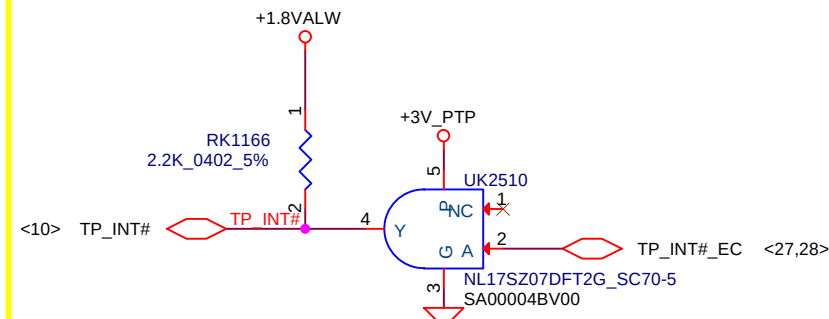
74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UM_Power_SRC/GPIO/PEWAKE#	RESERVED/REFCLKP1	71
68	UM_Power_SINK/CLAREQ#	GND	69
66	UM_SWP/PERST1#	Reserved/PER01	67
64	RESERVED	GND	65
62	ALERT# (I/O/3.3)	Reserved/PET01	61
60	DC CLK (I/O/3.3)	Reserved/PET01	59
58	DC DATA (I/O/3.3)	Reserved/PET01	57
56	VL_DISABLE# (I/O/3.3V)	GND	57
54	Reserved/V_DISABLE# (I/O/3.3V)	PEWAKE# (I/O/3.3V)	55
52	PERST0# (I/O/3.3V)	CLKREQ# (I/O/3.3V)	53
50	SUSCLK(32KHz) (I/O/3.3V)	GND	51
48	COEX1 (I/O/1.8V)	REFCLKN0	49
46	COEX2 (I/O/1.8V)	REFCLKP0	47
44	COEX3 (I/O/1.8V)	GND	45
42	VENDOR DEFINED	PER00	43
40	VENDOR DEFINED	PER00	41
38	VENDOR DEFINED	PET00	37
36	UART RTS (I/O/1.8V)	PET00	35
34	UART CTS (I/O/1.8V)	GND	33
32	UART Tx (I/O/1.8V)	GND	31
30	UART Rx (I/O/1.8V)	GND	29
28	UART Wake# (I/O/3.3V)	GND	27
26	GND	GND	25
24	PCIE_OUT/IS_SD_OUT (I/O/1.8V)	SDIO Reset# (I/O/1.8V)	23
22	PCIE_IN/IS_SD_IN (I/O/1.8V)	SDIO Wake# (I/O/1.8V)	21
20	PCIE_SYNC/IS_VS (I/O/1.8V)	SDIO DAT0 (I/O/1.8V)	19
18	PCIE_CLK/IS_SCK (I/O/1.8V)	SDIO DAT1 (I/O/1.8V)	17
16	LED#1 (I/O/1.8V)	SDIO DAT2 (I/O/1.8V)	15
14	LED#2 (I/O/1.8V)	SDIO DAT3 (I/O/1.8V)	13
12	LED#3 (I/O/1.8V)	SDIO DAT4 (I/O/1.8V)	11
10	LED#4 (I/O/1.8V)	SDIO DAT5 (I/O/1.8V)	9
8	LED#5 (I/O/1.8V)	SDIO DAT6 (I/O/1.8V)	7
6	LED#6 (I/O/1.8V)	SDIO DAT7 (I/O/1.8V)	5
4	LED#7 (I/O/1.8V)	SDIO DAT8 (I/O/1.8V)	3
2	LED#8 (I/O/1.8V)	SDIO DAT9 (I/O/1.8V)	1

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				Rev	1.A
				Date	Monday, July 25, 2016
				Sheet	23 of 45

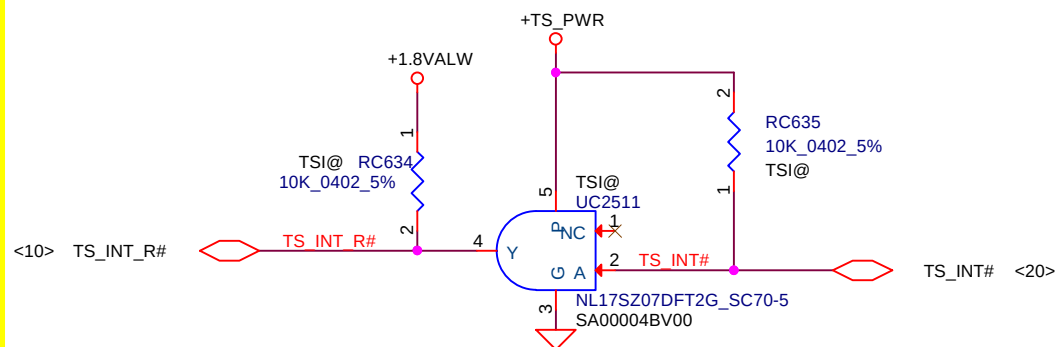
eDP Level Shifter (Other for BOM)



TP_INT Level Shifter

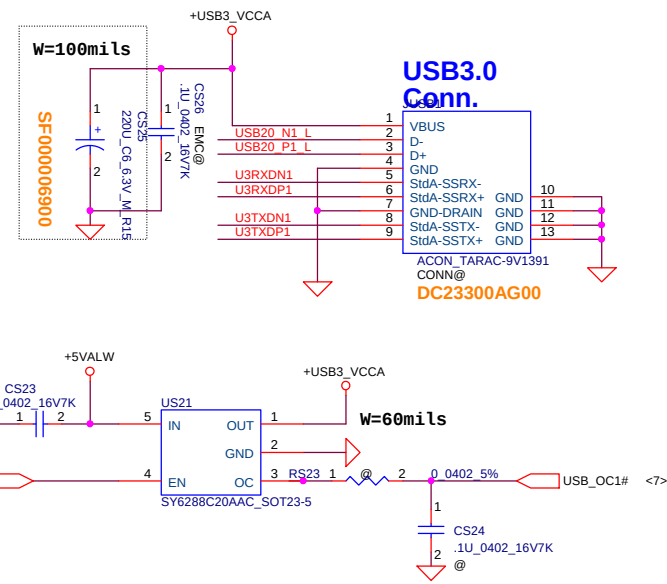
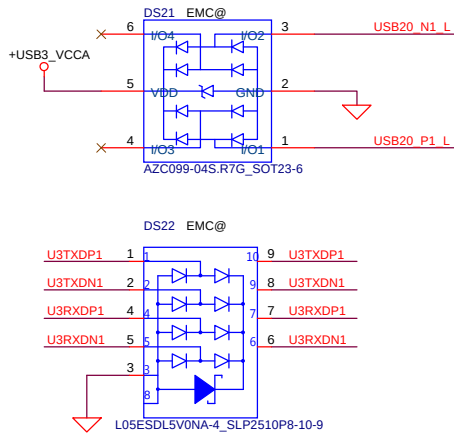
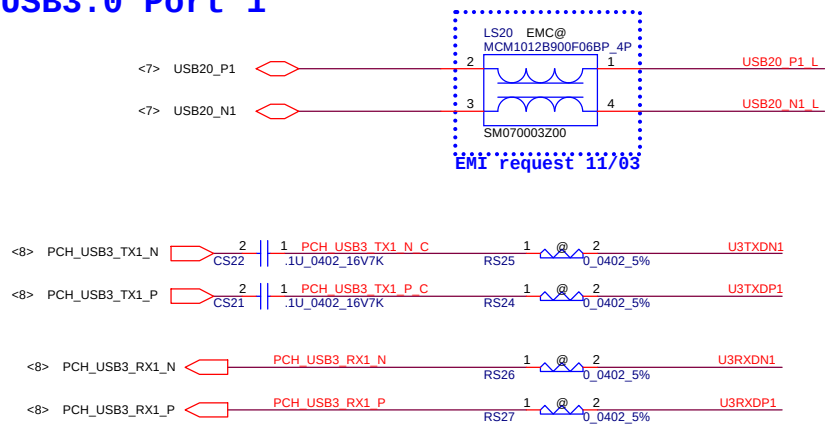


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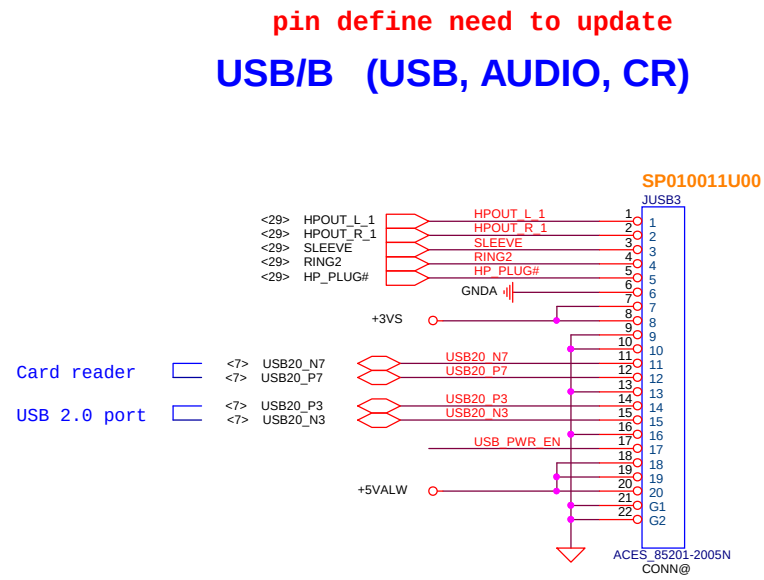
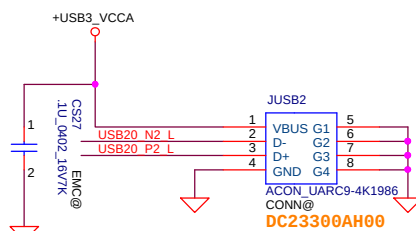
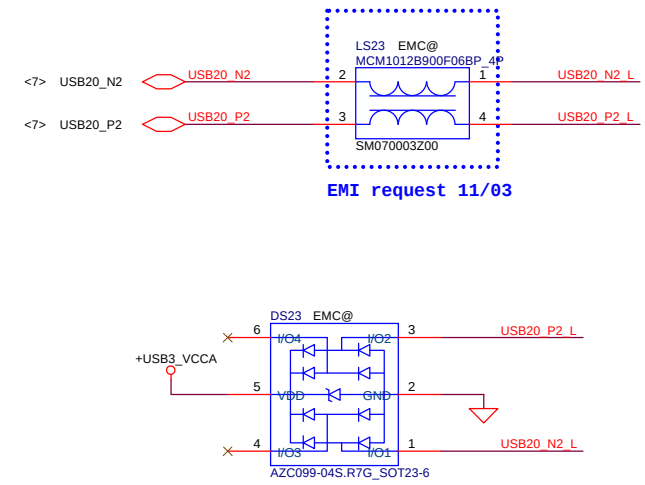


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				Size Custom	Rev 1.A
				Document Number	
				B5W1A_LA-D641PR1A	
				Date: Monday, July 25, 2016	Sheet 24 of 45

USB3.0 Port 1

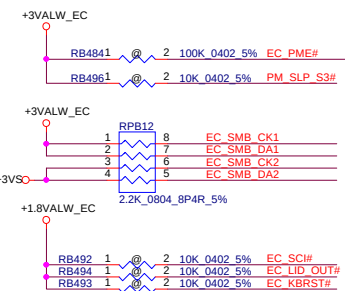
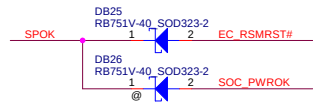


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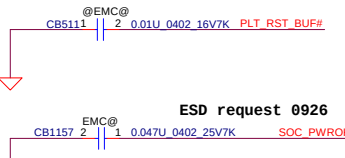


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Issued Date		2014/08/28		Deciphered Date		2016/08/28		Title			
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						Size		Document Number		Rev	
						Custom		B5W1A LA-D641PR1A		1.A	
						Date:		Monday, July 25, 2016		Sheet 26 of 45	

For abnormal shutdown



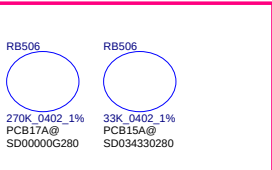
ESD request 0926



Charger and BATT

To SOC

For 1A Board ID
PreMP modify



Board ID

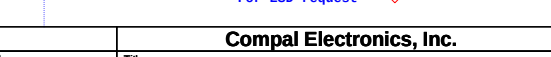
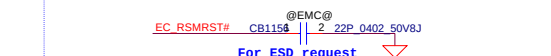
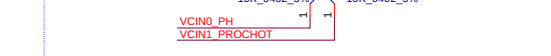
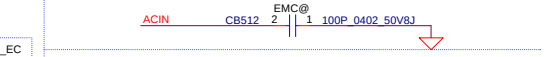
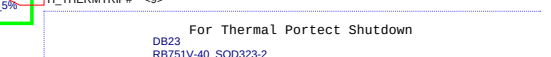
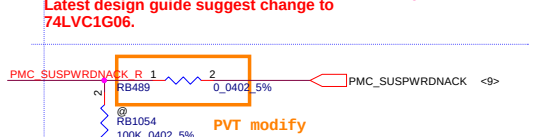
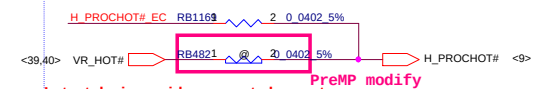
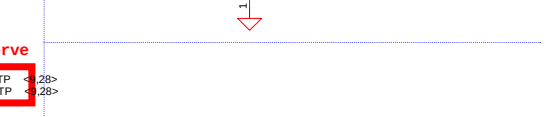
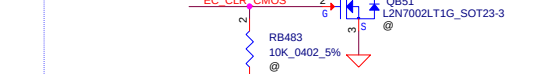
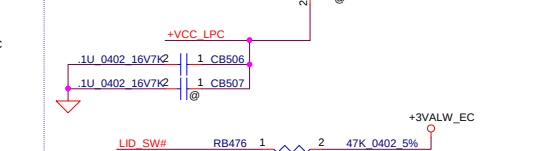
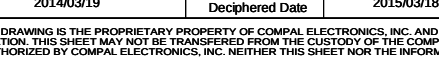
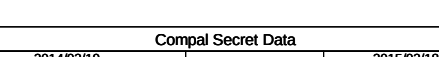
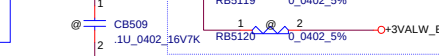
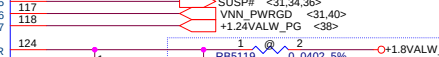
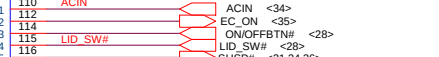
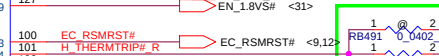
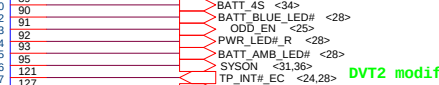
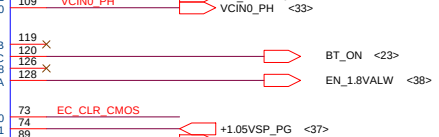
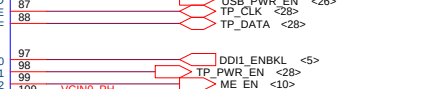
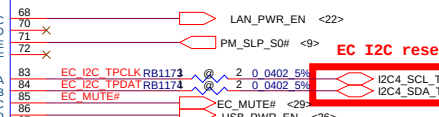
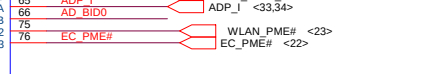
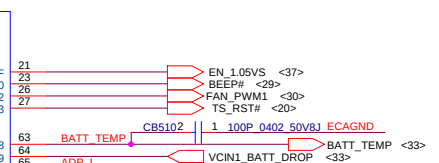
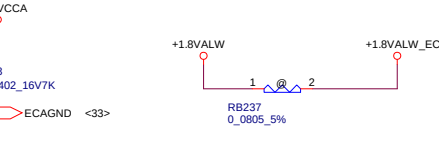
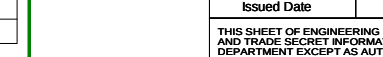
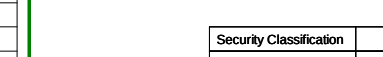
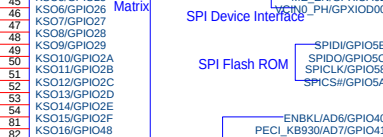
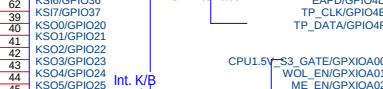
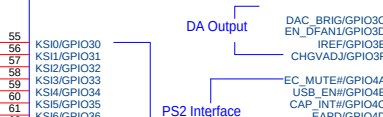
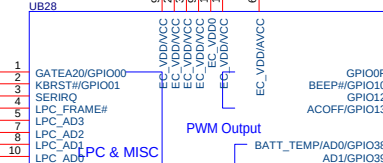
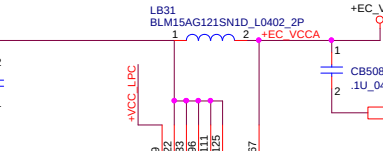
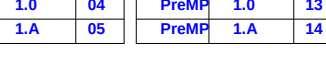
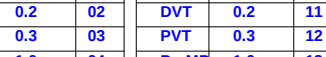
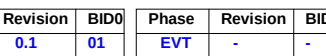
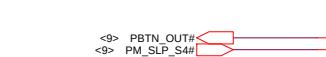
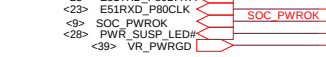
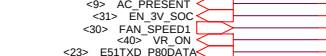
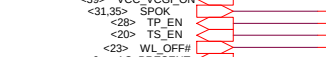
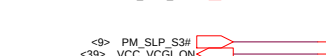
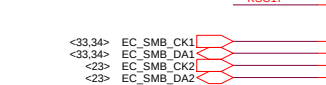
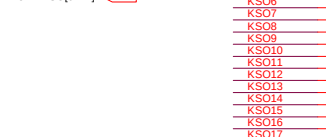
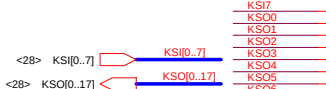
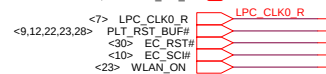
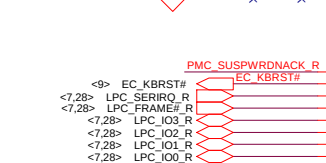
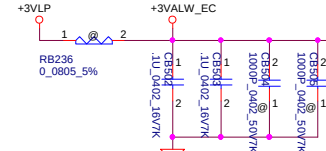
Analog Board ID definition,
Please see page 3.

15"

Phase	Revision	BID0
EVT	0.1	01
DVT	0.2	02
PVT	0.3	03
PreMP	1.0	04
PreMP	1.A	05

17"

Phase	Revision	BID1
EVT	-	-
DVT	0.2	11
PVT	0.3	12
PreMP	1.0	13
PreMP	1.A	14



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				Date	Monday, July 25, 2016
				Sheet	27 of 45



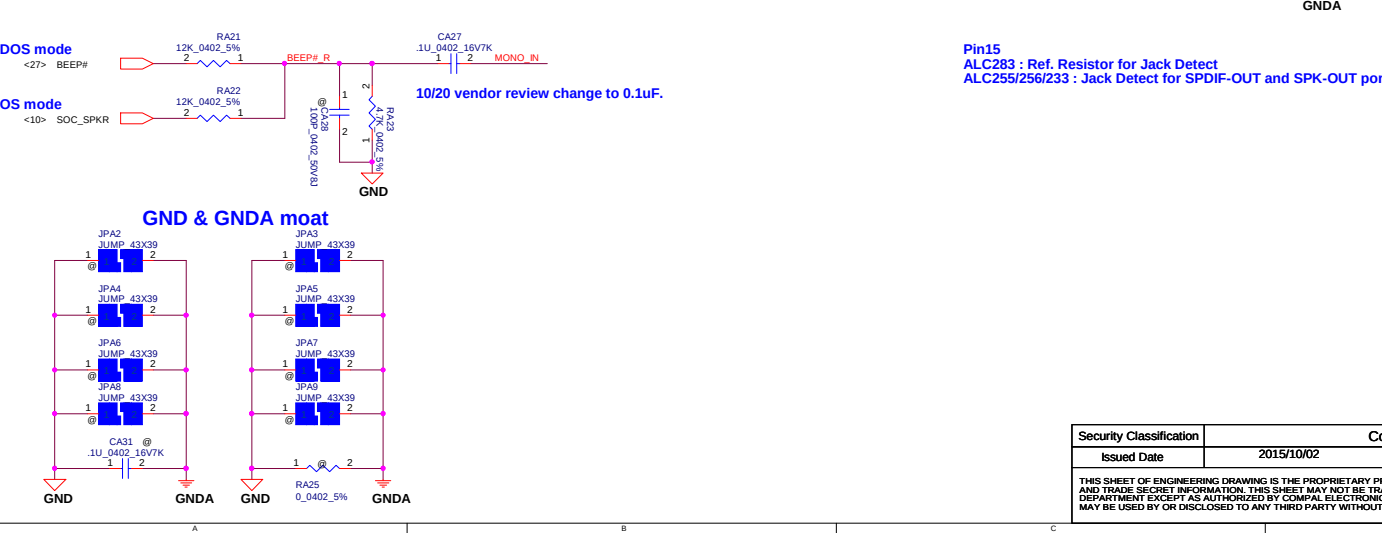
avoid flash issue wh
shoemall, shoemall

SA00008EL40, S IC NPCT650AB1YX QFN 32P TPM

Security Classification		Compal Secret Data		Compal Electronics, Inc.			
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				B5W1A LA-D641PR1A		1A	
				Date: Monday, July 25, 2016	Sheet 28 of 45		

SM01000EJ00 3000mA 220ohm@100mhz DCR 0.04

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[illegible]

Place near Codec

15mil

15mil

0.0603_5%

INT MIC R

INT MIC R 1

AMIC1

CA14

EMC@

220P_0402_50V7K

GND A

GETTOP SOM4013SL-G423-RC

CY000002V00

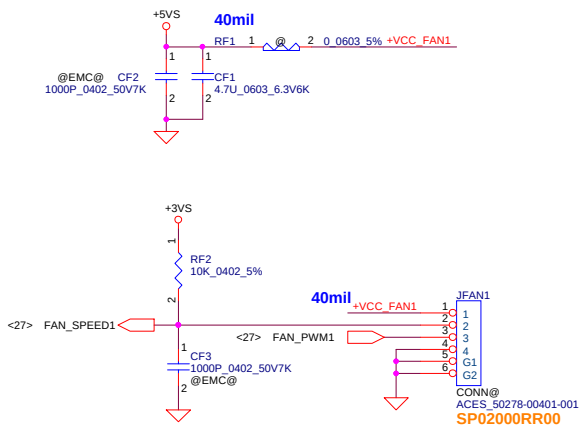
Omnidirectional

Follow EA52_BM(LA-B511P) footprint

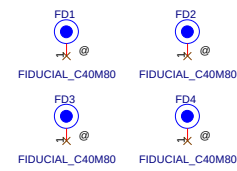
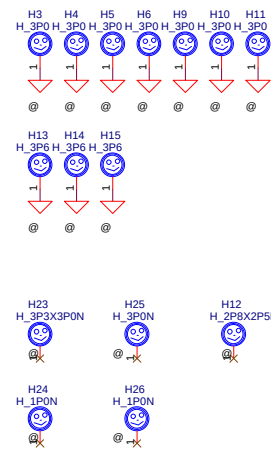
The diagram shows a circuit for the SLEEVE and RING2 signals. A common node is connected to +MIC2_VREF0 through a resistor labeled RA19 (2.2K_0402_5%). This same node is also connected to the RING2 signal through a resistor labeled RA20 (2.2K_0402_5%). The SLEEVE signal is shown as a single line, while RING2 is shown as a differential pair. The output signals are labeled SLEEVE <26> and RING2 <26>.

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				HD Audio Codec ALC255/ALC233 Colay					
				Size		Document Number		Rev	
				Customer		B5W1A LA-D641PR1A		1.A	
				Date:		Monday, July 25, 2016			
				Sheet		29 of 45			

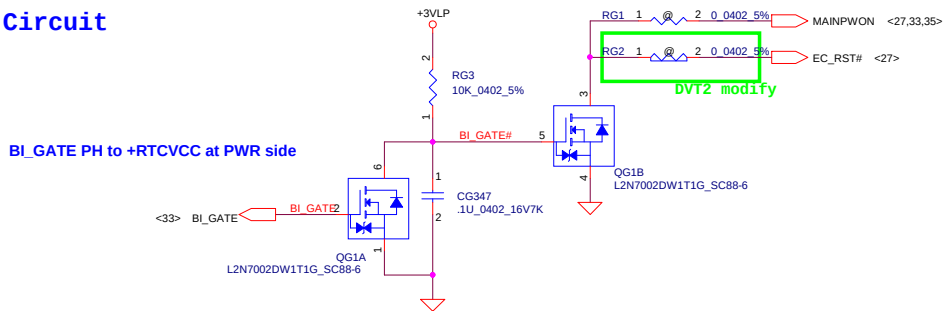
FAN1 Conn



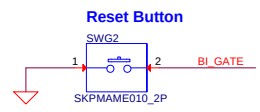
Screw Hole



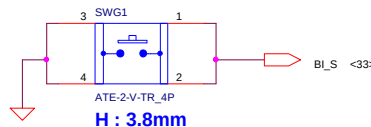
Reset Circuit



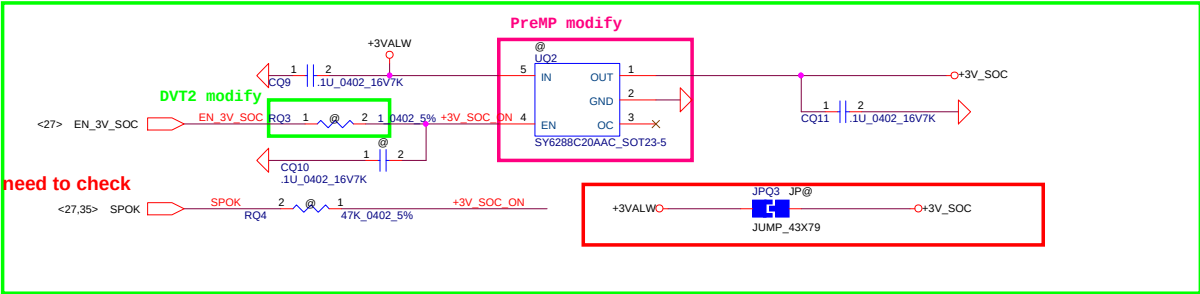
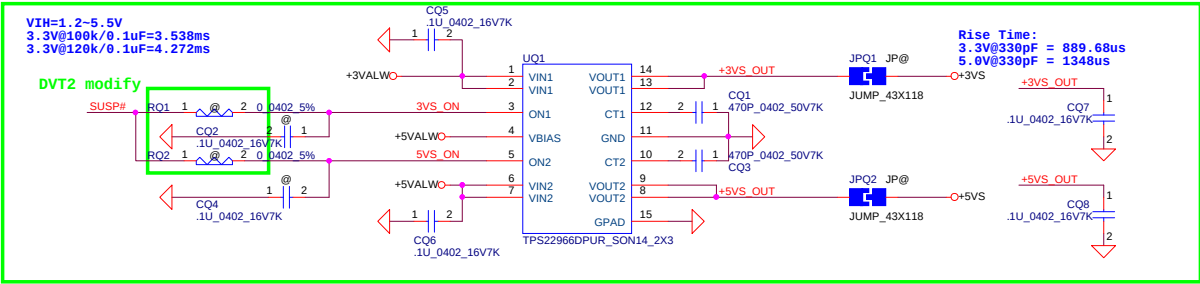
Reset Button



BI SW

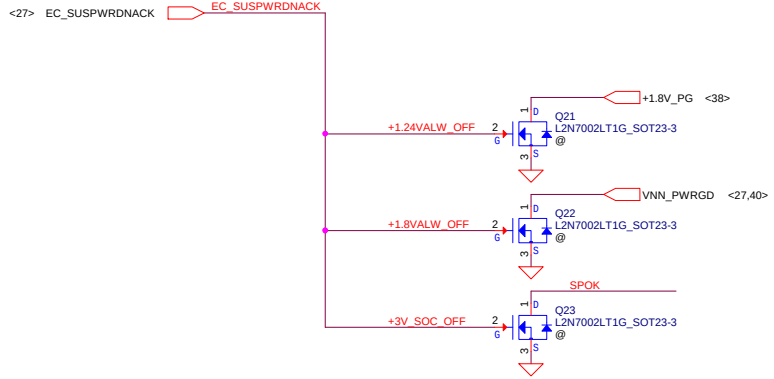


Release : Battery Off
Push : Battery ON

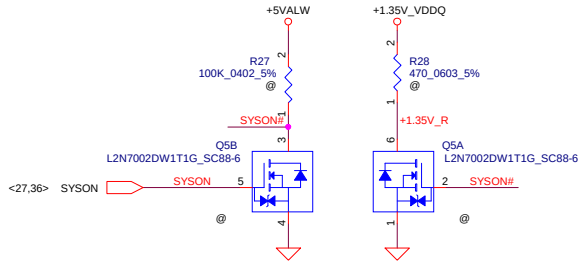
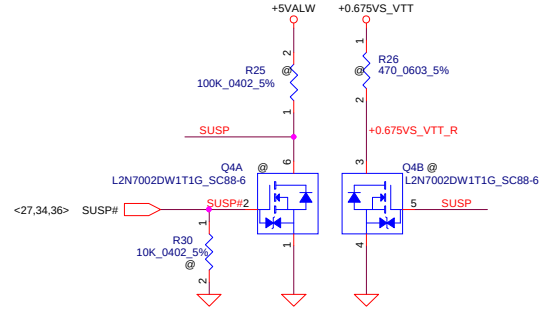
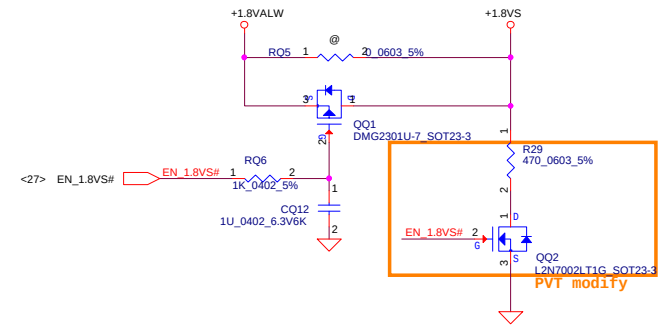


Power-off sequencing schematic

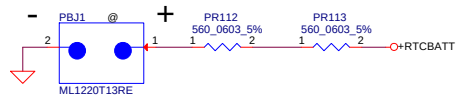
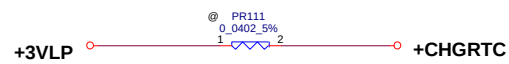
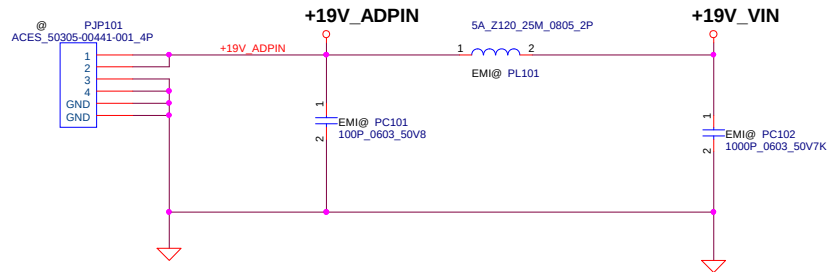
Q2509, Q2510, Q2511
Change to SB000001200
Vgs = 0.49V~1V



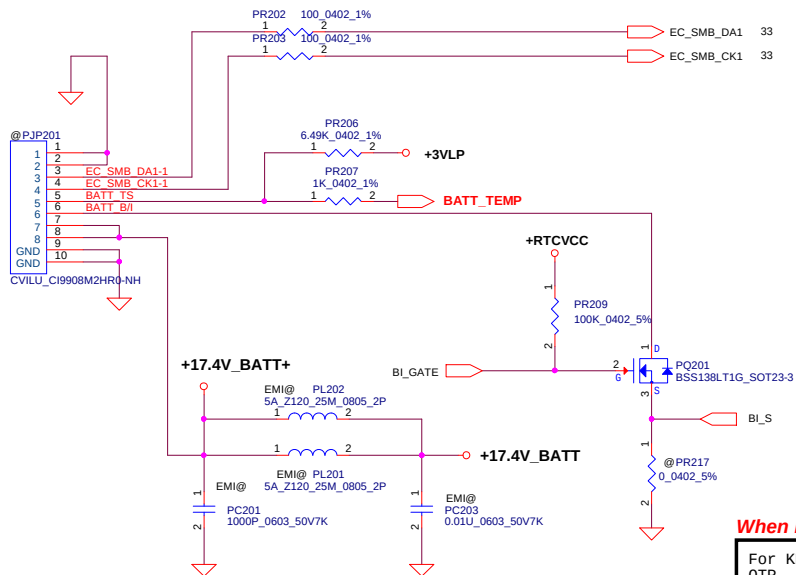
+1.8VALW TO +1.8VS



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				Custom	1A
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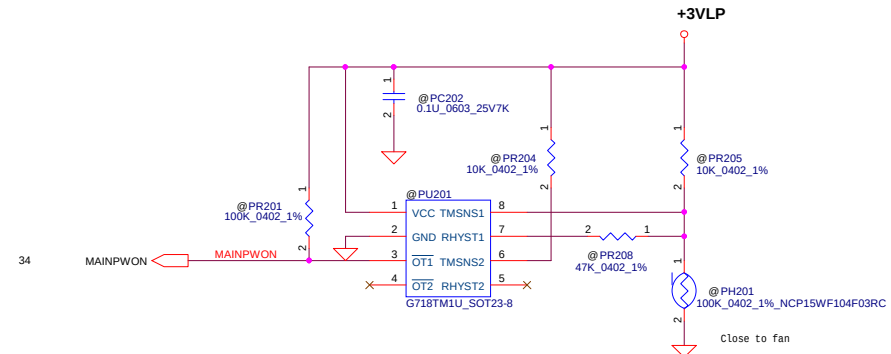


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When PR210=16.9K

For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92'C, 1V	56'C, 2V
PH202 (ohm)	7.3092K	26.11K

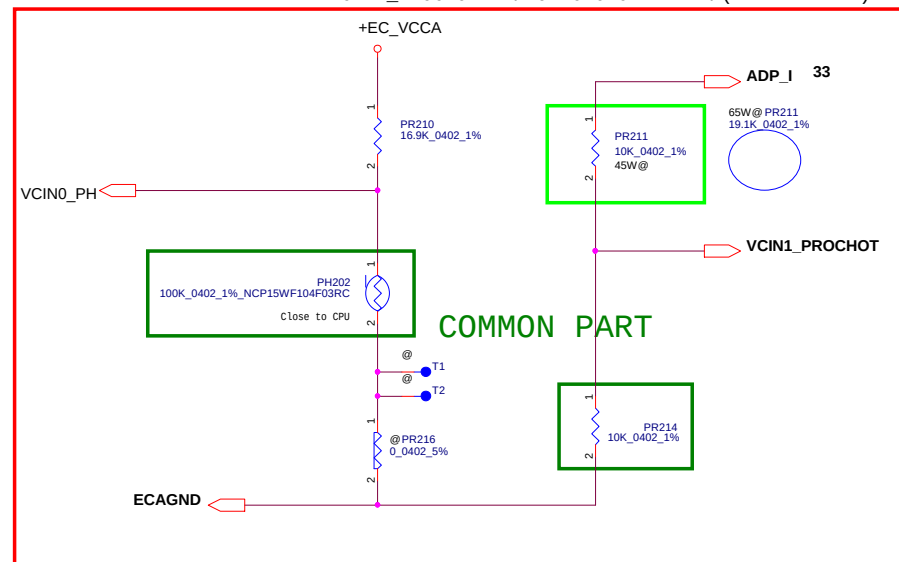
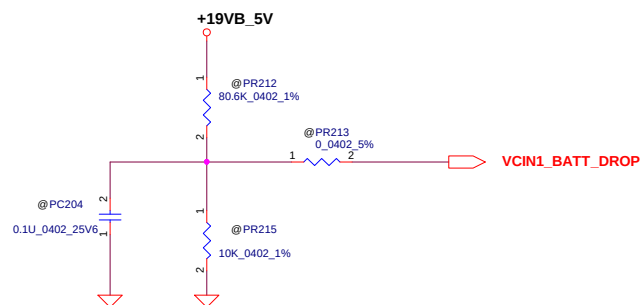


2015/09/30 update

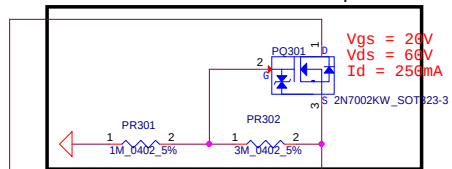
VCIN1_PROCHOT For KB9022 sense 20mΩ	Active	Recovery	PR211
65W	84.5W, 0.61V	84.5W, 0.61V	19.1KΩ SD034191280
45W	58.5W, 0.61V	58.5W, 0.61V	10KΩ SD034100280

130% 130%

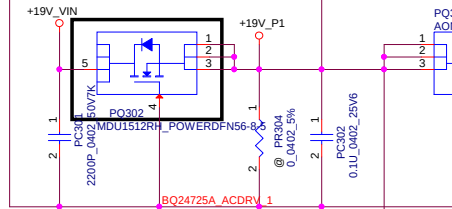
$$VCIN1_PROCHOT = PW / 19 * 20 * 0.02 * PR214 / (PR211 + PR214)$$



Protection for reverse input

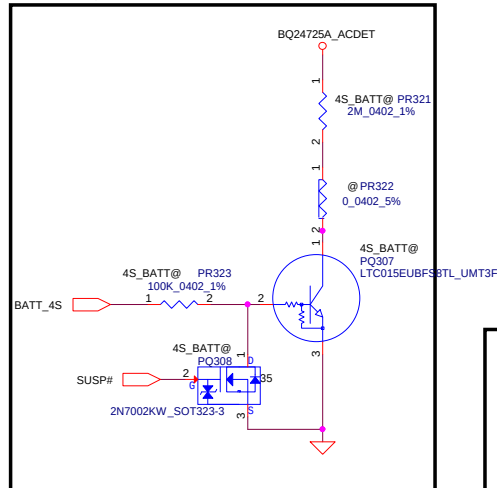


Need check the S0A for inrush



ACFET MDU1512 SB00000SY00
Rds(on): 4.2~5mohm
Vgs=20V
Vds=30V
ID= 24.2A (Ta=70C)

For 4S per cell 4.35V battery



Vin Detector

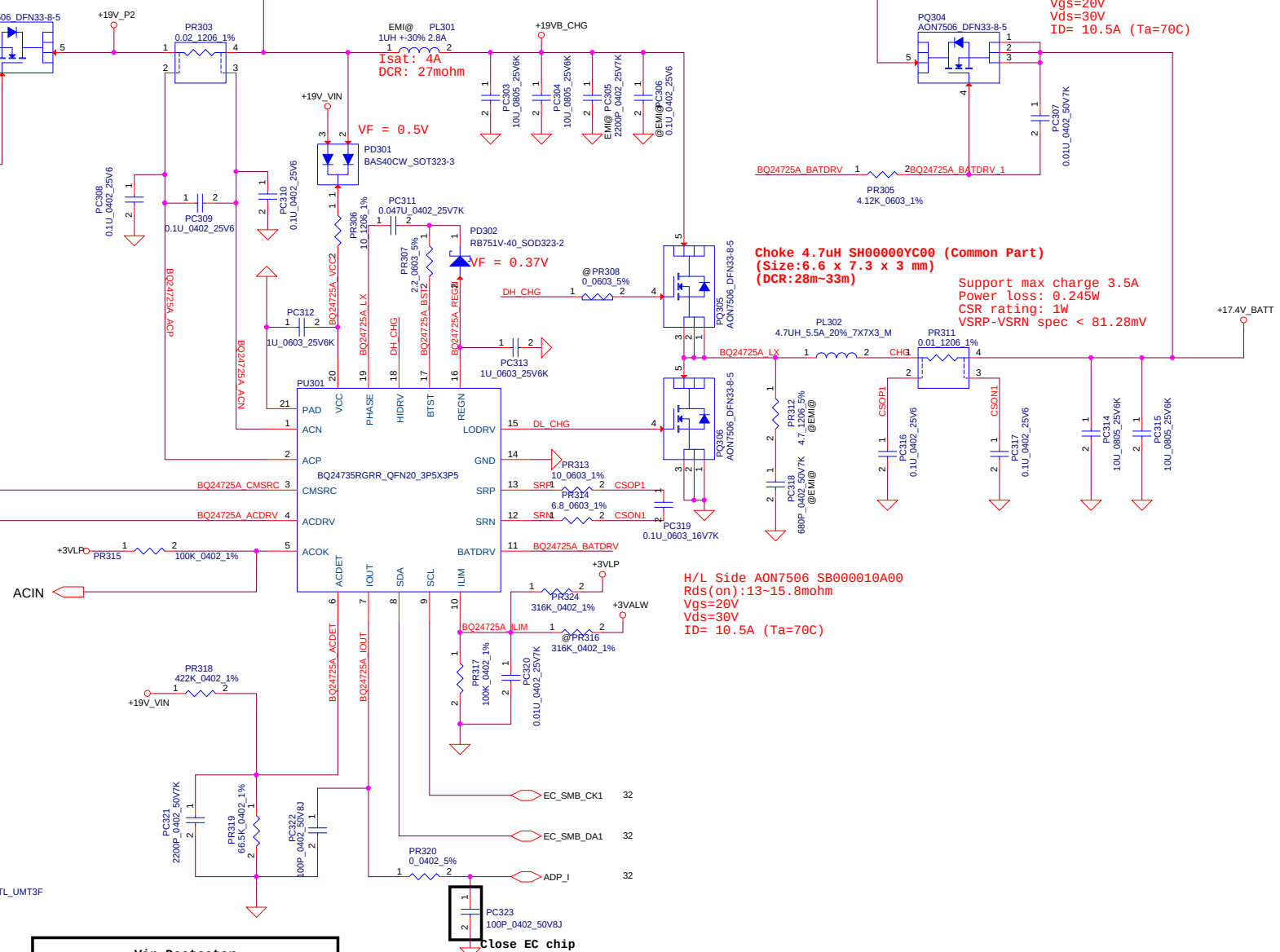
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

$$VILIM = 20 * ILIM * Rsr$$

$$ILIM = 3.3 * 100 / (100 + 316) / 20 / 0.01$$

$$= 3.966 A$$

2014/01/21 update PL301 change
Common part SH00000YG00



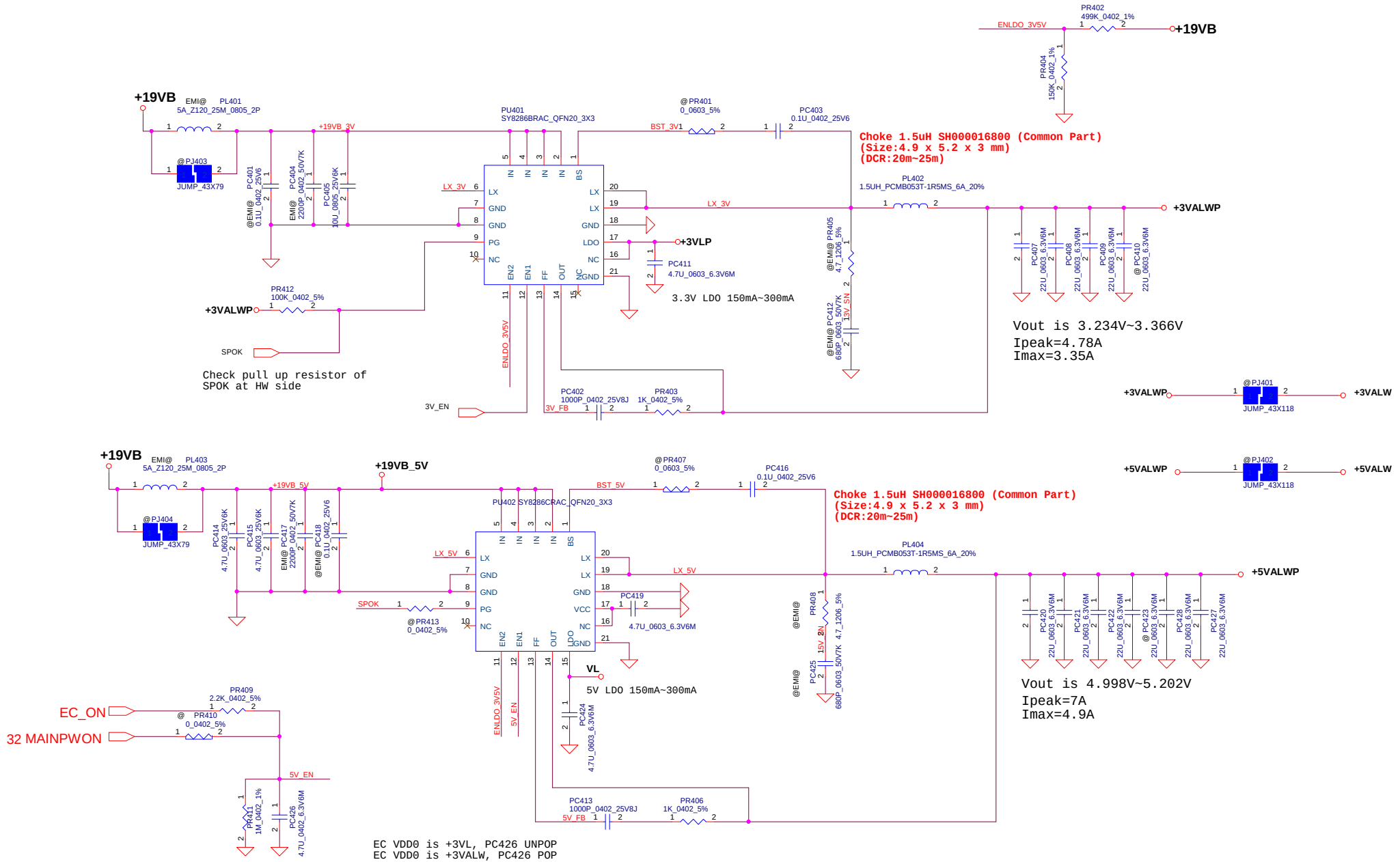
H/L Side AON7506 SB000010A00
Rds(on): 13~15.8mohm
Vgs=20V
Vds=30V
ID= 10.5A (Ta=70C)

BATFET AON7506 SB000010A00
Rds(on): 13~15.8mohm
Vgs=20V
Vds=30V
ID= 10.5A (Ta=70C)

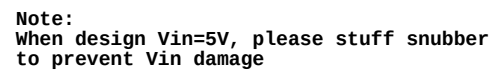
Choke 4.7uH SH00000YC00 (Common Part)
(Size: 6.6 x 7.3 x 3 mm)
(DCR: 28m~33m)

Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VSRP-VSRN spec < 81.28mV

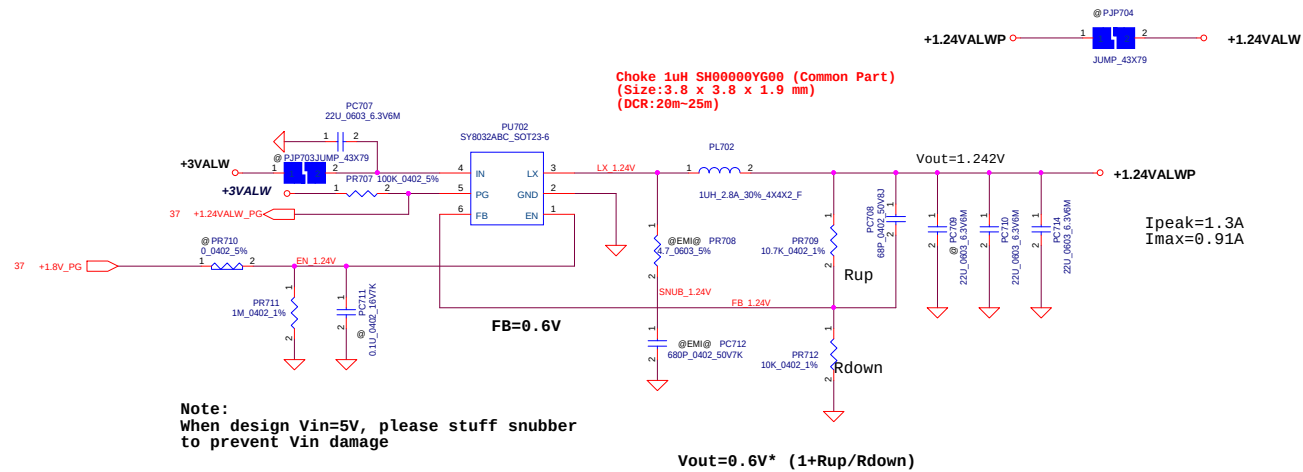
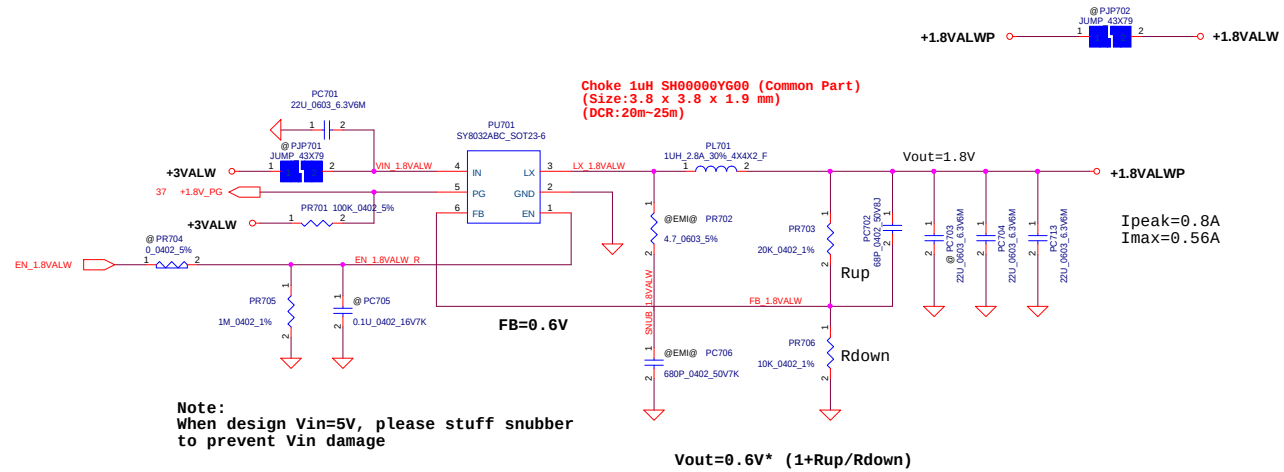
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2013/10/01				Title			
Deciphered Date				2014/05/24				CHARGER			
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Date				Monday, July 25, 2016				Sheet			
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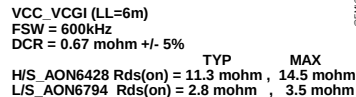
Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2012/07/10		Deciphered Date		2013/07/10		Title					
								3VALW/5VALW					
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$$V_{out} = 0.6V^* (1 + R_{up}/R_{down})$$

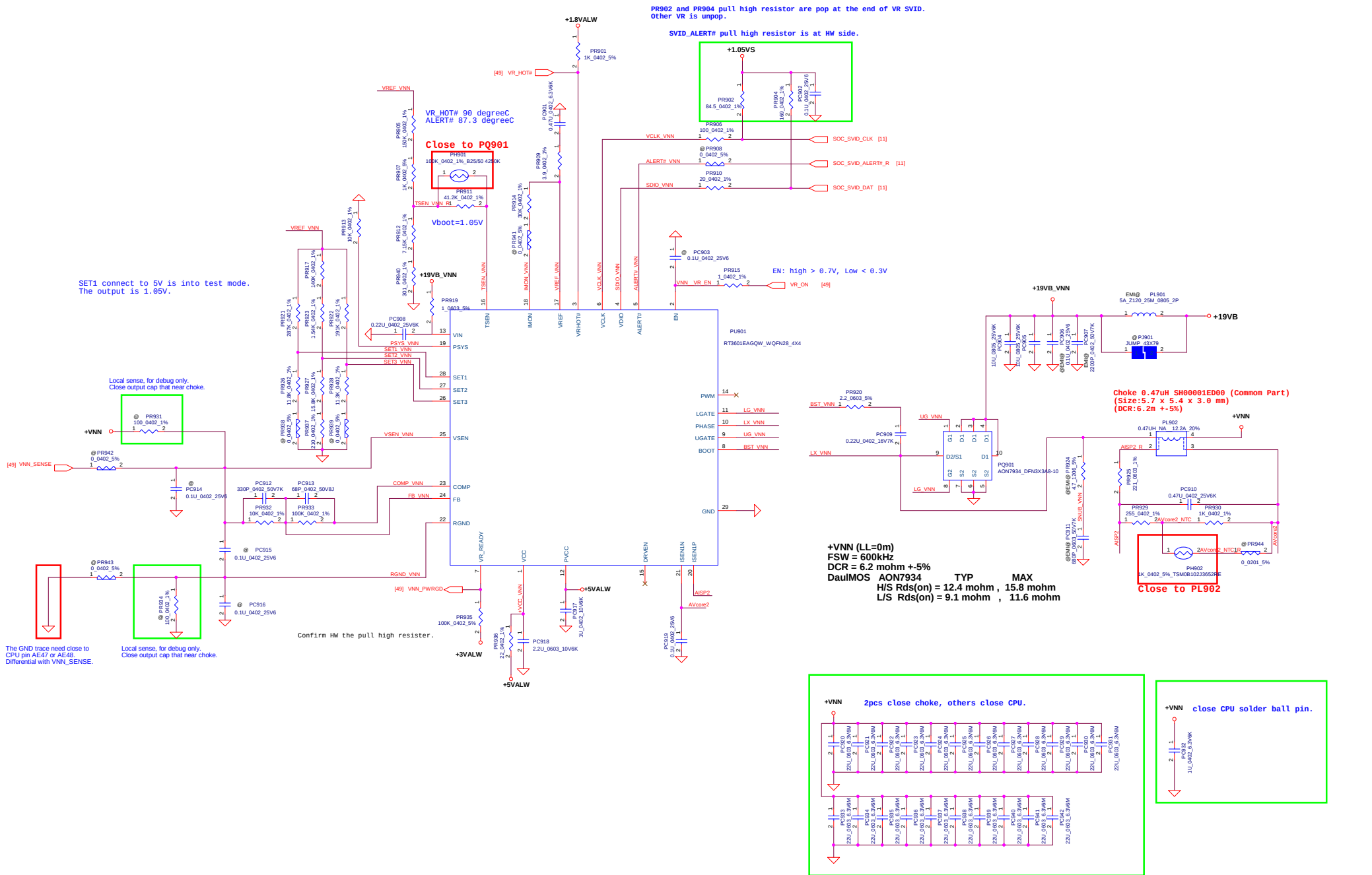
Security Classification	Compal Secret Data					
Issued Date	2011/06/13	Deciphered Date	2012/06/13	Title		
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SET1 connect to 5V is into test mode.
The output is 1.05V.



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Issued Date	2011/06/13	Deciphered Date	2012/06/13	RT3601EA VCCGI
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Issued Date	2011/06/13	Deciphered Date	2012/06/13	RT3601EA VNN	
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Version change list (P.I.R. List)

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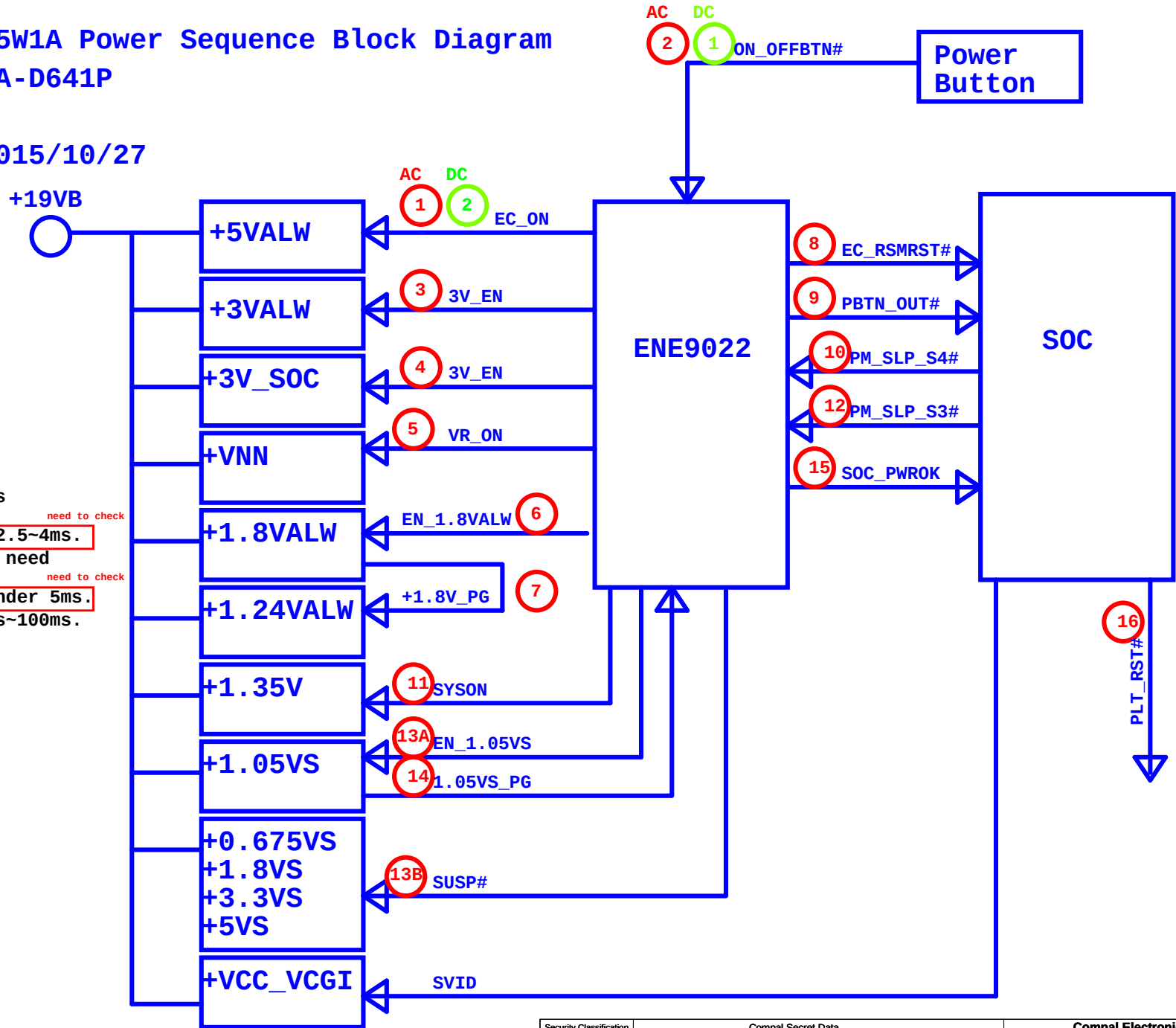
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Design update	Solution Change	01	34	Change the PQ305 from MDV1528 to AON7506. Change the PQ306 from MDV1527 to AON7506.	12/01	EVT
2	Design update	Power Sequence Modify	02	40	Change the PR935.2 from connect +1.8VALW to +3VALW.	12/11	DVT
3	Design update	Solution Change	02	34	Change the PL302 from 10uF to 4.7uF.	12/15	DVT
4	Design update	Solution Change	02	39	Change the PC803, PC804, PC805, PC806 from 4.7uF_0603 *4 to 10uF_0805 *3.	12/15	DVT
5	Design update	Power Sequence Modify	02	38	Change the PR704.2 net name from VNN_PWRGD to EN_1.8VALW. Add the PR707.2 page symbol +1.24VALW_PG.	12/28	DVT
6	Design update	CPU transient test result	02	39	Change the PC814 from 270pF to 470pF. Change the PR833 from 40.2k Ohm to 45.3k Ohm. Change the PR828 from 604 Ohm to 750 Ohm. Change the PR830 from 243 Ohm to 300 Ohm. Change the PR813 from 68.1k Ohm to 57.6k Ohm. Change the PC856 to un-pop.	12/31	DVT
7	Design update	Solution Change	02	39	Delete the jump PJ801.	12/31	DVT
8	Design update	Change the P/N to comment part	02	39	Change the PL802 P/N from SH00001D900 to SH00001EE00.	01/05	DVT
9	Design update	Solution Change	02	35	Change the PR401 from 0 Ohm to R-short. Change the PR407 from 0 Ohm to R-short.	01/28	DVT
10	Design update	Cancel Co-lay	03	34,39	Delete the jump PJ301 and capacitance PC857.	04/25	DVT-2
11	Design update	Solution Change	03	36,37 38,39	Change the PR509, PR601, PR704, PR710, PR815 from 1 Ohm to R-short.	04/25	DVT-2
12	Design update	Solution Change	03	39,40	Change the PR842, PR843, PR807, PR942, PR943, PR908 from 0 Ohm to R-short.	04/28	DVT-2
13	Design update	Solution Change	03	40	Change the PC930, PC931 from 0402 1uF to 0603 22uF.	04/28	DVT-2
14	Design update	Solution Change	03	40	Change the PC924, PC929, PC931, PC933, PC939 from un-pop to pop for PVT test.	04/28	DVT-2
15	Design update	CPU transient test result	03	40	Change the PC913 from 39pF to 68pF. Change the PR933 from 100k Ohm to 60.4k Ohm. Change the PR925 from 191 Ohm to 221 Ohm. Change the PR929 from 232 Ohm to 255 Ohm. Change the PR914 from 21.5k Ohm to 35.7k Ohm. Change the PL902 from 0.68uH to 0.47uH.	05/04	DVT-2
16	Design update	Solution Change	1.0	40	Change the PR942 from R-short to 0 Ohm .	05/17	Pre MP
17	Design update	ME red ink result	1.0	36	Add PC520 、PC521 、PC522 to on-pup, and change PC512 、PC513 、PC515 to un-pop.	06/20	Pre MP
18	Design update	CPU transient test result	1.0	40	Change the PR914 from 35.7k Ohm to 30k Ohm. Change the PR933 from 60.4k Ohm to 100k Ohm.	07/07	Pre MP
19	Design update	Solution Change	1.0	39,40	Change the PR841, PR938, PR939, PR941, PR942 from 0 Ohm to R-short.	07/07	Pre MP

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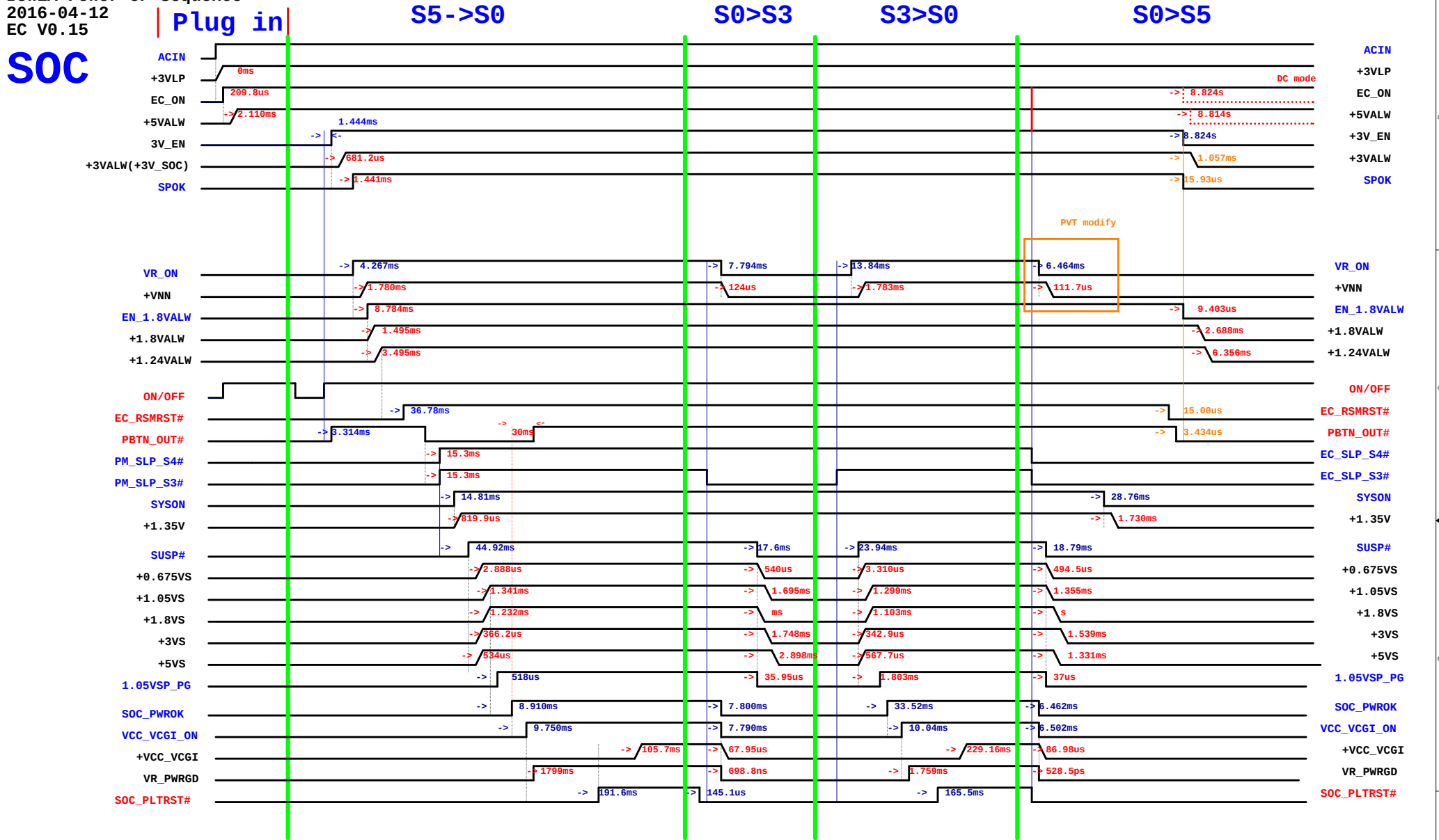
COMPAL CONFIDENTIAL

MODEL NAME: B5W1A Power Sequence Block Diagram
PCB NAME: LA-D641P
REVISION:
DATE: 2015/10/27

Note:
1.7 to 8 need over 10ms
(compal setting 30ms)
2.10 to 11 need under 2.5~4ms.
3.+0.675VS rising time need
under 100us.
4.12 to +1.05VS need under 5ms.
5.14 to 15 need set 5ms~100ms.
(compal setting 20ms)



SOC



Version change list (P.I.R. List)

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for HW

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Design update	Remove SOC side ODD_EN	0.2	P.09	only need reserve EC side ODD_EN	12/28	DVT
2	Design update	UC56 need PU to +3VS	0.2	P.09	Remove RC492 and add RC1162	12/28	DVT
3	Design update	GPI043 need to PD	0.2	P.11	RC408 un-stuff, pop RC433	12/28	DVT
4	Design update	Diode may cause leakage	0.2	P.19	D1 un-stuff, pop U2	12/28	DVT
5	Design update	reserve VNN_PWRGD(Pin117) & +1.24VALW_PG(Pin118)	0.2	P.27	reserve only	12/28	DVT
6	Design update	for power sequence control +1.8VALW	0.2	P.27	add EC pin EN_1.8VALW	12/28	DVT
7	Design update	for EC Board ID	0.2	P.27	change RB506 to 15K	12/28	DVT
8	Design update	Change speaker bead PN by sourcer request.	0.2	P.29	Change LA2,LA3,LA4,LA5 PN from SM01000CC00 to SM01000W00.	12/28	DVT
9	Design update	for 1.8VS discharge	0.2	P.31	add R29,QQ2	12/28	DVT
10	Design update	for 1.8VS soft start	0.2	P.31	pop CQ12	12/28	DVT
11	Design update	Reserve PD and follow EVT SMT BOM	0.2	P.09	Reserve RC492 and pop RC99	12/29	DVT
12	Design update	For cost reivew	0.2	P.21	Remove RY11,RY12,QY2	12/29	DVT
13	Design update	DFX highlight EM5209VF_DFN14_3X2 footprint symbol dosen't release	0.2	P.31	change UQ1 footprint to TPS22966DPUR_SON14_2X3	12/29	DVT
14	Design update	For enlarge H13~15 Screw GND pad to avoid thermal module scrape to PCB	0.2	P.30	change Screw hole from 4.2mm to 3.6mm	01/05	DVT
15	Design update	follow memory down white paper	0.2	P.17	change RD154,RD155 to 1K	01/08	DVT
16	Design update	follow vendor's suggestion	0.2	P.07	change CC7,CC137 to 15pF	01/08	DVT
17	Design update	follow vendor's suggestion	0.2	P.12	change CC15,CC16 to 15pF	01/08	DVT
18	Design update	For part count	0.2	P.20	RX10,RX11 change to R short	01/22	DVT
19	Design update	For cost down experiment	0.2	P.09	change RC524,RC525,RC528,RC529 location for QC2511 & QC2508 cost down	01/22	DVT
20	Design update	For HDMI part count	0.2	P.21	change RY1~5,RY7,RY8,RY10 to 1ohm	01/22	DVT
21	Design update	Follow intel checklist	0.2	P.09	Remove RPC27,add RC342~344 for PM_RST_BTN# need to PU 2.7K	01/22	DVT
22	Design update	For 0 ohm part count	0.2	P.09, P.28	RG8,RC213,RC211 change to R short	01/22	DVT
23	Design update	For common component	0.2	P.07,21 30,31	SB00000DH00 change to SB00000PV00	01/22	DVT
24	Design update	For common component	0.2	P.18	change SE00000G880 to SE076104K80(CD48,50,51,54,58)	01/22	DVT
25	Design update	For intel suggestion	0.2	P09,27	H_THERMTRIP# connect to EC pin 126	01/22	DVT
26	Design update	For I2C cost down	0.2	P.09	unpop QC2508,pop RC528,RC529	01/28	DVT
27	Design update	For DVT phase part count reduce	0.2	P.26	USB3 CMC change to R short (Del LS21~LS22,add RS24~27)	01/28	DVT
28	Design update	For common part	0.2	P.30	change CF1 SE00000MA00 to SE107475K80 (10V change to 6.3V)	01/29	DVT
29	Design update	for H_THERMTRIP# reserve	0.2	P.27	reserve RB490	01/29	DVT
30	Design update	For correct to ABO material	0.2	P.12	change 105_0402_1% from SD00000FY8L to SD00000FY00	01/29	DVT
31	Design update	For DVT phase	0.2	P.05	change CPU PN for ES2 QKKW(SA00009S800),QKKX@(SA00009S900),QKKY@(SA00009SA00)	02/02	DVT
32	Design update	For Intel 2016 WW04 Sightings Report update(560733)	0.2	P.10	Change RC79 from 1K_0402_1% to 680_0402_1%	02/02	DVT

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				Custom	1.A
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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
33	Design update	For different Fan table	0.2	P.27	Add 17" EC board ID	02/02	DVT
34	Design update	for 1.8VS discharge	0.3	P.31	Q02 change to Q4B, and stuff Q4 & R25, un stuff Q02	04/12	DVT2
35	Design update	verify +3V_SOC for cost down	0.3	P.31	Un stuff RQ3 as DVT memo	04/12	DVT2
36	Design update	For intel request	0.3	P.27	change H_THERMTRIP# to EC pin 101	04/12	DVT2
37	Design update	follow CRB	0.3	P.9	SOC_PLTRST# reserve PU +3VS change to +3V_SOC	04/12	DVT2
38	Design update	for BOM structure option	0.3	P.16	change memory down BOM structure to MD04/12	04/12	DVT2
39	Design update	for part count reduce.	0.3	P.21	HDMI RY1~RY5, RY7~RY8, RY10 change to R short	04/25	DVT2
40	Design update	Intel HDA issue, Fix on QS sample.	0.3	P.10	RC483&RC779 un-stuff	04/25	DVT2
41	Design update	Follow APL PDG v1.2 suggestion	0.3	P.7	Del RPC28, add RC522, RC524, RC525, RC516	04/25	DVT2
42	Design update	Follow APL Checklist v1.2 suggestion	0.3	P.24	un stuff RC383, and BIOS internal PU	04/25	DVT2
43	Design update	Follow APL Checklist v1.2 suggestion	0.3	P.21	un stuff RY14, and BIOS internal PU	04/25	DVT2
44	Design update	For 0 ohm part count reduce	0.3	P9 10 22 23	RL1, RC99, RC528, RC529, RC1052, RG2	04/25	DVT2
45	Design update	For part count reduce	0.3	P.31	RQ1, RQ2 change from 10hm to RShort	04/25	DVT2
46	Design update	for option SM Bus	0.3	P.18	reserve RD168 to PU +3VALW	04/26	DVT2
47	Design update	for part count reduce	0.3	P.18	RD165 change to 0ohm	04/26	DVT2
48	Design update	intel checklist v1.2 update	0.3	P.9	RC344 change from 2.7K to 10K	04/26	DVT2
49	Design update	Update DVT2 Board ID	0.3	P.27	RB506 change to 20K(15") and 200K(17")	04/26	DVT2
50	Design update	Connect PMC_SUSPWDNACK from SOC to EC	0.3	P.27	Stuff RB489	05/12	PVT
51	Design update	Update circuit	0.3	P.5	Update QS CPU in circuit	05/24	PVT
52	Design update	add +1.8VS discharge circuit	0.3	P.31	stuff R29 & Q02	05/24	PVT
53	Design update	Update Pre MP Board ID	1.0	P.27	change EC board ID 15" to 27K, 17" to 240K	06/27	PreMP
54	Design update	PDG 1.5 update	1.0	P.21	RY17&RY18 un stuff	06/27	PreMP
55	Design update	RC517, RC519, RC480, RC481, RC476, RC145, RC146, RD165, RL13, RB482 chagne to RS	1.0	P.7, 13, 14 18, 22, 24	for 0 ohm part count reduce	06/27	PreMP
56	Design update	For ME EN	1.0	P.10	RC1052 change to 0ohm	06/27	PreMP
57	Design update	For part count reduce	1.0	P.31	UQ2 un stuff	06/27	PreMP
58	Design update	For intel PDG update	1.0	P.12	swap JCM0S1 & JCM0S2, SOC_SRTCRST# & SOC_RTCTEST#	07/04	PreMP
59	Design update	For part count reduce	1.0	P.13	RC476 & RC481 change to 0_0603	07/04	PreMP
60	Design update	For +1.35V power	1.0	P.14	add RC147 for +1.35V R short	07/05	PreMP
61	Design update	For 0 ohm part count reduce	1.0	P.29	change RA24, RA27 to R short	07/05	PreMP
62	Design update	For part count reduce	1.0	P.12	RC340 & RC402 change to @CMC@	07/05	PreMP
63	Design update	For MP BOM	1.A	P.05	Update B0 & B1 CPU	07/22	PreMP
64	Design update	For intel spec update	1.A	P.12	un stuff RC273, RC266, RC268	07/22	PreMP
65	Design update	For intel spec update	1.A	P.12	change RC245, RC93 to 57.6K stuff RC251	07/22	PreMP
66	Design update	For PCB update	1.A	P.27	Add 1A board ID	07/22	PreMP
67	Design update	For Acer request	1.A	P.11	Add Micron on board RAM	07/22	PreMP
68	Design update	For intel signting	1.A	P.9	Un stuff RC343	07/22	PreMP

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