

COMPAL CONFIDENTIAL

MODEL NAME : CDP70
PCB NO : LA-E141P
BOM P/N :
GPIO MAP: Dell GPIO map EC16 062416 Compal Only

Breckenridge 14 UMA

Kabylake H

2016-07-01

REV : 0.2 (X01)

- @ : Nopop Component
- EMI@ : EMI Component
- @EMI@ : EMI Nopop Component
- ESD@ : ESD Component
- @ESD@ : ESD Nopop Component
- RF@ : RF Component
- @RF@ : RF Nopop Component
- XDP@ : XDP Component
- CONN@ : Connector Component

MB PCB	
Part Number	Description
DAB0001R000	PCB 1SC LA-E141P REV0 MB UMA 1

Layout Dell logo

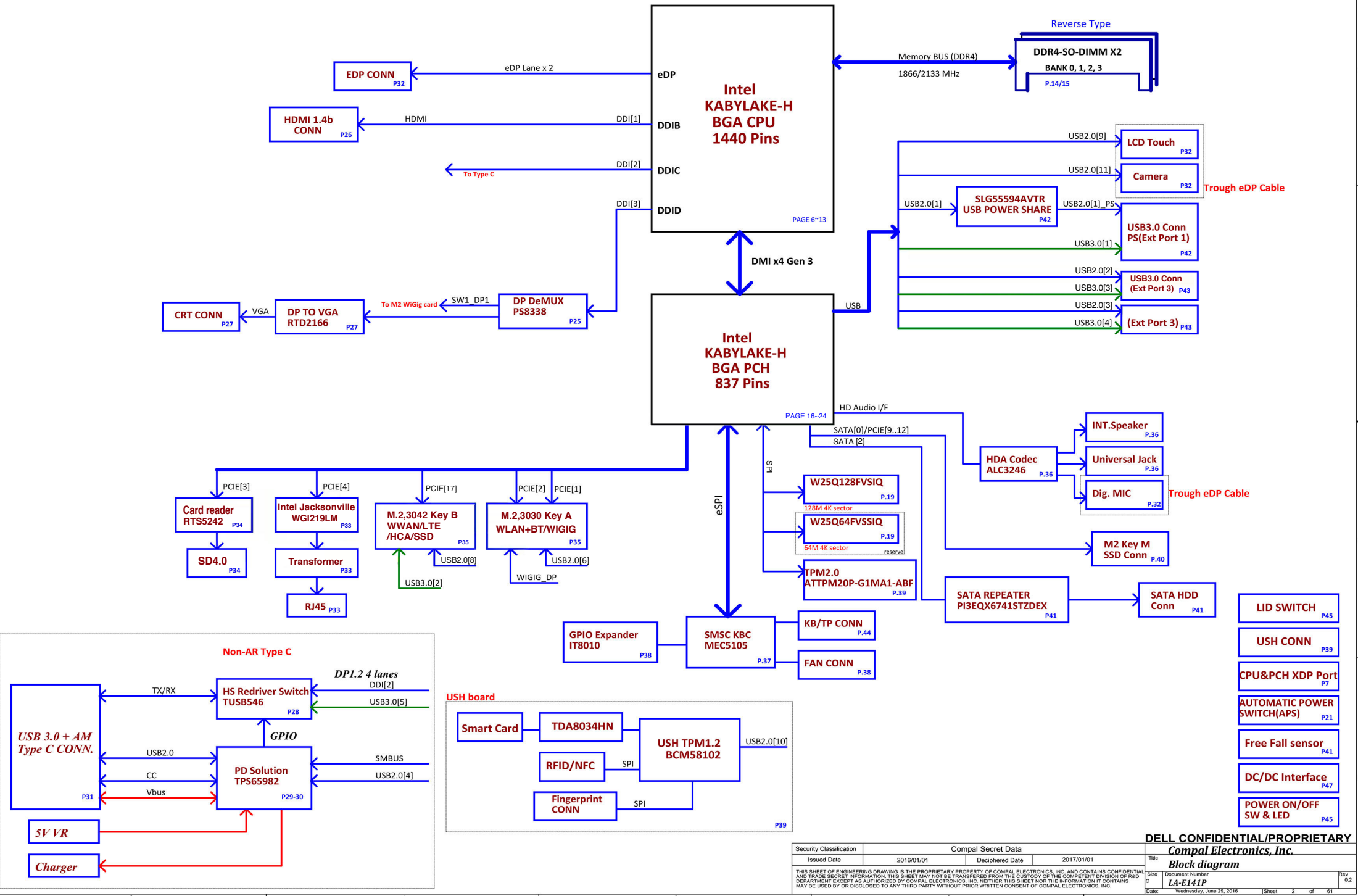


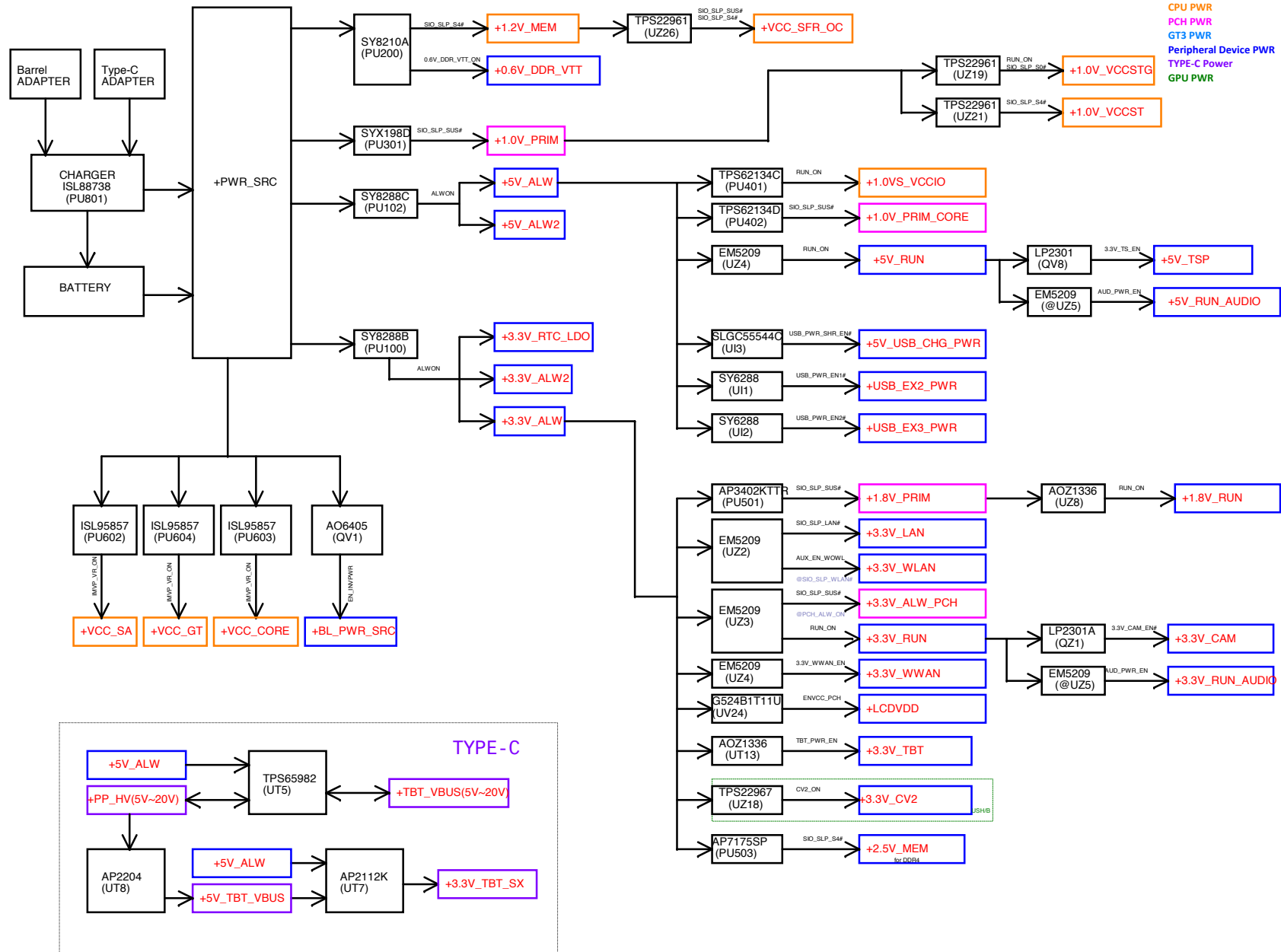
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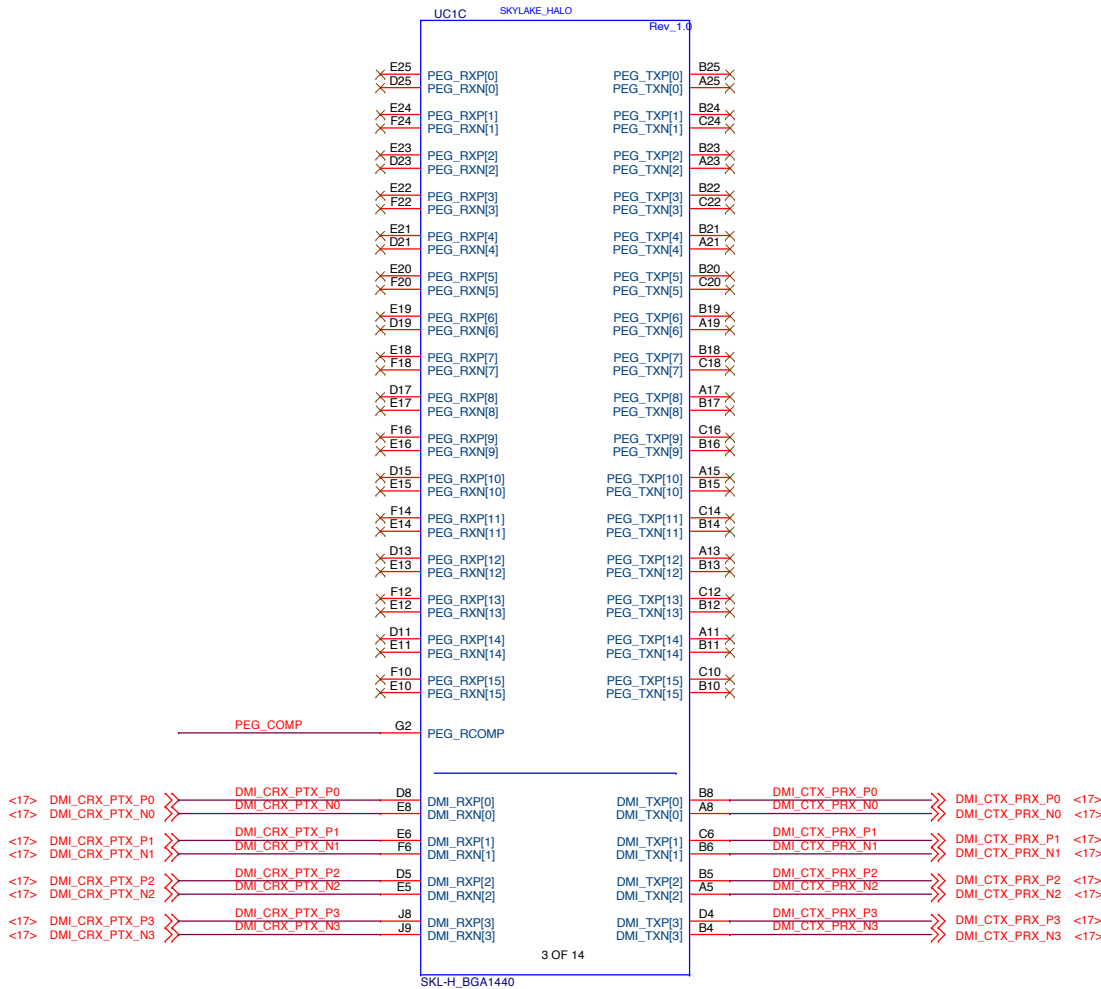
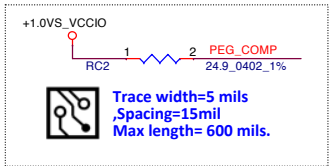
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Issued Date		2016/01/01		2017/01/01	
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Title		Compal Electronics, Inc.		Cover Sheet	
Size		Document Number		Rev	
A		LA-E141P		0.2	
Date:		Friday, July 01, 2016		Sheet 1 of 61	

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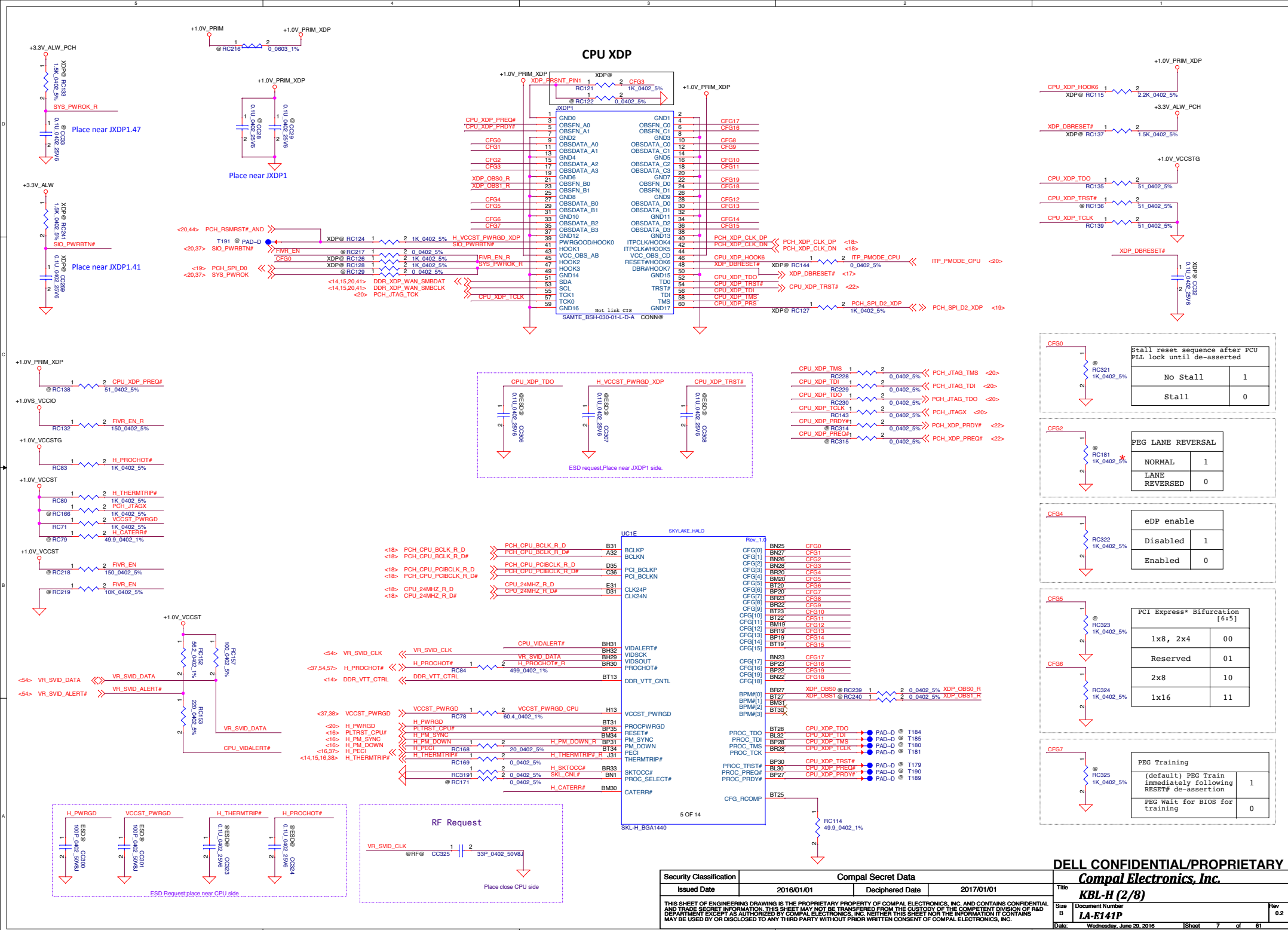
Breckenridge 14 UMA non-TBT Block Diagram







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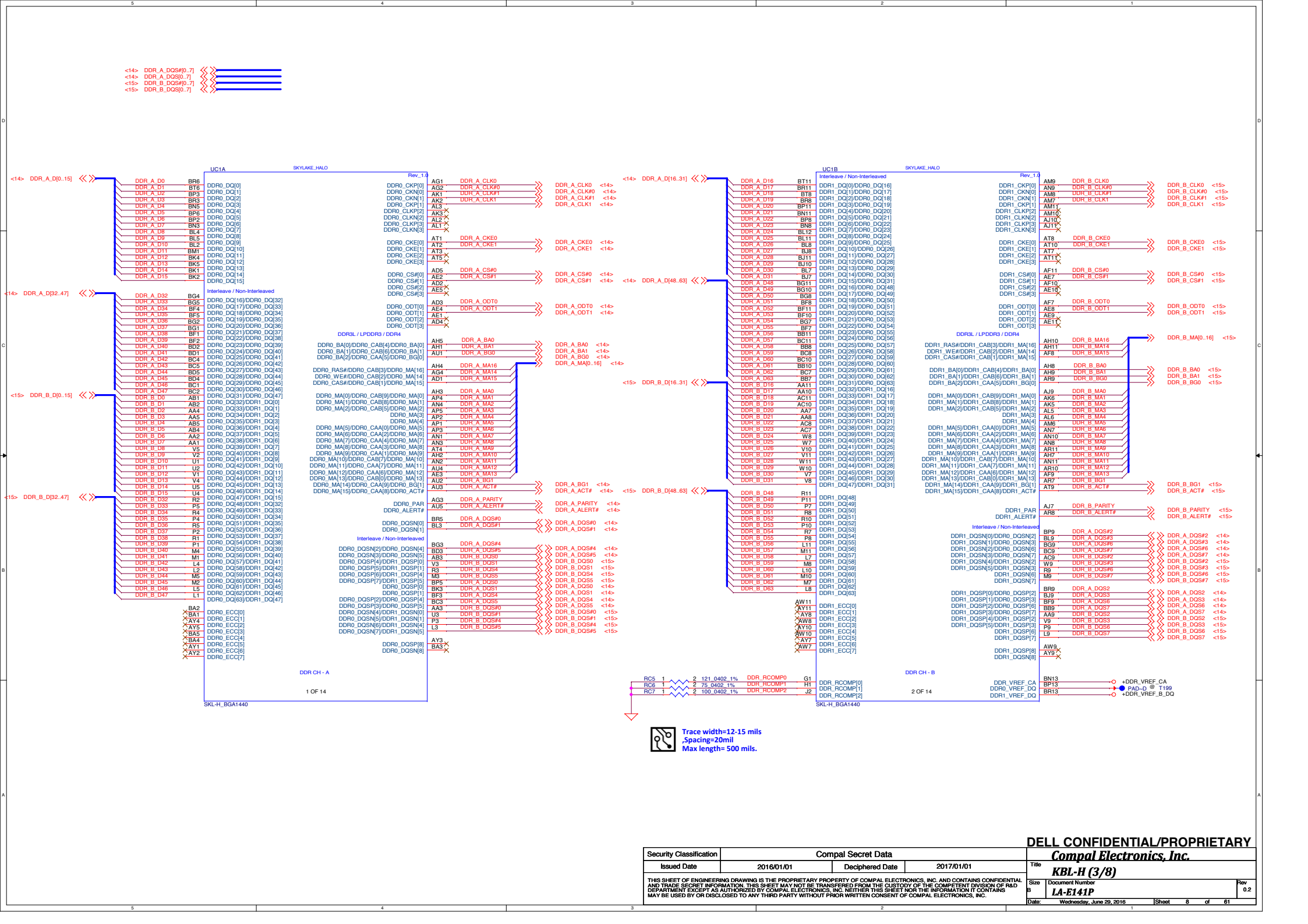


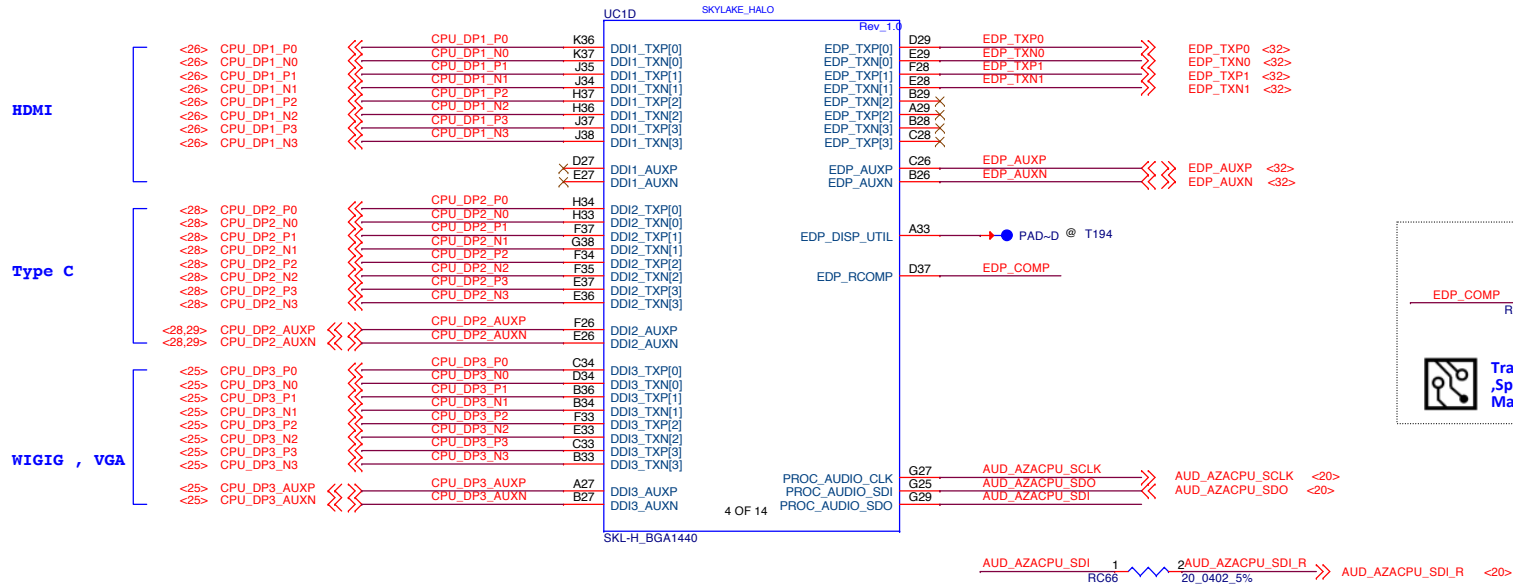
CPU XDP

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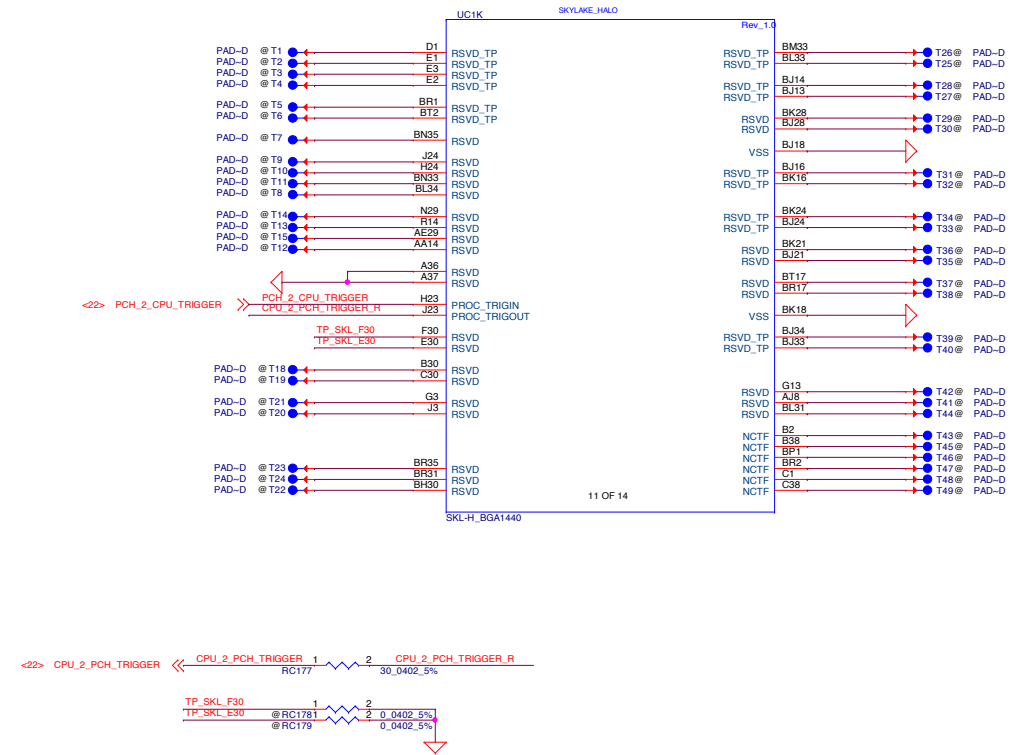
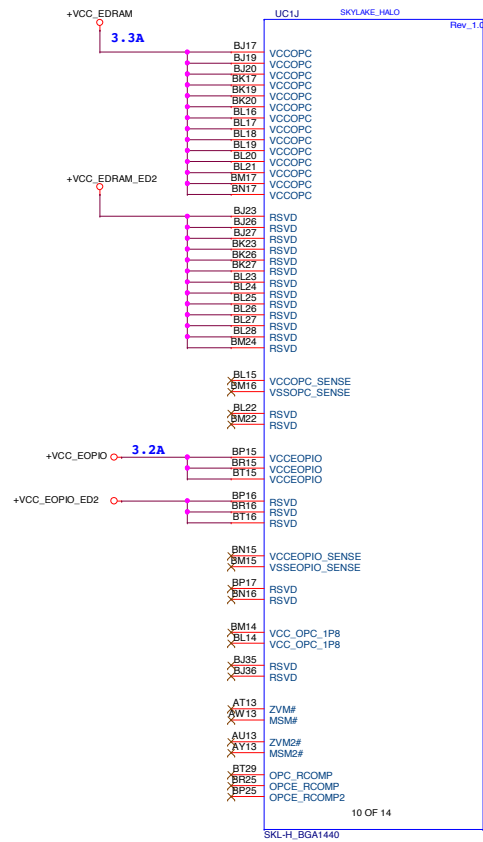
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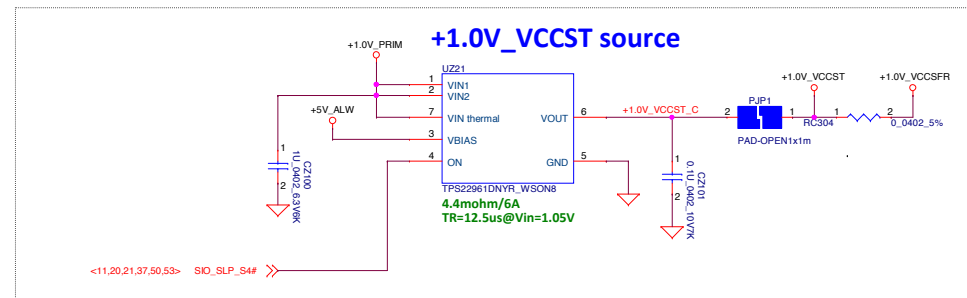
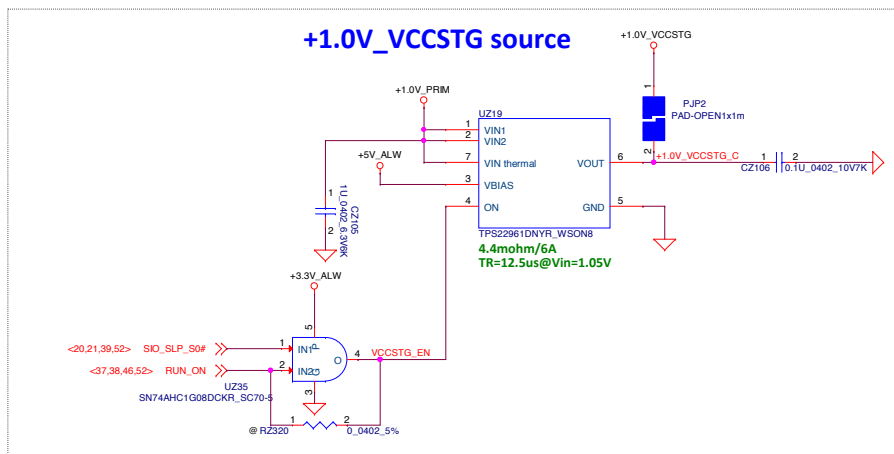
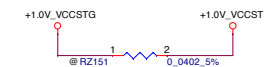
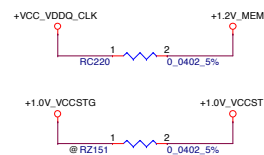
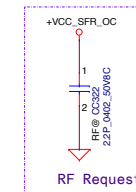
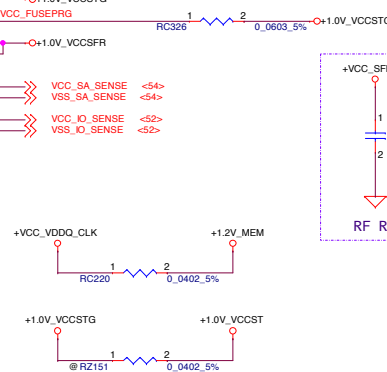
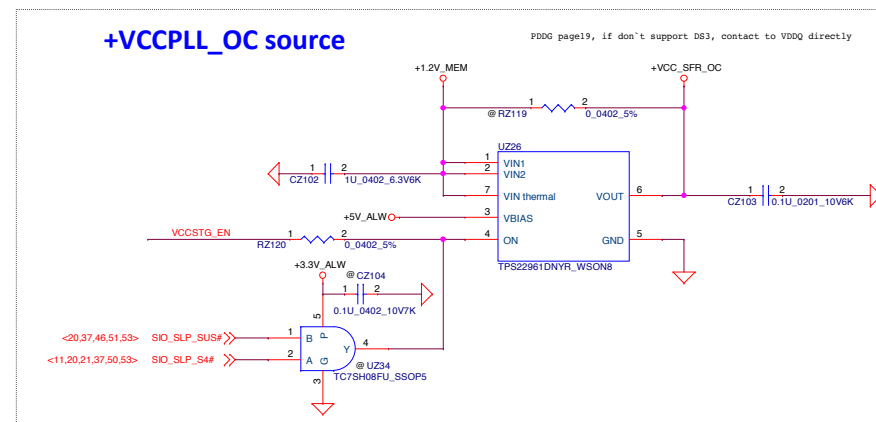
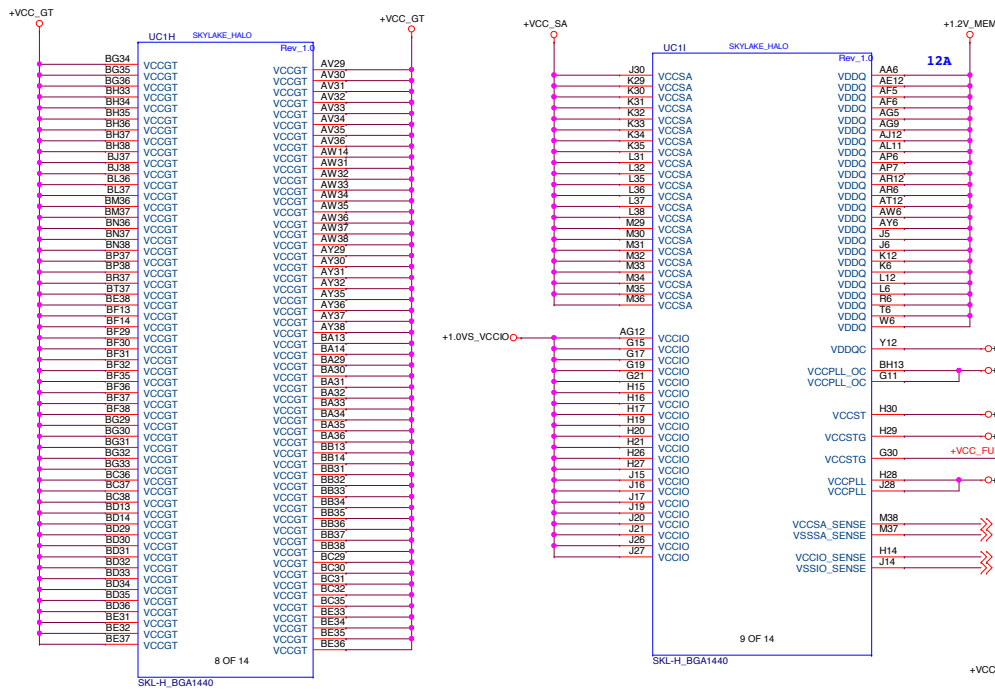


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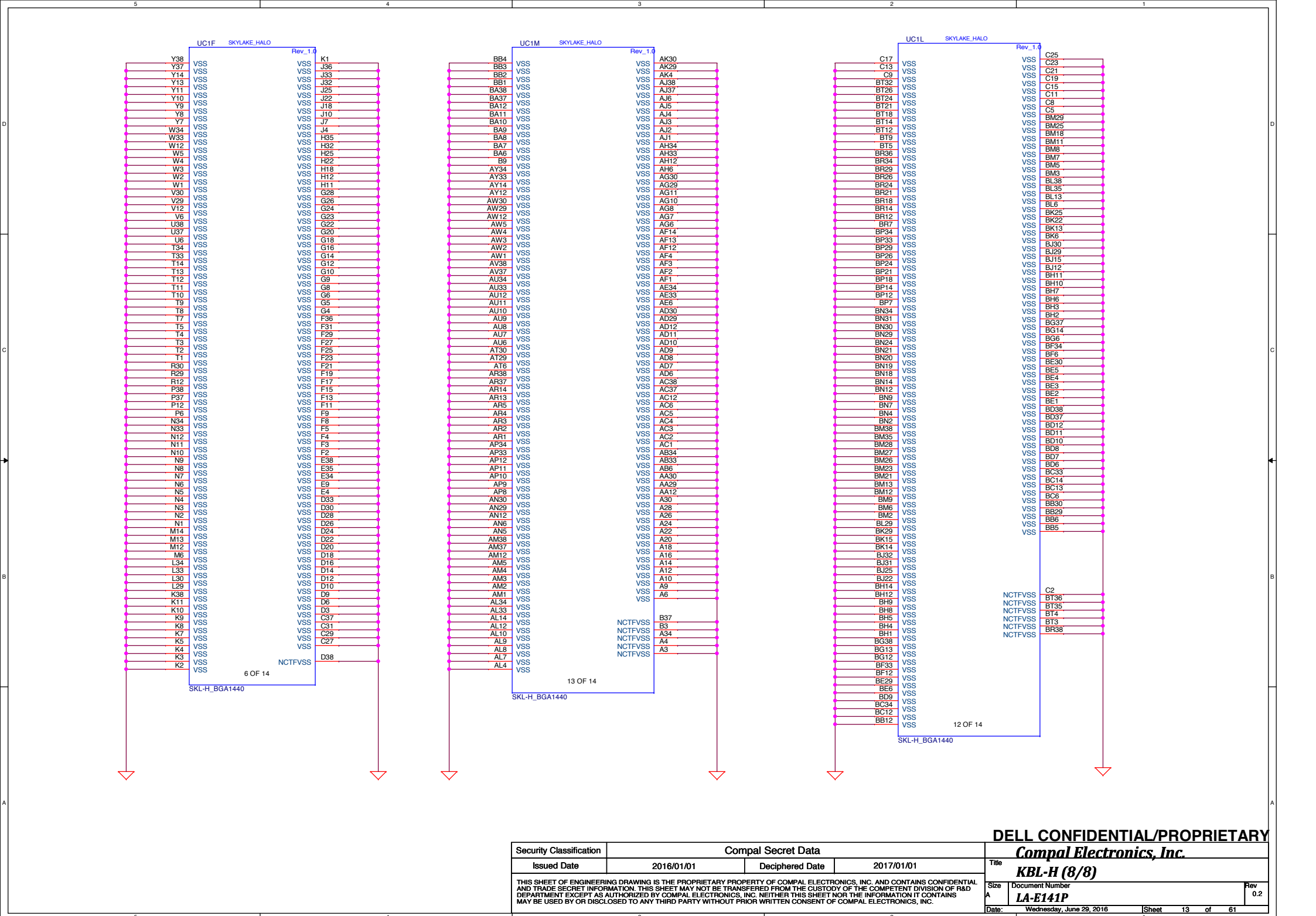


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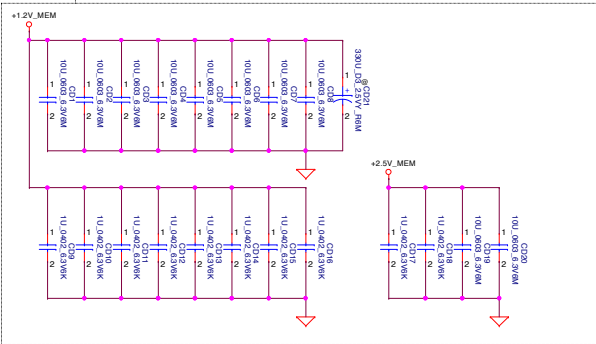


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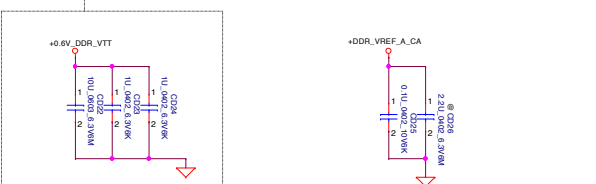


 DDR_A_DQS[0:7]
 DDR_A_DQ[0:7]
 DDR_A_DQ[15:15]
 DDR_A_DQ[16:31]
 DDR_A_DQ[32:47]
 DDR_A_DQ[48:63]
 DDR_A_MA[0:16]

Layout Note:
Place near JDIMM1



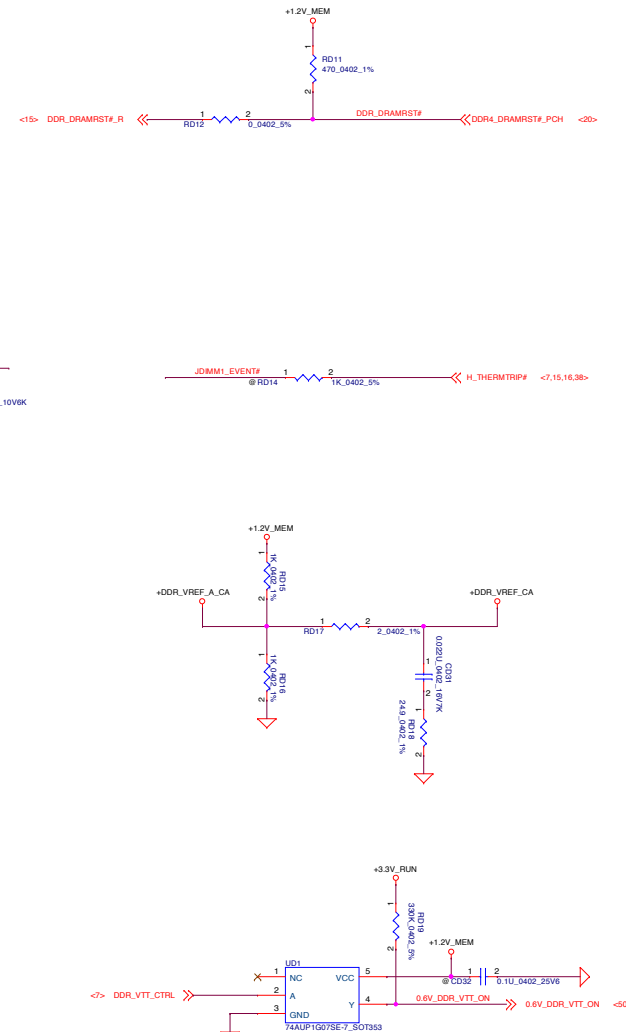
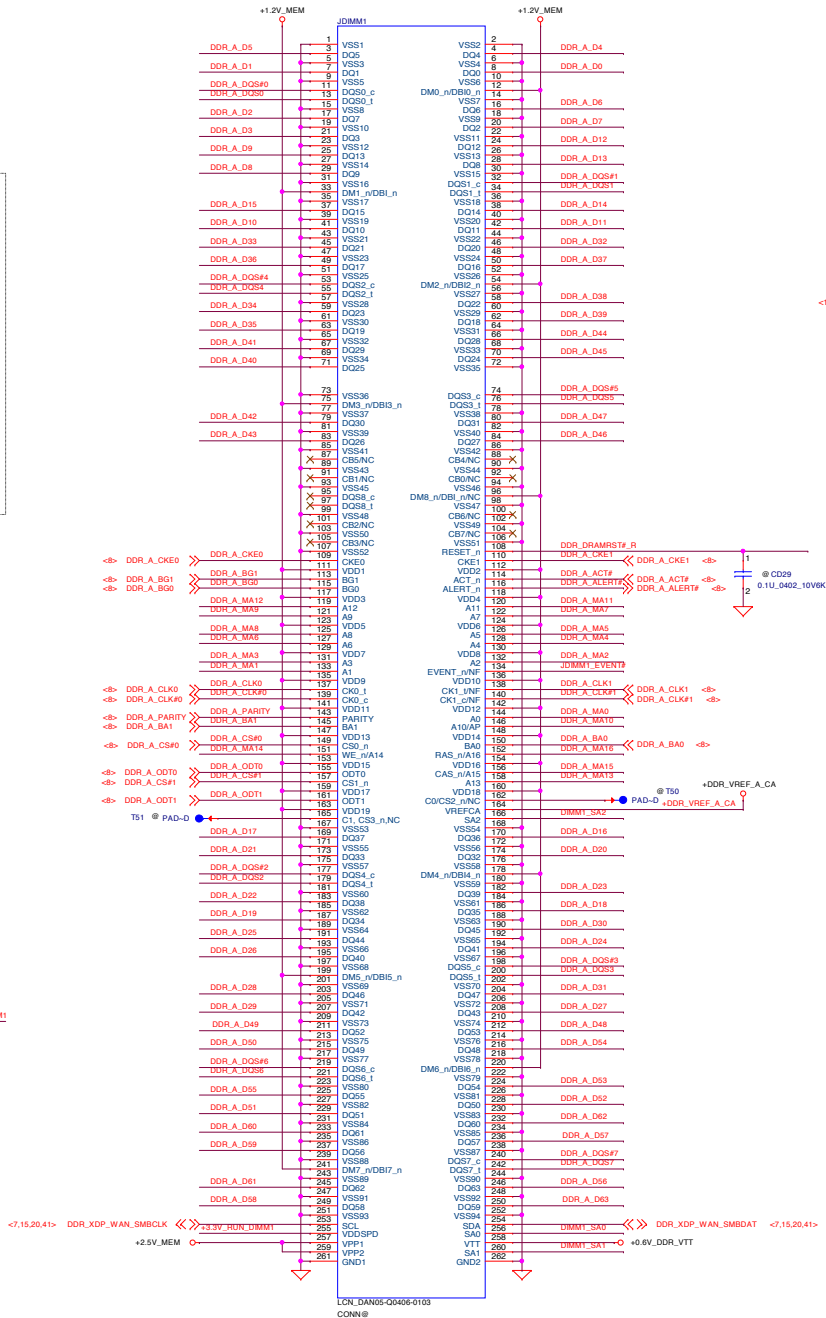
Layout Note:
Place near JDIMM1.258



DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

Byte[0]	DQ[7:0]	DQS/DQS#[0]
Byte[1]	DQ[15:8]	DQS/DQS#[1]
Byte[2]	DQ[23:16]	DQS/DQS#[2]
Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
Byte[5]	DQ[47:40]	DQS/DQS#[5]
Byte[6]	DQ[55:48]	DQS/DQS#[6]
Byte[7]	DQ[63:56]	DQS/DQS#[7]



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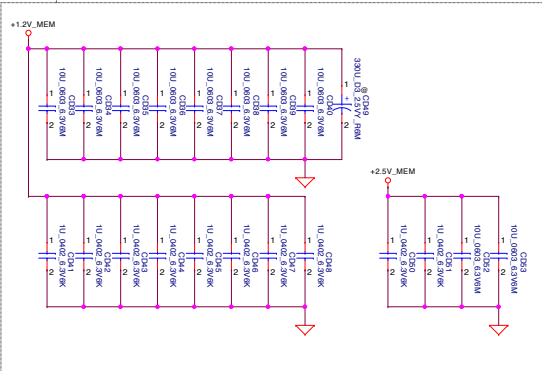
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DDR4-SODIMM SLOT1

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DDR_B_DQS#0..7
DDR_B_DQS#0..7
DDR_B_DQ15..31
DDR_B_DQ15..31
DDR_B_DQ32..47
DDR_B_DQ32..47
DDR_B_DQ48..63
DDR_B_DQ48..63
DDR_B_MA0..16

Layout Note:
Place near J1MM2

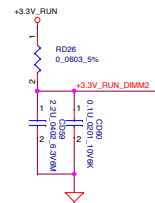
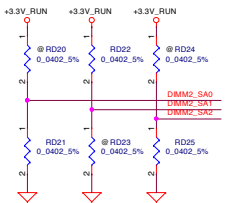


Layout Note:
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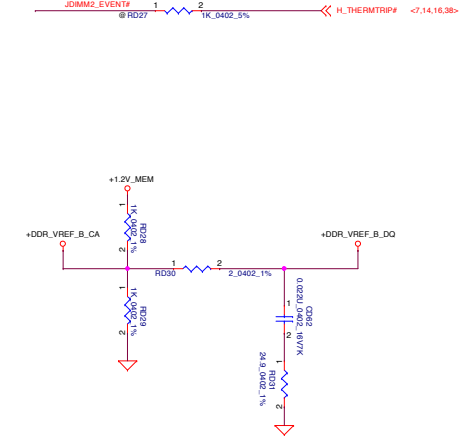


DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



Byte[0]	DQ[7:0]	DQS/DQS#0]
Byte[1]	DQ[15:8]	DQS/DQS#1]
Byte[2]	DQ[23:16]	DQS/DQS#2]
Byte[3]	DQ[31:24]	DQS/DQS#3]
Byte[4]	DQ[39:32]	DQS/DQS#4]
Byte[5]	DQ[47:40]	DQS/DQS#5]
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Byte[7]	DQ[63:56]	DQS/DQS#7]



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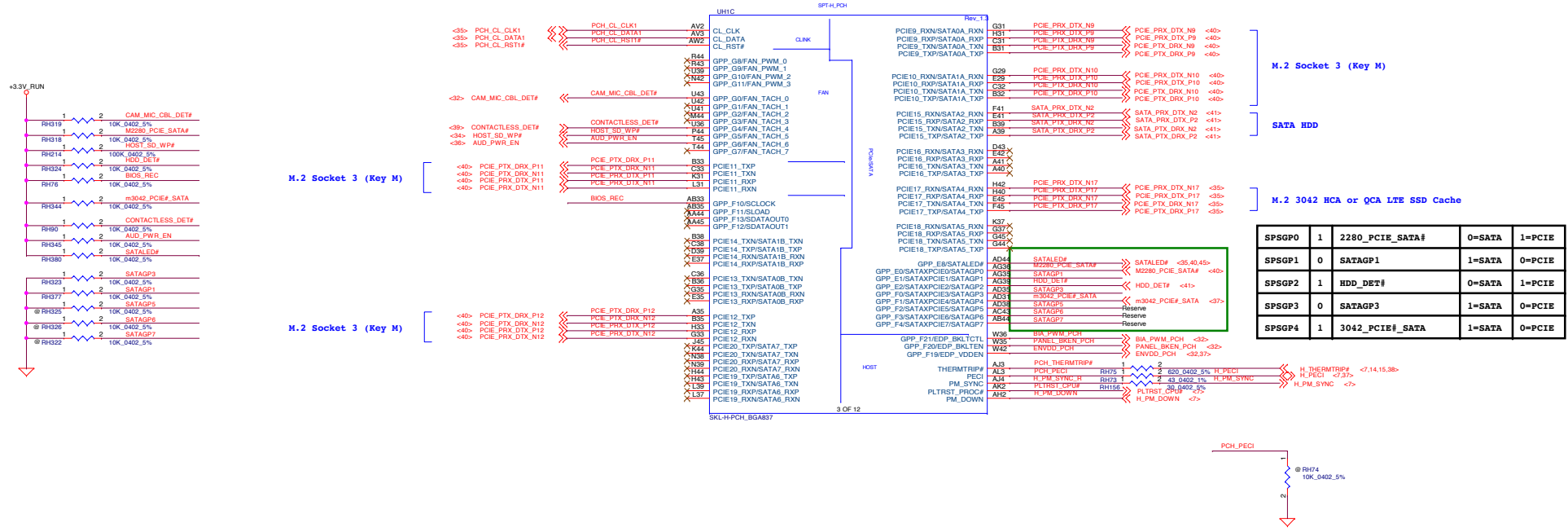
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DDR4-SODIMM SLOT2

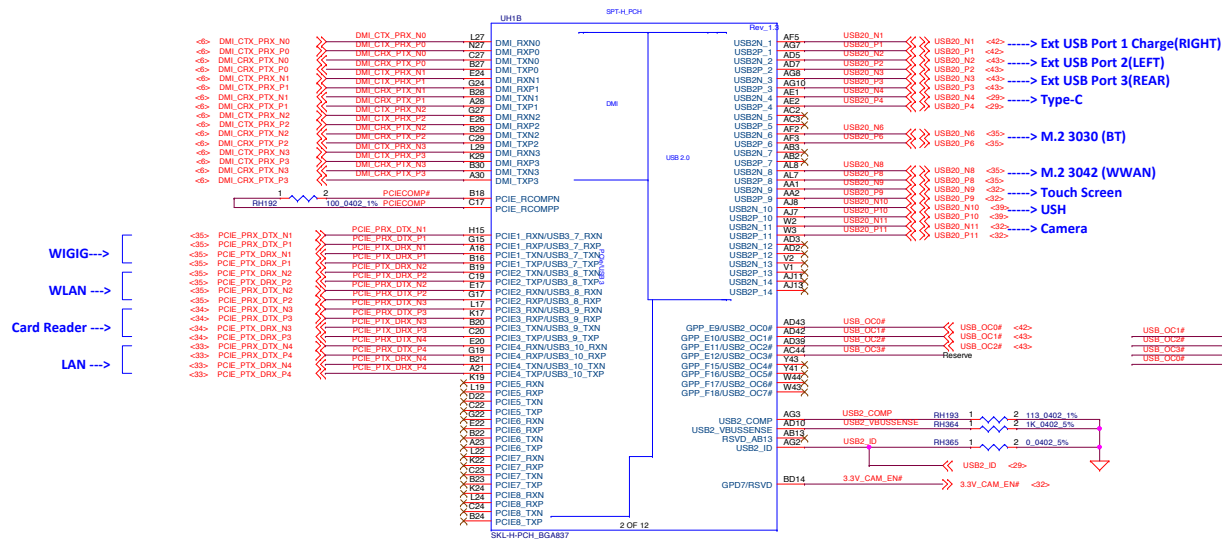
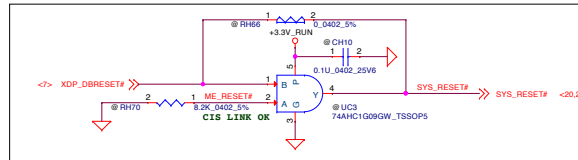
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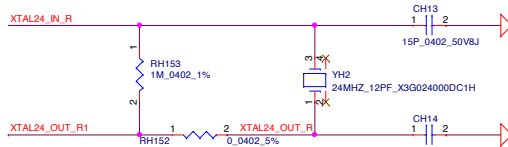
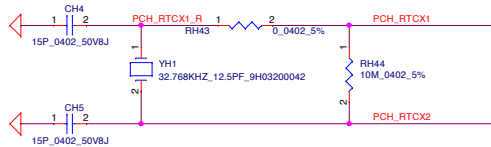
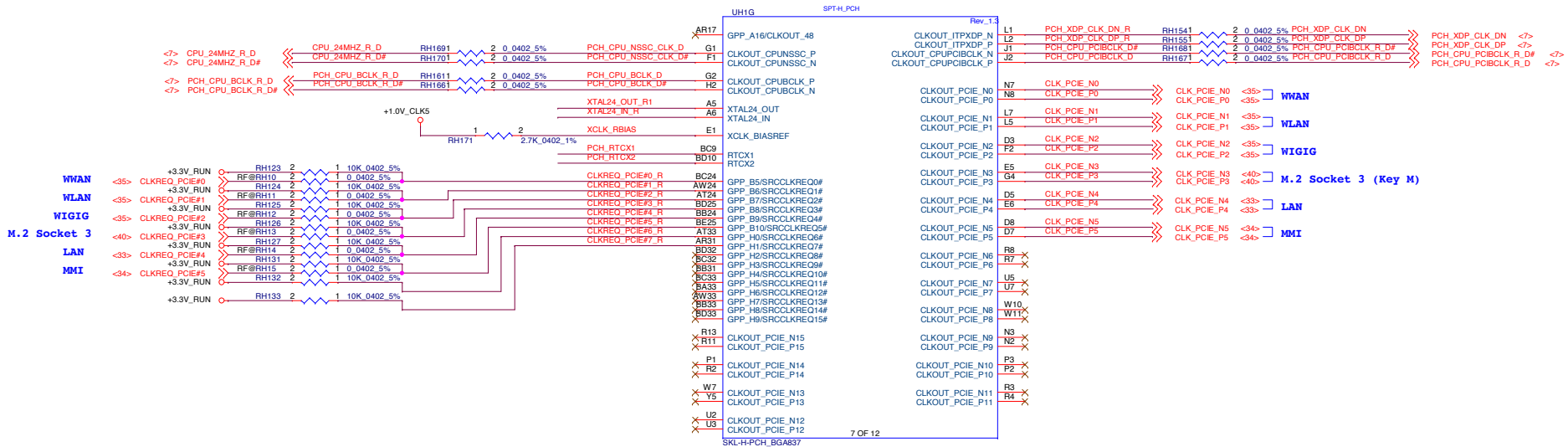
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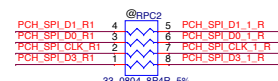
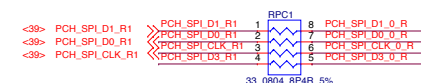
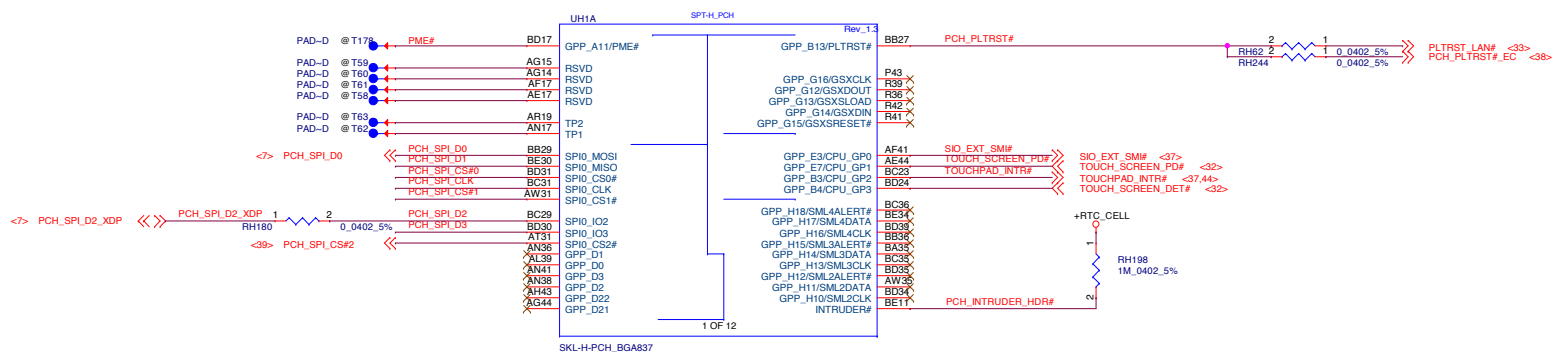
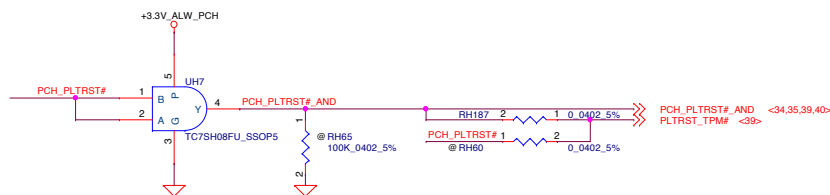
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SPSGP0	1	2280_PCIE_SATA#	0=SATA	1=PCIE
SPSGP1	0	SATAGP1	1=SATA	0=PCIE
SPSGP2	1	HDD_DET#	0=SATA	1=PCIE
SPSGP3	0	SATAGP3	1=SATA	0=PCIE
SPSGP4	1	3042_PCIE#_SATA	1=SATA	0=PCIE

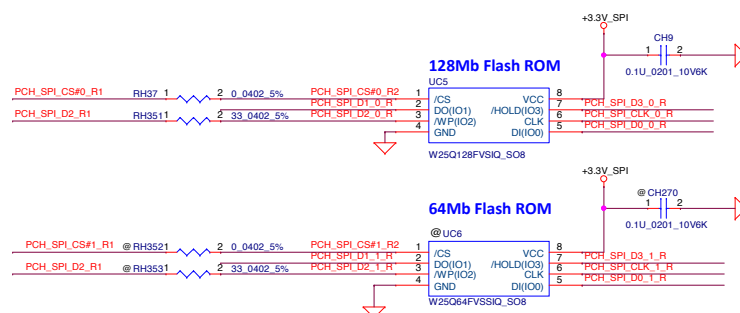




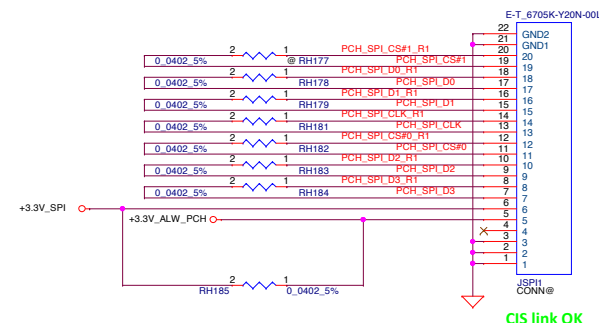
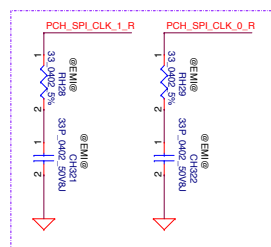


Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with FS and SKL S/H platforms with pre-FS1/FS1 samples.

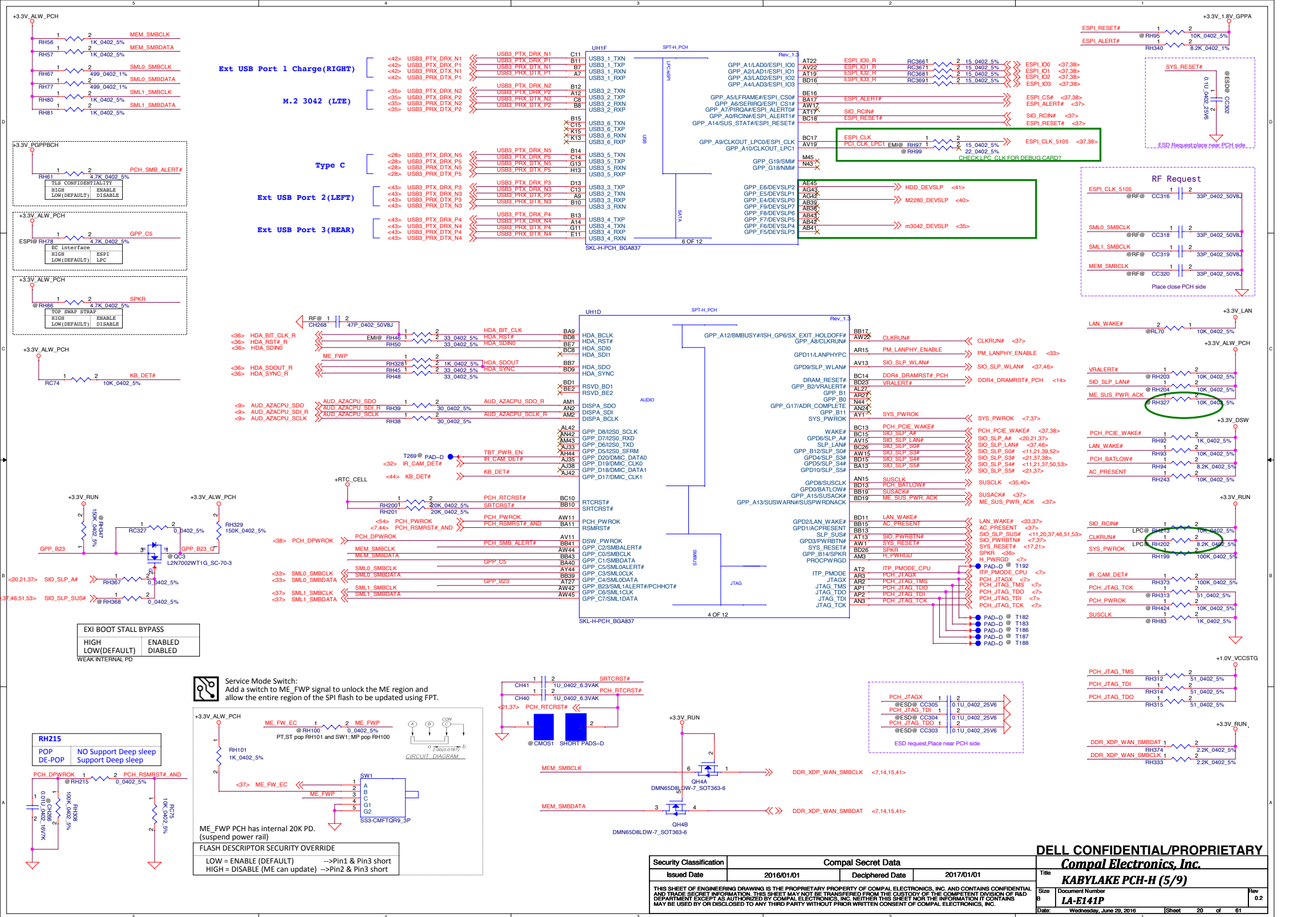


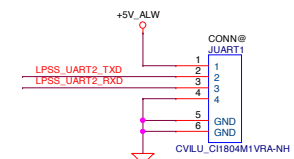
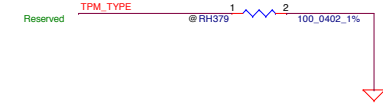
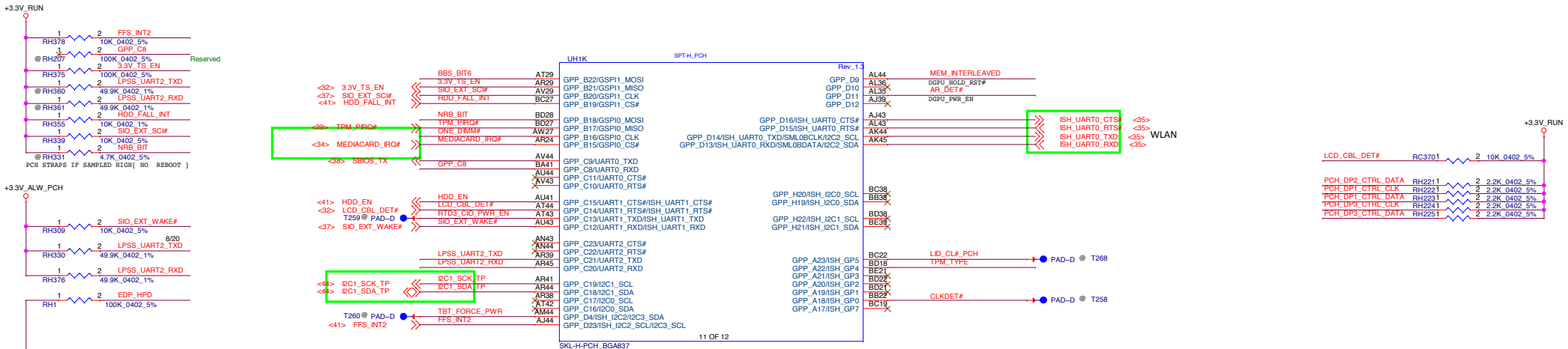
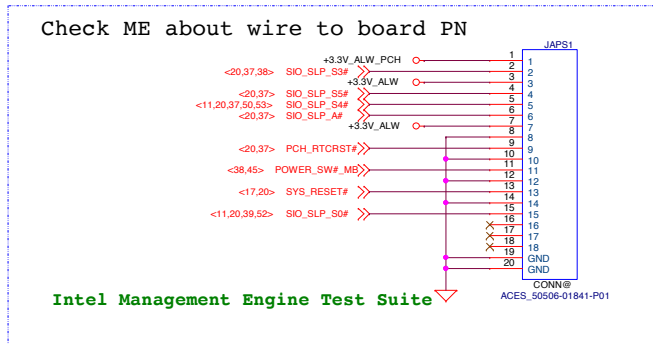
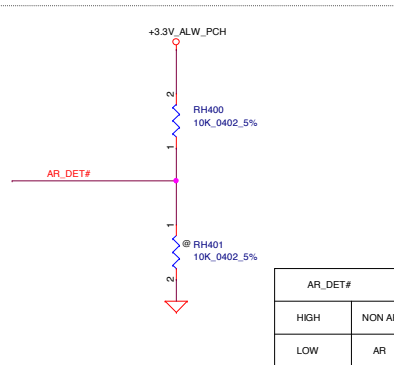
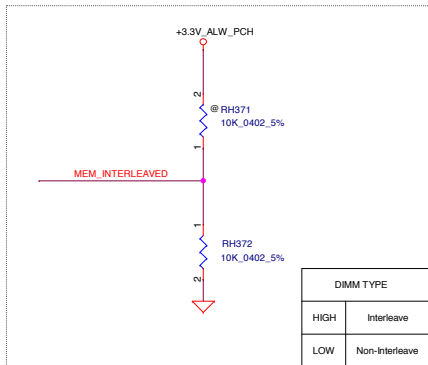
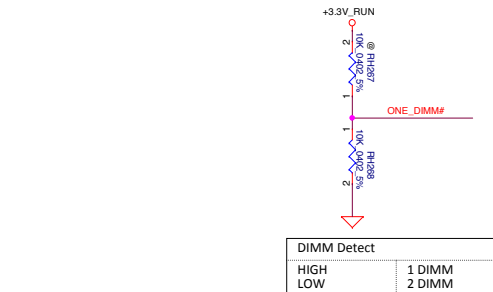
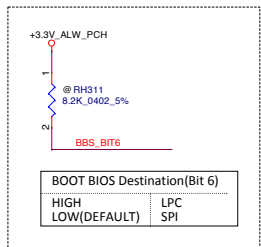
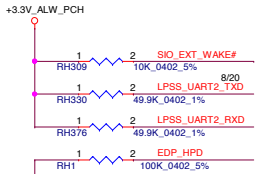
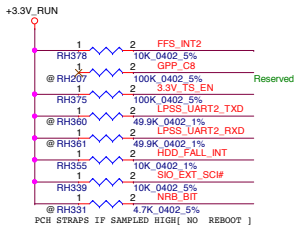
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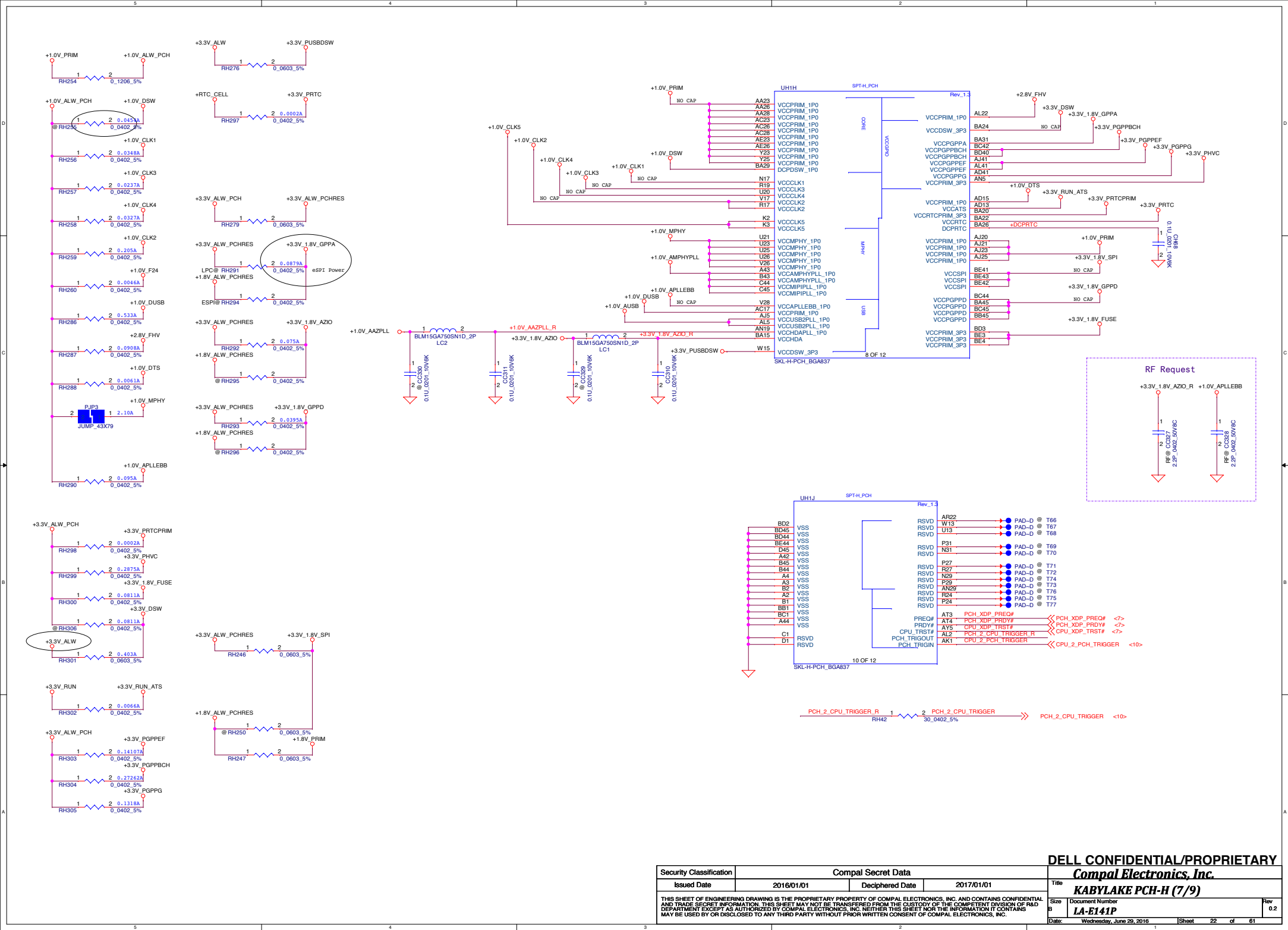


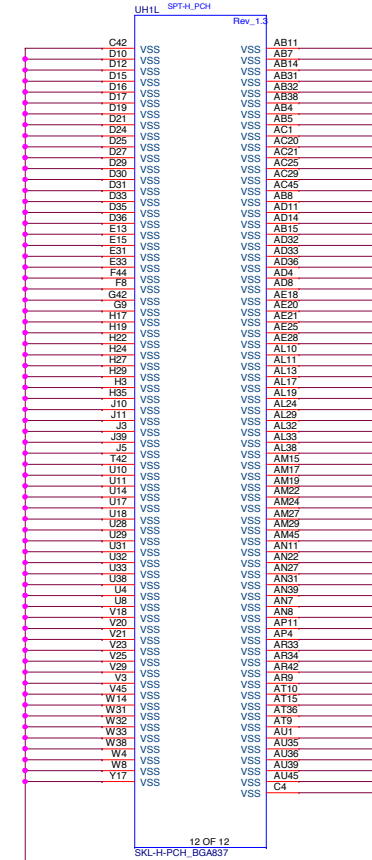
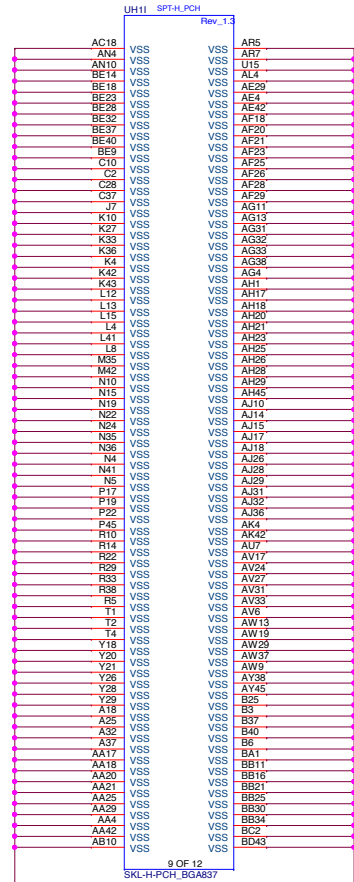
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				Date:	Wednesday, June 29, 2016
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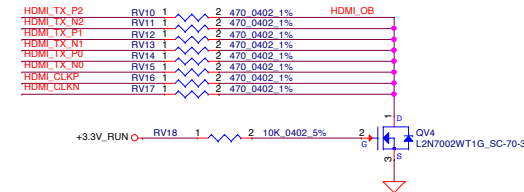
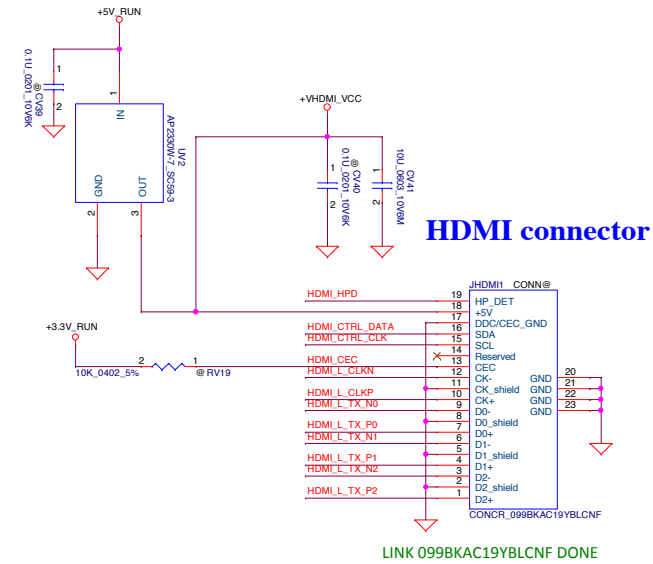
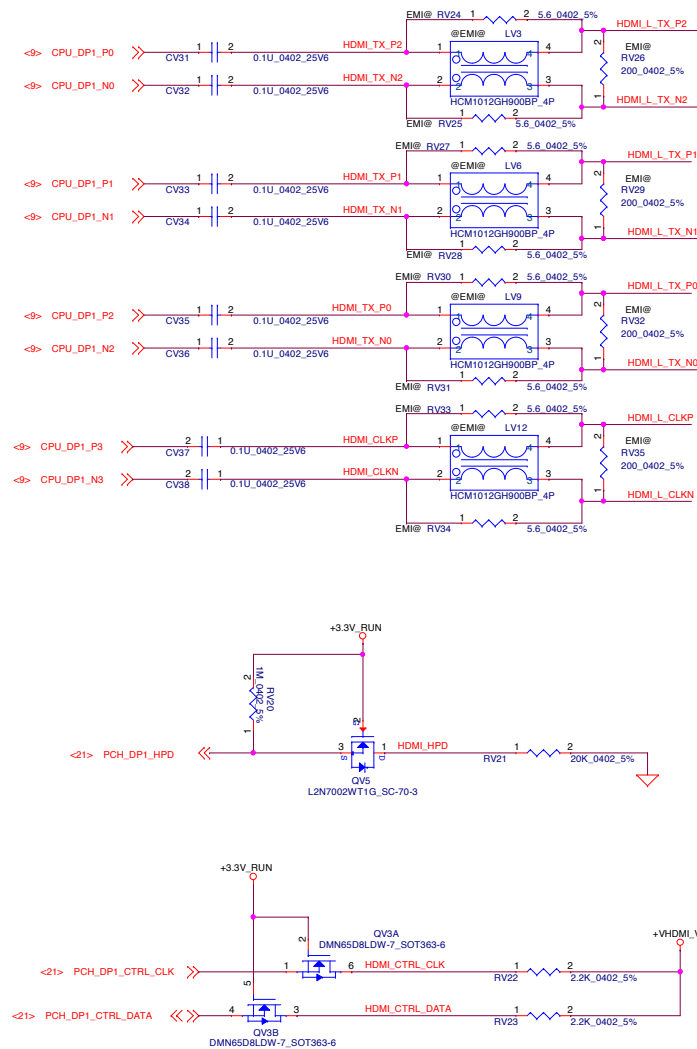






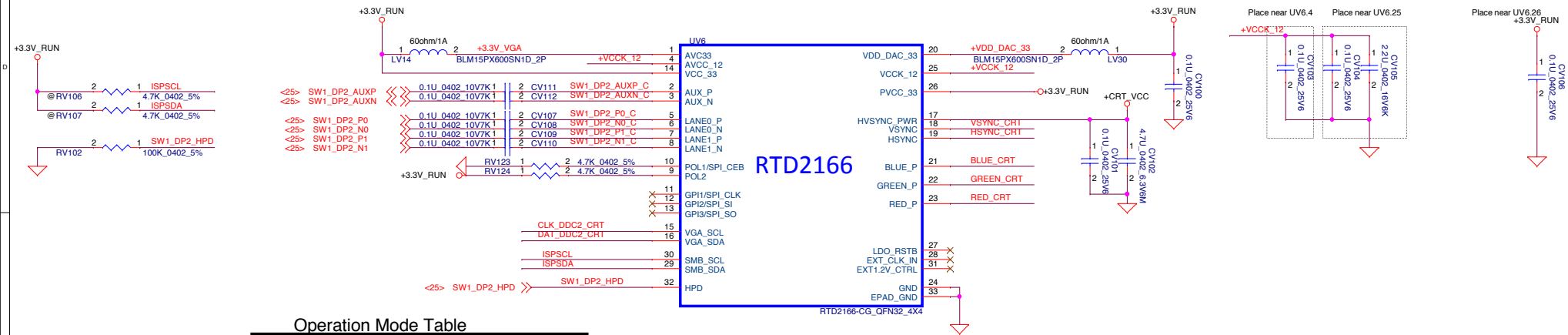


For Breckenridge 14



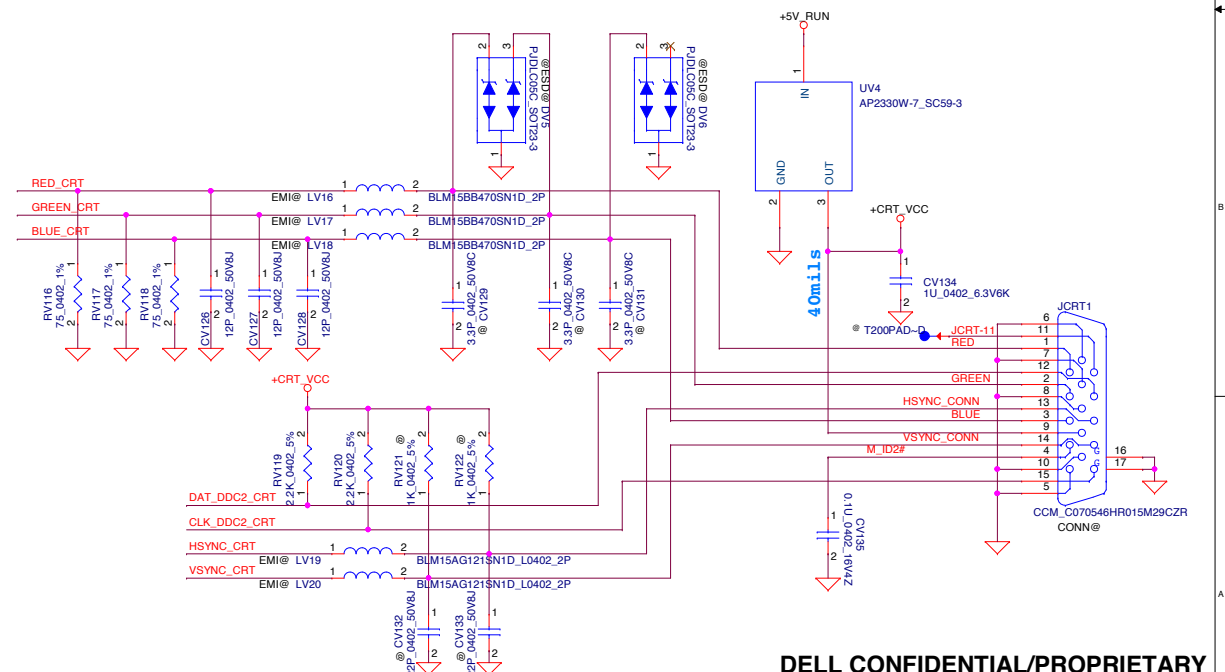
For TBT SW2_DP2
For non-TBT SW1_DP2

For Realtek Solution



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM



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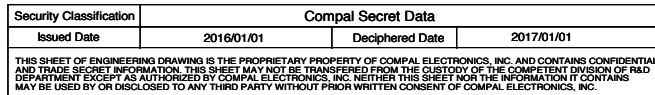
Compal Electronics, Inc.

DP to VGA & VGA Conn

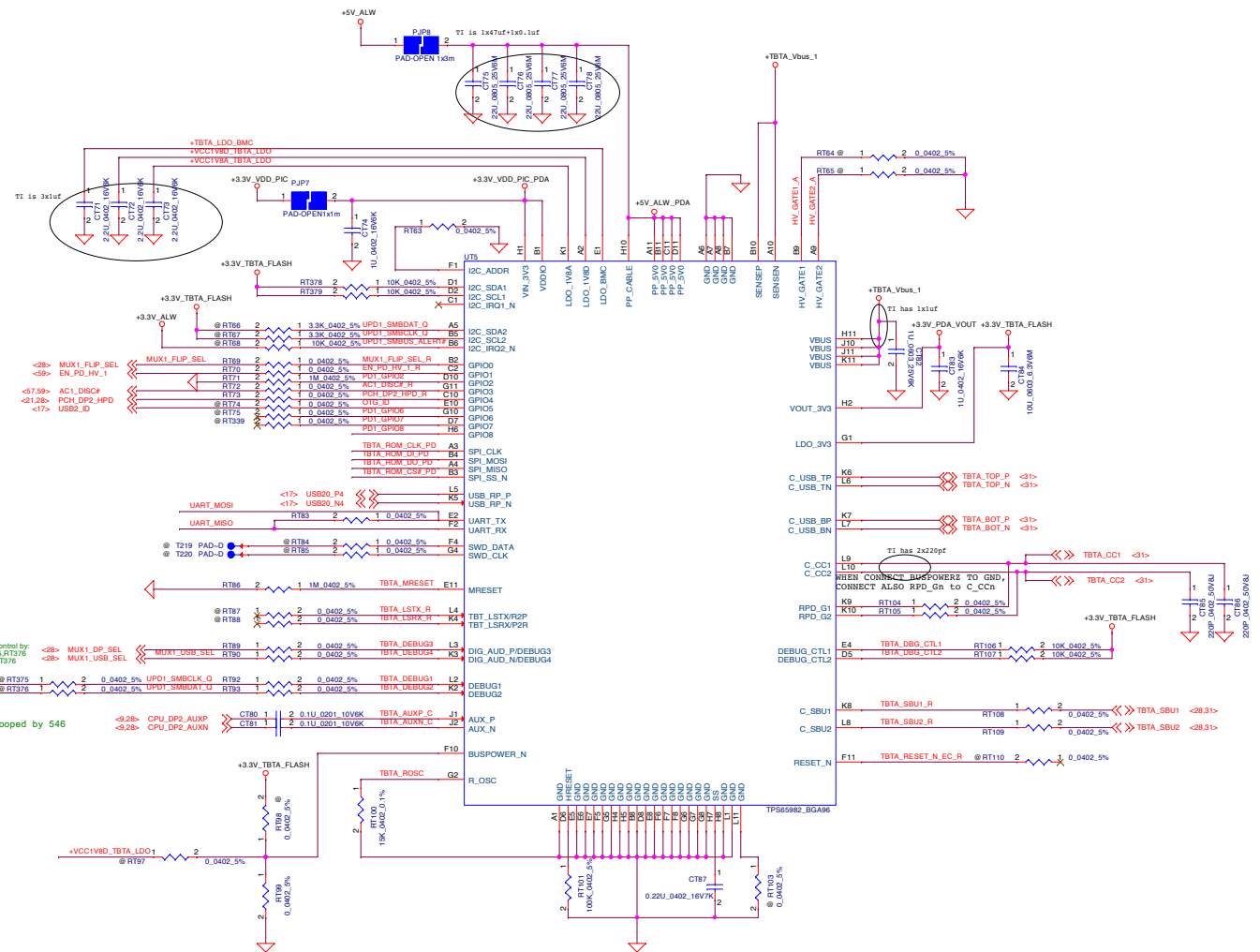
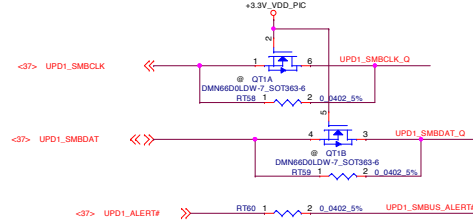
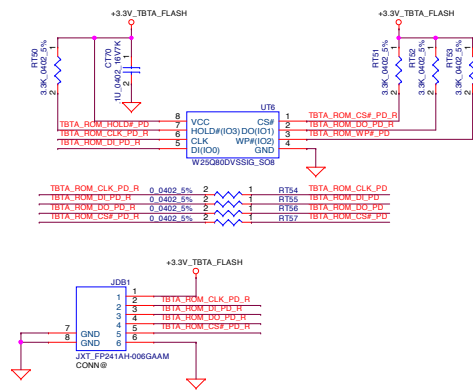
Document Number
LA-E141P

Rev	0.2
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Date: Wednesday, June 29, 2016		Sheet 27 of 61	
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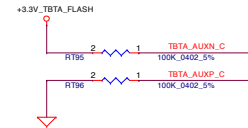


For Non-AR config



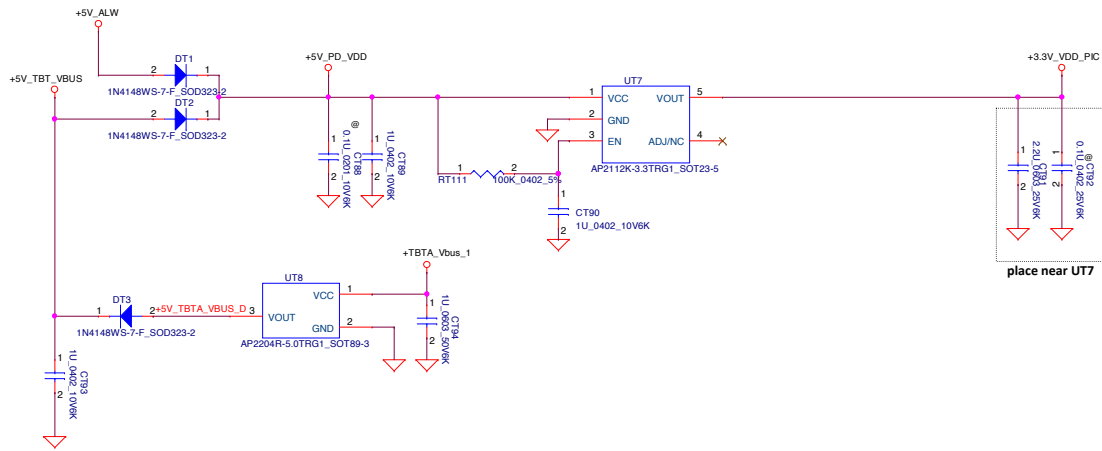
DIV = R2 / (R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only SV @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported T1 VID supported
0.10	0.18	1	UFP only SV @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes-Sink, C and D pin configuration T1 VID supported
0.20	0.28	2	UFP only SV @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported T1 VID supported
0.30	0.38	3	UFP only SV @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes-Sink, C and D pin configuration T1 VID supported
0.40	0.48	4	DRP SV @0.9-3.0A Sink capability SV @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported T1 VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP SV @0.9-3.0A Sink capability SV @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes- Source, C, D, and E pin configurations. T1 VID supported Accepts power role swaps but will not initiate. Accepts data role swap to DFP and can initiate.
0.60	0.68	6	DRP SV @0.9-3.0A Sink capability SV @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes- Source, C, D, and E pin configurations. T1 VID supported Accepts power role swaps but will not initiate. Accepts power role swap to DFP and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host IF can't.

Route in pass through manner so AUX can be snooped by 546



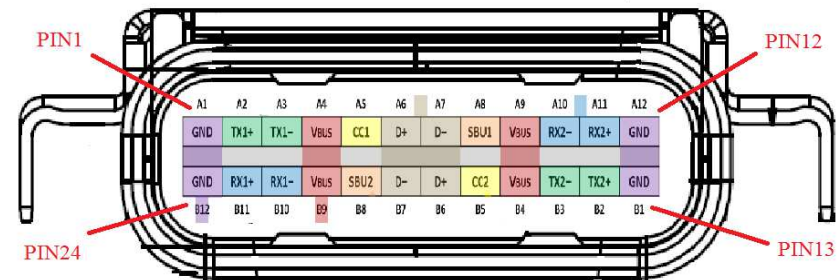
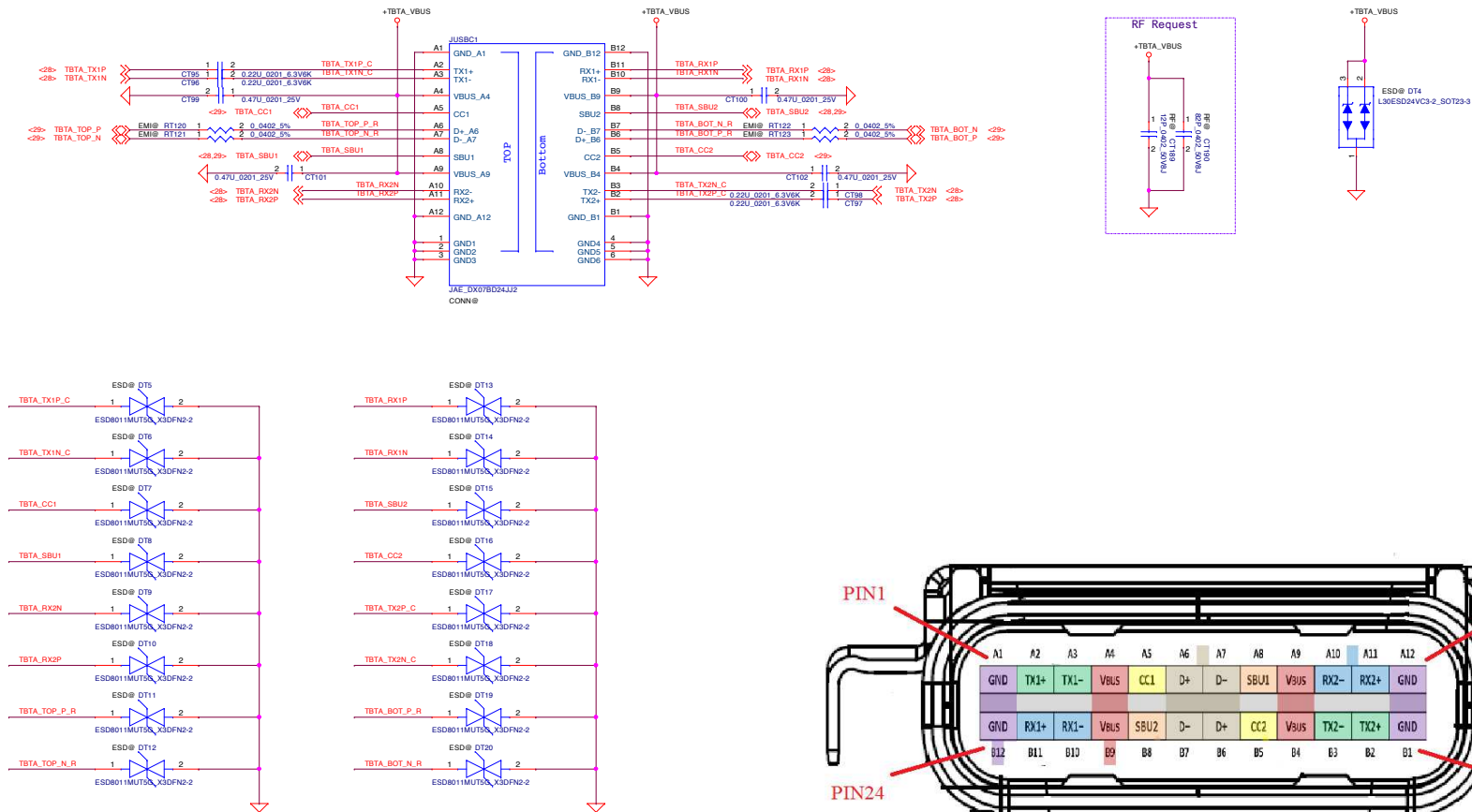
Need Link TPS65982D

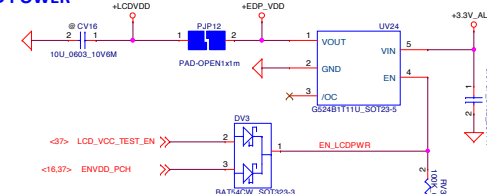
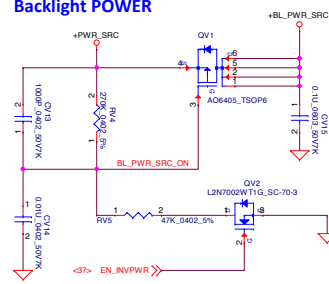
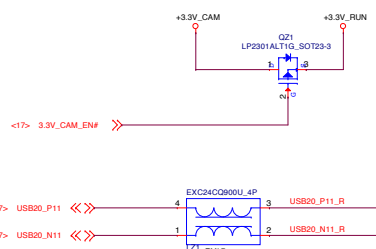
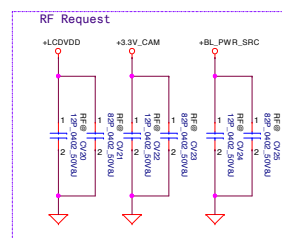
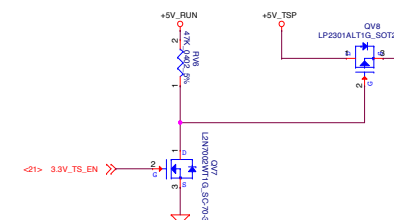
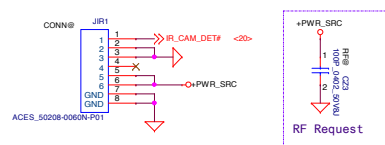
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Issued Date	2016/01/01	Deciphered Date	2017/01/01	[Type CPJD Controller TI] Title	
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Date	2016-01-26	Deciphered	2017-01-01	Rev 0.2	



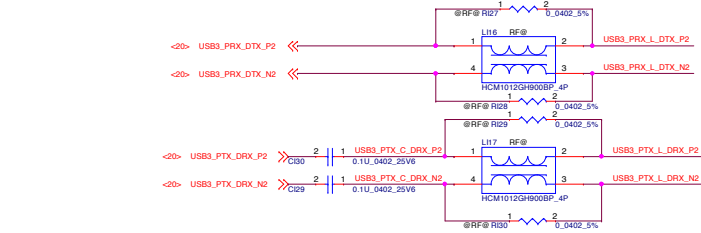
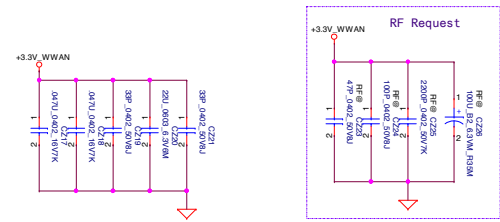
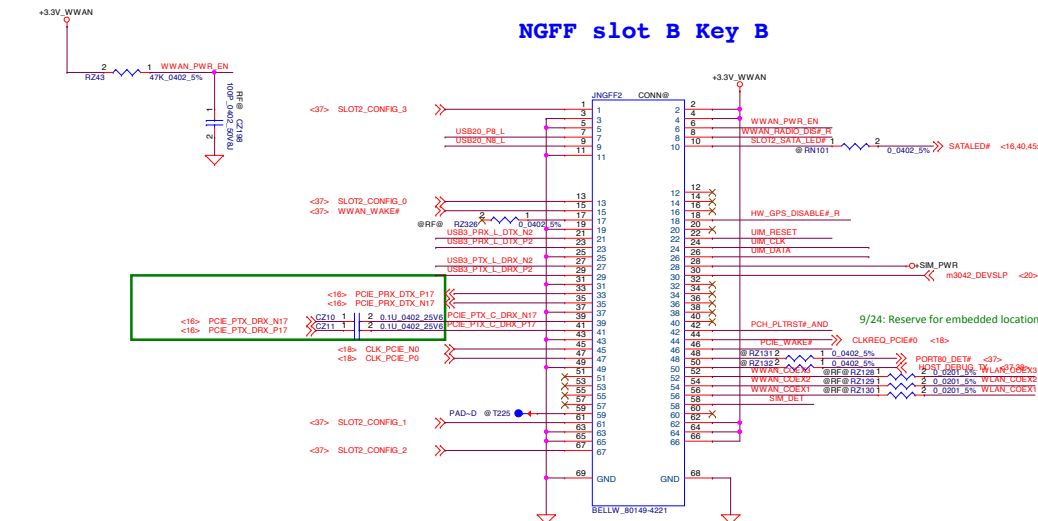
place near UT7

Security Classification		Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY	
Issued Date		2016/01/01		Deciphered Date	
2017/01/01		Title		Compal Electronics, Inc.	
2017/01/01		[Type C]PD Power		Rev	
2017/01/01		LA-E141P		0.2	
Date		Wednesday, June 29, 2016		Sheet	
30		of		61	

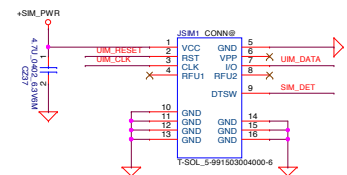




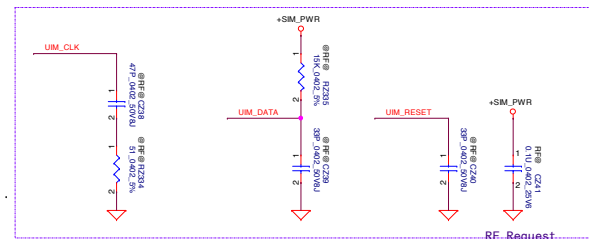
NGFF slot B Key B



SIM Card Push-Push



T-SOL_5-991503004000-6 LINK DONE



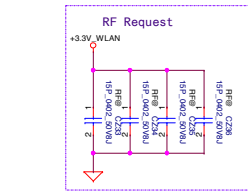
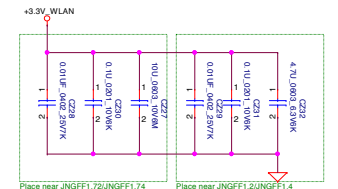
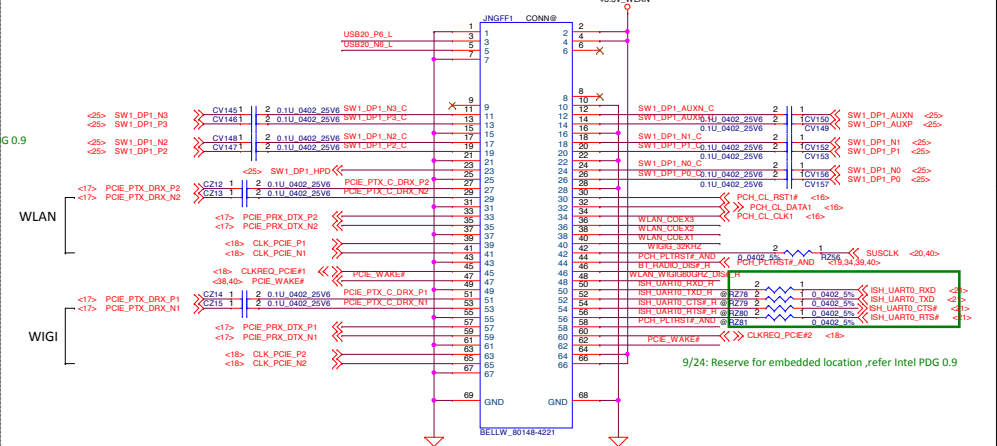
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	m3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIe(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIe(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

for Brekenridge 12/14/15 UMA

For TBT SW2_DP1
For non-TBT SW1_DP1

NGFF slot A Key A

80148-3221&80148-4221 Footprint the same

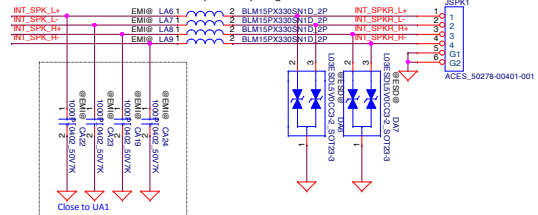


Power Rating TBD

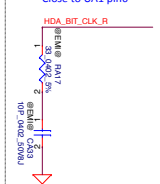
PWR Rail	Voltage Tolerance	Primary Power Peak	Aux Power Normal
+3.3V			

Internal Speakers Header

40 mils trace keep 20 mil spacing



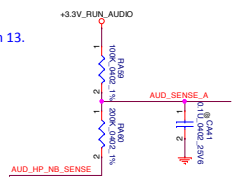
Close to UA1 pin6



DMIC_CLK0

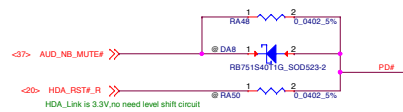


Place closely to Pin 13.



Add for solve
pop noise and
detect issue

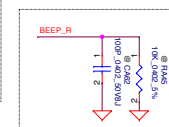
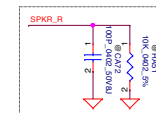
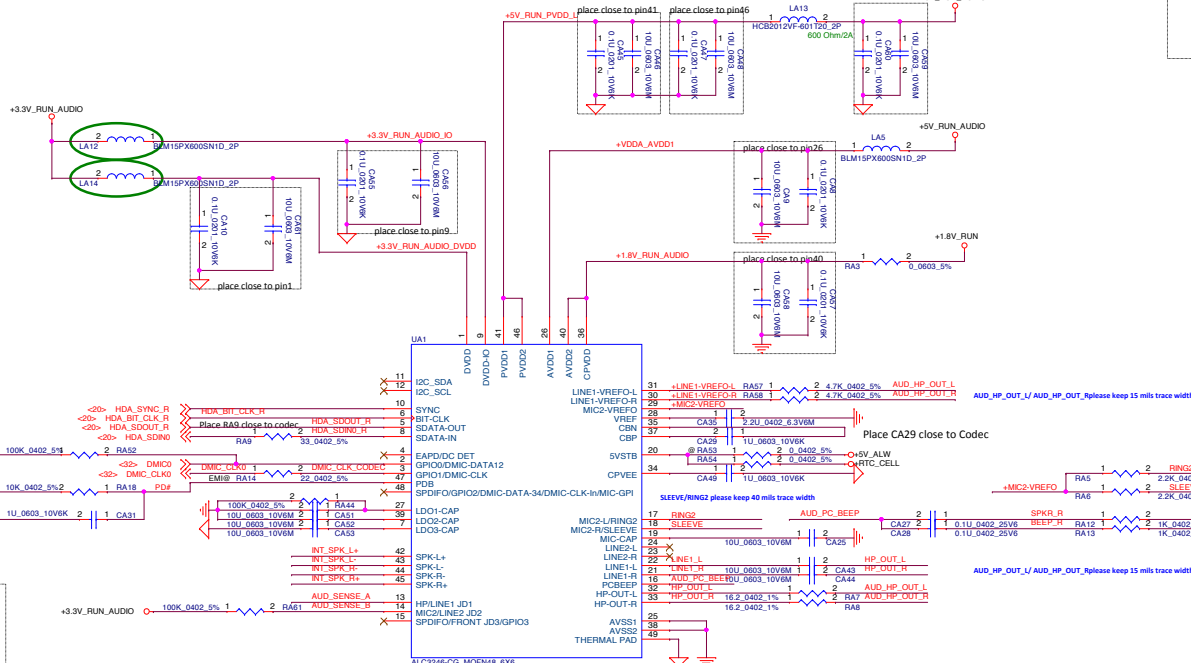
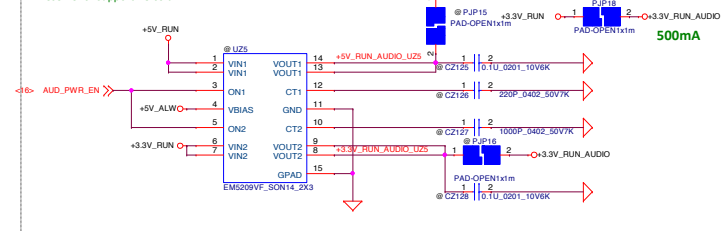
CLASS-D POWER DOWN CONTROL CIRCUIT



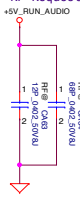
RE313@one control line if DVDD
DE2@two control lines1

Power sequence +5V, RUN, AUDIO(501μs) > +3.3V, RUN, AUDIO(1204μs) > +1.5V, RUN

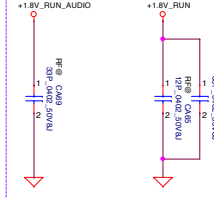
Reserve for support D3 cold



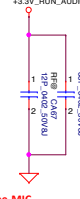
RF Request



RF Request



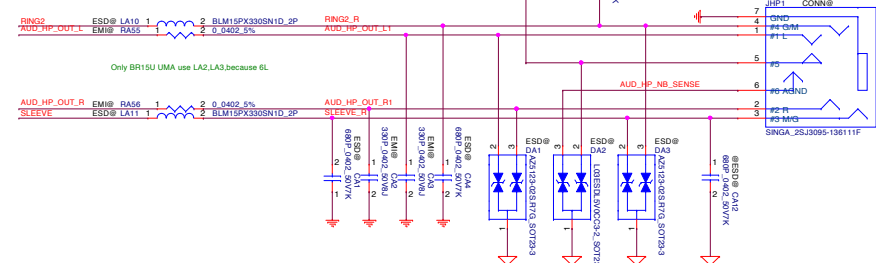
- 2.0V DUM. AUDIO



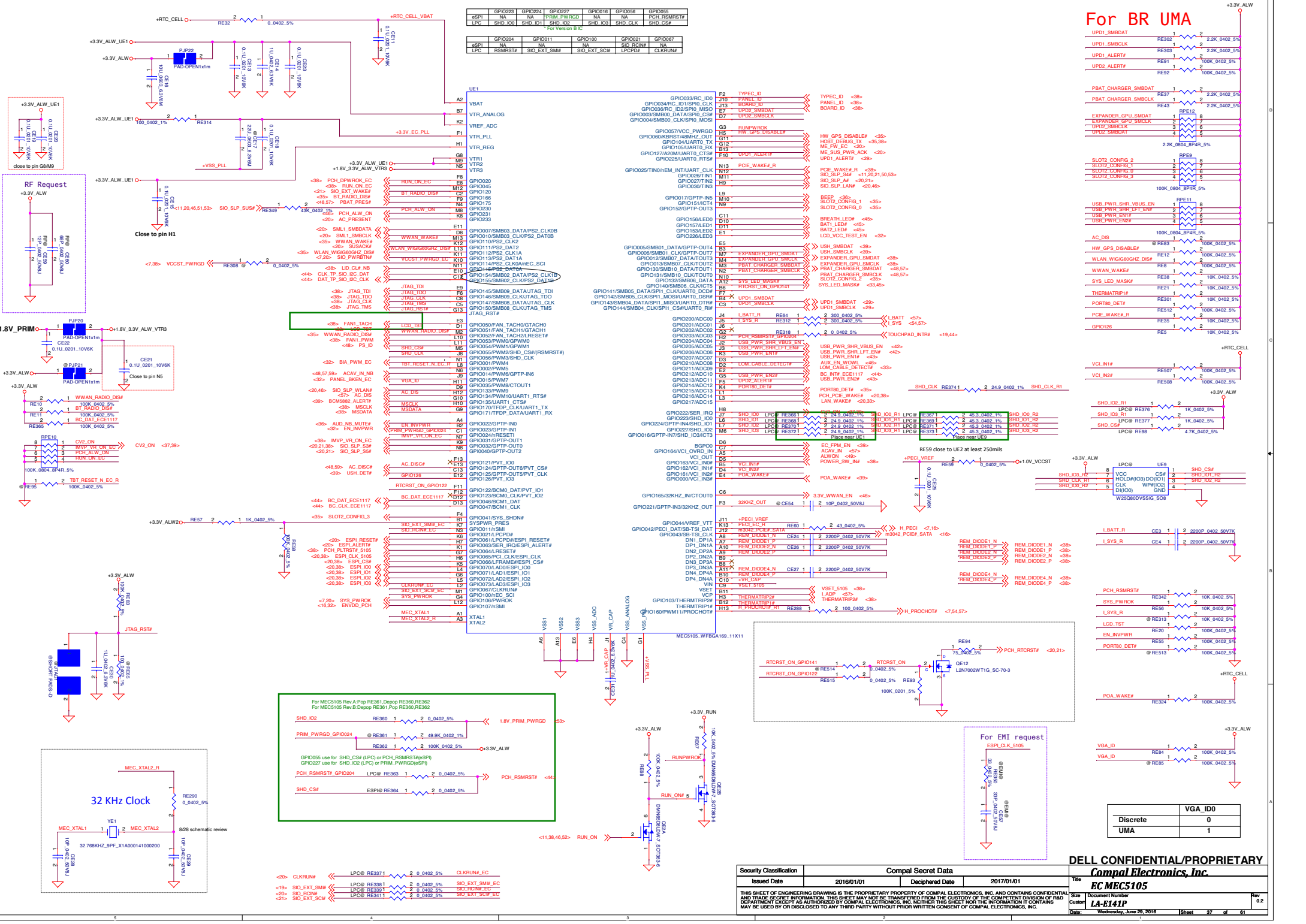
Add this Filter to avoid other components/chips be influenced



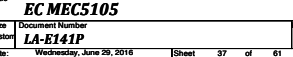
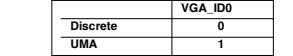
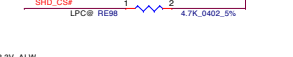
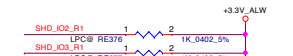
Global Headset
Universal Jack



Security Classification		Compal Secret Data		Title	
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				A4	LA-E141P
Date:				Ver:	Rev
2016.01.01				1	0.2



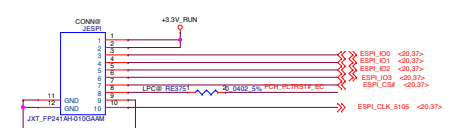
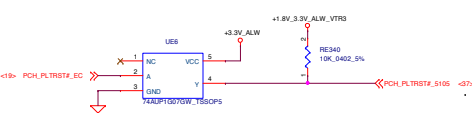
For BR UMA



DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
EC MEC5105

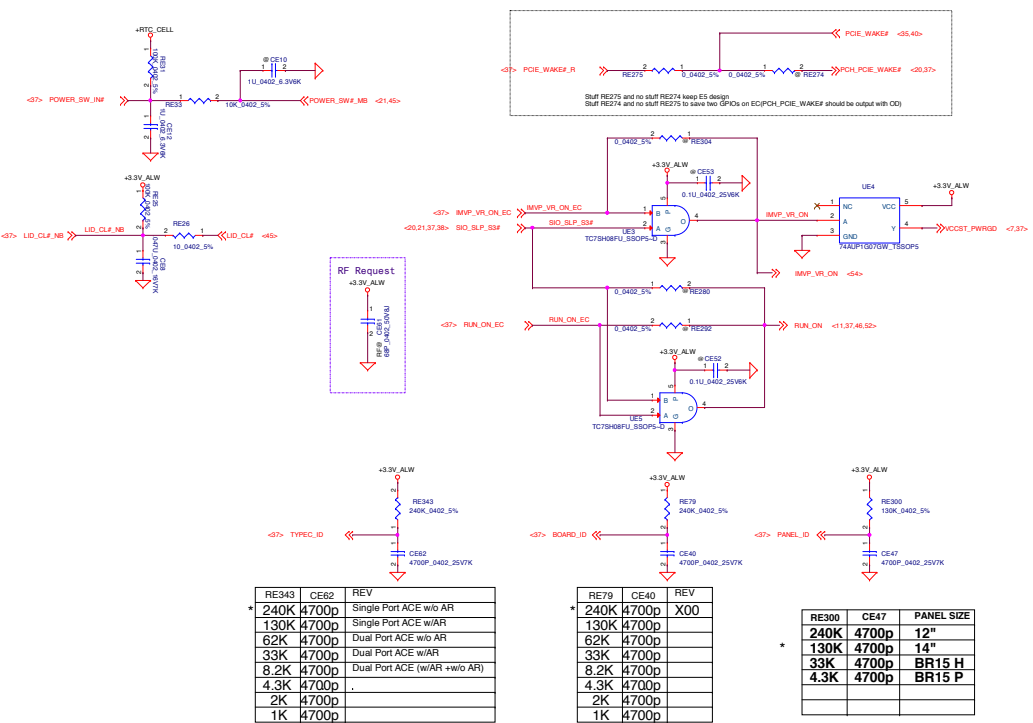
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Deciphered Date	2017/01/01

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LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_I00
4	LPC_LAD1	ESPI_I01
5	LPC_LAD2	ESPI_I02
6	LPC_LAD3	ESPI_I03
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

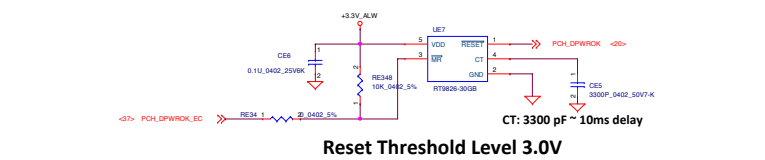


RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	

RE79	CE40	REV
240K	4700p	X00
130K	4700p	
62K	4700p	
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	12"
130K	4700p	14"
33K	4700p	BR15 H
4.3K	4700p	BR15 P

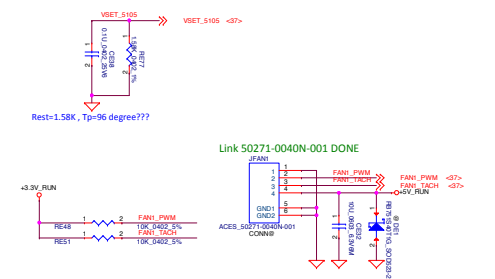
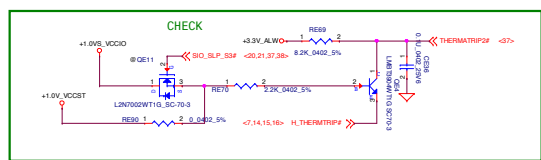
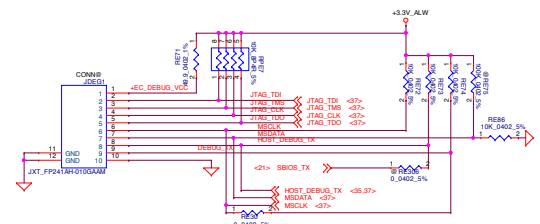
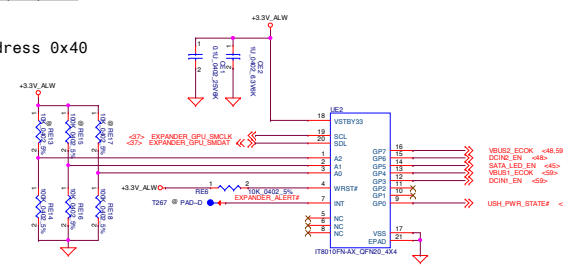
PD_ACE_DET# rise time is measured from 5%~68% BOARD_ID rise time is measured from 5%~68% PANEL_ID rise time is measured from 5%~68%



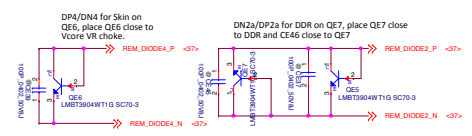
Reset Threshold Level 3.0V

Control Byte
0 1 0 0 A2 A1 A0 R/W
R/W = 0 = Write
R/W = 1 = Read

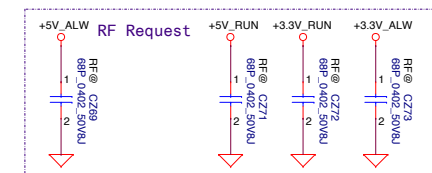
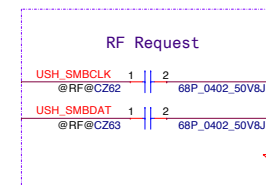
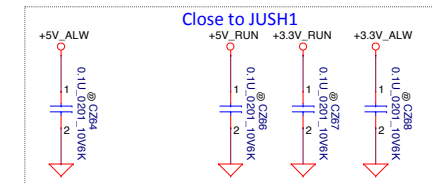
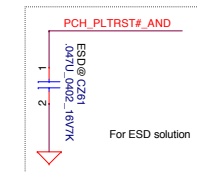
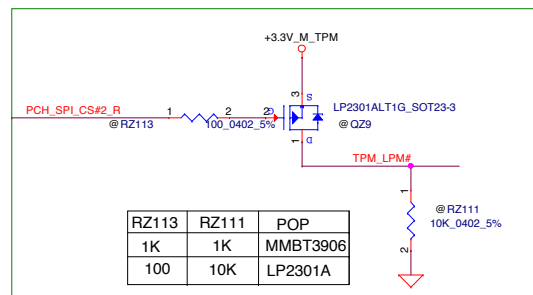
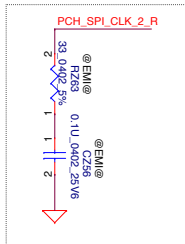
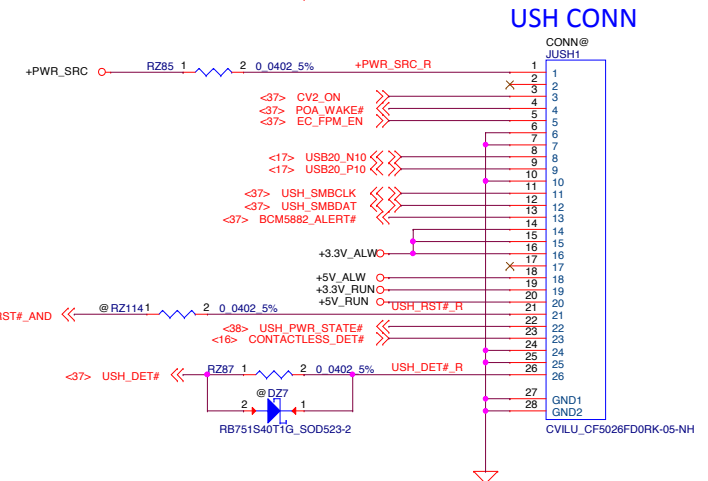
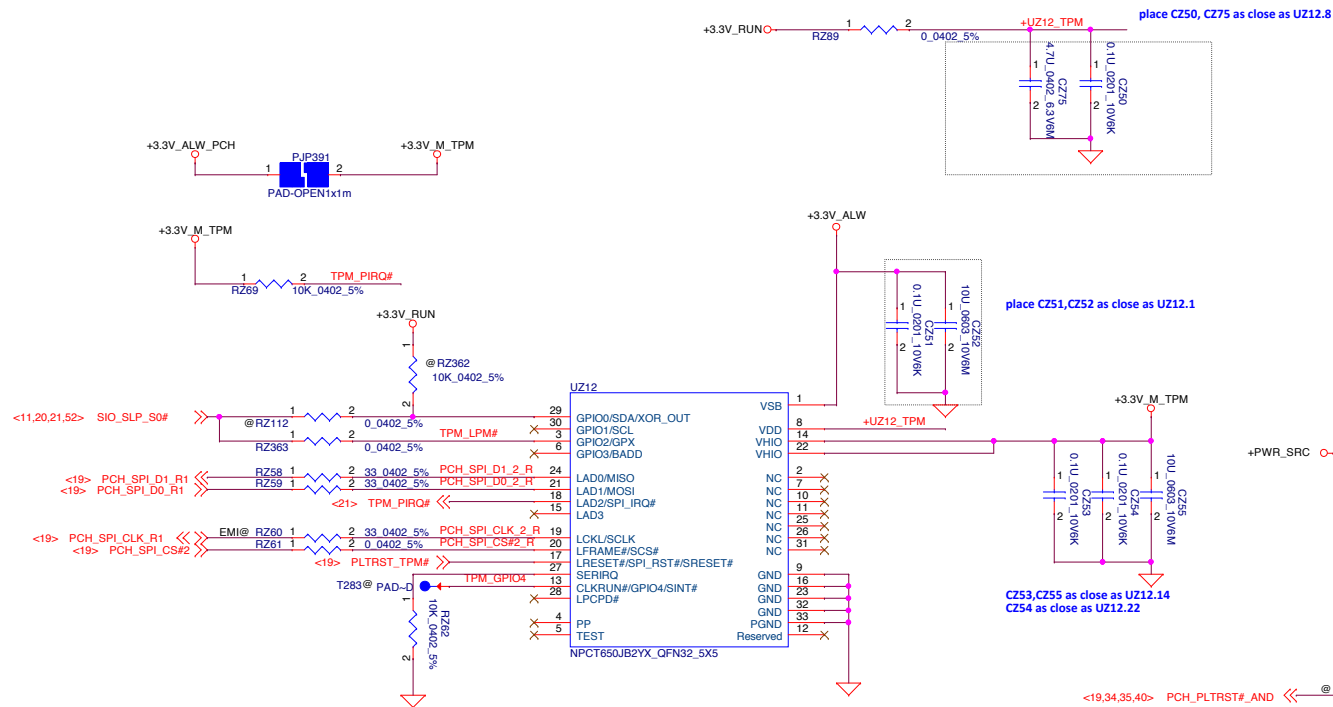
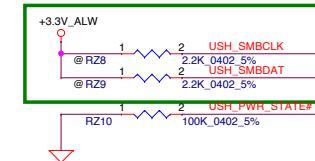
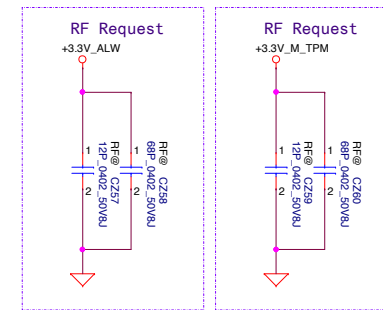
SMbus address 0x40



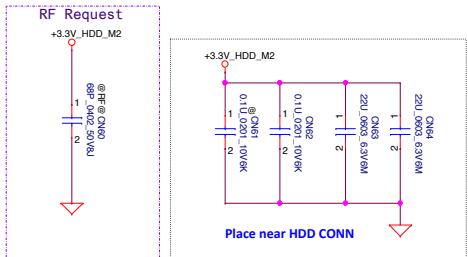
5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)



For NUVOTON TPM

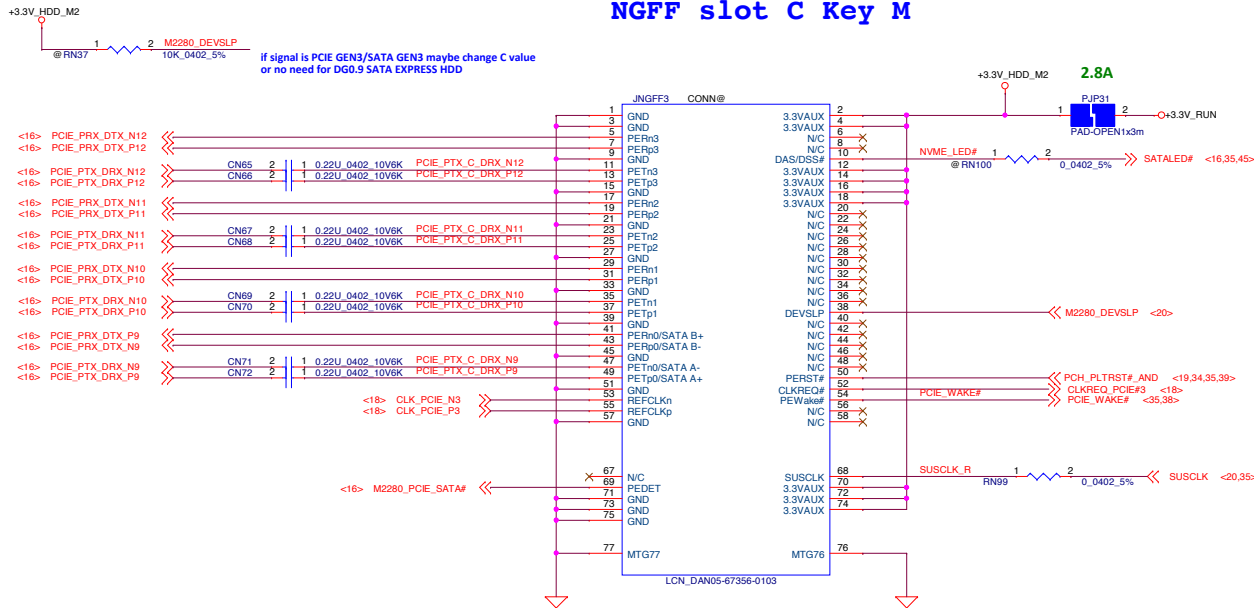


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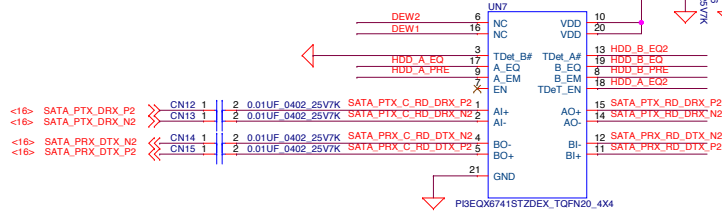
2280 SSD

NGFF slot C Key M



	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDeT_B#	NC	TDeT_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

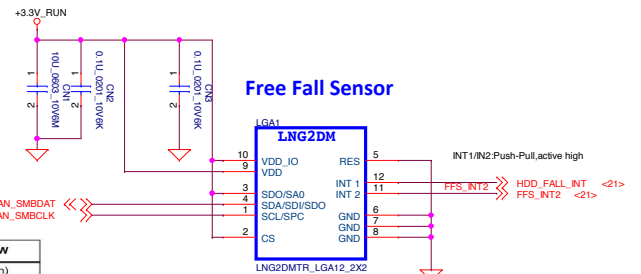
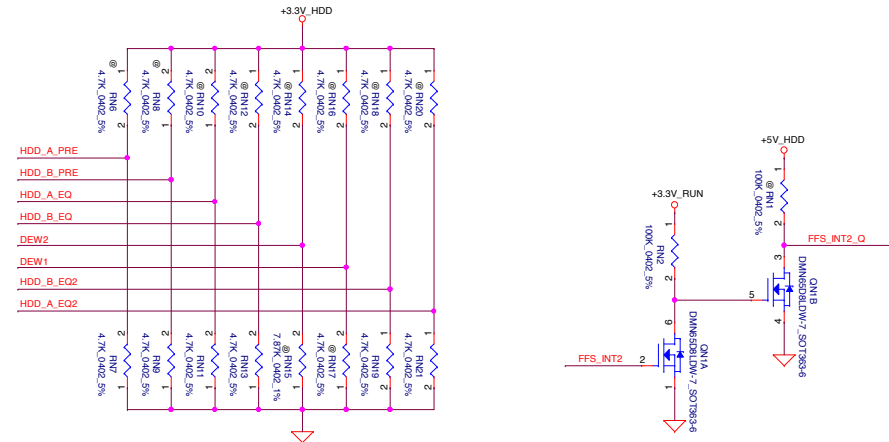
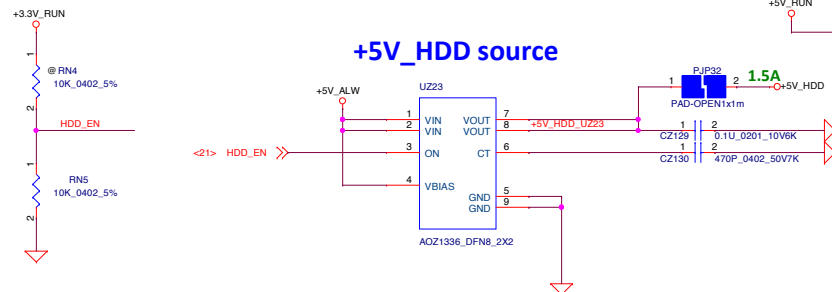
SATA Repeater



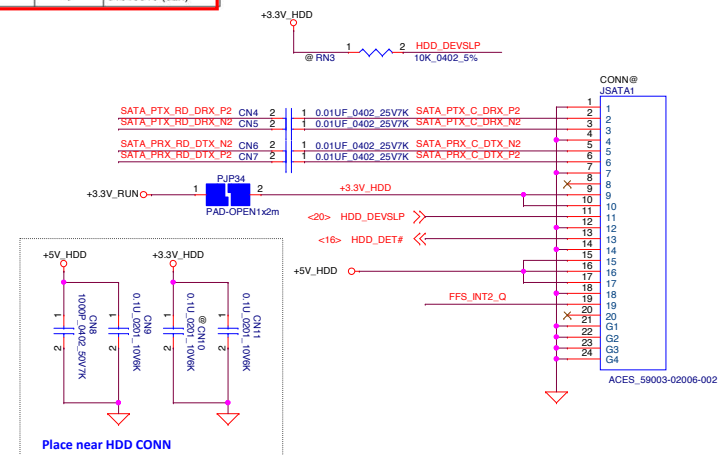
	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom PI3EQX6741ST	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC	NC	PD (RN5)	PD (RN11)
TI SN75LVCP601	PD (RN13)	NC	PD (RN83)	PD (RN23)	NC (IPU)	NC (IPU)	PH (RN8)	PH (RN10)
Parade PS8527C	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC (1/2 VDD)	PD (RN19)	NC (1/2 VDD)	NC (1/2 VDD)

			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB
2nd	TI	0 NC 1	7dB 9dB 14dB	7dB 9dB 14dB	0 NC 1	0dB -4dB -2dB	0dB -4dB -2dB
3rd	Parade	EQ2 EQ1 (M = VDD/2) 0 M 0 0 0 1 M M M 0 M 1 1 M 1 0 1 1	2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	0 NC 1	0dB -3.5dB -1.5dB	0dB -3.5dB -1.5dB

* red color is current setting



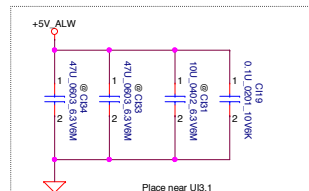
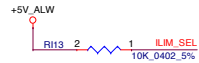
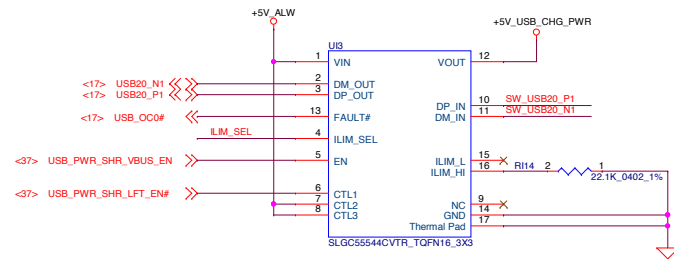
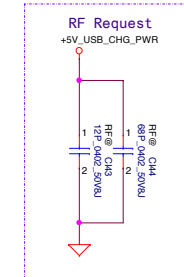
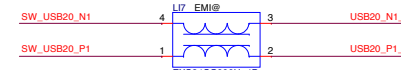
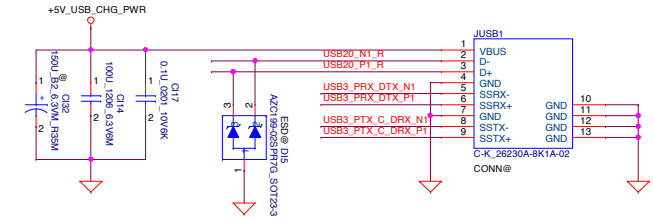
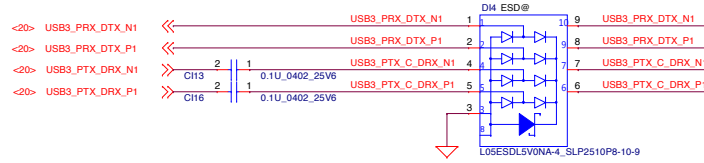
Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)



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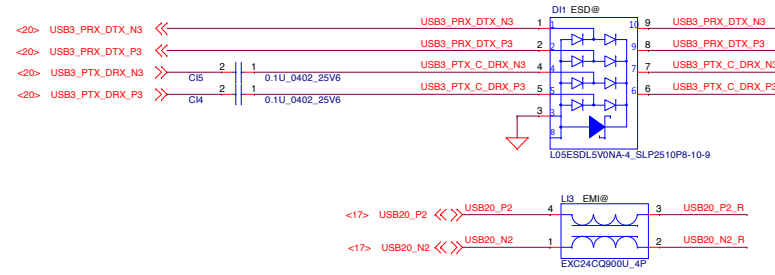
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For PWR SW + Charger combine IC

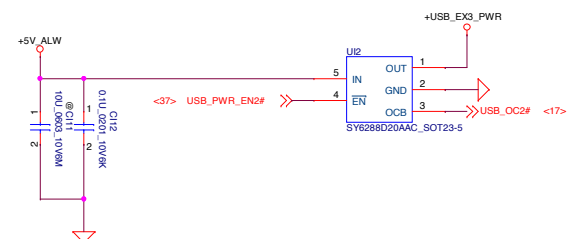
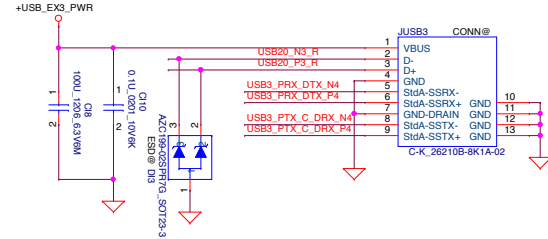
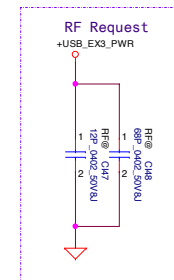
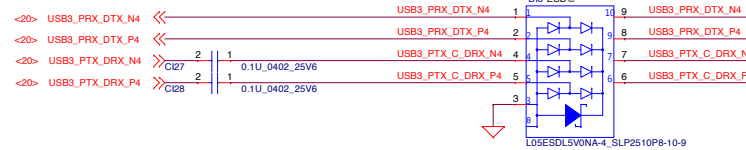
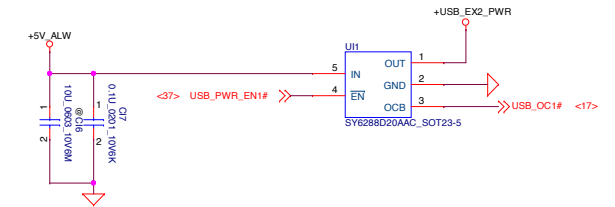
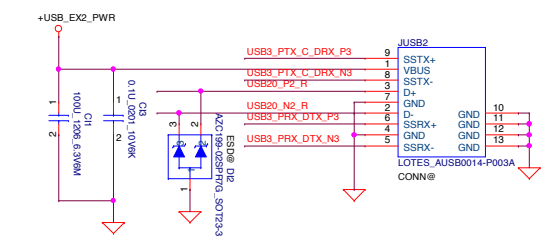
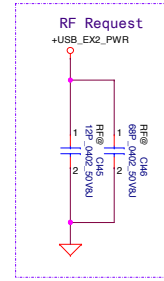


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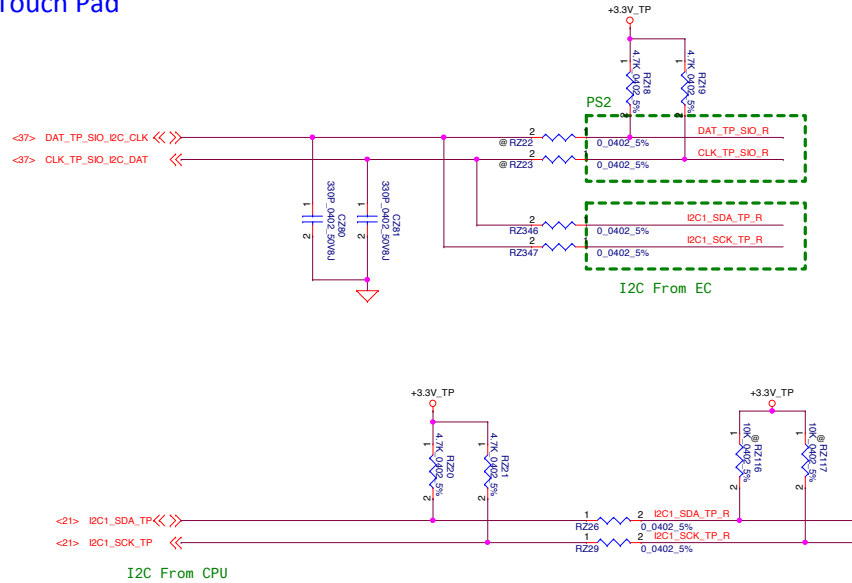
For Breckenridge 14&15/Steamboat 14



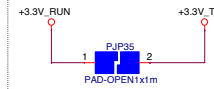
DfB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm



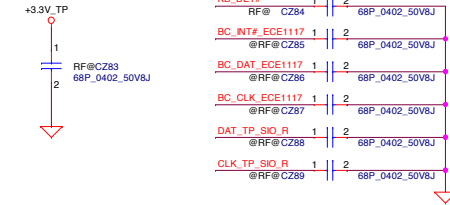
Touch Pad



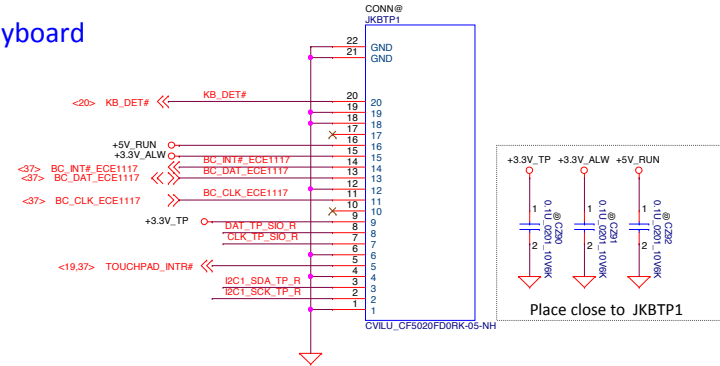
Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



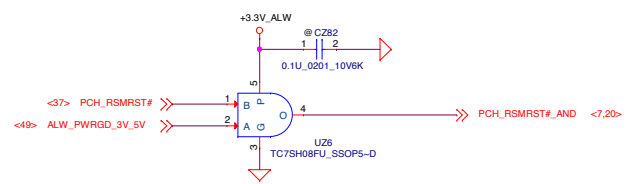
RF Request



Keyboard



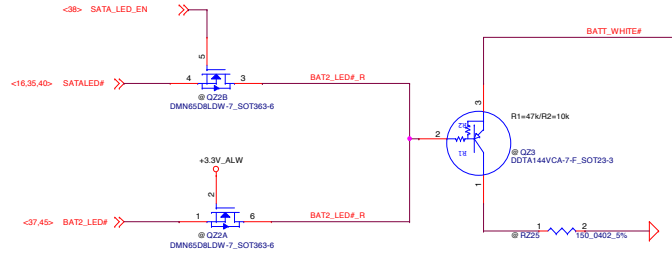
RSMRST circuit



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							Keyboard
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HDD LED MUX

means EC can switch battery white led and HDD LED by hot key "Fn+H"

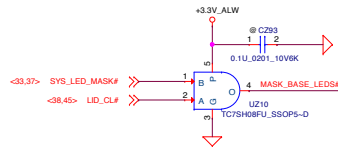
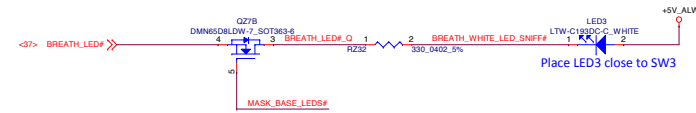


Battery LED

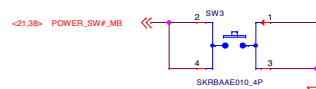


Breath LED

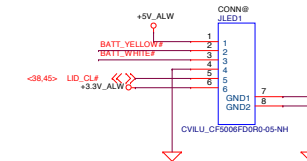
LED PIN change to SC50000FL00 from SC50000BA00



POWER & INSTANT ON SWITCH



LED board CONN

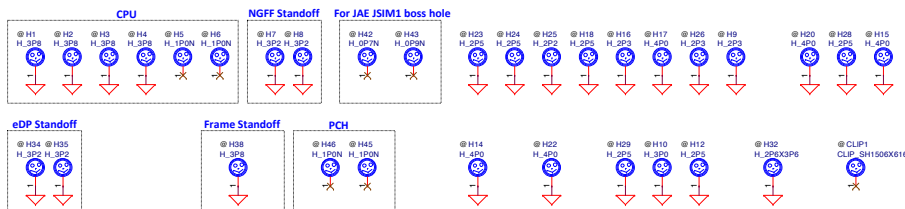


Fiducial Mark



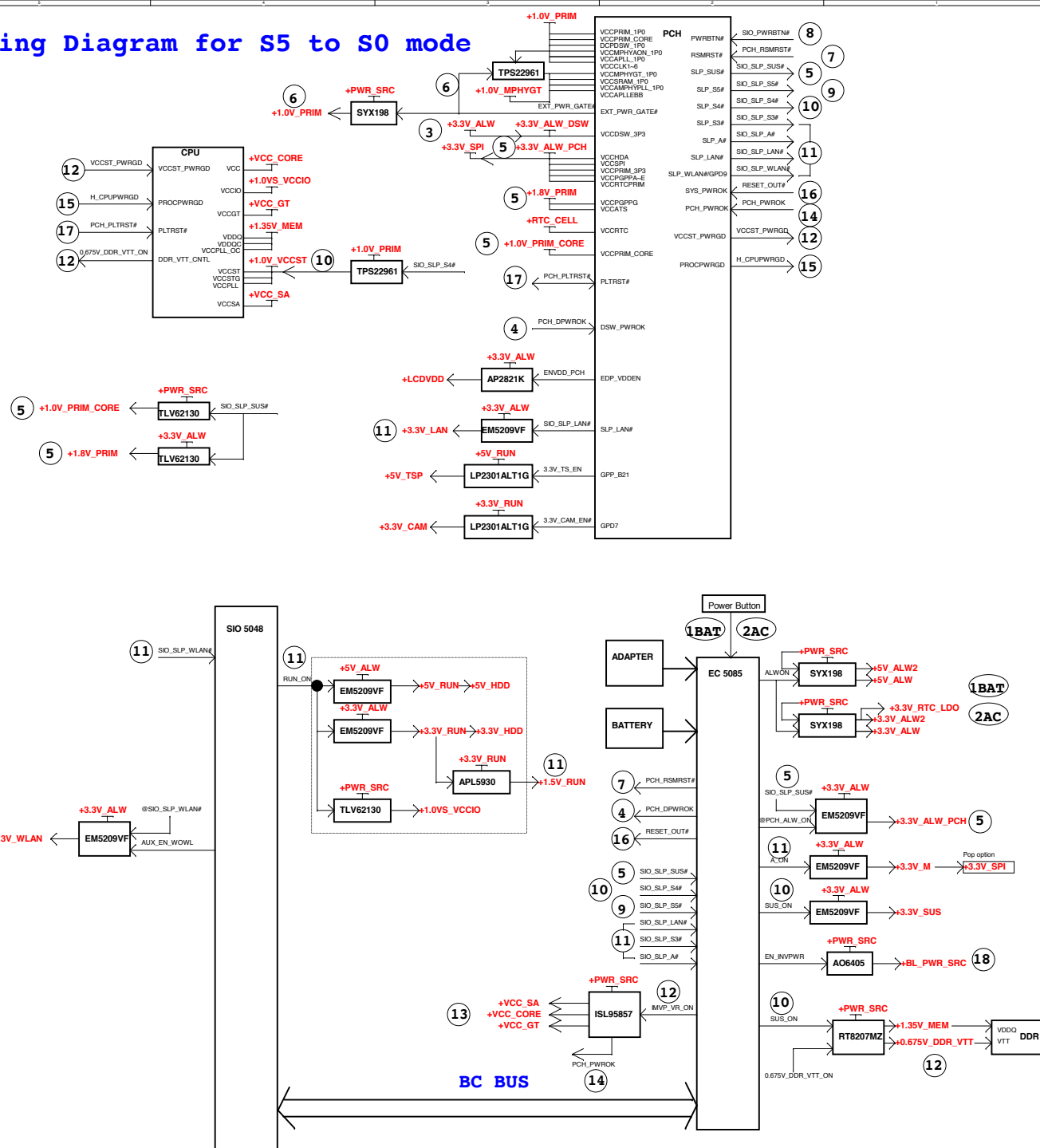
LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



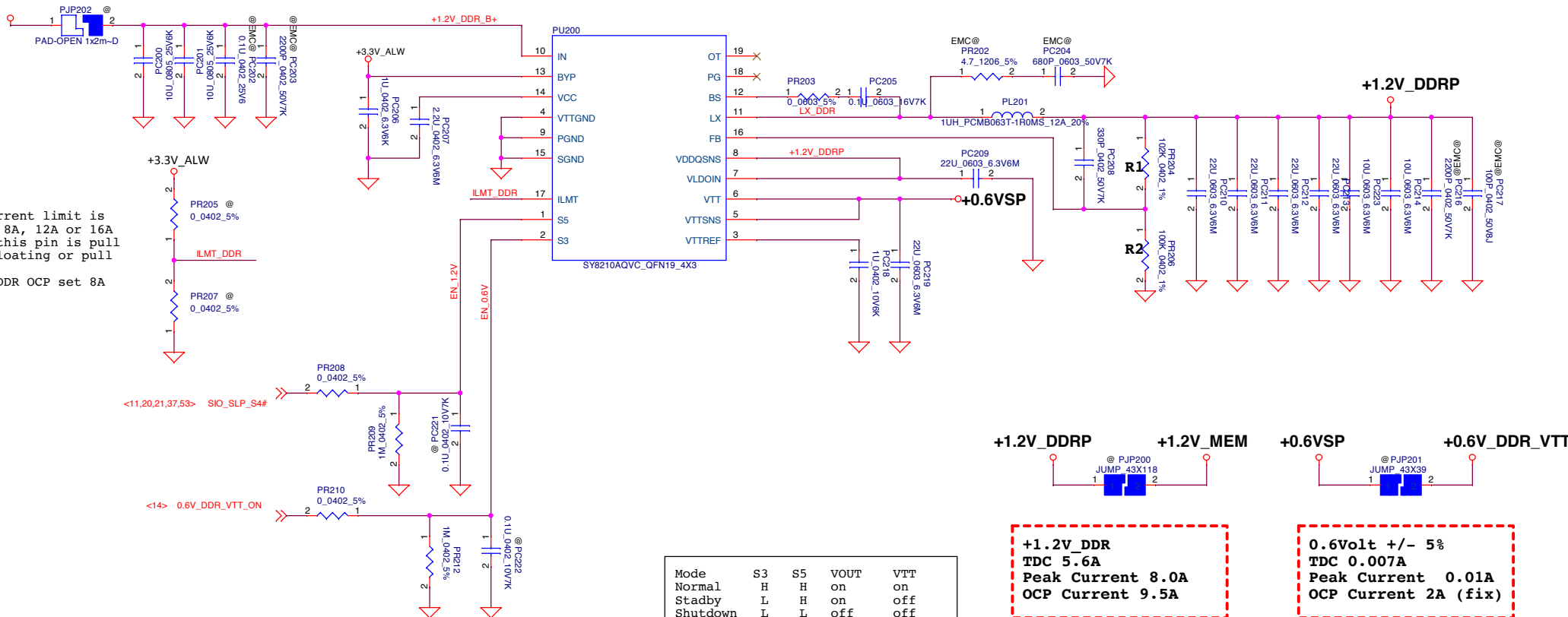
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				PAD, LED
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Timing Diagram for S5 to S0 mode



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+PWR_SRC



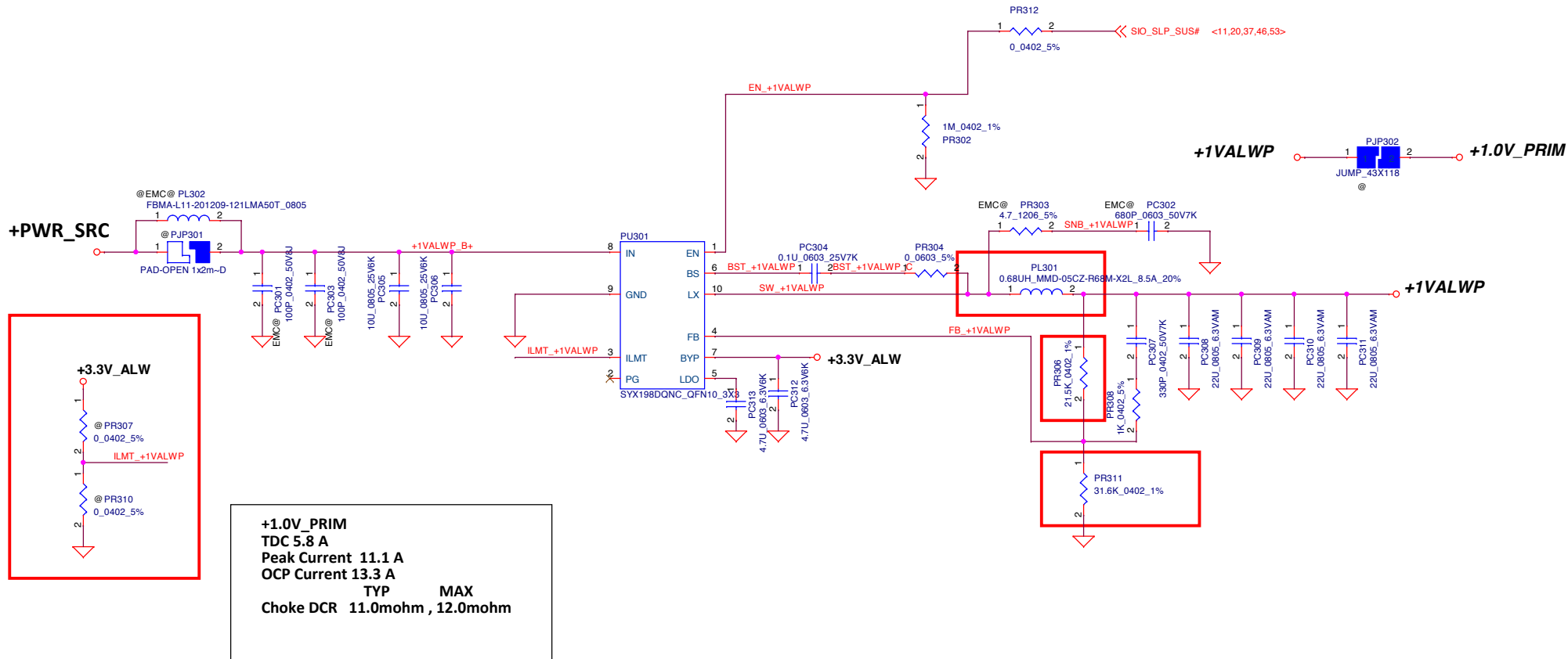
The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high
+1.2V_DDR OCP set 8A

Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_DDR
TDC 5.6A
Peak Current 8.0A
OCP Current 9.5A

0.6Volt +/- 5%
TDC 0.007A
Peak Current 0.01A
OCP Current 2A (fix)



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

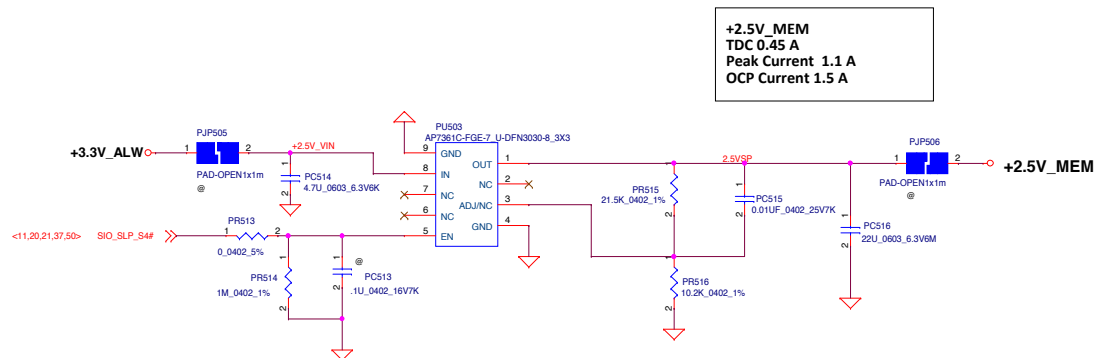
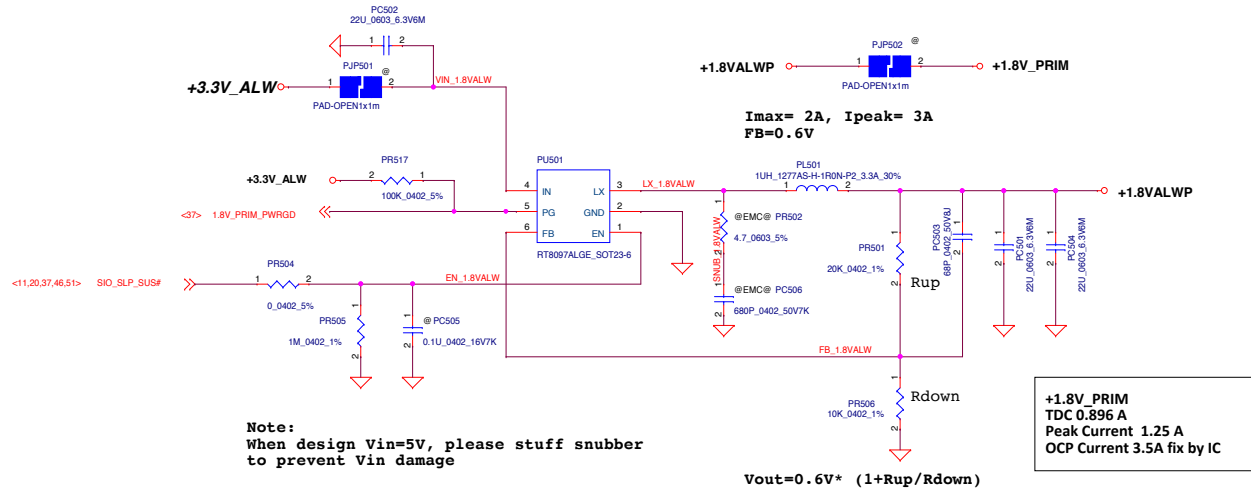
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+1VALWP

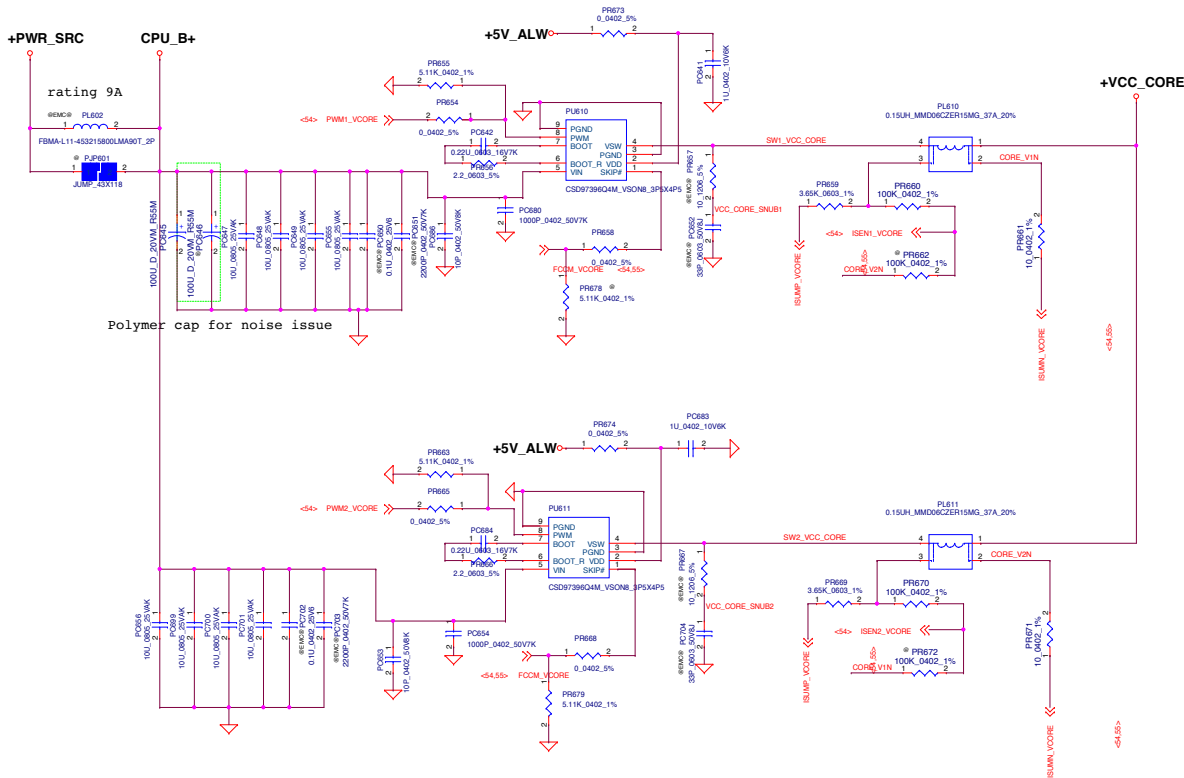
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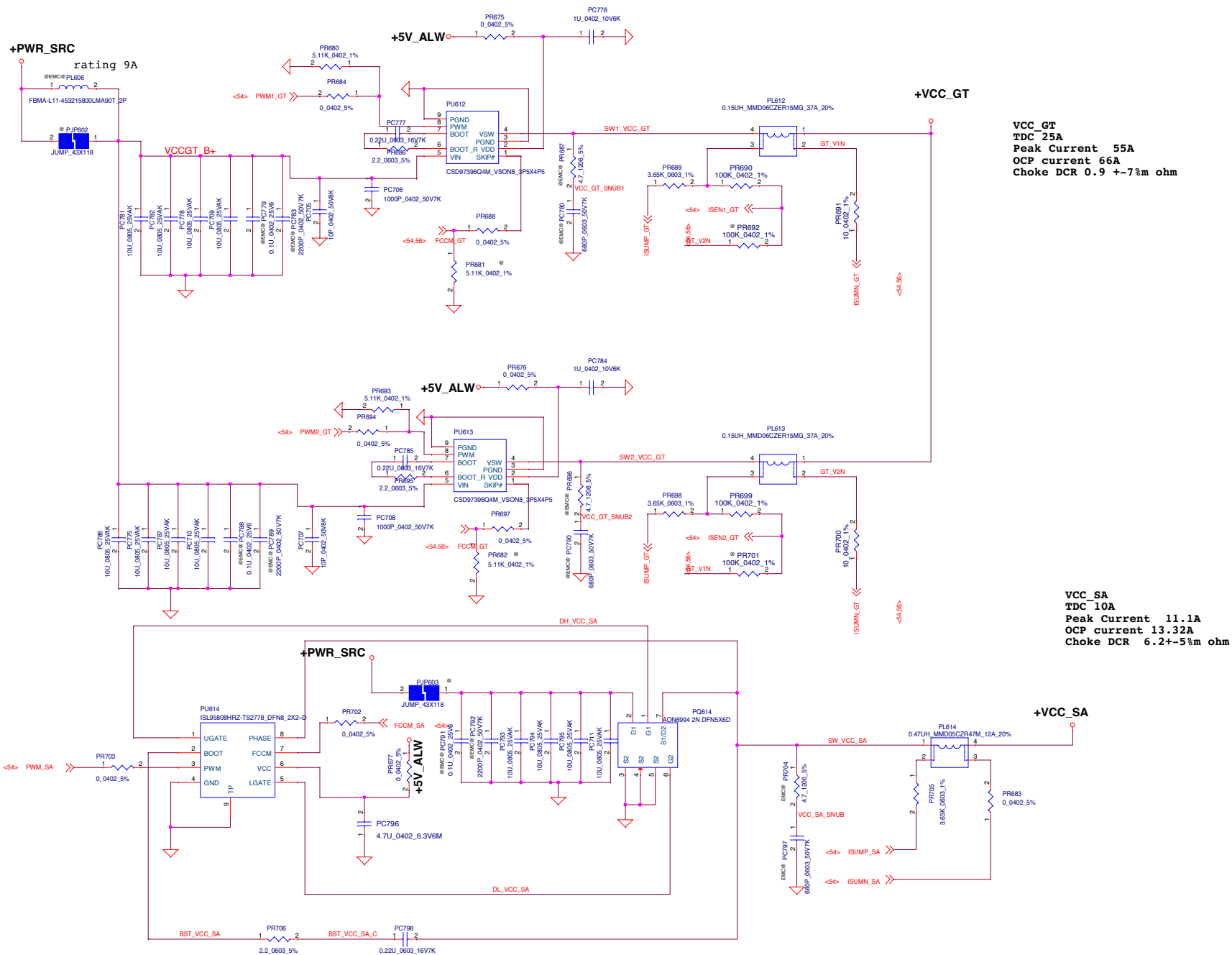
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VCC_core
TDC 50A
Peak Current 60A
OCP current 81.6A
Choke DCR 0.9 +-7% ohm





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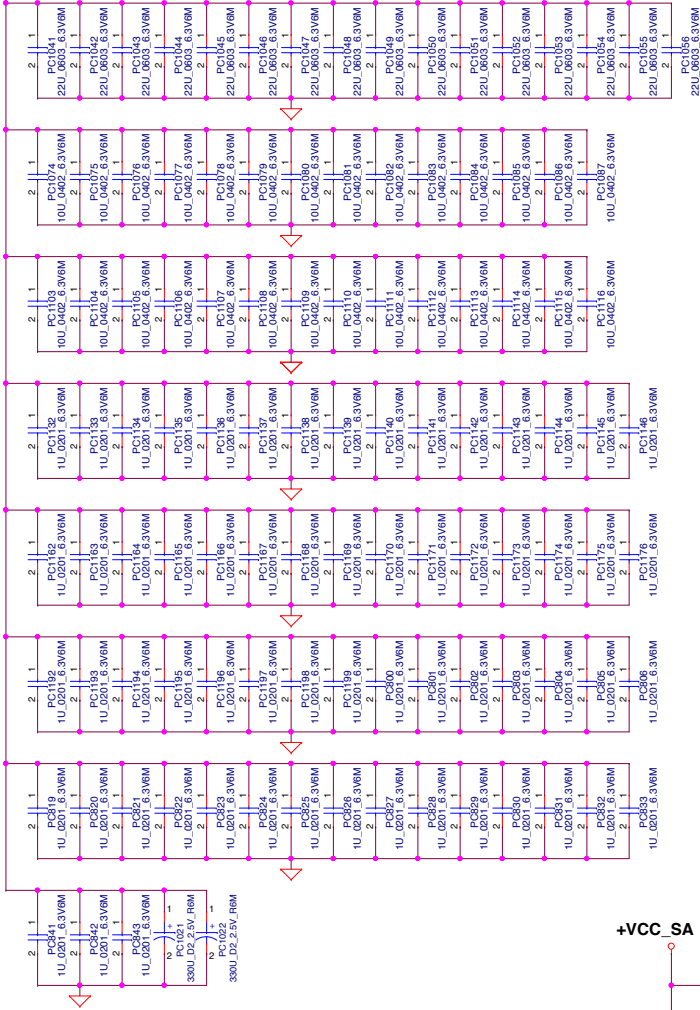
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Size	Document Number	Rev	
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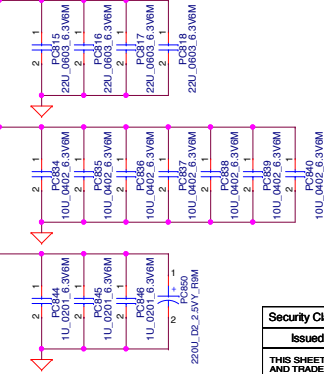
+VCC_CORE

VCC_CORE Place on CPU
Back Side.
22U_0603 * 8 pcs + 10U_0402*28 pcs + 1U_0201*35 pcs
Primary Side.
22U_0603 * 8 pcs+330u_D2*2 pcs



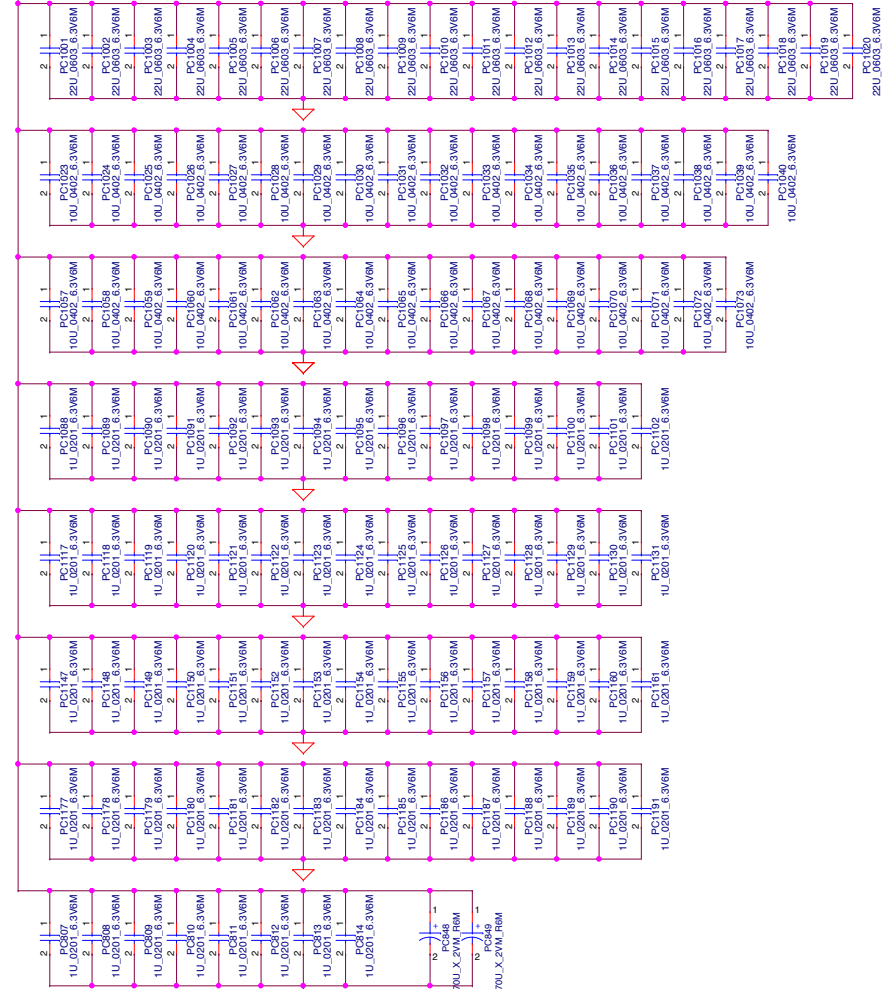
+VCC_SA

VCC_SA Place on CPU
Back Side.
22U_0603 * 2 pcs + 10U_0402*7 pcs + 1U_0201*3 pcs
Primary Side.
22U_0603 * 2 pcs + 220u_D2*1 pcs



+VCC_GT

VCC_GT Place on CPU
Back Side.
22U_0603 * 8 pcs +10U_0402*35 pcs +1U_0201*68 pcs
Primary Side.
22U_0603 * 12 pcs +470u_D2*2 pcs



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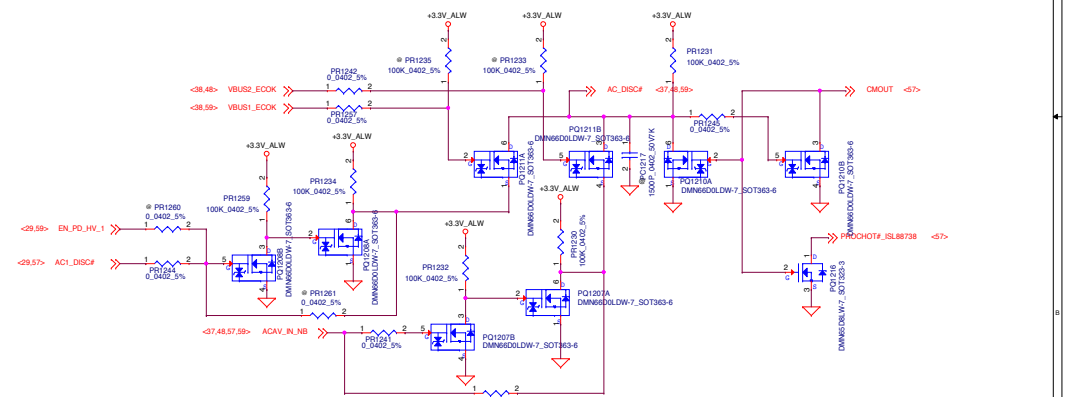
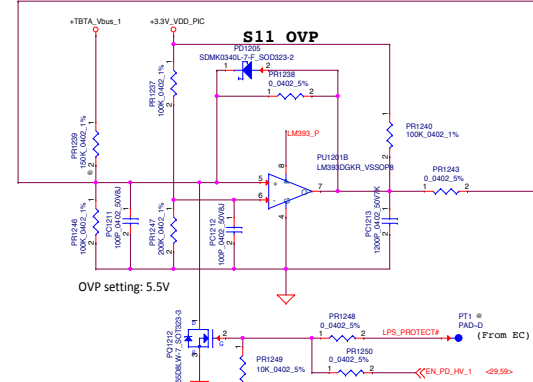
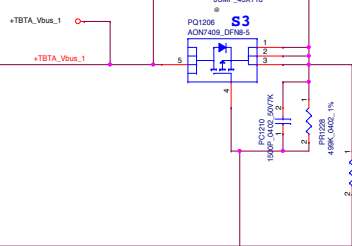
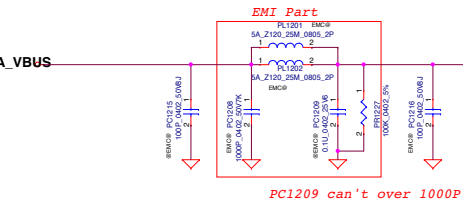
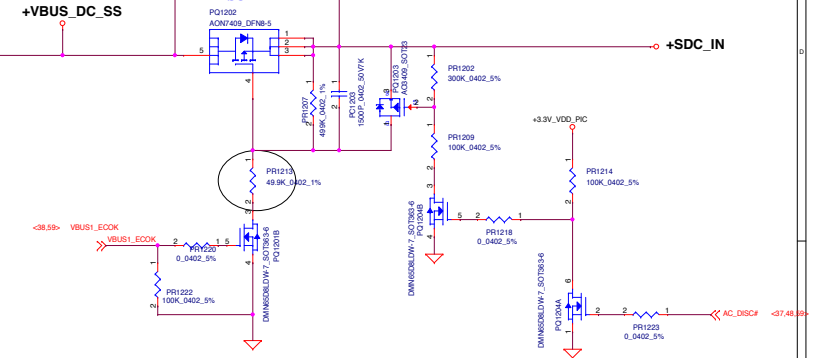
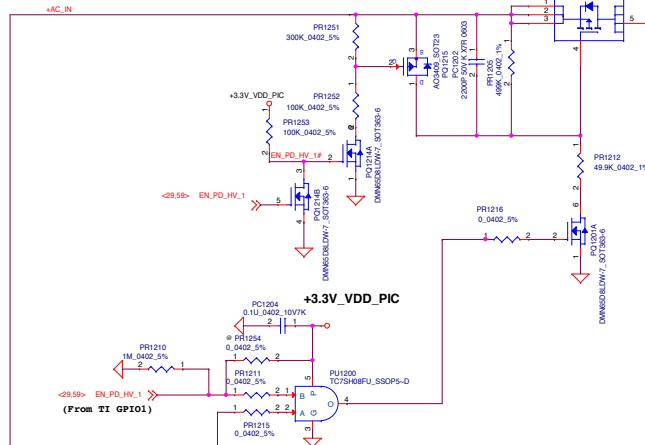
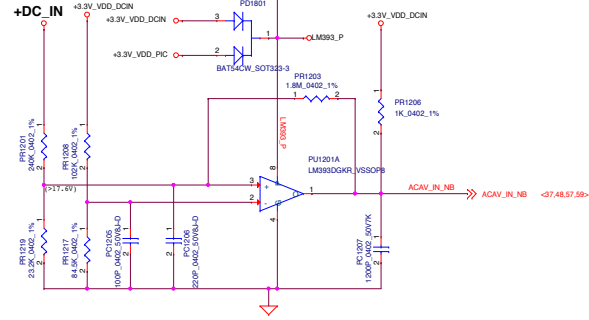
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PROCESSOR DECOUPLING

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DCIN_AC_Detector



Version Change List (P.J.R. List)				Issue		Solution		Rev.
Item	Page	Title	Date	Change	Description	Description	Description	
1	43	PHS, TCM, 10/1/2017	2017-10-01	PHS	Change solution version to the PHS Solution version	Change solution from 10.0.0.000 to 10.0.0.001		100
2	43	PHS, TCM, 10/1/2017	2017-10-01	PHS	Modify the software	PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002		100
3	43	PHS, TCM, 10/1/2017	2017-10-01	PHS	Modify the software	PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002		100
4	43	PHS, TCM, 10/1/2017	2017-10-01	PHS	Modify the software	PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002		100
5	43	PHS, TCM, 10/1/2017	2017-10-01	PHS	Modify the software	PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002		100
6	43	PHS, TCM, 10/1/2017	2017-10-01	PHS	Modify the software	PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002		100
7	43	PHS, TCM, 10/1/2017	2017-10-01	PHS	Modify the software	PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002		100
8	43	PHS, TCM, 10/1/2017	2017-10-01	PHS	Modify the software	PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002		100
9	43	PHS, TCM, 10/1/2017	2017-10-01	PHS	Modify the software	PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002		100
10	43	PHS, TCM, 10/1/2017	2017-10-01	PHS	Modify the software	PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002		100
11	43	PHS, TCM, 10/1/2017	2017-10-01	PHS	Modify the software	PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002		100
12	43	PHS, TCM, 10/1/2017	2017-10-01	PHS	Modify the software	PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002 PHS, TCM, 10/1/2017, 10.0.0.001 to 10.0.0.002		100

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	11	HW	2016/5/27	COMPAL	S0ix(modern standby) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)
2	37	HW	2016/5/27	COMPAL	Reserve PORT80_DET# PD resistance	Reserve RE513 100k (SD028100380) to GND	0.2(X01)
3	35	HW	2016/6/1	COMPAL	Intel schematics reivew modify item	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(0201) to 10uF_0603	0.2(X01)
4	39	HW	2016/6/1	COMPAL	TPM change to NUVOTON	Change TPM from Atmel to NUVOTON.	0.2(X01)
5	35	HW	2016/6/1	COMPAL	Intel reviwie result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
6	35	HW	2016/6/7	COMPAL	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
7	37	HW	2016/6/7	COMPAL	For MEC5105K-D1-TN setting	1. Change UE1 to SA00009GL00 2. POP RE360,RE362 3. De-POP RE361	0.2(X01)
8	35,32	HW	2016/6/16	COMPAL	For EMC request	De-pop RZ131, RZ132. CL22 change to 10pf , POP CA7,CZ1 (100P),CH268 modify from 22p to 47p and POP,Change LV1 to SM01000NY00	0.2(X01)
9	41	HW	2016/6/16	COMPAL	BITS284924-HDD is still working after press power button into S5 during POST.	POP RN5	0.2(X01)
10	39	ME	2016/6/17	COMPAL	Connector change	1. JKBTP1 change to CVILU CF5020FD0RK-05-NH 2. JUSH1 change to CVILU CF5026FD0RK-05-NH 3. JIR1 change to ACES_50208-0060N-P01	0.2(X01)
11	36	HW	2016/6/20	COMPAL	Vender suggest	RA7,RA8 change to 16.2ohm	0.2(X01)
12	37	HW	2016/6/22	COMPAL	The possibility of GPIO map update	Add RE514,RE515 for RTCRST_ON	0.2(X01)
13	41	HW	2016/6/22	COMPAL	BITS283552 - [BR_CSLP] FFS AP no function when execute FF generator or shake SU	FFS VDD_IO change to +3.3V_RUN	0.2(X01)

Security Classification		Compal Secret Data		TITLE Compal Electronics, Inc.	
Issued Date	2016/01/01	Deciphered Date	2017/01/01	Title EE P.I.R (1/6)	
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