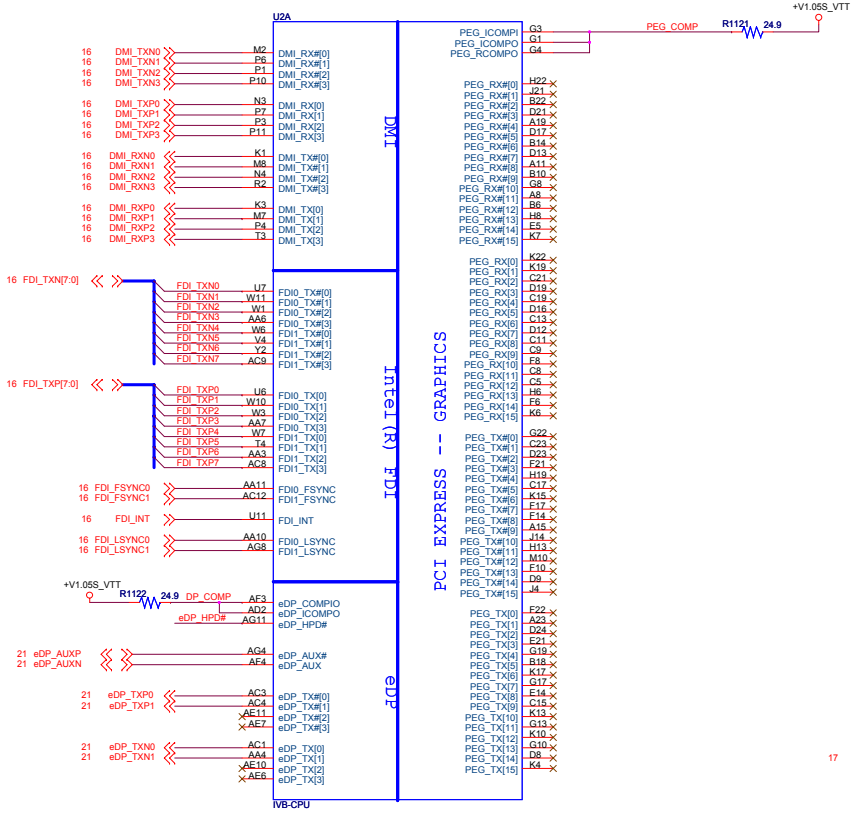
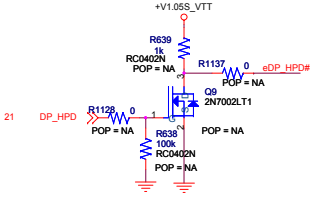
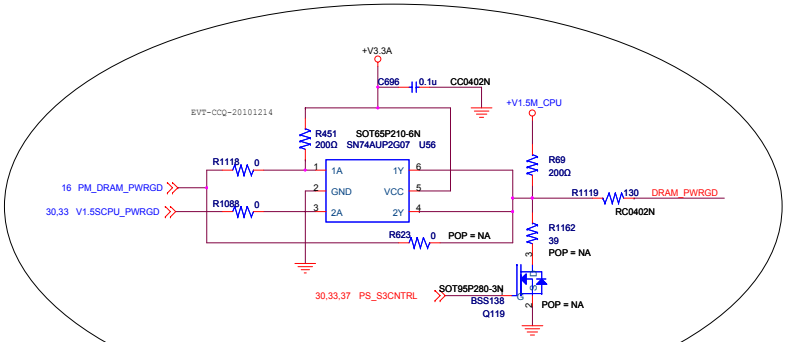
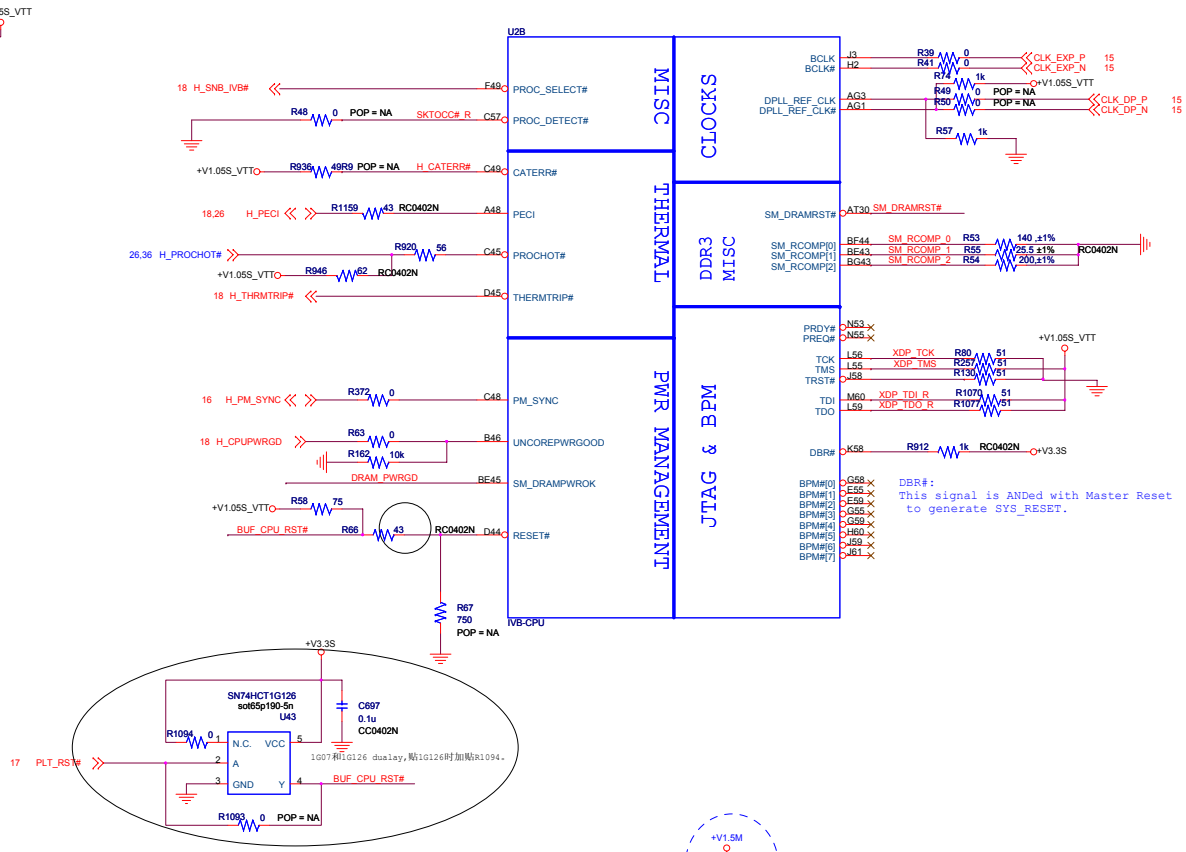
CAD NOTE: PEG_ICOMPI and RCOMPO signals
should be shorted and routed with
- max length = 500 mils
- typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 mohms

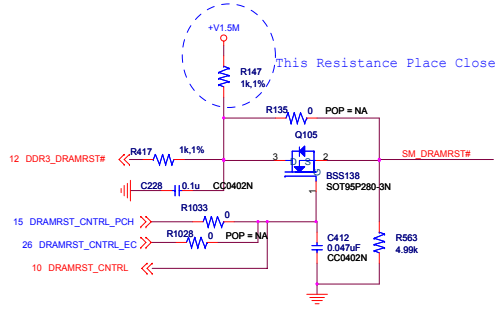


CAD NOTE: DP_COMPIO and ICOMPO signals
should be shorted near balls and routed with
- typical impedance < 25 mohms









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	Title <Title>		
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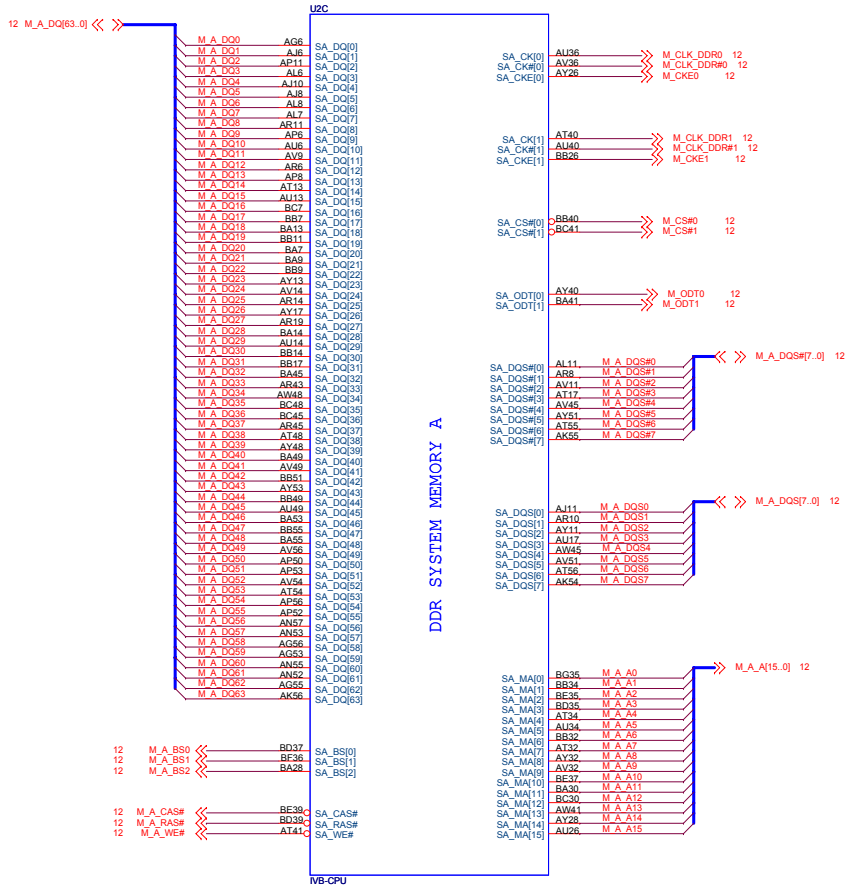
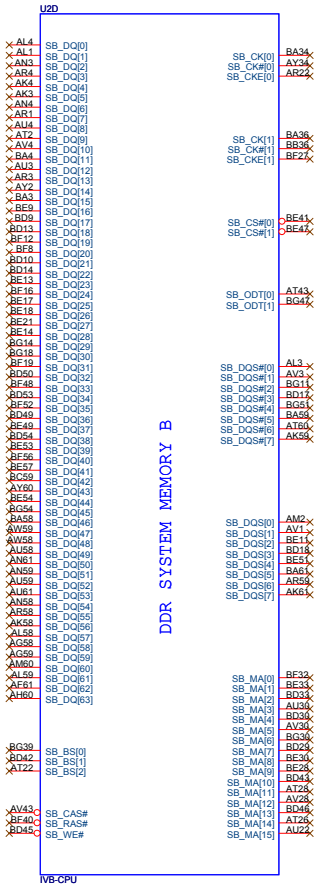
	Date: Thursday, February 16, 2012	Sheet 6 of 38	





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Title <Title>

Size	Sheet Name	Rev
C	CPU2	A

ENGINEER: Wain

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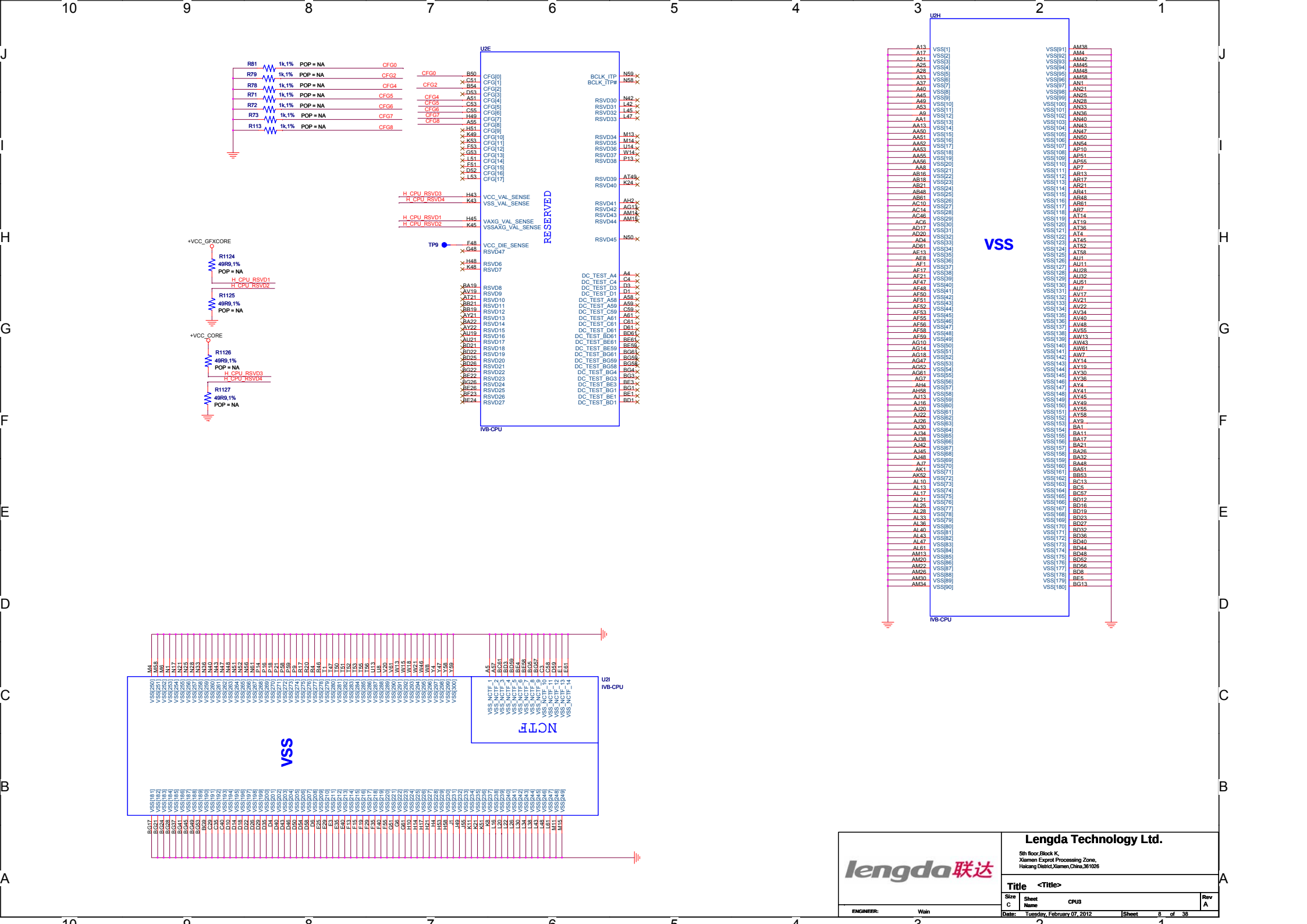

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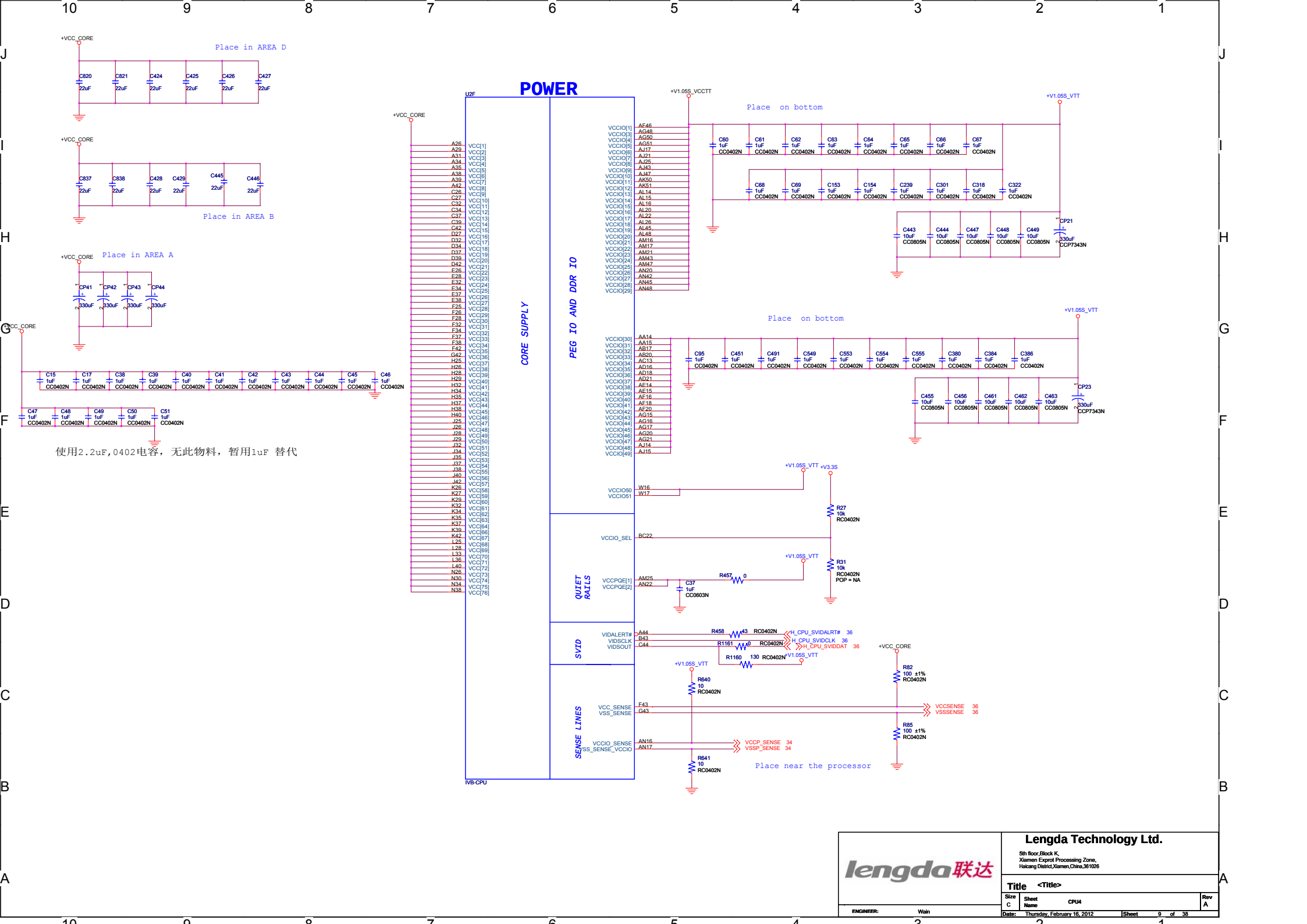
Title	<Title>
Size C	Sheet Name CPU3
Rev A	
ENGINEER: Wain	
Date: Tuesday, February 07, 2012	Sheet 8 of 38


POWER
U2F
CORE SUPPLY
PEG IO AND DDR IO
QUIET RAILS
SVID
SENSE LINES
iVB-CPU
Place in AREA D
Place in AREA B
Place in AREA A
Place on bottom
Place on bottom
Place near the processor
+VCC_CORE
+V1.05S_VCCTT
+V1.05S_VTT
+V3.3S
使用2.2uF,0402电容，无此物料，暂用1uF 替代
Lengda Technology Ltd.
5th floor,Block K,
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Haicang District,Xiamen,China,361026
Title <Title>
Size C
Sheet Name CPU4
Rev A
ENGINEER: Wain
Date: Thursday, February 16, 2012
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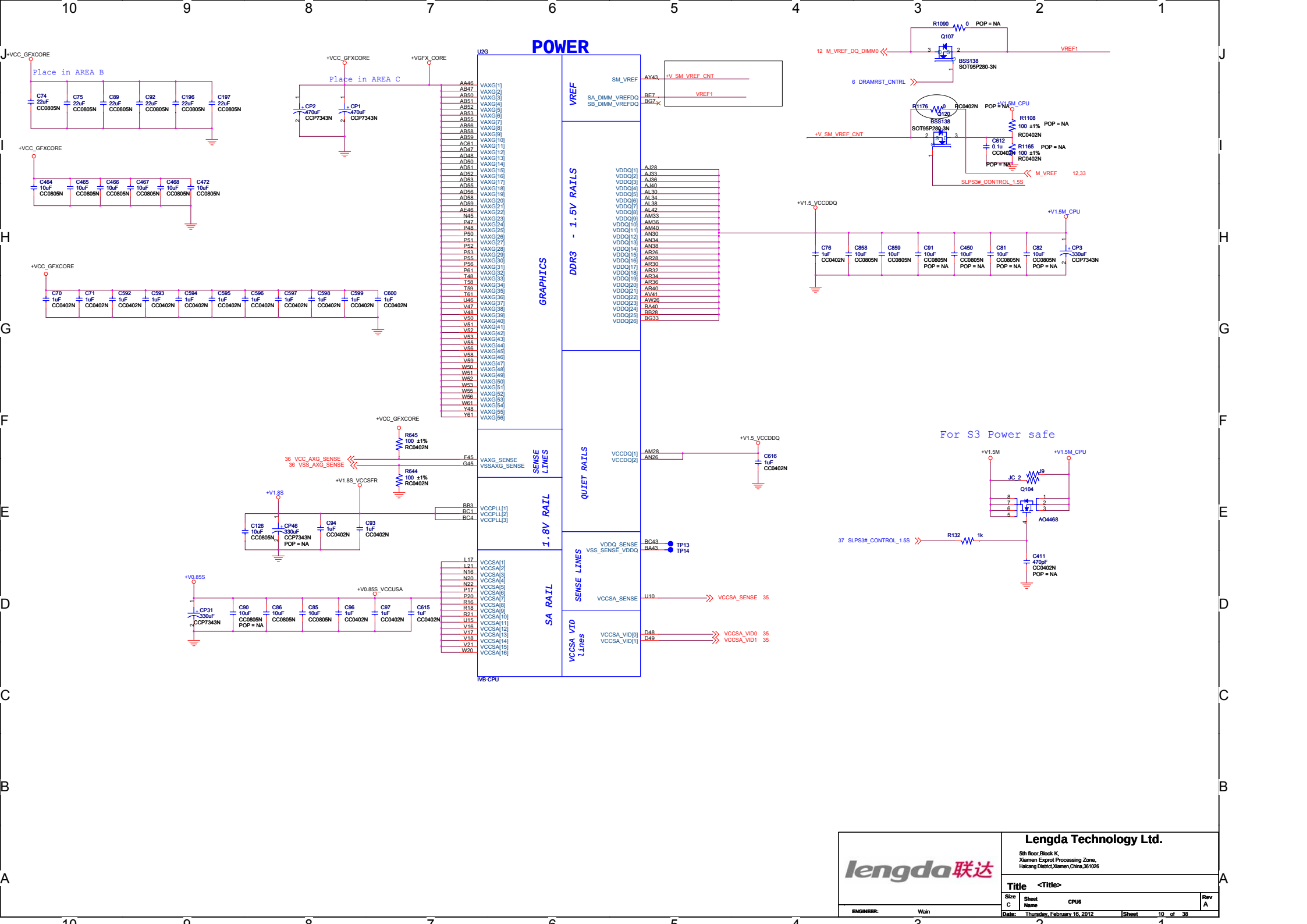
POWER



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5th floor,Block K,
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Title <Title>

Size	Sheet Name	Rev
C	CPU6	A

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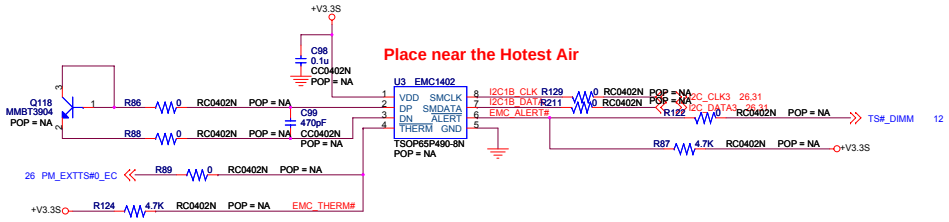
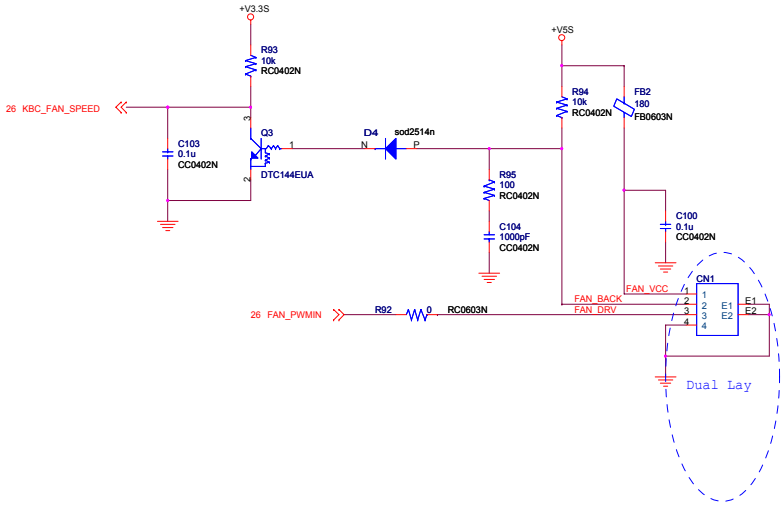
Thermal Sensor



CPU FAN Control



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Title	<Title>
Size C	Sheet Name THERMAL
Rev A	
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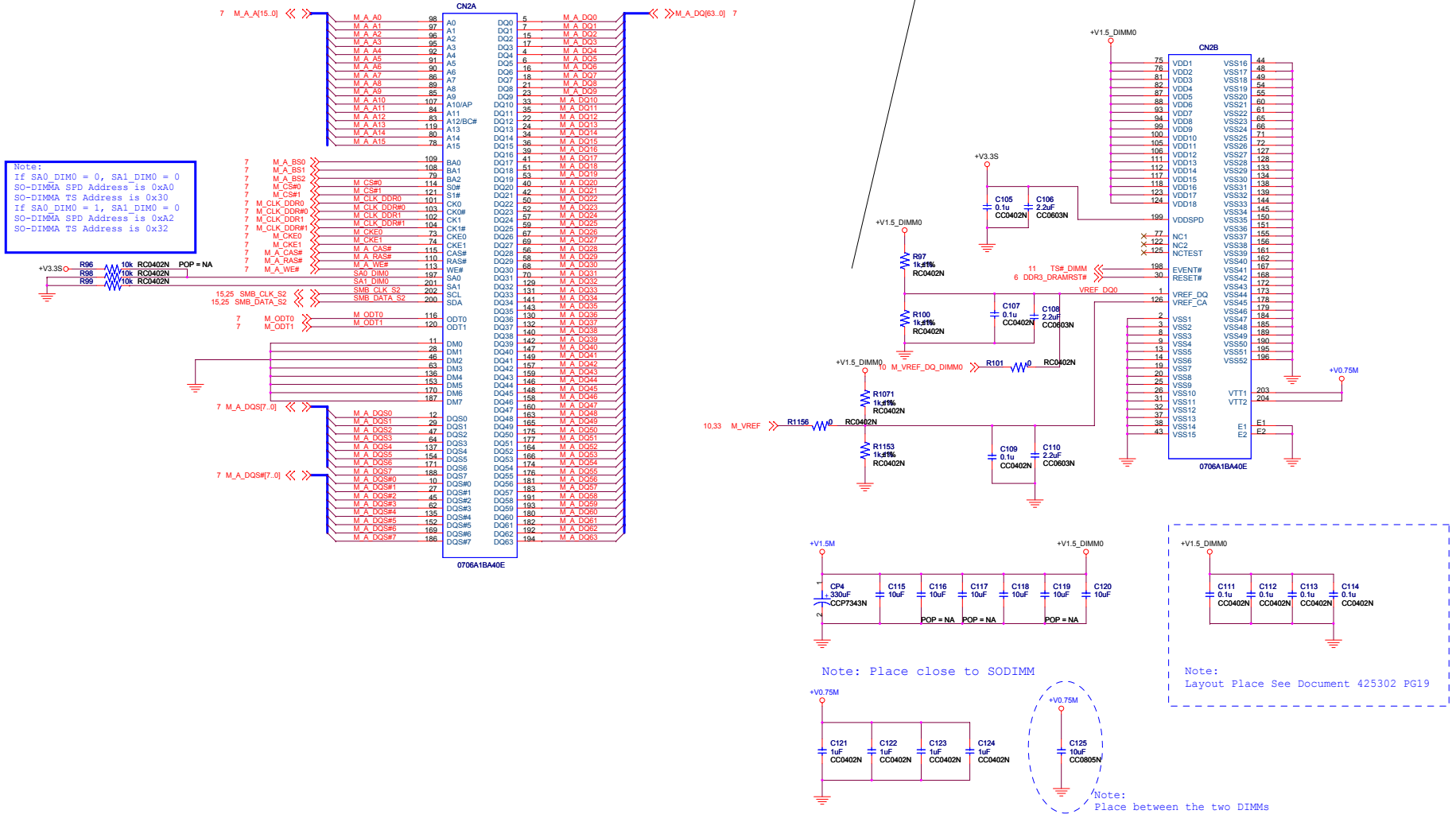
DDR3 SODIMM0



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Title <Title>

Size	Sheet Name	Rev
C	DDR3_SODIMM0	A

ENGINEER: Wain

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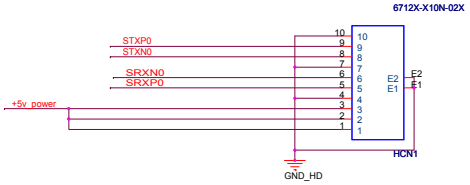
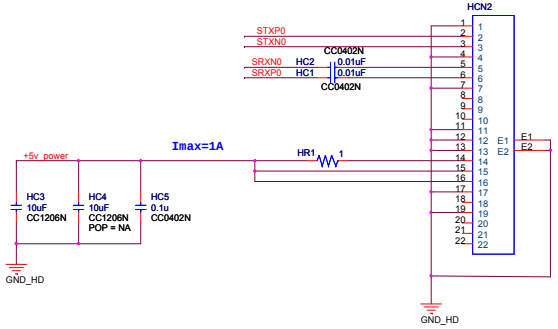
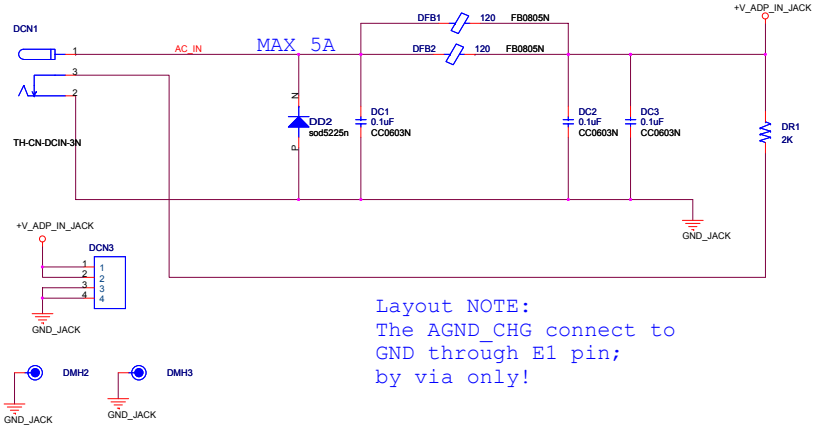
HDD CONN



HDD CONN



ADP_IN



Layout NOTE:
The AGND_CHG connect to
GND through E1 pin;
by via only!

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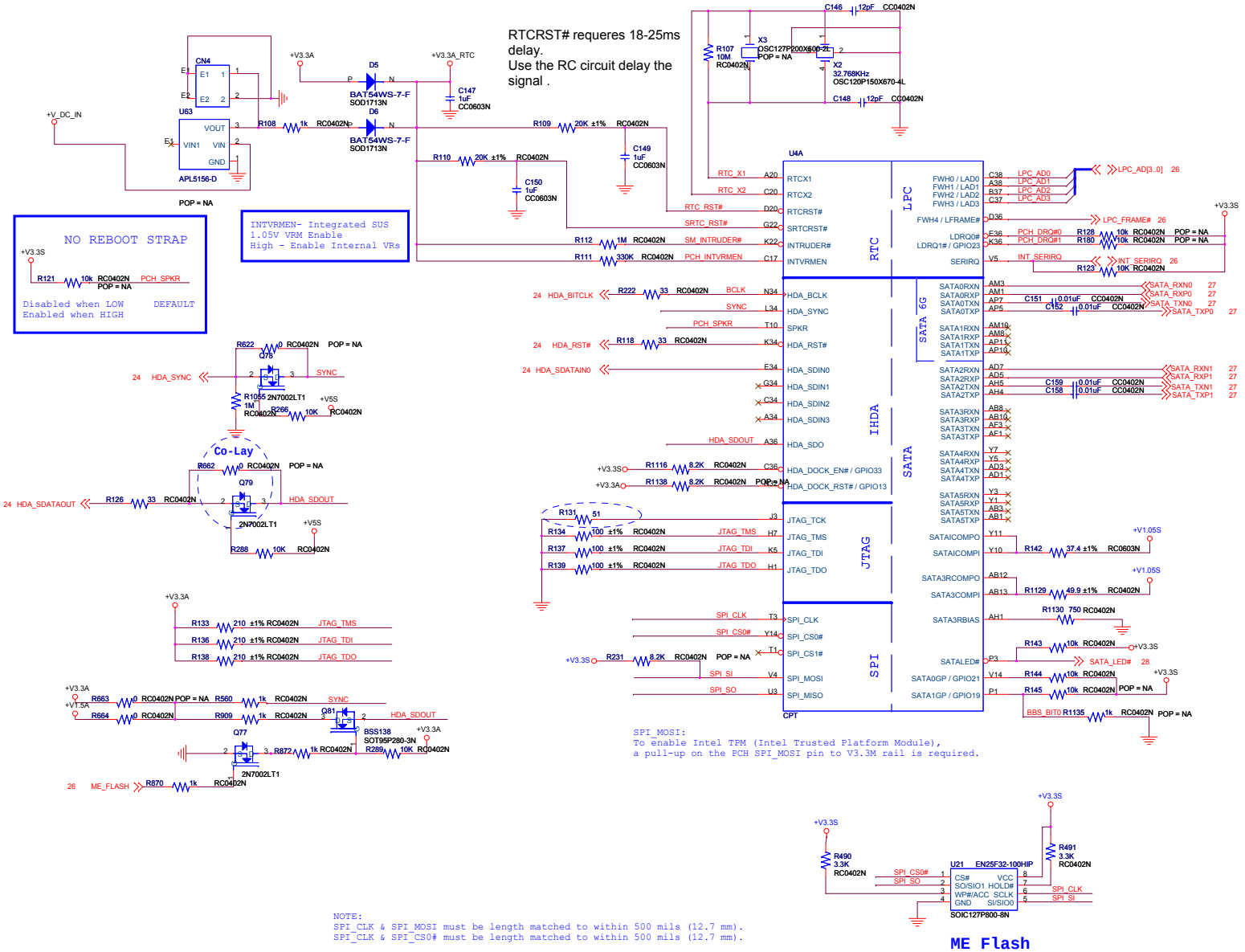
	Title <Title>		
	Size C	Sheet Name DDR3_SODIMM1	Rev A
	Date: Tuesday, February 07, 2012	Sheet 13 of 38	



GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. It has a weak internal pull-up. When GPIO33 is sampled low, the Flash Security gets overridden as well as Intel ME gets halt. This signal should be only asserted low through an external pull-down (1 kW ±5%) in manufacturing or debug environments ONLY.

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Title <Title>		
Size C	Sheet Name PCH1	Rev A
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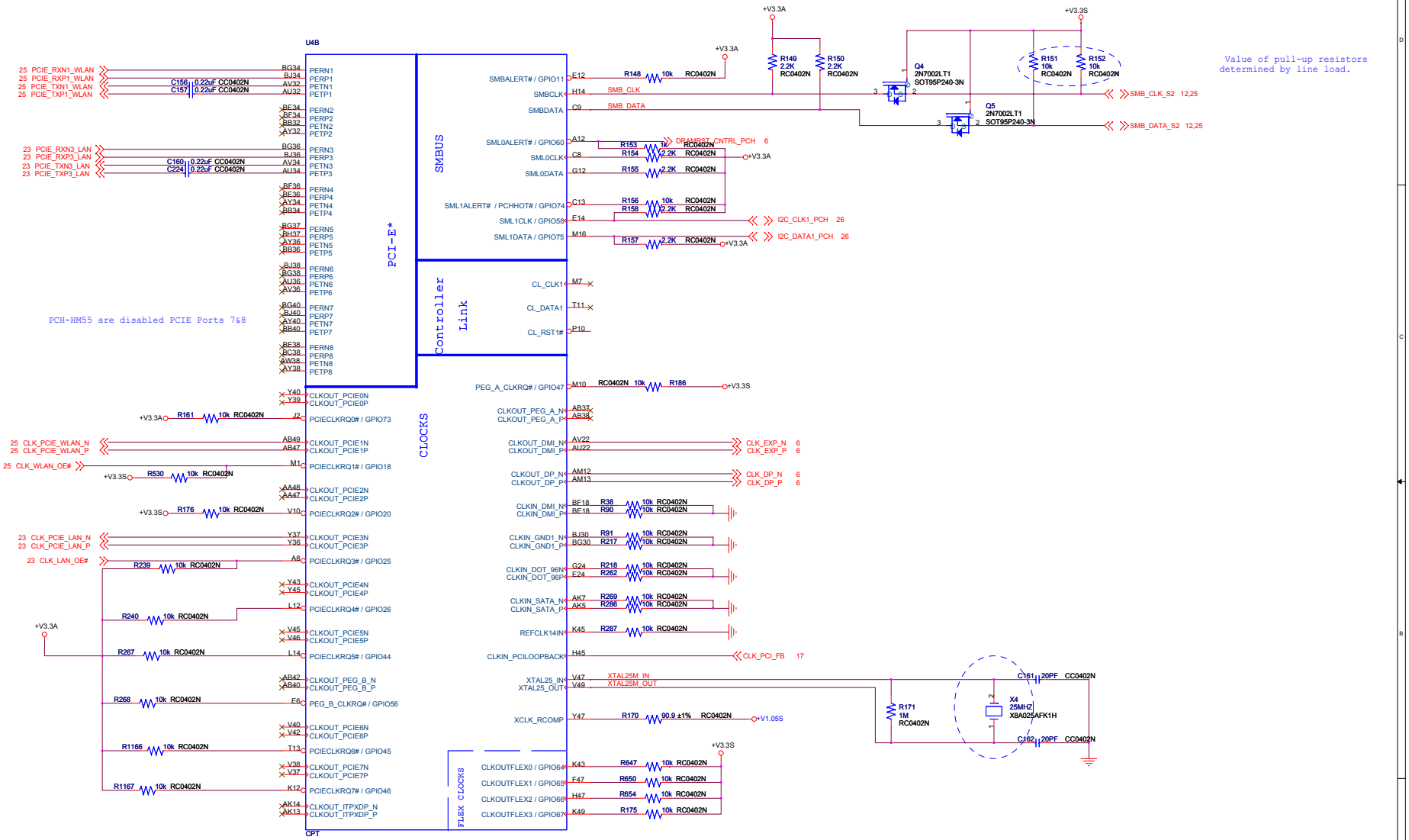

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Title <Title>

Size	Sheet Name	Rev
C	PCH2	A

ENGINEER: Wain

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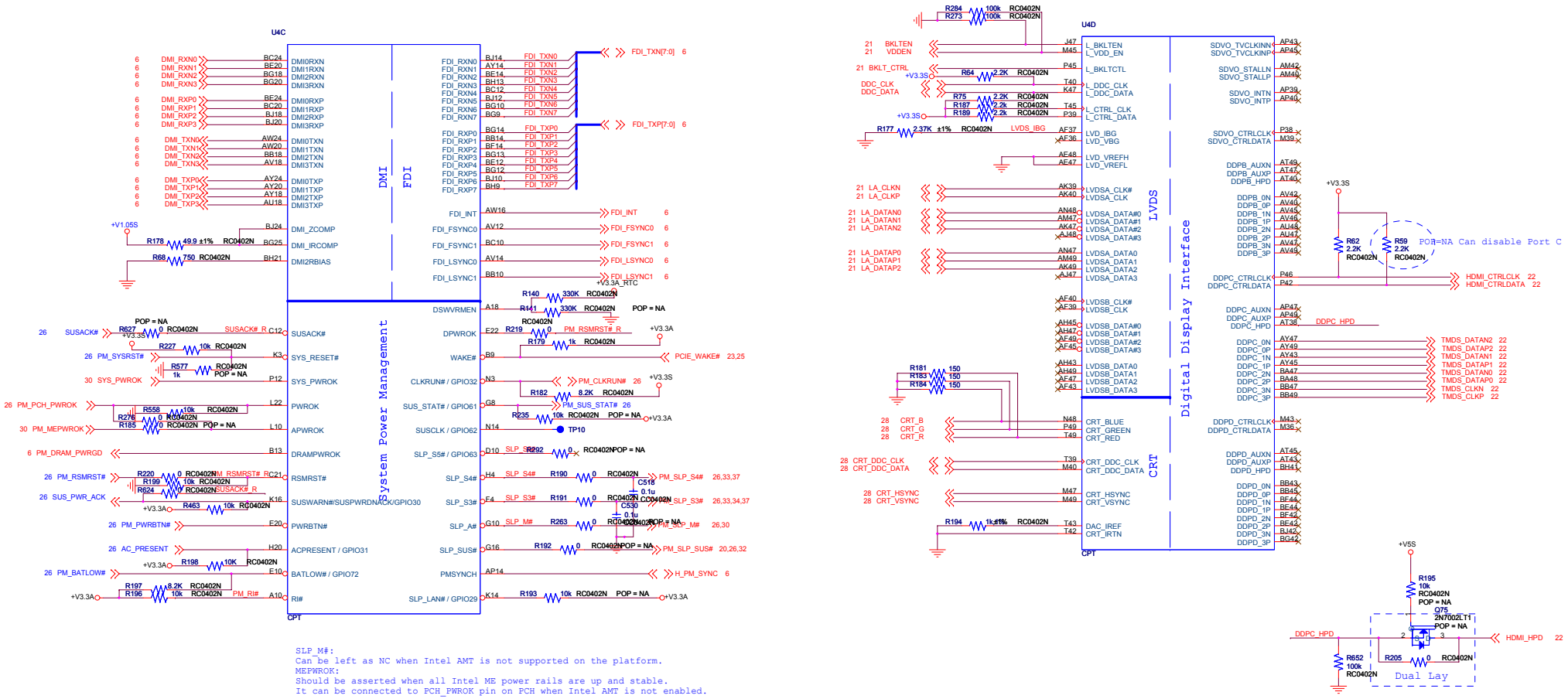

SLP_M#:
Can be left as NC when Intel AMT is not supported on the platform.
MEPWROK:
Should be asserted when all Intel ME power rails are up and stable.
It can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.

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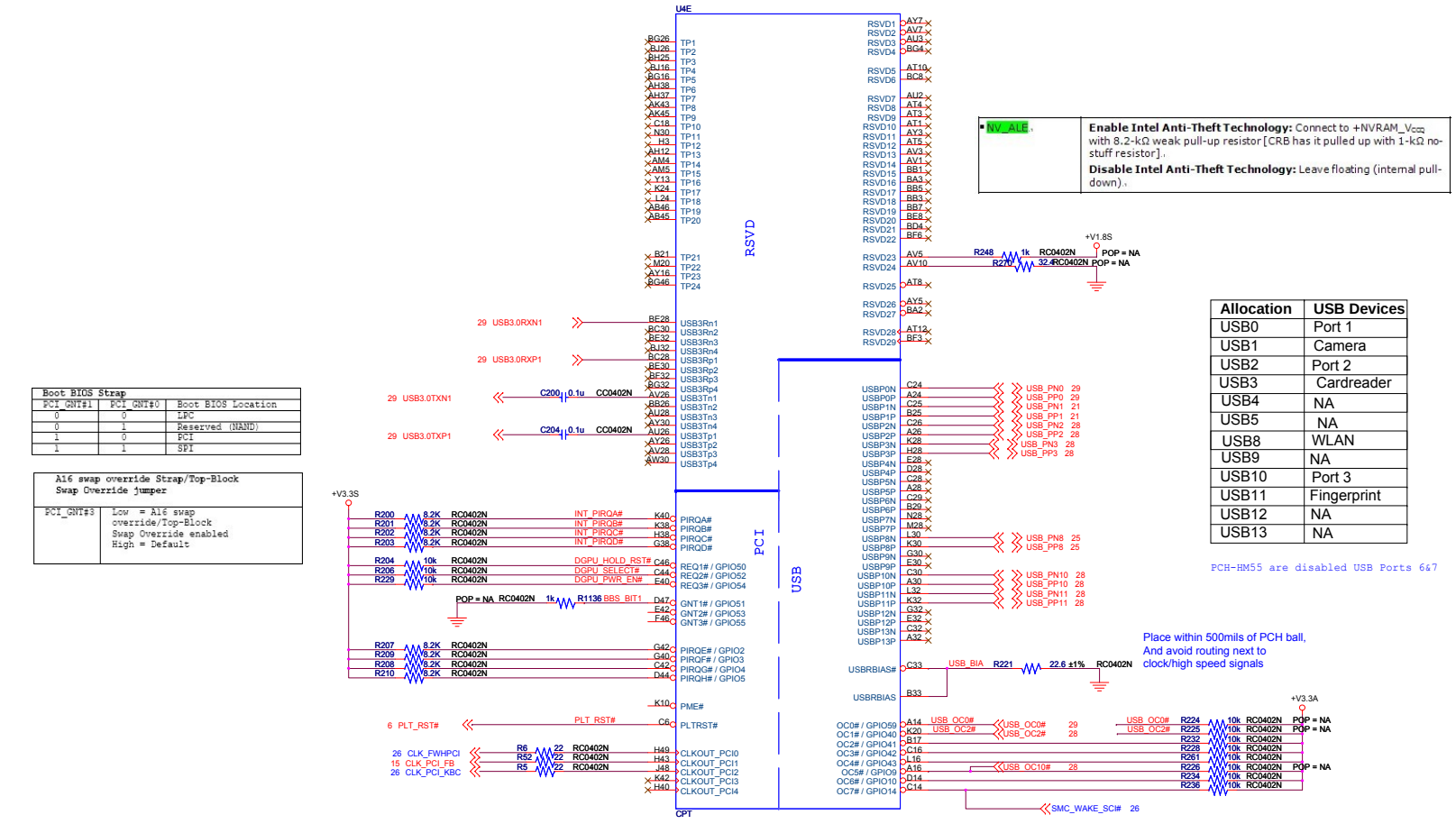
Title <Title>

Size	Sheet Name	Rev
C	PCH3	A

ENGINEER: Wain

Date: Thursday, February 16, 2012 Sheet 16 of 38



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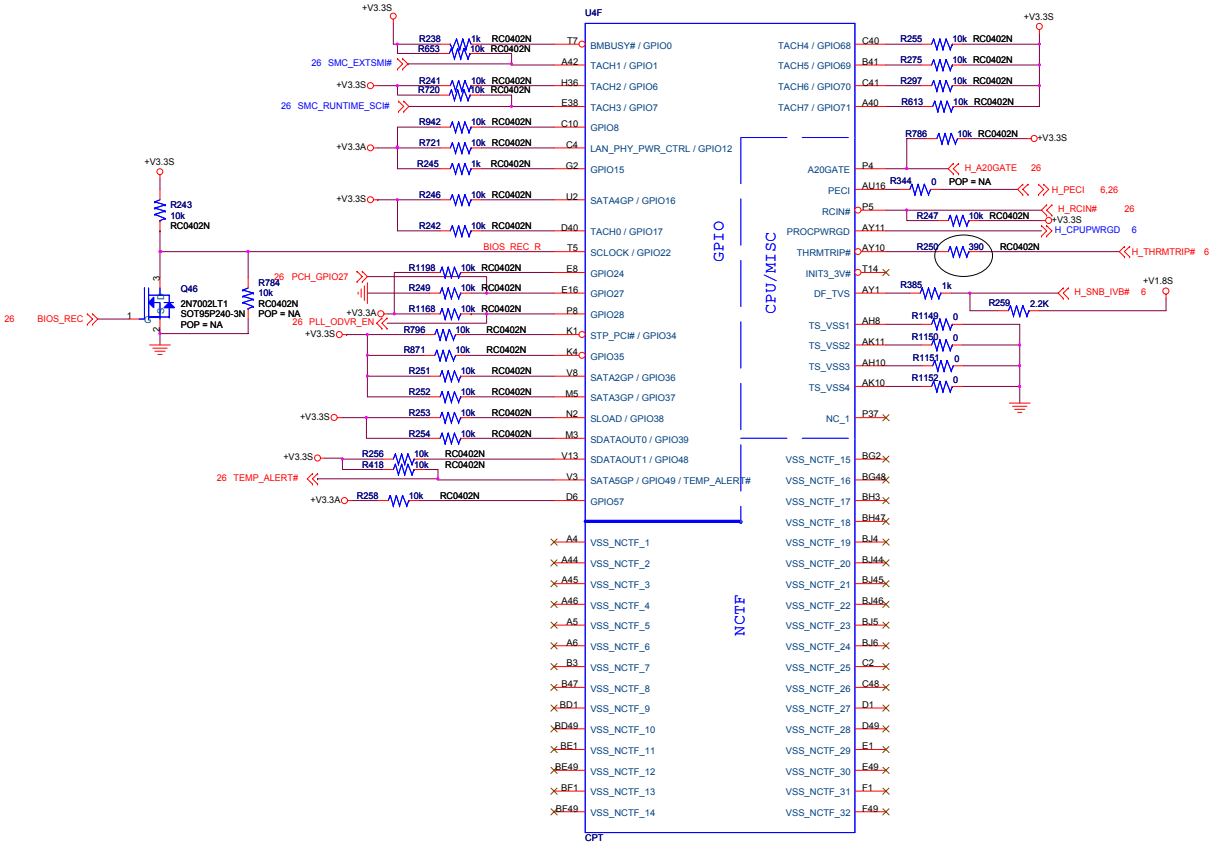
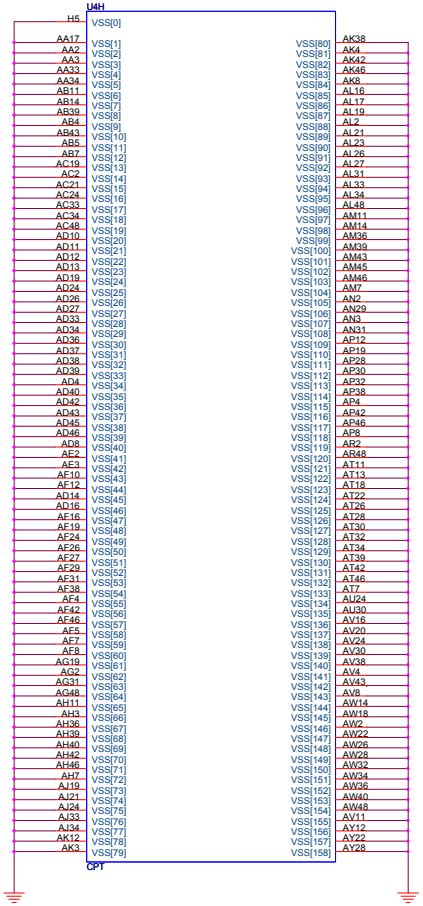
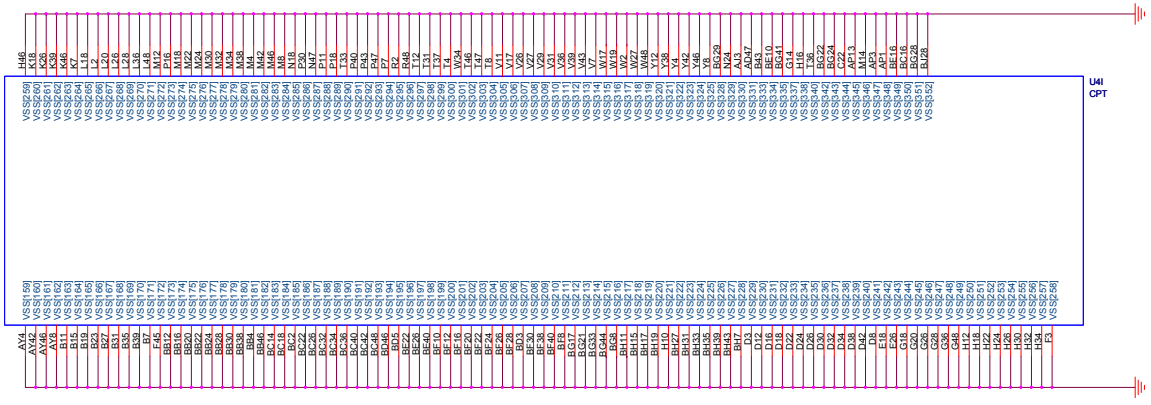
Size: C	Sheet Name: PCH4
Rev: A	
ENGINEER: Wain	Date: Monday, February 27, 2012
Sheet 17 of 38	







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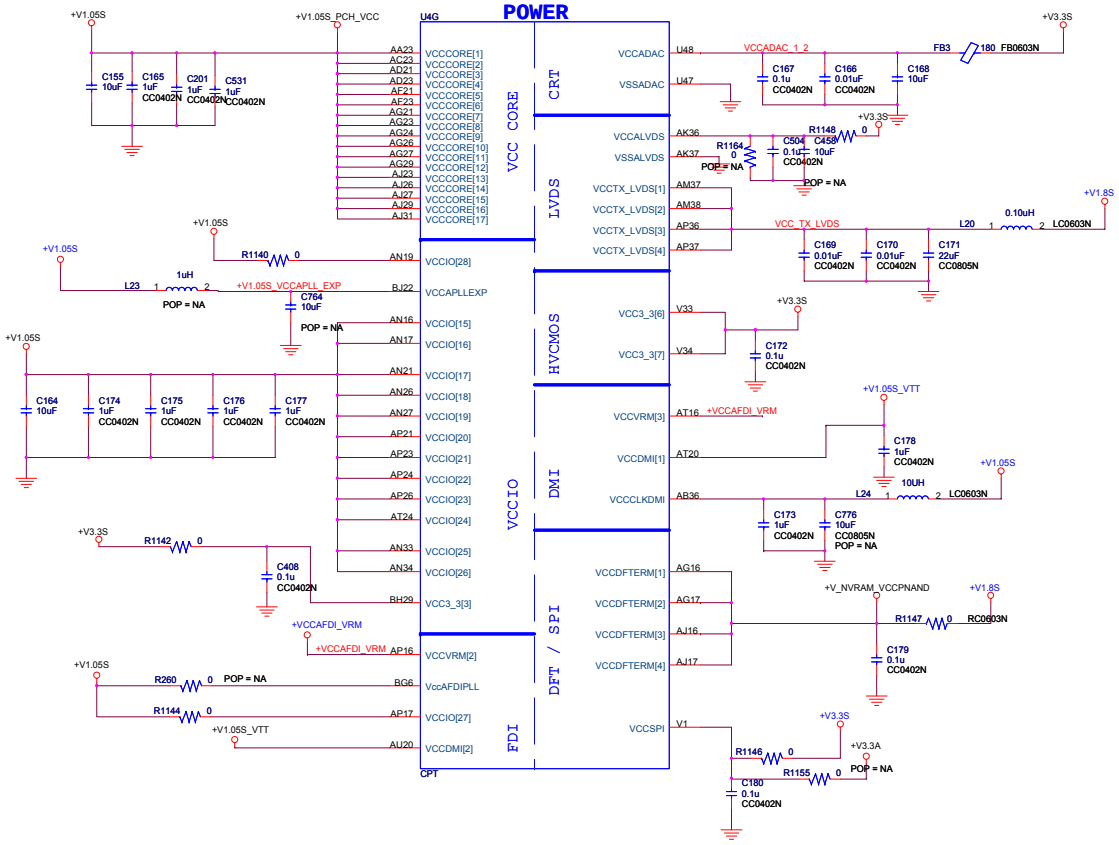
Title	<Title>		
Size C	Sheet Name PCH5		Rev A
ENGINEER: Wain	Date: Thursday, February 16, 2012	Sheet 18 of 38	



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5th floor,Block K,
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Title <Title>

Size	Sheet Name	Rev
C	PCH6	A

ENGINEER: Wain

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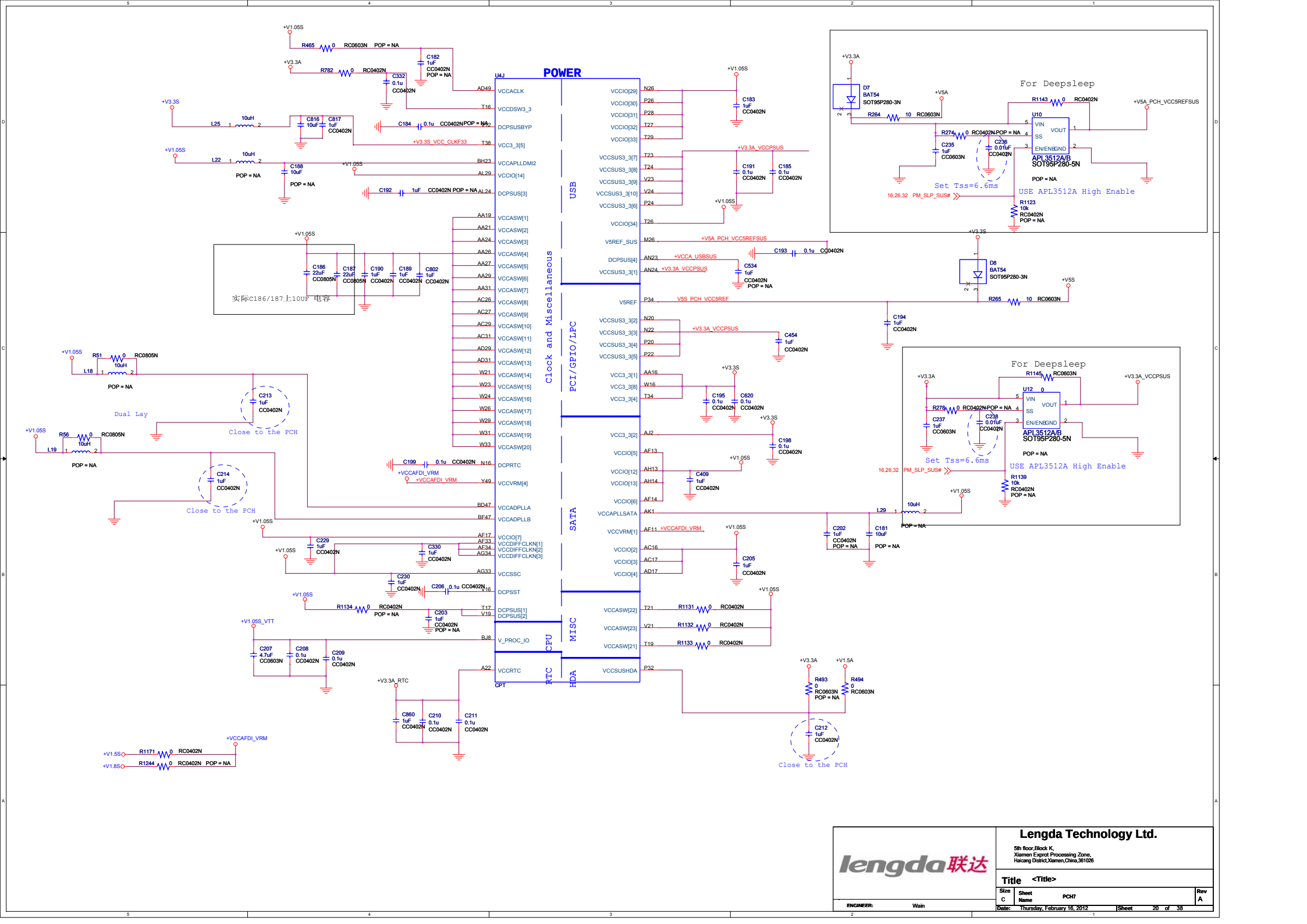
POWER
U4J
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
CPT
For Deepsleep
APL3512A/B
SOT95P280-5N
USE APL3512A High Enable
Set Tss=6.6ms
Close to the PCH
Dual Lay
实际C186/187上10uF 电容
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5th floor,Block K,
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Title <Title>
ENGINEER: Wain
Sheet Name PCH7
Date: Thursday, February 16, 2012
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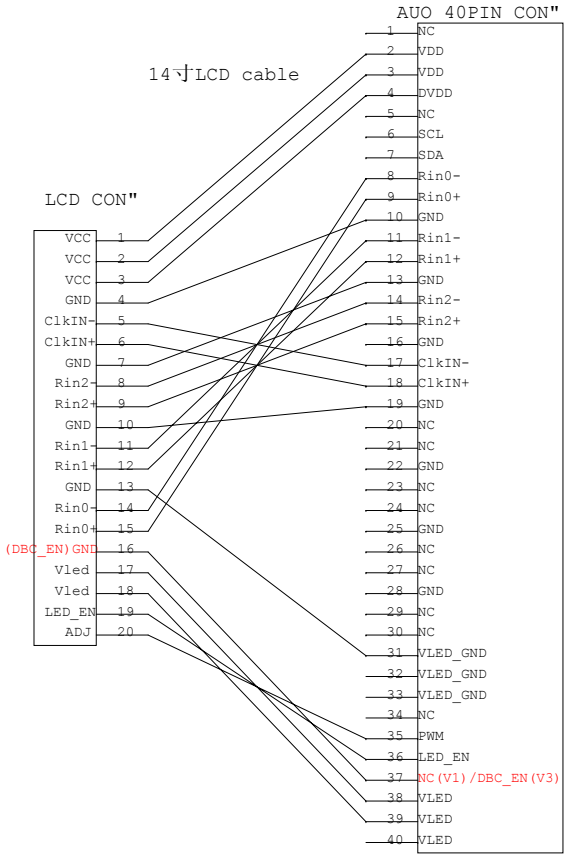
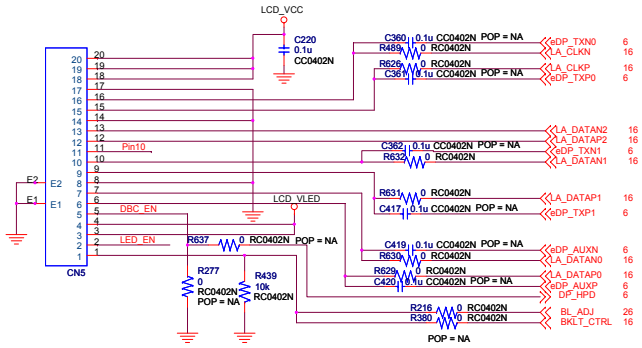
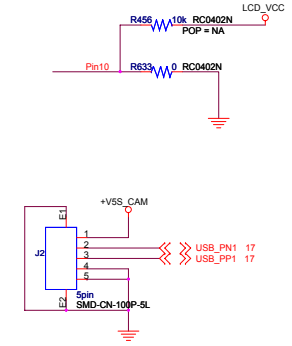
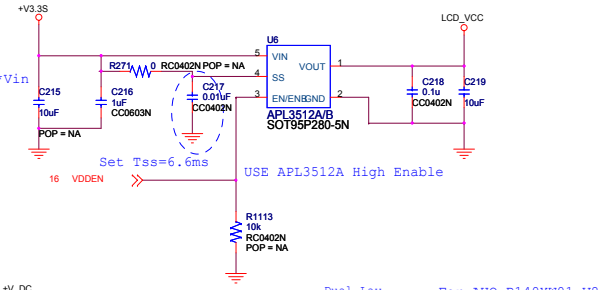
LVDS Connector

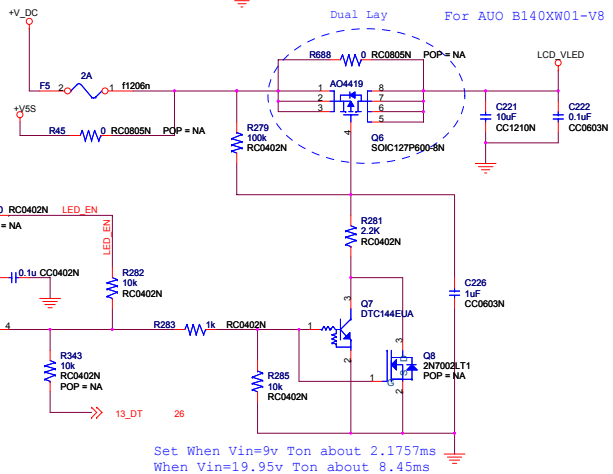


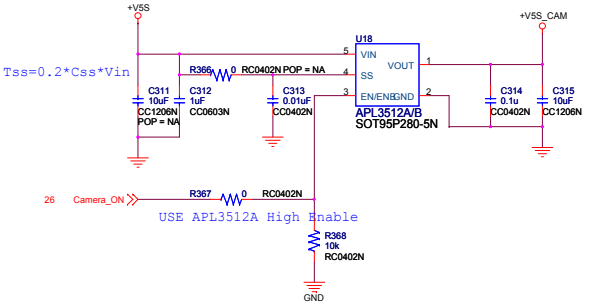


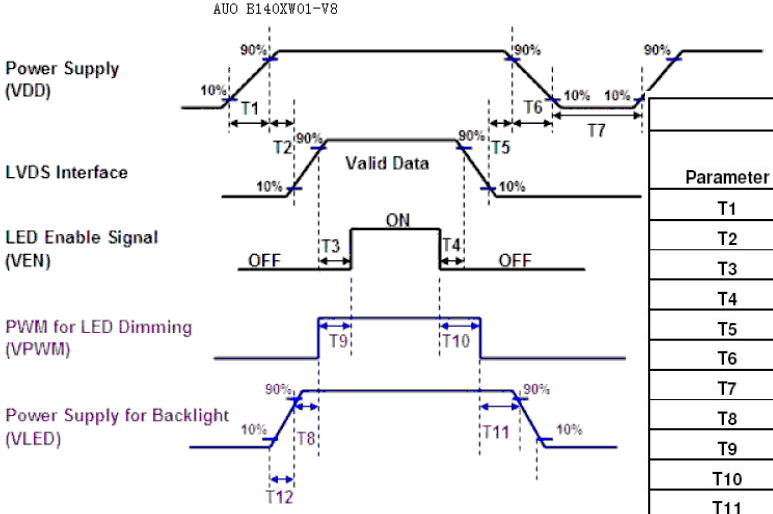


PIN1 to PIN1 Dual Lay









Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	50	
T3	200	-	-	
T4	200	-	-	
T5	10	-	50	
T6	0	-	10	
T7	500	-	-	
T8	10	-	-	
T9	10	-	180	
T10	10	-	180	
T11	10	-	-	
T12	0.5	-	10	

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5th floor,Block K,
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Haicang District,Xiamen,China,361026

Title <Title>

Size	Sheet Name	Rev
C	LCD CONN	A

ENGINEER: Wain

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NOTE:
Place one capacitor for two power pins.

Changed SDA and SCL Pull up on CPU side

From Chipset or Gfx

NOTE:
PS8101 4 pairs of TMDS input pins(IN_Dx+/IN_Dx-) are identical
So TMDS CLK+/- and Datax+/- can be connected freely to any pair of TMDS input pins
Also positive and negtive can be swapped for each pair TMDS input pins

It's the same for PS8101 4 pairs of TMDS output pins

U11 SN75DP139

Recommended Equalization: [PC1,PC0]=01, 4dB

For PS8101 Value=499ohm
For SN75DP139 Value=4.02kohm

U44 TPD8S009
For HDMI ESD
Place as close to the HDMI CONN as possible

CN6 HDMI Source Receptacle Connector

Layout Note: Place these Resistors close to HDMI CONN

HDMI Pull Downs

1920x 1200 @ 60 Hz using HDMI

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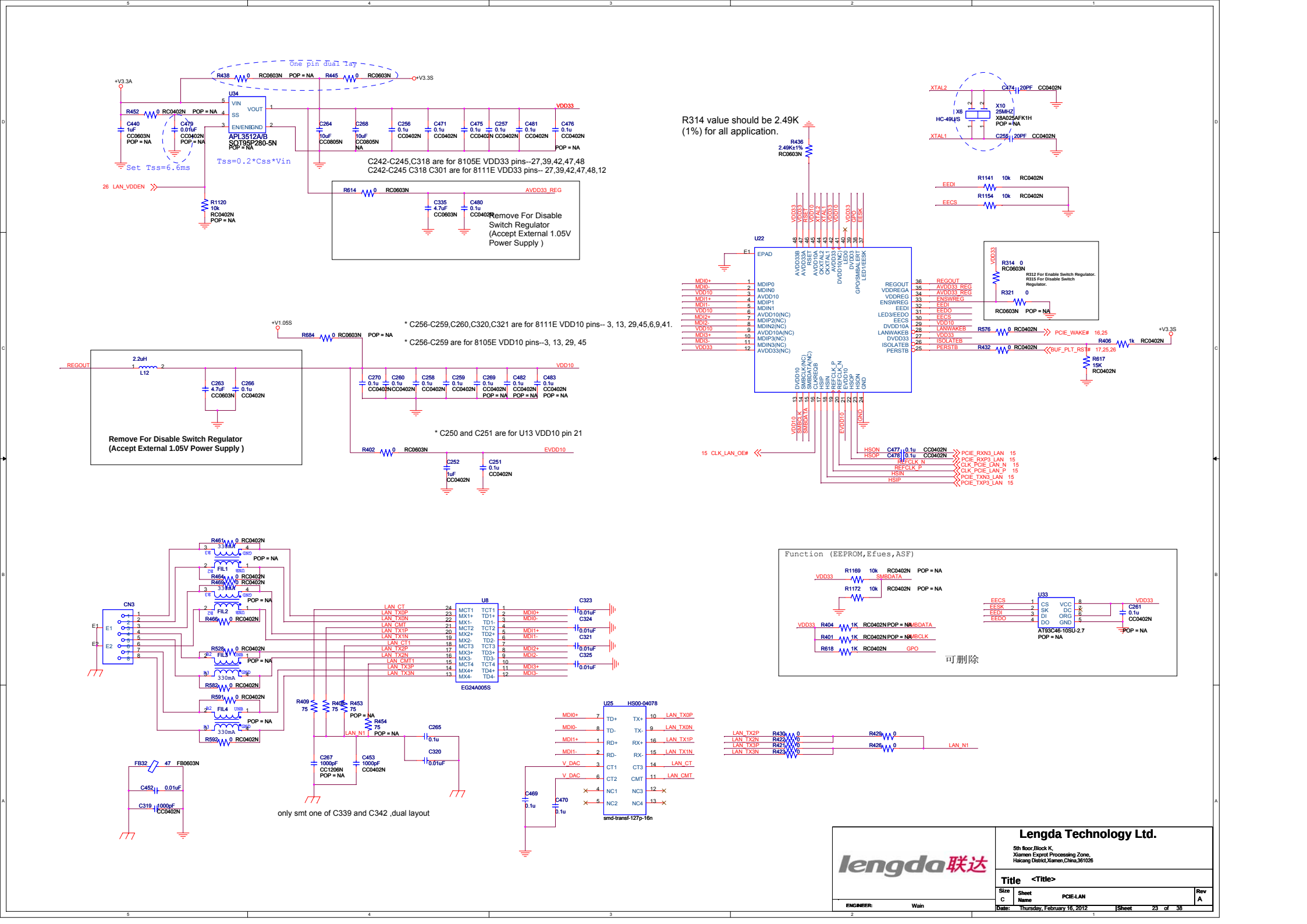
Title	<Title>
Size C	Sheet Name HDMI Port
Rev A	
ENGINEER: Wain	Date: Thursday, February 16, 2012 Sheet 22 of 38



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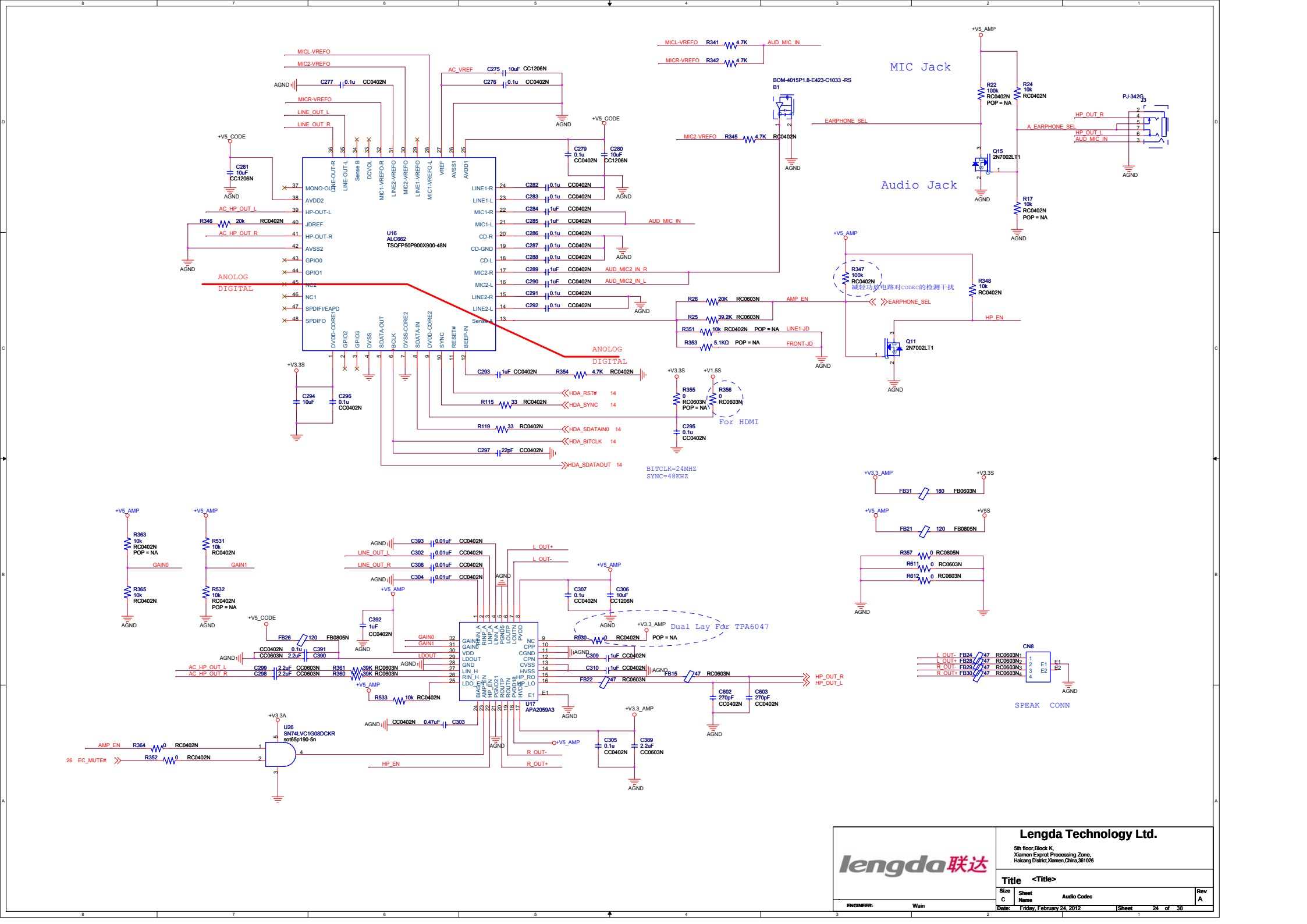
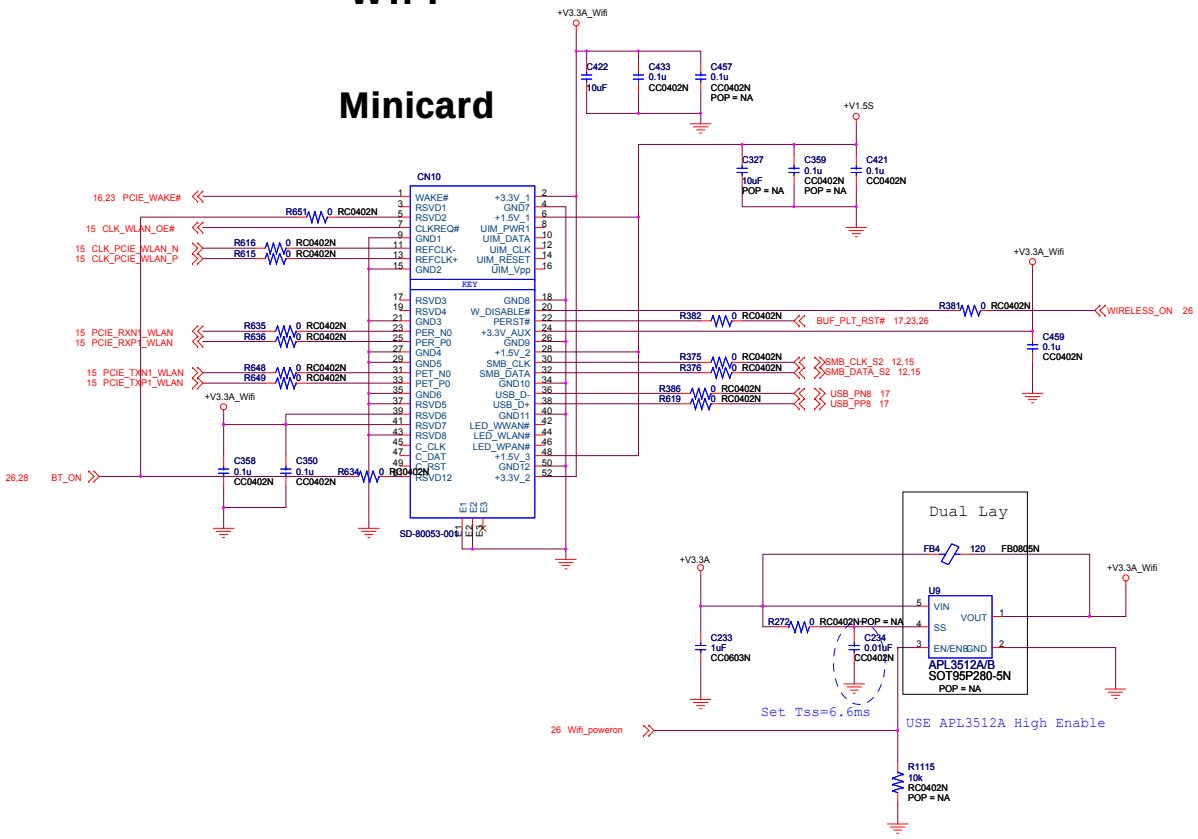
5th floor,Block K, Xiamen Exprol Processing Zone, Haicang District,Xiamen,China,361026		
Title	<Title>	
Size C	Sheet Name PCIE-LAN	Rev A
ENGINEER: Wain	Date: Thursday, February 16, 2012	Sheet 23 of 38


MIC Jack
Audio Jack
U16
ALC662
TSQFP50P900X900-48N
ANOLOG
DIGITAL
U17
APA2059A3
U26
SN74LVC1G08DCKR
SOT65P190-5N
Dual Lay For TPA6047
For HDMI
BITCLK=24MHZ
SYNC=48KHZ
SPEAK CONN
减轻功放电路对CODEC的检测干扰
Lengda Technology Ltd.
5th floor,Block K,
Xiamen Exprot Processing Zone,
Haicang District,Xiamen,China,361026
Title <Title>
Audio Codec
ENGINEER: Wain
Friday, February 24, 2012
Sheet 24 of 38

WIFI

Minicard



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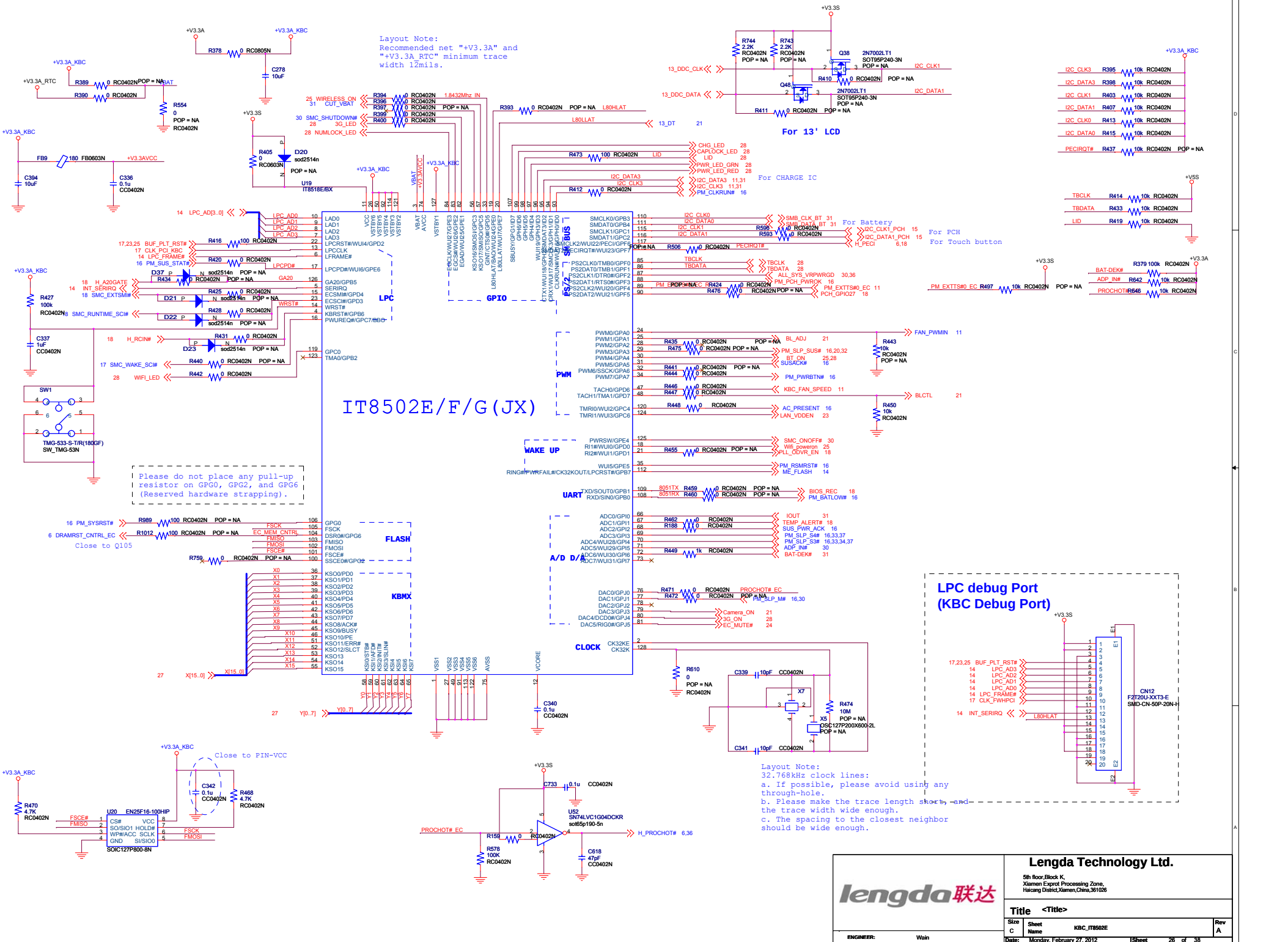
ENGINEER: Wain	**Title** <Title>	
	Size C / Sheet Name Minicard1	Rev A
	Date: Thursday, February 16, 2012	Sheet 25 of 38


IT8502E/F/G(JX)
Layout Note:
Recommended net "+V3.3A" and
"+V3.3A_RTC" minimum trace
width 12mils.
For 13' LCD
For CHARGE IC
For Battery
For PCH
For Touch button
Please do not place any pull-up
resistor on GPG0, GPG2, and GPG6
(Reserved hardware strapping).
Close to Q105
Close to PIN-VCC
LPC debug Port
(KBC Debug Port)
CN12
F2T20U-XXT3-E
SMD-CN-50P-20N-H
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any
through-hole.
b. Please make the trace length short, and
the trace width wide enough.
c. The spacing to the closest neighbor
should be wide enough.
LPC
GPIO
SPI BUS
FWH
PWM
WAKE UP
UART
FLASH
KBMX
A/D D/A
CLOCK
SW1
TMG-533-S-T/R(180GF)
SW_TMG-53N
U19
IT8518E/BX
U20
EN25F16-100HIP
SOIC127P800-8N
U52
SN74LVC1G04DCKR
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Title <Title>
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Sheet Name KBC_IT8502E
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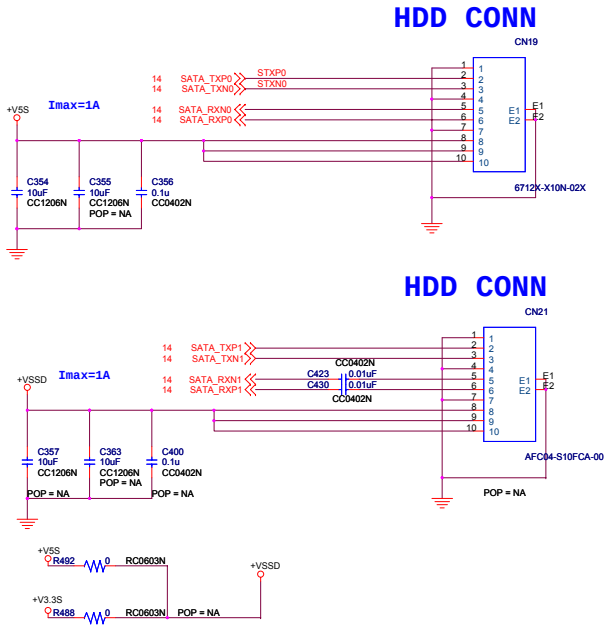

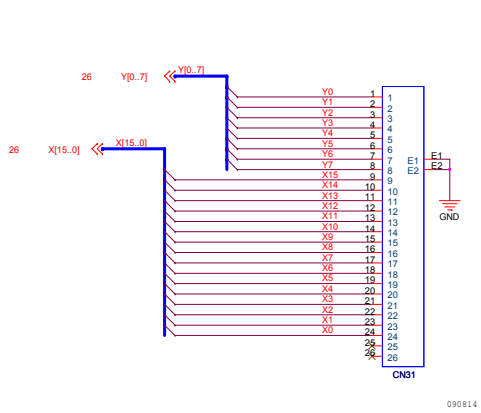

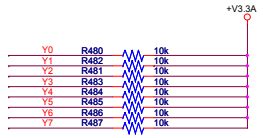

TO KEY_BOARD

10.3.2 Pin Assignment

The following table describes all of the pins on Serial ATA connector.

Table 10.3-1 Signal pin assignment

Signal segment key			
Signal segment	S1	GND	2nd mate
	S2	A+	Differential Pair A from PHY
	S3	A-	
	S4	GND	
	S5	B-	Differential Pair B from PHY
	S6	B+	
	S7	GND	2nd mate
Signal segment "L"			
Central connector polarizer			
Power segment "L"			
Power segment	P1	V33	3.3V power (Unused)
	P2	V33	3.3V power (Unused)
	P3	V33	3.3V power pre-charge 2nd mate (Unused)
	P4	GND	
	P5	GND	
	P6	GND	
	P7	V5	5V power pre-charge 2nd mate
	P8	V5	5V power
	P9	V5	5V power
	P10	GND	
	P11	ACT/ Spin	
	P12	GND	1st mate
	P13	V12	12V power pre-charge 2nd mate (Unused)
	P14	V12	12V power (Unused)
	P15	V12	12V power (Unused)
Power segment key			

Notice: This drive uses 5V power only. 3.3V and 12V power are not used.

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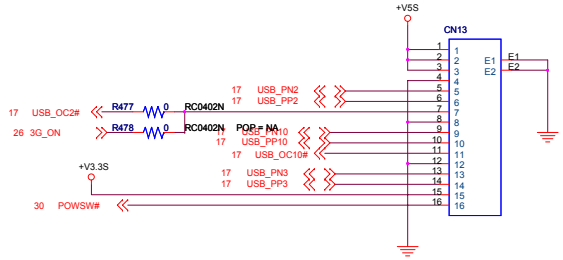
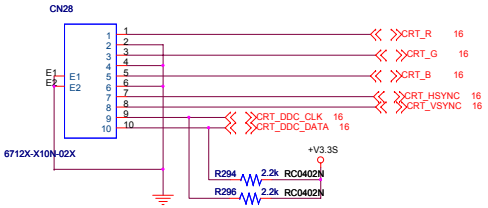
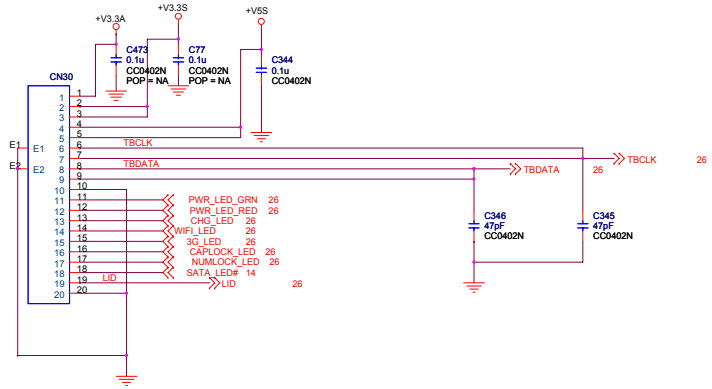
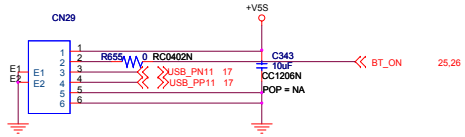
TO USB BOARD









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Size	Sheet Name	Rev
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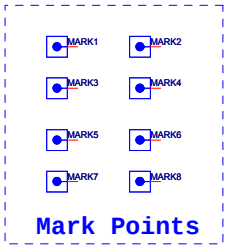
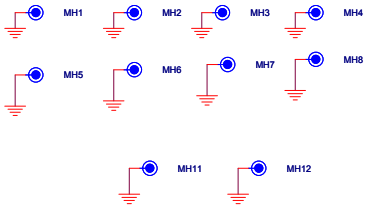
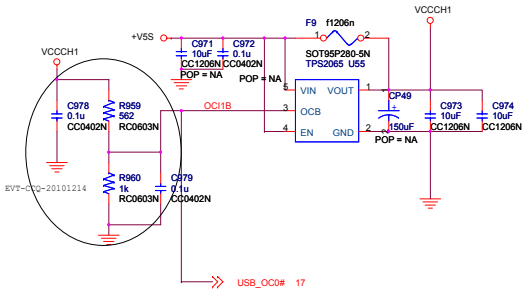
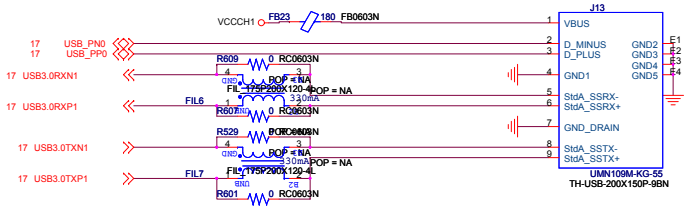






USB3.0 Port



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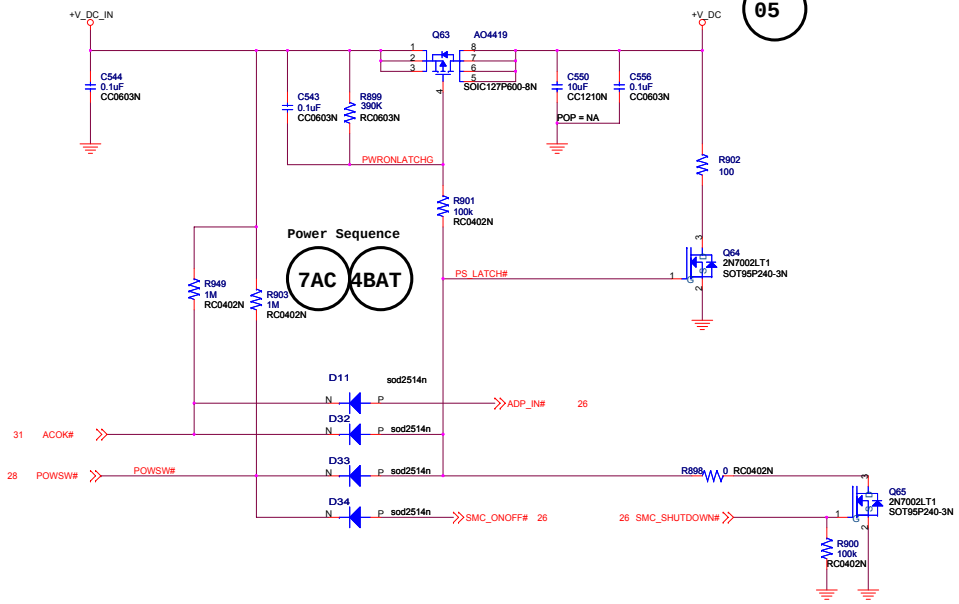
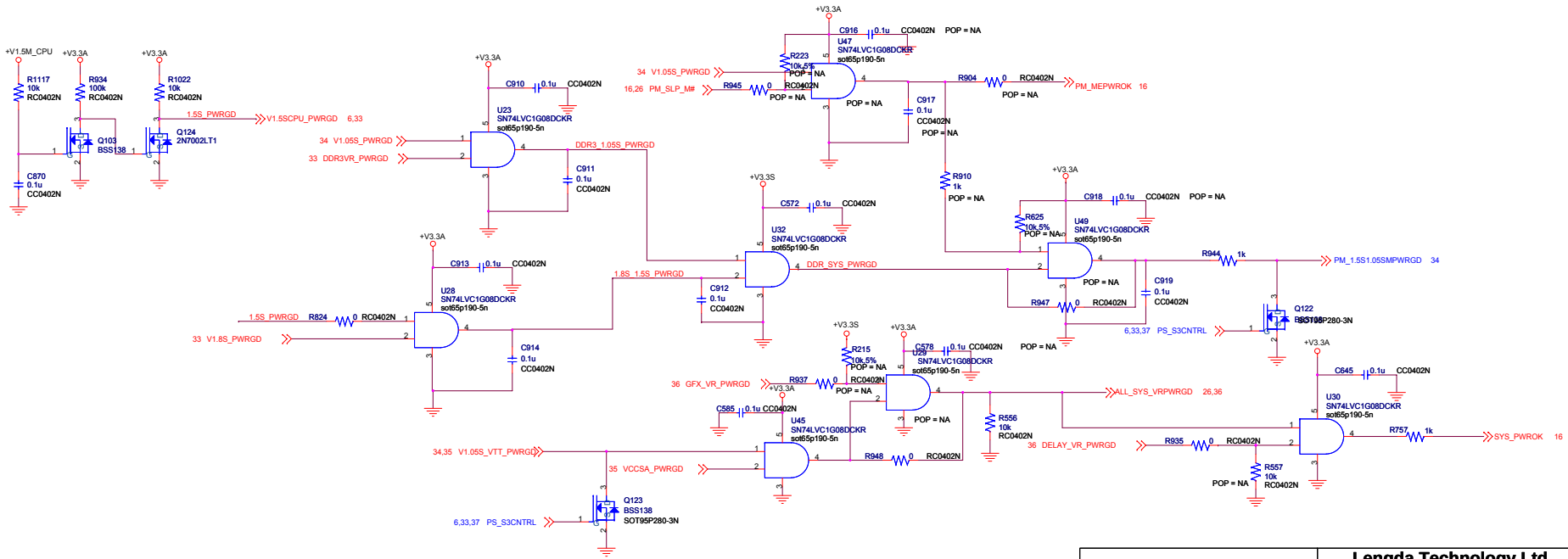
Power Button Detect & Latch

Power Sequence 05





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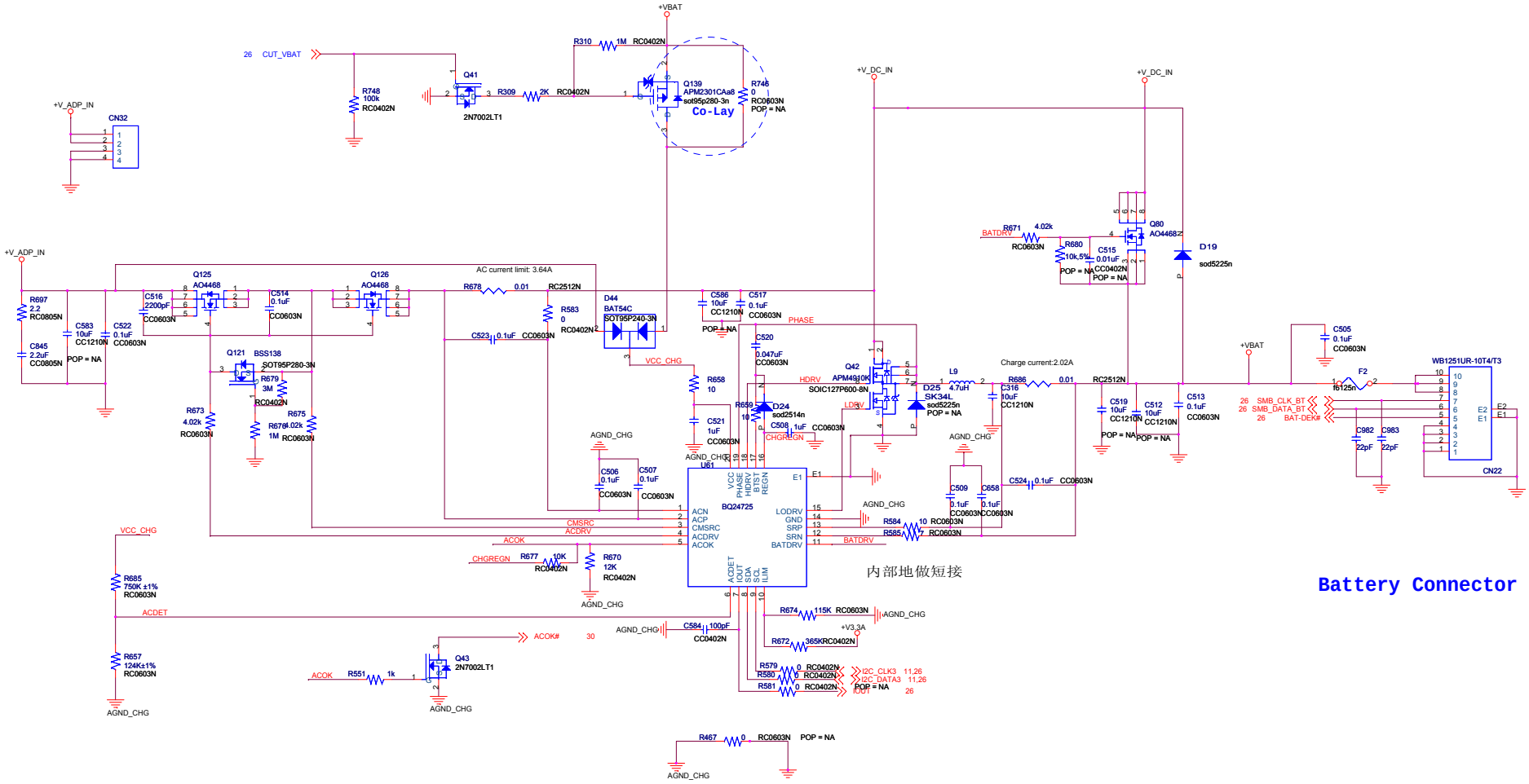

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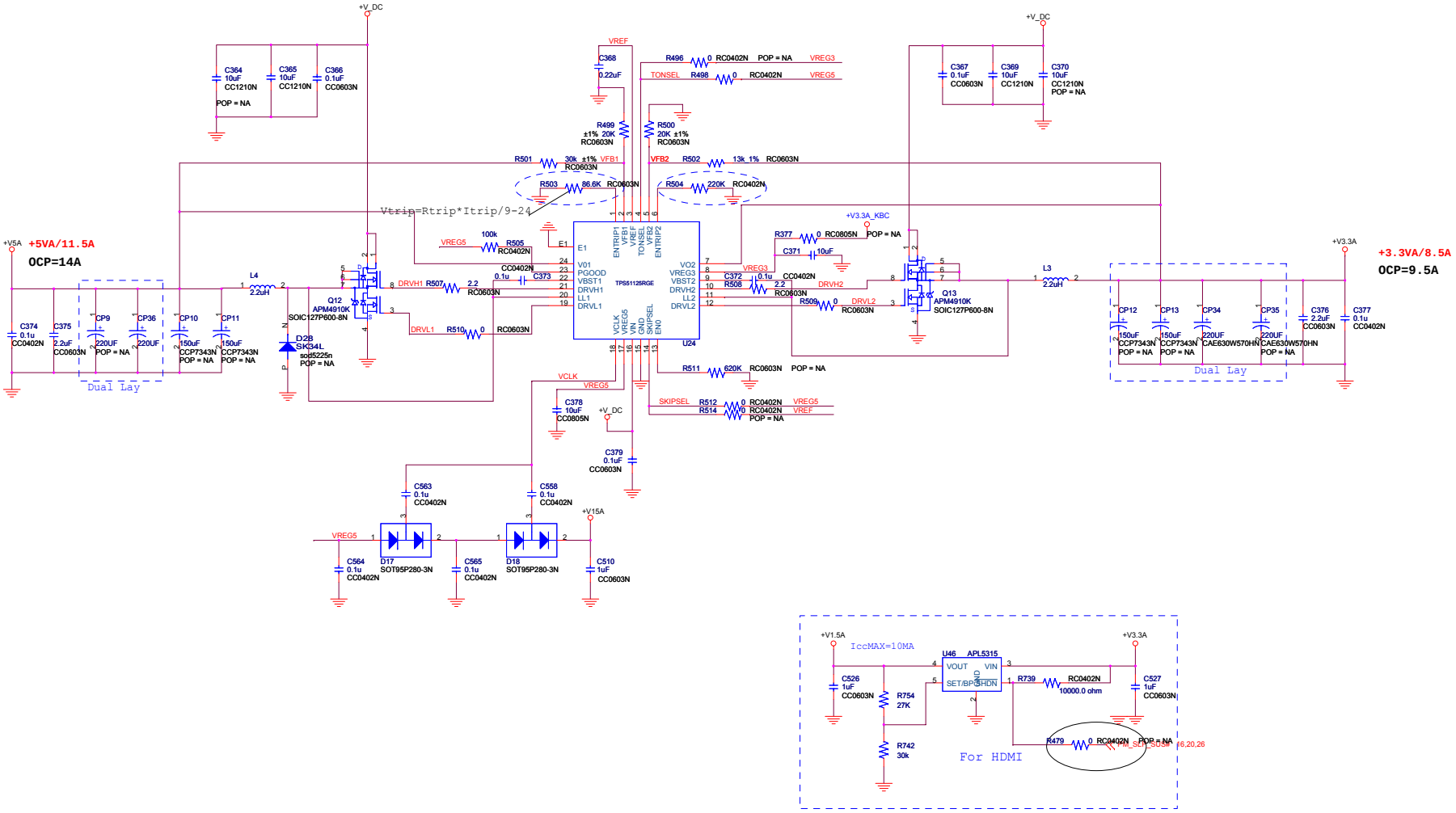

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ENGINEER: Wain	Size C / Sheet Name Power_System / Rev A	
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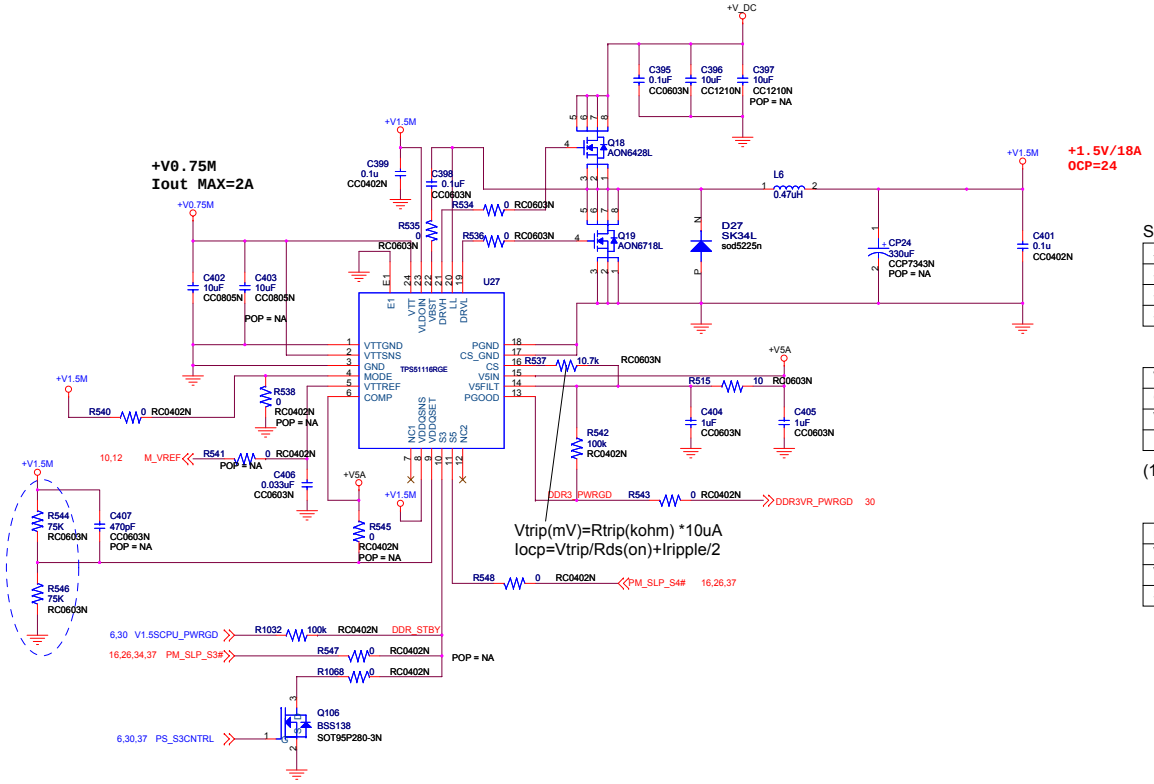

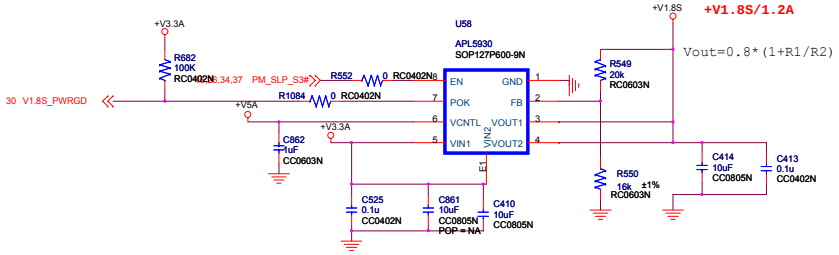

S3 & S5 Control

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF(HI-Z)
S4/S5	LO	LO	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

VDDQSET	VDDQ (V)	VTTREF & VTT	NOTE
GND	2.5	VDDQSNS/2	DDR
V5IN	1.8	VDDQSNS/2	DDR2
FB Resistors	Adjustable	VDDQSNS/2	1.5V< VDDQ<3V

(100*VDDQ-75)kohm

MODE	DISCHARGE MODE
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

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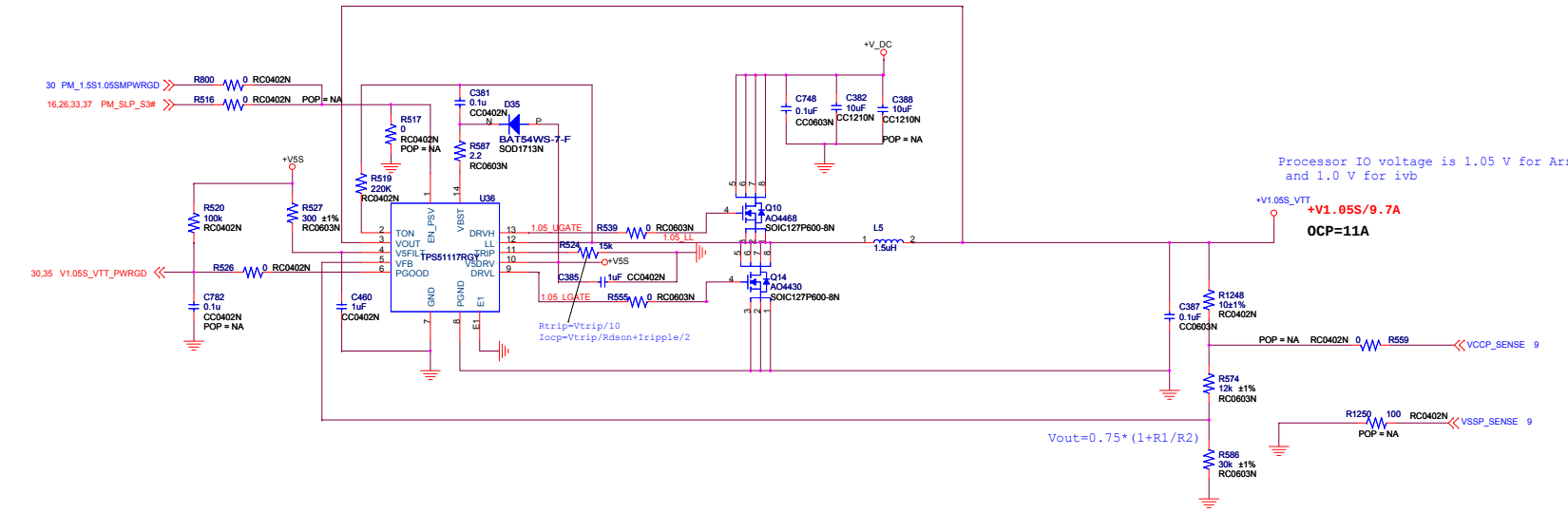

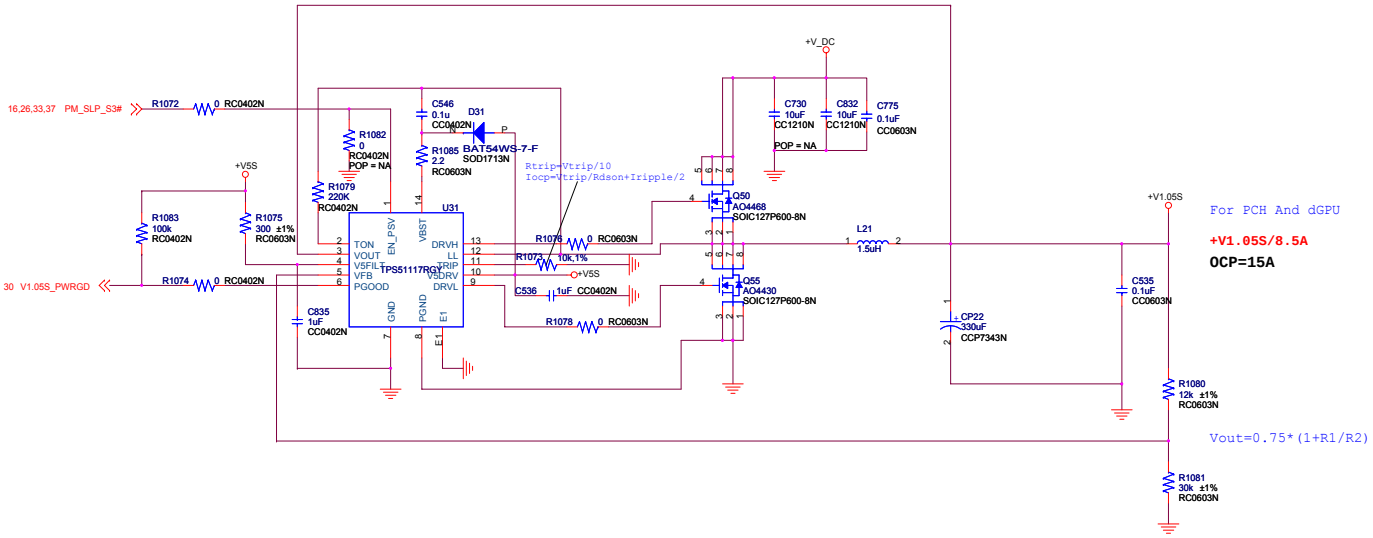

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Size	Sheet Name	Rev
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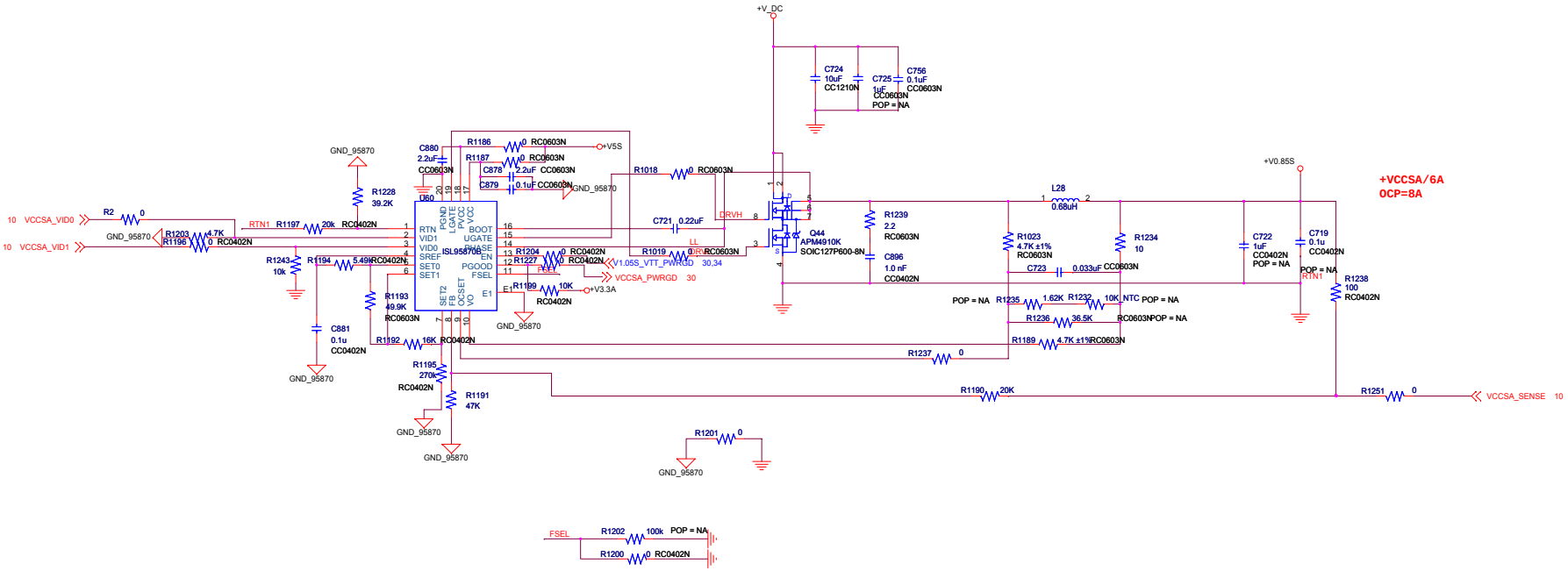

FSEL VOLTAGE	FREQUENCY(KHZ)
GND	300KHZ
FLOAT	500KHZ
100K to GND	600KHZ
5.0V	1000KHZ

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Size	Sheet Name	Rev
C	Power_GFXCore	A

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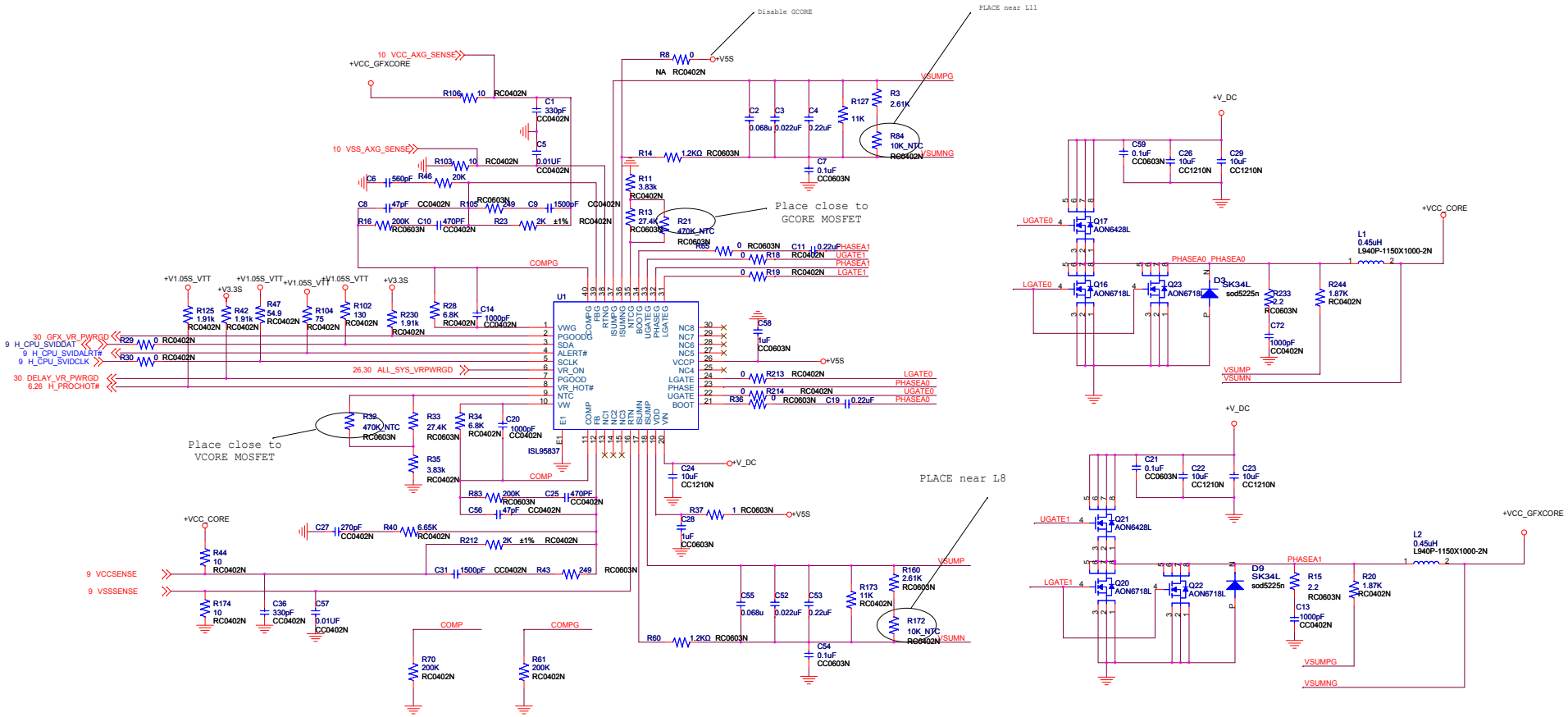

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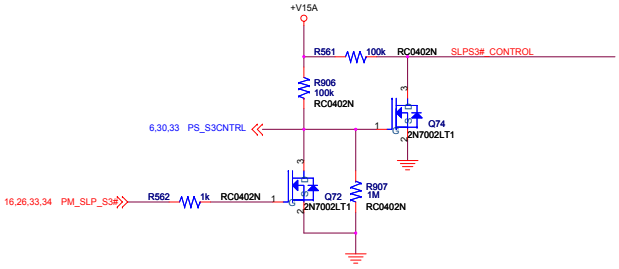
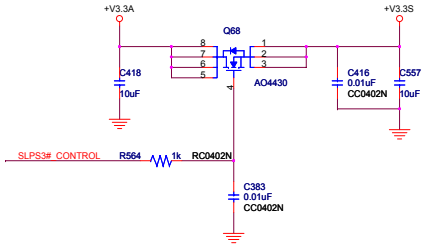
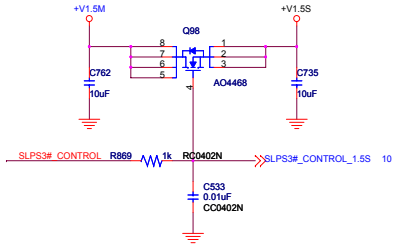
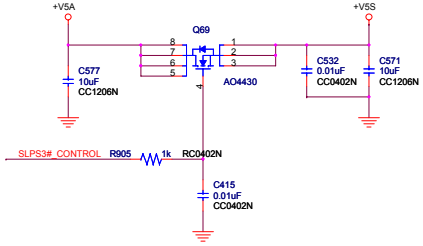
S3 /S4 Power control



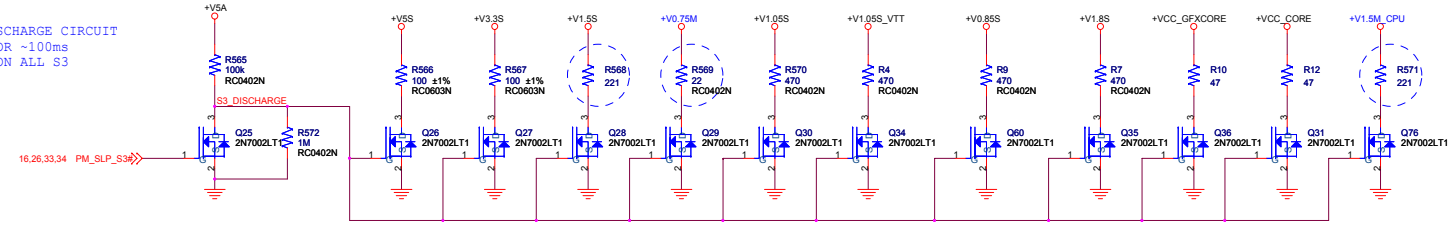




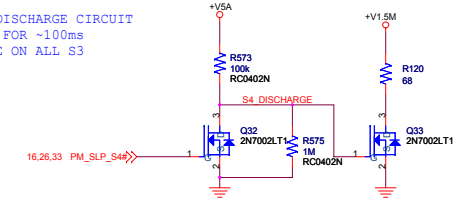


Power Discharge Circuit

SLP_S3# DISCHARGE CIRCUIT
DESIGNED FOR ~100ms
DISCHARGE ON ALL S3
RAILS.



SLP_S4# DISCHARGE CIRCUIT
DESIGNED FOR ~100ms
DISCHARGE ON ALL S3
RAILS.



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1.R685 be changed to connect to VCC_CHG

2.Install R57,R74;Uninstall R49,R50

3.Install R97,R100,R1156 ; Uninstall R780,R1089

4.Install R664 ; Uninstall R31

5. Add R467

6. Uninstall R1244

7. install FB23

8 .Exchange VCCSA_VID0 and VCCSA_VID1; R1194 change to 5.49k, R1193 change to 49.9K, R1191 change to 47k, R1192 change to 16K

9. Add CN32

V1.O2->V1.03

1.ADD Q79,Q81,R288,R289,R662,R872

2.ADD R488,R492

3.BOM ADD r2

V1.O2->V1.04

1.Core:Add Q22,Q23 (Page 36)

2.ADD BT_ON to CN29,add R655

3.Charger. Add Q41.Q139.R309.R310.R746,R748,install R396

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