E450

Sandy Bridge Mobile PROCESSOR
With Cougar Point-M

June 2010

Revision 0.2

HASEE 神舟	HASEE TECHNOLOGY INC.,			
	Cover Page			
Draw by LIZX	Size B	CAGE Code <Cage Code>	DWG NO	Rev 0.2
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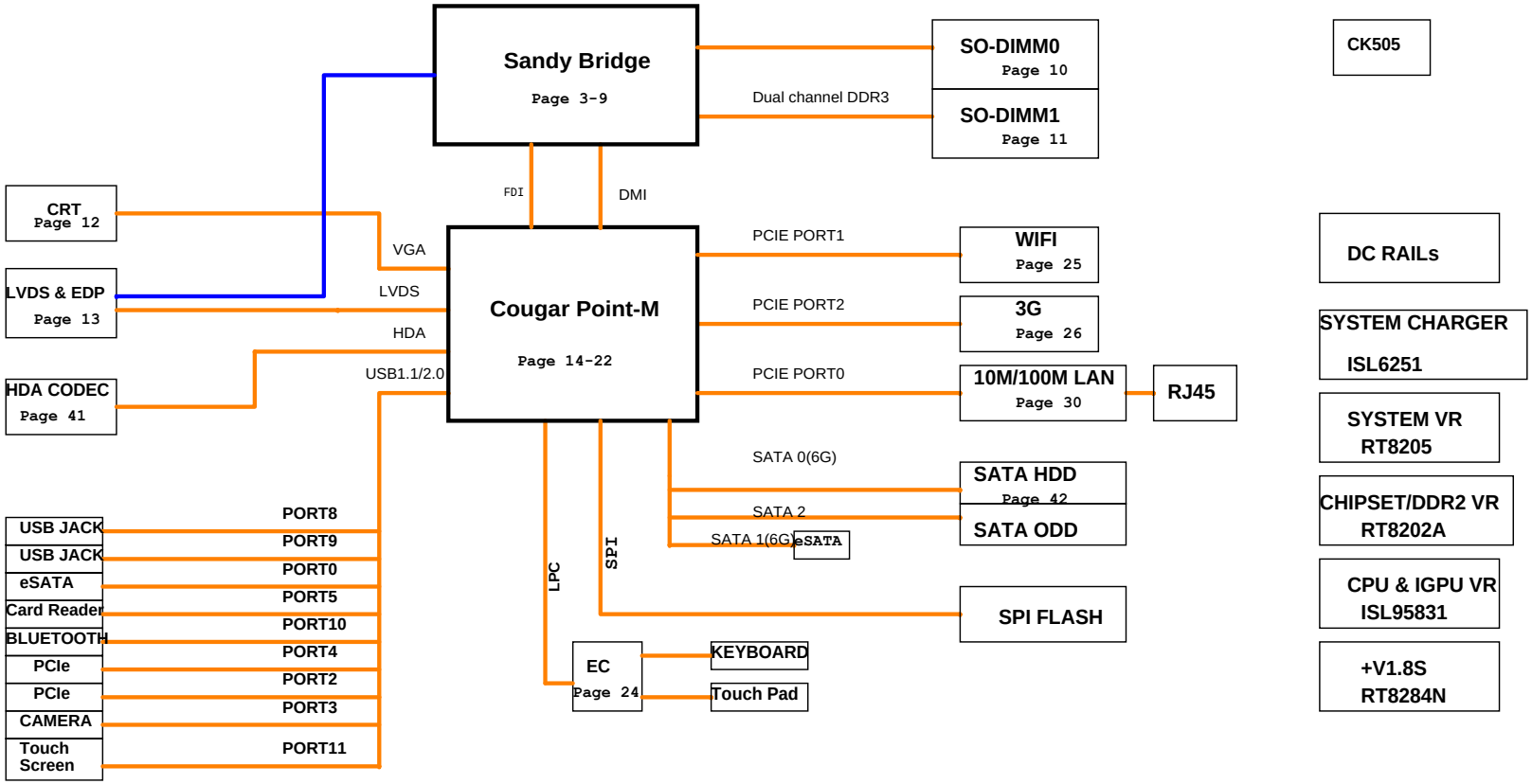

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Block Diagram

Draw by	Size B	CAGE Code <Cage Code>	DWG NO	Rev 0.2
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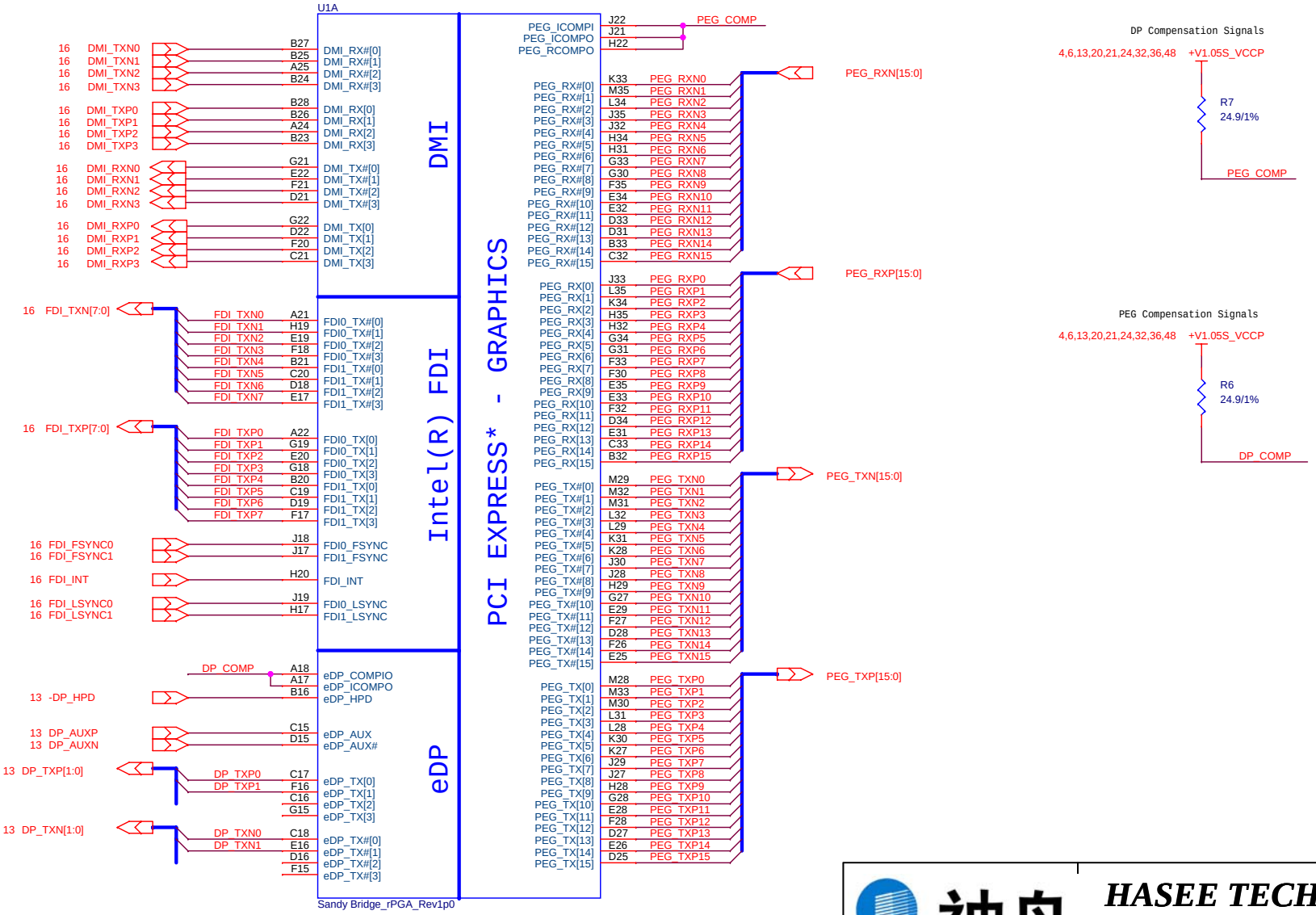

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SANDYBRIDGE 1/7

Draw by	Size B	CAGE Code <Cage Code>	DWG NO	Rev 0.2
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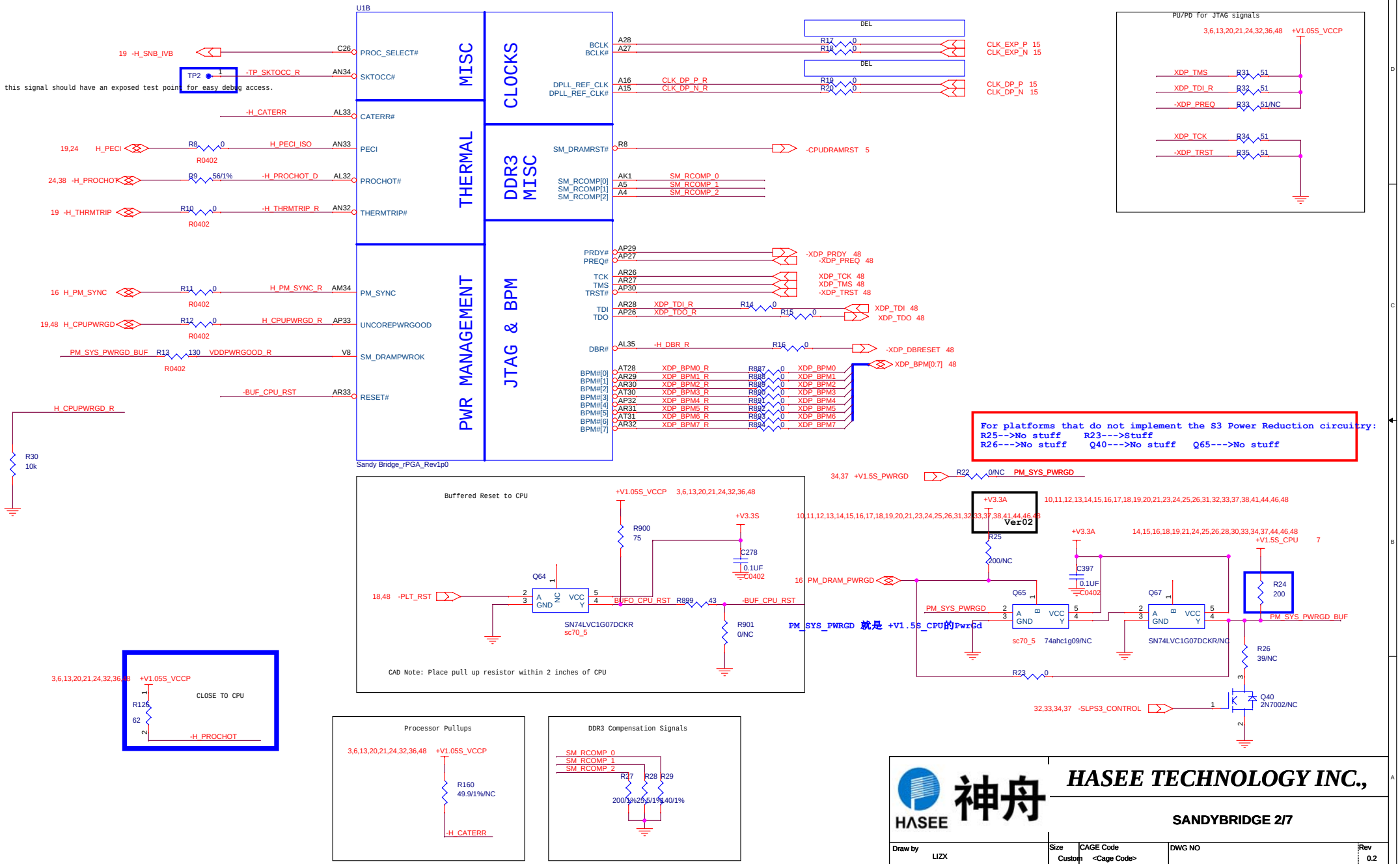

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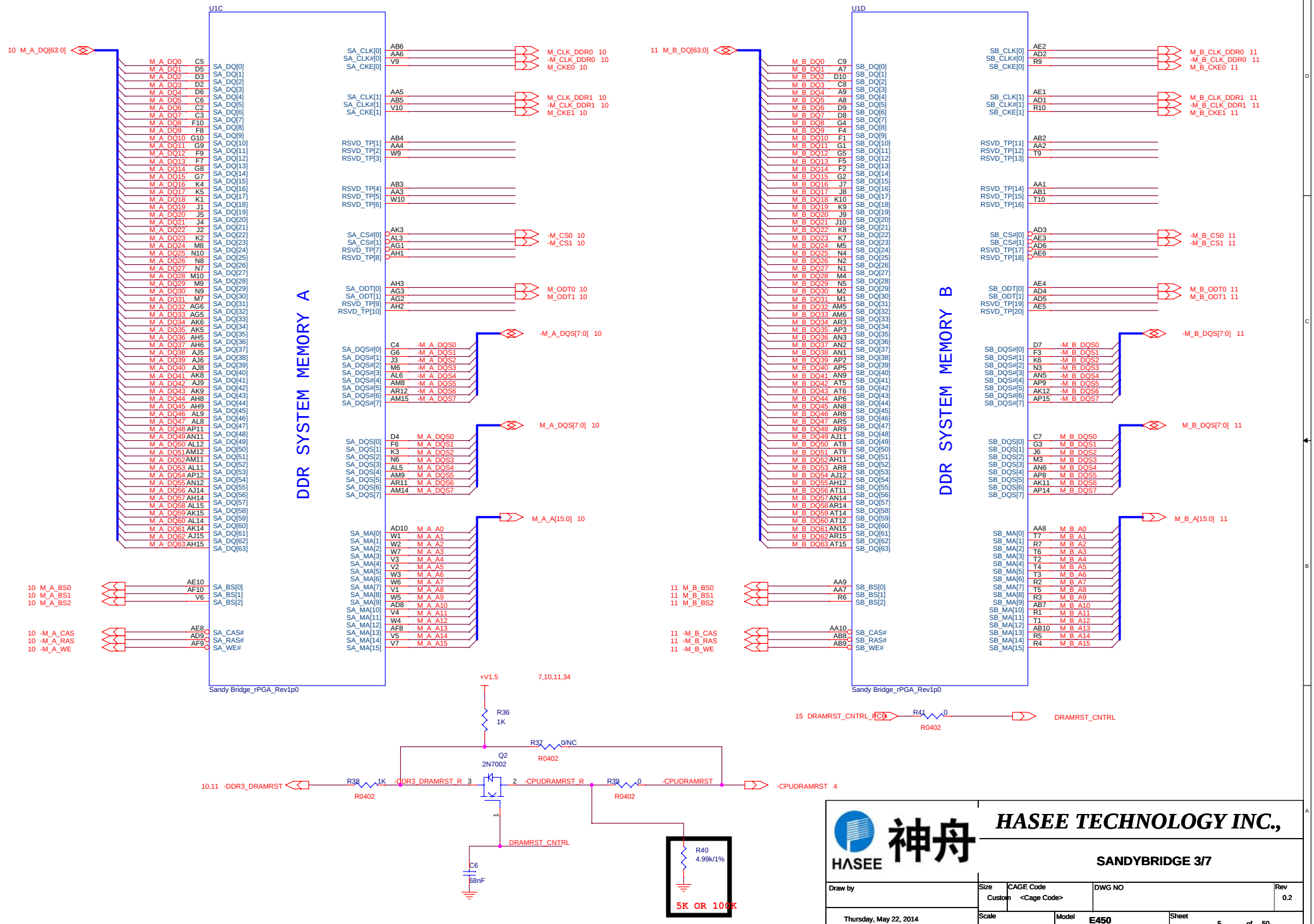
SANDYBRIDGE 2/7

Draw by LIZX	Size Custom	CAGE Code <Cage Code>	DWG NO	Rev 0.2
Thursday, May 22, 2014	Scale	Model E450	Sheet 4 of 50	



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SANDYBRIDGE 3/7

Draw by	Size: Custom	CAGE Code: <Cage Code>	DWG NO	Rev: 0.2
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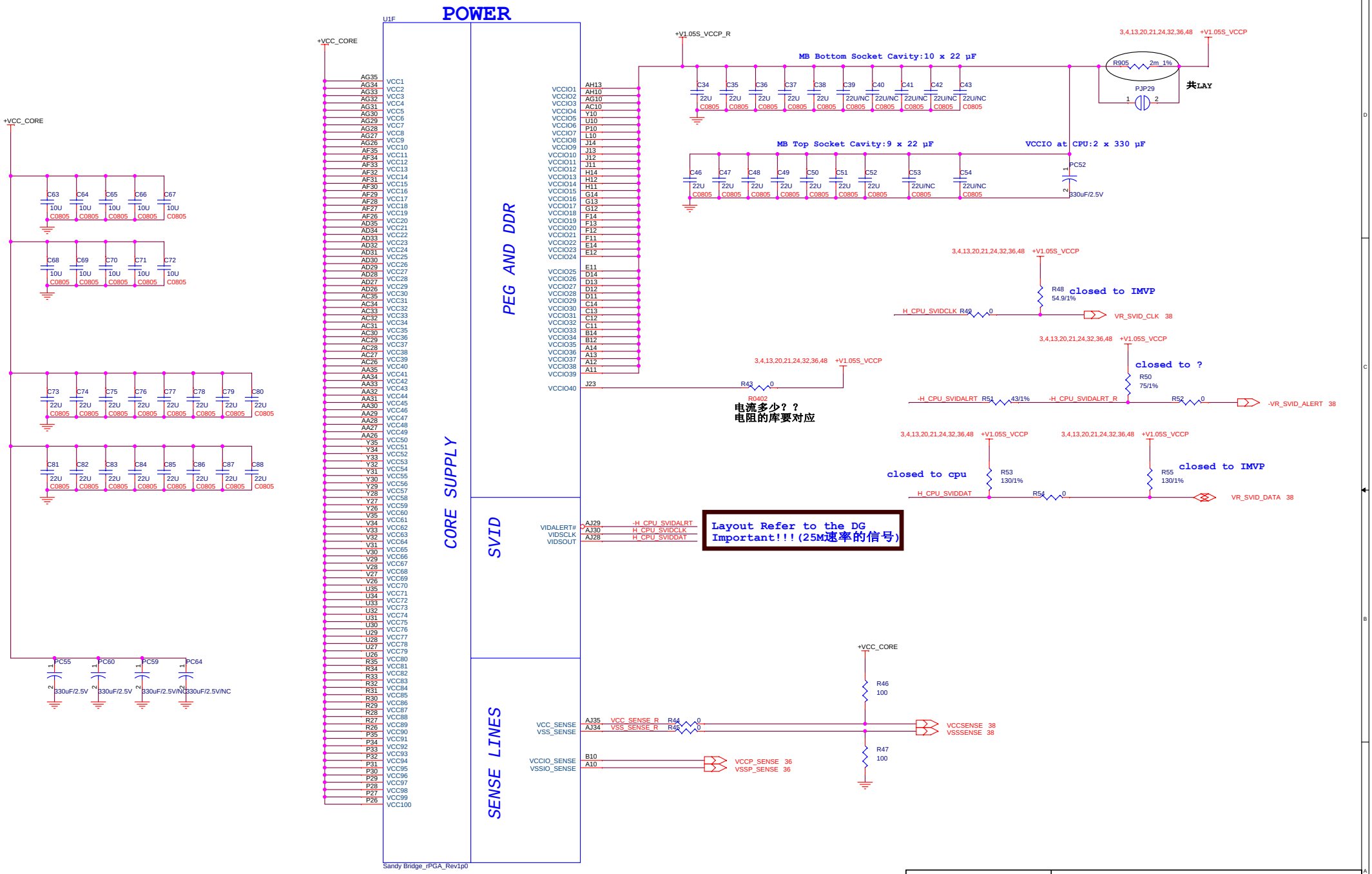

HASEE 神舟	HASEE TECHNOLOGY INC.,			
	SANDYBRIDGE 4/7			
Draw by	Size Custom	CAGE Code <Cage Code>	DWG NO	Rev 0.2
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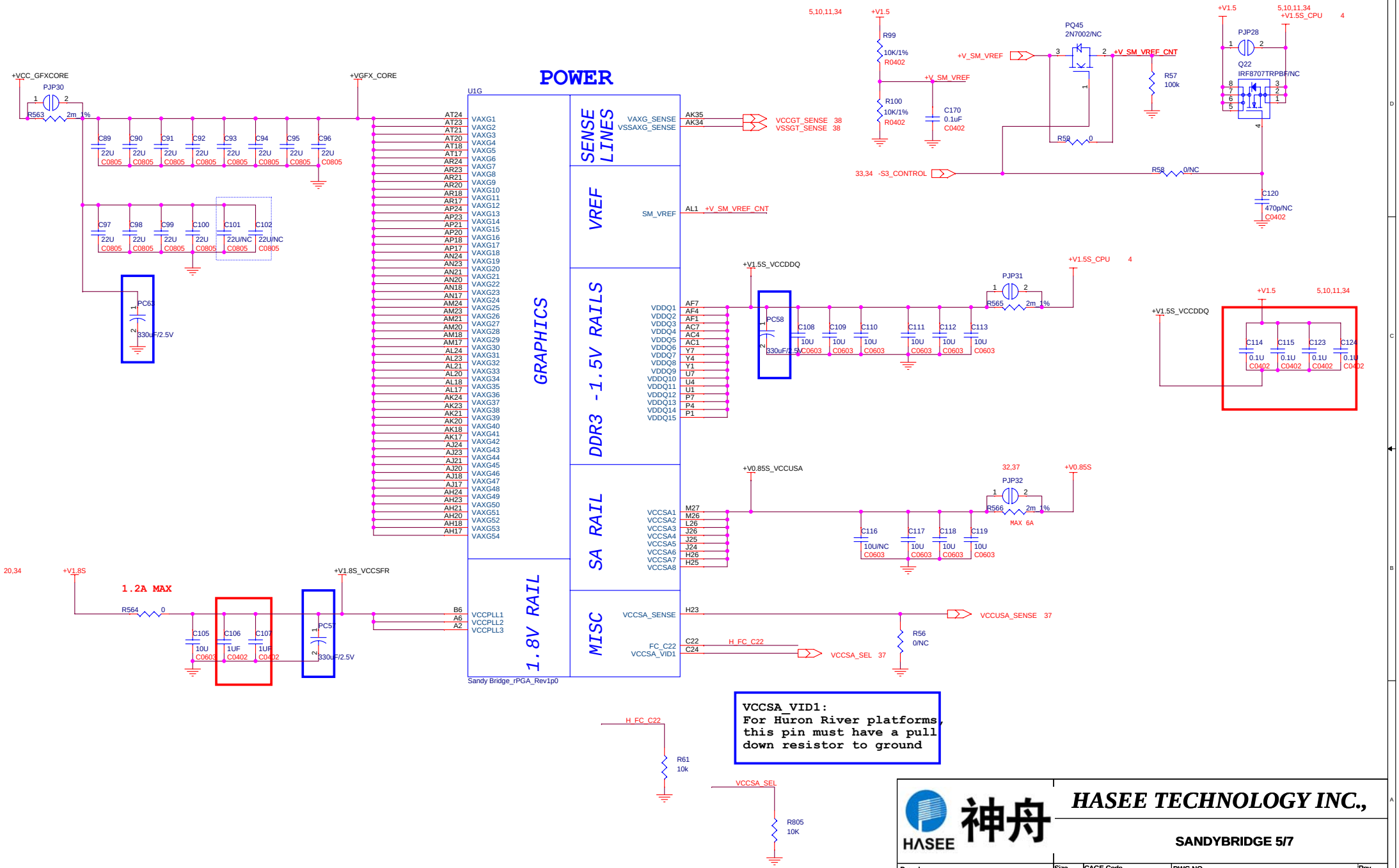

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SANDYBRIDGE 5/7

Draw by	Size	CAGE Code	DWG NO	Rev
	Custom	<Cage Code>		0.2
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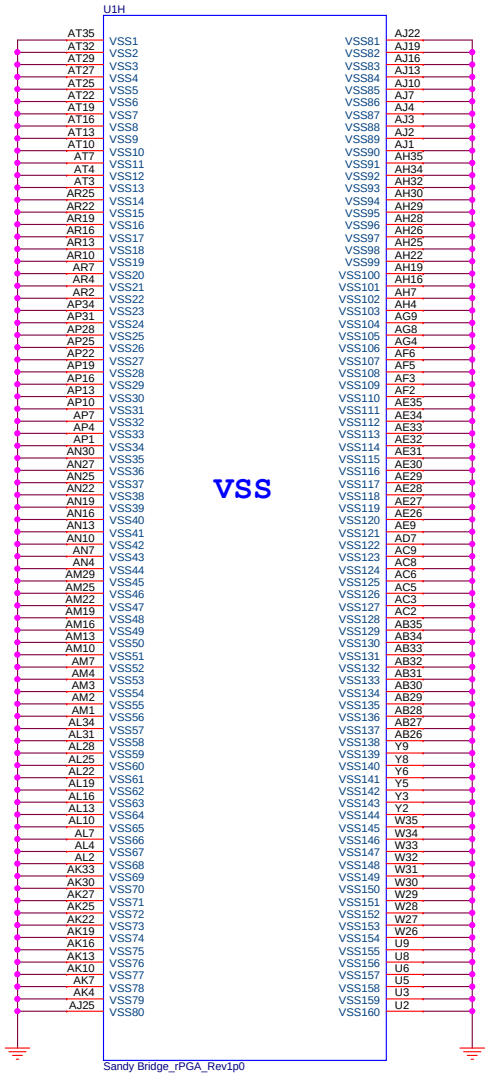

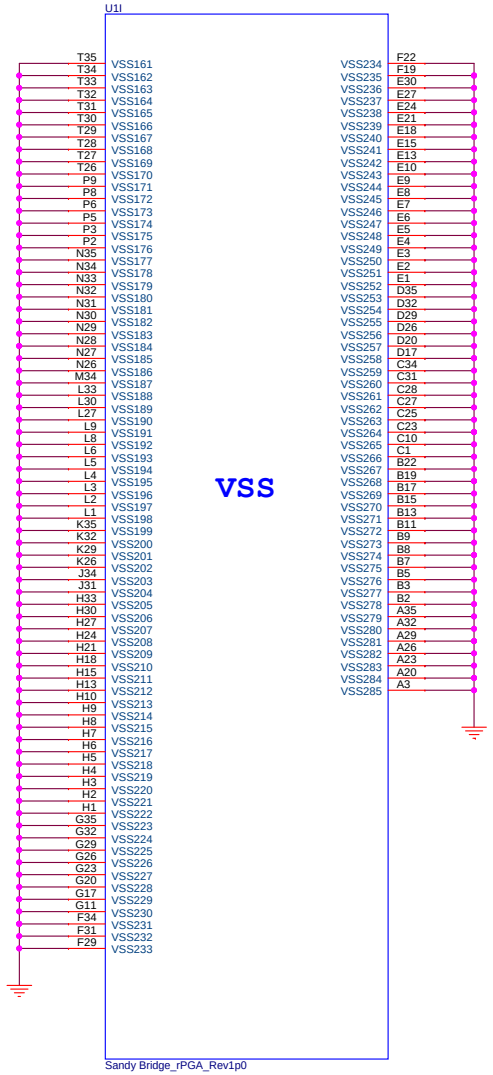

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SANDYBRIDGE 6/7

Draw by	Size: Custom	CAGE Code: <Cage Code>	DWG NO	Rev: 0.2
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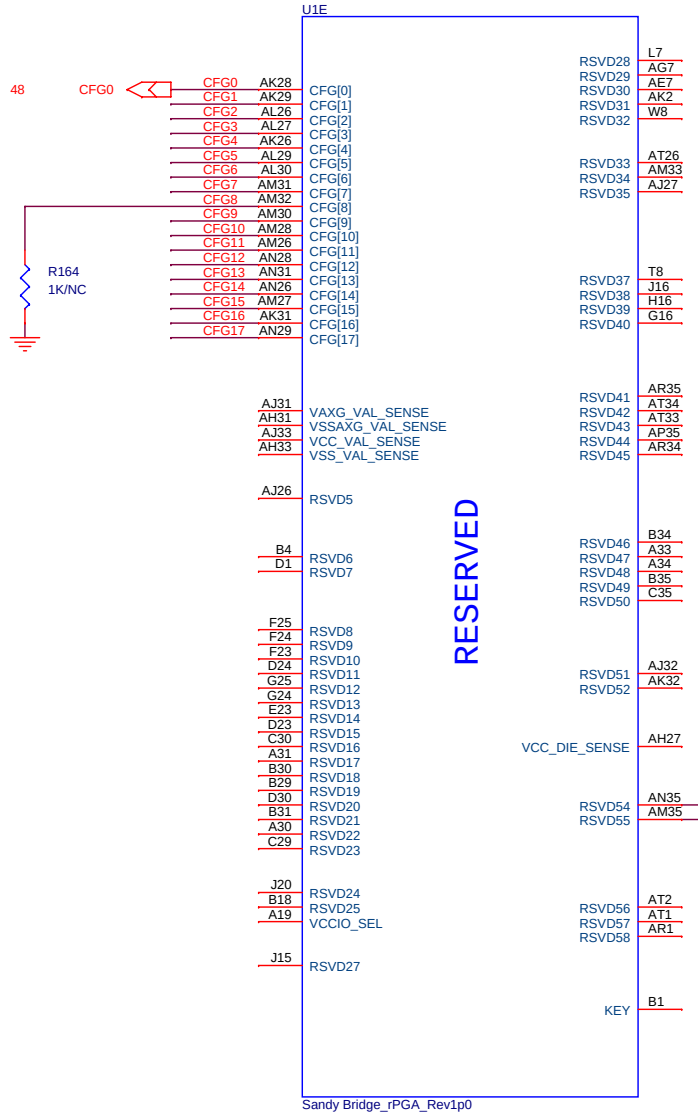
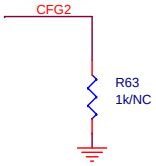
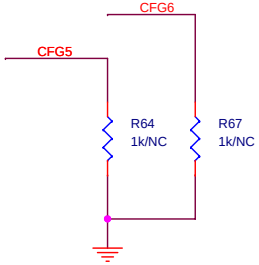
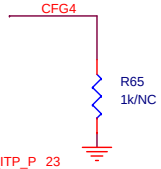




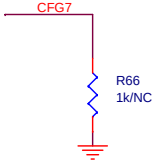
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



Display Port Presence Strap(EDP)	
CFG4	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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SANDYBRIDGE 7/7

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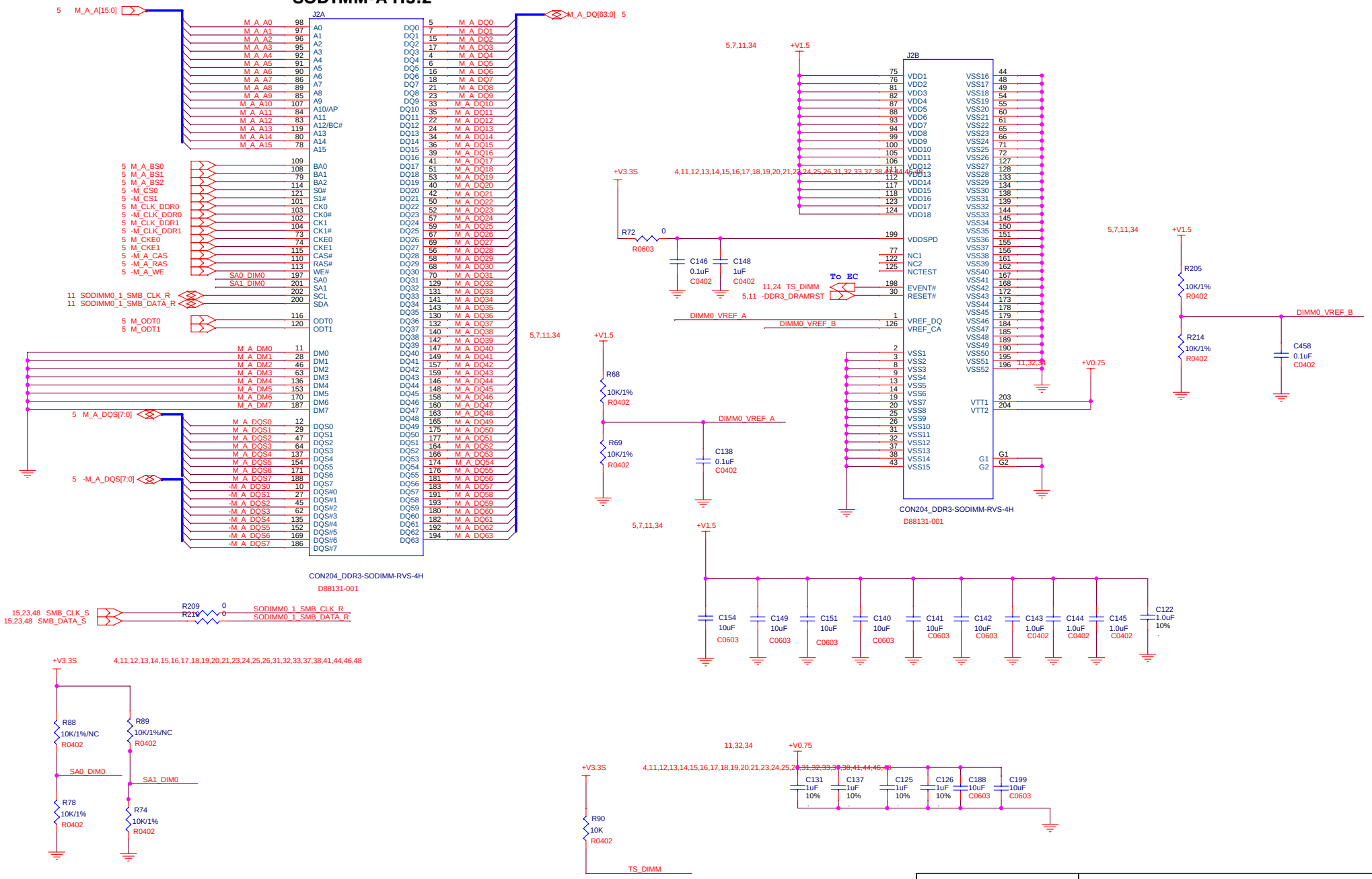
SODIMM-A H5.2



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	DIMM 0		
Draw by	Size: Custom	CAGE Code: <Cage Code>	DWG NO	Rev: 0.2
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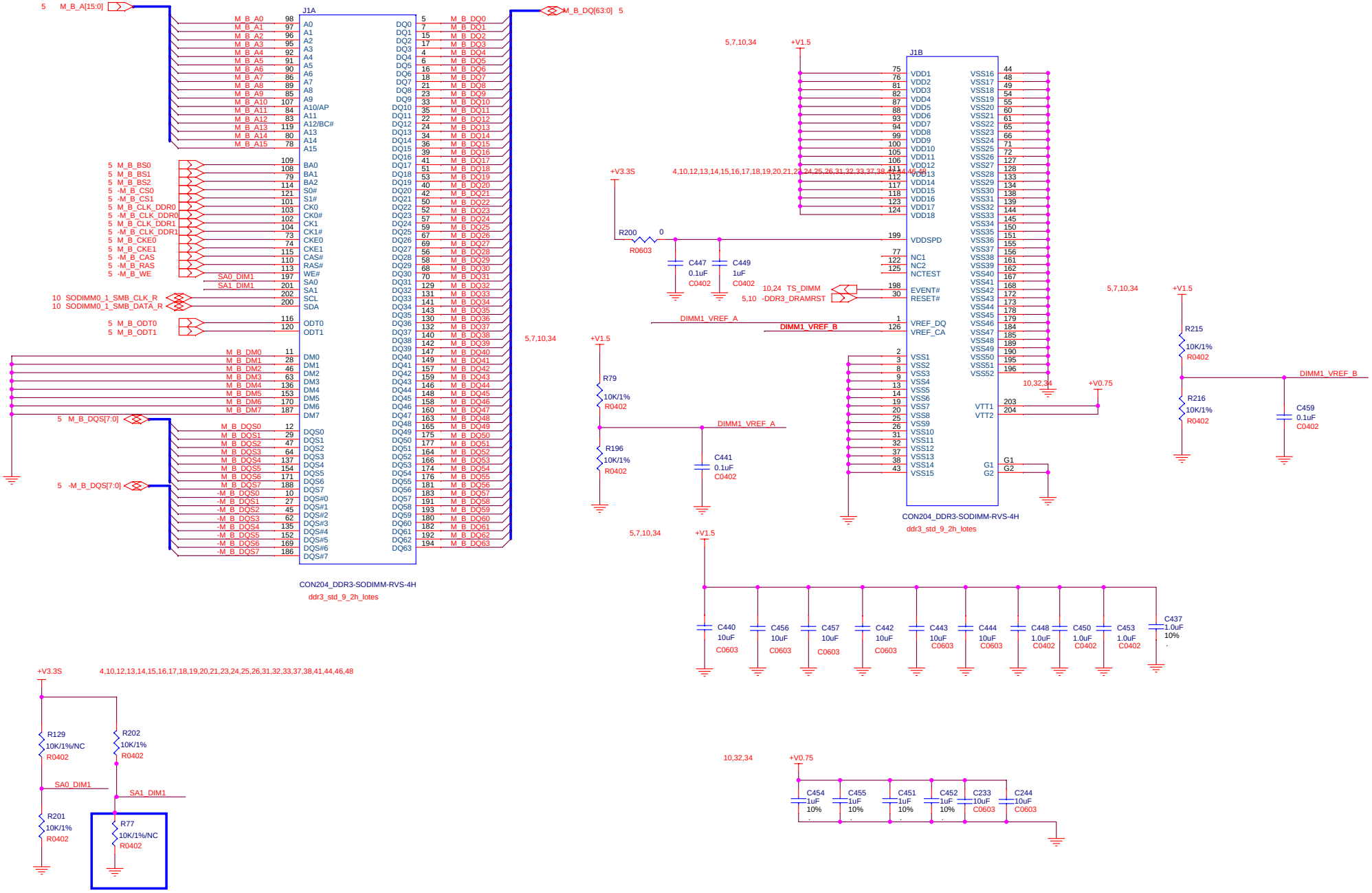
SODIMM-B H9.2



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DIMM 1

Draw by	Size	CAGE Code	DWG NO	Rev
	Custom	<Cage Code>		0.2
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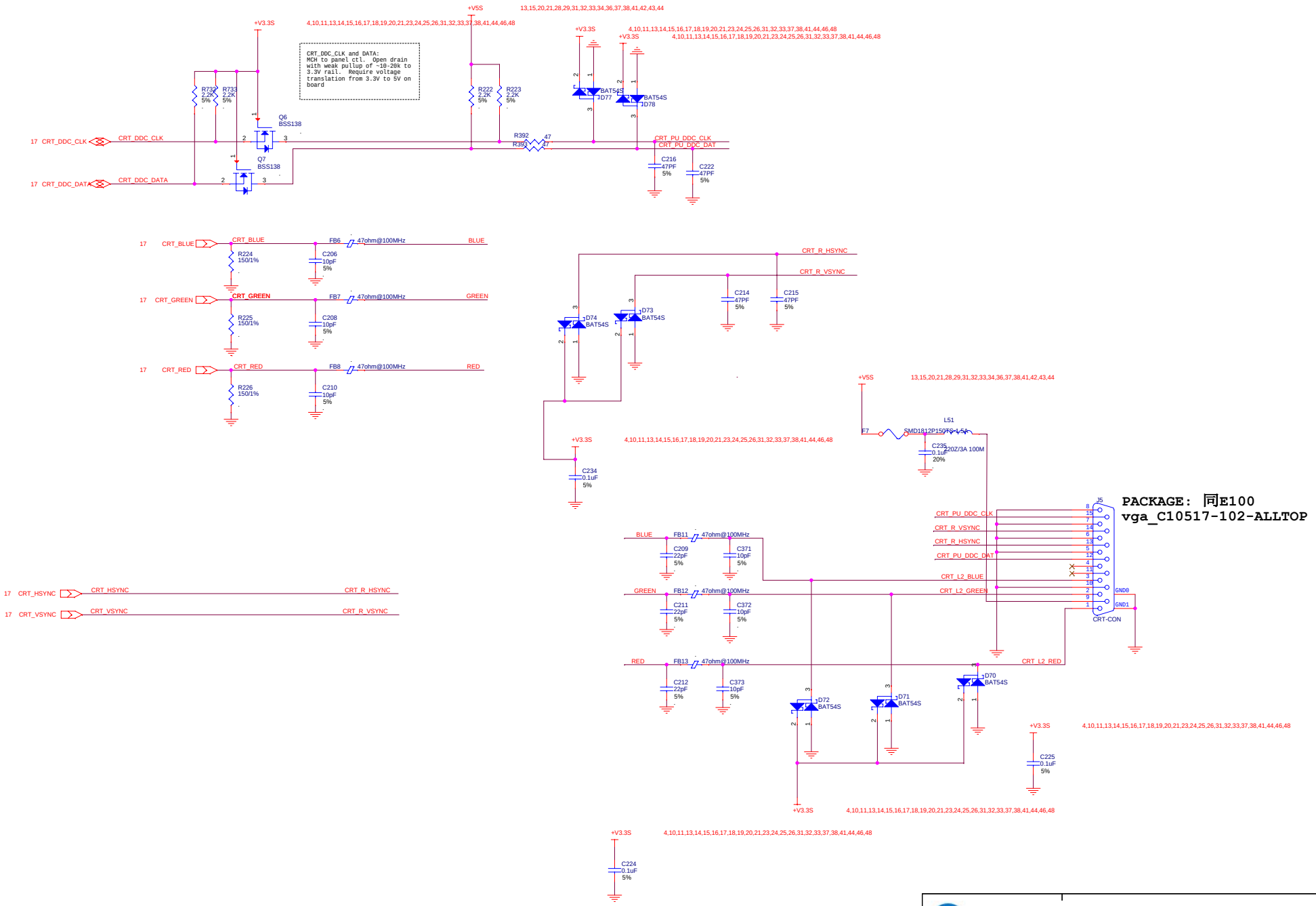

PACKAGE: 同E100
vga_C10517-102-ALLTOP

HASEE 神舟	**HASEE TECHNOLOGY INC.,**			
	VGA			
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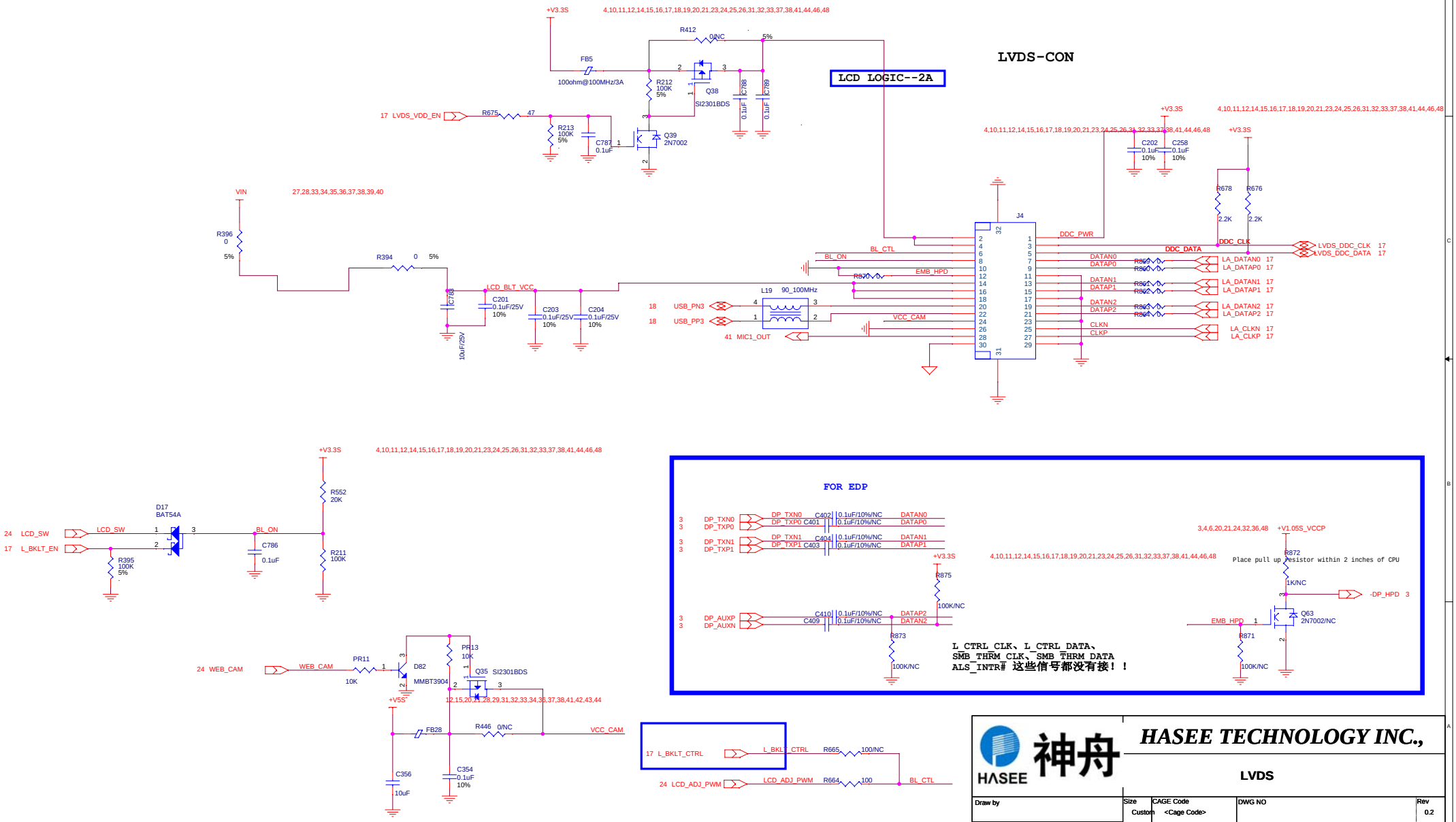

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LVDS

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	Custom	<Cage Code>		0.2
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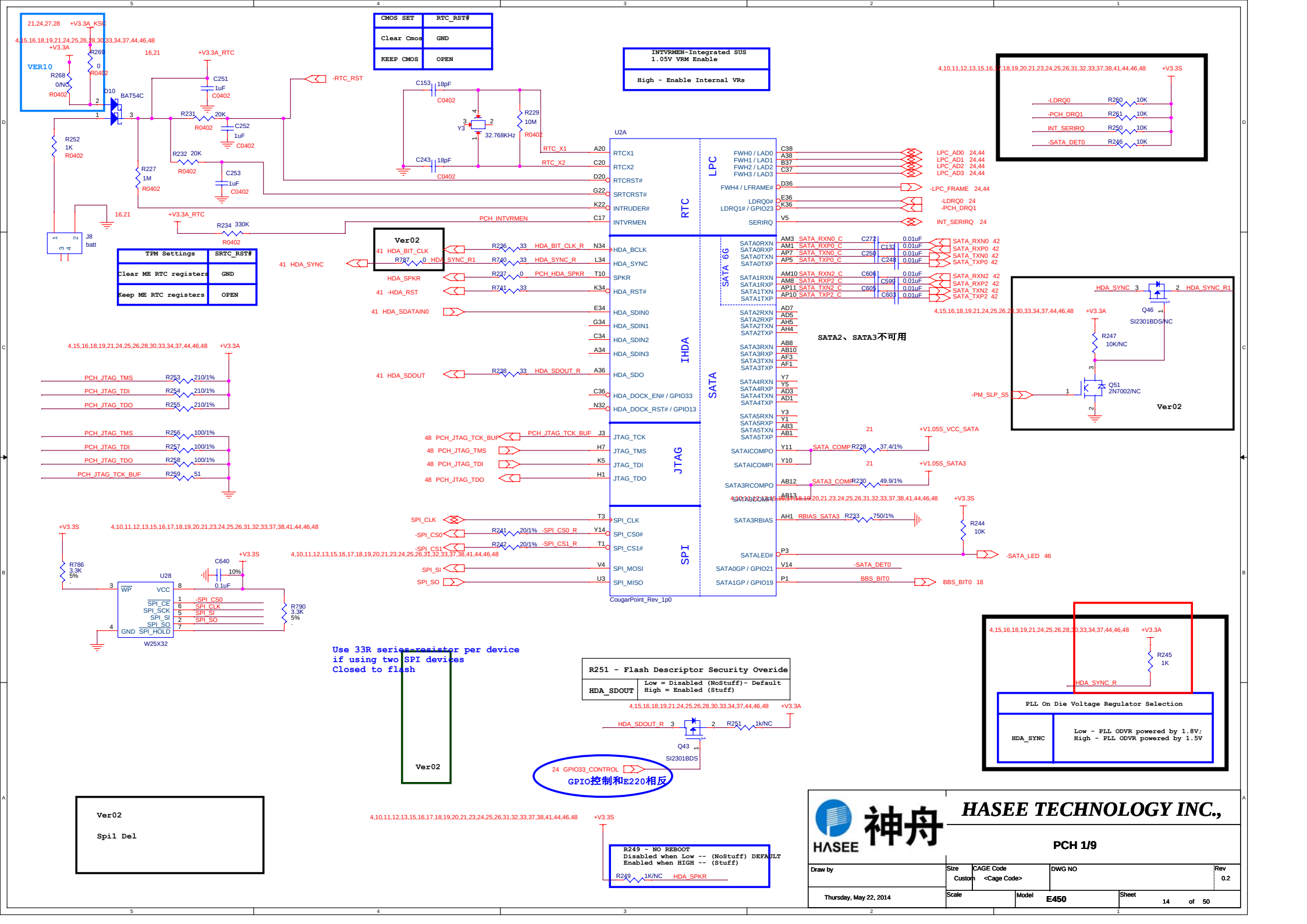
CMOS SET | RTC_RST#
Clear Cmos | GND
KEEP CMOS | OPEN
INTVRMEN-Integrated SUS 1.05V VRM Enable
High - Enable Internal VRs
TPM Settings | SRTC_RST#
Clear ME RTC registers | GND
Keep ME RTC registers | OPEN
Ver02
SATA2、SATA3不可用
R251 - Flash Descriptor Security Overide
HDA_SDOUT | Low = Disabled (NoStuff)- Default
High = Enabled (Stuff)
Use 33R series resistor per device
if using two SPI devices
Closed to flash
GPIO控制和E220相反
PLL On Die Voltage Regulator Selection
HDA_SYNC | Low - PLL ODVR powered by 1.8V;
High - PLL ODVR powered by 1.5V
R249 - NO REBOOT
Disabled when Low -- (NoStuff) DEFAULT
Enabled when HIGH -- (Stuff)
Spi1 Del
U2A
RTC
LPC
IHDA
SATA
JTAG
SPI
CougarPoint_Rev_1p0
U28
W25X32
HASEE TECHNOLOGY INC.,
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PCH 1/9
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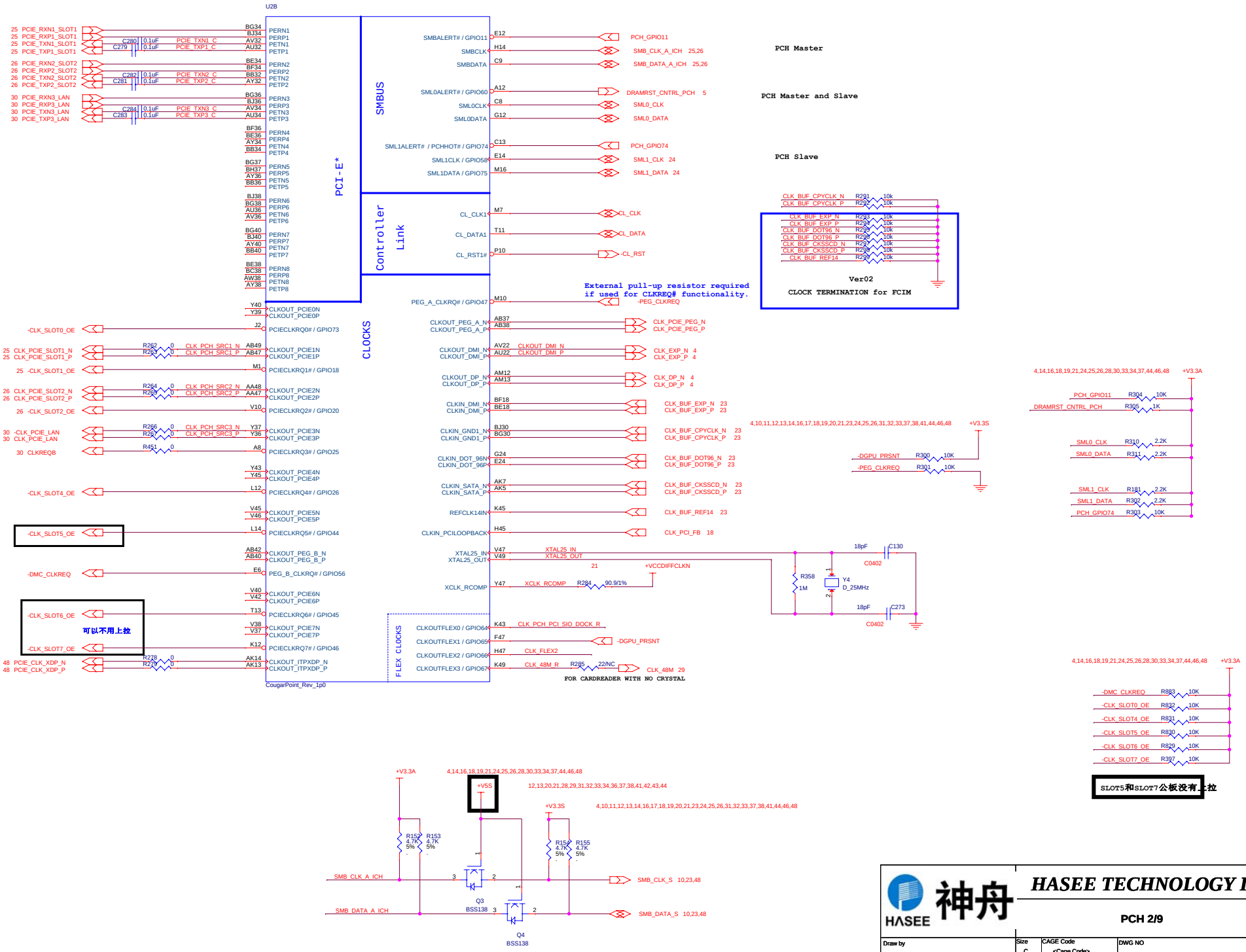

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PCH 2/9

Draw by	Size	CAGE Code	DWG NO	Rev
	C	<Cage Code>		0.2
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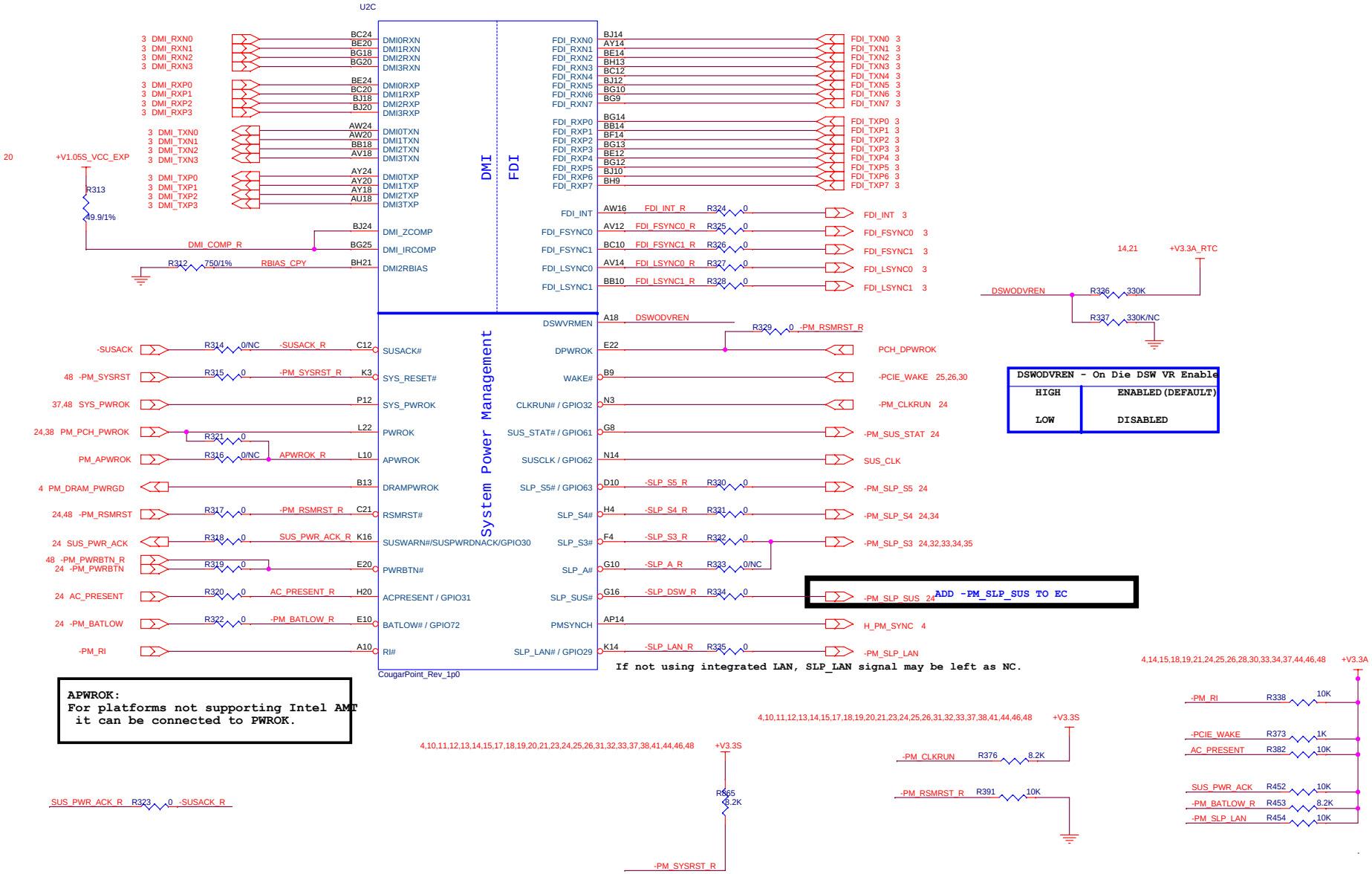

DSWODVREN - On Die DSW VR Enable	
HIGH	ENABLED(DEFAULT)
LOW	DISABLED

ADD -PM_SLP_SUS TO EC

If not using integrated LAN, SLP_LAN signal may be left as NC.

APWROK:
For platforms not supporting Intel AMT it can be connected to PWROK.

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PCH 3/9--DMI,FDI,GPIO

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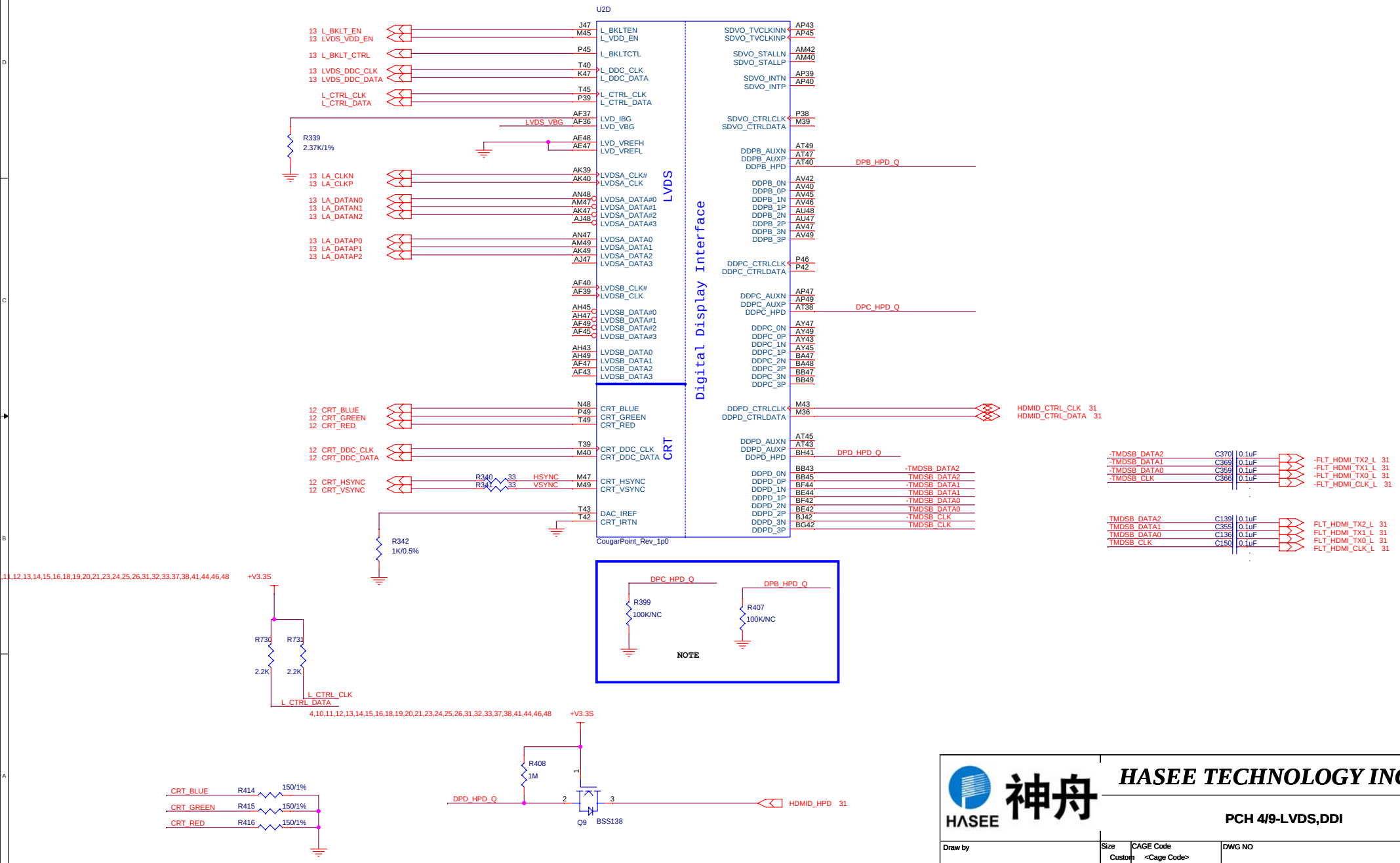

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PCH 4/9-LVDS,DDI

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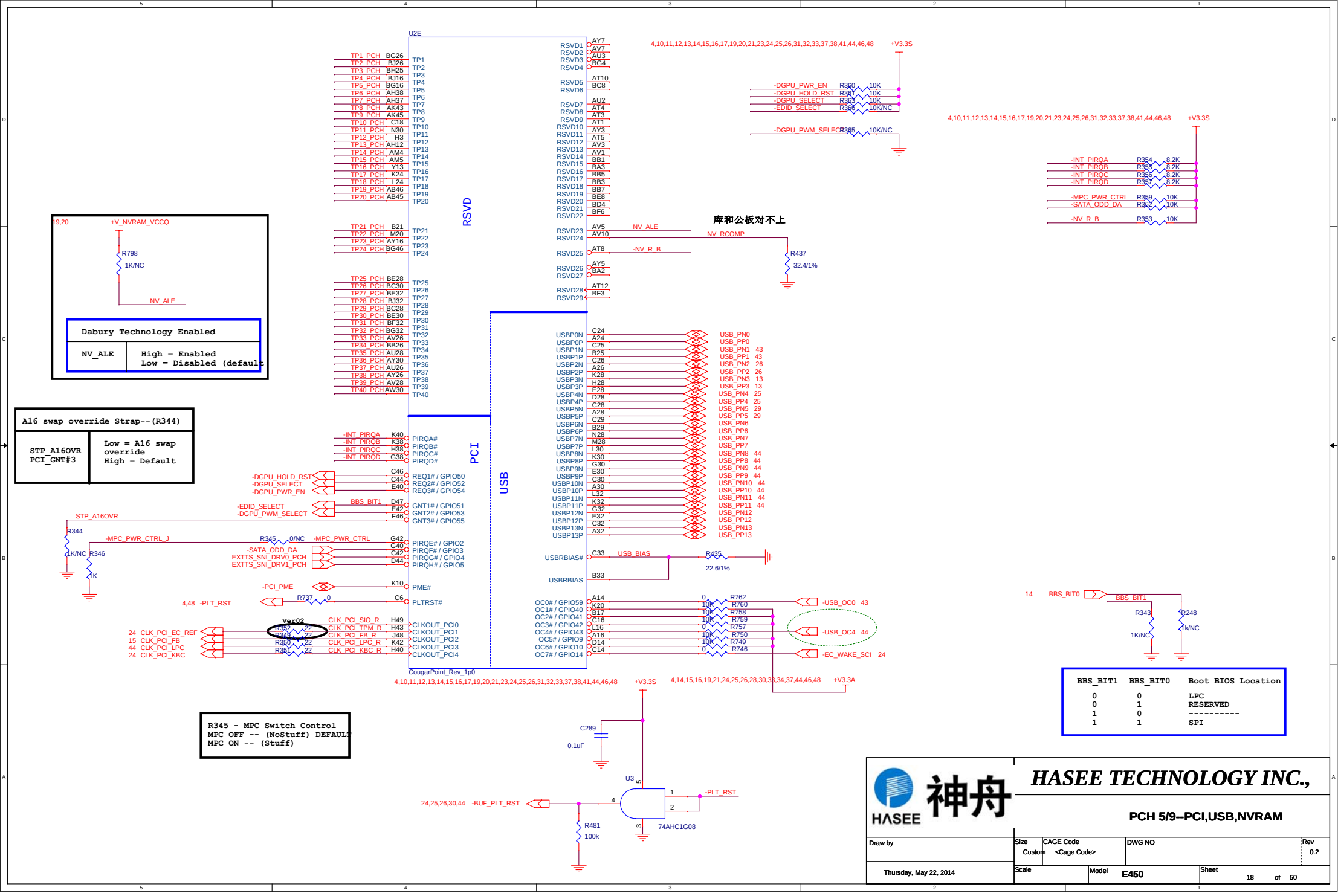

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PCH 5/9--PCI,USB,NVRAM

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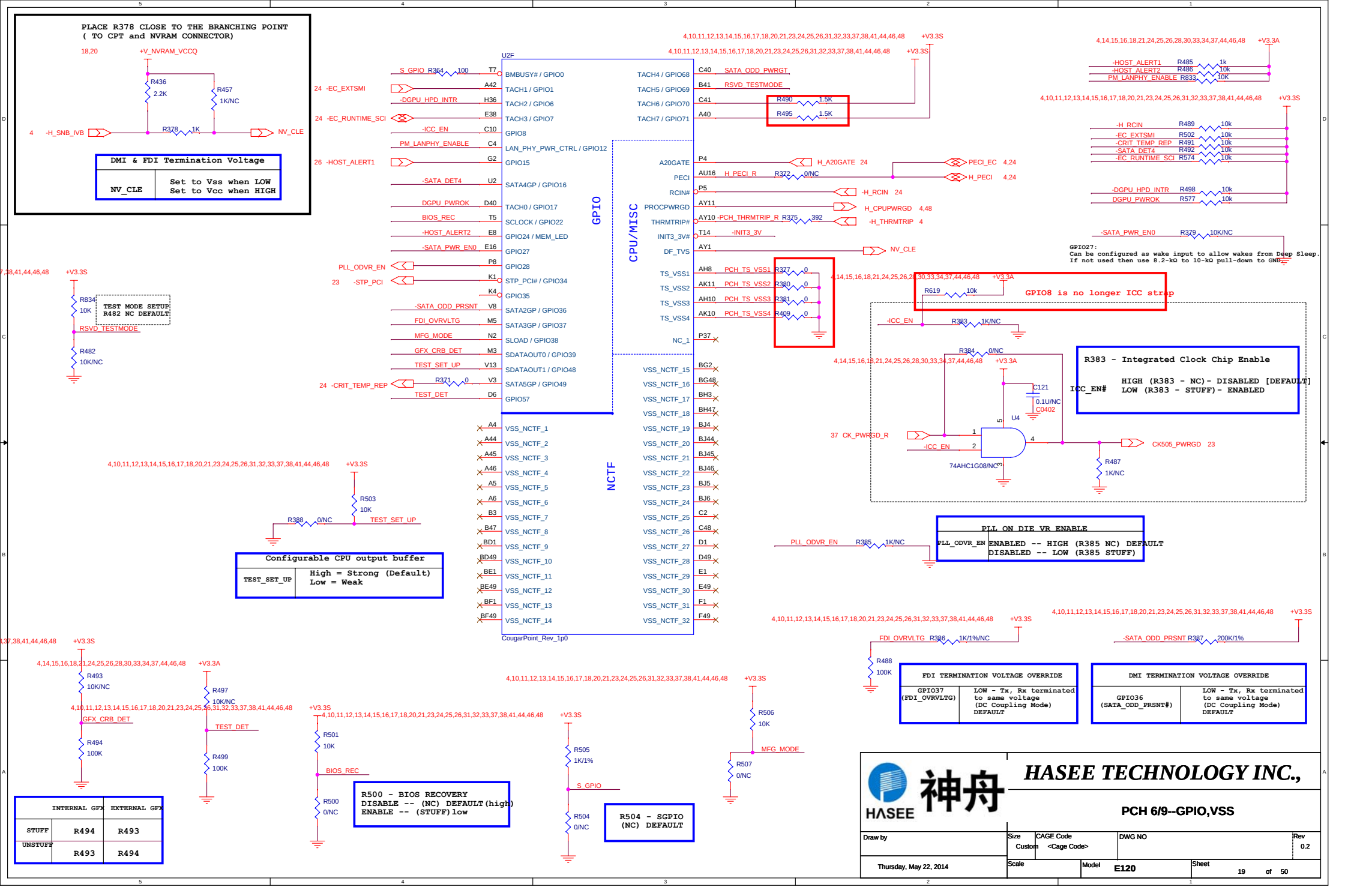
PLACE R378 CLOSE TO THE BRANCHING POINT
(TO CPT and NVRAM CONNECTOR)
DMI & FDI Termination Voltage
NV_CLE
Set to Vss when LOW
Set to Vcc when HIGH
U2F
GPIO
CPU/MISC
NCTF
CougarPoint_Rev_1p0
GPIO8 is no longer ICC strap
GPIO27:
Can be configured as wake input to allow wakes from Deep Sleep.
If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.
TEST MODE SETUP
R482 NC DEFAULT
R383 - Integrated Clock Chip Enable
HIGH (R383 - NC)- DISABLED [DEFAULT]
LOW (R383 - STUFF)- ENABLED
ICC_EN#
74AHC1G08/NC
PLL ON DIE VR ENABLE
PLL_ODVR_EN
ENABLED -- HIGH (R385 NC) DEFAULT
DISABLED -- LOW (R385 STUFF)
Configurable CPU output buffer
TEST_SET_UP
High = Strong (Default)
Low = Weak
FDI TERMINATION VOLTAGE OVERRIDE
GPIO37
(FDI_OVRVLTG)
LOW - Tx, Rx terminated
to same voltage
(DC Coupling Mode)
DEFAULT
DMI TERMINATION VOLTAGE OVERRIDE
GPIO36
(SATA_ODD_PRSNT#)
LOW - Tx, Rx terminated
to same voltage
(DC Coupling Mode)
DEFAULT
R500 - BIOS RECOVERY
DISABLE -- (NC) DEFAULT(high)
ENABLE -- (STUFF)low
R504 - SGPIO
(NC) DEFAULT
INTERNAL GFX
EXTERNAL GFX
STUFF
UNSTUFF
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HASEE TECHNOLOGY INC.,
PCH 6/9--GPIO,VSS
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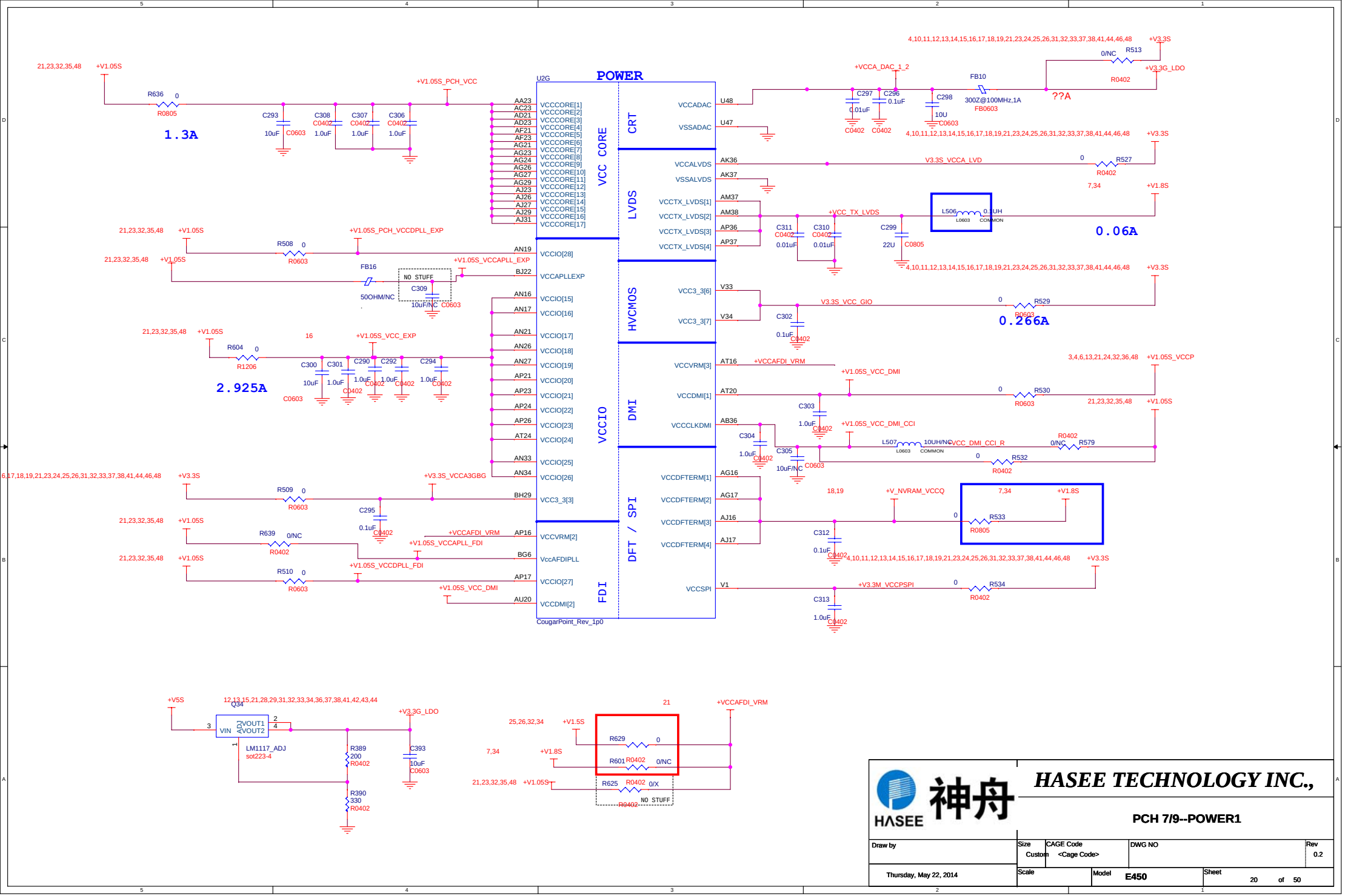

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PCH 7/9--POWER1

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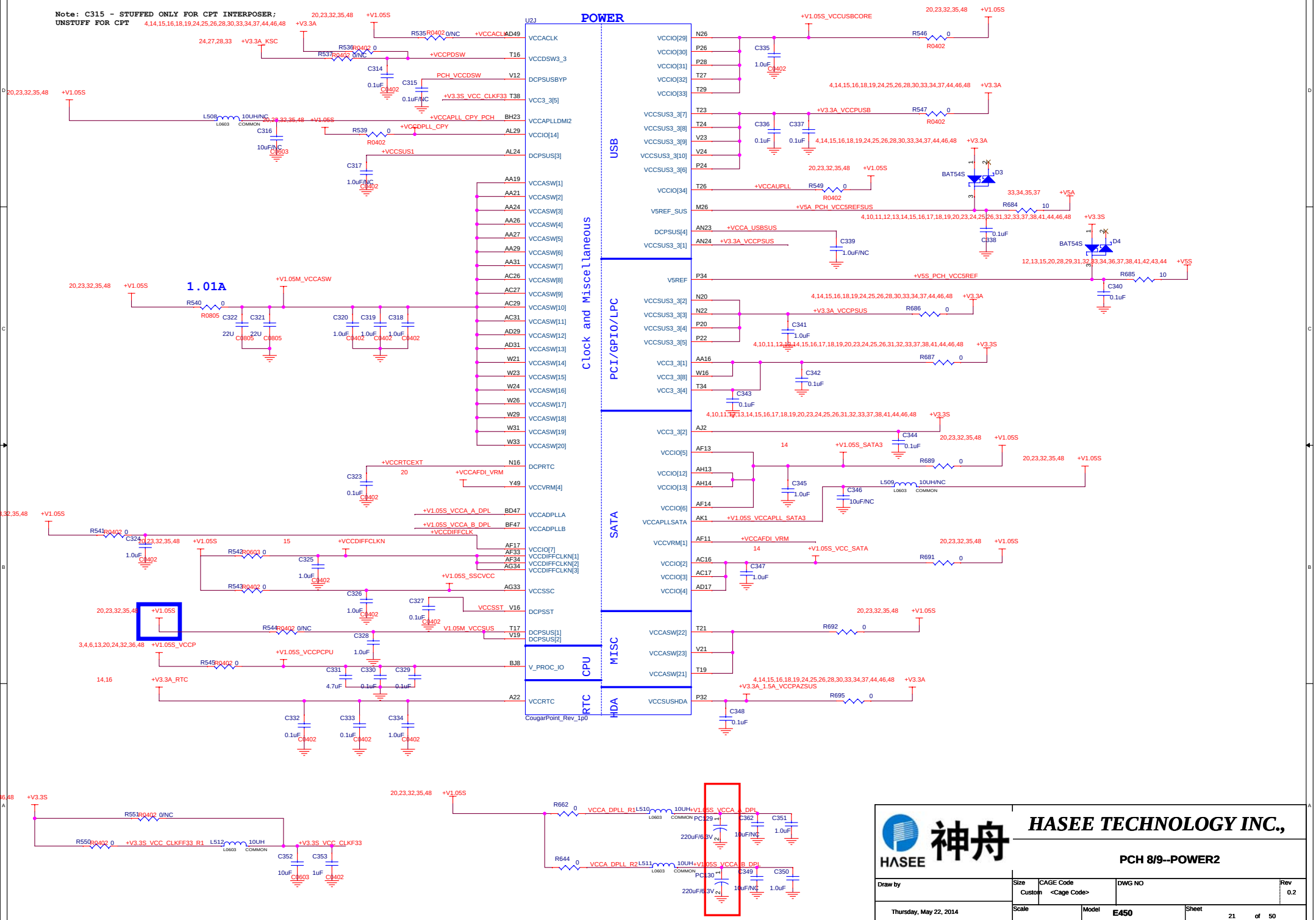

HASEE 神舟	HASEE TECHNOLOGY INC.,		
	PCH 8/9--POWER2		
Draw by	Size: Custom	CAGE Code: <Cage Code>	DWG NO	Rev: 0.2
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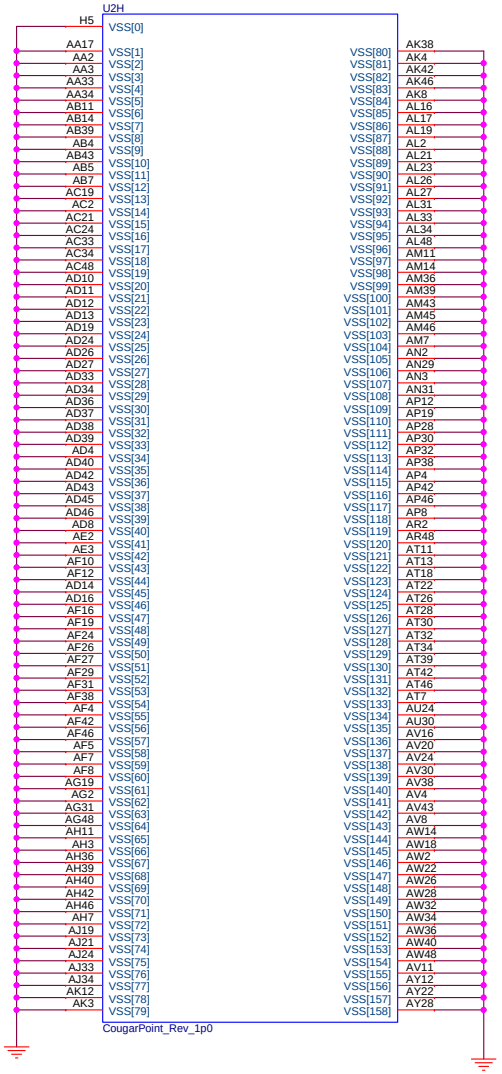

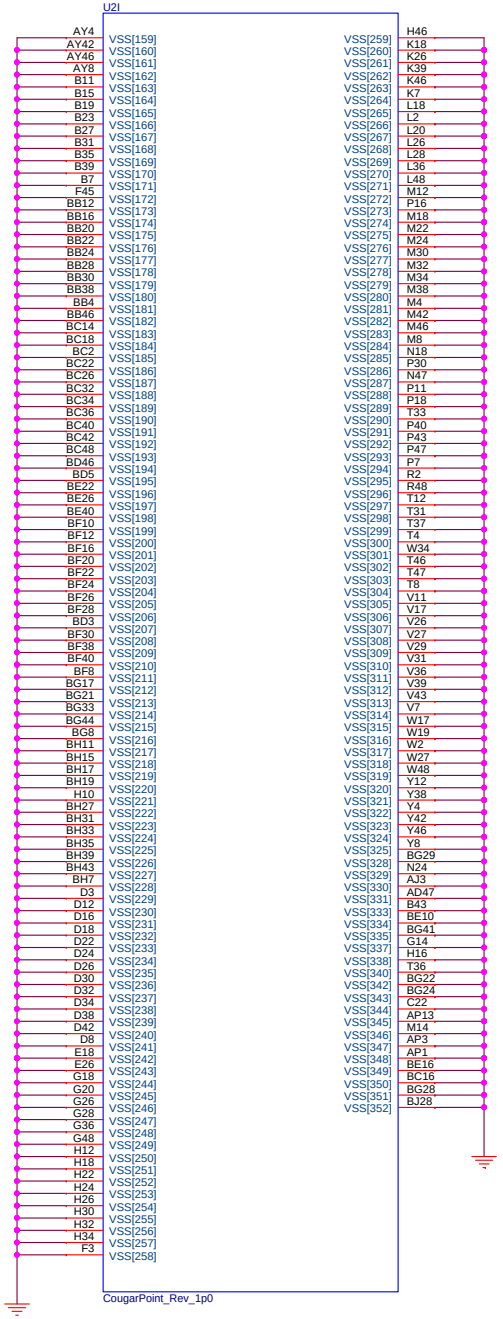

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PCH 9/9--VSS

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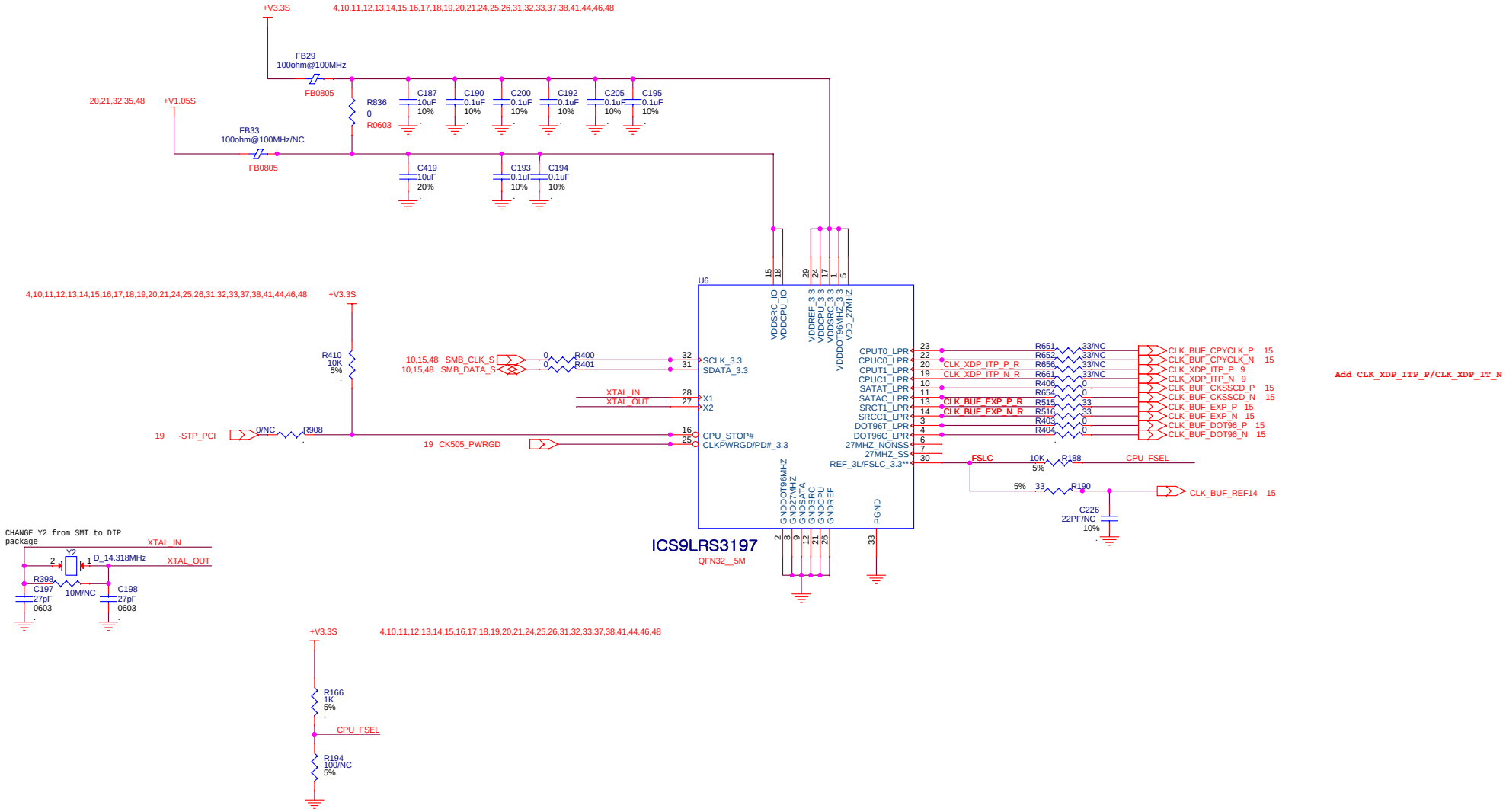

CPU frequency setting is 100 MHz

FSLC	CPU
0	133MHZ
1	100MHZ

0

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HASEE TECHNOLOGY INC.,

CK505

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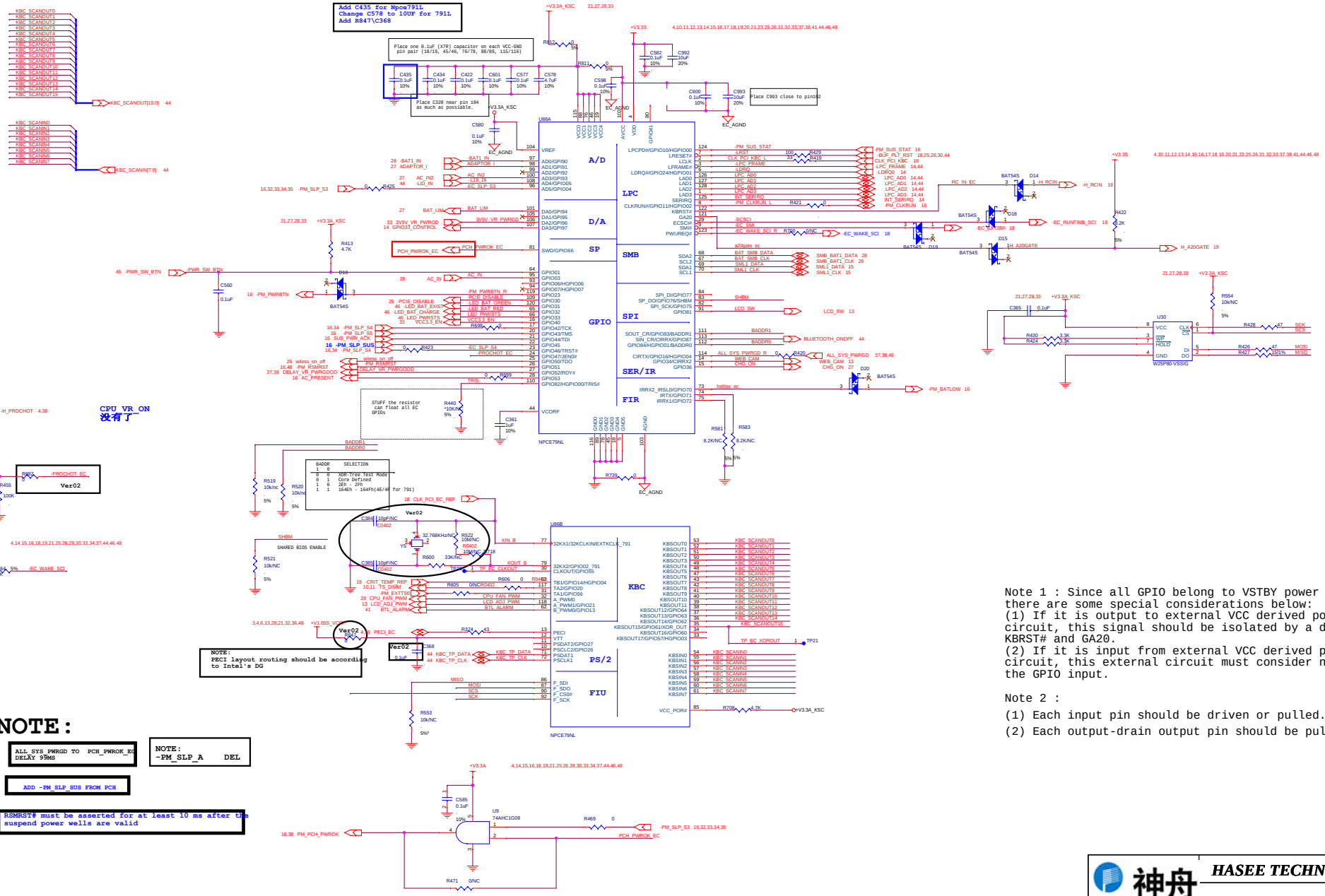

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

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EC

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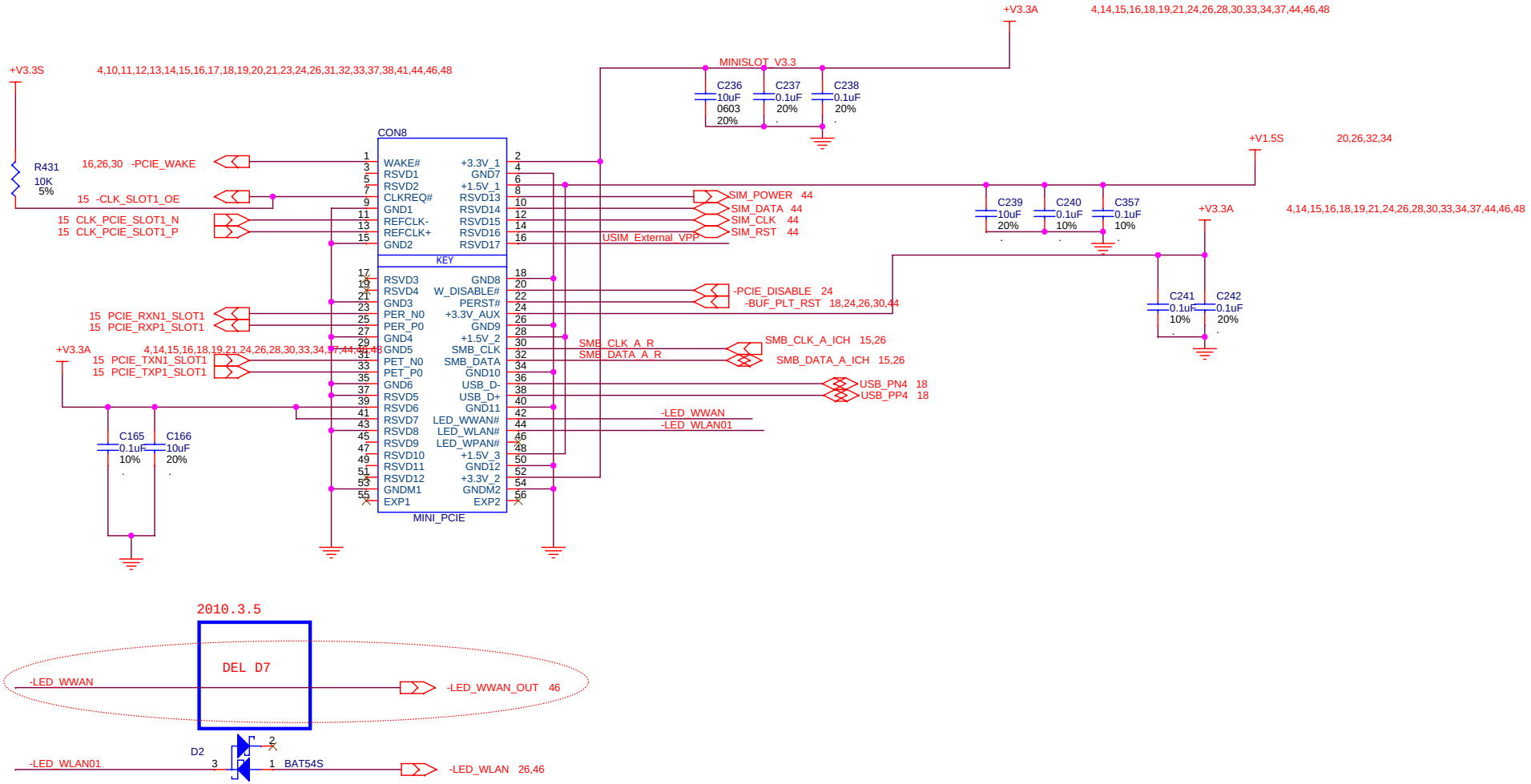

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	MiniPCI-E 1			
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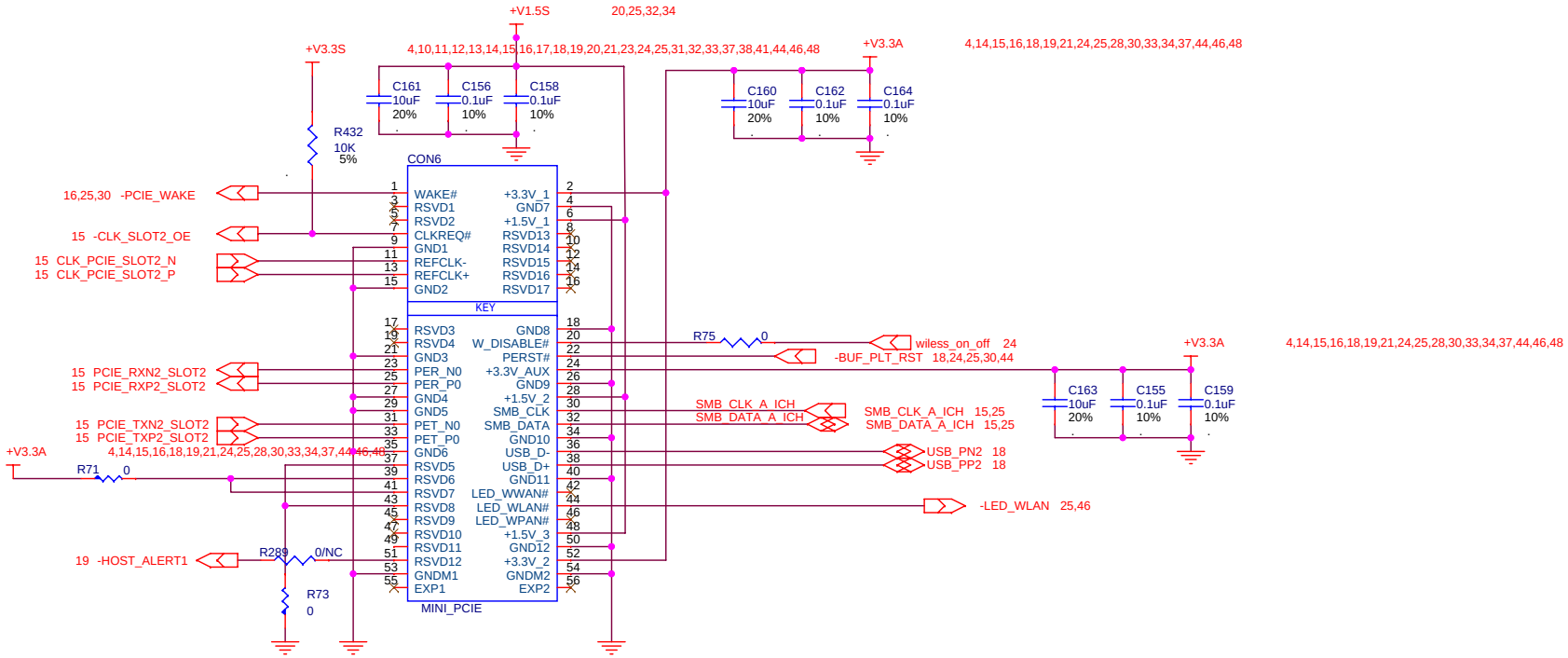

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MiniPCI-E 2

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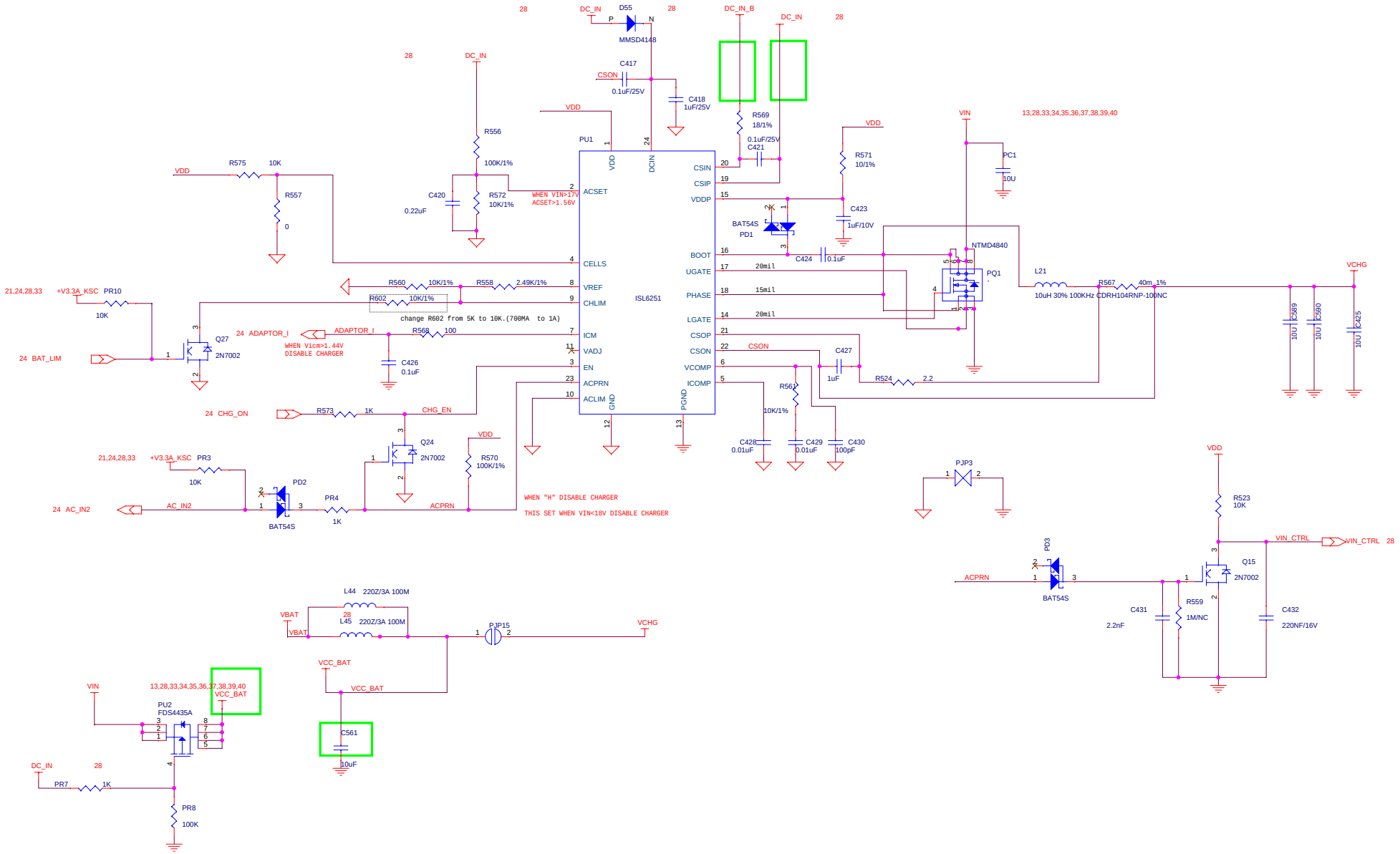

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CHARGE VR

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	Custom	<Cage Code>		0.2
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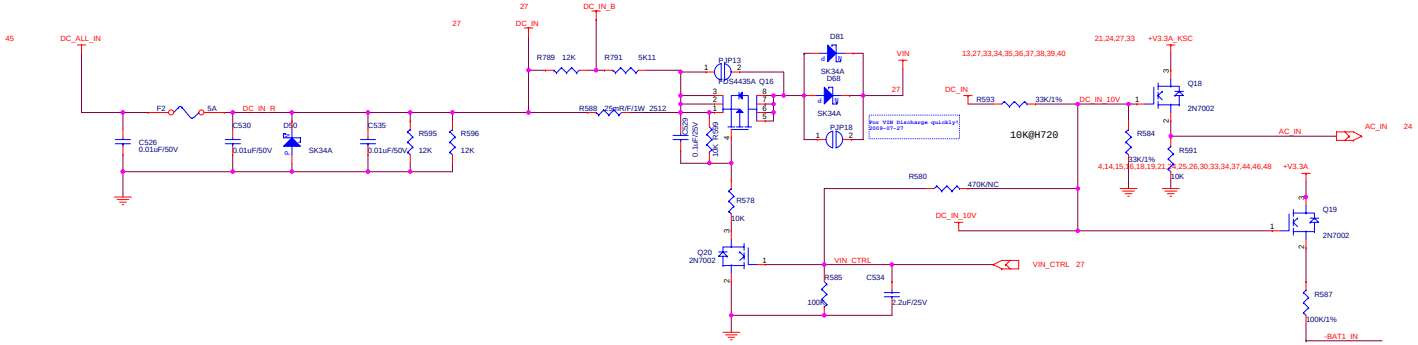
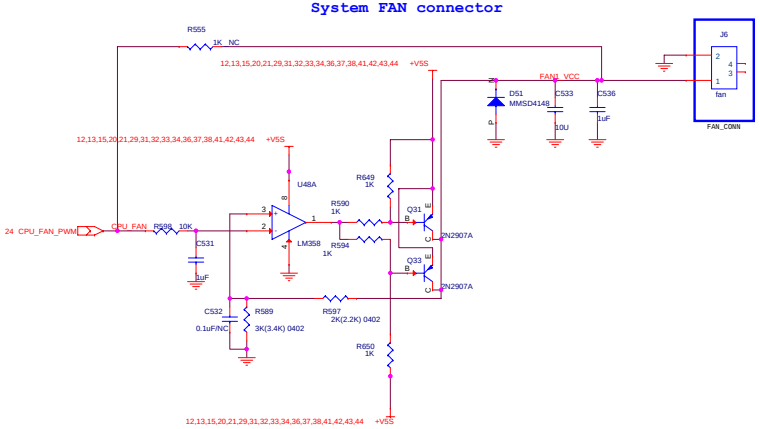
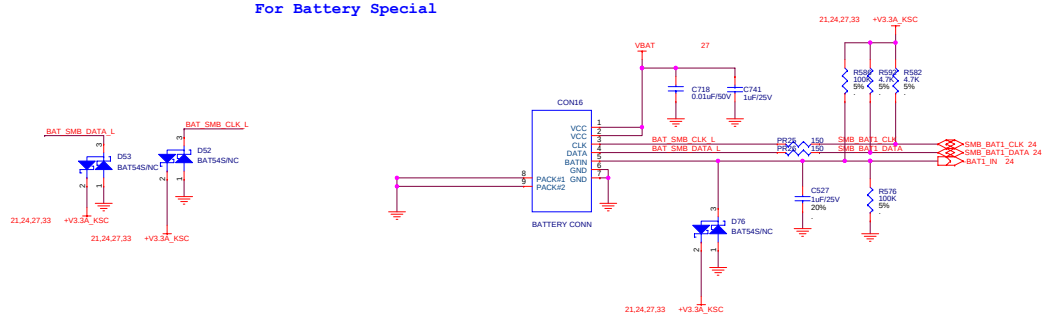


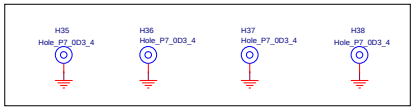
System FAN connector

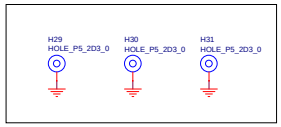


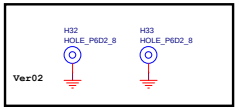
For Battery Special

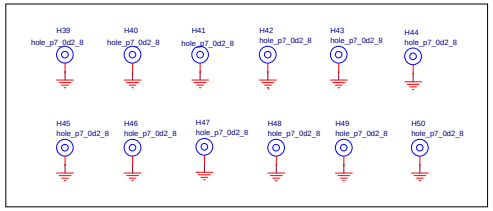


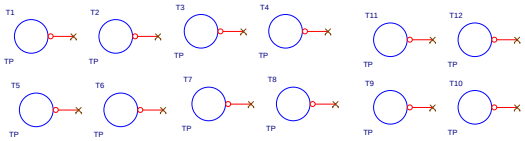
HOLE

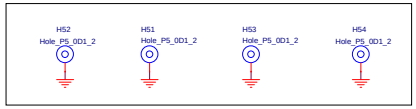












HASEE 神舟	HASEE TECHNOLOGY INC.,		
	DC-IN FAN BAT		
Draw by	Size: Custom	CAGE Code: <Cage Code>	DWG NO	Rev: 0.2
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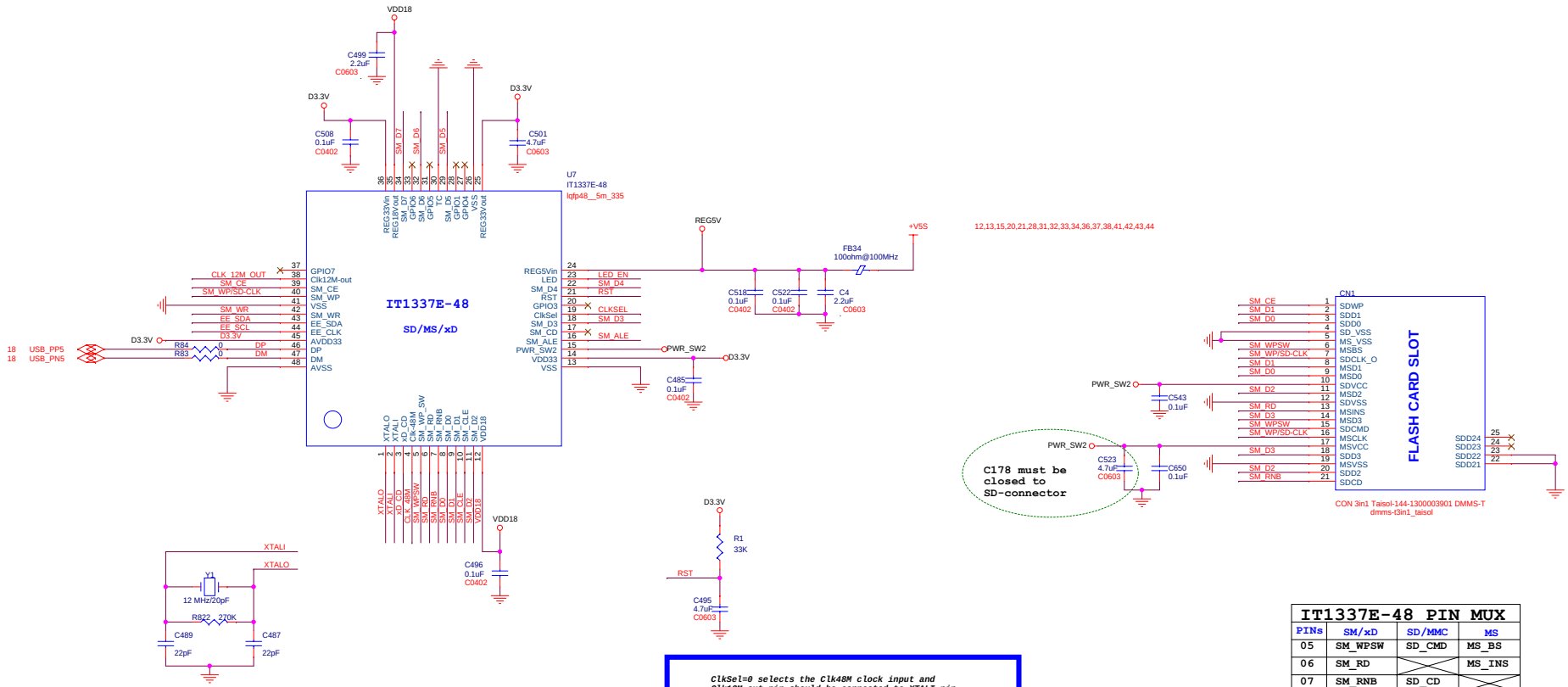
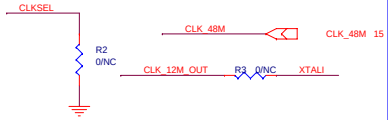
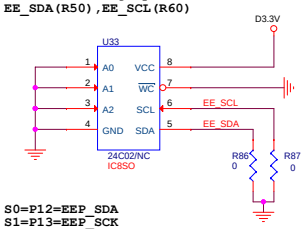


IT1337E-48 PIN MUX			
PINs	SM/xD	SD/MMC	MS
05	SM_WPSW	SD_CMD	MS_BS
06	SM_RD		MS_INS
07	SM_RNB	SD_CD	
08	SM_D0	SD_D0	MS_D0
09	SM_D1	SD_D1	MS_D1
11	SM_D2	SD_D2	MS_D2
18	SM_D3	SD_D3	MS_D3
22	SM_D4	SD_D4	MS_D4
29	SM_D5	SD_D5	MS_D5
32	SM_D6	SD_D6	MS_D6
34	SM_D7	SD_D7	MS_D7
39	SM_CE	SD_WP	
40	SM_WP	SD_CLK	MS_CLK

ClkSel=0 selects the Clk48M clock input and Clk12M_out pin should be connected to XTALI pin.

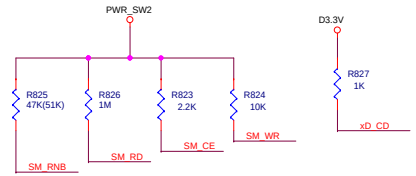


When mount EEPROM(U27)
Please remove jump
EE_SDA(R50),EE_SCL(R60)



S0=P12=EEP_SDA
S1=P13=EEP_SCK

1. Normal mode=11
   R60=NC,R50=NC
2. enable MS/xD Logo
   R60=0,R50=NC
3. Connector don't have SD_WP pin
   R60=0,R50=0



Reserved resistors to pass xD logo

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CARD READER

Draw by	Size	CAGE Code	DWG NO	Rev
	C	<Cage Code>		0.2
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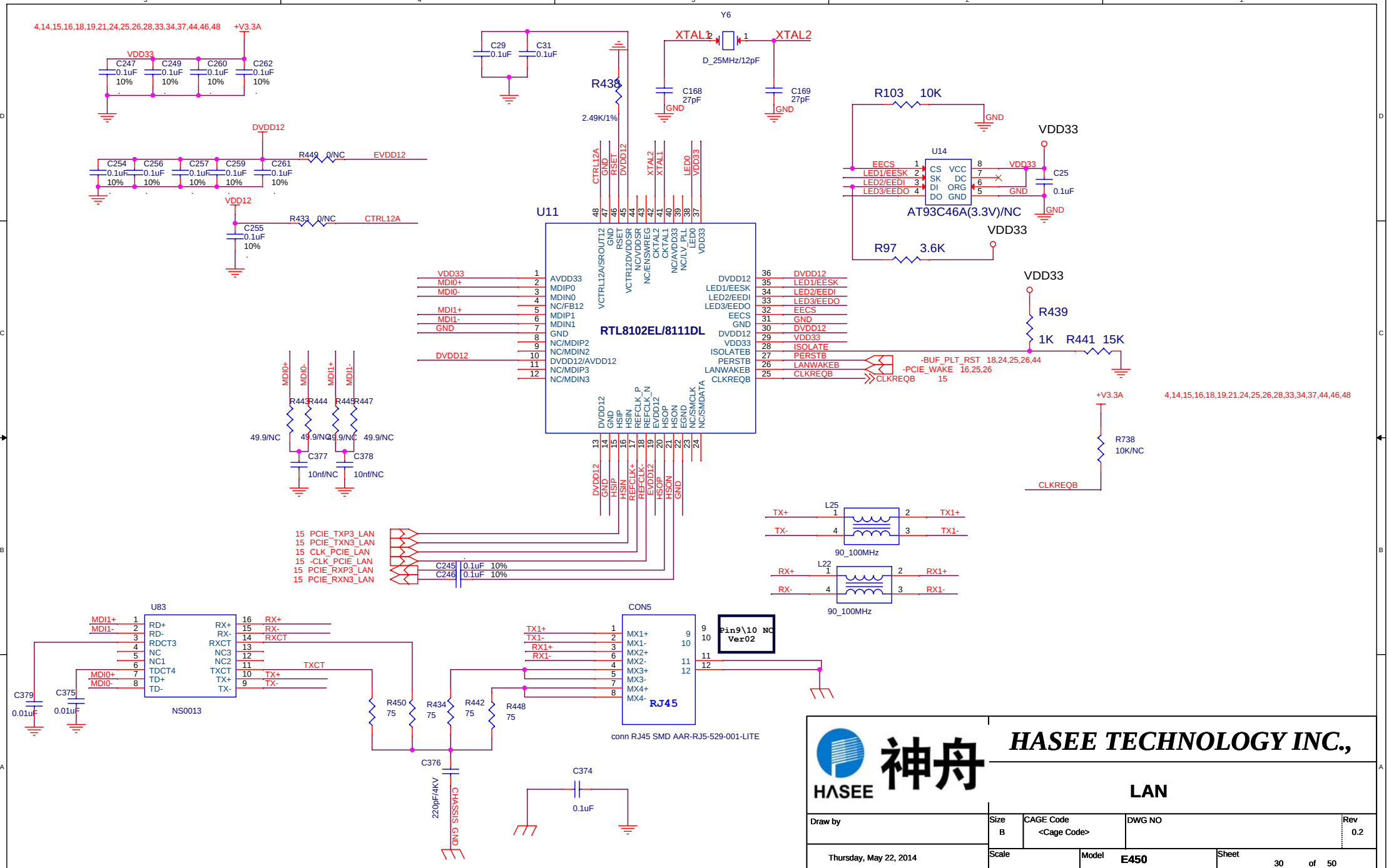
4,14,15,16,18,19,21,24,25,26,28,33,34,37,44,46,48
+V3.3A
VDD33
C247 0.1uF 10%
C249 0.1uF 10%
C260 0.1uF 10%
C262 0.1uF 10%
DVDD12
C254 0.1uF 10%
C256 0.1uF 10%
C257 0.1uF 10%
C259 0.1uF 10%
C261 0.1uF 10%
R449 0/NC
EVDD12
VDD12
C255 0.1uF 10%
R433 0/NC
CTRL12A
C29 0.1uF
C31 0.1uF
R438
2.49K/1%
Y6
XTAL1
XTAL2
D_25MHz/12pF
C168 27pF
C169 27pF
GND
R103 10K
U14
EECS
LED1/EESK
LED2/EEDI
LED3/EEDO
CS VCC
SK DC
DI ORG
DO GND
AT93C46A(3.3V)/NC
C25 0.1uF
R97 3.6K
U11
RTL8102EL/8111DL
AVDD33
MDIP0
MDIN0
NC/FB12
MDIP1
MDIN1
GND
NC/MDIP2
NC/MDIN2
DVDD12/AVDD12
NC/MDIP3
NC/MDIN3
DVDD12
LED1/EESK
LED2/EEDI
LED3/EEDO
EECS
GND
DVDD12
VDD33
ISOLATEB
PERSTB
LANWAKEB
CLKREQB
ISOLATE
PERSTB
LANWAKEB
CLKREQB
-BUF_PLT_RST 18,24,25,26,44
-PCIE_WAKE 16,25,26
CLKREQB 15
R439 1K
R441 15K
+V3.3A
4,14,15,16,18,19,21,24,25,26,28,33,34,37,44,46,48
R738 10K/NC
CLKREQB
MDI0+
MDI0-
MDI1+
MDI1-
R443 R444 R445 R447
49.9/NC
C377 10nf/NC
C378 10nf/NC
15 PCIE_TXP3_LAN
15 PCIE_TXN3_LAN
15 CLK_PCIE_LAN
15 -CLK_PCIE_LAN
15 PCIE_RXP3_LAN
15 PCIE_RXN3_LAN
C245 0.1uF 10%
C246 0.1uF 10%
L25
TX+
TX-
TX1+
TX1-
90_100MHz
L22
RX+
RX-
RX1+
RX1-
90_100MHz
U83
RD+
RD-
RDCT3
NC
NC1
TDCT4
TD+
TD-
RX+
RX-
RXCT
NC3
NC2
TXCT
TX+
TX-
NS0013
C379 0.01uF
C375 0.01uF
R450 75
R434 75
R442 75
R448 75
CON5
MX1+
MX1-
MX2+
MX2-
MX3+
MX3-
MX4+
MX4-
RJ45
Pin9\10 NC
Ver02
conn RJ45 SMD AAR-RJ5-529-001-LITE
C376 220pF/4KV
CHASSIS GND
C374 0.1uF
HASEE
神舟
HASEE TECHNOLOGY INC.,
LAN
Draw by
Size B
CAGE Code <Cage Code>
DWG NO
Rev 0.2
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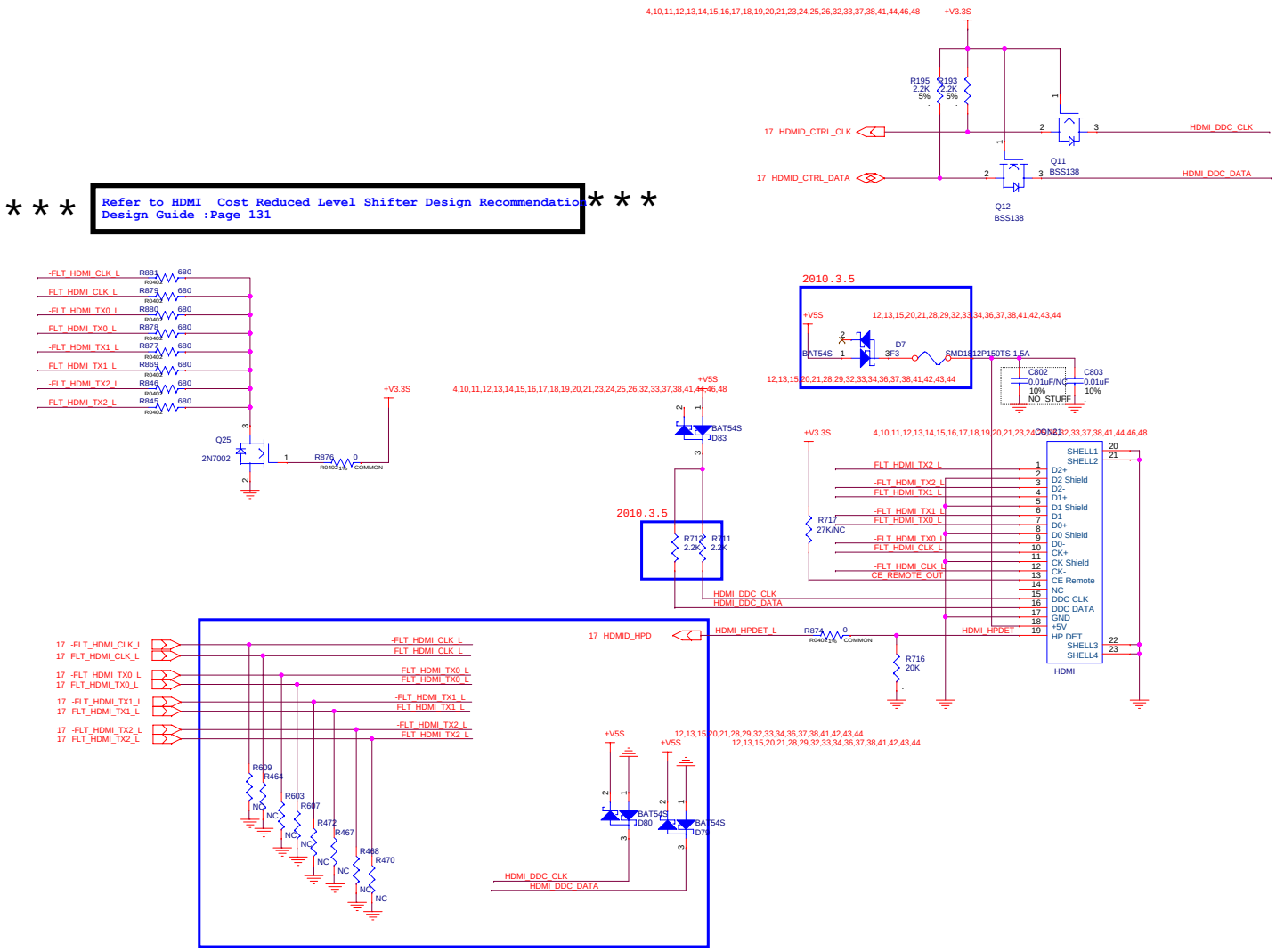
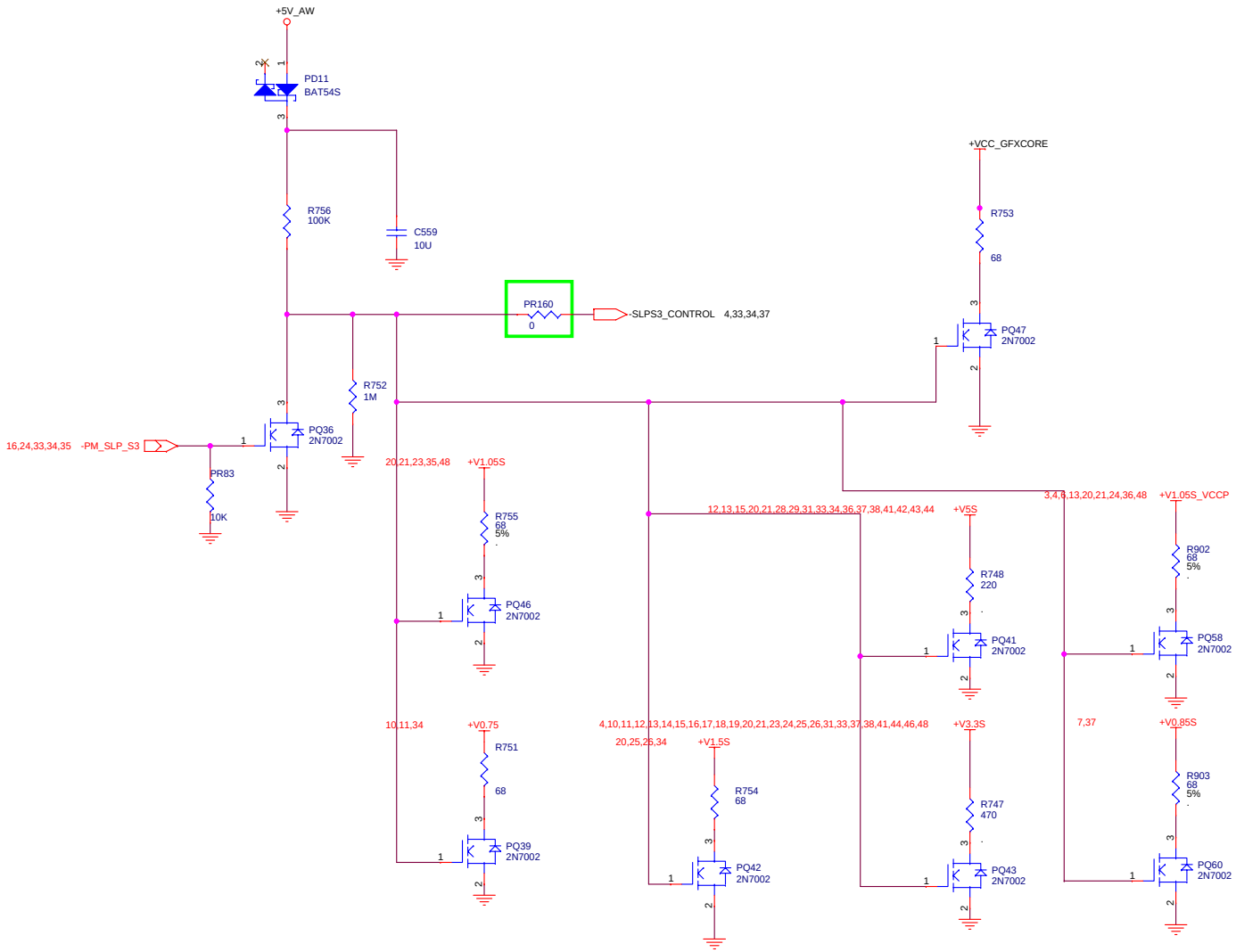

Refer to HDMI Cost Reduced Level Shifter Design Recommendation
Design Guide :Page 131
R195 2.2K 5%
R193 2.2K 5%
+V3.3S
17 HDMID_CTRL_CLK
17 HDMID_CTRL_DATA
HDMI_DDC_CLK
HDMI_DDC_DATA
Q11 BSS138
Q12 BSS138
-FLT_HDMI_CLK_L
FLT_HDMI_CLK_L
-FLT_HDMI_TX0_L
FLT_HDMI_TX0_L
-FLT_HDMI_TX1_L
FLT_HDMI_TX1_L
-FLT_HDMI_TX2_L
FLT_HDMI_TX2_L
Q25 2N7002
R876 0
2010.3.5
+V5S
BAT54S
D7 3F3
SMD1812P150TS-1.5A
C802 0.01uF/NC 10% NO_STUFF
C803 0.01uF 10%
R712 2.2K
R711 2.2K
R717 27K/NC
CON21
HDMI
HDMI_HPDET_L
HDMI_HPDET
17 HDMID_HPD
R716 20K
R874 0
R609 R464 R603 R607 R472 R467 R468 R470
NC



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HASEE TECHNOLOGY INC.,

SLEEP CONTRON/DISCHARGE

Draw by	Size: Custom	CAGE Code: <Cage Code>	DWG NO	Rev: 0.2
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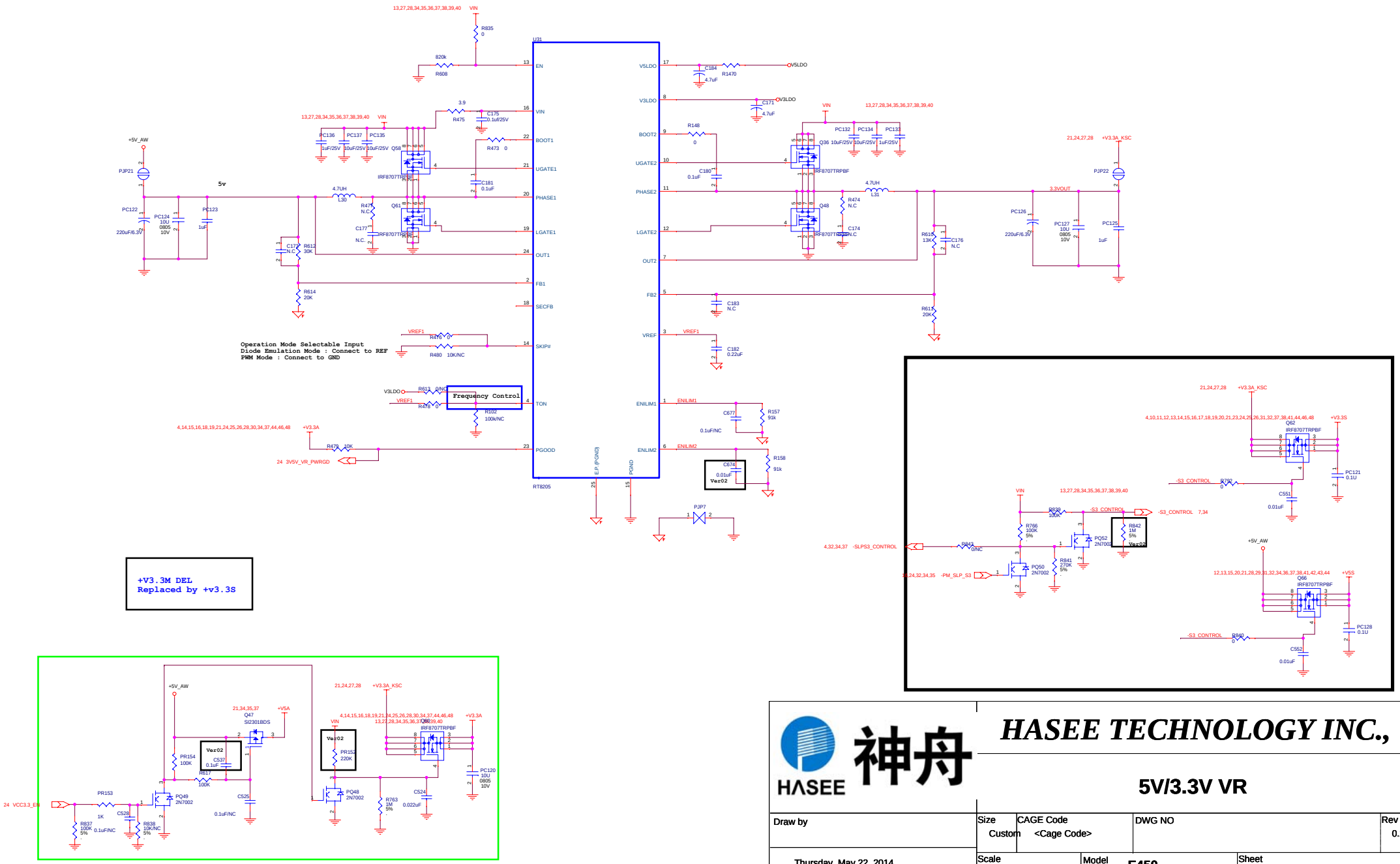

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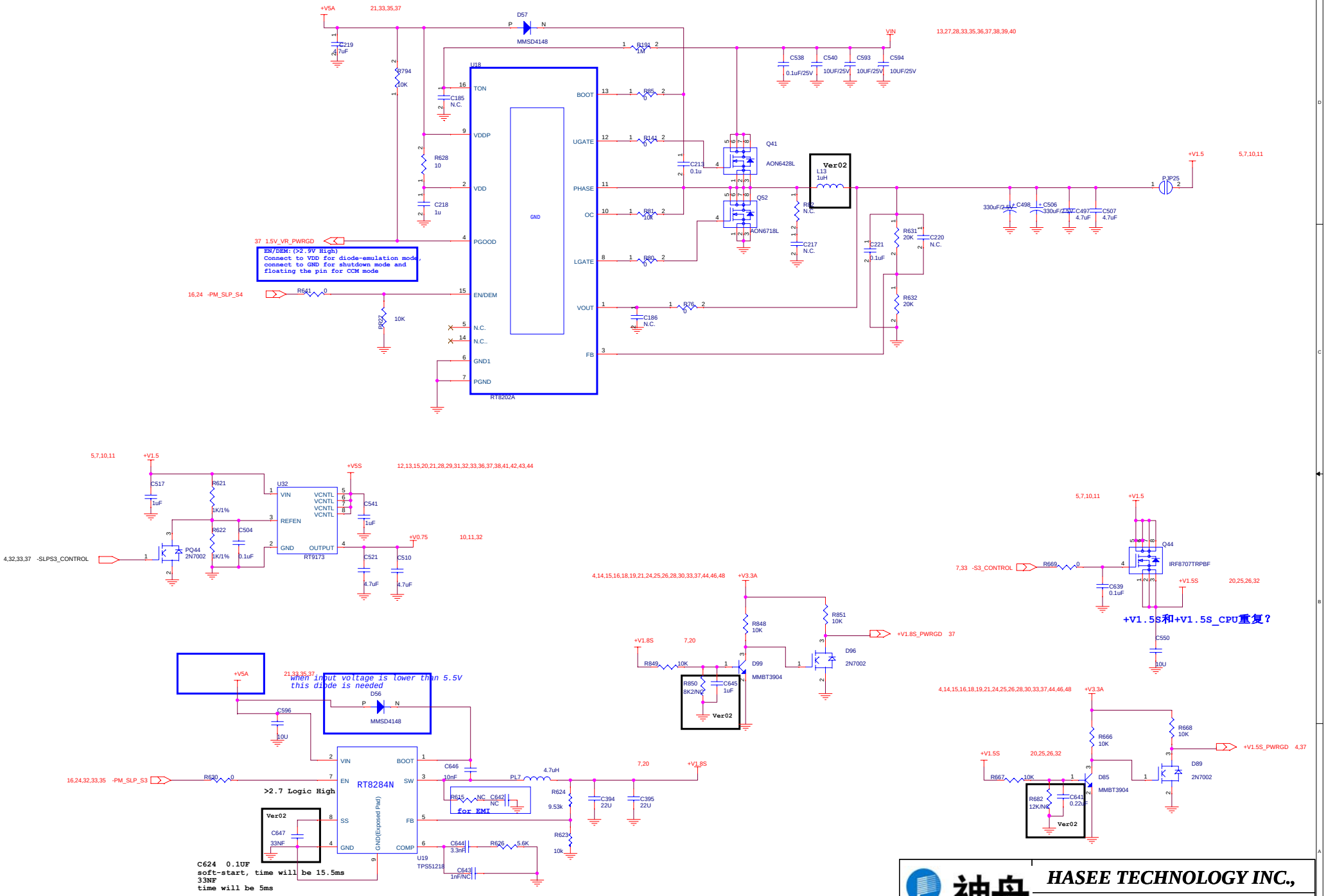
HASEE TECHNOLOGY INC.,

5V/3.3V VR

Draw by	Size	CAGE Code	DWG NO	Rev
	Custom	<Cage Code>		0.2
Thursday, May 22, 2014	Scale	Model E450	Sheet 33 of 50	



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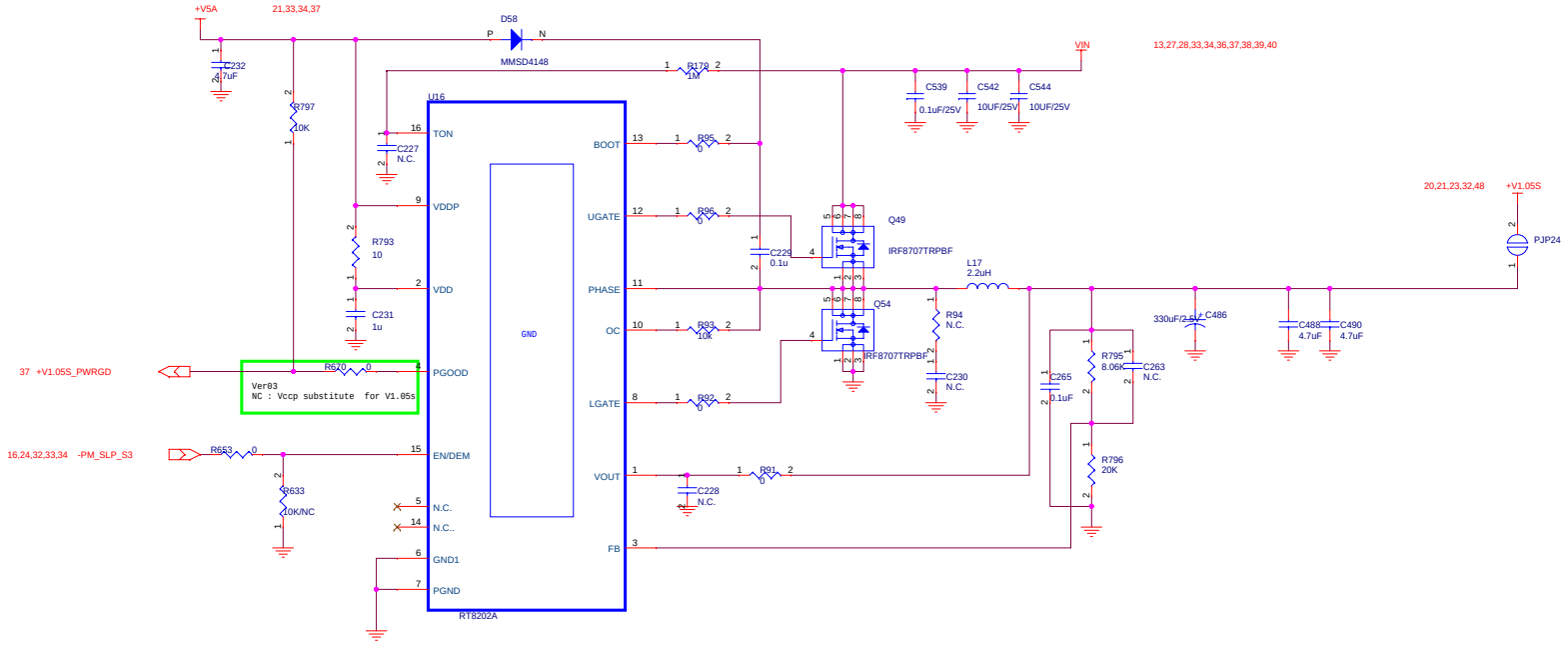
HASEE TECHNOLOGY INC.,

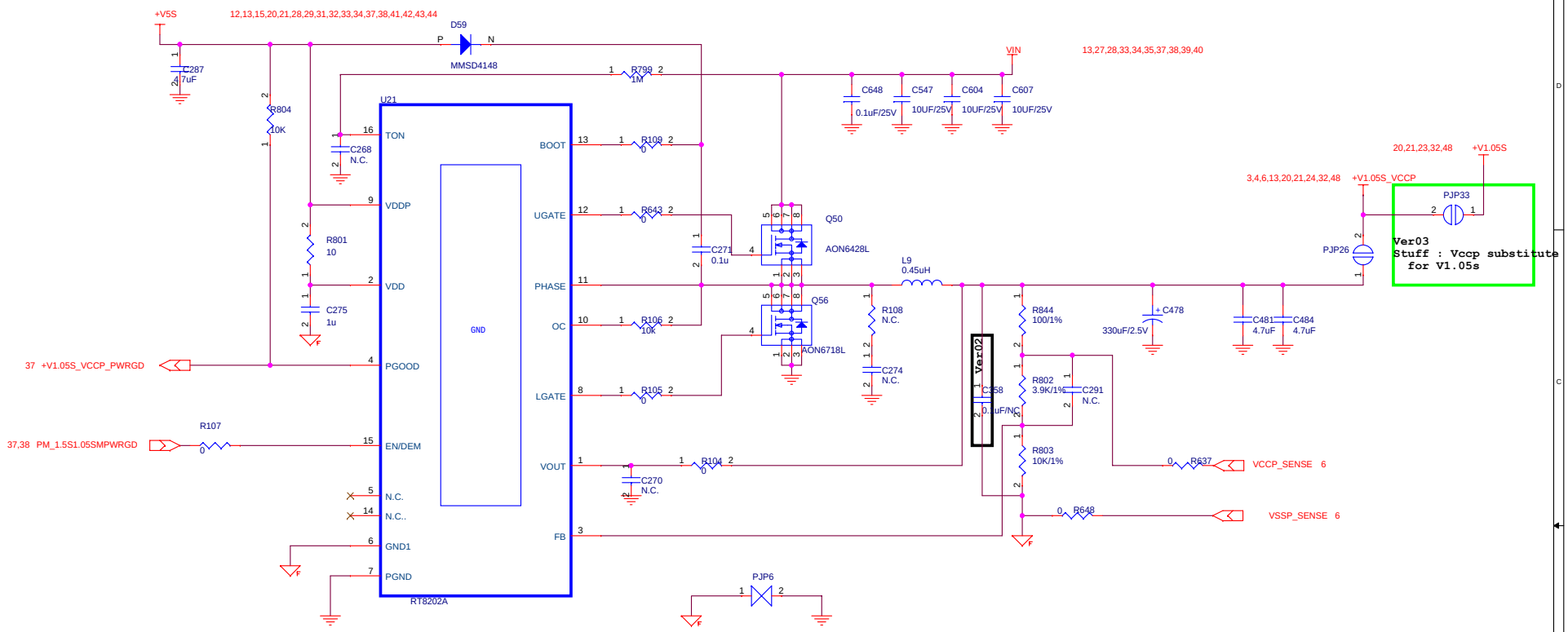
DDR VR,VTT,1.5S,1.8S

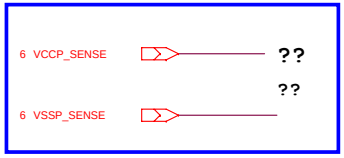
Draw by	Size	CAGE Code	DWG NO	Rev
	C	<Cage Code>		0.2
Thursday, May 22, 2014	Scale	Model E450	Sheet 34 of 50	



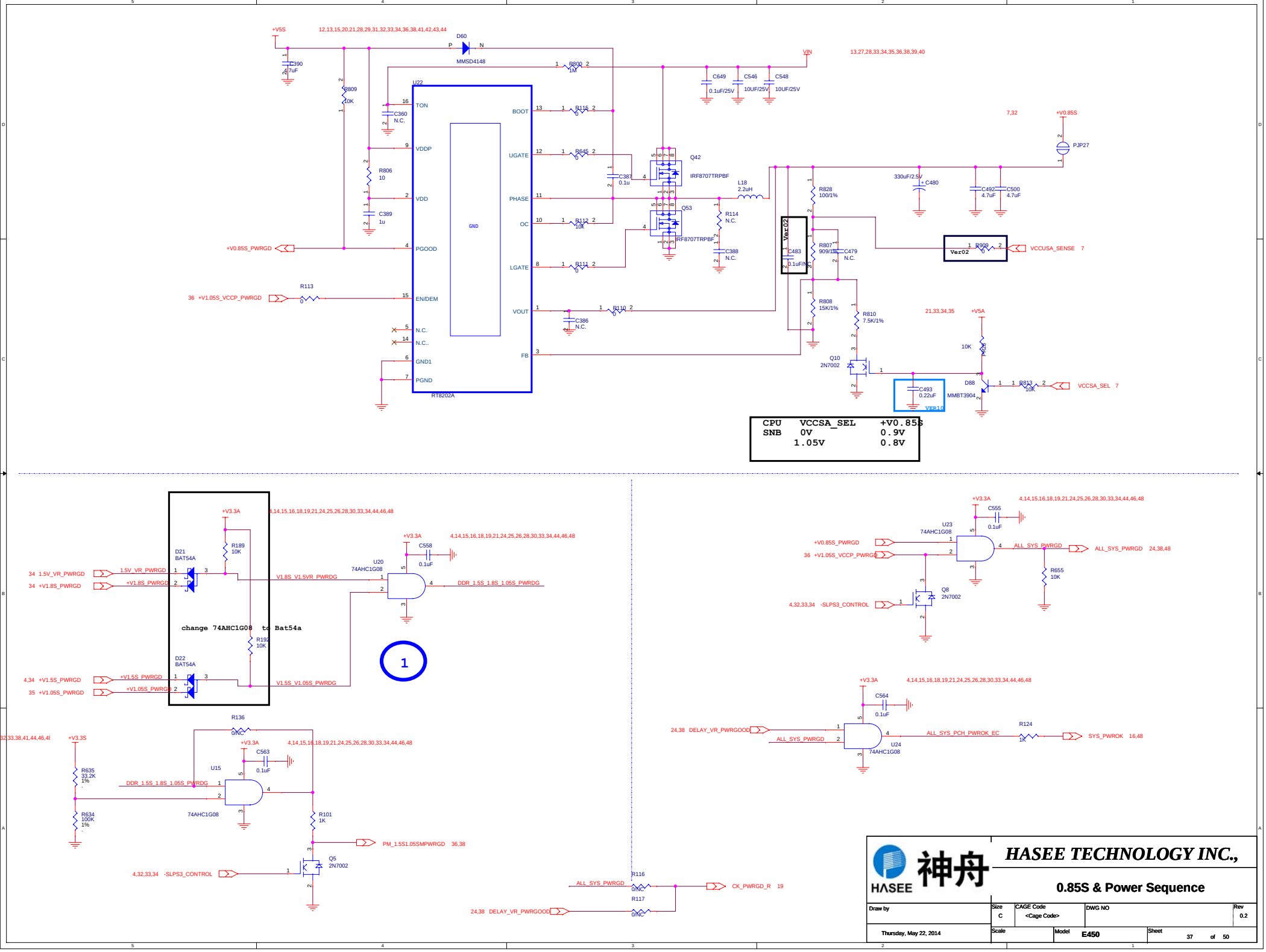
SLP_A is replaced by SLP_S3
Be controlled by SLP_S3# for platforms that don't support M3

HASEE 神舟	HASEE TECHNOLOGY INC.,			
	1.05M,1.05S			
Draw by	Size C	CAGE Code <Cage Code>	DWG NO	Rev 0.2
Thursday, May 22, 2014	Scale	Model E450	Sheet 35 of 50	





HASEE 神舟	HASEE TECHNOLOGY INC.,			
	1.05S_VCCP			
Draw by	Size: Custom	CAGE Code: <Cage Code>	DWG NO	Rev: 0.2
Thursday, May 22, 2014	Scale	Model: E450	Sheet: 36 of 50	



CPU	VCCSA_SEL	+V0.85S
SNB	0V	0.9V
	1.05V	0.8V

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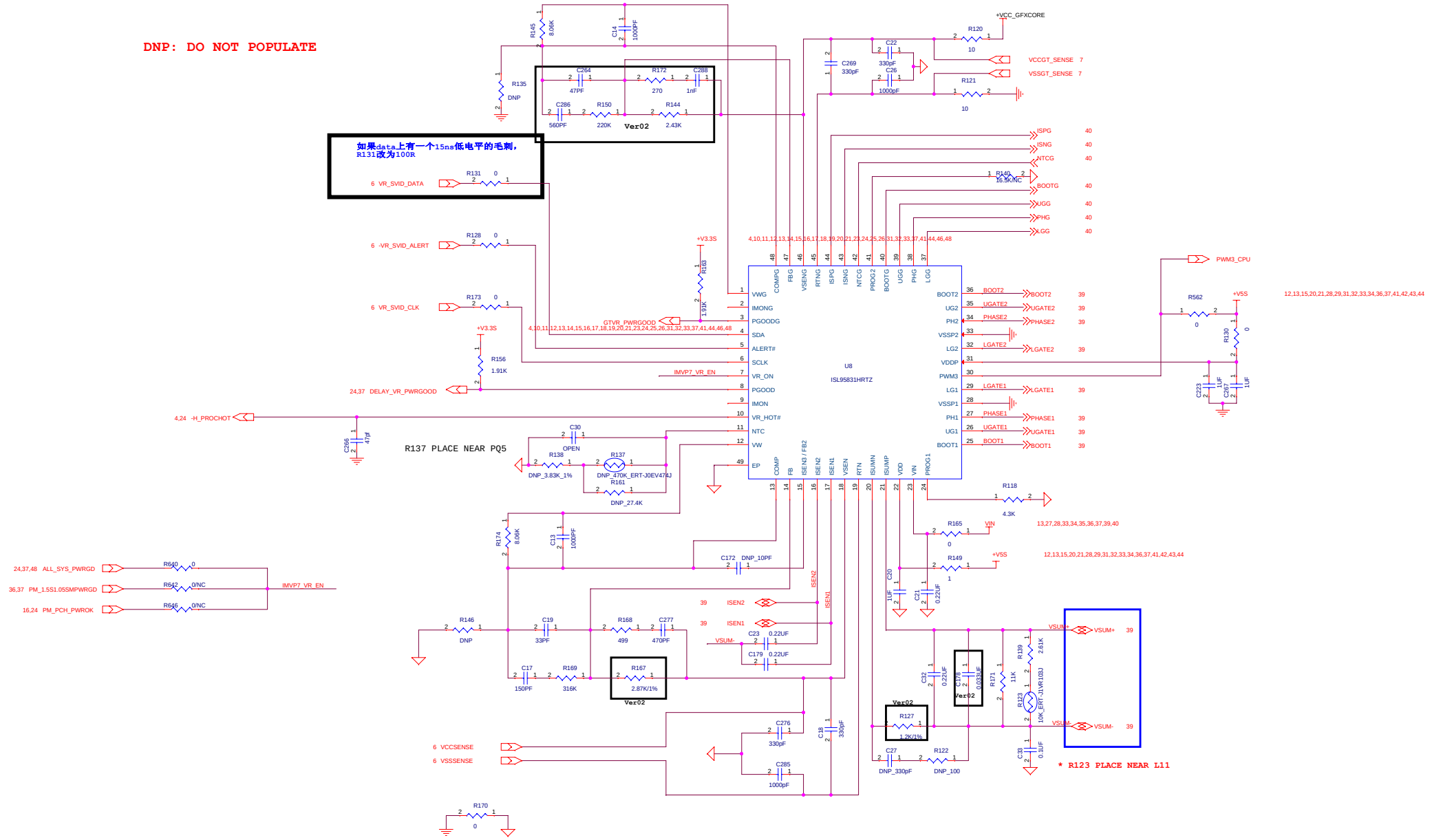
HASEE TECHNOLOGY INC.,

0.85S & Power Sequence

Draw by	Size	CAGE Code	DWG NO	Rev
	C	<Cage Code>		0.2
Thursday, May 22, 2014	Scale	Model E450	Sheet 37 of 50	



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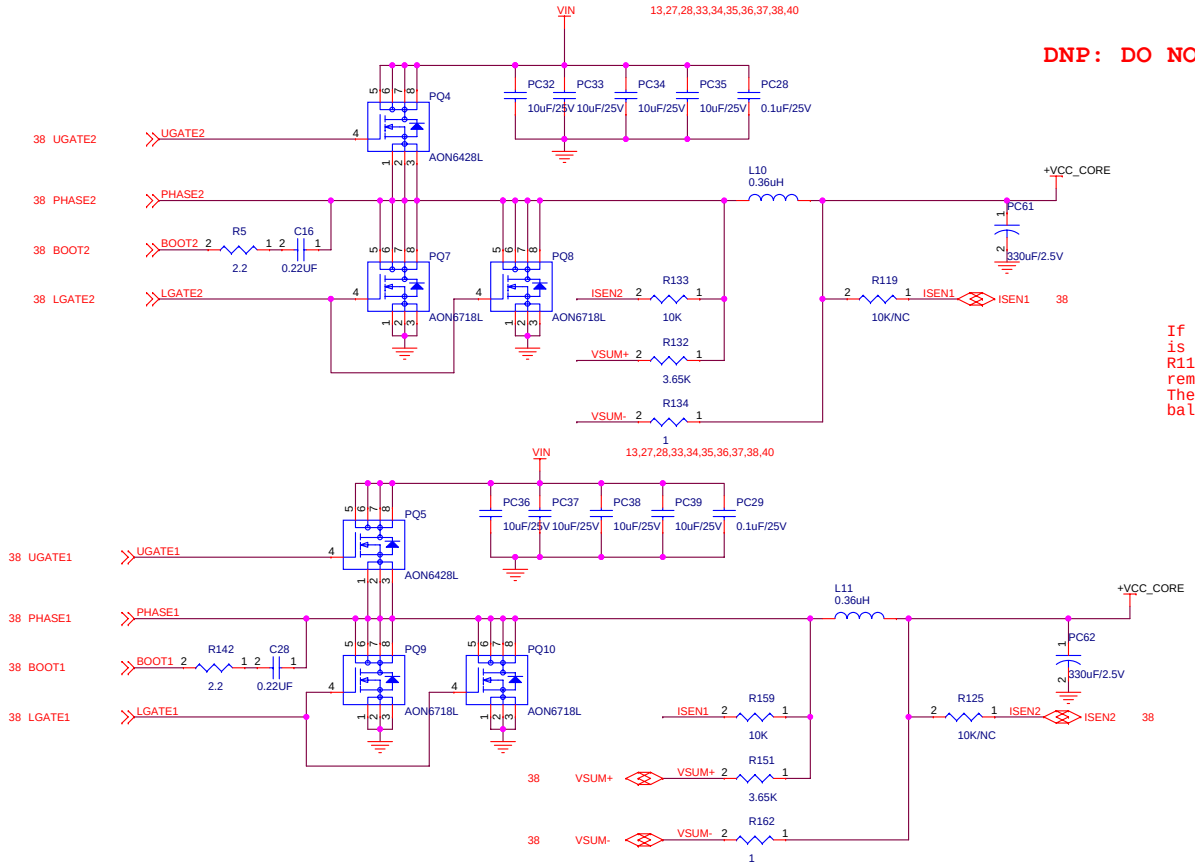
HASEE TECHNOLOGY INC.,

CPU VR1

Draw by	Size	CAGE Code	DWG NO	Rev
	Custom	<Cage Code>		0.2
Thursday, May 22, 2014	Scale	Model E450	Sheet 38 of 50	



DNP: DO NOT POPULATE

If the layout of each phase to CPU is symmetric.
R119,R160,R125,R164, can be removed.
They are used for phase current balance adjustment.

HASEE 神舟	**HASEE TECHNOLOGY INC.,**			
	CPU VR2			
Draw by	Size: Custom	CAGE Code: <Cage Code>	DWG NO	Rev: 0.2
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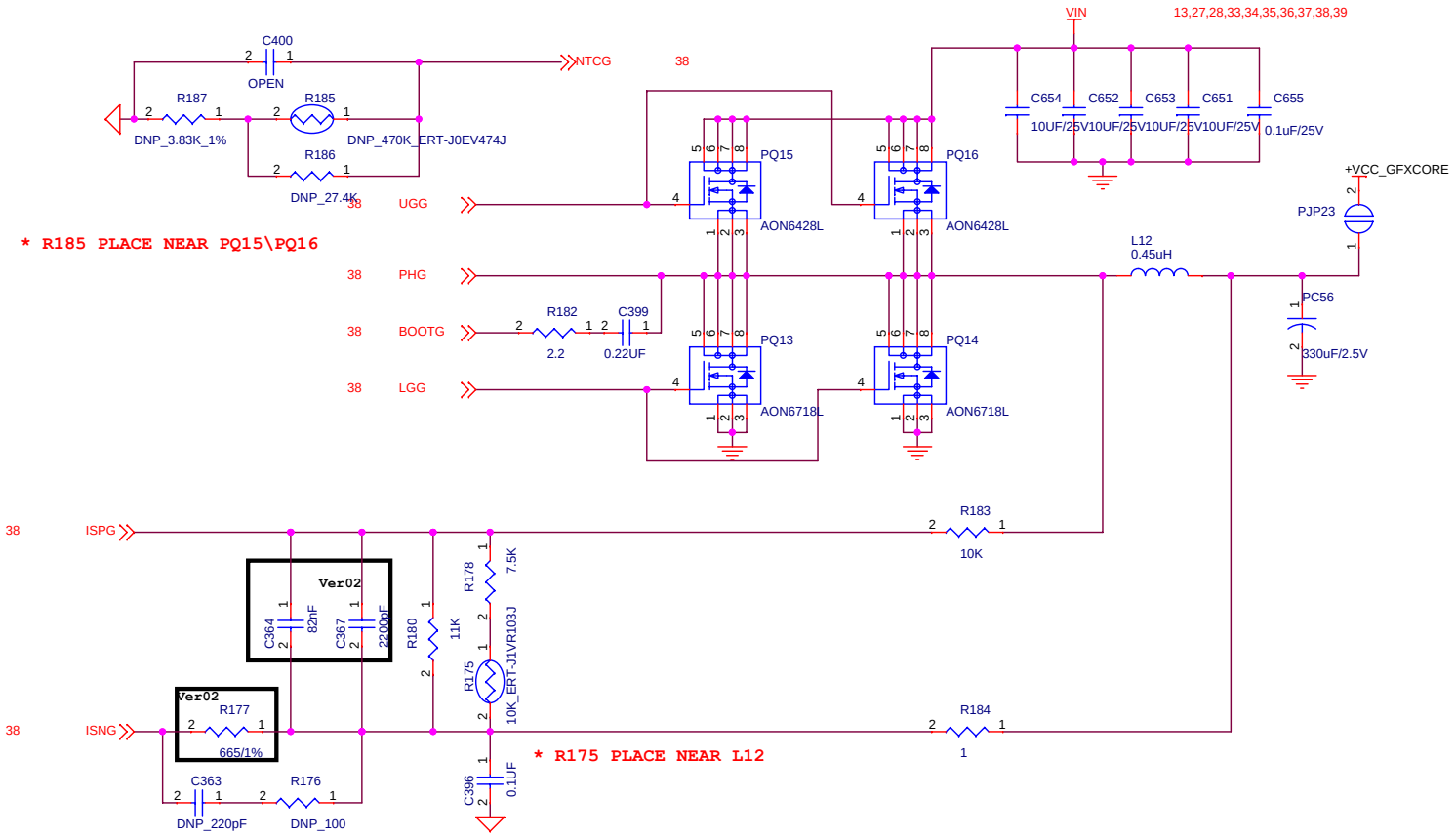

HASEE 神舟	HASEE TECHNOLOGY INC.,			
	Gforce VR			
Draw by	Size B	CAGE Code <Cage Code>	DWG NO	Rev 0.2
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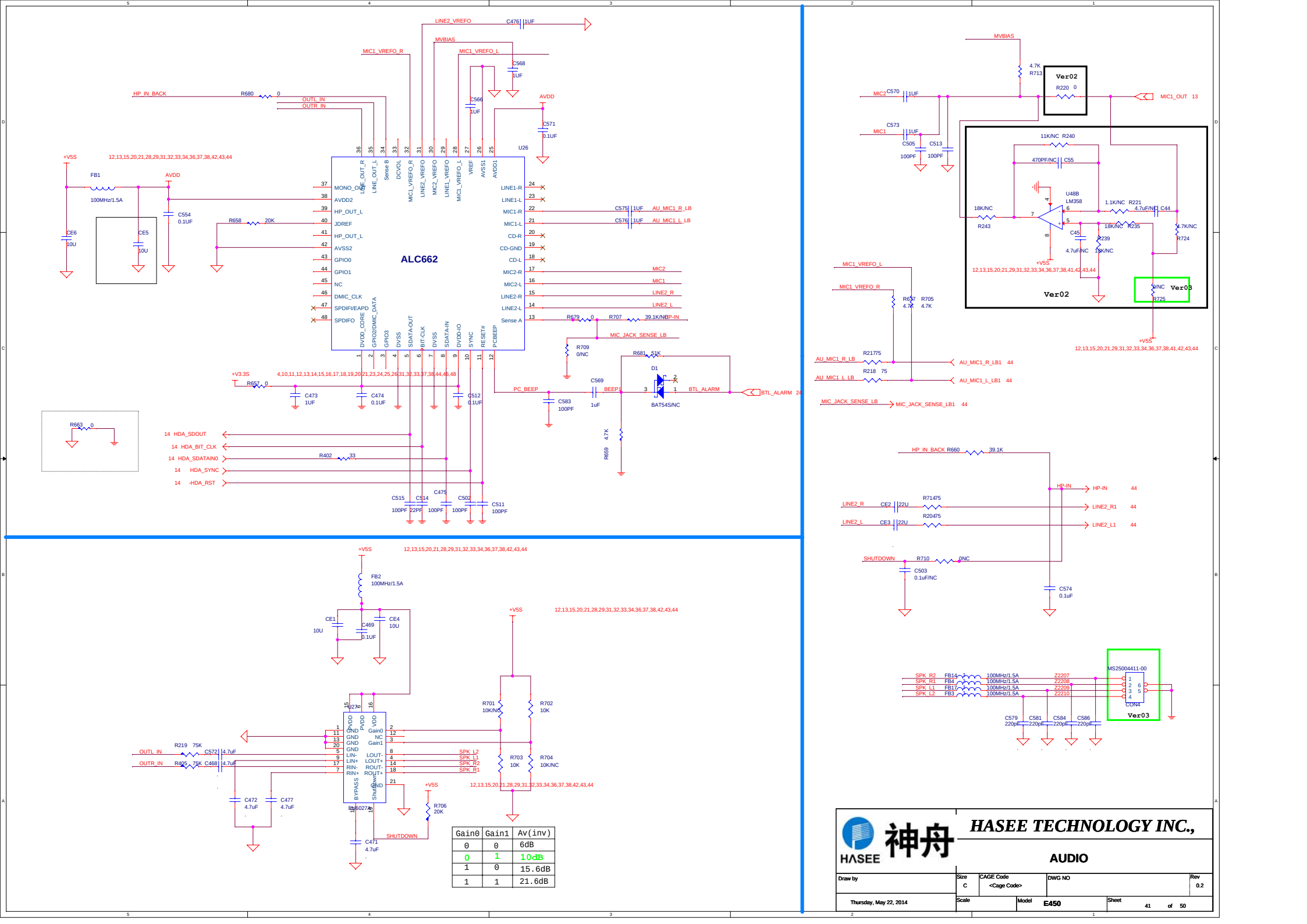
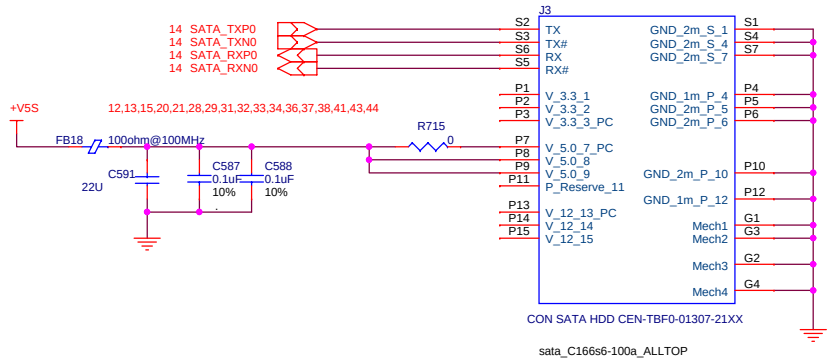

ALC662
U26
LINE2_VREFO
MVBIAS
MIC1_VREFO_R
MIC1_VREFO_L
HP_IN_BACK
OUTL_IN
OUTR_IN
AVDD
+V5S
12,13,15,20,21,28,29,31,32,33,34,36,37,38,42,43,44
FB1
100MHz/1.5A
CE6
10U
CE5
10U
C554
0.1UF
R658
20K
C575
1UF
AU_MIC1_R_LB
C576
1UF
AU_MIC1_L_LB
MIC2
MIC1
LINE2_R
LINE2_L
HP-IN
MIC_JACK_SENSE_LB
R679
0
R707
39.1K/NC
R709
0/NC
R681
51K
D1
BAT54S/NC
BTL_ALARM
BTL_ALARM 24
PC_BEEP
C569
BEEP1
C583
100PF
1uF
R659
4.7K
+V3.3S
4,10,11,12,13,14,15,16,17,18,19,20,21,23,24,25,26,31,32,33,37,38,44,46,48
R657
0
C473
1UF
C474
0.1UF
C512
0.1UF
R663
0
14 HDA_SDOUT
14 HDA_BIT_CLK
14 HDA_SDATAIN0
14 HDA_SYNC
14 -HDA_RST
R402
33
C515
100PF
C514
22PF
C475
100PF
C502
100PF
C511
100PF
C476
1UF
C568
1UF
C566
1UF
C571
0.1UF
MONO_OUT
AVDD2
HP_OUT_L
JDREF
HP_OUT_L
AVSS2
GPIO0
GPIO1
NC
DMIC_CLK
SPDIFI/EAPD
SPDIFO
LINE1-R
LINE1-L
MIC1-R
MIC1-L
CD-R
CD-GND
CD-L
MIC2-R
MIC2-L
LINE2-R
LINE2-L
Sense A
LINE_OUT_R
LINE_OUT_L
Sense B
DCVOL
MIC1_VREFO_R
LINE2_VREFO
MIC2_VREFO
LINE1_VREFO
MIC1_VREFO_L
VREF
AVSS1
AVDD1
DVDD_CORE
GPIO2/DMIC_DATA
GPIO3
DVSS
SDATA-OUT
BIT-CLK
DVSS
SDATA-IN
DVDD-IO
SYNC
RESET#
PCBEEP
MVBIAS
4.7K
R713
Ver02
R220
0
MIC2
C570
1UF
MIC1
C573
1UF
C505
100PF
C513
100PF
MIC1_OUT 13
11K/NC R240
470PF/NC C55
U48B
LM358
1.1K/NC R221
4.7uF/NC C44
18K/NC
R243
18K/NC R235
C45
4.7uF/NC
R239
18K/NC
4.7K/NC
R724
+V5S
12,13,15,20,21,29,31,32,33,34,36,37,38,41,42,43,44
Ver02
0/NC
R725
Ver03
+V5S
12,13,15,20,21,29,31,32,33,34,36,37,38,41,42,43,44
MIC1_VREFO_L
MIC1_VREFO_R
R637
4.7K
R705
4.7K
AU_MIC1_R_LB
R217/75
AU_MIC1_R_LB1 44
AU_MIC1_L_LB
R218 75
AU_MIC1_L_LB1 44
MIC_JACK_SENSE_LB
MIC_JACK_SENSE_LB1 44
HP_IN_BACK R660
39.1K
HP-IN
HP-IN 44
LINE2_R
CE2
22U
R71475
LINE2_R1 44
LINE2_L
CE3
22U
R20475
LINE2_L1 44
SHUTDOWN
R710
0NC
C503
0.1uF/NC
C574
0.1uF
SPK_R2
FB14
100MHz/1.5A
Z2207
SPK_R1
FB4
100MHz/1.5A
Z2208
SPK_L1
FB17
100MHz/1.5A
Z2209
SPK_L2
FB3
100MHz/1.5A
Z2210
MS25004411-00
CON4
Ver03
C579
220pF
C581
220pF
C584
220pF
C586
220pF
+V5S
12,13,15,20,21,28,29,31,32,33,34,36,37,38,42,43,44
FB2
100MHz/1.5A
CE1
10U
C469
0.1UF
CE4
10U
+V5S
12,13,15,20,21,28,29,31,32,33,34,36,37,38,42,43,44
U27
PVDD
GND
LIN-
LIN+
RIN-
RIN+
BYPASS
Gain0
NC
Gain1
LOUT-
LOUT+
ROUT-
ROUT+
Shutdown
R701
10K/NC
R702
10K
R703
10K
R704
10K/NC
SPK_L2
SPK_L1
SPK_R2
SPK_R1
12,13,15,20,21,28,29,31,32,33,34,36,37,38,42,43,44
OUTL_IN
R219 75K
C572
4.7uF
OUTR_IN
R405 75K
C468
4.7uF
C472
4.7uF
C477
4.7uF
+V5S
R706
20K
SHUTDOWN
C471
4.7uF
Gain0 | Gain1 | Av(inv)
0 | 0 | 6dB
0 | 1 | 10dB
1 | 0 | 15.6dB
1 | 1 | 21.6dB
HASEE 神舟
HASEE TECHNOLOGY INC.,
AUDIO
Draw by
Size C
CAGE Code <Cage Code>
DWG NO
Rev 0.2
Thursday, May 22, 2014
Scale
Model E450
Sheet 41 of 50

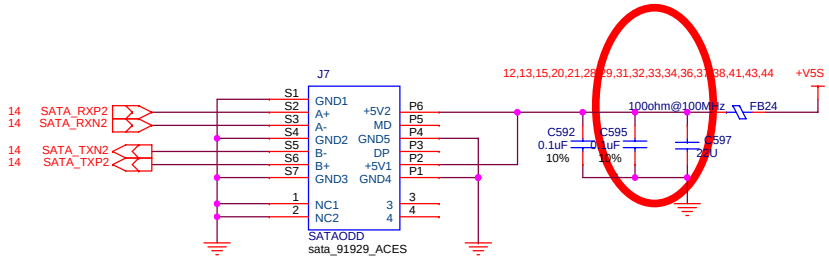
SATA-HDD

PACKAGE: 同E100
sata_C166s6-100a_ALLTOP

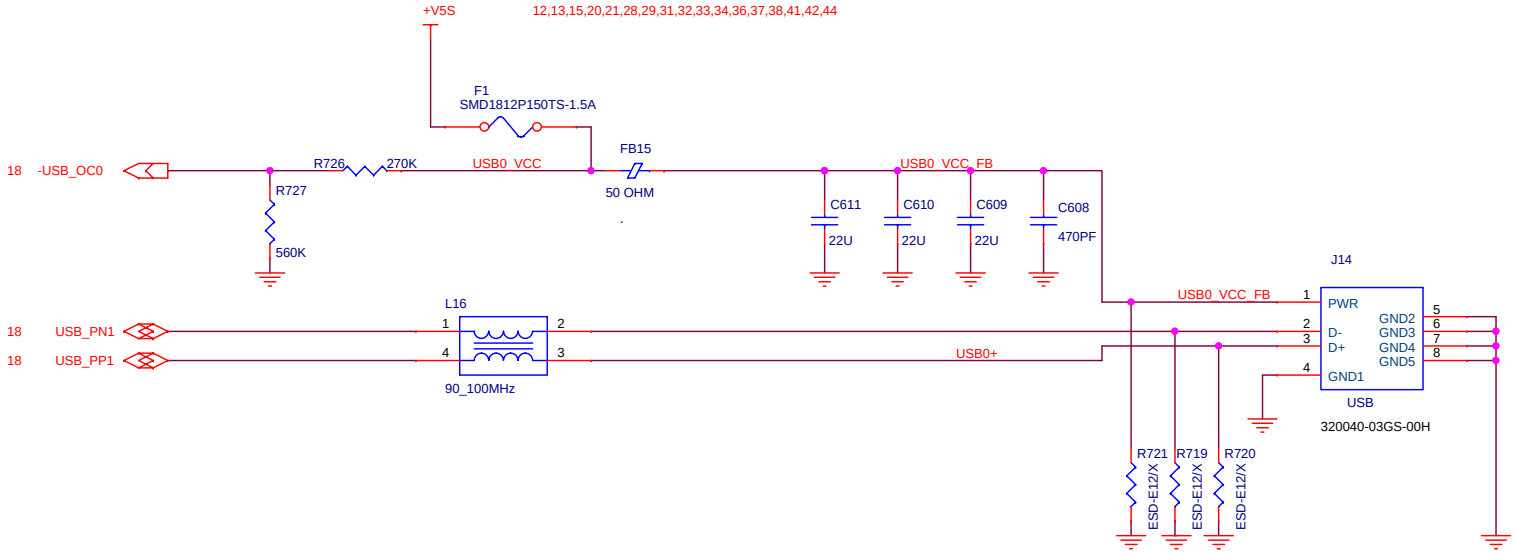


SATA-ODD

(PACKAGE:sata_91929_ACES)



HASEE 神舟	HASEE TECHNOLOGY INC.,		
	SATA HDD & ODD		
Draw by	Size: Custom	CAGE Code: <Cage Code>	DWG NO	Rev: 0.2
Thursday, May 22, 2014	Scale	Model: E450	Sheet: 42 of 50

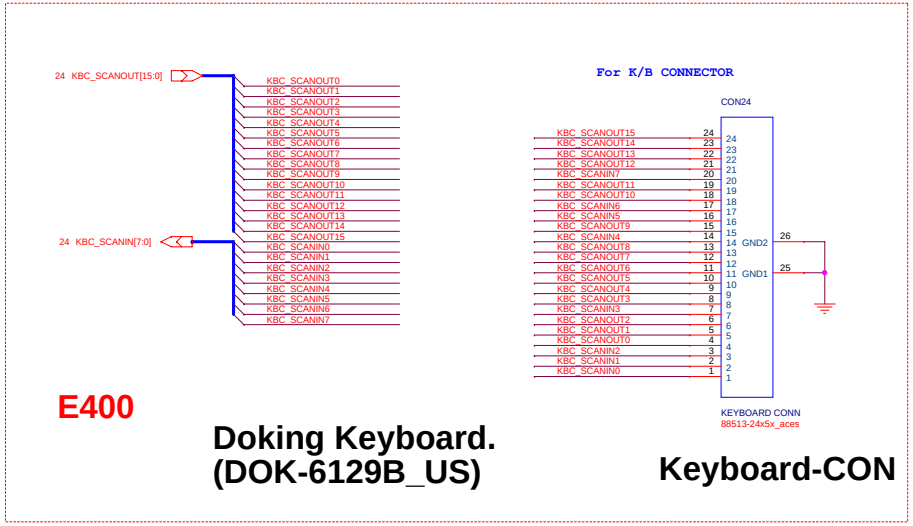


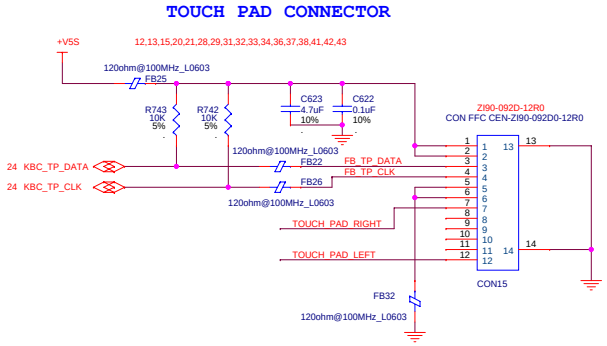
HASEE 神舟

HASEE TECHNOLOGY INC.,

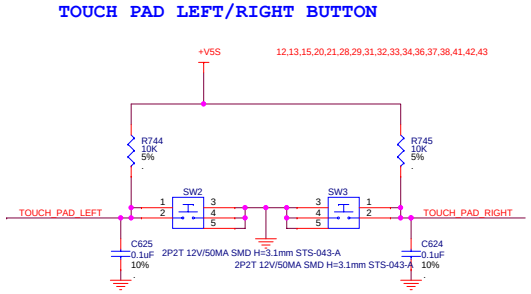
ESATA & USB Ports

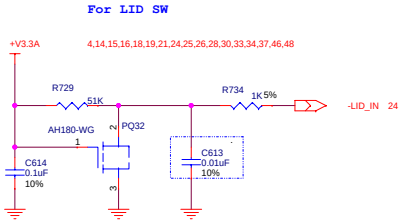
Draw by	Size B	CAGE Code <Cage Code>	DWG NO	Rev 0.2
Thursday, May 22, 2014	Scale	Model E450	Sheet 43 of 50	

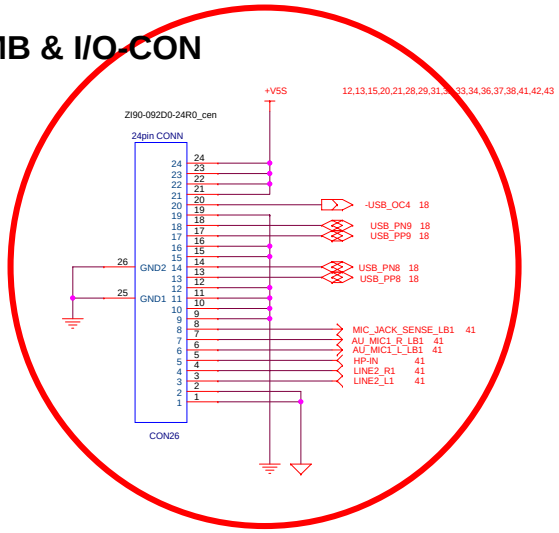




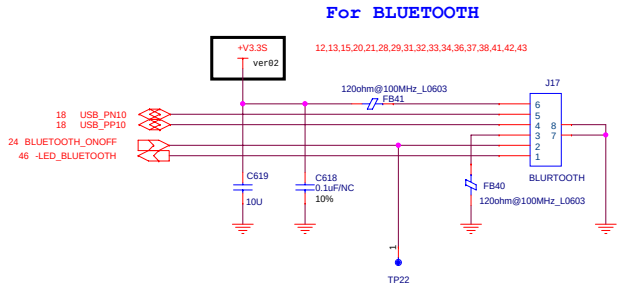
TOUCHPAD (CON15)
线序已更改同 TM-00372-027
封装已更改同 E220
20100629

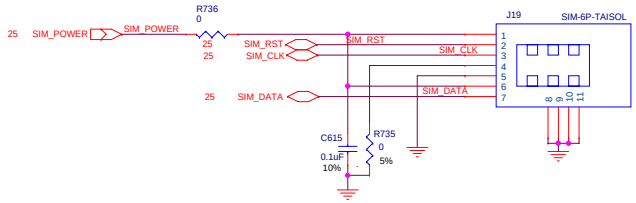


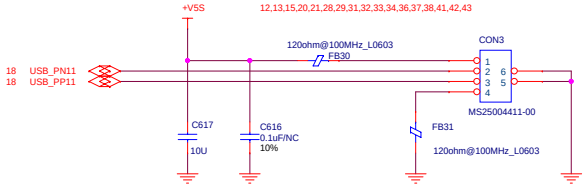


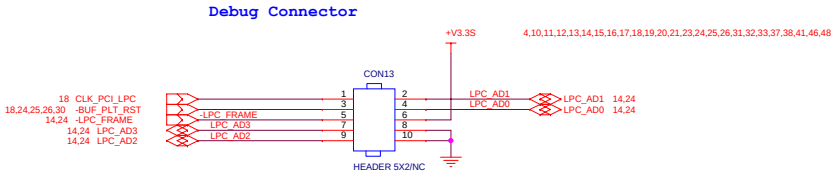


PACKAGE
ZI90-092D0-24R0_cen
朝向









HASEE 神舟

HASEE TECHNOLOGY INC.,

Board Connector

Draw by	Size	CAGE Code	DWG NO	Rev
	C	<Cage Code>		0.2
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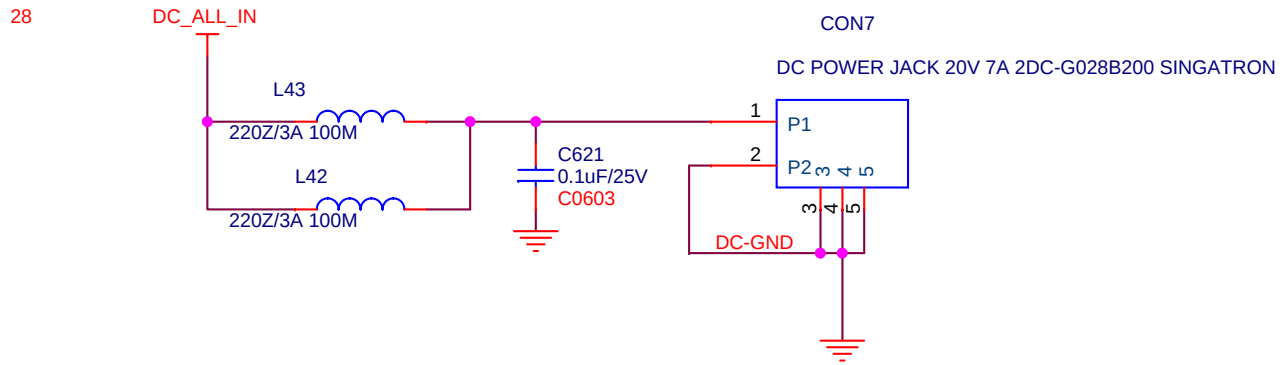
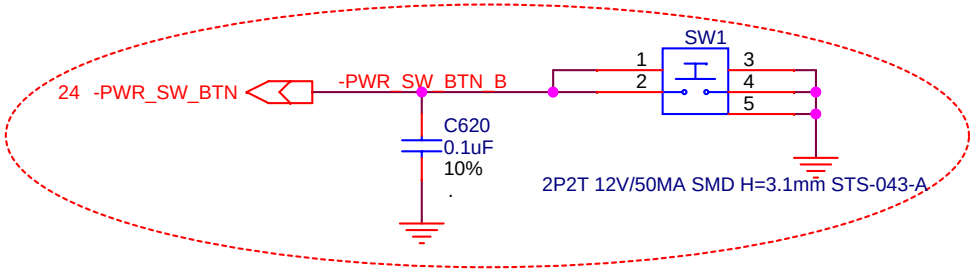
DC IN-PORT



POWER BUTTON



HASEE 神舟

HASEE TECHNOLOGY INC.,

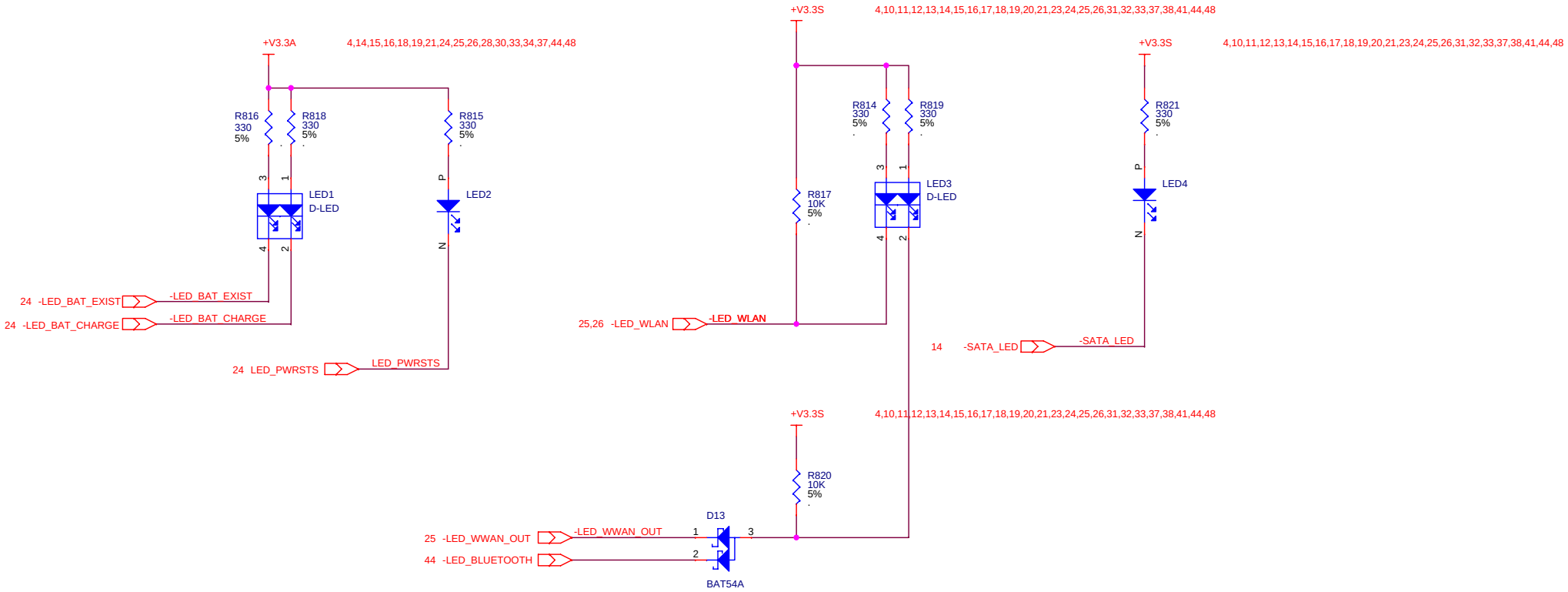
DC-PORT & POWER-BUTTON

Draw by	Size A	CAGE Code <Cage Code>	DWG NO	Rev 0.2
Thursday, May 22, 2014	Scale	Model E450	Sheet 45 of 50	

PWRSTS	WLAN	BATT-LED	HDD
LED2	LED3	LED1	LED4

TOP Left Right

LED



HASEE 神舟

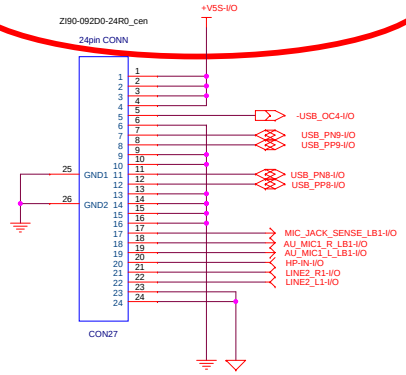
HASEE TECHNOLOGY INC.,

LED

Draw by	Size	CAGE Code	DWG NO	Rev
	B	<Cage Code>		0.2
Thursday, May 22, 2014	Scale	Model E450	Sheet 46 of 50	

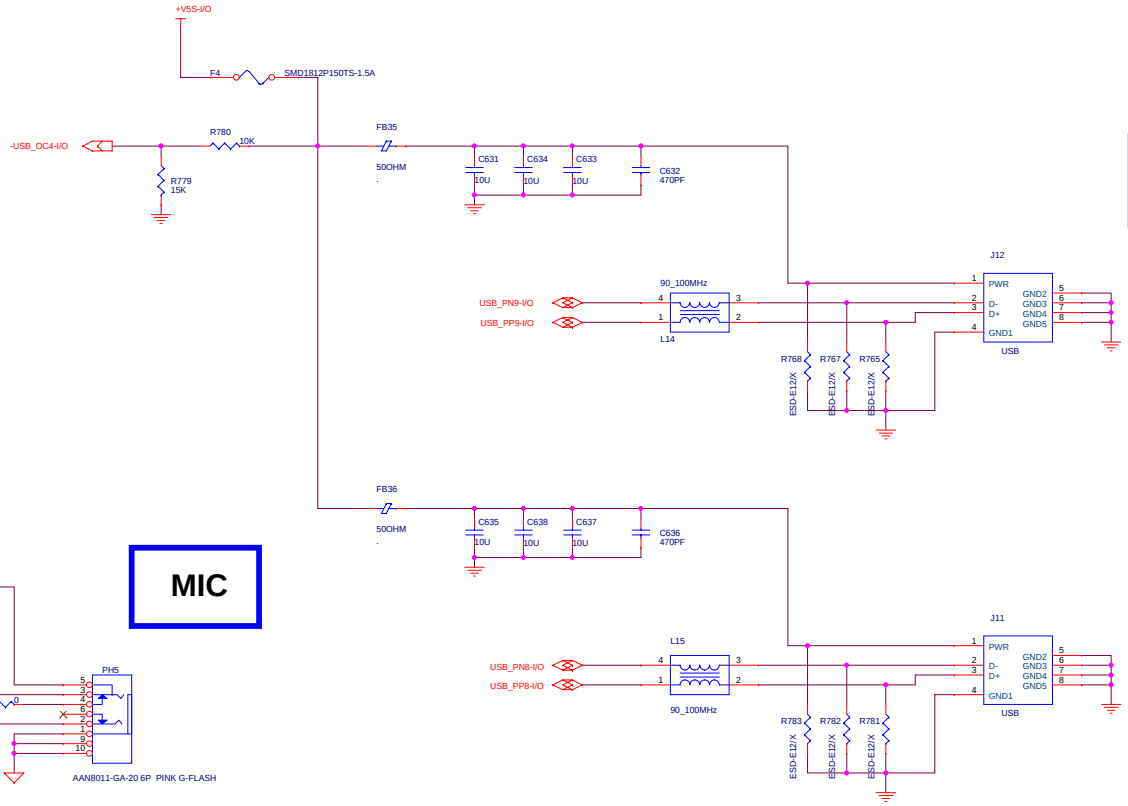
I/O & MB-CON
GND-I/O
GND_CODEC-I/O

I/O & MB-CON

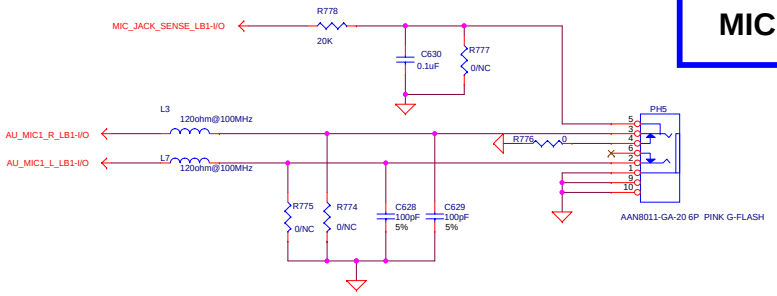


PACKAGE
ZI90-092D0-24R0_cen
朝向

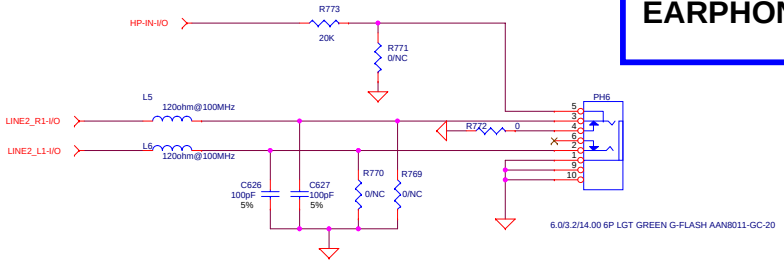
USB PORT

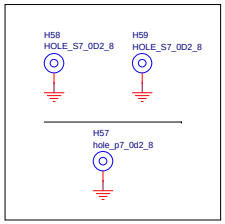


MIC

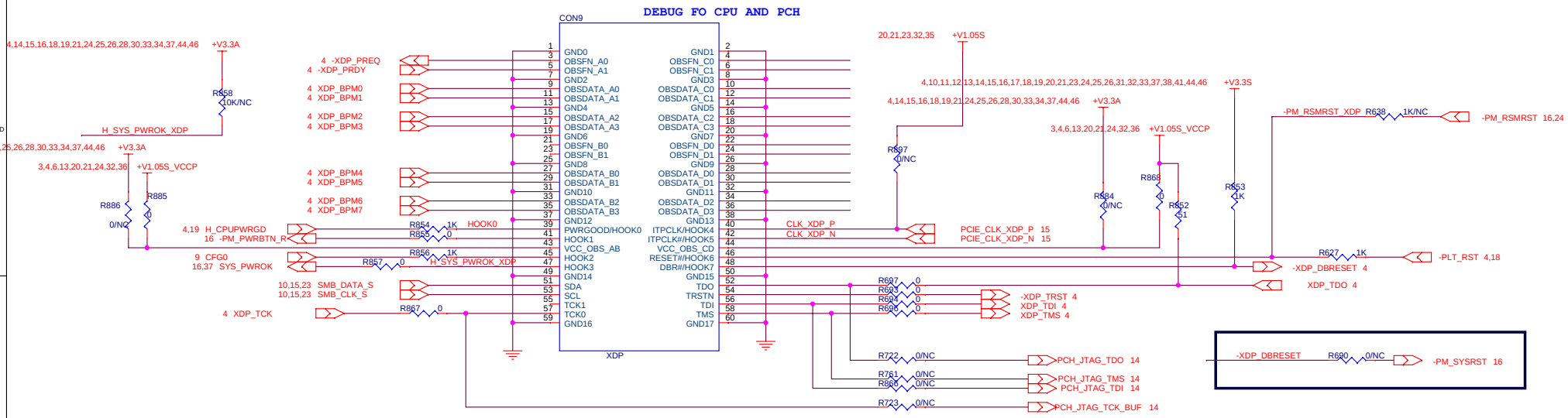


EARPHONE





HASEE 神舟	HASEE TECHNOLOGY INC.,		
	I/O BOARD USB & MIC-EARPHONE		
Draw by	Size Custom	CAGE Code <Cage Code>	DWG NO	Rev 0.2
Thursday, May 22, 2014	Scale	Model E450	Sheet 47 of 50

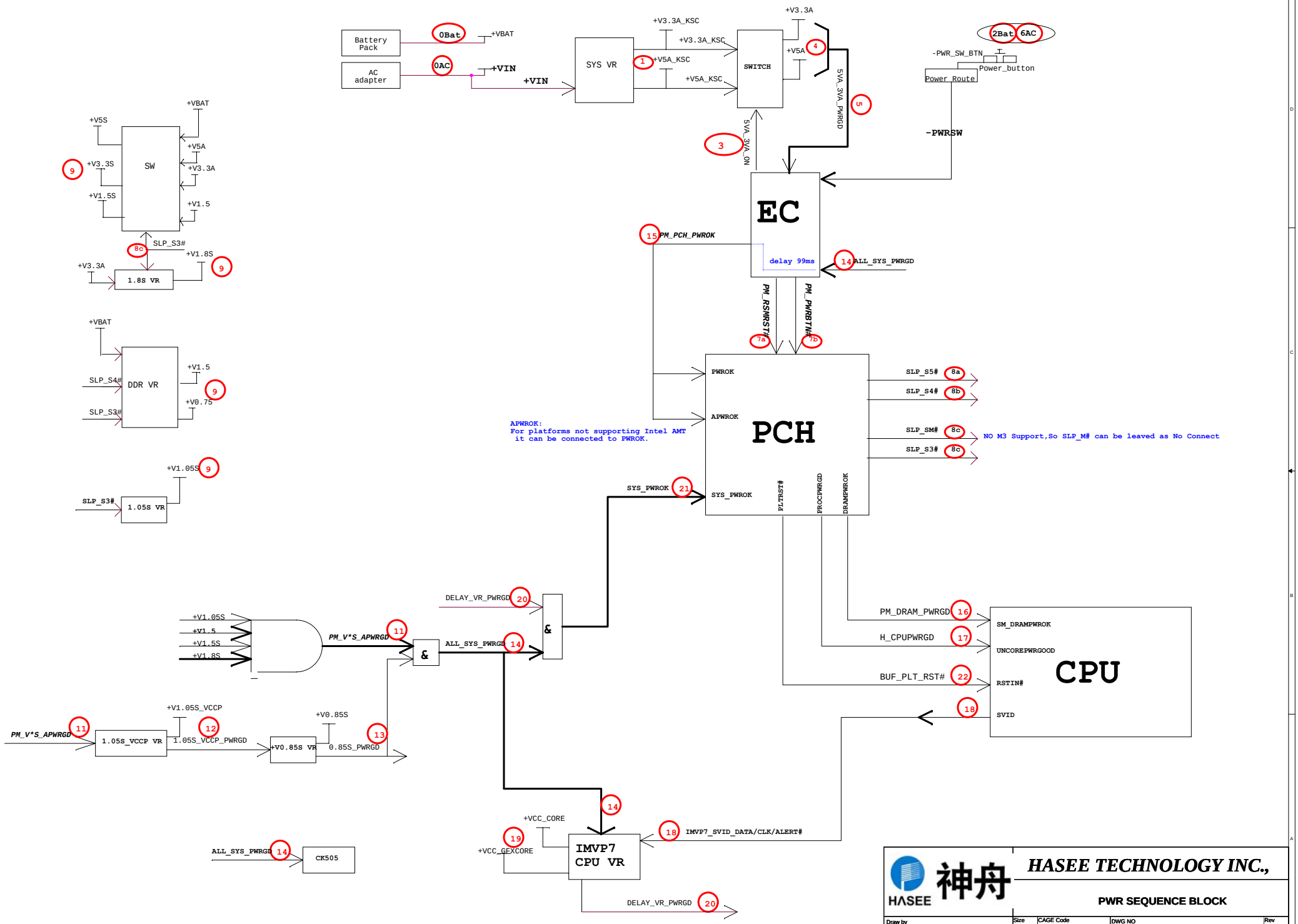


For PCH debug with XDP, need to NO STUFF R364

To debug for pch:
Stuff: R858\R886\R772\R761\R866\R732
\R895\R897\R884\R638
Unstuff:R854\R885\R857\R867\R868\R856
R627\R697\R693\R694\R696\R278\R279

To debug for CPU:
Stuff: R885\R854\R856\R857\R867\R868\R627\R690
Unstuff:

HASEE 神舟	HASEE TECHNOLOGY INC.,		
	XDP		
Draw by LIZX	Size Custom	CAGE Code <Cage Code>	DWG NO	Rev 0.2
Thursday, May 22, 2014	Scale	Model E450	Sheet 48 of 50


Battery Pack
AC adapter
0Bat
0AC
+VBAT
+VIN
SYS VR
+V3.3A_KSC
+V5A_KSC
SWITCH
+V3.3A
+V5A
5VA_3VA_PWRGD
5VA_3VA_ON
2Bat
6AC
-PWR_SW_BTN
Power_button
Power Route
-PWRSW
EC
delay 99ms
PM_PCH_PWROK
ALL_SYS_PWRGD
PM_RSMRST#
PM_PWRBTN#
PCH
PWROK
APWROK
SYS_PWROK
PLTRST#
PROCPWRGD
DRAMPWROK
SLP_S5#
SLP_S4#
SLP_SM#
SLP_S3#
APWROK:
For platforms not supporting Intel AMT
it can be connected to PWROK.
NO M3 Support,So SLP_M# can be leaved as No Connect
CPU
SM_DRAMPWROK
UNCOREPWRGOOD
RSTIN#
SVID
PM_DRAM_PWRGD
H_CPUPWRGD
BUF_PLT_RST#
IMVP7_SVID_DATA/CLK/ALERT#
IMVP7
CPU VR
+VCC_CORE
+VCC_GEXCORE
DELAY_VR_PWRGD
SYS_PWROK
ALL_SYS_PWRGD
PM_V*S_APWRGD
&
SW
+V5S
+V3.3S
+V1.5S
+V1.5
+V1.8S
SLP_S3#
1.8S VR
DDR VR
SLP_S4#
+V0.75
+V1.05S
1.05S VR
+V1.5S
+V1.8S
1.05S_VCCP VR
+V1.05S_VCCP
1.05S_VCCP_PWRGD
+V0.85S VR
+V0.85S
0.85S_PWRGD
CK505
HASEE
神舟
HASEE TECHNOLOGY INC.,
PWR SEQUENCE BLOCK
Draw by
LIZX
Thursday, May 22, 2014
Size
C
CAGE Code
<Cage Code>
DWG NO
Rev
0.2
Scale
Model
E450
Sheet
49
of
50

Change List from Ver01 to Ver02

1、Page4,Pull-up R25 from +V3.3S changed to +V3.3A

2、Page4, R25,R22,Q65,Q67 all NoStuff
R23 Stuff

3、Page7, PQ45,Q22,R58 all NoStuff
R59 Stuff

4、Page14, U29、R243 、R618、R785、R787、R788、C641 Deleted (SPI1 Flash Del)
R240、R616、R784 Deleted （SPI0 series-resistor Del）

5、Page19,U4,C121,R487 all NOstuff

6、Page23,All NoStuff

7、Page24,C384,C385,Y5,R522,R600,R718 All NoStuff; R847,C368 Stuff
同时 Page18, R352 Stuff
R882 Stuff

8、Page28,H33\H32 change the footprint

9、Page33, PR152--〉220K,R842-->1M,C537-->0.1UF,C674-->0.01UF(Stuff)

10、Page36,C358 change and NC

11、Page37, C483 change and NC; R909-->Stuff

12、Page14, Isolate HDA SYNC from the codec during the strap:
Add R787(Stuff),Q51,Q46,R247

13、Page44,J17(for bluetooth) pin6, from +V5s changed to +V3.3s

14、Layout J6和J14的库要更改及PCH上方邮票孔位置更改

15、About the Power:
L13(2.2u)-->1u----------+V1.5
C537(0.01U)-->0.1U----------+V5A
C178-->33nF,R167-->2.87K,R127-->1.2K all 1%----------+VCORE
C364-->82nF,C367-->2200pF,R177-->665,R144-->2.43K,
R150-->220K,R172-->270,C286-->560pF,C288-->1nF,C264-->47pF-------+VGFORCE

16、Page34, add C641-->0.22uF,C645-->1uF
change C647 -->33nF

17、Page41,add R220 and amplifier for Mic in

Change List from Ver02 to Ver03

1、Page35,add R670
Page36,add PJP33
(Vccp substitute for V1.05s)

2、Page41,con4 change
add R725

Change List from Ver03 to Ver10

1、Page14,add R268\R269

2、Page37,add C493

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HASEE TECHNOLOGY INC.,

PWR SEQUENCE BLOCK

Draw by LIZX	Size B	CAGE Code <Cage Code>	DWG NO	Rev 0.2
Thursday, May 22, 2014	Scale	Model E450	Sheet 50 of 50	