

LCFC Confidential

DS321 MB Schematics Document

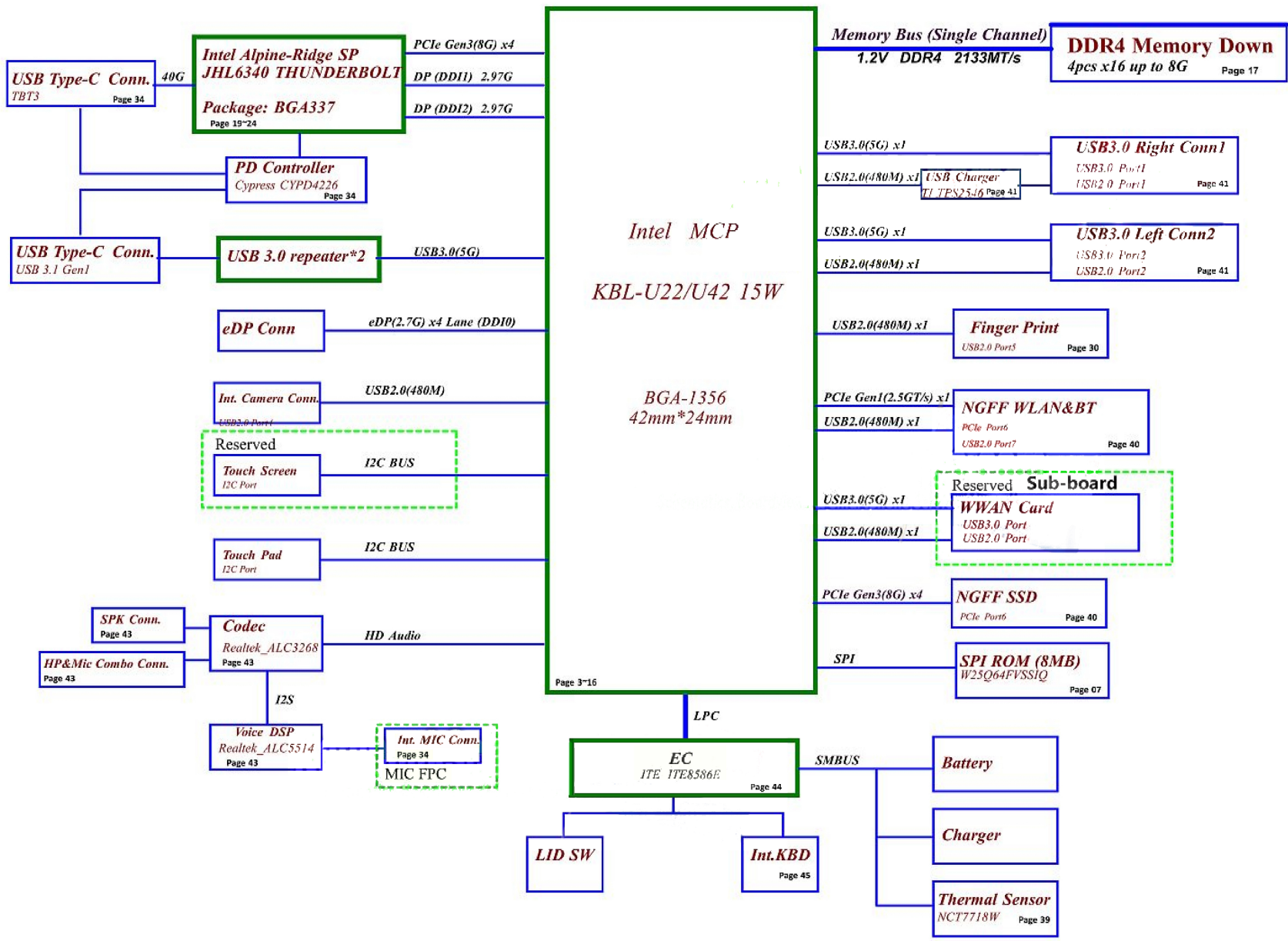
Intel Kabylake-U22&U42 with DDR4

2016-12-05

REV: 0.2

Intel Kabylake-U22&U42 with DDR4

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Cover Page		
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State		+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
	V20B+			
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

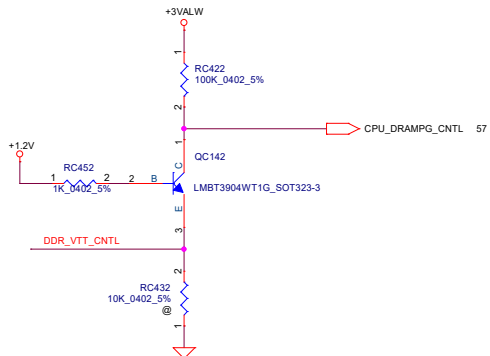
Device	Address
PMIC	need to update

PCH SM Bus address

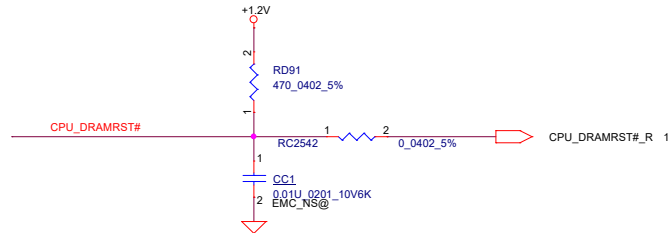
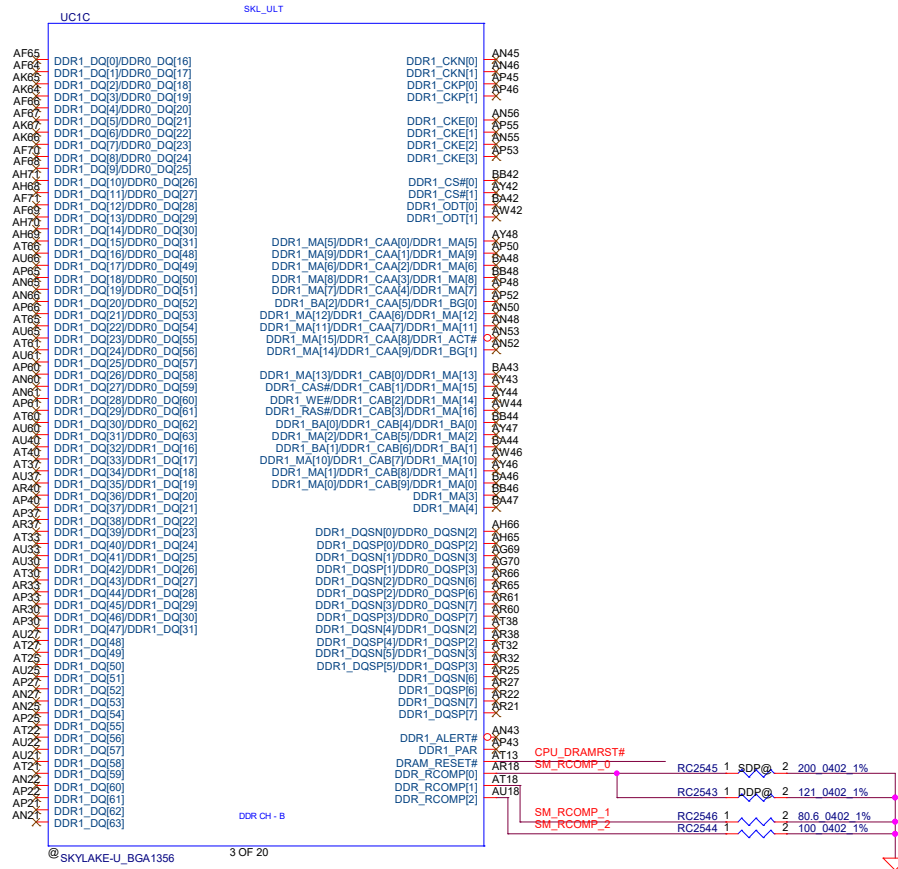
Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

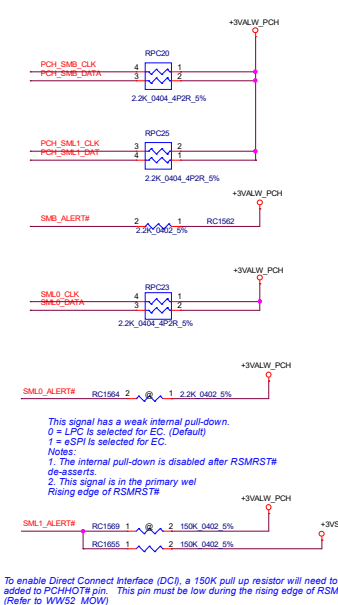
HSIO PORT	Function	BOM Structure	BTO Item
USB3.0	1 USB3.0 Conn Left	@	Not stuff
	2 USB3.0 Conn Right(optional)	14@	For 14" part
	3 3D Camera(optional)	15@	For 15" part
	4 NC	14or15@	For 14" or 15" part
	5 NC	14or17@	For 14" or 17" part
	6 NC		
USB2.0	1 USB3.0 Conn Left	Cannonlake@	For Cannonlake part
	2 USB2.0 Conn1 Right	CD@	For C cost down
	3 USB2.0 Conn2 Right	DUALMIC@	For Dual MIC part
	4 Camera	EMC@	For EMC part
	5 Cardreader	EMC_15@	For EMC 15" part
	6 Touch Panel	EMC_NS@	For EMC nu-stuff part
	7 Bluetooth	EMC_PX@	For EMC PX part
	8 TBT	EMC_PXNS@	For EMC PX nu-stuff part
	9 NC	ES@	For ES CPU
	10 NC	EXO@	For EXO GPU
PCIE	1 NC		
	2 NC		
	3 NC	ME@	For ME part
	4 NC	NTS@	For nu-touch part
	5 LAN		
	6 WLAN		
	7 used as SATA		
	8 used as SATA		
SATA	9~12 X4 PCIE	PX@	For PX part
	0 HDD	RANKA@	For VRAM rank A part
	1A ODD	RANKB@	For VRAM rank B part
	1B used as PCIE	Realtek SD@	For Realtek SD part
	2 used as PCIE	SINGLEMIC@	For single MIC part
		SINGLERANK@	For single VRAN rank part
		DUALRANK@	For dual VRAN rank part
		TS@	For touch screen part
		TPM@	For TPM part
		UMA@	For UMA part



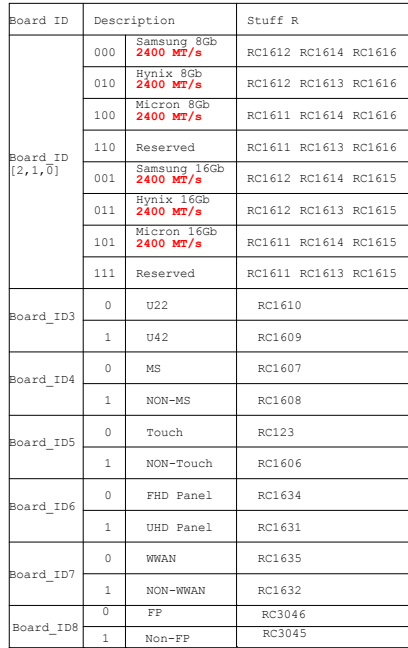
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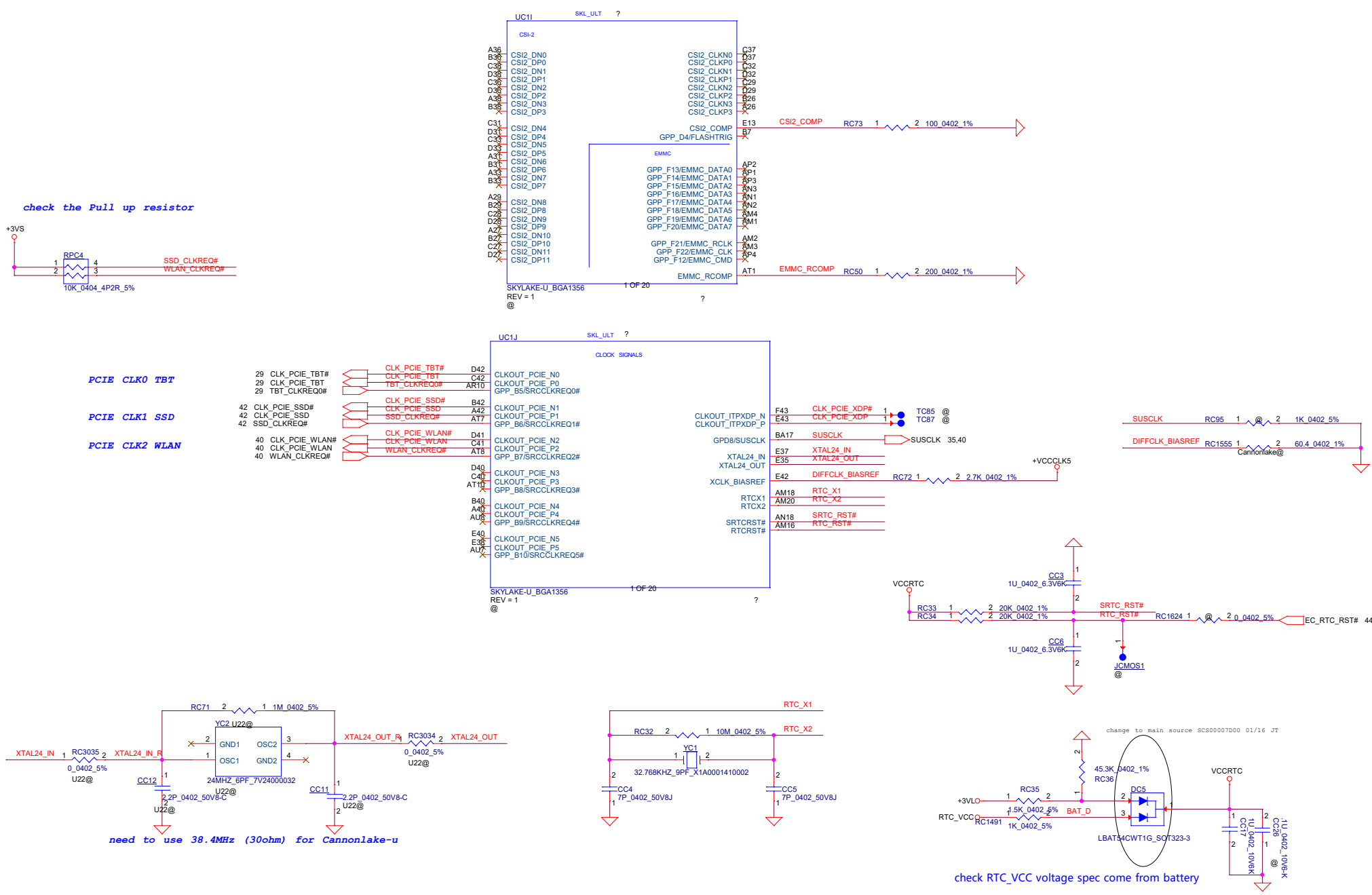
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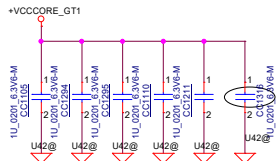
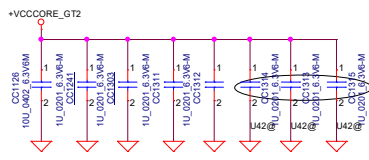
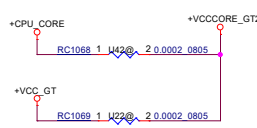
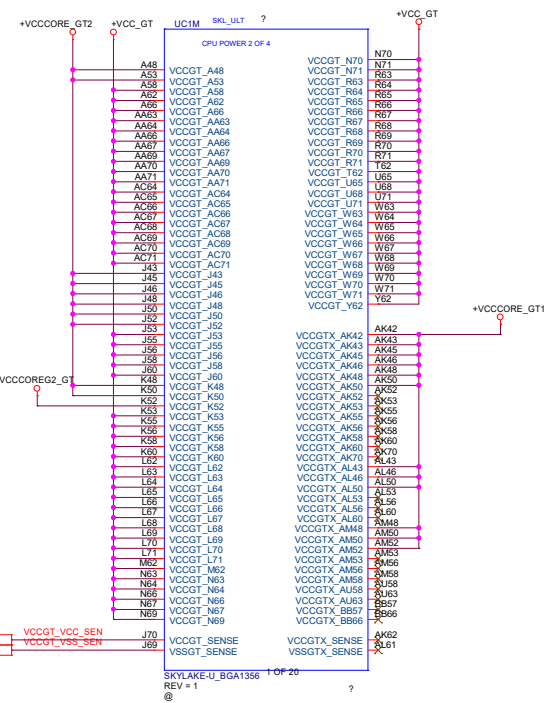
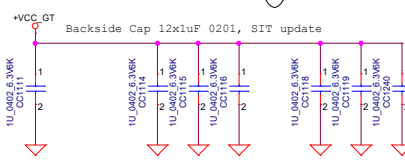
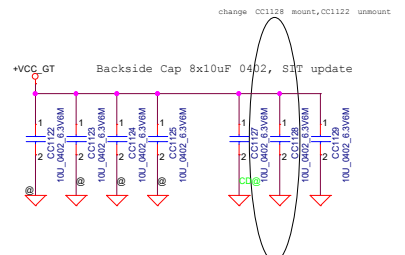
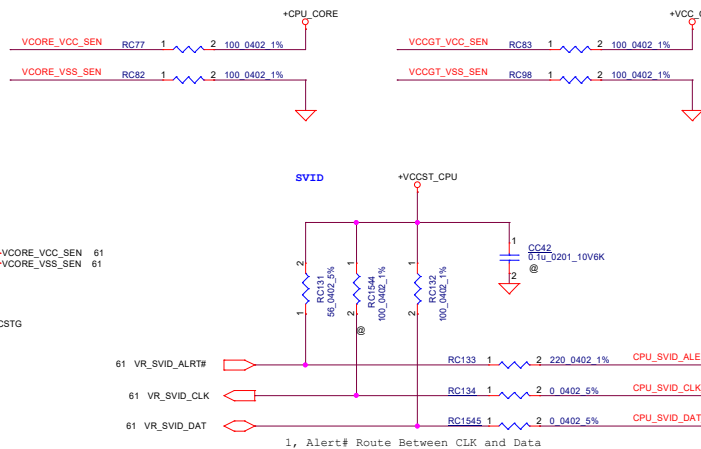
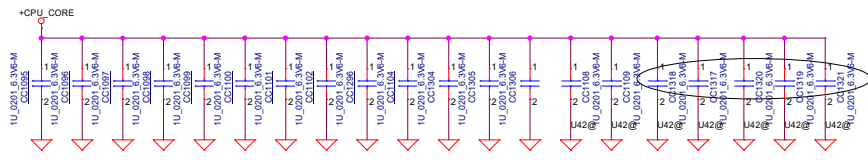
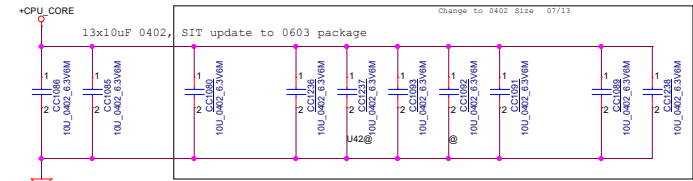
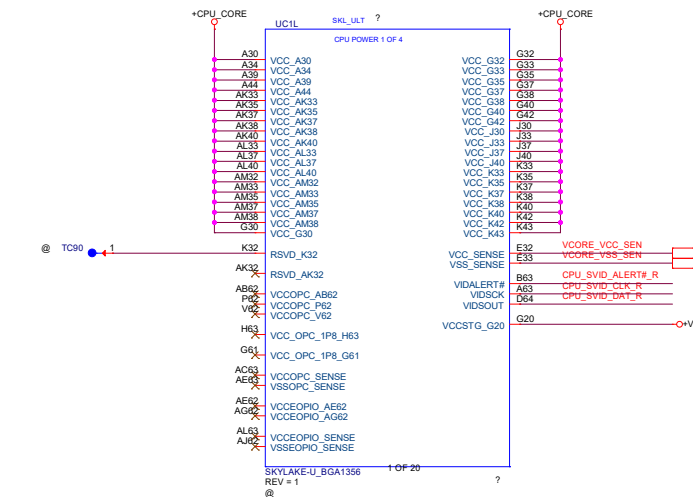


Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable "Top Swap" mode. (Default) ★ 1 = Enable "Top Swap" mode.	0	Rising edge of PCH_PWROK
SSPI0 MOSI / GPP_E18	No Reboot	Internal PD 0 = Disable "No Reboot" mode. (Default) ★ 1 = Enable "No Reboot" mode	0	Rising edge of PCH_PWROK
SSPI1 MOSI / GPP_E22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) ★ 1 = LPC	0	Rising edge of PCH_PWROK

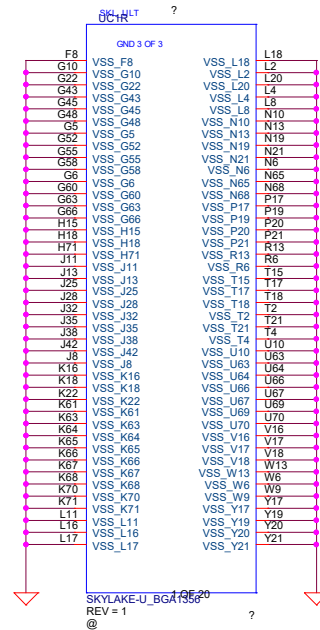
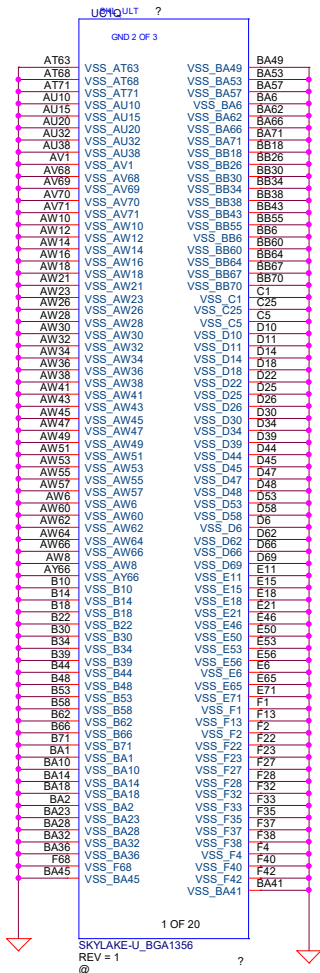
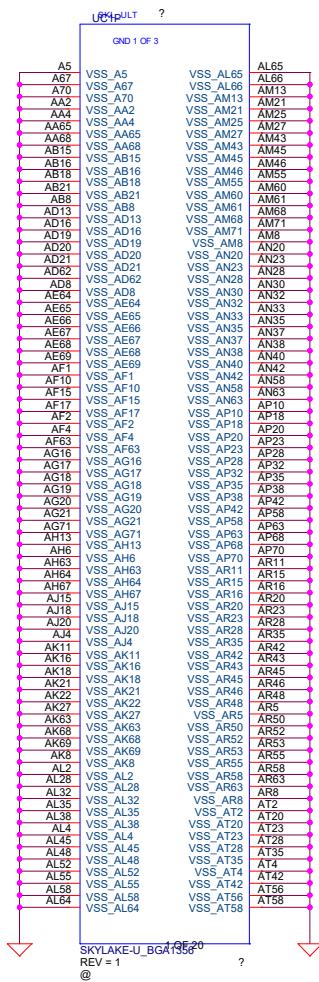
Need change to SB000019A00
S TR DMN5L06DWK-7 2N SOT363-6
Vqs(th) max1.0V

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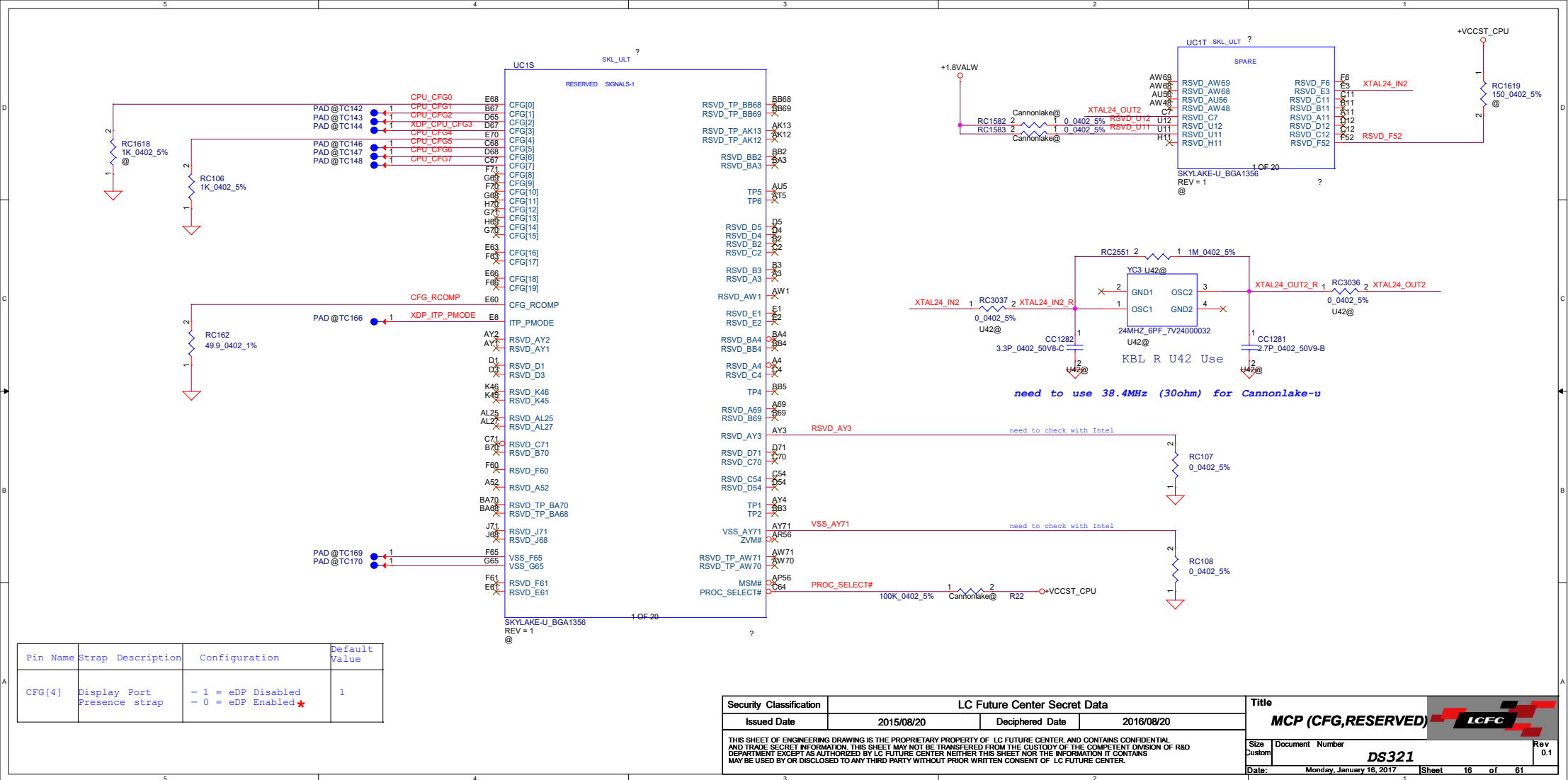
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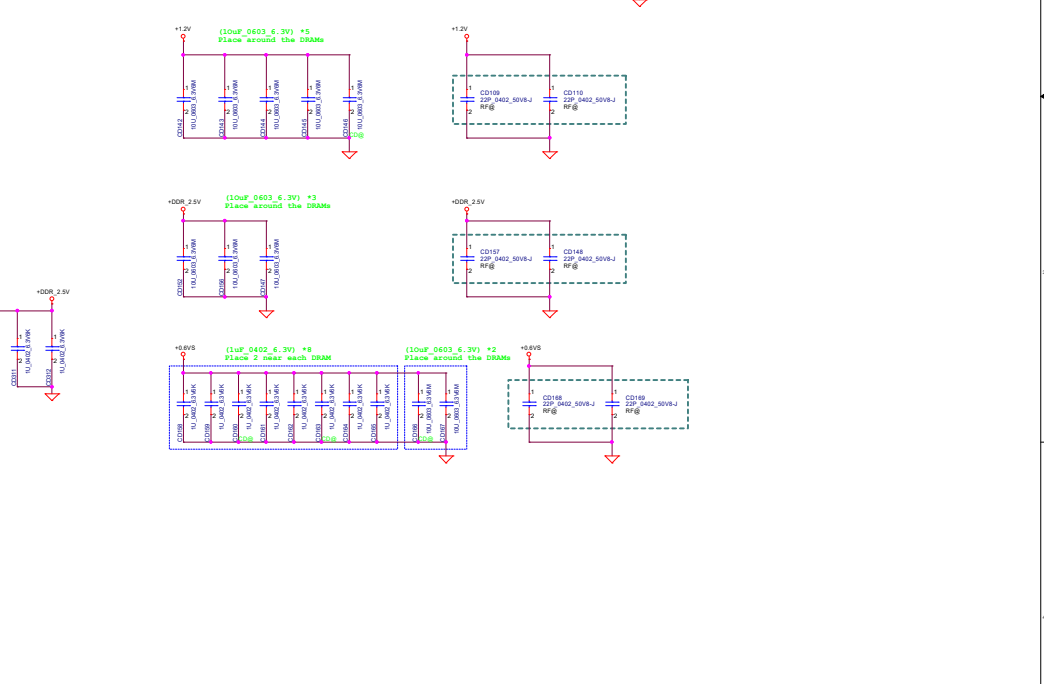
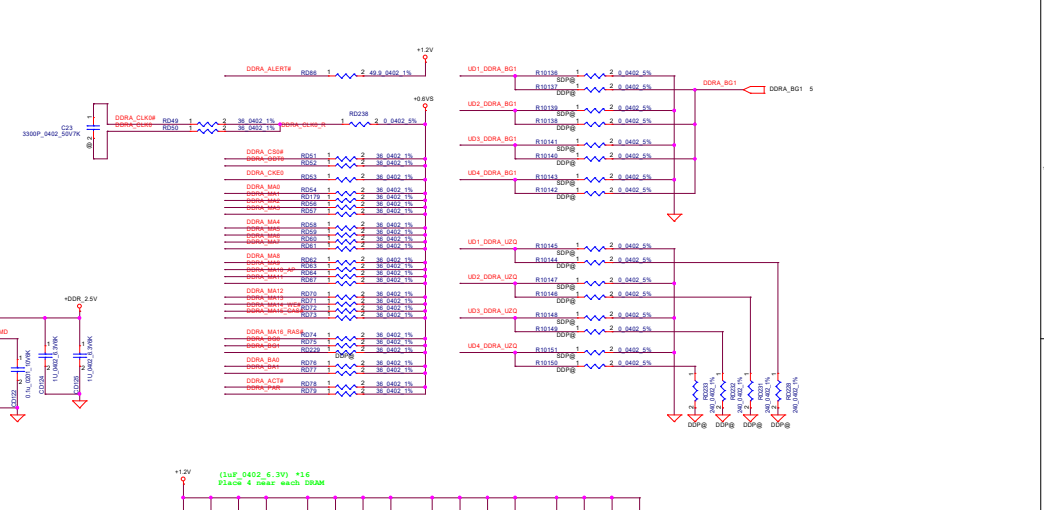
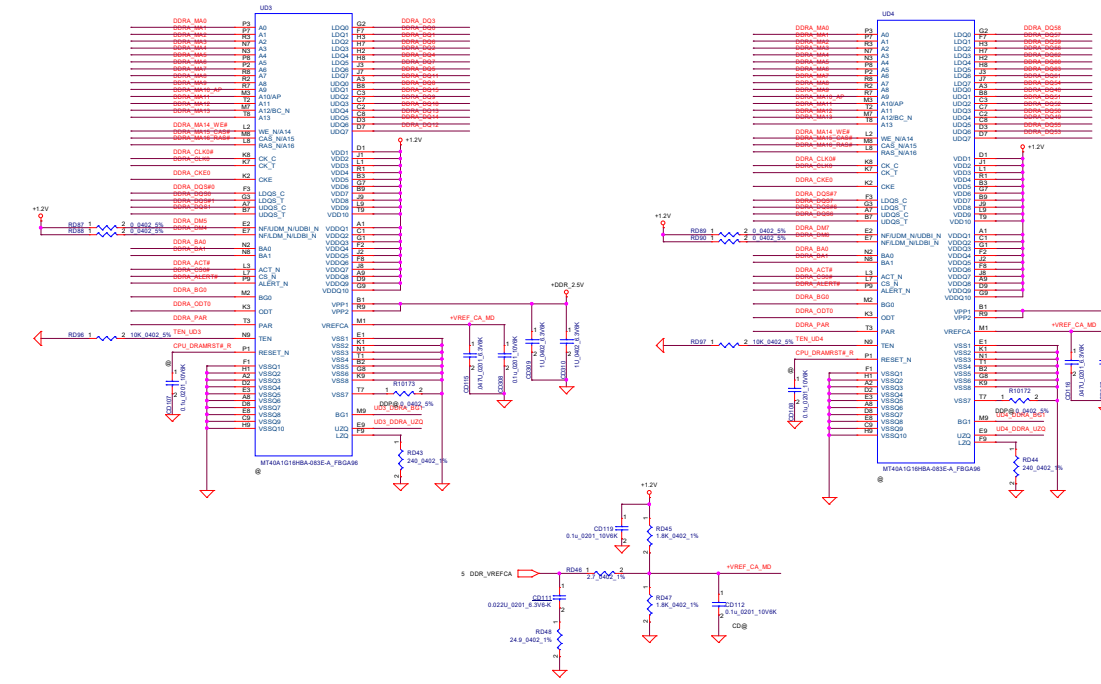
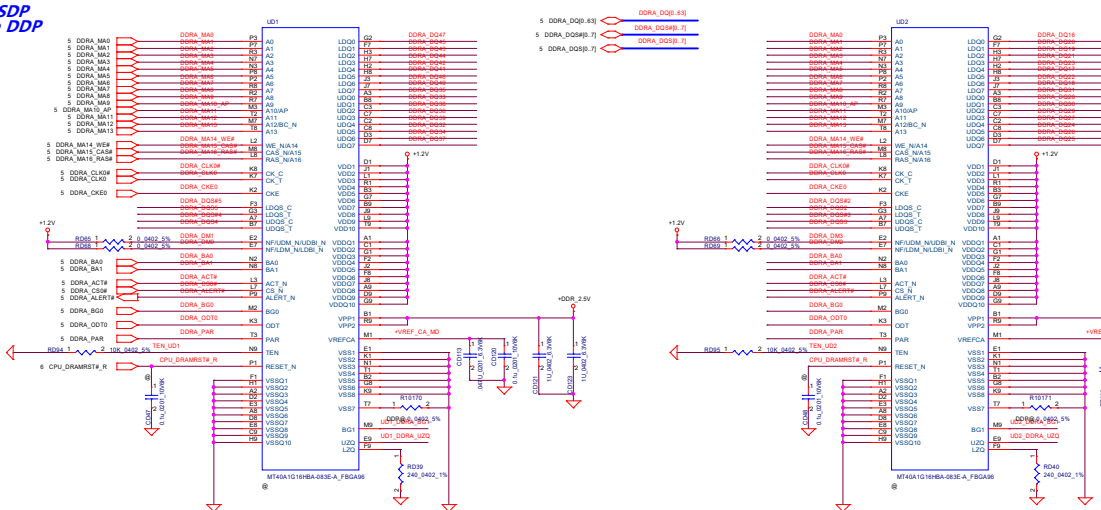
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Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	- 1 = eDP Disabled - 0 = eDP Enabled ★	1

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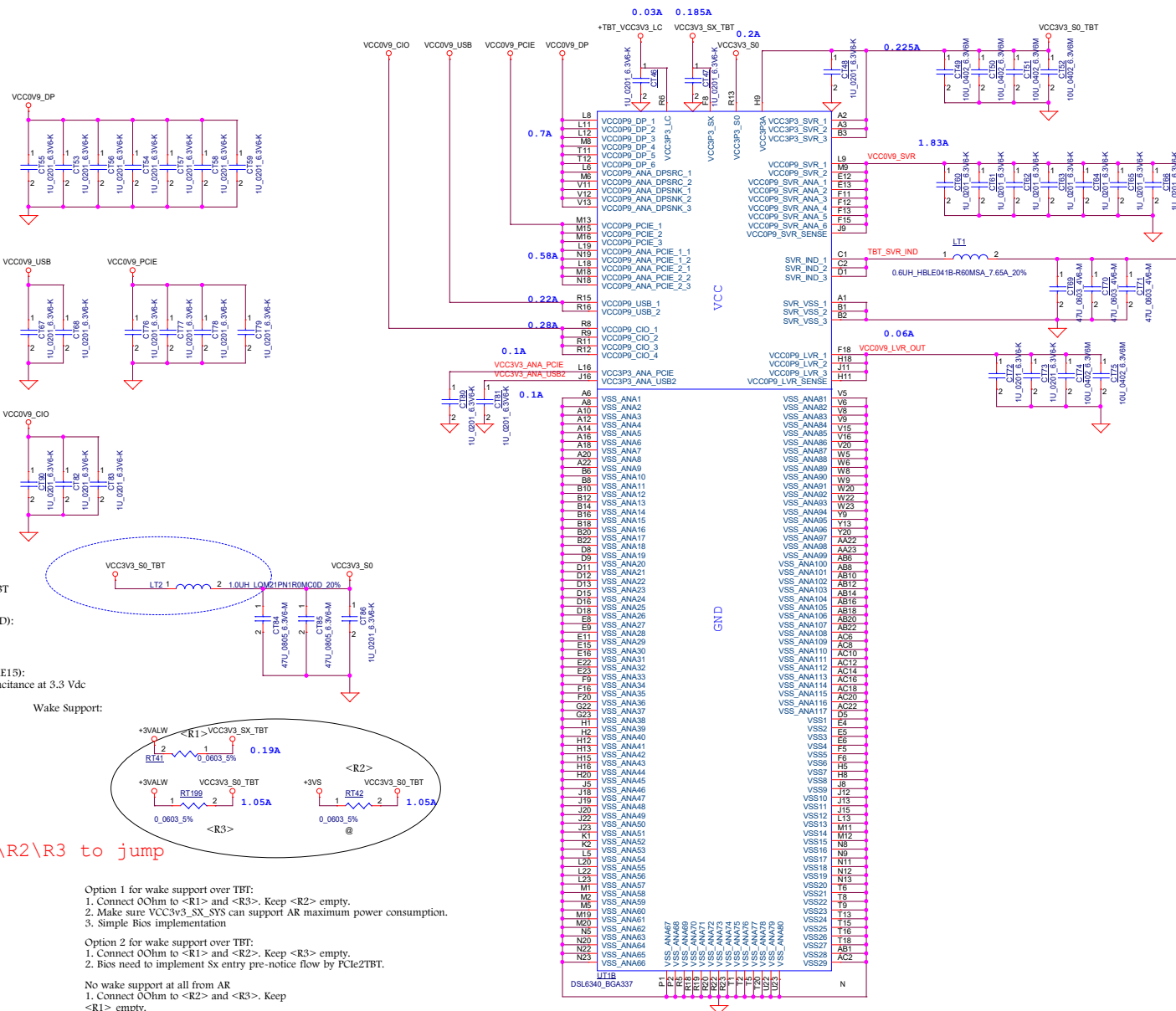
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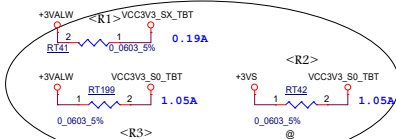
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40KHz LC Filter to reduce VCC3V3_S0_TBT ripple
 L (LQM18PN1R0MFHD):
 RDC < 0.20hm
 IDC > 0.2A
 C (GRM188R60J476ME15):
 Need to notice the capacitance at 3.3 Vdc

Wake Support:



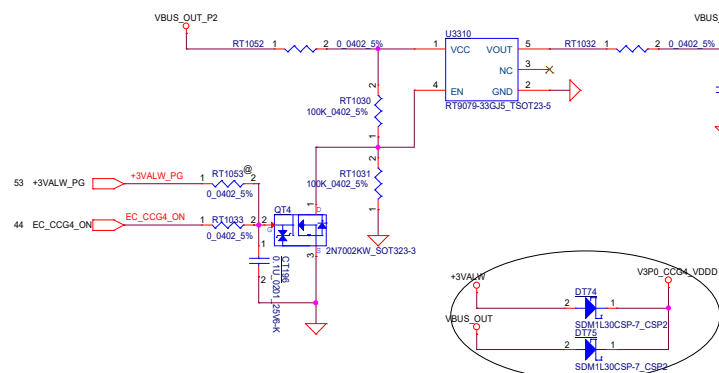
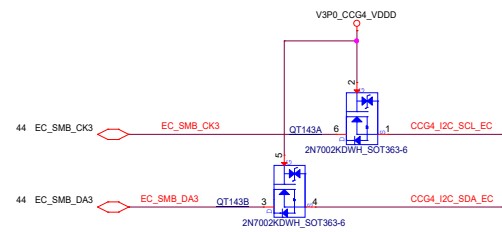
change R1\R2\R3 to jump

- Option 1 for wake support over TBT:
 1. Connect 00hm to <R1> and <R3>. Keep <R2> empty.
 2. Make sure VCC3V3_SX_SYS can support AR maximum power consumption.
 3. Simple Bios implementation

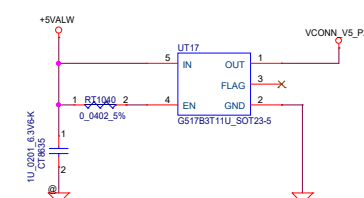
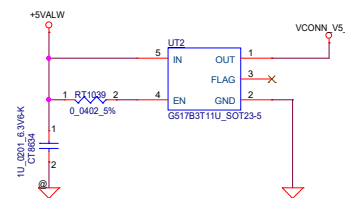
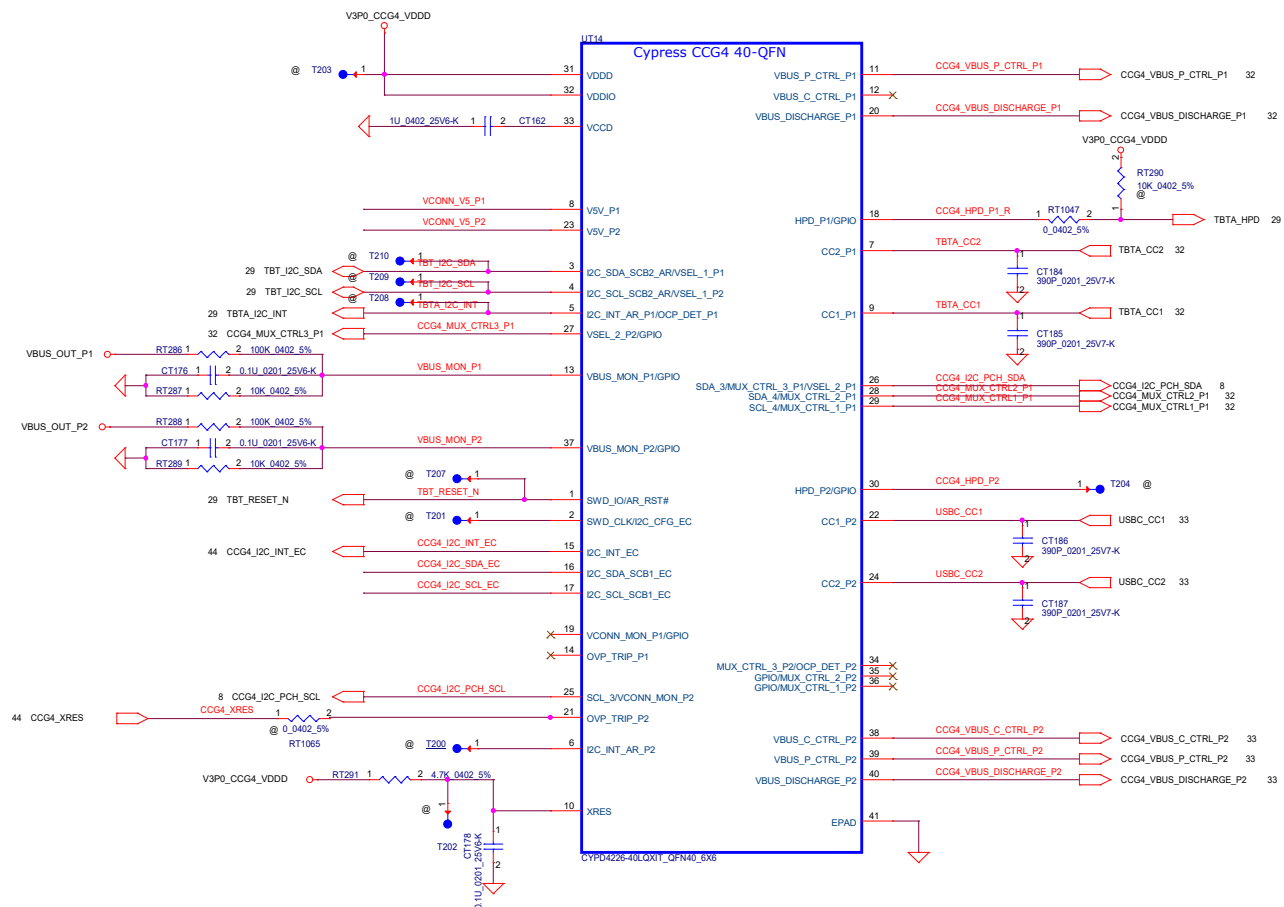
- Option 2 for wake support over TBT:
 1. Connect 00hm to <R1> and <R2>. Keep <R3> empty.
 2. Bios need to implement Sx entry pre-notice flow by PCIe2TBT.

No wake support at all from AR
 1. Connect 00hm to <R2> and <R3>. Keep <R1> empty.

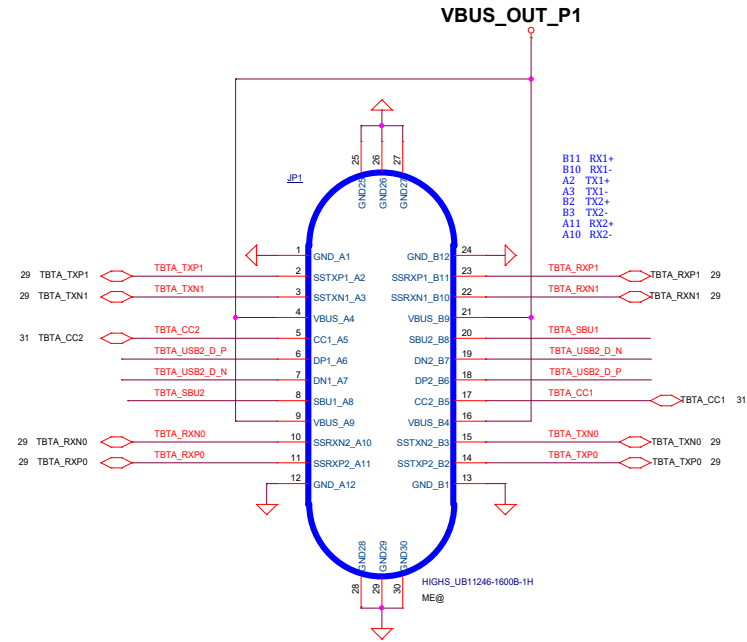
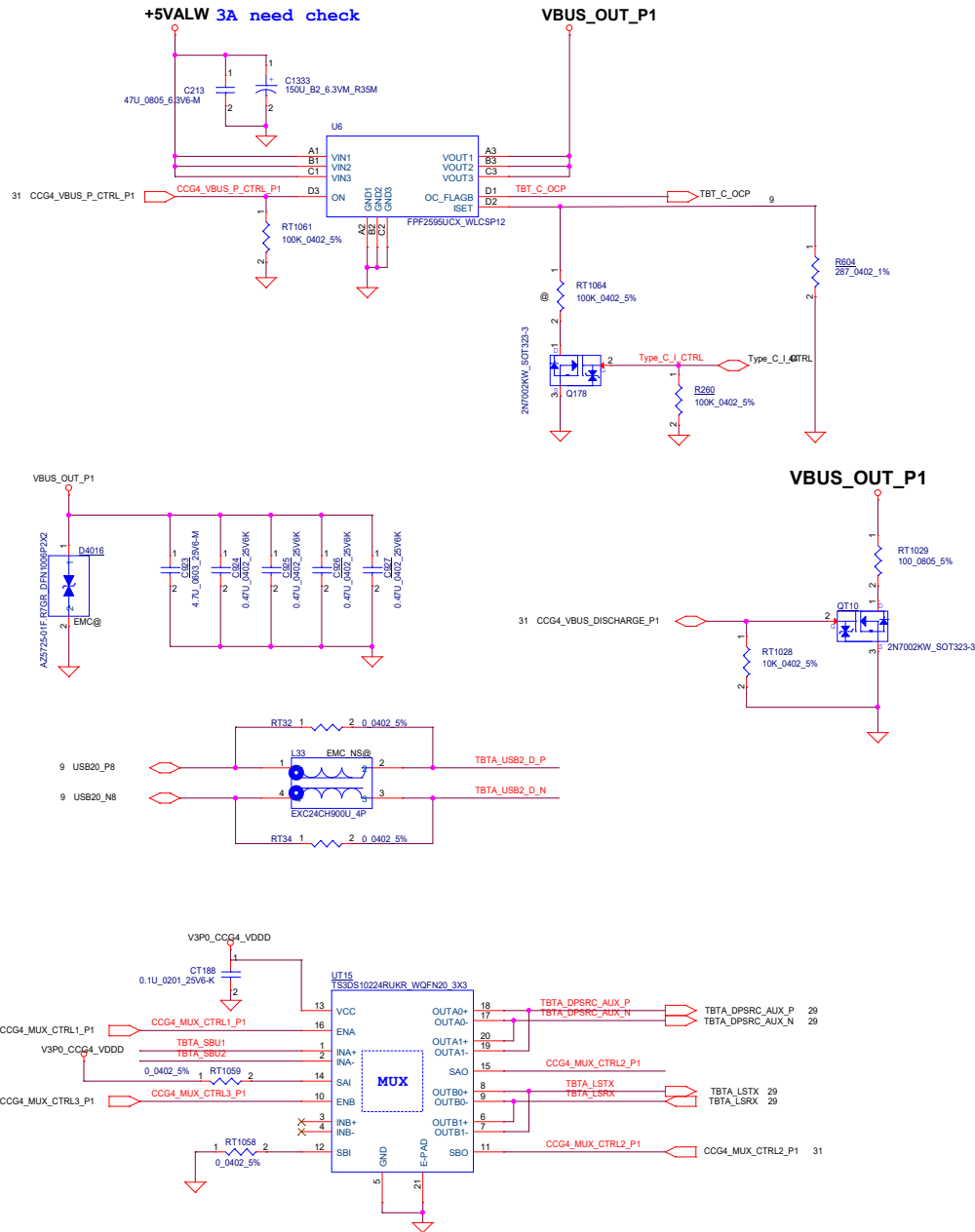
S IC JHL6340 SLLSQ C1 CONTROLLER 12 !,



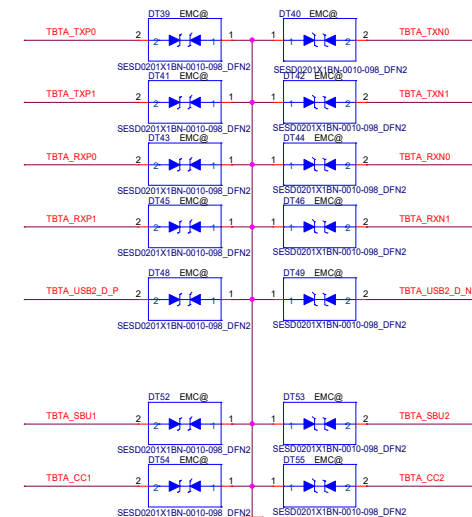
SCS00006000,
S SCH DIO SDM20U30LP-7 DFN1006-2



TBT3 not support type-c adppter

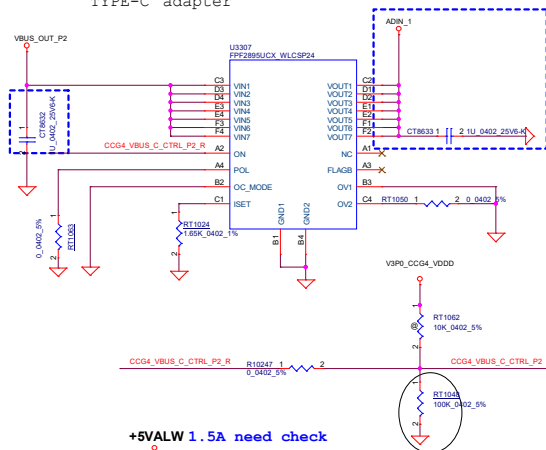


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1116 update symbol
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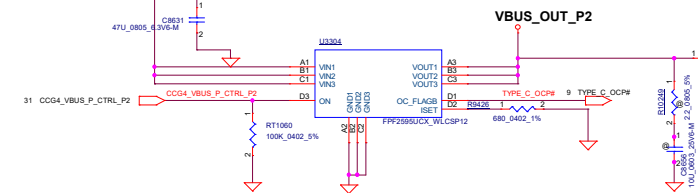


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Date:								Monday, January 18, 2017		Sheet 32 of 61	

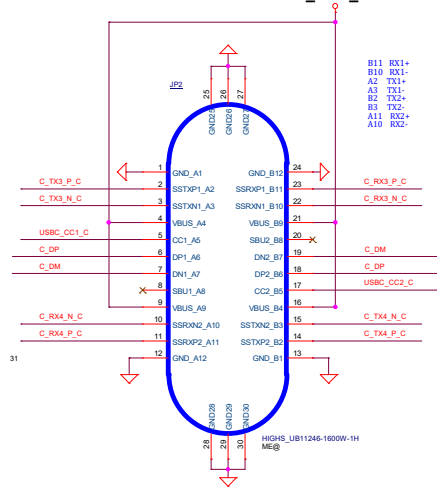
TYPE-C adapter



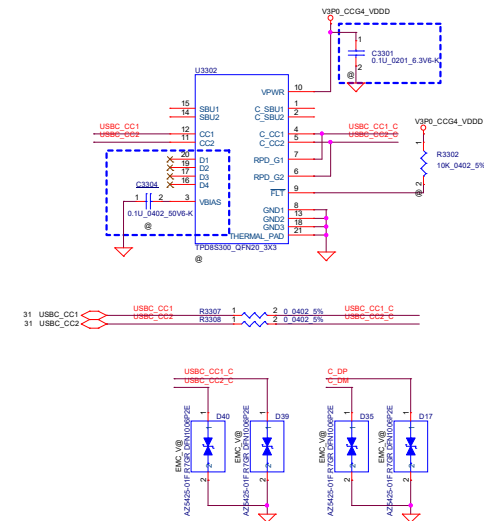
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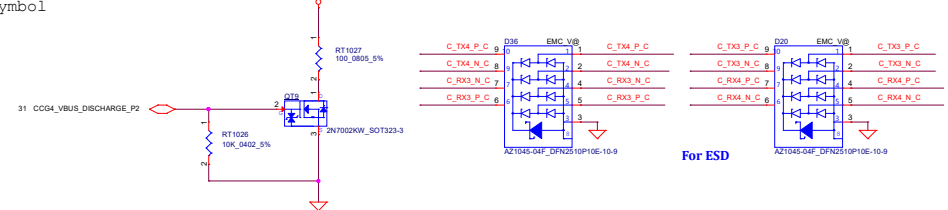
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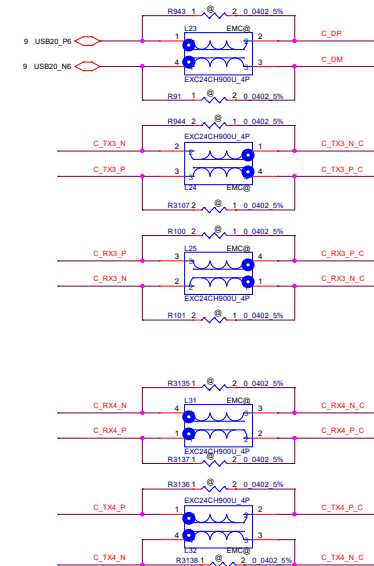
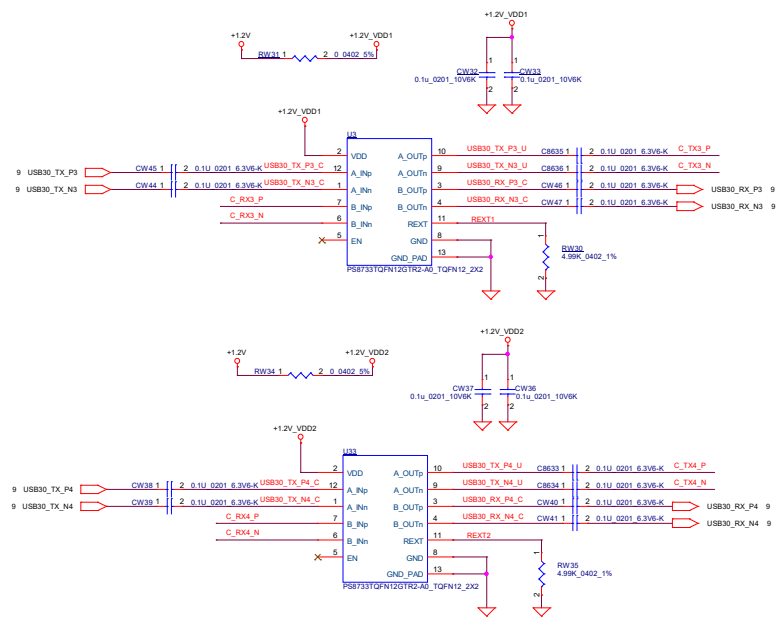
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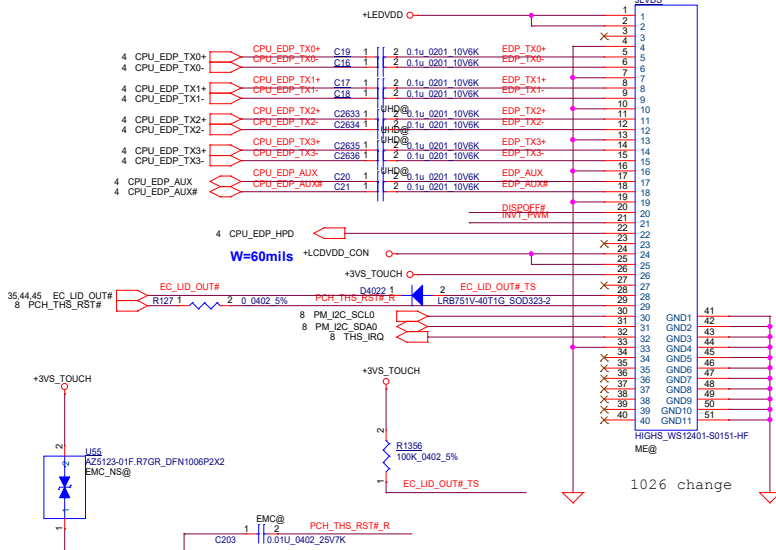
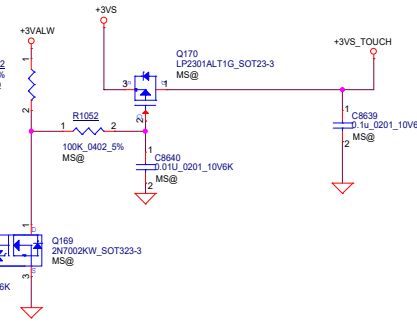
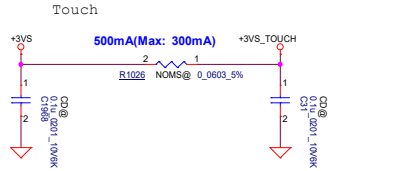
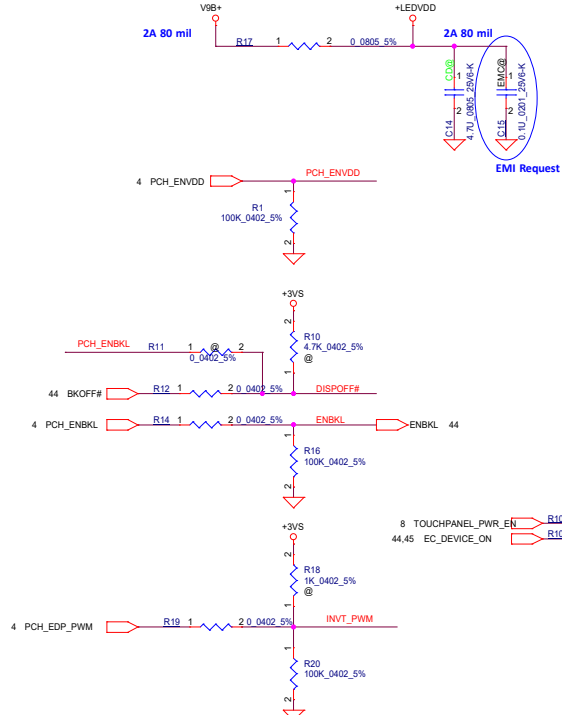
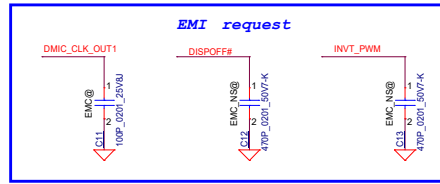
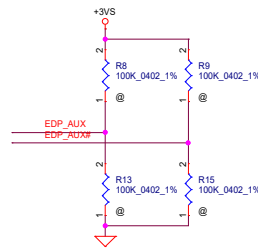
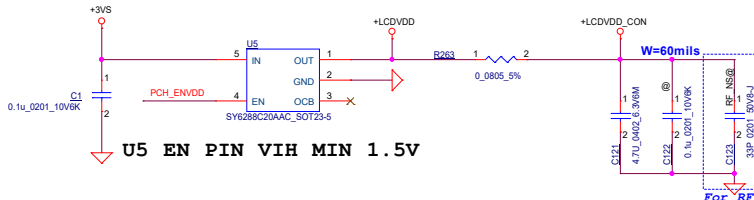


For ESD

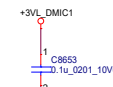
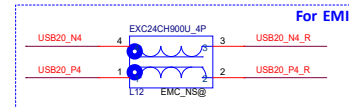
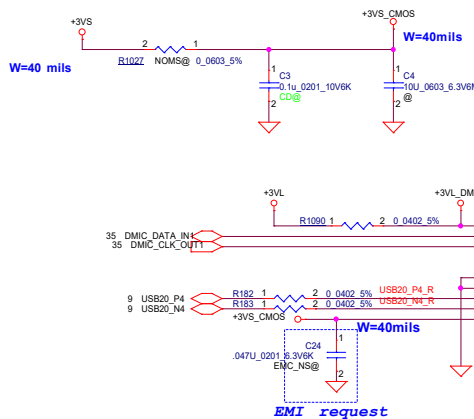


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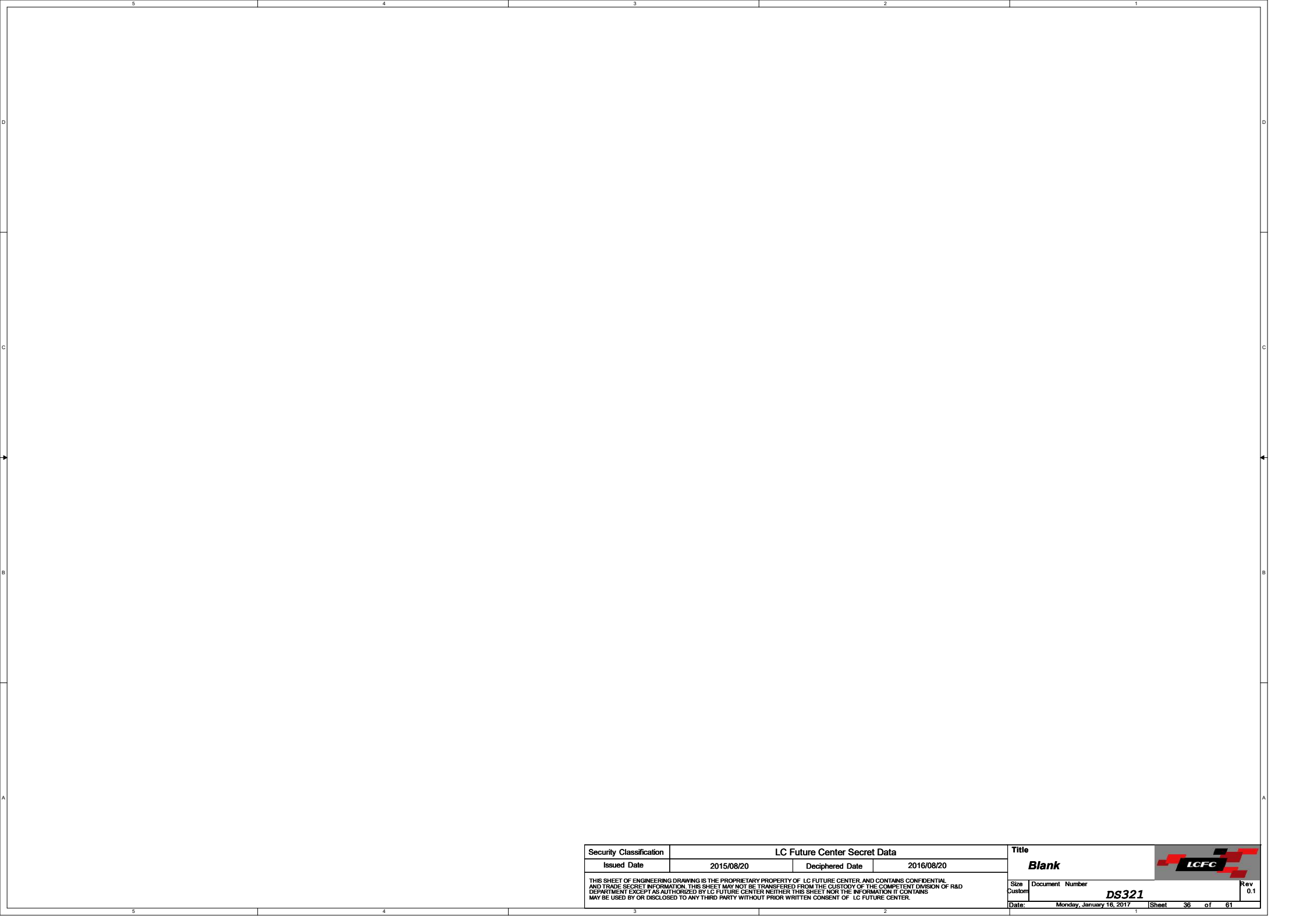
LCD POWER CIRCUIT



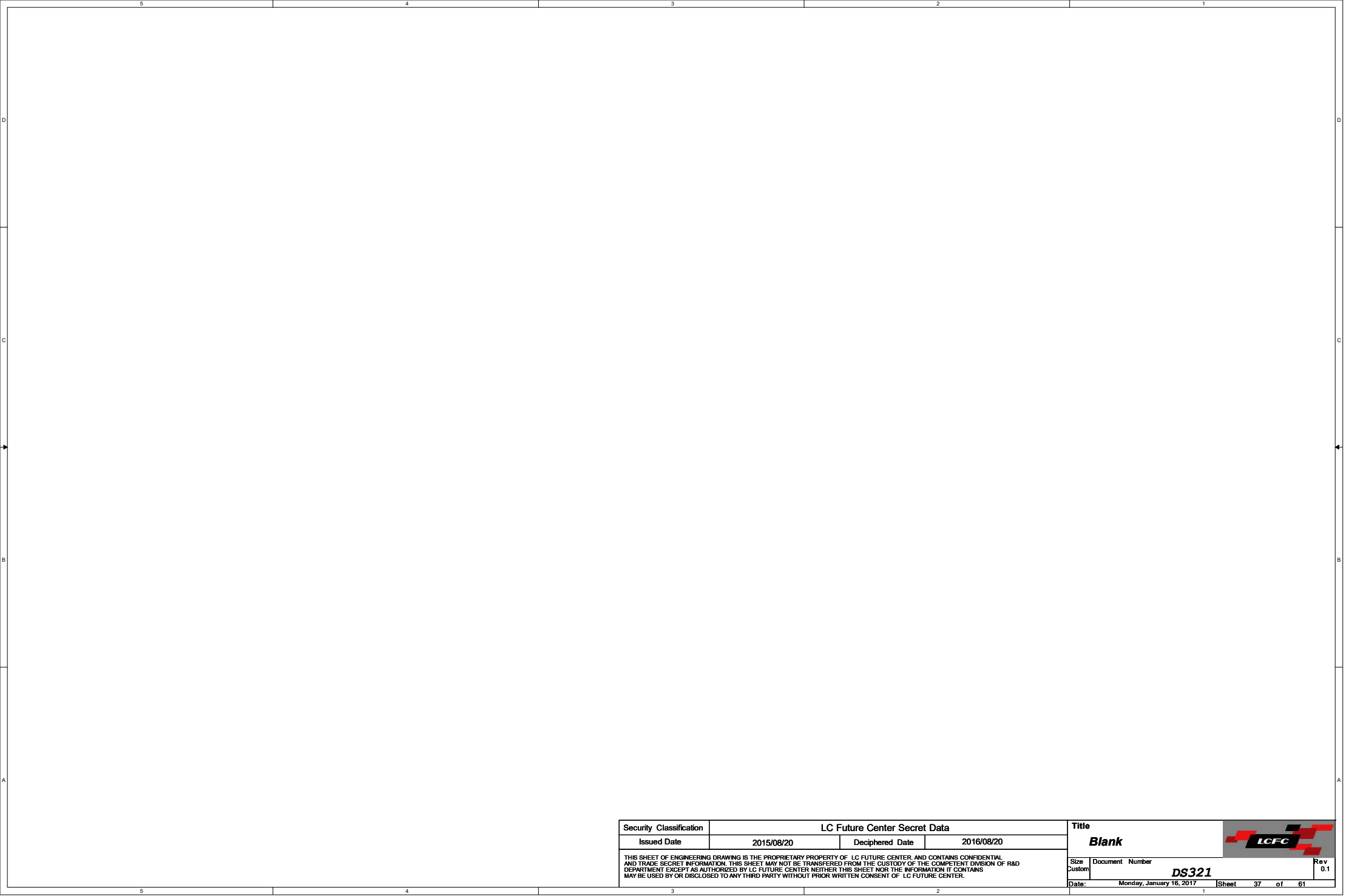
CMOS Camera



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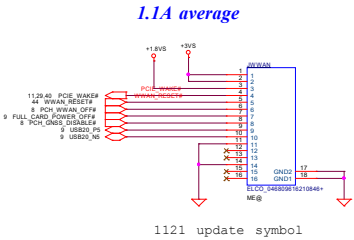


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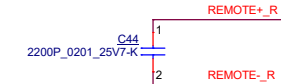


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Mini Card(WWAN)

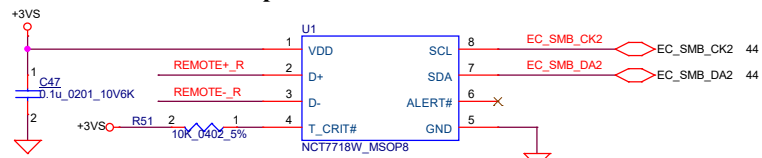


Close to U1



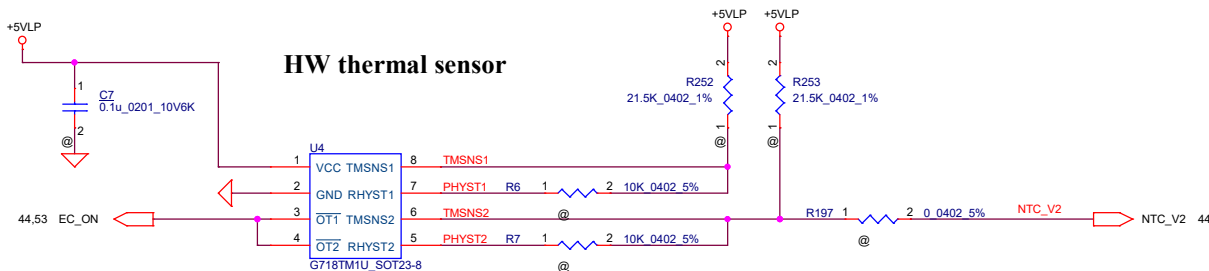
REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

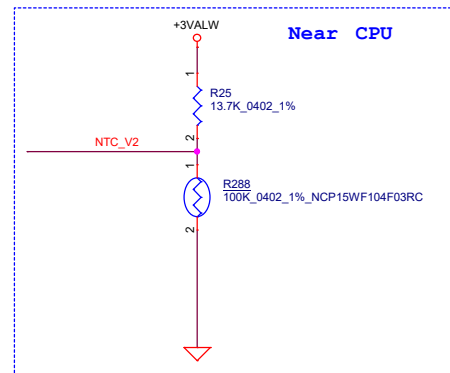
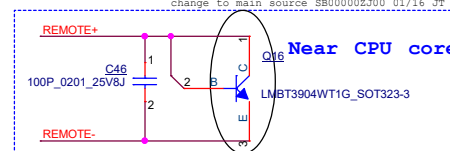


Address 1001_101xb

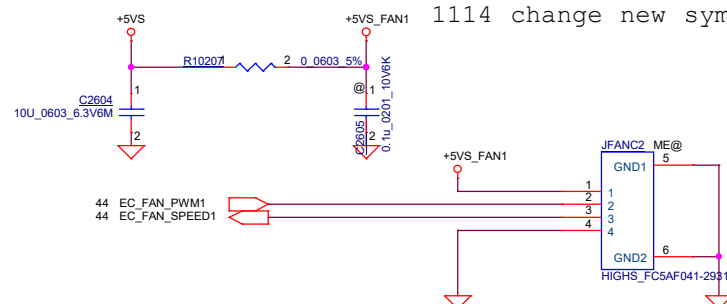
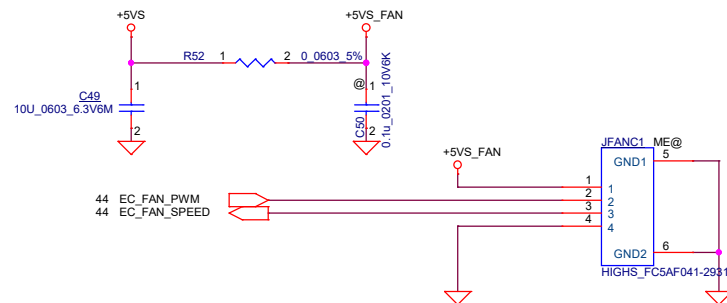
HW thermal sensor



over temperature threshold:
 $RSET = 3 * RTMH$
 $92 \pm 30C$
Hysteresis temperature threshold.
 $RHYST = (RSET * RTML) / (3 * RTML - RSET)$
 $56 \pm 30C$



for layout optimized, change the EC_AGND to GND

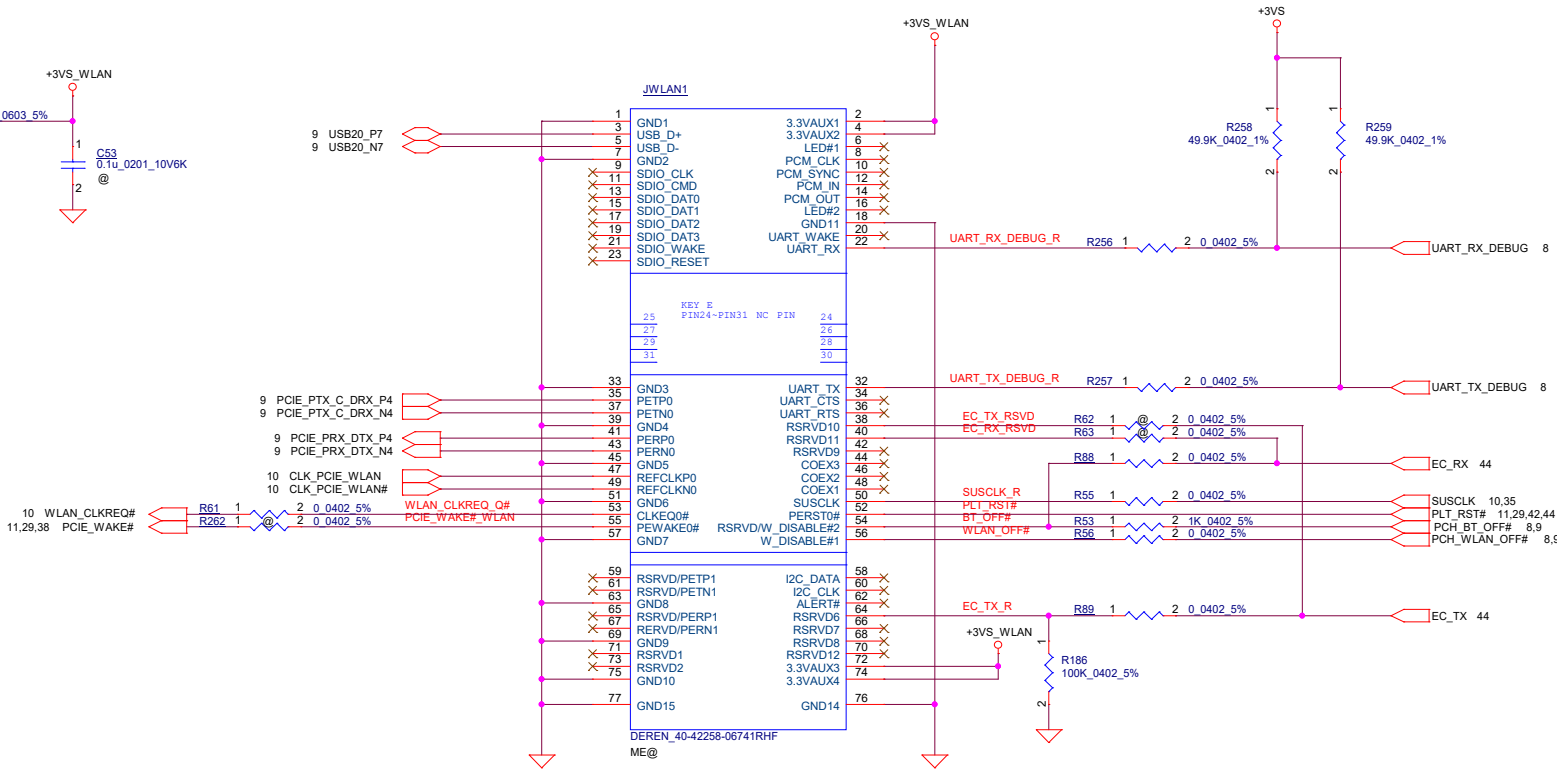


1114 change new symbol

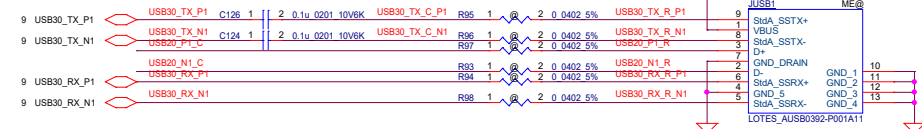
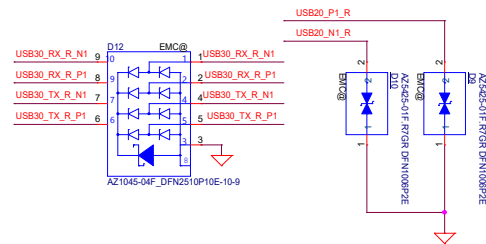
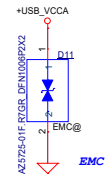
1114 change new symbol

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Issued Date	2015/08/20	Deciphered Date	2016/08/20	Thermal sensor/FAN CONN	
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				DS321	
				Date: Monday, January 16, 2017	Sheet 39 of 61

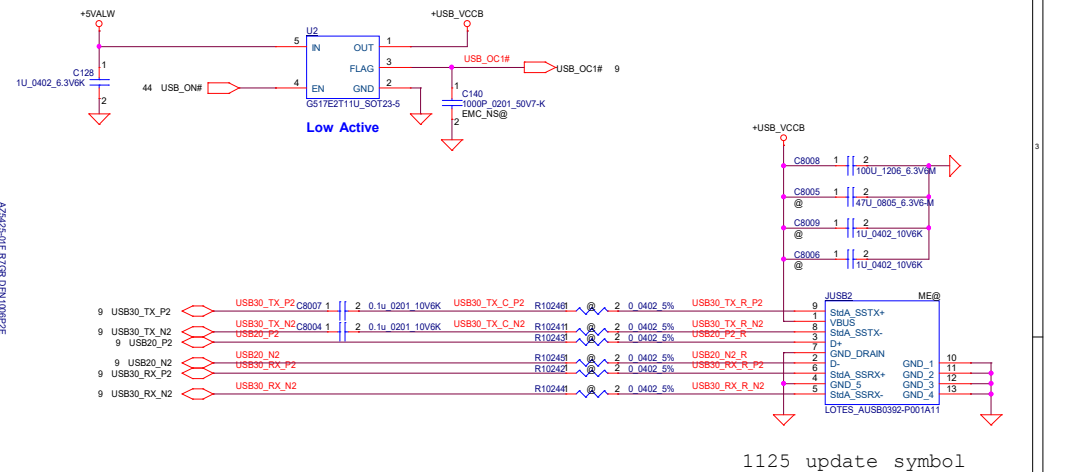
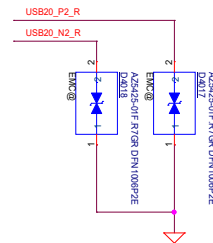
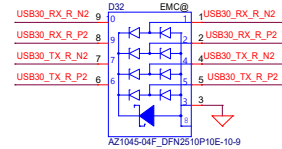
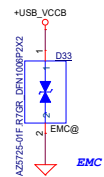
Mini-Express Card(WLAN/WiMAX)



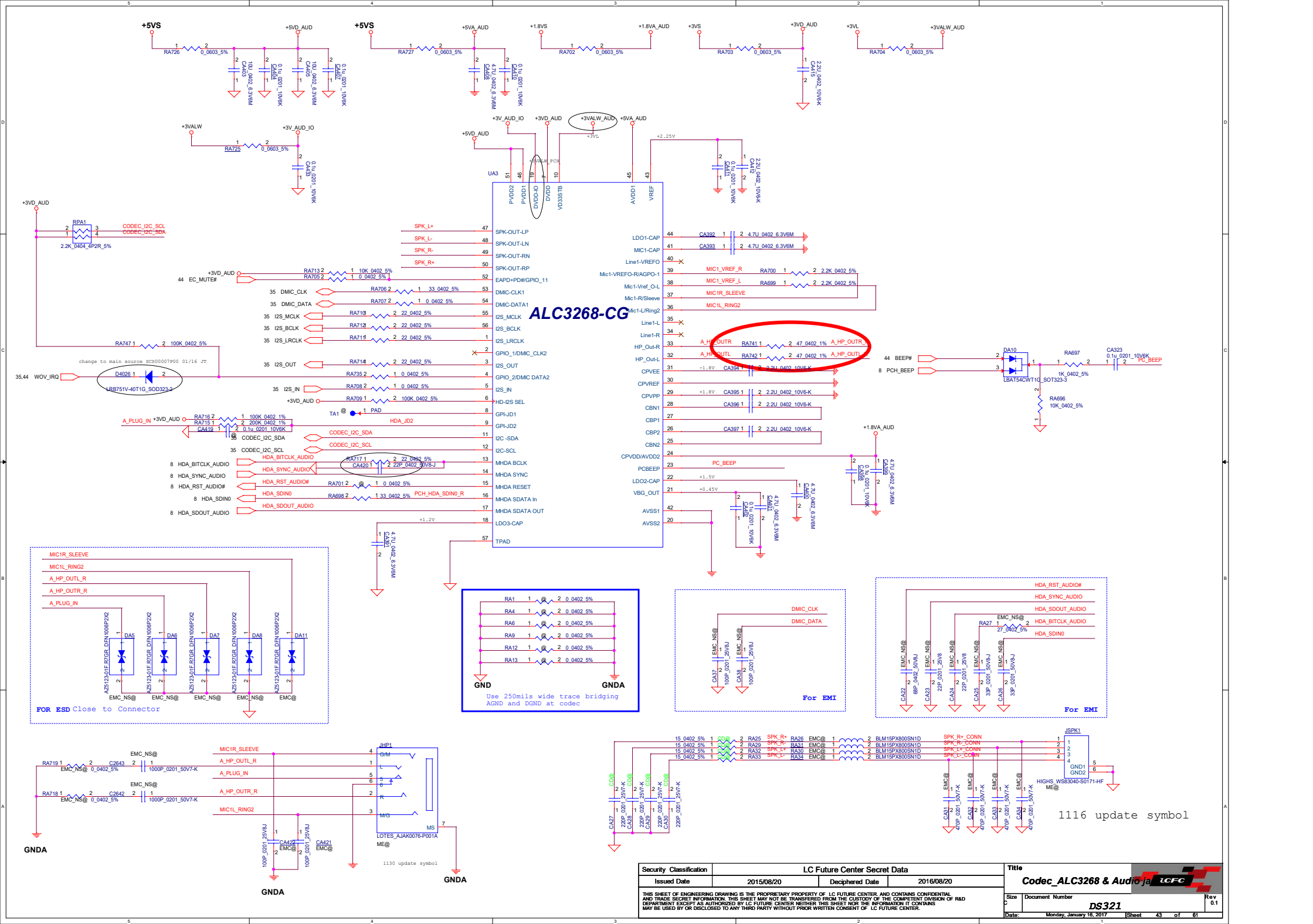
1114 change new symbol

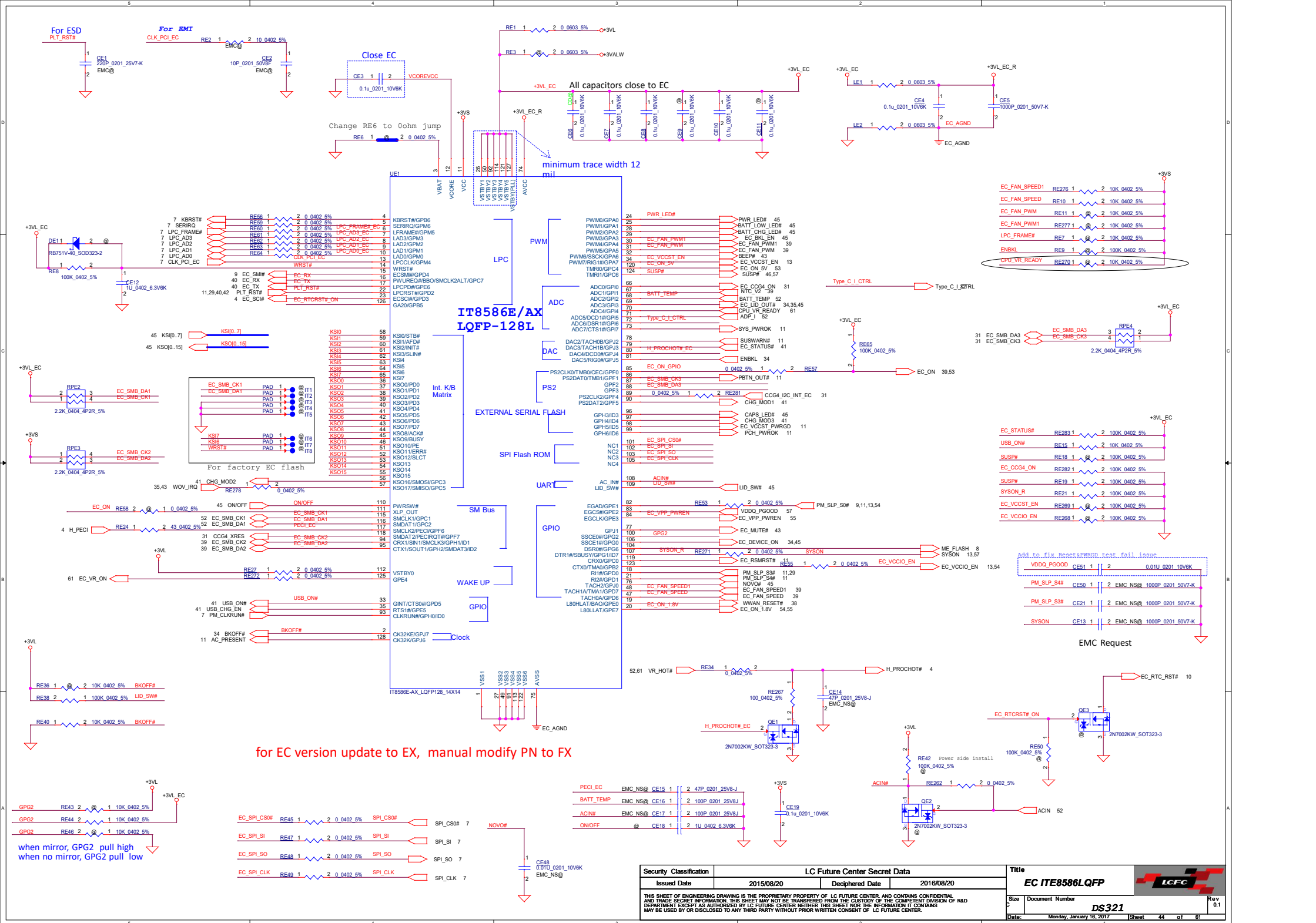
[illegible]

	pin number	6	7	8	4
	pin name	Ctl1	Ctl2	Ctl3	ILM_SE
Charge port Pin5 Enable H for all	S0 CDP	1	1	1	1
	S3 DCP	0	1	1	0/1
	S4/S5 DCP	0	0	1	0/1
Normal port Pin5 Enable H for S0/S3 L for S4/S5	S0 SDP1	1	1	0	0/1
	S3 SDP1	0	1	0	0/1
	S4/S5 Disable	0	0	0	0/1

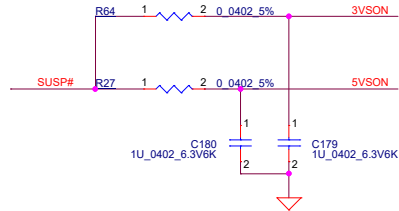


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Issued Date		2015/08/20		Deciphered Date		2016/08/20		USB3.0 PORT (Right/Left)			
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Date: Monday, January 18, 2017										Sheet 41 of 81	





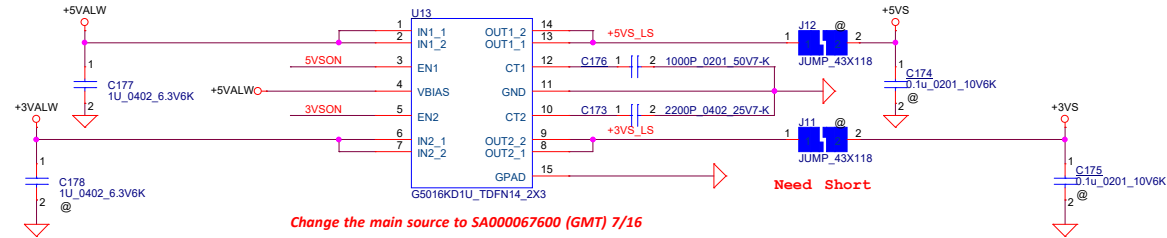
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Issued Date		Deciphered Date		EC ITE8586LQFP			
2015/08/20		2016/08/20		Size		Document Number	
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				DS321			
Date:				Monday, January 16, 2017		Sheet 44 of 61	



Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

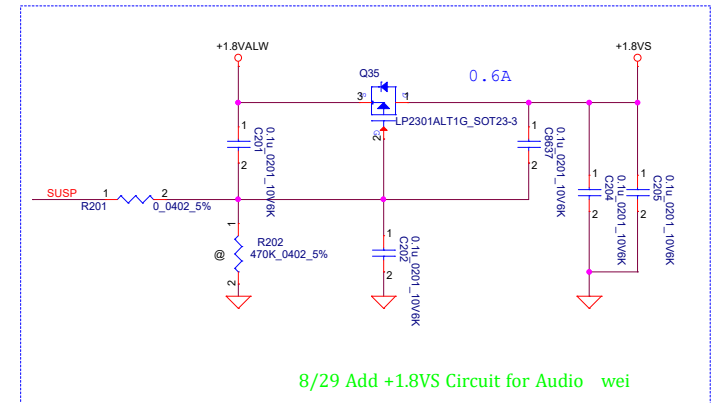
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm



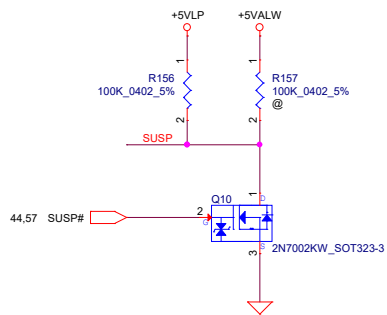
Change the main source to SA000067600 (GMT) 7/16



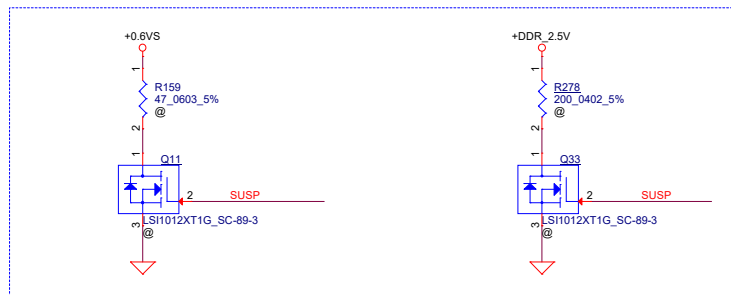
Need short



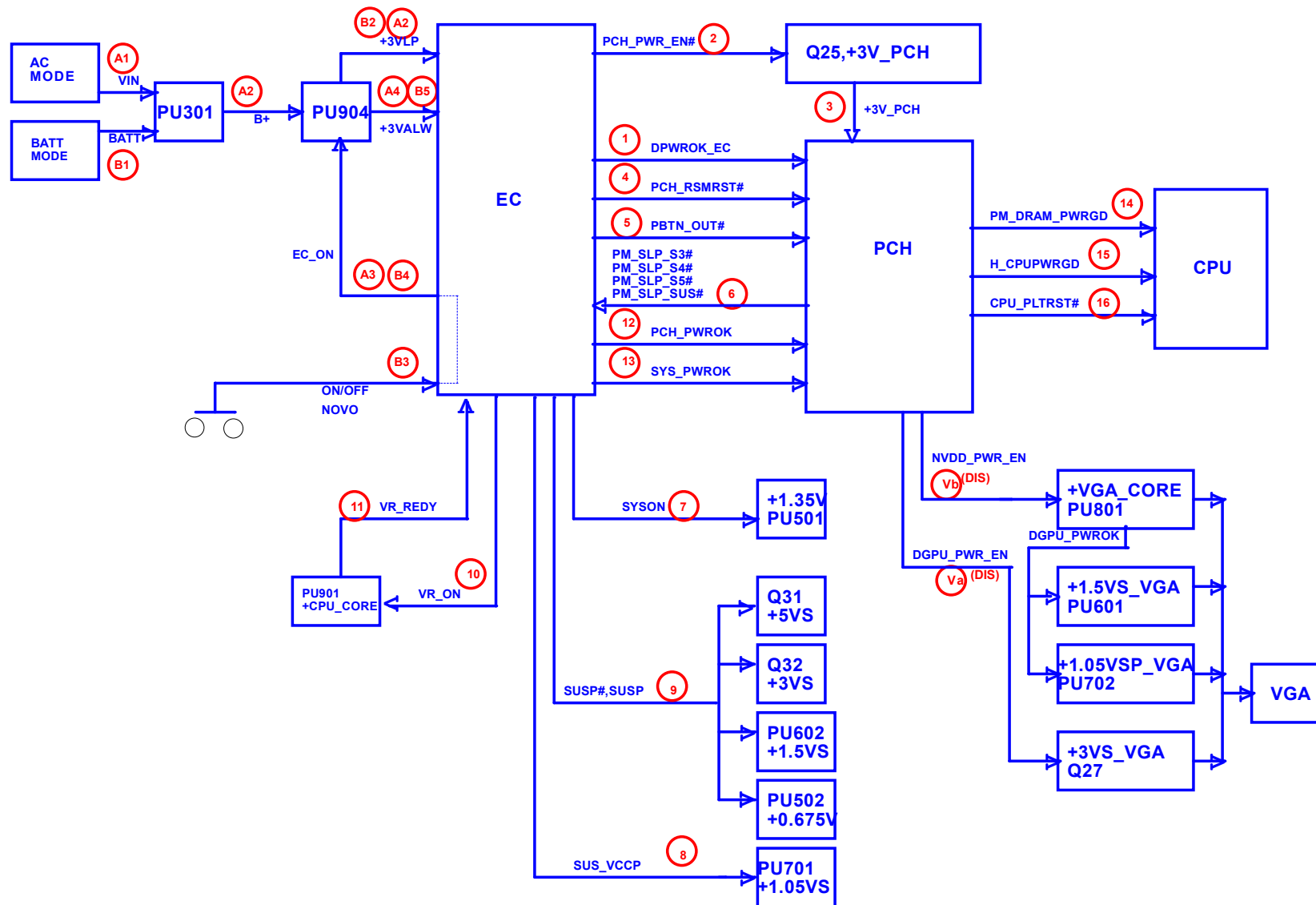
8/29 Add +1.8VS Circuit for Audio wei



For DisCharge



08/29: Need double check enable signal and the resistance



PCB And LOGO Config

PCB	ZZZ1 DAB@ PCB 149 NM-B331 REV0.MB	LOGO
CPU	ZZZ2 I7@ ZZZ10 I5@ ZZZ11 I3@ Intel I7-7500U 2.7G/2C/4MH Intel I5-7200U 2.5G/2C/3MH Intel I3-7100U 2.4G/2C/3MH	
VRAM	ZZZ4 MICR@ ZZZ5 MIC4@ ZZZ6 SAM@ ZZZ7 SAM4@ ZZZ9 HY4@ MICRON8G MICRON 4G SAMSUNG 8G SAMSUNG 4G HYNIX 4G	

PCB Federal Mark PAD

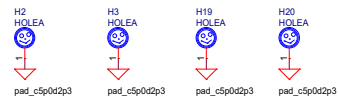


Pad_o2p0x2p2d2p0x2p2n



Pad_o2p0x2p2d2p0x2p2n

pad_c5p0d2p3



pad_c5p0d3p2



pad_c4p5d2p3



pad_o1p2x2p8d1p2x2p8n



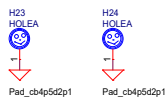
pad_o1p2x2p8d1p2x2p8n

pad_o4p0x2p0d4p0x2p0n



pad_o4p0x2p0d4p0x2p0n

Pad_cb4p5d2p1



Pad_ct4p0b4p5d2p1



Pad_ct4p0b4p5d2p1

Pad_o7p0x9p0d4p0x6p0



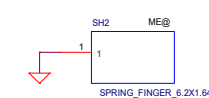
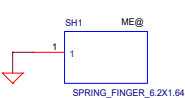
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PAD_C2P3D2P3N

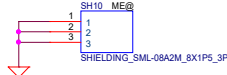
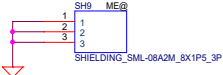
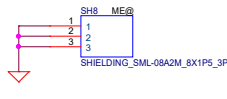
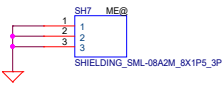
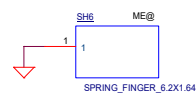
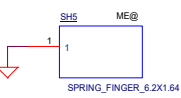
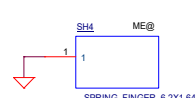
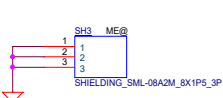


PAD_C2P3D2P3N

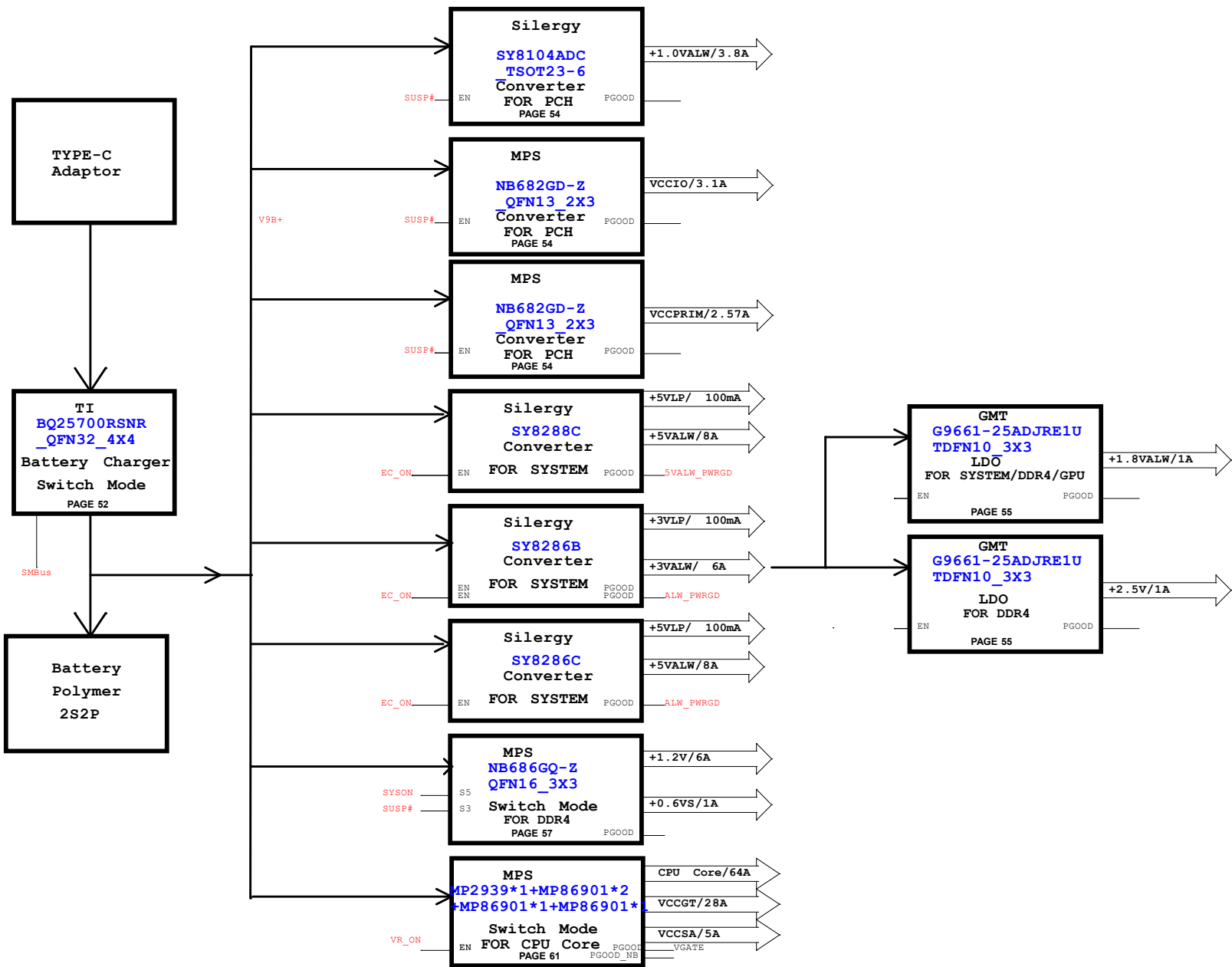
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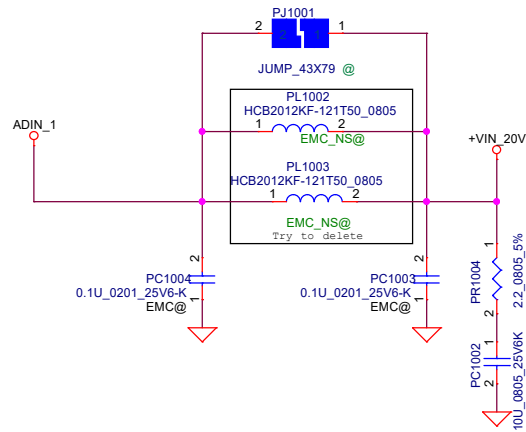


EMI-STOP_SML-08A2M

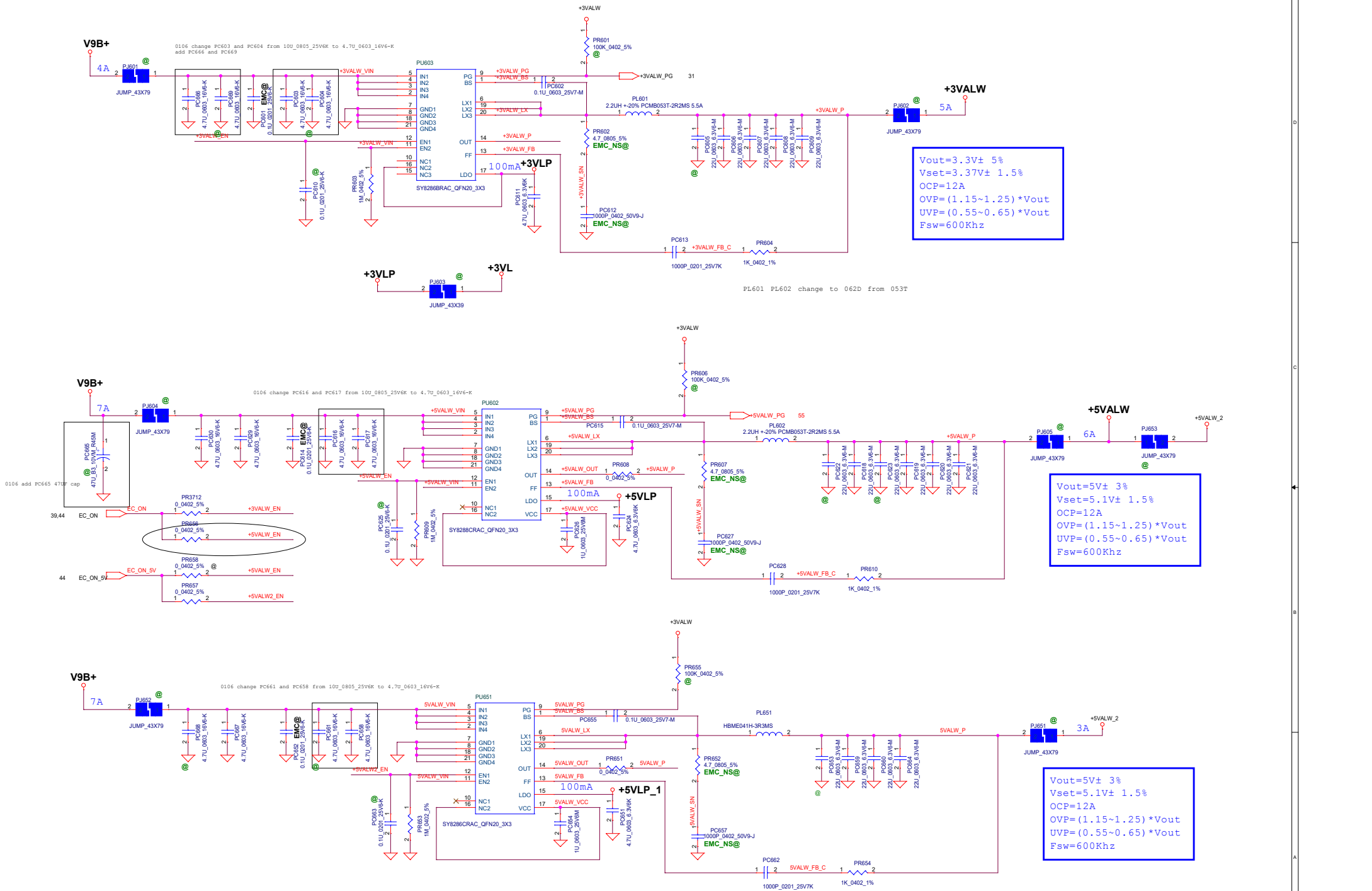


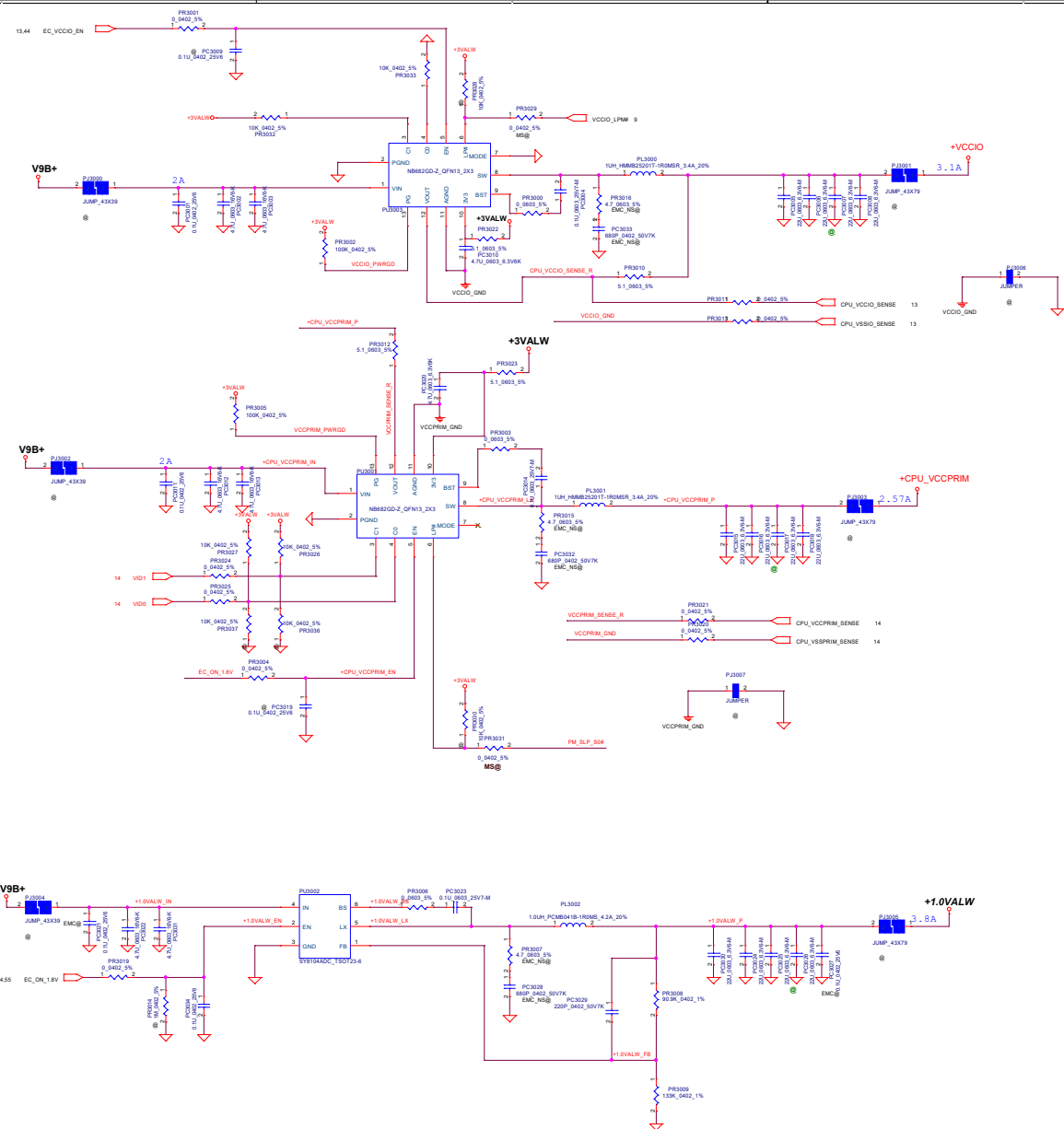
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	Hole		
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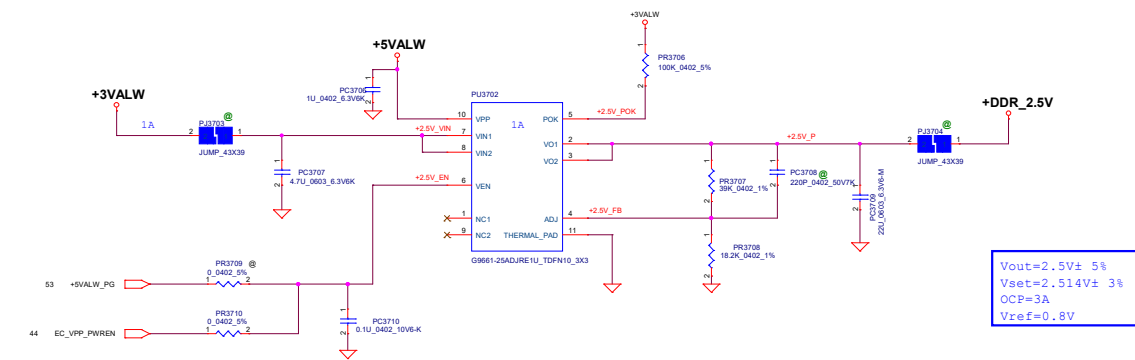
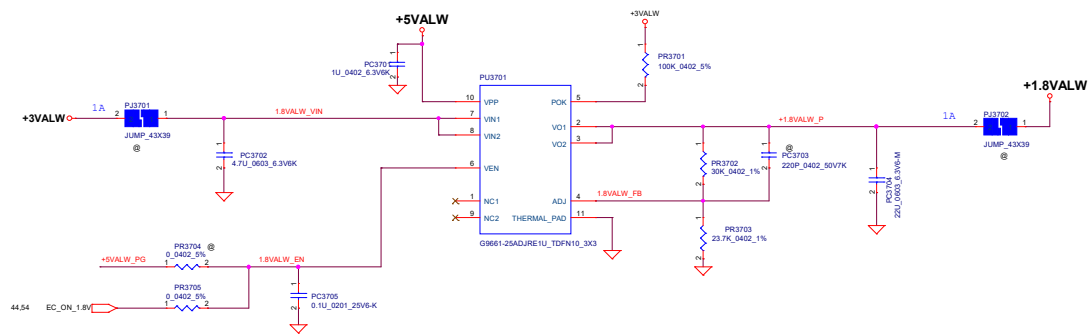




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Issued Date	2016/01/20	Deciphered Date	2016/01/20	PWR-XXXX		
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				Date:	Monday, January 16, 2017	Sheet 51 of 61

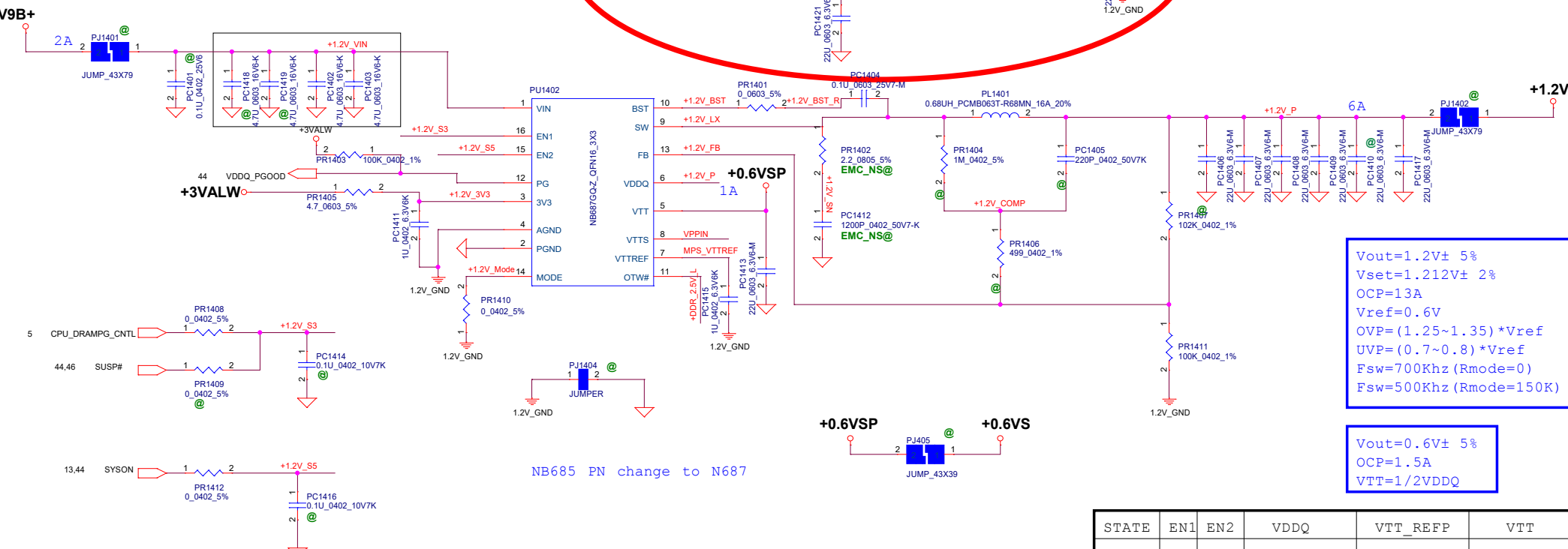
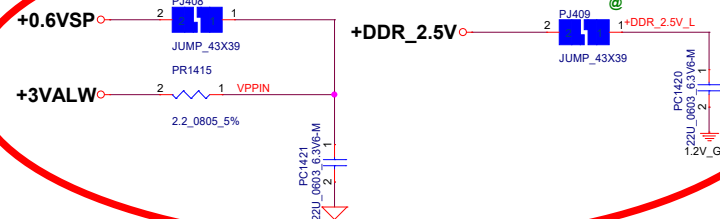






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D				D																								
C				C																								
B				B																								
A				A																								
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C	DS321	0.1																										
Date: Monday, January 16, 2017																												
5	4	3	2	1																								

NB687 must add below circuit



Vout=1.2V± 5%
Vset=1.212V± 2%
OCP=13A
Vref=0.6V
OVP=(1.25~1.35)*Vref
UVP=(0.7~0.8)*Vref
Fsw=700Khz (Rmode=0)
Fsw=500Khz (Rmode=150K)

Vout=0.6V± 5%
OCP=1.5A
VTT=1/2VDDQ

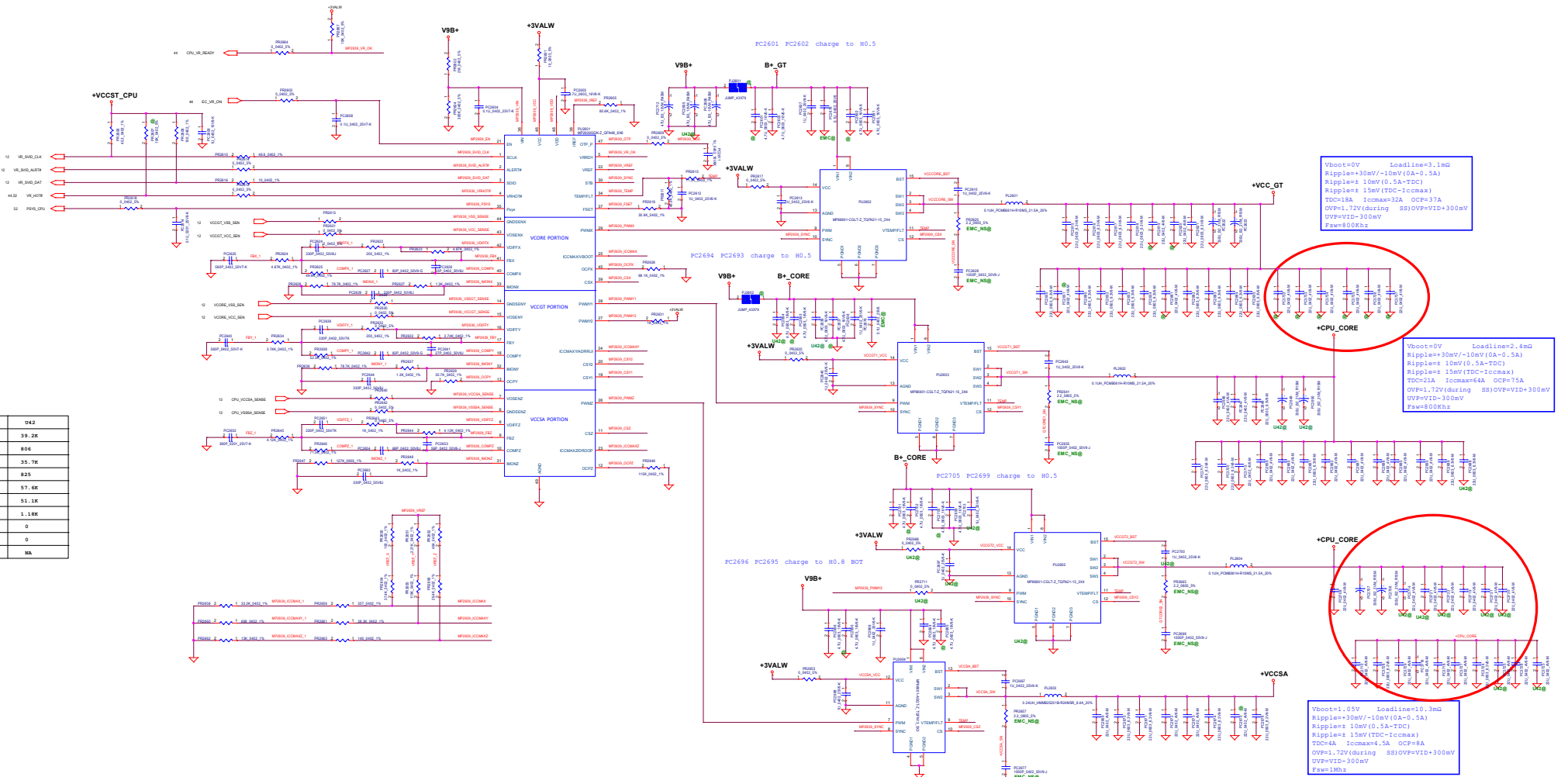
STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

5	4	3	2	1																										
D				D																										
C				C																										
B				B																										
A				A																										
<table><tr><td>Security Classification</td><td colspan="3">LC Future Center Secret Data</td><td>Title</td></tr><tr><td>Issued Date</td><td>2015/08/20</td><td>Deciphered Date</td><td>2016/08/20</td><td>Blank</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</td><td><table><tr><td>Size</td><td>Document Number</td><td>Rev</td></tr><tr><td>C</td><td>DS321</td><td>0.1</td></tr></table></td></tr><tr><td colspan="4">Date: Monday, January 16, 2017</td><td>Sheet 58 of 61</td></tr></table>					Security Classification	LC Future Center Secret Data			Title	Issued Date	2015/08/20	Deciphered Date	2016/08/20	Blank	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				<table><tr><td>Size</td><td>Document Number</td><td>Rev</td></tr><tr><td>C</td><td>DS321</td><td>0.1</td></tr></table>	Size	Document Number	Rev	C	DS321	0.1	Date: Monday, January 16, 2017				Sheet 58 of 61
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	Q22	Q42
PR2634	78.7K	39.2K
PR2637	1.3K	90K
PR2639	35.7K	35.7K
PR2651	182	825
PR2655	37.4K	57.6K
PR2660	12.4K	55.1K
PR2661	150	1.18K
PR2668	NA	0
PR2669	NA	0
PR2631	1K	NA



Vboot=0V Loadline=3.1mΩ
 Ripple=±30mV/-10mV(0A-0.5A)
 Ripple=±10mV(0.5A-TDC)
 Ripple=±15mV(TDC-Iccmax)
 TDC=18A Iccmax=32A OCP=37A
 OVP=1.72V(during SS)OVP=VID+300mV
 UV=VID-300mV
 Fsw=800KHz

Vboot=0V Loadline=2.4mΩ
 Ripple=±30mV/-10mV(0A-0.5A)
 Ripple=±10mV(0.5A-TDC)
 Ripple=±15mV(TDC-Iccmax)
 TDC=21A Iccmax=64A OCP=75A
 OVP=1.72V(during SS)OVP=VID+300mV
 UV=VID-300mV
 Fsw=800KHz

Vboot=1.05V Loadline=0.3mΩ
 Ripple=±30mV/-10mV(0A-0.5A)
 Ripple=±10mV(0.5A-TDC)
 Ripple=±15mV(TDC-Iccmax)
 TDC=4A Iccmax=4.5A OCP=8A
 OVP=1.72V(during SS)OVP=VID+300mV
 UV=VID-300mV
 Fsw=1MHz