Compal Confidential

A4WAD MB Schematic Document

LA-C871P

Rev: 1.0

2015.07.13

DAX

Part Number	Description
DA6001ED010	PCB 1DS LA-C871P REV1 MB 1

A4WAD_PCB_REV10
PCB@

DAZ

Part Number	Description
DAZ1DS00100	PCB A4WAD LA-C871P LS-C341P

A4WAD_PCB_Panelization
@

Security Classification	Compal Secret Data		
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Title: Cover Sheet

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eDP

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Skylake H PROCESSOR
BGA1440
(42X28) (SKL-H_2+2)

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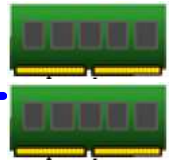
Memory BUS
Dual Channel

1.35V DDR3L 1333/1600

Interleaved Memory



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SATA3.0
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Int.KBD

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Title: Block Diagrams

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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3
0	0	0 V	0 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64

Power State

STATE	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	0.7
7	0.8

BOM Structure Table

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
EMC requirement	EMC@
EMC requirement depop	@EMC@
CODEC(ALC255)	255@
CODEC(ALC283)	283@
SPI ROM 8M*2	8M_DUAL@
SPI ROM 8M*1	8M_SINGLE@
UMA only	UMA@
TPM	TPM@
CMC	CMC@
Keyboard backlight	KB@
LPC MODE for EC	LPC@
ESPI MODE for EC	ESPI@
BA Serial	BA@

BOM Option Table

Item	BOM Structure
dGPU	VGA@
N16S-GT	SGT@
N16V-GM	VGM@
Non GPU CG6 funct i on	NGC6@
GPU CG6 funct i on	GC6@
VRAM BOM Select	X76@
DMIC*1	DMIC@
For Acer IOAC	IOAC@
No Acer IOAC	NIOAC@

Voltage Rails (TBC)

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
VIN	Adapter power supply	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW_PCH	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW_SPI	+3VALW_PRIM supply for the SPI IO	ON	ON	ON	ON
+1.0VALW	+1.0V Always power rail	ON	ON	ON	ON
+1.35V_VDDQ	DDRIIIL/L-RS +1.35V power rail	ON	ON	OFF	OFF
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.675VS_VTT	DDR +0.675VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+3VSDGPU_AON	+3VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+3VSDGPU_MAIN	+3VS power rail for GPU GC62.0	ON	OFF	OFF	OFF
+VGA_CORE	Core voltage for VGA	ON	OFF	OFF	OFF
+1.8VSDGPU	+1.8VS power rail for GPU	ON	OFF	OFF	OFF
+1.5VSDGPU	+1.5VS power rail for GPU	ON	OFF	OFF	OFF
+1.05VSDGPU	+1.05VS power rail for GPU	ON	OFF	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

I2C Address Table (TBC)

BUS	Device	Address(7 bit)	Address(8bit) Write	Address(8bit) Read
I2C_0 (+3VS)	Touch Panel	reserved		
I2C_1 (+3VS)	TM-P2969-001 (Touch Pad)	0x2C		
	SB8787-1200 (Touch Pad)	0x15		
PCH_SMBCLK (+3VALW)	DIMM1	0xA0		
	DIMM2	0xA4		
	LIS3DHTR(G-sensor)	0x30		
PCH_SML1CLK (+3VALW)	N16S-GT (VGA)	0x9E		
	RTD2168 (CRT)	reserved		
	EC			
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

43 level BOM table

43 Level	Description	BOM Structure
4319YYBOL01	SMT MB AC871 A4WAD QHR7 1.6G UMA HDMI	QHR7@/1DMIC@/255@/8M_SINGLE@/BA@/EMC@/IOAC@/KB@/LPC@/PCB@/PCH@/TPM@/XDP@/ES@/UMA@
4319YYBOL02	SMT MB AC871 A4WAD QHR7 1.6G GM2G HDMI	QHR7@/1DMIC@/255@/8M_SINGLE@/BA@/EMC@/IOAC@/KB@/LPC@/PCB@/PCH@/TPM@/XDP@/ES@/VGA@/VGM@/NGC6@/X7601@
4319YYBOL03	SMT MB AC871 A4WAD QHPW 2.2G GM2G HDMI	QHPW@/1DMIC@/255@/8M_SINGLE@/BA@/EMC@/IOAC@/KB@/LPC@/PCB@/PCH@/TPM@/XDP@/ES@/VGA@/VGM@/NGC6@/X7601@
4319YYBOL04	SMT MB AC871 A4WAD QHPW 2.2G GT2G HDMI	QHPW@/1DMIC@/255@/8M_SINGLE@/BA@/EMC@/IOAC@/KB@/LPC@/PCB@/PCH@/TPM@/XDP@/ES@/VGA@/SGT@/GC6@/X7603@/

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Title: Notes List

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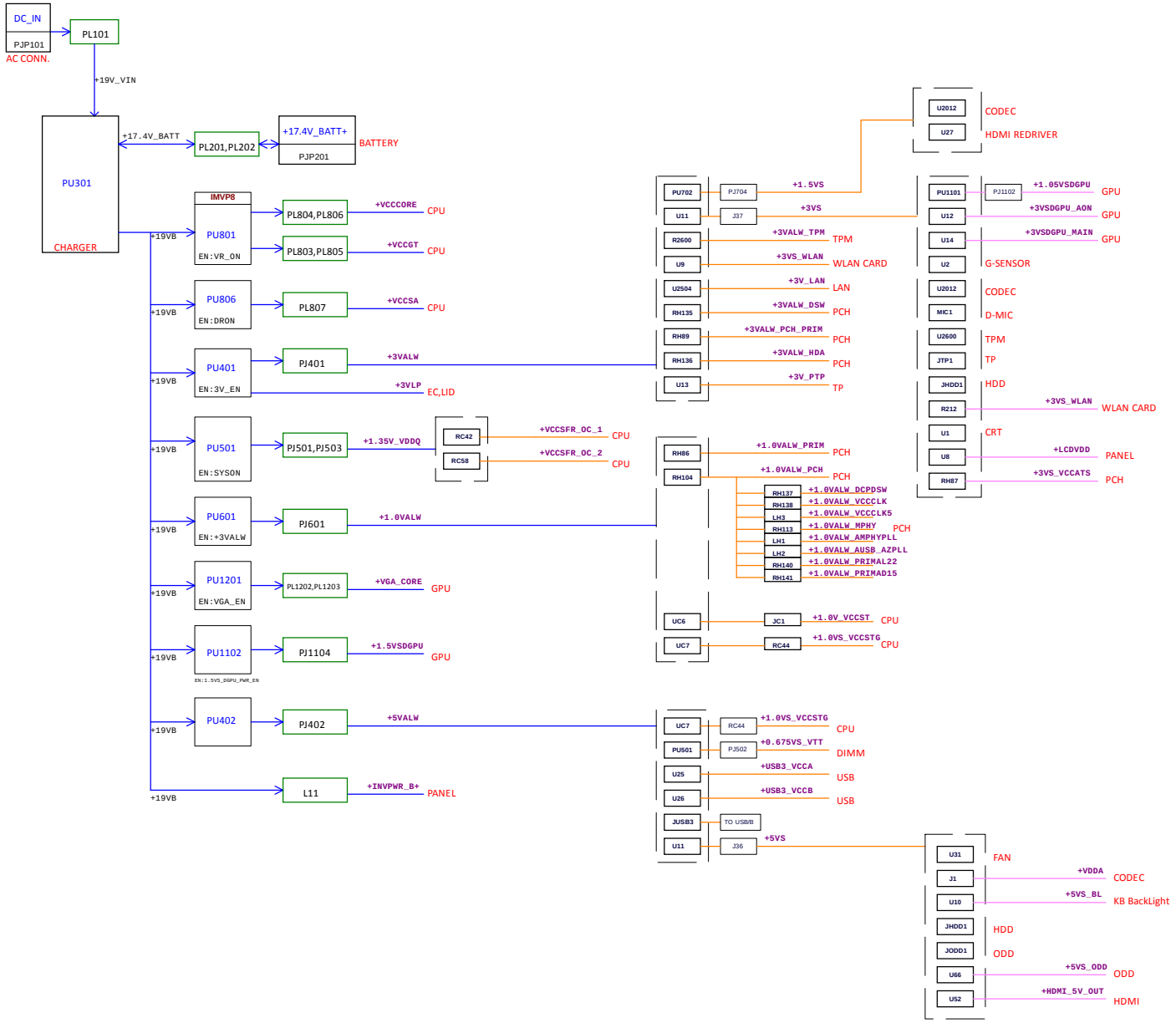

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/01/01	Deciphered Date	2016/12/31	Title: Power Map
Size: B	Document Number: A4WAD M/B LA-C971P		Rev: 1.0
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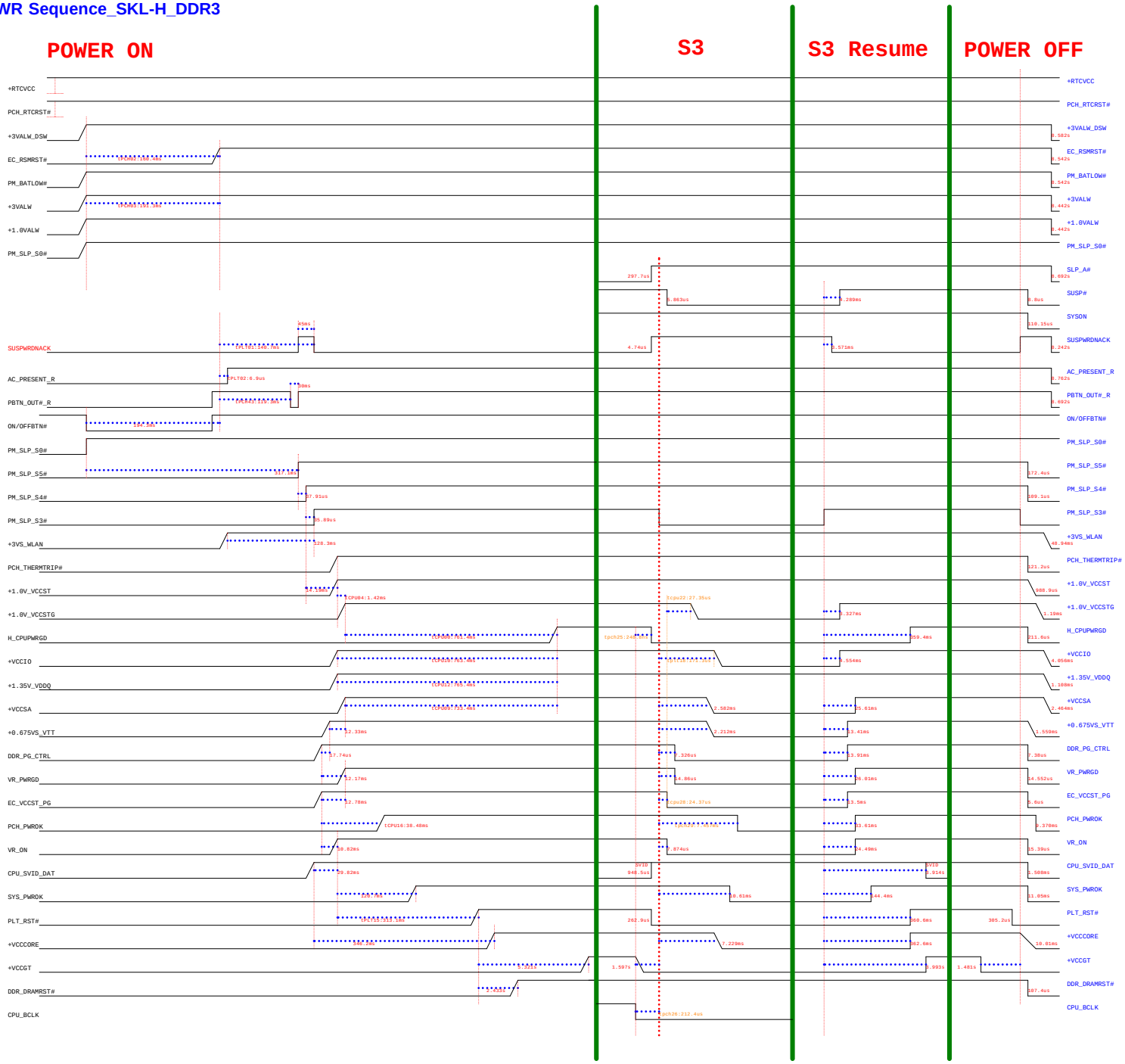
PWR Sequence_SKL-H_DDR3



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Compal Electronics, Inc.

Title: Power Sequence

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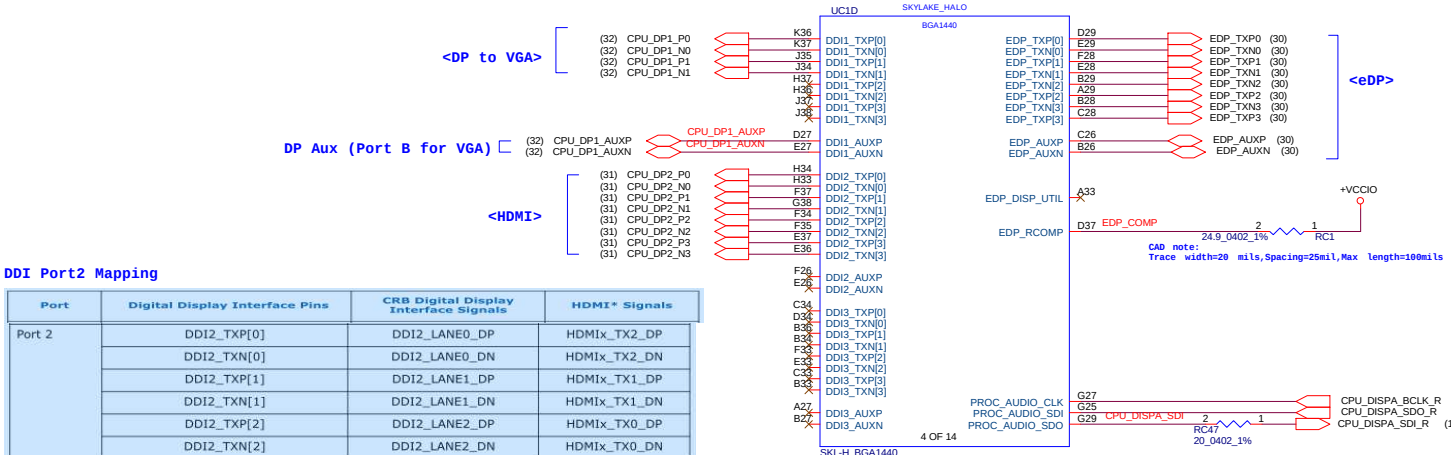
UC1 QJJQ QJJQ@ SA000096Q00

UC1 QJJR QJJR@ SA000095Z10

UC1 QHR7 QHR7@ SA00008RP00

UC1 QHPW QHPW@ SA00008RQ00



Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
59	GND	GND	NA		60	GND[3] (XDP_PRESENT#)	See XDP_PRESENT# routing guidelines	NA	system

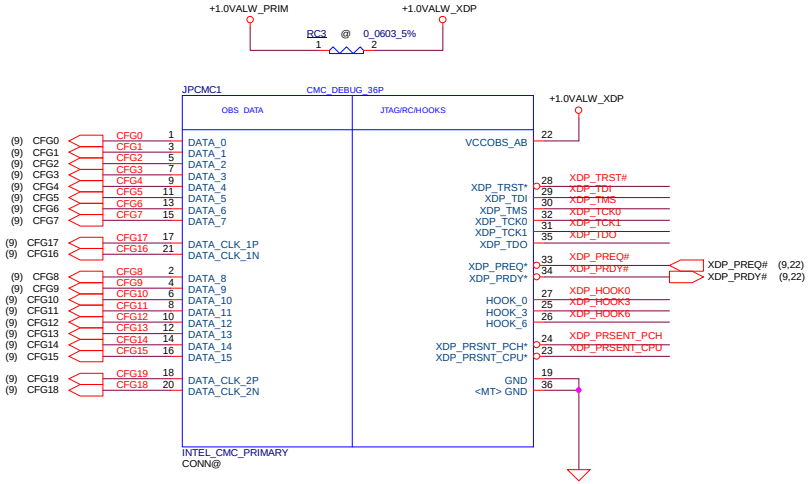
Notes:
1. These signals are optional, can be left as OPEN/No-Connect.
2. See XDP_PRESENT# routing guidelines for additional routing guidelines.
3. Routing of this signal to CFG[0] is OPTIONAL.

1	XDP_Rsvd[2]	See XDP_PRESENT# routing guidelines	NA	Skylake	2	GND	GND	NA	
3	OBSFN_A0	PROC_PREQ#	O	Skylake	4	OBSFN_C0	CFG[17]	I	Skylake
5	OBSFN_A1	PROC_PRDY#	I	Skylake	6	OBSFN_C1	CFG[18]	I	Skylake
7	GND	GND	NA		8	GND	GND	NA	
9	OBSDATA_A0	CFG[0]	I/O	Skylake	10	OBSDATA_C0	CFG[8]	I/O	Skylake
11	OBSDATA_A1	CFG[1]	I/O	Skylake	12	OBSDATA_C1	CFG[9]	I/O	Skylake
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2	CFG[2]	I/O	Skylake	16	OBSDATA_C2	CFG[10]	I/O	Skylake
17	OBSDATA_A3	CFG[3]	I/O	Skylake	18	OBSDATA_C3	CFG[11]	I/O	Skylake
19	GND	GND	NA		20	GND	GND	NA	
21	OBSFN_B0	BPM#[0]	I/O	Skylake	22	OBSFN_D0	CFG[19]	I	Skylake
23	OBSFN_B1	BPM#[1]	I/O	Skylake	24	OBSFN_D1	CFG[18]	I	Skylake
25	GND	GND	NA		26	GND	GND	NA	
27	OBSDATA_B0	CFG[4]	I/O	Skylake	28	OBSDATA_D0	CFG[12]	I/O	Skylake
29	OBSDATA_B1	CFG[5]	I/O	Skylake	30	OBSDATA_D1	CFG[13]	I/O	Skylake
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2	CFG[6]	I/O	Skylake	34	OBSDATA_D2	CFG[14]	I/O	Skylake
35	OBSDATA_B3	CFG[7]	I/O	Skylake	36	OBSDATA_D3	CFG[15]	I/O	Skylake
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK0	RSVRSTF#	I	Skylake	40	ITPCLK1/HOOK4[1]	CLKOUT_ITPX DP_P	I	Skylake
41	HOOK1	PWRBTN#	O	Skylake	42	ITPCLK#/HOOK5	CLKOUT_ITPX DP_N	I	Skylake
43	VCC_OBS_AB	PCH V1.0A	NA		44	VCC_OBS_CD	PCH V1.0A	NA	
45	HOOK3[2]	Open	NA		46	HOOK6/RESET#	ITP_PMODE	I	Skylake
47	HOOK7[2]	SPI0_MOSI	O	Skylake	48	HOOK7/DBR#	SYS_RESET#	O	Skylake
49	GND	GND	NA		50	GND	GND	NA	
51	XDP_BOA[3]	SDA	I/O	system	52	XDP_TDO	PROC_TDO / PCH_JTAG_TD O	I	Skylake
53	XDP_BCL[3]	SCL	I/O	system	54	XDP_TRSTn	PROC_TRST# / PCH_TRST#	O	Skylake
55	XDP_TDI1	PCH_JTAG_TCK	O	Skylake	56	XDP_TDI	PROC_TDI / PCH_JTAG_TDI	O	Skylake
57	XDP_TCK0	PROC_TCK / JTAGX	O	Skylake	58	XDP_THS	PROC_THS / PCH_JTAG_TH S	O	Skylake

DDI Port2 Mapping

Port	Digital Display Interface Pins	CRB Digital Display Interface Signals	HDMI* Signals
Port 2	DDI2_TXP[0]	DDI2_LANE0_DP	HDMIx_TX2_DP
	DDI2_TXN[0]	DDI2_LANE0_DN	HDMIx_TX2_DN
	DDI2_TXP[1]	DDI2_LANE1_DP	HDMIx_TX1_DP
	DDI2_TXN[1]	DDI2_LANE1_DN	HDMIx_TX1_DN
	DDI2_TXP[2]	DDI2_LANE2_DP	HDMIx_TX0_DP
	DDI2_TXN[2]	DDI2_LANE2_DN	HDMIx_TX0_DN
	DDI2_TXP[3]	DDI2_LANE3_DP	HDMIx_CLK_DP
	DDI2_TXN[3]	DDI2_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 2	DDPC_HPD	DDI2_HPD_Q
	HDMI DDC lines for Port 2	DDPC_CTRLCLK	DDI2_CTRL_CK
		DDPC_CTRLDATA	DDI2_CTRL_DATA

CMC CONN



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Compal Electronics, Inc.

Title: SKL-H(1/9)DDI,EDP

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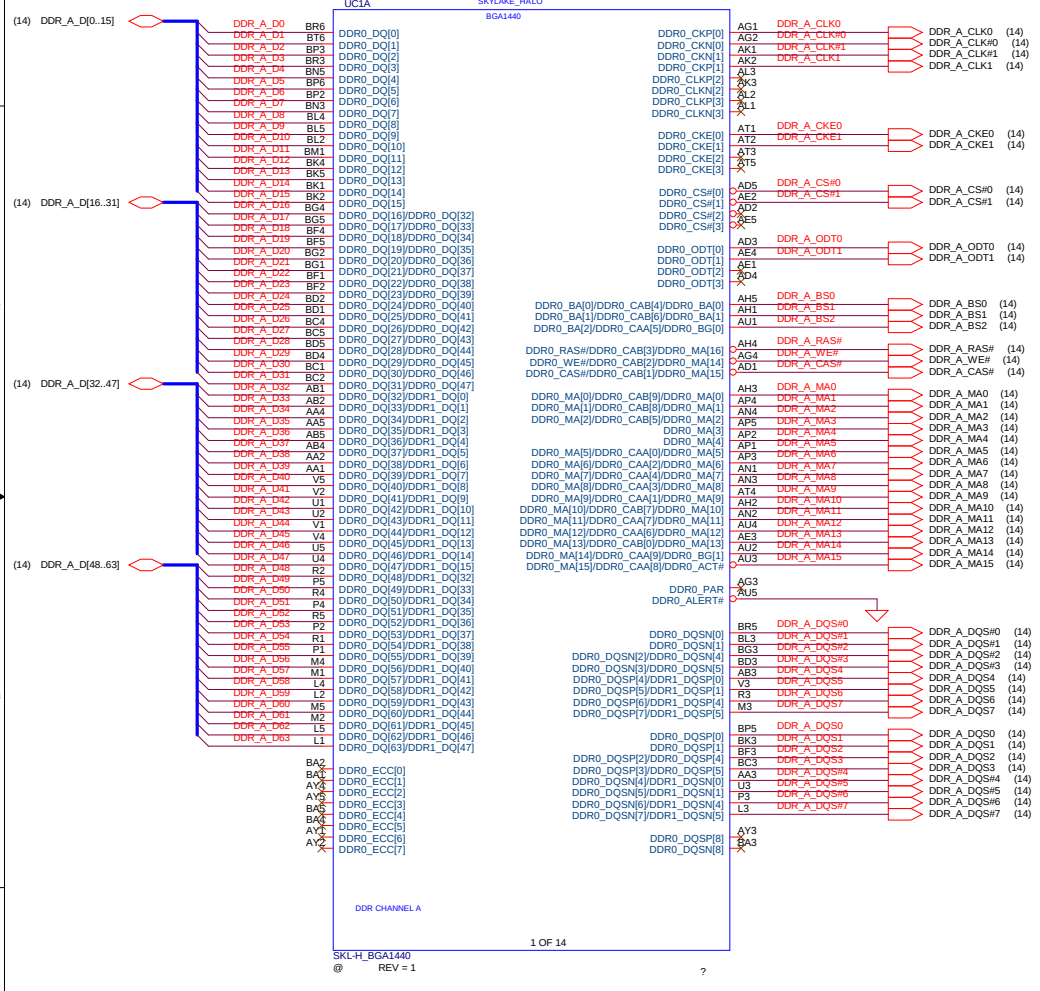
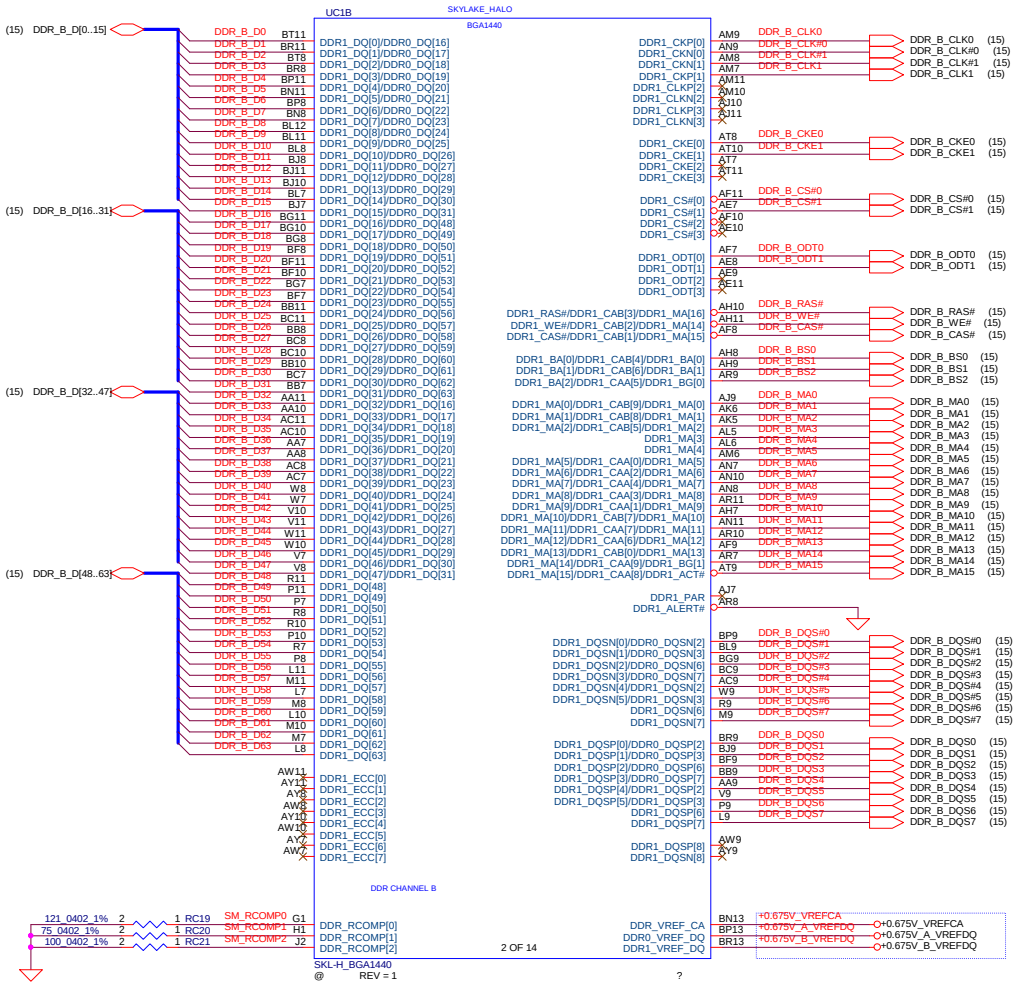
Interleaved Memory





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Title: **SKL-H(2/9)DDRIII**

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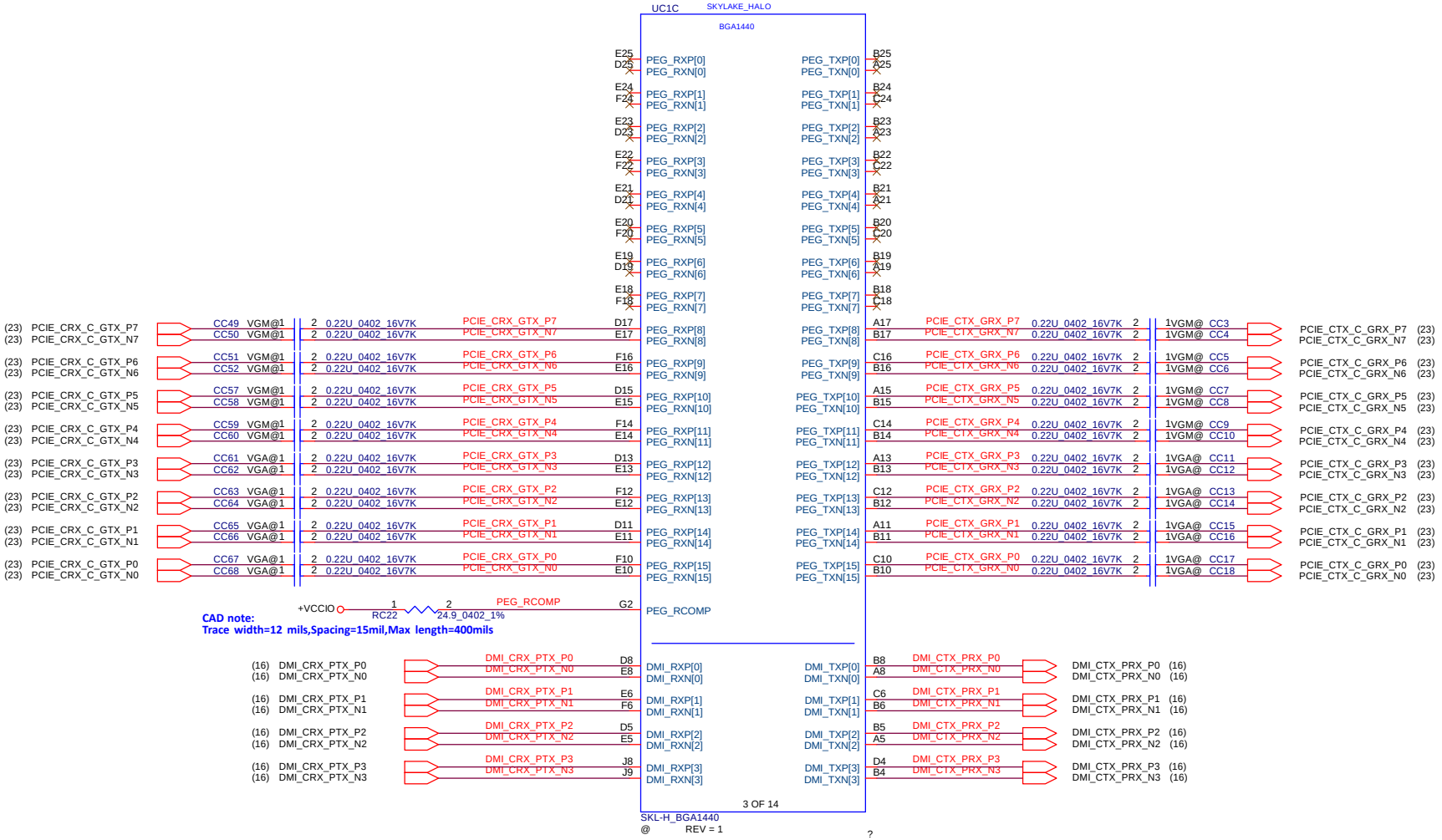
UC1C
SKYLAKE_HALO
BGA1440
PEG_RXP[0]
PEG_RXN[0]
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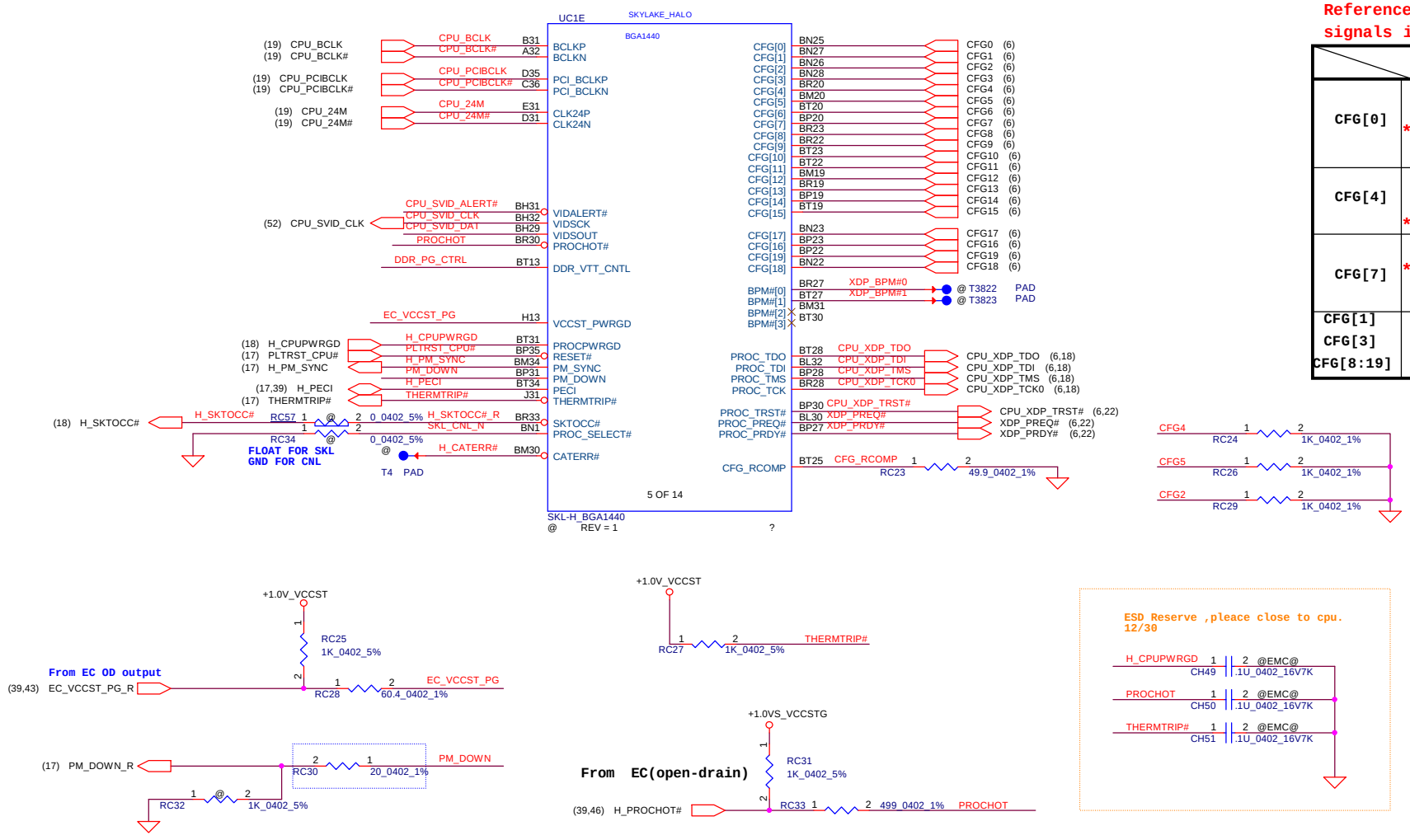
PEG_TXP[15]
PEG_TXN[15]
PEG_RCOMP
DMI_RXP[0]
DMI_RXN[0]
DMI_TXP[0]
DMI_TXN[0]
DMI_RXP[1]
DMI_RXN[1]
DMI_TXP[1]
DMI_TXN[1]
DMI_RXP[2]
DMI_RXN[2]
DMI_TXP[2]
DMI_TXN[2]
DMI_RXP[3]
DMI_RXN[3]
DMI_TXP[3]
DMI_TXN[3]
3 OF 14
SKL-H_BGA1440
@ REV = 1
+VCCIO
RC22
24.9_0402_1%
CAD note:
Trace width=12 mils,Spacing=15mil,Max length=400mils

Reference SKL EDS 0.85 Table 6-8CFG signals internal PH default value = 1

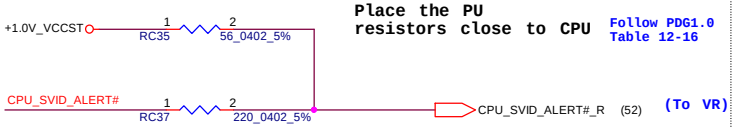
		Description
CFG[0]	*	Stall reset sequence after PCU PLL lock until de-asserted – 1 = (Default) Normal Operation; No stall. – 0 = Stall.
CFG[4]	*	Enable eDP – 1 = Disabled. – 0 = Enabled.
CFG[7]	*	PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training
CFG[1] CFG[3] CFG[8:19]		Reserved configuration lane.

PCIE pore assign	Config. Signals		
	CFG[6]	CFG[5]	CFG[2]
1 x 16	1	1	1
1 x 16 reverse	1	1	0
2 x 8	1	0	1
2 x 8 * reverse	1	0	0
1 x 8 + 2 x 4	0	0	1
1x8+2x4 reverse	0	0	0

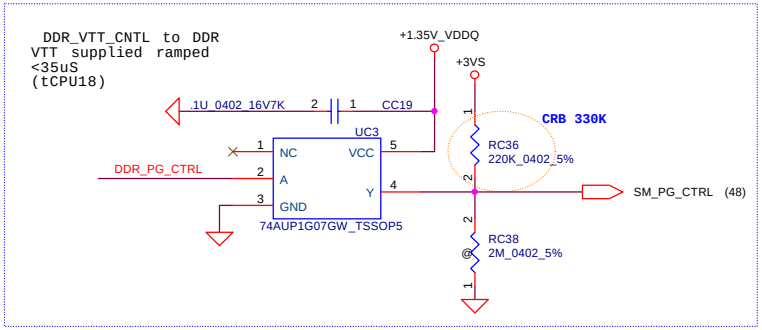


ESD Reserve ,pleace close to cpu. 12/30

SVID ALERT



SVID DATA



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Title: SKL-H(4/9)CLK,GPIO

Size: Custom | Document Number: A4WAD M/B LA-C871P | Rev: 1.0

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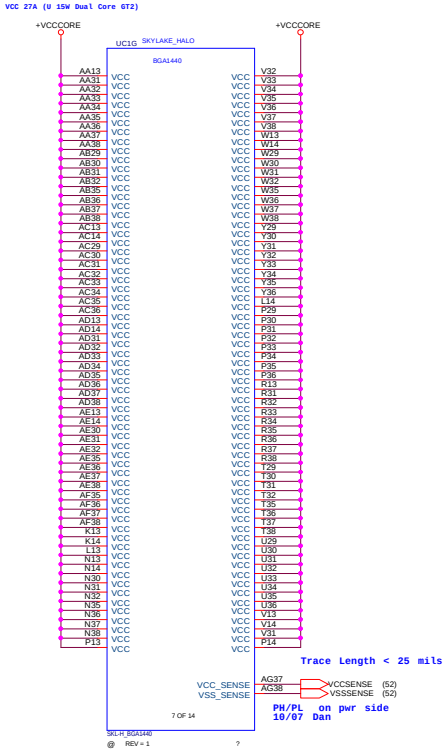
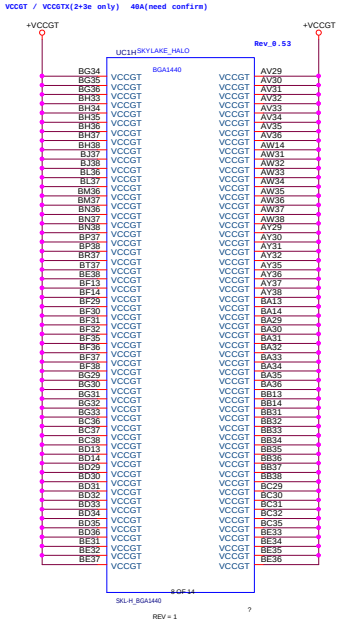
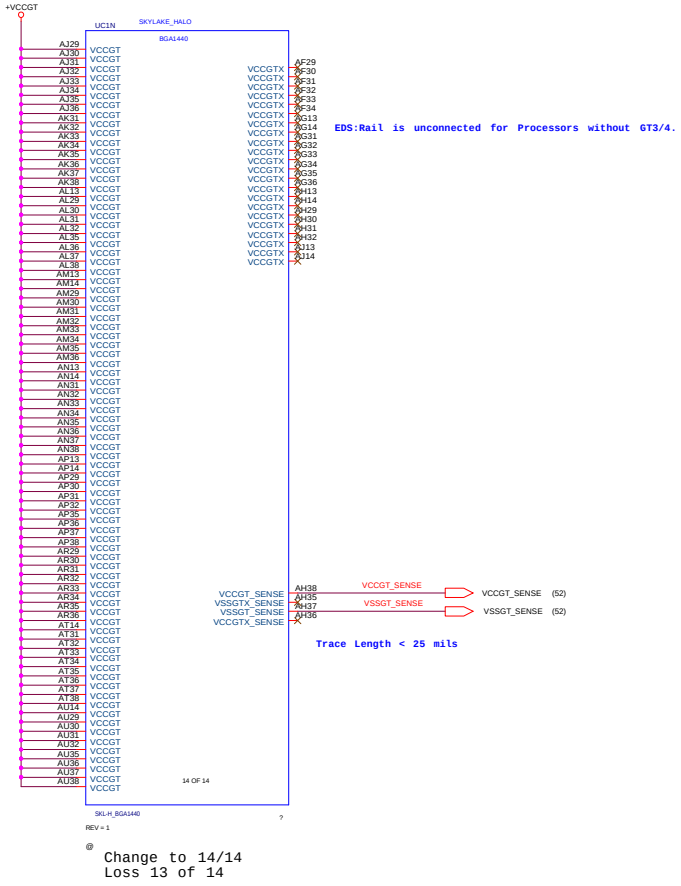
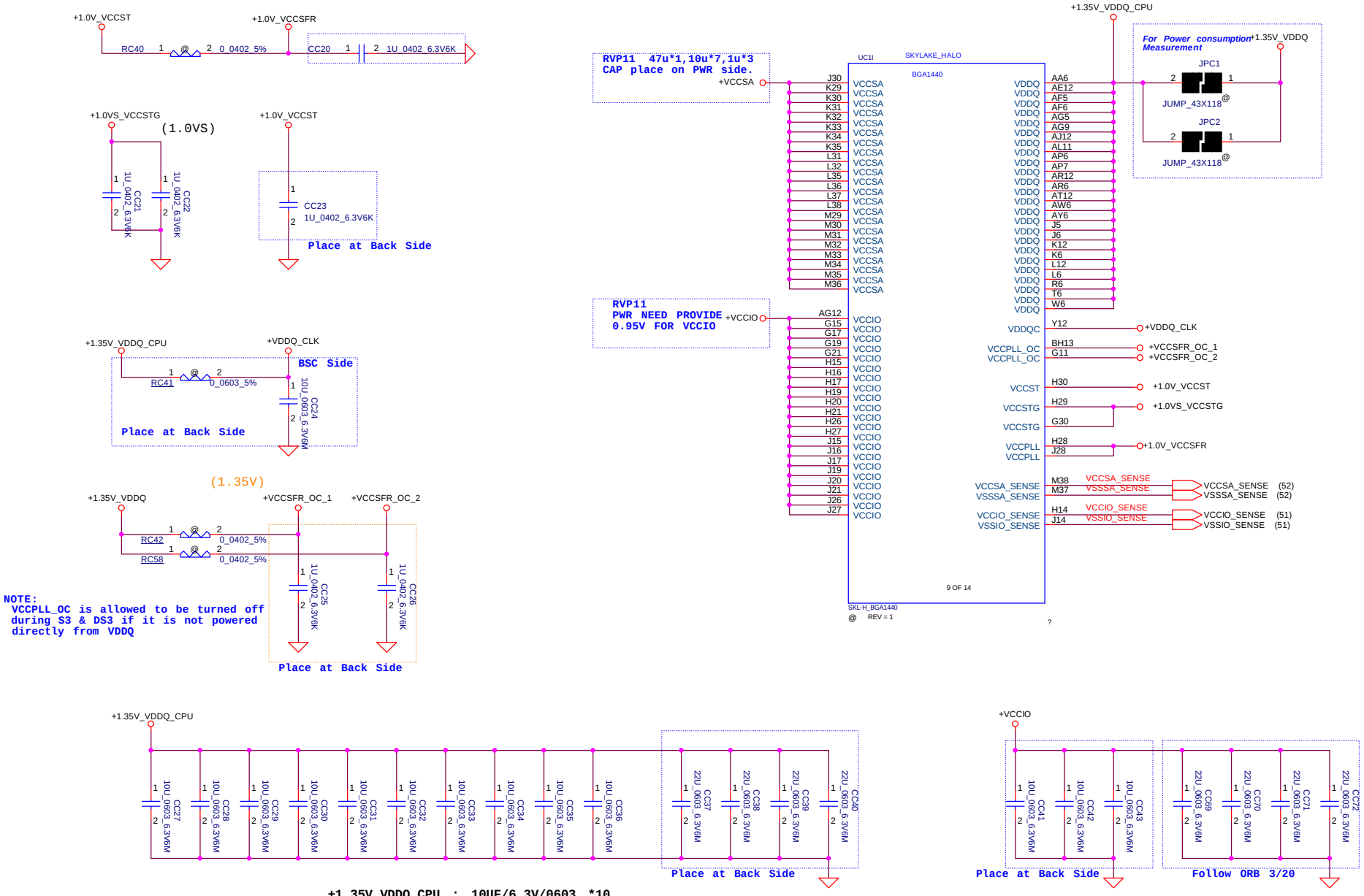






Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title: SKL-H(5/9)Power,SVID			
Size: Custom	Document Number: A4WAD M/B LA-C871P		Rev: 1.0
Date: Monday, July 13, 2015	Sheet 10 of 61		



CPU_CORE/VCCGT/VCCSA decoupling capacitor place to PWR side

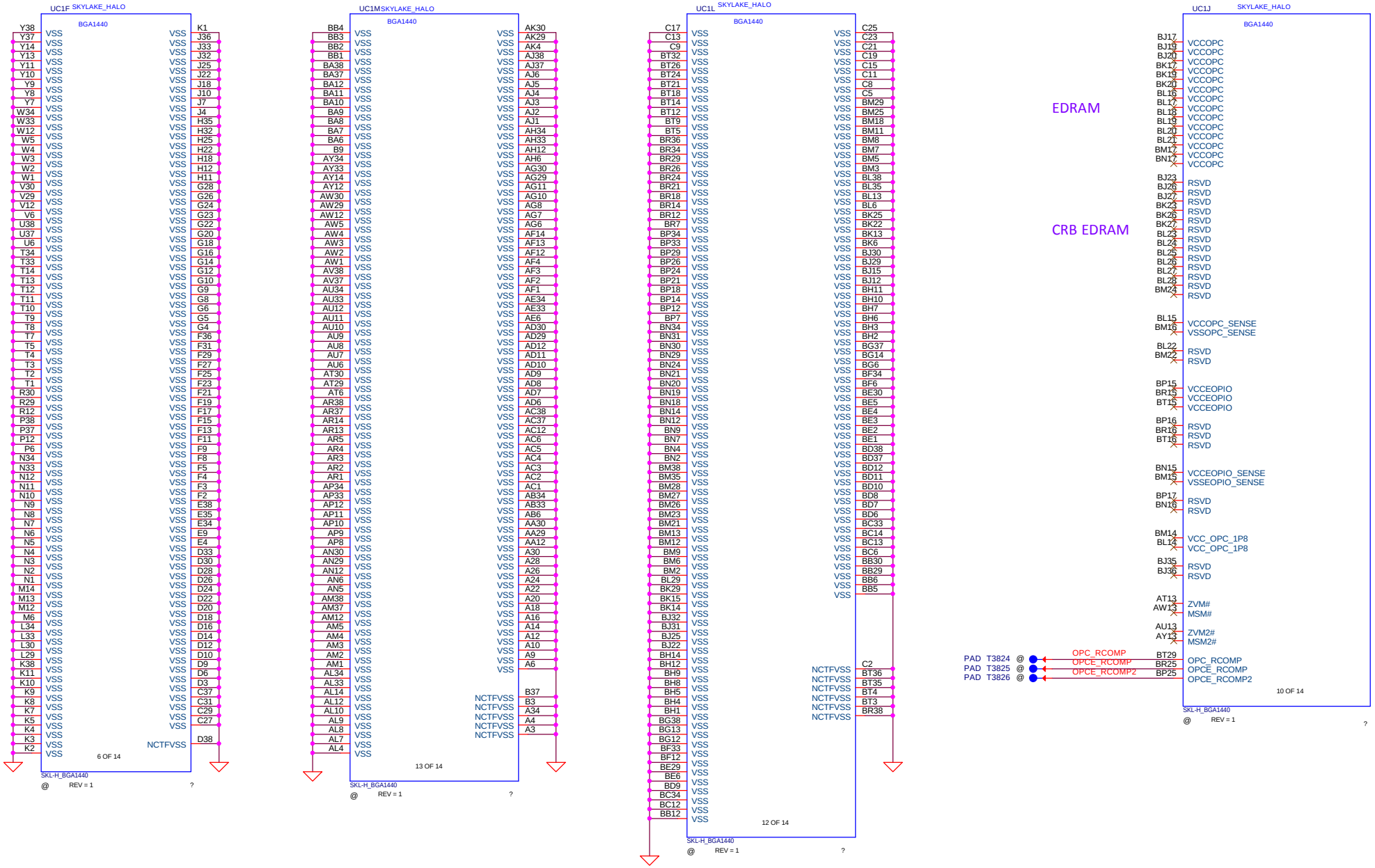
Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: SKL-H(6/9)POWER

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 Sheet 11 of 61



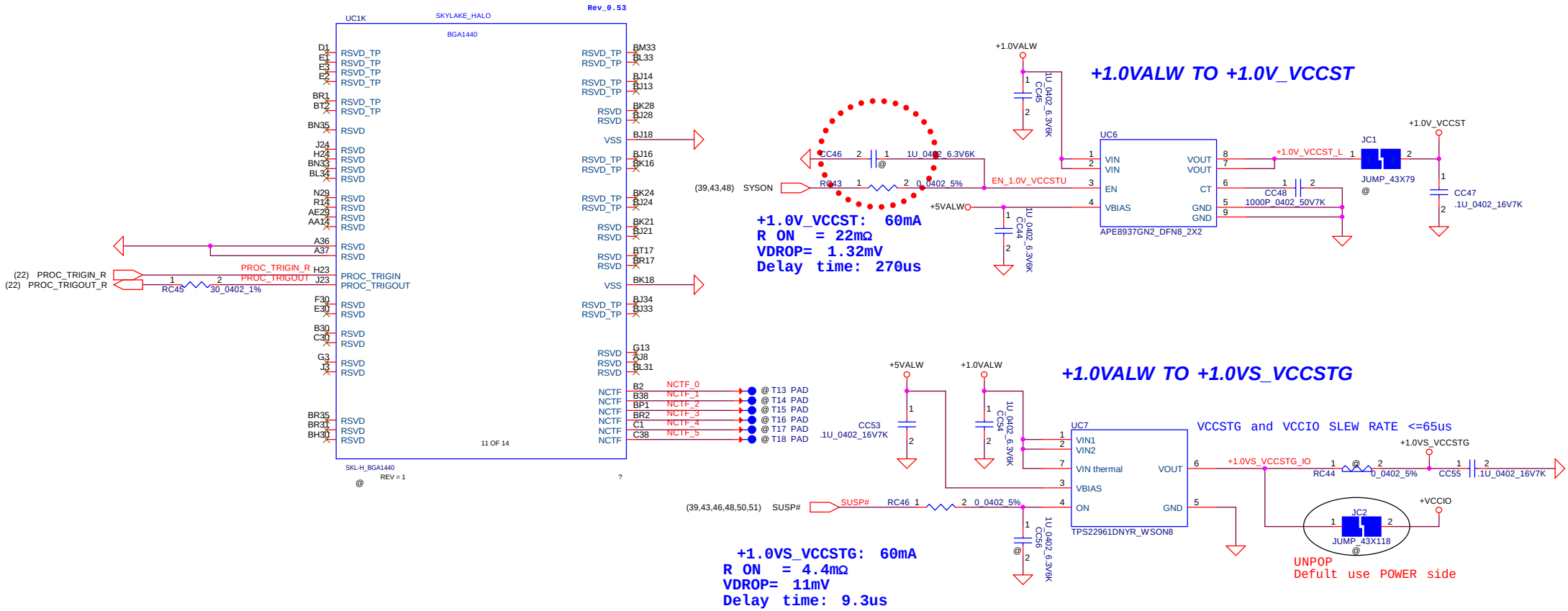
Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: SKL-H(8/9)GND

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 Sheet 12 of 61



Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: SKL-H(9/9)RSVD

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 Sheet 13 of 61

Reverse Type

2-3A to 1 DIMMs/channel

(7) DDR_A_DQS#[0..7]
(7) DDR_A_D[0..63]
(7) DDR_A_DQS[0..7]
(7) DDR_A_MA[0..15]
(7) DDR_A_BS0 — DDR_A_BS0
(7) DDR_A_BS1 — DDR_A_BS1
(7) DDR_A_BS2 — DDR_A_BS2
(7) DDR_A_WE# — DDR_A_WE#
(7) DDR_A_CAS# — DDR_A_CAS#
(7) DDR_A_RAS# — DDR_A_RAS#
(7) DDR_A_CLK0 — DDR_A_CLK0
(7) DDR_A_CLK#0 — DDR_A_CLK#0
(7) DDR_A_CLK1 — DDR_A_CLK1
(7) DDR_A_CLK#1 — DDR_A_CLK#1
(7) DDR_A_CKE0 — DDR_A_CKE0
(7) DDR_A_CKE1 — DDR_A_CKE1
(7) DDR_A_CS#0 — DDR_A_CS#0
(7) DDR_A_CS#1 — DDR_A_CS#1
(15,18,42) PCH_SMBDATA_R — PCH_SMBDATA_R
(15,18,42) PCH_SMBCLK_R — PCH_SMBCLK_R
(7) DDR_A_ODT0 — DDR_A_ODT0
(7) DDR_A_ODT1 — DDR_A_ODT1

+0.675V_A_VREFDQ
+1.35V_VDDQ
+0.675V_DDRA_VREFDQ
RD1 1K_0402_1%
RD2 2_0402_1%
RD3 1K_0402_1%
RD4 24.9_0402_1%
CD3 0.022U_0402_16V7K
CD1 2.2U_0402_6.3V6M
CD2 .1U_0402_16V7K
@

10mils

Place near to SO-DIMM connector.

JDIMM1

1	VREF_DQ		2	VSS1			
3	VSS2	DDR_A_D0	4	DQ4	DDR_A_D1		
5	DQ0	DDR_A_D5	6	DQ5	DDR_A_D4		
7	DQ1		8	VSS3			
9	VSS4		10	DQS#0	DDR_A_DQS#0		
11	DM0		12	DQS0	DDR_A_DQS0		
13	VSS5		14	VSS6			
15	DQ2	DDR_A_D6	16	DQ6	DDR_A_D7		
17	DQ3	DDR_A_D2	18	DQ7	DDR_A_D3		
19	VSS7		20	VSS8			
21	DQ8	DDR_A_D13	22	DQ12	DDR_A_D9		
23	DQ9	DDR_A_D12	24	DQ13	DDR_A_D8		
25	VSS9		26	VSS10			
27	DQS#1	DDR_A_DQS#1	28	DM1			
29	DQS1		30	RESET#	DDR_DRAMRST#		
31	VSS11		32	VSS12			
33	DQ10	DDR_A_D10	34	DQ14	DDR_A_D15		
35	DQ11	DDR_A_D11	36	DQ15	DDR_A_D14		
37	VSS13		38	VSS14			
39	DQ16	DDR_A_D20	40	DQ20	DDR_A_D16		
41	DQ17	DDR_A_D21	42	DQ21	DDR_A_D17		
43	VSS15		44	VSS16			
45	DQS#2	DDR_A_DQS#2	46	DM2			
47	DQS2	DDR_A_DQS2	48	VSS17			
49	VSS18		50	DQ22	DDR_A_D22		
51	DQ18	DDR_A_D18	52	DQ23	DDR_A_D23		
53	DQ19	DDR_A_D19	54	VSS19			
55	VSS20		56	DQ28	DDR_A_D24		
57	DQ24	DDR_A_D29	58	DQ29	DDR_A_D25		
59	DQ25	DDR_A_D28	60	VSS21			
61	VSS22		62	DQS#3	DDR_A_DQS#3		
63	DM3		64	DQS3	DDR_A_DQS3		
65	VSS23		66	VSS24			
67	DQ26	DDR_A_D30	68	DQ30	DDR_A_D26		
69	DQ27	DDR_A_D31	70	DQ31	DDR_A_D27		
71	VSS25		72	VSS26			
73	CKE0	DDR_A_CKE0	74	CKE1	DDR_A_CKE1		
75	VDD1		76	VDD2			
77	NC1		78	A15	DDR_A_MA15		
79	BA2	DDR_A_BS2	80	A14	DDR_A_MA14		
81	VDD3		82	VDD4			
83	A12/BC#	DDR_A_MA12	84	A11	DDR_A_MA11		
85	A9	DDR_A_MA9	86	A7	DDR_A_MA7		
87	VDD5		88	VDD6			
89	A8	DDR_A_MA8	90	A6	DDR_A_MA6		
91	A5	DDR_A_MA5	92	A4	DDR_A_MA4		
93	VDD7		94	VDD8			
95	A3	DDR_A_MA3	96	A2	DDR_A_MA2		
97	A1	DDR_A_MA1	98	A0	DDR_A_MA0		
99	VDD9		100	VDD10			
101	CK0	DDR_A_CLK0	102	CK1	DDR_A_CLK1		
103	CK0#	DDR_A_CLK#0	104	CK1#	DDR_A_CLK#1		
105	VDD11		106	VDD12			
107	A10/AP	DDR_A_MA10	108	BA1	DDR_A_BS1		
109	BA0	DDR_A_BS0	110	RAS#	DDR_A_RAS#		
111	VDD13		112	VDD14			
113	WE#	DDR_A_WE#	114	S0#	DDR_A_CS#0		
115	CAS#	DDR_A_CAS#	116	ODT0	DDR_A_ODT0		
117	VDD15		118	VDD16			
119	A13	DDR_A_MA13	120	ODT1	DDR_A_ODT1		
121	S1#	DDR_A_CS#1	122	NC2			
123	VDD17		124	VDD18			
125	NCTEST		126	VREF_CA			
127	VSS27		128	VSS28			
129	DQ32	DDR_A_D33	130	DQ36	DDR_A_D32		
131	DQ33	DDR_A_D37	132	DQ37	DDR_A_D36		
133	VSS29		134	VSS30			
135	DQS#4	DDR_A_DQS#4	136	DM4			
137	DQS4	DDR_A_DQS4	138	VSS31			
139	VSS32		140	DQ38	DDR_A_D38		
141	DQ34	DDR_A_D35	142	DQ39	DDR_A_D39		
143	DQ35	DDR_A_D34	144	VSS33			
145	VSS34		146	DQ44	DDR_A_D44		
147	DQ40	DDR_A_D40	148	DQ45	DDR_A_D41		
149	DQ41	DDR_A_D45	150	VSS35			
151	VSS36		152	DQS#5	DDR_A_DQS#5		
153	DM5		154	DQS5	DDR_A_DQS5		
155	VSS37		156	VSS38			
157	DQ42	DDR_A_D46	158	DQ46	DDR_A_D42		
159	DQ43	DDR_A_D47	160	DQ47	DDR_A_D43		
161	VSS39		162	VSS40			
163	DQ48	DDR_A_D48	164	DQ52	DDR_A_D52		
165	DQ49	DDR_A_D50	166	DQ53	DDR_A_D49		
167	VSS41		168	VSS42			
169	DQS#6	DDR_A_DQS#6	170	DM6			
171	DQS6		172	VSS43			
173	VSS44		174	DQ54	DDR_A_D55		
175	DQ50	DDR_A_D54	176	DQ55	DDR_A_D53		
177	DQ51	DDR_A_D51	178	VSS45			
179	VSS46		180	DQ60	DDR_A_D60		
181	DQ56	DDR_A_D61	182	DQ61	DDR_A_D57		
183	DQ57	DDR_A_D56	184	VSS47			
185	VSS48		186	DQS#7	DDR_A_DQS#7		
187	DM7		188	DQS7	DDR_A_DQS7		
189	VSS49		190	VSS50			
191	DQ58	DDR_A_D59	192	DQ62	DDR_A_D62		
193	DQ59	DDR_A_D63	194	DQ63	DDR_A_D58		
195	VSS51		196	VSS52			
197	SA0		198	EVENT#			
199	VDDSPD		200	SDA	PCH_SMBDATA_R		
201	SA1		202	SCL	PCH_SMBCLK_R		
203	VTT1		204	VTT2	+0.675VS_VTT		
205	G1		206	G2			

LCN_DAN06-K4406-0101
CONN@ SP07000PT00

+0.675VS_VTT +3VS

Address : 00

+1.35V_VDDQ
RD5 470_0402_5%
From CPU to CHB
DDR_DRAMRST# (15,18)
CD4 .1U_0402_16V7K
@

CAD NOTE
PLACE THE CAP NEAR TO
DIMM RESET PIN

DIMM1 RVS H:4mm
<Address: 00>

+0.675V_DDRA_VREFCA
+0.675V_DDR_VREFCA
10mils
RD6 0_0402_5%
CD20 2.2U_0402_6.3V6M
CD21 .1U_0402_16V7K
@

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

+1.35V_VDDQ
CD5 1U_0402_6.3V6K
CD6 1U_0402_6.3V6K @
CD7 1U_0402_6.3V6K
CD8 1U_0402_6.3V6K @
CD9 1U_0402_6.3V6K @
CD10 1U_0402_6.3V6K

+1.35V_VDDQ
CD11 10U_0603_6.3V6M
CD12 10U_0603_6.3V6M @
CD13 10U_0603_6.3V6M
CD14 10U_0603_6.3V6M
CD15 10U_0603_6.3V6M @
CD16 10U_0603_6.3V6M
CD17 10U_0603_6.3V6M
CD18 10U_0603_6.3V6M @
CD19 330U_D2_2V_Y

Follow Robin_SL
SGA00009S00
330U 2V H1.9
9mohm POLY

Layout Note:
Place near JDIMM1.203,204

+0.675VS_VTT
CD22 1U_0402_6.3V6K
CD23 1U_0402_6.3V6K

Layout Note:
Place near JDIMM1.199

+3VS
CD24 .1U_0402_16V7K

Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

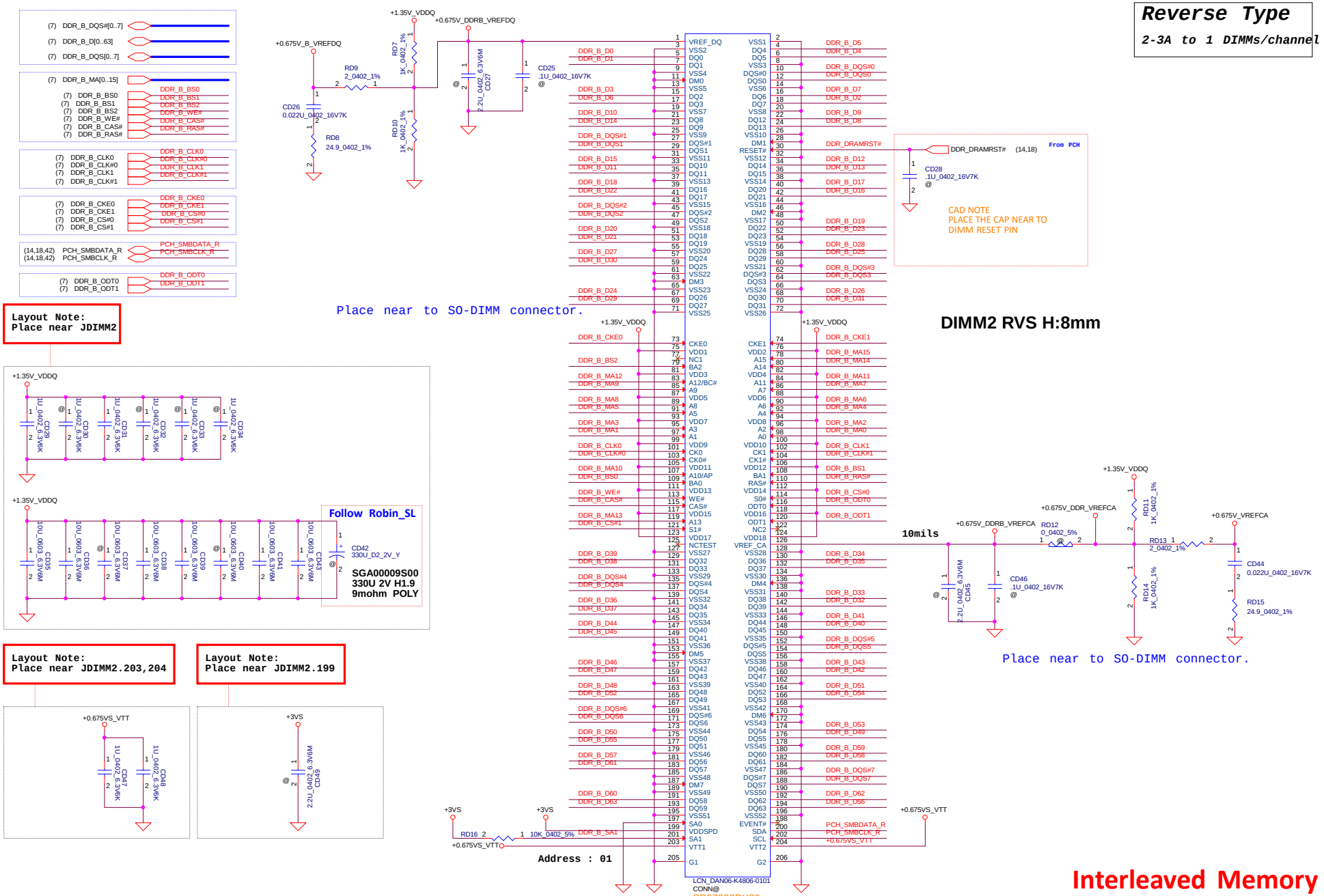
Title: DDR3L DIMMA

Size: Custom | Document Number: A4WAD M/B LA-C871P | Rev: 1.0

Date: Monday, July 13, 2015 | Sheet 14 of 61

Reverse Type

2-3A to 1 DIMMs/channel



Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **DDR3L_DIMMB**

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

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UH1
SKL-PCH_QJHT
PCH_QJHT@
SA000096J10

UH1
SKL-PCH_QHPU
PCH_QHPU@
SA00008RM30

USB3 MB
USB3 MB

(38) USB3_PTX_DRX_N1
(38) USB3_PTX_DRX_P1
(38) USB3_PRX_DTX_N1
(38) USB3_PRX_DTX_P1
(38) USB3_PTX_DRX_N2
(38) USB3_PRX_DTX_P2
(38) USB3_PRX_DTX_N2
(38) USB3_PRX_DTX_P2

CHECK ACER DVR for port use

UH1F
SPT-H_PCH
USB3_1_TXN C11
USB3_1_TXP B11
USB3_1_RXN B7
USB3_1_RXP A7
USB3_2_TXN/SSIC_1_TXN B12
USB3_2_TXP/SSIC_1_TXP A12
USB3_2_RXN/SSIC_1_RXN C8
USB3_2_RXP/SSIC_1_RXP B8
USB3_6_TXN B15
USB3_6_TXP C15
USB3_6_RXN K15
USB3_6_RXP K14
USB3_5_TXN B14
USB3_5_TXP C14
USB3_5_RXN G13
USB3_5_RXP H13
USB3_3_TXP/SSIC_2_TXP D13
USB3_3_TXN/SSIC_2_TXN C13
USB3_3_RXP/SSIC_2_RXP A9
USB3_3_RXN/SSIC_2_RXN B10
USB3_4_TXP B13
USB3_4_TXN A14
USB3_4_RXP G11
USB3_4_RXN E11
6 OF 12
GPP_A1/LAD0/ESPI_IO0 AT22
GPP_A2/LAD1/ESPI_IO1 AV22
GPP_A3/LAD2/ESPI_IO2 AT19
GPP_A4/LAD3/ESPI_IO3 BD16
GPP_A5/LFRAME#/ESPI_CS0# BE16
GPP_A6/SERIRQ/ESPI_CS1# BA17
GPP_A7/PIRQA#/ESPI_ALERT0# AW17
GPP_A0/RCIN#/ESPI_ALERT1# AT17
GPP_A14/SUS_STAT#/ESPI_RESET# BC18
GPP_A9/CLKOUT_LPC0/ESPI_CLK BC17
GPP_A10/CLKOUT_LPC1 AV19
GPP_G19/SMI# M45
GPP_G18/NMI# M43
GPP_E6/DEVSLP2 AE45
GPP_E5/DEVSLP1 AG43
GPP_E4/DEVSLP0 AG42
GPP_F9/DEVSLP7 AB39
GPP_F8/DEVSLP6 AB36
GPP_F7/DEVSLP5 AB43
GPP_F6/DEVSLP4 AB42
GPP_F5/DEVSLP3 AB41
SKL-H-PCH_BGA837
@ REV = 1.3

LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_AD0 (39,40)
LPC_AD1 (39,40)
LPC_AD2 (39,40)
LPC_AD3 (39,40)
LPC Bus
LPC : +3.3V
LPC_FRAME#
TPM_SERIRQ
LPC_PIRQA#
EC_KBRST#_R
LPC_FRAME# (39,40)
TPM_SERIRQ (39,40)
To TPM
EC_KBRST#_R (39)
ESPI_RST# (39)
LPC_CLK
CK_LPC_TPM_R
RH2 2 1 22_0402_5%
RH4 2 1 22_0402_5%
TPM@
LPC_CLK_R (39)
CK_LPC_TPM (40)
To EC

+3VS
TPM_SERIRQ
RH1 1 2 10K_0402_5%
DG requierment 8.2k PH +3VS
CRB 10K PH +3vs
EC_KBRST#_R
RH3 1 @ 2 10K_0402_5%
check EC design needed
pop RC118 or not

+3VALW_PCH_PRIM
LPC_PIRQA#
RH122 2 1 10K_0402_5%

(8) DMI_CTX_PRX_N0
(8) DMI_CTX_PRX_P0
(8) DMI_CRX_PTX_N0
(8) DMI_CRX_PTX_P0
(8) DMI_CTX_PRX_N1
(8) DMI_CTX_PRX_P1
(8) DMI_CRX_PTX_N1
(8) DMI_CRX_PTX_P1
(8) DMI_CTX_PRX_N2
(8) DMI_CTX_PRX_P2
(8) DMI_CRX_PTX_N2
(8) DMI_CRX_PTX_P2
(8) DMI_CTX_PRX_N3
(8) DMI_CTX_PRX_P3
(8) DMI_CRX_PTX_N3
(8) DMI_CRX_PTX_P3

RH5 1 2 100_0402_1%

#546884 P.231 PCIE_RCOMPN/PCIE_RCOMPP
BO=4 W=12~15 S=12 R=100ohm

UH1B
SPT-H_PCH
DMI_CTX_PRX_N0 L27
DMI_CTX_PRX_P0 N27
DMI_CRX_PTX_N0 C27
DMI_CRX_PTX_P0 B27
DMI_CTX_PRX_N1 E24
DMI_CTX_PRX_P1 G24
DMI_CRX_PTX_N1 B28
DMI_CRX_PTX_P1 A28
DMI_CTX_PRX_N2 G27
DMI_CTX_PRX_P2 E26
DMI_CRX_PTX_N2 B29
DMI_CRX_PTX_P2 C29
DMI_CTX_PRX_N3 L29
DMI_CTX_PRX_P3 K29
DMI_CRX_PTX_N3 B30
DMI_CRX_PTX_P3 A30
PCIE_RCOMPN B18
PCIE_RCOMPP C17
DMI_RXN0
DMI_RXP0
DMI_TXN0
DMI_TXP0
DMI_RXN1
DMI_RXP1
DMI_TXN1
DMI_TXP1
DMI_RXN2
DMI_RXP2
DMI_TXN2
DMI_TXP2
DMI_RXN3
DMI_RXP3
DMI_TXN3
DMI_TXP3
PCIE_RCOMPN
PCIE_RCOMPP
DMI
USB 2.0
PCIE/USB 3
USB2N_1 AF5
USB2P_1 AG7
USB2N_2 AD5
USB2P_2 AD7
USB2N_3 AG8
USB2P_3 AG10
USB2N_4 AE1
USB2P_4 AE2
USB2N_5 AC2
USB2P_5 AC3
USB2N_6 AF2
USB2P_6 AF3
USB2N_7 AB3
USB2P_7 AB2
USB2N_8 AL8
USB2P_8 AL7
USB2N_9 AA1
USB2P_9 AA2
USB2N_10 AJ8
USB2P_10 AJ7
USB2N_11 W2
USB2P_11 W3
USB2N_12 AD3
USB2P_12 AD2
USB2N_13 V2
USB2P_13 V1
USB2N_14 AJ11
USB2P_14 AJ13
USB20_N1
USB20_P1
USB20_N2
USB20_P2
USB20_N3
USB20_P3
USB20_N7
USB20_P7
USB20_N8
USB20_P8
USB20_N9
USB20_P9
USB20_N1 (38)
USB20_P1 (38)
USB20_N2 (38)
USB20_P2 (38)
USB20_N3 (38)
USB20_P3 (38)
USB20_N7 (36)
USB20_P7 (36)
USB20_N8 (30)
USB20_P8 (30)
USB20_N9 (30)
USB20_P9 (30)
USB3 MB
USB3 MB
USB2/B
BT
TS
Camera
CHECK ACER DVR for port use
12/08 Change Port, follow DVR1044_R1.03
PCIE1_RXN/USB3_7_RXN H15
PCIE1_RXP/USB3_7_RXP G15
PCIE1_TXN/USB3_7_TXN A16
PCIE1_TXP/USB3_7_TXP B16
PCIE2_TXN/USB3_8_TXN B19
PCIE2_TXP/USB3_8_TXP C19
PCIE2_RXN/USB3_8_RXN E17
PCIE2_RXP/USB3_8_RXP G17
PCIE3_RXN/USB3_9_RXN L17
PCIE3_RXP/USB3_9_RXP K17
PCIE3_TXN/USB3_9_TXN B20
PCIE3_TXP/USB3_9_TXP C20
PCIE4_RXN/USB3_10_RXN E20
PCIE4_RXP/USB3_10_RXP G19
PCIE4_TXN/USB3_10_TXN B21
PCIE4_TXP/USB3_10_TXP A21
PCIE5_RXN K19
PCIE5_RXP L19
PCIE5_TXN D22
PCIE5_TXP C22
PCIE6_RXN G22
PCIE6_RXP E22
PCIE6_TXN B22
PCIE6_TXP A22
PCIE7_RXN K22
PCIE7_RXP L22
PCIE7_TXN C23
PCIE7_TXP B23
PCIE8_RXN K24
PCIE8_RXP L24
PCIE8_TXN C24
PCIE8_TXP B24
2 OF 12
GPP_E9/USB2_OC0# AD43
GPP_E10/USB2_OC1# AD42
GPP_E11/USB2_OC2# AD39
GPP_E12/USB2_OC3# AC44
GPP_F15/USB2_OCB_4 Y43
GPP_F16/USB2_OCB_5 Y41
GPP_F17/USB2_OCB_6 W44
GPP_F18/USB2_OCB_7 W43
USB2_COMP AG3
USB2_VBUSSENSE AD10
RSVD_AB13 AB13
USB2_ID AG2
GPD7/RSVD BD14
USB_OC0#
USB_OC1#
USB_OC2#
USB_OC3#
USB_OC4
USB_OC5
USB_OC6
USB_OC7
USB_OC0# (38)
USB_OC1# (38)
USB2_COMP
USB2_VBUSSENSE
USB2_ID
RH6 1 2 113_0402_1%
RH149 1 2 0_0402_5%
RH150 1 2 0_0402_5%
SKL-H-PCH_BGA837
@ REV = 1.3

546765_2015WW10_Skylake_MOW_Rev_1_0
05/19 RH150

reference PDG1.0 50-30
+3VALW_PCH_PRIM
RPH1
USB_OC0# 8 1
USB_OC1# 7 2
USB_OC3# 6 3
USB_OC2# 5 4
10K_0804_8P4R_5%
RPH2
USB_OC5 8 1
USB_OC4 7 2
USB_OC6 6 3
USB_OC7 5 4
10K_0804_8P4R_5%
@

NGFF WL+BT(KEY E)
GLAN+CR

(36) PCIE_PRX_DTX_N3
(36) PCIE_PRX_DTX_P3
(36) PCIE_PTX_C_DRX_N3
(36) PCIE_PTX_C_DRX_P3
(34) PCIE_PRX_DTX_N4
(34) PCIE_PRX_DTX_P4
(34) PCIE_PTX_C_DRX_N4
(34) PCIE_PTX_C_DRX_P4

CH3 2 1 .1U_0402_16V7K
CH4 2 1 .1U_0402_16V7K
CH1 2 1 .1U_0402_16V7K
CH2 2 1 .1U_0402_16V7K

PCIE_PRX_DTX_N3
PCIE_PRX_DTX_P3
PCIE_PTX_DRX_N3
PCIE_PTX_DRX_P3
PCIE_PRX_DTX_N4
PCIE_PRX_DTX_P4
PCIE_PTX_DRX_N4
PCIE_PTX_DRX_P4

CHECK ACER DVR for port use
12/08 Change Port, follow DVR1044_R1.03

3.4 Intel SKYLAKE two chip.

SKL		Acer 2015	Robin_SLS (A4WAD)
Lane1	USB3 Port1	USB3 (I/O)	USB3(Left up)
Lane2	USB3 Port2 / SSIC Port1	USB3 (I/O)	USB3(Left down)
Lane3	USB3 Port3 / SSIC Port2	USB3 (I/O)	
Lane4	USB3 Port4	USB3 (I/O)	
Lane5	USB3 Port5	3D Camera	
Lane6	USB3 Port6		
Lane7	USB3 Port7 / PCIe Port1		
Lane8	USB3 Port8 / PCIe Port2	WIFI	WLAN (M.2)
Lane9	PCIe Port3	LAN	LAN + CR
Lane10	PCIe Port4		
Lane11	PCIe Port5	Alpine-Ridge (PCIex4)	
Lane12	PCIe Port6		
Lane13	PCIe Port7	M.2 SSD (SATA)	
Lane14	PCIe Port8		
Lane15	SATA3 Port0	M.2 SSD (PCIE x4)	
Lane16	SATA3 Port1 / PCIe Port10		
Lane17	PCIe Port11		
Lane18	PCIe Port12		
Lane19	PCIe Port13		
Lane20	PCIe Port14		
Lane21	SATA3 Port2 / PCIe Port15	HDD	HDD
Lane22	SATA3 Port3 / PCIe Port16	ODD	ODD
Lane23			
Lane24		N/A	
Lane25			
Lane26			
USB20	USB2 Port1	USB3 (I/O)	USB3(Left up)
USB20	USB2 Port2	USB3 (I/O)	USB3(Left down)
USB20	USB2 Port3	USB3 (I/O)	USB2(Right)
USB20	USB2 Port4	USB3 (I/O)	
USB20	USB2 Port5	USB2 (I/O)/Sensor Hub	
USB20	USB2 Port6	USB2 (I/O)/Sensor Hub	
USB20	USB2 Port7	BT	BT (M.2)
USB20	USB2 Port8	TS	TS
USB20	USB2 Port9	CCD	Camera
USB20	USB2 Port10	CR(USB)/FP	
USB20	USB2 Port11		
USB20	USB2 Port12		
USB20	USB2 Port13		
USB20	USB2 Port14	N/A	

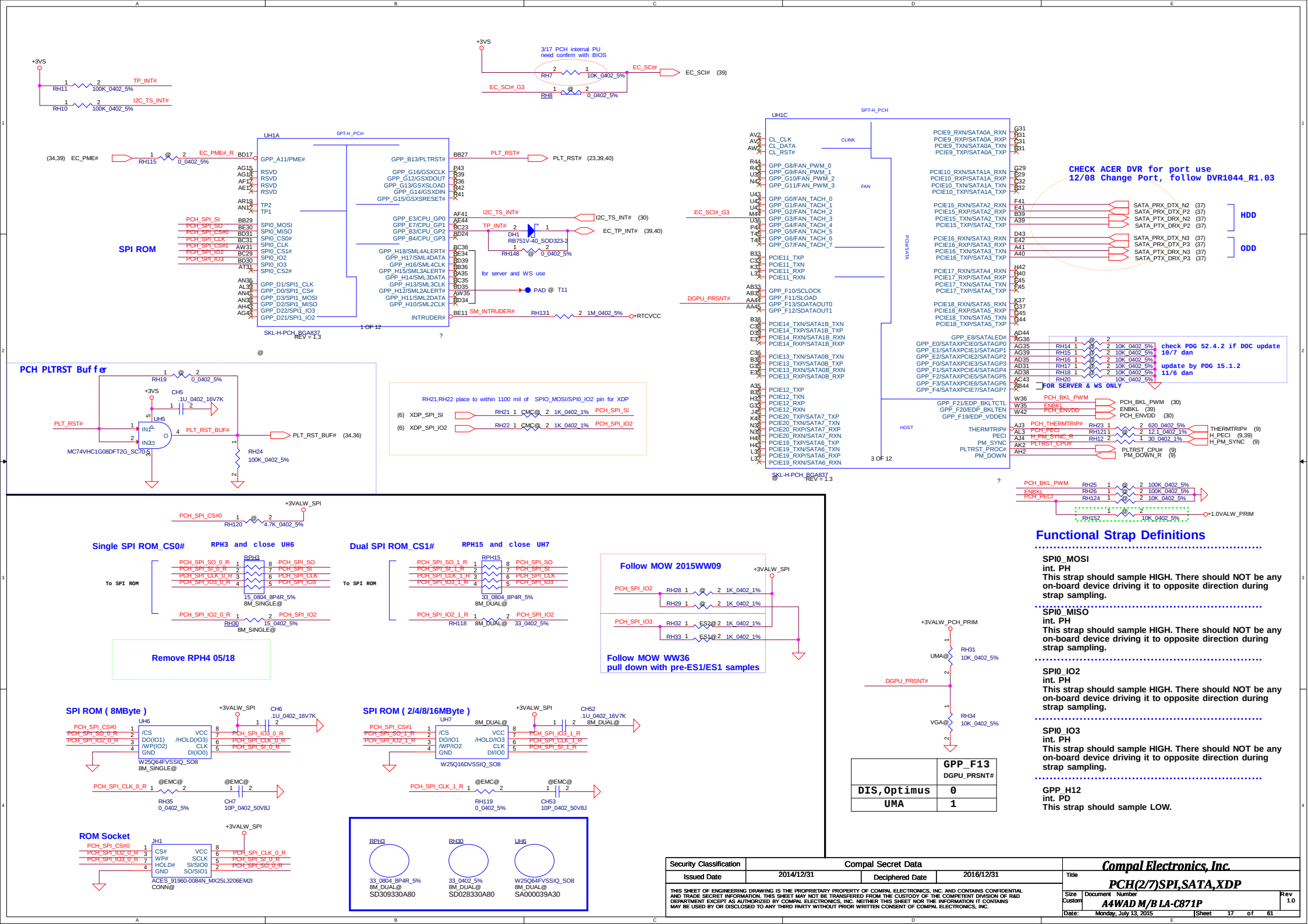
Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: PCH(1/7)DMI,PCIE,USB

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 Sheet 16 of 61


+3VS
TP_INT#
RH11 100K_0402_5%
I2C_TS_INT#
RH10 100K_0402_5%
3/17 PCH internal PU need confirm with BIOS
EC_SCI#
EC_SCI# (39)
RH7 10K_0402_5%
EC_SCI#_G3
RH8 0_0402_5%
UH1A
SPT-H_PCH
(34,39) EC_PME#
EC_PME#_R
RH115 0_0402_5%
GPP_A11/PME#
RSVD
TP1
SPI ROM
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CLK
SPI0_CS1#
SPI0_IO2
SPI0_IO3
SPI0_CS2#
GPP_D1/SPI1_CLK
GPP_D0/SPI1_CS#
GPP_D3/SPI1_MOSI
GPP_D2/SPI1_MISO
GPP_D22/SPI1_IO3
GPP_D21/SPI1_IO2
GPP_B13/PLTRST#
PLT_RST# (23,39,40)
GPP_G16/GSXCLK
GPP_G12/GSXDOUT
GPP_G13/GSXSLOAD
GPP_G14/GSXDIN
GPP_G15/GSXSRESET#
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
I2C_TS_INT# (30)
TP_INT#
EC_TP_INT# (39,40)
DH1 RB751V-40_SOD323-2
RH148 0_0402_5%
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML2ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
for server and WS use
PAD @ T11
INTRUDER#
SM_INTRUDER#
RH131 1M_0402_5%
+RTCVCC
1 OF 12
SKL-H-PCH_BGA837
REV = 1.3
UH1C
CL_CLK
CL_DATA
CL_RST#
CLINK
GPP_G8/FAN_PWM_0
GPP_G9/FAN_PWM_1
GPP_G10/FAN_PWM_2
GPP_G11/FAN_PWM_3
FAN
GPP_G0/FAN_TACH_0
GPP_G1/FAN_TACH_1
GPP_G2/FAN_TACH_2
GPP_G3/FAN_TACH_3
GPP_G4/FAN_TACH_4
GPP_G5/FAN_TACH_5
GPP_G6/FAN_TACH_6
GPP_G7/FAN_TACH_7
PCIE11_TXP
PCIE11_TXN
PCIE11_RXP
PCIE11_RXN
PCIE/SATA
GPP_F10/SCLOCK
GPP_F11/SLOAD
GPP_F13/SDATAOUT0
GPP_F12/SDATAOUT1
DGPU_PRSNT#
PCIE14_TXN/SATA1B_TXN
PCIE14_TXP/SATA1B_TXP
PCIE14_RXN/SATA1B_RXN
PCIE14_RXP/SATA1B_RXP
PCIE13_TXN/SATA0B_TXN
PCIE13_TXP/SATA0B_TXP
PCIE13_RXN/SATA0B_RXN
PCIE13_RXP/SATA0B_RXP
PCIE12_TXP
PCIE12_TXN
PCIE12_RXP
PCIE12_RXN
PCIE20_TXP/SATA7_TXP
PCIE20_TXN/SATA7_TXN
PCIE20_RXP/SATA7_RXP
PCIE20_RXN/SATA7_RXN
PCIE19_TXP/SATA6_TXP
PCIE19_TXN/SATA6_TXN
PCIE19_RXP/SATA6_RXP
PCIE19_RXN/SATA6_RXN
3 OF 12
SKL-H-PCH_BGA837
REV = 1.3
PCIE9_RXN/SATA0A_RXN
PCIE9_RXP/SATA0A_RXP
PCIE9_TXN/SATA0A_TXN
PCIE9_TXP/SATA0A_TXP
PCIE10_RXN/SATA1A_RXN
PCIE10_RXP/SATA1A_RXP
PCIE10_TXN/SATA1A_TXN
PCIE10_TXP/SATA1A_TXP
PCIE15_RXN/SATA2_RXN
PCIE15_RXP/SATA2_RXP
PCIE15_TXN/SATA2_TXN
PCIE15_TXP/SATA2_TXP
PCIE16_RXN/SATA3_RXN
PCIE16_RXP/SATA3_RXP
PCIE16_TXN/SATA3_TXN
PCIE16_TXP/SATA3_TXP
PCIE17_RXN/SATA4_RXN
PCIE17_RXP/SATA4_RXP
PCIE17_TXN/SATA4_TXN
PCIE17_TXP/SATA4_TXP
PCIE18_RXN/SATA5_RXN
PCIE18_RXP/SATA5_RXP
PCIE18_TXN/SATA5_TXN
PCIE18_TXP/SATA5_TXP
GPP_E8/SATALED#
GPP_E0/SATAXPCIE0/SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2
GPP_F0/SATAXPCIE3/SATAGP3
GPP_F1/SATAXPCIE4/SATAGP4
GPP_F2/SATAXPCIE5/SATAGP5
GPP_F3/SATAXPCIE6/SATAGP6
GPP_F4/SATAXPCIE7/SATAGP7
CHECK ACER DVR for port use
12/08 Change Port, follow DVR1044_R1.03
HDD
SATA_PRX_DTX_N2 (37)
SATA_PRX_DTX_P2 (37)
SATA_PTX_DRX_N2 (37)
SATA_PTX_DRX_P2 (37)
ODD
SATA_PRX_DTX_N3 (37)
SATA_PRX_DTX_P3 (37)
SATA_PTX_DRX_N3 (37)
SATA_PTX_DRX_P3 (37)
check PDG 52.4.2 if DOC update 10/7 dan
update by PDG 15.1.2 11/6 dan
FOR SERVER & WS ONLY
GPP_F21/EDP_BKLTCTL
GPP_F20/EDP_BKLTEN
GPP_F19/EDP_VDDEN
PCH_BKL_PWM (30)
ENBKL (39)
PCH_ENVDD (30)
HOST
THERMTRIP#
PECI
PM_SYNC
PLTRST_PROC#
PM_DOWN
PCH_THERMTRIP#
PCH_PECI
H_PM_SYNC_R
PLTRST1_CPU#
THERMTRIP# (9)
H_PECI (9,39)
H_PM_SYNC (9)
PLTRST_CPU# (9)
PM_DOWN_R (9)
PCH PLTRST Buffer
RH19 0_0402_5%
+3VS
CH5 .1U_0402_16V7K
PLT_RST#
UH5
MC74VHC1G08DFT2G_SC70-5
PLT_RST_BUF#
PLT_RST_BUF# (34,36)
RH24 100K_0402_5%
RH21,RH22 place to within 1100 mil of SPIO_MOSI/SPI0_IO2 pin for XDP
(6) XDP_SPI_SI
RH21 1 CMC@ 2 1K_0402_1%
PCH_SPI_SI
(6) XDP_SPI_IO2
RH22 1 CMC@ 2 1K_0402_1%
PCH_SPI_IO2
PCH_BKL_PWM
ENBKL
PCH_PECI
RH25 100K_0402_5%
RH26 100K_0402_5%
RH124 10K_0402_5%
RH152 10K_0402_5%
+1.0VALW_PRIM
PCH_SPI_CS#0
RH120 4.7K_0402_5%
+3VALW_SPI
Single SPI ROM_CS0#
RPH3 and close UH6
To SPI ROM
PCH_SPI_SO_0_R
PCH_SPI_SI_0_R
PCH_SPI_CLK_0_R
PCH_SPI_IO3_0_R
PCH_SPI_SO
PCH_SPI_SI
PCH_SPI_CLK
PCH_SPI_IO3
15_0804_8P4R_5%
8M_SINGLE@
PCH_SPI_IO2_0_R
RH30 15_0402_5%
8M_SINGLE@
PCH_SPI_IO2
Dual SPI ROM_CS1#
RPH15 and close UH7
PCH_SPI_SO_1_R
PCH_SPI_SI_1_R
PCH_SPI_CLK_1_R
PCH_SPI_IO3_1_R
33_0804_8P4R_5%
8M_DUAL@
PCH_SPI_IO2_1_R
RH118 8M_DUAL@ 33_0402_5%
Follow MOW 2015WW09
PCH_SPI_IO2
RH28 1 @ 2 1K_0402_1%
RH29 1 @ 2 1K_0402_1%
PCH_SPI_IO3
RH32 1 ES2@ 2 1K_0402_1%
RH33 1 ES1@ 2 1K_0402_1%
Follow MOW WW36
pull down with pre-ES1/ES1 samples
Remove RPH4 05/18
SPI ROM (8MByte)
UH6
/CS
DO(IO1)
/WP(IO2)
GND
VCC
/HOLD(IO3)
CLK
DI(IO0)
W25Q64FVSSIQ_SO8
8M_SINGLE@
CH6 .1U_0402_16V7K
PCH_SPI_CLK_0_R
@EMC@
RH35 0_0402_5%
CH7 10P_0402_50V8J
SPI ROM (2/4/8/16MByte)
UH7
8M_DUAL@
W25Q16DVSSIQ_SO8
CH52 .1U_0402_16V7K
PCH_SPI_CLK_1_R
RH119 0_0402_5%
CH53 10P_0402_50V8J
ROM Socket
JH1
CS#
WP#
HOLD#
GND
SI/SIO0
SO/SIO1
SCLK
ACES_91960-0084N_MX25L3206EM2I
CONN@
RPH3
33_0804_8P4R_5%
8M_DUAL@
SD309330A80
RH30
33_0402_5%
8M_DUAL@
SD028330A80
UH6
W25Q64FVSSIQ_SO8
8M_DUAL@
SA000039A30
+3VALW_PCH_PRIM
UMA@
RH31 10K_0402_5%
DGPU_PRSNT#
VGA@
RH34 10K_0402_5%
GPP_F13
DGPU_PRSNT#
DIS,Optimus 0
UMA 1
Functional Strap Definitions
SPI0_MOSI
int. PH
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO
int. PH
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2
int. PH
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3
int. PH
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_H12
int. PD
This strap should sample LOW.
Security Classification
Compal Secret Data
Issued Date
2014/12/31
Deciphered Date
2016/12/31
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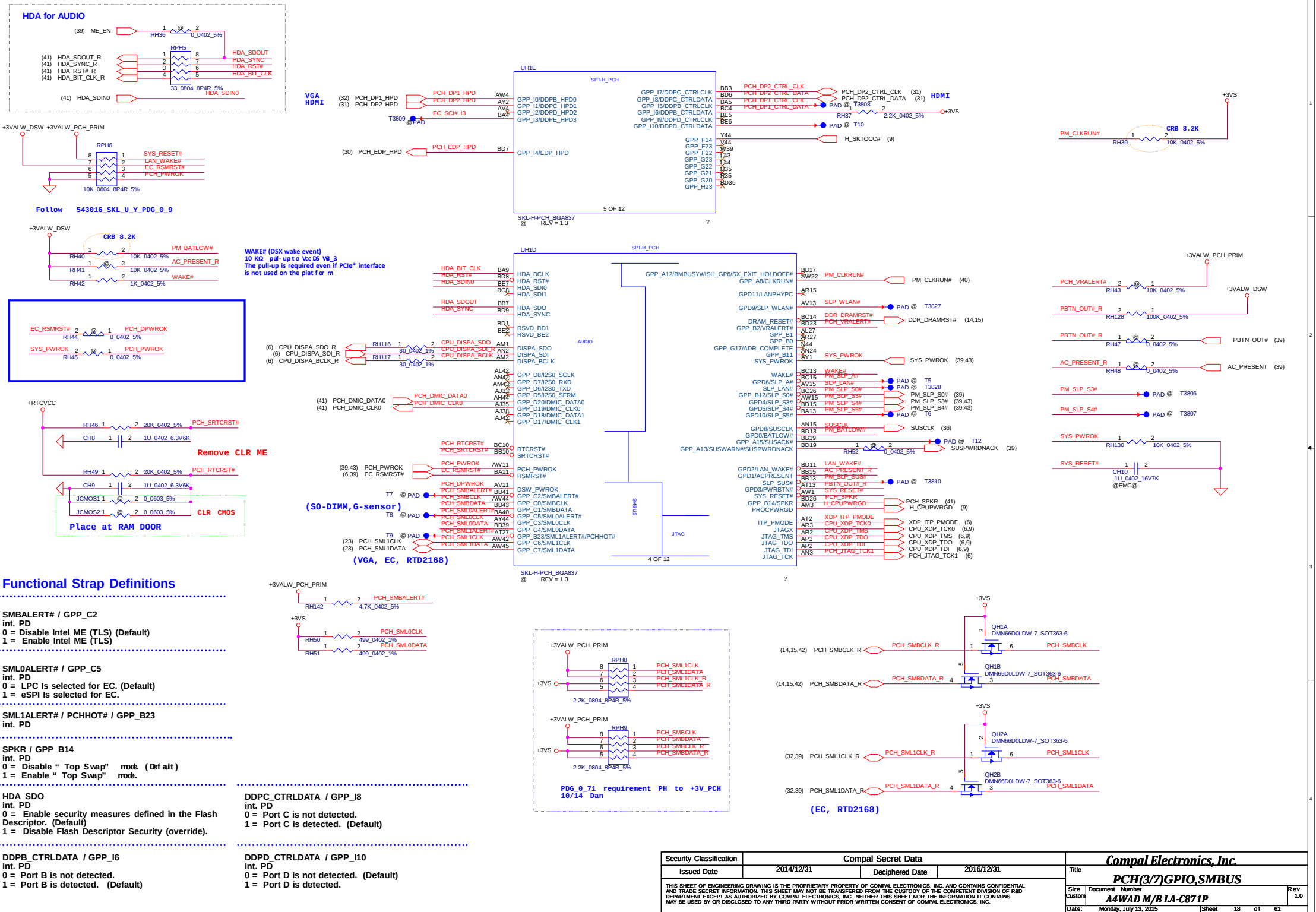
Compal Electronics, Inc.
Title
PCH(2/7)SPI,SATA,XDP
Size Custom
Document Number
A4WAD M/B LA-C871P
Rev 1.0
Date: Monday, July 13, 2015
Sheet 17 of 61



Functional Strap Definitions

SMBALERT# / GPP_C2
int. PD
0 = Disable Intel ME (TLS) (Default)
1 = Enable Intel ME (TLS)

SML0ALERT# / GPP_C5
int. PD
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.

SML1ALERT# / PCHHOT# / GPP_B23
int. PD

SPKR / GPP_B14
int. PD
0 = Disable “ Top Swap” mode. (Default)
1 = Enable “ Top Swap” mode.

HDA_SDO
int. PD
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override).

DDPB_CTRLDATA / GPP_I6
int. PD
0 = Port B is not detected.
1 = Port B is detected. (Default)

DDPC_CTRLDATA / GPP_I8
int. PD
0 = Port C is not detected.
1 = Port C is detected. (Default)

DDPD_CTRLDATA / GPP_I10
int. PD
0 = Port D is not detected. (Default)
1 = Port D is detected.

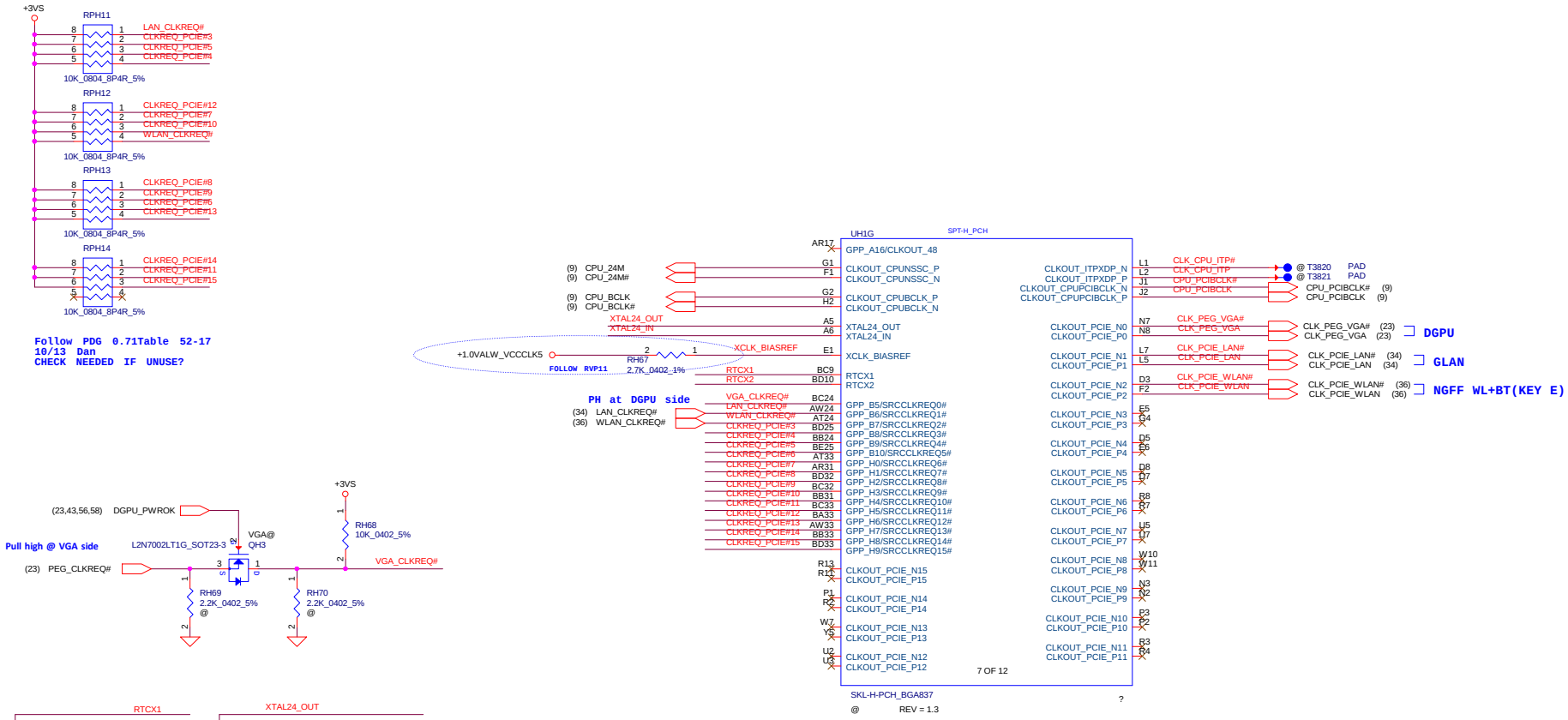
Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: PCH(3/7)GPIO,SMBUS

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 Sheet 18 of 61



Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: PCH(4/7)CLK

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

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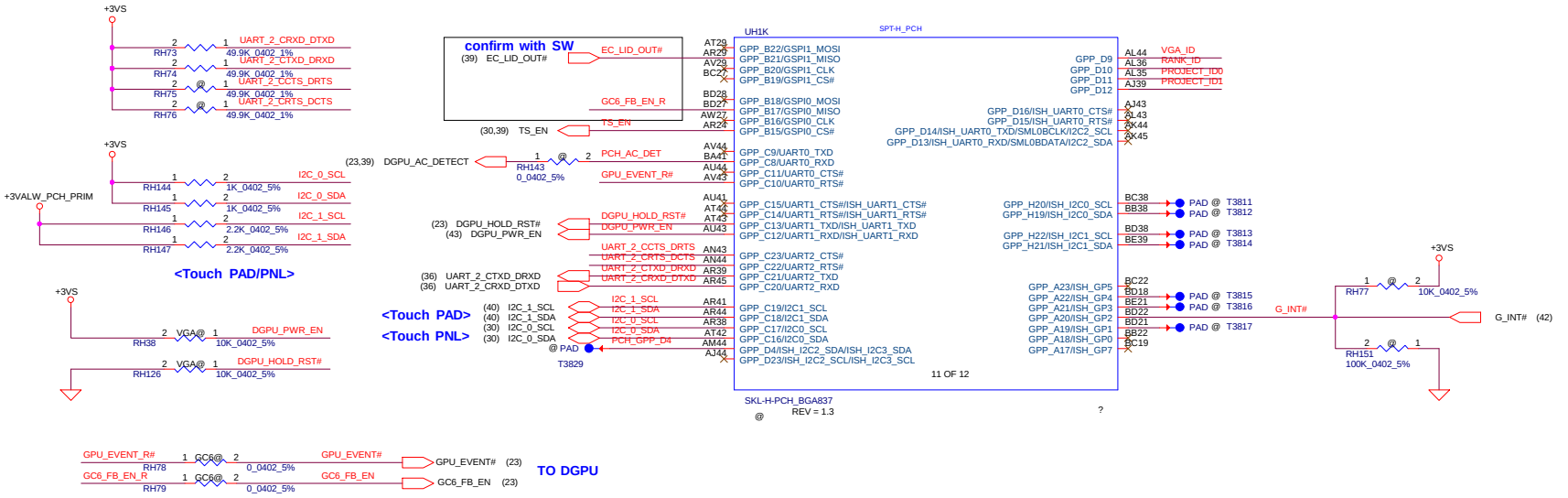
Functional Strap Definitions

GSPI1_MOSI / GPP_B22
int. PD
Boot BIOS Destination
0 = SPI (Default)
1 = LPC

GSPI0_MOSI / GPP_B18
int. PD
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature).



VGA_ID	GPP_D9
SGT	0
VGM	1

RANK_ID	GPP_D10
DR	0
SR	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
*A4WAD	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: PCH(5/7)UART,I2C,GPIO

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 Sheet 20 of 61

+1.0VALW
+1.0VALW_PRIM
RH86 1 @ 2 0_0805_5%
+1.0VALW_PCH
RH104 1 @ 2 0_0805_5%

RH137 for Deep SX.
+1.0VALW_PCH
RH137 1 @ 2 0_0402_5%
+1.0VALW_DCPDSW
Near PIN BA29
CH15 1U_0402_6.3V6K

+1.0VALW_VCCCLK
RH138 1 @ 2 0_0603_5%

LH3 FBMA-L11-160808-800LMT_0603
+1.0VALW_VCCCLK5
Near PIN K2,K3
CH28 22U_0603_6.3V6M
CH29 22U_0603_6.3V6M
CH27 1U_0402_6.3V6K @

+1.0VALW_MPHY
modify follow PDG 05/18
RH113 1 @ 2 0_0603_5%
CH47 22U_0603_6.3V6M
CH48 1U_0402_6.3V6K
CH38 1U_0402_6.3V6K
CH37 1U_0402_6.3V6K
NO USE MPHYGT ON H
CHANGE TO +1.0VALW_MPHY
Near PIN U21,U23,U25,U26,V26
Near PIN V28
Near PIN AC17

+1.0VALW_AMPHYPLL
LH1 FBMA-L11-160808-800LMT_0603
Near PIN A42,A43,B43
CH17 22U_0603_6.3V6M
CH18 22U_0603_6.3V6M
CH19 1U_0402_6.3V6K @

+1.0VALW_AUSB_AZPLL
LH2 FBMA-L11-160808-800LMT_0603
Near PIN AJ5,AL5
CH23 22U_0603_6.3V6M
CH24 22U_0603_6.3V6M

+1.0VALW_PRIMAL22
RH140 1 @ 2 0_0402_5%
+1.0VALW_PRIMAD15
RH141 1 @ 2 0_0402_5%

PCH_EDS Table10-4
12/30 J
UH1H
SPT-H_PCH
+1.0VALW_PRIM
2.899A AA23 VCCPRIM_1P0
AA26 VCCPRIM_1P0
AA28 VCCPRIM_1P0
AC23 VCCPRIM_1P0
AC26 VCCPRIM_1P0
AC28 VCCPRIM_1P0
AE23 VCCPRIM_1P0
AE26 VCCPRIM_1P0
Y23 VCCPRIM_1P0
Y25 VCCPRIM_1P0
+1.0VALW_DCPDSW 0.0454A BA29 DCPDSW_1P0
+1.0VALW_VCCCLK 0.021A N17 VCCCLK1
0.050A R19 VCCCLK3
0.024A U20 VCCCLK4
0.137A V17 VCCCLK2
R17 VCCCLK2
0.006A K2 VCCCLK5
+1.0VALW_VCCCLK5 K3 VCCCLK5
+1.0VALW_MPHY MAX 1.307A U21 VCCMPHY_1P0
U23 VCCMPHY_1P0
U25 VCCMPHY_1P0
U26 VCCMPHY_1P0
V26 VCCMPHY_1P0
+1.0VALW_AMPHYPLL 0.110A A43 VCCMPHYPLL_1P0
B43 VCCMPHYPLL_1P0
C44 VCCPCIE3PLL_1P0
C45 VCCPCIE3PLL_1P0
modify follow PDG 05/18
+1.0VALW_MPHY 0.030A V28 VCCAPLLEBB_1P0
0.533A AC17 VCCPRIM_1P0
+1.0VALW_AUSB_AZPLL 0.012A AJ5 VCCUSB2PLL_1P0
AL5 VCCUSB2PLL_1P0
0.033A AN19 VCCHDAPLL_1P0
+3VALW_HDA 0.075A BA15 VCCHDA
+3VALW_DSW W15 VCCDSW_3P3
CH54 1U_0402_6.3V6K
Near PIN W15
Add 05/18
CORE VCCPRIM_1P0 AL22 0.0908A +1.0VALW_PRIMAL22
VCCDSW_3P3 BA24 0.195A +3VALW_DSW
VCCPGPPA BA31 0.082A +3VALW_PCH_PRIM
VCCPGPBCH BC42 0.2726A
VCCPGPBCH BD40
VCCPGPEF AJ41 0.1410A
VCCPGPEF AL41
VCCPGPPG AD41 0.1318A
VCCPRIM_3P3 AN5 0.2875A
VCCPRIM_1P0 AD15 0.0061A +1.0VALW_PRIMAD15
VCCATS AD13 0.007A +3VS_VCCATS
VCCRTCPRIM_3P3 BA20 0.0002A +3VALW_PCH_PRIM
VCCRTC BA22 +RTCVCC
DCPRTC BA26
Near PIN BA26
CH26 1U_0402_16V7K
VCCPRIM_1P0 AJ20 +1.0VALW_PRIM
AJ21
AJ23
AJ25
MPHY VCCSPI BE41 0.029A +3VALW_SPI
VCCSPI BE43
VCCSPI BE42
VCCSPI BC44 0.078A +3VALW_PCH_PRIM
VCCPGPPD BA45
VCCPGPPD BC45
VCCPGPPD BB45
USB VCCPRIM_3P3 BD3 0.117A +3VALW_PCH_PRIM
VCCPRIM_3P3 BE3
VCCPRIM_3P3 BE4
VCCHDA
VCCDSW_3P3
8 OF 12
SKL-H-PCH_BGA837
@ REV = 1.3

+3VALW
+3VALW_DSW
RH135 1 @ 2 0_0603_5%
+3VALW_PCH_PRIM
RH89 1 @ 2 0_0805_5%
+3VALW_HDA
RH136 1 @ 2 0_0402_5%

+3VALW_PCH_PRIM
+3VALW_SPI
RH27 1 @ 2 0_0402_5%

+3VALW_PCH_PRIM
CH20 1 @ 2 1U_0402_6.3V6K Near PIN BD3,BE3,BE4
CH21 1 @ 2 1U_0402_6.3V6K Near PIN BA20
CH22 1 2 .1U_0402_16V7K Near PIN AN5
CH25 1 2 1U_0402_6.3V6K No requirment Near PIN BC44
CH30 1 2 .1U_0402_16V7K Near PIN BC42,BD40
CH31 1 2 .1U_0402_16V7K Near PIN AJ41 , AL41
CH32 1 2 .1U_0402_16V7K Near PIN AD41
CH35 1 2 .1U_0402_16V7K
CH36 1 2 1U_0402_6.3V6K Near PIN BA20

+3VS
+3VS_VCCATS
RH87 1 @ 2 0_0402_5%
CH16 1 @ 2 1U_0402_6.3V6K Near PIN AD13

+3VALW_PCH_PRIM
CH39 1U_0402_6.3V6K
+1.0VALW_PRIM
CH40 1U_0402_6.3V6K
+3VALW_PCH_PRIM
CH41 22U_0603_6.3V6M
CH42 22U_0603_6.3V6M
+1.0VALW_PRIM
CH43 22U_0603_6.3V6M
CH44 22U_0603_6.3V6M

Power Rail	Voltage
+CHGRTC	3.383V(MAX)
BAT54C(VF)	240 mV
+3VL_RTC	3.143V
Result : Pass	

RTC Battery
+RTCBATT
+CHGRTC
W=20mils
DH2
+RTCVCC
W=10mil
W=20mils
BAS40-04_SOT23-3
CH45 1U_0402_6.3V6K
CH46 .1U_0402_16V7K
Near PIN BA22
09/26 dan

Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.
Title: PCH(6/7)POWER
Size: Custom
Document Number: A4WAD M/B LA-C871P
Rev: 1.0
Date: Monday, July 13, 2015
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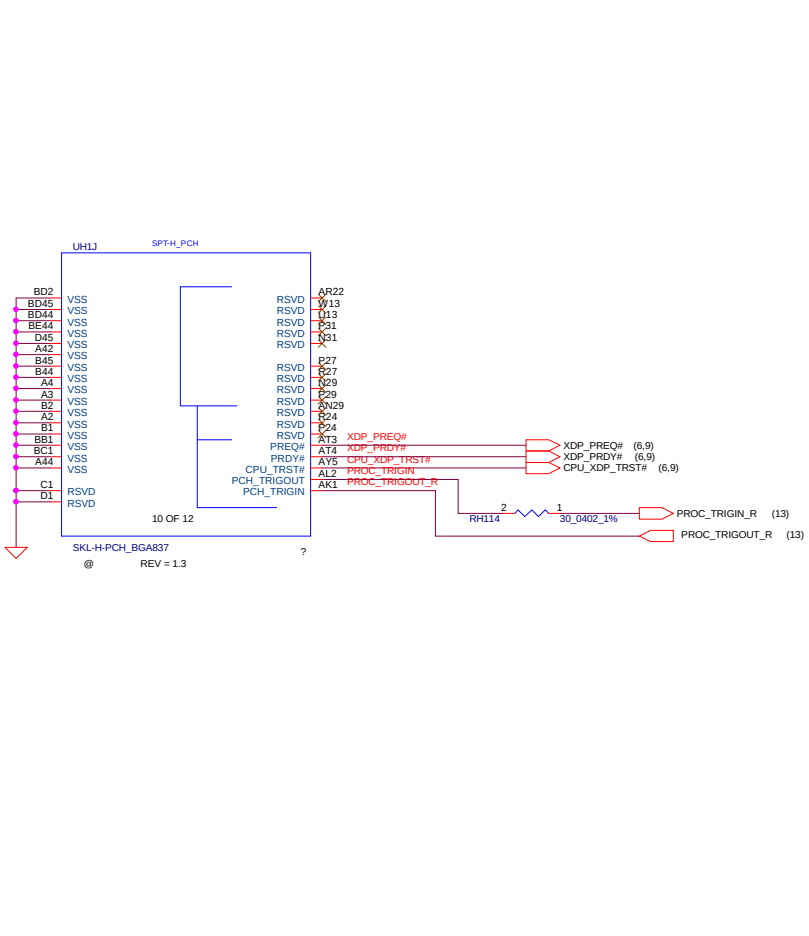
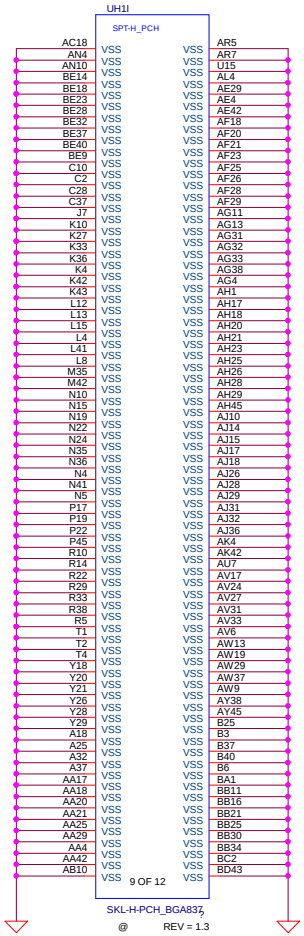
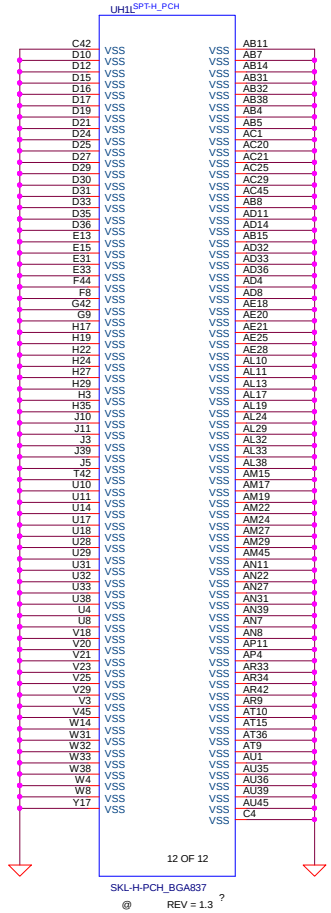






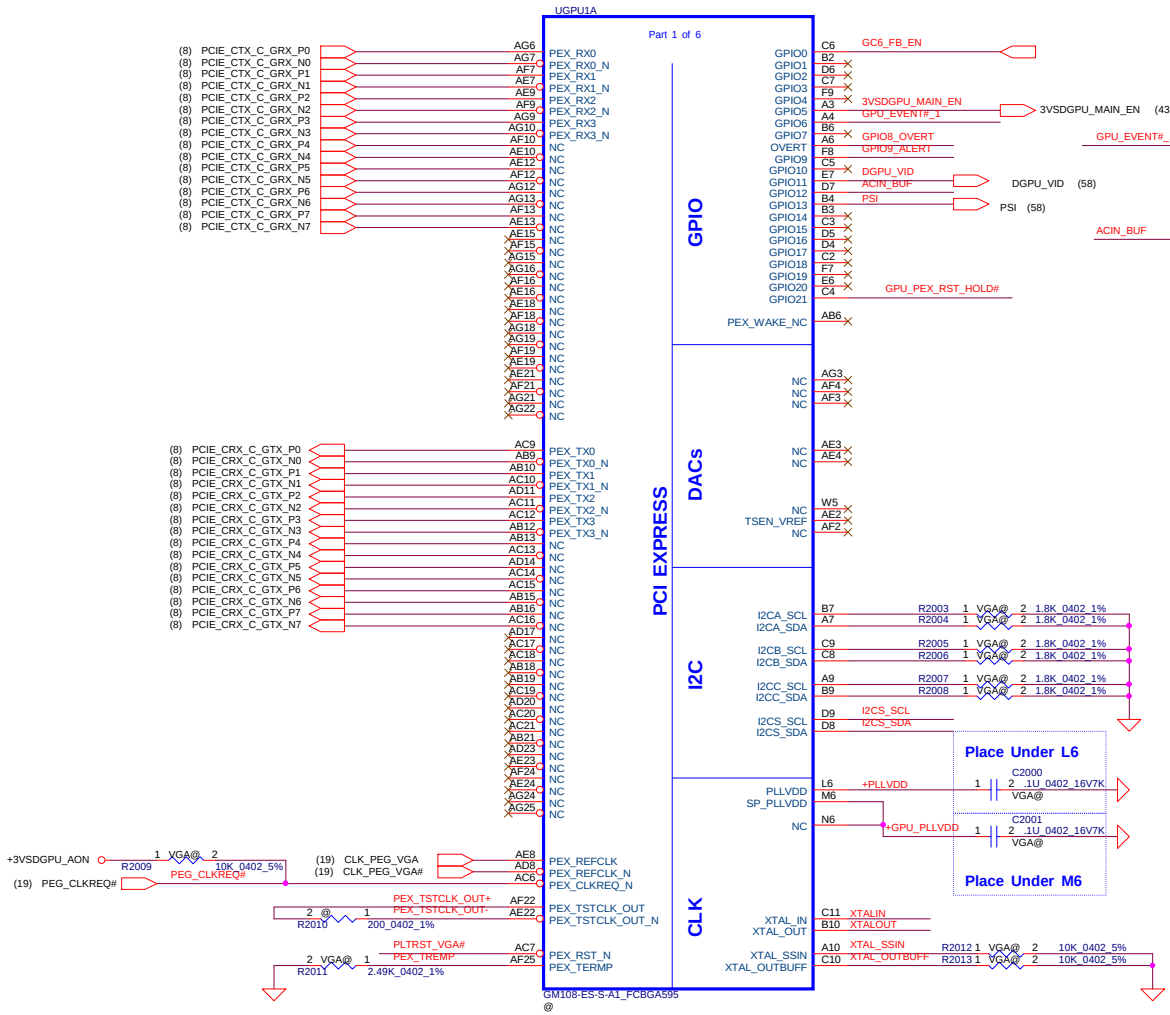
Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

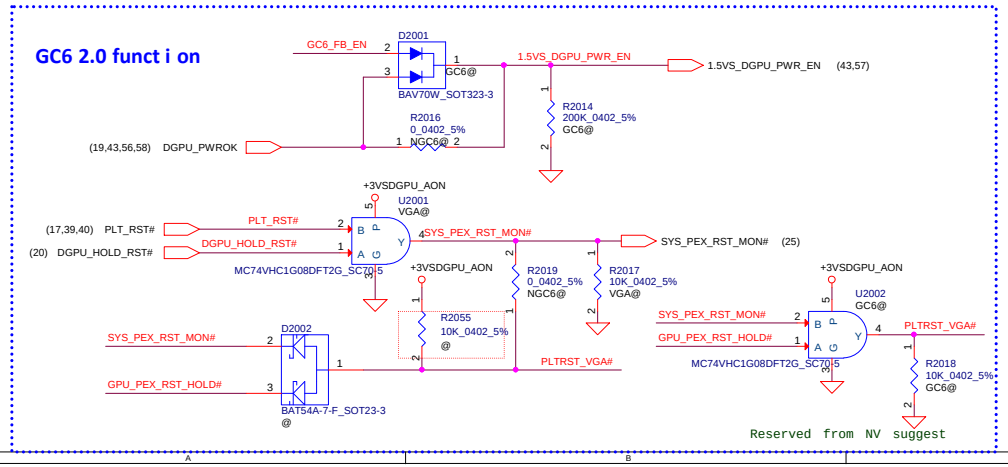
Title: PCH(7/7)GND

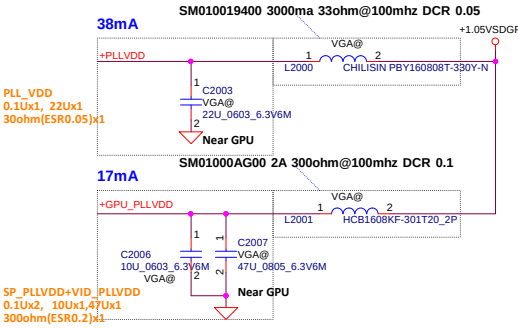
Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

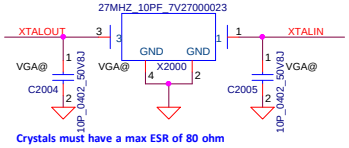
Date: Monday, July 13, 2015 Sheet 22 of 61



GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		







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Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: N16x(1/7) PEG & DAC

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

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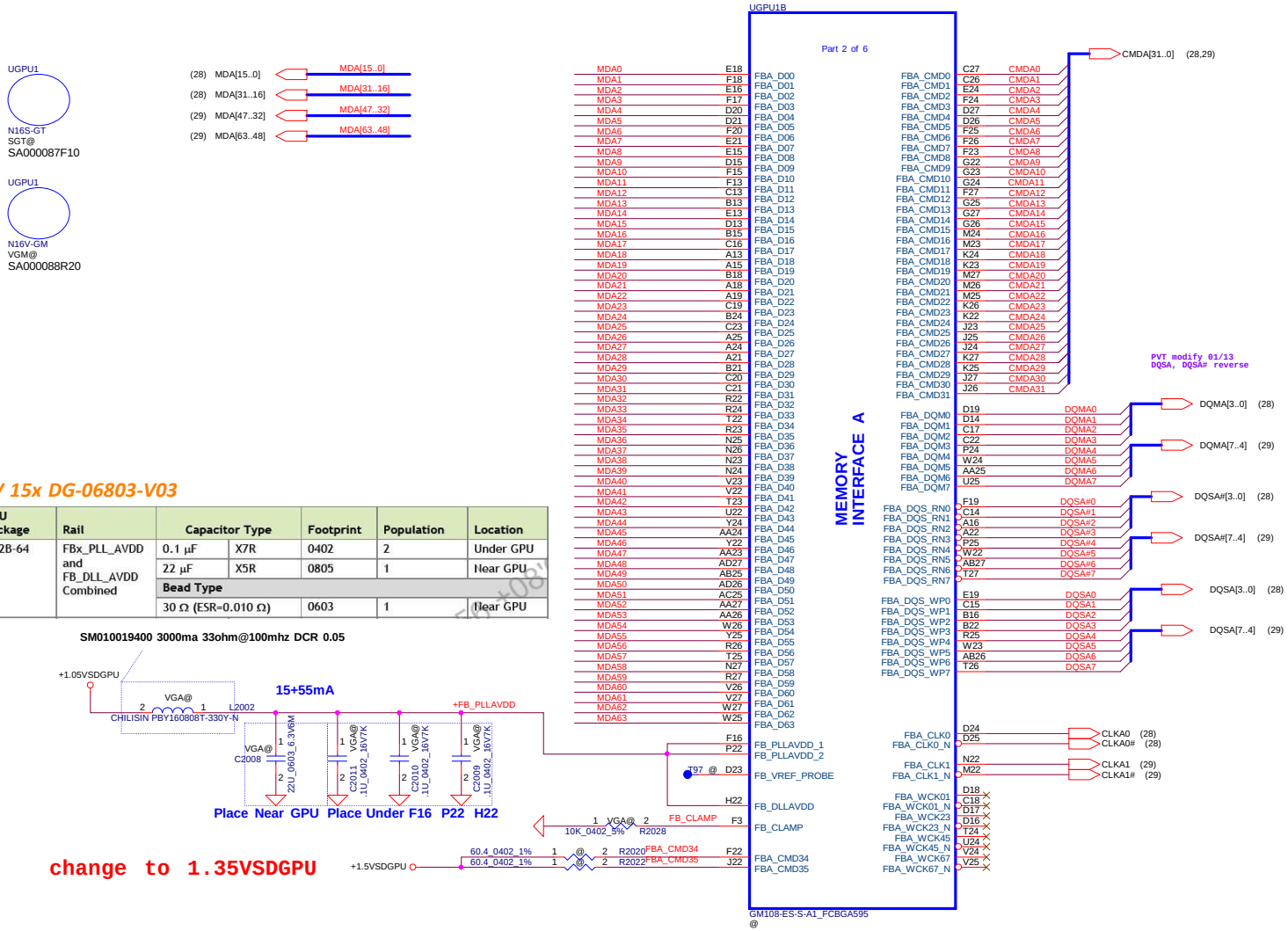
VRAM Interface



NV 15x DG-06803-V03

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

SM010019400 3000ma 33ohm@100mhz DCR 0.05

15+55mA

Place Near GPU Place Under F16 P22 H22

change to 1.35VSDGPU

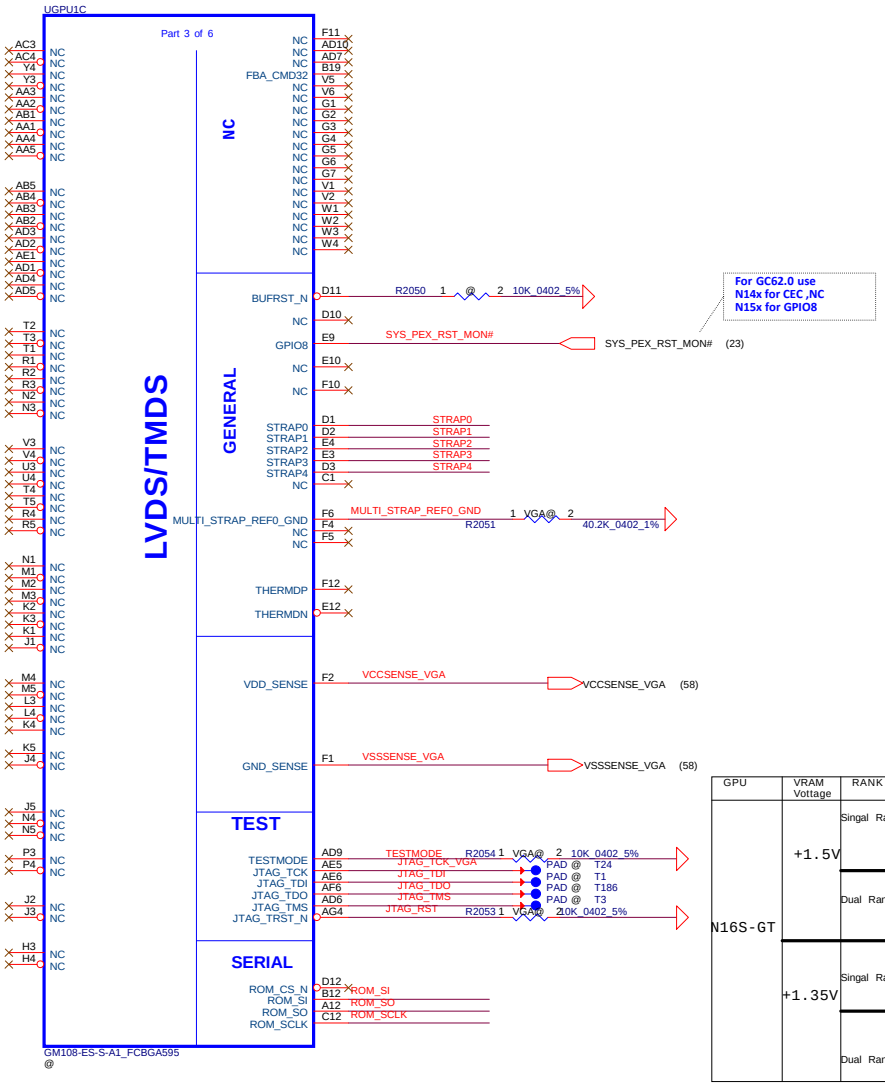
Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

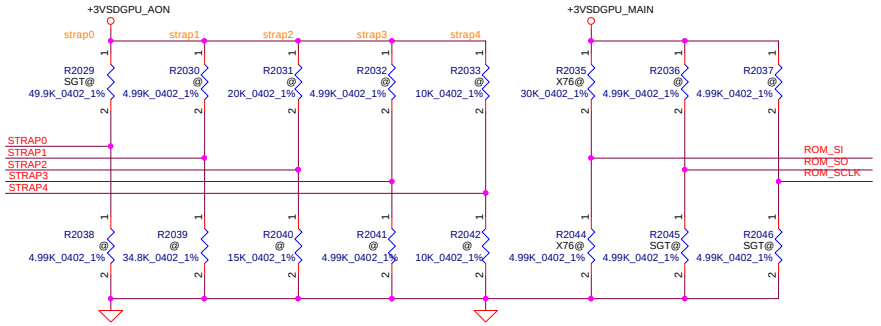
Title: **N16x(2/7) VRAM Interface**

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 Sheet 24 of 61



MULTI LEVEL STRAPS



N16VGM Option Component

```
STRAP0  --->  R2029 2 VGM@1 45.3K_0402_1% SD034453280
STRAP1  --->  R2039 2 VGM@1 45.3K_0402_1% SD034453280
STRAP2  --->  R2031 2 VGM@1 10K_0402_1%   SD034100280
STRAP3  --->  R2041 2 VGM@1 4.99K_0402_1% SD034499180
STRAP4  --->  R2042 2 VGM@1 45.3K_0402_1% SD034453280
ROM_SO  --->  R2036 2 VGM@1 4.99K_0402_1% SD034499180
ROM_SCLK--->  R2037 2 VGM@1 4.99K_0402_1% SD034499180

ROM_SI pull down 15kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x2
ROM_SI pull down 10kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x1
ROM_SI pull down 25kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x4
ROM_SI pull up 35kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0xE
ROM_SI pull up 30kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0xD
ROM_SI pull down 30kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x5
ROM_SI pull up 25kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0xC
```

N16SGT Option Component

```
ROM_SI pull down 4.99kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x0
ROM_SI pull down 10kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x1
ROM_SI pull down 15kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x2
ROM_SI pull down 20kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x3
ROM_SI pull down 25kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x4
ROM_SI pull down 30kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x5
```

For N16S-GT Multi strap table

Decive ID : 0x1347

GPU	VRAM Vottage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16S-GT	+1.5V	Singal Rank		1GHz	256Mx16x4 2GB	0x0 (SA00006E840) Hynix H5TC4G63AFR-11C	PU 50K	NC	NC	NC	NC	PD 4.99K	PD 4.99K	PD 4.99K
						0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
						0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
		Dual Rank	X76607B0L01	1GHz	256Mx16x8 4GB	0x0 (SA00006E840) Hynix H5TC4G63AFR-11C						PD 4.99K		
			X76607B0L03			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76607B0L02			0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
	+1.35V	Singal Rank		900MHz	256Mx16x4 2GB	0x3 (SA00006E840) Hynix H5TC4G63AFR-11C						PD 20K		
						0x4 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 25K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		
		Dual Rank		900MHz	256Mx16x8 4GB	0x3 (SA00006E840) Hynix H5TC4G63AFR-11C						PD 20K		
						0x4 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 25K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		

For N16V-GM Multi strap table

Decive ID : 0x1299

GPU	VRAM Vottage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16V-GM	+1.5V	Singal Rank		1GHz	256Mx16x8 4GB	0x2 (SA00006E840) Hynix H5TC4G63AFR-11C	PU 45.3K	PD45.3K	PU 10K	PD 4.99K	PD 45.3K	PD 15K	PU 4.99K	PU 4.99K
						0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
						0x4 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 25K		
	+1.35V	Singal Rank		900MHz	256Mx16x4 2GB	0xE (SA00006E840) Hynix H5TC4G63AFR-11C						PU 30K		
						0xD (SA000077K20) Micron MT41J256M16HA-093G:E						PU 25K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		
		Dual Rank		900MHz	256Mx16x4 2GB	0xE (SA00006E840) Hynix H5TC4G63AFR-11C						PU 30K		
						0xD (SA000077K20) Micron MT41J256M16HA-093G:E						PU 25K		
						0xC (SA000076P20) Samsung K4W4G1646D-BC1A						PU 20K		

ZZZ X7601@	ZZZ X7602@	ZZZ X7603@	ZZZ X7604@	ZZZ X7605@	ZZZ X7606@
X76614BOL51 GM2G SAM 256M16	X76614BOL52 GM2G HYN 256M16	X76614BOL53 GT2G SAM 256M16	X76614BOL54 GT2G HYN 256M16	X76614BOL55 GM2G MIC 256M16	X76614BOL56 GT2G MIC 256M16
ZZZ X7607@	ZZZ X7608@				
X76614BOL57 GM2G SAM-N 256M16	X76614BOL58 GT2G SAM-N 256M16				

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Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **N16x(3/7) LVDS&TMDS**

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

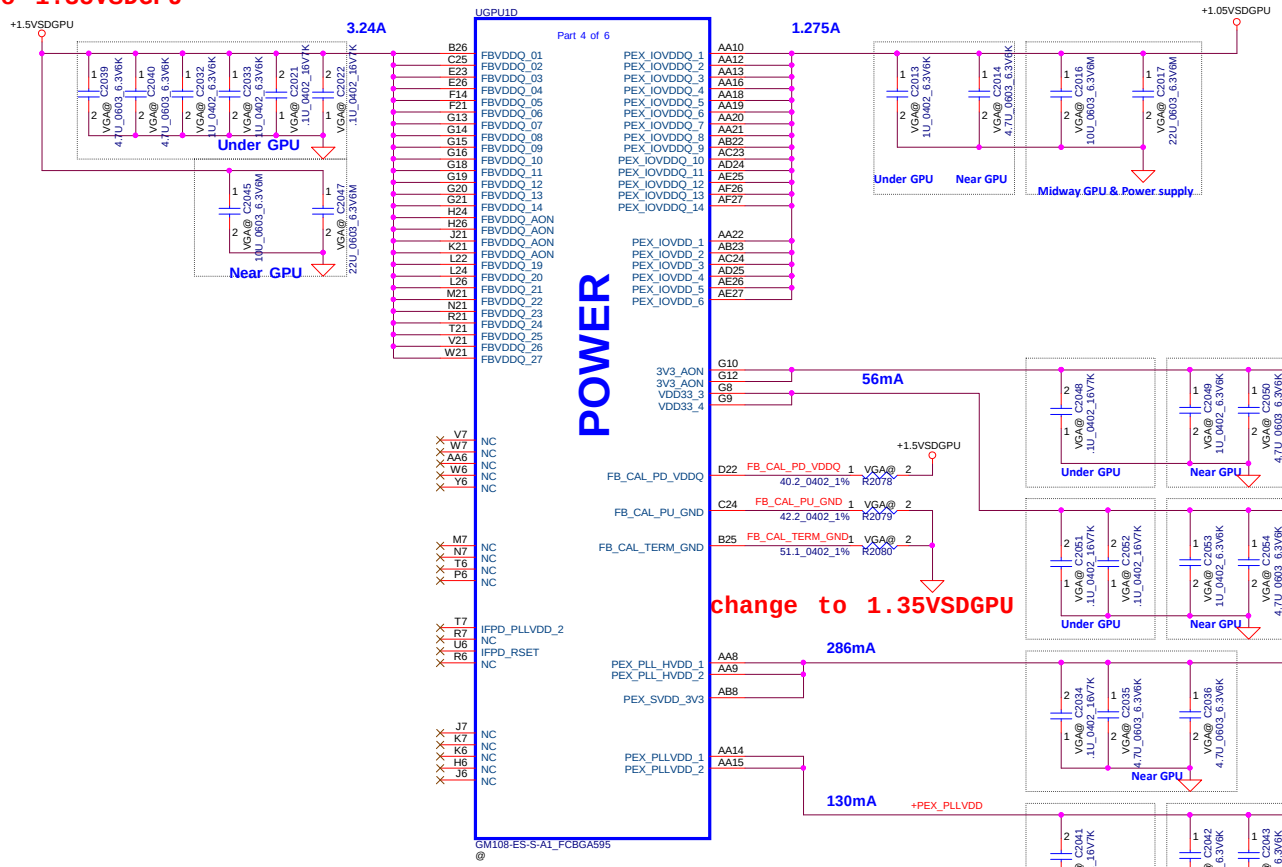
Date: Monday, July 13, 2015 Sheet 25 of 61

NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64 DDR3	0.1μF	X7R	0402	2	2	Under GPU
	1 μF	X7R	0603	2	2	Under GPU
	4.7 μF	X6S	0603	2	2	Under GPU
	10 μF	X5R	0805	1	1	Near GPU
	22 μF	X5R	0805	1	1	Near GPU

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 μF	X6S	0402	1	Under GPU
	4.7 μF	X6S	0603	1	Near GPU
	10 μF	X5R	0805	1	Midway between GPU and Power Supply
	22 μF	X5R	0805	1	Midway between GPU and Power Supply

change to 1.35VSDGPU



GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1μF	X6S	0402	2	2	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1μF	X6S	0402	1	1	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X5R	0402	1	Near GPU
4.7 μF	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X6S	0402	1	Under GPU
1.0 μF	X5R	0603	1	Near GPU
4.7 μF	X5R	0805	1	Near GPU

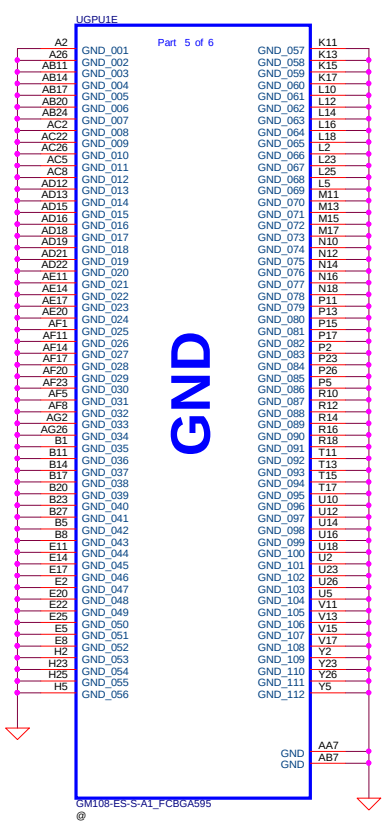
Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

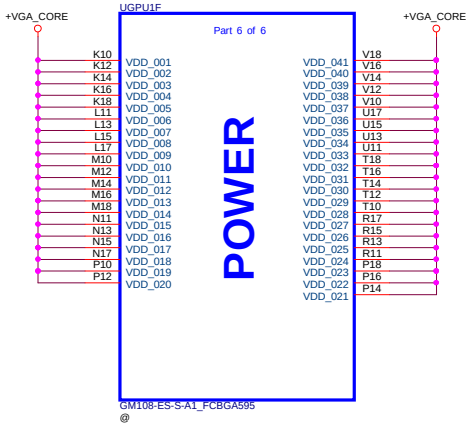
Compal Electronics, Inc.

Title: N16x(4/7)POWER

Size: Custom | Document Number: A4WAD M/B LA-C871P | Rev: 1.0

Date: Monday, July 13, 2015 | Sheet 26 of 61





NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core — (A)	FB Total 1.5/1.35V (A)	1.05V Total 1.05V (A)
~~N15S-GM~~	~~DDR3/L~~	~~48.11~~	~~4.23~~	~~0.91~~
N15S-GT	DDR3/L	60.07	4.26	0.91

DA-06925-V05

Table 6. EDP-Peak at T_J = 102°C

Power Supply Rail	N15V-GM-S DDR3/L
(V)	(A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

DA07075-V01

Table 7. EDP-Peak at T_J = 102°C

Power Supply Rail	N15V-GL DDR3
(V)	(A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

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Title: N16x(5/7)POWER & GND

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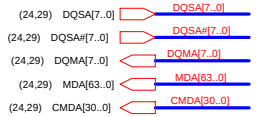
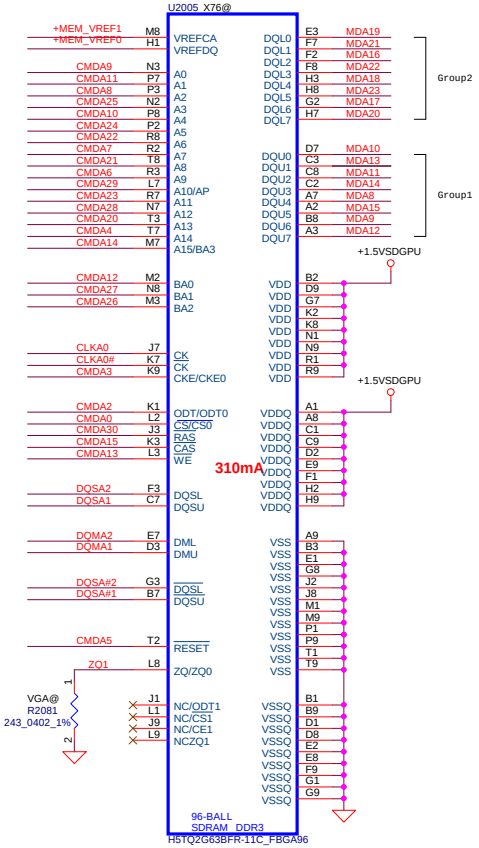
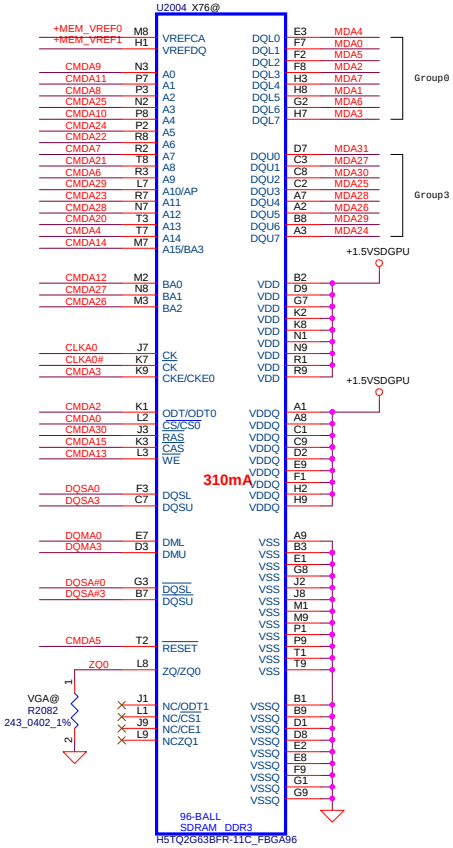
VRAM DDR3 chips

LOW BIT





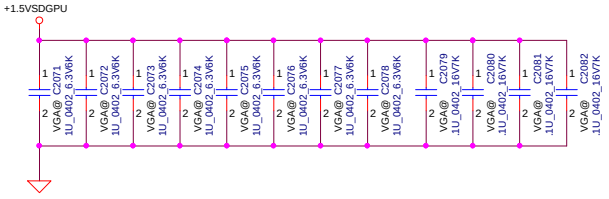


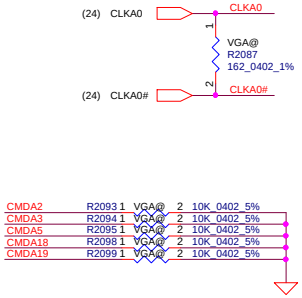
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

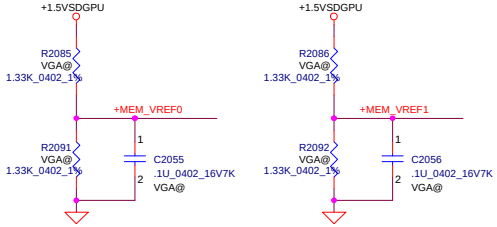
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM







Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: N16x(6/7)VRAM Upper Rank0

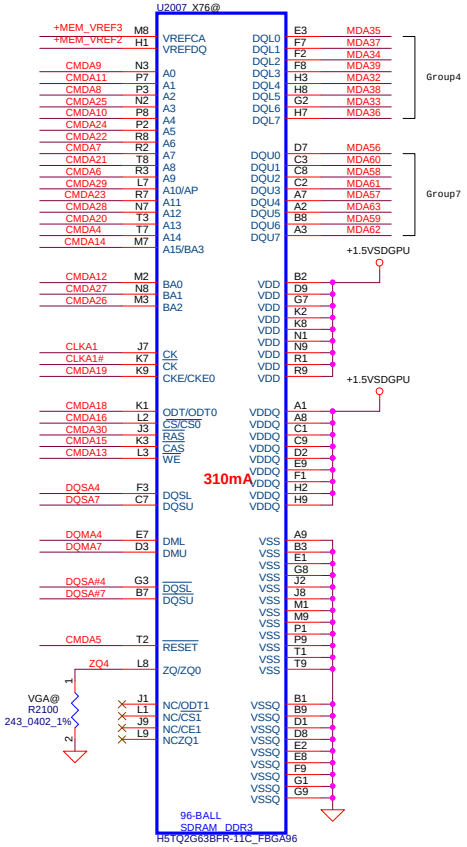
Size: Custom | Document Number: A4WAD M/B LA-C871P | Rev: 1.0

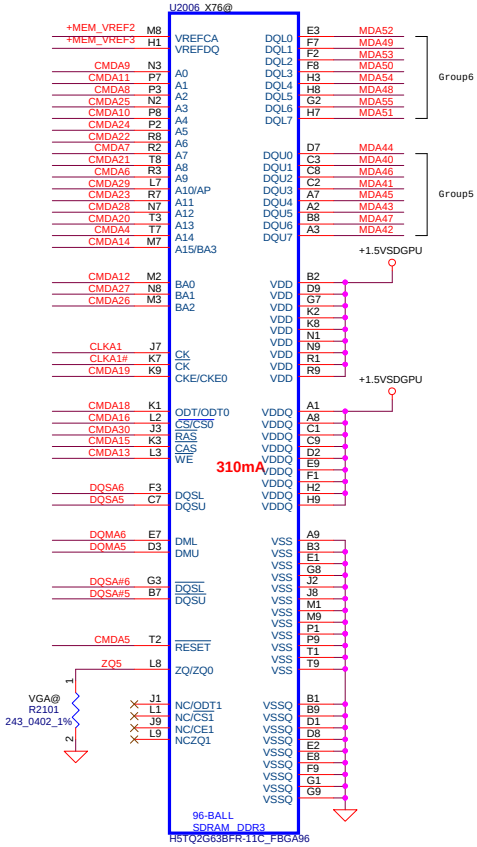
Date: Monday, July 13, 2015 | Sheet 28 of 61

VRAM DDR3 chips

(24,28) DQSA[7..0] → DQSA[7..0]
(24,28) DQSA#[7..0] → DQSA#[7..0]
(24,28) DQMA[7..0] → DQMA[7..0]
(24,28) MDA[63..0] → MDA[63..0]
(24,28) CMDA[30..0] → CMDA[30..0]

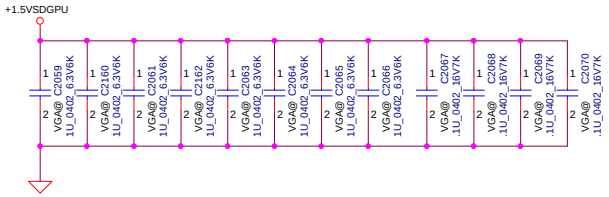
HIGH BIT

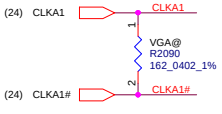


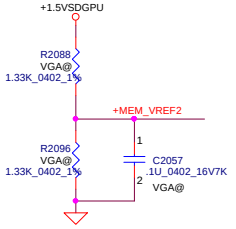


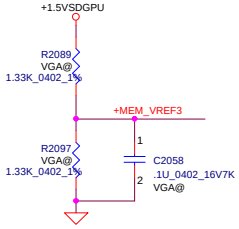
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination









Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: N16x(7/7(VRAM Lower Rank0

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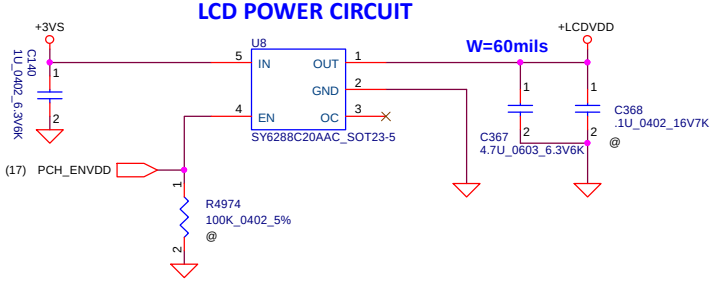
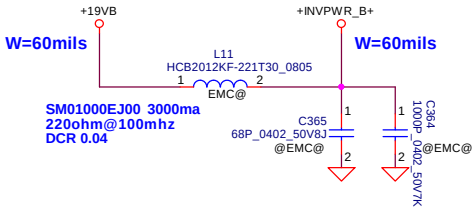
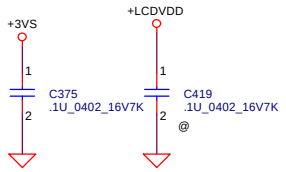
LCD POWER CIRCUIT

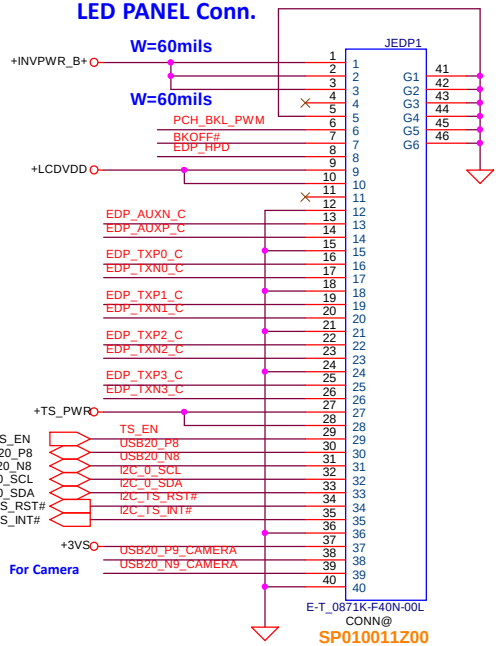


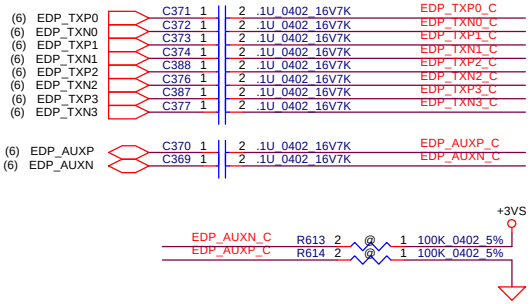


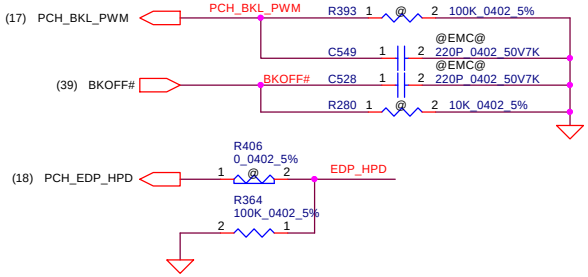
Place closed to JEDP1



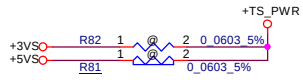
LED PANEL Conn.





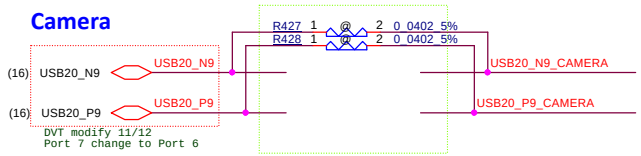


I2C Touch Screen



SPI touch RST follow CRB #544669 P.8

Camera



Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title: eDP CONN.			
Size: Custom	Document Number: A4WAD M/B LA-C871P		Rev: 1.0
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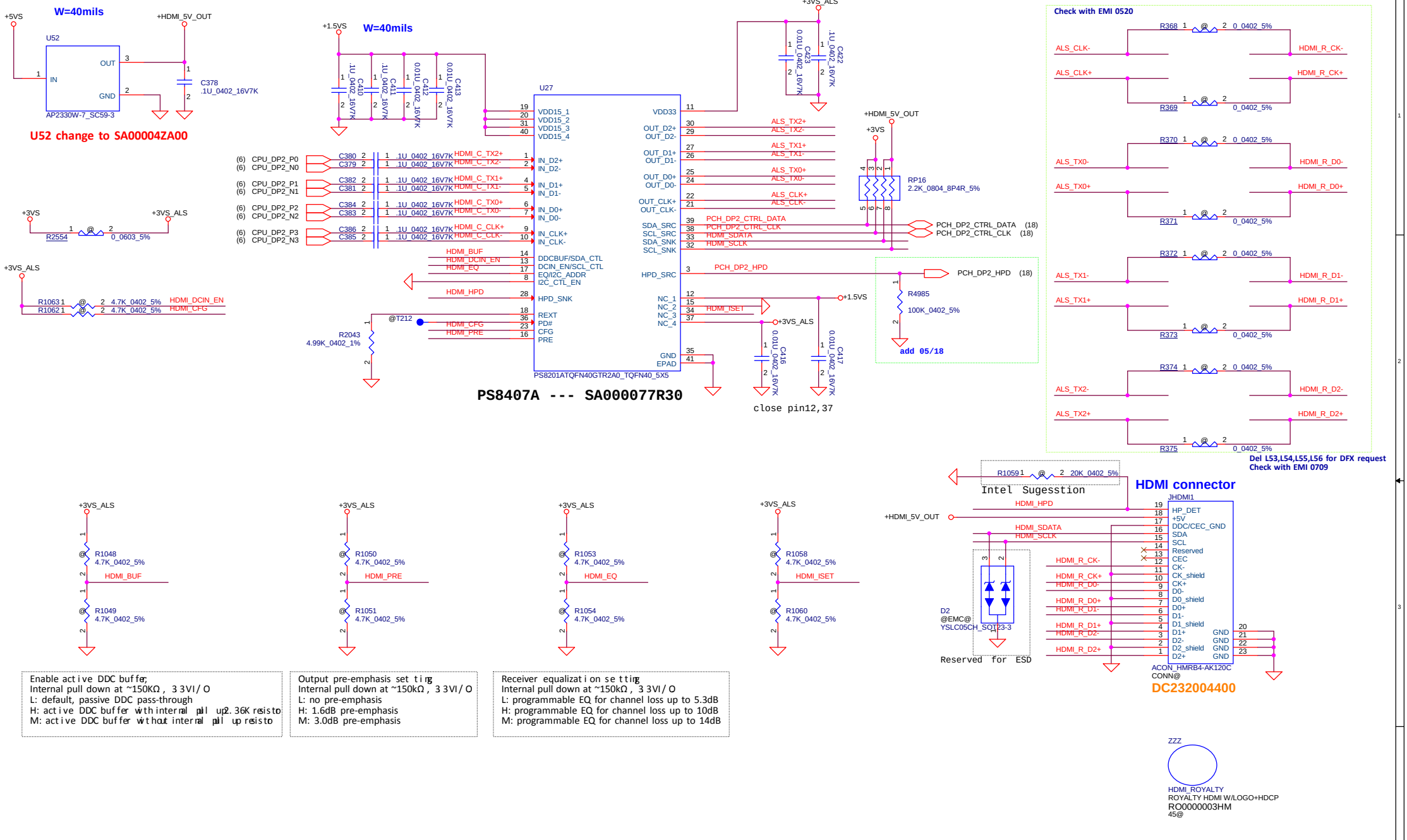
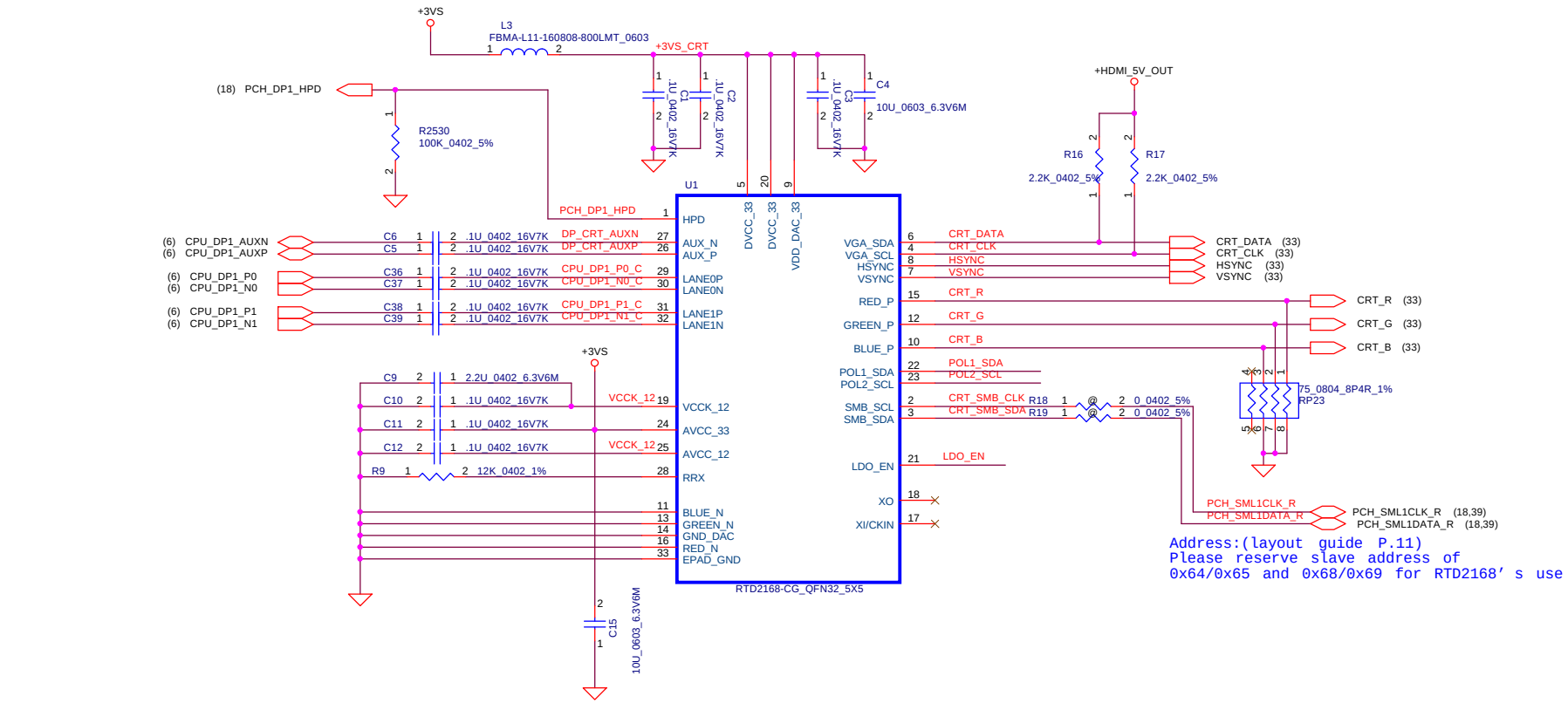


Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title	HDMI PS8407 CONN.		
Size: Custom	Document Number: A4WAD M/B LA-C871P		Rev: 1.0
Date: Monday, July 13, 2015	Sheet 31 of 61		



		POL_SDA	
		0	1
POL_SCL	0	X	EP
	1	*ROM	EEPROM

ROM: Internal ROM
EP: Programmed external EC
EEPROM: External ROM

LDO_EN:
*1: Internal 1.2V
0: External 1.2V

Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: CRT Realtek RTD2168

Size	Document Number	Rev
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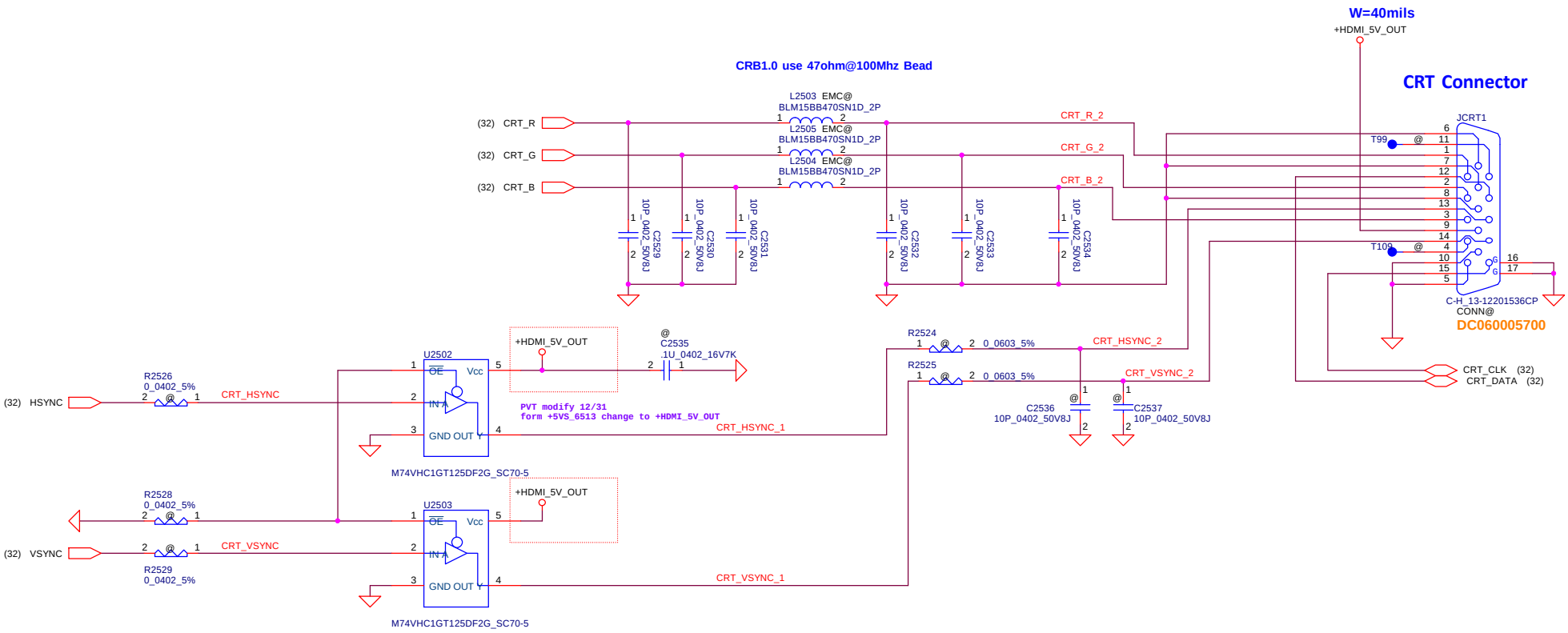
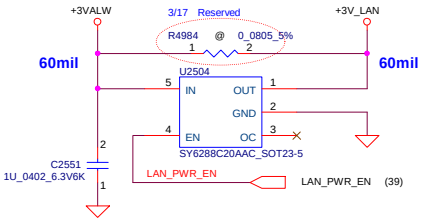
CRT conn.



Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title: CRT Connector			
Size: Custom	Document Number: A4WAD M/B LA-C871P		Rev: 1.0
Date: Monday, July 13, 2015	Sheet 33 of 61		

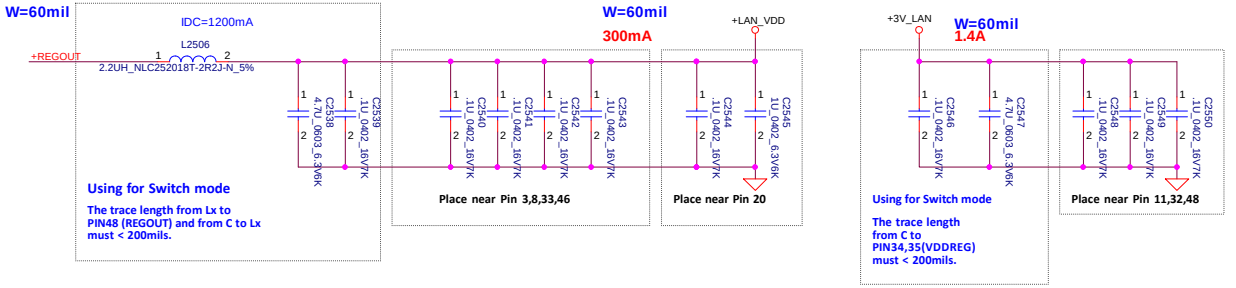
LAN-RTL8411B



From EC

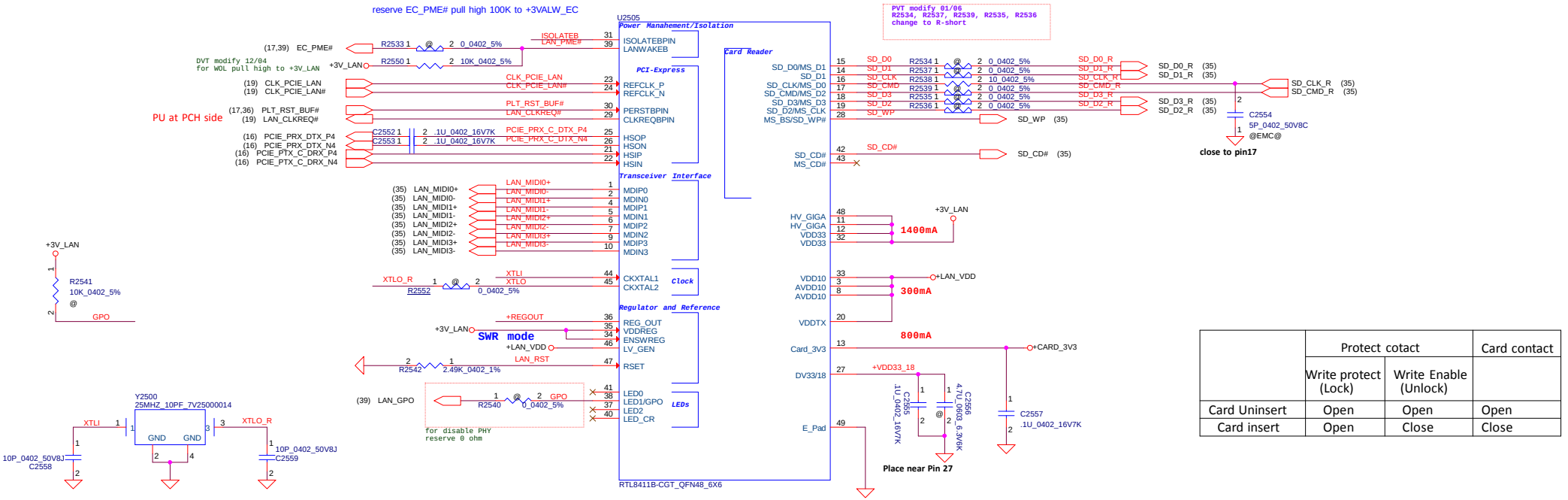
High act i ve
EN threshold voltage min:1.2V typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

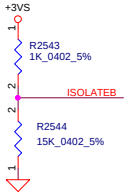
+3V_LAN Rising t i me must >0 5 ms and <100 ms



reserve EC_PME# pull high 100K to +3VALW_EC

PVT modify 01/06
R2534, R2537, R2539, R2535, R2536 change to R-short





	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: LAN RTL8411B

Size: Custom | Document Number: A4WAD M/B LA-C871P | Rev: 1.0

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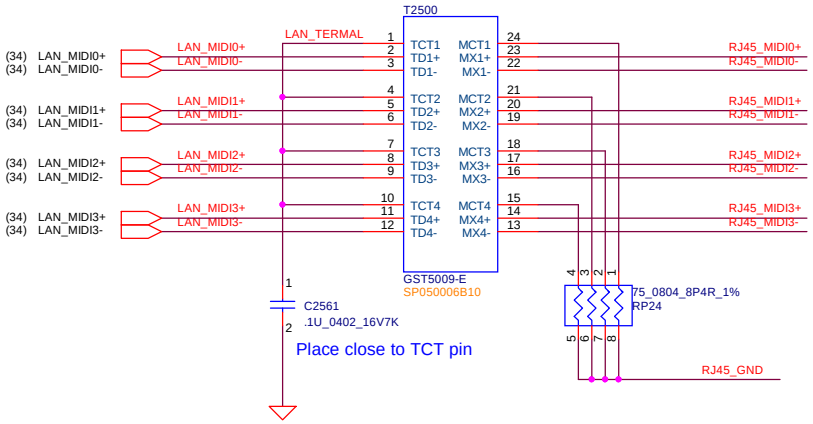
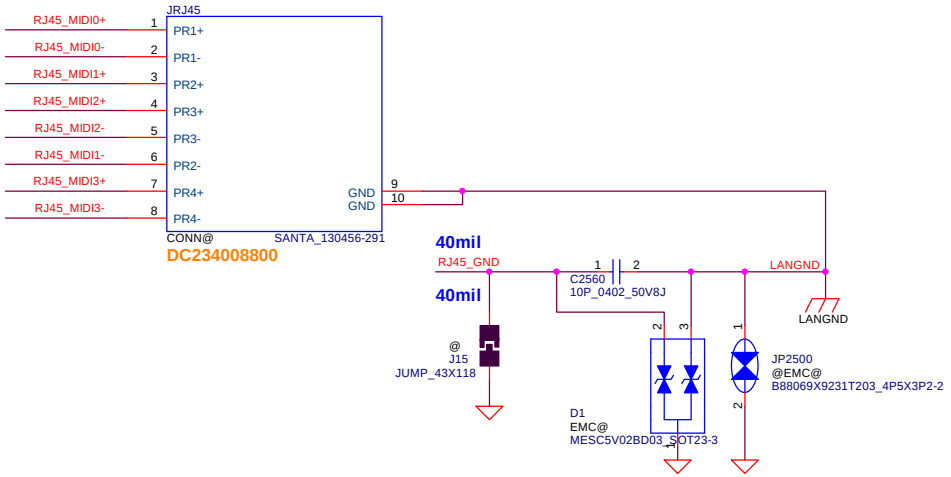
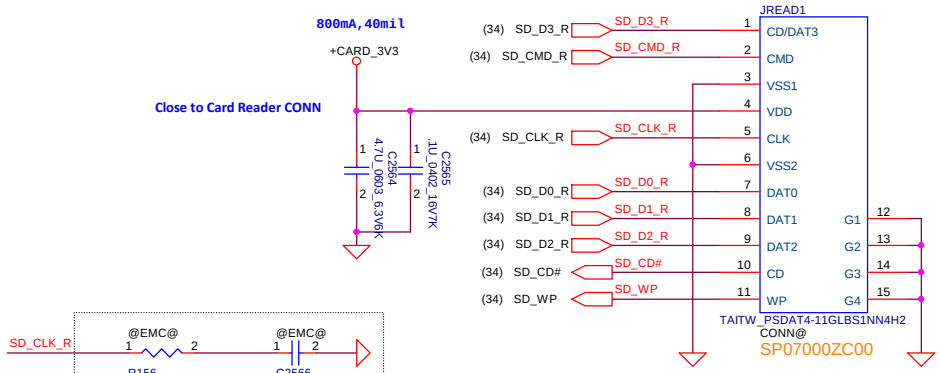
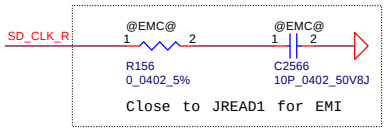
LAN Connector





Card Reader Connector





Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **LAN RJ45/CR SD Connector**

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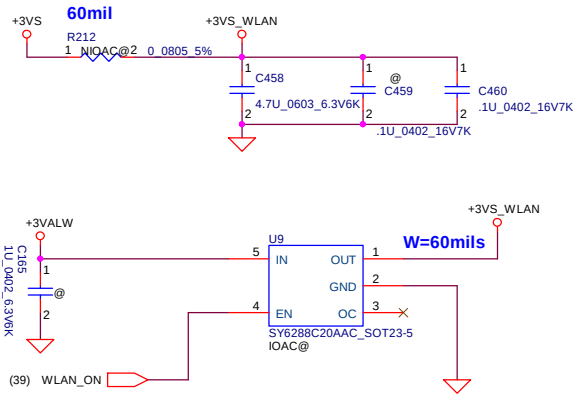
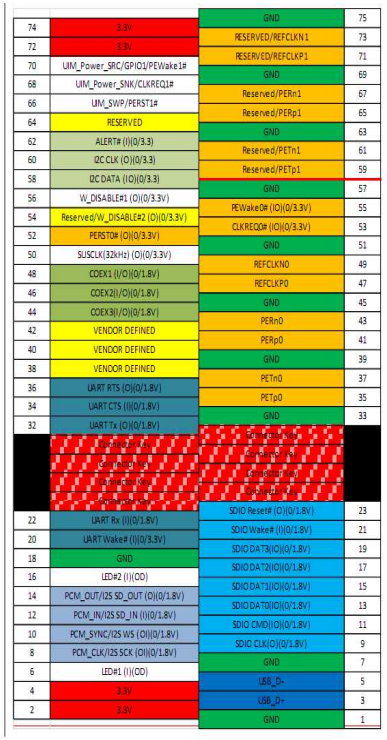
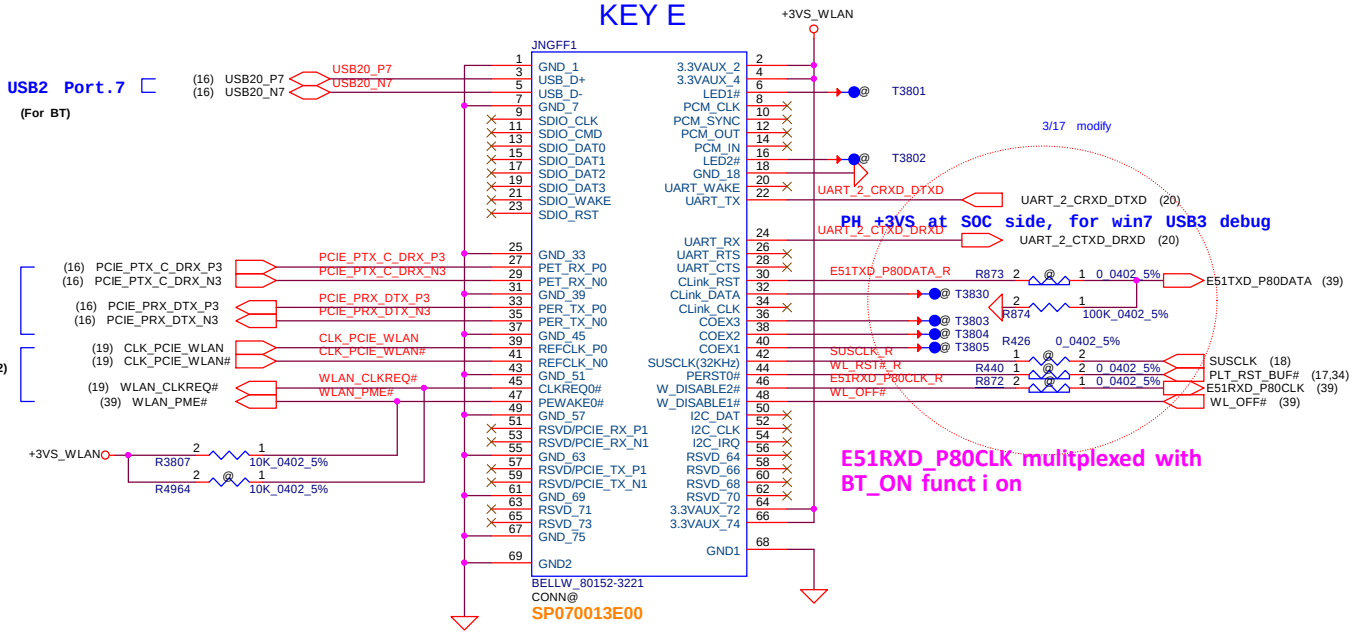
Wireless LAN



NGFF WL+BT (KEY E)



KEY E



~~3.1.8.1.~~3.1.7.1. UART Wakeup

The UART power management protocol supports the following 4-wire and 5-wire interfaces:

- ~~RDX~~UART_RXD (Input): Receive Data
- ~~RTX~~UART_TXD (Output): Transmit Data
- UART_RTS (Input): Request to Send (Host Flow Control)
- UART_CTS (Output): Clear to Send (Device Flow Control)
- ~~Host Wake Up~~UART_Wake# (Output): Host wake-up line is optional in case the host support in band wake-up

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Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.	
Title	M.2 Key E (WLAN)
Size: Custom	Document Number: A4WAD M/B LA-C871P
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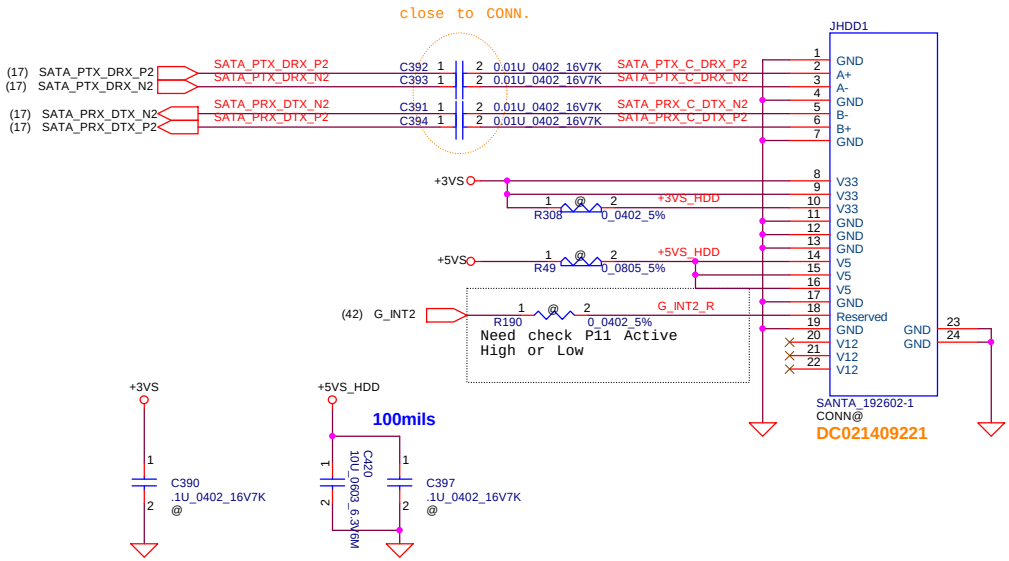
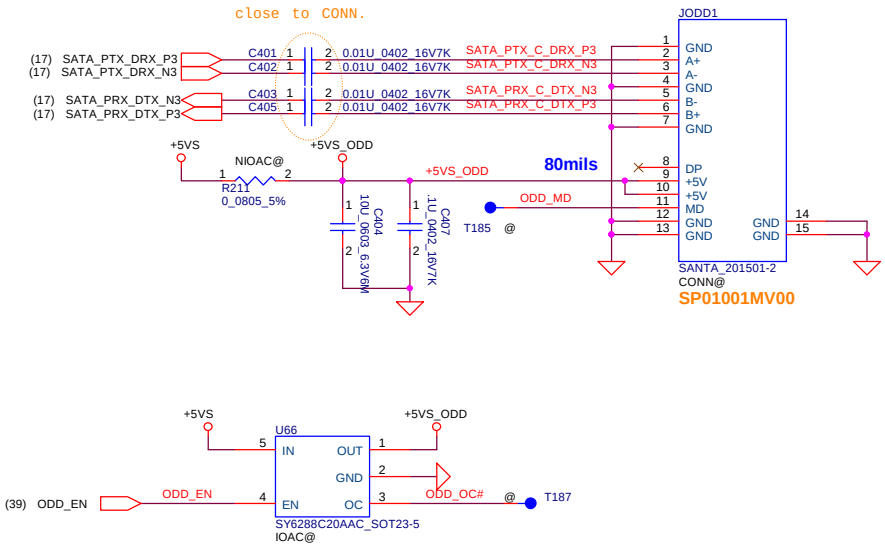
SATA HDD Conn.



SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title: HDD/ODD/ HDD Re-Driver			
Size: Custom	Document Number: A4WAD M/B LA-C871P		Rev: 1.0
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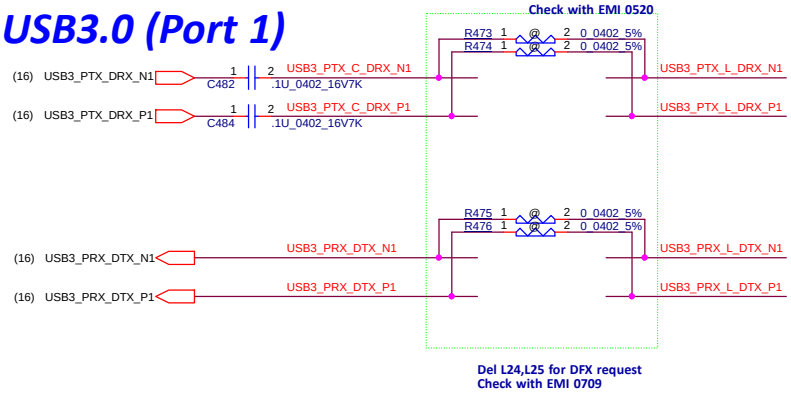
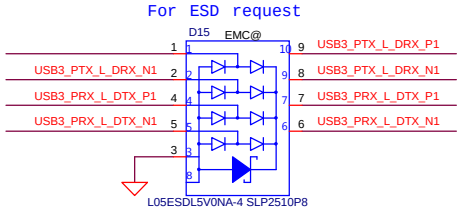
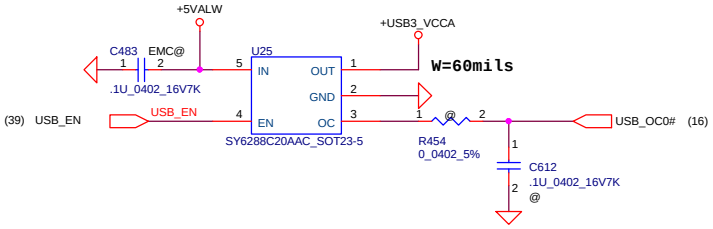
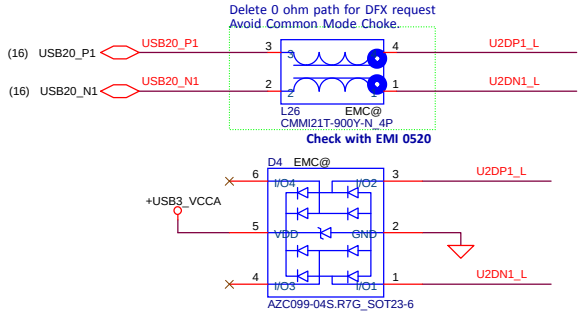
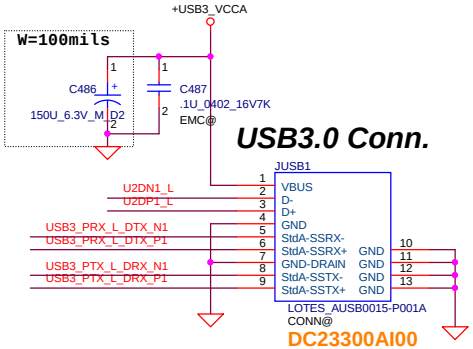
USB3.0 (Port 1)



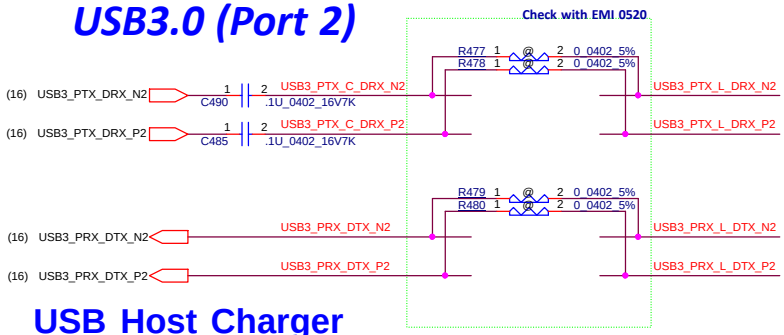


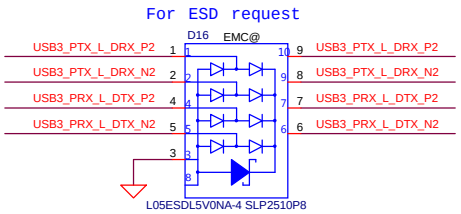


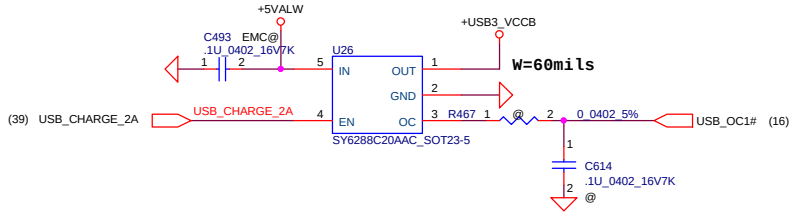




USB3.0 (Port 2)

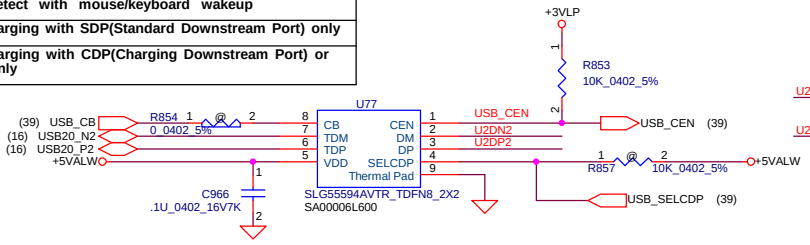


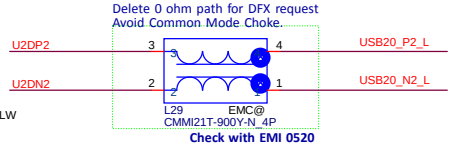


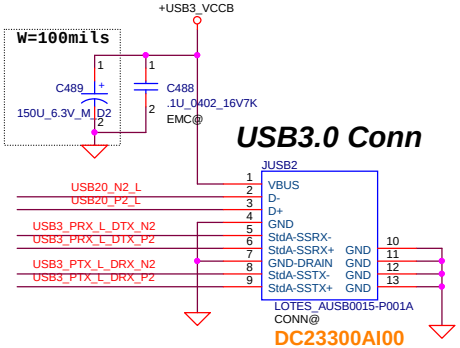


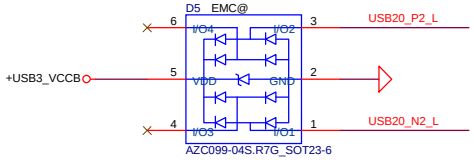
USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only

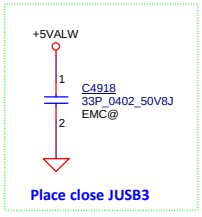


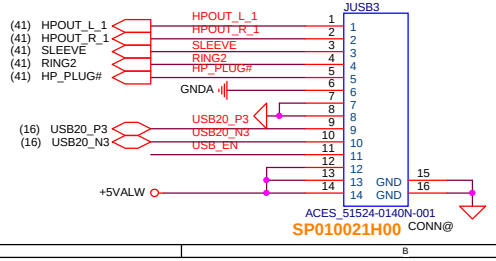






USB/B (USB Port 3, + AUDIO)





Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **USB3.0 Conn/USB_B**

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0
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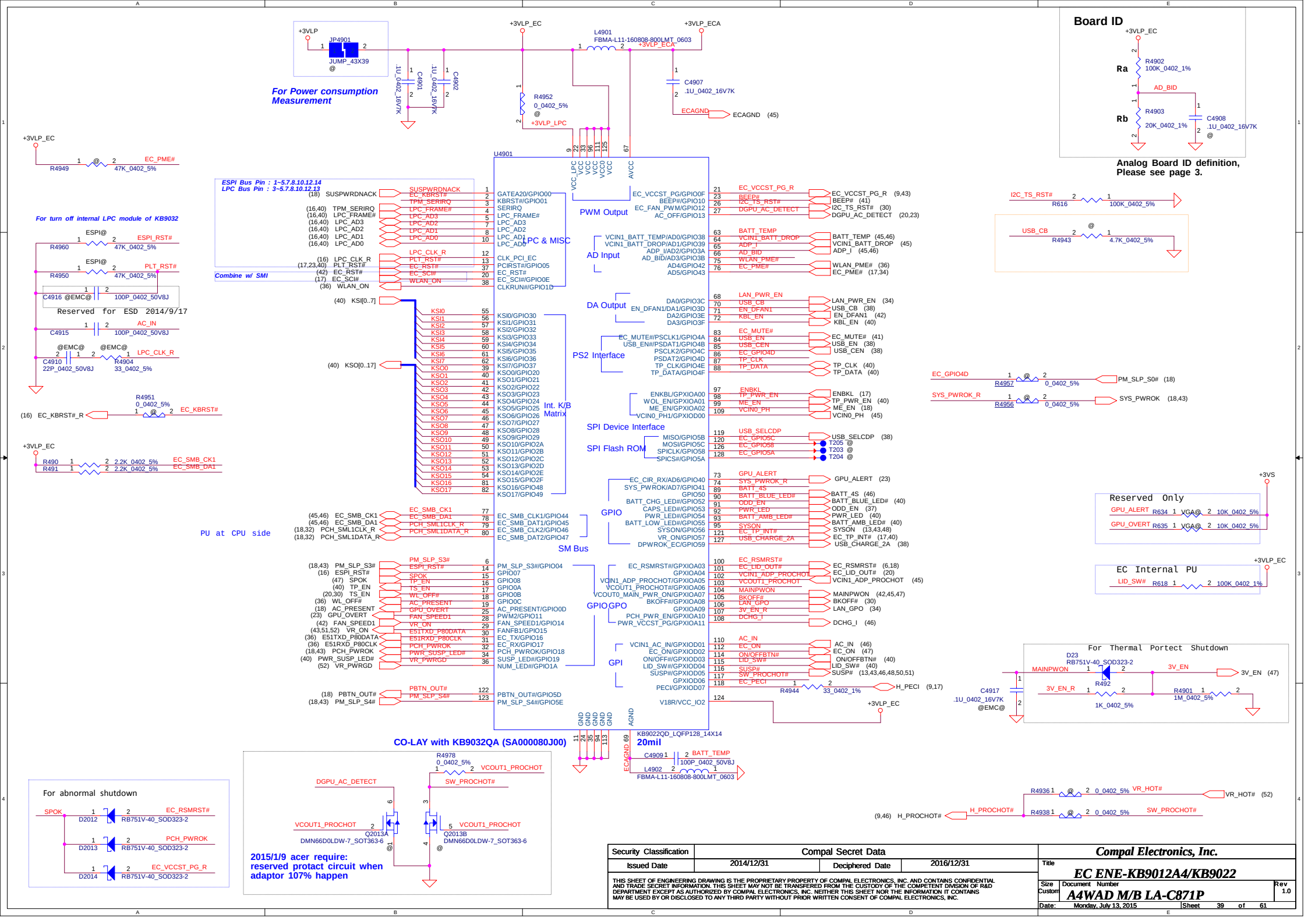
Board ID
Analog Board ID definition, Please see page 3.
For Power consumption Measurement
For turn off internal LPC module of KB9032
Reserved for ESD 2014/9/17
ESPI Bus Pin : 1~5.7.8.10.12.14
LPC Bus Pin : 3~5.7.8.10.12.13
Combine w/ SMI
U4901
KB9022QD_LQFP128_14X14
20mil
CO-LAY with KB9032QA (SA000080J00)
PWM Output
LPC & MISC
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
PU at CPU side
Reserved Only
EC Internal PU
For Thermal Portect Shutdown
For abnormal shutdown
2015/1/9 acer require:
reserved protact circuit when
adaptor 107% happen
Security Classification
Compal Secret Data
Issued Date
2014/12/31
Deciphered Date
2016/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
EC ENE-KB9012A4/KB9022
Size Custom
Document Number
A4WAD M/B LA-C871P
Rev 1.0
Date: Monday, July 13, 2015
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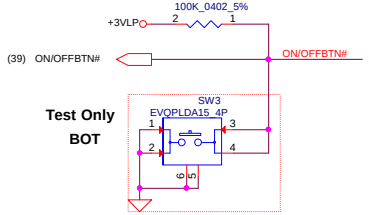
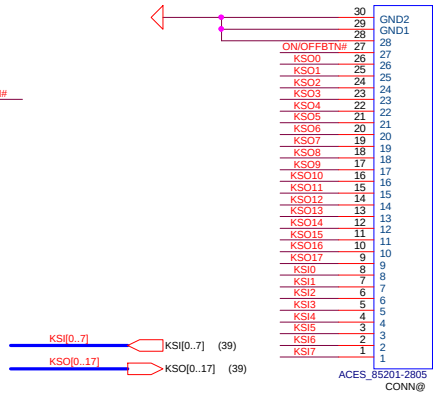
KB Conn.

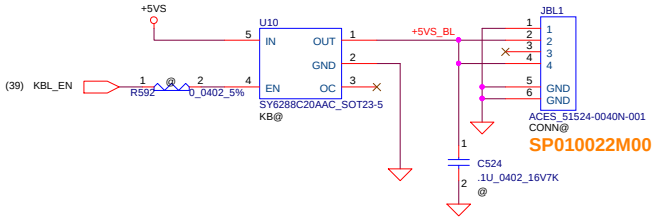
ON/OFF BTN





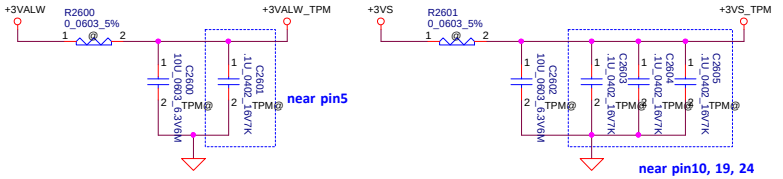
SP01000GO00

KB BackLight Conn. Reserve

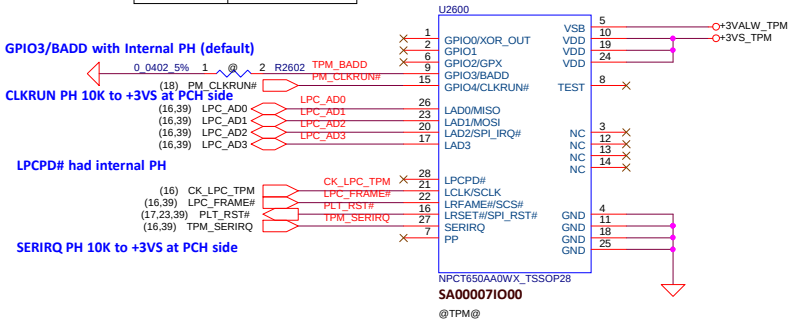


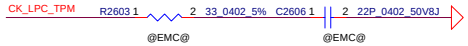
SP010022M00

TPM Board for 2015

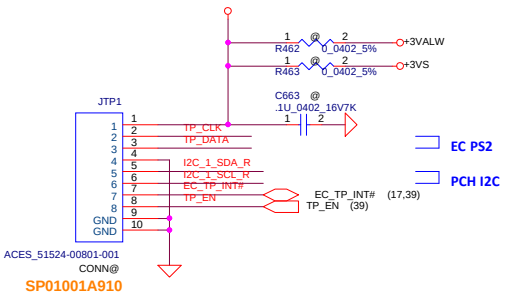


BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh

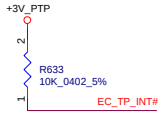


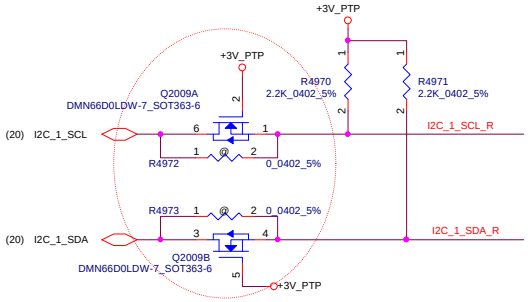


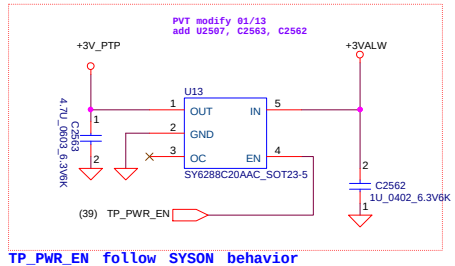
TP/B Conn.



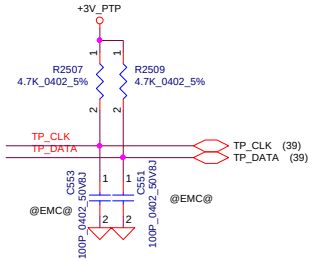
SP01001A910





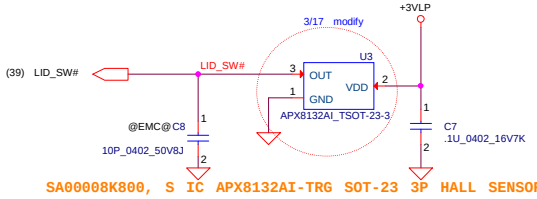


TP_PWR_EN follow SYSON behavior



Lid Switch

(Hall Effect Switch)



SA00008K800, S IC APX8132AI-TRG SOT-23 3P HALL SENSOR

LED

Dual Amber+Blue

LTST-S115TBKF-CA (SC50000C500)

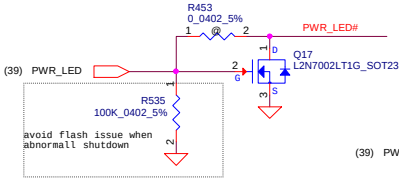
Vf @ 5 mA :

UD5: 1.7 ~ 2.3V
(3.3-1.7)/300=5.71 mA
(3.3-2.3)/300=3.57 mA
R min: 100 ohm
R max 700 ohm

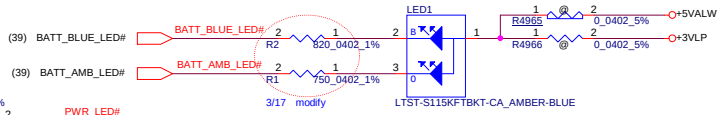
CB5: 2.65~3.05V
(3.3-2.65)/50=13.00 mA
(3.3-3.05)/100=5.0 mA
R min: 50 ohm
R max:475 ohm

100 1% :SD034100080
150 1% :SD034150080
301 1% :SD034301080
680 1% :SD034680080

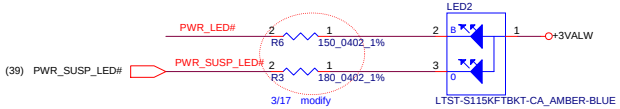
120 5% :SD028120080
560 5% :SD028560080
200 5% :SD028200080



Battery LED



Power LED



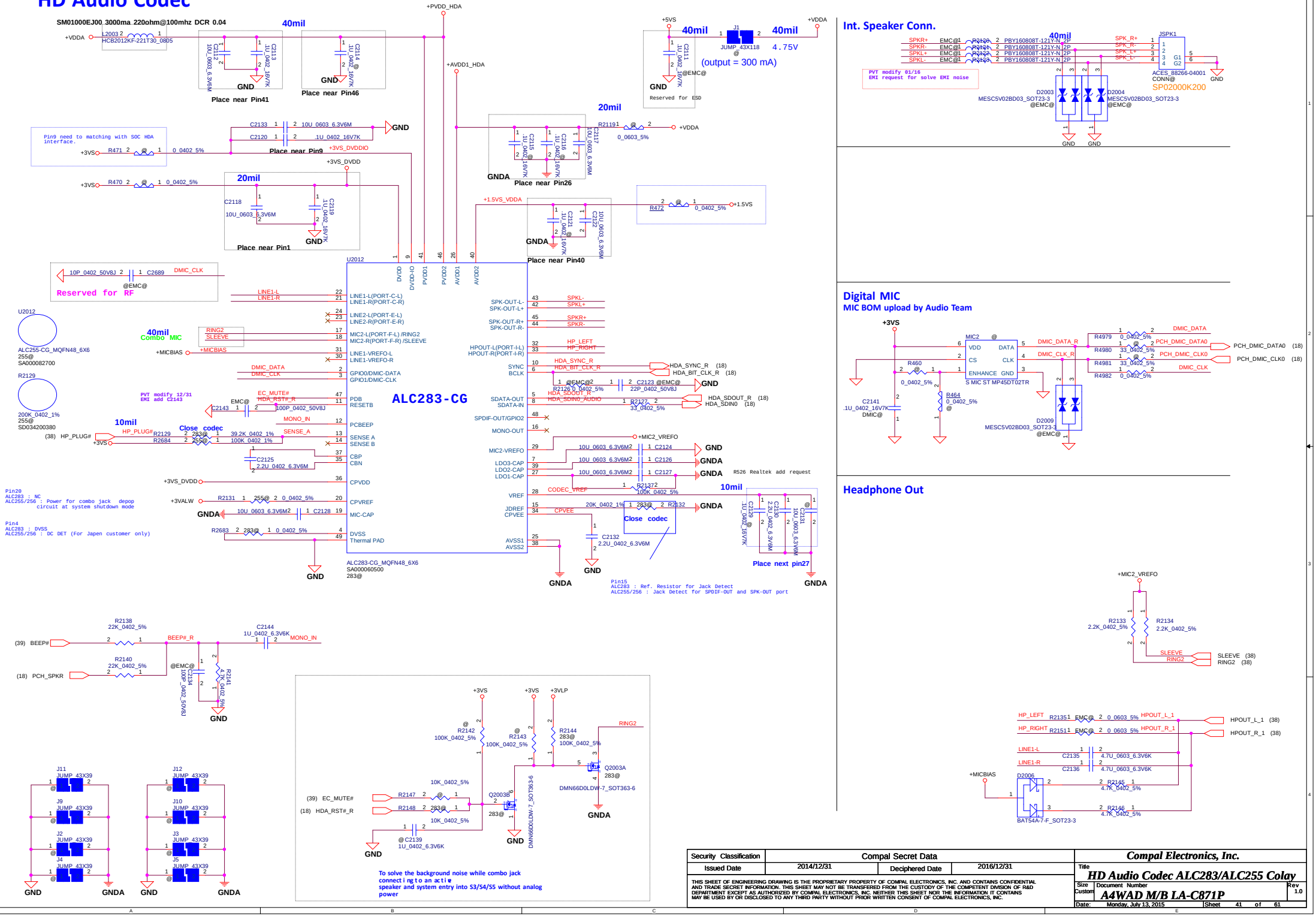
Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: KB & TP & TPM Connector & LED

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0
Date: Monday, July 13, 2015	Sheet 40 of 61	

HD Audio Codec



Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: HD Audio Codec ALC283/ALC255 Colay

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

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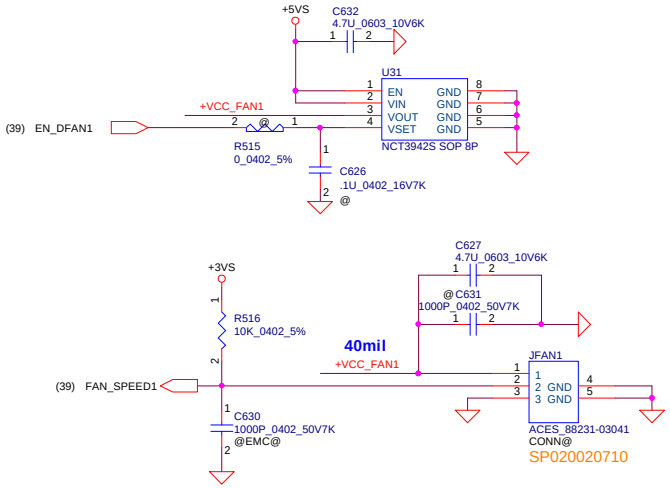
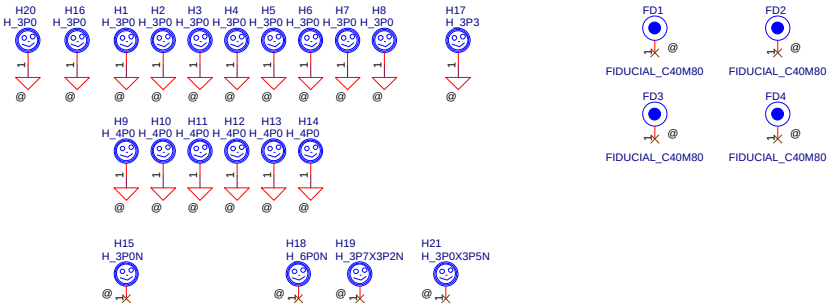
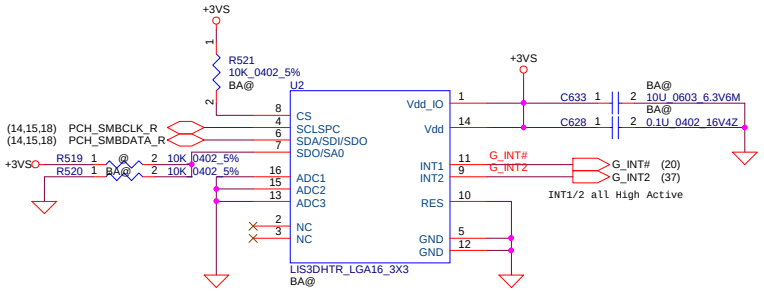
FAN1 Conn



Screw Hole

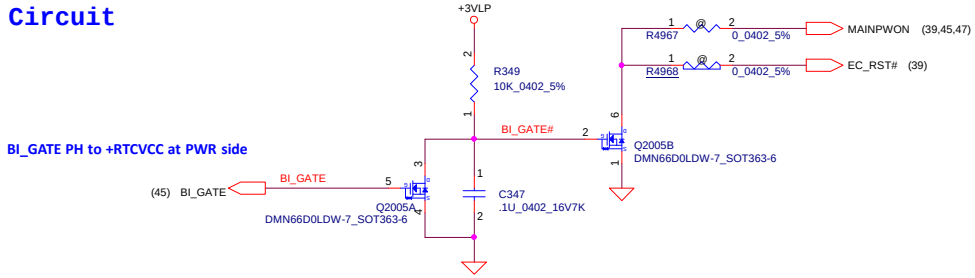


G-Sensor reserved for BA serial



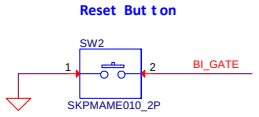
LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

Reset Circuit

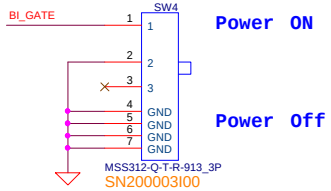


Debug SW

Reset Button

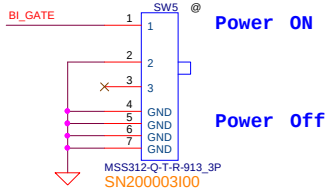


BI SW



Place TOP Side

BI SW



Place BOT Side
Reserved for memory door only

Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: FAN & Screw Hole & G-Sensor

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

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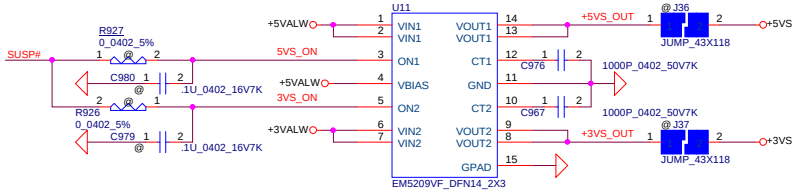
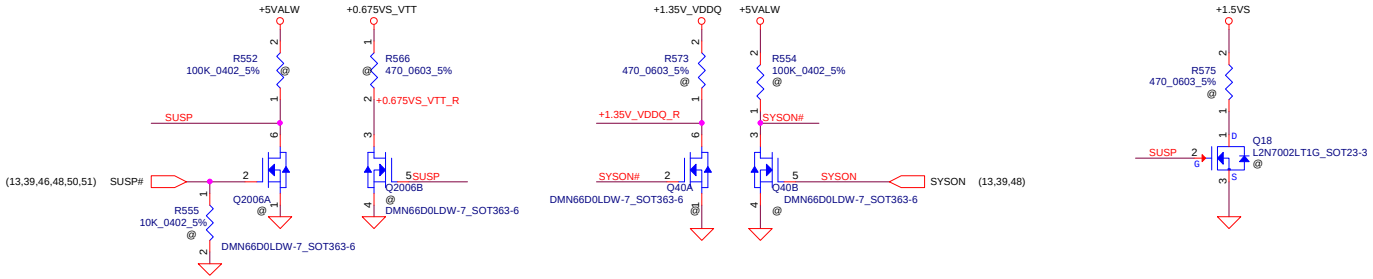
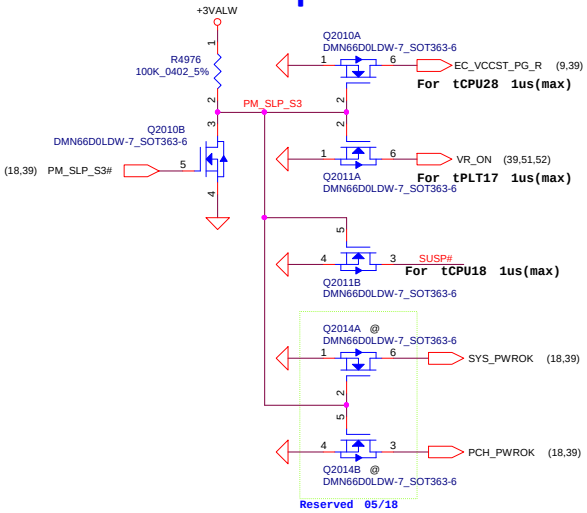
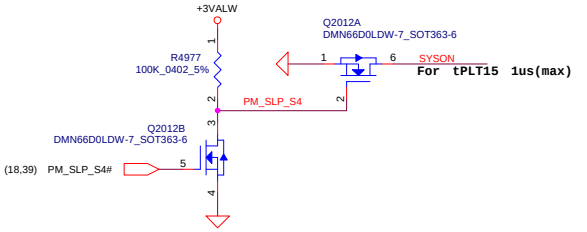
DC & VGA Interface



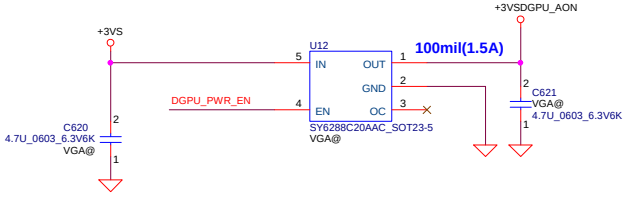


For Power Of f Sequence

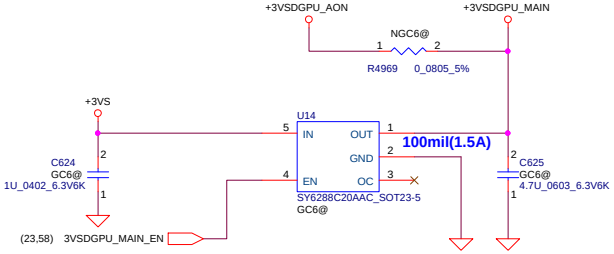




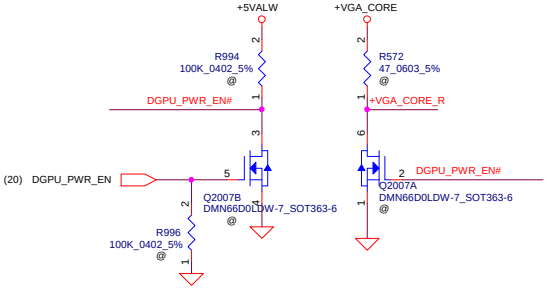
+3VS to +3VSDGPU_AON for GPU

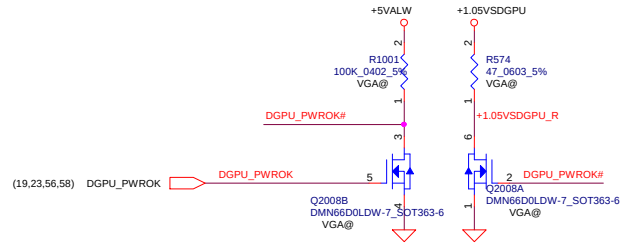


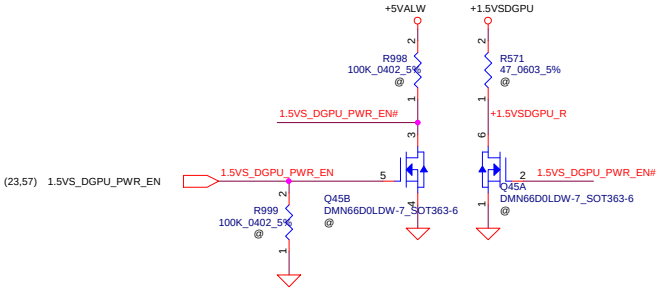
+3VS to +3VSDGPU_MAIN for GC6-2.0



3VSDGPU_MAIN_EN From GPU







Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0
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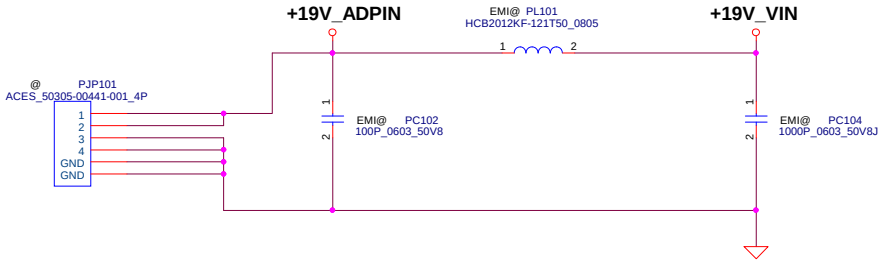

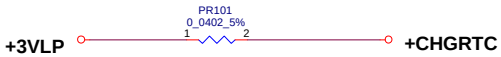

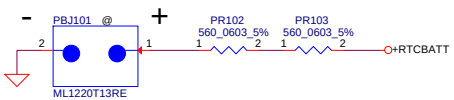

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

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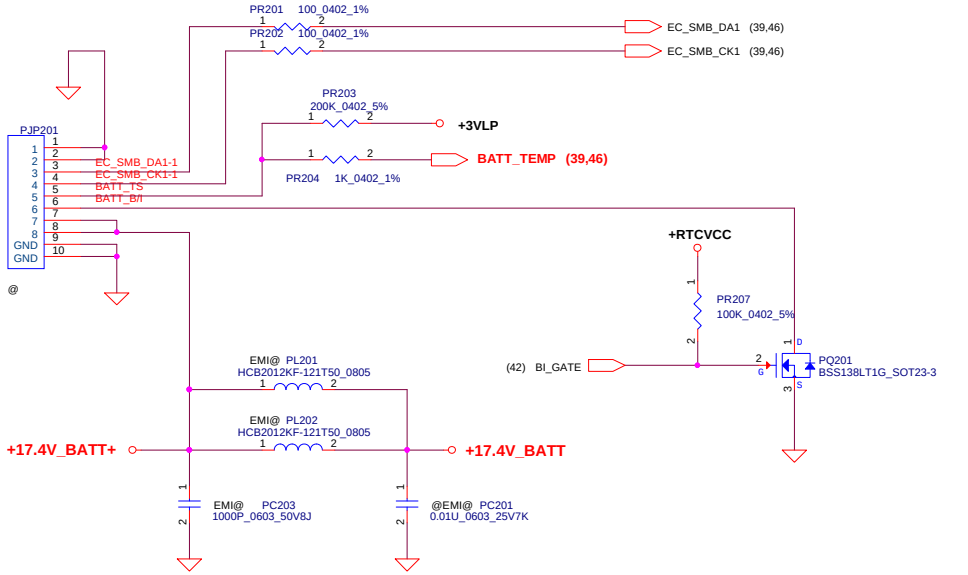
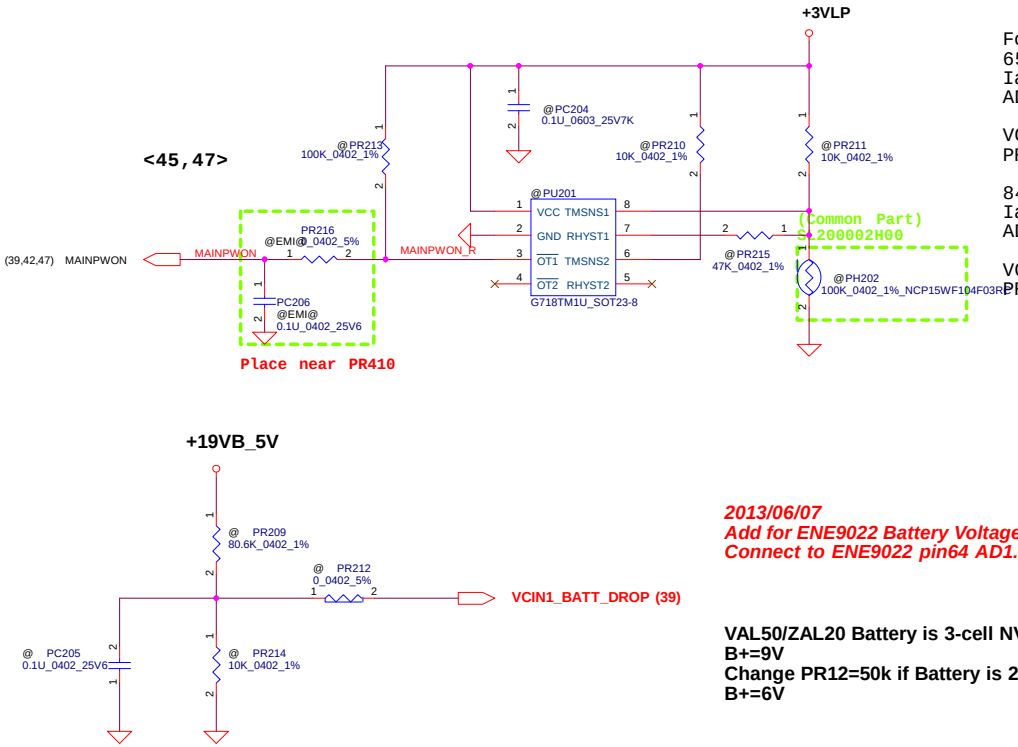


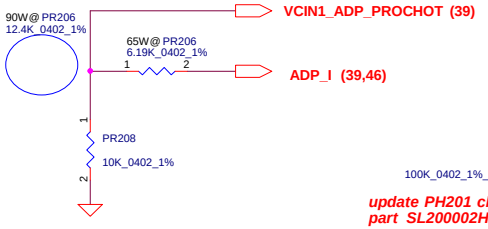


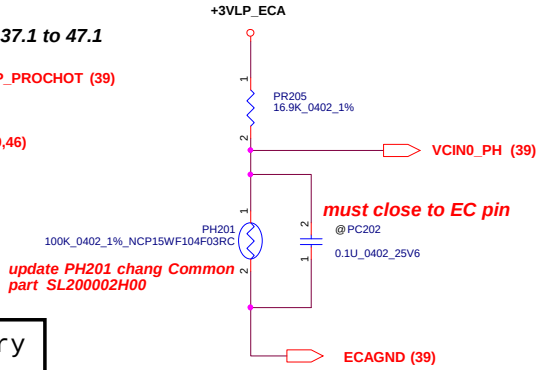
2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50k if Battery is 2-cell NVDC design
B+=6V

PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

2013/07/23
change PC5 and PC6 function field from 37.1 to 47.1





For KB9022 sense 20mΩ	Active	Recovery
65W PR206 6.19K ohm	84.5W,0.54V	65W,0.42V
90W PR206 12.4K ohm	117W,0.54V	90W,0.42V

For 65W adapter===>action 84.5W, recovery 65W
65W:
Iada=0~3.42A (65W/19v=3.42A)
ADP_I=20*Iada*Rsense
=20*3.42*0.01=0.6842V
VCIN1_PROCHOT=0.6842*10/(10+x)=0.42V
PR206=x=6.291k ohm

84.5W:
Iada=0~4.447A (84.5W/19v=4.447A)
ADP_I=20*Iada*Rsense
=20*4.447*0.01=0.8895V
VCIN1_PROCHOT=0.8895*10/(10+x)=0.55V
PR206=x=6.17k ohm

For 90W adapter===>action 117W, recovery 90W
90W:
Iada=0~4.737A (90W/19v=4.737A)
ADP_I=20*Iada*Rsense
=20*4.737*0.01=0.9474V
VCIN1_PROCHOT=0.9474*10/(10+x)=0.42V
PR206=x=12.56k ohm

117W:
Iada=0~6.158A (117W/19v=6.158A)
ADP_I=20*Iada*Rsense
=20*6.158*0.01=1.232V
VCIN1_PROCHOT=1.232*10/(10+x)=0.55V
PR206=x=12.39k ohm

Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: A4WAD M/B LA-C871P | Rev: 1.0

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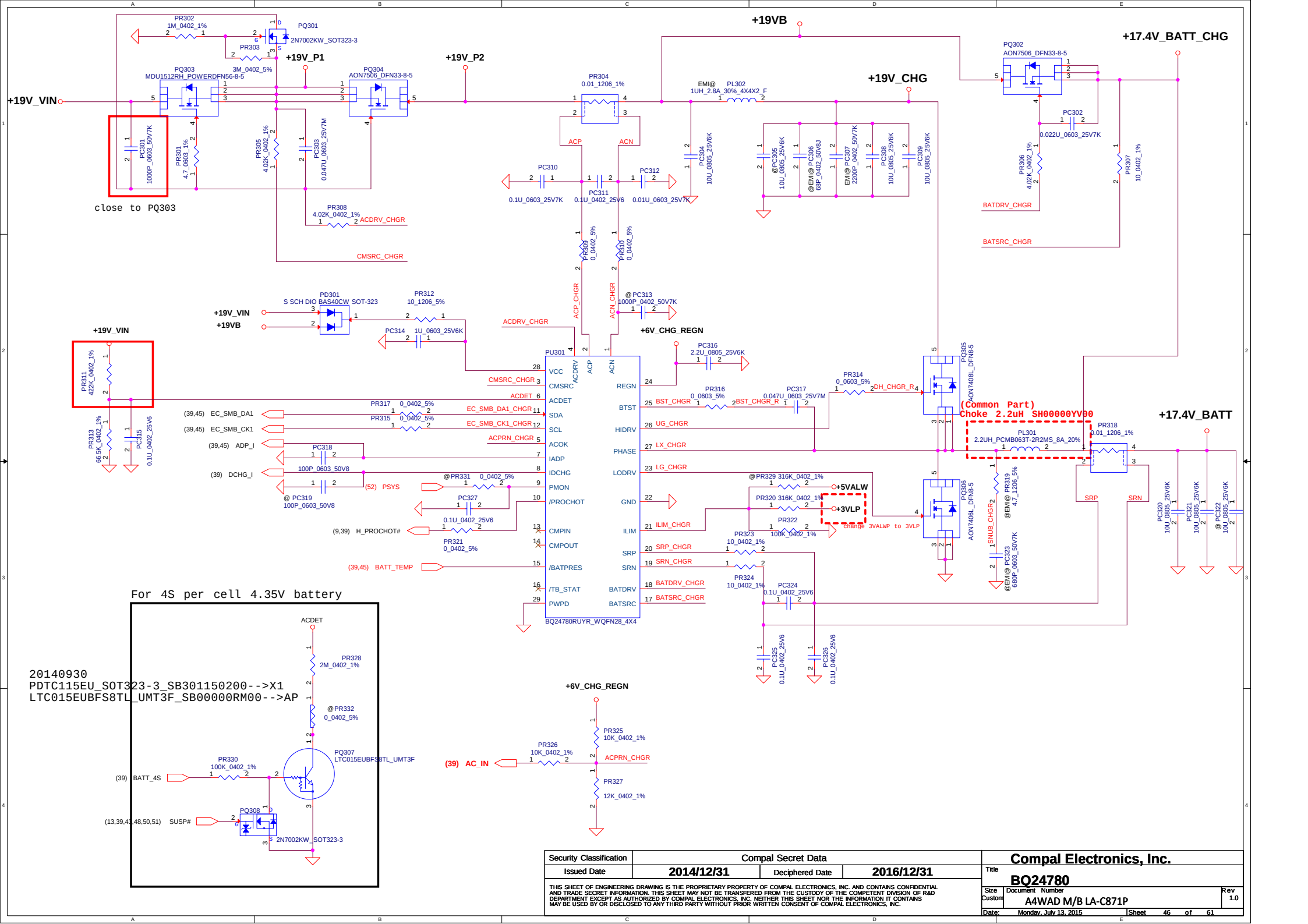
+19V_VIN
+19V_P1
+19V_P2
+19VB
+19V_CHG
+17.4V_BATT_CHG
+17.4V_BATT
close to PQ303
PU301
BQ24780RUYR_WQFN28_4X4
+6V_CHG_REGN
(Common Part)
Choke 2.2uH_SH00000YV00
For 4S per cell 4.35V battery
20140930
PDTC115EU_SOT323-3_SB301150200-->X1
LTC015EUBFS8TL_UMT3F_SB00000RM00-->AP
Compal Secret Data
2014/12/31
2016/12/31
Compal Electronics, Inc.
BQ24780
A4WAD M/B LA-C871P
Monday, July 13, 2015
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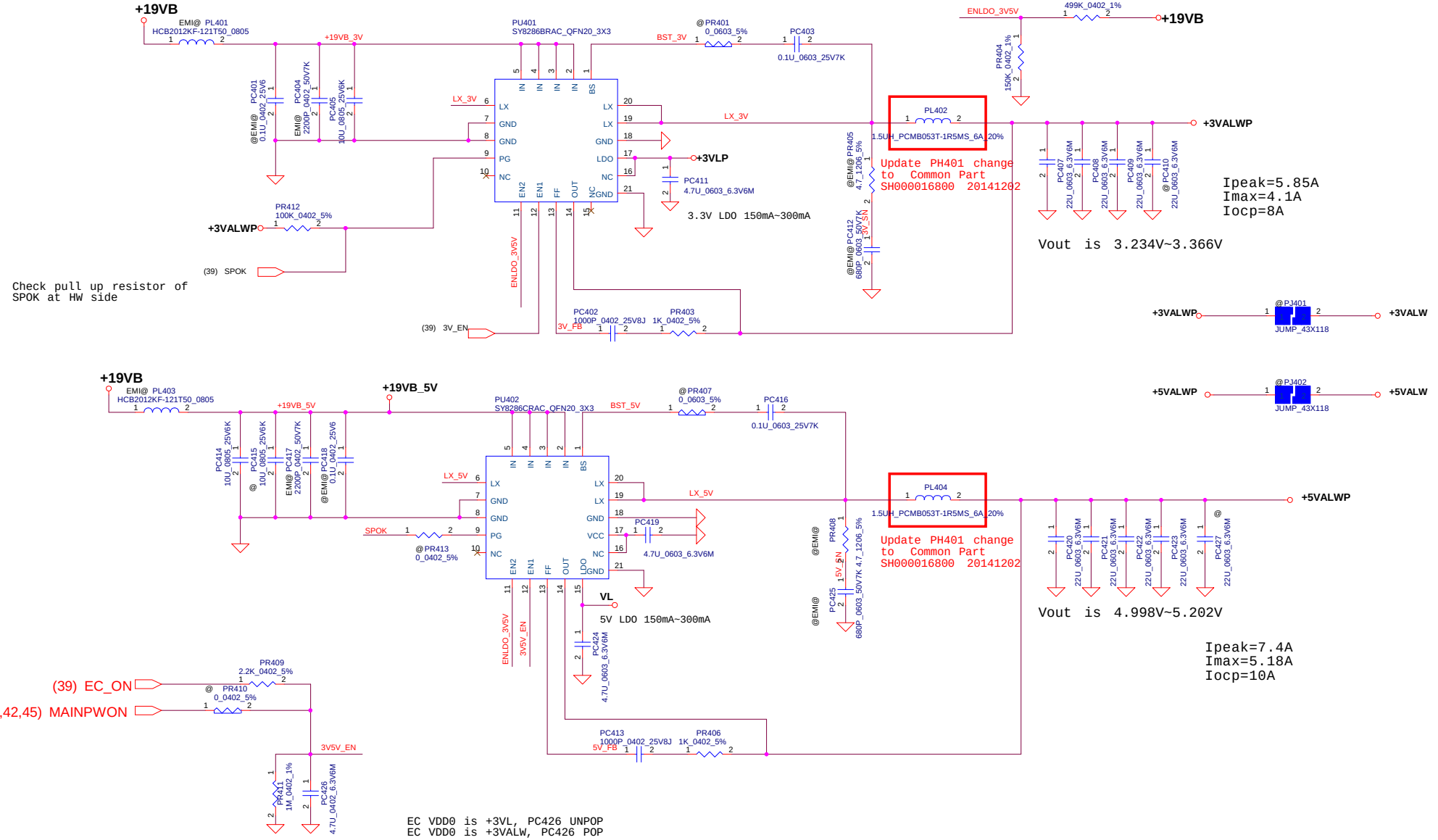
Module model information

SY8208B_V2.mdd
SY8208C_V2.mdd



Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: PWR-3.3VALWP/5VALWP

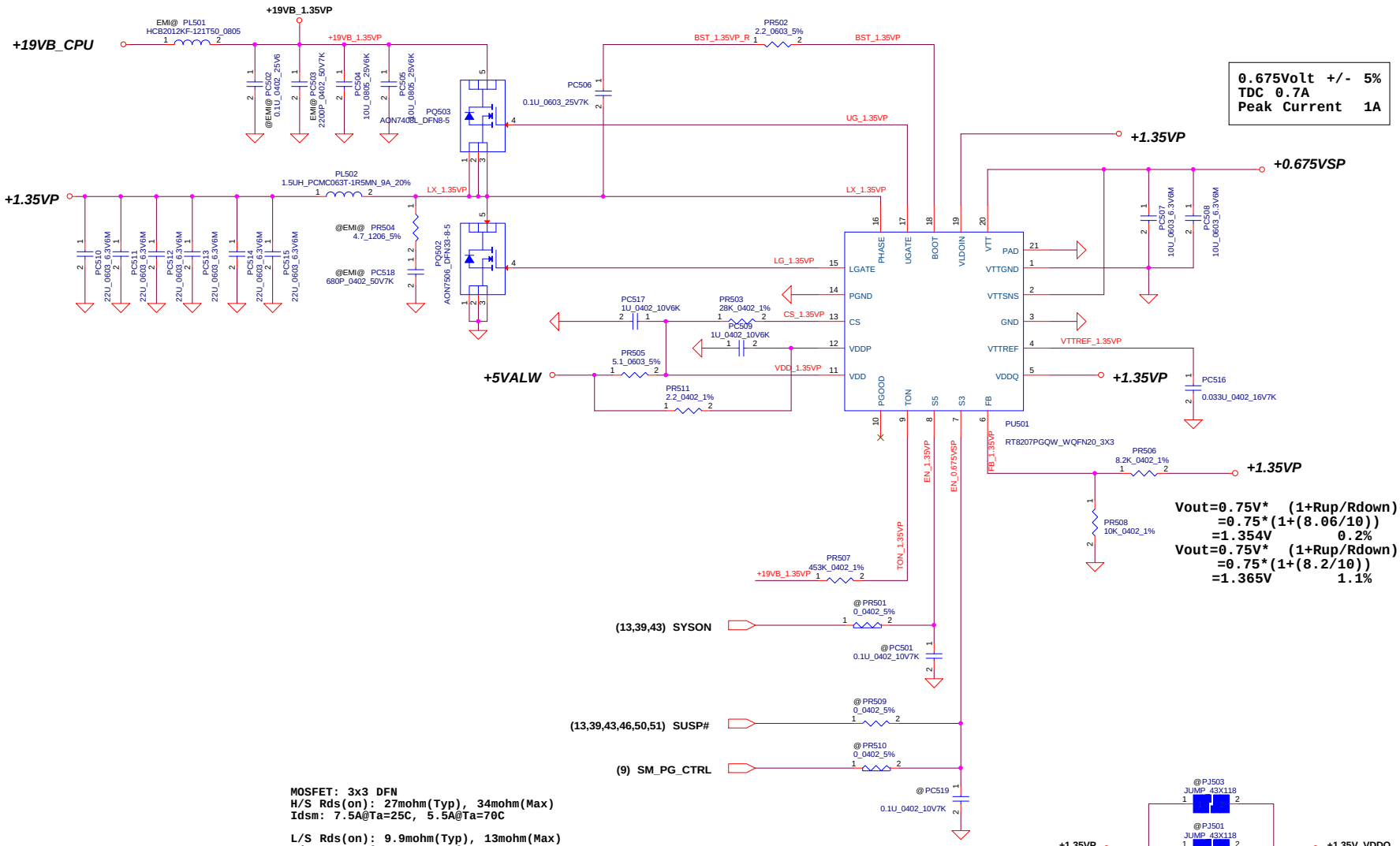
Size: Custom | Document Number: A4WAD M/B LA-C871P | Rev: 1.0

Date: Monday, July 13, 2015 | Sheet 47 of 61

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.



0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

Vout=0.75V* (1+Rup/Rdown)
=0.75*(1+(8.06/10))
=1.354V 0.2%
Vout=0.75V* (1+Rup/Rdown)
=0.75*(1+(8.2/10))
=1.365V 1.1%

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
VFB=0.75V, Vout=1.3545V
MOSFET footprint: SIS412DN

Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: RT8207P

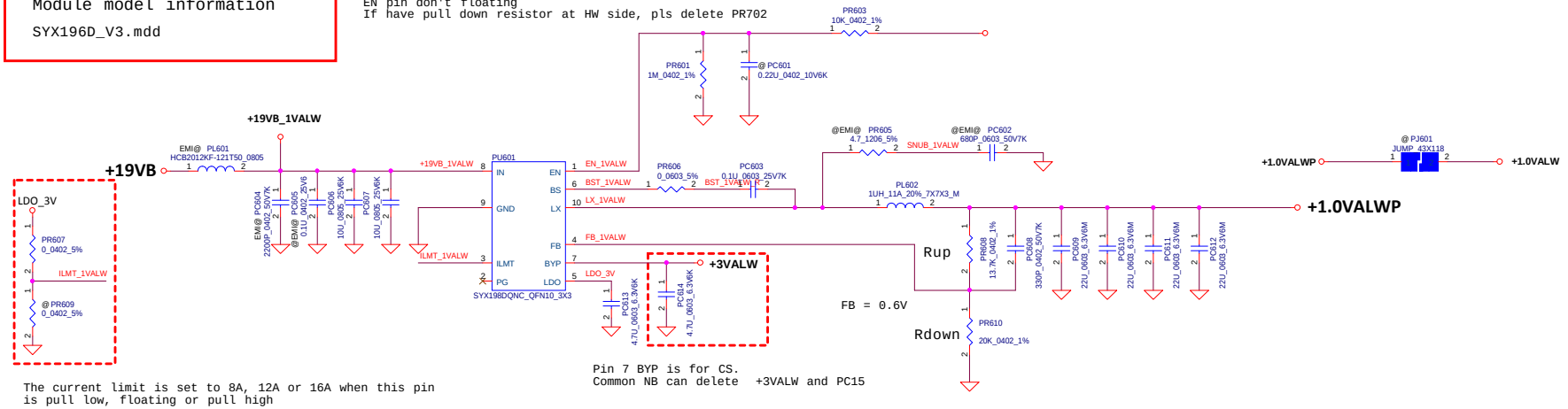
Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 Sheet 48 of 61

Module model information

SYX196D_V3.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

Vout=0.6V* (1+Rup/Rdown)
Vout=0.6V* (1+13.7k/20k)
Vout=1.011V

Function Field :
VCCEDPIO : IC-35.21 , others - 35.22
VCCEDRAM : IC-35.25 , others - 35.26

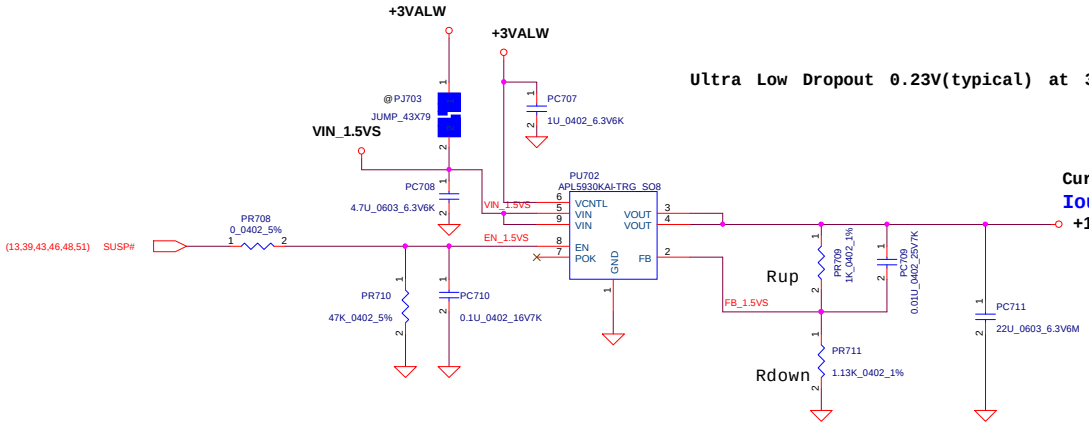
Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: VCCP

Size	Document Number	Rev
C	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 | Sheet 49 of 61



Ultra Low Dropout 0.23V(typical) at 3A Output Current

Current limit = 4.7A(min)

Iout=0.9A

Vout=0.8V* (1+Rup/Rdown)

Vout=0.8V* 1.884 = 1.507V

Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **SY8032**

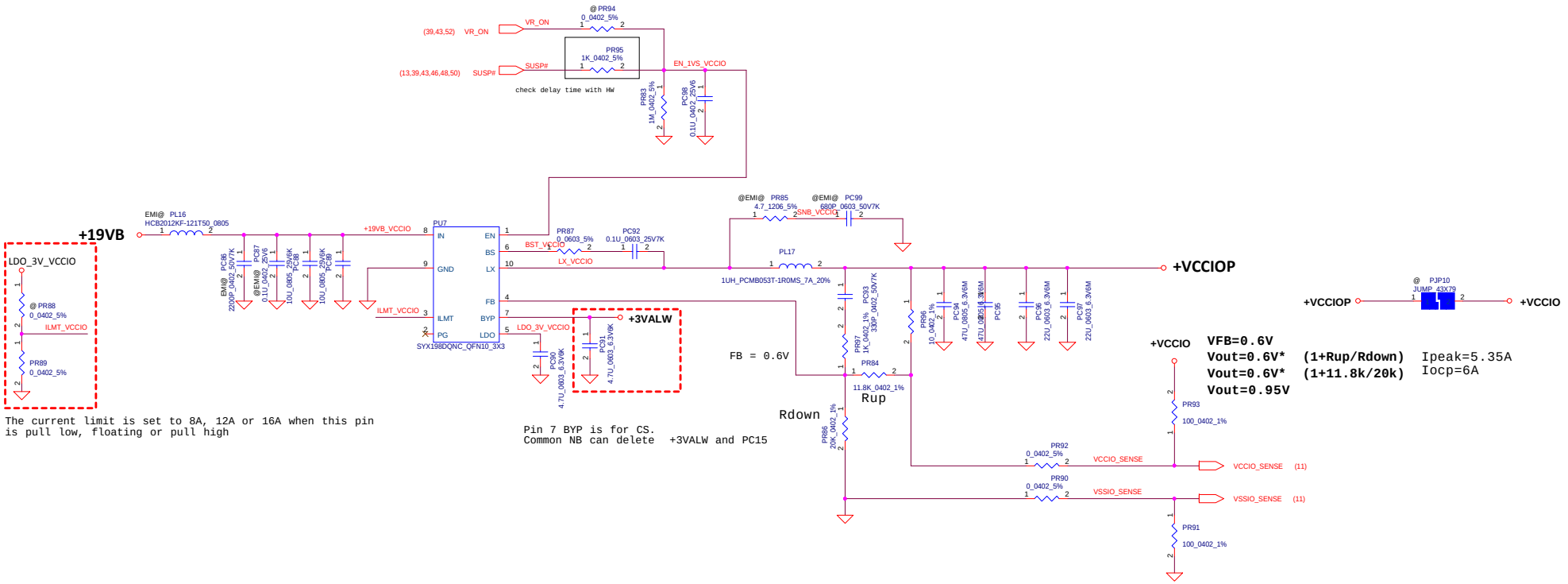
Size	Document Number	Rev
Custom	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 Sheet 50 of 61

Module model information

SYX196D_V3.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

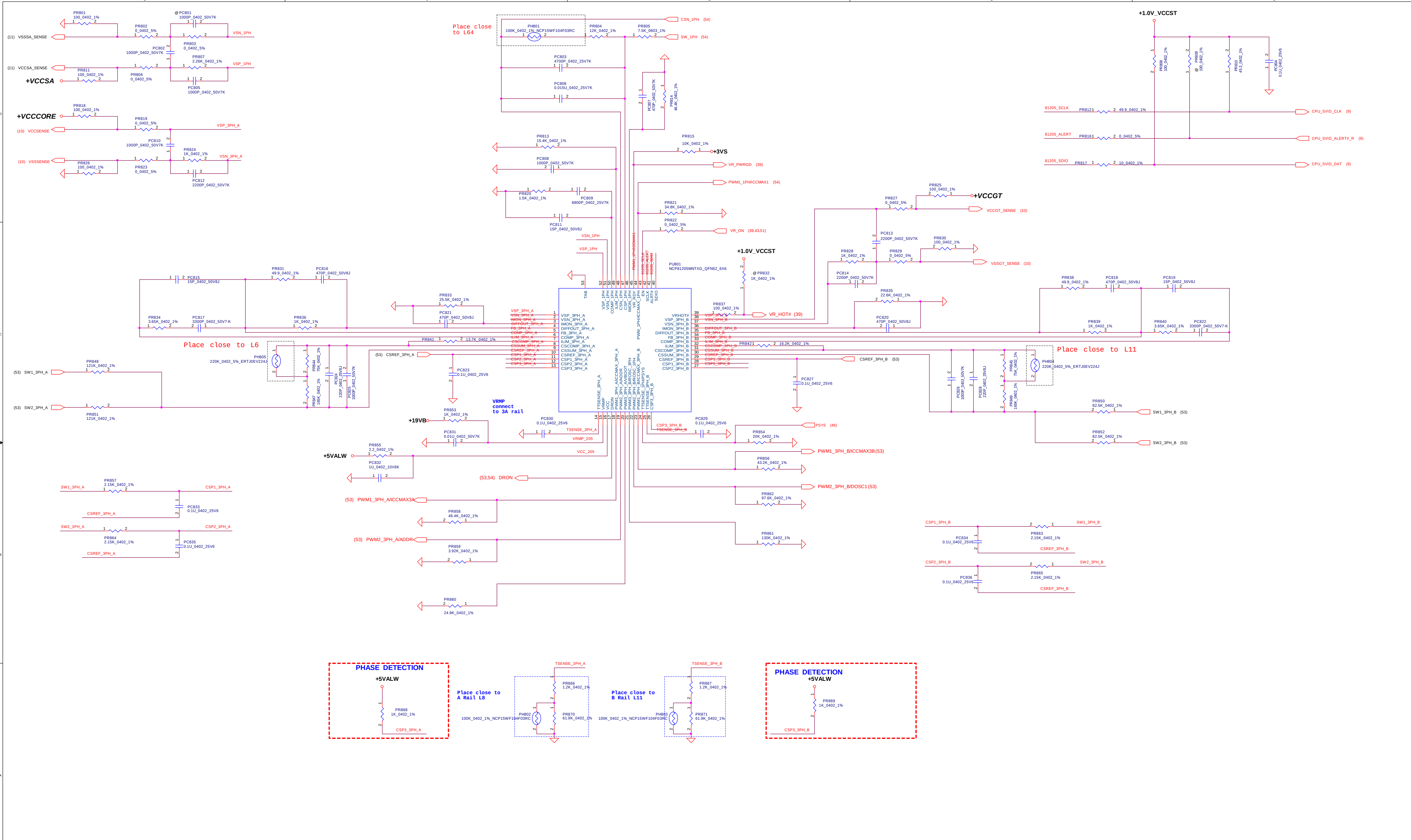
Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: TPS62134

Size	Document Number	Rev
C	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 Sheet 51 of 61



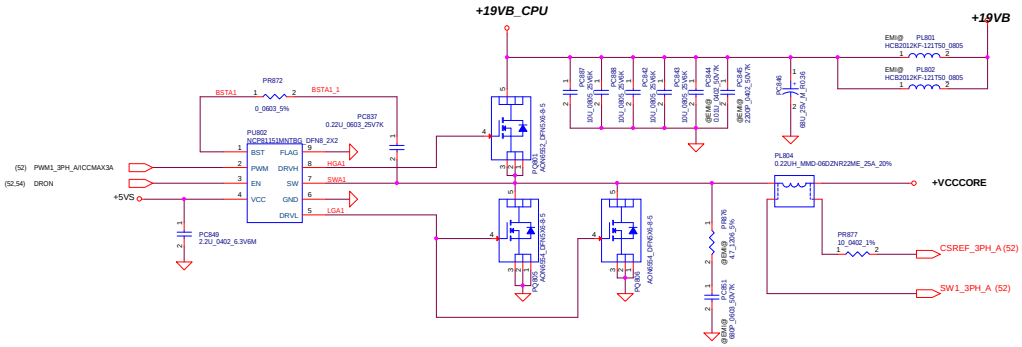
Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

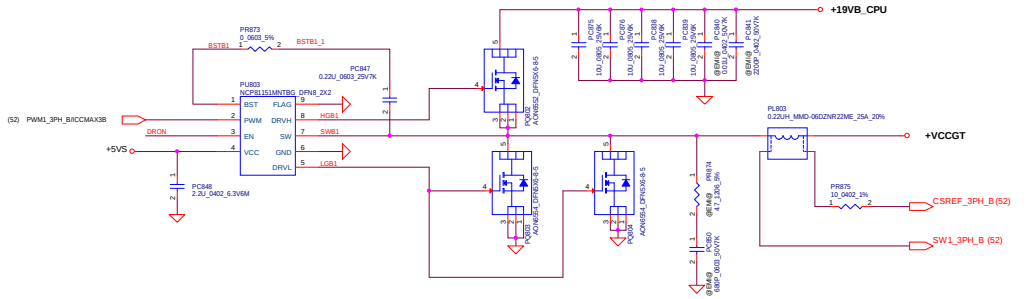
Compal Electronics, Inc.

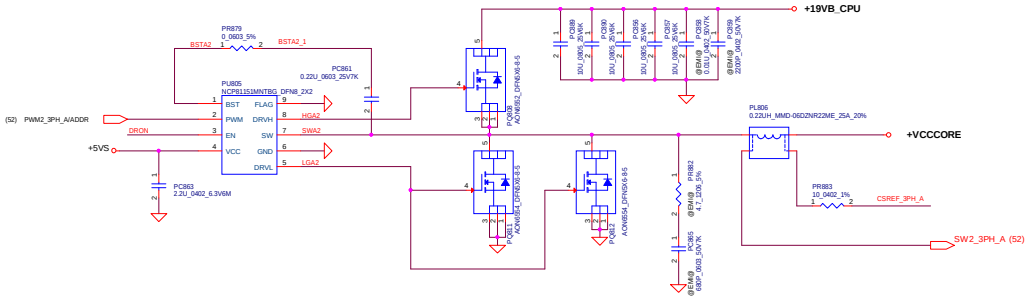
Title: **TBD**

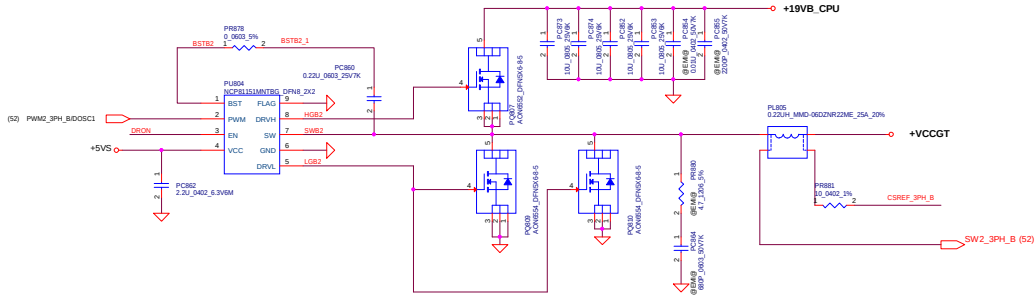
Size	Document Number	Rev
D	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 — Sheet 52 of 61









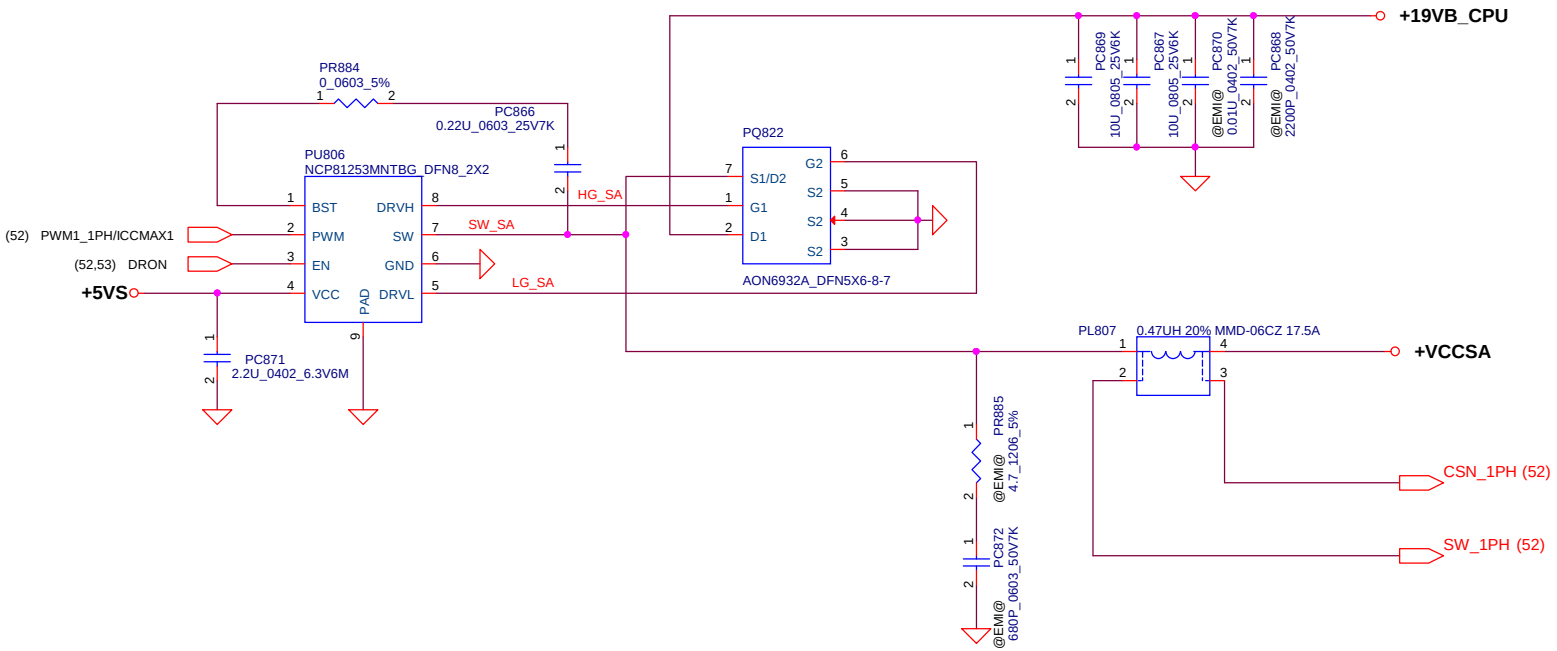
+VCCCORE
TDC 64A
Peak Current 60A
OCP current 76A
Load line mV/A
FSW=400kHz
DCR 0.98mohm +/-5%

	TYP	MAX
H/S Rds(on)	:6.7mohm ,	8.5mohm
L/S Rds(on)	:3mohm ,	3.7mohm

+VCCGT
TDC 49A
Peak Current 55A
OCP current 61A
Load line mV/A
FSW=400kHz
DCR 0.98mohm +/-5%

	TYP	MAX
H/S Rds(on)	:6.7mohm ,	8.5mohm
L/S Rds(on)	:3mohm ,	3.7mohm

Compal Electronics, Inc.			
Title: TBD			
Size: Custom	Document Number: A4WAD M/B LA-C871P		Rev: 1.0
Date: Monday, July 13, 2015	Sheet: 53	of: 61	



Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **TBD**

Size	Document Number	Rev
B	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 Sheet 54 of 61

Total VCORE Output Capacitor:
2 * 330uF+30 * 22uF_0603+63 * 1uF_0201

+VCCCORE

+VCCCORE

change SGA20331E10 to SGA00009S00 (comm part)

Total VCORE Output Capacitor:
3 * 330uF+38 * 22uF_0603+68 * 1uF_0201

+VCCGT

+VCCGT

change SGA20331E10 to SGA00009S00 (comm part)

+VCCSA

Total VCORE Output Capacitor:
1 * 330uF+8 * 22uF_0603+3 * 1uF_0201

+VCCSA

change SGA20331E10 to SGA00009S00 (comm part)

Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

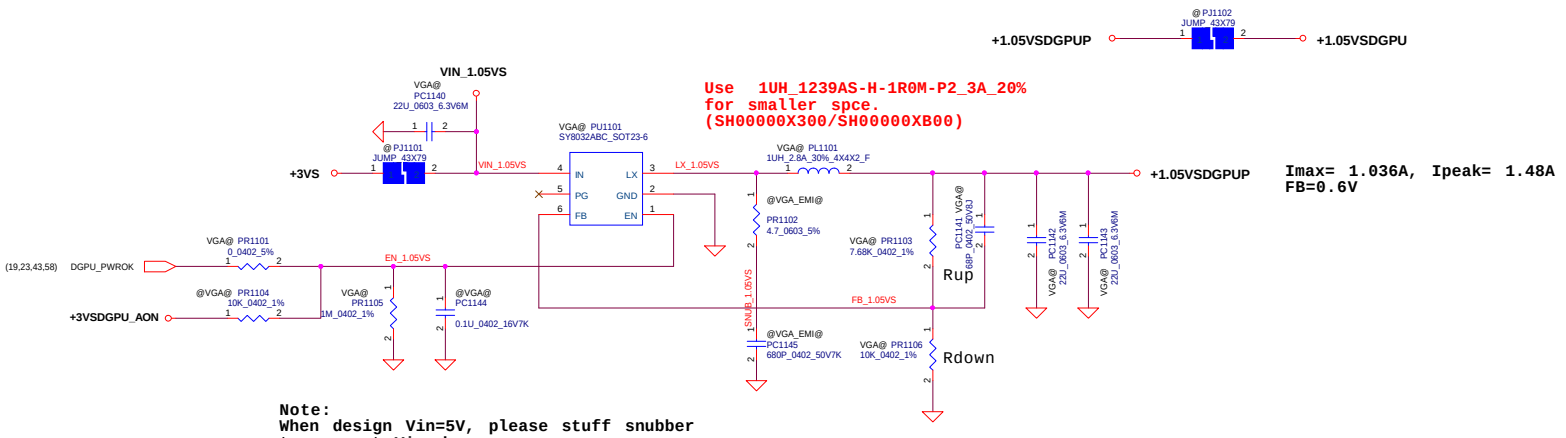
Title: TBD

Size: Custom | Document Number: A4WAD M/B LA-C871P | Rev: 1.0

Date: Monday, July 13, 2015 | Sheet: 55 of 61

Module model information

SY8032_V2.mdd



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)
=>0.6V*(1+(7.68/10)=1.061 (1.01%)
=>0.6V*(1+(7.87/10)=1.072 (2.1%)

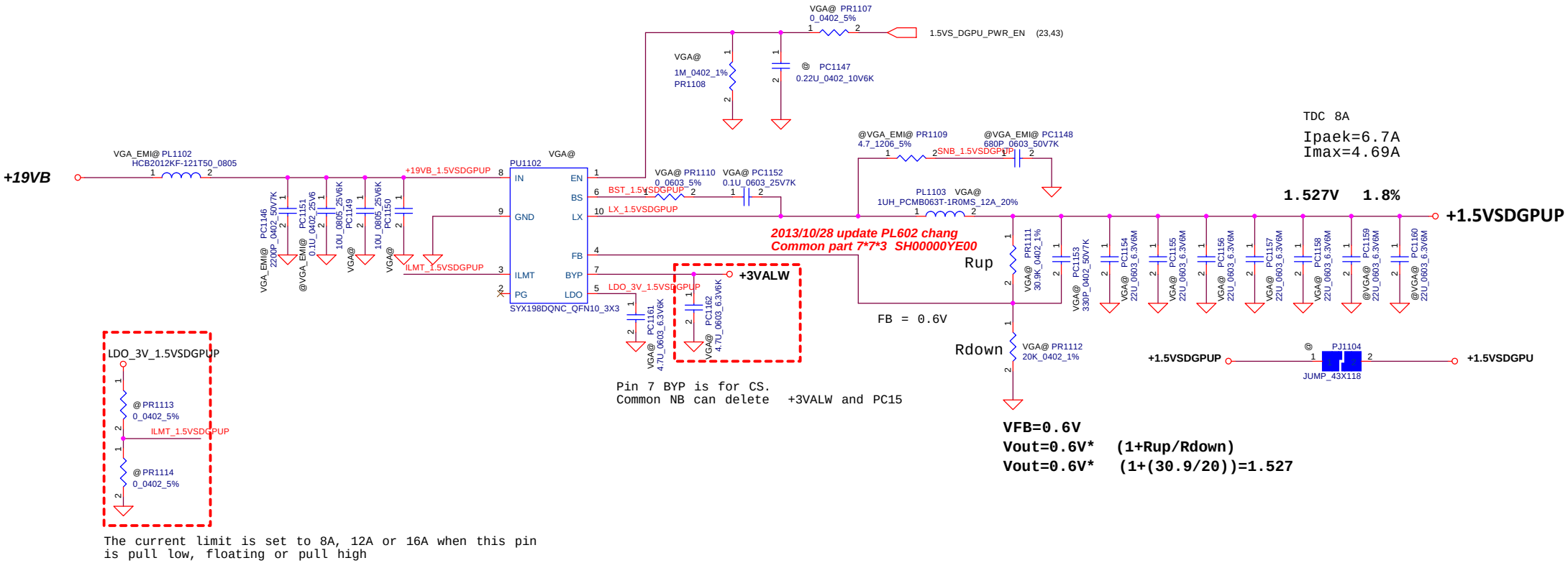
Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **SY8032**

Size	Document Number	Rev
C	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 Sheet 56 of 61



Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: 1.5VSDGPUP

Size	Document Number	Rev
A3	A4WAD M/B LA-C871P	1.0

Date: Monday, July 13, 2015 Sheet 57 of 61

PSI :
1 phase with DEM 0V to 0.8V
1 phase with CCM 1.2V to 1.8V
2 phase with CCM 2.4V to 5.5V

EN High Threshold = 1.6V

unmount PRV5 for 2 phase select

PU1201
VGA@
RT8812AGQW_WQFN20_3X3

PR1214: OCP setting
from 50A to 25A

H/L side Rds(on): 12.2mohm(Typ), 15mohm(Max)
Idsm: 11A@Ta=25C, 14A@Ta=70C

CHOKE:0.36uH, DCR 1.4m ohm, L/2 over 36A

FSW = 245.55KHz
Iripple = 12.74A
OCP = 50A
OVP=Vout*(145%~155%)

+VGA_CORE Under GPU Core GB4-128 package

+VGA_CORE Near GPU Core

Security Classification	Compal Secret Data		
Issued Date	2014/12/31	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: NVIDIA VGA_CORE

Size: Cust | Document Number: A4WAD M/B LA-C871P | Rev: 1.0

Date: Monday, July 13, 2015 | Sheet 58 of 61

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	ACIN can't boot	ACDET pin below 2.4V. It must above 2.4V.	02	46	1. Change PR313 59K to 66.5K	4/6	DVT
02	X1 Code	X1 code changed to AP code.	02	52	1. Change PC824,PC828 S CER CAP 220P 25V J NPO 0402	4/6	DVT
03	Design Change.	CPU CORE transient noise meets spec.	02	55	1. Delete PC1119,PC997 S POLY C 330U 2V Y ESR9M H1.9	4/6	DVT
04	Design Change.	For EMI Test	02	46	1. Add PL302 S COIL 1UH +-30% 2.8A 4X4X2 FERRITE	4/6	DVT
05	The sequence of VGA CORE is't correct	For VGA CORE Sequence	02	58	1.Change PR1202 10K ohm to 20k ohm 2. Change PR1206 0 ohm to 20k ohm 3. Add PC1209 S CER CAP .1U 16V K X7R 0402	4/6	DVT
06	Design Change.	For VGA ILIMIT	02	58	1. Change PR1214 11.8K to 13K	4/6	DVT
07	Design Change.	For meeting CPU Thermal criteria	02	52	1. Change PR866,PR867 909ohm to 1.2Kohm	4/6	DVT
08	Design Change.	For S5 mode, charger current charge	02	46	1.Add PR320 for power source 3VALWP to 3VLP. 2.Add PR239 for reserved 5VALWP	5/15	PVT
09	Design Change.	Changing VCCIO solution for power efficiency.	02	51	1. Change SY196D to SY198D	5/16	PVT
10	Design Change.	To decrease part count,no EMI concerned	02	47	1. Change PR401,PR407 to short pad	5/16	PVT
11	Design Change.	To decrease part count,no EMI concerned	02	53	1. Change PR1224,PR1201,PR1217,PR1219,PR1204 to short pad	5/16	PVT
12	Design Change.	Reserve for Intel solution	02	44	1. Change PR101 to 0 ohm	5/16	PVT
13	Design Change.	For meet DFB	02	46	1. Delete PJ301		
14	Design Change.		02	50			
15	Design Change.		02	45			
16	Design Change.		02	48			
17	Design Change.		02	50			

Version change list (P.I.R. List)

Item	Page	Title	Date		Solution Description	Phase	Rev.
1	6	CMC	3/17	Change XDP to CMC	Change JXDP1 CIS symbol to CMC CIS Symbol(JPCMC1) Rerout i ng RPC1, RPC2, RPC3, RC56 Del CC1,CC2,CC70,JXDP1,RC12,RC14, RC16,RC18,RC48,RC49,RC50,RC51, RC53,RC54,RC55,RC7,RC9,RPH10 Add JPCMC1,RC59	DVT	0.2
2	9,18,19	CPU,PCH	3/17	change XDP to CMC CONN, reserved test point	Add T3820,T3821,T3822,T3823	DVT	0.2
3	7	CPU	3/17	549401_549401_SKL_H_S_Plat_SMI_WP_Rev0_93	UC1.AU5 UC1.AR8 <DDR_ALERT#> Not used at DDR3L. Tied to GND.	DVT	0.2
4	17	PCH	3/17	Reserved path for TP_INT	Add RH148 0R @	DVT	0.2
5	17	SPI	3/17	546765_546765_2015WW09_Skylake_MOW_Rev_1_0	Change RH28 to @	DVT	0.2
6	31	HDMI	3/17	Reduce unuse part	Del R4962,R4963,R4975	DVT	0.2
7	34	LAN	3/17	Reserved path for +3V_LAN	Add R4984 @ 0_0805_5%	DVT	0.2
8	36	WLAN (M.2)	3/17	follow A4WAS (Reqruie from Acer) Separate M.2 pin32 and 46 for Intel WLAN 3165	Change "E51RXD_P80CLK_R" to JNGFF1.46	DVT	0.2
9	39	Board ID	3/17	Board ID change to DVT	Change R4903 from 0_0402_5% to 12K_0402_5%	DVT	0.2
10	40	LED	3/17	Follow A4WAD LED Light adjust report	change R1 to 750_0402_1% change R2 to 820_0402_1% change R3 to 180_0402_1% change R6 to 150_0402_1%	DVT	0.2
11	42	BI SW	3/17	Reserved for memory door on D-Cover, place BOT Side	Add SW5 @	DVT	0.2
12	9	PCH	3/20	follow PCH EDS Rev1.5 USB2_ID,USB_VBUSSENSE PD	Add RH149,RH150 1k_0402_5% to GND	DVT	0.2
13	39	EC	3/20	Reserved TPT PU RES	Del R4908,R4910	DVT	0.2
14	39	LID	3/30	EC doesn't internal PU	Change R618 to stuf f	DVT	0.2
15	20	G Sensor	4/1	Reserved	Reserved RH151 PD 100K @ to "G_INT#"	DVT	0.2
16	19	X'TAL	4/8	Change Common part	Change YH1 to S CRYSTAL 32.768KHZ CM7V-T1A9.0PF20PPM	DVT	0.2
17	19	X'TAL	4/8	Follow X'TAL test report	Change CH13 to 10p , CH14 to 8.2p	DVT	0.2
18	19	X'TAL	4/8	Follow X'TAL test report	Change CH11,CH12 to 15p	DVT	0.2
19	18	SMBUS	4/13	Follow INTEL PDG	Change RPH8,RPH9 to 2.2K_0804_8P4R_5%	DVT	0.2
20	41	PC BEEP	4/13	Colay PC_BEEP to EC	Change R2138 to stuf f	DVT	0.2
21	23	NV SMBus	4/13A	Follow INTEL PDG,already conf i r m wit h NVI D A	Change R2000,R2001 to 4.7K_0402_1%	DVT	0.2
22	21	PCH	5/18	Recommend to follow intel PDG decoupling requirement.	add CH54 1u_0402 for UH1.W15 "+3VALW_DSW" change UH1.V28 & AC17 connected to "+1.0VALW_MPHY"	PVT	0.3

Compal Electronics, Inc.

Title: PIR-HW1

Size: Custom | Document Number: A4WAD M/B LA-C871P | Rev: 1.0

Date: Monday, July 13, 2015 | Sheet 60 of 61

Version change list (P.I.R. List)

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
23	38	USB charger	5/18	EC control USB charger ic SELCDP	Add NET "USB_SELCDP" for EC control	PVT	0.3
24	16	PCH	5/18	546765_2015WW10_Skylake_MOW_Rev_1_0	change RH150 to 0R, let "USB2_ID" connect to GND change RH149 to 0R, let "USB2_VBUSSENSE" connect to GND	PVT	0.3
25	38	EMC request	5/19	EMC request	Add C4918 33PF_0402 for EMC@	PVT	0.3
26	31,32	HPD	5/19	INTEL request	Change R4985 to STUFF Change R2530 to STUFF	PVT	0.3
27	39	brard ID	5/19	Board ID change to PVT	change R4903 to 15K	PVT	0.3
28	39	brard ID	7/9	Board ID change to PreMP	change R4093 to 20K	Pre-MP	1.0

Compal Electronics, Inc.

Title: PIR-HW2

Size: Custom | Document Number: A4WAD M/B LA-C871P | Rev: 1.0

Date: Monday, July 13, 2015 | Sheet 61 of 61