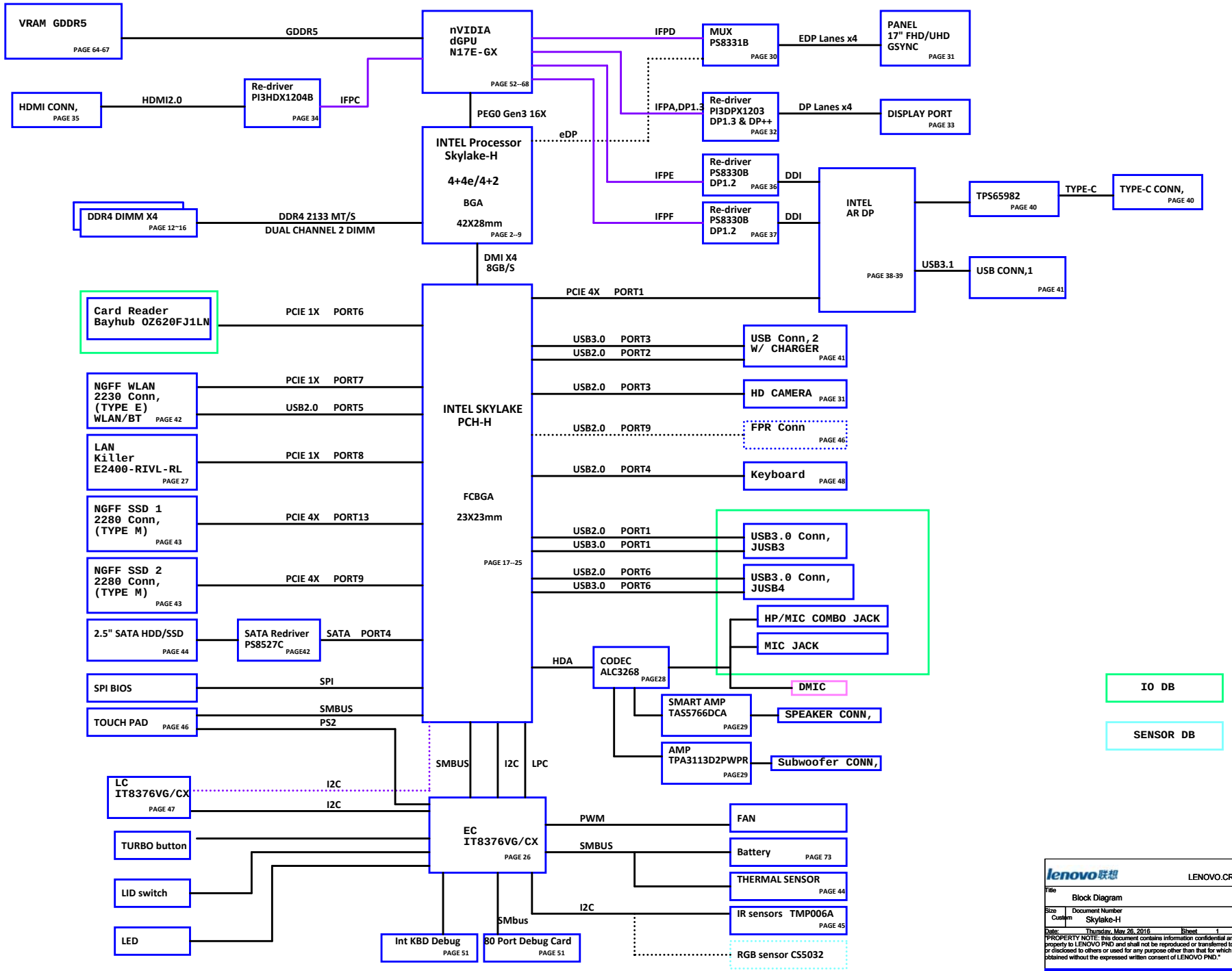
Schematic Block Diagram

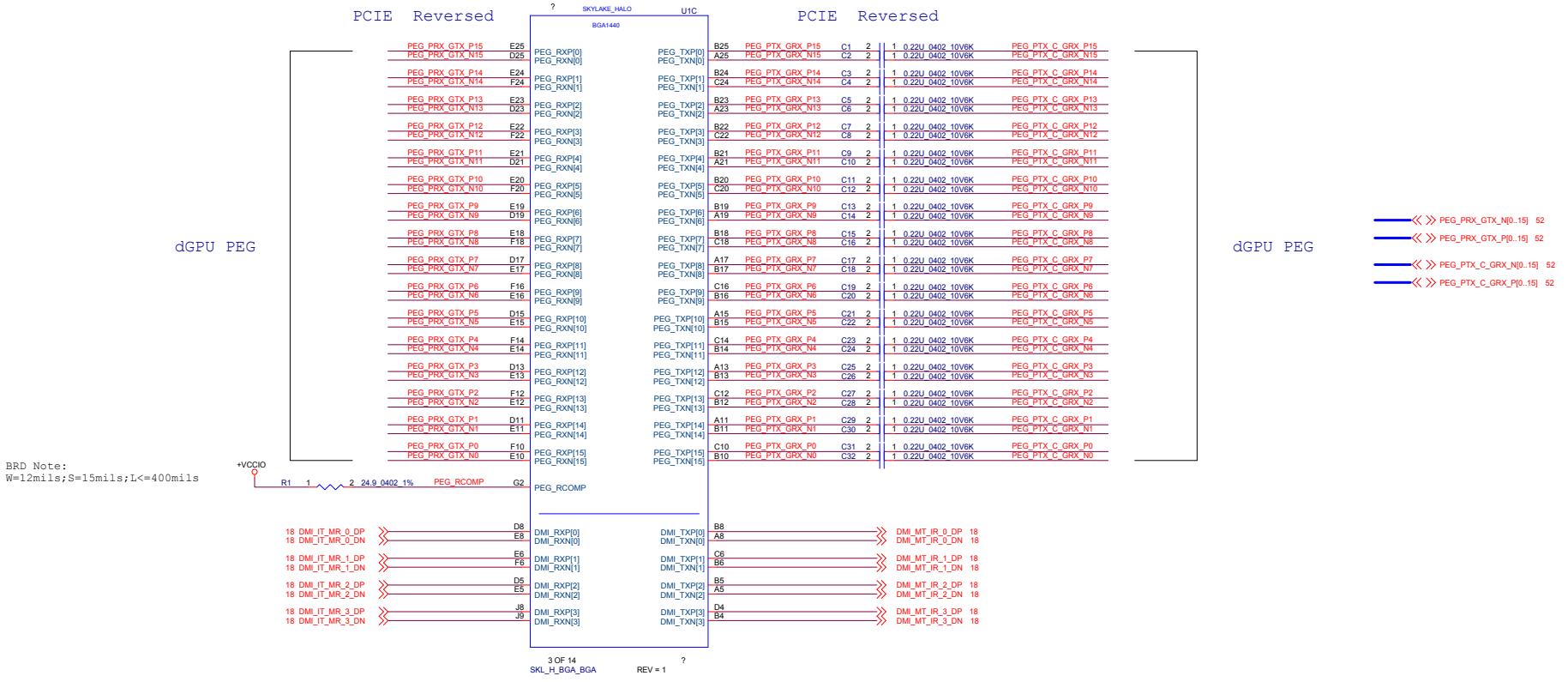


lenovo联想 LENOVO.CRDN

Title: Block Diagram

Size: Custom | Document Number: Skylake-H | Rev: V0.3

Date: Thursday, May 26, 2016 | Sheet 1 of 99



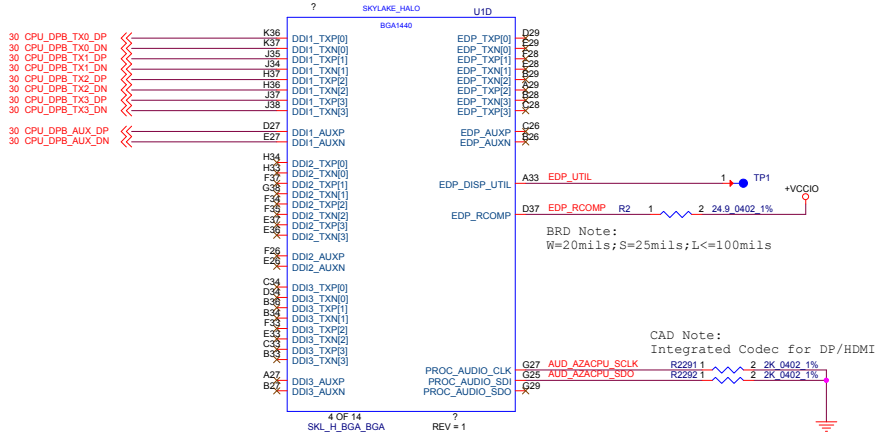
lenovo联想 LENOVO.CRDN

Title: PROCESSOR-PEG/DMI

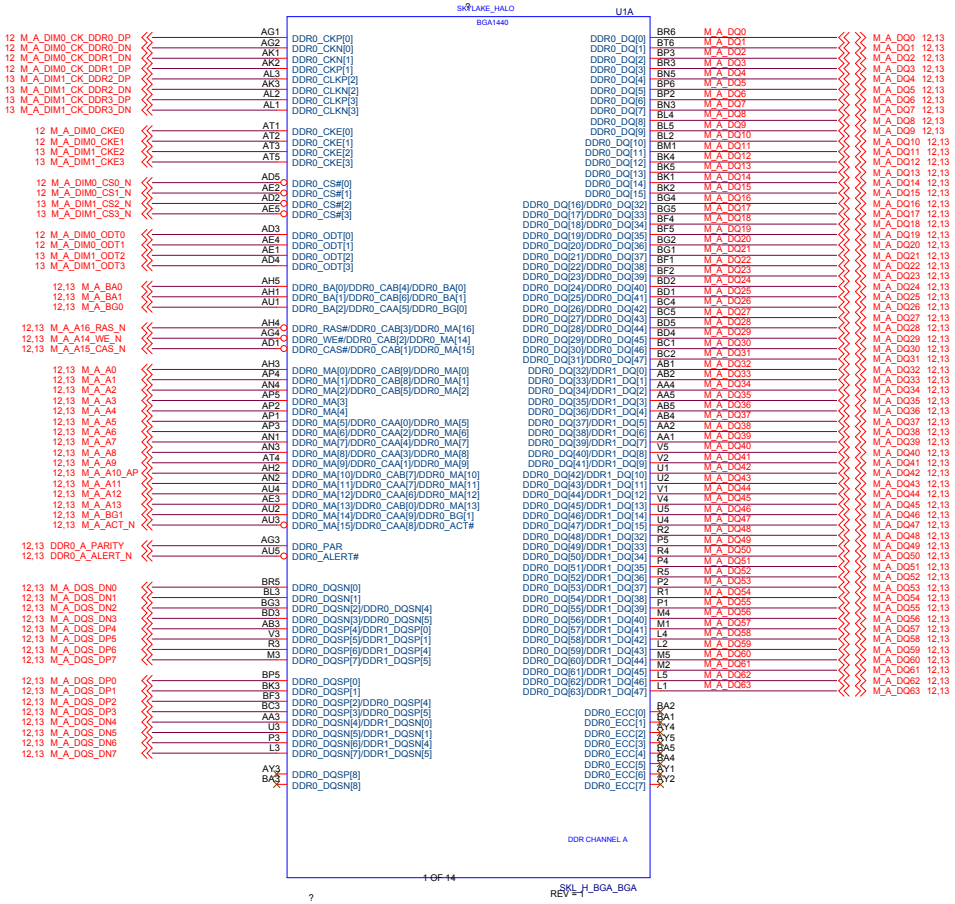
Size	Document Number	Rev
C	Skylake-H	V0.3

Date: Thursday, May 26, 2016 Sheet 2 of 99

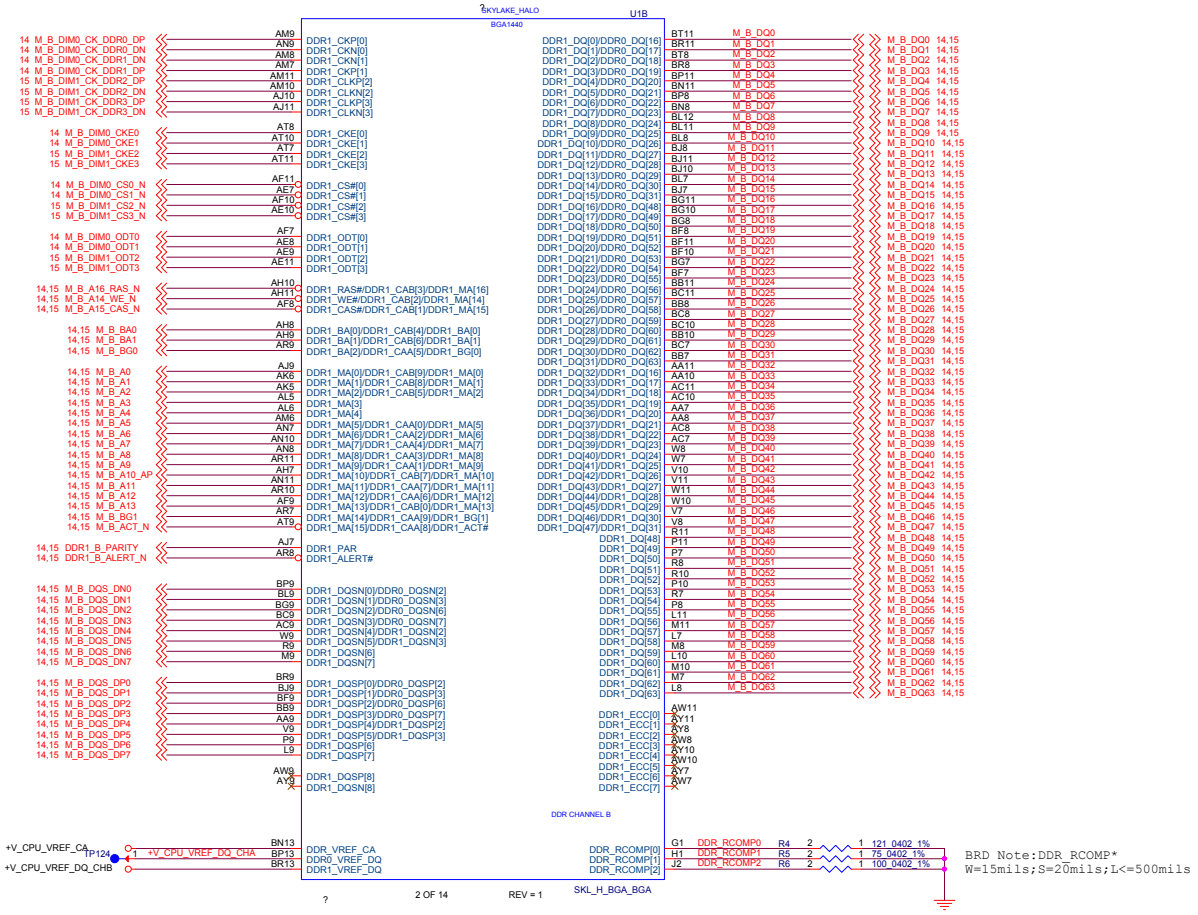
DDI B TO DP PORT, FOR DEBUG



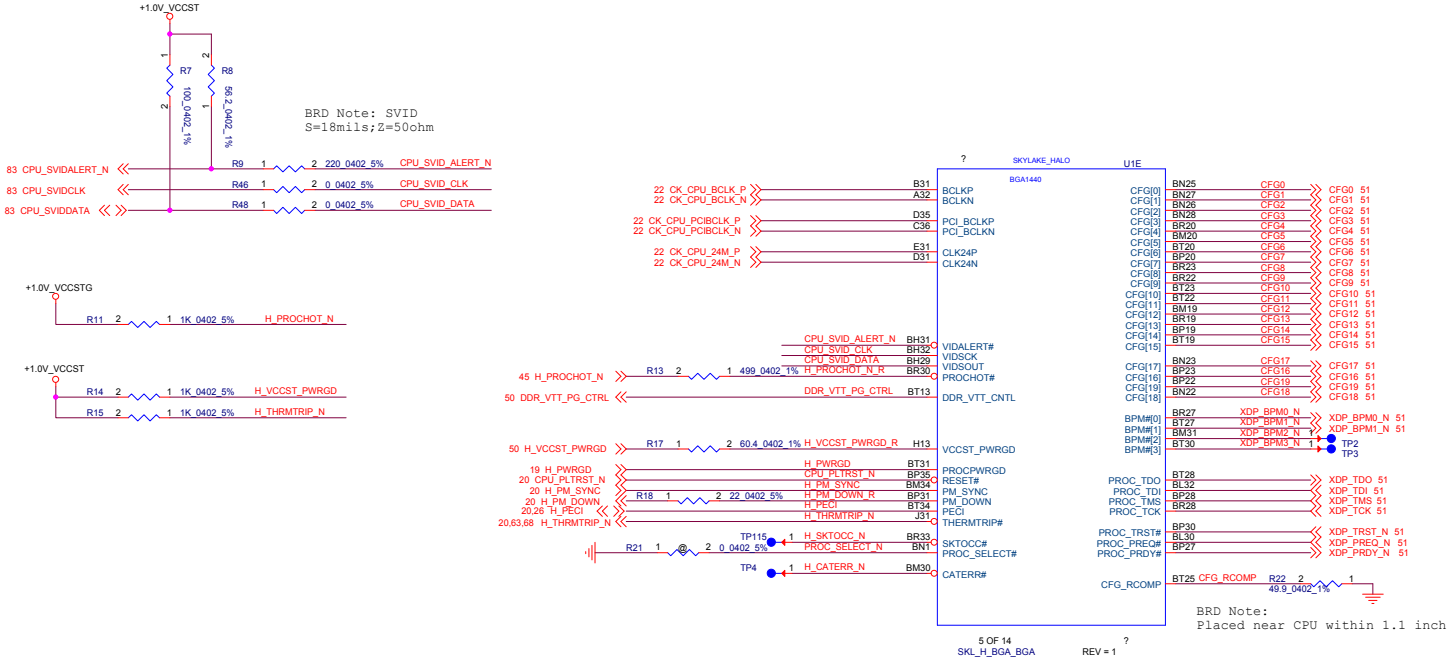
lenovo联想	LENOVO.CRDN	
Title: Processor--eDP/TBT/DP		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Thursday, May 26, 2016	Sheet 3 of 99	

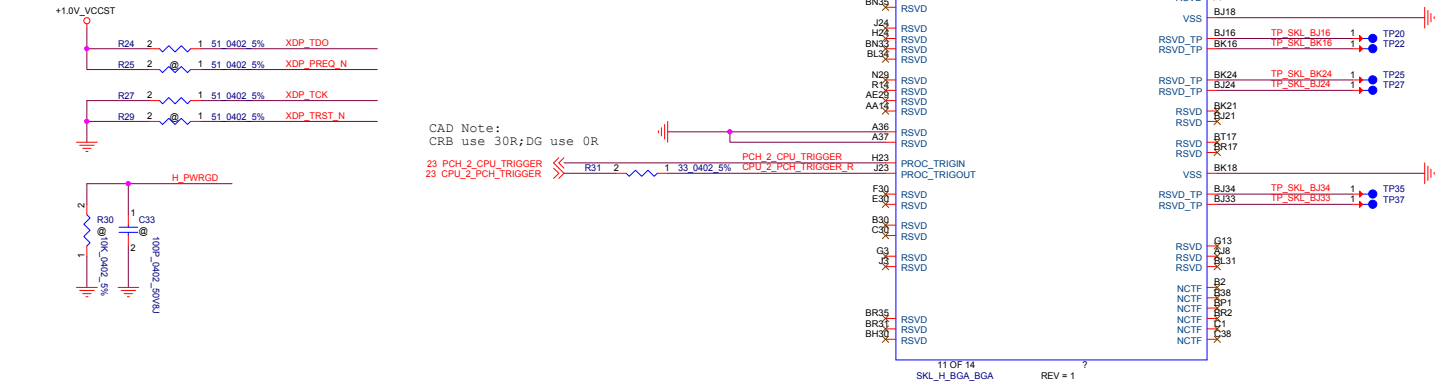


lenovo 联想	LENOVO.CRDN
Title	PROCESSOR-MEM_CH A
Size: C	Document Number: Skylake-H
Rev	V0.3
Date: Thursday, May 26, 2016	Sheet 4 of 99

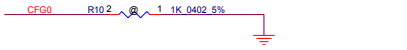


LENOVO.CRDN	
Title	PROCESSOR-MEM_CH B
Size	C
Document Number	Skylake-H
Rev	V0.3
Date:	Thursday, May 26, 2016
Sheet	5 of 99



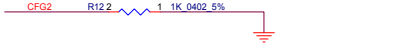


PROCESSOR CFG STRAPS



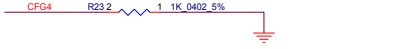
Stall reset sequence after PCU PLL lock until de-asserted

CFG0	1:Normal(Default) *
	0:Stall



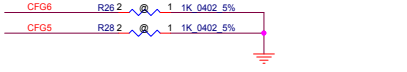
PEG16x Static Lane Reversal Strap

CFG2	1:Normal
	0:Reversed(Default) *



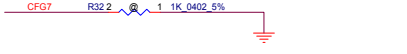
Embedded Display Port Presence Strap

CFG4	1:Disable
	0:Enable(Default) *



PEG CONFIG Straps

CFG[6:5]	11: x16 (Default)) *
	10: x8, x8
	01: Reserved
	00: x8,x4,x4



PEG TRAINNING

CFG7	1: follow RESET# deassertion *
	0: Wait for BIOS for training

lenovo联想 LENOVO.CRDN

Title: PROCESSOR-CLK/PM/STRAP/TP

Size: C | Document Number: Skylake-H | Rev V0.3

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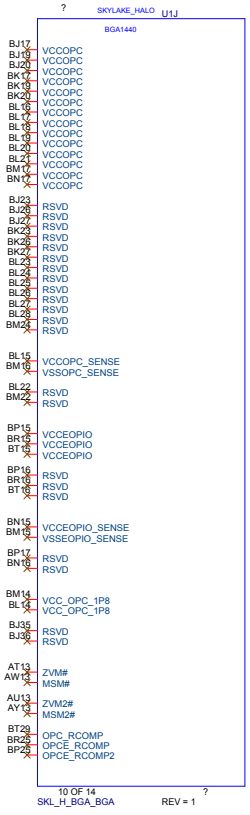
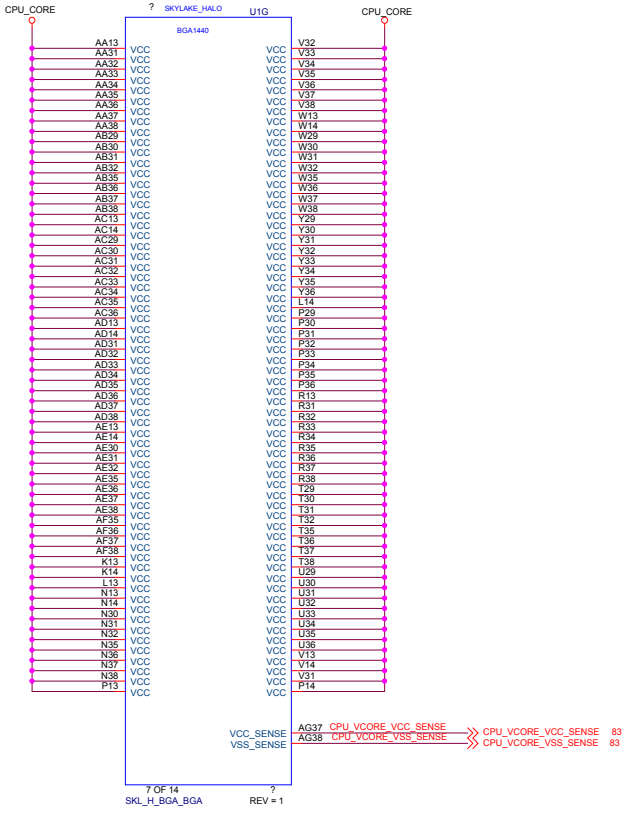
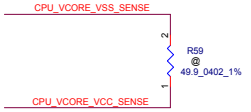
FOR H4+4e







lenovo联想 LENOVO.CRDN

Title: PROCESSOR-POWER

Size: C | Document Number: Skylake-H | Rev: V0.3

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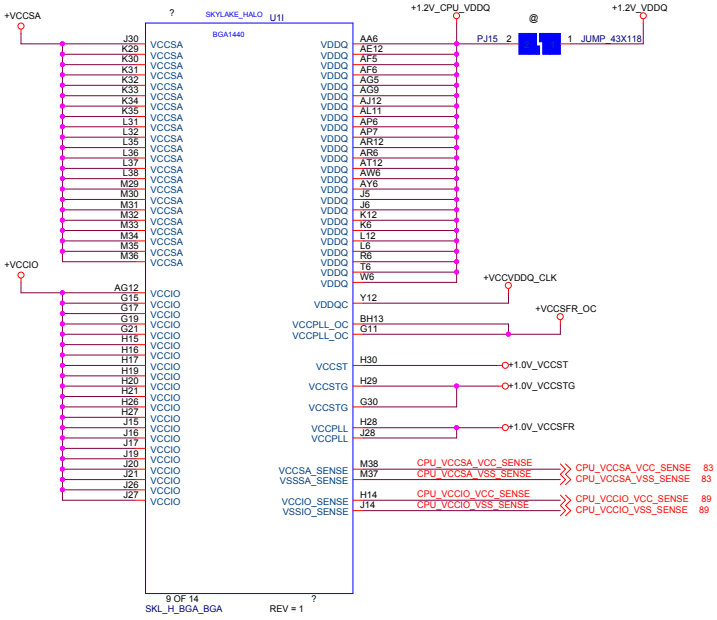
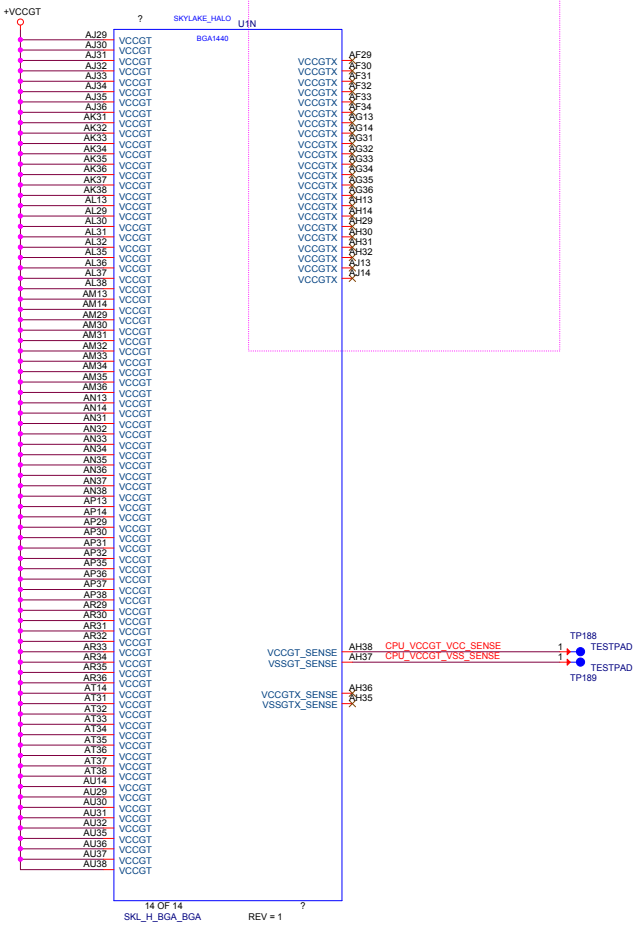
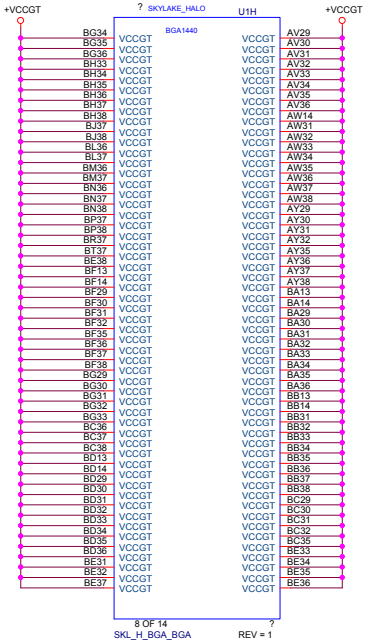
FOR H4+4e







lenovo联想	LENOVO.CRDN	
Title: PROCESSOR-POWER		
Size: C	Document Number: Skylake-H	Rev: V0.3
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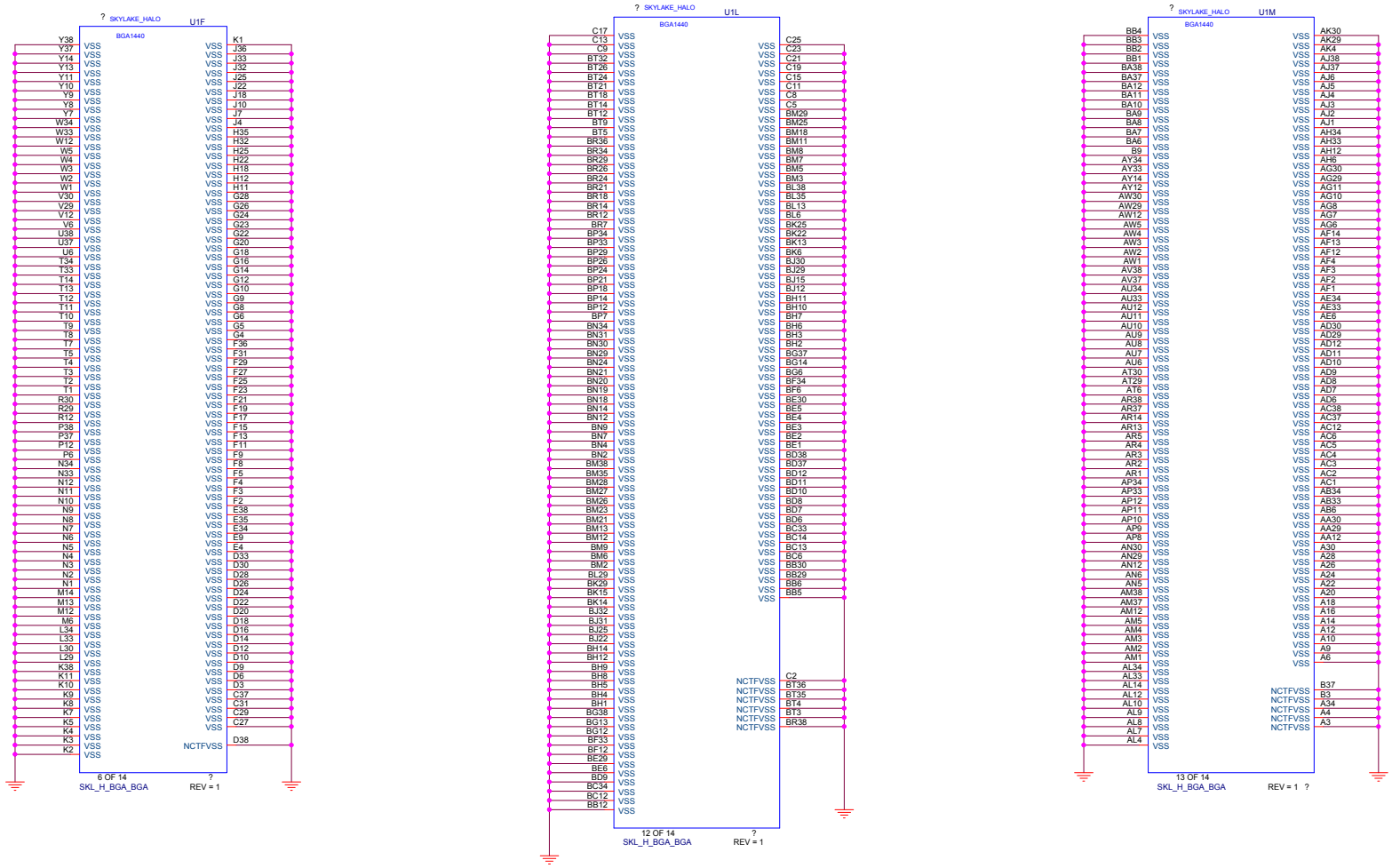

lenovo联想	LENOVO.CRDN
Title	PROCESSOR-VSS
Size C	Document Number Skylake-H
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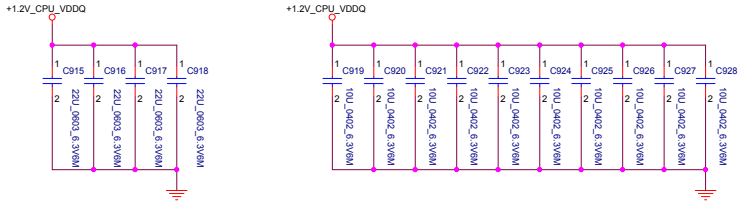
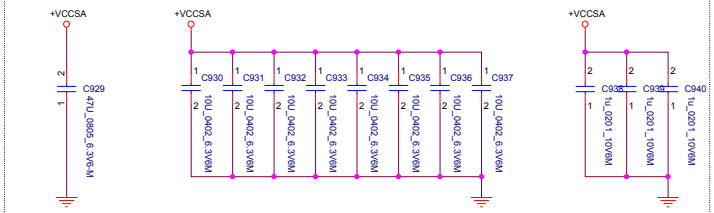
+1.2V_CPU_VDDQ 4X0603(22UF) 10X0402(10UF)

BRD Note:
Placed backside

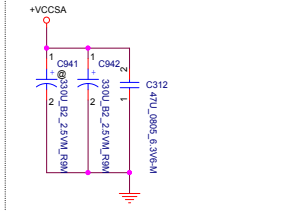


+VCCSA
BOTTOM:1X0805(47UF), 8X0402(10UF), 3X0201(1UF);
TOP:2XBULK(220UF),1X0805(22UF)

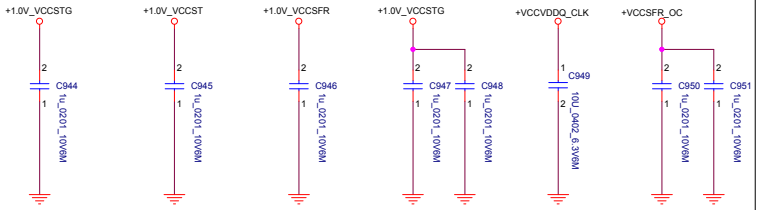
BRD Note:
Placed backside



BRD Note:
Placed TOP BGA EDGE



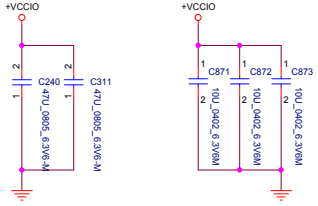
BRD Note:
Placed backside



+VCCIO 2x0805(47UF) 3X0402(10UF)

BRD Note:
Placed TOP BGA EDGE

BRD Note:
Placed backside



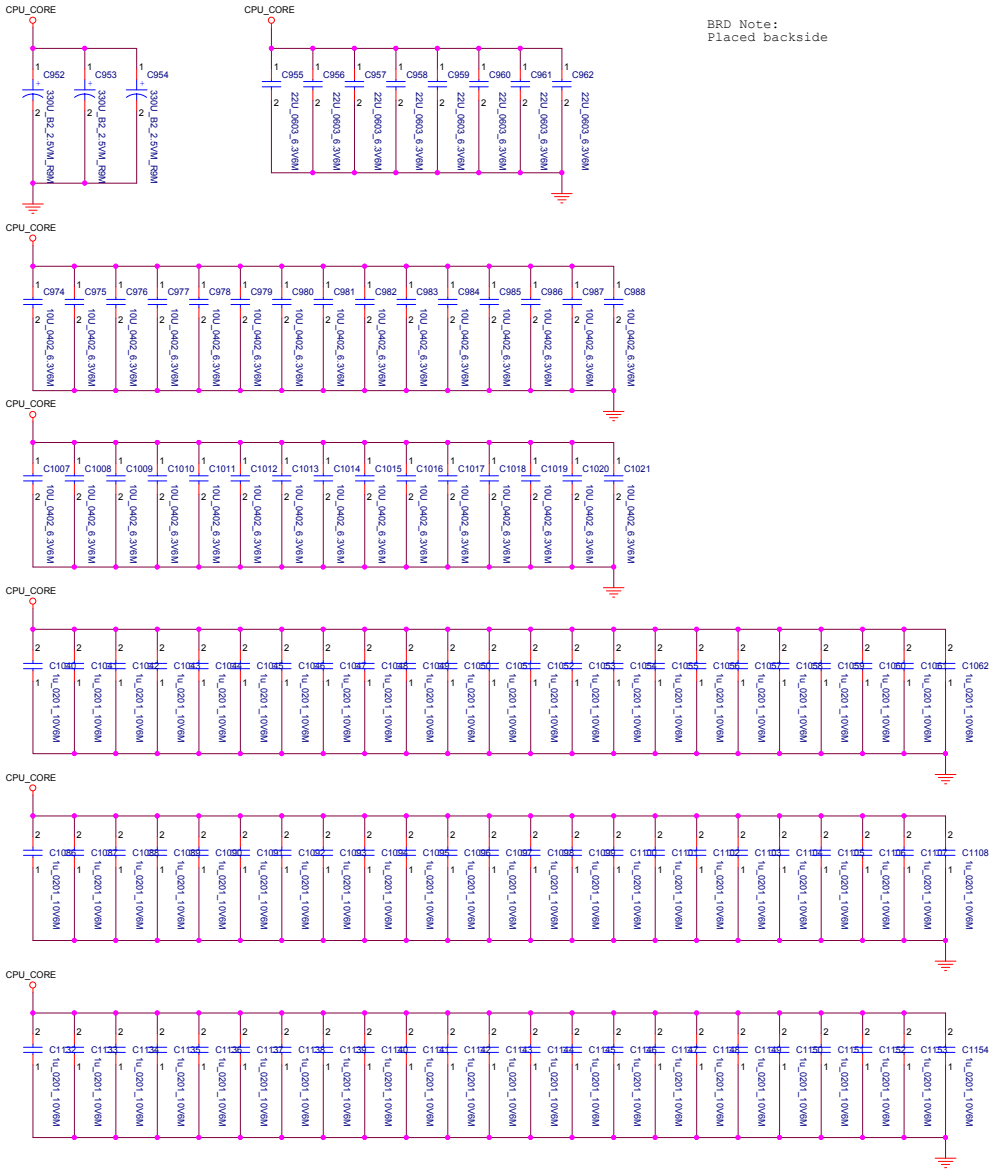
lenovo联想 LENOVO.CRDN

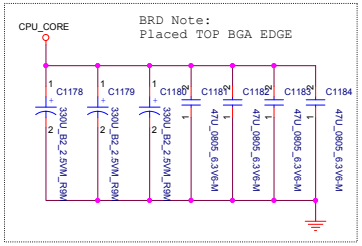
Title: PROCESSOR Decoupling 1/2

Size: C | Document Number: Skylake-H | Rev: V0.3

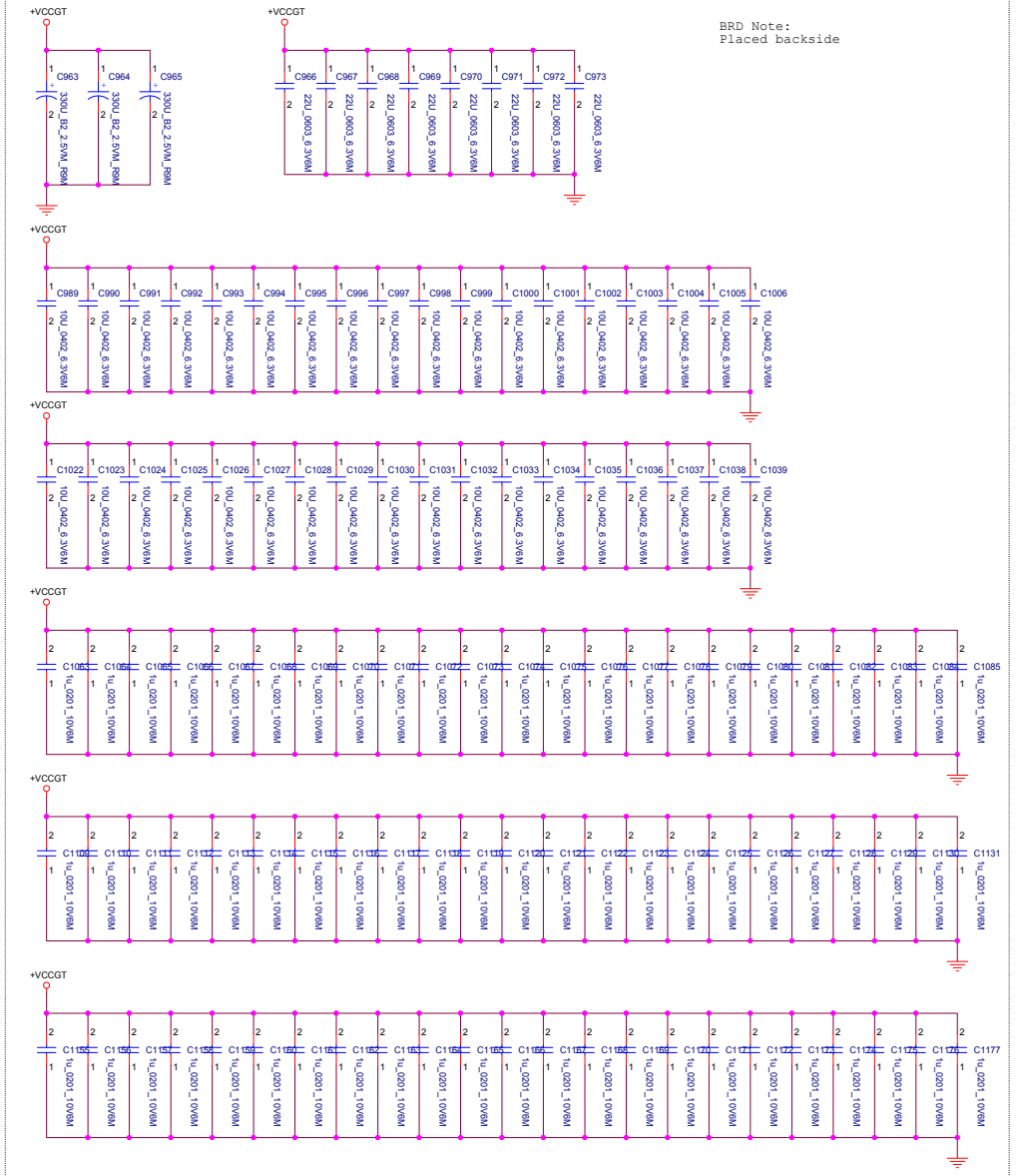
Date: Thursday, May 26, 2016 | Sheet 10 of 99

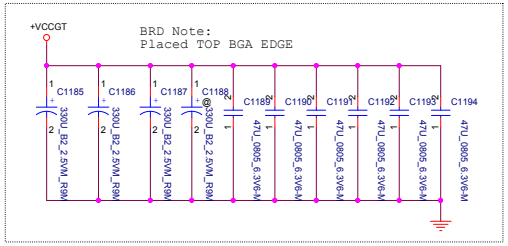
CPU_CORE
BOTTOM:3XBULK(220UF),8x0603(22U),30X0402(10UF), 69X0201(1UF);
TOP:3XBULK(220UF),4X0805(47UF)





+VCCGT
BOTTOM:4XBULK(220UF),8X0603(22U),36X0402(10UF), 69X0201(1UF);
TOP:4XBULK(220UF),6X0805(47UF)





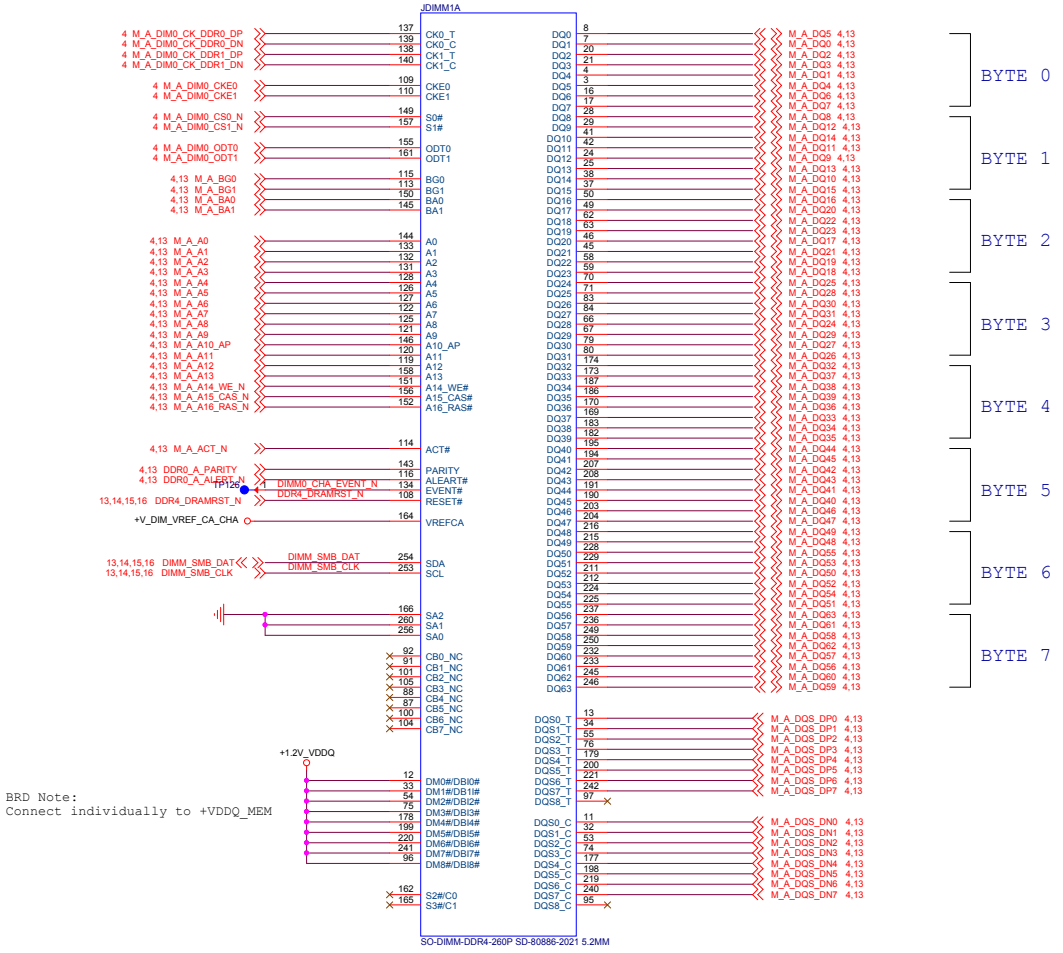
lenovo联想 LENOVO.CRDN

Title
PROCESSOR Decoupling 2/2

Size	Document Number	Rev
C	Skylake-H	V0.3

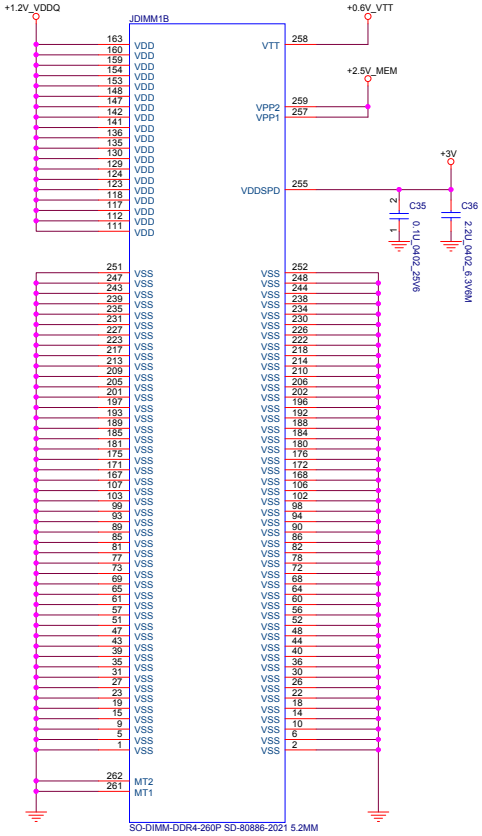
Date: Thursday, May 26, 2016 Sheet 11 of 99

DDR4 SODIMM CHANNEL - A BOTTOM REV DIMM0 (5.2 MM HEIGHT CONNECTOR)



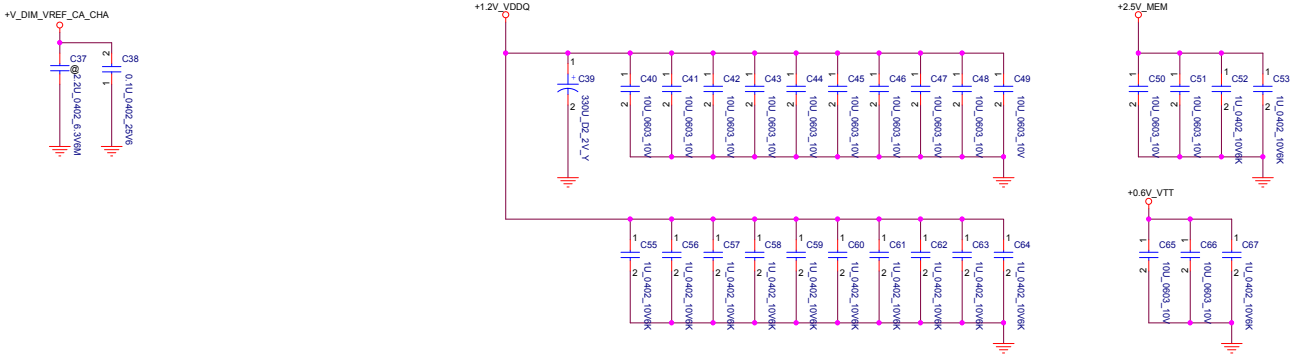
SPD ADDRESS:0xA0

BRD Note:
Connect individually to +VDDQ_MEM



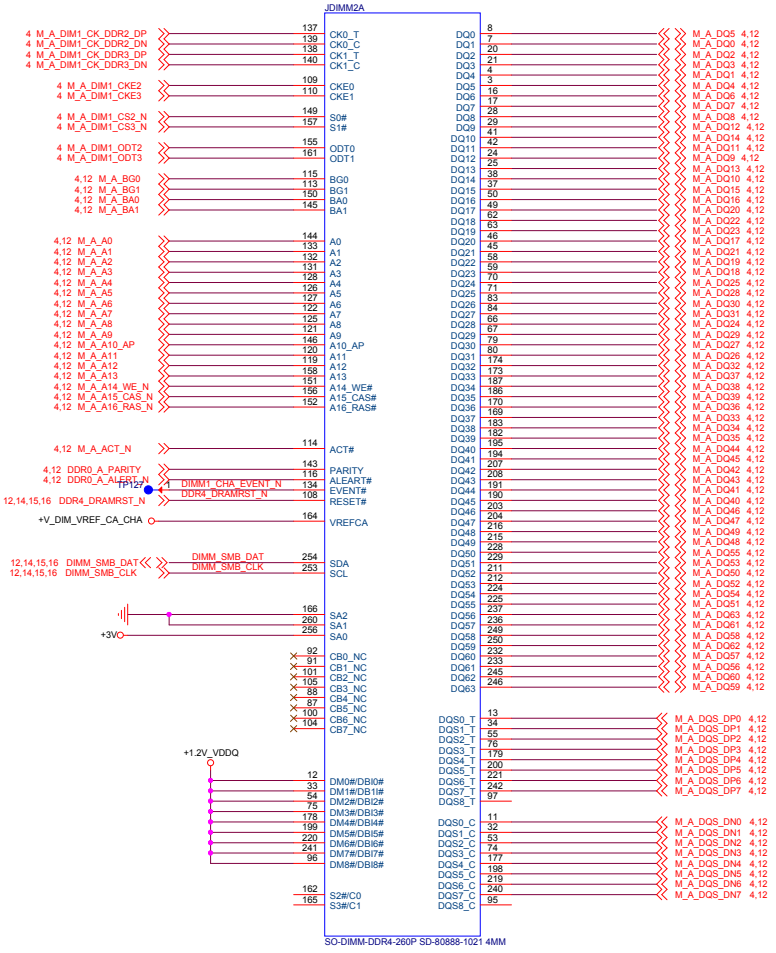
Decoupling Caps

BRD Note:
placed close to CHA DIMM0

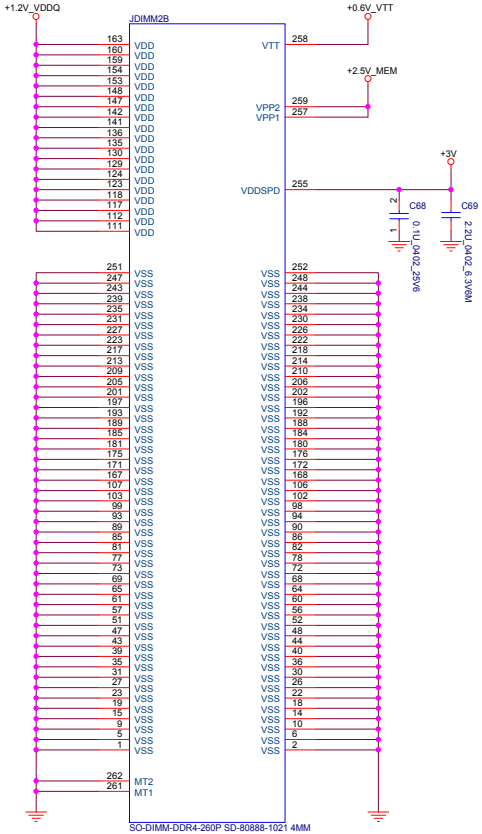


lenovo联想	LENOVO.CRDN
Title	DDR4 CHA DIMM0
Size C	Document Number Skylake-H
Rev	V0.3
Date: Thursday, May 26, 2016	Sheet 12 of 99

DDR4 SODIMM CHANNEL - A TOP STD DIMM1 (4 MM HEIGHT CONNECTOR)

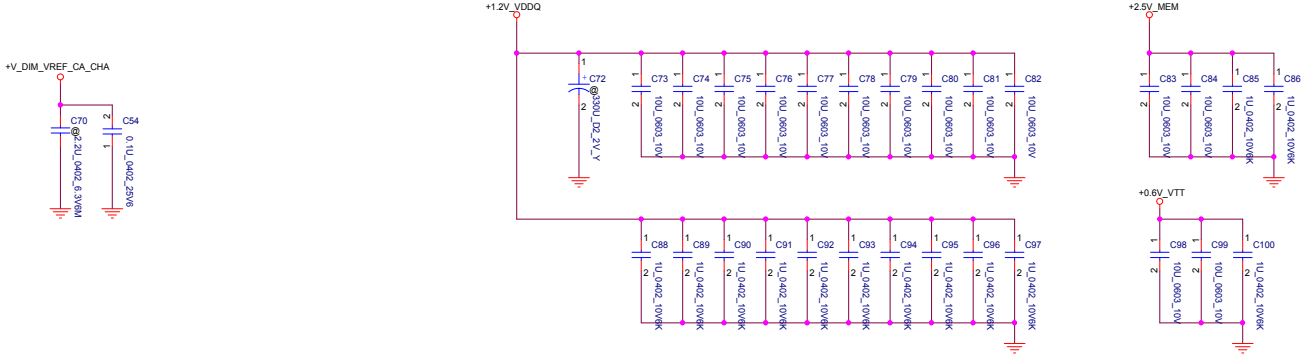


SPD ADDRESS:0xA2



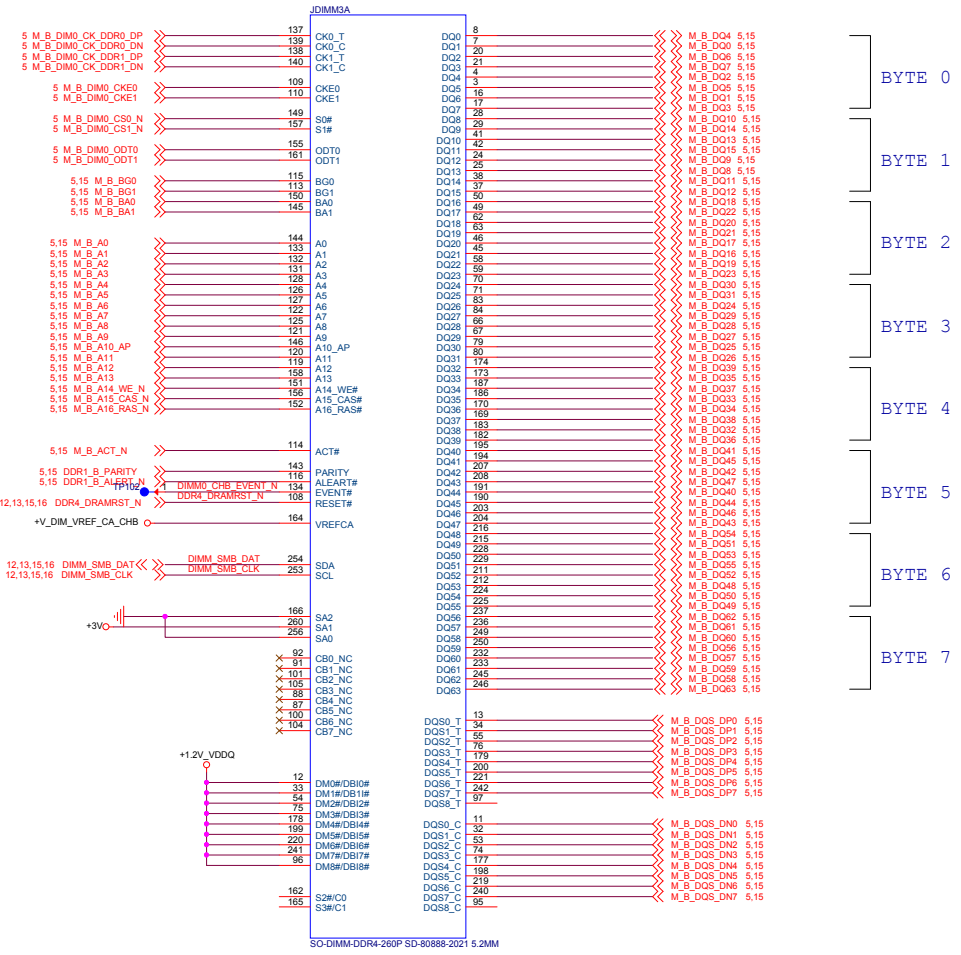
Decoupling Caps

BRD Note:
placed close to CHA DIMM0

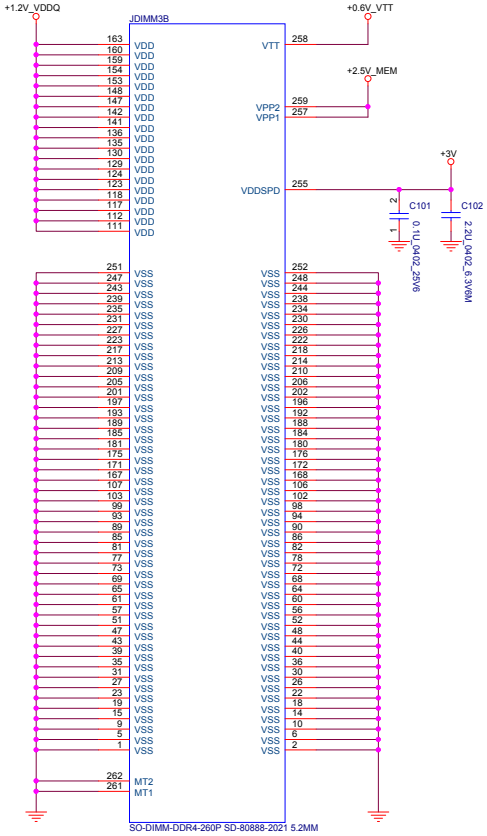


lenovo联想	LENOVO.CRDN
Title	DDR4 CHA DIMM1
Size C	Document Number Skylake-H
Rev	V0.3
Date: Thursday, May 26, 2016	Sheet 13 of 99

DDR4 SODIMM CHANNEL - B BOTTOM STD DIMM0 (5.2 MM HEIGHT CONNECTOR)

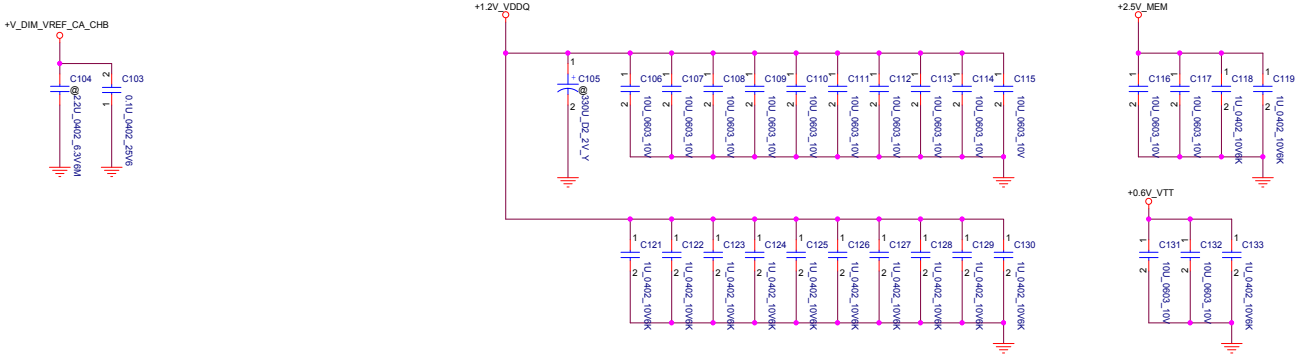


SPD ADDRESS:0xA4



Decoupling Caps

BRD Note:
placed close to CHA DIMM0



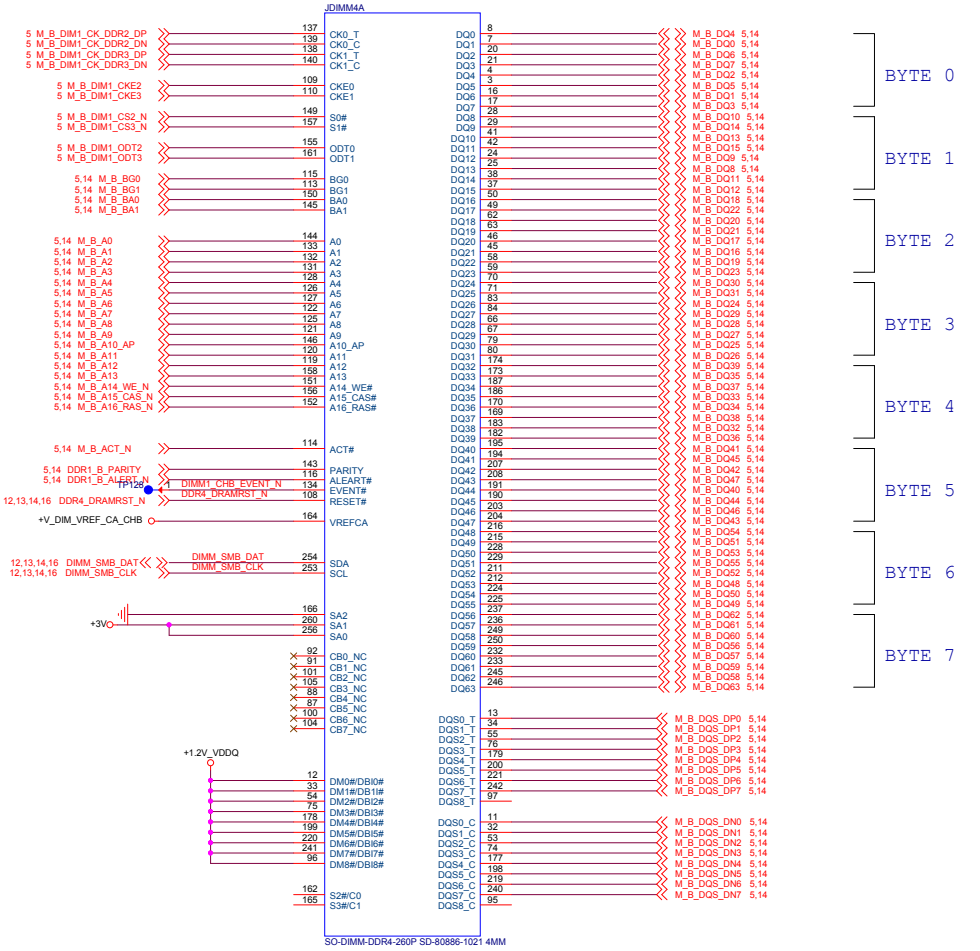
lenovo联想 LENOVO.CRDN

Title: DDR4 CHB DIMM0

Size: C | Document Number: Skylake-H | Rev V0.3

Date: Thursday, May 26, 2016 | Sheet 14 of 99

DDR4 SODIMM CHANNEL - B TOP REV DIMM1 (4.0 MM HEIGHT CONNECTOR)



SPD ADDRESS:0xA6

BYTE 0

BYTE 1

BYTE 2

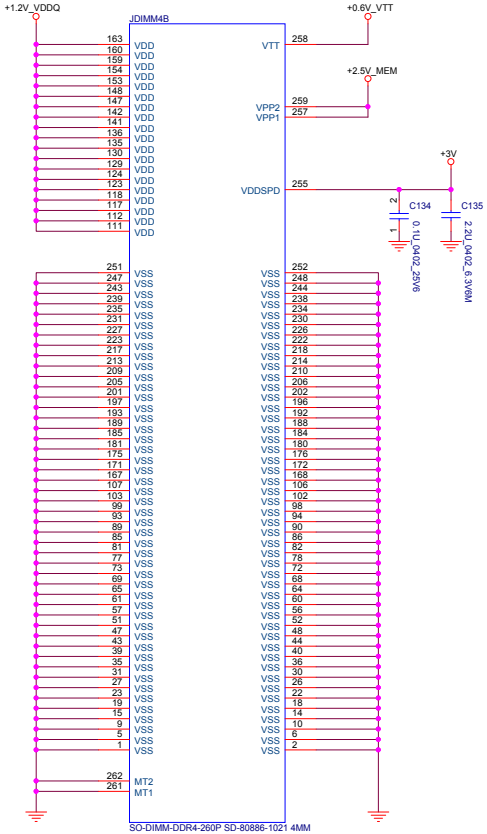
BYTE 3

BYTE 4

BYTE 5

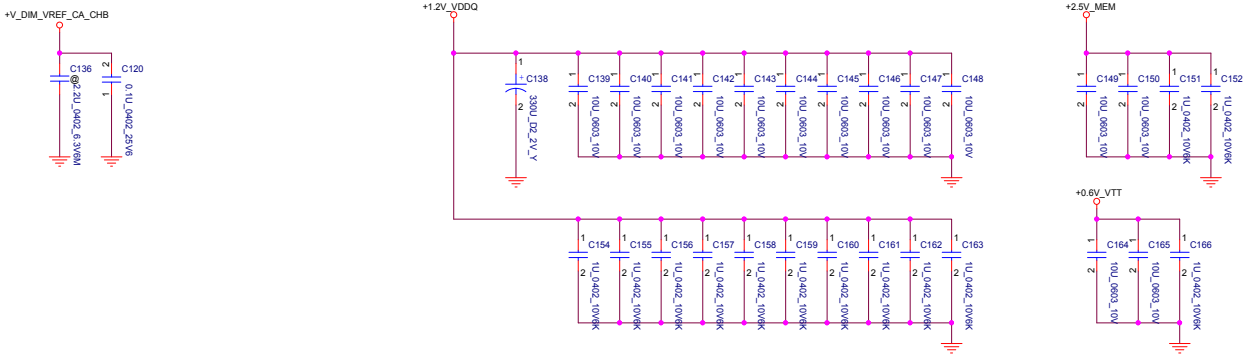
BYTE 6

BYTE 7



Decoupling Caps

BRD Note:
placed close to CHA DIMM0



lenovo联想 LENOVO.CRDN

Title: DDR4 CHB DIMM1

Size	Document Number	Rev
C	Skylake-H	V0.3

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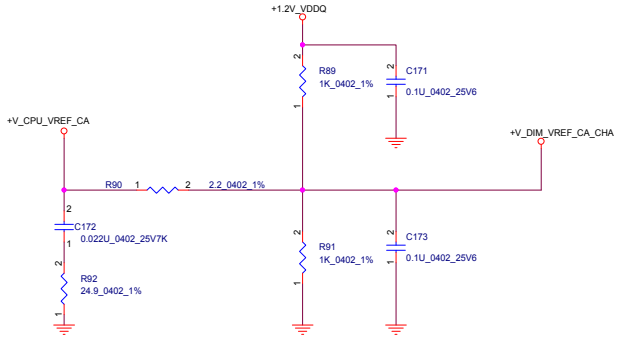
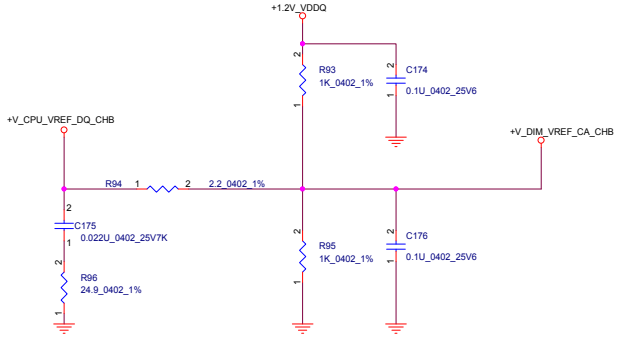
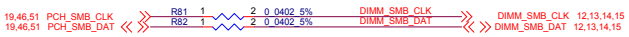
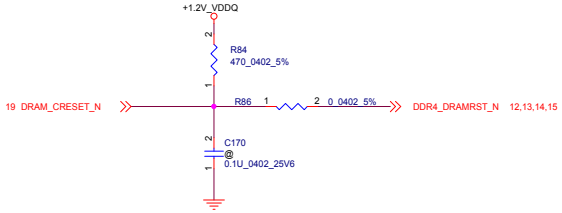
DDR VREF

BRD Note:
VREF trace width 20mils;spacing 20 mils to other signal/planes

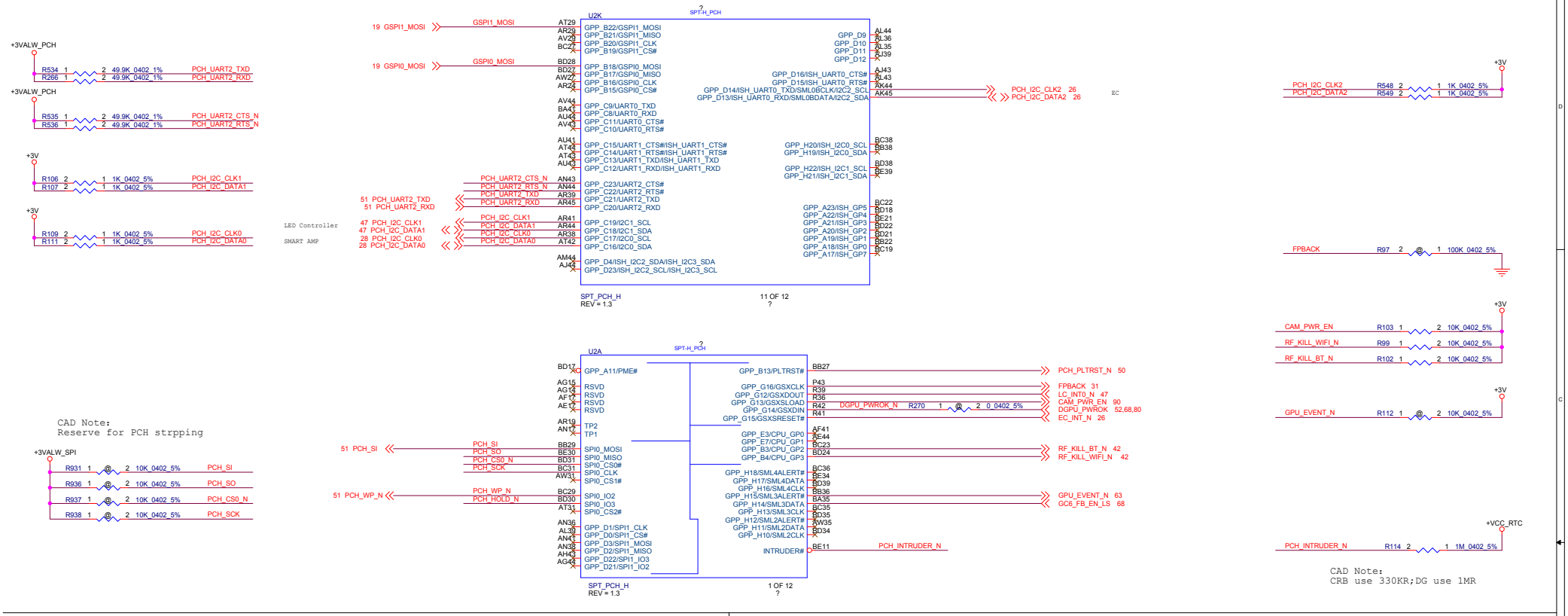




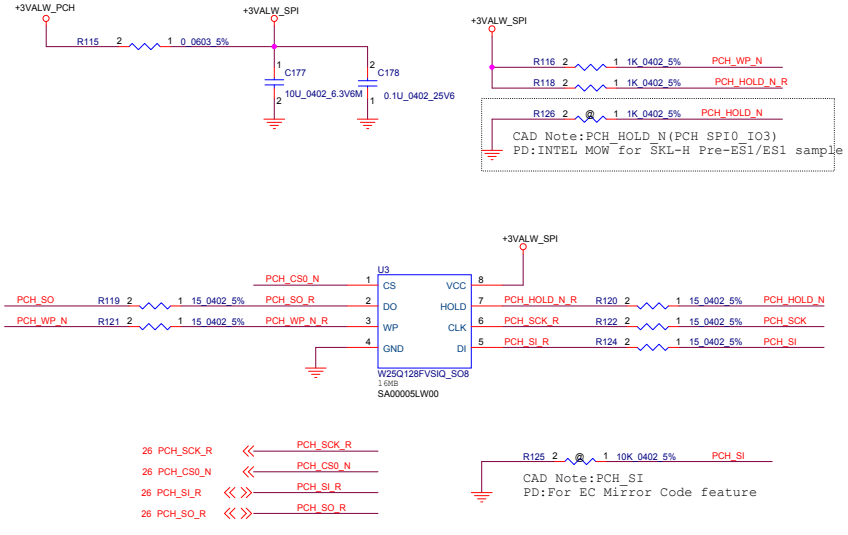




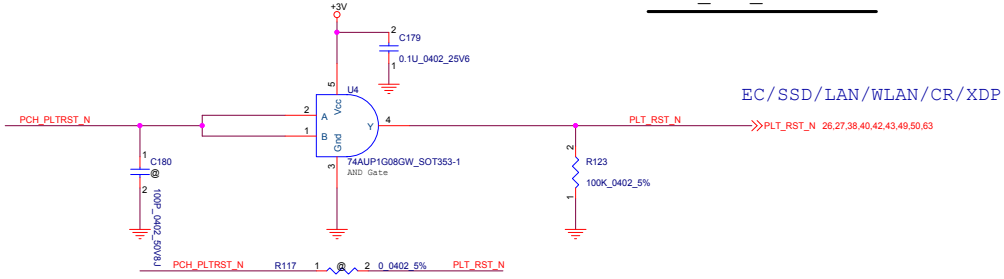
lenovo联想	LENOVO.CRDN	
Title: DDR4-VREF		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Thursday, May 26, 2016	Sheet 16 of 99	



SPI ROM



PLT_RST_N Buffer



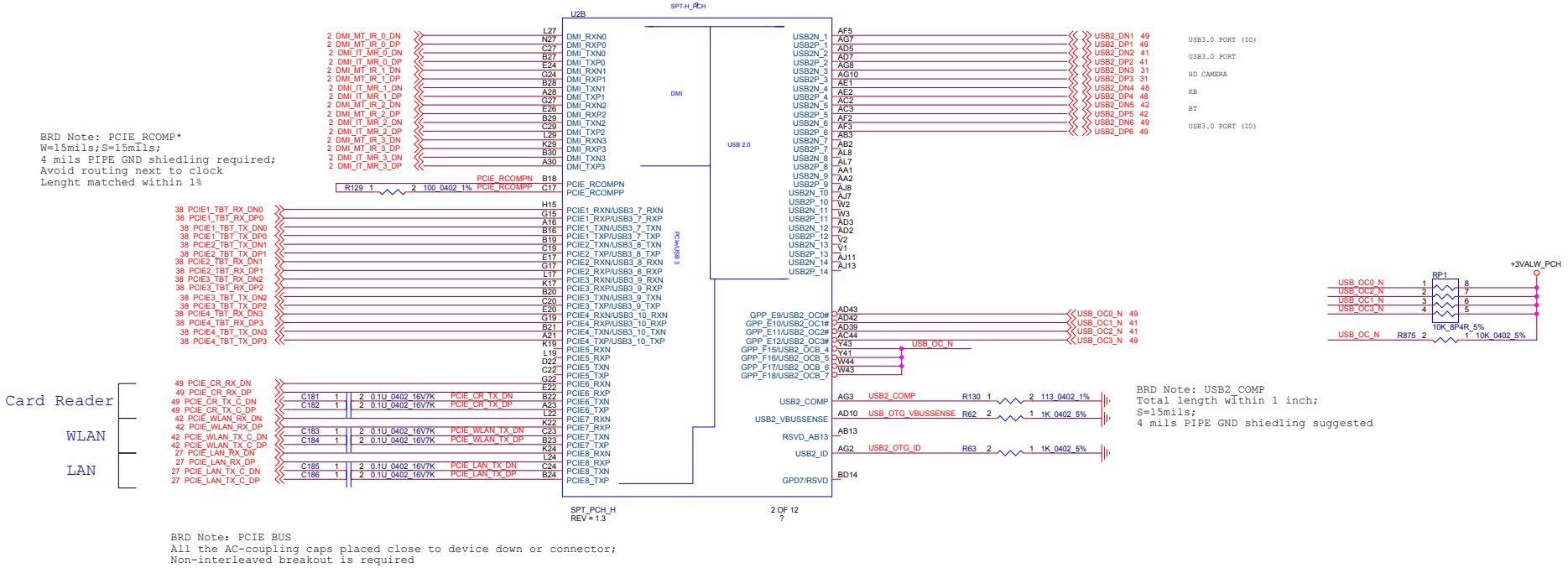
DISPLAY_MUX_SW Buffer

CAD Note: DISPLAY_MUX_SW
L=CPU output selected
H=dGPU output selected(default)

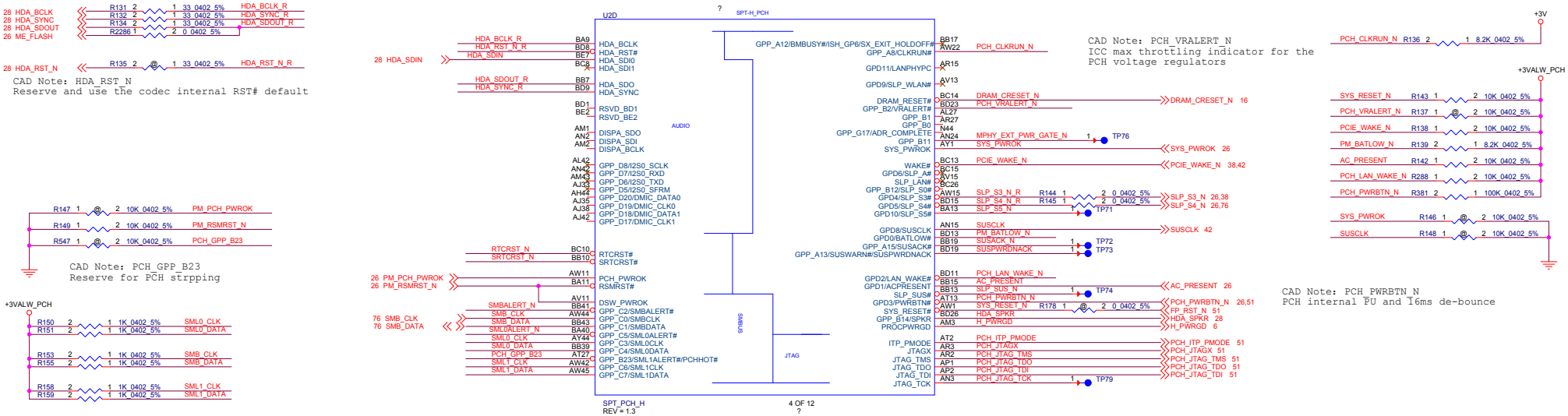
lenovo联想	LENOVO.CRDN	
Title: PCH-SPI/I2C/GPIO		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Thursday, May 26, 2016	Sheet 17 of 99	

Flexible I/O Configuration				
I / O	High Speed Signals	Configuration	DEVICE	GEN
Port 7	USB3_7 / PCIE 1	AR (L0)	U2005 (Intel AR DP)	
Port 8	USB3_8 / PCIE 2	AR (L1)		
Port 9	USB3_9 / PCIE 3	AR (L2)		
Port 10	USB3_10 / PCIE 4	AR (L3)		
Port 11	PCIE 5	NC		
Port 12	PCIE 6	Card Reader	U3001	PCIE 1x Gen2
Port 13	PCIE 7	WLAN	JWLAN1	PCIE 1x Gen2
Port 14	PCIE 8	LAN	U6	PCIE1x Gen1

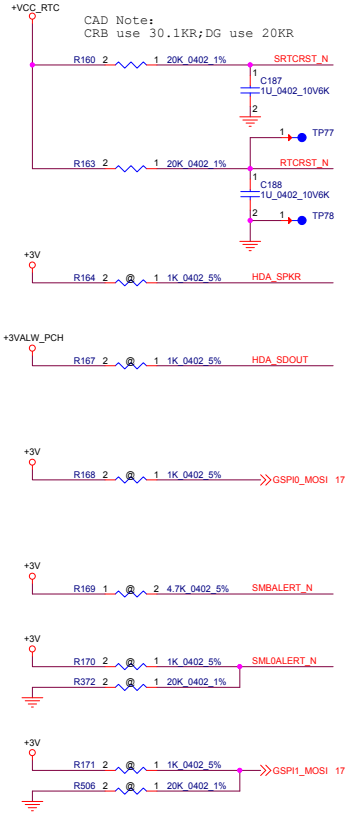
USB2.0 Configuration		
USB2 #	Assignment	OCx #
USB2 1	JUSB3(IO DB)	USB_OC0_N
USB2 2	JUSB2	USB_OC1_N
USB2 3	HD camera	
USB2 4	KB	
USB2 5	BT	
USB2 6	JUSB4(IO DB)	USB_OC3_N
USB2 7	NC	
USB2 8	NC	
USB2 9	NC	
USB2 10	NC	
USB2 11	NC	
USB2 12	NC	
USB2 13	NC	
USB2 14	NC	



lenovo联想	LENOVO.CRDN
Title	PCH-DMI/PCIE/USB2.0
Size C	Document Number Skylake-H
Rev	V0.3
Date: Thursday, May 26, 2016	Sheet 18 of 99



PCH Straps



ME RESET

SRTCRST_N	1:SAVE ME (Default) *
	0:CLEAR ME

CMOS RESET

RTCRST_N	1:SAVE CMOS (Default) *
	0:CLEAR CMOS

Top Swap MODE

HDA_SPKR	1:Enabled
	0:Disabled(Default),Internal PD *

Flash Descriptor Security Override

HDA_SDOUT	1:Disabled
	0:Enabled(Default),Internal PD *

TCO Timer System No Reboot mode

GSPI0_MOSI	1:Enable "No reboot" mode
	0:Disable (Default),Internal PD *

Intel ME TLS cipher suite

SMBALERT_N	1:Enabled
	0:Disabled(Default),Internal PD *

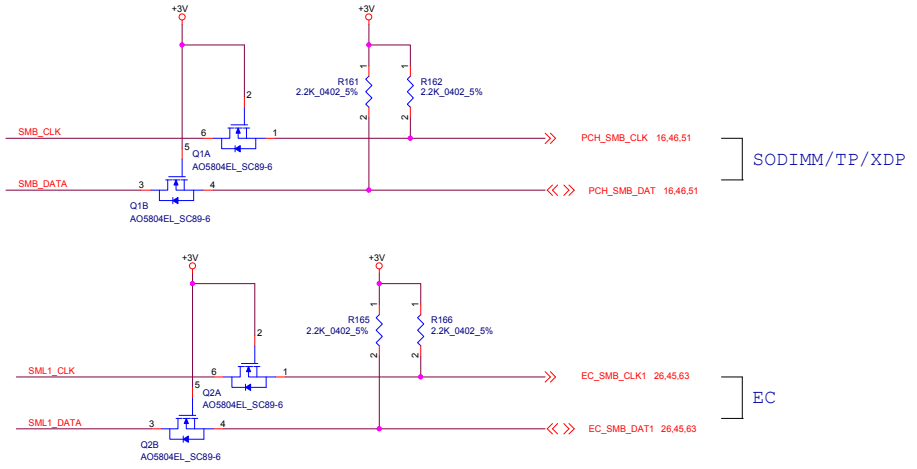
eSPI or LPC bus for EC

SML0ALERT_N	1:eSPI
	0:LPC(Default),Internal PD *

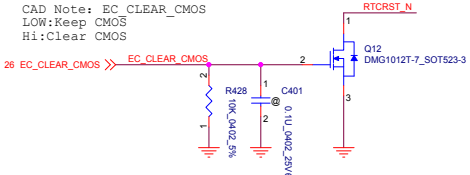
Boot BIOS Destination Bit 10

GSPI1_MOSI	1:LPC
	0:SPI(Default),Internal PD *

SMBus Isolation



EC Clear CMOS



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Title: PCH-HDA/PM/SMBUS/STRAP

Size: C | Document Number: Skylake-H | Rev: V0.3

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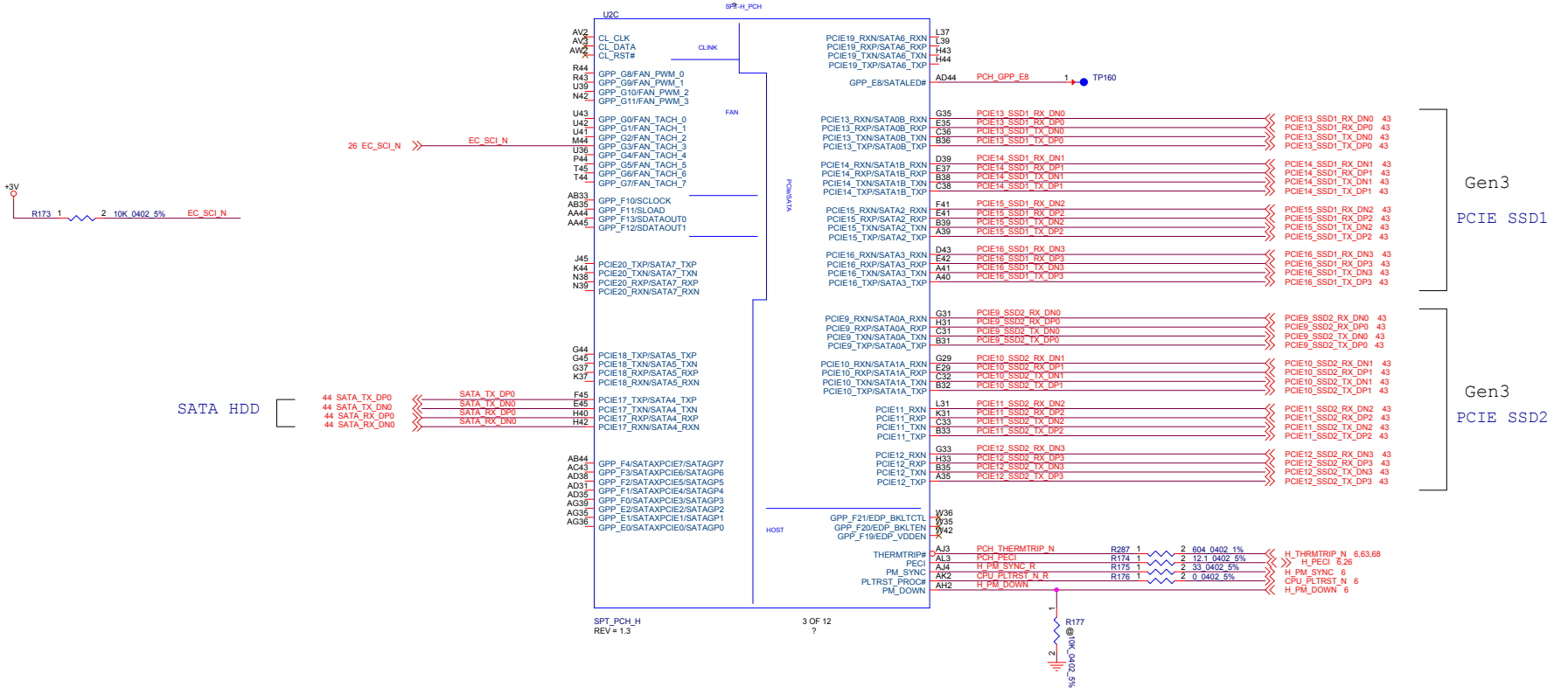
Flexible I/O Configuration

I / O	High Speed Signals	Configuration	DEVICE	GEN
Port 15	SATA 0A / PCIE 9	M.2 SSD2 (L0) / SATA0	JSSD2	PCIE 4x Gen 3 /SATA Gen 3
Port 16	SATA 1A / PCIE 10	M.2 SSD2 (L1)		
Port 17	/ PCIE 11	M.2 SSD2 (L2)		
Port 18	/ PCIE 12	M.2 SSD2 (L3)		
Port 19	SATA 0B / PCIE 13	M.2 SSD12(L0)	JSSD1	PCIE 4 x Gen 3
Port 20	SATA 1B / PCIE 14	M.2 SSD1 (L1)		
Port 21	SATA 2 / PCIE 15	M.2 SSD1 (L2)		
Port 22	SATA 3 / PCIE 16	M.2 SSD1 (L3)		
Port 23	SATA 4 / PCIE 17	SATA HDD	U14	SATA Gen 3
Port 24	SATA 5 / PCIE 18	NC		
Port 25	SATA6 / PCIE 19	NC		
Port 26	SATA7 / PCIE 20	NC		



BRD Note: PCIE BUS
All the AC-coupling caps placed close to connector side;
Non-interleaved breakout is required

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Title: PCH-PCIE/SATA/HOST

Size: C | Document Number: Skylake-H | Rev: V0.3

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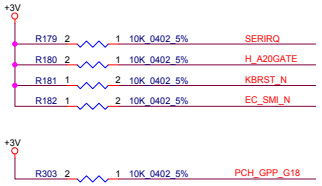
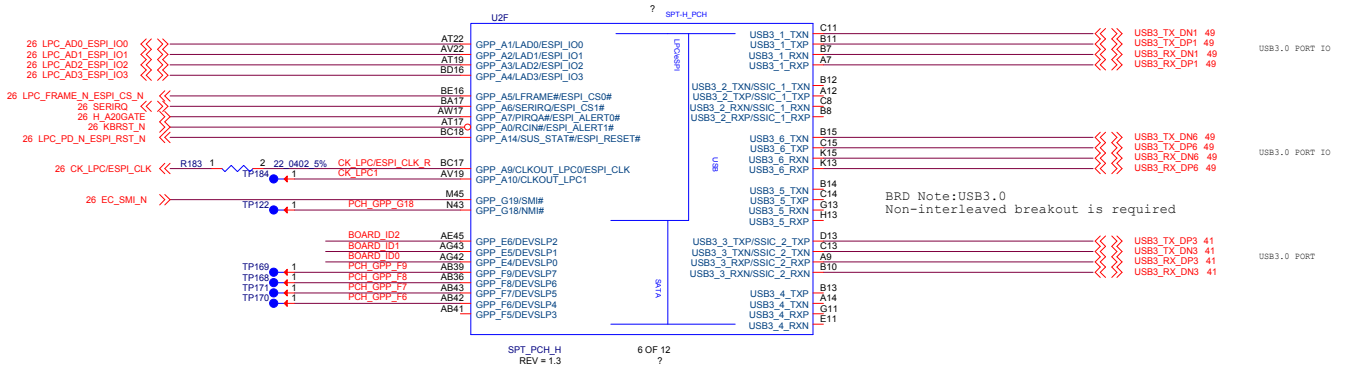
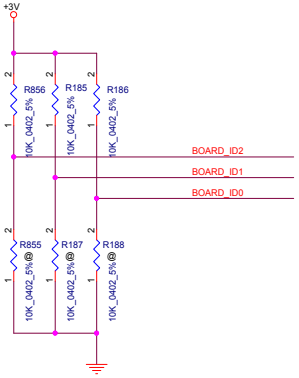
Flexible I/O Configuration				
I / O	High Speed Signals	Configuration	DEVICE	OCx #
Port 1	USB3 1 Capable of OTG	USB3.0	JUSB3(IO DB)	USB_OC0_N
Port 2	USB2 3 / SSIC 1	NC		
Port 3	USB3 3 / SSIC 2	USB3.0	JUSB2	USB_OC1_N
Port 4	USB3 4	NC		
Port 5	USB3 5	NC		
Port 6	USB3 6	USB3.0	JUSB4(IO DB)	USB_OC3_N



CAD Note:
LPC:24M Hz
eSPI:20/30/60M Hz





BOARD_ID2	BOARD_ID1	BOARD_ID0	Description
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

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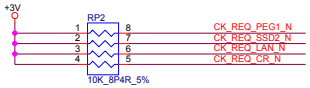
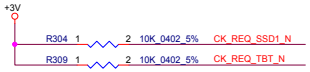
Title: PCH-USB3.0/LPC

Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Thursday, May 26, 2016 | Sheet 21 of 99

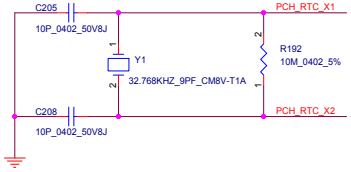




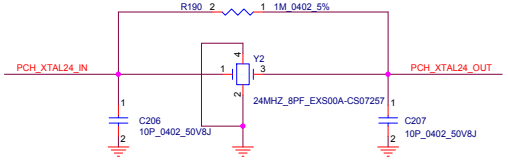
BRD Note: XCLK_BIASREF
Ground reference;Max via:2
Isolation spacing:20mils
Segment Length:100mils;Total length:1000mils
VSS shield recommened;S:W:S=6:4:6

dGPU
WLAN
Card Reader
PCIE SSD2
LAN
TBT
PCIE SSD1

CAD Note:
Max crystal ESR 50K ohm



BRD Note:
Z0=50 ohm +-15%;Ground reference;Max via:2
Group spacing:15mils;Isolation spacing:20mils
Segment Length:100mils;Total length:1000mils;Length match:100mils
VSS shield recommened;S:W:S=6:4:6



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Title: PCH-CLOCK

Size: C | Document Number: Skylake-H | Rev: V0.3

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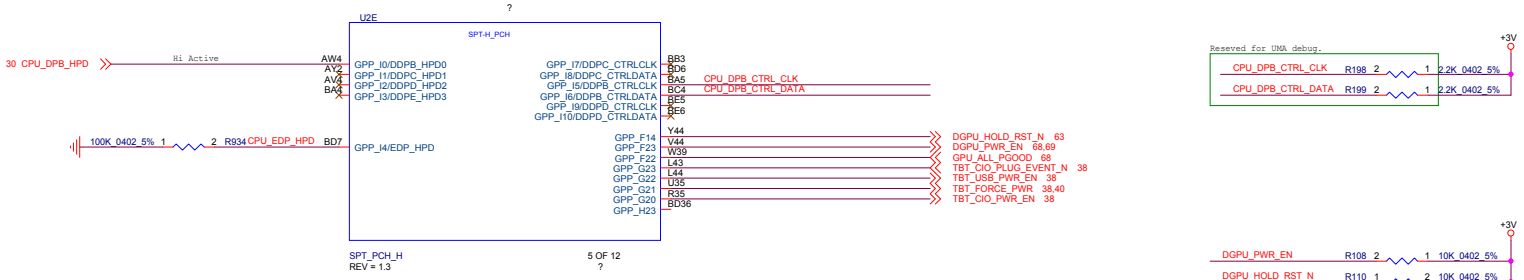

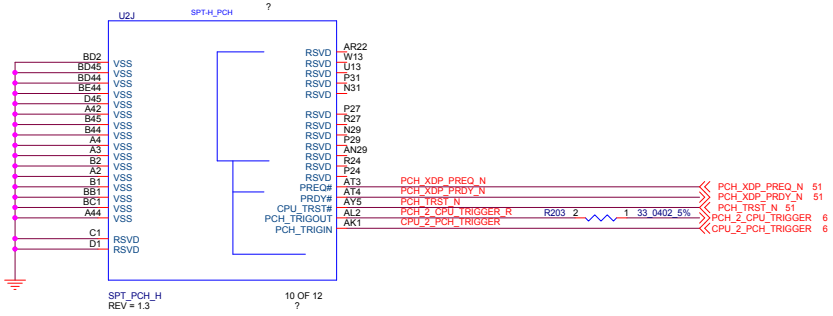

CAD Note:
CRB use 30R;DG use 0R

lenovo联想	LENOVO.CRDN	
Title: PCH-DISPLAY/RSVD		
Size: C	Document Number: Skylake-H	Rev: V0.3
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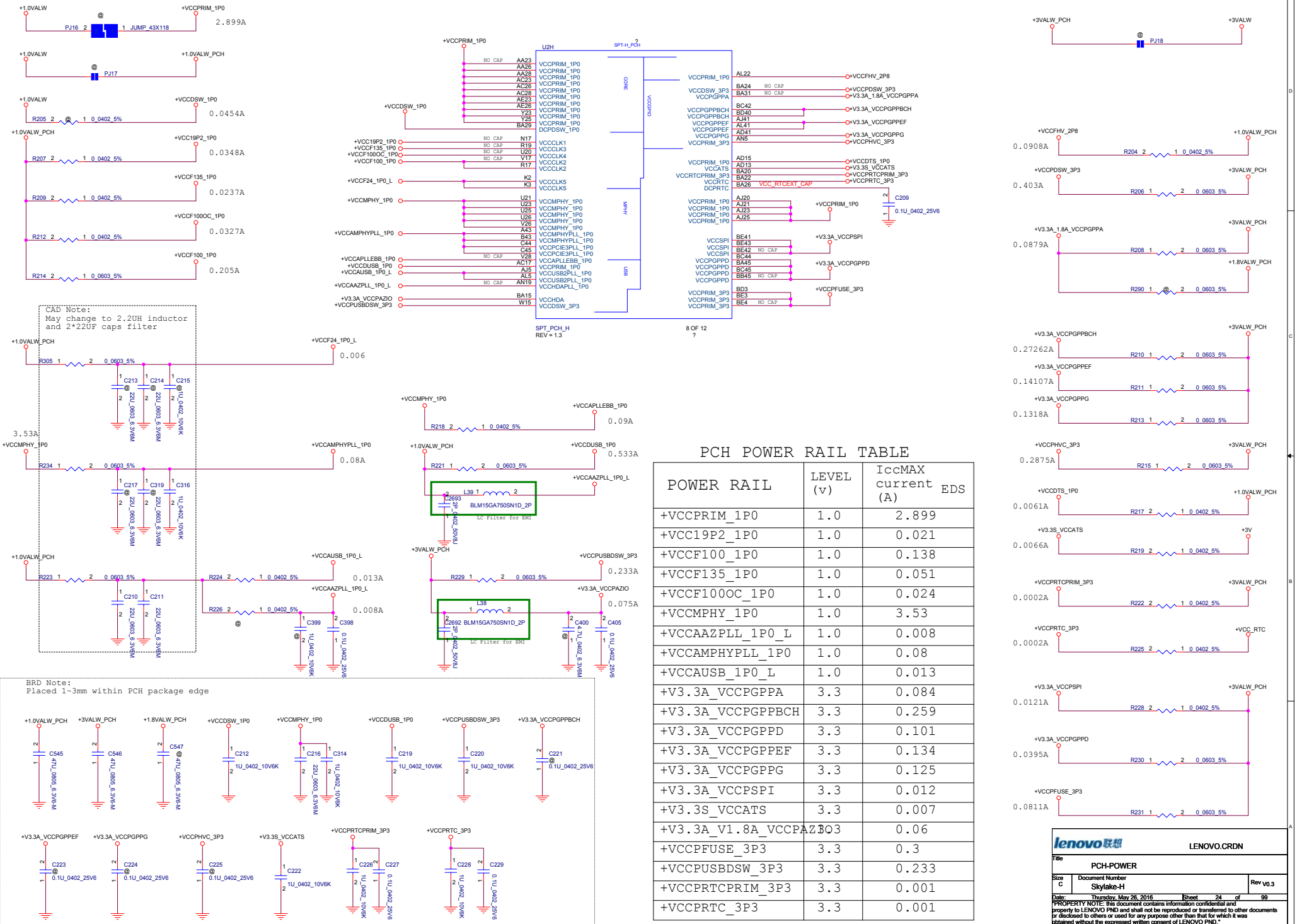

PCH POWER RAIL TABLE

POWER RAIL	LEVEL (v)	IccMAX current (A) EDS
+VCCPRIM_1P0	1.0	2.899
+VCC19P2_1P0	1.0	0.021
+VCCF100_1P0	1.0	0.138
+VCCF135_1P0	1.0	0.051
+VCCF100OC_1P0	1.0	0.024
+VCCMPHY_1P0	1.0	3.53
+VCCAAZPLL_1P0_L	1.0	0.008
+VCCAMPHYPLL_1P0	1.0	0.08
+VCCAUSB_1P0_L	1.0	0.013
+V3.3A_VCCPGPPA	3.3	0.084
+V3.3A_VCCPGPPBCH	3.3	0.259
+V3.3A_VCCPGPPD	3.3	0.101
+V3.3A_VCCPGPPEF	3.3	0.134
+V3.3A_VCCPGPPG	3.3	0.125
+V3.3A_VCCPSPI	3.3	0.012
+V3.3S_VCCATS	3.3	0.007
+V3.3A_V1.8A_VCCPAZ103	3.3	0.06
+VCCPFUSE_3P3	3.3	0.3
+VCCPUSBDSW_3P3	3.3	0.233
+VCCPRTCPRIM_3P3	3.3	0.001
+VCCPRTC_3P3	3.3	0.001

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Title: PCH-POWER

Size: C | Document Number: Skylake-H | Rev: V0.3

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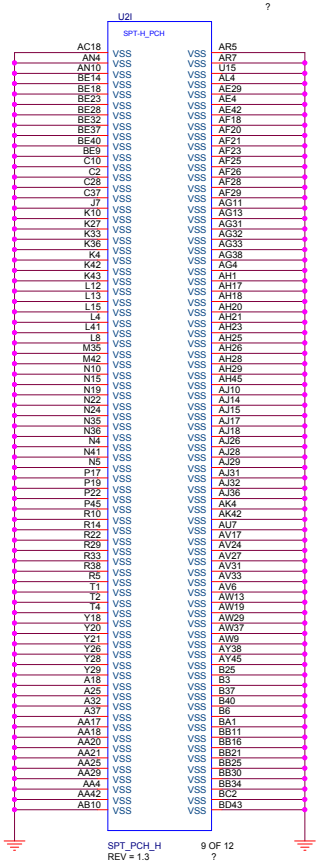

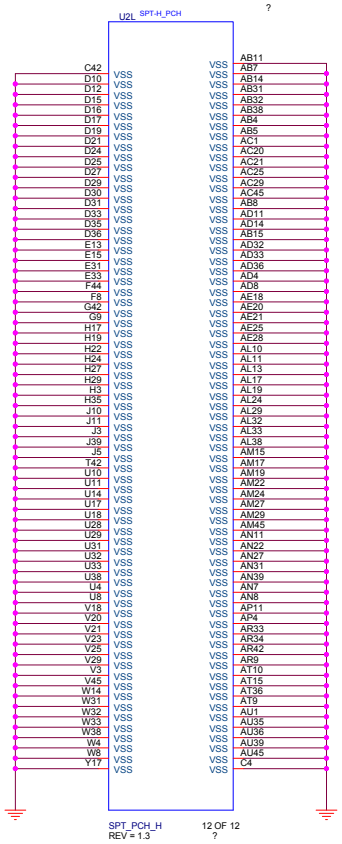

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Title: PCH-VSS

Size: C | Document Number: Skylake-H | Rev: V0.3

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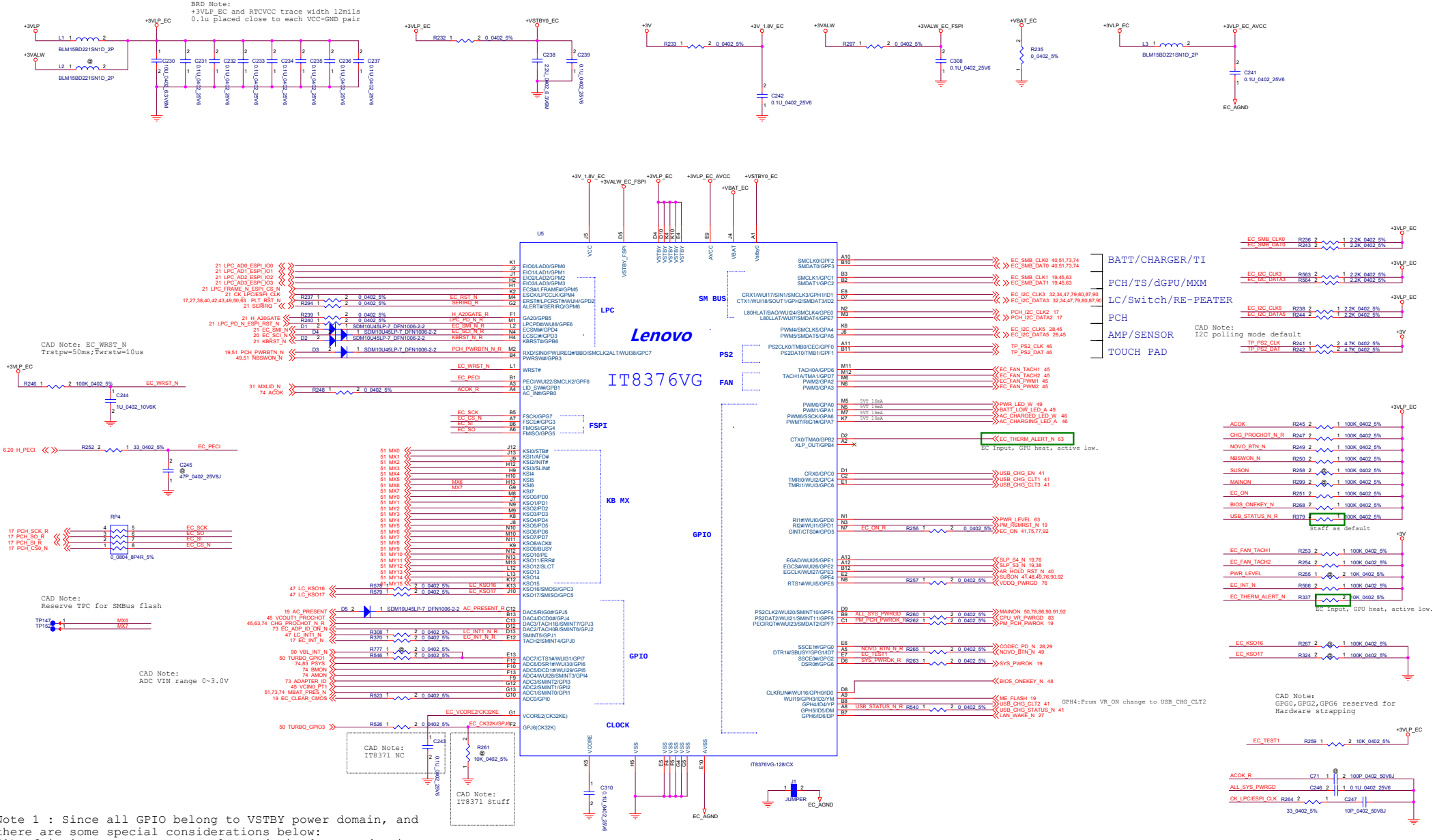
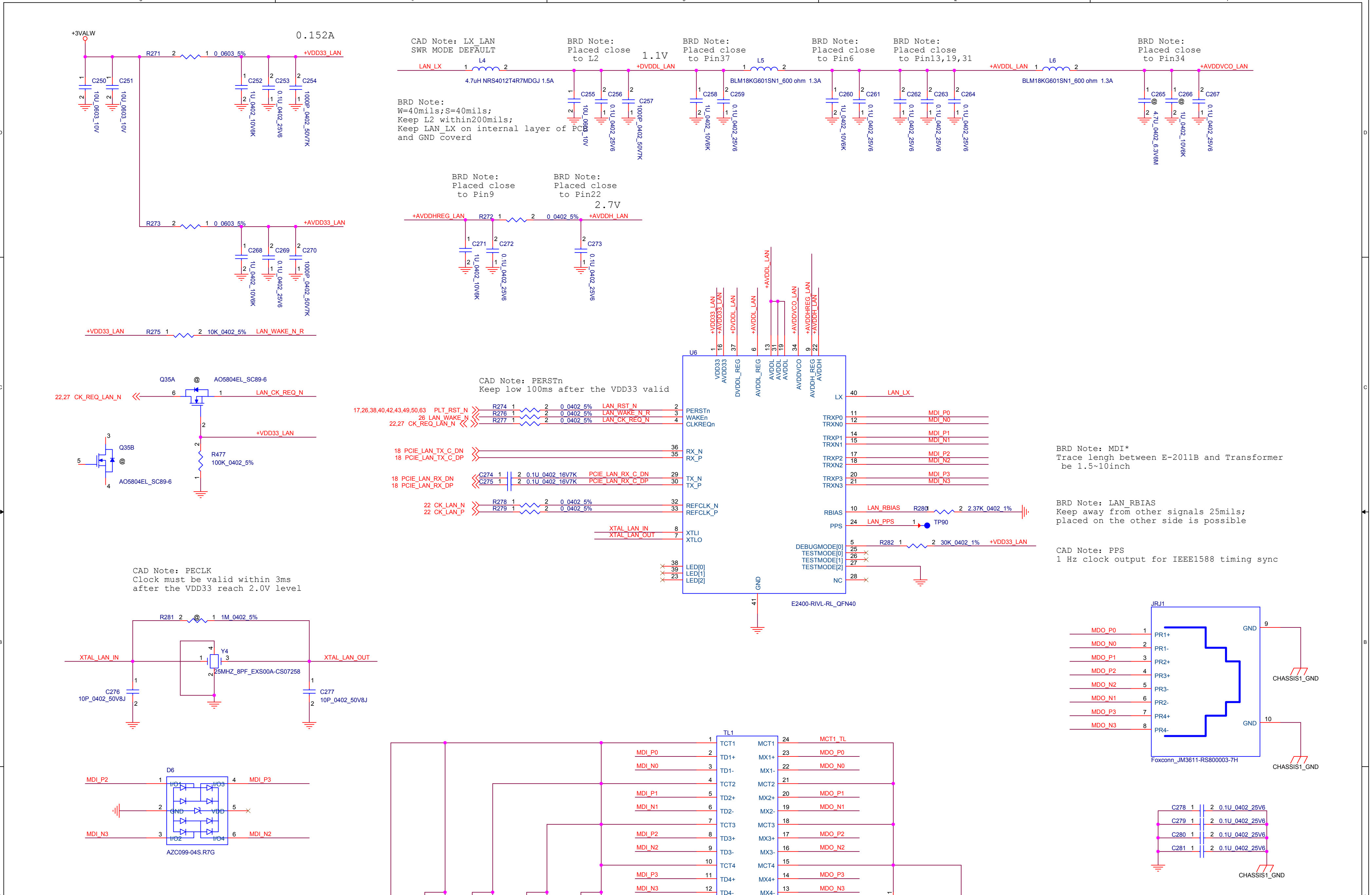


Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.



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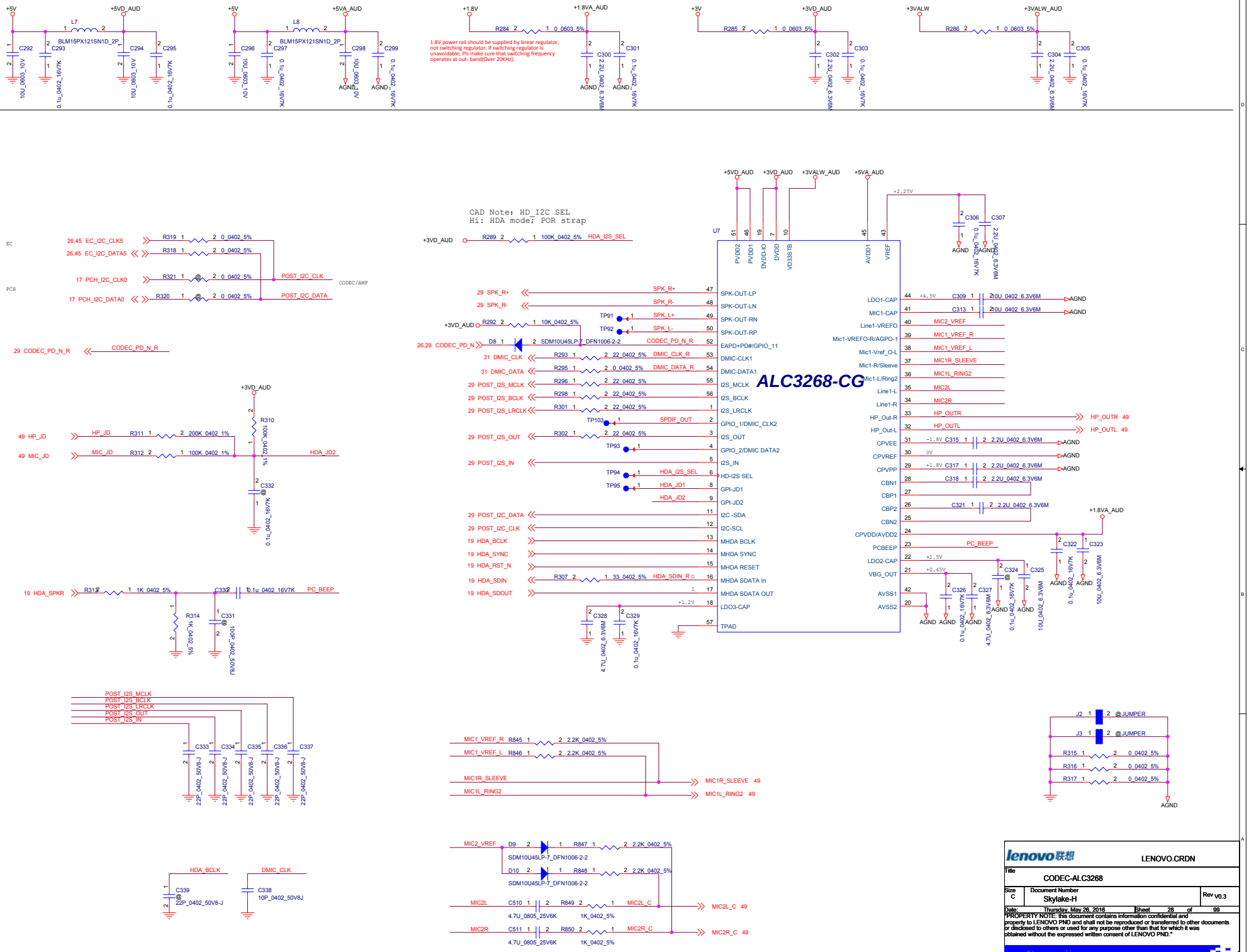
Title: LAN-E-E2400-RIVL

Size: C | Document Number: Skylake-H | Rev: V0.3

Date: Thursday, May 26, 2016 | Sheet 27 of 99


CAD Note: HD_I2C SEL
Hi: HDA mode; POR strap
ALC3268-CG
1.8V power rail should be supplied by linear regulator, not switching regulator. If switching regulator is unavoidable, Pls make sure that switching frequency operates at out- band(Over 20KHz).
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CODEC-ALC3268
Skylake-H
Rev V0.3
Thursday, May 26, 2016
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CAD Note: POST_I2C*
connect to PCH default and reserve to EC
PU at PCH or EC side

BRD Note:
placed near to Pin6&7
and Pin41&42&43 seperately

BRD Note:
Route 40 mils width and As short as possible

Internal Speaker

CAD Note: POST_I2S_MCLK
Use TAS5766M internal MCLK default

CAD Note: AMP_PD_R_N
Low active to mute,
Tr/Tf less than 20ns

I2C ADDRESS:0x 1001_100x

TAS5766M

TPA3113D2PWPR

BRD Note:
Route 40 mils width

Sub Woofer

CAD Note: SWF_GAIN[1::0]
00:Gain=20dB,RI=60k ohm(Default)
01:Gain=26dB,RI=30k ohm
00:Gain=32dB,RI=15k ohm
00:Gain=38dB,RI=9k ohm

Title	AMP
Size	C
Document Number	Skylake-H
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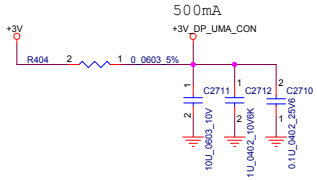
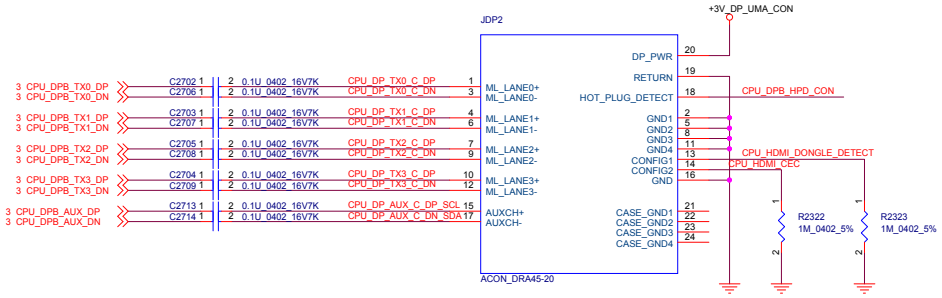
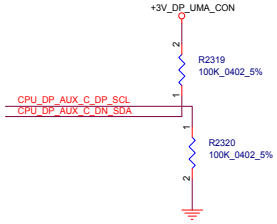
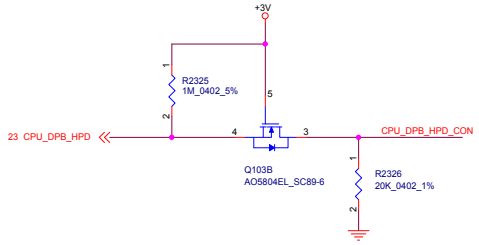
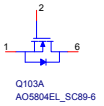




CAD Note: HDMI_DONGLE_DETECT
LOW:DP PORT ENABLED(Default)*
Hi:HDMI ENABLED







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Title: UMA DP PORT

Size	Document Number	Rev
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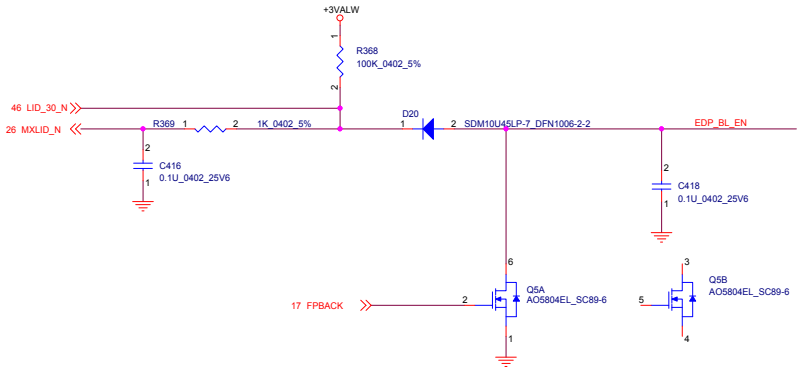
Panel Backlight Control

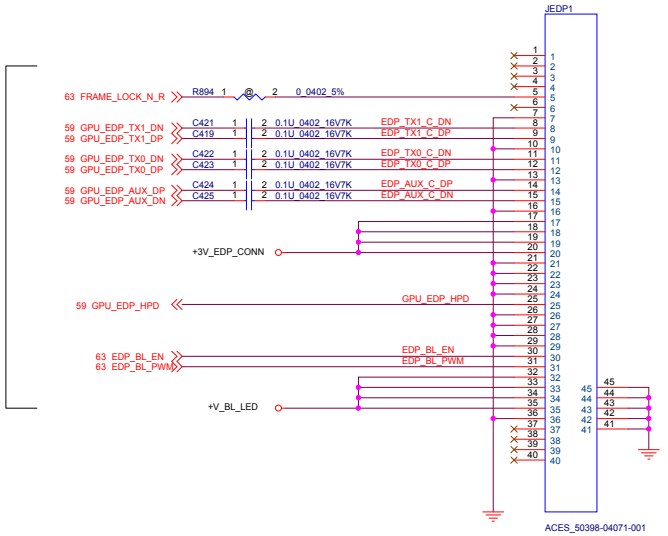


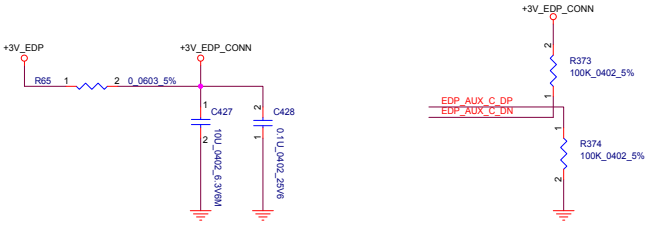
PANLE Contrl Signals

I2C Repeater

eDP/RGB sensor

eDP panel

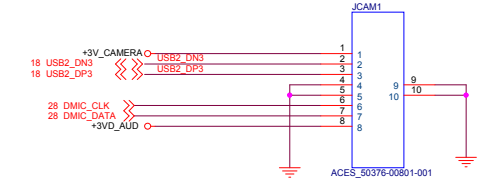


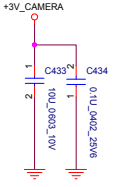


Camera/DMIC

HD camera

DMIC





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Title: eDP/RGB/CAMERA/DMIC

Size	Document Number	Rev
C	Skylake-H	V0.3

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300mA

CAD Note:
Internal pull up at ~100kΩ, 3.3V I/O.

+3V
+3V_DPA_REP
R382 2 1 0_0603_5%
C449 10U_0603_10V
C435 1U_0402_10V6K
C436 0.1U_0402_25V6
C437 0.1U_0402_25V6
C438 0.1U_0402_25V6
C439 0.1U_0402_25V6
C450 0.1U_0402_25V6

DPC_SW[1:0]=11, output swing=1000mv
Inputs with internal 100 kΩ pull-up.
This pin sets the output Voltage Level in all channel when EN12C is LOW.

DPC_FG[1:0]=10, gain=0.5db
Inputs with internal 100 kΩ pull up resistor.
Sets the output flat gain level on all channels when EN12C is low.

DPC_EQ[3:0]=0010, about 10inch,
Inputs with internal 100 kΩ pull-up.
This pins set the amount of Equalizer Boost in all channel when EN12C is LOW.
I2C Address=0xF2

DPC_I2C_RESET#:
Inputs with internal 100 kΩ pull up resistor.
Reset pin for I2C. When set low with reset the registers to default state.

DPC_I2C_DONE:
Valid register load status output, use for daisy chain master
Low = External EEPROM load failed
HIGH = External EEPROM load passed

DPC_PRSNT#:
This pin is active in both PIN mode(EN12C=LOW) and I2C mode (EN12C=HIGH).
Cable present detect input. This pin has internal 100 kΩ pull-up.
When High, a cable is not present, and the device is put in lower power mode.
When LOW, the device is enabled and in normal operation

DPA_REP_SW0 R390 2 1 4.7K_0402_5%
DPA_REP_SW1 R391 2 1 4.7K_0402_5%
DPA_REP_FG0 R392 2 1 4.7K_0402_5%
DPA_REP_FG1 R393 2 1 4.7K_0402_5%
DPA_REP_EQ0 R394 2 1 4.7K_0402_5%
DPA_REP_EQ1 R397 2 1 4.7K_0402_5%
DPA_REP_EQ2 R398 2 1 4.7K_0402_5%
DPA_REP_EQ3 R399 2 1 4.7K_0402_5%

Place BOT side.

+3V_DPA_REP
R2314 4.7K_0402_5%

U2015
PI3DPX1203ZHE-TQFN42P

58 GPU_DPA_TX0_DP C448 0.1U_0402_16V7K DPA_TX0_DP_C
58 GPU_DPA_TX0_DN C451 0.1U_0402_16V7K DPA_TX0_DN_C
58 GPU_DPA_TX1_DP C452 0.1U_0402_16V7K DPA_TX1_DP_C
58 GPU_DPA_TX1_DN C453 0.1U_0402_16V7K DPA_TX1_DN_C
58 GPU_DPA_TX2_DP C454 0.1U_0402_16V7K DPA_TX2_DP_C
58 GPU_DPA_TX2_DN C455 0.1U_0402_16V7K DPA_TX2_DN_C
58 GPU_DPA_TX3_DP C456 0.1U_0402_16V7K DPA_TX3_DP_C
58 GPU_DPA_TX3_DN C457 0.1U_0402_16V7K DPA_TX3_DN_C

DP_TX0_OUT_DP 33
DP_TX0_OUT_DN 33
DP_TX1_OUT_DP 33
DP_TX1_OUT_DN 33
DP_TX2_OUT_DP 33
DP_TX2_OUT_DN 33
DP_TX3_OUT_DP 33
DP_TX3_OUT_DN 33

DPA_REP_I2C_DONE
TESTPAD 1 TP96

DPA_REP_SW1 DPA_REP_SW0 DPA_REP_I2C_RESET# DPA_REP_FG1 DPA_REP_FG0 DPA_REP_EQ0 DPA_REP_EQ1 DPA_REP_EQ2 DPA_REP_EQ3 DPA_REP_SDA DPA_REP_SCL DPA_REP_EN12C

DPC_EN12C:
Input with internal 100 kΩ pull-up.
When LOW, each channel is programmed by the external pin voltage.
When HIGH, each channel is programmed by the data stored in the I2C bus.
When floating, master mode (Read External EEPROM)

Place BOT side.

R389 4.7K_0402_5%

Tuning by Pericom tool

+3V_DPA_REP
R2108 2 1 4.7K_0402_5% DPA_REP_SDA
R2109 2 1 4.7K_0402_5% DPA_REP_SCL
R2144 2 1 4.7K_0402_5% DPA_REP_EN12C
26,34,47,79,80,87,90 EC_I2C_CLK3 R2242 2 0_0402_5% DPA_REP_SCL
26,34,47,79,80,87,90 EC_I2C_DATA3 R2243 1 2 0_0402_5% DPA_REP_SDA

Tuning by EC

Place BOT side.

CAD Note: HDMI_DONGLE_DETECT
LOW:DP PORT ENABLED(Default)*
Hi:HDMI ENABLED

+5V
R386 4.7K_0402_5%
DPA_DDC_EN
Q6A AO5804EL_SC89-6
+3V_DPA_REP
R387 4.7K_0402_5%
DPA_DDC_AUX_SEL
Q6B AO5804EL_SC89-6
33 HDMI_DONGLE_DETECT
HDMI_DONGLE_DETECT

+3V_DPA_REP
R395 4.7K_0402_5%
Q7A AO5804EL_SC89-6
+3V_DPA_REP
R396 4.7K_0402_5%
Q7B AO5804EL_SC89-6
DPA_DDC_EN
C599 0.01U_0402_25V7K

GPU_DPA_AUX_DN_SDA R402 1 2 0_0402_5% GPU_DPA_SDA
GPU_DPA_AUX_DP_SCL R403 1 2 0_0402_5% GPU_DPA_SCL

GPU_DPA_SCL
GPU_DPA_SDA

U2016
PI3USB103ZLE-TQFN10P

58 GPU_DPA_AUX_DN_SDA C460 0.1U_0402_16V7K DPA_AUX_DN_C
58 GPU_DPA_AUX_DP_SCL C461 0.1U_0402_16V7K DPA_AUX_DP_C

DP_AUX_OUT_DN_SDA 33
DP_AUX_OUT_DP_SCL 33

R2315 4.7K_0402_5%
+3V_DPA_REP
DPA_DDC_AUX_SEL
C2715 0.1U_0402_25V6

True Table for PI3USB102G

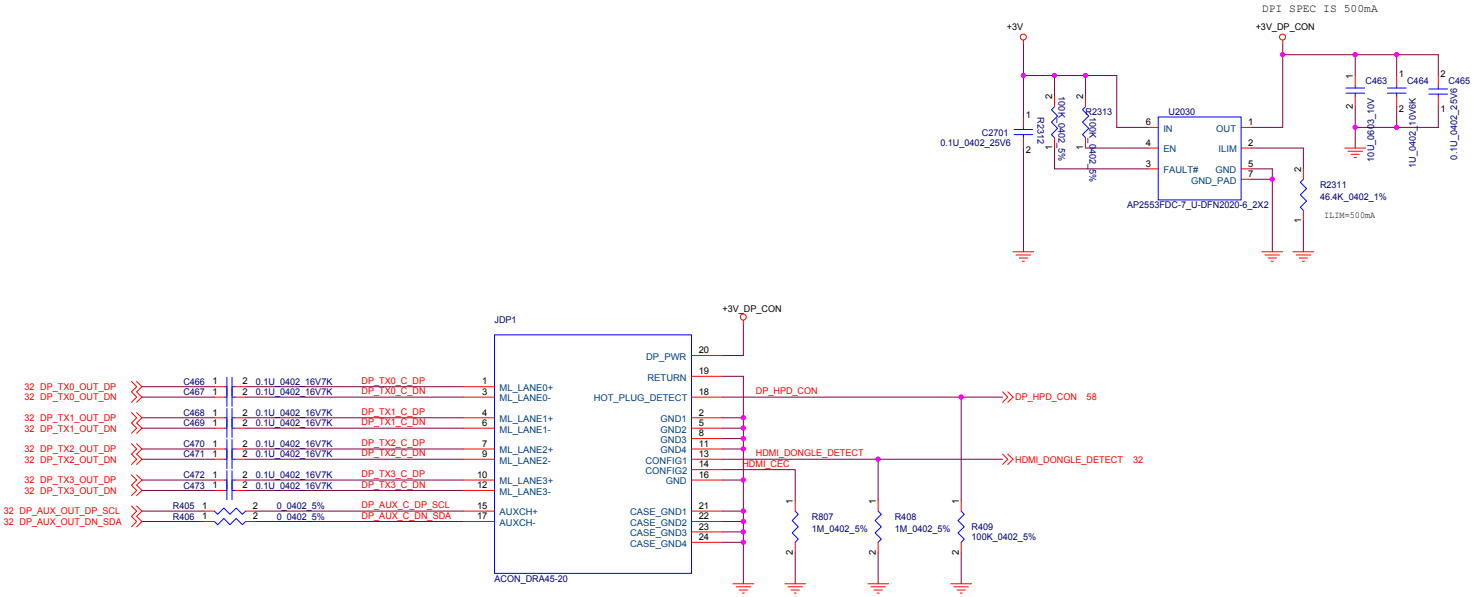
SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

lenovo联想 LENOVO.CRDN

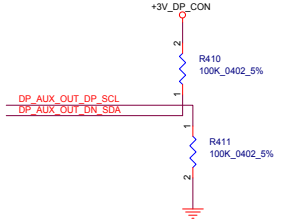
Title: DP1.3 REPEATER

Size: C | Document Number: Skylake-H | Rev: V0.3

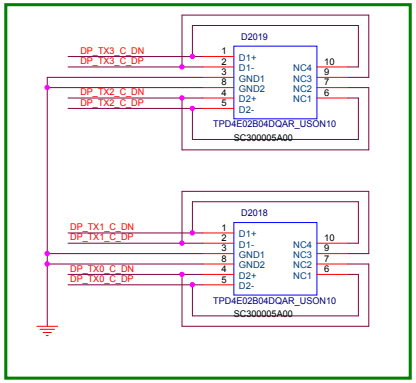
Date: Thursday, May 26, 2016 | Sheet 32 of 99



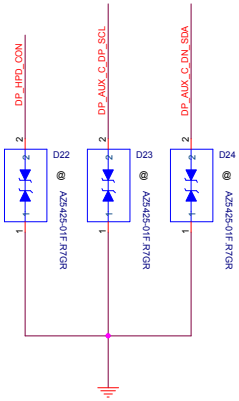
CAD Note: HDMI_DONGLE_DETECT
LOW:DP PORT ENABLED(Default)*
Hi:HDMI ENABLED



CAD Note: Reserve for ESD



CAD Note: Reserve for ESD



lenovo联想	LENOVO.CRDN	
Title: DISPLAY PORT		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Thursday, May 26, 2016	Sheet 33 of 99	

290mA

+3V

+3V_HDMI_REP

R2137 2 — 1 0_0603_5%

C2172 10U_0603_10V
C2169 1U_0402_10V6K
C2171 0.1U_0402_25V6
C2170 0.1U_0402_25V6
C2167 0.1U_0402_25V6
C2166 0.1U_0402_25V6
C2168 0.1U_0402_25V6

CAD Note:
Internal pull up at ~100kΩ, 3.3V I/O.

DE[1:0]=01, De-emphasis=3.5db
Inputs with internal 100k-Ohm Pull-Up.
This pins set the output De-Emphasis Level in all channel when Pin_Mode is HIGH.

PS[1:0]=10, Pre-shoot=3.5db
Inputs with internal 100k-Ohm Pull-Up.
This pins set the output Pre-Shoot Level in all channel when Pin_Mode is HIGH.

BST[3:0]:
Inputs with internal 100k-Ohm Pull-Up.
This pins set the amount of Equalizer Boost in all channel when Pin mode is HIGH.

PEN:(PI3HDX1204B)
Power Enable with internal 100K-Ohm Pull-Up device is enabled and in normal operation.
Reserve 4.7K PD for PI3HDX1204D.

HDMI_REP_VOD1:
Inputs with internal 100k-Ohm Pull-Up.
This pin sets the output Voltage Level in all channel when Pin mode is HIGH.

A4/A1/A0:
I2C programmable address bits, with internal 100k-Ohm Pull-Up.
I2C Address=0xC2

HDMI_REP_SW0 — R2123 2 — @ — 1 4.7K_0402_5%
HDMI_REP_SW1 — R2138 2 — 1 4.7K_0402_5%
HDMI_REP_FG0 — R2140 2 — 1 4.7K_0402_5%
HDMI_REP_FG1 — R2139 2 — @ — 1 4.7K_0402_5%
HDMI_REP_EQ0 — R2141 2 — 1 4.7K_0402_5%
HDMI_REP_EQ1 — R2142 2 — @ — 1 4.7K_0402_5%
HDMI_REP_EQ2 — R2125 2 — 1 4.7K_0402_5%
HDMI_REP_EQ3 — R2126 2 — 1 4.7K_0402_5%
HDMI_REP_VOD1 — R2238 2 — 1 4.7K_0402_5%
HDMI_REP_I2C_DONE_A0 — R2239 2 — @ — 1 4.7K_0402_5%
HDMI_REP_A1_VTH1 — R2236 2 — 1 4.7K_0402_5%
HDMI_REP_A4_VTH0 — R2237 2 — 1 4.7K_0402_5%

Place BOT side.

+3V_HDMI_REP

R2316 2 — @ — 1 4.7K_0402_5%

U2019 PI3HDX1204BZHE-TQFN42P

VDD 3, 9, 15, 24, 33, 36
GND 6, 12, 30, 43
HGND 20
PEN

AC couping cap @ GPU side, and place close to U2019.

59 GPU_HDMI_DATA2_DP	GPU_HDMI_DATA2_DP 4	A0RX+	A0TX+ 35 HDMI_DATA2_DP — HDMI_DATA2_DP 35
59 GPU_HDMI_DATA2_DN	GPU_HDMI_DATA2_DN 5	A0RX-	A0TX- 34 HDMI_DATA2_DN — HDMI_DATA2_DN 35
59 GPU_HDMI_DATA1_DP	GPU_HDMI_DATA1_DP 7	A1RX+	A1TX+ 32 HDMI_DATA1_DP — HDMI_DATA1_DP 35
59 GPU_HDMI_DATA1_DN	GPU_HDMI_DATA1_DN 8	A1RX-	A1TX- 31 HDMI_DATA1_DN — HDMI_DATA1_DN 35
59 GPU_HDMI_DATA0_DP	GPU_HDMI_DATA0_DP 10	A2RX+	A2TX+ 29 HDMI_DATA0_DP — HDMI_DATA0_DP 35
59 GPU_HDMI_DATA0_DN	GPU_HDMI_DATA0_DN 11	A2RX-	A2TX- 28 HDMI_DATA0_DN — HDMI_DATA0_DN 35
59 GPU_HDMI_CLK_DP	GPU_HDMI_CLK_DP 13	A3RX+	A3TX+ 26 HDMI_CLK_DP — HDMI_CLK_DP 35
59 GPU_HDMI_CLK_DN	GPU_HDMI_CLK_DN 14	A3RX-	A3TX- 25 HDMI_CLK_DN — HDMI_CLK_DN 35
	HDMI_REP_A1_VTH1 16	DNC	DNC 23 HDMI_REP_VOD1
	HDMI_REP_A4_VTH0 17	DNC	I2C_DONE 22 HDMI_REP_I2C_DONE_A0

SW1 1, SW0 2, FG1 37, FG0 38, EQ3 39, EQ2 41, EQ1 40, EQ0 42, RESET# 27, EN2C 21, SDA 18, SCL 19

Pin_Mode:(PI3HDX1204BZHE)
Input with internal 100k-Ohm Pull-Up.
When HIGH, each channel is programmed by the external pin voltage.
When LOW, each channel is programmed by the data stored in the I2C bus.

Place BOT side.

R2122 — @ — 1 4.7K_0402_5%

Tuning by pericom tool

+3V_HDMI_REP

R2130 2 — @ — 1 4.7K_0402_5% — HDMI_REP_SDA
R2131 2 — @ — 1 4.7K_0402_5% — HDMI_REP_SCL
R2143 2 — 1 4.7K_0402_5% — HDMI_REP_EN2C

26,32,47,79,80,87,90 EC_I2C_CLK3 — R2240 1 — 2 0_0402_5% — HDMI_REP_SCL
26,32,47,79,80,87,90 EC_I2C_DATA3 — R2241 1 — 2 0_0402_5% — HDMI_REP_SDA

Tuning by EC

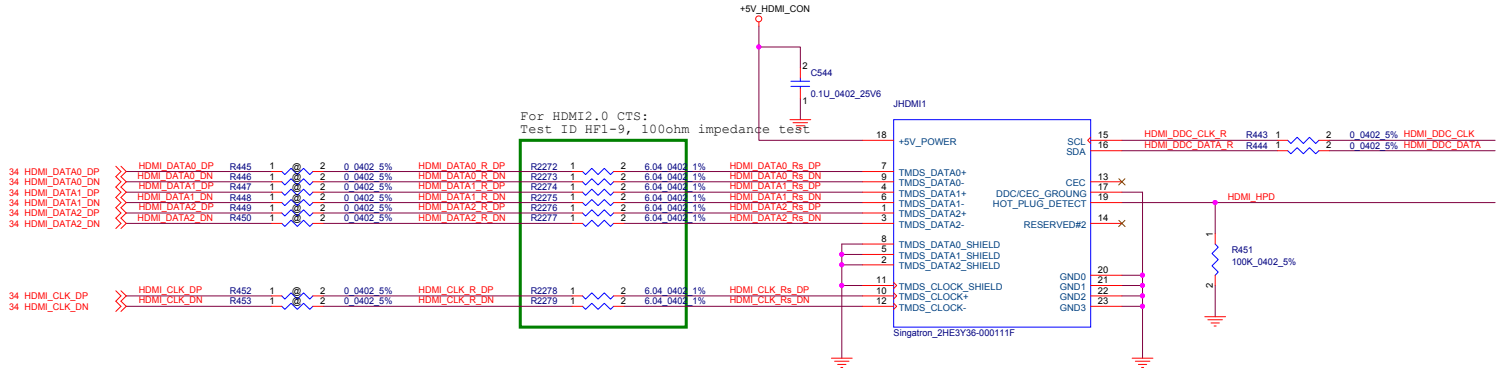
Place BOT side.

lenovo联想 LENOVO.CRDN

Title: HDMI2.0 REPEATER

Size: C | Document Number: Skylake-H | Rev: V0.3

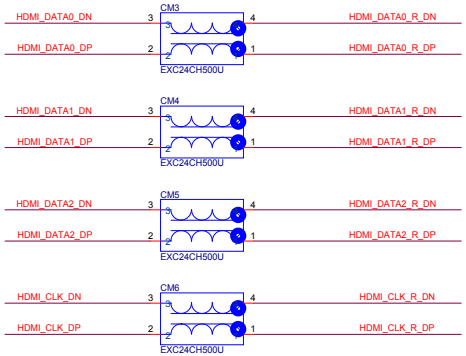
Date: Thursday, May 26, 2016 | Sheet 34 of 99



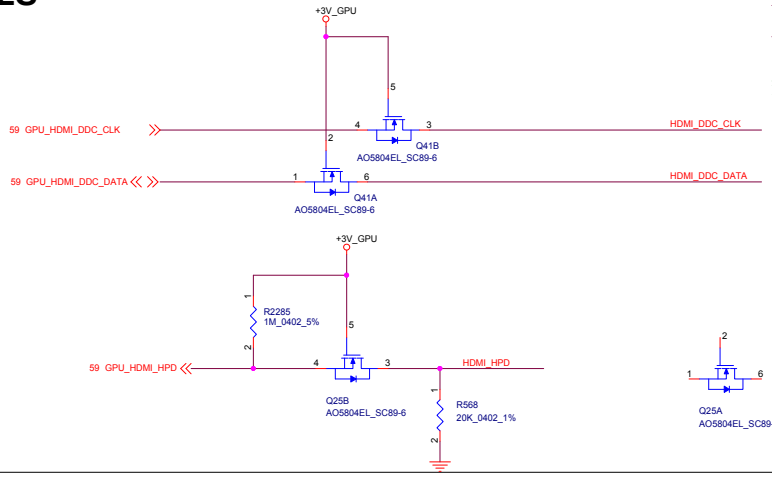
CM

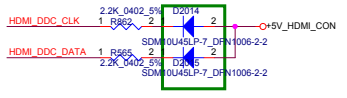
BRD Note: Co-lay with R

CAD Note: Reserve for EMI

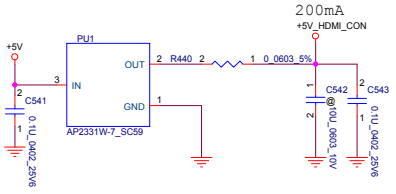


LS



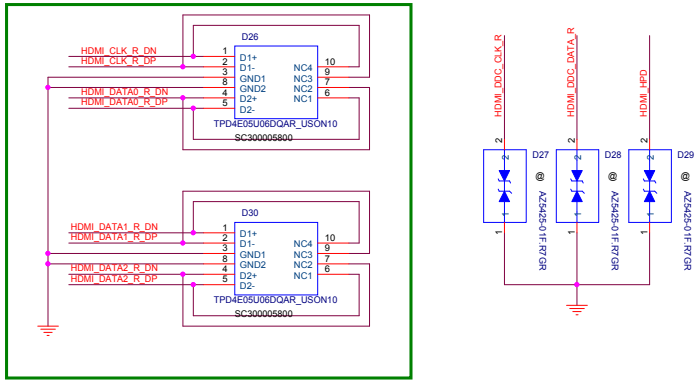


Power switch

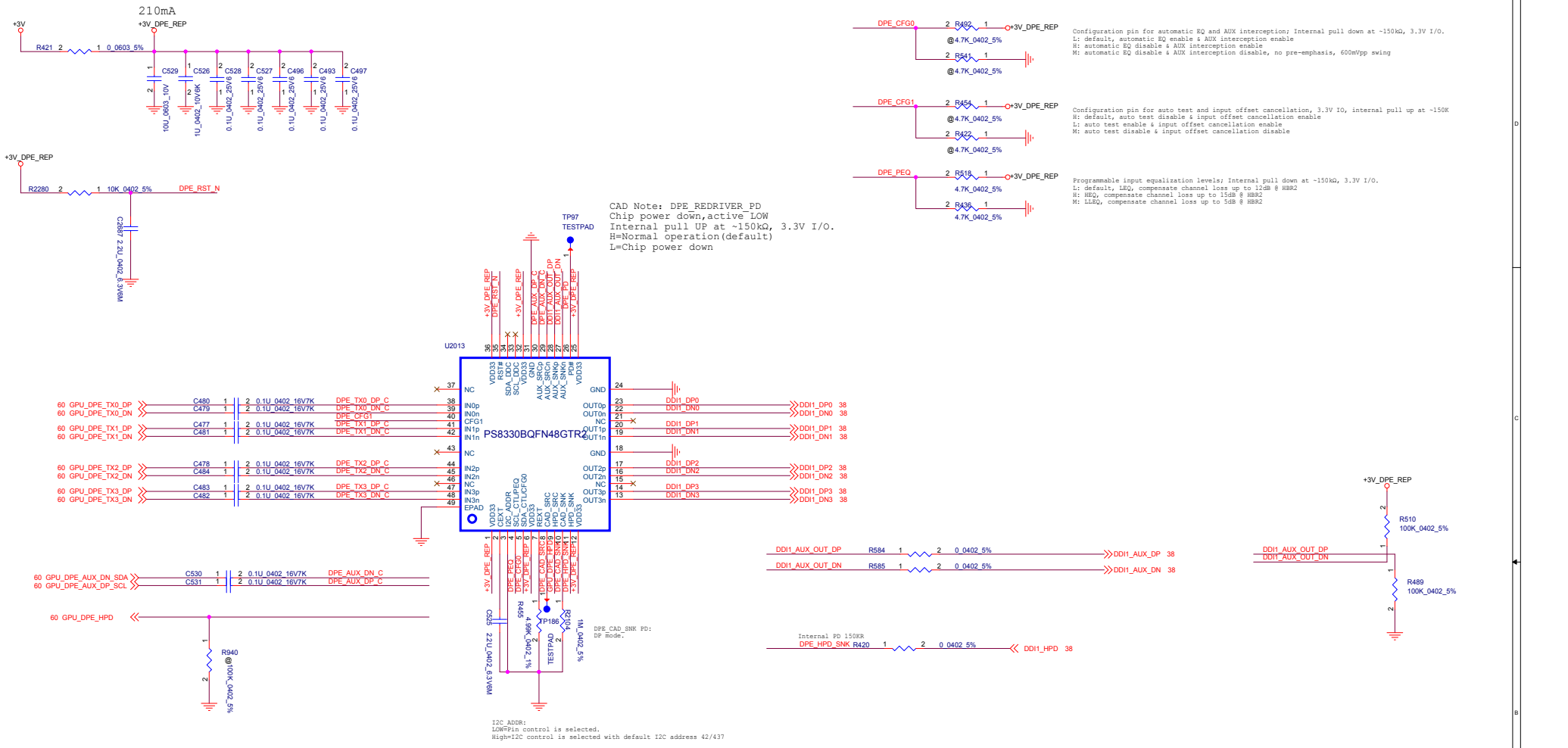


ESD

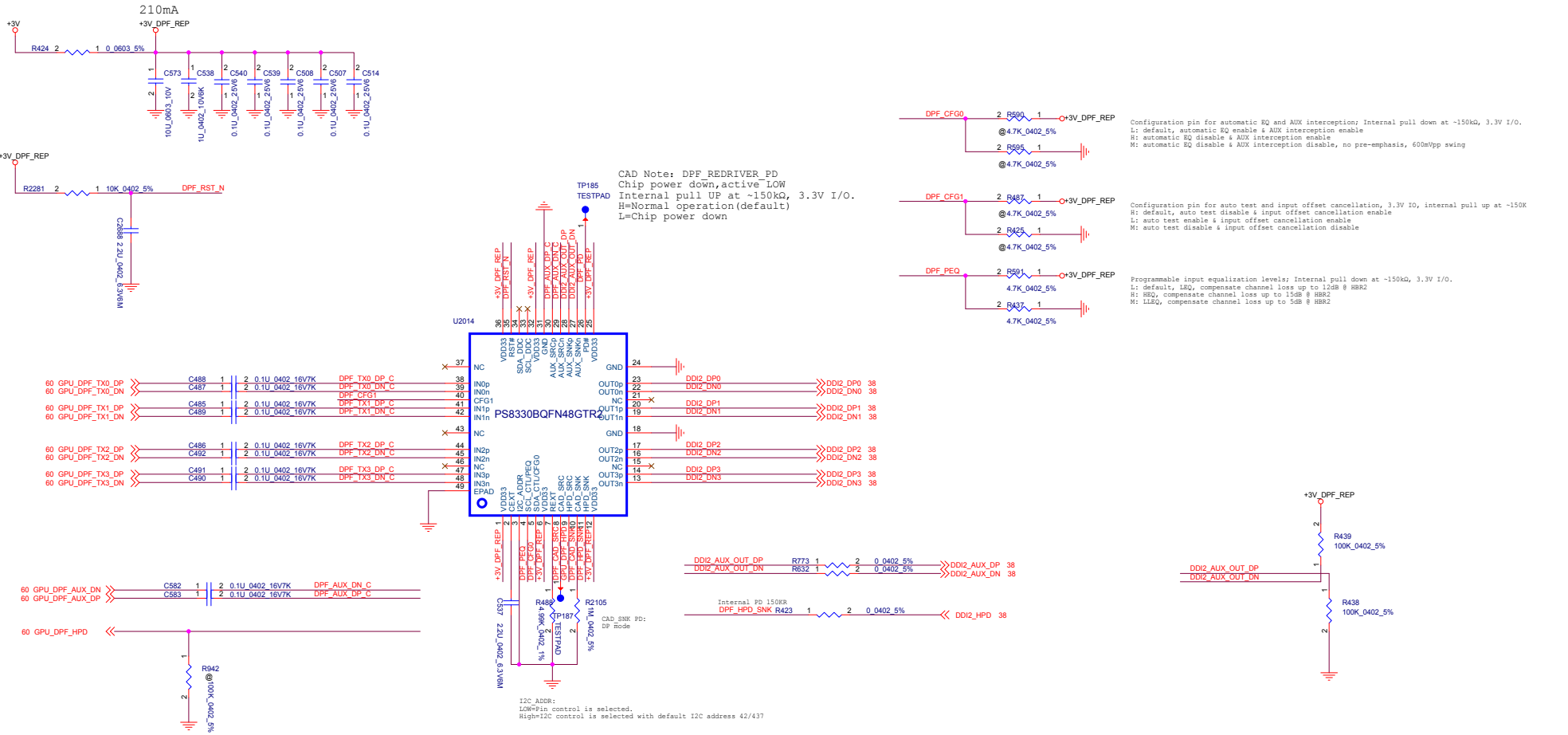
CAD Note: Reserve for ESD



lenovo联想	LENOVO.CRDN	
Title: HDMI CONN,		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Thursday, May 26, 2016	Sheet 35 of 99	



lenovo联想	LENOVO.CRDN	
Title	AR DP REPEATER-1	
Size C	Document Number Skylake-H	Rev V0.3
Date: Thursday, May 26, 2016	Sheet 36 of 99	



Automatic Power Down

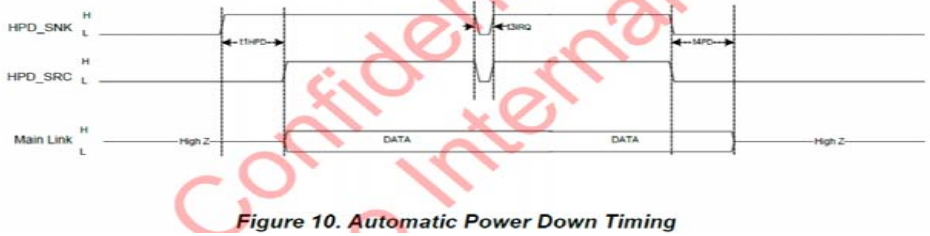


Figure 10. Automatic Power Down Timing

Parameter	Test Conditions	Min	Typ	Max	Unit
Switching Timing (Figures 10)					
$t1_{HPD}$ Propagation delay of HPD_SNK assertion at Power Down Mode to HPD_SRC assertion		100		400	ms
$t3_{IRQ}$ HPD pulse duration when treated as an IRQ				2	ms
$t4_{PD}$ Power down delay from HPD_SNK de-assertion to chip power down		400		1600	ms

lenovo联想 LENOVO.CRDN

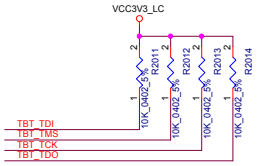
Title: AR DP MUX-2

Size: C | Document Number: Skylake-H | Rev: V0.3

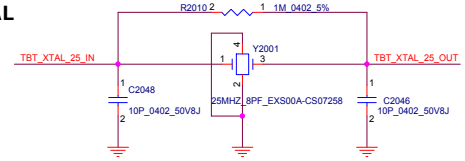
Date: Thursday, May 26, 2016 | Sheet 37 of 99

AR-DP TYPE C +USB 3.1 (3.0)

JTAG

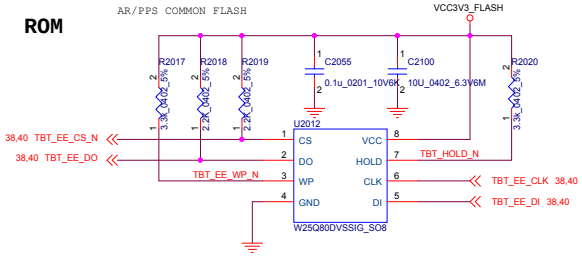


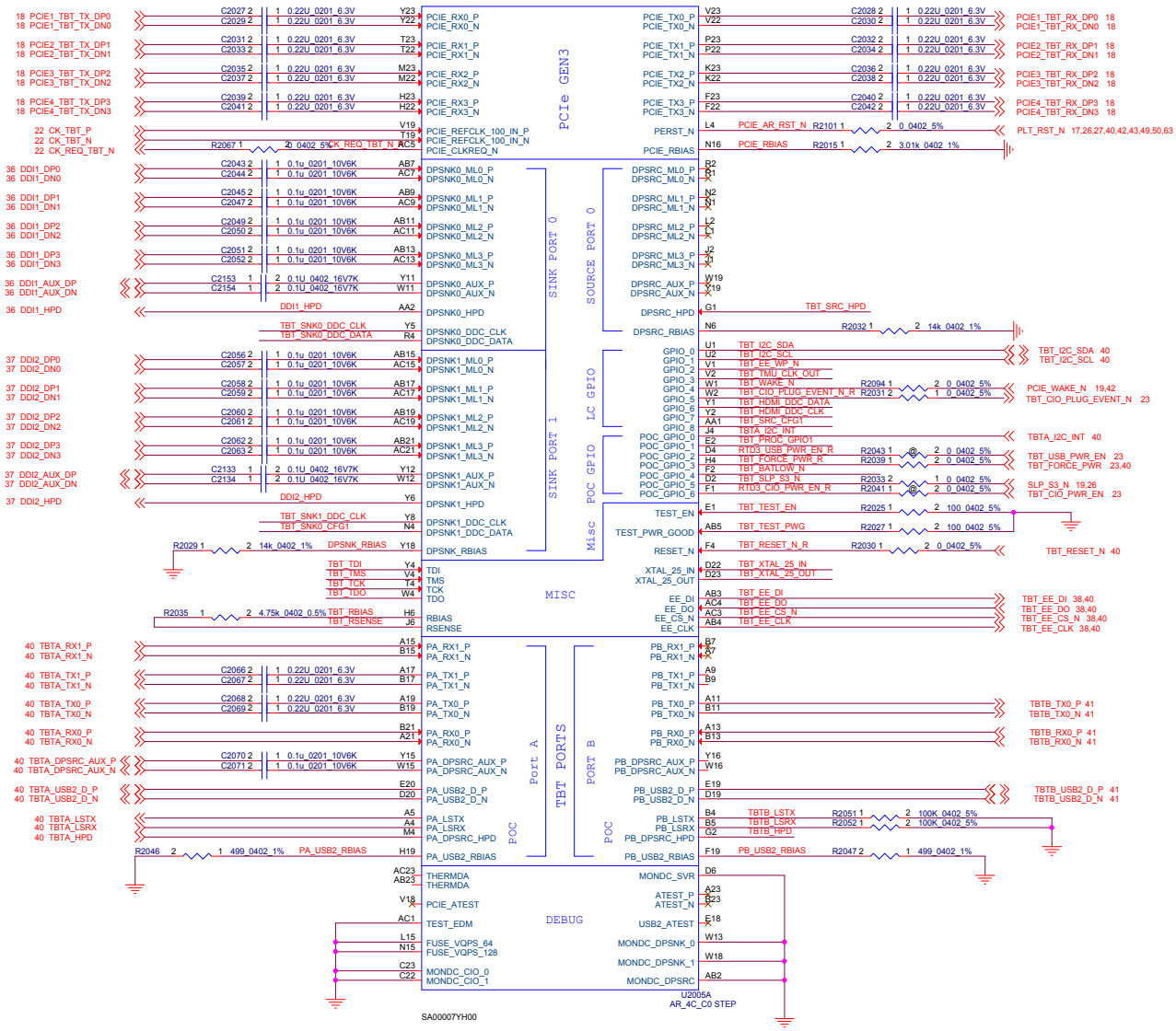
XTAL



GPIO

ROM





IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:

GPIO	TERMINATION	Power Rail
GPIO_0	10K PU	VCC3V3_LC
GPIO_1	10K PU	VCC3V3_LC
GPIO_2	3.3K PU	
GPIO_3	100k PD	
GPIO_4	10K PU	VCC3V3_LC
GPIO_5	10K PU	VCC3V3_LC
GPIO_6	100K PD	SRC NOT USED
GPIO_7	100K PD	SRC NOT USED
GPIO_8	1M PD	SRC NOT USED
POC_GPIO_0	10K PU	VCC3V3_TBT_SX
POC_GPIO_1	10K PU	VCC3V3_TBT_SX
POC_GPIO_2	100K PD	
POC_GPIO_3	10K PD	
POC_GPIO_4	10K PU	VCC3V3_TBT_SX
POC_GPIO_5	10K PU	VCC3V3_TBT_SX
POC_GPIO_6	100K PD	

DEBUG PINs:

PIN	TERMINATION
MONDC_SVR	GND
MONDC_DPSNK_0	GND
MONDC_DPSNK_1	GND
MONDC_DPSRC	GND
MONDC_CIO_0	GND
MONDC_CIO_1	GND
TEST_EDM	GND
FUSE_VQPS_64	GND
FUSE_VQPS_128	GND
ATEST_P/N	FLOATING
USB2_ATEST	FLOATING
PCIE_ATEST	FLOATING

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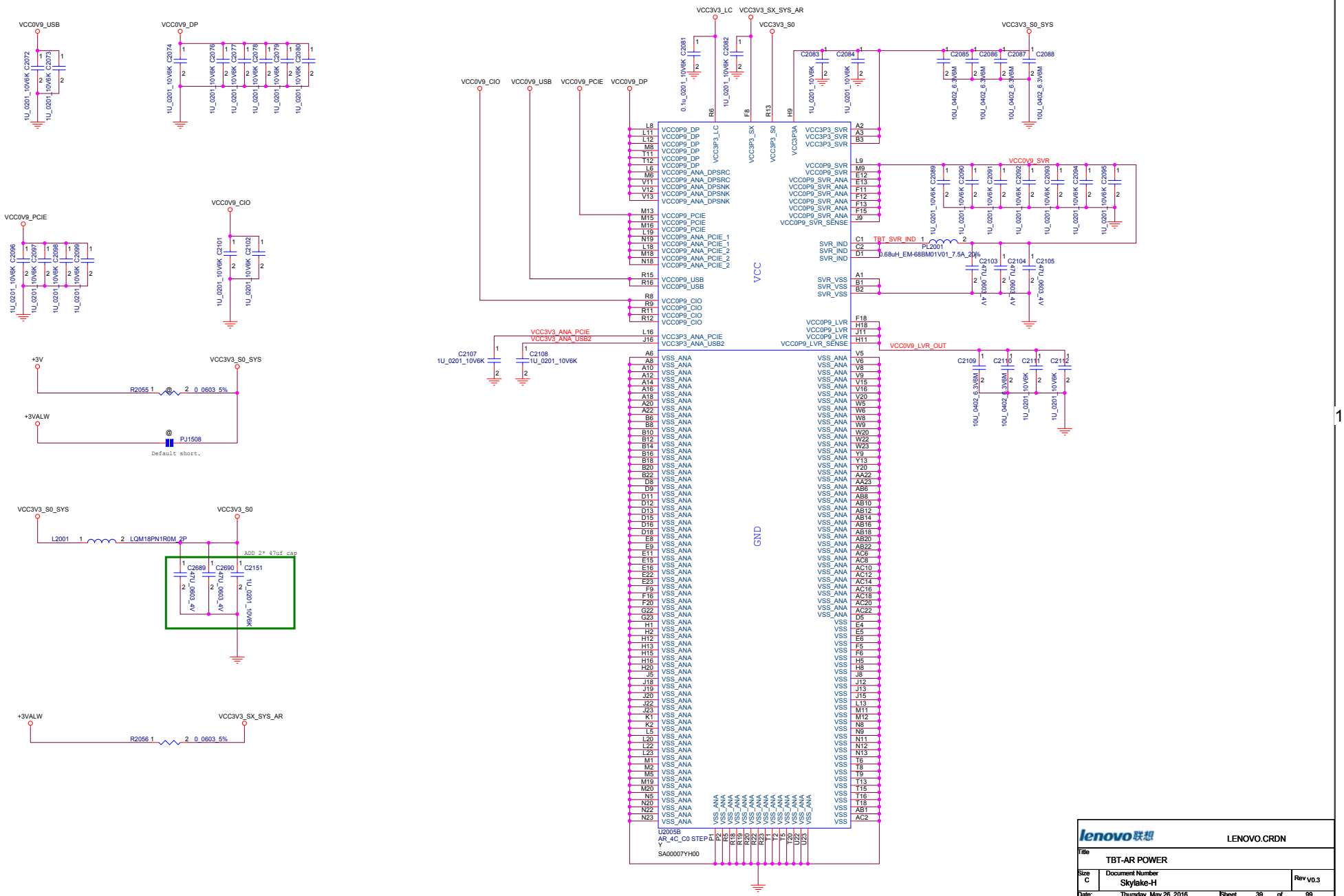
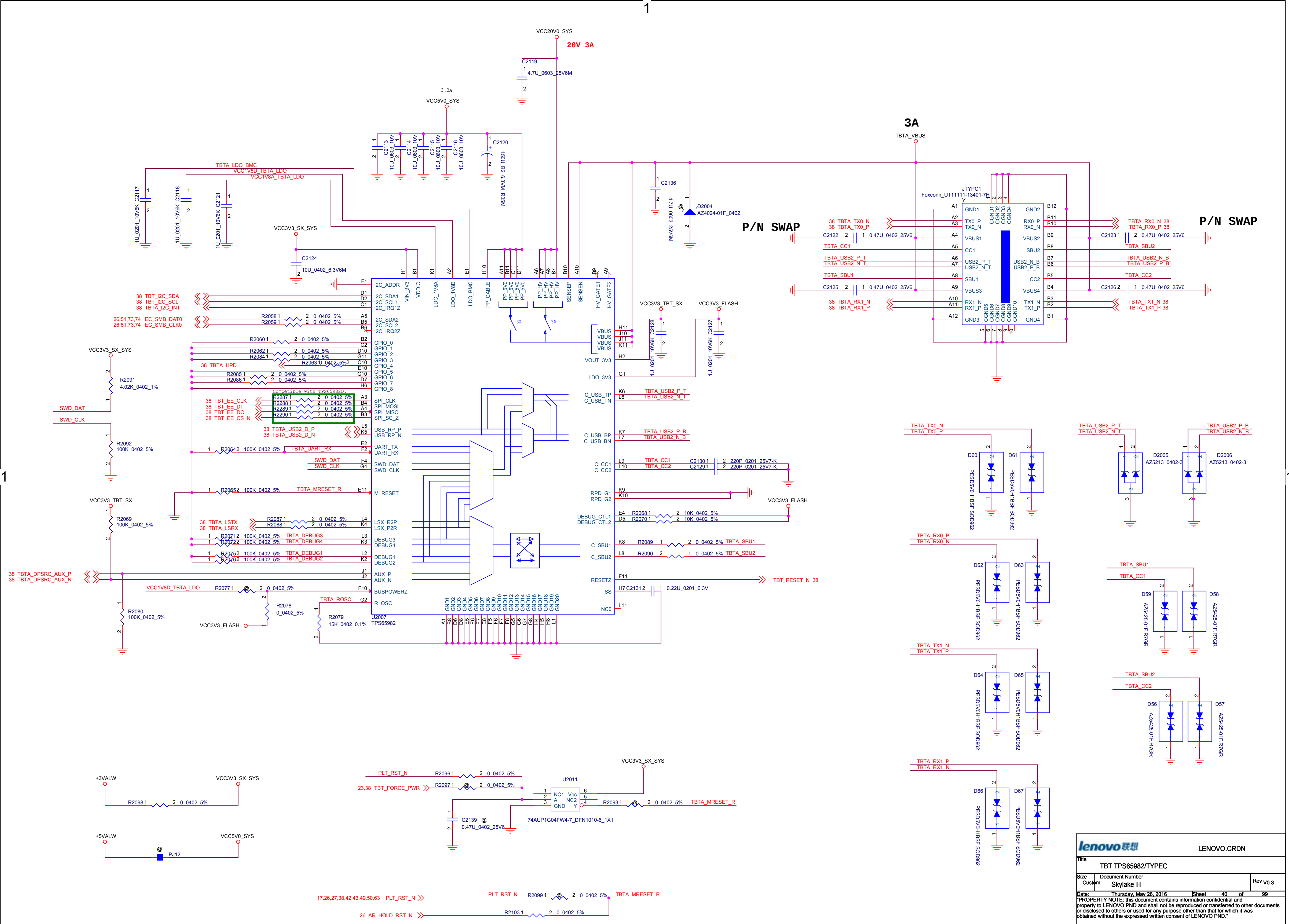
Title: DDI redriver PS8330

Size: C | Document Number: Skylake-H | Rev V0.3

Date: Thursday, May 26, 2016 | Sheet 38 of 99





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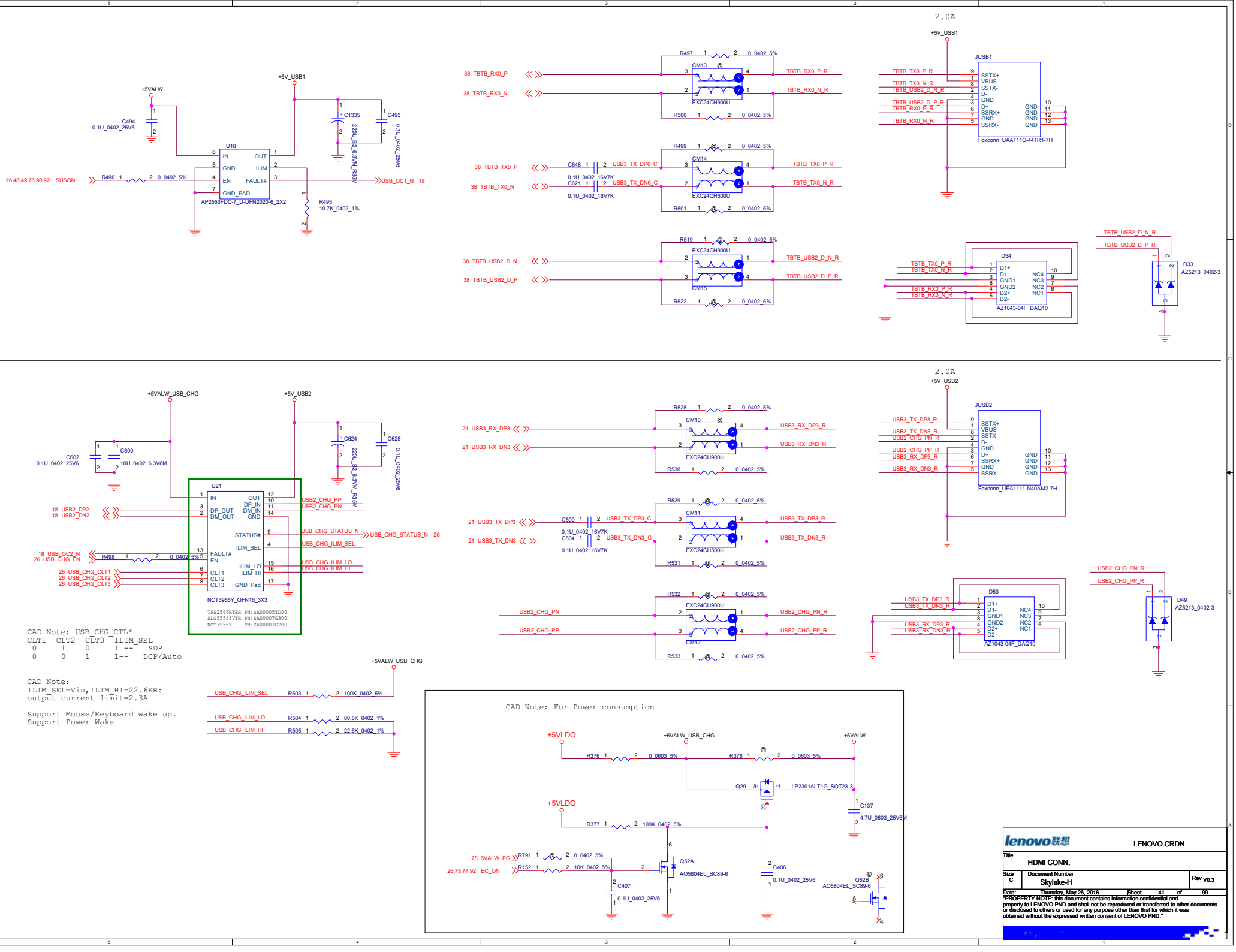
Title: TBT TPS65982/TYPEC

Size	Document Number	Rev
Custom	Skylake-H	V0.3

Date: Thursday, May 26, 2016 Sheet 40 of 99


2.0A
+5V_USB1
JUSB1
Foxconn_UAA111C-441R1-7H
AZ1043-04F_DAQ10
D54
D33
AZ5213_0402-3
+5VALW
+5V_USB1
U18
AP2553FDC-7_U-DFN2020-6_2X2
C494
C1335
C495
R496
R495
10.7K_0402_1%
R497
R499
R501
R500
CM13
CM14
CM15
EXC24CH900U
EXC24CH500U
C648
C621
0.1U_0402_16V7K
R519
R522
TBTB_RX0_P
TBTB_RX0_N
TBTB_TX0_P
TBTB_TX0_N
TBTB_USB2_D_N
TBTB_USB2_D_P
USB3_TX_DP6_C
USB3_TX_DN6_C
SUSON
USB_OC1_N
+5V_USB2
JUSB2
Foxconn_UEA1111-N40AM2-7H
D53
D49
AZ5213_0402-3
U21
NCT3955Y_QFN16_3X3
C602
C600
10U_0402_6.3V6M
C624
C625
0.1U_0402_25V6
220U_B2_6.3VM_R35M
R498
R528
R530
R529
R531
R532
R533
CM10
CM11
CM12
USB3_RX_DP3
USB3_RX_DN3
USB3_TX_DP3
USB3_TX_DN3
USB2_CHG_PN
USB2_CHG_PP
C500
C504
USB_CHG_STATUS_N
USB_CHG_ILIM_SEL
USB_CHG_ILIM_LO
USB_CHG_ILIM_HI
+5VALW_USB_CHG
R503
R504
R505
100K_0402_5%
80.6K_0402_1%
22.6K_0402_1%
CAD Note: USB_CHG_CTL*
CLT1 CLT2 CLT3 ILIM_SEL
0 1 0 1 -- SDP
0 0 1 1-- DCP/Auto
CAD Note:
ILIM_SEL=Vin,ILIM_HI=22.6KR:
output current limit=2.3A
Support Mouse/Keyboard wake up.
Support Power Wake
CAD Note: For Power consumption
+5VLDO
R376
R378
Q29
LP2301ALT1G_SOT23-3
C137
4.7U_0603_25V6M
R377
R791
R152
Q52A
Q52B
AO5804EL_SC89-6
C406
C407
0.1U_0402_25V6
75 5VALW_PG
26,75,77,92 EC_ON
lenovo联想
LENOVO.CRDN
Title
HDMI CONN,
Size C
Document Number
Skylake-H
Rev V0.3
Date: Thursday, May 26, 2016
Sheet 41 of 99
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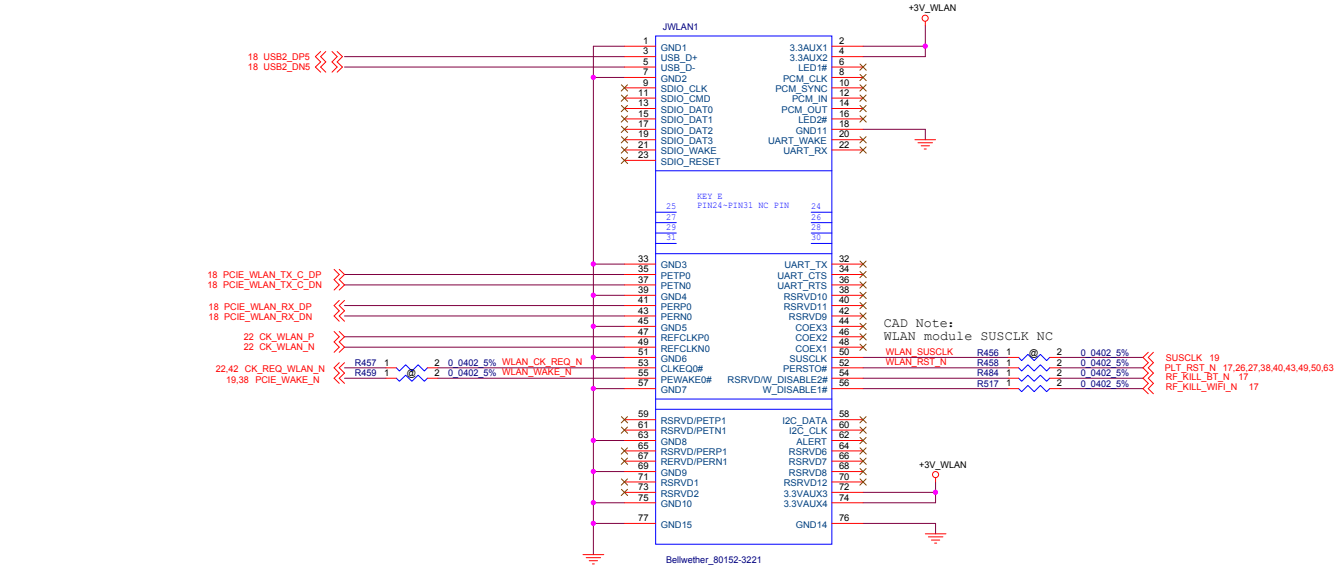

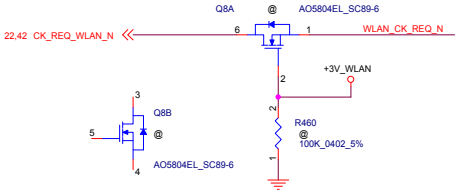

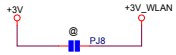

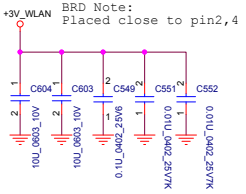

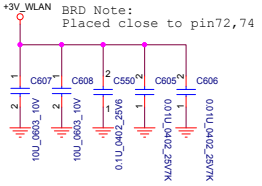

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Title: NGFF WLAN

Size	Document Number	Rev
C	Skylake-H	V0.3

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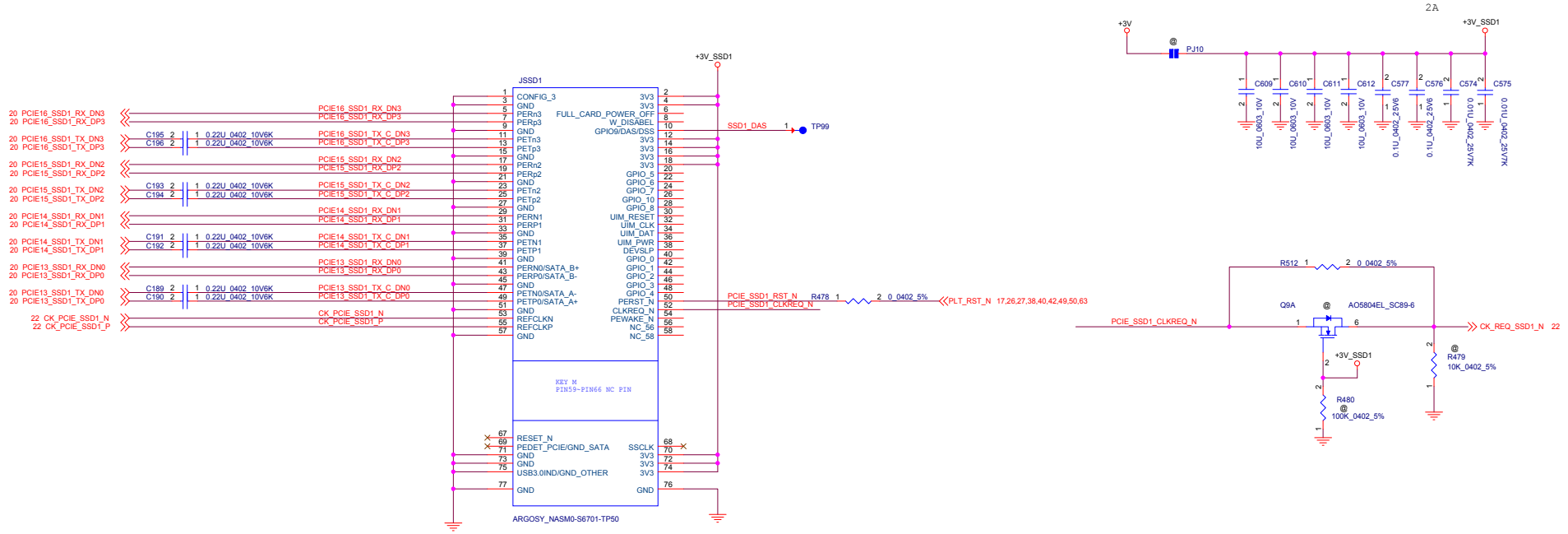
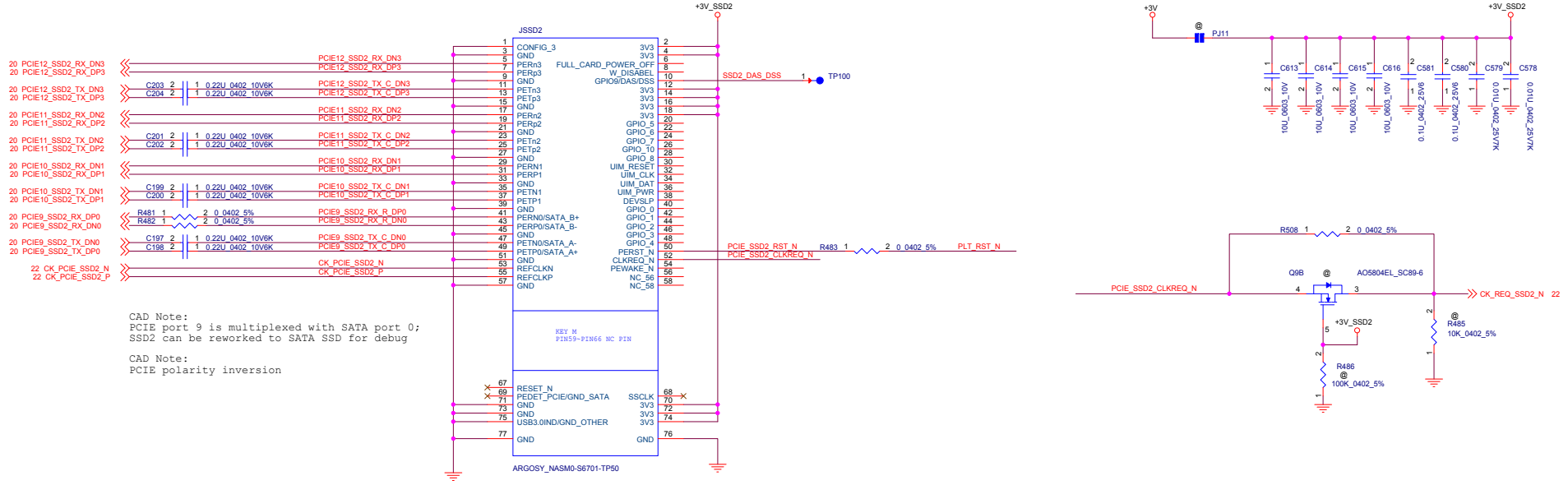




CAD Note:
PCIE port 9 is multiplexed with SATA port 0;
SSD2 can be reworked to SATA SSD for debug

CAD Note:
PCIE polarity inversion

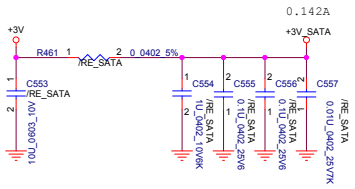
lenovo联想 LENOVO.CRDN

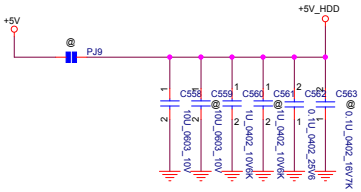
Title: NGFF SSD

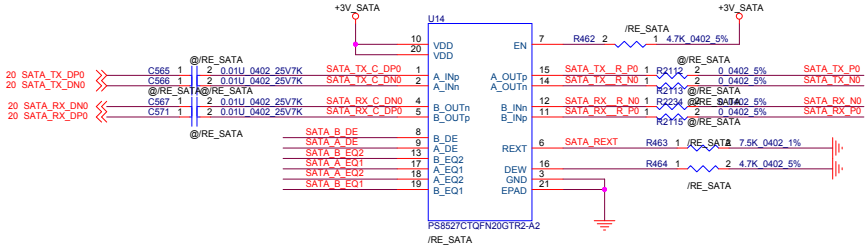
Size	Document Number	Rev
C	Skylake-H	V0.3

Date: Thursday, May 26, 2016 Sheet 43 of 99

CAD Note: PS8527A VDD
1.2V/1.35V/1.5V

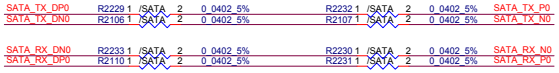






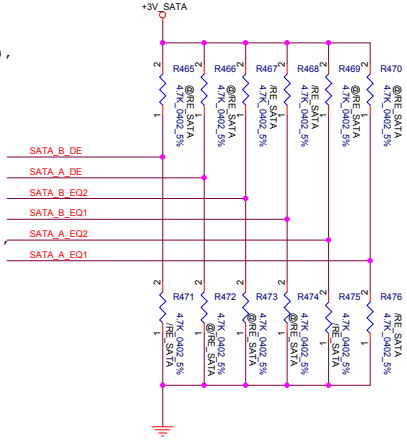
CAD Note:
SATA_REXT=7.5KR:
Vtx_diff=700 mV

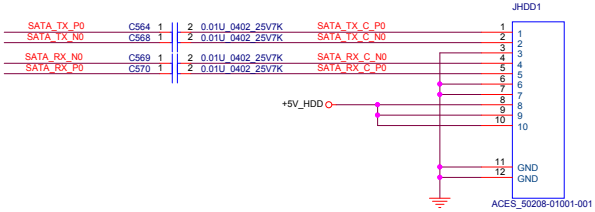
CAD Note: SATA_DEW
L:For SATA Gen3
H:For SATA Gen2



CAD Note: SATA_x_DE
De-emphasis level setting for channel x(x=A,B),
internally tied to VDD/2
[A_DE,B_DE]=M,L
M:-3.5dB
L: 0dB
H: -6dB

CAD Note: SATA_x_EQ
Equalization level setting for channel x(x=A,B),
internally tied to VDD/2
[x_EQ2,x_EQ1]=
L/M: for channel loss up to 2.4dB
L/L: for channel loss up to 7.4dB(CH A)
L/H: for channel loss up to 14.4dB
M/M: for channel loss up to 12.2dB
M/L: for channel loss up to 9.4dB
M/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB(CH B)





lenovo联想	LENOVO.CRDN	
Title: SATA HDD		
Size: C	Document Number: Skylake-H	Rev: V0.3
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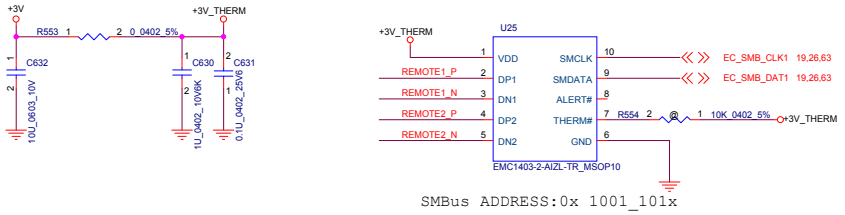
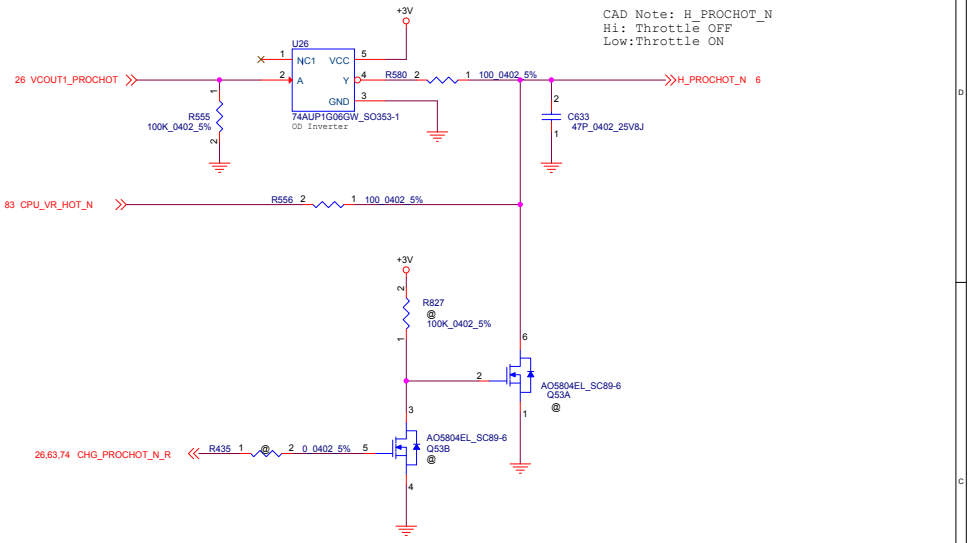
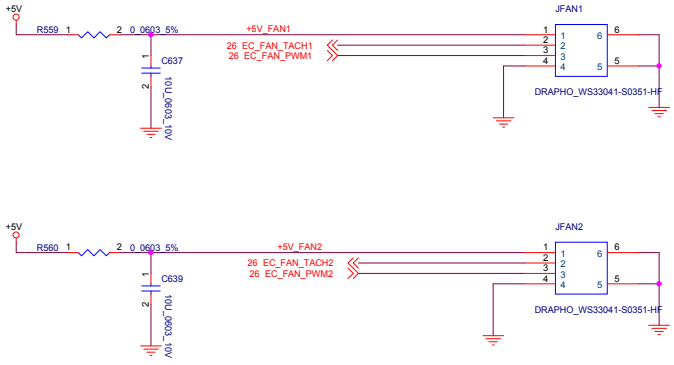
Theamal Sensor



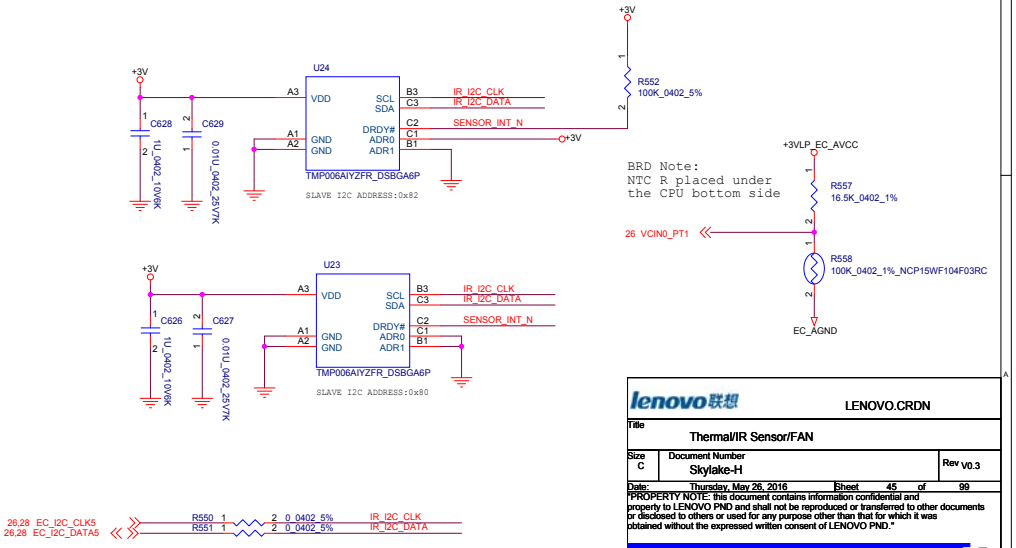
PROCHOT_N Logic



FAN CONN.



IR Sensor



lenovo联想 LENOVO.CRDN

Title: Thermal/IR Sensor/FAN

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C	Skylake-H	V0.3

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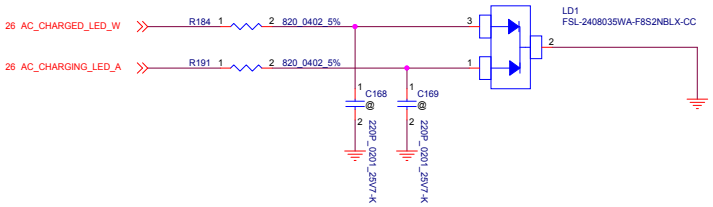
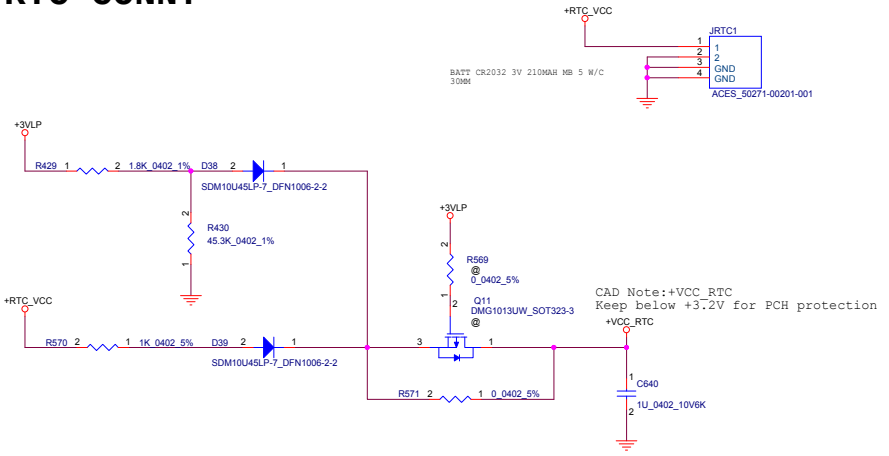
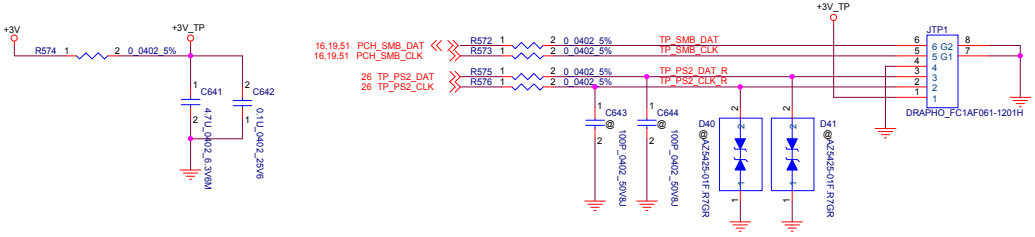
AC Charge LED



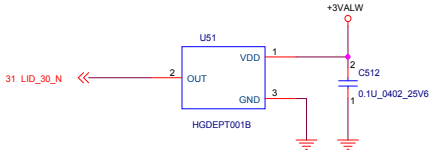
RTC CONN.



Touch Pad



LID



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Title: TP/FPR/RTC/LED CONN

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C	Skylake-H	V0.3

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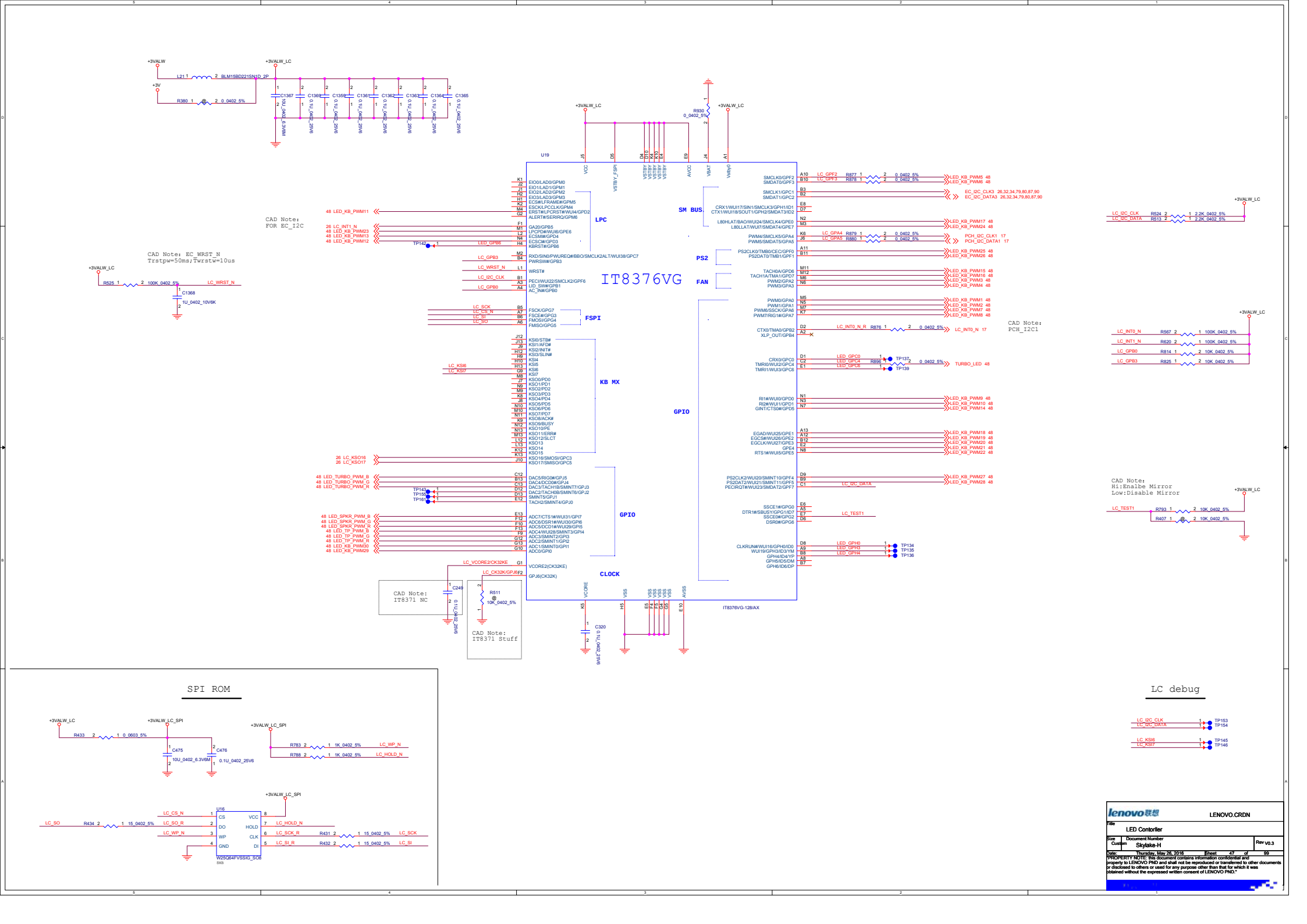
IT8376VG
U19
IT8376VG-128/AX
LPC
SM BUS
PS2
FAN
FSPI
KB MX
GPIO
GPIO
CLOCK
CAD Note:
FOR EC_I2C
CAD Note: EC_WRST_N
Trstpw=50ms;Twrstw=10us
CAD Note:
IT8371 NC
CAD Note:
IT8371 Stuff
CAD Note:
PCH_I2C1
CAD Note:
Hi:Enalbe Mirror
Low:Disable Mirror
SPI ROM
LC debug
W25Q64FVSSIG_SO8
LENOVO.CRDN
LED Contorller
Skylake-H
Thursday, May 26, 2016
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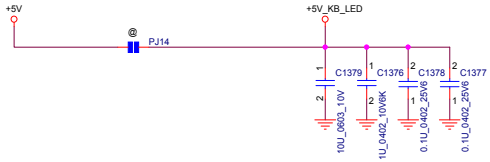
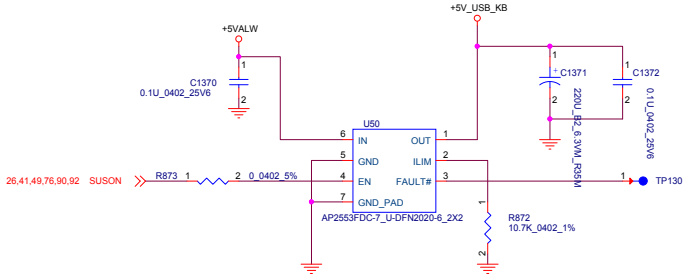
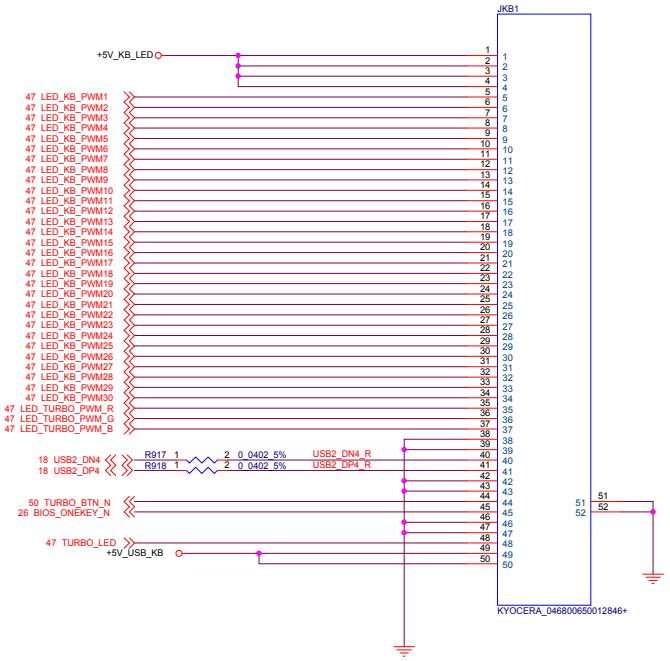
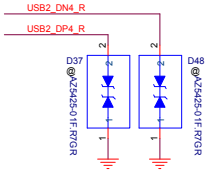


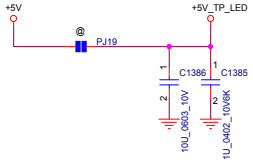


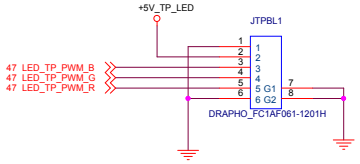
KB CONN.



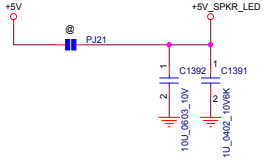


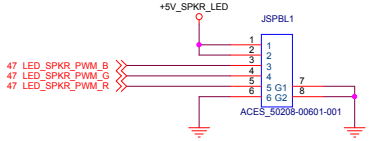
TP LED CONN.





SPKR LED CONN.





lenovo联想 LENOVO.CRDN

Title: KB/BACKLIGHT LED

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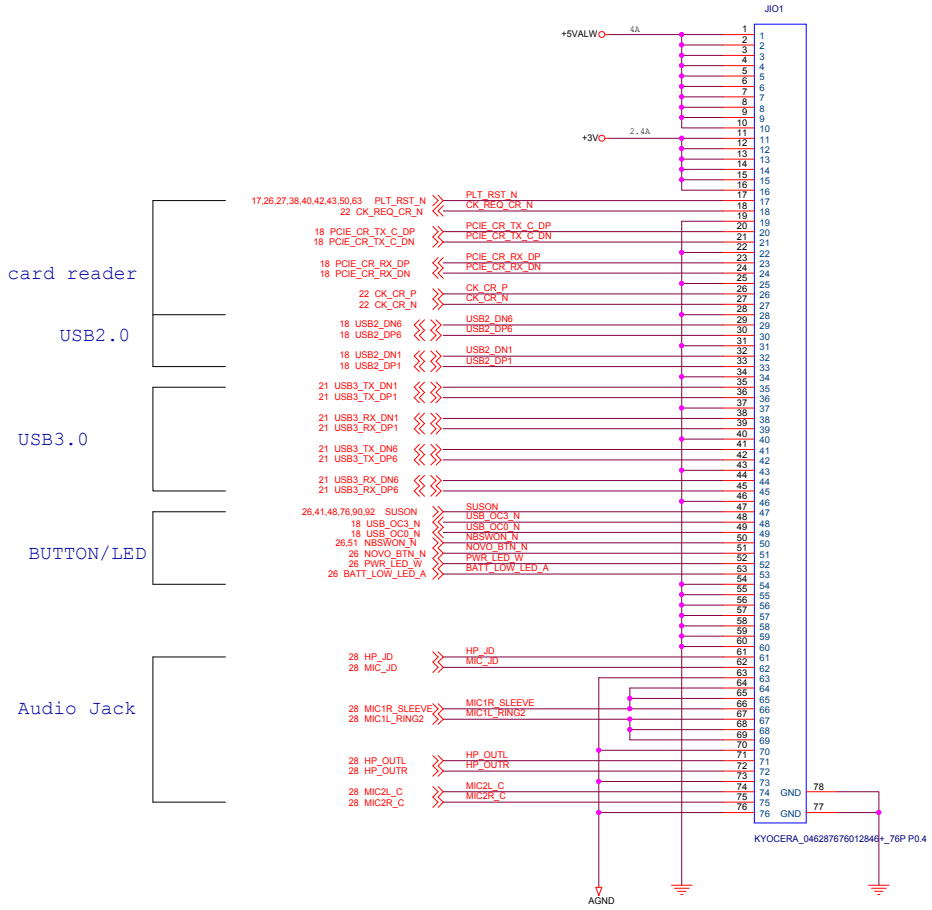

lenovo联想	LENOVO.CRDN	
Title	IO BTB Conn	
Size C	Document Number Skylake-H	Rev V0.3
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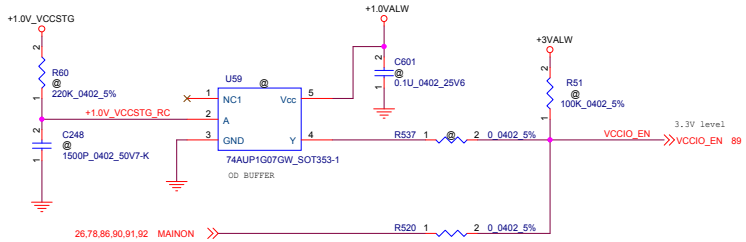
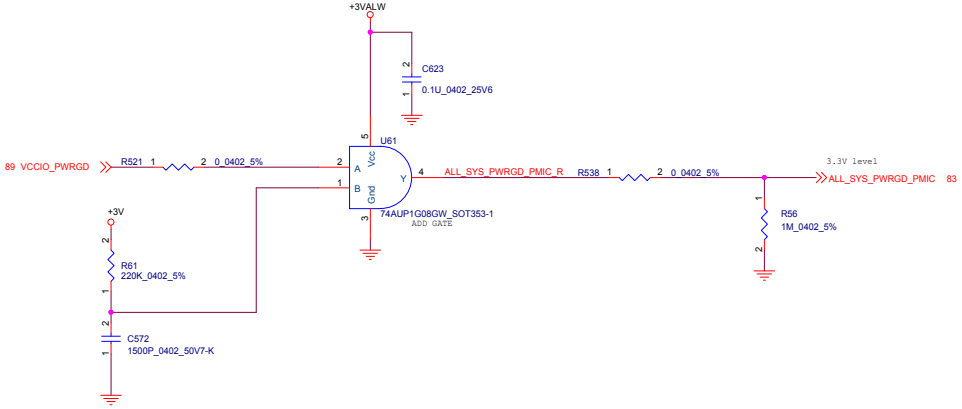
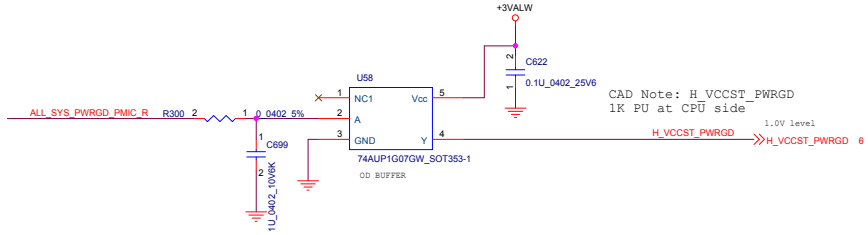
VCCIO_EN



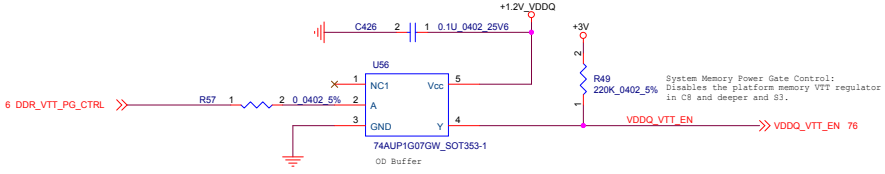
ALL_SYS_PWRGD_PMIC



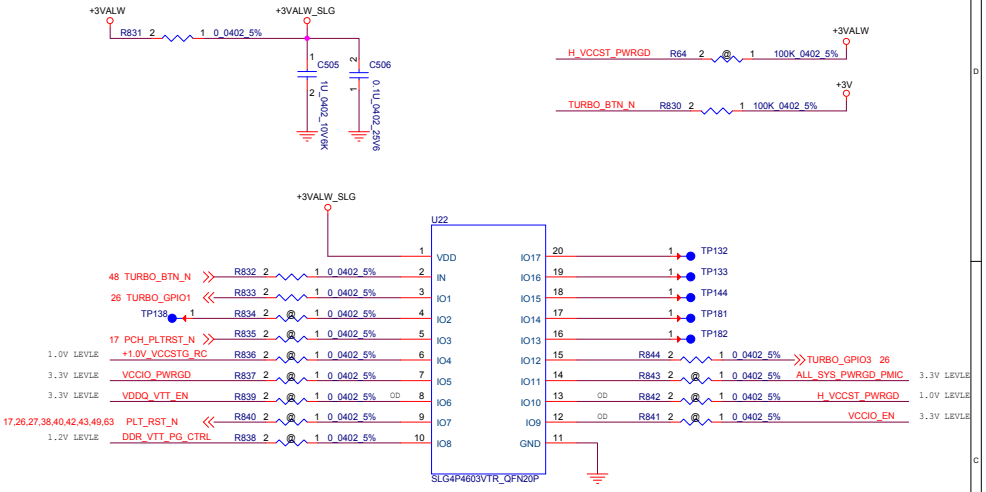
H_VCCST_PWRGD



VDDQ_VTT_EN



SLG4P4603VTR



lenovo联想	LENOVO.CRDN	
Title	PWRGD CONTROL	
Size C	Document Number Skylake-H	Rev V0.3
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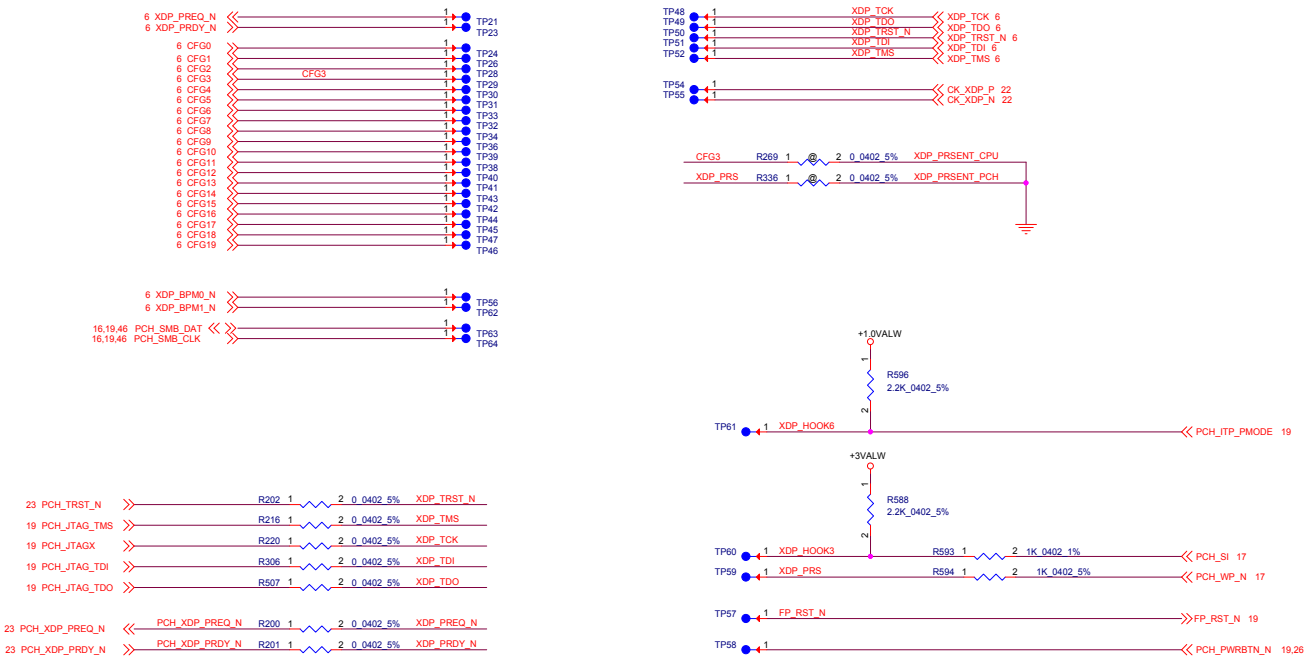
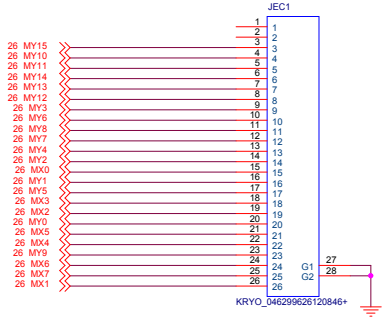
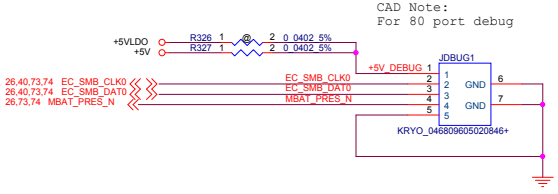
XDP CONN.



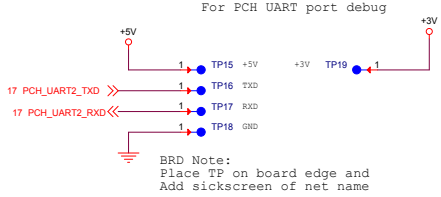
EC Debug CONN.



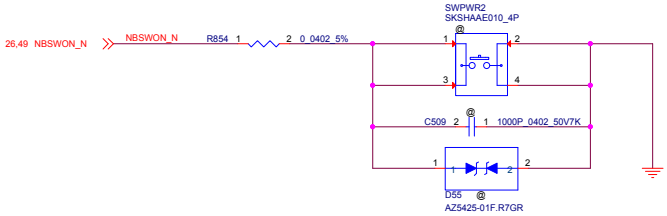
80 Port Debug CONN.



PCH UART Debug CONN.



MB PWRBTN



lenovo联想	LENOVO.CRDN	
Title	XDP/DEBUG	
Size C	Document Number Skylake-H	Rev V0.3
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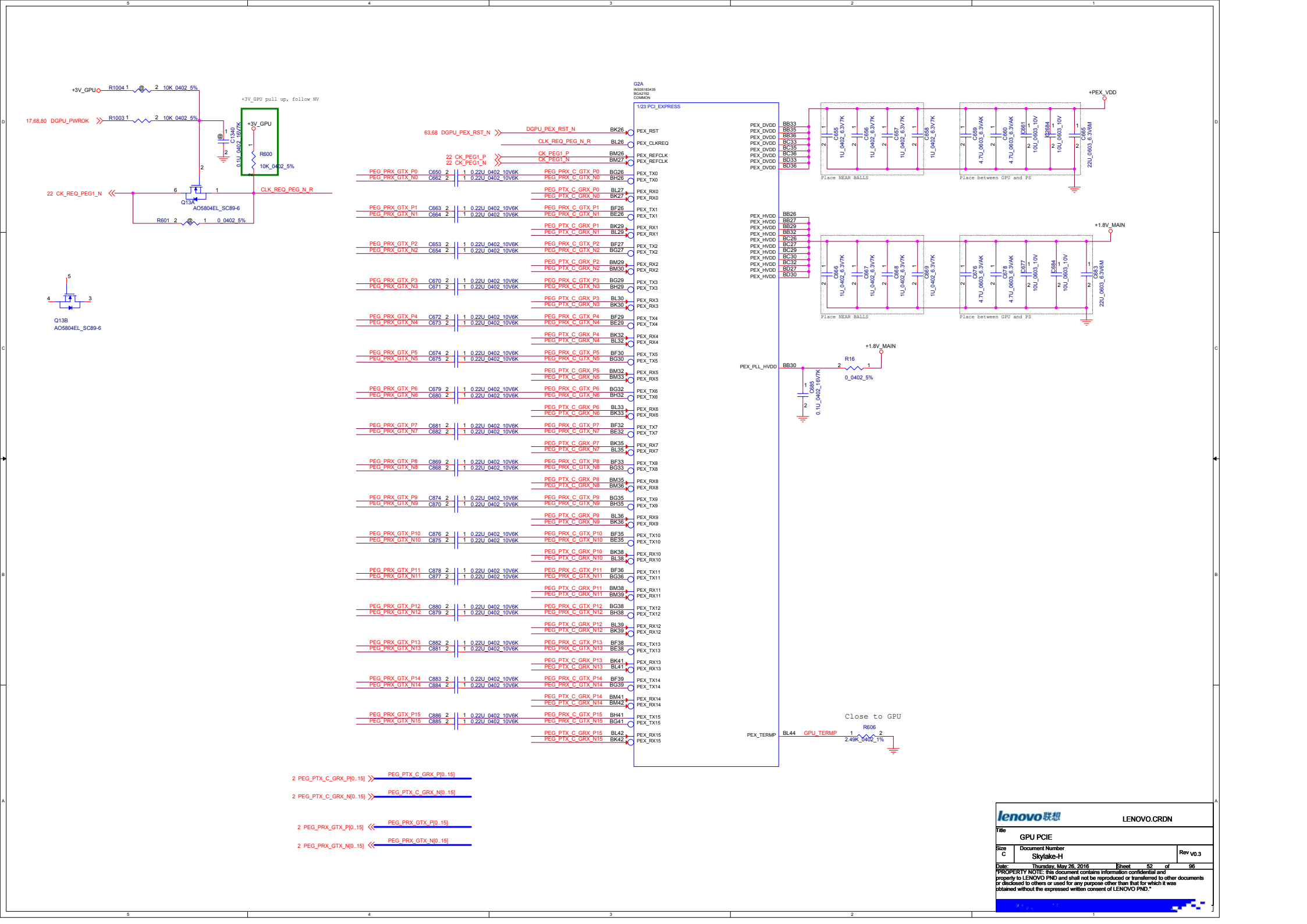
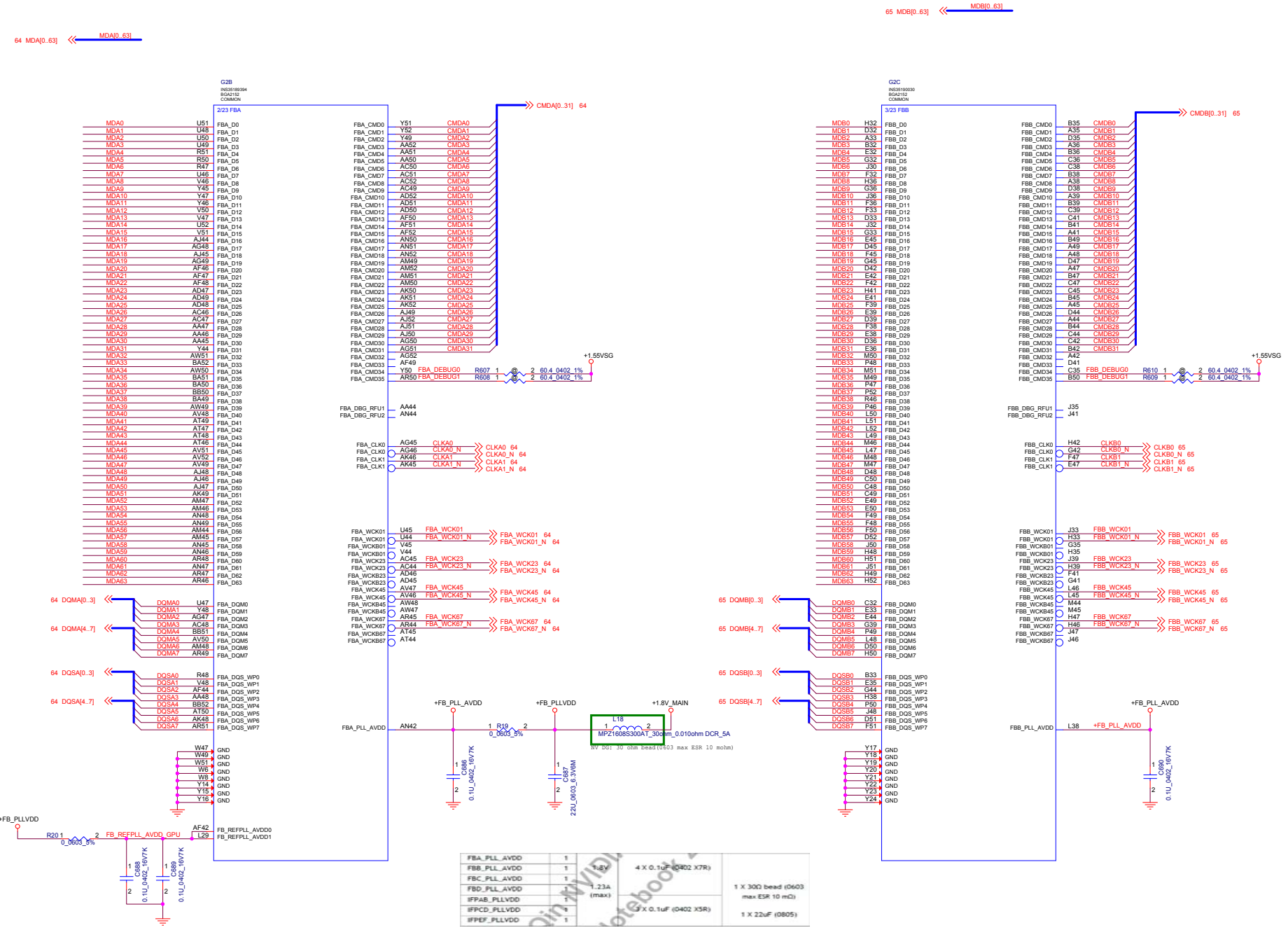
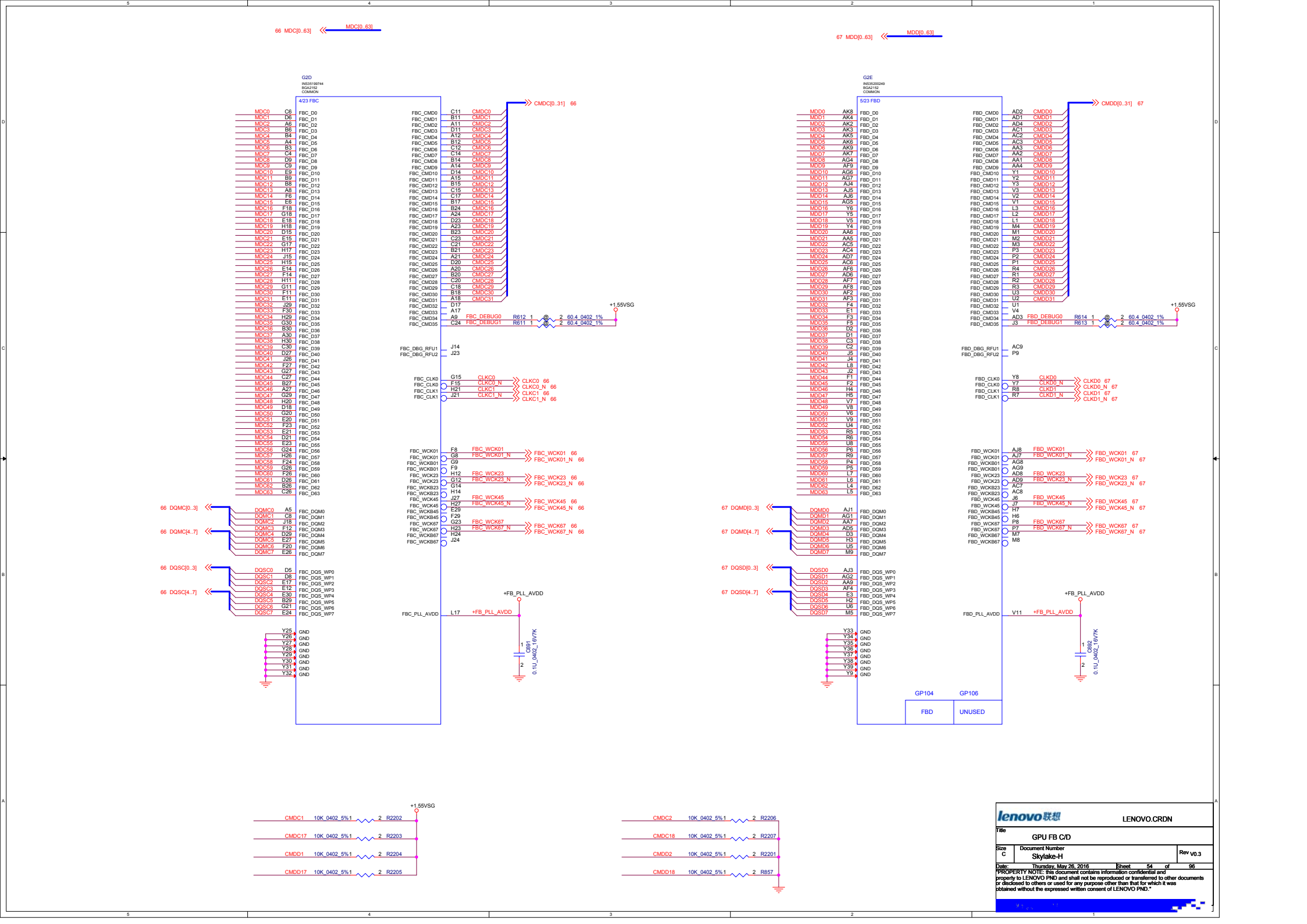


lenovo联想	LENOVO.CRDN	
Title	GPU PCIE	
Size C	Document Number Skylake-H	Rev V0.3
Date: Thursday, May 26, 2016	Sheet 52 of 96	



lenovo联想	LENOVO.CRDN	
Title	GPU FB A/B	
Size C	Document Number Skylake-H	Rev V0.3
Date: Thursday, May 26, 2016	Sheet 53 of 96	



lenovo联想	LENOVO.CRDN
Title	GPU FB C/D
Size C	Document Number Skylake-H
Rev	V0.3
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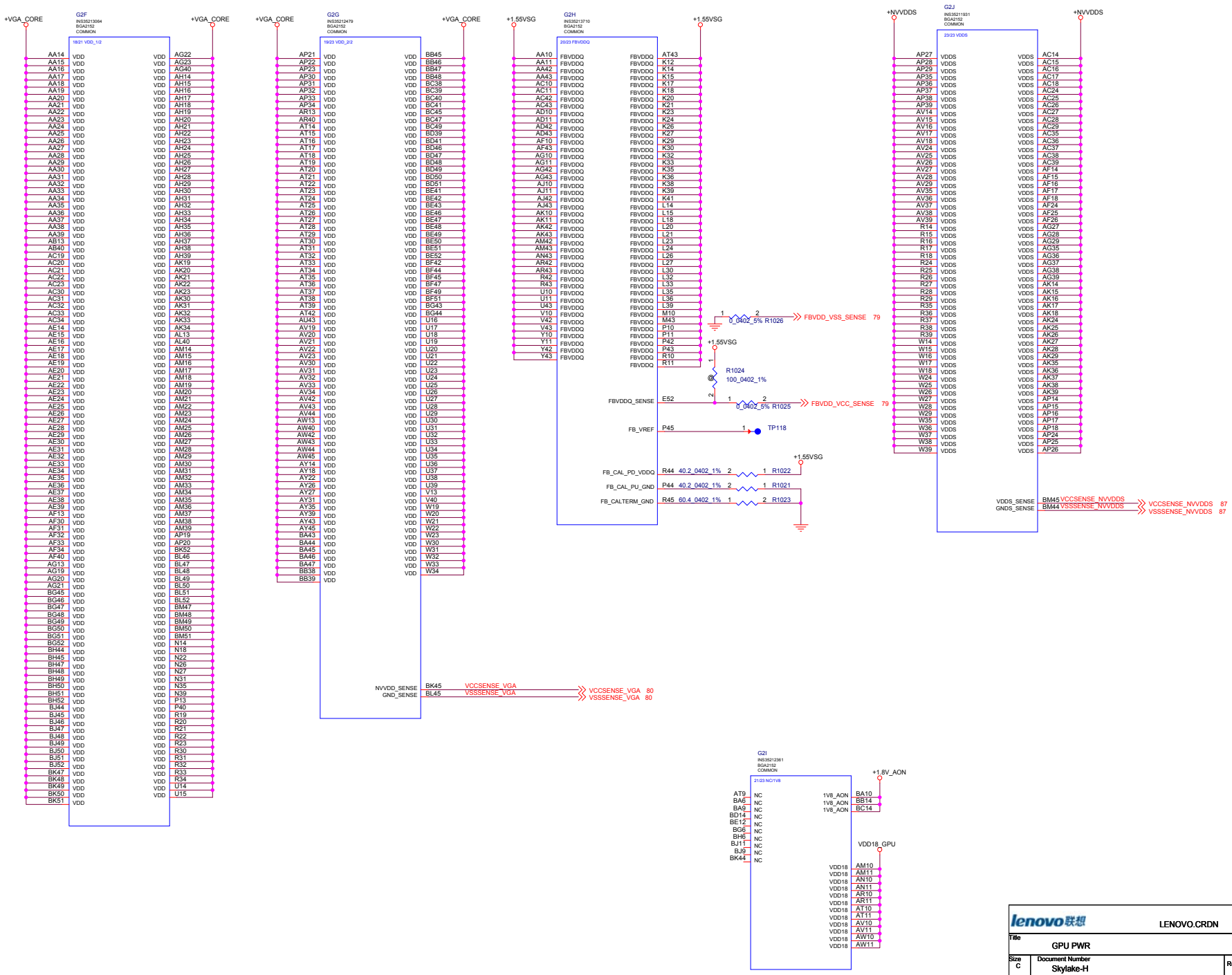
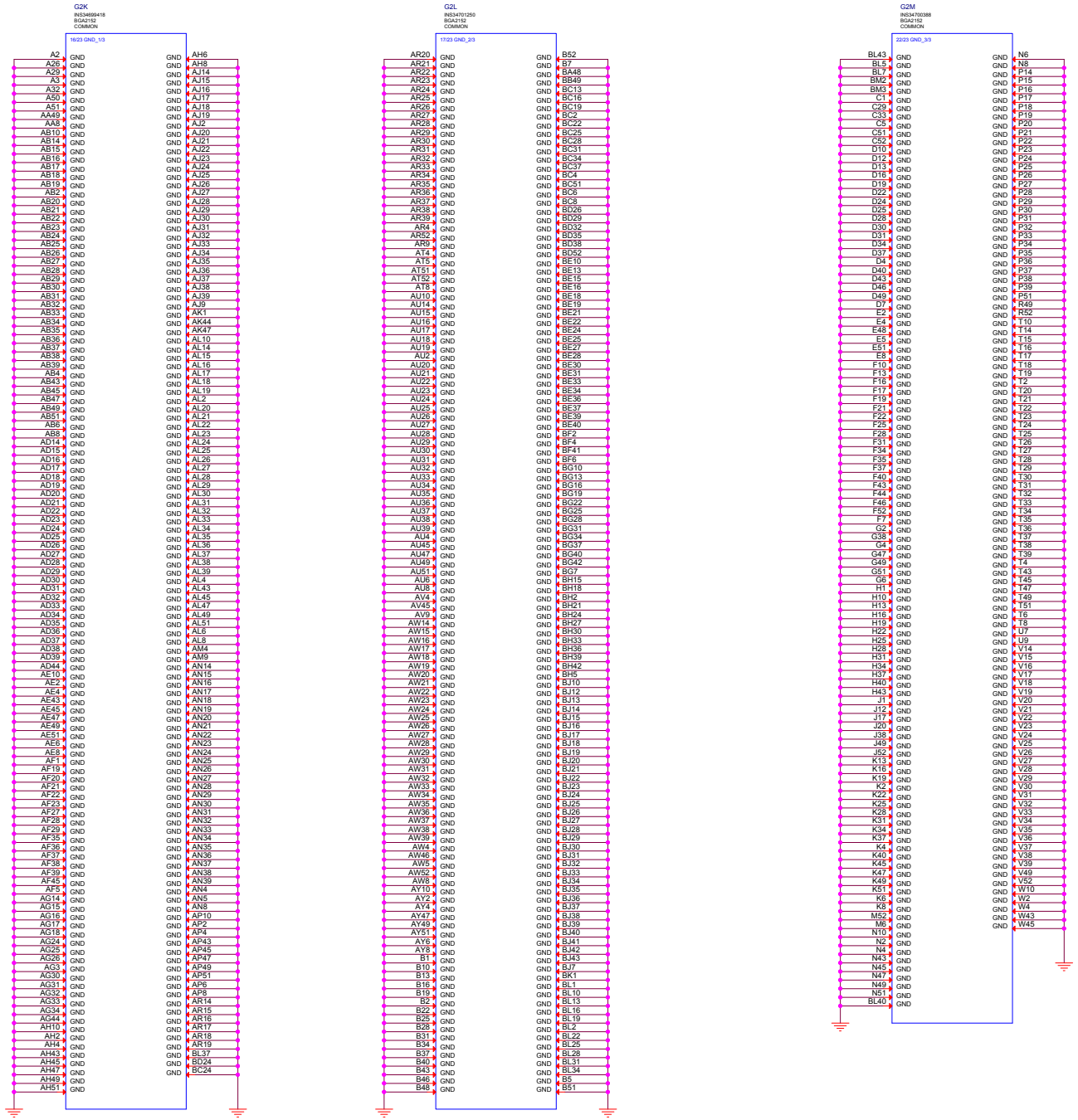


lenovo联想	LENOVO.CRDN
Title	GPU PWR
Size C	Document Number Skylake-H
	Rev V0.3
Date: Thursday, May 26, 2016	Sheet 55 of 96



Title	GPU GND		
Size C	Document Number Skylake-H		Rev V0.3
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LENOVO.CRDN

Follow NV ref-design

+VGA_CORE

+1.55VSG

Partition A 2 X 10UF, 6 X 1UF

Partition B 2 X 10UF, 6 X 1UF

Partition C 2 X 10UF, 6 X 1UF

Partition D 2 X 10UF, 6 X 1UF

2 x 330uF
2 x 47uF
4 x 22uF
11 x 10uF
49 X 1uF
2 x 330uF, Near GPU

Near GPU

Rail (GPU Ball) Name	Balls	Voltage: Current	Filtering under GPU	Filtering Near GPU
NVVDD		(+varies)	49 X 1uF (0402 X6S) 11 X 10uF (0603 X6S) 4 X 22uF (0805 X5R) 2 X 47uF (0805 X5R) 2 X 330uF (Poscap)	9 X 4.7uF (0603 X6S) 12 X 10uF (0603 X6S) 2 X 330uF (Poscap)
NVVDDS		(+varies)	16 X 1uF (0402 X6S) 4 X 10uF (0603 X6S)	2 X 4.7uF (0603 X6S) 2 X 47uF (0805 X5R) 1 X 330uF (Poscap)
FBVDDQ (GPU side)[1]		1.35V 1.5V 1.55V	24 X 1uF (0402 X6S) 8 X 10uF (0603 X6S)	4 X 10uF (0603 X6S) 9 X 22uF (0603 X6S)

+NVVDDS

1 x 330uF
1 x 47uF
4 x 10uF
16 x 1uF

Place close to GPU 4 X 10UF

Place close to GPU 9 X 22UF

+1.8V_MAIN

VDD18_GPU

R2147 1 2 0_0603_5%

1 X 4.7UF, 1 X 1UF, 2X 0.1UF

1 X 4.7UF, 1 X 1UF, 2X 0.1UF

1 X 4.7UF, 1 X 1UF, 3 X 0.1UF

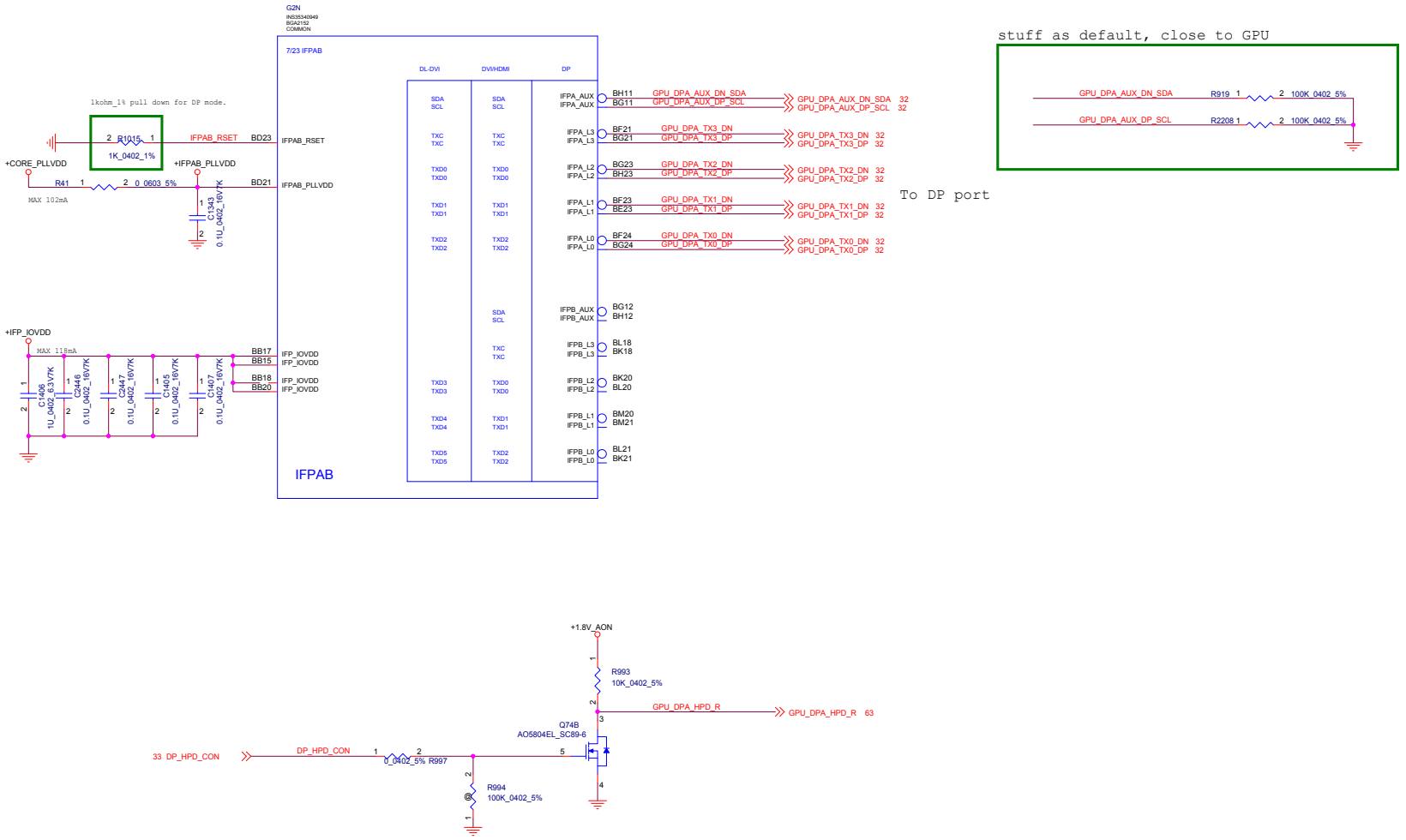
+1.8V_AON

place 1 0.1uF cap near BA10

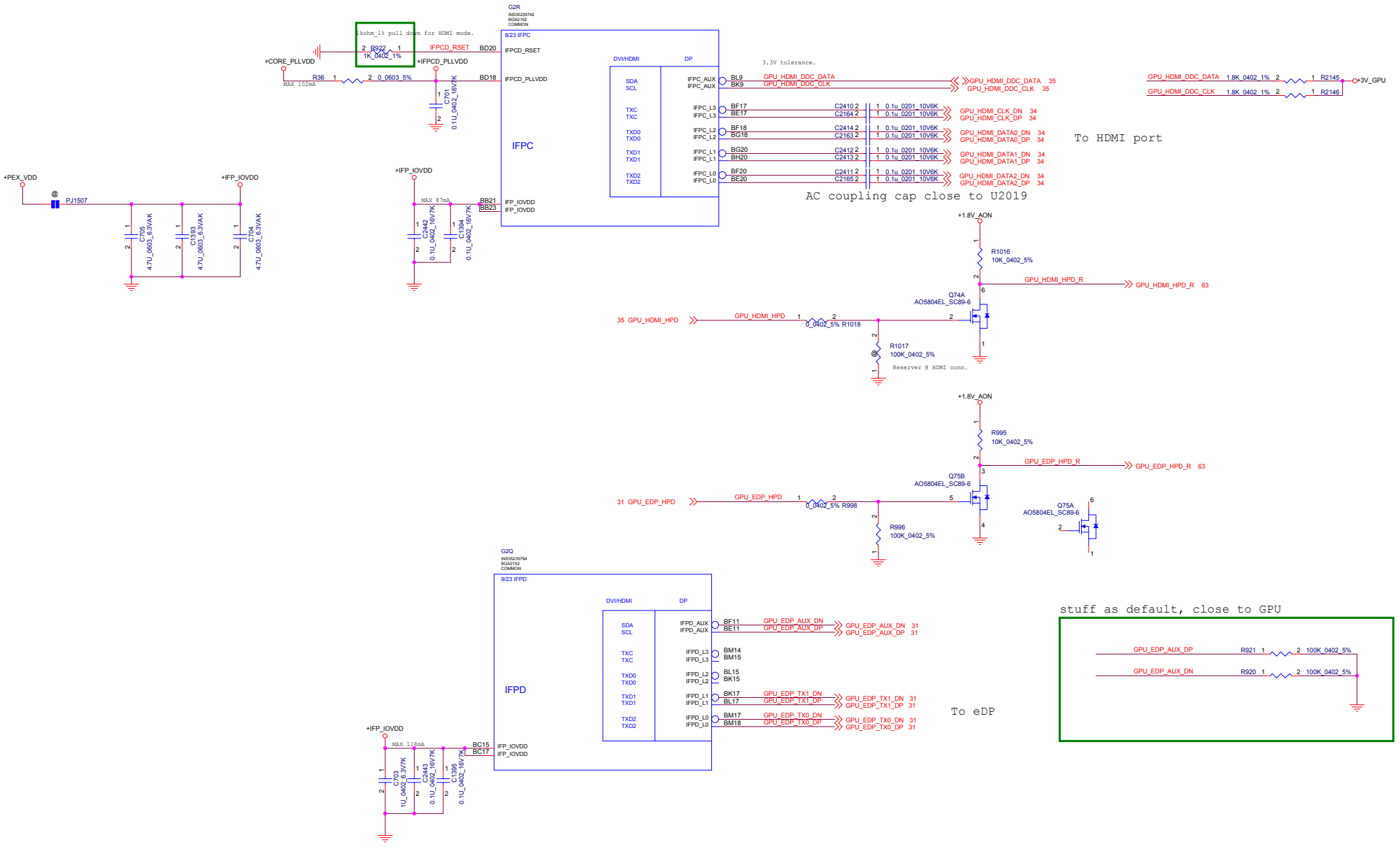
1 X 4.7UF, 1 X 1UF, 3 X 0.1UF

place 1 0.1uf cap for BB14 and BC14 to share

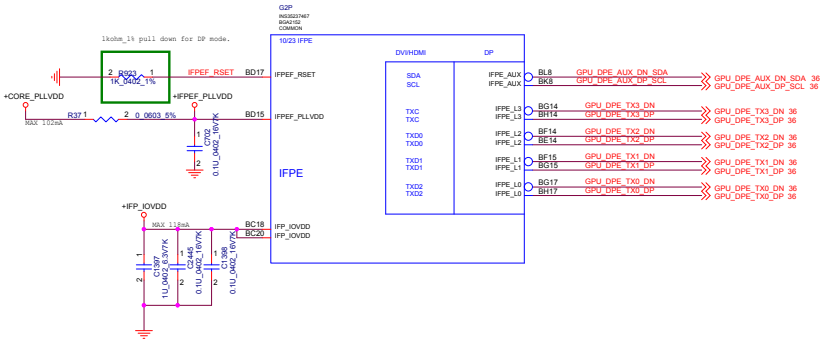
lenovo联想	LENOVO.CRDN
Title	GPU Decoupling
Size C	Document Number Skylake-H
Rev	V0.3
Date: Thursday, May 26, 2016	Sheet 57 of 96



lenovo联想	LENOVO.CRDN	
Title: GPU IFP AB		
Size: C	Document Number: Skylake-H	Rev: V0.3
Date: Thursday, May 26, 2016	Sheet 58 of 96	

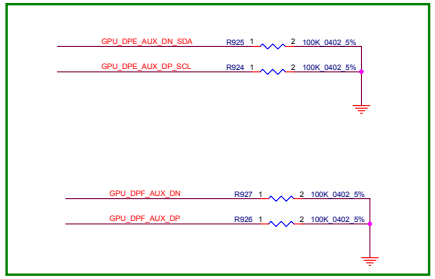


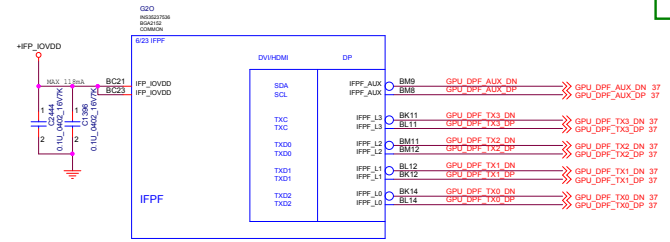
lenovo联想	LENOVO.CRDN	
Title	GPU IFP CD	
Size C	Document Number Skylake-H	Rev V0.3
Date: Thursday, May 26, 2016	Sheet 59 of 96	



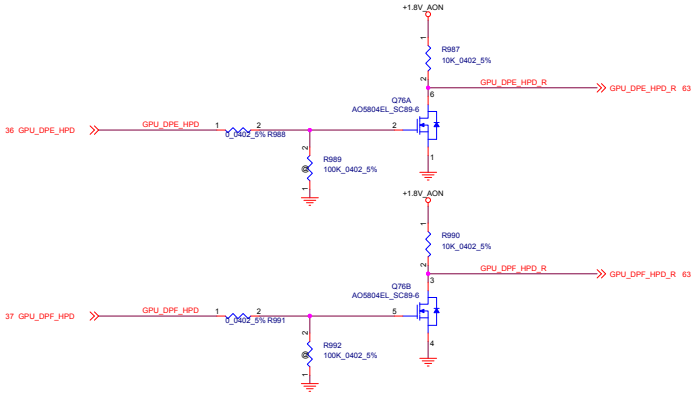
AR DP1

stuff as default, close to GPU

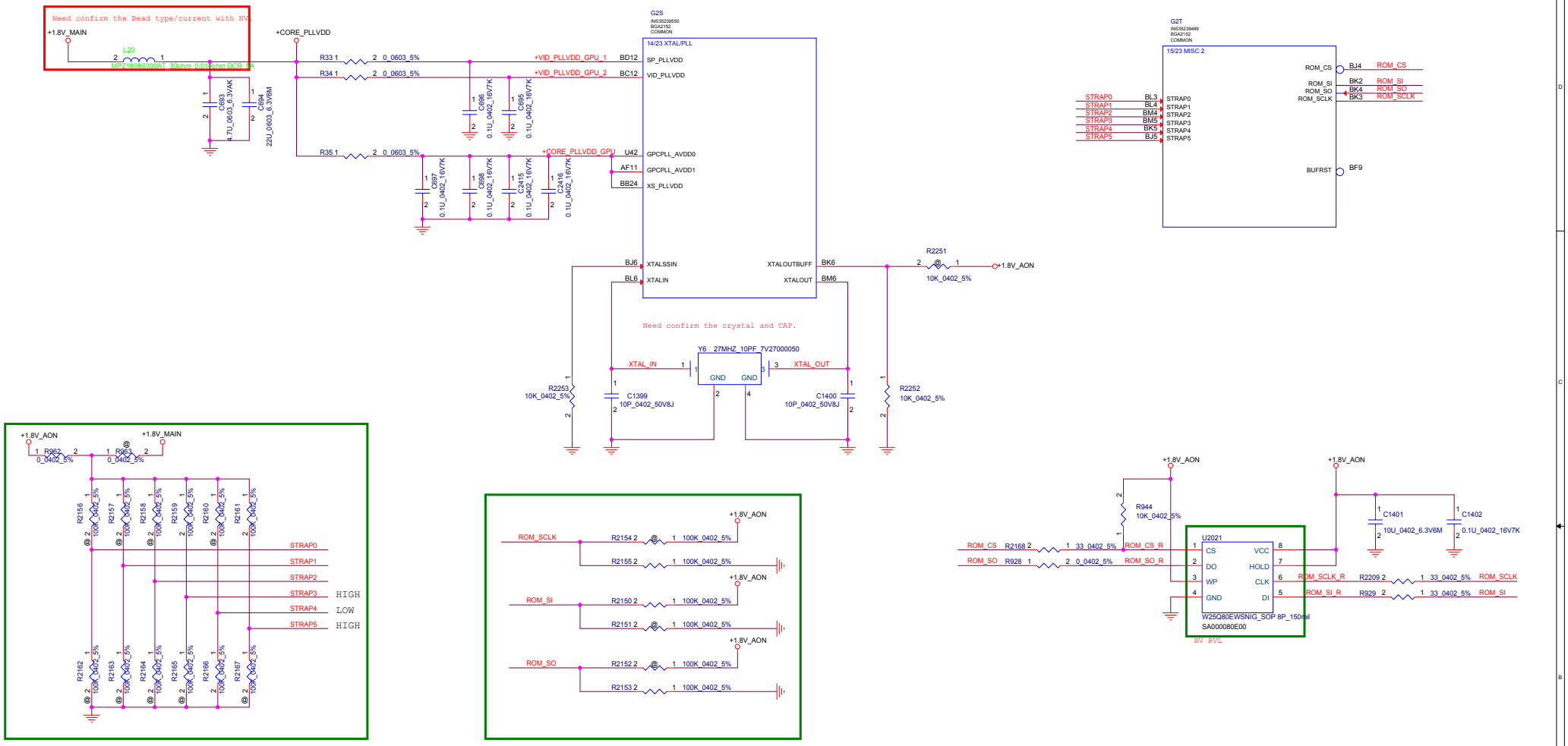




AR DP2



lenovo联想	LENOVO.CRDN	
Title: GPU IFP EF		
Size: Custom	Document Number: Skylake-H	Rev: V0.3
Date: Thursday, May 26, 2016	Sheet 60 of 96	



STRAP0~2 , Please ref RVL for BOM stuffing

GDDR5 RAM_CFG

GPU SKU	GPU	Type	FBVDD/Q	Memory Density	Allowed memory config	VRAM Vendor	VRAM P/N	Die-Revision	Memory Speed Grade	D/C Mini	RAM_CFG	STRAP2	STRAP1	STRAP0	Status
GP104	N17E-G1/G2	GDDR5	1.35V and 1.55V	8Gb	256Mx32	Samsung	K4G80325FB-HC25	B-Die	8Gbps	NA	0x0	L	L	L	Production candidate
		GDDR5	1.35V and 1.50V			Micron	MT51J256M32HF-80:A	A-Die		NA	0x1	L	L	H	Production candidate
		GDDR5	1.35V and 1.55V			Hynix	H5GQ8H24MJR-R4C	M-Die		NA	0x2	L	H	L	Post Production candidate

Note:
1. For N17E-Gx, the maximum allowable memory case temperature is 95 °C, as these are our highest end flagship GPUs.
2. N17E-Gx runs WCLK up to 3000 MHz with FBVDD=1.35V. DVS is required to run WCLK > 3000 MHz.

ROM_SCLK(LSB)/ROM_SI/ROM_SO(MSB) :

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED

lenovo联想 LENOVO.CRDN

Title: GPU PLL/XTAL

Size: C | Document Number: Skylake-H | Rev V0.3

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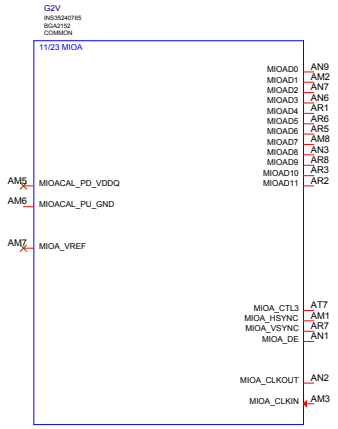

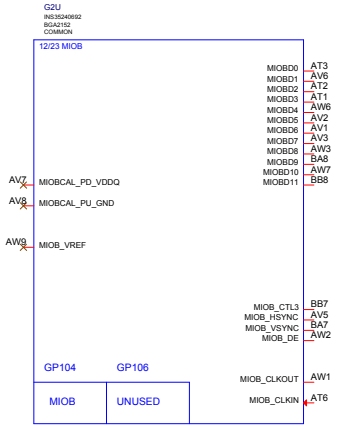

lenovo联想 LENOVO.CRDN

Title: GPU MIO

Size	Document Number	Rev
C	Skylake-H	V0.3

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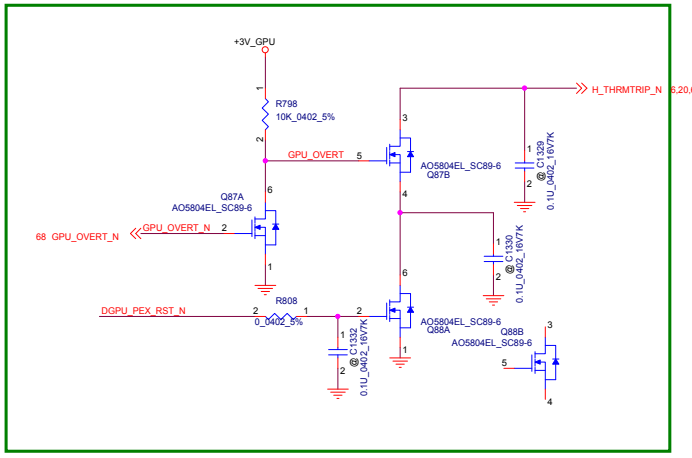
OVER Heat Protect



To PCH

G2W
INS35243086
BGA2152
COMMON

13/23 MISC 1

GPU_OVERT_N — BG5 OVERT
BF12 TS_VREF
BJ1 THERMDN
BJ2 THERMDP

+1.8V_AON
R1259 10K_0402_1%
R1260 270_0402_1%
R1261 10K_0402_5%
R1262 10K_0402_5%
R1263 10K_0402_5%

TP114 TP117 TP116 TP115
BK24 JTAG_TCK
BL23 JTAG_TMS
BM23 JTAG_TDI
BM24 JTAG_TDO
BL24 JTAG_TRST
BK23 NVJTAG_SEL

R1019 10K_0402_5%
R1265 270_0402_1%
R1020 10K_0402_5%

SMBUS Address= 0x9E

I2CS_SCL	BJ8	SMB_CLK_GPU	
I2CS_SDA	BH8	SMB_DATA_GPU	
I2CC_SCL	BG9	I2CC_SCL_R R2169 1	2 0_0402_5% I2CC_SCL → I2CC_SCL 68,80
I2CC_SDA	BH9	I2CC_SDA_R R2170 1	2 0_0402_5% I2CC_SDA → I2CC_SDA 68,80
I2CB_SCL	BG8	I2CB_SCL	
I2CB_SDA	BF8	I2CB_SDA	

need to confirm the resistor value
change to 0ohm from 33ohm-20160324

GPIO0	BD6	NVVDD_PWM_VID	NVVDD_PWM_VID 80
GPIO1	BB5	GC6_FB_EN	GC6_FB_EN 68
GPIO2	BD1	GPU_EVENT_N_R	
GPIO3	BE4	NVVDDS_PWM_VID	NVVDDS_PWM_VID 87
GPIO4	BE1	1.8V_MAIN_EN_R	
GPIO5	BG2	FRAME_LOCK_N	
GPIO6	BD2	NVVDD_PSI	NVVDD_PSI 80,87
GPIO7	BD7	GPU_EDP_BL_PWM_LS	
GPIO8	BH4	VRAM_VDDQ_ADJ_R	
GPIO9	BJ3	THERM_ALERT_N	
GPIO10	BD3	VRAM_VREF_CTL	VRAM_VREF_CTL 64,65,66,67
GPIO11	BH3	GPU_EDP_VDD_EN_LS	
GPIO12	BE6	PWR_LEVEL_R	
GPIO13	BB1	GPU_EDP_BL_EN_LS	
GPIO14	BG4	GPU_DPA_HPD_R	GPU_DPA_HPD_R 58
GPIO15	BG1		
GPIO16	BE2	SYS_PEX_RST_MON_N	
GPIO17	BH1	GPU_EDP_HPD_R	GPU_EDP_HPD_R 59
GPIO18	BE3	GPU_DPE_HPD_R	GPU_DPE_HPD_R 60
GPIO19	BD4		
GPIO20	BE5	NVVDDS_PSI	NVVDDS_PSI 87
GPIO21	BA5		
GPIO22	BB6		
GPIO23	BG3	GPU_PEX_RST_HOLD_N	
GPIO24	BD5	GPU_DPF_HPD_R	GPU_DPF_HPD_R 60
GPIO25	BB2		
GPIO26	BE7		
GPIO27	BA4	GPU_HDMI_HPD_R	
GPIO28	BB4	OC_WARN	OC_WARN 68
GPIO29	BA3	GPU_EDPc_OUTPUT_CAP	GPU_EDPc_OUTPUT_CAP 81
GPIO30	BB3		
GPIO31_RFU	BA2		
GPIO32_RFU	BA1		

To PWR VGA CORE

To PWR VGA CORE
Output,Open Drain,10 K? pull-up to 1V8_AON
NVSR pannel not used.

THERM_ALERT_N:
Output,Open Drain,10 K? pull-up to 1V8_AON
Active Low Thermal Alert
N17E GPU uses GPIO9 as a dedicated output, not supported as an input.

Output,Open Drain,10 K? pull-up to 1V8_AON

+1.8V_AON +3V_GPU

R796 2 — 1 10K_0402_5%
GPU_OVERT_N
R797 2 — @ 1 10K_0402_5%

+3V_GPU

SMB_CLK_GPU R2294 1 — 2 2.2K_0402_5%
SMB_DATA_GPU R2295 1 — 2 2.2K_0402_5%

I2CC_SCL R2296 1 — 2 2.2K_0402_5%
I2CC_SDA R2297 1 — 2 2.2K_0402_5%

I2CB_SCL R2298 1 — 2 2.2K_0402_5%
I2CB_SDA R2299 1 — 2 2.2K_0402_5%

+3V_GPU

C2694 1 — 2 0.1U_0402_16V7K
U2027 M74VHC1GT08DFT2G_SC-70-5P
VCC=3.3V, VIH>=1.4V
GPU_EDP_BL_PWM_LS
GPU_EDP_BL_PWM_R
SA000080W00 AND Gate
R2305 10K_0402_5%
R2300 100K_0402_5%

+3V_GPU

C2695 1 — 2 0.1U_0402_16V7K
U2028 M74VHC1GT08DFT2G_SC-70-5P
VCC=3.3V, VIH>=1.4V
GPU_EDP_VDD_EN_LS
GPU_EDP_VDD_EN_R
SA000080W00 AND Gate
R2306 10K_0402_5%
R2302 100K_0402_5%

+3V_GPU

C2696 1 — 2 0.1U_0402_16V7K
U2029 M74VHC1GT08DFT2G_SC-70-5P
VCC=3.3V, VIH>=1.4V
GPU_EDP_BL_EN_LS
GPU_EDP_BL_EN_R
SA000080W00 AND Gate
R2307 10K_0402_5%
R2304 100K_0402_5%

1.8V_MAIN_EN_R	R976	0_0402_5%	1.8V_MAIN_EN → 1.8V_MAIN_EN 68,69
GPU_EDP_BL_PWM_R	R979	0_0402_5%	EDP_BL_PWM → EDP_BL_PWM 31
VRAM_VDDQ_ADJ_R	R981	0_0402_5%	VRAM_VDDQ_ADJ → VRAM_VDDQ_ADJ 79
GPU_EDP_VDD_EN_R	R905	0_0402_5%	EDP_VDD_EN → EDP_VDD_EN 90,92
GPU_EDP_BL_EN_R	R985	0_0402_5%	EDP_BL_EN → EDP_BL_EN 31

to open 1.8V_main and NVVDD

Need confirm.

+1.8V_AON

GPU_EVENT_N_R	R974	10K_0402_5%	
1.8V_MAIN_EN_R	R975	10K_0402_5%	
NVVDD_PSI	R977	10K_0402_5%	
VRAM_VDDQ_ADJ	R980	@ 10K_0402_5%	
THERM_ALERT_N	R982	10K_0402_5%	
PWR_LEVEL_R	R983	100K_0402_5%	
OC_WARN	R986	10K_0402_5%	
SYS_PEX_RST_MON_N	R999	@ 10K_0402_5%	
GPU_PEX_RST_HOLD_N	R1000	10K_0402_5%	
NVVDDS_PSI	R1002	@ 10K_0402_5%	
FRAME_LOCK_N	R2271	10K_0402_5%	
GC6_FB_EN	R660	10K_0402_5%	

+3V_GPU

SMB_CLK_GPU — Q80A — EC_SMB_CLK1 19,26,45
SMB_DATA_GPU — Q80B — EC_SMB_DAT1 19,26,45
AO5804EL_SC89-6

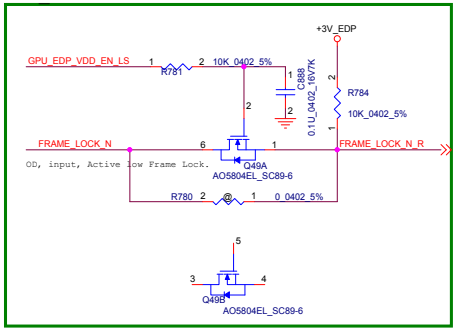
+1.8V_AON

THERM_ALERT_N — Q93A AO5804EL_SC89-6 — EC_THERM_ALERT_N 26
GPU Thermal Alert, OD, output
Q93B AO5804EL_SC89-6
To EC

GPU_EVENT_N_R — D52 SDM10U45LP-7_DFN1006-2-2 — GPU_EVENT_N 17
R973 1 — @ 2 0_0402_5%
From PCH

PWR_LEVEL_R
D2011 SDM10U45LP-7_DFN1006-2-2 — PWR_LEVEL 26 From EC
D2016 SDM10U45LP-7_DFN1006-2-2 @ — CHG_PROCHOT_N_R 26,45,74 From Charger

FRM LOCK Reserved



FRAME_LOCK_N_R 31

From PCH, 3.3V level

23 DGPU_HOLD_RST_N
17,26,27,38,40,42,43,49,50 PLT_RST_N

+1.8V_AON
C1333 0.1U_0402_16V7K
U63 74AUP1G08GW_SOT353-1 AND Gate

R2172 1 — 2 0_0402_5%

+1.8V_AON
C1339 0.1U_0402_16V7K
U62 74AUP1G08GW_SOT353-1 AND Gate

R2171 2 — @ 1 0_0402_5%
SYS_PEX_RST_MON_N
GPU_PEX_RST_HOLD_N

DGPU_PEX_RST_N → DGPU_PEX_RST_N 52,68
To GPU, 1.8V level

R1001 100K_0402_5%

lenovo联想	LENOVO.CRDN
Title	GPU GPIO
Size C	Document Number Skylake-H
Rev	V0.3
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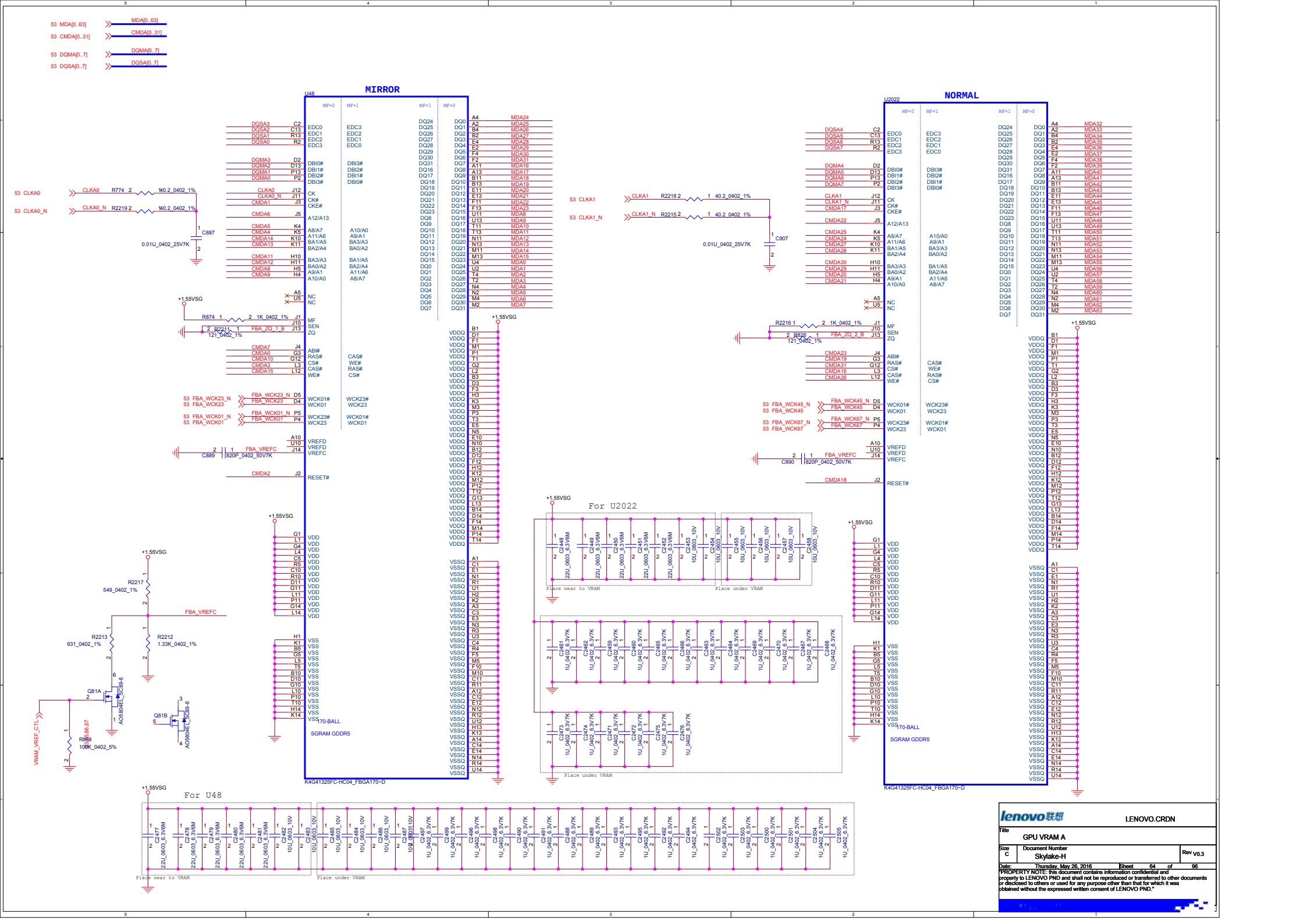
MIRROR
NORMAL
U48
U2022
MDA[0..63]
CMDA[0..31]
DQMA[0..7]
DQSA[0..7]
K4G41325FC-HC04_FBGA170~D
170-BALL
SGRAM GDDR5
+1.55VSG
For U2022
For U48
Place near to VRAM
Place under VRAM
VRAM_VREF_CTL
FBA_VREFC
LENOVO.CRDN
GPU VRAM A
Skylake-H
Rev V0.3
Thursday, May 26, 2016
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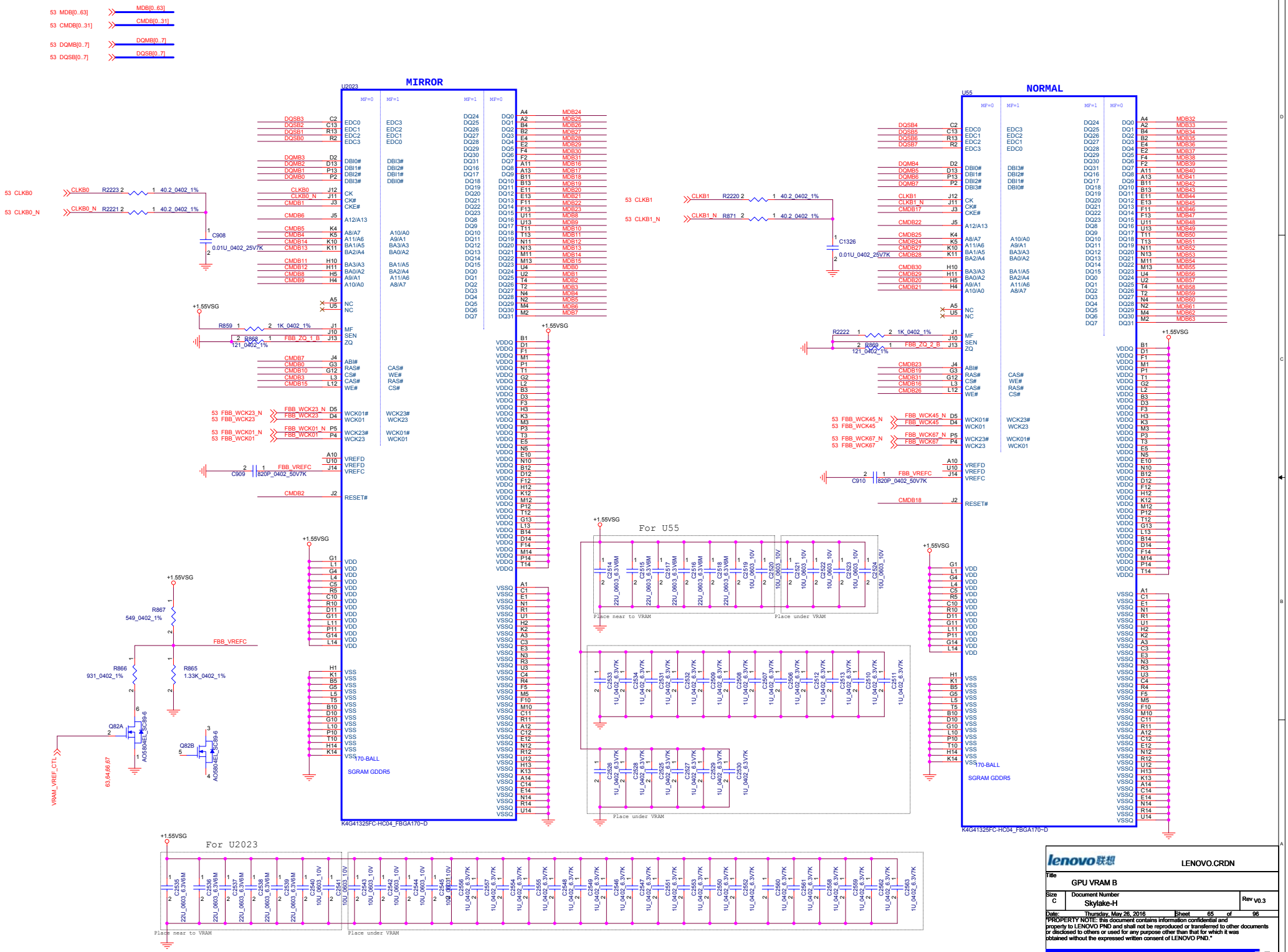

lenovo联想 LENOVO.CRDN

Title: GPU VRAM B

Size: C | Document Number: Skylake-H | Rev V0.3

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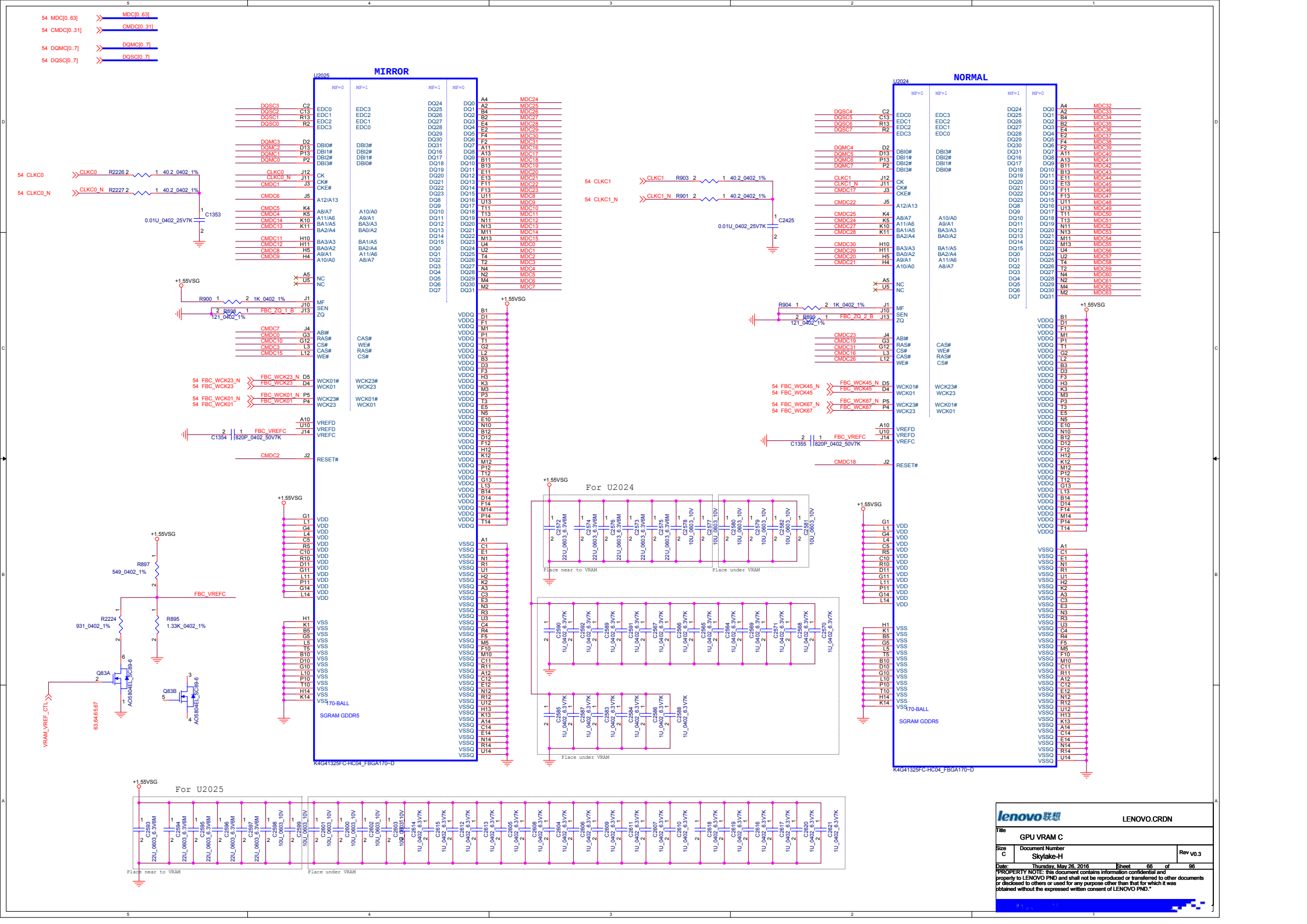

54 MDD[0..63] MDD[0..63]
54 CMDD[0..31] CMDD[0..31]
54 DQMD[0..7] DQMD[0..7]
54 DQSD[0..7] DQSD[0..7]

MIRROR

U2026

MF=0 MF=1 MF=1 MF=0

DQSD3 C2 EDC0 EDC3 DQ24 DQ0 A4 MDD24
DQSD2 C13 EDC1 EDC2 DQ25 DQ1 A2 MDD25
DQSD1 R13 EDC2 EDC1 DQ26 DQ2 B4 MDD26
DQSD0 R2 EDC3 EDC0 DQ27 DQ3 B2 MDD27
DQ28 DQ4 E4 MDD28
DQ29 DQ5 E2 MDD29
DQMD3 D2 DBI0# DBI3# DQ30 DQ6 F4 MDD30
DQMD2 D13 DBI1# DBI2# DQ31 DQ7 F2 MDD31
DQMD1 P13 DBI2# DBI1# DQ16 DQ8 A11 MDD16
DQMD0 P2 DBI3# DBI0# DQ17 DQ9 A13 MDD17
DQ18 DQ10 B11 MDD18
DQ19 DQ11 B13 MDD19
CLKD0 J12 DQ20 DQ12 E11 MDD20
CLKD0_N J11 CK DQ21 DQ13 E13 MDD21
CMDD1 J3 CKE# DQ22 DQ14 F11 MDD22
DQ23 DQ15 F13 MDD23
CMDD6 J5 A12/A13 DQ8 DQ16 U11 MDD8
DQ9 DQ17 U13 MDD9
CMDD5 K4 A8/A7 A10/A0 DQ10 DQ18 T11 MDD10
CMDD4 K5 A11/A6 A9/A1 DQ11 DQ19 T13 MDD11
CMDD14 K10 BA1/A5 BA3/A3 DQ12 DQ20 N13 MDD12
CMDD13 K11 BA2/A4 BA0/A2 DQ13 DQ21 M11 MDD13
DQ14 DQ22 M13 MDD14
CMDD11 H10 BA3/A3 BA1/A5 DQ15 DQ23 U4 MDD15
CMDD12 H11 BA0/A2 BA2/A4 DQ0 DQ24 U2 MDD0
CMDD8 H5 A9/A1 A11/A6 DQ1 DQ25 T4 MDD1
CMDD9 H4 A10/A0 A8/A7 DQ2 DQ26 T2 MDD2
DQ3 DQ27 N4 MDD3
A5 NC DQ4 DQ28 N2 MDD4
U5 NC DQ5 DQ29 M4 MDD5
DQ6 DQ30 M2 MDD6
DQ7 DQ31 MDD7

54 CLKD0 CLKD0 R785 2 1 40.2_0402_1%
54 CLKD0_N CLKD0_N R906 2 1 40.2_0402_1%
1 C1373 2 0.01U_0402_25V7K

+1.55VSG
R913 1 2 1K_0402_1%
2 R911 1 121_0402_1%
FBD_ZQ_1_B

J1 MF
J10 SEN
J13 ZQ

CMDD7 J4 ABI#
CMDD0 G3 RAS# CAS#
CMDD10 G12 CS# WE#
CMDD3 L3 CAS# RAS#
CMDD15 L12 WE# CS#

54 FBD_WCK23_N FBD_WCK23_N D5 WCK01# WCK23#
54 FBD_WCK23 FBD_WCK23 D4 WCK01 WCK23
54 FBD_WCK01_N FBD_WCK01_N P5 WCK23# WCK01#
54 FBD_WCK01 FBD_WCK01 P4 WCK23 WCK01

A10 U10 VREFD
2 1 C1374 FBD_VREFC J14 VREFC
820P_0402_50V7K

CMDD2 J2 RESET#

+1.55VSG
R910 549_0402_1%
FBD_VREFC
R909 931_0402_1%
R908 1.33K_0402_1%
Q84A AO6804E_SC89-6
Q84B AO6804E_SC89-6
VRAM_VREF_CTL
63,64,65,66

G1 VDD
L1 VDD
G4 VDD
L4 VDD
C5 VDD
R5 VDD
C10 VDD
R10 VDD
D11 VDD
G11 VDD
L11 VDD
P11 VDD
G14 VDD
L14 VDD

H1 VSS
K1 VSS
B5 VSS
G5 VSS
L5 VSS
T5 VSS
B10 VSS
D10 VSS
G10 VSS
L10 VSS
P10 VSS
T10 VSS
H14 VSS
K14 VSS

170-BALL
SGRAM GDDR5
K4G41325FC-HC04_FBGA170-D

+1.55VSG
VDDQ B1 D1 F1 M1 P1 T1 G2 L2 B3 D3 F3 H3 K3 M3 P3 T3 E5 N5 E10 N10 B12 D12 F12 H12 K12 M12 P12 T12 G13 L13 B14 D14 F14 M14 P14 T14

VSSQ A1 C1 E1 N1 R1 U1 H2 K2 A3 C3 E3 N3 R3 U3 C4 R4 F5 M5 F10 M10 C11 R11 A12 C12 E12 N12 R12 U12 H13 K13 A14 C14 E14 N14 R14 U14

For U60

C2630 C2632 C2634 C2631 C2633 C2636 C2635 C2638 C2637 C2640 C2639
22U_0603_6.3V6M 10U_0603_10V
Place near to VRAM
Place under VRAM

C2648 C2650 C2647 C2649 C2625 C2624 C2623 C2622 C2628 C2629 C2626 C2627
C2642 C2644 C2641 C2643 C2645 C2646
1U_0402_6.3V7K
Place under VRAM

For U20256

C2651 C2652 C2654 C2653 C2656 C2655 C2658
22U_0603_6.3V6M 10U_0603_10V
Place near to VRAM

C2660 C2657 C2659 C2661 C2672 C2670 C2671 C2664 C2665 C2662 C2663 C2668 C2669 C2666 C2667 C2677 C2676 C2673 C2675 C2679 C2678
10U_0603_10V 1U_0402_6.3V7K
Place under VRAM

NORMAL

U60

MF=0 MF=1 MF=1 MF=0

DQSD4 C2 EDC0 EDC3 DQ24 DQ0 A4 MDD32
DQSD5 C13 EDC1 EDC2 DQ25 DQ1 A2 MDD33
DQSD6 R13 EDC2 EDC1 DQ26 DQ2 B4 MDD34
DQSD7 R2 EDC3 EDC0 DQ27 DQ3 B2 MDD35
DQ28 DQ4 E4 MDD36
DQ29 DQ5 E2 MDD37
DQMD4 D2 DBI0# DBI3# DQ30 DQ6 F4 MDD38
DQMD5 D13 DBI1# DBI2# DQ31 DQ7 F2 MDD39
DQMD6 P13 DBI2# DBI1# DQ16 DQ8 A11 MDD40
DQMD7 P2 DBI3# DBI0# DQ17 DQ9 A13 MDD41
DQ18 DQ10 B11 MDD42
DQ19 DQ11 B13 MDD43
CLKD1 J12 DQ20 DQ12 E11 MDD44
CLKD1_N J11 CK DQ21 DQ13 E13 MDD45
CMDD17 J3 CKE# DQ22 DQ14 F11 MDD46
DQ23 DQ15 F13 MDD47
CMDD22 J5 A12/A13 DQ8 DQ16 U11 MDD48
DQ9 DQ17 U13 MDD49
CMDD25 K4 A8/A7 A10/A0 DQ10 DQ18 T11 MDD50
CMDD24 K5 A11/A6 A9/A1 DQ11 DQ19 T13 MDD51
CMDD27 K10 BA1/A5 BA3/A3 DQ12 DQ20 N13 MDD52
CMDD28 K11 BA2/A4 BA0/A2 DQ13 DQ21 M11 MDD53
DQ14 DQ22 M13 MDD54
CMDD30 H10 BA3/A3 BA1/A5 DQ15 DQ23 U4 MDD55
CMDD29 H11 BA0/A2 BA2/A4 DQ0 DQ24 U2 MDD56
CMDD20 H5 A9/A1 A11/A6 DQ1 DQ25 T4 MDD57
CMDD21 H4 A10/A0 A8/A7 DQ2 DQ26 T2 MDD58
DQ3 DQ27 N4 MDD59
A5 NC DQ4 DQ28 N2 MDD60
U5 NC DQ5 DQ29 M4 MDD61
DQ6 DQ30 M2 MDD62
DQ7 DQ31 MDD63

54 CLKD1 CLKD1 R916 2 1 40.2_0402_1%
54 CLKD1_N CLKD1_N R914 2 1 40.2_0402_1%
1 C2439 2 0.01U_0402_25V7K

+1.55VSG
R2228 1 2 1K_0402_1%
2 R912 1 121_0402_1%
FBD_ZQ_2_B

J1 MF
J10 SEN
J13 ZQ

CMDD23 J4 ABI#
CMDD19 G3 RAS# CAS#
CMDD31 G12 CS# WE#
CMDD16 L3 CAS# RAS#
CMDD26 L12 WE# CS#

54 FBD_WCK45_N FBD_WCK45_N D5 WCK01# WCK23#
54 FBD_WCK45 FBD_WCK45 D4 WCK01 WCK23
54 FBD_WCK67_N FBD_WCK67_N P5 WCK23# WCK01#
54 FBD_WCK67 FBD_WCK67 P4 WCK23 WCK01

A10 U10 VREFD
2 1 C1375 FBD_VREFC J14 VREFC
820P_0402_50V7K

CMDD18 J2 RESET#

+1.55VSG
G1 VDD
L1 VDD
G4 VDD
L4 VDD
C5 VDD
R5 VDD
C10 VDD
R10 VDD
D11 VDD
G11 VDD
L11 VDD
P11 VDD
G14 VDD
L14 VDD

H1 VSS
K1 VSS
B5 VSS
G5 VSS
L5 VSS
T5 VSS
B10 VSS
D10 VSS
G10 VSS
L10 VSS
P10 VSS
T10 VSS
H14 VSS
K14 VSS

170-BALL
SGRAM GDDR5
K4G41325FC-HC04_FBGA170-D

+1.55VSG
VDDQ B1 D1 F1 M1 P1 T1 G2 L2 B3 D3 F3 H3 K3 M3 P3 T3 E5 N5 E10 N10 B12 D12 F12 H12 K12 M12 P12 T12 G13 L13 B14 D14 F14 M14 P14 T14

VSSQ A1 C1 E1 N1 R1 U1 H2 K2 A3 C3 E3 N3 R3 U3 C4 R4 F5 M5 F10 M10 C11 R11 A12 C12 E12 N12 R12 U12 H13 K13 A14 C14 E14 N14 R14 U14

Title: GPU VRAM D

Size: C | Document Number: Skylake-H | Rev: V0.3

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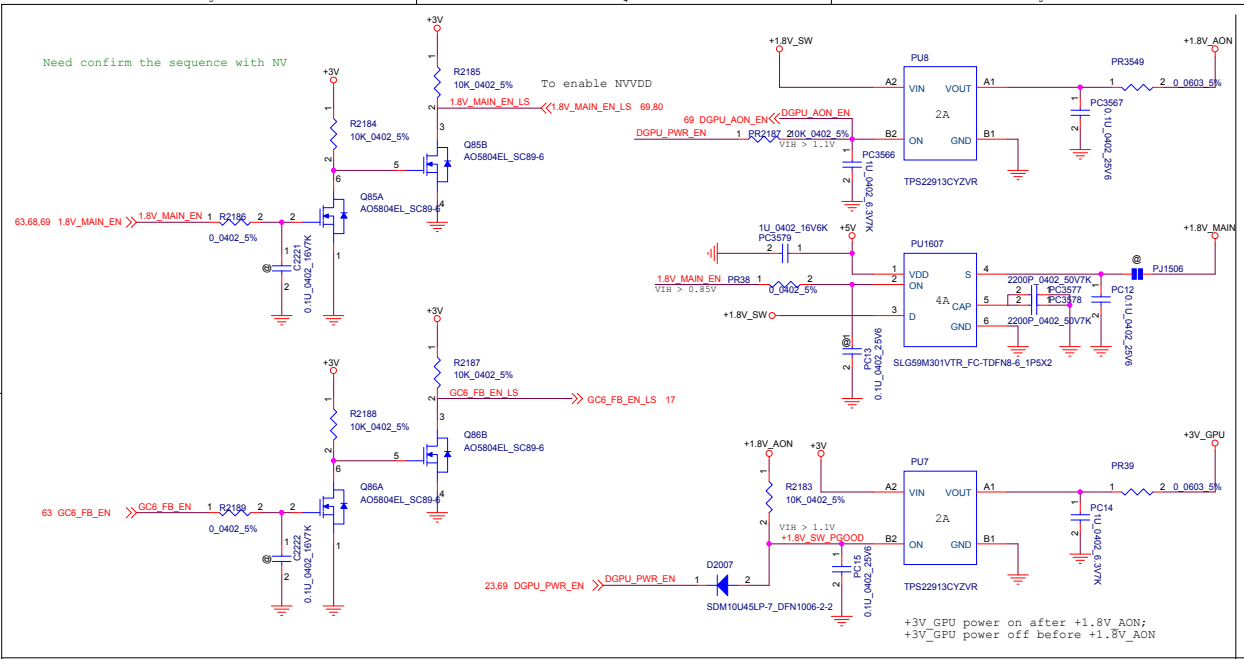

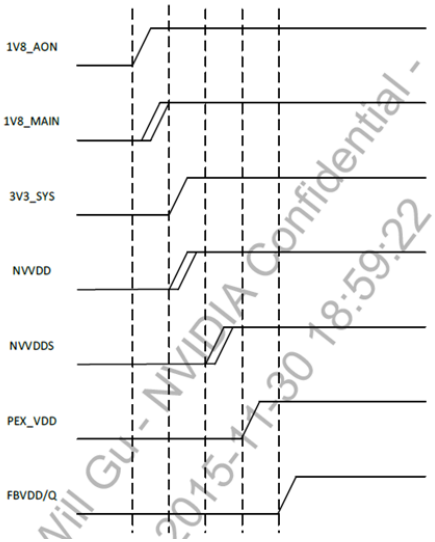

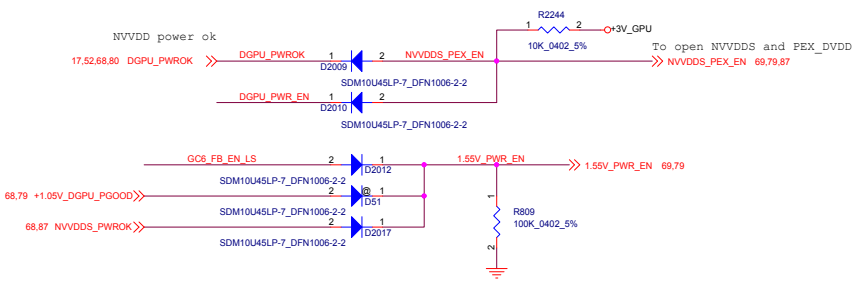

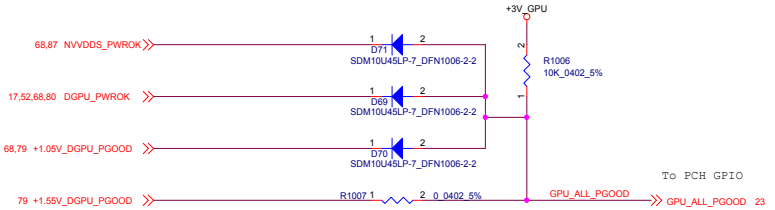

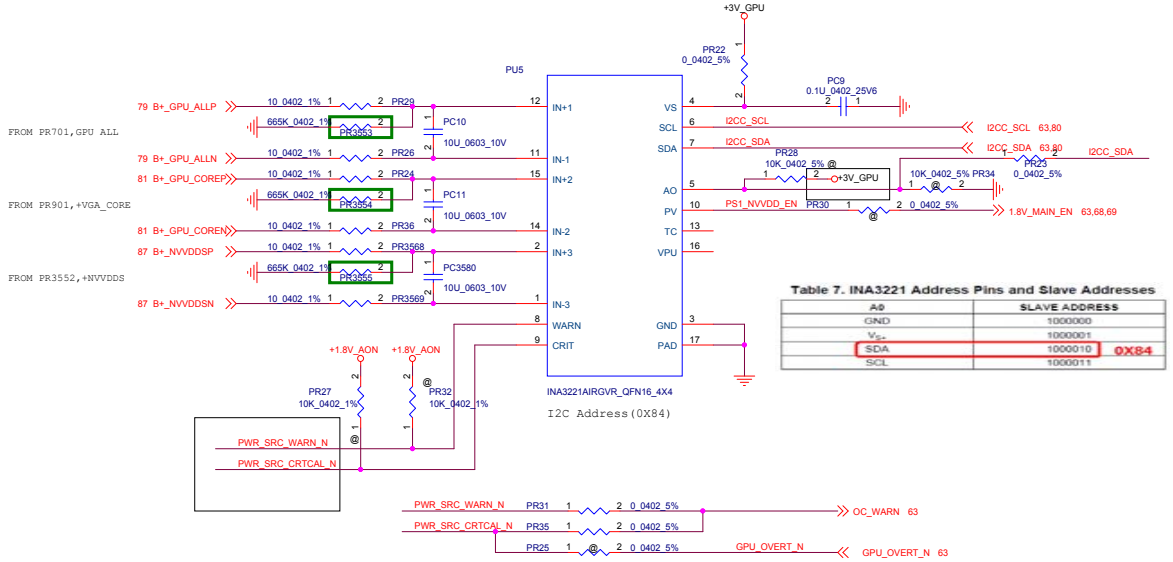

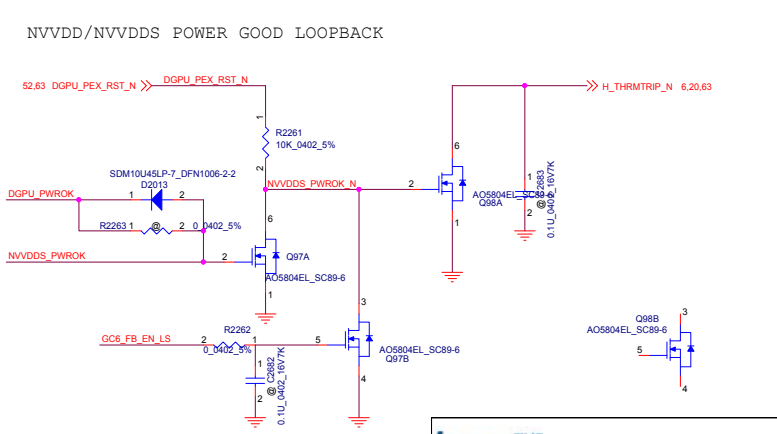

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Title: GPU Switch/Thermal

Size	Document Number	Rev
C	Skylake-H	V0.3

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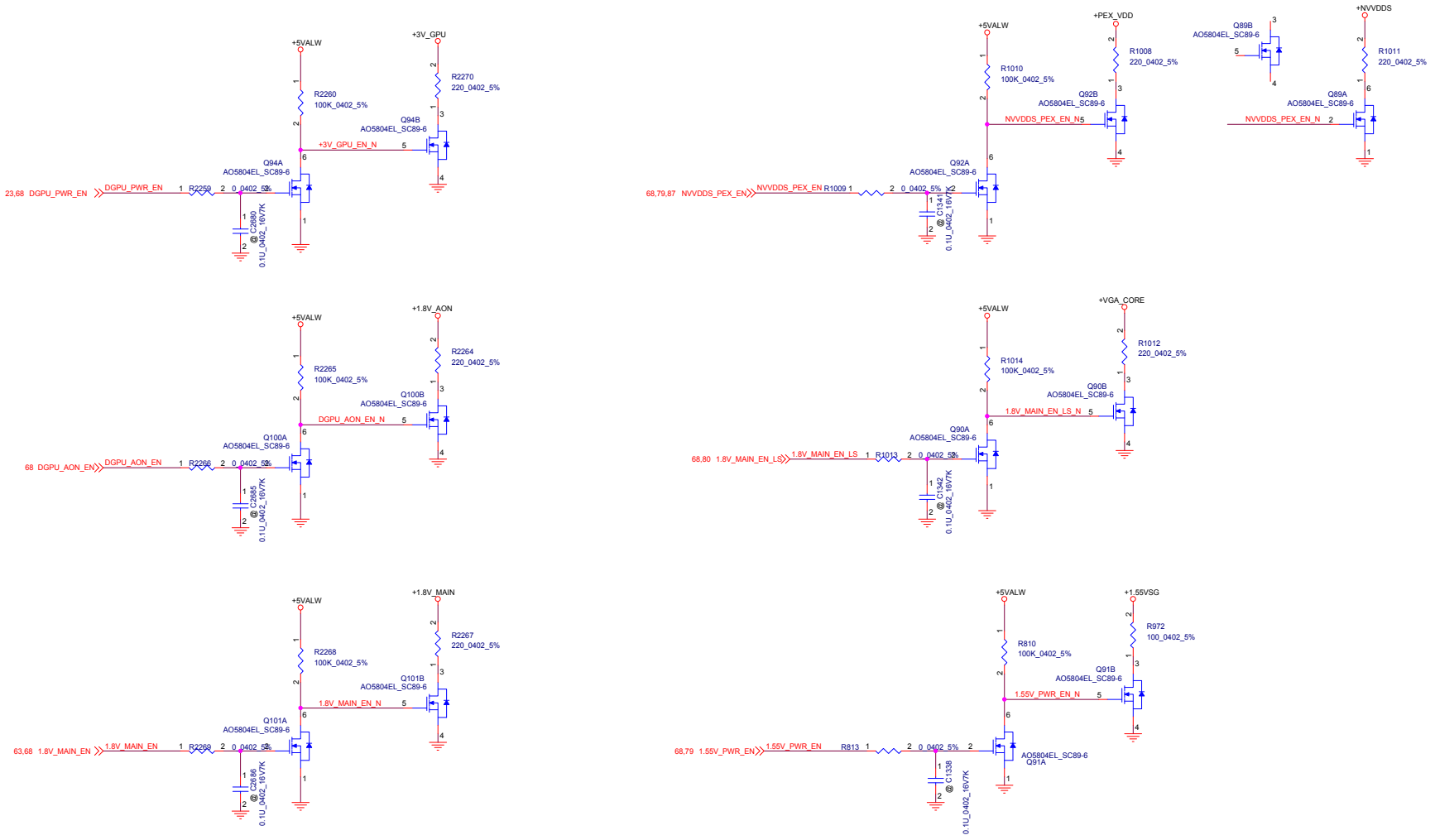

lenovo联想 LENOVO.CRDN

Title: BLANK

Size	Document Number	Rev
C	Skylake-H	V0.3

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lenovo联想 LENOVO.CRDN

Title: BLANK

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lenovo联想 LENOVO.CRDN

Title: BLANK

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lenovo联想 LENOVO.CRDN

Title: BLANK

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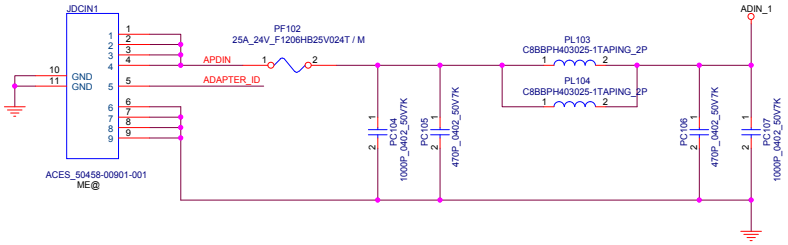
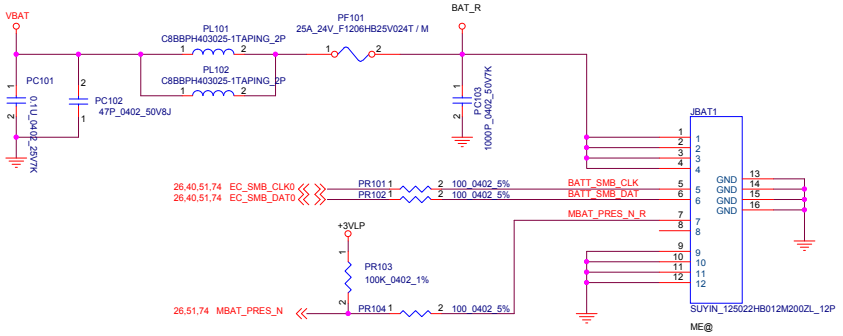
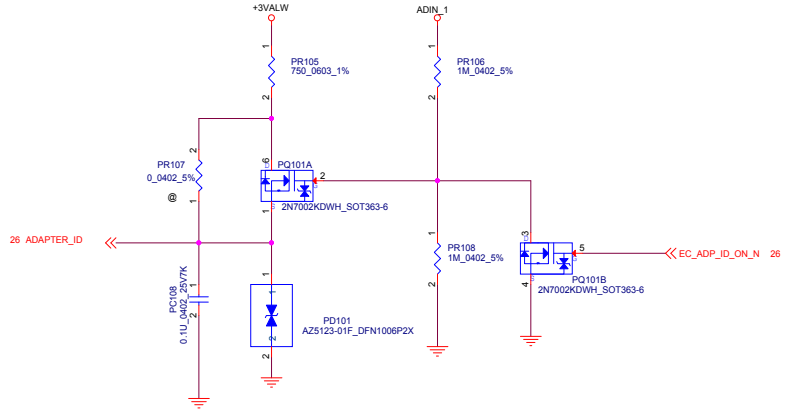
BATT CONN.







lenovo联想	LENOVO.CRDN	
Title	DCIN/BATT	
Size C	Document Number Skylake-H	Rev V0.3
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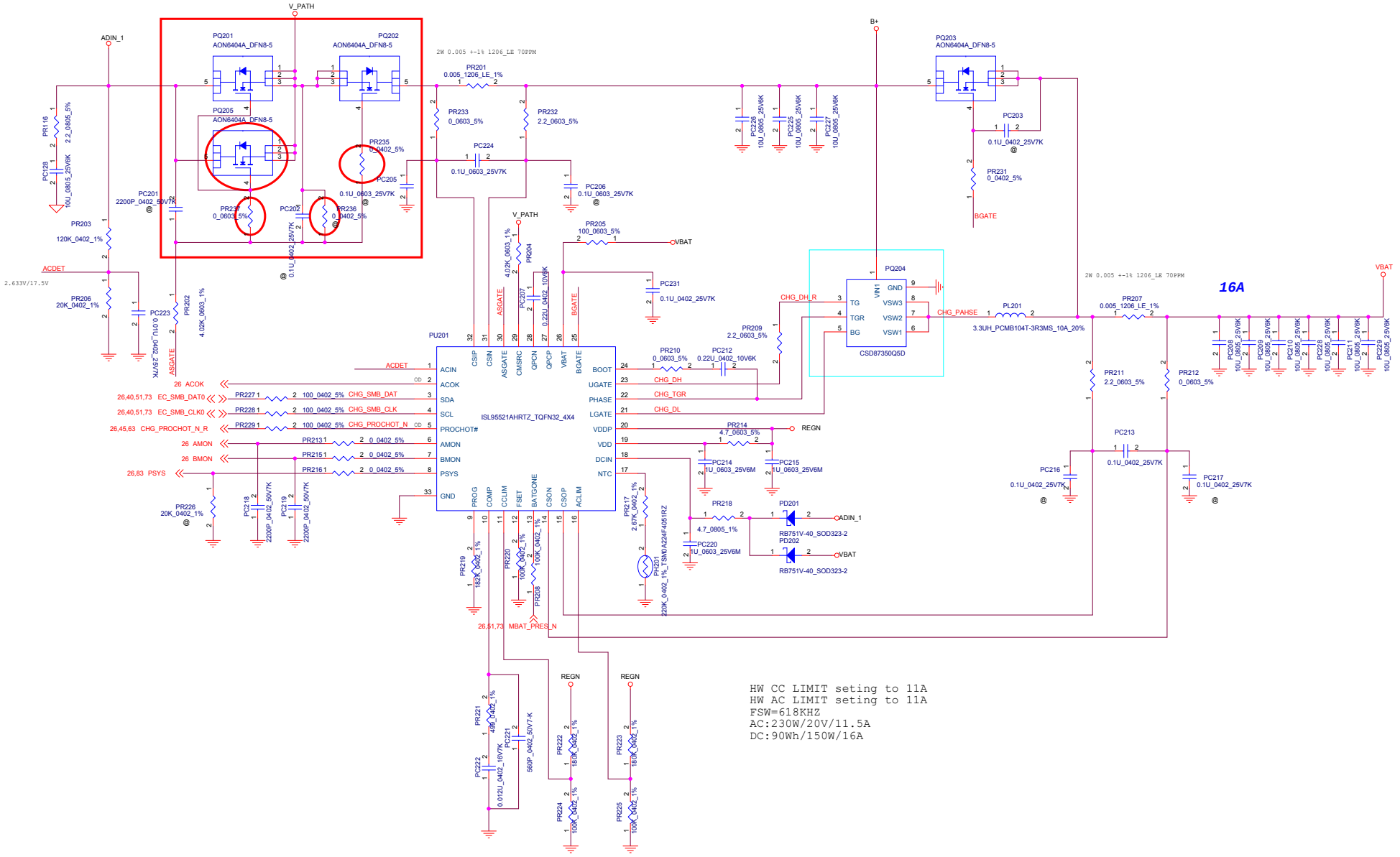

HW CC LIMIT seting to 11A
HW AC LIMIT seting to 11A
FSW=618KHZ
AC:230W/20V/11.5A
DC:90Wh/150W/16A

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Title: PWR Trubo charger ISL95520

Size	Document Number	Rev
C	Skylake-H	V0.3

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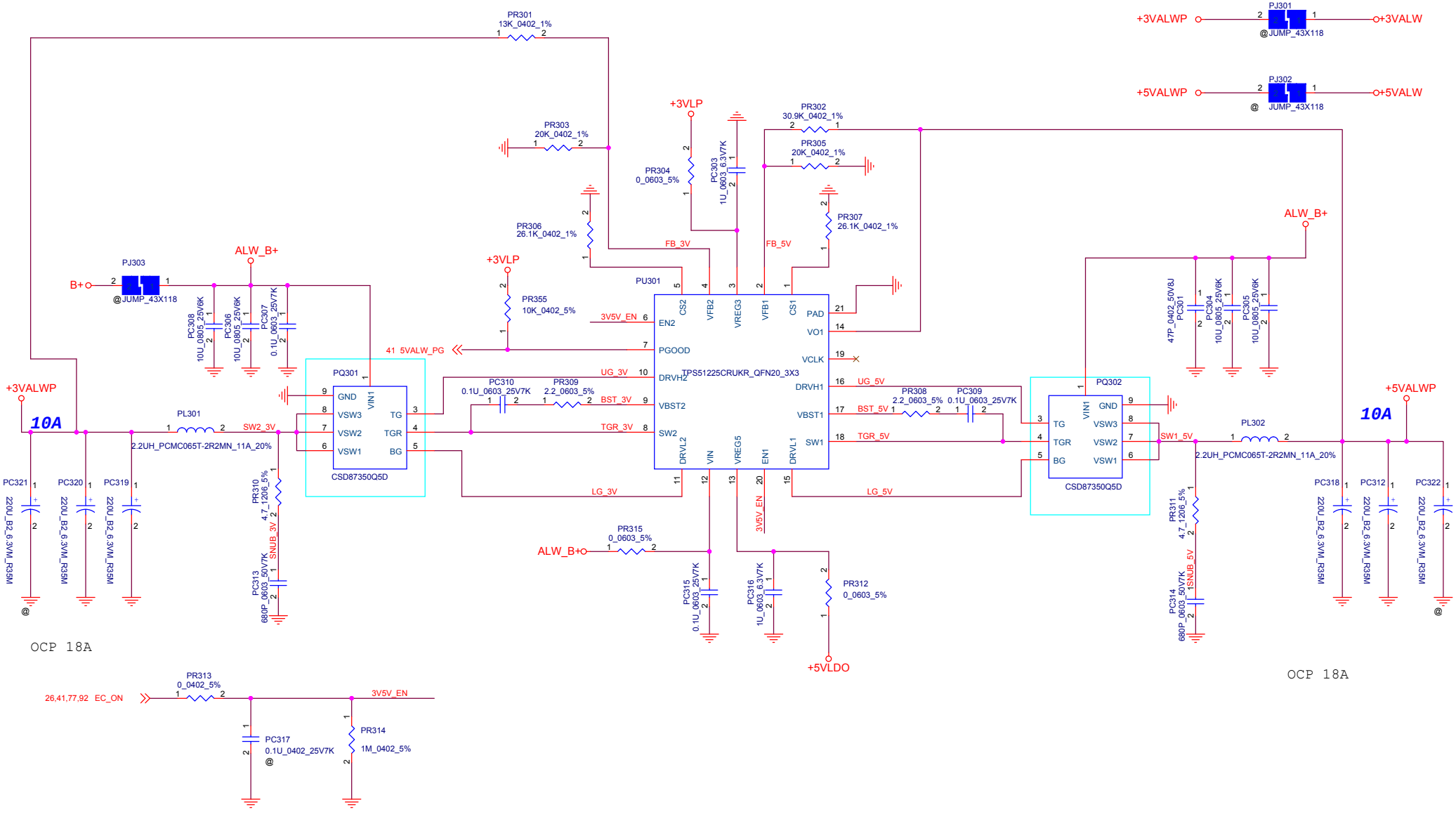

lenovo联想	LENOVO.CRDN	
Title: PWR 3VALW/5VALW		
Size: Custom	Document Number: Skylake-H	Rev: V0.3
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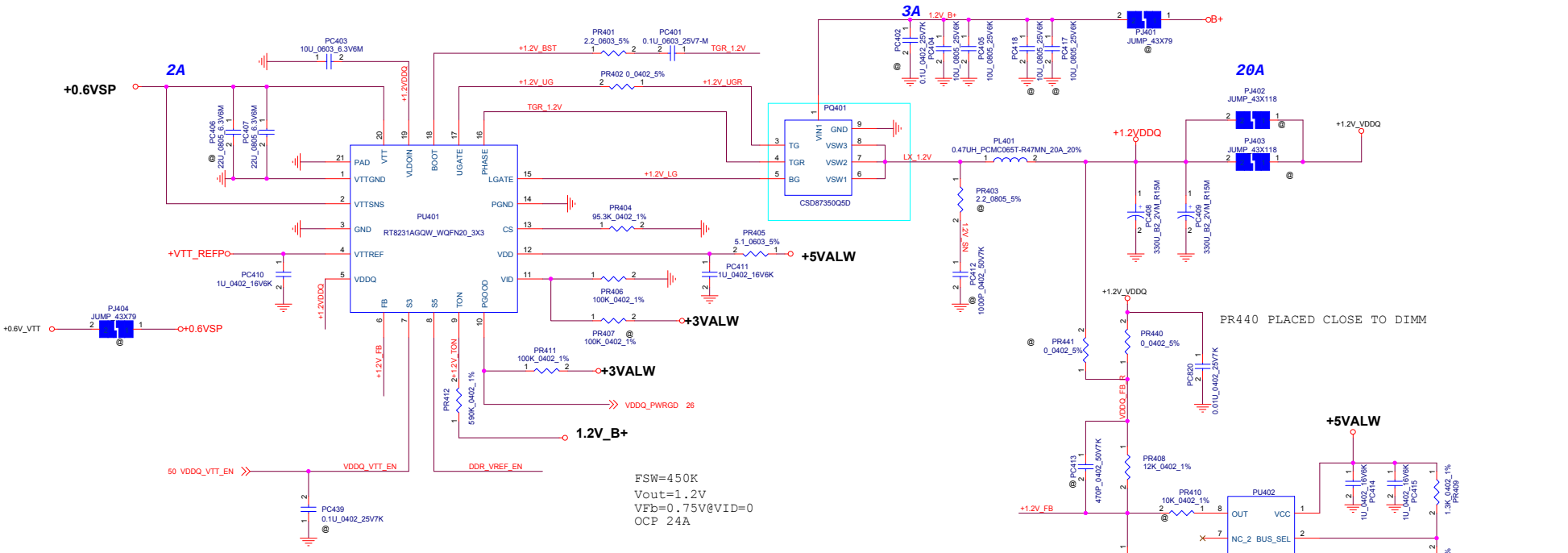
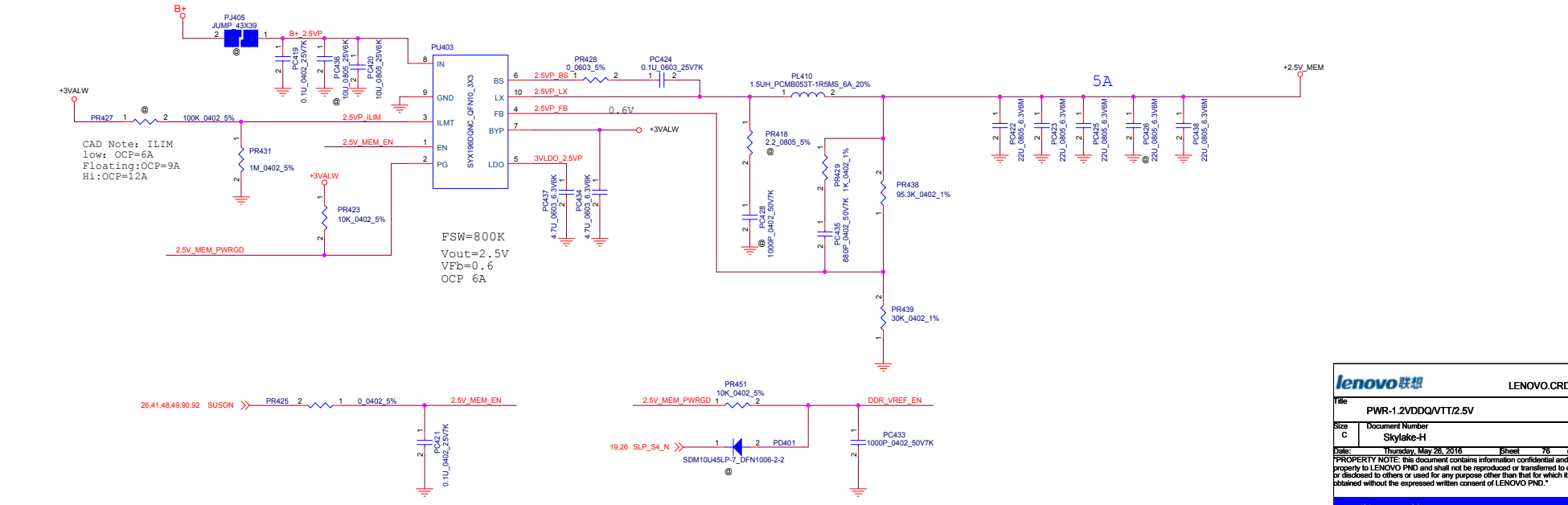


STATE	SUSON	MAINON	+1.2V_VDDQ	+0.6V_VTT
S0	HI	HI	ON	ON
S3	HI	LOW	ON	OFF(HighI-Z)
S5	LOW	LOW	OFF(Discharge)	OFF(Discharge)

Address	0X6A	0X68	0X66	0X64	0X62	0X60
TOP R (Kohm)	OPEN	3.9	3	2.3	1.3	10
BOT R (Kohm)	10	1.3	2.3	3	3.9	OPEN
Bus_sel Volt (% of VCC)	0%	25%	40%	60%	75%	100%



lenovo联想 LENOVO.CRDN

Title: PWR-1.2VDDQ/VTT/2.5V

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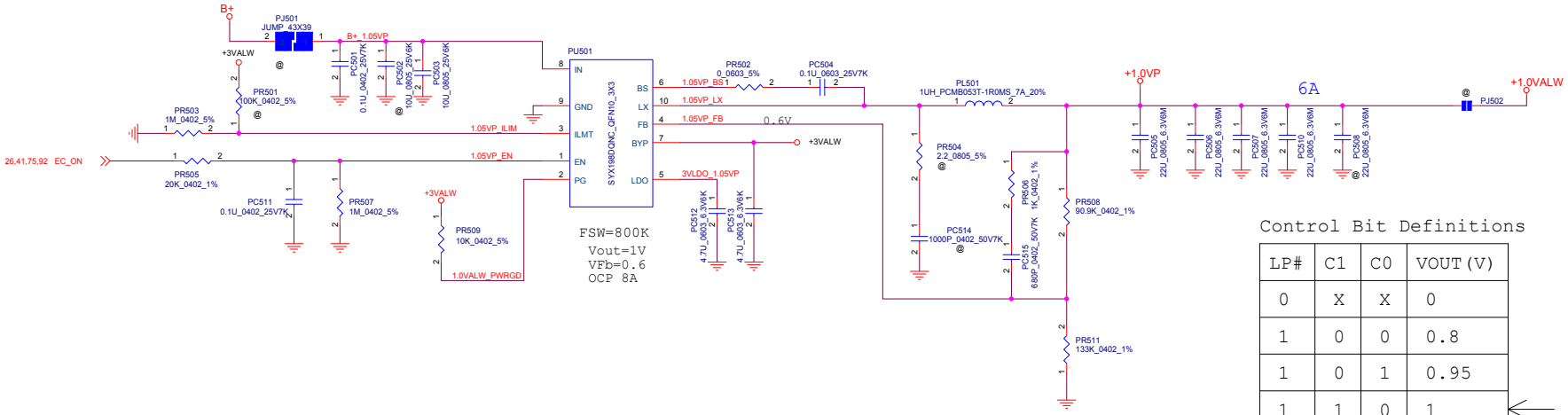

Control Bit Definitions

LP#	C1	C0	VOUT (V)
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1
1	1	1	1.05

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Title: PWR 1.0V/VCCEDRAM/EPIO

Size: C | Document Number: Skylake-H | Rev: V0.3

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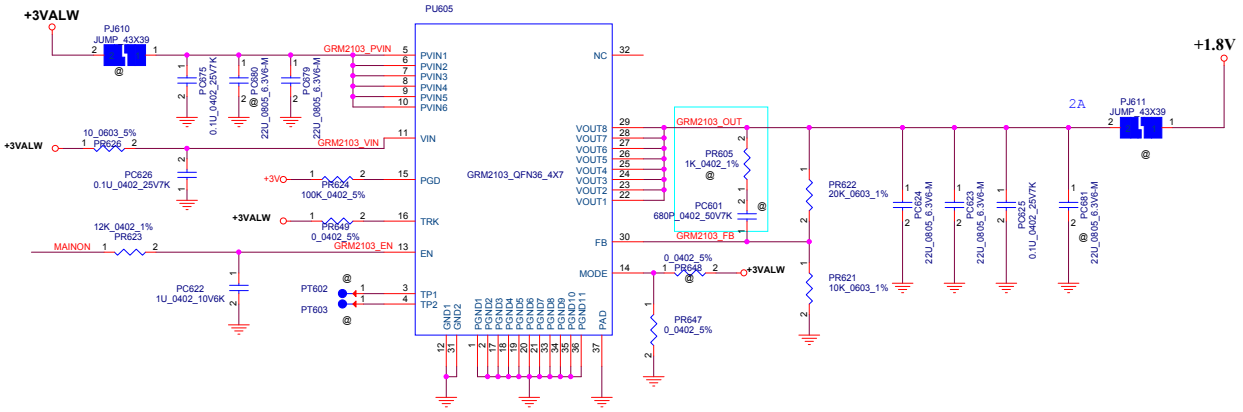

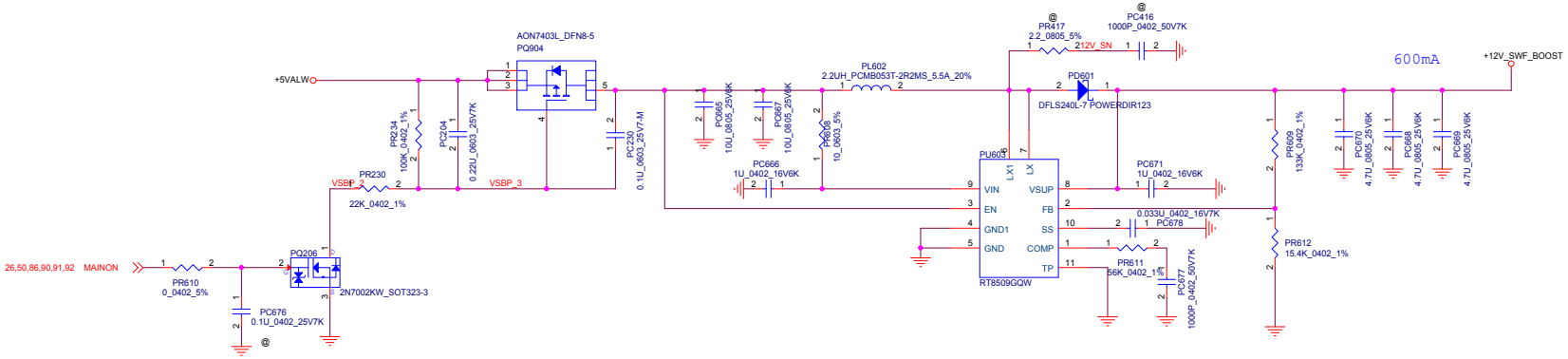

lenovo联想	LENOVO.CRDN	
Title	PWR 1.8V/1.2V/12V Boost	
Size C	Document Number Skylake-H	Rev V0.3
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1.55V GPU Side	
under GPU	Near GPU
24*1uF_0402_X6S	4*10uF_0603_X6S
8*10uF_0603_X6S	9*22uF_0603_X6S

Need one more X63 to fine tune if need 1.5V

1.501V/1.35V:PR3411 6.65K SD03466518J
PR415 45.3K SD03445328J

Vboot=1.55V
DC=±20mV AC=55mV
TDC=32A EDC=58A OCP>70A
Vref=2V
FUVP:Vfb=0.2V
SUVP:Vcomp=3V
OVP:Vfb=2V
Fsw=400KHz
LL: NA

CAD Note: VRAM_VDDQ_ADJ
L = 1.362V
H = 1.55V

VR Remote Sense - Tie to GPU sense points

Vout=1.01V
DC=±3% AC=100mV
TDC=6A EDC=8A OCP≈12A
Vfb=0.6V
UVP: 90% Vfb
OVP: 120% Vfb
Fsw=800KHz

CAD Note: 1.05VG_ILIM
low: OCP=8A
Floating:OCP=12A
Hi:OCP=16A

ADDR 0X62

lenovo联想	LENOVO.CRDN
Title	PWR VRAM/PCIE Power
Size: Custom	Document Number: Skylake-H
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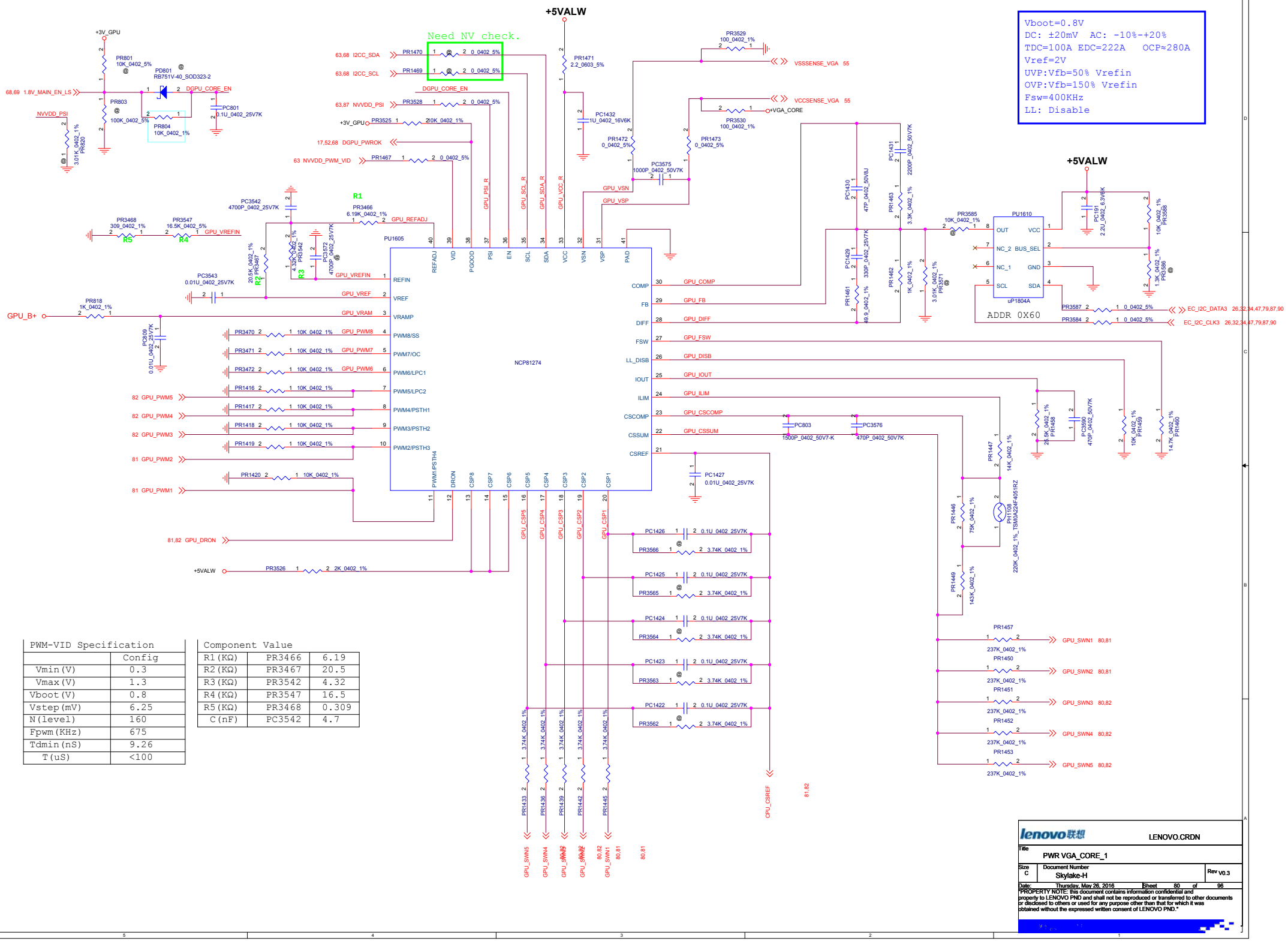
+5VALW
Need NV check.
Vboot=0.8V
DC: ±20mV AC: -10%-+20%
TDC=100A EDC=222A OCP≈280A
Vref=2V
UVP:Vfb=50% Vrefin
OVP:Vfb=150% Vrefin
Fsw=400KHz
LL: Disable
+3V_GPU
68,69 1.8V_MAIN_EN_LS
DGPU_CORE_EN
NVVDD_PSI
63,68 I2CC_SDA
63,68 I2CC_SCL
63,87 NVVDD_PSI
17,52,68 DGPU_PWROK
63 NVVDD_PWM_VID
VSSSENSE_VGA 55
VCCSENSE_VGA 55
+VGA_CORE
GPU_VSN
GPU_VSP
GPU_REFADJ
GPU_VREFIN
GPU_VREF
GPU_VRAM
GPU_B+
NCP81274
REFADJ
VID
PGOOD
PSI
EN
SCL
SDA
VCC
VSN
VSP
PAD
REFIN
VREF
VRAMP
PWM8/SS
PWM7/OC
PWM6/LPC1
PWM5/LPC2
PWM4/PSTH1
PWM3/PSTH2
PWM2/PSTH3
PWM1/PSTH4
DRON
CSP8
CSP7
CSP6
CSP5
CSP4
CSP3
CSP2
CSP1
COMP
FB
DIFF
FSW
LL_DISB
IOUT
ILIM
CSCOMP
CSSUM
CSREF
GPU_COMP
GPU_FB
GPU_DIFF
GPU_FSW
GPU_DISB
GPU_IOUT
GPU_ILIM
GPU_CSCOMP
GPU_CSSUM
GPU_PWM8
GPU_PWM7
GPU_PWM6
GPU_PWM5
GPU_PWM4
GPU_PWM3
GPU_PWM2
GPU_PWM1
GPU_DRON
GPU_CSP5
GPU_CSP4
GPU_CSP3
GPU_CSP2
GPU_CSP1
GPU_CSREF
GPU_SWN5
GPU_SWN4
GPU_SWN3
GPU_SWN2
GPU_SWN1
PU1605
PU1610
uP1804A
ADDR 0X60
EC_I2C_DATA3 26,32,34,47,79,87,90
EC_I2C_CLK3 26,32,34,47,79,87,90
PWM-VID Specification
Config
Vmin(V) 0.3
Vmax(V) 1.3
Vboot(V) 0.8
Vstep(mV) 6.25
N(level) 160
Fpwm(KHz) 675
Tdmin(nS) 9.26
T(uS) <100
Component Value
R1(KΩ) PR3466 6.19
R2(KΩ) PR3467 20.5
R3(KΩ) PR3542 4.32
R4(KΩ) PR3547 16.5
R5(KΩ) PR3468 0.309
C(nF) PC3542 4.7
LENOVO.CRDN
PWR VGA_CORE_1
Skylake-H
Rev V0.3
Thursday, May 26, 2016
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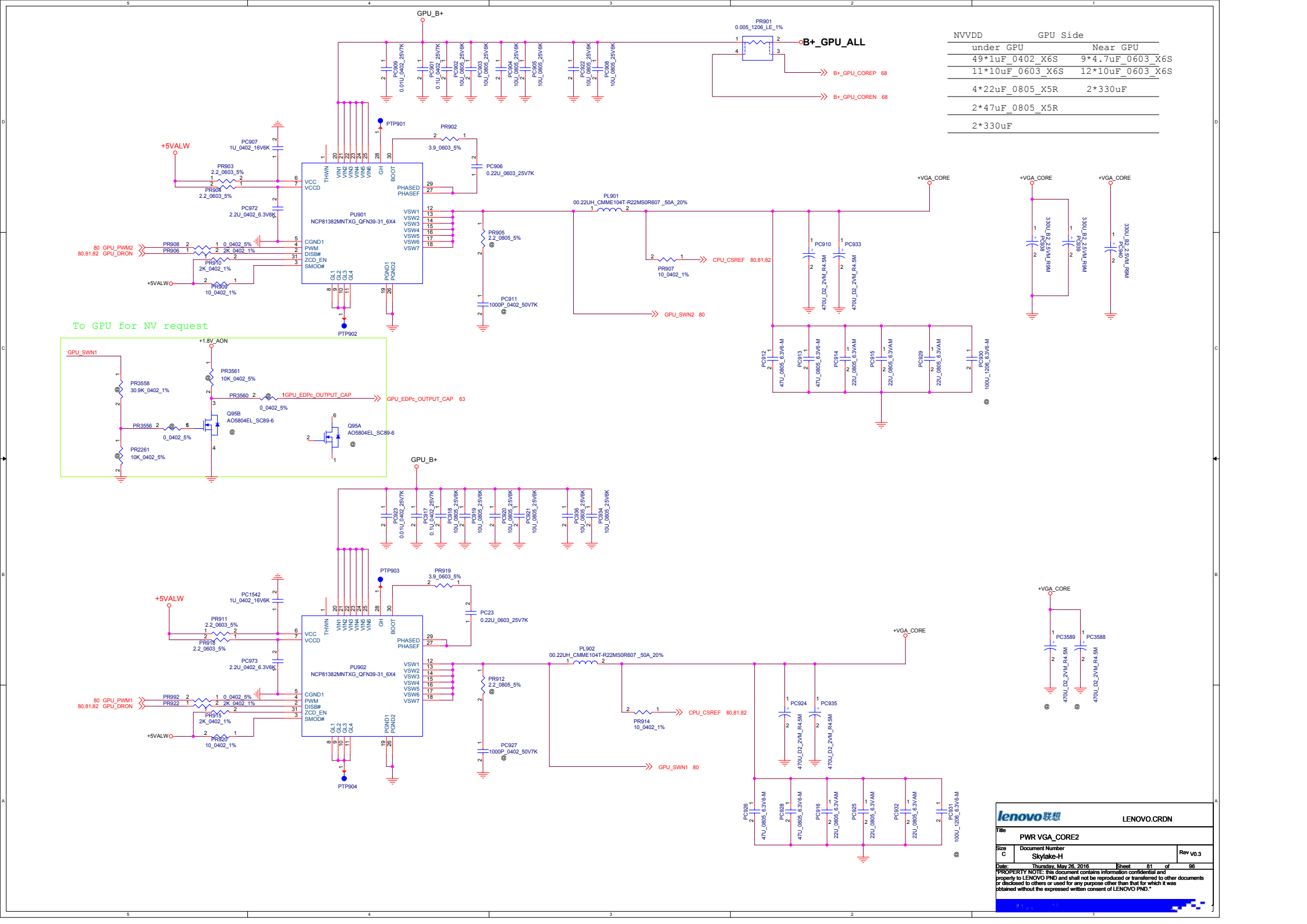

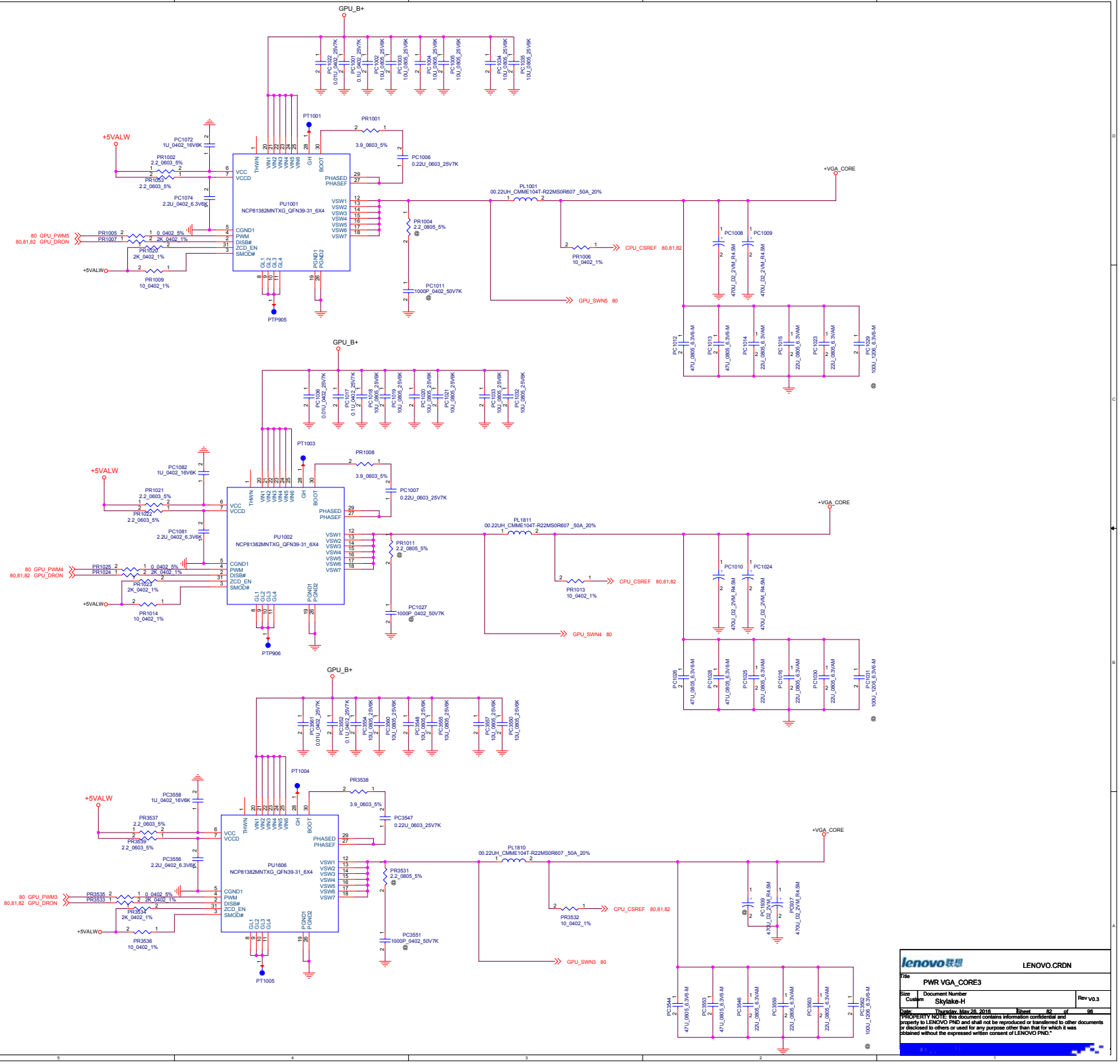

Title	PWR VGA_CORE3
Size	Custom
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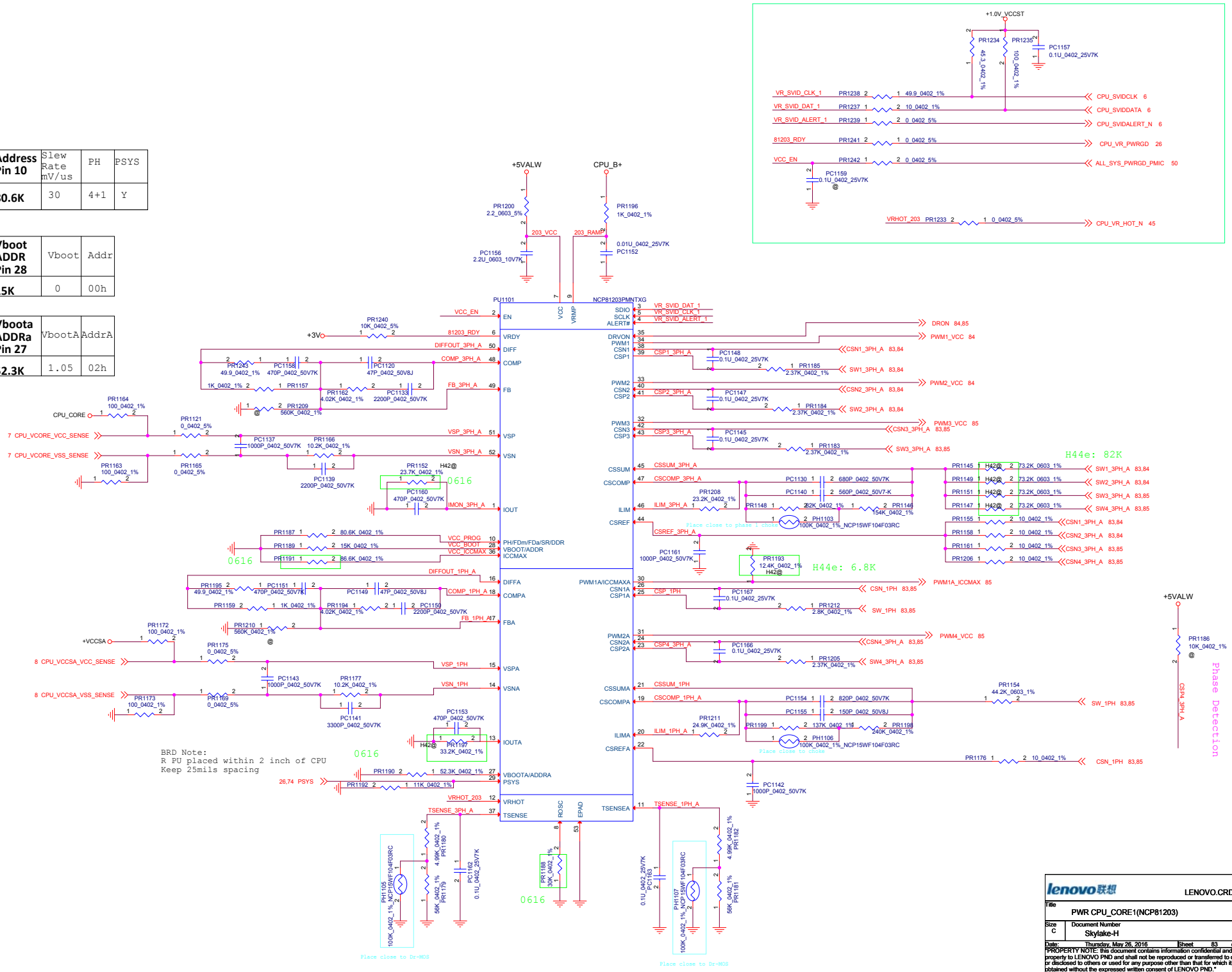
Address Pin 10	Slew Rate mV/us	PH	PSYS
80.6K	30	4+1	Y

Vboot ADDR Pin 28	Vboot	Addr
15K	0	00h

Vboota ADDRa Pin 27	VbootA	AddrA
52.3K	1.05	02h



lenovo联想	LENOVO.CRDN	
Title	PWR CPU_CORE1(NCP81203)	
Size C	Document Number Skylake-H	Rev V0.3
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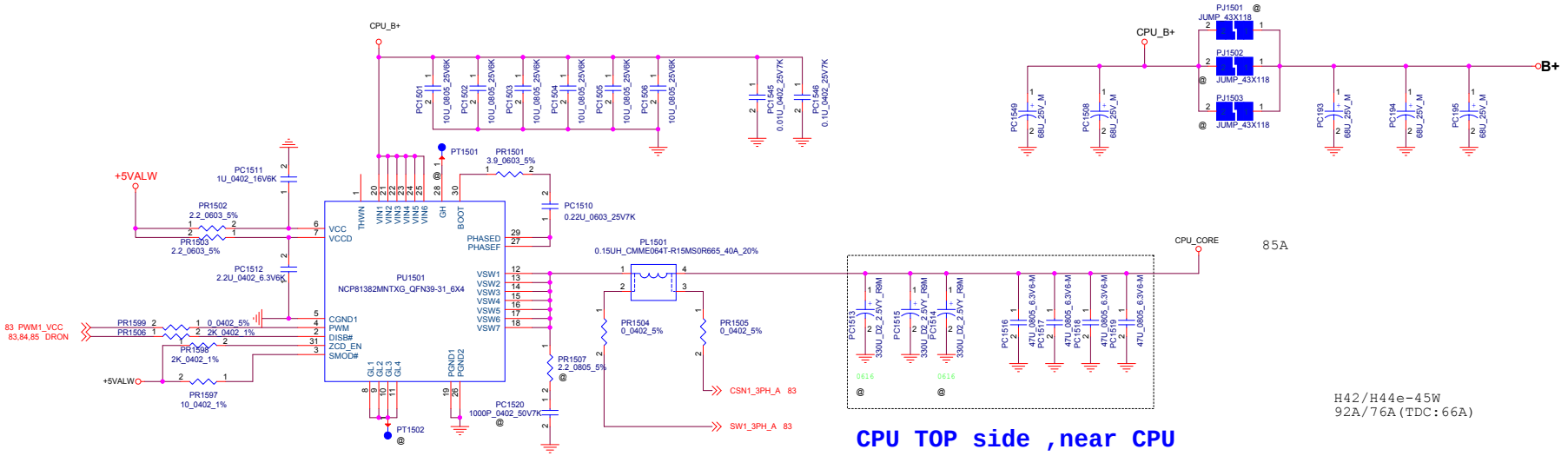
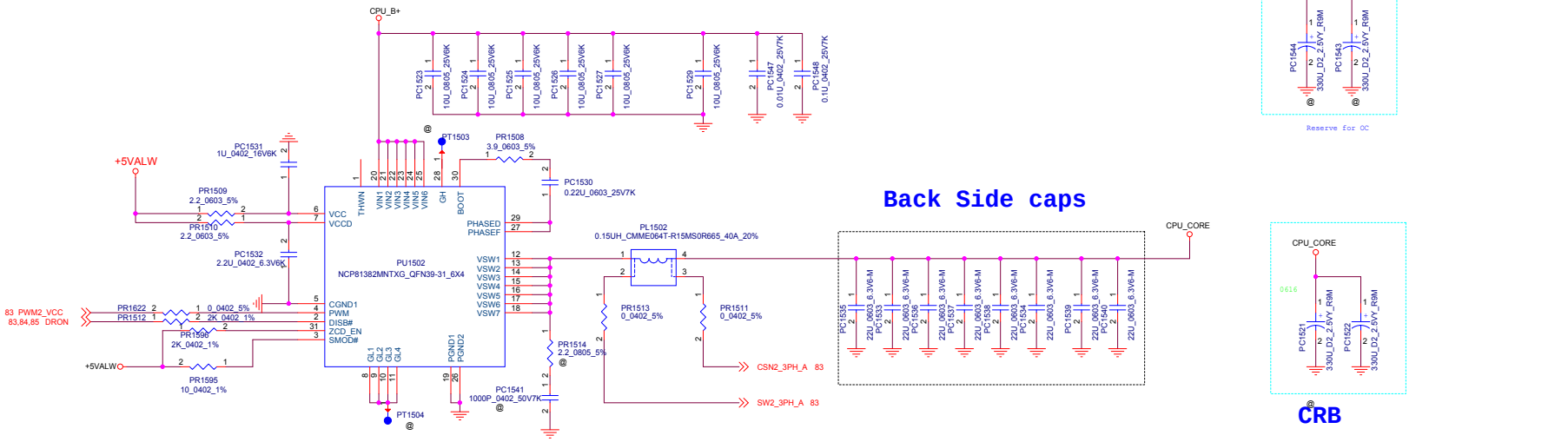


CPU TOP side ,near CPU



Back Side caps

	CPU BACK				CPU TOP	
CRB	220	22	10	1	220	47
	2V	0603	0402	0201	2V	0805
pcs	3	8	28	63	2	4

1,PDG 3*220uF TOP ,no Back; follow CRB/PDG;
2,47uF,22uF follow CRB;
3,Reserve 16pcs 22uF for OC;
4,10uF/1uF double check EE side
5,Total Cap double check with Vendor

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Title: PWR CPU_CORE2(NCP81382)

Size: C | Document Number: Skylake-H | Rev: V0.3

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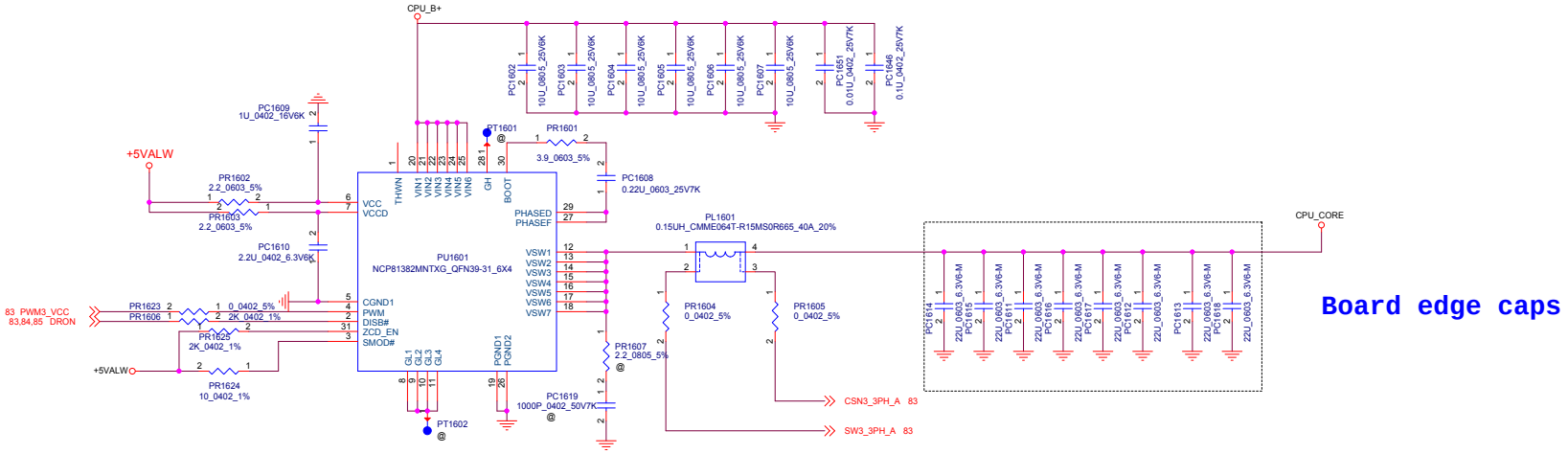

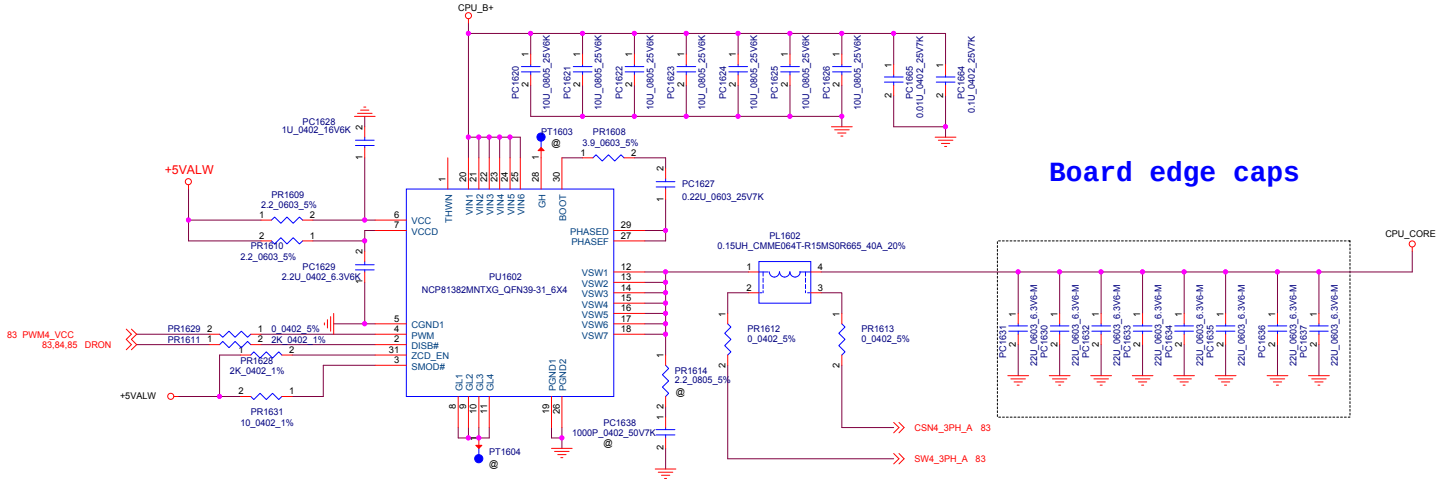

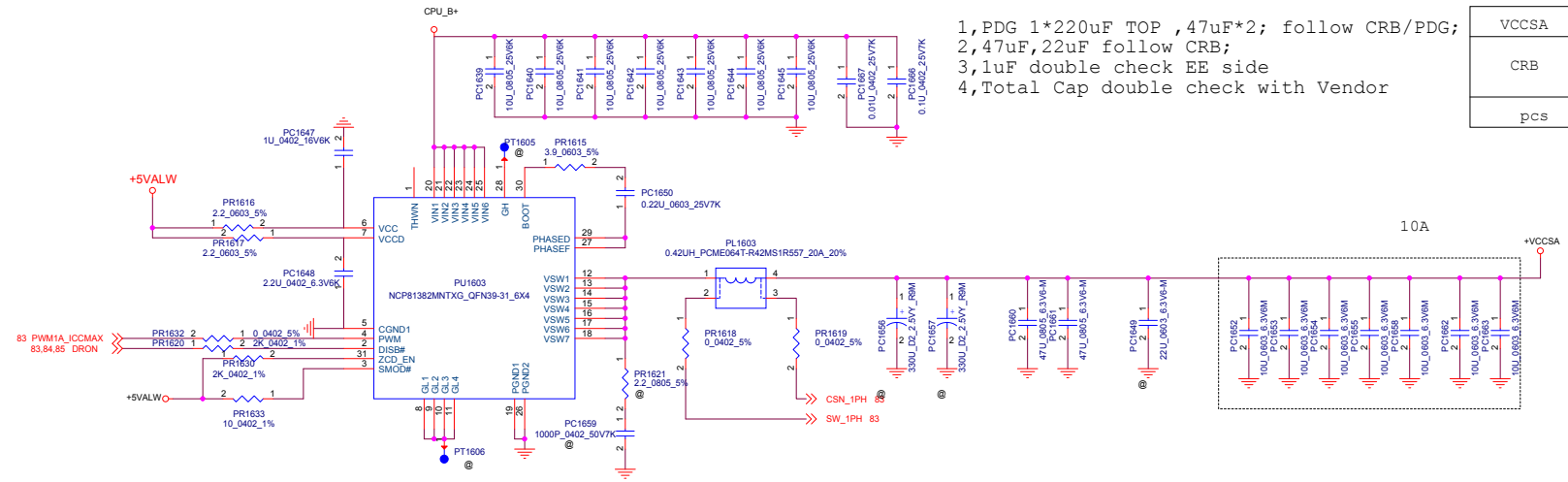

1,PDG 1*220uF TOP ,47uF*2; follow CRB/PDG;
2,47uF,22uF follow CRB;
3,1uF double check EE side
4,Total Cap double check with Vendor

VCCSA	CPU BACK				CPU TOP	
CRB	220	47	10	1	220	22
	2V	0805	0402	0201	2V	0603
pcs	0	1	7	3	2	1

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Title: PWR CPU_CORE3(NCP81382)

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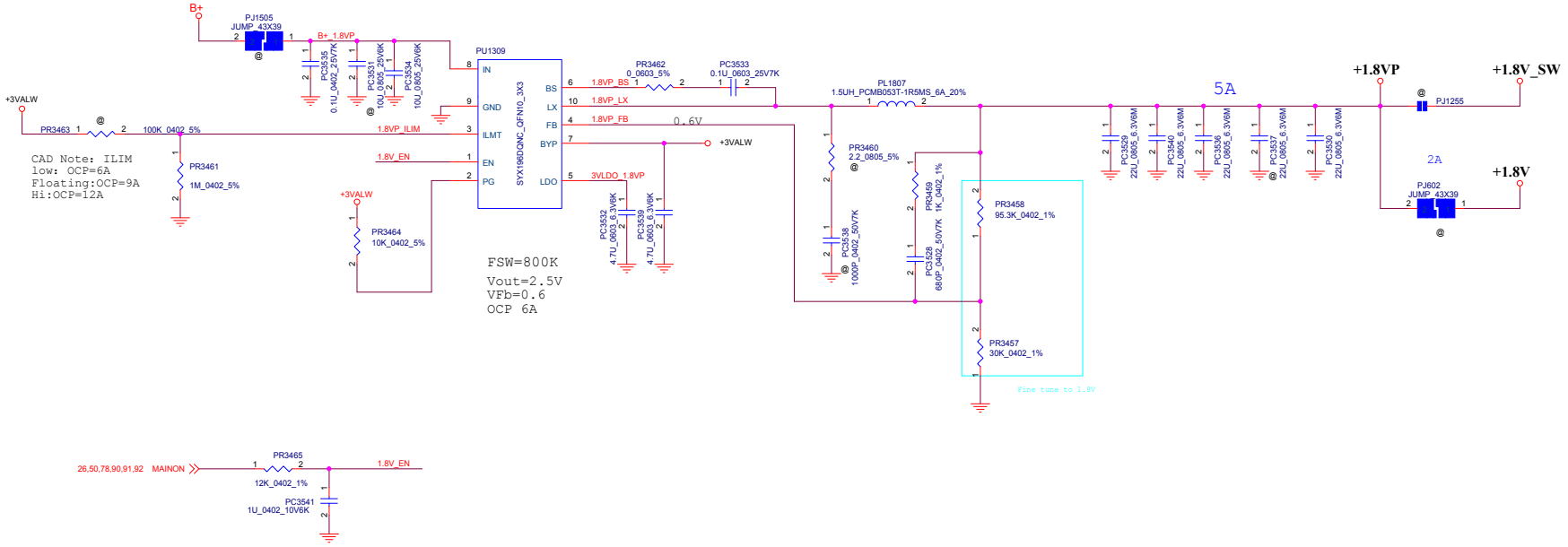

lenovo联想	LENOVO.CRDN	
Title: PWR 1V8AON		
Size: C	Document Number: Skylake-H	Rev: V0.3
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PWM-VID Specification	
	Config
Vmin(V)	0.3
Vmax(V)	1.3
Vboot(V)	0.8
Vstep(mV)	6.25
N(level)	160
Fpwm(KHz)	675
Tdmin(nS)	9.26
T(uS)	<100

Component Value		
R1(KΩ)	PR3433	6.19
R2(KΩ)	PR3431	20.5
R3(KΩ)	PR3540	4.32
R4(KΩ)	PR3432	16.5
R5(KΩ)	PR3541	0.309
C(nF)	PC1277	4.7

NVVDDS GPU Side	
under GPU	Near GPU
16*1uF_0402_X6S	2*10uF_4.7uF_X6S
4*10uF_0603_X6S	1*47uF_0805_X5R
1*330uF	

Vboot=0.8V
DC=±20mV AC: -10%~+20%
TDC=28A EDC=67A OCP>80A
Vref=2V
FUVP:Vfb=0.2V
SUVP:Vcomp=3V
OVP:Vfb=2V
Fsw=400KHz
LL: NA

+5VALW
PR3442 2_0603_5%
NVVDDS_PVCC 18
PC3509 1U_0402_6.3V6K
PVCC
THERM/GND
21
+3V_GPU
PR3570 0_0402_5%
PR3454 10K_0402_5%
PR3428 10K_0402_1%
63,80 NVVDD_PSI
63 NVVDDS_PSI
PR3436 0_0402_5%
PR3449 10K_0402_1%
NVVDDS_PSI_R 4
PSI
+3V_GPU
68 NVVDDS_PWROK
PR3426 0_0402_5%
PGOOD 13
68,69,79 NVVDDS_PEX_EN
PR3550 0_0402_5%
NVVDDS_EN_R 3
EN
PC3505 0.1U_0402_25V7K
Power on before 1.05v;
Power down before 1.05v
63 NVVDDS_PWM_VID
PR3439 0_0402_5%
NVVDDS_VID_R 5
VID
PC3510 @ 0.1U_0402_10V7K
NVVDDS_VREF 8
VREF
PR3431 20.5K_0402_1% R2
PC3507 0.01U_0402_25V7K
PC3520 @ 470P_0402_25V7K
PR3540 4.32K_0402_1% R3
NVVDDS_REFIN 7
REFIN
PR3541 309_0402_1% R5
PR3432 16.5K_0402_1% R4
NVVDDS_VIDBUF 6
VIDBUF
PR3433 6.19K_0402_1% R1
PC3518 4700P_0402_50V7K
NVVDDS_FS 9
PR3440 39K_0402_1%
FS
PU1604
NCP81278MNTXG_QFN20_3X3
HG1 2 NVVDDS_HG1
BST1 1 NVVDDS_BS1
PR3434 2.2_0603_5%
PC3515 0.22U_0603_25V7K
PH1 20 NVVDDS_TGR1
LG1 19 NVVDDS_LG1
HG2 14 NVVDDS_HG2
BST2 15 NVVDDS_BS2
PR3445 2.2_0603_5%
PC3519 0.22U_0603_25V7K
PH2 16 NVVDDS_TGR2
LG2 17 NVVDDS_LG2
FBRTN 10 NVVDDS_FBRTN
FB 11 NVVDDS_FB
COMP/ILMT 12 NVVDDS_COMP
PC3516 82P_0402_50V8J
PR3446 33.2K_0402_1%
PR3444 23.7K_0402_1%
COMP31_NVS 1
PC3571 2200P_0402_25V7-K
PR3441 124_0402_1%
COMP32_NVS 1
PC3514 1000P_0402_25V7-K
PR3438 10K_0402_1%
PC3506 @ 1000P_0402_25V7-K
PR3579 10K_0402_1%
PU1609
uP1804A
OUT VCC
NC_2 BUS_SEL
NC_1 GND
SCL SDA
PC3182 2.2U_0402_6.3V6K
PR3582 1.3K_0402_1%
PR3581 10K_0402_1%
PR3583 2 0_0402_5% EC_I2C_DATA3 26,32,34,47,79,80,90
PR3580 2 0_0402_5% EC_I2C_CLK3 26,32,34,47,79,80,90
ADDR 0X6A
NVVDDS_B+
PR3552 0.005_1206_LE_1%
B+_GPU_ALL
B+_NVVDDSP 68
B+_NVVDDSN 68
PC3511 EMC_NS@ 2200P_0402_25V7K
PC3520 10U_0805_25V6K
PC3523 10U_0805_25V6K
PC3522 10U_0805_25V6K
PC3521 10U_0805_25V6K
PQ1411
CSD87350Q5D
VIN1 GND
TG VSW3
TGR VSW2
BG VSW1
PL1808 0.22UH_PCMC065T-R22MN_30A_20%
NVVDDS_PH1
PR3447 4.7_0805_5% EMC_NS@
2N5 SIGDVN
PC3508 1000P_0402_50V9-J EMC_NS@
+NVVDDS
PC2268 330U_D2_2.5VY_R6M
PC1799 330U_D2_2.5VY_R6M
PC1800 330U_D2_2.5VY_R6M
PC1801 330U_D2_2.5VY_R6M
PC3504 330U_D2_2.5VY_R6M
PC3505 330U_D2_2.5VY_R6M
PC3512 EMC_NS@ 2200P_0402_25V7K
PC3524 10U_0805_25V6K
PC3525 10U_0805_25V6K
PC3527 10U_0805_25V6K
PC3526 10U_0805_25V6K
PQ1412
PL1809 0.22UH_PCMC065T-R22MN_30A_20%
PR3443 4.7_0805_5% EMC_NS@
PC3513 1000P_0402_50V9-J EMC_NS@
PR3448 100_0402_1%
PR3436 0_0402_5%
VSSSENSE_NVVDDS 55
VR Remote Sense - Tie to GPU sense points
PR3437 0_0402_5%
VCCSENSE_NVVDDS 55
PR3435 100_0402_1%
+NVVDDS
PC1802 4.7U_0603_6.3V6K
PC1803 4.7U_0603_6.3V6K
PC1804 4.7U_0603_6.3V6K
PC1805 4.7U_0603_6.3V6K
PC1806 4.7U_0603_6.3V6K
PC1807 4.7U_0603_6.3V6K
PC1808 4.7U_0603_6.3V6K
PC1809 4.7U_0603_6.3V6K
PC1810 4.7U_0603_6.3V6K
PC1811 4.7U_0603_6.3V6K
Under GPU
PC1812 0.1U_0402_25V7K
PC1813 0.1U_0402_25V7K
PC1814 0.1U_0402_25V7K
PC1815 0.1U_0402_25V7K
PC3568 47U_0805_6.3V6-M
PC3569 47U_0805_6.3V6-M
PC2264 4.7U_0805_25V6K
PC1417 4.7U_0805_25V6K
PC1418 4.7U_0805_25V6K
PC1419 4.7U_0805_25V6K
PC1420 4.7U_0805_25V6K
Near GPU

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Title: PWR VGA_NVVDDS
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Title: PWR CPU_CORE6(NCP81382)

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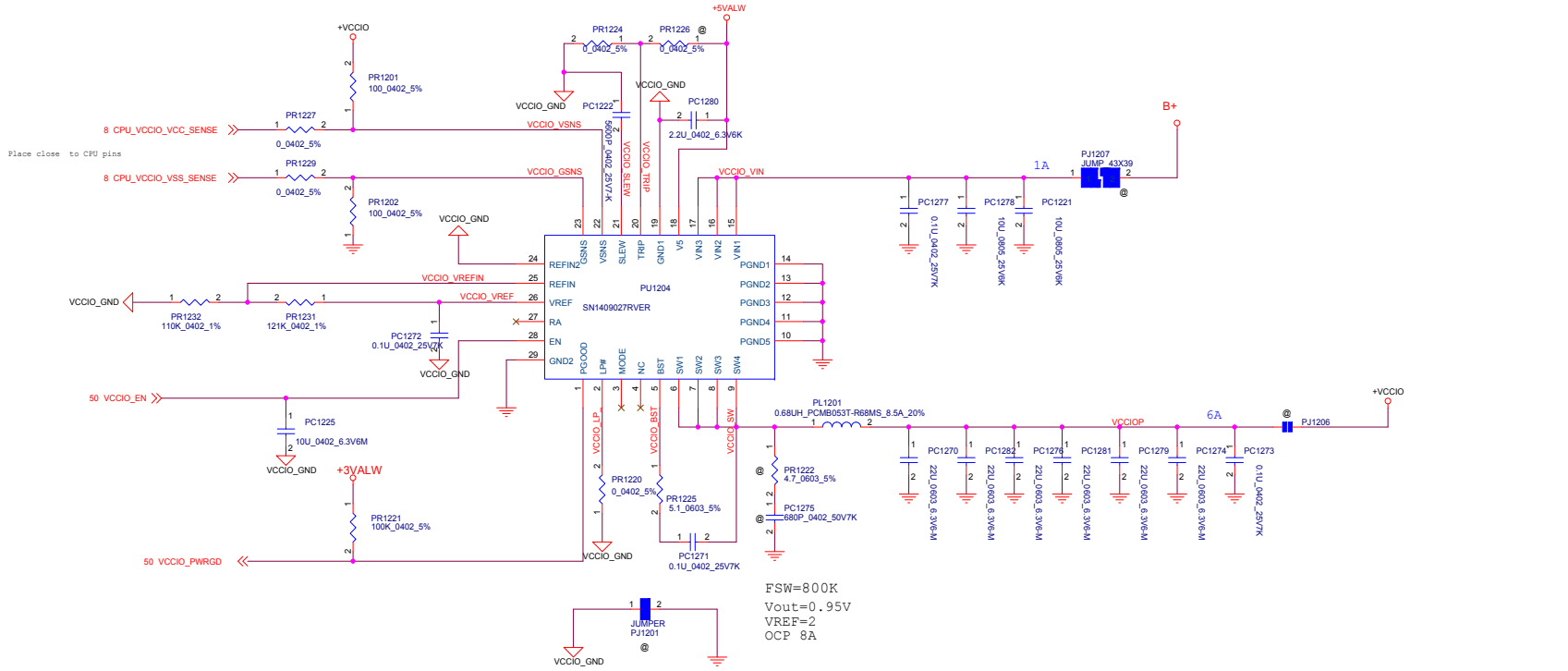

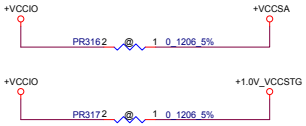

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Title: PWR VCCIO

Size: C | Document Number: Skylake-H | Rev: V0.3

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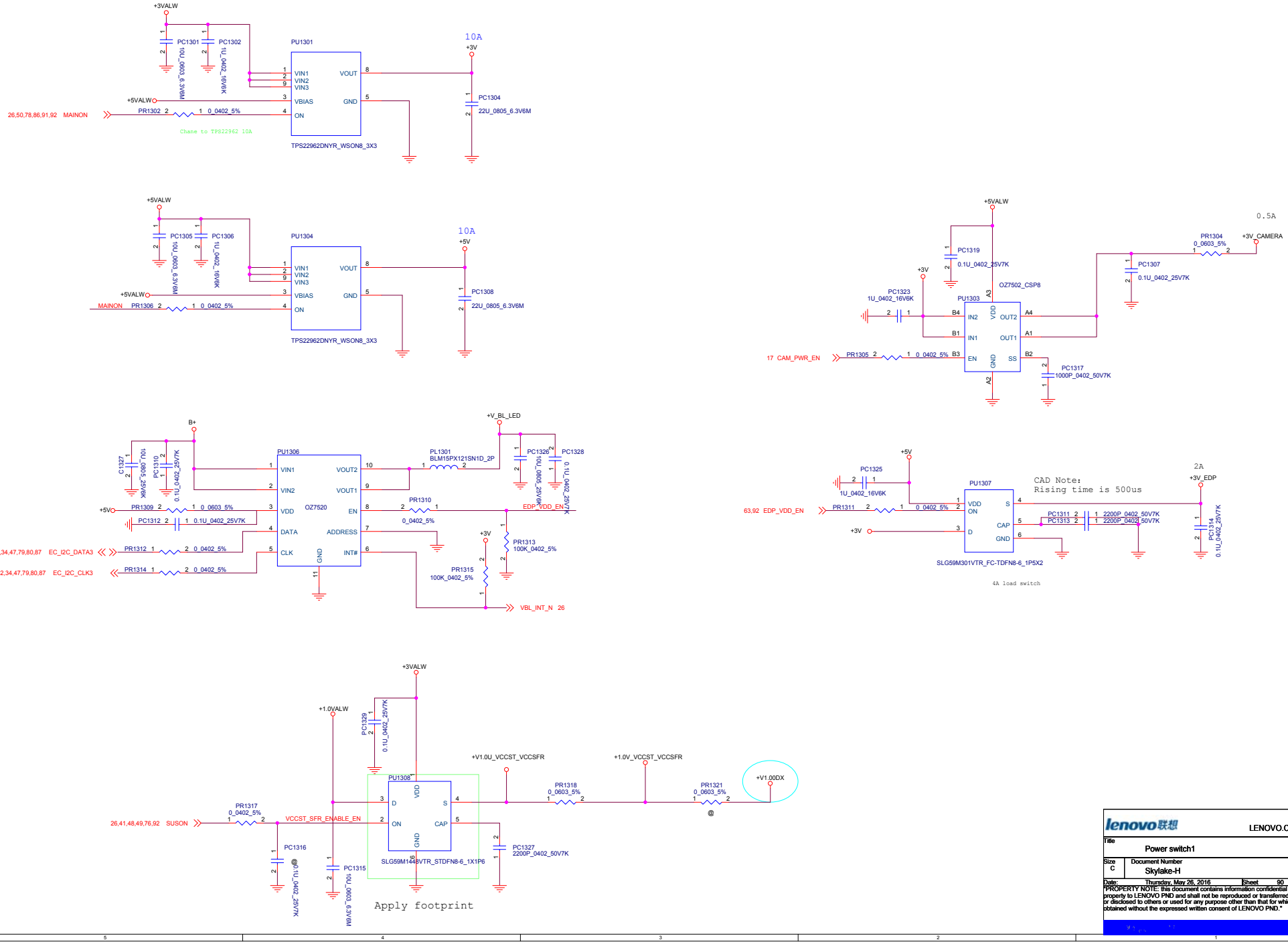

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Title: Power switch1

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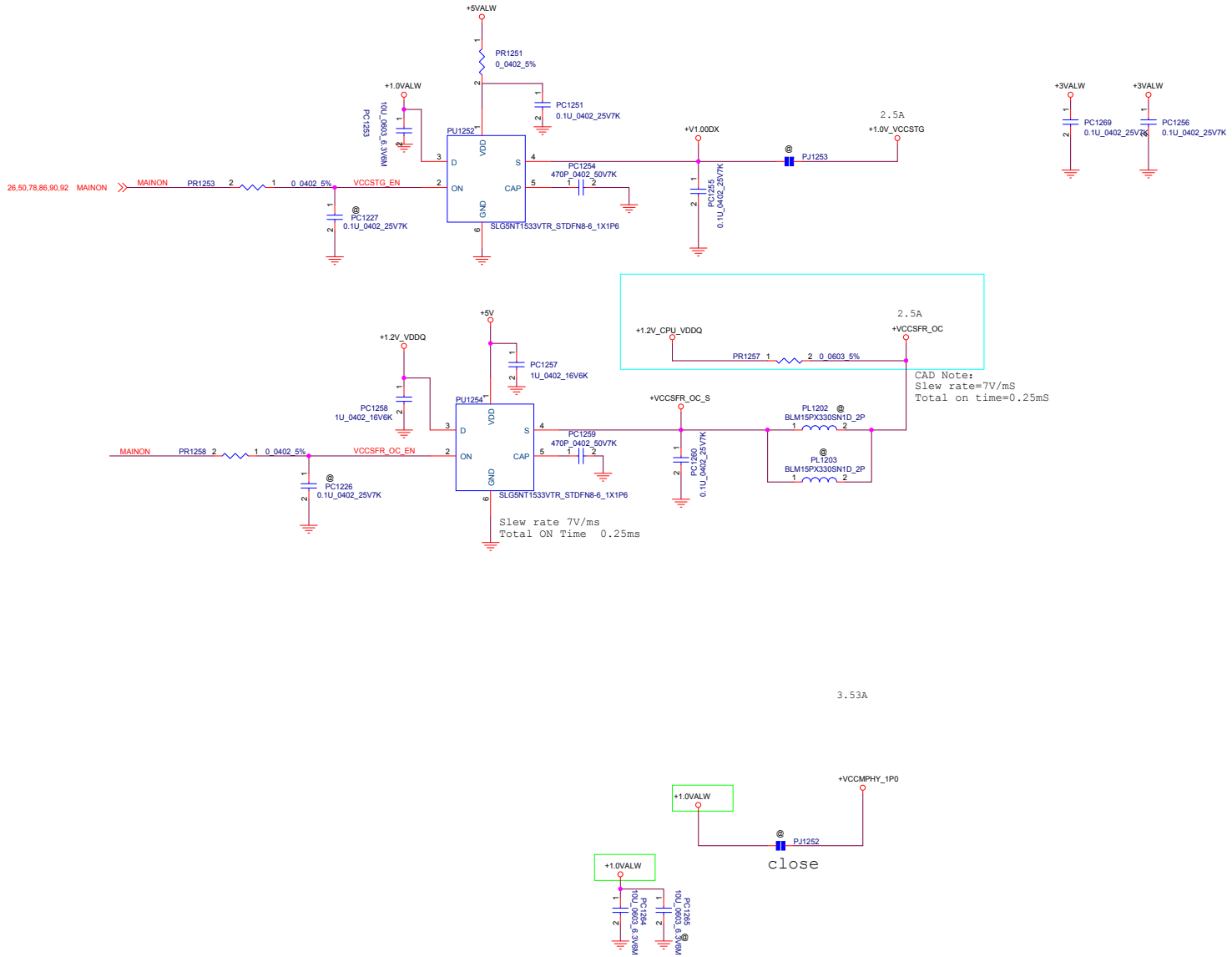

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Title	Power switch2	
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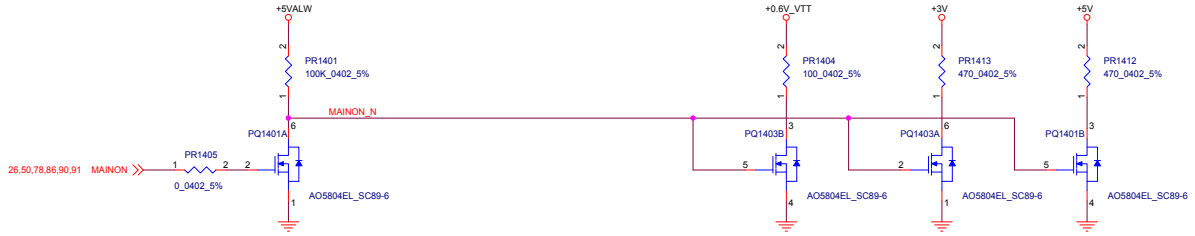

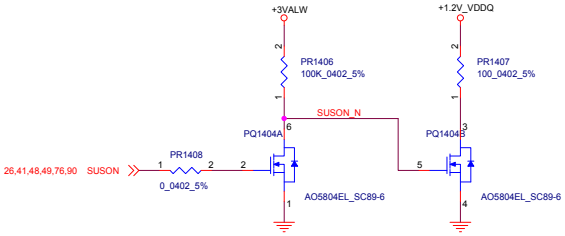

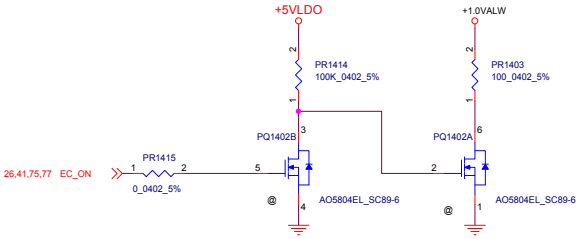

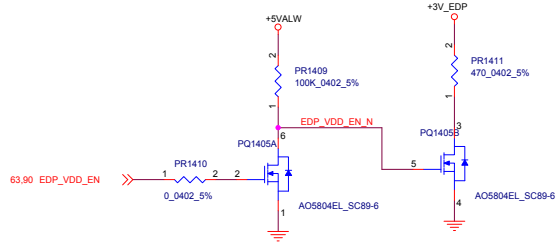

lenovo联想	LENOVO.CRDN	
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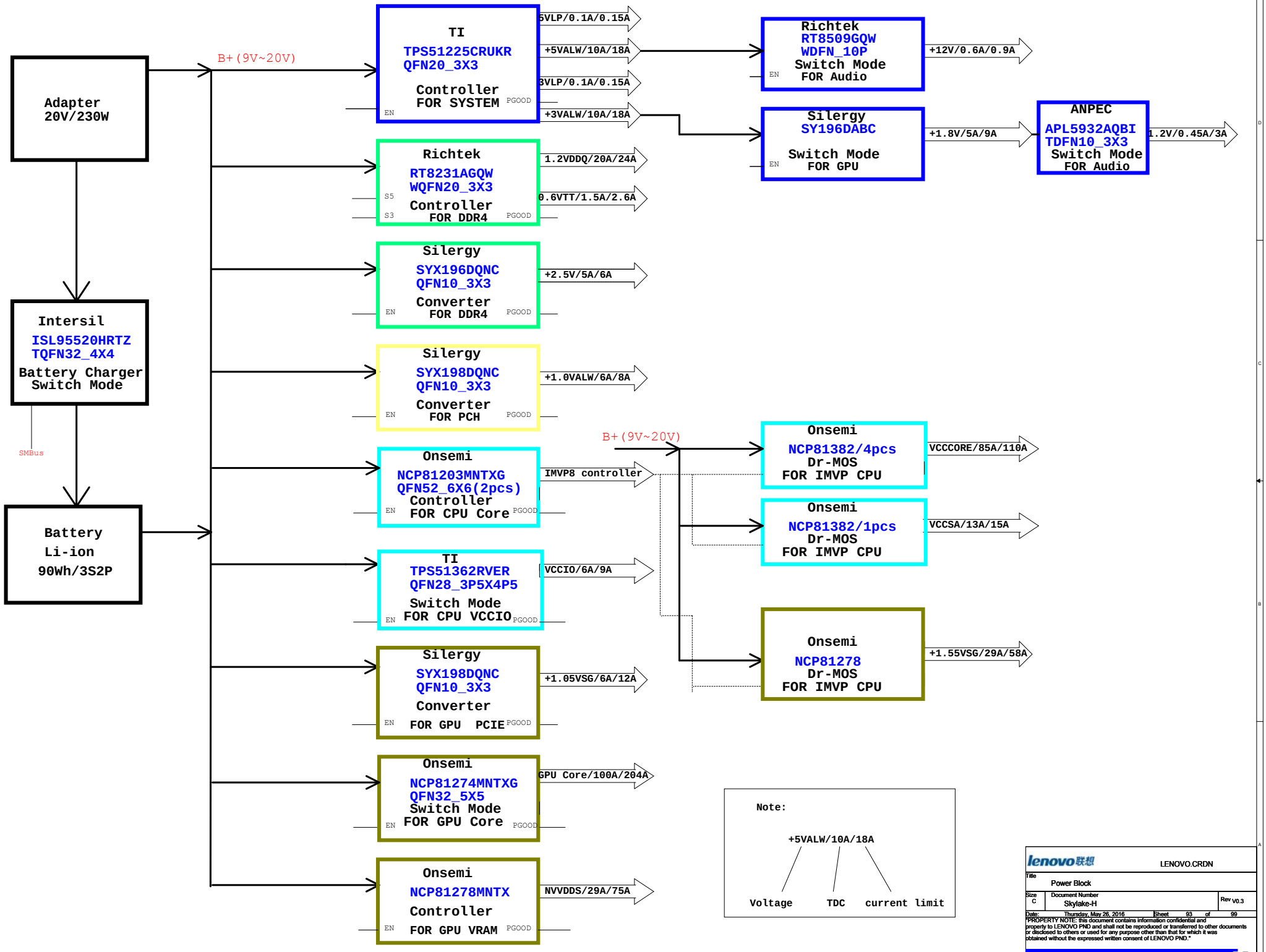

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Title: Power Block

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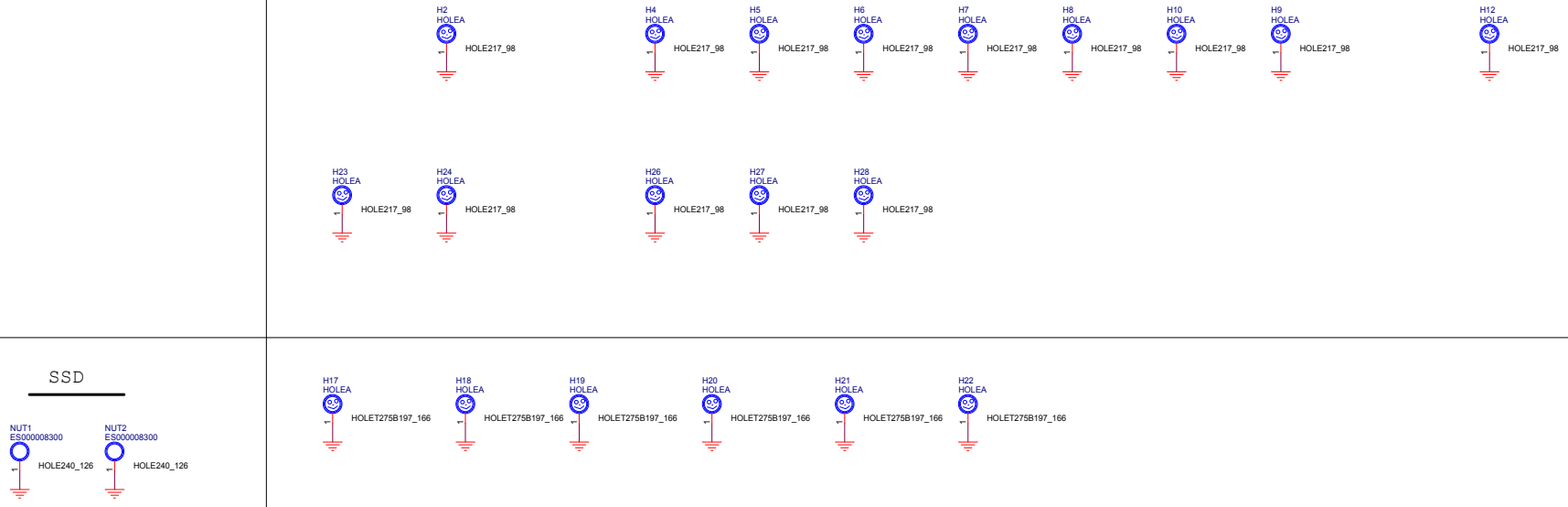
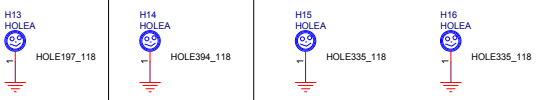
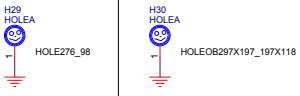


SSD

WLAN





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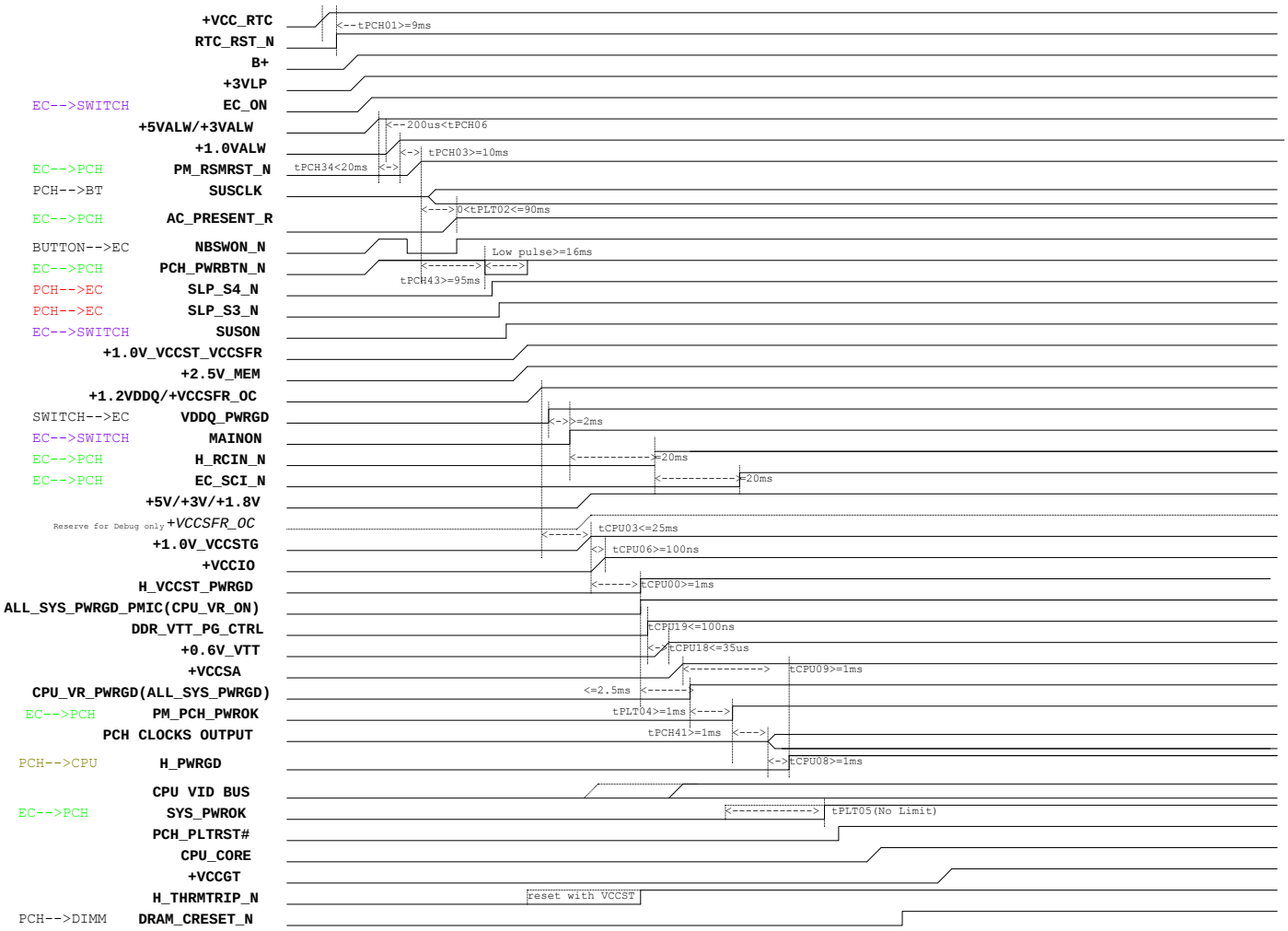
Power On Sequence

G3-->S5/S4-->S0(Non-Deep Sx platform)



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File: POWER ON SEQUENCE		
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Flexible I/O

HSIO PORTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
CONFIGER	USB3.0 PORT1		USB3.0 PORT3			USB3.0 PORT6	PCIE PORT1(1X4)					PCIE PORT6	PCIE PORT7	PCIE PORT8	PCIE PORT9(1X4)				PCIE PORT13(1X4)				SATA PORT6			
DEVICE	JUSB3(IO)		JUSB2			JUSB4(IO)	U2005(Intel AR DP）					Card Reader	WLAN	LAN	PCIE SSD2				PCIE SSD1				HDD			

SMBus Table

Master EC	Slave Device
EC_SMB_CLK0 EC_SMB_DAT0	*PU201* CHARGER 0x 0001 001x; *JBAT1* BATTERY 0x 16; *U2007* TPS65982 0x
EC_SMB_CLK1 EC_SMB_DAT1	*U2* PCH; *U25* Thermal Sensor 0x 1001 101x; *G2* dGPU 0x 9E; *JMXM1* MXM 0x 9C
EC_I2C_CLK3 EC_I2C_DATA3	*U19* LC; *PU1255* TPS22993 0x 1110 010x; *PU1256* TPS22993 0x 1110 000x; *PU1306* OZ7520 0x 2E; *U2019* PI3HDX1204BZHE 0XC2; *U2015* PI3DPX1203ZHE 0XF2
EC_I2C_CLK5 EC_I2C_DATA5	*U23* IR sensor 0x 1000 000x; *U24* IR sensor TMP006 0x 1000 001x; *U27* IR sensor 0x 1000 100x; *U5002(reserve)* RGB sensor CS5032 0x 1C; *U8 (reserve)* AMP TAS5766 0x 1001 100x

Master PCH	Slave Device
PCH_SMB_CLK PCH_SMB_DAT	*JDIMM1* SO-DIMM 0x 1010 000x; *JDIMM2* SO-DIMM 0x 1010 001x; *JDIMM3* SO-DIMM 0x 1010 010x; *JDIMM4* SO-DIMM 0x 1010 011x; *JTP1* Touch Pad 0x 2C; *PU402* uP1804A 0x 62; XDP
EC_SMB_CLK1 EC_SMB_DAT1	*U5* EC

I2C Table

Master PCH	Slave Device
PCH_I2C_CLK0 PCH_I2C_DATA0	*U8* AMP TAS5766 0x 1001 100x
PCH_I2C_CLK1 PCH_I2C_DATA1	*U19* LC
PCH_I2C_CLK1 PCH_I2C_DATA1	*U5* EC

USB2.0 Configuration		
USB2 #	Assignment	OCx #
USB2 1	JUSB3(IO DB)	USB_OC0_N
USB2 2	JUSB2	USB_OC1_N
USB2 3	HD camera	
USB2 4	KB	
USB2 5	BT	
USB2 6	JUSB4(IO DB)	USB_OC3_N
USB2 7	NC	
USB2 8	NC	
USB2 9	Finger print	
USB2 10	NC	
USB2 11	NC	
USB2 12	NC	
USB2 13	NC	
USB2 14	NC	

BOM Structure Table

BTO Item	BOM Structure
Unpop	@
CPU Option	H44e@, H42@
GPU Option	SLI@
Connector	ME@

BOARD ID Table

Flexible I/O Configuration				
I / O	High Speed Signals	Configuration	DEVICE	OCx #
Port 1	USB3 1 Capable of OTG	USB3.0	JUSB3(IO)	
Port 2	USB2 3 / SSIC 1	NC		
Port 3	USB3 3 / SSIC 2	USB3.0	JUSB2	USB_OC1_N
Port 4	USB3 4	NC		
Port 5	USB3 5	NC		
Port 6	USB3 6	USB3.0	JUSB4(IO)	

Flexible I/O Configuration				
I / O	High Speed Signals	Configuration	DEVICE	GEN
Port 7	USB3_7 / PCIE 1	AR (L0)	U2005 (Intel AR DP）	
Port 8	USB3_8 / PCIE 2	AR (L1)		
Port 9	USB3_9 / PCIE 3	AR (L2)		
Port 10	USB3_10 / PCIE 4	AR (L3)		
Port 11	PCIE 5	NC		
Port 12	PCIE 6	Card Reader	U3001	PCIE 1x Gen2
Port 13	PCIE 7	WLAN	JWLAN1	PCIE 1x Gen2
Port 14	PCIE 8	LAN	U6	PCIE1x Gen1

Flexible I/O Configuration				
I / O	High Speed Signals	Configuration	DEVICE	GEN
Port 15	SATA 0A / PCIE 9	M.2 SSD2 (L0) / SATA0	JSSD2	PCIE 4x Gen 3 /SATA Gen 3
Port 16	SATA 1A / PCIE 10	M.2 SSD2 (L1)		
Port 17	/ PCIE 11	M.2 SSD2 (L2)		
Port 18	/ PCIE 12	M.2 SSD2 (L3)		
Port 19	SATA 0B / PCIE 13	M.2 SSD12(L0)	JSSD1	PCIE 4 x Gen 3
Port 20	SATA 1B / PCIE 14	M.2 SSD1 (L1)		
Port 21	SATA 2 / PCIE 15	M.2 SSD1 (L2)		
Port 22	SATA 3 / PCIE 16	M.2 SSD1 (L3)		
Port 23	SATA 4 / PCIE 17	SATA HDD	U14	SATA Gen 3
Port 24	SATA 5 / PCIE 18	NC		
Port 25	SATA6 / PCIE 19	NC		
Port 26	SATA7 / PCIE 20	NC		

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