

COMPAL CONFIDENTIAL

MODEL NAME :
FDI40 N3-14", FDI4A V3-14", FDI43 N5-14",
FDI50 N3-15", FDI5A V3-15", FDI53 N5-15",
FDI70 N3-17"

PCB NO : DA8001K6000 (SBDR)
DA8001K6100 (NBDR)

BOM P/N :
SBDR-DIS NBDR-DIS X4E
431AJ431L51 431AJ431L01 X4E AJ431L51(N3)
431AJ431L52 431AJ431L02 X4E AJ431L52(V3)
431AJ431L53 X4E AJ431L01(N5)
431AJ431L54

CML-U+MEC1418

2019-06-20

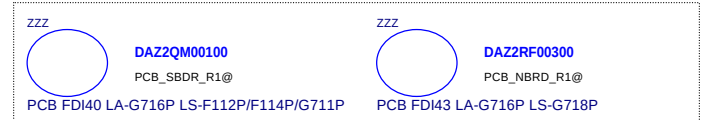
REV : 1.0 (A00)

@ : Un-pop Component
DIS@ : GPU Support
INSPIRON@/VOSTRO@ : Inspiron/Vostro
CML@/CNL@ : CML/CNL
BASE@/PREM@ : Pentium,Celeron / i3,i5,i7
EXO@/TOPAZ@ : R17M-M1-30/R17M-M2-50
EC@ : EC Support
JP@/PJP@ : JUMP
100@/1000@: Lan

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CMC@ : XDP Component
CONN@ : Connector Component
KBBL@ : KB Backlight
TPM@/FTPM@ : HW TPM/SW TPM
750_CTPM@:750 and china TPM
ST_CTPM@:ST and china TPM
CTPM@:China TPM
FFS@ : Free Fall Sensor
TYPEC@ : TypeC
TYPEC@EMI@/TYPEC@ESD@: EMI, ESD ,TypeC Component
M1_30@/M2_50@ : R17M-M1-30/R17M-M2-50
2G_G5@/2G_H@/2G_S@/2G_M@ : VRAM type
PCB@/PCB_R1@/PCB_R3_G@/PCB_R3_T@/PCB_R3_H@/PCB_R3_TM@: PCB MB

PCB_NBDR_R1@: PCB MB DAZ for NBDR
TS_NON@/TS_USB@/TS_I2C@: Touch Screen Interface Select
SBDR@/NBDR@: SBDR/ NBDR Select

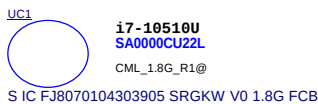
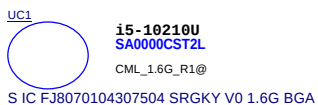
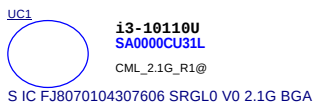
PCB R1



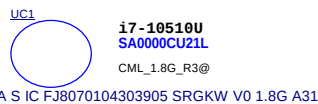
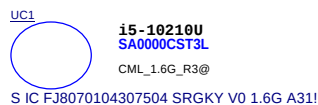
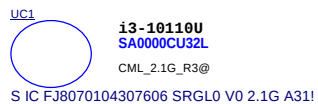
PCB R3



CPU R1



CPU R3



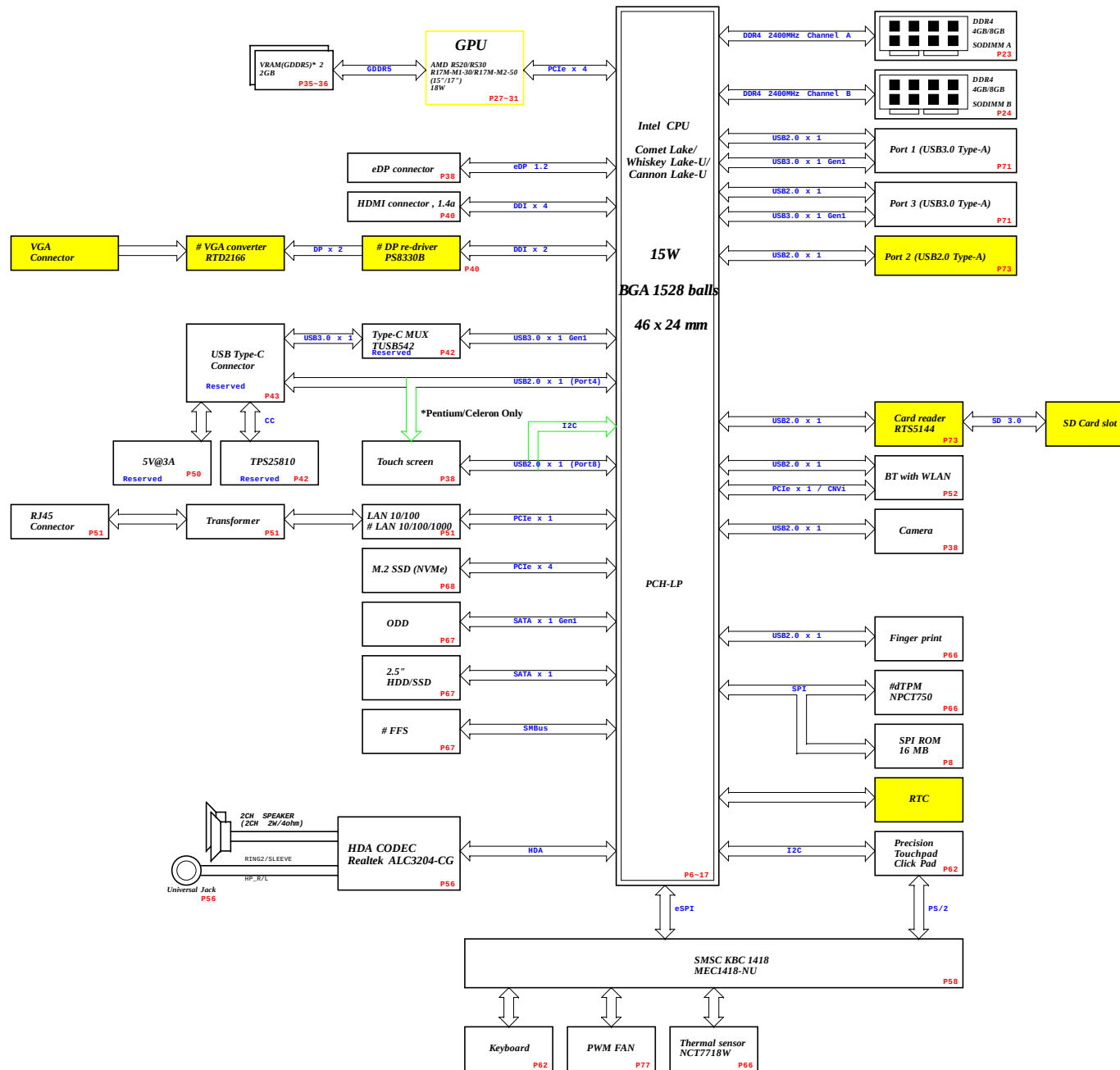
Layout Dell logo



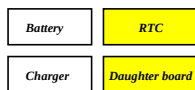
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PWB: 9HTP8

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				1.0	
				LA-G716P	
				Date:	Thursday, June 20, 2019
				Sheet	1 of 101

Block Diagram



----> V3 only



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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	---	---	---	---	---	---	---

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 Port2
3	USB2.0 Port, IO/B
4*	Touch screen
5	Finger printer
6	Camera
7	Card reader , IO/B
8*	Reserved
9	NA
10	BT

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_ADPIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for System	N/A	N/A	N/A
+RTC_CELL	RTC power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+5VALW	System +5V always on power rail	ON	ON	ON*
+3VALW	System +3V always on power rail	ON	ON	ON*
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON*
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF
+0.6V_DDR_VTT	DDR +0.6V power rail for DDR terminator	ON	OFF	OFF
+VCCST	+1.05 VCCST power rail	ON	ON	OFF
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF
+VCCIO	+1.05 VCCIO power rail	ON	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF
+1.35V_MEM GFX	+1.35V power rail for GPU	ON	OFF	OFF
+3VGS	+3V power rail for GPU	ON	OFF	OFF
+1.8VGS	+1.8V power rail for GPU	ON	OFF	OFF
+0.95VSDGPU	+0.95V power rail for GPU	ON	OFF	OFF

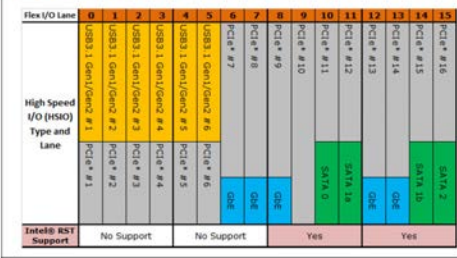
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Board ID & Model ID Table

#	Pull-down	Pull-up	Voltage	Board ID	Model ID
1	100	10.0	3.000	EVT	SBDR-UMA
2	100	17.8	2.801	DVT1	
3	100	27.0	2.598		NBDR-UMA
4	100	37.4	2.402	DVT2	
5	100	49.9	2.201		SBDR-DSC
6	100	64.9	2.001	Pilot	
7	100	82.5	1.808		NBDR-DSC
8	100	107.0	1.594		
9	100	154.0	1.299		
10	100	200.0	1.100		

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1	PCIE-1		USB3.0 port1
USB3.0-2	PCIE-2		NA
USB3.0-3	PCIE-3		USB3.0 port2
USB3.0-4	PCIE-4		TypeC
USB3.0-5	PCIE-5		GPU
USB3.0-6	PCIE-6		GPU
	PCIE-7		GPU
	PCIE-8		GPU
	PCIE-9		LOM
	PCIE-10		WLAN
	PCIE-11	SATA-0	SATA HDD
	PCIE-12	SATA-1A	SATA ODD
	PCIE-13		NVME SSD
	PCIE-14		NVME SSD
	PCIE-15	SATA-1B	NVME SSD
	PCIE-16	SATA-2	NVME SSD

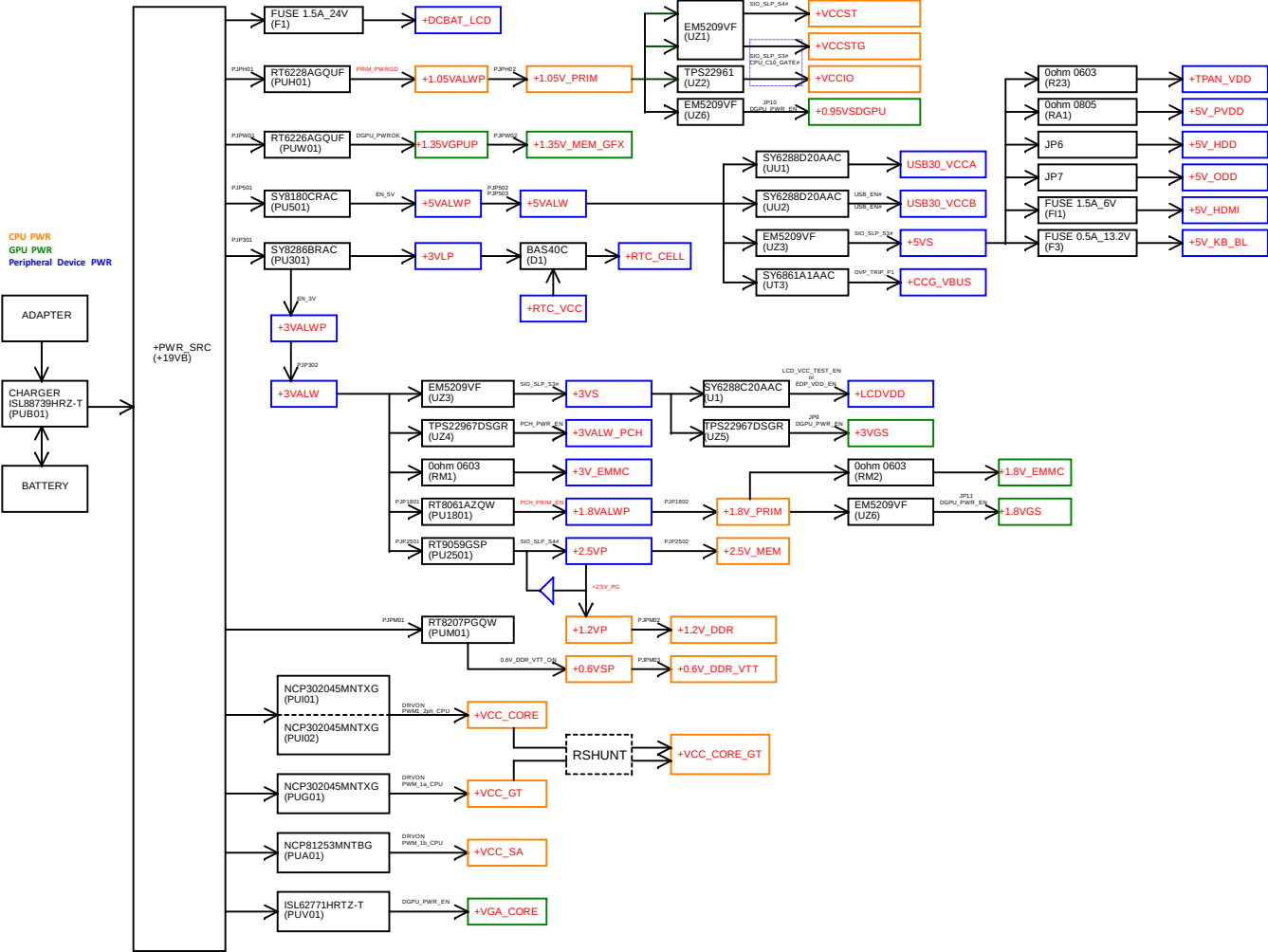
Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL PCH-LP



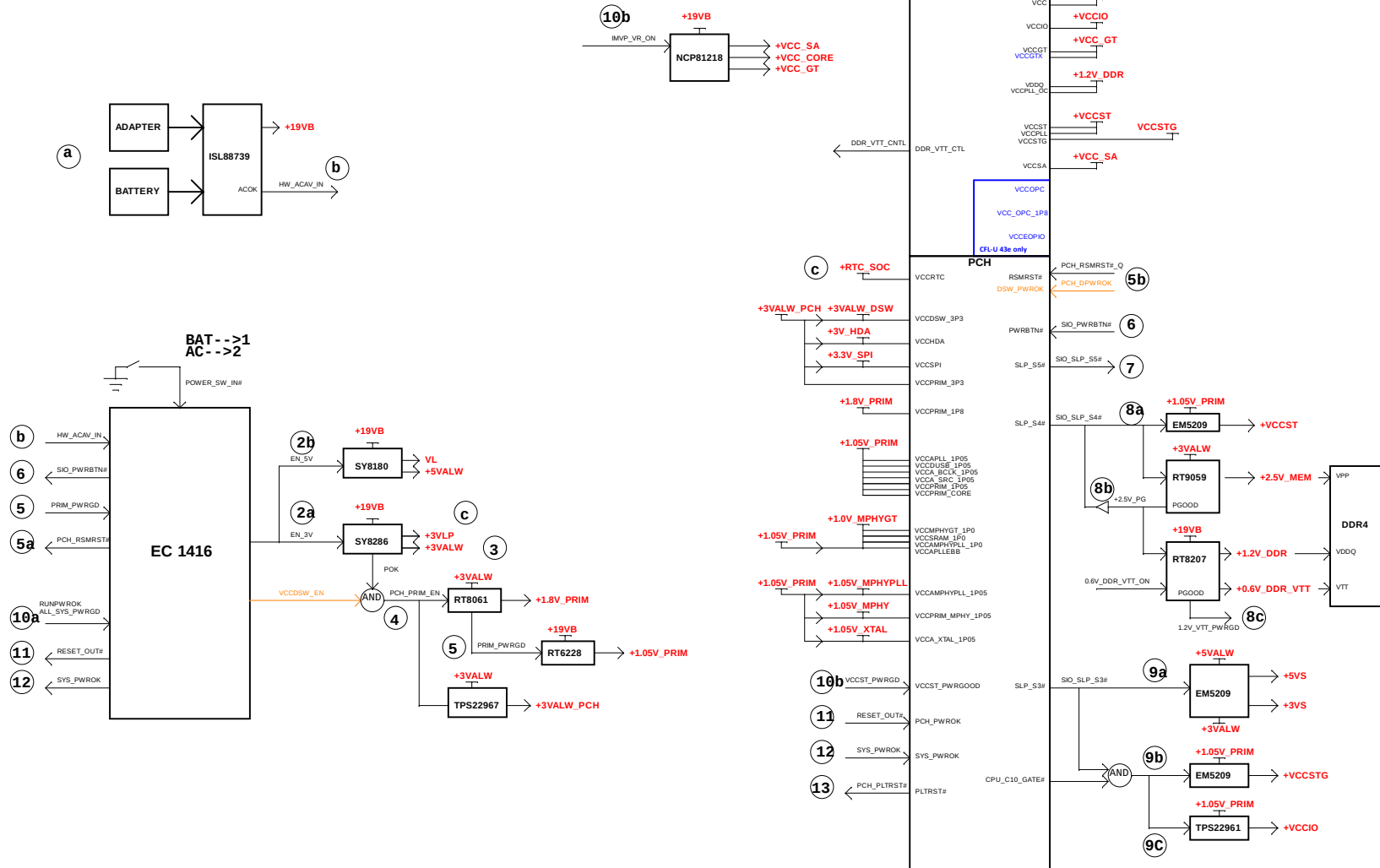
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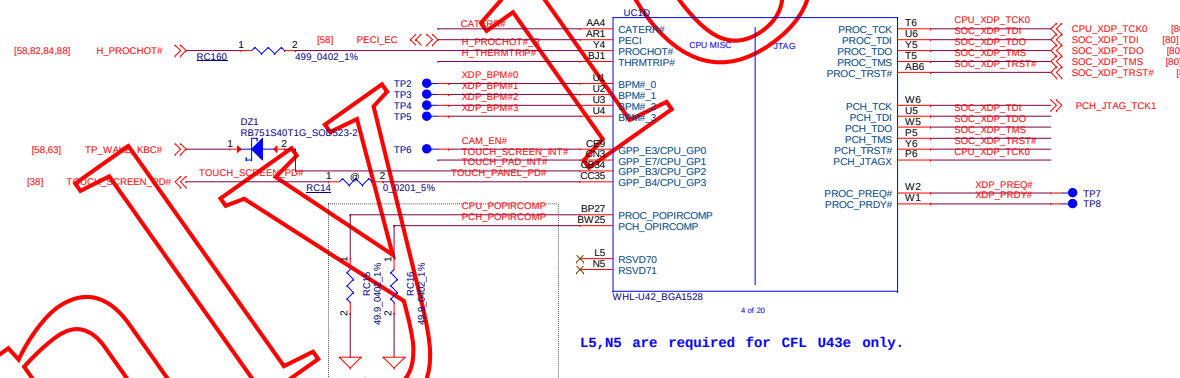
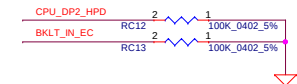
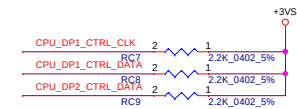
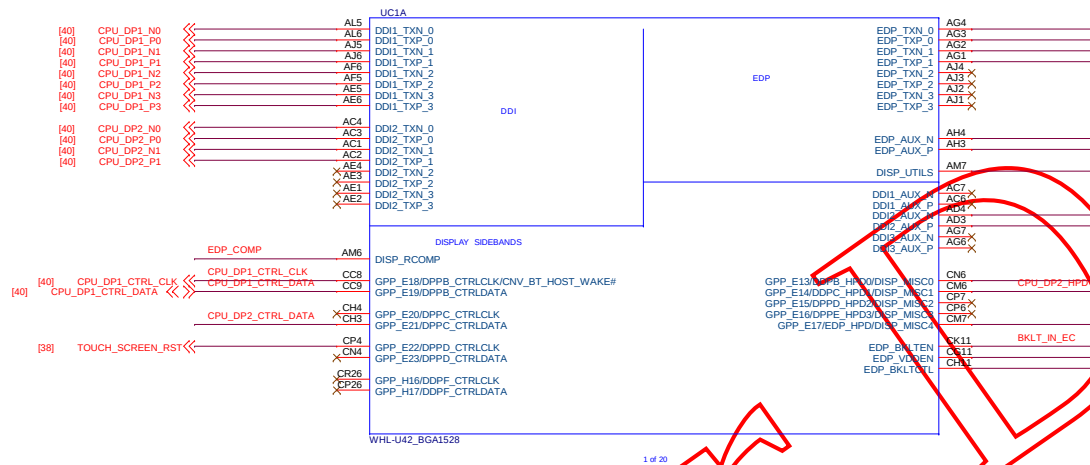
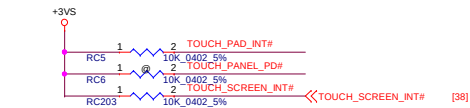
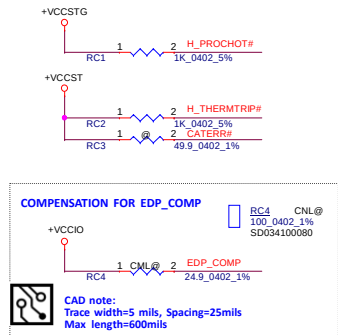
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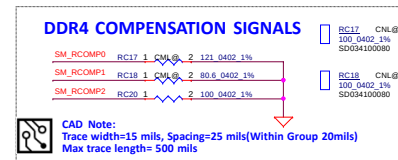
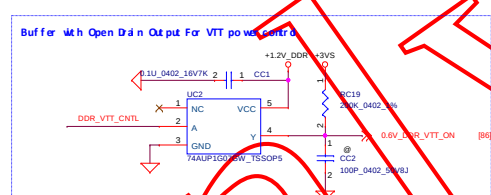
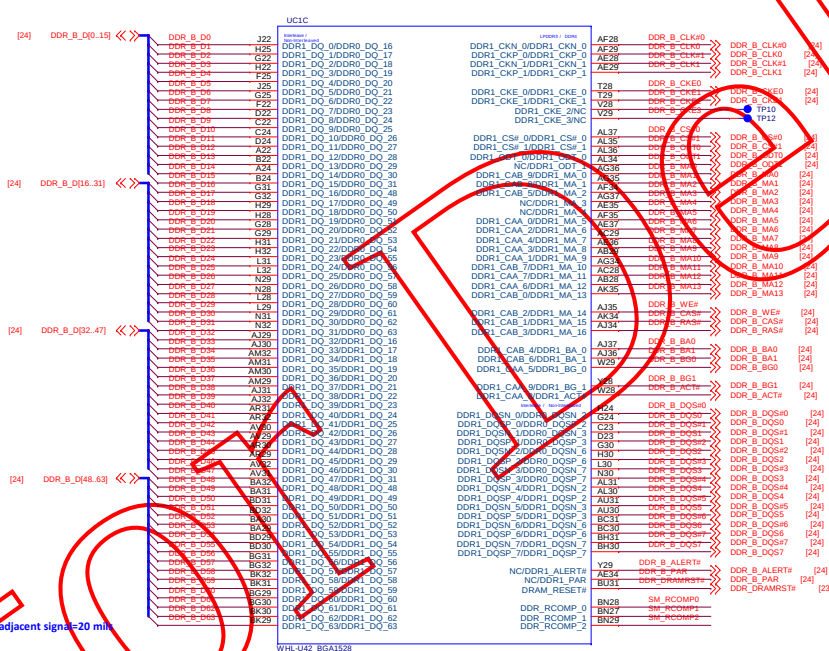
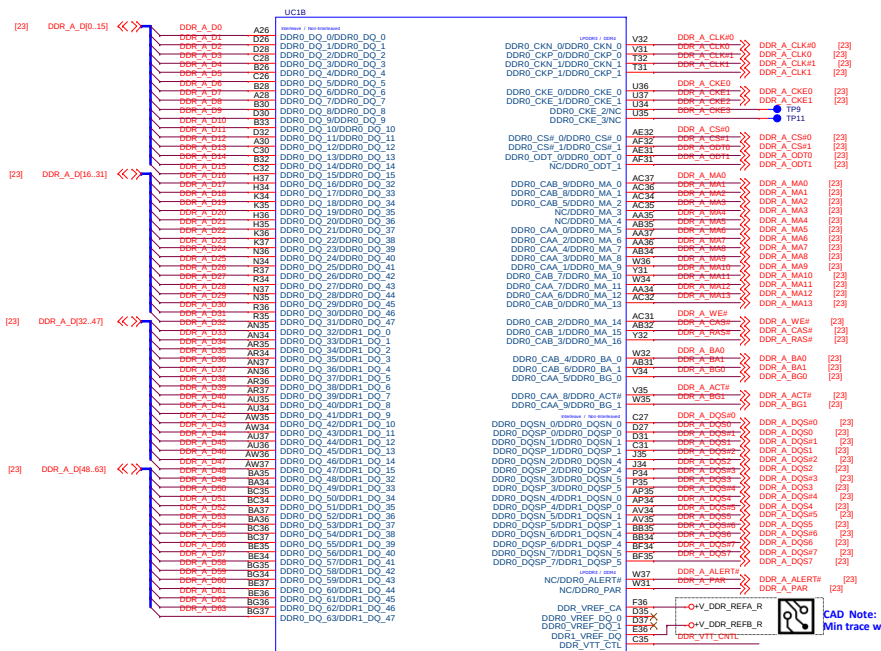
Timing Diagram for S5 to S0 mode



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DDR4 Interleaved Memory



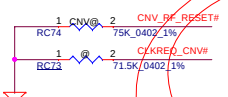
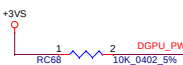
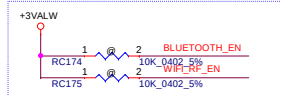
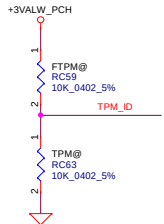
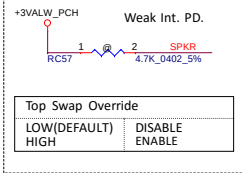
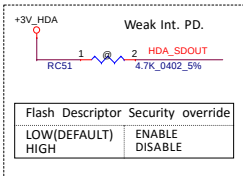
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RC21~RC25 place colse to Device



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				Size Custom	Document Number	Rev
					LA-G716P	1.0
Date: Thursday, June 20, 2019				Sheet	8	of 101

ME_FWP
LOW = ENABLE -->ME lock, can't update ME
HIGH = DISABLE -->ME un-lock, can update ME



COMPENSATION FOR CNV_WT_RCOMP

CAD Note:
Min trace width=10 mils, Spacing=15 mils
Max trace length=500 mils

CPU ID	BOARD_ID2 (GPP_C11)	BOARD_ID1 (GPP_C12)
CML-U	---	RC70
WHL-U(Reserved)	---	RC72
Pentium/Celeron	RC69	---
i3/i5/i7	RC71	---

COMPENSATION FOR SD_RCOMP

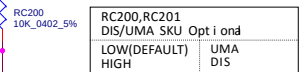
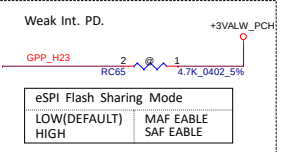
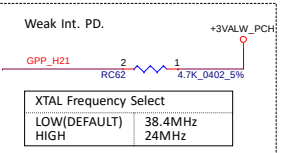
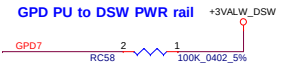
CAD Note:
Min trace width=10 mils, Spacing=12 mils
Max trace length=500 mils

COMPENSATION FOR SD_RCOMP

CAD Note:
Min trace width=10 mils, Spacing=12 mils
Max trace length=500 mils

COMPENSATION FOR EMMC_RCOMP

CAD Note:
Min trace width=10 mils, Spacing=12 mils
Max trace length=500 mils



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								LA-G716P		1.0			
								Date:		Thursday, June 20, 2019		Sheet 9 of 101	

Timing diagram for R7B0, R7B1, R7B2, R7B3, R7B4 close to Device. The diagram shows clock signals for GPU, WLAN, LAN, and SSD, and various clock outputs from the UC1J device. The signals are grouped into four main sections: GPU, WLAN, LAN, and SSD. Each section shows a clock signal (CLK_PEG_N, CLK_PCIE_N, CLK_PCIE_P1, CLK_PCIE_P2, CLK_PCIE_P4) and its corresponding output (CLKOUT_PCIE_N, CLKOUT_PCIE_P, CLKOUT_PCIE_P1, CLKOUT_PCIE_P2, CLKOUT_PCIE_P4). The signals are connected to the UC1J device via a bus (R7B0, R7B1, R7B2, R7B3, R7B4) and are labeled with their respective pin numbers (AW2, BC1, BC2, BC3, BH3, BH4, CE31, BA1, BA2, BE1, BE2, CF31). The diagram also shows the clock signals for the UC1J device (CLKOUT_PCIE_N, CLKOUT_PCIE_P, CLKOUT_PCIE_P1, CLKOUT_PCIE_P2, CLKOUT_PCIE_P4) and their corresponding outputs (CLKOUT_ITPXD_P_N, CLKOUT_ITPXD_P_P, CLKOUT_ITPXD_P_P1, CLKOUT_ITPXD_P_P2, CLKOUT_ITPXD_P_P4). The signals are connected to the UC1J device via a bus (R7B0, R7B1, R7B2, R7B3, R7B4) and are labeled with their respective pin numbers (AW2, BC1, BC2, BC3, BH3, BH4, CE31, BA1, BA2, BE1, BE2, CF31).

COMPENSATION FOR XCLK_BIASREF
CAD Note:
Min trace width=10 mils, Spacing=15 mils
Max trace length=1000 mils

UC4 change CPN & Description only
Jason 2019-04-26

PCH_PLTRST#

UC4

MC74VHC1G08BDF2G_SCT0

+3VS

IN1

IN2

100k 0.002 5%

PLTRST#

[27,51,52,58,66,68]

ESD0

07/4 ESD require

CC79 1 2 01U_0402_107K SYS_PWROK
①ESD②
07/4 ESD require

+3VALW_PCH

1 RC100

2 10K_0402_5% SYS_RESET#

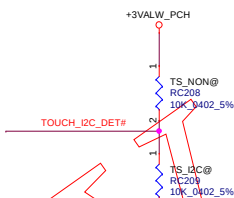
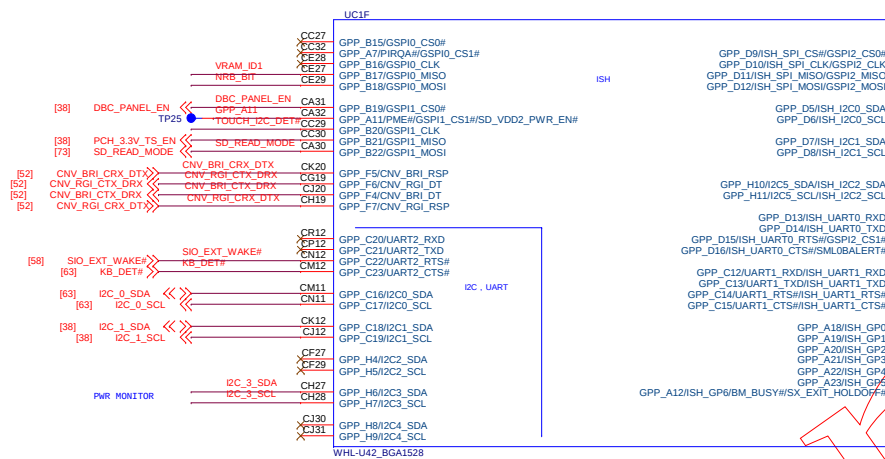
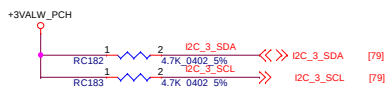
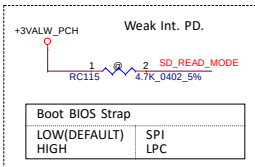
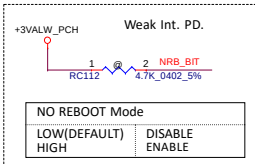
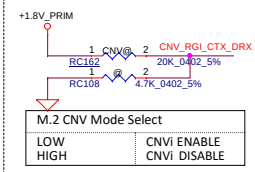
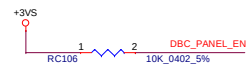
[illegible][illegible]

Timing diagram showing signals: PCH_BATLOW#, AC_PRESENT, RC96, RC97, RC98, and SIO_PWRBTN#.

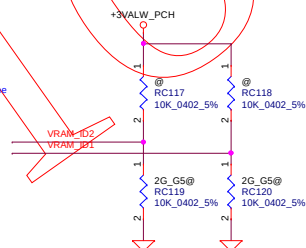
AC_PRESENT 2 1
RC68 2 1 10K 0402 5%
SIO_SLP_S3# 2 1
RC10 2 1 100K_0402_5%
SIO_SLP_S4# 2 1 100K_0402_5%
RC11 2 1 100K_0402_5%
WHL need PD
RC76 2 1 0.10_0402_10V7K
@ESD@
07/4 ESD require

3.0V Select	
LOW	0: 3.3V supply is 3.3V $\pm$ 5%
HIGH	1: 3.3V supply is 3.0V $\pm$ 5%

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				Size		Document Number	
				Custom		LA-G716P	
Date: Thursday, June 20, 2019				Sheet 10 of 101		Rev 1.0	



RC208,RC209	
Touch panel interface	
LOW	I2C
HIGH	USB

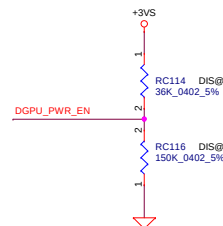


VRAM ID (PCBA VRAM Size Config.)	VBIOS_ID2 (GPP_CN23)	VBIOS_ID1 (GPP_CE27)
2G GDDR5	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

Timing diagram showing signals and their transitions over time. The signals are:

- DGPU_HOLD_RST#**: Transitions from high to low at RC107 and back to high at RC108. A 10K_0402_5% resistor is connected to the output.
- CAM_DET#**: Transitions from high to low at RC204 and back to high at RC109.
- FFS_INT2**: Transitions from high to low at RC204 and back to high at RC109.
- KB_DET#**: Transitions from high to low at RC110 and back to high at RC111.
- RTC_DET#**: Transitions from high to low at RC110 and back to high at RC111.
- SIO_EXT_WAKE#**: Transitions from high to low at RC113 and back to high at RC114.

Power supply rails are indicated as +3V and +3VALW.



[27] PEG_CRX_GTX_N[5..8] >> PEG_CRX_GTX_N[5..8]
[27] PEG_CRX_GTX_P[5..8] >> PEG_CRX_GTX_P[5..8]
[27] PEG_CTX_GRX_N[5..8] << PEG_CTX_GRX_N[5..8]
[27] PEG_CTX_GRX_P[5..8] << PEG_CTX_GRX_P[5..8]



COMPENSATION FOR PCIE_RCOMP

CAD Note:
Min trace width=10 mils
Max trace mismatch=5 mils



8 of 20

GPIO	DEVICE CONTROL
USB_OC0#	USB Port (MB)
USB_OC1#	USB Port (DB)
USB_OC2#	NA
USB_OC3#	USB Port (Type-C)
DEVSLP0	HDD
DEVSLP1	NA
DEVSLP2	M.2 SSD

PCIE1_RXN/USB31_1_RXN
PCIE1_RXP/USB31_1_RXP
PCIE1_TXN/USB31_1_TXN
PCIE1_TXP/USB31_1_TXP

PCIE2_RXN/USB31_2_RXN/SSIC_1_RXN
PCIE2_RXP/USB31_2_RXP/SSIC_1_RXP
PCIE2_TXN/USB31_2_TXN/SSIC_1_TXN
PCIE2_TXP/USB31_2_TXP/SSIC_1_TXP

PCIE3_RXN/USB31_3_RXN
PCIE3_RXP/USB31_3_RXP
PCIE3_TXN/USB31_3_TXN
PCIE3_TXP/USB31_3_TXP

PCIE4_RXN/USB31_4_RXN
PCIE4_RXP/USB31_4_RXP
PCIE4_TXN/USB31_4_TXN
PCIE4_TXP/USB31_4_TXP

USB2_1N
USB2_1P
USB2_2N
USB2_2P

USB2_3N
USB2_3P
USB2_4N
USB2_4P

USB2_5N
USB2_5P
USB2_6N
USB2_6P

USB2_7N
USB2_7P
USB2_8N
USB2_8P

USB2_9N
USB2_9P
USB2_10N
USB2_10P

USB2_COMP
USB2_ID
USB2_VBUSSENSE

GPP_E9/USB2_OC0#/GP_BSSB_CLK
GPP_E10/USB2_OC1#/GP_BSSB_DI
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#

GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2

GPP_E0/SATA/PCIE0/SATAGP0
GPP_E1/SATA/PCIE1/SATAGP1
GPP_E2/SATA/PCIE2/SATAGP2

GPP_E8/SATALED#/SP1_CS1#
RSVD_69

CB5
CB6
CA4
CA3

BY8
BY9
CA2
CA1

BY7
BY6
BY4
BY3

BW6
BW5
BW2
BW1

CE3
CE4
CE1
CE2

CG3
CG4
CD3
CD4

CG5
CG6
CC1
CC2

CG8
CG9
CB8
CB9

CH5
CH6
CC3
CC4

CC5
CE8
CC6

CK6
CK5
CK8
CK9

CP8
CR8
CM8

CN8
CM1
CP10

CN7
AR3

USB3_CRX_DTX_N1 [71]
USB3_CRX_DTX_P1 [71]
USB3_CTX_DRX_N1 [71]
USB3_CTX_DRX_P1 [71]

USB3_CRX_DTX_N2 [71]
USB3_CRX_DTX_P2 [71]
USB3_CTX_DRX_N2 [71]
USB3_CTX_DRX_P2 [71]

USB3_CRX_MTX_N4 [42]
USB3_CRX_MTX_P4 [42]
USB3_CTX_MRX_N4 [42]
USB3_CTX_MRX_P4 [42]

USB20_N1 [71]
USB20_P1 [71]
USB20_N2 [71]
USB20_P2 [71]

USB20_N3 [73]
USB20_P3 [73]
USB20_N4 [43]
USB20_P4 [43]

USB20_N5 [66]
USB20_P5 [66]
USB20_N6 [38]
USB20_P6 [38]

USB20_N7 [73]
USB20_P7 [73]
USB20_N8 [43]
USB20_P8 [43]

USB20_N10 [52]
USB20_P10 [52]

USB2_COMP
USB2_ID
USB2_VBUSSENSE

USB_OC0# [71]
USB_OC1# [73]
USB_OC2# [50]
USB_OC3# [50]

HDD_DEVSLP [67]
SSD_DEVSLP [68]

SATA_ODD_PRST# [67]
M2_SSD_PEDET [68]

SATA_LED# [63,68]

RSVD_69

USB3.0 (MB)

USB3.0 (MB)

TYPE C

USB2.0 (MB)

USB2.0 (M/B)

USB2.0 (IO/B)

Touch Screen

Finger Printer

CCD

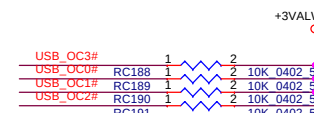
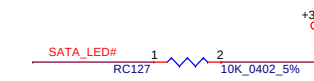
Card Reader (IO/B)

(Reserved)

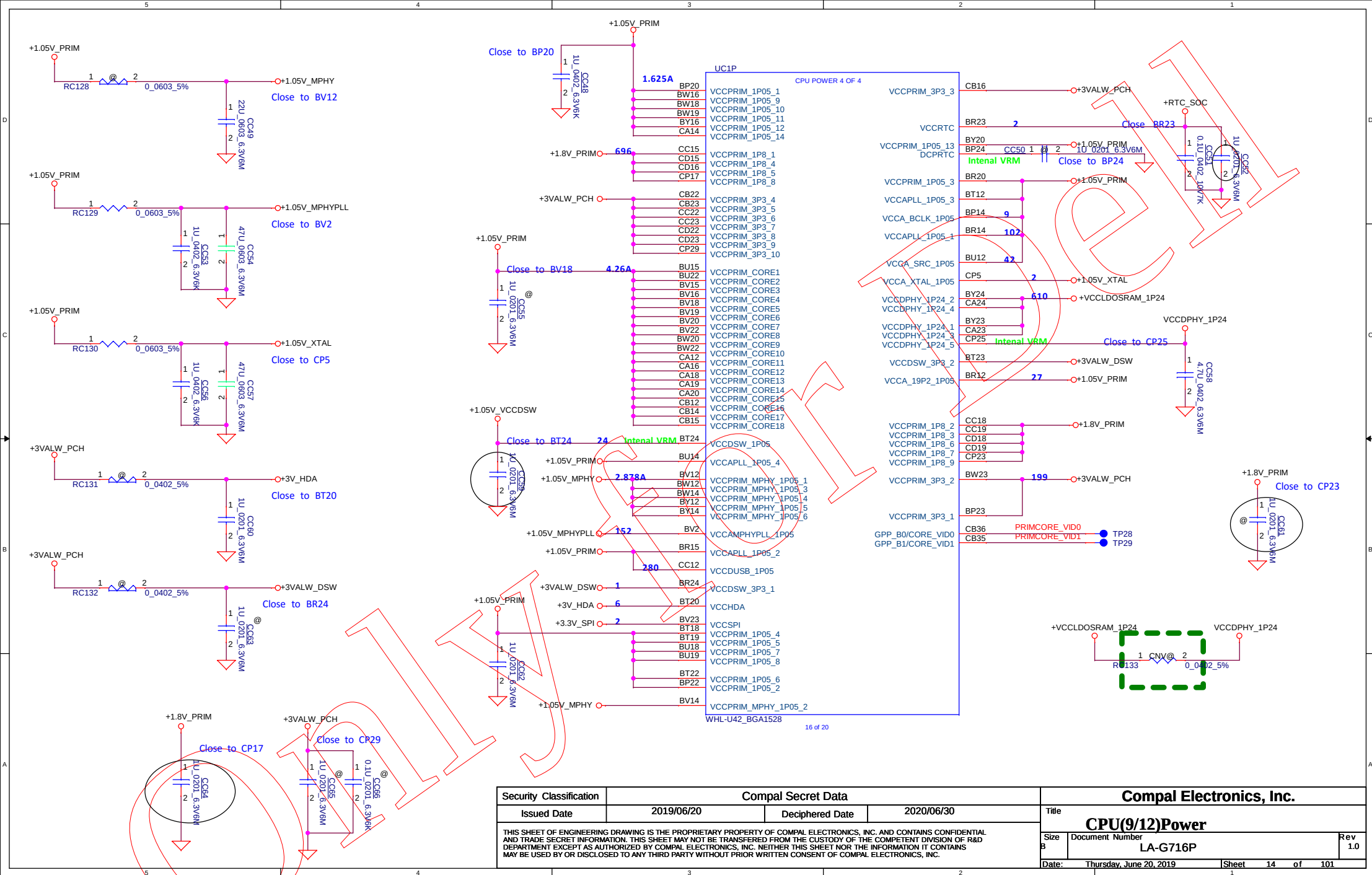
BT

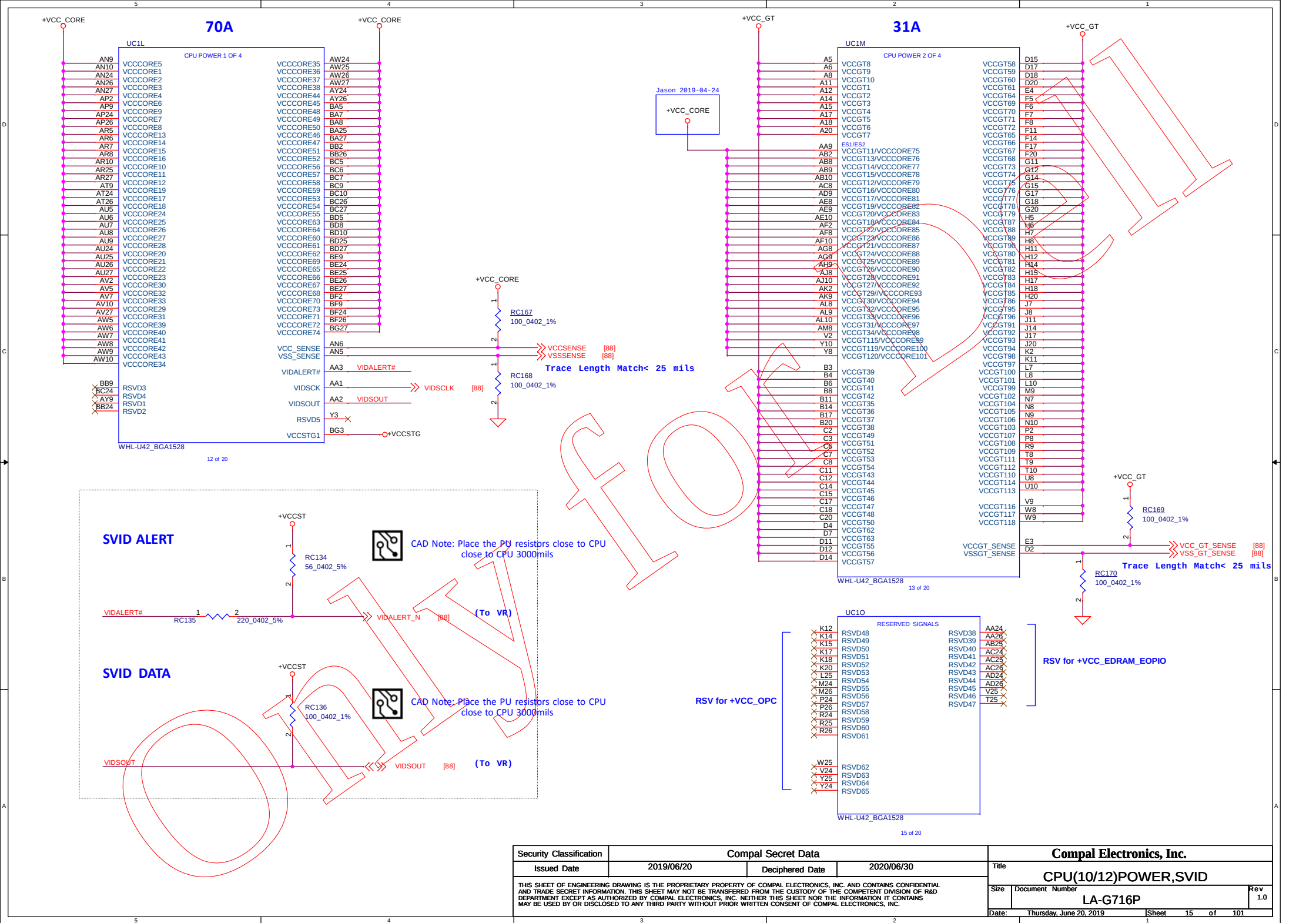
COMPENSATION FOR USB2_COMP

CAD Note:
Min trace width=50 Ohm, Spacing=15 mils
Max trace length=500 mils

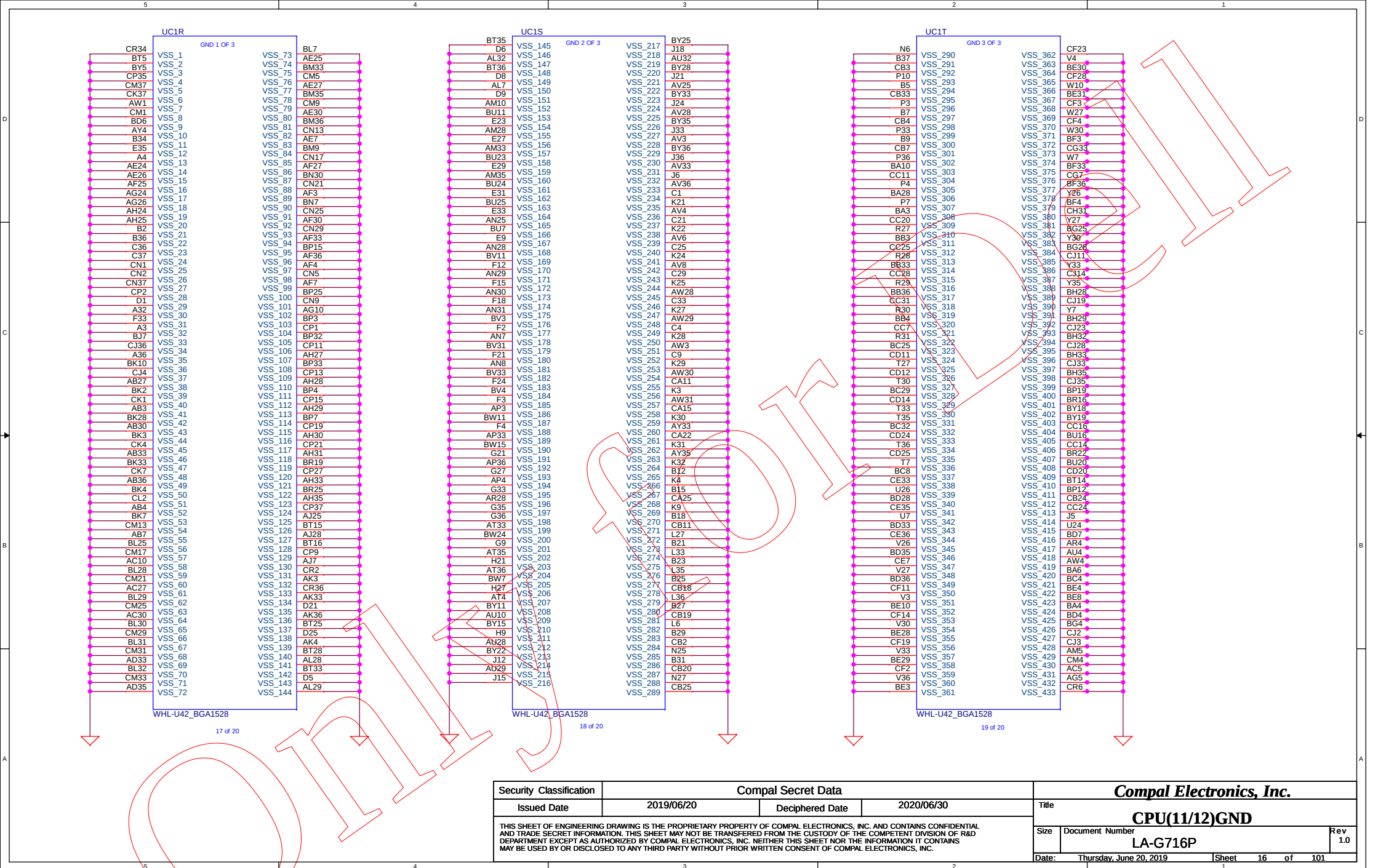


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						Size		Document Number		Rev	
						Custom		LA-G716P		1.0	
						Date:		Thursday, June 20, 2019		Sheet 12 of 101	



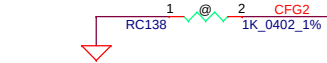


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								Size		Document Number		Rev	
										LA-G716P		1.0	
								Date:		Thursday, June 20, 2019		Sheet 15 of 101	
3				2									

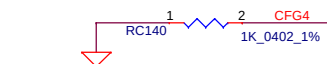




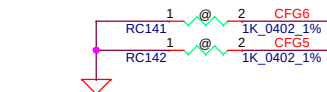
Reset sequence after PCU PLL is locked	
CFG0	1 : (DEFAULT) Normal Operation No Stall 0 : Stall



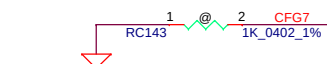
PCI Express Static Lane Reversal For All PEG Ports	
CFG2	1 : (DEFAULT) Normal Operation 0 : Lane Reversal



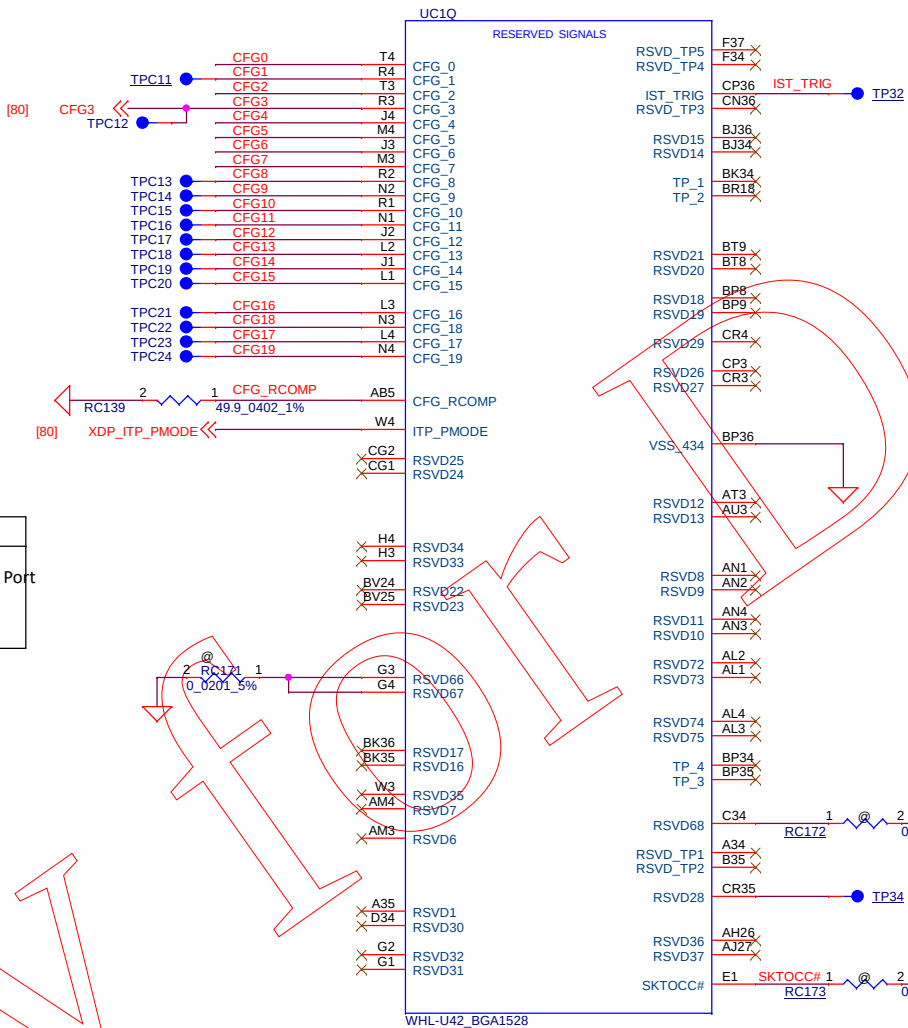
Display Port Presence Strap	
CFG4	0 : Enabled; An external Display Port device is connected to the Embedded Display Port 1 : Disabled; No Physical Display Port attached to Embedded Display Port



PCI Express Bifurcation	
CFG[6:5]	00 = 1x8 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*



PEG Training	
CFG7	1 : (default) PEG Train immediately following RESET# de-assertion 0 : PEG Wait for BIOS for training.



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				Sheet	17 of 101
				Rev	1.0

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				Date: Thursday, June 20, 2019	Sheet 18 of 101

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				Date:	Thursday, June 20, 2019
				Sheet	19 of 101

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				Date:	Thursday, June 20, 2019	Sheet 20 of 101

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Date: Thursday, June 20, 2019				Sheet	21	of 101

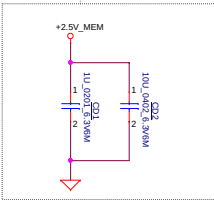
Main Function:

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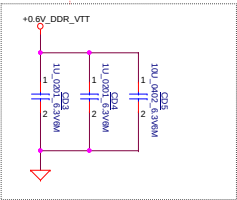
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					LA-G716P	1.0
				Date:	Thursday, June 20, 2019	Sheet 22 of 101

Main Func = DDR

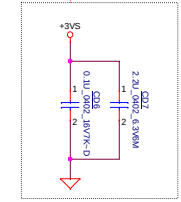
Layout Note:
Place near JDIMM1.257,259



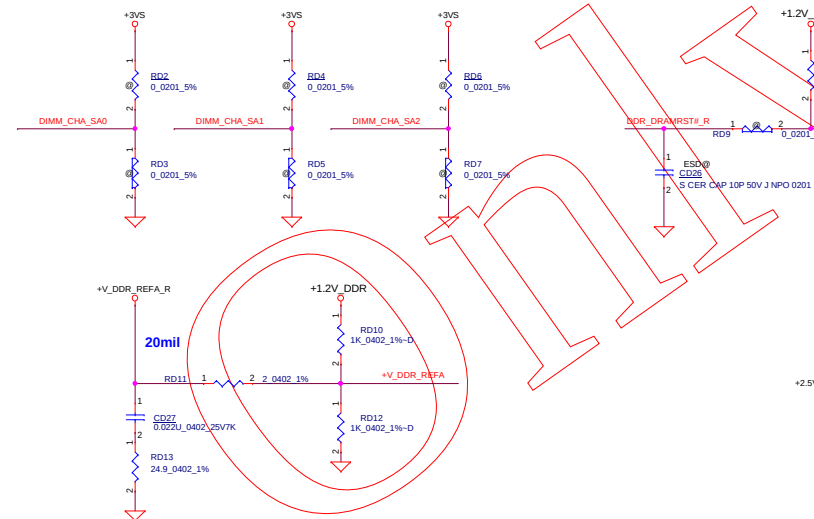
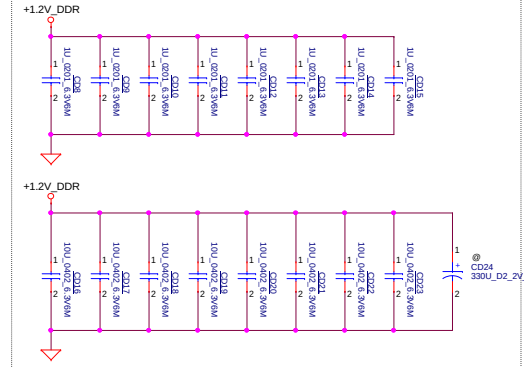
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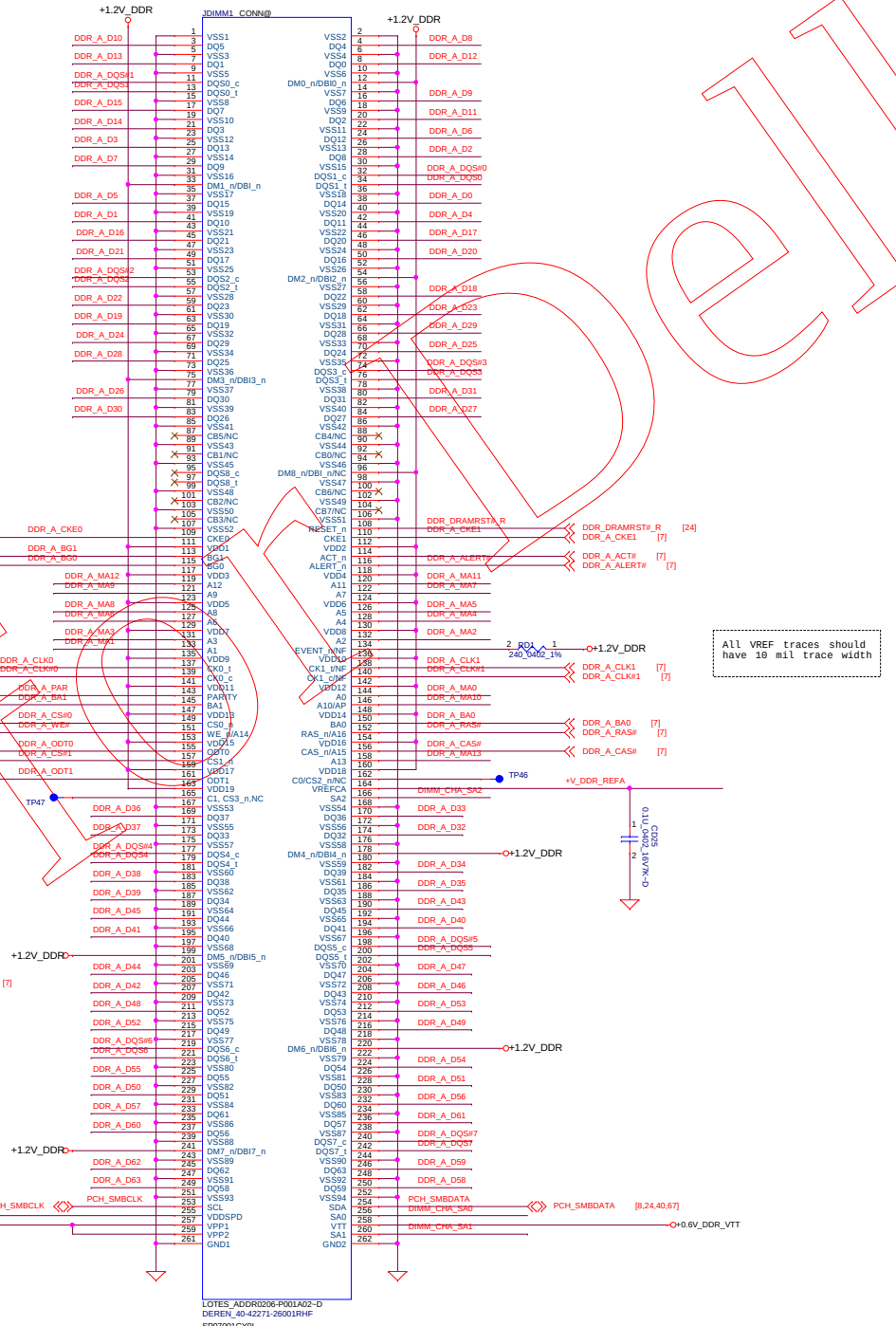
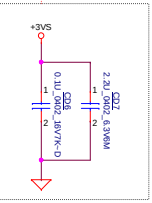
Layout Note:
Place near JDIMM1.255



Layout Note:
Place near JDIMM1



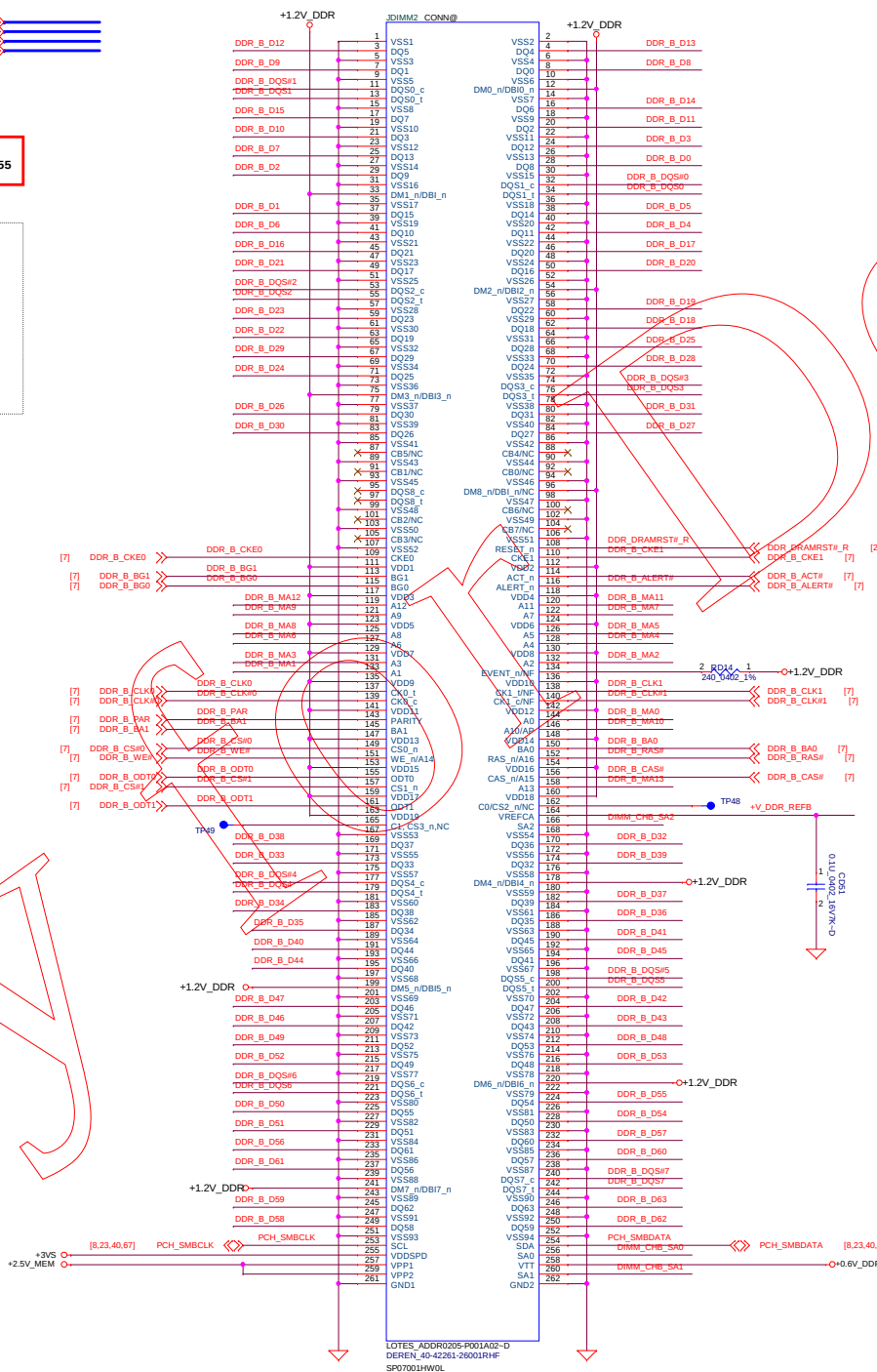
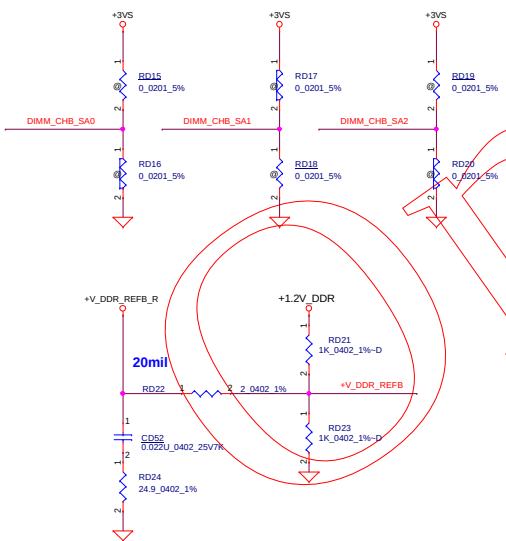
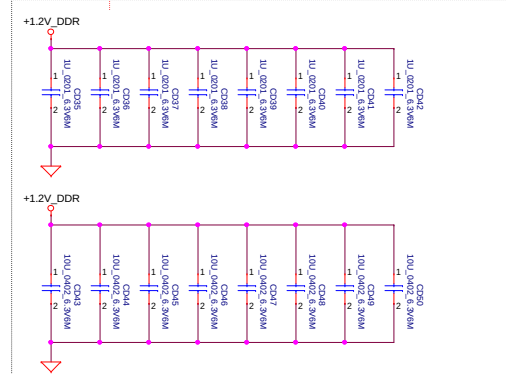
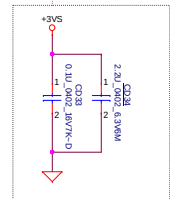
Layout Note:
Place near JDIMM1.255



All VREF traces should
have 10 mil trace width

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				LA-6716P	Rev 1.0
				Date	Thursday, June 20, 2019
				Sheet	23 of 101

Layout Note:
Place near JDIMM2.255



All VREF traces should have 10 mil trace width

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			LA-G716P	
Date	Thursday, June 20, 2019	Sheet	24	of 101

Main Function:

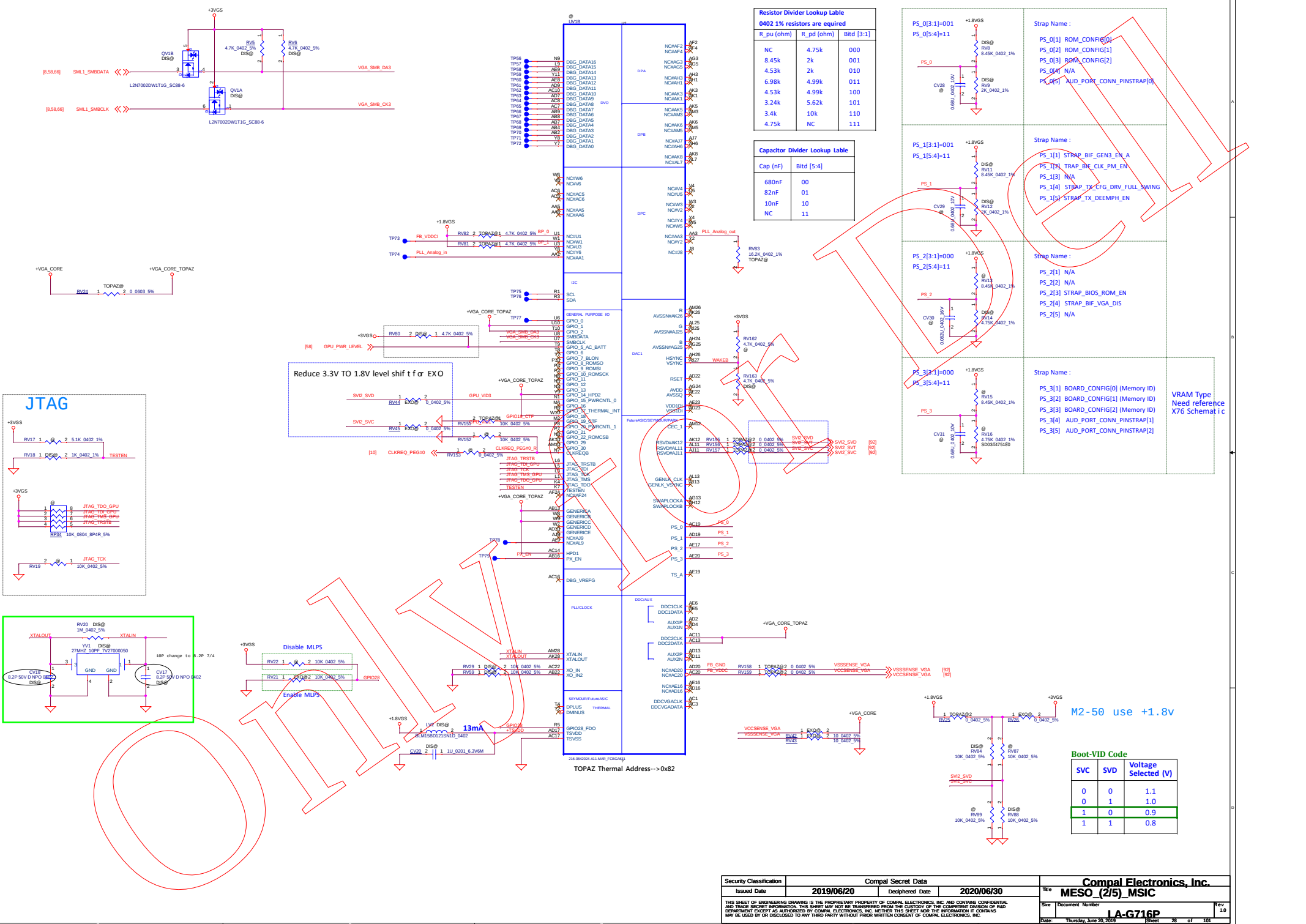
Reserve

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				LA-G716P		1.0

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				Date:	Thursday, June 20, 2019	Sheet 26 of 101



Resistor Divider Lookup Table
0402 1% resistors are equired

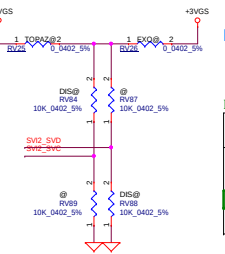
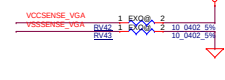
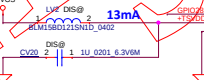
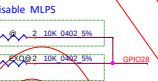
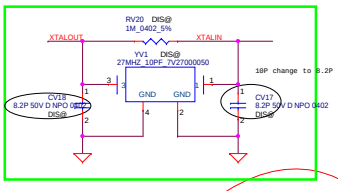
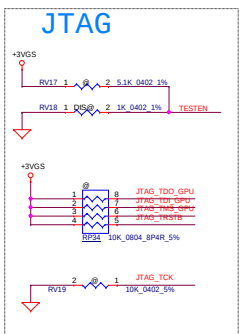
R_u (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

Capacitor Divider Lookup Table

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

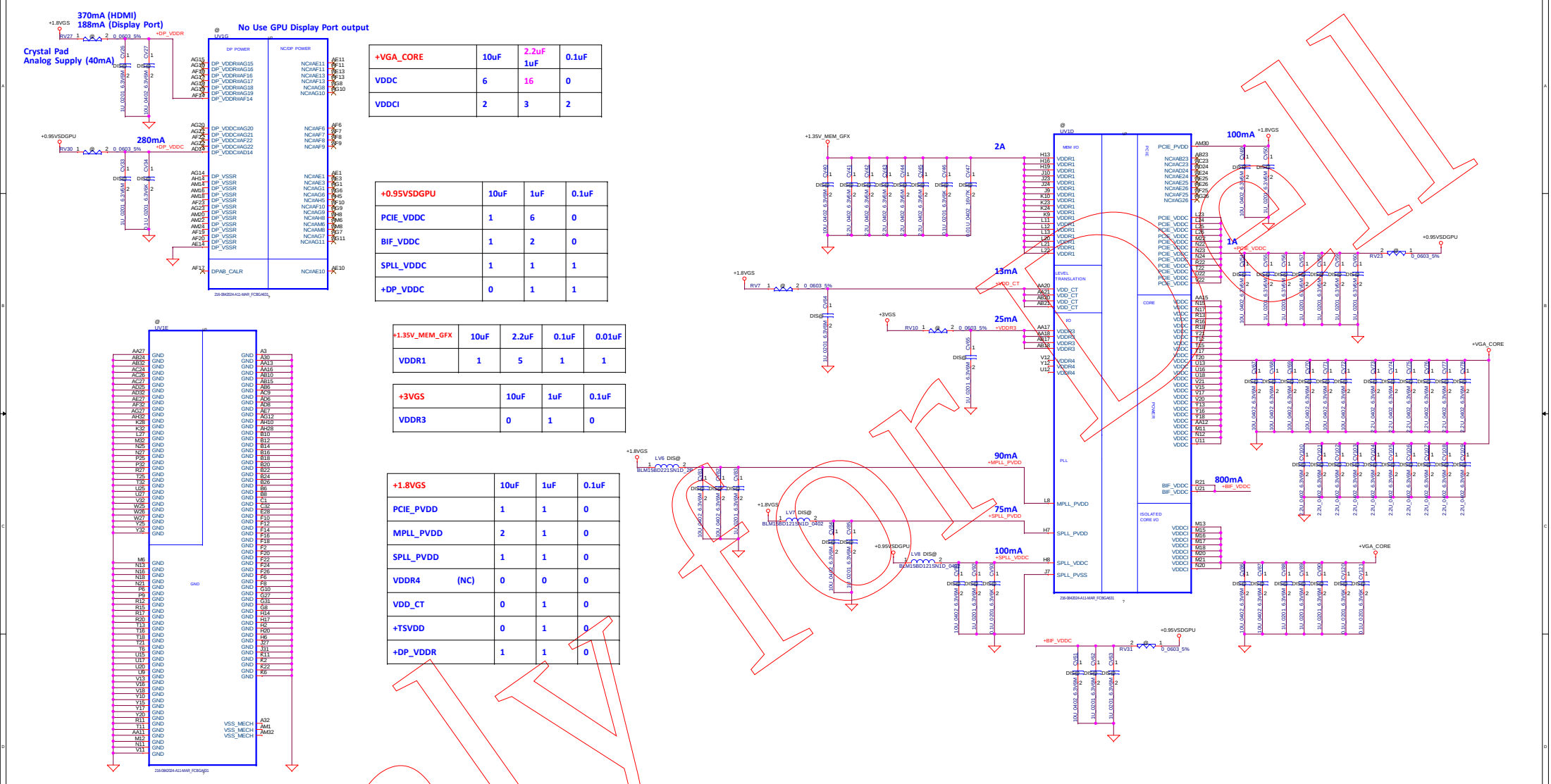
	Strap Name : PS_0[1] ROM_CONFIG[0] PS_0[2] ROM_CONFIG[1] PS_0[3] ROM_CONFIG[2] PS_0[4] N/A PS_0[5] AUD_PORT_CONN_PINSTRAP[0]
	Strap Name : PS_1[1] STRAP_BIF_GEN3_EN_A PS_1[2] STRAP_BIF_CLK_PM_EN PS_1[3] N/A PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING PS_1[5] STRAP_TX_DEEMPH_EN
	Strap Name : PS_2[1] N/A PS_2[2] N/A PS_2[3] STRAP_BIOS_ROM_EN PS_2[4] STRAP_BIF_VGA_DIS PS_2[5] N/A
	Strap Name : PS_3[1] BOARD_CONFIG[0] (Memory ID) PS_3[2] BOARD_CONFIG[1] (Memory ID) PS_3[3] BOARD_CONFIG[2] (Memory ID) PS_3[4] AUD_PORT_CONN_PINSTRAP[1] PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

VRAM Type
Need reference
X76 Schematic

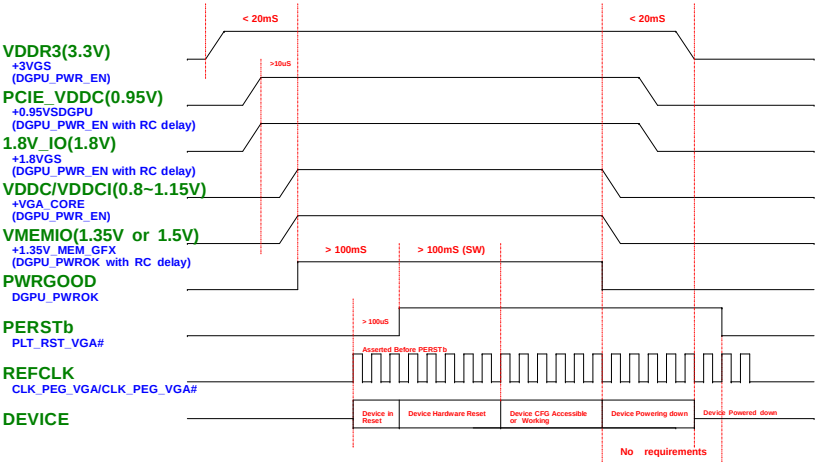


Boot-VID Code

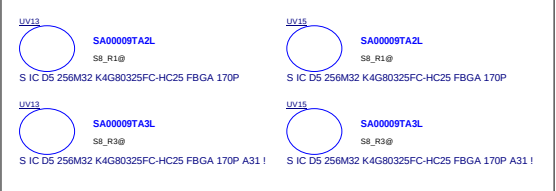
SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



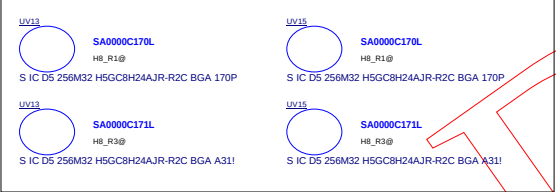
- Power-Up/Down Sequence**
1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.
 2. It is recommended that the 3.3-V rail ramp up first.
 3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
 4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ? 50 mV/ μ s).
 5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
 6. For power down, reversing the ramp-up sequence is recommended.



Samsung 2G



Hynix 2G



Micron 2G

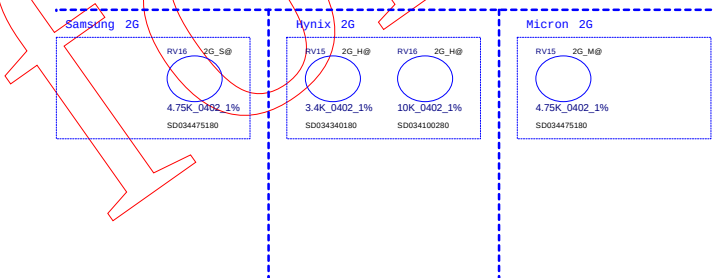
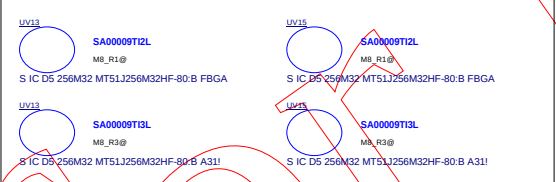


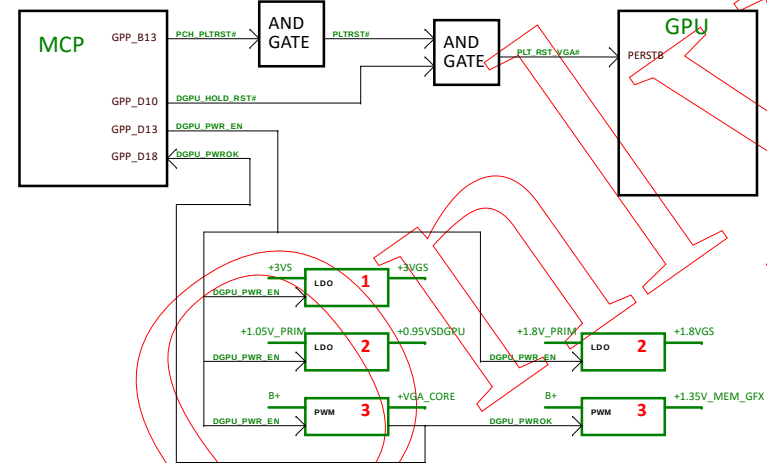
Table 3–21 Resistor Divider Lookup T.

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

For AMD R17M-M1-30 VRAM

Memory ID	8Gb R3 P/N	Vendor	Configuration	Size
000	SA00009TA3L	SAMSUNG	S IC D5 256M32 K4G80325FC-HC25 FBGA 170P A31 !	2GB
110	SA0000C171L	Hynix	S IC D5 256M32 H5GC8H24AJR-R2C BGA A31!	2GB
111	SA00009T13L	Micron	S IC D5 256M32 MT51J256M32HF-80:B A31!	2GB



Main Function:

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					LA-G716P	1.0
				Date:	Thursday, June 20, 2019	Sheet 32 of 101

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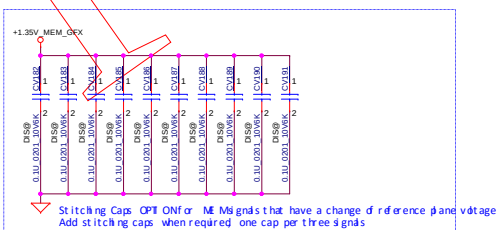
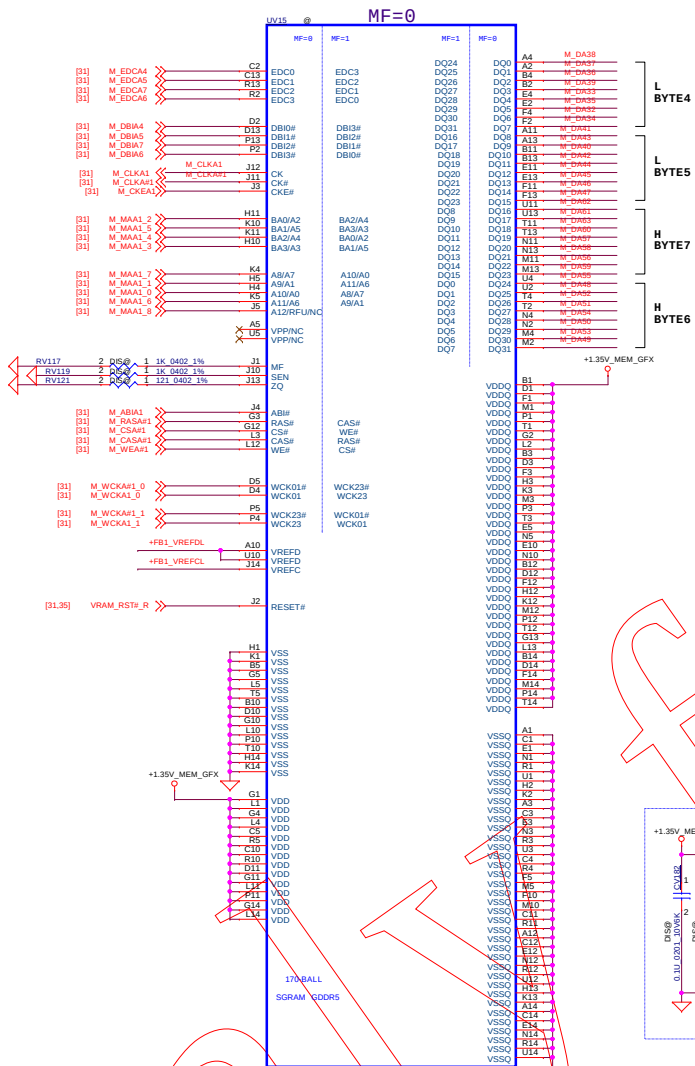
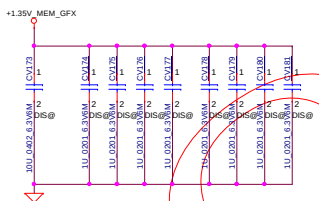
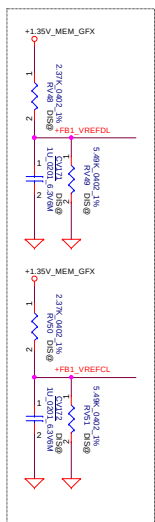
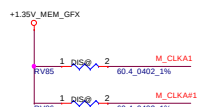
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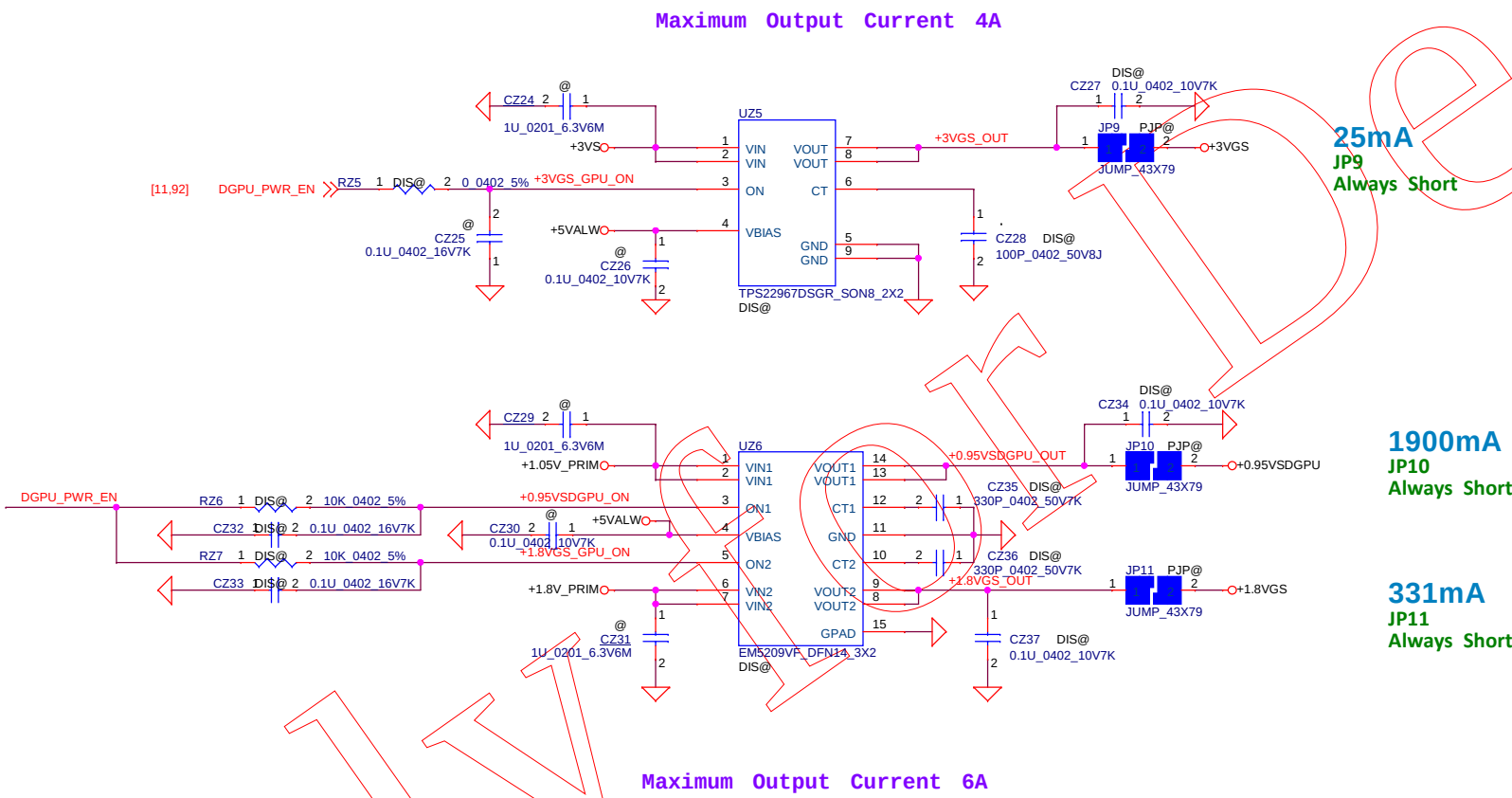
Main Func = GDDR5



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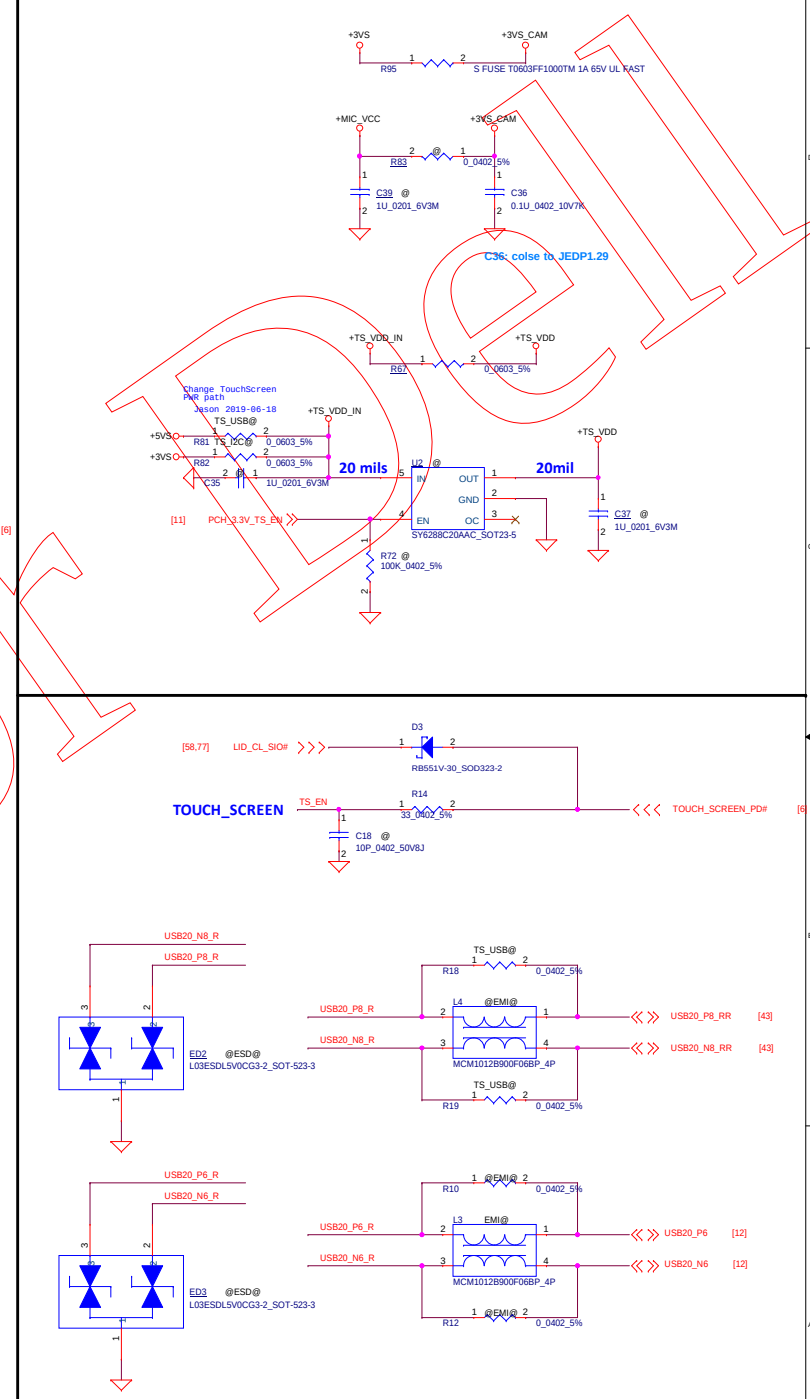
Main Func = GPU

+3V/+0.95V/+1.8V for GPU



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				LA-G716P	
Date:		Thursday, June 20, 2019		Sheet	37 of 101
				Rev	1.0

Main Func = CAM&MIC, TS



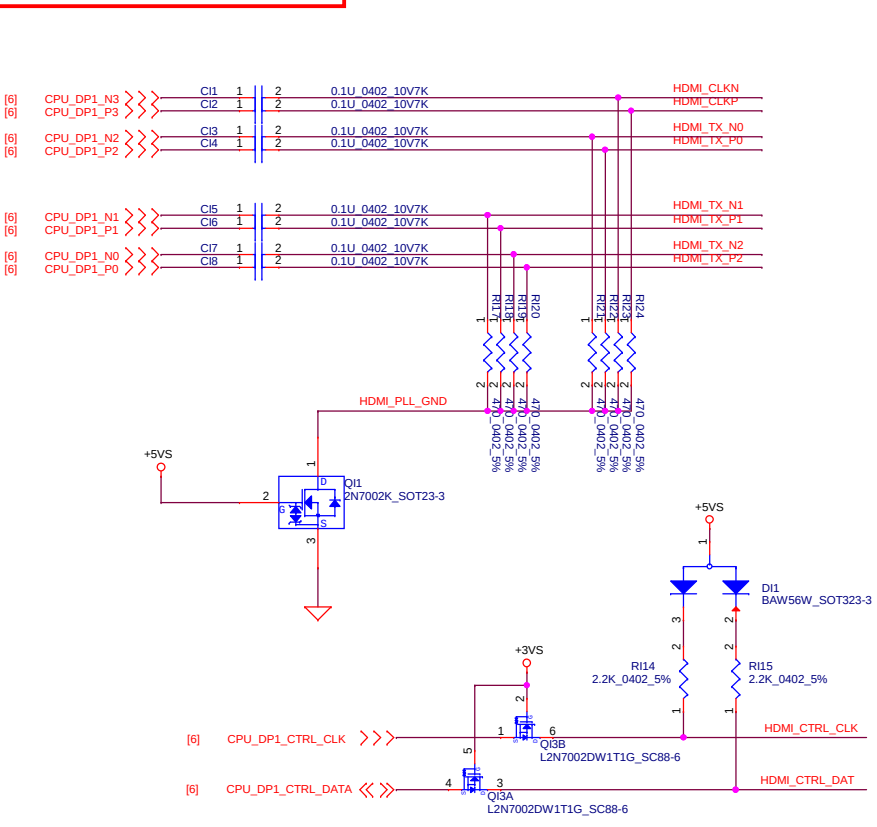
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Date:				Thursday, June 20, 2019	Sheet 38 of 101

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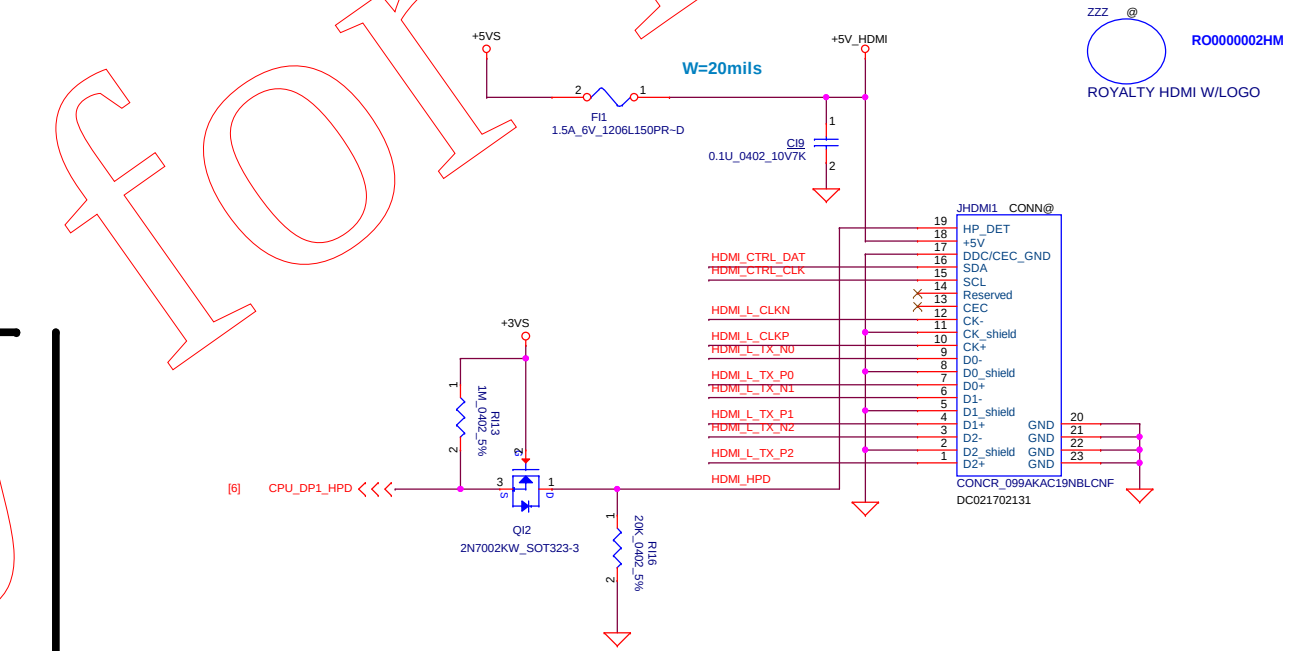
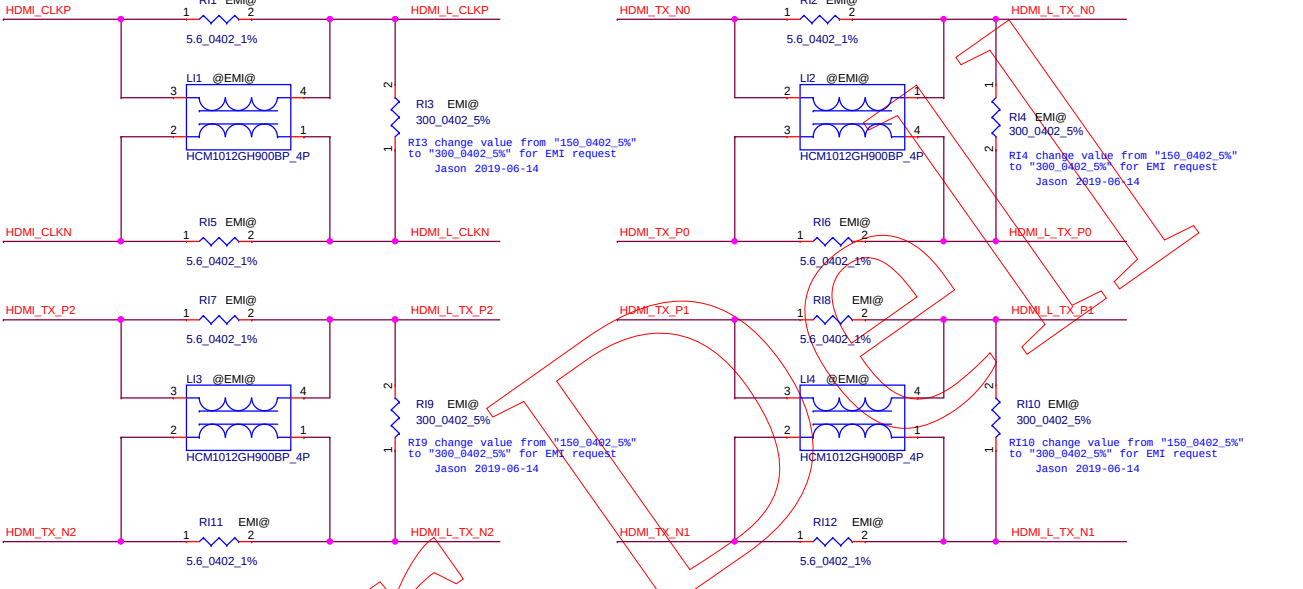
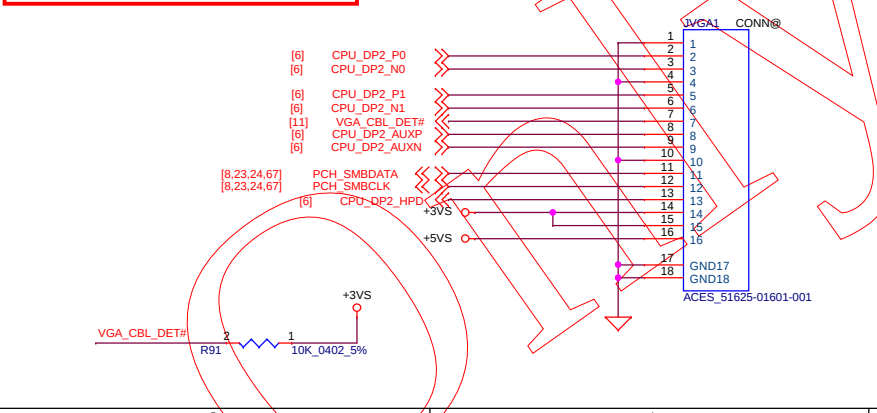
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				Date:	Thursday, June 20, 2019	Sheet 39 of 101

Main Func = HDMI



Main Func = VGA



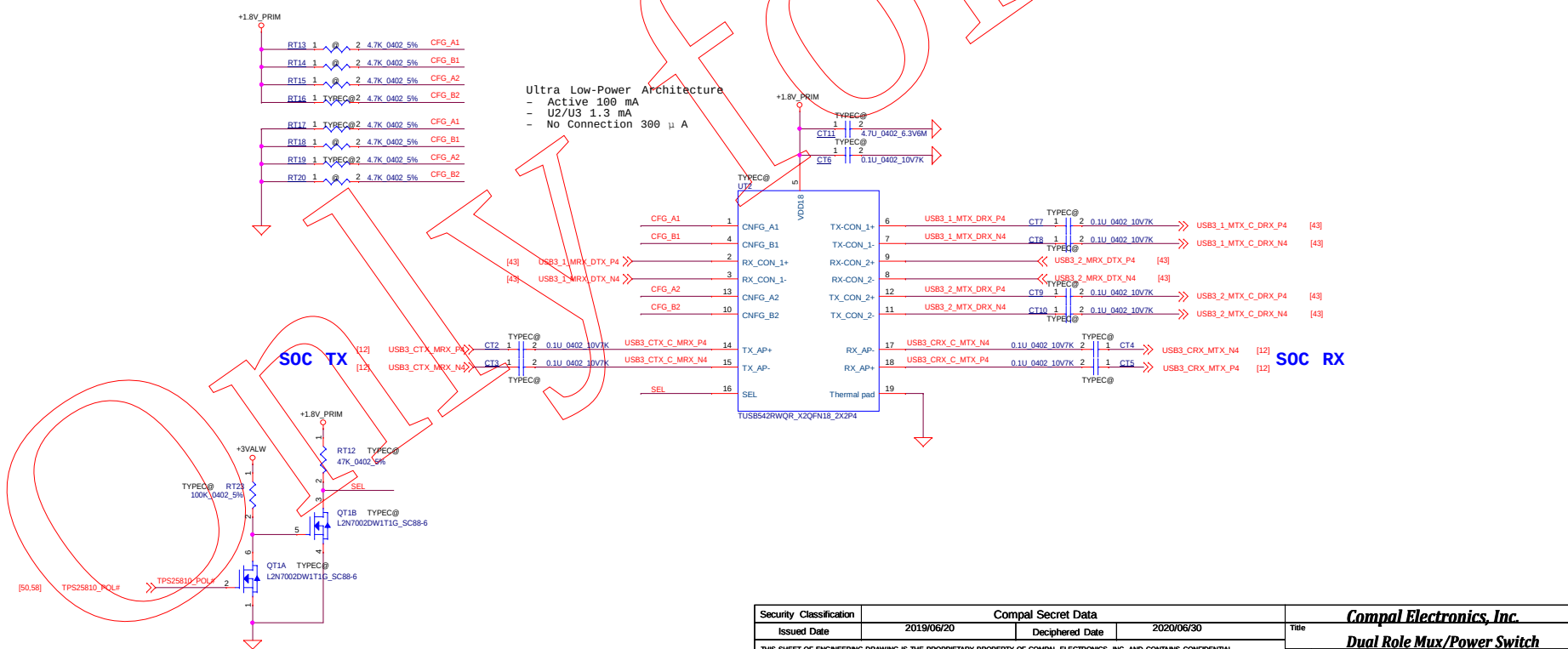
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				LA-G716P	Rev 1.0
				Date	Thursday, June 20, 2019
				Sheet	40 of 101

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				Date:	Thursday, June 20, 2019
				Sheet	41 of 101
				Rev	1.0
				LA-G716P	

Main Func = Typec MUX



Ultra Low-Power Architecture
- Active 100 mA
- U2/U3 1.3 mA
- No Connection 300 μ A

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LA-G716P					1.0	
Date: Thursday, June 20, 2019						
Sheet 42 of 101						

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					LA-G716P	1.0
				Date:	Thursday, June 20, 2019	Sheet 44 of 101

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Date: Thursday, June 20, 2019		Sheet 45 of 101			

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				LA-G716P	
Date:		Thursday, June 20, 2019		Sheet	46 of 101

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				LA-G716P	
Date:		Thursday, June 20, 2019		Sheet	47 of 101

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					LA-G716P	1.0
Date: Thursday, June 20, 2019				Sheet	48	of 101

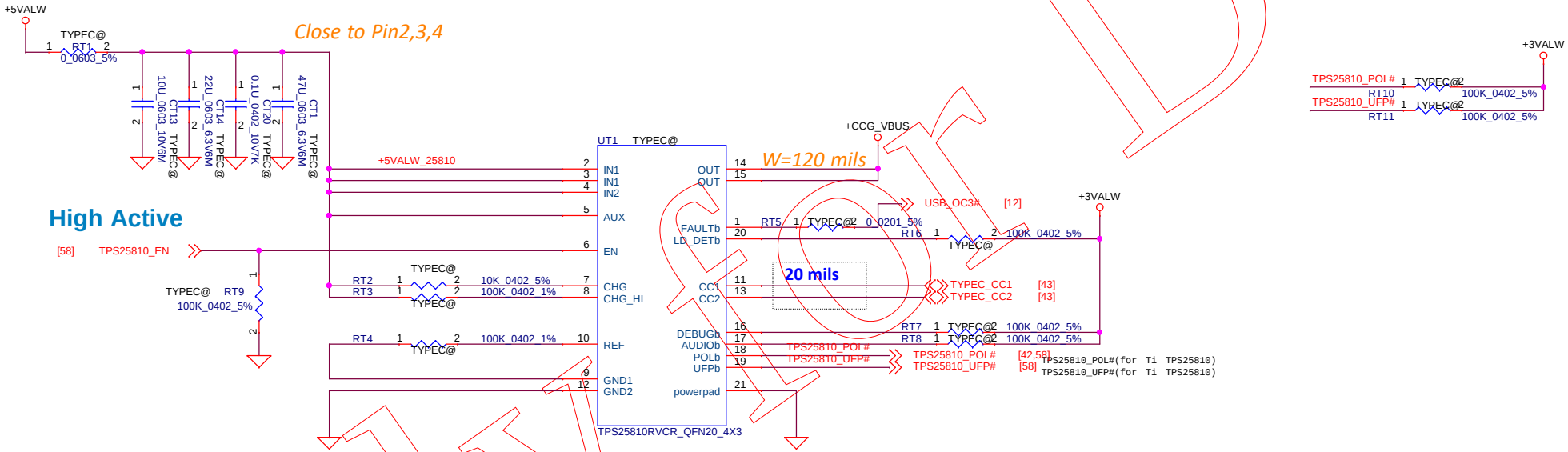
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Date: Thursday, June 20, 2019				Sheet	49	of 101

Main Function: TYPE-C_Power Path

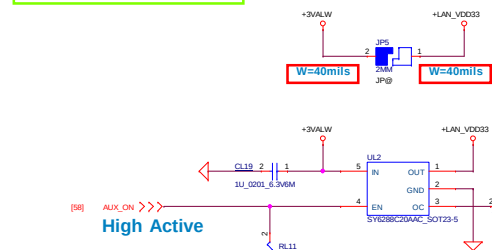
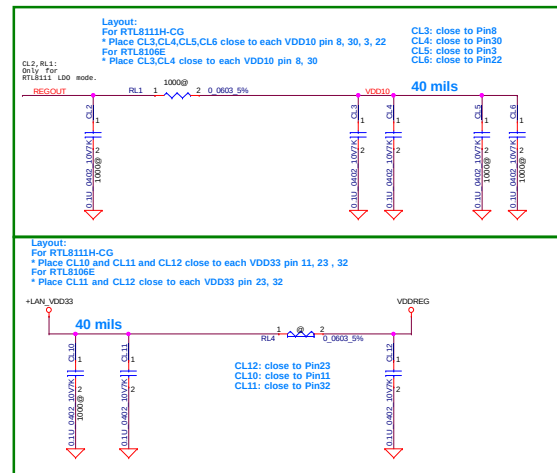
Main Func = Power Switch

5V@3A

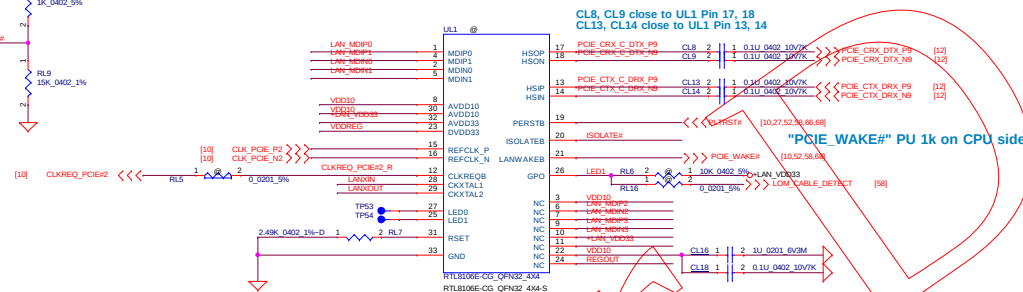
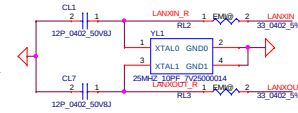
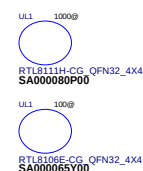
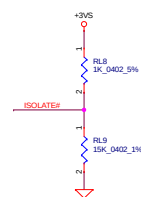


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Size		Document Number			Rev
		LA-G716P			1.0
Date:		Thursday, June 20, 2019		Sheet	50 of 101

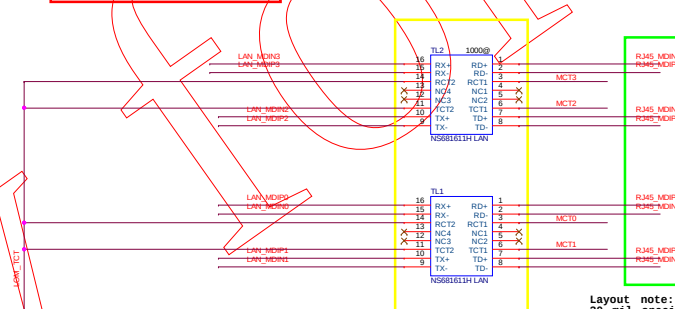
Main Func = LAN

**LAN CHIP 10/100/1000**

RTL8111H-CG	RTL8106E-CG
SA000000P00	SA0000005Y00
LDO mode	LDO mode
10/100/1000M	10/100M

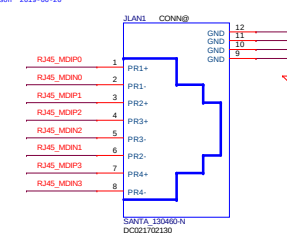
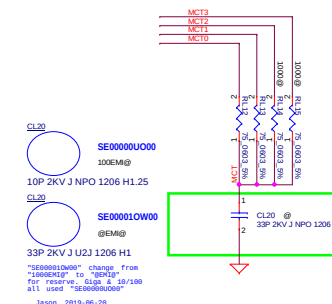


Main Func = LAN *LAN TransFormer 10/100M x2*



TL1 TOP, TL2 BOT

Layout note:
30 mil spacing between MDI differential pairs.



	1.0V Source	RL1	CL2	CL5	CL6	CL10	CL12
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	0	0	0	0	0	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	0

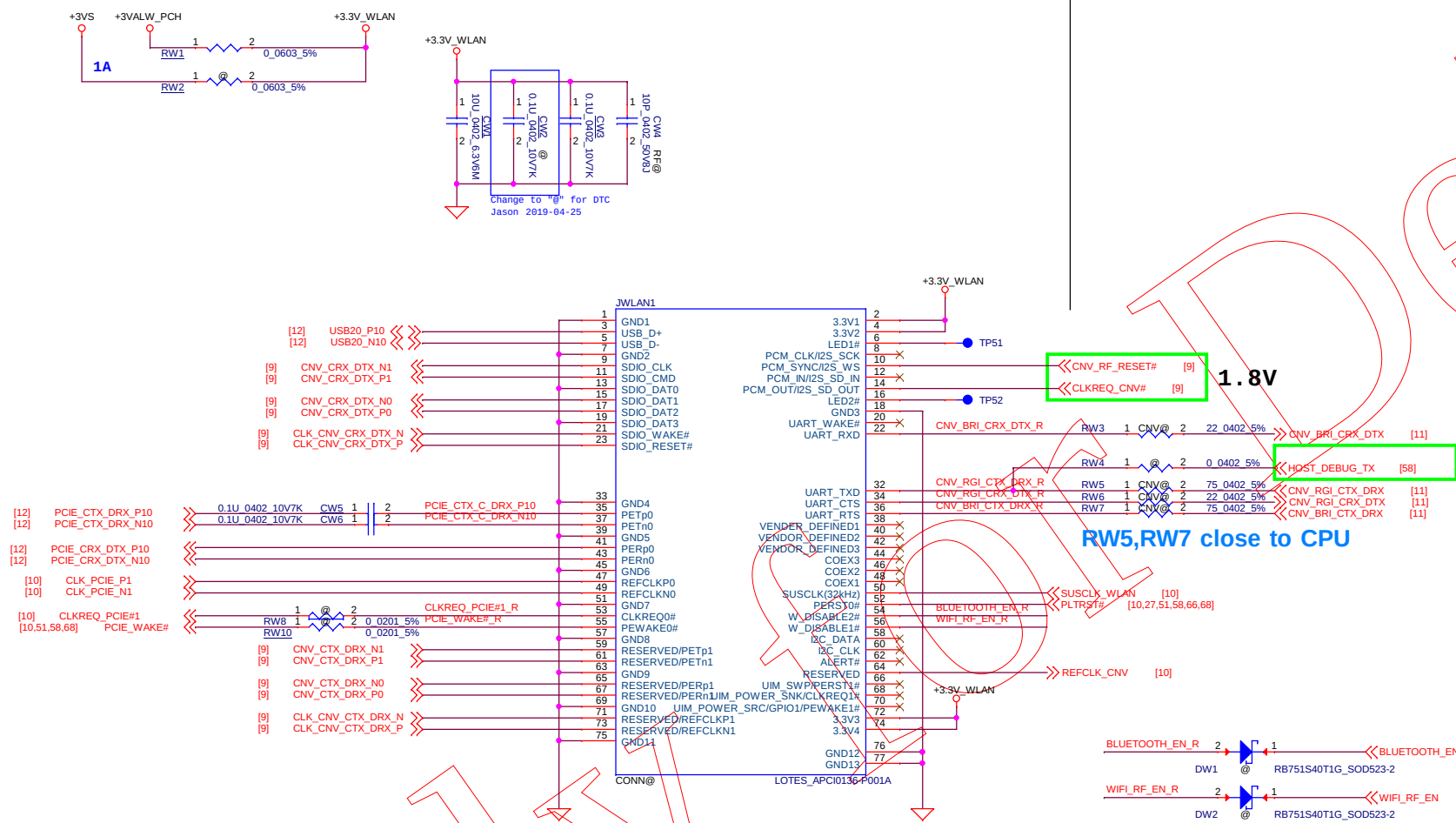
Layout note:
30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF

Main:
SP050006H00, S X'FORM_ NS0014 LF LAN
2nd:
SP050006W00, S X'FORM_ HD-245 10/100 PC CARD LAN

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Issued Date	2019/06/20	Deciphered Date	2020/06/30	Title	LAN RTL111/RTL8106	
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				LA-G716P		1.0
				Date	Thursday, June 20, 2019	
				Sheet	81	of 101

Main Func = WLAN E Key CONN



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Issued Date		2019/06/20		Deciphered Date		Title		
						NGFF WLAN CONN		
						Size		Rev
						Document Number		1.0
						LA-G716P		
						Date: Thursday, June 20, 2019		Sheet 52 of 101

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					LA-G716P
				Date:	Thursday, June 20, 2019
				Sheet	53 of 101
				Rev	1.0

Main Function:

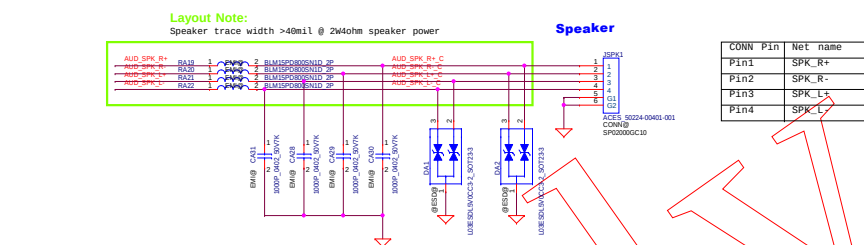
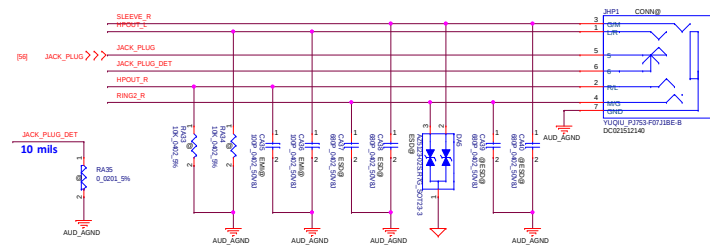
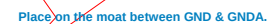
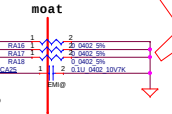
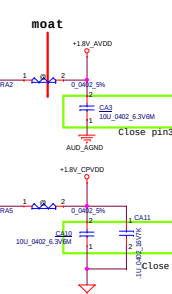
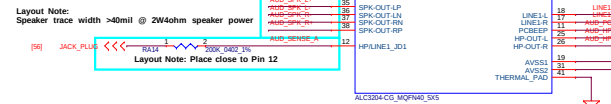
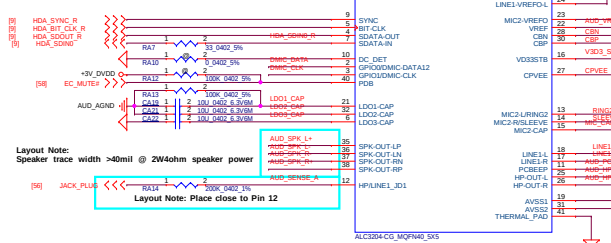
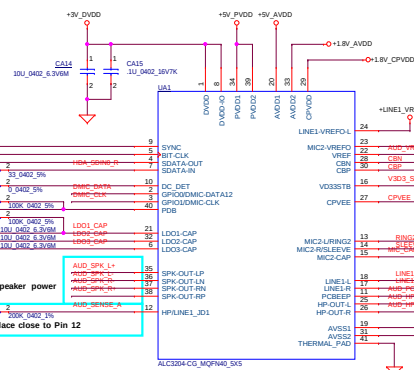
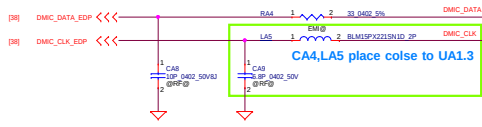
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					LA-G716P	1.0
				Date:	Thursday, June 20, 2019	Sheet 54 of 101

Main Function:

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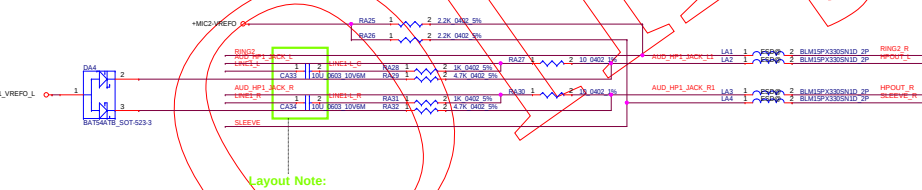
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Issued Date	2019/06/20	Deciphered Date	2020/06/30	Title	(RSVD)
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				Date:	Thursday, June 20, 2019
				Sheet	55 of 101
				Rev	1.0
				LA-G716P	



CONN	Pin	Net name
	Pin1	SPK_R+
	Pin2	SPK_R-
	Pin3	SPK_L+
	Pin4	SPK_L-

main Func = Audio Jack

Universal Jack
(Global Headset Jack + mic phone in + line in support)

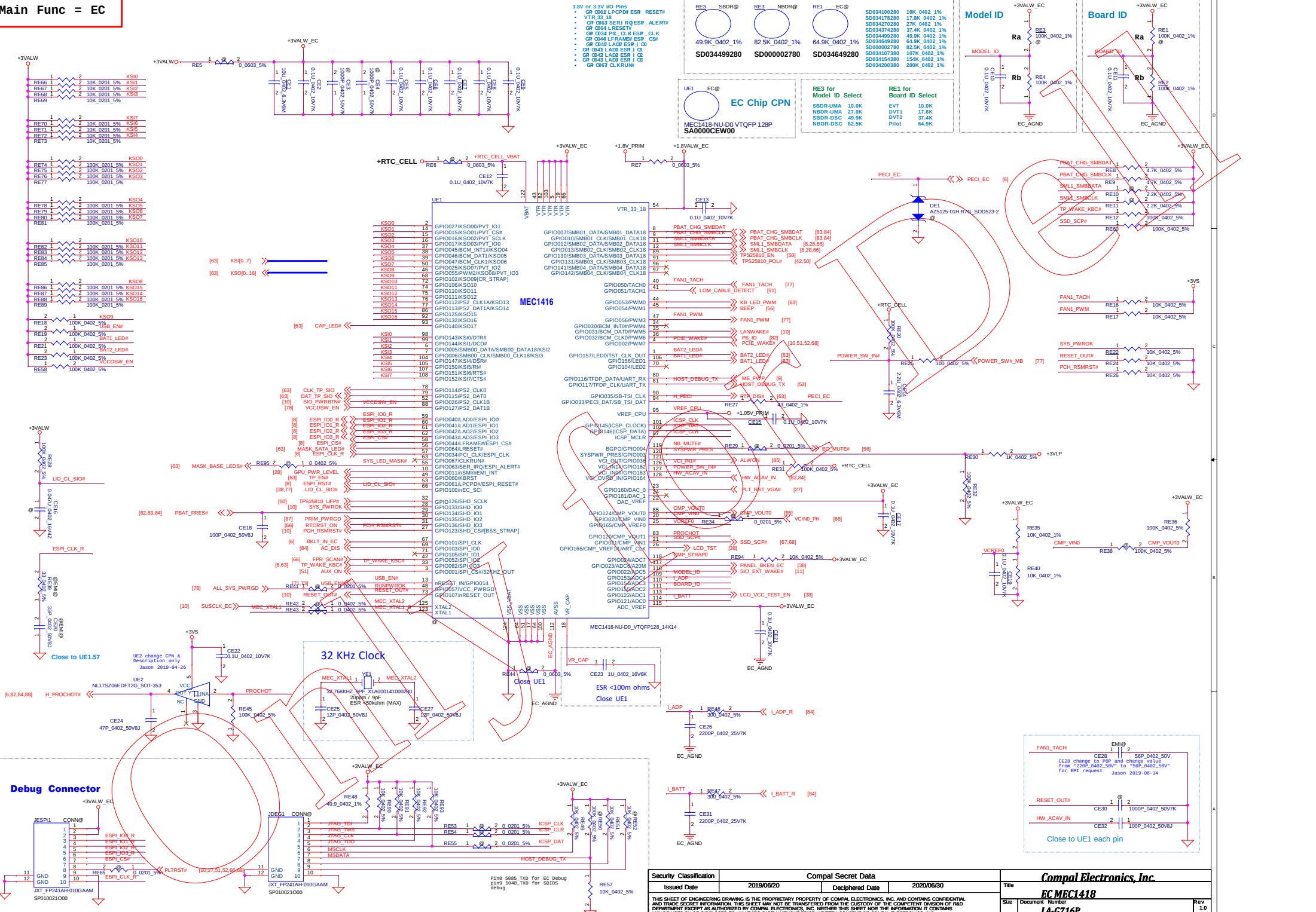


Main Function:

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					LA-G716P	1.0
Date: Thursday, June 20, 2019				Sheet	57	of 101

Main Func = EC



Main Function:

Reserve

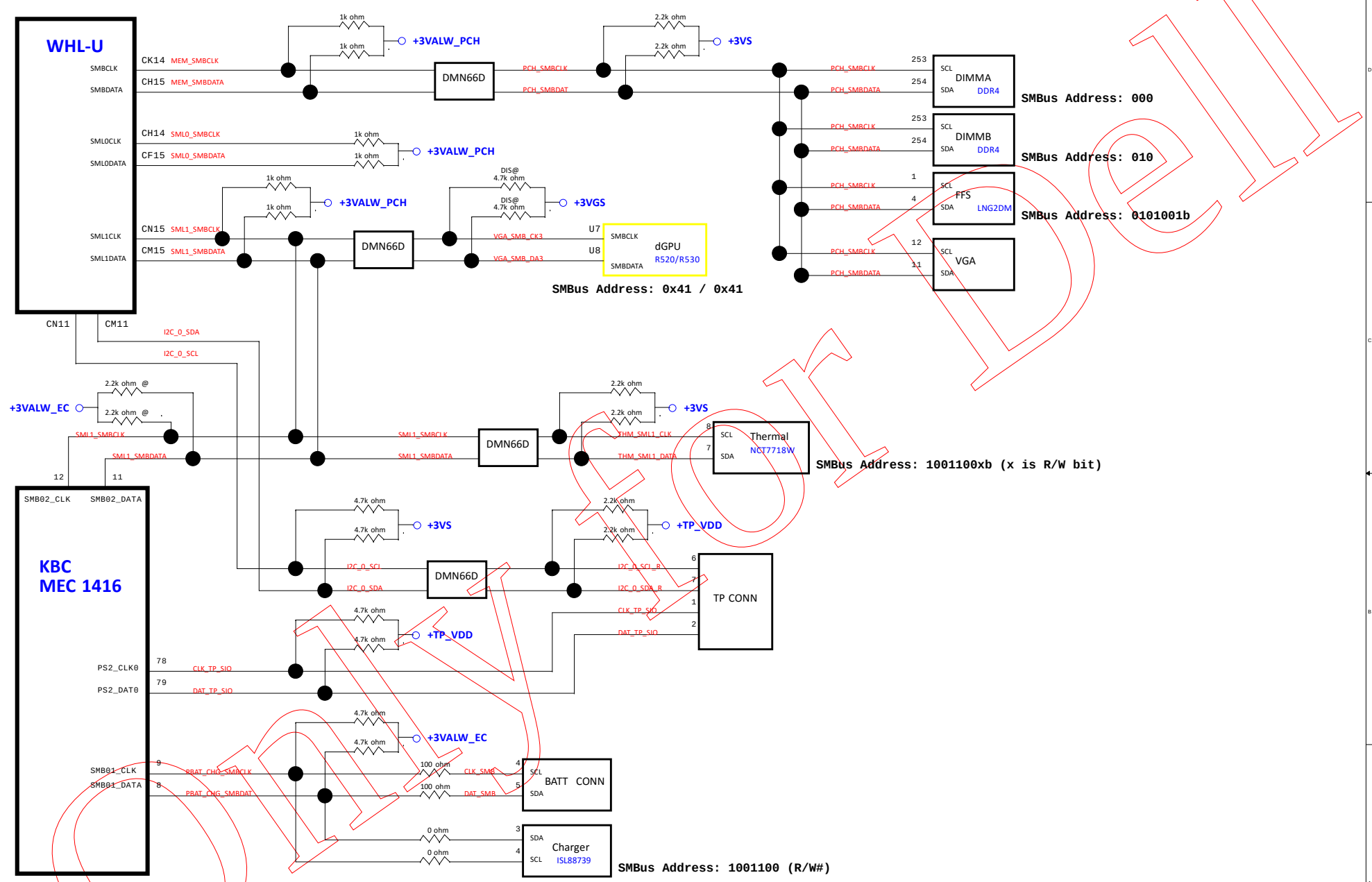
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2019/06/20	Deciphered Date	2020/06/30	Title	(RSVD)	
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				Date:	Thursday, June 20, 2019	Sheet 59 of 101

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					LA-G716P	1.0
				Date:	Thursday, June 20, 2019	Sheet 60 of 101

Main Function:SMB/I2C Block Diagrams

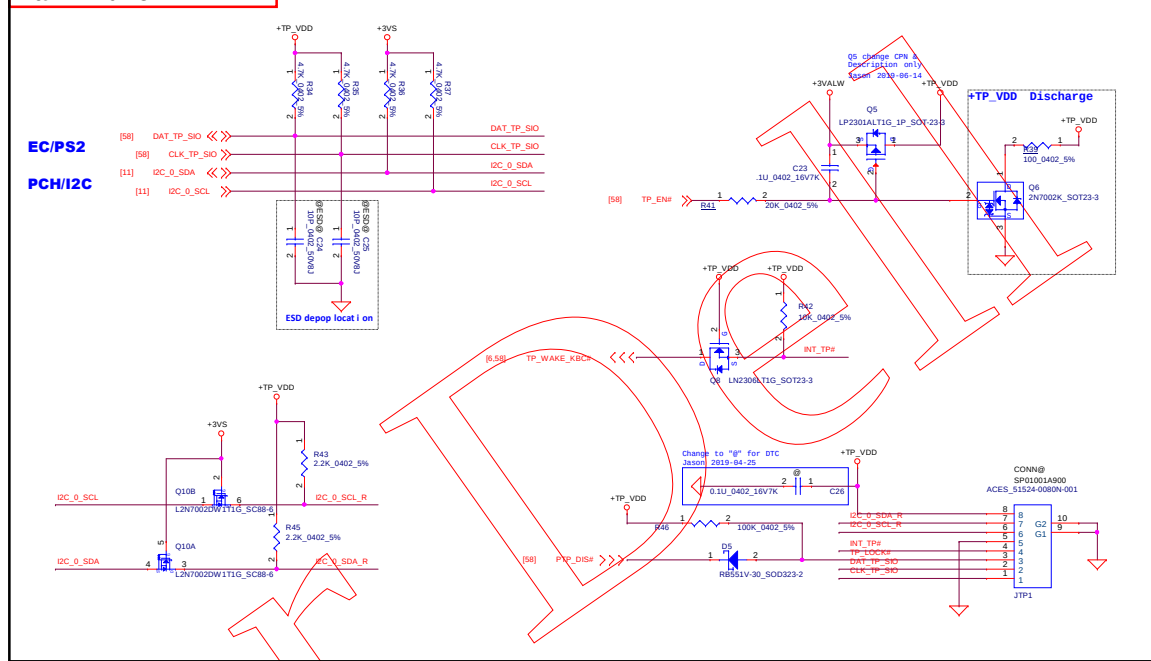
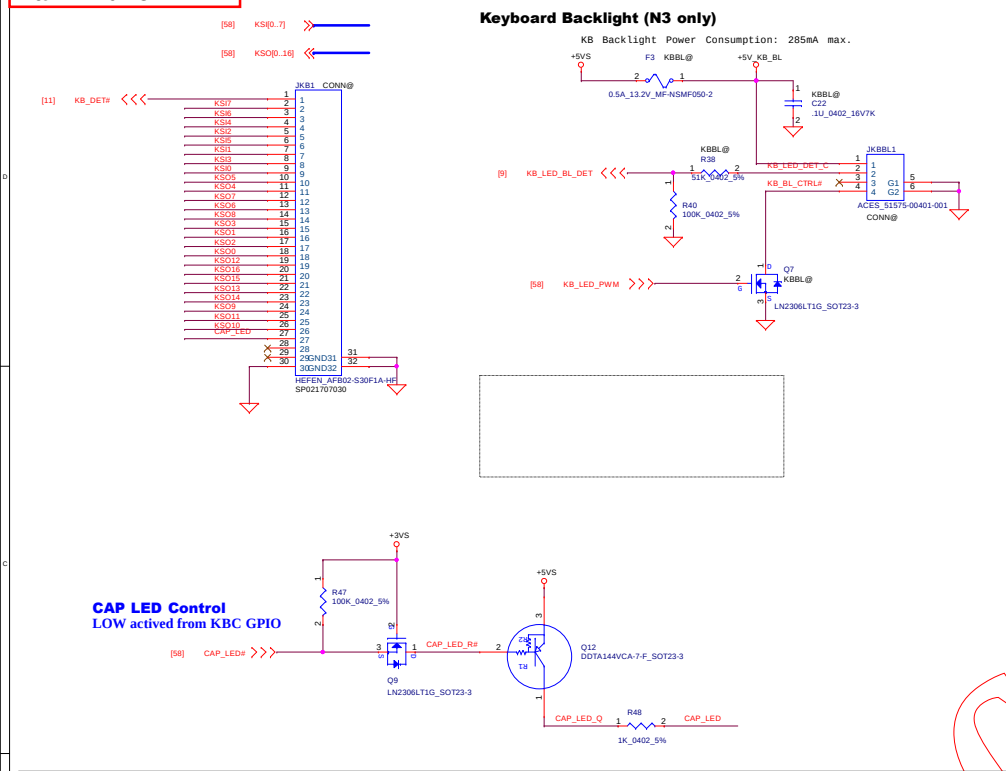


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					LA-G716P	1.0
				Date:	Thursday, June 20, 2019	Sheet 62 of 101

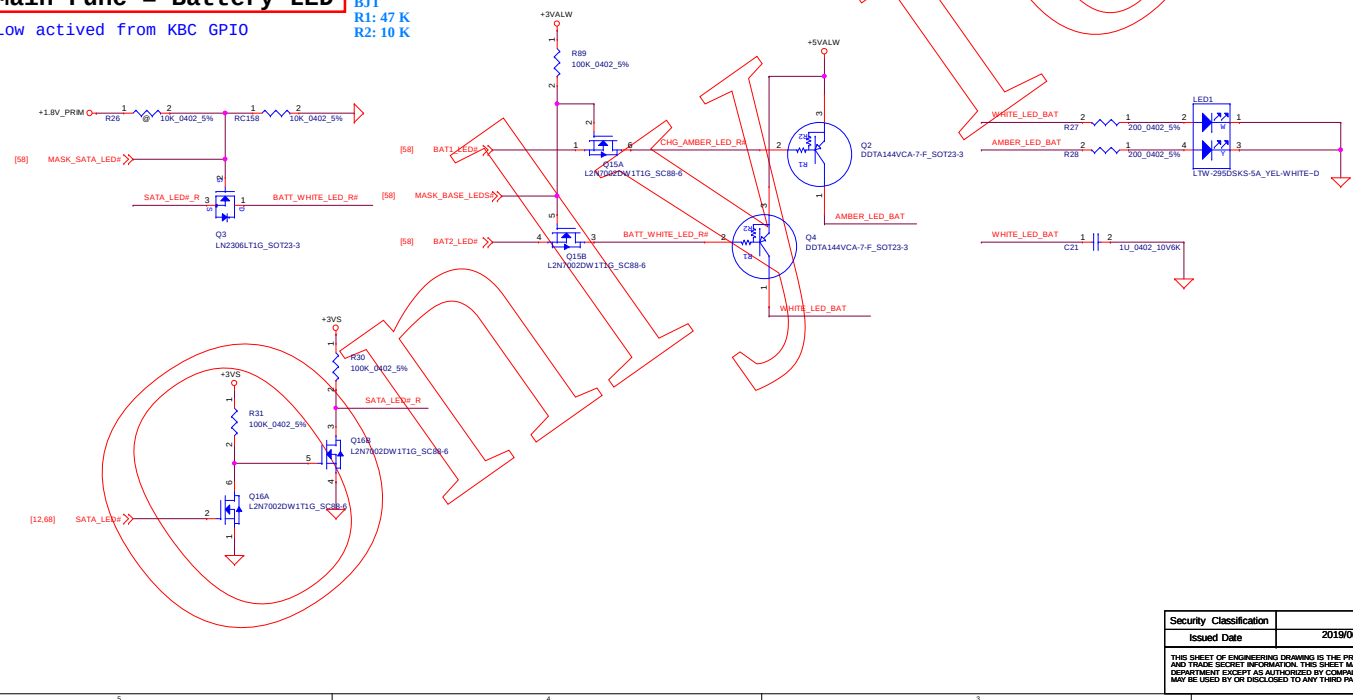
3
Main Func = TPAD



Main Func = Battery LED

Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K



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			Date: Thursday, June 20, 2019	Sheet 63 of 101

Main Function:

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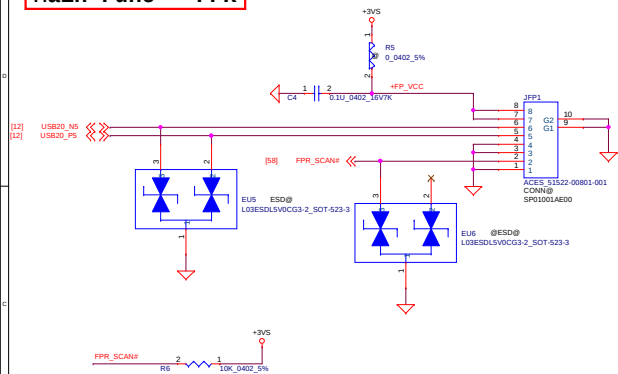
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/06/20	Deciphered Date	2020/06/30	Title	(RSVD)
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				Date:	Thursday, June 20, 2019
				Sheet	64 of 101
				Rev	1.0
				LA-G716P	

Main Function:

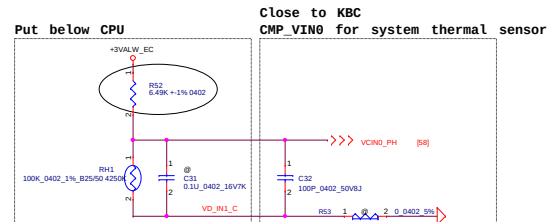
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				Date:	Thursday, June 20, 2019
				Sheet	65 of 101
				Rev	1.0
				LA-G716P	

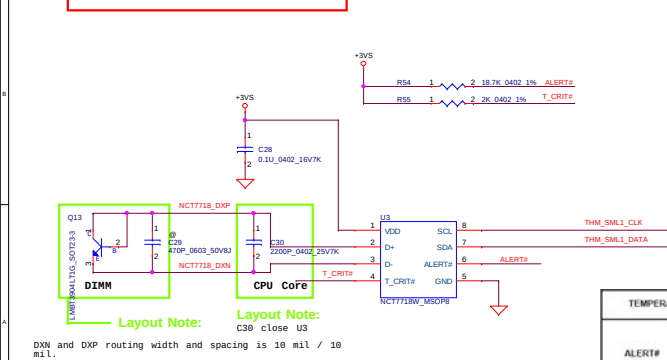
Main Func = FPR



Main Func = OTP

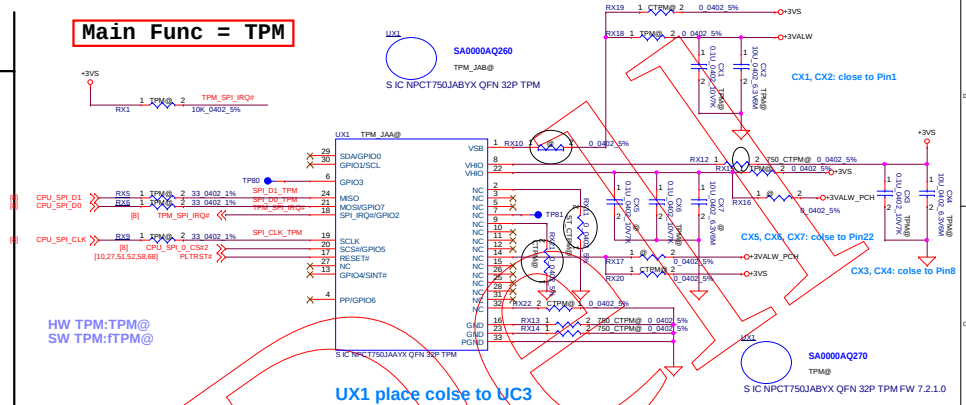


Main Func = Thermal

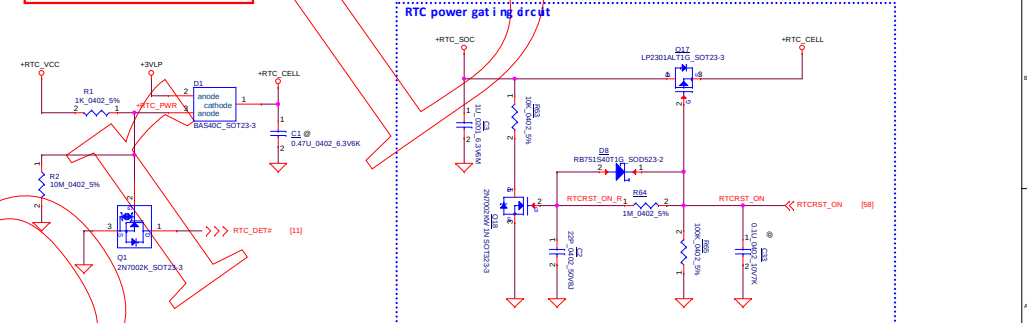


TEMPERATURE (°C)	T_CRIT#				
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
2KΩ	77	87	97	107	117
7.5KΩ	79	89	99	109	119
10.5KΩ	81	91	101	111	121
14KΩ	83	93	103	113	123
18.7KΩ	85	95	105	115	125

Main Func = TPM

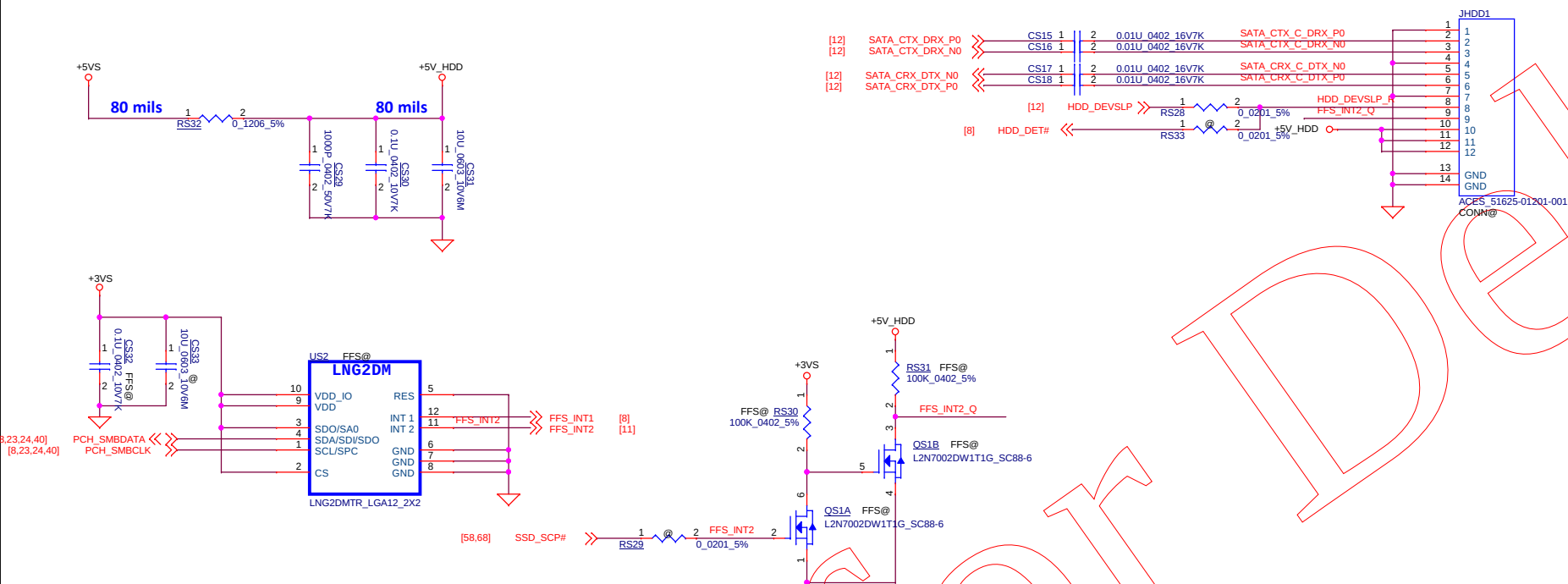


Main Func = RTC



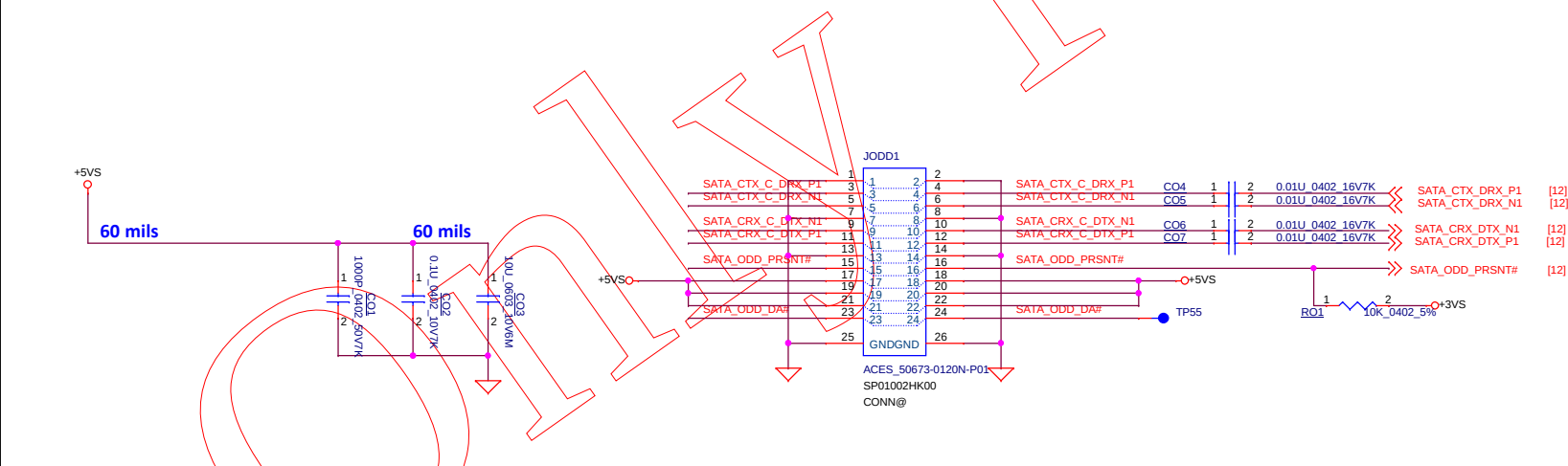
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Issued Date	2019/06/20	Deciphered Date	2020/06/30	Title
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				Document Number
				LA-0716P
				Rev
				1.0
				Date
				Thursday, June 20, 2019
				Sheet
				66 of 101

Main Func = HDD&FFS



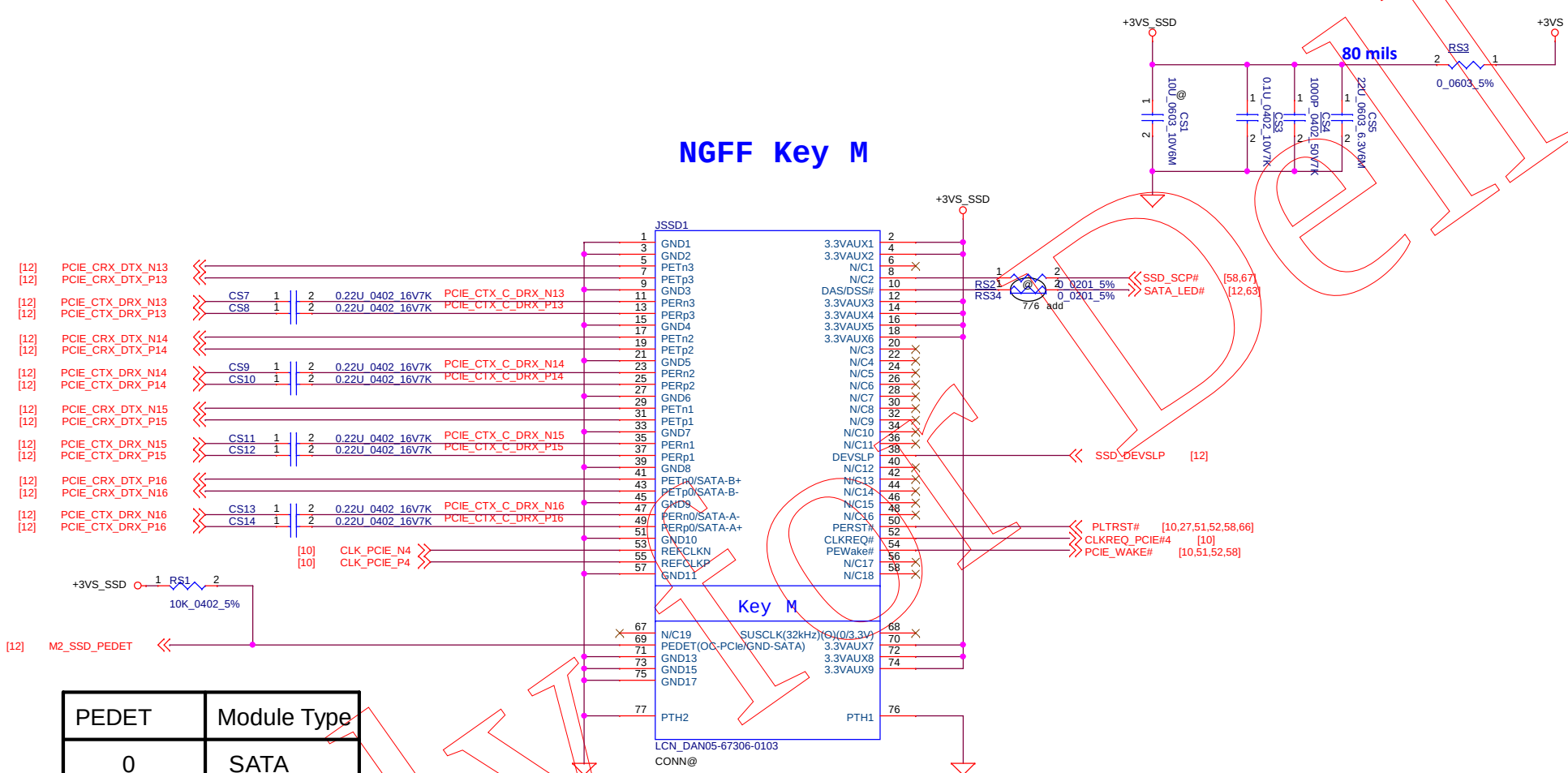
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	8
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	9

Main Func = ODD



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
PRSENT	P1	8
5V	P2	9
5V	P3	10
Attention	P4	12
GND	P5	
GND	P6	

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				Size	Document Number	Rev
				Custom	LA-G716P	1.
				Date:	Thursday, June 20, 2019	Sheet 67 of 101



Main Func = eMMC

Only for Del

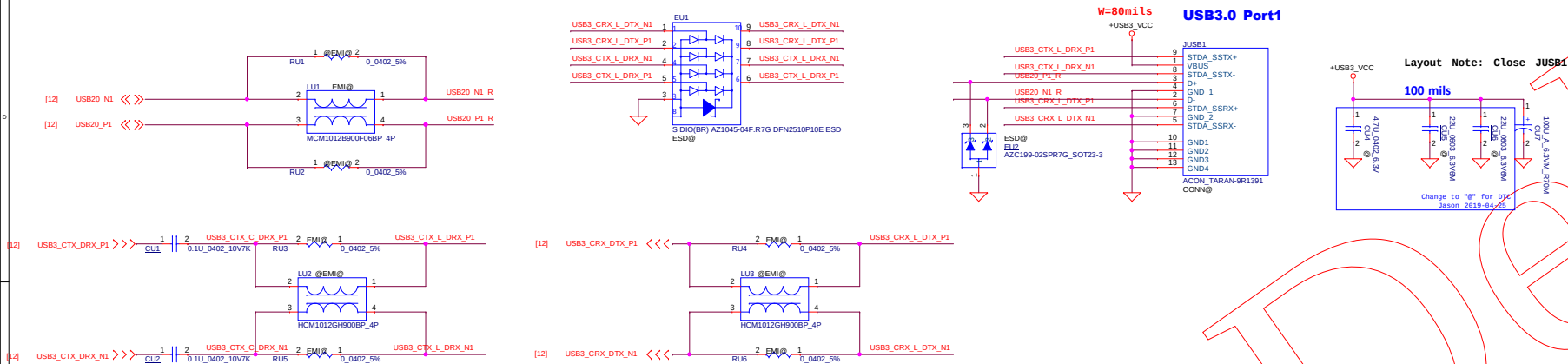
Security Classification	Compal Secret Data			Title		
Issued Date	2019/06/20	Deciphered Date	2020/06/30	eMMC (RSVD)		
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					LA-G716P	1.0
Date: Thursday, June 20, 2019				Sheet	69	of 101

Main Function:

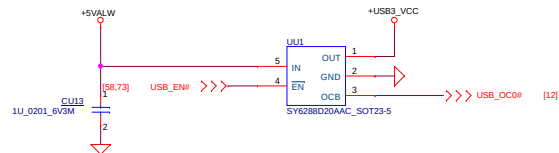
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				Date:	Thursday, June 20, 2019
				Sheet	70 of 101
				Rev	1.0
				LA-G716P	

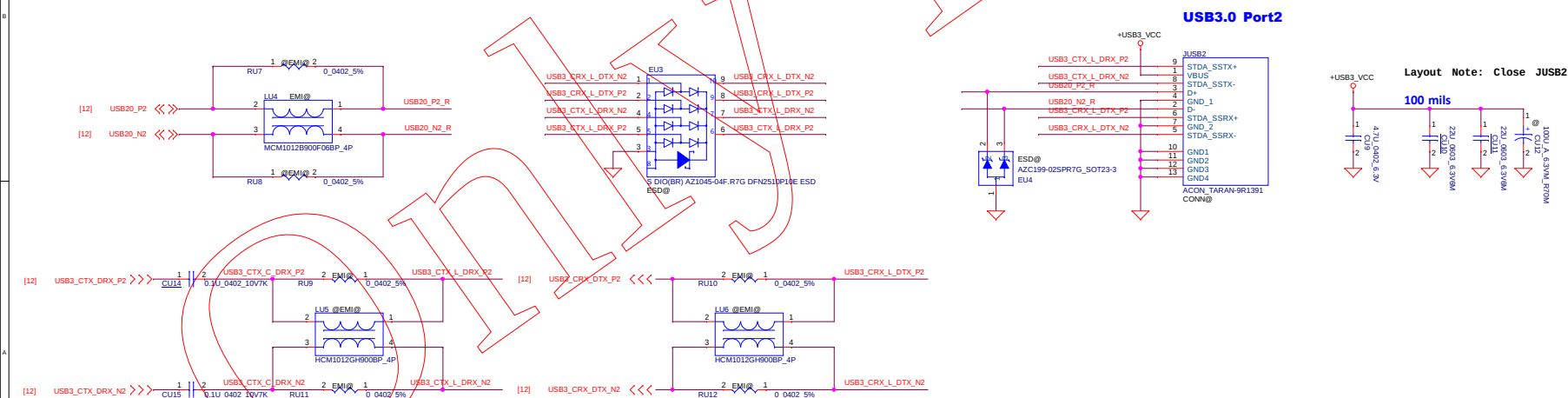
Main Func = USB3.0 Port1



Maximum Output
Current 2A



Main Func = USB3.0 Port2



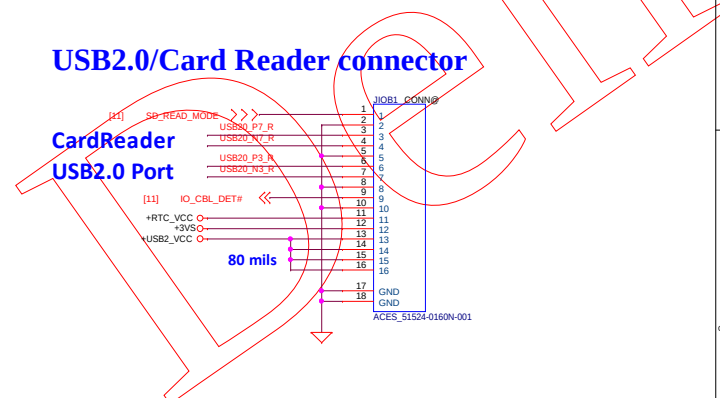
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Issued Date		Deciphered Date		Title		USB3.0	
2019/06/20		2020/06/30		Size		Document Number	
						LA-G716P	
						Rev 1.0	
						Date: Thursday, June 20, 2019	
						Sheet 71 of 101	

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					LA-G716P	1.0
				Date:	Thursday, June 20, 2019	Sheet 72 of 101

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					LA-G716P
				Date:	Thursday, June 20, 2019
				Sheet	74 of 101

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				Date:	Thursday, June 20, 2019
				Sheet	75 of 101
				Rev	1.0
				LA-G716P	

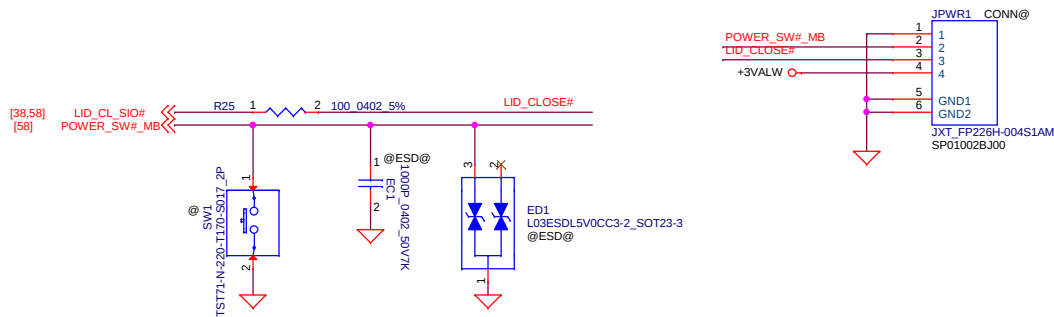
Main Function:

Reserve

Only for Del

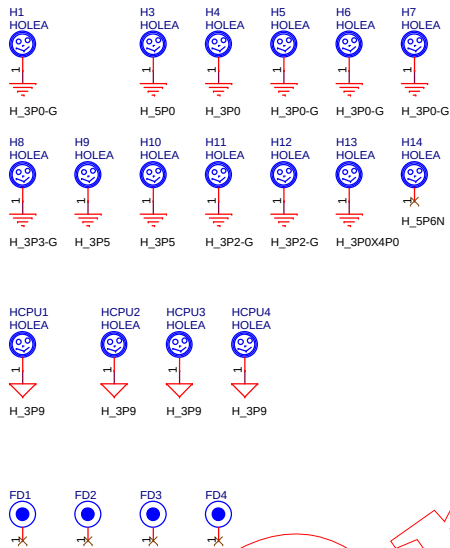
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Issued Date	2019/06/20	Deciphered Date	2020/06/30	Title	(RSVD)
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				Date:	Thursday, June 20, 2019
				Sheet	76 of 101
				Rev	1.0
				LA-G716P	

Main Func = Power BTN Low actived from KBC GPIO

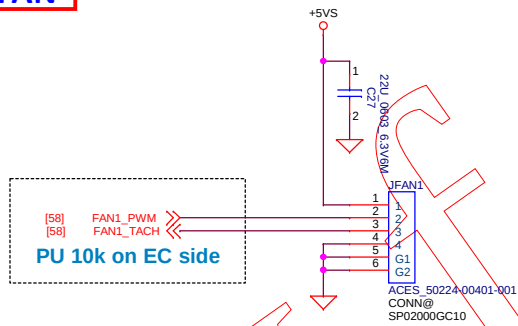


For EMI Reserved
LID_CLOSE# EC2 1 2 0.1U 0402 10V7K

Screw hole/FD

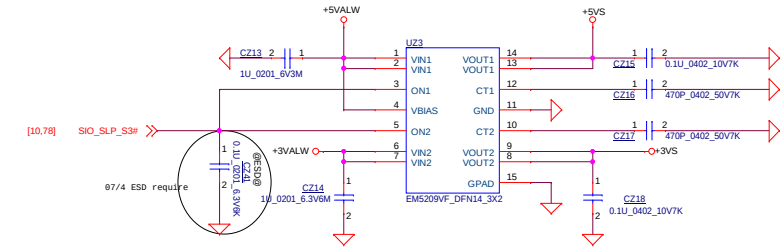


FAN

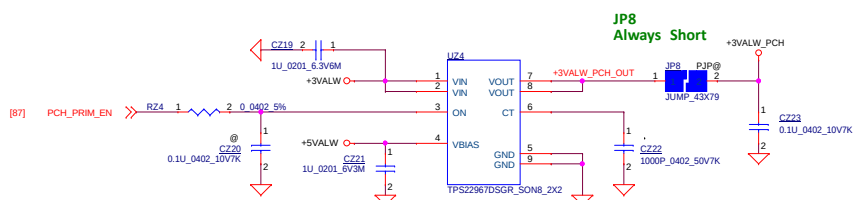


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					LA-G716P	1.0
				Date:	Thursday, June 20, 2019	Sheet 77 of 101

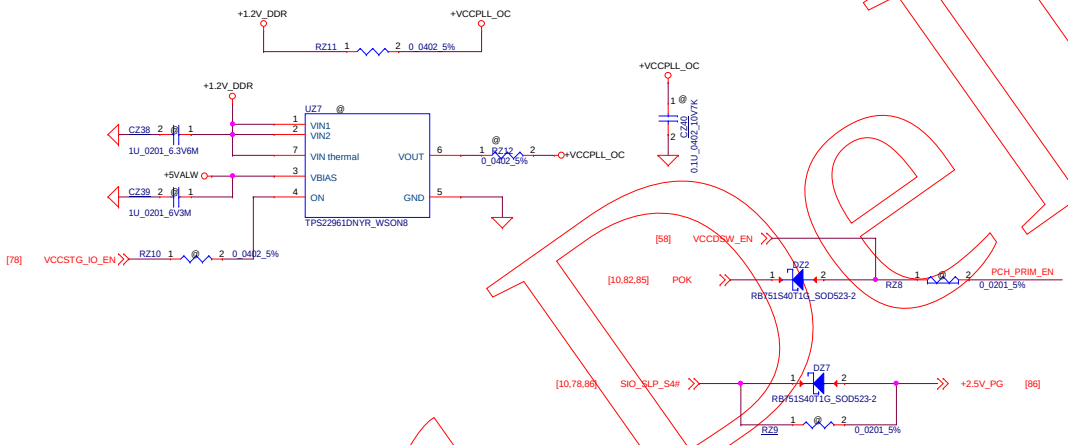
+5VS/+3VS for System



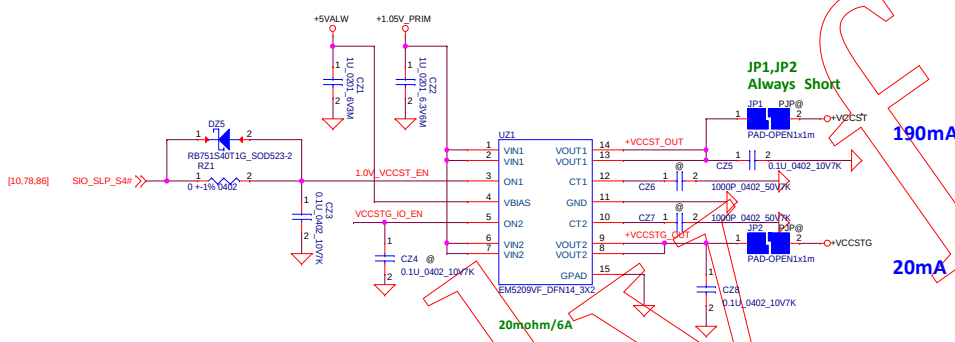
+3VALW_PCH for System



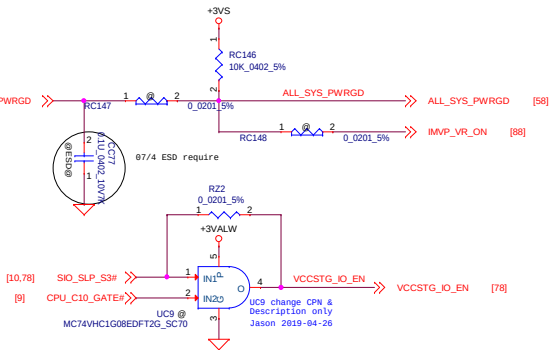
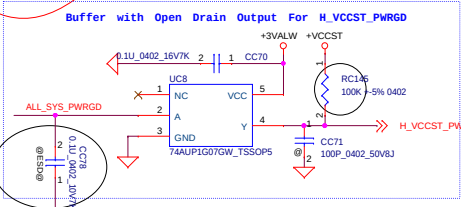
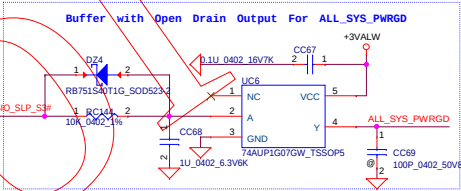
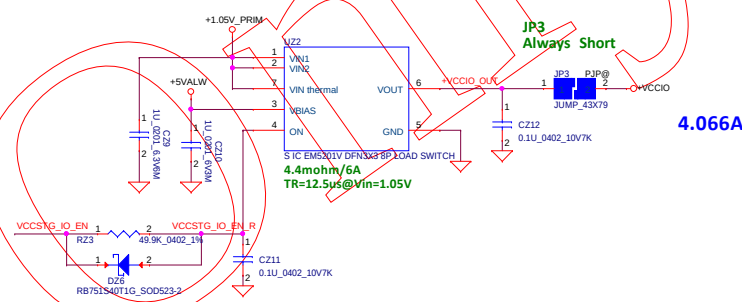
+VCCPLL_OC source



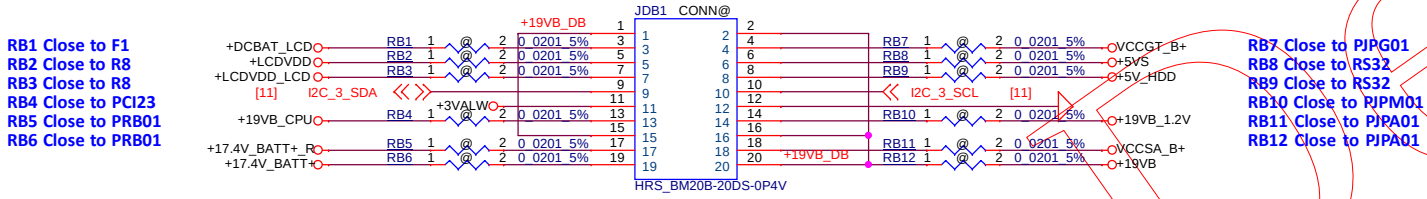
+1.05V_PRIM TO +VCCST /+VCCSTG



+1.05V_PRIM TO +VCCIO



Main Func = Power Monitor



2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19

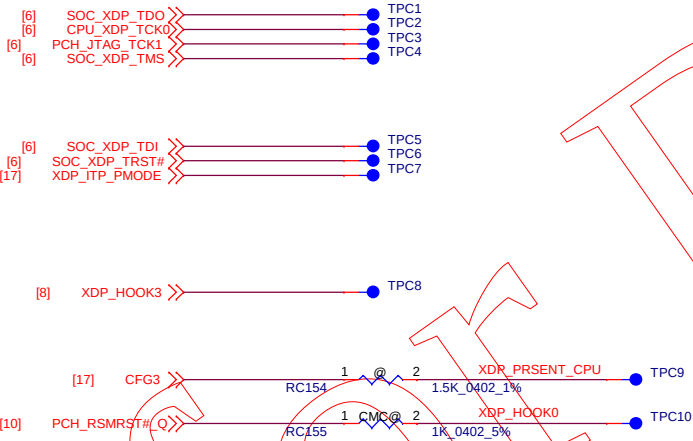
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Issued Date		2019/06/20		Deciphered Date	
2019/06/20		2020/06/30		Title	
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Date:		Thursday, June 20, 2019		Sheet 79 of 101	

PortConnector Less Routing Topology

Follow KBL DCI Link
RC152 need POP
RC156 need POP

Place to CPU side

Place to CPU side



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				Size	Document Number	Rev
				B	LA-G716P	1.0
				Date:	Thursday, June 20, 2019	Sheet 80 of 101

Reserve

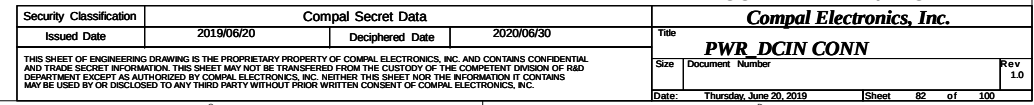
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		Compal Electronics, Inc.	
File		Reserve for PWR	
Size	Document Number	Rev 1.0	
Date: Thursday, June 20, 2019	Sheet 81 of 100		

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SPEC = 6KV

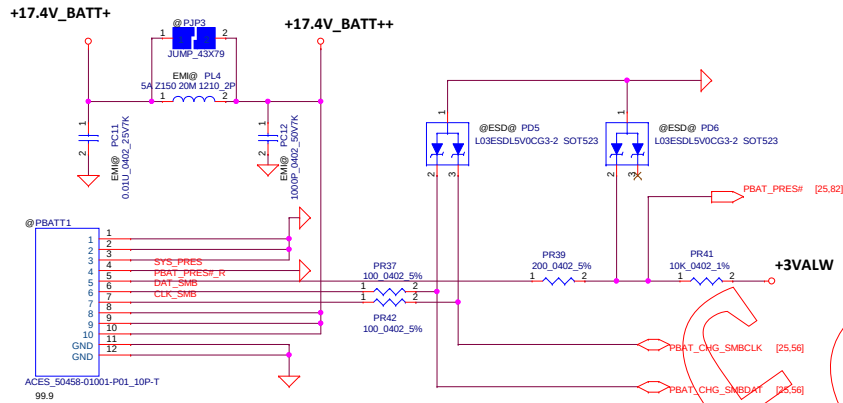


Main Func = BATT CONN

Bat tery Bat Side

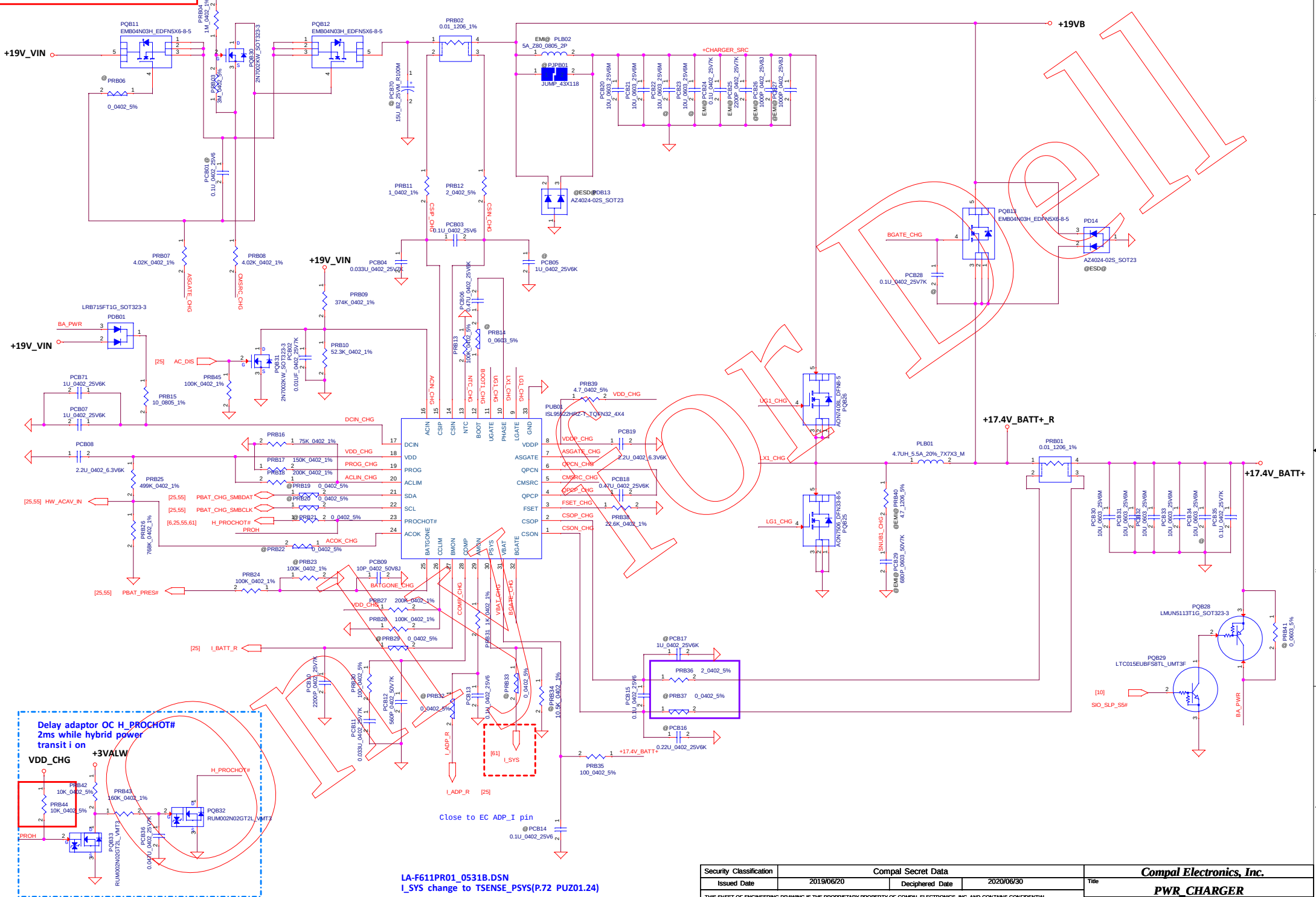
PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Bat t+
PIN9 Bat t+
PIN10 Bat t+
SP021412220

ACES_50458-01001-P01_10P-T



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2019/06/20		2020/06/30		PWR_BATT_CONN	
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				Rev 1.0	
				Date: Thursday, June 20, 2019	Sheet 83 of 100

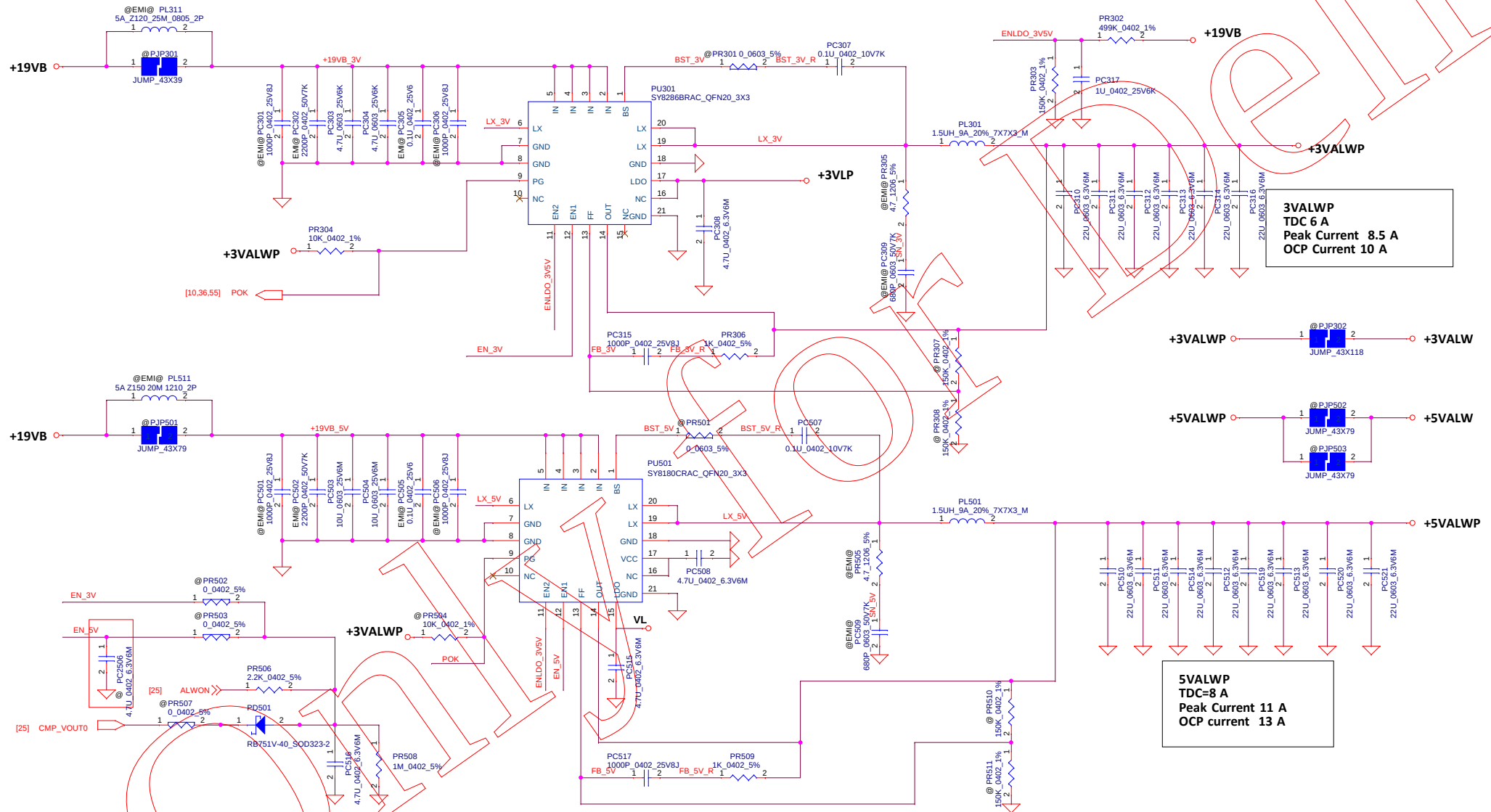
Main Func = CHARGER



LA-F611PR01_0531B.DSN
I_SYS change to TSENSE_PSYS(P.72 PUZ01.24)

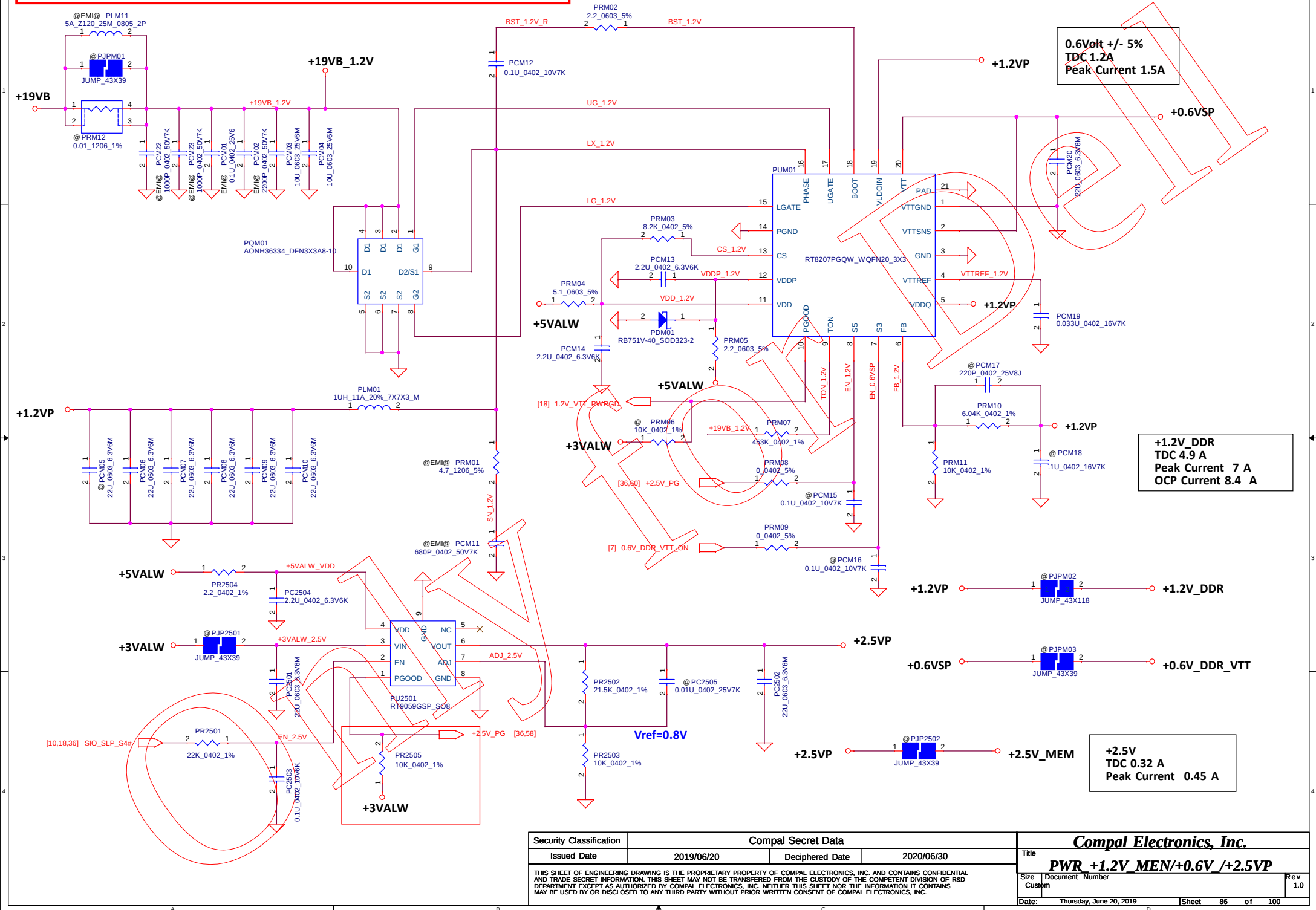
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Issued Date	2019/06/20	Deciphered Date	2020/06/30	Title		
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				Size	Document Number	Rev
				LA-F711P		1.0
Date: Thursday, June 20, 2019				Sheet 84 of 100		

Main Func = 3.3VALWP/5VALWP

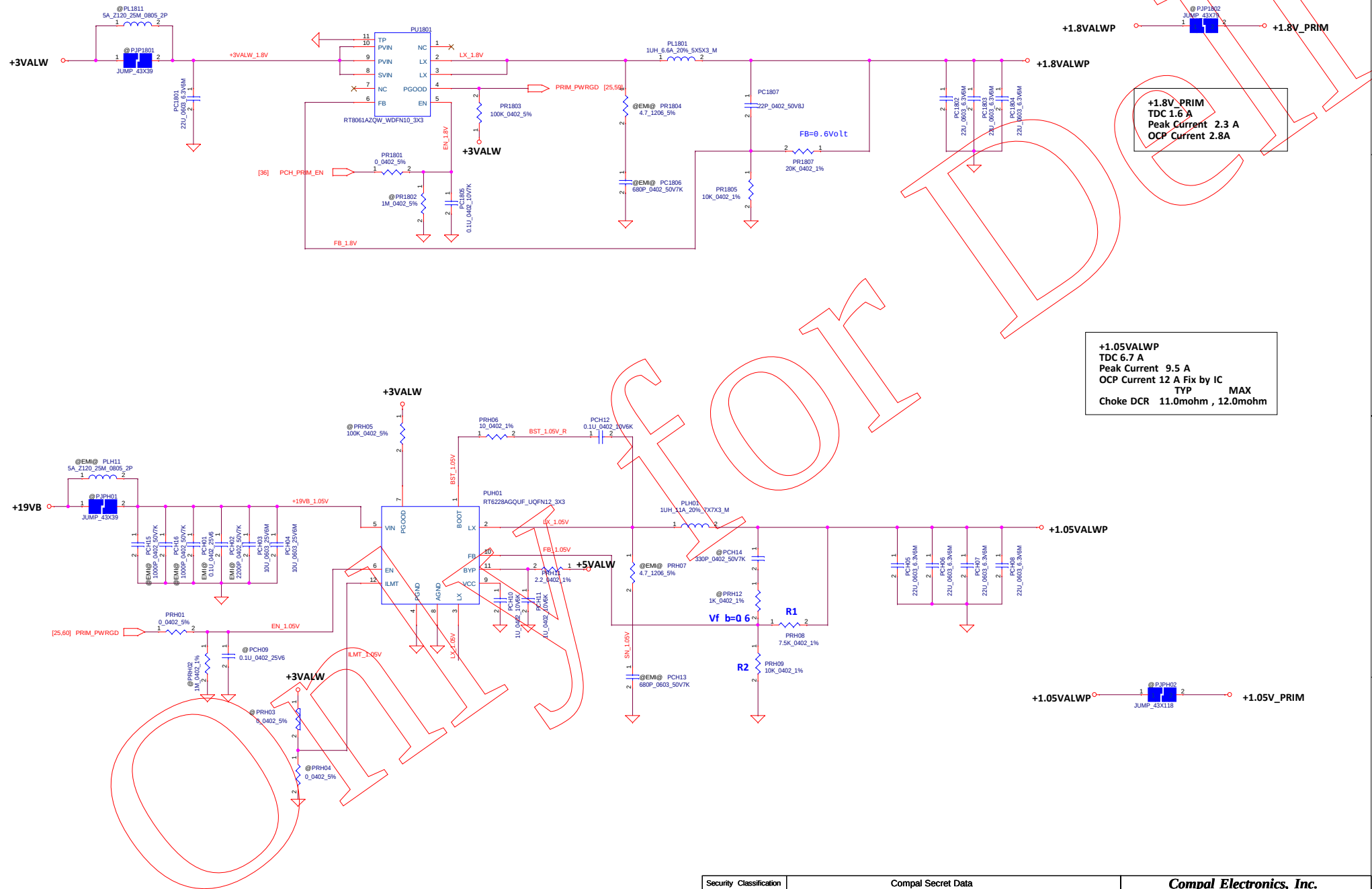


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				Size	Document Number	Rev
				Date	Thursday, June 20, 2019	Sheet 85 of 100

Main Func = +1.2V_DDR/+0.6V_DDR_VTT/+2.5VP



Main Func = +1.8VALWP /+1.05VALWP

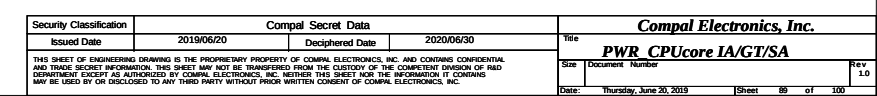


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Issued Date	2019/06/20	Deciphered Date	2020/06/30	Title PWR +1.8VALWP /+1.05VALWP	
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				Date: Thursday, June 20, 2019	Sheet 87 of 100

Main Func = CPU

<https://shop62935598.taobao.com>

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Size	Document Number	Rev		Date: Thursday, June 20, 2019	
		1.0		Sheet 88 of 100	

[illegible]

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Date	Thursday, June 20, 2019			Sheet	89 of 100

Main Func = CPU/ VGA / SA MLCC



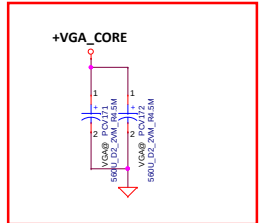
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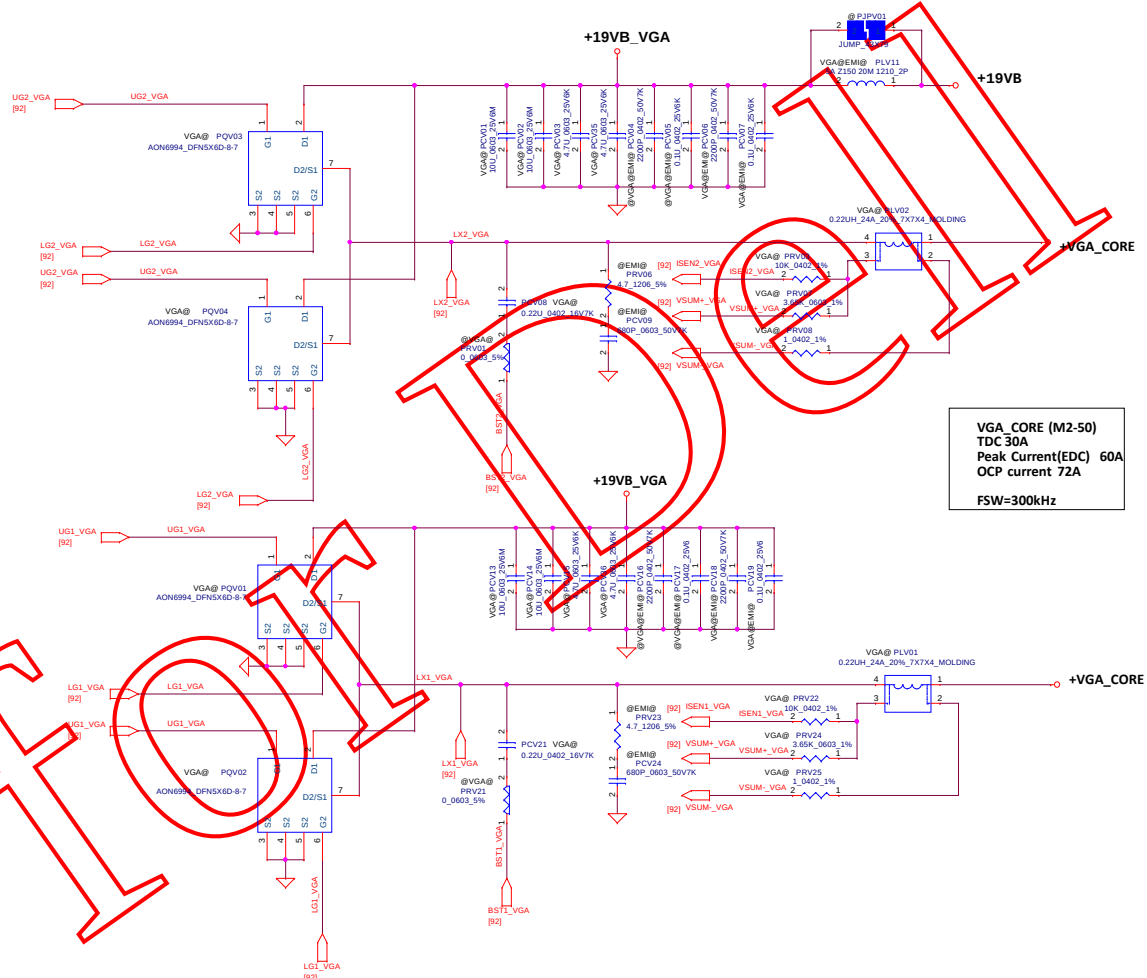
	Title		
	Compal Electronics, Inc.		
	Reserve for PWR		
	Size	Document Number	Rev 1.0
Date: Thursday, June 20, 2019		Sheet 91 of 100	

Main Func = VGA CORE



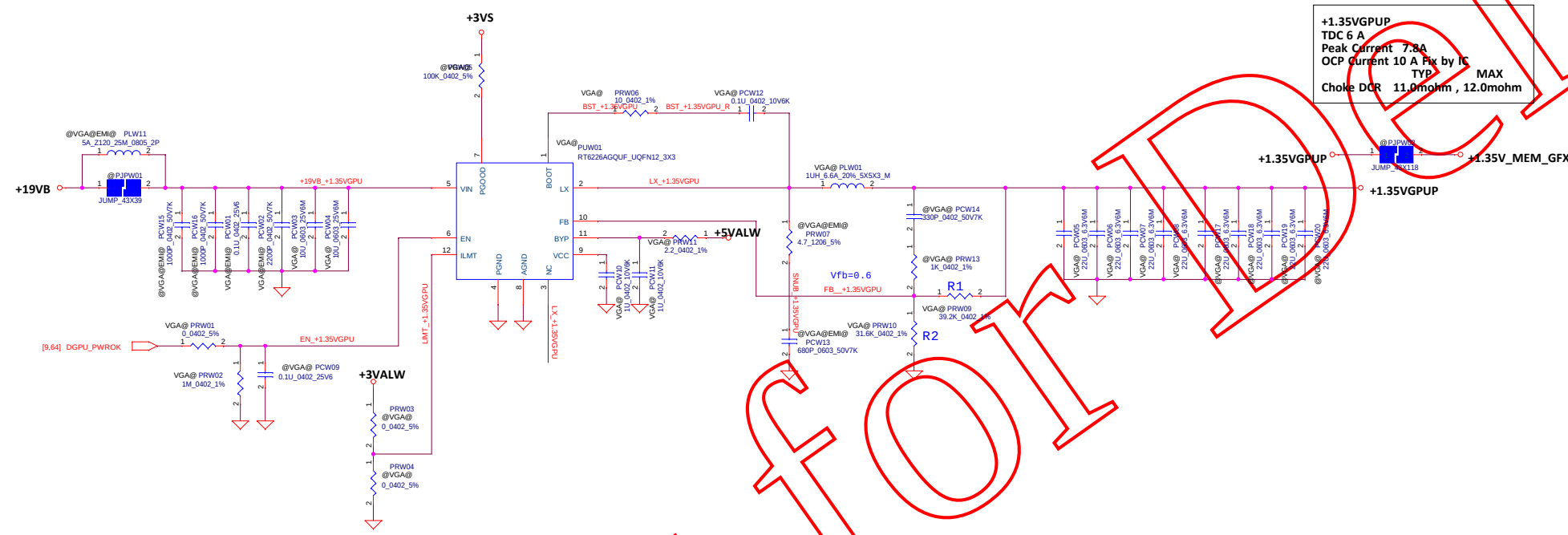
for VGACORE

ONLY



VGA_CORE (M2-50)
TDC 30A
Peak Current(EDC) 60A
OCP current 72A
FSW=300kHz

Main Func = +1.35VGUP



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Size		Document Number		Rev		
Date: Thursday, June 20, 2019		Sheet		94 of 100		

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Title		Reserve for PWR	
Size	Document Number	Rev 1.0	
Date: Thursday, June 20, 2019	Sheet 95 of 100		

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	Size	Document Number	Rev 1.0
	Date: Thursday, June 20, 2019	Sheet 96 of 100	

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File		Reserve for PWR	
Size	Document Number	Rev 1.0	
Date: Thursday, June 20, 2019	Sheet 97 of 100		

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File		Reserve for PWR	
Size	Document Number	Rev 1.0	
Date: Thursday, June 20, 2019	Sheet 98 of 100		

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File		Reserve for PWR	
Size	Document Number	Rev 1.0	
Date: Thursday, June 20, 2019	Sheet 99 of 100		

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Version Change List (P. I. R. List)

Item	Page#	Date	Request Owner	Issue Description	Solution Description	Rev.
1.	P84-PWR_CHARGER	2018 06/12	Compal	Vendor suggest	Change the PRB11 from 20hm to 10hm	X01
2.	P84-PWR_CHARGER	2018 06/12	Compal	Downsize	Change the PCB06 and PCB18 to 0.47U_0402	X01
3.	P84-PWR_CHARGER	2018 06/12	Compal	Vendor suggest	Change the PCB11 to 0.33U	X01
4.	P89-PWR_CPU_Stage	2018 06/14	Compal	Downsize	PCA07, PCG09, PCI09, PCI29 change to 0.47U_0402	X01
5.	P92-PWR_VGA_CORE(ISL62771)	2018 06/14	Compal	Downsize	Change PCV30 to 0.15U_0402 Change PCV32 to 0.1U_0402	X01
6.	P86-PWR_1.2V_DDR	2018 07/05	Compal	Factory suggest	Change the PDM01 to SCS00000Z00	X01
7.	P83-BATT_CONN	2018 07/05	Compal	ESD request	Change the PD5,PD6 to SCA00002A00	X01
8.	P84-PWR_CHARGER	2018 07/09	Compal	Modify for AC detect	Change the PRB10 from 47K to 52.3K	X01
9.	P90-PWR_CPU MLCC	2018 07/09	Compal	Change for PI simulat i on	move PCI134,PCI135,PCI136,PCI137,PCI138, PCI139,PCI140 to +VCC_CORE_GT	X01
10.	P84-PWR_CHARGER	2018 07/11	Compal	Factory request	Add PCB71, PCB07 change to 1U_0402	X01
11.	P92-PWR_VGA_CORE	2018 07/17	Compal	Downsize	Change the PCV30 to SE000011G00 0.15U 16V	X01
12.	P88-PWR_CPU	2018 07/17	Compal	Change for CPU EA test	Change the PRZ25, PRZ29 to SD014100380 100K Change the PRZ23 to SD034255200 25.5K	X01

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	PWR P.I.R		
	Size	Document Number	Rev 1.0
	Date: Thursday, June 20, 2019	Sheet 100 of 100	

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					LA-G716P	1.0
				Date:	Thursday, June 20, 2019	Sheet 101 of 101