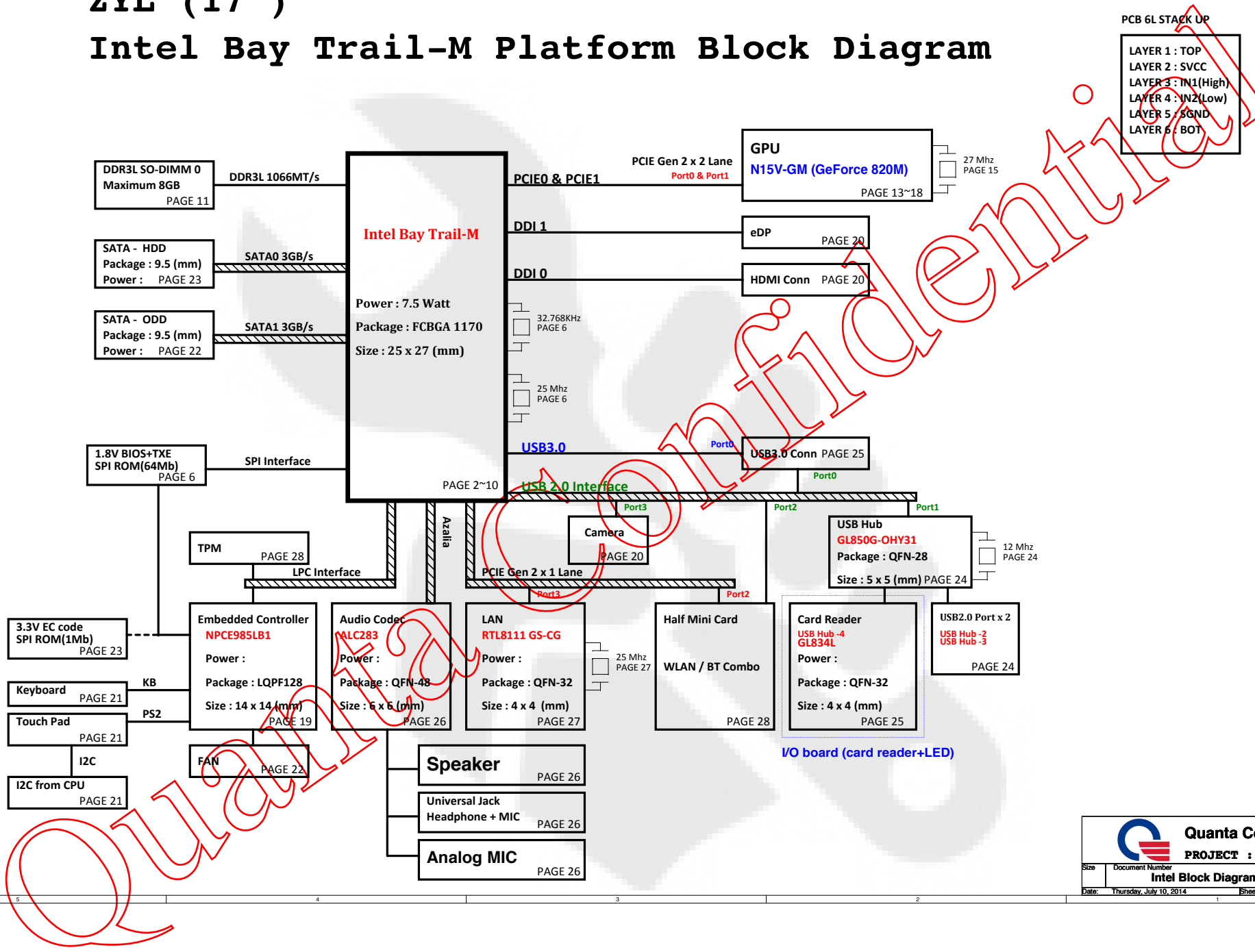
ZYL (17")
Intel Bay Trail-M Platform Block Diagram



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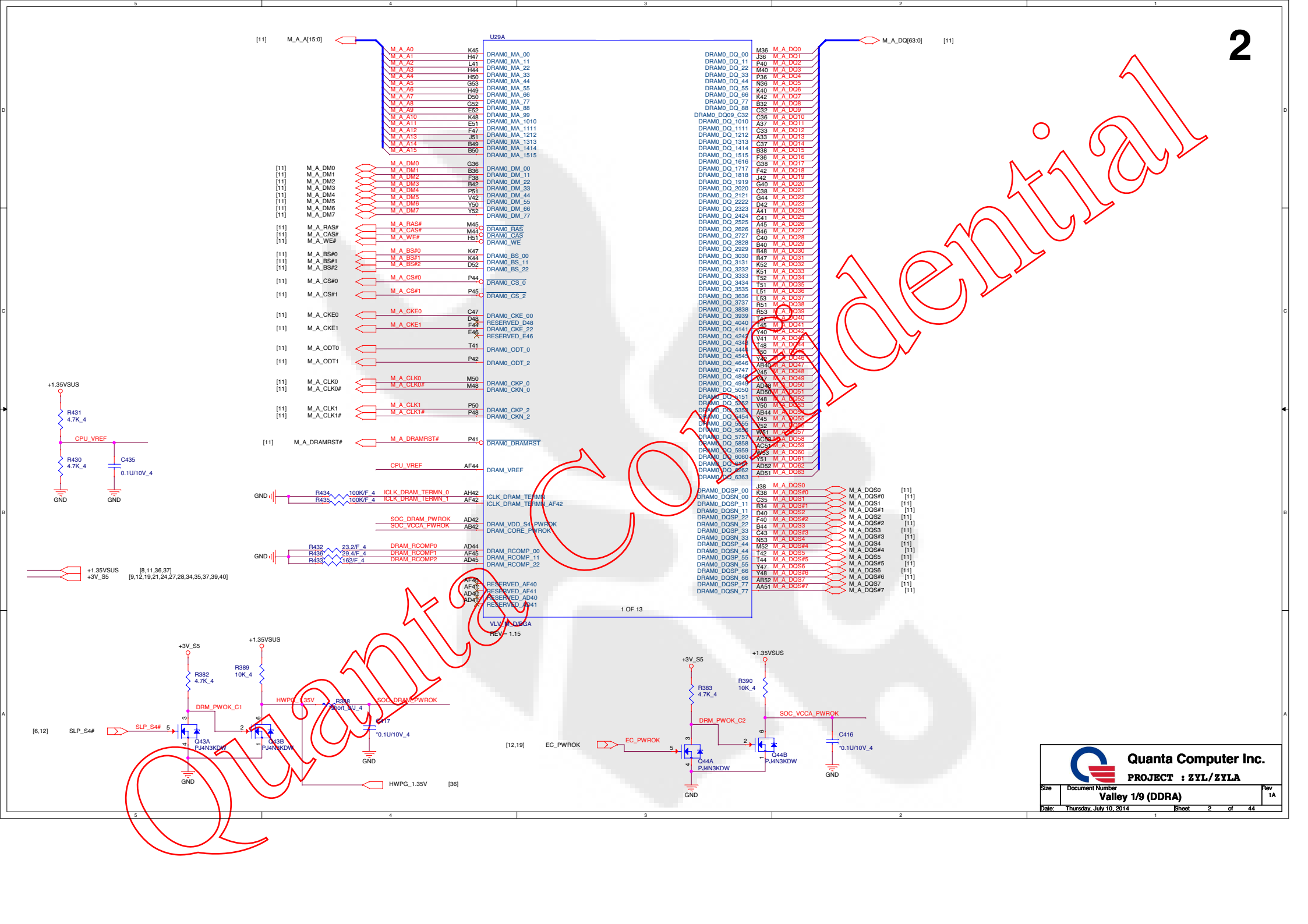
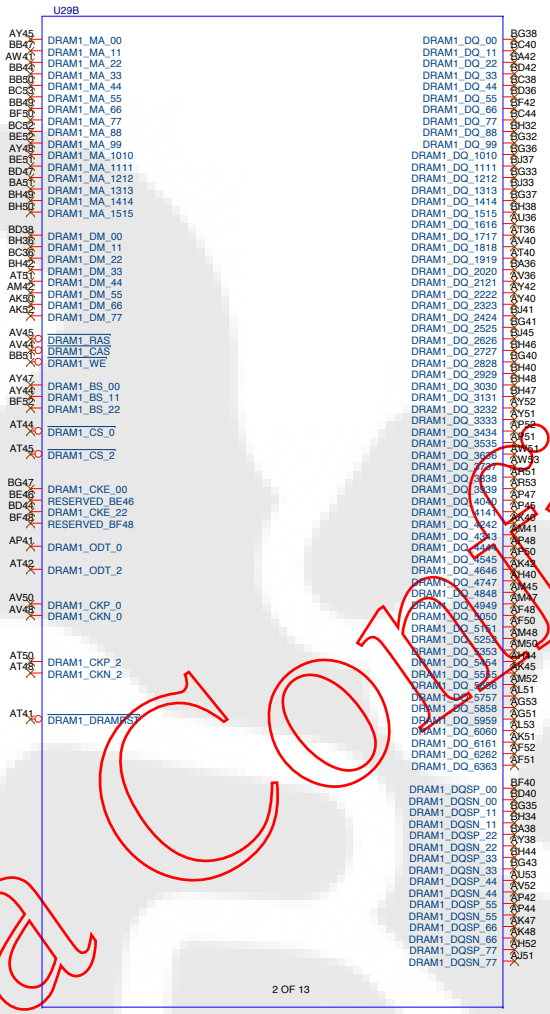
PROJECT : ZYL/ZYLA
Size | Document Number: Intel Block Diagram | Rev 1A
Date: Thursday, July 10, 2014 | Sheet 1 of 44





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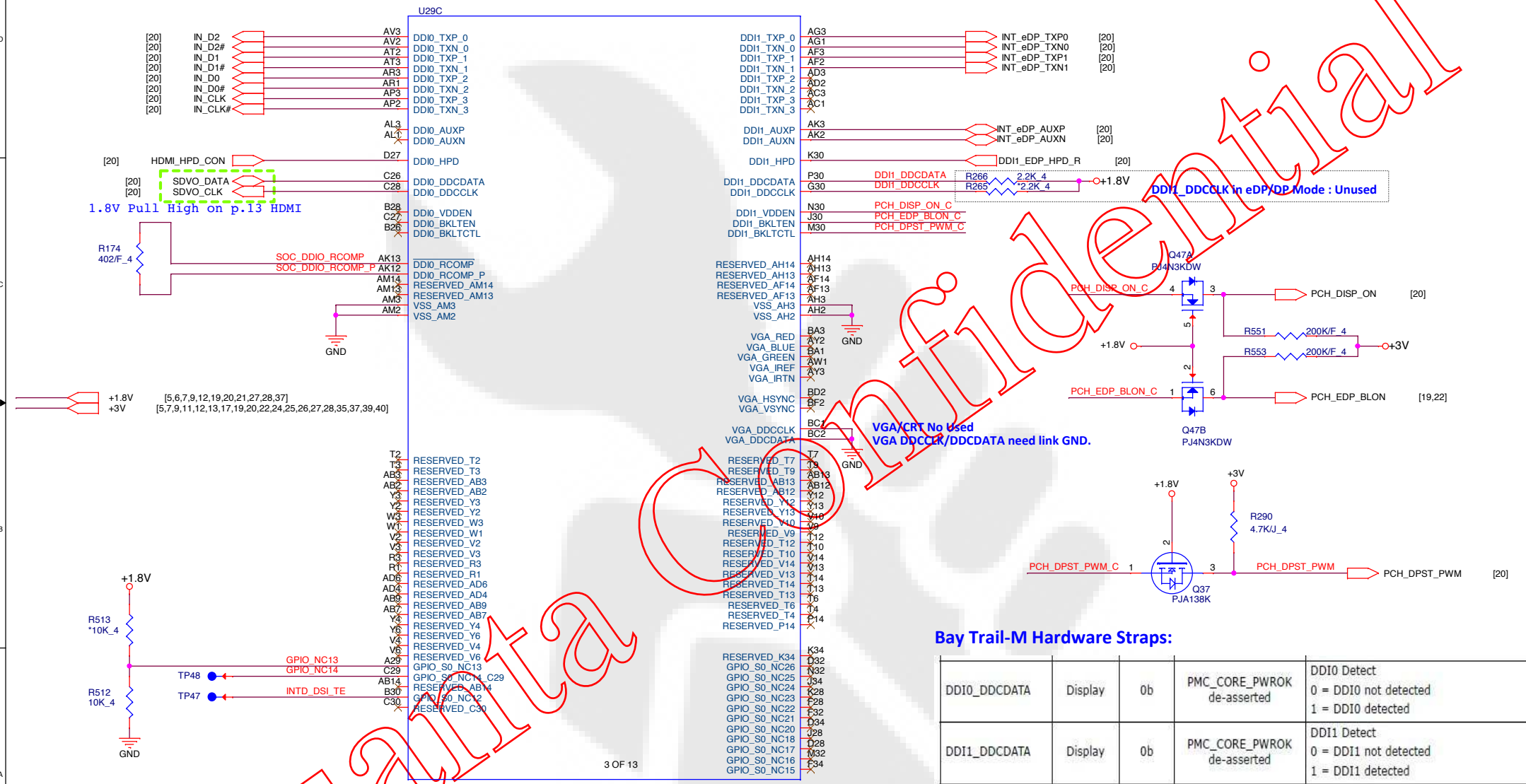
PROJECT : ZYL/ZYLA		
Size	Document Number: Valley 2/9 (DDRB)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 3 of 44	

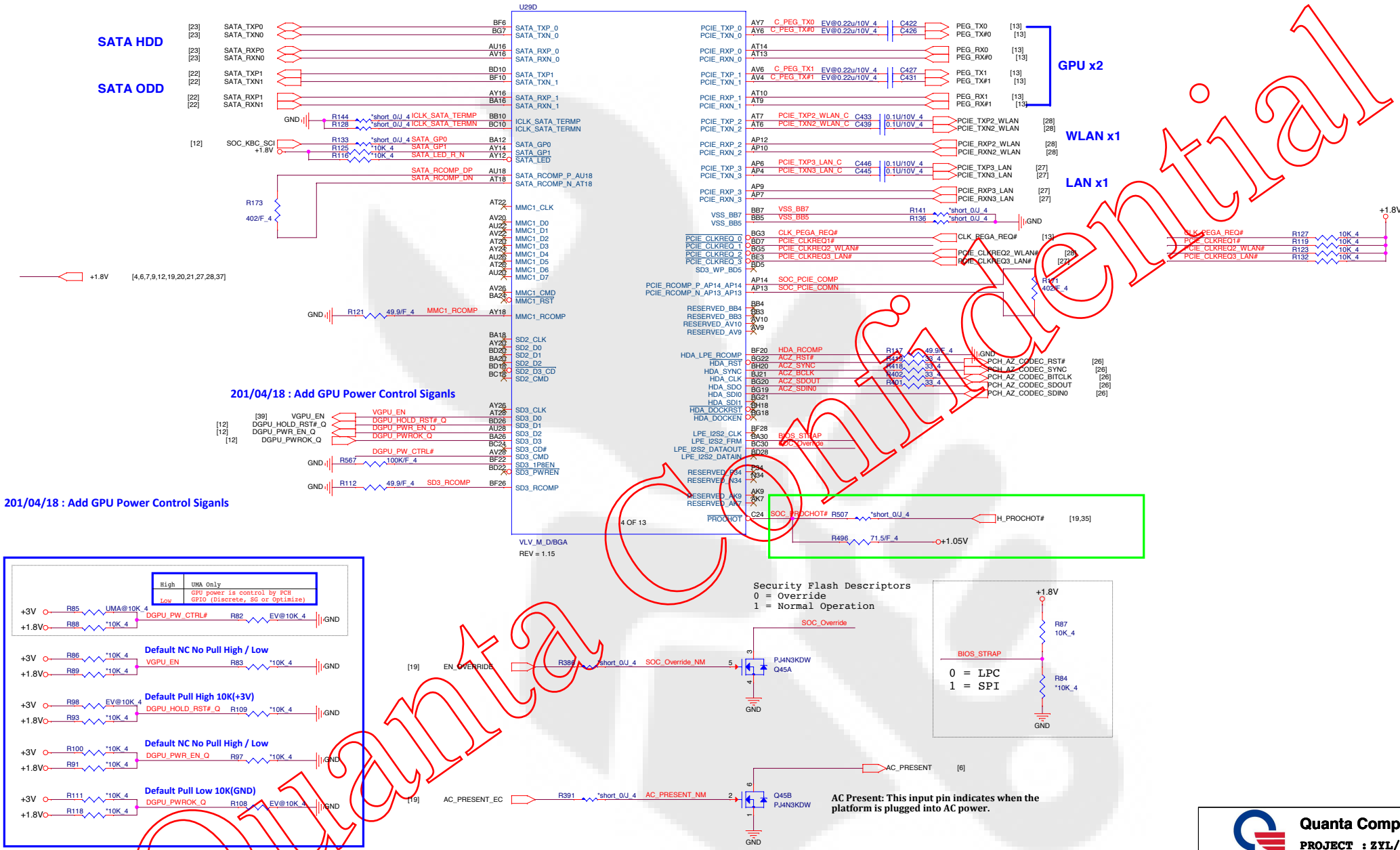


Bay Trail-M Hardware Straps:

DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Valley 3/9 (Display)	1A
Date: Thursday, July 10, 2014	Sheet 4 of 44	



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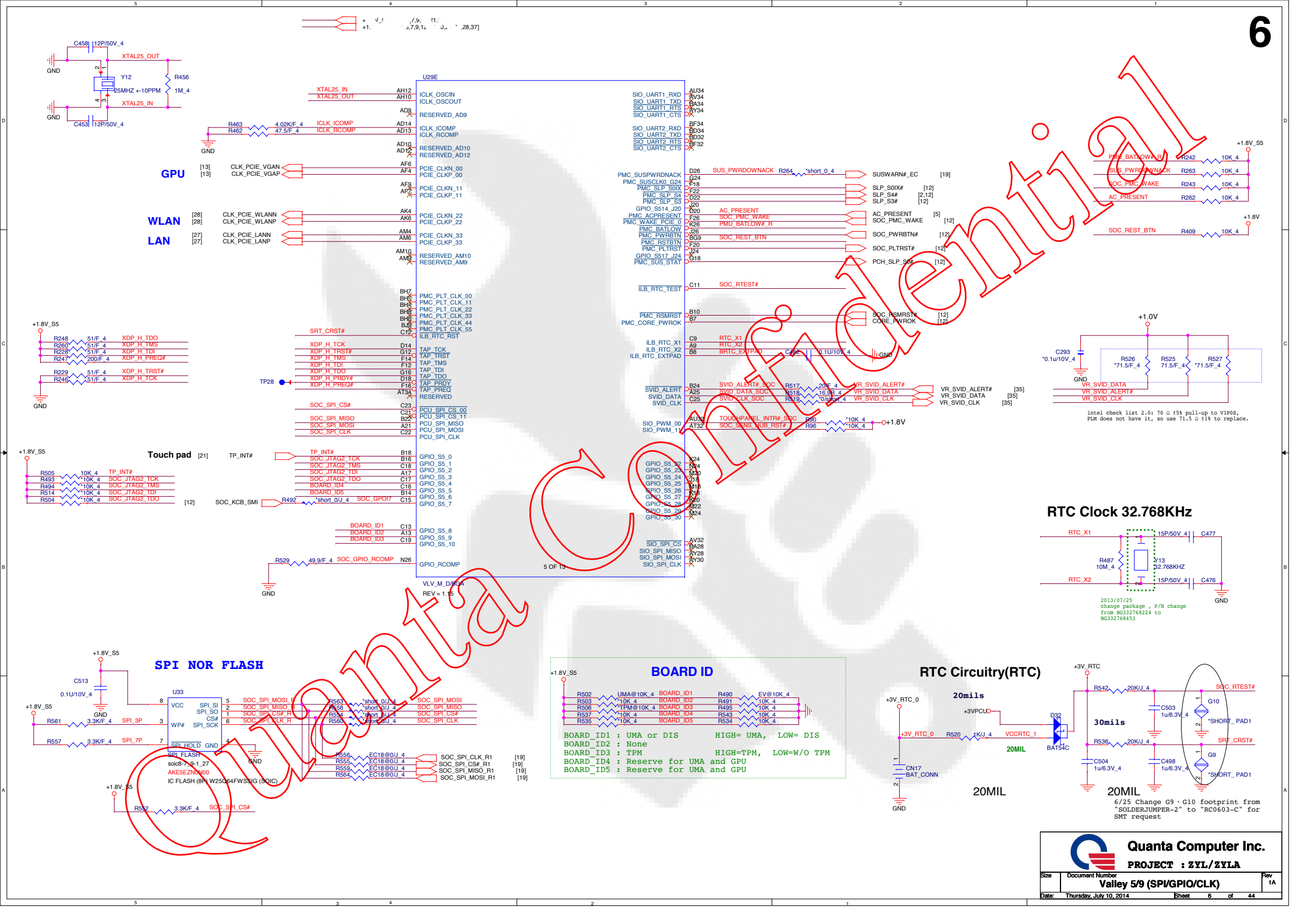
PROJECT : ZYL/ZYLA	
Size	Document Number: Valley 4/9 (SD/PCIE/SATA) — Rev: 1A
Date: Thursday, July 10, 2014	Sheet 5 of 44



Quanta Computer Inc.		
PROJECT : ZYL/ZYLA		
Size	Document Number: Valley 5/9 (SPI/GPIO/CLK)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 6 of 44	

+1.8V_S5 [6,9,12,21,37]
+1.8V [4,5,6,9,12,19,20,21,27,28,37]
+3V [4,5,9,11,12,13,17,19,20,22,24,25,26,27,28,35,37,39,40]

Port 1 is debug port

USB3.0

USB 2.0 HUB

Bluetooth

CAMERA

U29F

GPIO_S5_31
GPIO_S5_32
GPIO_S5_33
GPIO_S5_34
GPIO_S5_35
GPIO_S5_36
GPIO_S5_37
GPIO_S5_38
GPIO_S5_39
GPIO_S5_40
GPIO_S5_41
GPIO_S5_42
GPIO_S5_43

+1.8V_S5 — R475 *10K_4 — SOC_PWR_BUT

USBP0+ [25] / USBP0- [25] — USB_DP0 / USB_DN0
USB_H1_P [24] / USB_H1_N [24] — USB_DP1 / USB_DN1
USBP2+ [28] / USBP2- [28] — USB_DP2 / USB_DN2
USBP3+ [20] / USBP3- [20] — USB_DP3 / USB_DN3

R244 1K_4 — ICLK_USB_TERMN_0
R245 1K_4 — ICLK_USB_TERMN_1
ICLK_USB_TERMN_D10 / ICLK_USB_TERMN

GND [24] SOC_USB_OC0
+1.8V_S5 [25] SOC_USB_OC1
R515 10K_4 / R516 10K_4
USB_OC_00 / USB_OC_11

R219 45.3/F_4 — USB_RCOMP — USB_RCOMPO / USB_RCOMPI
R478 *0/J_4 — USB_PLL_MON

USB_HSIC0_DATA / USB_HSIC0_STROBE
USB_HSIC1_DATA / USB_HSIC1_STROBE

R489 45.3/F_4 — USB_HSIC_RCOMP
R124 49.9/F_4

LPC_RCOMP
LAD0 [19,28] / LAD1 [19,28] / LAD2 [19,28] / LAD3 [19,28] / LFRAME# [19,28]
ILB_LPC_AD_00 / ILB_LPC_AD_11 / ILB_LPC_AD_22 / ILB_LPC_AD_33 / ILB_LPC_FRAME / ILB_LPC_CLK_00 / ILB_LPC_CLK_11 / ILB_LPC_CLKRUN / ILB_LPC_SERIRQ

CLK_24M_KBC [19] — R428 22_4
CLK_TPM [28] — R411 *22_4 (For TPM)
CLK_24M_DEBUG [28] — R427 *22_4
CLKRUN# [19,28] — R429 22_4
SOC_SERIRQ [12,28]
SOC_CLKOUT_0 / SOC_CLKOUT_1 / SOC_CLKRUN# / SOC_SERIRQ

+1.8V — R394 2.2K_4 / R410 2.2K_4 / R426 2.2K_4
SMB_SOC_DATA / SMB_SOC_CLK / SMB_SOC_ALERTB
PCU_SMB_DATA / PCU_SMB_CLK / PCU_SMB_ALERT

Q46 (PJ4N3KDW)
SMB_SOC_DATA 4 — 4.7K_4 R392 — +3V — SMB_RUN_DAT — SMB_RUN_DAT [11,28]
SMB_SOC_CLK 1 — 4.7K_4 R387 — +3V — SMB_RUN_CLK — SMB_RUN_CLK [11,28]

6 OF 13
VLV_M_D/BGA
REV = 1.15

RESERVED_M10 / RESERVED_M9
RESERVED_P7 / RESERVED_P6
RESERVED_M7 / USB3_REXT0 — USB3_P0_REXT — R477 1.24K/F_4 — GND
RESERVED_P10 / RESERVED_P12
RESERVED_M4 / RESERVED_M6
USB3_RXP0 / USB3_RXN0 — USB30_RX1+ [25] / USB30_RX1- [25]
USB3_TXP0 / USB3_TXN0 — USB30_TX1+ [25] / USB30_TX1- [25]
RESERVED_H8 / RESERVED_H7
RESERVED_H5 / RESERVED_H4

Top Swap (A16 Override)
0 = Top address bit is unchanged
1 = Top address bit is inverted

+1.8V — R120 *10K_4 — GPIO_S0_SC_56 / SOC_UART_TX — R113 *10K_4 — GND
GPIO_S0_SC_55 / GPIO_S0_SC_56 / GPIO_S0_SC_57 / GPIO_S0_SC_58 / GPIO_S0_SC_59 / GPIO_S0_SC_60 / GPIO_S0_SC_61
SOC_UART_RX

ILB_8254_SPKR — SPKR [26]

SOC_UART_TX — R126 *0/J_4 — SOC_UART_RX
Un-Stuff for Test Only

SIO_I2C0_DATA / SIO_I2C0_CLK — R420 22/J_4 / R421 22/J_4 — I2C_0_SDA / I2C_0_SCL — [21] [21] **Touch pad**
SIO_I2C1_DATA / SIO_I2C1_CLK — I2C_1_SDA / I2C_1_SCL
SIO_I2C2_DATA / SIO_I2C2_CLK — I2C_2_SDA_R / I2C_2_SCL_R
SIO_I2C3_DATA / SIO_I2C3_CLK — I2C_3_SDA / I2C_3_SCL
SIO_I2C4_DATA / SIO_I2C4_CLK — I2C_4_SDA / I2C_4_SCL
SIO_I2C5_DATA / SIO_I2C5_CLK — I2C_5_SDA / I2C_5_SCL
SIO_I2C6_DATA / SIO_I2C6_CLK — I2C_6_SDA / I2C_6_SCL
GPIO_S0_SC_092 — T10
GPIO_S0_SC_093 — T9
I2C_NFC_SOC_SDA / I2C_NFC_SOC_SCL

+1.8V
I2C_0_SDA — R403 560_4
I2C_0_SCL — R404 560_4
I2C_1_SDA — R422 *560_4
I2C_1_SCL — R405 *560_4
I2C_2_SDA_R — R423 *560_4
I2C_2_SCL_R — R399 *560_4
I2C_3_SDA — R395 *560_4
I2C_3_SCL — R416 *560_4
I2C_4_SDA — R406 *560_4
I2C_4_SCL — R396 *560_4
I2C_5_SDA — R417 *560_4
I2C_5_SCL — R400 *560_4
I2C_6_SDA — R397 *560_4
I2C_6_SCL — R407 *560_4
I2C_NFC_SOC_SDA — R424 *560_4
I2C_NFC_SOC_SCL — R425 *560_4

I2C pull up:
Standard/ Fast Mode --> 560 ohm
Hight speed mode --> CLK- 560 ohm;
DATA- 910 ohm

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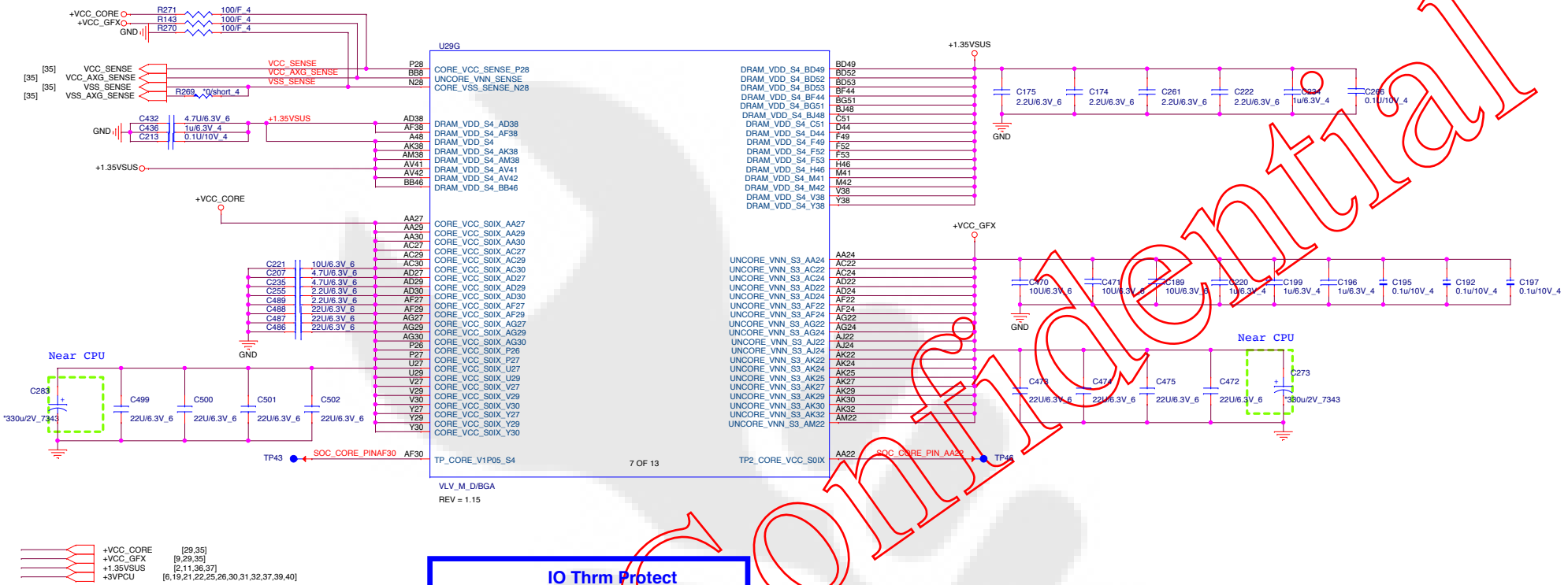
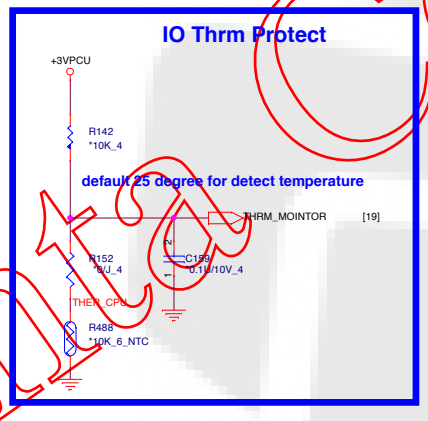
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Valley 6/9 (USB/LPC/I2C)	1A
Date: Thursday, July 10, 2014	Sheet 7 of 44	





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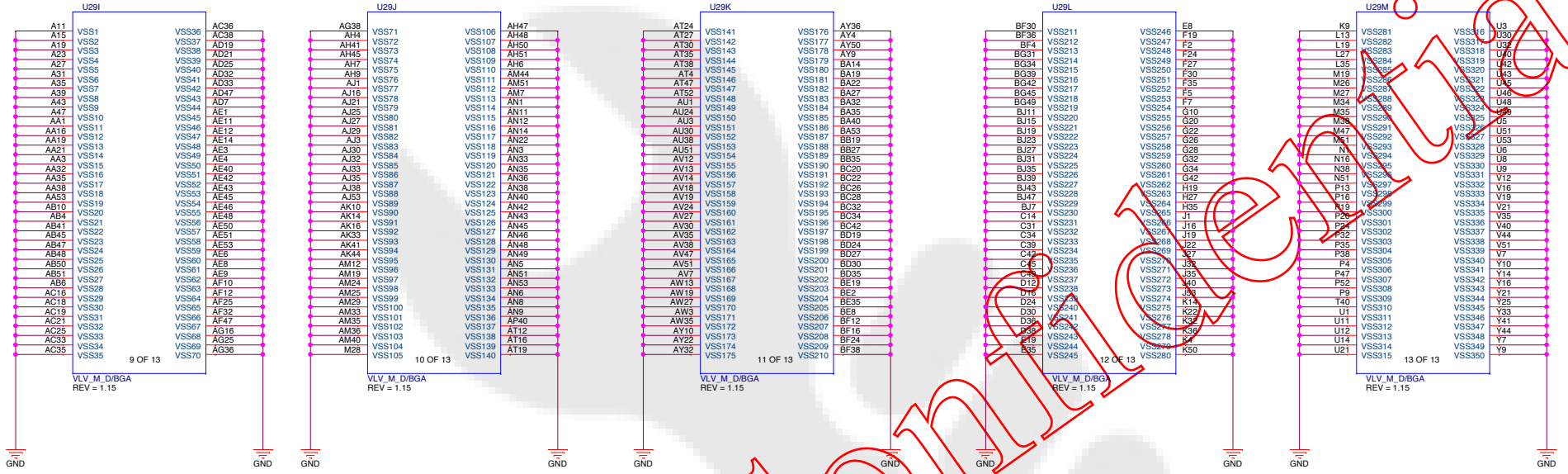
PROJECT : ZYL/ZYLA
Size | Document Number: Valley 7/9 (Power 1) | Rev: 1A
Date: Thursday, July 10, 2014 | Sheet 8 of 44

Quanta Computer Inc.		
PROJECT : ZYL/ZYLA		
Size	Document Number: Valley 8/9 (Power 2)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 9 of 44	



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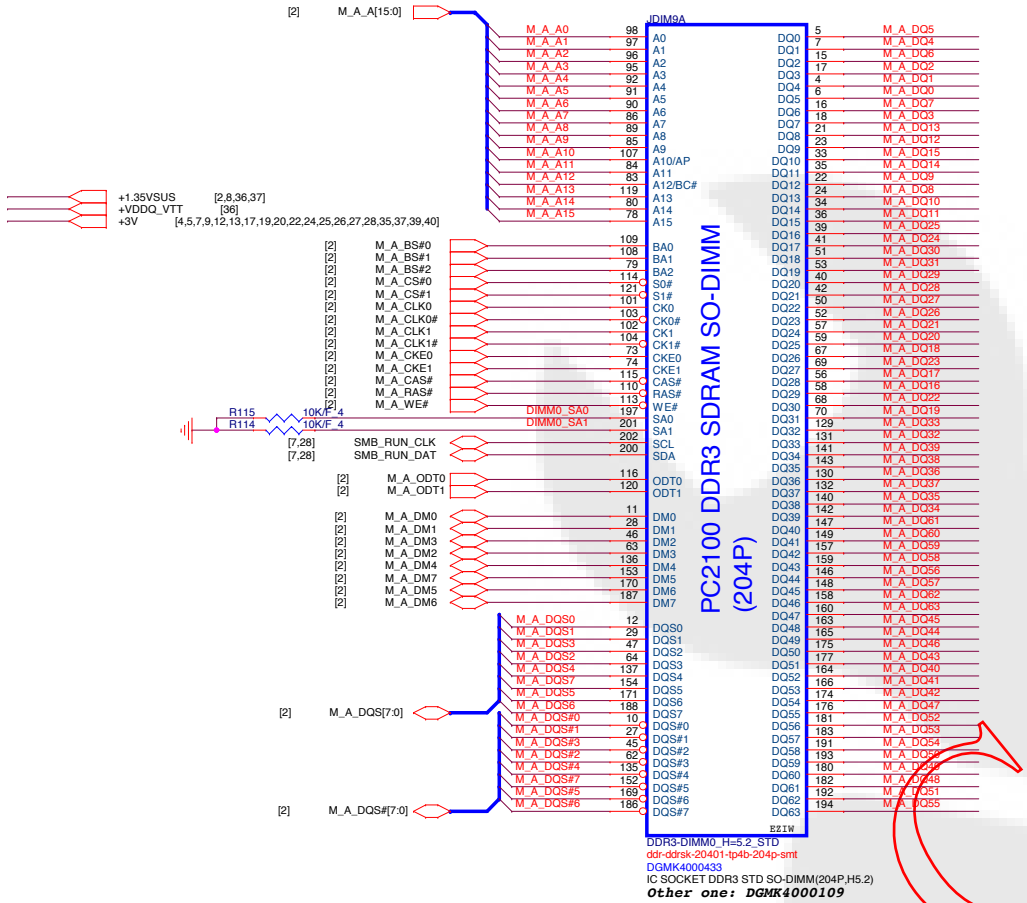
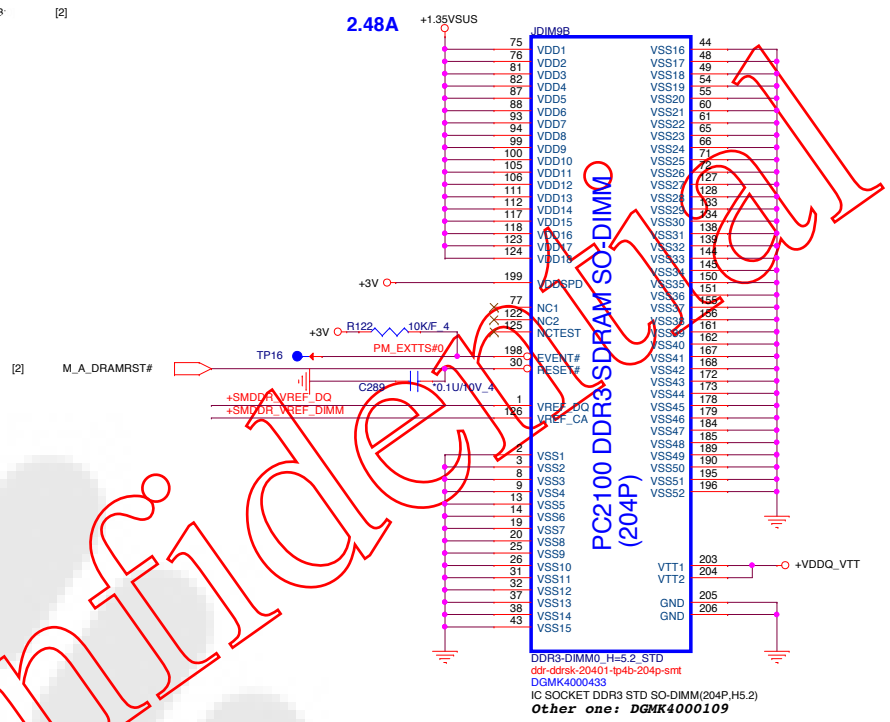
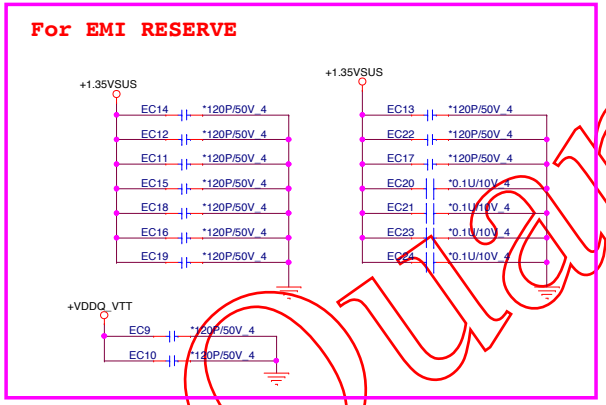
PROJECT : ZYL/ZYLA
Size | Document Number: Valley 9/9 (GND) | Rev: 1A
Date: Thursday, July 10, 2014 | Sheet 10 of 44

Address A0H



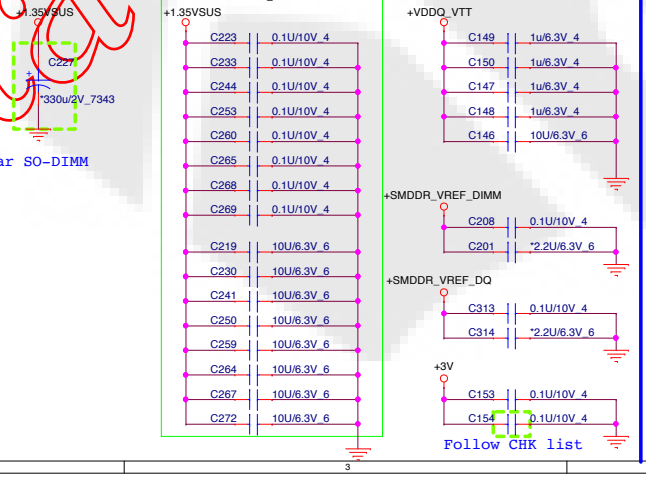


For EMI RESERVE

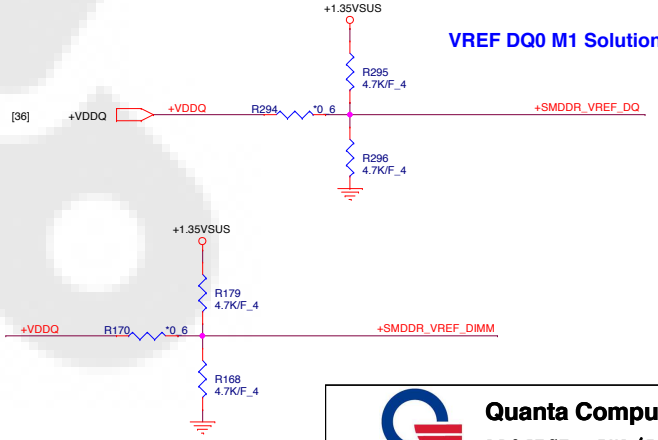


Place these Caps near So-Dimm0.

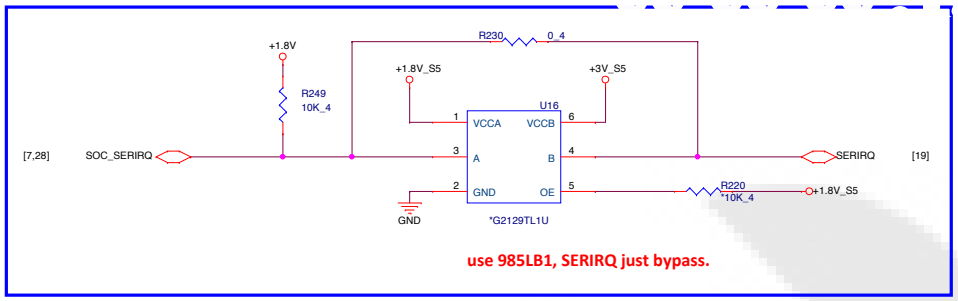
0.1uF/10uF 4pcs on each side of connector

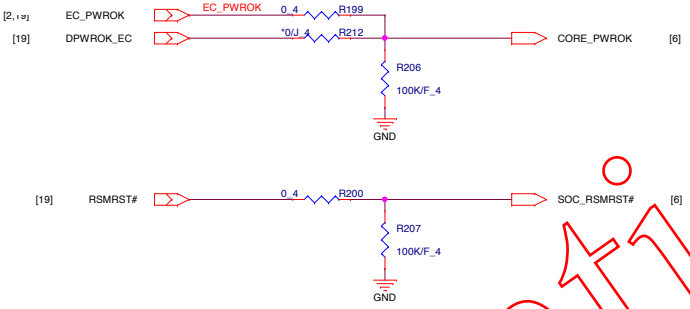


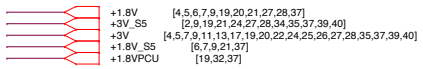
VREF DQ0 M1 Solution

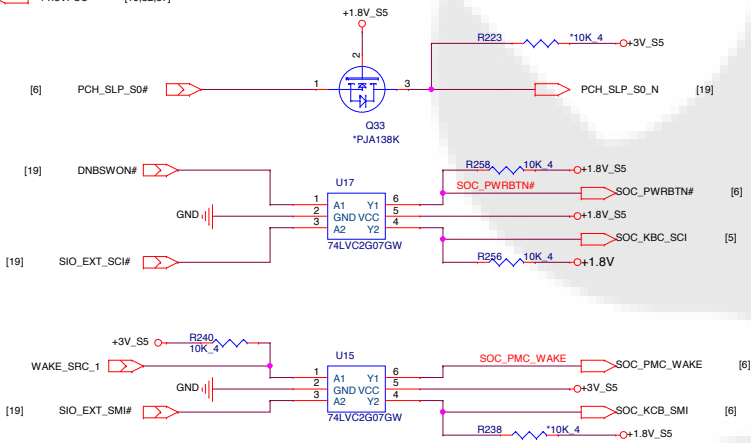


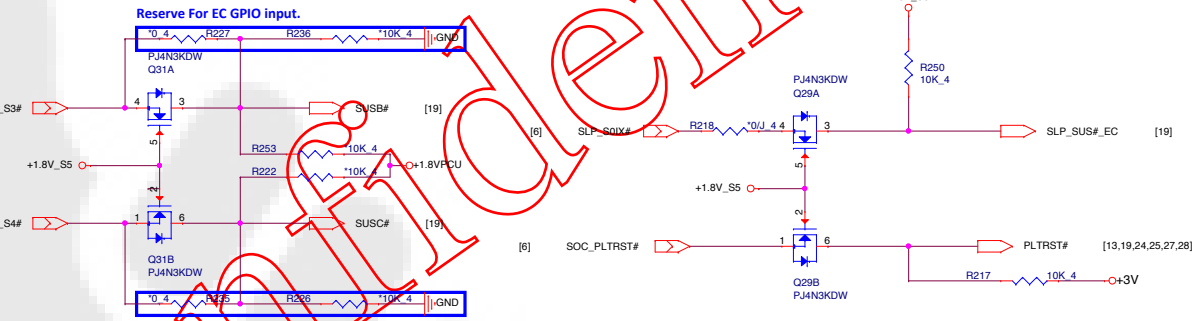
Quanta Computer Inc.			
PROJECT : ZYL/ZYLA			
Size	Document Number		Rev
	DDR3 DIMM0-STD(5.2H)		1A
Date: Thursday, July 10, 2014		Sheet 11 of 44	

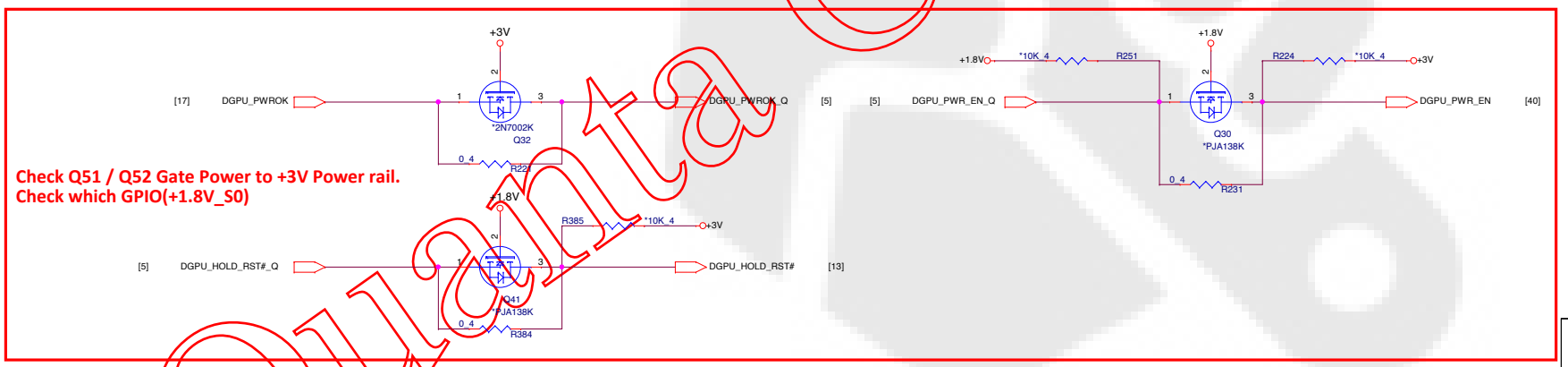












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PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Level Shfiter	1A
Date: Thursday, July 10, 2014	Sheet 12 of 44	

<VGA>

1000mA

2500mA

210mA of +3V_GFX

PLACE UNDER GPU BALLS

PLACE NEAR GPU

4.7uF x 15 population x10

0.1uF x 8 population x 4

Follow Z09 to isolate CLK_REQ#

not GC6 2.0 unstuff resistor

for meet Power down sequence for +3V_GFX

No stuff D8 when GC6 support.

8mils width (0.2MM)

PEX_PLLVDD : 0.3MM = 12mils (150mA)
RSVD R1 and C1 for GV2 co-layout sDDR3

PEX_RST timing

PCH control PEGX_RST#

Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	

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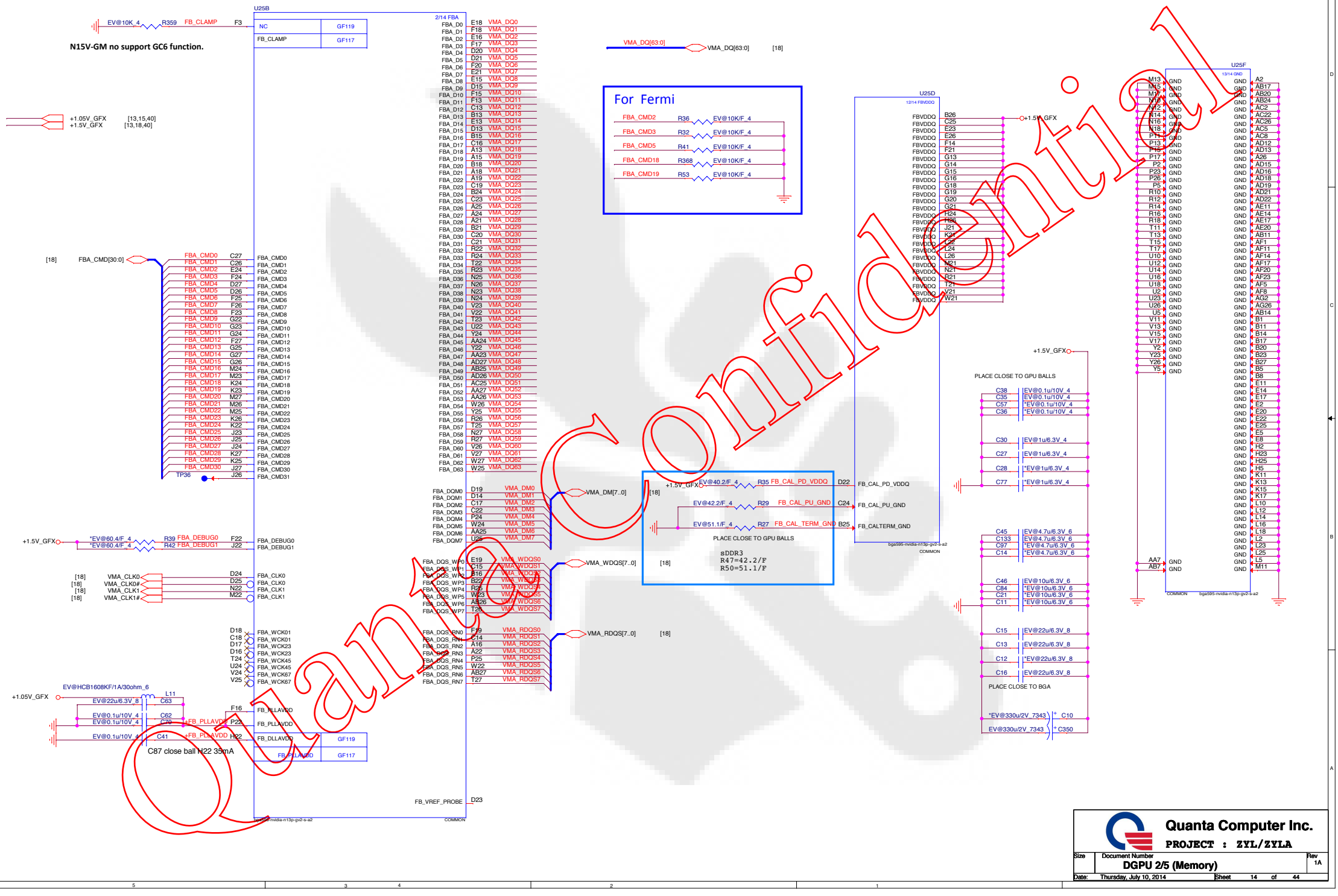
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	DGPU 1/5 (PEG)	1A

Date: Thursday, July 10, 2014 Sheet 13 of 44



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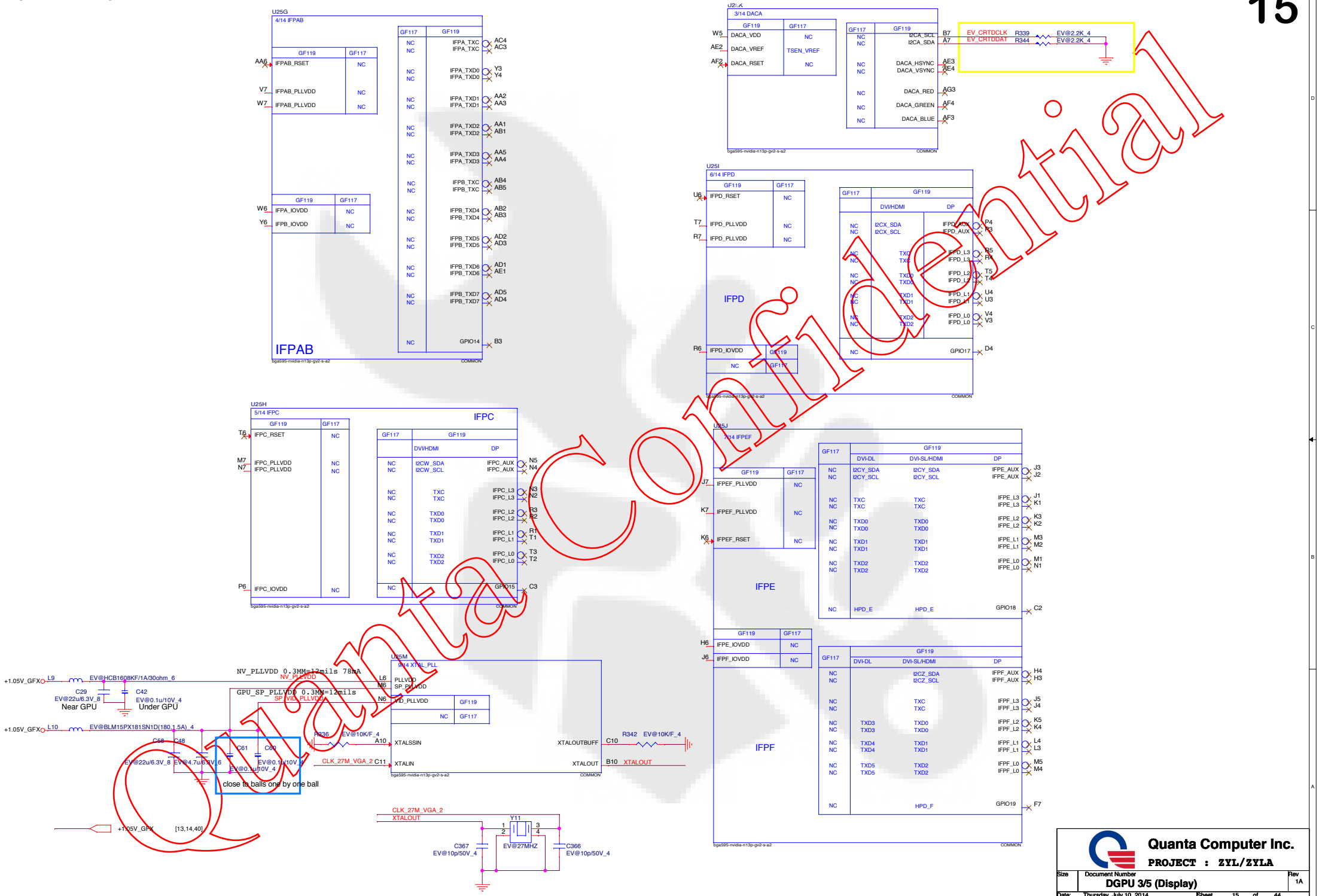
PROJECT : ZYL/ZYLA		
Size	Document Number: DGPU 2/5 (Memory)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 14 of 44	



<VGA>

U25L

R3

R362 *EV@40.2K/F_4 N15V-GM NC

R38 *EV@40.2K

R34 *EV@40.2K

+3V_GFX [13,17,40]
+3V_MAIN [13,17]

U25N

I2CS Slave Address= 0x9E (default)

TP39

GPIO8 VGA thrmtrip# => inform EC over temperature protect

GPIO12_ACIN
GPIO12 AC detect
AC high
DC low

SMBus(VGA)

VGA/VGA

EC/S5

For N15V-GM-B SKU:
Device ID=0x1140
R3= N.C.
1.ROM_SCLK =10K pull down.
2.ROM_SI= 10k pull down
3.ROM_SO= 10k pull down
4.Strap3~0 = RVL memory binary mode setting.
5.Strap4 =10k pull down

Vendor	Vendor P/N	Strap0	Strap1	Strap2	Strap3	
HYNIX	HT5C4G63AFR-11C	0	0	1	0	
MICRON	MT41J256M16HA-093G:E	1	0	1	1	
SAMSUNG	K4W4G164D-BC1A	1	0	0	1	Default

N15V-GM: Stuff 10K pull down

STRAP0~3:

N15V-GM: Stuff 10K

N15V-GM:Memory strap setting Please follow N15x latest RVL "RVL-06891-001".

N15V-GM VRAM Configuration Table:

	Strap [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N
4Gb	0100 (0x4) 1101 (0xD) 1001 (0x9)	DDR3 256MBx16,1000MHz DDR3 256MBx16,1000MHz DDR3 256MBx16,1000MHz	HYNIX MICRON SAMSUNG	H5TC4G63AFR-11C MT41J256M16HA-093G:E K4W4G1646D-BC1A	

STRAP3
Optimus ---> 4.99k PD

Resistor P/N
10K ---> CS31002FB26

Vendor P/N	820M		QCI P/N
N15V-GM-B-A2	GeForce 820M	0x1140	AJ0N15V0T03

Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	DGPU 4/5 (MIO/GPIO)	1A

Date: Thursday, July 10, 2014 Sheet 16 of 44

+3V_GFX [13,16,40]
+3V_MAIN [13,16]
+3V [4,5,7,9,11,12,13,19,20,22,24,25,26,27,28,35,37,39,40]

+3V_GFX
60mil
R10
EV@0_8
60mil
+3V_MAIN
N15V stuff not support GC6.

[12] DGPU_PWROK
R64
EV@100K_4
U10
EV@TC7SH08FU
+3V
C127
EV@0.1u/10V_4
R65
*short_4
GPU_PWR_GD
HWPG_1.5VGFX [40]
GPU_PWR_GD [39]
*EV@0_4
R63

+3V_GFX
+3V
R16
EV@4.7K_4
R12
EV@4.7K_4
3V_MAIN_PWGD [39,40]
+3V_MAIN
R9
EV@4.7K_4
C17
*EV@1000p/50V_4
Q10
EV@MMBT3904-7-F
C18
EV@1000p/50V_4
Q12
EV@DTC144EU
R17
EV@100K/F_4
+1.05V_GFX and GPU core power EN

For N15V-GM no Support GC6 Stuff R1299
[40] FBVDDQ_EN
EV@0_4
R62
GPU_PWR_GD
R61
EV@100K_4
C122
*EV@0.1u/10V_4
PD at GPU power side

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PROJECT : ZYL/ZYLA
Size | Document Number: DGPU 5/5 (Power/Ground) | Rev: 1A
Date: Thursday, July 10, 2014 | Sheet 17 of 44

CHANNEL A: 2048MiB DDR3X16

+1.05V_GFX [13,14,15,40]

[14] VMA_DQ[63..0]
[14] VMA_DM[7..0]
[14] VMA_WDQS[7..0]
[14] VMA_RDQS[7..0]

VRAM9 / VRAM11 / VRAM10 / VRAM12

96-BALL SDRAM DDR3
EV@VRAM _DDR3_HYNIX_256MX16

Should be 240 Ohms +-1%

R33 EV@243/F_4
R358 EV@243/F_4
R50 EV@243/F_4
R365 EV@243/F_4

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

VMA_CLK0 — R31 EV@162/F_4 — VMA_CLK0#

R360 EV@1.33K/F_4 — VREFC_VMA1 — C372 EV@0.1u/10V_4 — R361 EV@1.33K/F_4
R23 EV@1.33K/F_4 — VREFD_VMA1 — C26 EV@0.1u/10V_4 — R26 EV@1.33K/F_4

[14] FBA_CMD17 — TP11
[14] FBA_CMD1 — TP35
10/14 modify

VMA_CLK1 — R58 EV@162/F_4 — VMA_CLK1#

R47 EV@1.33K/F_4 — VREFC_VMA3 — C96 EV@0.1u/10V_4 — R44 EV@1.33K/F_4
R371 EV@1.33K/F_4 — VREFD_VMA3 — C386 EV@0.1u/10V_4 — R370 EV@1.33K/F_4

+1.5V_GFX decoupling:
C139 C393 C121 C384 EV@1u/10V_4
C34 C404 C371 C381 C365 C23 EV@1u/10V_4
C362 C364 C390 C124 C37 C113 C24 C368 EV@1u/10V_4
C400 C128 C363 C370 C403 C369 C114 EV@0.1u/10V_4
C20 C361 C383 C115 C25 EV@0.1u/10V_4

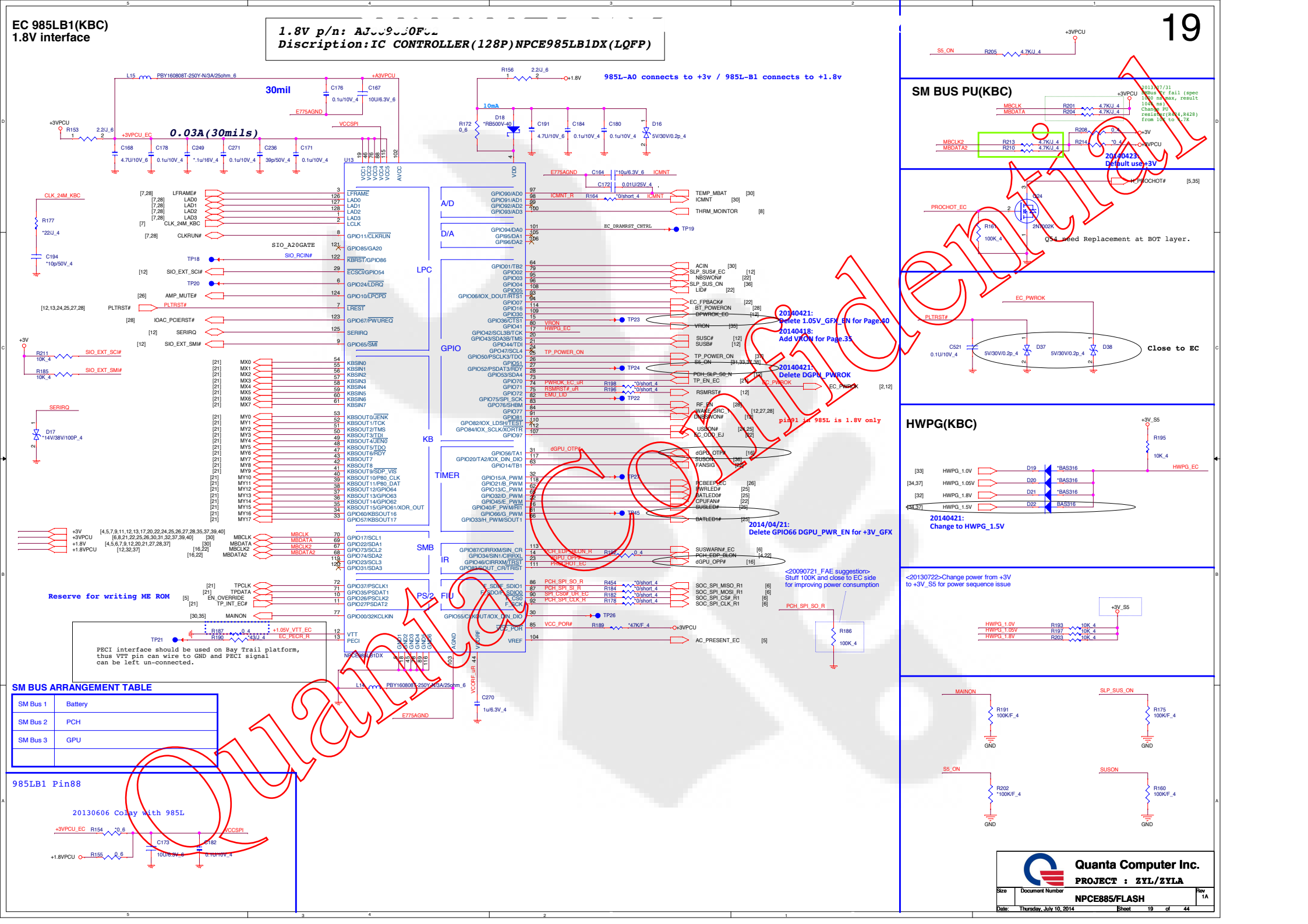
Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	N15P- DDR3 VRAM 1/2	1A

Date: Thursday, July 10, 2014 Sheet 18 of 44

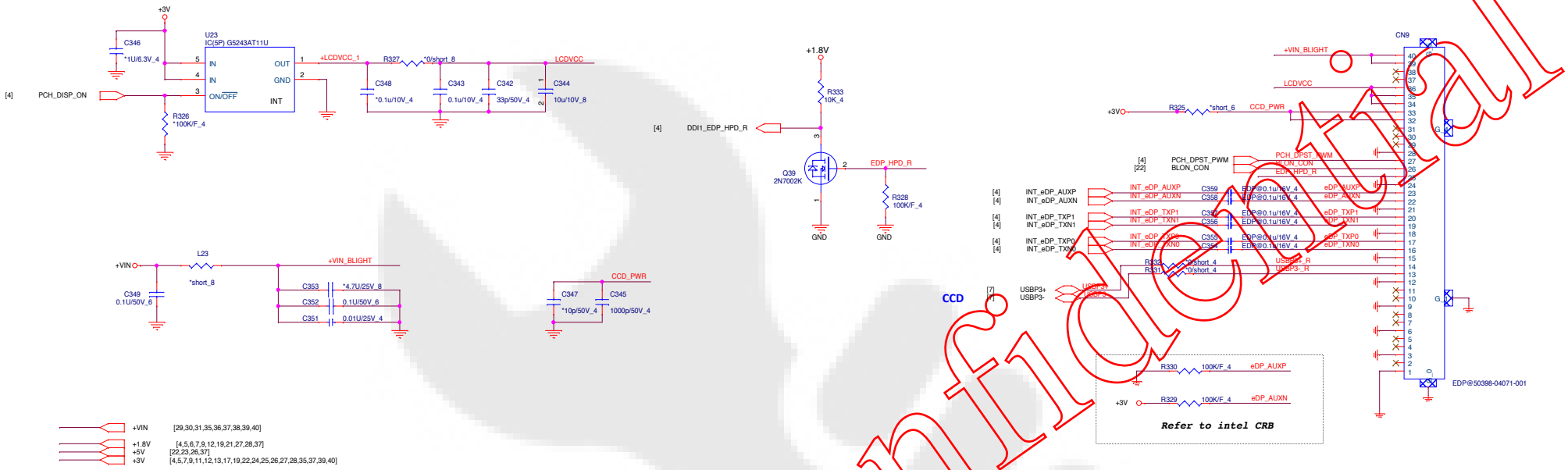
EC 985LB1(KBC)
1.8V interface

1.8V p/n: AJ009J0FC2
Discription:IC CONTROLLER(128P)NPCE985LB1DX(LQFP)

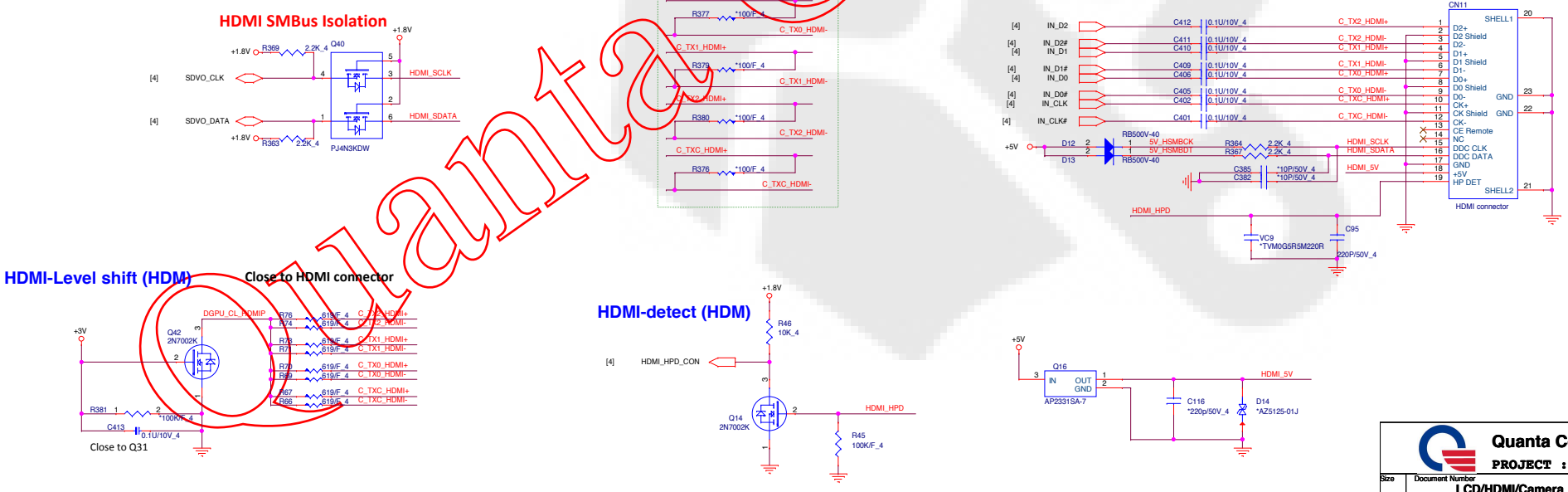


Quanta Confidential

EDP Conn.

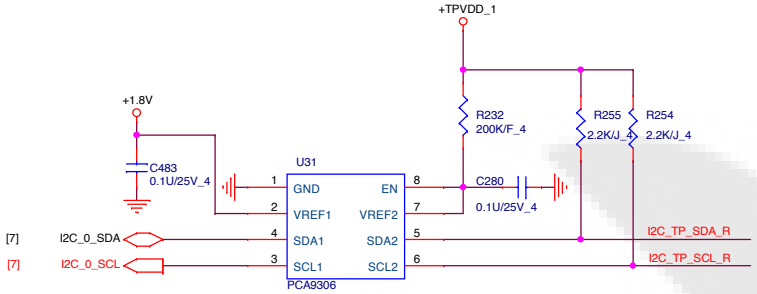


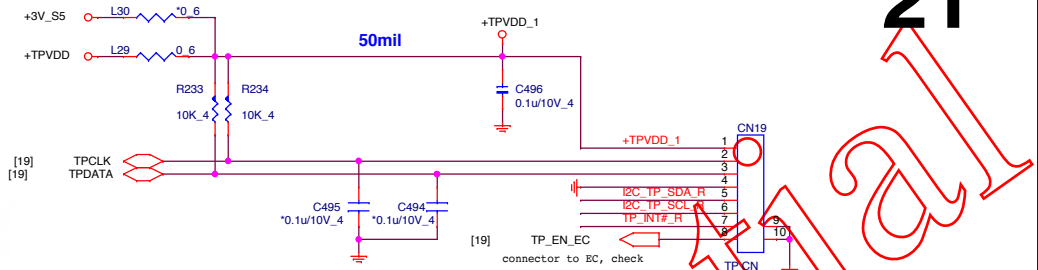
HDMI Conn.

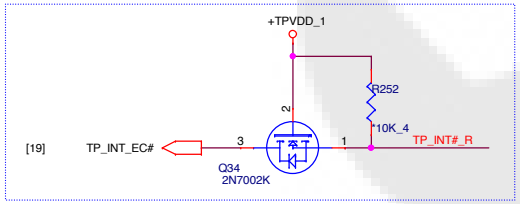


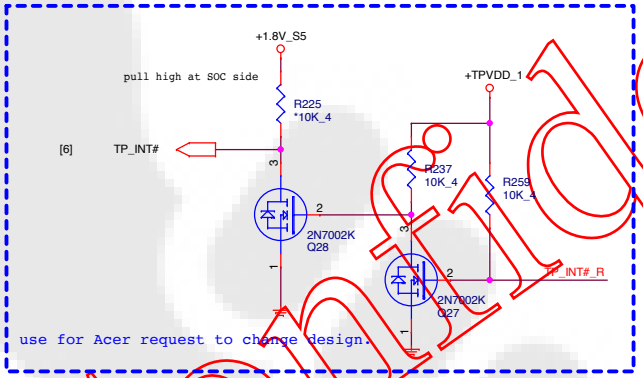
Quanta Computer Inc.		
PROJECT : ZYL/ZYLA		
Size	Document Number: LCD/HDMI/Camera	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 20 of 44	

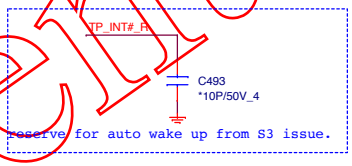
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



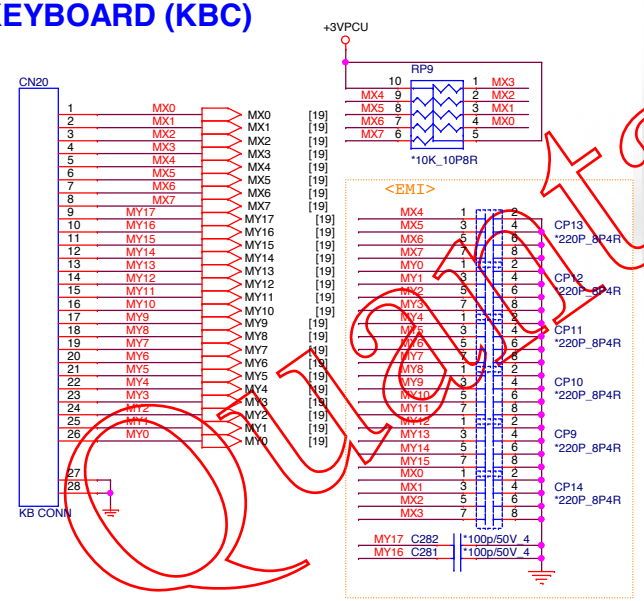


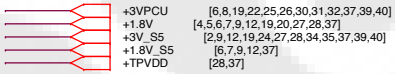






KEYBOARD (KBC)

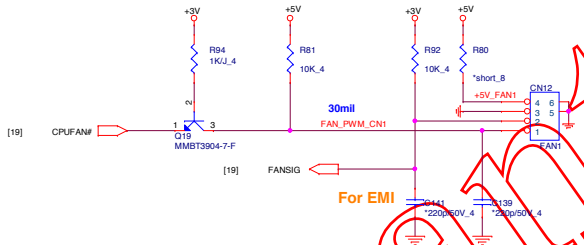




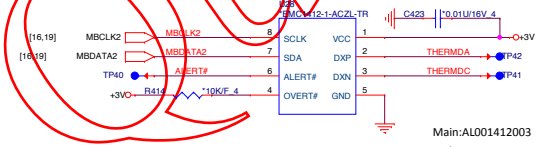
Quanta Computer Inc.
PROJECT : ZYL/ZYLA
Size | Document Number: KB/BT/TP/LED/Power Connector | Rev: 1A
Date: Thursday, July 10, 2014 | Sheet 21 of 44

SATA ODD Connector

CPU FAN CTRL(THM)



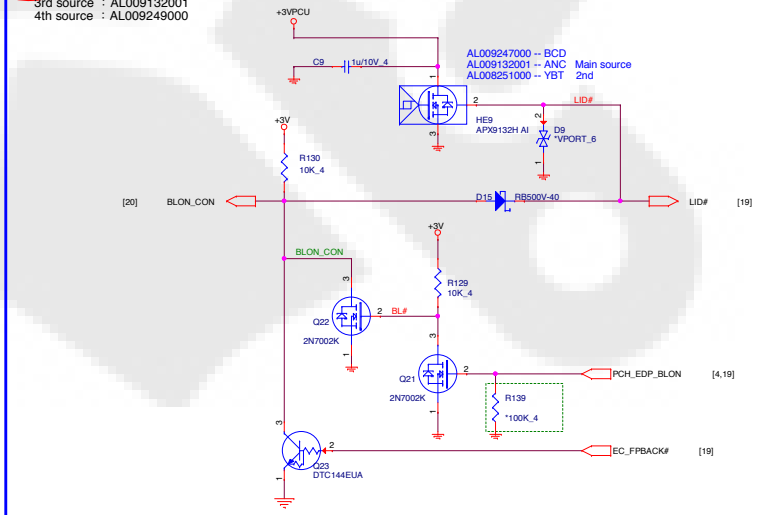
CPU Thermal sensor(THS) / MB Local TEMP



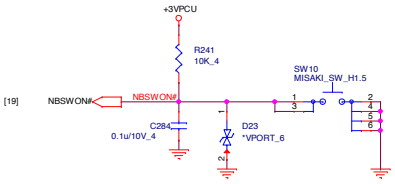
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

HALL IC (HSR)

1st source : EOD
2nd source : AL008251000 -- YBT
3rd source : AL009132001
4th source : AL009249000



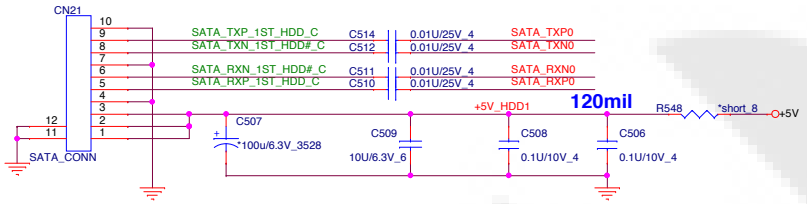
Power Switch. (FSW)



Quanta Computer Inc.		
PROJECT ZYL/ZYLA		
Size	Document Number: ODD/FAN/Hall/PSW	Rev 1A
Date: Thursday, July 10, 2014	Sheet 22 of 44	

SATA HDD1

HDD1



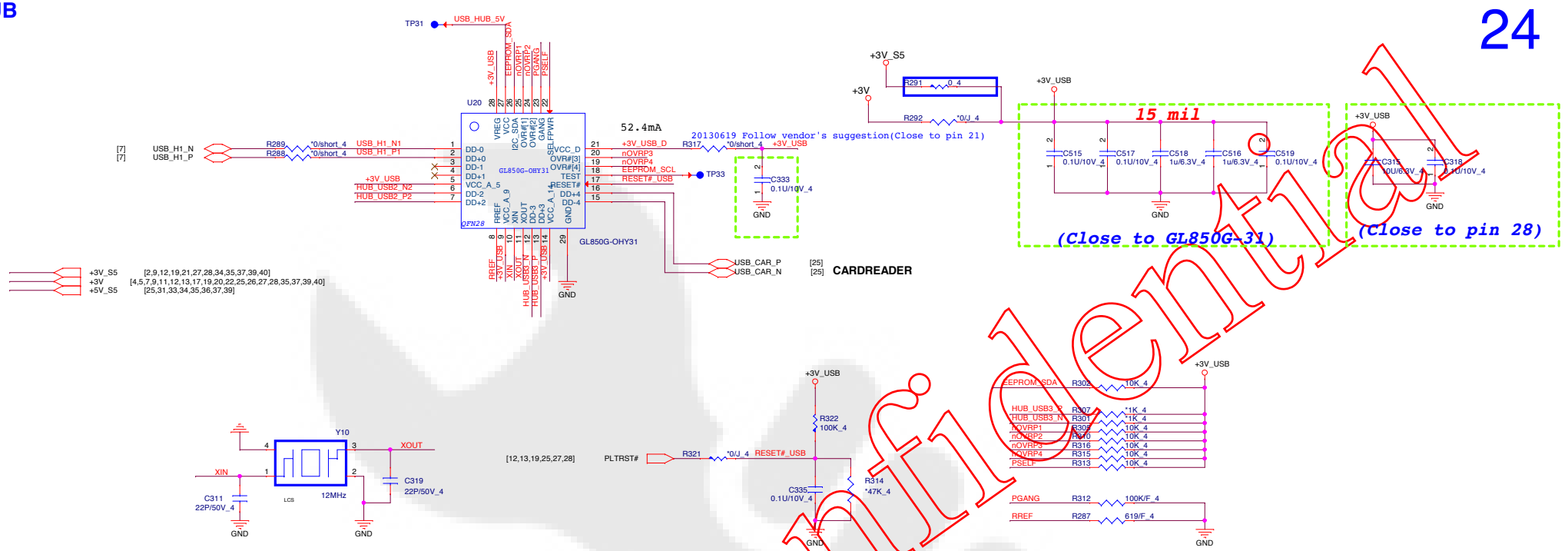
[5] SATA_TXP0 → SATA_TXP0
[5] SATA_TXN0 → SATA_TXN0

[5] SATA_RXN0 → SATA_RXN0
[5] SATA_RXP0 → SATA_RXP0

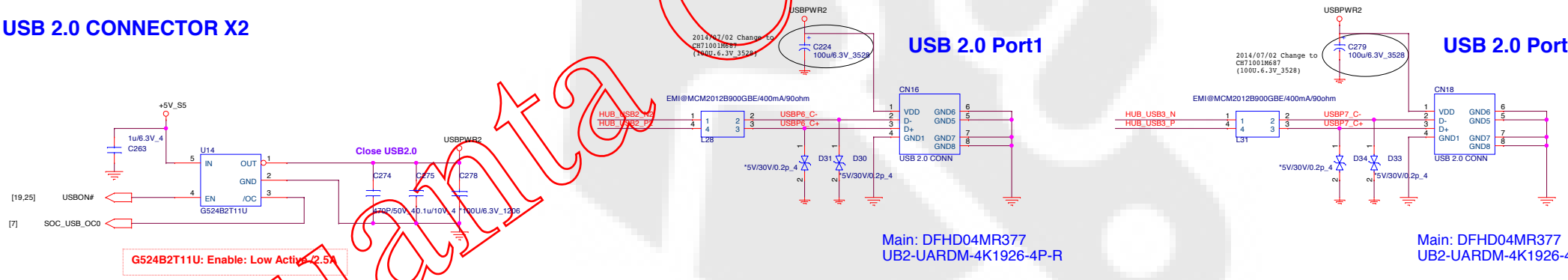
+5V [20,22,26,37]
+1.5V [9,22,26,34]

Quanta Computer Inc.		
PROJECT : ZYL/ZYLA		
Size	Document Number: SATA HDD/SATA REDRIVER	Rev 1A
Date: Thursday, July 10, 2014	Sheet 23 of 44	

USB HUB

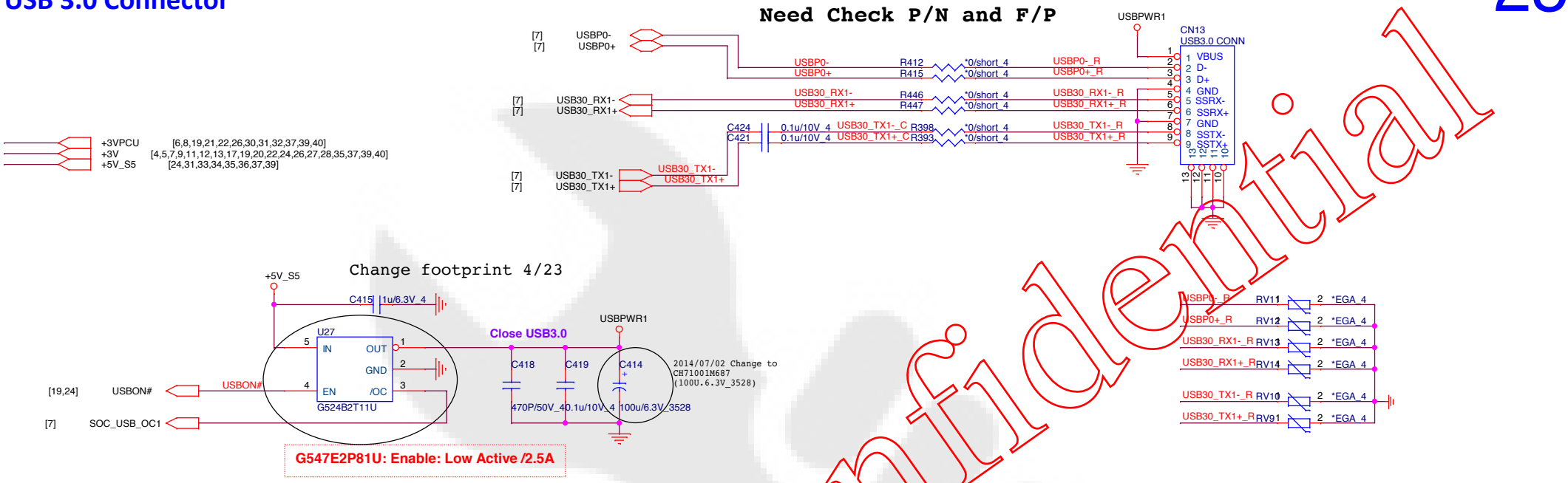


USB 2.0 CONNECTOR X2

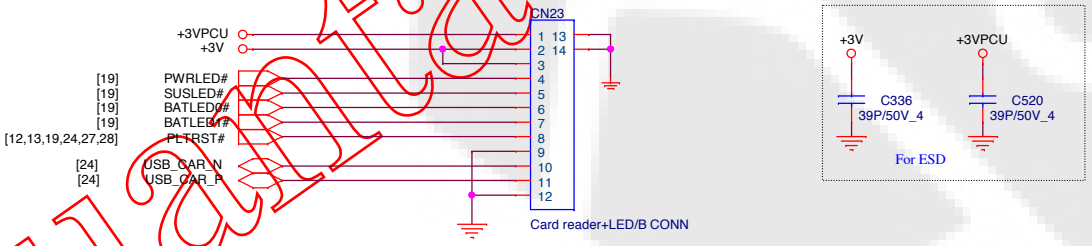


Quanta Computer Inc.
PROJECT : ZYL/ZYLA
Size | Document Number: USB BOARD CONN | Rev 1A
Date: Thursday, July 10, 2014 | Sheet 24 of 44

USB 3.0 Connector

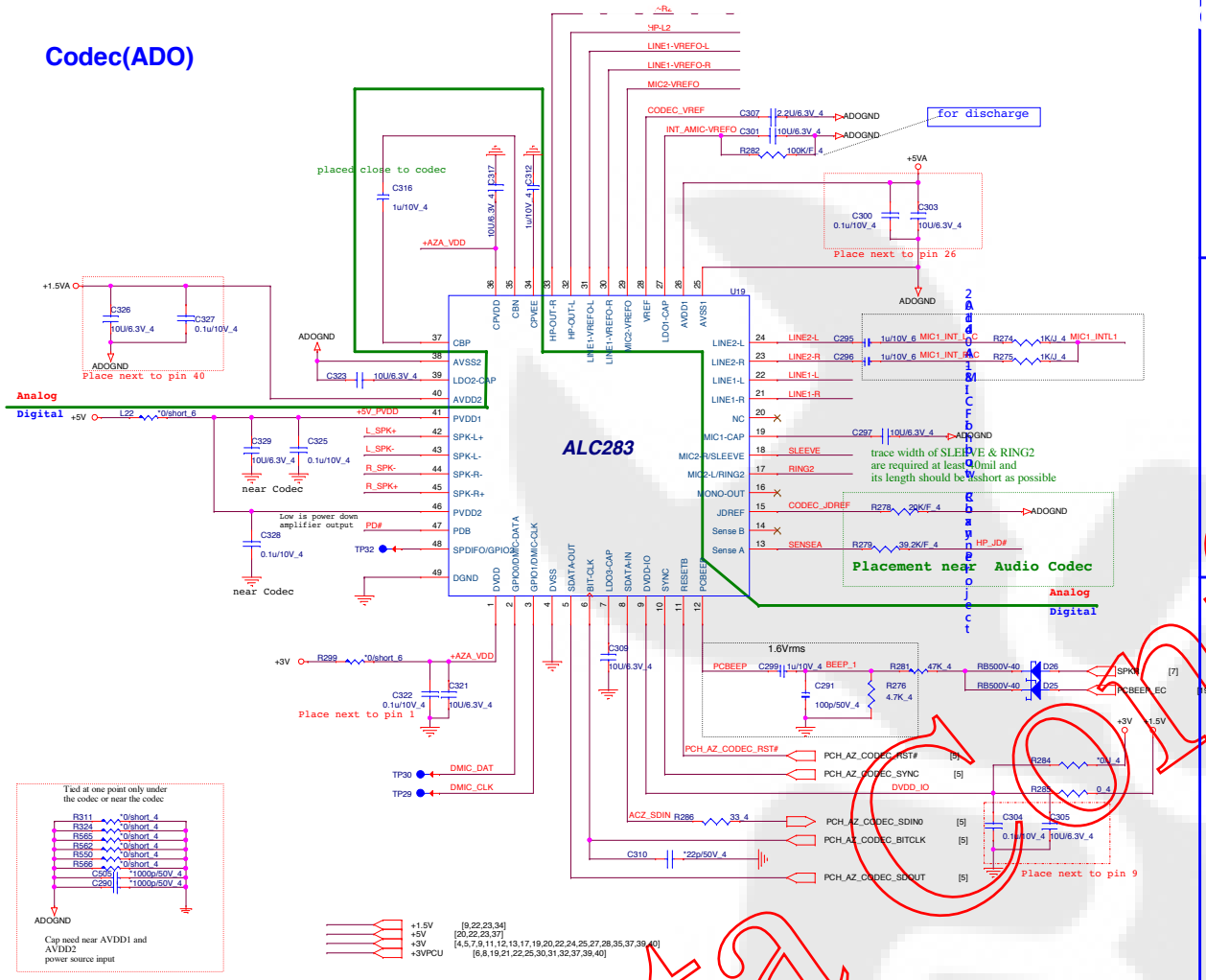


Card Reader+ LED/B Connector



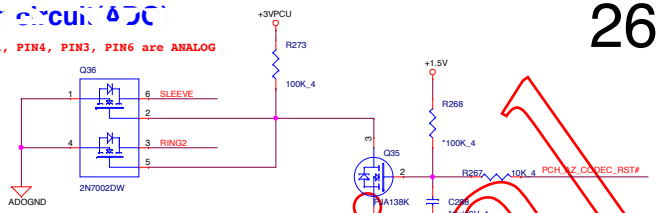
Quanta Computer Inc. PROJECT : ZYL/ZYLA		
Size	Document Number: USB 3.0 / Card Reader+LED CONN	Rev 1A
Date: Thursday, July 10, 2014	Sheet 25 of 44	

Codec(ADO)

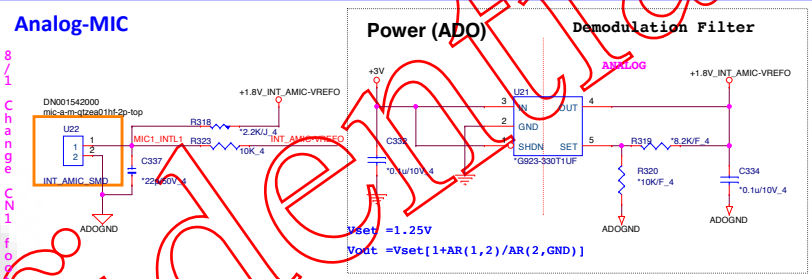


Ground circuit(ADO)

PIN1, PIN4, PIN3, PIN6 are ANALOG



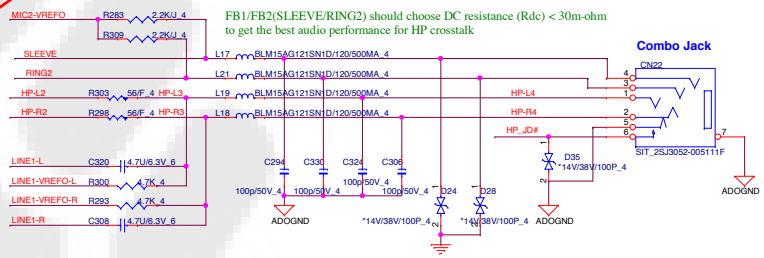
Analog-MIC



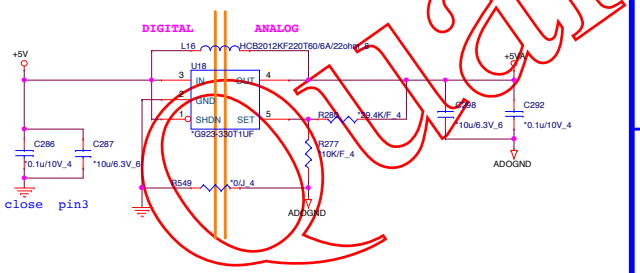
Power (ADO)

HEADPHONE/MIC/LINE combo (AMP)

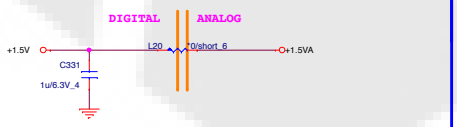
FB1/FB2(SLEEVE/RING2) should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk



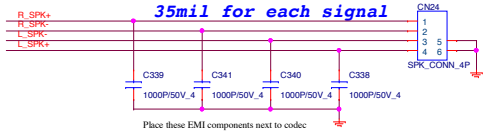
Codec PWR 5V(ADO)



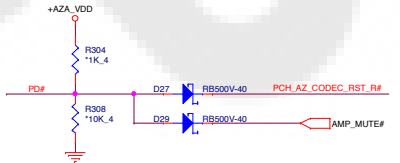
Codec PWR 1.5V(ADO)



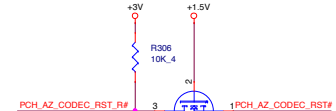
Internal Speaker



Mute(ADO)

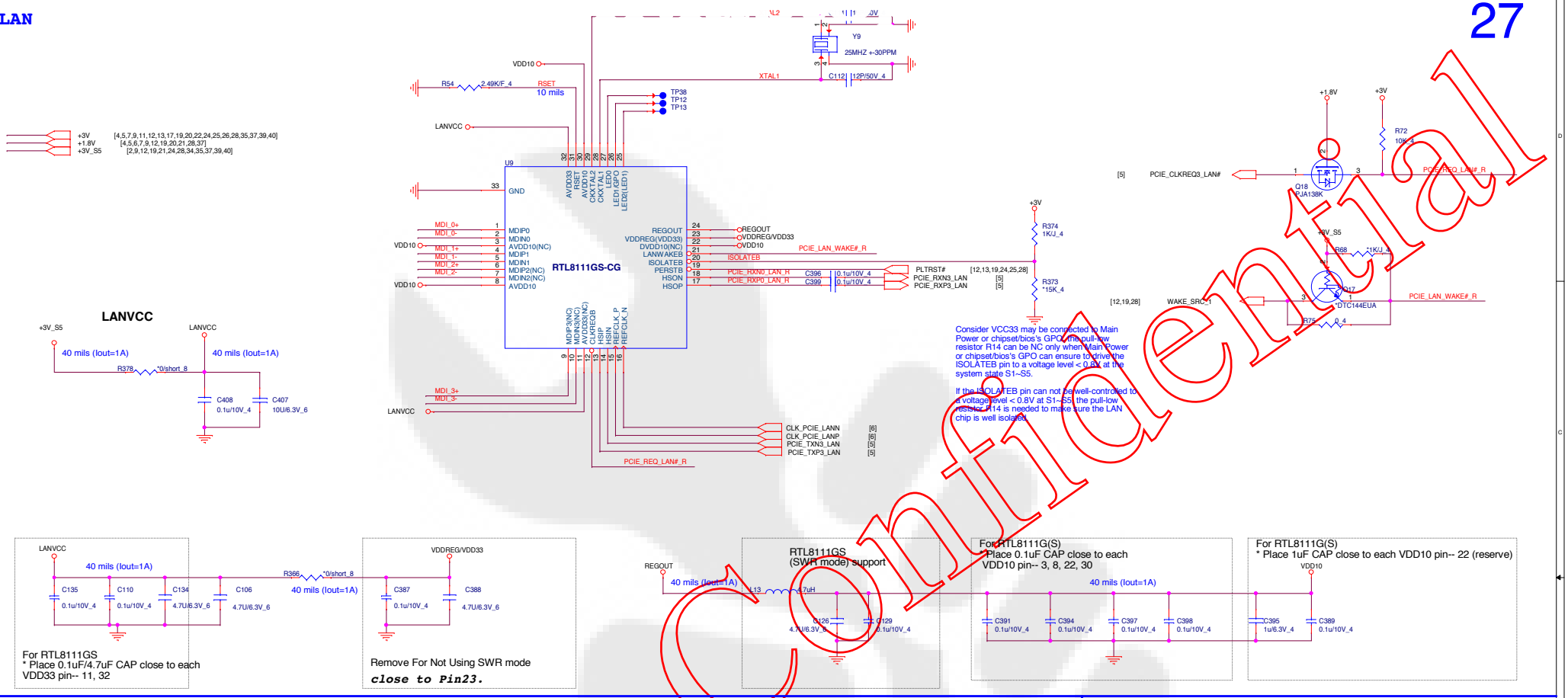


Level shift

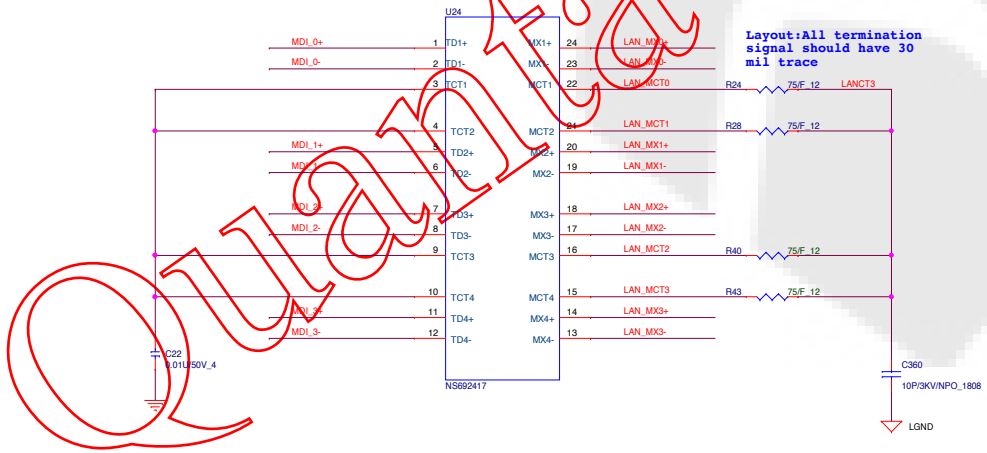


Quanta Computer Inc. PROJECT : ZYL/ZYLA			
Size	Document Number		Rev
	Codec ALC3225		1A
Date: Thursday, July 10, 2014	Sheet 26	of 44	

LAN

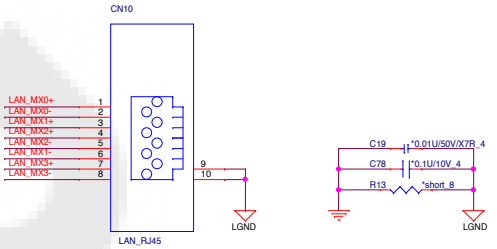


Tramsformer



RJ45 Connector

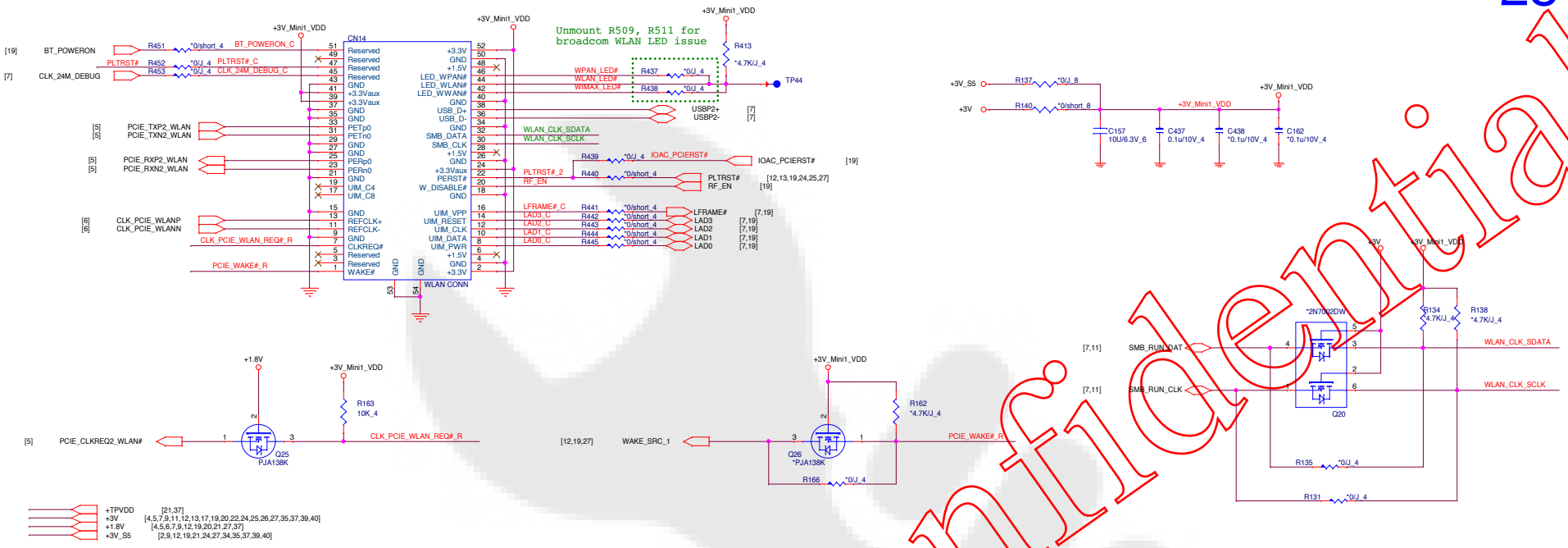
Need Check P/N and F/P



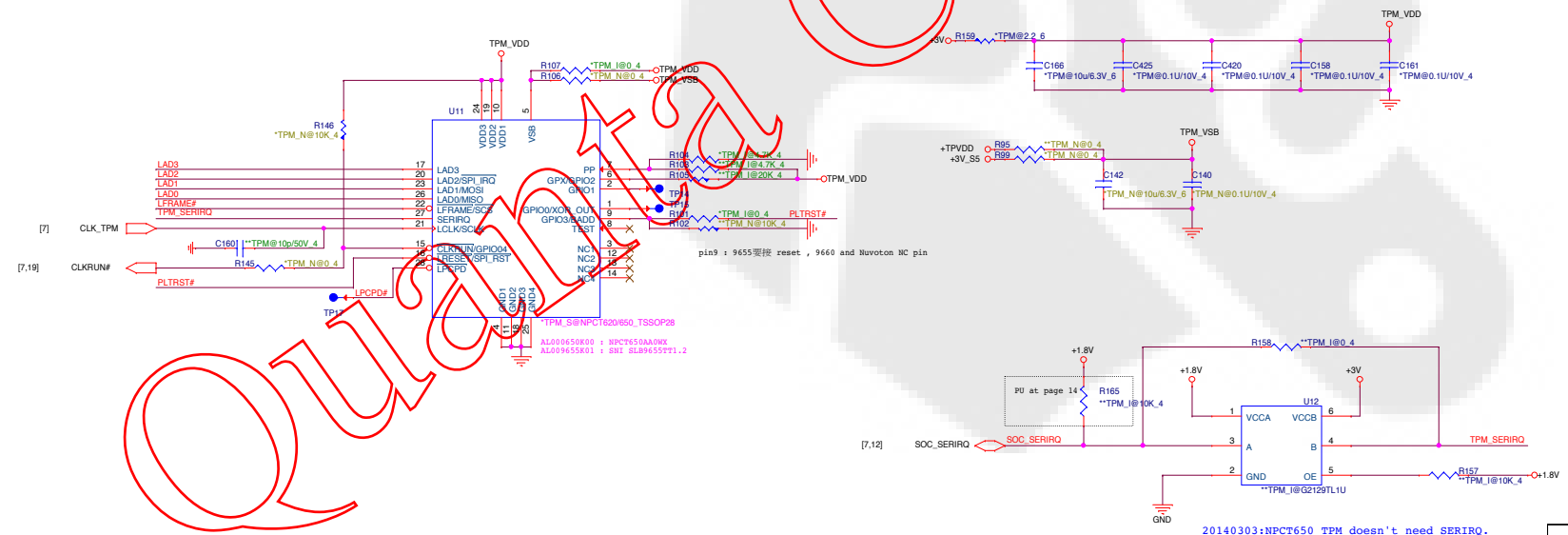
Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	LAN	1A
Date: Thursday, July 10, 2014	Sheet 27 of 44	

WLAN



TPM (TPM)



Quanta Computer Inc.		
PROJECT : ZYL/ZYLA		
Size	Document Number: WiFi & BT & TPM	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 28 of 44	

HOLE(OTH)

HOLE20 *H-C315D110P2

HOLE22 *HG-C315D110P2

HOLE29 *hg-tc315bc236d110p2

HOLE13 *HG-C315D110P2

HOLE18 *H-C315D110P2

HOLE12 *HG-C315D110P2-V5

HOLE26 *HG-C315D110P2

HOLE23 *HG-C315D110P2

HOLE27 *HG-C315D110P2

HOLE25 *HG-C315D110P2

HOLE15 *HG-C315D110P2

HOLE14 *H-C110D110N

HOLE24 *HG-C315D110P2

HOLE28 *H-C315D110P2

GPU nuts

HOLE16 EV@H-C236D138P2

HOLE19 EV@H-C236D138P2

HOLE17 EV@H-TC236I138BC236D138P2

Mini card nuts

HOLE21 H-C217D61P2

CPU nuts

HOLE9 *H-TC256BC236D161P2

HOLE10 *H-TC256BC236D161P2

HOLE11 *H-TC256BC236D161P2

reserve for ESD

C522 0.1U/25V_4 +1.05V_GFX

C523 0.1U/25V_4 +VA_IACM

C524 0.1U/25V_4 +3V

C258 0.1U/25V_4 +3V

C302 0.1U/25V_4 +5V_S5

+3VPCU C285 0.1U/25V_4 +5V_S5

0.1U/25V_4 C143 +3VPCU

+VCC_CORE C212 *0.1U/10V_4 +VCC_GFX

C205 *1000p/50V_4

+VA_IACM C429 *0.1U/25V_4 +VIN

C428 *1000p/50V_4

C262 *0.1U/25V_4 +VIN

C47 *1000p/50V_4

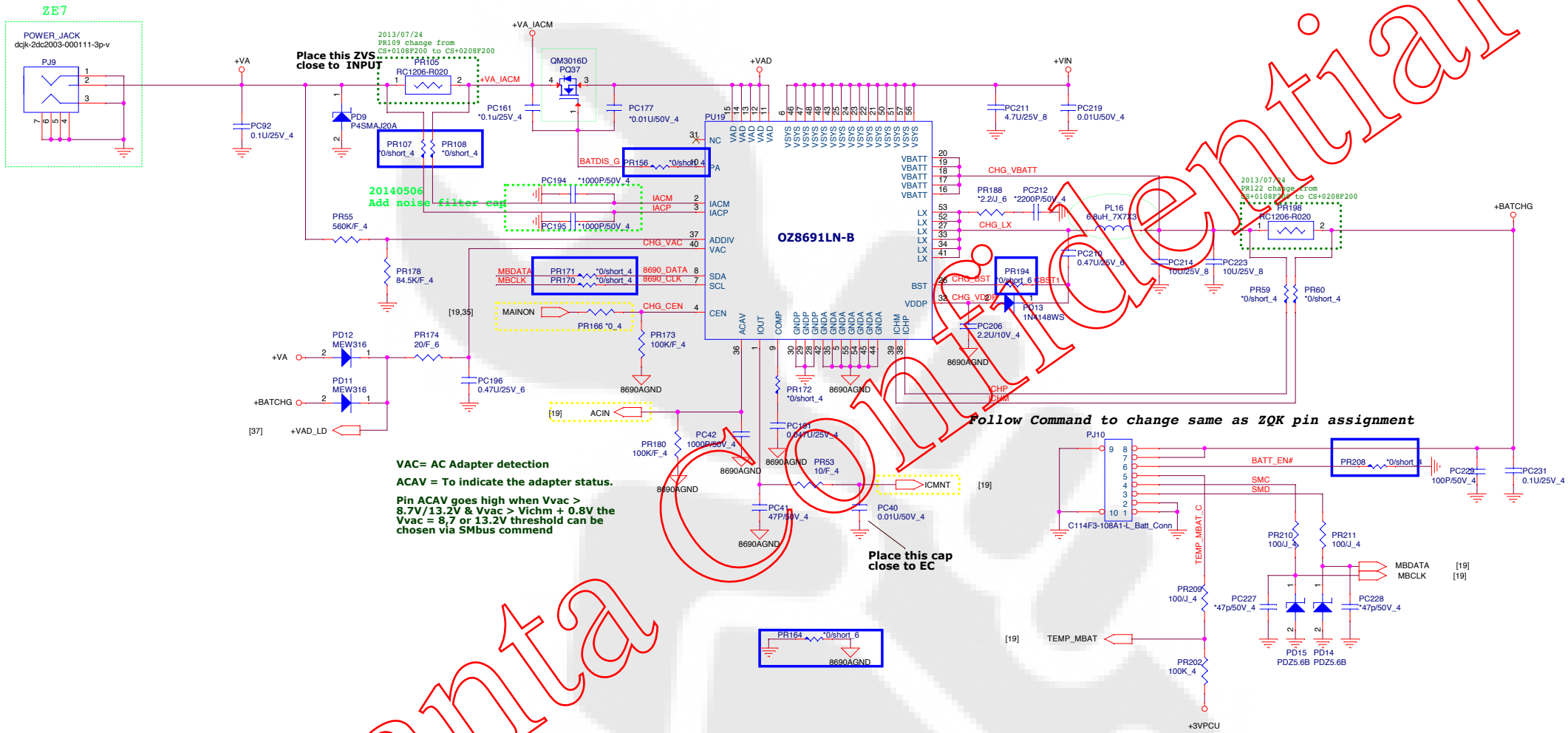
C430 2.2n/50V_6 +VA_IACM

Quanta Computer Inc.

PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	USB BOARD CONN	1A
Date: Thursday, July 10, 2014	Sheet 29 of 44	

DFPJ06MR013-- 95W
DFPJ06MR007--- 45W



Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: Charger (OZ8690ALN)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 30 of 44	

DC/DC +3VPCU/+5V_S5

LDO(MAX)=100mA

+3.3 Volt +/- 5%
Countinue current:2A
Peak current:2.7A
OCP minimum:A

Remove JP15

Remove JP13

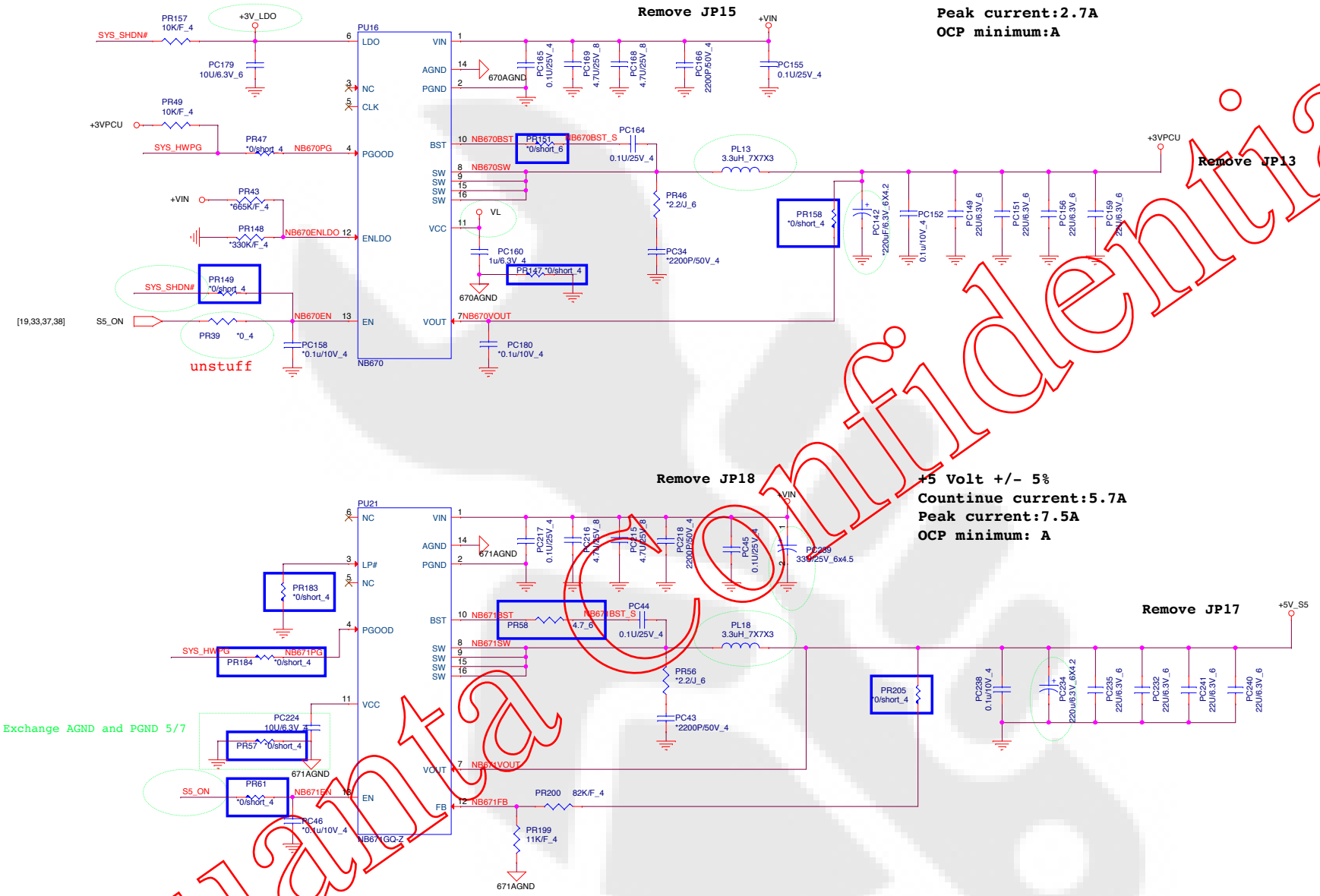
Remove JP18

+5 Volt +/- 5%
Countinue current:5.7A
Peak current:7.5A
OCP minimum: A

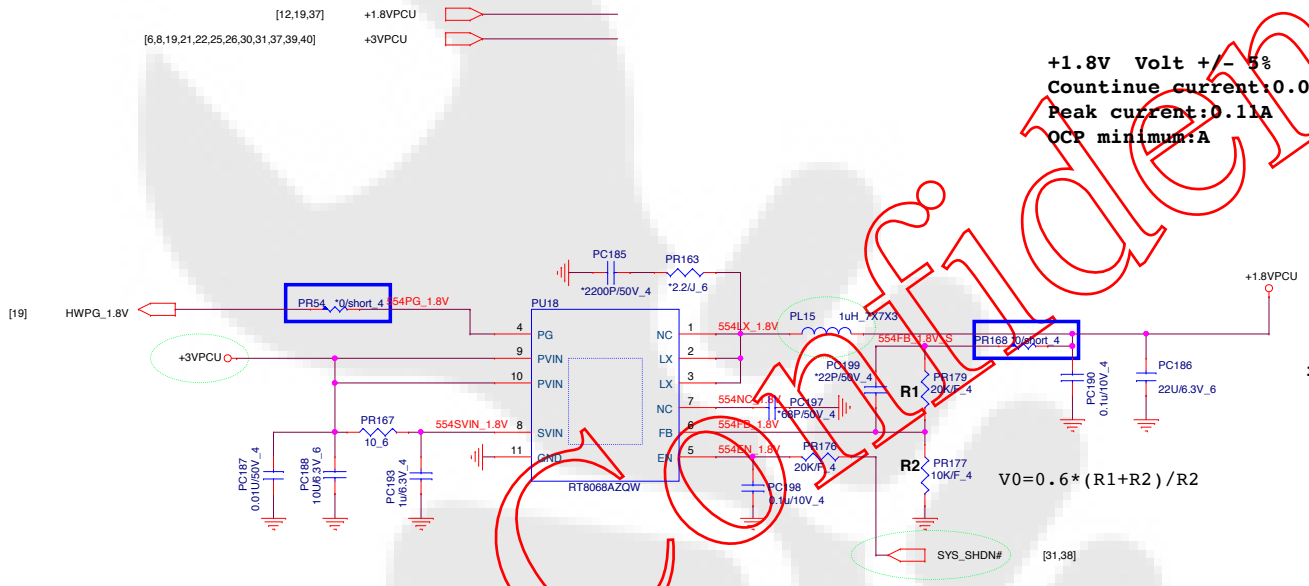
Remove JP17

unstuff

Exchange AGND and PGND 5/7



Quanta Computer Inc.
PROJECT : ZHJ
Size | Document Number: 3/5VS5 (NB670/NB669) | Rev: 1A
Date: Thursday, July 10, 2014 | Sheet 31 of 44



+1.8V Volt +/- 5%
Countinue current:0.08A
Peak current:0.11A
OCP minimum:A

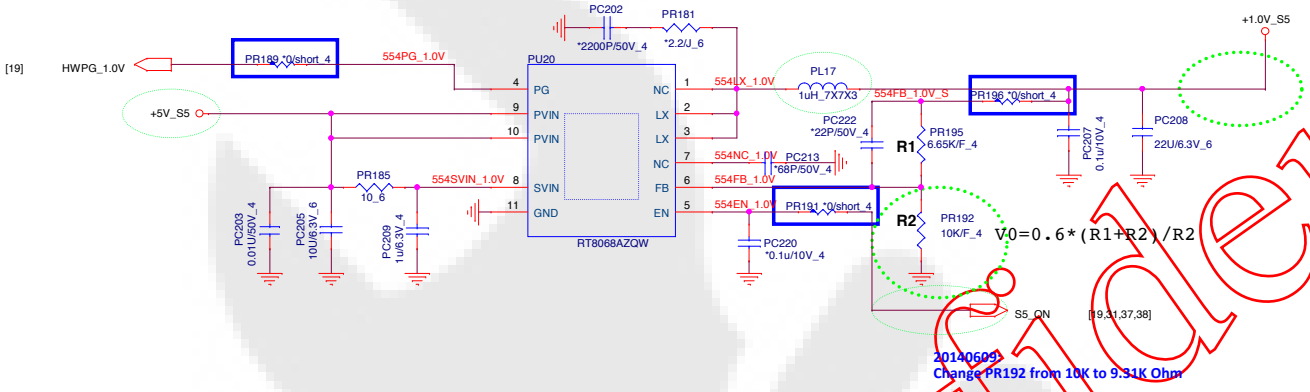
removed PR161 and PR165

V0=0.6*(R1+R2)/R2

Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: +1.8VPCU	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 32 of 44	

[9,37] +1.0V_S5
[24,25,31,34,35,36,37,39] +5V_S5
[2,9,12,19,21,24,27,28,34,35,37,39,40] +3V_S5

+1.0V Volt +/- 5%
Countinue current:2.4A
Peak current:3.2A
OCP minimum:A



removed PR169 ,PR175 and PR182

V0=0.6*(R1+R2)/R2

20140609
Change PR192 from 10K to 9.31K Ohm

Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: +1.0V	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 33 of 44	

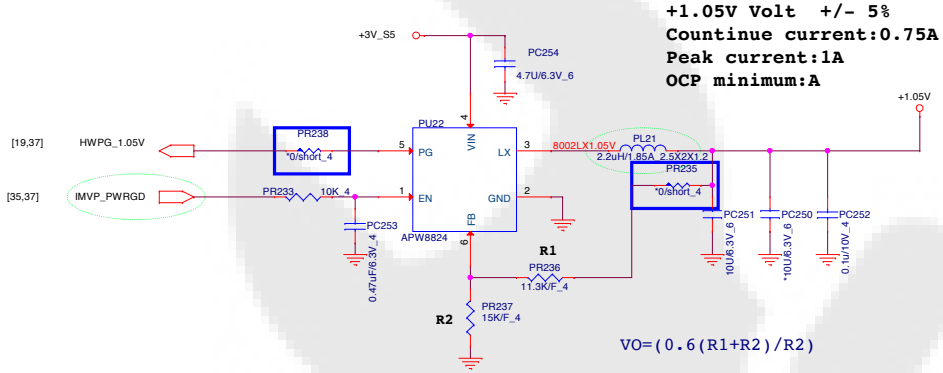
[2,9,12,19,21,24,27,28,35,37,39,40] +3V_S5

[5,9] +1.05V

[9,22,23,26] +1.5V

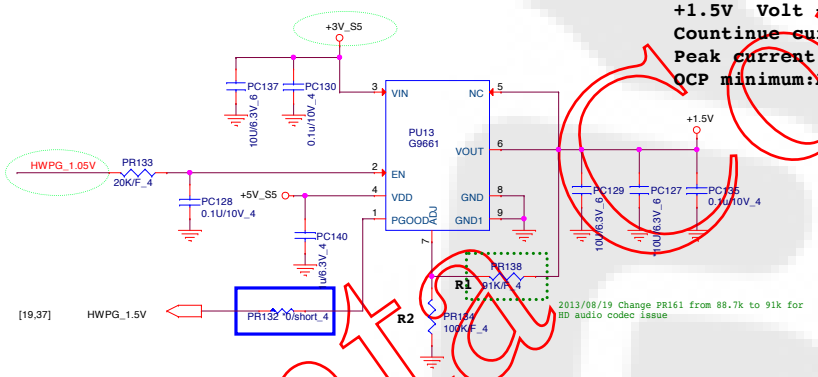
+1.05V Volt +/- 5%
Countinue current:0.75A
Peak current:1A
OCP minimum:A

removed PR232 and PR234



VO=(0.6(R1+R2)/R2)

+1.5V Volt +/- 5%
Countinue current:0.023A
Peak current:0.03A
OCP minimum:A



VO=(0.8(R1+R2)/R2)
R2<120KOhm

Quanta Computer Inc.
PROJECT : ZHJ
Size | Document Number +1.05V/1.5V | Rev 1A
Date: Thursday, July 10, 2014 Sheet 34 of 44

20130617 Change +1.05V to +1.05V

Close to VR

VR_SVID_ALERT# close to CPU

VR_SVID_DATA and VR_SVID_CLK close to VR

[6,9,37] +1.0V
[8,9,29] +VCC_GFX
[20,29,30,31,36,37,38,39,40] +VIN
[24,25,31,33,34,36,37,39] +5V_S5

AXG

Remove JP19

+VCC_GFX
TDC : A
PEAK : 14A
OCP : A
Width : mil

GFX_CORE Load Line :
-5.9mV/A for 2.xW SDP

Core

Remove JP20

+VCC_CORE
TDC : A
PEAK : 12A
OCP : A
Width : mil

VCORE Load Line :
-5.9mV/A for 2.xW SDP

PU9
ISL95833HRTZ-T

Parallel

Close to the CPU side.

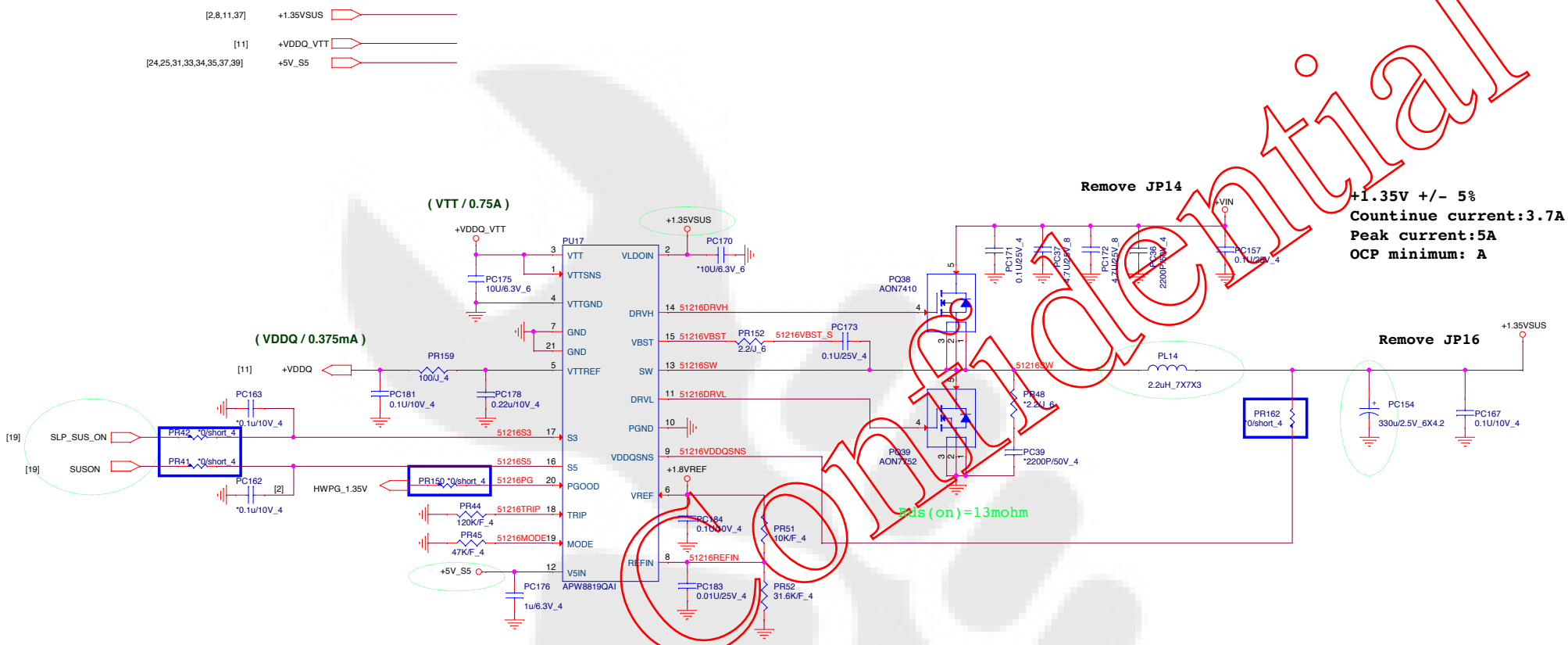
Close to the VR side.

Close with AXG inductor

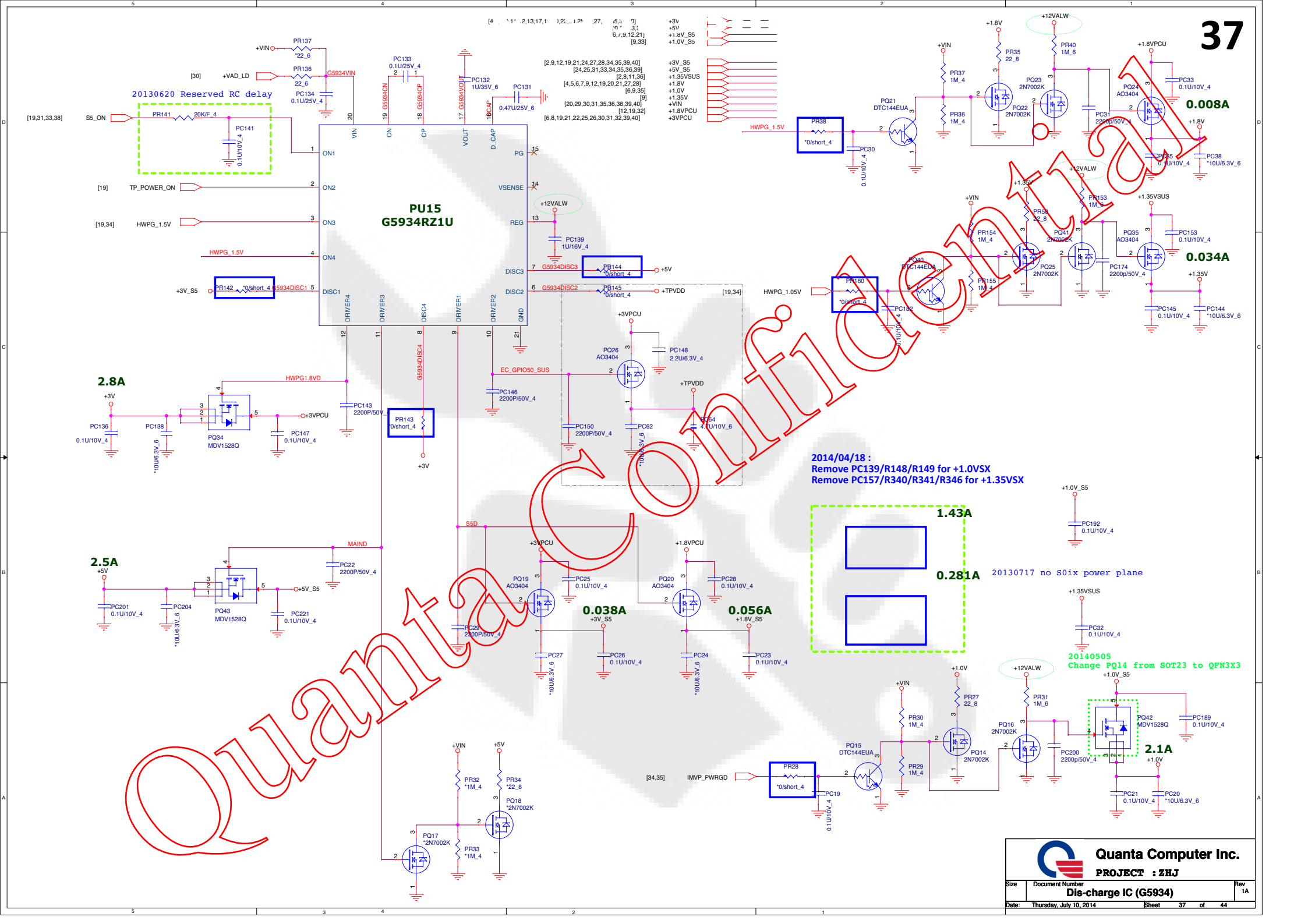
Close with phase1 inductor

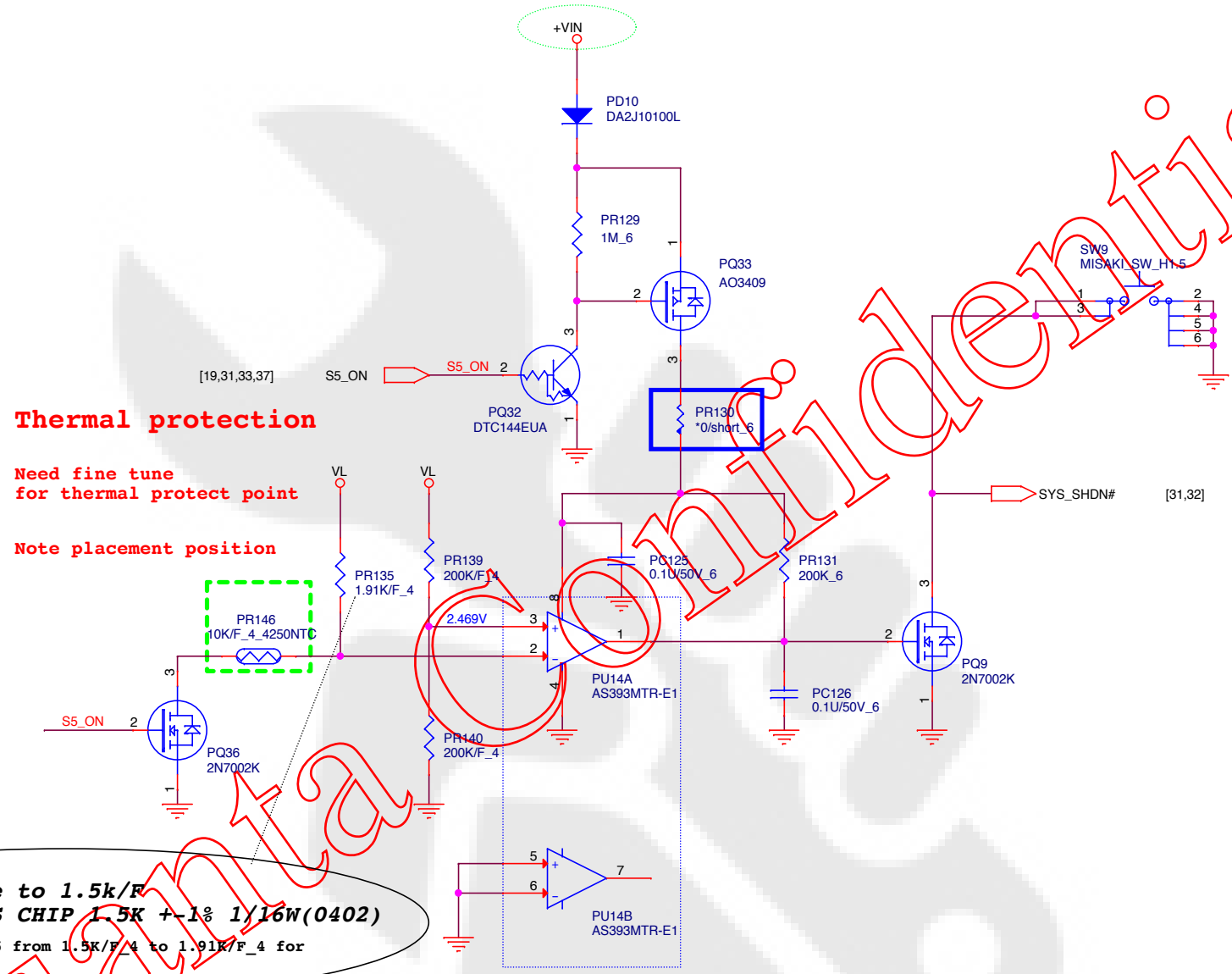
Quanta Computer Inc.
PROJECT : ZHJ

Size | Document Number: +VCC_CORE/+VGFX (ISL95833) | Rev 1A
Date: Thursday, July 10, 2014 | Sheet 35 of 44



Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: DDR3 (APW8819)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 36 of 44	


20130620 Reserved RC delay
PU15
G5934RZ1U
ON1
ON2
ON3
ON4
DISC1
VIN
CN
CP
VOUT
D_CAP
PG
VSENSE
REG
DISC3
DISC2
DRVER4
DRVER3
DISC4
DRVER1
DRVER2
GND
2.8A
2.5A
0.038A
0.056A
1.43A
0.281A
2.1A
0.008A
0.034A
2014/04/18 :
Remove PC139/R148/R149 for +1.0VSX
Remove PC157/R340/R341/R346 for +1.35VSX
20130717 no S0ix power plane
20140505
Change PQ14 from SOT23 to QFN3X3
Quanta Computer Inc.
PROJECT : ZHJ
Dis-charge IC (G5934)
Thursday, July 10, 2014
Sheet 37 of 44



Thermal protection

Need fine tune for thermal protect point

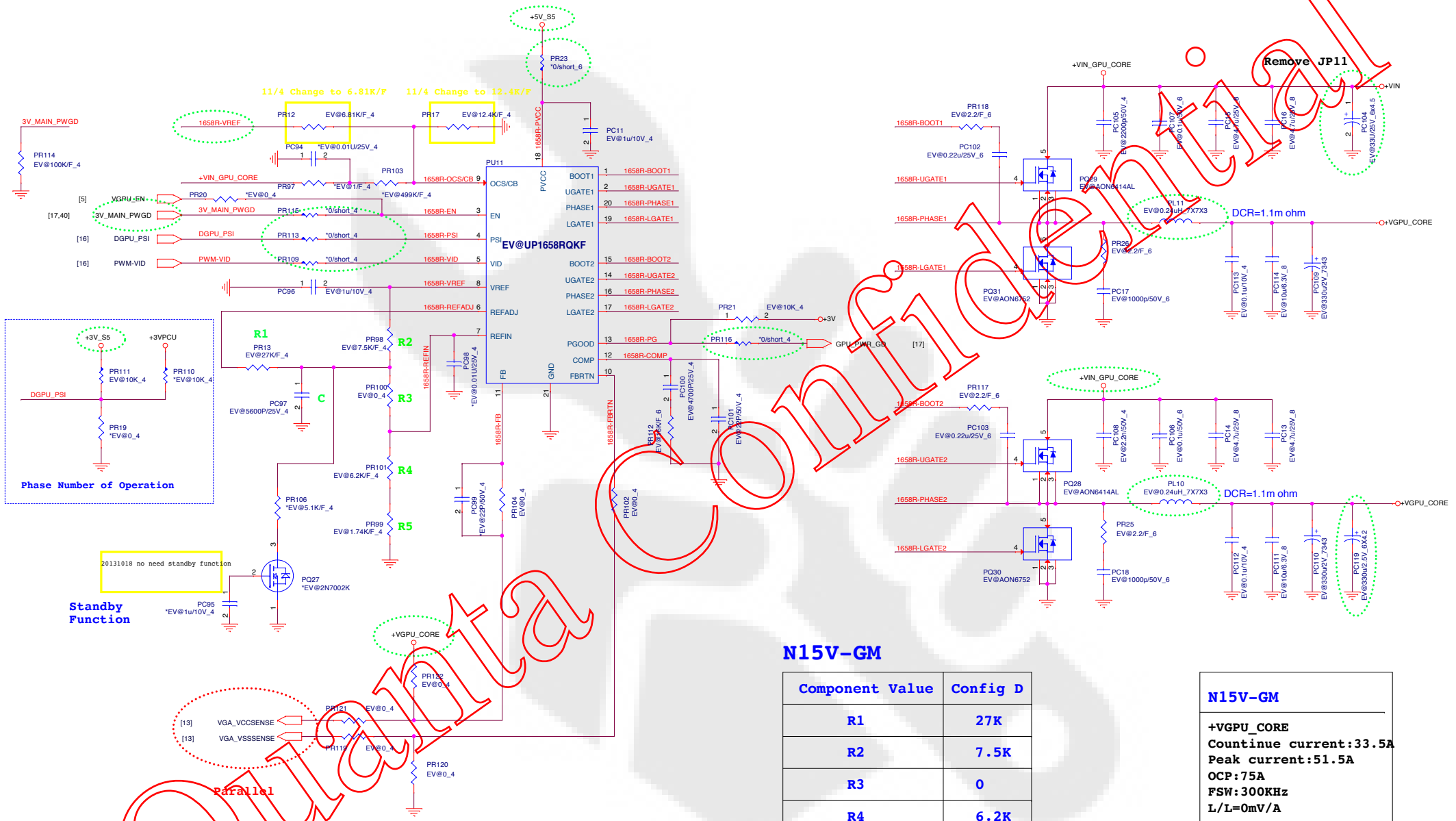
Note placement position

note: PR173 change to 1.5k/F
CS21502FB14 RES CHIP 1.5K +-1% 1/16W(0402)

20140702 Change PR135 from 1.5K/F_4 to 1.91K/F_4 for thermal request

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: Thermal / Hole	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 38 of 44	



N15V-GM

Component Value	Config D
R1	27K
R2	7.5K
R3	0
R4	6.2K
R5	1.74K
C	5.6nF

N15V-GM

+VGPU_CORE
Countinue current:33.5A
Peak current:51.5A
OCP:75A
FSW:300KHz
L/L=0mV/A

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	+VGPU_CORE (UP1658RQKF)	1A
Date: Thursday, July 10, 2014	Sheet 39 of 44	

[13,14,15] +1.05V_GFX
[13,14,18] +1.5V_GFX
[13,16,17] +3V_GFX

20140421:
Change 554PG_1.05V to Test PAD.

Remove JP12

Remove JP14

+1.05V_GFX
TDC : 1.553A
PEAK : 2.29A
Width : 90mil

20140529:
Change PR125 from 10K to 26.7K Ohm
VO=0.6*(R1+R2)/R2

20140421:
Change Enable from 3V_MAIN_PWRGD

+3V_GFX
TDC : 0.17A
PEAK : 0.342A
Width : 20mil

Remove JP9

20140609:
Change PL9 from 3.3uH to 2.2uH

Remove JP10

+1.5V_GFX
1.5 Volt +/- 5%
TDC : 3.24A
PEAK : 4.25A
Width : 170mil

Change to 1.35V_GFX

20140606:
modify +1.5V_GFX PG sequence

20140606:
modify +1.5V_GFX PG sequence

VREF=0.604V

20140709 Change PR9 from 54.9K to 66.5K for EMI request and +1.5V_GFX will Change to 1.35V_GFX

Quanta Computer Inc.		
PROJECT : ZQ0		
Size	Document Number: +1.5V_GFX/+1.05V_GFX/+3V_GFX	Rev 1A
Date: Thursday, July 10, 2014	Sheet 40 of 44	

Bay Trail-M Power On Timing with SOix (S3 to S0)

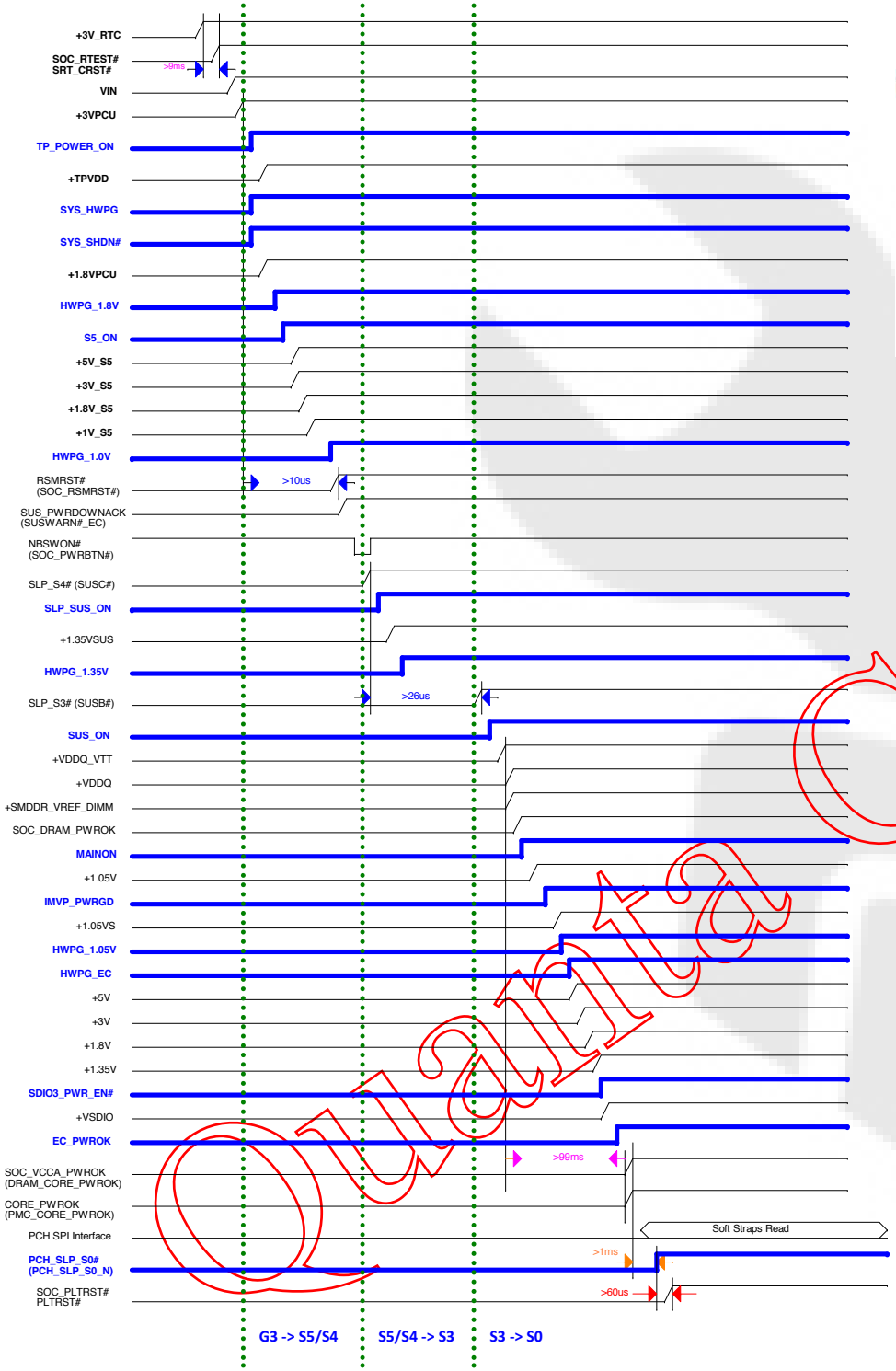
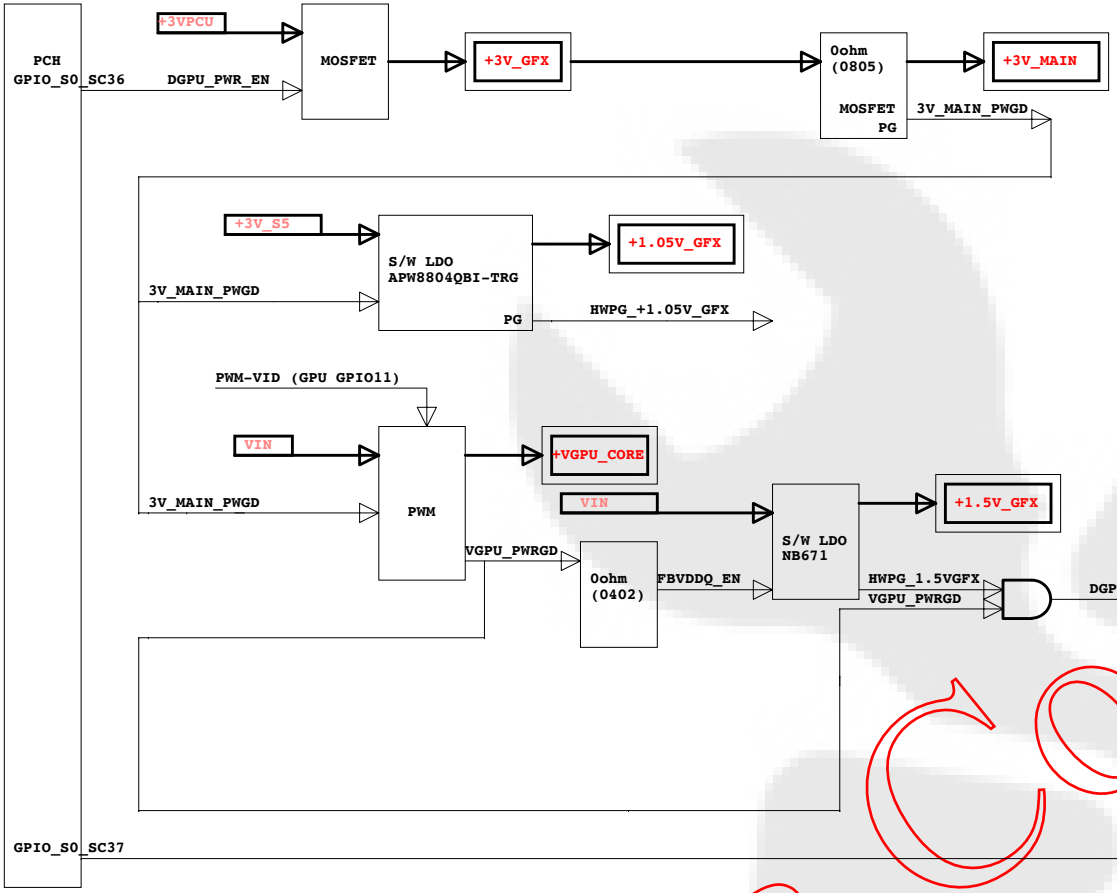


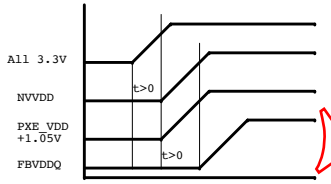
Table 37. SoC Sx-States to SLP_S*#

State	S0	S3	S4	S5	Reset w/o Power Cycle	Reset w/ Power Cycle
CPU Executing	In C0	OFF	OFF	OFF	No	OFF
PMC_SLP_S3#	HIGH	LOW	LOW	LOW	HIGH	LOW
PMC_SLP_S4#	HIGH	HIGH	LOW	LOW	HIGH	LOW
S0 Power Rails	ON	OFF	OFF	OFF	ON	OFF
PMC_PLTRST#	HIGH	LOW	LOW	LOW	LOW	LOW
PMC_SUS_STAT#	HIGH	LOW	LOW	LOW	HIGH	LOW
PCIe Links	L0, L1	L3	L3	L3	L3 Ready	L3

NOTES: The processor treats S4 and S5 requests the same. The processor does not have PMC_SLP_S5#. PMC_SUS_STAT# is required to drive low (asserted) even if core well is left on because PMC_SUS_STAT# also warns of upcoming reset.

VGA power up sequence

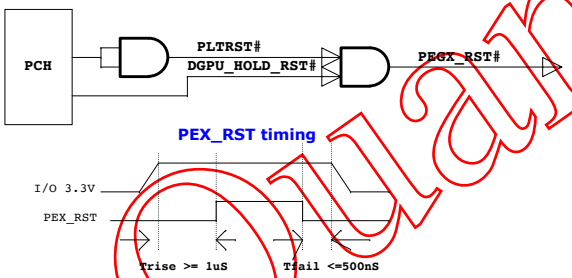




N15x Power on sequance

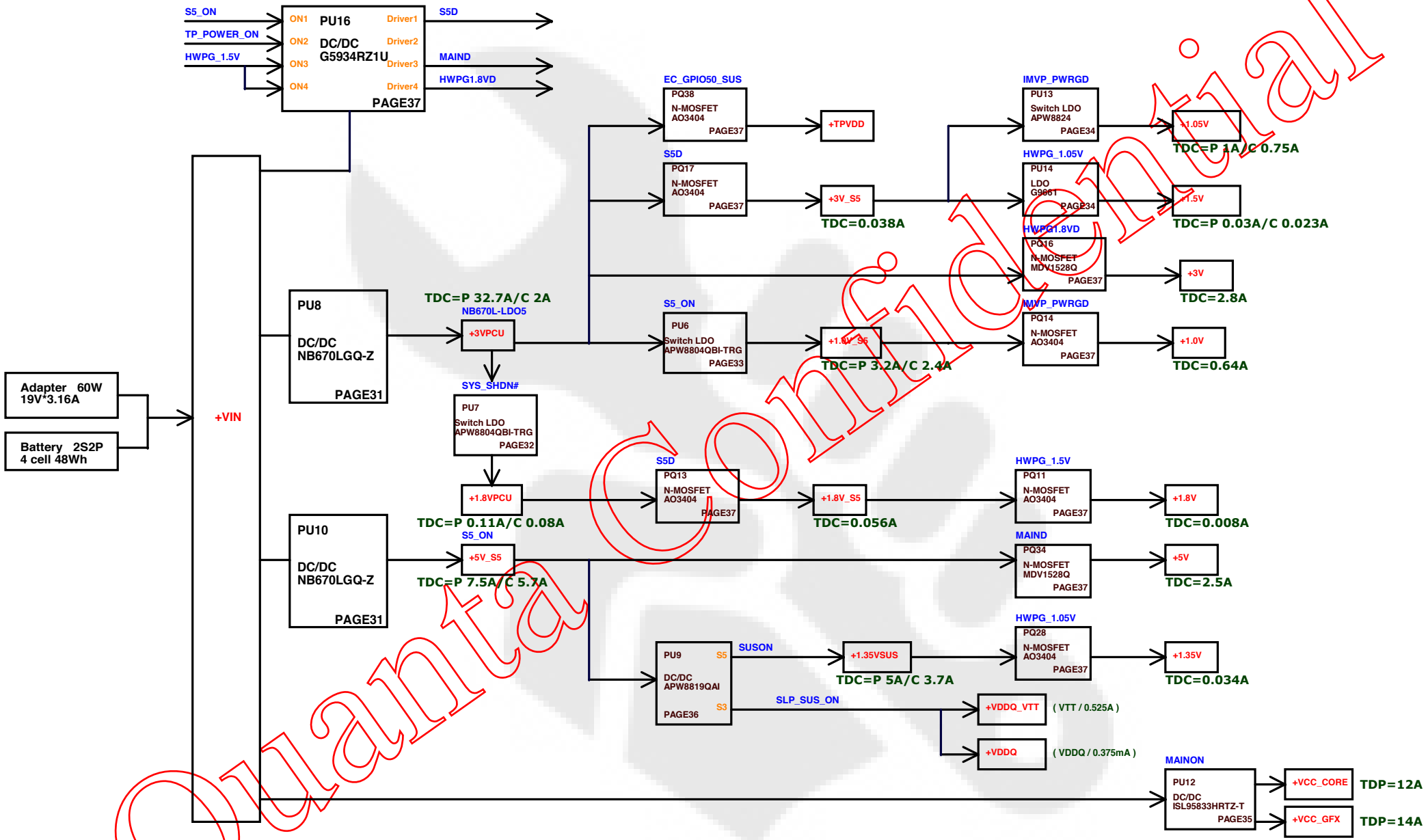
Notes: -All 3.3V includes all rails powered at 3.3V
-PEX_VDD 1.05V includes all rails that are shared

VGA Reset



Quanta Computer Inc.
PROJECT : ZYL
Size | Document Number: GPU PWR CRL | Rev 1A
Date: Thursday, July 10, 2014 | Sheet 42 of 44

ZYL POWER BLOCK DIAGRAM



Quanta Computer Inc.
PROJECT : ZYL

Size	Document Number	Rev
	ZYL Power Block Diagram	1A

Date: Thursday, July 10, 2014 Sheet 43 of 44

Model	Date	CHANGE LIST
ZYL REV:A		1. FIRST RELEASED
		Check CPU of P/N. ***Change VRAM of P/N.*** ***Check PJ6 for UMA or Dis- GVA.***
		VGA Chip (Buy and Sell) ***AJ0N15V0T07*** ***VR4GbIII9:*** ***HYNIX Graphic DDRIII 900 4Gb H5TC4G63AFR-11C*** ***AKD5PGWTW13 (B/S)*** ***MICRON Graphic DDRIII 900 4Gb MT41J256M16HA-093G:E*** ***AKD5PZSTL05 (B/S)*** ***SAMSUNG Graphic DDRIII 900 4Gb K4W4G1646D-BC1A*** ***AKD5PGWT504 (B/S)*** CPU (Buy and Sell) Intel BayTrial M cpu n3530 VGA Chip (Buy and Sell) AJ0N15V0T07 VRAM (Buy and Sell) VR2GbIII9 HYNIX Graphic DDRIII 900 2Gb H5TC2G63FFR-11C AKD5MZDTW04 ; AKD5MZDTW05 (B/S) MICRON Graphic DDRIII 900 2Gb MT41J128M16JT-093G:K AKD5MGSTL15 ; AKD5MGSTL25 (B/S) SAMSUNG Graphic DDRIII 900 2Gb K4W2G1646Q-BC1A AKD5MGST511 ; AKD5MGST513 (B/S)
ZYL REV:B	5/27	1.PAGE.22 , modify SW10 pin3 connect to pin1 ,pin2 connect to pin4&pin5&pin6 2.PAGE.24 , modify CN16 & CN18 footprint from "USB-TARA4-9B1323-9P-SMT" to "UB2-UARDM-4K1926-4P-R"
	5/28	1.PAGE.25 , SWAP CN23 USB_CAR_N & USB_CAR_P
	5/29	1.PAGE.40 , Change PR125 from 10K to 26.7K due to 1.05V_GFX output is incorrect
	6/6	1.PAGE.6 , Change C458、C453 from 10P/50V to 12P/50V 2.PAGE.40 , Add PR239 to modify +1.5V_GFX PG sequence
	6/9	1.PAGE.29 , change hole 18、hole20、hole28 footprint from "HG-C315D110P2" to "H-C315D110P2" 2.PAGE.19 , Add D37 D38 C521 3.PAGE.20 , change R66 R67 R69 R70 R71 R73 R74 R76 from 620ohm to 619 ohm 4.PAGE.29 , Change C430 from "CH22206K917" to "CH22206J911" 5.PAGE.22 , Change C464 C466 C468 C469 from "0.01u/16V_4" to "0.01u/25V_4"
	6/10	1.PAGE.29 , reserve & mount C522 C523 C524 for ESD 2.PAGE.40 , Change PL9 from 3.3uH to 2.2uH for modified 1.5V_GFX efficiency.
	6/11	1.PAGE.24 , delete R465 R468 R522 R530 & mount L28,L31 for EMI
	6/13	1.PAGE.7 , PAGE.26,PAGE.28 , unmount R427,C310,R452,R453 2.PAGE.19 , mount D16 and change value form 14V/38V to 5V/30V 3.PAGE.26 , mount C338,C339,C340,C341 for EMI
ZYL REV:C	6/25	1.PAGE.6 , Change G9、G10 footprint from "SOLDERJUMPER-2" to "RC0603-C" 2.PAGE.26 , Change R311、R324、R565、R562、R550、R566 、L23、R13 from "0ohm" to "shortpad"
	6/27	1.PAGE.7 & 28 , Unmount R411 & Delete R147,R148,R149 2.PAGE.9 , Delete R180 for CPU +1.0V voltage
	7/1	1.PAGE.24 & 25 , Change C279,C224,C414 from 100u/6.3V_3216 to 100u/6.3V_3528
	7/2	1.PAGE.38 , Change PR135 from 1.5K/F_4 to 1.91K/F_4 for thermal request
	7/9	1.PAGE.40 , Change PR9 from 54.9K to 64.9K for EMI request and +1.5V_GFX will Change to 1.35V_GFX

Quanta Computer Inc.	DOC NO.	PROJECT MODEL :	ZYL/ZYLA	APPROVED BY:		DATE:
PROJECT : ZYL/ZYLA		PART NUMBER:		DRAWING BY:		REVISON:

Size: Document Number: Change list Rev: 1A

Date: Thursday, July 10, 2014 Sheet 44 of 44