Compal Confidential

EH7LW/EH5LW/FH5TW/EH7LC/EH5LC

DIS MB Schematic Document

LA-H791P

Rev: 2.0
2019.05.29

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Compal Electronics, Inc.		
Title: Cover Sheet		
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HDMI Conn.

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DDI2
HDMI x 4 lanes

eDP

page 28

eDP

DDI

Intel Whiskey lake U
Intel Comet lake U

Processor

Cannon Lake PCH-LP

46x24 mm

15W
1528pin BGA
page 07~18

WHL-U 4+2
WHL-U 2+2

Memory BUS
Dual Channel

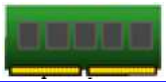
1.2V DDR4 2400

Interleaved Memory

DDR4-ON BOARD 4G 8Gbx16

page 19

260pin DDR4-SO-DIMM X1



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Nvidia N17S-G0/G2
with GDDR5 x2

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PCIe 3.0 x 4
8GT/s
port 1-4

SATA Gen 3
6.0 Gb/s
(SATA2)

PCIE 3.0 x4
8GT/s
Port 9-12

Flexible IO
Base-U PCIE 3.0x2 (CML)

NGFF
WLAN
support CNVi
USB2 port 10

PCIe 1.0
2.5GT/s
port 6
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PCIe 1.0
2.5GT/s
port 5

LAN(GbE)
Realtek 8111H
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RJ45 conn.

SATA Gen 3
6.0 Gb/s
port 0
(SATA0)

SATA HDD
Conn.

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SATA Gen 1
1.5. Gb/s
port 1
(SATA1A)

SATA ODD
Conn.

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conn x1
USB3 port 1
USB2 port 1

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conn x2
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USB2 port4(SUB)

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CMOS
Camera
USB2 port 7

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Card Reader
RTS5140
Reserved

USB2 port 6(SUB)

USBx8 48MHz

Finger
Printer
USB2 port 5

HD Audio 3.3V 24MHz

HDA Codec
ALC255
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Touch
Screen
USB2 port 3
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SPI

SPI ROM
128Mb
page 9

LPC/eSPI BUS
CLK=24MHz

ENE
KB9022
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Int.KBD

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Touch Pad
PS2 (from EC) / I2C (from SOC)
USB2 port 8 (FP)

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Int. Speaker
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Int. DMIC
on Camera
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Fan Control
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RTC CKT.
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Power On/Off CKT.
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DC/DC Interface CKT.
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Power Circuit DC/DC
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Sub Board

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HDD/B
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LS-H783P
LID/B
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LS-H781P
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LS-H784P
ODD/B
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Title: Block Diagrams

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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 1%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3	PCB Revision
0	0	0 V	0 V	0.300 V	0x00 - 0x13	0.1(EVT)
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	0.2(DVT)
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	0.3(PVT)
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	1.0(PreMP)
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Table

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
CODEC	255@/256@
EC Mode Select	LPC@ / ESPI@
For Intel CMC	CMC@
CNVi /BT PCM Select	CNVI@/PCM@
EMI requirement	EMI@ / @EMI@
ESD requirement	ESD@ / @ESD@
RF requirement	@RF@
TPM	TPM@
Finger Print	FP@/FPEMC@
Finger print power	FP3V@/FP5V@
UMA or DGPU	UMA@/VGA@
CPU Select	WHL@/CML@
SATA/ODD select	RD@/NRD@/ODD@
USB charger	CHG@

BOM Option Table

Item	BOM Structure
MB Stage	EVT@/DVT@/PVT@/MP@
G Sensor	GSEN@
For over 3 cell battery	3S@
MD BOM Select	NOX76@/X76DSAM@/ X76DMIC@/X76DHYN@/
VRAM BOM Select	X76VSAM@/X76VMIC@/ X76VHYN@/
Memory related	SPD@/DDP@/MEM@
CPU C10 support	C10@
BOM select	15DIS@/15@/
VGA chip	G0@/G2@

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.05VALW_PRIM	+1.05V Always power rail	ON	ON	ON*1
+1.05V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.05VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VSDGPU	+1.0VS power rail for N17S	ON*2	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON*2	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for N17S(AON)	ON*2	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for N17S(MAIN)	ON*2	OFF	OFF
+VGA_CORE	Core power for discrete GPU	ON*2	OFF	OFF

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.
ON*2 power plane is ON when DGPU turn on

43 level BOM table

43 Level	Description	BOM Structure
431AHVBOL01	SMT MB AH791 EH7LW I37020U22 230 HDMI	8145U@/PCB@/MEM@/SPD@/X76DHYN@/VGA@/G0@/X76VHYN@/NC10@/CNVI@/NCHG@/FP@/3S@/LPC@/CMC@/GSEN@/RD@/ODD@/255@/BYOC@/TPM@/EVT@/X4E@/15@/15DIS@/FP3V@
431AHVBOL02	SMT MB AH791 EH7LW I38130U42 250 HDMI	8265U@/PCB@/MEM@/SPD@/X76DHYN@/VGA@/G2@/X76VHYN@/NC10@/CNVI@/NCHG@/FP@/3S@/LPC@/CMC@/GSEN@/RD@/ODD@/255@/BYOC@/TPM@/EVT@/X4E@/15@/15DIS@/FP3V@
431AHVBOL03	SMT MB AH791 EH7LW I38145U22 230 HDMI	8145U@/PCB@/WHL@/MEM@/SDP@/X76DHYN@/VGA@/G0@/X76VHYN@/NC10@/CNVI@/NCHG@/RD@/ODD@/3S@/LPC@/CMC@/255@/DVT@/X4E@/17@/
431AHVBOL04	SMT MB AH791 EH7LW I58265U42 230 HDMI	8265U@/PCB@/WHL@/MEM@/SDP@/X76DHYN@/VGA@/G0@/X76VHYN@/NC10@/CNVI@/NCHG@/RD@/ODD@/3S@/LPC@/CMC@/255@/DVT@/X4E@/17@/
431AHVBOL05	SMT MB AH791 EH7LW I38145U22 230V8 HDMI	8145U@/PCB@/WHL@/MEM@/SDP@/X76DHYN@/VGA@/G0@/X76VSAM@/NC10@/CNVI@/NCHG@/RD@/ODD@/3S@/LPC@/CMC@/255@/DVT@/X4E@/17@/
431AHVBOL06	SMT MB AH791 EH7LW I58265U42 230V8 HDMI	8265U@/PCB@/WHL@/MEM@/SDP@/X76DHYN@/VGA@/G0@/X76VSAM@/NC10@/CNVI@/NCHG@/RD@/ODD@/3S@/LPC@/CMC@/255@/DVT@/X4E@/17@/
431AHVBOL51	SMT MB AH791 EH5LW I38145U22 230 HDMI	8145U@/PCB@/WHL@/MEM@/SDP@/X76DHYN@/VGA@/G0@/X76VHYN@/NC10@/CNVI@/NCHG@/NRD@/3S@/LPC@/CMC@/255@/DVT@/X4E@/15@/15DIS@/
431AHVBOL52	SMT MB AH791 EH5LW I58265U42 230 HDMI	8265U@/PCB@/WHL@/MEM@/SDP@/X76DHYN@/VGA@/G0@/X76VHYN@/NC10@/CNVI@/NCHG@/NRD@/3S@/LPC@/CMC@/255@/DVT@/X4E@/15@/15DIS@/
431AHVBOL53	SMT MB AH791 EH5LW I38145U22 230V8 HDMI	8145U@/PCB@/WHL@/MEM@/SDP@/X76DHYN@/VGA@/G0@/X76VSAM@/NC10@/CNVI@/NCHG@/NRD@/3S@/LPC@/CMC@/255@/DVT@/X4E@/15@/15DIS@/
431AHVBOL54	SMT MB AH791 EH5LW I58265U42 230V8 HDMI	8265U@/PCB@/WHL@/MEM@/SDP@/X76DHYN@/VGA@/G0@/X76VSAM@/NC10@/CNVI@/NCHG@/NRD@/3S@/LPC@/CMC@/255@/DVT@/X4E@/15@/15DIS@/

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Title: Notes List

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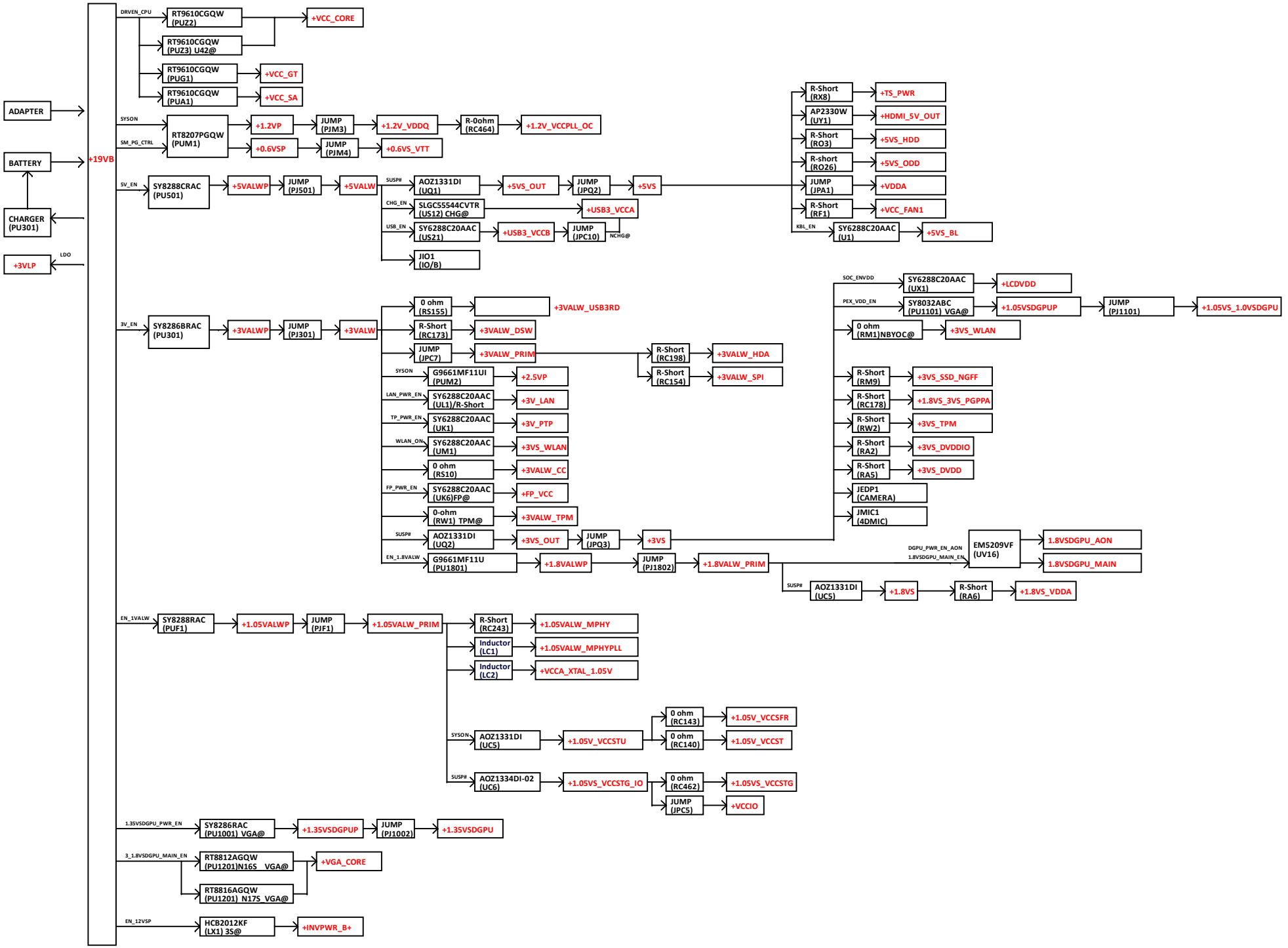

Security Classification	Compal Secret Data		Compal Electronics, Inc.
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			Title: Power Rail
Size: Custom	Document Number: EH7LW M/B LA-H791P		Rev: 0.2
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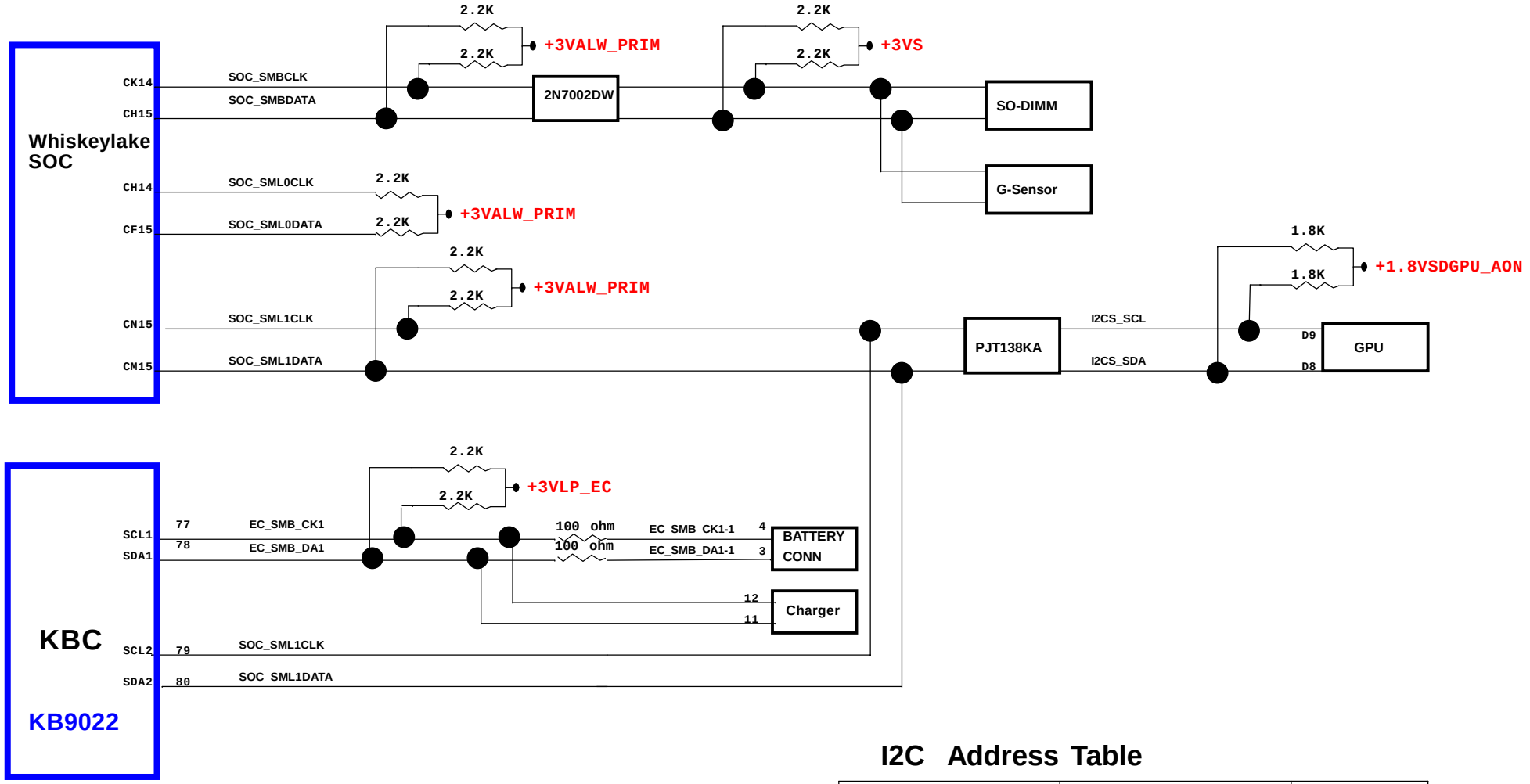

I2C Address Table

BUS	Device	Address (8 bit)
I2C_0 (+3VS)	Reserved	
I2C_1 (+3VALW_PRIM)	TM-P3393-003 (TP)	0x2C
	FA577E-1206 (TP-ELAN)	0x15
	SA577C-12A0 (TP-ELAN)	0x15
SOC_SMBCLK (+3VS)	SO-DIMM2	0xA4
	G-Sensor	0x30
SOC_SML1CLK (+3VALW_PRIM)	GPU	0x9E
	EC	
EC_SMB_CK1 (+3VLP)	BQ24781 (Charger IC)	0x12
	BATTERY PACK	0x16

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: SMBUS Routing Table

Size: Custom | Document Number: EH7LW M/B LA-H791P | Rev: 0.2

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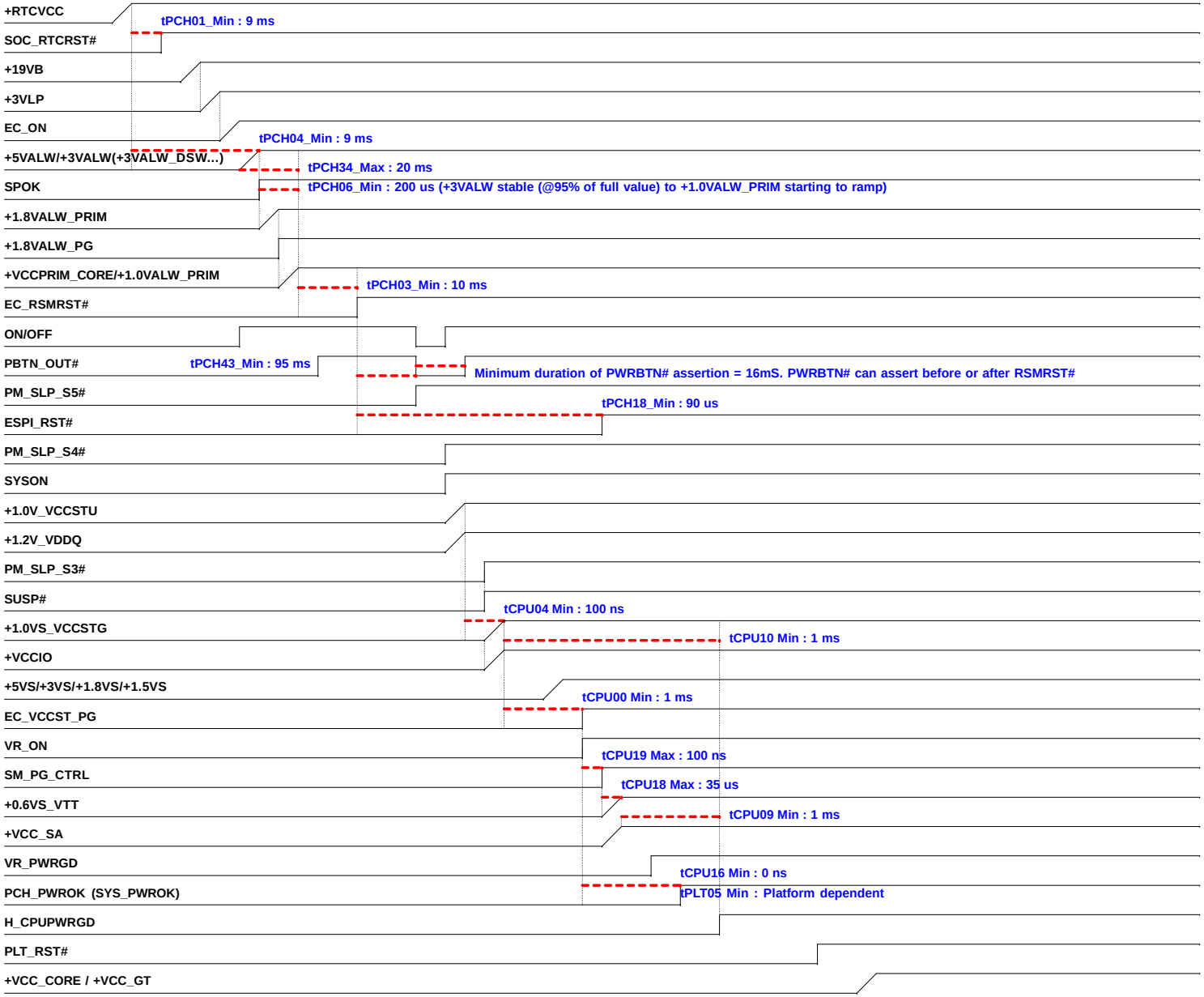
PWR Sequence_SKL-U2+2_DDR3L_Value_NON CS



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Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: Power Sequence

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UC1
S IC FJ8068404064702 SRD1V W0 2.1G ABO!
8145W0@
SA0000C6R60

UC1
S IC FJ8068404064604 SREJQ W0 1.6G ABO!
8265W0@
SA0000C6Q60

UC1
S IC CL8068404064708 SRFFZ V0 2.1G ABO!
8145U@
SA0000CNT60

UC1
S IC CL8068404064610 SRFFX V0 1.6G ABO!
8265U@
SA0000CNS70

UC1
S IC CL8068404064409 SRFFW V0 1.8G ABO!
8565U@
SA0000CNR50

UC1
S IC FJ8070104303905 SRGKW V0 1.8G BGA
10510U@
SA0000CNR50

UC1
S IC FJ8070104307606 SRGL0 V0 2.1G BGA
10110U@
SA0000CNR50

UC1
S IC FJ8070104307504 SRGKY V0 1.6G BGA
10210U@
SA0000CNR50

HDMI change to DDI2 port 11/26

HDMI

<29> SOC_DP2_N0
<29> SOC_DP2_P0
<29> SOC_DP2_N1
<29> SOC_DP2_P1
<29> SOC_DP2_N2
<29> SOC_DP2_P2
<29> SOC_DP2_N3
<29> SOC_DP2_P3

HDMI DDC (Port B)

<29> SOC_DP2_CTRL_CLK
<29> SOC_DP2_CTRL_DATA

UC1A

AL5 DDI1_TXN_0
AL6 DDI1_TXP_0
AJ5 DDI1_TXN_1
AJ6 DDI1_TXP_1
AF6 DDI1_TXN_2
AF5 DDI1_TXP_2
AE5 DDI1_TXN_3
AE6 DDI1_TXP_3
DDI

AC4 DDI2_TXN_0
AC3 DDI2_TXP_0
AC1 DDI2_TXN_1
AC2 DDI2_TXP_1
AE4 DDI2_TXN_2
AE3 DDI2_TXP_2
AE1 DDI2_TXN_3
AE2 DDI2_TXP_3

DISPLAY SIDEBANDS

EDP_COMP AM6 DISP_RCOMP

CC8 GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
CC9 GPP_E19/DPPB_CTRLDATA

SOC_DP2_CTRL_CLK CH4 GPP_E20/DPPC_CTRLCLK
SOC_DP2_CTRL_DATA CH3 GPP_E21/DPPC_CTRLDATA

CP4 GPP_E22/DPPD_CTRLCLK
CN4 GPP_E23/DPPD_CTRLDATA

CR26 GPP_H16/DDPF_CTRLCLK
CP26 GPP_H17/DDPF_CTRLDATA

WHL-U42_BGA1528
@
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EDP

AG4 EDP_TXN_0
AG3 EDP_TXP_0
AG2 EDP_TXN_1
AG1 EDP_TXP_1
AJ4 EDP_TXN_2
AJ3 EDP_TXP_2
AJ2 EDP_TXN_3
AJ1 EDP_TXP_3

EDP_TXN0 <28>
EDP_TXP0 <28>
EDP_TXN1 <28>
EDP_TXP1 <28>
EDP_TXN2 <28>
EDP_TXP2 <28>
EDP_TXN3 <28>
EDP_TXP3 <28>

eDP

AH4 EDP_AUX_N
AH3 EDP_AUX_P

EDP_AUXN <28>
EDP_AUXP <28>

AM7 DISP_UTILS

AC7 DDI1_AUX_N
AC6 DDI1_AUX_P
AD4 DDI2_AUX_N
AD3 DDI2_AUX_P
AG7 DDI3_AUX_N
AG6 DDI3_AUX_P

CN6 GPP_E13/DDPB_HPD0/DISP_MISC0
CM6 GPP_E14/DDPC_HPD1/DISP_MISC1
CP7 GPP_E15/DPPD_HPD2/DISP_MISC2
CP6 GPP_E16/DDPE_HPD3/DISP_MISC3
CM7 GPP_E17/EDP_HPD/DISP_MISC4

SOC_DP2_HPD
SOC_DP2_HPD <29>

From HDMI

EC_SCI#
CPU_EDP_HPD
EC_SCI# <36>
CPU_EDP_HPD <28>

From eDP

CK11 EDP_BKLTEN
CG11 EDP_VDDEN
CH11 EDP_BKLTCTL

ENBKL
SOC_ENVDD
SOC_BKL_PWM
ENBKL <36>
SOC_ENVDD <28>
SOC_BKL_PWM <28>

#571021 CFL-U PDG R0.7 p.104

Table 5-13. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	

+VCCIO
RC1 1 2 24.9_0402_1% EDP_COMP

#571021 CFL-U PDG R0.7 p.39
PU 24.9ohm for eDP

+1.05V_VCCST

#571021 CFL-U PDG R0.7 p.248
PU 1Kohm to VCCST

RC2 1 2 1K_0402_5% H_THERMTRIP#
CC132 1 2 ESD@ 1000P_0402_50V7K

CC52 @ESD@ .1U_0402_16V7K 2 1 H_PECI
ESD@ 2 1 H_PROCHOT#_R CC53 1000P_0402_50V7K

+1.05VS_VCCSTG

For Intel debug, place to CPU side.
#575412 WHL-U PDG R0.8 Figure.13-6

RC11 2 CMC@ 1 51_0402_5% SOC_XDP_TMS
RC13 2 CMC@ 1 51_0402_5% SOC_XDP_TDI
RC15 2 CMC@ 1 51_0402_5% SOC_XDP_TDO
RC35 2 CMC@ 1 51_0402_5% CPU_XDP_TCK0

+1.05VS_VCCSTG
RC3 1K_0402_5%
RC4 499_0402_1%

Reserved CATERR# for sighti ngs issue check

<36,43> H_PROCHOT#
@ T166 H_CATERR#
<36> H_PECI H_PECI
H_PROCHOT#_R
H_THERMTRIP#

@ T160 XDP_BPM#0
@ T161 XDP_BPM#1

<36,37> EC_TP_INT# RC137 2 @ 1 0_0402_5% TP_INT#

RC5 2 1 49.9_0402_1% CPU_POPIRCOMP
RC6 2 1 49.9_0402_1% PCH_OPIRCOMP
RC7 2 @ 1 49.9_0402_1% EDRAM_OPIO_RCOMP
RC8 2 @ 1 49.9_0402_1% EOPIO_RCOMP

#575412 WHL-U PDG R0.8
For CFL U43e, Pins L5 and N5 are OPCE_RCOMP and OPC_RCOMP respectively while in WHL, CNL SoCs these pins are RSVD

UC1D

AA4 CATERR#
AR1 PECI
Y4 PROCHOT#
BJ1 THRMTRIP#

CPU MISC

U1 BPM#_0
U2 BPM#_1
U3 BPM#_2
U4 BPM#_3

CE9 GPP_E3/CPU_GP0
CN3 GPP_E7/CPU_GP1
CB34 GPP_B3/CPU_GP2
CC35 GPP_B4/CPU_GP3

BP27 PROC_POPIRCOMP
BW25 PCH_OPIRCOMP

L5 RSVD70
N5 RSVD71

WHL-U42_BGA1528
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JTAG

PROC_TCK T6 CPU_XDP_TCK0
PROC_TDI U6 SOC_XDP_TDI
PROC_TDO Y5 SOC_XDP_TDO
PROC_TMS T5 SOC_XDP_TMS
PROC_TRST# AB6 SOC_XDP_TRST#

PCH_TCK W6 PCH_JTAG_TCK1
PCH_TDI U5 SOC_XDP_TDI
PCH_TDO W5 SOC_XDP_TDO
PCH_TMS P5 SOC_XDP_TMS
PCH_TRST# Y6 SOC_XDP_TRST#
PCH_JTAGX P6 CPU_XDP_TCK0

T280 @

PROC_PREQ# W2 XDP_PREQ#
PROC_PRDY# W1 XDP_PRDY#

T197 @
T196 @

12/21 PU

RC212 10K_0402_5% EC_SCI# 1 @ 2 +3VS

EC_SCI# SOC internal PU

#545659 PCH EDS1.51 P.131
SCI capability is available on all GPIOs, while NMI and SMI capability is available on only select GPIOs.
Below are the PCH GPIOs that can be routed to generate SMI# or NMI:
- GPP_B14 GPP_B20 GPP_B23
- GPP_C [23: 22]
- GPP_D [4: 0]
- GPP_E [8: 0], GPP_E [16: 13]

@ESD@ CC81 .1U_0402_16V7K SOC_XDP_TRST# 1 2

ZZZ PCB@
PCB EH7LW LA-H791P LS-H781P/H802P/H783P
DAZ2MF00301

ZZZ PCB20@
PCB EH7LW LA-H791P LS-H781P/H802P/H783P
DAZ2MF00302

ZZZ HDMI LOGO LOGO@
RO0000003HM

ZZZ X4E@
SMT EMC EE AH791 EH7LW
X4EAHVBOL01

ZZZ X4E@
SMT EMC DIS AH791 EH5LC
X4EAHVBOLD1

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Title: WHL-U(1/12)DDI,MSIC,XDP,EDP

Size: Custom | Document Number: EH7LW M/B LA-H791P | Rev: 0.2

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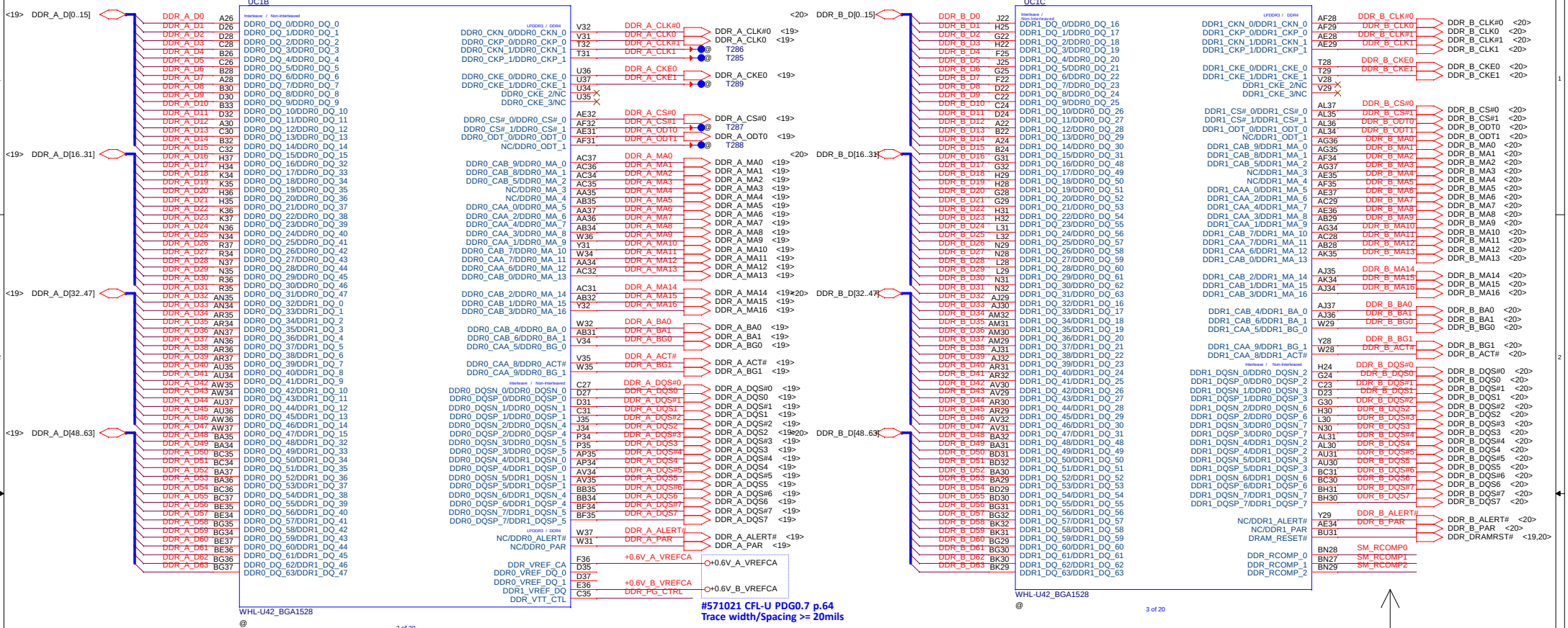
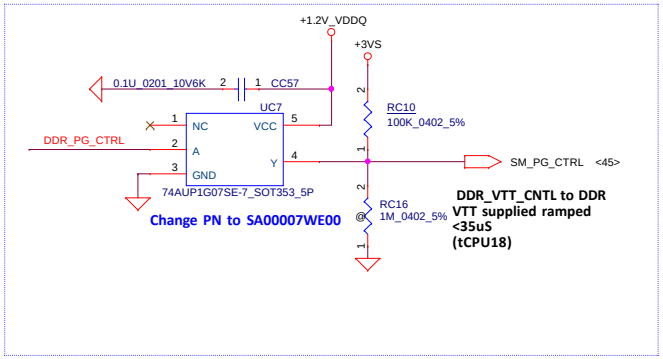
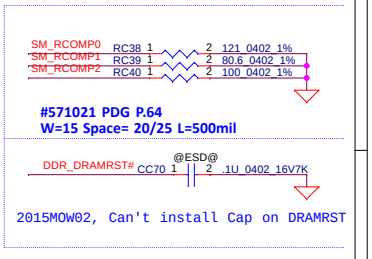
Interleaved Memory



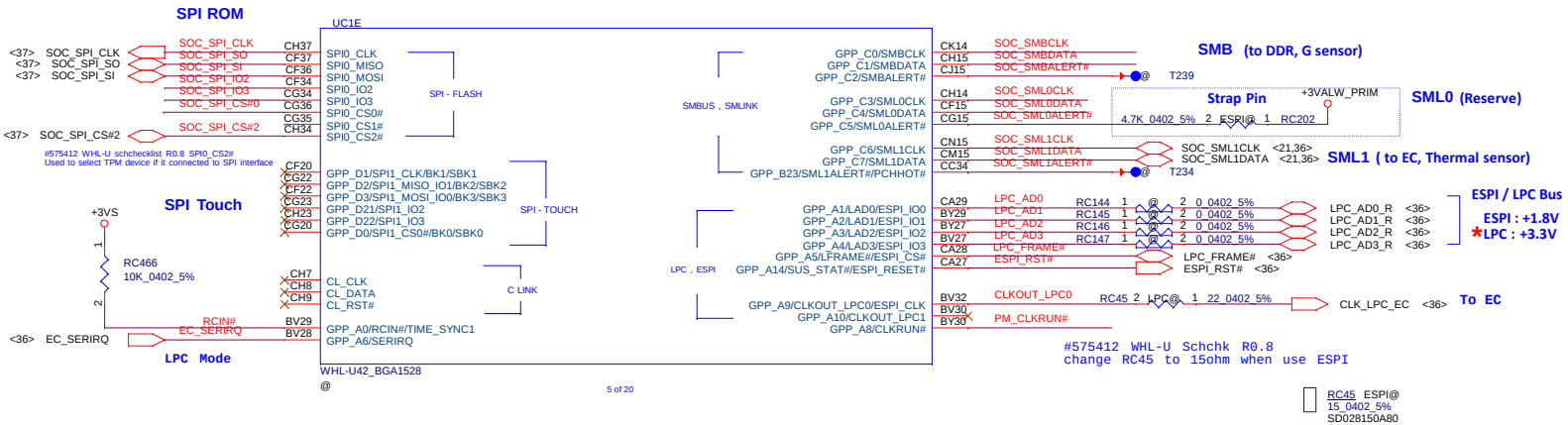


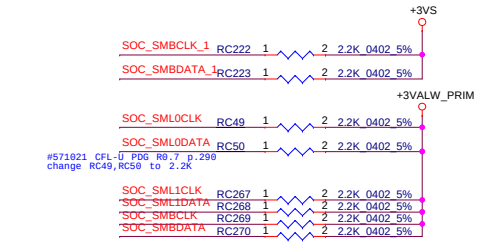
#595182 P38

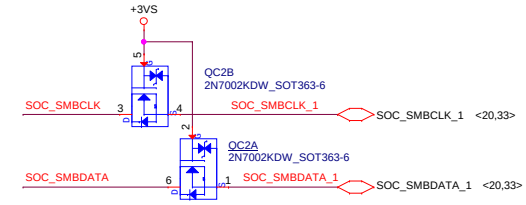


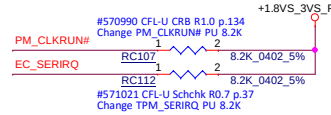
Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.			
Title	WHL-U(2/12)DDR4		
Size: Custom	Document Number: EH7LW M/B LA-H791P		Rev: 0.2
Date: Thursday, June 06, 2019	Sheet 8 of 57		







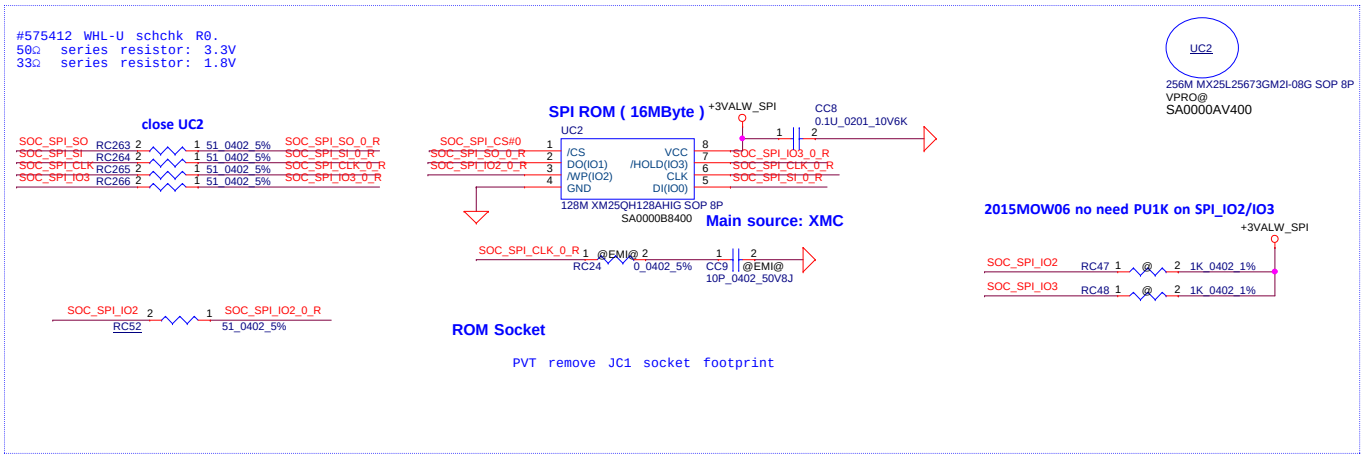


SML0ALERT# / GPP_C5 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

eSPI or LPC
***0 = LPC is selected for EC --> For KB9022/9032 Use**
1 = eSPI is selected for EC --> For KB9032 Only.

SMBALERT# / GPP_C2 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

TLS Confidentiality
***0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)**
1 = Enable Intel ME Crypto (TLS) (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: WHL-U(3/12)SPI,ESPI,SMB,LPC

Size	Document Number	Rev
Custom	EH7LW M/B LA-H791P	0.2

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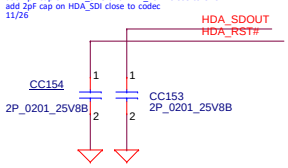
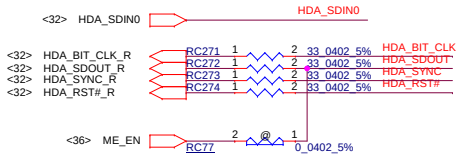
#575412 WHL DG p292_
add 2pF cap on HDA_SDO and HDA_RST# close to CPU
add 2pF cap on HDA_SDI close to codec
11/26



HDA for AUDIO



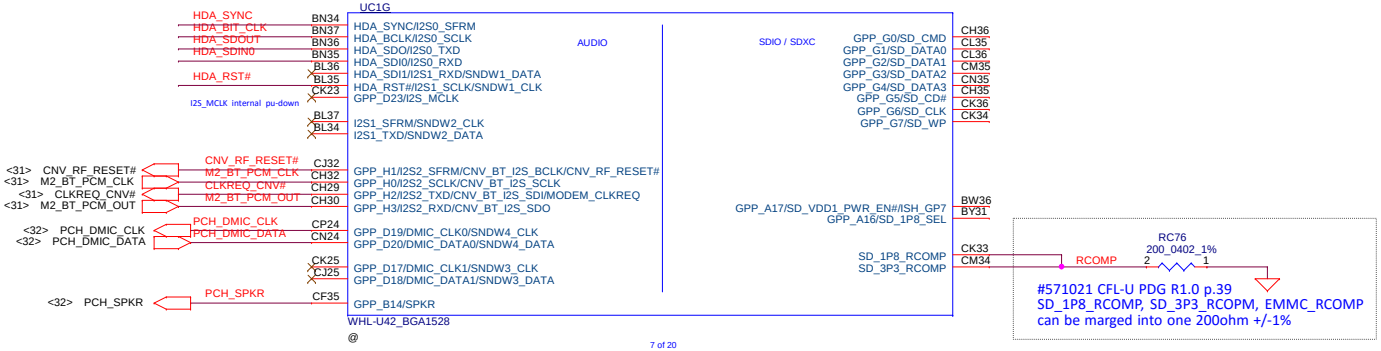
HDA_SDO / I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override
0 = Enable security measures def i nedi nt he fl as h Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external

pull-up in manufacturing/debug environments ONLY.

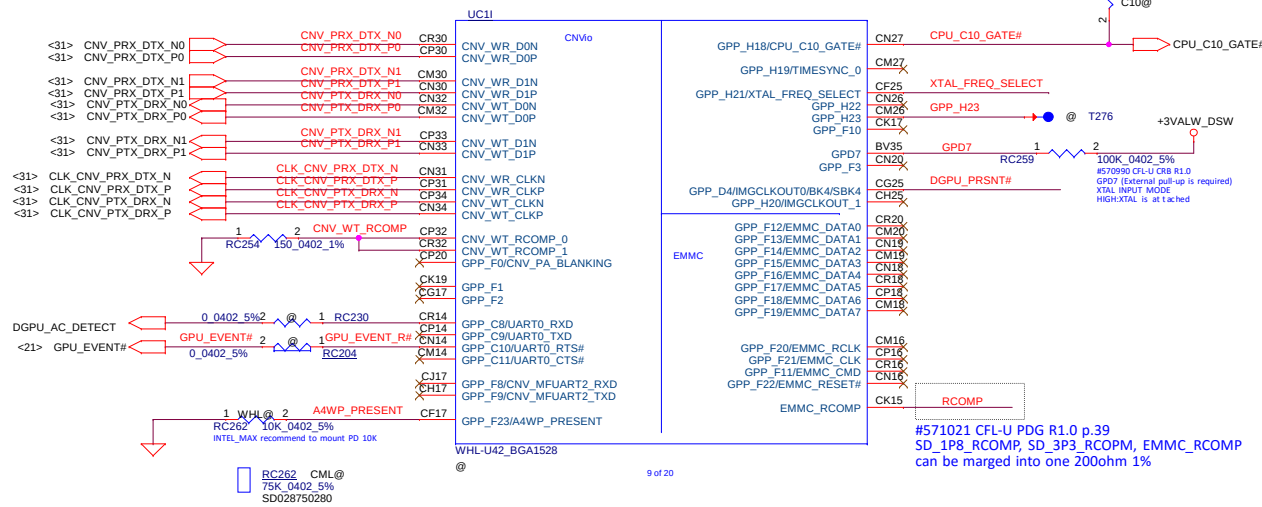
SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

TOP Swap Override
*** 0 = Disable TOP Swap mode.**
1 = Enable TOP Swap Mode.

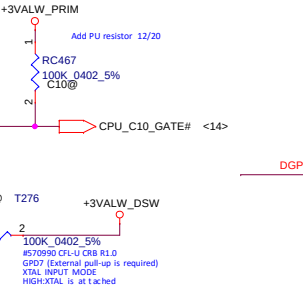
Intel HD Audio link capabilit i es
> Two SDI signals to support two external codecs.
> Drivers variable requency (5MHz to 24MHz) BCLK to support:
-- SDO double pumped up to 48 Mb/s
-- SDI's single pumped up to 24 Mb/s
> Provides cadence for 44.1 kHz based sample rate output.
> Support 1.5V, 1.8V, and 3.3V modes.



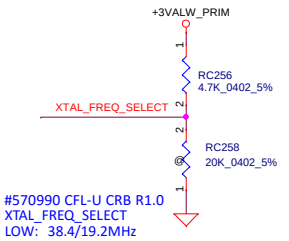
#571021 CFL-U PDG R1.0 p.39
SD_1P8_RCOMP, SD_3P3_RCOPM, EMMC_RCOMP can be marged into one 200ohm +/-1%



#571021 CFL-U PDG R1.0 p.39
SD_1P8_RCOMP, SD_3P3_RCOPM, EMMC_RCOMP can be marged into one 200ohm 1%



	DGPU_PRSNT#
DIS,Optimus	0
UMA	1



#570990 CFL-U CRB R1.0
XTAL_FREQ_SELECT
LOW: 38.4/19.2MHz
HIGH: 24MHz

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: WHL-U(4/12)HDA,EMMC,SDIO,CNVI

Size	Document Number	Rev
Custom	EH7LW M/B LA-H791P	0.2

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#575412 P31

+RTCVCC

RC91 1 2 20K_0402_5% SOC_SRTCRST#

CC10 1 2 1U_0201_6.3V6M

RC93 1 2 20K_0402_5% SOC_RTCRST#

SOC_RTCRST# <36>

CC11 1 2 1U_0201_6.3V6M

JCMOS1 1 @ 2 0_0603_5%

CLR CMOS

Place at RAM DOOR

RC941 2 1M_0402_5% SM_INTRUDER#

+3VS

RC121 1 2 10K_0402_5% CLKREQ_PCIE#1

R115 1 2 10K_0402_5% CLKREQ_PCIE#0

RC282 2 1 10K_0402_5% CLKREQ_PCIE#5

RC281 2 1 10K_0402_5% CLKREQ_PCIE#4

RC280 2 1 10K_0402_5% CLKREQ_PCIE#3

RC279 2 1 10K_0402_5% CLKREQ_PCIE#2

+1.05V_VCCST

From EC(open-drain)

RC113 1K_0402_5%

RC116 62_0201_1%

<36,40> EC_VCCST_PG_R

EC_VCCST_PG

#575412 WHL DG p274 change to 62 1% resistor 11/26

+3VALW_PRIM

+3VALW_DSW

RC277 2 1 10K_0402_5% SYS_RESET#

RC278 2 1 10K_0402_5% LAN_WAKE#

RC275 2 1 10K_0402_5% PCH_PWROK

RC276 2 1 10K_0402_5% EC_RSMRST#

RC110 2 1 10K_0402_5% SYS_PWROK

+3VALW_DSW

RC104 1 2 1K_0402_5% WAKE#

#575412 WHL-U schchecklist R0.8
1 Kohm pull-up to VCCDSW_3p3.
The pull-up is required even if PCIe* interface is not used on the plat f or m

ESD@ 1000P_0402_50V7K

CC131 EC_VCCST_PG

@ESD@ .1U_0402_16V7K CC51 SYS_RESET#

ESD@ 1000P_0402_50V7K CC50 H_CPUPWRGD

ESD@ .1U_0402_16V7K CC66 SYS_PWROK

ESD@ 1000P_0402_50V7K CC65 PCH_PWROK_R

ESD@ .1U_0402_16V7K CC69 EC_RSMRST#

#543016 PDG2.0 P.599
PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the plat f or m

For layout routing ,PCIE CLK P0/P3 exchange

M.2/SSD

<31> CLK_PCIE_N0
<31> CLK_PCIE_P0
<31> CLKREQ_PCIE#0

GLAN

<30> CLK_PCIE_N1
<30> CLK_PCIE_P1
<30> CLKREQ_PCIE#1

WLAN

<31> CLK_PCIE_N2
<31> CLK_PCIE_P2
<31> CLKREQ_PCIE#2

DGPU

<21> CLK_PCIE_N3
<21> CLK_PCIE_P3
<21> CLKREQ_PCIE#3

UC1J

CLOCK SINGNALS

CLK_PCIE_N0 AW2
CLK_PCIE_P0 AY3
CLKREQ_PCIE#0 CF32
CLK_PCIE_N1 BC1
CLK_PCIE_P1 BC2
CLKREQ_PCIE#1 CE32
CLK_PCIE_N2 BD3
CLK_PCIE_P2 BC3
CLKREQ_PCIE#2 CF30
CLK_PCIE_N3 BH3
CLK_PCIE_P3 BH4
CLKREQ_PCIE#3 CE31
CLKREQ_PCIE#4 BA1 BA2 CE30
CLKREQ_PCIE#5 BE1 BE2 CF31

CLKOUT_PCIE_N_0
CLKOUT_PCIE_P_0
GPP_B5/SRCCLKREQ0#
CLKOUT_PCIE_N_1
CLKOUT_PCIE_P_1
GPP_B6/SRCCLKREQ1#
CLKOUT_PCIE_N_2
CLKOUT_PCIE_P_2
GPP_B7/SRCCLKREQ2#
CLKOUT_PCIE_N_3
CLKOUT_PCIE_P_3
GPP_B8/SRCCLKREQ3#
CLKOUT_PCIE_N_4
CLKOUT_PCIE_P_4
GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N_5
CLKOUT_PCIE_P_5
GPP_B10/SRCCLKREQ5#

CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
GPD8/SUSCLK
XTAL_IN
XTAL_OUT
XCLK_BIASREF
CLKIN_XTAL
RTCX1
RTCX2
SRTCRST#
RTCRST#

AU1 CLK_CPU_ITP# T164 @
AU2 CLK_CPU_ITP T165 @
BT32 SUSCLK SUSCLK <31>
CK3 SOC_XTAL24_IN
CK2 SOC_XTAL24_OUT
CJ1 XCLK_BIASREF
CM3
BN31 SOC_RTCX1
BN32 SOC_RTCX2
BR37 SOC_SRTCRST#
BR34 SOC_RTCRST#

WHL-U42_BGA1528
@
10 of 20

SOC_XTAL24_IN RC235 1 2 33_0402_1% SOC_XTAL24_IN_R

SOC_XTAL24_OUT RC236 1 2 33_0402_1% SOC_XTAL24_OUT_R

563377 Intel MOW 33

#575412 WHL DG p268 change to 200K 1% resistor 11/26

RC92 2 1 200K_0402_1%

YC1 24MHZ_18PF_XRCGB24M000F2P51R0

NC NC

CC12 27P_0402_50V8J

CC13 27P_0402_50V8J

REFCLK_CNV <31>

RC255 10K_0402_5%

#575412 P46
PD 60 ohm

XCLK_BIASREF RC136 1 2 60.4_0402_1%

XCLK_BIASREF
T:50ohm S:12/15 L:1000 Via:2

2014MOW48:
Skylake-U use 24M 50 ohm ESR
Cannonlake U use 38.4M 30 ohm ESR

SOC_RTCX2

SOC_RTCX1 RC98 1 2 10M_0402_5%

YC2 32.768KHZ_9PF_X1A000141000200

Change PN to SJ10000Q400

CC15 6.8P_0402_50V8C

CC16 6.8P_0402_50V8C

+3VALW_PRIM

EXT_PWR_GATE# RC295 100K_0402_5%
PM_SLP_S0# RC296 100K_0402_5%
PM_SLP_S3# RC297 100K_0402_5%
PM_SLP_S4# RC298 100K_0402_5%
PM_SLP_A# RC299 100K_0402_5%
SLP_WLAN# RC300 100K_0402_5%
SLP_SUS# RC301 100K_0402_5%
SLP_LAN# RC302 100K_0402_5%

INTEL WHL-U Schchecklist R0.9

UC1K

SYSTEM POWER MANAGEMENT

<36,37> PLT_RST# PLT_RST# BJ35
SYS_RESET# CN10
<36> EC_RSMRST# EC_RSMRST# BR36
T95 @ H_CPUPWRGD AR2
EC_VCCST_PG BJ2
T89 @ SYS_PWROK CR10
PCH_PWROK_R BP31
RC20 10_0402_5% PCH_DPWROK BP30
<36> SUSPWRDNACK SUSPWRDNACK BV34
SUSACK# BV32
T92 @ WAKE# BU30
LAN_WAKE# BU32
BU34

GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGOOD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC

GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SPL_WLAN#
GPD6/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#
INPUT3VSEL

BJ37 PM_SLP_S0# PM_SLP_S0# <36,37>
BU36 PM_SLP_S3# PM_SLP_S3# <36,40>
BU27 PM_SLP_S4# PM_SLP_S4# <36,40>
BT29 PM_SLP_S5# @ T84
BU29 SLP_SUS#
BT31 SLP_LAN# @ T90
BT30 SLP_WLAN# @ T87
BU37 PM_SLP_A# @ T290
@ T291
BU28 PBTN_OUT#_R
BU35 AC_PRESENT
BV36 PM_BATLOW# AC_PRESENT <36>
BR35 SM_INTRUDER#
CC37 EXT_PWR_GATE#
CC36 SOC_VRALERT# @ T93
BT27 INPUT3VSEL

WHL-U42_BGA1528
@
11 of 20

PCH internal PU

PBTN_OUT#_R RC111 1 @ 2 100K_0402_5%

EC internal PU

AC_PRESENT RC106 1 @ 2 10K_0402_5%

PM_BATLOW# RC103 1 2 10K_0402_5%

Default : GPI

SOC_VRALERT# RC115 2 @ 1 10K_0402_5%

PCH PLTRST Buffer

<36> PBTN_OUT# RC109 2 @ 1 PBTN_OUT#_R 0_0402_5%

EC_RSMRST# RC114 2 @ 1 PCH_DPWROK 0_0402_5%

SYS_PWROK RC122 2 @ 1 PCH_PWROK 0_0402_5%

+3VS

PLT_RST# UC3 MC74VHC1G08DFT2G_SC70-5 PLT_RST_BUF#

PLT_RST_BUF# <21,30,31>

RC118 100K_0402_5%

RC125 2 @ 1 0_0402_5%

PLT_RST_BUF# CC130 100P_0402_50V8J ESD@

Reserved for ESD place near UC2.1

+3VALW_DSW

RC260 @ 4.7K_0402_5%

INPUT3VSEL

RC261 4.7K_0402_5%

#570990 CFL-U CRB R1.0
INPUT3VSEL
L : supply is 3.3V +- 5%
H : supply is 3.0V +- 5%

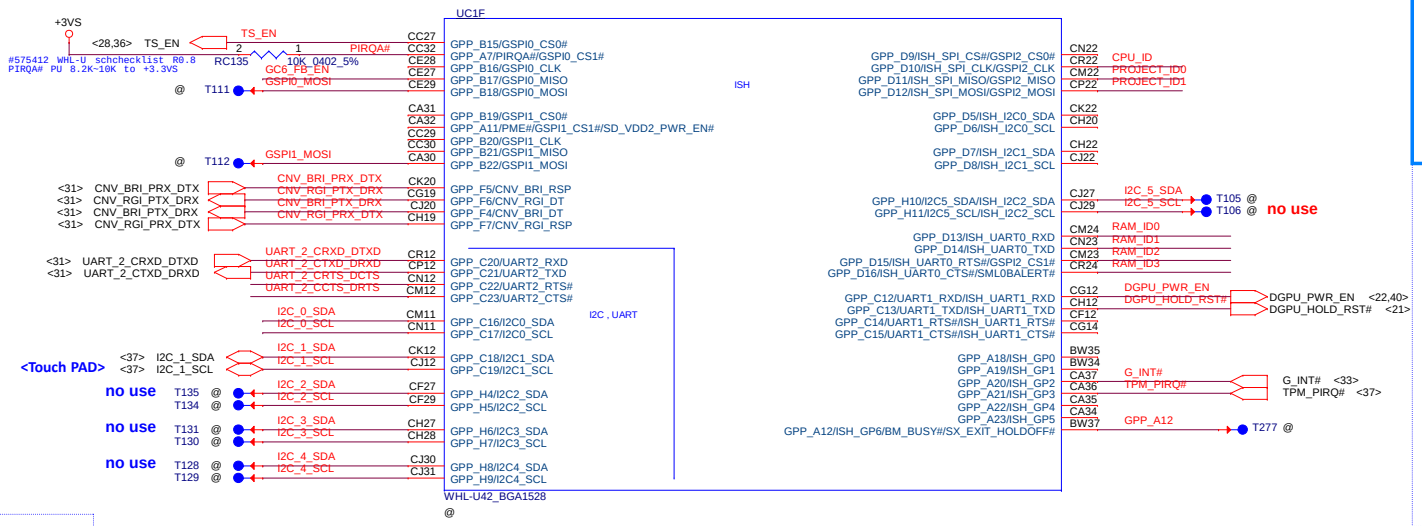
Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: WHL-U(5/12)CLK,GPIO

Size: Custom | Document Number: EH7LW M/B LA-H791P | Rev: 0.2

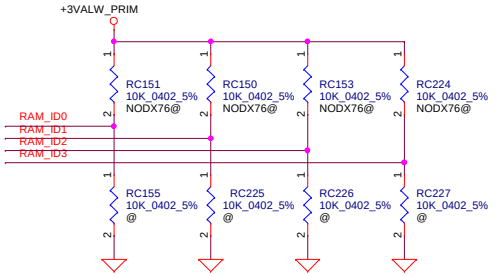
Date: Thursday, June 06, 2019 | Sheet 11 of 57

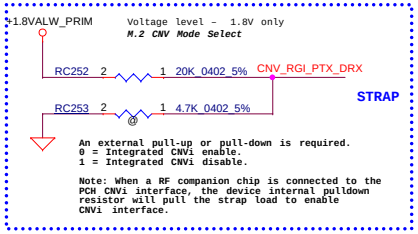


	CPU_ID
WHL	1
CML	0

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
* EH7LW/FH7LC	0	0
EH5LW/FH5LC	0	1
NA	1	0
FH5TW	1	1

Memory Down Strap





Functional Strap Definitions

GSPI0_MOSI /GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

***0 = Disable No Reboot mode. --> AAX05 Use**
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

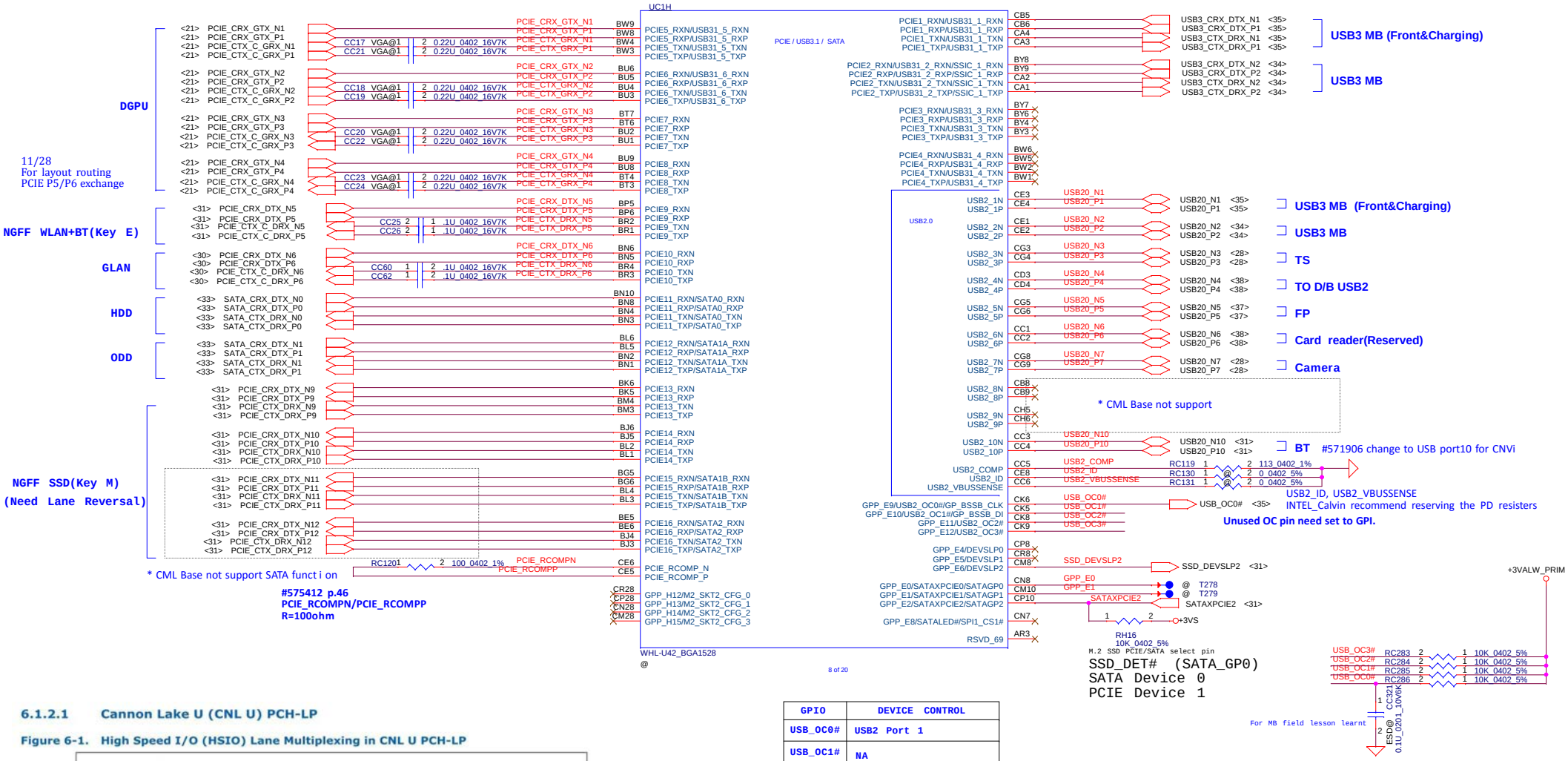
GSPI1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
***0 = SPI Mode --> AAX05 Use**
1 = LPC Mode

ZZZ1 X76DHYN@ Hynix4GB X76829BOL04
ZZZ2 X76DMIC@ Micron4GB X76829BOL05
ZZZ3 X76DSAM@ Samsung4GB X76829BOL06

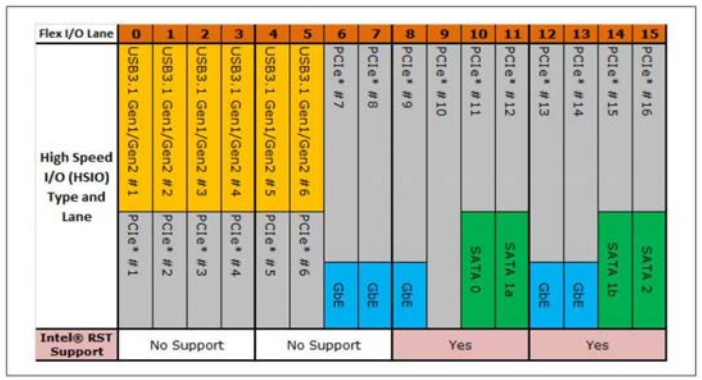
	RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description
Hynix 4GB	0	0	0	0	SA0000BMN30 (S IC D4 512M16 H5AN8G6NCJR-VKC FBGA ABO!)
Micron 4GB	0	0	0	1	SA0000ARD60 (S IC D4 8G/2666 MT40A512M16LY-075:E ABO!)
Samsung 4GB	0	0	1	0	SA0000B6F00 (S IC D4 512M16 K4A8G165WC-BCTD FBGA 96P)
	0	0	1	1	
No OnBoard Memory	1	1	1	1	No On Board Memory

Compal Electronics, Inc.
Title: WHL-U(6/12)GPIO
Size: Custom | Document Number: EH7LW M/B LA-H791P | Rev: 0.2
Date: Thursday, June 06, 2019 | Sheet 12 of 57



6.1.2.1 Cannon Lake U (CNL U) PCH-LP

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP



GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

DEVSLP[2:0] Implementation
DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.
The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.
• When high, DEVSLP requests the SATA device to enter into the DEVSLP power state
• When low, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals
•The processor provides three SATA general purpose input signals SATAGP[2:0] for SKL U. These signals can be configured as interlock switch inputs corresponding to a given SATA port.
• When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.
If mechanical presence switches will not be used on the platform SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

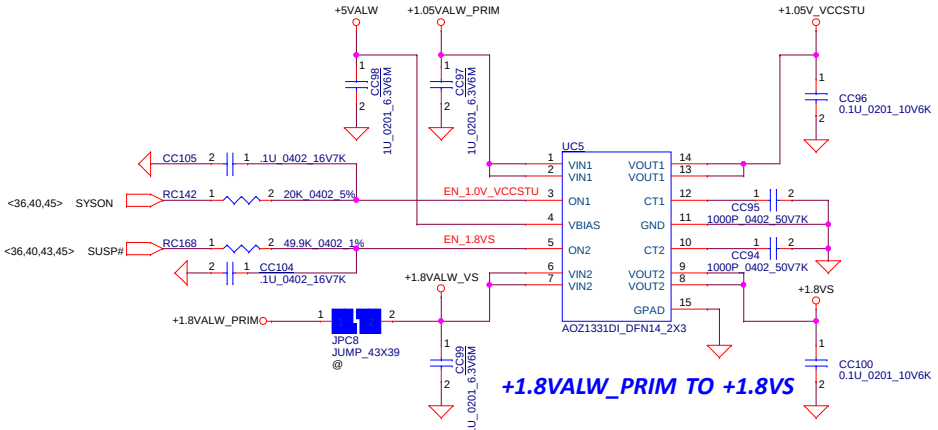
Compal Electronics, Inc.

Title: WHL-U(7/12)PCIE,USB,SATA

Size: Custom | Document Number: EH7LW M/B LA-H791P | Rev: 0.2

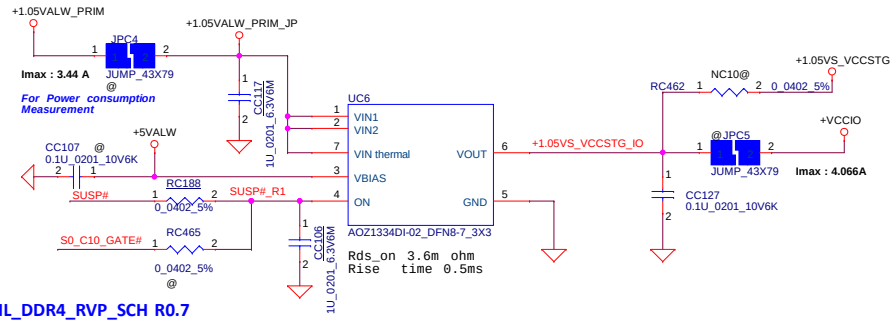
Date: Thursday, June 06, 2019 | Sheet 13 of 57

+1.05VALW_PRIM TO +1.05V_VCCSTU / +1.05VCCST

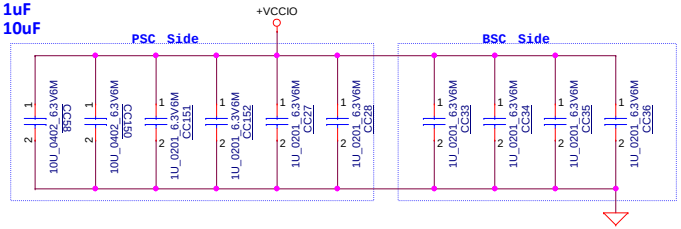


+1.8VALW_PRIM TO +1.8VS

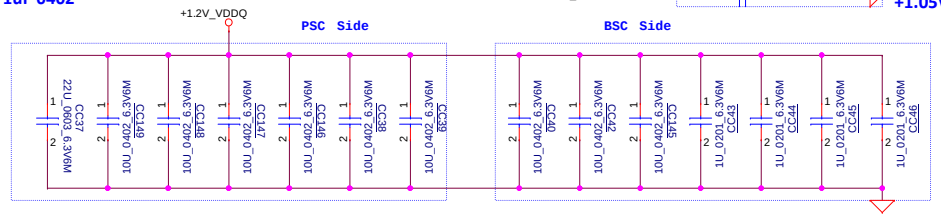
+1.05VALW_PRIM TO +1.05VS_VCCSTG

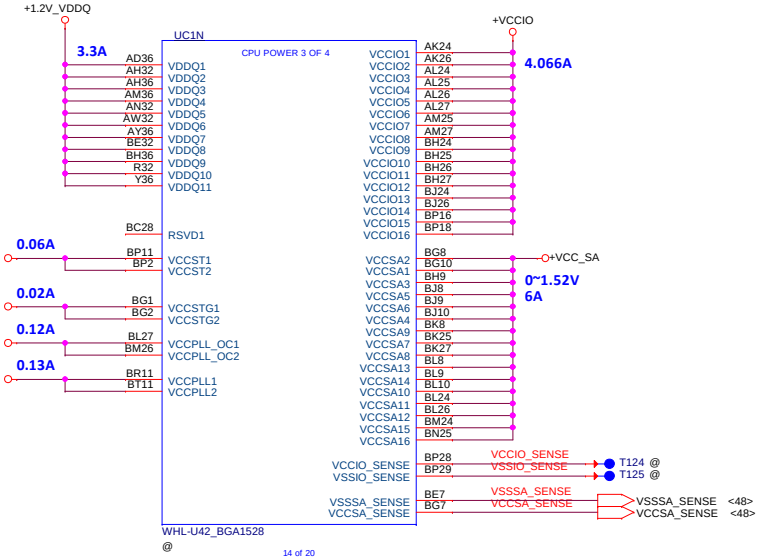


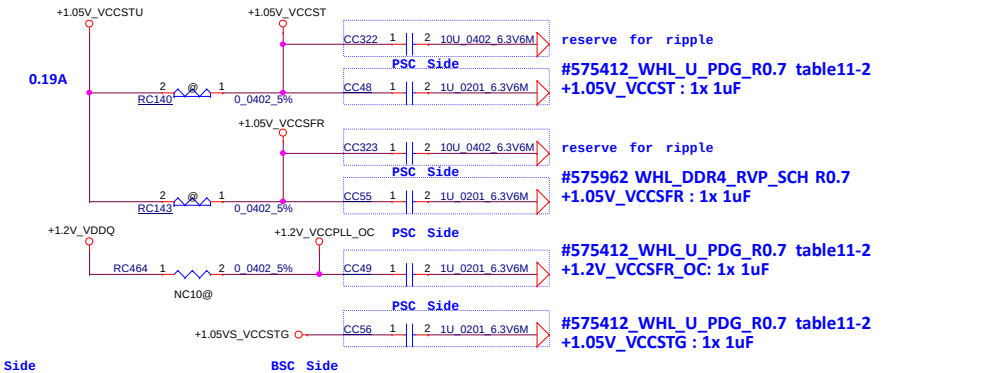
#575962 WHL_DDR4_RVP_SCH R0.7
+VCCIO :
8 x 1uF
2 x 10uF

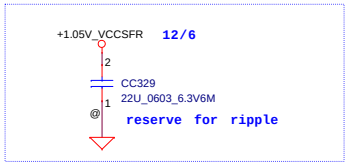


#575412_WHL_U_PDG_R0.7 table11-2
+1.2V_VDDQ_CPU:
9 x 10uF 0402
1 x 22uF 0603
4 x 1uF 0402



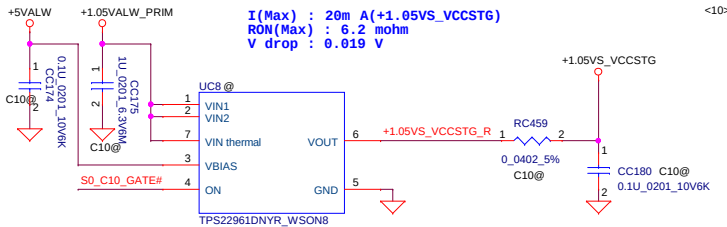


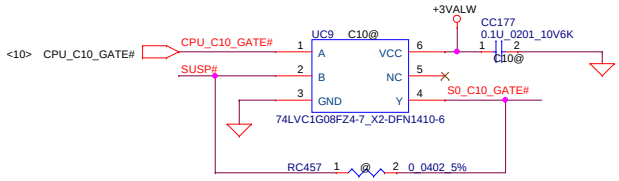




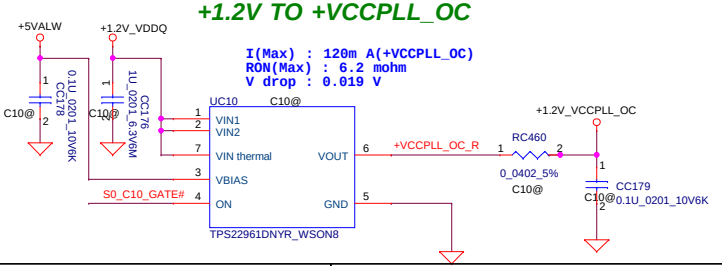
CPU C10 Save Power

+1.05VALW TO +1.05VS_VCCSTG





+1.2V TO +VCCPLL_OC



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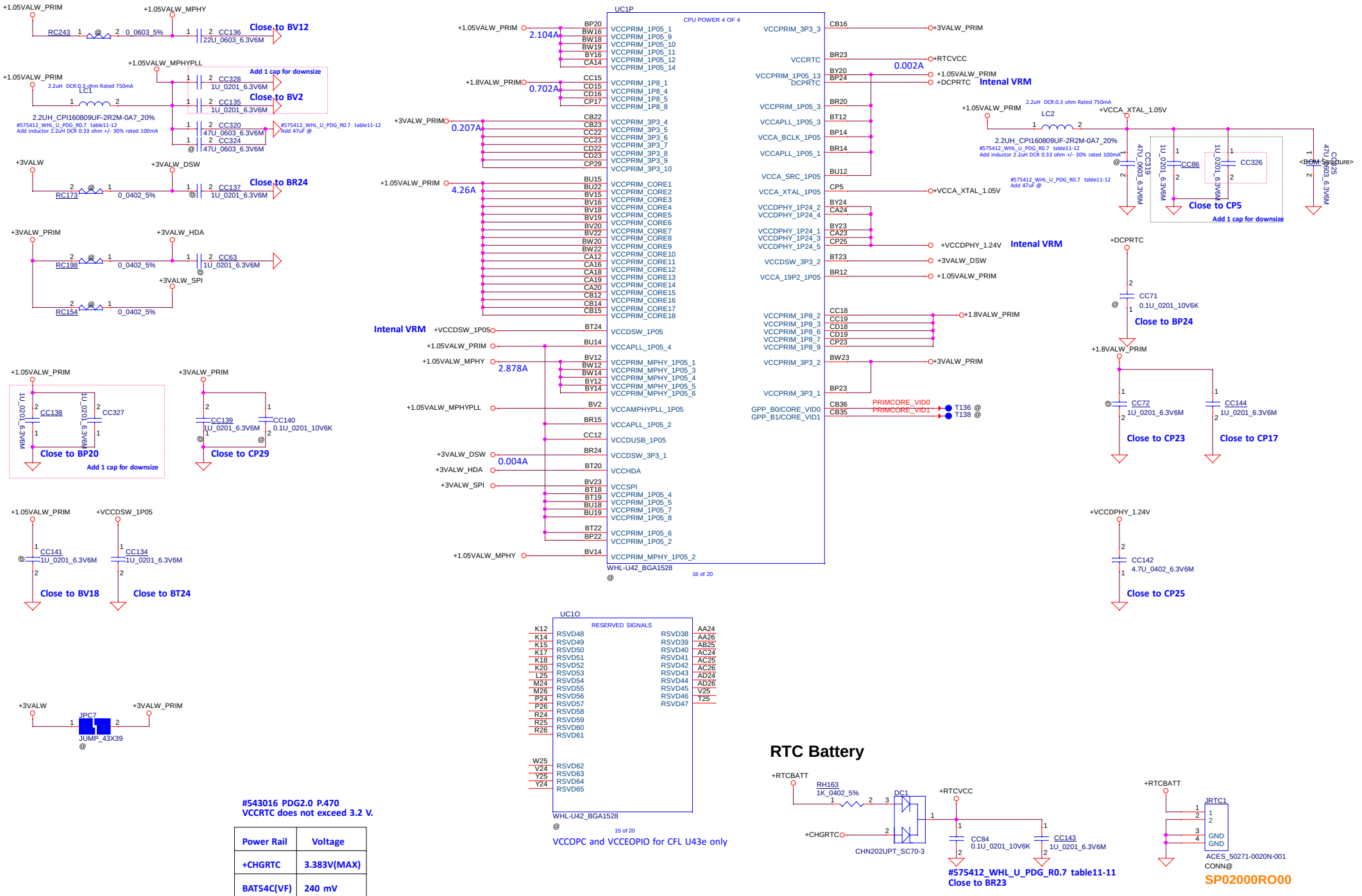

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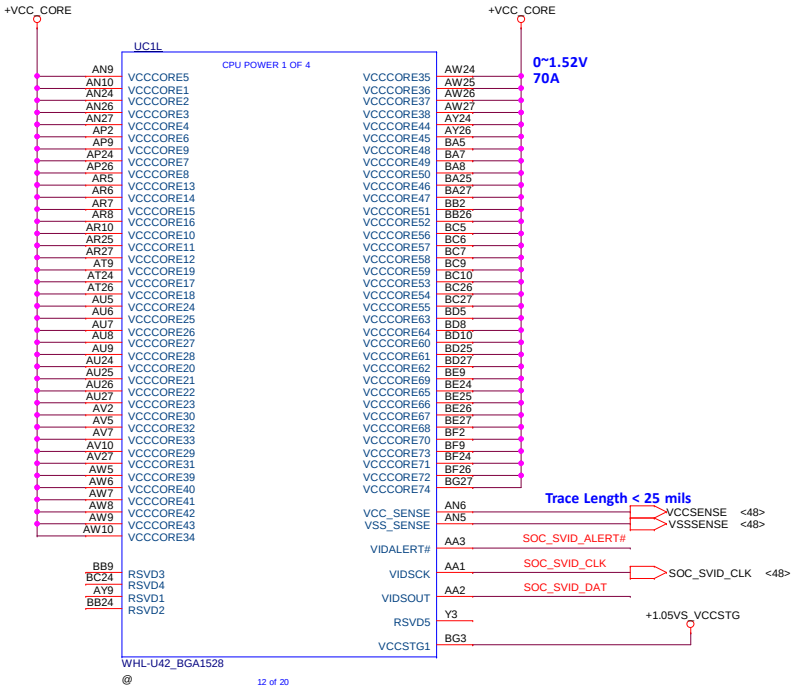

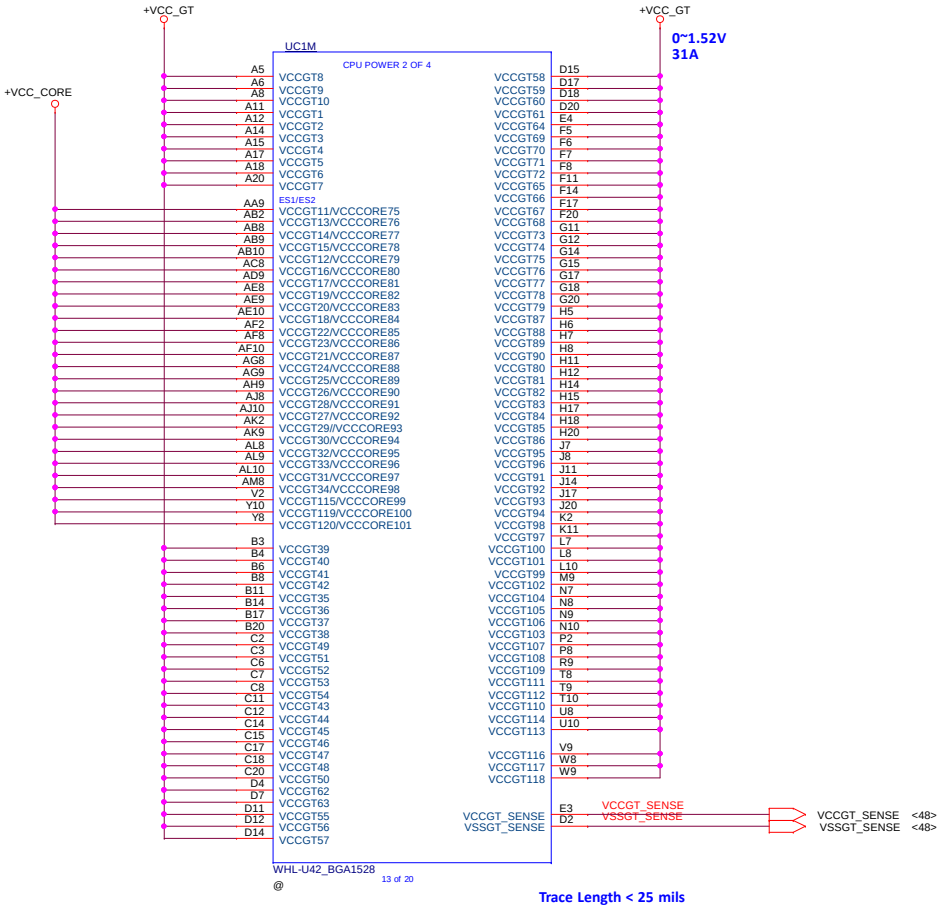

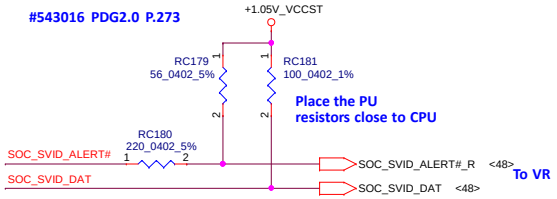

Processor Power Rails

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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Title: WHL-U(10/12)Power,SVID

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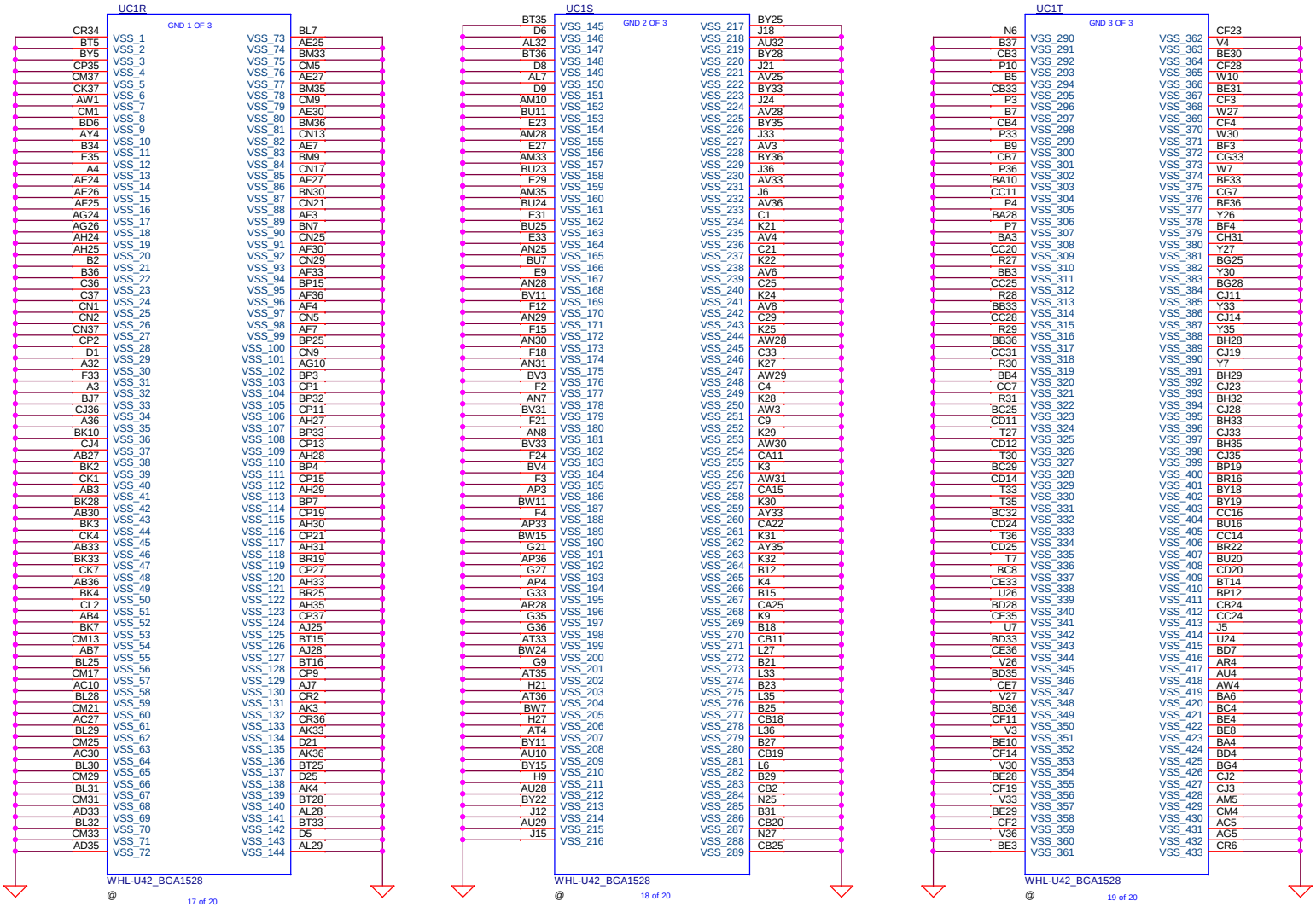

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Title: **WHL-U(11/12)GND**

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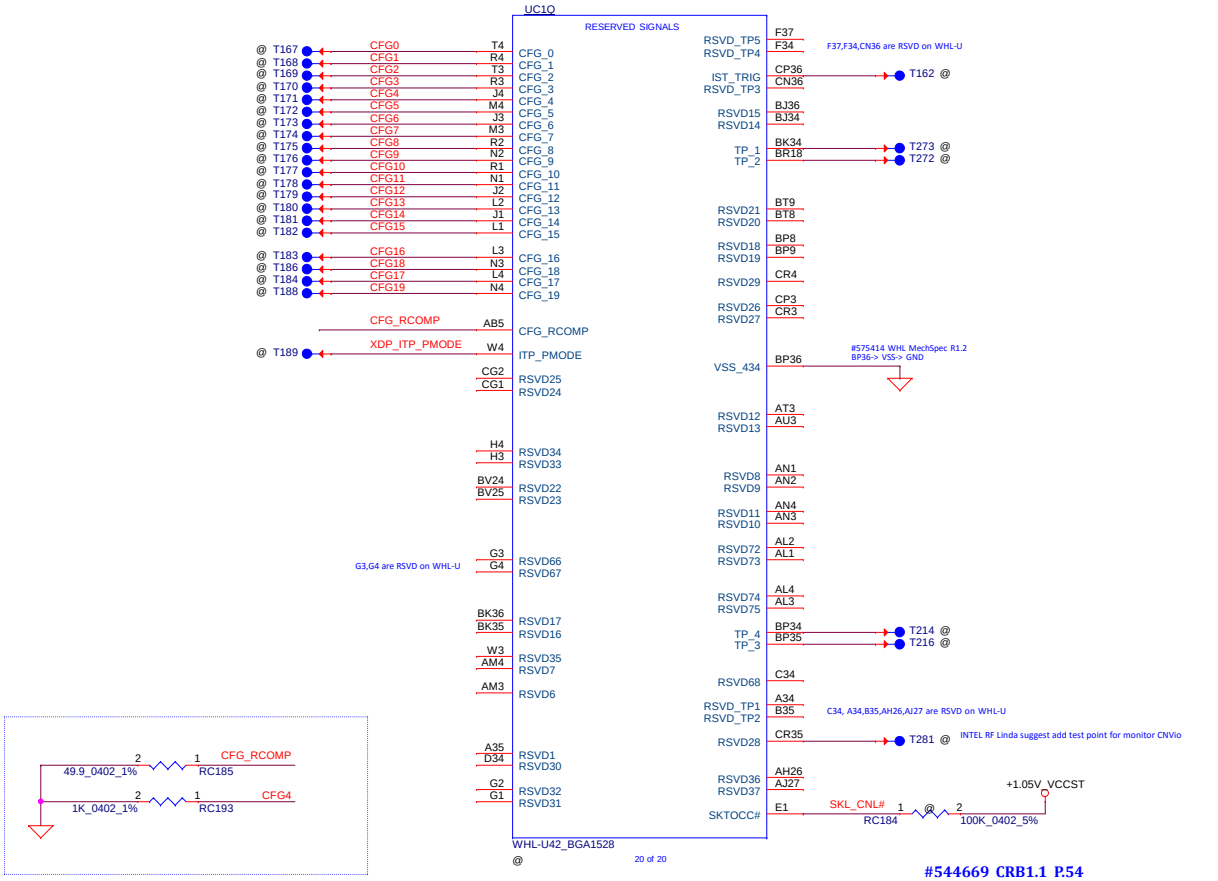

#544669 CRB1.1 P.54
#544924 SKL EDS1.2 P.125
PROC_SELECT#
This pin is for compatibility with future platforms. It should be unconnected for the processor.

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Title: WHL-U(12/12)RSVD

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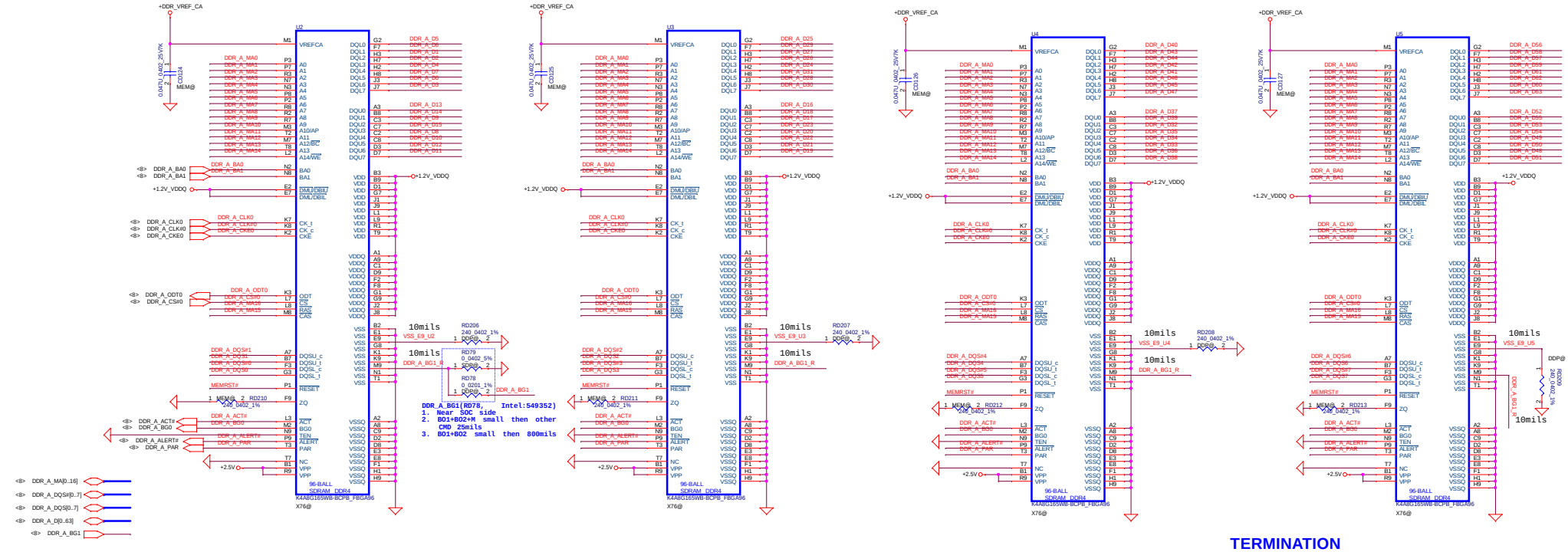


DDR4 mapping	SDP	DDP
E9	VSS	UZQ
M9	VSS	BG1
T7	NC	VSS
RCOMP[0] (SOC side)	200_1%	121_1%

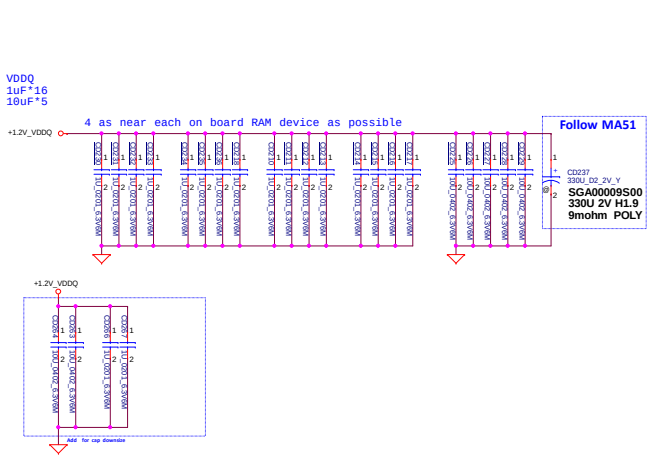
SDP@ RD206 0_0402_5% SD028000080

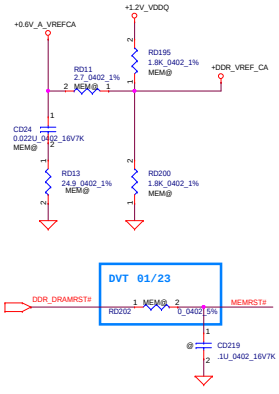
SDP@ RD208 0_0402_5% SD028000080

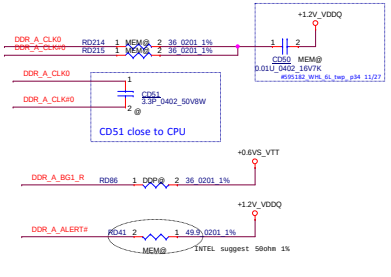
SDP@ RD207 0_0402_5% SD028000080

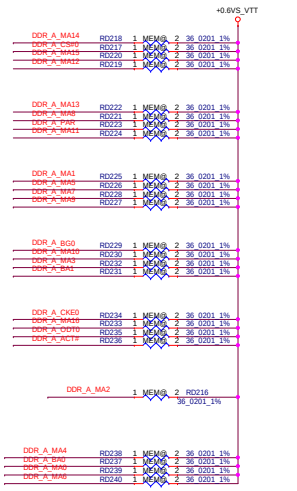
SDP@ RD209 0_0402_5% SD028000080

TERMINATION

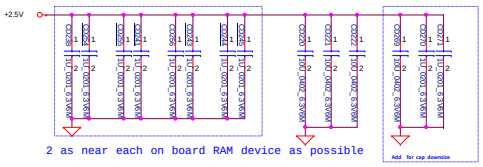




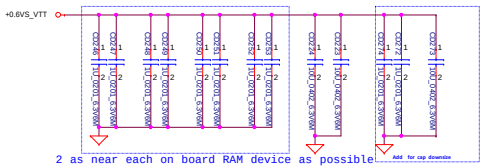




VPP
1uF*8
10uF*3



VTT
1uF*8
10uF*2



Page12

	RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description
Hynix 4GB	0	0	0	0	SA0000A1H20 (S IC D4 512M16 H5AN8G6NAFR-UHC FBGA ABO!)
Micron 4GB	0	0	0	1	SA00009V220 (S IC D4 512M16 MT40A512M16JY-083E:B ABO!)
Samsung 4GB	0	0	1	0	SA00009U420 (S IC D4 512M16 K4A8G165WB-BCRC FBGA 96P ABO !)
	0	0	1	1	
No OnBoard Memory	1	1	1	1	No On Board Memory

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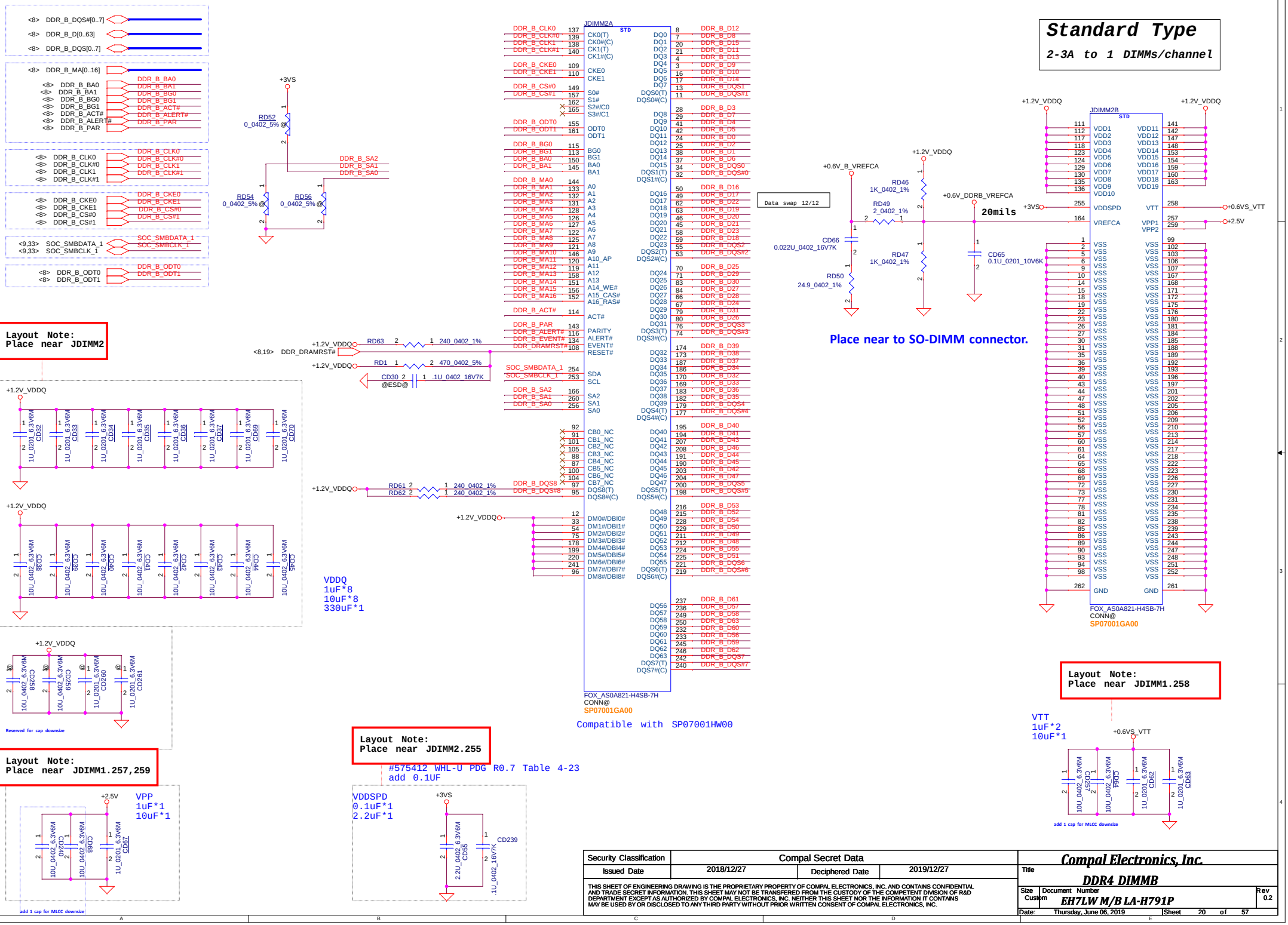
Standard Type

2-3A to 1 DIMMs/channel



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Title: **DDR4 DIMMB**

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N16 GPU		
GPIO	I/O	USAGE
GPIO0	O	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	THERM_ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16	I	FRAME_LOCK#
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		

N17 GPU		
GPIO	I/O	USAGE
GPIO0	O	PWM_VID
GPIO1	O	GC6_FB_EN
GPIO2	I	GPU_EVENT#
GPIO3	I/O	NVVDDS_PWM
GPIO4	O	1V8_MAIN_EN
GPIO5	I	FRAME_LOCK#
GPIO6	O	PSI
GPIO7	O	LCD_BL_PWM
GPIO8	O	MEM_VDD_CTL
GPIO9	I/O	THERM_ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	LCD_VDD
GPIO12	I	PWR_LEVEL
GPIO13	O	LCD_BLEN
GPIO14	I	HPD_IFPA
GPIO15	I	HPD_IFPB
GPIO16		Reserved
GPIO17	I	HPD_IFPD
GPIO18	I	HPD_IFPE
GPIO19	O	3D_VISION
GPIO20		Reserved
GPIO21		Reserved (OC_WARN)
GPIO22		Reserved
GPIO23		Reserved

DA-08329-001_V02

Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	Population N16	Population N17	Location
PLLVDD (N17: XS_PLLVDD) Supply Rail					
GB2B-64, GB2C-64	0.1 µF X7R	0402	1	1	Under GPU
	22 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=30 Ω (ESR=0.05 Ω)	0402	1	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails					
GB2B-64, GB2C-64	0.1 µF X7R	0402	2	2	Under GPU
	10 µF X5R	0603	1	0	Near GPU
	47 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=300 Ω (ESR=0.2 Ω)	0603		0	Near GPU

GC6 2.0 function

Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

10.2.2 I²CS Slave Address

N16x GPUs use I²CS slave address 0x96h for NVIDIA internal testing. I²C address 0x96h must not be used by other I²C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter

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Title: N17S PEG 1/7

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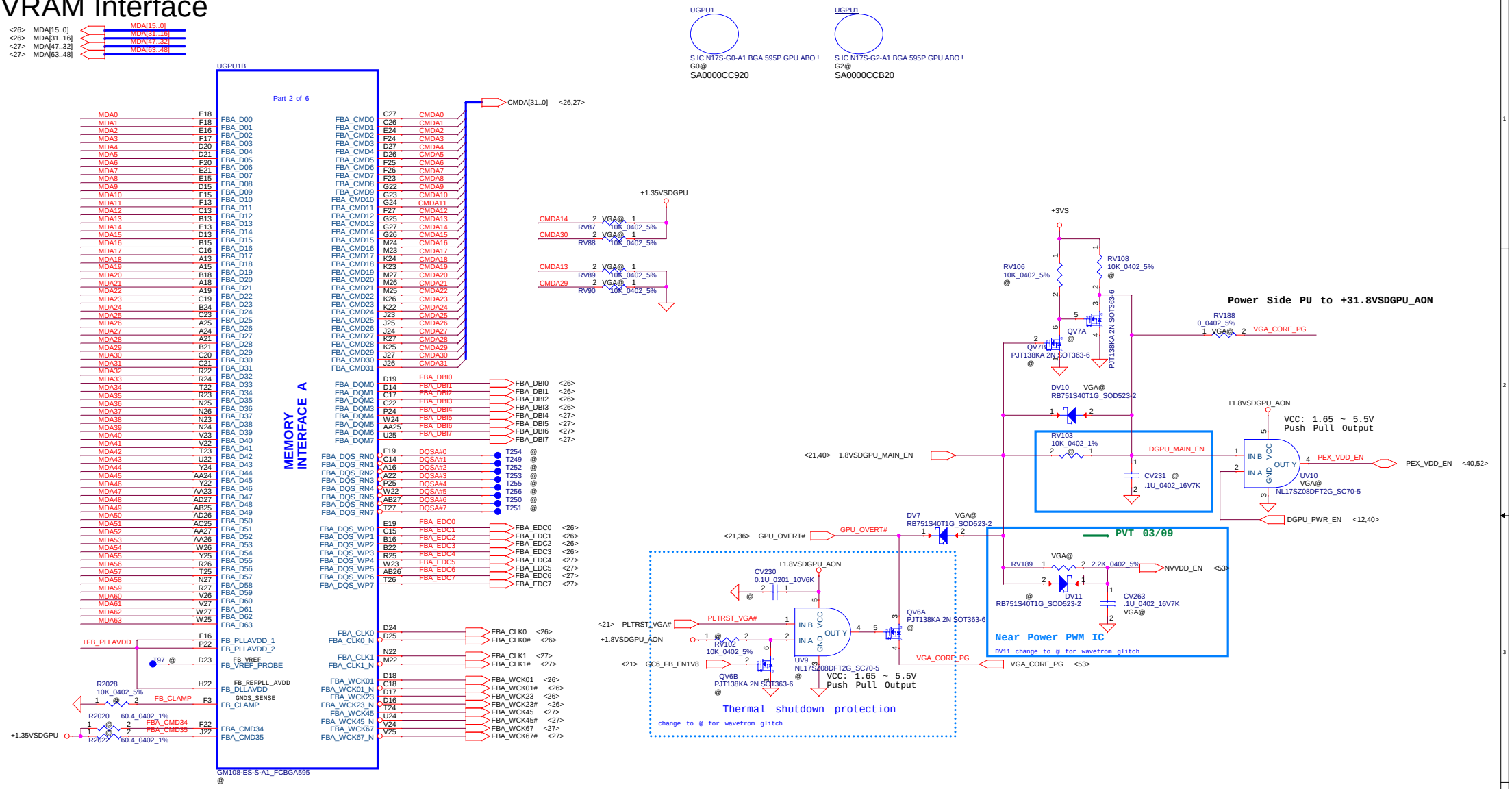
VRAM Interface



DA-08329-001_V01

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

NV 15x DG-06803-V03
NV 16x DG-07158-V04

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

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Title: *N17S VRAM 2/7*

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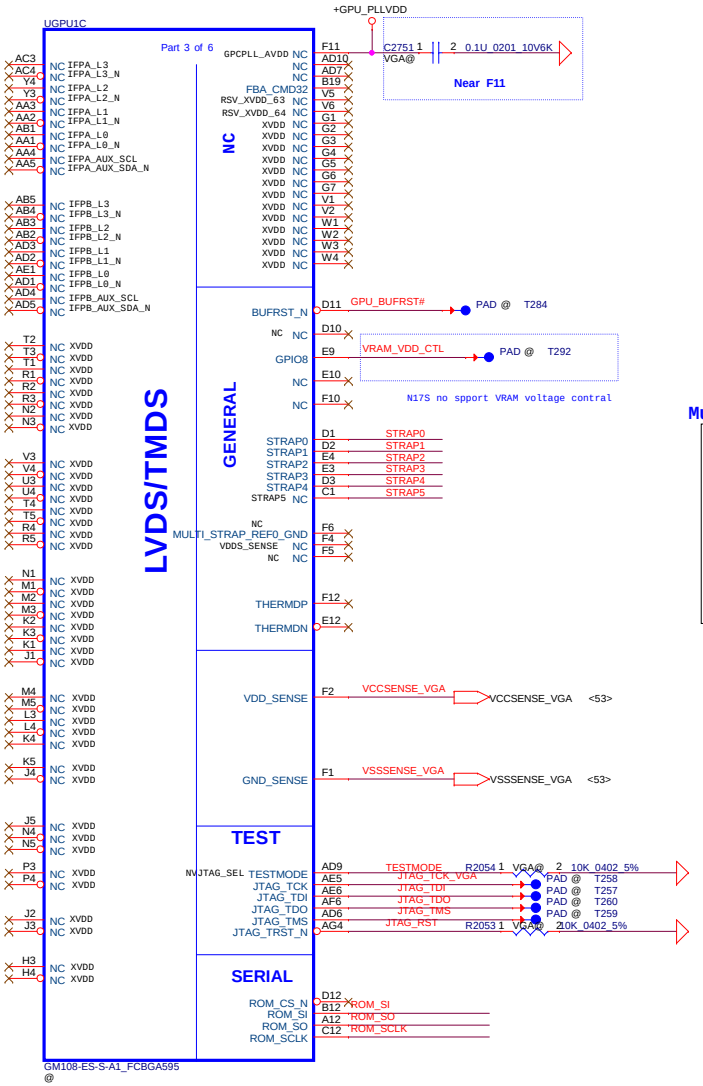
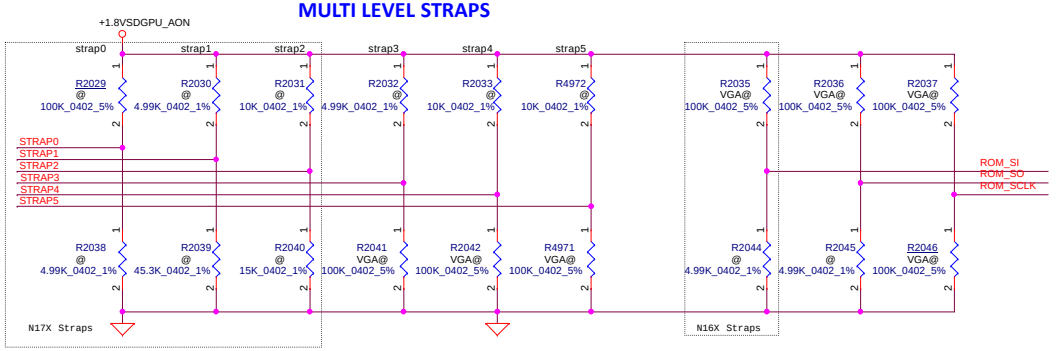


MULTI LEVEL STRAPS



Multi strap table

MX230/250 Decive ID : N17S-G0/G2-A1 0x1D11/0x1D13

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3 strap4 strap5	ROM_SI	ROM_SO	ROM_SCLK
N17S-G0 N17S-G2	+1.35V	SR	X76xxxxxxx	3.0GHz	256Mx32x2 2G	0x4 (SA00009TV50) Micron MT51J256M32HF-70:B	PD 100K	PD 100K	PU 100K	PD 100K	PU 100K	PU 100K	PU 100K PD 100K
						0x5 (SA00009U160) Hynix H5GC8H24AJR-R0C	PU 100K	PD 100K	PU 100K				
						0x0 (SA00009TA10) Samsung K4G80325FB-HC25	PD 100K	PD 100K	PD 100K				
							PD 100K	PD 100K	PD 100K				
							PD 100K	PU 100K	PD 100K				
							PU 100K	PD 100K	PD 100K				

NV 17S DG-07785-001_V07

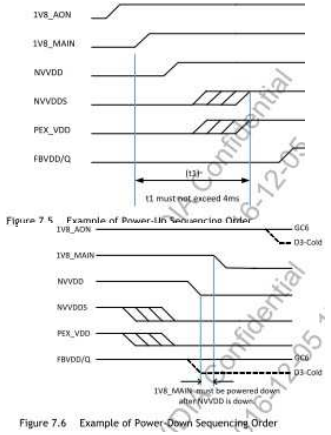


Figure 7.5 Example of Power-Up Sequencing Order

Figure 7.6 Example of Power-Down Sequencing Order

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Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	Population N16	Population N17	Location
PLLVDD (N17: XS_PLLVDD) Supply Rail					
GB2B-64, GB2C-64	0.1 µF X7R	0402	1	1	Under GPU
	22 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L=30 Ω (ESR=0.05 Ω)	0402	1	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails					
GB2B-64, GB2C-64	0.1 µF X7R	0402	2	2	Under GPU
	10 µF X5R	0603	1	0	Near GPU
	47 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L=300 Ω (ESR=0.2 Ω)	0603	1	0	Near GPU
NC (N17: GPCPLL_AVDD) Supply Rail					
GB2C-64	0.1 µF X7R	0402	N/A	1	Under GPU
	4.7 µF X6S	0603	N/A	1	Near GPU
	22 µF X6S	0805	N/A	1	Near GPU
	Bead Type				
	L=30 Ω (ESR=0.010 Ω)	0603	N/A	1	Near GPU

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Title: **N17S LVDS 3/7**

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NV 16x DG-07158-V05

Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint	Population		Location
GB2B-64/GB2-64 DDR3	0.1µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU

DA-08329-001_V02

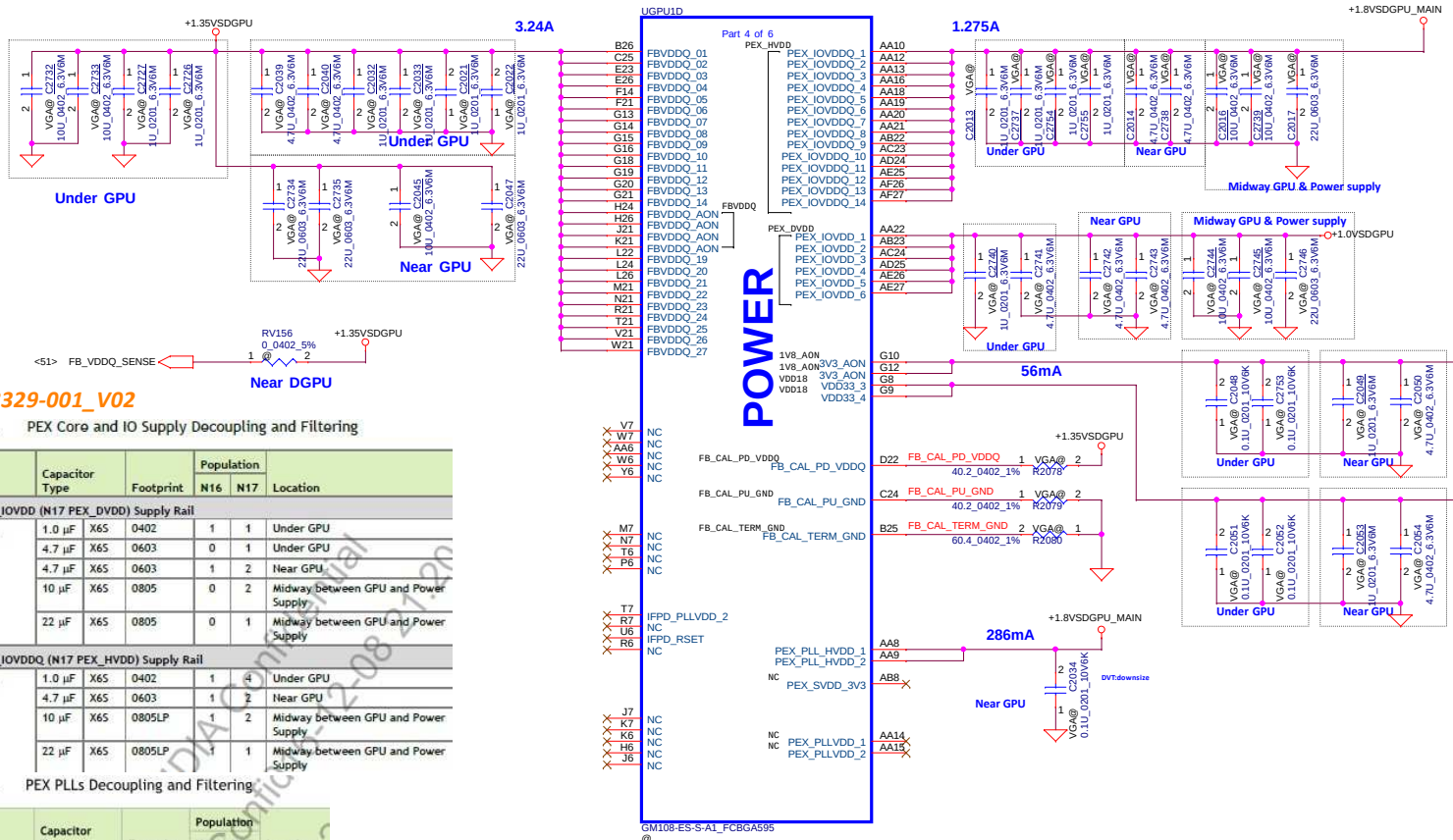
Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

NV 16x DG-07158-V05

Table 3-16. PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply



NV 16x DG-07158-V05

Table 7-13. Default GPU Drive Calibration for Frame Buffer Interface

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
GDDR5/ BGA-170	1.35 V or 1.50 V	40.2 Ω	40.2 Ω	60.4 Ω

NV 16x DG-07158-V05

GPU Package	Rail	Capacitor Type		Footprint	Population		Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU

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Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

Table 7. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
PEX_PLLVDD Supply Rail					
GB2B-64	0.1 µF	X7R	0402	1	N/A	Under GPU
	1.0 µF	X5R	0603	1	N/A	Near GPU
	4.7 µF	X5R	0805	1	N/A	Near GPU
PEX_SVDD_3V3 Supply Rail						
GB2B-64	4.7 µF	X5R	0603	2	N/A	Near GPU
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

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Table 9. VDD AON and VDD_MAIN Decoupling

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 3V3_MAIN (N17 VDD18) Supply Rail					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	2	Under GPU
	1.0 µF	X6S	0603	1	1	Near GPU
	4.7 µF	X6S	0603	1	1	Near GPU
N16 3V3_AON (N17 1V8_AON) Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Under GPU
	1.0 µF	X6S	0603	1	1	Near GPU
	4.7 µF	X6S	0603	1	1	Near GPU

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Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 µF	X7R	0402	1	Near GPU
4.7 µF	X5R	0603	2	Near GPU

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Table 3-17. PEX_PLLVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 µF	X7R	0402	1	Under GPU
1.0 µF	X5R	0603	1	Near GPU
4.7 µF	X5R	0805	1	Near GPU

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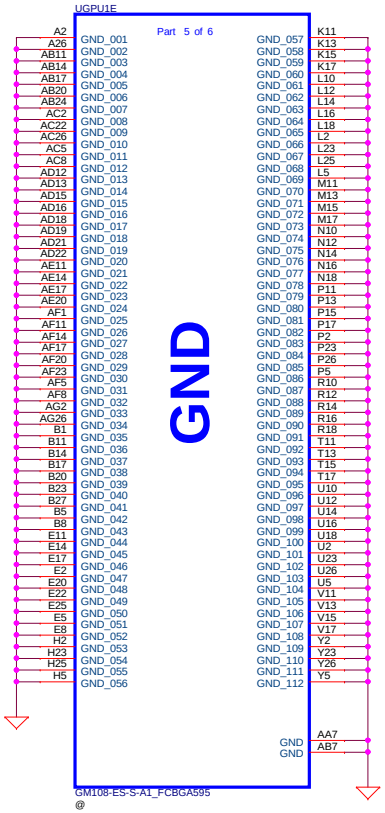

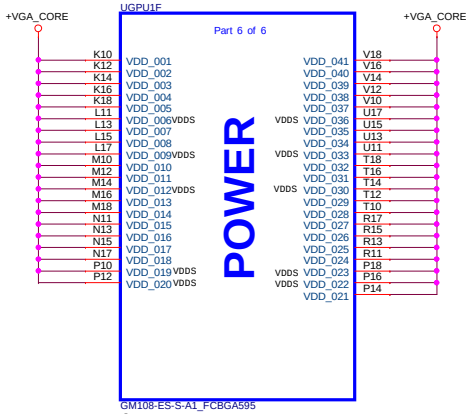

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Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64 / GB2-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

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Table 3. NVVDD and NVVDDS Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
NVVDD Supply Net						
GB2B-64, GB2C-64	4.7 µF	X6S	0603	10	8	Under GPU
	1 µF	X6S	0402	4	3	Under GPU
	47 µF	X5R	0805	1	-	Near GPU
	10 µF	X7R	0805	-	4	Near GPU
	22 µF	X5R	0805	1	3	Near GPU
	4.7 µF	X5R	0805	1	4	Near GPU
	330 µF	POS	7343	1	1	Near GPU
NVVDDS Supply Net						
GB2C-64 Only	4.7 µF	X6S	0603	N/A	4	Under GPU
	1 µF	X6S	0402	N/A	2	Under GPU
	10 µF	X6S	0805	N/A	7	Near GPU
	22 µF	X6S	0805LP	N/A	1	Near GPU
	330 µF	POS	7343	N/A	1	Near GPU

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Table 6. EDP-Continuous [3]

Products	VRAM Type	GPU Core – (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)	3.3V Total 3.3V [4] (A)
N16S-GMR	GDDR5	19.0	–	2.0	–	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5 @ 2.0 GHz	26.5	–	2.0	–	4.2	0.80	0.06
	GDDR5 @ 2.5 GHz	26.5	–	2.0	–	4.7	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

Table 7. EDP-Peak [3]

Products	VRAM Type	GPU Core – (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)
N16S-GMR	GDDR5	34.0	–	2.9	–	6.8	2.1
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1
N16S-GTR	GDDR5 @ 2.0 GHz	53.0	–	2.9	–	6.8	2.1
	GDDR5 @ 2.5 GHz	53.0	–	3.1	–	7.2	2.1
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1

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Table 5. EDP-Continuous [3]

Product	VRAM Type	GPU Core – (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)	3.3V Total 3.3V [4] (A)
N16V-GMR1	GDDR5 @ 2.0 GHz	18.5	–	2.0	–	4.2	0.8	0.06
	GDDR5 @ 2.5 GHz	18.5	–	2.0	–	4.7	0.8	0.06
	DDR3/L	19.0	1.4	1.4	2.4	2.3	0.8	0.06

Table 6. EDP-Peak [3]

Products	VRAM Type	GPU Core – (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)
N16V-GMR1	GDDR5 @ 2.0 GHz	30.0	–	2.9	–	6.8	2.1
	GDDR5 @ 2.5 GHz	31.0	–	3.1	–	7.2	2.1
	DDR3/L	28.5	2.6	2.3	4.1	3.9	2.1

SP-08318-001_V03

Table 7. Output EDP-Continuous

Product	NVVDD – (A)	GPU FBIO 1.35V[4] (A)	FB Total[5] 1.35V[4] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17S-G1	30.0	2.0	3.4	0.1	0.3

Table 8. Output EDP-Peak

Product	NVVDD – (A)	GPU FBIO 1.35V[3] (A)	FB TOTAL[4] 1.35V[3] (A)	1.0V Total[1] 1.0V[3] (A)
N17S-G1	60.1	3.2	6.6	0.2

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VRAM GDDR5 chips

<22,27> MDA[63..0] — MDA[63..0]
<22,27> CMDA[31..0] — CMDA[31..0]

X76 for N17S 2G VRAM

ZZZ X76VSAM@ — Samsung_256Mx32x2 X76829BOL03
ZZZ X76VHYN@ — Hynix_256Mx32x2 X76829BOL01
ZZZ X76VMIC@ — Micron_256Mx32x2 X76829BOL02

GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Channel 0 BOT SIDE

MF=0

UV13 @ — 170-BALL SGRAM GDDR5 — H5GC4H24AJR-R0C_BGA170

MF=0	MF=1	MF=1	MF=0
EDC0	EDC3	DQ24	DQ0
EDC1	EDC2	DQ25	DQ1
EDC2	EDC1	DQ26	DQ2
EDC3	EDC0	DQ27	DQ3
		DQ28	DQ4
		DQ29	DQ5
		DQ30	DQ6
DBI0#	DBI3#	DQ31	DQ7
DBI1#	DBI2#	DQ16	DQ8
DBI2#	DBI1#	DQ17	DQ9
DBI3#	DBI0#	DQ18	DQ10
		DQ19	DQ11
		DQ20	DQ12
		DQ21	DQ13
		DQ22	DQ14
		DQ23	DQ15
BA0/A2	BA2/A4	DQ8	DQ16
BA1/A5	BA3/A3	DQ9	DQ17
BA2/A4	BA0/A2	DQ10	DQ18
BA3/A3	BA1/A5	DQ11	DQ19
		DQ12	DQ20
		DQ13	DQ21
		DQ14	DQ22
		DQ15	DQ23
A8/A7	A10/A0	DQ0	DQ24
A9/A1	A11/A6	DQ1	DQ25
A10/A0	A8/A7	DQ2	DQ26
A11/A6	A9/A1	DQ3	DQ27
A12/RFU/NC		DQ4	DQ28
		DQ5	DQ29
		DQ6	DQ30
		DQ7	DQ31
ABI#	CAS#		
RAS#	WE#		
CS#	RAS#		
WE#	CS#		
WCK01#	WCK23#		
WCK01	WCK23		
WCK23#	WCK01#		
WCK23	WCK01		

BYTE0: MDA0–MDA7
BYTE1: MDA8–MDA16
BYTE2: MDA17–MDA24
BYTE3: MDA25–MDA31

<22> FBA_EDC0–FBA_EDC3 → C2, C13, R13, R2
<22> FBA_DBI0–FBA_DBI3 → D2, D13, P13, P2
<22> FBA_CLK0, FBA_CLK0# → J12, J11; CMDA14 → J3
CMDA2 → H11; CMDA4 → K10; CMDA3 → K11; CMDA1 → H10
CMDA6 → K4; CMDA11 → H5; CMDA10 → H4; CMDA7 → K5; CMDA9 → J5
A5 → U5 VPP/NC; VPP/NC
RV131 2 VGA@ 1 1K_0402_1% → J1; RV132 2 VGA@ 1 121_0402_1% → J13; J10 MF SEN ZQ
CMDA8 → J4; CMDA12 → G3; CMDA0 → G12; CMDA15 → L3; CMDA5 → L12
<22> FBA_WCK01#, FBA_WCK01 → D5, D4
<22> FBA_WCK23#, FBA_WCK23 → P5, P4
A10 → U10 VREFD VREFD VREFC; +FBA_VREFC0 → J14
CMDA13 → J2 RESET#

VDDQ: B1, D1, F1, M1, P1, T1, G2, L2, B3, D3, F3, H3, K3, M3, P3, T3, E5, N5, E10, N10, B12, D12, F12, H12, K12, M12, P12, T12, G13, L13, B14, D14, F14, M14, P14, T14
VSSQ: A1, C1, E1, N1, R1, U1, H2, K2, A3, C3, E3, N3, R3, U3, C4, R4, F5, M5, F10, M10, C11, R11, A12, C12, E12, N12, R12, U12, H13, K13, A14, C14, E14, N14, R14, U14
VSS: H1, K1, B5, G5, L5, T5, B10, D10, G10, L10, P10, T10, H14, K14
VDD: G1, L1, G4, L4, C5, R5, C10, R10, D11, G11, L11, P11, G14, L14

+1.35VSDGPU

FBA_CLK0 / FBA_CLK0# → RV63 40.2_0402_1% VGA@, RV95 40.2_0402_1% VGA@, C0100 0.01U_0402_16V7K VGA@ <27>

+1.35VSDGPU → RV136 549_0402_1% VGA@; RV135 931_0402_1% VGA@; FBA_VREFC_L; RV56 1.33K_0402_1% VGA@; +FBA_VREFC0; CV195 820PF_0402_50V7K VGA@
<21> VRAM_VREF_CTL → QV3 BSS138W-7-F_SOT323-3 VGA@

DA8335 Cap Q'ty
22U x2
10U x 6
1U x 10
22U x 3 (unPOP)

+1.35VSDGPU → CV72 22U_0603_6.3V6M; CV196 22U_0603_6.3V6M
+1.35VSDGPU → CV75, CV102, CV197, CV198, CV199, CV200 10U_0402_6.3V6M
+1.35VSDGPU → CV201–CV210 1U_0201_6.3V6M

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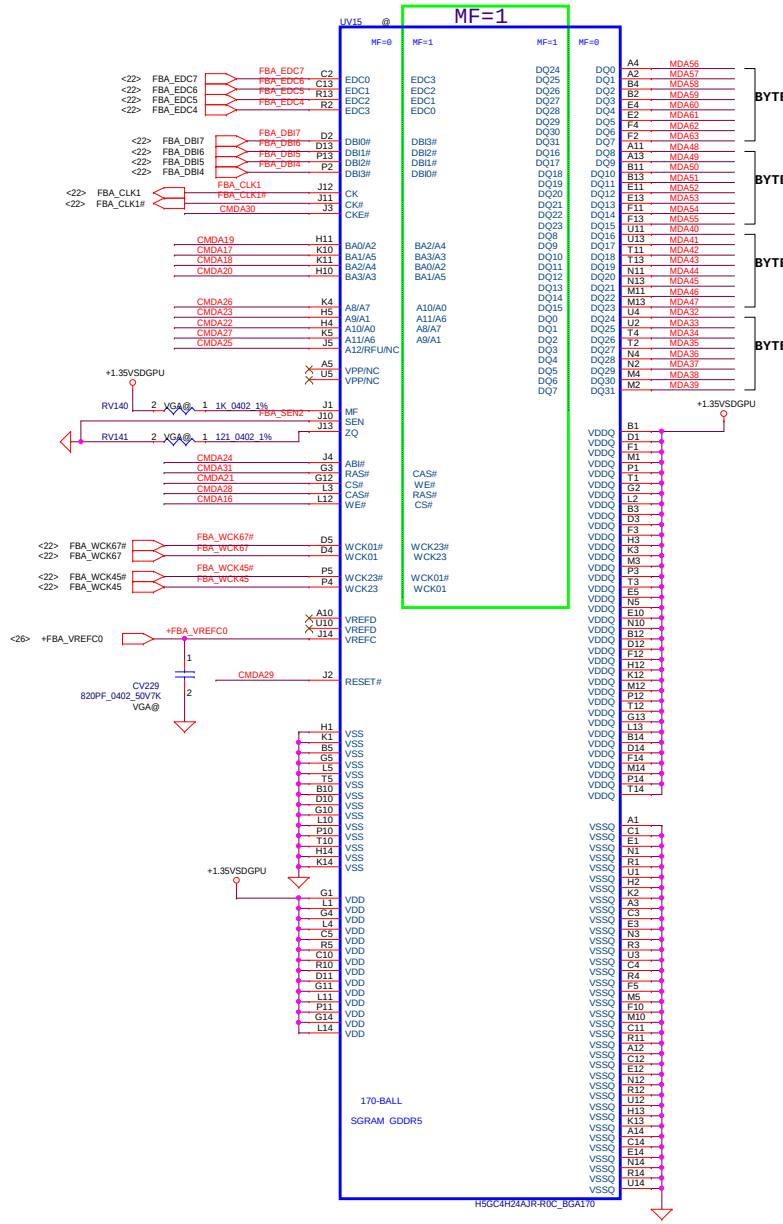
VRAM GDDR5 chips

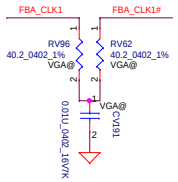
<22,26> MDA[63..0] → MDA[63..0]
<22,26> CMDA[31..0] → CMDA[31..0]

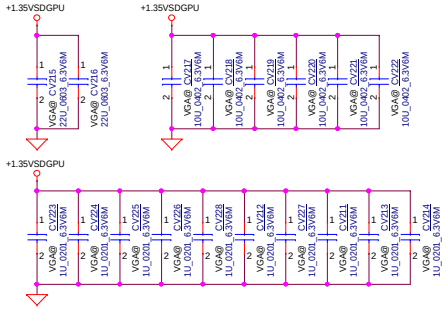
GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Channel 1 BOT SIDE







DA8335 Cap Q'ty
22U x2
10U x 6
1U x 10
22U x 3 (unPOP)

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Issued Date	2018/12/27	Deciphered Date	2019/12/27

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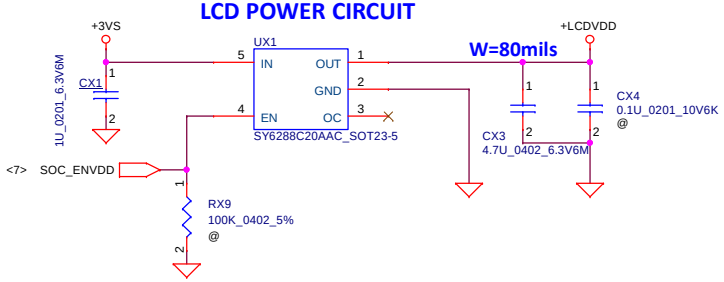
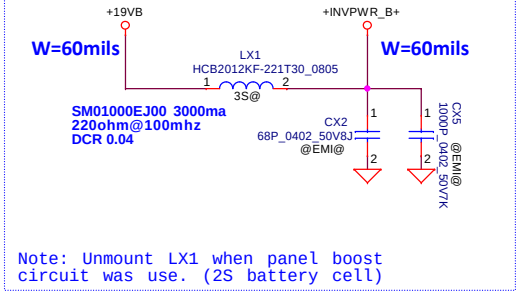
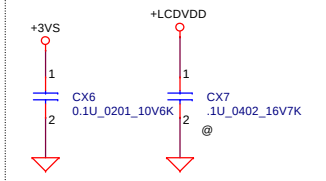
LCD POWER CIRCUIT

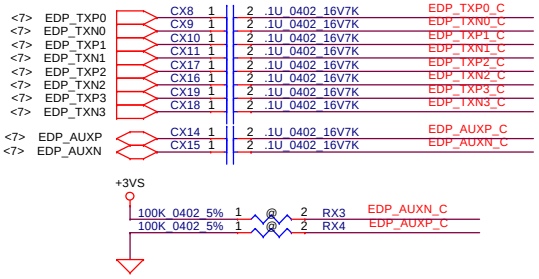


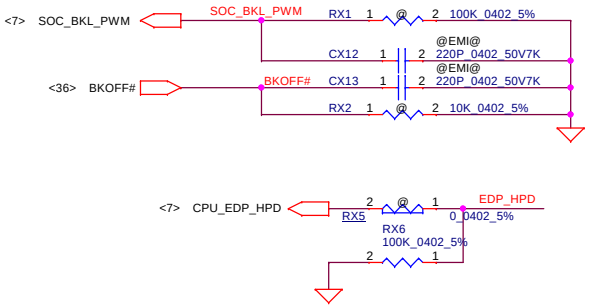


Note: Unmount LX1 when panel boost circuit was use. (2S battery cell)

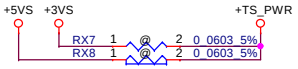
Place closed to JEDP1



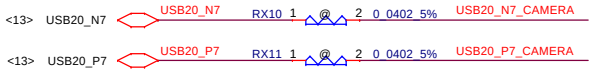




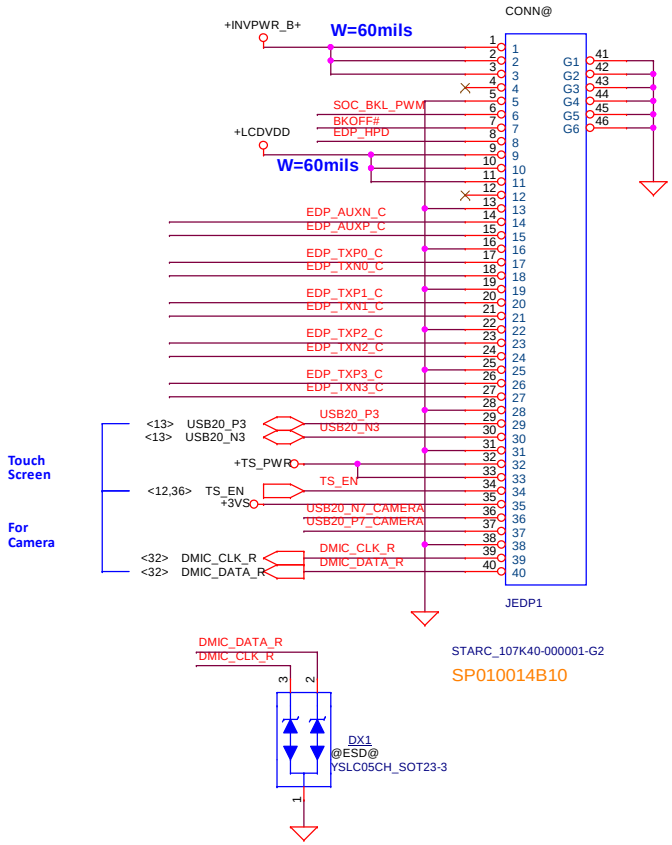
Touch Screen



Camera



LED PANEL Conn.



Touch Screen

For Camera

STARC_107K40-000001-G2

SP010014B10

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

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Title: **eDP Connector**

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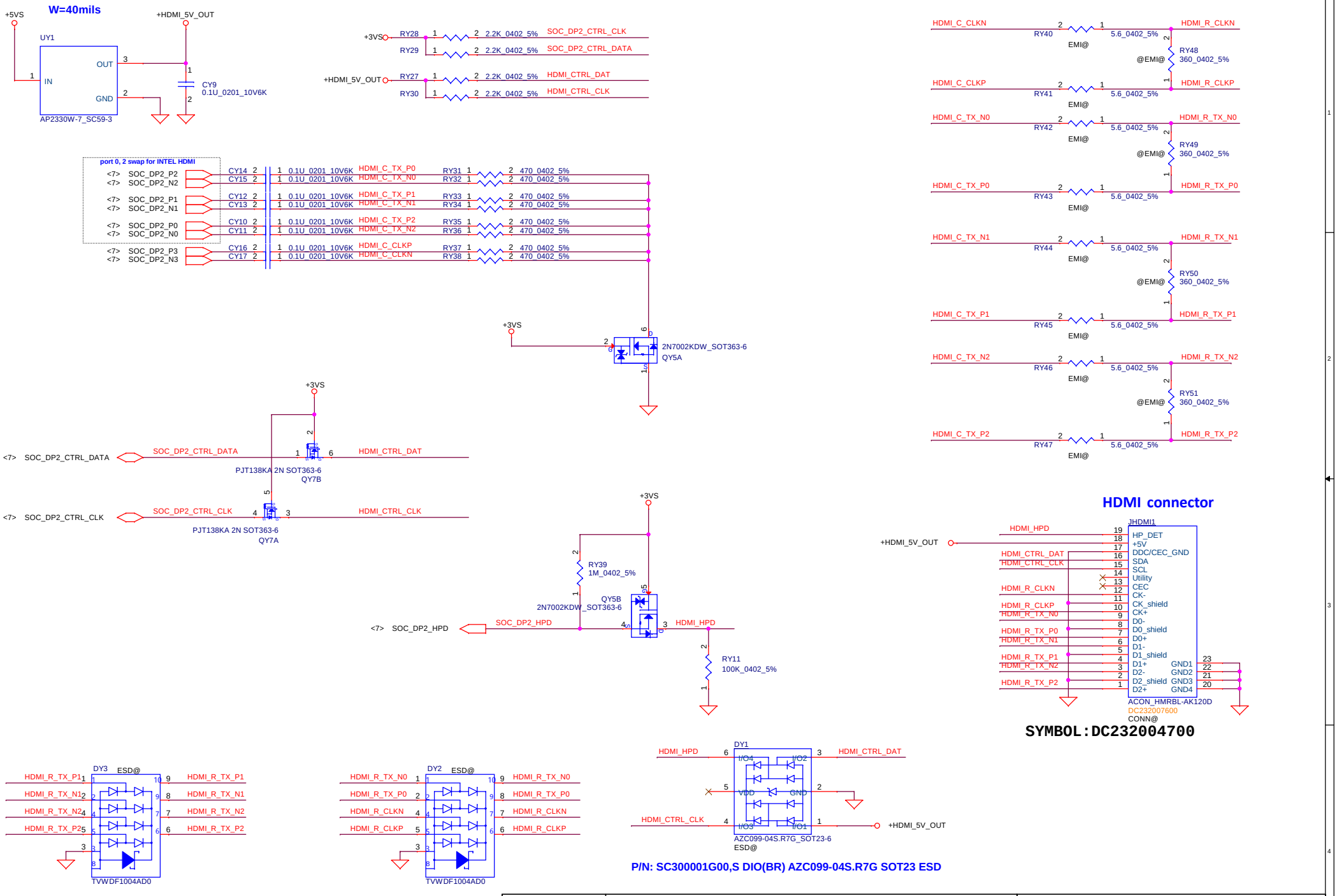


Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

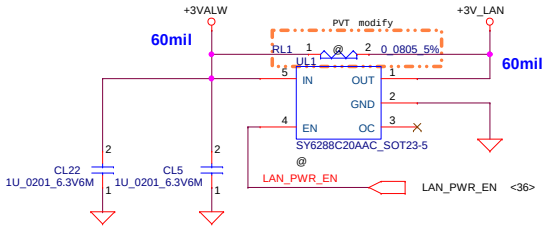
Compal Electronics, Inc.

Title: **HDMI CONN.**

Size	Document Number	Rev
Custom	EH7LW M/B LA-H791P	0.2

Date: Thursday, June 06, 2019 Sheet 29 of 57

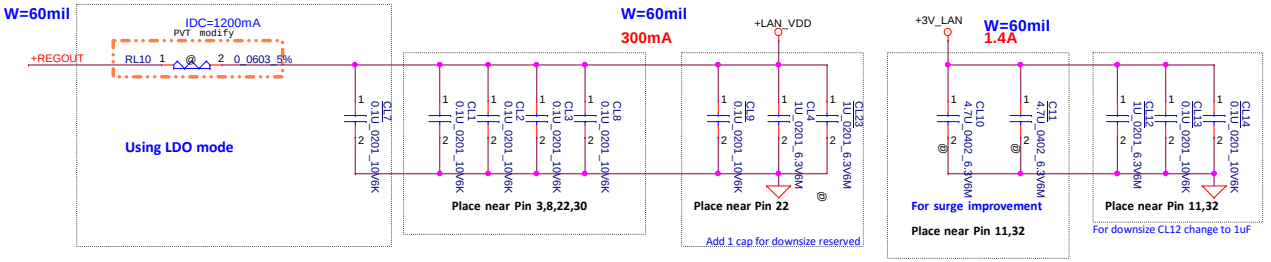
LAN-RTL8111H



From EC

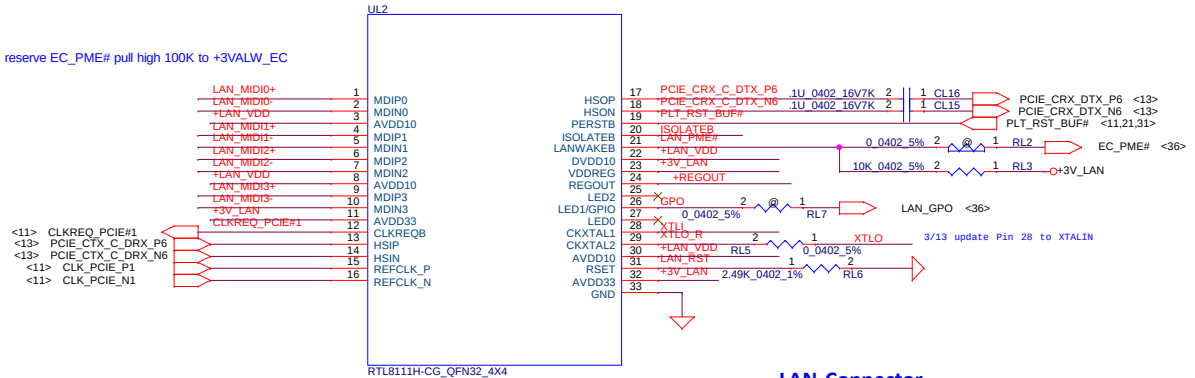
High active
EN threshold voltage min:1.2V typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

+3V_LAN Rising time must >0.5 ms and <100 ms

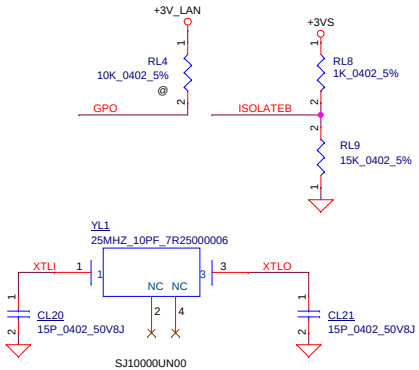


reserve EC_PME# pull high 100K to +3VALW_EC

PU at PCH side

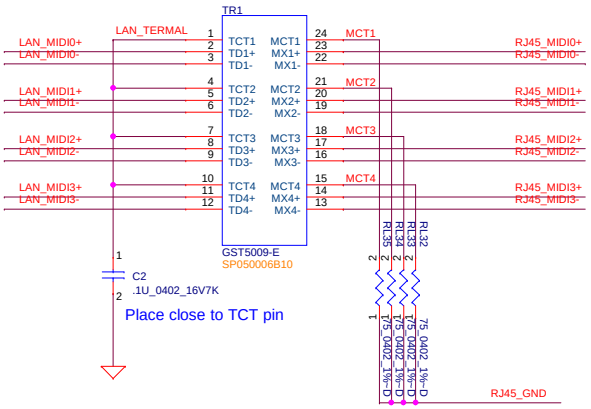


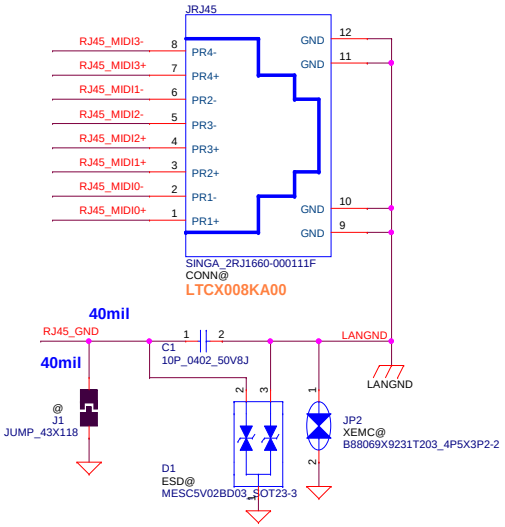
RTL8111H-CG_QFN32_4X4
SA000080P00



12/21 change YL1 size to 20x16

LAN Connector





Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: LAN RTL8111H-CG

Size: Custom | Document Number: EH7LW M/B LA-H791P | Rev: 0.2

Date: Wednesday, June 19, 2019 | Sheet 30 of 57

Wireless LAN

NGFF WL+BT (KEY E)

Co-layout with CNVi

PH +3VS at SOC side, for win7 USB3 debug

KEY E

#571906 change to USB port10 for CNVi

For BT

reserve for BT_ON OD pull high (1.0)

reserve 1000p for cnvi

PH +3VS at SOC side, for win7 USB3 debug

P80CLK and BT_ON enable seperate.

ESD reserve LC filter close PCH

For CNVi Feature

Reserved for BT I2S bus

SP070013E00

mSATA/SSD

KEY M

PETp0/SATA-A+	49
PETn0/SATA-A-	47
GND	45
PERp0/SATA-B-	43
PERn0/SATA-B+	41

Port P and N follow SATA

Table 35-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

SSD_DET# (SATA_GP0)
SATA Device 0
PCIE Device 1

SP070018L00

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

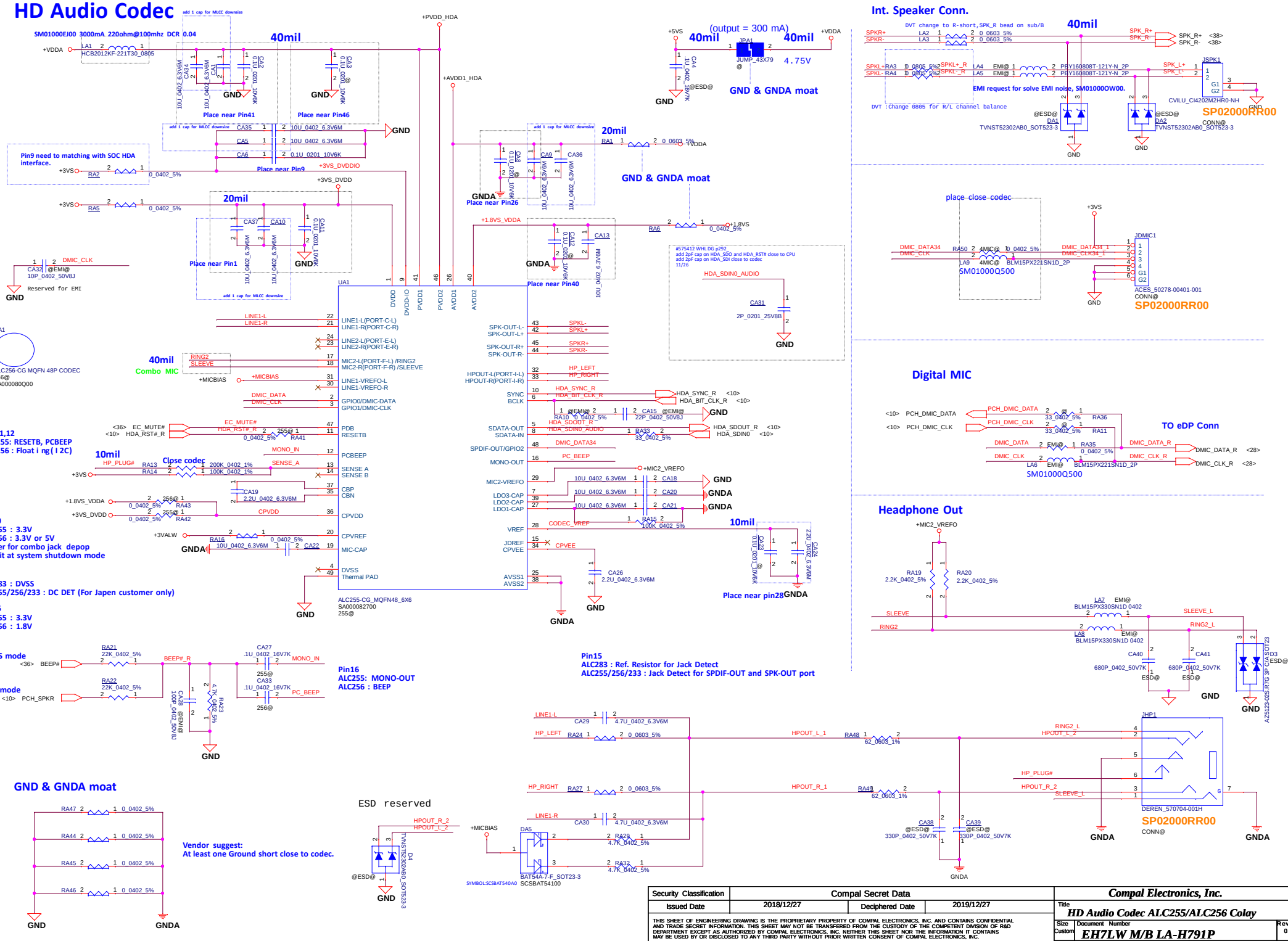
Compal Electronics, Inc.

Title: M.2 Key E (WLAN)/Key M(SSD)

Size: Custom | Document Number: EH7LW M/B LA-H791P | Rev: 0.2

Date: Thursday, June 06, 2019 | Sheet 31 of 57

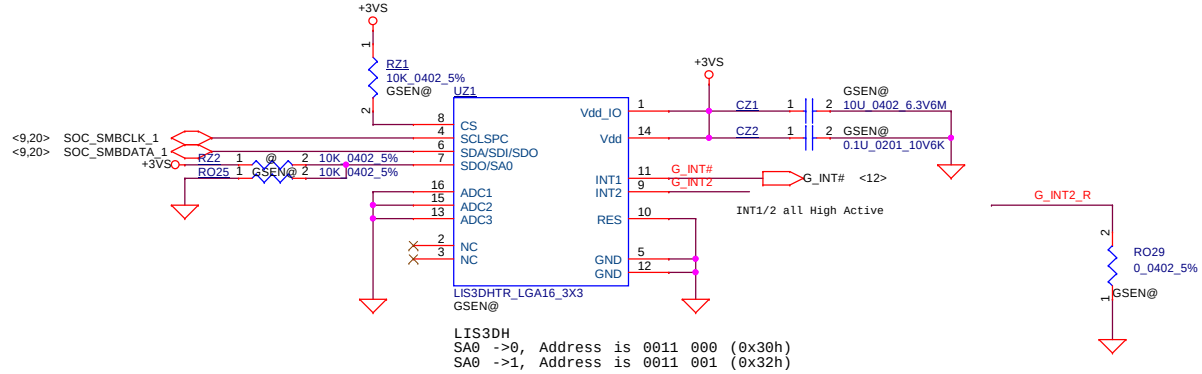
HD Audio Codec



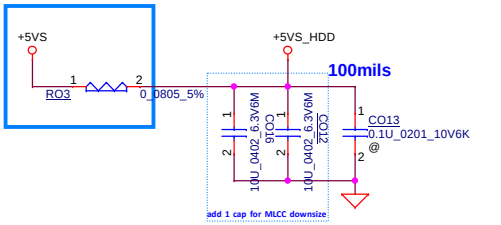
Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.			
Title: HD Audio Codec ALC255/ALC256 Colay			
Size: Custom	Document Number: EH7LW M/B LA-H791P		Rev: 0.2
Date: Thursday, June 06, 2019	Sheet 32 of 57		

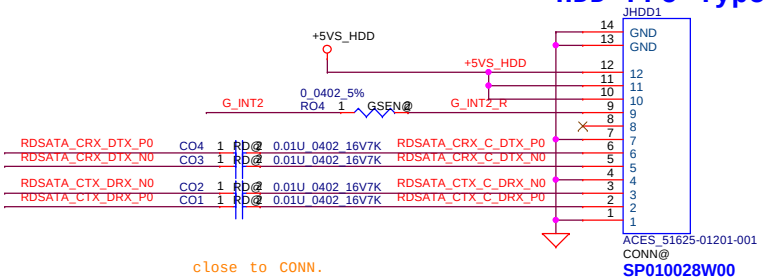
G-Sensor reserved for BA serial



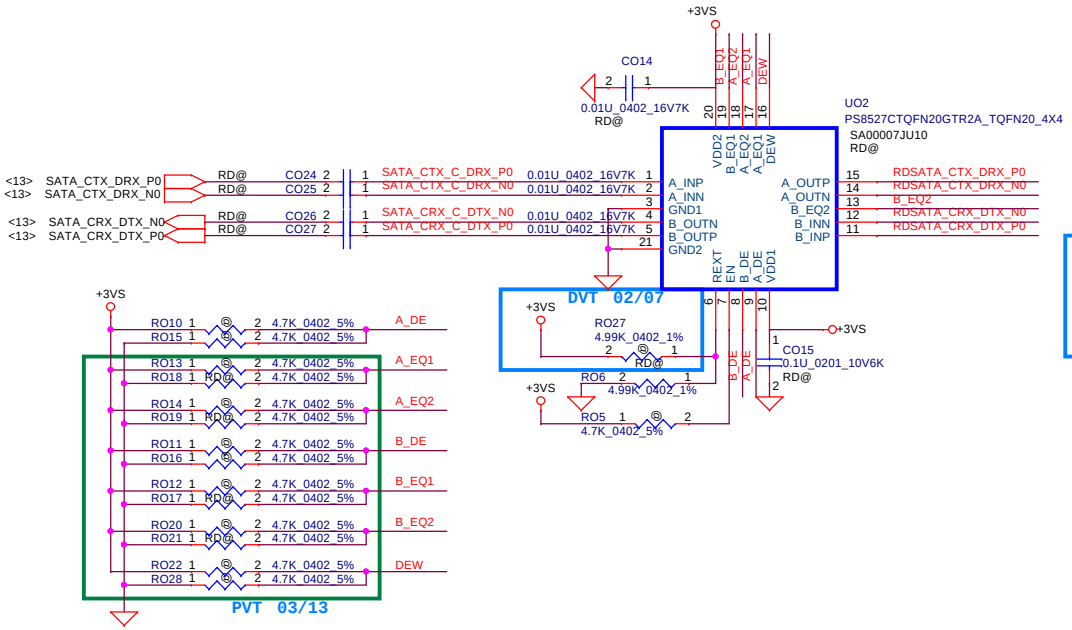
LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

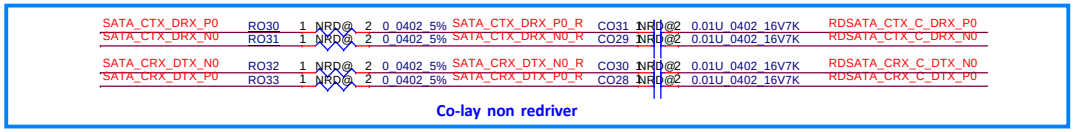


HDD FFC Type



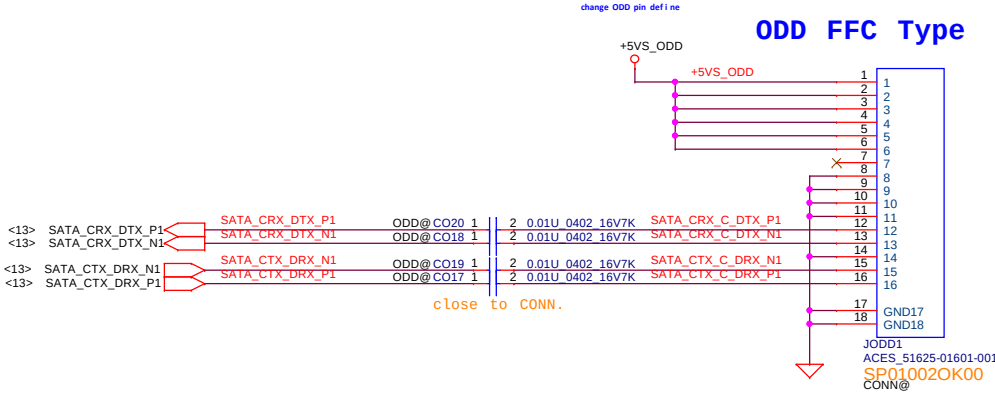
close to CONN.



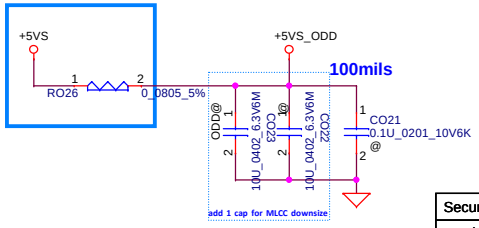


change ODD pin define

ODD FFC Type



close to CONN.



Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

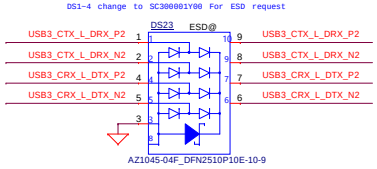
Title: G-Sensor/HDD/ODD

Size: Custom | Document Number: EH7LW M/B LA-H791P | Rev: 0.2

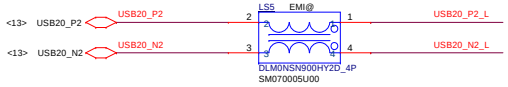
Date: Thursday, June 06, 2019 | Sheet 33 of 57

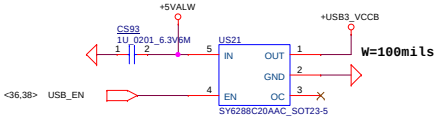
USB3.0 (Port 2)

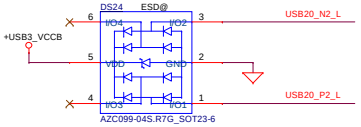
USB3 port reserved

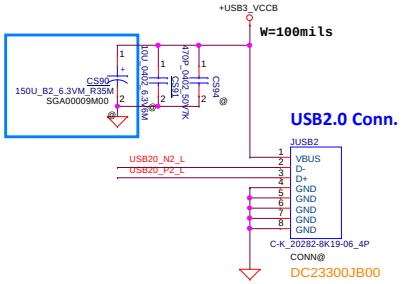


USB2.0 (Port 2)









Symbol:DC23300N800
compatible: DC23300TT00

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

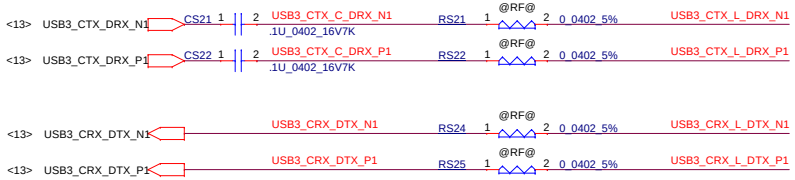
Compal Electronics, Inc.

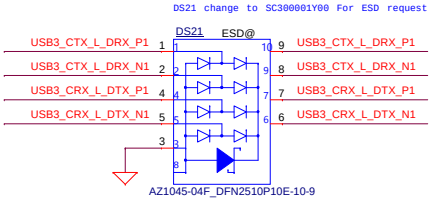
Title: USB3_P2_MB

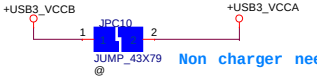
Size	Document Number	Rev
Custom	EH7LW M/B LA-H791P	0.2

Date: Thursday, June 06, 2019 Sheet 34 of 57

USB3.0 (Port 1)

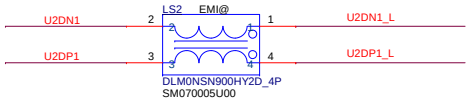


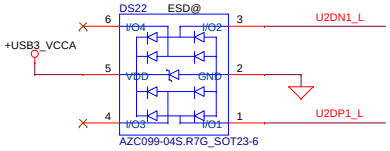




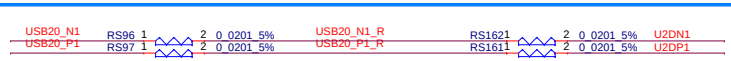
Non charger need short this JP

modify 11/12

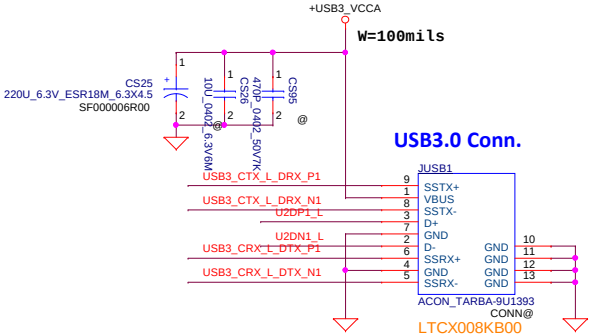


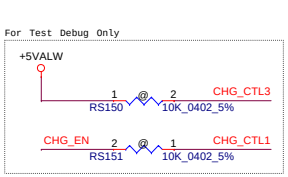


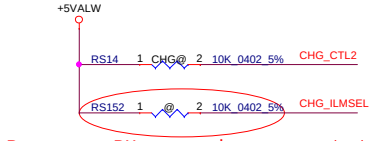
DVT: R-short



Co-lay non redriver / Reserved-1/29 change to R-short





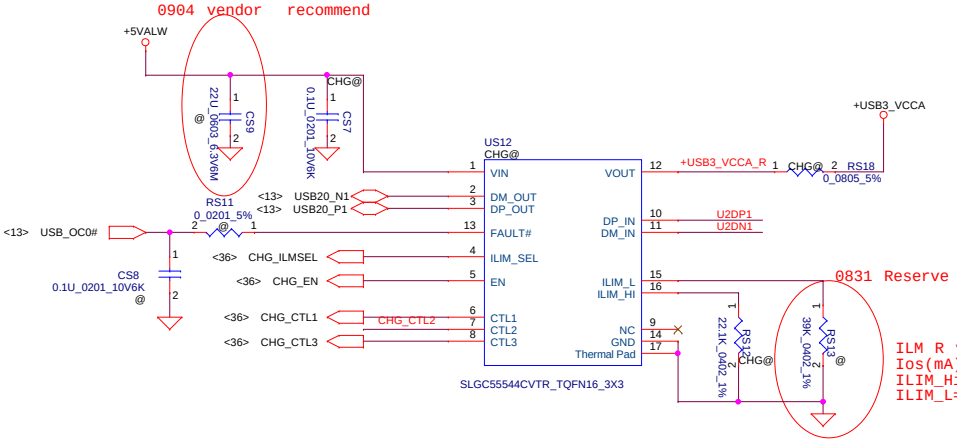


Rerserve PU, vendor suggest to EC control if future need support SDP2

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

0904 vendor recommend



0831 Reserve ILIM_L R as vendor recommend

ILM R vaule
Ios(mA)=50250/R(Kohm)
ILIM_Hi=2273mA
ILIM_L=1288mA(reserve)

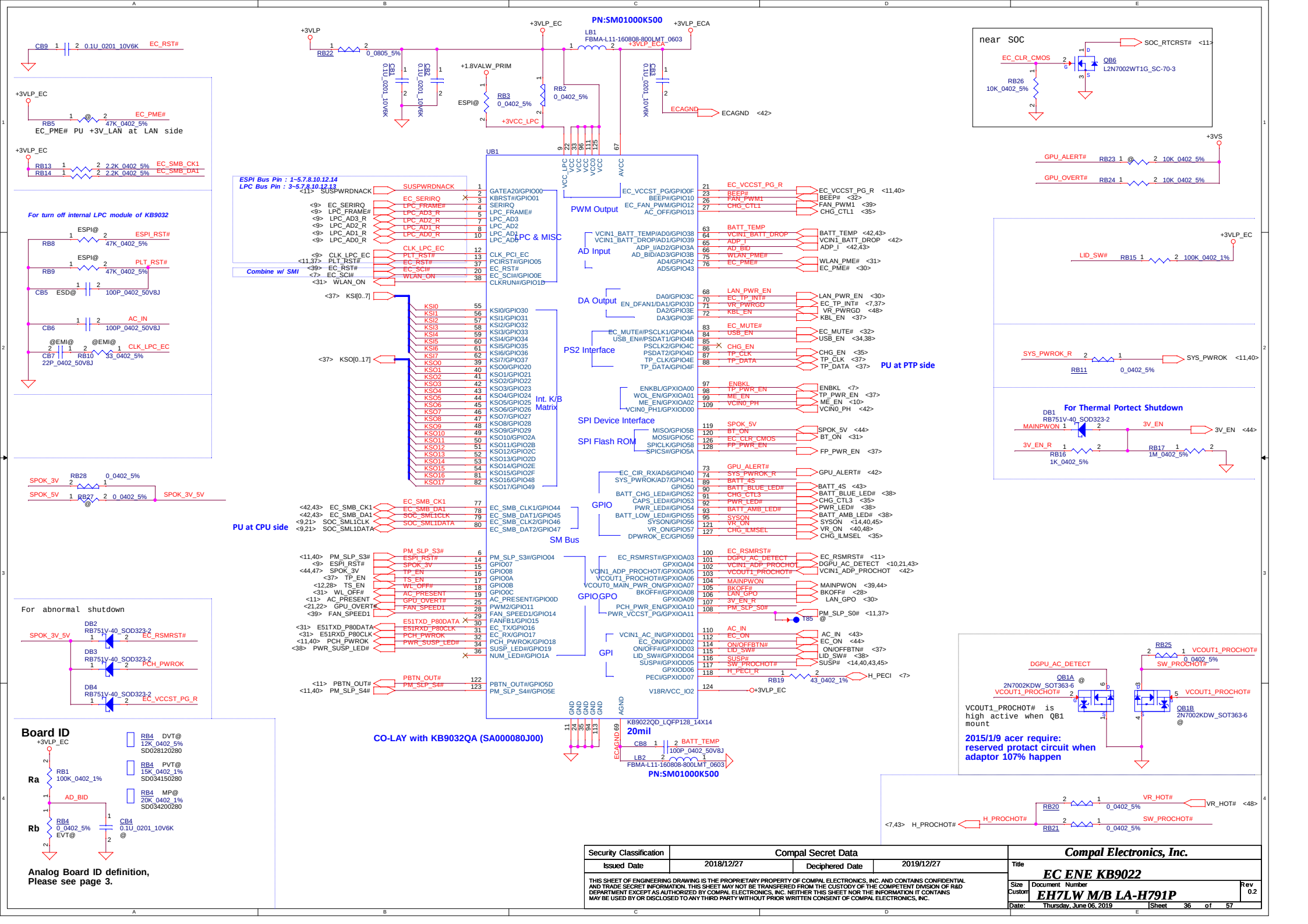
Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: USB3_P1_CHG_MB

Size: Custom | Document Number: EH7LW M/B LA-H791P | Rev: 0.2

Date: Thursday, June 06, 2019 | Sheet 35 of 57



Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

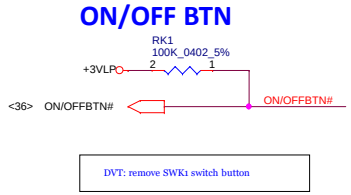
Title: **EC ENE KB9022**

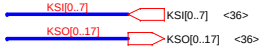
Size: Custom | Document Number: **EH7LW M/B LA-H791P** | Rev: 0.2

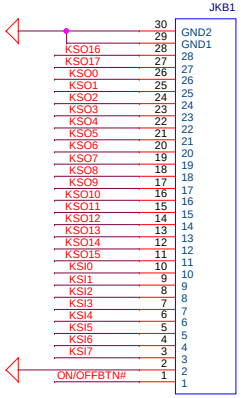
Date: Thursday, June 06, 2019 | Sheet 36 of 57

KB Conn.

ON/OFF BTN

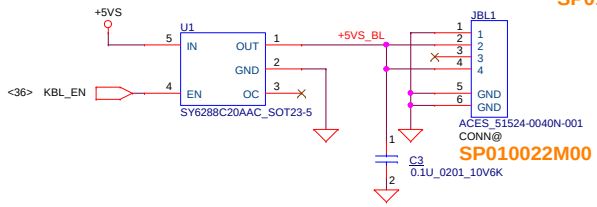






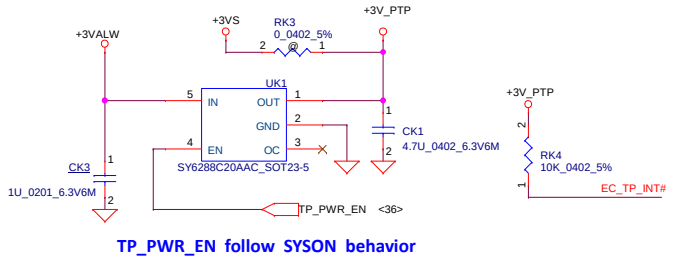
ACES_85201-2805
CONN@
SP01000GO00

KB BackLight

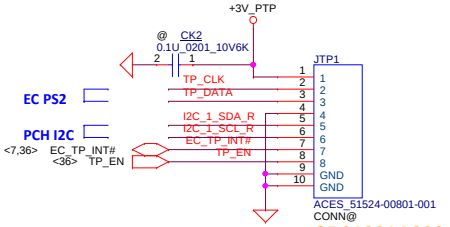


SP010022M00

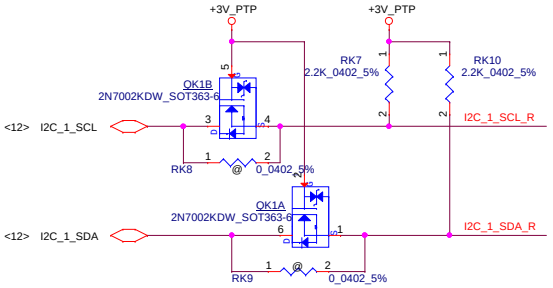
TP/B Conn.

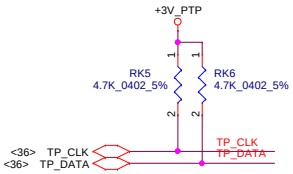


TP_PWR_EN follow SYSON behavior

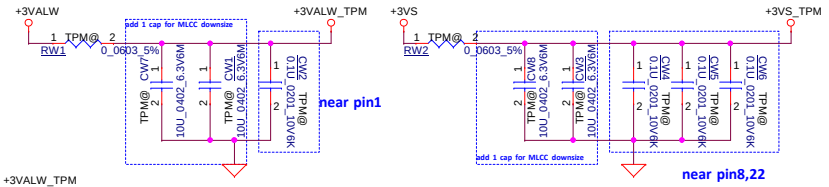


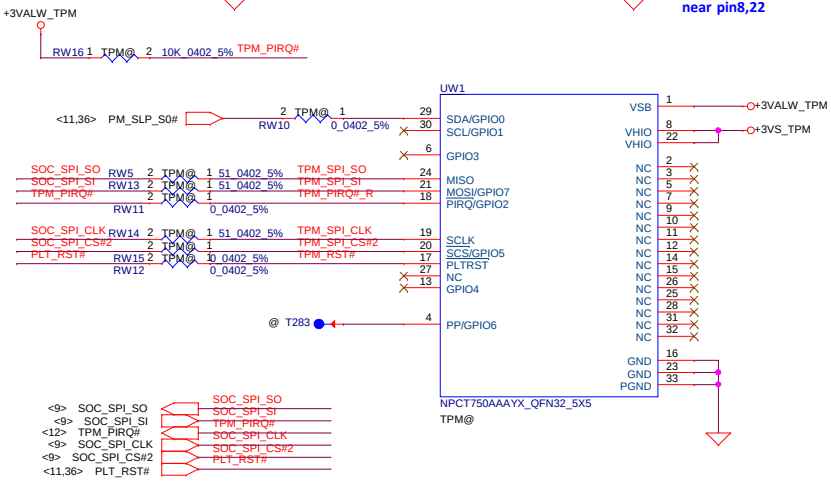
SP01001A900





TPM 2.0

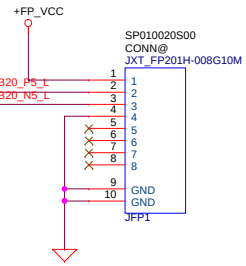


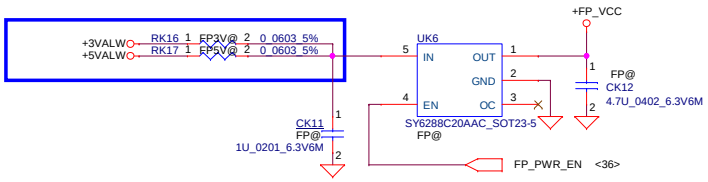


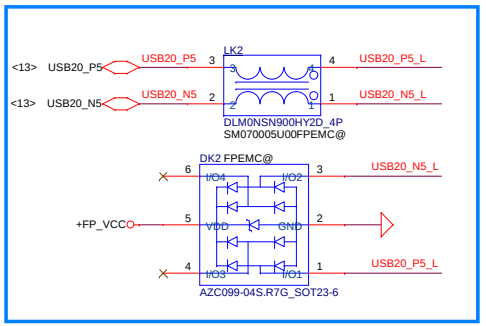
SA0000AQ230, S IC NPCT750AAAYX QFN 32P TPM (SPI interface)

Finger Print

Power Souce Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V







Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

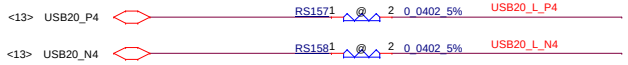
Compal Electronics, Inc.

Title: KB & TP & TPM & FP

Size: Custom | Document Number: EH7LW M/B LA-H791P | Rev: 0.2

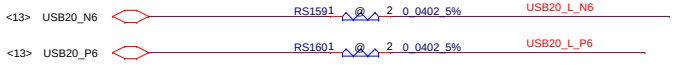
Date: Thursday, June 06, 2019 | Sheet 37 of 57

USB2 I/O



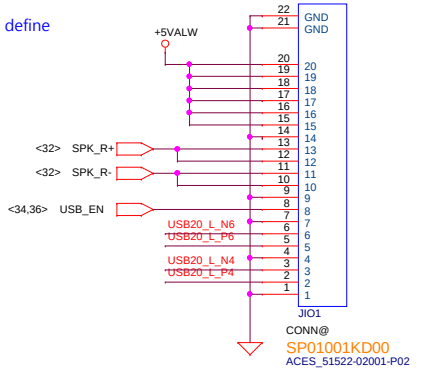
Reserved CMC on SUB/B side

Card reader

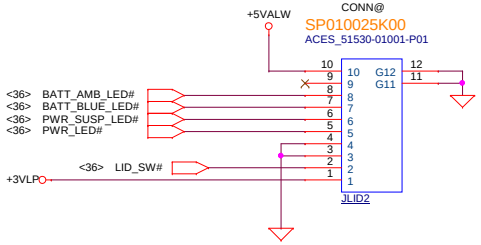


I/O Borad (USB2 /Card reader/ Speaker-RCH)

DVT:update JIO1 pin define

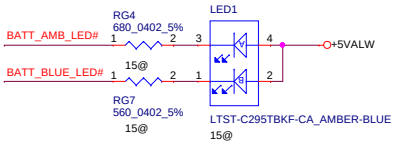


LID/B with LED for 17" UMA &DIS

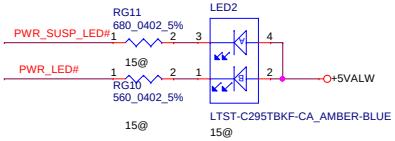


LED for 15" UMA

Battery LED

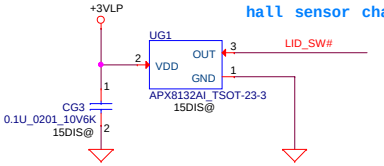


Power LED

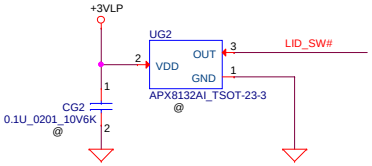


LID for 15" DIS

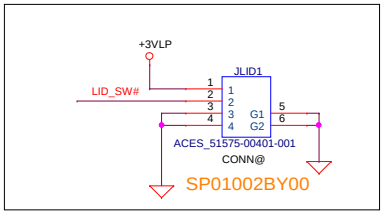
hall sensor change to TOP side



SA00008K800, S IC APX8132AI-TRG SOT-23 3P HALL SENSOR



LID/B for 15" UMA 4pin



Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: IO/LiD/LED

Size: Custom | Document Number: EH7LW M/B LA-H791P | Rev: 0.2

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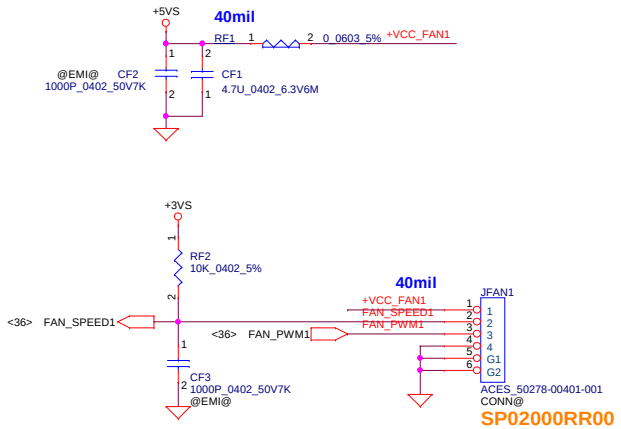
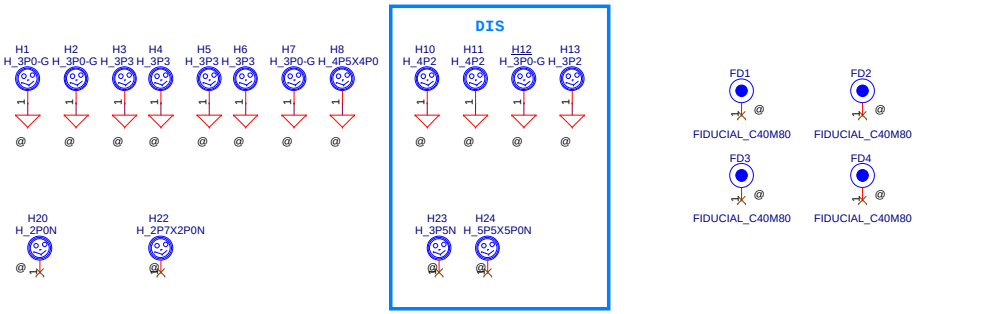
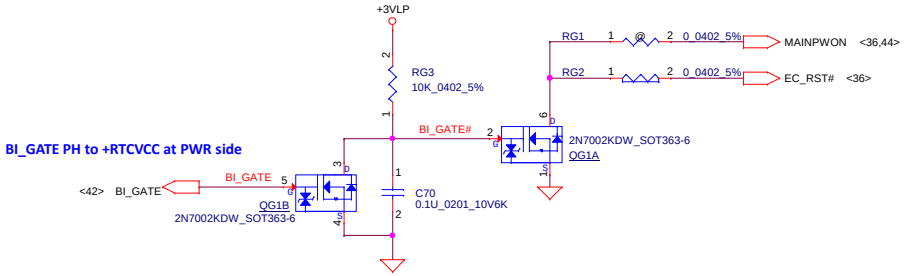
FAN1 Conn



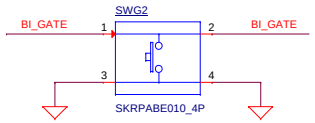
Screw Hole



Reset Circuit



Reset Button



Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: **FAN & Screw Hole & Reset**

Size	Document Number	Rev
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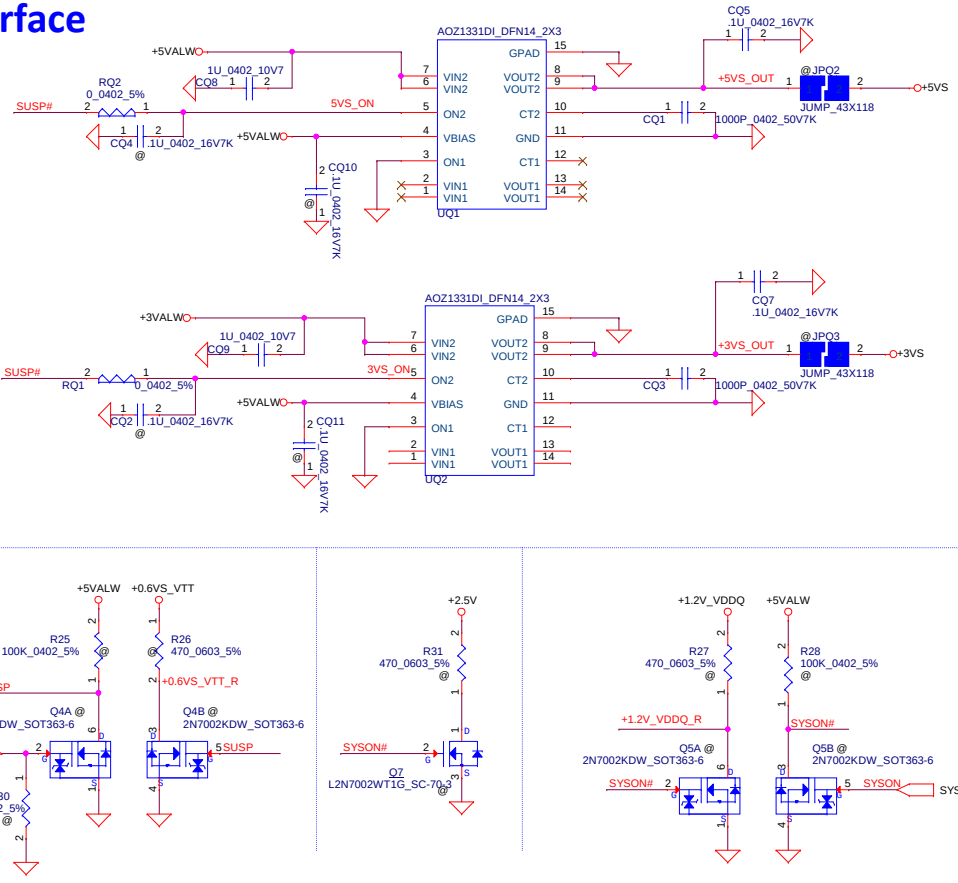
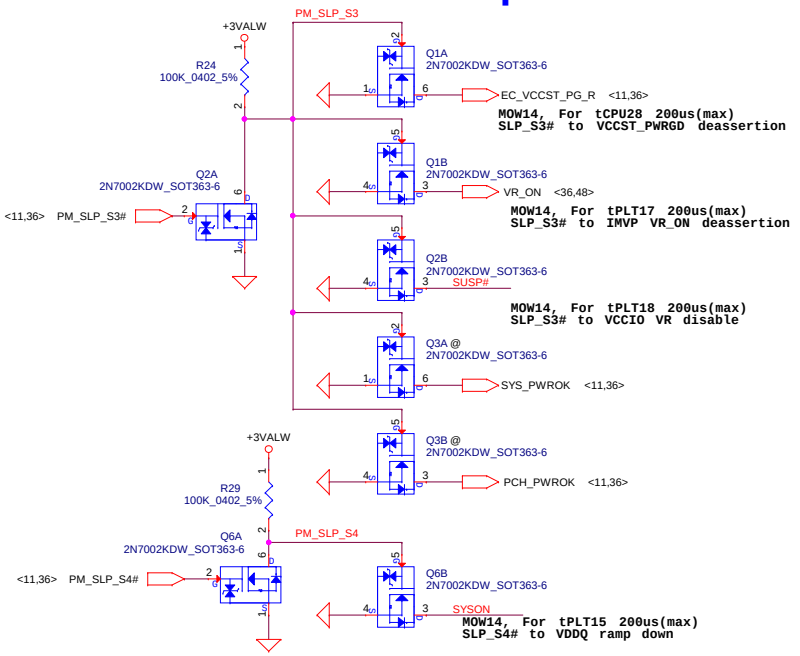
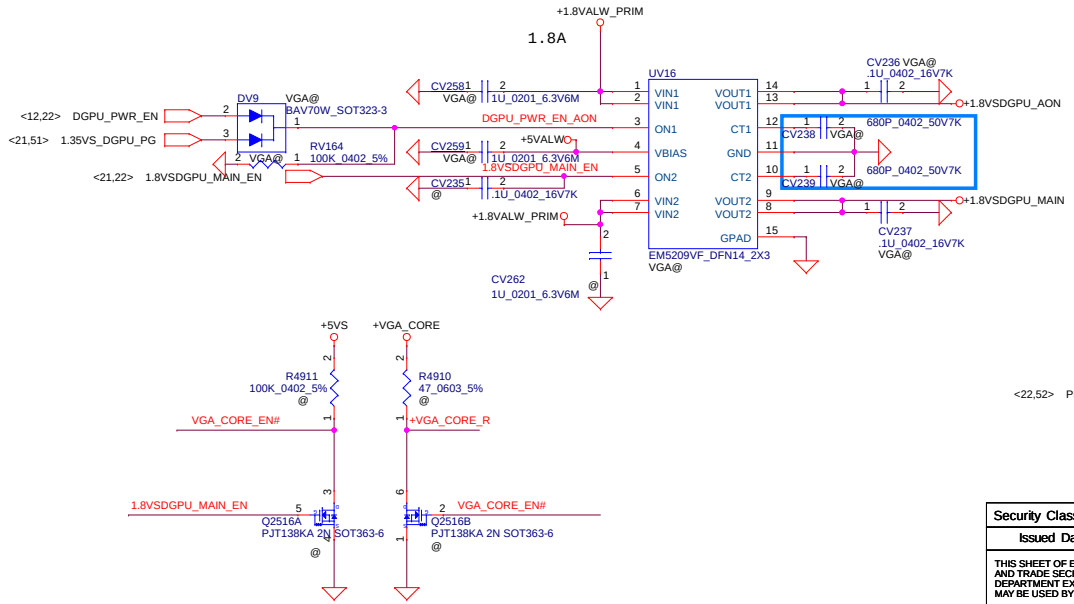
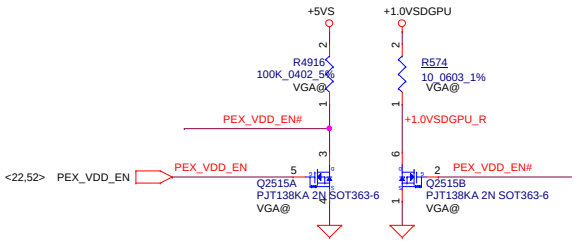
DC Interface

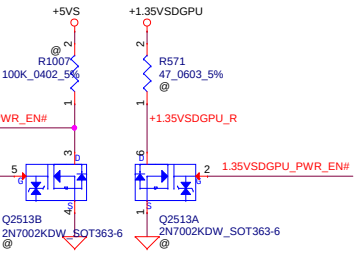


For Power ON/Off Sequence









Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: EH7LW M/B LA-H791P | Rev: 0.2

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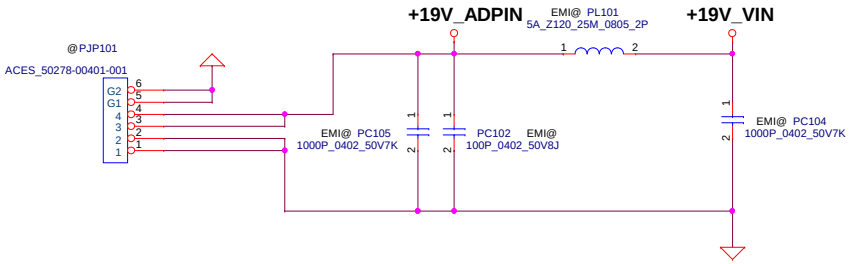

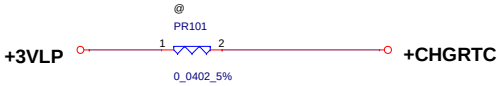

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: **PWR DCIN / Pre-charge**

Size	Document Number	Rev
Custom	EH7LW M/B LA-H791P	0.2

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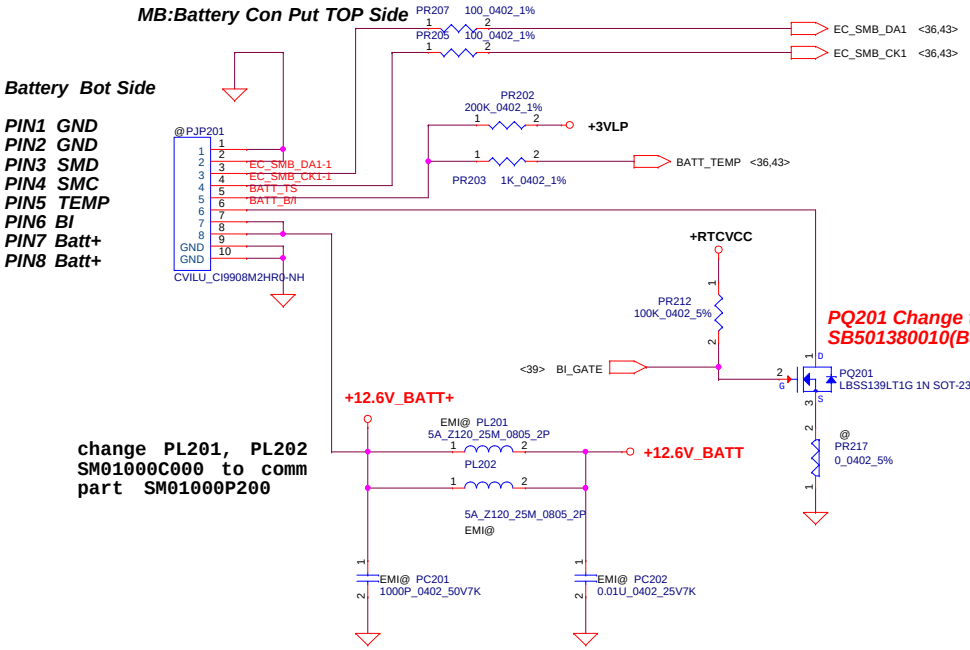
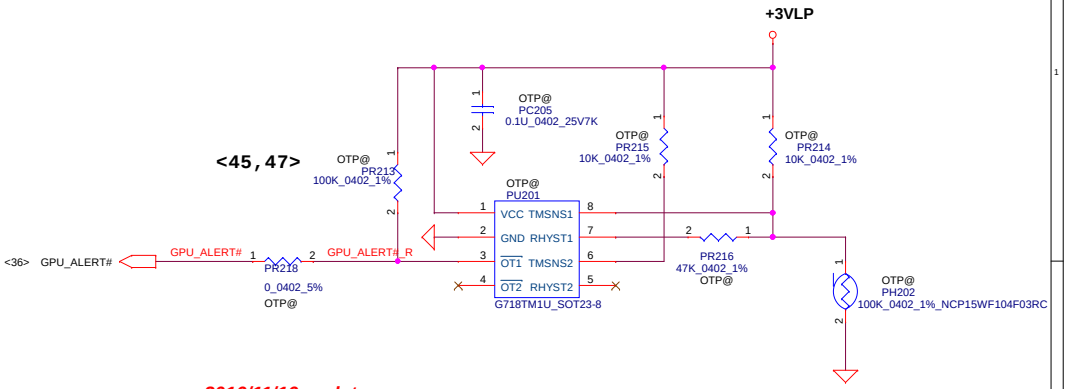


PQ201 Change to SB00000QO00, SB501380010(BSS138LT1G Del)

change PL201, PL202 SM01000C000 to comm part SM01000P200



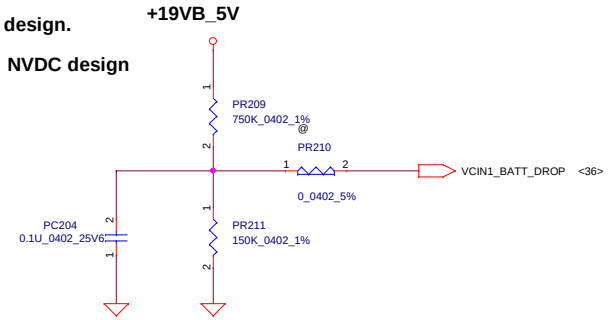
2016/11/16 update

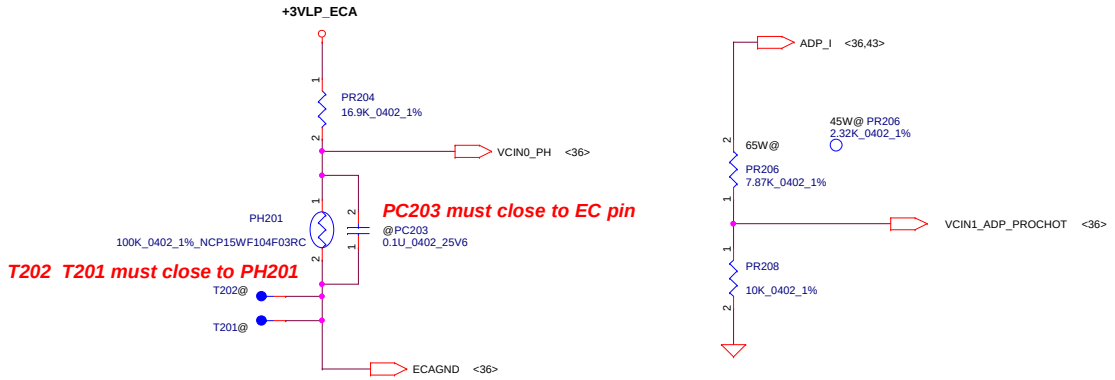
For KB9022 sense 20mΩ	Active	Recovery
45W PR206 2.32K ohm	58.5W,1V	Active=recovery
65W PR206 7.87K ohm	84.5W,1V	Active=recovery
90W PR20K ohm	__W,__V	Active=recovery
PH1	2V	1V

PH1 under CPU botten side :
CPU thermal protection at 89 +-3 degree C
Recovery at 56 +-3 degree C

2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

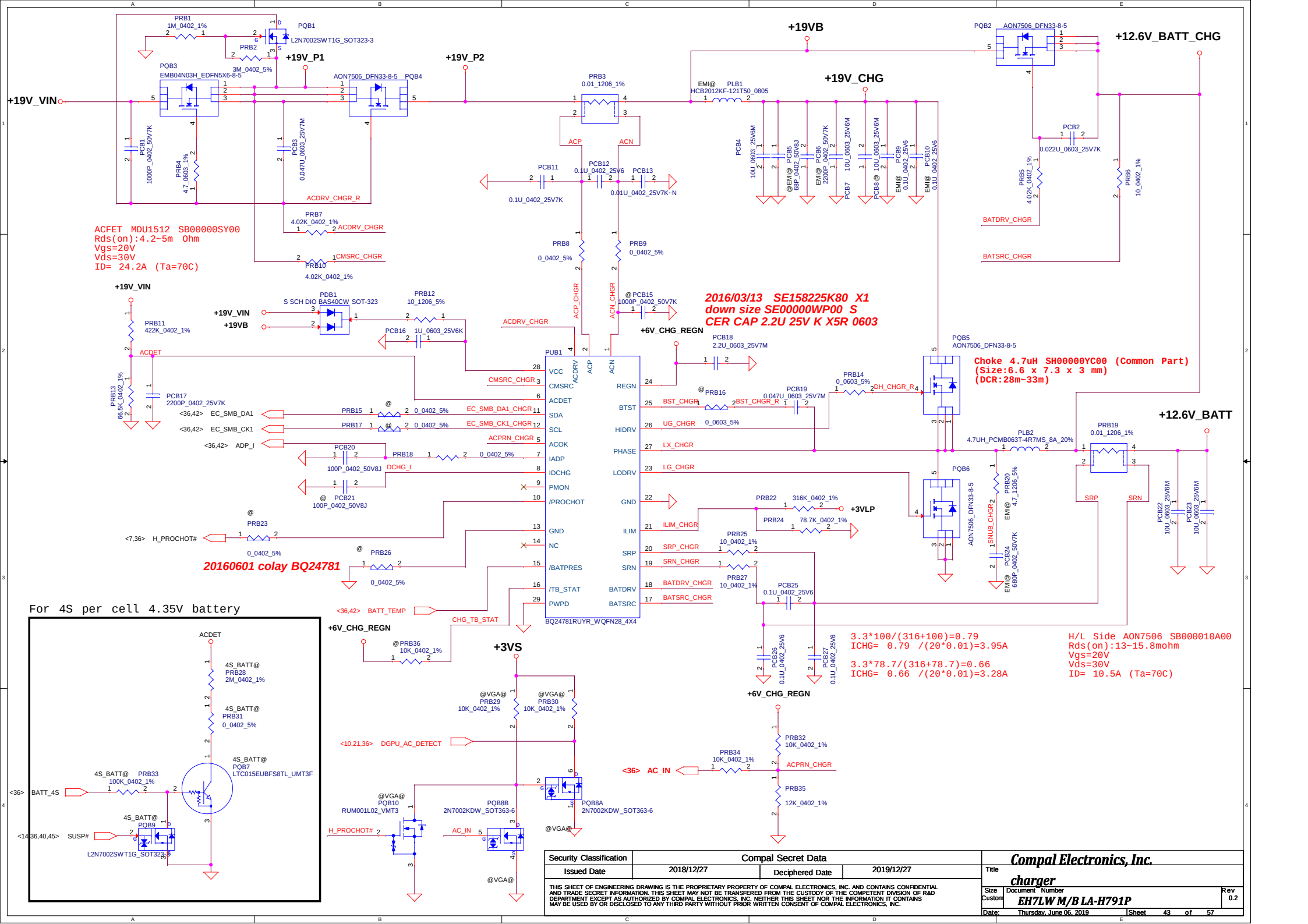
VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50k if Battery is 2-cell NVDC design
B+=6V





Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size Custom	Document Number EH7LW M/B LA-H791P		Rev 0.2
Date: Thursday, June 06, 2019	Sheet 42 of 57		



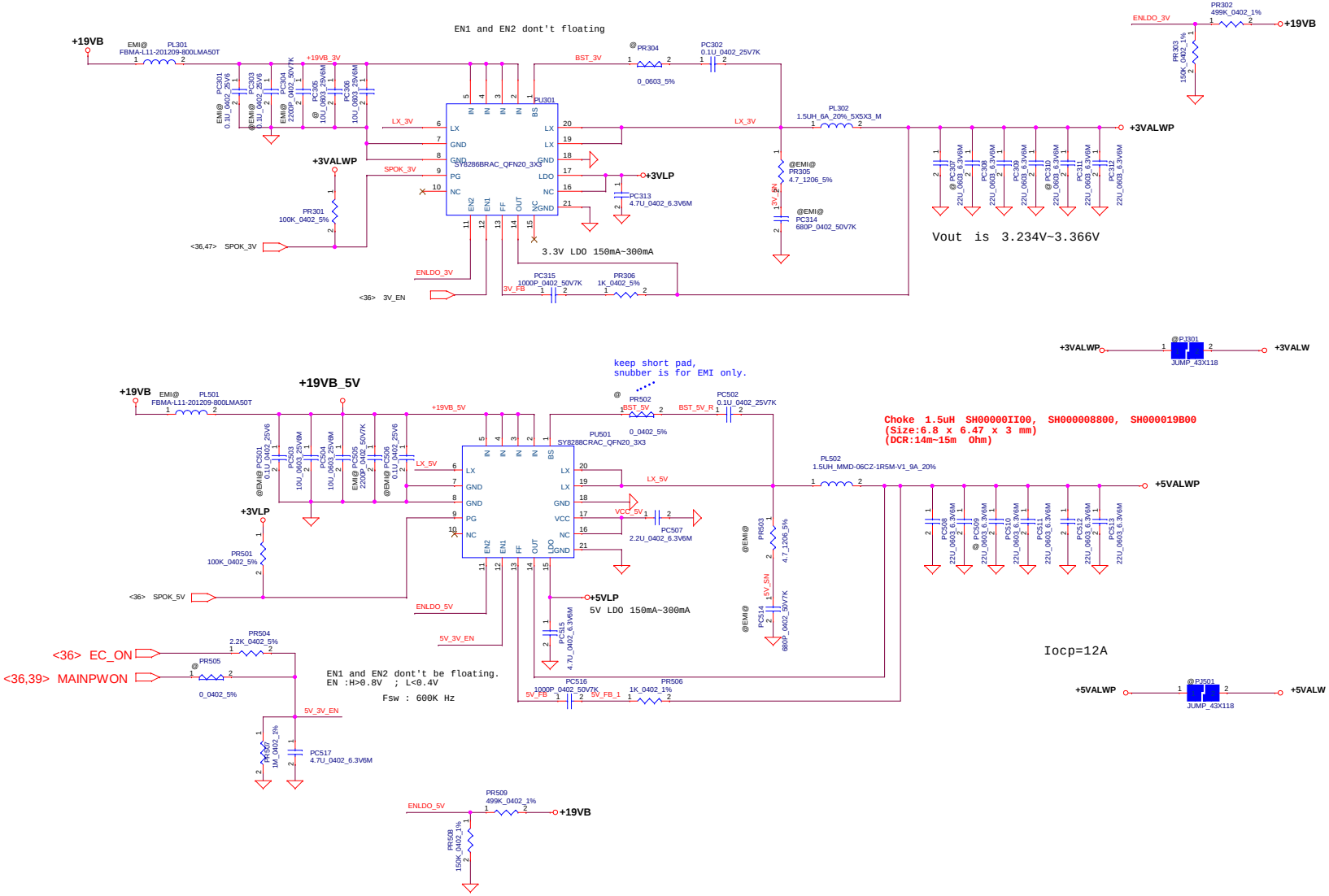
Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: charger

Size	Document Number	Rev
Custom	EH71LW M/B LA-H791P	0.2

Date: Thursday, June 06, 2019 Sheet 43 of 57



Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom	EH7LW M/B LA-H791P	0.2

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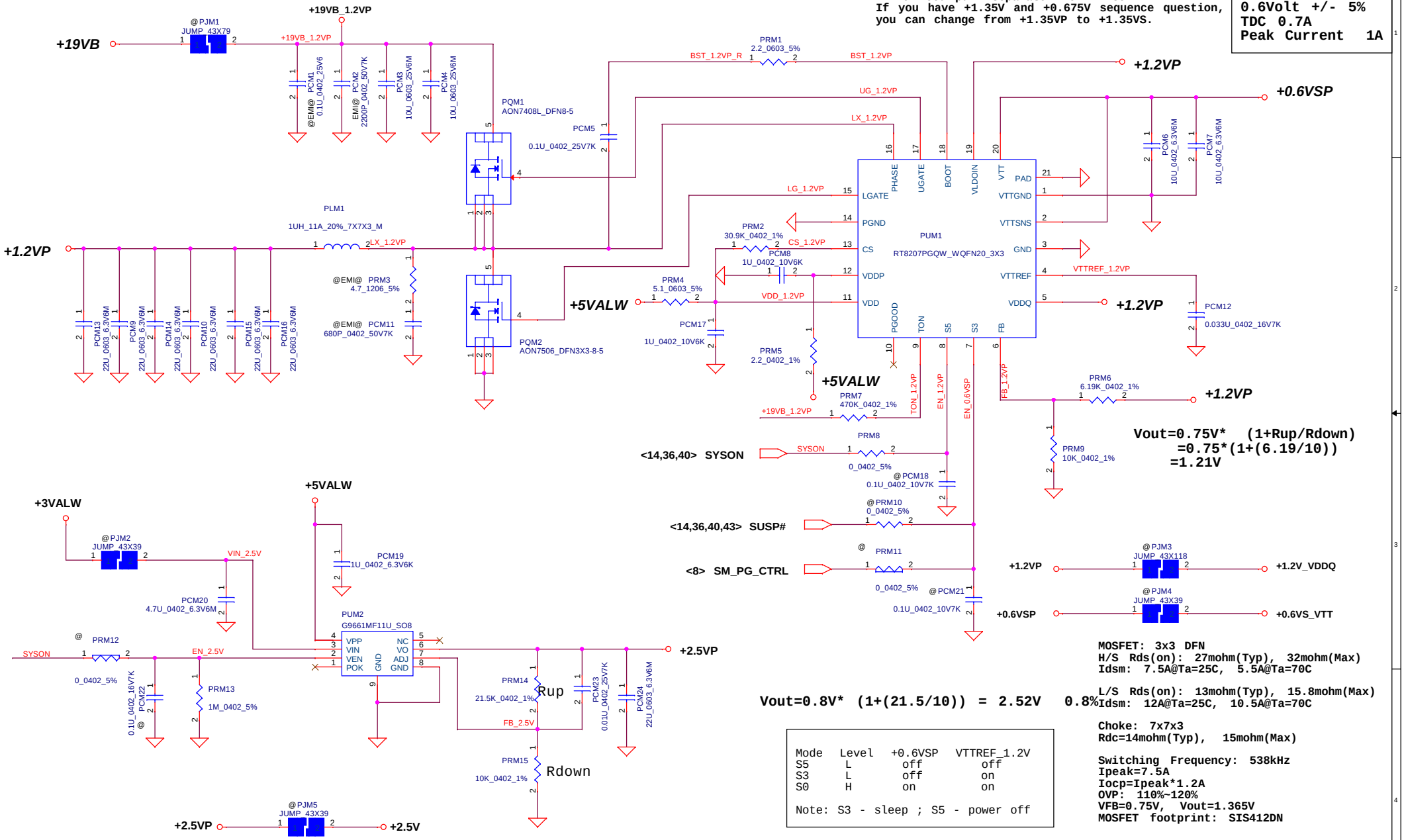
Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A



Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 32mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 13mohm(Typ), 15.8mohm(Max)
Idsm: 12A@Ta=25C, 10.5A@Ta=70C

Choke: 7x7x3
Rdc=14mohm(Typ), 15mohm(Max)

Switching Frequency: 538kHz
Ipeak=7.5A
Iocp=Ipeak*1.2A
OVP: 110%~120%
VFB=0.75V, Vout=1.365V
MOSFET footprint: SIS412DN

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

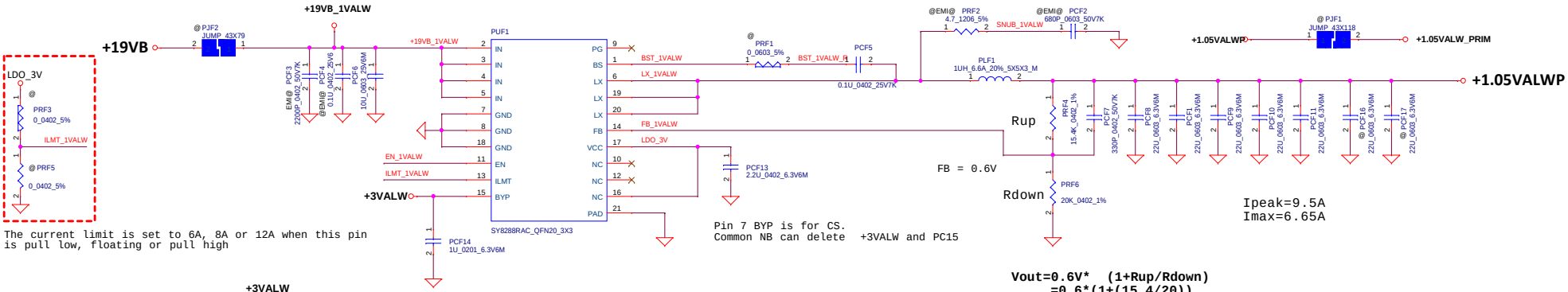
Compal Electronics, Inc.

Title: RT8207P

Size: Custom | Document Number: EH7LW M/B LA-H791P | Rev: 0.2

Date: Thursday, June 06, 2019 | Sheet 45 of 57

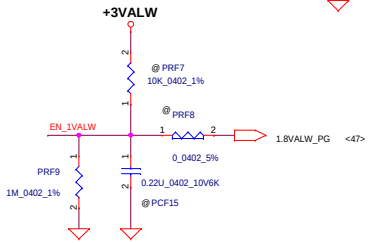
EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

Vout=0.6V* (1+Rup/Rdown)
=0.6*(1+(15.4/20))
Vout=1.062V



Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: VCCP

Size	Document Number	Rev
C	EH7LW M/B LA-H791P	0.2

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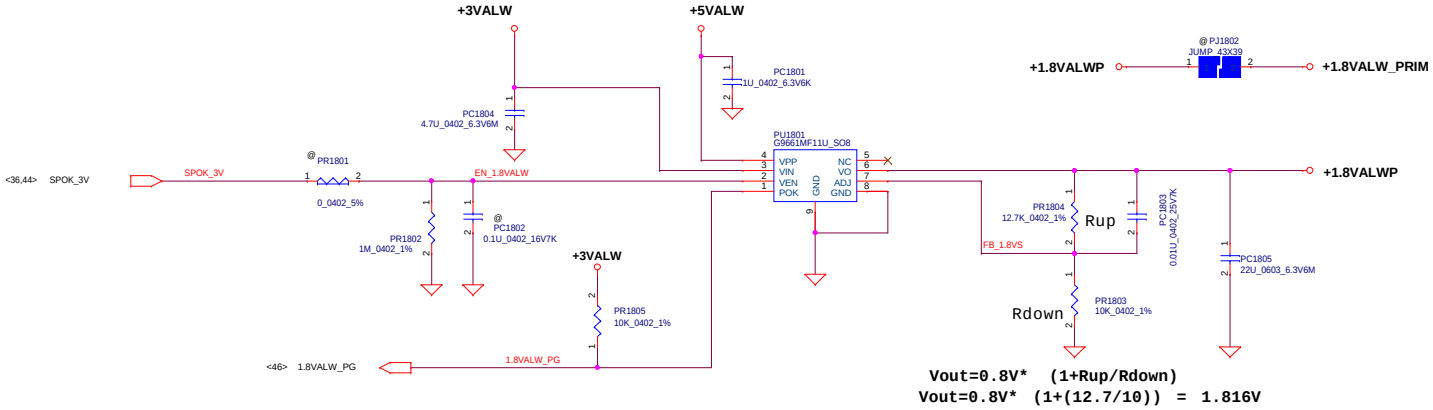


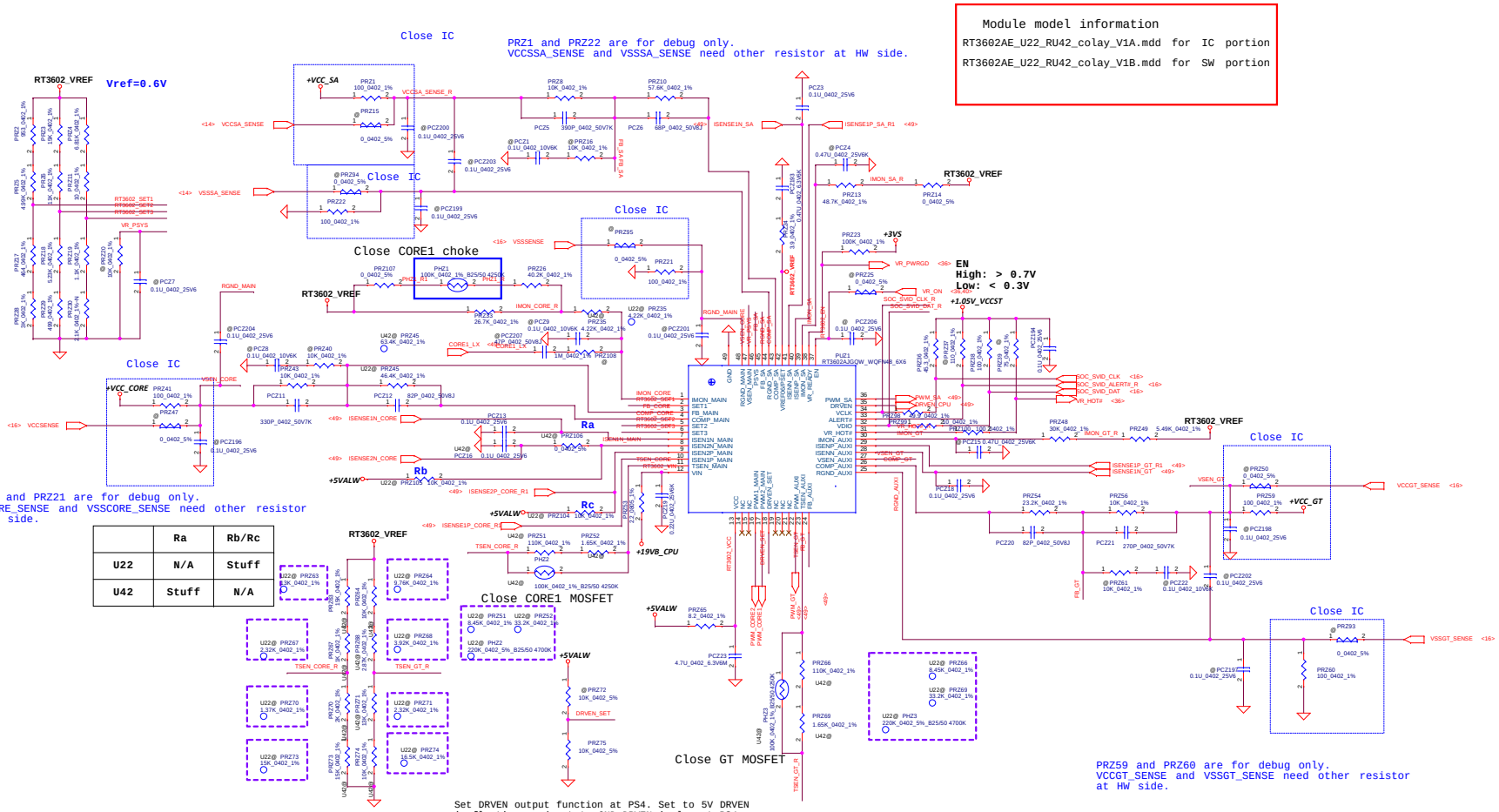
Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: SY8032

Size	Document Number	Rev
C	EH7LW M/B LA-H791P	0.2

Date: Thursday, June 06, 2019 | Sheet 47 of 57



	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

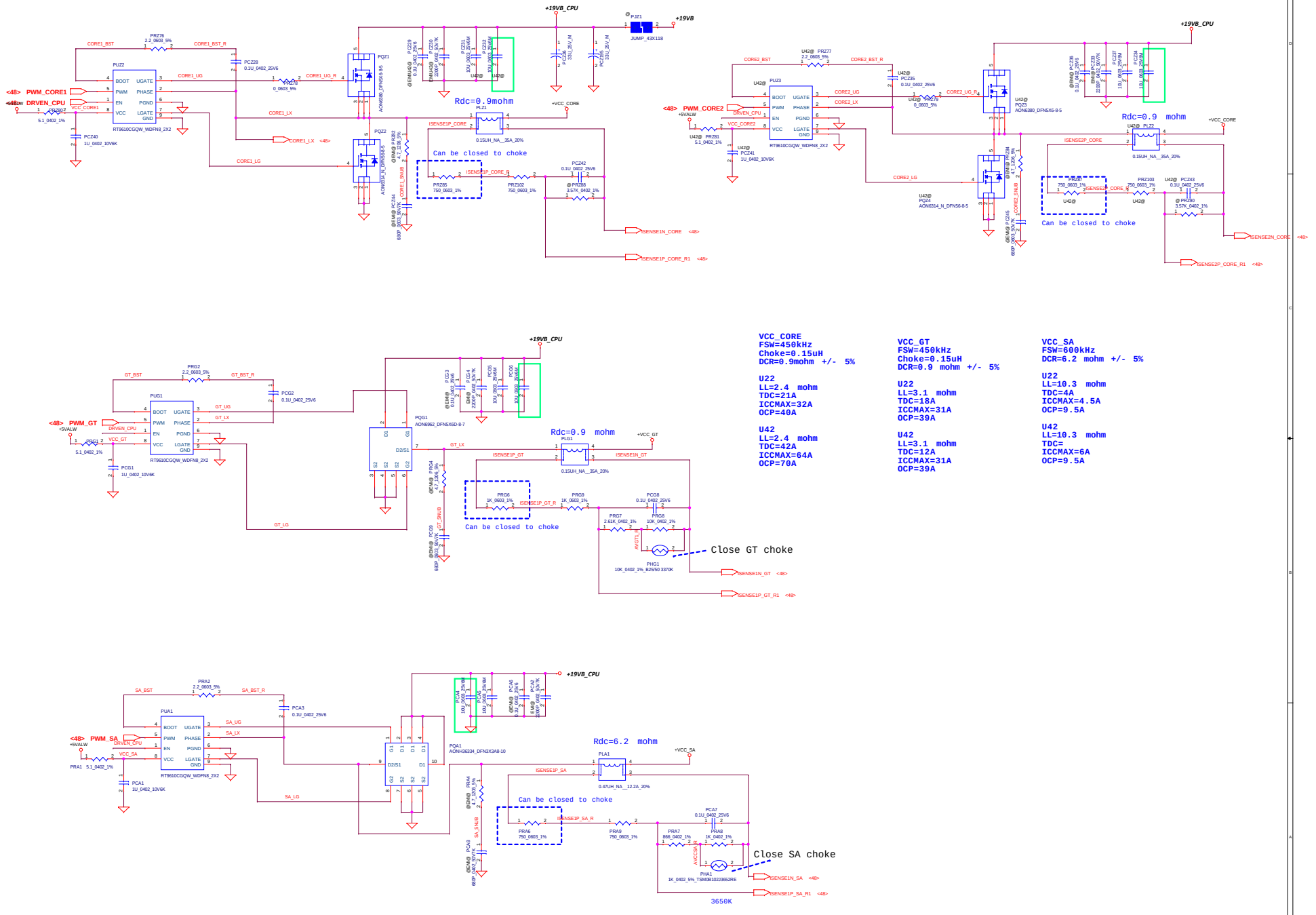
Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: CPU_CORE

Size: Document Number: EH7LW M/B LA-H791P Rev: 0.2

Date: Thursday, June 06, 2019 Sheet 48 of 57



VCC_CORE
FSW=450kHz
Choke=0.15uH
DCR=0.9mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

VCC_GT
FSW=450kHz
Choke=0.15uH
DCR=0.9 mohm +/- 5%

U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

U42
LL=3.1 mohm
TDC=12A
ICCMAX=31A
OCP=39A

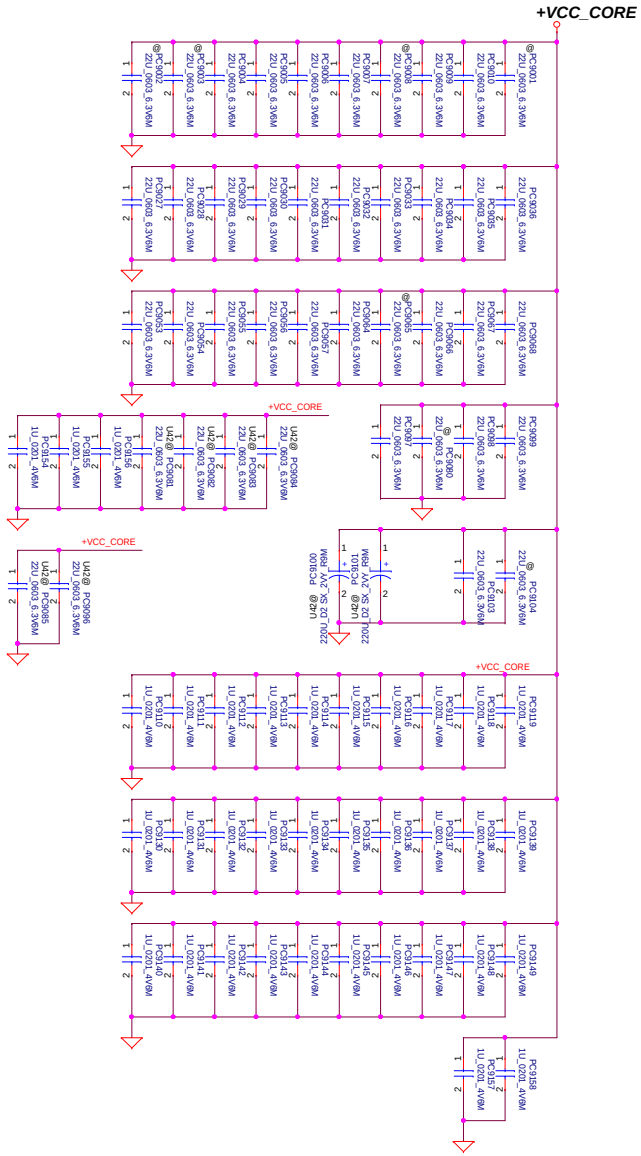
VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

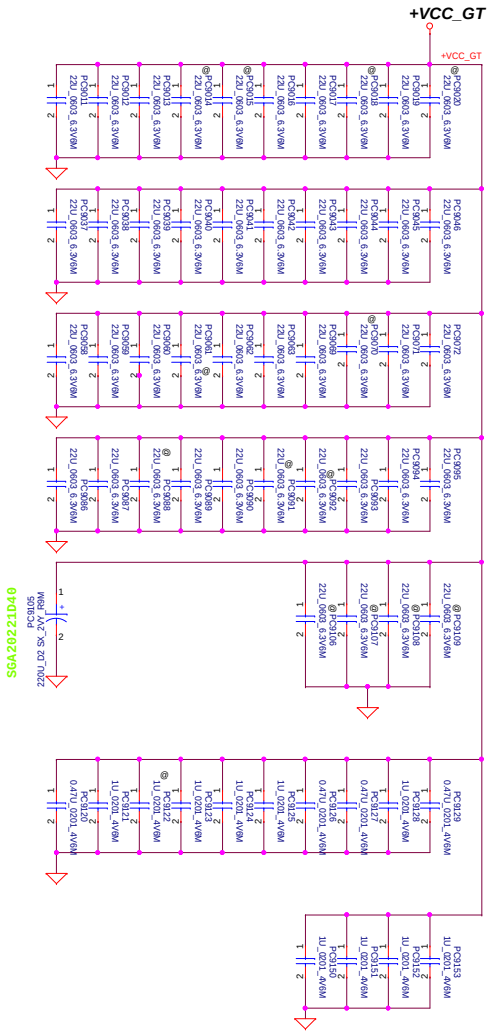
U22
LL=10.3 mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A

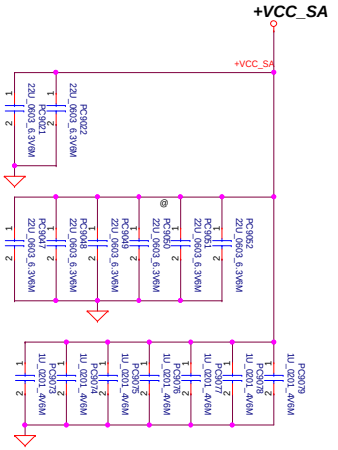
U42
LL=10.3 mohm
TDC=
ICCMAX=6A
OCP=9.5A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Title	CPU Power stage		
Size	Document Number		Rev
	EH7LW M/B LA-H791P		0.2
Date:	Thursday, June 06, 2019	Sheet 49 of 57	







SA
pop:
22uF_0603*7
1uF_0201*7
unpop:
22uF_0603*1

220uF*1
22uF*31
1uF*9
0.47uF*4
unpop:
22uF *13
1uF*1

2017/07/03
VCORE Output Capacitor:
U42
22uF_0603*35
1uF_0201*35
220uF *2
UNPOP
22_0603*7

2017/07/03
VCORE Output Capacitor:
U22
22uF_0603*29
1uF_0201*35
UNPOP
22_0603*7
220uF *2

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	EH7LW M/B LA-H791P	0.2

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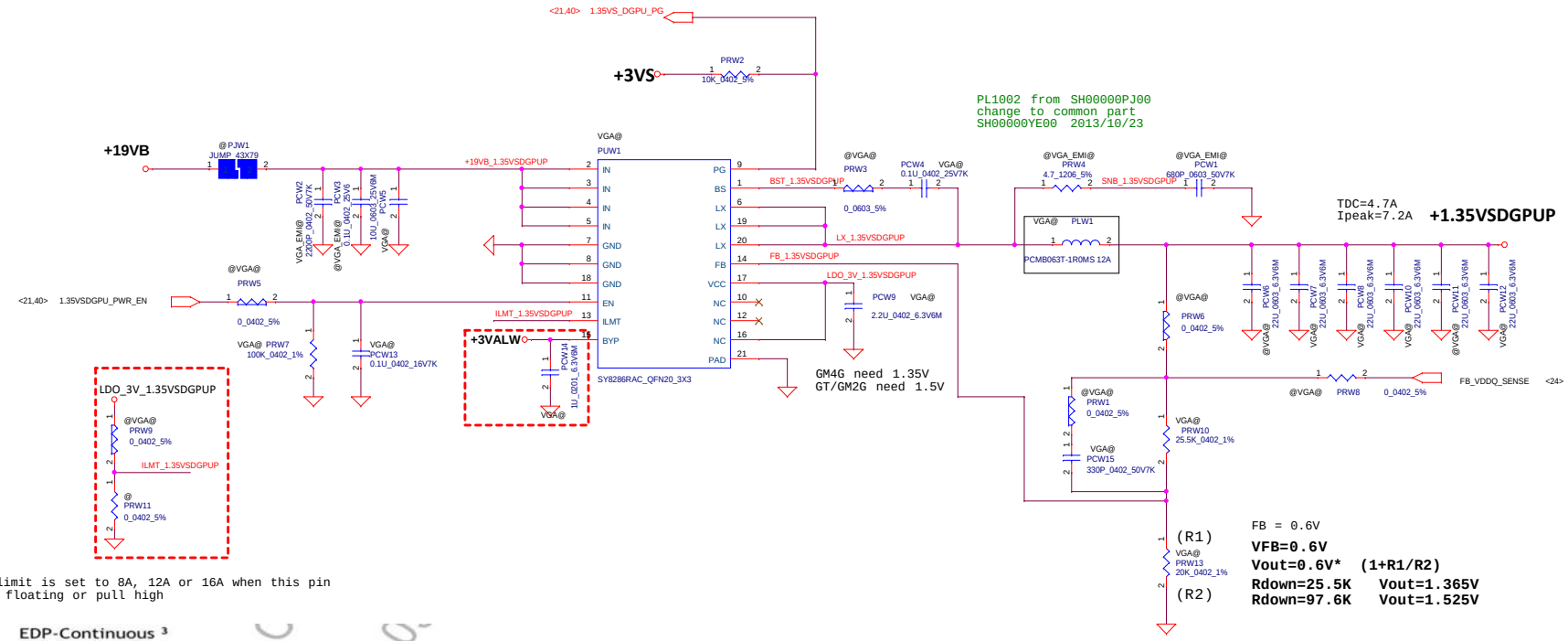
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Table 6. EDP-Continuous [3]

Products	VRAM Type	GPU Core	GPU FBIO		FB Total [1,5]		1.05V Total [2]	3.3V Total
		—	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]	3.3V [4]
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0	—	2.0	—	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5 @ 2.0 GHz	26.5	—	2.0	—	4.2	0.80	0.06
	GDDR5 @ 2.5 GHz	26.5	—	2.0	—	4.7	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GXR	GDDR5	35.4	—	2.4	—	4.9	2.6	0.40

Table 7. EDP-Peak [3]

Products	VRAM Type	GPU Core	GPU FBIO		FB Total [1,5]		1.05V Total [2]
		—	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]
		(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	34.0	—	2.9	—	6.8	2.1
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1
N16S-GTR	GDDR5 @ 2.0 GHz	53.0	—	2.9	—	6.8	2.1
	GDDR5 @ 2.5 GHz	53.0	—	3.1	—	7.2	2.1
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1
N16S-GXR	GDDR5	54.0	—	4.6	—	9.5	2.9

Table 7. Output EDP-Continuous

Product	NVVDD	GPU FBIO	FB Total[5]	1.0V Total[1]	1.8V Total[2]
	—	1.35V[4]	1.35V[4]	1.0V[4]	1.8V[4]
	(A)	(A)	(A)	(A)	(A)
N17S-G1	29.7	2.0	3.4	0.1	0.3
N17S-LG	15.4	1.6	2.8	0.1	0.2

Table 8. Output EDP-Peak

Product	NVVDD	GPU FBIO	FB TOTAL[4]	1.0V Total[1]
	—	1.35V[3]	1.35V[3]	1.0V[3]
	(A)	(A)	(A)	(A)
N17S-G1	59.2	3.2	6.6	0.2
N17S-LG	49.6	3.2	6.6	0.2

Security Classification	Compal Secret Data		
Issued Date	2018/12/27	Deciphered Date	2019/12/27

Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	EH7LW M/B LA-H791P	0.2

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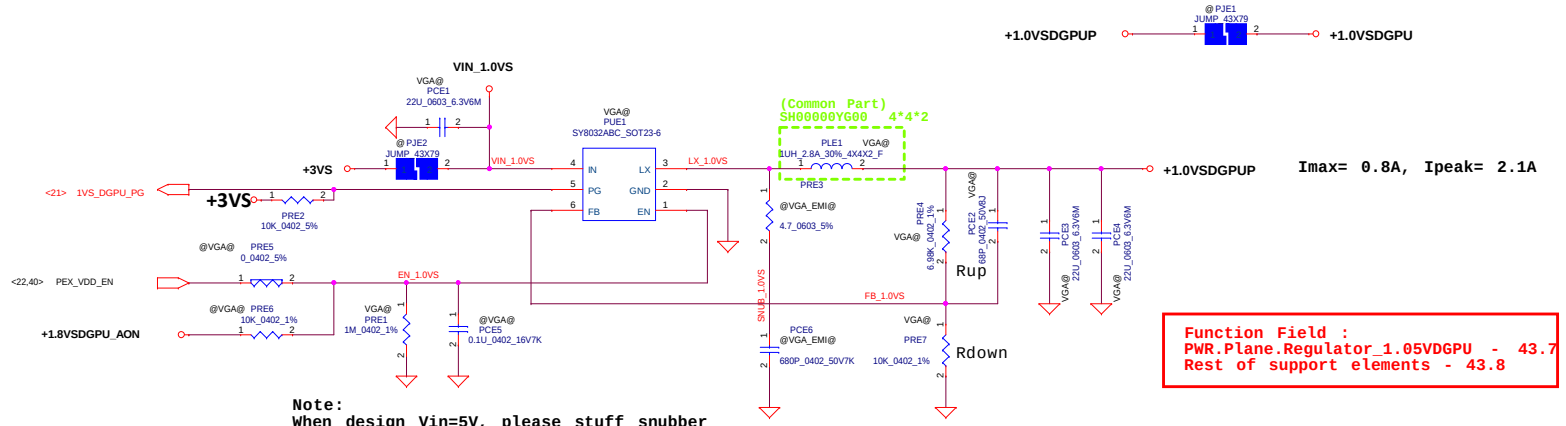
Module model information

SY8032_V2.mdd



Function Field :
PWR.Plane.Regulator_1.05VDGPU - 43.7
Rest of support elements - 43.8

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)
N16=>1.05V
=>0.6V*(1+(7.68/10)=1.061 (1.01%)
=>0.6V*(1+(7.32/10)=1.039 (-1%)

N17=>1.0V
Vout=0.6V*(1+(6.98/10)=1.019V (1.02%)

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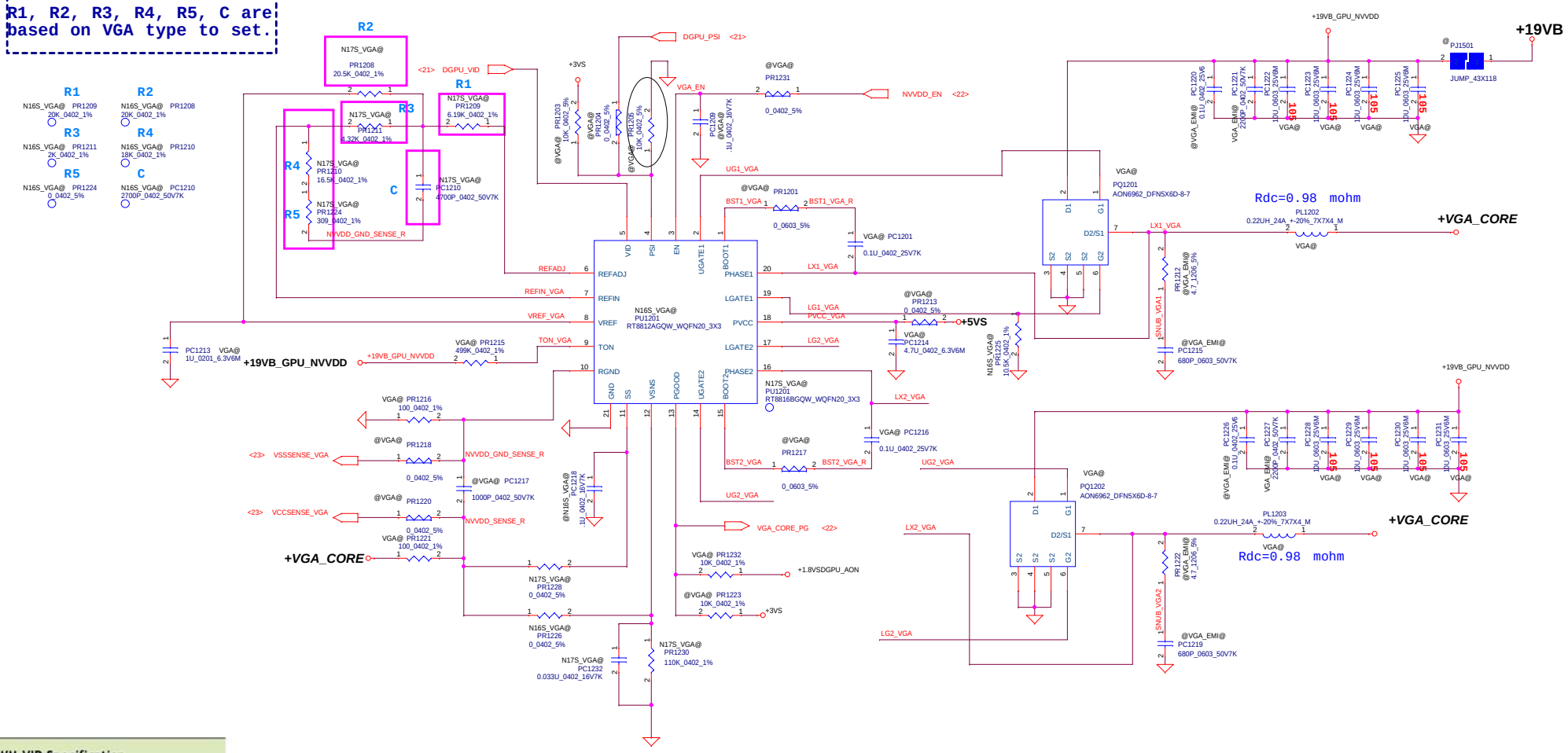
R1, R2, R3, R4, R5, C are based on VGA type to set.

unmount PRV5 for 2 phase select



PWM-VID Specification		
		Config B
Vmin	V	0.6
Vmax	V	1.2
Vboot	V	0.9
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	96
PWM Frequency F_{PWM}	MHz	1.125
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	20
R2 (1%)	KΩ	20
R3 (1%)	KΩ	2
R4 (1%)	KΩ	18
R5 (1%)	KΩ	0
C	nF	2.7

N17x DG-07875-001_v08.pdf:

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7

Table 6. EDP-Continuous [3]

Products	VRAM Type	GPU Core — (A)
N16S-GMR	GDDR5	19.0
	DDR3/L	21.0
N16S-GTR	GDDR5 @ 2.0 GHz	26.5
	GDDR5 @ 2.5 GHz	26.5
	DDR3/L	26.0
N16S-GXR	GDDR5	35.4

Table 7. EDP-Peak [3]

Products	VRAM Type	GPU Core — (A)
N16S-GMR	GDDR5	34.0
	DDR3/L	39.5
N16S-GTR	GDDR5 @ 2.0 GHz	53.0
	GDDR5 @ 2.5 GHz	53.0
	DDR3/L	51.0
N16S-GXR	GDDR5	54.0

Table 7. Output EDP-Continuous

Product	NVVDD — (A)	GPU FBIO 1.35V[4] (A)	FB Total[5] 1.35V[4] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17S-G1	29.7	2.0	3.4	0.1	0.3
N17S-LG	15.4	1.6	2.8	0.1	0.2

Table 8. Output EDP-Peak

Product	NVVDD — (A)	GPU FBIO 1.35V[3] (A)	FB TOTAL[4] 1.35V[3] (A)	1.0V Total[1] 1.0V[3] (A)
N17S-G1	59.2	3.2	6.6	0.2
N17S-LG	49.6	3.2	6.6	0.2

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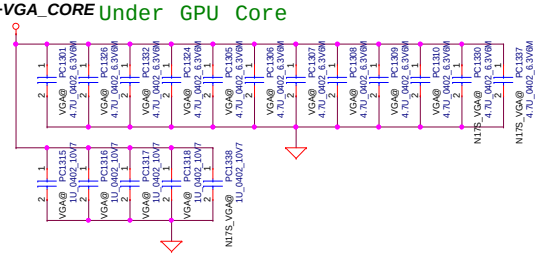
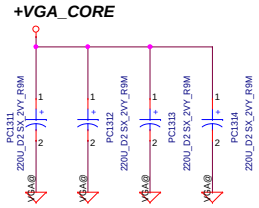
GB4-128 package

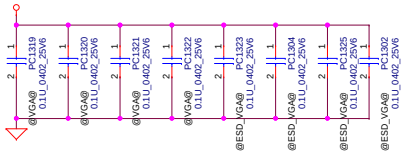
+VGA_CORE Under GPU Core



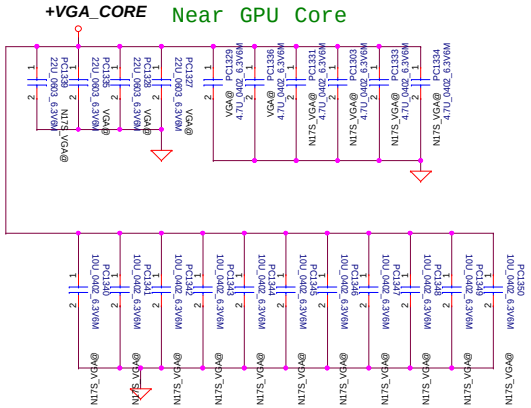
+VGA_CORE



+VGA_CORE



+VGA_CORE Near GPU Core



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Reserve gpu prochot function	Reserve gpu prochot function		P.43	Del PQB8 for function reserve.	19.0103	EVT
02	change PL502 to common part	change PL502 to common part		P.44	change PL502 to common part(SH000016700)	19.0212	DVT
03	change PR1230 to 110K	change PR1230 to 110K for ocp setting		P.53	change PR1230 to 110K(SD034110380)	19.0212	DVT
04	change CAP size to 0402	change CAP size to 0402 for cost down		P.43,44	change PC302,PC502,PCB11 to SE00000W210 change PCB1 to SE074102K80	19.0212	DVT
05	change 0 ohm to R-short	change 0 ohm to R-short for cost down			change PR101,PR217,PR210,PRB15,PRB17,PRB23,PRB26,PRB16,PR304,PR505,PR502,PRM8,PRM11, PRM12,PRF3,PRF8,PRF1,PR1801,PRZ15,PRZ94,PRZ47,PRZ95,PRZ50,PRZ93,PRZ25,PRW5,PRW9, PRW6,PRW1,PRW3,PRE5,PR1231,PR1204,PR1218,PR1220,PR1201,PR1217,PR1213 to R-short (38PCS)	19.0212	DVT
06	DDR sequence	change PRM8 to 48.7K and PCM18 to 0.1u for sequence		P.38	change PRM8 to SD034487280 change PCM18 to SE102104K00	19.0215	DVT
07	CPU transient	change R and C value for CPU transient test		P.48	change PCZ11 to 330PuF(SE074331K80) change PRZ45 to 63.4k ohm(SD03463K280)(U42) change PRZ49 to 5.49k ohm(SD034549180)	19.0218	DVT
08	DDR sequence	change PRM8 to 0 ohm and del PCM18 for sequence		P.38	change PRM8 to SD028000080 del PCM18	19.0328	PVT
09	VR thermal alert adjust	change protect from 100c to 110c		P.48	change PHZ2,PHZ3 to SL200002I00, change PRZ51,PRZ66 to SD000000680, change PRZ52,PRZ69 to SD034332280, change PRZ67 to SD00000WS80,change PRZ63 to SD034130280, change PRZ70 to SD034137180,change PRZ68 to SD034392180, change PRZ64 to SD034976180,change PRZ71 to SD00000WS80,change PRZ74 to SD034165280	19.0507	pre MP
10							
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HW Schematic chang list (P.I.R)

Date	Rev.	Modify Item
1/25	0.2	Add cnvi cap(CM4) as intel request Swap JFP1 pin define update JIO1 pin define update H12 hole,downsize C2034/C2750
1/29	0.2	update JIO1 pin define change 0-ohm to R-short remove SWK1
2/12	0.2	change RA3/RA4 to 0805 size
3/13	1A	update UL2 pin28/pin29 pin define Add DA3/DA4 for audio ESD protection update JIO1 footprint
5/9	1B	update RC262 75k for CML

Date	Rev.	Modify Item

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HW Schematic chang list (P.I.R)

Item	Page	Date	Rev.	Reason for change	Modify Item

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Title: *HW-P.I.R page2*

Size	Document Number	Rev
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