16932 Buzz_KBL
Schematics Document

DY : None Installed
UMA: UMA only installed
DIS: DISCRTE OPTIMUS installed

DIS

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

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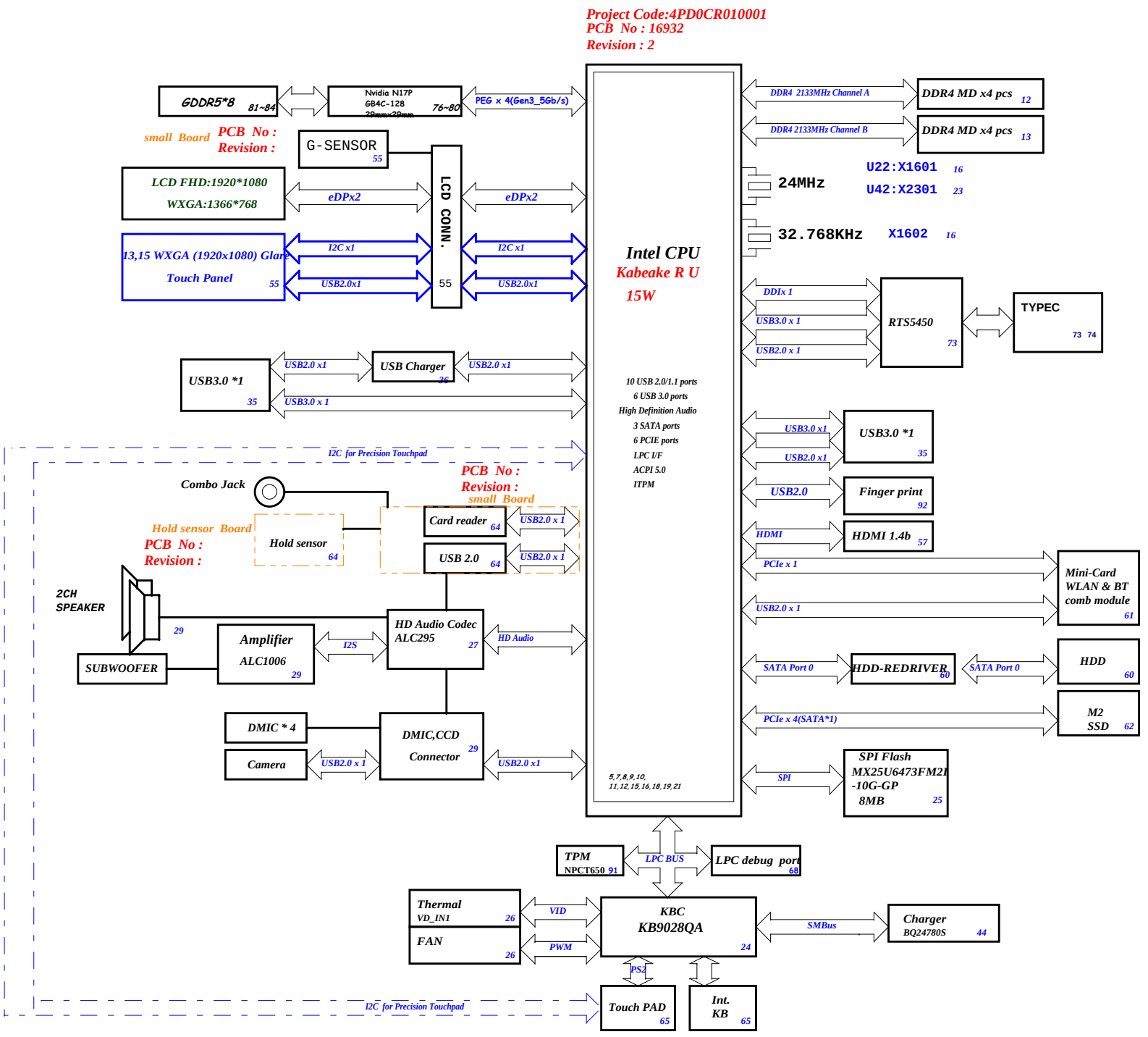

GPU DC/DC RT8813DGQW-GP 85	
INPUTS	OUTPUTS
5V_S0	1V_VGACORE_S0

GPU DC/DC RT8816AGQW-GP 85	
INPUTS	OUTPUTS
5V_S5	1V_VGACORE1_S0

GPU DC/DC RT8816AGQW-GP 86	
INPUTS	OUTPUTS
5V_S5	1D35V_VGA_S0

GPU DC/DC SY8003ADFC-GP 86	
INPUTS	OUTPUTS
3D3V_S5	1D8V_AON_S0

GPU DC/DC APE8939GN3-GP 86	
INPUTS	OUTPUTS
1D8V_AON_S0	1D8V_VGA_S0

GPU DC/DC APE8939GN3-GP 86	
INPUTS	OUTPUTS
1D0V_S5	1V_1D05V_VGA_S0

GPU DC/DC RT8068A 88	
INPUTS	OUTPUTS
3D3V_S5	1V_1D05V_VGA_S0

CPU DC/DC TPS22976DPUR 88	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0 3D3V_AON_S0

CHARGER BQ24780S 44	
INPUTS	OUTPUTS
AD+ BT+	19V_DCBATOUT

SYSTEM DC/DC RT6228CGQUF-GP 45	
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5 5V_S5

SYSTEM DC/DC RT6226BGQUF-GP 45	
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_S5

CPU DC/DC RT3602 46-47	
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE

CPU DC/DC AOZ5049 48	
INPUTS	OUTPUTS
19V_DCBATOUT	1V_VCCGT

CPU DC/DC RT9610B 50	
INPUTS	OUTPUTS
5V_S5	1V_VCCSA

CPU DC/DC G5388K11U-GP 51	
INPUTS	OUTPUTS
5V_S5	PWR_VDDQ

CPU DC/DC APL5930KAI 51	
INPUTS	OUTPUTS
5V_S5	2D5V_S3

SYSTEM DC/DC G5388K11U-GP 52	
INPUTS	OUTPUTS
5V_S5	1D0V_S5

SYSTEM DC/DC 9661-25ADJ 53	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

SYSTEM Load switch TPS22976 40	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
5V_S5	5V_S0
1D0V_S5	1V_VCCST
1D8V_S5	1D8V_S0

SYSTEM Load switch APE8939 40	
INPUTS	OUTPUTS
1D0V_S5	1V_VCCIO

DIS

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Title: Block Diagram

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Main Func = CPU

eDP

[55] eDP_TX_CPU_N0
[55] eDP_TX_CPU_P0
[55] eDP_TX_CPU_N1
[55] eDP_TX_CPU_P1

[55] eDP_AUX_CPU_N
[55] eDP_AUX_CPU_P

[55] eDP_HPD_CPU
[24] eDP_BLEN_CPU
[55] eDP_BLCTRL_CPU
[55] eDP_VDDEN_CPU

HDMI

[57] HDMI_DATA_CPU_N2
[57] HDMI_DATA_CPU_P2
[57] HDMI_DATA_CPU_N1
[57] HDMI_DATA_CPU_P1
[57] HDMI_DATA_CPU_N0
[57] HDMI_DATA_CPU_P0
[57] HDMI_DATA_CPU_N3
[57] HDMI_DATA_CPU_P3

[14,57] HDMI_CLK_CPU
[14,57] HDMI_DATA_CPU

[57] HDMI_DET_CPU

TYPEC

[73] DP_DDI_TX_N0
[73] DP_DDI_TX_P0
[73] DP_DDI_TX_N1
[73] DP_DDI_TX_P1
[73] DP_DDI_TX_N2
[73] DP_DDI_TX_P2
[73] DP_DDI_TX_N3
[73] DP_DDI_TX_P3

[73] DP_AUX_CPU_N

[73] DP_AUX_CPU_P

[14] DDPC_CTRLDATA

[14] DDPD_CDA

[73] DP_HPD_CON

[24] EC_SMI#
[24] EC_SCI#

HDMI

HDMI_DATA_CPU_N2 E55
HDMI_DATA_CPU_P2 F55
HDMI_DATA_CPU_N1 E58
HDMI_DATA_CPU_P1 F58
HDMI_DATA_CPU_N0 F53
HDMI_DATA_CPU_P0 G53
HDMI_DATA_CPU_N3 F56
HDMI_DATA_CPU_P3 G56

TYPEC

DP_DDI_TX_N0 C50
DP_DDI_TX_P0 D50
DP_DDI_TX_N1 C52
DP_DDI_TX_P1 D52
DP_DDI_TX_N2 A50
DP_DDI_TX_P2 B50
DP_DDI_TX_N3 D51
DP_DDI_TX_P3 C51

HDMI

HDMI_CLK_CPU L13
HDMI_DATA_CPU L12

DDPC_CTRLDATA N7 N8

DDPD_CDA N11 N12

1V_VCCIO

R301 1 2 24D9R2F-L-GP

EDP_RCOMP E52

CPU1A

SKYLAKE_ULT

1 OF 20

DDI1_TXN[0]
DDI1_TXP[0]
DDI1_TXN[1]
DDI1_TXP[1]
DDI1_TXN[2]
DDI1_TXP[2]
DDI1_TXN[3]
DDI1_TXP[3]

DDI

DDI2_TXN[0]
DDI2_TXP[0]
DDI2_TXN[1]
DDI2_TXP[1]
DDI2_TXN[2]
DDI2_TXP[2]
DDI2_TXN[3]
DDI2_TXP[3]

DISPLAY SIDEBANDS

GPP_E18/DDPB_CTRLCLK
GPP_E19/DDPB_CTRLDATA
Strap

GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA
Strap

GPP_E22
GPP_E23
Strap

EDP_RCOMP

SKYLAKE-U-GP

EDP

EDP_TXN[0] C47 eDP_TX_CPU_N0
EDP_TXP[0] C46 eDP_TX_CPU_P0
EDP_TXN[1] D46 eDP_TX_CPU_N1
EDP_TXP[1] C45 eDP_TX_CPU_P1
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_AUXN E45 eDP_AUX_CPU_N
EDP_AUXP F45 eDP_AUX_CPU_P

EDP_DISP_UTIL B52

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48 DP_AUX_CPU_N
DDI2_AUXP F48 DP_AUX_CPU_P
RSVD#G46 G46
RSVD#F46 F46

GPP_E13/DDPB_HPD0 L9 HDMI_DET_CPU
GPP_E14/DDPC_HPD1 L7 DP_HPD_CON
GPP_E15/DDPD_HPD2 L6 EC_SMI#
GPP_E16/DDPE_HPD3 N9 EC_SCI#
GPP_E17/EDP_HPD L10 eDP_HPD_CPU

EDP_BKLTEN R12 eDP_BLEN_CPU
EDP_BKLTCTL R11 eDP_BLCTRL_CPU
EDP_VDDEN U13 eDP_VDDEN_CPU

eDP

CPU

3D3V_S0
SB

R302 10KR2F-L1-GP
EC_SMI# 1 2
DY
R307
EC_SCI# 2K2R2J-L1-GP

eDP_BLEN_CPU 1 R304 100KR2F-L3-GP
DP_HPD_CON 1 R320 100KR2F-L3-GP

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

DIS

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Title: CPU_(DISPLAY)

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Main Func = CPU

DDR4 ball type:NON Interleaved Type

CPU1B — SKYLAKE_ULT — 2 OF 20

M_A_DQ[0:7]
M_A_DQ0 AL71 — DDR0_DQ[0]
M_A_DQ1 AL68 — DDR0_DQ[1]
M_A_DQ2 AN68 — DDR0_DQ[2]
M_A_DQ3 AN69 — DDR0_DQ[3]
M_A_DQ4 AL70 — DDR0_DQ[4]
M_A_DQ5 AL69 — DDR0_DQ[5]
M_A_DQ6 AN70 — DDR0_DQ[6]
M_A_DQ7 AN71 — DDR0_DQ[7]

M_A_DQ[8:15]
M_A_DQ8 AR70 — DDR0_DQ[8]
M_A_DQ9 AR68 — DDR0_DQ[9]
M_A_DQ10 AU71 — DDR0_DQ[10]
M_A_DQ11 AU68 — DDR0_DQ[11]
M_A_DQ12 AR71 — DDR0_DQ[12]
M_A_DQ13 AR69 — DDR0_DQ[13]
M_A_DQ14 AU70 — DDR0_DQ[14]
M_A_DQ15 AU69 — DDR0_DQ[15]

M_A_DQ[16:23]
M_A_DQ16 AF65 — DDR1_DQ[0]/DDR0_DQ[16]
M_A_DQ17 AF64 — DDR1_DQ[1]/DDR0_DQ[17]
M_A_DQ18 AK65 — DDR1_DQ[2]/DDR0_DQ[18]
M_A_DQ19 AK64 — DDR1_DQ[3]/DDR0_DQ[19]
M_A_DQ20 AF66 — DDR1_DQ[4]/DDR0_DQ[20]
M_A_DQ21 AF67 — DDR1_DQ[5]/DDR0_DQ[21]
M_A_DQ22 AK67 — DDR1_DQ[6]/DDR0_DQ[22]
M_A_DQ23 AK66 — DDR1_DQ[7]/DDR0_DQ[23]

M_A_DQ[24:31]
M_A_DQ24 AF70 — DDR1_DQ[8]/DDR0_DQ[24]
M_A_DQ25 AF68 — DDR1_DQ[9]/DDR0_DQ[25]
M_A_DQ26 AH71 — DDR1_DQ[10]/DDR0_DQ[26]
M_A_DQ27 AH68 — DDR1_DQ[11]/DDR0_DQ[27]
M_A_DQ28 AF71 — DDR1_DQ[12]/DDR0_DQ[28]
M_A_DQ29 AF69 — DDR1_DQ[13]/DDR0_DQ[29]
M_A_DQ30 AH70 — DDR1_DQ[14]/DDR0_DQ[30]
M_A_DQ31 AH69 — DDR1_DQ[15]/DDR0_DQ[31]

M_A_DQ[32:39]
M_A_DQ32 BB65 — DDR0_DQ[16]/DDR0_DQ[32]
M_A_DQ33 AW65 — DDR0_DQ[17]/DDR0_DQ[33]
M_A_DQ34 AW63 — DDR0_DQ[18]/DDR0_DQ[34]
M_A_DQ35 AY63 — DDR0_DQ[19]/DDR0_DQ[35]
M_A_DQ36 BA65 — DDR0_DQ[20]/DDR0_DQ[36]
M_A_DQ37 AY65 — DDR0_DQ[21]/DDR0_DQ[37]
M_A_DQ38 BA63 — DDR0_DQ[22]/DDR0_DQ[38]
M_A_DQ39 BB63 — DDR0_DQ[23]/DDR0_DQ[39]

M_A_DQ[40:47]
M_A_DQ40 BA61 — DDR0_DQ[24]/DDR0_DQ[40]
M_A_DQ41 AW61 — DDR0_DQ[25]/DDR0_DQ[41]
M_A_DQ42 BB59 — DDR0_DQ[26]/DDR0_DQ[42]
M_A_DQ43 AW59 — DDR0_DQ[27]/DDR0_DQ[43]
M_A_DQ44 BB61 — DDR0_DQ[28]/DDR0_DQ[44]
M_A_DQ45 AY61 — DDR0_DQ[29]/DDR0_DQ[45]
M_A_DQ46 BA59 — DDR0_DQ[30]/DDR0_DQ[46]
M_A_DQ47 AY59 — DDR0_DQ[31]/DDR0_DQ[47]

M_A_DQ[48:55]
M_A_DQ48 AT66 — DDR1_DQ[16]/DDR0_DQ[48]
M_A_DQ49 AU66 — DDR1_DQ[17]/DDR0_DQ[49]
M_A_DQ50 AP65 — DDR1_DQ[18]/DDR0_DQ[50]
M_A_DQ51 AN65 — DDR1_DQ[19]/DDR0_DQ[51]
M_A_DQ52 AN66 — DDR1_DQ[20]/DDR0_DQ[52]
M_A_DQ53 AP66 — DDR1_DQ[21]/DDR0_DQ[53]
M_A_DQ54 AT65 — DDR1_DQ[22]/DDR0_DQ[54]
M_A_DQ55 AU65 — DDR1_DQ[23]/DDR0_DQ[55]

M_A_DQ[56:63]
M_A_DQ56 AT61 — DDR1_DQ[24]/DDR0_DQ[56]
M_A_DQ57 AU61 — DDR1_DQ[25]/DDR0_DQ[57]
M_A_DQ58 AP60 — DDR1_DQ[26]/DDR0_DQ[58]
M_A_DQ59 AN60 — DDR1_DQ[27]/DDR0_DQ[59]
M_A_DQ60 AN61 — DDR1_DQ[28]/DDR0_DQ[60]
M_A_DQ61 AP61 — DDR1_DQ[29]/DDR0_DQ[61]
M_A_DQ62 AT60 — DDR1_DQ[30]/DDR0_DQ[62]
M_A_DQ63 AU60 — DDR1_DQ[31]/DDR0_DQ[63]

DDR CH - A

DDR0_CKN[0] AU53 M_A_CLK#0
DDR0_CKP[0] AT53 M_A_CLK0 — A-CLK
DDR0_CKN[1] AU55
DDR0_CKP[1] AT55

DDR0_CKE[0] BA56 M_A_CKE0 — A-CTRL-CKE
DDR0_CKE[1] BB56
DDR0_CKE[2] AW56
DDR0_CKE[3] AY56

DDR0_CS#[0] AU45 M_A_CS#0 — A-CTRL-CS
DDR0_CS#[1] AU43
DDR0_ODT[0] AT45 M_A_ODT0 — A-CTRL-ODT
DDR0_ODT[1] AT43

DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5] BA51 M_A_A5
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9] BB54 M_A_A9
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6] BA52 M_A_A6
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8] AY52 M_A_A8
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7] AW52 M_A_A7
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0] AY55 M_A_BG0 — A-CMD-MA
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12] AW54 M_A_A12
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11] BA54 M_A_A11
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT# BA55 M_A_ACT_N
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1] AY54 M_A_BG1

DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13] AU46 M_A_A13
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15] AU48 M_A_A15
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14] AT46 M_A_A14
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16] AU50 M_A_A16 — A-CMD-MA
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0] AU52 M_A_BA0
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2] AY51 M_A_A2
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1] AT48 M_A_BA1
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10] AT50 M_A_A10
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1] BB50 M_A_A1
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0] AY50 M_A_A0
DDR0_MA[3] BA50 M_A_A3
DDR0_MA[4] BB52 M_A_A4

DDR0_DQSN[0] AM70 M_A_DQS_DN0 — M_A_DQS0
DDR0_DQSP[0] AM69 M_A_DQS_DP0
DDR0_DQSN[1] AT69 M_A_DQS_DN1 — M_A_DQS1
DDR0_DQSP[1] AT70 M_A_DQS_DP1
DDR1_DQSN[0]/DDR0_DQSN[2] AH66 M_A_DQS_DN2 — M_A_DQS2
DDR1_DQSP[0]/DDR0_DQSP[2] AH65 M_A_DQS_DP2
DDR1_DQSN[1]/DDR0_DQSN[3] AG69 M_A_DQS_DN3 — M_A_DQS3
DDR1_DQSP[1]/DDR0_DQSP[3] AG70 M_A_DQS_DP3
DDR0_DQSN[2]/DDR0_DQSN[4] BA64 M_A_DQS_DN4 — M_A_DQS4
DDR0_DQSP[2]/DDR0_DQSP[4] AY64 M_A_DQS_DP4
DDR0_DQSN[3]/DDR0_DQSN[5] AY60 M_A_DQS_DN5 — M_A_DQS5
DDR0_DQSP[3]/DDR0_DQSP[5] BA60 M_A_DQS_DP5
DDR1_DQSN[2]/DDR0_DQSN[6] AR66 M_A_DQS_DN6 — M_A_DQS6
DDR1_DQSP[2]/DDR0_DQSP[6] AR65 M_A_DQS_DP6
DDR1_DQSN[3]/DDR0_DQSN[7] AR61 M_A_DQS_DN7 — M_A_DQS7
DDR1_DQSP[3]/DDR0_DQSP[7] AR60 M_A_DQS_DP7

DDR0_ALERT# AW50 M_A_ALERT_N
DDR0_PAR AT52 M_A_PARITY

DDR_VREF_CA AY67 V_SMA_VREF_CA
DDR0_VREF_DQ AY68
DDR1_VREF_DQ BA67 V_SMB_VREF_CA

DDR_VTT_CNTL AW67 SM_PGCNTL

SKYLAKE-U-GP

CPU 071.SKYLA.000U

[12] M_A_DQ0 … [12] M_A_DQ63
[12] M_A_A5 … [12] M_A_A13
[12] M_A_ACT_N
[12] M_A_BG0
[12] M_A_BG1
[12] M_A_BA0
[12] M_A_BA1
[12] M_A_A0 … [12] M_A_A4
[12] M_A_A14 … [12] M_A_A15
[12] M_A_ALERT_N
[12] M_A_PARITY
[12] V_SMA_VREF_CA
[13] V_SMB_VREF_CA
[51] VTT_CNTL_CPU
[12] M_A_CLK#0
[12] M_A_CLK0
[12] M_A_CKE0
[12] M_A_CS#0
[12] M_A_ODT0
[12] M_A_DQS_DN0 … [12] M_A_DQS_DN7
[12] M_A_DQS_DP0 … [12] M_A_DQS_DP7

3D3V_S0
1D2V_S3
R401 220KR2F-GP
Q401
G
D
S
SM_PGCNTL
VTT_CNTL_CPU
Vth(max)=1.1V
PJA138KA-GP
084.00138.0A31
2nd = 84.05067.031

DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(DDR)
Size: Custom
Document Number: Buzz_KBL
Rev: 2
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Main Func = CPU

DDR4 ball type:NON Interleaved Type

CPU1C — 3 OF 20 — SKYLAKE_ULT

M_B_DQ[0:7]
M_B_DQ[8:15]
M_B_DQ[16:23]
M_B_DQ[24:31]
M_B_DQ[32:39]
M_B_DQ[40:47]
M_B_DQ[48:55]
M_B_DQ[56:63]

B-CLK
B-CTRL-CKE
B-CTRL-CS
B-CTRL-ODT
B-CMD-MA
B-CMD-MA
B-CMD-MA
B-CMD-MA

M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7

DDR CH - B

SKYLAKE-U-GP

071.SKYLA.000U

CPU

#543016

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

	R501
DDP	121ohm(64.12105.6DL)
SDP	200ohm(64.20005.6DL)

close CPU

SM_DRAMRST# CPU — ED501 A25735-01FDR7G-GP DY

Figure 5-14. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology
Memory Down Strobe/Data/Reset/RCOMP Signal Topologies

SKL U — VDDQ — R1 — R2 — C1 — DRAM Device — Reset — Strobe, Data — RCOMP — VIA #1 — VIA #2 — VIA #3
R1=470 ohm , R2=0 ohm
C1=0.1uF

1D2V_S3 — R506 470R2F-GP — SM_DRAMRST#

R501 SDP 200R2F-L-GP
R501 DDP 121R2F-GP
R504 0R0402-PAD
R502 80D6R2F-L-GP
R503 100R2F-L3-GP

Layout Note:

C501 SC100P50V2JN-L-GP

DIS

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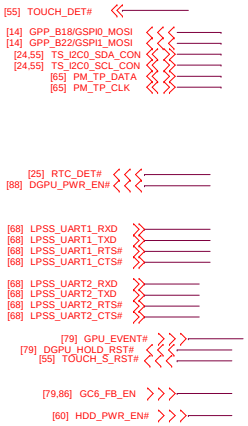
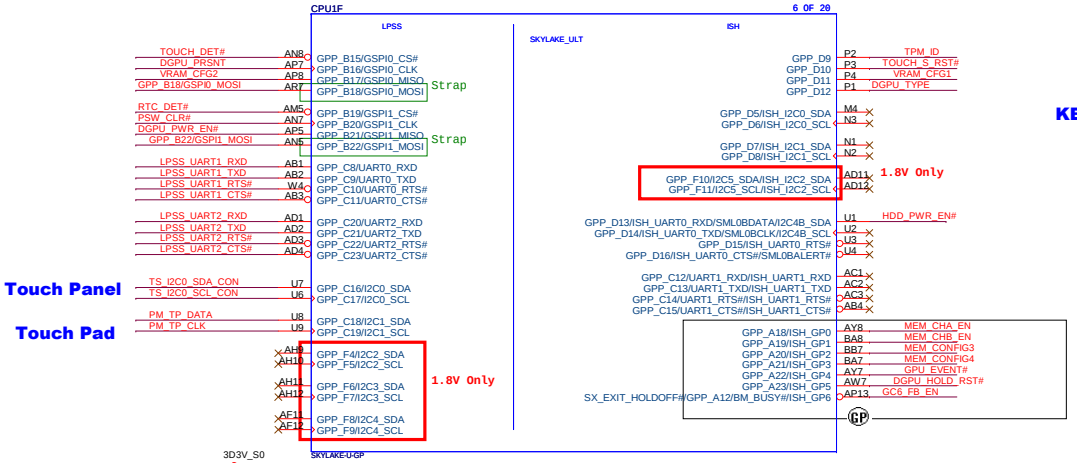
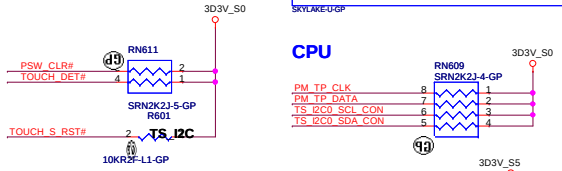
Taipei Hsien 221, Taiwan, R.O.C.

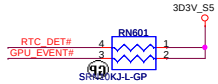
Title: CPU_(DDR)
Size: Custom — Document Number: Buzz_KBL — Rev: 2
Date: Friday, July 07, 2017 — Sheet 5 of 106

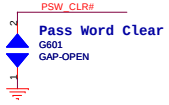
Main Func = PCH

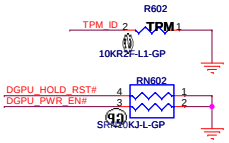


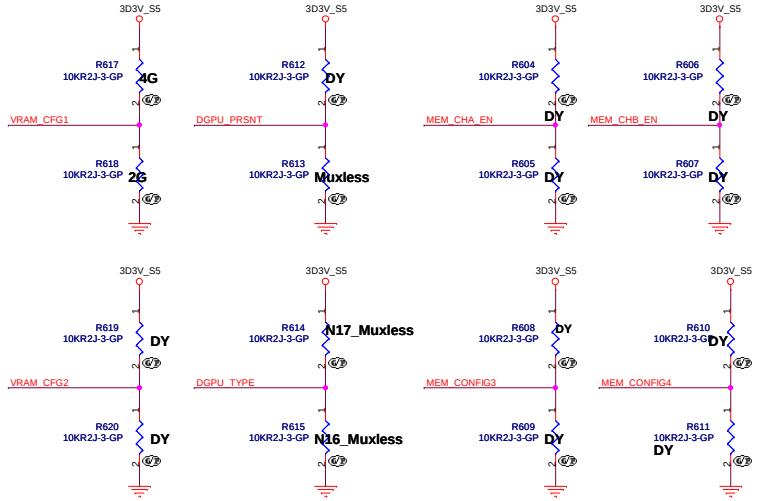












GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

PCH_GPIO	Pull-High	Pull-Low
DGPU_PRSNT	UMA	DIS
DGPU_TYPE	N17	N16
VRAM_CFG1	4G	2G
VRAM_CFG2	NA	NA

Vendor	CONFIG4 (GPP_A19)	CONFIG3 (GPP_A18)	CONFIG2 (GPP_A21)	CONFIG1 (GPP_A20)	Mfr. PN	Wistron . P/N	Capacity
HYNIX	0	0	0	0	H5AN8G6NAFR-UHC	KN.8GB0G.049	8Gb
MICRON	0	0	0	1	MT40A512M16JY-083E:B	KN.8GB04.013	8Gb
SAMSUNG	0	0	1	0	K4A8G165WB-BCRC	KN.8GB0B.048	8Gb
HYNIX	0	0	1	1	H5AN4G6NAFR-TF	KN.0040G.015	4Gb
HYNIX	0	1	0	0	H5AN4G6NAFR-UHC	KN.0040G.016	4Gb
MICRON	0	1	0	1	MT40A256M16GE-083E:B	KN.00404.010	4Gb
SAMSUNG	0	1	1	0	K4A4G165WE-BCRC	KN.0040B.014	4Gb
HYNIX	0	1	1	1	H5ANAG6NAMR-UHC	KN.0160G.010	16Gb
MICRON	1	0	0	0	MT40A1G16WBU-083E:B	KN.01604.001	16Gb

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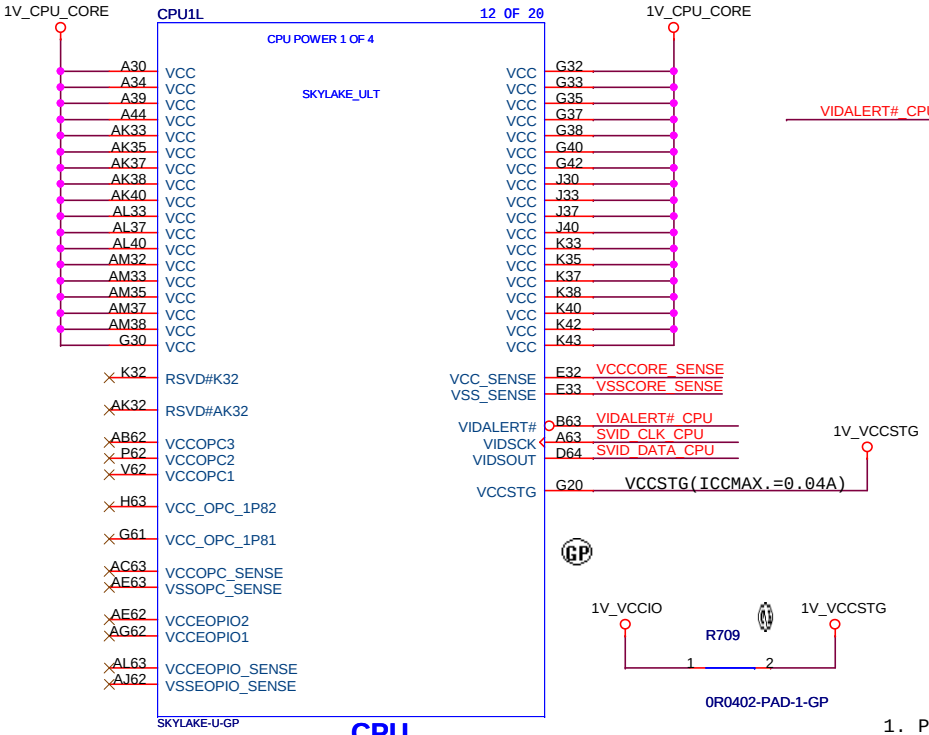
Main Func = CPU

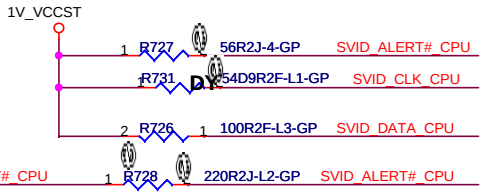
SVID

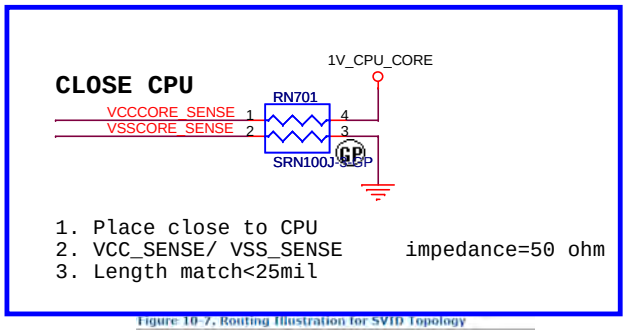
[7,46] SVID_ALERT#_CPU
[7,46] SVID_CLK_CPU
[7,46] SVID_DATA_CPU

[7,46] VCCCORE_SENSE
[7,46] VSSCORE_SENSE
[7,46] SVID_ALERT#_CPU
[7,46] SVID_CLK_CPU
[7,46] SVID_DATA_CPU
[7,46] VCCCORE_SENSE
[7,46] VSSCORE_SENSE



CPU





Layout Note

1. Place close to
2. VCC_SENSE/ VSS
   impedance=50
3. Length match<2

Figure 10-7. Routing Illustration for SVID Topology

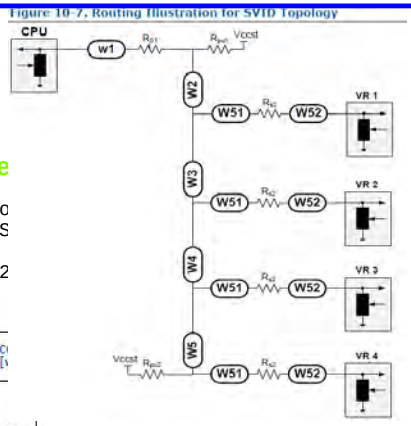


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VC [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

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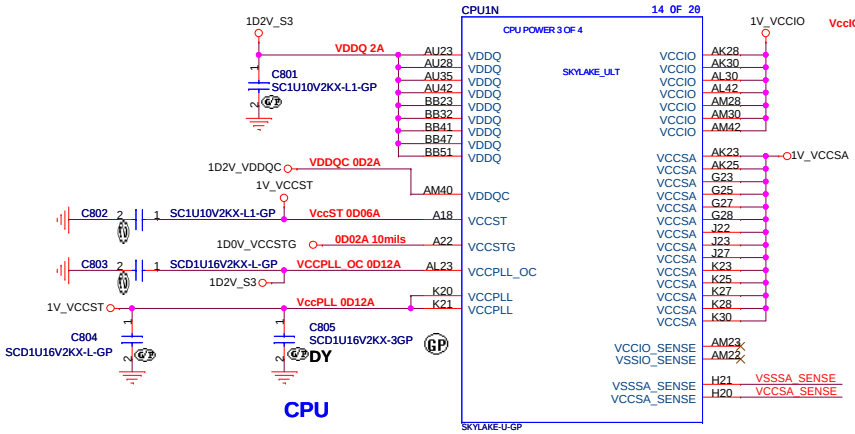
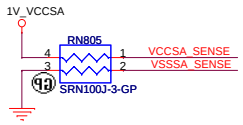
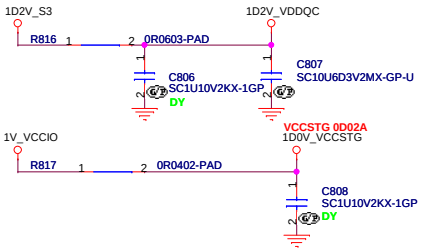
Main Func = CPU

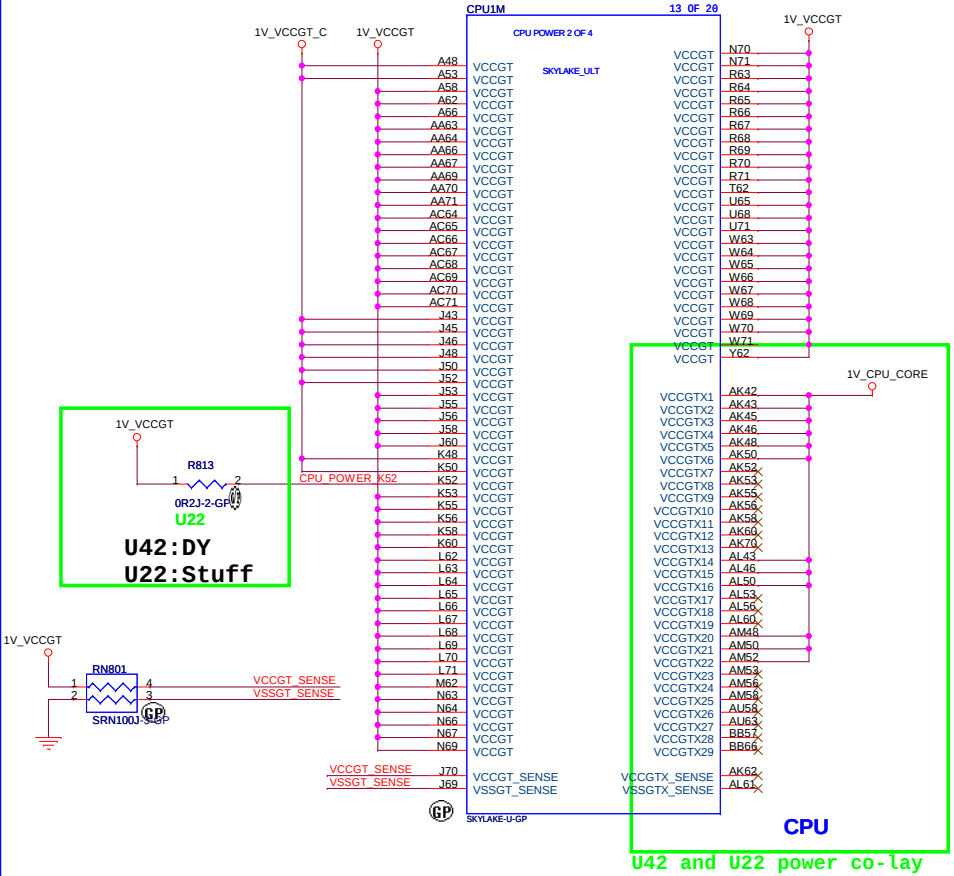
[46] VSSSA_SENSE
[46] VCCSA_SENSE
[46] VCCGT_SENSE
[46] VSSGT_SENSE





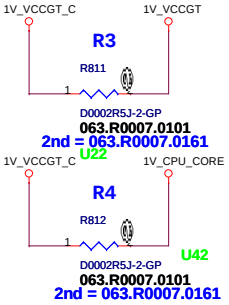


VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 44, "Platform Debug and Test Hooks" for more details. VCCSTG should only ramp up equal to or after VCCST.



KBL U42 Board Compatibility with KBL U22/23e

- 4 Rshunts Required
- R1 – between VCCGTU VR and VCCGTU
- R2 – between VCCGTU and VCCCORE
- R3 – between VCCGT and VCCGT VR
- R4 – between VCCGT and VCCCORE
- Stuff R1 and R3 when U22 or U23e mount on board
- Stuff R2 and R4 and de-pop R1 and R3 when U42 mount on board



R811 R812 Wait change parts

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Blanking

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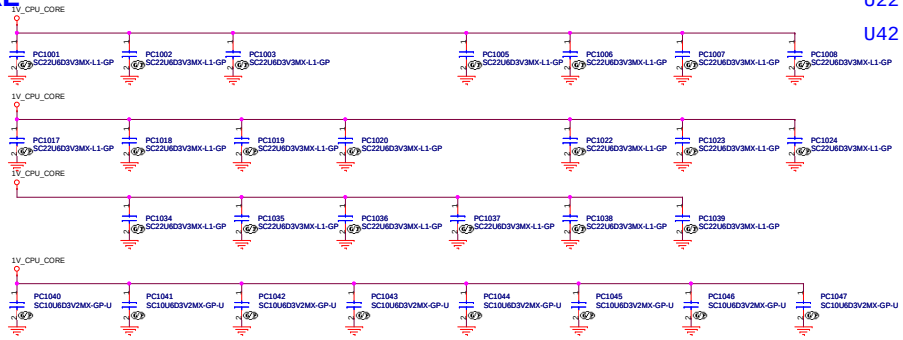
Main Func = CPU

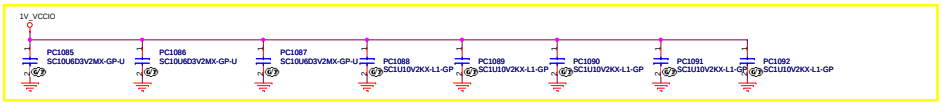
VCORE

1V_CPU_CORE

U22 0603 22uF *23 , 0402 10uF*20

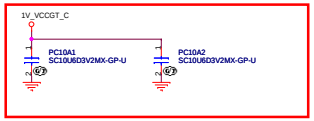
U42 0603 22uF *4 , 0402 10uF*20

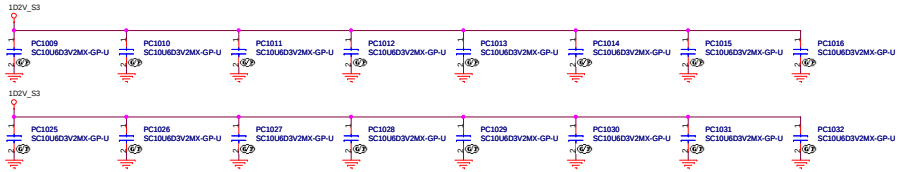


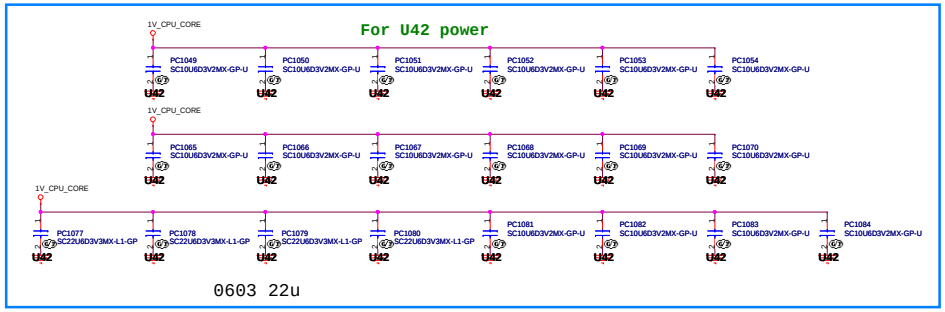


1V_VCCIO

10uF * 3 1uF *4







0603 22u

Power Layout

48.1.3 Kaby Lake U Compatible Design Recommendation

48.1.3.1 KBL-R U 4+2 / KBL U 2+2 Design Recommendation

Table 48-3. Bulk Decoupling Example (KBL-R U42/KBL U22)

Bulk Decoupling Locations	Example - U 4+2	Example - U 2+2	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mΩ ESR)	1x 220 uF (@4.5mΩ ESR)	Placed at primary side near to VR output
	1x 220 uF (@4.5mΩ ESR)		Placed at backside side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220 uF (@4.5mΩ ESR)		Placed at primary side near to VR output
V_{DDQ} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{IO} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{SA} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{PLL} Power Plane at V1P0A VR output	1x 0.1uF 0402		Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

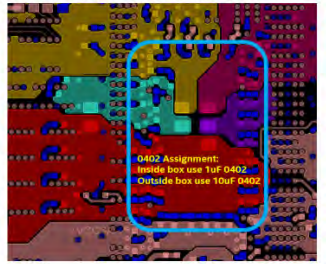
Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 1 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	31x 1 uF 0402 or 0201		Refer to diagram in Note 4 below for placement recommendation of 0402 caps Refer to diagram in Note 5 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V)[1]	
		8x 10 uF 0402	
Vcc/Vcc_{GT}	5x 1 uF 0402 or 0201		Place as close to the package as possible
Vcc_{GT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V)[1]	

Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc_{SA}	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
Vcc_{IO}		4x 1 uF 0402	Place as close to the package as possible
V_{DDQ}		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
V_{DDQC}		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQC BGA routing should not exceed 48mohm (Rdc). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
Vcc_{PLL}		1 x 1 uF 0402	Place as close to the package as possible.
Vcc_{PLL_OC}		1x 1 uF 0201	Do not route Vcc_{PLL} Vcc_{PLL_OC} Vcc_{ST} closest adjacent layer over any power net other than ground.
Vcc_{ST}		1x 1 uF 0402	For VccST: Refer to Figure 48-2 for additional routing details for VccST & VccSTG.

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ~ 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source
3. Due to the difference between the package designs, KBL U 2+2 design requires more on-board decoupling in order to maintain the same loadline.
4. Diagram of placement for 0402 backside caps for CPU decoupling.



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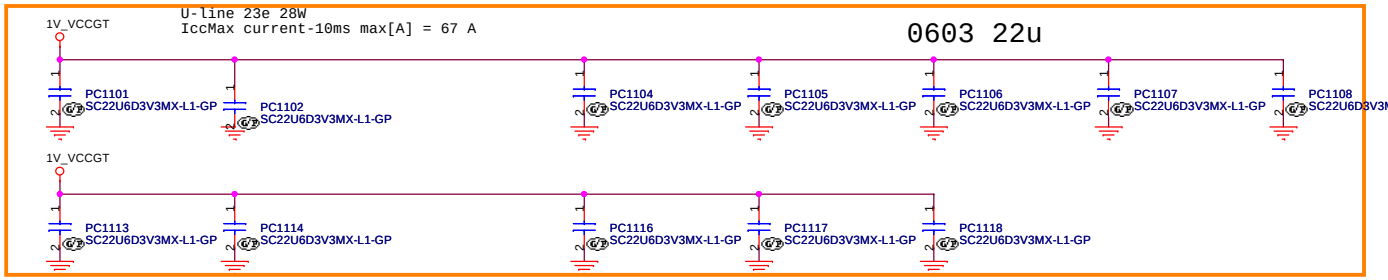
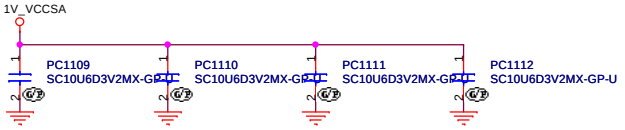
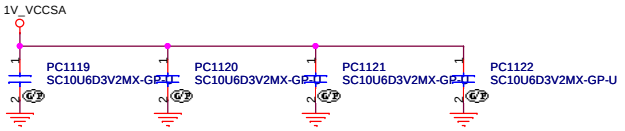
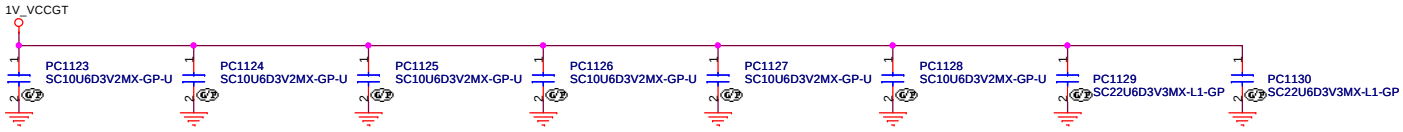
Main Func = CPU

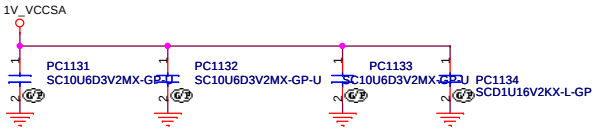
SLICED GT

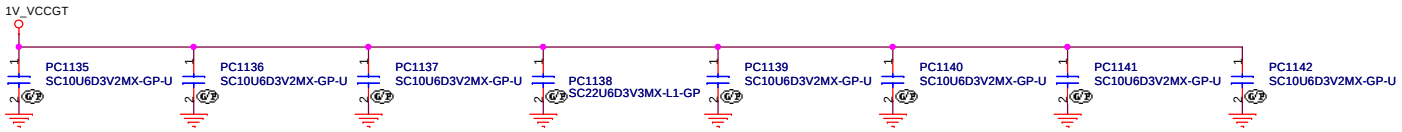


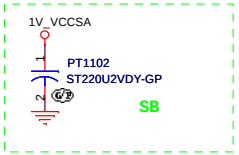


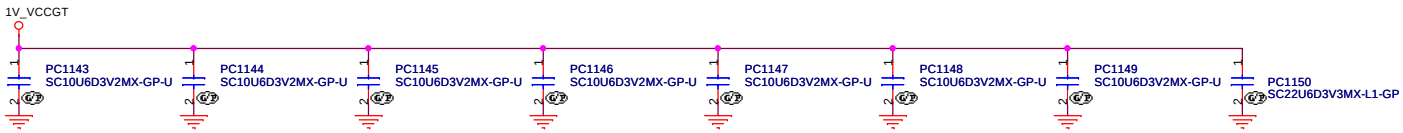


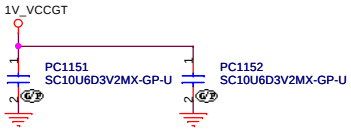




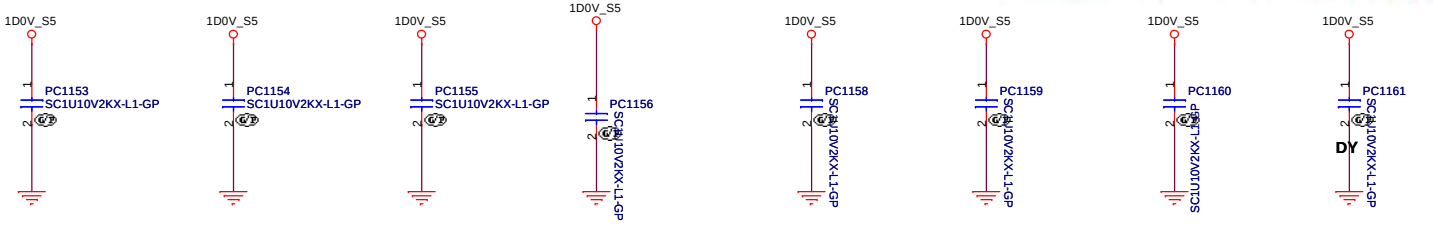


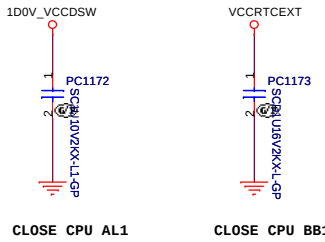


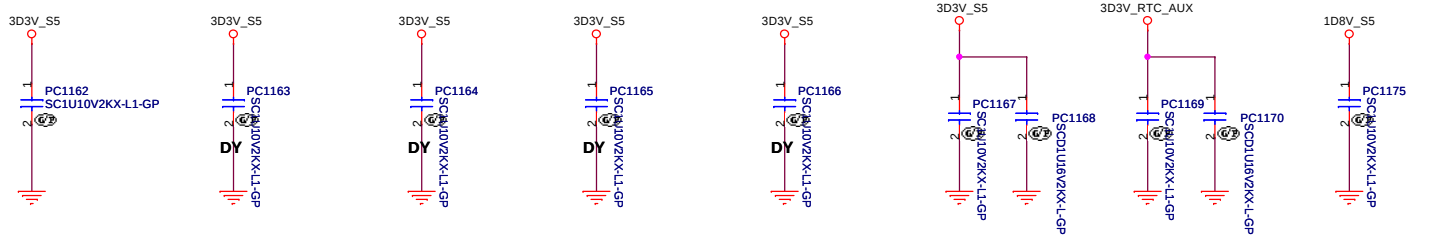




U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
								Or	1x330uF/9mW	36x22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								Or	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF







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SSID = DDR4 CHA

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

please notice that signal BG1 (pin:M9) and UZQ (pin:E9) are required

SDP & DDP SETTING

DDP: 240ohm
SDP: 0ohm

DDP x16 and SDP x16 Compatible Layout

- Alternate two layout, risk of VSS offset increases a little

Figure 3-29. SKL/KBL U DDR4 x16 Memory Down SDP and DDP common board BG1 Signal Topology

Note: When DDP: R3 = 0 ohms/0201/1%, R2 = Unstuffed
Note: When SDP: R3 = Unstuffed , R2 = 0 ohms.
Note: BG1+ BG1 + M should be 25mils shorter than other CMD signals.

Figure 4-3. SKL/KBL U DDR4 Memory Down V_{REF_DQ} and V_{REF_CA} Overview

SKL/KBL U
VREF_DQ_A
VREF_DQ_B
DDR_VREF_CA

DDR4 On Board RAM Power Decouple Cap

VDDQ/VDD 10uF x6

VDDQ/VDD 1uF x20

VPP 1uF x16

VPP 10uF x4

VTT 10uF x3

VTT 1uF x16

4.14.3 KBL-R DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

Table 4-27. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1µF (0402) (All stuffed)	
		Distributed around the DRAM devices	10x 10µF (0603) (All stuffed)	
	VPP	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	5x 10µF (0603)	
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	4x 10µF (0603)	

For ODIMM1,ODIMM2,ODIMM3,ODIMM4

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LPDDR3L_CHA
Buzz_KBL
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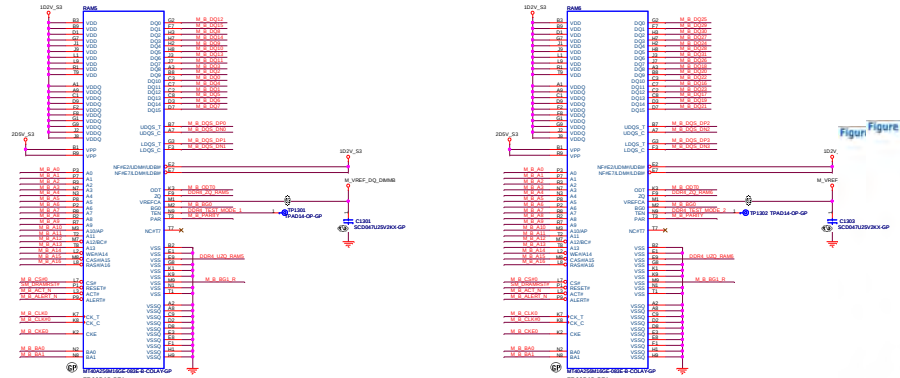
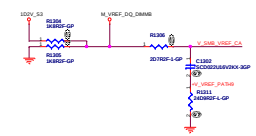
SSID = DDR4 CHB

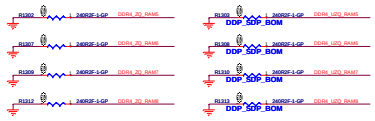
DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

please notice that signal BG1 (pin:M9) and UZQ (pin:E9) are required





SDP & DDP SETTING



DDP: 240ohm
SDP: 0ohm

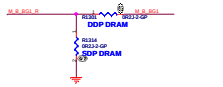


Figure 3-29. SKL/KBL U DDR4 x16 Memory Down SDP and DDP common board BG1 Signal Topology

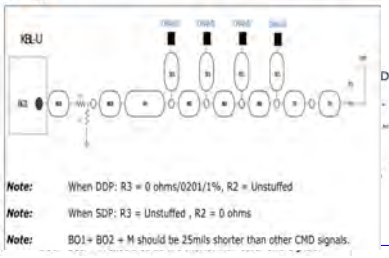
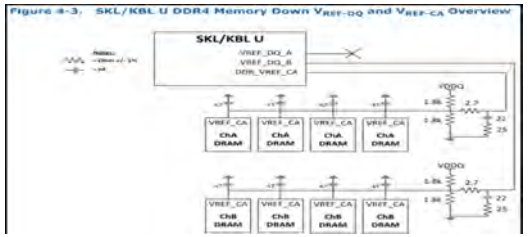
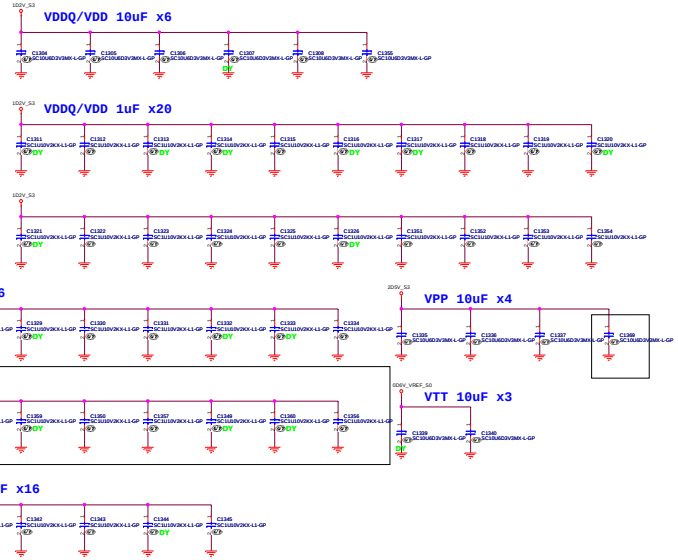
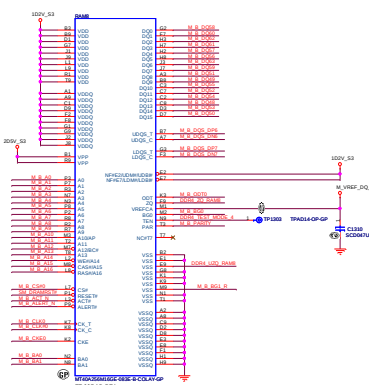


Figure 4-3. SKL/KBL U DDR4 Memory Down V_{REF_DQ} and V_{REF_CA} Overview



DDR4 On Board RAM Power Decouple Cap



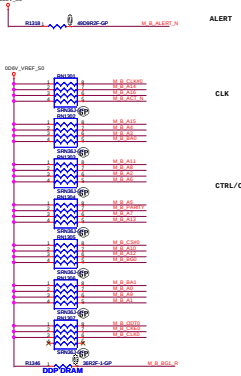


4.14.3 KBL-R DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

Table 4-27. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1µF (0402) (All stuffed)	
		Distributed around the DRAM devices	10x 10µF (0603) (All stuffed)	
	VPP	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	5x 10µF (0603)	
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	4x 10µF (0603)	



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LPDDR3L_CHB

Buzz_KBL

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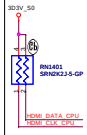
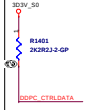
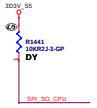
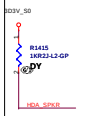
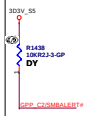
SSID = STRAP

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic							
High	Detected	Detected	Detected	Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confi-dentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic							
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default	NMI or SMI Capable	Note
		Input	Output				
GPP_B22	20K PD (see note)	No	No	GSPI1_MOSI	GPO	None	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts
GPP_B23	20K PD (see note)	Yes	No	SML1ALERT#/ PCHHOT#	GPO	NMI SMI	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
HD Audio Interface					
HDA_RST#	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SYNC	Primary	Internal Pull-down	Driven Low	Internal Pull-down	OFF
HDA_BLK	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SDO	Primary	Internal Pull-down	Driven Low		OFF
HDA_SDI[1:0]	Primary	Internal Pull-down	Internal Pull-down		OFF

I/O Signal Planes and States

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
SPI0_CLK	Primary	Driven Low (See Note 1)	Driven Low	Driven Low	Off
SPI0_MOSI	Primary	Internal Pull up/ Pull-down (See Note 1 &2)	Driven Low	Driven Low	Off
SPI0_MISO	Primary	Internal Pull-up	Internal Pull-up	Internal Pull-up	Off
SPI0_CS0#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_CS1#	Primary	Internal Pull-up (See Note 1)	Driven High	Driven High	Off
SPI0_CS2#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_IO[2:3]	Primary	Internal Pull-up (See Note 1)	Internal Pull-up	Internal Pull-up	Off
SPI1_CLK	Primary	Undriven	Undriven	Undriven	Off
SPI1_MOSI	Primary	Undriven	Undriven	Undriven	Off
SPI1_MISO	Primary	Undriven	Undriven	Undriven	Off
SPI1_CS#	Primary	Undriven	Undriven	Undriven	Off
SPI_IO[2:3]	Primary	Undriven	Undriven	Undriven	Off

Notes:
1. Pins are tri-stated (with weak internal pull-up) prior to RSMRST# de-assertion.
2. Weak internal pull-up resistor is enabled when RSMRST# is asserted and is switched to a weak internal pull-down when RSMRST# is de-asserted.

DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h:Bit 5). 3. This signal is in the primary well.
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. Bit 10: 0 = SPI; 1 = LPC *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
Signal	Usage	When Sampled	Comment
DDPD_CTRLDATA / GPP_E23	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. 1 = Port D is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot block. PCH will invert A16 (default) for cycles going to the upper two 64KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC). *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit14). 4. This signal is in the primary well.
SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** Is selected for EC. 1 = **eSPI** Is selected for EC. *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

DIS

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File: (Reserved)_SODIMM _SODIMM4

Size	Document Number	Rev
Custom	Buzz_KBL	2

Date: Friday, July 07, 2017 Sheet 14 of 106

Main Func = PCH

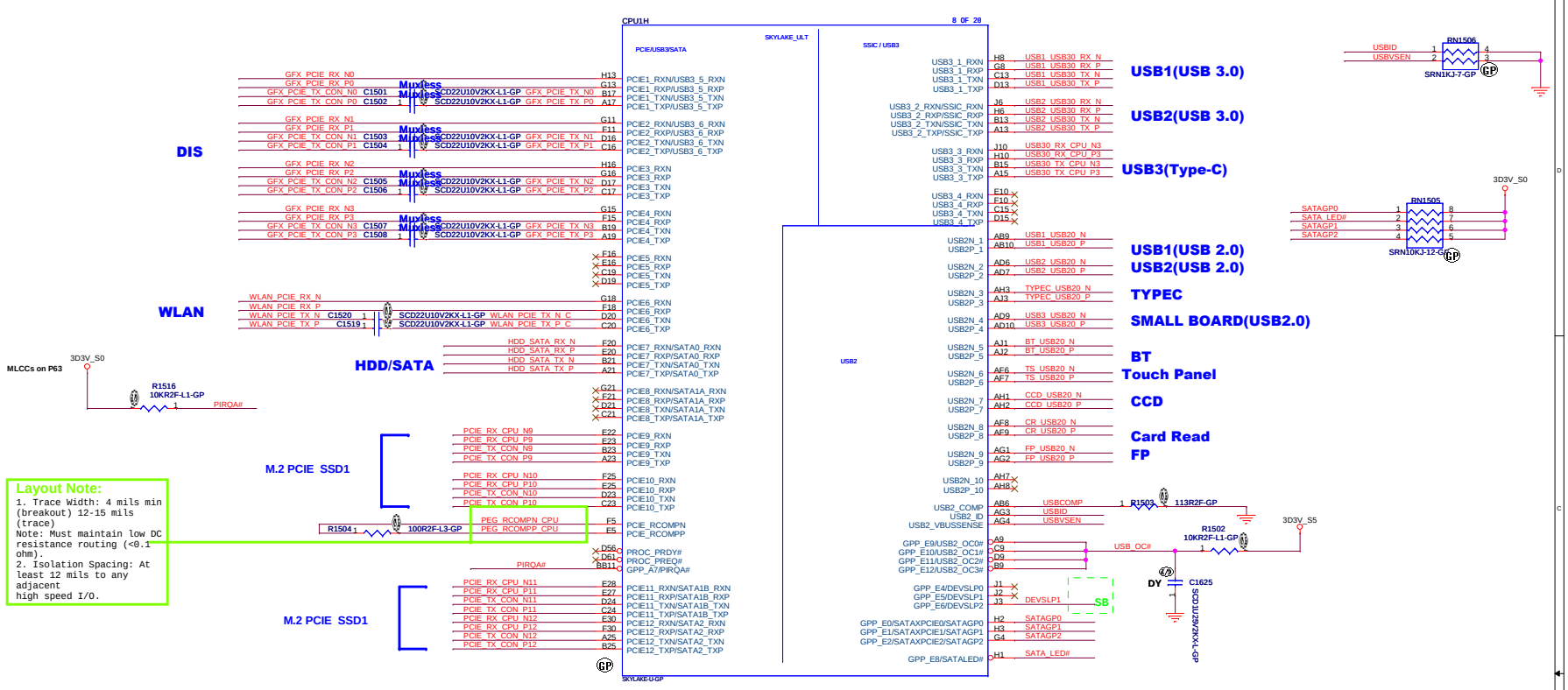


Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

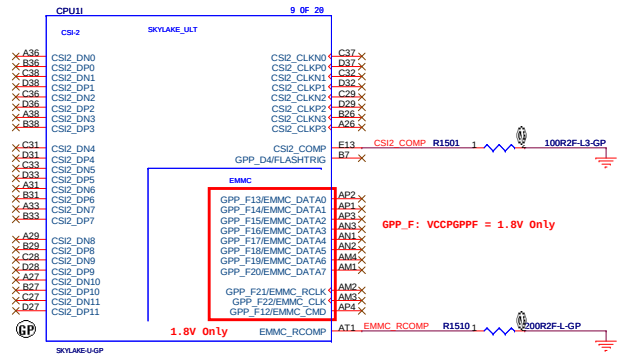
Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

M.2 auto detection

	Acer 2015	2017 R15(Premium)	2017 R15(base)
Lane1	USB3 Port1	USB 3 (I/O)	USB 3 (I/O)	USB 3 (I/O)
Lane2	USB3 Port2	USB 3 (I/O)	USB 3 (I/O)	USB 3 (I/O)
Lane3	USB3 Port3	USB 3 (I/O)	USB 3 Type-C (I/O)	USB 3 Type-C (I/O)
Lane4	USB3 Port4			
Lane5	USB3 Port5 (Premium)	PCIe Port1	dGPU	dGPU	dGPU
Lane6	USB3 Port6 (Premium)	PCIe Port2			
Lane7		PCIe Port3			
Lane8		PCIe Port4			
Lane9		PCIe Port5	LAN		
Lane10		PCIe Port6	WIFI	WIFI	WIFI
Lane11	SATA0 (Base/Premium)	PCIe Port7 (Premium)	HDD	HDD	HDD
Lane12	SATA1 (Base/Premium)	PCIe Port8 (Premium)	ODD		
Lane13		PCIe Port9			
Lane14		PCIe Port10	NA	M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal	M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal	M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal
Lane15	SATA1 (Premium)	PCIe Port11			
Lane16	SATA2 (Premium)	PCIe Port12	M.2 SSD (SATA x1)	M.2 SSD SATA	
	USB2 Port1		USB 3 (I/O)	USB 3 (I/O) (USB20)	USB 3 (I/O) (USB20)
	USB2 Port2		USB 3 (I/O)	USB 3 (I/O) (USB20)	USB 3 (I/O) (USB20)
	USB2 Port3		USB 3 (I/O)	USB 2 Type-C (I/O)	USB 2 Type-C (I/O)
	USB2 Port4		USB 2 (I/O) / SensorHub	USB 2 (I/O)	USB 2 (I/O)
	USB2 Port5		BT	BT	BT
	USB2 Port6		TS	TS	TS
	USB2 Port7		CCD	CCD	CCD
	USB2 Port8		CR (USB) / FP	CR	CR
	USB2 Port9		3G	FP	FP
	USB2 Port10				



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Title	CPU_(PCIE/SATA/USB)
Size: Custom	Document Number: Buzz_KBL
Rev	2
Date: Friday, July 07, 2017	Sheet 15 of 106

Main Func = PCH

WLAN
[76] PEG_CLK_CPU
[76] PEG_CLK_CPU#
[76] PEG_CLKREQ_CPU#

WLAN
[61,89] WLAN_CLK_CPU#
[61,89] WLAN_CLK_CPU
[61,89] WLAN_CLKREQ_CPU#

KBC
[24] RTCRST_ON

NGFF1
[62] SSD1_CLK_CPU_N
[62] SSD1_CLK_CPU
[62] SSD1_CLKREQ_CPU_N

[61] SUS_CLK_CPU

CPU1J
10 OF 20
CLOCK SIGNALS
SKYLAKE_ULT

PEG_CLK_CPU# D42 CLKOUT_PCIE_N0
PEG_CLK_CPU C42 CLKOUT_PCIE_P0
PEG_CLKREQ_CPU# AR10 GPP_B5/SRCCLKREQ0#

B42 CLKOUT_PCIE_N1
A42 CLKOUT_PCIE_P1
LAN_CLKREQ_CPU# AT7 GPP_B6/SRCCLKREQ1#

WLAN
WLAN_CLK_CPU# D41 CLKOUT_PCIE_N2
WLAN_CLK_CPU C41 CLKOUT_PCIE_P2
WLAN_CLKREQ_CPU# AT8 GPP_B7/SRCCLKREQ2#

NGFF1
SSD1_CLK_CPU_N D40 CLKOUT_PCIE_N3
SSD1_CLK_CPU C40 CLKOUT_PCIE_P3
SSD1_CLKREQ_CPU_N AT10 GPP_B8/SRCCLKREQ3#

B40 CLKOUT_PCIE_N4
A40 CLKOUT_PCIE_P4
SRCCLKREQ4# AU8 GPP_B9/SRCCLKREQ4#

E40 CLKOUT_PCIE_N5
E38 CLKOUT_PCIE_P5
SRCCLKREQ5# AU7 GPP_B10/SRCCLKREQ5#

CPU

CLKOUT_ITPXDP_N F43
CLKOUT_ITPXDP_P E43

GPD8/SUSCLK BA17 SUS_CLK_CPU

XTAL24_IN E37 XTL_24M_X1_CPU
XTAL24_OUT E35 XTL_24M_X2_CPU

XCLK_BIASREF E42 XCLK_BIASREF
R1603 2K7R2F-GP
1D0V_S5

RTCX1 AM18 XTL_32K_X1_CPU
RTCX2 AM20 XTL_32K_X2_CPU

SRTCRST# AN18 SRTC_RST#
RTCRST# AM16 RTC_RST#

SKYLAKE-U-GP

3D3V_RTC_AUX
RN1601
SRN20KJ-1-GP

RTC Reset
C1606 SC1U50V3KX-GP
GJ601 GAP-OPEN
C1605 SC1U50V3KX-GP

For AFR
RTCRST_ON
Q1603
G D S
RTC_RST#
RTC_RST#_R
2N7002K-2-GP
84.2N702.J31
2ND = 084.27002.0L31
3rd = 84.2N702.031
R1618 100KR2F-L3-GP
R1621 2K2R2J-L1-GP

XTL_32K_X1_CPU
XTL_32K_X2_CPU
R1615 10MR2J-L-GP
X1602
XTAL-32D768KHZ-88-GP
082.30003.0191
C1603 SC15P50V2JN-2-GP SB
C1604 SC15P50V2JN-2-GP SB

XTL_24M_X1_CPU
C1601 SC15P50V2JN-L-GP
U22
R1602 1MR2F-L-GP
INPUT/OUTPUT#1
NC#2
INPUT/OUTPUT#3
X1601
XTAL-24MHZ-135-GP
082.30006.0041
2nd = 82.30004.A01
U22
XTL_24M_X2_CPU
C1602 SC15P50V2JN-L-GP
U22

close to CPU
3D3V_S0
SSD1_CLKREQ_CPU_N
PEG_CLKREQ_CPU#
WLAN_CLKREQ_CPU#
LAN_CLKREQ_CPU#
RN1608
SRN10KJ-12-GP
SRCCLKREQ4#
SRCCLKREQ5#
RN1609
SRN10KJ-L-GP

DIS

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Title: MCP_CLOCK
Size: Custom
Document Number: Buzz_KBL
Rev: 2
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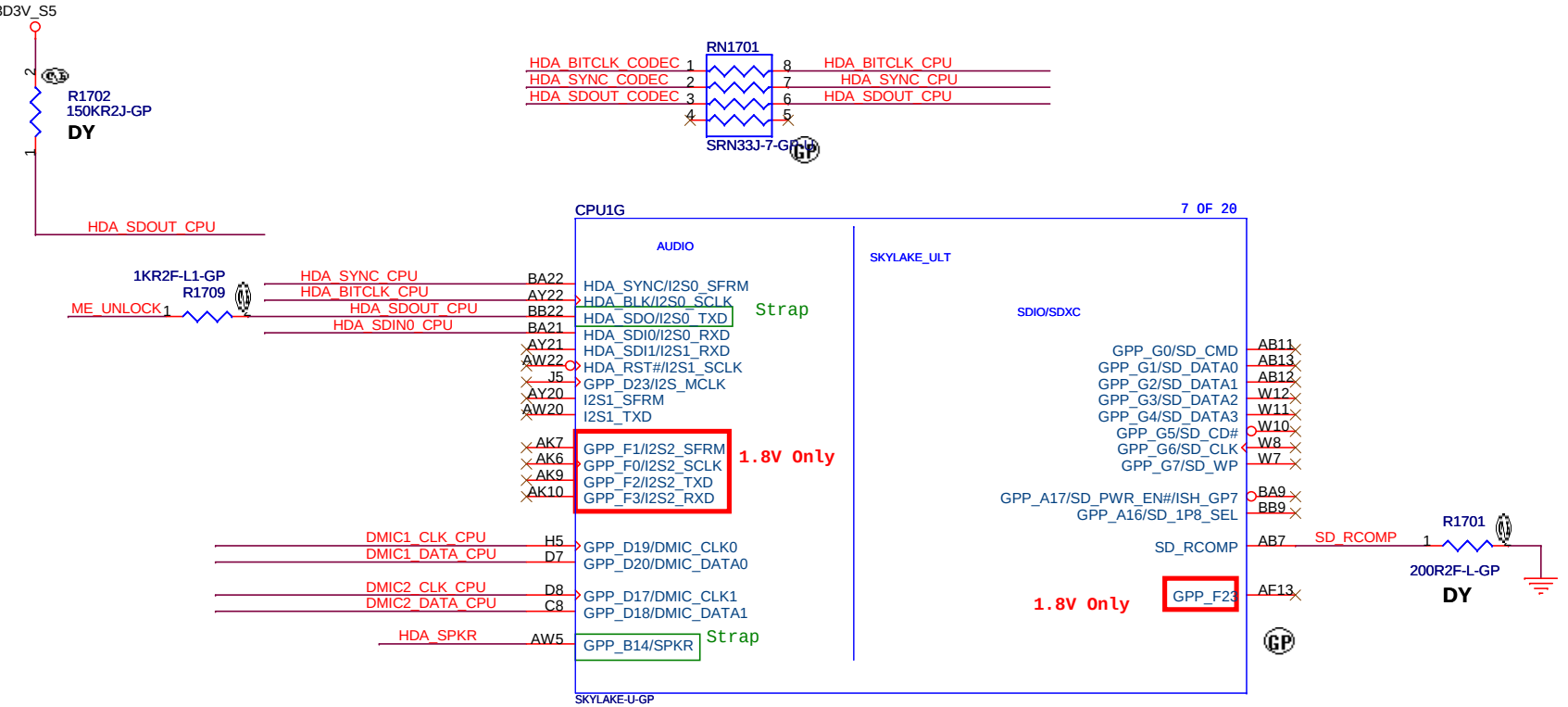
Main Func = PCH

Audio Code

[17,27] HDA_SYNC_CODEC
[17,27] HDA_BITCLK_CODEC
[27] HDA_SDOUT_CODEC
[27] HDA_SDIN0_CPU
[14,27] HDA_SPKR

[24] ME_UNLOCK
[17,27] HDA_SYNC_CODEC
[17,27] HDA_BITCLK_CODEC

[29] DMIC2_DATA_CPU
[29] DMIC2_CLK_CPU
[29] DMIC1_DATA_CPU
[29] DMIC1_CLK_CPU



CPU

18.3 Terminating Unused SDXC Signals

SDXC signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDXC interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

Additionally, if SDXC interface is not used, the SD_RCOMP pin does not need to be connected to a RCOMP resistor.

DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_(AUDIO/SDIO/SDXC)	
Size: Custom	Document Number: Buzz_KBL	Rev: 2
Date: Friday, July 07, 2017	Sheet 17 of 106	

Main Func = PCH

LPC

[24,68,91] LPC_AD_CPU_P0
[24,68,91] LPC_AD_CPU_P1
[24,68,91] LPC_AD_CPU_P2
[24,68,91] LPC_AD_CPU_P3
[24,68,91] LPC_FRAME#_CPU
[18,24] LPC_CLK_KBC
[18,68] LPC_CLK_DBG

SPI

[24,25] SPI_CS_CPU_N0
[24,25] SPI_CLK_ROM
[25] SPI_WP_ROM
[25] SPI_HOLD_ROM
[24,25] SPI_SO_ROM
[24,25] SPI_SI_ROM
[14] SPI_SO_CPU
[14] SPI_SI_CPU

DM1&2 TPAD and XDP

KBC

[24,55,70,73,79] SML1_CLK
[24,55,70,73,79] SML1_DATA
[24] H_RCIN#
[24,68,91] INT_SERIRQ
[24,91] PM_CLKRUN#_EC
[91] LPC_CLK_TPM
[69] SMB_DATA_CPU
[69] SMB_CLK_CPU
[27,29] SML0_DATA_CPU
[27,29] SML0_CLK_CPU
[18,24] LPC_CLK_KBC
[18,68] LPC_CLK_DBG
[14] GPP_C2/SMBALERT#
[14] GPP_C5/SML0ALERT#
[14] GPP_B23/SML1ALERT#
[91] SUS_STAT

SPI_SO_CPU
SPI_SI_CPU
SPI_CLK_ROM R1806 0R0402-PAD-1-GP
SPI_SO_ROM R1807 0R0402-PAD-1-GP
SPI_SI_ROM R1808 0R0402-PAD-1-GP
SPI_WP_ROM R1809 0R0402-PAD-1-GP
SPI_HOLD_ROM R1810 0R0402-PAD-1-GP
SPI_CS_CPU_N0

CPU1E 5 OF 20
SKYLAKE_ULT
SPI - FLASH
SPI0_CLK AV2
SPI0_MISO AW3
SPI0_MOSI AV3
SPI0_IO2 AW2
SPI0_IO3 AU4
SPI0_CS0# AU3
SPI0_CS1# AU2
SPI0_CS2# AU1
Strap
SPI - TOUCH
GPP_D1/SPI1_CLK M2
GPP_D2/SPI1_MISO M3
GPP_D3/SPI1_MOSI J4
GPP_D21/SPI1_IO2 V1
GPP_D22/SPI1_IO3 V2
GPP_D0/SPI1_CS# M1
C LINK
CL_CLK G3
CL_DATA G2
CL_RST# G1
GPP_A0/RCIN# AW13
GPP_A6/SERIRQ AY11
SKYLAKE-U-GP

SMBUS, SMLINK
GPP_C0/SMBCLK R7 SMB_CLK
GPP_C1/SMBDATA R8 SMB_DATA
GPP_C2/SMBALERT# R10 GPP_C2/SMBALERT#
GPP_C3/SML0CLK R9 SML0_CLK
GPP_C4/SML0DATA W2 SML0_DATA
GPP_C5/SML0ALERT# W1 GPP_C5/SML0ALERT#
GPP_C6/SML1CLK W3 SML1_CLK
GPP_C7/SML1DATA V3 SML1_DATA
GPP_B23/SML1ALERT#/PCHHOT# AM7 GPP_B23/SML1ALERT#
Strap

3V3

LPC
GPP_A1/LAD0/ESPI_IO0 AY13 LPC_AD_CPU_P0
GPP_A2/LAD1/ESPI_IO1 BA13 LPC_AD_CPU_P1
GPP_A3/LAD2/ESPI_IO2 BB13 LPC_AD_CPU_P2
GPP_A4/LAD3/ESPI_IO3 AY12 LPC_AD_CPU_P3
GPP_A5/LFRAME#/ESPI_CS# BA12 LPC_FRAME# CPU
GPP_A14/SUS_STAT#/ESPI_RESET# BA11 SUS_STAT
GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 LPC_CLK_CPU_P0
GPP_A10/CLKOUT_LPC1 AY9 LPC_CLK_TPM_R
GPP_A8/CLKRUN# AW11 PM_CLKRUN# EC

HDD_G-sensor
Audio Codec/AMP
KBC /G-SENSOR

TPM
R1830 22R2J-L1-GP LPC_CLK_TPM

R1824 1K2J-L2-GP SPI_HOLD_CPU
DY

3D3V_S0
RN1801 SRN10KJ-L-GP
H_RCIN#
INT_SERIRQ

Processor Interface	RCIN#	Keyboard Controller Reset Processor: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the processor other sources of INIT#. When the processor detects the assertion of this signal, INIT# is generated for 16 PCI clocks.

20.9 Serial Interrupt

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase,** Signal driven low
- **R – Recovery Phase,** Signal driven high
- **T – Turn-around Phase,** Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.

CPU

3D3V_S0
RN1802 SRN10KJ-L-GP
Q1801 2N7002KDW-1-GP
SMB_DATA
SMB_CLK
SMB_DATA_CPU
SMB_CLK_CPU
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.063D1.007C

PM_CLKRUN# EC
R1818 8K2R2F-1-GP
3D3V_S5
RN1810 SRN2K2J-5-GP
SML0_CLK
SML0_DATA

RN1807 SRN2K2J-4-GP
SML1_CLK
SML1_DATA
SMB_CLK
SML1_DATA

SB
RN1803 SRN10KJ-L-GP
AMP
Q1803 2N7002KDW-1-GP
DY
SML0_DATA
SML0_CLK
SML0_DATA_CPU
SML0_CLK_CPU
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.063D1.007C

LPC_CLK_CPU_P0
R1811 22R2J-L1-GP LPC_CLK_KBC
R1804 22R2J-L1-GP LPC_CLK_DBG
0129 TM Larry
LAB
EC1801 SC22P50V2JN-4GP DY
EC1802 SC22P50V2JN-4GP DY

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Title: LPC,SPI,SMBUS,CLINK
Size: Custom
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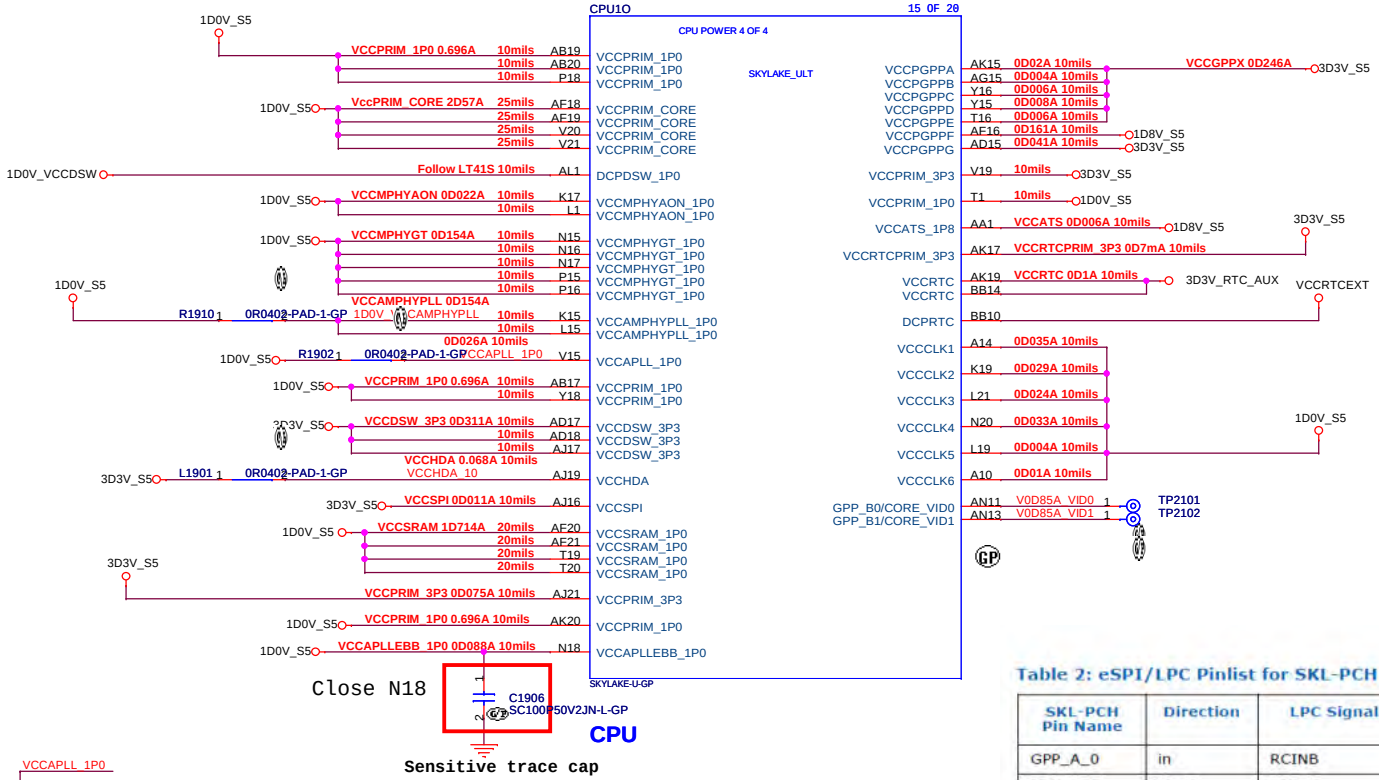

Table 2: eSPI/LPC Pinlist for SKL-PCH

SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_ 0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SM L0ALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

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Title: CPU_POWER3

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Main Func = PCH

[24] SYS_PWROK
[40] PCH_PWROK
[24,61,62] PCIE_WAKE#
[24,40] ALL_SYS_PWRGD
[24,61,62,68,79,89,91] PLT_RST#
[24] RSMRST#_KBC
[45,53,73] 3V_5V_POK
[24,40,45] PM_SLP_S3#
[24,40,51] PM_SLP_S4#
[24] PM_PWRBTN#
[24] AC_PRESENT
[40,60,91] PM_SLP_S0#

CPU1K — 11 OF 20
SYSTEM POWER MANAGEMENT
SKYLAKE_ULT
SKYLAKE-U-GP

PLT_RST# AN10 GPP_B13/PLTRST#
XDP_DBRESET# B5 SYS_RESET#
PM_RSMRST# AY17 RSMRST#
VCCST_PWRGD A68 PROCPWRGD
B65 VCCST_PWRGD
SYS_PWROK B6 SYS_PWROK
PCH_PWROK BA20 PCH_PWROK
PM_RSMRST# BB20 DSW_PWROK
AR13 GPP_A13/SUSWARN#/SUSPWRDNACK
AP11 GPP_A15/SUSACK#
PCIE_WAKE# BB15 WAKE#
GPD2/LAN_WAKE# AM15 GPD2/LAN_WAKE#
AW17 GPD11/LANPHYPC
AT15 GPD7/RSVD#AT15

GPP_B12/SLP_S0# AT11 PM_SLP_S0#
GPD4/SLP_S3# AP15 PM_SLP_S3#
GPD5/SLP_S4# BA16 PM_SLP_S4#
GPD10/SLP_S5# AY16
SLP_SUS# AN15
SLP_LAN# AW16
GPD9/SLP_WLAN# BB17
GPD6/SLP_A# AN16
GPD3/PWRBTN# BA15 PM_PWRBTN#
GPD1/ACPRESENT AY15 AC_PRESENT
GPD0/BATLOW# AU13 BATLOW#
GPP_A11/PME# AU11
INTRUDER# AP16 SM_INTRUDER#
GPP_B11/EXT_PWR_GATE# AM10 EXT_PWR_GATE#
GPP_B2/VRALERT# AM11

BATLOW#:
Pull-up required even if not implemented.

3D3V_S5
RN2005 SRN10KJ-L-GP
BATLOW# 1 4
GPD2/LAN_WAKE# 2 3
RN2006 SRN10KJ-L-GP
PCIE_WAKE# 1 4
AC_PRESENT 2 3
PM_PWRBTN# R2009 10KR2F-L1-GP

CPU

3D3V_S0
R2024 1KR2F-L1-GP
分壓
R2020 10KR2F-L1-GP
R2021 4K7R2J-L-GP
C2001 SC100P50V2JN-L-GP
EC2020 SC22P50V2JN-L-GP DY
PLT_RST#
ALL_SYS_PWRGD
VCCST_PWRGD

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

3D3V_AUX_S5
R2004 100KR2F-3-GP DY
R2005 10KR2F-L1-GP DY
Q2001 2N7002KDW-1-GP
3V_5V_POK_#
PM_RSMRST#
3V_5V_POK_C
R2001 1KR2F-L1-GP DY
R2002 0R0402-PAD-1-GP DY
RSMRST#_KBC
3V_5V_POK
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.063D1.007C
DY

3D3V_S5
U2005 U74LVC1G08GW-R-GP-U
RSMRST#_KBC
3V_5V_POK
C2056 SCD1U25V2KX-L-GP DY
PM_RSMRST#
73.01G08.EHG
2nd = 73.7SZ08.DAH
SB

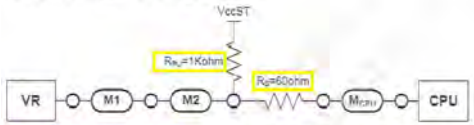
3D3V_S5
EXT_PWR_GATE# R2031 10KR2J-L-GP DY
3D3V_RTC_AUX
SM_INTRUDER# R2019 1MR2F-L-GP
PM_RSMRST# R2010 10KR2F-L1-GP

3D3V_S0
R2014 10KR2F-L1-GP
XDP_DBRESET#

GPP_A13-15 pin(LPC/eSPI):

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default
		Input	Output		
GPP_A13	None	No	Yes	LPC mode: SUSWARN#/ SUSPWRDNACK eSPI mode: None	SUSWANRN#/ SUSPWRDNACK (LPC mode) GPI (eSPI mode)
GPP_A14	None	No	Yes	LPC mode: SUS_STAT# eSPI mode: ESPI_RESET#	SUS_STAT# (LPC mode) ESPI_RESET# (eSPI mode)
GPP_A15	None	No	Yes	LPC mode: SUS_ACK# eSPI mode: None	SUS_ACK# (LPC mode) GPI (eSPI mode)

VCCST_PWRGOOD



- VCCST_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

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Title: CPU_(POWER MANAGEMENT)
Size: Custom | Document Number: Buzz_KBL | Rev: 2
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Main Func = PCH

DIS

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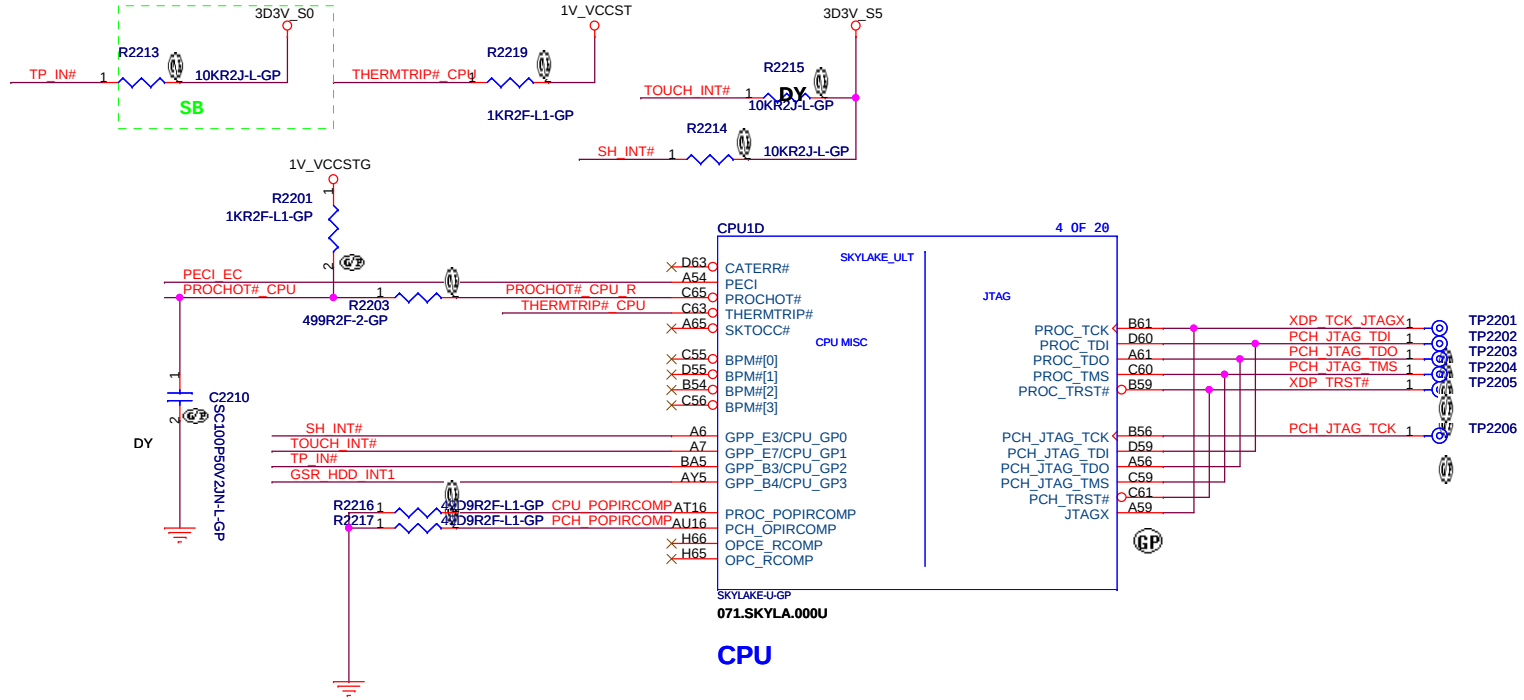
Title	***CPU_(VSS)***	
Size: Custom	Document Number: **Buzz_KBL**	Rev: **2**
Date: Friday, July 07, 2017	Sheet 21 of 106	

Main Func = CPU

[24] PECI_EC
[24,44,46] PROCHOT#_CPU
[24] SH_INT#
[55] TOUCH_INT#
[65] TP_IN#
[69] GSR_HDD_INT1



CPU

PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All processor lines
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O	OD	SE	All processor lines

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Title: CPU_(JTAG/CPU SIDE BAND)

Size: Custom | Document Number: Woody_KBL | Rev: 2

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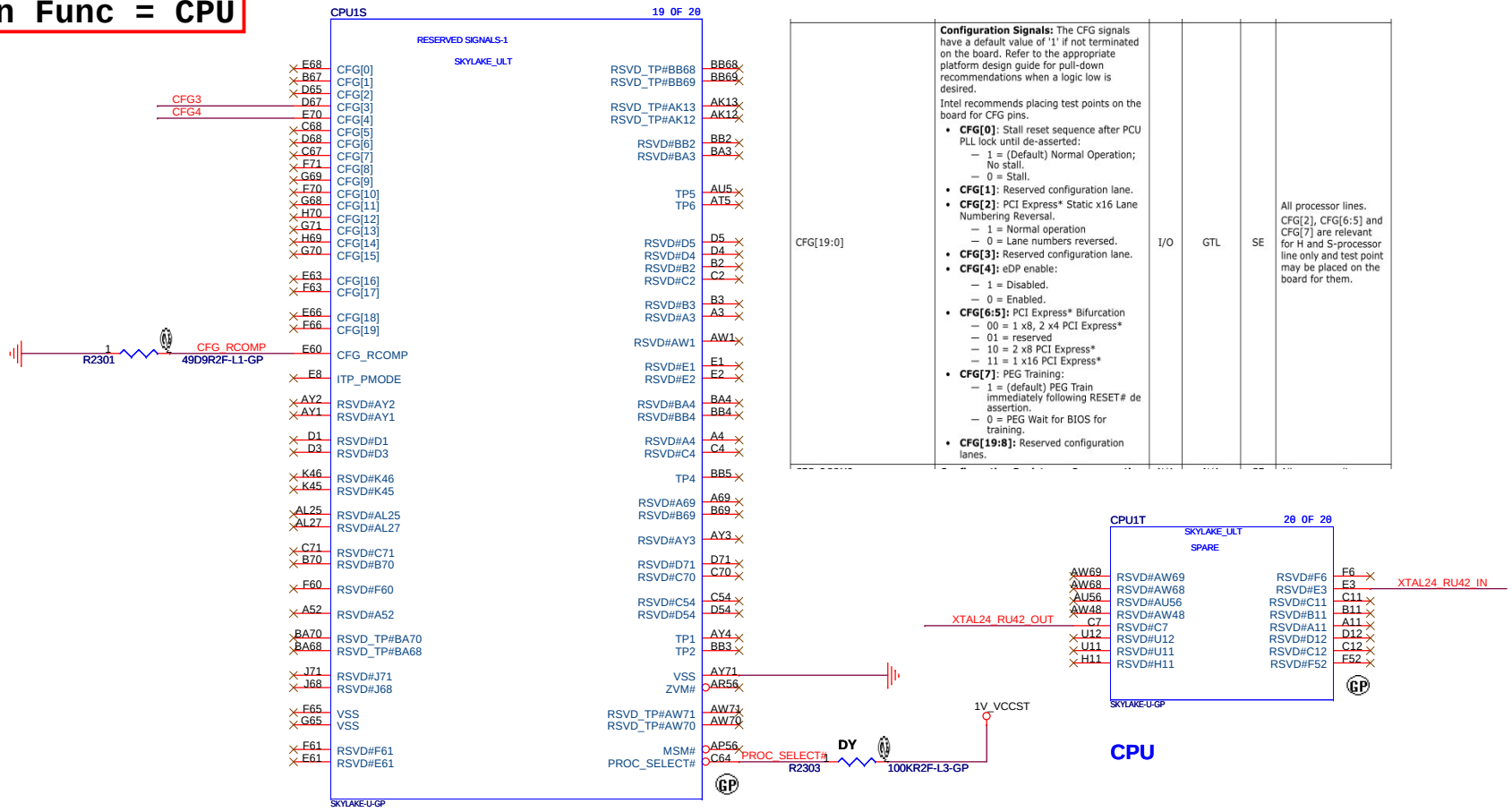
Main Func = CPU



CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

PCH strap pin:

CPU

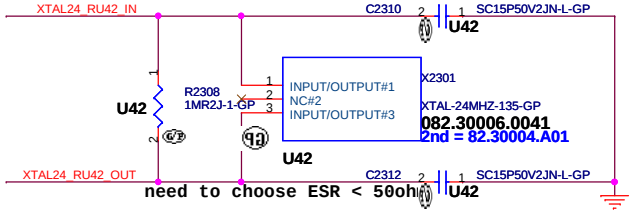
CFG3 — R2305 1KR2J-1-GP — DY

[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

PCH strap pin:

CFG4 — R2304 1KR2J-1-GP

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.



PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for SKL.			N/A	All processor lines

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Title: CPU_RESERVED,CFG

Size: Custom | Document Number: Woody_KBL | Rev: 2

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SSID = KBC

Power

3D3V_AUX_S5
3D3V_S0
3D3V_RTC_AUX

Signal

H_RCIN# [18]
FUN_OFF# [65,89]
LPC_FRAME# CPU [18,68,91]
LPC_AD_CPU_P3 [18,68,91]
LPC_AD_CPU_P2 [18,68,91]
LPC_AD_CPU_P1 [18,68,91]
LPC_AD_CPU_P0 [18,68,91]
LPC_CLK_KBC [18]
PLT_RST# [20,61,62,68,79,89,91]
WLAN_PCIE_WAKE# [24,61]

LID_CLOSE# [64]
PTP_PWR_EN# [65]
PURE_HW_SHUTDOWN# [26,40]
PM_CLKRUN# EC [18,91]
ES1_TXD [61,68]
SH_INT# [22]

EC_TP_IN# [24,65]
KBC_BEEP [27]
KB_BL_DET [65]
FAN1_PWM [26,89]
FAN_TACH1 [26]

Value+ [64]
Value- [64]

KSI0 [65,89]
KSI1 [65,89]
KSI2 [65,89]
KSI3 [65,89]
KSI4 [65,89]
KSI5 [65,89]
KSI6 [65,89]
KSI7 [65,89]
KSO0 [65,89]
KSO1 [65,89]
KSO2 [65,89]
KSO3 [65,89]
KSO4 [65,89]
KSO5 [65,89]
KSO6 [65,89]
KSO7 [65,89]
KSO8 [65,89]
KSO9 [65,89]
KSO10 [65,89]
KSO11 [65,89]
KSO12 [65,89]
KSO13 [65,89]
KSO14 [65,89]
KSO15 [65,89]
KSO16 [65,89]
KSO17 [65,89]

AC_IN# [44,74]
DC_Protect_EC [44]
KBC_PWRBTN# [64,68,89]
BAT_IN# [43,44]

AD_IA [44]
BT_IA [44]
ALL_SYS_PWRGD [20,40]

STDBY_LED [64,89]

SMIL1_CLK [18,55,70,73,79]
SMIL1_DATA [18,55,70,73,79]
BAT_SCL [43,44]
BAT_SDA [43,44]
SPI_WP_ROM [18,25]

EC_TPCLK [65]
EC_TPDATA [65]
ME_UNLOCK [17]
EC_TP_IN# [24,65]

RTCRST_ON [16]
BLON_OUT [55]
AD_OFF [43]
VD_IN1 [26]
VD_OUT1 [26]
PROCHOT# CPU [22,44,46]
CHARGE_LED [64,89]
DC_BATFULL [64,89]
RSMRST# KBC [20]
AMP_MUTE# [27]
5V_EN [45]
KB_BL_PWM [65]
TOUCH_EN [55]
3V_5S_ENABLE [40]

AC_PRESENT [20]
eDP_BLEN_CPU [3]
PM_PWRBTN# [20]
PCIE_WAKE# [20,61,62]

INT_SERIRQ [18,68,91]
EC_SCI# [3,24]

3.3V
PM_SLP_S3# [20,40,45]
PM_SLP_S4# [20,40,51]

LPC BUS=>3.3V
SPI BUS=>3.3V/1.8V (VCC_IO2 PIN:124 OPTION)

PD_INT# [73]

Type_C

USB_CHAR_SEL [36]
USB_CHAR_CTL [36]
USB_CHARGER_EN [36]

Charger

WIFI_RF_EN [61]
BLUETOOTH_EN [61,89]
USB_PWR_EN# [35,64]
WLAN_PCIE_WAKE# [24,61]
CHG_ON# [44]
PECI_EC [22]
WLAN_PERST# [61]
WLAN_PWR_EN# [61]
LID_CLOSE# [64]

TS_I2C0_SCL_CON [6,55]
TS_I2C0_SDA_CON [6,55]
SYS_PWROK [20]
POWER_LED [64,89]
SPI_SO_ROM [18,25]
SPI_SI_ROM [18,25]
SPI_CLK_ROM [18,25]
SPI_CS_CPU_N0 [18,25]

DGPUHOT [79]
DGPU_PWROK [76,85,86,88]
FAN2_PWM [26,89]
FAN_TACH2 [26]
EC_SMI# [3]
EC_SCI# [3,24]
DC_IN_OK [44,73,74]

Close to the EC

PLT_RST#
R2460 47KR2J-L2-GP

For EC power consumption reserver

3D3V_AUX_KBC — R2406 0R0603-PAD-1-GP-U — 3D3V_AUX_S5

VCC_LPC(Pin9)

3D3V_AUX_KBC — R2435 0R0402-PAD-1-GP — VCC_LPC

U2401 KB9028Q-C-GP

LPC_CLK_KBC
LPC_FRAME# CPU
LPC_AD_CPU_P0
LPC_AD_CPU_P1
LPC_AD_CPU_P2
LPC_AD_CPU_P3
INT_SERIRQ
LID_CLOSE# 2
PLT_RST#
ECSCI# KBC
PM_CLKRUN# EC
ECRST#

KBC_BEEP
KB_BL_PWM
DC_BATFULL

FAN1_PWM
FAN2_PWM
FAN_TACH1
FAN_TACH2

KSO0
KSO1
KSO2
KSO3
KSO4
KSO5
KSO6
KSO7
KSO8
KSO9
KSO10
KSO11
KSO12
KSO13
KSO14
KSO15
KSO16
KSO17
KSI0
KSI1
KSI2
KSI3
KSI4
KSI5
KSI6
KSI7

SMIL1_DATA
SMIL1_CLK
BAT_SDA
BAT_SCL

Type C CPU/G-sensor --->
BATTER /CHARGER --->

TS_I2C0_SCL_CON
TS_I2C0_SDA_CON
DGPU_PWROK
DC_IN_OK
EC_TPCLK
EC_TPDATA

CPU--->
Touch Pad

5V_EN
CHG_ON#

LID_CLOSE#
WLAN_PERST#

STDBY_LED

ES1_TXD
SH_INT#
ME_UNLOCK
CHARGE_LED
WIFI_RF_EN

GPIO00
GPIO0C
GPIO0A
GPIO0D
GPIO19
GPIO16
GPIO17
GPIO52
GPIO54
GPIO56

PSCLK1
PSDAT1
PSCLK2
PSDAT2
PSCLK3
PSDAT3
SDA0
SCL0
SDA1
SCL1

3.3V
1.8V

VCC_LPC
AVCC
VCC_IO2
AGND
GND

DA0 DA1 DA2 DA3
AMP_MUTE#
DGPUHOT
PM_SLP_S4#
WLAN_PCIE_WAKE#

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
AD_IA
PCB_VER_AD
ADT_TYPE_AD
EC_TP_IN#
Value+
MODEL_ID_AD
BT_IA
USB_CHARGER_EN

GPXIOA00 GPXIOA01 GPXIOA02 GPXIOA03 GPXIOA04 GPXIOA05 GPXIOA06 GPXIOA07 GPXIOA08 GPXIOA09 GPXIOA10 GPXIOA11
KB_BL_DET
BLON_OUT
AD_OFF
3V_5S_ENABLE
FUN_OFF#
TOUCH_EN
RSMRST# KBC
VD_OUT1
USB_PWR_EN#
SYS_PWROK
RTCRST_ON
PD_INT#

GPXIOD00 GPXIOD01 GPXIOD02 GPXIOD03 GPXIOD04 GPXIOD05 GPXIOD06
VD_IN1
AC_IN#
USB_CHAR_SEL
KBC_PWRBTN# R
ALL_SYS_PWRGD
USB_CHAR_CT1
DC_Protect_EC
PECI_EC
H_PECI_KBC — R2446 43R3F-2-GP

GPIO1A GPIO53 GPIO55
WLAN_PWR_EN#
BAT_IN#
POWER_LED

GPIO5D GPIO5E
eDP_BLEN_CPU
PM_PWRBTN#

GPIO59 GPIO57 GPIO50 GPIO18 GPIO08 GPIO04
PCIE_WAKE# — R2445 0R2J-L-GP
PCIE_WAKE#
AC_PRESENT
Value-
PTP_PWR_EN#
PROCHOT_EC
BLUETOOTH_EN
PM_SLP_S3#

SPI_CS_KBC_N0 — R2412 0R0402-PAD-1-GP — SPI_CS_CPU_N0
SPI_SI_KBC — R2407 0R0402-PAD-1-GP — SPI_SI_ROM
SPI_SO_KBC — R2418 0R0402-PAD-1-GP — SPI_SO_ROM
SPI_CLK_KBC — R2411 0R0402-PAD-1-GP — SPI_CLK_ROM

071.09028.000G

IOAC

SYS_PWROK(S0_PWR_GOOD) ==DELAY 99ms

TOUCH_EN — R2401 10KR2J-L-GP — 3D3V_S0

RN2412 SRN10KJ-L — 5V_EN / 3V_5S_ENABLE
RN2410 SRN10KJ-L — FAN_TACH1 / FAN_TACH2
RN2415 SRN10KJ-L — FUN_OFF# / KB_BL_PWM

EC_SMI# — R2466 0R2J-L-GP
EC_SCI# — R2465 0R0402-PAD-1-GP — ECSCI# KBC

KBC_PWRBTN# — R2441 330KR2J-L-GP — R2444 470KF-GP — KBC_PWRBTN# R — G2402 GAP-OPEN

PURE_HW_SHUTDOWN# — RN2407 SRN10KJ-L — ECRST# Q — Q2403 PMBS3906-GP — ECRST#

84.03906.F11
2nd = 84.T3906.E11

C2428 SC11U10V2KX-L1-GP

LID_CLOSE# 1 — LID_CLOSE# 2 — RN8603 SRN10KJ-L

ECRST# — R2451 10KR2J-3-GP — USB_PWR_EN#

BAT_IN# — RN2413 SRN100KJ-6-GP — CHG_ON#

L2401 BLM15AG121SN-1GP
68.00084.921
2nd = 68.00217.401

AD_OFF — R2453 1KR2F-L1-GP

close RN2407

PURE_HW_SHUTDOWN# — ED2401 DY

GPIO0 High Active

PROCHOT_EC — R2404 100KR2F-L3-GP — C2430 SC100P50V2KX-1GP — Q2404 2N7002K-2-GP — PROCHOT# CPU

84.2N702.J31
2ND = 084.27002.0L31
3rd = 84.2N702.031

Model_ID — R2434 47KR2J-L2-GP — MODEL_ID_AD
Model_ID — R2455 100KR2J-4-GP — EC_AGND

PCB_VER_AD — R2428 47KR2J-L2-GP — R2427 100KR2F-L3-GP — EC_AGND

ADT_TYPE_AD — R2425 10KR2F-L1-GP — R2430 90W — EC_AGND

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	ADC Firmware Setting
65W	N/A	100.0 K	0.300 V		>=3.000 V
90W	100.0 K	N/A	0.600 V		<0.150 V
33W	13.0 K	100.0 K	0.330 V	0.395 V	>=0.150 V, <0.425 V
45W	20.0 K	100.0 K	0.450 V	0.550 V	>=0.425 V, <0.694 V
120W	33.0 K	100.0 K	0.818 V	0.831 V	>=0.694 V, <0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>=0.937 V, <1.177 V
150W	64.9 K	100.0 K	1.286 V	1.315 V	>=1.177 V, <1.395 V
Reserved	78.9 K	100.0 K	1.433 V	1.480 V	>=1.395 V, <1.542 V
Reserved	100.0 K	100.0 K	1.667 V	1.667 V	>=1.542 V, <1.842 V

MODEL_ID_AD	EVA Low register	EVA High Register	Typical Voltage
Buzz_CRL			
Buzz_KBL	OK		
Reserved	N/A	47.0K	2.200 V
Reserved	N/A	64.9K	2.500 V
Reserved	N/A	78.9K	1.800 V
Reserved	N/A	100.0K	1.650 V

Buzz_DIS without subwoofer
Buzz_DIS with subwoofer

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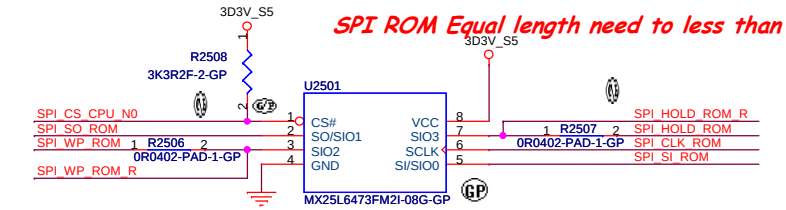
Title: KBC_KB9028
Size: Custom | Document Number: Buzz_KBL | Rev: 2
Date: Friday, July 07, 2017 | Sheet 24 of 106

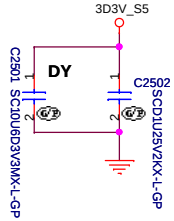
[18,24] SPI_CS_CPU_N0
[18,24] SPI_SO_ROM
[18] SPI_WP_ROM
[14] SPI_WP_ROM_R
[14] SPI_HOLD_ROM_R
[18] SPI_HOLD_ROM
[18,24] SPI_CLK_ROM
[18,24] SPI_SI_ROM
[6] RTC_DET#

Main Func = SPI Flash

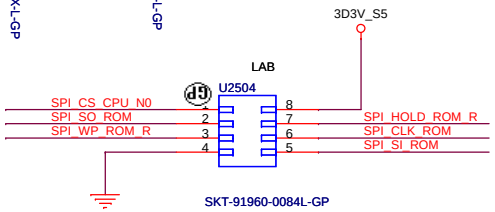
SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

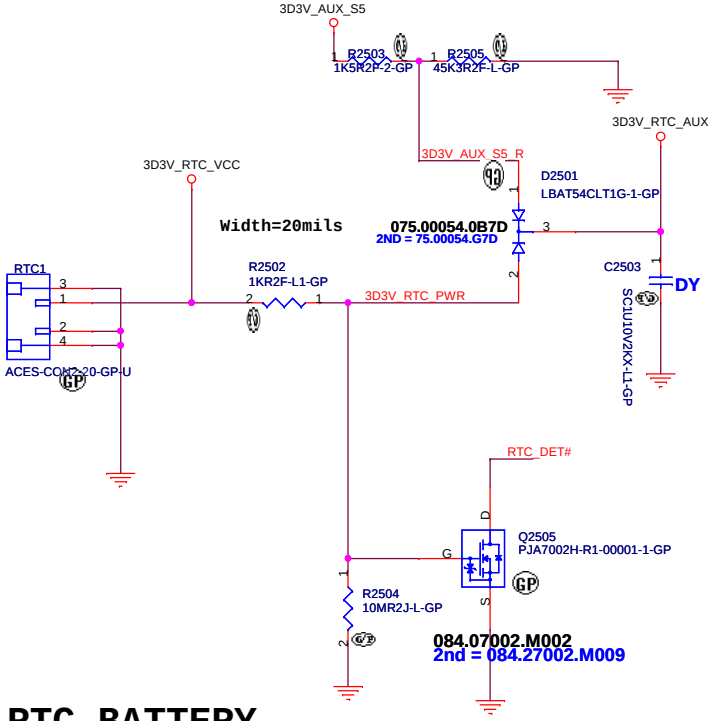




072.25647.000D_MX25L6473FM2I-08G_MXIC
72.25Q64.K01_W25Q64FVSSIQ_WINBOND(EOL)
072.25Q64.0H01_W25Q64JVSSIQ



Main Func = RTC



RTC BATTERY
1st= TBD
2nd= TBD

DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***Flash(KBC+PCH)/RTC***	
Size: Custom	Document Number: **Buzz_KBL**	Rev: **2**
Date: Friday, July 07, 2017	Sheet 25 of 106	

[24] VD_IN1

[24,89] FAN1_PWM

[24,89] FAN2_PWM

[24] FAN_TACH1

[24] FAN_TACH2

[24,40] PURE_HW_SHUTDOWN#

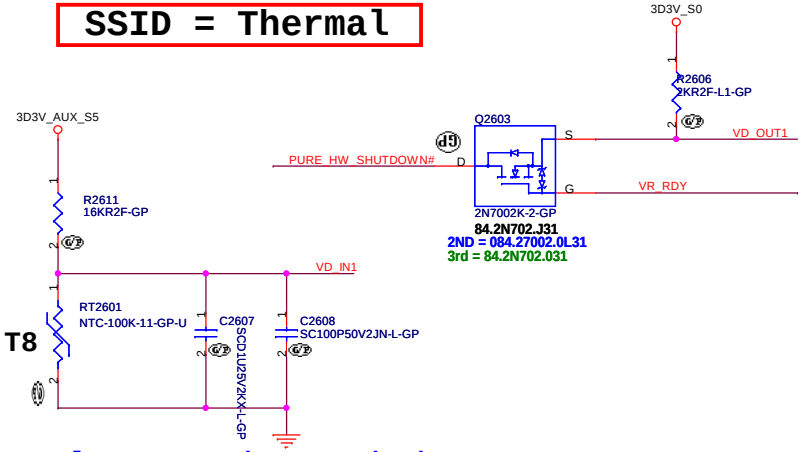
[24] VD_OUT1

[40,46] VR_RDY

[89] FAN_TACH1_C

[89] FAN_TACH2_C

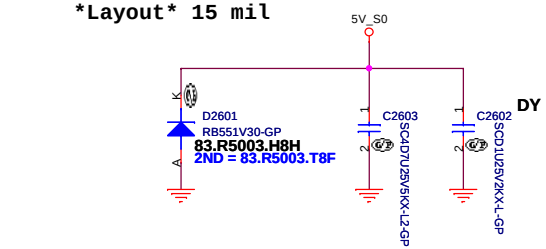
SSID = Thermal

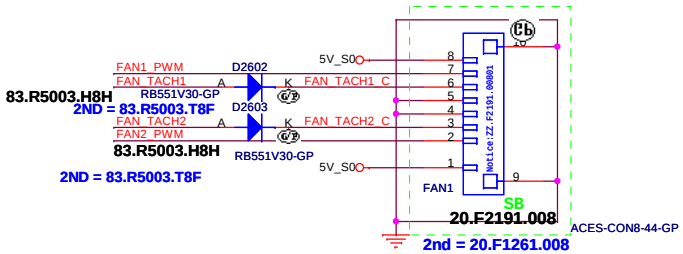


RT2601 close CPU and Vcore chock

VD_IN1 trace 10 mli

***Layout* 15 mil**





DIS

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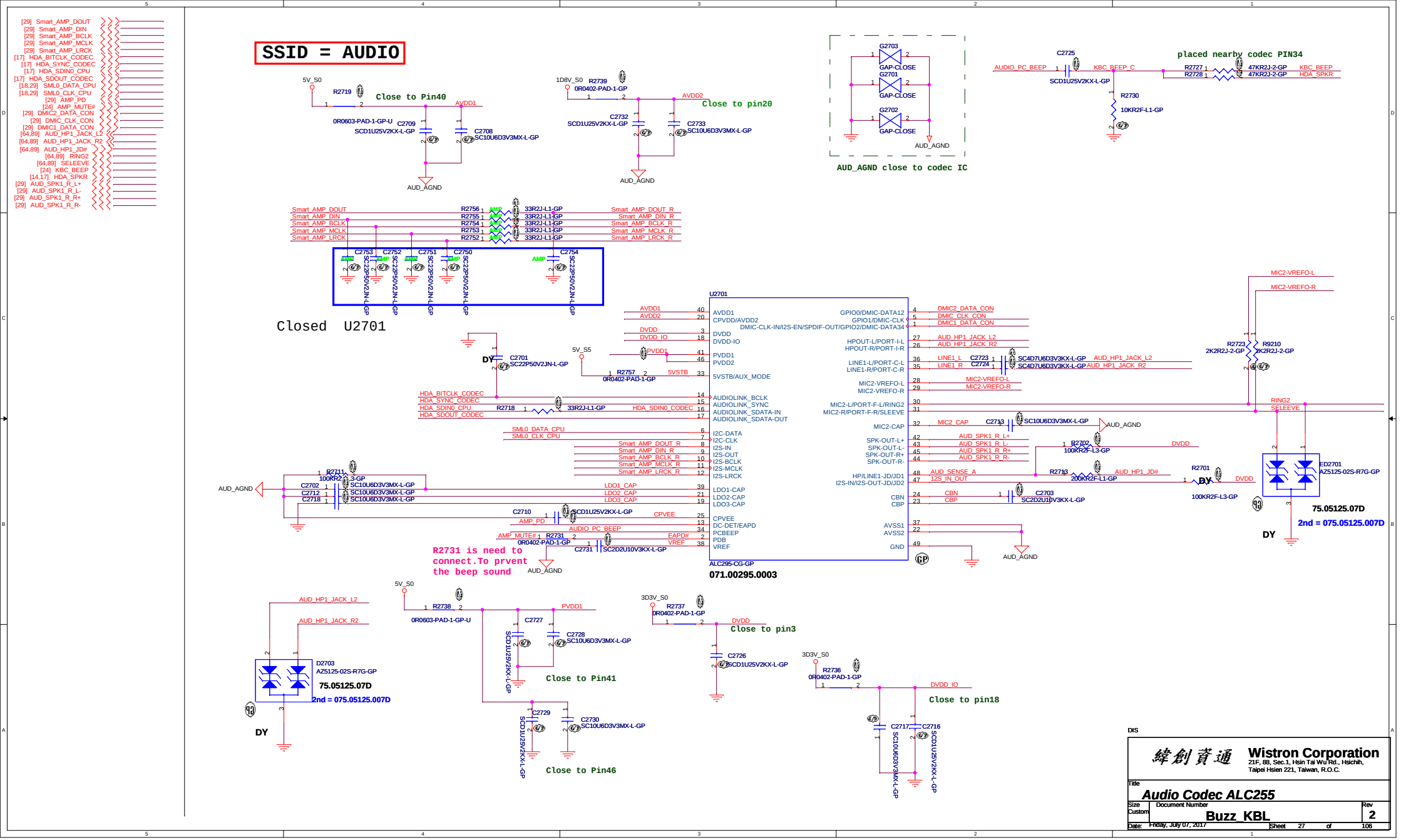
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal 7718/Fan Controllor P2793*

Size	Document Number	Rev
Custom	Buzz_KBL	2

Date: Friday, July 07, 2017 Sheet 26 of 106


SSID = AUDIO
Close to Pin40
Close to pin20
AUD_AGND close to codec IC
placed nearby codec PIN34
Closed U2701
U2701
ALC295-CG-GP
071.00295.0003
R2731 is need to connect.To prvent the beep sound
Close to Pin41
Close to pin3
Close to pin18
Close to Pin46
75.05125.07D
2nd = 075.05125.007D
Wistron Corporation
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Audio Codec ALC255
Buzz_KBL
Rev 2
Friday, July 07, 2017
Sheet 27 of 106

Blanking

DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A4	Buzz_KBL	2

Date: Friday, July 07, 2017 Sheet 28 of 106

SSID = AUDIO

Speaker

[18,27] SML0_CLK_CPU
[18,27] SML0_DATA_CPU
[27] Smart_AMP_MCLK
[27] Smart_AMP_BCLK
[27] Smart_AMP_LRCK
[27] Smart_AMP_DIN
[27] Smart_AMP_DOUT
[27] AMP_PD
[27] AUD_SPK1_R_L-
[27] AUD_SPK1_R_L+
[27] AUD_SPK1_R_R-
[27] AUD_SPK1_R_R+

[89] AUD_SPK1_L-_CON
[89] AUD_SPK1_L+_CON
[89] AUD_SPK1_R-_CON
[89] AUD_SPK1_R+_CON

[89] OUT_RN_CON
[89] OUT_RP_CON

[17] DMIC2_CLK_CPU
[17] DMIC2_DATA_CPU
[17] DMIC1_CLK_CPU
[17] DMIC1_DATA_CPU

[89] CCD_USB20_CON_P
[89] CCD_USB20_CON_N

[89] DMIC_CLK_CON_C
[89] DMIC1_DATA_CON_C
[89] DMIC2_DATA_CON_C

[27] DMIC_CLK_CON
[27] DMIC1_DATA_CON
[27] DMIC2_DATA_CON

[15] CCD_USB20_P
[15] CCD_USB20_N

SML0_CLK_CPU
SML0_DATA_CPU
Smart_AMP_MCLK
Smart_AMP_BCLK
Smart_AMP_LRCK
Smart_AMP_DIN
Smart_AMP_DOUT
R2917 0R0402-PAD-1-GP
R2918 0R0402-PAD-1-GP
R2916 0R0402-PAD-1-GP
R2915 0R0402-PAD-1-GP
R2914 0R0402-PAD-1-GP
R2913 0R0402-PAD-1-GP
R2940 0R0402-PAD-1-GP
AMP_SCL
AMP_SDA
AMP_MCLK
AMP_BCLK
AMP_LRCK
AMP_DACDAT
3P3A_DVDD_IO
R2960 10KR2F-L3-GP
AMP_PD
AMP_DOUT
U2905
SPDIF_IN
DACDAT
LRCK
BCLK
MCLK
SCL
SDA
BYPASS/I2
NCI#1
SPDIF_OUT/I2S_DATOUT
PDB_JD
DVDD_IO
DVDD
ASEL
DGND
AGND
AVDD2
LDO_A1D5
VREF
AGND
LISENSE+
LISENSE-/LVSENSE+
LVSENSE-
GND
NC#48
PGND_R
OUT_RN
OUT_RP
PVDD_R
AVDD1
AVDD1
PVDD_L
OUT_LP
OUT_LN
PGND_L
NC#37
NC#36
NC#35
ALC1006-VB-CGT-GP
074.01006.0A13
AMP_VDD1V8
C2924 SC10U6D3V3MX-L-GP
C2923 SC1U50V3KX-GP
C2922 SC1U10V2KX-L1-GP
DY
R2934 10KR2F-L1-GP
R2933 10KR2F-L1-GP
I2C Address Select ion Low:0x24 Hi :0x26
AUDIO_AMP_ASEL
AMP_AVDD2_1V8
C2921 SC10U6D3V3MX-L-GP
C2920 SC1U10V2KX-L1-GP
C2919 SC1U10V2KX-L1-GP
C2918 SC1U10V2KX-L1-GP
C2917 SC1U10V2KX-L1-GP
LDO_A1_5_R
AMP_VREF
C2911 SC2D2U10V3KX-L-GP
BYPASS
AMP_DOUT
C2912 SC2D2U10V3KX-L-GP
C2913 SC2D2U10V3KX-L-GP
C2914 SC2D2U10V3KX-L-GP
C2915 SC2D2U10V3KX-L-GP
SPK_VDD5V
OUT_RN
OUT_RP
R2928 0R0402-PAD-1-GP
R2927 0R0402-PAD-1-GP
R2926 0R0402-PAD-1-GP
SPK_RIP
SPK_RINRVP
SPK_RVN
SPK_RP_R
SPK_RINRVP_R
SPK_RN_R
RISENSE+
RISENSE-/RVSENSE+
RVSENSE-
NC#27
BYPASS#28
NC#29
GND
NC#31
NC#32
NC#33
NC#34
BYPASS_2
C2916 SC2D2U10V3KX-L-GP
AMP_BTL
R2925 0R0402-PAD-1-GP
Output Mode Selection
Low:BTL
Hi:PBTL

ER2914 0R0603-PAD
ER2915 0R0603-PAD
ER2916 0R0603-PAD
ER2917 0R0603-PAD
ER2918 0R0603-PAD
ER2919 0R0603-PAD
AUD_SPK1_R_L-
AUD_SPK1_R_L+
AUD_SPK1_R_R-
AUD_SPK1_R_R+
OUT_RN
OUT_RP
R2939 D1R5F-L-GP
OUT_RN_R
EC2965 SC2D2U10V3KX-L-GP
EC2966 SC2D2U10V3KX-L-GP
EC2967 SC2D2U10V3KX-L-GP
EC2968 SC2D2U10V3KX-L-GP
EC2969 SC2D2U10V3KX-L-GP
EC2970 SC2D2U10V3KX-L-GP
SC1K50V2KX-L-GP
R2941 0R0402-PAD
R2923 0R0402-PAD
R2942 0R0402-PAD
SPK_RIP
SPK_RINRVP
SPK_RVN
Trace width=40mil
SPK1
HR-CON6-5-GP
SB
020.F0976.0006
PIN5: SUBWOOFER -
PIN6: SUBWOOFER +
AUD_SPK1_L-_CON
AUD_SPK1_L+_CON
AUD_SPK1_R-_CON
AUD_SPK1_R+_CON
OUT_RN_CON
OUT_RP_CON
ED2901 AZ5125-02S-R7G-GP
ED2902 AZ5125-02S-R7G-GP
ED2903 AZ5125-02S-R7G-GP
75.05125.07D
2nd = 075.05125.007D

Change to 3v3
3D3V_S0
1D8V_S0
AMP_VDD1V8
AMP_AVDD2_1V8
3P3A_DVDD_IO
R2934 0R0402-PAD-1-GP
R2935 0R0402-PAD-1-GP
R2936 0R0402-PAD-1-GP
5V_S0
SPK_VDD5V
R2937 0R0402-PAD-1-GP
R2938 20KR2F-L3-GP

MICBD1
ACES-CON15-9-GP
20.F1633.014
2nd = 20.F1261.014
3D3V_CAMERA_S0
CCD_USB20_CON_N
CCD_USB20_CON_P
DMIC2_DATA_CON
DMIC_CLK_CON
DMIC1_DATA_CON
DMIC1_CLK_CPU
DMIC2_CLK_CPU
DMIC2_DATA_CPU
ER2957 33R2J-L1-GP
ER2955 SBY100505T-121Y-N-GP
68.00225.091
2nd = 68.00084.001
ER2956 33R2J-L1-GP
NON-MS
SB
ER2922 33R2J-L1-GP
ER2923 33R2J-L1-GP
ER2958 33R2J-L1-GP
ER2924 33R2J-L1-GP
MS

Camera Power
F2902 POLYSW-1D1A6V-9-GP-U
69.48001.081
2ND = 69.50011.081
C2958 SC10U6D3V3MX-L-GP
C2959 SC1U10V2KX-L-GP
3rd = 068.24900.2001
2nd = 68.00396.001
68.01012.20B
FILTER-4P-137-GP-U
EL2901

EU2905
I/O1
I/O4
GND
VDD
I/O2
I/O3
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C
EC2963 SC22P50V2JN-1-GP
EC2961 SC22P50V2JN-1-GP
EC2962 SC22P50V2JN-1-GP

DIS

Wistron Corporation
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Title: Speaker/HPMIC
Size: Custom
Document Number: Buzz_KBL
Rev: 2
Date: Friday, July 07, 2017
Sheet 29 of 106

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DIS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		
Size A4	Document Number **Buzz_KBL**	Rev **2**
Date: Friday, July 07, 2017	Sheet 30 of 106	

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Title	***(LAN+VGA) CONNECTOR***	
Size A4	Document Number **Buzz_KBL**	Rev **2**
Date: Friday, July 07, 2017	Sheet 31 of 106	

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緯創資通 **Wistron Corporation**
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Title: ***RTS5170(CARD READER)***

Size	Document Number	Rev
A3	Buzz_KBL	2

Date: Friday, July 07, 2017 Sheet 32 of 106

SSID = SDIO

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DIS

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Title

Size	Document Number	Rev
A4	Buzz_KBL	2

Date: Friday, July 07, 2017 Sheet 33 of 106

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Title		
Size A4	Document Number **Buzz_KBL**	Rev **2**
Date: Friday, July 07, 2017	Sheet 34 of 106	

[15] USB1_USB20_N
[15] USB1_USB20_P
[24,35,64] USB_PWR_EN#
[15] USB1_USB30_RX_N
[15] USB1_USB30_RX_P
[15] USB1_USB30_TX_N
[15] USB1_USB30_TX_P
[24,35,64] USB_PWR_EN#
[89] USB1_CON_USB20_N
[89] USB1_CON_USB20_P
[36] USB2_CHAR_N
[36] USB2_CHAR_P
[15] USB2_USB30_RX_N
[15] USB2_USB30_RX_P
[15] USB2_USB30_TX_N
[15] USB2_USB30_TX_P
[89] USB2_CON_USB20_N
[89] USB2_CON_USB20_P

Low Active 2A

5V_S5
USB_PWR_EN#
U3501
IN
EN#
OUT
GND
OC#
SY6288DAAC-GP
074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F
C3501
SC1U10V2KX-L1-GP
C3502
SCD1U25V2KX-L-GP
5V_USB30
C3504
SC100U6D3V6MX-GP

USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

EU3501
USB1_USB30_RX_N
USB1_USB30_RX_P
USB1_USB30_TX_N
USB1_USB30_TX_P
SCD1U25V2KX-L-GP
C3508
C3509
SCD1U25V2KX-L-GP
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

5V_USB30
USB1
VBUS
D-
D+
GND-DRAIN
STDA_SSRX-
STDA_SSRX+
STDA_SSTX-
STDA_SSTX+
CHASSIS#12
CHASSIS#13
GND
USB3.0
SKT-USB13-348-GP-U
022.10005.08R1
2nd = 022.10005.08Q1
3rd = 022.10005.08W1

EL3501
USB1_USB20_N
USB1_USB20_P
FILTER-4P-137-GP-U
68.01012.20B
2nd = 68.00396.001
3rd = 068.24900.2001

EU3503
I/O1
I/O2
I/O3
I/O4
GND
VDD
5V_S5
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

EU3502
USB2_USB30_RX_N
USB2_USB30_RX_P
USB2_USB30_TX_N
USB2_USB30_TX_P
SCD1U16V2KX-L-GP
C3520
C3521
SCD1U16V2KX-L-GP
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

5V_USB30_CHARGER
USB2
SKT-USB13-348-GP-U
022.10005.08R1
2nd = 022.10005.08Q1
3rd = 022.10005.08W1

5V_USB30_CHARGER
C3516
SC100U6D3V6MX-GP
EC3501
SCD1U25V2KX-L-GP

EL3502
USB2_CHAR_N
USB2_CHAR_P
FILTER-4P-137-GP-U
68.01012.20B
2nd = 68.00396.001
3rd = 068.24900.2001

DIS

緯創資通 Wistron Corporation
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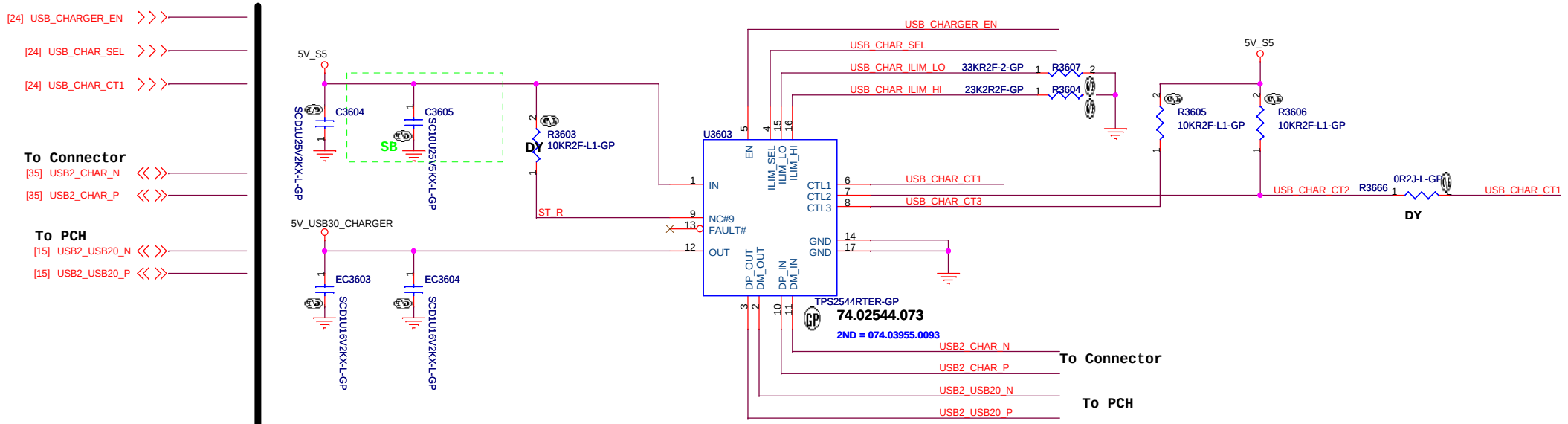
Title: USB 3.0
Size: Custom
Document Number: Buzz_KBL
Rev: 2
Date: Friday, July 07, 2017
Sheet 35 of 106



CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	1	X			
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 (1)	ILIM_LO	
1	1	1	1	CDP (1)	ILIM_HI	Data Lines Connected

DIS

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Title: **USB CHARGER**

Size	Document Number	Rev
Custom	Buzz_KBL	2

Date: Friday, July 07, 2017 Sheet 36 of 106

Blanking

DIS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Reserved***	
Size A4	Document Number **Buzz_KBL**	Rev **2**
Date: Friday, July 07, 2017	Sheet 37 of 106	

Blanking

DIS

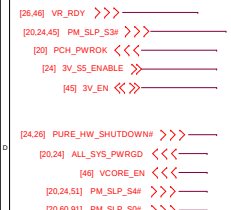
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Size A4	Document Number Buzz_KBL	Rev 2
Date: Friday, July 07, 2017	Sheet 38 of 106	

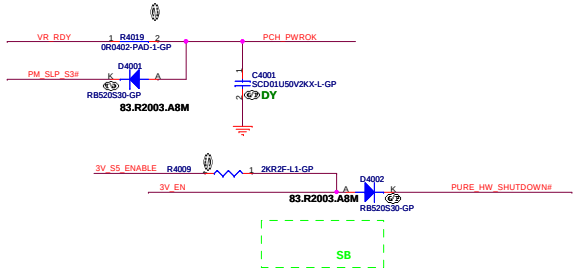
Blanking

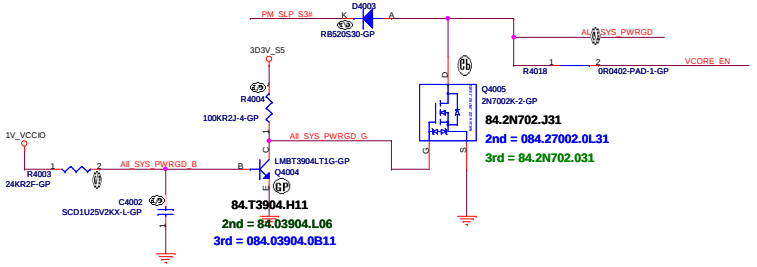
DIS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Size A4	Document Number Buzz KBL	Rev 2
Date: Friday, July 07, 2017	Sheet 39 of	106

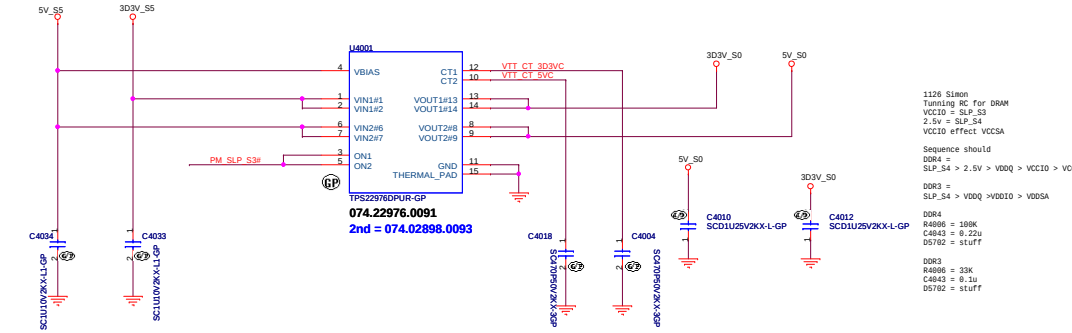
Power Sequence







ANNIE Run Power



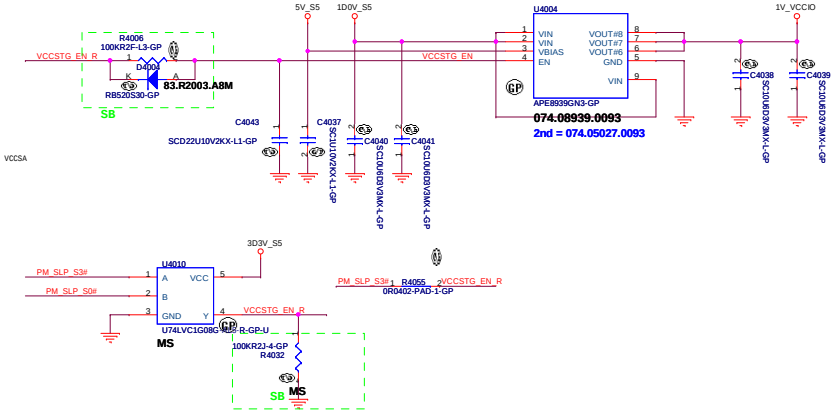
1126 Simon
Tunning RC for DRAM
VCCIO = SLP_S3
2.5v = SLP_S4
VCCIO effect VCCSA

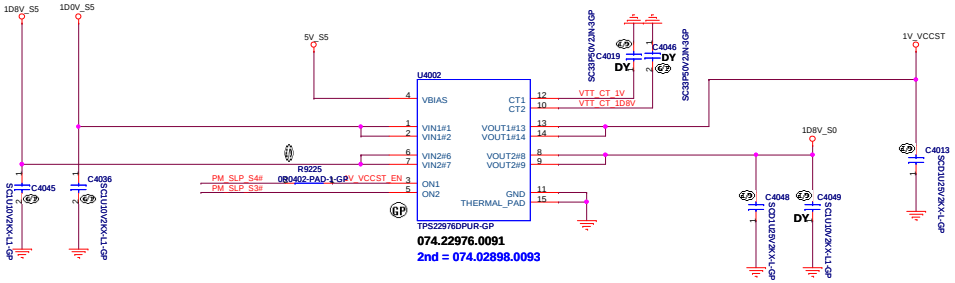
Sequence should
DDR4 =
SLP_S4 > 2.5V > VDDQ > VCCIO > VCCSA

DDR3 =
SLP_S4 > VDDQ >VDDIO > VDDSA

DDR4
R4006 = 100K
C4043 = 0.22u
D5702 = stuff

DDR3
R4006 = 33K
C4043 = 0.1u
D5702 = stuff





DIS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Power Plane Enable & SEQUENCE	
Size: Custom	Document Number: Buzz_KBL	Rev: 2
Date: Friday, July 07, 2017	Sheet 40 of 106	

Blanking

DIS

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Title: ***(Reserved)***

Size	Document Number	Rev
A4	Buzz_KBL	2

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DIS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***DCIN JACK***
Size: A4	Document Number: **Buzz_KBL**
Rev: **2**	
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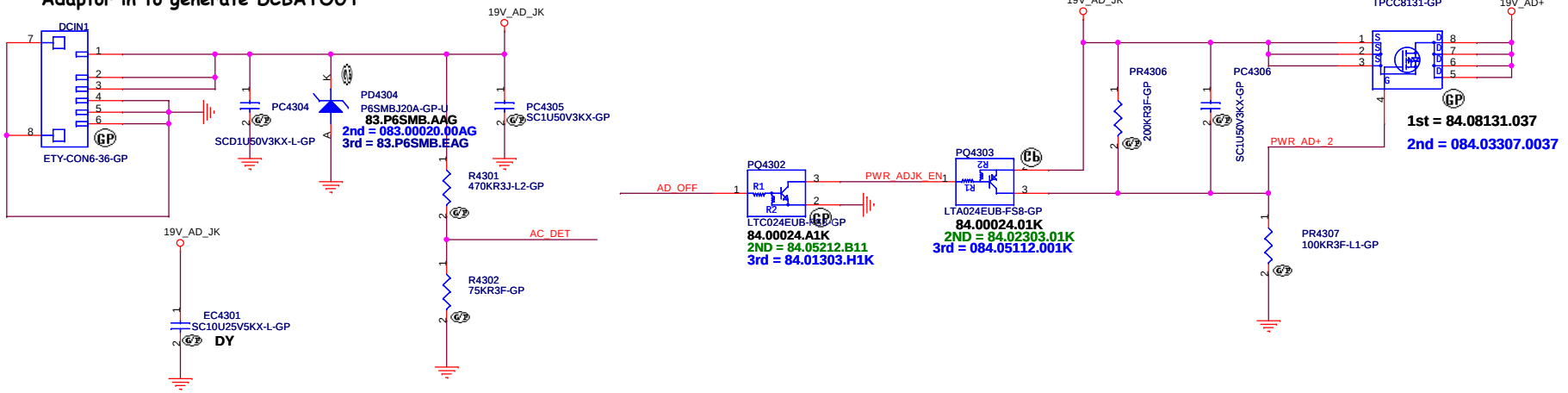
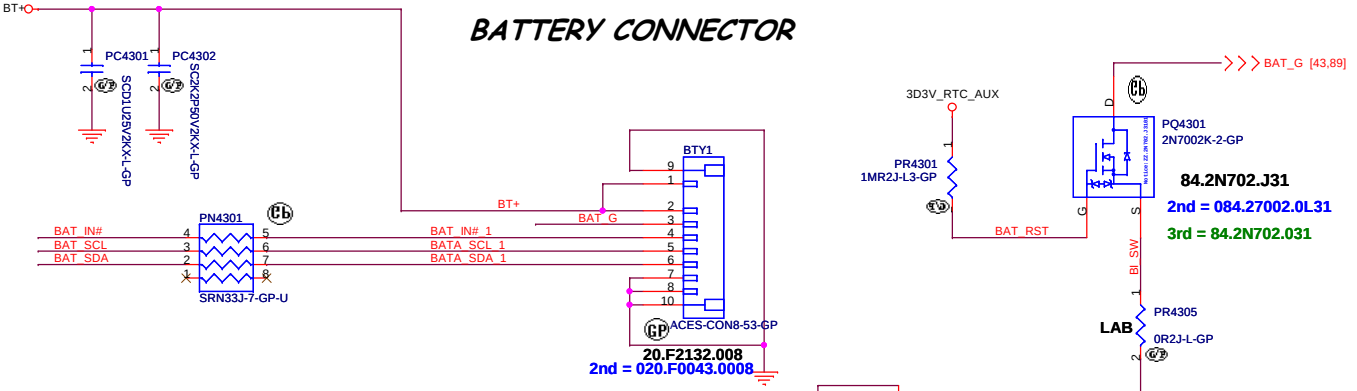
ANNIE solution

[24] AD_OFF
[24,44] BAT_IN#
[24,44] BAT_SCL
[24,44] BAT_SDA
[43,89] BAT_G
[89] BAT_IN#_1
[89] BATA_SCL_1
[89] BATA_SDA_1
[64] BAT_RST
[74] AC_DET

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



Battery Insert

DIS

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Title	**BATT CONN**	
Size: Custom	Document Number: **Buzz_KBL**	Rev: 2
Date: Friday, July 07, 2017	Sheet 43 of 106	

SSID = Charger

close to PU4401

PD 0624 change

Cyntec. 6.5mm x 6.9mm x 3.0mm
DCR: 28m ~ 33mOhm
Idc : 5.5A , Isat : 6.5A

Charger Current=1.4~3.6A

close to PU4404

Total Power Setting

SMBuS

IDCHG : Dischange detect current :
= 8 or 16 x (Vsrn - Vsrp)

IADP : AC adapter detect current :
= 20 or 40 x (Vacp - Vacn) / 10mohm

PMON : Total system power

	Stat	PM_SLP_A#	Adaptor Current	AC_Protect preset	AC_Protect Current	PR4404 Sense resistor	0x12H_Bit 4 IADP GAIN	0x3EH_Bit 7 CM_VREF	Current to Voltage	R1 PR4407	R2 PR4401	CAL Vcomp	Vsense	R1	R2
40W	AC+Battery	High	7.1	102%	7.242	10	40	1.2 V	1.79136	41.2	100	1.213598	1.7136	41.2	100
45W	AC+Battery	High	2.37	102%	2.4174	20	40	1.2 V	1.93392	60.4	100	1.206686	1.93392	60.4	100
65W	AC+Battery	High	3.42	102%	3.4884	10	40	1.2 V	1.39536	16.2	100	1.200826	1.39536	16.2	100
90W	AC+Battery	High	4.76	102%	4.8348	10	40	1.2 V	1.93392	60.4	100	1.206686	1.93392	60.4	100
120W	AC+Battery	High	6.31	102%	6.4362	10	40	1.2 V	2.57448	113	100	1.208676	2.57448	113	100
135W	AC+Battery	High	7.1	102%	7.242	10	40	1.2 V	2.8968	140	100	1.207	2.8968	140	100

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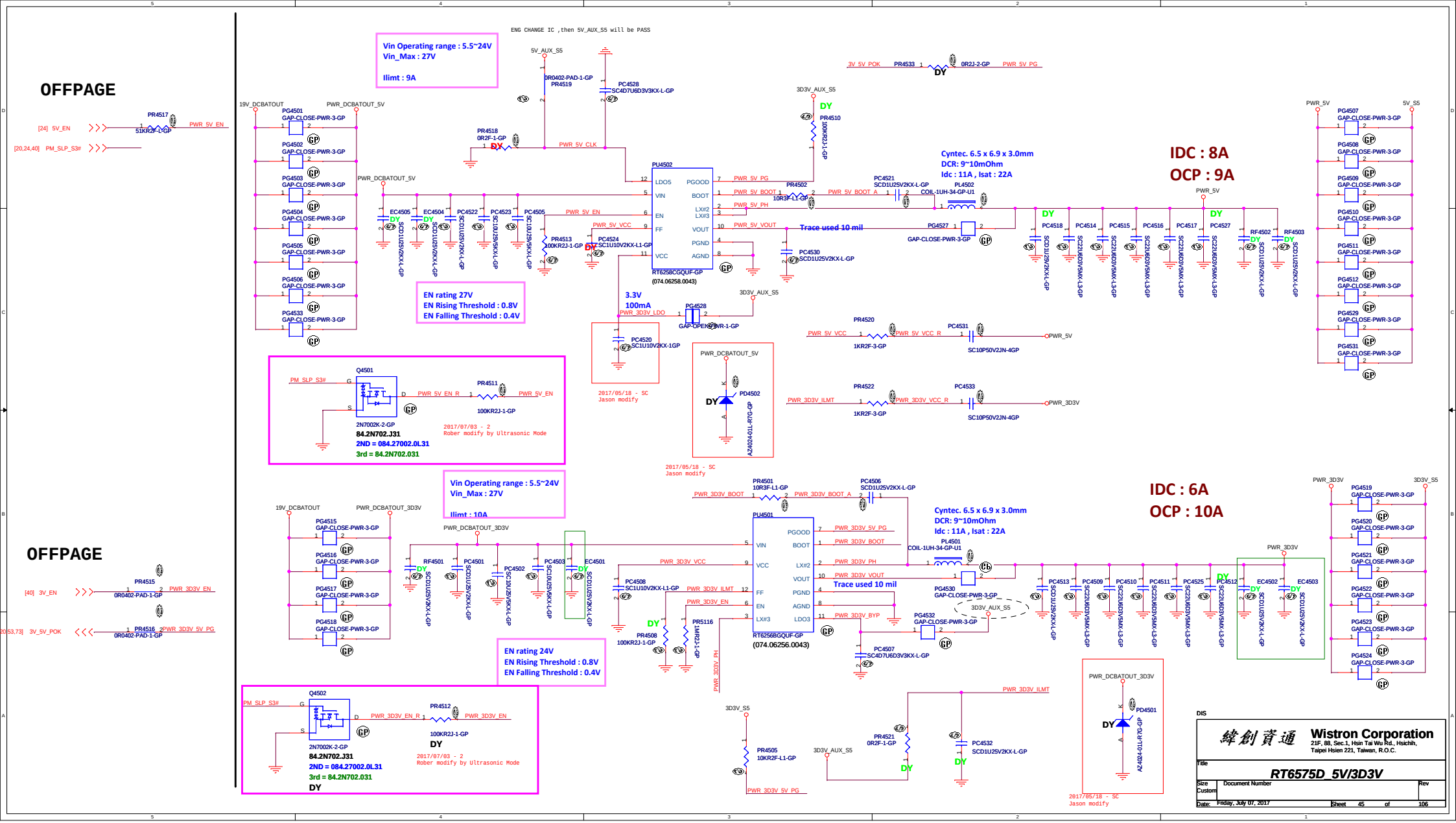
Title	CHARGER HPA02224
Size / Custom	Document Number: Buzz_KBL
Rev	2
Date: Friday, July 07, 2017	Sheet 44 of 106


OFFPAGE
[24] 5V_EN
[20,24,40] PM_SLP_S3#
PR4517
51KR2F-L-GP
PWR_5V_EN
ENG CHANGE IC ,then 5V_AUX_S5 will be PASS
Vin Operating range : 5.5~24V
Vin_Max : 27V
Ilimt : 9A
5V_AUX_S5
PR4519
0R0402-PAD-1-GP
PC4528
SC4D7U6D3V3KX-L-GP
PR4518
0R2F-1-GP
PWR_5V_CLK
19V_DCBATOUT
PWR_DCBATOUT_5V
PG4501
PG4502
PG4503
PG4504
PG4505
PG4506
PG4533
GAP-CLOSE-PWR-3-GP
PU4502
RT6258CGQUF-GP
(074.06258.0043)
LDO5
VIN
EN
FF
VCC
PGOOD
BOOT
LX#2
LX#3
VOUT
PGND
AGND
PWR_5V_PG
PWR_5V_BOOT
PWR_5V_PH
PWR_5V_VOUT
PWR_5V_EN
PWR_5V_VCC
3V_5V_POK
PR4533
0R2J-2-GP
PWR_5V_PG
3D3V_AUX_S5
PR4510
100KR2J-1-GP
PR4502
10R3F-L1-GP
PC4521
SCD1U25V2KX-L-GP
PL4502
COIL-1UH-34-GP-U1
Cyntec. 6.5 x 6.9 x 3.0mm
DCR: 9~10mOhm
Idc : 11A , Isat : 22A
IDC : 8A
OCP : 9A
Trace used 10 mil
PC4530
PG4527
PC4518
PC4514
PC4515
PC4516
PC4517
PC4527
RF4502
RF4503
PWR_5V
5V_S5
PG4507
PG4508
PG4509
PG4510
PG4511
PG4512
PG4529
PG4531
EC4505
EC4504
EC4522
EC4523
PC4505
PR4513
100KR2J-1-GP
PC4524
SC1U10V2KX-L1-GP
EN rating 27V
EN Rising Threshold : 0.8V
EN Falling Threshold : 0.4V
3.3V
100mA
PWR_3D3V_LDO
PG4528
GAP-OPEN-PWR-1-GP
PC4520
SC1U10V2KX-1GP
2017/05/18 - SC
Jason modify
PR4520
1KR2F-3-GP
PC4531
SC10P50V2JN-4GP
PR4522
PC4533
PWR_3D3V_ILMT
PWR_3D3V_VCC_R
PWR_3D3V
Q4501
2N7002K-2-GP
PM_SLP_S3#
PWR_5V_EN_R
PR4511
100KR2J-1-GP
84.2N702.J31
2ND = 084.27002.0L31
3rd = 84.2N702.031
2017/07/03 - 2
Rober modify by Ultrasonic Mode
PD4502
AZ4024-01L-R7G-GP
OFFPAGE
[40] 3V_EN
[20,53,73] 3V_5V_POK
PR4515
0R0402-PAD-1-GP
PWR_3D3V_EN
PR4516
0R0402-PAD-1-GP
PWR_3D3V_5V_PG
Vin Operating range : 5.5~24V
Vin_Max : 27V
Ilimt : 10A
19V_DCBATOUT
PWR_DCBATOUT_3D3V
PG4515
PG4516
PG4517
PG4518
PU4501
RT6256BGQUF-GP
(074.06256.0043)
PGOOD
VIN
VCC
FF
EN
BOOT
LX#2
LX#3
VOUT
PGND
AGND
LDO3
PWR_3D3V_5V_PG
PWR_3D3V_BOOT
PWR_3D3V_PH
PWR_3D3V_VOUT
PWR_3D3V_VCC
PWR_3D3V_ILMT
PWR_3D3V_EN
PWR_3D3V_BYP
PR4501
10R3F-L1-GP
PC4506
SCD1U25V2KX-L-GP
PC4508
SC1U10V2KX-L1-GP
PR4508
100KR2J-1-GP
PR5116
1MR-1-GP
PC4507
SC4D7U6D3V3KX-L-GP
PL4501
COIL-1UH-34-GP-U1
Cyntec. 6.5 x 6.9 x 3.0mm
DCR: 9~10mOhm
Idc : 11A , Isat : 22A
IDC : 6A
OCP : 10A
Trace used 10 mil
PG4530
PG4532
PC4513
PC4509
PC4510
PC4511
PC4525
PC4512
EC4502
EC4503
PWR_3D3V
3D3V_S5
PG4519
PG4520
PG4521
PG4522
PG4523
PG4524
RF4501
PC4501
PC4502
PC4503
EC4501
EN rating 24V
EN Rising Threshold : 0.8V
EN Falling Threshold : 0.4V
Q4502
2N7002K-2-GP
PM_SLP_S3#
PWR_3D3V_EN_R
PR4512
100KR2J-1-GP
DY
84.2N702.J31
2ND = 084.27002.0L31
3rd = 84.2N702.031
2017/07/03 - 2
Rober modify by Ultrasonic Mode
PR4505
10KR2F-L1-GP
PR4521
0R2F-1-GP
PC4532
SCD1U25V2KX-L-GP
PD4501
dP-DL-HT01-V20VZV
2017/05/18 - SC
Jason modify
DIS
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT6575D_5V/3D3V
Size
Custom
Document Number
Rev
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Main Func = CPU_CORE

OFFPAGE

[22,24,44] PROCHOT#_CPU — PR4602 0R0402-PAD-1-GP — PWR_CPU_PROCHOT#

[7] SVID_ALERT#_CPU — PR4603 0R0402-PAD-1-GP — PWR_VCORE_ALERT#

[7] SVID_CLK_CPU — PR4607 0R0402-PAD-1-GP — VIDSCK_CPU_R

[7] SVID_DATA_CPU — PR4608 0R0402-PAD-1-GP — VIDSOUT_CPU_R

[26,40] VR_RDY — PR4612 0R0402-PAD-1-GP — PWR_IMVP_PWRGD

[40] VCORE_EN — PR4618 0R0402-PAD-1-GP — PWR_VR_EN

[7] VSSCORE_SENSE — PR4617 0R0402-PAD-1-GP — PWR_VCORE_RTN

[7] VCCCORE_SENSE — PR4627 0R0402-PAD-1-GP — PWR_VCORE_VSEN

[8] VCCGT_SENSE — PR4623 0R0402-PAD-1-GP — PWR_VCCGT_VSEN

[8] VSSGT_SENSE — PR4625 0R0402-PAD-1-GP — PWR_VCCGT_RTN

[8] VSSSA_SENSE — PR4631 0R0402-PAD-1-GP — PWR_VCCSA_RTN

[8] VCCSA_SENSE — PR4634 0R0402-PAD-1-GP — PWR_VCCSA_FB2

[44] PSYS — PR4643 0R0402-PAD-1-GP — PWR_VCORE_PSYS

1V_VCCST — PR4600 0R0402-PAD-1-GP — PR4601 100R2F-L3-GP — PC4602 SCD1U25V2KX-L-GP — DY

VIDSOUT_CPU_R
PWR_VCORE_ALERT#
VIDSCK_CPU_R

1V_VCCST — PR4619 1KR2F-L1-GP — PR4601 100R2F-L3-GP — DY

PWR_CPU_PROCHOT# — PWR_VCORE_VRHOT#

PWR_VREF

PR4604 4K42R2F-GP — PWM_VCORE_SET1
PR4605 9K53R2F-GP — PWM_VCORE_SET4
PR4606 21K3R3F-GP — PWM_VCORE_SET3
PR4613 60D4R2F-GP — PWM_VCORE_SET1
PR4614 0R0402-PAD-1-GP — PWM_VCORE_SET2
PR4615 392R2F-GP — PWM_VCORE_SET3
PR4620 4K32R2F-GP — PWM_VCORE_SET1
PR4621 9K1R2F-1-GP — PWM_VCORE_SET2
PR4622 10K7R2F-GP — PWM_VCORE_SET3
PR4629 24D9R2F-L-GP — PWM_VCORE_SET1
PR4630 143R2F-1-GP — PWM_VCORE_SET2
PR4626 130R2F-1-GP — PWM_VCORE_SET3

5V_S5 — DY — 5V_CORE_S0 — R4678 0R3-0-U-GP — 5V_S0 — R4679 0R0603-PAD-1-GP-U — SB

5V_CORE_S0 — SB — PR4618 8D2R3F-GP — PC4603 SC4D7U6D3V3KX-L-GP

PWR_VREF — 19V_DCBATOUT — PR4624 2D2R3F-L-GP — PR4628 4D99R2F-GP — PC4606 SCD22U10V2KX-L1-GP — PC4608 SC1KP50V2JN-2GP — DY

PWR_VREF — PR4635 52K3R2F-L-GP — SB — PC4610 SC1KP50V2JN-2GP — DY

3D3V_S0 — PR4636 10KR2F-L1-GP — PR4638 49D9R2F-L1-GP — PR4639 10R2F-L1-GP — VIDSCK_CPU_R — VIDSOUT_CPU_R

PWR_VREF — PR4640 31K6R2F-GP — PWR_VCORE_IMON_A — PR4678 NTC-100K-12-GP-U — B = 4250 — PWR_VCORE_IMON_B — PR4642 48D7K92F-GP

PR4641 2K61R2F-1-GP — DY — PC4612 SCD1U25V2KX-2GP

PU4601 RT3602AEGQW-GP 074.03602.0073

Pin	Name	Net
46	PSYS	PWR_VCORE_PSYS
13	VCC	PWR_VCORE_VCC
2	SET1	PWR_VCORE_SET1
5	SET2	PWR_VCORE_SET2
6	SET3	PWR_VCORE_SET3
12	VIN	PWR_VCORE_VIN
42	VREF06/PSET	PWR_VREF
30	IMON_AUXI	PWR_VCCGT_IMON
1	IMON_MAIN	PWR_VCORE_IMON
39	IMON_SA	PWR_VCCSA_IMON
38	VR_READY	PWR_IMVP_PWRGD
31	VR_HOT#	PWR_VCORE_VRHOT#
34	VCLK	PWR_VCORE_SCLK
32	VDIO	PWR_VCORE_SDIO
33	ALERT#	PWR_VCORE_ALERT#
37	EN	PWR_VR_EN
27	VSEN_AUXI	PWR_VCCGT_VSEN
26	COMP_AUXI	PWR_VCCGT_COMP
24	FB_AUXI	PWR_VCCGT_FB
25	RGND_AUXI	PWR_VCCGT_RTN
18	DRVEN_SET	PWR_VCORE_DRVEN_SET
4	COMP_MAIN	PWR_VCORE_COMP
3	FB_MAIN	PWR_VCORE_FB
48	RGND_MAIN	PWR_VCORE_RTN
47	VSEN_MAIN	PWR_VCORE_VSEN
43	COMP_SA	PWR_VCCSA_COMP
45	FB_SA	PWR_VCCSA_FB
44	RGND_SA	PWR_VCCSA_RTN
14	NC#14	
15	NC#15	
19	NC#19	
20	NC#20	
21	NC#21	
36	PWM_SA	PWR_VCCSA_PWM [50]
40	ISENP_SA	PWR_VCCSA_ISUMP [50]
41	ISENN_SA	PWR_VCCSA_ISUMN [50]
22	PWM_AUXI	PWR_VCCGT_PWM [48]
29	ISENP_AUXI	PWR_VCCGT_ISUMP [48]
28	ISENN_AUXI	PWR_VCCGT_ISUMN [48]
16	PWM1_MAIN	PWR_VCORE_PWMA [47]
10	ISEN1P_MAIN	PWR_VCORE_ISUMP_A [47]
7	ISEN1N_MAIN	PWR_VCORE_ISUMN_A [47]
17	PWM2_MAIN	PWR_VCORE_PWMB [47]
9	ISEN2P_MAIN	PWR_VCORE_ISUMP_B [47]
8	ISEN2N_MAIN	PWR_VCORE_ISEN2N_B
35	DRVEN	PWR_VCORE_FCCM# [47,48,49]
23	TSEN_AUXI	PWR_VCCGT_TSEN
11	TSEN_MAIN	PWR_VCORE_TSEN
49	GND	

PR4643 0R0402-PAD-1-GP — [44] PSYS — PWR_VCORE_PSYS

PR4648 10KR2F-L1-GP — PWR_VCCGT_VSEN — PWR_VCCGT_COMP_B — PR4649 0R0402-PAD-1-GP — PC4616 SC220P50V2KX-3GP — PR4650 30KR2F-GP — PWR_VCCGT_COMP_A — PR4651 0R0402-PAD-1-GP — PC4617 SC68P50V2JN-1GP

PC4618 SC1KP50V2JN-2GP — PWR_VCCGT_FB_A — PR4653 0R2F-1-GP — DY

5V_CORE_S0 — SB — PR4645 0R0402-PAD-1-GP

PR4657 10KR2F-L1-GP — PWR_VCORE_VSEN — PWR_VCORE_COMP_B — PR4658 0R0402-PAD-1-GP — PC4619 SC220P50V2KX-3GP — PR4659 52K3R2F-L-GP — PWR_VCORE_COMP_A — PR4660 0R0402-PAD-1-GP — PC4620 SC68P50V2JN-1GP

PC4621 SC1KP50V2JN-2GP — PWR_VCORE_FB_A — PR4663 0R2F-1-GP — DY

PR4666 10KR2F-L1-GP — PWR_VCCSA_FB2 — PWR_VCCSA_COMP_B — PR4667 0R0402-PAD-1-GP — PC4622 SC330P50V2KX-3GP — PR4668 63K4R2F-2-GP — PWR_VCCSA_COMP_A — PR4669 0R0402-PAD-1-GP — PC4623 SC68P50V2JN-1GP

PC4624 SC1KP50V2JN-2GP — PWR_VCCSA_FB_A — PR4673 0R2F-1-GP — DY

PC4601 SC1KP50V2JN-2GP — PWR_VCCSA_ISUMP [50] — PC4605 SCD1U50V2KX-L-GP — PWR_VCCSA_ISUMN [50]

PC4607 SC1KP50V2JN-2GP — PWR_VCCGT_ISUMP [48] — PC4609 SCD1U50V2KX-L-GP — PWR_VCCGT_ISUMN [48]

PR4683 1R2F-GP — PC4611 SC1KP50V2JN-2GP — PC4613 SCD1U25V2KX-L-GP — PWR_VCORE_ISUMP_A [47] — PWR_VCORE_ISUMN_A [47]

	PR4652	PR4682	PR4684
U22	0	0	DY
U42	DY	DY	1R

PR4682 0R2F-1-GP — PR4684 1R2F-GP — U42 — PWR_VCORE_ISUMP_B [47] — PWR_VCORE_ISUMN_B [47]

U22 — PR4652 0R2F-1-GP — PC4615 SCD1U25V2KX-1-GP — OSV_CORE_S0 — SB

PWR_VREF

PR4654 8K45R2F-2-GP — PWR_VCCGT_TSEN_B
PR4655 8K45R2F-2-GP — PWR_VCORE_TSEN_B
PR4661 191R2F-GP
PR4662 187R2F-GP

PR4676 NTC-100K-12-GP-U — B = 4250 — PR4664 100KR2F-L-GP — PWR_VCCGT_TSEN_A

PR4681 NTC-100K-12-GP-U — B = 4250 — PR4677 100KR2F-L-GP — PWR_VCORE_TSEN_A

PR4670 180KR2F-4-L-GP — PWR_VCCGT_TSEN_C
PR4671 178KR2F-GP — PWR_VCORE_TSEN_C
PR4674 357R2F-GP
PR4675 715R2F-GP

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Main Func = CPU_CORE

[46] PWR_VCORE_PWMA
[46,48,50] PWR_VCORE_FCCM#
[46] PWR_VCORE_ISUMP_A
[46] PWR_VCORE_ISUMN_A
[46] PWR_VCORE_PWMB
[46] PWR_VCORE_ISUMP_B
[46] PWR_VCORE_ISUMN_B

19V_DCBATOUT
PWR_DCBATOUT_VCOREA
PG4702 GAP-CLOSE-PWR-3-GP
PG4703 GAP-CLOSE-PWR-3-GP
PG4704 GAP-CLOSE-PWR-3-GP
PG4705 GAP-CLOSE-PWR-3-GP
PG4706 GAP-CLOSE-PWR-3-GP

PC4702 PC4703 PC4704 PC4705 EC4705 SCD10U25V5KX-L-GP / SCD22U25V3KX-L-GP / SCD1U25V2KX-L-GP

5V_CORE_S0 SB
PR4702 2D2R2F-GP
PC4706 SC1U10V2KX-L1-GP
EC4701 EC4702 SCD1U25V2KX-L-GP

PU4702 AOZ5049QI-1-GP
GH GL#19 GL#20 BOOT NC#23 VCC VIN VSWH#5 VSWH#13 VSWH#14 VSWH#15 VSWH#16 PGND PWM FCCM
PWR_VCORE_VCCDA
PWR_VCORE_BOOTA
PWR_VCORE_PHASEDA
PWR_VCORE_SWA
PWR_VCORE_PWM_RA
PWR_VCORE_FCCM#A
PWR_VCORE_PWMA
PWR_VCORE_FCCM#
PC4707 SCD22U25V3KX-GP
PR4703 2D2R3E-L-GP
PR4704 0R0402-PAD-1-GP
PR4705 0R0402-PAD-1-GP

074.05049.0A73

SKL_U42
Icc(max)=64A
TDC=42A

Confirm with EE
22uF/0805 total 32pcs
(78.22610.L2L)

Cyntec. 6.8mm x7.6mmx3.0mm
DCR: 0.9m Ohm+/-7%
Idc : 37A , Isat : 41A

1V_CPU_CORE
PL4702 COIL-D15UH-7-GP
068.R1510.2041
PT4702 SE330U2VDM-4-GP
RF4703 SCD1U25V2KX-L-GP
PANASONIC
ESR: 9 mohm

PWR_VCORE_SWA
PR4707 2D2R6J-3-GP
PWR_VCORE_SNB
PC4709 SC1KP50V2KX-L-1-GP

PR4708 360R2F-GP
PC4708 SCD47U25V3KX-1GP
PR4709 10KR2F-L1-GP
PWR_VCORE_ISUMP_A
PWR_VCORE_ISUMN_A
CLOSE to IC

19V_DCBATOUT
PWR_DCBATOUT_VCOREB
PG4708 PG4709 PG4710 PG4711 PG4712 GAP-CLOSE-PWR-3-GP

PC4701 PC4711 PC4712 PC4710 EC4706 SCD10U25V5KX-L-GP / SCD22U25V3KX-L-GP / SCD1U25V2KX-L-GP

PU4701 AOZ5049QI-1-GP
PWR_VCORE_VCCDB
PWR_VCORE_BOOTB
PWR_VCORE_PHASEDB
PWR_VCORE_SWB
PWR_VCORE_PWM_RB
PWR_VCORE_FCCM#B
PWR_VCORE_PWMB
PWR_VCORE_FCCM#
PC4714 SCD22U25V3KX-GP
PR4711 2D2R3E-L-GP
PR4701 0R0402-PAD-1-GP
PR4712 0R0402-PAD-1-GP

074.05049.0A73
U42

SKL_U42
Icc(max)=64A
TDC=42A

Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)

Cyntec. 6.8mm x7.6mmx3.0mm
DCR: 0.9m Ohm+/-7%
Idc : 37A , Isat : 41A

1V_CPU_CORE
PL4701 COIL-D15UH-7-GP
068.R1510.2041
PT4701 SE330U2VDM-4-GP
RF4702 SCD1U25V2KX-L-GP
PANASONIC
ESR: 9 mohm

PWR_VCORE_SWB
PR4714 2D2R6J-3-GP
PWR_VCORE_SNB_B
PC4716 SC1KP50V2KX-L-1-GP

PR4716 360R2F-GP
PC4715 SCD47U25V3KX-1GP
PR4717 10KR2F-L1-GP
PWR_VCORE_ISUMP_B
PWR_VCORE_ISUMN_B
CLOSE to IC

DIS

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Main Func = CPU_CORE

[46] PWR_VCCGT_PWM
[46,47,50] PWR_VCORE_FCCM#
[46] PWR_VCCGT_ISUMP
[46] PWR_VCCGT_ISUMN

19V_DCBATOUT
PWR_DCBATOUT_VCCGTA

PG4802 GAP-CLOSE-PWR-GP
PG4803 GAP-CLOSE-PWR-GP
PG4804 GAP-CLOSE-PWR-GP
PG4801 GAP-CLOSE-PWR-GP
PG4805 GAP-CLOSE-PWR-GP
PG4806 GAP-CLOSE-PWR-GP

DY PT4803 ST15U25VDM-7-GP
DY PT4802 ST15U25VDM-7-GP
79.15612.207
79.15612.20L

PWR_DCBATOUT_VCCGTA
PC4802 SC10U25V5KX-L-GP
PC4803 SC10U25V5KX-L-GP
PC4804 SC10U25V5KX-L-GP
PC4801 SC10U25V5KX-L-GP
EC4805 SCD1U25V2KX-L-GP

5V_CORE_S0 SB

PR4802 2D2R2F-GP
PC4805 SC1U10V2KX-L1-GP
EC4801 DY SCD1U25V2KX-L-GP
EC4802 DY SCD1U25V2KX-L-GP
PR4803 2D2R3F-L-GP

PU4801
PWR_VCCGT_BOOT
PWR_VCCGT_VCC_R
PWR_DCBATOUT_VCCGTA
PWR_VCCGT_PHASE
PWR_VCCGT_SW
PWR_VCCGT_BOOT_RC
PWR_VCCGT_PWM_R
PWR_VCCGT_FCCM#_R
PWR_VCCGT_PWM
PWR_VCORE_FCCM#
PC4806 SCD22U25V3KX-GP
PR4804 0R0402-PAD-1-GP
PR4805 0R0402-PAD-1-GP
AOZ5049QI-1-GP
074.05049.0A73

SKL_U42
Icc(max)=28A
~~TDC=12A~~

Confirm with EE
22uF/0805 total 26pcs
(78.22610.L2L)

Cyntec. 6.8mm x7.6mmx3.0mm
DCR: 0.9m Ohm+/-7%
Idc : 37A , Isat : 41A

PL4801
COIL-D15UH-7-GP
068.R1510.2041

1V_VCCGT
PG4807 GAP-CLOSE-PWR-3-GP
PG4808 GAP-CLOSE-PWR-3-GP
EC4803 SCD1U25V2KX-L-GP
PT4801 SE330U2VDM-4-GP

PWR_VCCGT_SW
DY PR4808 2D2R6J-3-GP
PWR_VCCGT_SNB
DY PC4808 SC1KP50V2KX-L-1-GP

PWR_VCCGT_ISEN
PR4807 383R2F-1-GP
PC4807 SCD47U25V3KX-1GP
PR4809 82R2F-GP
PR4810 10KR2F-L1-GP
PWR_VCCGT_ISUMP
PWR_VCCGT_NTC
CLOSE to IC
PR4801 NTC-10K-29-GP-U
B = 3370
PWR_VCCGT_ISUMN

DIS

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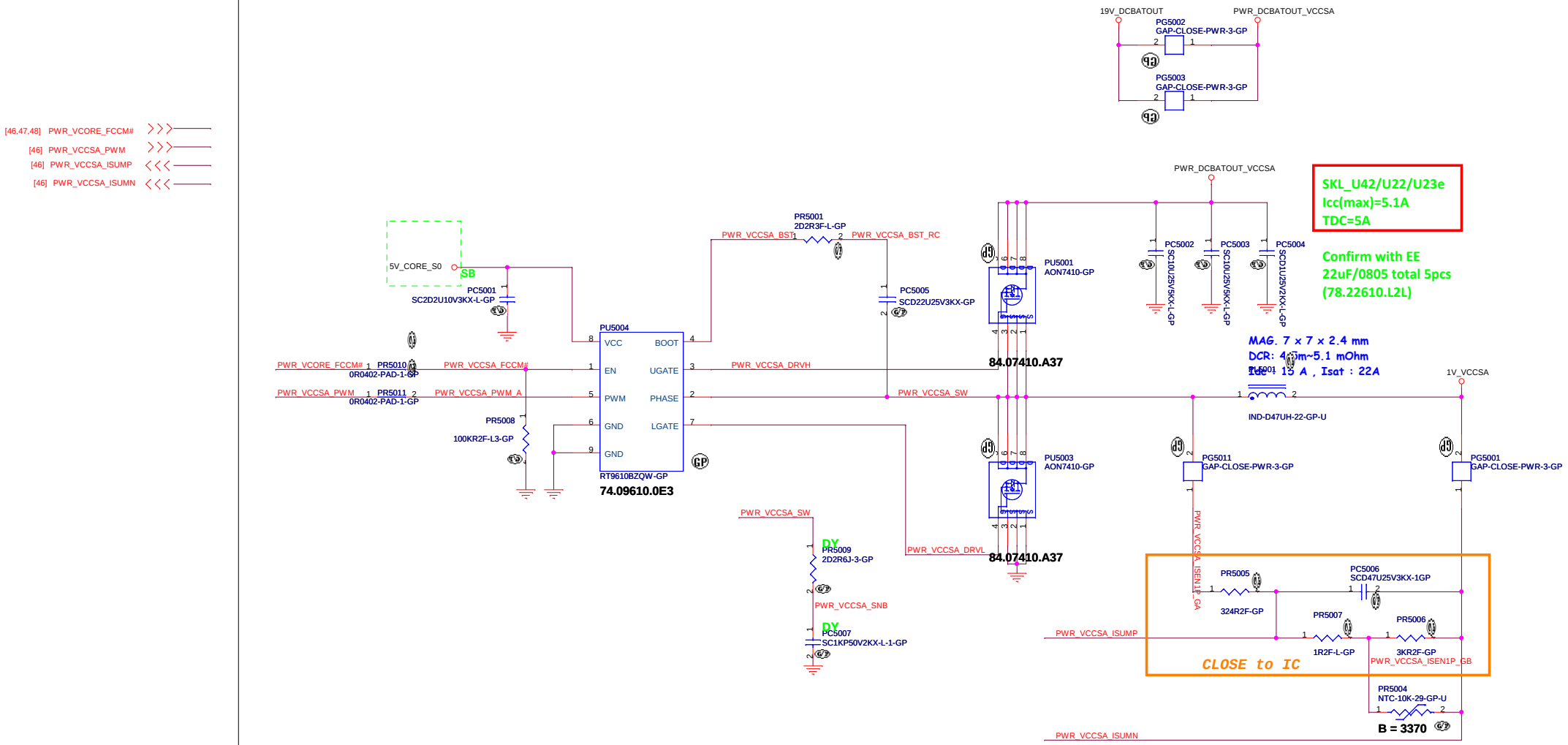
Main Func = CPU_CORE



DIS

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VDDQ ENABLE CONTROL

[4] VTT_CNTL_CPU

2D5V ENABLE CONTROL

[20,24,40] PM_SLP_S4#

19V_DCBATOUT

PWR_DCBATOUT_VDDQ

PG5101 GAP-CLOSE-PWR-6-GP

PG5102 GAP-CLOSE-PWR-6-GP

PG5103 GAP-CLOSE-PWR-6-GP

PWR_VDDQ

1D2V_S3

PG5105 GAP-CLOSE-PWR-6-GP

PG5106 GAP-CLOSE-PWR-6-GP

PG5107 GAP-CLOSE-PWR-6-GP

PG5108 GAP-CLOSE-PWR-6-GP

PG5109 GAP-CLOSE-PWR-6-GP

PG5110 GAP-CLOSE-PWR-6-GP

PG5112 GAP-CLOSE-PWR-6-GP

PG5114 GAP-CLOSE-PWR-6-GP

PG5118 GAP-CLOSE-PWR-6-GP

5V_S5

PR5101 10R2F-L1-GP

PWR_VDDQ_VCC

EC5102 DY SCD1U25V2KX-L-GP

EC5101 DY SCD1U25V2KX-L-GP

PC5102 SC4D7U25V5KX-L2-GP

PC5104 SC1U10V2KX-L1-GP

PR5102 12KR2F-L-GP

PWR_VDDQ_6S

3D3V_S5

PR5104 100KR2J-4-GP

PR5108 = 510K

Fs = 400~550KHz

PWR_VDDQ_PG

PR5108 510KR2F-GP

PWR_VDDQ_TON

2D5V_S3_PWRGD

PR5103 0R0402-PAD-1-GP

PWR_VDDQ_EN

VTT_CNTL_CPU

PR5107 0R0402-PAD-1-GP

PWR_VDDQ_VTT_EN

PG5115 GAP-CLOSE-PWR-6-GP

PWR_VDDQ_LVOIN

PC5103 SC1U10V2KX-L1-GP

PG5119 GAP-CLOSE-PWR-6-GP

PU5101

CS

VCC

PGOOD

TON

S5

S3

VLDOIN

VTTGND

VTTGND

VTTGND

VTT

VTTSNS

NC#26

GND

VTTREF

V+

V+

V+

V+

V+

BST

LX#25

LX#17

LX#18

LX#19

LX#20

LX#35

PGND

PGND

PGND

PGND

PGND

PGND

VDDQSNS

VDDQSET

G5388K11U-GP

074.05388.0043

PWR_VDDQ_VTTREF

PC5114 SCD1U25V2KX-L-GP

PWR_DCBATOUT_VDDQ

PC5108 SCD1U25V2KX-L-GP

PC5101 SC10U25V5KX-L-GP

PC5122 SC10U25V5KX-L-GP

PD5101 L35L24VCB2-GP

SB

DY

PR5112 0R0805-PAD-1-GP-U

PWR_VDDQ_BOOT

PWR_VDDQ_BOOTA

PC5110 SCD1U25V2KX-L-GP

PWR_VDDQ_PH

PL5101 COIL-1UH-34-GP-U1

Cyntec. 6.5 x 6.9 x 3.0mm

DCR: 9~10mOhm

Idc : 11A , Isat : 22A

TDC : 8.0A

PG5104 GAP-CLOSE-PWR-6-GP

PC5106 SC22U6D3V3MX-L-GP

PC5107 SC22U6D3V3MX-L-GP

PC5109 SC22U6D3V3MX-L-GP

PC5121 SC22U6D3V3MX-L-GP

PC5113 SC22U6D3V3MX-L-GP

EC5103 DY SCD1U25V2KX-L-GP

EC5104 DY SCD1U25V2KX-L-GP

PR5105 6K2R2F-GP

PR5106 10K2R2F-GP

Vout= 0.75*(1+R1/R2) = 1.2

0D6V_VREF_S0

PG5111 GAP-CLOSE-PWR-6-GP

PG5113 GAP-CLOSE-PWR-6-GP

PC5111 DY SC10U6D3V3MX-L-GP

PC5112 SC10U6D3V3MX-L-GP

V2D5_S5

MAX=2A

Pd=(3.3-2.5)*0.5=0.4W

3D3V_S5

SC10U6D3V3MX-L-GP PC5118

PU5102 APL5930KAI-TRG-1-GP

74.05930.B3D

VIN#5

VOUT#4

VOUT#3

FB

GND

VCNTL

POK

EN

VIN#9

CRITICAL

5V_S5

PC5119 SC1U50V3KX-GP

PR5111 100KR2J-4-GP

2D5V_PWR_GOOD

PWR_2D5V_PG

PR5113 0R0402-PAD-1-GP

2D5V_S3_PWRGD

PWR_2D5V_PG

PWR_2D5V_EN

PR5125 0R0402-PAD-1-GP

PM_SLP_S4#

PC5120 SCD1U25V2KX-L-GP

2D5V_S3

PG5116 GAP-CLOSE-PWR-6-GP

PG5117 GAP-CLOSE-PWR-6-GP

PWR_2D5V_S3

PC5116 SC10U6D3V3MX-L-GP

PC5115 SC10U6D3V3MX-L-GP

PC5117 SC100P50V2JN-L-GP

PWR_2D5V_FB

PR5115 21.5K_1% 0402

R1

PR5110 10KR2F-L1-GP

R2

Vout = 0.8*(1+R1/R2)=2.52V

DIS

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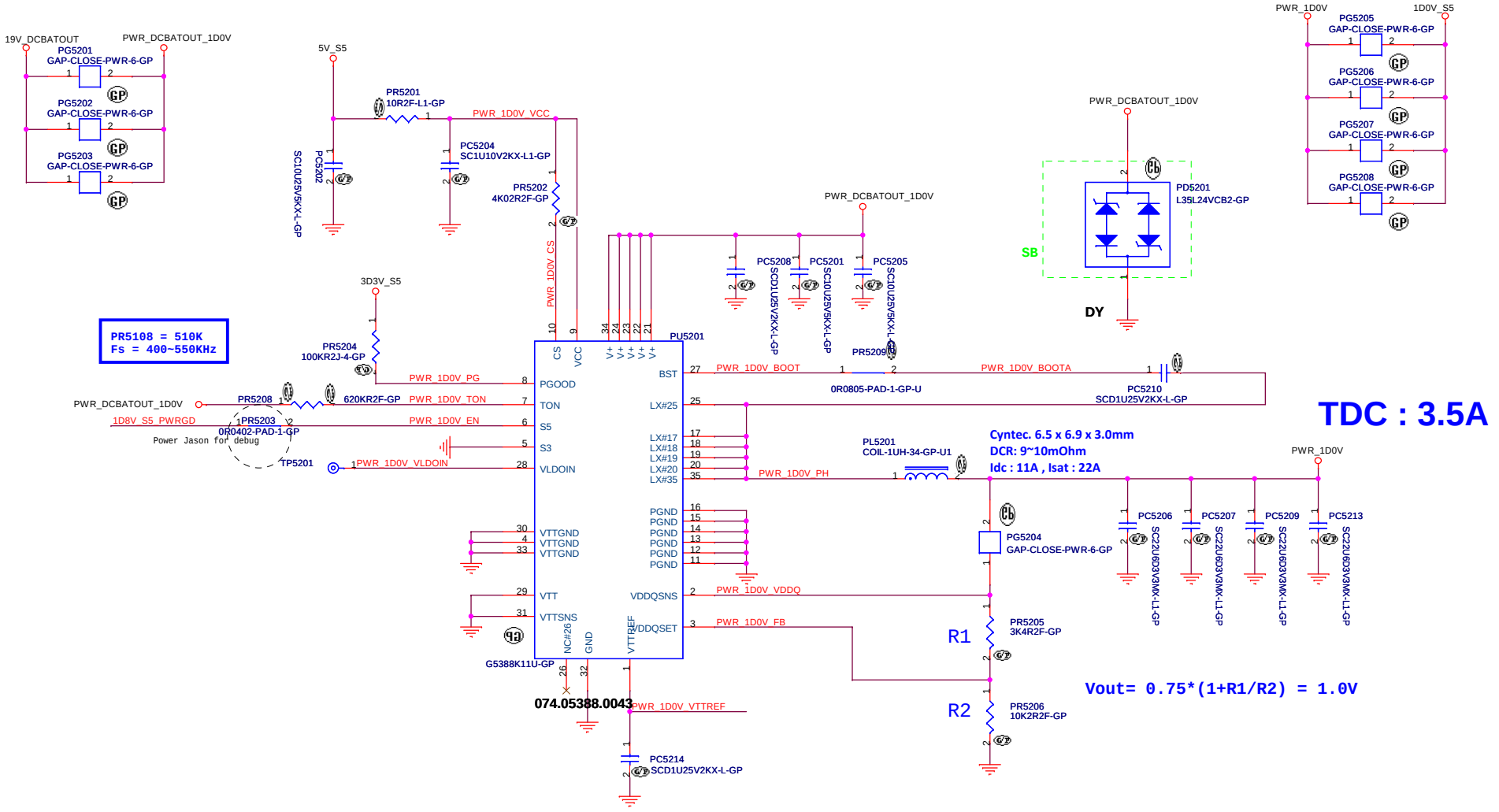
1D0V ENABLE CONTROL

[53] 1D8V_S5_PWRGD



DIS

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Title: ***DC2DC 1D0V_APW8861***

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1D8V_S5 POWER GOOD

1D8V_S5_PWRGD [52]

3V_5V_POK [20,45,73]

1D8V_S5

PD = (Vin Vout) x Iout
= (3.3 - 1.8) x 0.3A = 0.45W
PD de-rating(%) = 0.45W/1.33W = 33.8%
1125 Simon
Vendor suggest to replace 74.09025.A3D by 74.09025.D3D

PU5301
G9661-25ADJF11U-GP-U
74.09661.07D

Vout Setting
Vout = 0.8 * (1 + R1/R2)
= 0.8 * (1 + 12K7 / 10K)
= 1.816V

DIS	
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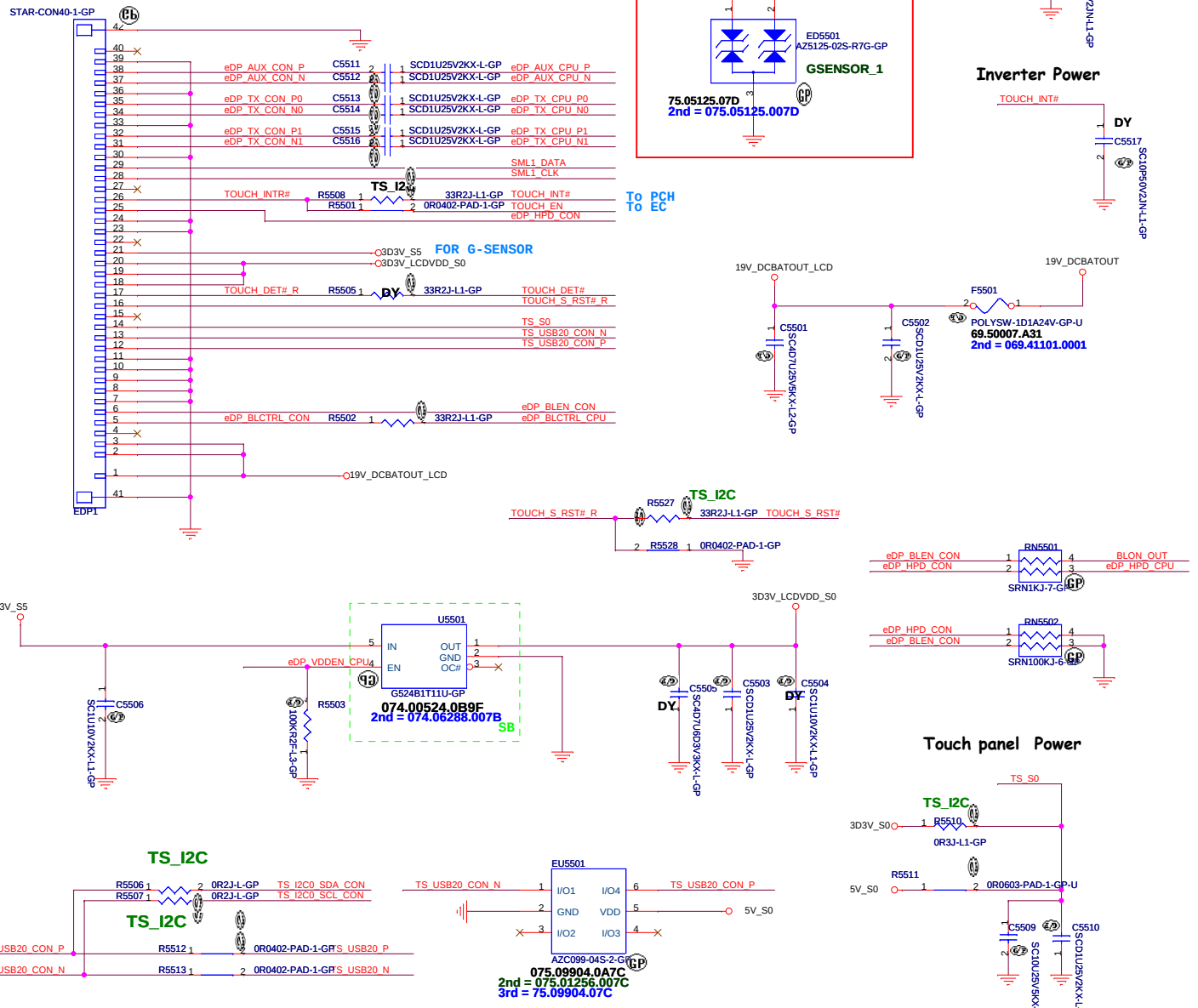
Main Func = LCD

20.K0809.040
2nd = 20.K0678.040
3rd = 020.K0160.0040



[89] TOUCH_DET#_R
[89] TS_S0
[89] eDP_TX_CON_P0
[89] eDP_TX_CON_N0
[89] eDP_TX_CON_P1
[89] eDP_TX_CON_N1
[89] eDP_AUX_CON_P
[89] eDP_AUX_CON_N
[89] TOUCH_INTR#
[89] eDP_HPD_CON
[89] eDP_BLEN_CON
[89] eDP_BLCTRL_CON
[3] eDP_VDDEN_CPU
[3] eDP_AUX_CPU_P
[3] eDP_AUX_CPU_N
[3] eDP_TX_CPU_P0
[3] eDP_TX_CPU_N0
[3] eDP_TX_CPU_P1
[3] eDP_TX_CPU_N1
[6] TOUCH_S_RST#
[18,24,70,73,79] SML1_DATA
[18,24,70,73,79] SML1_CLK
[6] TOUCH_DET#
[24] TOUCH_EN
[24] BLON_OUT
[3] eDP_HPD_CPU
[3] eDP_BLCTRL_CPU
[15] TS_USB20_P
[15] TS_USB20_N
[6,24] TS_I2C0_SDA_CON
[6,24] TS_I2C0_SCL_CON
[22] TOUCH_INT#
[89] TS_USB20_CON_N
[89] TS_USB20_CON_P
[89] TOUCH_S_RST#_R

DIS

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Title

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SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN

[3] HDMI_DATA_CPU_P0
[3] HDMI_DATA_CPU_N0
[3] HDMI_DATA_CPU_P1
[3] HDMI_DATA_CPU_N1
[3] HDMI_DATA_CPU_P2
[3] HDMI_DATA_CPU_N2
[3] HDMI_DATA_CPU_P3
[3] HDMI_DATA_CPU_N3
[3,14,57] HDMI_CLK_CPU
[3,14,57] HDMI_DATA_CPU
[3] HDMI_DET_CPU
[89] HDMI_CLK_CON_N3
[89] HDMI_CLK_CON_P3
[89] HDMI_DATA_CON_P0
[89] HDMI_DATA_CON_N0
[89] HDMI_DATA_CON_P1
[89] HDMI_DATA_CON_N1
[89] HDMI_DATA_CON_P2
[89] HDMI_DATA_CON_N2
[89] HDMI_CLK_CON
[89] HDMI_DATA_CON
[89] HDMI_DET_CON

HDMI_DATA_CPU_N3 C5701 SCD1U16V2KX-L-GP — HDMI_CLK_CON_N3
HDMI_DATA_CPU_P3 C5702 SCD1U16V2KX-L-GP — HDMI_CLK_CON_P3
HDMI_DATA_CPU_N0 C5703 SCD1U16V2KX-L-GP — HDMI_DATA_CON_N0
HDMI_DATA_CPU_P0 C5704 SCD1U16V2KX-L-GP — HDMI_DATA_CON_P0
HDMI_DATA_CPU_N1 C5705 SCD1U16V2KX-L-GP — HDMI_DATA_CON_N1
HDMI_DATA_CPU_P1 C5706 SCD1U16V2KX-L-GP — HDMI_DATA_CON_P1
HDMI_DATA_CPU_N2 C5707 SCD1U16V2KX-L-GP — HDMI_DATA_CON_N2
HDMI_DATA_CPU_P2 C5708 SCD1U16V2KX-L-GP — HDMI_DATA_CON_P2

R5701 470R2F-GP
R5704 470R2F-GP
R5706 470R2F-GP
R5707 470R2F-GP
R5709 470R2F-GP
R5710 470R2F-GP
R5711 470R2F-GP
R5708 470R2F-GP

HDMI PLL GND

ER5701 150R2J-L1-GP-U — HDMI_CLK_CON_N3
ER5702 150R2J-L1-GP-U — HDMI_CLK_CON_P3
ER5703 150R2J-L1-GP-U — HDMI_DATA_CON_N0
ER5704 150R2J-L1-GP-U — HDMI_DATA_CON_P0
HDMI_DATA_CON_P1
HDMI_DATA_CON_N1
HDMI_DATA_CON_P2
HDMI_DATA_CON_N2

Q5702 2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 84.2N702.031
5V_S0

HDMI1 SKT-HDMI23-190-GP
022.10025.00S1
2nd = 022.10025.00M1
SB

HDMI_DATA_CON_P2
HDMI_DATA_CON_N2
HDMI_DATA_CON_P1
HDMI_DATA_CON_N1
HDMI_DATA_CON_P0
HDMI_DATA_CON_N0
HDMI_CLK_CON_P3
HDMI_CLK_CON_N3
HDMI_CLK_CON
HDMI_DATA_CON
5V_HDMI_S0
HDMI_DET_CON

5V_HDMI_S0 — C5733 SCD1U25V2KX-L-GP — F5701 POLYSW-16V-9-GP-U
69.48001.081
2ND = 69.50011.081

HDMI_DET_CON — R5729 150KR2J-L1-GP — HDMI_HPD_B — Q5701 LMBT3904LT1G-GP
84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.T3904.C11
3D3V_S0
R5718 20KR2F-L3-GP
DY
HDMI_DET_CPU
R5717 10KR2J-L-GP

5V_HDMI_S0 — D5701 BAW56H-1-GP
75.00056.D7D
5V_DDC_HDMI1
5V_DDC_HDMI2
RN5701 SRN2K2J-5-GP

3D3V_S0 — Q5703 2N7002KDW-1-GP
[3,14,57] HDMI_CLK_CPU
[3,14,57] HDMI_DATA_CPU
HDMI_CLK_CON
HDMI_DATA_CON

EMI Request:

HDMI_DATA_CON_N0 — HDMI_DATA_CON_P0 — ED5701 L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073
HDMI_CLK_CON_N3
HDMI_CLK_CON_P3

HDMI_DATA_CON_N2 — HDMI_DATA_CON_P2 — ED5702 L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073
HDMI_DATA_CON_P1

HDMI_CLK_CON — HDMI_DET_CON — EU5701 AZC099-04S-2-GP
I/O1 GND I/O2 VDD I/O3 I/O4
HDMI_DATA_CON
5V_HDMI_S0
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

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Title: HDMI Level Shifter/Connector
Size: Custom
Document Number: Buzz_KBL
Rev: 2
Date: Friday, July 07, 2017
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Title		
Size: A	Document Number: Buzz_KBL	Rev: 2
Date: Friday, July 07, 2017	Sheet 58 of 106	

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Title		
Size: A4	Document Number: Buzz_KBL	Rev: 2
Date: Friday, July 07, 2017	Sheet 59 of 106	

HDD_SATA_RX_P [15]
HDD_SATA_RX_N [15]
HDD_SATA_TX_N [15]
HDD_SATA_TX_P [15]
HDD_UNLOAD [69]
PM_SLP_S3# [20,24,40,45]
HDD_PWR_EN# [6]
PM_SLP_S0# [20,40,91]

SSID = SATA

SATA HDD Connector

3D3V_S0 3D3V_HDD_S0 3D3V_S5 R6027 0R0402-PAD-1-GP R6028 0R2J-L-GP DY

5V_S0 R6029 5V_HDD_S0 0R0805-PAD-1-GP-U RF6001 DY SCD1U25V2KX-L-GP RF6002 DY SCD1U25V2KX-L-GP

5V_S0 U6005 VIN VIN VBIAS EN VOUT#8 VOUT#7 VOUT#6 GND VIN HDD_EN# APE8939GN3-GP 074.08939.0093 2nd = 074.05027.0093 5V_HDD_S0 5V_S0 C6015 SC1U10V2KX-L1-GP HDD_PWR_EN# R6025 0R2J-L-GP MS DY HDD_EN# PM_SLP_S0# R6026 0R2J-L-GP MS

5V_HDD_S0 C6005 HDD SC10U25V5KX-L-GP C6006 HDD SCD1U25V2KX-L-GP HDD_UNLOAD HDD_SATA_RX_C_P HDD_SATA_RX_C_N HDD_SATA_TX_C_N HDD_SATA_TX_C_P J9 HDD1 HRS-CON12-8-GP 20.K0824.012 2nd = 020.K0125.0012 3rd = 020.K0190.0012 SB

3D3V_HDD_S0 U6001 VCC VCC TX1P TX1N TX2P TX2N RX1P RX1N RX2P RX2N EN DE1 DE2 DEW1 DEW2 GND GND GND GND SN75LVCP601RTJR-GP

HDD_SATA_TX_P SCD01U50V2KX-L-GP C6018 HDD_SATA_TX_RE_P
HDD_SATA_TX_N SCD01U50V2KX-L-GP C6019 HDD_SATA_TX_RE_N
HDD_SATA_RX_C_P SCD01U50V2KX-L-GP C6020 SATA_RX_REO_P0
HDD_SATA_RX_C_N SCD01U50V2KX-L-GP C6021 SATA_RX_REO_N0

SATA_TX_REO_P0 C6022 SCD01U50V2KX-L-GP HDD_SATA_TX_C_P
SATA_TX_REO_N0 C6023 SCD01U50V2KX-L-GP HDD_SATA_TX_C_N
HDD_SATA_RX_RE_P C6024 SCD01U50V2KX-L-GP HDD_SATA_RX_P
HDD_SATA_RX_RE_N C6025 SCD01U50V2KX-L-GP HDD_SATA_RX_N

EQ1 EQ2 3D3V_HDD_S0 HDD_EN R6033 10KR2J-3-GP R6035 0R2J-L-GP DY PM_SLP_S0#

DY EU6001 HDD_SATA_RX_C_P HDD_SATA_RX_C_N HDD_SATA_TX_C_N HDD_SATA_TX_C_P L05ESDL5V0NA-4-GP 075.00550.0071 2nd = 075.08809.0073 3rd = 075.01043.0073

3D3V_HDD_S0 10KR2J-3-GP R6010 EQ1 R6016 DY
10KR2J-3-GP R6011 EQ2 R6017 DY
10KR2J-3-GP R6012 DE1 R6018 DY
10KR2J-3-GP R6013 DE2 R6019 DY
10KR2J-3-GP R6014 DEW1 R6020 DY
10KR2J-3-GP R6015 DEW2 R6021 DY

DIS

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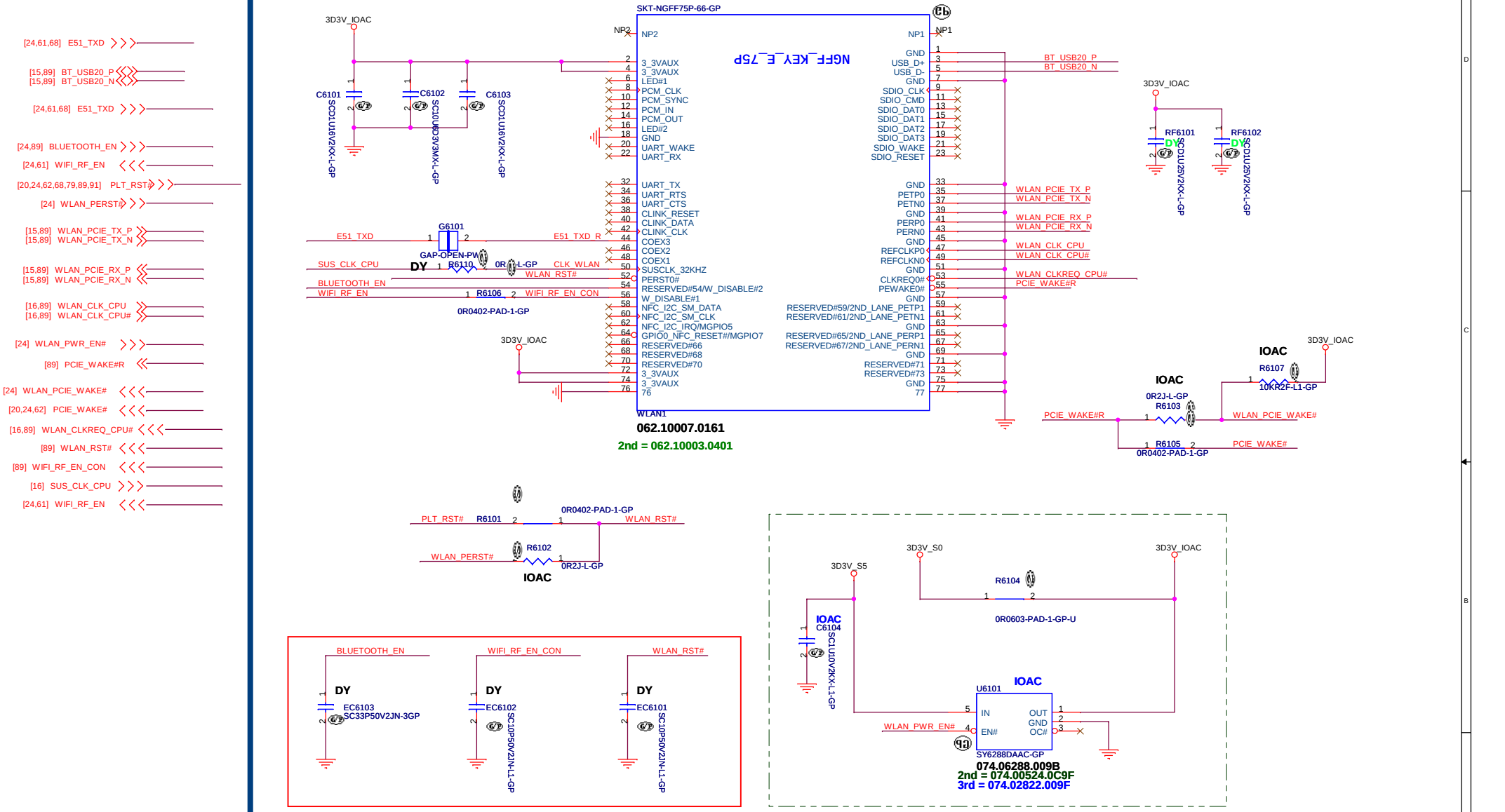
Title: HDD_GSENSOR

Size: Custom | Document Number: Buzz_KBL | Rev: 2

Date: Friday, July 07, 2017 | Sheet 60 of 106

SSID = Wireless Mini Card Connector(802.11a/b/g/n)



DIS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Mini Card-WLAN		
Size: Custom	Document Number: Buzz_KBL	Rev: 2
Date: Friday, July 07, 2017	Sheet 61 of 106	

SSID = mSATA

Mini Card Connector(mSATA)

[20,24,61] PCIE_WAKE#
[16] SSD1_CLKREQ_CPU_N
[20,24,61,68,79,89,91] PLT_RST#
[15,62] SSD1_PEDET
[15] DEVSLP1
[16,62] SSD1_CLK_CPU
[16,62] SSD1_CLK_CPU_N
[15,62] SSD1_PEDET
[16,62] SSD1_CLK_CPU
[16,62] SSD1_CLK_CPU_N
[15] PCIE_TX_CON_P12
[15] PCIE_TX_CON_N12
[15] PCIE_RX_CPU_N12
[15] PCIE_RX_CPU_P12
[15] PCIE_TX_CON_P11
[15] PCIE_TX_CON_N11
[15] PCIE_RX_CPU_P11
[15] PCIE_RX_CPU_N11
[15] PCIE_TX_CON_P10
[15] PCIE_TX_CON_N10
[15] PCIE_RX_CPU_N10
[15] PCIE_RX_CPU_P10
[15] PCIE_TX_CON_P9
[15] PCIE_TX_CON_N9
[15] PCIE_RX_CPU_N9
[15] PCIE_RX_CPU_P9

3D3V_S0 — R6201 — 3D3V_MSATA1_S0
0R0805-PAD-1-GP-U

3D3V_MSATA1_S0
EC6205 DY SCD1U25V2KX-L-GP
RF6201 DY SCD1U25V2KX-L-GP
C6201 SCD1U16V2KX-L-GP
C6202 SCD1U16V2KX-L-GP
C6203 SC10U6D3V3MX-L-GP
C6204 SC10U6D3V3MX-L-GP
C6205 SC10U6D3V3MX-L-GP

EU6201
SSD1_SATA_TX_CON_P12 ↔ SSD1_SATA_TX_CON_P12
SSD1_SATA_TX_CON_N12 ↔ SSD1_SATA_TX_CON_N12
PCIE_RX_CPU_N12 ↔ PCIE_RX_CPU_N12
PCIE_RX_CPU_P12 ↔ PCIE_RX_CPU_P12
AZ1043-04F-R7G-GP

3D3V_MSATA1_S0 — R6204 1MR2F-L-GP — SSD1_PEDET

SSD1
3D3V_MSATA1_S0
NP2 76 74 72 70 68 — NP2 / 3_3V / 3_3V / 3_3V / SUSCLK(32KHZ)
NC#58 56 54 52 50 48 46 44 42 40 38 36 34 32 30 28 26 24 22 20 18 16 14 12 10 8 6 4 2
PCIE_WAKE# — R6203 0R0402-PAD-1-GP — SSD1_PCIE_WAKE# C
SSD1_CLKREQ_CPU_N — 0R0402-PAD-1-GP
PLT_RST# — R6205 0R0402-PAD-1-GP — SSD1_RST#
PEWAKE#/NC#54
CLKREQ#/NC#52
PERST#/NC#50
NC#48 NC#46 NC#44 NC#42 NC#40
DEVSLP1 — R6210 0R2J-L-GP DY — DEVSL_P1
DEVSLP
NC#36 NC#34 NC#32 NC#30 NC#28 NC#26 NC#24 NC#22 NC#20
3_3V 3_3V 3_3V 3_3V
TPAD14-OP-GP — TP18 — DAS/DSS2#
DAS/DSS#
NC#8 NC#6
3_3V 3_3V 3_3V
NP1 77 75 73 71 69 67 — NP1 / GND / GND / GND / PEDET(NC-PCIE/GND-SATA) / NC#67
SSD1_PEDET — SSD1_PEDET
GND 57 55 53 51 49 47 45 43 41 39 37 35 33 31 29 27 25 23 21 19 17 15 13 11 9 7 5 3 1
REFCLKP — SSD1_CLK_CPU
REFCLKN — SSD1_CLK_CPU_N
PETP0/SATA-A+ — SSD1_SATA_TX_CON_P12 — C6206 — SCD22U10V2KX-L1-GP — PCIE_TX_CON_P12
PETN0/SATA-A- — SSD1_SATA_TX_CON_N12 — C6207 — SCD22U10V2KX-L1-GP — PCIE_TX_CON_N12
PERP0/SATA-B- — PCIE_RX_CPU_N12
PERN0/SATA-B+ — PCIE_RX_CPU_P12
PETP1 — SSD1_PCIE_TX_CON_P11 — C6208 — SCD22U10V2KX-L1-GP — PCIE_TX_CON_P11
PETN1 — SSD1_PCIE_TX_CON_N11 — C6209 — SCD22U10V2KX-L1-GP — PCIE_TX_CON_N11
PERP1 — PCIE_RX_CPU_P11
PERN1 — PCIE_RX_CPU_N11
PETP2 — SSD1_PCIE_TX_CON_P10 — C6210 — SCD22U10V2KX-L1-GP — PCIE_TX_CON_P10
PETN2 — SSD1_PCIE_TX_CON_N10 — C6211 — SCD22U10V2KX-L1-GP — PCIE_TX_CON_N10
PERP2 — PCIE_RX_CPU_N10
PERN2 — PCIE_RX_CPU_P10
PETP3 — SSD1_PCIE_TX_CON_P9 — C6212 — SCD22U10V2KX-L1-GP — PCIE_TX_CON_P9
PETN3 — SSD1_PCIE_TX_CON_N9 — C6213 — SCD22U10V2KX-L1-GP — PCIE_TX_CON_N9
PERP3 — PCIE_RX_CPU_N9
PERN3 — PCIE_RX_CPU_P9
SKT-NGFF75P-145-GP

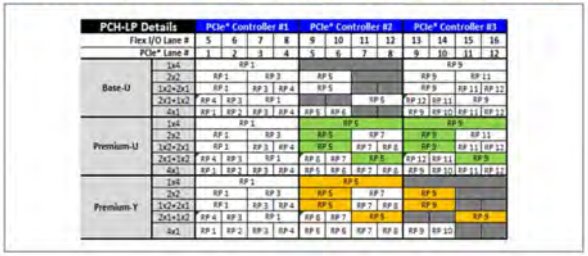
062.10003.0991
2nd = 062.10003.00A1

SSD1_PCIE_WAKE# C — EC6201 DY SC10P50V2JN-L1-GP
SSD1_RST# — ED6201 DY AZ5725-01FDR7G-GP

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:
1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer tChapter 3, "General Differential Signals Design Guidelines" " along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter



Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

DIS

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Title: **(Reserved)WWAN**
Size: Custom | Document Number: **Buzz_KBL** | Rev: **2**
Date: Friday, July 07, 2017 | Sheet 62 of 106

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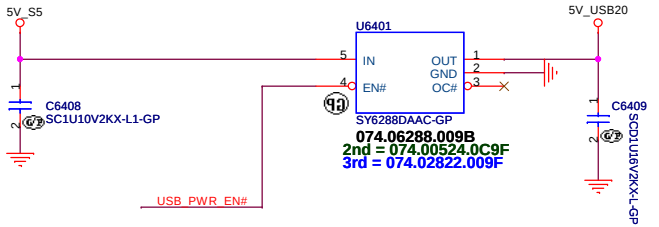
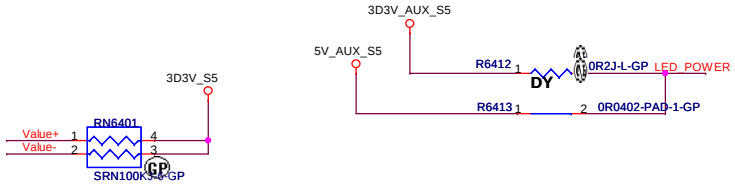
Title		
Size A4	Document Number **Buzz_KBL**	Rev **2**
Date: Friday, July 07, 2017	Sheet 63 of 106	

[24,89] STDBY_LED
[24,89] POWER_LED
[24,89] CHARGE_LED
[24,89] DC_BATFULL
[24] Value+
[24] Value-
[24] LID_CLOSE#
[24] LID_CLOSE2#
[15,89] USB3_USB20_N
[15,89] USB3_USB20_P
[15,89] CR_USB20_N
[15,89] CR_USB20_P
[43] BAT_RST
[24,68,89] KBC_PWRBTN#
[27,89] AUD_HP1_JACK_L2
[27,89] AUD_HP1_JACK_R2
[27,89] AUD_HP1_JD#
[27,89] RING2
[27,89] SELEEVE
[24,35] USB_PWR_EN#

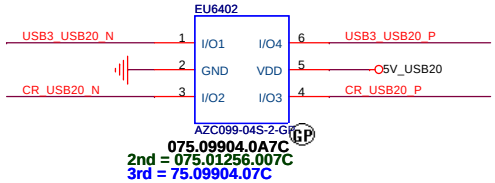
SSID = User.Interface

Low Active 2A

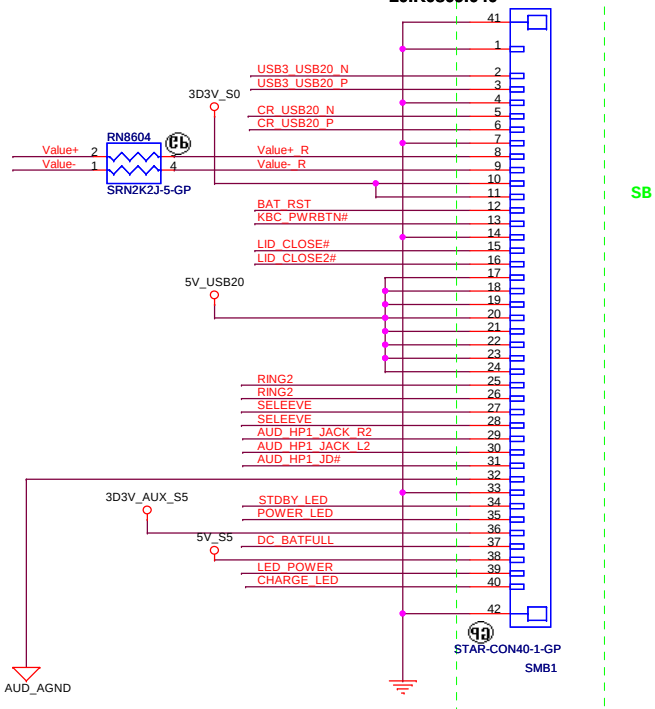




Close connector



2ND = 20.K0678.040
20.K0809.040



DIS

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Title: **LED Bard/Power Button**

Size	Document Number	Rev
Custom	Buzz_KBL	2

Date: Friday, July 07, 2017 Sheet 64 of 106

SSID = KBC

[24,89] KSI[0..7]
[24,89] KSO[0..17]
[24] EC_TPCLK
[24] EC_TPDATA
[24,89] FUN_OFF#
[89] EC_TP_CLK_C
[89] EC_TP_DATA_C
[89] I2C1_DATA_TP
[89] I2C1_CLK_TP
[89] TP_IN#_R
[24] PTP_PWR_EN#
[22] TP_IN#
[24] EC_TP_IN#
[6] PM_TP_CLK
[6] PM_TP_DATA
[24] KB_BL_PWM
[24] KB_BL_DET
[89] KB_LED_PWM_R
[89] KB_BL_DET_R

3D3V_TP_S3
3D3V_S0
RN6505
SRN2K2J-5-GP
Q6503
2N7002KDW-1-GP
PM_TP_CLK
PM_TP_DATA
I2C1_CLK_TP
I2C1_DATA_TP
EC6504
EC6505
DY
SCD1U16V2KX-L-GP
75.27002.E7C
2nd = 075.67002.007C
3rd = 075.063D1.007C

3D3V_TP_S3
3D3V_S0
R6506
100KR2F-L3-GP
Q6502
2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 84.2N702.031
TP_IN#
TP_IN#_R
EC_TP_IN#
R6513
0R0402-PAD-1-GP

3D3V_TP_S3
RN6503
SRN4K7J-8-GP
RN6502
SRN33J-5-GP-U
EC_TPCLK
EC_TPDATA
FUN_OFF#
TP_IN#_R
EC6507
SCD1U16V2KX-L-GP
DY

TOUCH PAD
3D3V_TP_S3
EC6502
SC22950V2JN-L-GP
EC6501
EC6503
SC15P50V2JN-3GP
EC_TP_CLK_C
EC_TP_DATA_C
I2C1_DATA_TP
I2C1_CLK_TP
TP_IN#_R
TP1
ST14CON8-3-GP
020.K0277.0008
2nd = 020.K0235.0008

3D3V_S5
U6502
SY6288DAAC-GP
PTP_PWR_EN#
IN
EN#
OUT
GND
OC#
C6509
SC4D7U6D3V3KX-L-GP
074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F
3D3V_TP_S3
C6504
SC4D7U6D3V3KX-L-GP

Internal KeyBoard Connector

KBBL1
PTWO-CON4-16-GP
KB_BL
20.K0397.004
2nd = 020.K0262.0004
KB_BL_DET_R
KB_BL_DET
KB_LED_PWM_R
R6504
100KR2F-L3-GP
KB_BL
R6502
200KR2F-L-3-GP
KB_BL
0R0402-PAD-1-GP
R6521
5V_S0
C6501
SCD1U16V2KX-L-GP
KB_LED_PWM_D
KB_BL
Q6501
2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 84.2N702.031
KB_BL_PWM
C6502
SCD1U16V2KX-L-GP

KB1
ACES-CON28-10-GP
020.K0173.0028
2nd = 020.K0266.0028
KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15 KSO16 KSO17

DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad
Size: Custom
Document Number: Buzz_KBL
Rev: 2
Date: Friday, July 07, 2017
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Title	***Reserved***	
Size A4	Document Number **Buzz_KBL**	Rev **2**
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Title: ***Reserved***

Size	Document Number	Rev
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[18,24,91] INT_SERIRQ
[18] LPC_CLK_DBG

[20,24,61,62,79,89,91] PLT_RST#
[18,24,91] LPC_FRAME#_CPU

[18,24,91] LPC_AD_CPU_P3
[18,24,91] LPC_AD_CPU_P2

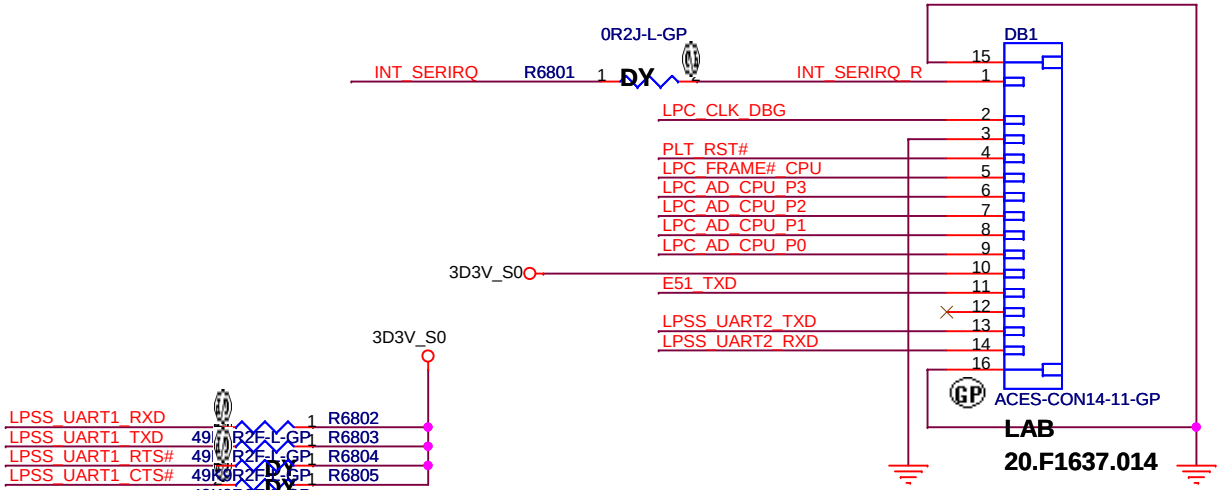
[18,24,91] LPC_AD_CPU_P1
[18,24,91] LPC_AD_CPU_P0

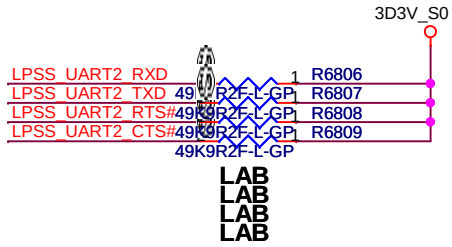
[24,61] E51_TXD

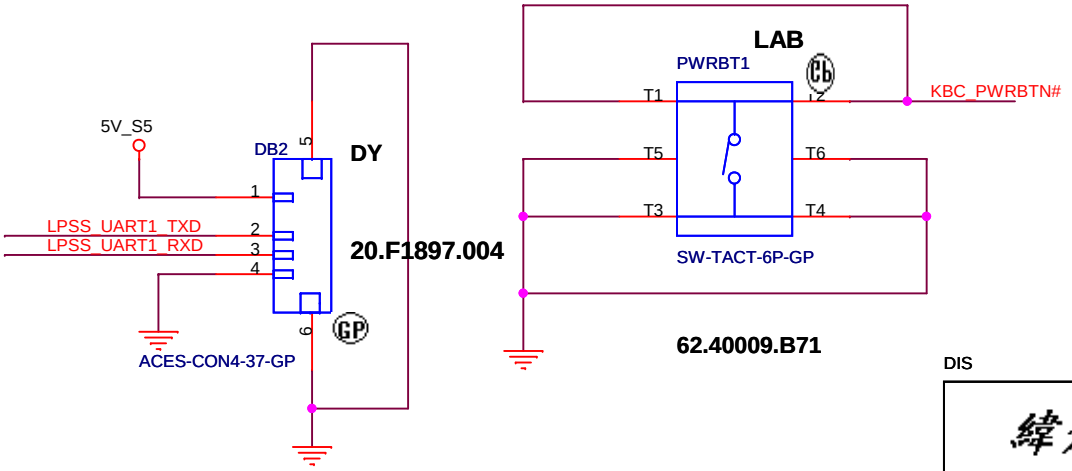
[6,68] LPSS_UART2_TXD
[6,68] LPSS_UART2_RXD

[24,64,89] KBC_PWRBTN#

[6] LPSS_UART1_RXD
[6] LPSS_UART1_TXD
[6] LPSS_UART1_RTS#
[6] LPSS_UART1_CTS#
[6,68] LPSS_UART2_RXD
[6,68] LPSS_UART2_TXD
[6] LPSS_UART2_RTS#
[6] LPSS_UART2_CTS#







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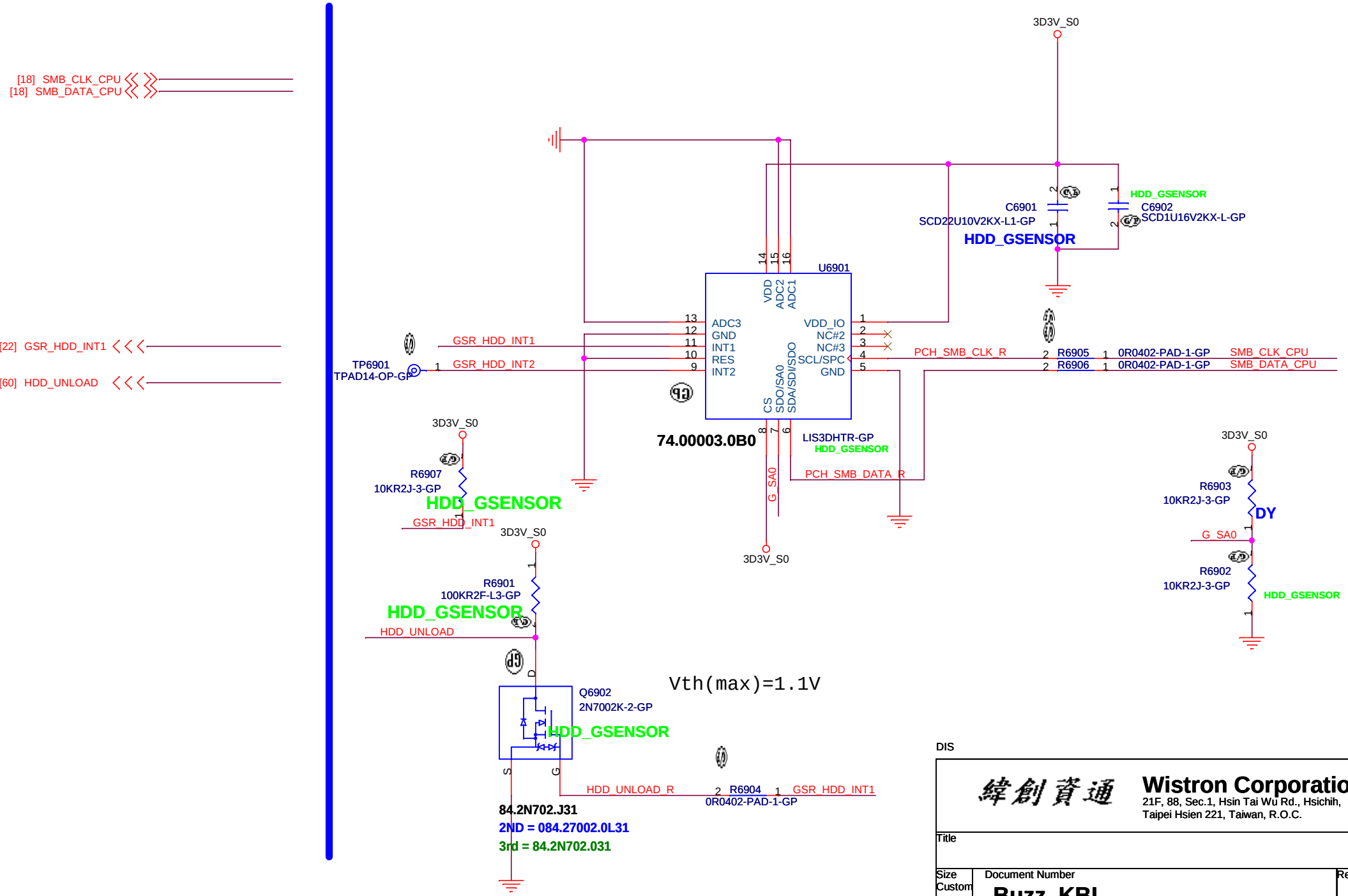
Title: Dubug connector

Size	Document Number	Rev
A4	Buzz_KBL	2

Date: Friday, July 07, 2017 Sheet 68 of 106


[18] SMB_CLK_CPU
[18] SMB_DATA_CPU
[22] GSR_HDD_INT1
[60] HDD_UNLOAD
3D3V_S0
C6901
SCD22U10V2KX-L1-GP
HDD_GSENSOR
C6902
SCD1U16V2KX-L-GP
U6901
VDD
ADC2
ADC1
ADC3
GND
INT1
RES
INT2
CS
SDO/SA0
SDA/SDI/SDO
VDD_IO
NC#2
NC#3
SCL/SPC
GND
GSR_HDD_INT1
GSR_HDD_INT2
TP6901
TPAD14-OP-GP
PCH_SMB_CLK_R
PCH_SMB_DATA_R
R6905
R6906
0R0402-PAD-1-GP
SMB_CLK_CPU
SMB_DATA_CPU
74.00003.0B0
LIS3DHTR-GP
HDD_GSENSOR
G_SA0
R6907
10KR2J-3-GP
R6903
DY
R6902
R6901
100KR2F-L3-GP
HDD_UNLOAD
Q6902
2N7002K-2-GP
Vth(max)=1.1V
HDD_UNLOAD_R
R6904
0R0402-PAD-1-GP
84.2N702.J31
2ND = 084.27002.0L31
3rd = 84.2N702.031
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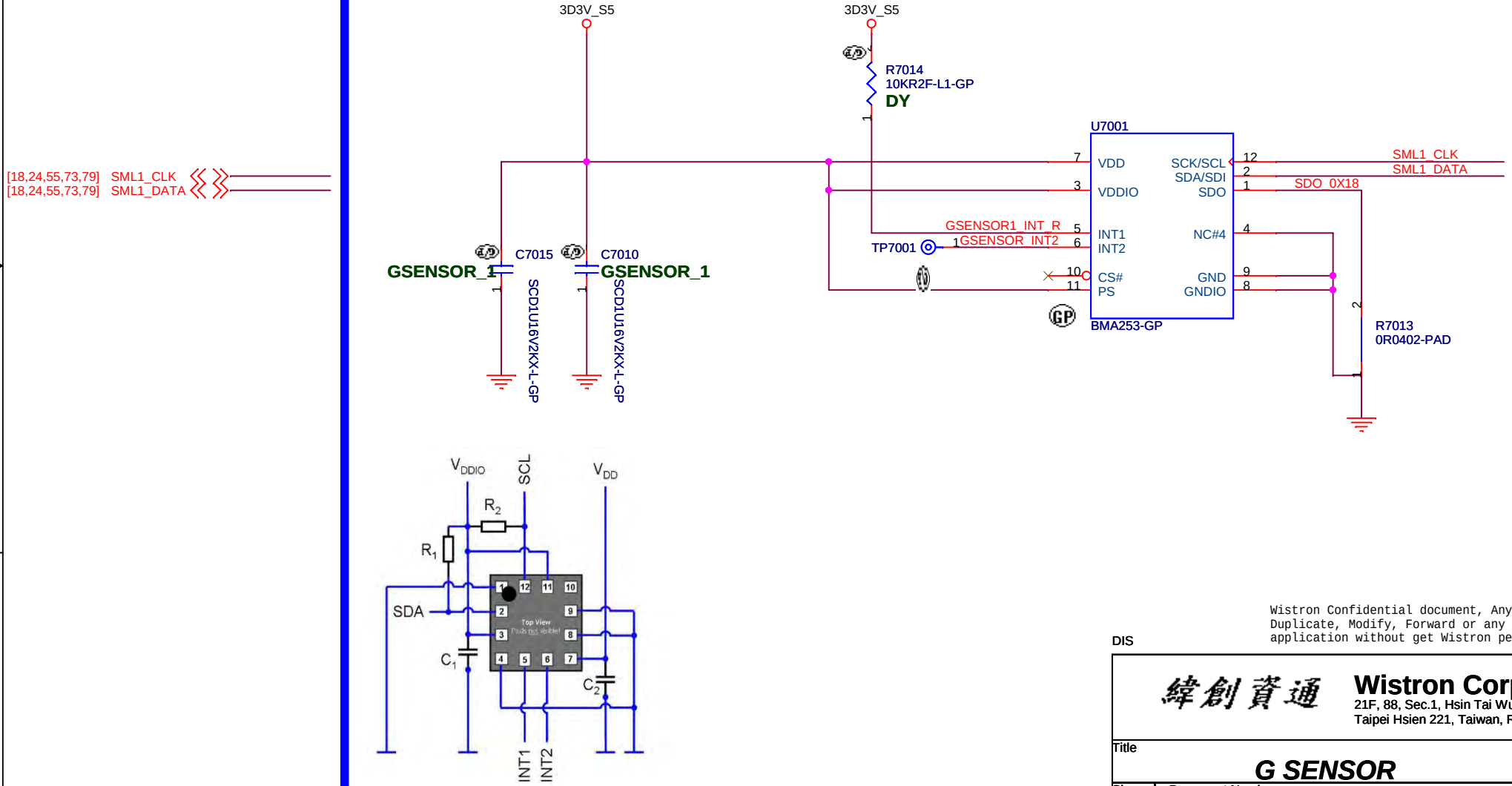
SSID = User.Interface

G Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

The default I²C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V_{DDIO}'.



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Title: G SENSOR

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Title: ***Thunderbolt (4/5)***

Size	Document Number	Rev
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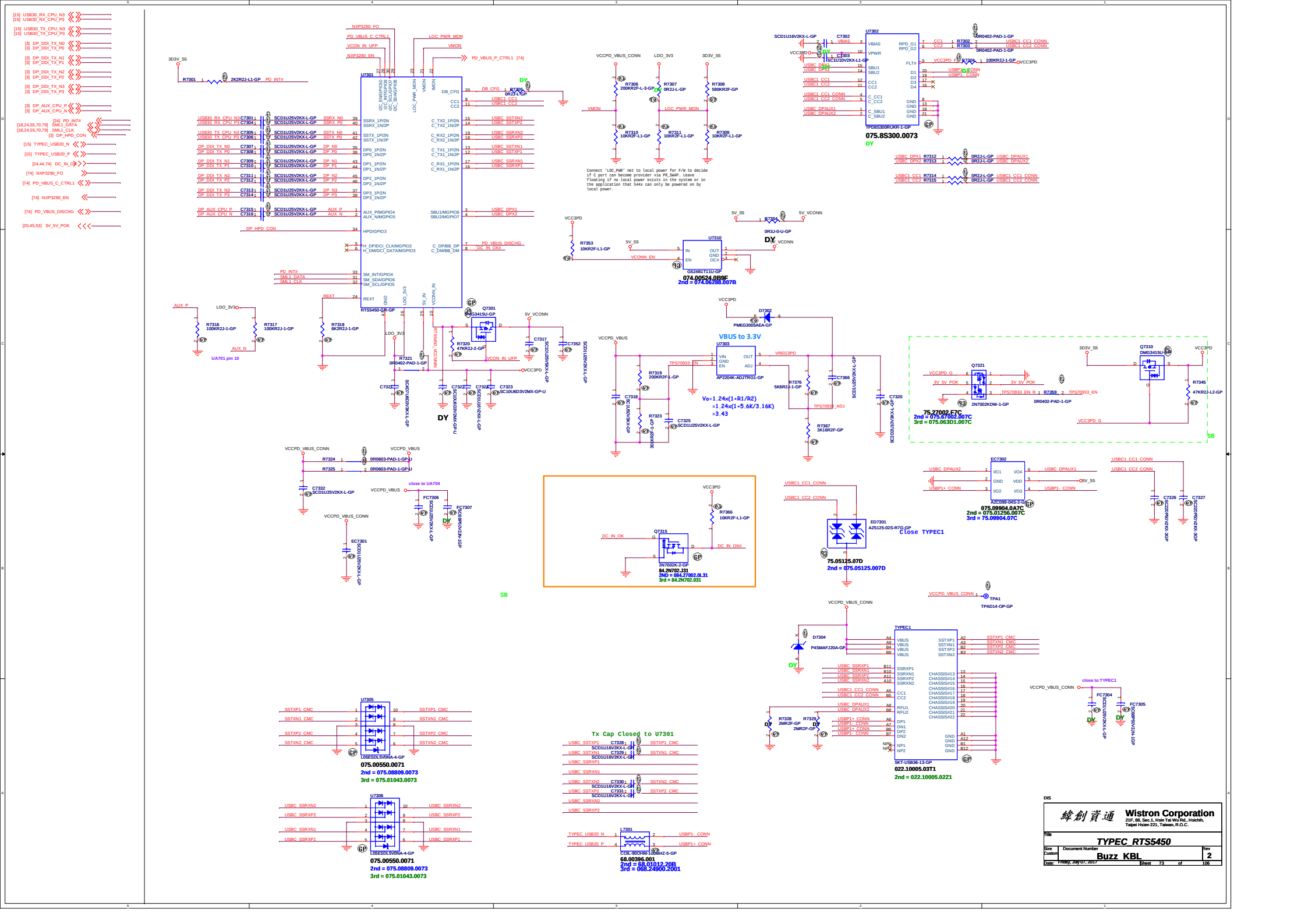
[15] USB30_RX_CPU_N3
[15] USB30_RX_CPU_P3
[15] USB30_TX_CPU_N3
[15] USB30_TX_CPU_P3
[3] DP_DDI_TX_N0
[3] DP_DDI_TX_P0
[3] DP_DDI_TX_N1
[3] DP_DDI_TX_P1
[3] DP_DDI_TX_N2
[3] DP_DDI_TX_P2
[3] DP_DDI_TX_N3
[3] DP_DDI_TX_P3
[3] DP_AUX_CPU_P
[3] DP_AUX_CPU_N
[18,24,55,70,79] SML1_DATA
[18,24,55,70,79] SML1_CLK
[24] PD_INT#
[3] DP_HPD_CON
[15] TYPEC_USB20_N
[15] TYPEC_USB20_P
[24,44,74] DC_IN_OK#
[74] NXP3290_FO
[74] PD_VBUS_C_CTRL1
[74] NXP3290_EN
[74] PD_VBUS_DISCHG
[20,45,53] 3V_5V_POK
NXP3290_FO
PD_VBUS_C_CTRL1
VCON_IN_UFP
NXP3290_EN
LOC_PWR_MON
VMON
PD_VBUS_P_CTRL1 [74]
3D3V_S5
R7301 2K2R2J-1-GP PD_INT#
U7301
RTS5450-GR-GP
DB_CFG
R7305 0R2J-1-GP
USB30_RX_CPU_N3 C7301 SCD1U25V2KX-L-GP SSRX_N0
USB30_RX_CPU_P3 C7304 SCD1U25V2KX-L-GP SSRX_P0
USB30_TX_CPU_N3 C7305 SCD1U25V2KX-L-GP SSTX_N0
USB30_TX_CPU_P3 C7306 SCD1U25V2KX-L-GP SSTX_P0
DP_DDI_TX_N0 C7307 SCD1U25V2KX-L-GP DP_N0
DP_DDI_TX_P0 C7308 SCD1U25V2KX-L-GP DP_P0
DP_DDI_TX_N1 C7309 SCD1U25V2KX-L-GP DP_N1
DP_DDI_TX_P1 C7310 SCD1U25V2KX-L-GP DP_P1
DP_DDI_TX_N2 C7311 SCD1U25V2KX-L-GP DP_N2
DP_DDI_TX_P2 C7312 SCD1U25V2KX-L-GP DP_P2
DP_DDI_TX_N3 C7313 SCD1U25V2KX-L-GP DP_N3
DP_DDI_TX_P3 C7314 SCD1U25V2KX-L-GP DP_P3
DP_AUX_CPU_P C7315 SCD1U25V2KX-L-GP AUX_P
DP_AUX_CPU_N C7316 SCD1U25V2KX-L-GP AUX_N
DP_HPD_CON
PD_INT#
SML1_DATA
SML1_CLK
SSRX_1P/2N
SSRX_1N/2P
SSTX_1P/2N
SSTX_1N/2P
DP0_1P/2N
DP0_1N/2P
DP1_1P/2N
DP1_1N/2P
DP2_1P/2N
DP2_1N/2P
DP3_1P/2N
DP3_1N/2P
AUX_P/MGPIO4
AUX_N/MGPIO5
HPD/GPIO3
H_DP/DCI_CLK/MGPIO2
H_DM/DCI_DATA/MGPIO3
SM_INT/GPIO4
SM_SDA/GPIO6
SM_SCL/GPIO5
REXT
C_TX2_1P/2N
C_TX2_1N/2P
C_RX2_1P/2N
C_RX2_1N/2P
C_TX1_1P/2N
C_TX1_1N/2P
C_RX1_1P/2N
C_RX1_1N/2P
SBU1/MGPIO6
SBU2/MGPIO7
C_DP/BB_DP
C_DM/BB_DM
USBC_SSTXN2
USBC_SSTXP2
USBC_SSRXN2
USBC_SSRXP2
USBC_SSTXN1
USBC_SSTXP1
USBC_SSRXN1
USBC_SSRXP1
USBC_DPX1
USBC_DPX2
PD_VBUS_DISCHG
DC_IN_OK#
VCCPD_VBUS_CONN
LDO_3V3
5V_S5
R7306 200KR2F-L-3-GP
R7307 0R2J-L-GP
R7308 590KR2F-GP
R7310 10KR2F-L1-GP
R7311 10KR2F-L1-GP
R7309 10KR2F-L1-GP
Connect 'LOC_PWR' net to local power for F/W to decide if C port can become provider via PR_SWAP. Leave floating if no local power exists in the system or in the application that 544x can only be powered on by local power.
SCD1U16V2KX-L-GP
C7302 VBIAS
VCC3PD
C7303 SC1U10V2KX-L1-GP
U7302
TPD8S300RUKR-1-GP
VBIAS
VPWR
RPD_G1
RPD_G2
SBU1
SBU2
CC1
CC2
C_CC1
C_CC2
C_SBU1
C_SBU2
FLT#
D1
D2
D3
D4
GND
075.8S300.0073
DY
R0R402-PAD-1-GP
USBC1_CC1_CONN
USBC1_CC2_CONN
R7302 0R2J-L-GP USBC_DPAUX1
R7303 0R2J-L-GP USBC_DPAUX2
R7312 0R2J-L-GP USBC_DPAUX1
R7313 0R2J-L-GP USBC_DPAUX2
R7314 0R2J-L-GP USBC1_CC1_CONN
R7315 0R2J-L-GP USBC1_CC2_CONN
USBP1+_CONN
USBP1-_CONN
VCC3PD
R7353 10KR2F-L1-GP
5V_S5
VCONN_EN
U7310
G524B1T11U-GP
074.00524.0B9F
2nd = 074.00288.007B
R7354
0R3J-0-U-GP
5V_VCONN
AUX_P
AUX_N
LDO_3V3
R7316 100KR2J-1-GP
R7317 100KR2J-1-GP
UA701 pin 10
R7318 6K2R2J-1-GP
REXT
R7321 0R0402-PAD-1-GP
Q7301 G3415U-GP
R7320 47KR2J-2-GP
VCON_IN_UFP
C7317 SCD1U25V2KX-L-GP
C7352 SCD1U25V2KX-L-GP
C7322 SCD1U25V2KX-L-GP
C7323 SC10U6D3V2MX-GP-U
DY
VCCPD_VBUS
VBUS to 3.3V
D7302 PMEG3005AEA-GP
U7303
AP2204K-ADJTRG1-GP
VIN
VOUT
EN
ADJ
VREG3PD
TPS70933_EN
TPS70933_ADJ
R7319 200KR2F-L-GP
R7323 30K1R2F-L-GP
R7376 5K6R2J-1-GP
R7367 3K16R2F-GP
C7318 SC1U10V2KX-GP
C7325 SCD1U25V2KX-L-GP
C7366 SCD1U25V2KX-L-GP
C7320 SC22U10V5MX-GP
Vo=1.24x(1+R1/R2)
=1.24x(1+5.6K/3.16K)
=3.43
Q7321 2N7002KDW-1-GP
VCC3PD_G
3V_5V_POK
TPS70933_EN_R
R7359 0R0402-PAD-1-GP
Q7310 DMG3415U
R7345 47KR2J-L2-GP
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.063D1.007C
SB
VCCPD_VBUS_CONN
R7324 0R0603-PAD-1-GP-U
R7325 0R0603-PAD-1-GP-U
C7332 SCD1U25V2KX-L-GP
close to UA704
FC7306 SCD1U25V2KX-L-GP
FC7307 SC820P50V2KX-1GP
EC7301 SCD1U16V2KX-L-GP
Q7315 2N7002K-2-GP
R7366 10KR2F-L1-GP
DC_IN_OK
DC_IN_OK#
84.2N702.J31
2ND = 084.27002.0L31
3rd = 84.2N702.031
SB
EC7302 AZC099-04S-2-GP
USBC_DPAUX2
USBC_DPAUX1
USBP1+_CONN
USBP1-_CONN
5V_S5
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C
C7326 SC220P50V2KX-3GP
C7327 SC220P50V2KX-3GP
ED7301 AZ5125-02S-R7G-GP
Close TYPEC1
75.05125.07D
2nd = 075.05125.007D
TPA1 TPAD14-OP-GP
D7304 P4SMAFJ20A-GP
TYPEC1
SKT-USB36-13-GP
SSTXP1
SSTXN1
SSTXP2
SSTXN2
SSRXP1
SSRXN1
SSRXP2
SSRXN2
CC1
CC2
RFU1
RFU2
DP1
DN1
DP2
DN2
NP1
NP2
CHASSIS#13
CHASSIS#14
CHASSIS#15
CHASSIS#16
CHASSIS#17
CHASSIS#18
CHASSIS#19
CHASSIS#20
CHASSIS#21
CHASSIS#22
R7328 2MR2F-GP
R7329 2MR2F-GP
022.10005.03T1
2nd = 022.10005.02Z1
FC7304 SCD1U25V2KX-L-GP
FC7305 SC820P50V2KX-1GP
close to TYPEC1
U7305
L05ESDL5V0NA-4-GP
SSTXP1_CMC
SSTXN1_CMC
SSTXP2_CMC
SSTXN2_CMC
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073
U7306
L05ESDL5V0NA-4-GP
USBC_SSRXN2
USBC_SSRXP2
USBC_SSRXN1
USBC_SSRXP1
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073
Tx Cap Closed to U7301
C7328 SCD1U16V2KX-L-GP
C7329 SCD1U16V2KX-L-GP
C7330 SCD1U16V2KX-L-GP
C7331 SCD1U16V2KX-L-GP
L7301 COIL-90OHM-100MHZ-5-GP
TYPEC_USB20_N
TYPEC_USB20_P
USBP1-_CONN
USBP1+_CONN
68.00396.001
2nd = 68.01012.20B
3rd = 068.24900.2001
DIS
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TYPEC_RTS5450
Size
Custom
Document Number
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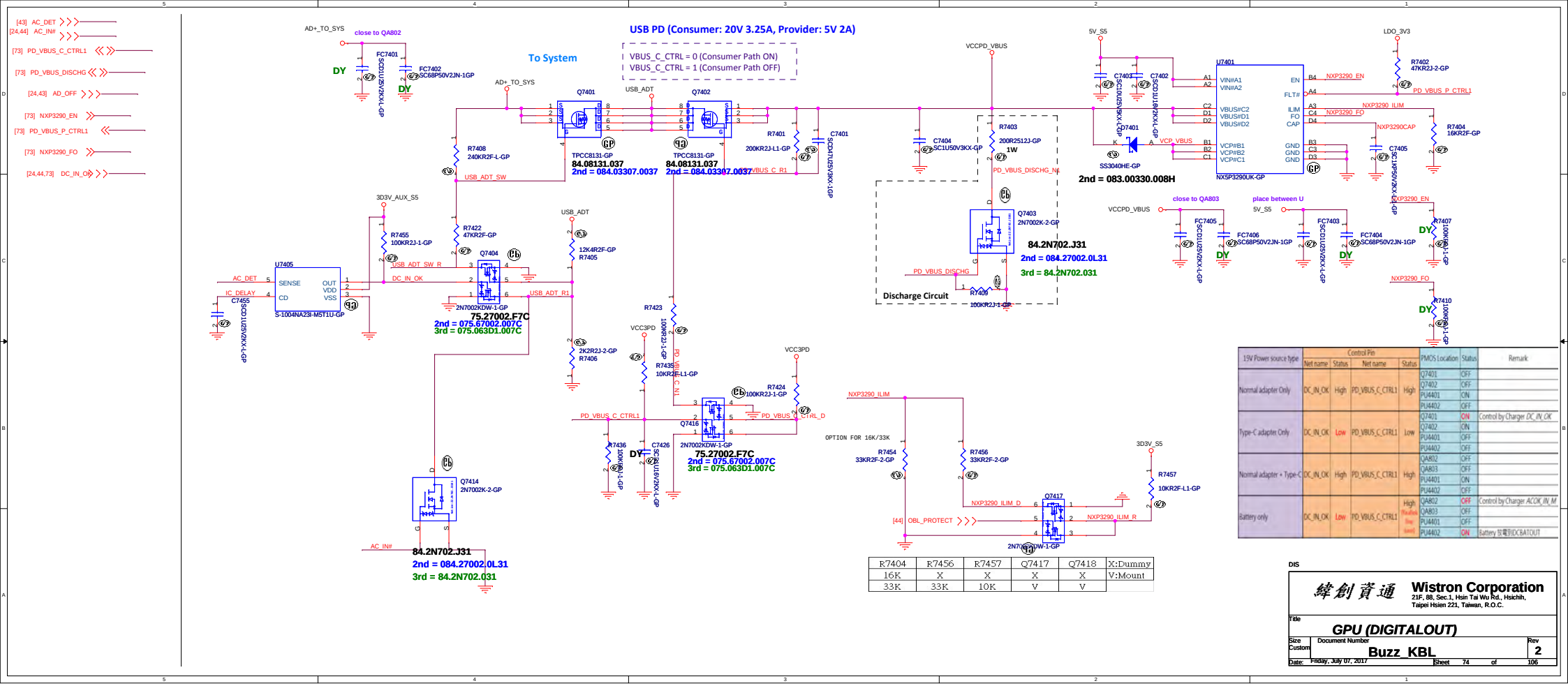

19V Power source type	Control Pin				PMOS Location	Status	Remark
	Net name	Status	Net name	Status			
Normal adapter Only	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4401	ON	
					PU4402	OFF	
Type-C adapter Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	Low	Q7401	ON	Control by Charger DC_IN_OK
					Q7402	ON	
					PU4401	OFF	
					PU4402	OFF	
Normal adapter + Type-C	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	QA802	OFF	
					QA803	OFF	
					PU4401	ON	
					PU4402	OFF	
Battery only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	High (Realtek low level)	QA802	OFF	Control by Charger ACOK_IN_M
					QA803	OFF	
					PU4401	OFF	
					PU4402	ON	Battery 放電到DCBATOUT

R7404	R7456	R7457	Q7417	Q7418	X:Dummy
16K	X	X	X	X	V:Mount
33K	33K	10K	V	V	

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Title: GPU (DIGITALOUT)

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***GPU (VRAM I/F)***

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- PEX_HVDD and PEX_PLL_HVDD rails must be shared with 1V8_AON for GC6 2.1

[24,85,86,88] DGPU_PWROK
[16] PEG_CLKREQ_CPU#
[79] VGA_RST#
[16] PEG_CLK_CPU
[16] PEG_CLK_CPU#
[15] GFX_PCIE_RX_P3
[15] GFX_PCIE_RX_N3
[15] GFX_PCIE_RX_P2
[15] GFX_PCIE_RX_N2
[15] GFX_PCIE_RX_P1
[15] GFX_PCIE_RX_N1
[15] GFX_PCIE_RX_P0
[15] GFX_PCIE_RX_N0
[15] GFX_PCIE_TX_CON_P3
[15] GFX_PCIE_TX_CON_N3
[15] GFX_PCIE_TX_CON_P2
[15] GFX_PCIE_TX_CON_N2
[15] GFX_PCIE_TX_CON_P1
[15] GFX_PCIE_TX_CON_N1
[15] GFX_PCIE_TX_CON_P0
[15] GFX_PCIE_TX_CON_N0

1D8V_3D3V_AON_S0
R7604 10KR2J-L-GP Muxless
DGPU_PWROK
Q7601 PJA138KA-GP
084.00138.0A31
2nd = 84.05067.031
Muxless
PEG_CLKREQ_CPU#
PEG_CLKREQ_dGPU#
VGA_RST#
PEG_CLK_CPU
PEG_CLK_CPU#

GFX_PCIE_RX_P0 / GFX_PCIE_RX_N0 — C7601 / C7606 — SCD22U10V2KX-L1-GP Muxless — GFX_PCIE_RX_CON_P0 / GFX_PCIE_RX_CON_N0
GFX_PCIE_TX_CON_P0 / GFX_PCIE_TX_CON_N0
GFX_PCIE_RX_P1 / GFX_PCIE_RX_N1 — C7607 / C7608 — SCD22U10V2KX-L1-GP Muxless — GFX_PCIE_RX_CON_P1 / GFX_PCIE_RX_CON_N1
GFX_PCIE_TX_CON_P1 / GFX_PCIE_TX_CON_N1
GFX_PCIE_RX_P2 / GFX_PCIE_RX_N2 — C7613 / C7614 — SCD22U10V2KX-L1-GP Muxless — GFX_PCIE_RX_CON_P2 / GFX_PCIE_RX_CON_N2
GFX_PCIE_TX_CON_P2 / GFX_PCIE_TX_CON_N2
GFX_PCIE_RX_P3 / GFX_PCIE_RX_N3 — C7615 / C7616 — SCD22U10V2KX-L1-GP Muxless — GFX_PCIE_RX_CON_P3 / GFX_PCIE_RX_CON_N3
GFX_PCIE_TX_CON_P3 / GFX_PCIE_TX_CON_N3

EMI Reserved
VGA_RST#
EC7601 SC33P50V2JN-3GP DY

VGA1A 1 0F 17
1/17 PCI_EXPRESS
N17P-G1-A1-GP Muxless

AJ12	PEX_RST#	
AK12	PEX_CLKREQ#	
AL13	PEX_REFCLK	
AK13	PEX_REFCLK#	
AK14	PEX_TX0	GFX_PCIE_RX_CON_P0
AJ14	PEX_TX0#	GFX_PCIE_RX_CON_N0
AN12	PEX_RX0	GFX_PCIE_TX_CON_P0
AM12	PEX_RX0#	GFX_PCIE_TX_CON_N0
AH14	PEX_TX1	GFX_PCIE_RX_CON_P1
AG14	PEX_TX1#	GFX_PCIE_RX_CON_N1
AN14	PEX_RX1	GFX_PCIE_TX_CON_P1
AM14	PEX_RX1#	GFX_PCIE_TX_CON_N1
AK15	PEX_TX2	GFX_PCIE_RX_CON_P2
AJ15	PEX_TX2#	GFX_PCIE_RX_CON_N2
AP14	PEX_RX2	GFX_PCIE_TX_CON_P2
AP15	PEX_RX2#	GFX_PCIE_TX_CON_N2
AL16	PEX_TX3	GFX_PCIE_RX_CON_P3
AK16	PEX_TX3#	GFX_PCIE_RX_CON_N3
AN15	PEX_RX3	GFX_PCIE_TX_CON_P3
AM15	PEX_RX3#	GFX_PCIE_TX_CON_N3
AK17	PEX_TX4	
AJ17	PEX_TX4#	
AN17	PEX_RX4	
AM17	PEX_RX4#	
AH17	PEX_TX5	
AG17	PEX_TX5#	
AP17	PEX_RX5	
AP18	PEX_RX5#	
AK18	PEX_TX6	
AJ18	PEX_TX6#	
AN18	PEX_RX6	
AM18	PEX_RX6#	
AL19	PEX_TX7	
AK19	PEX_TX7#	
AN20	PEX_RX7	
AM20	PEX_RX7#	
AK20	PEX_TX8	
AJ20	PEX_TX8#	
AP20	PEX_RX8	
AP21	PEX_RX8#	
AH20	PEX_TX9	
AG20	PEX_TX9#	
AN21	PEX_RX9	
AM21	PEX_RX9#	
AK21	PEX_TX10	
AJ21	PEX_TX10#	
AN23	PEX_RX10	
AM23	PEX_RX10#	
AL22	PEX_TX11	
AK22	PEX_TX11#	
AP23	PEX_RX11	
AP24	PEX_RX11#	
AK23	PEX_TX12	
AJ23	PEX_TX12#	
AN24	PEX_RX12	
AM24	PEX_RX12#	
AH23	PEX_TX13	
AG23	PEX_TX13#	
AN26	PEX_RX13	
AM26	PEX_RX13#	
AK24	PEX_TX14	
AJ24	PEX_TX14#	
AP26	PEX_RX14	
AP27	PEX_RX14#	
AL25	PEX_TX15	
AK25	PEX_TX15#	
AN27	PEX_RX15	
AM27	PEX_RX15#	

PCIE/PLL DIGITAL PWR
1V Interface

PEX_DVDD_1	AG19
PEX_DVDD_2	AG21
PEX_DVDD_3	AG22
PEX_DVDD_4	AG24
PEX_DVDD_5	AH21
PEX_DVDD_6	AH25

PCIE/PLL ANALOG PWR
1.8V Interface

PEX_HVDD_1	AG13
PEX_HVDD_2	AG15
PEX_HVDD_3	AG16
PEX_HVDD_4	AG18
PEX_HVDD_5	AG25
PEX_HVDD_6	AH15
PEX_HVDD_7	AH18
PEX_HVDD_8	AH26
PEX_HVDD_9	AH27
PEX_HVDD_10	AJ27
PEX_HVDD_11	AK27
PEX_HVDD_12	AL27
PEX_HVDD_13	AM28
PEX_HVDD_14	AN28
PEX_PLL_HVDD	AH12
PEX_TERMP	AP29

1V_1D05V_VGA_S0
1D8V_1D05_VGA_S0
Place under GPU
Place near GPU
Midway between GPU and VR
1D8V_VGA_3D3V_AON_S0
Place Under GPU
PEX_TERMP — R7607 2K49R2F-2-L-GP Muxless
R7607 Close to GPU

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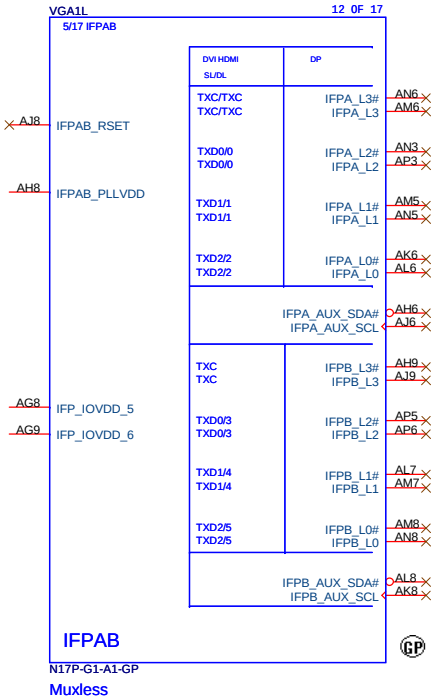
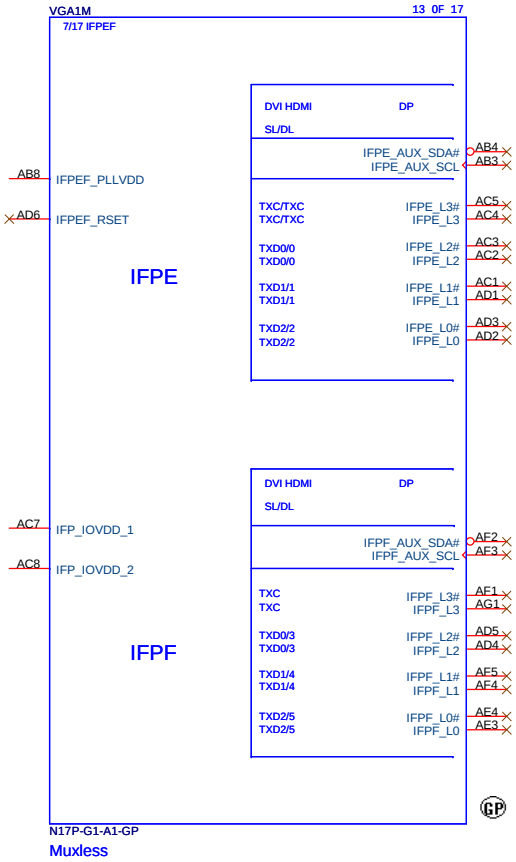
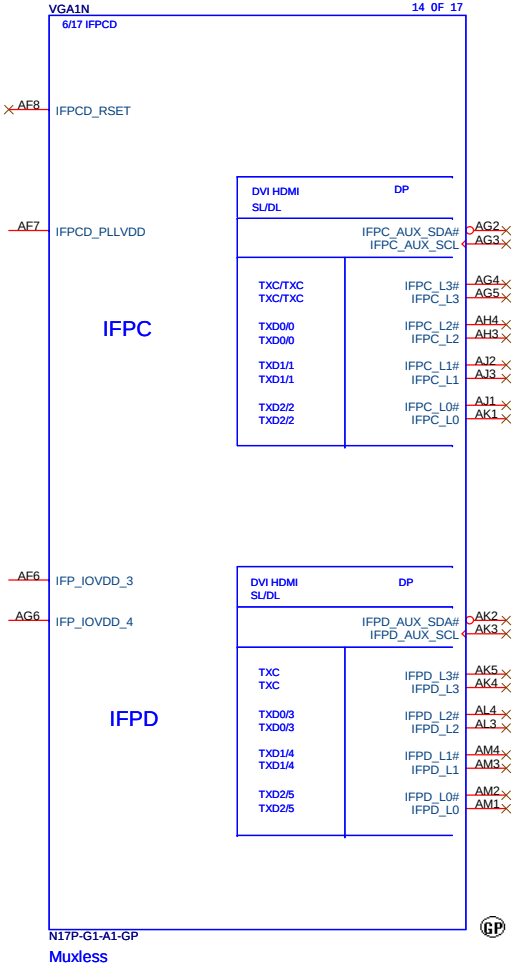
Title: GPU_840M_PEG (1/5)
Size: Custom | Document Number: Buzz_KBL | Rev: 2
Date: Friday, July 07, 2017 | Sheet 76 of 106







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Title	***VGA Power A***	
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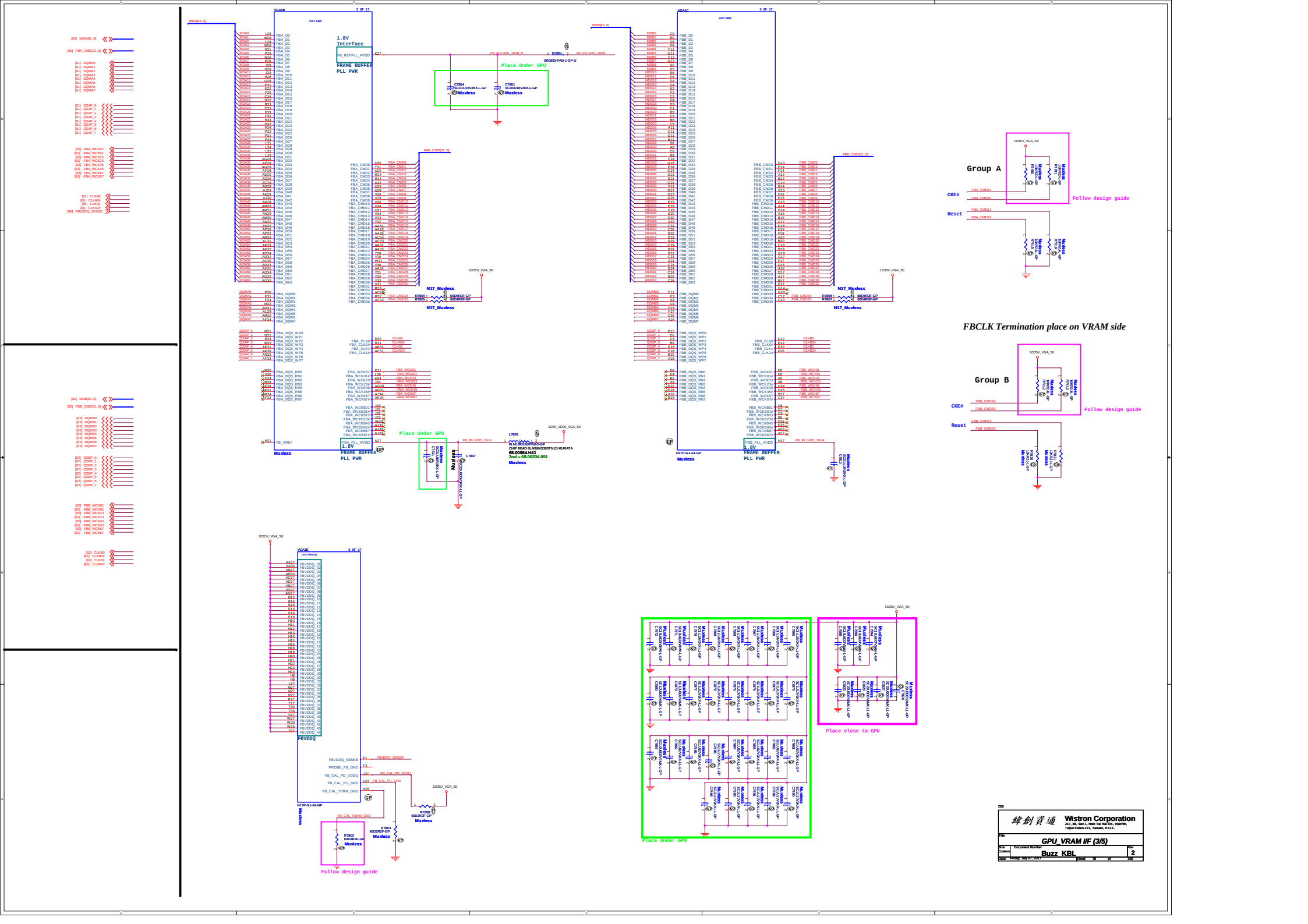
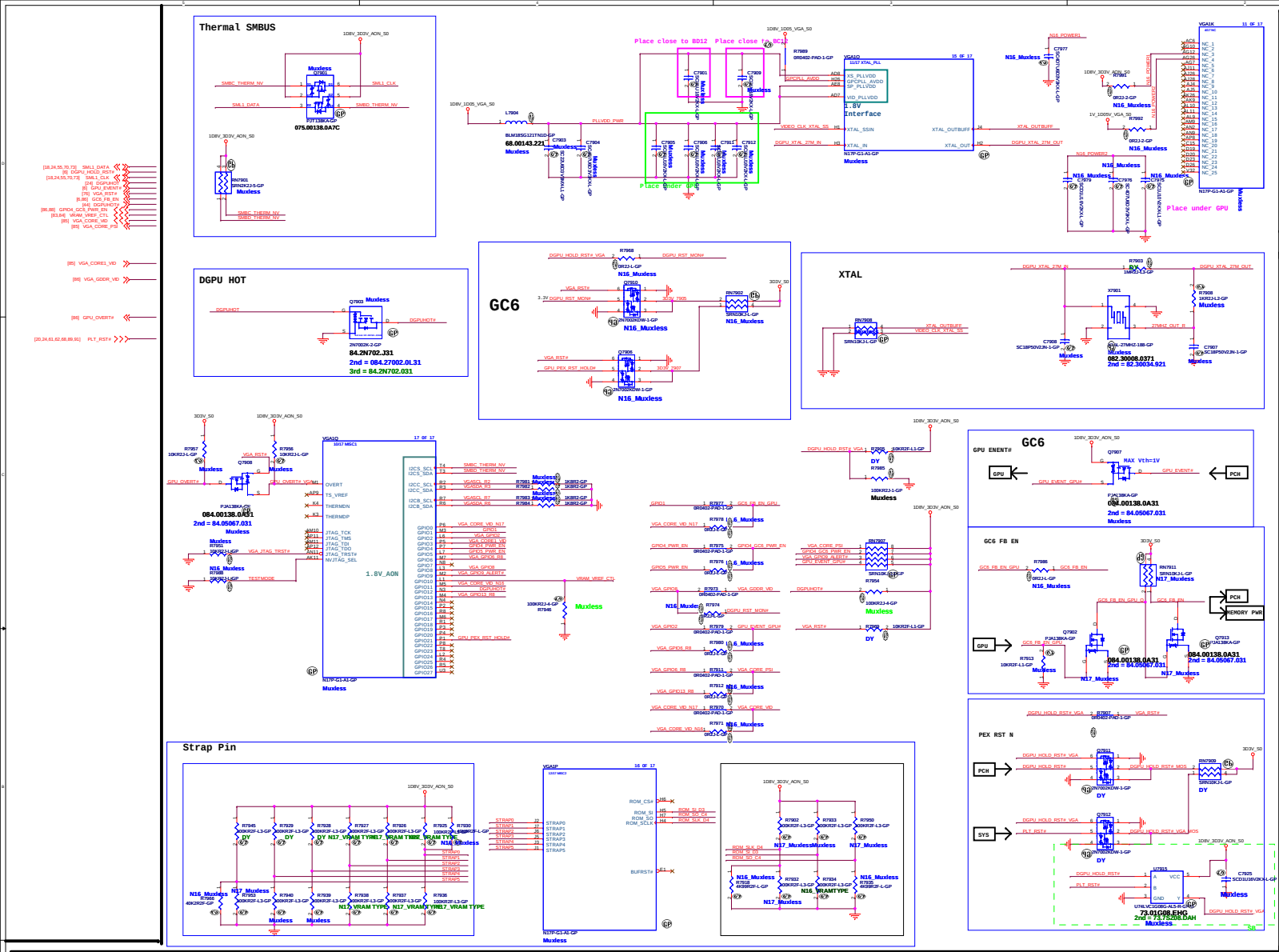

VGA1B
2 OF 17
3/17 FBA
1.8V Interface
FRAME BUFFER PLL PWR
Place Under GPU
VGA1C
3 OF 17
3/17 FBB
FBCLK Termination place on VRAM side
Group A
Group B
CKE#
Reset
Follow design guide
VGA1E
5 OF 17
Place close to GPU
Wistron Corporation
GPU_VRAM I/F (3/5)
Buzz_KBL



STRAP0	STRAP1	STRAP2	Vendor PN
L	L	L	Samsung K4G80325FB-HC28
H	L	L	Micron MT51J256M32HF-70:A
L	H	L	Hynix H5GC8H24MJR-R0C

N17P_VRAM_MATRIX

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDDQ	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Abbrv.	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24MJR-R0C	M-die	0x3	7 Gbps	N/A	Full	Production candidate
4 Gb	128Mx32	1.35V and 1.5V	Samsung	K4G41325FE-HC28	E-die	0x4	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.5V	Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V	Micron	EDH4032BAEJ-70:A	A-die	0x8	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V								Post production candidate

STRAP3	STRAP4	STRAP5	Function
L	L	L	as below picture

ROM_SLK	ROM_SI	ROM_SO	Function
M(0.9V)	L	L	as below picture

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

GDDR5 Device	STRAP0		STRAP1		STRAP2	
	R7925	R7936	R7926	R7937	R7927	R7938
Samsung K4G80325FB-HC28	NA	100K	NA	100K	NA	100K
Micron MT51J256M32HF-70:A	100K	NA	NA	100K	NA	100K
Hynix H5GC8H24MJR-R0C	NA	100K	100K	NA	NA	100K

STRAP0	STRAP1	STRAP2	Vendor PN
L	L	L	Samsung K4G80325FB-HC28
H	L	L	Micron MT51J256M32HF-70:A
L	H	L	Hynix H5GC8H24MJR-R0C

Function	STRAP3		STRAP4		STRAP5	
	R7928	R7939	R7929	R7940	R7945	R7953
SMB ALT ADDR DEVID_SEL PCIE CFG VGA DEVICE	NA	100K	NA	100K	NA	100K

STRAP3	STRAP4	STRAP5	Function
L	L	L	as Table 5.6

Function	ROM_SLK_D5		ROM_SI_D4		ROM_SO_C5	
	R7903	R7933	R7934	R7935	R7951	R7936
SORX_EXPOSED	100K	100K	NA	100K	NA	100K

Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010 Hynix 4G
20.0 k	1011	0011 Samsung 4G
24.9 k	1100	0100 Hynix 2G
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

Hynix 4G/Samsung 2G
Samsung 4G
Hynix 2G

4.99Kohm 64.49915.6DL
10Kohm 64.10025.L0L
15Kohm 64.15025.6DL
20Kohm 64.20025.6DL
24.9Kohm 64.24925.6DL
30.1Kohm 64.30125.6DL
34.8Kohm 64.34825.6DL
45Kohm 64.45325.6DL

N16P_VRAM_MATRIX

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Title	VGA Power A
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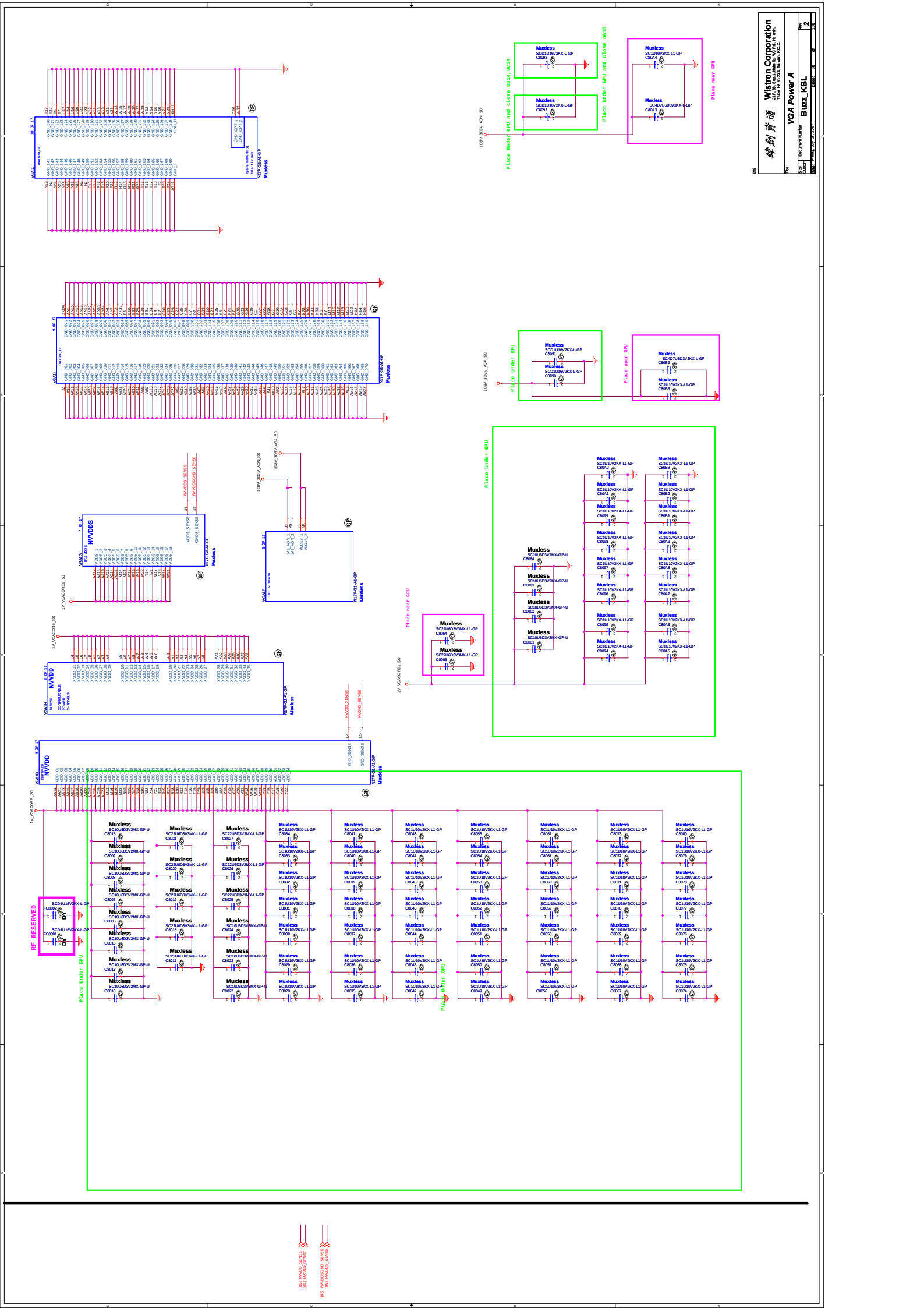
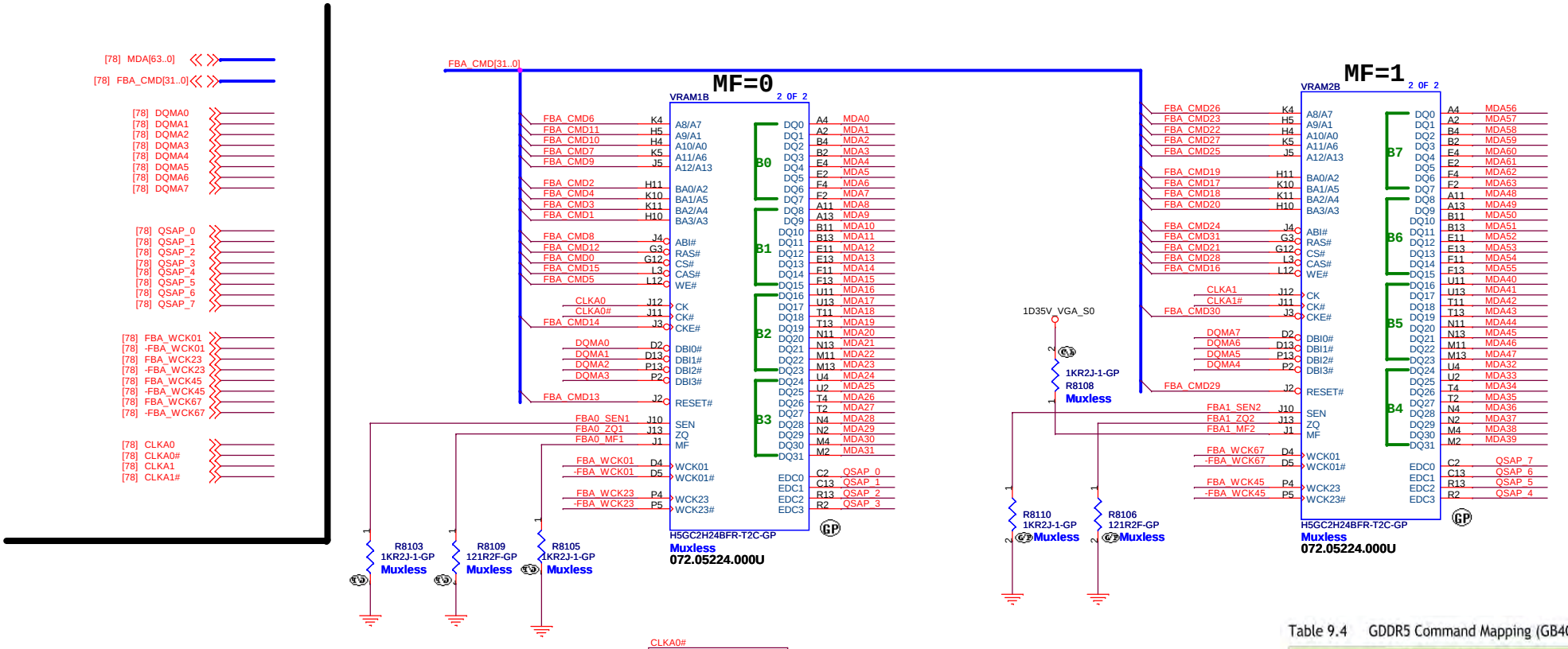

Wistron Corporation
VGA Power A
Buzz_KBL
RF RESERVED
Place Under GPU
Place near GPU
Muxless



GDDR5 Data Mapping

BYTE0 (BYTE4)		BYTE1 (BYTE5)		BYTE2 (BYTE6)		BYTE3 (BYTE7)	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24 (DQ32)	DQ8	DQ16 (DQ40)	DQ16	DQ8 (DQ48)	DQ24	DQ0 (DQ56)
DQ1	DQ25 (DQ33)	DQ9	DQ17 (DQ41)	DQ17	DQ9 (DQ49)	DQ25	DQ1 (DQ57)
DQ2	DQ26 (DQ34)	DQ10	DQ18 (DQ42)	DQ18	DQ10 (DQ50)	DQ26	DQ2 (DQ58)
DQ3	DQ27 (DQ35)	DQ11	DQ19 (DQ43)	DQ19	DQ11 (DQ51)	DQ27	DQ3 (DQ59)
DQ4	DQ28 (DQ36)	DQ12	DQ20 (DQ44)	DQ20	DQ12 (DQ52)	DQ28	DQ4 (DQ60)
DQ5	DQ29 (DQ37)	DQ13	DQ21 (DQ45)	DQ21	DQ13 (DQ53)	DQ29	DQ5 (DQ61)
DQ6	DQ30 (DQ38)	DQ14	DQ22 (DQ46)	DQ22	DQ14 (DQ54)	DQ30	DQ6 (DQ62)
DQ7	DQ31 (DQ39)	DQ15	DQ23 (DQ47)	DQ23	DQ15 (DQ55)	DQ31	DQ7 (DQ63)
DBI0	DBI3 (DBI4)	DBI1	DBI2 (DBI5)	DBI2	DBI1 (DBI6)	DBI3	DBI0 (DBI7)
EDC0	EDC3 (EDC4)	EDC1	EDC2 (EDC5)	EDC2	EDC1 (EDC6)	EDC3	EDC0 (EDC7)

GDDR5 CLK Mapping

WCK01	WCK23 (WCK45)		WCK23	WCK01 (WCK67)	
WCK01#	WCK23# (WCK45#)		WCK23#	WCK01# (WCK67#)	
CK	CK				
CK#	CK#				

Others

MF	MF	SEN	SEN
ZQ	ZQ	RESET#	RESET#

Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

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Title	VRAM 1,2 (1/4)	
Size: Custom	Document Number: Buzz_KBL	Rev: 2
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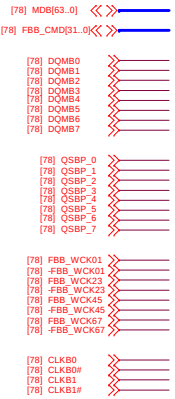

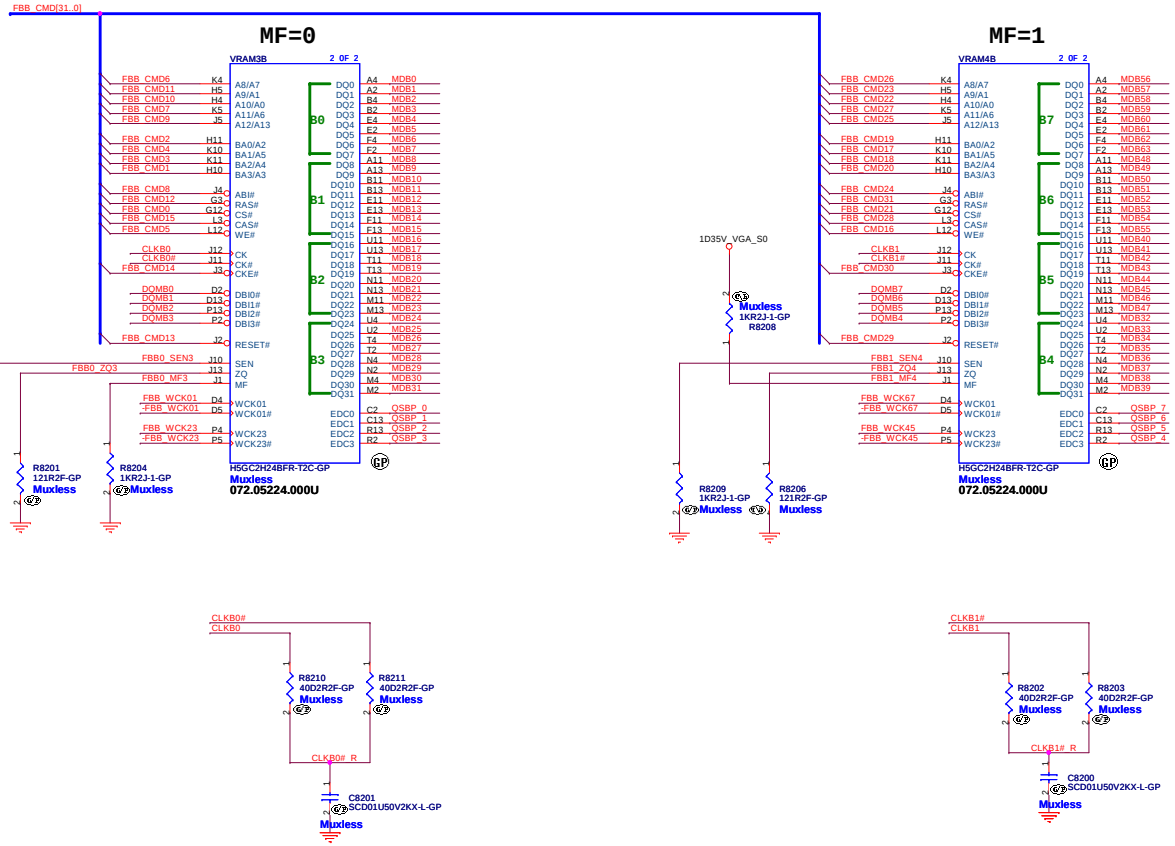

GDDR5 Data Mapping							
BYTE0 (BYTE4)		BYTE1 (BYTE5)		BYTE2 (BYTE6)		BYTE3 (BYTE7)	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24 (DQ32)	DQ8	DQ16 (DQ40)	DQ16	DQ8 (DQ48)	DQ24	DQ0 (DQ56)
DQ1	DQ25 (DQ33)	DQ9	DQ17 (DQ41)	DQ17	DQ9 (DQ49)	DQ25	DQ1 (DQ57)
DQ2	DQ26 (DQ34)	DQ10	DQ18 (DQ42)	DQ18	DQ10 (DQS0)	DQ26	DQ2 (DQ58)
DQ3	DQ27 (DQ35)	DQ11	DQ19 (DQ43)	DQ19	DQ11 (DQ51)	DQ27	DQ3 (DQ59)
DQ4	DQ28 (DQ36)	DQ12	DQ20 (DQ44)	DQ20	DQ12 (DQ52)	DQ28	DQ4 (DQ60)
DQ5	DQ29 (DQ37)	DQ13	DQ21 (DQ45)	DQ21	DQ13 (DQ53)	DQ29	DQ5 (DQ61)
DQ6	DQ30 (DQ38)	DQ14	DQ22 (DQ46)	DQ22	DQ14 (DQ54)	DQ30	DQ6 (DQ62)
DQ7	DQ31 (DQ39)	DQ15	DQ23 (DQ47)	DQ23	DQ15 (DQ55)	DQ31	DQ7 (DQ63)
DBI0	DBI3 (DBI4)	DBI1	DBI2 (DBI5)	DBI2	DBI1 (DBI6)	DBI3	DBI0 (DBI7)
EDC0	EDC3 (EDC4)	EDC1	EDC2 (EDC5)	EDC2	EDC1 (EDC6)	EDC3	EDC0 (EDC7)

GDDR5 CLK Mapping			
WCK01	WCK23 (WCK45)	WCK23	WCK01 (WCK67)
WCK01#	WCK23# (WCK45#)	WCK23#	WCK01# (WCK67#)
CK	CK		
CK#	CK#		

Others			
MF	MF	SEN	SEN
ZQ	ZQ	RESET#	RESET#

Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

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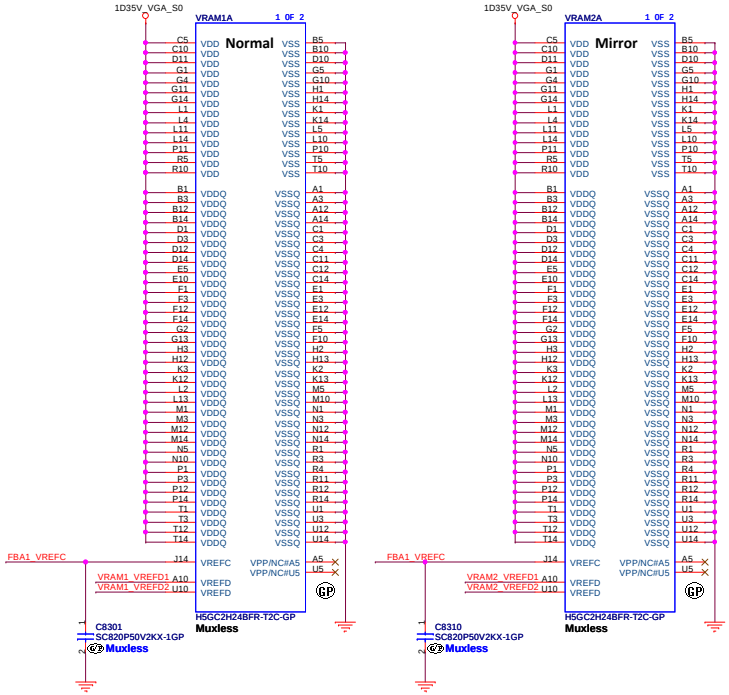
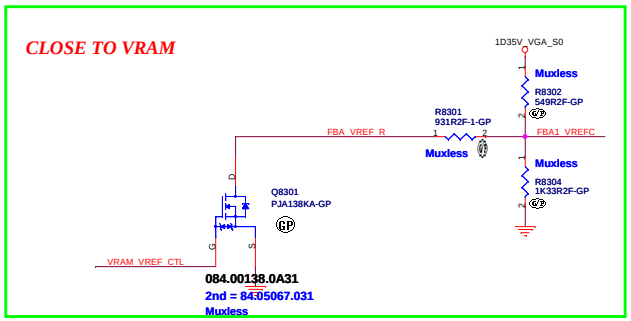
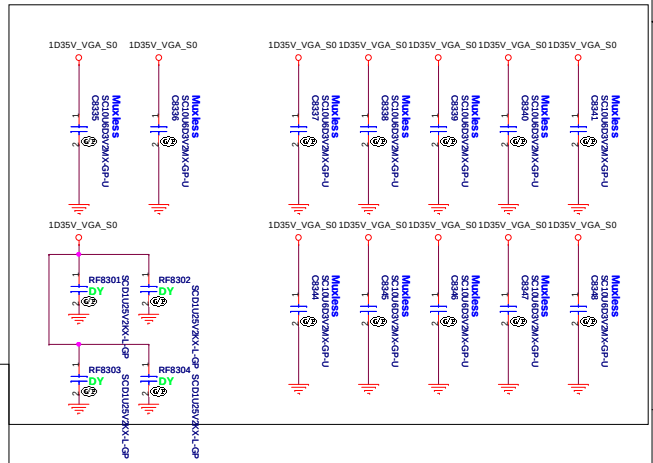
[79,84] VRAM_VREF_CTL



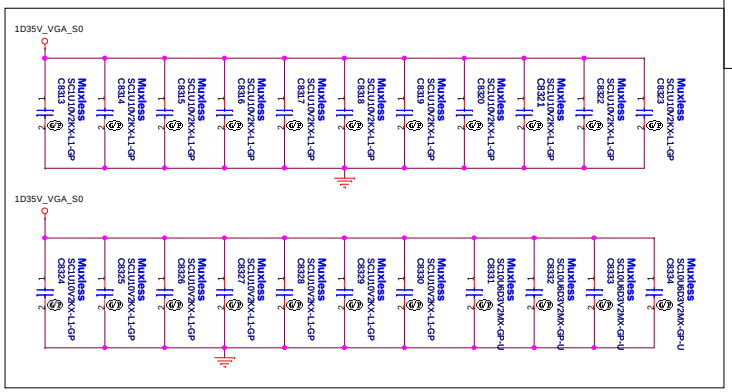
FOR VRAM1/ VRAM2



FOR VRAM1/ VRAM2



CLOSE TO THE MEMORY



UNDER THE MEMORY

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Title	***VRAM 5,6 (3/4)***	
Size: Custom	Document Number: **Buzz_KBL**	Rev: **2**
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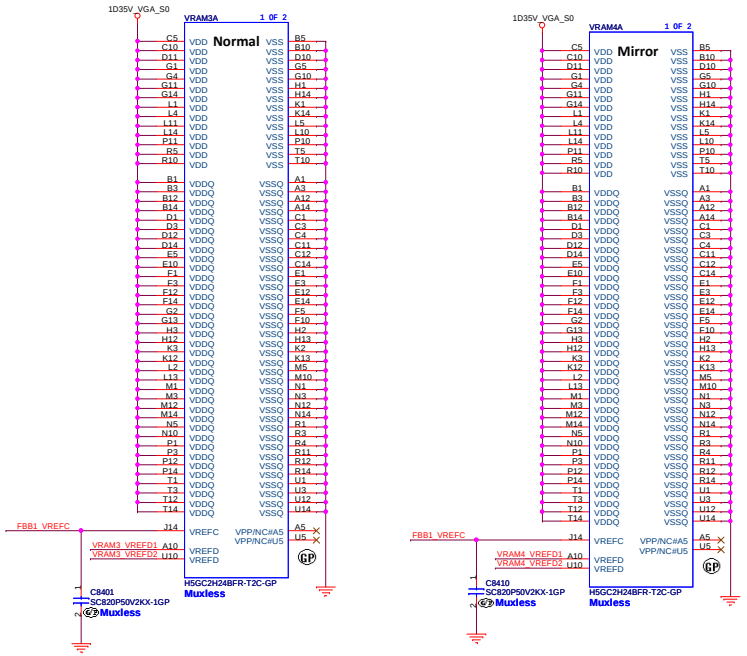
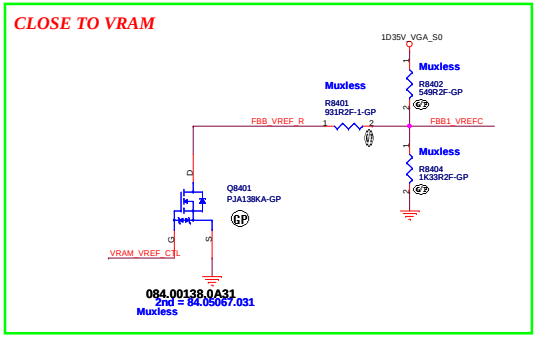
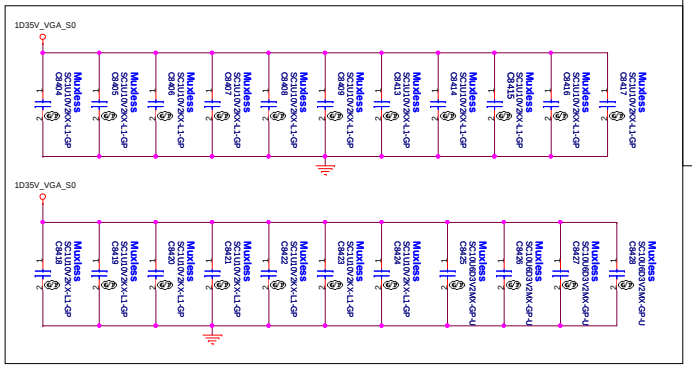
[79,83] VRAM_VREF_CTL

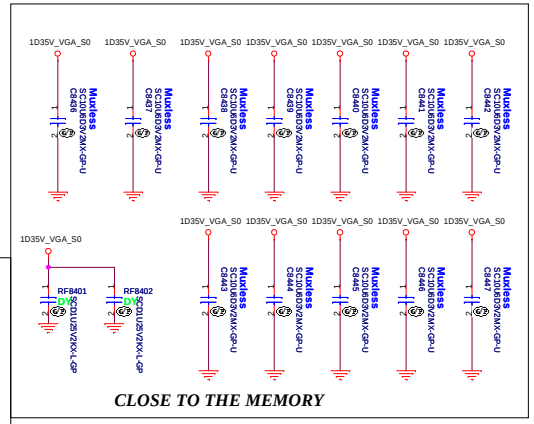




FOR VRAM3/ VRAM4

UNDER TO THE MEMORY





CLOSE TO THE MEMORY

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Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Number of Voltage Levels M	level	160
PWM Frequency F_{PWM}	KHz	675
PWM Minimum Pulse Width T_{OWB}	ns	9.26
VID Transient Time T	us	>100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	9.09
C	nF	1.47

N17 P-G0
EDP-Continuous : 38 A
EDP-Peak : 84 A

N16 950M
EDP-Continuous : 30 A
EDP-Peak : 53 A

RT8816A For NVVDDS

N17 P-G0
EDP-Continuous : 13 A
EDP-Peak : 16 A

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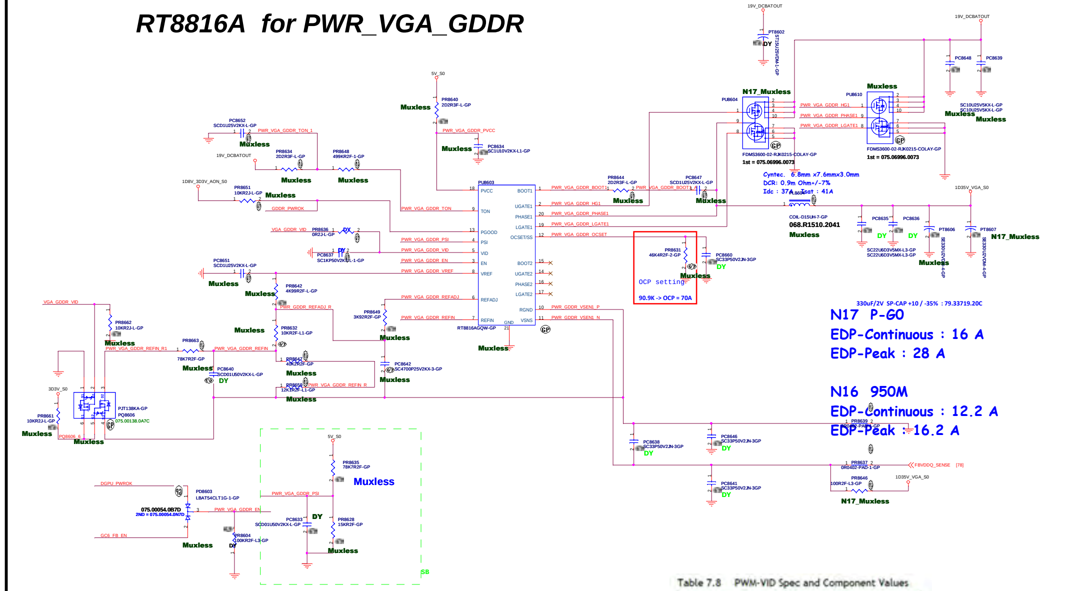


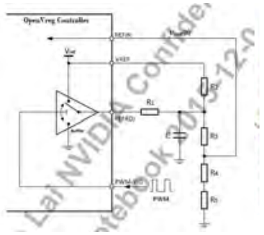
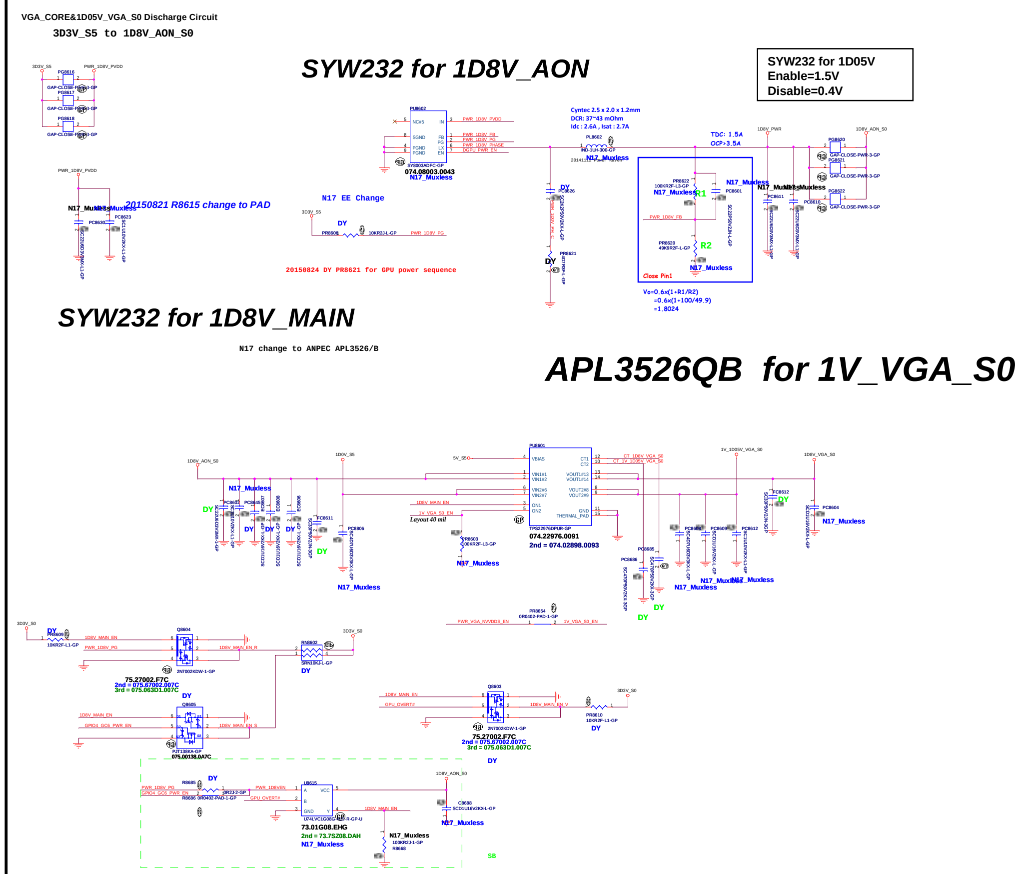


Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width $T_{(MIN)}$	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7



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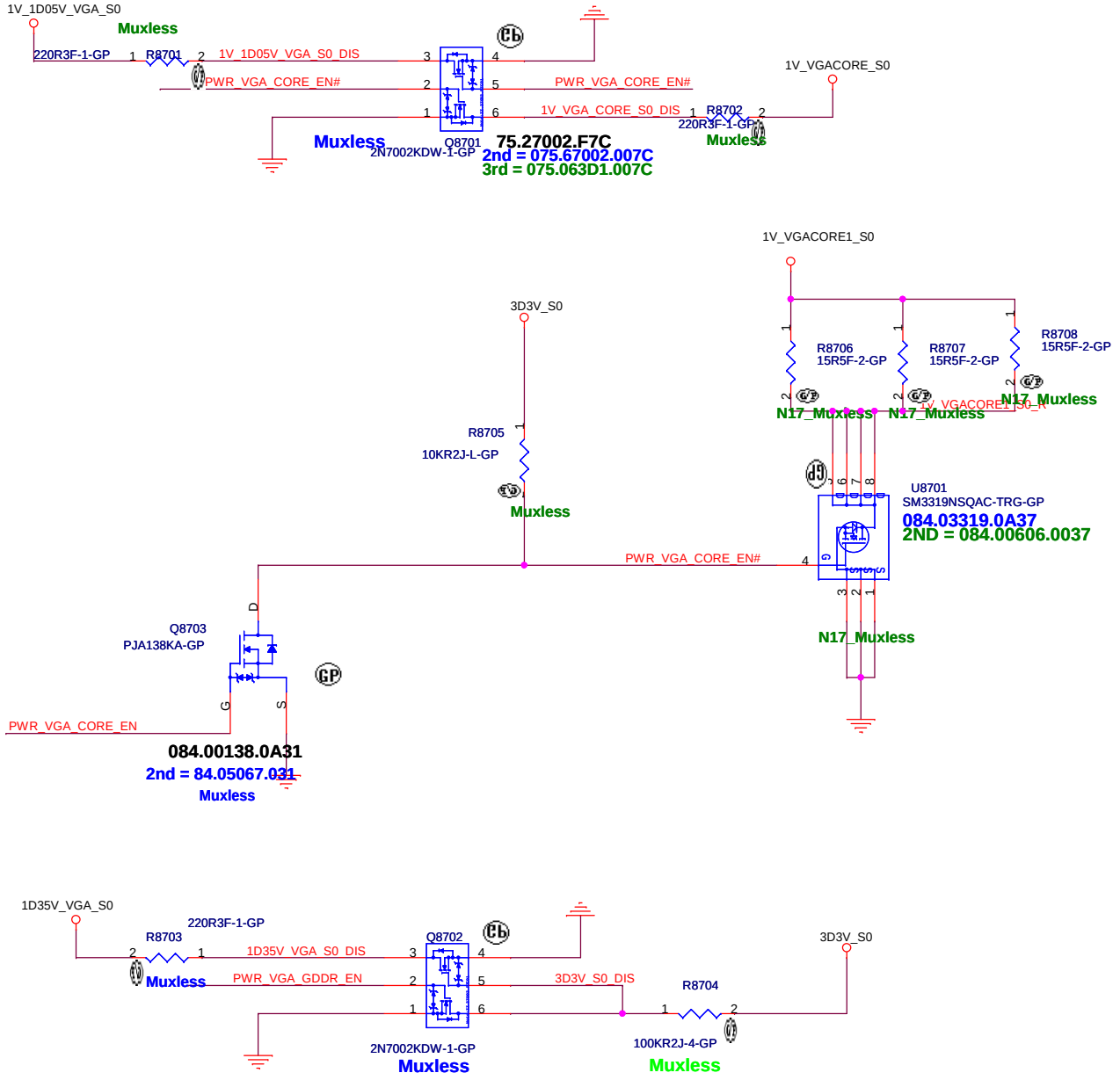

DIS

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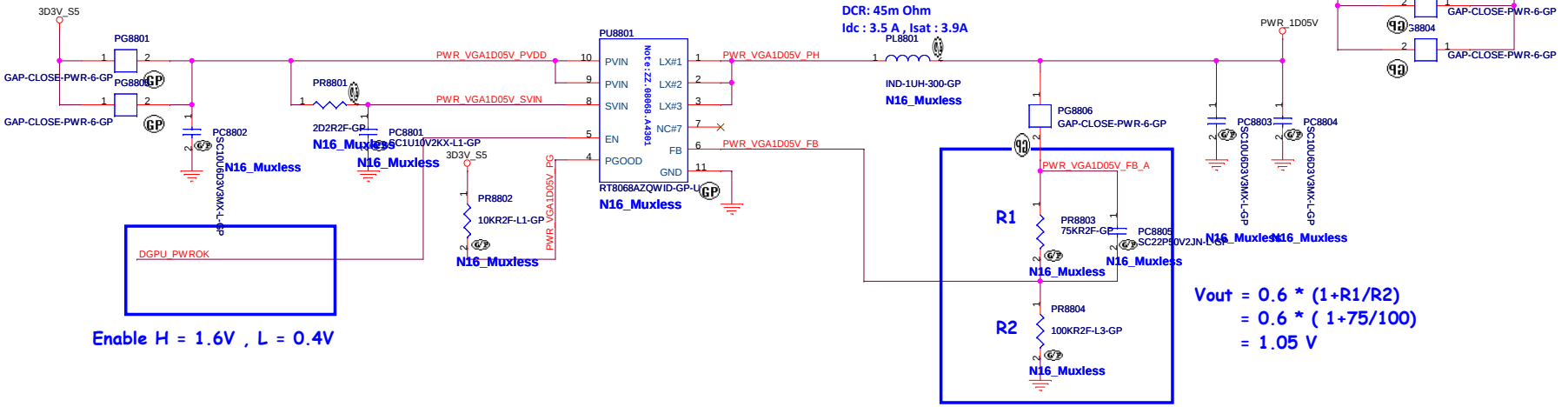
[6] DGPU_PWR_EN#
[24,76,85,86] DGPU_PWROK
[6,79,86] GC6_FB_EN
[79,86] GPIO4_GC6_PWR_EN
[86] DGPU_PWR_EN

1D05V_VGA_S0

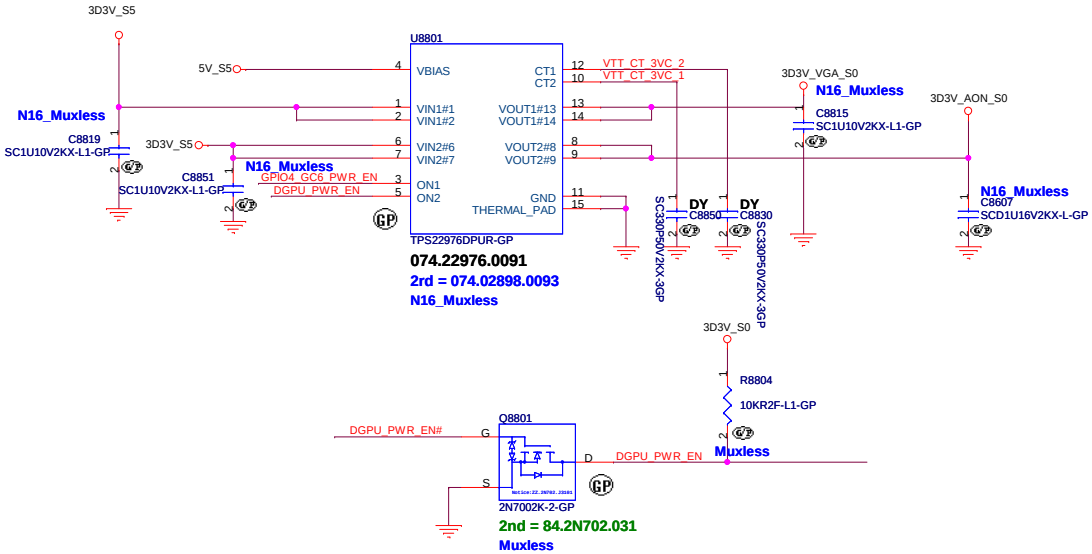
Freq = 1M Hz

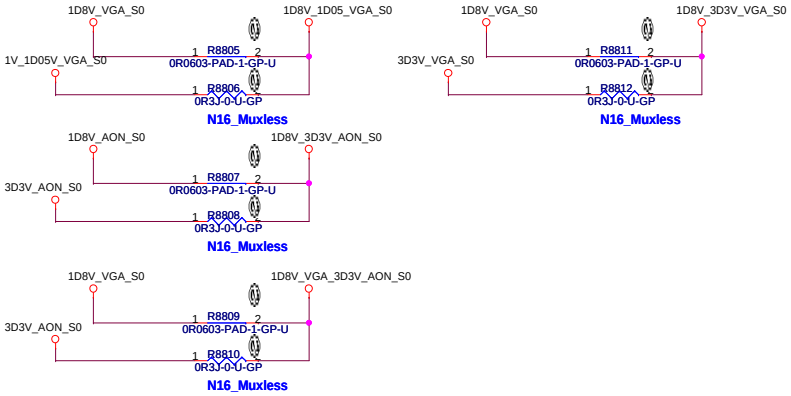


Enable H = 1.6V , L = 0.4V

Vout = 0.6 * (1+R1/R2)
= 0.6 * (1+75/100)
= 1.05 V

3D3V_S5 to 3D3V_VGA_S0





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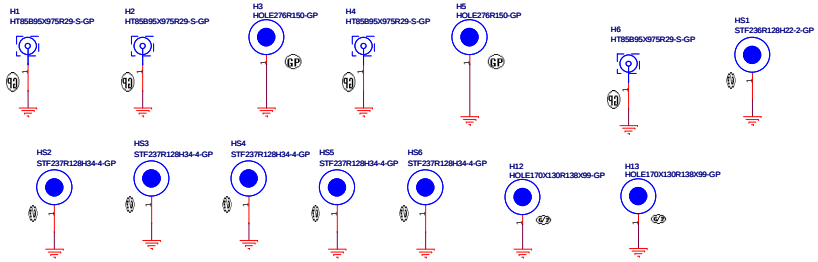
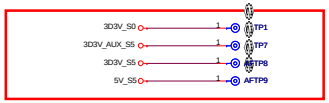
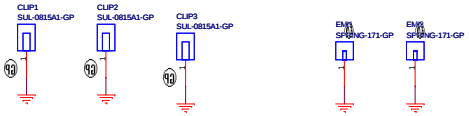
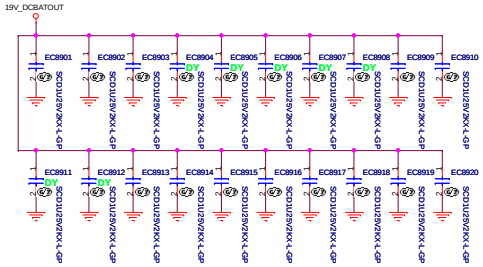


Check test point

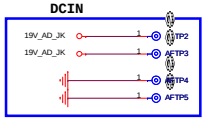


Top side

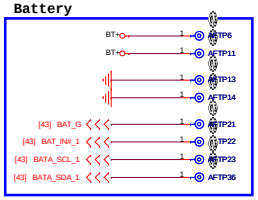




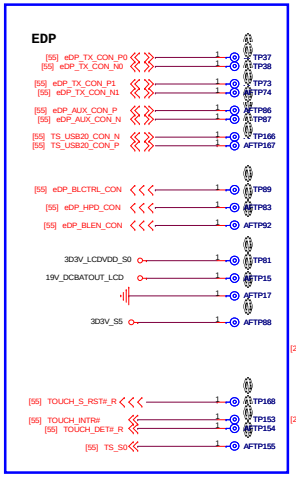
DCIN



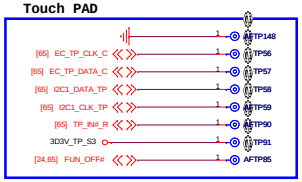
Battery



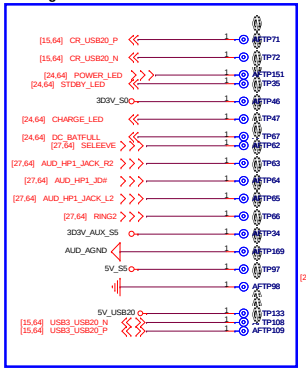
EDP



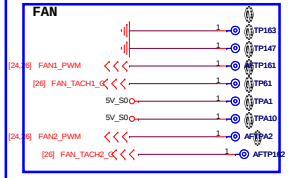
Touch PAD



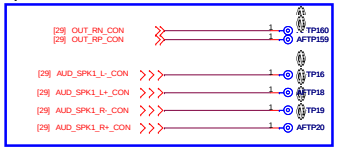
Daughter BD



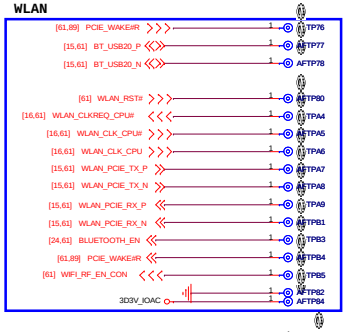
FAN



Speaker

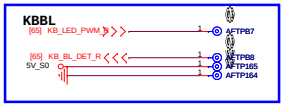


WLAN

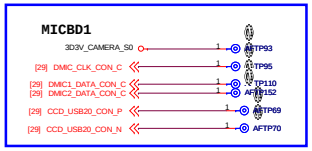


[20,24,61,62,68,79,91] PLT_RST# — AFTPB6

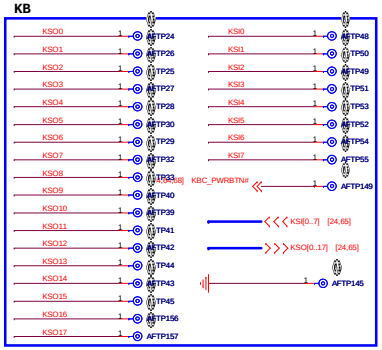
KBBL



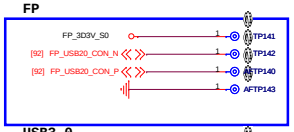
MICBD1



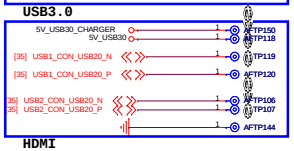
KB



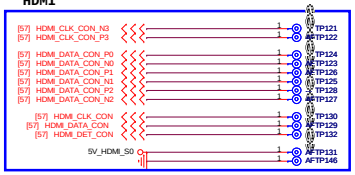
FP



USB3.0



HDMI



EMI Soluation

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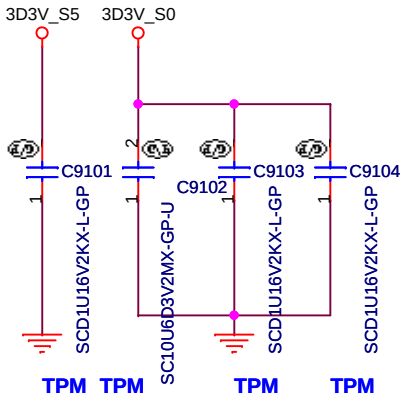
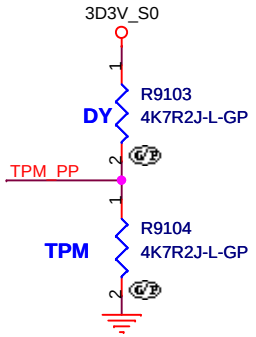
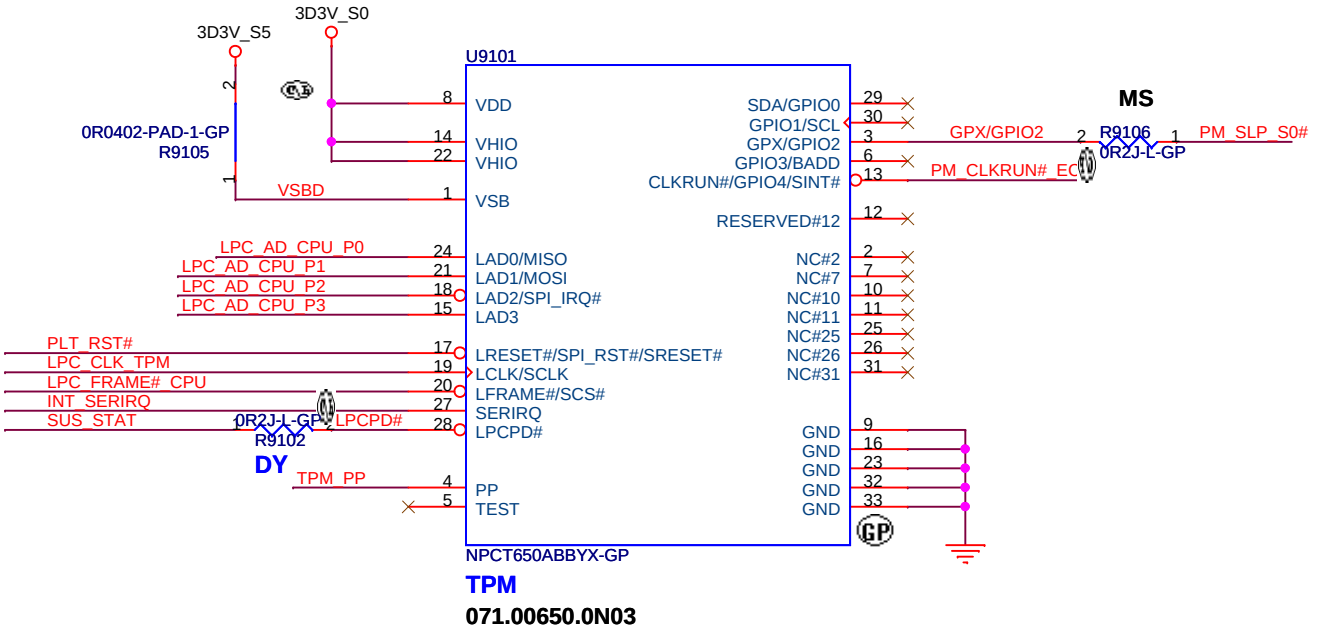
[18,24,68] LPC_AD_CPU_P0
[18,24,68] LPC_AD_CPU_P1
[18,24,68] LPC_AD_CPU_P2
[18,24,68] LPC_AD_CPU_P3

[18] LPC_CLK_TPM
[18,24,68] LPC_FRAME#_CPU
[20,24,61,62,68,79,89] PLT_RST#
[18,24,68] INT_SERIRQ
[18,24] PM_CLKRUN#_EC
[18] SUS_STAT
[20,40,60] PM_SLP_S0#







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[15] FP_USB20_N

[15] FP_USB20_P

[89] FP_USB20_CON_N

[89] FP_USB20_CON_P

3D3V_S0 — R9201 — FP_3D3V_S0

1 2

0R0603-PAD-1-GP-U

FP_3D3V_S0

FP_USB20_CON_P

FP_USB20_CON_N

FP1

10 8 7 6 5 4 3 2 1 9

FP

PTWO-CON8-17-GP

SB

020.K0312.0008

2nd = 20.K0481.008

0R0402-PAD-1-GP

FP_USB20_P R9202 1 2 FP_USB20_CON_P

0R0402-PAD-1-GP

FP_USB20_N R9203 1 2 FP_USB20_CON_N

FP

EU9201

FP_USB20_CON_P 1 I/O1 I/O4 6 FP_USB20_CON_N

2 GND VDD 5 5V_S0

3 I/O2 I/O3 4

AZC099-04S-2-GP

075.09904.0A7C

2nd = 075.01256.007C

3rd = 75.09904.07C

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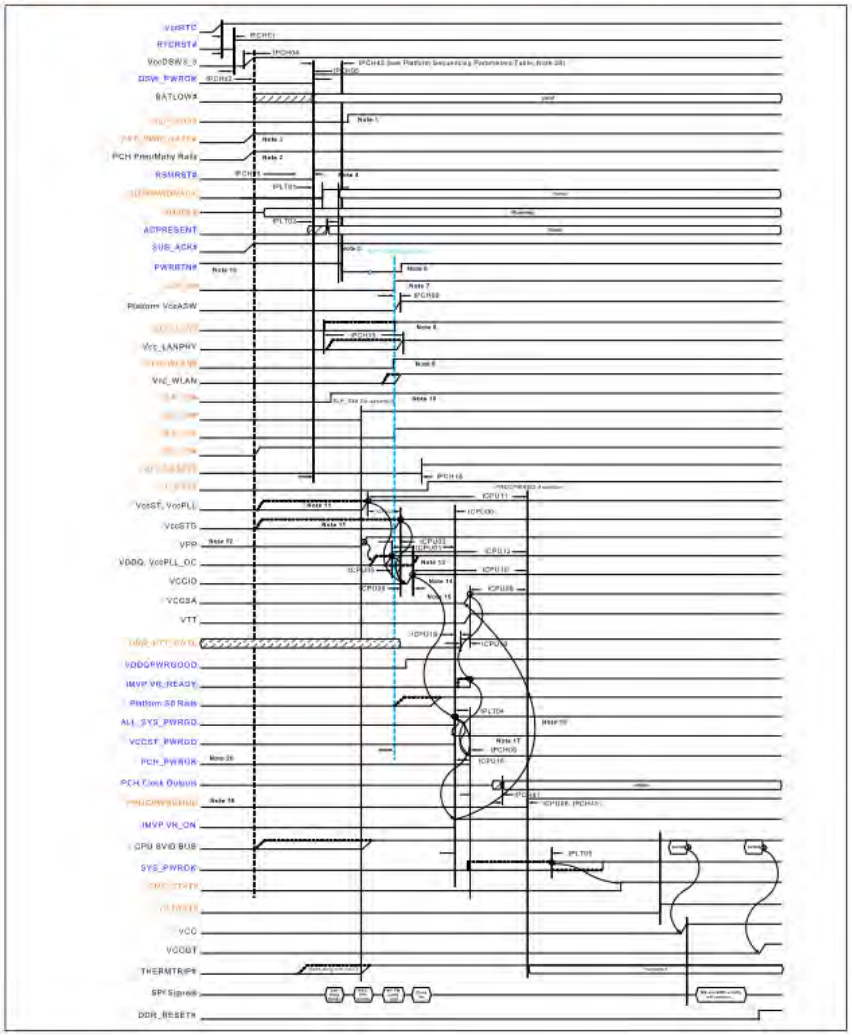
Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)



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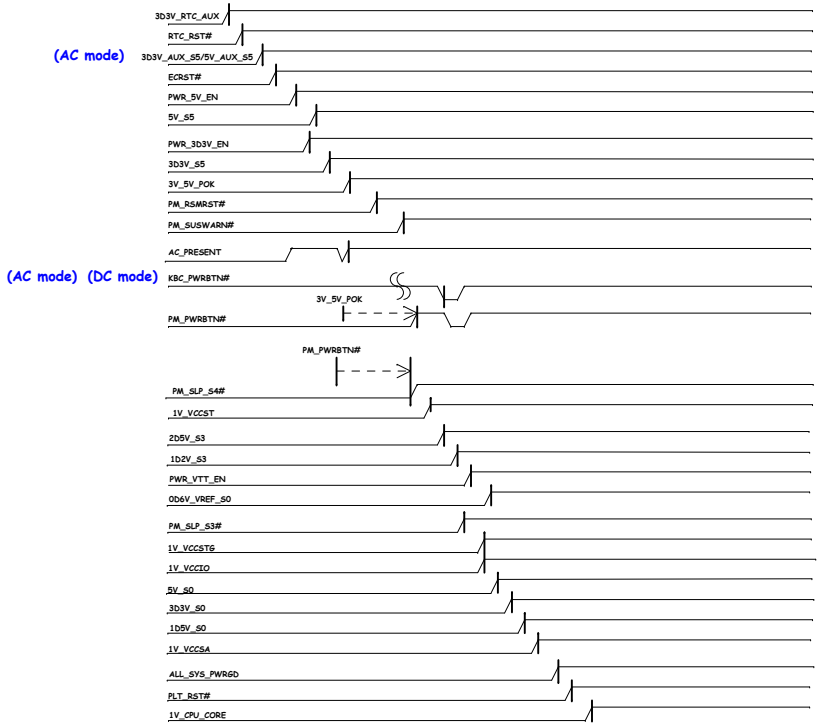
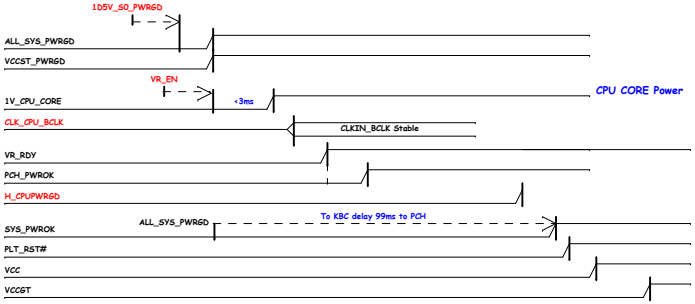
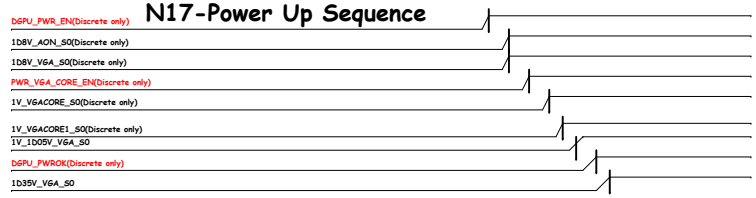
Intel-Power Up Sequence

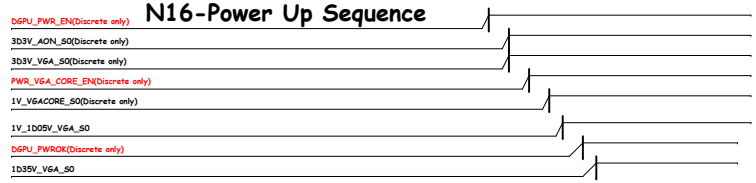


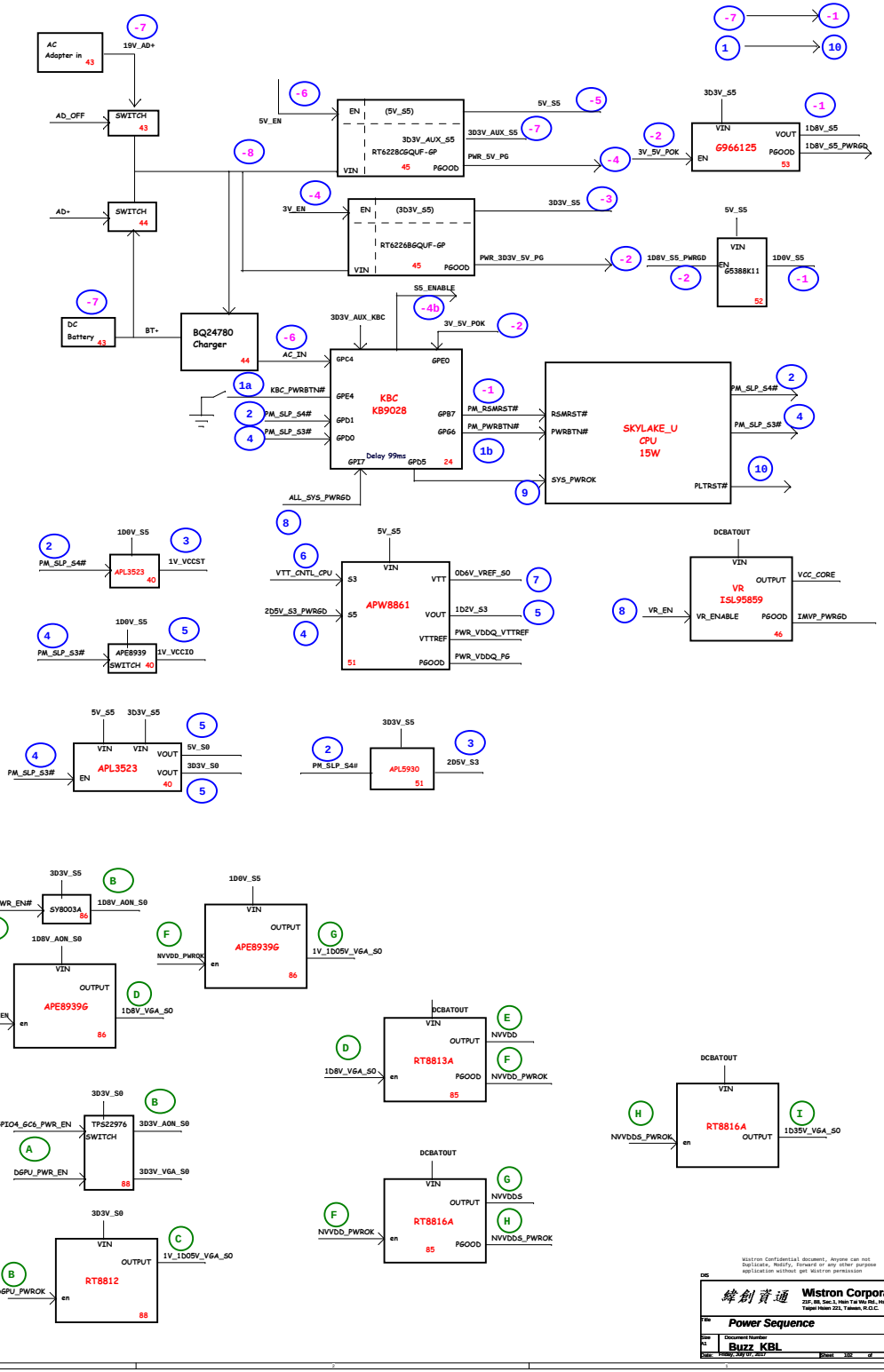


N17-Power Up Sequence



N16-Power Up Sequence





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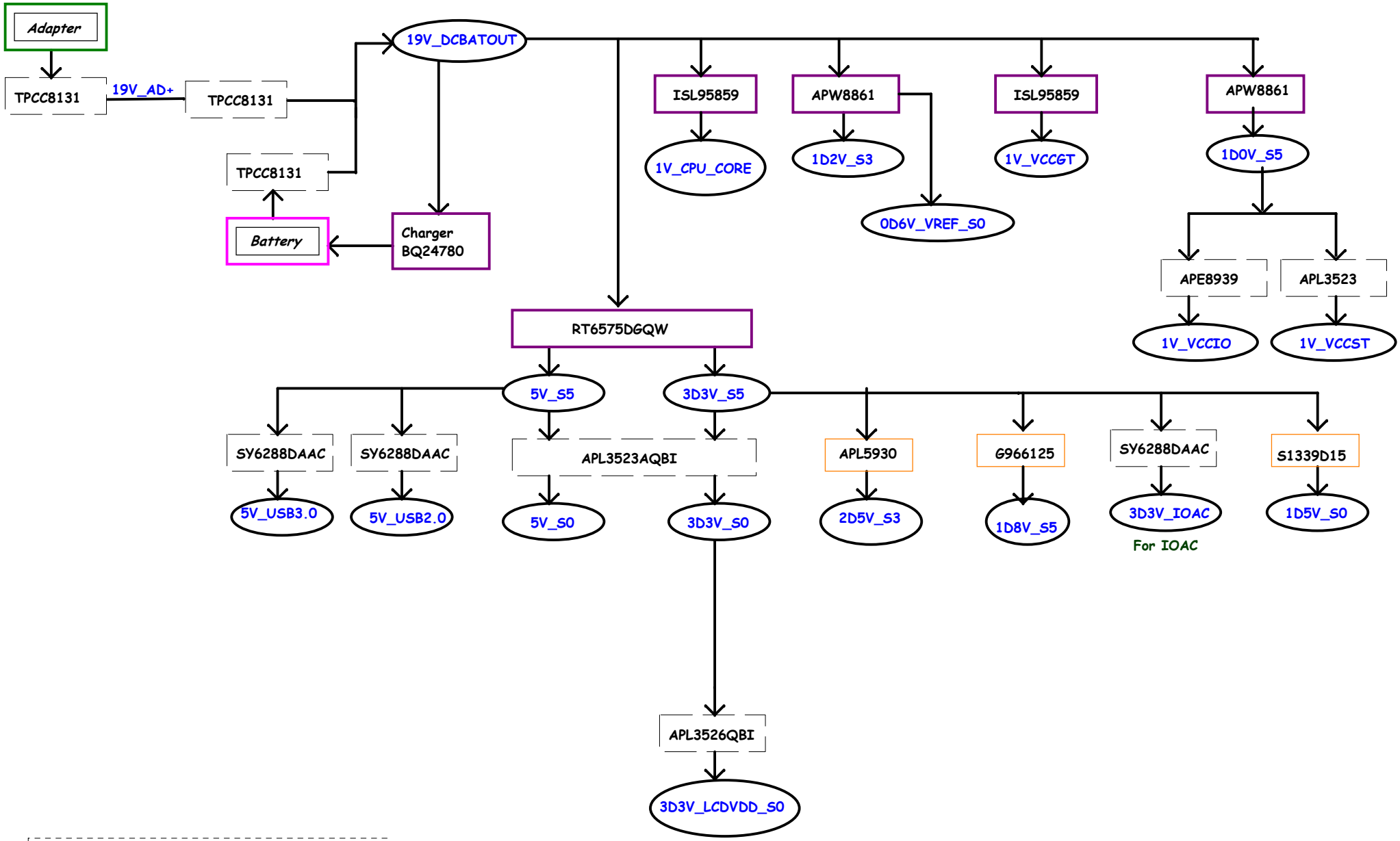

Power Shape

Regulator | LDO | Switch

DIS

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Title: **Power Block Diagram**

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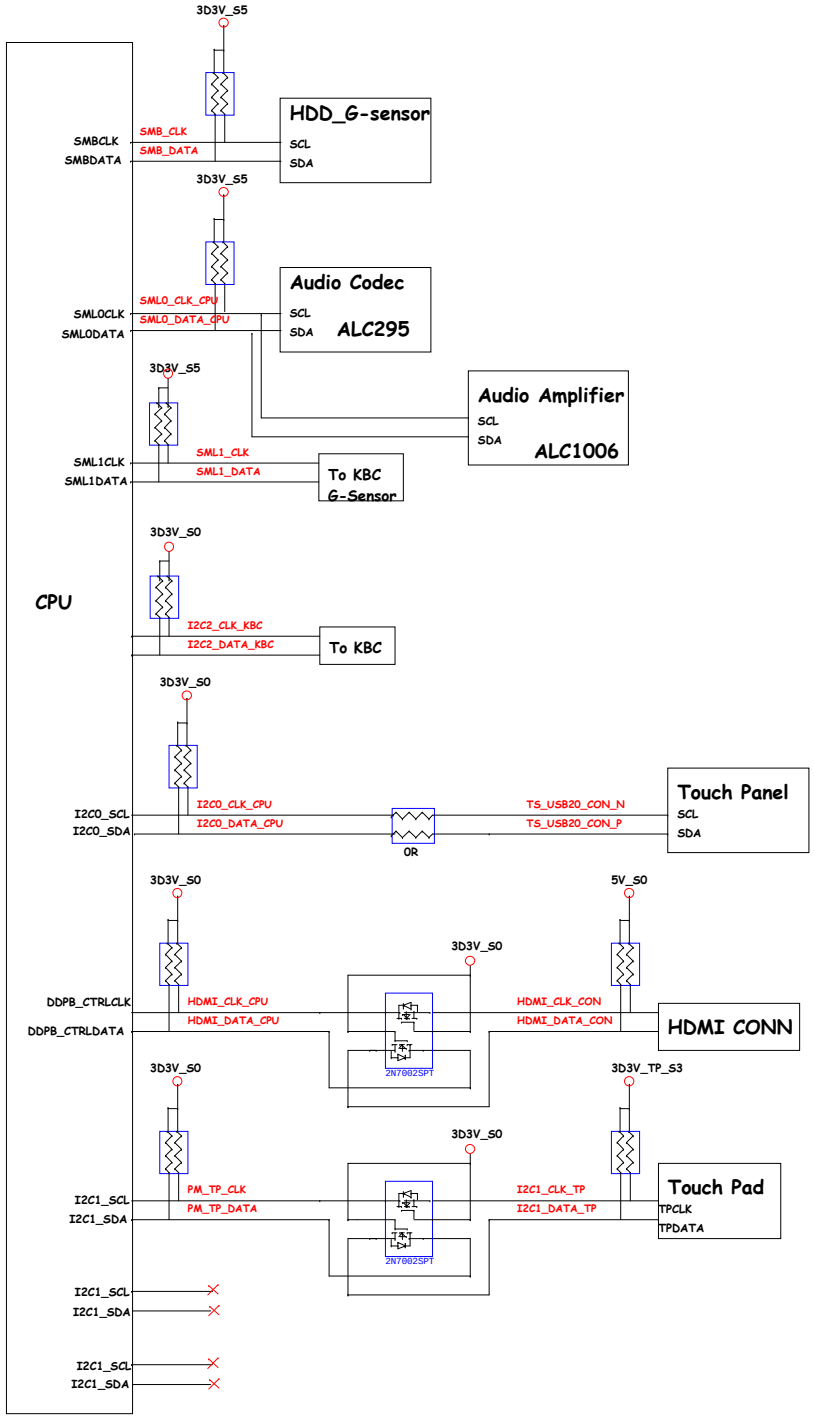
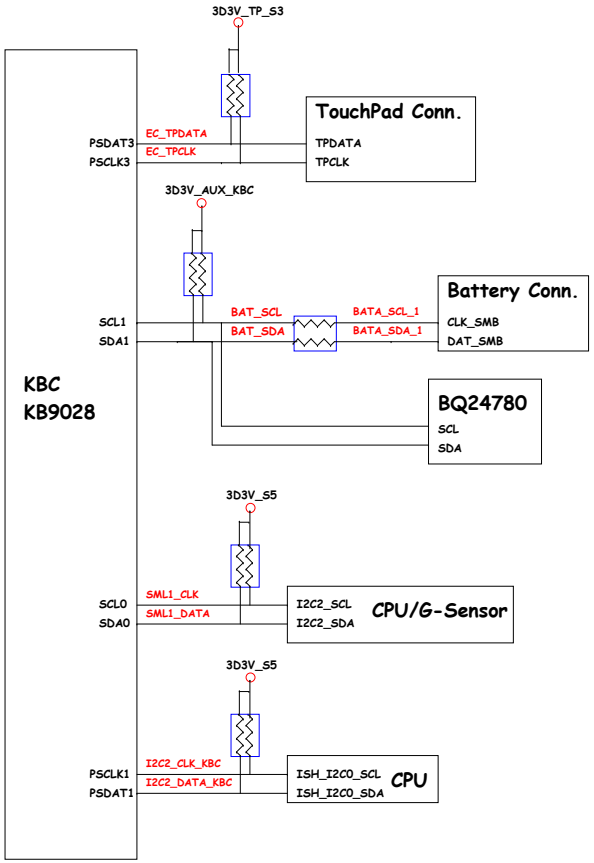
PCH SMBus/I2C Block Diagram



KBC SMBus/I2C Block Diagram



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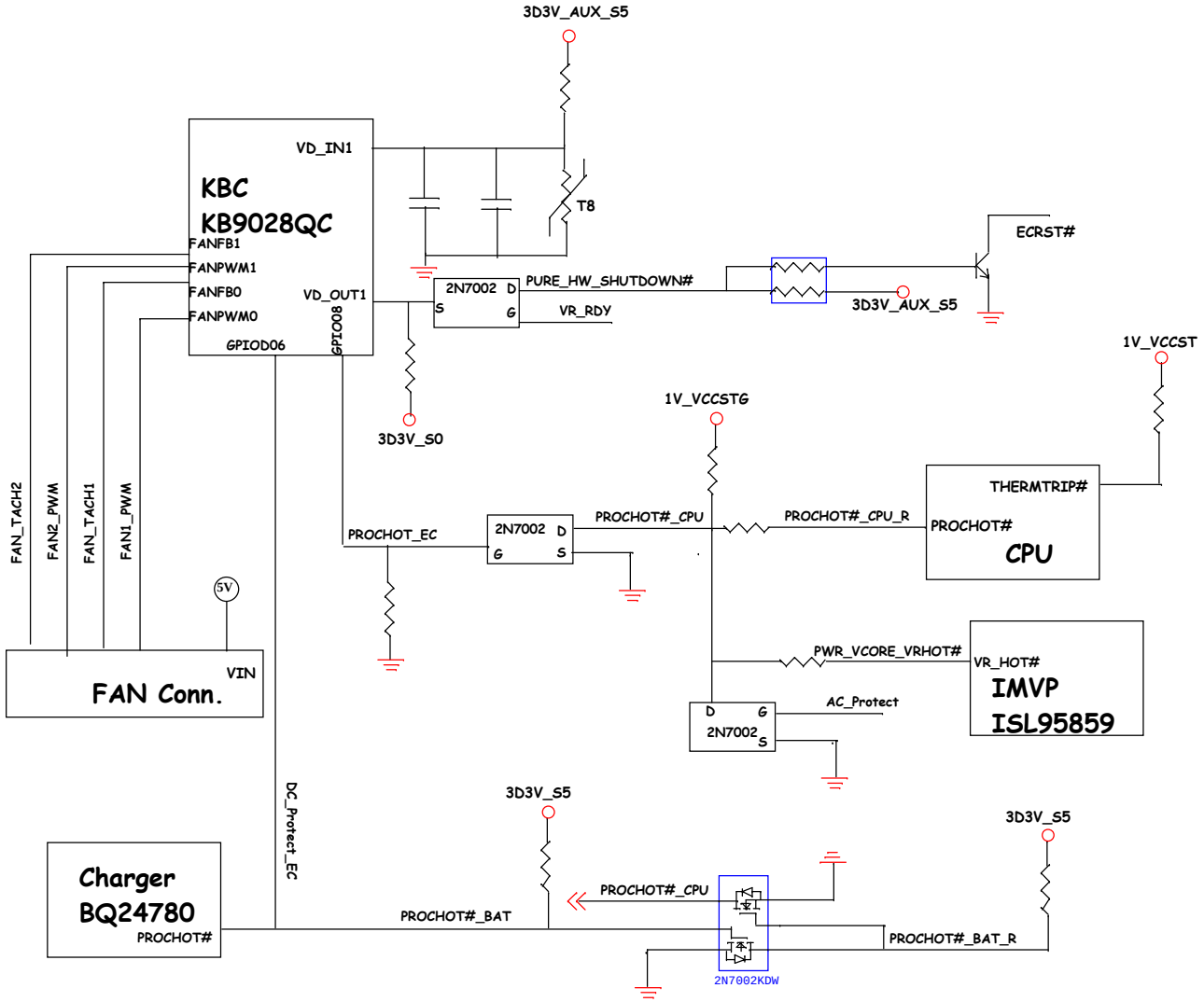
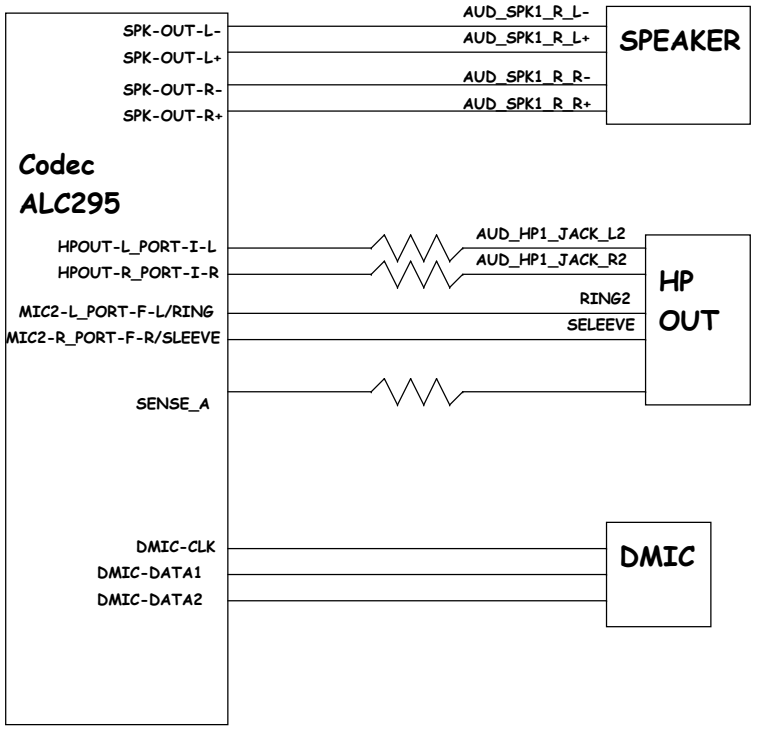
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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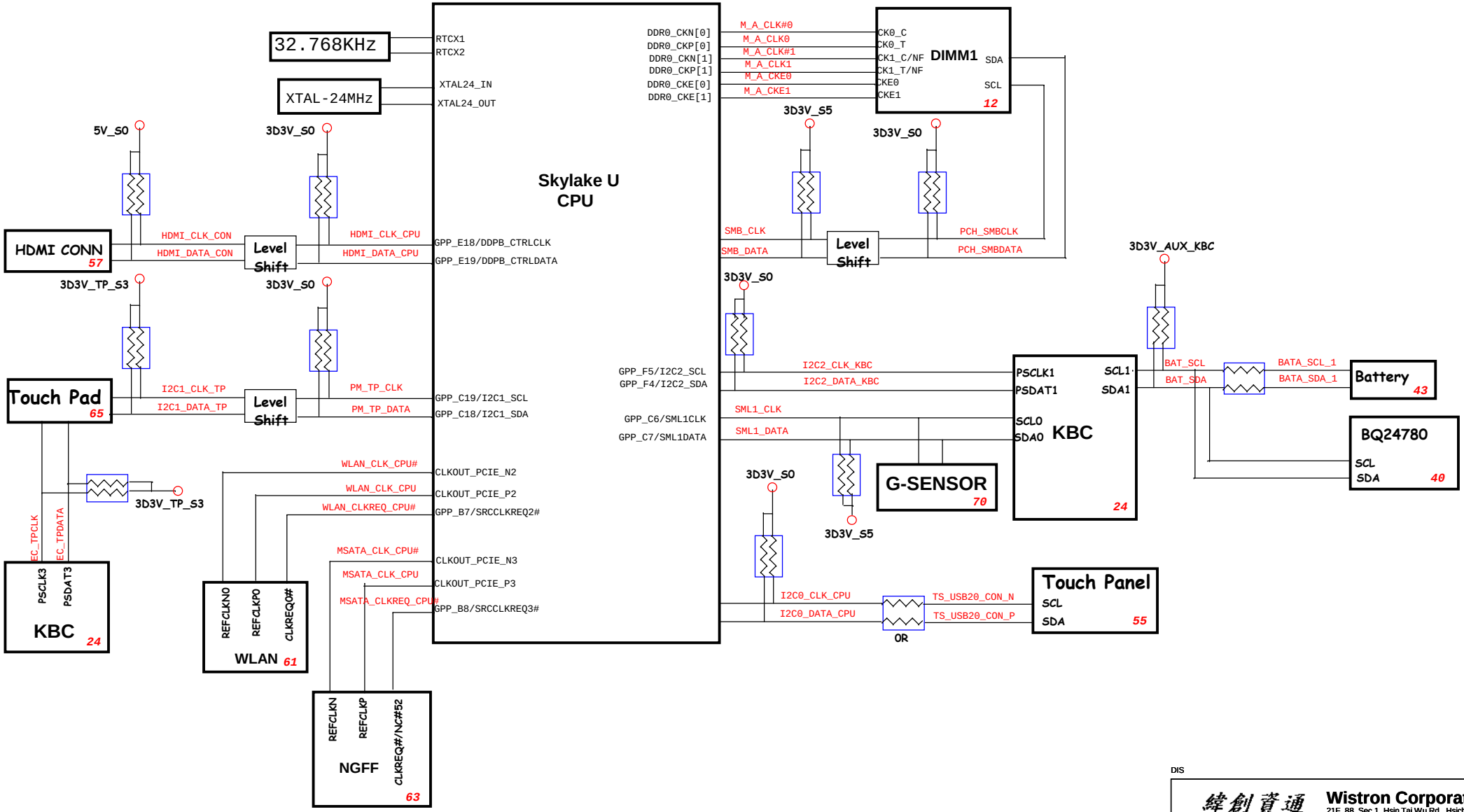
CLOCK BLOCK DIAGRAM



DIS

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